Combining FPGAs and RF: A New SDR Design & Test Methodology

Presented by:

Agilent Technologies
A New SDR Design & Test Methodology Presentation Overview

– **Mixed-Signal Design Challenges**
  - System Design Flow Challenges - *several teams, disconnected tools*

– **Algorithm Level Development**
  - Algorithm Design and Exploration

– **Transmitter Design and Circuit Co-Simulation**
  - Mixed-Signal Simulation: HDL - RF Transmitter - RF Circuit Co-Simulation

– **Receiver Design and Mixed-Signal Verification**
  - WiMax BER vs. Receiver LO Phase Noise & ADC Jitter

This presentation will be dealing primarily with the PHY (Physical Layer) of the radio. It will present new design flow methods that will provide enhanced interaction and verification between all areas of the SDR development team.
A Brief Note About this Presentation

• Note: This paper is a continuation of the Agilent SDR webinar paper entitled “Simulation and Design of SDRs”, which covered the following topics:
  • SDR Overview & Challenges
  • Comparing RF interference susceptibility of FPGA 16 QAM waveform to a Mobile WiMAX™ COTS waveform
  • FPGA Implementation and Test of an OFMDA Mobile WiMAX Waveform

An archived version of this webinar can be viewed at: http://www.techonline.com/learning/webinar/202403894

Or contact your local Agilent representative for more details
Mixed-Signal Challenges: System Design Tradeoffs

Mixed-Signal Application Examples:
• PAs (polar loop, DPD)
• Direct conversion receivers and A/D converters

Considerations:
• Sampling Rates and Bitwidth
• Key Algorithms
• RF Gain, Linearity, NF
• Channel Impairments and Interferers
System Design Tradeoffs- Performance Budgeting

System Design Tradeoffs for EVM & BER/PER

- With SDR having such high performance targets every part of the transmit and receive chain becomes critical to the link budget
- So how to decide the optimum balance?

Diagram with sections:
- RF Upconverter/Downconverter
- LOs (Phase Noise)
- Baseband HW Bitwidth
- Channel Compensation
- PA Nonlinearities
- RF Channel

Bits In → Coding Algorithms → D/A → Tx → Rx → A/D → Decoding Algorithms → Bits Out
System Design Flow Challenges

...several teams, disconnected tools
Agenda

• Mixed-Signal Design Challenges
• **Algorithm Design**
• Transmitter Design and Circuit Co-Simulation
• Receiver Design and Mixed-Signal Verification
• Summary
Algorithm Design and Exploration- Agilent SystemVue

SystemVue

- Algorithm Design
- System Architecture

Wireless Libraries

- Partition
- Refine

- Functional Design
- Component Firmware Design

- Component Verification

- System Verification

- Prototype Verification
- Production

- Integrate
- Verify
SystemVue Algorithm Exploration

• Probe frequency and time domain characteristics throughout design stages

• Evaluate fixed-point effects
HDL Code Generation

```vhdl
-- Automatically generated VHDL code for non-primitive component
-- Modulator_OFDM.vhd

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
library work;
use work.p_fxp.all;

-- declare Modulator_OFDM entity
entity Modulator_OFDM is

    port
    (
        Clock : in std_logic;
        InpO : in std_logic_vector(1-1 downto 0);
        Inp0Enable : in std_logic;
        OutO : out std_logic_vector(17-1 downto 0);
        Out0_Rdy : out std_logic;
        RST : in std_logic
    );

-- end of entity Modulator_OFDM
end Modulator_OFDM;
```

© Agilent Technologies, Inc. 2008
SystemVue Example- WiMAX™ IQ Modulator

WiMAX IQ
Data from ADS
Wireless Library

Export HDL with HDS

“WiMAX,” “Mobile WiMAX” and “WiMAX Forum” are trademarks of the WiMAX Forum®
FPGA Implementation and Test Flow Used

- IQ Data
- Verify HDL Code with ADS + VSA SW
- HDL Code
- FPGA Synthesis Tool(s)

Run Simulation Inside of Instruments to Create Software-Defined Instruments

Software-Defined Instruments with ADS Installed (Custom Application Example - ADS not Shipped with Equipment)

- Logic Analyzer With ADS
- MXA Signal Analyzer with ADS
- Infinium Scope with ADS
- MXG / ESG
Mobile WiMAX FPGA Implementation Test Setup

MXA Signal Analyzer with VSA SW and ADS

ESG to Clock FPGA Board

16900 Logic Analyzer with VSA SW and ADS

FPGA Board (DUT)
Agenda

• Mixed-Signal Design Challenges
• Algorithm Design
• **Transmitter Design and Circuit Co-Simulation**
• Receiver Design and Mixed-Signal Verification
• Summary
RF Design and Verification
Agilent ADS and Wireless Libraries
Agilent ADS for RF Design & Verification

Simulated and real world signal inputs

RF/Analog Subsystem

Transistor-level

RF sub-System Designer

RF Circuit Designer

Implementation

Design

Verification

ADS Ptolemy Top Level

Simulated and real world analysis

ESG / MXG → DUT → MXA → PSA → Infiniium → Logic Analyzer
Multiple Methods to Simulate FPGA Effects along with RF

EVM @ Receiver Output is ~ 1.2%

Transfer captured FPGA signal to ADS

or HDL Co-Sim

or MATLAB® Co-Sim

UpConverter

Transmitter Design

Signal Path

RF Design with Digitized IQ

Analog Devices
AD9433_105
Mobile WiMAX Source: Co-Simulate FPGA HDL

Bring FPGA HDL into ADS to Co-Simulate

FPGA Source EVM 0.74%

UpConverter
Transmitter Design
Signal Path
RF Design with Digitized IQ

Analog Devices
AD9433_105
RF Transmitter Co-Simulation

Circuit Level Co-Sim

HDL Co_sim

UpConverter

Mixer

Transmitter Design

Transmitter

VGA

NCO Bit Width Effects on Transmit Spectrum
Mixed-Signal Simulation: Add RF Circuit to RF Transmitter and FPGA HDL Co-Simulation

Circuit Level
Non-Linear
Co-Simulation

Circuit Envelope
System Level
Co-Simulation

Synthesized
Bandpass Filter

Behavioral
Mixer

UpConverter
Transmitter
Design
Signal Path
RF Design with Digitized IQ

Analog Devices
AD9433_105
Mixed-Signal Simulation: Circuit Co-Simulation

Decoded WiMax Data

Note the Gain Expansion and AM to PM from the Power Amp

Transmitter Gain and Phase Change vs. Output Power

Transmitter Output Spectra (dBm)

Just a few of the close-in mixer products are displayed
Mixed-Signal Simulation: Peak to Average Power Measurements

OFDM signals have a very high Peak to Average Ratio

Transmitter running in the Linear Region

Running in Saturation

Preamble Data
Agenda

- Mixed-Signal Design Challenges
- Algorithm Design
- Transmitter Design and Circuit Co-Simulation
- Receiver Design and Mixed-Signal Verification
- Summary
Receiver Design: WiMAX BER vs. EbNo

RF Receiver Design with Digitized IQ

- Swept EbNo
- Phase Noise vs. Freq. Offset
- Analog to Digital Converter Models

Delay
WiMAX BER vs. EbNo vs. Phase Noise (64 QAM)

Receiver BER vs EbNo vs. Swept Phase Noise

-60 dBc/Hz @ 10kHz offset
-85 dBc/Hz @ 10kHz offset
-70 dBc/Hz @ 10kHz offset
WiMAX BER vs. EbNo vs. Phase Noise
(QPSK, 16 QAM, 64 QAM)
WiMAX BER vs. EbNo vs. ADC Jitter (64 QAM)
WiMAX BER vs. EbNo vs. ADC Jitter (QPSK, 16 QAM, 64 QAM)

Receiver BER vs EbNo vs. ADC Jitter (QPSK)  Receiver BER vs EbNo vs. ADC Jitter (16QAM)

Receiver BER vs EbNo vs. ADC Jitter

© Agilent Technologies, Inc. 2008
SDR’s Flexibility

- Interoperability
  - One radio with ability to communicate with everyone.
Other ADS COTS Wireless Libraries
http://eesof.tm.agilent.com/products/wireless_libraries.html

- CDMA
- GSM
- DTV
- 3GPP WCDMA
- CDMA2000
- EDGE
- WLAN
- CDMA2000 1XEV
- TDSDMA
- HSPA
- Fixed WiMAX
- Mobile WiMAX
- 802.11n
- WiMedia
- 3GPP LTE
End-to-End System BER: Upconverter, Transmitter, Signal Path, Receiver, ADCs

SystemVue

HDL Generated with SystemVue HDS3

Sweep Jitter on Analog to Digital Converter Models

FPGA Target
RF Amplifier
End-to-End System BER Simulation Results
Upconverter, Transmitter, Signal Path, Receiver, ADCs

System BER vs. ADC Clock Jitter

Bit Error Rate (% BER)

Percent Jitter (% of ADC Clock Period)
A New SDR Design & Test Methodology Summary:

- **Mixed-Signal Design Challenges**
  - The various SDR component development teams need to work together

- **Algorithm Level Development**
  - Using Agilent‘s SystemVue as an HDL development tool

- **Transmitter Design and Circuit Co-Simulation**
  - Mixed-Signal Simulation: HDL - RF Transmitter - RF Circuit Co-Simulation

- **Receiver Design and Mixed-Signal Verification**
  - Evaluating WiMax BER vs. Receiver LO Phase Noise & ADC Jitter
Additional SDR References


Contact your local Agilent representative for more details
Thank You !