<table>
<thead>
<tr>
<th>Time</th>
<th>Agenda</th>
<th>Presenter</th>
</tr>
</thead>
<tbody>
<tr>
<td>9:30 - 10:00</td>
<td>Registration &amp; Continental Breakfast</td>
<td></td>
</tr>
<tr>
<td>10:00 - 10:30</td>
<td>Welcome and keynote presentation - A methodology for predictable design closure in the high speed digital era</td>
<td>Dave Wilton</td>
</tr>
<tr>
<td>10:30 – 11:30</td>
<td>Anticipate SI issues on your High Speed Digital PCBs using Virtual Prototypes and Advanced Channel Simulation for early evaluation and optimization of design trade-offs</td>
<td>Nilesh Kamdar</td>
</tr>
<tr>
<td>11:30 – 12:30</td>
<td>How to characterize and debug high-speed digital links on your physical prototype. What part of your design is eating up your eye margins?</td>
<td>Russ McHugh</td>
</tr>
<tr>
<td>12:30 – 2:00</td>
<td>Question &amp; Answer Lunch Product &amp; Application Demos Giveaway</td>
<td></td>
</tr>
</tbody>
</table>
**Speaker Bios**

**Dave Wilton** is the WW field leader at Agilent for High-Speed Digital Design Solutions. He joined Agilent in 2012 following a lengthy EDA background at Synopsys and has over 19 years of experience in the field of Semiconductor/FPGA Electronic Systems design and debug at both the technical and business levels. Dave’s mission is to connect practical HSD solutions spanning initial design, through debug, and onto compliance with our customer’s business objectives to reduce prototype development cost, shorten debug cycle, improve TTM or to improve competitiveness through enhanced low power and system performance. With his Engineering background combined with years of commercial Account Management experience, already he has successfully consulted with several International Companies to assist them with getting robust High Speed Digital products to market on time. Dave graduated in 1995 from University of Bath and l’INPG in Grenoble with a Masters Degree in Electronics and Communications Engineering.

**Nilesh Kamdar** is Senior Applications Engineer at Agilent Technologies. Nilesh has over 14 years of experience working on high frequency and high speed digital design. He managed the Simulation Architecture team at Agilent EEsof in his previous role. Nilesh received his Masters of Science degree in Electrical Engineering from Utah State University in 1999.

**Russ McHugh** has worked for Agilent Technologies/Hewlett-Packard for 27 years in the areas of high speed digital and analog test, measurement automation, custom systems, and data acquisition, as an Application Engineer and Systems Engineer. He is the author of “Understanding the Effects of Limited Bandwidth Channels on Digital Signals” in the Agilent Measurement Journal, “How Best to Measure SSC on Data” in Evaluation Engineering, and a coauthor of “Total Jitter Measurement at Low Probability Levels, Using Optimized BERT Scan Method”, DesignCon 2005. He has a bachelor and a master degree in mechanical engineering from Stanford University. His hobbies include auto racing, fine wines, cooking and travel.
See the “Cliff Edge”

(Or: A methodology for predictable design closure in the high speed digital era)

Dave Wilton
WW Business Development Manager, HSD solutions
November 2013
Keynote Agenda

Why are we here?

Methodologies for design and verification of HSD designs

From Simulation to Compliance test

Summary
Interconnect goes serial, fast, and multi-standard

What are your companies’ business drivers?

- Reduce cost
- Increase density
- Reduce power consumption
- More robust
- Higher speed
- More features
- Faster time to market

<table>
<thead>
<tr>
<th>Protocol</th>
<th>Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB 3.0</td>
<td>4.8 Gb/s</td>
</tr>
<tr>
<td>HDMI</td>
<td>5 Gb/s</td>
</tr>
<tr>
<td>DVI</td>
<td>8 Gb/s</td>
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<tr>
<td>DP</td>
<td>8.6 Gb/s</td>
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<tr>
<td>PCIe</td>
<td>5 Gb/s</td>
</tr>
<tr>
<td>SATA</td>
<td>3 Gb/s</td>
</tr>
<tr>
<td>DDR3</td>
<td>0.8-2.133 Gb/s</td>
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</table>
Signal Integrity is critical...
...Protocol is now of secondary importance

Would you like a beer?

什麼是英語的人在談論什麼？？
**Signal Integrity engineering challenges**

Need microwave techniques to prevent eye closure and BER

For 60 cm interconnect @ 1Gb/s
- Flight time ~ 4ns
- Bit period = 1ns

Implies 4 bits in transit = No time for reflections: Match impedances

![Diagram showing interconnect impedance and matching outputs](image)

**But Impedance problems are everywhere**

- Backplanes
- Connectors
- PC Boards/DIMMS
- IC Packages / DDR
- Cables
High-speed PCB challenges - Impact of Bandwidth

FR4 is common, low cost and easy to manufacture

BUT at multi GB/s it’s like wet string!

3.125 Gb/s
6.25 Gb/s
12.5 Gb/s
Introducing the “cliff edge”!
See the “cliff edge” - Speed and power margins
Keynote Agenda

Why are we here?

Methodologies for design and verification of HSD designs

From Simulation to Compliance test

Summary
Why don’t our designs work first time?

System Design → Interconnect Design → Analysis Debug → Compliance Test

Are we done yet?
What were the HSD Challenges on Your Last Design?

- SI issues or lack of margin visibility (eg. Jitter, collapsed "eyes")
- Problems probing signals
- Power Integrity (eg. Rail bounce, ground plane instability)
- EMI / EMC
- Missing skills /"know-how" on HSD design
- Lack of simulation models and/or accuracy
- Other
- Difficulty w compliance
- Couldn’t correlate models/simulations to HW
- Inherent jitter/noise of test equipment meant wasted design margins

Source 2013 EMEA HSD seminars.
Data size: 411 respondents

2/3rds of last designs required 1 or more respins due to SI issues
The business issues

Cost of a prototype respin:

- Cost of proto board build = $10k x 100 = $1M
- Extra Engineering time (2 months) = $100k/yr x 2 mths x 10 people = $170k
- Additional emergency test equipment rental = $200k
  - Total $1.4M.

Time to Market (TTM) – Cost of being late:

Risk:

- Are we done testing? How do we know?
- Can we fulfil compliance test?
- What happens after 1M units of component variation?
What were the HSD Challenges on Your Last Design?

- SI issues or lack of margin visibility (e.g., Jitter, collapsed "eyes")
- Power Integrity (e.g., Rail bounce, ground plane instability)
- Missing skills / "know-how" on HSD design
- Lack of simulation models and/or accuracy
- Problems probing signals
- Other
- Difficulty w/ compliance
- Couldn’t correlate models/simulations to HW
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Agilent HSD solution for predictable design closure

- **System Design**
  - Build accurate Models
  - Accurate Simulation

- **Interconnect Design**
  - Refine Models & Simulations
  - Accurate Design Analysis
  - Correlation

- **Active Signal Analysis**
  - Accurate Design Analysis
  - Measurement Automation
  - Debug
  - Correlation

- **Compliance Test**
  - Stress test
  - Protocol test
  - Measurement Automation
  - Compliance

**HSD Design**: To optimise mutually exclusive cost, power consumption and robustness tradeoffs

**HSD Lab Verification**: To prove trade-off decisions through margin analysis and compliance test
Channel Simulation with Agilent ADS

- Fast to Extremely Fast AND Accurate
- Waveforms/BER/Bathtubs
- Electrical & Optical S-parameters from EM/ VNA/ TDR/ LCA
- Easy to explore DSP vs. Channel
The importance of accurate Measurement

- Safe design margin
- Measurement system contribution

Easier correlation!
+ Your competitive advantage!

Agilent's 5000 Q-series Oscilloscope
Real-time Bandwidth: 4 channels @ 33 GHz, 2 channels @ 63 GHz

Differentiating Technology...
- High bandwidth np chipset
- Agilent's proprietary "HB2B Process"
- Proprietary epitaxial material
- Packaged in Agilent’s proprietary "QuickFilm" modules

Enables Differentiating Performance...
- Analog bandwidth to 63 GHz
- Industry leading low-noise and superior signal integrity

In The World's Fastest and Most Accurate Scope...

Agilent Technologies
Why this test case?
- Models not available, unusual routing, diff pair + single-ended.

We must be able to detect the signal integrity problems using simulations.

Differential pair MGH_DIA
- Length: 190 mm
- Width of the trace: w=130 µm
- Width of the via: d=150 µm
- Spacing between P & N channels: s=155 µm
- Embedded microstrip on layers 2 & 3

Single-ended SS
- Length: 160 mm

Comparison simulations vs measurements

➔ MGH_DIA2 without single-ended aggressor (MGH_DIA1 active)
  - Data rate: 1 Gbps
  - Pattern: PRBS7
  - VOD: 800 mV

Jitter Separation processed with Agilent’s Infiniview

Simulation
Measurement
Agilent DSA-X 93204A 33 GHz

Despite the inability of simulating the PJ, the correlation is quite good.
Effect of predictable design closure

Target spec.
eg. BER, power, cost

Bigger risk margin

Build visibility of “cliff edge” through Virtual Prototype.
Target power/ cost /speed /robustness

Development time

TTM saving

Typical HW Prototype only design process
Virtual and Physical prototype process
Why Did Cisco Choose ADS For Signal Integrity?

“Our systems include multi-gigabit per second chip-to-chip serial links across PCBs and backplanes. We selected ADS because it lets us couple simulations at the channel-, circuit-, and physical-levels with measured data from the instruments.

“The resulting workflow requires fewer respins of the physical prototypes. We get fewer unwanted surprises, and get to market quicker.”

-- Straty Argyrakis, CPP Integrity Engineer, Cisco Systems
What were the HSD Challenges on Your Last Design?

- SI issues or lack of margin visibility (e.g., Jitter, collapsed "eyes")
- Power Integrity (e.g., Rail bounce, ground plane instability)
- Problems probing signals
- SI issues or lack of margin visibility (e.g., Jitter, collapsed "eyes")
- Lack of simulation models and/or accuracy
- Missing skills /"know-how" on HSD design
- Inherent jitter/noise of test equipment meant wasted design margins
- Difficulty w/ compliance
- Couldn't correlate models/simulations to HW
- Other

Agilent Technologies
The importance of accurate Models

- Component Models (IC Interface & Physical Channel)
- Simulation Engine
- Simulated Performance

<table>
<thead>
<tr>
<th>IC Models</th>
<th>Connector / Cable Models</th>
<th>PCB Models</th>
</tr>
</thead>
<tbody>
<tr>
<td>IBIS</td>
<td>S-param Models</td>
<td>S-param Models</td>
</tr>
<tr>
<td>Encrypted Hspice</td>
<td>Mechanical data</td>
<td>PCB Layout data</td>
</tr>
<tr>
<td>IBIS AMI</td>
<td>Materials data</td>
<td>Materials/Stack-up data</td>
</tr>
<tr>
<td>Verilog AMS</td>
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<td></td>
</tr>
</tbody>
</table>
Creating accurate S-parameter Models

• Pre-Layout Simulation Model - Based on Analytic or Simple 2D EM Based

• Post-Layout Simulation Model – Based on EM Simulation

• Post Manufacture Simulation Model – Based on VNA Measurements
More coming up in part 2!

2) Anticipate SI issues on your high-speed digital PCBs using virtual prototypes and advanced channel simulation for early evaluation and optimization of design trade-offs

Nilesh Kamdar,
Applications Engineer, Agilent EEsof EDA
What were the HSD Challenges on Your Last Design?

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- Missing skills / "know-how" on HSD design
- Lack of simulation models and/or accuracy
- Problems probing signals
- Other
- couldn’t correlate models/simulations to HW
- Difficulty w/ compliance
- Inherent jitter/noise of test equipment meant wasted design margins
De-embedding:
- Removes the effects of the measurement system + probes
- Use S-parameter model of the probing system
- Special solution for DDR!

Embedding:
- Is the reverse – emulate the effects of an interconnect or channel, trace, etc.
- Use S-parameter model from EMPro or measured from ENA/TDR

Another idea!:
- Change reference plane by re-characterising receiver card from connector (BERT)
Real Example - De-embedding DDR2 BGA Probe

NB. Actually need this to comply with JEDEC Spec! (measure at solder balls)
2) Probe signal through BGA interposer

3) De-embed BGA Interposer s2p file using InfiniiSim

1) Probing Reference signal at VIA
More coming up in part 3!

3) How to characterize and debug high-speed digital links on your physical prototype. What part of your design is eating up your eye margins?

Russ McHugh,
Senior Application Engineer,
High Speed Digital and Analog Test
Keynote Agenda

Why are we here?

Methodologies for design and verification of HSD designs

From Simulation to Compliance test

Summary
Compliance test - will optimised design still work when we build it?

System Design | Interconnect Design | Analysis Debug | Compliance Test

Protocol-based Analysis tools

SI Analysis

High Speed Channel Design

Package and Board Level Simulation
We know Standards Compliance

Our solutions are driven and supported by Agilent experts involved in international standards committees:

- JEDEC
  - Perry Keller
  - Jim Cholis
  - Thomas Dugan
- USB
  - Rick Eads
- HDMI
  - Rick Eads
  - Roland Schwenger
- PCI Express
  - Lightpeak Program
  - Andreas Gerster

PCI Express® 3.0 – Total Solution

Transmitter Test
- N9301C PCI Compliance Test Software
- USB3.0 or USB3.1 Compliance Test
- PCIe Gen 3

Interconnect Test
- IEEE 1149.1 Test Application
- PCIe Gen 3

Receiver Test
- PCIe Gen 3

Protocol Test
- PCIe Gen 3

Memory DDR3 – Total Solution

Active Signal Validation
- U2213A DDR 3 Compliance Test Software
- DDR3 1866 or 2133 Memory

Protocol Validation & Function Test
- FS2400 DDR3 Diagnostic Test Equipment
- DDR3 1866 or 2133 Memory

Agilent Technologies
Introducing 2014 HSD flow!
Design and Lab measurement - Share data easily
InfiniiView application

- InfiniiView scope analysis software to share measurement environment with designers.
- ADS users can import simulation data to compare in same environment.
What were the HSD Challenges on Your Last Design?

- SI issues or lack of margin visibility (e.g., Jitter, collapsed "eyes")
- Problems probing signals
- Power Integrity (e.g., Rail bounce, ground plane instability)
- Missing skills/"know-how" on HSD design
- Lack of simulation models and/or accuracy
- Other
- Protocol
- Difficulty w/ compliance
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Agilent HSD Technology Development Centers
A Global Presence to Support You

Santa Rosa, California
Colorado Springs
Boeblingen, Germany
Beijing, China
Santa Clara, California
Hachioji, Japan
Westlake Village, California
Alpharetta, Georgia
Ghent, Belgium
New Delhi, India
Agilent HSD Services & Support

- Local Language/Time Zone Technical Support
  - Telephone, email, web
- On-site Premium Support
  - Proactive support to help projects go smoothly
- Comprehensive Training Solution
  - Self-paced & live courses
- Consulting
  - Bridge the gap between product and application
HSD SI Design is a classic engineering trade off
Agilent tools and methodology helped solve this visibility challenge allowing xxx to see the “cliff edge” and create more robust design.

ROI: 6 weeks debug versus 6 months
Summary

- HSD designs create new problems for Digital Designers - We understand your challenges!
- Agilent Technologies is your design partner for HSD Design through to Compliance test!
- Our people can help you see the “Cliff Edge” and optimise your next design!
<table>
<thead>
<tr>
<th>Date</th>
<th>Technical Programs</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tuesday, Jan 28th</td>
<td>Hands-on Tutorial for Fixture Removal of 28Gbps Tx Measurements</td>
<td>Heidi Barnes(Agilent Technologies, Inc.), Mike Resso(Agilent Technologies, Inc.), Rob Sleight(Agilent Technologies, Inc.), Jack Carrel(Xilinx, Inc.), Romi Mayder(Xilinx, Inc.)</td>
</tr>
<tr>
<td></td>
<td>Battle on the Chip - Embed vs De-Embed?</td>
<td>Ransom Stephens(Ransom's Notes), Chris Loberg(Tektronix, Inc.), Eric Kvamme(LSI Corporation), Greg LeCheminant(Agilent Technologies, Inc.), Martin Miller(Teledyne LeCroy Corporation), Mike Li(Altera Corporation), Pavel Zivny(Tektronix, Inc.)</td>
</tr>
<tr>
<td>Wednesday, Jan 29th</td>
<td>Mechanism of Jitter Amplification in Clock Channels</td>
<td>Fangyi Rao(Agilent Technologies, Inc.), Sammy Hindi(Juniper Networks, Inc.)</td>
</tr>
<tr>
<td></td>
<td>Touchstone v2.0 SI/PI S-Parameter Models for Simultaneous Switching Noise (SSN) Analysis of DDR4 Memory Interface Applications</td>
<td>Romi Mayder(Xilinx, Inc.), Nilesh Kamdar(Agilent Technologies, Inc.), Raymond Anderson(Xilinx, Inc.)</td>
</tr>
<tr>
<td></td>
<td>Improving IBIS-AMI Model Accuracy: Model-to-Model and Model-to-Lab Correlation Case Studies</td>
<td>Yunong Gan(Broadcom Corporation), Dong Yang(Broadcom Corporation), Vivek Telang(Broadcom Corporation), Magesh Valliappan(Broadcom Corporation), Todd Westerhoff(SiSoft, Inc.), Fangyi Rao(Agilent Technologies, Inc.)</td>
</tr>
<tr>
<td></td>
<td>How PCB Design is Changing: Simulation and Design Techniques</td>
<td>Michael Dunn(EDN), Eric Bogatin(Bogatin Enterprises), Scott McMorrow(Teraspeed Consulting Group, LLC), Lee Ritchey(Speeding Edge), Filip Demuyck(Agilent Technologies, Inc.), David Wiens(Mentor Graphics, Inc.)</td>
</tr>
<tr>
<td>Thursday, Jan 30th</td>
<td>Modeling, Extraction and Verification of VCSEL Model for Optical IBIS AMI</td>
<td>Zhaokai Yuan(Agilent Technologies, Inc.), Ramana Murty(Avago Technologies, Ltd.), Amolak Badesha(Avago Technologies, Ltd.), Sanjeev Gupta(Avago Technologies, Ltd.)</td>
</tr>
<tr>
<td>Friday, Jan 31st</td>
<td>Higher Speed Ethernet: 40 Gb/s Operation Over Twisted-Pair Copper Cabling</td>
<td>Christopher DiMinico(MC Communications, Inc.), Mike Resso(Agilent Technologies, Inc.), Mike Sapozhnikov(Cisco Systems, Inc.), Ronald Nordin(Panduit Corporation)</td>
</tr>
<tr>
<td></td>
<td>De-Mystifying the 28 Gb/s SERDES Channel - Design to Measurement</td>
<td>Heidi Barnes(Agilent Technologies, Inc.), Mike Resso(Agilent Technologies, Inc.), Rob Sleight(Agilent Technologies, Inc.), Jack Carrel(Xilinx, Inc.), Hoss Hakimi(Xilinx, Inc.)</td>
</tr>
</tbody>
</table>
Thank you for attending

For more information on
High-Speed Digital Design and Verification

If you have a current need for a design and verification solution, you can request a quick quote, contact your field engineer, or call the Agilent Customer Care Center at the numbers below:

United States: 1-800-452-4844
Canada: 1-877-894-4414

www.agilent.com/find/hsd