# Keysight Logic and Protocol Analyzer Software (64-bit Application)

## Version 7.00.0086 (March 20, 2024)

### Modifications

- In DDR/LPDDR Post process Compliance Tool, improve display of limit value in the results tab when the limit varies by clock speed.
- Fix issue with display of refresh per bank for LPDDR4 in memory viewer. (TTS-72661)
- Remove DDR5 and LPDDR5 tests from Real-time Compliance Tool. They are no longer supported.

### Additions

- Support in all tools for protocol and measurement changes for LPDDR5X.
- Many new and updated LPDDR5/5X compliance measurements.
- Support in all tools for DRFM for LPDDR5/5X.
- Two new features in the Transaction Decode tab in the DDR/LPDDR Memory Viewer:
    - Allow exporting a range of transactions (rather than the entire trace).
    - Allow exporting the read/write data along with the transactions.

## Version 7.00.0050 (October 6, 2023)

### Modifications

- Many new and updated DDR5 compliance measurements.
- Fix issue with DDR Setup Assistant and the FP-FS2600. The selections available on the initial DDR Setup Assistant page were not working correctly.
- Fix bug with 16861A and transitional timing mode. Storage qualification options were not available in the trigger dialog.

### Additions

- Add support for LPDDR4 123-ball interposer.

## Version 7.00.0040 (June 16, 2023)

### Modifications

- Fix crash when saving a configuration file with a DDR/LPDDR Memory Viewer on the workspace, and particular data in the viewer. (TTS-54399)
- Removed the Logic Update Tool from the install process. It is obsolete.
- Fix problem with DDR/LPDDR Memory Viewer when computing GDDR6 data.
- Add new test to DDR/LPDDR Post-process Compliance Tool, measuring precharge to refresh (tRP).
- Fix defect in DDR/LPDDR Post-process Compliance Tool – exception when trying to load a saved project containing test results. (CSG-106044)

## Version 7.00.0031 (April 19, 2023)

### Modifications

- Fix issue with DDR/LPDDR memory viewer not correctly detecting clock speed changes in all cases.
- Fix for DDR5 in DDR/LPDDR memory viewer and DDR/LPDDR post-process compliance tool – correctly handle non-target ODT commands issued to a rank that is currently in powerdown mode.
- Add support in all tools for DDR5 solution consisting of FP-FS2600 DDR5 RDIMM interposer combined with FP-FS2605 DDR5 RDIMM satellite interposer.

## Version 7.00.0028 (March 28, 2023)

### Modifications

- Update to final version of licensing code.

## Version 7.00.0026 (March 16, 2023)

### Modifications

- Fix several LPDDR4 measurements in DDR/LPDDR Post Process Compliance Tool. (CSG-106044)
- Enhancements to DDR Setup Assistant:
    - Recognize and handle 2N timing in DDR5 for probes that do *not* have a clock divider and set 2N mode in all tools and viewers that require this setting.
    - Improve default values for prepend text for DDR5 configuration file load step.
    - Modify wording in the configuration load step to improve clarity.
    - New feature (beta at this time) to allow user running DDR Setup Assistant to automatically launch the DDR/LPDDR Post Process Compliance Tool to run the steps needed to validate CK/CS/CA tuning. This feature is available only for DDR5 setup at this time, but it will be added for other DDR/LPDDR types when the feature moves out of the beta phase.
- When the module name provides a hint, pre-select the DDR/LPDDR type selection when starting the DDR/LPDDR Post Process Configuration Tool.
- Update to latest version of licensing code.

### Additions

- Add beta feature in DDR Configuration Creator that allows users to create configurations for the ONFi memory viewer.

## Version 7.00.0022 (January 27, 2023)

### Modifications

- Add support for decode of MRR response for LPDDR5 even when DUT is changing system clock speeds.
- Updates and fixes to DDR5 configuration files for FP-FS2601, FP-FS2670, and BGA probes.
- Add configuration files and DDR Setup Assistant support for FP-FS2611.
- Fix defect in DDR Memory Viewer with handling of MRS commands when user has selected that there is only one active BG bit.
- Fix potential crash in DDR and ONFi Memory Viewers.

- Several corrections to DDR5 protocol compliance: 1) WR->RDA test updated to measure only when BG and bank match. 2) Update calculation of tRRD_L parameter value to be a clock (not time) value. This increases the accuracy of the measurement. 3) Fix WRToRD type tests to exclude measuring when the WR is a WR w/AP.
- Updates/fixes for DDR Setup Assistant's handling of DDR5 probes that are designed for use above 5GT/s (i.e., those with active clock divider circuitry). DDR Setup Assistant now correctly handles setting of CK/CS/CA sample positions when target is running in 1N or 2N modes.
- Fix to handling of "empty" bits – signals that are not probed but are expected by various tools to be assigned to different labels – in DDR Configuration Creator.

## Additions

- Add configuration files and DDR Setup Assistant support for FP-FS2611.

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## Version 7.00.0013 (September 19, 2022)

### Modifications

- Add configuration files and support in DDR Setup Assistant for FP-FS2660 and FP-FS2670 DDR5 RDIMM interposers.
- Fix problems with “Reconstructed Signals” window in DDR5 setups with probing solution that has a clock divider (FP-FS2670 and BGA 78-ball w/ clock divider).

## Version 7.00.0008 (August 22, 2022)

### Modifications

- Update all DDR/LPDDR tools to be current with latest LPDDR4 spec – JESD209-4D. This includes handling decode of new Refresh Management commands.
- Fix problems with handling of DDR5 MRR command in the DDR/LPDDR memory viewer. (CSG95192)

## Version 7.00.0007 (July 19, 2022)

### Modifications

- Fix issue with DDR5 4000 limits file that resulted in error when trying to edit limit values.
- Fix WRToRDASameBankGroup test. It should be to the same *bank*, not the same *bank group*. Updated it to work on bank, not bank group. (CSG-90176)
- Add configs and setup assistant support for Blossom x16 102-ball DDR5 probe.
- Add configs for FP-FS2603 DDR5 RDIMM CA-only probe.
- Fix tRFC1 and tRFC2 tests for DDR5 to exclude PDX from measurements, as per recent spec change.
- Update algorithm in DDR Setup Assistant for LPDDR5 eye placements for CK/CS/CA signals.
- Add new symbols for LPDDR5 configurations that represent either a MWR or Write.
- Simplify LPDDR5 real-time compliance trigger specs that measure to MWR or Write.
- For LPDDR5 compliance, change references to CAS latency and CAS write latency to read latency and write latency, respectively.

- Change default for bank group organization for LPDDR5 “Set Limits from System Parameters” dialog. It had been 8B mode, and now defaults to Bank Group.
- Update DDR5 parameters for lower speed bins (3200 to 4800), in both post-process compliance and real-time compliance tools, to match latest draft spec.