DDR5/LPDDR5 Design, Debug, Probing, and Validation Challenges and Solutions

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Jennie Grosslight,
Stephen Slater,
Agenda

- DDR5 Challenges / Solutions
- LPDDR5 Challenges / Solutions
- Probing Challenges / Solutions
- Simulation Challenges / Solutions

Summary
# How Did we Get to DDR5?

## A ROAD PAVED BY INNOVATION

<table>
<thead>
<tr>
<th>Signal</th>
<th>MT/s</th>
<th>Generation</th>
<th>Characteristics</th>
<th>Specification</th>
<th>Introduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDRAM</td>
<td>33 – 133</td>
<td></td>
<td>“Low Speed”</td>
<td></td>
<td>1961</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SDRAM</td>
<td>• Fanout</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Capacitance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDR/2/3</td>
<td>200 – 1600</td>
<td>“High Speed Digital”</td>
<td>• Transmission lines</td>
<td></td>
<td>2002</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Ts / Th, Skew</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDR4</td>
<td>1600 – 4200</td>
<td>“Serial Speed”</td>
<td>• Rx Masks</td>
<td></td>
<td>2014</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Bit error rates</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDR5+</td>
<td>4200 – 8000+</td>
<td>“Hyper Speed”</td>
<td>• Eye collapses</td>
<td></td>
<td>2019</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Impulse response</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• BER Rj/Dj, Rn/Dn</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Characteristics
- **“Hyper Speed”**
  - Eye collapses
  - Impulse response
  - BER Rj/Dj, Rn/Dn

- **“Serial Speed”**
  - Eye Diagrams
  - Rx Masks
  - Bit error rates

- **“High Speed Digital”**
  - Transmission lines
  - Ts / Th, Skew

- **“Low Speed”**
  - Fanout
  - Capacitance

---

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The Original Game Plan

WIDER SEEMED EASIER THAN FASTER

Materials and Process Physics

Channel Thruput (GBytes/sec)

\[ \nabla \times E = -\frac{\partial B}{\partial t} \]

Signaling

Memory Wall

Current Technology

3D Cubes

Gbits/sec per Pin

# I/O Pins

Channel Thruput (GBytes/sec)

Materials and Process Physics

Current Technology

3D Cubes

Gbits/sec per Pin

# I/O Pins
A whole new game for memory
Game On #3

USE VIRTUAL PROBING TO VERIFY AN OPEN EYE

Instrument does de-embedding
Tx – New measurements
**Tx – New Specs**

- tCK_NUI jitter (Dj Rj)
- DQS_NUI jitter (Dj Rj)
- DQ_NUI jitter (Dj Rj)
- DQ_Stressed Eye
Total Jitter – \( T_j = D_j + Q_j \times R_j \)

- **Deterministic Jitter (DJ)**
- **Data Dependent Jitter (DDJ)**
- **Inter-symbol Interference (ISI)**
- **Duty Cycle Distortion (DCD)**
- **Sub Rate Jitter (SRJ)**
- **Uncorrelated PJ (BUJ)**

- **Data Independent**
- **Random Jitter (RJ)**
- **Unbounded Gaussian distribution (thermal, noise)**
- **Periodic Jitter (PJ)**

**Total Jitter (TJ)**

**Periodic Jitter (PJ)**

**Uncorrelated PJ (BUJ)**

**Bounded (non-Gaussian)**

**Inter-symbol Interference (ISI)**

**Duty Cycle Distortion (DCD)**

**Sub Rate Jitter (SRJ)**

**Threshold shift, clock distortion**

**Crosstalk, serializer, etc.,**
# Timing Margin Evaporation

<table>
<thead>
<tr>
<th>Data Rate (Mt/s)</th>
<th>Bit Time (ps UI)</th>
<th>UI (%)*</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>5000.00</td>
<td>1.75%</td>
</tr>
<tr>
<td>400</td>
<td>2500.00</td>
<td>3.50%</td>
</tr>
<tr>
<td>800</td>
<td>1250.00</td>
<td>7.01%</td>
</tr>
<tr>
<td>1600</td>
<td>625.00</td>
<td>14.01%</td>
</tr>
<tr>
<td>2400</td>
<td>416.67</td>
<td>21.02%</td>
</tr>
<tr>
<td>3200</td>
<td>312.50</td>
<td>28.02%</td>
</tr>
<tr>
<td>4200</td>
<td>238.10</td>
<td>36.77%</td>
</tr>
<tr>
<td>4800</td>
<td>208.33</td>
<td>42.04%</td>
</tr>
<tr>
<td>6400</td>
<td>156.25</td>
<td>56.05%</td>
</tr>
</tbody>
</table>

Random jitter is rapidly consuming the entire data valid window

* Assumes 5ps RMS jitter at a channel error rate of 1.3E-16 (1e-18 Bit Error Rate)
Tx app jitter measurement
New Probes for New Technology

KEY PIECE TO COMPLEMENT THE TX SOLUTION

• We want to solve these challenges:
  • Existing BGA interposer design cannot handle top speeds in DDR5
  • Homegrown interposer requires engineering resource which is expensive

• The DDR5 BGA Interposer plan:
  • Design and build an initial DDR5 x4/x8 High Performance SI Interposer and riser
  • Re-spin the DDR5 HP SI Interposer for improved bandwidth
  • Develop an integrated Riser + Interposer
    • Better performance than separate parts
    • Easier attachment to DUT
Calibration Connection Diagram - RDIMM

- Scope is a reference receiver

- InfiniiSim – remove cable between 1X and scope

- InfiniiSim – add from gold finger to ball

- Connect to 1X through

- 50 Ω term
Test and Characterization Diagram (DQS/DQ)
Test Card Types for DDR5 Measurements

- **RCD Test Card**
- **DB Test Card**
- **Combo Test Card**

**Standard RDIMM**

**Channel Modeling Board**
- 1 DPC DQ Corner 2
- 1 DPC CA/DQ Corner
- 2 DPC CA/DQ Corner 2

- **Channel Modeling Board**
  - Open field emulation
  - Transition Zone (CPU Breakout Model)

- **UDIMM and SODIMM adapters for CTC2 and system modeling TBD**
DQ Voltage Sensitivity

<table>
<thead>
<tr>
<th>Test</th>
<th>DQ</th>
<th>DQS</th>
<th>CLK</th>
<th>DFE</th>
<th>Fixture</th>
</tr>
</thead>
<tbody>
<tr>
<td>DQ voltage sensitivity</td>
<td>Sweep V (clean)</td>
<td>Clean</td>
<td>Clean</td>
<td>Off</td>
<td>CTC 1 slot</td>
</tr>
</tbody>
</table>
## DQS Jitter Sensitivity

<table>
<thead>
<tr>
<th>Test</th>
<th>DQ</th>
<th>DQS</th>
<th>CLK</th>
<th>DFE</th>
<th>Fixture</th>
</tr>
</thead>
<tbody>
<tr>
<td>DQS jitter sensitivity - MEAS1</td>
<td>Clean</td>
<td>Sweep phase (clean)</td>
<td>Clean</td>
<td>Off</td>
<td>CTC 1 slot</td>
</tr>
<tr>
<td>DQS jitter sensitivity - MEAS2 (DCD)</td>
<td>Clean</td>
<td>Sweep phase (specified DCD)</td>
<td>Clean</td>
<td>Off</td>
<td>CTC 1 slot</td>
</tr>
<tr>
<td>DQS jitter sensitivity - MEAS3 (Rj)</td>
<td>Clean</td>
<td>Sweep phase (specified Rj)</td>
<td>Clean</td>
<td>Off</td>
<td>CTC 1 slot</td>
</tr>
<tr>
<td>DQS jitter sensitivity - MEAS4 (DCD+Rj)</td>
<td>Clean</td>
<td>Sweep phase (specified DCD+Rj)</td>
<td>Clean</td>
<td>Off</td>
<td>CTC 1 slot</td>
</tr>
</tbody>
</table>

![Diagram of DQS Jitter Sensitivity](image)

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## Stressed Eye

<table>
<thead>
<tr>
<th>Test</th>
<th>DQ</th>
<th>DQS</th>
<th>CLK</th>
<th>DFE</th>
<th>Fixture</th>
</tr>
</thead>
<tbody>
<tr>
<td>DQ stressed eye</td>
<td>Stress</td>
<td>Clean</td>
<td>Clean</td>
<td>Optimal – found in calibration</td>
<td>CTC 1 slot with Channel impairment board</td>
</tr>
</tbody>
</table>

**Diagram:***

- Receiver
- Pad
- 1/2/4 Tap DFE
- FF
- XOA
- DQ
  - VDDQ
  - gain
  - internal Vref

**Test Eye Result:***

- Calibrate eye to after DFE
LPDDR5 Challenges
# LPDDR5 / LPDDR4 Comparison

<table>
<thead>
<tr>
<th></th>
<th>LPDDR4/LPDDR4x</th>
<th>LPDDR5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Data Rate</td>
<td>3200MT/s LPDDR4 4266 LPDDR4x</td>
<td>6400MT/s POR</td>
</tr>
<tr>
<td>Clocks</td>
<td>CK CA and CNTRL DQS DQ Read &amp; Write</td>
<td>CK (800MHz max) WCK for DQ (Write &amp; Read) RDQS for Read DQ in RDQS mode</td>
</tr>
<tr>
<td>Clocking for DQ</td>
<td>DQ clocked DDR 1:1 ratio DQS to CK</td>
<td>WCK:CK ratio dynamically changes between 2:1 and <strong>4:1 clock ratio</strong> modes</td>
</tr>
<tr>
<td>Clock Termination</td>
<td>CK and DQS are Differential</td>
<td>CK, WCK, and RDQS can <strong>dynamically change between single ended and differential</strong></td>
</tr>
<tr>
<td>Minimum Signal swing</td>
<td>300mV</td>
<td>250mV</td>
</tr>
<tr>
<td>VDDQ</td>
<td>1.1V LPDDR4 0.6V LPDDR4x</td>
<td>Variable 0.5V to 1.1V</td>
</tr>
<tr>
<td><strong>ODT and CKE</strong></td>
<td>LPDDR4/LPDDR4x</td>
<td>LPDDR5</td>
</tr>
<tr>
<td>----------------</td>
<td>----------------</td>
<td>--------</td>
</tr>
<tr>
<td>Discrete Signals</td>
<td>No CKE /ODT signals – Frequency set points handled with MRS commands</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>CA</strong></th>
<th>LPDDR4/LPDDR4x</th>
<th>LPDDR5</th>
</tr>
</thead>
</table>
| CA 0-5 | CA 0-6  
SDR 2133MT/s for 4266MT/s data rate | DDR 1600MT/s max (up to 6400MT/s data rate) |

<table>
<thead>
<tr>
<th><strong>Command Protocol</strong></th>
<th>LPDDR4/LPDDR4x</th>
<th>LPDDR5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-cycle Commands</td>
<td>Multi-cycle commands with increased complexity to protocol</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Link ECC</strong></th>
<th>LPDDR4/LPDDR4x</th>
<th>LPDDR5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vendor specific</td>
<td>Optional</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Deep Sleep</strong></th>
<th>LPDDR4/LPDDR4x</th>
<th>LPDDR5</th>
</tr>
</thead>
<tbody>
<tr>
<td>No</td>
<td>Optional</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>DFE</strong></th>
<th>LPDDR4/LPDDR4x</th>
<th>LPDDR5</th>
</tr>
</thead>
<tbody>
<tr>
<td>No</td>
<td>Optional</td>
<td></td>
</tr>
</tbody>
</table>
Power Saving Features in LPDDR5

Variable VDDQ (up to 1.1V)

Deep Sleep

Clocks (CK, WCK, and RDQS) switch between SE and differential termination for low/high speeds.

- Clocks turn off/on dynamically
  - No CKE to indicate CK is turning off/on
  - Dynamic speed / threshold changes
LPDDR5 Signal Integrity Challenges

Historic Areas of Issues and New Concerns

- Areas of TX failures with previous LPDDR technologies often involve dynamic changes:
  - ODT
  - Speed
  - Bursty clocks
  - Clocks turning off/on
  - Thresholds

- New concerns for LPDDR5:
  - Dynamically changing CK terminations, single ended for slow speeds and differential for high speeds.
  - Shrinking noise margin with 250mV voltage swing at high speeds
LPDDR5 Tx Design Test and Validation

CHALLENGES AND SOLUTIONS

CHALLENGES

- Signal integrity
- Ensure interoperability
- Time-to-market Pressure

SOLUTIONS

- Higher Bandwidth / Low Noise Scopes/Probes
- LPDDR5 test parameters
- Automated Characterization and Compliance test
- Debug
- Data Analytics
Ensuring Signal Integrity and Interoperability

TX CHARACTERIZATION AND COMPLIANCE TEST

- LPDDR5 JESD209-5 spec.
  - Speed bins 3200 to 6400 MT/s.
- Electrical, timing, jitter and eye diagram tests.
- SE and differential clocks (CK, WCK, RDQS)*
- R/W separation

Benefits:
- Ensure interoperability between system and devices.
- Repeatability for accurate statistical analysis.
- Automation for speedy test time.
- Images in test reports
- Margin information

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### Test Report

#### Overall Result: PASS

<table>
<thead>
<tr>
<th>Test Configuration Details</th>
<th>Application</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Mode</td>
<td>DUT Test</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data Rate (MT/s)</td>
<td>500</td>
<td></td>
<td></td>
</tr>
<tr>
<td>WORatio</td>
<td>2:1</td>
<td></td>
<td></td>
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</table>

<table>
<thead>
<tr>
<th>Test Session Details</th>
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</thead>
<tbody>
<tr>
<td>Instrument Serial Number</td>
<td>1102993451</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Instrument Model</td>
<td>4344081</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Instrument Version</td>
<td>3.1.29.01</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Test Name</th>
<th>Actual Value</th>
<th>Margin</th>
<th>Pass Limits</th>
</tr>
</thead>
</table>
| Vdd| 1.745 V | 3.656 % | VALUE => Vdd
| CK/CK2 High| 0.94 mV | 3.109 % | VALUE => CK/CK2 High
| CK/CK2 Low| 0.92 mV | 3.737 % | VALUE => CK/CK2 Low
| CK| 728 mV | 4.021 % | VALUE => CK
| CK2| 785 mV | 4.414 % | VALUE => CK2
| SR| 6.14 Vm | 20.5 % | VALUE => SR
| CK| 2.211 Vm | 1.8 % | VALUE => CK
| CK| 3.639 ns | 0.8 % | VALUE => CK
| CK| 3.017 ns | Information Only |  |
| CK| 577.66290123 mVCK (avg) | 37.7 % | VALUE => CK
| CK| 496.69209000 mVCK (avg) | 45.9 % | VALUE => CK
| CK| 398.655215496 mVCK (avg) | 48.3 % | VALUE => CK

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Read Write Separation

**LPDDR4 METHODS WILL NOT WORK FOR LPDDR5**

LPDDR4 R/W Separation Techniques
- DQS/DQ phase difference.
- Pre-amble pattern difference
- DQ validation: Rx mask test

LPDDR5 R/W Separation Techniques
- TBD New Methods in development
- RDQS when available
- No DQS/DQ phase difference
- No Pre-amble pattern difference
- No amplitude difference between R/W
CHALLENGES AND SOLUTIONS*

CHALLENGES

Ensure interoperability

Identify root cause of system failure

Time-to-market Pressure

SOLUTIONS

Protocol Compliance and validation

Debug with complete view of the DDR traffic using powerful analysis tools

Viewscape to visualize noise on power or signal integrity issues correlated to memory analysis

* Data rate coverage will vary by system under test, CA/DQ, and logic analysis solution.
Ensure Interoperability

PROTOCOL COMPLIANCE AND DATA VALIDATION

Test
- Test and monitor your system under variable conditions.

Functional Compliance Validation
- Validate system is within JEDEC specifications.
  - Quick pass/fail results
  - Includes margin information on how far the system is deviating from the ‘pass limits’
  - Includes number of times violation occurred and how many times violation was tested
  - If not…..risk of system failures

Violation detection across speed changes and CK termination changes
Identify Root Cause of System Failure

**DEBUG CAPABILITIES**

- See the flow of the traffic between the memory controller and memory device to get to the root cause of system issues.

- Correlate memory traffic to scope capture of:
  - Signal integrity of specific signals
  - Power integrity
DDR5 and LPDDR5 Probing Challenges and Solutions
Dynamic ODT enables the DRAM to switch between high or low termination impedance. When the termination impedance goes high, probe impedance needs to be high enough to reduce probe loading.
MX0023A InfiniiMax 25 GHz RC Probe Overview

- 25 GHz (with MX0100A micro head)
- AutoProbe II interface – direct plug-in to UXR Jr, V, Q, 90kX
- RC input impedance profile with low midband loading
  - 25 k ohm input R @DC each signal to ground
  - 0.17 pF input C when used with MX0100A
- Compatible with most of InfiniiMax I/II probe head accessories

“RC” (red trace): traditional resistance – then capacitance impedance
“RCRC” (blue trace): High DC impedance, moderate mid-band
RC vs RCRC Probe For Probing LPDDR4 Signal

RC probe is a better choice when probing buses that transition to a “high Z” state or when dealing with signal with high impedance.
New PoP/BGA Interposers for DDR5 and LPDDR5

previous generation BGA/PoP interposer design/materials don’t cover DDR5/LPDDR5 data rates.

- Thinner (previously 70 mils, new 20 – 22 mils)
- New materials and processes.
  - Improved SI
  - Decreased crosstalk
- Integrated Riser + Interposer
  - Better performance than separate parts
  - Easier attachment to DUT
  - Available on custom probes
Riser, Interposer, and DRAM stack up (side view):

- **THINNER IS BETTER**

- **DRAM**
- **BGA Interposer**
- **Riser (or optional socket)**
- **PC Board**

New DDR5 BGA interposer f/u/w logic analyzer installed directly onto PC Board.
Designing for DDR5 and LPDDR5

CHALLENGES AND SOLUTIONS
Jitter

BER CONTOUR AT 1E-16 TELLS US THE REAL MARGIN

No Jitter – Just ISI from Channel

Random Jitter = 0.02 UI Applied at Tx (2%)

Jitter injected at Tx, and eye measured at the DRAM Solder-Ball (Rx Input)

Simulated with Memory Designer

47% Reduction in Timing Margin
(27ps less margin to mask)
Crosstalk

THE IMPORTANCE OF THE SIGNAL RETURN PATH

No Crosstalk, No Jitter – Just ISI from Channel

Signal Return Path – through shared Ground Pin

PCB Trace Routing of Victim + Worst Aggressors

Electromagnetic (EM) simulation with SIPro

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Rx Equalization

FIRST TIME TO HAVE DFE ON DRAM!

ISI affecting future bits

Variable Gain

DFE Tap 1

DFE Tap 2

DFE Tap 3

DFE Tap 4

VrefDQ

Variable Gain

DFE Summer

Variable Gain

Clk Tree

Clk Tree

Gain + DFE

Mode Register Settings (per DQ)

All values subject to change

<table>
<thead>
<tr>
<th>Setting</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Variable Gain</td>
<td>-6dB to 6dB</td>
</tr>
<tr>
<td>VrefDQ</td>
<td>-3 to +3 Offset steps</td>
</tr>
<tr>
<td>DFE Tap 1</td>
<td>-200mV to 50mV</td>
</tr>
<tr>
<td>DFE Tap 2</td>
<td>-75mV to 75mV</td>
</tr>
<tr>
<td>DFE Tap 3</td>
<td>-60mV to 60mV</td>
</tr>
<tr>
<td>DFE Tap 4</td>
<td>-45mV to 45mV</td>
</tr>
</tbody>
</table>
What Do We Need for DDR5 AMI To Work?

Supporting Parallel, Single-Ended Signals with External Clocks

Input to DRAM

After Gain & 4 Tap DFE

1.1V

0.55V

Single-Ended Signal can have a DC Offset

Asymmetric Eye: Rise Time ≠ Fall Time

Asymmetric Eye: Crossing Points are shifted in the Equalized Eye

DFE Clocked by DQS:

- Correlated Jitter on DQ & DQS cancels out
- Uncorrelated Jitter on DQS is transferred to DQ
An Enhanced AMI Solution for DDR

1. Multiple Tx and Rx in one Simulation

2. Calculate Impulse Responses for both a Rising Edge and a Falling Edge

3. Simulator applies the correct impulse responses to the part of the waveform that is rising, or falling

4. Simulator passes DC Offset value to the AMI model

5. Simulator can pass both DQ & DQS waveform to AMI model

TX AMI FFE → TX Analog + Pkg → Channel → RX Analog + Pkg → RX AMI DFE+ CTLE/VGA → Post-EQ Waveform

Back-Channel Interface For Training

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Reduce Simulation Complexity

• From hours of setup time to minutes
• One schematic for both DDR Bus simulation & Transient simulation
• Apply IBIS models for groups of signals as one
• Simple wiring- to automatically match and connect components
• Same testbench for both pre-layout and post-layout flow
• Easy EM setup of many nets at once
• EM must capture critical effects like Crosstalk
• Apply measurements to groups of signals
## Memory Bus Simulation for Today’s Challenges

### Challenge | Solution
---|---
Predict Eye closure due to Jitter | **Memory Designer** – DDR Bus Simulation based on channel simulation technology
Predict Eye closure due to Crosstalk | Accurate EM simulations that account for return path, such as **SIPr**
Equalization Modeling | **Memory Designer** – Enhanced DDR Bus simulation with **Bit-by-Bit IBIS-AMI** simulation
Asymmetric Eye Shape | Enhanced DDR Bus AMI simulation
DC Offset | Enhanced DDR Bus AMI simulation
DQ to DQS clocking | Enhanced DDR Bus AMI simulation
Multiple Tx and Rx at Once | **Memory Designer**
Simplify Complex Topology Setup & Measurement | **Memory Designer**
Write-leveling | **Memory Designer**
Ensuring First Pass Success

**KEYSIGHT IS THE ONLY PARTNER WITH SOLUTIONS IN ALL DDR5 TOUCH POINTS**

- Logic / Protocol
- Power Integrity
- Probing
- Rx Test
- DDR5 Methodology
- Test Fixtures
- Modeling and Simulation
- Tx Test
Q&A Session
Solution Configurations
LPDDR5 application test setup selections:

- Speed grade of device
- Live Signal or Off-line
- Signal sources
• Select Tab lists tests available in the setup.

• Easily setup individual test or groups of tests.
Comprehensive Compliance App Format and Features

**Test Report includes:**
- Pass/Fail indicator, # of Trials
- Test Name, Actual value
- Margin
- Pass limits
- Image (where appropriate)

### Summary of Results

<table>
<thead>
<tr>
<th>Test Name</th>
<th>Actual Value</th>
<th>Margin</th>
<th>Pass Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vddiff_CK</td>
<td>1.745 V</td>
<td>398.6%</td>
<td>VALUE &gt;= Vddiff_CK Limit_Min V</td>
</tr>
<tr>
<td>Vddiff_CK/HighPulse</td>
<td>894 mV</td>
<td>410.9%</td>
<td>VALUE &gt;= Vddiff_CK Limit_Min V</td>
</tr>
<tr>
<td>Vddiff_CK/LowPulse</td>
<td>829 mV</td>
<td>373.7%</td>
<td>VALUE &gt;= Vddiff_CK Limit_Min V</td>
</tr>
<tr>
<td>Vhalt_CK</td>
<td>728 mV</td>
<td>402.1%</td>
<td>VALUE &gt;= Vddiff_CK Limit_Min V</td>
</tr>
<tr>
<td>Vddiff_CK</td>
<td>-785 mV</td>
<td>441.4%</td>
<td>VALUE &lt;= Vddiff_CK Limit_Max V</td>
</tr>
<tr>
<td>SR_Margin_CK</td>
<td>4.814 Vms</td>
<td>23.9%</td>
<td>VALUE &lt;= SR_Margin Limit Max V</td>
</tr>
<tr>
<td>SR_Margin_CK</td>
<td>2.211 Vms</td>
<td>1.8%</td>
<td>VALUE &lt;= SR_Margin Limit Max V</td>
</tr>
<tr>
<td>ICK(avg) Average Clock period</td>
<td>3.636 ns</td>
<td>0.6%</td>
<td>VALUE &lt;= ICK(avg) Limit Max s</td>
</tr>
<tr>
<td>ICK(avg) Absolute Clock period</td>
<td>3.017 ns</td>
<td></td>
<td>Information Only</td>
</tr>
<tr>
<td>ICK(avg) Absolute Clock width</td>
<td>5.171 ms</td>
<td>37.7%</td>
<td>VALUE &lt;= ICK(avg) Limit Max (Avg)</td>
</tr>
<tr>
<td>ICK(avg) Average Clock width</td>
<td>4.636 ms</td>
<td>45.9%</td>
<td>VALUE &lt;= ICK(avg) Limit Max (Avg)</td>
</tr>
<tr>
<td>ICK(avg) Maximum Clock width</td>
<td>3.038 mV</td>
<td>-65.3%</td>
<td>VALUE &lt;= ICK(avg) Limit Max (Avg)</td>
</tr>
</tbody>
</table>

**Overall Result:** FAIL

**Test Configuration Details**
- **Application:** Memory DDR5 FDDR Test
- **Version:** 0.99-10051.0
- **Device Description:** DDR5 (D-16) 2G

**Test Session Details**
- **Instrument SW Version:** 64.0.00025
- **Instrument Model Number:** S9029A/DA
- **Instrument Serial Number:** No Serial
- **Debug Mode Used:** No
- **Compliance Limits:** LPR325-P30(2023) Test Line (Off-Chip)
- **Last Test Date:** 2019-11-17 16:17:02 UTC +00:00
Typical TX LPDDR5 SW Configuration

**Software**

<table>
<thead>
<tr>
<th>Model number</th>
<th>Description</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9050LDDC</td>
<td>LPDDR5 Compliance Test Software</td>
<td>Required</td>
</tr>
<tr>
<td>D9020JITA</td>
<td>Jitter, Vertical and Phase Noise Analysis Software</td>
<td>Required</td>
</tr>
<tr>
<td>D9020ASIA</td>
<td>Advanced Signal Integrity Software (EQ, InfiniiSim Advanced)</td>
<td>Optional</td>
</tr>
<tr>
<td>KS6810A</td>
<td>Data Analytics software (1 license)</td>
<td>Optional</td>
</tr>
<tr>
<td>D9010LSPO</td>
<td>Infiniium Offline Analysis Software</td>
<td>Optional</td>
</tr>
</tbody>
</table>
Minimum TX HW Configuration

**UXR PROVIDES OPTIONS TO INCREASE BANDWIDTH**

### Example of Hardware Configuration

<table>
<thead>
<tr>
<th>Model number</th>
<th>Description</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>UXR0164A</td>
<td>16 GHz Infiniium oscilloscope</td>
<td>1</td>
</tr>
<tr>
<td>1169B</td>
<td>12GHz InfiniiMax II probe amplifiers</td>
<td>3</td>
</tr>
<tr>
<td>N5442A</td>
<td>Precision BNC adapter</td>
<td>3</td>
</tr>
<tr>
<td>MX0100A</td>
<td>Micro probe head</td>
<td>1 (includes 5 probe heads, 1 bullet adapter)</td>
</tr>
<tr>
<td>MX0103A</td>
<td>Bullet adapter</td>
<td>2</td>
</tr>
</tbody>
</table>
# Typical TX Solution - 25GHz HW Configuration

**COVERS LPDDR5 UP TO 8400MT/S**

<table>
<thead>
<tr>
<th>Model number</th>
<th>Description</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>UXR0254A</td>
<td>25 GHz Infiniium oscilloscope</td>
<td>1</td>
</tr>
<tr>
<td>MX0023A</td>
<td>25GHz RC probe amplifier</td>
<td>3</td>
</tr>
<tr>
<td>MX0100A</td>
<td>Micro probe head</td>
<td>1 (includes 5 probe heads, 1 bullet adapter)</td>
</tr>
<tr>
<td>MX0103A</td>
<td>Bullet adapter</td>
<td>2</td>
</tr>
</tbody>
</table>

*NEW!* 25GHz RC probe SHP Feb 2020
Challenging trends in target devices (connection pads, SMD, vias, interposers etc.):

- Smaller
- Denser
- Narrowing spacing

Keysight Education Forum – DesignCon 2020
### MX0023A Internal Comparison

**Extending RC Probing Bandwidth to Unprecedented 25 GHz TX Solution**

<table>
<thead>
<tr>
<th></th>
<th>Keysight InfiniiMax II 1168B/69B</th>
<th>Keysight InfiniiMax III+</th>
<th>Keysight MX0023A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth</td>
<td>10, 12 GHz</td>
<td>4, 8, 13, 16, 20 GHz</td>
<td>25 GHz</td>
</tr>
<tr>
<td>Probe loading</td>
<td>50 kohm//0.17 pF RC</td>
<td>100 kohm @DC, 1kohm @&gt;1 kHz // 0.108 pF RCRC</td>
<td>50 kohm//0.17 pF RC</td>
</tr>
<tr>
<td>Attenuation ratio</td>
<td>3.45:1</td>
<td>5:1 or 10:1</td>
<td>1:1 or 4:1</td>
</tr>
<tr>
<td>Input range</td>
<td>3.3Vpp diff, +/-16V offset</td>
<td>2.5Vpp @5:1, 5Vpp @10:1, +/-16V offset</td>
<td>0.6Vpp @1:1, 2.5Vpp @4:1, +/-16V offset</td>
</tr>
<tr>
<td>Noise</td>
<td>23 nV/rt(Hz)</td>
<td>33.5 nV/rt(Hz) @5:1</td>
<td>25 nV/rt(Hz) @1:1 (preliminary)</td>
</tr>
<tr>
<td>Probe accessories</td>
<td>Solder-in, browser, ZIF, SMA, Micro head, Extreme temp, in-line attenuator, Socketed, QuickTip</td>
<td>Solder-in, browser, ZIF, SMA, Extreme temp, in-line attenuator, QuickTip</td>
<td>Solder-in, browser, ZIF, SMA, Micro head, Extreme temp, TBD for other new RC probe heads</td>
</tr>
<tr>
<td>InfiniiMode</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>S parameter correction</td>
<td>Probe and head Nominal</td>
<td>Probe specific, head nominal</td>
<td>Probe specific, head nominal</td>
</tr>
</tbody>
</table>

New features include:

- **Keysight InfiniiMax II 1168B/69B**
  - Bandwidth: 10, 12 GHz
  - Probe loading: 50 kohm//0.17 pF RC
  - Attenuation ratio: 3.45:1
  - Input range: 3.3Vpp diff, +/-16V offset
  - Noise: 23 nV/rt(Hz)
  - Probe accessories: Solder-in, browser, ZIF, SMA, Micro head, Extreme temp, in-line attenuator, Socketed, QuickTip

- **Keysight InfiniiMax III+**
  - Bandwidth: 4, 8, 13, 16, 20 GHz
  - Probe loading: 100 kohm @DC, 1kohm @>1 kHz // 0.108 pF RCRC
  - Attenuation ratio: 5:1 or 10:1
  - Input range: 2.5Vpp @5:1, 5Vpp @10:1, +/-16V offset
  - Noise: 33.5 nV/rt(Hz) @5:1
  - Probe accessories: Solder-in, browser, ZIF, SMA, Extreme temp, in-line attenuator, QuickTip

- **Keysight MX0023A**
  - Bandwidth: 25 GHz
  - Probe loading: 50 kohm//0.17 pF RC
  - Attenuation ratio: 1:1 or 4:1
  - Input range: 0.6Vpp @1:1, 2.5Vpp @4:1, +/-16V offset
  - Noise: 25 nV/rt(Hz) @1:1 (preliminary), 39 nV/rt(Hz) @4:1 (preliminary)
  - Probe accessories: Solder-in, browser, ZIF, SMA, Micro head, Extreme temp, TBD for other new RC probe heads

Additional features:

- **InfiniiMode**
  - No
  - Yes

- **S parameter correction**
  - Probe and head Nominal
  - Probe specific, head nominal
  - Probe specific, head nominal
# Types of Probe Heads for MX0023A Probe Amp

## Industry's The "Widest" Variety of Probe Heads

<table>
<thead>
<tr>
<th>Probe heads</th>
<th>“Micro” Solder-in – full BW</th>
<th>Solder-in</th>
<th>Socketed</th>
<th>ZIF (zero insertion force) tip</th>
<th>Browser</th>
<th>SMA</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bandwidth and diff loading</strong></td>
<td>25 GHz, 0.17 pF (lowest)</td>
<td>23 GHz, 0.17 pF (tie)</td>
<td>12 GHz</td>
<td>18 GHz</td>
<td>Up to 21 GHz</td>
<td>20 GHz</td>
</tr>
<tr>
<td><strong>Applications</strong></td>
<td>For accessing small geometry, high-density fine-pitch devices</td>
<td>The most reliable semi-permanent signal access for high fidelity measurement</td>
<td>Measuring signal via a plug-on socket connection</td>
<td>For probing multiple signals in tight space such as DDR memory</td>
<td>General purpose trouble-shooting and signal browsing</td>
<td>For diff cable measurement with voltage termination</td>
</tr>
<tr>
<td><strong>Availability</strong></td>
<td>MX0100A released in Aug 2018</td>
<td>N5381B (12 GHz) continues to be available. MX0106A covers up to 23 GHz</td>
<td>E2678B available</td>
<td>N5425B + N5426A, N5451A or N2884A</td>
<td>E2675B (6 GHz), N2839A (12 GHz) available now</td>
<td>N5380B (12 GHz) to be discontinued in Dec 2020 MX0105A (20 GHz)</td>
</tr>
</tbody>
</table>
MX0100A micro probe head

UNCOMPROMISED ACCESS TO YOUR FINE PITCH DEVICES

- < Half the size of existing solder-in probe heads
- Small, flat and flexible (using flex printed circuit)
- Full probe amp bandwidth (12 GHz with 1169B, 25 GHz with MX0023A)
- Excellent probe loading (0.17 pF)
- Compatible with “RC” probe amps (InfiniiMax I/II and RC probes)
- Reusable
- Wider operating temp range: -55 to +150 degC (per JEDEC JESD22-A104 revision E spec)
- Half the price of existing solder-in heads
Protocol Probing for DDR5/LPDDR5 Form Factors

ACCURATE, RELIABLE PROBES TO CONNECT TO ANY SYSTEM

RDIMM/LRDIMM, UDIMM and SODIMM Interposers

BGA Interposers for Chip down applications

Mid-Bus Probing (footprint must be designed into system under test)

Custom probes to meet unique requirements are also available.
# B4661A Memory Analysis SW licensed options

## Charted by Technology and Views/Tools

<table>
<thead>
<tr>
<th>Licensed Viewers, Tabs, and Tools</th>
<th>Features Included in Licensed Options by Memory Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DDR/2</td>
</tr>
<tr>
<td>Listing Decoder</td>
<td></td>
</tr>
<tr>
<td></td>
<td>B4661A-1FP/1TP/1NP DDR/2/3/4 Listing Decode</td>
</tr>
<tr>
<td>Timeline View (ONFi)</td>
<td></td>
</tr>
<tr>
<td>Payload tab (ONFi)</td>
<td></td>
</tr>
<tr>
<td>Traffic Overview</td>
<td></td>
</tr>
<tr>
<td>Transaction Decode</td>
<td></td>
</tr>
<tr>
<td>Details tab</td>
<td></td>
</tr>
<tr>
<td>Performance Overview</td>
<td></td>
</tr>
<tr>
<td>Memory Access Overview</td>
<td></td>
</tr>
<tr>
<td>Mode Register Overview</td>
<td></td>
</tr>
<tr>
<td>Speed Change Overview</td>
<td></td>
</tr>
<tr>
<td>Refresh Rate Overview</td>
<td></td>
</tr>
<tr>
<td>Post Process compliance Violation Tool</td>
<td></td>
</tr>
<tr>
<td>Real Time Compliance Violation Tool</td>
<td></td>
</tr>
<tr>
<td></td>
<td>B4661A-4FP/4TP/4NP DDR3/4 LPDDR3/3/ Analysis coverage</td>
</tr>
<tr>
<td></td>
<td>B4661A-3FP/3TP/3NP DDR/2/3/4 and LPDDR2/3/4 Compliance Validation</td>
</tr>
</tbody>
</table>
One U4164A module with option -02G covers a single LPDDR5 x16 DRAM for CA and DQ/DQS capture.

- DQ tuned for single frequency
- Simultaneous Read/Write 2:1 clock ratio only
  - Reason: simultaneous R/W capture in 4:1 mode would require double probing for 8 samples per DQ. Doubtful LPDDR5 will tolerate double probing due to space and loading constraints.
- 4:1 clock ratio, configurations and tuning DQ for either Read or Write
- CA capture is expected to track speed changes for all LPDDR5 data rates.
Configuration for LPDDR4 200-ball package, CHA CA and limited DQ capture.

- Qty(1) U4164A module
- M9502A AXIe 5-Slot Chassis
- M9537A AXIe Embedded Controller
- Qty (1) W6601A-001 LPDDR4 200-ball 2 wing BGA interposer
- Qty(1) U4208A ZIF cable Left
- Qty(1) U4209A ZIF cable Right
- B4661A Memory Analysis SW
- B4661A-2TP/2FP/2NP LPDDR2/3/4 Listing Decoder
- B4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
- B4661A-4TP/4FP/4NP DDR3/4, LPDDR2/3/4, and ONFi Analysis

When memory systems don’t behave as expected, use the U4164A system for trace capture and analysis insights to resolve issues quickly!
**DDR5 configuration for RDIMM or LRDIMM Protocol**

- Qty (4) U4164A logic analyzer modules
  - Qty (2) sets of 2 modules
- Qty (4) option -02G speed grade option
- Qty (4) optional customer choice of memory depth options
- Qty (1) M9505A chassis
- Qty (1) M9537A embedded controller
- Qty (1) FS2600 DDR5 RDIMM/LRDIMM Interposer
- Qty (1) B4661A Memory Analysis SW
  - Qty (1) B4661A-5FP/5TP/5NP

**Modified Photo of DDR4 system**

DDR5 will require 4 U4164A modules in two 2 module sets to view two DDR5 RDIMM channels simultaneously.

FS2600 DDR5 RDIMM/LRDIMM interposer will be similar to the DDR4 interposer.

RDIMM/LRDIMM, UDIMM and SODIMM are unique, other solution components remain the same for all DDR5 DIMM protocol solutions.

Requires 100mV x 100ps eye on signals at interposer for accurate capture
**DDR5 x4/X8 78-ball DRAM configuration for Protocol**

- Qty (1) U4164A logic analyzer module
- Qty (1) option -02G speed grade option
- Qty (1) optional customer choice of memory depth options
- Qty (1) M9502A chassis
- Qty (1) M9537A embedded controller
- Qty (1) W5643A DDR5 78 ball BGA interposer with riser
- Qty(1) U4208A ZIF cable
- Qty (1) U209A ZIF cable
- Qty (1) B4661A Memory Analysis SW
  - Qty (1) B4661A-5FP/5TP/5NP DDR5 Analysis and Compliance Validation
DDR4 configuration for RDIMM, LRDIMM or UDIMM

- U4164A logic analyzer modules
  - Qty (3) each with option -02G for all ADD/CMD/DQ

- M9505A chassis

- M9537A embedded controller

- PS-X10-650-3PH Interposer FS2520 DDR4 4Gb/s 288 pin DIMM

- B4661A Memory Analysis SW
  - B4661A -1TP/1FP/1NP DDR Decoder
  - B4661A - 2TP/3FP/3NP Compliance Analysis
  - B4661A - 4TP/4FP/4NP Performance Analysis

Proven to 4.2GT/s!
**LPDDR4 Configuration**  
200-ball package with W6602A BGA interposer

Configuration for LPDDR4 200-ball package, CHA and CHB CA and DQ capture.

- Qty(2) U4164A module
- M9505A AXIe 5-Slot Chassis
- M9537A AXIe Embedded Controller
- Qty (1) W6602A-001 LPDDR4 200-ball ridgid BGA interposer
- Qty(2) U4207A ZIF cable Left
- B4661A Memory Analysis SW
- B4661A-2TP/2FP/2NP LPDDR2/3/4 Listing Decoder
- B4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
- B4661A-4TP/4FP/4NP DDR3/4, LPDDR2/3/4, and ONFi Analysis

When memory systems don’t behave as expected, use the U4164A system for trace capture and analysis insights to resolve issues quickly!
W6600A Series LPDDR4 BGA Interposers

Solution requires a BGA interposer and two probe cables to connect between the logic analyzer front panel and the LPDDR4 DRAM

<table>
<thead>
<tr>
<th>LDDR4 package</th>
<th>LPDDR4 Signal Access</th>
<th>BGA Interposer</th>
<th>Probe cables (qty)</th>
<th>LA Compatibility</th>
<th>Order Summary Model-opt (qty)</th>
</tr>
</thead>
<tbody>
<tr>
<td>200-ball</td>
<td>CHA only: Command, Address, Control Partial DQ from each Byte lane</td>
<td>W6601A</td>
<td>U4208A (1)</td>
<td>U4164A only -01G &lt; 2500Mb/s -02G &gt; 2500 Mb/s</td>
<td>U4164A (1)* U4164A-02G (1) W6601A U4208A (1) U4209A (1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>U4209A (1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>200-ball</td>
<td>CHA and CHB Command, Address, Control and Data **</td>
<td>W6602A</td>
<td>U4207A (2)</td>
<td>U4164A only -01G &lt; 2500Mb/s -02G &gt; 2500 Mb/s</td>
<td>U4164A (2)* U4164A-02G (2) W6602A U4207A (2)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*U4164A requires M9502A or M9505A AXIe chassis and host controller.
** W6602A brings most LPDDR4 200-ball signals out to the logic analyzer