D9040DPPC DisplayPort Compliance Test Application

KEYSIGHT

METHODS OF IMPLEMENTATION

Notices

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DisplayPort Automated Testing—At A Glance

The Keysight D9040DPPC DisplayPort Compliance Test Application can be operated in following two modes:

1 Online Mode (On Infiniium Oscilloscope) - This mode allows to analyze live waveform, capture and store live waveform, or analyze a saved waveform.

2 Offline Mode (On PC) - This mode only allows to analyze saved waveform or simulated waveform.

NOTE **The tests performed by the DisplayPort Compliance Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.**

You may refer to the following specification documents for compliance testing measurements. For more information, see the VESA web site at www.vesa.org.

Test Specification	Reference Documents
DisplayPort 1.2b	VESA DisplayPort Standard Version 1, Revision 2a, May 23, 2012 VESA DisplayPort PHY Compliance Test Specification Version 1.2b, November 26, 2012
DisplayPort 1.4a	VESA DisplayPort (DP) Standard 1.4a, April 19, 2018 VESA DisplayPort 1.4a PHY Compliance Test Specification (PHY CTS) Version 1.1, June 05, 2020
DisplayPort 1.4 (1.4)	VESA DisplayPort (DP) Standard Version 1.4, February 23, 2016
DisplayPort Alt Mode on USB Type-C (DPoC 1.4a)	VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.0a, August 05, 2015 VESA DisplayPort 1.4a PHY Compliance Test Specification (PHY CTS) Version 1.1, June 05, 2020
DisplayPort Alt Mode on USB Type-C (DPoC)	VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.0a, August 05, 2015
Mobility DisplayPort 1.0 (MyDP)	VESA Mobility DisplayPort (MyDP) Standard Version 1, May 21, 2012 VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, April 26, 2013
SlimPort (MyDP HBR25)	SlimPort Compliance Test Specification Version 1, February 28, 2014

Online Mode:

The Keysight D9040DPPC DisplayPort Compliance Test Application helps to verify compliance of the DisplayPort devices with DisplayPort specifications using Keysight Infiniium Digital Storage Oscilloscopes with bandwidths of 13 GHz or higher. The DisplayPort Compliance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.
- Allows to analyze saved waveforms or simulated waveforms in offline mode

Required Equipment and Software

In order to run the DisplayPort automated tests, you need the following equipment and software:

- Infiniium 90000A Series / 90000X Series / 90000Q Series / V-Series / Z-Series / UXR Series Oscilloscope
- The minimum version of Infiniium Oscilloscope Software (see the D9040DPPC DisplayPort Compliance Test Application Release Notes)
- D9040DPPC DisplayPort Compliance Test Application version 3.76 or above.
- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- D9040DPPC DisplayPort Compliance Test Application license.

NOTE

Keysight D9040DPPC DisplayPort Compliance Test Application supports **Keysight D9010AGGC Compliance Test Software Measurement Server** for using multiple machines/PCs over a network as acquisition engines and processing engines in order to significantly enhance the test execution speed. To know more, please see the D9010AGGC product page on keysight.com (http://www.keysight.com/find/d9010aggc).

In order to run the automated tests on DisplayPort DUTs, you need the following fixtures and accessories:

- DisplayPort Test Point Adapter:

For DUT Type	Required Fixtures/Accessories (Recommended)	Quantity	Recommended Oscilloscope
Source	For USB Type-C Connector ▪ N7015A Type-C High-Speed Test Fixture ▪ Wilder Technologies DPC-TPA-P* For DisplayPort Connector ▪ Wilder Technologies DP-TPA-P* ▪ W2641B DisplayPort Test Point Access Adapter For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-P* ▪ Luxshare ICT mDP Plug (mDP-TPA-P)** For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P*	1 (each)	Infiniium Series
Sink or Cable	For USB Type-C Connector ▪ Wilder technologies DPC-TPA-R* For DisplayPort Connector ▪ Wilder technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Receptacle (mDP-TPA-R)** For MyDP Connector ▪ Wilder Technologies (MYDP-TPA-R*)		

* All Wilder Technologies Test Point Adapters require the Wilder Technologies DP-TPA-A Aux Control Board.

** All Luxshare ICT Test Point Adapters require the Luxshare ICT DP-TPA-A AUX Control Board.

- InfiniiMax Series Probe Amplifiers with minimum 12GHz bandwidth:

Required Fixtures/Accessories (Recommended)	Quantity	Recommended Oscilloscope
▪ 1169A 12GHz InfiniiMax II Series Probe Amplifier ▪ N2832A 13GHz InfiniiMax III+ Series Probe Amplifier ▪ N2800A 16GHz InfiniiMax III Series Probe Amplifier	4	Infiniium Series

- InfiniiMax Series Probe Head with minimum 12GHz bandwidth:

Test Type	Required Fixtures/Accessories (Recommended)	Quantity	Recommended Oscilloscope
Physical Layer Tests	▪ N5380A InfiniiMax II 12GHz Differential SMA Adapter ▪ N5444A InfiniiMax III 28GHz SMA Probe Head ▪ MX0105A InfiniiMax Differential SMA Probe Head, 20 GHz	4	Infiniium Series
AUX Channel Tests	▪ E2677A InfiniiMax 12GHz Differential Solder-In Probe Head ▪ E2678A/B InfiniiMax 12GHz Single-Ended/Differential Probe Head & Accessories	1	

- Other Equipment (required for Internal/Self Calibration of the Infiniium Oscilloscope):

Required Fixtures/Accessories (Recommended)	Quantity	Recommended Oscilloscope/Description
BNC to SMA (female) Adapter	4	Infiniium 90000A Series
SMA (female) to SMA (female) Adapter	4	Infiniium 90000X Series / 90000Q Series / V-Series / Z Series / UXR Series
E2655A/B/C Probe De-Skew and Performance Verification Kit	1	Infiniium Series
Calibration Cable	1	Infiniium Series
80 Ω Damping Resistors (01130-81506)	1	To be used with Socketed Differential Probe Head

- Automation Controllers (Optional):

Testing Type	Supported Fixtures/Accessories (Optional)	Quantity	Recommended Oscilloscope
For Source DUT Testing	Unigraf DPR-100 Compact Sized DisplayPort Reference Sink	1 (each)	Infiniium Series
For Sink DUT Testing	Unigraf DPT-200 Compact Sized DisplayPort Reference Source		
For Alt Mode Control	Keysight N7018A Type-C Test Controller		

Offline Mode:

The Keysight D9040DPPC DisplayPort Compliance Test Application in offline mode provides a framework for using Keysight Infiniium Oscilloscopes software to perform offline compliance testing by using saved waveforms or simulated waveforms. The automated test application guides a user through the process of identifying the test environment, selecting and configuring tests, running tests, and evaluating the test results.

In order to run the DisplayPort automated tests, the following software are needed:

- The minimum version of Infiniium Oscilloscope Software (see the D9040DPPC DisplayPort Compliance Test Application Release Notes)
- D9040DPPC DisplayPort Compliance Test Application version 3.76 or above
- D9040DPPC DisplayPort Compliance Test Application license
- Saved waveforms or simulated waveforms in.wfm or.h5 format for analysis

NOTE

In offline mode of DisplayPort Compliance Test Application, only following two **Test Selection** types are available:

1. Physical Layer Tests

2. Test Tools

Therefore, only the test associated with the mentioned **Test Selection** types will be available for running/execution in offline mode.

In This Book

This manual describes the tests that are performed by the DisplayPort Compliance Test Application in more detail; it contains information from (and refers to) various DisplayPort specifications and it describes how the tests are performed.

- Chapter 1, “Installing the DisplayPort Compliance Test Application” shows how to install and license the automated test application (if it was purchased separately).
- Chapter 2, “Preparing to Take Measurements” shows how to start the DisplayPort Compliance Test Application and gives a brief overview of how it is used.
- Chapter 3, “DisplayPort 1.2b Source Tests” describes the normative and informative tests for compliance verification of DisplayPort 1.2 source devices.
- Chapter 4, “DisplayPort 1.2b Sink Tests” describes the normative and informative tests for compliance verification of DisplayPort 1.2 sink devices.
- Chapter 5, “DisplayPort 1.2b Cable Tests” describes the normative and informative tests for compliance verification of DisplayPort 1.2 cable devices.
- Chapter 6, “DisplayPort 1.2b AUX Channel Tests” describes the normative and informative AUX channel physical layer tests for compliance verification of DisplayPort 1.2 source and sink devices.
- Chapter 7, “DisplayPort 1.2b Inrush Tests” describes the normative and informative inrush tests for compliance verification of DisplayPort 1.2 source and sink devices as a power consumer.
- Chapter 8, “DisplayPort 1.2b Dual Mode Tests” describes the normative and informative Dual Mode physical layer tests for compliance verification of DisplayPort 1.2 source devices.
- Chapter 9, “DisplayPort 1.4a Source Tests” describes the normative and informative tests for compliance verification of DisplayPort 1.4a source devices.
- Chapter 10, “DisplayPort 1.4a Sink Tests” describes the normative and informative tests for compliance verification of DisplayPort 1.4a sink devices.
- Chapter 11, “DisplayPort 1.4a Cable Tests” describes the normative and informative tests for compliance verification of DisplayPort 1.4a cable devices.
- Chapter 12, “DisplayPort 1.4a AUX Channel Tests” describes the normative and informative AUX channel physical layer tests for compliance verification of DisplayPort 1.4a source and sink devices.
- Chapter 13, “DisplayPort 1.4a Inrush Tests” describes the normative and informative inrush tests for compliance verification of DisplayPort 1.4a source and sink devices as a power consumer.
- Chapter 14, “DisplayPort 1.4a Dual Mode Tests” describes the normative and informative Dual Mode physical layer tests for compliance verification of DisplayPort 1.4a source devices.
- Chapter 14, “DisplayPort 1.4 Source Tests” describes the normative and informative tests for compliance verification of DisplayPort 1.4 source devices.
- Chapter 15, “DisplayPort 1.4 Sink Tests” describes the normative and informative tests for compliance verification of DisplayPort 1.4 sink devices.
- Chapter 16, “DisplayPort 1.4 Cable Tests” describes the normative and informative tests for compliance verification of DisplayPort 1.4 cable devices.
- Chapter 17, “DisplayPort 1.4 AUX Channel Tests” describes the normative and informative AUX channel physical layer tests for compliance verification of DisplayPort 1.4 source and sink devices.
- Chapter 18, “DisplayPort 1.4 Inrush Tests” describes the normative and informative inrush tests for compliance verification of DisplayPort 1.4 source and sink devices as a power consumer.
- Chapter 20, “DisplayPort 1.4 Dual Mode Tests” describes the normative and informative Dual Mode physical layer tests for compliance verification of DisplayPort 1.4 source devices.
- Chapter 19, “DPoC 1.4a Source Tests” describes the normative and informative tests for compliance verification of Type-C enabled DisplayPort source devices.

- Chapter 20, “DPoC 1.4a Sink Tests” describes the normative and informative tests for compliance verification of Type-C enabled DisplayPort sink devices.
- Chapter 21, “DPoC 1.4a Cable Tests” describes the normative and informative tests for compliance verification of Type-C enabled DisplayPort cable devices.
- Chapter 22, “DPoC 1.4a AUX Channel Tests” describes the normative and informative AUX channel physical layer tests for compliance verification of Type-C enabled DisplayPort source and sink devices.
- Chapter 23, “DPoC 1.4a Inrush Tests” describes the normative and informative inrush tests for compliance verification of Type-C enabled DisplayPort source and sink devices as a power consumer.
- Chapter 24, “DPoC Source Tests” describes the normative and informative tests for compliance verification of Type-C enabled DisplayPort source devices.
- Chapter 25, “DPoC Sink Tests” describes the normative and informative tests for compliance verification of Type-C enabled DisplayPort sink devices.
- Chapter 26, “DPoC Cable Tests” describes the normative and informative tests for compliance verification of Type-C enabled DisplayPort cable devices.
- Chapter 27, “DPoC AUX Channel Tests” describes the normative and informative AUX channel physical layer tests for compliance verification of Type-C enabled DisplayPort source and sink devices.
- Chapter 28, “DPoC Inrush Tests” describes the normative and informative inrush tests for compliance verification of Type-C enabled DisplayPort source and sink devices as a power consumer.
- Chapter 29, “CTLE Optimization Tests” describes the normative and informative CTLE Optimization tests for compliance verification of DisplayPort devices.
- Chapter 30, “MyDP 1.0 Source Tests” describes the normative and informative tests for compliance verification of MyDP 1.0 source devices.
- Chapter 31, “MyDP 1.0 Sink Tests” describes the normative and informative tests for compliance verification of MyDP 1.0 sink devices.
- Chapter 32, “MyDP 1.0 Cable Tests” describes the normative and informative tests for compliance verification of MyDP 1.0 cable devices.
- Chapter 33, “MyDP 1.0 AUX Channel Tests” describes the normative and informative AUX channel physical layer tests for compliance verification of MyDP 1.0 source and sink devices.
- Chapter 34, “MyDP 1.0 Inrush Tests” describes the normative and informative inrush tests for compliance verification of MyDP 1.0 source and sink devices as a power consumer.
- Chapter 35, “SlimPort Source Tests” describes the normative and informative tests for compliance verification of SlimPort source devices.
- Chapter 36, “SlimPort Sink Tests” describes the normative and informative tests for compliance verification of SlimPort sink devices.
- Chapter 37, “SlimPort Cable Tests” describes the normative and informative tests for compliance verification of SlimPort cable devices.
- Chapter 38, “SlimPort AUX Channel Tests” describes the normative and informative AUX channel physical layer tests for compliance verification of SlimPort source and sink devices.
- Chapter 39, “SlimPort Inrush Tests” describes the normative and informative inrush tests for compliance verification of SlimPort source and sink devices as a power consumer.
- Appendix 40, “DisplayPort AUX Channel Cookbook for Tx Automated Test” provides a guide on how to implement the test automation features architected in the *DisplayPort Specification 1.1a* using a sink emulator such as the Keysight W2642 DPTC controller.

See Also

- The DisplayPort Compliance Test Application's Online Help, which describes:
  - Keysight D9040DPPC DisplayPort Automated Testing—At a Glance
  - Starting the Keysight D9040DPPC DisplayPort Test Application
  - Creating or Opening a Test Project
  - Setting Up the Test Environment
  - Selecting Tests
  - Configuring Tests
  - Verifying Physical Connections
  - Running Tests
  - Configuring Automation in the Test Application
  - Viewing Results
  - Viewing HTML Test Report
  - Exiting the Test Application
  - Additional Settings in the Test App

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1 Installing the DisplayPort Compliance Test Application

If you purchased the D9040DPPC DisplayPort Compliance Test Application, you need to install the software and license key.

Installing the Software

1. Make sure you have the minimum version of Infiniium oscilloscope software (see the D9040DPPC test application release notes) by choosing **Help > About Infiniium...** from the main menu.
2. To obtain the DisplayPort Compliance Test Application, go to Keysight website: http://www.keysight.com/find/scope-apps-sw.
3. Search the list on this web page for the link to the D9040DPPC DisplayPort Compliance Test Application. Click the appropriate link and follow the instructions to download and install the application.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

1 Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.

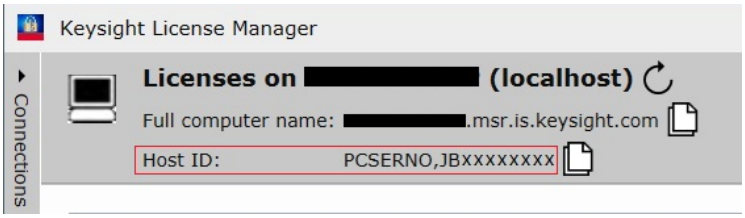


Figure 1 Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager.

3 From the configuration menu, use one of the options to install each license file.

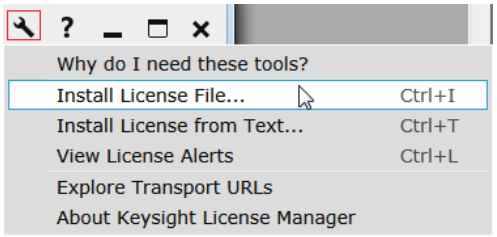


Figure 2 Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

1. Launch Keysight License Manager 6 on your machine, where you wish to run the Test Application and its features.
2. Copy the Host ID, which is the first set of alphanumeric value (as highlighted in Figure 3) that appears in the Environment tab of the application. Note that x indicates numeric values.

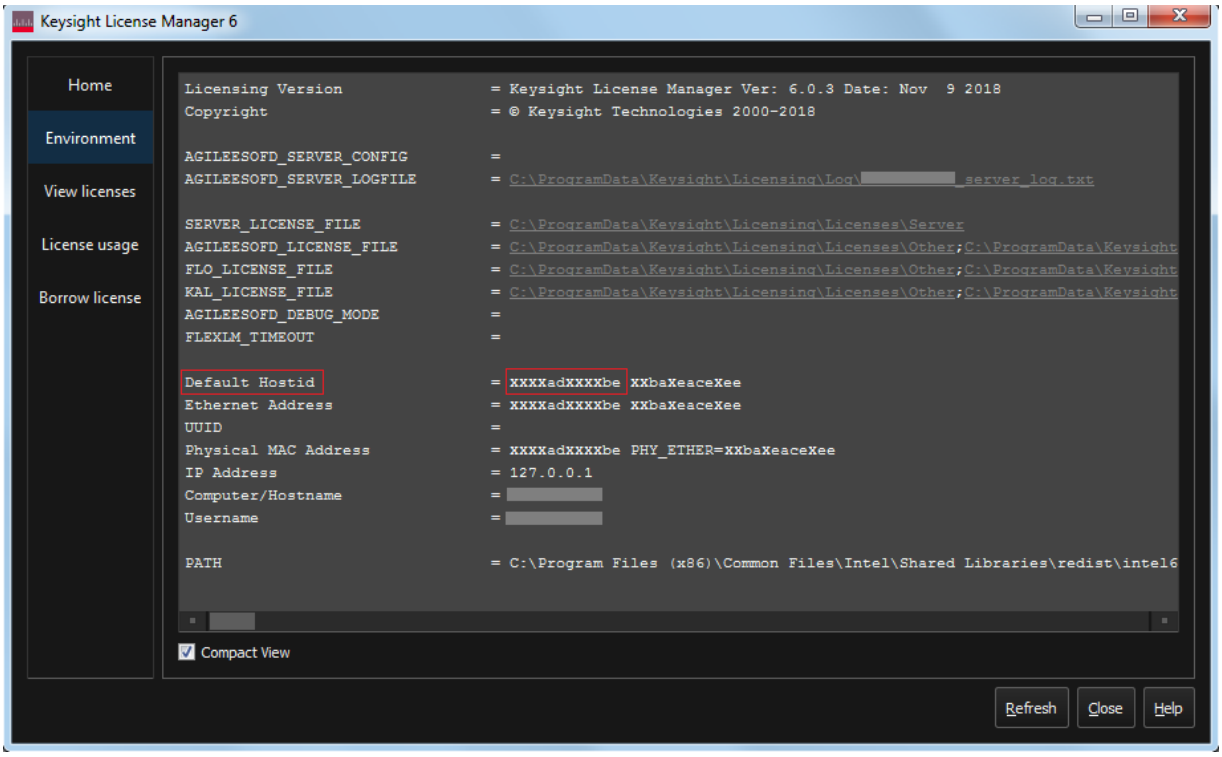


Figure 3 Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager 6.

3 From the Home tab, use one of the options to install each license file.

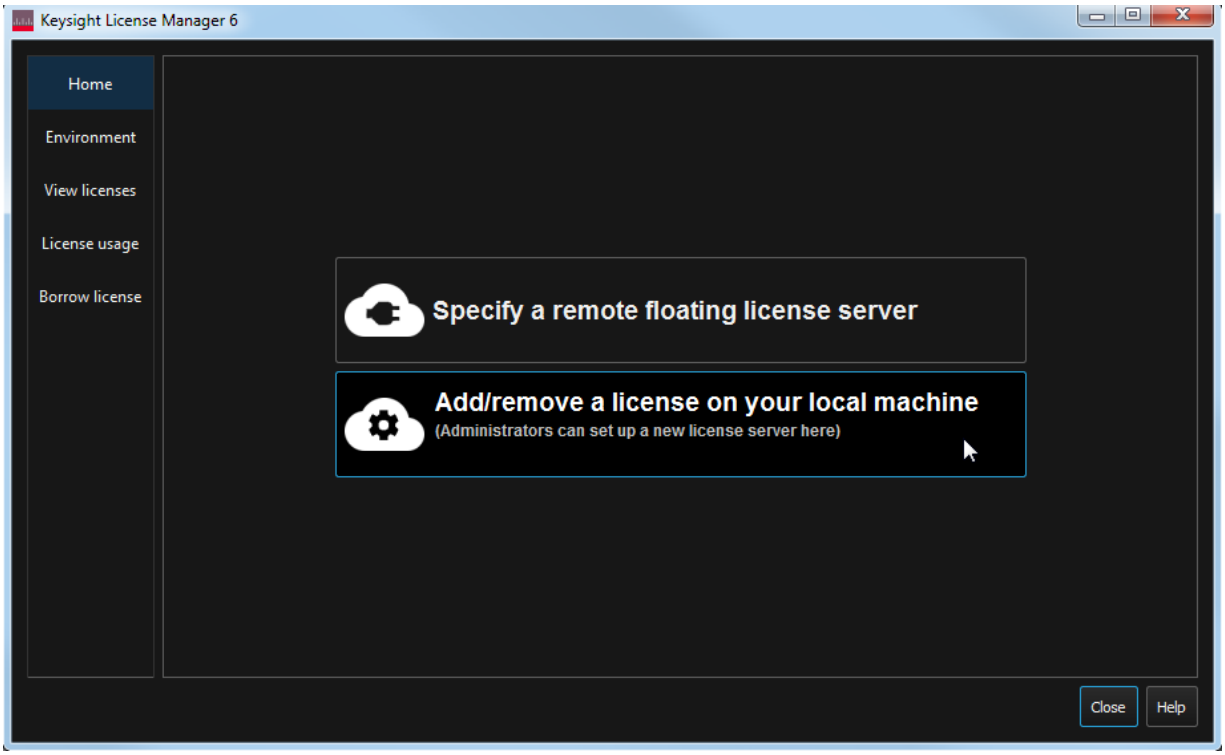


Figure 4 Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

2 Preparing to Take Measurements

Before running the DisplayPort automated tests, you must acquire the appropriate test fixtures, and you should calibrate the oscilloscope and probe. After the oscilloscope and probe have been calibrated, you are ready to start the DisplayPort Compliance Test Application and perform the measurements.

Calibrating the Oscilloscope

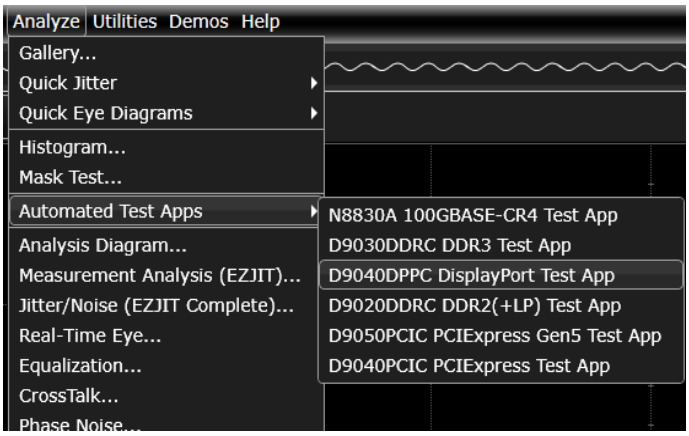
If you haven't already calibrated the oscilloscope and probe, refer to the documentation for the Infiniium Oscilloscope being used for testing, to know more about Calibration procedures. This step is not applicable to offline mode of DisplayPort Compliance Test Application.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the DisplayPort Compliance Test Application

1 From the Infiniium oscilloscope's main menu, choose **Analyze > Automated Test Apps > D9040DPPC DisplayPort Test App**.



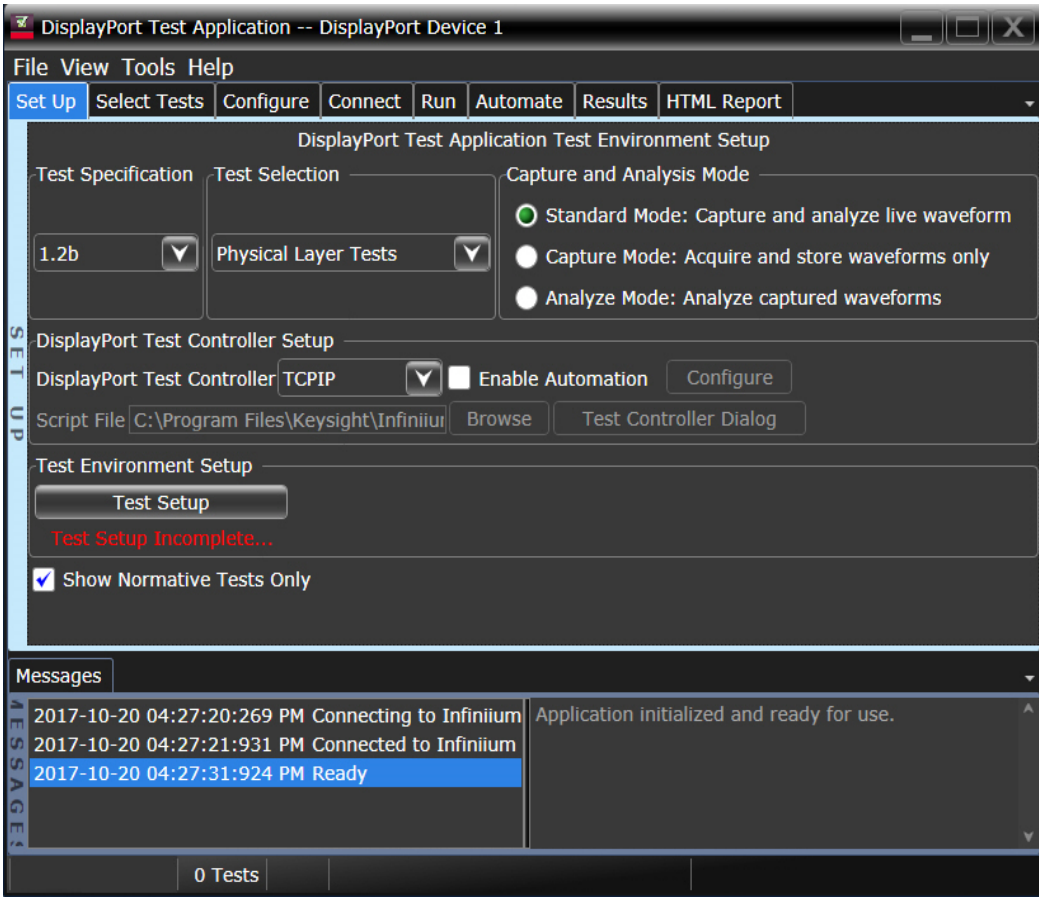


Figure 5 Default View of the DisplayPort Compliance Test Application in Online Mode

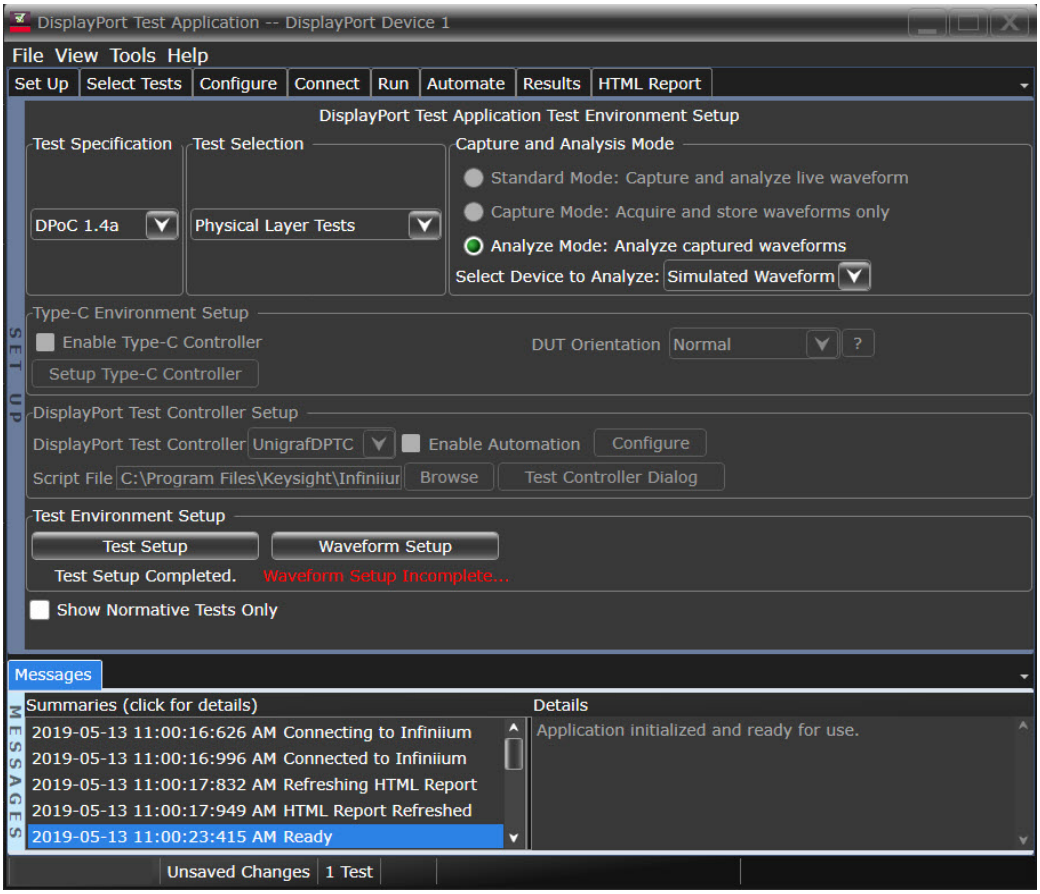


Figure 6 Default View of the DisplayPort Compliance Test Application in Offline Mode

NOTE If DisplayPort Test does not appear in the Automated Test Apps menu, the DisplayPort Compliance Test Application has not been installed (see Chapter 1, “Installing the DisplayPort Compliance Test Application).

Figure 6 shows the DisplayPort Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests.

Table 1 DisplayPort Application Tabs and Their Description

Tab	Description
Set Up	Lets you select your setup options. Allows you to setup by device type, test type, fixture type, and connection type.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically, so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you enter information about the device being tested configure test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automate	Enables construction of automated script of commands that drive the functionality of the test application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

Online Help Topics

For information on using the DisplayPort Compliance Test Application, see the Online Help (which you can access by choosing **Help > Contents...** from the application's main menu).

The DisplayPort Compliance Test Application's Online Help describes:

- Keysight D9040DPPC DisplayPort Automated Testing—At a Glance
- Starting the Keysight D9040DPPC DisplayPort Test Application
- Creating or Opening a Test Project
- Setting Up the Test Environment
- Selecting Tests
- Configuring Tests
- Verifying Physical Connections
- Running Tests
- Configuring Automation in the Test Application
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
- Additional Settings in the Test App

3 DisplayPort 1.2b Source Tests

This section provides the guidelines for source eye diagram differential tests using a Keysight 13 GHz or greater Infiniium oscilloscope, 1168A, or 1169A probes, and the DisplayPort Compliance Test Application.

Overview

This section describes the normative and informative main link physical layer tests for compliance verification of DisplayPort 1.2 source, sink and cable devices.

Test Point Definition for DisplayPort 1.2 (1.2b) Tests

Five different test points are identified for the physical layer measurement. See Figure 7

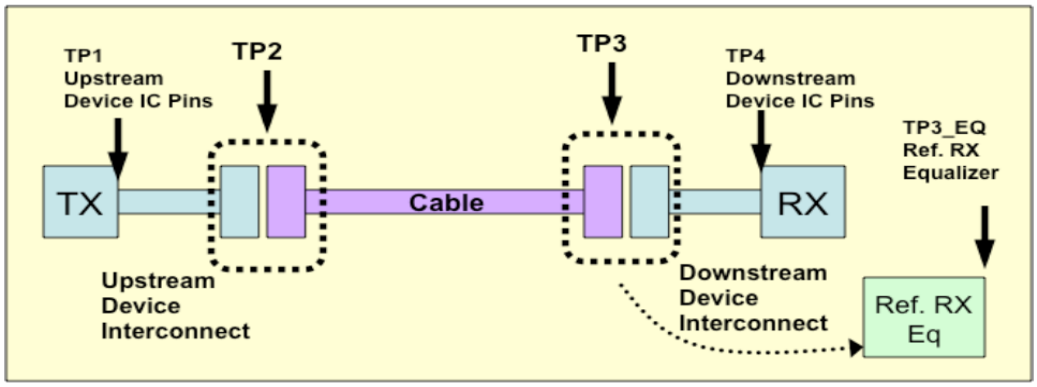


Figure 7 Test Points in a DisplayPort InterConnect System

Table 2 defines the Test Points used for various DisplayPort 1.2 Tests:

Table 2 Test Points for DisplayPort Tests

Test Point	Description
TP1	At the pins of the Transmitter Device
TP2	At the test interface on a test access fixture as close as possible to the DP mated connection to a Source device
TP3	At the test interface on a test access fixture as close as possible to the DP mated connection to a Sink device
TP3_EQ	At TP3, when a defined cable model with equalizer is applied. There are two defined cable models: ▪ Worst Cable Model as defined in VESA DisplayPort 1.2a Standard, ▪ Zero length, zero loss cable. The equalizer is also defined in VESA DisplayPort 1.2a Standard
TP4	At the pins of a receiving device

Cable Models

The two cable models defined in VESA DisplayPort 1.2a Standard are:

1 Worst Case Cable Model—To achieve the TP3_EQ signal with the worst case cable model:

- Acquire the signal at TP2.
- Embed the TP2 signal with a “worst case” cable model using an InfiniiSim Waveform Transformation Toolset software to emulate the insertion loss as defined in Figure 4-10 of the VESA DisplayPort 1.2a Standard.
  - The “*CIC_rev0p6.s4p*” cable model transfer function is used.
- Finally, apply the HBR or HBR2 equalization using the Serial Data Equalization software as defined in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard.

2 Zero Length Cable Model—To achieve the TP3_EQ signal with the zero length cable model:

- Acquire the signal at TP2.
- No cable model is embedded for the Zero Length cable model.
- Finally, apply the HBR or HBR2 equalization using the Serial Data Equalization software as defined in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard.

Equalization

When equalization is required, use the CTLE (Continuous Time Linear Equalization) transfer function, as given in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard.

For main link, use the CTLE model with the following transfer function for HBR (2.7 Gbps):

The HBR Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s + \omega_z}{(s + \omega_{p1})(s + \omega_{p2})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{\sqrt{\omega^2 + \omega_z^2}}{\sqrt{\omega^2 + \omega_{p1}^2} \cdot \sqrt{\omega^2 + \omega_{p2}^2}}$$

where

$$\omega_z = 2\pi(0.725 \times 10^9)$$

$$\omega_{p1} = 2\pi(1.35 \times 10^9)$$

$$\omega_{p2} = 2\pi(2.5 \times 10^9)$$

Figure 8 Transfer Function of the CTLE model for HBR

Table 3 CTLE Model for HBR

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
Gain	1.0	1.0
Zero Frequency	0.725 GHz	0.725 GHz
Pole 1 Frequency	1.35 GHz	1.35 GHz
Pole 2 Frequency	2.5 GHz	2.5 GHz

For main link, use the CTLE model with the following transfer function for HBR2 (5.4 Gbps):

The HBR2 Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})(s+\omega_{p3})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{\sqrt{\omega^2+\omega_z^2}}{\sqrt{\omega^2+\omega_{p1}^2}\cdot\sqrt{\omega^2+\omega_{p2}^2}\cdot\sqrt{\omega^2+\omega_{p3}^2}}$$

where

$\omega z = 2\pi\ (0.64 \times 10^9)$ for upstream device compliance

and

$\omega p1 = 2\pi\ (2.7 \times 10^9)$

$\omega p2 = 2\pi\ (4.5 \times 10^9)$

$\omega p3 = 2\pi\ (13.5 \times 10^9)$

Figure 9 Transfer Function of the CTLE model for HBR2

Table 4 CTLE Model for HBR2

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
Gain	1.0	1.0
Zero Frequency	0.64 GHz	0.64 GHz
Pole 1 Frequency	2.7 GHz	2.7 GHz
Pole 2 Frequency	4.5 GHz	4.5 GHz
Pole 3 Frequency	13.5 GHz	13.5 GHz

Clock Recovery

When Clock Recovery is required, the clock recovery technique follows the definition of the receiver PLL as defined in Section 3.5.3.5 of the VESA DisplayPort 1.2a Standard. For main link, use the second-order clock recovery function with a closed loop tracking bandwidth and damping factor, with respect to the PRBS7 pattern, as shown in Table 5:

Table 5 Main Link Second-Order Clock Recovery Function

Bit Rate	Bandwidth	Damping Factor
HBR2 (5.4 Gbps)	10 MHz	1.00
HBR (2.7 Gbps)	10 MHz	1.51
RBR (1.62 Gbps)	5.4 MHz	1.51

Test Point Definition for DisplayPort 1.2 (1.2b) Source Tests

Test the Source DUT at Test Point 2 (TP2) as shown in Figure 10. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

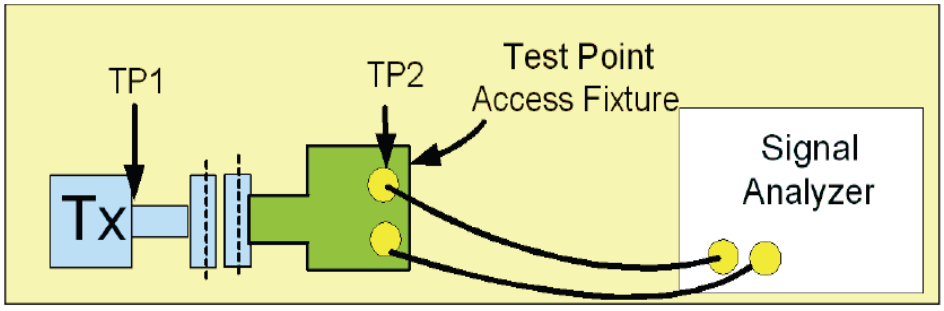


Figure 10 Test Point 2 Connection for DisplayPort 1.2 Source Tests

Table 6 defines the test point fixtures and instruments used for DisplayPort 1.2 (1.2b) Source Tests:

Table 6 Test Point Fixtures and Instruments for DisplayPort 1.2 Source Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-P* ▪ W2641B DisplayPort Test Point Access Adapter For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-P* ▪ Luxshare ICT mDP Plug (mDP-TPA-P)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort 1.2b Standards, the option **1.2b** appears by default in the **Test Specification** drop-down options.
5. The option **Physical Layer Tests** appears by default in the **Test Selection** area.
6. Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.
7. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
8. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
9. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
10. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
11. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
12. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
13. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
14. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DisplayPort 1.2 Source Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

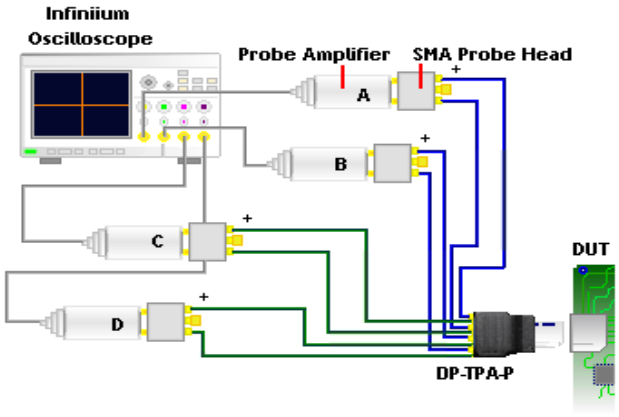


Figure 11 Sample connection diagram for DisplayPort 1.2 Source Tests with Differential Probes

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Source tests (either differential or single-ended) to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1 In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.

2 On the **Test Setup** window,

a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b In the **DUT Info** area, the **Device Type** is selected as **Source** by default.

c In the **Test Info** area, the **Test Type** is selected as **Differential Tests** by default. Select **Single-Ended Tests** from the drop-down options for the respective tests to appear in the **Select Tests** tab.

d In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.

3 Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1. Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.
2. On the **Connection Setup** window,
   a. Select the appropriate option in the **Fixture Type** to indicate where the DUT is connected to.
   b. Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.
   c. In the **Channel Selection** area, assign appropriate channels to lanes.
3. Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of source tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 88 to complete the task flow for DUT setup along with configuring the Compliance Application to run each test.

Source Eye Diagram Test

Test ID

1210001, 1210002, 1210003, 1210004 – Eye Diagram Test

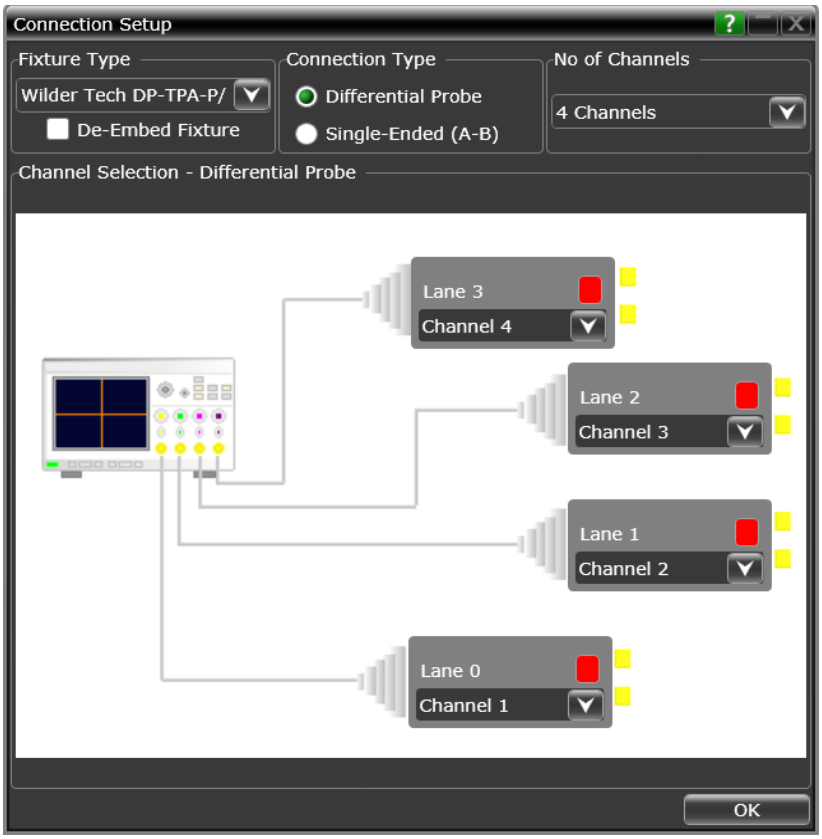
Test Overview

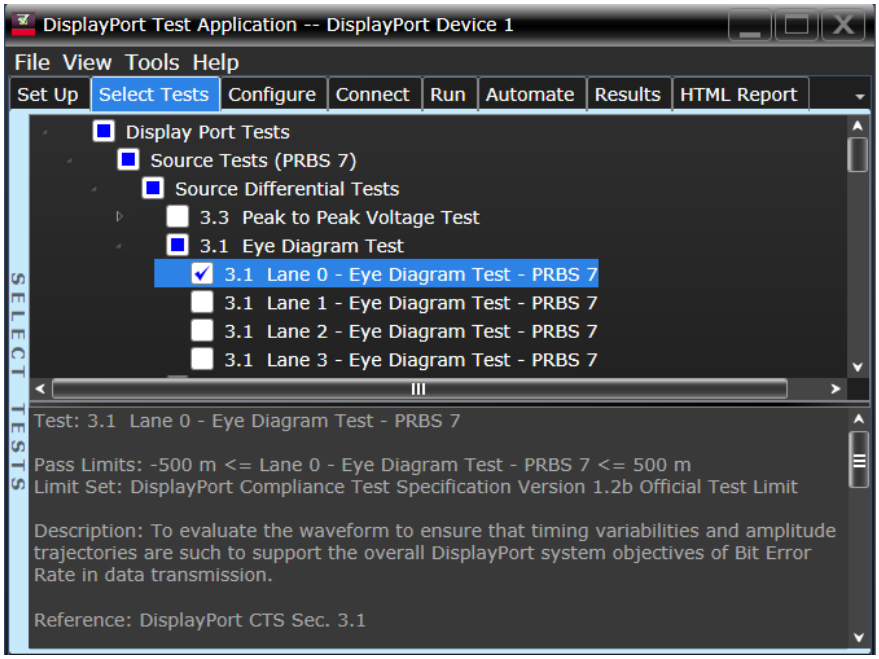
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
Spread Spectrum Clocking	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Swing 2
Pre-Emphasis Level	Level 0
Post Cursor2 Level	Level 0
Lane Setting	All test lanes supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Measure V_{TOP} and V_{BASE} of the input signal using the pattern folding.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the input signal eye diagram to measure the left edge.
7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the eye height of the eye diagram using the Histogram.
9 Measure the jitter of the eye diagram using the Histogram.
10 Calculate the eye width based on the measured jitter of the eye diagram.
11 Check for any signal trajectories that may have entered into the mask.
12 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 7 shows the voltage and time coordinates for the mask used in the eye diagram.

Table 7 Eye Diagram Mask Coordinates for HBR and RBR

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	High (2.7 Gb/s)
1	0.127, 0.000	0.210, 0.000
2	0.291, 0.160	0.355, 0.140
3	0.500, 0.200	0.500, 0.175
4	0.709, 0.200	0.645, 0.175
5	0.873, 0.000	0.790, 0.000
6	0.709,-0.200	0.645,-0.175
7	0.500,-0.200	0.500,-0.175
8	0.291,-0.160	0.355,-0.140

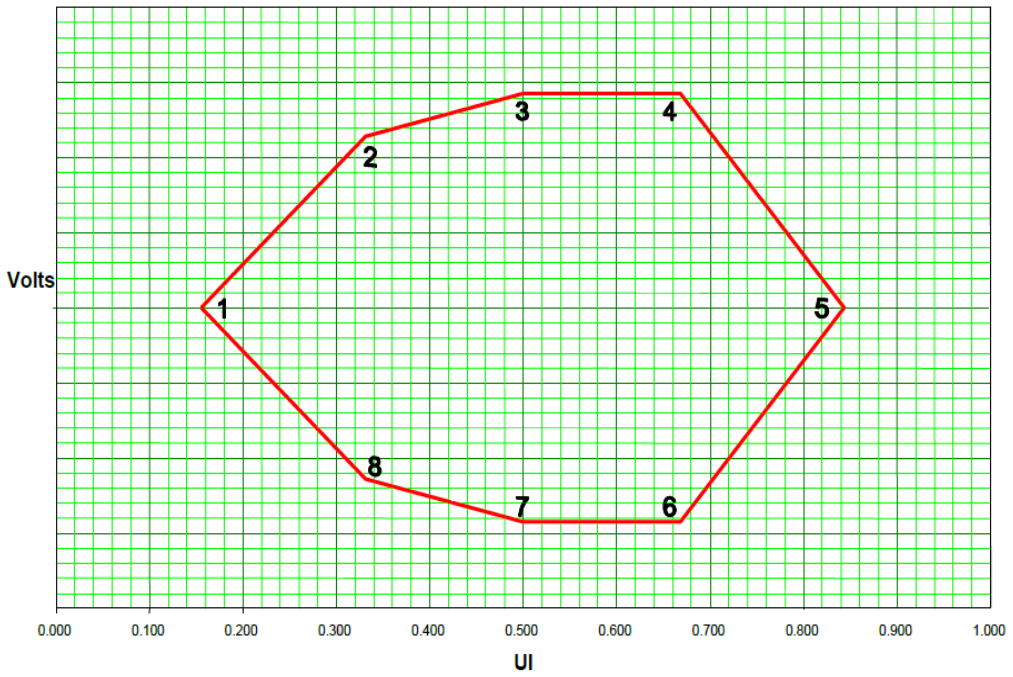


Figure 12 The Source Eye Mask

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-24 for RBR and Table 3-23 for HBR*

Expected/Observable Results

The measured eye diagram for the source degraded signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test

Test ID

1220001, 1220002, 1220003, 1220004 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

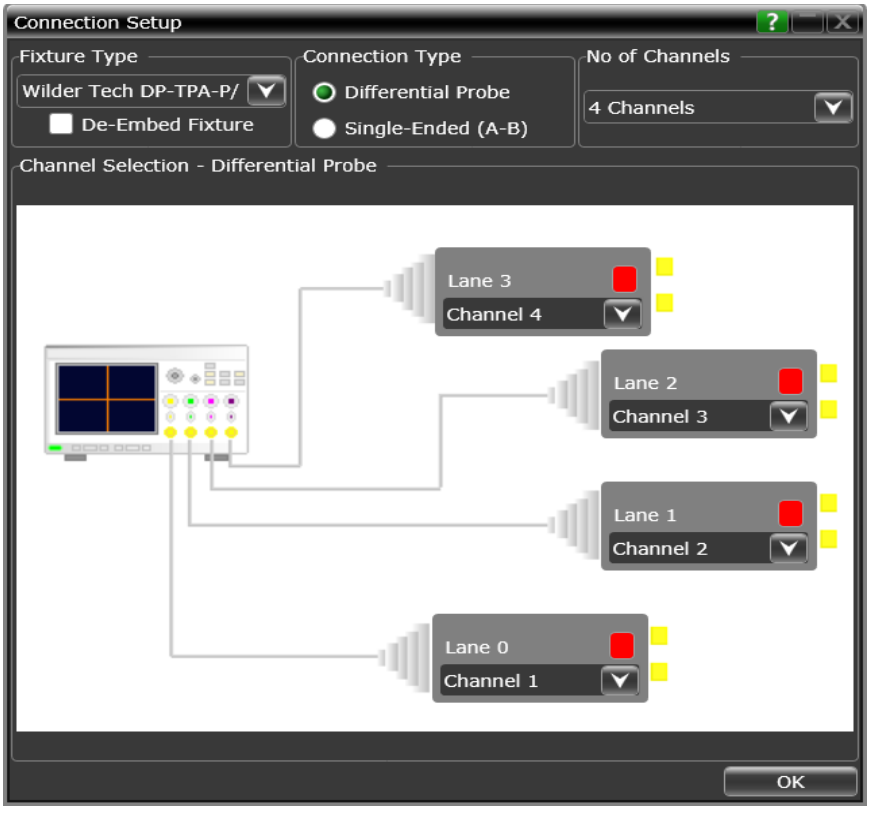
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

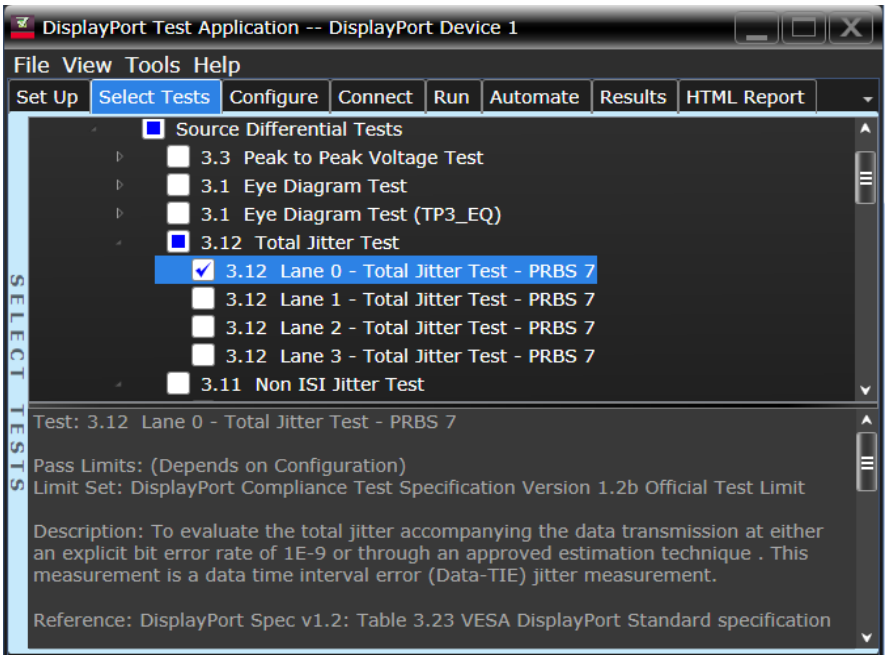
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Report the measurement results.

PASS Condition

Table 8 Total Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.294 UI	0.420 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.180 UI	0.270 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non ISI Jitter Test

Test ID

1230001, 1230002, 1230003, 1230004 – Non ISI Jitter Test

Test Overview

The objective of the test is to evaluate the amount of Non ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

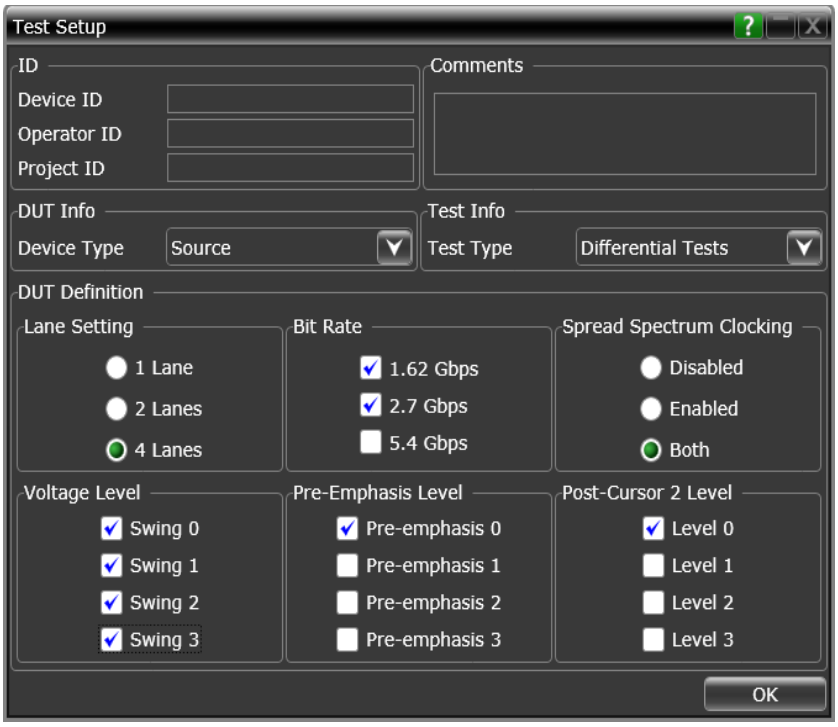
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

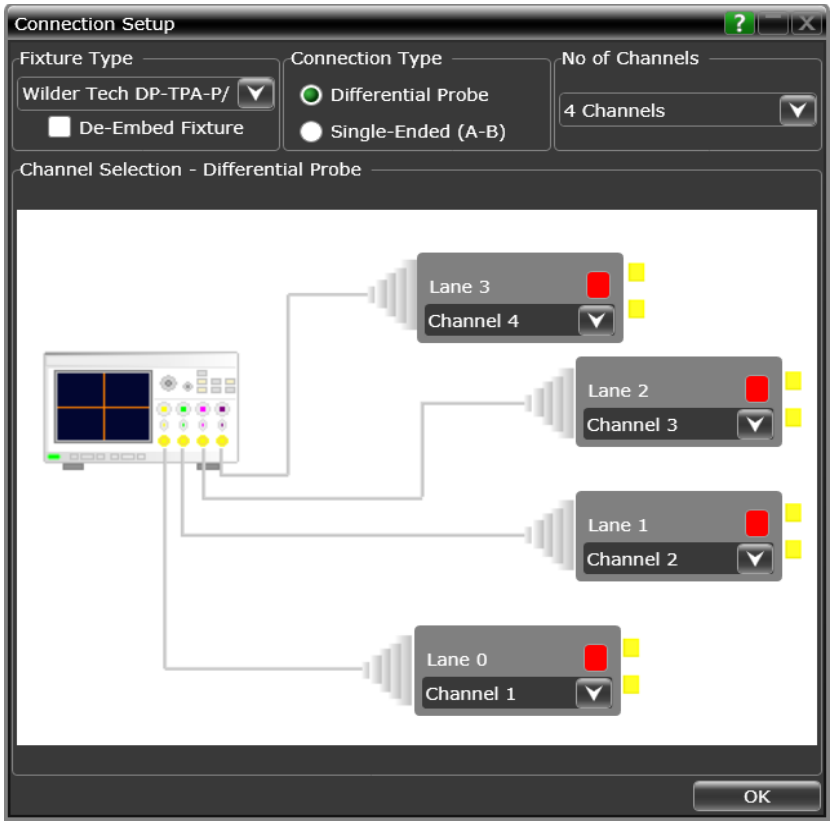
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

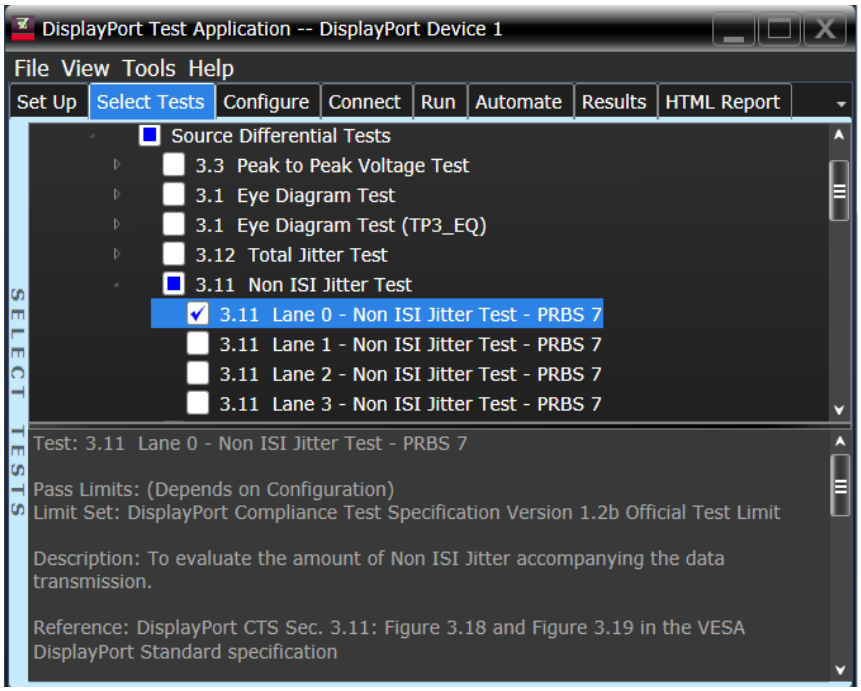
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Non ISI Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Calculate the Non ISI jitter using the following equation:

$$\text{Non ISI Jitter} = \text{TJ} - \text{ISI}$$

7 Report the measurement results.

PASS Condition

Table 9 Non-ISI Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.260 UI	0.276 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.160 UI	0.210 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.11*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Pre-Emphasis Level Test

Test ID

For RBR and HBR:

- 1261001, 1261002, 1261003, 1261004 – Non Pre-Emphasis Level Test (Swing 1/Swing 0)
- 1262001, 1262002, 1262003, 1262004 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263001, 1263002, 1263003, 1263004 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

For HBR2:

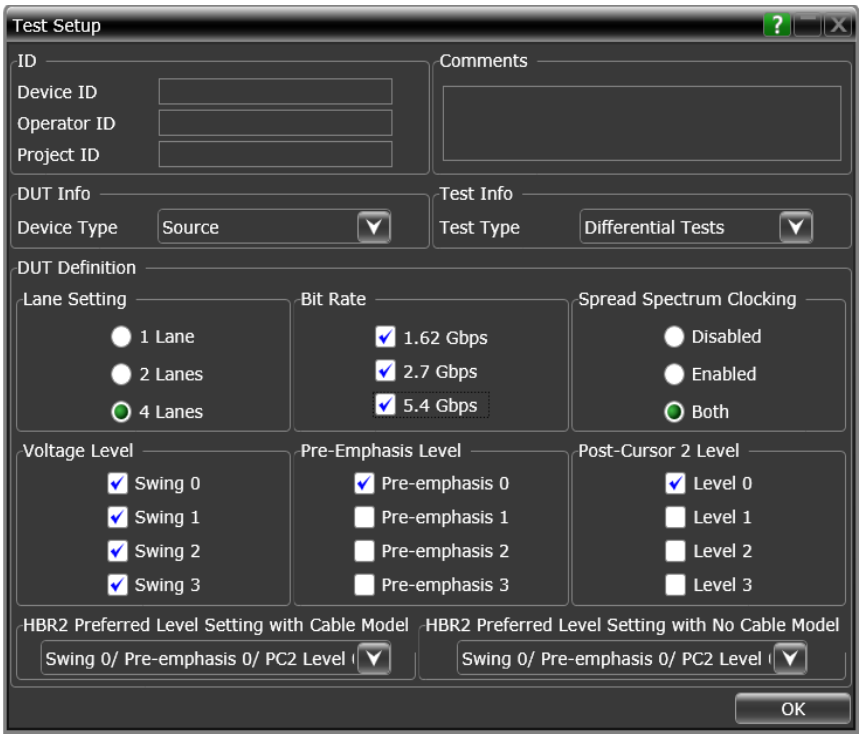
- 1264101, 1264102, 1264103, 1264104 – Non Pre-Emphasis Level Test (Swing 2/Swing 0)
- 1262101, 1262102, 1262103, 1262104 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263101, 1263102, 1263103, 1263104 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

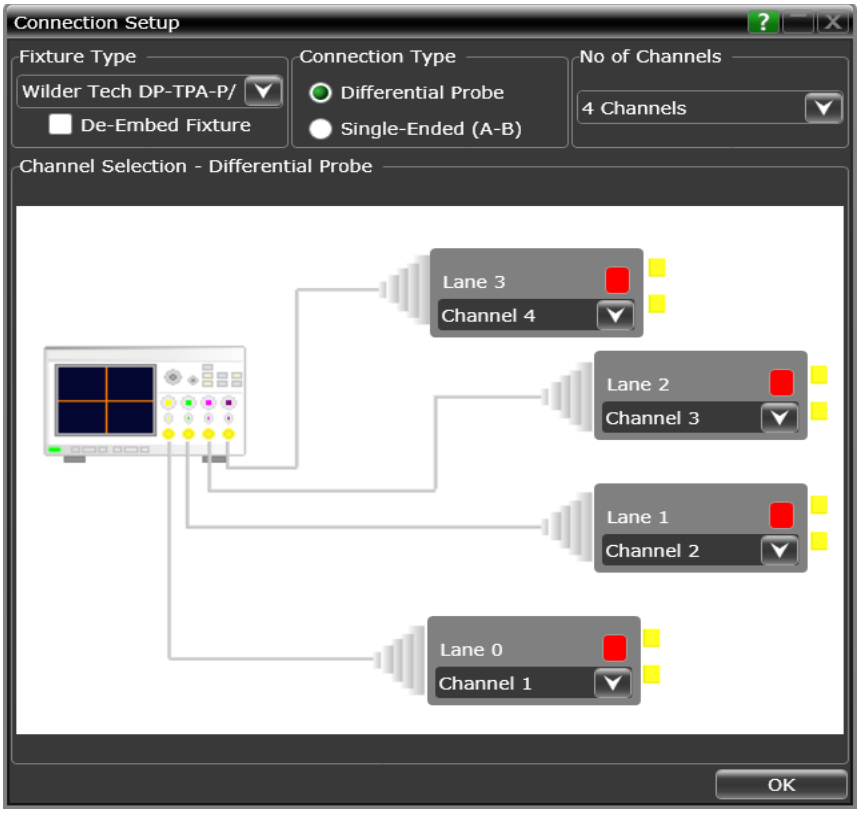
Test Overview

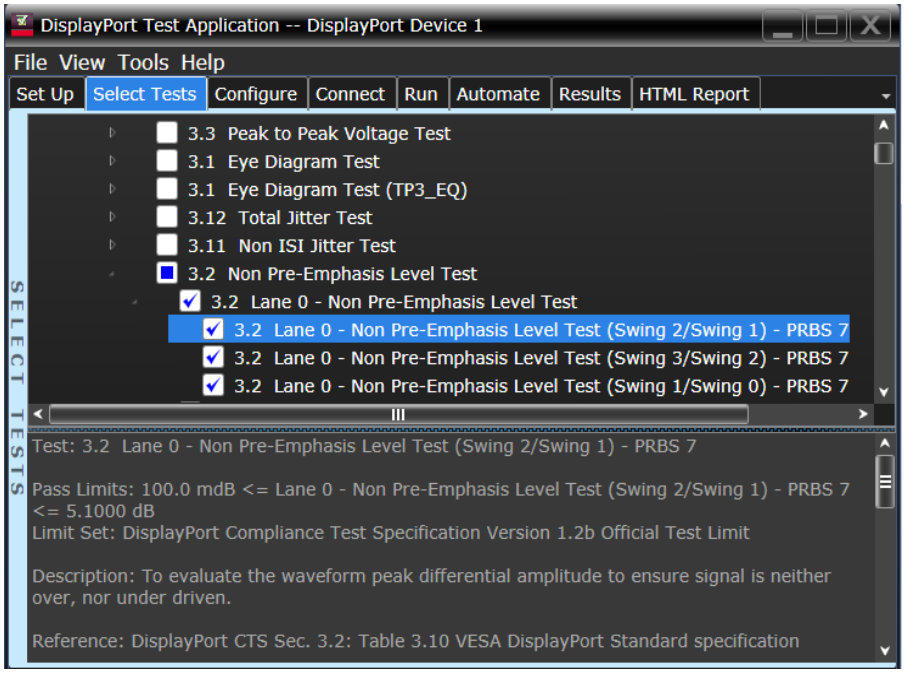
The objective of this test is to ensure that the system budget elements are obeyed and to ensure that the level settings are monotonic so that the sink relies on the source to incrementally increase upon request by the sink.

Test Conditions for Non Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7 HBR2 – PLTPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For Voltage Level A with no pre-emphasis level:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

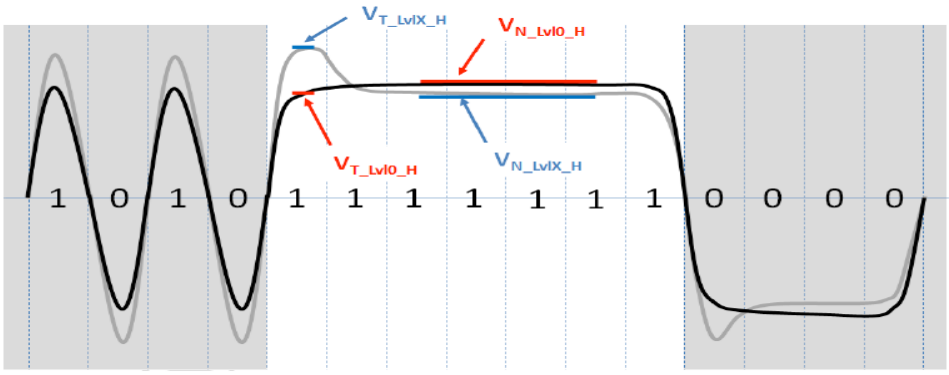


Figure 13 High Voltage measurement for RBR and HBR

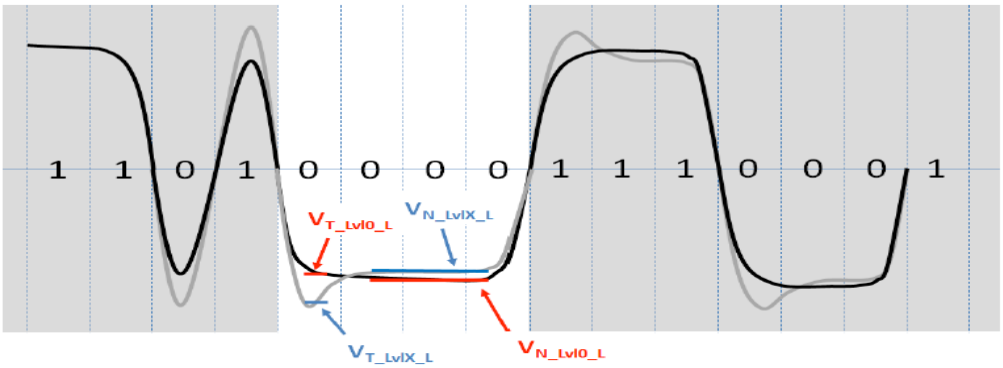


Figure 14 Low Voltage measurement for RBR and HBR

e For HBR2 using the test pattern PLTPAT:

i The qualifying pattern in PLTPAT test pattern for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

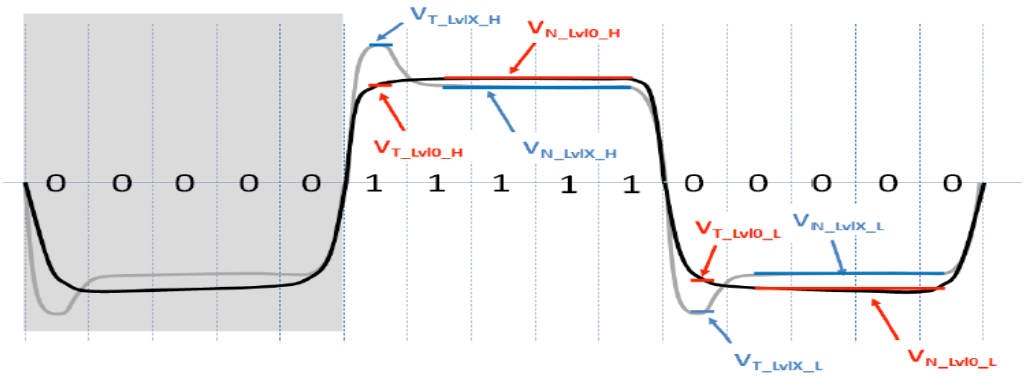


Figure 15 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_Lvl0\_PP} = V_{T\_Lvl0\_H} - V_{T\_Lvl0\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_Lvl0\_PP} = V_{N\_Lvl0\_H} - V_{N\_Lvl0\_L}$$

2 Repeat Step 1 for Voltage Level B with no pre-emphasis level.

3 Calculate the non pre-emphasis level output voltage ratio using the equation:

Non Pre-Emphasis Level = $20 * \text{Log}_{10}[\text{Voltage Level A } V_{N\_Lvl0\_PP} / \text{Voltage Level B } V_{N\_Lvl0\_PP}]$

4 Report the measurement results.

PASS Condition

For each level setting testes, the following equation should be used:

$\text{Resultant} = 20 * \text{Log}_{10}[\text{Voltage}_{\text{Peak-Peak\_LevelA}} / \text{Voltage}_{\text{Peak-Peak\_LevelB}}]$

Table 10 Compared Levels

Measurement#	$\text{Voltage}_{\text{Peak-Peak\_LevelA}}$	$\text{Voltage}_{\text{Peak-Peak\_LevelB}}$
RBR & HBR		
1	Level 1 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)
2	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
3*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)
HBR2		
4	Level 2 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)

Table 10 Compared Levels

Measurement#	$Voltage_{Peak\text{-}Peak\_LevelA}$	$Voltage_{Peak\text{-}Peak\_LevelB}$
5	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
6*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)

* if device optionally capable of Level 3

The resultants specifications are as identified below:

Measurement 1: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 2: 0.1 dB ≤ Resultant ≤ 5.1 dB

Measurement 3: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 4: 5.2 dB ≤ Resultant ≤ 6.9 dB

Measurement 5: 1.6 dB ≤ Resultant ≤ 3.5 dB

Measurement 6: 1 dB ≤ Resultant ≤ 4.4 dB

Table 11 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}OUTPUT\text{-}RATIO\_RBR\_HBR}$	Ratio of Output Voltage Level 1/Level 0	0.8	-	6.0	dB	Measured on non-transition bits at Pre-emphasis level 0 setting
	Ratio of Output Voltage Level 2/Level 1	0.1	-	5.1	dB	
	Ratio of Output Voltage Level 3/Level 2	0.8	-	6.0	dB	
$V_{TX\text{-}OUTPUT\text{-}RATIO\_HBR2}$	Ratio of Output Voltage Level 2/Level 0	5.2	-	6.9	dB	Measured on non-transition bits at Pre-emphasis level 0 setting
	Ratio of Output Voltage Level 2/Level 1	1.6	-	3.5	dB	
	Ratio of Output Voltage Level 3/Level 2	1	-	4.4	dB	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured output voltage level ratio of the non pre-emphasis level test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Pre-Emphasis Level Test

Test ID

For RBR and HBR:

- 1270001, 1270002, 1270003, 1270004 – Pre-Emphasis Level Test

For HBR2:

- 1270501, 1270502, 1270503, 1270504 – Pre-Emphasis Level Test

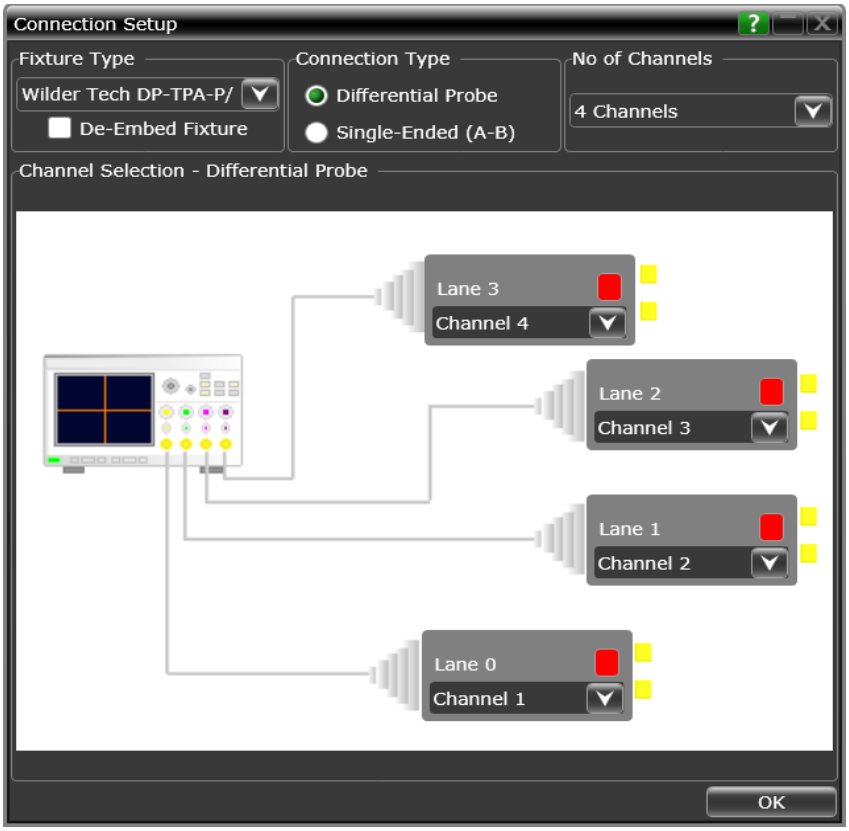
Test Overview

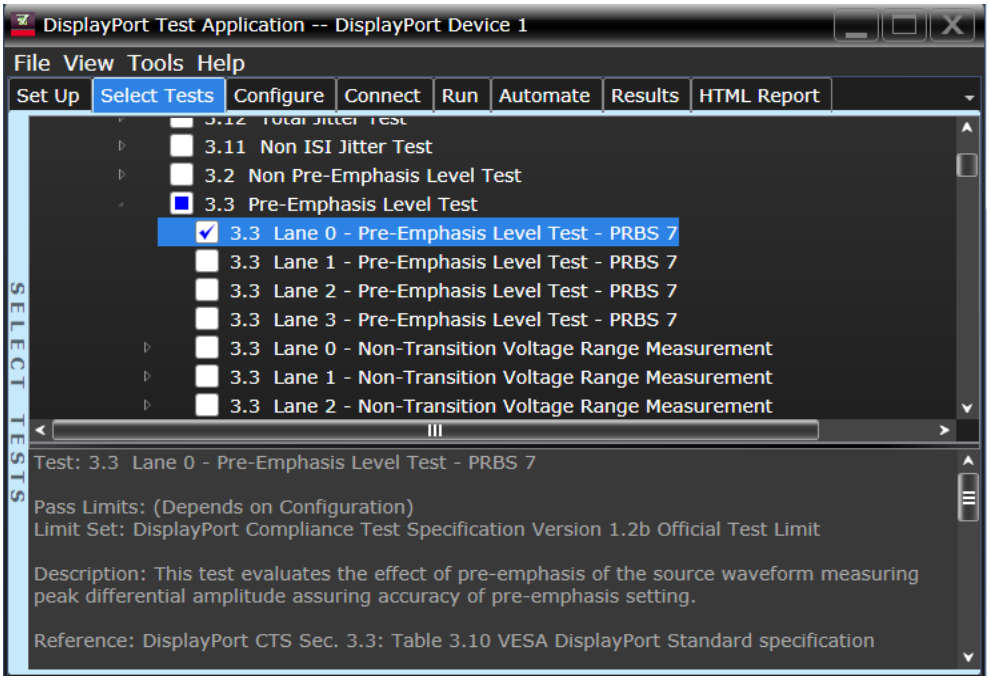
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings.

Test Conditions for Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels are supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	RBR, HBR – PRBS7 HBR2 – PLTPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given Voltage Level and a Pre-Emphasis Level X:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

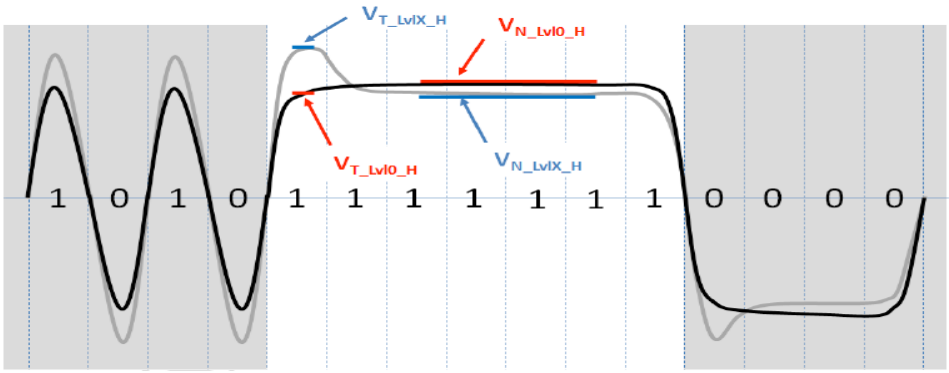


Figure 16 High Voltage measurement for RBR and HBR

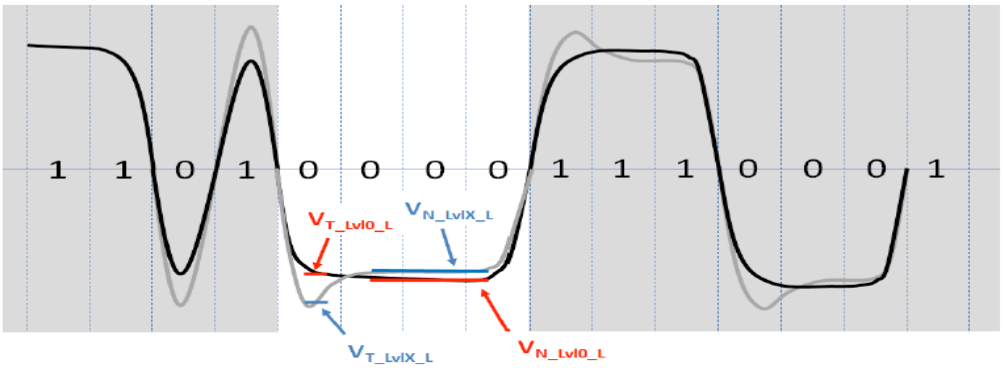


Figure 17 Low Voltage measurement for RBR and HBR

e For HBR2 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PLTPAT for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted zeros of the pattern.

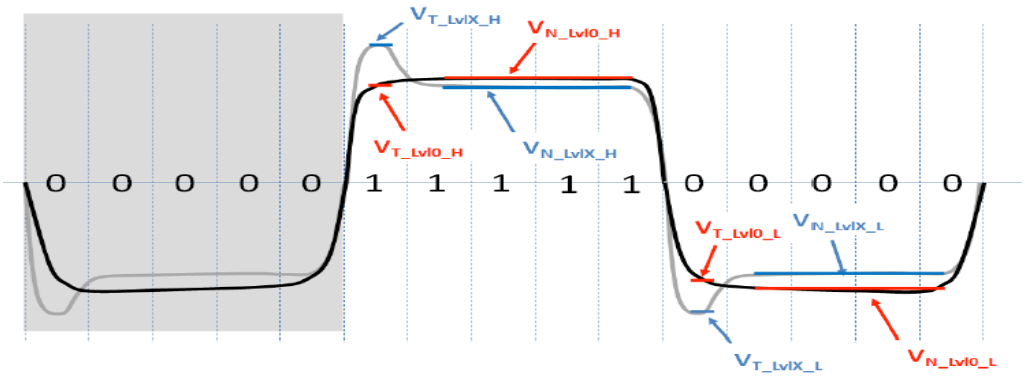


Figure 18 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

l Calculate the pre-emphasis level using the equation:

$$\text{Pre-Emphasis}_{LvlX} = 20 * \text{Log}_{10}[V_{T\_LvlX\_PP} / V_{N\_LvlX\_PP}]$$

2 For Pre-Emphasis Level 0 (no pre-emphasis level), the result for $\text{Pre-Emphasis}_{Lvl0}$ is compared with the maximum pre-emphasis disabled limit.

3 Repeat Step 1 for the next Pre-Emphasis level and for each Pre-Emphasis levels, compare the pre-emphasis delta with the pre-emphasis delta limits.

4 Calculate the pre-emphasis delta using the equation:

$$\text{Pre-Emphasis Delta (Level 1 vs Level 0)} = \text{Pre-Emphasis}_{Lvl1} - \text{Pre-Emphasis}_{Lvl0}$$

$$\text{Pre-Emphasis Delta (Level 2 vs Level 1)} = \text{Pre-Emphasis}_{Lvl2} - \text{Pre-Emphasis}_{Lvl1}$$

$$\text{Pre-Emphasis Delta (Level 3 vs Level 2)} = \text{Pre-Emphasis}_{Lvl3} - \text{Pre-Emphasis}_{Lvl2}$$

5 Report the measurement results.

PASS Condition

Pre-emphasis values for the Level 0 (OFF) state (Normative)

Level 0 (OFF) Pre-emphasis measurement:

Resultant = 20 * Log [$Voltage_{T\_Lvl0\_PP}$ / $Voltage_{N\_Lvl0\_PP}$] for all supported levels.

Level 0 (OFF) Pre-emphasis Measurement condition: +0.25 dB $\geq$ Resultant

Pre-emphasis Delta values for:

a Level 1 vs. Level 0 Pre-emphasis settings (NORMATIVE)

b Level 2 vs. Level 1 Pre-emphasis settings (NORMATIVE)

c Level 3 vs. Level 2 Pre-emphasis settings (NORMATIVE)

Pre-emphasis Delta measurements:

- Level 1 vs. Level 0

Resultant = 20 * Log [$Voltage_{T\_Lvl1\_PP}$ / $Voltage_{N\_Lvl1\_PP}$] - 20 * Log [$Voltage_{T\_Lvl0\_PP}$ / $Voltage_{N\_Lvl0\_PP}$] for Voltage Swing Levels 0, 1 and 2.

- Level 2 vs. Level 1

Resultant = 20 * Log [$Voltage_{T\_Lvl2\_PP}$ / $Voltage_{N\_Lvl2\_PP}$] - 20 * Log [$Voltage_{T\_Lvl1\_PP}$ / $Voltage_{N\_Lvl1\_PP}$] for Voltage Swing Levels 0 and 1.

- Level 3 vs. Level 2

Resultant = 20 * Log [$Voltage_{T\_Lvl3\_PP}$ / $Voltage_{N\_Lvl3\_PP}$] - 20 * Log [$Voltage_{T\_Lvl2\_PP}$ / $Voltage_{N\_Lvl2\_PP}$] for Voltage Swing Level 0, if supported.

Table 12 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX\text{-}PREEMP\text{-}OFF}$	Maximum Pre-emphasis when disabled	-	-	0.25	dB	Pre-emphasis Level 0 setting must not show any pre-emphasis at TP2 to prevent link training issues.
$V_{TX\text{-}PREEMP\text{-}DELTA}$	Delta of Pre-emphasis Level 1 vs. Level 0	2	-	-	dB	Applies to all valid voltage settings. Measured at Pre-emphasis Post Cursor2 Level 0. Support for Pre-emphasis Level 3 is optional.
	Delta of Pre-emphasis Level 2 vs. Level 1	1.6	-	-	dB	
	Delta of Pre-emphasis Level 3 vs. Level 2	1.6	-	-	dB	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured pre-emphasis level or pre-emphasis delta for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Transition Voltage Range Measurement Test

Test ID

For RBR and HBR:

- 1272001, 1272002, 1272003, 1272004 – Non Transition Voltage Range Measurement (Swing 0)
- 1273001, 1273002, 1273003, 1273004 – Non Transition Voltage Range Measurement (Swing 1)
- 1274001, 1274002, 1274003, 1274004 – Non Transition Voltage Range Measurement (Swing 2)

For HBR2:

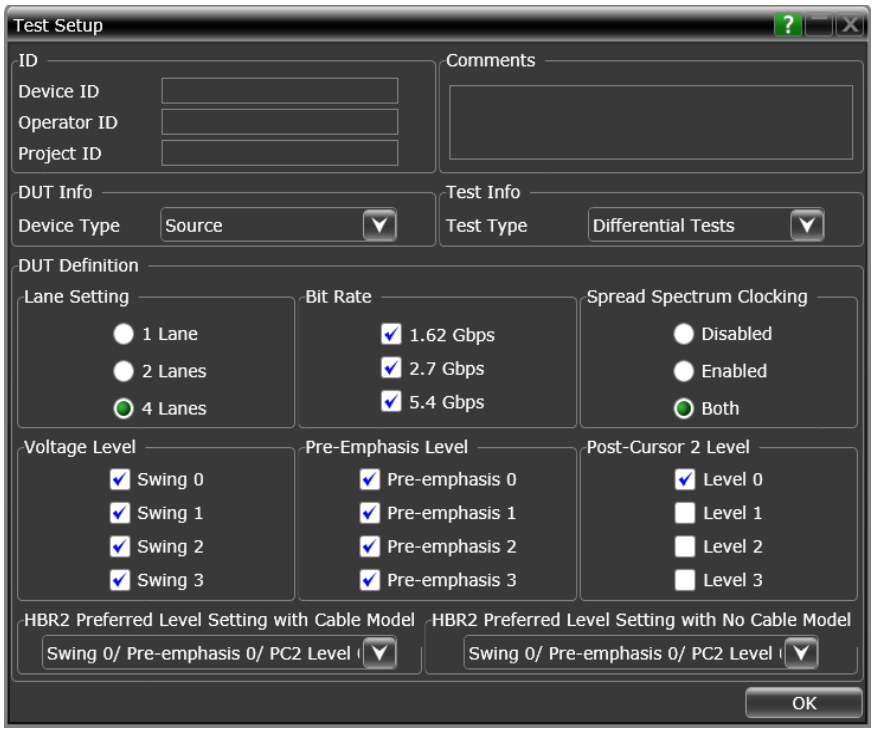
- 1272101, 1272102, 1272103, 1272104 – Non Transition Voltage Range Measurement (Swing 0)
- 1273101, 1273102, 1273103, 1273104 – Non Transition Voltage Range Measurement (Swing 1)
- 1274101, 1274102, 1274103, 1274104 – Non Transition Voltage Range Measurement (Swing 2)

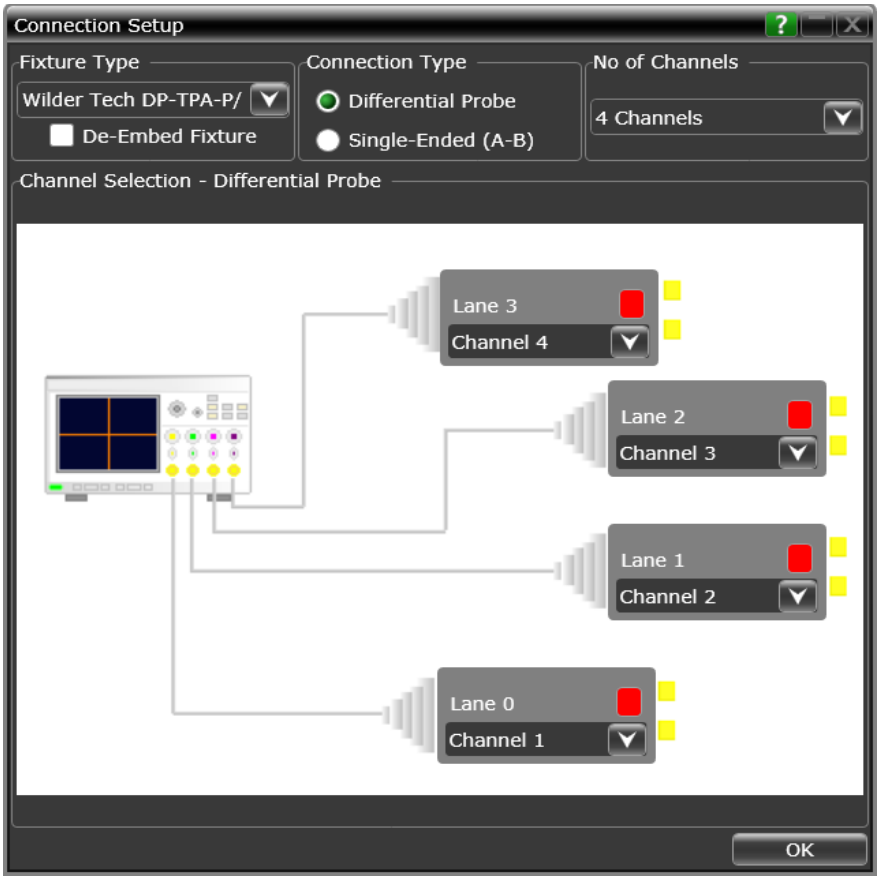
Test Overview

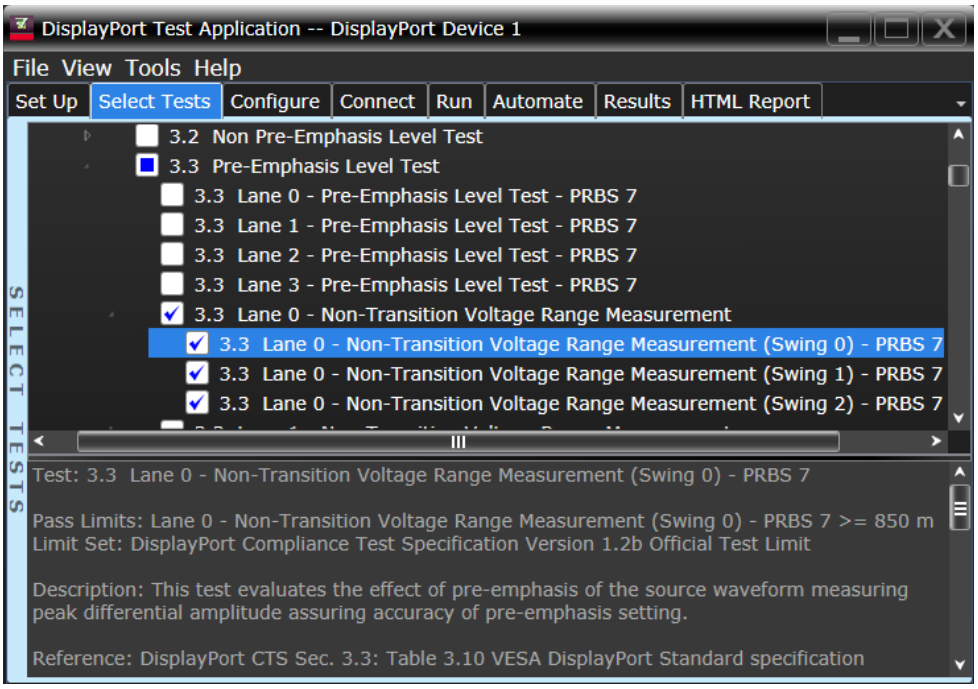
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings. Comparisons are also made for the Level 0 transition state as well as non-transition levels.

Test Conditions for Non Transition Voltage Range Measurement Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels are supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	RBR, HBR – PRBS7 HBR2 – PLTPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given Voltage Level, repeat the following steps for all pre-emphasis levels subjected to constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

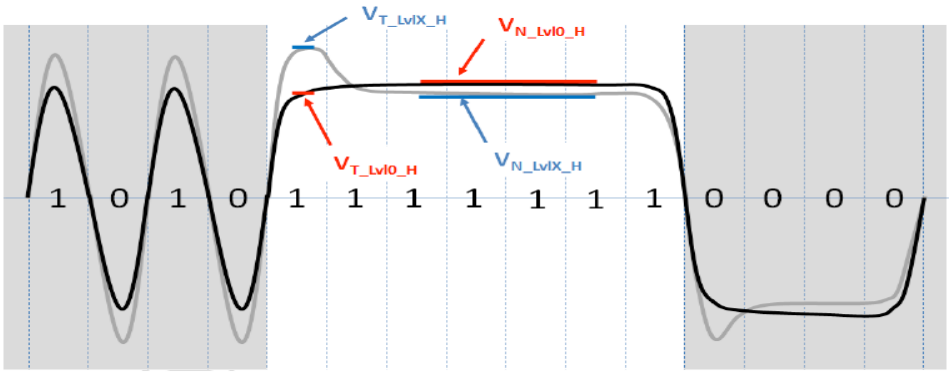


Figure 19 High Voltage measurement for RBR and HBR

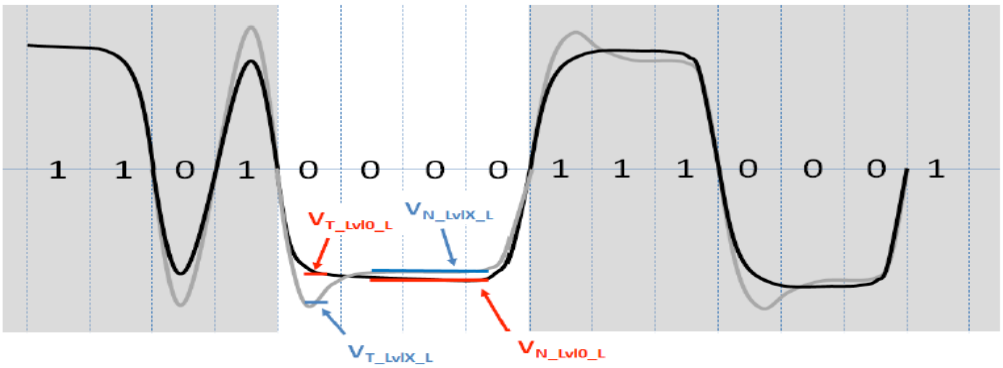


Figure 20 Low Voltage measurement for RBR and HBR

e For HBR2 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PLTPAT for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted zeros of the pattern.

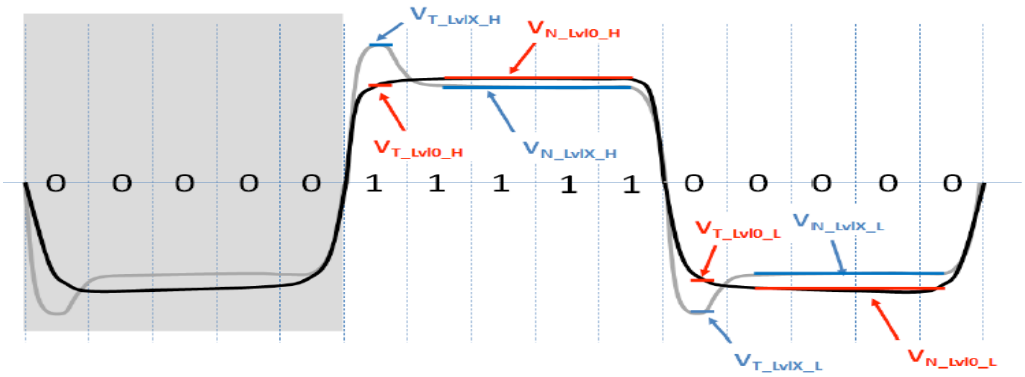


Figure 21 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

2 Calculate the non transition voltage range using the equation:

$$\text{Non Transition Voltage Range} = \text{Minimum } [(V_{N\_LvlX\_PP}) / (V_{N\_Lvl0\_PP})]$$

where, $V_{N\_LvlX\_PP}$) refers to all supported pre-emphasis levels (Level1, Level2, Level3 and so on up to Level X).

3 Report the measurement results.

PASS Condition

Non-Transition Voltage Range Measurements

For Level 2 voltage setting: Resultant > 0.708 OR 20*log(Resultant) > -3dB

For Level 1 voltage setting: Resultant > 0.708 OR 20*log(Resultant) > -3dB

For Level 0 voltage setting: Resultant > 0.85 OR 20*log(Resultant) > -1.4dB

Table 13 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX-DIFF\_REDUCTION}$	Non-transition reduction Output Voltage Level 2	-	-	3	dB	$V_{TX-DIFF}$ at each non-zero nominal pre-emphasis level must not be lower than the specified amount less than $V_{TX-DIFF}$ at the zero nominal pre-emphasis level.
	Non-transition reduction Output Voltage Level 1	-	-	3	dB	
	Non-transition reduction Output Voltage Level 0	-	-	1.4	dB	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured output voltage level reduction of the non transition bit for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Peak to Peak Voltage Test

Test ID

For RBR and HBR:

- 1266001, 1266002, 1266003, 1266004 – Peak to Peak Voltage Test

For HBR2:

- 1266101, 1266102, 1266103, 1266104 – Peak to Peak Voltage Test

Test Overview

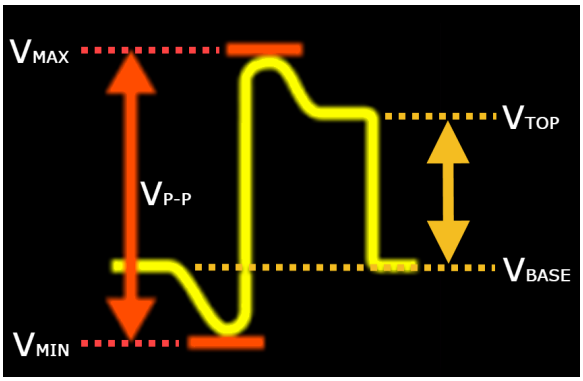
The objective of this test is to evaluate the maximum differential peak to peak voltage.

NOTE

The peak to peak voltage (V_{P-P}) formula is:

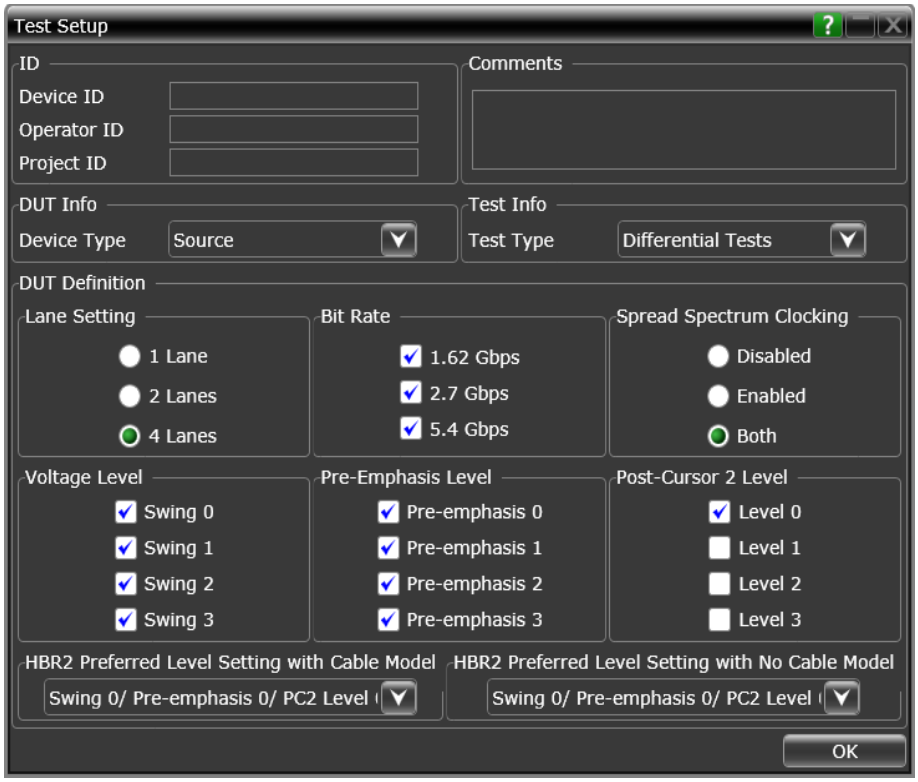
$$V_{P-P} = V_{MAX} - V_{MIN}$$

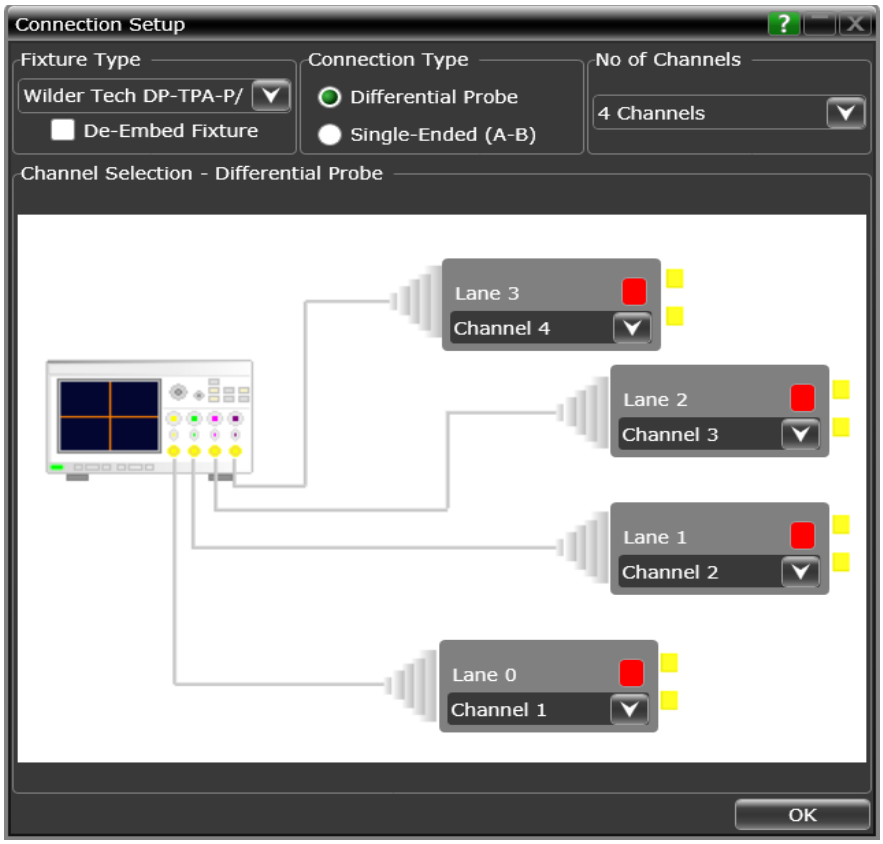
Please see the figure below for more info.

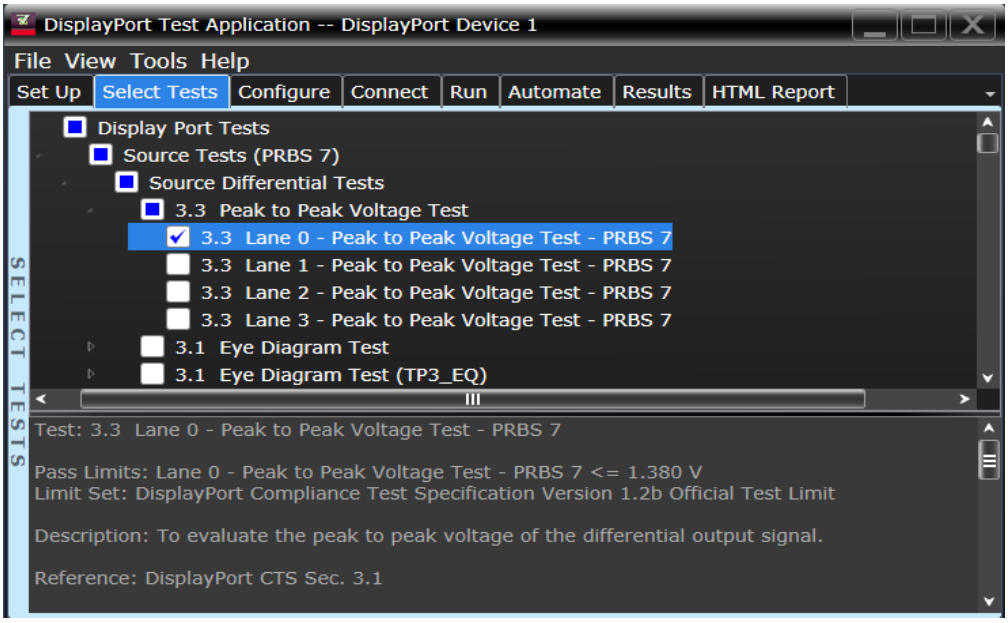


Test Conditions for Peak to Peak Voltage Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels are supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	RBR, HBR – PRBS7 HBR2 – PLTPAT




Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
Display Port Tests
Source Tests (PRBS 7)
Source Differential Tests
3.3 Peak to Peak Voltage Test
3.3 Lane 0 - Peak to Peak Voltage Test - PRBS 7
3.3 Lane 1 - Peak to Peak Voltage Test - PRBS 7
3.3 Lane 2 - Peak to Peak Voltage Test - PRBS 7
3.3 Lane 3 - Peak to Peak Voltage Test - PRBS 7
3.1 Eye Diagram Test
3.1 Eye Diagram Test (TP3_EQ)
SELECT TESTS
Test: 3.3 Lane 0 - Peak to Peak Voltage Test - PRBS 7
Pass Limits: Lane 0 - Peak to Peak Voltage Test - PRBS 7 <= 1.380 V
Limit Set: DisplayPort Compliance Test Specification Version 1.2b Official Test Limit
Description: To evaluate the peak to peak voltage of the differential output signal.
Reference: DisplayPort CTS Sec. 3.1

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{MAX} and V_{MIN} of the input signal.
   d Measure the data rate of the input signal.
3 Measure the maximum and minimum voltage of the input signal.
4 Calculate the peak to peak voltage using the equation:

$$\text{Peak to Peak Voltage} = V_{MAX} - V_{MIN}$$

5 Report the measurement results.

PASS Condition

For all Data Rates:

Maximum Differential Peak to Peak Voltage $\leq$ 1.38V

Table 14 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}DIFFp\text{-}p\_MAX}$	Max Output Voltage Level	-	-	1.38	V	For all Output Level and Pre-emphasis combinations.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured peak to peak voltage for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Inter Pair Skew Test

Test ID

1290001 – Lane0/Lane1 Inter-Pair Skew Test

1290002 – Lane0/Lane2 Inter-Pair Skew Test

1290003 – Lane0/Lane3 Inter-Pair Skew Test

1290004 – Lane1/Lane2 Inter-Pair Skew Test

1290005 – Lane1/Lane3 Inter-Pair Skew Test

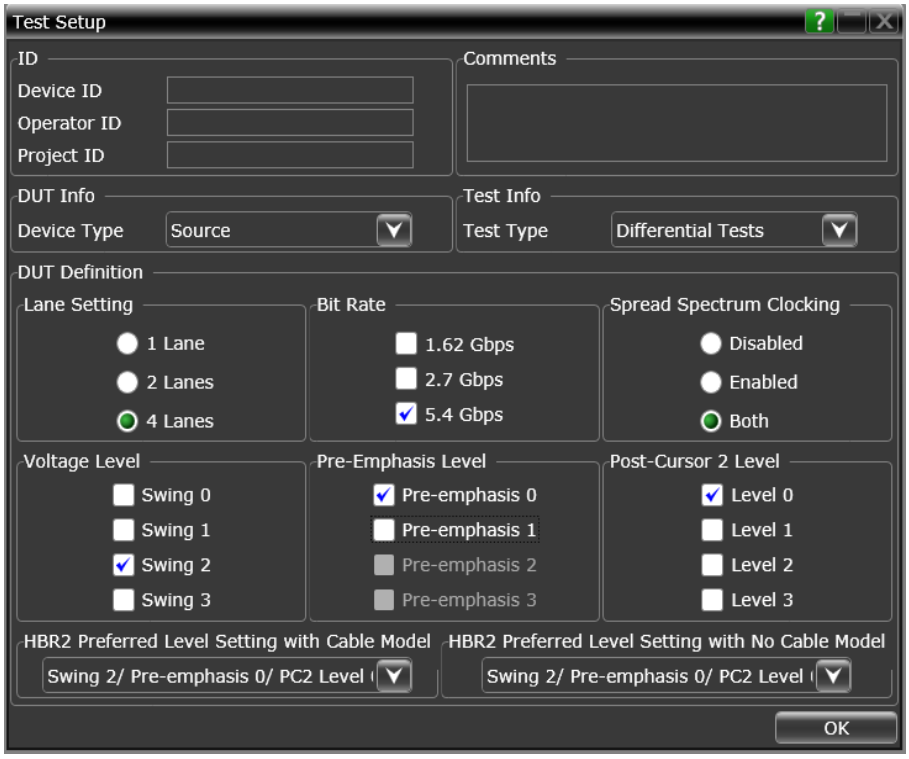
1290006 – Lane2/Lane3 Inter-Pair Skew Test

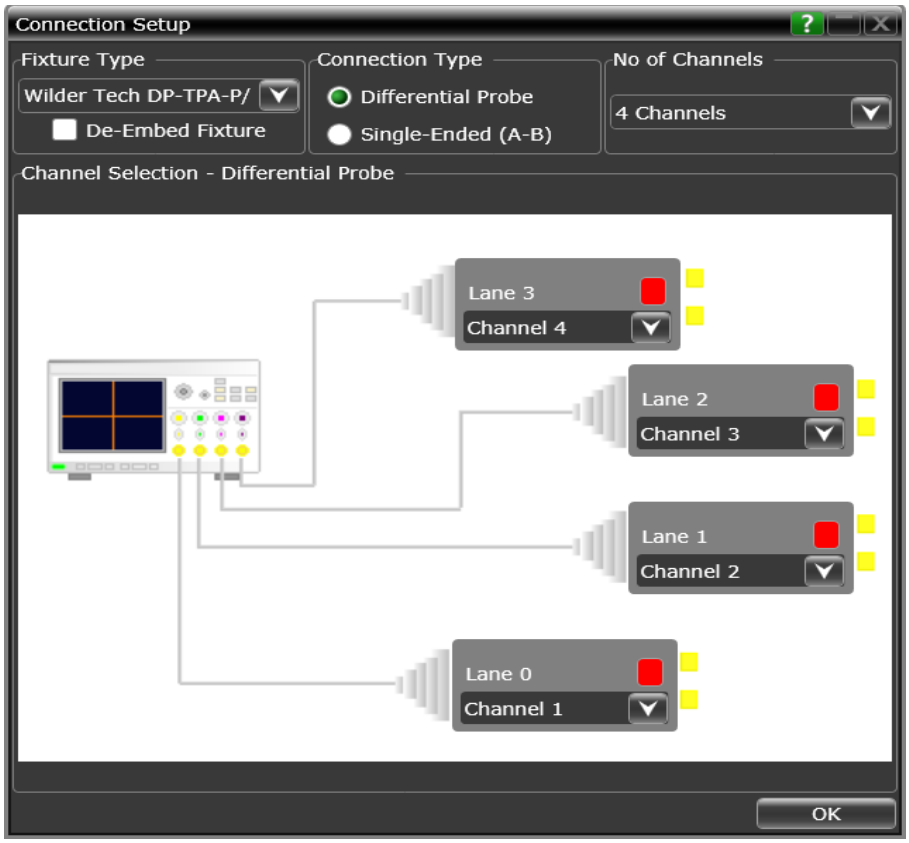
Test Overview

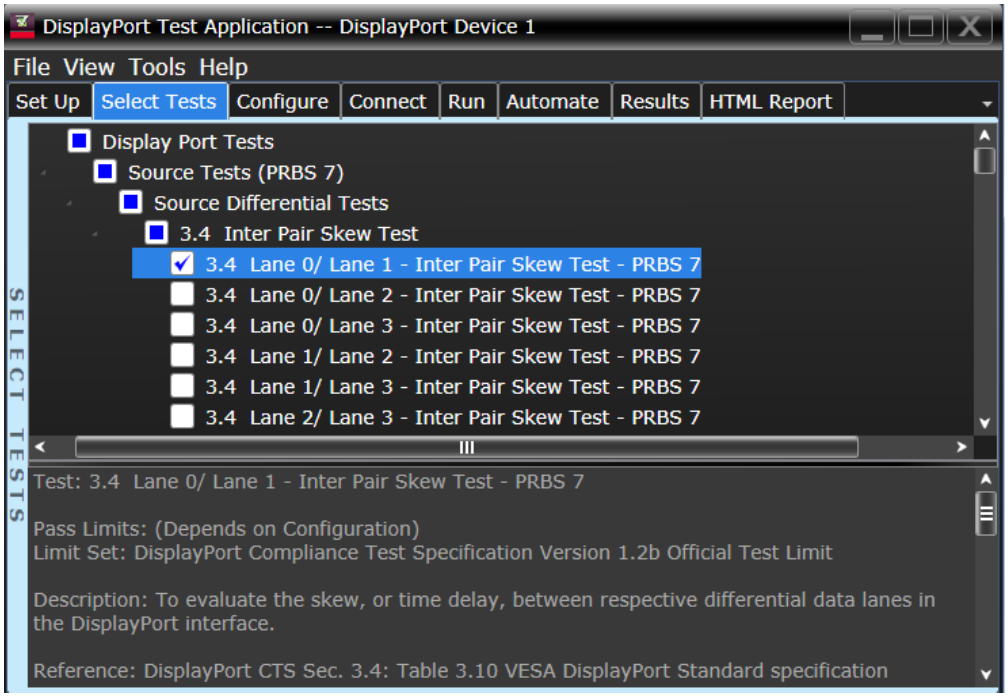
The objective of the test is to evaluate the skew or time delay between differential data lanes in the DisplayPort interface.

Test Conditions for Inter Pair Skew Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported For two lane operation: Lane 0 to Lane 1 For four lane operation: Lane 0 to Lane 1 Lane 0 to Lane 2 Lane 0 to Lane 3 Lane 1 to Lane 2 Lane 1 to Lane 3 Lane 2 to Lane 3
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given inter-pair skew measurement of Lane A to Lane B:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the Lane A input signal.

ii Scale the vertical display of the Lane A input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the Lane A input signal.

iv Verify the trigger and the amplitude of the Lane B input signal.

v Scale the vertical display of the Lane B input signal to optimum value.

vi Measure V_{TOP} and V_{BASE} of the Lane B input signal.

vii Measure the data rate of the Lane A input signal.

viii Measure the data rate of the Lane B input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

d Set up the parameter for the inter-pair skew measurement:

i Set up two display grids such that each grid displays one test lane data signal.

ii Set up the measurement threshold for each test lane data signal on the Transition Voltage = 0V.

iii Decode the data signal for each test lane.

iv Search the desired pattern from the decoded data signal.

v Measure the time difference between the corresponding edges of both test lanes:

$T_{Transition\_LaneA} - T_{Transition\_LaneB}$

vi Repeat the previous step until you measure 100 edges.

vii VESA DisplayPort 1.2a Standard specifies 20 UI offset Lane 0 to Lane 1, Lane 1 to Lane 2 and Lane 2 to Lane 3. The resultant offset is cumulative.

viii Calculate the inter-pair skew using the equation:

$$\text{Inter-Pair Skew} = \{1/\text{Number of Edges}\} \sum|T_{Transition\_LaneA} - T_{Transition\_LaneB}| - \text{Nominal Skew}$$

where, Nominal Skew is the expected offset between tested lanes.

2 Report the measurement results.

PASS Condition

For RBR or HBR: -2UI $\leq$ Inter-Lane Skew Tolerance $\leq$ 2UI.

For HBR2: -(4UI + 500ps) $\leq$ Inter-Lane Skew Tolerance $\leq$ (4UI + 500ps).

Table 15 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$L_{TX-SKEW-INTER\_PAIR-HBR\_RBR}$	Lane-to-Lane Output Skew	-	-	2	UI	Applies to transmitters capable of 2- and 4-lane operation. Also, applies to all pairwise combinations of supported lanes.
$L_{TX-SKEW-INTER\_PAIR-HBR2}$	Lane-to-Lane Output Skew	-	-	4UI + 500ps		

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured inter-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Main Link Frequency Compliance Test

Test ID

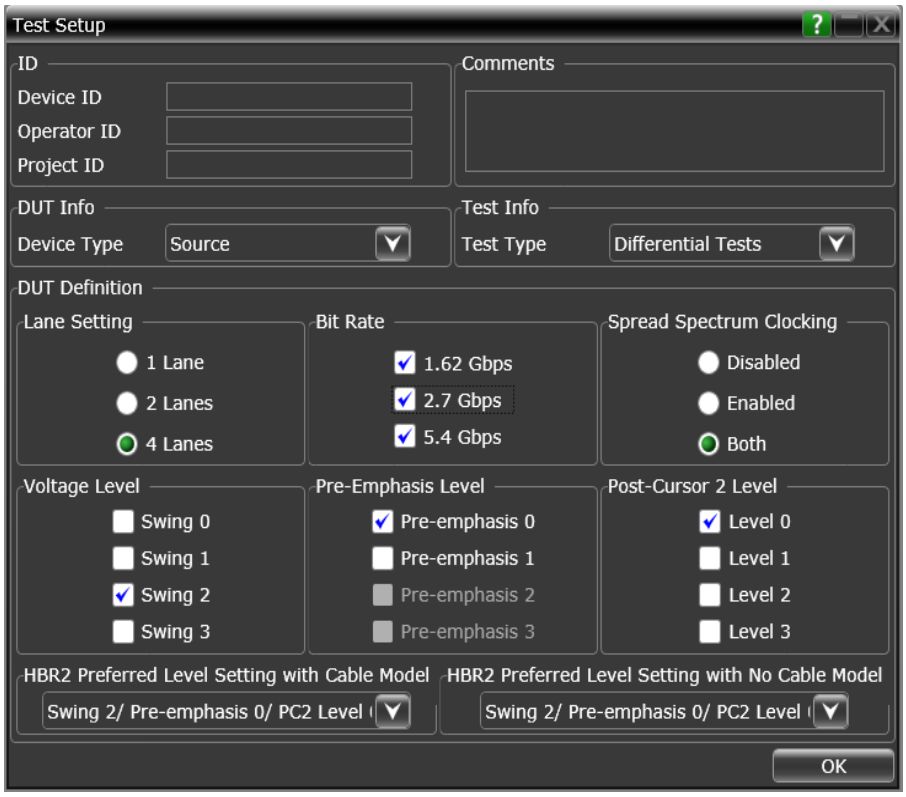
12193001 12193002 12193003 12193004 — Main Link Frequency Compliance

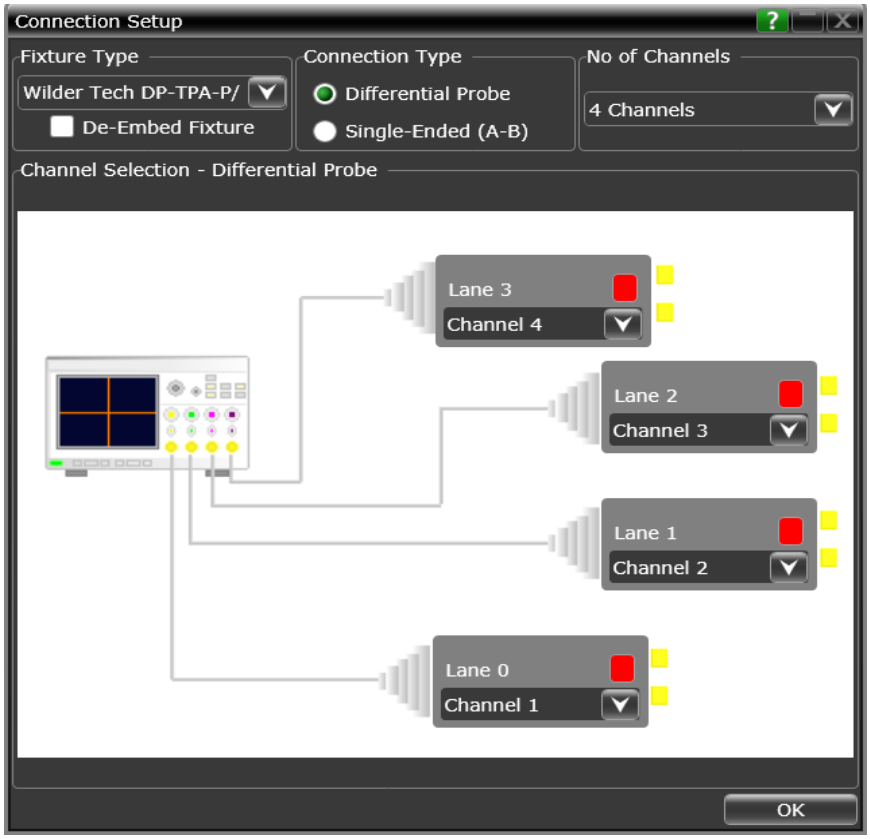
Test Overview

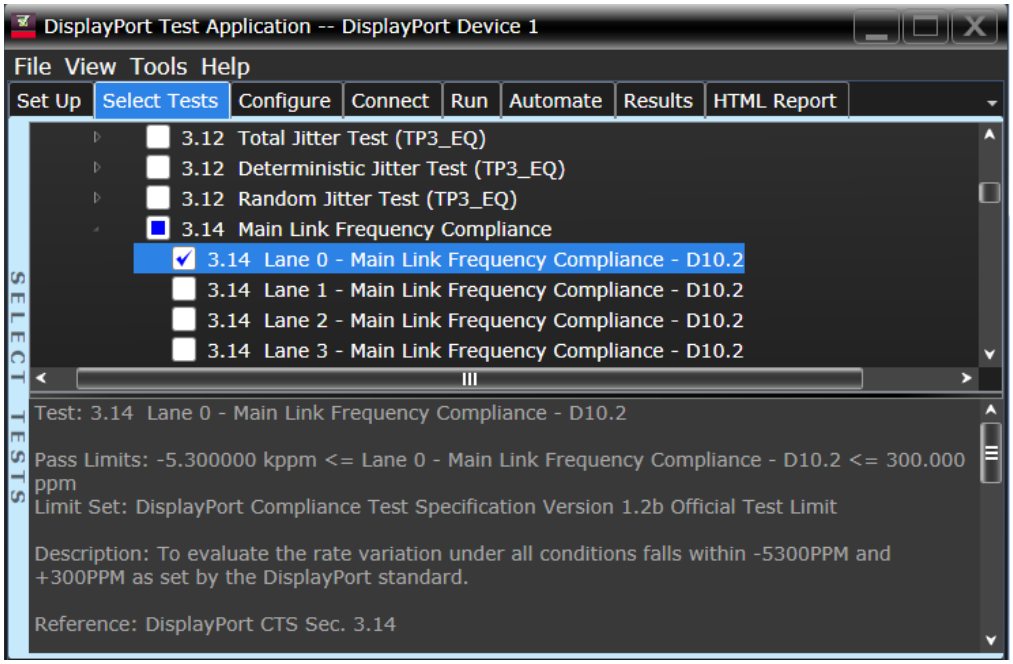
The objective of this test is to ensure that the average data rate under all conditions does not exceed the minimum and maximum values as set by the VESA DisplayPort 1.2a Standard.

Test Conditions for Main Link Frequency Compliance Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.

5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and the minimum measurement levels for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurement levels for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e For SSC Enabled Test condition, check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.
9 For the test condition “SSC Enabled”, set up the parameter of the SSC measurement:
   a Set up the memory depth and time-base to display one complete SSC cycle based on the measured SSC modulation frequency in Step 5.
   b Acquire the signal with one complete SSC cycle.
   c Get the minimum of FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

      Maximum Data Rate = 1 / (Minimum Unit Interval)

   d Get the maximum of FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

      Minimum Data Rate = 1 / (Maximum Unit Interval)

   e Repeat steps b, c and d until you acquire 10 SSC Cycles.
   f Calculate the mean value for the maximum and minimum data rates.
10 Report the measurement results.

PASS Condition

Maximum Data Rate (Frequency Max_{ppm}) $\leq$ 300 ppm

Minimum Data Rate (Frequency Min_{ppm}) $\geq$ -5300 ppm

Table 16 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
f_{HBR2}	Frequency for High Bit Rate 2	5.37138	5.4	5.40162	Gbps	Frequency high limit = +300ppm Frequency low limit = -5300ppm
f_{HBR}	Frequency for High Bit Rate	2.68569	2.7	2.70081	Gbps	
f_{RBR}	Frequency for Reduced Bit Rate	1.611414	1.62	1.620486	Gbps	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.14*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured data rate for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Frequency Test

Test ID

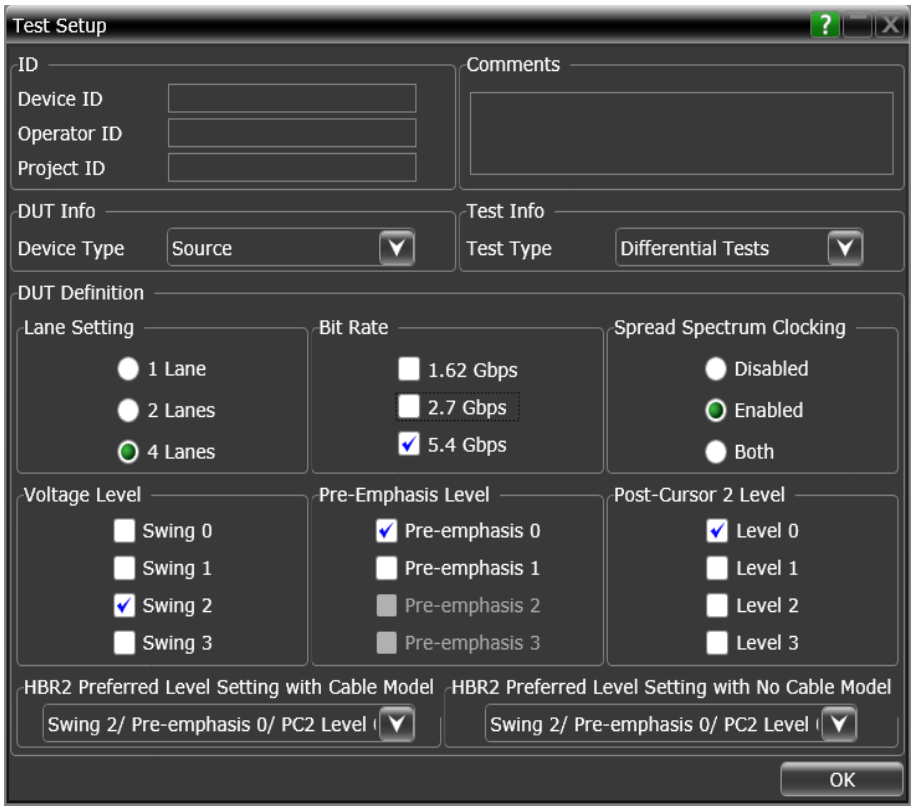
12170001 12170002 12170003 12170004 – SSC Modulation Frequency Test

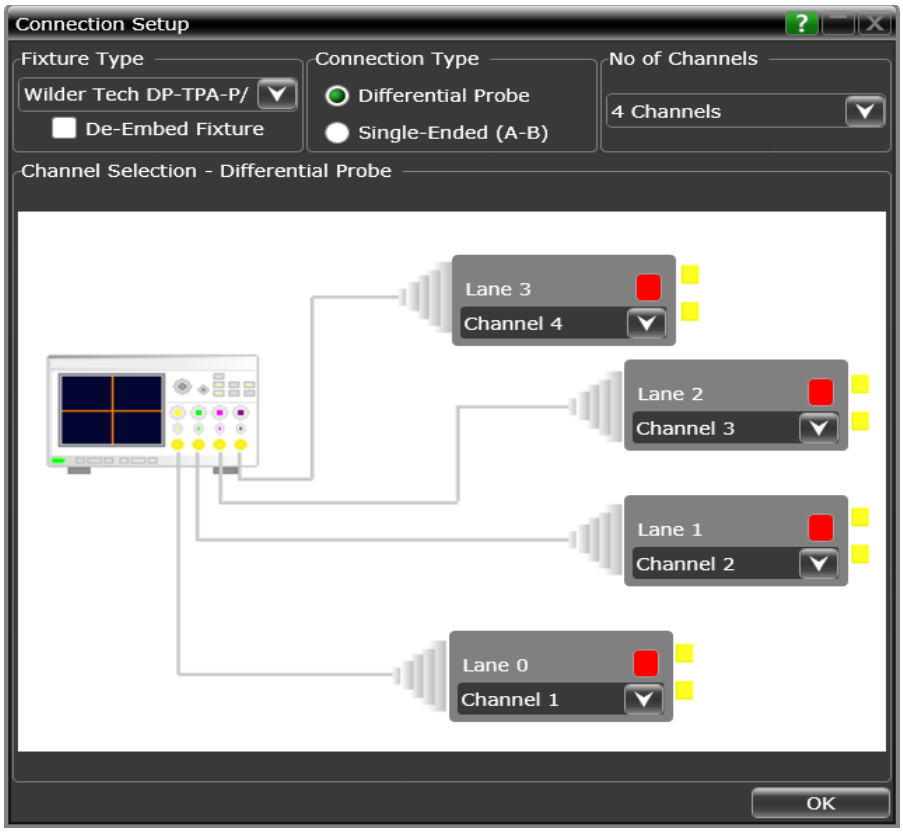
Test Overview

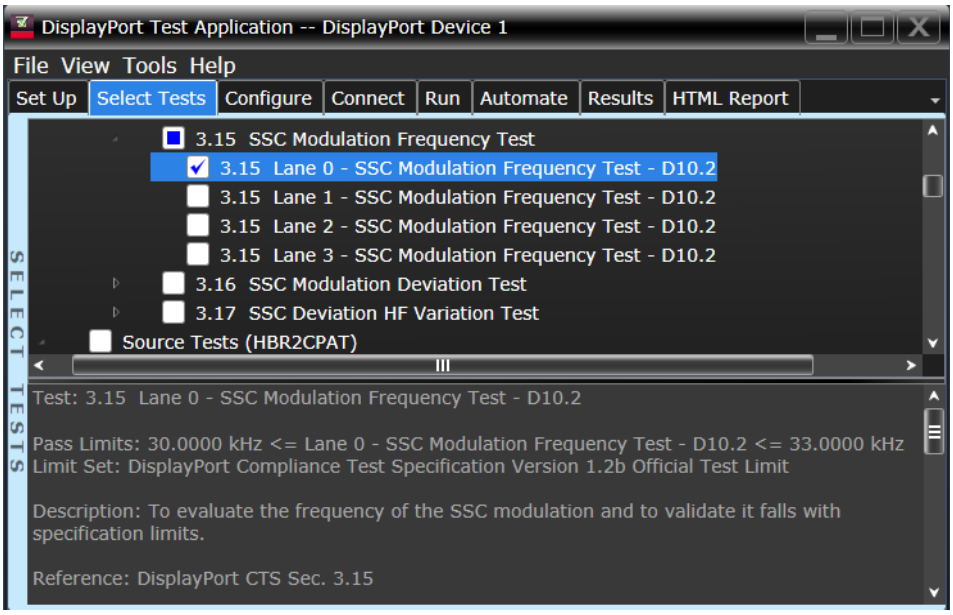
The objective of this test is to evaluate the frequency of the SSC modulation and to validate that the frequency is within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. Calculate the SSC modulation frequency from the average of the measured SSC modulation frequency for each cycle.

Test Conditions for SSC Modulation Frequency Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.

5 Set up the parameters for the frequency measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.
   g Acquire the signal for 10 SSC Cycles.
6 Get the mean value for the SSC Modulation frequency.
7 Report the measurement results.

PASS Condition

30kHz $\leq$ SSC Modulation Frequency (f_{SSC}) $\leq$ 33kHz

Table 17 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
Down_Spread_Frequency	Link clock down-spreading frequency	30	-	33	kHz	Range: 30kHz ~ 33kHz when down-spread enabled

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.15*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured SSC modulation frequency for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Deviation Test

Test ID

12180001 12180002 12180003 12180004 – SSC Modulation Deviation Test

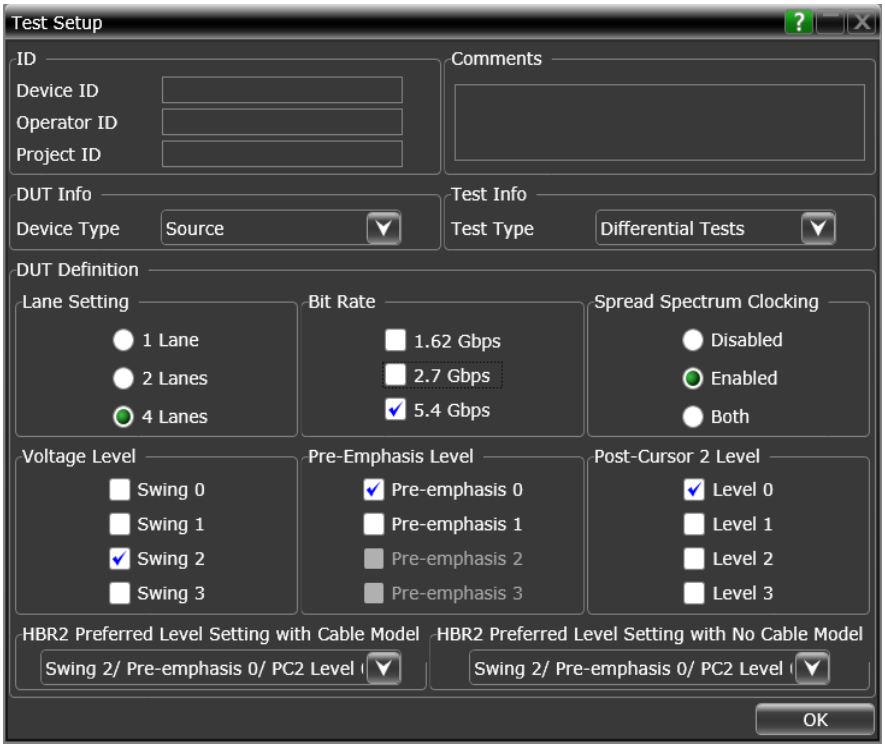
Test Overview

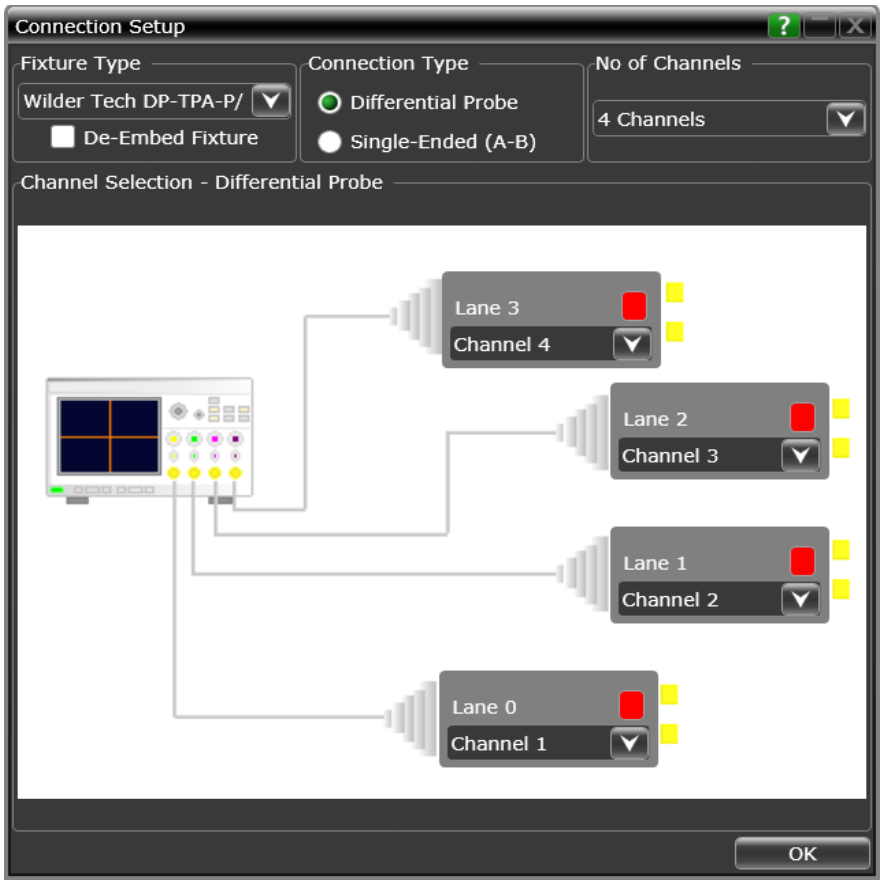
The objective of this test is to evaluate the range of SSC down-spreading of the transmitter signal in ppm and to validate that the values are within specification limits. This test includes the use of the 2^{nd} order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. For each cycle, the minimum and maximum data rate is evaluated. Calculate the SSC modulation deviation from the average of the maximum minus the average of the minimum using the equation:

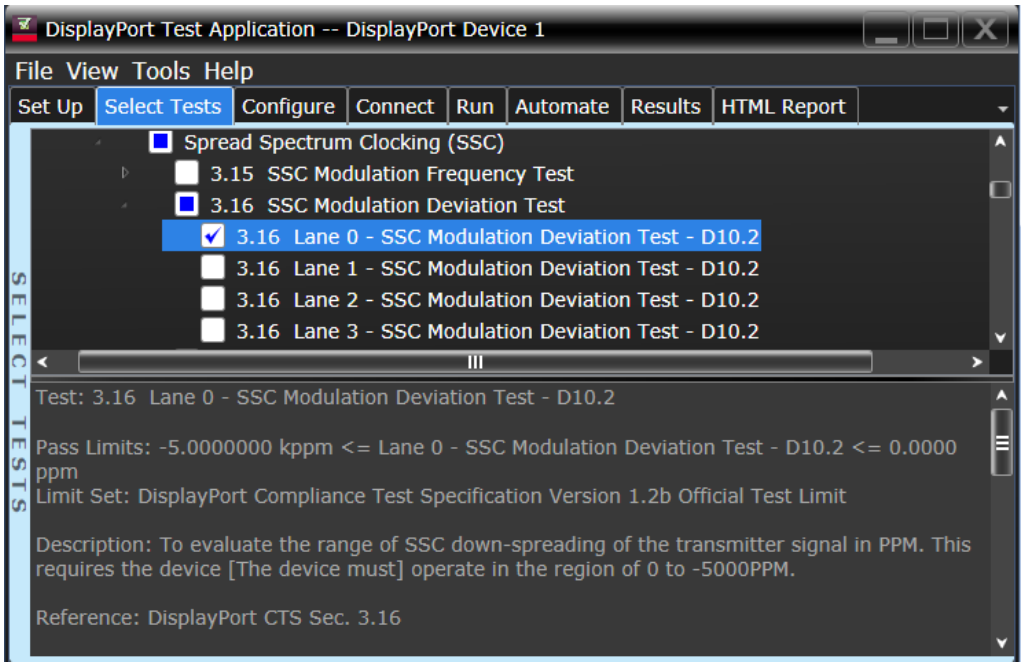
SSC Modulation Deviation = {[Average (Minimum Data Rate) - Average (Maximum Data Rate)] / Nominal Data Rate}*1E+6

Test Conditions for SSC Modulation Deviation Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.

5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and minimum measurements for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurements for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e Check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point for three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 filtered unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurements for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.
9 Set up the parameters for SSC measurement.
   a Set up memory depth and time-base to display one complete SSC Cycle based on the measured SSC modulation frequency in step 5.
   b Acquire the signal with one complete SSC Cycle.
   c Get the minimum of the FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

      Maximum Data Rate = 1/Minimum Unit Interval

   d Get the maximum of the FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

      Minimum Data Rate = 1/Maximum Unit Interval

   e Repeat steps b, c and d until you acquire 10 SSC Cycles.
   f Calculate the mean value for the maximum and minimum data rate.
10 Calculate the SSC Modulation Deviation using the equation:

   SSC Modulation Deviation = {[Average (Minimum Data Rate) - Average (Maximum Data Rate)] / Nominal Data Rate}*1E+6

11 Report the measurement results.

PASS Condition

-5000ppm $\leq$ SSC Modulation Deviation ($Resultant_{SSC\ Range}$) $\leq$ 0ppm

Table 18 DisplayPort Main Link Transmitter System Parameters

Symbol	Parameter	Min	Nom	Max	Unit	Comments
Down_Spread_Amplitude	Link clock down-spreading	0	-	0.5	%	Range: 0% ~ 0.5% when down-spread enabled

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.16*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured SSC modulation deviation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Spread Spectrum Clocking (SSC) Deviation HF Variation Test (Informative)

Test ID

12200001 12200002 12200003 12200004 – SSC Deviation HF Variation Test (Informative)

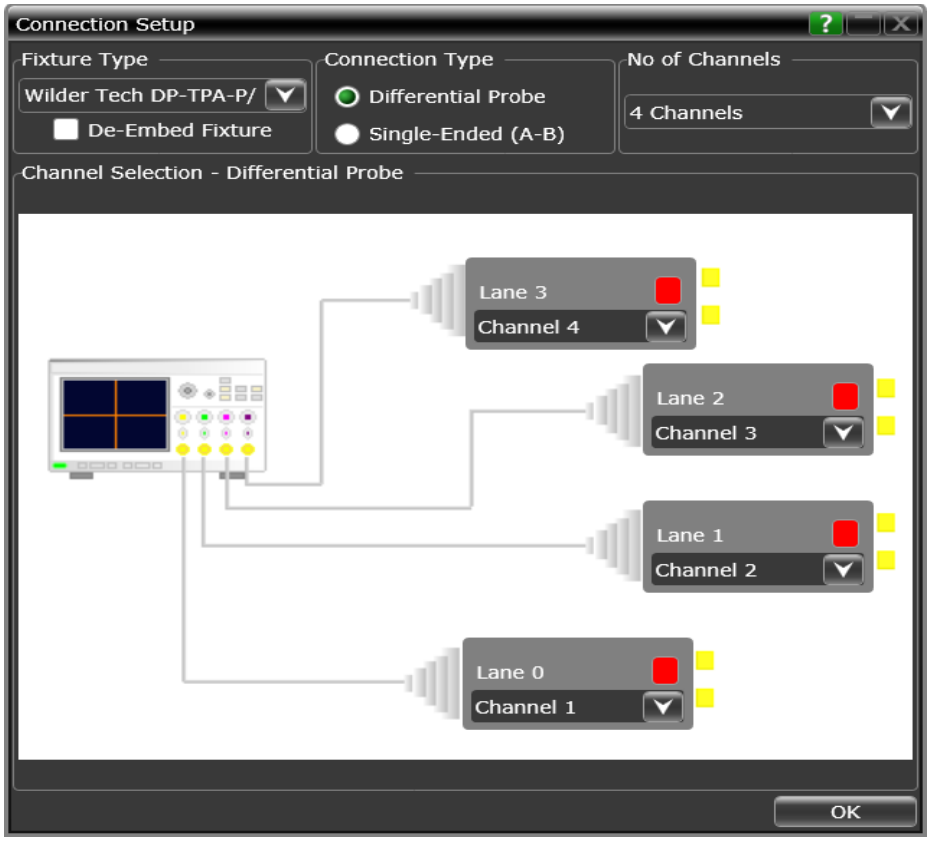
Test Overview

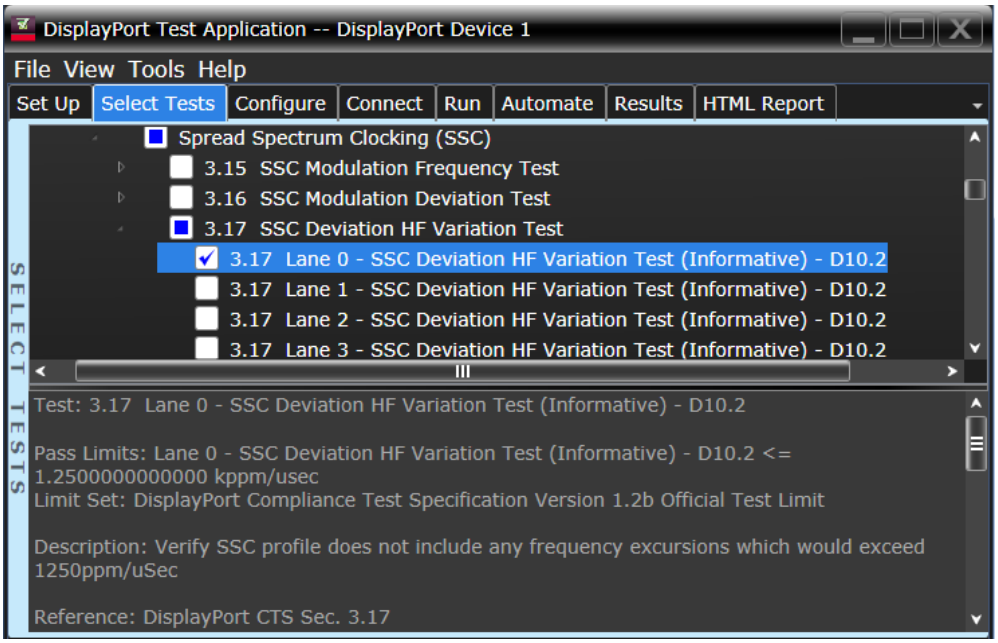
The objective of this test is to verify that the SSC profile does not include any frequency deviation that may exceed 1250 ppm/µsec. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles.

Test Conditions for SSC Deviation HF Variation Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.

5 Set up the parameters for the frequency measurement.

a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.

b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.

c Set up the memory depth and time-base using the settings defined in the Configuration Variable.

d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.

e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).

f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.

6 Set up the parameters for the SSC measurement.

a Set up memory depth and time-base to display one complete SSC cycle using the measured SSC Modulation Frequency in Step 5.

b Acquire the signal with one complete SSC Cycles.

c Read the FUNC2 filtered unit interval measurement trend.

d Compute the slope using the “Sliding Window” with 1.00 µsec window width. Calculate the slope using the equation:

$$\text{Slope} = [f(t) - f(t\text{-}1.00\ \mu\text{sec})/1.00\ \mu\text{sec}$$

e Repeat step b, c and d until you acquire 10 SSC Cycles.

f Get the maximum value for the computed value of slope.

7 Report the measurement results.

PASS Condition

SSC_t dF/dt $\leq$ 1250ppm/µsec

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.17*

Expected/Observable Results

The measured SSC deviation high frequency variation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Post-Cursor 2 Verification Test (Informative)

Test ID

1279001 1279002 1279003 1279004 — Post Cursor 2 Verification Test - Level 1/Level 0 (Informative)

1279101 1279102 1279103 1279104 — Post Cursor 2 Verification Test - Level 2/Level 1 (Informative)

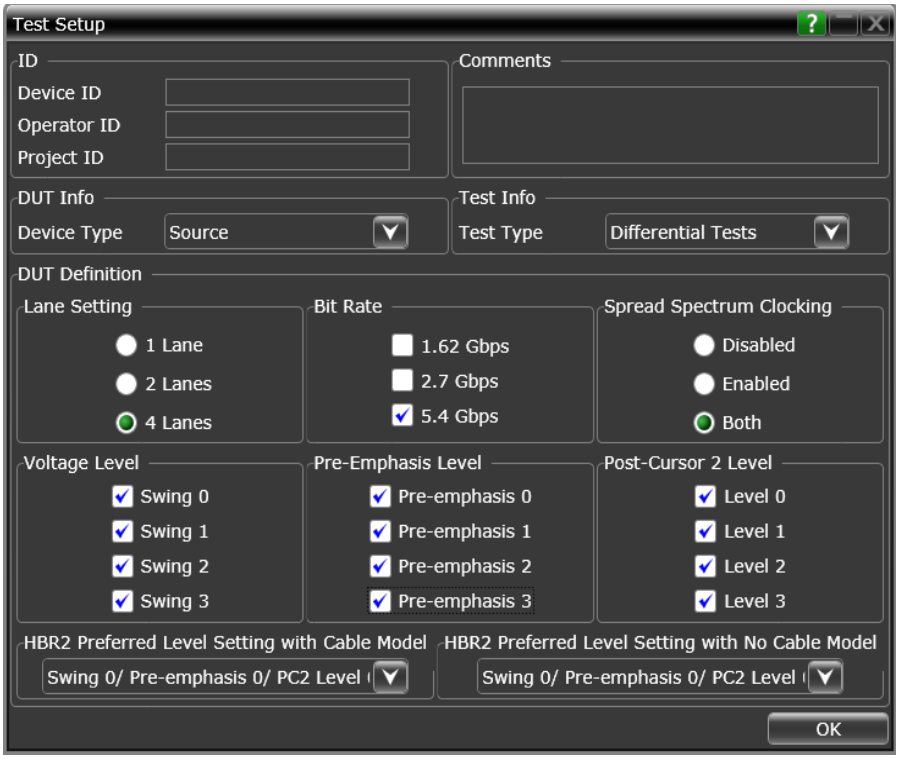
1279201 1279202 1279203 1279204 — Post Cursor 2 Verification Test - Level 3/Level 2 (Informative)

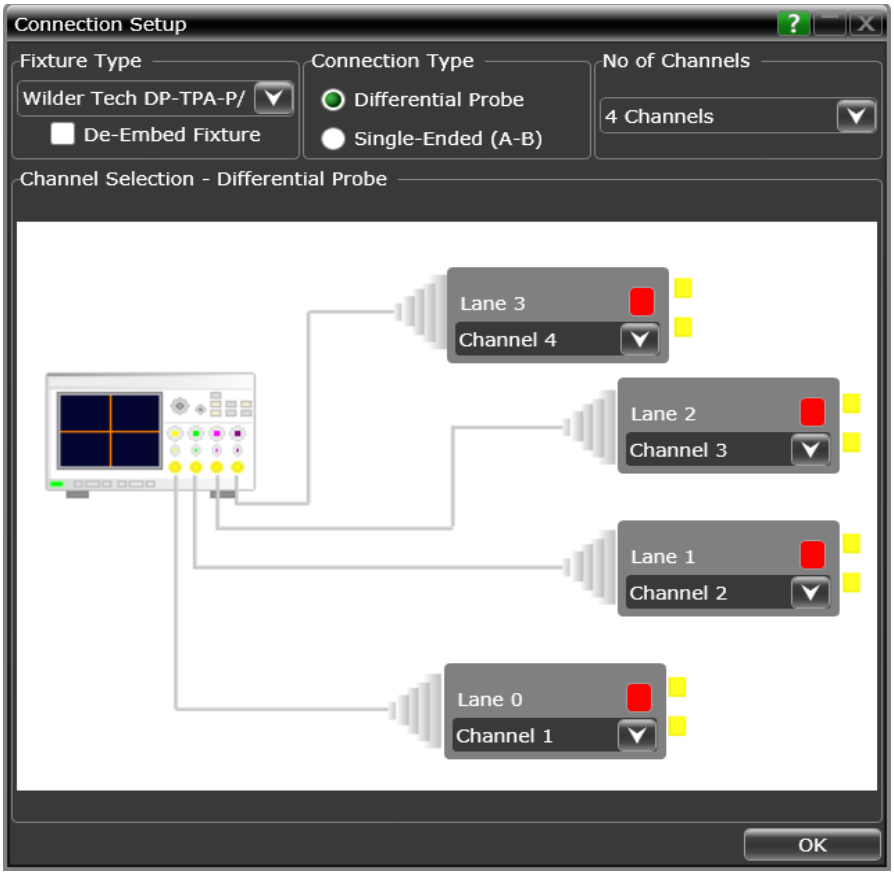
Test Overview

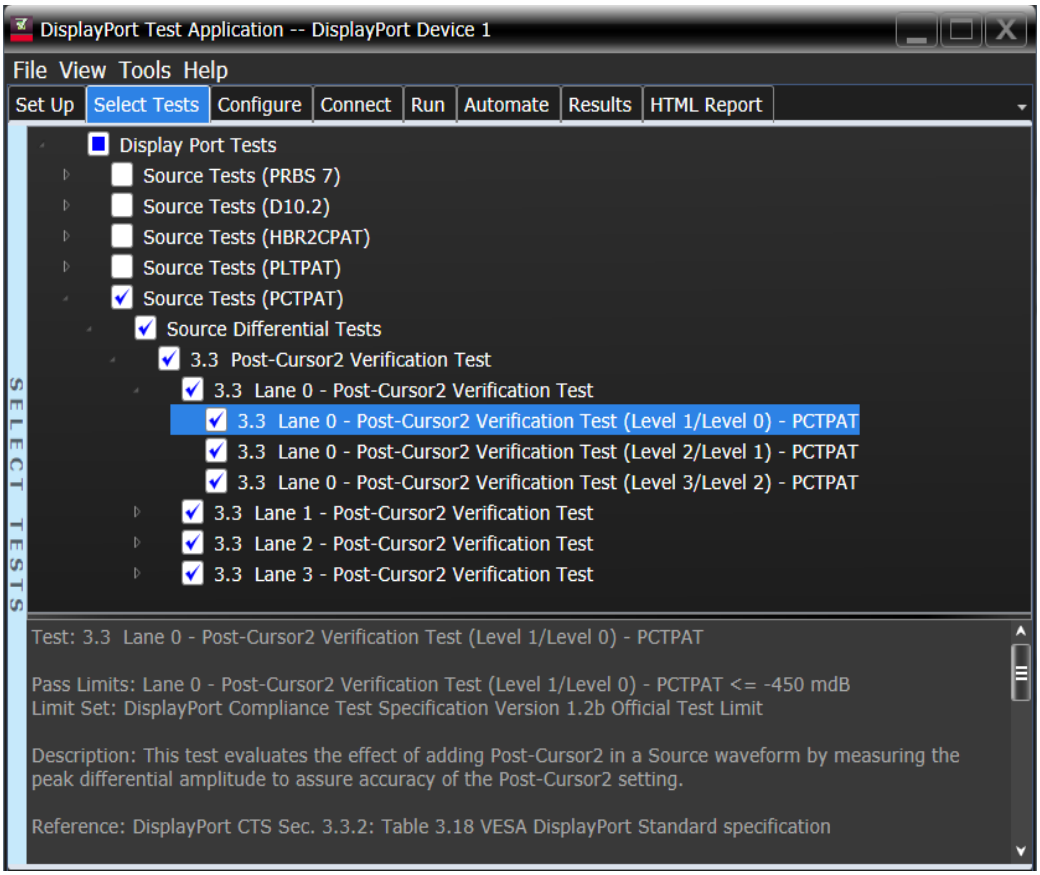
The objective of this test is to evaluate the effect of adding Post-Cursor 2 of the source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor 2 settings.

Test Conditions for Post Cursor 2 Verification Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels supported subject to constraints in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	All Post-Cursor 2 levels supported
Test Lane	All test lanes are supported
Test Pattern	PCTPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Display Port Tests
Source Tests (PRBS 7)
Source Tests (D10.2)
Source Tests (HBR2CPAT)
Source Tests (PLTPAT)
Source Tests (PCTPAT)
Source Differential Tests
3.3 Post-Cursor2 Verification Test
3.3 Lane 0 - Post-Cursor2 Verification Test
3.3 Lane 0 - Post-Cursor2 Verification Test (Level 1/Level 0) - PCTPAT
3.3 Lane 0 - Post-Cursor2 Verification Test (Level 2/Level 1) - PCTPAT
3.3 Lane 0 - Post-Cursor2 Verification Test (Level 3/Level 2) - PCTPAT
3.3 Lane 1 - Post-Cursor2 Verification Test
3.3 Lane 2 - Post-Cursor2 Verification Test
3.3 Lane 3 - Post-Cursor2 Verification Test
Test: 3.3 Lane 0 - Post-Cursor2 Verification Test (Level 1/Level 0) - PCTPAT
Pass Limits: Lane 0 - Post-Cursor2 Verification Test (Level 1/Level 0) - PCTPAT <= -450 mdB
Limit Set: DisplayPort Compliance Test Specification Version 1.2b Official Test Limit
Description: This test evaluates the effect of adding Post-Cursor2 in a Source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor2 setting.
Reference: DisplayPort CTS Sec. 3.3.2: Table 3.18 VESA DisplayPort Standard specification

Measurement Procedure

1 For a given Voltage Level, Pre-Emphasis Level and Post-Cursor 2 Level X:
   a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   b Acquire and verify the input signal:
      i Verify the trigger and the amplitude of the input signal.
      ii Scale the vertical display of the input signal to optimum value.
      iii Measure V_{TOP} and V_{BASE} of the input signal.
      iv Measure the data rate of the input signal.
   c Set up the parameter of the measurement:
      i Enable measurement of all edges to obtain a statistical value of the measurement.
      ii Set up the measurement threshold.
      iii Set up the Clock Recovery as described in the section “Clock Recovery”.
   d Pattern fold the input signal based on the qualifying pattern 00101010 for the measurement of voltage $V_{T1010\_PC2\_LvlX\_PP}$ in the test pattern PLTPAT.
   e Set up the vertical waveform histogram on the input signal at the points specified below to measure the High voltage $V_{T1010\_PC2\_LvlX\_H}$ and Low Voltage $V_{T1010\_PC2\_LvlX\_L}$.
      i $V_{T1010\_PC2\_LvlX\_H}$ is the average value over the 40% to 70% UI points in the fifth relevant bit (1s bit) in the 1010 portion of the qualifying pattern.
      ii $V_{T1010\_PC2\_LvlX\_L}$ is the average value over the 40% to 70% UI points in the sixth relevant bit (0s bit) in the 1010 portion of the qualifying pattern.
   f Calculate the peak-to-peak voltage $V_{T1010\_PC2\_LvlX\_PP}$ using the equation:

$$V_{T1010\_PC2\_LvlX\_PP} = V_{T1010\_PC2\_LvlX\_H} - V_{T1010\_PC2\_LvlX\_L}$$

   g Pattern fold the input signal based on the qualifying pattern 00011001100 for the measurement of voltage $V_{T1100\_PC2\_LvlX\_PP}$ in the test pattern PLTPAT.
   h Set up the vertical waveform histogram on the input signal at the points specified below to measure the High voltage $V_{T1100\_PC2\_LvlX\_H}$ and Low Voltage $V_{T1100\_PC2\_LvlX\_L}$.
      i $V_{T1100\_PC2\_LvlX\_H}$ is the average value over the 40% to 70% UI points in the fifth relevant bit (1s bit) in the 1100 portion of the qualifying pattern.
      ii $V_{T1100\_PC2\_LvlX\_L}$ is the average value over the 40% to 70% UI points in the sixth relevant bit (0s bit) in the 1100 portion of the qualifying pattern.
   i Calculate the peak-to-peak voltage $V_{T1100\_PC2\_LvlX\_PP}$ using the equation:

$$V_{T1100\_PC2\_LvlX\_PP} = V_{T1100\_PC2\_LvlX\_H} - V_{T1100\_PC2\_LvlX\_L}$$

   j Calculate the Post-Cursor 2 ratio using the equation:

$$\text{Post-Cursor 2 Ratio}_{LvlX} = V_{T1100\_PC2\_LvlX\_PP} / V_{T1010\_PC2\_LvlX\_PP}$$

2 Compare the pre-emphasis delta of Post-Cursor 2 Level with the limits by repeating Step 1 with another Post-Cursor2 Level.
3 Calculate the pre-emphasis delta of Post-Cursor 2 Level using the equation:

$$\text{Post-Cursor 2 Delta (Level 1 vs Level 0)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl1} / \text{Post-Cursor 2 Ratio}_{Lvl0}]$$

$$\text{Post-Cursor 2 Delta (Level 2 vs Level 1)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl2} / \text{Post-Cursor 2 Ratio}_{Lvl1}]$$

$$\text{Post-Cursor 2 Delta (Level 3 vs Level 2)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl3} / \text{Post-Cursor 2 Ratio}_{Lvl2}]$$

4 Report the measurement results.

PASS Condition

Post Cursor 2 Verification Measurements

For Level 1 vs. Level 0 Pre-emphasis Post Cursor 2 settings: $Resultant_{Lvl0\_to\_Lvl1} \leq -0.45$ dB

For Level 2 vs. Level 1 Pre-emphasis Post Cursor 2 settings: $Resultant_{Lvl1\_to\_Lvl2} \leq -0.5$ dB

For Level 3 vs. Level 2 Pre-emphasis Post Cursor 2 settings: $Resultant_{Lvl2\_to\_Lvl3} \leq -0.6$ dB

Table 19 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX-PREEMP\_POST2-DELTA}$	Delta of Pre-emphasis Post Cursor2 Level 1 vs. Level 0	-0.45	-	-	dB	Measured on 2nd T_{BIT} at Pre-emphasis Level 0
	Delta of Pre-emphasis Post Cursor2 Level 2 vs. Level 1	-0.5	-	-	dB	Support for Pre-emphasis Post Cursor2 is optional
	Delta of Pre-emphasis Post Cursor2 Level 3 vs. Level 2	-0.6	-	-	dB	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2a, Section 3.3.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured pre-emphasis delta of Post-Cursor 2 for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Eye Diagram Test (TP3_EQ)

Test ID

For HBR:

- 1211001, 1211002, 1211003, 1211004 – Eye Diagram Test (TP3_EQ) - PRBS7
- 1211011, 1211012, 1211013, 1211014 – Eye Diagram Test with No Cable Model (TP3_EQ) - PRBS7

For HBR2:

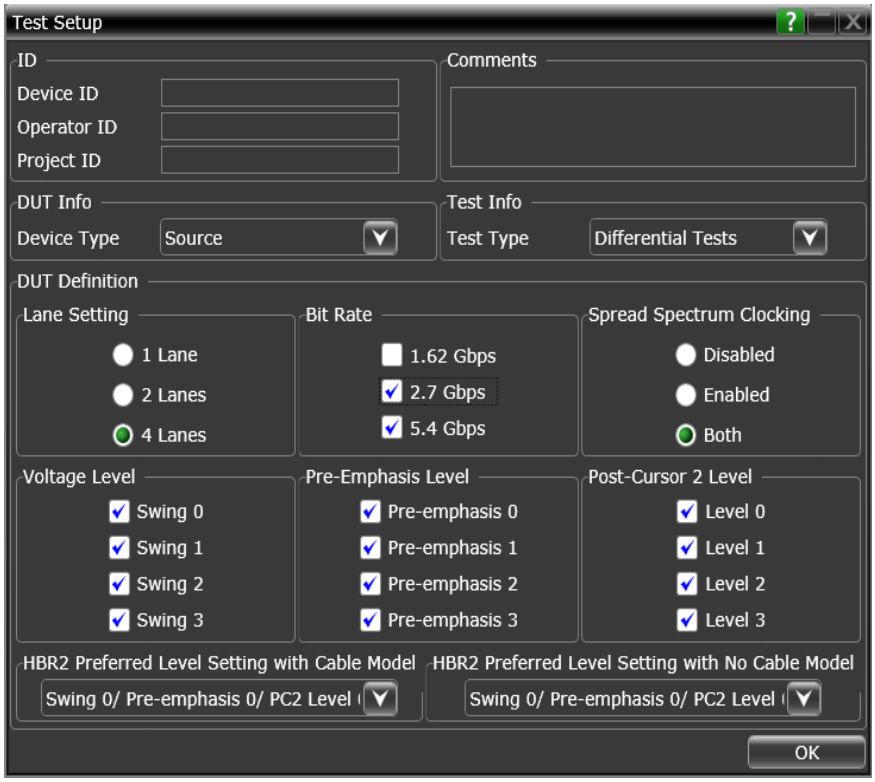
- 1215001, 1215002, 1215003, 1215004 – Eye Diagram Test (TP3_EQ) - HBR2CPAT
- 1215011, 1215012, 1215013, 1215014 – Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT

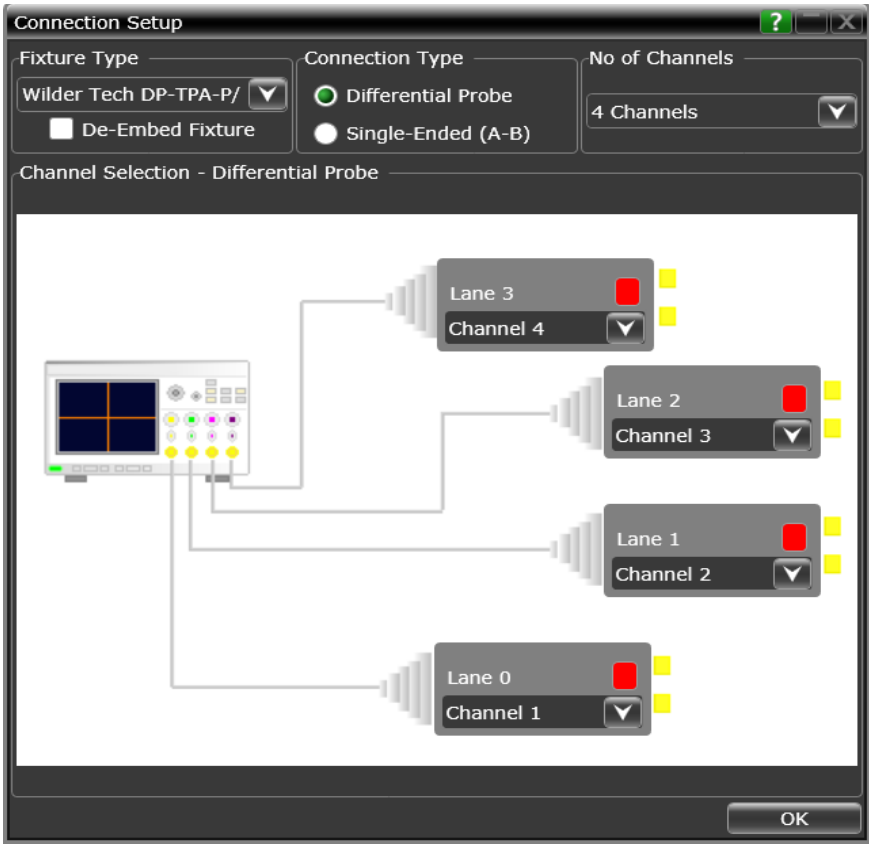
Test Overview

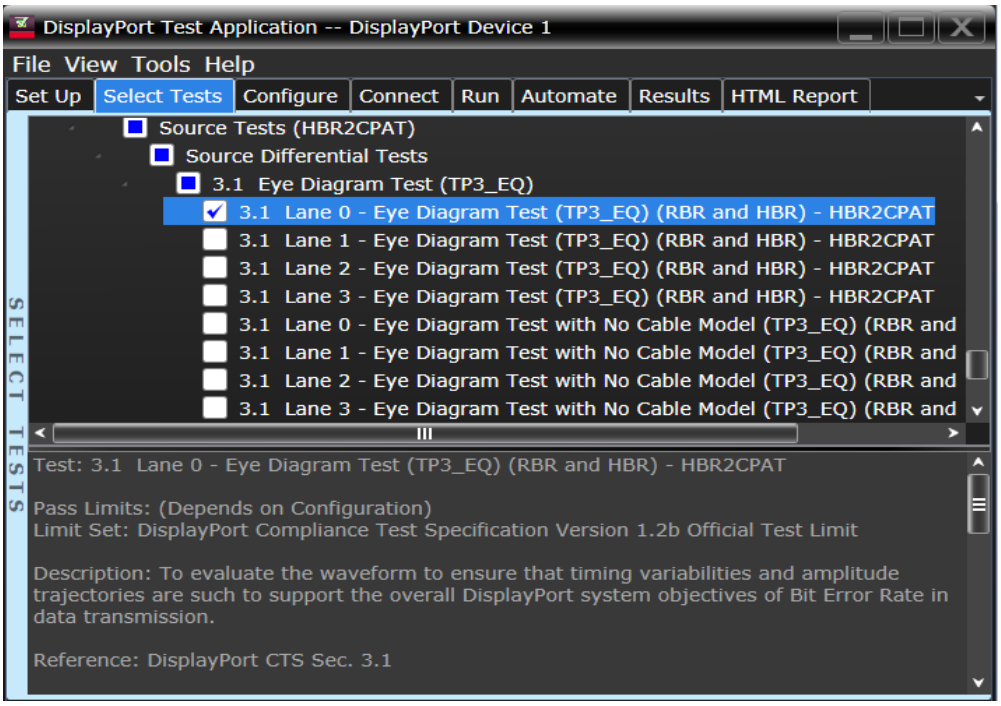
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions for Eye Diagram Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR (Informative) and HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	HBR – Level 2 HBR2 – Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	HBR – Level 0 HBR2 – Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	HBR – Level 0 HBR2 – Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes are supported
Test Pattern	HBR–PRBS7 HBR2–HBR2CPAT
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure for HBR

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.

7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the jitter of the eye diagram using the Histogram.
9 Check for any signal trajectories that may have entered into the mask.
10 Report the measurement results.

Measurement Procedure for HBR2

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]:
   a Pattern fold the equalized signal based on the High Level Voltage (V_{HIGH}) random noise configuration variable.
   b Set up the vertical waveform histogram on the equalized signal to measure random noise of High Level Voltage (V_{HIGH}).
   c Measure the High Level Voltage (V_{HIGH}) random noise based on the standard deviation of the waveform histogram.
   d Pattern fold the equalized signal based on the Low Level Voltage (V_{LOW}) random noise configuration variable.
   e Set up the vertical waveform histogram on the equalized signal to measure the random noise of Low Level Voltage (V_{LOW}).
   f Measure the Low Level Voltage (V_{LOW}) random noise based on the standard deviation of the waveform histogram.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge and right edge.
8 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.

9 Find the maximum eye height location of the eye diagram.

10 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:

a Set up the parameter of the jitter separation using the EZJIT Plus/Complete Software.

i Load the jitter separation parameter into EZJIT Plus/Complete Software based on the settings in the Configuration Variable.

ii Acquire the signal until 1,000,000 edges are analyzed.

b Note the value of the jitter component from the EZJIT Plus/Complete Software.

11 Create the eye mask based on the following criteria:

a If you select more than one lane (2 lanes or 4 lanes DUT configuration), the eye mask height and width is derate in the following manner, to include crosstalk as defined in DisplayPort 1.2b Compliance Test Specification:

i Eye Mask Width Derate (Crosstalk) = 0.04 UI

ii Eye Mask Height Derate (Crosstalk) = 0.014V

b If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]: eye mask height and width is derate as below to comprehend the noise/jitter extrapolated to BER 10^{-9} for an Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI:

i Calculate the Eye Mask Width Derate (Random Jitter) using the equation:

$$\text{Eye Mask Width Derate (Random Jitter)} = 2.5 * \text{Random Jitter}_{rms}$$

ii Calculate the Eye Mask Height Derate (Random Noise) using the equation:

$$V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{HIGH}\ \text{Random Noise}_{rms}$$

$$V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{LOW}\ \text{Random Noise}_{rms}$$

NOTE The factor 2.5 is the delta between BER 10^{-6} (9.507) and 10^{-9} (11.996) to comprehend the noise/jitter extrapolated to BER 10-9 as the Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI.

BER	N
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996

c Place the eye mask height at the point of the maximum eye height found in Step 9.

d Calculate the Eye Mask Width:

$$\text{Eye Mask Width} = \text{Eye Width Specification (0.38 UI)} + \text{Eye Mask Width Derate (Crosstalk)} + 2 * \text{Eye Mask Width Derate (Random Jitter)}$$

e Calculate the Eye Mask Height:

$$V_{HIGH}\ \text{Eye Mask Height} = \{\text{Eye Height Specification (0.09 V)} + \text{Eye Mask Height Derate (Crosstalk)}\}/2 + V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)}$$

$$V_{LOW}\ \text{Eye Mask Height} = -\{\text{Eye Height Specification (0.09 V)} + \text{Eye Mask Height Derate (Crosstalk)}\}/2 - V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)}$$

12 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram.
   c Run the eye mask until 1,000,000 UI are folded.
13 Measure the eye height of the eye diagram using the Histogram.
14 Measure the jitter of the eye diagram using the Histogram.
15 Calculate the eye width based on the measured jitter of the eye diagram.
16 Check for any signal trajectories that may have entered into the mask.
17 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 20 and Table 21 show the voltage and time coordinates for the mask used for the eye diagram.

Table 20 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

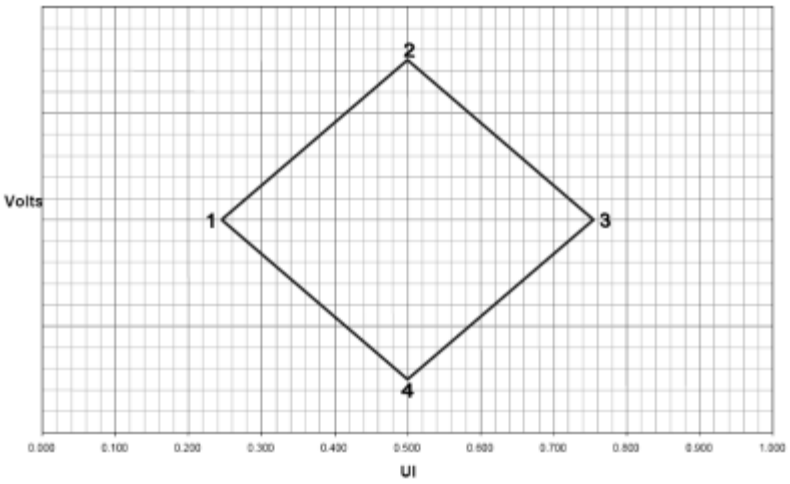


Figure 22 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 21 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.045*
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.045*

NOTE

*Eye height limit of 45 mV and -45 mV assumes cross-talk as 0, which is only possible in case of single lane testing.

In case of multi-lane testing, cross talk exists, and the eye height values deviate by ± 7 mV. Thus the eye height becomes (+45 +7) mV and (-45 -7) mV or +52 mV and -52 mV.

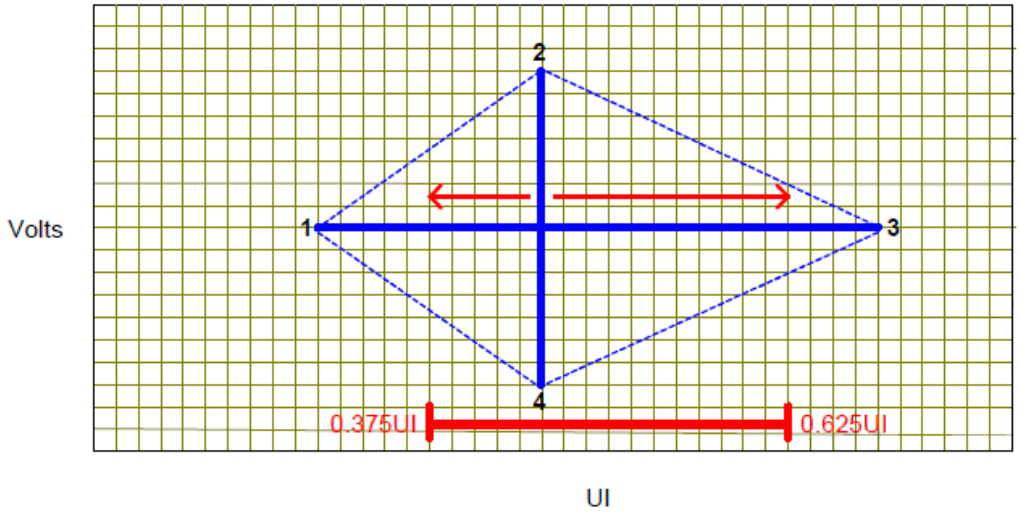


Figure 23 The Sink Eye Mask at TP3_EQ (HBR2)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test (TP3_EQ)

Test ID

For HBR2:

- 1222001, 1222002, 1222003, 1222004 – Total Jitter Test (TP3_EQ) - HBR2CPAT
- 1222011, 1222012, 1222013, 1222014 – Total Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1221001, 1221002, 1221003, 1221004 – Total Jitter Test (TP3_EQ) - D10.2
- 1221011, 1221012, 1221013, 1221014 – Total Jitter Test with No Cable Model (TP3_EQ) - D10.2

Test Overview

The objective of this test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

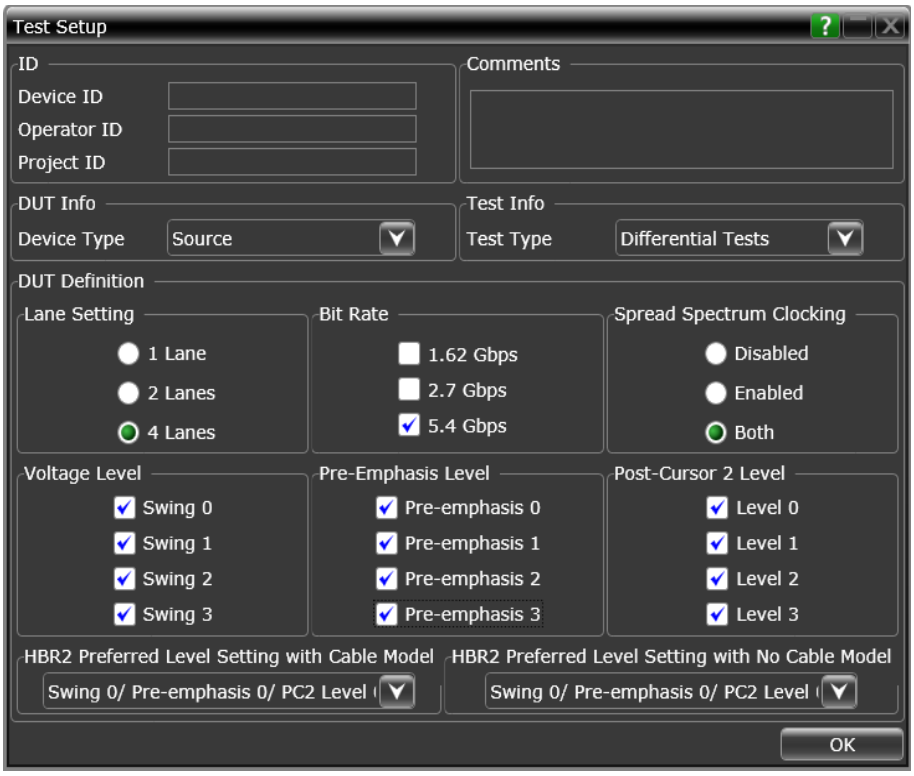
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

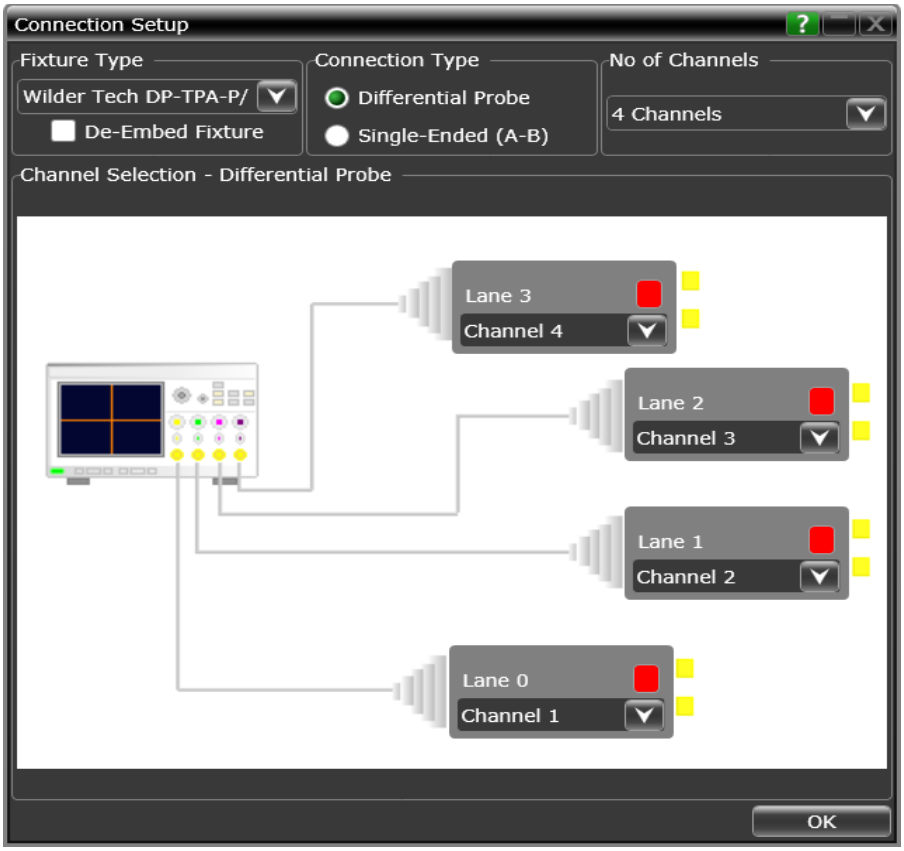
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

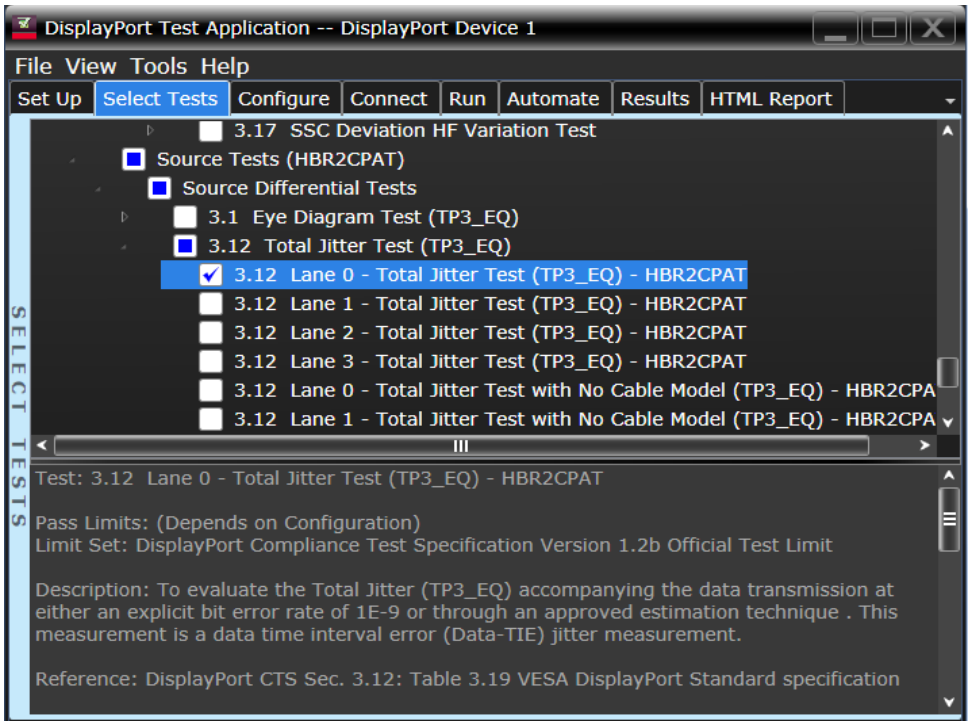
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes are supported
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Total Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Total Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.

7 Report the measurement results.

PASS Condition

Table 22 Total Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.580 UI*

* The limits for the Total Jitter are derated by 0.04 UI from 0.62 UI in DisplayPort 1.2a Standard.

Table 23 Total Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.40 UI

UI is Unit Interval.

Test References

See:

For HBR2CPAT

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

For D10.2

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18*

Expected/Observable Results

The measured total jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Deterministic Jitter Test (TP3_EQ)

Test ID

- 1236001, 1236002, 1236003, 1236004 — Deterministic Jitter Test (TP3_EQ) - HBR2CPAT
- 1236011, 1236012, 1236013, 1236014 — Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1235001, 1235002, 1235003, 1235004 — Deterministic Jitter Test (TP3_EQ) - D10.2
- 1235011, 1235012, 1235013, 1235014 — Deterministic Jitter Test with No Cable Model (TP3_EQ) - D10.2

Test Overview

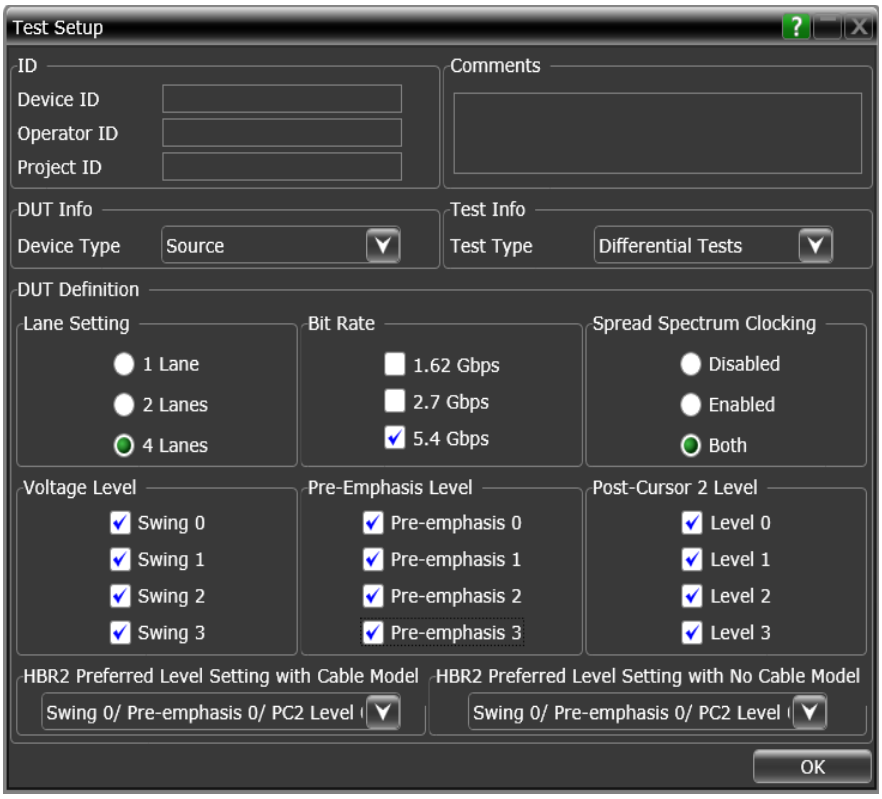
The objective of this test is to evaluate the deterministic jitter accompanying the data transmission. The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

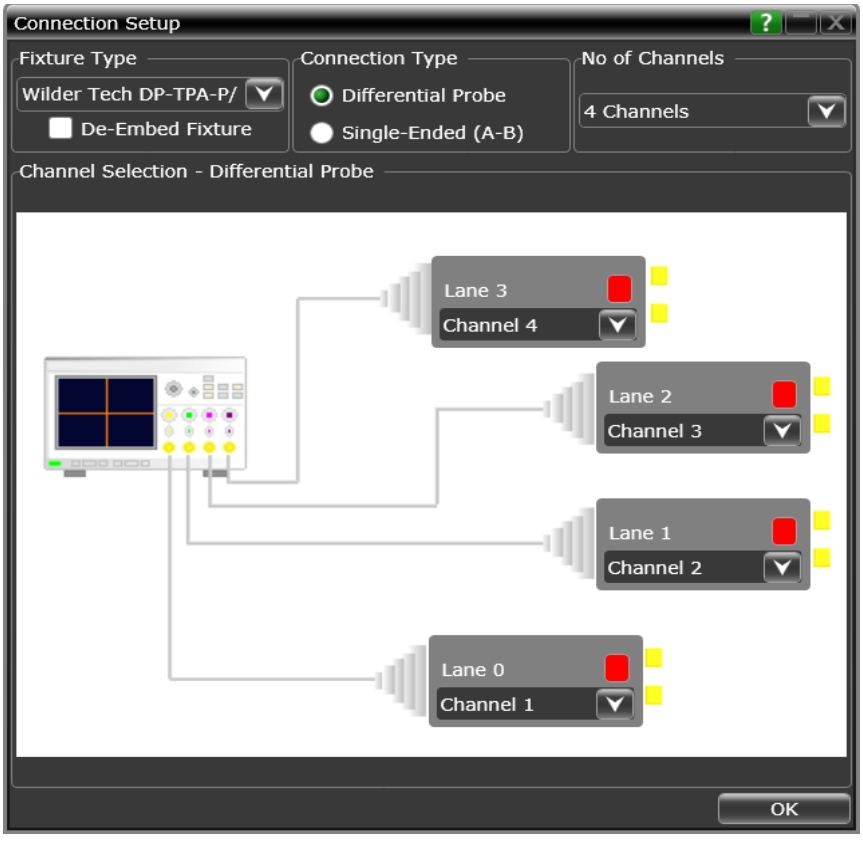
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

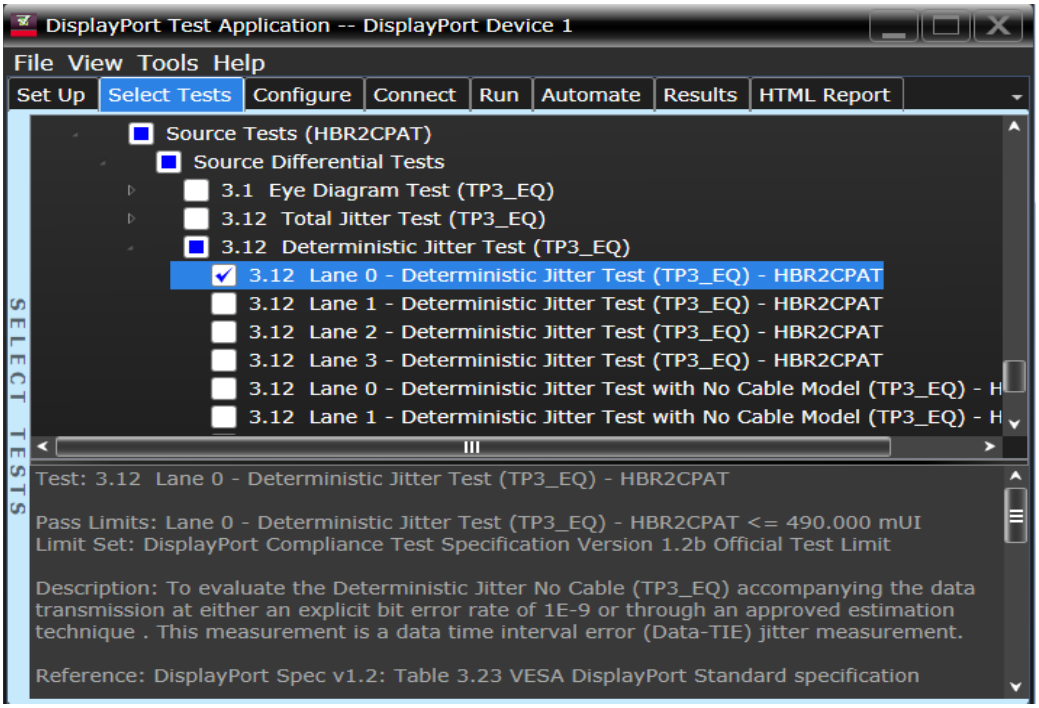
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Deterministic Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes are supported
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Deterministic Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Deterministic Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 24 Deterministic Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.49 UI

Table 25 Deterministic Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.25 UI

UI is Unit Interval.

Test References

See:

For HBR2CPAT

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

For D10.2

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18*

Expected/Observable Results

The measured deterministic jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Random Jitter Test (TP3_EQ)

Test ID

- 1238001, 1238002, 1238003, 1238004 — Random Jitter Test (TP3_EQ) - D10.2
- 1238011, 1238012, 1238013, 1238014 — Random Jitter Test with No Cable Model (TP3_EQ) - D10.2

Test Overview

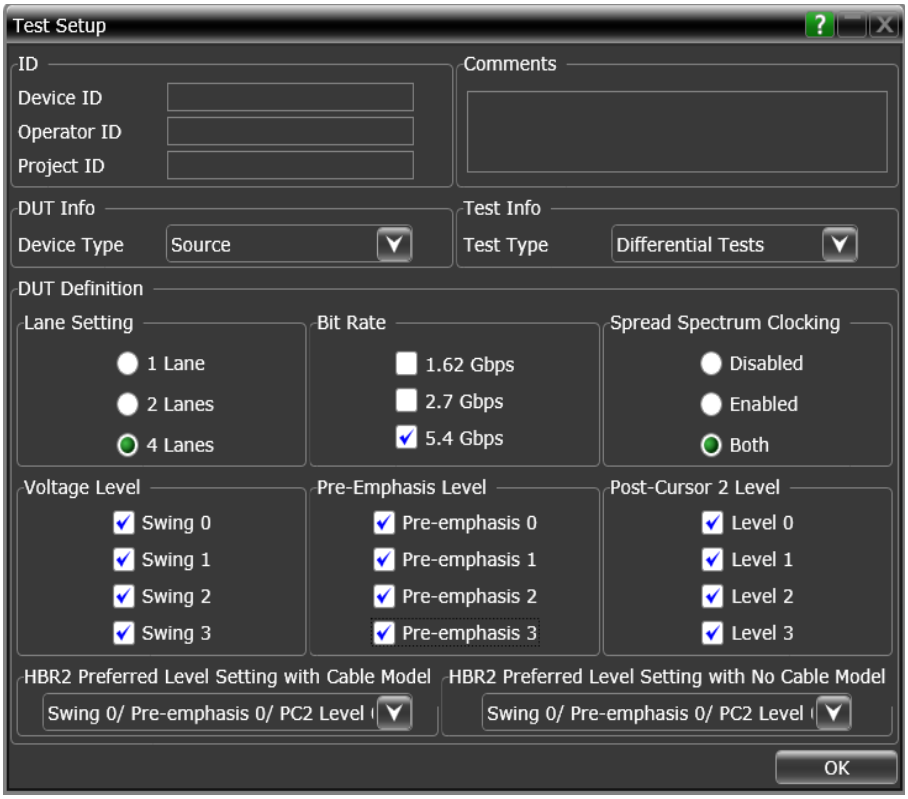
The objective of this test is to evaluate the random jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. The jitter is separated into each jitter components and the random jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

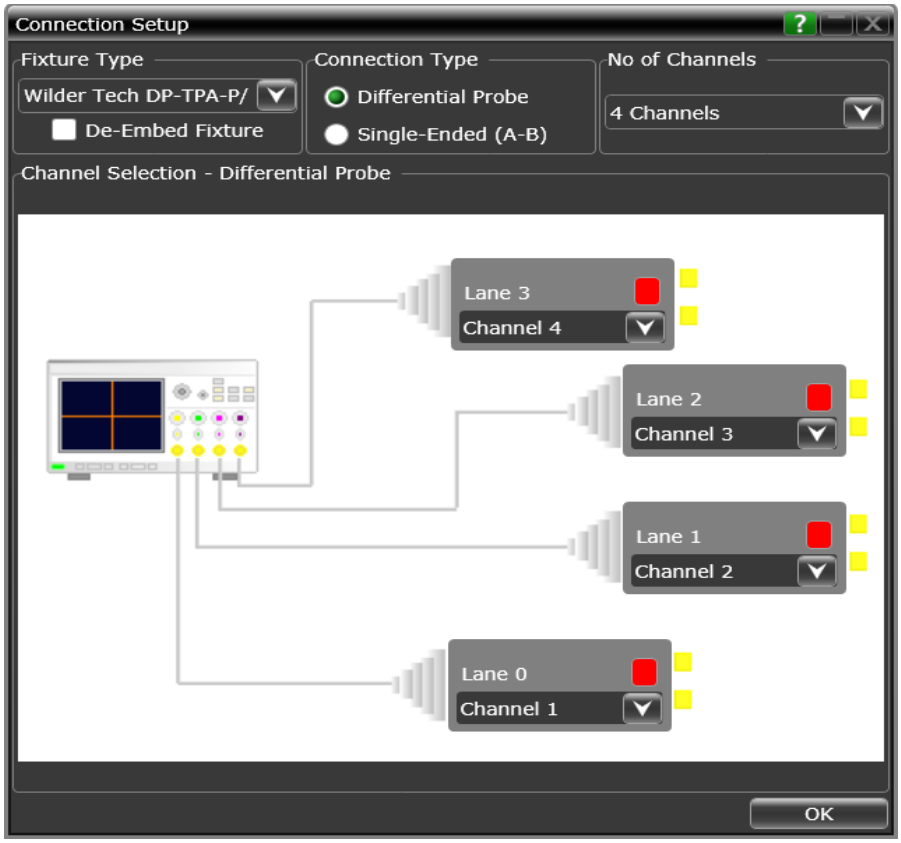
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

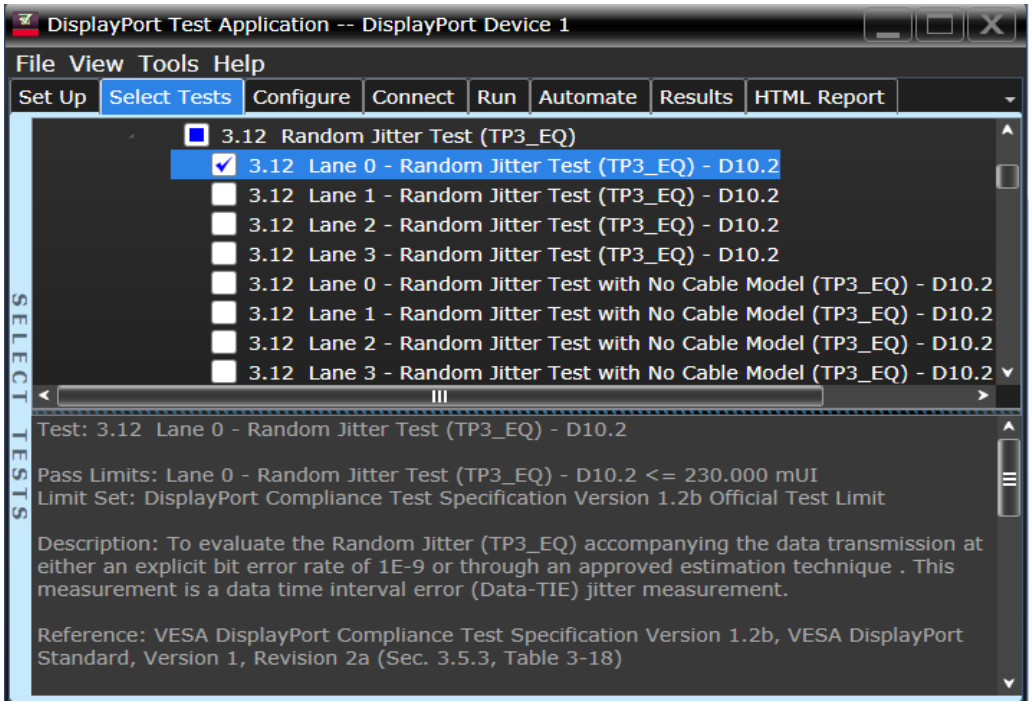
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Random Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes are supported
Test Pattern	D10.2
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Random Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Random Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 26 Random Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.23 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18*

Expected/Observable Results

The measured random jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source AC Common Mode Test (Informative)

Test ID

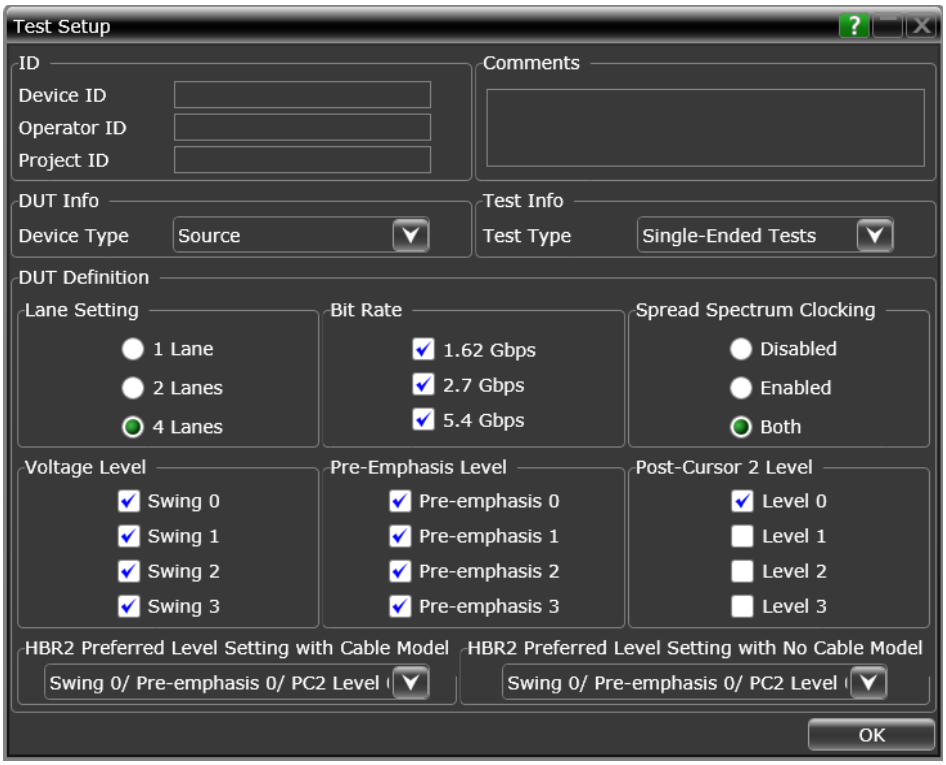
12110001, 12110002, 12110003, 12110004 – AC Common Mode Test (Informative)

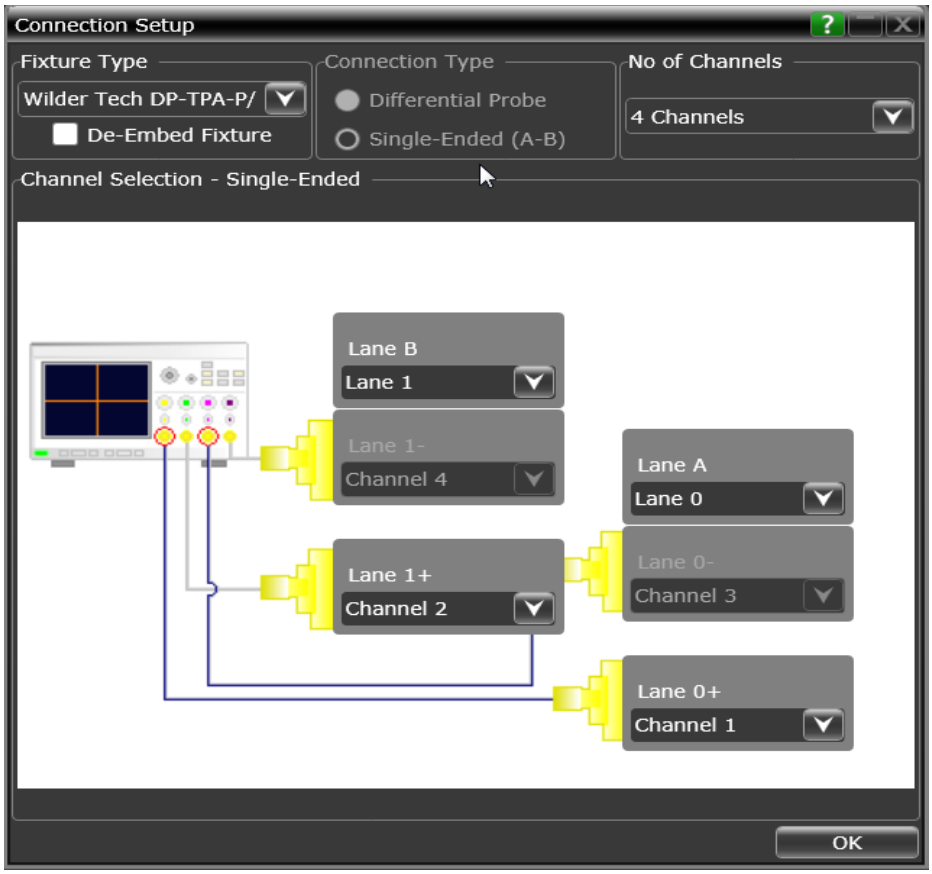
Test Overview

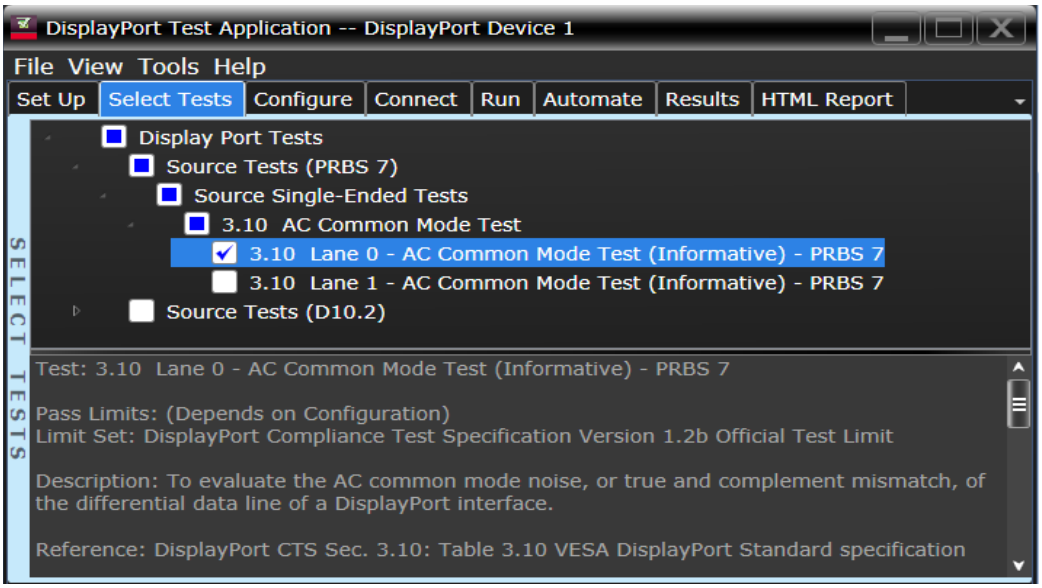
The objective of this test is to evaluate the AC Common Mode noise (unfiltered rms) of the differential data line of the DP interface.

Test Conditions for AC Common Mode Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis level supported subject to the constraints in Table 3-1 of the VESA DisplayPort 1.2a Standard
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Single-Ended Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Create FUNC3 signal, which is the common mode signal of the input single-ended signal.
4 If the filter is enabled [“Filter” configuration variable set to “High Pass Filter”, “Low Pass Filter” or “None” (Default)]:
   a Create FUNC4 signal, which is the filtered FUNC3 signal by applying the High Pass filter or Low Pass filter on the FUNC3 signal based on the Configuration Variable.
5 Set up two display grids such that one grid displays the input single-ended signal while the other grid displays the common mode signal.
6 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
7 Set up the parameters for RMS voltage measurement of the common mode signal.
   a Set up the V_{rms} measurement for the common mode signal.
   b Acquire the signal until 100,000 edges are measured.
8 Get the mean for the V_{rms} measurement.
9 Report the measurement results.

PASS Condition

For RBR and HBR:

AC Common Mode Voltage $\leq$ 20mV

For HBR2:

AC Common Mode Voltage $\leq$ 30mV

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.10*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 9.2, Table 9-6*

Expected/Observable Results

The measured AC common mode noise for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Intra-Pair Skew Test (Informative)

Test ID

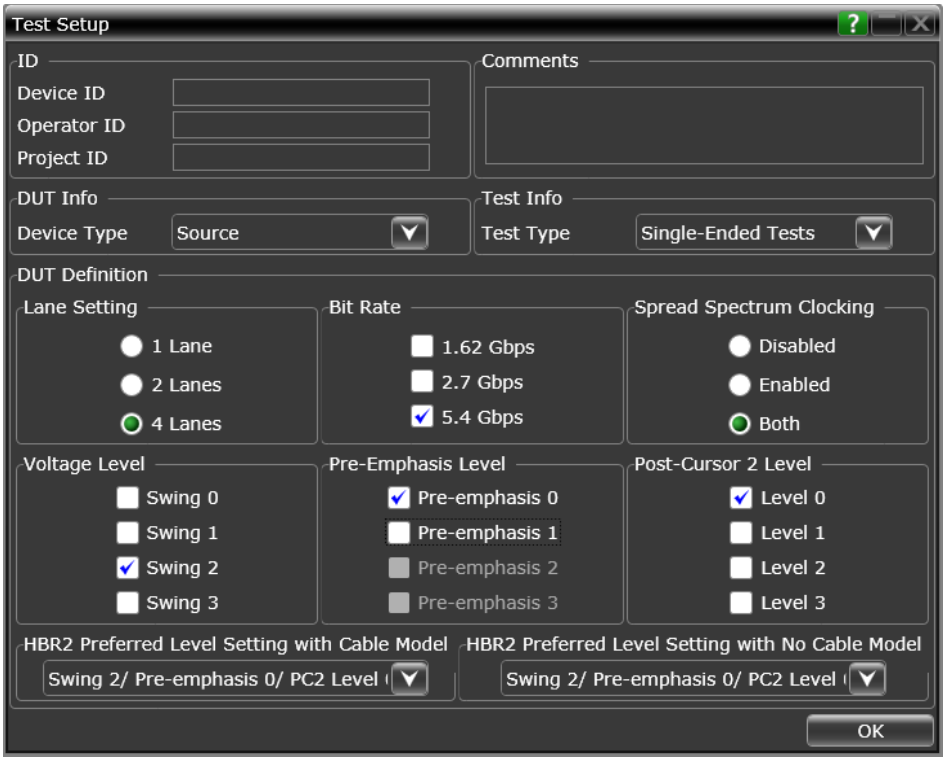
12100001, 12100002, 12100003, 12100004 — Intra-Pair Skew Test (Informative)

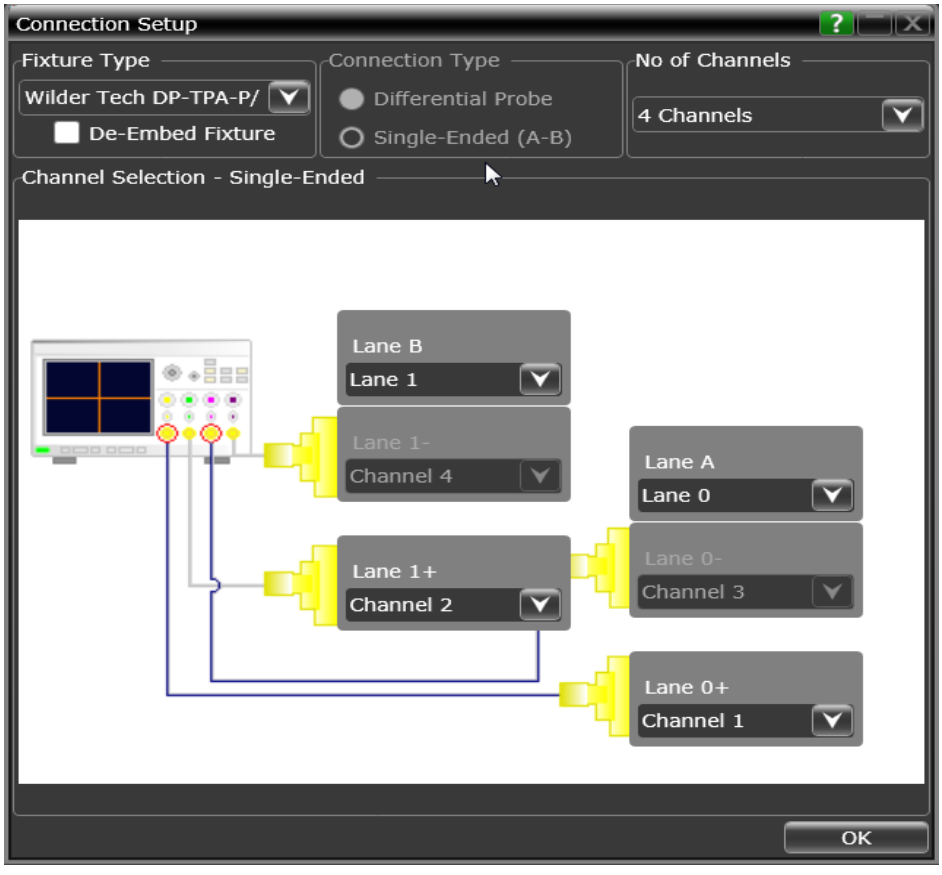
Test Overview

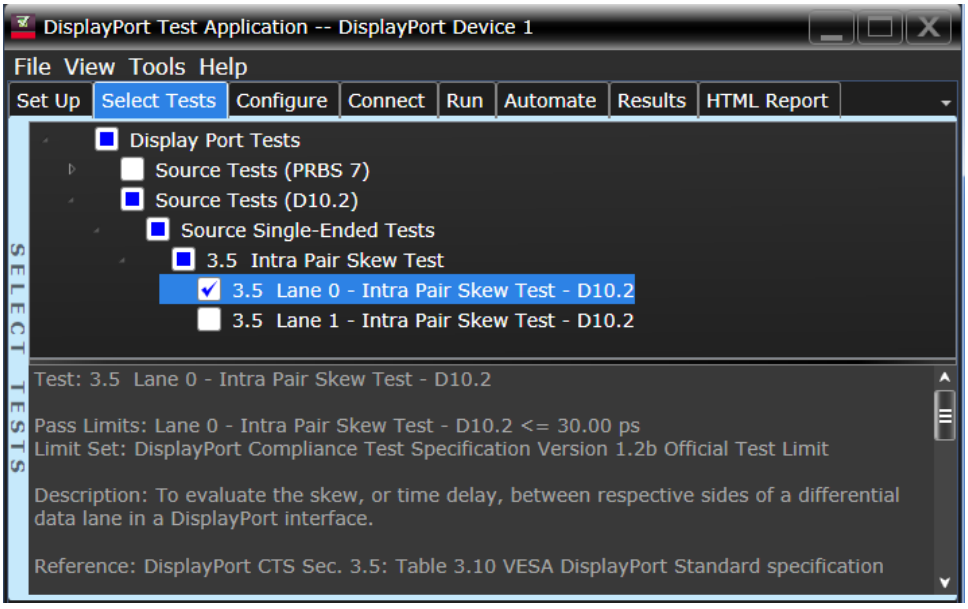
The objective of this test is to evaluate the skew or time delay between respective sides of a differential data lane in the DP interface.

Test Conditions for Intra-Pair Skew Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported For one lane operation: Lane 0+ to Lane 0- For two lane operation: Lane 0+ to Lane 0- Lane 1+ to Lane 1- For four lane operation: Lane 0+ to Lane 0- Lane 1+ to Lane 1- Lane 2+ to Lane 2- Lane 3+ to Lane 3-
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Single-Ended Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
4 Set up the parameters to perform High Level Voltage (V_{HIGH}) and Low Level Voltage (V_{LOW}) for each input single-ended signal.
   a Scale the vertical display of the input single-ended signal to optimum value.
   b Acquire the signal for 100 waveforms.
   c Find VHIGH by measuring the average voltage at 0.06 UI to 0.75 UI of the High Level.
   d Find VLOW by measuring the average voltage at 0.06 UI to 0.75 UI of the Low Level.
   e Calculate the Transition Voltage (V_{Trans}) using the equation:

$$V_{Trans} = (V_{HIGH} + V_{LOW}) / 2$$

5 Set up the parameters for the intra-pair skew measurement:

a Set up the measurement threshold for each single-ended data signal based on the measured Transition Voltage.

b Set up InfiniiScan to trigger on the desired pattern.

c Set up delta time measurement to measure time difference between the rising edge of the data true signal (D+) and the complement's (D-) falling edge:

$$D+_{Transition\_High} - D-_{Transition\_Low}$$

d Set up delta time measurement to measure time difference between the falling edge of the data true signal (D+) and the complement's (D-) rising edge:

$$D+_{Transition\_Low} - D-_{Transition\_High}$$

e Acquire the signal until you measure 100 edges.

f Calculate the intra-pair skew using the equation:

$$\text{Intra-Pair Skew} = \{1/\text{Number of Edges}\}$$

$$\sum \{[(D+_{Transition\_High} - D-_{Transition\_Low}) + (D+_{Transition\_Low} - D-_{Transition\_High})] / 2\}$$

6 Report the measurement results.

PASS Condition

Intra Pair Skew ≤ 30 ps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.5*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured intra-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the "Test References" section for this test.

4 DisplayPort 1.2b Sink Tests

Overview

Test Point Definition for DisplayPort 1.2 (1.2b) Sink Tests

NOTE Sink Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Sink DUT at Test Point 3 (TP3) as shown in Figure 24. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

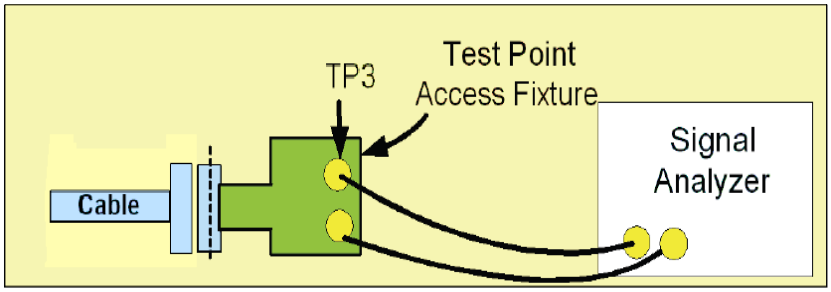


Figure 24 Test Point 3 Connection for DisplayPort 1.2 Sink Tests

Table 27 defines the test point fixtures and instruments used for DisplayPort 1.2 (1.2b) Sink Tests:

Table 27 Test Point Fixtures and Instruments for DisplayPort 1.2 Sink Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Calibration of Stress Signal

For the calibration of the stress signal, you must test the stress signal in the manner shown in the Figure 25 for RBR and Figure 26 for HBR and HBR2.

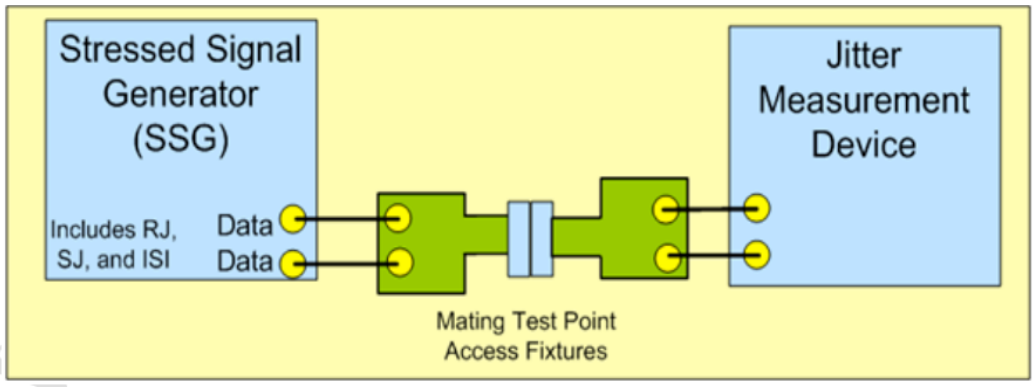


Figure 25 Test Point 3 Connection for Stress Signal Calibration of RBR

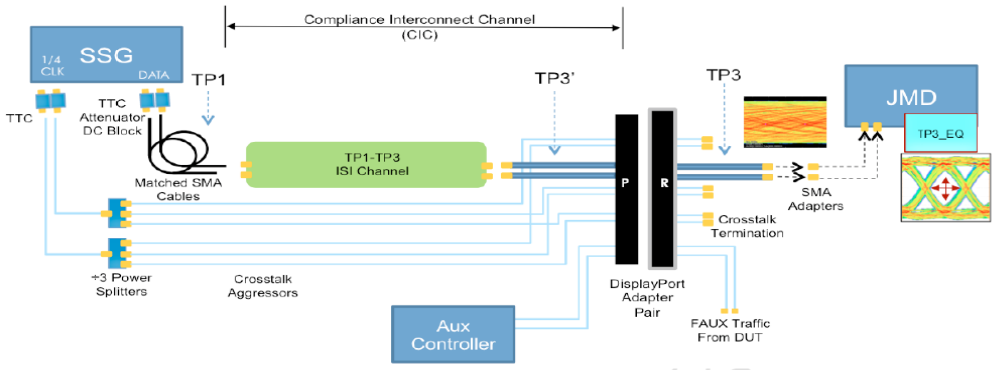


Figure 26 Test Point 3 Connection for Stress Signal Calibration of HBR and HBR2

Table 28 defines the Test Point 3 Connections for Stress Signal Calibration:

Table 28 Test Point Connections for Stress Signal Calibration

Test Requirement	Device Used
Stress Signal Generator (SSG)	Bit Error Rate Tester ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Jitter Measurement Device (JMD)	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Sink Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort 1.2b Standards, the option **1.2b** appears by default in the **Test Specification** drop-down options.

5 The option **Physical Layer Tests** appears by default in the **Test Selection** area.

6 Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.

7 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

8 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

9 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

10 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

11 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

12 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

13 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

14 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DisplayPort 1.2 Sink Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

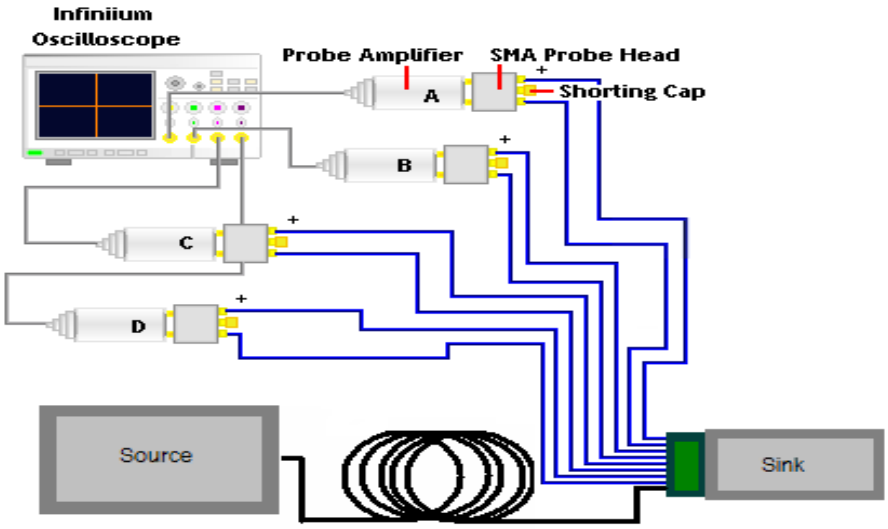


Figure 27 Sample connection diagram for DisplayPort 1.2 Sink Tests

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Sink tests to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1. In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.
2. On the **Test Setup** window,
   a. Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.
   b. In the **DUT Info** area, select the **Device Type** as **Sink**.
   c. In the **Test Info** area, the **Test Type** options are grayed out.
   d. In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.
3. Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1. Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.
2. On the **Connection Setup** window,
   a. Select the appropriate option in the **Fixture Type** to indicate where the DUT is connected to.
   b. Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.
   c. In the **Channel Selection** area, assign appropriate channels to lanes.
3. Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of sink tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Sink Tests" on page 186 to complete the task flow for DUT setup along with configuring the Compliance Application to run each test.

Sink Eye Diagram Test

Test ID

12140001, 12140002, 12140003, 12140004 – Sink Eye Diagram Test

Test Overview

The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

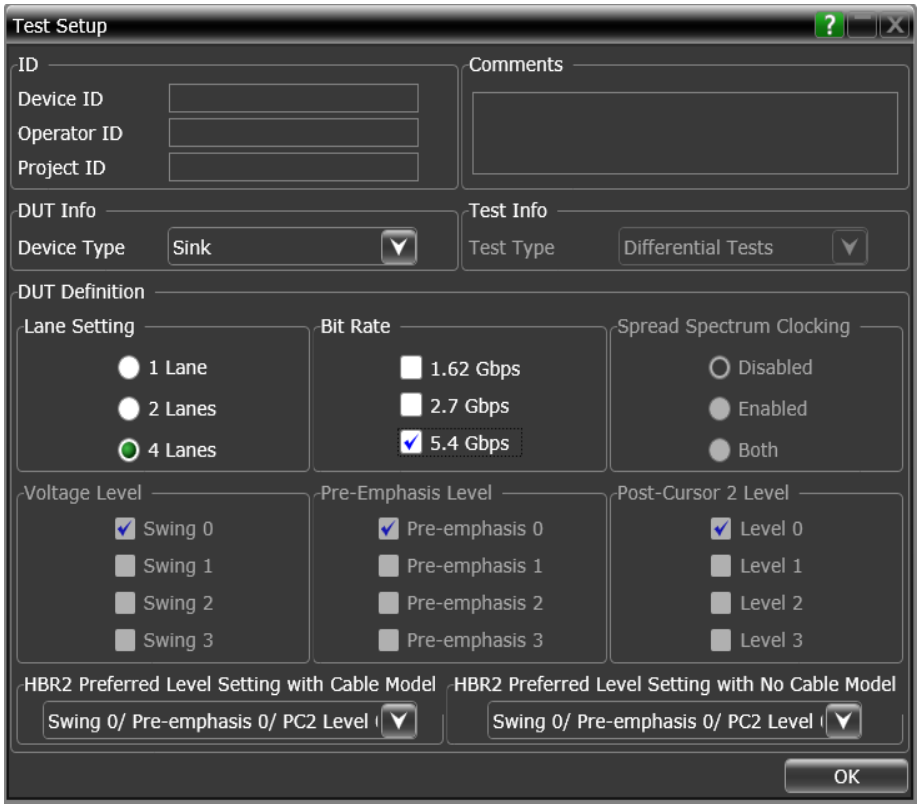
You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the following specifications for degradation:

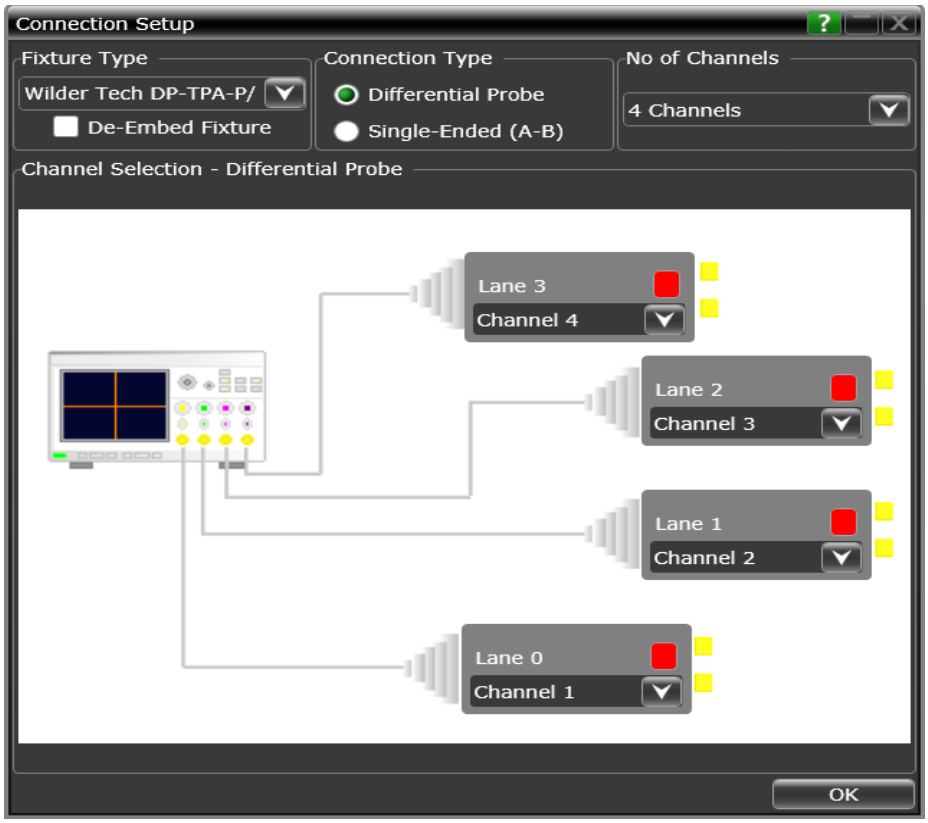
- Voltage Level:
  - 90mV peak to peak +/- 10% for HBR2 at TP3_EQ (Table 3-18, DP1.2a)
  - 150mV peak to peak +/- 10% for HBR at TP3_EQ (Table 3-25, DP1.2a)
  - 46mV peak to peak +/- 10% for RBR at TP3 (Table 3-26, DP1.2a)

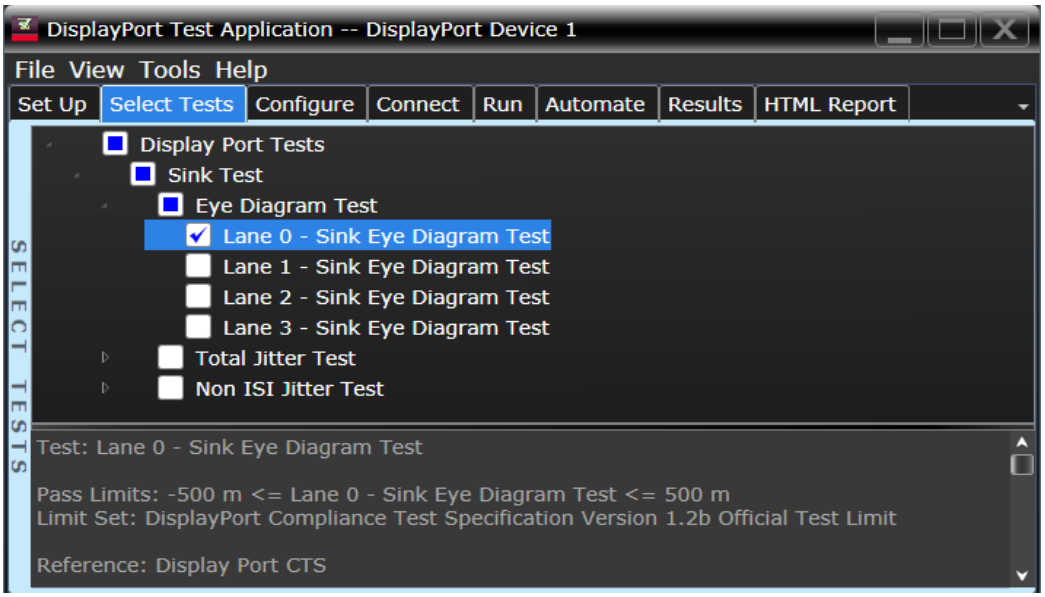
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR and HBR2)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	RBR, HBR–PRBS7 HBR2–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer).
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
9 Measure the jitter of the eye diagram using the Histogram.
10 Check for any signal trajectories that may have entered into the mask.

11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 29 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 29 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

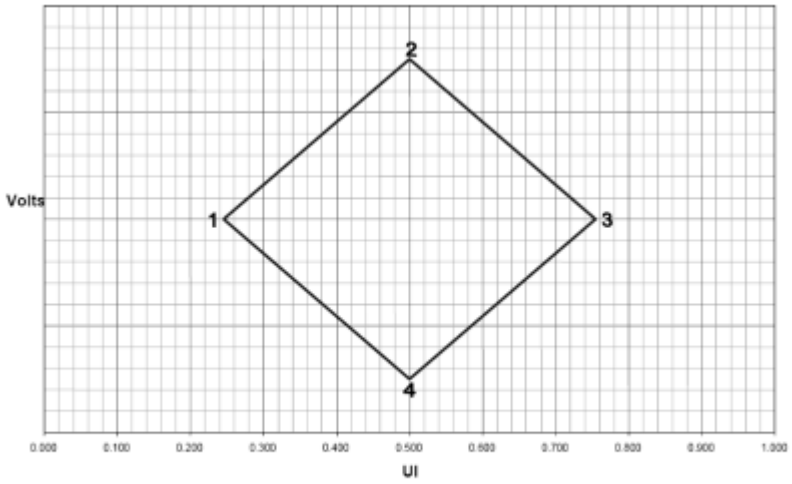


Figure 28 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 30 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.045*
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.045*

NOTE

*Eye height limit of 45 mV and -45 mV assumes cross-talk as 0, which is only possible in case of single lane testing.

In case of multi-lane testing, cross talk exists, and the eye height values deviate by ± 7 mV. Thus the eye height becomes (+45 +7) mV and (-45 -7) mV or +52 mV and -52 mV.

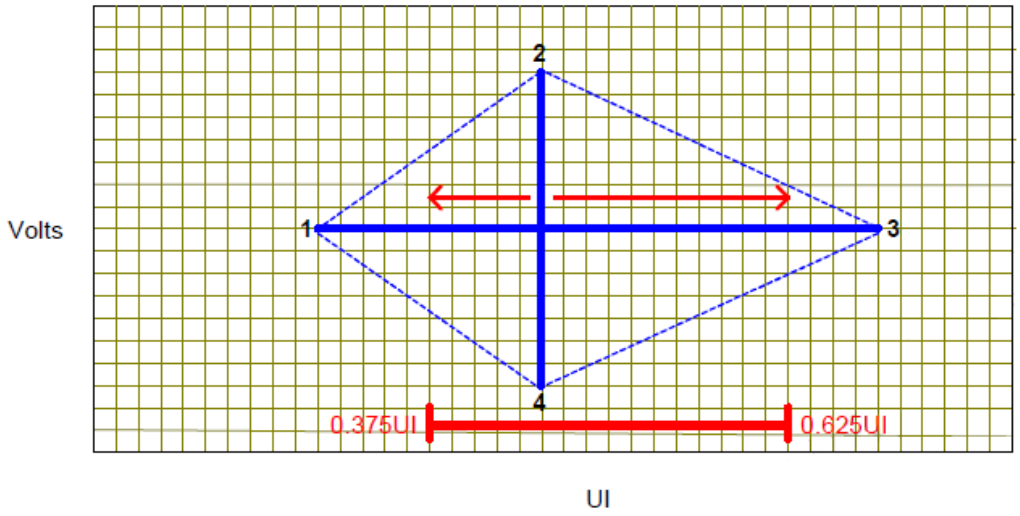


Figure 29 The Sink Eye Mask at TP3_EQ (HBR2)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Sink Total Jitter Test

Test ID

12210001, 12210002, 12210003, 12210004 – Sink Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

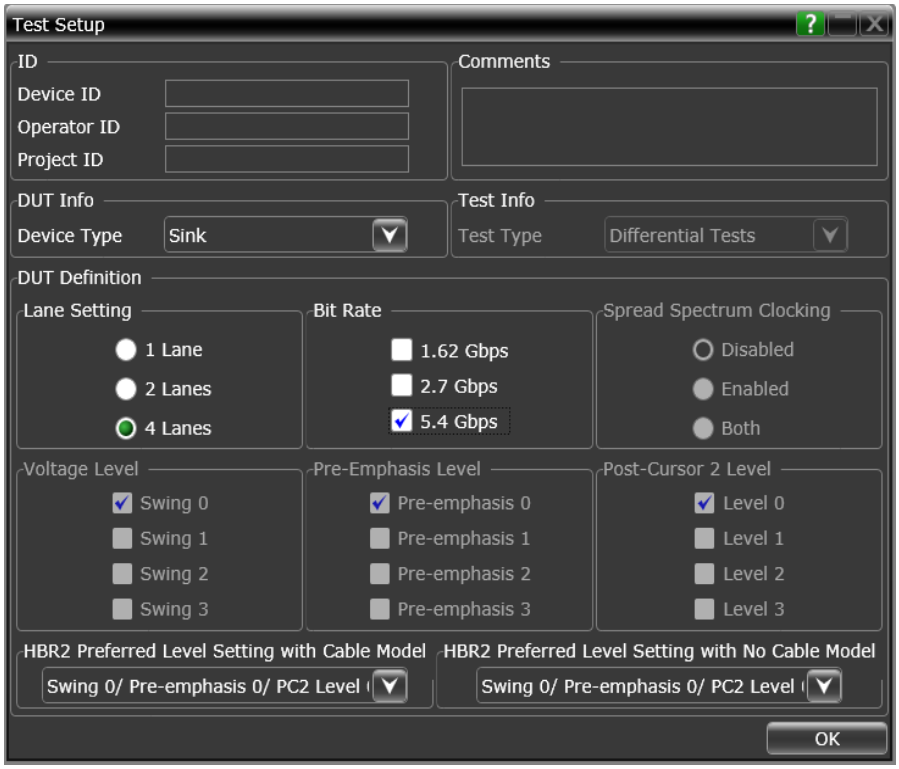
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

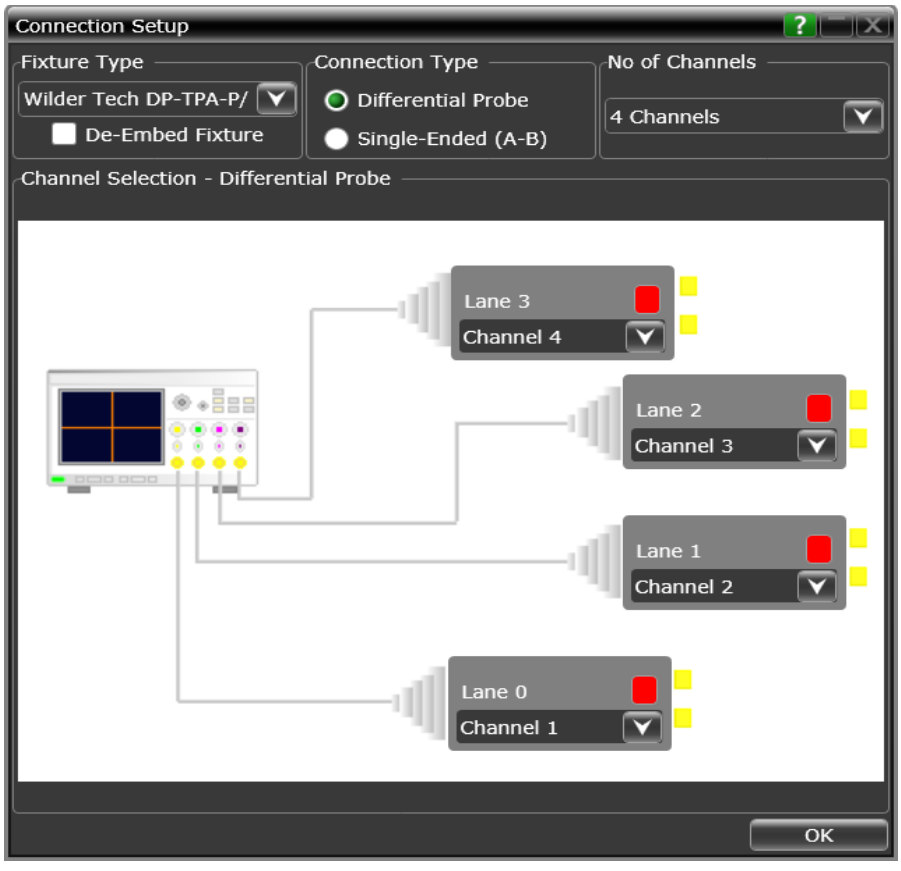
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

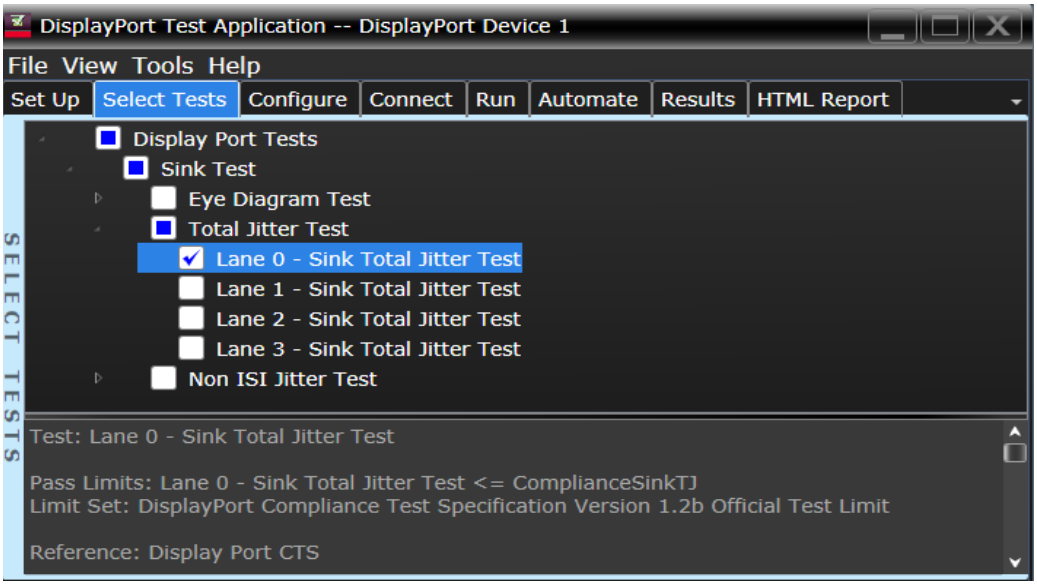
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR and HBR2)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	RBR, HBR–PRBS7 HBR2–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 31 Total Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	0.580 UI*

* The limits for the Total Jitter are derated by 0.04 UI from 0.62 UI in DisplayPort 1.2a Standard.

Table 32 Total Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Sink Non-ISI Jitter Test

Test ID

12220001, 12220002, 12220003, 12220004 — Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the Non ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

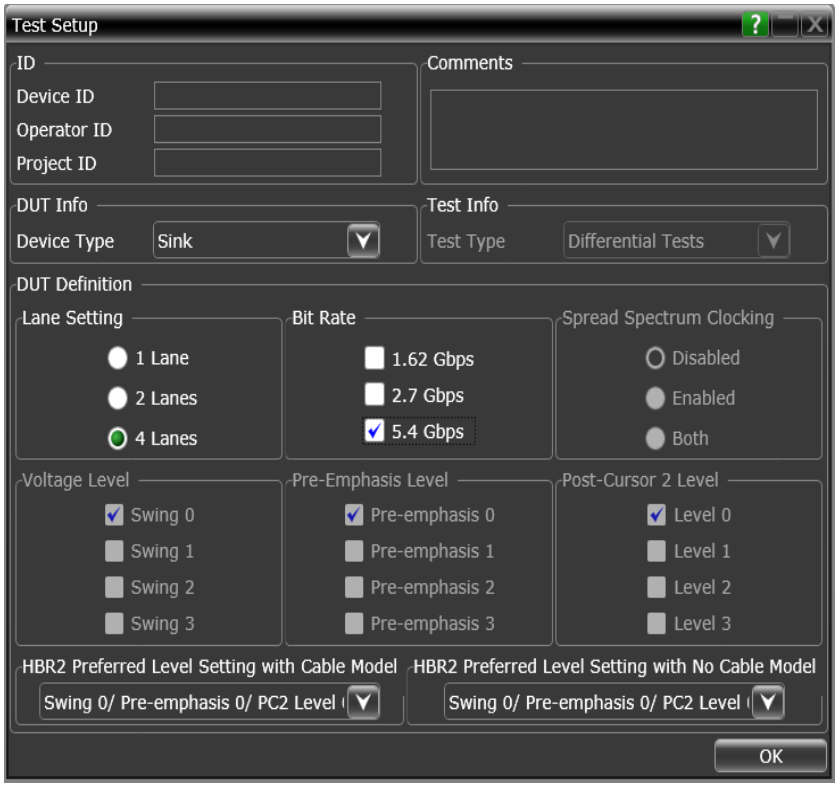
Calculate Non-ISI Jitter using the following equation:

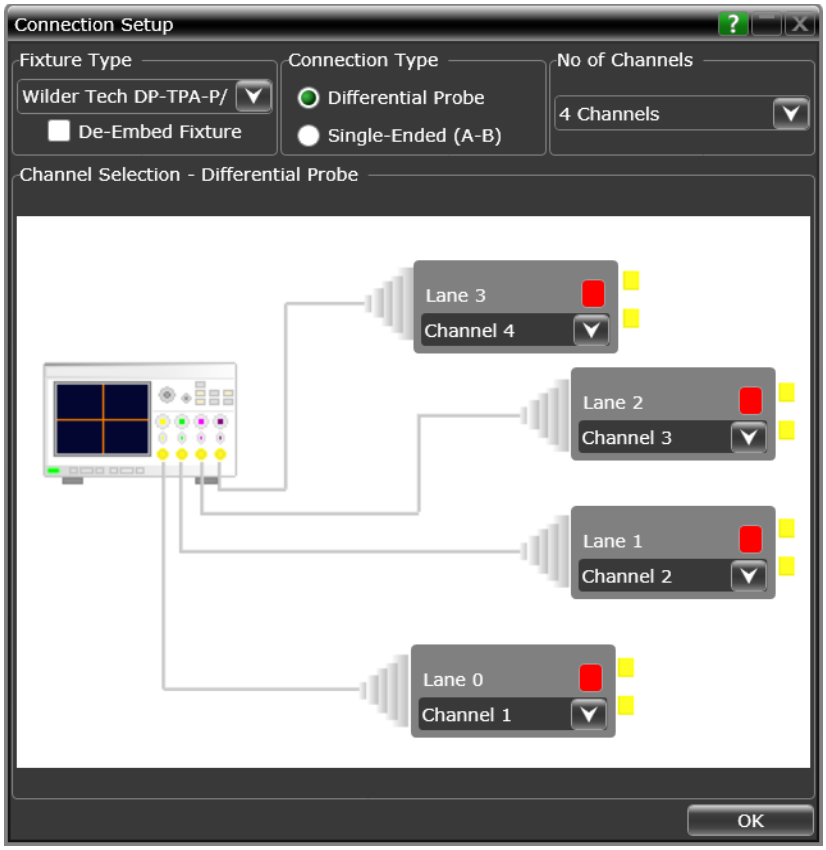
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

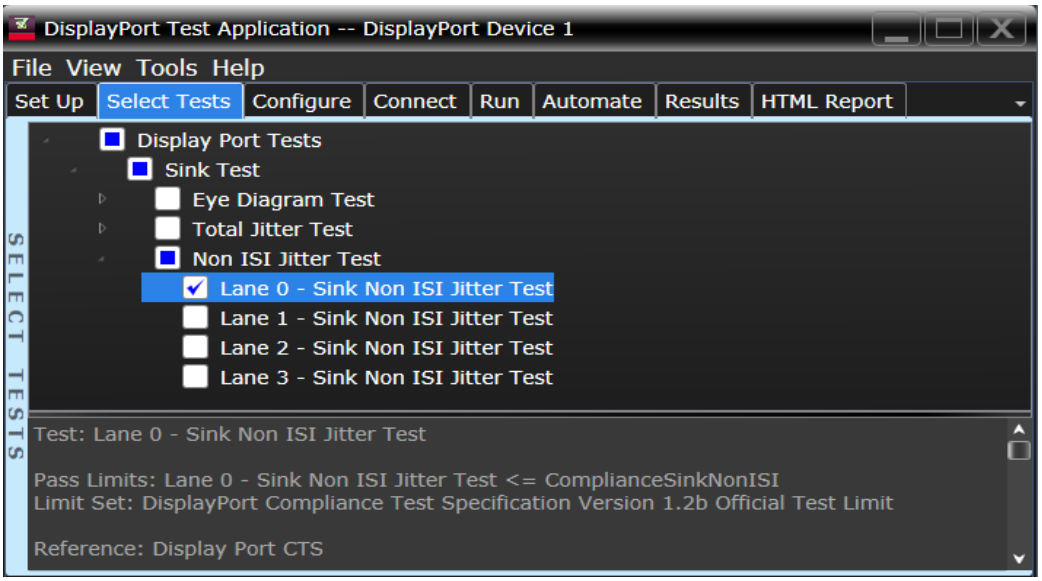
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR and HBR2)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	RBR, HBR–PRBS7 HBR2–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 33 Non ISI Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	-

Table 34 Non ISI Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

5 DisplayPort 1.2b Cable Tests

Overview

Test Point Definition for DisplayPort 1.2 (1.2b) Cable Tests

NOTE Cable Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Cable DUT at Test Point 3 (TP3) as shown in Figure 30. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

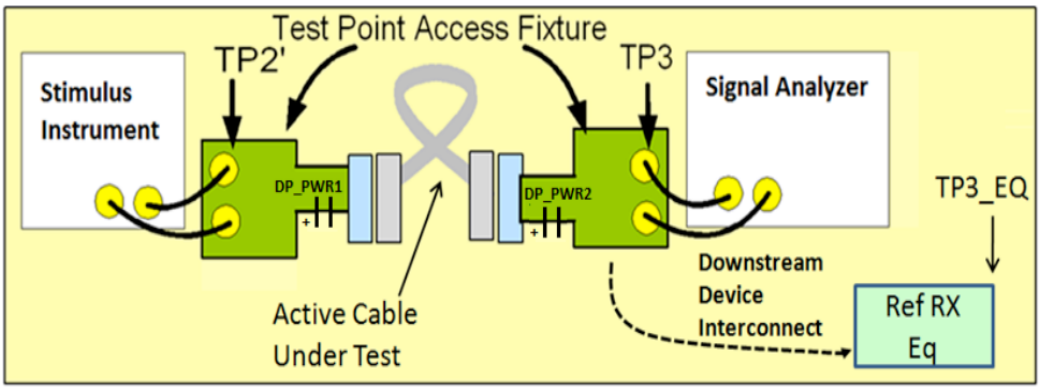


Figure 30 Test Point 3 Connection for DisplayPort 1.2 Cable Tests

Table 35 defines the test point fixtures and instruments used for DisplayPort 1.2 (1.2b) Cable Tests:

Table 35 Test Point Fixtures and Instruments for DisplayPort 1.2 Cable Tests

Test Requirement	Device Used
Stimulus Instrument	Pulse Pattern Generator ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Table 36 defines the input signal parameters applied by the stimulus instrument at TP2:

Table 36 Input Signal Parameters by Stimulus Instrument

RBR	▪ Reference Table 3-22 and Table 3-24, DP 1.2a ▪ Edge Rate (20-80): 155-165ps (260mUI) ▪ Eye Height: 400mV ▪ Total Jitter: 270mUI ▪ ISI: 100mUI ▪ Random Jitter (rms): 7.9mUI ▪ Sinusoidal Jitter: ~75mUI at 20MHz (Adjust to achieve Total Jitter)
HBR	▪ Reference Table 3-22 and Table 3-23, DP 1.2a ▪ Edge Rate (20-80): 90-100ps (260mUI) ▪ Eye Height: 350mV ▪ Total Jitter: 420mUI ▪ ISI: 144mUI ▪ Random Jitter (rms): 13.2mUI ▪ Sinusoidal Jitter: ~117mUI at 20MHz (Adjust to achieve Total Jitter)

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Cable Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort 1.2b Standards, the option **1.2b** appears by default in the **Test Specification** drop-down options.
5. The option **Physical Layer Tests** appears by default in the **Test Selection** area.
6. Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.
7. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
8. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
9. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
10. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
11. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
12. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
13. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
14. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DisplayPort 1.2 Cable Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

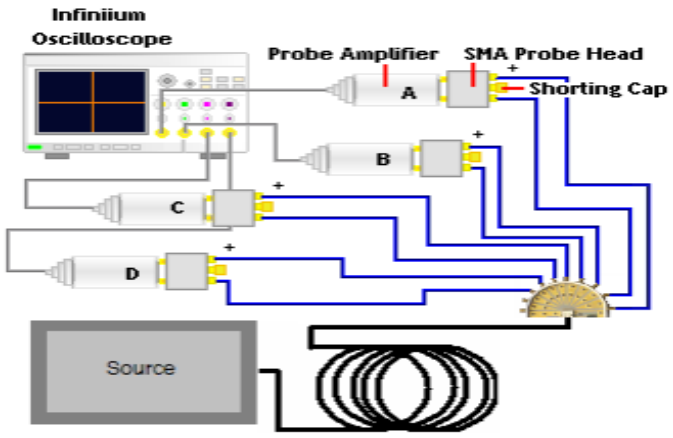


Figure 31 Sample connection diagram for DisplayPort 1.2 Cable Tests

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Cable tests to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1 In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.

2 On the **Test Setup** window,

a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b In the **DUT Info** area, select the **Device Type** as **Cable**.

c In the **Test Info** area, the **Test Type** options are grayed out.

d In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.

3 Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1 Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.

2 On the **Connection Setup** window,

a Select the appropriate option in the **Fixture Type** to indicate where the DUT is connected to.

b Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.

c In the **Channel Selection** area, assign appropriate channels to lanes.

3 Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of cable tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Cable Tests" on page 206 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Cable Eye Diagram Test

Test ID

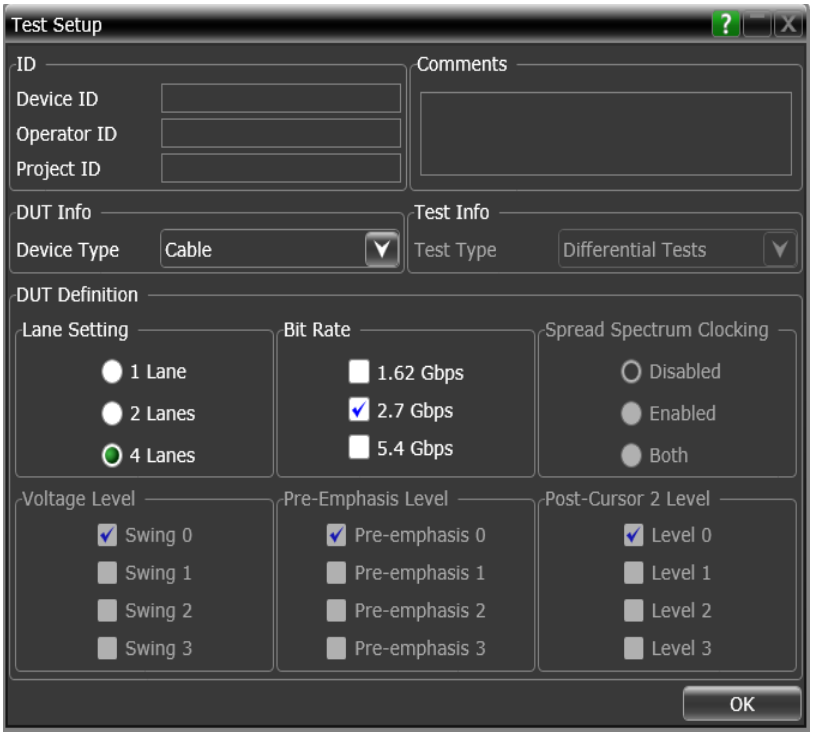
12150001, 12150002, 12150003, 12150004 – Cable Eye Diagram Test

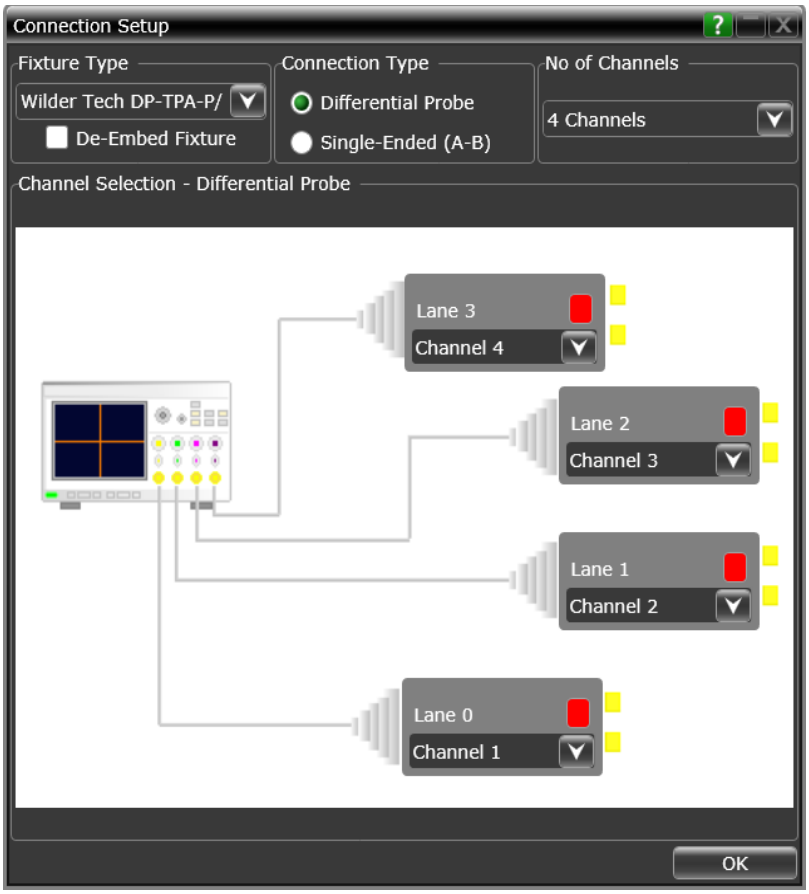
Test Overview

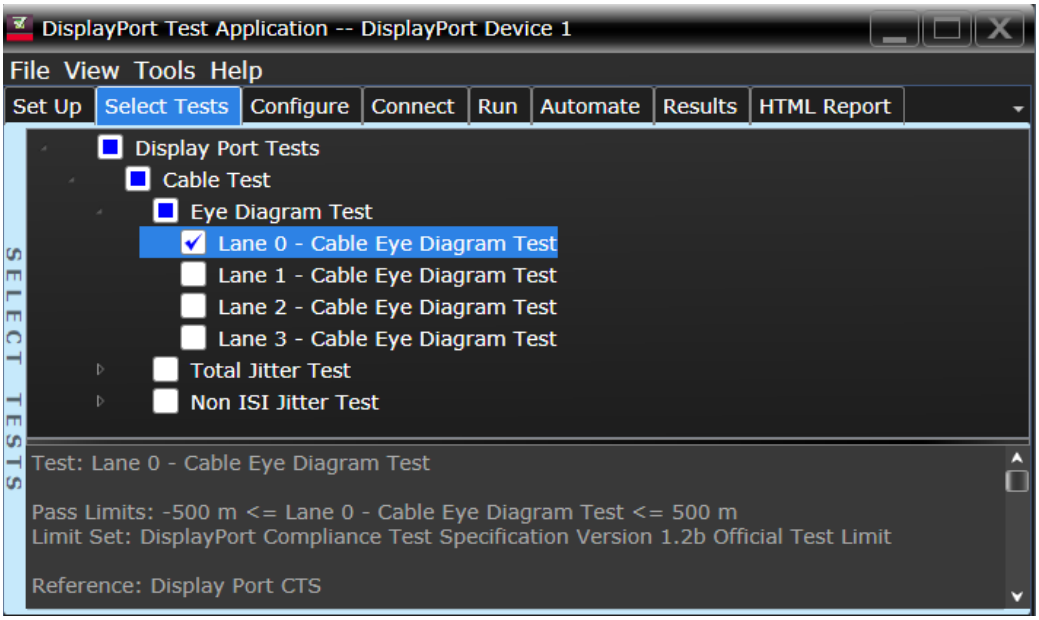
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 36
Crosstalk Signal Parameter	Quarter-rate clock signal (D24.3 pattern) is injected to lanes other than the lane under test. The characteristics of the aggressor signals are: Pattern–D24.3 Bit Rate–(Same as lane under test) Voltage Amplitude–(Same as lane under test) ▪ RBR-400mV ▪ HBR-350mV Edge Rate (20-80)–130ps at TP3


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
9 Measure the jitter of the eye diagram using the Histogram.

10 Check for any signal trajectories that may have entered into the mask.

11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 37 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 37 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

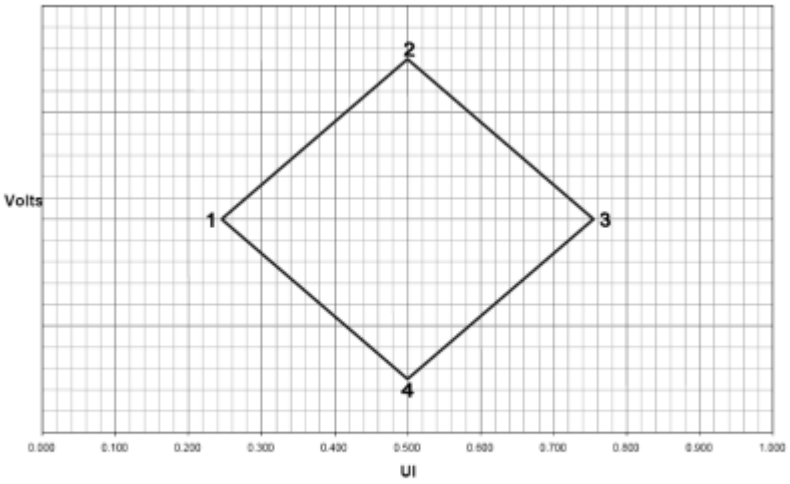


Figure 32 The Cable Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Cable Total Jitter Test

Test ID

12230001, 12230002, 12230003, 12230004 – Cable Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

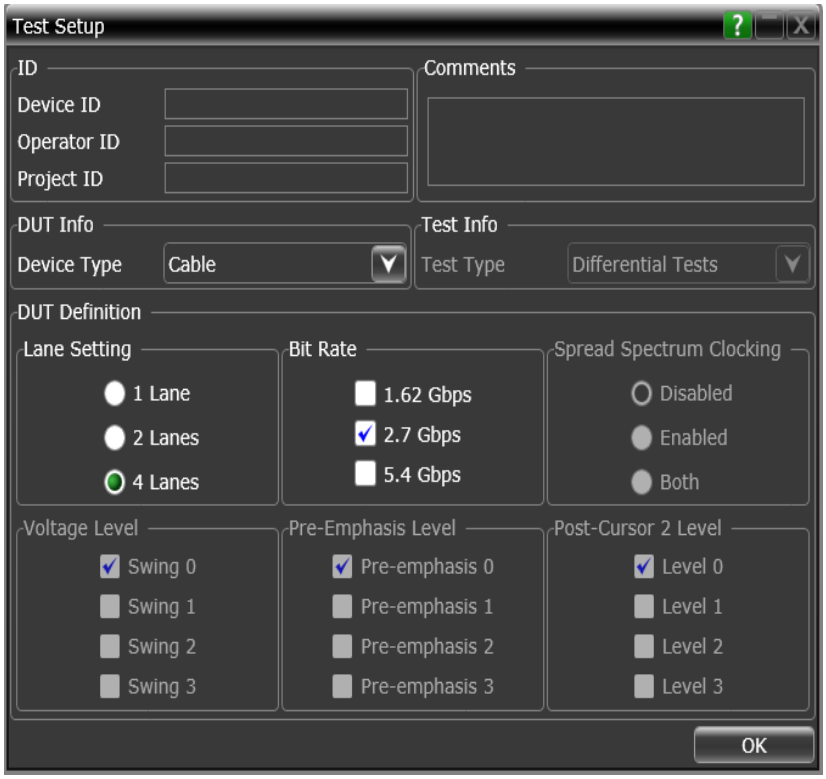
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

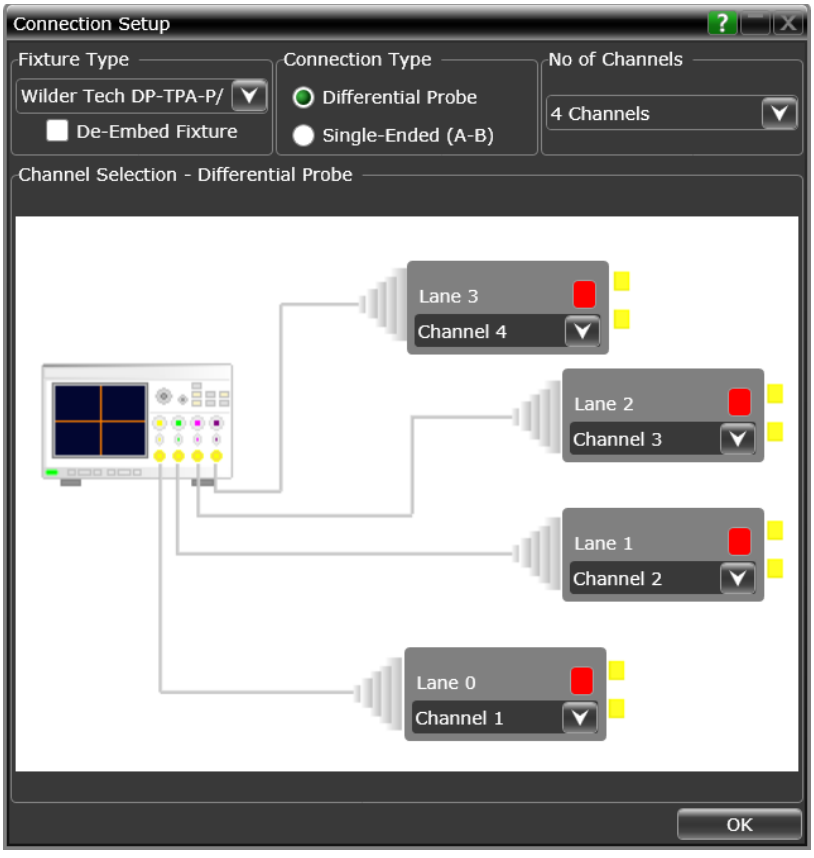
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

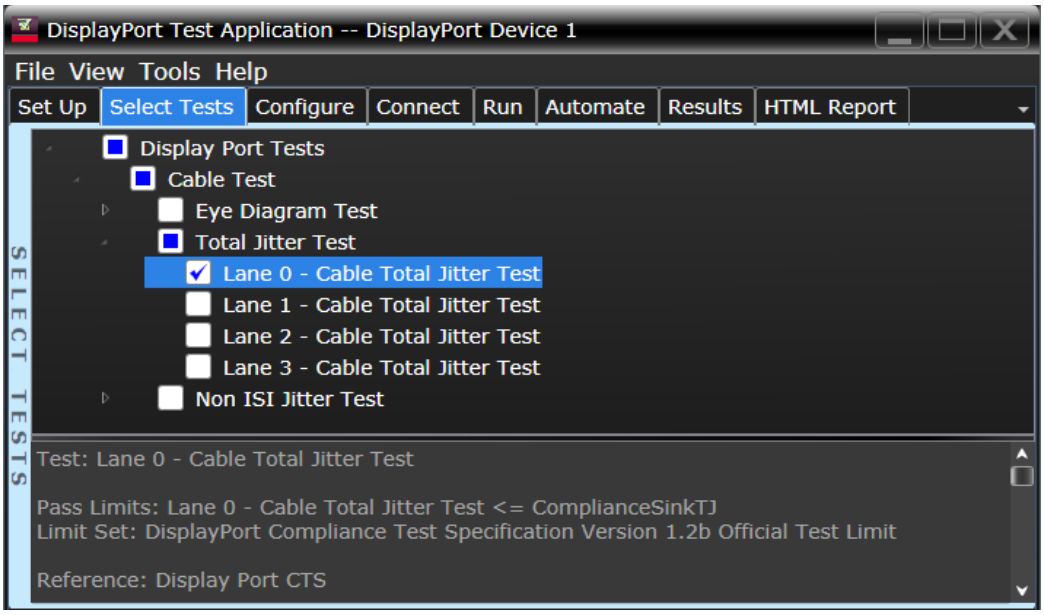
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 36


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 38 Total Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Cable Non-ISI Jitter Test

Test ID

12240001, 12240002, 12240003, 12240004 – Cable Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

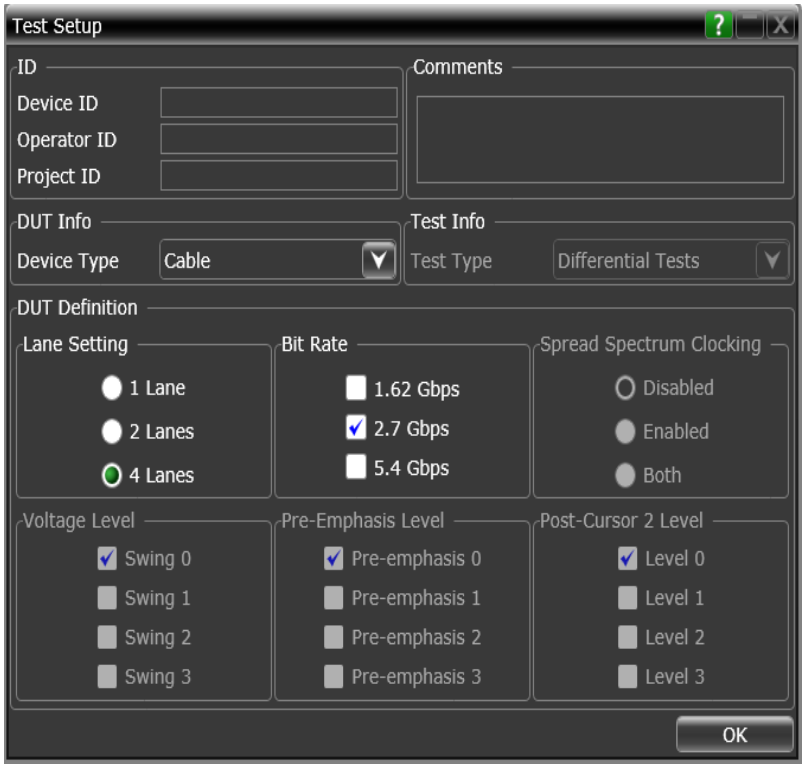
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

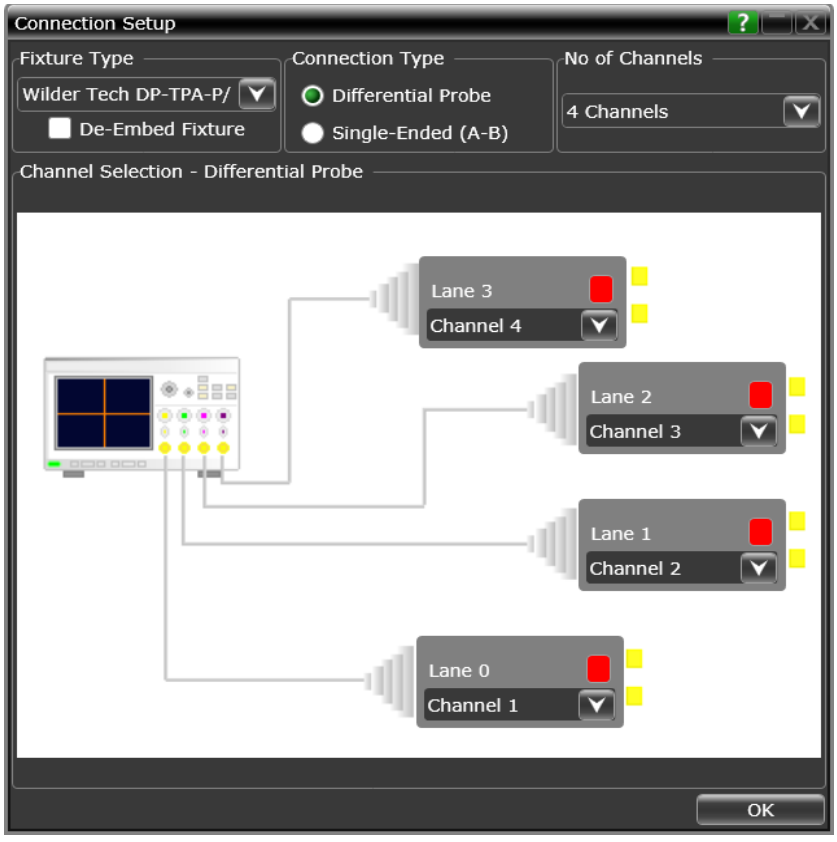
Calculate Non-ISI Jitter using the following equation:

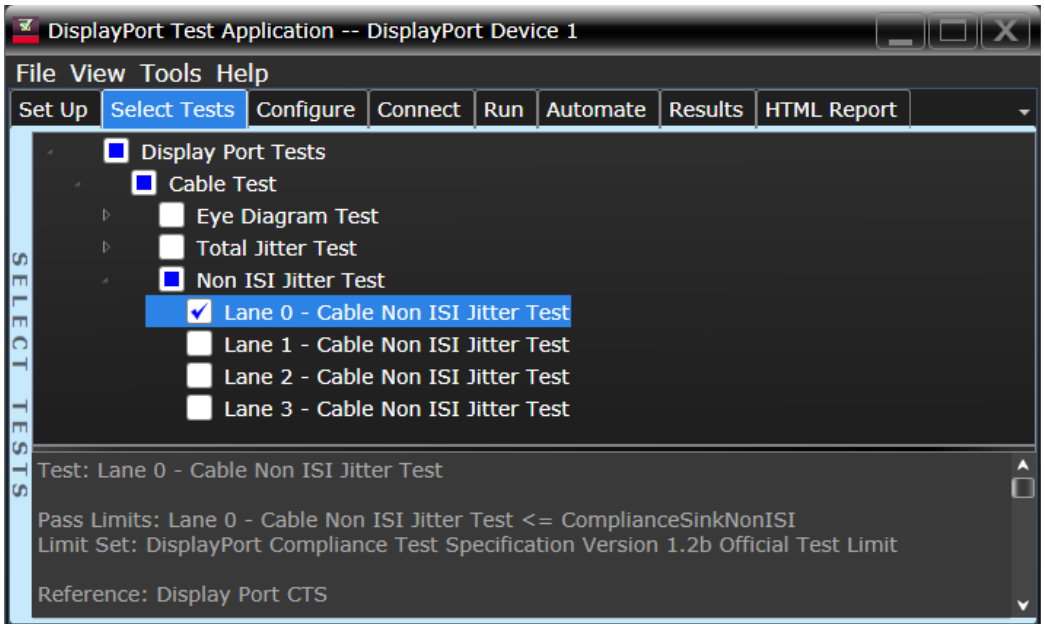
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 36


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 39 Non ISI Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non-ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

6 DisplayPort 1.2b AUX Channel Tests

This section describes the normative and informative AUX Channel physical layer tests and inrush tests for compliance verification of DisplayPort1.2 source and sink.

Overview

Test Point for AUX Channel Tests

You must test the Source devices at Test Point 2 (TP2) while the Sink devices must be tested at Test Point 3 (TP3). See Figure 33.

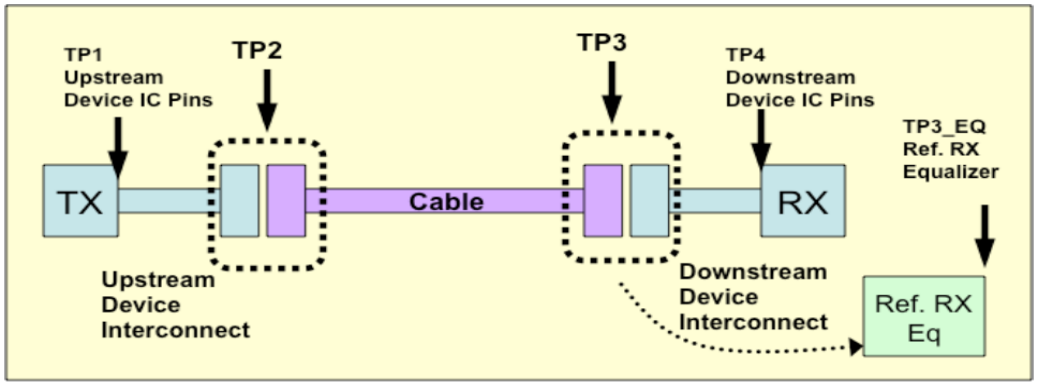


Figure 33 Test Point Connections for AUX Channel Tests

Table 40 defines the test point fixtures and instruments used for AUX Channel Tests:

Table 40 Test Point Fixtures and Instruments for AUX Channel Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-P* ▪ W2641B DisplayPort Test Point Access Adapter For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-P* ▪ Luxshare ICT mDP Plug (mDP-TPA-P)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope
Stimulus	Stimulus must be applied to the DUT to cause AUX Channel transactions to occur. This stimulus shall not be included in or affect the measurements. Reference Sink needed as stimulus for the Source DUT: ▪ Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Reference Source needed as stimulus for the Sink DUT: ▪ Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 AUX Channel Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort 1.2b Standards, the option **1.2b** appears by default in the **Test Specification** drop-down options.

5 Select the option **AUX PHY and Inrush Tests** in the **Test Selection** area.

6 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

7 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

8 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

9 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

10 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

11 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

12 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

13 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Settings for AUX PHY and Inrush Tests

Perform the following steps before you run the Auxiliary Channel and Inrush tests on the source or sink device:

1 Click the **Test Setup** button on the **Set Up** tab to set up for Auxiliary Channel and Inrush tests.

2 On the **Test Setup** window,

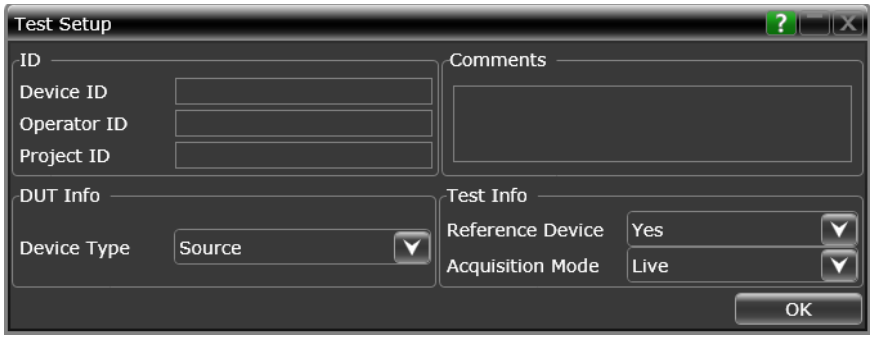
a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b From the **Device Type** drop-down options, select either **Source** or **Sink**.

c From the **Reference Device** drop-down options, select **Yes** if a reference sink/source is attached to device under test during testing.

d From the **Acquisition Mode** drop-down options, select **Live** if waveform acquisition and analysis will be performed on an online Infiniium Oscilloscope, else select **Offline**.

3 Click **OK** to exit the **Test Setup** window.

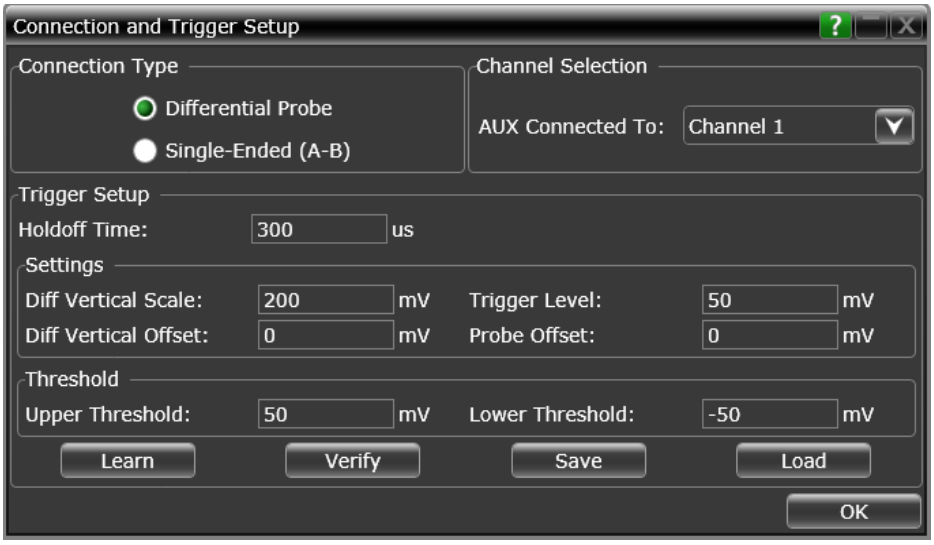


4 Click the **Connection Setup** button that now appears on the **Set Up** tab.

5 On the **Connection and Trigger Setup** window,

a Select either **Differential Probe** or **Single-Ended (A-B)** in the **Connection Type** area, depending on the probe connection you are using.

b From the **AUX Connected To:** drop-down options of the **Channel Selection** area, select the Oscilloscope Channel where the Auxiliary Lane is connected to.



c In the **Trigger Setup** area, define the Oscilloscope parameters to trigger on an Auxiliary signal during testing.

- **Hold Off Time** – The Oscilloscope minimum hold off time before triggering the next waveform. Note that any Auxiliary transaction from the source must receive a reply from the sink in 400 us, else such a transaction is considered a timeout. Hold off time, in such cases, represents the minimum idle time before each AUX transaction is initialized. It is defaulted to 300 us, which is a safe timing value for most devices tested in the lab. Most devices respond much faster than 300 us.
- **Trigger Level** – The AUX Channel signal level on which to trigger. Note that for a bi-directional signal (where a reference sink is attached), you must set the trigger level such that it crosses both the source command and the sink reply signal. Figure 34 and Figure 35 shows correct and incorrect trigger levels.

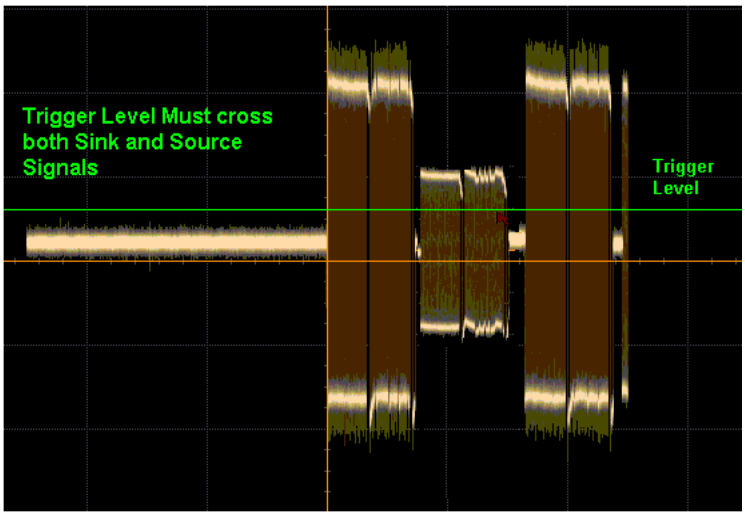


Figure 34 Correct Trigger Level

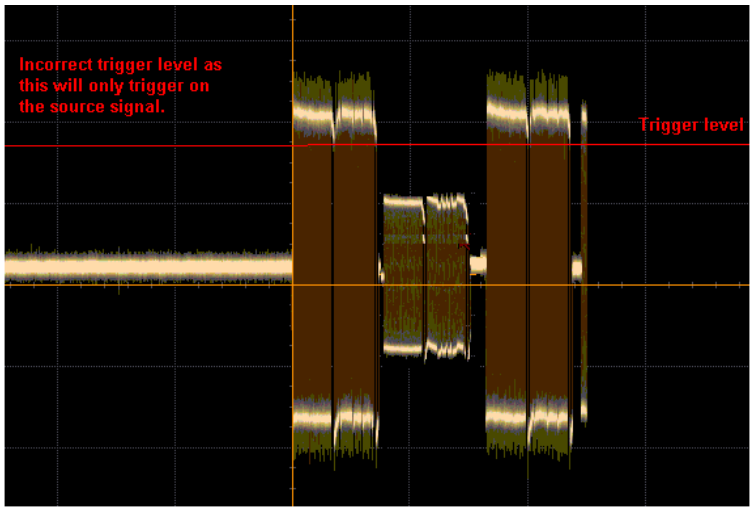


Figure 35 Incorrect Trigger Level

- **Vertical Scale** – The Oscilloscope vertical scale. Set the vertical to make sure that all signals are visible on the oscilloscope display.
- **Vertical Offset** – The Oscilloscope vertical offset. Set the offset so that the center point is aligned with the center of the oscilloscope display.
  Upper Threshold/Lower Threshold – The threshold level of signal must be set properly so that both upper and lower thresholds cross both the source and sink signals when the DUT is attached with a reference sink. The threshold levels are important parameters because they are used for edge detection when decoding a source command from a sink reply. Figure 36 and Figure 37 shows correct and incorrect threshold levels.

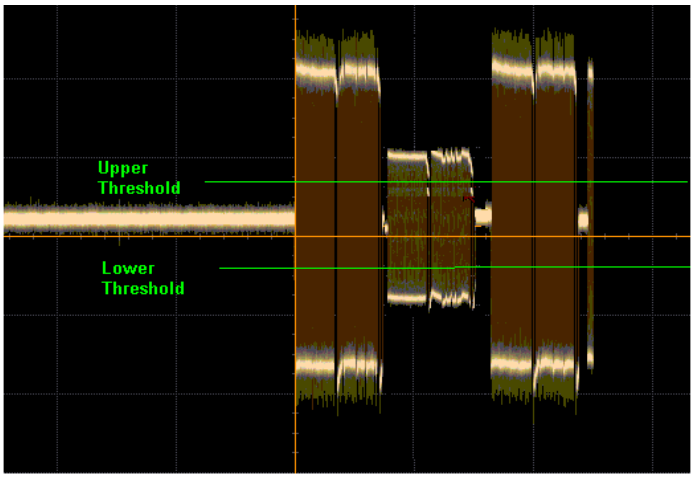


Figure 36 Correct Threshold set

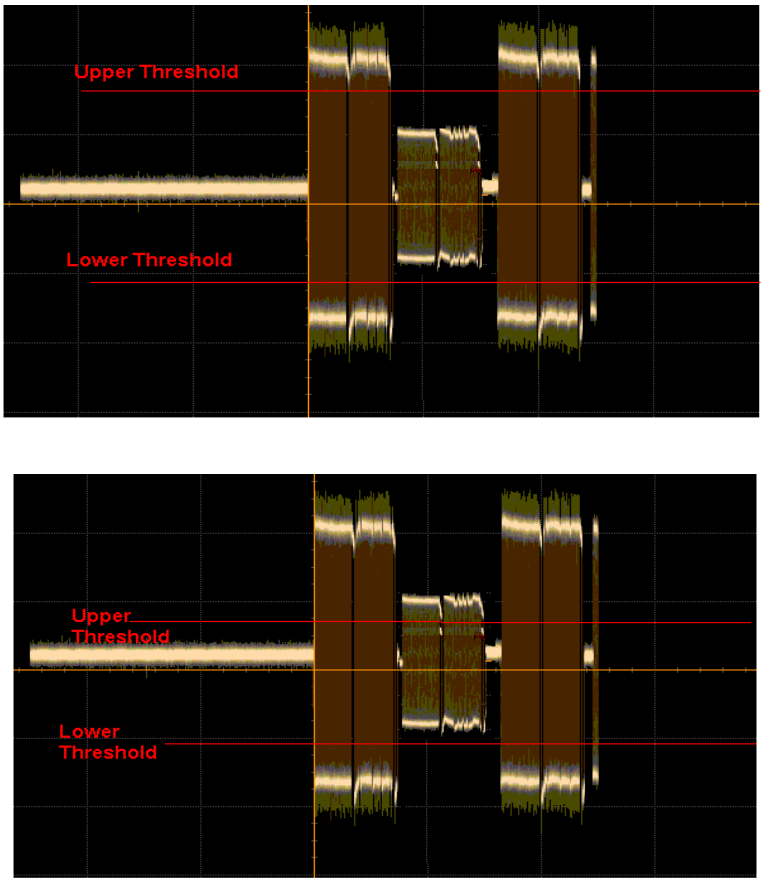


Figure 37 Wrong Thresholds set

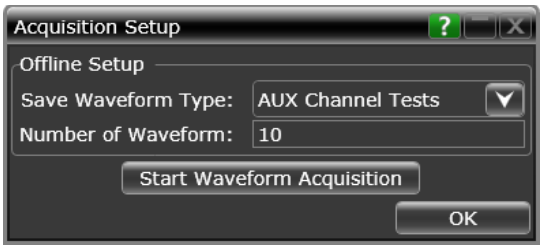
- Click the **Learn** button to access the information guide about the trigger setup parameters. However, note that the learning guide may not necessarily work due to variation in the actual Auxiliary signals, owing to different manufacturers. Keysight recommends that you must check to make sure that the parameters are correctly set as previously described.

- Click **Verify** and follow the instructions, if you wish to check the AUX Channel trigger.
- You may **Save** or **Load** the trigger setup configuration as a **.tsf* file.

6 Click **OK** to exit the **Connection and Trigger Setup** window.

7 If you select the option **Offline** for the **Acquisition Mode** in the **Test Setup** window, the **Acquisition Setup** button appears in the **Test Environment Setup** area of the **Set Up** tab.

8 Click the **Acquisition Setup** button to save the waveform files so that you can avoid the manual process to initiate Auxiliary transactions during the time of test runs.



9 On the **Acquisition Setup** window,

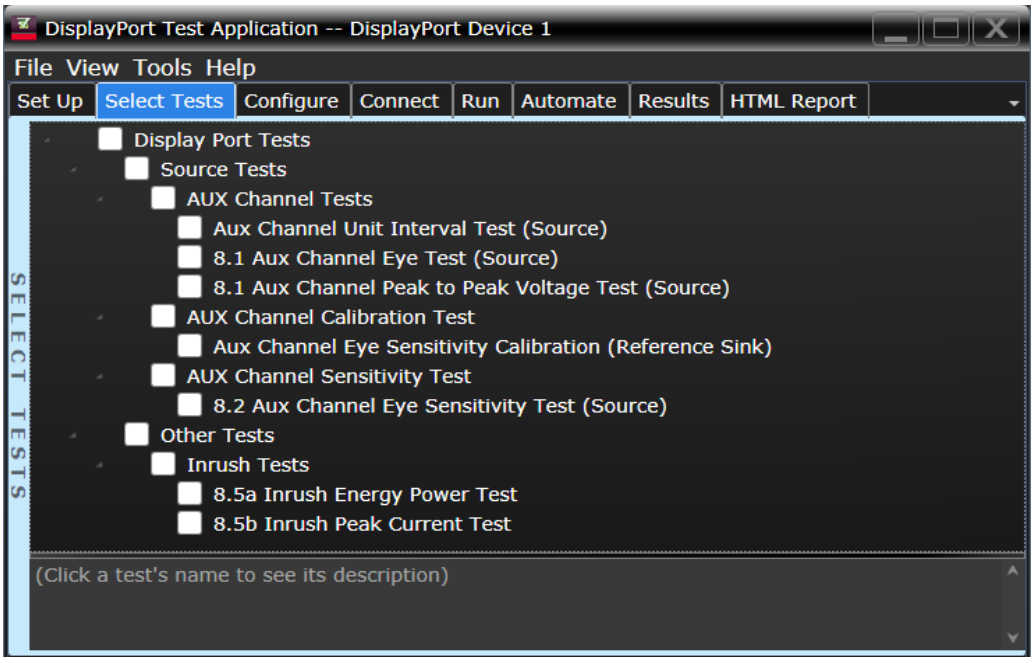
a select the type of waveforms to be saved from the **Save Waveform Type:** drop-down options.

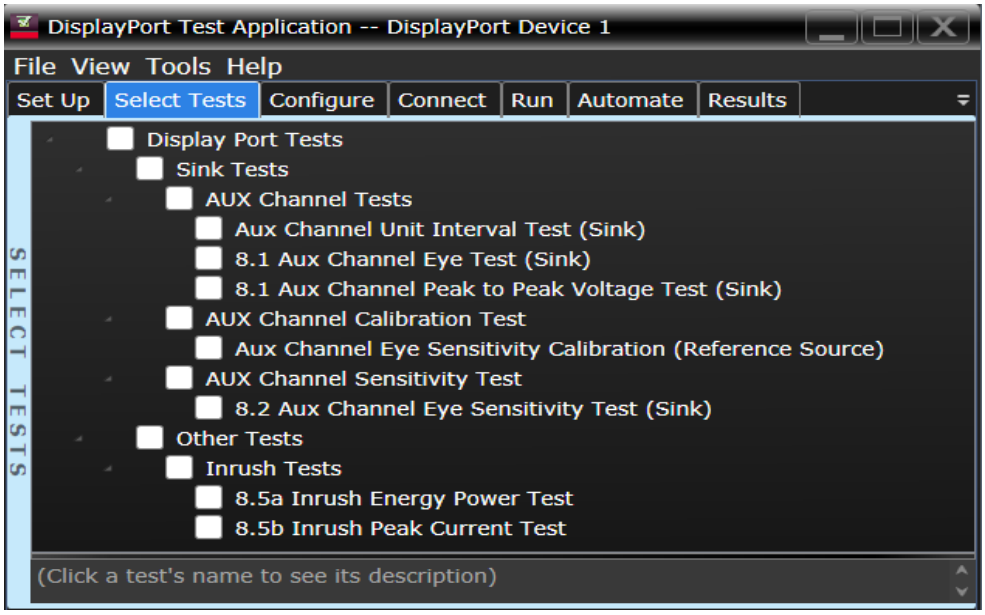
b define the number of waveforms to be saved in the **Number of Waveform:** field.

c Click the **Start Waveform Acquisition** button to start capturing and saving waveforms.

d Click **OK** to return to the **Set Up** tab.

10 Click the **Select Tests** tab where the AUX Channel tests for Source or Sink devices appear.





Probing/Connection Set Up for AUX Channel Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests. When performing the Source AUX Channel tests, a Reference Sink device is required. Similarly, when performing the Sink AUX Channel tests, a Reference Source device is required.

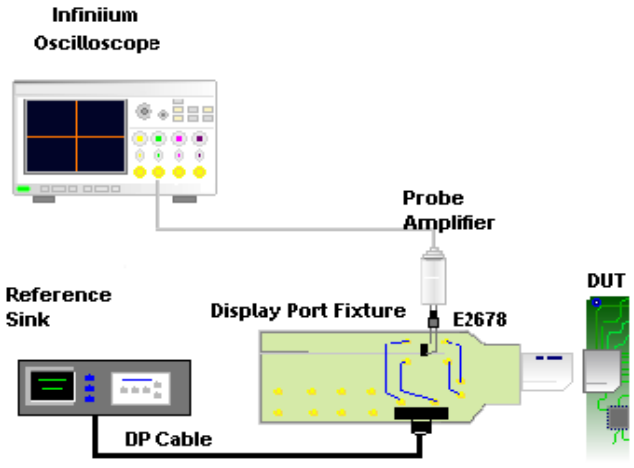


Figure 38 Sample connection diagram for source AUX channel tests with source DUT connected to a reference sink

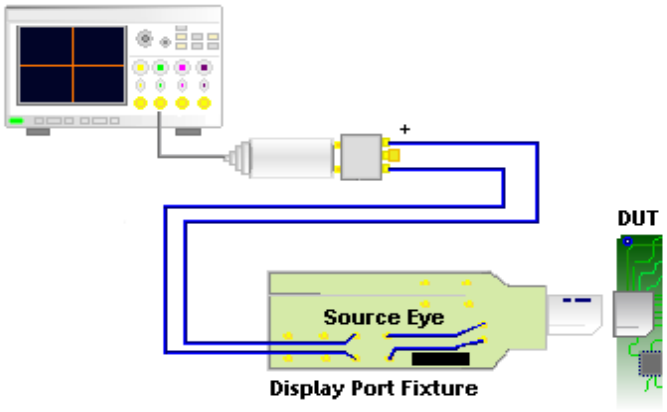


Figure 39 Sample connection diagram for source AUX channel tests without connecting to a reference sink

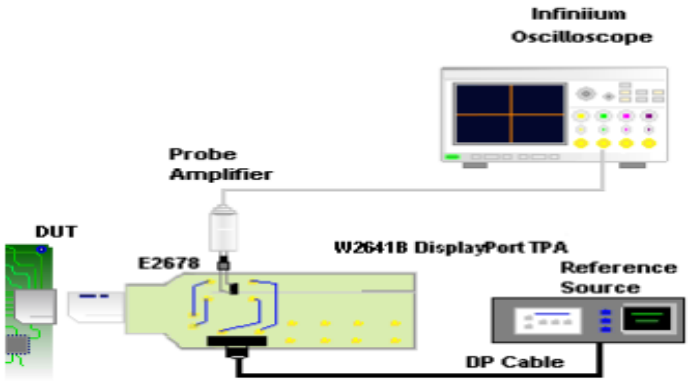


Figure 40 Sample connection diagram for sink AUX channel tests with sink DUT connected to a reference source

AUX Channel Unit Interval Test

Test ID

125000 – AUX Channel Unit Interval Test (Source)

125010 – AUX Channel Unit Interval Test (Sink)

Test Overview

The objective of the test is to evaluate the AUX Channel waveform, ensuring that the overall variation of the Manchester transaction Unit Interval stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Set up the parameter of the measurement trend:

   a Set up the Unit Interval measurement for the differential AUX Channel signal.

   b Set up the frequency measurement for the Clock signal.

   c Set up the measurement trend.

6 Set up the waveform Histogram on the measurement trend:

   a Initialize AUX Channel transactions and acquire the differential AUX Channel signal.

   b Identify the first and the last points for the desired transaction.

   c Zoom-in on the desired transaction.

   d Set up the Vertical Waveform Histogram on the measurement trend within the desired transaction.

   e Obtain the measurement for the mean, maximum and minimum values of the waveform Histogram.

7 Repeat step 6 ten times.

8 Report the measurement results.

PASS Condition

Manchester Transaction Unit Interval (UI_{MAN}):

Minimum = 0.4 µsec

Maximum = 0.6 µsec

Test References

See:

- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured unit interval for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Test

Test ID

125001 – AUX Channel Eye Test (Source)

125011 – AUX Channel Eye Test (Sink)

Test Overview

The objective of this test is to evaluate the transmitter AUX Channel waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

7 Set up the waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

8 Set up the parameters for the Mask Test.

   a Load the eye mask based on the settings in the Configuration Variable.

   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

   c Initialize the AUX Channel transaction and run the eye mask until 10 waveforms are folded.

9 Check for any signal trajectories entering into the mask.

10 Report the measurement results.

PASS Condition

PASS Value = 290mV_diff_pp or higher

FAIL Value = lower than 290mV_diff_pp

Table 41 Eye Mask Vertices for AUX Channel for Manchester Transactions

Mask Point	Time (from EYE Center)	Minimum Voltage Value at Six Vertices (mV)
1	-185ns	0
2	-135ns	145
3	135ns	145
4	185ns	0
5	135ns	-145
6	-135ns	-145

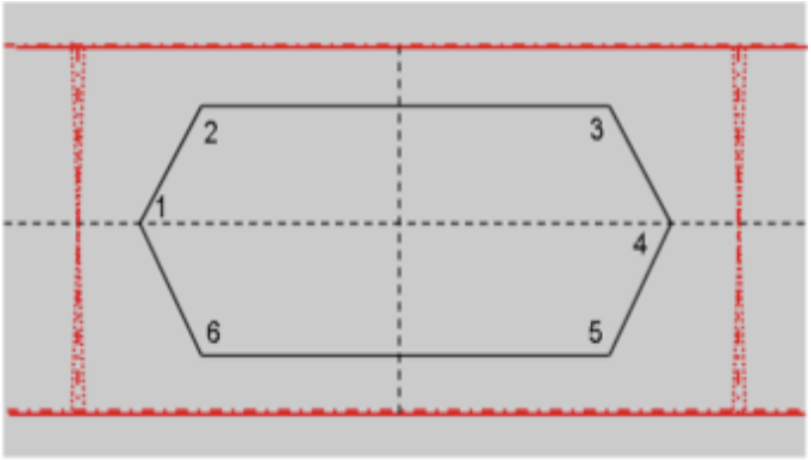


Figure 41 AUX Channel EYE Mask for Manchester Transactions

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2.6, Figure 3-29 and Table 3-8*

Expected/Observable Results

The measured eye diagram for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

AUX Channel Peak-to-Peak Voltage Test

Test ID

125002 – AUX Channel Peak-to-Peak Voltage Test (Source)

125012 – AUX Channel Peak-to-Peak Voltage Test (Sink)

Test Overview

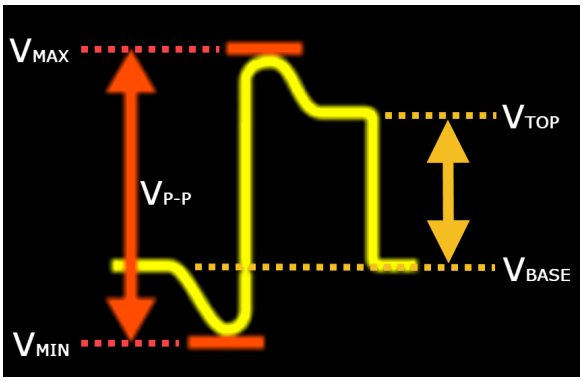
The objective of the test is to evaluate the transmitter AUX Channel Waveform, ensuring that the peak-to-peak voltage stays within the specification limits.

NOTE

The peak to peak voltage (V_{P-P}) formula is:

$$V_{P-P} = V_{MAX} - V_{MIN}$$

Please see the figure below for more info.



Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

a Enable measurement of all edges to obtain a statistical value of the measurement.

b Set up the measurement threshold.

c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

7 Set up the horizontal waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

8 If you have selected the “AUX Channel Eye Test” under the **Select Tests** tab of the compliance application:

a Set up the parameter of the Mask Test:

i Load the eye mask based on the settings in the Configuration Variable.

ii Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

iii Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.

b Check for any signal trajectories entering into the mask.

9 Set up the waveform histogram on the AUX Channel eye diagram.

a Set up the vertical waveform histogram on the AUX Channel eye diagram to measure the peak to peak voltage.

10 Report the measurement results.

PASS Condition

Table 42 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage at a transmitting device ($V_{AUX\text{-}DIFFp\text{-}p}$)	0.29V	1.38V

Test References

See:

- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured peak-to-peak voltage for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Calibration Test

Test ID

125021 – AUX Channel Eye Sensitivity Calibration (Reference Sink)

125031 – AUX Channel Eye Sensitivity Calibration (Reference Source)

Test Overview

The objective of this test is to calibrate the peak-to-peak voltage of the transmitter AUX Channel waveform by reference device (reference source or reference sink), ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.

2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

4 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

5 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

6 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

7 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

8 Set up the waveform Histogram on the AUX Channel eye diagram:

   a Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.

   b Set up the vertical waveform Histogram of width 0.6 UI at the center of the AUX Channel eye diagram.

   c Measure the V_{TOP} and V_{BASE} using the waveform Histogram mean value.

9 Repeat Step 8 three times.

10 Report the measurement results.

PASS Condition

Table 43 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage for AUX Channel Eye Sensitivity	0.24V	0.28V

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured peak-to-peak voltage for the AUX Channel signal by reference device (reference source or reference sink) shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Test

Test ID

125041 – AUX Channel Eye Sensitivity Test (Source)

125051 – AUX Channel Eye Sensitivity Test (Sink)

Test Overview

The objective of the test is to evaluate the sensitivity to the AUX Channel Eye Opening of the DUT as per the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.

2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

4 Set up the parameter of the measurement:

a Enable measurement of all edges to obtain a statistical value of the measurement.

b Set up the measurement threshold.

c Set up the Clock Recovery.

5 Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.

6 Check if the reference device could detect the transaction or not.

7 Decode the AUX Channel signal and check whether the transaction passed or failed.

8 Report the measurement results.

PASS Condition

Determine whether the AUX Channel communication is successful. For example, the Transmitter DUT sends an AUX Request to the Reference Receiver. The Reference Receiver acknowledges and the Transmitter DUT responds to the to indicate that the acknowledgment was successfully received.

PASS = No errors observed in the response

FAIL = One or more errors observed

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured AUX Channel transaction shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

7 DisplayPort 1.2b Inrush Tests

Overview

This section describes the normative and informative inrush tests for compliance verification of DisplayPort1.2 source and sink, which is a power consumer.

Test Point for Inrush Tests

The test fixture for inrush tests implements the schematic shown in Figure 42.

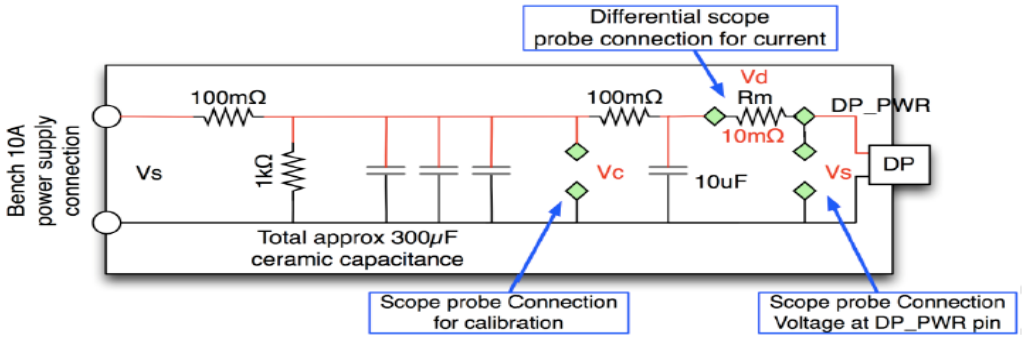


Figure 42 Schematics for testing Power Consumer Device

The test fixture must be designed and used according to the following guidelines:

- A high gate voltage FET on the DP_PWR line is recommended to allow a fast connect capability, which allows a single connection event for testing. Without such an arrangement, multiple connections will be required to obtain a reasonable “worst-case” attachment event.
- Connection length between the power supply and the test fixture must be minimized. A maximum of four inches is recommended.
- The power supply must have enough outrush capability as to not negatively affect the test fixture’s outrush capability.
- The power supply must be run at 3.6V (3.3V + 10%) read across V_C.

Any Power Consumer test fixture must be calibrated using the Power User test fixture, as shown in Figure 42. Testing with the two fixtures combined should result in the approximate values given below. If required, the component values on the Power Consumer test fixture should be adjusted to match the expected results.

- V_C steady before connection = 3.6V
- V_C droop = ~3.1V
- Inrush Current = ~13.0A

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Inrush Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort 1.2b Standards, the option **1.2b** appears by default in the **Test Specification** drop-down options.

5 Select the option **AUX PHY and Inrush Tests** in the **Test Selection** area.

6 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

7 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

8 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

9 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

10 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

11 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

12 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

13 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Refer to "Settings for AUX PHY and Inrush Tests" on page 225 for instructions on setting the DisplayPort 1.2b InRush tests.

Inrush Energy Power Test

Test ID

127000 – Inrush Energy Power Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush energy power measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Energy $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 13.5$ Amps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.5*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.2.3*

Expected/Observable Results

The measured worst case inrush energy power for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Inrush Peak Current Test

Test ID

127001 – Inrush Peak Current Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush peak current measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Energy $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 13.5$ Amps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.5*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.2.3*

Expected/Observable Results

The measured worst case inrush peak current for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

8 DisplayPort 1.2b Dual Mode Tests

Overview

This section describes the normative and informative dual mode physical layer (differential and single-ended) tests for compliance verification of DisplayPort1.2 DUTs.

Test Point

The source device for dual mode tests must be tested at Test Point 2 (TP2), as shown in Figure 43.

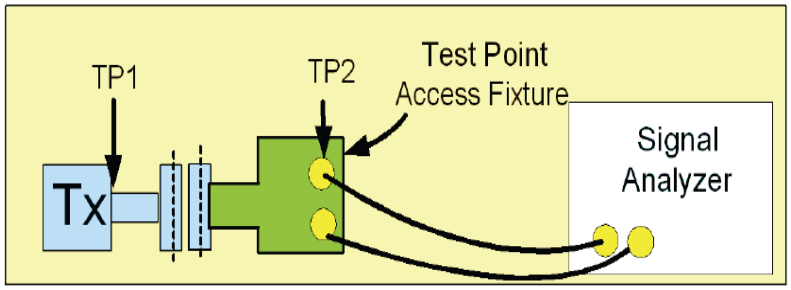


Figure 43 Test Point 2 Connection for Dual Mode Source Tests

Table 44 defines the test point fixtures and instruments used for DisplayPort 1.2 Dual Mode Tests:

Table 44 Test Point Fixtures and Instruments for DisplayPort 1.2 Dual Mode Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-P* ▪ W2641B DisplayPort Test Point Access Adapter For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-P* ▪ Luxshare ICT mDP Plug (mDP-TPA-P)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Dual Mode Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort 1.2b Standards, the option **1.2b** appears by default in the **Test Specification** drop-down options.

5 Select the option **Dual Mode Tests** in the **Test Selection** area.

6 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

7 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

8 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

9 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

10 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

11 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

12 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

13 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Setting Up for Dual Mode Tests

Perform the following steps before you run the Dual Mode tests on the source device:

1 Click the **Test Setup** button on the **Set Up** tab to set up for Auxiliary Channel and Inrush tests.

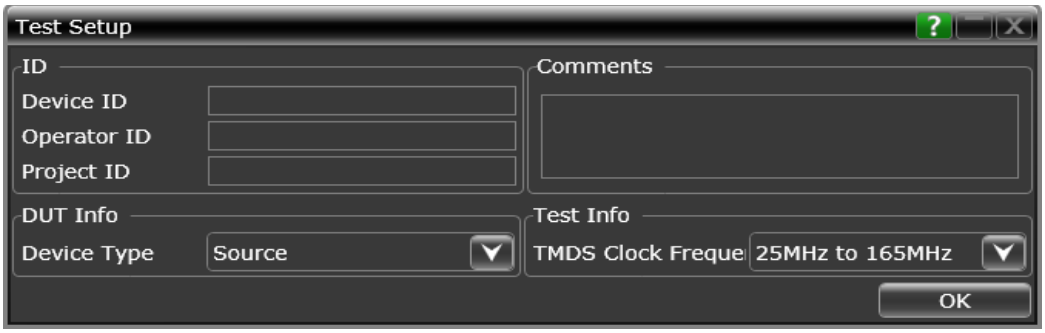
2 On the **Test Setup** window,

a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b In the **DUT Info** area, the **Device Type** is selected as **Source** by default.

c In the **Test Info** area, select the **TMDS Clock Frequency** either as **25 MHz to 165 MHz** or **165 MHz to 300 MHz**.

3 Click **OK** to exit the **Test Setup** window.



4 Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.

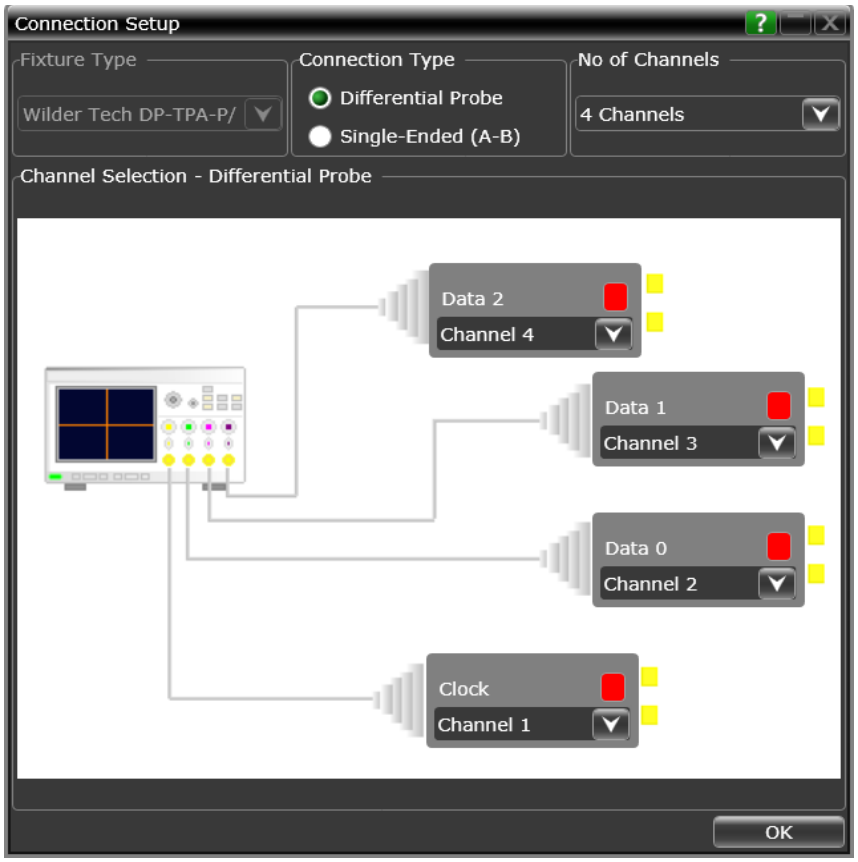
5 On the **Connection Setup** window,

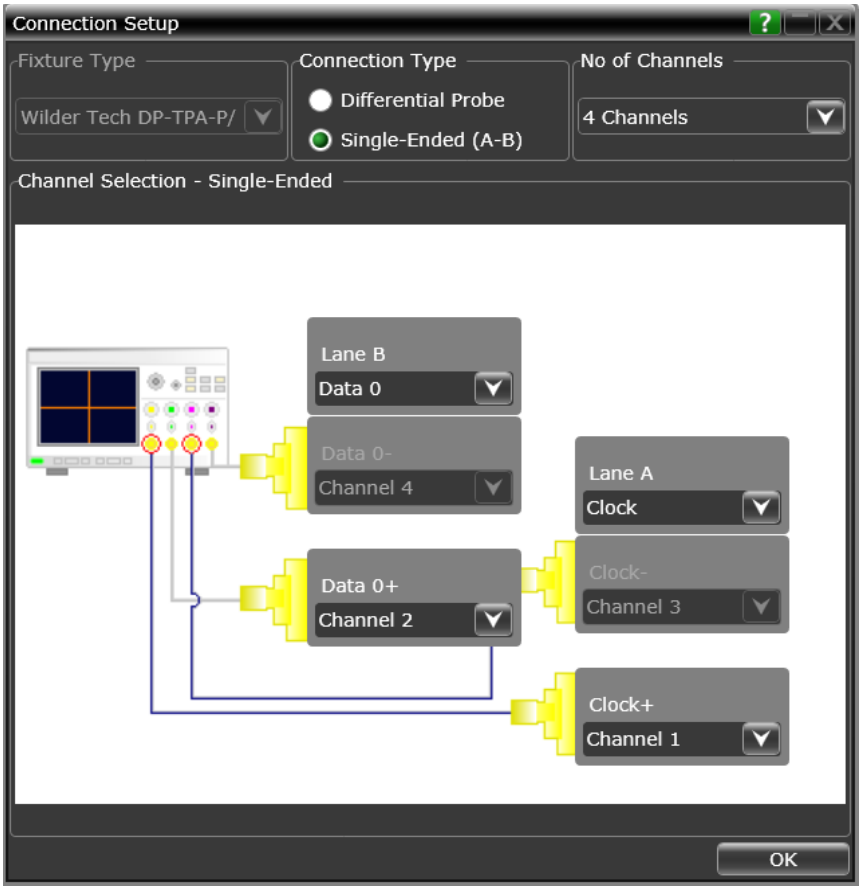
a The **Fixture Type** area is grayed out.

b Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.

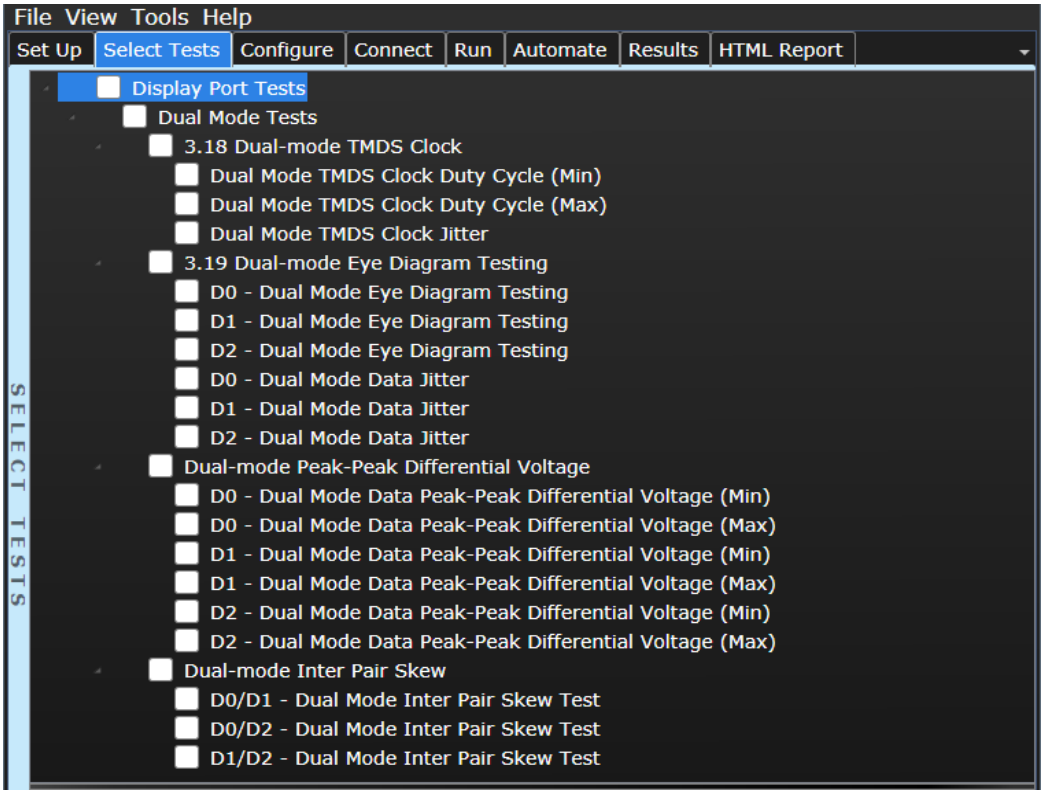
c In the **Channel Selection** area, assign appropriate channels to lanes.

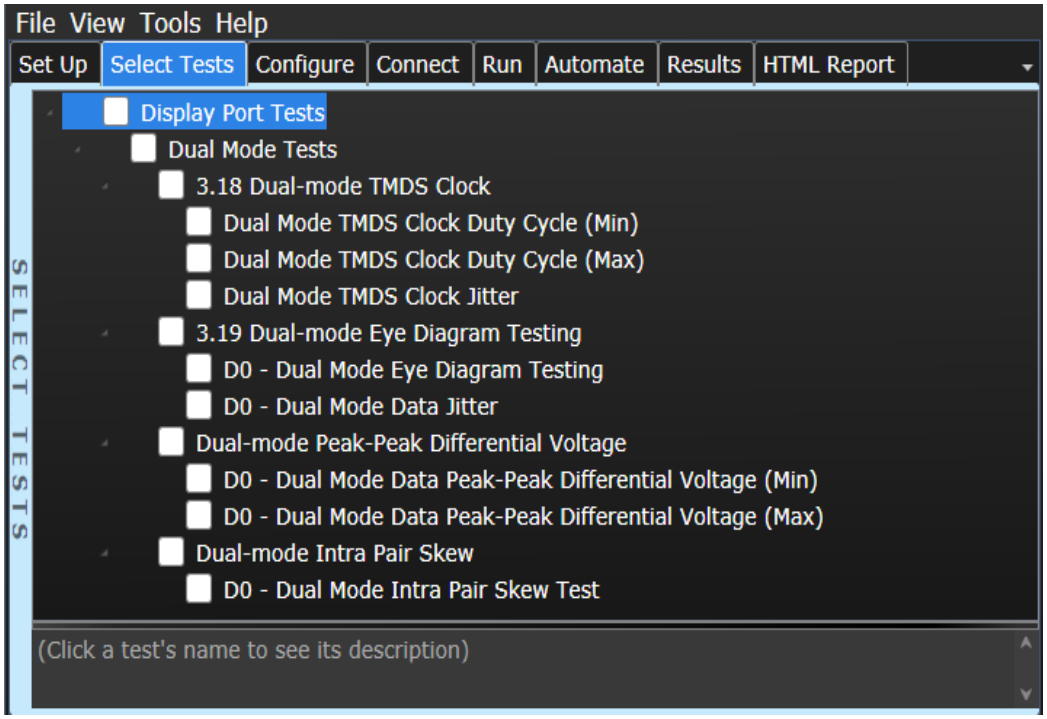
6 Click **OK** to return to the **Set Up** tab.





After configuring the **Test Setup** and **Connection Setup** to run a specific type of source tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Dual Mode Tests" on page 252 to complete the task flow for DUT setup along with configuring the Compliance Application to run each test.


File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Display Port Tests
Dual Mode Tests
3.18 Dual-mode TMDS Clock
Dual Mode TMDS Clock Duty Cycle (Min)
Dual Mode TMDS Clock Duty Cycle (Max)
Dual Mode TMDS Clock Jitter
3.19 Dual-mode Eye Diagram Testing
D0 - Dual Mode Eye Diagram Testing
D1 - Dual Mode Eye Diagram Testing
D2 - Dual Mode Eye Diagram Testing
D0 - Dual Mode Data Jitter
D1 - Dual Mode Data Jitter
D2 - Dual Mode Data Jitter
Dual-mode Peak-Peak Differential Voltage
D0 - Dual Mode Data Peak-Peak Differential Voltage (Min)
D0 - Dual Mode Data Peak-Peak Differential Voltage (Max)
D1 - Dual Mode Data Peak-Peak Differential Voltage (Min)
D1 - Dual Mode Data Peak-Peak Differential Voltage (Max)
D2 - Dual Mode Data Peak-Peak Differential Voltage (Min)
D2 - Dual Mode Data Peak-Peak Differential Voltage (Max)
Dual-mode Inter Pair Skew
D0/D1 - Dual Mode Inter Pair Skew Test
D0/D2 - Dual Mode Inter Pair Skew Test
D1/D2 - Dual Mode Inter Pair Skew Test


File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Display Port Tests
Dual Mode Tests
3.18 Dual-mode TMDS Clock
Dual Mode TMDS Clock Duty Cycle (Min)
Dual Mode TMDS Clock Duty Cycle (Max)
Dual Mode TMDS Clock Jitter
3.19 Dual-mode Eye Diagram Testing
D0 - Dual Mode Eye Diagram Testing
D0 - Dual Mode Data Jitter
Dual-mode Peak-Peak Differential Voltage
D0 - Dual Mode Data Peak-Peak Differential Voltage (Min)
D0 - Dual Mode Data Peak-Peak Differential Voltage (Max)
Dual-mode Intra Pair Skew
D0 - Dual Mode Intra Pair Skew Test
(Click a test's name to see its description)

Probing/Connection Set Up for Dual Mode Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

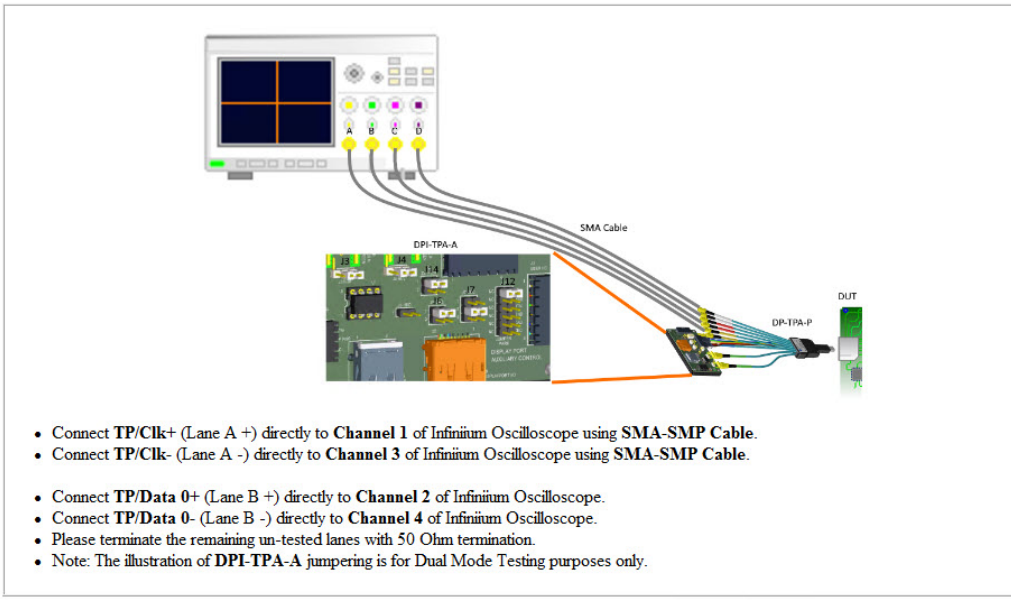


Figure 44 Sample Connection Diagram for a 4-Channel Single-Ended Dual Mode Test

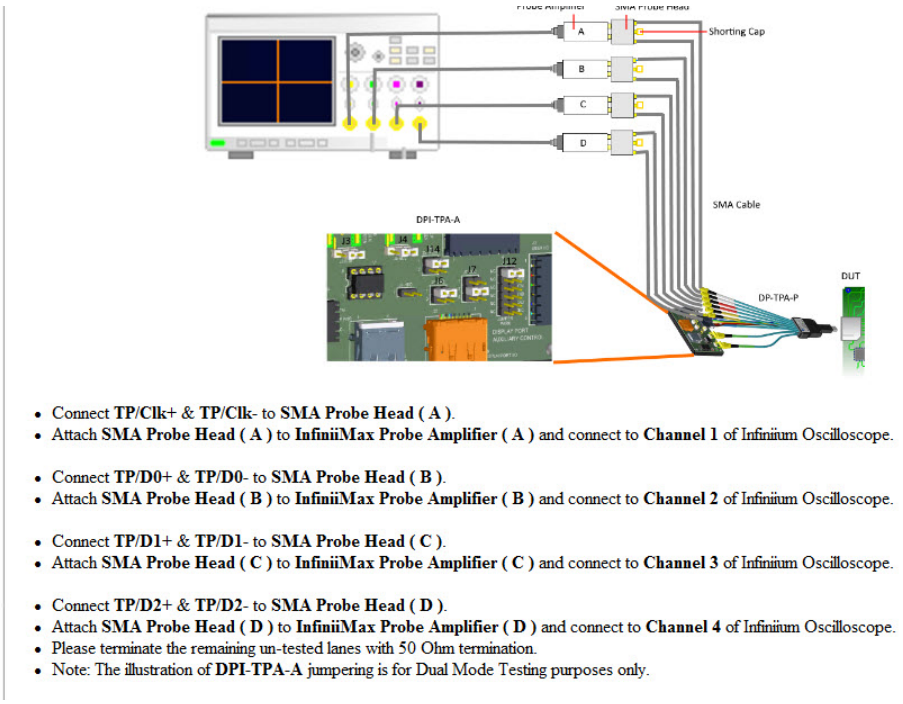
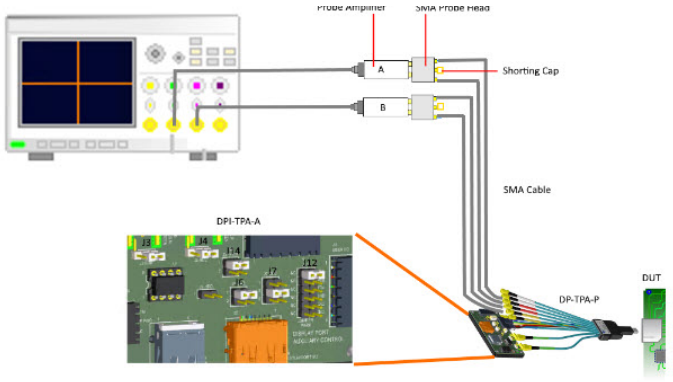


Figure 45 Sample Connection Diagram for a 4-Channel Differential Dual Mode Test



- Connect **TP/Clk+** (Lane A +) & **TP/Clk-** (Lane A -) to **SMA Probe Head (A)**.
- Attach **SMA Probe Head (A)** to **InfiniiMax Probe Amplifier (A)** and connect to **Channel 1** of Infiniium Oscilloscope.

- Connect **TP/Data 0+** (Lane B +) & **TP/Data 0-** (Lane B -) to **SMA Probe Head (B)**.
- Attach **SMA Probe Head (B)** to **InfiniiMax Probe Amplifier (B)** and connect to **undefinedData 0** of Infiniium Oscilloscope.
- Please terminate the remaining un-tested lanes with 50 Ohm termination.
- Note: The illustration of **DPI-TPA-A** jumpering is for Dual Mode Testing purposes only.

Figure 46 Sample Connection Diagram for a 2-Channel Differential Dual Mode Test

Dual Mode TMDS Clock Duty Cycle Test

Test ID

501 – Dual Mode TMDS Clock Duty Cycle (Min)

502 – Dual Mode TMDS Clock Duty Cycle (Max)

Test Overview

The objective of the test is to confirm that the duty cycle of the TMDS Clock waveform of a Source DUT operating in dual mode does not exceed the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_CLOCK

Measurement Procedure

1 Acquire and verify the input TMDS Clock signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Scale the vertical display of the input TMDS Clock signal to optimum value.
   c Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   d Measure the Clock Frequency of the input TMDS Clock signal.
2 Generate FUNC4 signal, which is the differential signal of the TMDS Clock signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery (Explicit Clock, input TMDS Clock signal).
4 Overlap the TMDS Clock signal to fold the differential signal of the TMDS Clock signal.
   a Acquire the signal until 10,000 clock periods are folded.
5 Set up the waveform histogram on the differential signal of the TMDS Clock signal to measure the minimum and maximum duty cycle.
   a The minimum duty cycle is measured as the earliest crossing of the TMDS Clock signal falling edge.
   b The maximum duty cycle is measured as the latest crossing of the TMDS Clock signal falling edge.
6 Report the measurement results.

PASS Condition

PASS: 40% < TMDS_CLOCK duty cycle < 60%.

FAIL: TMDS_CLOCK duty cycle < 40% or TMDS_CLOCK duty cycle > 60%

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.18*

Expected/Observable Results

The measured duty cycle of the dual mode TMDS Clock signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Dual Mode TMDS Clock Jitter Test

Test ID

For 25MHz ≤ TMDS Clock Frequency ≤ 165MHz

- 503 – Dual Mode TMDS Clock Jitter

For TMDS Clock Frequency > 165MHz

- 803 – Dual Mode TMDS Clock Jitter

Test Overview

The objective of the test is to confirm that the TMDS Clock waveform of a Source DUT operating in dual mode does not carry excessive jitter than that defined in the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_CLOCK

Measurement Procedure

1 Acquire and verify the input TMDS Clock signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Scale the vertical display of the input TMDS Clock signal to optimum value.
   c Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   d Measure the Clock Frequency of the input TMDS Clock signal.
2 Generate FUNC4 signal, which is the differential signal of the TMDS Clock signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery (Explicit Clock, input TMDS Clock signal).
4 Overlap the TMDS Clock signal to fold the differential signal of the TMDS Clock signal.
   a Acquire the signal until 400,000 clock periods are folded.
5 Set up the waveform histogram on the differential signal of the TMDS Clock signal to measure the total jitter of the TMDS Clock signal.
6 Report the measurement results.

PASS Condition

For 25MHz ≤ TMDS Clock Frequency ≤ 165MHz

- PASS: Measured TMDS Clock Jitter ≤ 0.20 Tbit and Data Jitter ≤ 0.25 Tbit

For 165MHz < TMDS Clock Frequency ≤ 300MHz

- PASS: Measured TMDS Clock Jitter ≤ 120 ps and Data Jitter ≤ 150 ps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.18*
- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2*

Expected/Observable Results

The measured jitter of the dual mode TMDS Clock signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Dual Mode Eye Diagram Test

Test ID

601, 602, 603 – Dual Mode Eye Diagram Testing

Test Overview

The objective of the test is to evaluate the waveform ensuring that the timing variables and amplitude trajectories of a Source DUT operating in dual mode meets the specification requirements.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_DATA0, TMDS_DATA1, TMDS_DATA2

Measurement Procedure

1 Acquire and verify the input TMDS Clock and data signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Verify the trigger and the amplitude of the input data signal.
   c Scale the vertical display of the input TMDS Clock signal to optimum value.
   d Scale the vertical display of the input data signal to optimum value.
   e Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   f Measure V_{TOP} and V_{BASE} of the input data signal.
   g Measure the Clock Frequency of the input TMDS Clock signal.
2 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery (Explicit First Order PLL, input TMDS Clock signal).
3 Fold the differential signal of the data signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
4 Set up the waveform histogram on the data signal eye diagram to measure the left edge and right edge.
5 Set up the parameter of the Mask Test.
   a Load the Eye mask.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.
   c Run the Eye mask until the 400,000 UI are folded.
6 Check for any signal trajectories entering into the mask.
7 Measure the jitter of the eye diagram using the histogram.
8 Measure the eye height of the eye diagram using the histogram.
9 Measure the peak-to-peak voltage at 0.5UI of the eye diagram using the histogram.

10 Overlap the TMDS Clock Signal to fold the differential signal of the data signal.

a Acquire the signal until 400,000 clock period are folded.

11 Set up the waveform histogram on the differential signal of the TMDS Clock signal to measure the total jitter of the TMDS Clock signal.

12 Report the measurement results.

PASS Condition

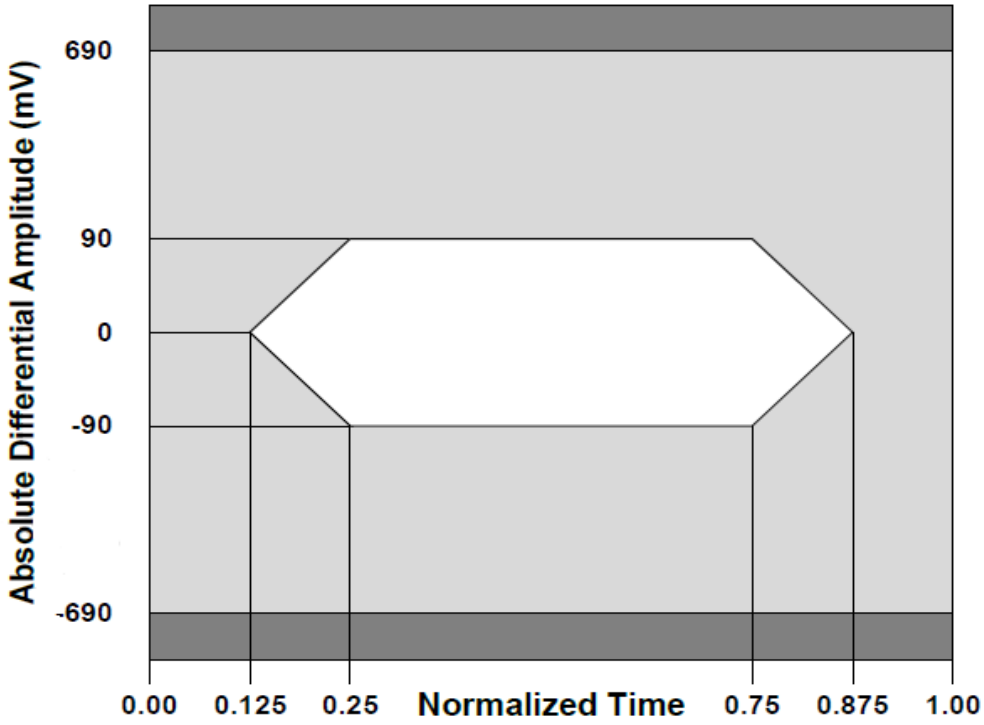


Figure 47 TMDS Data EYE Mask for TMDS Clock Frequencies from 25MHz to 165MHz

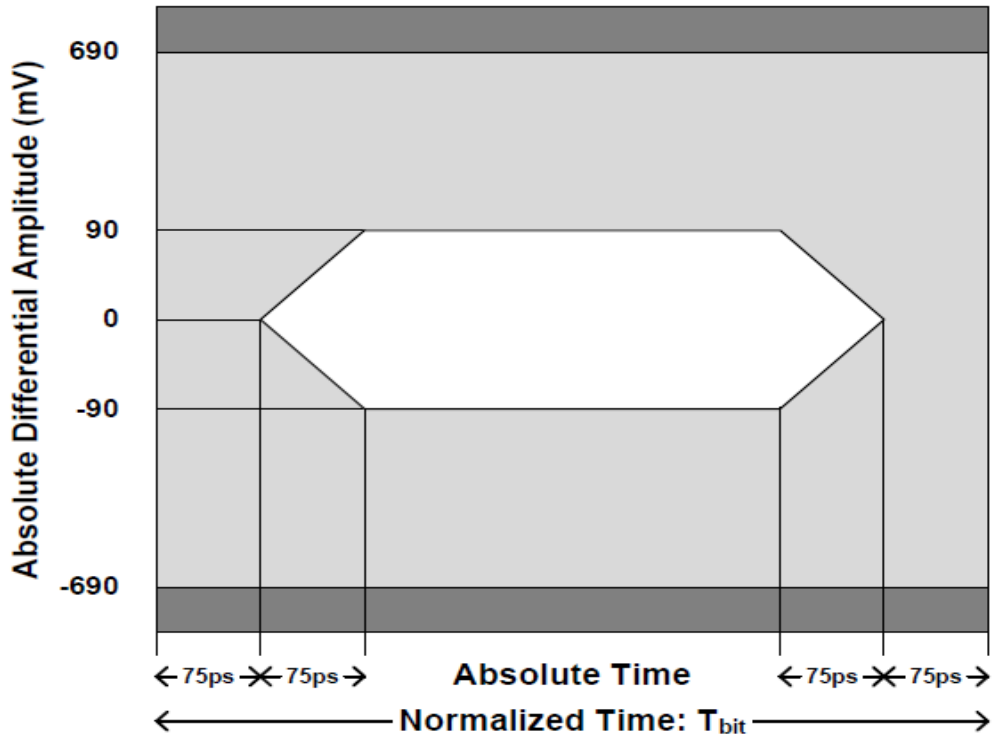


Figure 48 TMDS Data EYE Mask for TMDS Clock Frequencies above 165 MHz

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.19*
- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2, Figure 3-10* (for 25MHz < TMDS Clock Frequency < 165MHz) and *Figure 3-11* (for TMDS Clock Frequency > 165MHz)

Expected/Observable Results

The measured eye diagram for the dual mode data signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Dual Mode Data Jitter Test

Test ID

For 25MHz $\leq$ TMDS Clock Frequency $\leq$ 165MHz

- 611, 612, 613 – Dual Mode Data Jitter

For TMDS Clock Frequency > 165MHz

- 911, 912, 913 – Dual Mode Data Jitter

Test Overview

The objective of the test is to confirm that the data waveform of a Source DUT operating in dual mode does not carry excessive jitter than that defined in the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_DATA0, TMDS_DATA1, TMDS_DATA2

Measurement Procedure

1 Acquire and verify the input TMDS Clock and data signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Verify the trigger and the amplitude of the input data signal.
   c Scale the vertical display of the input TMDS Clock signal to optimum value.
   d Scale the vertical display of the input data signal to optimum value.
   e Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   f Measure V_{TOP} and V_{BASE} of the input data signal.
   g Measure the Clock Frequency of the input TMDS Clock signal.
2 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery (Explicit First Order PLL, input TMDS Clock signal).
3 Fold the differential signal of the data signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
4 Set up the waveform histogram on the data signal eye diagram to measure the left edge and right edge.
5 Set up the parameter of the Mask Test.
   a Load the Eye mask.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.
   c Run the Eye mask until the 400,000 UI are folded.
6 Check for any signal trajectories entering into the mask.
7 Measure the jitter of the eye diagram using the histogram.

8 Measure the eye height of the eye diagram using the histogram.

9 Measure the peak-to-peak voltage at 0.5UI of the eye diagram using the histogram.

10 Overlap the TMDS Clock Signal to fold the differential signal of the data signal.

a Acquire the signal until 400,000 clock period are folded.

11 Set up the waveform histogram on the differential signal of the TMDS Clock signal to measure the total jitter of the TMDS Clock signal.

12 Report the measurement results.

PASS Condition

For 25MHz $\leq$ TMDS Clock Frequency $\leq$ 165MHz

- PASS: Measured TMDS Clock Jitter $\leq$ 0.20 Tbit and Data Jitter $\leq$ 0.25 Tbit

For 165MHz < TMDS Clock Frequency $\leq$ 300MHz

- PASS: Measured TMDS Clock Jitter $\leq$ 120 ps and Data Jitter $\leq$ 150 ps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.19*
- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2*

Expected/Observable Results

The measured jitter of the dual mode data signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Dual Mode Data Peak-Peak Differential Voltage Test

Test ID

811, 812, 813 – Dual Mode Peak-Peak Differential Voltage (Min)

821, 822, 823 – Dual Mode Peak-Peak Differential Voltage (Max)

Test Overview

The objective of the test is to evaluate and confirm that the data waveform ensuring that the timing variables and amplitude trajectories of a Source DUT operating in a dual mode meets the specification requirements.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_DATA0, TMDS_DATA1, TMDS_DATA2

Measurement Procedure

1 Acquire and verify the input TMDS Clock and data signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Verify the trigger and the amplitude of the input data signal.
   c Scale the vertical display of the input TMDS Clock signal to optimum value.
   d Scale the vertical display of the input data signal to optimum value.
   e Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   f Measure V_{TOP} and V_{BASE} of the input data signal.
   g Measure the Clock Frequency of the input TMDS Clock signal.
2 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery (Explicit First Order PLL, input TMDS Clock signal).
3 Fold the differential signal of the data signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
4 Set up the waveform histogram on the data signal eye diagram to measure the left edge and right edge.
5 Set up the parameter of the Mask Test.
   a Load the Eye mask.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.
   c Run the Eye mask until the 400,000 UI are folded.
6 Check for any signal trajectories entering into the mask.
7 Measure the jitter of the eye diagram using the histogram.
8 Measure the eye height of the eye diagram using the histogram.

9 Measure the peak-to-peak voltage at 0.5UI of the eye diagram using the histogram.

10 Overlap the TMDS Clock Signal to fold the differential signal of the data signal.

a Acquire the signal until 400,000 clock period are folded.

11 Set up the waveform histogram on the differential signal of the TMDS Clock signal to measure the total jitter of the TMDS Clock signal.

12 Report the measurement results.

PASS Condition

For all TMDS Clock Frequencies:

- Minimum Peak-Peak Differential Voltage: 180mV
- Maximum Peak-Peak Differential Voltage: 1380mV

Test References

See:

- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2*

Expected/Observable Results

The measured peak-peak differential voltage of the dual mode data signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Dual Mode Inter-Pair Skew Test

Test ID

711 – D0/D1 - Dual Mode Inter Pair Skew Test

712 – D0/D2 - Dual Mode Inter Pair Skew Test

713 – D1/D2 - Dual Mode Inter Pair Skew Test

Test Overview

The objective of the test is to evaluate and confirm that the skew or time delay between differential data lane of a Source DUT operating in a dual mode meets the specification requirements.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_DATA0, TMDS_DATA1, TMDS_DATA2

Measurement Procedure

1 Acquire and verify the input TMDS Clock and data signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Verify the trigger and the amplitude of the input Lane A data signal.
   c Verify the trigger and the amplitude of the input Lane B data signal.
   d Scale the vertical display of the input TMDS Clock signal to optimum value.
   e Scale the vertical display of the input Lane A data signal to optimum value.
   f Scale the vertical display of the input Lane B data signal to optimum value.
   g Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   h Measure V_{TOP} and V_{BASE} of the input Lane A data signal.
   i Measure V_{TOP} and V_{BASE} of the input Lane B data signal.
   j Measure the Clock Frequency of the input TMDS Clock signal.
2 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
3 Set up the parameter of the Inter Pair Skew measurement.
   a Set up two display grids such that each grid displays one test lane data signal.
   b Set up the measurement threshold of each test lane data signal on the Transition Voltage = 0V.
   c Decode the data signal for each test lane.
   d Search the desired pattern from the decoded data signal.

e Measure the time difference between the corresponding edges of both the test lanes using the equation:

$$T_{Transition\_LaneA} - T_{Transition\_LaneB}$$

f Repeat the previous step until you measure 100 edges.

g Calculate the Inter Pair Skew using the equation:

$$\text{Inter Pair Skew} = \{1/\text{Number of Edges}\} \sum |T_{Transition\_LaneA} - T_{Transition\_LaneB}|$$

4 Report the measurement results.

PASS Condition

For all TMDS Clock Frequencies, Inter-Pair Skew $\leq$ 976 ps

Test References

See:

- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2*

Expected/Observable Results

The measured inter pair skew of the dual mode data signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Dual Mode Intra-Pair Skew Test

Test ID

701, 702, 703 – Dual Mode Intra Pair Skew Test

Test Overview

The objective of the test is to evaluate and confirm that the skew or time delay between the respective sides of the differential data lane of a Source DUT operating in a dual mode meets the specification requirements.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_DATA0, TMDS_DATA1, TMDS_DATA2

Measurement Procedure

1 Acquire and verify the input TMDS Clock and data signal:
   - *a* Verify the trigger and the amplitude of the input TMDS Clock signal.
   - *b* Verify the trigger and the amplitude of the input data signal.
   - *c* Scale the vertical display of the input TMDS Clock signal to optimum value.
   - *d* Scale the vertical display of the input data signal to optimum value.
   - *e* Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   - *f* Measure V_{TOP} and V_{BASE} of the input data signal.
   - *g* Measure the Clock Frequency of the input TMDS Clock signal.

2 Set up the parameter of the measurement:
   - *a* Enable measurement of all edges to obtain the statistical values of the measurement.
   - *b* Set up the measurement threshold.

3 Set up the parameter to perform High Level Voltage (V_{High}) and Low Level Voltage (V_{Low}) for each single-ended data signal:
   - *a* Scale the vertical display of the single-ended input data signal to optimum value.
   - *b* Acquire the signal for 100 waveforms.
   - *c* Find V_{High} by measuring the average voltage at 0.6UI to 0.75UI of the High level.
   - *d* Find V_{Low} by measuring the average voltage at 0.6UI to 0.75UI of the Low level.
   - *e* Calculate the Transition Voltage (V_{Trans}) using the equation:

$$V_{Trans} = (V_{High} + V_{Low})/2$$

4 Set up the parameter of the Intra Pair Skew measurement.

a Set up measurement threshold od each single-ended data signal based on the Transition Voltage measured.

b Set up InfiniiScan to trigger on the desired pattern.

c Set up delta time measurement to measure the time difference between the rising edge of the data true signal (D+) and the complement's (D-) falling edge using the equation:

$$D+_{Transition\_High} - D-_{Transition\_Low}$$

d Set up delta time measurement to measure the time difference between the falling edge of the data true signal (D+) and the complement's (D-) falling edge using the equation:

$$D+_{Transition\_Low} - D-_{Transition\_High}$$

e Acquire the signal until you measure 100 edges.

f Calculate the Intra Pair Skew using the equation:

$$\text{Intra Pair Skew} = \{1/\text{Number of Edges}\} \sum \{[(D+_{Transition\_High} - D-_{Transition\_Low}) + (D+_{Transition\_Low} - D-_{Transition\_High})]/2\}$$

5 Report the measurement results.

PASS Condition

For all TMDS Clock Frequencies, Intra-Pair Skew $\leq$ 60 ps

Test References

See:

- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2*

Expected/Observable Results

The measured intra pair skew of the dual mode data signal shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

9 DisplayPort 1.4a Source Tests

Overview

This section describes the normative and informative main link physical layer tests for compliance verification of DisplayPort 1.4a source, sink and cable devices.

Test Point Definition for DisplayPort 1.4a Tests

Five different test points are identified for the physical layer measurement. See Figure 49.

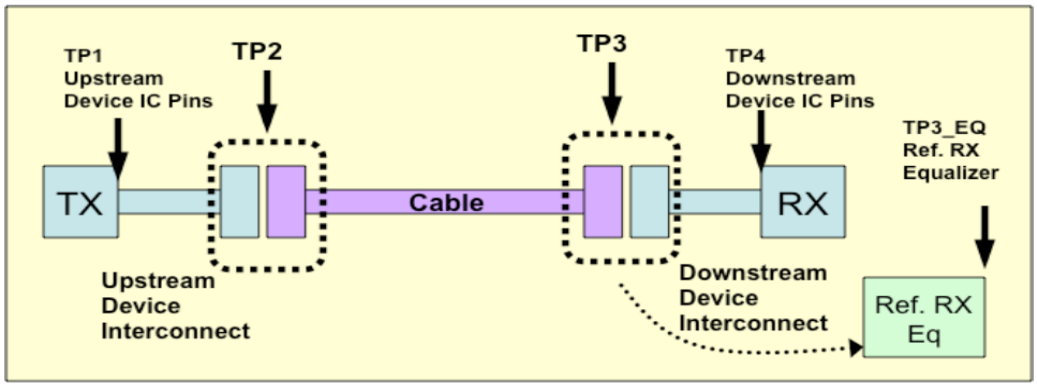


Figure 49 Test Points in a DisplayPort InterConnect System

Table 45 defines the Test Points used for various DisplayPort 1.4a Tests:

Table 45 Test Points for DisplayPort Tests

Test Point	Description
TP1	At the pins of the Transmitter Device
TP2	At the test interface on a test access fixture as close as possible to the DP mated connection to a Source device
TP3	At the test interface on a test access fixture as close as possible to the DP mated connection to a Sink device
TP3_EQ	At TP3, when a defined cable model with equalizer is applied. There are two defined cable models: ▪ Worst Cable Model as defined in VESA DisplayPort 1.4a Standard, ▪ Zero length, zero loss cable. The equalizer is also defined in VESA DisplayPort 1.4a Standard
TP2_CTLE	Receiver Jitter Tolerance calibration and testing interface point of DUT with plug.
TP3_CTLE	At TP3, when a defined HBR3 cable model with CTLE is applied.
TP3_DFE	At TP3, when a defined HBR3 cable model with CTLE and DFE are applied.
TPS4	At the pins of a receiving device

NOTE

Among the patterns that are used at the test points described above, HBR2CPAT pattern is the same as CP2520.
The CP2520 pattern can be further divided into “CP2520.Pattern1”, “CP2520.Pattern2”, or “CP2520.Pattern3”.

The TPS4 pattern is “CP2520.Pattern3” (HBR2CPAT Pattern 3).

Cable Models

The two cable models defined in VESA DisplayPort 1.4a Standard are:

1 Worst Case Cable Model—To achieve the TP3_EQ signal with the worst case cable model:

- Acquire the signal at TP2.
- Embed the TP2 signal with a “worst case” cable model using an InfiniiSim Waveform Transformation Toolset software to emulate the insertion loss as defined in Figure 4-10 of the VESA DisplayPort 1.4a Standard.
  - For Standard DisplayPort: The “*CIC_rev0p6.s4p*” cable model transfer function is used for RBR, HBR and HBR2 whereas the “*Source_100ohms_CIC.sp4*” cable model transfer function is used for HBR3.
  - For USB Type-C – The “*c2dp_90ohms_0psSkew.s4p*” cable model transfer function is used for RBR, HBR and HBR2 whereas “*Source_100ohms_CIC.sp4*” cable model transfer function is used for HBR3.
- Finally, apply the HBR, HBR2 or HBR3 equalization using the Serial Data Equalization software as defined in the VESA DisplayPort 1.4a Standard.

2 Zero Length Cable Model—To achieve the TP3_EQ signal with the zero length cable model:

- Acquire the signal at TP2.
- No cable model is embedded for the Zero Length cable model.
- Finally, apply the HBR, HBR2 or HBR3 equalization using the Serial Data Equalization software as defined in the VESA DisplayPort 1.4a Standard.

Equalization

When equalization is required, use the CTLE (Continuous Time Linear Equalization) transfer function, as given in the VESA DisplayPort 1.4a Standard.

For main link, use the CTLE model or the DFE model with the following transfer function for HBR (2.7 Gbps):

The HBR Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s + \omega_z}{(s + \omega_{p1})(s + \omega_{p2})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{\sqrt{\omega^2 + \omega_z^2}}{\sqrt{\omega^2 + \omega_{p1}^2} \cdot \sqrt{\omega^2 + \omega_{p2}^2}}$$

where

$$\omega_z = 2\pi(0.725 \times 10^9)$$

$$\omega_{p1} = 2\pi(1.35 \times 10^9)$$

$$\omega_{p2} = 2\pi(2.5 \times 10^9)$$

Figure 50 Transfer Function of the CTLE/DFE model for HBR

Table 46 CTLE Model for HBR

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
Gain	1.0	1.0
Zero Frequency	0.725 GHz	0.725 GHz
Pole 1 Frequency	1.35 GHz	1.35 GHz
Pole 2 Frequency	2.5 GHz	2.5 GHz

For main link, use the CTLE model or the DFE model with the following transfer function for HBR2 (5.4 Gbps):

The HBR2 Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})(s+\omega_{p3})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{\sqrt{\omega^2+\omega_z^2}}{\sqrt{\omega^2+\omega_{p1}^2}\cdot\sqrt{\omega^2+\omega_{p2}^2}\cdot\sqrt{\omega^2+\omega_{p3}^2}}$$

where

$\omega z = 2\pi\ (0.64 \times 10^9)$ for upstream device compliance

and

$\omega p1 = 2\pi\ (2.7 \times 10^9)$

$\omega p2 = 2\pi\ (4.5 \times 10^9)$

$\omega p3 = 2\pi\ (13.5 \times 10^9)$

Figure 51 Transfer Function of the CTLE/DFE model for HBR2

Table 47 CTLE Model for HBR2

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
Gain	1.0	1.0
Zero Frequency	0.64 GHz	0.64 GHz
Pole 1 Frequency	2.7 GHz	2.7 GHz
Pole 2 Frequency	4.5 GHz	4.5 GHz
Pole 3 Frequency	13.5 GHz	13.5 GHz

For main link, use the CTLE model or the DFE model with the following transfer function for HBR3 (8.1 Gbps):

For each acquisition, using the appropriate cable model from Table 3-2, the analyzer software sweeps the range of CTLE Transfer Functions as defined in Table 3-4, and then uses the value with the optimal EYE Height (TP3_CTLE_Optimal) for the compliance test result (see Figure 3-3)

$$H(s) = A_{ac} \times \omega_{p2} \times \frac{[s + (A_{dc} / A_{ac}) \times \omega_{p1}]}{(s + \omega_{p1}) \times (s + \omega_{p2})}$$

where:

- A_{ac} is 3.5dB
- A_{dc} is an integer within the range of 0 through -8dB, inclusive, in 1 db steps
- $\omega_{p1} = 3.03\text{GHz}$
- $\omega_{p2} = 5.60\text{GHz}$

Test equipment analyzer software shall store each TP3_CTLE waveform and associated recovered clock waveform to be used in TP3_DFE compliance test evaluation, if needed

Figure 52 Transfer Function of the CTLE/DFE model for HBR3

Table 48 CTLE Model for HBR3

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
AC Gain	3.5 dB	3.5 dB
Pole 1 Frequency	3.03 GHz	3.03 GHz
Pole 2 Frequency	5.60 GHz	5.60 GHz

HBR3 Reference DFE: The HBR3 Reference Equalizer includes a CTLE cascaded with a one-tap adaptive DFE with a coefficient limited to less than 50mV. The DFE behavior is described as:

$$y_k = x_k - d1 sgn(y_{k-1})$$

where, y_k is the DFE differential output voltage, y_k* is the decision function output voltage, x_k is the differential input voltage after CTLE, d1 is the feedback coefficient, k is the UI sample.

A flowchart representing the HBR3 Reference Equalizer is shown in Figure 53.

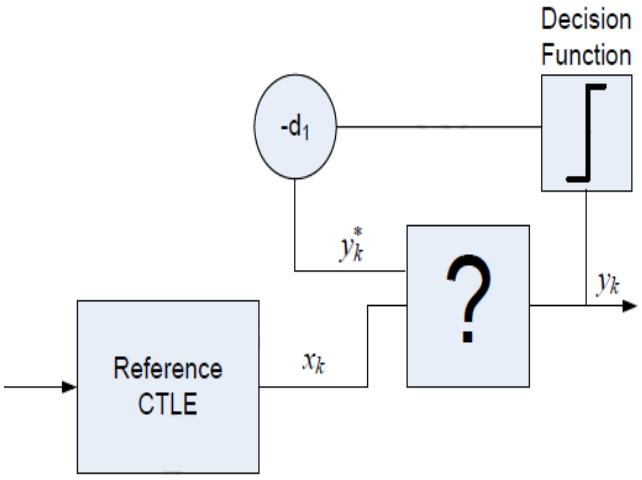


Figure 53 HBR3 Reference Equalizer based on the DFE

Table 49 DFE Model for HBR3

DFE Parameter	Value
Number of Taps	1
DFE Mode	Auto
Eye Width	0.0 UI
Max Tap value	0.050
Min Tap value	0.0

Clock Recovery

When Clock Recovery is required, the clock recovery technique follows the definition of the receiver PLL as defined in Section 3.5.2.5 of the VESA DisplayPort 1.4a Standard. For main link, use the second-order clock recovery function with a closed loop tracking bandwidth and damping factor, with respect to the PRBS7 pattern, as shown in Table 50:

Table 50 Main Link Second-Order Clock Recovery Function

Bit Rate	Bandwidth	Damping Factor
HBR3 (8.1 Gbps)	15 MHZ	1.00
HBR2 (5.4 Gbps)	10 MHz	1.00
HBR (2.7 Gbps)	10 MHz	1.51
RBR (1.62 Gbps)	5.4 MHz	1.51

Test Point Definition for DisplayPort 1.4a Source Tests

Test the Source DUT at Test Point 2 (TP2) as shown in Figure 54. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

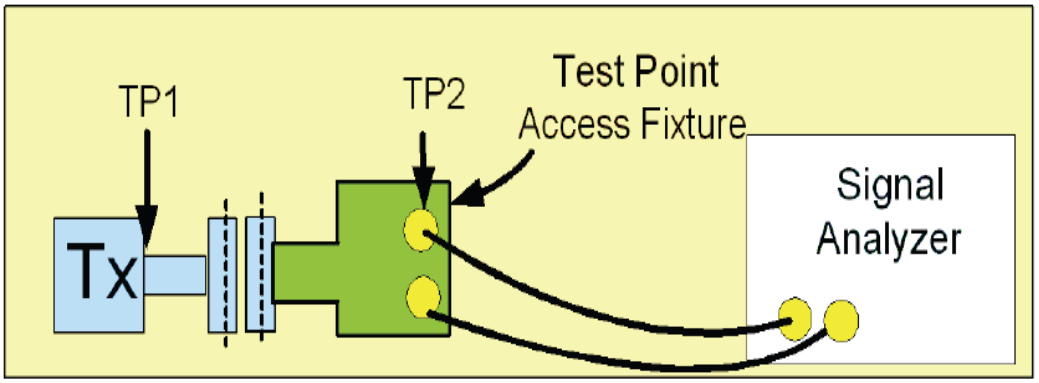


Figure 54 Test Point 2 Connection for DisplayPort 1.4a Source Tests

Table 51 defines the test point fixtures and instruments used for DisplayPort 1.4a Source Tests:

Table 51 Test Point Fixtures and Instruments for DisplayPort 1.4a Source Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-P* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-P* ▪ Luxshare ICT mDP Plug (mDP-TPA-P)** For USB Type-C Connector ▪ N7015A Type-C High-Speed Test Fixture ▪ Wilder Technologies DPC-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.4a Source Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort 1.4a Standards, select the option **1.4a** in the **Test Specification** area.

5 The option **Physical Layer Tests** appears by default in the **Test Selection** area.

6 Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.

7 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

8 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

9 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

10 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

11 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

12 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

13 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

14 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DisplayPort 1.4a Source Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

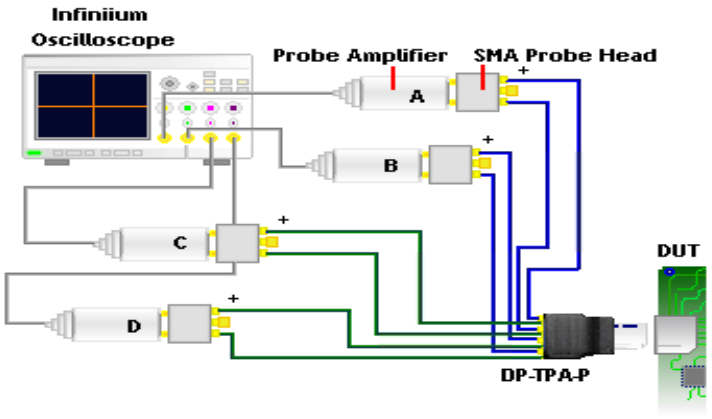


Figure 55 Sample connection diagram for DisplayPort 1.4a Source Tests

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Source tests (either differential or single-ended) to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1. In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.
2. On the **Test Setup** window,
   - *a* Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.
   - *b* In the **DUT Info** area, the **Device Type** is selected as **Source** by default. The **Connector Type** is grayed out.
   - *c* In the **Test Info** area, the **Test Type** is selected as **Differential Tests** by default. Select **Single-Ended Tests** from the drop-down options for the respective tests to appear in the **Select Tests** tab. From the **Data Pattern** drop-down options, select **Standard DP Pattern** or **Arbitrary Pattern**, based on the type of pattern generated.
   - *d* In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.
3. Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1. Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.
2. On the **Connection Setup** window,
   - *a* Select the appropriate option in the **Fixture Type** to indicate where the DUT is connected to.
   - *b* Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.
   - *c* In the **Channel Selection** area, assign appropriate channels to lanes.
3. Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of source tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.4a Source Tests" on page 281 to complete the task flow for DUT setup along with configuring the Compliance Application to run each test.

Source Eye Diagram Test

Test ID

For Standard DP Pattern:

- 1210001, 1210002, 1210003, 1210004 – Eye Diagram Test

For Arbitrary Pattern:

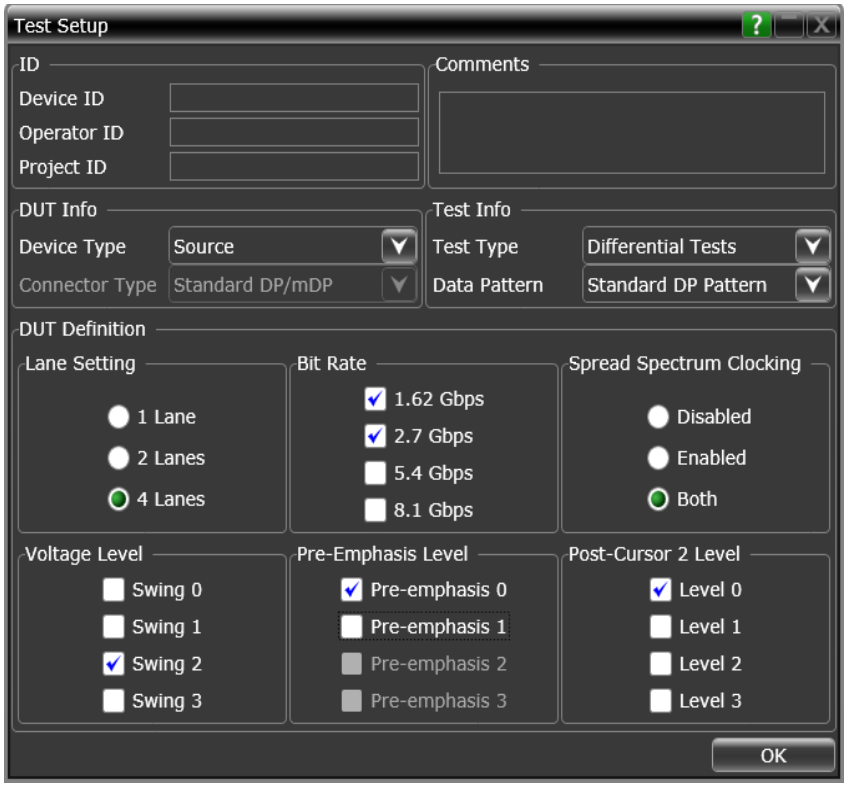
- 1310001, 1310002, 1310003, 1310004 – Eye Diagram Test

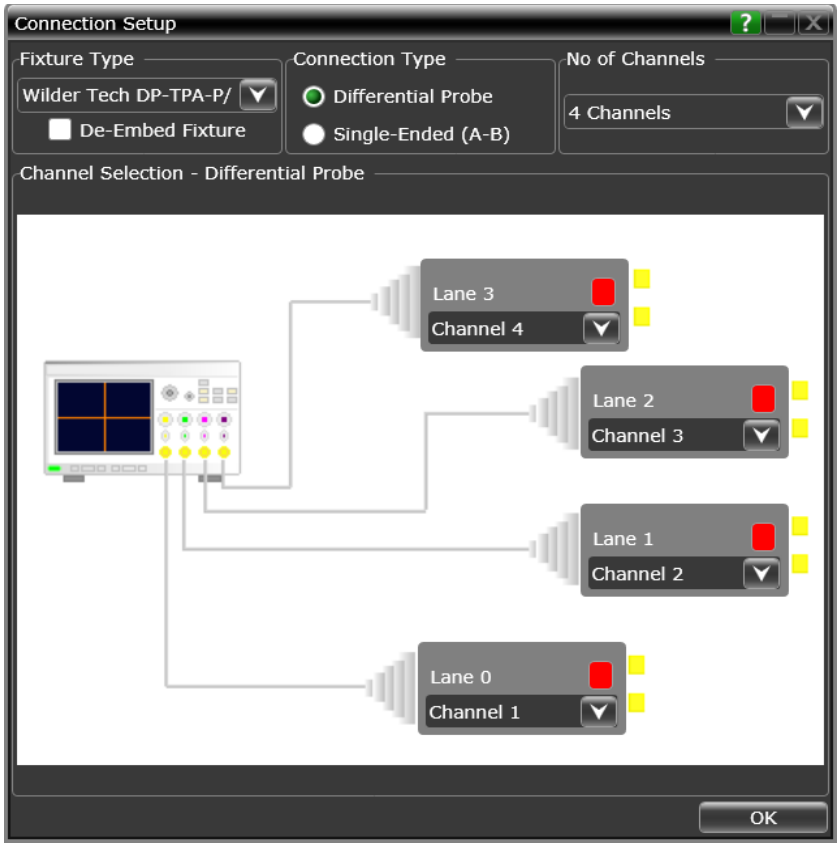
Test Overview

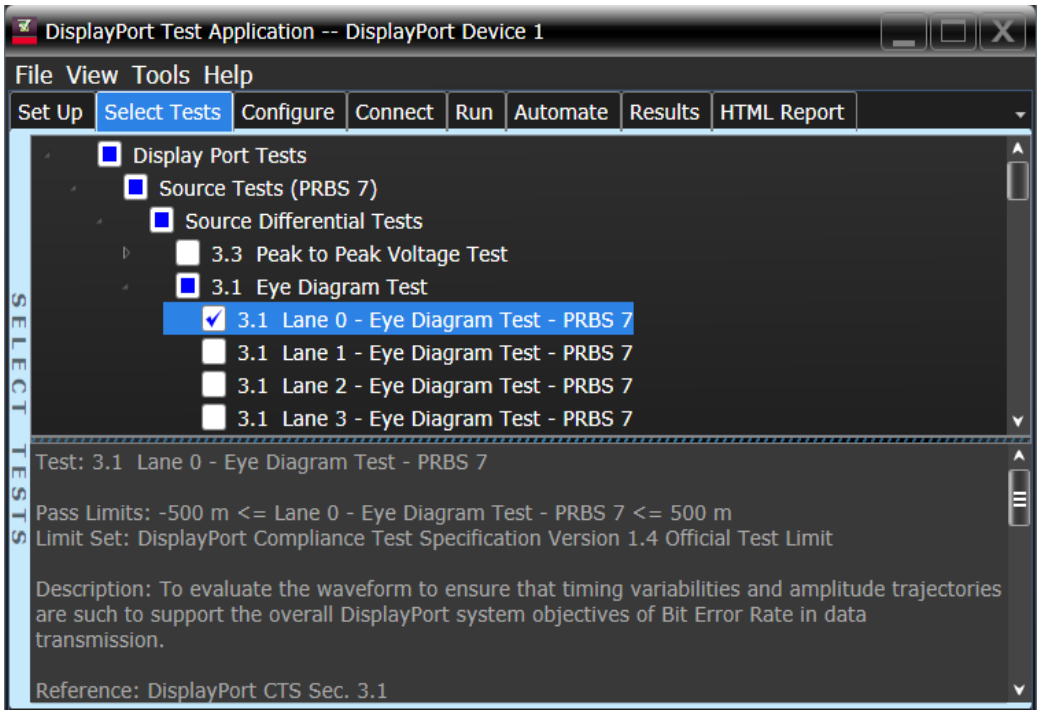
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Measure V_{TOP} and V_{BASE} of the input signal using the pattern folding.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the input signal eye diagram to measure the left edge.
7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 2 million UI are folded.
8 Measure the eye height of the eye diagram using the Histogram.
9 Measure the jitter of the eye diagram using the Histogram.
10 Calculate the eye width based on the measured jitter of the eye diagram.

11 Check for any signal trajectories that may have entered into the mask.

12 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 52 shows the voltage and time coordinates for the mask used in the eye diagram.

Table 52 Eye Diagram Mask Coordinates

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	**High (2.7 Gb/s)**
1	0.127, 0.000	0.210, 0.000
2	0.291, 0.160	0.355, 0.140
3	0.500, 0.200	0.500, 0.175
4	0.709, 0.200	0.645, 0.175
5	0.873, 0.000	0.790, 0.000
6	0.709,-0.200	0.645,-0.175
7	0.500,-0.200	0.500,-0.175
8	0.291,-0.160	0.355,-0.140

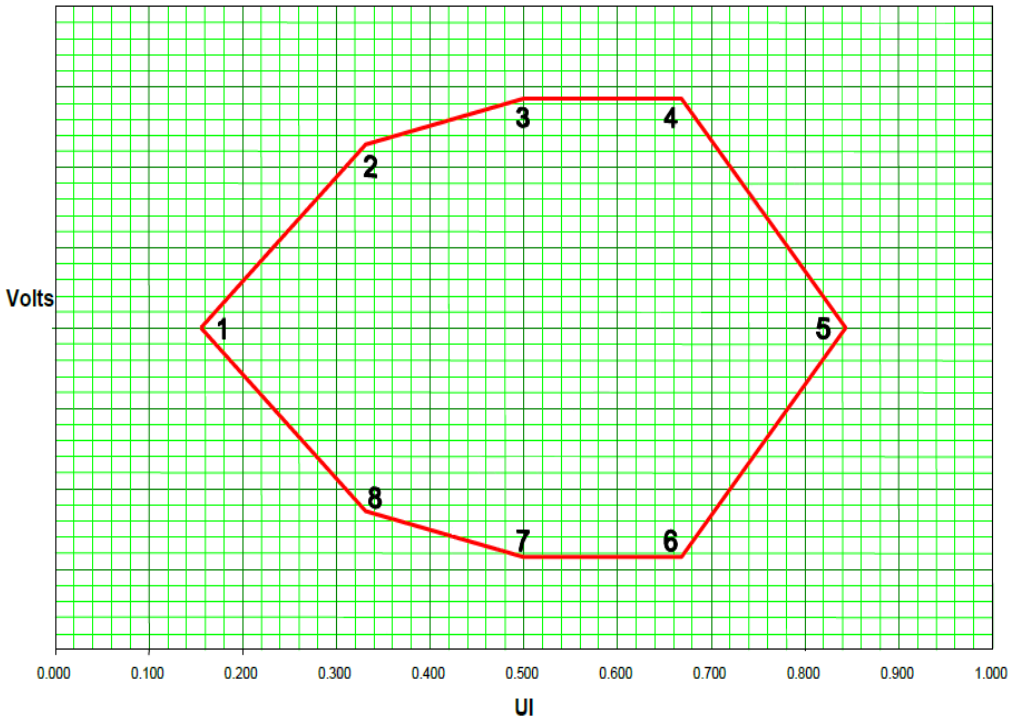


Figure 56 The Source Eye Mask

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.1*
- *VESA DisplayPort Standard Version 1.4a, Section 3.5.2.8.2, Table 3-31 for RBR, Table 3-30 for HBR*

Expected/Observable Results

The measured eye diagram for the source degraded signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test

Test ID

For Standard DP Pattern:

- 1220001, 1220002, 1220003, 1220004 – Total Jitter Test

For Arbitrary Pattern:

- 1320001, 1320002, 1320003, 1320004 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

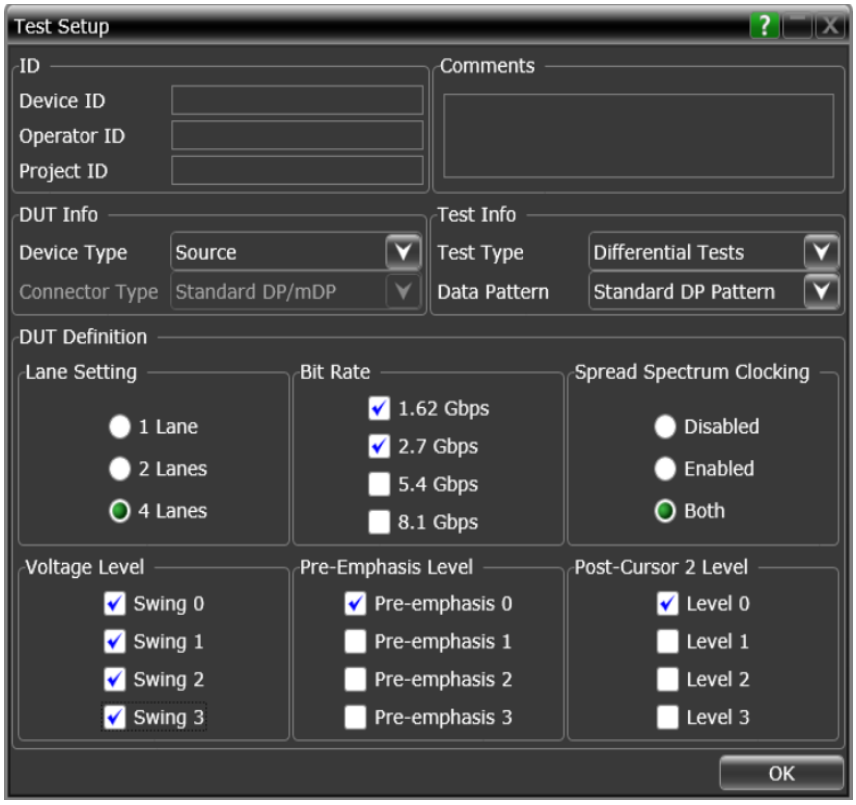
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

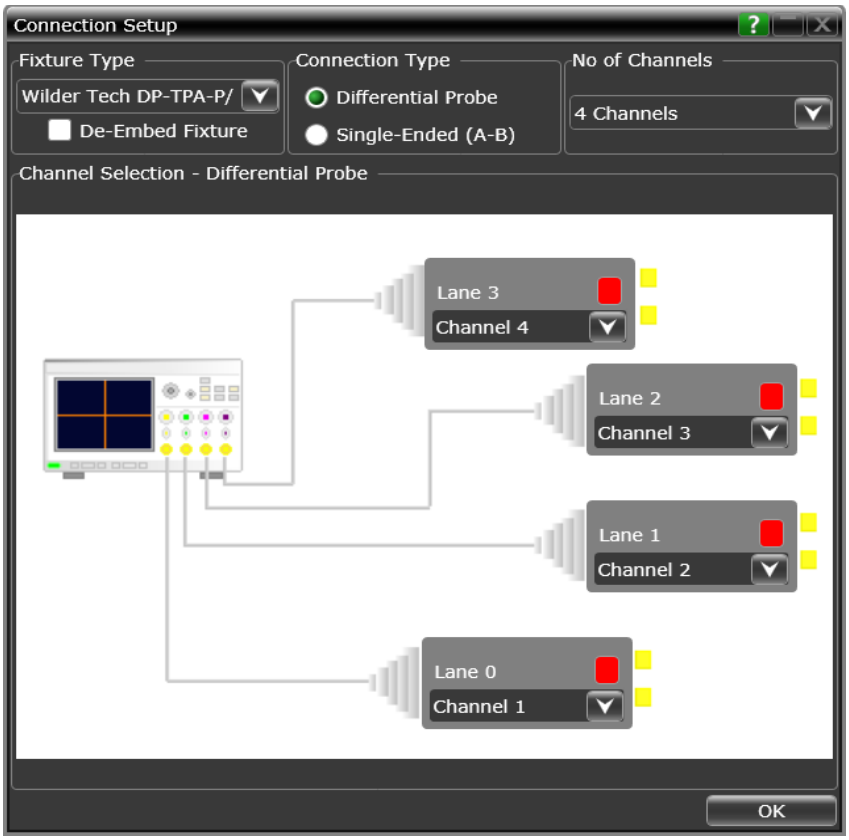
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

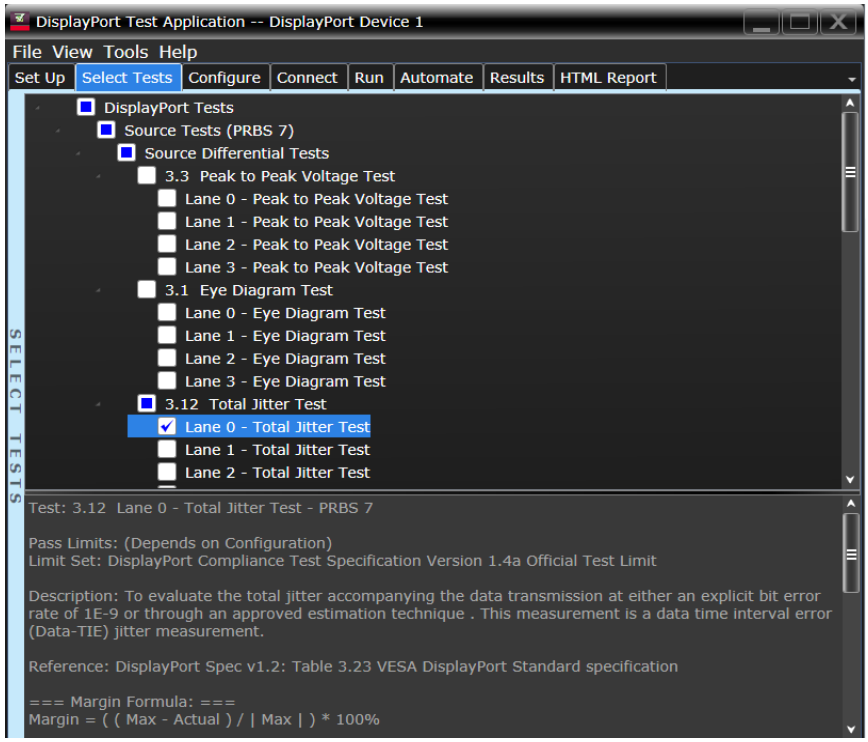
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	All voltage levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 2 million UI edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Report the measurement results.

PASS Condition

Table 53 Total Jitter at Internal and Compliance Points.

	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)	
$A_{p\text{-}pTX}$	0.420 UI
Reduced-bit Rate (1.62 Gb/s per lane)	
$A_{p\text{-}pTX}$	0.270 UI

UI stands for Unit Interval.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.1*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2.7.2*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non-ISI Jitter Test

Test ID

For Standard DP Pattern:

- 1230001, 1230002, 1230003, 1230004 — Non ISI Jitter Test - PRBS7
- 1233001, 1233002, 1233003, 1233004 — Non ISI Jitter Test - TPS4

For Arbitrary Pattern:

- 1330001, 1330002, 1330003, 1330004 — Non ISI Jitter Test

Test Overview

The objective of the test is to evaluate the amount of Non ISI jitter accompanying the data transmission.

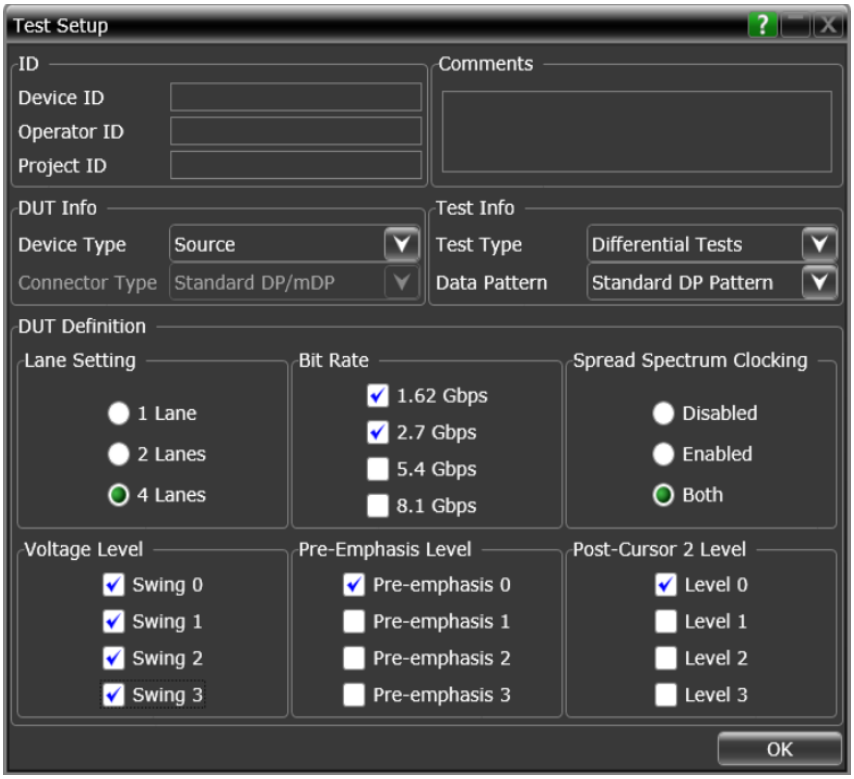
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-6} BER (for HBR3) and 10^{-9} BER (for RBR, HBR, and HBR2) based on the Dual-Dirac Model:

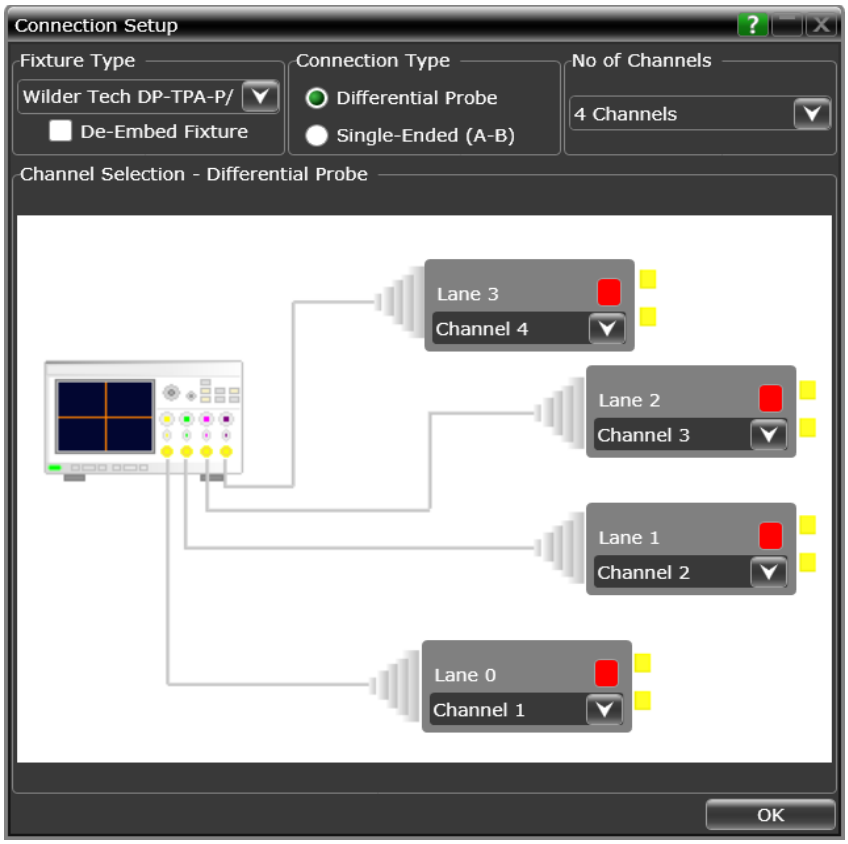
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

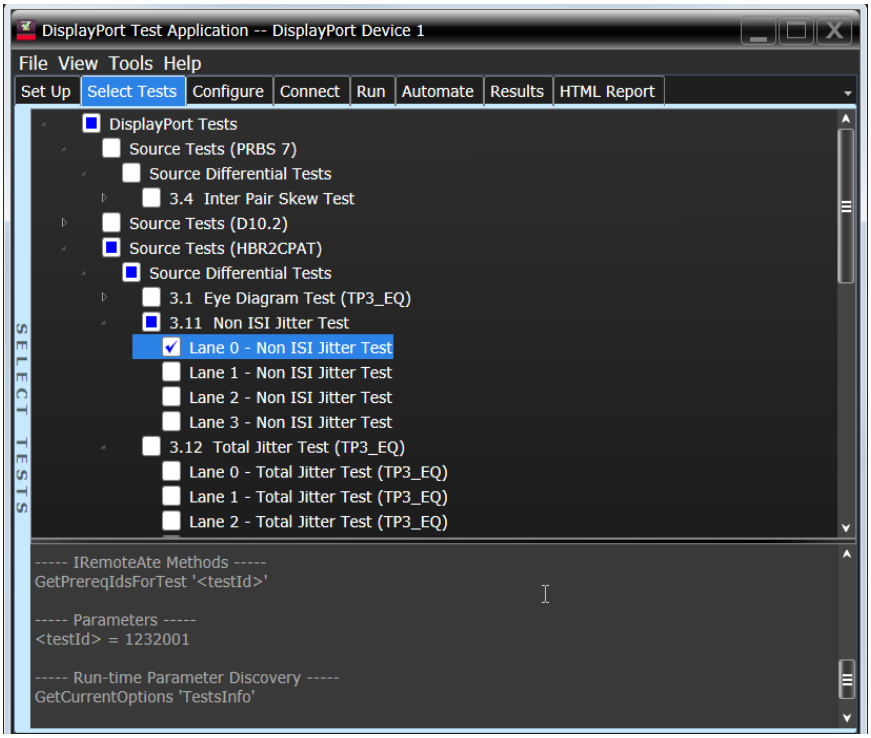
where, DJ is the Deterministic Jitter, RJ is the Random Jitter;
for HBR3 use 10^{-6} BER, for rest of the bit rates use 10^{-9} BER

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR, HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	All voltage levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR - PRBS7 HBR3 - TPS4


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 2 million UI edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Calculate the Non ISI jitter using the following equation:

$$\text{Non ISI Jitter} = \text{TJ} - \text{ISI}$$

7 Report the measurement results.

PASS Condition

Table 54 Non-ISI Jitter at Internal and Compliance Points

	Transmitter Connector (TP2)
Reduced-bit Rate (1.62 Gb/s per lane)-PRBS7	
$A_{p\text{-}p\ TX}$	0.170 UI (DP 1.4a)
High-bit Rate (2.7 Gb/s per lane)-PRBS7	
$A_{p\text{-}p\ TX}$	0.276 UI
High-bit Rate 3 (8.1 Gb/s per lane)-TPS4	
$A_{p\text{-}p\ TX}$	0.230 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.9*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2.7.2, Table 3-23*

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Pre-Emphasis Level Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1261001, 1261002, 1261003, 1261004 – Non Pre-Emphasis Level Test (Swing 1/Swing 0)
- 1262001, 1262002, 1262003, 1262004 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263001, 1263002, 1263003, 1263004 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

For Standard DP Pattern (HBR2 and HBR3):

- 1264101, 1264102, 1264103, 1264104 – Non Pre-Emphasis Level Test (Swing 2/Swing 0)
- 1262101, 1262102, 1262103, 1262104 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263101, 1263102, 1263103, 1263104 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

For Arbitrary Pattern:

- 1364101, 1364102, 1364103, 1364104 – Non Pre-Emphasis Level Test (Swing 2/Swing 0)
- 1362101, 1362102, 1362103, 1362104 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1363101, 1363102, 1363103, 1363104 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

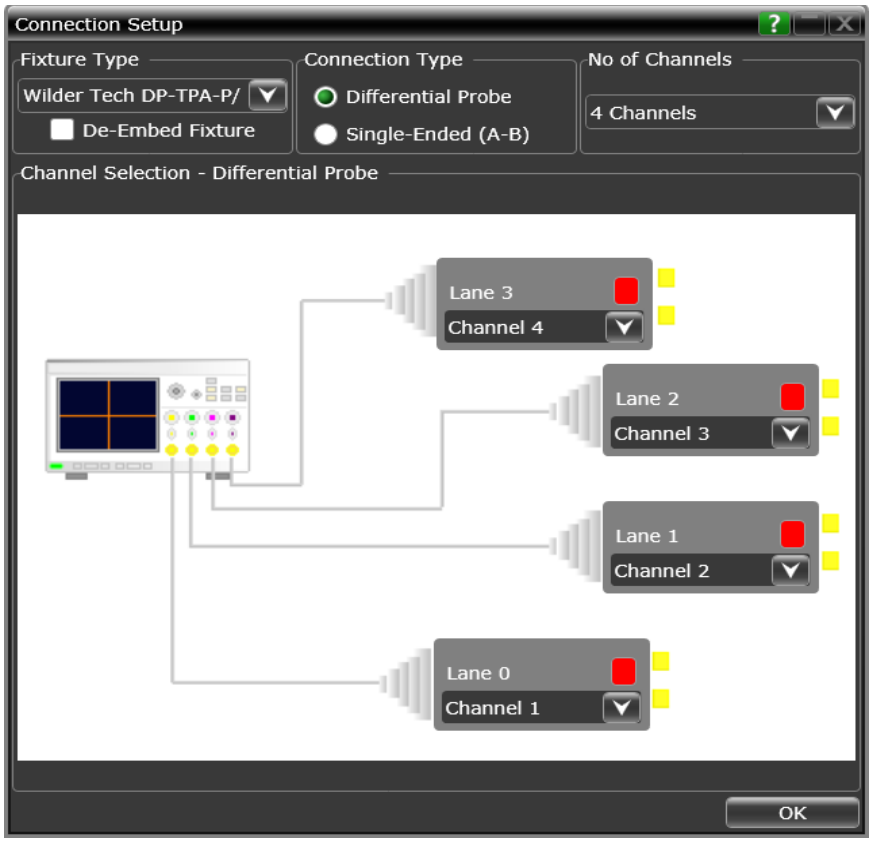
Test Overview

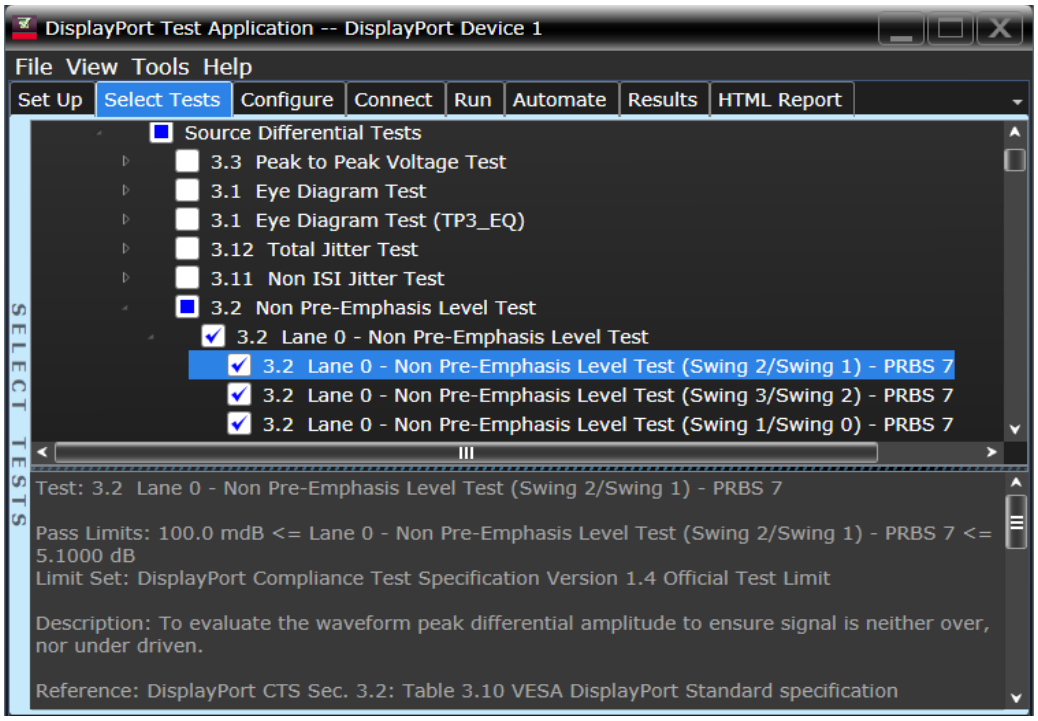
The objective of this test is to ensure that the system budget elements are obeyed and to ensure that the level settings are monotonic so that the sink relies on the source to incrementally increase upon request by the sink.

Test Conditions for Non Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR and HBR
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For Voltage Level A with no pre-emphasis level:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

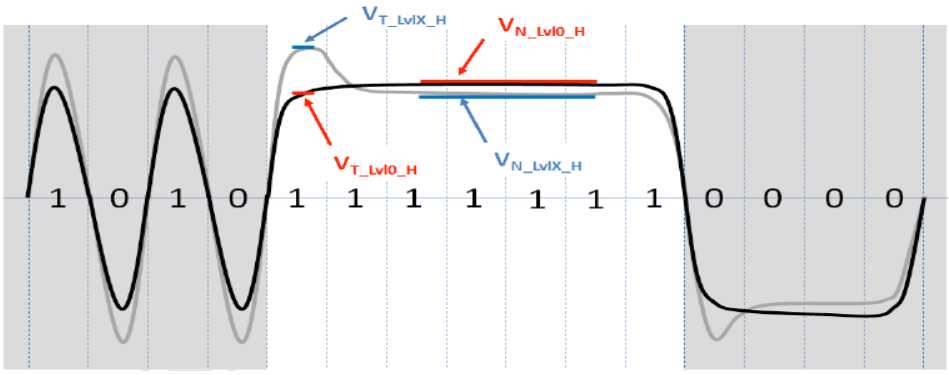


Figure 57 High Voltage measurement for RBR and HBR

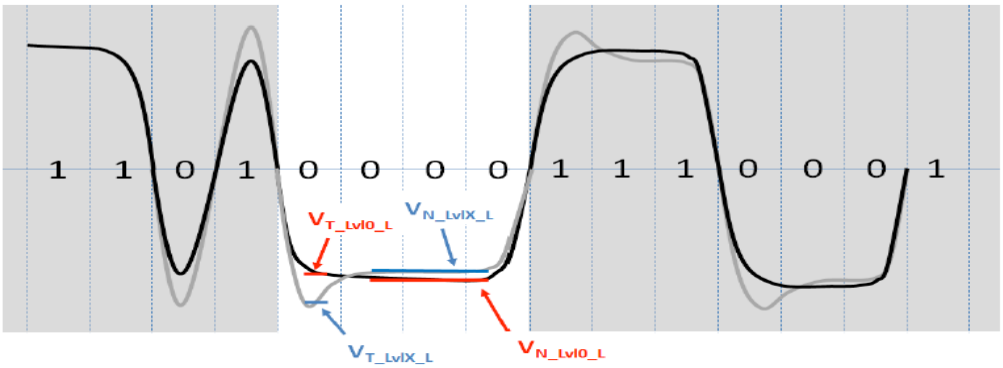


Figure 58 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR3 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted zeros of the pattern.

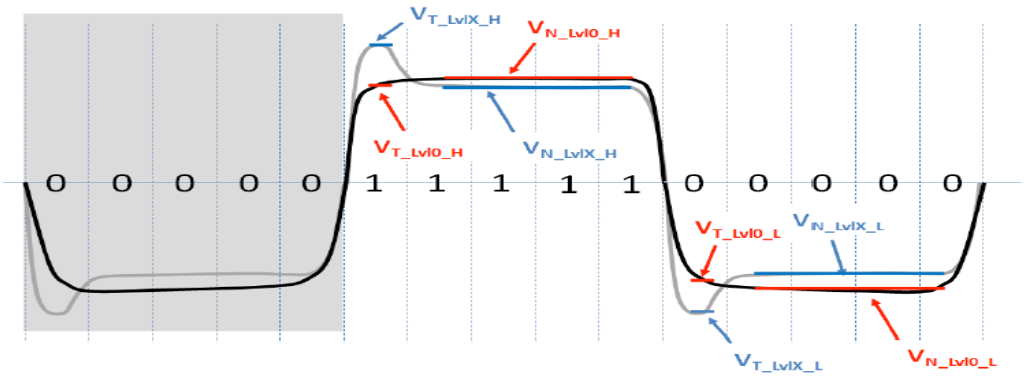


Figure 59 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_Lvl0\_PP} = V_{T\_Lvl0\_H} - V_{T\_Lvl0\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_Lvl0\_PP} = V_{N\_Lvl0\_H} - V_{N\_Lvl0\_L}$$

2 Repeat Step 1 for Voltage Level B with no pre-emphasis level.

3 Calculate the non pre-emphasis level output voltage ratio using the equation:

Non Pre-Emphasis Level = $20 * \text{Log}_{10}[\text{Voltage Level A } V_{N\_Lvl0\_PP} / \text{Voltage Level B } V_{N\_Lvl0\_PP}]$

4 Report the measurement results.

PASS Condition

For each level setting testes, the following equation should be used:

$\text{Resultant} = 20 * \text{Log}_{10}[\text{Voltage}_{\text{Peak-Peak\_LevelA}} / \text{Voltage}_{\text{Peak-Peak\_LevelB}}]$

Table 55 Compared Levels

Measurement#	$\text{Voltage}_{\text{Peak-Peak\_LevelA}}$	$\text{Voltage}_{\text{Peak-Peak\_LevelB}}$
RBR & HBR		
1	Level 1 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)
2	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
3*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)
* if device optionally capable of Level 3		

The resultants specifications are as identified below:

Measurement 1: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 2: 0.1 dB ≤ Resultant ≤ 5.1 dB

Measurement 3: 0.8 dB ≤ Resultant ≤ 6.0 dB

Table 56 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}OUTPUT\text{-}RATIO\_RBR\_HBR}$*	Ratio of Output Voltage Level 1/Level 0	0.8	-	6.0	dB	Measured on non-transition bits at Pre-emphasis level 0 setting. Support for Voltage Level 3 is optional.
	Ratio of Output Voltage Level 2/Level 1	0.1	-	5.1	dB	
	Ratio of Output Voltage Level 3/Level 2	0.8	-	6.0	dB	

* Earlier versions of DisplayPort have the Main-Link DPTX output voltage ratios to ensure that the DPTX supports the required range of output voltage levels. For HBR2 and higher, you need not test or specify exclusively because the compliance test point is moved to TP3_EQ. So, the ratio of output voltage levels is removed from the table above for HBR2 and above.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.2*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-22*

Expected/Observable Results

The measured output voltage level ratio of the non pre-emphasis level test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Pre-Emphasis Level Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1270001, 1270002, 1270003, 1270004 – Pre-Emphasis Level Test

For Standard DP Pattern (HBR2 and HBR3):

- 1270501, 1270502, 1270503, 1270504 – Pre-Emphasis Level Test

For Arbitrary Pattern:

- 1370501, 1370502, 1370503, 1370504 – Pre-Emphasis Level Test

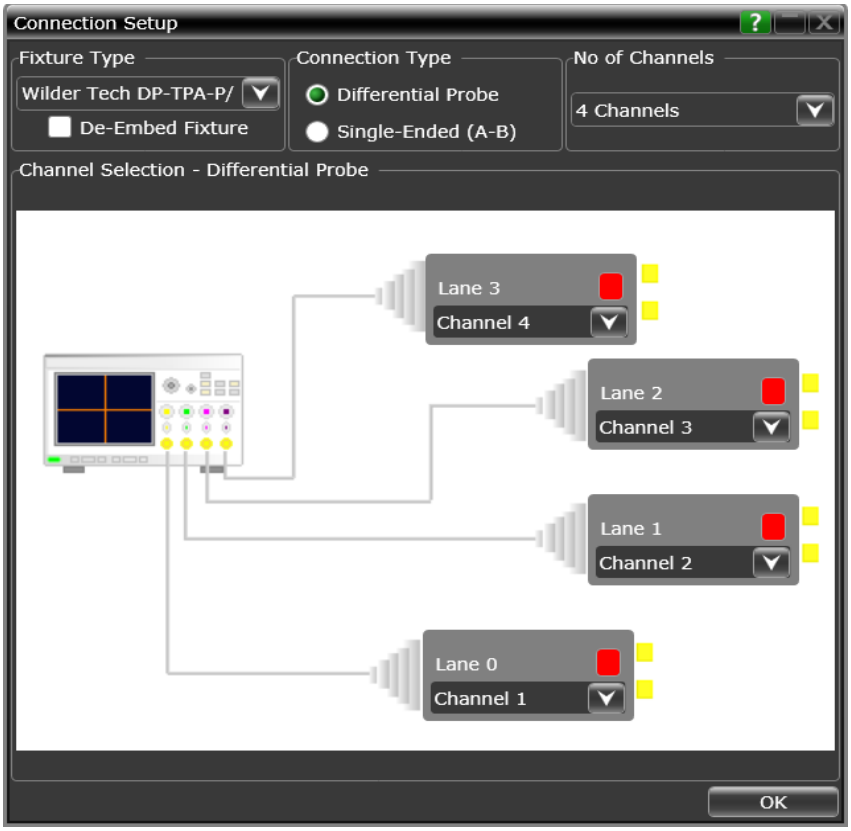
Test Overview

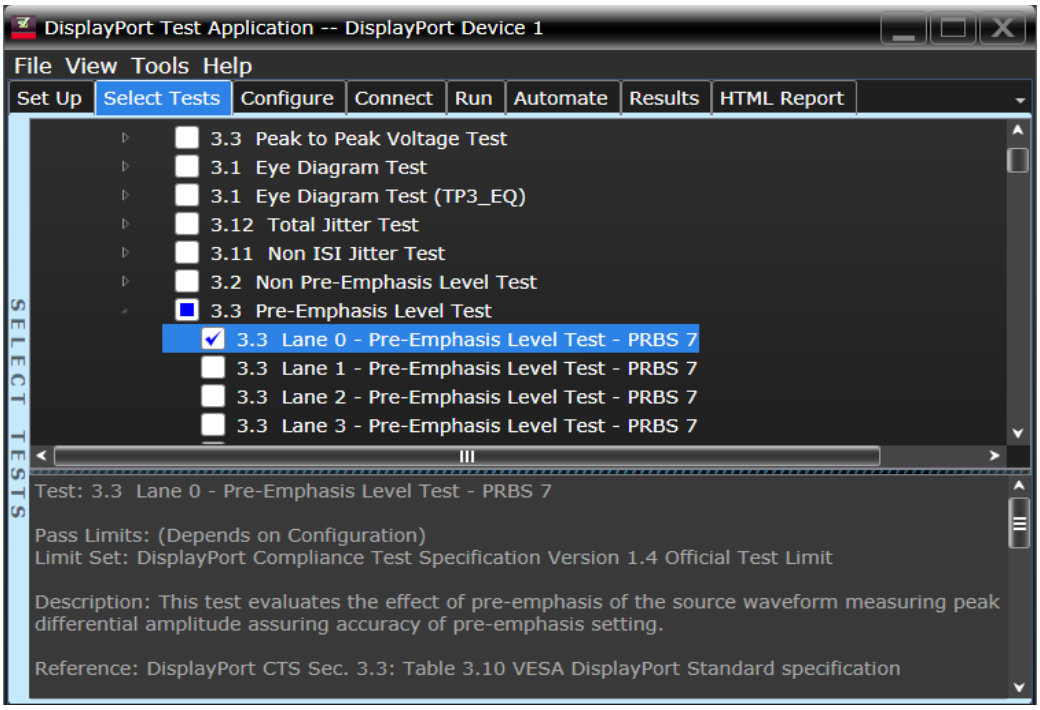
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings.

Test Conditions for Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR and HBR
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.4a Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given Voltage Level and a Pre-Emphasis Level X:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

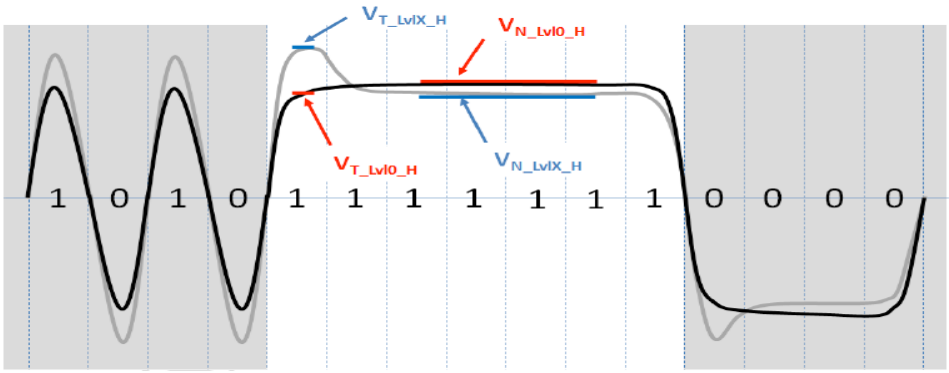


Figure 60 High Voltage measurement for RBR and HBR

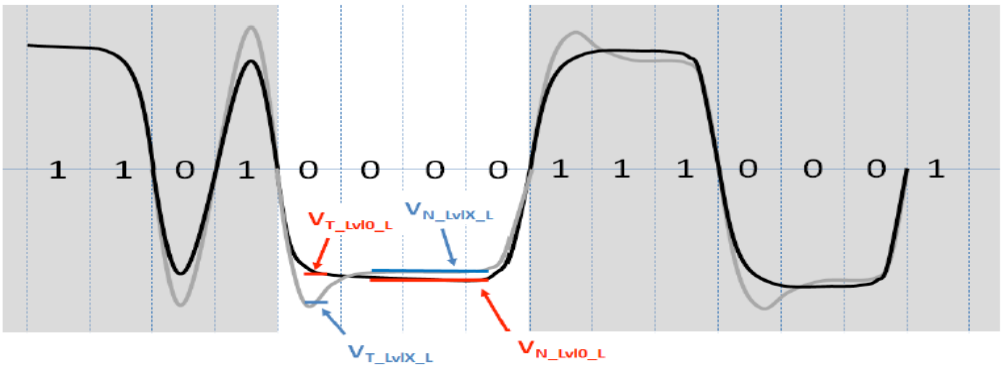


Figure 61 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR3 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted zeros of the pattern.

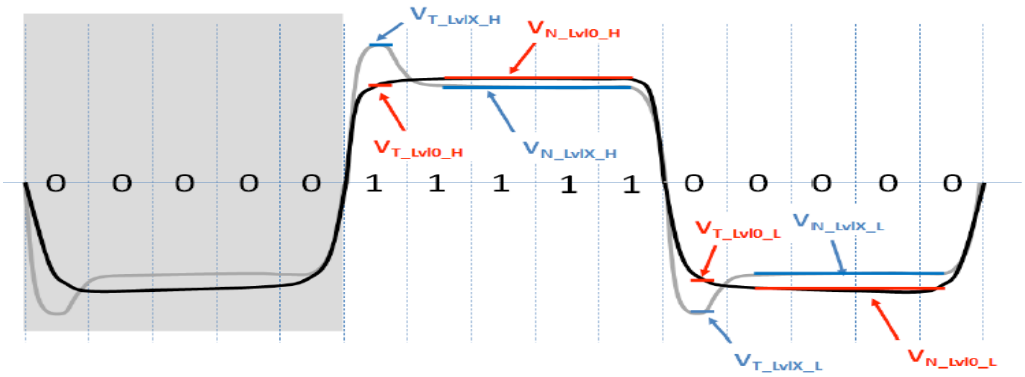


Figure 62 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

l Calculate the pre-emphasis level using the equation:

$$\text{Pre-Emphasis}_{LvlX} = 20 * \text{Log}_{10}[V_{T\_LvlX\_PP} / V_{N\_LvlX\_PP}]$$

2 For Pre-Emphasis Level 0 (no pre-emphasis level), the result for $\text{Pre-Emphasis}_{Lvl0}$ is compared with the maximum pre-emphasis disabled limit.

3 Repeat Step 1 for the next Pre-Emphasis level and for each Pre-Emphasis levels, compare the pre-emphasis delta with the pre-emphasis delta limits.

4 Calculate the pre-emphasis delta using the equation:

$$\text{Pre-Emphasis Delta (Level 1 vs Level 0)} = \text{Pre-Emphasis}_{Lvl1} - \text{Pre-Emphasis}_{Lvl0}$$

$$\text{Pre-Emphasis Delta (Level 2 vs Level 1)} = \text{Pre-Emphasis}_{Lvl2} - \text{Pre-Emphasis}_{Lvl1}$$

$$\text{Pre-Emphasis Delta (Level 3 vs Level 2)} = \text{Pre-Emphasis}_{Lvl3} - \text{Pre-Emphasis}_{Lvl2}$$

5 Report the measurement results.

PASS Condition

Pre-emphasis values for the Level 0 (OFF) state (Normative)

Level 0 (OFF) Pre-emphasis measurement:

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl0\_PP} / \text{Voltage}_{N\_Lvl0\_PP}]$ for all supported levels.

Level 0 (OFF) Pre-emphasis Measurement condition: +0.25 dB $\geq$ Resultant

Pre-emphasis Delta values for:

a Level 1 vs. Level 0 Pre-emphasis settings (NORMATIVE)

b Level 2 vs. Level 1 Pre-emphasis settings (NORMATIVE)

c Level 3 vs. Level 2 Pre-emphasis settings (NORMATIVE)

Pre-emphasis Delta measurements:

- Level 1 vs. Level 0

Resultant = 20 * Log [$Voltage_{T\_Lvl1\_PP}$ / $Voltage_{N\_Lvl1\_PP}$] - 20 * Log [$Voltage_{T\_Lvl0\_PP}$ / $Voltage_{N\_Lvl0\_PP}$] for Voltage Swing Levels 0, 1 and 2.

- Level 2 vs. Level 1

Resultant = 20 * Log [$Voltage_{T\_Lvl2\_PP}$ / $Voltage_{N\_Lvl2\_PP}$] - 20 * Log [$Voltage_{T\_Lvl1\_PP}$ / $Voltage_{N\_Lvl1\_PP}$] for Voltage Swing Levels 0 and 1.

- Level 3 vs. Level 2

Resultant = 20 * Log [$Voltage_{T\_Lvl3\_PP}$ / $Voltage_{N\_Lvl3\_PP}$] - 20 * Log [$Voltage_{T\_Lvl2\_PP}$ / $Voltage_{N\_Lvl2\_PP}$] for Voltage Swing Level 0, if supported.

Table 57 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX-PREEMP-OFF}$	Maximum Pre-emphasis when disabled	-	-	0.25	dB	Pre-emphasis Level 0 setting must not show any pre-emphasis at TP2 to prevent link training issues.
$V_{TX-PREEMP-DELTA}$	Delta of Pre-emphasis Level 1 vs. Level 0	2	-	-	dB	Applies to all valid voltage settings. Measured at Pre-emphasis Post Cursor2 Level 0. Support for Pre-emphasis Level 3 is optional.
	Delta of Pre-emphasis Level 2 vs. Level 1	1.6	-	-	dB	
	Delta of Pre-emphasis Level 3 vs. Level 2	1.6	-	-	dB	

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.3*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-22*

Expected/Observable Results

The measured pre-emphasis level or pre-emphasis delta for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Transition Voltage Range Measurement Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1272001, 1272002, 1272003, 1272004 – Non Transition Voltage Range Measurement (Swing 0)
- 1273001, 1273002, 1273003, 1273004 – Non Transition Voltage Range Measurement (Swing 1)
- 1274001, 1274002, 1274003, 1274004 – Non Transition Voltage Range Measurement (Swing 2)

For Standard DP Pattern (HBR2 and HBR3):

- 1272101, 1272102, 1272103, 1272104 – Non Transition Voltage Range Measurement (Swing 0)
- 1273101, 1273102, 1273103, 1273104 – Non Transition Voltage Range Measurement (Swing 1)
- 1274101, 1274102, 1274103, 1274104 – Non Transition Voltage Range Measurement (Swing 2)

For Arbitrary Pattern:

- 1372101, 1372102, 1372103, 1372104 – Non Transition Voltage Range Measurement (Swing 0)
- 1373101, 1373102, 1373103, 1373104 – Non Transition Voltage Range Measurement (Swing 1)
- 1374101, 1374102, 1374103, 1374104 – Non Transition Voltage Range Measurement (Swing 2)

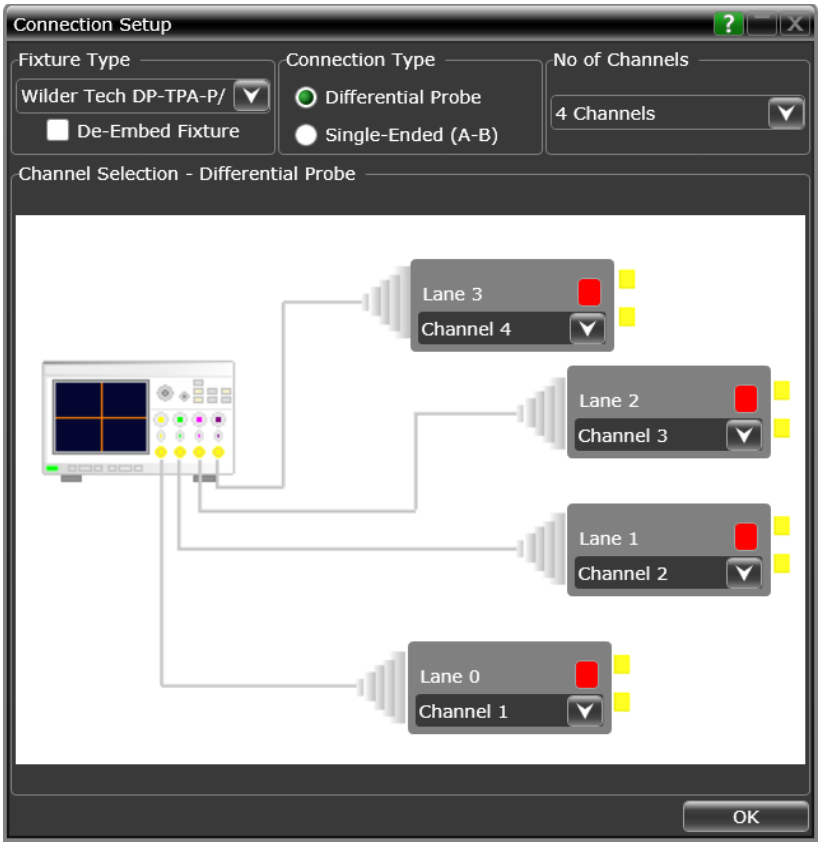
Test Overview

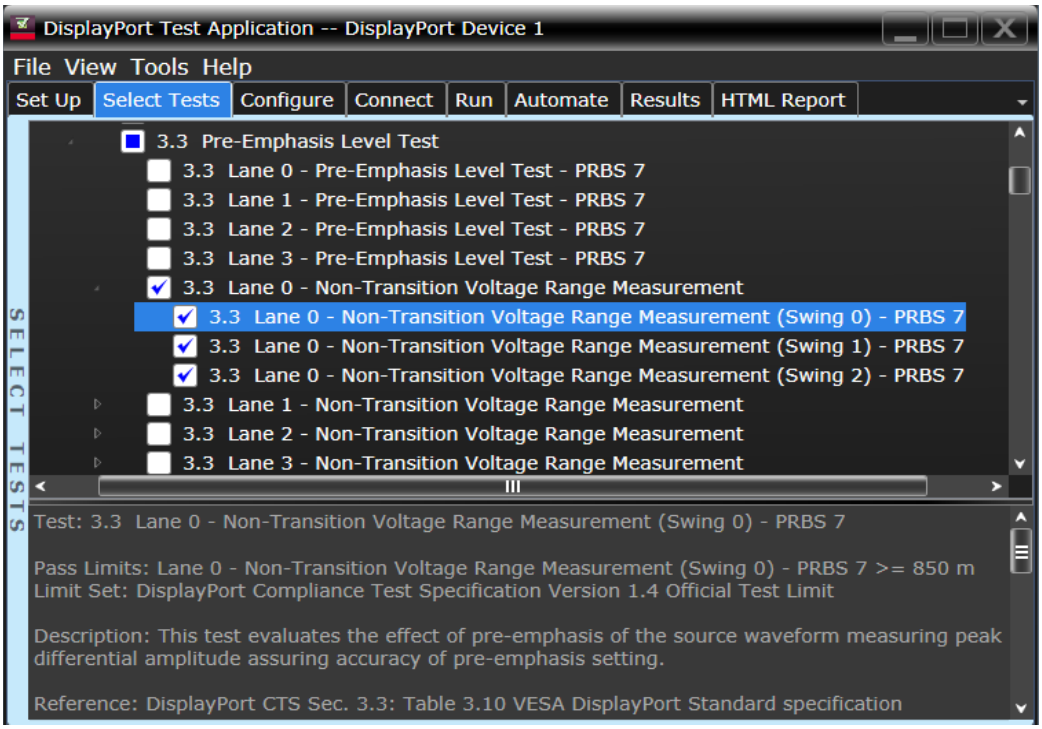
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings. Comparisons are also made for the Level 0 transition state as well as non-transition levels.

Test Conditions for Non-Transition Voltage Range Measurement Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.4a Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given Voltage Level, repeat the following steps for all pre-emphasis levels subjected to constraints specified in Table 3-1 of the VESA DisplayPort 1.4a Standard:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.

- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6th bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4th bit of the four successive transmitted zeros of the pattern.

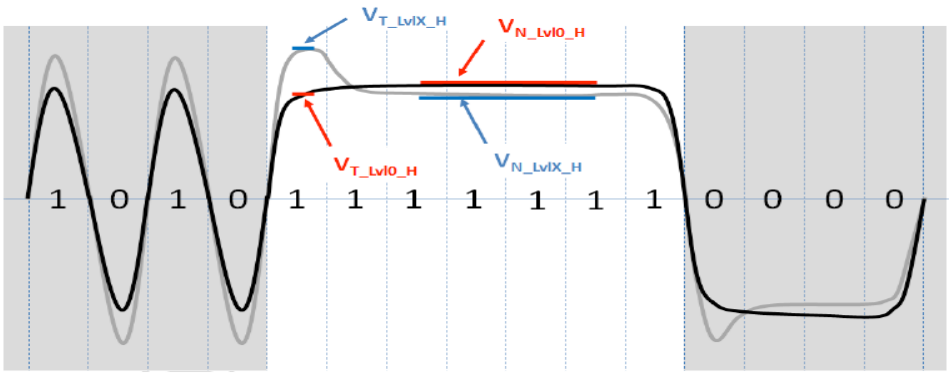


Figure 63 High Voltage measurement for RBR and HBR

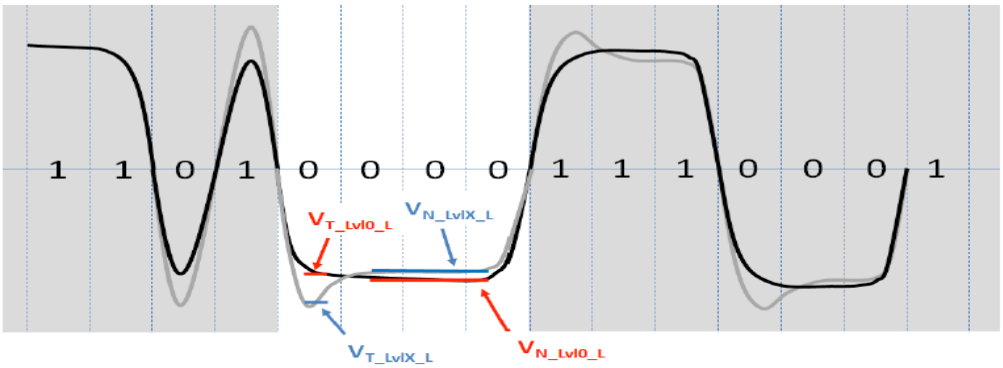


Figure 64 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR3 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

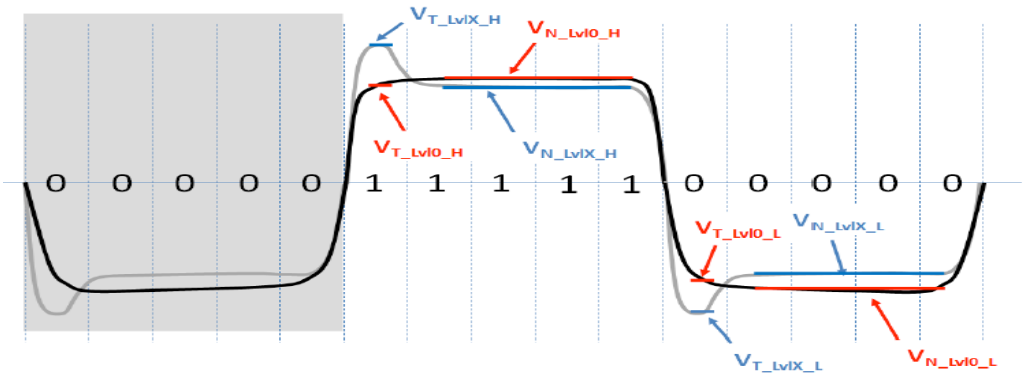


Figure 65 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

2 Calculate the non transition voltage range using the equation:

$$\text{Non Transition Voltage Range} = \text{Minimum } [(V_{N\_LvlX\_PP}) / (V_{N\_Lvl0\_PP})]$$

where, $V_{N\_LvlX\_PP}$) refers to all supported pre-emphasis levels (Level1, Level2, Level3 and so on up to Level X).

3 Report the measurement results.

PASS Condition

Non-Transition Voltage Range Measurements

For Level 2 voltage setting: Resultant > 0.708 OR 20*log(Resultant) > -3dB

For Level 1 voltage setting: Resultant > 0.708 OR 20*log(Resultant) > -3dB

For Level 0 voltage setting: Resultant > 0.85 OR 20*log(Resultant) > -1.4dB

Table 58 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX-DIFF\_REDUCTION}$	Non-transition reduction Output Voltage Level 2	-	-	3	dB	$V_{TX-DIFF}$ at each non-zero nominal pre-emphasis level must not be lower than the specified amount less than $V_{TX-DIFF}$ at the zero nominal pre-emphasis level.
	Non-transition reduction Output Voltage Level 1	-	-	3	dB	
	Non-transition reduction Output Voltage Level 0	-	-	1.4	dB	

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.3*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-22*

Expected/Observable Results

The measured output voltage level reduction of the non transition bit for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Peak to Peak Voltage Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1266001, 1266002, 1266003, 1266004 – Peak to Peak Voltage Test

For Standard DP Pattern (HBR2 and HBR3):

- 1266101, 1266102, 1266103, 1266104 – Peak to Peak Voltage Test

For Arbitrary Pattern:

- 1366101, 1366102, 1366103, 1366104 – Peak to Peak Voltage Test

Test Overview

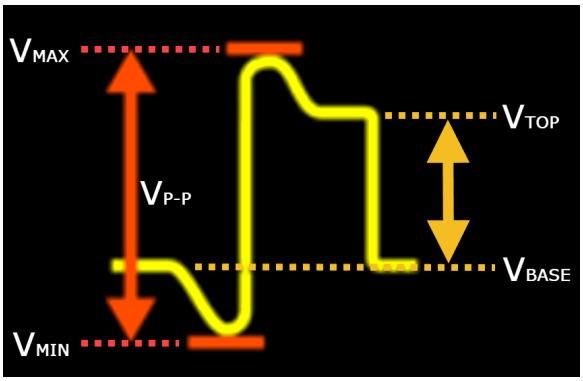
The objective of this test is to evaluate the maximum differential peak to peak voltage.

NOTE

The peak to peak voltage (V_{P-P}) formula is:

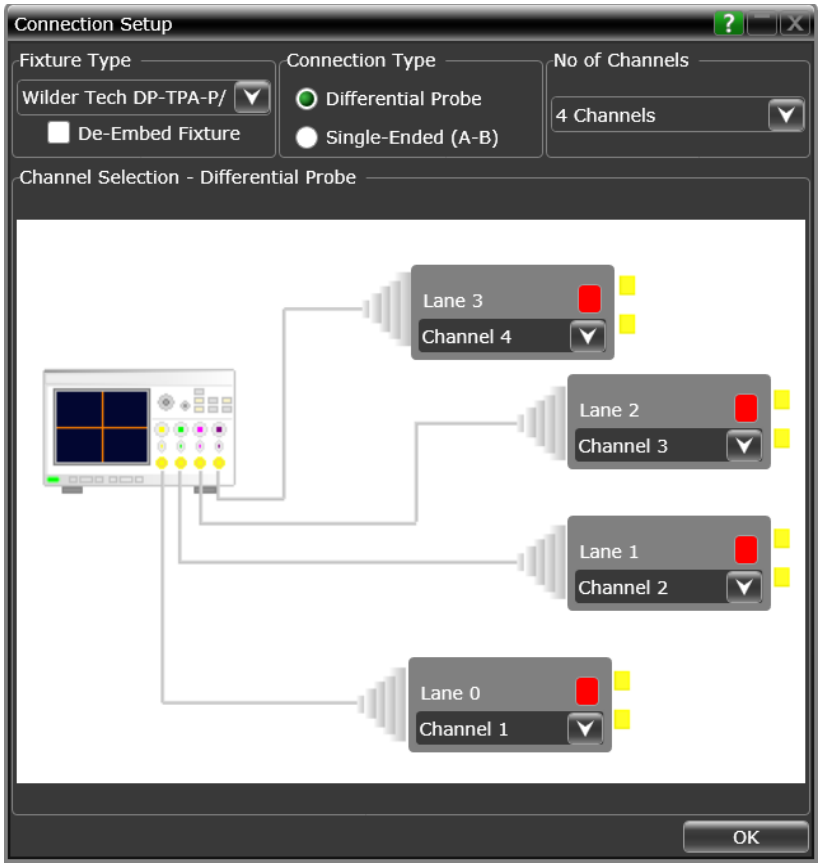
$$V_{P-P} = V_{MAX} - V_{MIN}$$

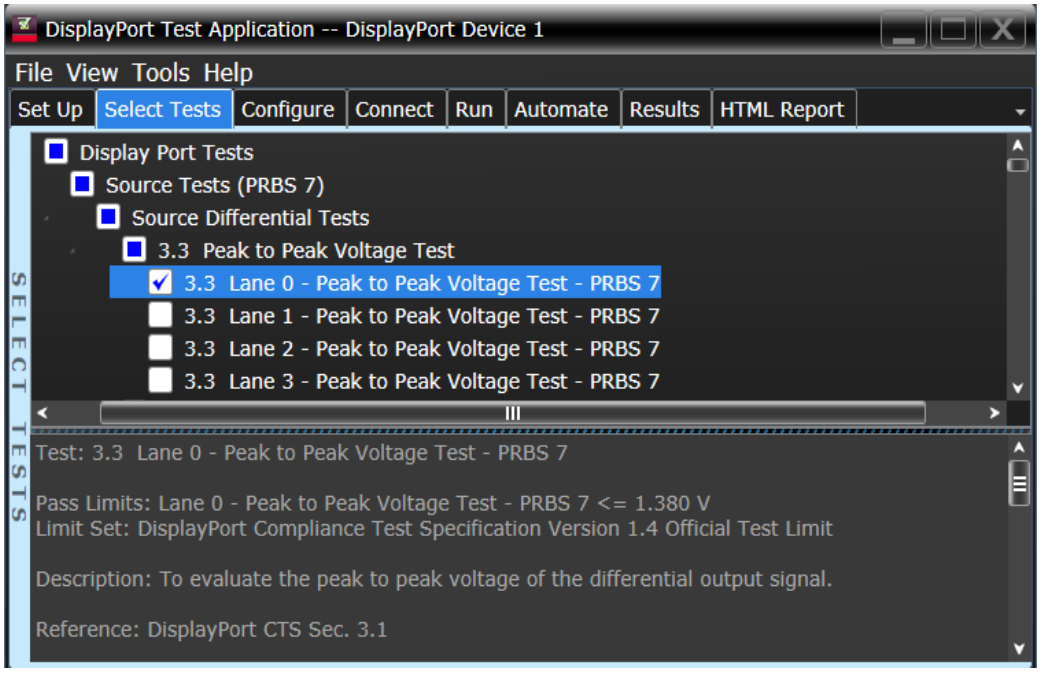
Please see the figure below for more info.



Test Conditions for Peak to Peak Voltage Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	▪ For RBR/HBR using PRBS7 pattern, test with SSC Enabled only if that condition is supported by the DUT. ▪ For HBR2/HBR3 using PLTPAT pattern, test with SSC Disabled if that condition is supported by the DUT.
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.4a Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR3 – PLTPAT


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Display Port Tests
Source Tests (PRBS 7)
Source Differential Tests
3.3 Peak to Peak Voltage Test
3.3 Lane 0 - Peak to Peak Voltage Test - PRBS 7
3.3 Lane 1 - Peak to Peak Voltage Test - PRBS 7
3.3 Lane 2 - Peak to Peak Voltage Test - PRBS 7
3.3 Lane 3 - Peak to Peak Voltage Test - PRBS 7
Test: 3.3 Lane 0 - Peak to Peak Voltage Test - PRBS 7
Pass Limits: Lane 0 - Peak to Peak Voltage Test - PRBS 7 <= 1.380 V
Limit Set: DisplayPort Compliance Test Specification Version 1.4 Official Test Limit
Description: To evaluate the peak to peak voltage of the differential output signal.
Reference: DisplayPort CTS Sec. 3.1

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{MAX} and V_{MIN} of the input signal.
   d Measure the data rate of the input signal.
3 Measure the maximum and minimum voltage of the input signal.
4 Calculate the peak to peak voltage using the equation:

$$\text{Peak to Peak Voltage} = V_{MAX} - V_{MIN}$$

5 Report the measurement results.

PASS Condition

For all Data Rates:

Maximum Differential Peak to Peak Voltage $\leq$ 1.38V.

Table 59 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX\text{-}DIFFp\text{-}p\_MAX}$	Max Output Voltage Level	-	-	1.38	V	For all Output Level and Pre-emphasis combinations.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.3*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-22*

Expected/Observable Results

The measured peak to peak voltage for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Inter-Pair Skew Test (Informative)

Test ID

For Standard DP Pattern:

- 1290001 – Lane0/Lane1 Inter-Pair Skew Test
- 1290002 – Lane0/Lane2 Inter-Pair Skew Test
- 1290003 – Lane0/Lane3 Inter-Pair Skew Test
- 1290004 – Lane1/Lane2 Inter-Pair Skew Test
- 1290005 – Lane1/Lane3 Inter-Pair Skew Test
- 1290006 – Lane2/Lane3 Inter-Pair Skew Test

For Arbitrary Pattern:

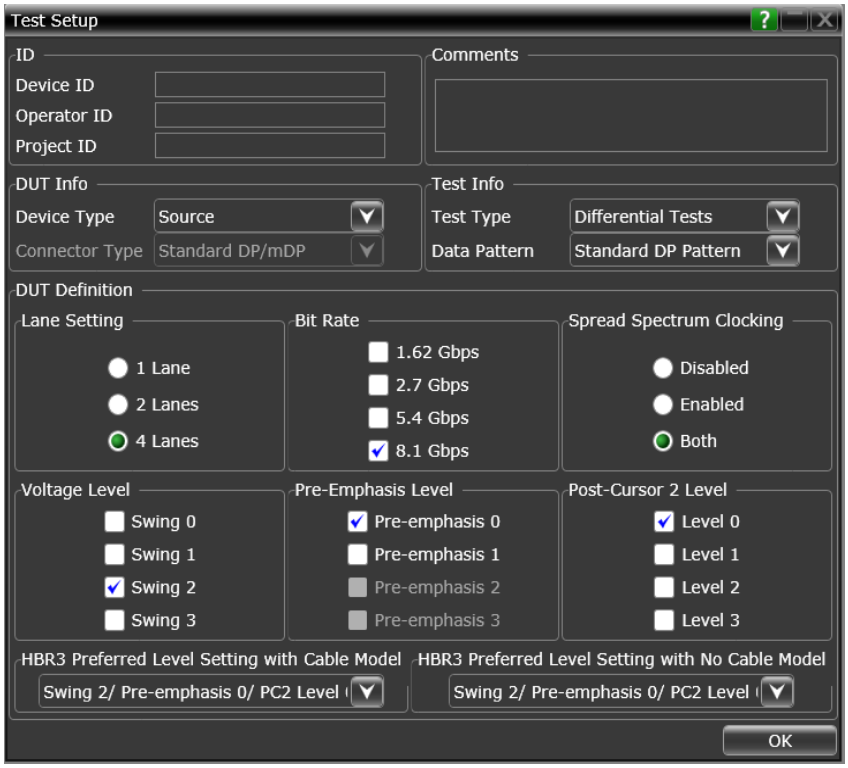
- Not applicable for arbitrary pattern

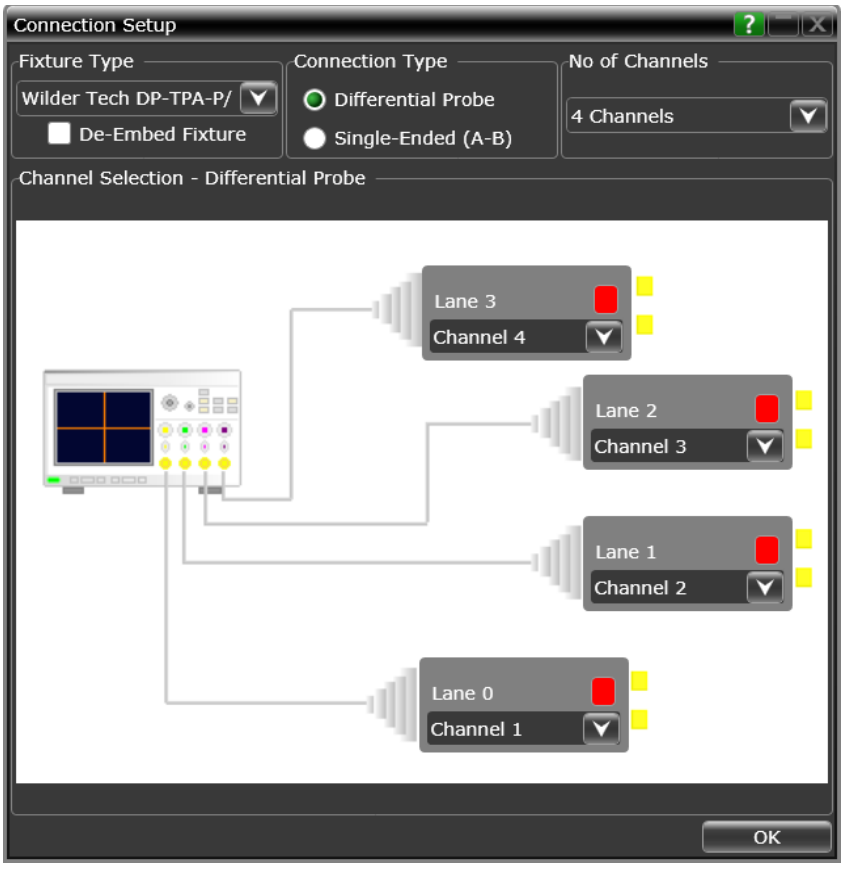
Test Overview

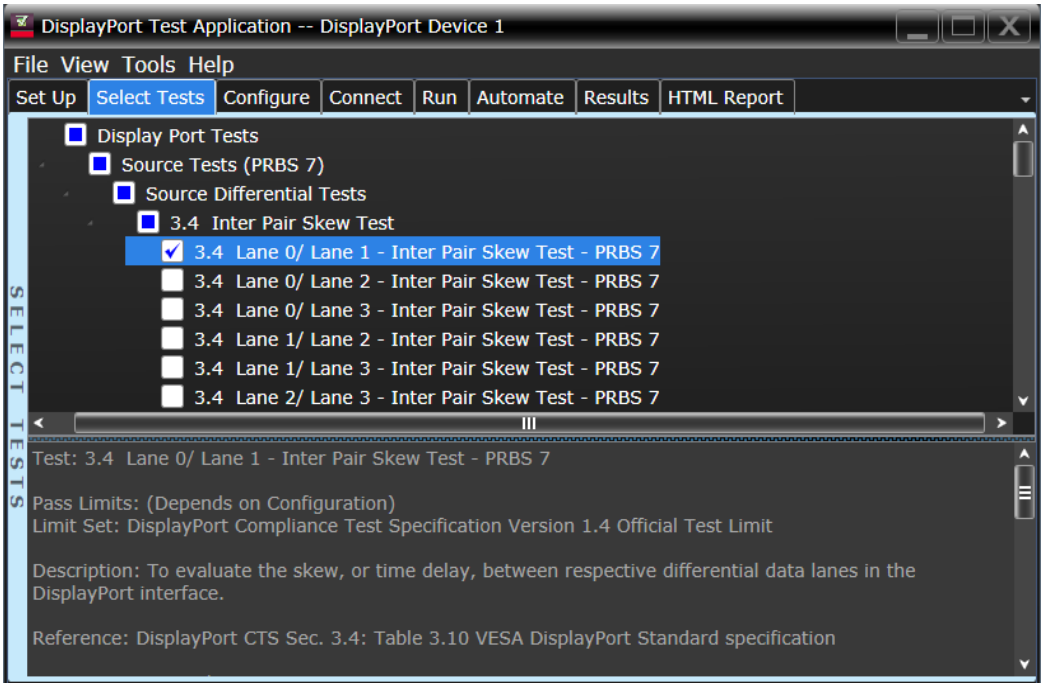
The objective of the test is to evaluate the skew or time delay between differential data lanes in the DisplayPort interface.

Test Conditions for Inter Pair Skew Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest Bit Rate supported (RBR, HBR, HBR2 or HBR3)
SSC	If DUT supports both SSC On and Off conditions, run tests using SSC Enabled only.
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported For two lane operation: Lane 0 to Lane 1 For four lane operation: Lane 0 to Lane 1 Lane 0 to Lane 2 Lane 0 to Lane 3 Lane 1 to Lane 2 Lane 1 to Lane 3 Lane 2 to Lane 3
Test Pattern	PRBS7 or DUT-dependent custom pattern


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given inter-pair skew measurement of Lane A to Lane B:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the Lane A input signal.

ii Scale the vertical display of the Lane A input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the Lane A input signal.

iv Verify the trigger and the amplitude of the Lane B input signal.

v Scale the vertical display of the Lane B input signal to optimum value.

vi Measure V_{TOP} and V_{BASE} of the Lane B input signal.

vii Measure the data rate of the Lane A input signal.

viii Measure the data rate of the Lane B input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

d Set up the parameter for the inter-pair skew measurement:

i Set up two display grids such that each grid displays one test lane data signal.

ii Set up the measurement threshold for each test lane data signal on the Transition Voltage = 0V.

iii Decode the data signal for each test lane.

iv Search the desired pattern from the decoded data signal.

v Measure the time difference between the corresponding edges of both test lanes:

$T_{Transition\_LaneA} - T_{Transition\_LaneB}$

vi Repeat the previous step until you measure 100 edges.

vii VESA DisplayPort 1.4a Standard specifies 20 UI offset Lane 0 to Lane 1, Lane 1 to Lane 2 and Lane 2 to Lane 3. The resultant offset is cumulative.

viii Calculate the inter-pair skew using the equation:

$$\text{Inter-Pair Skew} = \{1/\text{Number of Edges}\} \sum |T_{Transition\_LaneA} - T_{Transition\_LaneB}| - \text{Nominal Skew}$$

where, Nominal Skew is the expected offset between tested lanes.

2 Report the measurement results.

PASS Condition

Table 60 Pass/Fail Criteria

Highest Bit Rate	HBR3	-(6UI + 500ps) ≤ Inter-lane Skew Tolerance ≤ (6UI + 500ps)
	HBR2	-(4UI + 500ps) ≤ Inter-lane Skew Tolerance ≤ (4UI + 500ps)
	HBR/RBR	-2UI ≤ Inter-lane Skew Tolerance ≤ 2UI

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.6*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-22*

Expected/Observable Results

The measured inter-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Main Link Frequency Compliance Test

Test ID

For Standard DP Pattern:

- 12193001 12193002 12193003 12193004 – Main Link Frequency Compliance

For Arbitrary Pattern:

- 13193001 13193002 13193003 13193004 – Main Link Frequency Compliance

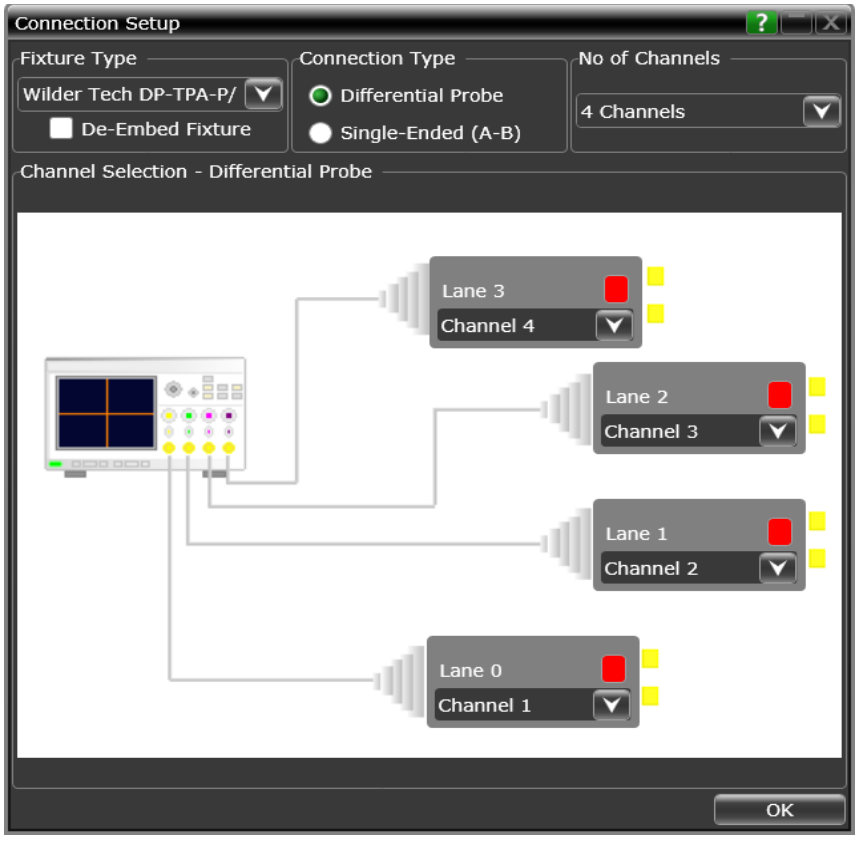
Test Overview

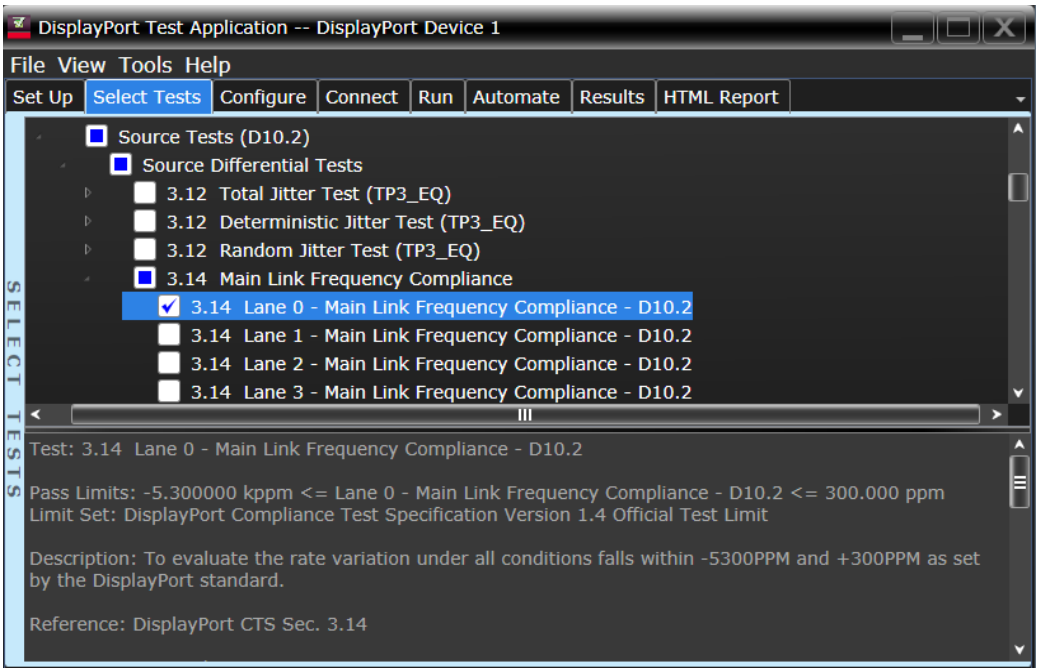
The objective of this test is to ensure that the average data rate under all conditions does not exceed the minimum and maximum values as set by the VESA DisplayPort 1.4a Standard.

Test Conditions for Main Link Frequency Compliance Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.

5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and the minimum measurement levels for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurement levels for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e For SSC Enabled Test condition, check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 5.0 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.
9 For the test condition “SSC Enabled”, set up the parameter of the SSC measurement:
   a Set up the memory depth and time-base to display one complete SSC cycle based on the measured SSC modulation frequency in Step 5.
   b Acquire the signal with one complete SSC cycle.
   c Get the minimum of FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

      Maximum Data Rate = 1 / (Minimum Unit Interval)

   d Get the maximum of FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

      Minimum Data Rate = 1 / (Maximum Unit Interval)

   e Repeat steps b, c and d until you acquire 10 SSC Cycles.
   f Calculate the mean value for the maximum and minimum data rates.
10 Report the measurement results.

PASS Condition

For SSC Enabled:
Maximum Data Rate (Frequency Max_{ppm}) $\leq$ 300 ppm

Minimum Data Rate (Frequency Min_{ppm}) $\geq$ -5300 ppm

For SSC Disabled:
Maximum Data Rate (Frequency Max_{ppm}) $\leq$ 300 ppm

Minimum Data Rate (Frequency Min_{ppm}) $\geq$ -300 ppm

Table 61 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
f_{HBR3}	Frequency for High Bit Rate 3	8.05707	8.1	8.10243	Gbps	
f_{HBR2}	Frequency for High Bit Rate 2	5.37138	5.4	5.40162	Gbps	Frequency high limit = +300ppm Frequency low limit = -5300ppm
f_{HBR}	Frequency for High Bit Rate	2.68569	2.7	2.70081	Gbps	
f_{RBR}	Frequency for Reduced Bit Rate	1.611414	1.62	1.620486	Gbps	

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.12*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-20*

Expected/Observable Results

The measured data rate for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Frequency Test

Test ID

For Standard DP Pattern:

- 12170001 12170002 12170003 12170004 – SSC Modulation Frequency Test

For Arbitrary Pattern:

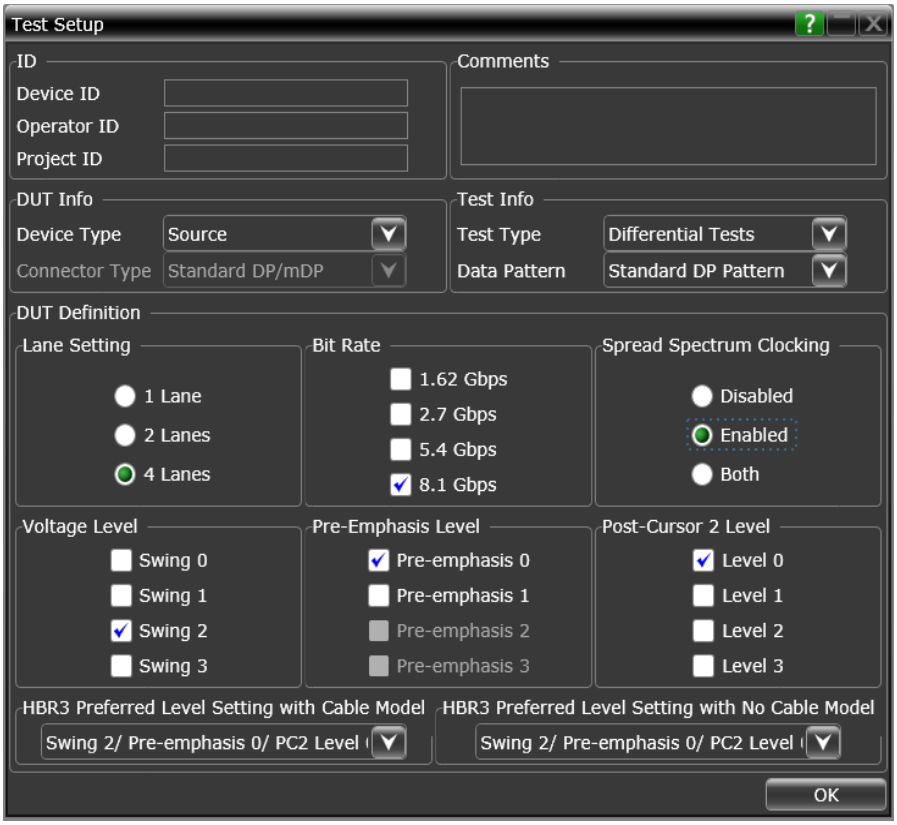
- 13170001 13170002 13170003 13170004 – SSC Modulation Frequency Test

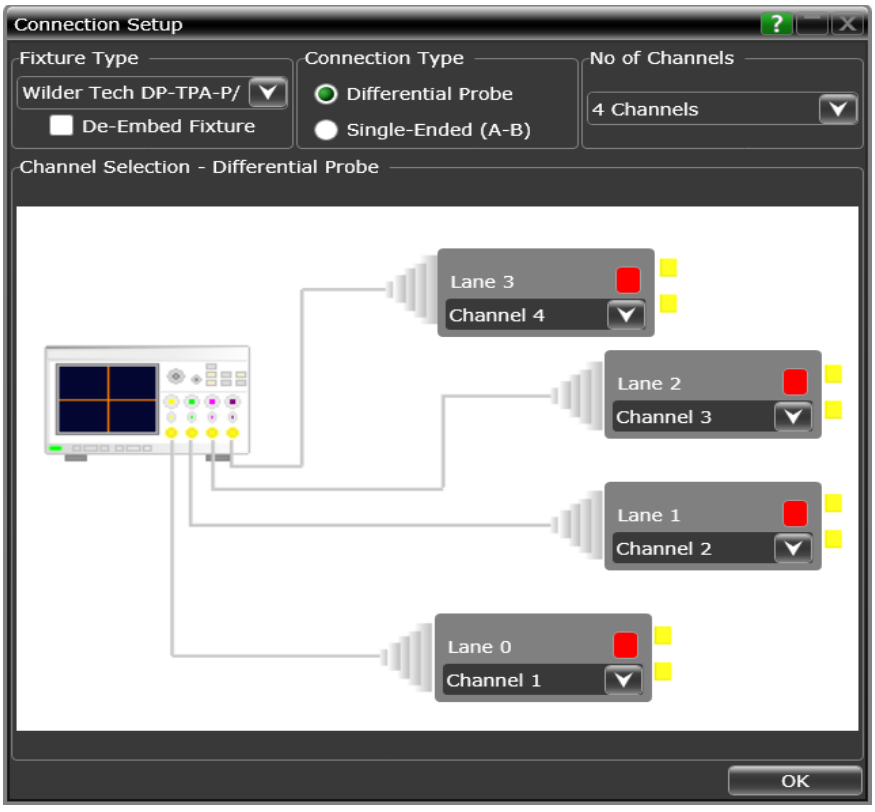
Test Overview

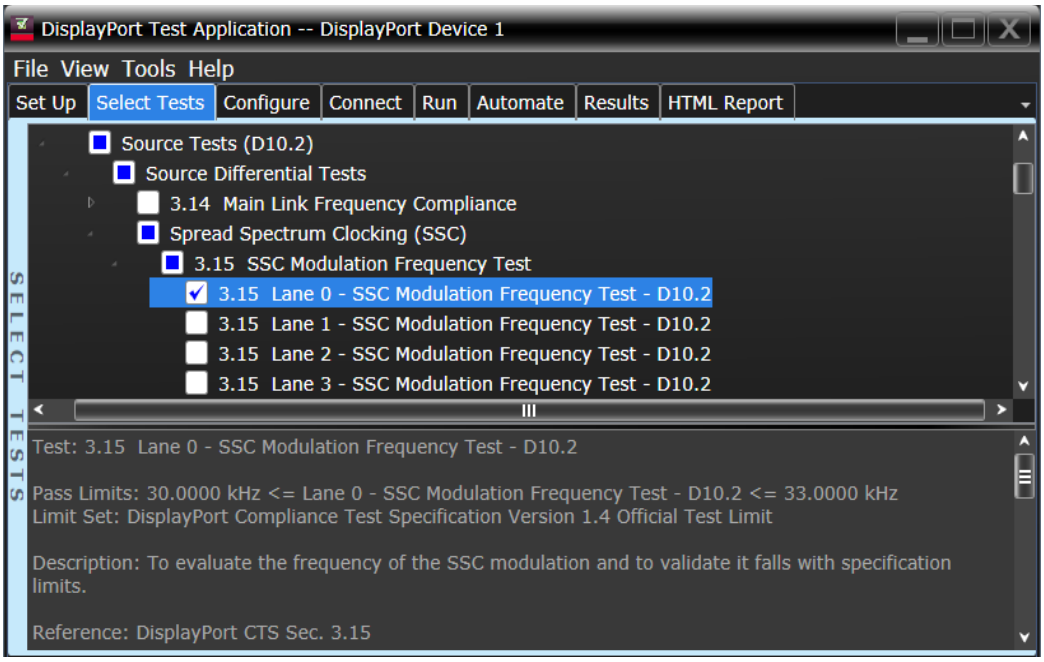
The objective of this test is to evaluate the frequency of the SSC modulation and to validate that the frequency is within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. Calculate the SSC modulation frequency from the average of the measured SSC modulation frequency for each cycle.

Test Conditions for SSC Modulation Frequency Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR3)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.

5 Set up the parameters for the frequency measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 5.0 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.
   g Acquire the signal for 10 SSC Cycles.
6 Get the mean value for the SSC Modulation frequency.
7 Report the measurement results.

PASS Condition

30kHz $\leq$ SSC Modulation Frequency (f_{SSC}) $\leq$ 33kHz

Table 62 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
Down_Spread_Frequency	Link clock down-spreading frequency	30	-	33	kHz	Range: 30kHz ~ 33kHz when down-spread enabled

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.13*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-20*

Expected/Observable Results

The measured SSC modulation frequency for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Deviation Test

Test ID

For Standard DP Pattern:

- 12180001 12180002 12180003 12180004 – SSC Modulation Deviation Test

For Arbitrary Pattern:

- 13180001 13180002 13180003 13180004 – SSC Modulation Deviation Test

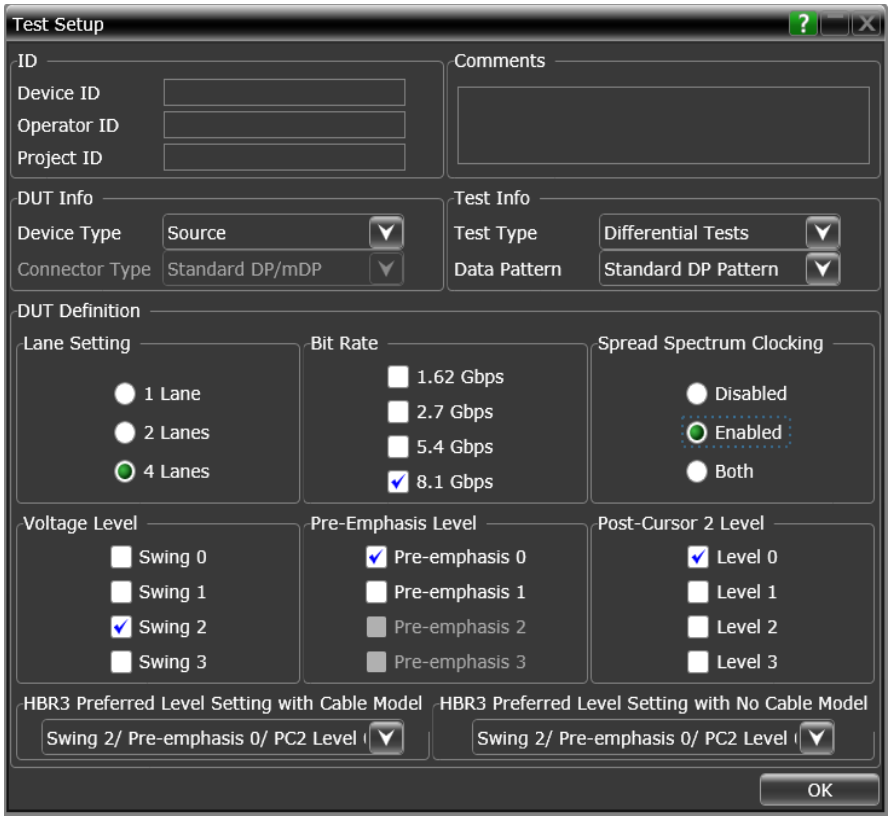
Test Overview

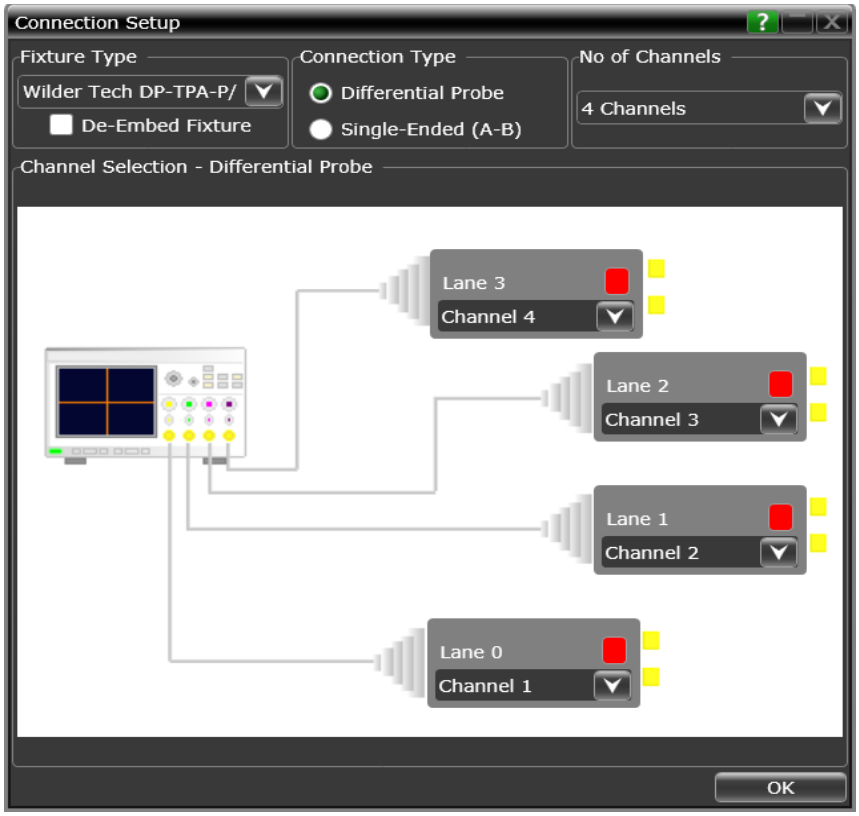
The objective of this test is to evaluate the range of SSC down-spreading of the transmitter signal in ppm and to validate that the values are within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3.0 dB corner frequency of 1.98 MHz. The analysis is conducted over a minimum of 10 full SSC cycles. For each cycle, the minimum and maximum data rate is evaluated. Calculate the SSC modulation deviation from the average of the minimum minus the average of the maximum using the equation:

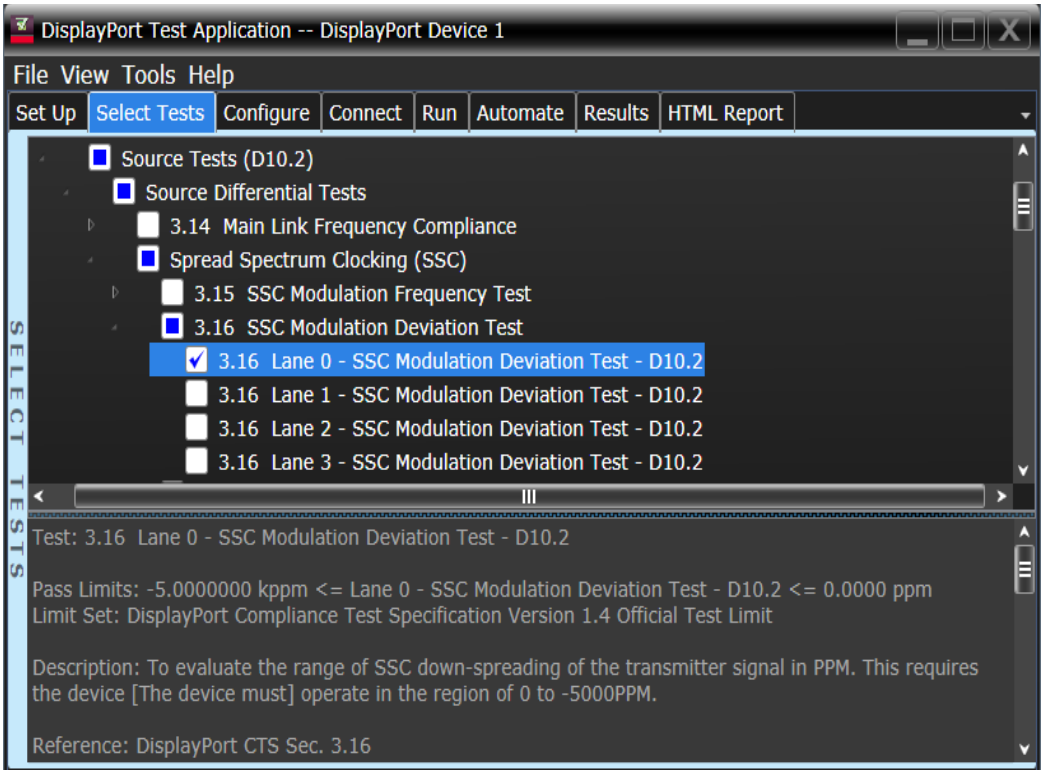
SSC Modulation Deviation = {[Average (Minimum Data Rate) - Average (Maximum Data Rate)] / Nominal Data Rate}*1E+6

Test Conditions for SSC Modulation Deviation Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR3)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.

5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and minimum measurements for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurements for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e Check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point for three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 5.0 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 filtered unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurements for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.
9 Set up the parameters for SSC measurement.
   a Set up memory depth and time-base to display one complete SSC Cycle based on the measured SSC modulation frequency in step 5.
   b Acquire the signal with one complete SSC Cycle.
   c Get the minimum of the FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

      Maximum Data Rate = 1/Minimum Unit Interval

   d Get the maximum of the FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

      Minimum Data Rate = 1/Maximum Unit Interval

   e Repeat step b,c and d until you acquire 10 SSC Cycles.
   f Calculate the mean value for the maximum and minimum data rate.
10 Calculate the SSC Modulation Deviation using the equation:

   SSC Modulation Deviation = {[Average (Minimum Data Rate) - Average (Maximum Data Rate)] / Nominal Data Rate}*1E+6

11 Report the measurement results.

PASS Condition

-5300 ppm $\leq$ SSC Modulation Deviation (Resultant$_{SSC\ Range}$) $\leq$ 300 ppm

Table 63 DisplayPort Main Link Transmitter System Parameters

Symbol	Parameter	Min	Nom	Max	Unit	Comments
Down_Spread_Amplitude	Link clock down-spreading	0	-	0.5	%	Range: 0% ~ 0.5% when down-spread enabled

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.14*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-20*

Expected/Observable Results

The measured SSC modulation deviation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Deviation HF Variation Test (Informative)

Test ID

For Standard DP Pattern:

- 12200001 12200002 12200003 12200004 – SSC Deviation HF Variation Test (Informative)

For Arbitrary Pattern:

- 13200001 13200002 13200003 13200004 – SSC Deviation HF Variation Test (Informative)

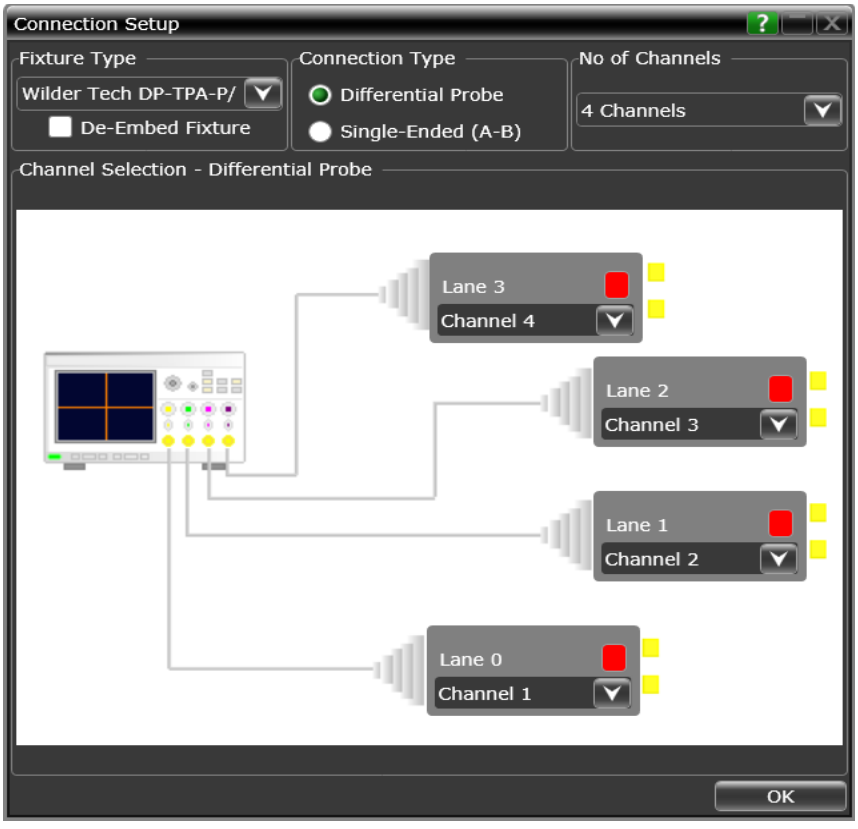
Test Overview

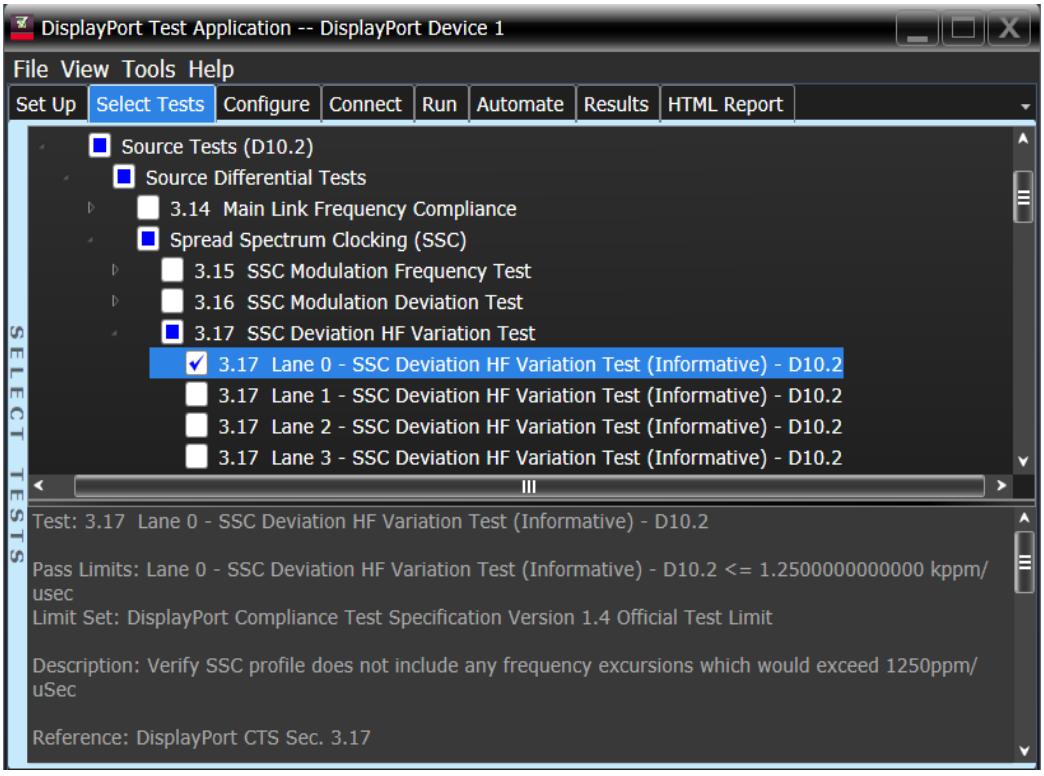
The objective of this test is to verify that the SSC profile does not include any frequency deviation that may exceed 1250 ppm/µsec. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles.

Test Conditions for SSC Deviation HF Variation Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR3)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.

5 Set up the parameters for the frequency measurement.

a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 5.0 MHz.

b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.

c Set up the memory depth and time-base using the settings defined in the Configuration Variable.

d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.

e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).

f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.

6 Set up the parameters for the SSC measurement.

a Set up memory depth and time-base to display one complete SSC cycle using the measured SSC Modulation Frequency in Step 5.

b Acquire the signal with one complete SSC Cycles.

c Read the FUNC2 filtered unit interval measurement trend.

d Compute the slope using the “Sliding Window” with 0.5 µsec window width. Calculate the slope using the equation:

$$\text{Slope} = [f(t) - f(t-0.5\ \mu\text{sec})/0.5\ \mu\text{sec}$$

e Repeat step b, c and d until you acquire 10 SSC Cycles.

f Get the maximum value for the computed value of slope.

7 Report the measurement results.

PASS Condition

SSC_t dF/dt $\leq$ 1250ppm/µsec

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.15*

Expected/Observable Results

The measured SSC deviation high frequency variation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Eye Diagram Test (TP3_EQ)

Test ID

For Standard DP Pattern (HBR):

- 1211001, 1211002, 1211003, 1211004 – Eye Diagram Test (TP3_EQ) - PRBS7
- 1211011, 1211012, 1211013, 1211014 – Eye Diagram Test with No Cable Model (TP3_EQ) - PRBS7

For Standard DP Pattern (HBR2):

- 1215001, 1215002, 1215003, 1215004 – Eye Diagram Test (TP3_EQ) - HBR2CPAT
- 1215011, 1215012, 1215013, 1215014 – Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT

For Arbitrary Pattern:

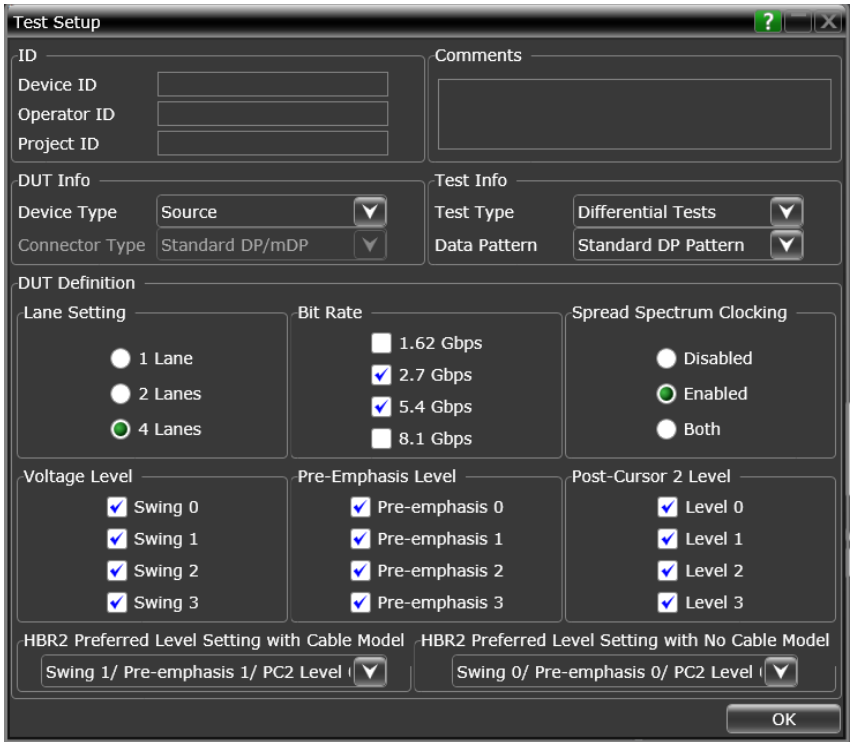
- 1315001, 1315002, 1315003, 1315004 – Eye Diagram Test (TP3_EQ)
- 1315011, 1315012, 1315013, 1315014 – Eye Diagram Test with No Cable Model (TP3_EQ)

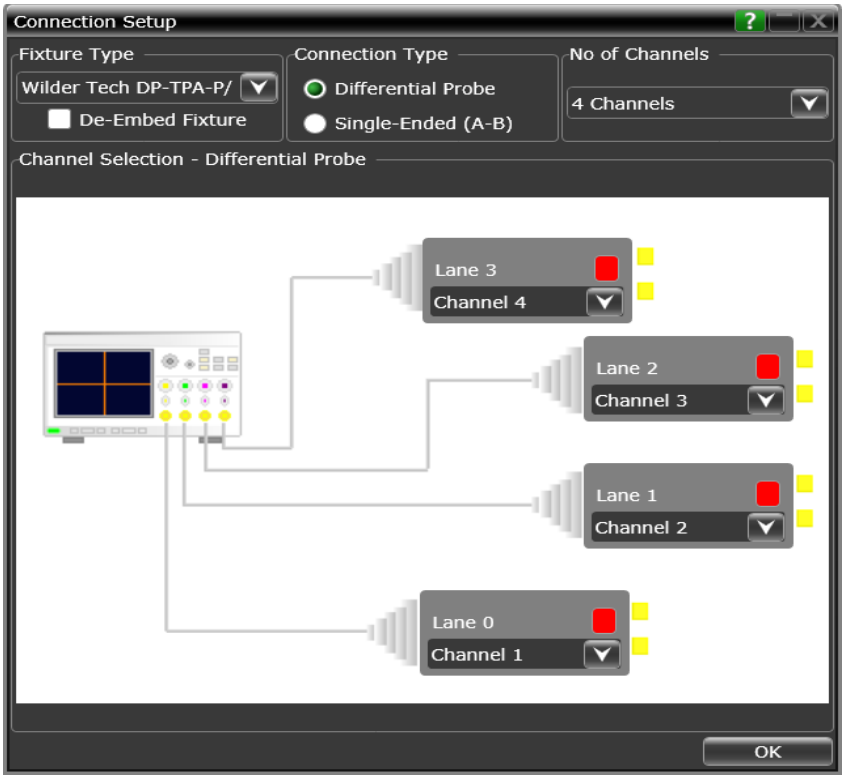
Test Overview

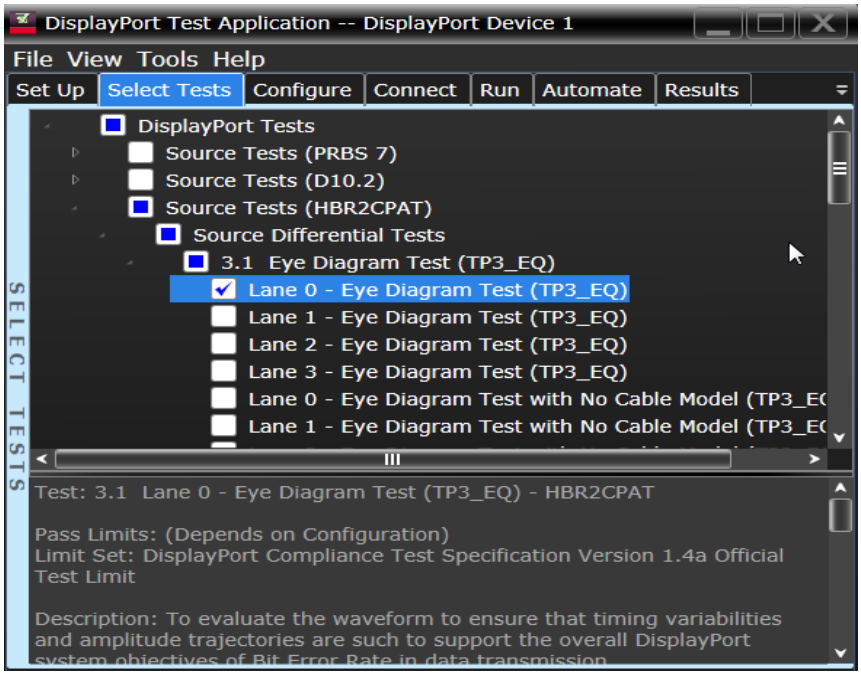
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions for Eye Diagram Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR (Informative) and HBR2
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	HBR – Level 2 HBR2 – Any Voltage Level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	HBR – Level 0 HBR2 – Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	HBR – Level 0 HBR2 – Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	HBR – PRBS7 HBR2 – HBR2CPAT
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure for HBR

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.

7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 2 million UI are folded.
8 Measure the jitter of the eye diagram using the Histogram.
9 Check for any signal trajectories that may have entered into the mask.
10 Report the measurement results.

Measurement Procedure for HBR2

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]:
   a Pattern fold the equalized signal based on the High Level Voltage (V_{HIGH}) random noise configuration variable.
   b Set up the vertical waveform histogram on the equalized signal to measure random noise of High Level Voltage (V_{HIGH}).
   c Measure the High Level Voltage (V_{HIGH}) random noise based on the standard deviation of the waveform histogram.
   d Pattern fold the equalized signal based on the Low Level Voltage (V_{LOW}) random noise configuration variable.
   e Set up the vertical waveform histogram on the equalized signal to measure the random noise of Low Level Voltage (V_{LOW}).
   f Measure the Low Level Voltage (V_{LOW}) random noise based on the standard deviation of the waveform histogram.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge and right edge.
8 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.

9 Find the maximum eye height location of the eye diagram.

10 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:

a Set up the parameter of the jitter separation using the EZJIT Plus/Complete Software.

i Load the jitter separation parameter into EZJIT Plus/Complete Software based on the settings in the Configuration Variable.

ii Acquire the signal until 2 million edges are analyzed.

b Note the value of the jitter component from the EZJIT Plus/Complete Software.

11 Create the eye mask based on the following criteria:

a If you select more than one lane (2 lanes or 4 lanes DUT configuration), the eye mask height and width is derate in the following manner, to include crosstalk as defined in DisplayPort 1.4a Compliance Test Specification:

i Eye Mask Width Derate (Crosstalk) = 0.04 UI

ii Eye Mask Height Derate (Crosstalk) = 0.014V

b If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]: eye mask height and width is derate as below to comprehend the noise/jitter extrapolated to BER 10^{-9} for an Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI:

i Calculate the Eye Mask Width Derate (Random Jitter) using the equation:

$$\text{Eye Mask Width Derate (Random Jitter)} = 2.5 * \text{Random Jitter}_{rms}$$

ii Calculate the Eye Mask Height Derate (Random Noise) using the equation:

$$V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{HIGH}\ \text{Random Noise}_{rms}$$

$$V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{LOW}\ \text{Random Noise}_{rms}$$

NOTE The factor 2.5 is the delta between BER 10^{-6} (9.507) and 10^{-9} (11.996) to comprehend the noise/jitter extrapolated to BER 10^{-9} as the Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI.

BER	N
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996

c Place the eye mask height at the point of the maximum eye height found in Step 9.

d Calculate the Eye Mask Width:

$$\text{Eye Mask Width} = \text{Eye Width Specification (0.38 UI)} + \text{Eye Mask Width Derate (Crosstalk)} + 2 * \text{Eye Mask Width Derate (Random Jitter)}$$

e Calculate the Eye Mask Height:

$$\text{Eye Mask Height} = \{\text{Eye Height Specification (0.09 V)} + \text{Eye Mask Height Derate (Crosstalk)}\}/2 + V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)}$$

$$\text{Eye Mask Height} = -\{\text{Eye Height Specification (0.09 V)} + \text{Eye Mask Height Derate (Crosstalk)}\}/2 - V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)}$$

12 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram.
   c Run the eye mask until 2 million UI are folded.
13 Measure the eye height of the eye diagram using the Histogram.
14 Measure the jitter of the eye diagram using the Histogram.
15 Calculate the eye width based on the measured jitter of the eye diagram.
16 Check for any signal trajectories that may have entered into the mask.
17 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 64 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 64 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

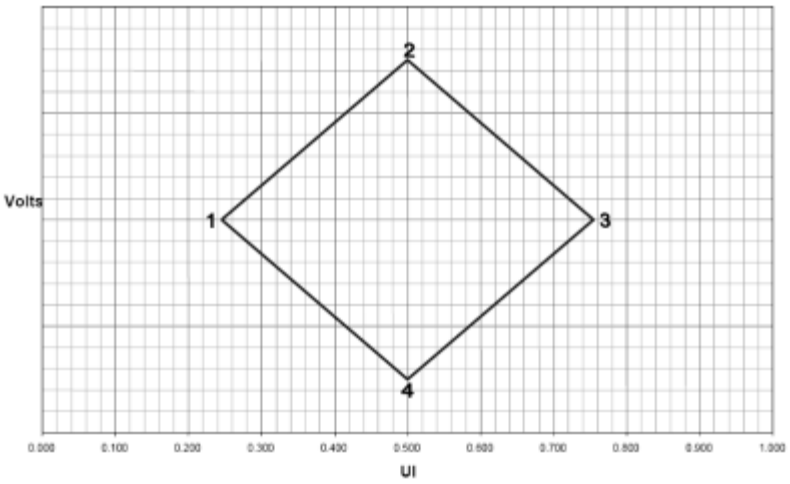


Figure 66 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 65 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.045*
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.045*

NOTE

*Eye height limit of 45 mV and -45 mV assumes cross-talk as 0, which is only possible in case of single lane testing.

In case of multi-lane testing, cross talk exists, and the eye height values deviate by ± 7 mV. Thus the eye height becomes (+45 +7) mV and (-45 -7) mV or +52 mV and -52 mV.

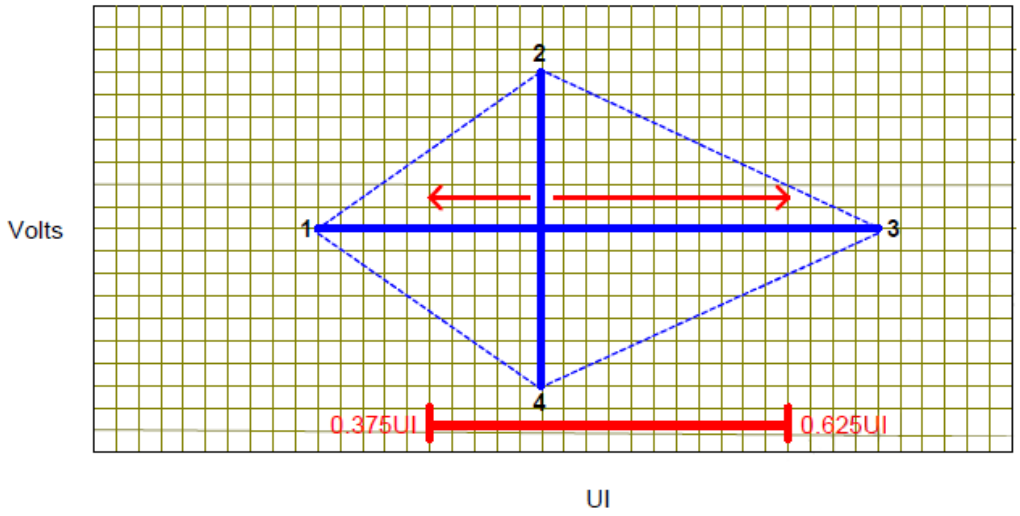


Figure 67 The Eye Mask at TP3_EQ (HBR2)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.1*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2.8.2, Table 3-32 for HBR and Section 3.5.2, Table 3-24 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Eye Diagram Test (TP3_CTLE)

Test ID

For Standard DP Pattern (HBR3):

- 1216001, 1216002, 1216003, 1216004 – Eye Diagram Test (TP3_CTLE)

For Arbitrary Pattern:

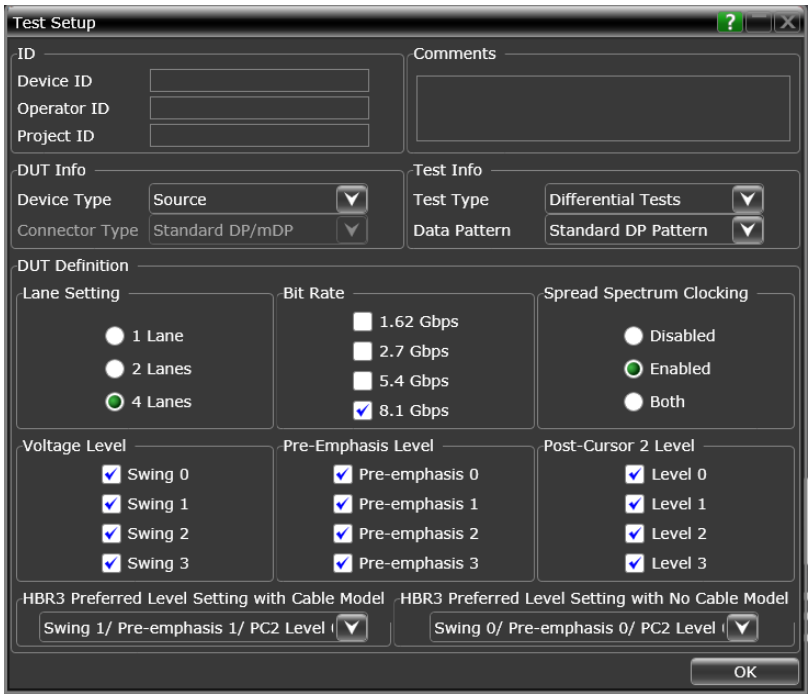
- 1316001, 1316002, 1316003, 1316004 – Eye Diagram Test (TP3_CTLE)

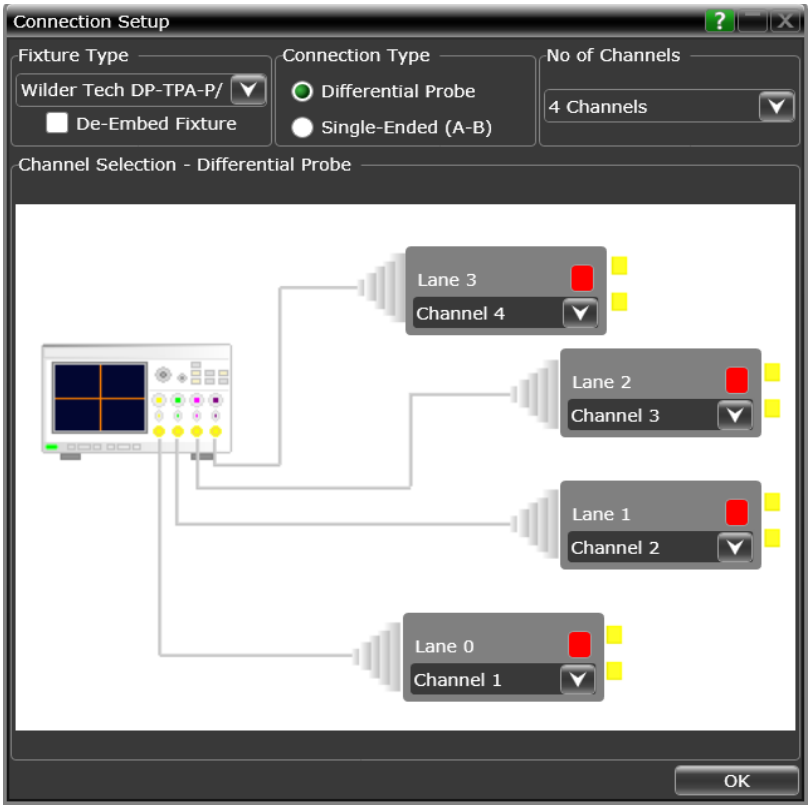
Test Overview

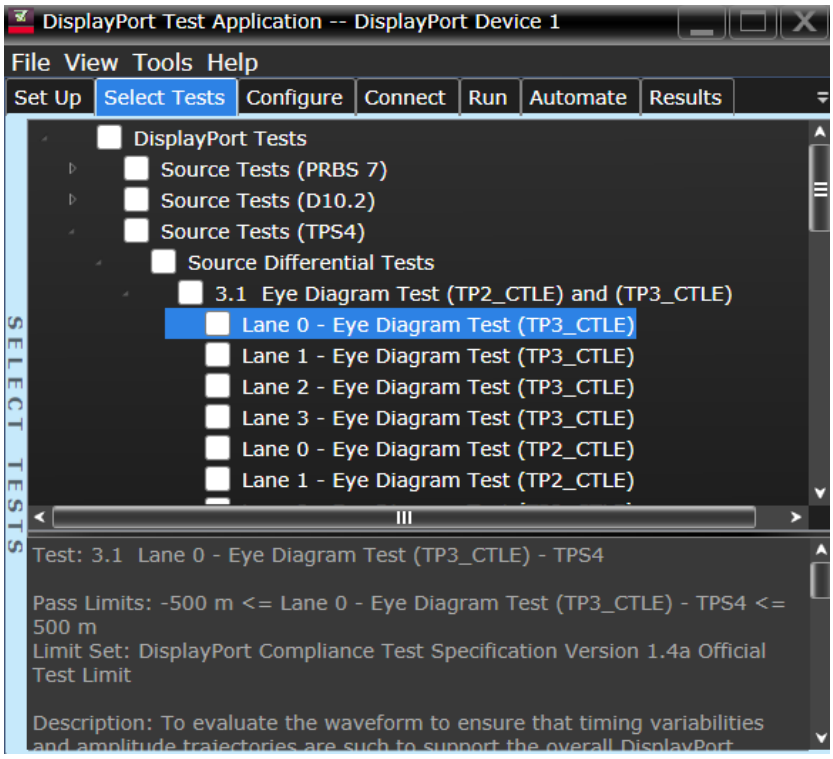
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions for Eye Diagram Test (TP3_CTLE)

Test Parameter	Condition
Test Point	TP3_CTLE
Bit Rate	HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any Voltage Level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	TPS4
Cable Model	“Worst Case”


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure for HBR3

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_CTLE): Use “Worst Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”, exclude the DFE.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.

5 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:
   a Pattern fold the equalized signal based on the High Level Voltage (V_{HIGH}) random noise configuration variable.
   b Set up the vertical waveform histogram on the equalized signal to measure random noise of High Level Voltage (V_{HIGH}).
   c Measure the High Level Voltage (V_{HIGH}) random noise based on the standard deviation of the waveform histogram.
   d Pattern fold the equalized signal based on the Low Level Voltage (V_{LOW}) random noise configuration variable.
   e Set up the vertical waveform histogram on the equalized signal to measure the random noise of Low Level Voltage (V_{LOW}).
   f Measure the Low Level Voltage (V_{LOW}) random noise based on the standard deviation of the waveform histogram.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge and right edge.
8 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.
9 Find the maximum eye height location of the eye diagram.
10 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:
   a Set up the parameter of the jitter separation using the EZJIT Plus/Complete Software.
      i Load the jitter separation parameter into EZJIT Plus/Complete Software based on the settings in the Configuration Variable.
      ii Acquire the signal until 2 million edges are analyzed.
   b Note the value of the jitter component from the EZJIT Plus/Complete Software.
11 Create the eye mask based on the following criteria:
   a If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]: eye mask height and width is derate as below to comprehend the noise/jitter extrapolated to BER 10^{-9} for an Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI:
      i Calculate the Eye Mask Width Derate (Random Jitter) using the equation:

$$\text{Eye Mask Width Derate (Random Jitter)} = 2.5 * \text{Random Jitter}_{rms}$$

      ii Calculate the Eye Mask Height Derate (Random Noise) using the equation:

$$V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{HIGH}\ \text{Random Noise}_{rms}$$

$$V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{LOW}\ \text{Random Noise}_{rms}$$

NOTE The factor 2.5 is the delta between BER 10^{-6} (9.507) and 10^{-9} (11.996) to comprehend the noise/jitter extrapolated to BER 10-9 as the Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI.

BER	N
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996

c Place the eye mask height at the point of the maximum eye height found in Step 9.

d Calculate the Eye Mask Width:

Eye Mask Width = Eye Width Specification + 2 * Eye Mask Width Derate (Random Jitter)

e Calculate the Eye Mask Height:

Eye Mask Height = {Eye Height Specification}/2 + V_{HIGH} Eye Mask Height Derate (Random Noise)

Eye Mask Height = -{Eye Height Specification}/2 - V_{LOW} Eye Mask Height Derate (Random Noise)

12 Set up the parameters for the Mask Test.

a Load the eye mask based on the settings in the Configuration Variable.

b Center the eye mask at the middle of the eye diagram.

c Run the eye mask until 2 million UI are folded.

13 Measure the eye height of the eye diagram using the Histogram.

14 Measure the jitter of the eye diagram using the Histogram.

15 Calculate the eye width based on the measured jitter of the eye diagram.

16 Check for any signal trajectories that may have entered into the mask.

17 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 64 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 66 Eye Diagram Mask Coordinates for TP3_CTLE (HBR3)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.53 UI	0.00000
2	Any passing UI location between 0.375 and 0.625 UI	0.0325
3	Point 1 + 0.53 UI	0.00000
4	Same as Point 2	-0.0325

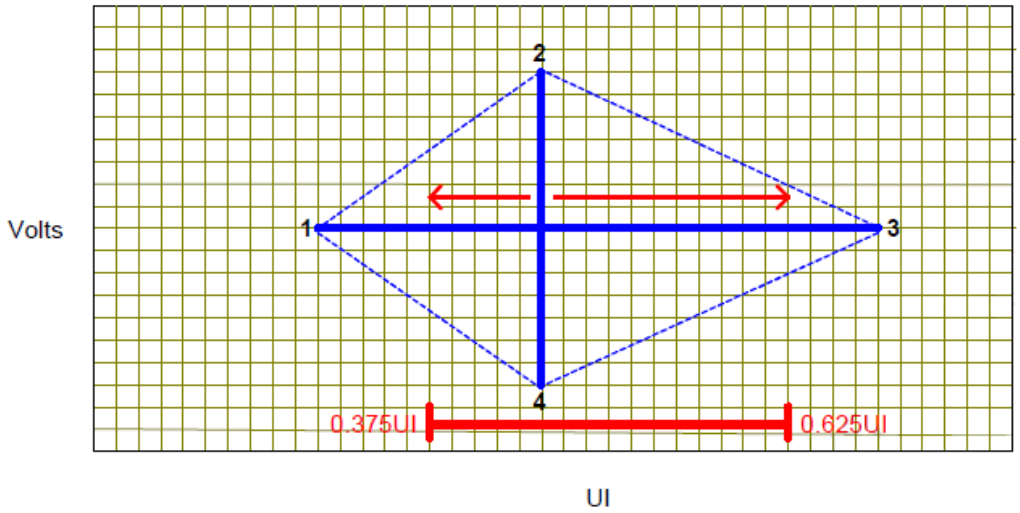


Figure 68 The Eye Mask at TP3_CTLE (HBR3)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.1*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2 and Table 3-23 for HBR3*

Expected/Observable Results

The measured eye diagram for the test signal at TP3_CTLE shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Eye Diagram Test (TP2_CTLE) (Informative)

Test ID

For Standard DP Pattern (HBR3):

- 1216011, 1216012, 1216013, 1216014 – Eye Diagram Test (TP2_CTLE)

For Arbitrary Pattern:

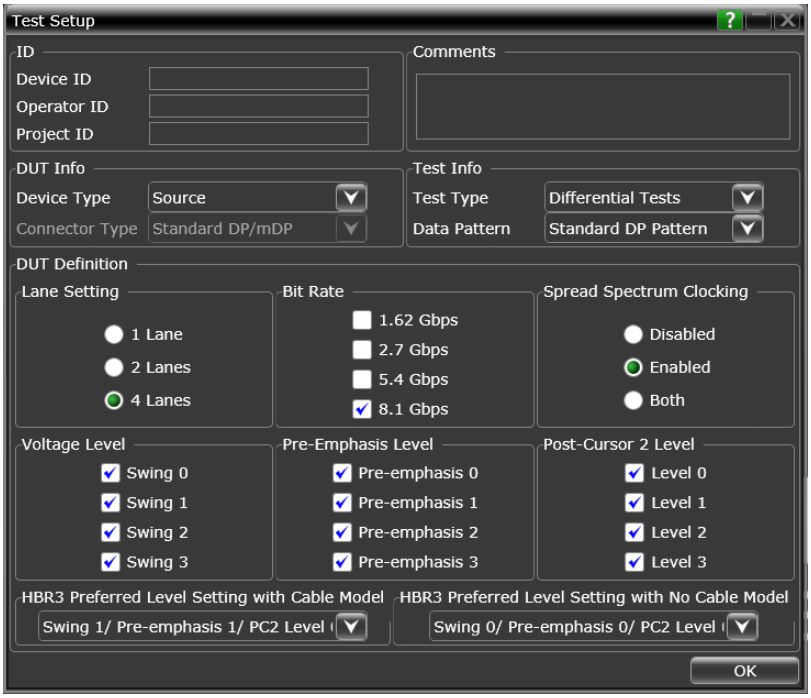
- 1316011, 1316012, 1316013, 1316014 – Eye Diagram Test (TP2_CTLE)

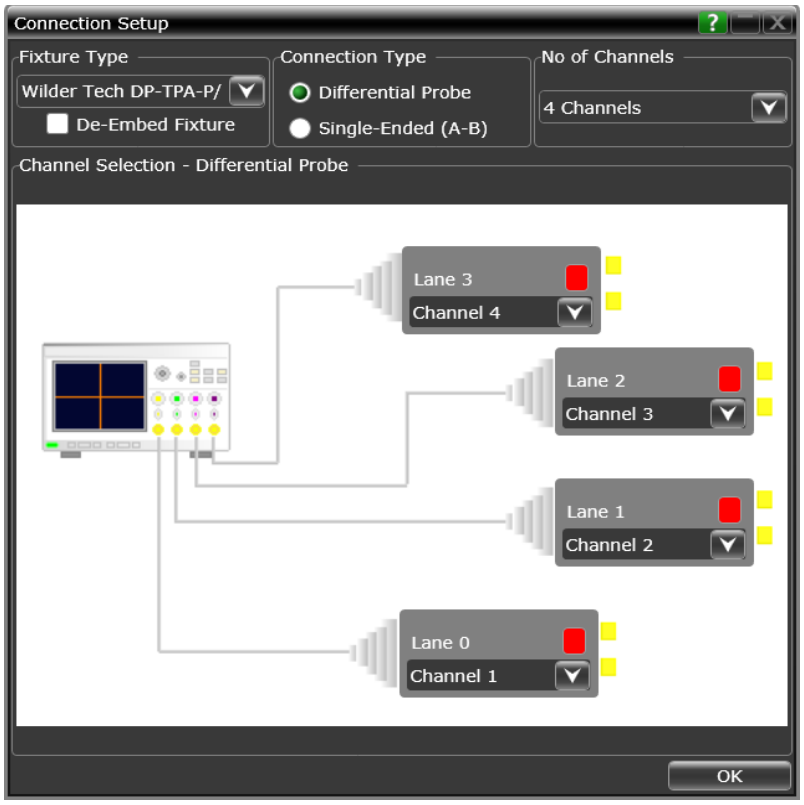
Test Overview

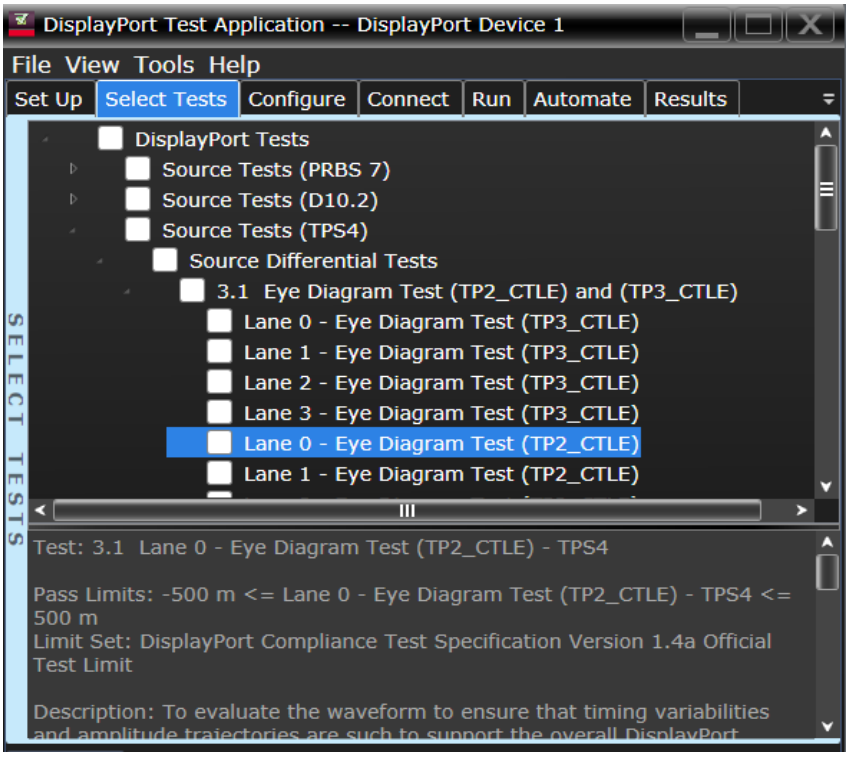
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions for Eye Diagram Test (TP2_CTLE)

Test Parameter	Condition
Test Point	TP2_CTLE
Bit Rate	HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any Voltage Level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	TPS4
Cable Model	“Zero Length”


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure for HBR3

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP2_CTLE): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”, exclude the DFE.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.

5 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:
   a Pattern fold the equalized signal based on the High Level Voltage (V_{HIGH}) random noise configuration variable.
   b Set up the vertical waveform histogram on the equalized signal to measure random noise of High Level Voltage (V_{HIGH}).
   c Measure the High Level Voltage (V_{HIGH}) random noise based on the standard deviation of the waveform histogram.
   d Pattern fold the equalized signal based on the Low Level Voltage (V_{LOW}) random noise configuration variable.
   e Set up the vertical waveform histogram on the equalized signal to measure the random noise of Low Level Voltage (V_{LOW}).
   f Measure the Low Level Voltage (V_{LOW}) random noise based on the standard deviation of the waveform histogram.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge and right edge.
8 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.
9 Find the maximum eye height location of the eye diagram.
10 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:
   a Set up the parameter of the jitter separation using the EZJIT Plus/Complete Software.
      i Load the jitter separation parameter into EZJIT Plus/Complete Software based on the settings in the Configuration Variable.
      ii Acquire the signal until 2 million edges are analyzed.
   b Note the value of the jitter component from the EZJIT Plus/Complete Software.
11 Create the eye mask based on the following criteria:
   a If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]: eye mask height and width is derate as below to comprehend the noise/jitter extrapolated to BER 10^{-9} for an Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI:
      i Calculate the Eye Mask Width Derate (Random Jitter) using the equation:

$$\text{Eye Mask Width Derate (Random Jitter)} = 2.5 * \text{Random Jitter}_{rms}$$

      ii Calculate the Eye Mask Height Derate (Random Noise) using the equation:

$$V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{HIGH}\ \text{Random Noise}_{rms}$$

$$V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{LOW}\ \text{Random Noise}_{rms}$$

NOTE The factor 2.5 is the delta between BER 10^{-6} (9.507) and 10^{-9} (11.996) to comprehend the noise/jitter extrapolated to BER 10-9 as the Eye Diagram Test (TP2_CTLE) only acquiring 1e6 UI.

BER	N
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996

c Place the eye mask height at the point of the maximum eye height found in Step 9.

d Calculate the Eye Mask Width:

Eye Mask Width = Eye Width Specification + 2 * Eye Mask Width Derate (Random Jitter)

e Calculate the Eye Mask Height:

Eye Mask Height = {Eye Height Specification}/2 + V_{HIGH} Eye Mask Height Derate (Random Noise)

Eye Mask Height = -{Eye Height Specification}/2 - V_{LOW} Eye Mask Height Derate (Random Noise)

12 Set up the parameters for the Mask Test.

a Load the eye mask based on the settings in the Configuration Variable.

b Center the eye mask at the middle of the eye diagram.

c Run the eye mask until 2 million UI are folded.

13 Measure the eye height of the eye diagram using the Histogram.

14 Measure the jitter of the eye diagram using the Histogram.

15 Calculate the eye width based on the measured jitter of the eye diagram.

16 Check for any signal trajectories that may have entered into the mask.

17 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 64 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 67 Eye Diagram Mask Coordinates for TP2_CTLE (HBR3)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.67UI	0.00000
2	Any passing UI location between 0.375 and 0.625UI	0.0325
3	Point 1 + 0.67UI	0.00000
4	Same as Point 2	-0.0325

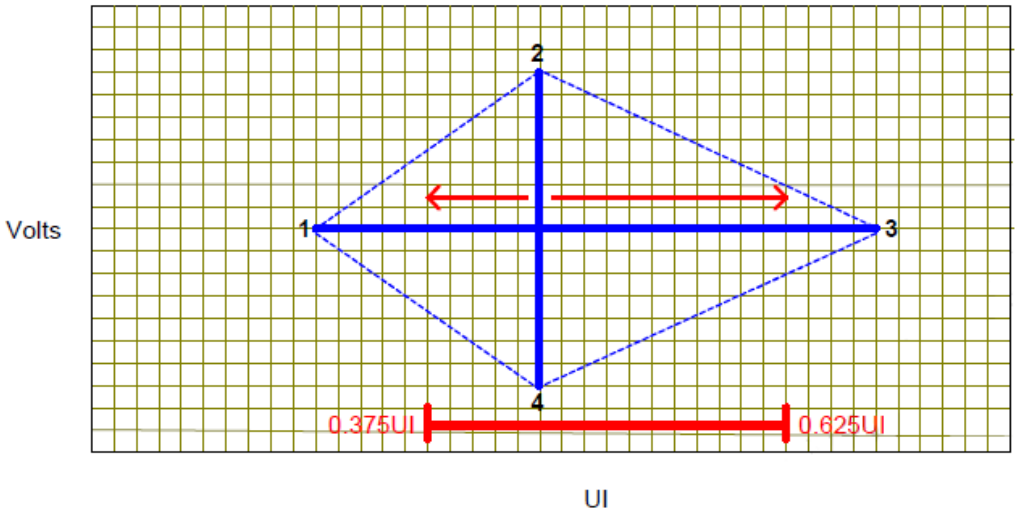


Figure 69 The Eye Mask at TP2_CTLE (HBR3)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.1*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2 and Table 3-23 for HBR3*

Expected/Observable Results

The measured eye diagram for the test signal at TP2_CTLE shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Eye Diagram Test (TP3_DFE) (VESA DFE Tool)

Test ID

For Standard DP Pattern (HBR3):

- 1218001, 1218002, 1218003, 1218004 - Eye Diagram Test (TP3_DFE)

For Arbitrary Pattern:

- 1318001, 1318002, 1318003, 1318004 - Eye Diagram Test (TP3_DFE)

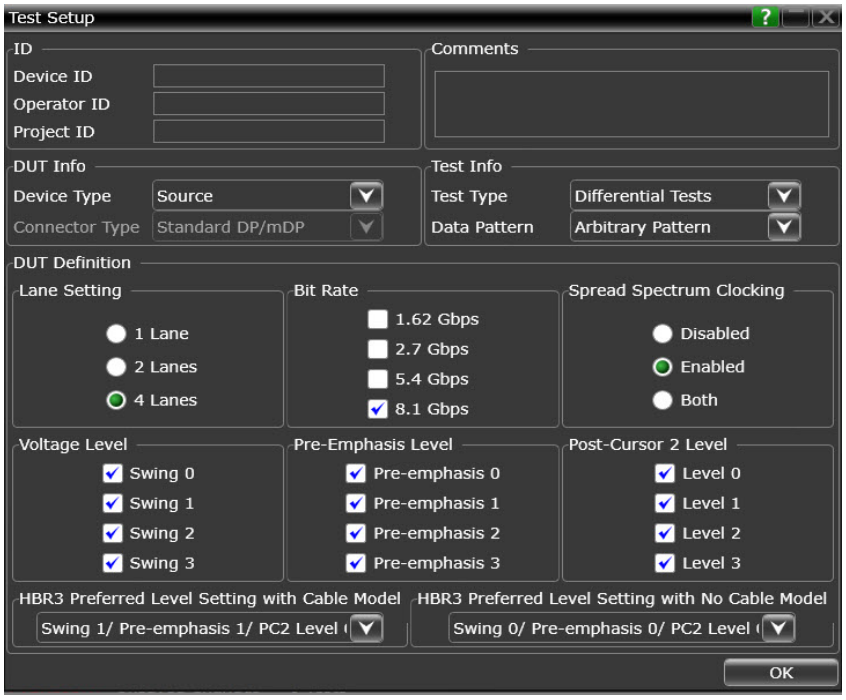
Test Overview

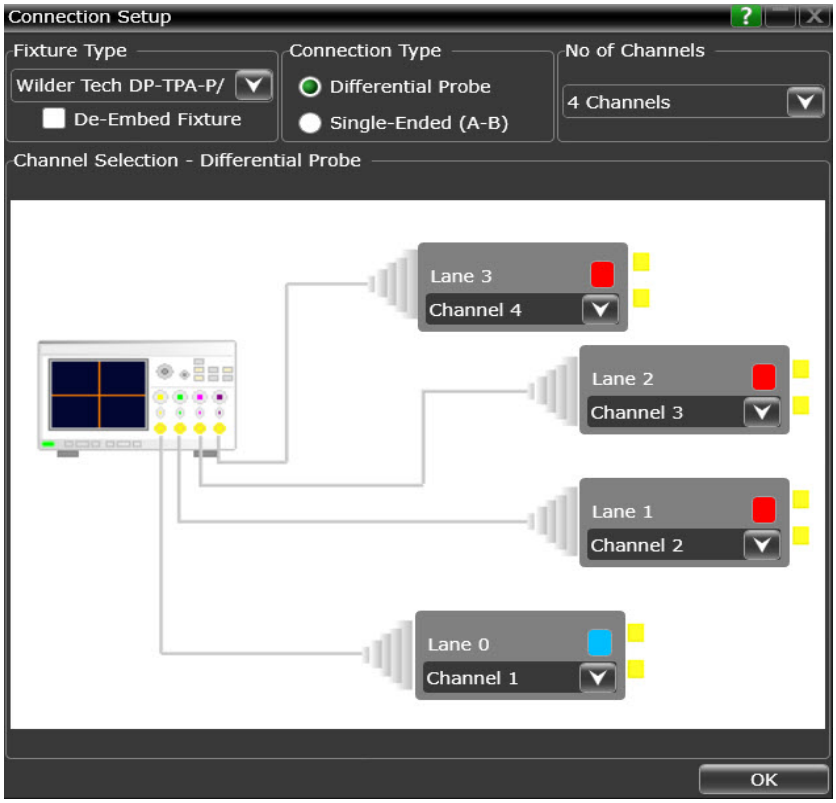
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

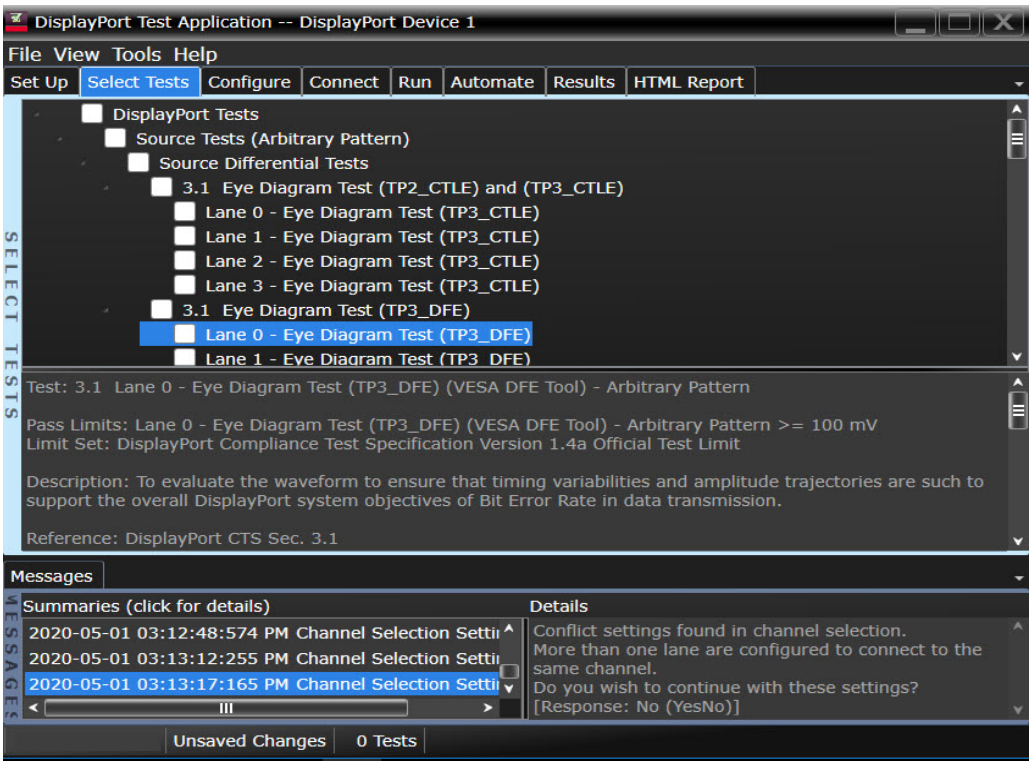
Test Conditions for Eye Diagram Test (TP3_DFE)

Test Parameter	Condition
Test Point	TP3_DFE
Bit Rate	HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any Voltage Level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	TPS4
Cable Model	“Worst Case”

NOTE The Eye Diagram Test (TP3_DFE) will only run if the Eye Diagram Test (TP3_CTLE) fails. The user must manually download the VESA DP Eye Test tool from VESA website.


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Arbitrary Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure for HBR3

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_DFE): Use “Worst Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”, exclude the DFE.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Sweep the CTLE DC gain to generate different equalized signal
   a Generate the recovered clock for the given equalized signal.
   b Save both the waveform for equalized signal and recovered clock.
5 Load all the waveforms into the VESA DP Eye Test Tool and generate the eye height and eye width for different CTLE DC gain with DFE.
6 Report the optimum CTLE DC gain that will generate the highest eye height at TP3_DFE and measurement result.

PASS Condition

Eye Height at TP3_DFE with optimum CTLE DC Gain >= 100 mV

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1*, Section 3.1

Expected/Observable Results

The measured eye height for the optimum CTLE DC gain shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

Source Total Jitter Test (TP3_EQ)

Test ID

For Standard DP Pattern:

- 1225001, 1225002, 1225003, 1225004 – Total Jitter Test (TP3_EQ) - PRBS 7
- 1225011, 1225012, 1225013, 1225014 – Total Jitter Test with No Cable Model (TP3_EQ) - PRBS 7
- 1222001, 1222002, 1222003, 1222004 – Total Jitter Test (TP3_EQ) - HBR2CPAT
- 1222011, 1222012, 1222013, 1222014 – Total Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1221001, 1221002, 1221003, 1221004 – Total Jitter Test (TP3_EQ) - D10.2
- 1221011, 1221012, 1221013, 1221014 – Total Jitter Test with No Cable Model (TP3_EQ) - D10.2

For Arbitrary Pattern:

- 1322001, 1322002, 1322003, 1322004 – Total Jitter Test (TP3_EQ)
- 1322011, 1322012, 1322013, 1322014 – Total Jitter Test with No Cable Model (TP3_EQ)

Test Overview

The objective of this test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

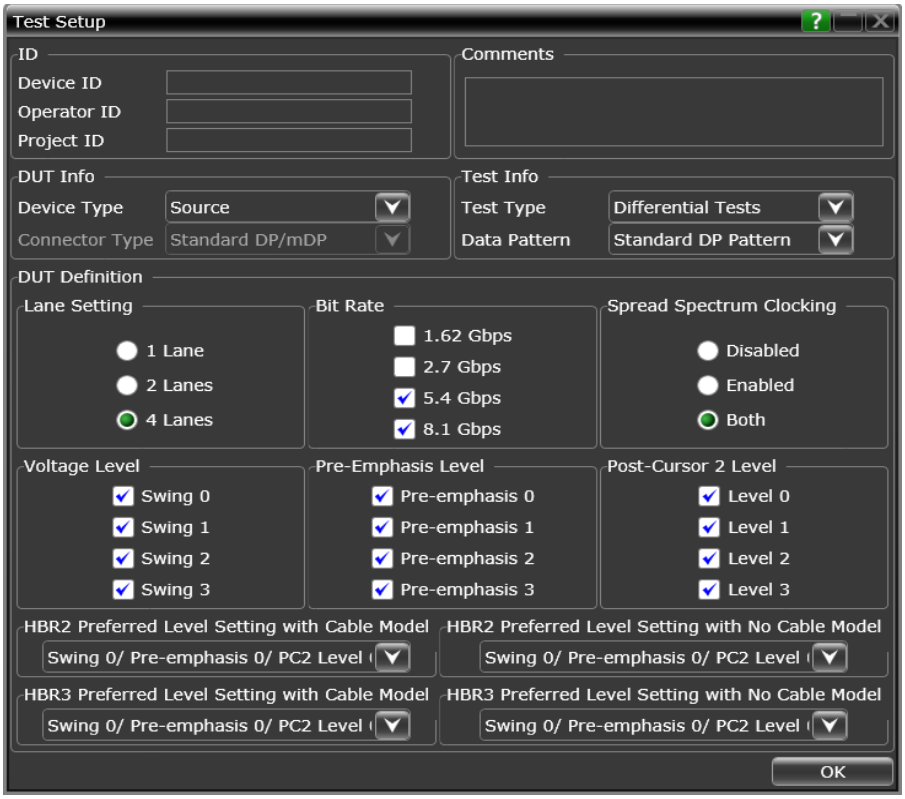
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

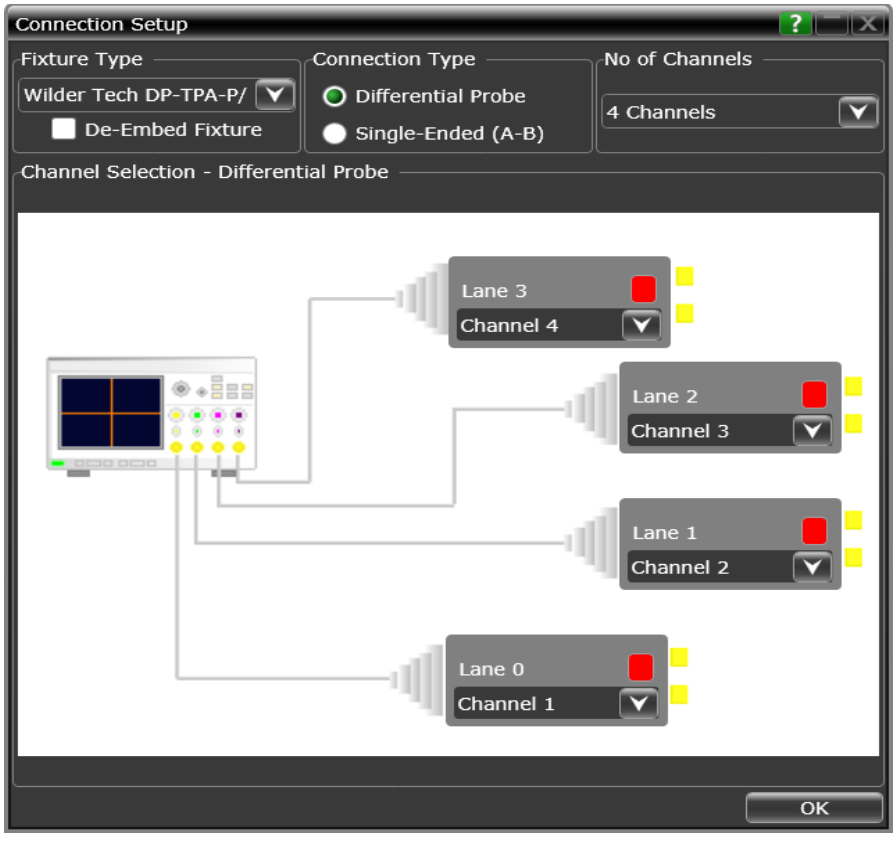
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

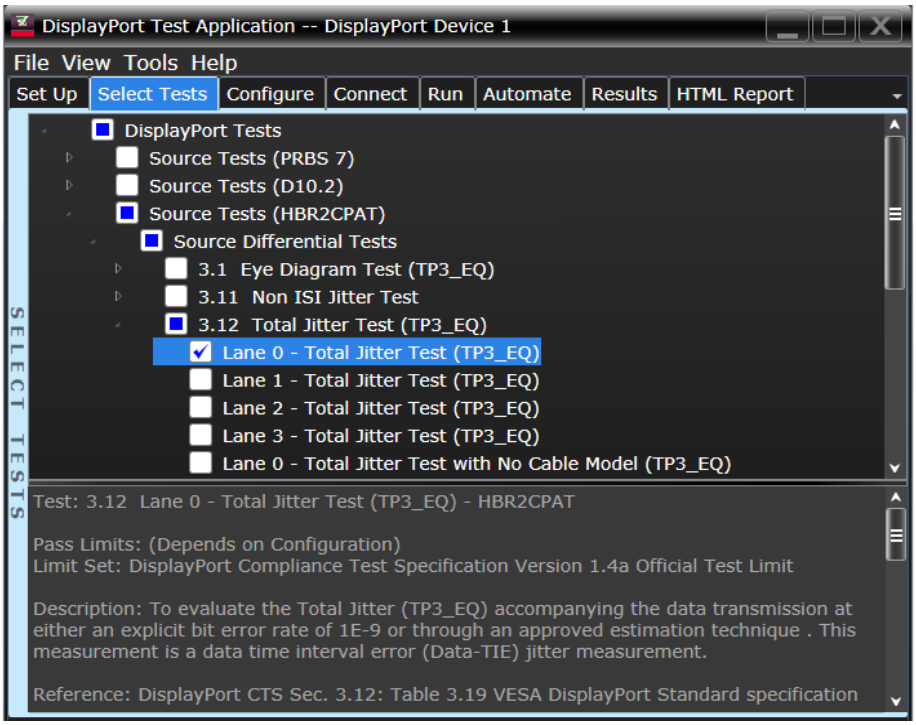
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR (Informative) and HBR2
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	HBR: PRBS 7, HBR2: D10.2, and HBR2CPAT
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Total Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Total Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 2 million UI edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 68 Total Jitter at TP3_EQ

	Receiver Connector (TP3_EQ)
High-Bite Rate 2 (5.4 Gb/s per lane) - for D10.2 pattern	
A_{p-p}	≤ 0.40 UI
High-Bit Rate 2 (5.4 Gb/s per lane) - for HBR2CPAT (or CP2520) pattern	
A_{p-p}	≤ 0.580 UI*
High-Bite Rate (2.7 Gb/s per lane) - for PRBS7	
A_{p-p}	≤ 0.491 UI

The HBR2 limits for Total Jitter calculated at TP3_EQ include a de-rating of 0.04 UI to account for cable crosstalk effect.

UI is Unit Interval.

Test References

See:

For HBR (PRBS7)

- VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.1
- VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2.7.2, Table 3-23.

For HBR2 (HBR2CPAT)

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.1*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-24.*

For HBR2 (D10.2)

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.3*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*

Expected/Observable Results

The measured total jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Total Jitter Test (TP2_CTLE (Informative) and TP3_CTLE)

Test ID

For Standard DP Pattern:

- 1223001, 1223002, 1223003, 1223004 – Total Jitter Test (TP3_CTLE) - TPS4
- 1223011, 1223012, 1223013, 1223014 – Total Jitter Test (TP2_CTLE) - TPS4

For Arbitrary Pattern:

- 1323001, 1323002, 1323003, 1323004 – Total Jitter Test (TP3_CTLE)
- 1323011, 1323012, 1323013, 1323014 – Total Jitter Test (TP2_CTLE)

Test Overview

The objective of this test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-6} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

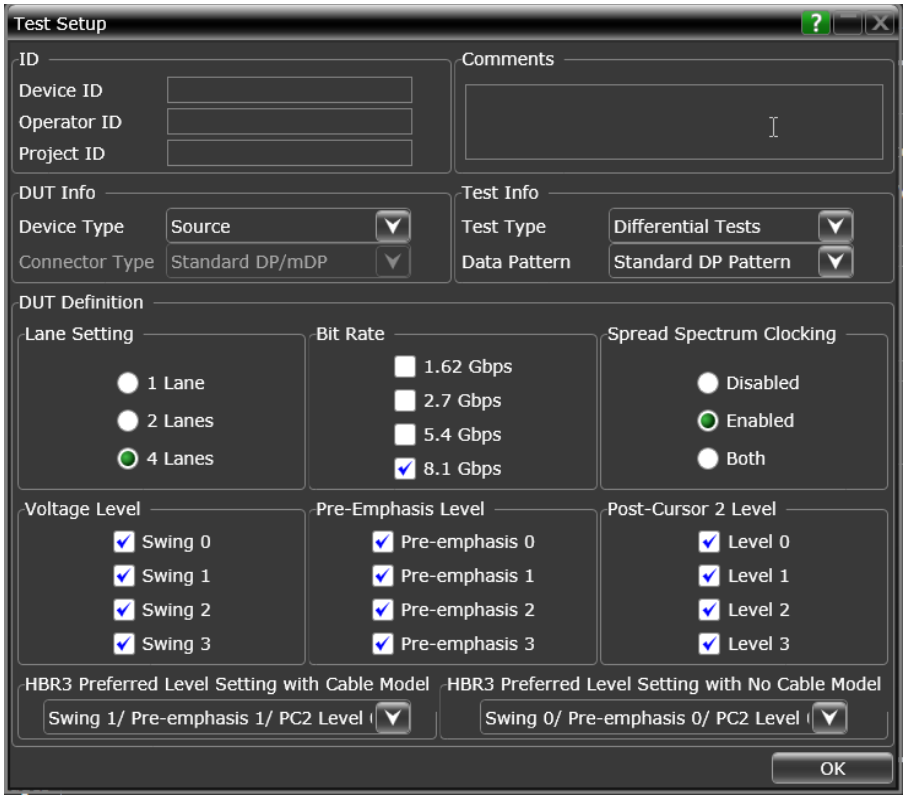
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-6} BER based on the Dual-Dirac Model:

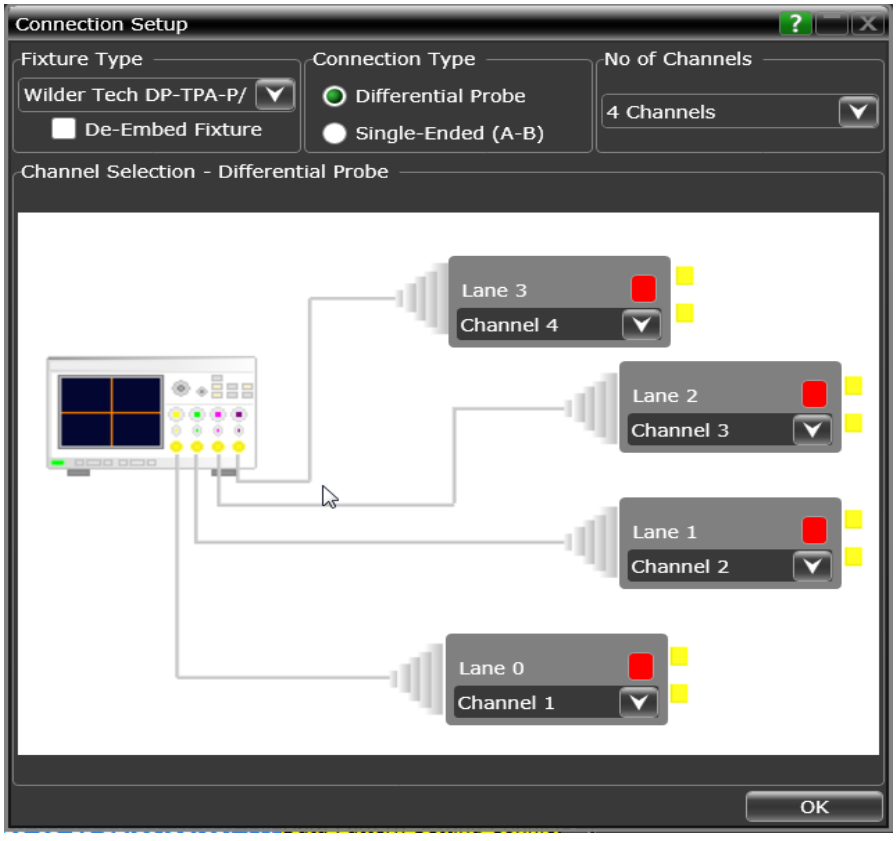
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

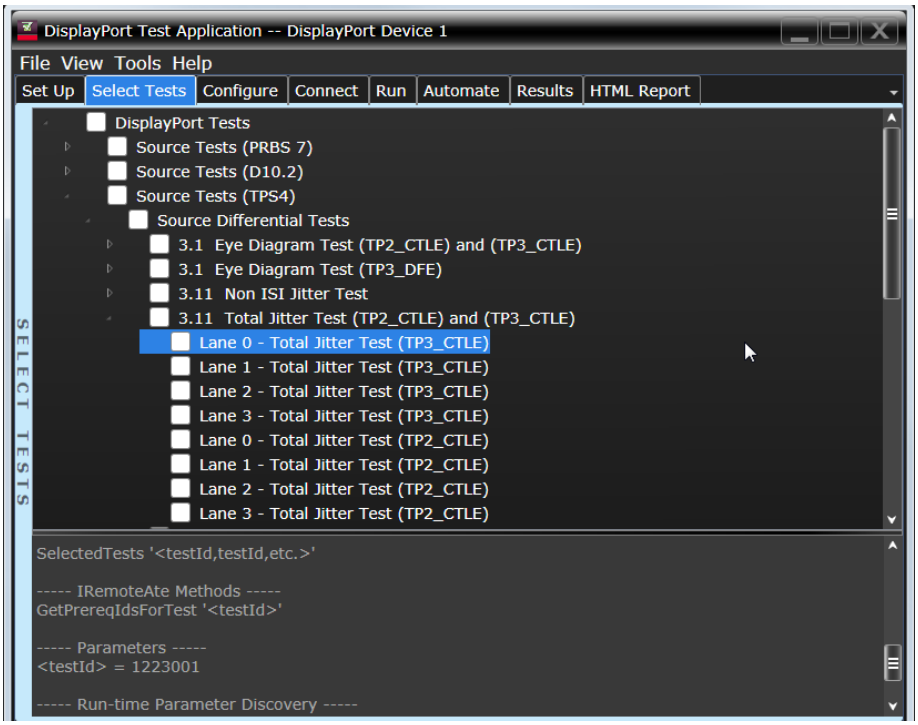
where,
DJ is the Deterministic Jitter and RJ is the Random Jitter.

Test Conditions for Total Jitter Test (TP2_CTLE and TP3_CTLE)

Test Parameter	Condition
Test Point	HBR3: TP3_CTLE HBR3: TP2_CTLE (Informative)
Bit Rate	HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	TPS4
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Total Jitter Test (TP3_CTLE): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Total Jitter Test (TP2_CTLE): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”, exclude the DFE.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 2 million UI edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 69 Total Jitter at TP3_CTLE

	Receiver Connector
High-Bite Rate 3 (8.1 Gb/s per lane)	
A_{p-p}	≤ 0.47 UI

Table 70 Total Jitter at TP2_CTLE

	Receiver Connector (TP2_CTLE)
High-Bit Rate 3 (8.1 Gb/s per lane)	
A_{p-p}	≤ 0.33 UI

UI is Unit Interval.

Test References

See:

For HBR3 (TPS4 pattern)

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.1*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-23*

Expected/Observable Results

The measured total jitter for the test signal at TP3_CTLE and TP2_CTLE shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non ISI Jitter Test (TP2_CTLE (Informative) and TP3_CTLE)

Test ID

For Standard DP Pattern:

- 1234001, 1234002, 1234003, 1234004 – Non ISI Jitter Test (TP3_CTLE) - TPS4
- 1234011, 1234012, 1234013, 1234014 – Non ISI Jitter Test (TP2_CTLE) - TPS4

For Arbitrary Pattern:

- 1334001, 1334002, 1334003, 1334004 – Non ISI Jitter Test (TP3_CTLE)
- 1334011, 1334012, 1334013, 1334014 – Non ISI Jitter Test (TP2_CTLE)

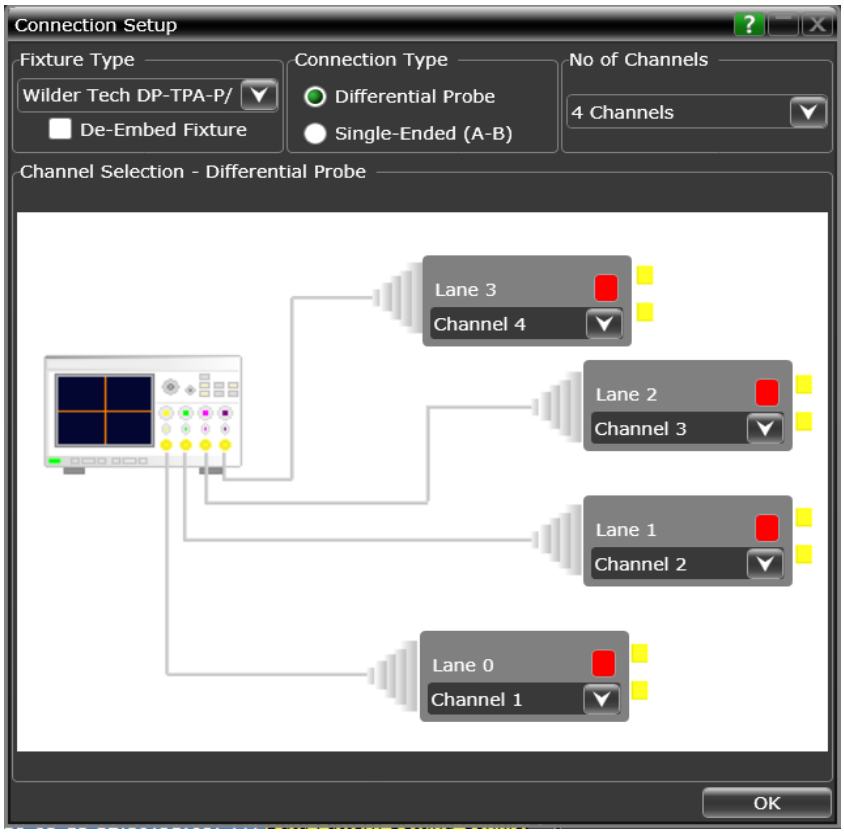
Test Overview

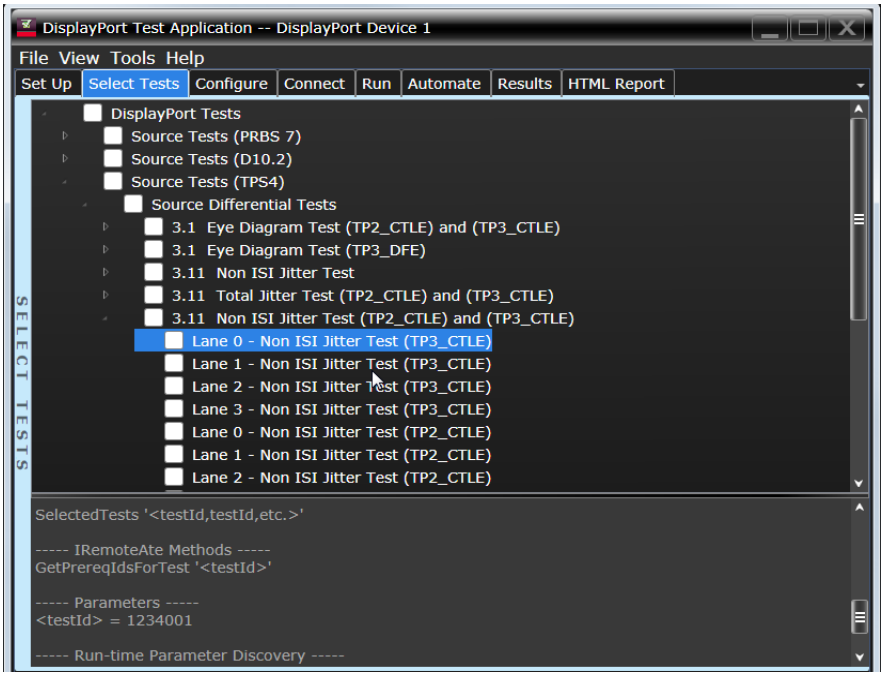
The objective of this test is to evaluate the non ISI jitter accompanying the data transmission.

Test Conditions for Non ISI Jitter Test (TP2_CTLE and TP3_CTLE)

Test Parameter	Condition
Test Point	TP2_CTLE (Informative) and TP3_CTLE
Bit Rate	HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	TPS4
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Non ISI Jitter Test (TP3_CTLE): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Non ISI Jitter Test (TP2_CTLE): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”, exclude the DFE.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 2 million UI edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.

7 Calculate the non ISI jitter base on following equation:
Non ISI Jitter = TJ - ISI

8 Report the measurement results.

PASS Condition

Table 71 Non ISI Jitter at TP3_CTLE

	Receiver Connector (TP3_CTLE)
High-Bit Rate 3 (8.1 Gb/s per lane)	
A_{p-p}	≤0.23 UI

Table 72 Non ISI Jitter at TP2_CTLE

	Receiver Connector (TP2_CTLE)
High-Bit Rate 3 (8.1 Gb/s per lane)	
A_{p-p}	≤0.23 UI

UI is Unit Interval.

See:

- VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.2
- VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-23

Expected/Observable Results

The measured non ISI jitter for the test signal at TP2_CTLE and TP3_CTLE shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Deterministic Jitter Test (TP3_EQ)

Test ID

For Standard DP Pattern:

- 1236001, 1236002, 1236003, 1236004 — Deterministic Jitter Test (TP3_EQ) - HBR2CPAT
- 1236011, 1236012, 1236013, 1236014 — Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1235001, 1235002, 1235003, 1235004 — Deterministic Jitter Test (TP3_EQ) - D10.2
- 1235011, 1235012, 1235013, 1235014 — Deterministic Jitter Test with No Cable Model (TP3_EQ) - D10.2

For Arbitrary Pattern:

- 1336001, 1336002, 1336003, 1336004 — Deterministic Jitter Test (TP3_EQ)
- 1336011, 1336012, 1336013, 1336014 — Deterministic Jitter Test with No Cable Model (TP3_EQ)

Test Overview

The objective of this test is to evaluate the deterministic jitter accompanying the data transmission. The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

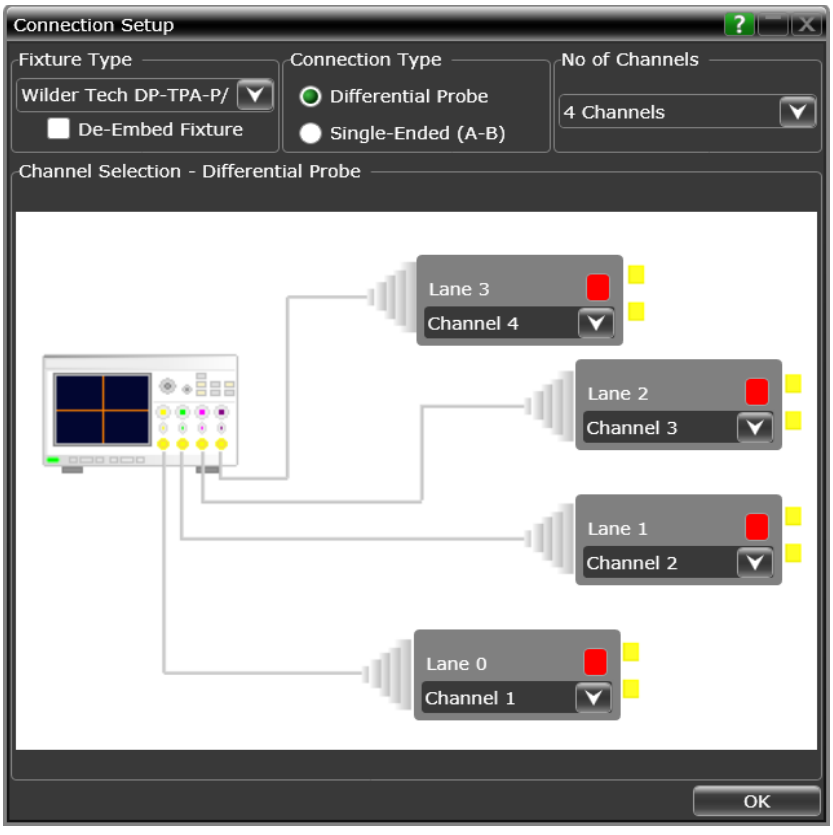
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

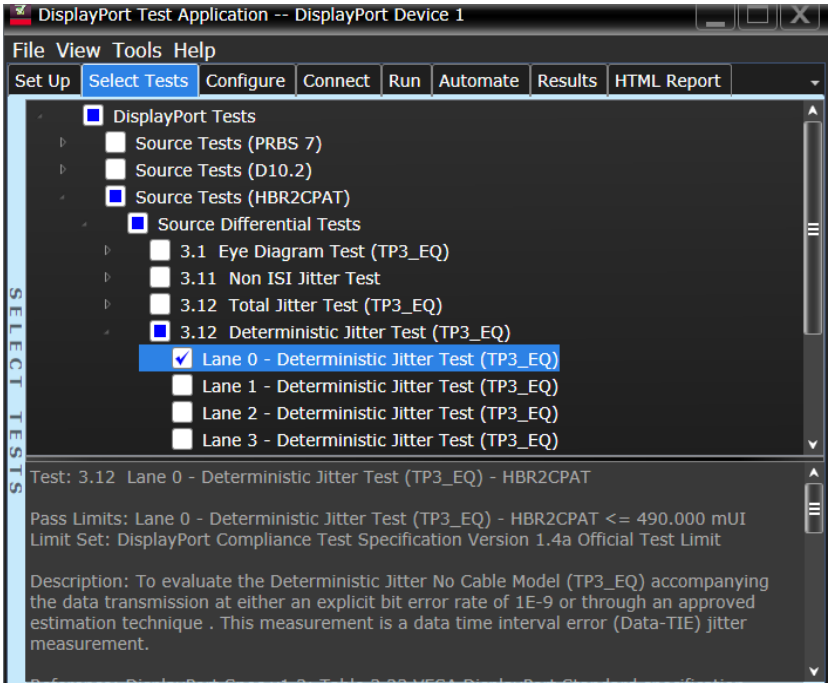
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Deterministic Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Deterministic Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Deterministic Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 2 million UI edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 73 Deterministic Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	≤ 0.49 UI

Table 74 Deterministic Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	≤ 0.27 UI

UI is Unit Interval.

Test References

See:

For HBR2CPAT

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*

For D10.2

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.3*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*

Expected/Observable Results

The measured deterministic jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Random Jitter Test (TP3_EQ)

Test ID

For Standard DP Pattern:

- 1238001, 1238002, 1238003, 1238004 – Random Jitter Test (TP3_EQ) - D10.2
- 1238011, 1238012, 1238013, 1238014 – Random Jitter Test with No Cable Model (TP3_EQ) - D10.2

For Arbitrary Pattern:

- 1338001, 1338002, 1338003, 1338004 – Random Jitter Test (TP3_EQ)
- 1338011, 1338012, 1338013, 1338014 – Random Jitter Test with No Cable Model (TP3_EQ)

Test Overview

The objective of this test is to evaluate the random jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. The jitter is separated into each jitter components and the random jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

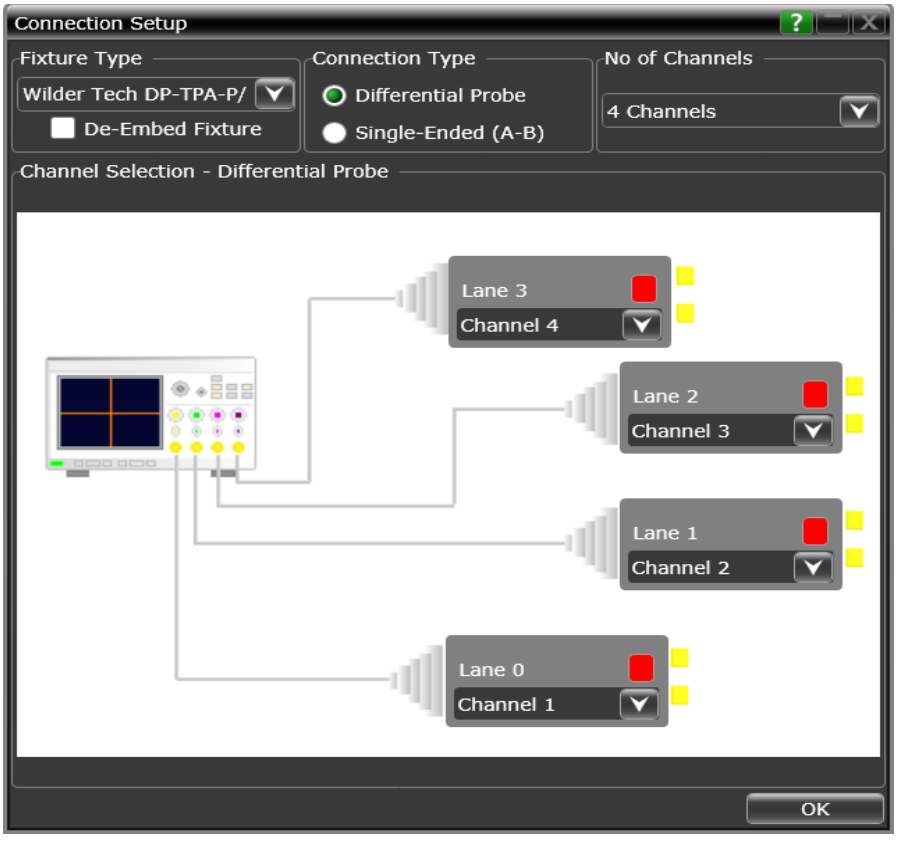
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

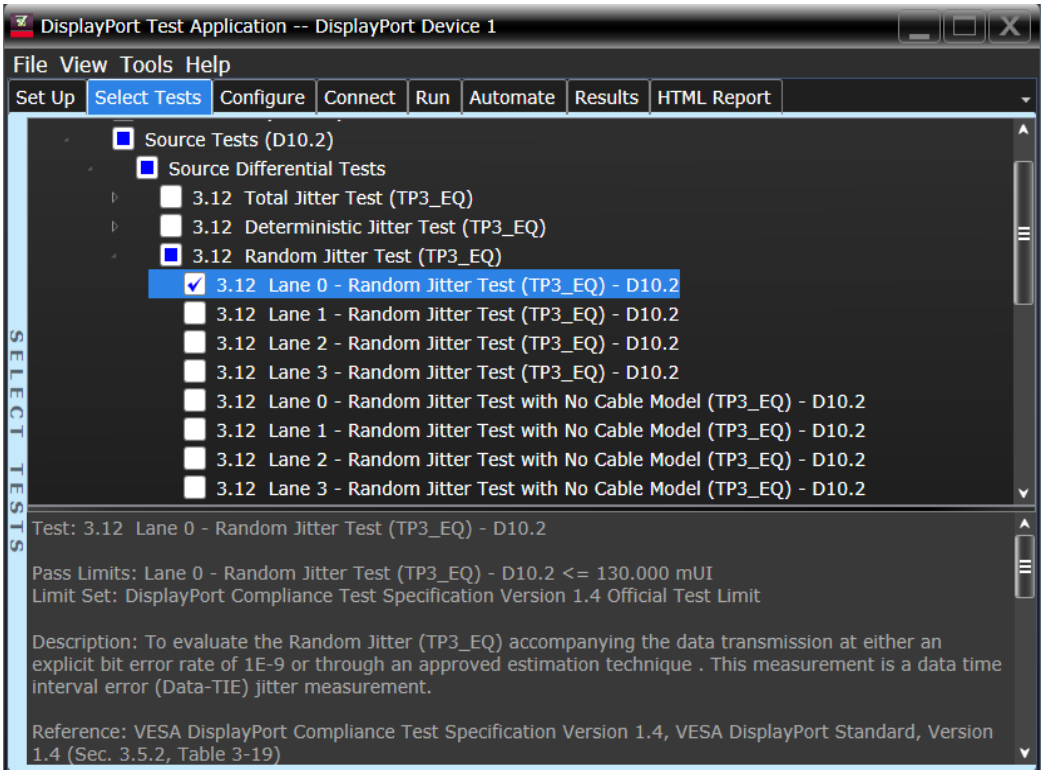
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Random Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	D10.2
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Random Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Random Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 2 million UI edges are analyzed.

6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 75 Random Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.2304 UI*

UI is Unit Interval.
* Calculated based on RJ_{rms} = 19.2 mUI

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.3*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*
- VESA DisplayPort (DP) *Standard Version 1.4*a, HBR2 Rj SCR

Expected/Observable Results

The measured random jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Low Frequency Uncorrelated Deterministic Jitter Test (Informative)

Test ID

For Standard DP Pattern:

- 1239001, 1239002, 1239003, 1239004 – Low Frequency Uncorrelated Deterministic Jitter Test (Informative)

For Arbitrary Pattern:

- 1339001, 1339002, 1339003, 1339004 – Low Frequency Uncorrelated Deterministic Jitter Test (Informative)

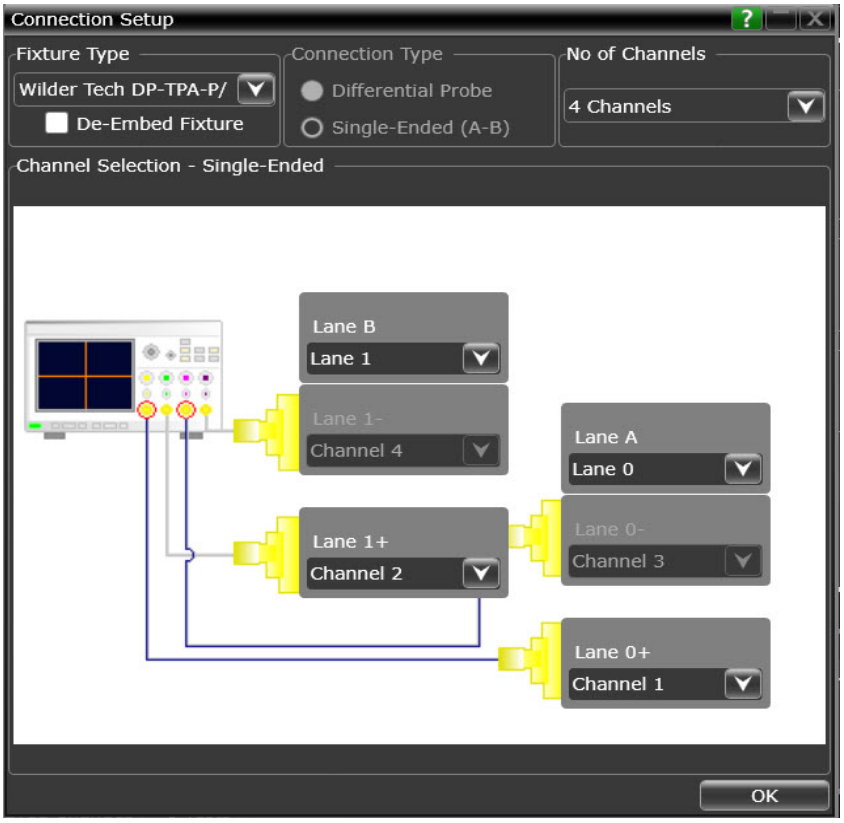
Test Overview

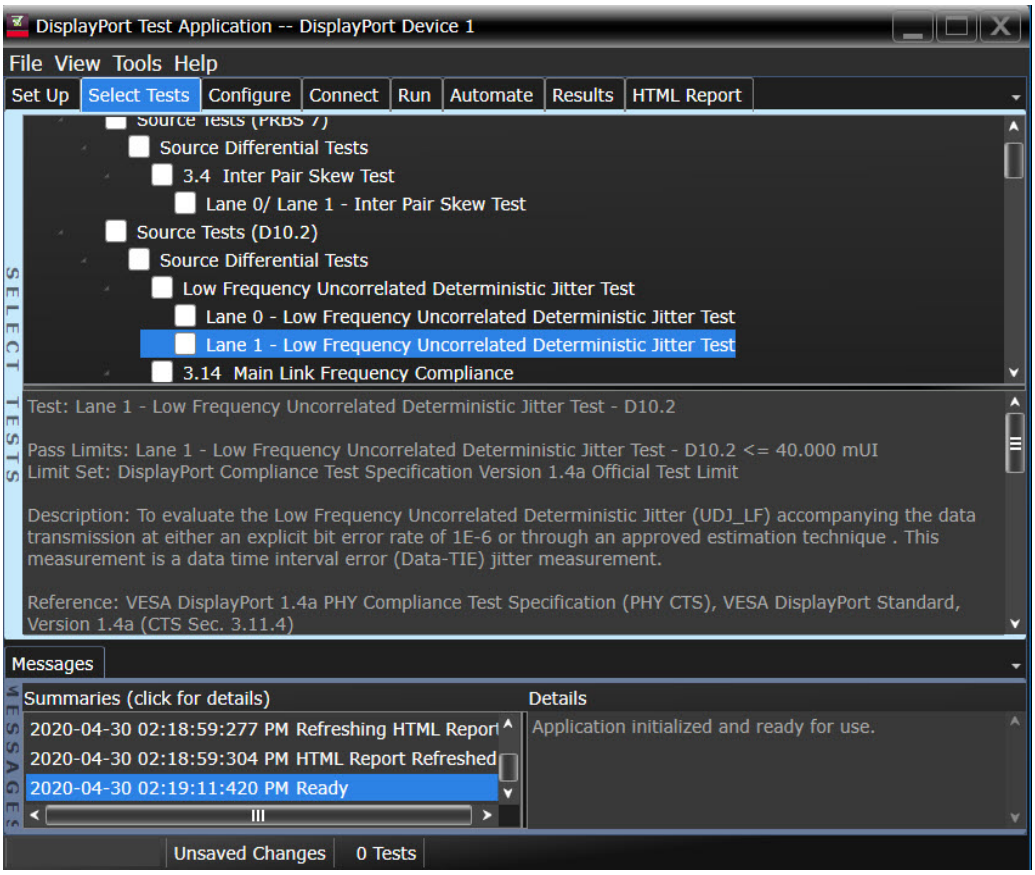
The objective of this test is to confirm that the transmitter low frequency uncorrelated deterministic jitter falls within the limits.

Test Conditions Low Frequency Uncorrelated Deterministic Jitter Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any Voltage Level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Both
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



NOTE

Acquisition length is set to capture 10 cycles of SSC at 30KHz. For 80 GSa/s sample rate, acquisition length shall be set to 27 MSa. For 100 GSa/s sample rate, acquisition length shall be 34 MSa.

The recommended maximum memory depth for UXR oscilloscope is 48M and for 90000 series and others is 30M.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.

4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Apply low pass filter (2^{nd} order, 3 dB cut-off at 500 KHz) to TIE data
   c UDJ_LF = measured TJ after low pass filter applied
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Report the measurement results. UDJ_LF is the measured TJ after applying low pass filter.

PASS Condition

Table 76 Low Frequency Uncorrelated Deterministic Jitter at Internal and Compliance Points.

	Transmitter Connector (TP2)
High-bit Rate (8.1 Gb/s per lane)	
$A_{p\text{-}pTX}$	40.0 mUI

UI stands for Unit Interval.

Test References

See:

- VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.4.

Expected/Observable Results

The measured low frequency uncorrelated deterministic jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source AC Common Mode Test (Informative)

Test ID

For Standard DP Pattern:

- 12110001, 12110002, 12110003, 12110004 – AC Common Mode Test (Informative)

For Arbitrary Pattern:

- 13110001, 13110002, 13110003, 13110004 – AC Common Mode Test (Informative)

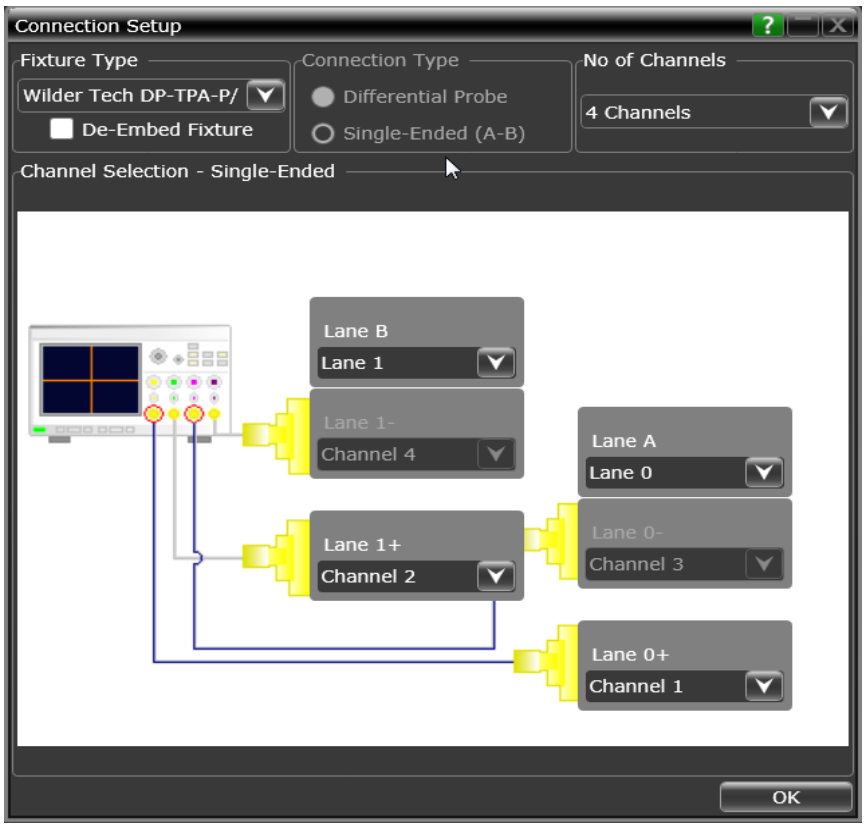
Test Overview

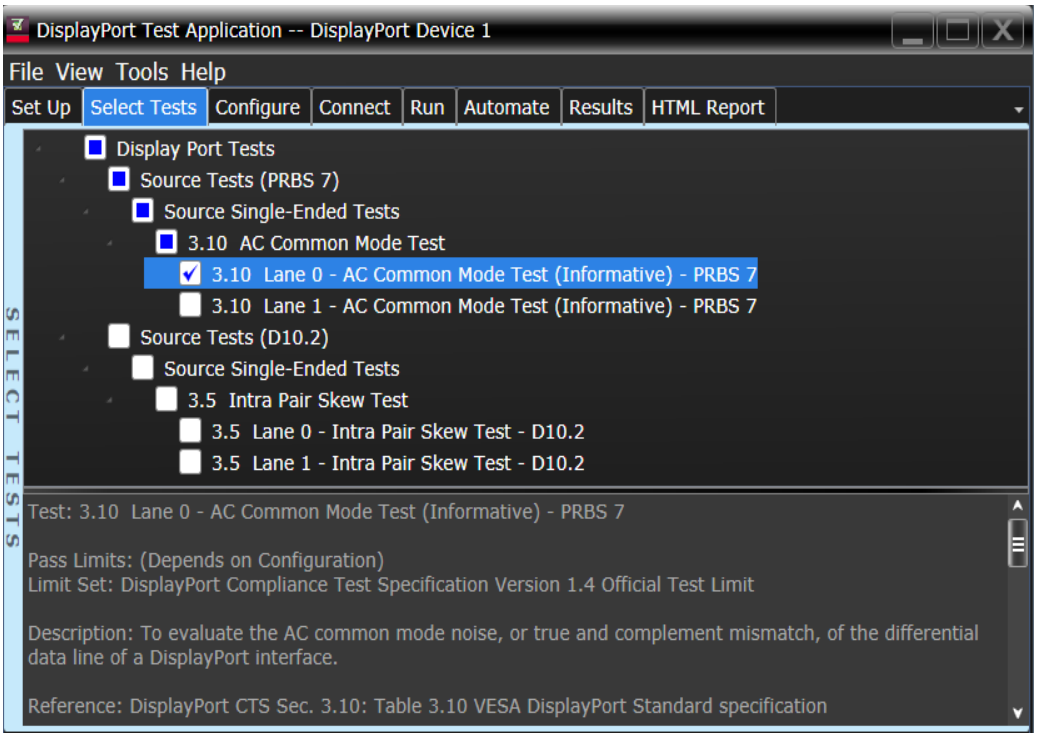
The objective of this test is to evaluate the AC Common Mode noise (unfiltered rms) of the differential data line of the DP interface.

Test Conditions for AC Common Mode Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR, and HBR2
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC enabled only.
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels supported subject to the constraints in Table 3-2 of the VESA DisplayPort 1.4a Standard
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Single-Ended Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Create FUNC3 signal, which is the common mode signal of the input single-ended signal.
4 If the filter is enabled ["Filter" configuration variable set to "High Pass Filter", "Low Pass Filter" or "None" (Default)]:
   a Create FUNC4 signal, which is the filtered FUNC3 signal by applying the High Pass filter or Low Pass filter on the FUNC3 signal based on the Configuration Variable.
5 Set up two display grids such that one grid displays the input single-ended signal while the other grid displays the common mode signal.
6 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
7 Set up the parameters for RMS voltage measurement of the common mode signal.
   a Set up the V_{rms} measurement for the common mode signal.
   b Acquire the signal until 100,000 edges are measured.

8 Get the mean for the V_{rms} measurement.

9 Report the measurement results.

PASS Condition

For RBR and HBR:

AC Common Mode Voltage $\leq$ 20mV

For HBR2:

AC Common Mode Voltage $\leq$ 30mV

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.8.2*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section D.2, Table D-3*

Expected/Observable Results

The measured AC common mode noise for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source AC Common Mode Test (Informative - HBR3)

Test ID

For Standard DP Pattern:

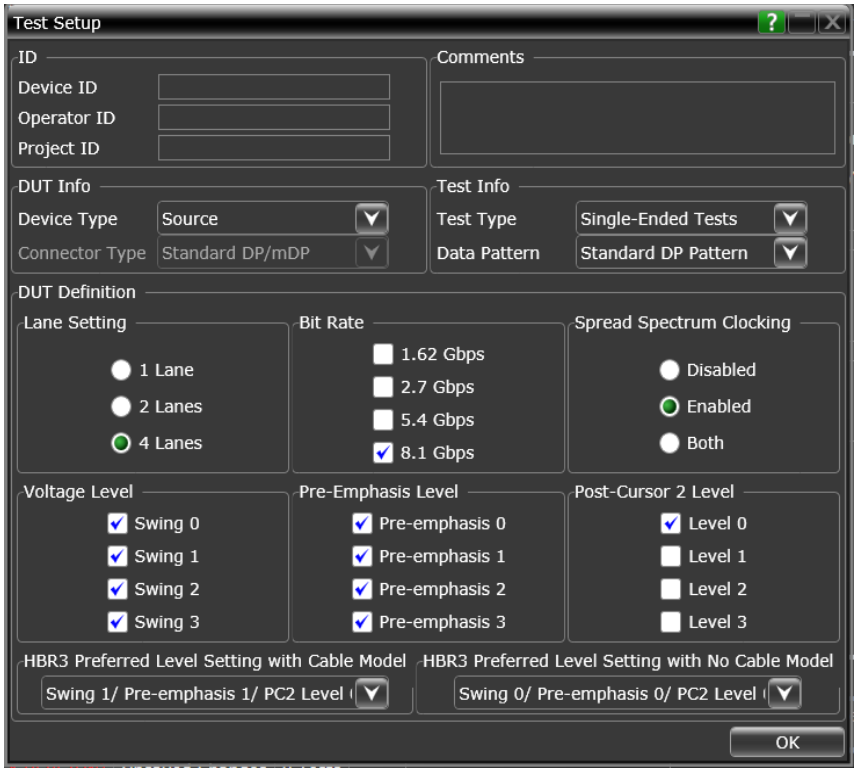
- 12110011, 12110012, 12110013, 12110014 – AC Common Mode Test (Informative)

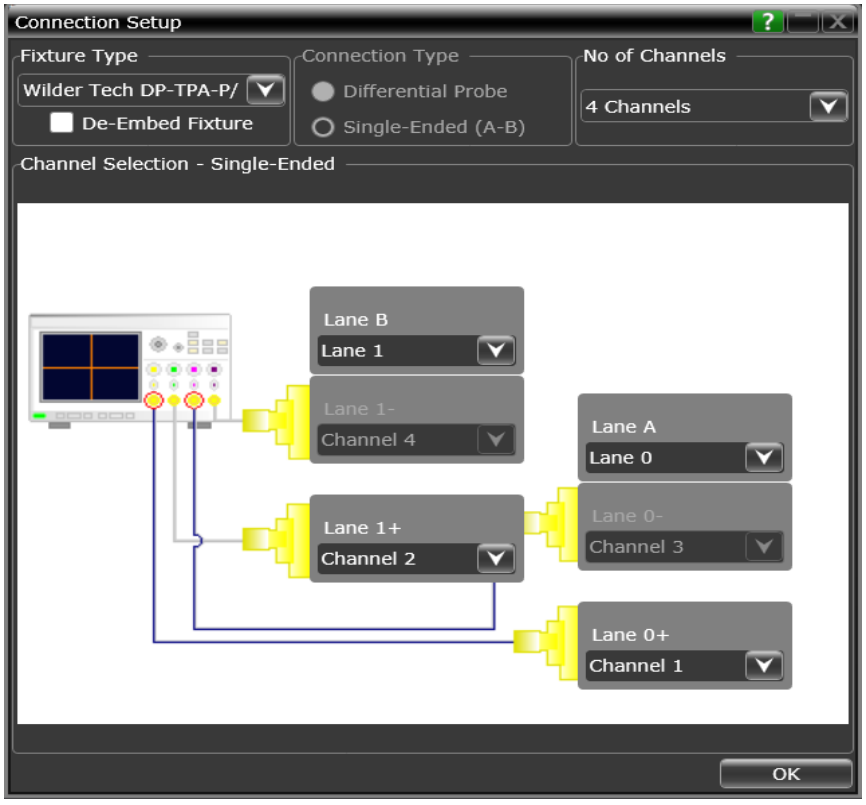
Test Overview

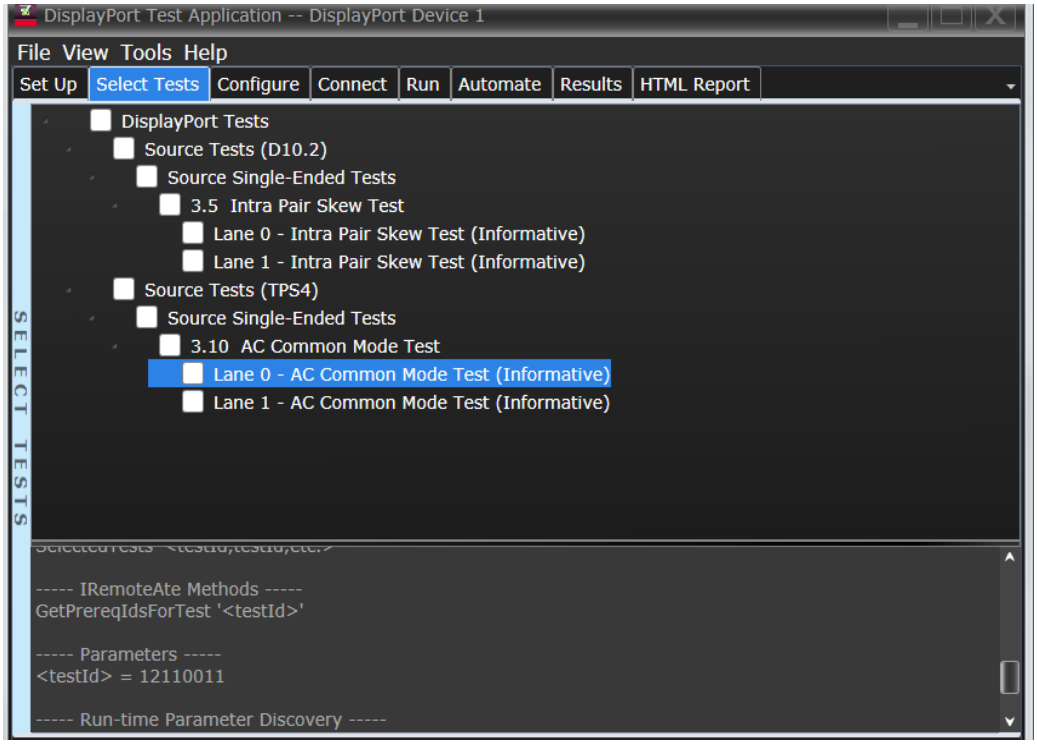
The objective of this test is to evaluate the AC Common Mode noise (unfiltered RMS) of the differential data line of the DP interface.

Test Conditions for AC Common Mode Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	HBR3 - Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	HBR3 - Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes are supported
Test Pattern	TPS4


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Single-Ended Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Create FUNC3 signal, which is the common mode signal of the input single-ended signal.
4 If the filter is enabled [“Filter” configuration variable set to “High Pass Filter”, “Low Pass Filter” or “None” (Default)]:
   a Create FUNC4 signal, which is the filtered FUNC3 signal by applying the High Pass filter or Low Pass filter on the FUNC3 signal based on the Configuration Variable.
5 Set up two display grids such that one grid displays the input single-ended signal while the other grid displays the common mode signal.
6 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
7 Set up the parameters for Peak to Peak voltage measurement of the common mode signal.
   a Set up the V_{pk-pk} measurement for the common mode signal.
   b Acquire the signal until 100,000 edges are measured.

8 Get the mean for the V_{pk-pk} measurement.

9 Report the measurement results.

PASS Condition

For HBR3:

AC Common Mode Voltage < 100 mV_{pk-pk}

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.8.1*

Expected/Observable Results

The measured AC common mode noise for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Intra-Pair Skew Test (Informative)

Test ID

For Standard DP Pattern:

- 12100001, 12100002, 12100003, 12100004 – Intra-Pair Skew Test (Informative)

For Arbitrary Pattern:

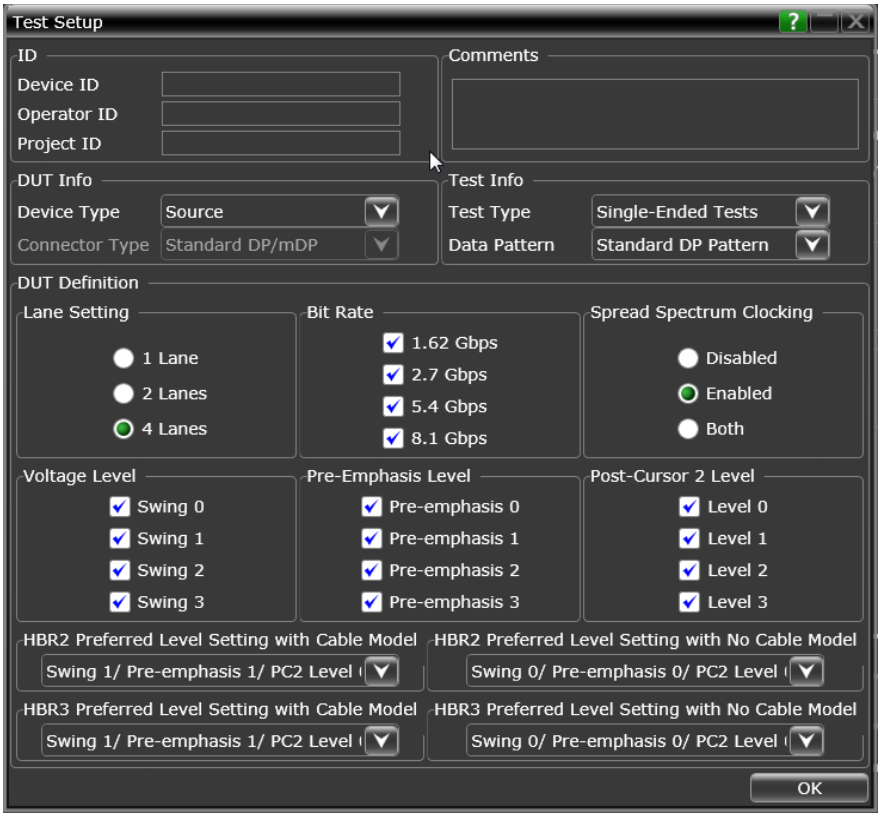
- 13100001, 13100002, 13100003, 13100004 – Intra-Pair Skew Test (Informative)

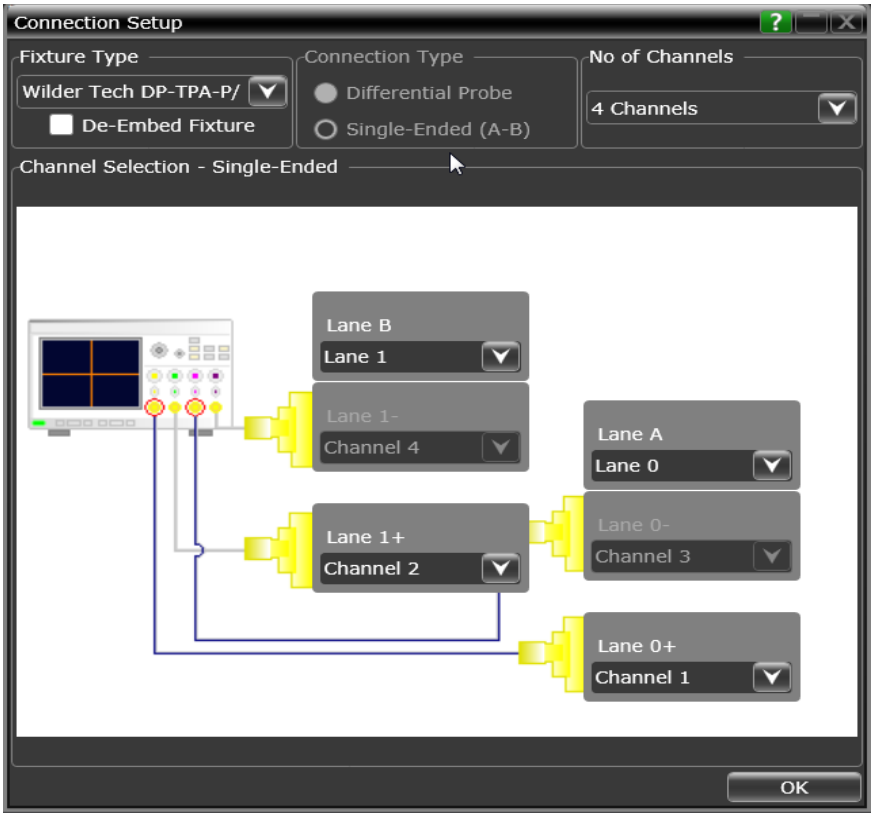
Test Overview

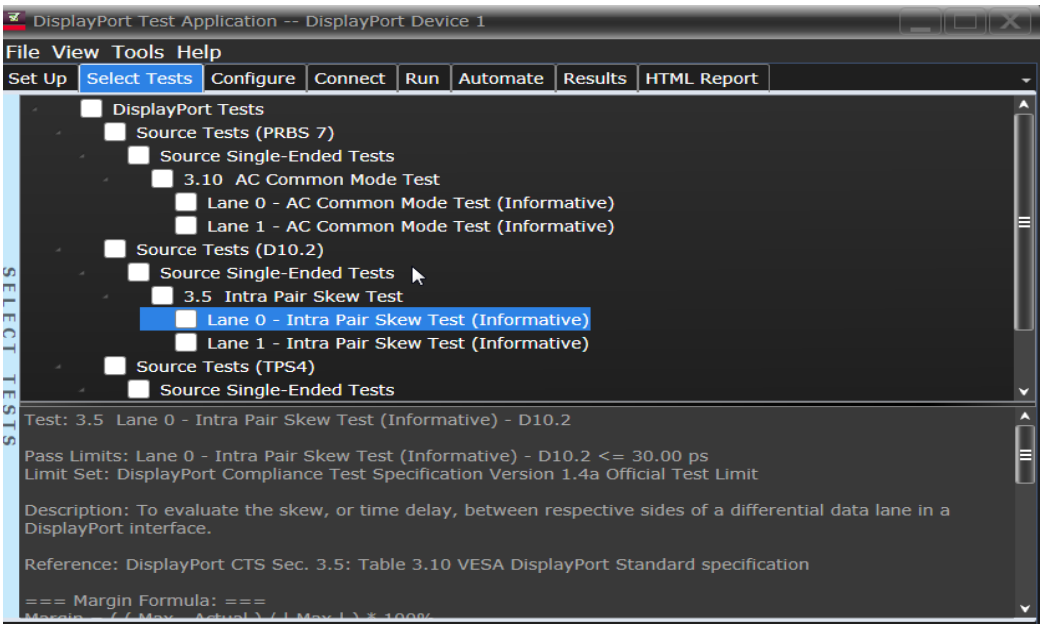
The objective of this test is to evaluate the skew or time delay between respective sides of a differential data lane in the DP interface.

Test Conditions for Intra-Pair Skew Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR3)
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported For one lane operation: Lane 0+ to Lane 0- For two lane operation: Lane 0+ to Lane 0- Lane 1+ to Lane 1- For four lane operation: Lane 0+ to Lane 0- Lane 1+ to Lane 1- Lane 2+ to Lane 2- Lane 3+ to Lane 3-
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Single-Ended Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
4 Set up the parameters to perform High Level Voltage (V_{HIGH}) and Low Level Voltage (V_{LOW}) for each input single-ended signal.
   a Scale the vertical display of the input single-ended signal to optimum value.
   b Acquire the signal for 100 waveforms.
   c Find V_{HIGH} by measuring the average voltage at 0.06 UI to 0.75 UI of the High Level.
   d Find V_{LOW} by measuring the average voltage at 0.06 UI to 0.75 UI of the Low Level.
   e Calculate the Transition Voltage (V_{Trans}) using the equation:

$$V_{Trans} = (V_{HIGH} + V_{LOW}) / 2$$

5 Set up the parameters for the intra-pair skew measurement:

a Set up the measurement threshold for each single-ended data signal based on the measured Transition Voltage.

b Set up InfiniiScan to trigger on the desired pattern.

c Set up delta time measurement to measure time difference between the rising edge of the data true signal (D+) and the complement's (D-) falling edge:

$$D+_{Transition\_High} - D-_{Transition\_Low}$$

d Set up delta time measurement to measure time difference between the falling edge of the data true signal (D+) and the complement's (D-) rising edge:

$$D+_{Transition\_Low} - D-_{Transition\_High}$$

e Acquire the signal until you measure 100 edges.

f Calculate the intra-pair skew using the equation:

$$\text{Intra-Pair Skew} = \{1/\text{Number of Edges}\}$$

$$\sum \{[(D+_{Transition\_High} - D-_{Transition\_Low}) + (D+_{Transition\_Low} - D-_{Transition\_High})] / 2\}$$

6 Report the measurement results.

PASS Condition

Intra-Pair skew ≤ 30 ps

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.7*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-22*

Expected/Observable Results

The measured intra-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

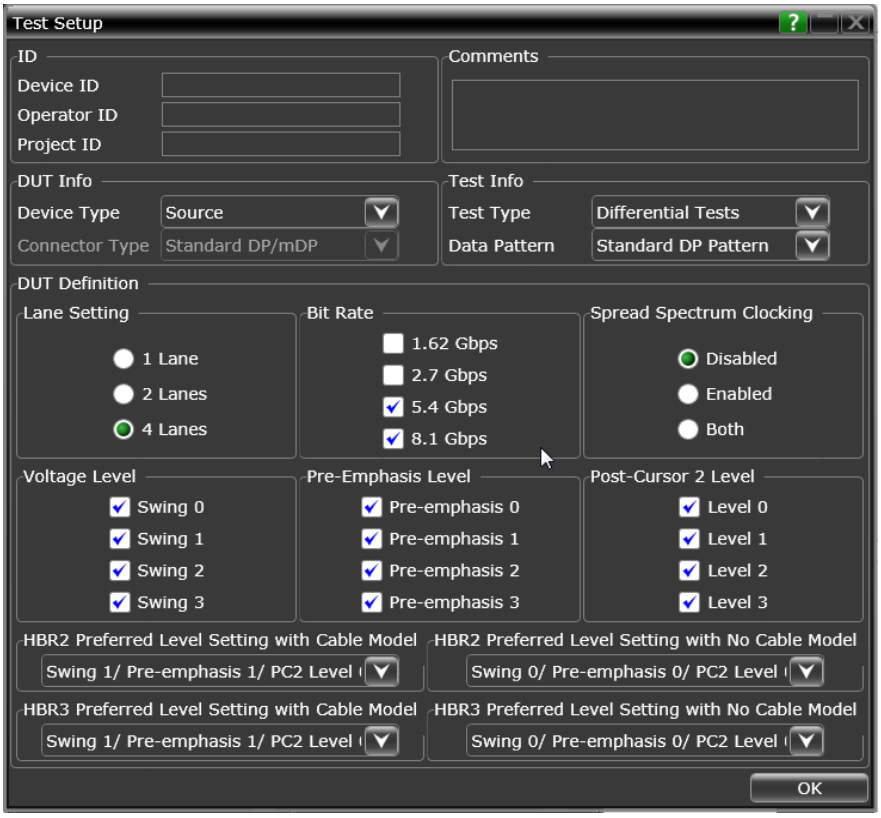
Source Level and Equalization Verification Tests

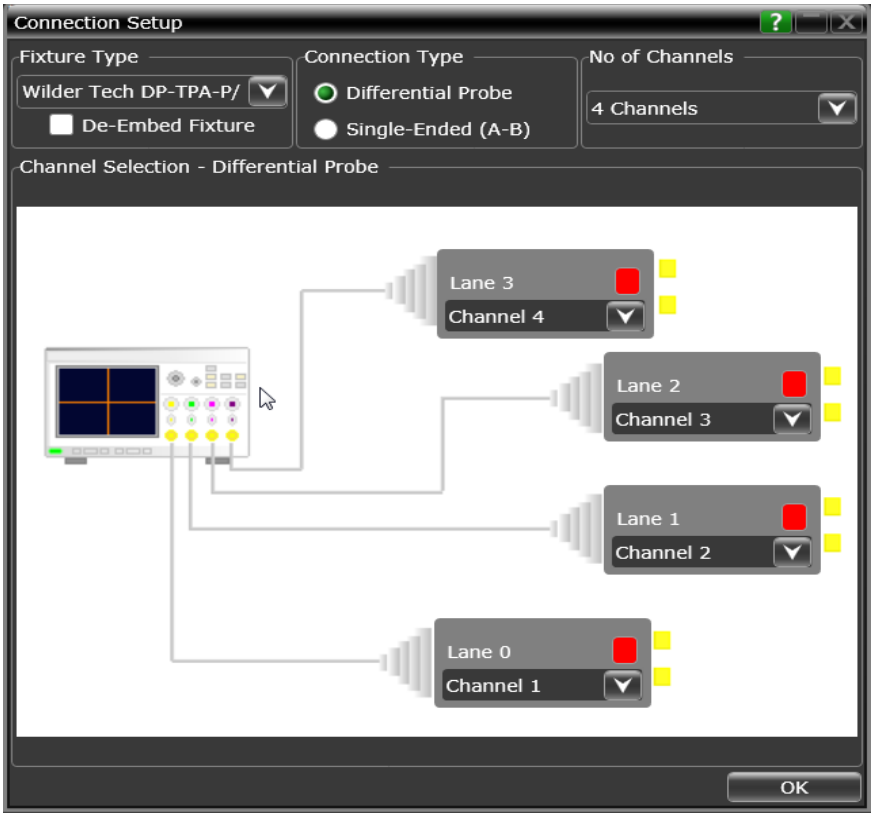
Test Overview

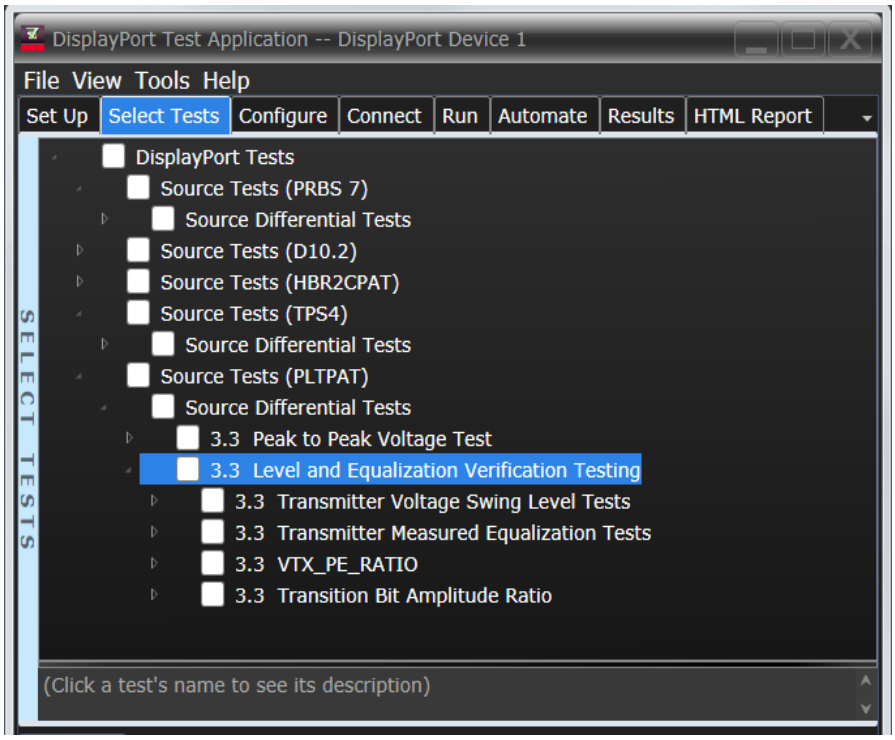
The objective of this test is to ensure that the DUT obeys the system budget also that the Voltage level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by Sink.

Test Conditions for Level and Equalization Verification Tests

Test Parameter	Condition
Test Point	TP2
Bit Rate	HBR2 HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC disabled only.
Voltage Level	VSL[N], Transmitter Voltage Swing Level N, where N = 0,1,2, or 3
Pre-Emphasis Level	TX_EQL[N], Transmitter Equalization Level N, where N = 0,1,2, or 3
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	PLTPAT




Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
DisplayPort Tests
Source Tests (PRBS 7)
Source Differential Tests
Source Tests (D10.2)
Source Tests (HBR2CPAT)
Source Tests (TPS4)
Source Differential Tests
Source Tests (PLTPAT)
Source Differential Tests
3.3 Peak to Peak Voltage Test
3.3 Level and Equalization Verification Testing
3.3 Transmitter Voltage Swing Level Tests
3.3 Transmitter Measured Equalization Tests
3.3 VTX_PE_RATIO
3.3 Transition Bit Amplitude Ratio
(Click a test's name to see its description)

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities>Calibration** menu.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure VTOP and VBASE of the input signal.
   d Measure the data rate of the input signal.
3 Setup the parameter of spectral measurements:
   a Set Sampling Rate at > 40GSa/s.
   b Configure the FFT feature with the following parameters:
      i RBW* - 10 KHz
      ii Detector Type - Average
      iii Start frequency - 500 MHz
      iv Stop frequency - 4.5 GHz
      v Select the **Mark Peaks** check-box
      vi Set Hanning window

* To reduce the test time, the test will run the FFT using 10 kHz RBW by default. If the DUT has a low-frequency SJ that causes inconsistent pass/fail result, user may reduce the RBW to 1 kHz.

4 Set the Source device's output to VSL[0] and TX_AEQ[0], where VSL is the Transmitter Voltage Swing Level and TX_AEQ is Transmitter's Applied Equalization Level.
5 Measure the peak FFT at the fundamental (first) and fifth harmonic levels (in dB) and denote them as f1 and f5.
6 Repeat step 5 to measure f1 and f5 for each value of VSL[0] and valid TX_AEQ[0] to TX_AEQ[3] values. The peak frequencies to obtain the FFT peak f1 and f5 locations are:

Bit Rate	Peak Frequencies	
	f1 (MHz)	f5 (GHz)
HBR3	810	4.05
HBR2	540	2.70

7 Calculate Δf [N] value for each setting of VSL[0] and valid TX_AEQ[0] to TX_AEQ[3] values using the equation: Δf [N] = f1-f5
8 Repeat steps 4 to 7 for all VSL[N] and TX_AEQ[N], where N = 1, 2, or 3.

NOTE Not all combinations of VSL[N] and TX_AEQ[N] are valid to measure the harmonic levels. Refer to Table 77 for the valid combinations of swing level and pre-emphasis levels to derive valid values of Δf [N].

Table 77 FFT 1st and 5th harmonic amplitude (dB) for valid VSL[N] and TX_AEQ[N]

VSL[0]		f1	f5	f1-f5 (Δf [0])
TX_AEQ	P0	Available	Available	Δf [0] at VSL[0] and P0
	P1	Available	Available	Δf [0] at VSL[0] and P1
	P2	Available	Available	Δf [0] at VSL[0] and P2
	P3	Available	Available	Δf [0] at VSL[0] and P3
VSL[1]		f1	f5	f1-f5 (Δf [1])
TX_AEQ	P0	Available	Available	Δf [1] at VSL[1] and P0
	P1	Available	Available	Δf [1] at VSL[1] and P1
	P2	Available	Available	Δf [1] at VSL[1] and P2
	P3	Not Available	Not Available	Not Available
VSL[2]		f1	f5	f1-f5 (Δf [2])
TX_AEQ	P0	Available	Available	Δf [2] at VSL[2] and P0
	P1	Available	Available	Δf [2] at VSL[2] and P1
	P2	Not Available	Not Available	Not Available
	P3	Not Available	Not Available	Not Available
VSL[3]		f1	f5	f1-f5 (Δf [3])
TX_AEQ	P0	Available	Available	Δf [3] at VSL[3] and P0
	P1	Not Available	Not Available	Not Available
	P2	Not Available	Not Available	Not Available
	P3	Not Available	Not Available	Not Available

Transmitter Voltage Swing Level Tests

VTX_OUTPUT_LEVEL0_RATIO (VSL 1/VSL 0)

VTX_OUTPUT_LEVEL0_RATIO (VSL 2/VSL 0)

VTX_OUTPUT_LEVEL0_RATIO (VSL 3/VSL 0)

VTX_OUTPUT_RATIO (VSL 1/VSL 0)

VTX_OUTPUT_RATIO (VSL 2/VSL 1)

VTX_OUTPUT_RATIO (VSL 3/VSL 2)

Test ID

For Standard DP Pattern

1281101, 1281102, 1281103, 1281104 – VTX_OUTPUT_LEVEL0_RATIO (VSL 1/VSL 0) - PLTPAT

1282101, 1282102, 1282103, 1282104 – VTX_OUTPUT_LEVEL0_RATIO (VSL 2/VSL 0) - PLTPAT

1283101, 1283102, 1283103, 1283104 – VTX_OUTPUT_LEVEL0_RATIO (VSL 3/VSL 0) - PLTPAT

1285101, 1285102, 1285103, 1285104 – VTX_OUTPUT_RATIO (VSL 1/VSL 0) - PLTPAT

1286101, 1286102, 1286103, 1286104 – VTX_OUTPUT_RATIO (VSL 2/VSL 1) - PLTPAT

1287101, 1287102, 1287103, 1287104 – VTX_OUTPUT_RATIO (VSL 3/VSL 2) - PLTPAT

Procedure:

1 Perform the procedure for Spectral Measurements as a prerequisite.
2 Ensure that Pre-Emphasis is set to Level 0; that is, measurements are performed with TX_EQL[0].
3 For each value of f1 measured for each VSL[N], as calculated in Table 1, calculate $f1_{VSL[N]}$ - $f1_{VSL[0]}$.
4 Calculate $V_{TX\_OUTPUT\_LEVEL0\_RATIO}$ using the equation:
$V_{TX\_OUTPUT\_LEVEL0\_RATIO}$ = VSL[N] / VSL[0] = $f1_{VSL[N]}$ - $f1_{VSL[0]}$, where N = 1,2 or 3
5 Record each value for $V_{TX\_OUTPUT\_LEVEL0\_RATIO}$ in the following table:

VSL[N] value	Minimum	VSL[N] / VSL[0]	Maximum
1	1.6		4.5
2	3.2		7.0
3	4.8		10.5

6 For each value of f1 measured for each VSL[N], as calculated in Table 1, calculate $f1_{VSL[N]}$ - $f1_{VSL[N-1]}$.
7 Calculate $V_{TX\_OUTPUT\_RATIO}$ using the equation:
$V_{TX\_OUTPUT\_RATIO}$ = VSL[N] / VSL[N-1] = $f1_{VSL[N]}$ - $f1_{VSL[N-1]}$, where N = 1, 2, or 3

8 Record each value for $V_{TX\_OUTPUT\_RATIO}$ in the following table:

VSL[N] value	Minimum	VSL[N] / VSL[N-1]
1	1.6	
2	1.1	
3	1.1	

Pass Condition for Transmitter Voltage Swing Level Tests

Symbol	Parameter	Min.	Max.	Units	Comments
$V_{TX\_OUTPUT\_LEVEL0\_RATIO}$	Ratio of Voltage Swing VSL[1] / VSL[0]	1.6	4.5	dB	▪ Calculated using measured value of 1st harmonic of FFT at TX_EQL[0] ▪ VSL[3] mandatory
	Ratio of Voltage Swing VSL[2] / VSL[0]	3.2	7.0	dB	
	Ratio of Voltage Swing VSL[3] / VSL[0]	4.8	10.5	dB	
$V_{TX\_OUTPUT\_RATIO}$	Ratio of Voltage Swing VSL[1] / VSL[0]	1.6	-	dB	▪ Calculated using measured value of 1st harmonic of FFT at TX_EQL[0] ▪ VSL[3] mandatory
	Ratio of Voltage Swing VSL[2] / VSL[1]	1.1	-	dB	
	Ratio of Voltage Swing VSL[3] / VSL[2]	1.1	-	dB	

Transmitter Measured Equalization Tests

VTX_MEQ_LEVEL0_DELTA

VTX_MEQ_DELTA

Test ID:

For Standard DP Pattern

1291101, 1291102, 1291103, 1291104 – VTX_MEQ_LEVEL0_DELTA - PLTPAT

1295101, 1295102, 1295103, 1295104 – VTX_MEQ_DELTA - PLTPAT

Procedure:

1 Perform the procedure for Spectral Measurements as a prerequisite.

2 Ensure that Pre-Emphasis is set to Level 0; that is, measurements are performed with TX_EQL[0] as reference.

NOTE This test verifies that the TX_EQL[N] values increase monotonically within the specified ranges.

3 For each valid value of VSL[N] and TX_EQL[N] value, calculate $V_{TX\_MEQ\_LEVEL0\_DELTA[N]}$ using the equation:
$V_{TX\_MEQ\_LEVEL0\_DELTA}[N] = \Delta f_{[0]} - \Delta f_{[N]}$ (refer to Table 77 for values of $\Delta f_{[N]}$)

4 Calculate $V_{TX\_MEQ\_LEVEL0\_DELTA}$ using the equation:
$V_{TX\_MEQ\_LEVEL0\_DELTA[N]}$ = TX_EQL[N] / TX_EQL[0]= $\Delta f_{[0]} - \Delta f_{[N]}$, where N = 1, 2, or 3

5 Record each value for $V_{TX\_MEQ\_LEVEL0\_DELTA}$ in the following table:

VSL[0]	Minimum	TX_EQL[N] / TX_EQL[0]	Maximum
P1	1.3		4.0
P2	2.4		6.0
P3	3.5		8.0
VSL[1]	Minimum	TX_EQL[N] / TX_EQL[0]	Maximum
P1	1.3		4.0
P2	2.4		6.0
VSL[2]	Minimum	TX_EQL[N] / TX_EQL[0]	Maximum
P1	1.3		4.0

6 Calculate $V_{TX\_MEQ\_DELTA}$ using the equation:
$V_{TX\_MEQ\_DELTA}$ = TX_EQL[N] / TX_EQL[N-1] = $\Delta f_{[N-1]} - \Delta f_{[N]}$, where N = 1, 2, or 3

7 Record each value for $V_{TX\_OUTPUT\_RATIO}$ in the following table:

VSL[0]	Minimum	TX_EQL[N] / TX_EQL[N-1]
P1	1.3	
P2	0.7	
P3	0.7	
VSL[1]	Minimum	TX_EQL[N] / TX_EQL[N-1]
P1	1.3	
P2	0.7	
VSL[2]	Minimum	TX_EQL[N] / TX_EQL[N-1]
P1	1.3	

Pass Condition for Transmitter Measured Equalization Tests:

Symbol	Parameter	Min.	Max.	Units	Comments
$V_{TX\_MEQ\_LEVEL0\_DELTA}$	Delta of TX Emphasis TX_EQL[1] / TX_EQL[0]	1.3	4.0	dB	▪ Applies to all valid VSLs ▪ Calculated using measured value of 1st and 5th harmonics of FFT ▪ For a given VSL[N]: TX_EQL[N] / TX_EQL[0] = (5th - 1st)[N] - (5th - 1st)[0] ▪ TX_EQL[3] mandatory
	Delta of TX Emphasis TX_EQL[2] / TX_EQL[0]	2.4	6.0	dB	
	Delta of TX Emphasis TX_EQL[3] / TX_EQL[0]	3.5	8.0	dB	
$V_{TX\_MEQ\_DELTA}$	Delta of TX Pre-Emphasis TX_EQL[1] / TX_EQL[0]	1.3	-	dB	▪ Applies to all valid VSLs ▪ Calculated using measured value of 1st and 5th harmonics of FFT ▪ For a given VSL[N]: TX_EQL[N] / TX_EQL[N - 1] = (5th - 1st)[N] - (5th - 1st)[N - 1] ▪ TX_EQL[3] mandatory
	Delta of TX Pre-Emphasis TX_EQL[2] / TX_EQL[1]	0.7	-	dB	
	Delta of TX Pre-Emphasis TX_EQL[3] / TX_EQL[2]	0.7	-	dB	

VTX_PE_RATIO

Test ID:

For Standard DP Pattern

1298101, 1298102, 1298103, 1298104 – VTX_PE_RATIO- PLTPAT

Procedure:

1 Perform the procedure for Spectral Measurements and Transmitter Measured Equalization Tests as prerequisites.

2 For each valid value of VSL[N] and TX_EQL[N], calculate PE[N] using the equation:
PE[N] = f5[N] - f5[0] (refer to Table 1 for values of f5)

3 Record each value for PE[N] in the following table:

VSL[0]	PE[0]
P0	Reference
P1	
P2	
P3	
VSL[1]	PE[1]
P0	Reference
P1	
P2	
VSL[2]	PE[2]
P0	Reference
P1	

4 For each value of $V_{TX\_MEQ\_LEVEL0\_DELTA}$ calculated in the Transmitter Measured Equalization Tests, determine the closest adjacent TX_MEQ values in dB.

5 Using Linear Interpolation, calculate the normative minimum PE (minPE) that corresponds to each measured value of TX_MEQ.
minPE = [(TX_MEQ - X1) (Y2 - Y1) / (X2 - X1)] + Y1
where, (X1,Y1) and (X2,Y2) are adjacent TX_MEQ and Normative minPE values.

6 Verify that the actual calculated values of PE[N] are above those illustrated in the following Figure.

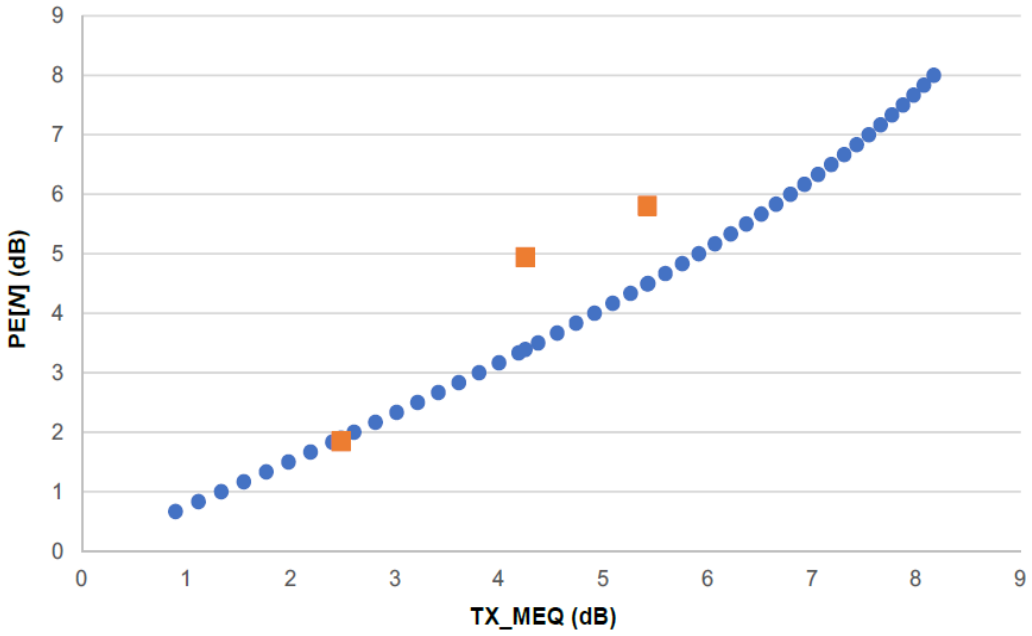


Figure 70 PE v/s TX_MEQ curve

Pass Condition for VTX_PE_RATIO Tests:

Symbol	Parameter	Min.	Max.	Units	Comments
$V_{TX\_PE\_RATIO}$	Ratio of PE[N] / TX_MEQL[N]	2/3	-		▪ Applies to all valid VSL and TX_EQL combinations ▪ PE[N] = 5th[N] - 5th[0] ▪ Pass/fail based on PE vs. MEQ curve

PE[N] > minPE calculated

Transmitter Bit Amplitude Ratio

VTX_TRANSITION_BIT_OUTPUT_RATIO

Test ID:

For Standard DP Pattern

1299101, 1299102, 1299103, 1299104 – VTX_TRANSITION_BIT_OUTPUT_RATIO - PLTPAT

Procedure:

1 Perform the procedure for Spectral Measurements as a prerequisite.

NOTE

The TX_EQL[N] transition bit amplitude shall be greater than or equal to TX_EQL[N-1] transition bit amplitude.

2 For a given value of VSL, calculate $V_{TX\_TRANSITION\_BIT\_OUTPUT\_RATIO}$ using the equation: $V_{TX\_TRANSITION\_BIT\_OUTPUT\_RATIO}$ = f5[N] - f5[N-1], where N = 1, 2, or 3 (refer to Table 77 for f5)

3 Record each value for $V_{TX\_TRANSITION\_BIT\_OUTPUT\_RATIO}$ in the following table:

VSL[0]	Minimum	Notes
P0	Not Available	Reference
P1	0	
P2	0	
P3	0	
VSL[1]	-	-
P0	Not Available	Reference
P1	0	
P2	0	
VSL[2]	-	-
P0	Not Available	Reference
P1	0	

Pass Condition for Transmitter Bit Amplitude Ratio Tests:

Symbol	Parameter	Min.	Max.	Units	Comments
$V_{TX\_TRANSITION\_BIT\_OUTPUT\_RATIO\_PEL[N]/PEL[N-1]}$	Transition bit amplitude ratio between TX_EQL[N] and TX_EQL[N - 1] for a given VSL[N]	0	-	dB	▪ TX_EQL[N] transition bit amplitude shall be greater than or equal to that of TX_EQL[N - 1] ▪ 5th (N) - 5th (N - 1)

Test References

See:

VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.4, Table 3-15.

VESA DisplayPort (DP) Standard, Version 1.4a, Section 3.5.2, Table 3-21.

Expected/Observable Results

The measured values for Level and Equalization testing shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for each test.

10 DisplayPort 1.4a Sink Tests

Overview

Test Point Definition for DisplayPort 1.4a Sink Tests

NOTE Sink Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Sink DUT at Test Point 3 (TP3) as shown in Figure 71. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

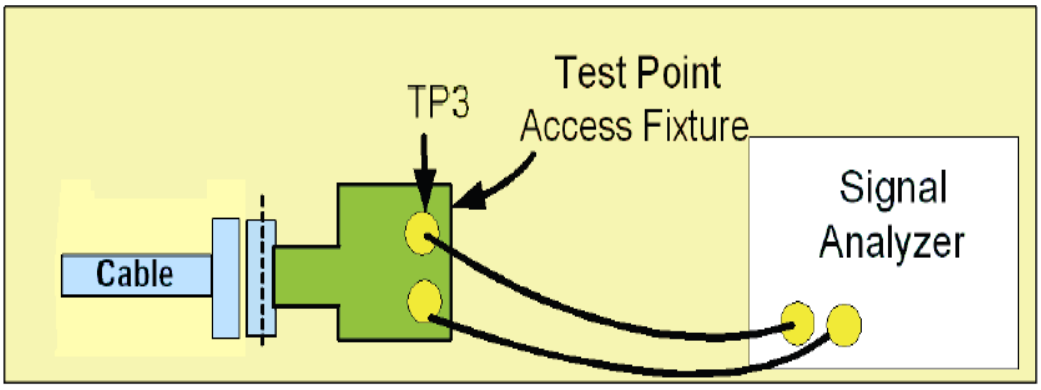


Figure 71 Test Point 3 Connection for DisplayPort 1.4a Sink Tests

Table 78 defines the test point fixtures and instruments used for DisplayPort 1.4a Sink Tests:

Table 78 Test Point Fixtures and Instruments for DisplayPort 1.4a Sink Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** For USB Type-C Connector, ▪ Wilder Technologies DPC-TPA-R* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Calibration of Stress Signal

For the calibration of the stress signal, you must test the stress signal in the manner shown in the Figure 72 for RBR and Figure 73 for HBR and HBR2.

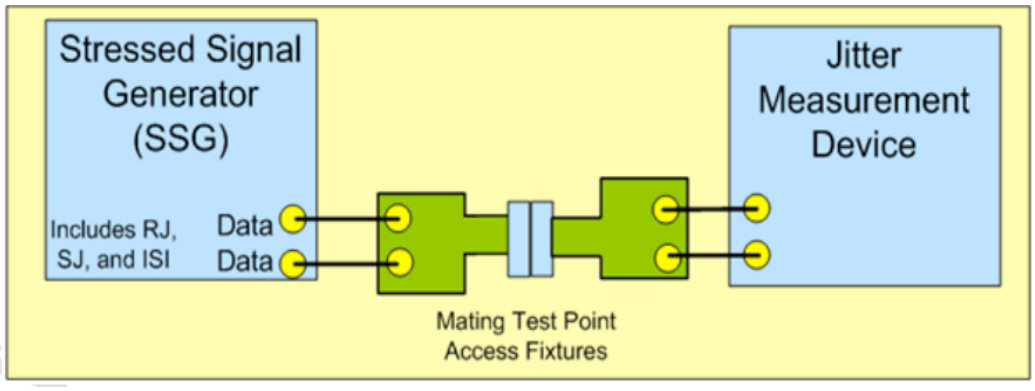


Figure 72 Test Point 3 Connection for Stress Signal Calibration of RBR

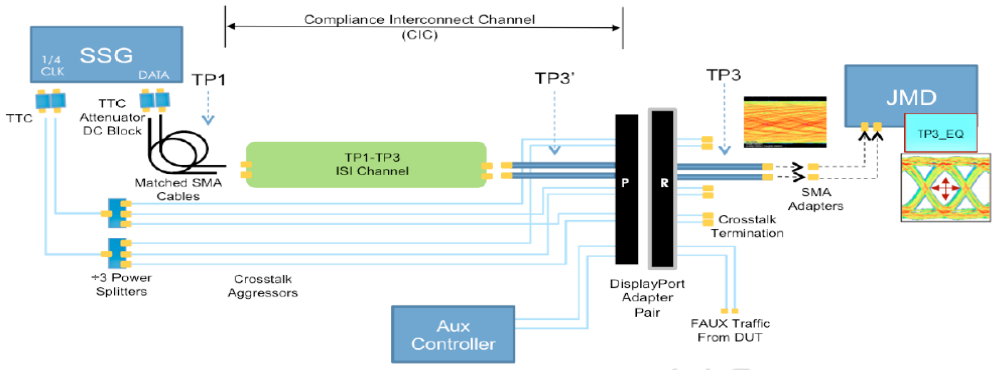


Figure 73 Test Point 3 Connection for Stress Signal Calibration of HBR and HBR2

Table 79 defines the Test Point 3 Connections for Stress Signal Calibration:

Table 79 Test Point Connections for Stress Signal Calibration

Test Requirement	Device Used
Stress Signal Generator (SSG)	Bit Error Rate Tester ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** For USB Type-C Connector, ▪ Wilder Technologies DPC-TPA-R* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Jitter Measurement Device (JMD)	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.4a Sink Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort 1.4a Standards, select the option **1.4a** in the **Test Specification** area.

5 The option **Physical Layer Tests** appears by default in the **Test Selection** area.

6 Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.

7 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

8 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

9 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

10 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

11 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

12 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

13 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

14 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DisplayPort 1.4a Sink Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

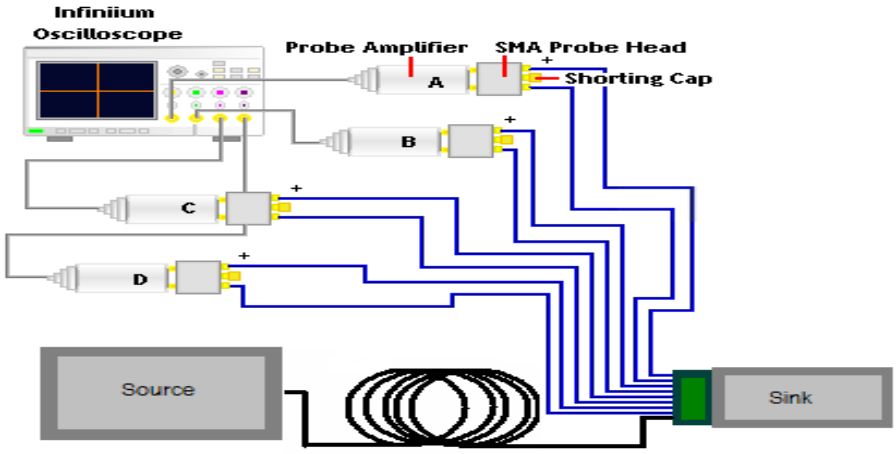


Figure 74 Sample connection diagram for DisplayPort 1.4a Sink Tests

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Sink tests to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1 In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.

2 On the **Test Setup** window,

a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b In the **DUT Info** area, select **Device Type** as **Sink**. The **Connector Type** is grayed out.

c In the **Test Info** area, the **Test Type** is grayed out.

d In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.

3 Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1 Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.

2 On the **Connection Setup** window,

a Select the appropriate option in the **Fixture Type** to indicate where the DUT is connected to.

b Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.

c In the **Channel Selection** area, assign appropriate channels to lanes.

3 Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of sink tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.4a Sink Tests" on page 420 to complete the task flow for DUT setup along with configuring the Compliance Application to run each test.

Sink Eye Diagram Test

Test ID

12140001, 12140002, 12140003, 12140004 – Eye Diagram Test

Test Overview

The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

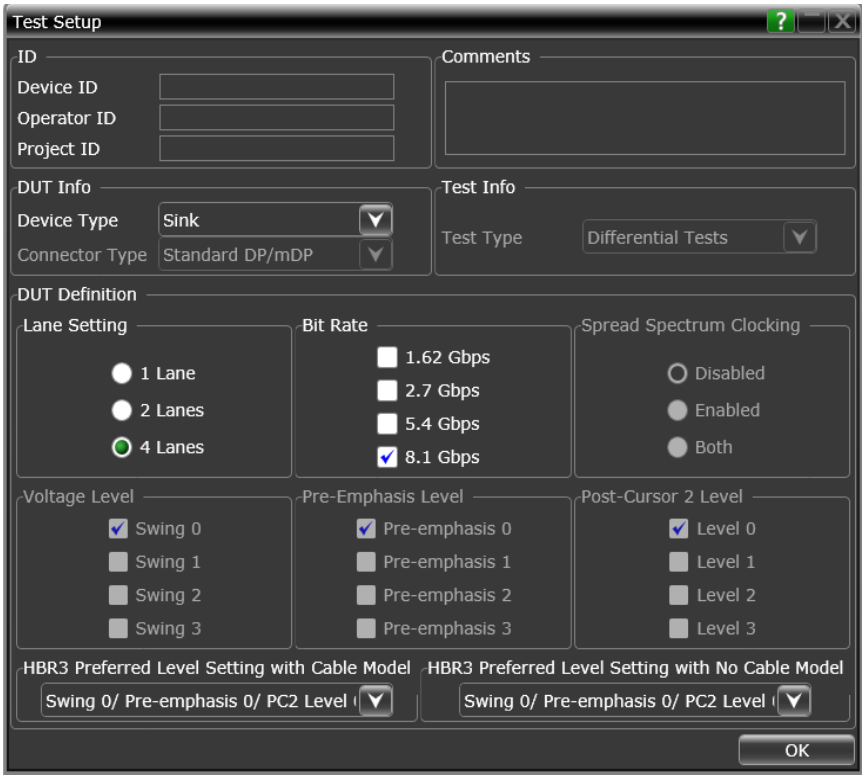
You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the following specifications for degradation:

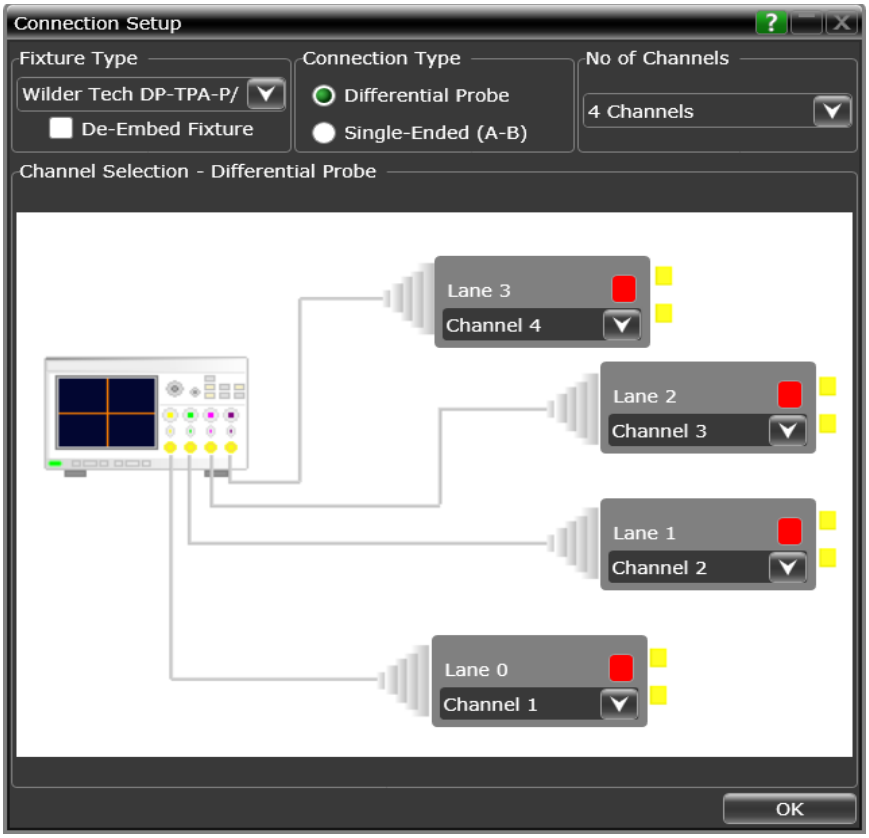
- Voltage Level:
  - 90mV peak to peak +/- 10% for HBR2 at TP3_EQ (Table 3-18, DP1.2a)
  - 150mV peak to peak +/- 10% for HBR at TP3_EQ (Table 3-25, DP1.2a)
  - 46mV peak to peak +/- 10% for RBR at TP3 (Table 3-26, DP1.2a

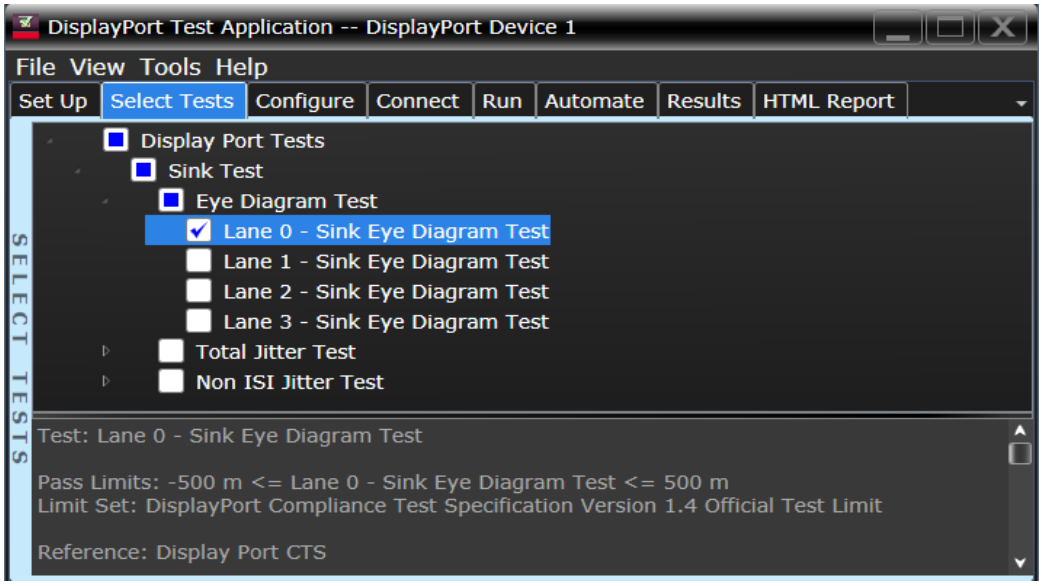
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR3–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR3)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR3–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
9 Measure the jitter of the eye diagram using the Histogram.
10 Check for any signal trajectories that may have entered into the mask.
11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 80 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 80 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	High (2.7 Gb/s)
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

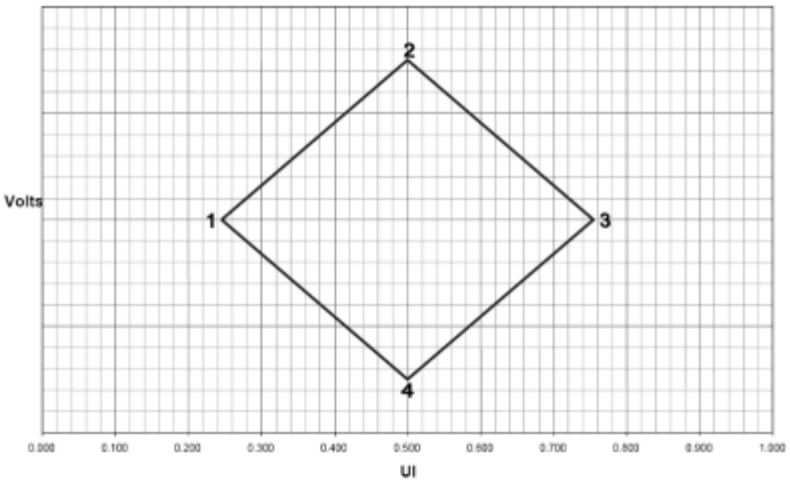


Figure 75 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 81 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.045*
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.045*

NOTE

*Eye height limit of 45 mV and -45 mV assumes cross-talk as 0, which is only possible in case of single lane testing.

In case of multi-lane testing, cross talk exists, and the eye height values deviate by ± 7 mV. Thus the eye height becomes (+45 +7) mV and (-45 -7) mV or +52 mV and -52 mV.

Table 82 Eye Diagram Mask Coordinates for TP3_EQ (HBR3)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.53UI	0.00000
2	Any passing UI location between 0.375 and 0.625UI	0.0325
3	Point 1 + 0.53UI	0.00000
4	Same as Point 2	-0.0325

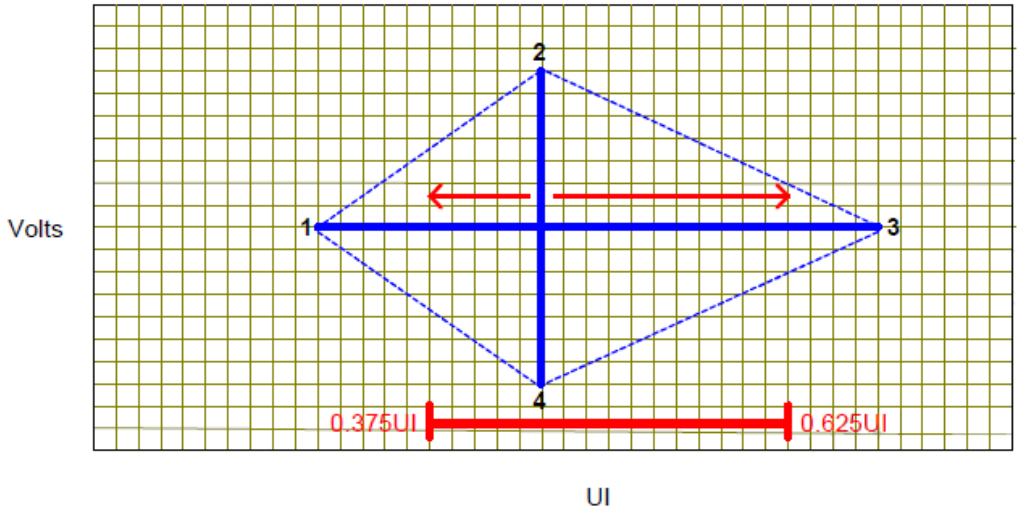


Figure 76 The Eye Mask at TP3_EQ (HBR2 and HBR3)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Sink Total Jitter Test

Test ID

12210001, 12210002, 12210003, 12210004 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

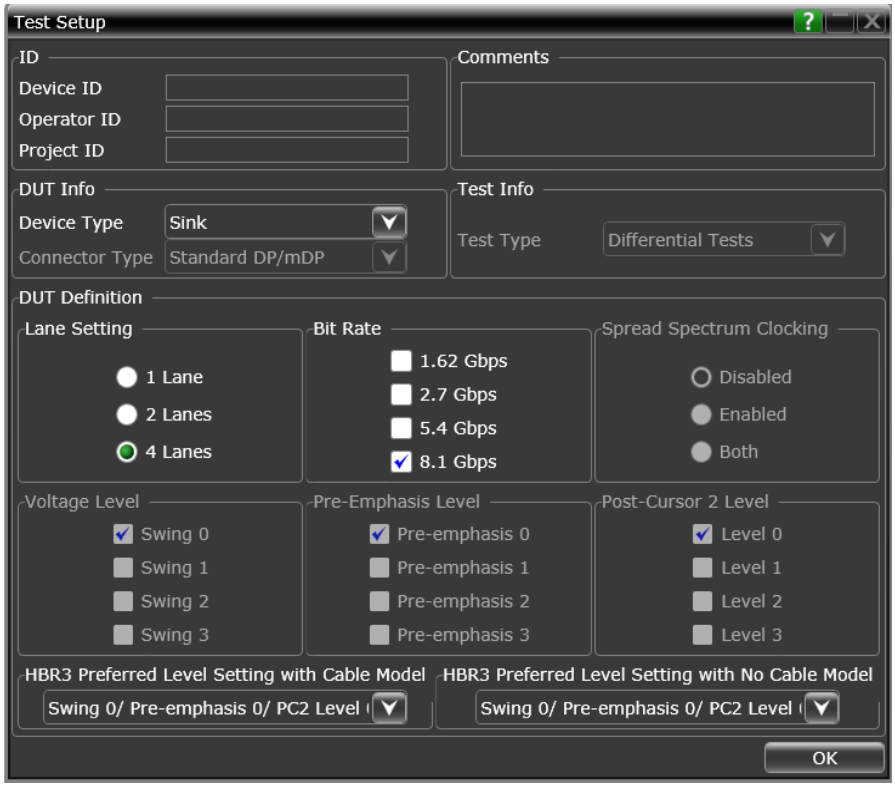
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

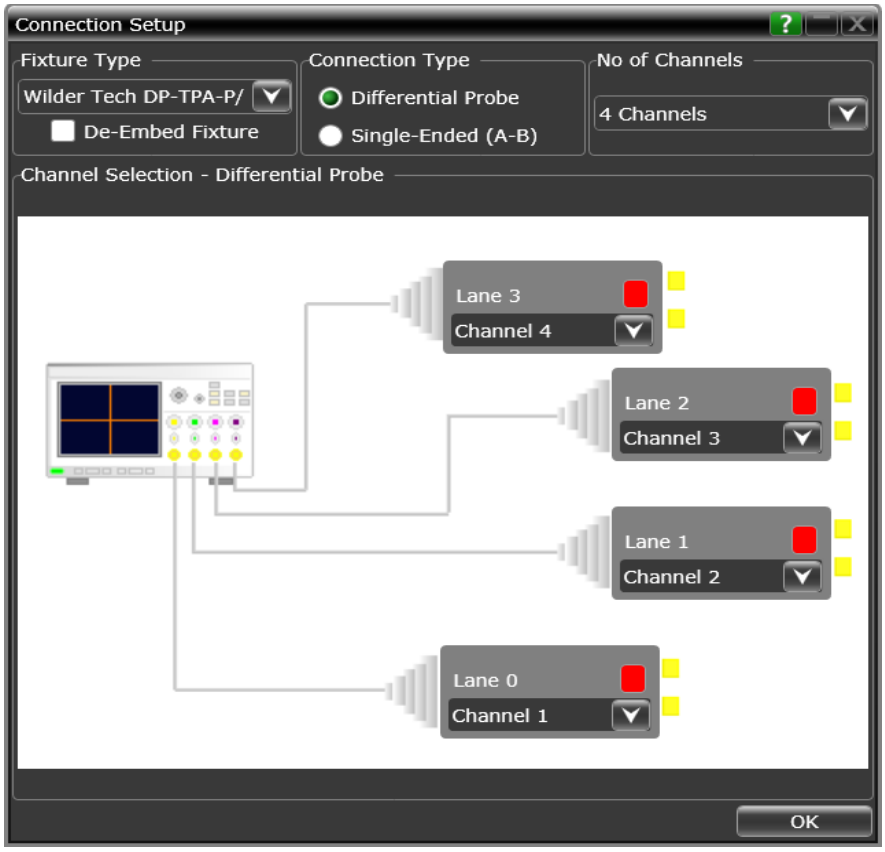
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

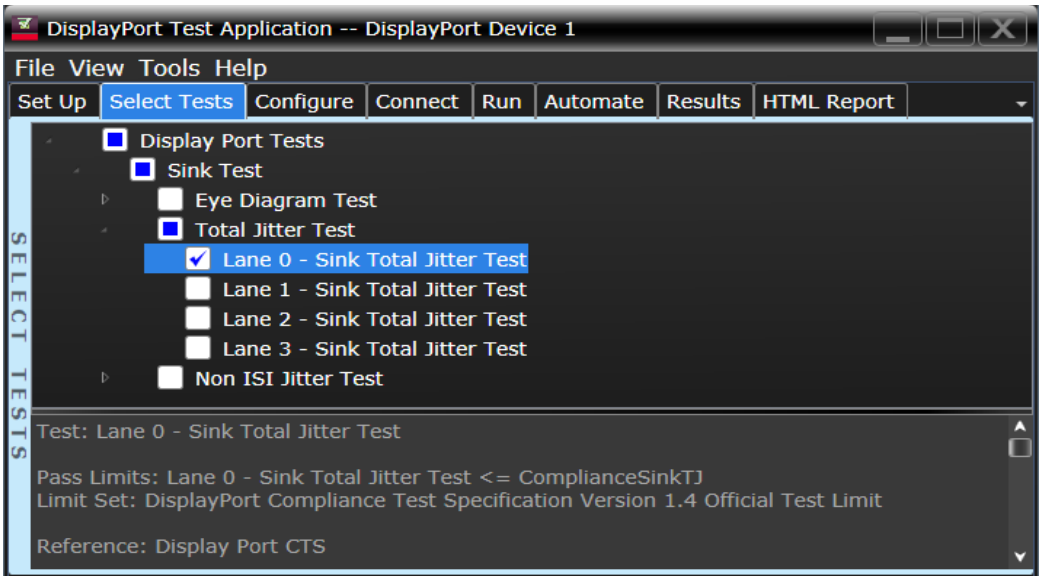
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR3–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR3)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR3–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 83 Total Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	0.580 UI*

* The limits for the Total Jitter are derated by 0.04 UI from 0.62 UI limit in DisplayPort 1.2a Standard.

Table 84 Total Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 4.1*
- VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Sink Non-ISI Jitter Test

Test ID

12220001, 12220002, 12220003, 12220004 – Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

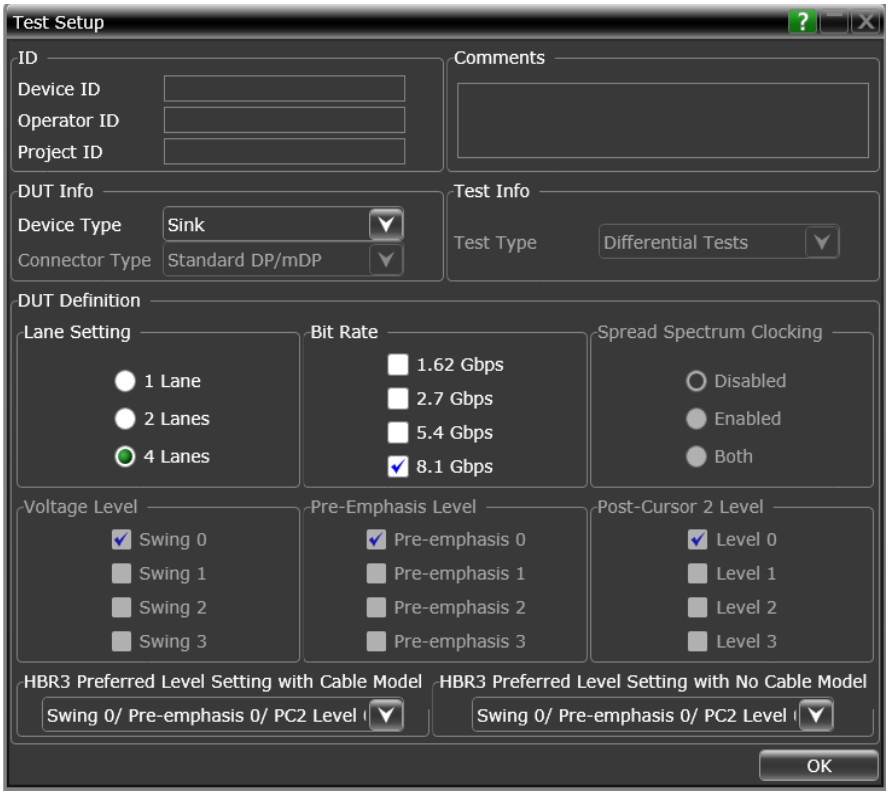
Calculate Non-ISI Jitter using the following equation:

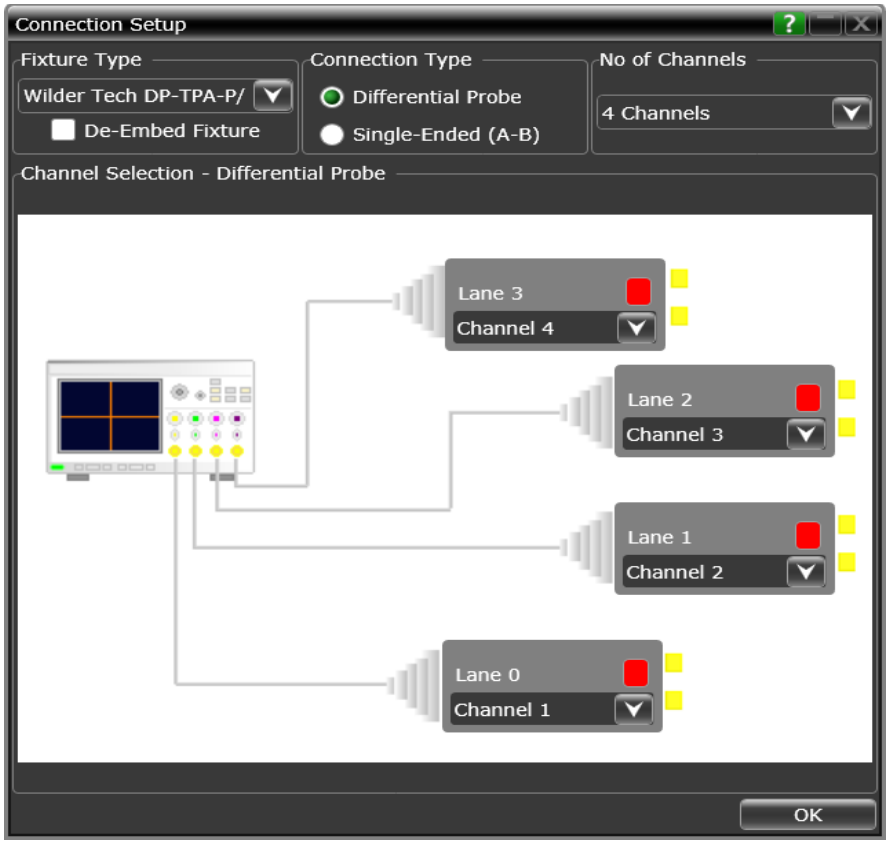
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

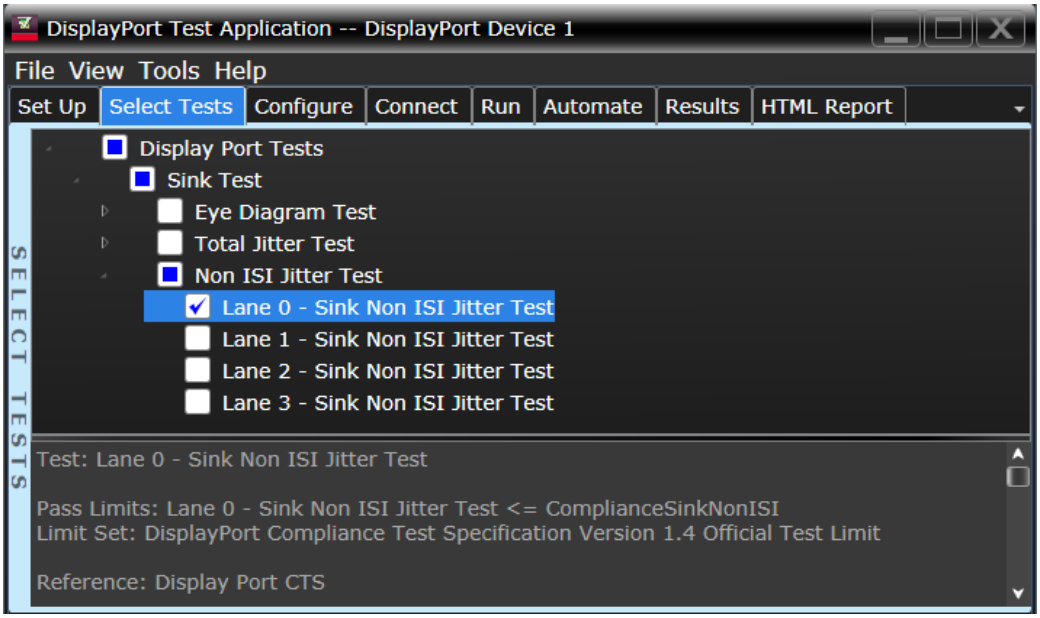
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR3–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR3)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR3–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 85 Non ISI Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	-

Table 86 Non ISI Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 4.1*
- VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

11 DisplayPort 1.4a Cable Tests

Overview

Test Point Definition for DisplayPort 1.4a Cable Tests

NOTE Cable Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Cable DUT at Test Point 3 (TP3) as shown in Figure 77. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

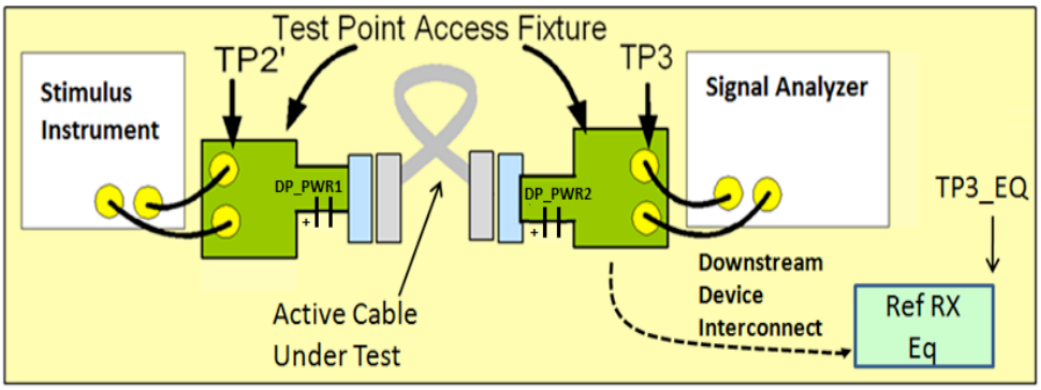


Figure 77 Test Point 3 Connection for DisplayPort 1.4a Cable Tests

Table 87 defines the test point fixtures and instruments used for DisplayPort 1.4a Cable Tests:

Table 87 Test Point Fixtures and Instruments for DisplayPort 1.4a Cable Tests

Test Requirement	Device Used
Stimulus Instrument	Pulse Pattern Generator ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** For USB Type-C Connector ▪ Wilder Technologies DPC-TPA-R* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Table 88 defines the input signal parameters applied by the stimulus instrument at TP2:

Table 88 Input Signal Parameters by Stimulus Instrument

RBR	▪ Reference Table 3-22 and Table 3-24, DP 1.2a ▪ Edge Rate (20-80): 155-165ps (260mUI) ▪ Eye Height: 400mV ▪ Total Jitter: 270mUI ▪ ISI: 100mUI ▪ Random Jitter (rms): 7.9mUI ▪ Sinusoidal Jitter: ~75mUI at 20MHz (Adjust to achieve Total Jitter)
HBR	▪ Reference Table 3-22 and Table 3-23, DP 1.2a ▪ Edge Rate (20-80): 90-100ps (260mUI) ▪ Eye Height: 350mV ▪ Total Jitter: 420mUI ▪ ISI: 144mUI ▪ Random Jitter (rms): 13.2mUI ▪ Sinusoidal Jitter: ~117mUI at 20MHz (Adjust to achieve Total Jitter)

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.4a Cable Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort 1.4a Standards, select the option **1.4a** in the **Test Specification** area.
5. The option **Physical Layer Tests** appears by default in the **Test Selection** area.
6. Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.
7. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
8. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
9. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
10. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
11. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
12. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
13. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
14. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DisplayPort 1.4a Cable Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

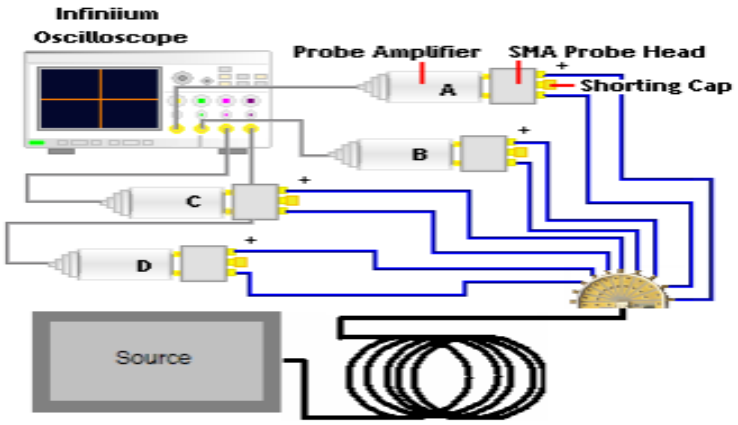


Figure 78 Sample connection diagram for DisplayPort 1.4a Cable Tests

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Cable tests to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1 In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.

2 On the **Test Setup** window,

a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b In the **DUT Info** area, select the **Device Type** as **Cable**. The **Connector Type** is grayed out.

c In the **Test Info** area, the **Test Type** options are grayed out.

d In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.

3 Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1 Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.

2 On the **Connection Setup** window,

a Select the appropriate option in the **Fixture Type** to indicate where the DUT is connected to.

b Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.

c In the **Channel Selection** area, assign appropriate channels to lanes.

3 Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of cable tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.4a Cable Tests" on page 440 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Cable Eye Diagram Test

Test ID

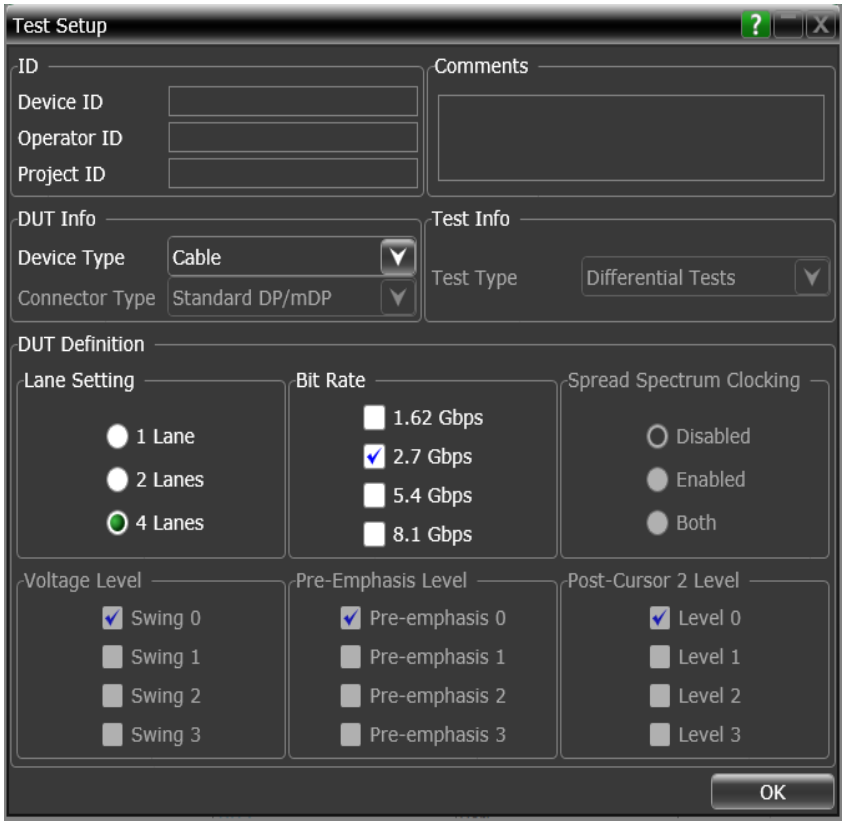
12150001, 12150002, 12150003, 12150004 – Eye Diagram Test

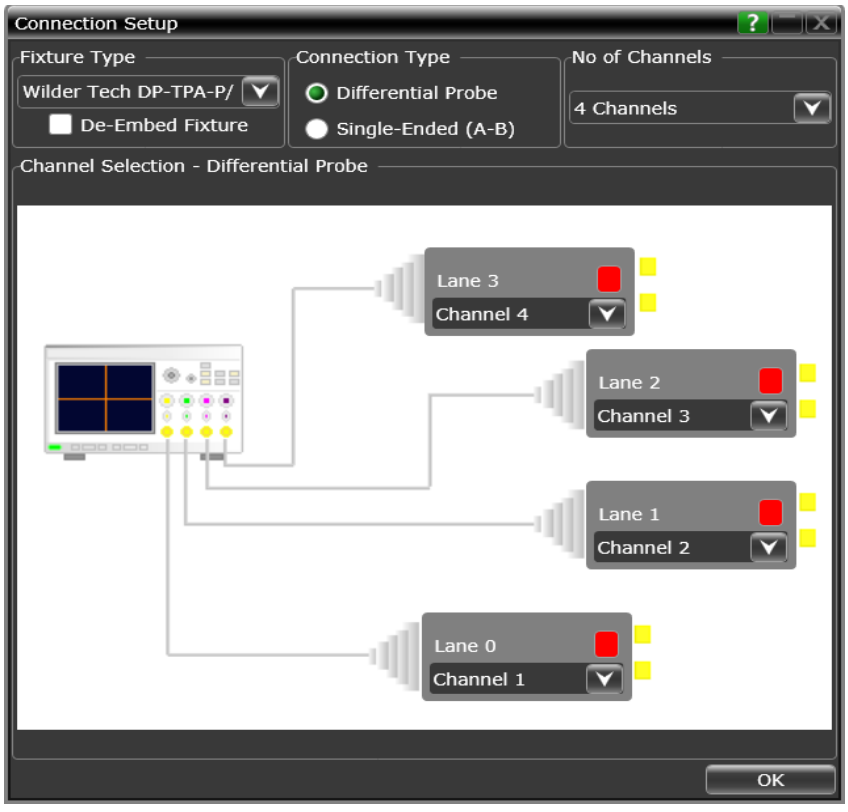
Test Overview

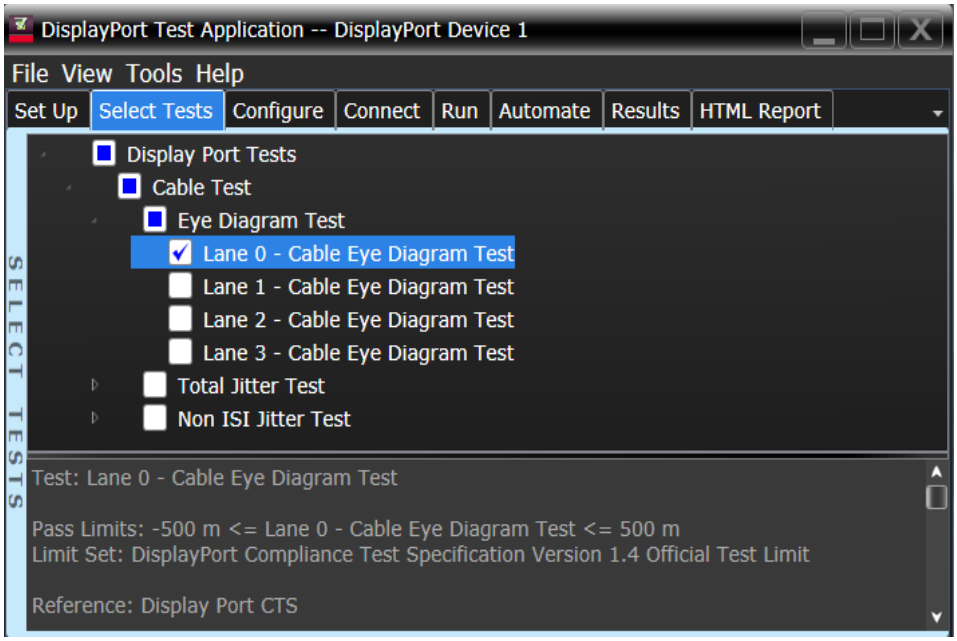
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 88
Crosstalk Signal Parameter	Quarter-rate clock signal (D24.3 pattern) is injected to lanes other than the lane under test. The characteristics of the aggressor signals are: Pattern–D24.3 Bit Rate–(Same as lane under test) Voltage Amplitude–(Same as lane under test) ▪ RBR-400mV ▪ HBR-350mV Edge Rate (20-80)–130ps at TP3


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
9 Measure the jitter of the eye diagram using the Histogram.

10 Check for any signal trajectories that may have entered into the mask.

11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 89 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 89 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

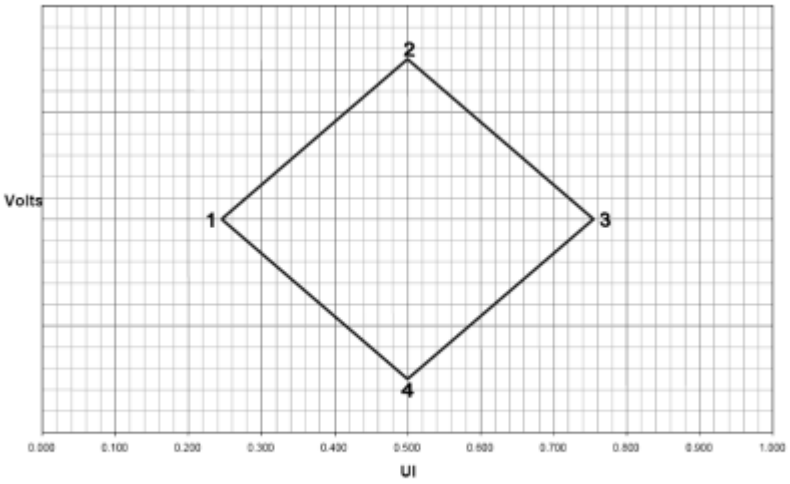


Figure 79 The Cable Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Cable Total Jitter Test

Test ID

12230001, 12230002, 12230003, 12230004 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

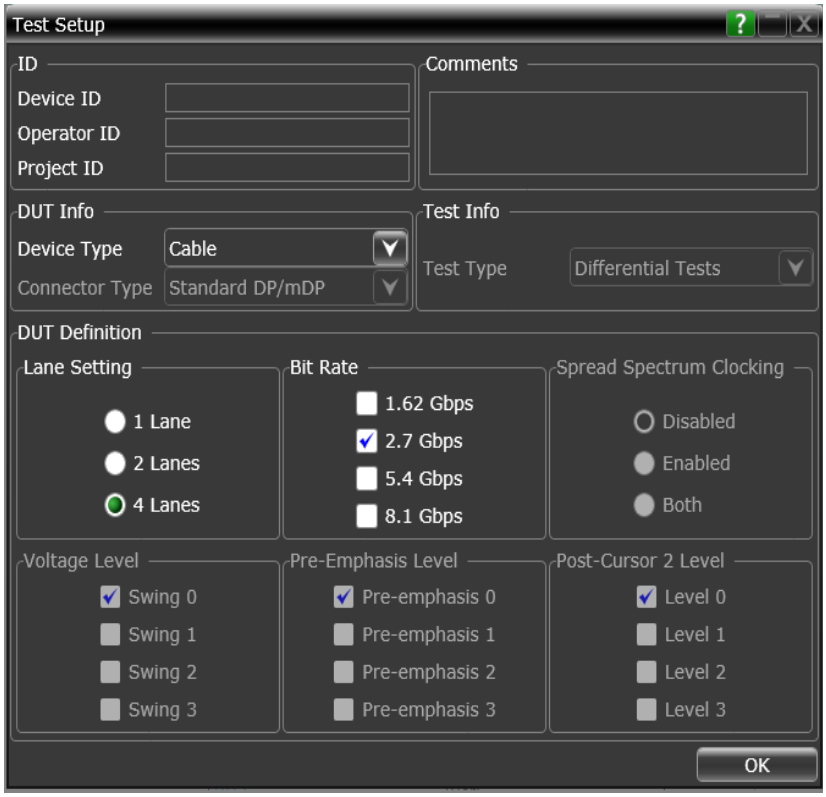
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

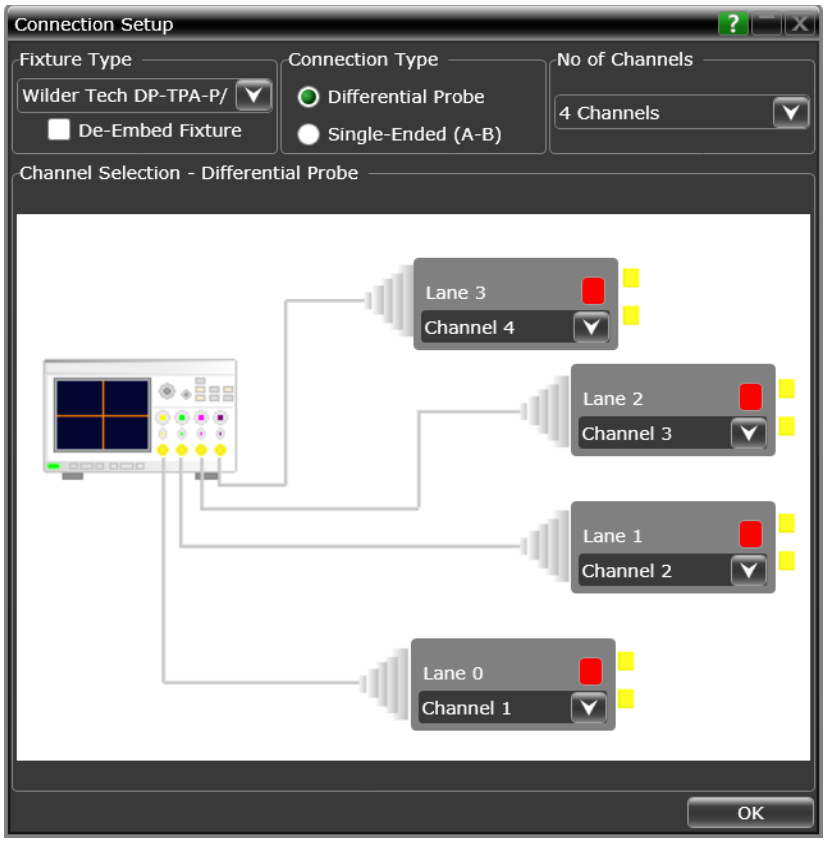
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

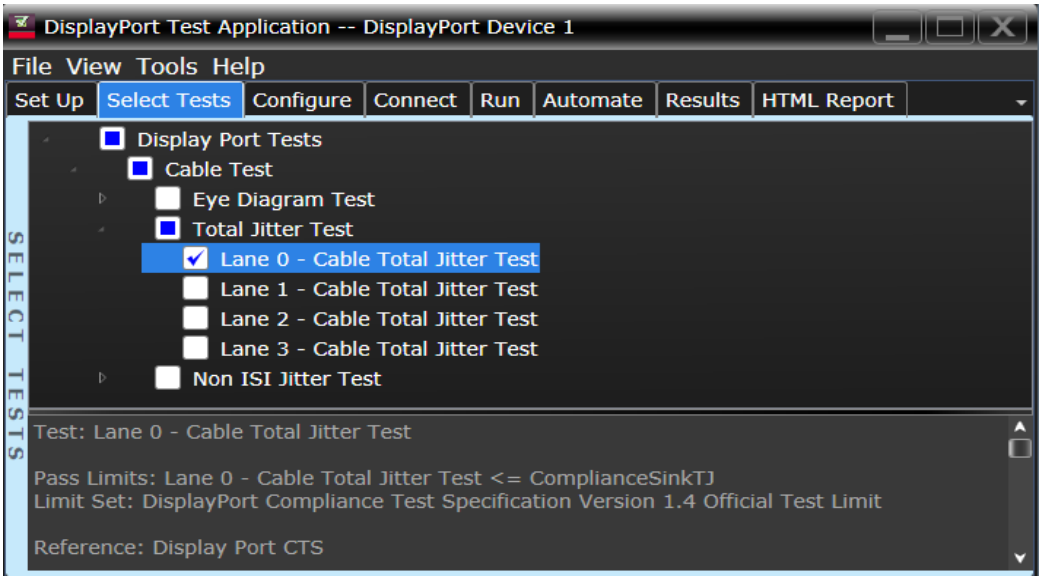
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 88


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 90 Total Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Cable Non-ISI Jitter Test

Test ID

12240001, 12240002, 12240003, 12240004 — Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

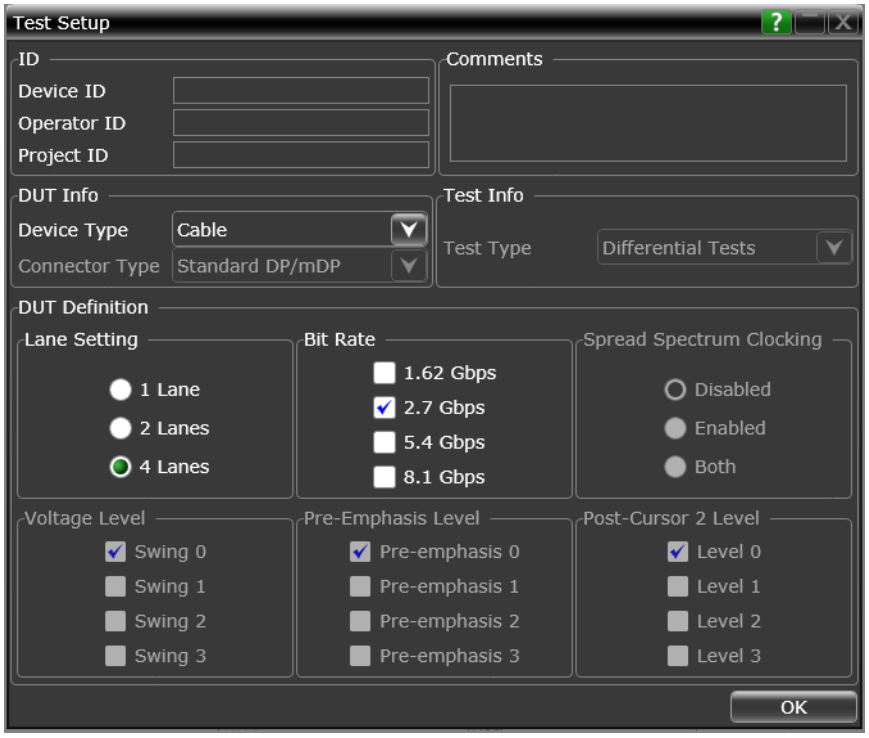
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

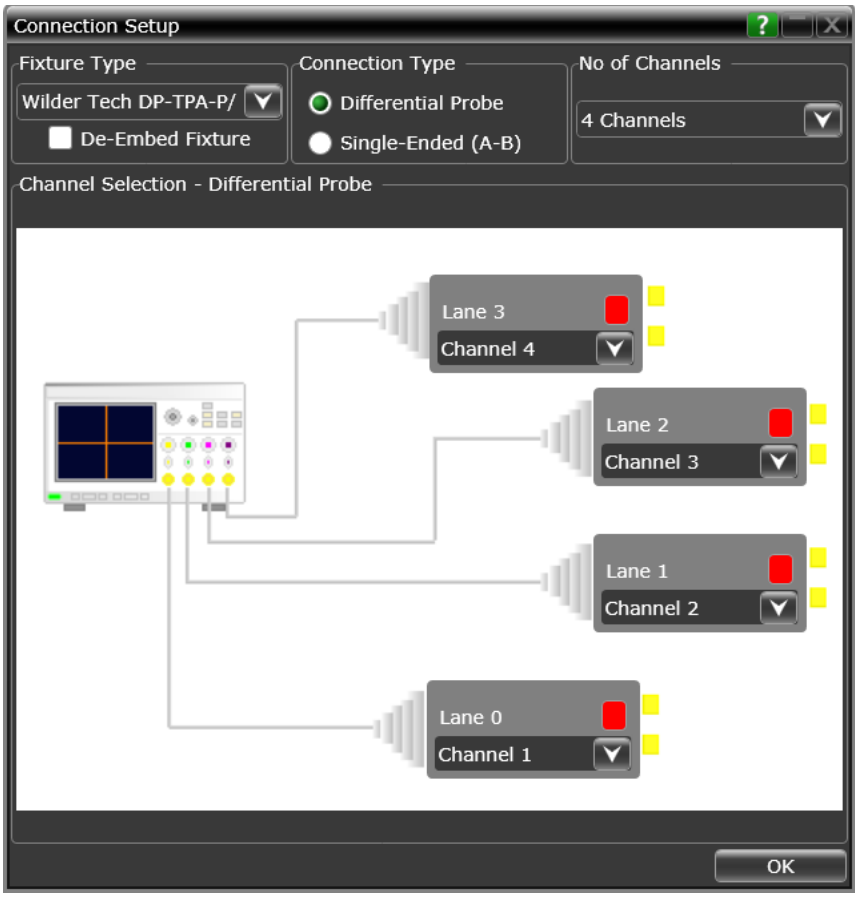
Calculate Non-ISI Jitter using the following equation:

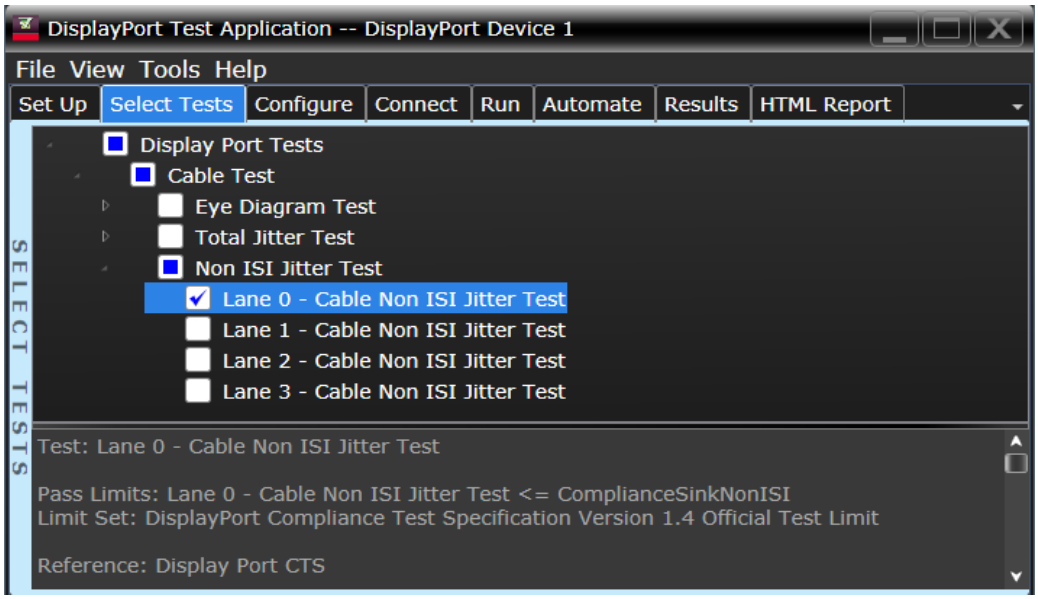
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 88


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 91 Non ISI Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non-ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

12 DisplayPort 1.4a AUX Channel Tests

Overview

This section describes the normative and informative AUX Channel physical layer tests and inrush tests for compliance verification of DisplayPort 1.4a source and sink.

Test Point for AUX Channel Tests

You must test the Source devices at Test Point 2 (TP2) while the Sink devices must be tested at Test Point 3 (TP3). See Figure 80.

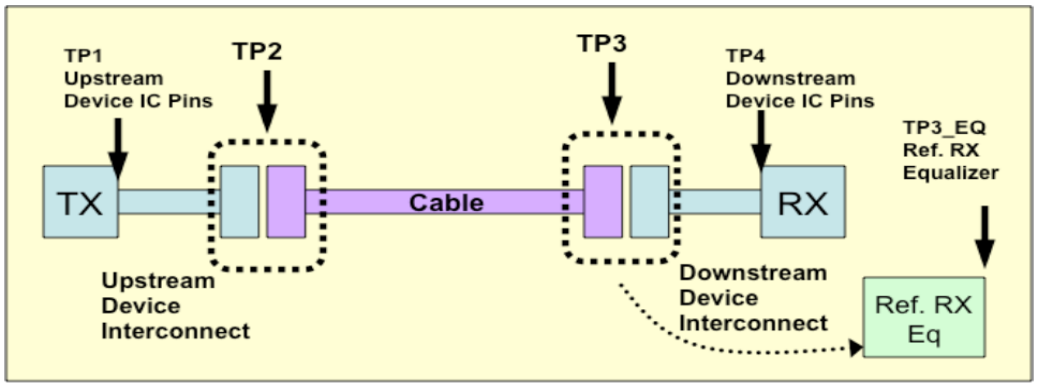


Figure 80 Test Points for DisplayPort 1.4a AUX Channel Tests

Table 92 defines the test point fixtures and instruments used for DisplayPort 1.4a AUX Channel Tests:

Table 92 Test Point Fixtures and Instruments for DisplayPort 1.4a AUX Channel Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-P* ▪ W2641B DisplayPort Test Point Access Adapter For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-P* ▪ Luxshare ICT mDP Plug (mDP-TPA-P)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope
Stimulus	Stimulus must be applied to the DUT to cause AUX Channel transactions to occur. This stimulus shall not be included in or affect the measurements. Reference Sink needed as stimulus for the Source DUT: ▪ Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Reference Source needed as stimulus for the Sink DUT: ▪ Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.4a AUX Channel Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort 1.4a Standards, select the option **1.4a** in the **Test Specification** area.

5 Select the option **AUX PHY and Inrush Tests** in the **Test Selection** area.

6 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

7 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

8 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

9 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

10 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

11 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

12 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

13 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Settings for AUX PHY and Inrush Tests

Perform the following steps before you run the Auxiliary Channel and Inrush tests on the source or sink device:

1 Click the **Test Setup** button on the **Set Up** tab to set up for Auxiliary Channel and Inrush tests.

2 On the **Test Setup** window,

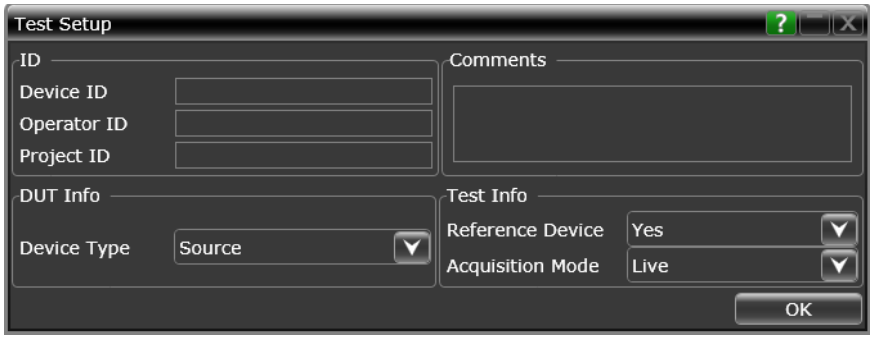
a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b From the **Device Type** drop-down options, select either **Source** or **Sink**.

c From the **Reference Device** drop-down options, select **Yes** if a reference sink/source is attached to device under test during testing.

d From the **Acquisition Mode** drop-down options, select **Live** if waveform acquisition and analysis will be performed on an online Infiniium Oscilloscope, else select **Offline**.

3 Click **OK** to exit the **Test Setup** window.

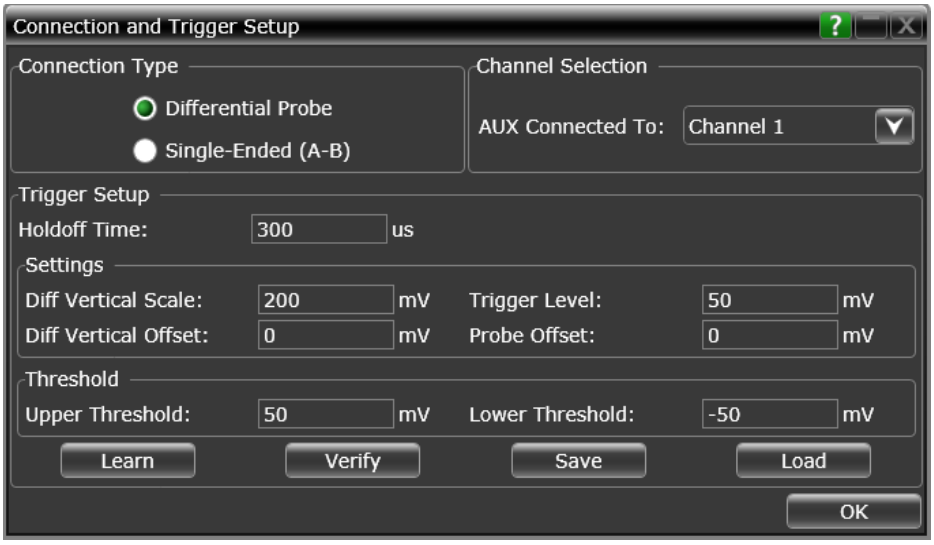


4 Click the **Connection Setup** button that now appears on the **Set Up** tab.

5 On the **Connection and Trigger Setup** window,

a Select either **Differential Probe** or **Single-Ended (A-B)** in the **Connection Type** area, depending on the probe connection you are using.

b From the **AUX Connected To:** drop-down options of the **Channel Selection** area, select the Oscilloscope Channel where the Auxiliary Lane is connected to.



c In the **Trigger Setup** area, define the Oscilloscope parameters to trigger on an Auxiliary signal during testing.

- **Hold Off Time** – The oscilloscope minimum hold off time before triggering the next waveform. Note that any Auxiliary transaction from the source must receive a reply from the sink in 400 us, else such a transaction is considered a timeout. Hold off time, in such cases, represents the minimum idle time before each Aux transaction is initialized. It is defaulted to 300 us which is a safe timing value for most devices tested in the lab. Most devices respond much faster than 300 us.
- **Trigger Level** – The AUX Channel signal level on which to trigger. Note that for a bi-directional signal (where a reference sink is attached), you must set the trigger level such that it crosses both the source command and the sink reply signal. Figure shows correct and incorrect trigger levels.

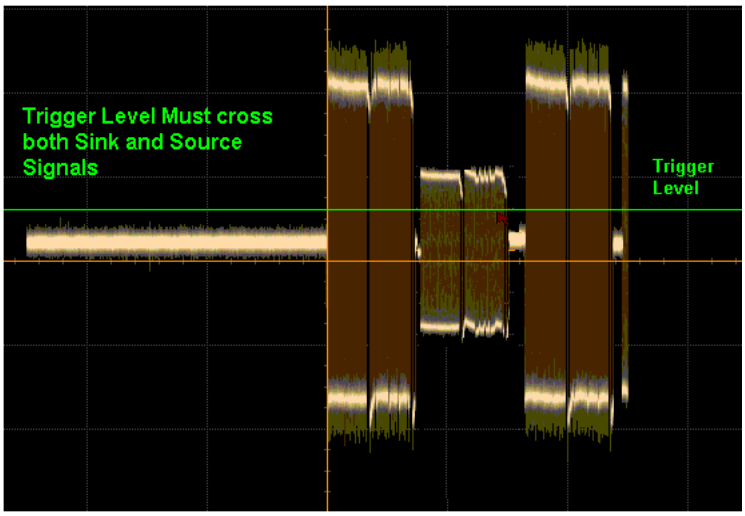


Figure 81 Correct Trigger Level

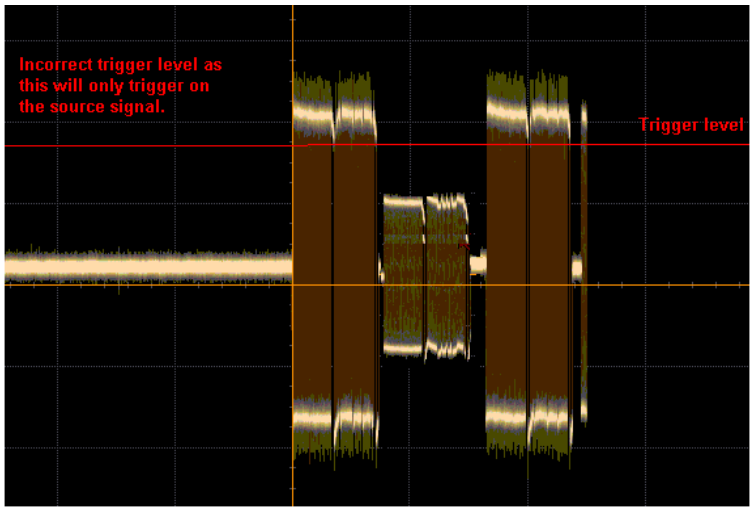


Figure 82 Incorrect Trigger Level

- **Vertical Scale** – The oscilloscope vertical scale. Set the vertical to make sure that all signals are visible on the oscilloscope display.
- **Offset** – Set the offset so that the center point is aligned with the center of the oscilloscope display.
- **Upper Threshold/Lower Threshold** – The threshold level of signal must be set properly so that both upper and lower thresholds cross both the source and sink signals when the DUT is attached with a reference sink. The threshold levels are important parameters because they are used for edge detection when decoding a source command from a sink reply.

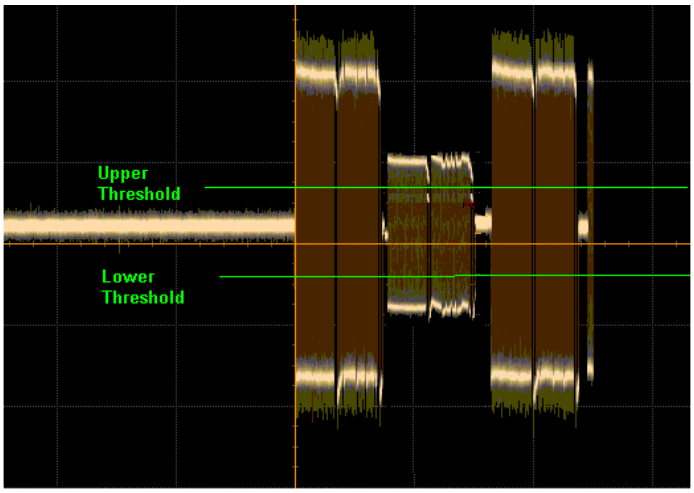
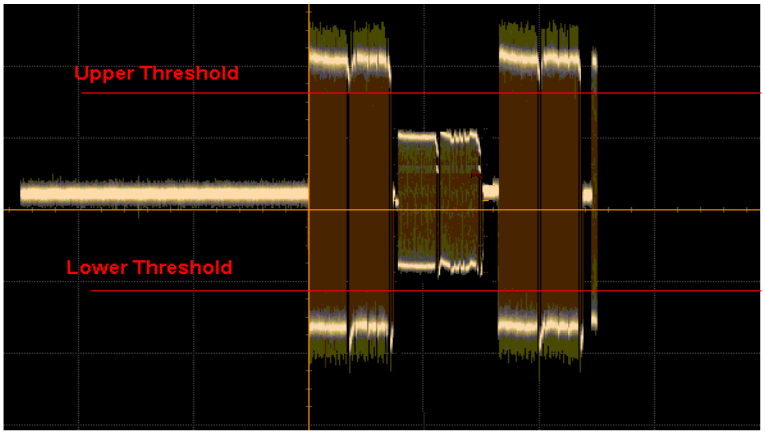


Figure 83 Correct Threshold set



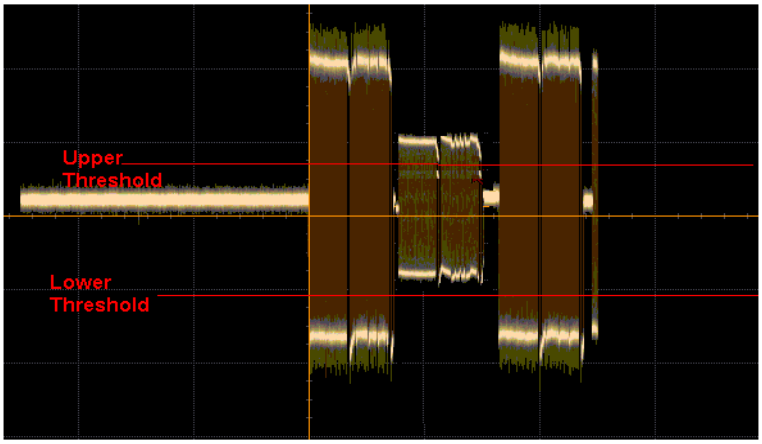


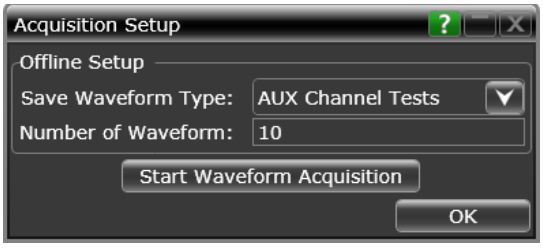
Figure 84 Wrong Thresholds set

- Click the **Learn** button to access the information guide about the trigger setup parameters. However, note that the learning guide may not necessarily work due to variation in the actual Auxiliary signals, owing to different manufacturers. Keysight recommends that you must check to make sure that the parameters are correctly set as previously described.
- Click **Verify** and follow the instructions, if you wish to check the AUX Channel trigger.
- You may **Save** or **Load** the trigger setup configuration as a **.tsf* file.

6 Click **OK** to exit the **Connection and Trigger Setup** window.

7 If you select the option **Offline** for the **Acquisition Mode** in the **Test Setup** window, the **Acquisition Setup** button appears in the **Test Environment Setup** area of the **Set Up** tab.

8 Click the **Acquisition Setup** button to save the waveform files so that you can avoid the manual process to initiate Auxiliary transactions during the time of test runs.



9 On the **Acquisition Setup** window,

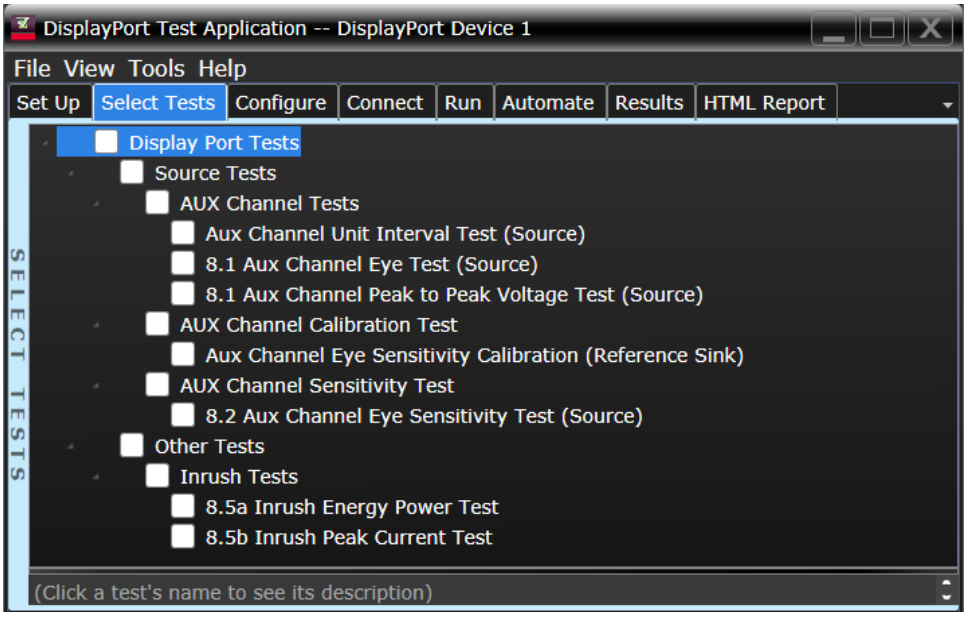
a select the type of waveforms to be saved from the **Save Waveform Type:** drop-down options.

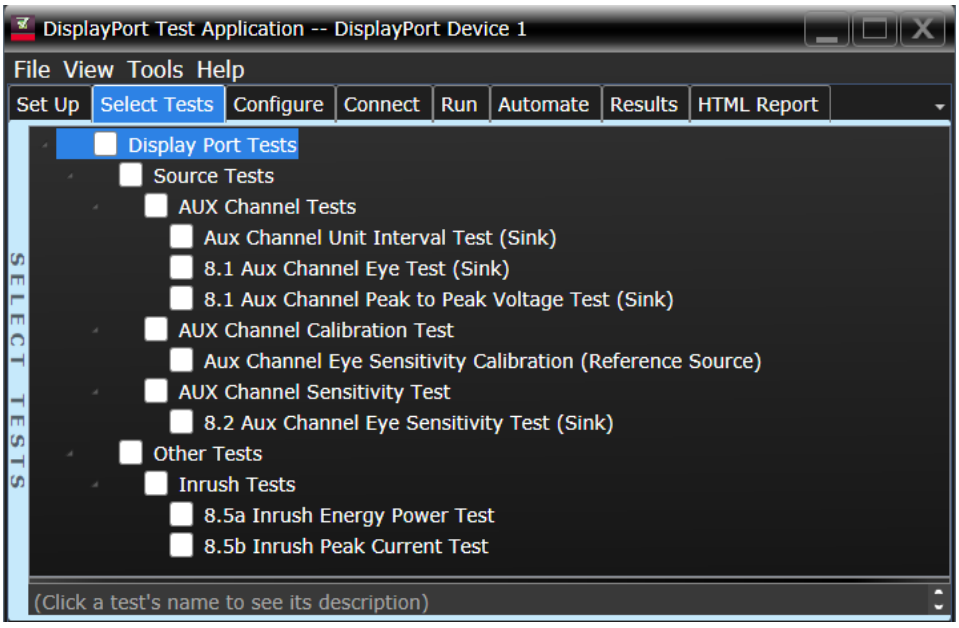
b define the number of waveforms to be saved in the **Number of Waveform:** field.

c Click the **Start Waveform Acquisition** button to start capturing and saving waveforms.

d Click **OK** to return to the **Set Up** tab.

10 Click the **Select Tests** tab where the AUX Channel tests for Source or Sink devices appear.


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Display Port Tests
Source Tests
AUX Channel Tests
Aux Channel Unit Interval Test (Source)
8.1 Aux Channel Eye Test (Source)
8.1 Aux Channel Peak to Peak Voltage Test (Source)
AUX Channel Calibration Test
Aux Channel Eye Sensitivity Calibration (Reference Sink)
AUX Channel Sensitivity Test
8.2 Aux Channel Eye Sensitivity Test (Source)
Other Tests
Inrush Tests
8.5a Inrush Energy Power Test
8.5b Inrush Peak Current Test
(Click a test's name to see its description)


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Display Port Tests
Source Tests
AUX Channel Tests
Aux Channel Unit Interval Test (Sink)
8.1 Aux Channel Eye Test (Sink)
8.1 Aux Channel Peak to Peak Voltage Test (Sink)
AUX Channel Calibration Test
Aux Channel Eye Sensitivity Calibration (Reference Source)
AUX Channel Sensitivity Test
8.2 Aux Channel Eye Sensitivity Test (Sink)
Other Tests
Inrush Tests
8.5a Inrush Energy Power Test
8.5b Inrush Peak Current Test
(Click a test's name to see its description)

Probing/Connection Set Up for AUX Channel Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests. When performing the Source AUX Channel tests, a Reference Sink device is required. Similarly, when performing the Sink AUX Channel tests, a Reference Source device is required.

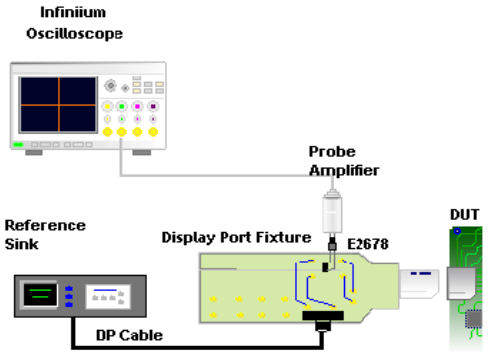


Figure 85 Sample connection diagram for source AUX channel tests with source DUT connected to a reference sink

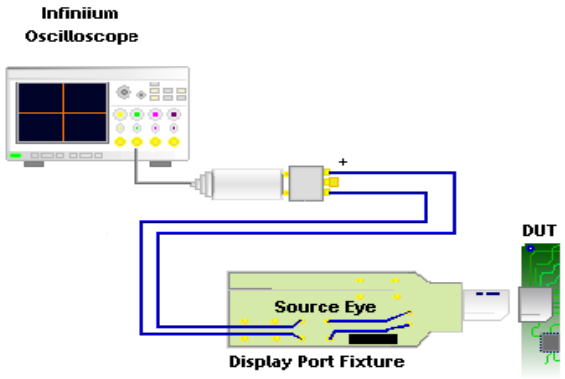


Figure 86 Sample connection diagram for source AUX channel tests without connecting to a reference sink

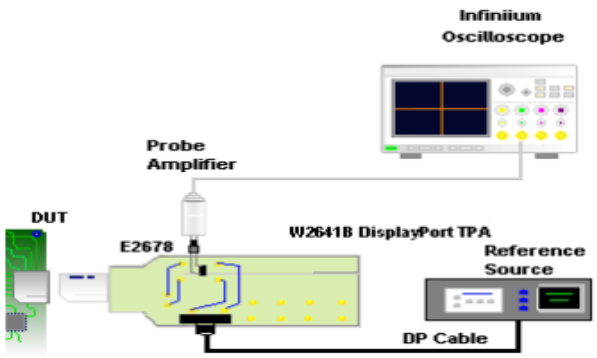


Figure 87 Sample connection diagram for sink AUX channel tests with sink DUT connected to a reference source

AUX Channel Unit Interval Test

Test ID

125000 – AUX Channel Unit Interval Test (Source)

125010 – AUX Channel Unit Interval Test (Sink)

Test Overview

The objective of the test is to evaluate the AUX Channel waveform, ensuring that the overall variation of the Manchester transaction Unit Interval stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Set up the parameter of the measurement trend:

   a Set up the Unit Interval measurement for the differential AUX Channel signal.

   b Set up the frequency measurement for the Clock signal.

   c Set up the measurement trend.

6 Set up the waveform Histogram on the measurement trend:

   a Initialize AUX Channel transactions and acquire the differential AUX Channel signal.

   b Identify the first and the last points for the desired transaction.

   c Zoom-in on the desired transaction.

   d Set up the Vertical Waveform Histogram on the measurement trend within the desired transaction.

   e Obtain the measurement for the mean, maximum and minimum values of the waveform Histogram.

7 Repeat step 6 ten times.

8 Report the measurement results.

PASS Condition

Manchester Transaction Unit Interval (UI_{MAN}):

Minimum = 0.4 µsec

Maximum = 0.6 µsec

Test References

See:

- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.4.2, Table 3-5*

Expected/Observable Results

The measured unit interval for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Test

Test ID

125001 – AUX Channel Eye Test (Source)

125011 – AUX Channel Eye Test (Sink)

Test Overview

The objective of this test is to evaluate the transmitter AUX Channel waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Apply a 300 kHz low-frequency cutoff (high-pass filter) to minimize impact caused due to baseline wander. HPF will have low frequency cutoff. LPF will have high frequency cutoff.

7 Apply a 500 MHz high-frequency cutoff (low-pass filter) to minimize impact caused due to instrument noise.

8 Apply measurement window on the AUX Channel signals, which starts immediately after the second pulse and ends immediately before auxiliary stop condition of the signal.

9 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

10 Set up the waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

11 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.
   c Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.
12 Check for any signal trajectories entering into the mask.
13 Report the measurement results.

PASS Condition

PASS Value = 290mV_diff_pp or higher

FAIL Value = lower than 290mV_diff_pp

The rendered Eye Diagram should not have signal trajectories entering the mask area.

Table 93 Eye Mask Vertices for AUX Channel for Manchester Transactions

Mask Point	Time (from EYE Center)	Minimum Voltage Value at Six Vertices (mV)
1	-185ns	0
2	-135ns	145
3	135ns	145
4	185ns	0
5	135ns	-145
6	-135ns	-145

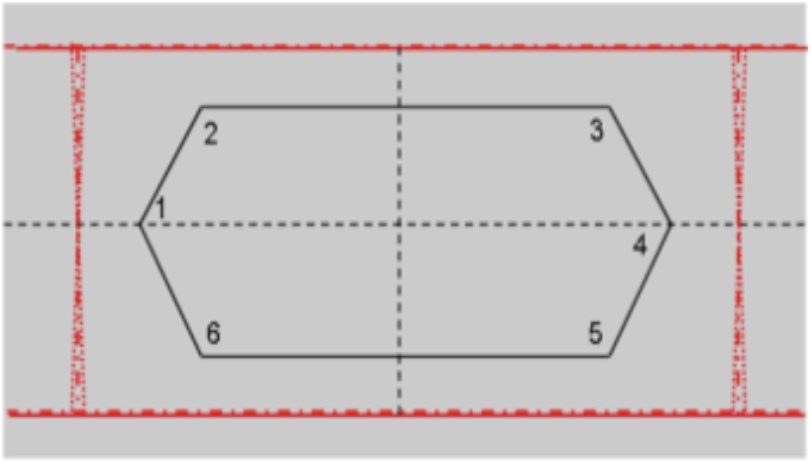


Figure 88 AUX Channel EYE Mask for Manchester Transactions

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.1*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.4.2.5, Figure 3-10 and Table 3-7*

Expected/Observable Results

The measured eye diagram for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

AUX Channel Peak-to-Peak Voltage Test

Test ID

125002 – AUX Channel Peak-to-Peak Voltage Test (Source)

125012 – AUX Channel Peak-to-Peak Voltage Test (Sink)

Test Overview

The objective of the test is to evaluate the transmitter AUX Channel Waveform, ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

a Enable measurement of all edges to obtain a statistical value of the measurement.

b Set up the measurement threshold.

c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

7 Set up the horizontal waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

8 If you have selected the “AUX Channel Eye Test” under the **Select Tests** tab of the compliance application:

a Set up the parameter of the Mask Test:

i Load the eye mask based on the settings in the Configuration Variable.

ii Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

iii Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.

b Check for any signal trajectories entering into the mask.

9 Report the measurement results.

PASS Condition

Table 94 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage at a transmitting device ($V_{AUX\text{-}DIFFp\text{-}p}$)	0.29V	1.38V

Test References

See:

- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.4.2, Table 3-5*

Expected/Observable Results

The measured peak-to-peak voltage for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Slew Rate Test

Test ID

125003 – AUX Channel Slew Rate Test (Source)

125013 – AUX Channel Slew Rate Test (Sink)

Test Overview

The objective of the test is to evaluate the AUX signaling edge rates, thereby ensuring that any crosstalk to the Main-Link signals are minimized.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

a Enable measurement of all edges to obtain a statistical value of the measurement.

b Set up the measurement threshold.

c Set up the Clock Recovery.

5 Set up the parameters to perform High Level Voltage (V_{HIGH}) and Low Level Voltage (V_{LOW}) for AUX Channel signal.

a Find V_{HIGH} by measuring the mode voltage of the high level of AUX Channel.

b Find V_{LOW} by measuring the mode voltage of the low level of AUX Channel.

c Calculate the peak-to-peak differential voltage of the AUX Channel signal and denote this value as $V_{Aux\_PP\_Diff\_Mean}$.
Note: Ignore any overshoot or ringing that follows the positive or negative transition.

d Calculate the time taken by the AUX Voltage to rise or fall between V20% and V80% levels. Denote this value at ΔT20-80%, which is either Rising Time at 20%-80% (RT20_80) or Falling Time at 20%-80% (FT20_80).

6 Calculate slew rate for all edges within the Capture window.

a The minimum value of Rising or Falling Time (in ns), denoted as ΔT20-80%_min, is measured as the worst-case slew rate.

b Multiply the value of $V_{Aux\_PP\_Diff\_Mean}$ (measured in step 5c) by 60% and denote the derived value as ΔV20-80%.

7 To determine the slew rate between the V20% and V80% vertices, calculate the rate of change using the following equation:
Slew Rate = Rate of Change = Rise/Run
= ΔV20-80% / ΔT20-80%
= ($V_{Aux\_PP\_Diff}$ x 0.6) / ΔT20-80%_min (V/ns)

8 Report the measurement results.

PASS Condition

The Slew Rate must be less than or equal to 375mV/ns for all transitions within the measurement window.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.3*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.4.2, Table 3-5*

Expected/Observable Results

The measured Slew Rate for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Calibration Test

Test ID

125021 – AUX Channel Eye Sensitivity Calibration (Reference Sink)

125031 – AUX Channel Eye Sensitivity Calibration (Reference Source)

Test Overview

The objective of this test is to calibrate the peak-to-peak voltage of the transmitter AUX Channel waveform by reference device (reference source or reference sink), ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.

2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

4 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

5 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

6 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

7 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

8 Set up the waveform Histogram on the AUX Channel eye diagram:

   a Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.

   b Set up the vertical waveform Histogram of width 0.6 UI at the center of the AUX Channel eye diagram.

   c Measure the V_{TOP} and V_{BASE} using the waveform Histogram mean value.

9 Repeat Step 8 three times.

10 Report the measurement results.

PASS Condition

Table 95 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage for AUX Channel Eye Sensitivity	0.24V	0.28V

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.3*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.4.2, Table 3-5*

Expected/Observable Results

The measured peak-to-peak voltage for the AUX Channel signal by reference device (reference source or reference sink) shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Test

Test ID

125041 – AUX Channel Eye Sensitivity Test (Source)

125051 – AUX Channel Eye Sensitivity Test (Sink)

Test Overview

The objective of the test is to evaluate the sensitivity to the AUX Channel Eye Opening of the DUT as per the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.
2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.
3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery.
5 Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.
6 Check if the reference device could detect the transaction or not.
7 Decode the AUX Channel signal and check whether the transaction passed or failed.
8 Report the measurement results.

PASS Condition

Determine whether the AUX Channel communication is successful. For example, the Transmitter DUT sends an AUX Request to the Reference Receiver. The Reference Receiver acknowledges and the Transmitter DUT responds to the to indicate that the acknowledgment was successfully received.

PASS = No errors observed in the response

FAIL = One or more errors observed

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.3*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.4.2, Table 3-5*

Expected/Observable Results

The measured AUX Channel transaction shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

13 DisplayPort 1.4a Inrush Tests

Overview

This section describes the normative and informative inrush tests for compliance verification of DisplayPort1.4a source and sink (a power consumer).

Test Point

The test fixture for inrush tests implements the schematic shown in Figure 89.

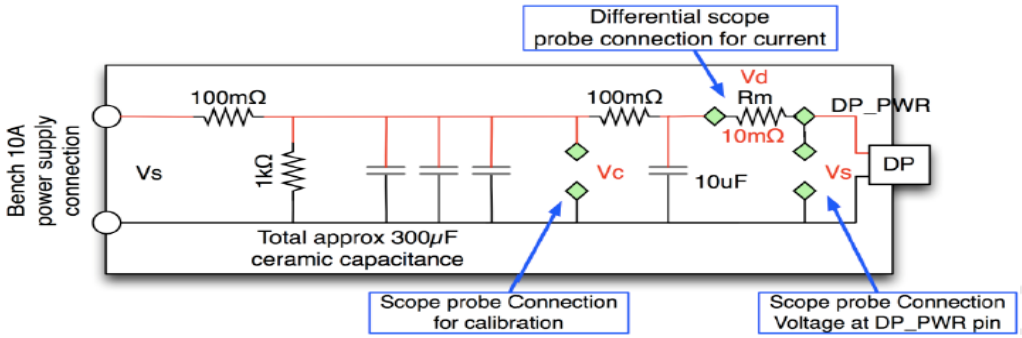


Figure 89 Schematics for testing a Power Consumer Device

The test fixture must be designed and used according to the following guidelines:

- A high gate voltage FET on the DP_PWR line is recommended to allow a fast connect capability, which allows a single connection event for testing. Without such an arrangement, multiple connections will be required to obtain a reasonable “worst-case” attachment event.
- Connection length between the power supply and the test fixture must be minimized. A maximum of four inches is recommended.
- The power supply must have enough outrush capability as to not negatively affect the test fixture’s outrush capability.
- The power supply must be run at 3.6V (3.3V + 10%) read across V_C.

Any Power Consumer test fixture must be calibrated using the Power User test fixture, as shown in Figure 89. Testing with the two fixtures combined should result in the approximate values given below. If required, the component values on the Power Consumer test fixture should be adjusted to match the expected results.

- V_C steady before connection = 3.6V
- V_C droop = ~3.1V
- Inrush Current = ~13.0A

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.4a Inrush Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort 1.4a Standards, select the option **1.4a** in the **Test Specification** area.

5 Select the option **AUX PHY and Inrush Tests** in the **Test Selection** area.

6 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

7 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

8 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

9 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

10 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

11 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

12 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

13 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Refer to "Settings for AUX PHY and Inrush Tests" on page 389 for instructions on setting the DisplayPort 1.4a InRush tests.

Inrush Energy Power Test

Test ID

127000 – Inrush Energy Power Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush energy power measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Energy $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 13.5$ Amps

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.6*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.2.3*

Expected/Observable Results

The measured worst case inrush energy power for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Inrush Peak Current Test

Test ID

127001 – Inrush Peak Current Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush peak current measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Energy $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 13.5$ Amps

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.6*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.2.3*

Expected/Observable Results

The measured worst case inrush peak current for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

14 DisplayPort 1.4 Source Tests

Overview

This section describes the normative and informative main link physical layer tests for compliance verification of DisplayPort 1.4 source, sink and cable devices.

Test Point Definition for DisplayPort 1.4 Tests

Five different test points are identified for the physical layer measurement. See Figure 90.

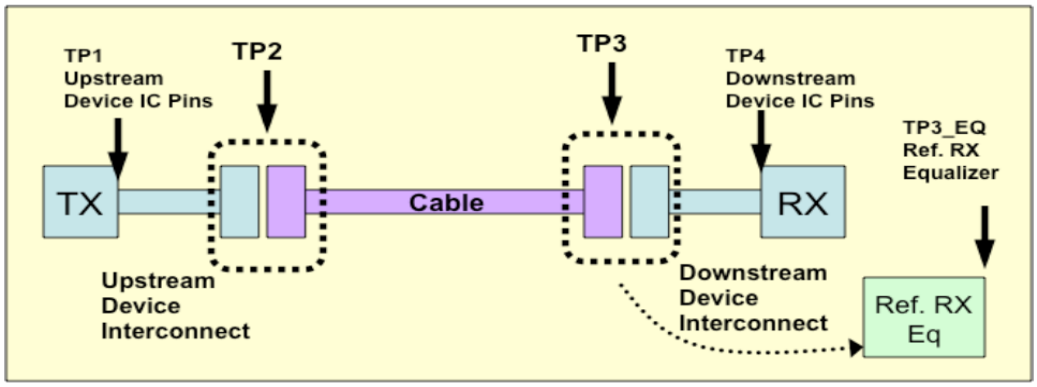


Figure 90 Test Points in a DisplayPort InterConnect System

Table 96 defines the Test Points used for various DisplayPort 1.4 Tests:

Table 96 Test Points for DisplayPort Tests

Test Point	Description
TP1	At the pins of the Transmitter Device
TP2	At the test interface on a test access fixture as close as possible to the DP mated connection to a Source device
TP3	At the test interface on a test access fixture as close as possible to the DP mated connection to a Sink device
TP3_EQ	At TP3, when a defined cable model with equalizer is applied. There are two defined cable models: ▪ Worst Cable Model as defined in VESA DisplayPort 1.4 Standard, ▪ Zero length, zero loss cable. The equalizer is also defined in VESA DisplayPort 1.4 Standard
TP3_DFE	At TP3, when a defined HBR3 cable model with CTLE and DFE are applied.
TP4	At the pins of a receiving device

NOTE Among the patterns that are used at the test points described above, HBR2CPAT pattern is the same as CP2520. The CP2520 pattern can be further divided into “CP2520.Pattern1”, “CP2520.Pattern2”, or “CP2520.Pattern3”. The TPS4 pattern is “CP2520.Pattern3” (HBR2CPAT Pattern 3).

Cable Models

The two cable models defined in VESA DisplayPort 1.4 Standard are:

1 Worst Case Cable Model—To achieve the TP3_EQ signal with the worst case cable model:

- Acquire the signal at TP2.
- Embed the TP2 signal with a “worst case” HBR cable model using an InfiniiSim Waveform Transformation Toolset software to emulate the insertion loss as defined in Figure 4-10 of the VESA DisplayPort 1.4 Standard.
  - For Standard DisplayPort: The “CIC_rev0p6.s4p” cable model transfer function is used for RBR, HBR, and HBR2 whereas the “Source_100ohms_CIC.sp4” cable model transfer function is used for HBR3.
  - For USB Type-C: The “c2dp_90ohms_0psSkew.s4p” cable model transfer function is used for RBR, HBR, and HBR2 whereas “Source_100ohms_CIC.sp4” cable model transfer function is used for HBR3.
- Finally, apply the HBR, HBR2 or HBR3 equalization using the Serial Data Equalization software as defined in the VESA DisplayPort 1.4 Standard.

2 Zero Length Cable Model—To achieve the TP3_EQ signal with the zero length cable model:

- Acquire the signal at TP2.
- No cable model is embedded for the Zero Length cable model.
- Finally, apply the HBR, HBR2 or HBR3 equalization using the Serial Data Equalization software as defined in the VESA DisplayPort 1.4 Standard.

Equalization

When equalization is required, use the CTLE (Continuous Time Linear Equalization) transfer function, as given in the VESA DisplayPort 1.4 Standard.

For main link, use the CTLE model or the DFE model with the following transfer function for HBR (2.7 Gbps):

The HBR Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s + \omega_z}{(s + \omega_{p1})(s + \omega_{p2})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{\sqrt{\omega^2 + \omega_z^2}}{\sqrt{\omega^2 + \omega_{p1}^2} \cdot \sqrt{\omega^2 + \omega_{p2}^2}}$$

where

$$\omega_z = 2\pi(0.725 \times 10^9)$$

$$\omega_{p1} = 2\pi(1.35 \times 10^9)$$

$$\omega_{p2} = 2\pi(2.5 \times 10^9)$$

Figure 91 Transfer Function of the CTLE/DFE model for HBR

Table 97 CTLE Model for HBR

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
Gain	1.0	1.0
Zero Frequency	0.725 GHz	0.725 GHz
Pole 1 Frequency	1.35 GHz	1.35 GHz
Pole 2 Frequency	2.5 GHz	2.5 GHz

For main link, use the CTLE model or the DFE model with the following transfer function for HBR2 (5.4 Gbps):

The HBR2 Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})(s+\omega_{p3})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{\sqrt{\omega^2+\omega_z^2}}{\sqrt{\omega^2+\omega_{p1}^2}\cdot\sqrt{\omega^2+\omega_{p2}^2}\cdot\sqrt{\omega^2+\omega_{p3}^2}}$$

where

$\omega z = 2\pi\ (0.64 \times 10^9)$ for upstream device compliance

and

$\omega p1 = 2\pi\ (2.7 \times 10^9)$

$\omega p2 = 2\pi\ (4.5 \times 10^9)$

$\omega p3 = 2\pi\ (13.5 \times 10^9)$

Figure 92 Transfer Function of the CTLE/DFE model for HBR2

Table 98 CTLE Model for HBR2

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
Gain	1.0	1.0
Zero Frequency	0.64 GHz	0.64 GHz
Pole 1 Frequency	2.7 GHz	2.7 GHz
Pole 2 Frequency	4.5 GHz	4.5 GHz
Pole 3 Frequency	13.5 GHz	13.5 GHz

For main link, use the CTLE model or the DFE model with the following transfer function for HBR3 (8.1 Gbps):

For each acquisition, using the appropriate cable model from Table 3-2, the analyzer software sweeps the range of CTLE Transfer Functions as defined in Table 3-4, and then uses the value with the optimal EYE Height (TP3_CTLE_Optimal) for the compliance test result (see Figure 3-3)

$$H(s) = A_{ac} \times \omega_{p2} \times \frac{[s + (A_{dc} / A_{ac}) \times \omega_{p1}]}{(s + \omega_{p1}) \times (s + \omega_{p2})}$$

where:

- A_{ac} is 3.5dB
- A_{dc} is an integer within the range of 0 through -8dB, inclusive, in 1 db steps
- $\omega_{p1} = 3.03\text{GHz}$
- $\omega_{p2} = 5.60\text{GHz}$

Test equipment analyzer software shall store each TP3_CTLE waveform and associated recovered clock waveform to be used in TP3_DFE compliance test evaluation, if needed

Figure 93 Transfer Function of the CTLE/DFE model for HBR3

Table 99 CTLE Model for HBR3

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
AC Gain	3.5 dB	3.5 dB
Pole 1 Frequency	3.03 GHz	3.03 GHz
Pole 2 Frequency	5.60 GHz	5.60 GHz

HBR3 Reference DFE: The HBR3 Reference Equalizer includes a CTLE cascaded with a one-tap adaptive DFE with a coefficient limited to less than 50mV. The DFE behavior is described as:

$$y_k = x_k - d1 sgn(y_{k-1})$$

where, y_k is the DFE differential output voltage, y_k* is the decision function output voltage, x_k is the differential input voltage after CTLE, d1 is the feedback coefficient, k is the UI sample.

A flowchart representing the HBR3 Reference Equalizer is shown in Figure 94.

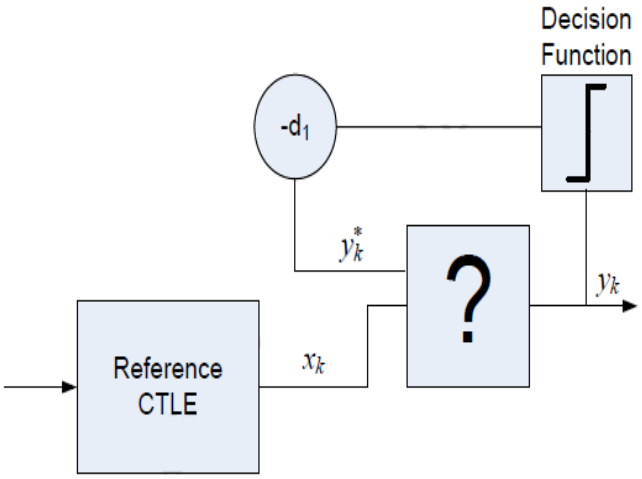


Figure 94 HBR3 Reference Equalizer based on the DFE

Table 100 DFE Model for HBR3

DFE Parameter	Value
Number of Taps	1
DFE Mode	Auto
Eye Width	0.0 UI
Max Tap value	0.050
Min Tap value	0.0

Clock Recovery

When Clock Recovery is required, the clock recovery technique follows the definition of the receiver PLL as defined in Section 3.5.2.5 of the VESA DisplayPort 1.4 Standard. For main link, use the second-order clock recovery function with a closed loop tracking bandwidth and damping factor, with respect to the PRBS7 pattern, as shown in Table 101:

Table 101 Main Link Second-Order Clock Recovery Function

Bit Rate	Bandwidth	Damping Factor
HBR3 (8.1 Gbps)	15 MHZ	1.00
HBR2 (5.4 Gbps)	10 MHz	1.00
HBR (2.7 Gbps)	10 MHz	1.51
RBR (1.62 Gbps)	5.4 MHz	1.51

Test Point Definition for DisplayPort 1.4 Source Tests

Test the Source DUT at Test Point 2 (TP2) as shown in Figure 95. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

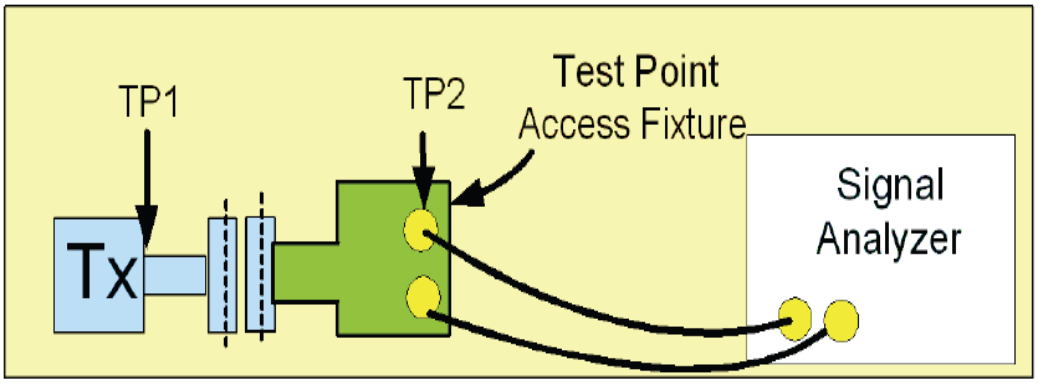


Figure 95 Test Point 2 Connection for DisplayPort 1.4 Source Tests

Table 102 defines the test point fixtures and instruments used for DisplayPort 1.4 Source Tests:

Table 102 Test Point Fixtures and Instruments for DisplayPort 1.4 Source Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-P* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-P* ▪ Luxshare ICT mDP Plug (mDP-TPA-P)** For USB Type-C Connector ▪ N7015A Type-C High-Speed Test Fixture ▪ Wilder Technologies DPC-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.4 Source Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort 1.4 Standards, select the option **1.4** in the **Test Specification** area.

5 The option **Physical Layer Tests** appears by default in the **Test Selection** area.

6 Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.

7 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

8 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

9 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

10 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

11 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

12 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

13 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

14 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DisplayPort 1.4 Source Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

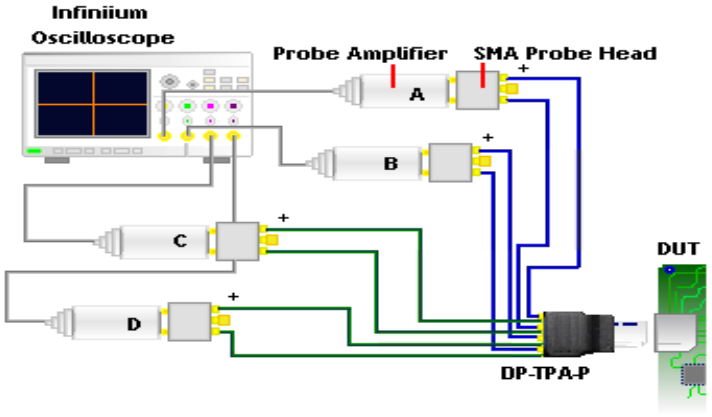


Figure 96 Sample connection diagram for DisplayPort 1.4 Source Tests

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Source tests (either differential or single-ended) to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1. In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.
2. On the **Test Setup** window,
   - *a* Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.
   - *b* In the **DUT Info** area, the **Device Type** is selected as **Source** by default. The **Connector Type** is grayed out.
   - *c* In the **Test Info** area, the **Test Type** is selected as **Differential Tests** by default. Select **Single-Ended Tests** from the drop-down options for the respective tests to appear in the **Select Tests** tab. From the **Data Pattern** drop-down options, select **Standard DP Pattern** or **Arbitrary Pattern**, based on the type of pattern generated.
   - *d* In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.
3. Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1. Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.
2. On the **Connection Setup** window,
   - *a* Select the appropriate option in the **Fixture Type** to indicate where the DUT is connected to.
   - *b* Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.
   - *c* In the **Channel Selection** area, assign appropriate channels to lanes.
3. Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of source tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.4 Source Tests" on page 495 to complete the task flow for DUT setup along with configuring the Compliance Application to run each test.

Source Eye Diagram Test

Test ID

For Standard DP Pattern:

- 1210001, 1210002, 1210003, 1210004 – Eye Diagram Test

For Arbitrary Pattern:

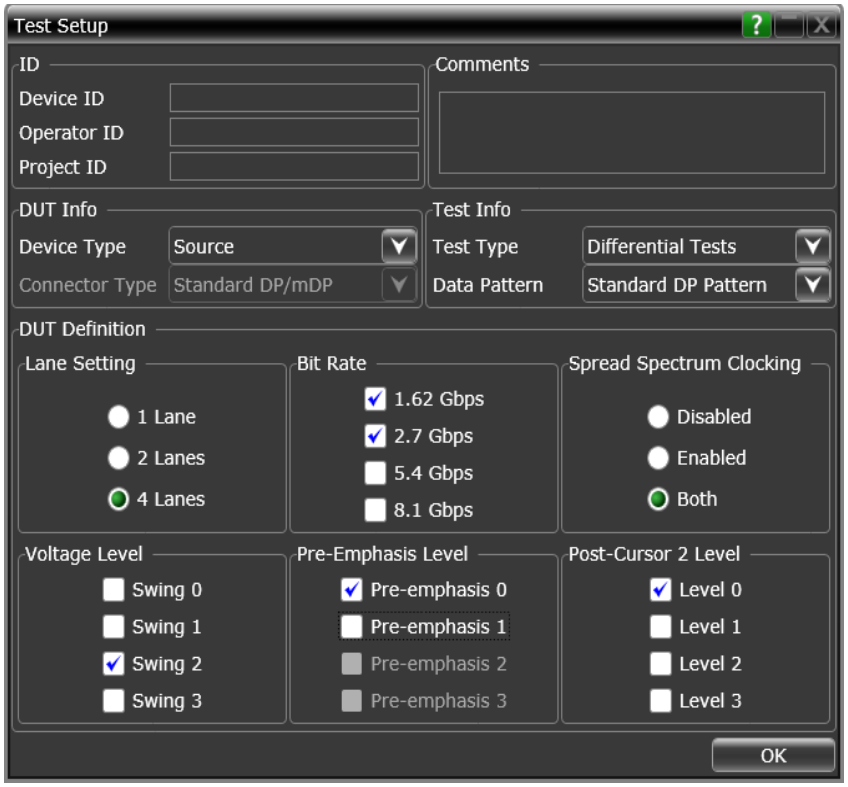
- 1310001, 1310002, 1310003, 1310004 – Eye Diagram Test

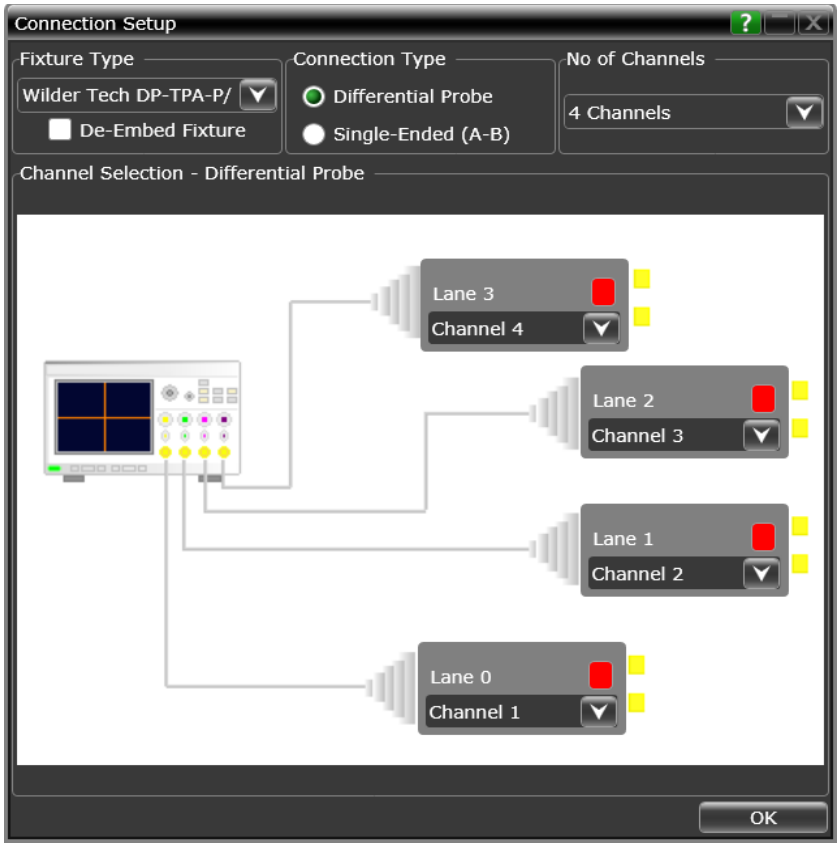
Test Overview

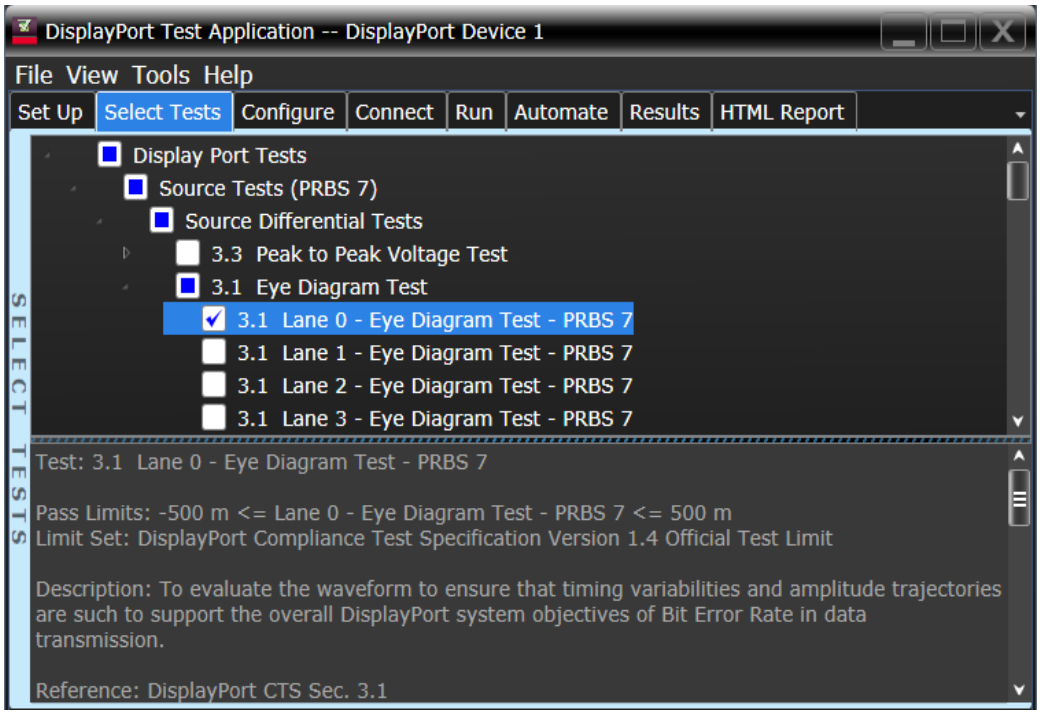
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Measure V_{TOP} and V_{BASE} of the input signal using the pattern folding.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the input signal eye diagram to measure the left edge.
7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the eye height of the eye diagram using the Histogram.
9 Measure the jitter of the eye diagram using the Histogram.
10 Calculate the eye width based on the measured jitter of the eye diagram.

11 Check for any signal trajectories that may have entered into the mask.

12 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 103 shows the voltage and time coordinates for the mask used in the eye diagram.

Table 103 Eye Diagram Mask Coordinates

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	**High (2.7 Gb/s)**
1	0.127, 0.000	0.210, 0.000
2	0.291, 0.160	0.355, 0.140
3	0.500, 0.200	0.500, 0.175
4	0.709, 0.200	0.645, 0.175
5	0.873, 0.000	0.790, 0.000
6	0.709,-0.200	0.645,-0.175
7	0.500,-0.200	0.500,-0.175
8	0.291,-0.160	0.355,-0.140

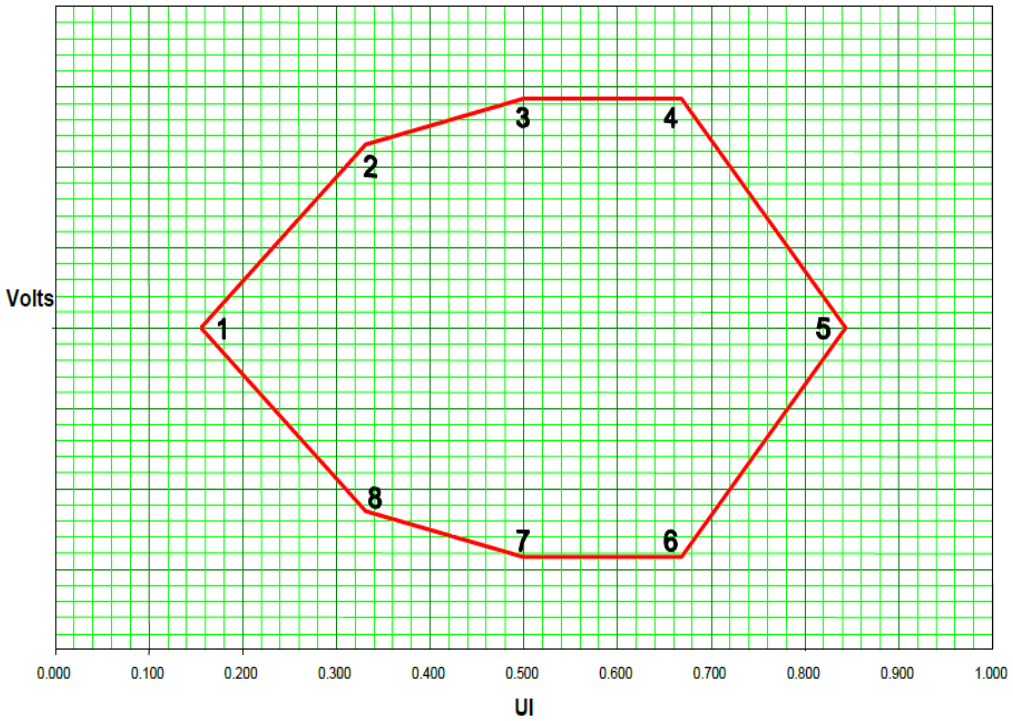


Figure 97 The Source Eye Mask

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort Standard Version 1.4, Section 3.5.2.8.2, Table 3-28 for RBR, Table 3-27 for HBR*

Expected/Observable Results

The measured eye diagram for the source degraded signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test

Test ID

For Standard DP Pattern:

- 1220001, 1220002, 1220003, 1220004 – Total Jitter Test

For Arbitrary Pattern:

- 1320001, 1320002, 1320003, 1320004 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

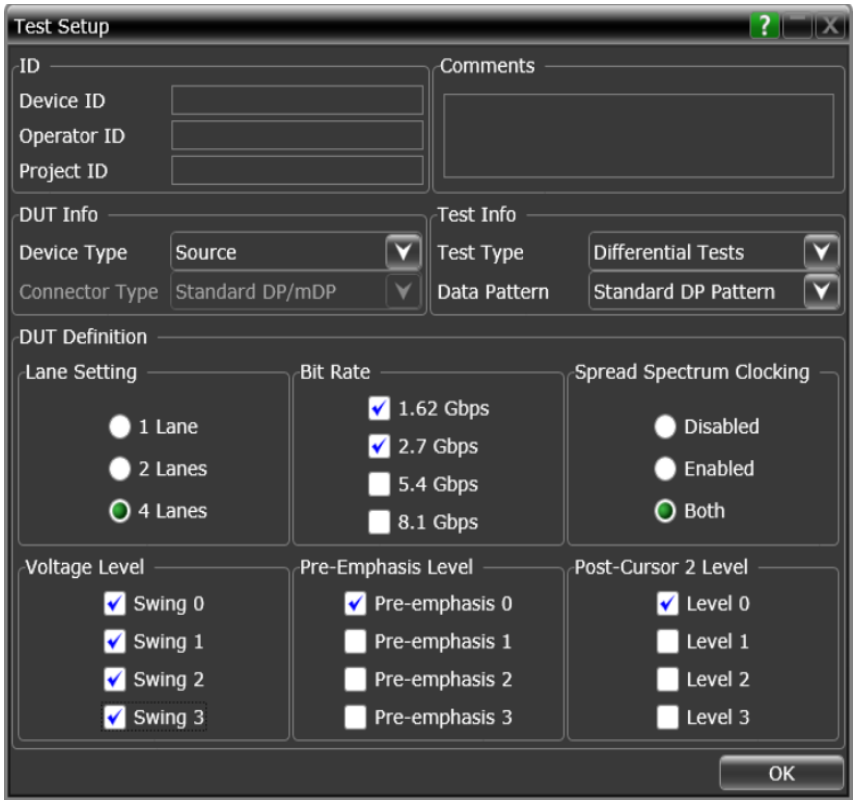
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

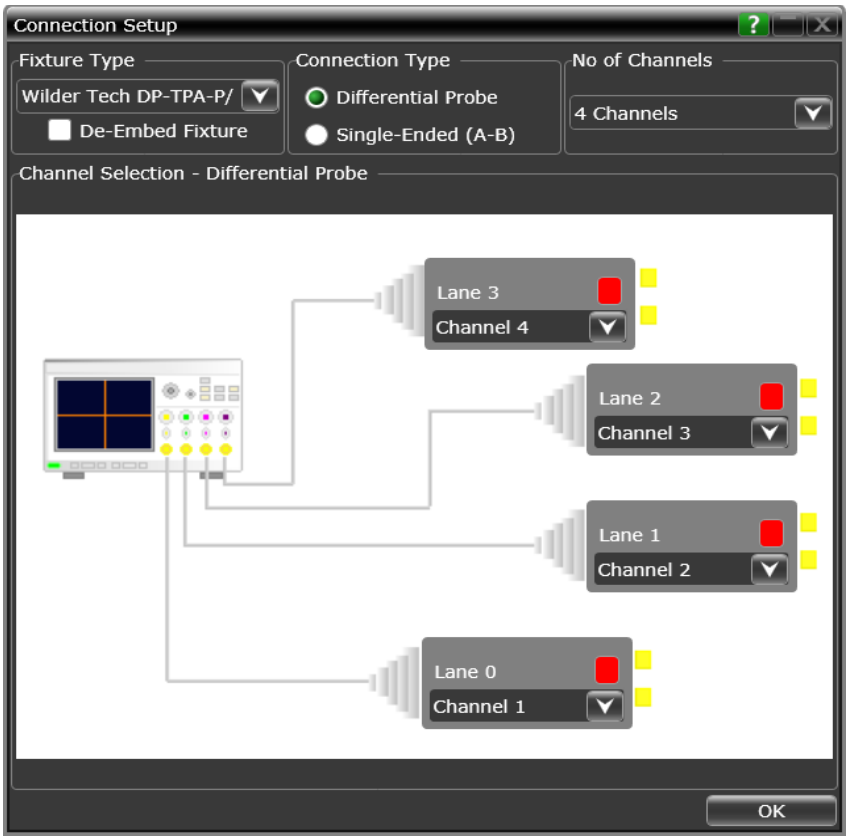
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

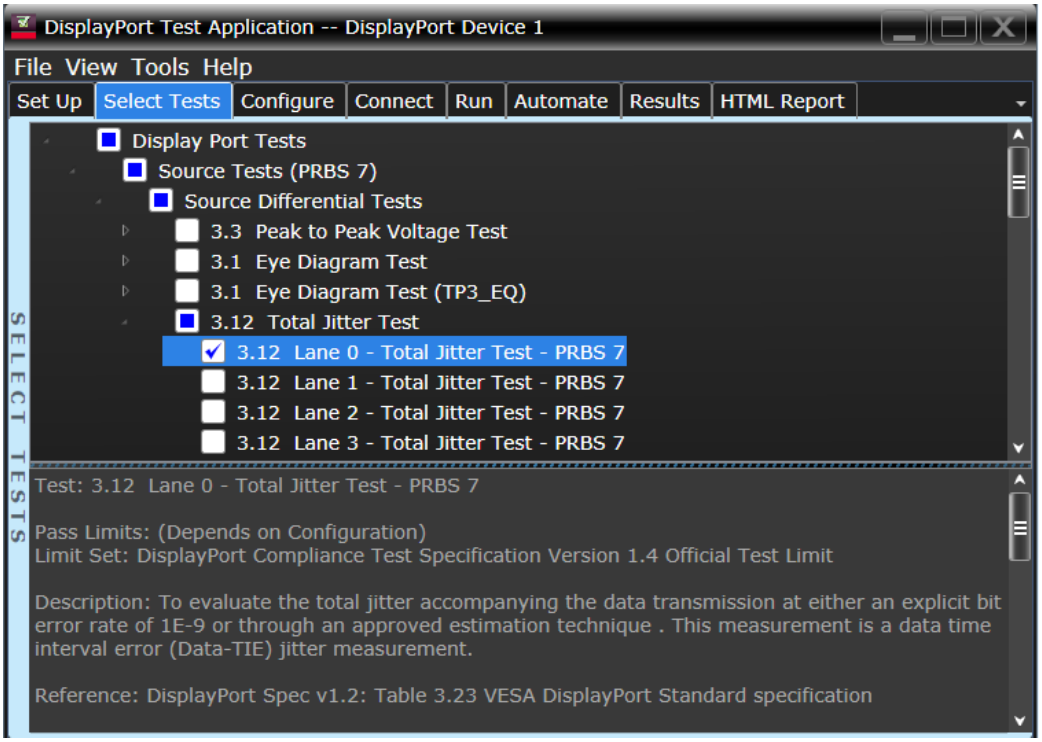
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Report the measurement results.

PASS Condition

Table 104 Total Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
Ap-p	0.294 UI	0.420 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
Ap-p	0.180 UI	0.270 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2.7.2, Table 3-23*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non-ISI Jitter Test

Test ID

For Standard DP Pattern:

- 1230001, 1230002, 1230003, 1230004 – Non ISI Jitter Test

For Arbitrary Pattern:

- 1330001, 1330002, 1330003, 1330004 – Non ISI Jitter Test

Test Overview

The objective of the test is to evaluate the amount of Non ISI jitter accompanying the data transmission.

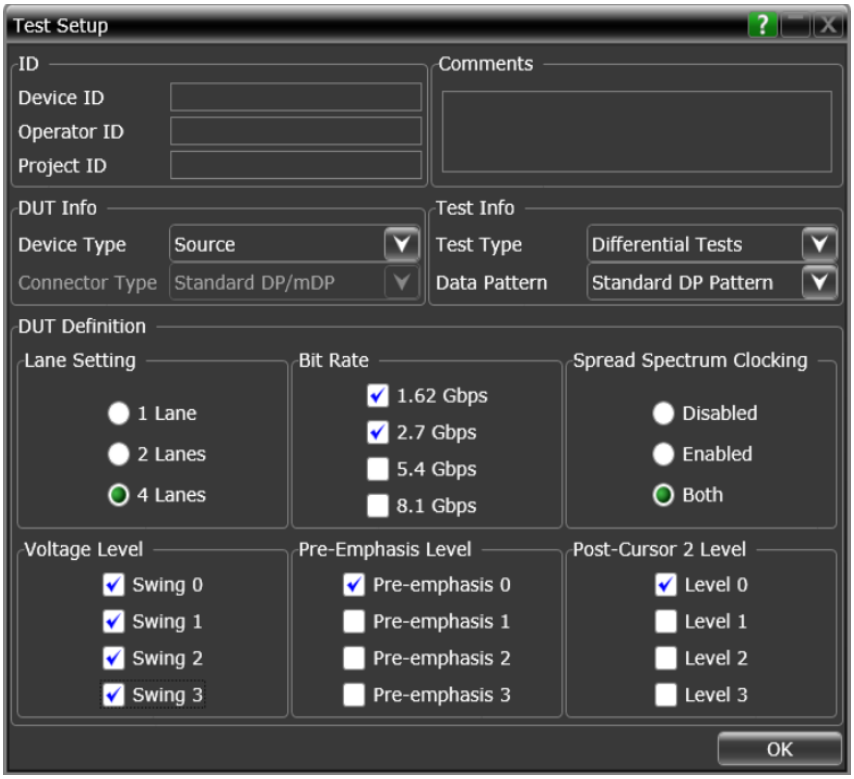
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

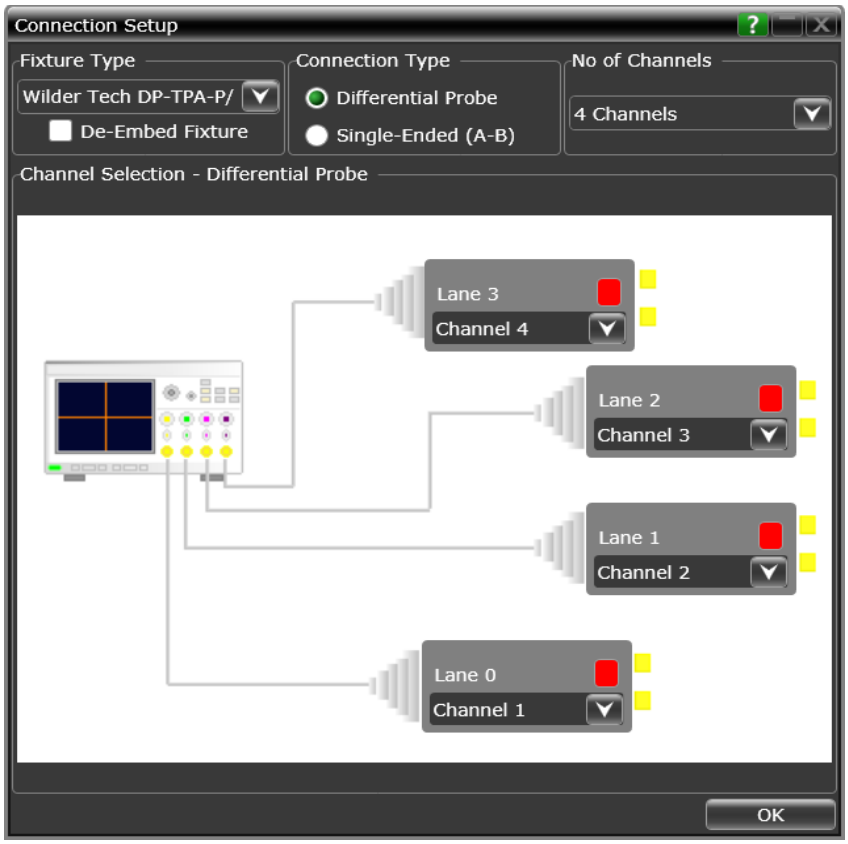
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

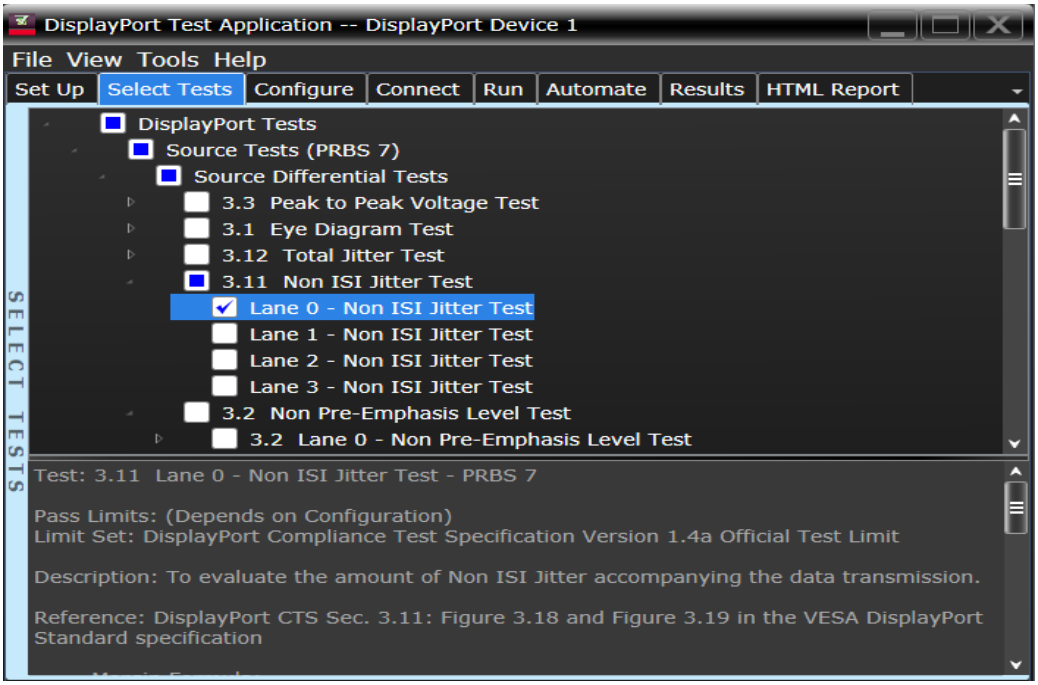
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Calculate the Non ISI jitter using the following equation:

$$\text{Non ISI Jitter} = \text{TJ} - \text{ISI}$$

7 Report the measurement results.

PASS Condition

Table 105 Non-ISI Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.260 UI	0.276 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.160 UI	0.170 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.11*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2.7.2, Table 3-23*

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Pre-Emphasis Level Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1261001, 1261002, 1261003, 1261004 – Non Pre-Emphasis Level Test (Swing 1/Swing 0)
- 1262001, 1262002, 1262003, 1262004 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263001, 1263002, 1263003, 1263004 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

For Standard DP Pattern (HBR2 and HBR3):

- 1264101, 1264102, 1264103, 1264104 – Non Pre-Emphasis Level Test (Swing 2/Swing 0)
- 1262101, 1262102, 1262103, 1262104 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263101, 1263102, 1263103, 1263104 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

For Arbitrary Pattern:

- 1364101, 1364102, 1364103, 1364104 – Non Pre-Emphasis Level Test (Swing 2/Swing 0)
- 1362101, 1362102, 1362103, 1362104 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1363101, 1363102, 1363103, 1363104 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

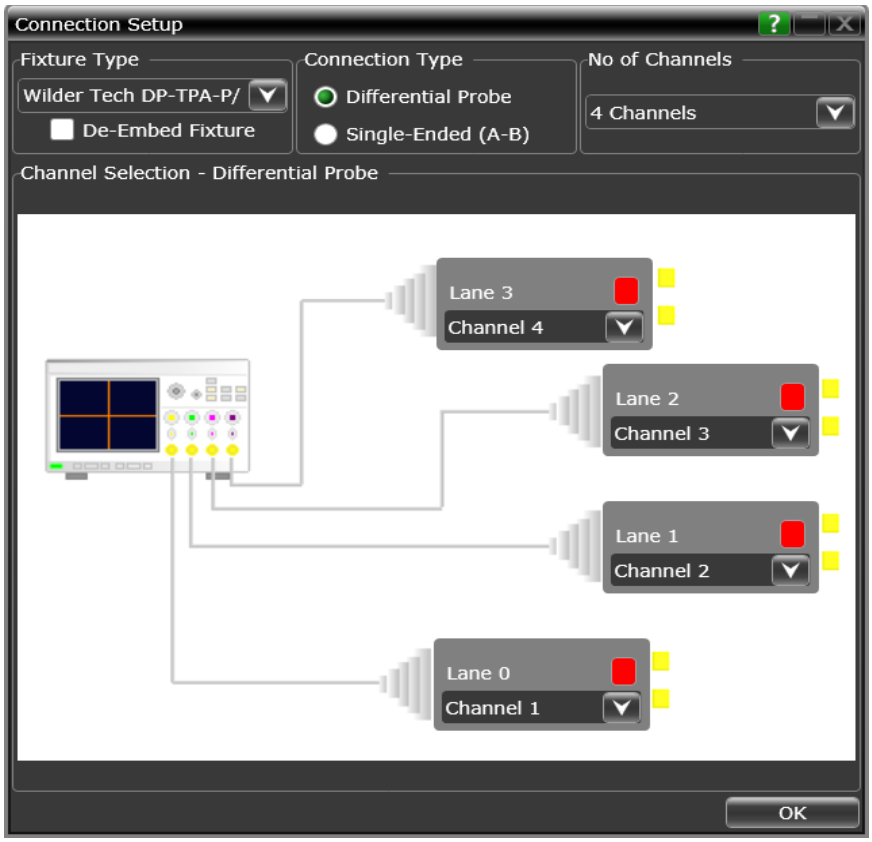
Test Overview

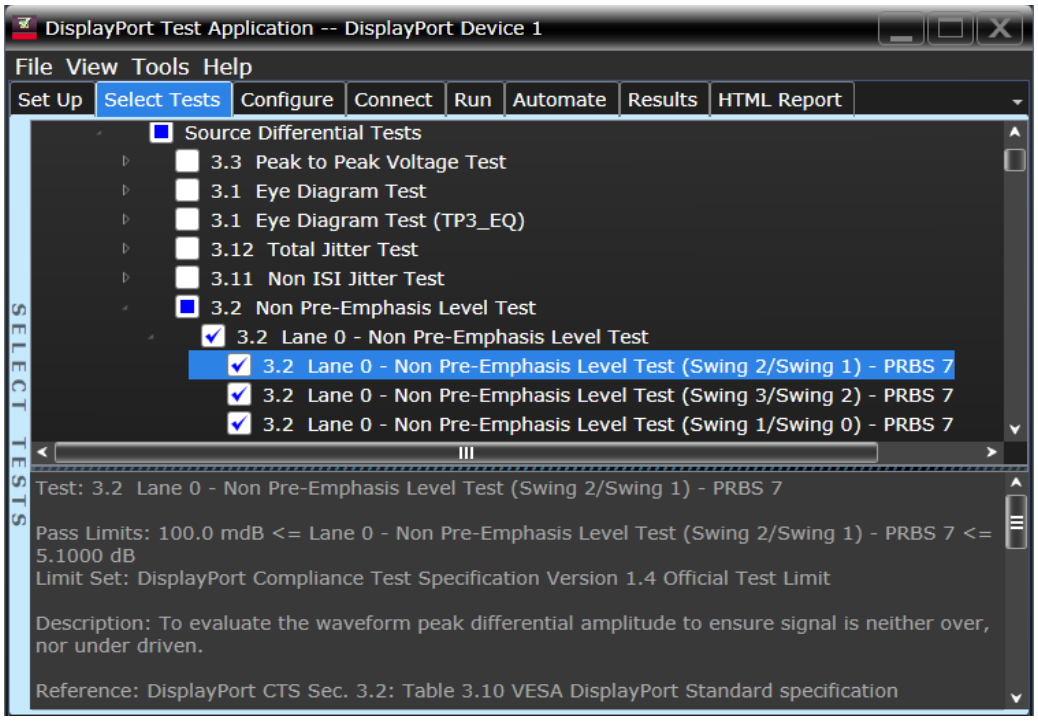
The objective of this test is to ensure that the system budget elements are obeyed and to ensure that the level settings are monotonic so that the sink relies on the source to incrementally increase upon request by the sink.

Test Conditions for Non Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR3 – PLTPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For Voltage Level A with no pre-emphasis level:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

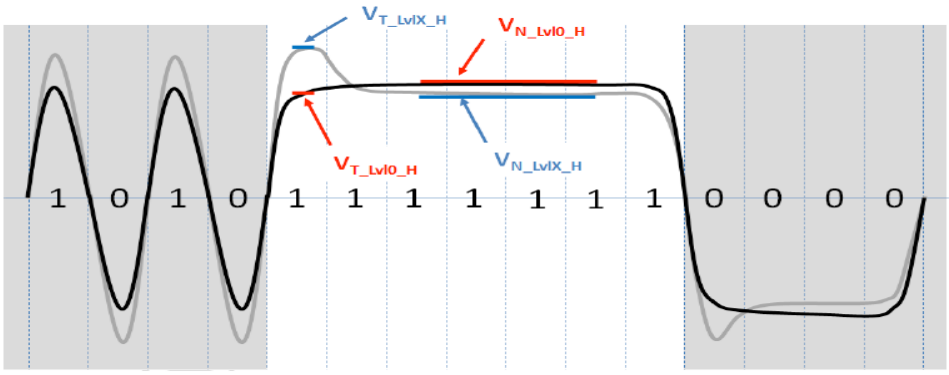


Figure 98 High Voltage measurement for RBR and HBR

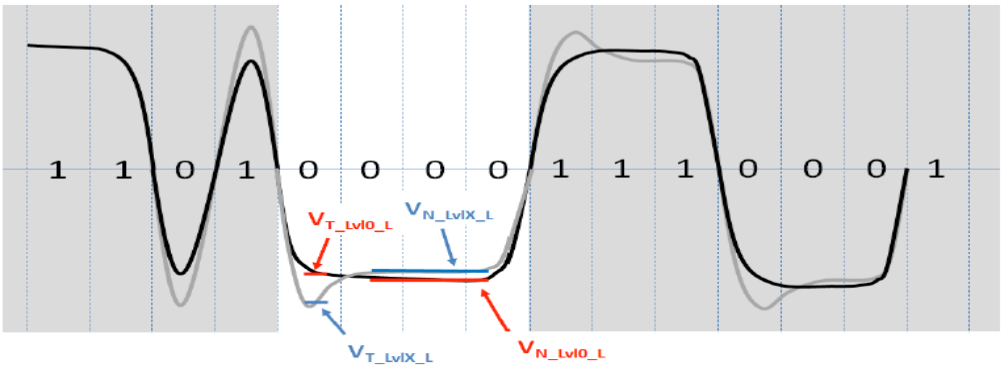


Figure 99 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR3 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted zeros of the pattern.

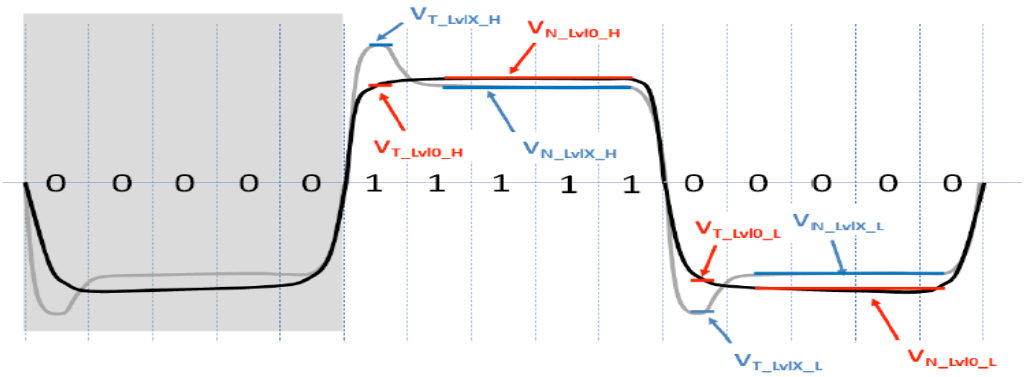


Figure 100 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_Lvl0\_PP} = V_{T\_Lvl0\_H} - V_{T\_Lvl0\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_Lvl0\_PP} = V_{N\_Lvl0\_H} - V_{N\_Lvl0\_L}$$

2 Repeat Step 1 for Voltage Level B with no pre-emphasis level.

3 Calculate the non pre-emphasis level output voltage ratio using the equation:

Non Pre-Emphasis Level = $20 * \text{Log}_{10}[\text{Voltage Level A } V_{N\_Lvl0\_PP} / \text{Voltage Level B } V_{N\_Lvl0\_PP}]$

4 Report the measurement results.

PASS Condition

For each level setting testes, the following equation should be used:

$\text{Resultant} = 20 * \text{Log}_{10}[\text{Voltage}_{\text{Peak-Peak\_LevelA}} / \text{Voltage}_{\text{Peak-Peak\_LevelB}}]$

Table 106 Compared Levels

Measurement#	$\text{Voltage}_{\text{Peak-Peak\_LevelA}}$	$\text{Voltage}_{\text{Peak-Peak\_LevelB}}$
RBR & HBR		
1	Level 1 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)
2	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
3*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)
HBR2 and HBR3		
4	Level 2 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)

Table 106 Compared Levels

Measurement#	$Voltage_{Peak\text{-}Peak\_LevelA}$	$Voltage_{Peak\text{-}Peak\_LevelB}$
5	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
6*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)

* if device optionally capable of Level 3

The resultants specifications are as identified below:

Measurement 1: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 2: 0.1 dB ≤ Resultant ≤ 5.1 dB

Measurement 3: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 4: 5.2 dB ≤ Resultant ≤ 6.9 dB

Measurement 5: 1.6 dB ≤ Resultant ≤ 3.5 dB

Measurement 6: 1 dB ≤ Resultant ≤ 4.4 dB

Table 107 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}OUTPUT\text{-}RATIO\_RBR\_HBR}$*	Ratio of Output Voltage Level 1/Level 0	0.8	-	6.0	dB	Measured on non-transition bits at Pre-emphasis level 0 setting. Support for Voltage Level 3 is optional.
	Ratio of Output Voltage Level 2/Level 1	0.1	-	5.1	dB	
	Ratio of Output Voltage Level 3/Level 2	0.8	-	6.0	dB	

* Earlier versions of DisplayPort have the Main-Link DPTX output voltage ratios to ensure that the DPTX supports the required range of output voltage levels. For HBR2 and higher, you need not test or specify exclusively because the compliance test point is moved to TP3_EQ. So, the ratio of output voltage levels is removed from the table above for HBR2 and above.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.2*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-18*

Expected/Observable Results

The measured output voltage level ratio of the non pre-emphasis level test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Pre-Emphasis Level Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1270001, 1270002, 1270003, 1270004 – Pre-Emphasis Level Test

For Standard DP Pattern (HBR2 and HBR3):

- 1270501, 1270502, 1270503, 1270504 – Pre-Emphasis Level Test

For Arbitrary Pattern:

- 1370501, 1370502, 1370503, 1370504 – Pre-Emphasis Level Test

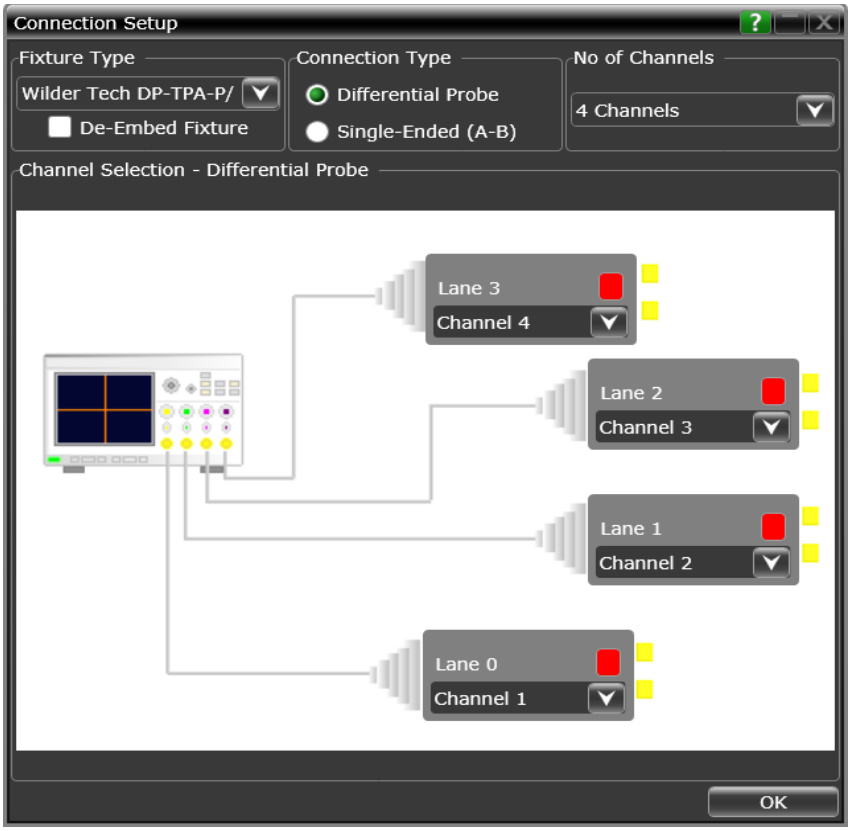
Test Overview

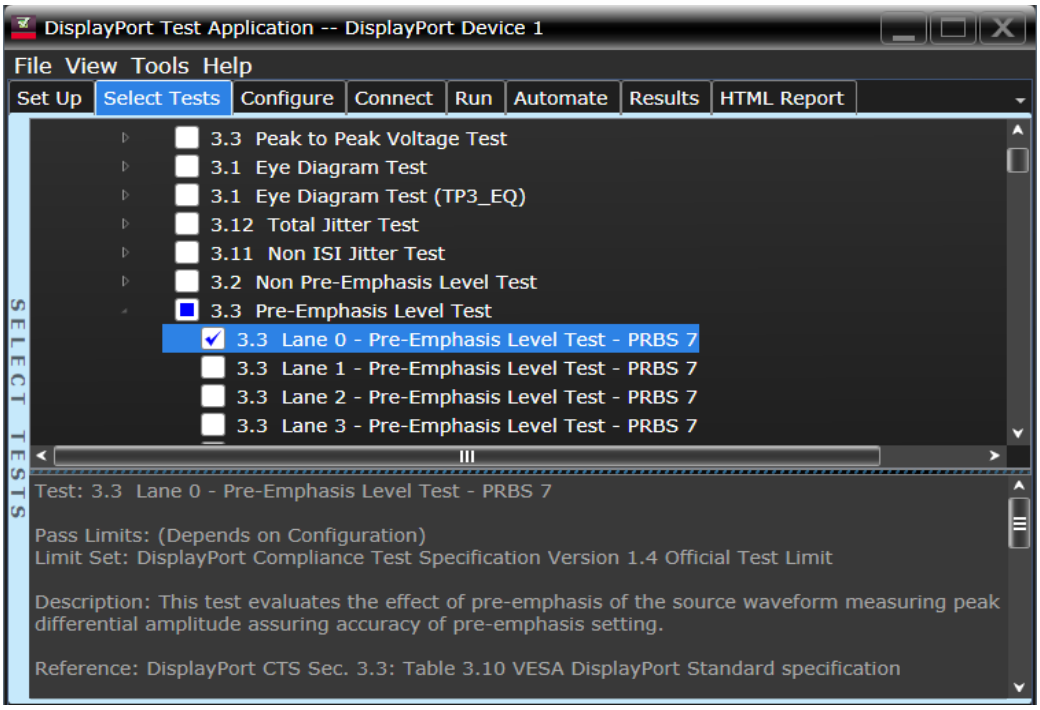
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings.

Test Conditions for Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.4 Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR3– PLTPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given Voltage Level and a Pre-Emphasis Level X:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

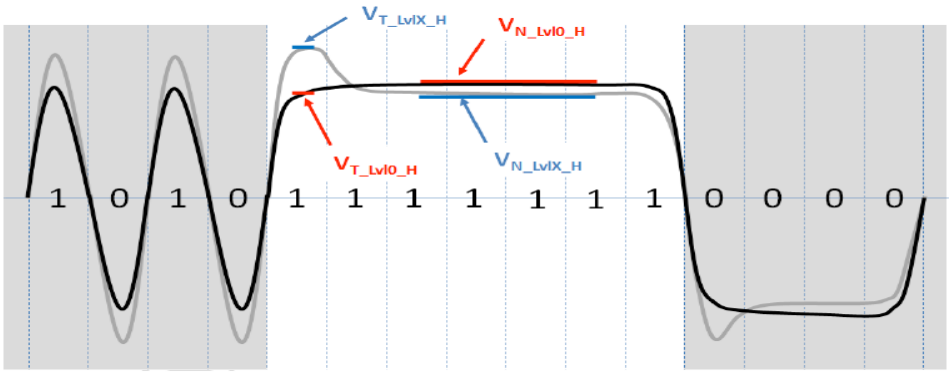


Figure 101 High Voltage measurement for RBR and HBR

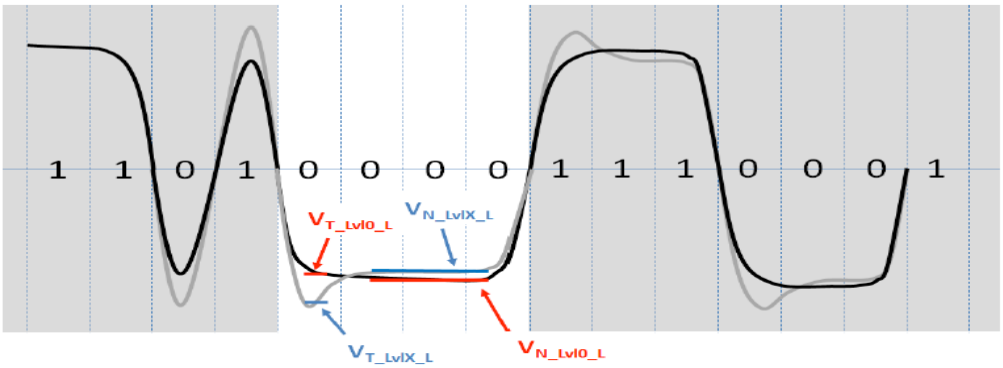


Figure 102 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR3 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted zeros of the pattern.

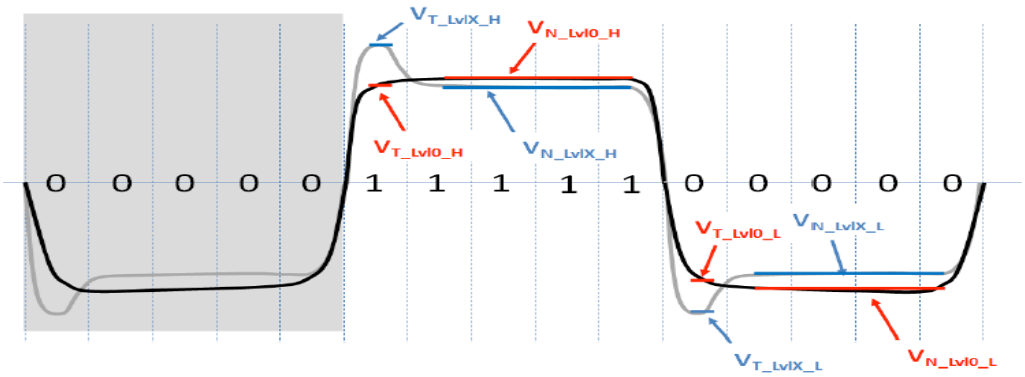


Figure 103 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

l Calculate the pre-emphasis level using the equation:

$$\text{Pre-Emphasis}_{LvlX} = 20 * \text{Log}_{10}[V_{T\_LvlX\_PP} / V_{N\_LvlX\_PP}]$$

2 For Pre-Emphasis Level 0 (no pre-emphasis level), the result for $\text{Pre-Emphasis}_{Lvl0}$ is compared with the maximum pre-emphasis disabled limit.

3 Repeat Step 1 for the next Pre-Emphasis level and for each Pre-Emphasis levels, compare the pre-emphasis delta with the pre-emphasis delta limits.

4 Calculate the pre-emphasis delta using the equation:

$$\text{Pre-Emphasis Delta (Level 1 vs Level 0)} = \text{Pre-Emphasis}_{Lvl1} - \text{Pre-Emphasis}_{Lvl0}$$

$$\text{Pre-Emphasis Delta (Level 2 vs Level 1)} = \text{Pre-Emphasis}_{Lvl2} - \text{Pre-Emphasis}_{Lvl1}$$

$$\text{Pre-Emphasis Delta (Level 3 vs Level 2)} = \text{Pre-Emphasis}_{Lvl3} - \text{Pre-Emphasis}_{Lvl2}$$

5 Report the measurement results.

PASS Condition

Pre-emphasis values for the Level 0 (OFF) state (Normative)

Level 0 (OFF) Pre-emphasis measurement:

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl0\_PP} / \text{Voltage}_{N\_Lvl0\_PP}]$ for all supported levels.

Level 0 (OFF) Pre-emphasis Measurement condition: +0.25 dB $\geq$ Resultant

Pre-emphasis Delta values for:

a Level 1 vs. Level 0 Pre-emphasis settings (NORMATIVE)

b Level 2 vs. Level 1 Pre-emphasis settings (NORMATIVE)

c Level 3 vs. Level 2 Pre-emphasis settings (NORMATIVE)

Pre-emphasis Delta measurements:

- Level 1 vs. Level 0

Resultant = 20 * Log [$Voltage_{T\_Lvl1\_PP}$ / $Voltage_{N\_Lvl1\_PP}$] - 20 * Log [$Voltage_{T\_Lvl0\_PP}$ / $Voltage_{N\_Lvl0\_PP}$] for Voltage Swing Levels 0, 1 and 2.

- Level 2 vs. Level 1

Resultant = 20 * Log [$Voltage_{T\_Lvl2\_PP}$ / $Voltage_{N\_Lvl2\_PP}$] - 20 * Log [$Voltage_{T\_Lvl1\_PP}$ / $Voltage_{N\_Lvl1\_PP}$] for Voltage Swing Levels 0 and 1.

- Level 3 vs. Level 2

Resultant = 20 * Log [$Voltage_{T\_Lvl3\_PP}$ / $Voltage_{N\_Lvl3\_PP}$] - 20 * Log [$Voltage_{T\_Lvl2\_PP}$ / $Voltage_{N\_Lvl2\_PP}$] for Voltage Swing Level 0, if supported.

Table 108 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX-PREEMP-OFF}$	Maximum Pre-emphasis when disabled	-	-	0.25	dB	Pre-emphasis Level 0 setting must not show any pre-emphasis at TP2 to prevent link training issues.
$V_{TX-PREEMP-DELTA}$	Delta of Pre-emphasis Level 1 vs. Level 0	2	-	-	dB	Applies to all valid voltage settings. Measured at Pre-emphasis Post Cursor2 Level 0. Support for Pre-emphasis Level 3 is optional.
	Delta of Pre-emphasis Level 2 vs. Level 1	1.6	-	-	dB	
	Delta of Pre-emphasis Level 3 vs. Level 2	1.6	-	-	dB	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-18*

Expected/Observable Results

The measured pre-emphasis level or pre-emphasis delta for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Transition Voltage Range Measurement Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1272001, 1272002, 1272003, 1272004 – Non Transition Voltage Range Measurement (Swing 0)
- 1273001, 1273002, 1273003, 1273004 – Non Transition Voltage Range Measurement (Swing 1)
- 1274001, 1274002, 1274003, 1274004 – Non Transition Voltage Range Measurement (Swing 2)

For Standard DP Pattern (HBR2 and HBR3):

- 1272101, 1272102, 1272103, 1272104 – Non Transition Voltage Range Measurement (Swing 0)
- 1273101, 1273102, 1273103, 1273104 – Non Transition Voltage Range Measurement (Swing 1)
- 1274101, 1274102, 1274103, 1274104 – Non Transition Voltage Range Measurement (Swing 2)

For Arbitrary Pattern:

- 1372101, 1372102, 1372103, 1372104 – Non Transition Voltage Range Measurement (Swing 0)
- 1373101, 1373102, 1373103, 1373104 – Non Transition Voltage Range Measurement (Swing 1)
- 1374101, 1374102, 1374103, 1374104 – Non Transition Voltage Range Measurement (Swing 2)

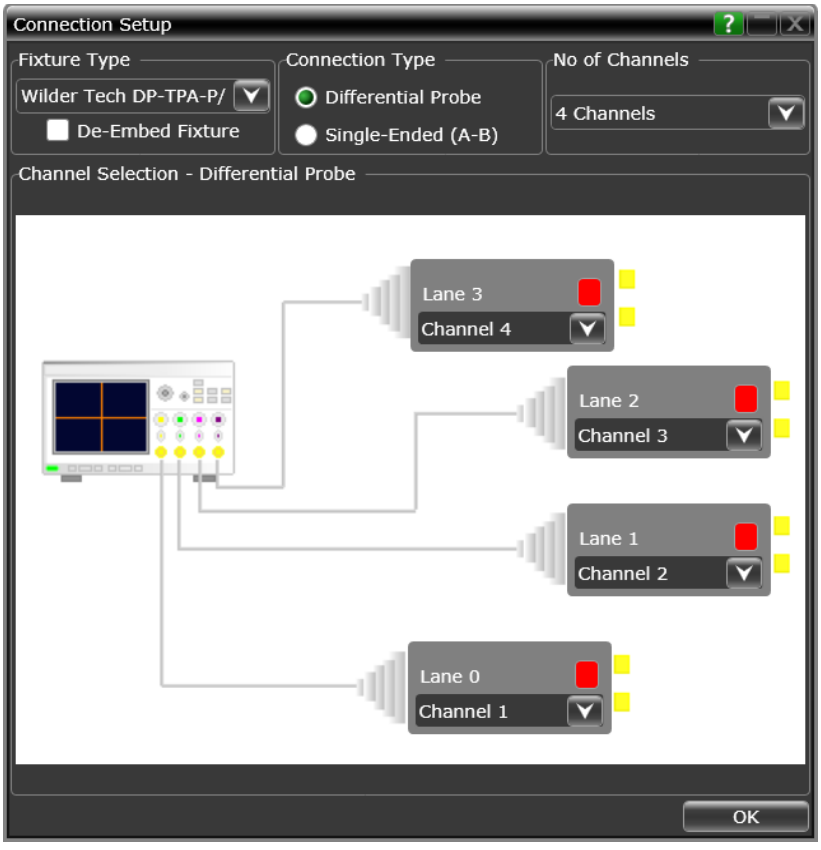
Test Overview

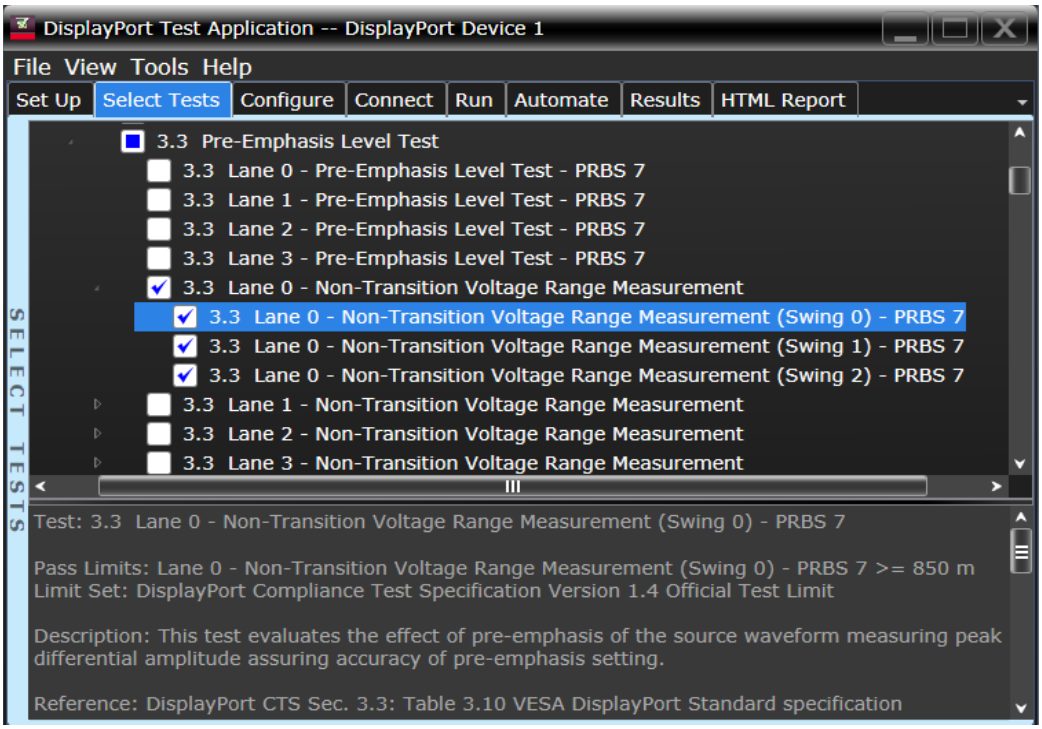
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings. Comparisons are also made for the Level 0 transition state as well as non-transition levels.

Test Conditions for Non-Transition Voltage Range Measurement Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.4 Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR3 – PLTPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given Voltage Level, repeat the following steps for all pre-emphasis levels subjected to constraints specified in Table 3-1 of the VESA DisplayPort 1.4 Standard:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.

- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6th bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4th bit of the four successive transmitted zeros of the pattern.

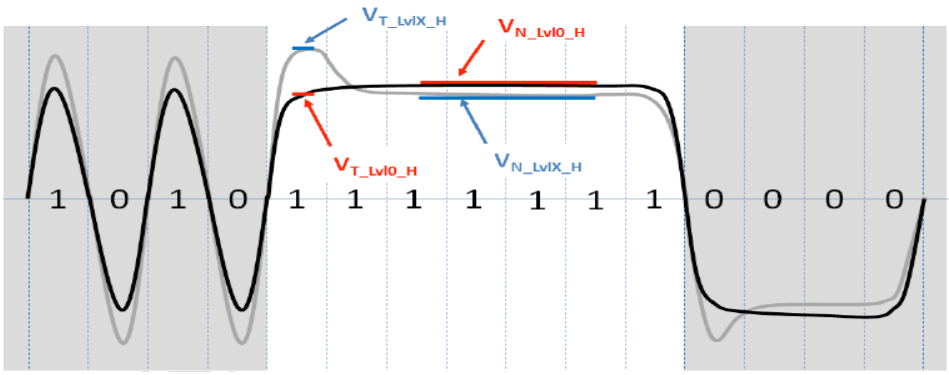


Figure 104 High Voltage measurement for RBR and HBR

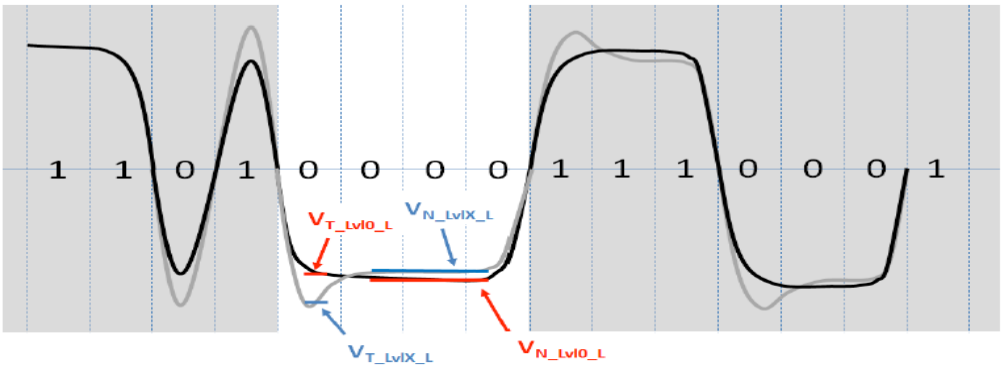


Figure 105 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR3 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

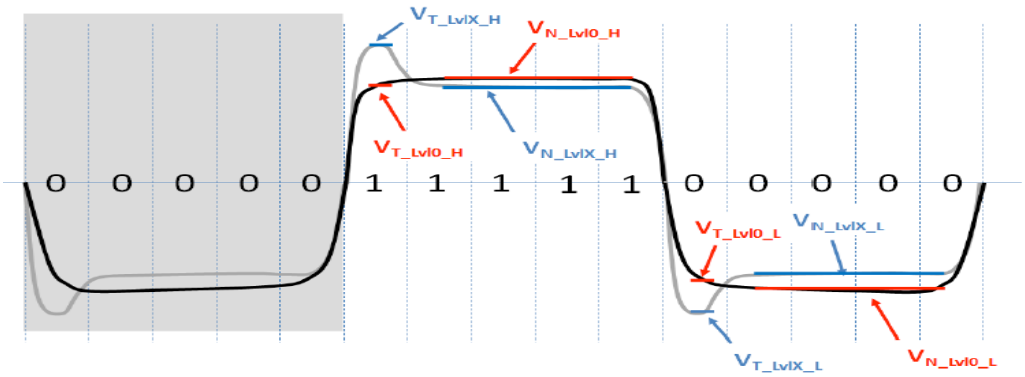


Figure 106 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

2 Calculate the non transition voltage range using the equation:

$$\text{Non Transition Voltage Range} = \text{Minimum } [(V_{N\_LvlX\_PP}) / (V_{N\_Lvl0\_PP})]$$

where, $V_{N\_LvlX\_PP}$) refers to all supported pre-emphasis levels (Level1, Level2, Level3 and so on up to Level X).

3 Report the measurement results.

PASS Condition

Non-Transition Voltage Range Measurements

For Level 2 voltage setting: Resultant > 0.708 OR 20*log(Resultant) > -3dB

For Level 1 voltage setting: Resultant > 0.708 OR 20*log(Resultant) > -3dB

For Level 0 voltage setting: Resultant > 0.85 OR 20*log(Resultant) > -1.4dB

Table 109 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX-DIFF\_REDUCTION}$	Non-transition reduction Output Voltage Level 2	-	-	3	dB	$V_{TX-DIFF}$ at each non-zero nominal pre-emphasis level must not be lower than the specified amount less than $V_{TX-DIFF}$ at the zero nominal pre-emphasis level.
	Non-transition reduction Output Voltage Level 1	-	-	3	dB	
	Non-transition reduction Output Voltage Level 0	-	-	1.4	dB	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-18*

Expected/Observable Results

The measured output voltage level reduction of the non transition bit for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Peak to Peak Voltage Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1266001, 1266002, 1266003, 1266004 – Peak to Peak Voltage Test

For Standard DP Pattern (HBR2 and HBR3):

- 1266101, 1266102, 1266103, 1266104 – Peak to Peak Voltage Test

For Arbitrary Pattern:

- 1366101, 1366102, 1366103, 1366104 – Peak to Peak Voltage Test

Test Overview

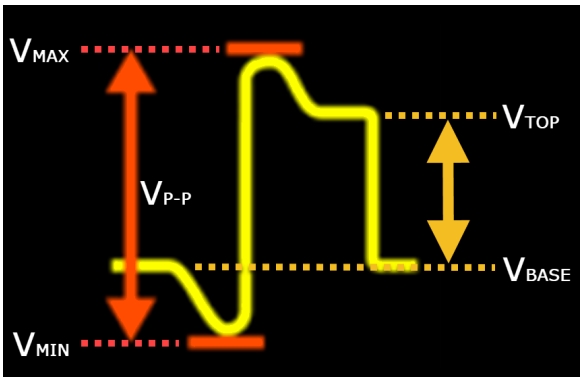
The objective of this test is to evaluate the maximum differential peak to peak voltage.

NOTE

The peak to peak voltage (V_{P-P}) formula is:

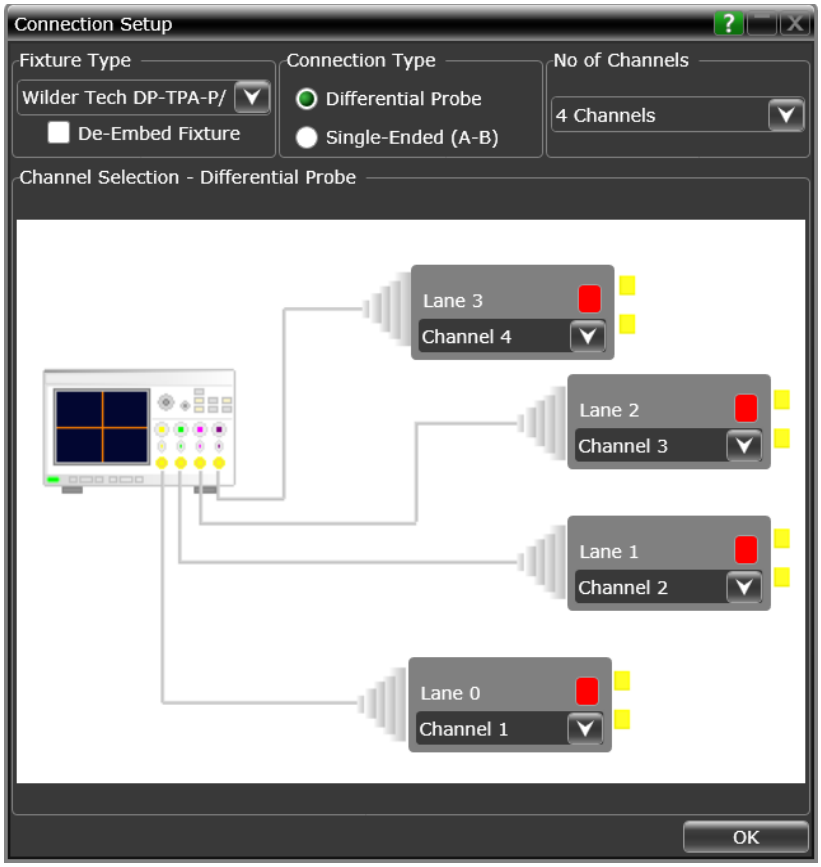
$$V_{P-P} = V_{MAX} - V_{MIN}$$

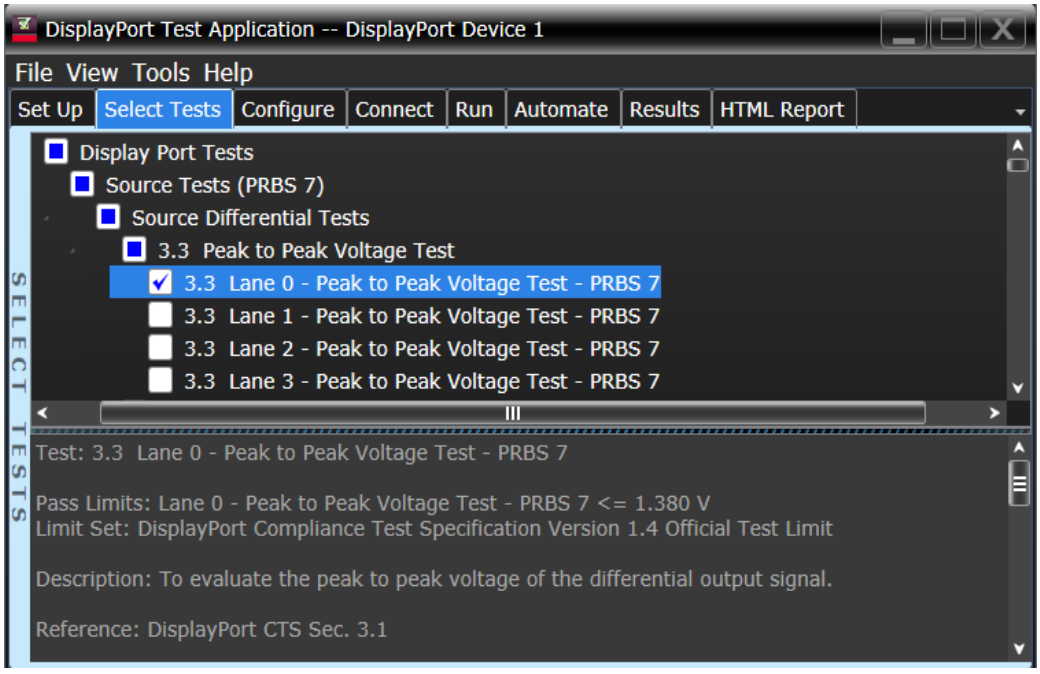
Please see the figure below for more info.



Test Conditions for Peak to Peak Voltage Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.4 Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR3 – PLTPAT


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
Display Port Tests
Source Tests (PRBS 7)
Source Differential Tests
3.3 Peak to Peak Voltage Test
3.3 Lane 0 - Peak to Peak Voltage Test - PRBS 7
3.3 Lane 1 - Peak to Peak Voltage Test - PRBS 7
3.3 Lane 2 - Peak to Peak Voltage Test - PRBS 7
3.3 Lane 3 - Peak to Peak Voltage Test - PRBS 7
SELECT TESTS
Test: 3.3 Lane 0 - Peak to Peak Voltage Test - PRBS 7
Pass Limits: Lane 0 - Peak to Peak Voltage Test - PRBS 7 <= 1.380 V
Limit Set: DisplayPort Compliance Test Specification Version 1.4 Official Test Limit
Description: To evaluate the peak to peak voltage of the differential output signal.
Reference: DisplayPort CTS Sec. 3.1

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{MAX} and V_{MIN} of the input signal.
   d Measure the data rate of the input signal.
3 Measure the maximum and minimum voltage of the input signal.
4 Calculate the peak to peak voltage using the equation:

$$\text{Peak to Peak Voltage} = V_{MAX} - V_{MIN}$$

5 Report the measurement results.

PASS Condition

For all Data Rates:

Maximum Differential Peak to Peak Voltage $\leq$ 1.38V.

Table 110 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX\text{-}DIFFp\text{-}p\_MAX}$	Max Output Voltage Level	-	-	1.38	V	For all Output Level and Pre-emphasis combinations.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-18*

Expected/Observable Results

The measured peak to peak voltage for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Inter-Pair Skew Test

Test ID

For Standard DP Pattern:

- 1290001 – Lane0/Lane1 Inter-Pair Skew Test
- 1290002 – Lane0/Lane2 Inter-Pair Skew Test
- 1290003 – Lane0/Lane3 Inter-Pair Skew Test
- 1290004 – Lane1/Lane2 Inter-Pair Skew Test
- 1290005 – Lane1/Lane3 Inter-Pair Skew Test
- 1290006 – Lane2/Lane3 Inter-Pair Skew Test

For Arbitrary Pattern:

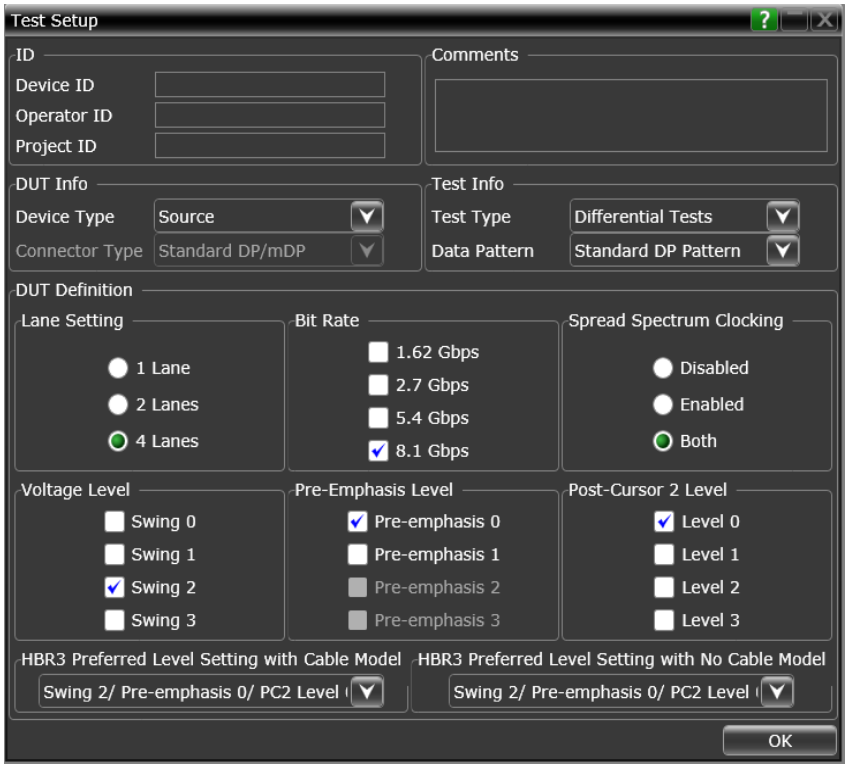
- Not applicable for arbitrary pattern

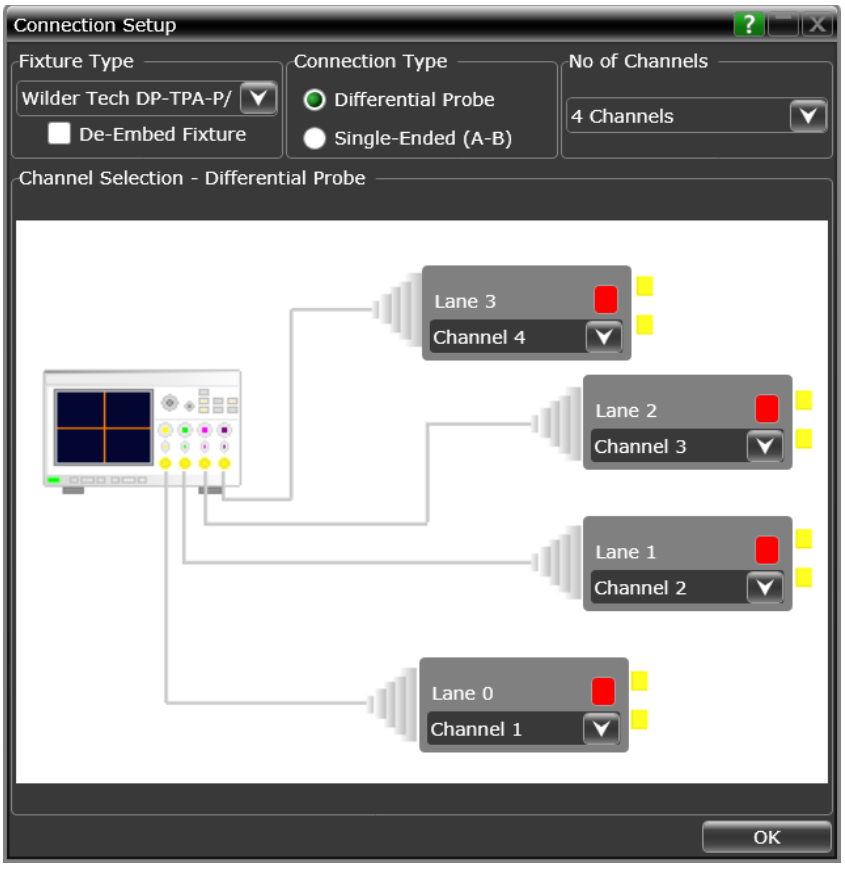
Test Overview

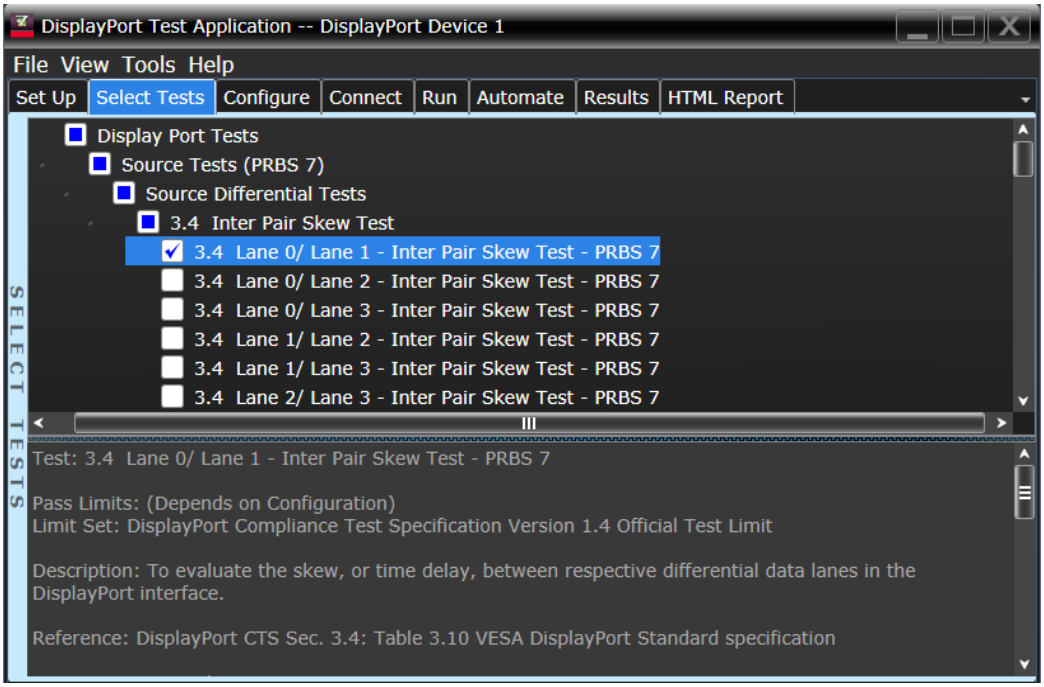
The objective of the test is to evaluate the skew or time delay between differential data lanes in the DisplayPort interface.

Test Conditions for Inter Pair Skew Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest Bit Rate supported (RBR, HBR, HBR2 or HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported For two lane operation: Lane 0 to Lane 1 For four lane operation: Lane 0 to Lane 1 Lane 0 to Lane 2 Lane 0 to Lane 3 Lane 1 to Lane 2 Lane 1 to Lane 3 Lane 2 to Lane 3
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given inter-pair skew measurement of Lane A to Lane B:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the Lane A input signal.

ii Scale the vertical display of the Lane A input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the Lane A input signal.

iv Verify the trigger and the amplitude of the Lane B input signal.

v Scale the vertical display of the Lane B input signal to optimum value.

vi Measure V_{TOP} and V_{BASE} of the Lane B input signal.

vii Measure the data rate of the Lane A input signal.

viii Measure the data rate of the Lane B input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

d Set up the parameter for the inter-pair skew measurement:

i Set up two display grids such that each grid displays one test lane data signal.

ii Set up the measurement threshold for each test lane data signal on the Transition Voltage = 0V.

iii Decode the data signal for each test lane.

iv Search the desired pattern from the decoded data signal.

v Measure the time difference between the corresponding edges of both test lanes:

$T_{Transition\_LaneA} - T_{Transition\_LaneB}$

vi Repeat the previous step until you measure 100 edges.

vii VESA DisplayPort 1.4 Standard specifies 20 UI offset Lane 0 to Lane 1, Lane 1 to Lane 2 and Lane 2 to Lane 3. The resultant offset is cumulative.

viii Calculate the inter-pair skew using the equation:

$$\text{Inter-Pair Skew} = \{1/\text{Number of Edges}\} \sum |T_{Transition\_LaneA} - T_{Transition\_LaneB}| - \text{Nominal Skew}$$

where, Nominal Skew is the expected offset between tested lanes.

2 Report the measurement results.

PASS Condition

-1250ps < Inter-Lane Skew Tolerance < 1250ps

Table 111 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$t_{TX-SKEW-INTER\_PAIR}$	Lane-to-Lane Output Skew	-	-	1250	ps	Applies to transmitters capable of 2- and 4-lane operation. Also, applies to all pairwise combinations of supported lanes for all data rates.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.4*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-18*

Expected/Observable Results

The measured inter-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Main Link Frequency Compliance Test

Test ID

For Standard DP Pattern:

- 12193001 12193002 12193003 12193004 – Main Link Frequency Compliance

For Arbitrary Pattern:

- 13193001 13193002 13193003 13193004 – Main Link Frequency Compliance

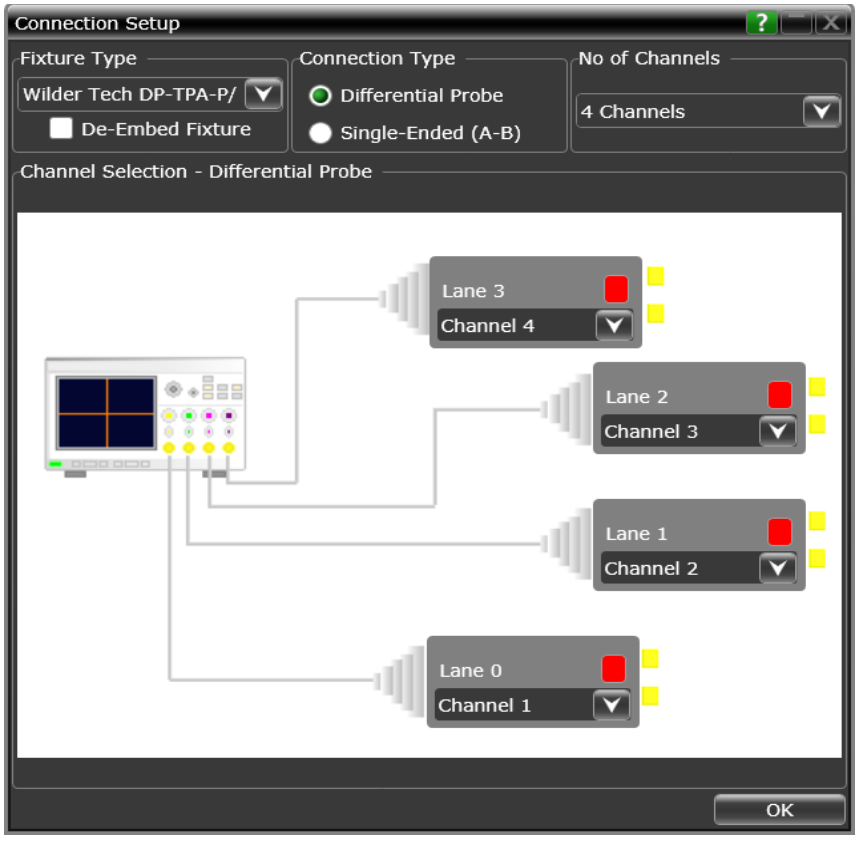
Test Overview

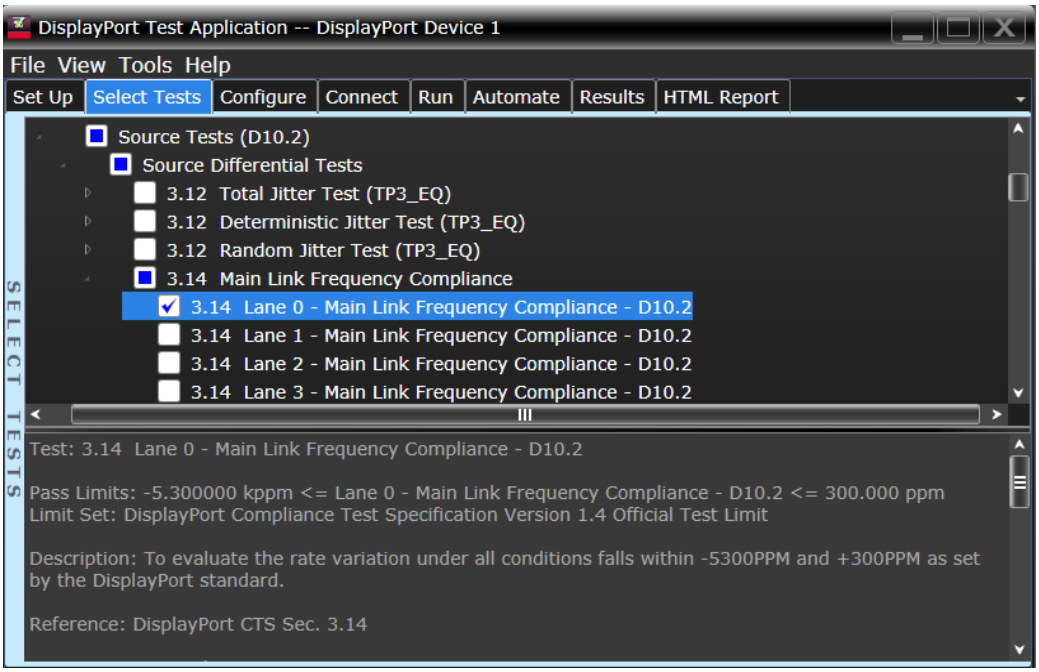
The objective of this test is to ensure that the average data rate under all conditions does not exceed the minimum and maximum values as set by the VESA DisplayPort 1.4 Standard.

Test Conditions for Main Link Frequency Compliance Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.

5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and the minimum measurement levels for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurement levels for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e For SSC Enabled Test condition, check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.
9 For the test condition “SSC Enabled”, set up the parameter of the SSC measurement:
   a Set up the memory depth and time-base to display one complete SSC cycle based on the measured SSC modulation frequency in Step 5.
   b Acquire the signal with one complete SSC cycle.
   c Get the minimum of FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

      Maximum Data Rate = 1 / (Minimum Unit Interval)

   d Get the maximum of FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

      Minimum Data Rate = 1 / (Maximum Unit Interval)

   e Repeat steps b, c and d until you acquire 10 SSC Cycles.
   f Calculate the mean value for the maximum and minimum data rates.
10 Report the measurement results.

PASS Condition

Maximum Data Rate (Frequency Max_{ppm}) $\leq$ 300 ppm

Minimum Data Rate (Frequency Min_{ppm}) $\geq$ -5300 ppm

Table 112 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
f_{HBR3}	Frequency for High Bit Rate 3	8.05707	8.1	8.10243	Gbps	
f_{HBR2}	Frequency for High Bit Rate 2	5.37138	5.4	5.40162	Gbps	Frequency high limit = +300ppm Frequency low limit = -5300ppm
f_{HBR}	Frequency for High Bit Rate	2.68569	2.7	2.70081	Gbps	
f_{RBR}	Frequency for Reduced Bit Rate	1.611414	1.62	1.620486	Gbps	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.14*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-17*

Expected/Observable Results

The measured data rate for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Frequency Test

Test ID

For Standard DP Pattern:

- 12170001 12170002 12170003 12170004 – SSC Modulation Frequency Test

For Arbitrary Pattern:

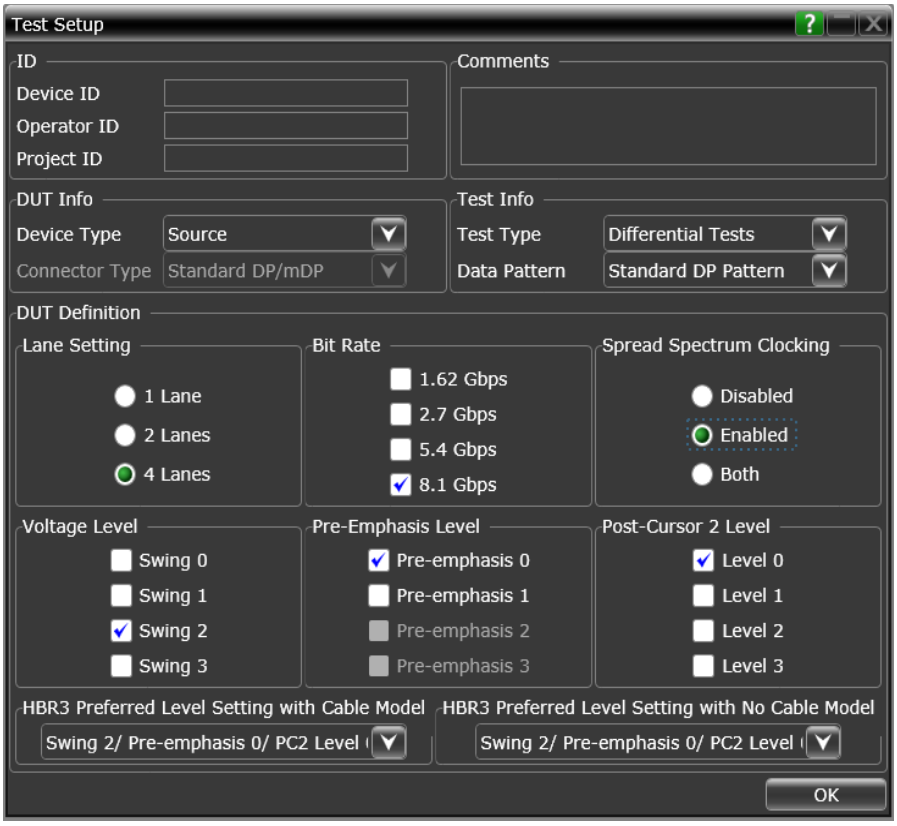
- 13170001 13170002 13170003 13170004 – SSC Modulation Frequency Test

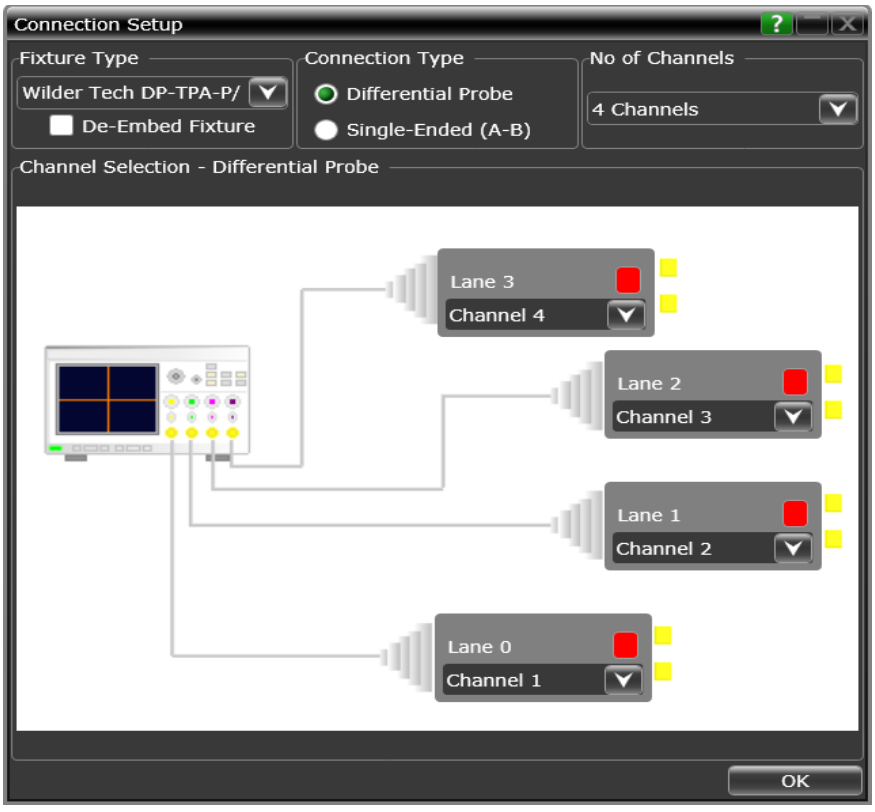
Test Overview

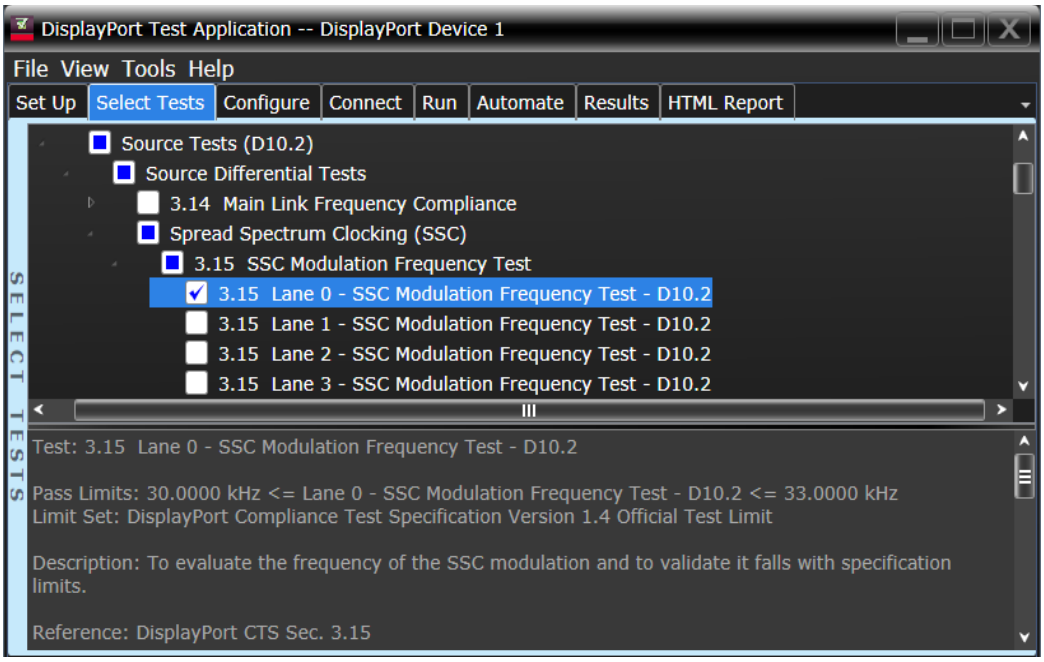
The objective of this test is to evaluate the frequency of the SSC modulation and to validate that the frequency is within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. Calculate the SSC modulation frequency from the average of the measured SSC modulation frequency for each cycle.

Test Conditions for SSC Modulation Frequency Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR3)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.

5 Set up the parameters for the frequency measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.
   g Acquire the signal for 10 SSC Cycles.
6 Get the mean value for the SSC Modulation frequency.
7 Report the measurement results.

PASS Condition

30kHz $\leq$ SSC Modulation Frequency (f_{SSC}) $\leq$ 33kHz

Table 113 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
Down_Spread_Frequency	Link clock down-spreading frequency	30	-	33	kHz	Range: 30kHz ~ 33kHz when down-spread enabled

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.15*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-17*

Expected/Observable Results

The measured SSC modulation frequency for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Deviation Test

Test ID

For Standard DP Pattern:

- 12180001 12180002 12180003 12180004 – SSC Modulation Deviation Test

For Arbitrary Pattern:

- 13180001 13180002 13180003 13180004 – SSC Modulation Deviation Test

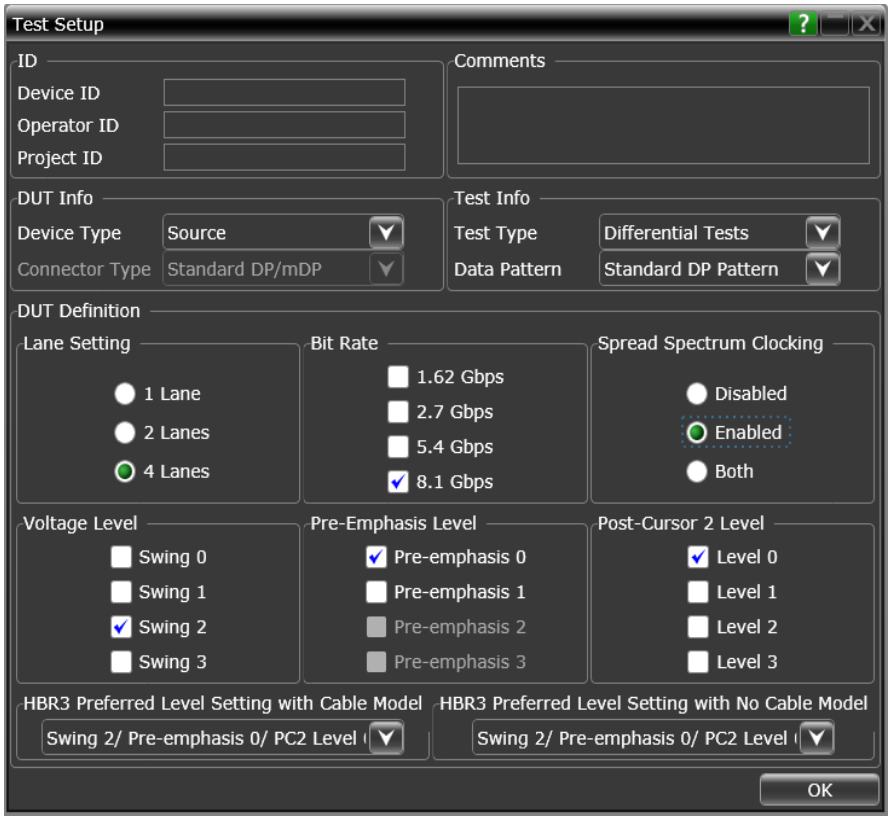
Test Overview

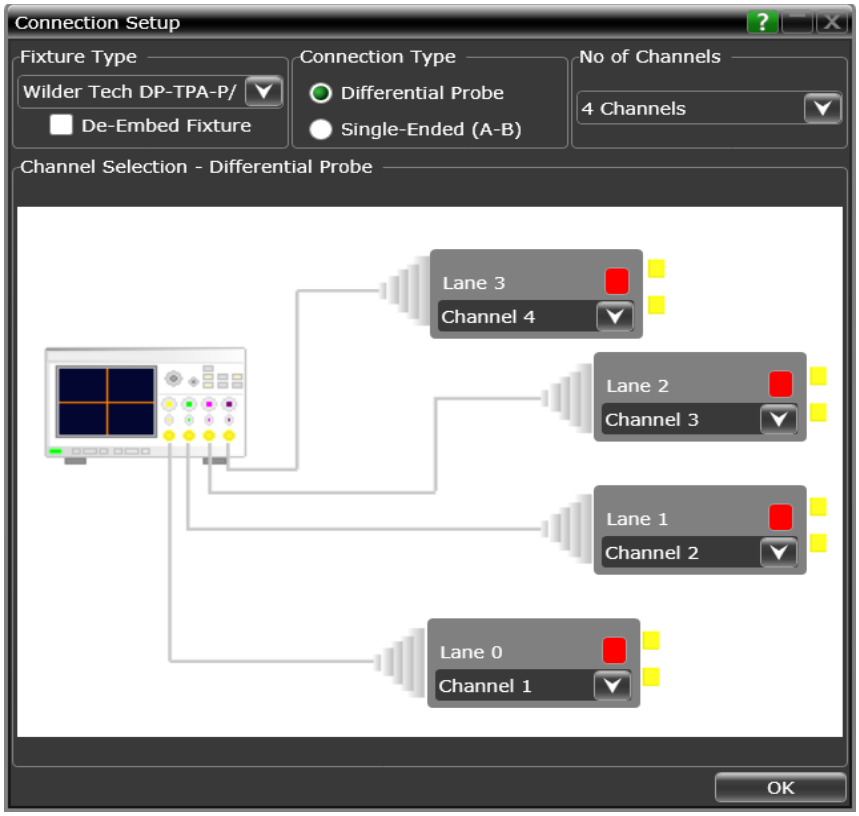
The objective of this test is to evaluate the range of SSC down-spreading of the transmitter signal in ppm and to validate that the values are within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. For each cycle, the minimum and maximum data rate is evaluated. Calculate the SSC modulation deviation from the average of the maximum minus the average of the minimum using the equation:

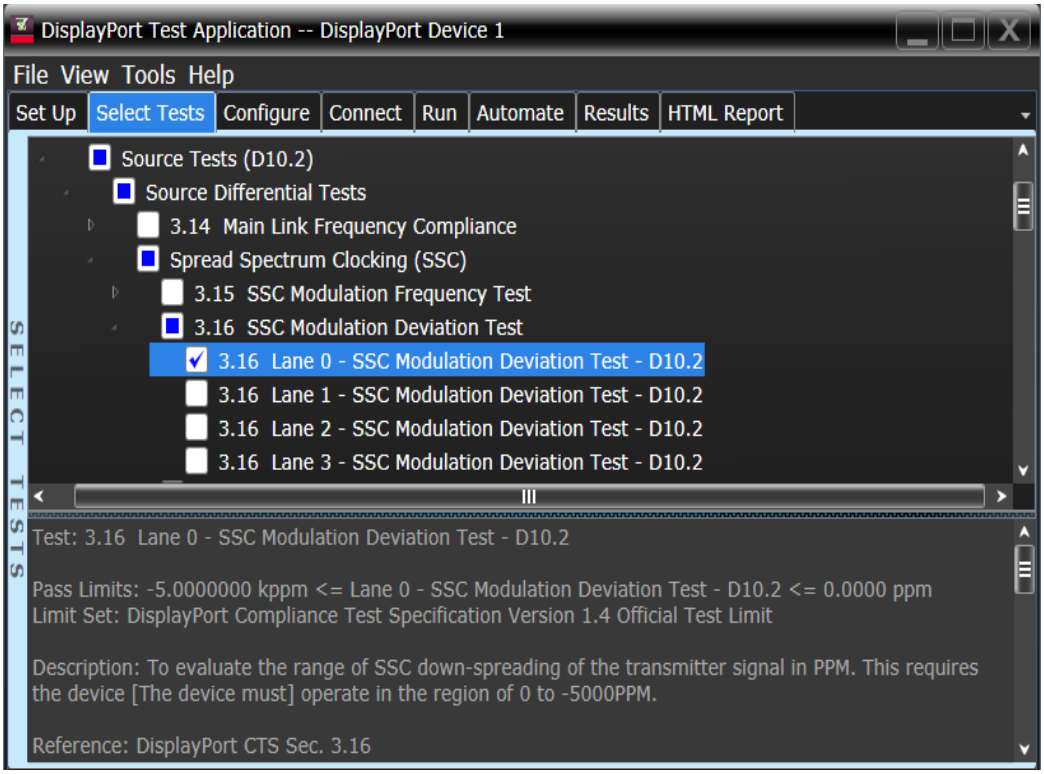
SSC Modulation Deviation = {[Average (Minimum Data Rate) - Average (Maximum Data Rate)] / Nominal Data Rate}*1E+6

Test Conditions for SSC Modulation Deviation Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR3)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.

5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and minimum measurements for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurements for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e Check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point for three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 filtered unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurements for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.
9 Set up the parameters for SSC measurement.
   a Set up memory depth and time-base to display one complete SSC Cycle based on the measured SSC modulation frequency in step 5.
   b Acquire the signal with one complete SSC Cycle.
   c Get the minimum of the FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

      Maximum Data Rate = 1/Minimum Unit Interval

   d Get the maximum of the FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

      Minimum Data Rate = 1/Maximum Unit Interval

   e Repeat step b,c and d until you acquire 10 SSC Cycles.
   f Calculate the mean value for the maximum and minimum data rate.
10 Calculate the SSC Modulation Deviation using the equation:

   SSC Modulation Deviation = {[Average (Minimum Data Rate) - Average (Maximum Data Rate)] / Nominal Data Rate}*1E+6

11 Report the measurement results.

PASS Condition

-5000ppm $\leq$ SSC Modulation Deviation (Resultant$_{SSC\ Range}$) $\leq$ 0ppm

Table 114 DisplayPort Main Link Transmitter System Parameters

Symbol	Parameter	Min	Nom	Max	Unit	Comments
Down_Spread_Amplitude	Link clock down-spreading	0	-	0.5	%	Range: 0% ~ 0.5% when down-spread enabled

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.16*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-17*

Expected/Observable Results

The measured SSC modulation deviation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Deviation HF Variation Test (Informative)

Test ID

For Standard DP Pattern:

- 12200001 12200002 12200003 12200004 – SSC Deviation HF Variation Test (Informative)

For Arbitrary Pattern:

- 13200001 13200002 13200003 13200004 – SSC Deviation HF Variation Test (Informative)

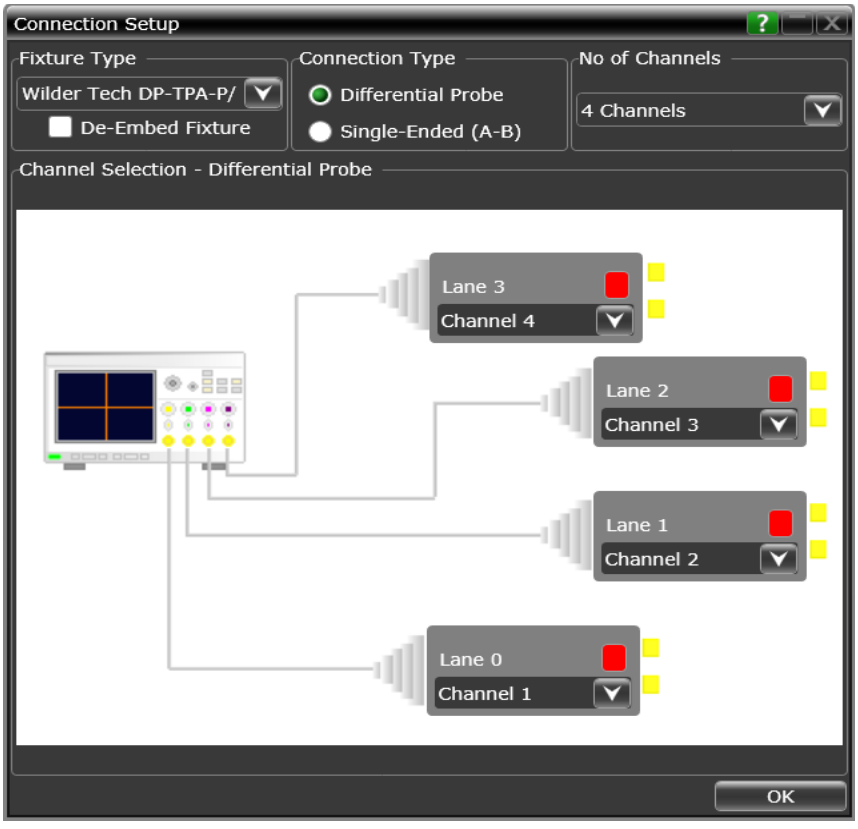
Test Overview

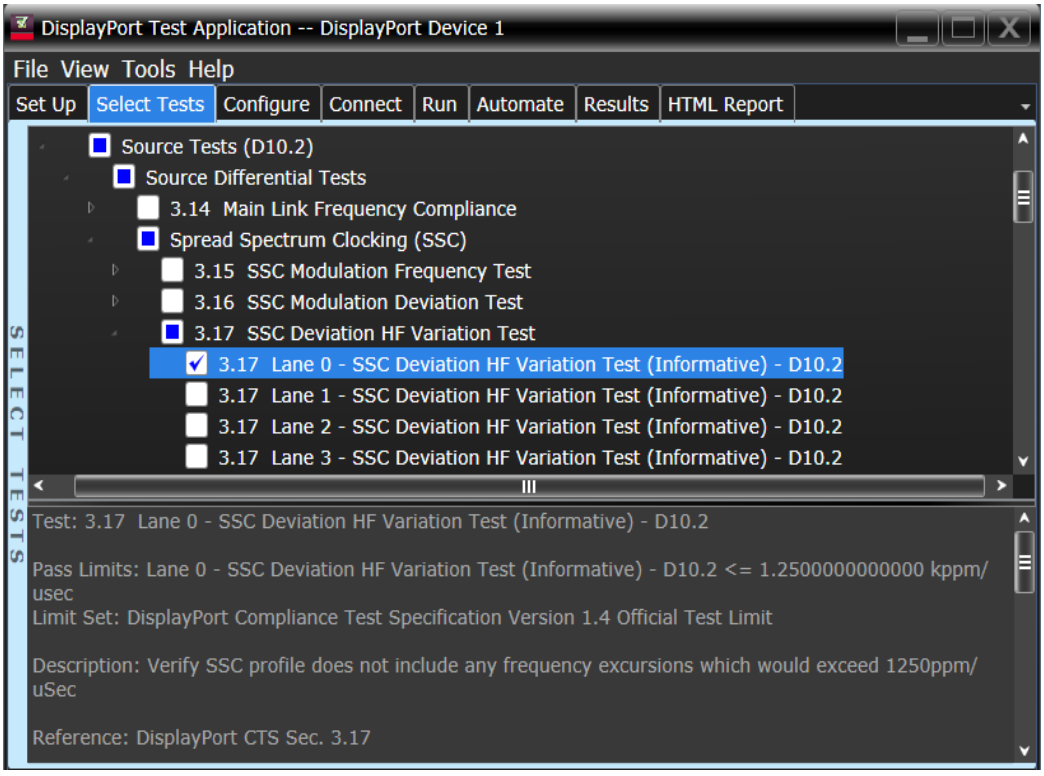
The objective of this test is to verify that the SSC profile does not include any frequency deviation that may exceed 1250 ppm/µsec. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles.

Test Conditions for SSC Deviation HF Variation Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR3)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.

5 Set up the parameters for the frequency measurement.

a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.

b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.

c Set up the memory depth and time-base using the settings defined in the Configuration Variable.

d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.

e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).

f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.

6 Set up the parameters for the SSC measurement.

a Set up memory depth and time-base to display one complete SSC cycle using the measured SSC Modulation Frequency in Step 5.

b Acquire the signal with one complete SSC Cycles.

c Read the FUNC2 filtered unit interval measurement trend.

d Compute the slope using the “Sliding Window” with 1.00 µsec window width. Calculate the slope using the equation:

$$\text{Slope} = [f(t) - f(t\text{-}1.00\ \mu\text{sec})/1.00\ \mu\text{sec}$$

e Repeat step b, c and d until you acquire 10 SSC Cycles.

f Get the maximum value for the computed value of slope.

7 Report the measurement results.

PASS Condition

SSC_t dF/dt $\leq$ 1250ppm/µsec

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.17*

Expected/Observable Results

The measured SSC deviation high frequency variation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Eye Diagram Test (TP3_EQ)

Test ID

For Standard DP Pattern (HBR):

- 1211001, 1211002, 1211003, 1211004 – Eye Diagram Test (TP3_EQ) - PRBS7
- 1211011, 1211012, 1211013, 1211014 – Eye Diagram Test with No Cable Model (TP3_EQ) - PRBS7

For Standard DP Pattern (HBR2):

- 1215001, 1215002, 1215003, 1215004 – Eye Diagram Test (TP3_EQ) - HBR2CPAT
- 1215011, 1215012, 1215013, 1215014 – Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT

For Arbitrary Pattern:

- 1315001, 1315002, 1315003, 1315004 – Eye Diagram Test (TP3_EQ)
- 1315011, 1315012, 1315013, 1315014 – Eye Diagram Test with No Cable Model (TP3_EQ)

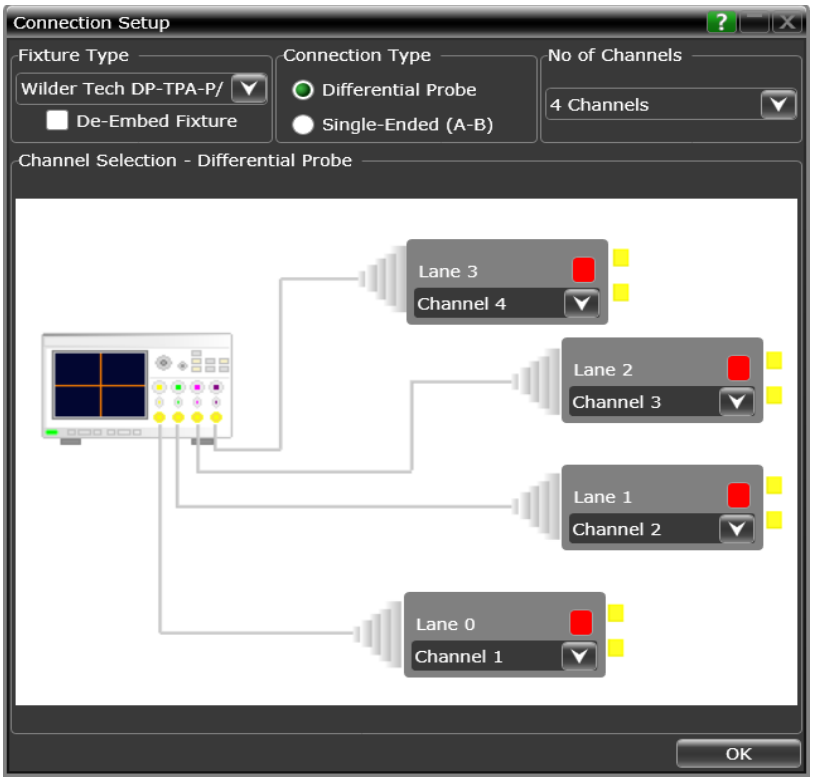
Test Overview

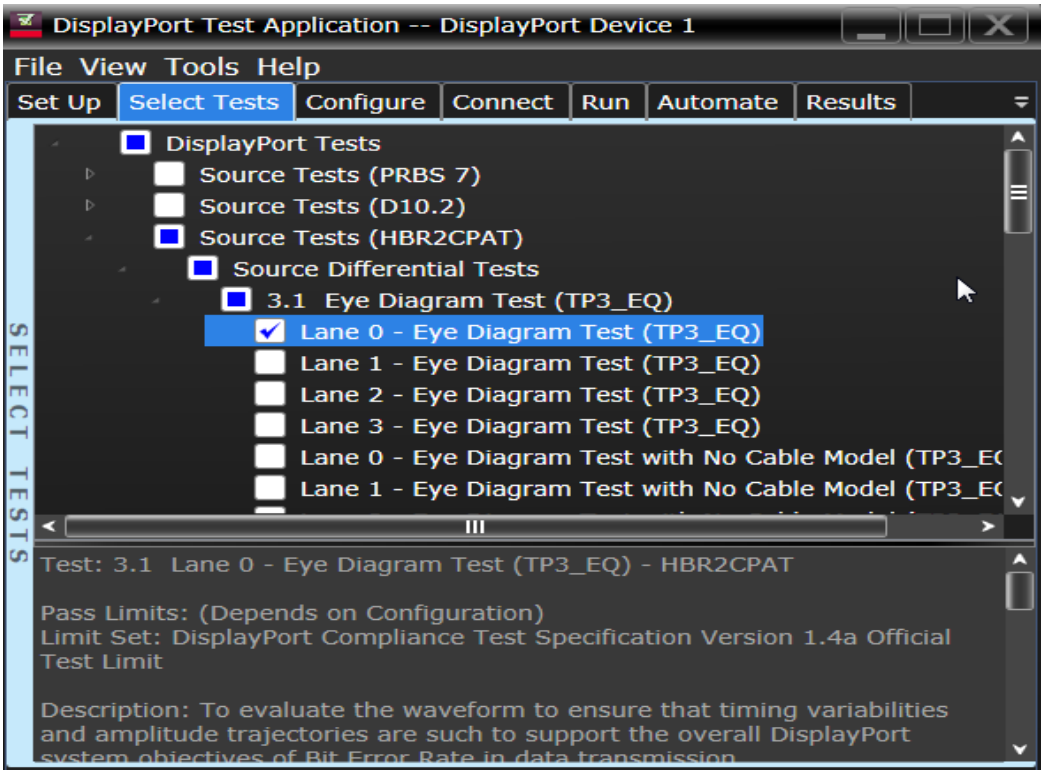
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions for Eye Diagram Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR (Informative) and HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	HBR – Level 2 HBR2 – Any Voltage Level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	HBR – Level 0 HBR2 – Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	HBR – Level 0 HBR2 – Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	HBR – PRBS7 HBR2 – HBR2CPAT
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure for HBR

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.

7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the jitter of the eye diagram using the Histogram.
9 Check for any signal trajectories that may have entered into the mask.
10 Report the measurement results.

Measurement Procedure for HBR2

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]:
   a Pattern fold the equalized signal based on the High Level Voltage (V_{HIGH}) random noise configuration variable.
   b Set up the vertical waveform histogram on the equalized signal to measure random noise of High Level Voltage (V_{HIGH}).
   c Measure the High Level Voltage (V_{HIGH}) random noise based on the standard deviation of the waveform histogram.
   d Pattern fold the equalized signal based on the Low Level Voltage (V_{LOW}) random noise configuration variable.
   e Set up the vertical waveform histogram on the equalized signal to measure the random noise of Low Level Voltage (V_{LOW}).
   f Measure the Low Level Voltage (V_{LOW}) random noise based on the standard deviation of the waveform histogram.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge and right edge.
8 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.

9 Find the maximum eye height location of the eye diagram.

10 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:

a Set up the parameter of the jitter separation using the EZJIT Plus/Complete Software.

i Load the jitter separation parameter into EZJIT Plus/Complete Software based on the settings in the Configuration Variable.

ii Acquire the signal until 1,000,000 edges are analyzed.

b Note the value of the jitter component from the EZJIT Plus/Complete Software.

11 Create the eye mask based on the following criteria:

a If you select more than one lane (2 lanes or 4 lanes DUT configuration), the eye mask height and width is derate in the following manner, to include crosstalk as defined in DisplayPort 1.4 Compliance Test Specification:

i Eye Mask Width Derate (Crosstalk) = 0.04 UI

ii Eye Mask Height Derate (Crosstalk) = 0.014V

b If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]: eye mask height and width is derate as below to comprehend the noise/jitter extrapolated to BER 10^{-9} for an Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI:

i Calculate the Eye Mask Width Derate (Random Jitter) using the equation:

$$\text{Eye Mask Width Derate (Random Jitter)} = 2.5 * \text{Random Jitter}_{rms}$$

ii Calculate the Eye Mask Height Derate (Random Noise) using the equation:

$$V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{HIGH}\ \text{Random Noise}_{rms}$$

$$V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{LOW}\ \text{Random Noise}_{rms}$$

NOTE The factor 2.5 is the delta between BER 10^{-6} (9.507) and 10^{-9} (11.996) to comprehend the noise/jitter extrapolated to BER 10-9 as the Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI.

BER	N
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996

c Place the eye mask height at the point of the maximum eye height found in Step 9.

d Calculate the Eye Mask Width:

$$\text{Eye Mask Width} = \text{Eye Width Specification (0.38 UI)} + \text{Eye Mask Width Derate (Crosstalk)} + 2 * \text{Eye Mask Width Derate (Random Jitter)}$$

e Calculate the Eye Mask Height:

$$\text{Eye Mask Height} = \{\text{Eye Height Specification (0.09 V)} + \text{Eye Mask Height Derate (Crosstalk)}\}/2 + V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)}$$

$$\text{Eye Mask Height} = -\{\text{Eye Height Specification (0.09 V)} + \text{Eye Mask Height Derate (Crosstalk)}\}/2 - V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)}$$

12 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram.
   c Run the eye mask until 1,000,000 UI are folded.
13 Measure the eye height of the eye diagram using the Histogram.
14 Measure the jitter of the eye diagram using the Histogram.
15 Calculate the eye width based on the measured jitter of the eye diagram.
16 Check for any signal trajectories that may have entered into the mask.
17 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 115 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 115 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

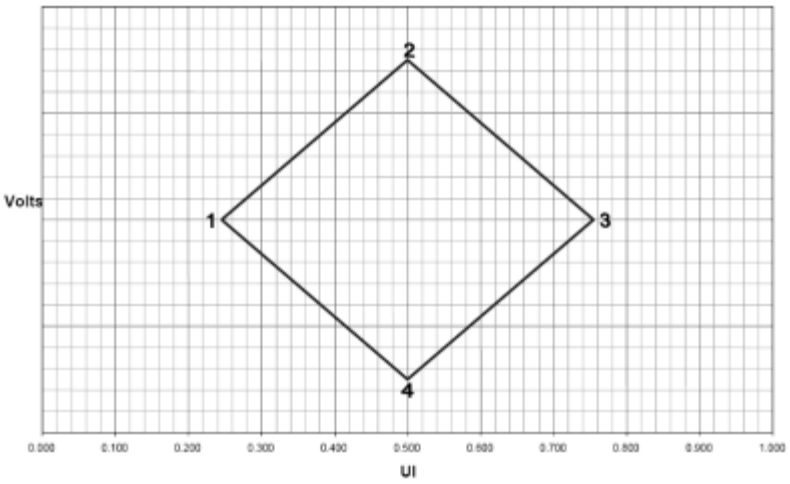


Figure 107 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 116 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.045*
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.045*

NOTE

*Eye height limit of 45 mV and -45 mV assumes cross-talk as 0, which is only possible in case of single lane testing.

In case of multi-lane testing, cross talk exists, and the eye height values deviate by ± 7 mV. Thus the eye height becomes (+45 +7) mV and (-45 -7) mV or +52 mV and -52 mV.

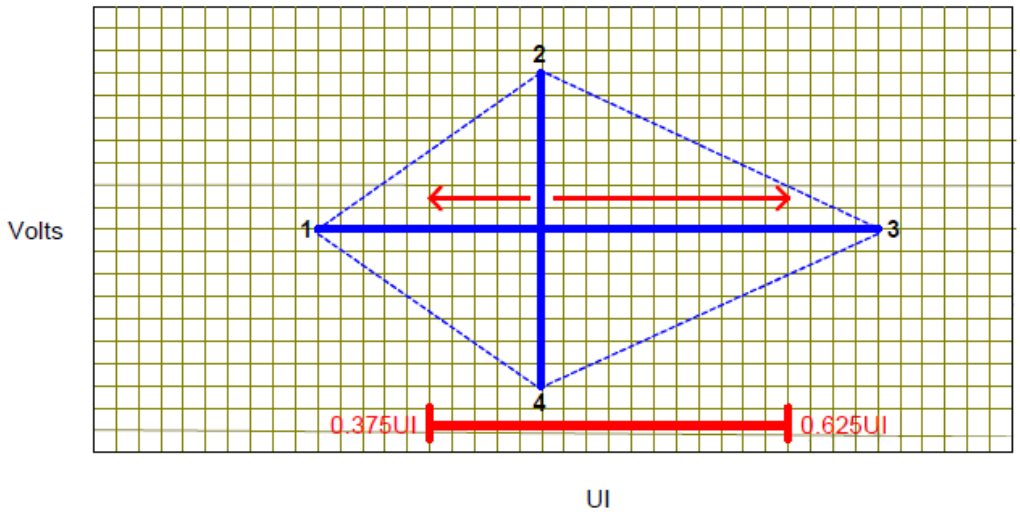


Figure 108 The Eye Mask at TP3_EQ (HBR2)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2.8.1 for HBR2, section 3.5.2.8.2 for HBR, Table 3-29 for HBR, and Table 3-25 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Eye Diagram Test (TP3_DFE)

Test ID

For Standard DP Pattern (HBR3):

- 1217001, 1217002, 1217003, 1217004 – Eye Diagram Test (TP3_DFE)
- 1217011, 1217012, 1217013, 1217014 – Eye Diagram Test with No Cable Model (TP3_DFE)

For Arbitrary Pattern:

- 1317001, 1317002, 1317003, 1317004 – Eye Diagram Test (TP3_DFE)
- 1317011, 1317012, 1317013, 1317014 – Eye Diagram Test with No Cable Model (TP3_DFE)

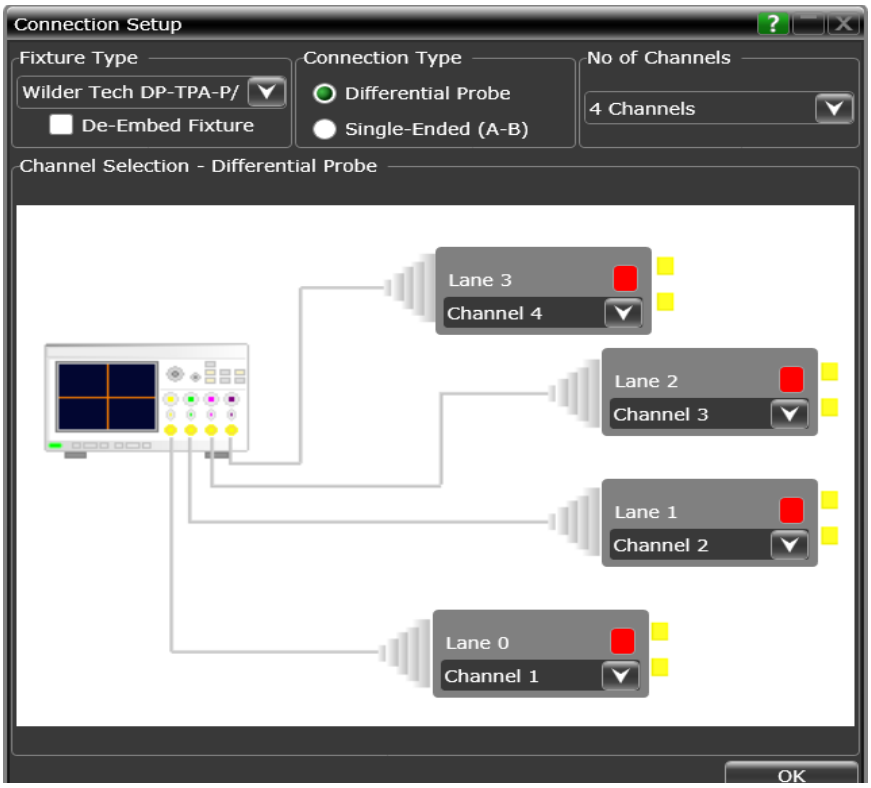
Test Overview

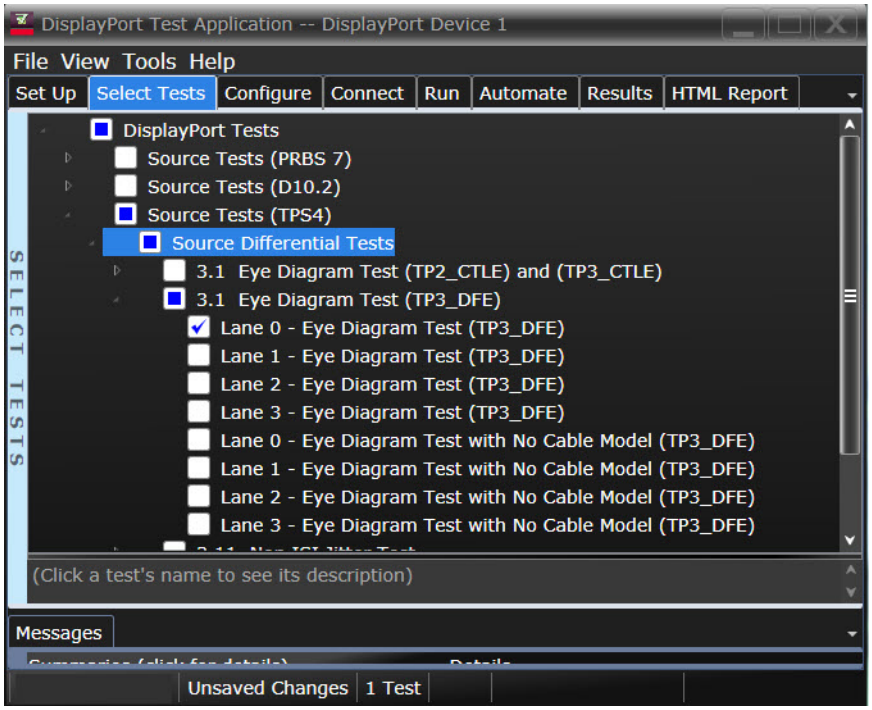
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions for Eye Diagram Test (TP3_DFE)

Test Parameter	Condition
Test Point	TP3_DFE
Bit Rate	HBR3
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any Voltage Level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	TPS4
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 3/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 3/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure for HBR3

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_DFE): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_DFE): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.

5 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:
   a Pattern fold the equalized signal based on the High Level Voltage (V_{HIGH}) random noise configuration variable.
   b Set up the vertical waveform histogram on the equalized signal to measure random noise of High Level Voltage (V_{HIGH}).
   c Measure the High Level Voltage (V_{HIGH}) random noise based on the standard deviation of the waveform histogram.
   d Pattern fold the equalized signal based on the Low Level Voltage (V_{LOW}) random noise configuration variable.
   e Set up the vertical waveform histogram on the equalized signal to measure the random noise of Low Level Voltage (V_{LOW}).
   f Measure the Low Level Voltage (V_{LOW}) random noise based on the standard deviation of the waveform histogram.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left and right edge.
8 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.
9 Find the maximum eye height location of the eye diagram.
10 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:
   a Set up the parameter of the jitter separation using the EZJIT Plus/Complete Software.
      i Load the jitter separation parameter into EZJIT Plus/Complete Software based on the settings in the Configuration Variable.
      ii Acquire the signal until 1,000,000 edges are analyzed.
   b Note the value of the jitter component from the EZJIT Plus/Complete Software.
11 Create the eye mask based on the following criteria:
   a If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]: eye mask height and width is derate as below to comprehend the noise/jitter extrapolated to BER 10-9 for an Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI:
      i Calculate the Eye Mask Width Derate (Random Jitter) using the equation:

      Eye Mask Width Derate (Random Jitter) = 2.5 * Random Jitterrms

      ii Calculate the Eye Mask Height Derate (Random Noise) using the equation:

      VHIGH Eye Mask Height Derate (Random Noise) = 2.5 * V_{HIGH} Random Noiserms

      VLOW Eye Mask Height Derate (Random Noise) = 2.5 * V_{LOW} Random Noiserms

NOTE The factor 2.5 is the delta between BER 10^{-6} (9.507) and 10^{-9} (11.996) to comprehend the noise/jitter extrapolated to BER 10-9 as the Eye Diagram Test (TP3_DFE) only acquiring 1e6 UI.

BER	N
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996

b Place the eye mask height at the point of the maximum eye height found in Step 9.

c Calculate the Eye Mask Width:

Eye Mask Width = Eye Width Specification + 2 * Eye Mask Width Derate (Random Jitter)

d Calculate the Eye Mask Height:

Eye Mask Height = {Eye Height Specification}/2 + V_{HIGH} Eye Mask Height Derate (Random Noise)

Eye Mask Height = -{Eye Height Specification}/2 - V_{LOW} Eye Mask Height Derate (Random Noise)

12 Set up the parameters for the Mask Test.

a Load the eye mask based on the settings in the Configuration Variable.

b Center the eye mask at the middle of the eye diagram.

c Run the eye mask until 1,000,000 UI are folded.

13 Measure the eye hight of the eye diagram using the Histogram.

14 Measure the jitter of the eye diagram using the Histogram.

15 Calculate the eye width based on the measured jitter of the eye diagram.

16 Check for any signal trajectories that may have entered into the mask.

17 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 115 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 117 Eye Diagram Mask Coordinates for TP3_DFE (HBR3)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the eye width is open from x to x + 0.53 UI	0.00000
2	Any passing UI location between 0.375 and 0.625 UI	0.0375
3	Point 1 + 0.35 UI	0.00000
4	Same as point 2	- 0.0375

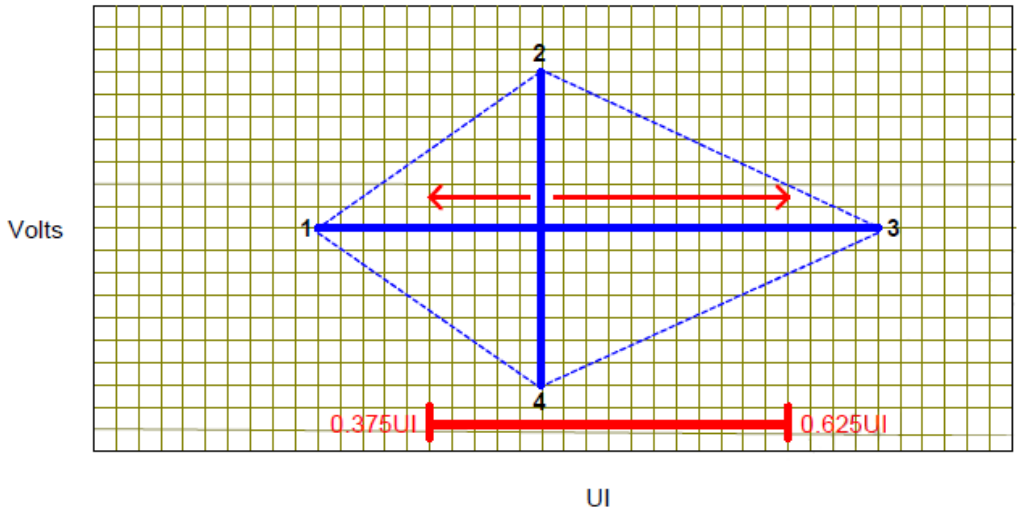


Figure 109 The Eye Mask at TP3_DFE (HBR3)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*

Expected/Observable Results

The measured eye diagram for the test signal at TP3_DFE shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test (TP3_EQ)

Test ID

For Standard DP Pattern:

- 1225001, 1225002, 1225003, 1225004 – Total Jitter Test (TP3_EQ) - PRBS 7
- 1225011, 1225012, 1225013, 1225014 – Total Jitter Test with No Cable Model (TP3_EQ) - PRBS 7
- 1222001, 1222002, 1222003, 1222004 – Total Jitter Test (TP3_EQ) - HBR2CPAT
- 1222011, 1222012, 1222013, 1222014 – Total Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1221001, 1221002, 1221003, 1221004 – Total Jitter Test (TP3_EQ) - D10.2
- 1221011, 1221012, 1221013, 1221014 – Total Jitter Test with No Cable Model (TP3_EQ) - D10.2

For Arbitrary Pattern:

- 1322001, 1322002, 1322003, 1322004 – Total Jitter Test (TP3_EQ)
- 1322011, 1322012, 1322013, 1322014 – Total Jitter Test with No Cable Model (TP3_EQ)

Test Overview

The objective of this test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

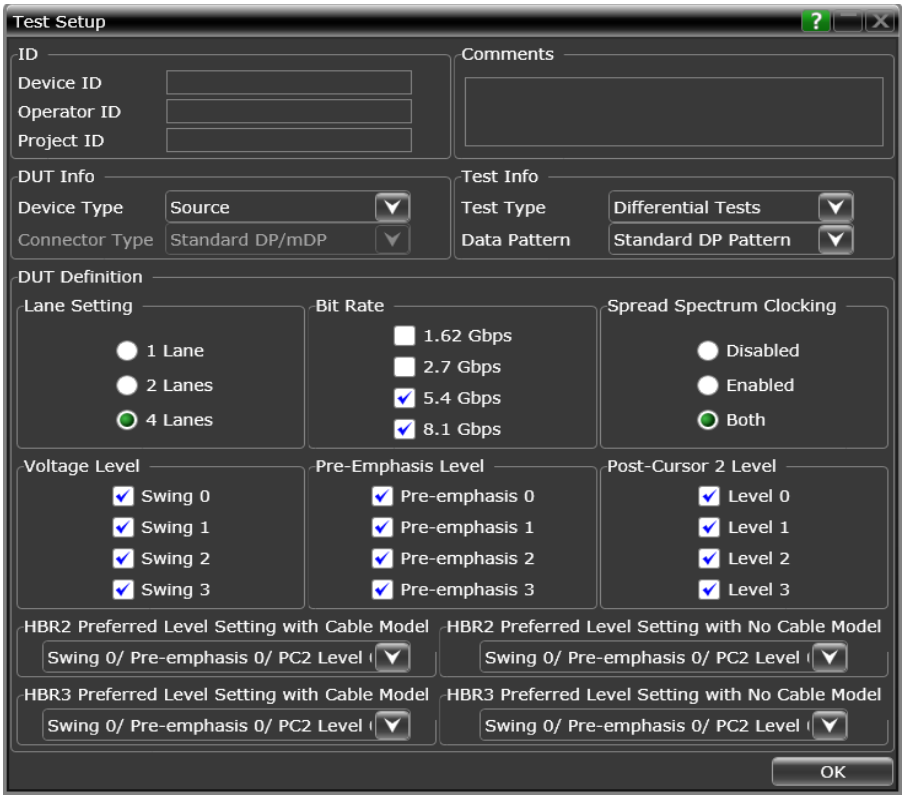
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

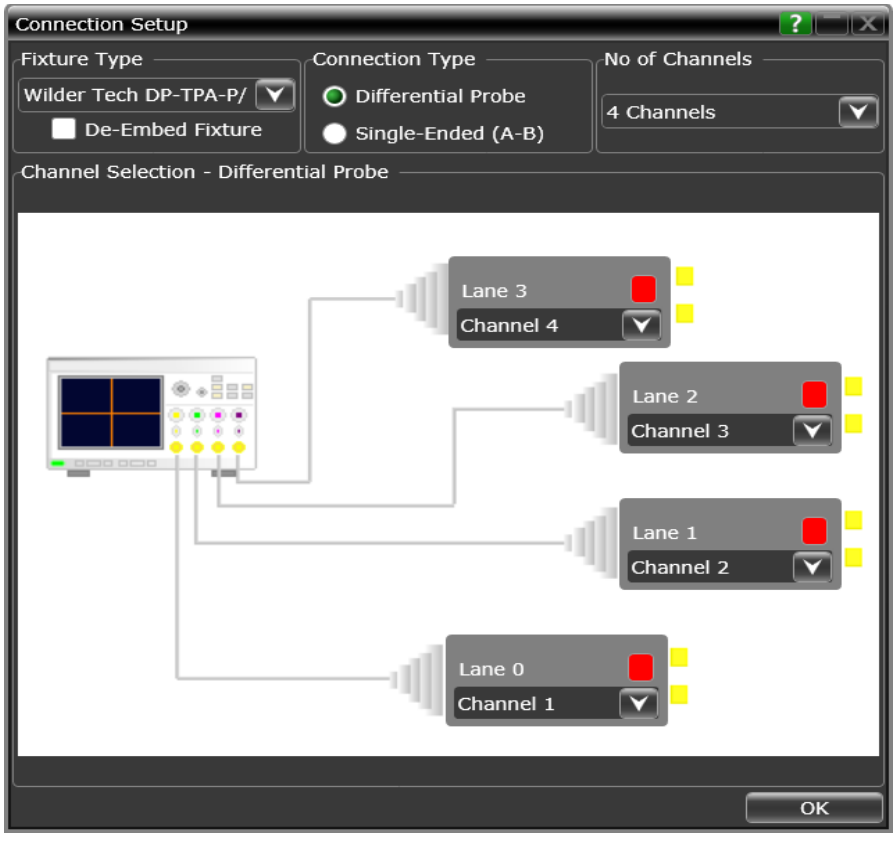
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

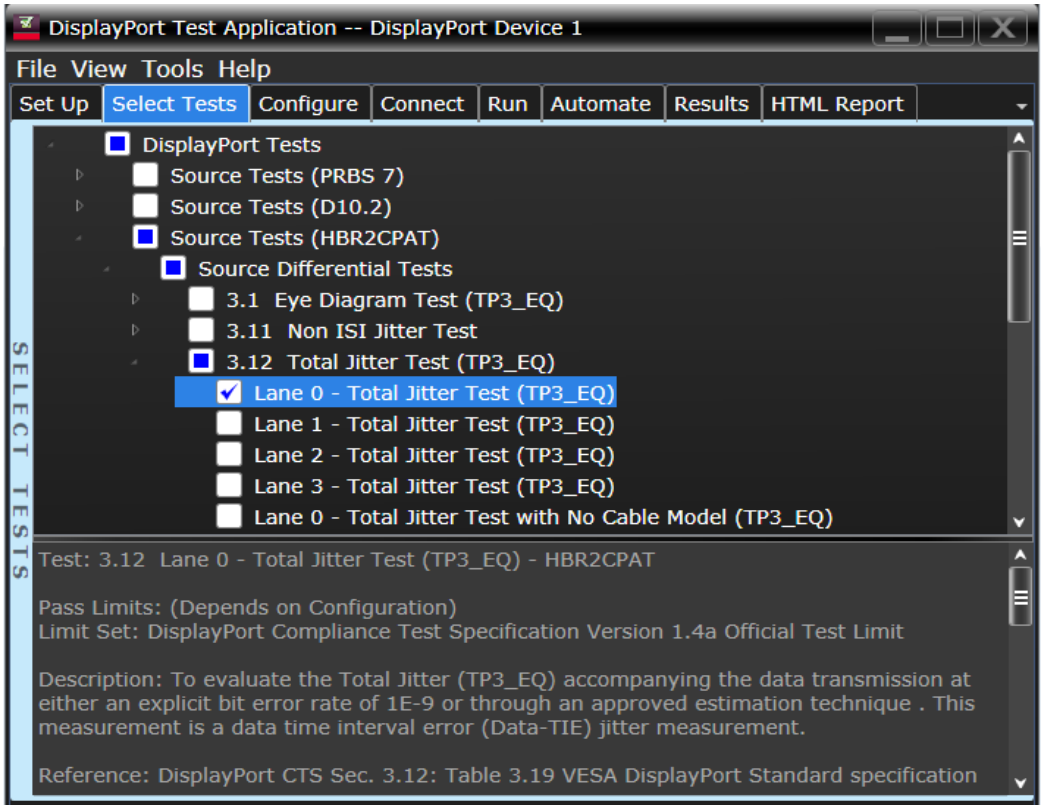
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR (Informative) and HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	HBR: PRBS7, HBR2: D10.2, and HBR2CPAT
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.

5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 118 Total Jitter at TP3_EQ

	Receiver Connector (TP3_EQ)
High-Bite Rate 2 (5.4 Gb/s per lane) - for D10.2 pattern	
A_{p-p}	≤ 0.40 UI
High-Bit Rate 2 (5.4 Gb/s per lane) - for HBR2CPAT (or CP2520) pattern	
A_{p-p}	≤ 0.580 UI*
High-Bite Rate (2.7 Gb/s per lane) - for PRBS7	
A_{p-p}	≤ 0.491 UI

* The HBR2 limits for Total Jitter calculated at TP3_EQ include a de-rating of 0.04 UI to account for cable crosstalk effect.

UI is Unit Interval.

Test References

See:

For HBR (PRBS7)

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2.7.2, Table 3-23*

For HBR2CPAT

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2.7.2, Table 3-23*

For D10.2

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*

Expected/Observable Results

The measured total jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Total Jitter Test (TP3_DFE)

Test ID

For Standard DP Pattern:

- 1224001, 1224002, 1224003, 1224004 – Total Jitter Test (TP3_DFE)
- 1223011, 1223012, 1223013, 1223014 – Total Jitter Test (TP3_DFE)

For Arbitrary Pattern:

- 1324001, 1324002, 1324003, 1324004 – Total Jitter Test (TP3_DFE)
- 1324011, 1324012, 1324013, 1324014 – Total Jitter Test (TP3_DFE)

Test Overview

The objective of this test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

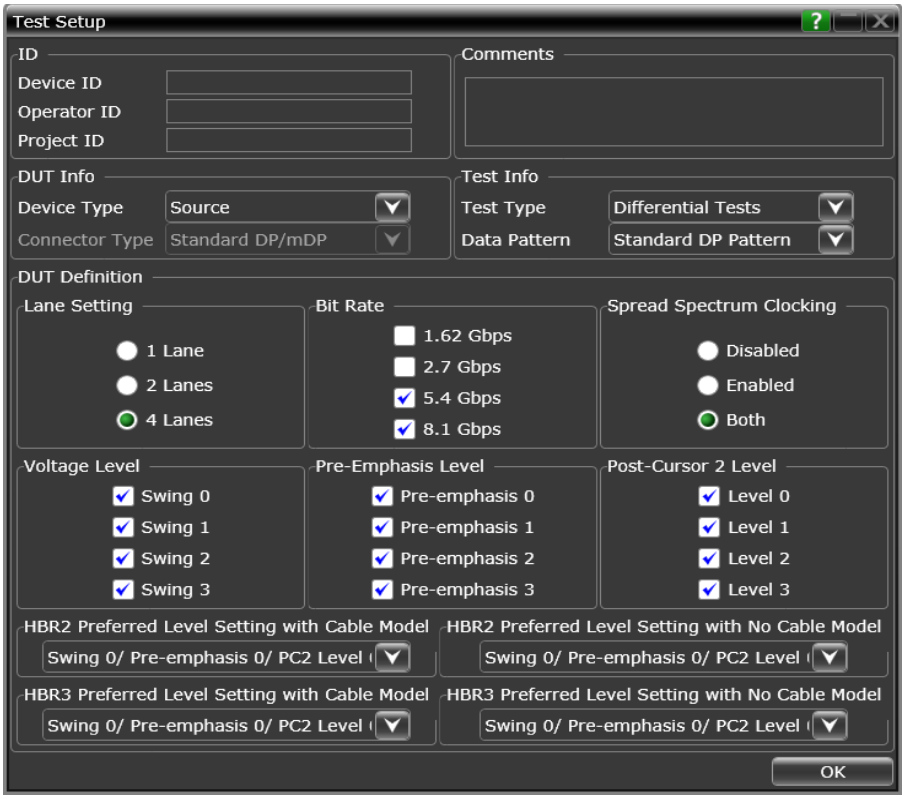
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

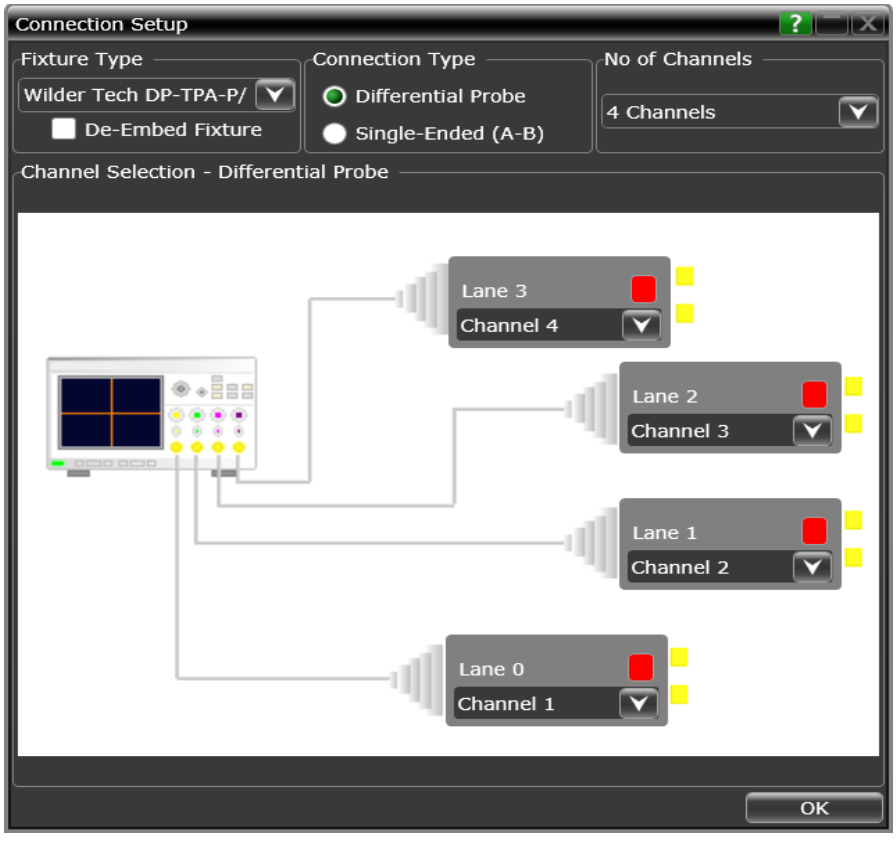
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

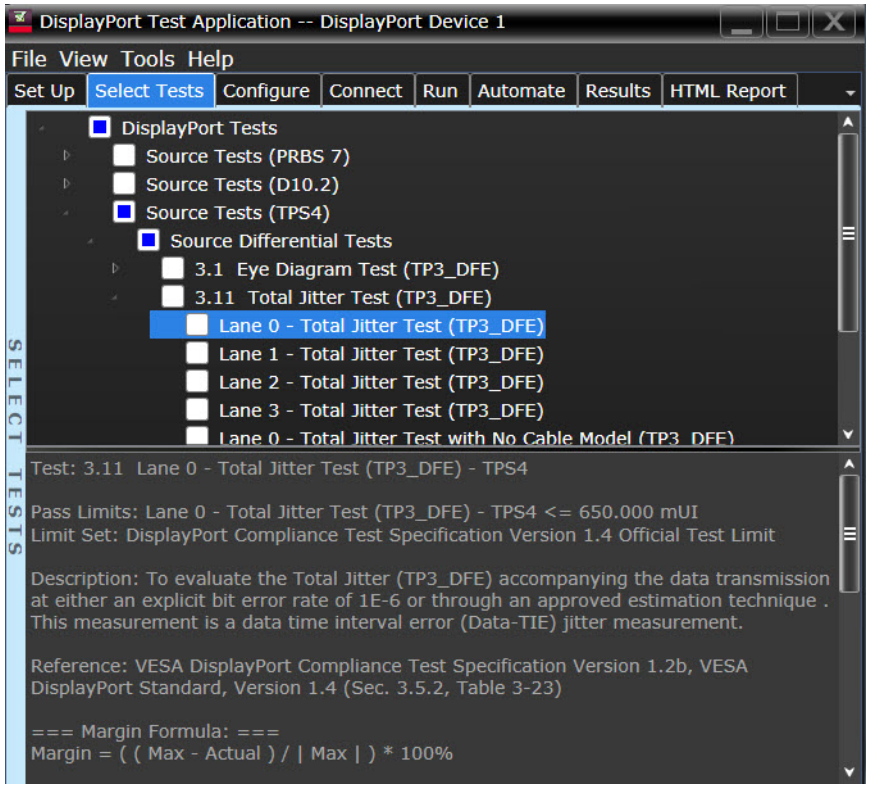
where, DJ is the Deterministic Jitter, RJ is the Random Jitter, and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test (TP3_DFE)

Test Parameter	Condition
Test Point	TP3_DFE
Bit Rate	HBR3
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	TPS4
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Total Jitter Test (TP3_DFE): Use "Worst Cable Model" as defined in the section "Cable Model".
   b For Total Jitter Test with No Cable Model (TP3_DFE): Use "Zero Length Cable Model" as defined in the section "Cable Model".
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”, exclude the DFE.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.

5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 119 Total Jitter at TP3_DFE

	Receiver Connector (TP3_DFE)
High-Bite Rate 3 (8.1 Gb/s per lane)	
A_{P-P}	0.65 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*

Expected/Observable Results

The measured total jitter for the test signal at TP3_DFE shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non ISI Jitter Test (TP3_DFE)

Test ID

For Standard DP Pattern:

- 1231001, 1231002, 1231003, 1231004 – Non ISI Jitter Test (TP3_DFE) - HBR2CPAT
- 1231011, 1231012, 1231013, 1231014 – Non ISI Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT

For Arbitrary Pattern:

- 1331001, 1331002, 1331003, 1331004 – Non ISI Jitter Test (TP3_DFE)
- 1331011, 1331012, 1331013, 1331014 – Non ISI Jitter Test with No Cable Model (TP3_EQ)

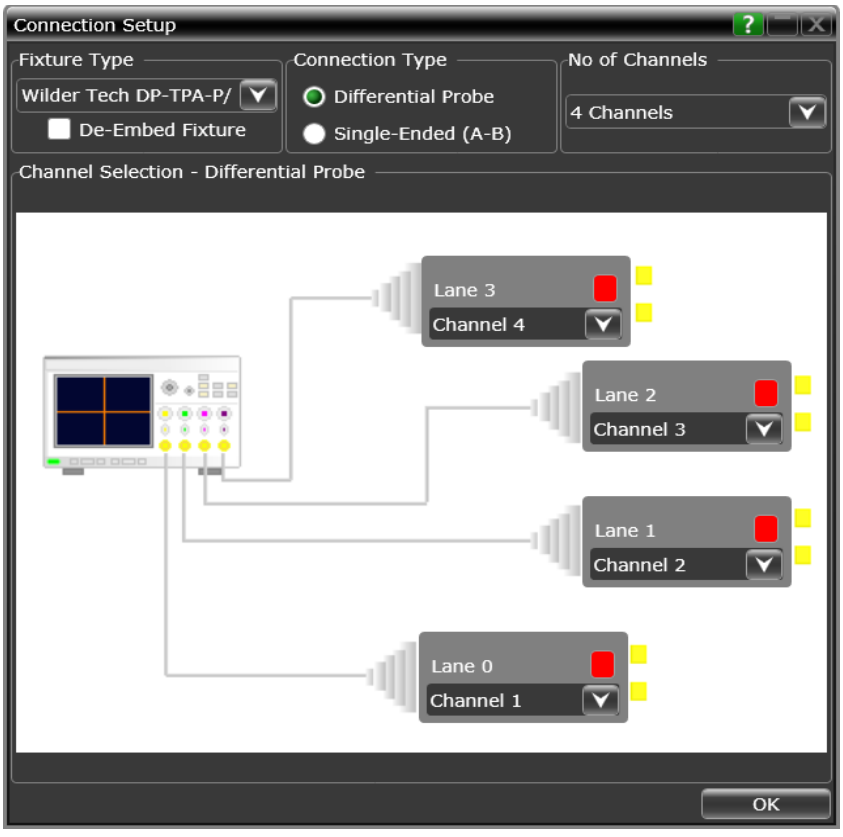
Test Overview

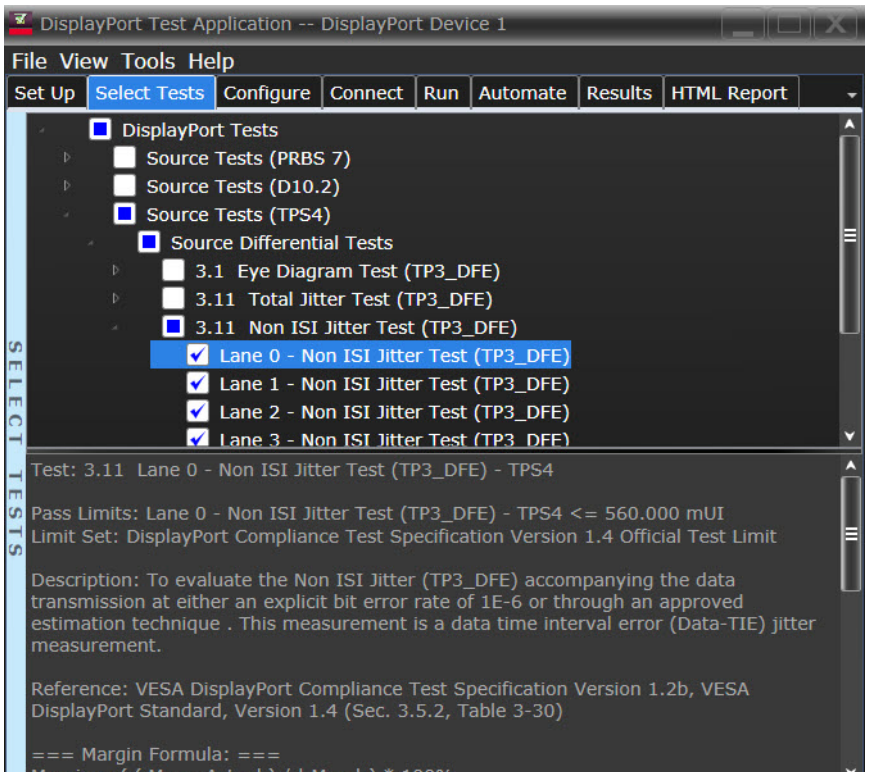
The objective of this test is to evaluate the non ISI jitter accompanying the data transmission.

Test Conditions for Non ISI Jitter Test (TP3_DFE)

Test Parameter	Condition
Test Point	TP3_DFE
Bit Rate	HBR3
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	TPS4
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Non ISI Jitter Test (TP3_DFE): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Non ISI Jitter Test with No Cable Model (TP3_DFE): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.

5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Calculate the non ISI jitter base on following equation:
   Non ISI Jitter = TJ - ISI
8 Report the measurement results.

PASS Condition

Table 120 Non ISI Jitter at TP3_DFE

	Receiver Connector (TP3_DFE)
High-Bit Rate 3 (8.1 Gb/s per lane)	
A_{p-p}	0.56 UI

UI is Unit Interval.

xTest References

See:

- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2.7.2, Table 3-23*

Expected/Observable Results

The measured non ISI jitter for the test signal at TP3_DFE shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Deterministic Jitter Test (TP3_EQ)

Test ID

For Standard DP Pattern:

- 1236001, 1236002, 1236003, 1236004 – Deterministic Jitter Test (TP3_EQ) - HBR2CPAT
- 1236011, 1236012, 1236013, 1236014 – Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1235001, 1235002, 1235003, 1235004 – Deterministic Jitter Test (TP3_EQ) - D10.2
- 1235011, 1235012, 1235013, 1235014 – Deterministic Jitter Test with No Cable Model (TP3_EQ) - D10.2

For Arbitrary Pattern:

- 1336001, 1336002, 1336003, 1336004 – Deterministic Jitter Test (TP3_EQ)
- 1336011, 1336012, 1336013, 1336014 – Deterministic Jitter Test with No Cable Model (TP3_EQ)

Test Overview

The objective of this test is to evaluate the deterministic jitter accompanying the data transmission. The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

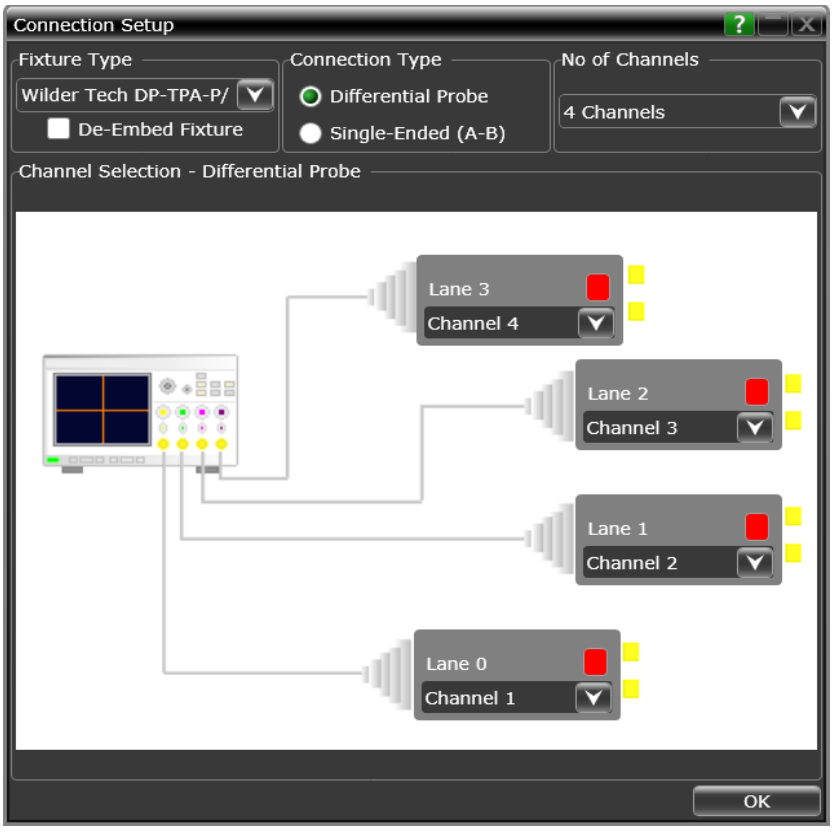
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

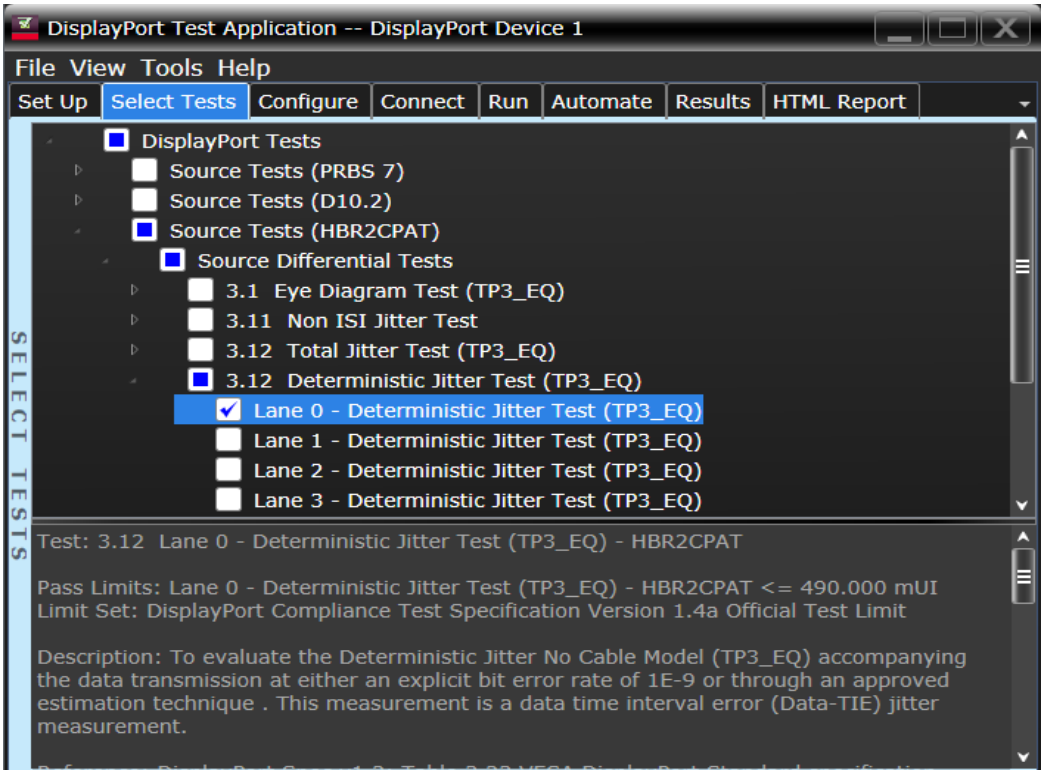
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Deterministic Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Deterministic Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Deterministic Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.

6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 121 Deterministic Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.49 UI

Table 122 Deterministic Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.27 UI

UI is Unit Interval.

Test References

See:

For HBR2CPAT

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2.7.2, Table 3-23*

For D10.2

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*

Expected/Observable Results

The measured deterministic jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Random Jitter Test (TP3_EQ)

Test ID

For Standard DP Pattern:

- 1238001, 1238002, 1238003, 1238004 – Random Jitter Test (TP3_EQ) - D10.2
- 1238011, 1238012, 1238013, 1238014 – Random Jitter Test with No Cable Model (TP3_EQ)

For Arbitrary Pattern:

- 1338001, 1338002, 1338003, 1338004 – Random Jitter Test (TP3_EQ)
- 1338011, 1338012, 1338013, 1338014 – Random Jitter Test with No Cable Model (TP3_EQ)

Test Overview

The objective of this test is to evaluate the random jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. The jitter is separated into each jitter components and the random jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

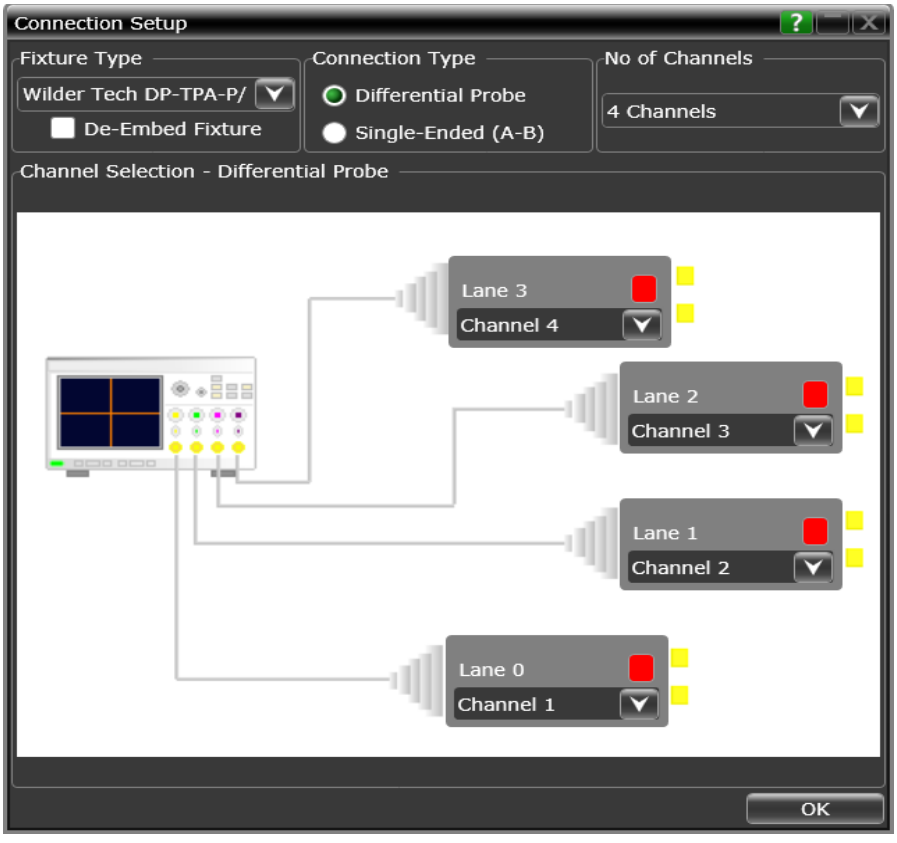
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

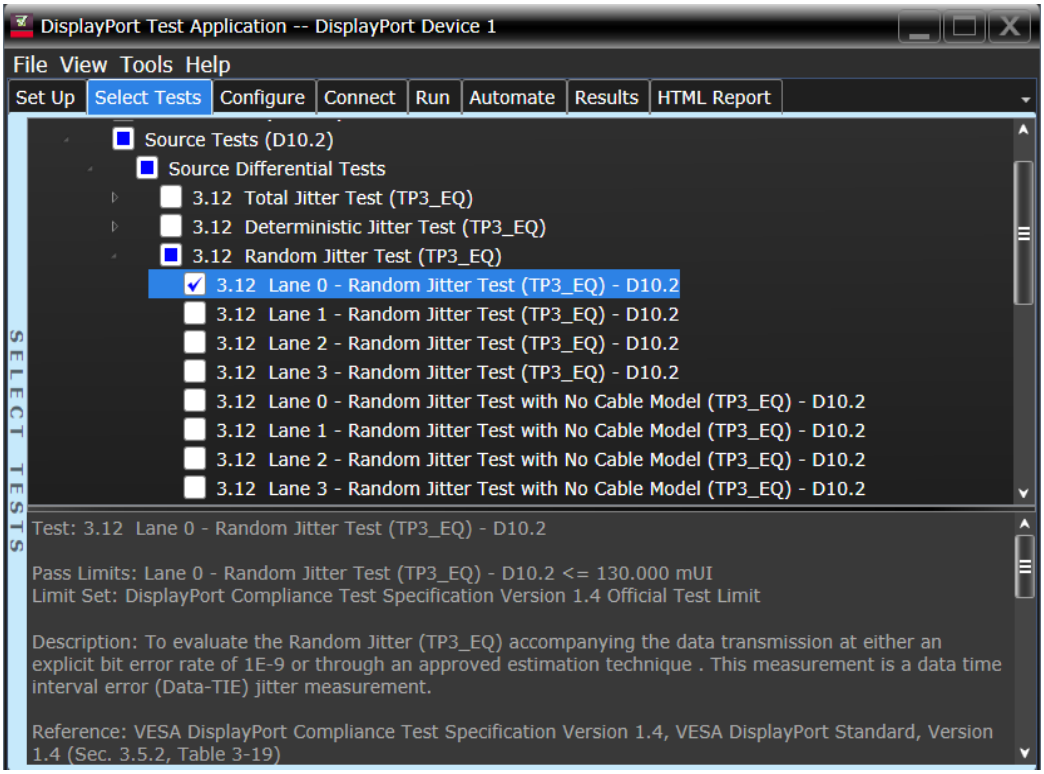
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Random Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	D10.2
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Random Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Random Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.

6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 123 Random Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.13 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*

Expected/Observable Results

The measured random jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source AC Common Mode Test (Informative)

Test ID

For Standard DP Pattern:

- 12110001, 12110002, 12110003, 12110004 – AC Common Mode Test (Informative)

For Arbitrary Pattern:

- 13110001, 13110002, 13110003, 13110004 – AC Common Mode Test (Informative)

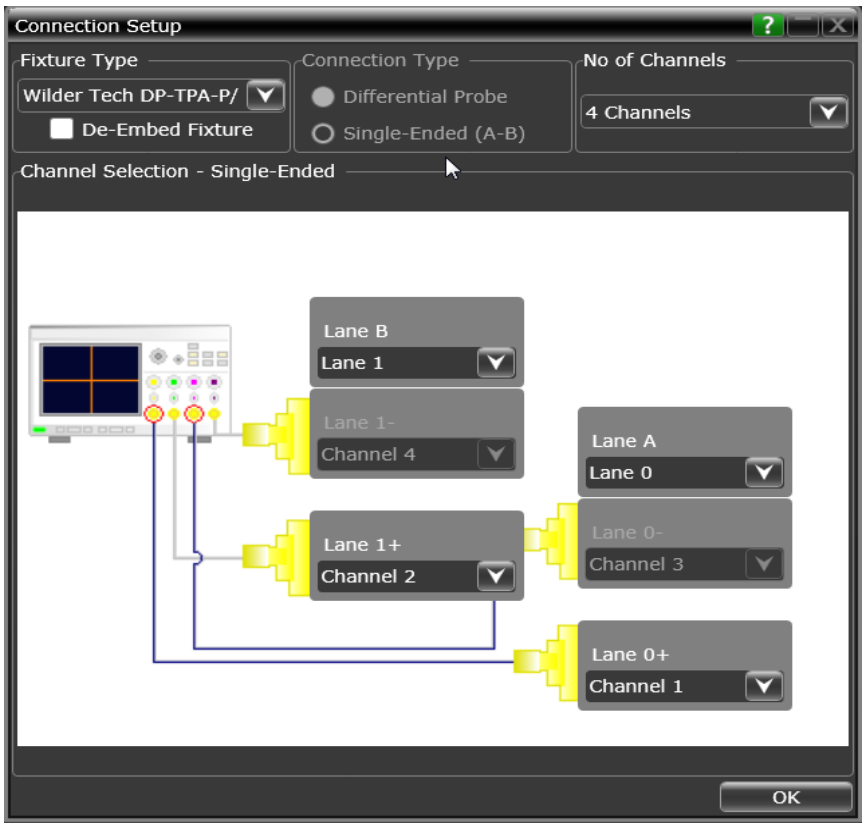
Test Overview

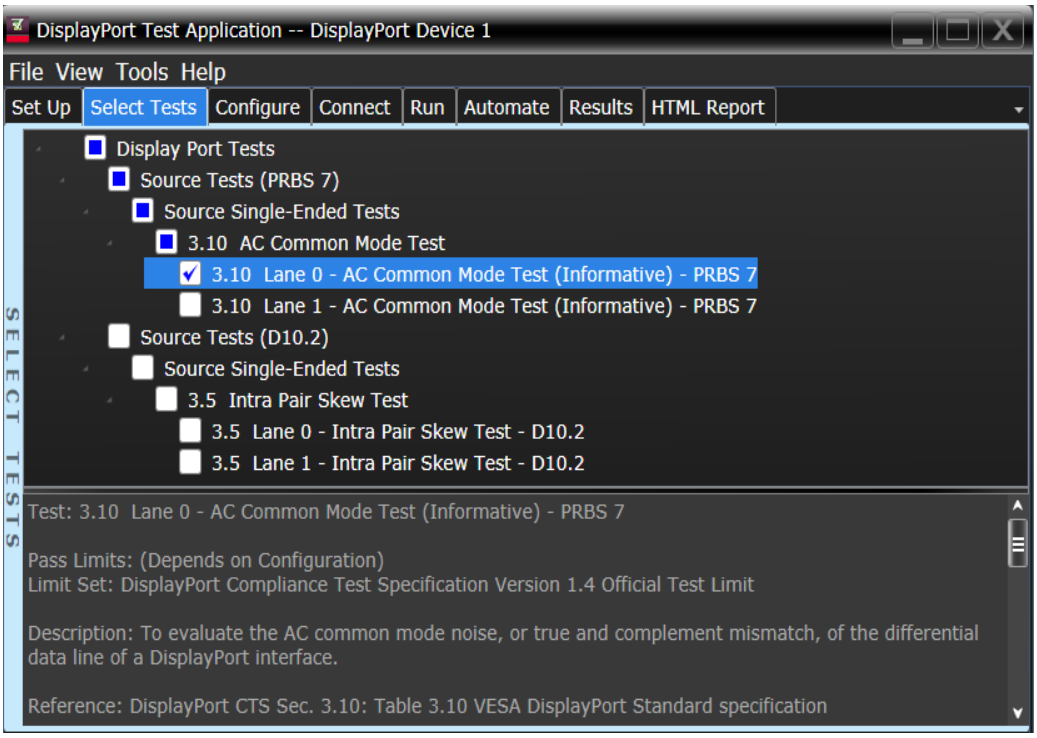
The objective of this test is to evaluate the AC Common Mode noise (unfiltered rms) of the differential data line of the DP interface.

Test Conditions for AC Common Mode Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels supported subject to the constraints in Table 3-1 of the VESA DisplayPort 1.4 Standard
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Single-Ended Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Create FUNC3 signal, which is the common mode signal of the input single-ended signal.
4 If the filter is enabled [“Filter” configuration variable set to “High Pass Filter”, “Low Pass Filter” or “None” (Default)]:
   a Create FUNC4 signal, which is the filtered FUNC3 signal by applying the High Pass filter or Low Pass filter on the FUNC3 signal based on the Configuration Variable.
5 Set up two display grids such that one grid displays the input single-ended signal while the other grid displays the common mode signal.
6 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
7 Set up the parameters for RMS voltage measurement of the common mode signal.
   a Set up the V_{rms} measurement for the common mode signal.
   b Acquire the signal until 100,000 edges are measured.

8 Get the mean for the V_{rms} measurement.

9 Report the measurement results.

PASS Condition

For RBR and HBR:

AC Common Mode Voltage $\leq$ 20mV

For HBR2 and HBR3:

AC Common Mode Voltage $\leq$ 30mV

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.10*
- *VESA DisplayPort (DP) Standard Version 1.4, Section D.2, Table D-3*

Expected/Observable Results

The measured AC common mode noise for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Intra-Pair Skew Test (Informative)

Test ID

For Standard DP Pattern:

- 12100001, 12100002, 12100003, 12100004 – Intra-Pair Skew Test (Informative)

For Arbitrary Pattern:

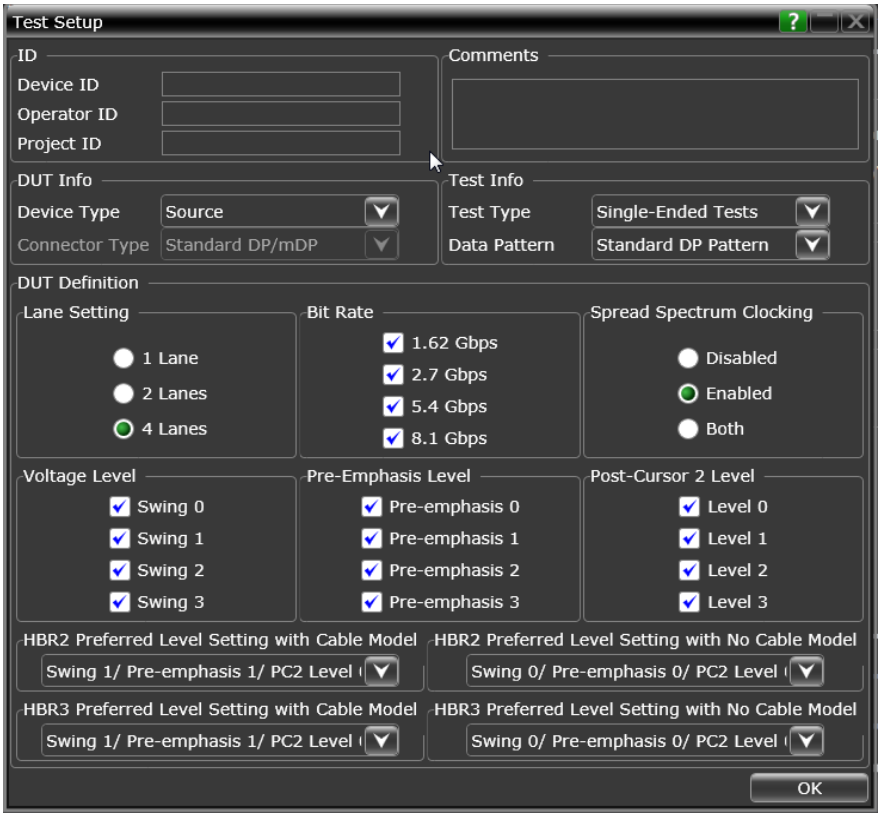
- 13100001, 13100002, 13100003, 13100004 – Intra-Pair Skew Test (Informative)

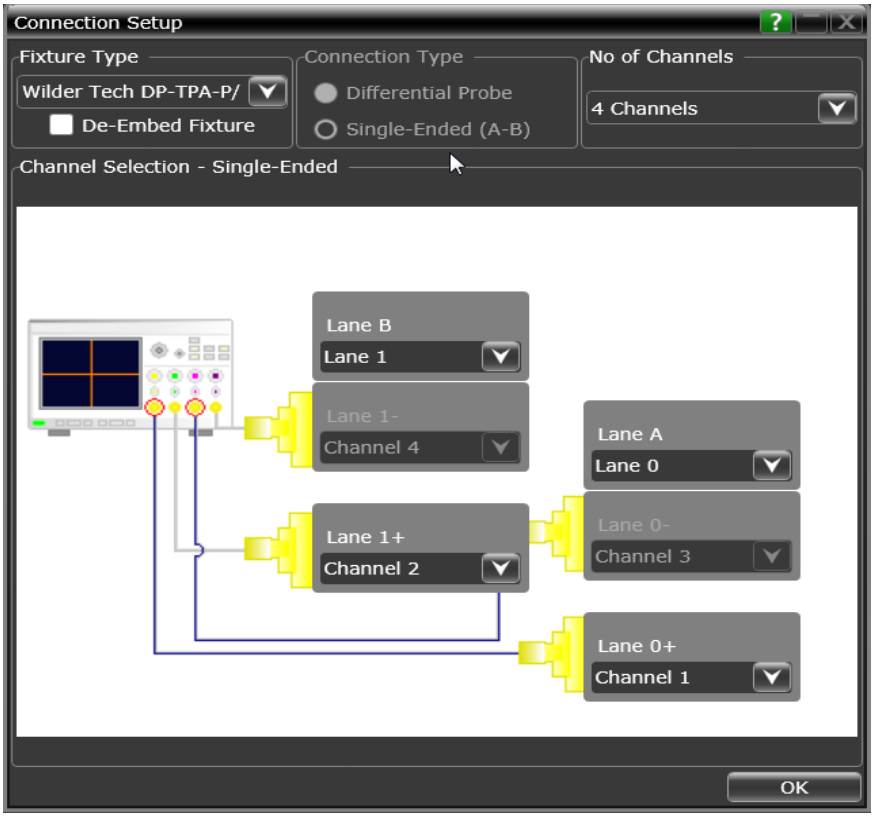
Test Overview

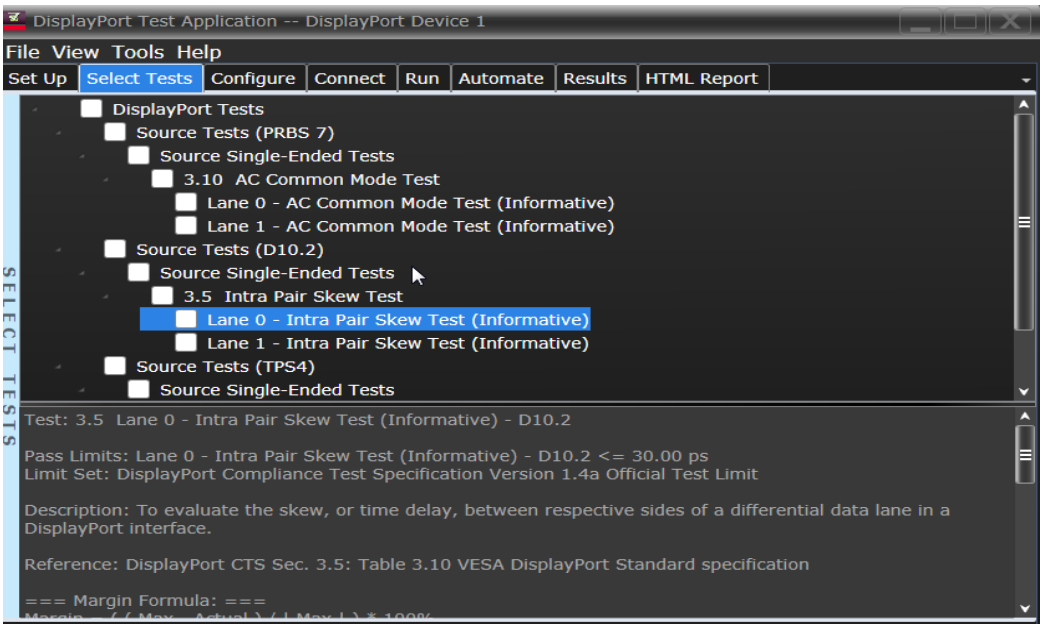
The objective of this test is to evaluate the skew or time delay between respective sides of a differential data lane in the DP interface.

Test Conditions for Intra-Pair Skew Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR3)
SSC	Both SSC conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported For one lane operation: Lane 0+ to Lane 0- For two lane operation: Lane 0+ to Lane 0- Lane 1+ to Lane 1- For four lane operation: Lane 0+ to Lane 0- Lane 1+ to Lane 1- Lane 2+ to Lane 2- Lane 3+ to Lane 3-
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Single-Ended Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
4 Set up the parameters to perform High Level Voltage (V_{HIGH}) and Low Level Voltage (V_{LOW}) for each input single-ended signal.
   a Scale the vertical display of the input single-ended signal to optimum value.
   b Acquire the signal for 100 waveforms.
   c Find V_{HIGH} by measuring the average voltage at 0.06 UI to 0.75 UI of the High Level.
   d Find V_{LOW} by measuring the average voltage at 0.06 UI to 0.75 UI of the Low Level.
   e Calculate the Transition Voltage (V_{Trans}) using the equation:

$$V_{Trans} = (V_{HIGH} + V_{LOW}) / 2$$

5 Set up the parameters for the intra-pair skew measurement:

a Set up the measurement threshold for each single-ended data signal based on the measured Transition Voltage.

b Set up InfiniiScan to trigger on the desired pattern.

c Set up delta time measurement to measure time difference between the rising edge of the data true signal (D+) and the complement's (D-) falling edge:

$$D+_{Transition\_High} - D-_{Transition\_Low}$$

d Set up delta time measurement to measure time difference between the falling edge of the data true signal (D+) and the complement's (D-) rising edge:

$$D+_{Transition\_Low} - D-_{Transition\_High}$$

e Acquire the signal until you measure 100 edges.

f Calculate the intra-pair skew using the equation:

$$\text{Intra-Pair Skew} = \{1/\text{Number of Edges}\}$$

$$\sum \{[(D+_{Transition\_High} - D-_{Transition\_Low}) + (D+_{Transition\_Low} - D-_{Transition\_High})] / 2\}$$

6 Report the measurement results.

PASS Condition

Intra-Pair skew ≤ 30 ps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.5*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-18*

Expected/Observable Results

The measured intra-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

15 DisplayPort 1.4 Sink Tests

Overview

Test Point Definition for DisplayPort 1.4 Sink Tests

NOTE Sink Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Sink DUT at Test Point 3 (TP3) as shown in Figure 110. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

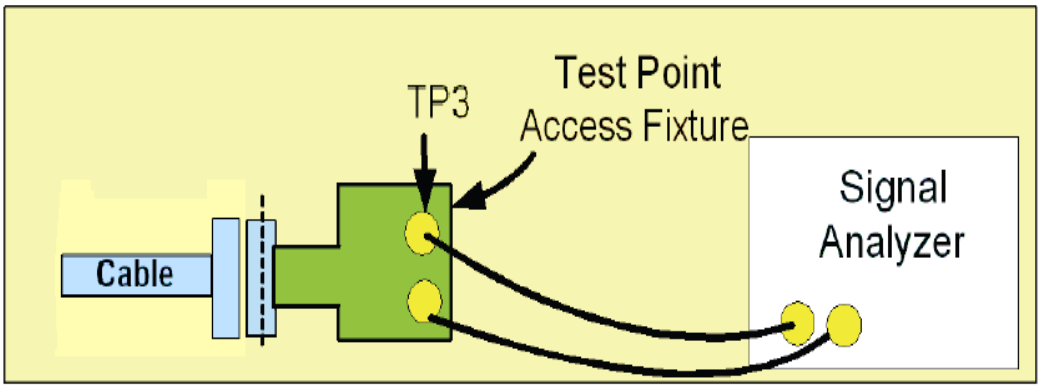


Figure 110 Test Point 3 Connection for DisplayPort 1.4 Sink Tests

Table 124 defines the test point fixtures and instruments used for DisplayPort 1.4 Sink Tests:

Table 124 Test Point Fixtures and Instruments for DisplayPort 1.4 Sink Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** For USB Type-C Connector, ▪ Wilder Technologies DPC-TPA-R* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Calibration of Stress Signal

For the calibration of the stress signal, you must test the stress signal in the manner shown in the Figure 111 for RBR and Figure 112 for HBR and HBR2.

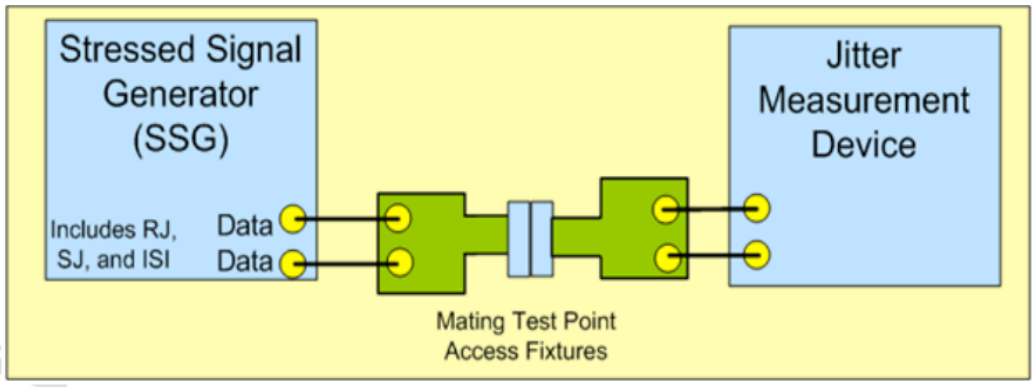


Figure 111 Test Point 3 Connection for Stress Signal Calibration of RBR

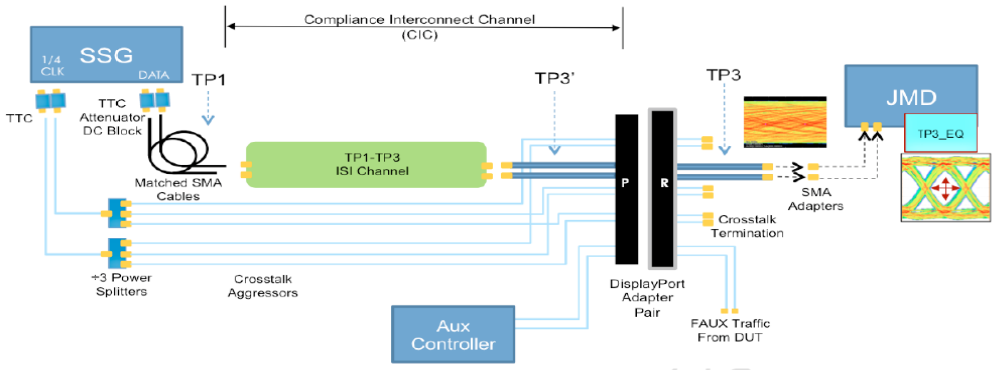


Figure 112 Test Point 3 Connection for Stress Signal Calibration of HBR and HBR2

Table 125 defines the Test Point 3 Connections for Stress Signal Calibration:

Table 125 Test Point Connections for Stress Signal Calibration

Test Requirement	Device Used
Stress Signal Generator (SSG)	Bit Error Rate Tester ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** For USB Type-C Connector, ▪ Wilder Technologies DPC-TPA-R* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Jitter Measurement Device (JMD)	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.4 Sink Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort 1.4 Standards, select the option **1.4** in the **Test Specification** area.

5 The option **Physical Layer Tests** appears by default in the **Test Selection** area.

6 Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.

7 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

8 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

9 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

10 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

11 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

12 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

13 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

14 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DisplayPort 1.4 Sink Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

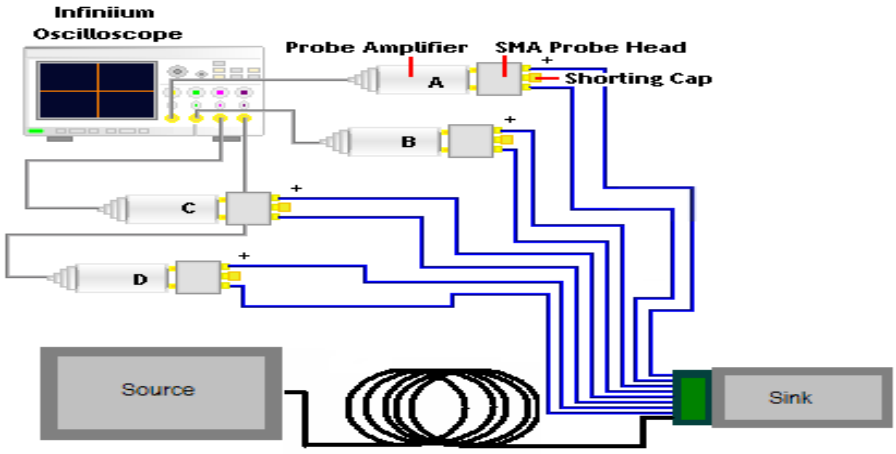


Figure 113 Sample connection diagram for DisplayPort 1.4 Sink Tests

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Sink tests to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1 In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.

2 On the **Test Setup** window,

a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b In the **DUT Info** area, select **Device Type** as **Sink**. The **Connector Type** is grayed out.

c In the **Test Info** area, the **Test Type** is grayed out.

d In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.

3 Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1 Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.

2 On the **Connection Setup** window,

a Select the appropriate option in the **Fixture Type** to indicate where the DUT is connected to.

b Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.

c In the **Channel Selection** area, assign appropriate channels to lanes.

3 Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of sink tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.4 Sink Tests" on page 602 to complete the task flow for DUT setup along with configuring the Compliance Application to run each test.

Sink Eye Diagram Test

Test ID

12140001, 12140002, 12140003, 12140004 – Eye Diagram Test

Test Overview

The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

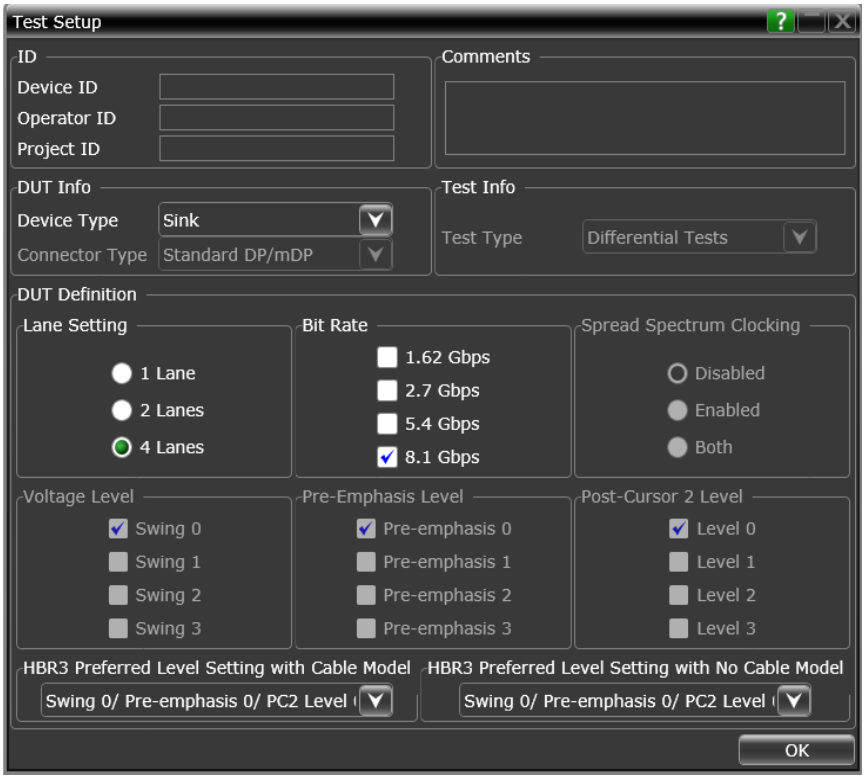
You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the following specifications for degradation:

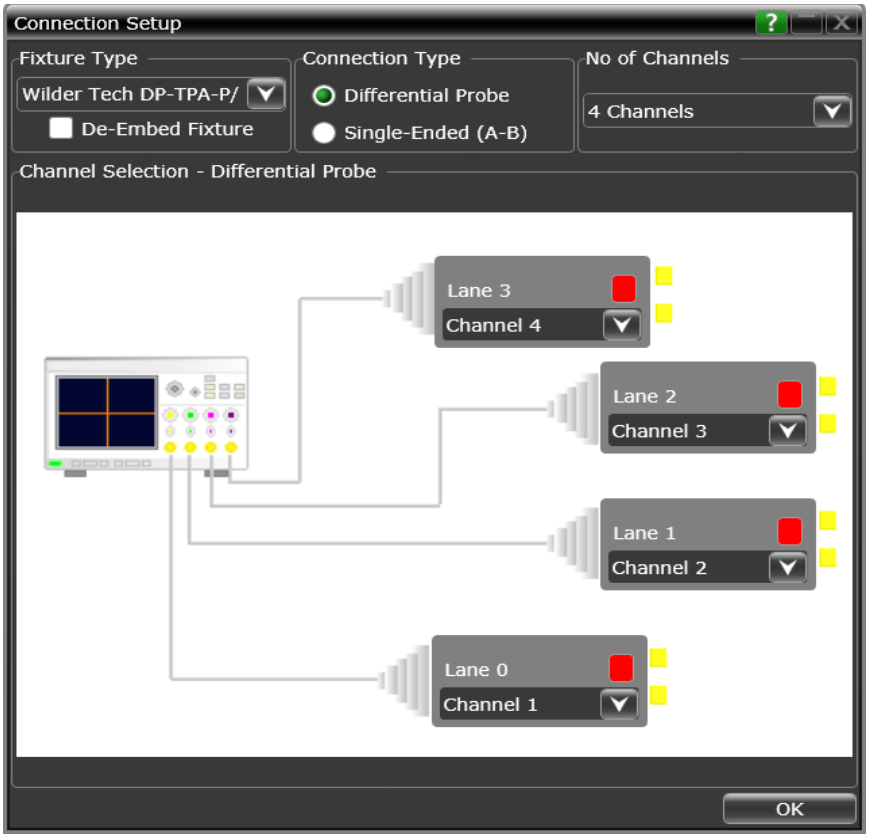
- Voltage Level:
  - 90mV peak to peak +/- 10% for HBR2 at TP3_EQ (Table 3-18, DP1.2a)
  - 150mV peak to peak +/- 10% for HBR at TP3_EQ (Table 3-25, DP1.2a)
  - 46mV peak to peak +/- 10% for RBR at TP3 (Table 3-26, DP1.2a

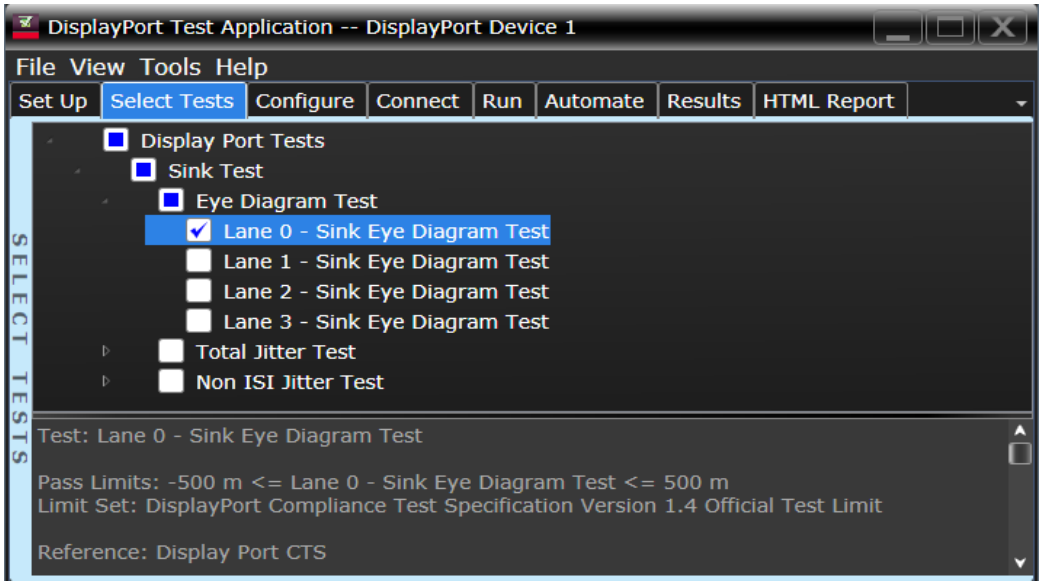
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR3–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR3)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR3–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
9 Measure the jitter of the eye diagram using the Histogram.
10 Check for any signal trajectories that may have entered into the mask.

11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 126 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 126 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

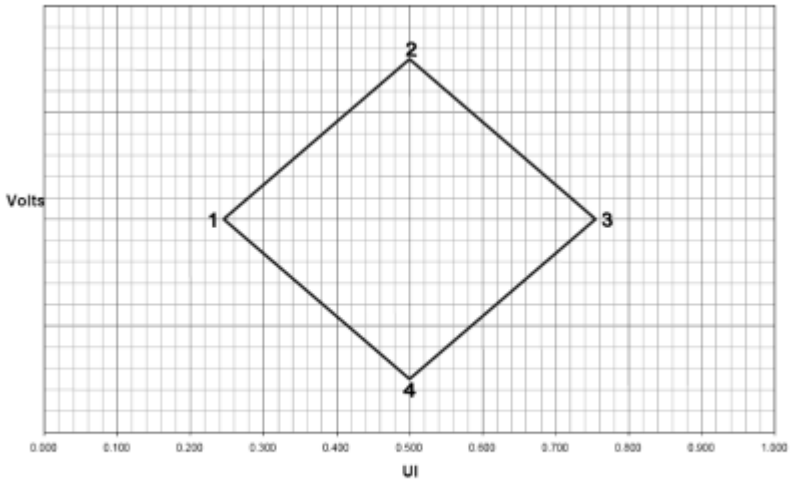


Figure 114 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 127 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.045*
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.045*

NOTE

*Eye height limit of 45 mV and -45 mV assumes cross-talk as 0, which is only possible in case of single lane testing.

In case of multi-lane testing, cross talk exists, and the eye height values deviate by ± 7 mV. Thus the eye height becomes (+45 +7) mV and (-45 -7) mV or +52 mV and -52 mV.

Table 128 Eye Diagram Mask Coordinates for TP3_EQ (HBR3)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.35UI	0.00000
2	Any passing UI location between 0.375 and 0.625UI	0.00375
3	Point 1 + 0.35UI	0.00000
4	Same as Point 2	-0.00375

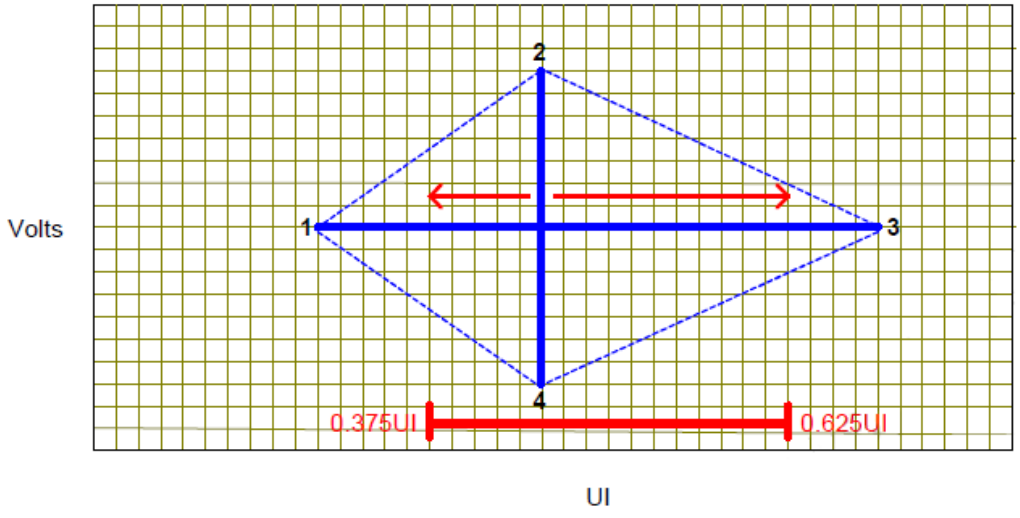


Figure 115 The Eye Mask at TP3_EQ (HBR2 and HBR3)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Sink Total Jitter Test

Test ID

12210001, 12210002, 12210003, 12210004 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

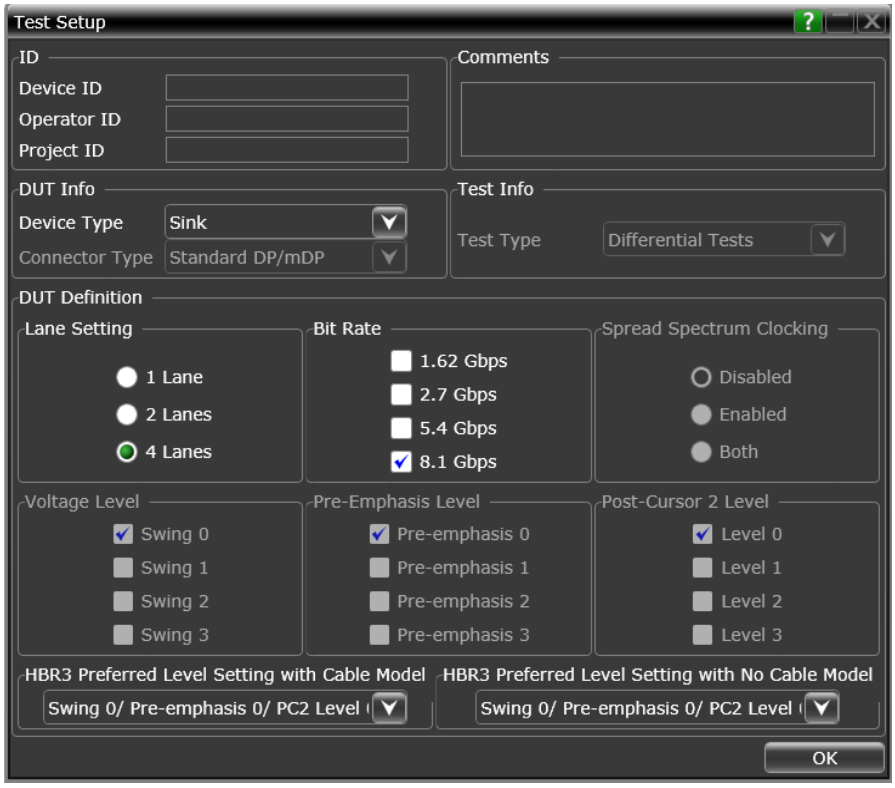
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

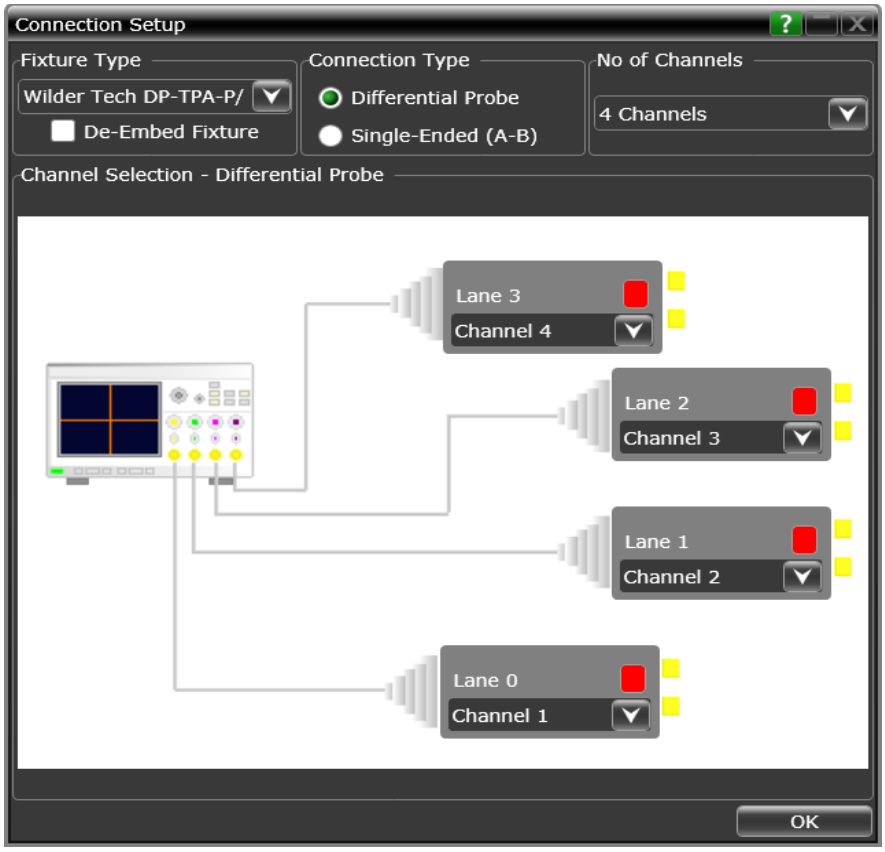
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

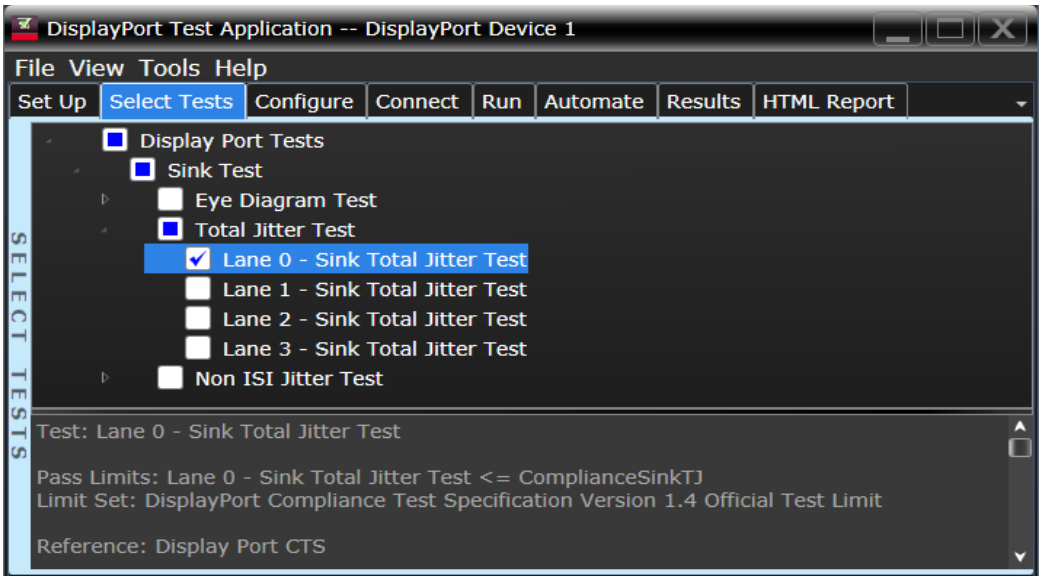
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR3–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR3)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR3–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 129 Total Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	0.580 UI*

* The limits for the Total Jitter are derated by 0.04 UI from 0.62 UI limit in DisplayPort 1.2a Standard.

Table 130 Total Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Sink Non-ISI Jitter Test

Test ID

12220001, 12220002, 12220003, 12220004 – Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

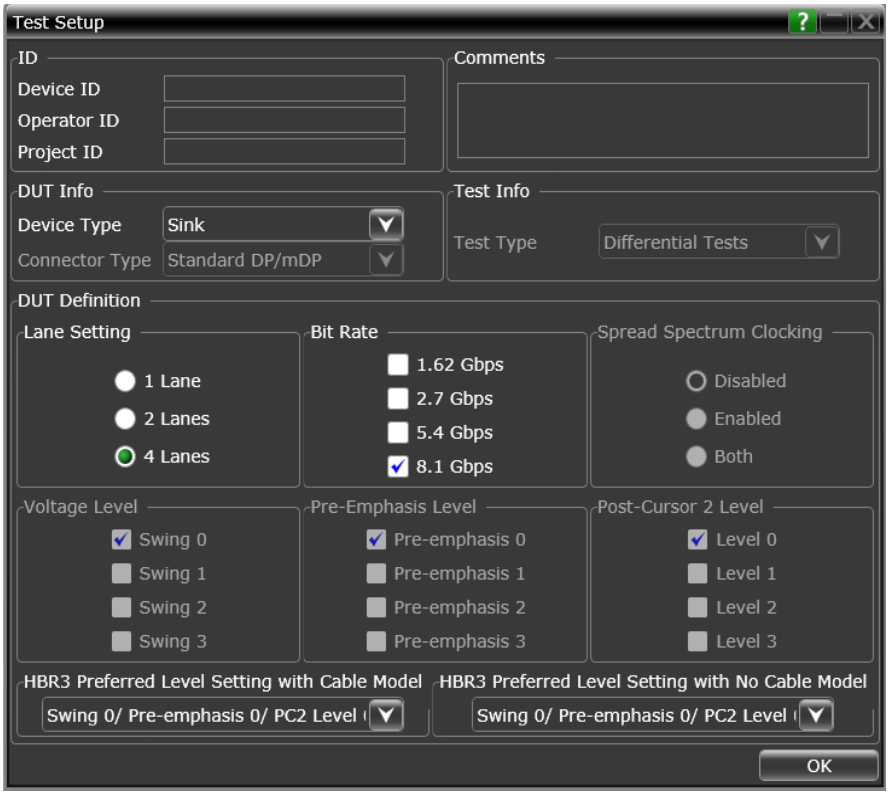
Calculate Non-ISI Jitter using the following equation:

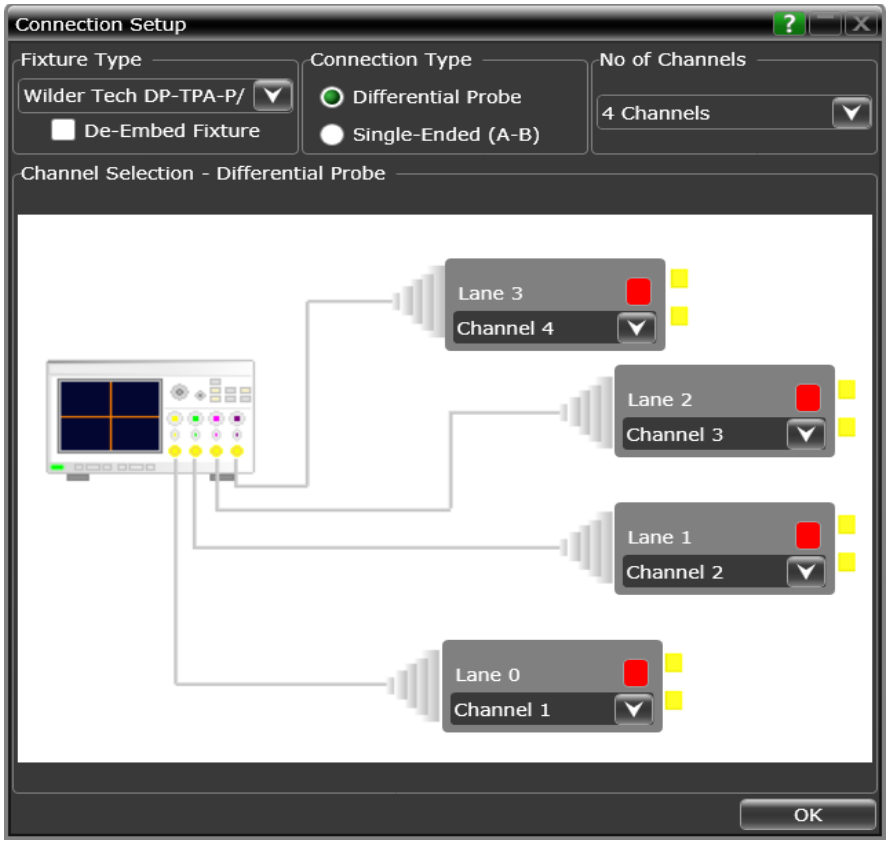
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

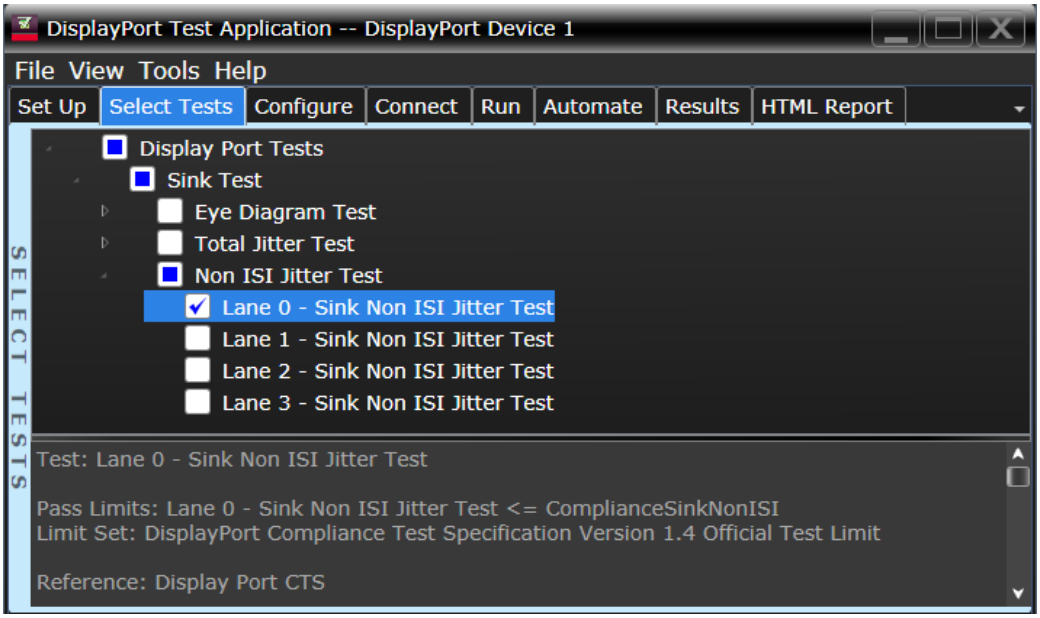
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR3–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR3)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR3–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 131 Non ISI Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	-

Table 132 Non ISI Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

16 DisplayPort 1.4 Cable Tests

Overview

Test Point Definition for DisplayPort 1.4 Cable Tests

NOTE Cable Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Cable DUT at Test Point 3 (TP3) as shown in Figure 116. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

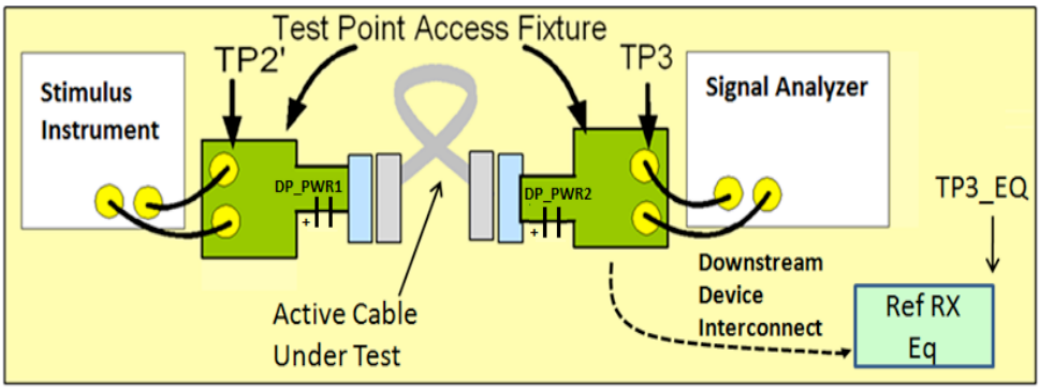


Figure 116 Test Point 3 Connection for DisplayPort 1.4 Cable Tests

Table 133 defines the test point fixtures and instruments used for DisplayPort 1.4 Cable Tests:

Table 133 Test Point Fixtures and Instruments for DisplayPort 1.4 Cable Tests

Test Requirement	Device Used
Stimulus Instrument	Pulse Pattern Generator ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** For USB Type-C Connector ▪ Wilder Technologies DPC-TPA-R* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Table 134 defines the input signal parameters applied by the stimulus instrument at TP2:

Table 134 Input Signal Parameters by Stimulus Instrument

RBR	▪ Reference Table 3-22 and Table 3-24, DP 1.2a ▪ Edge Rate (20-80): 155-165ps (260mUI) ▪ Eye Height: 400mV ▪ Total Jitter: 270mUI ▪ ISI: 100mUI ▪ Random Jitter (rms): 7.9mUI ▪ Sinusoidal Jitter: ~75mUI at 20MHz (Adjust to achieve Total Jitter)
HBR	▪ Reference Table 3-22 and Table 3-23, DP 1.2a ▪ Edge Rate (20-80): 90-100ps (260mUI) ▪ Eye Height: 350mV ▪ Total Jitter: 420mUI ▪ ISI: 144mUI ▪ Random Jitter (rms): 13.2mUI ▪ Sinusoidal Jitter: ~117mUI at 20MHz (Adjust to achieve Total Jitter)

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.4 Cable Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort 1.4 Standards, select the option **1.4** in the **Test Specification** area.
5. The option **Physical Layer Tests** appears by default in the **Test Selection** area.
6. Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.
7. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
8. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
9. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
10. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
11. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
12. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
13. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
14. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DisplayPort 1.4 Cable Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

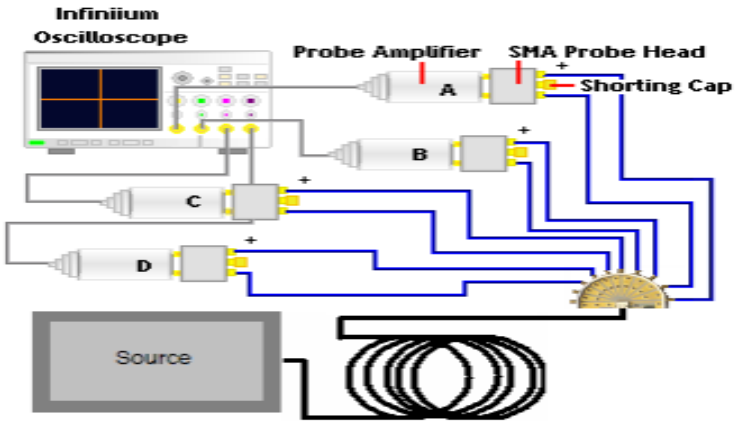


Figure 117 Sample connection diagram for DisplayPort 1.4 Cable Tests

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Cable tests to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1 In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.

2 On the **Test Setup** window,

a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b In the **DUT Info** area, select the **Device Type** as **Cable**. The **Connector Type** is grayed out.

c In the **Test Info** area, the **Test Type** options are grayed out.

d In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.

3 Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1 Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.

2 On the **Connection Setup** window,

a Select the appropriate option in the **Fixture Type** to indicate where the DUT is connected to.

b Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.

c In the **Channel Selection** area, assign appropriate channels to lanes.

3 Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of cable tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.4 Cable Tests" on page 622 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Cable Eye Diagram Test

Test ID

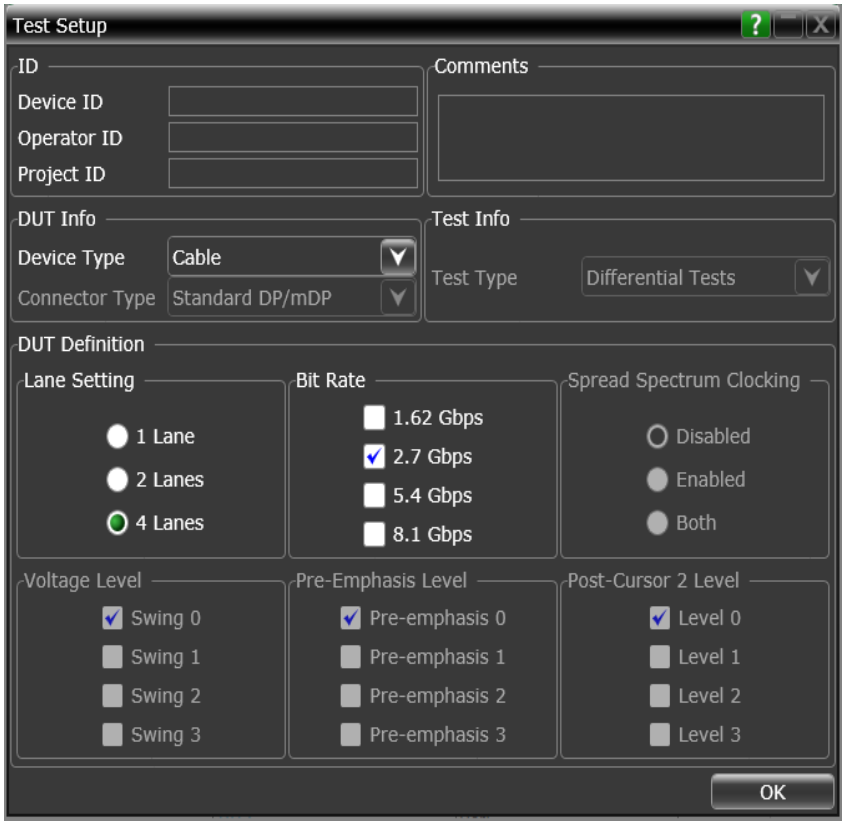
12150001, 12150002, 12150003, 12150004 – Eye Diagram Test

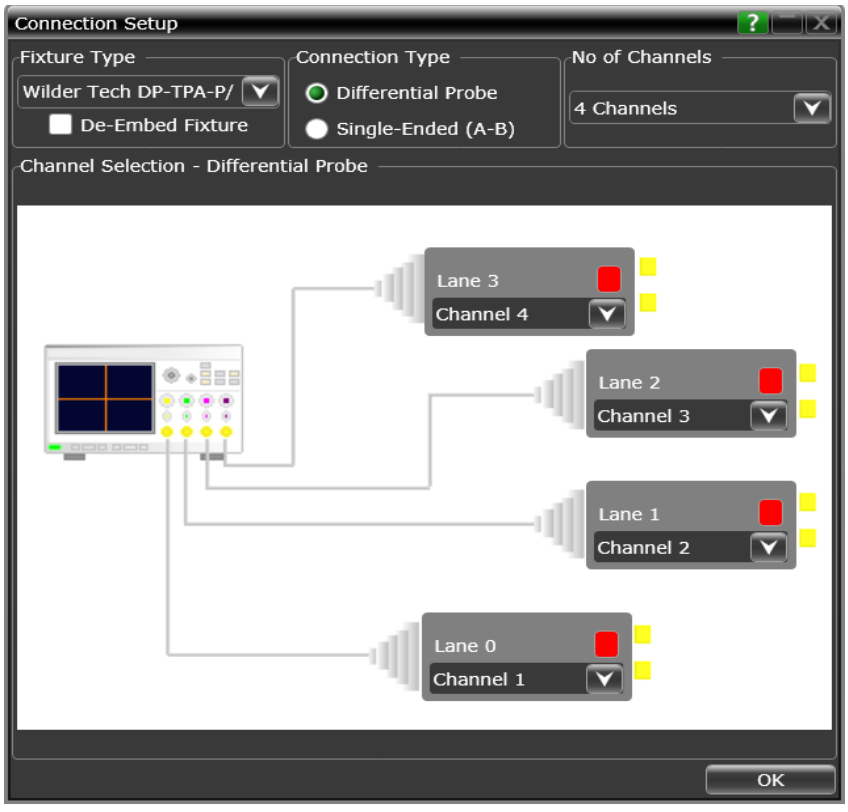
Test Overview

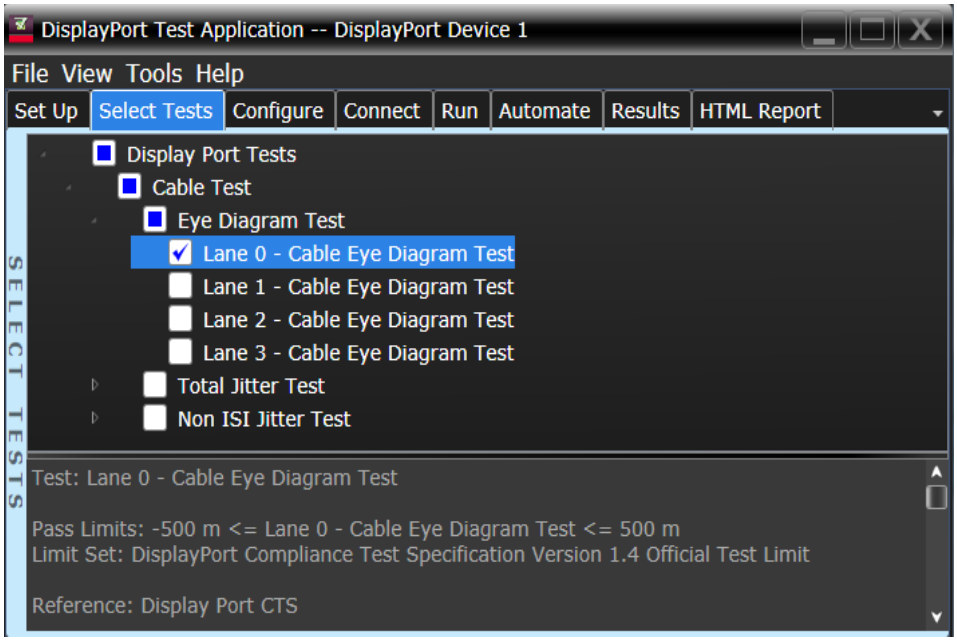
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 134
Crosstalk Signal Parameter	Quarter-rate clock signal (D24.3 pattern) is injected to lanes other than the lane under test. The characteristics of the aggressor signals are: Pattern–D24.3 Bit Rate–(Same as lane under test) Voltage Amplitude–(Same as lane under test) ▪ RBR-400mV ▪ HBR-350mV Edge Rate (20-80)–130ps at TP3


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
9 Measure the jitter of the eye diagram using the Histogram.

10 Check for any signal trajectories that may have entered into the mask.

11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 135 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 135 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

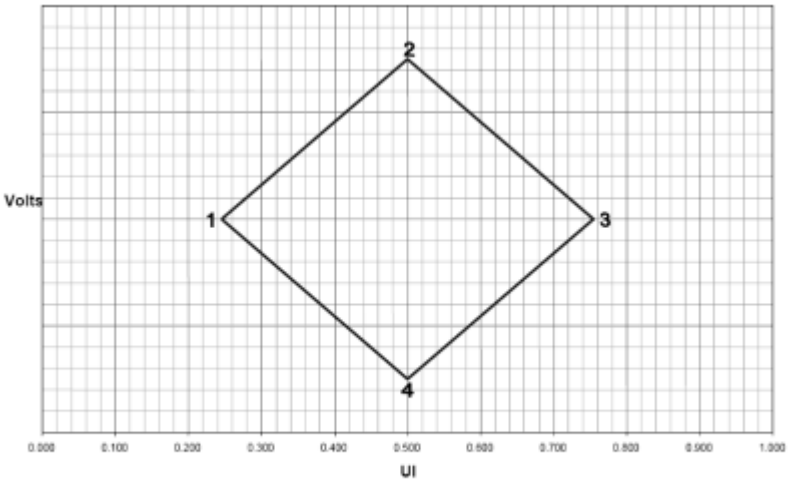


Figure 118 The Cable Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Cable Total Jitter Test

Test ID

12230001, 12230002, 12230003, 12230004 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

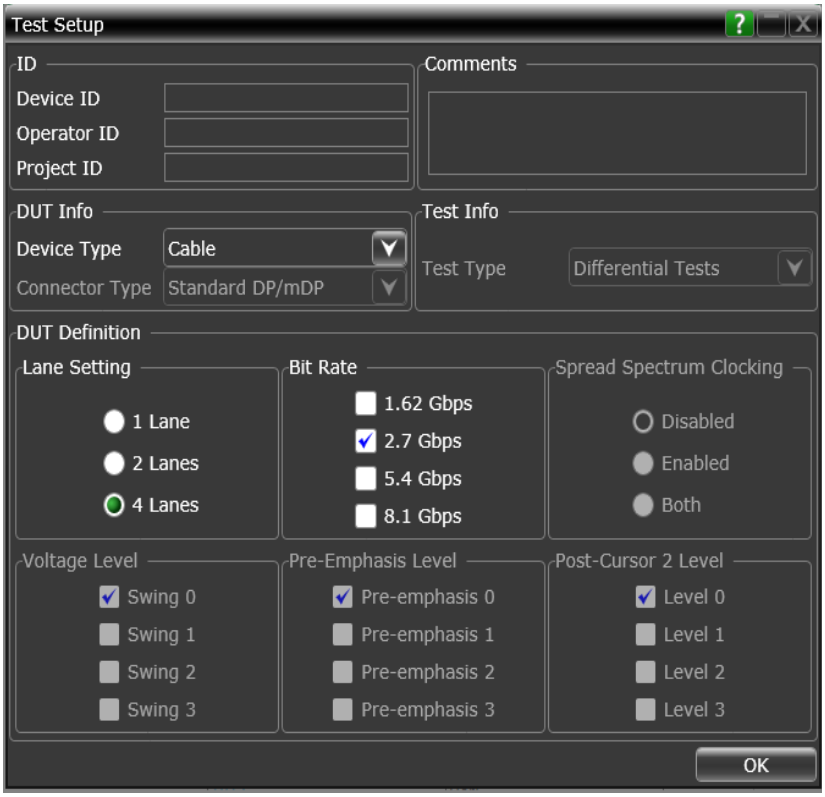
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

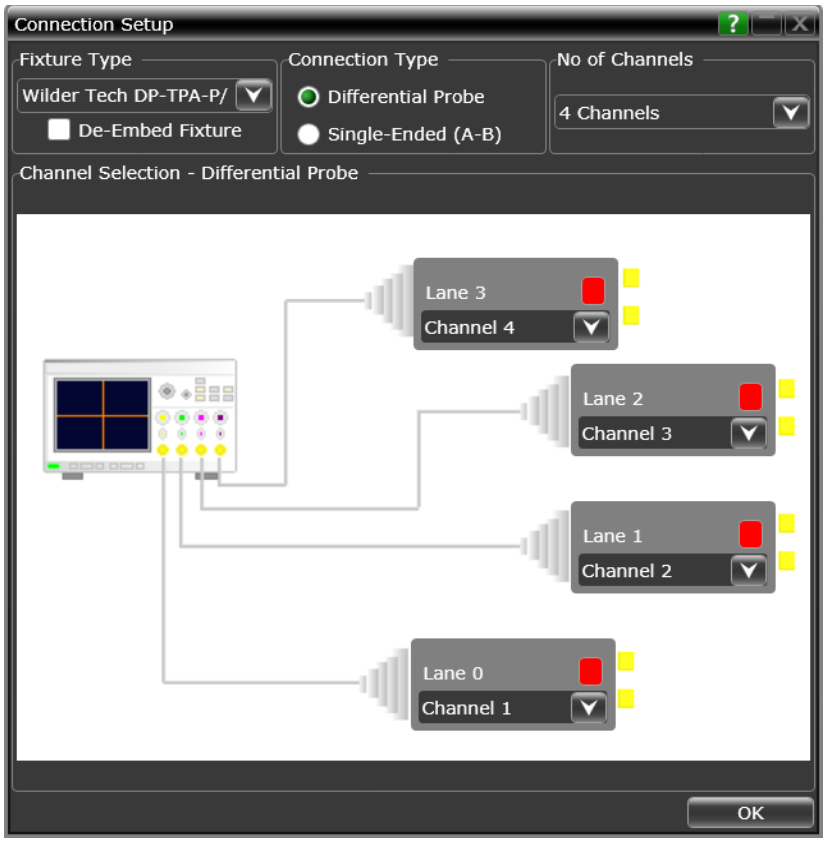
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

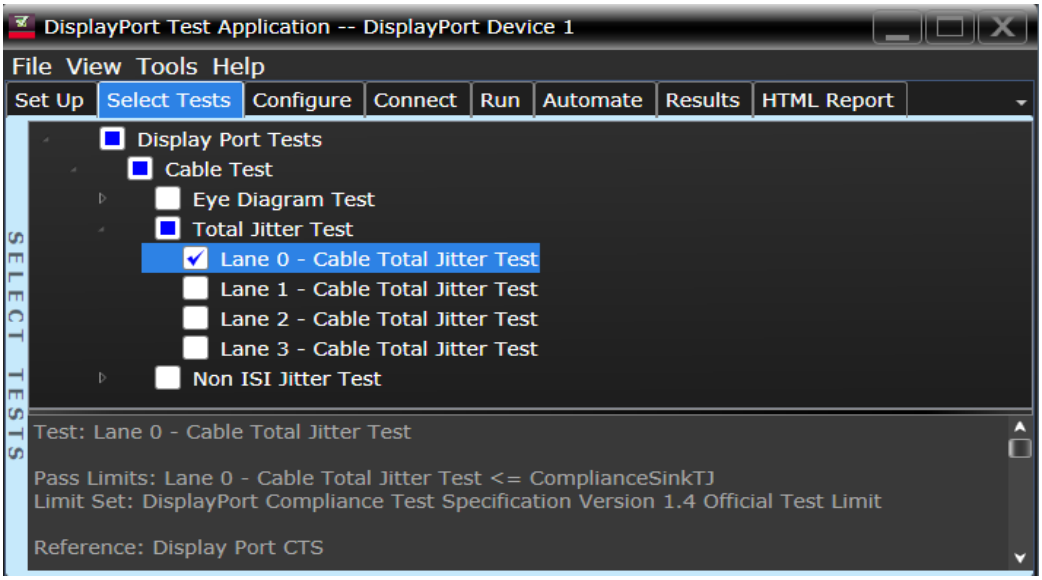
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 134


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 136 Total Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Cable Non-ISI Jitter Test

Test ID

12240001, 12240002, 12240003, 12240004 – Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

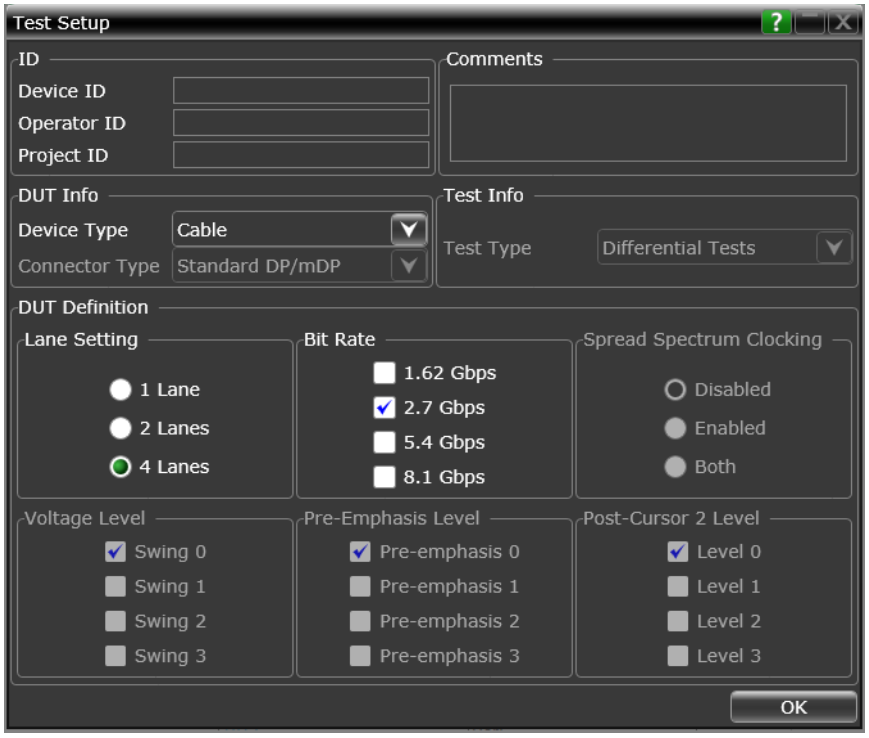
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

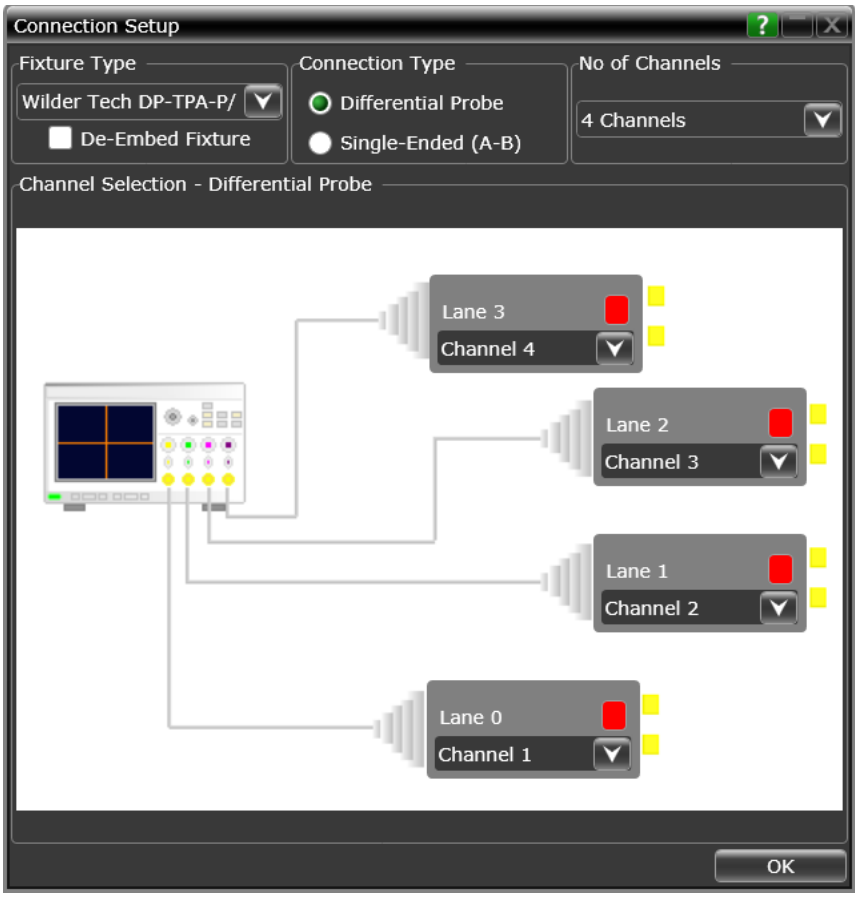
Calculate Non-ISI Jitter using the following equation:

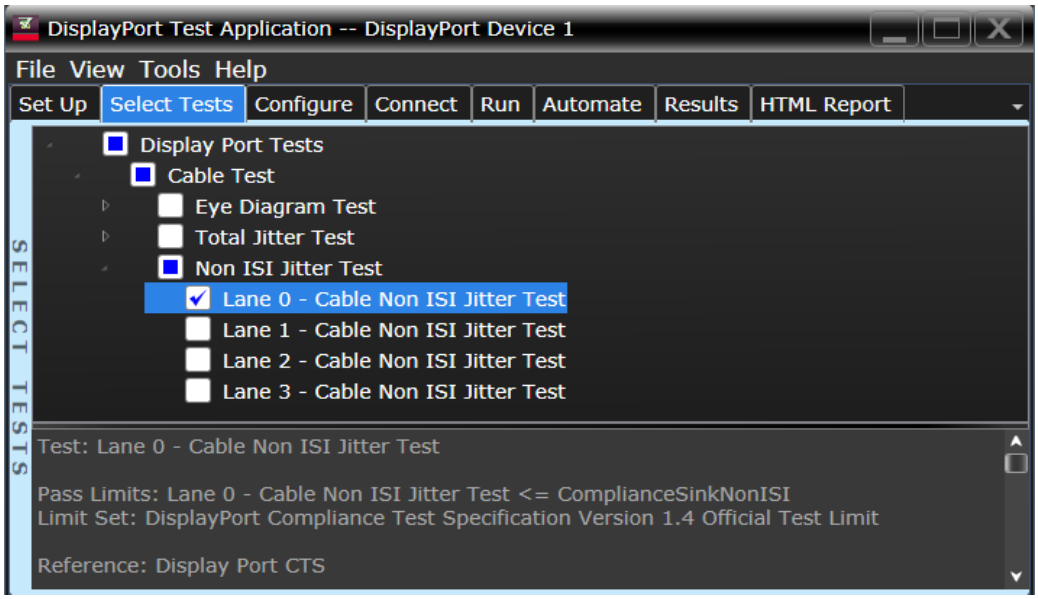
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 134


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 137 Non ISI Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non-ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

17 DisplayPort 1.4 AUX Channel Tests

Overview

This section describes the normative and informative AUX Channel physical layer tests and inrush tests for compliance verification of DisplayPort1.4 source and sink.

Test Point for AUX Channel Tests

You must test the Source devices at Test Point 2 (TP2) while the Sink devices must be tested at Test Point 3 (TP3). See Figure 119.

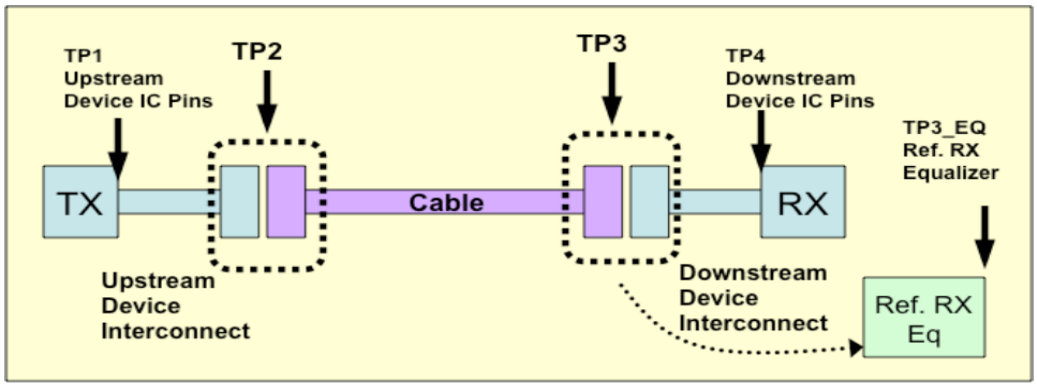


Figure 119 Test Points for DisplayPort 1.4 AUX Channel Tests

Table 138 defines the test point fixtures and instruments used for DisplayPort 1.4 AUX Channel Tests:

Table 138 Test Point Fixtures and Instruments for DisplayPort 1.4 AUX Channel Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-P* ▪ W2641B DisplayPort Test Point Access Adapter For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-P* ▪ Luxshare ICT mDP Plug (mDP-TPA-P)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope
Stimulus	Stimulus must be applied to the DUT to cause AUX Channel transactions to occur. This stimulus shall not be included in or affect the measurements. Reference Sink needed as stimulus for the Source DUT: ▪ Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Reference Source needed as stimulus for the Sink DUT: ▪ Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.4 AUX Channel Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort 1.4 Standards, select the option **1.4** in the **Test Specification** area.

5 Select the option **AUX PHY and Inrush Tests** in the **Test Selection** area.

6 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

7 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

8 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

9 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

10 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

11 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

12 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

13 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Settings for AUX PHY and Inrush Tests

Perform the following steps before you run the Auxiliary Channel and Inrush tests on the source or sink device:

1 Click the **Test Setup** button on the **Set Up** tab to set up for Auxiliary Channel and Inrush tests.

2 On the **Test Setup** window,

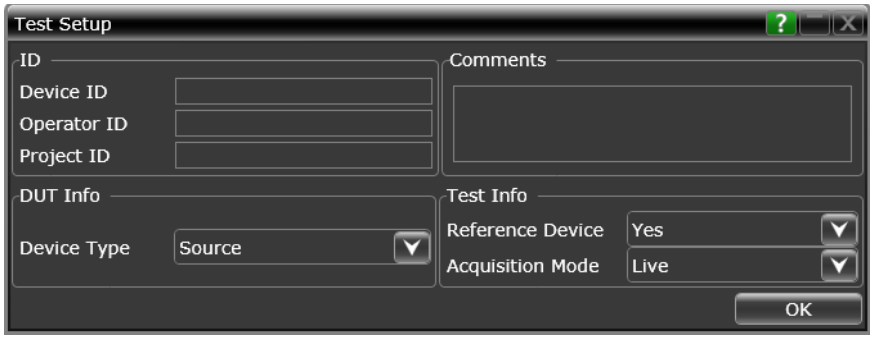
a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b From the **Device Type** drop-down options, select either **Source** or **Sink**.

c From the **Reference Device** drop-down options, select **Yes** if a reference sink/source is attached to device under test during testing.

d From the **Acquisition Mode** drop-down options, select **Live** if waveform acquisition and analysis will be performed on an online Infiniium Oscilloscope, else select **Offline**.

3 Click **OK** to exit the **Test Setup** window.

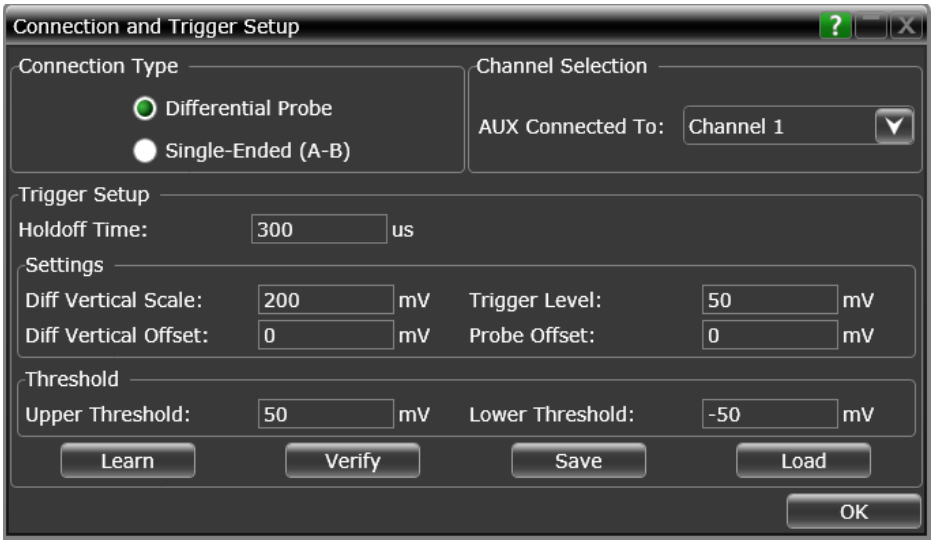


4 Click the **Connection Setup** button that now appears on the **Set Up** tab.

5 On the **Connection and Trigger Setup** window,

a Select either **Differential Probe** or **Single-Ended (A-B)** in the **Connection Type** area, depending on the probe connection you are using.

b From the **AUX Connected To:** drop-down options of the **Channel Selection** area, select the Oscilloscope Channel where the Auxiliary Lane is connected to.



c In the **Trigger Setup** area, define the Oscilloscope parameters to trigger on an Auxiliary signal during testing.

- **Hold Off Time** – The oscilloscope minimum hold off time before triggering the next waveform. Note that any Auxiliary transaction from the source must receive a reply from the sink in 400 us, else such a transaction is considered a timeout. Hold off time, in such cases, represents the minimum idle time before each Aux transaction is initialized. It is defaulted to 300 us which is a safe timing value for most devices tested in the lab. Most devices respond much faster than 300 us.
- **Trigger Level** – The AUX Channel signal level on which to trigger. Note that for a bi-directional signal (where a reference sink is attached), you must set the trigger level such that it crosses both the source command and the sink reply signal. Figure shows correct and incorrect trigger levels.

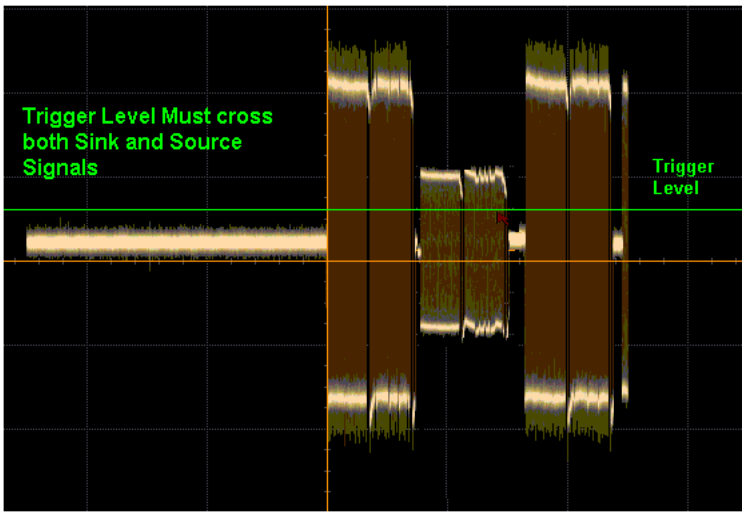


Figure 120 Correct Trigger Level

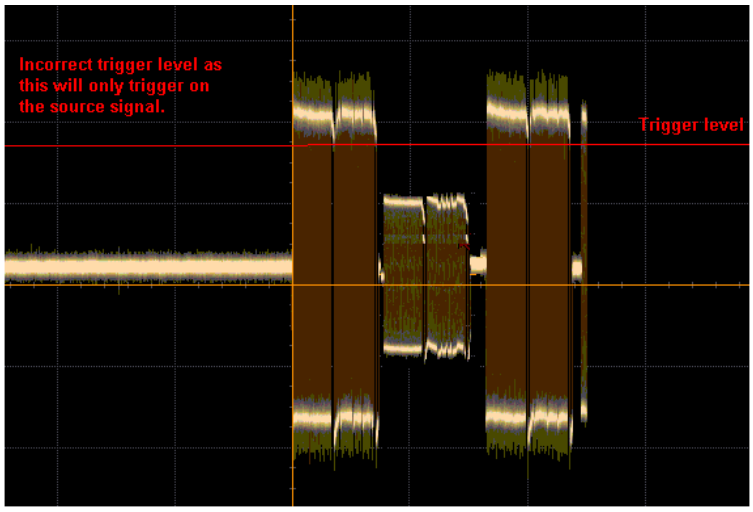


Figure 121 Incorrect Trigger Level

- **Vertical Scale** – The oscilloscope vertical scale. Set the vertical to make sure that all signals are visible on the oscilloscope display.
- **Offset** – Set the offset so that the center point is aligned with the center of the oscilloscope display.
- **Upper Threshold/Lower Threshold** – The threshold level of signal must be set properly so that both upper and lower thresholds cross both the source and sink signals when the DUT is attached with a reference sink. The threshold levels are important parameters because they are used for edge detection when decoding a source command from a sink reply.

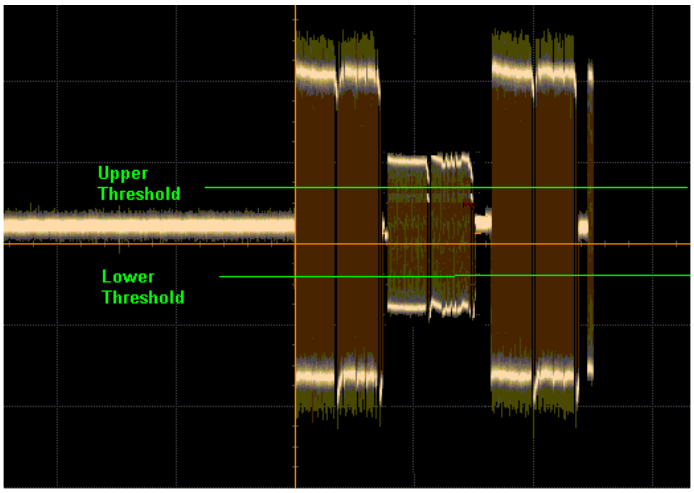
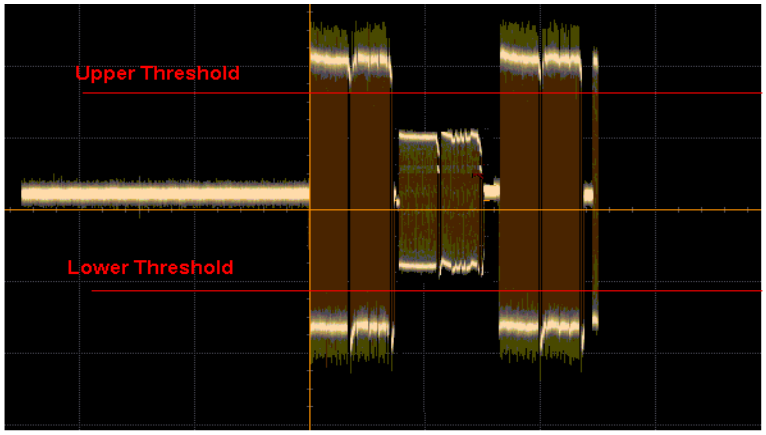


Figure 122 Correct Threshold set



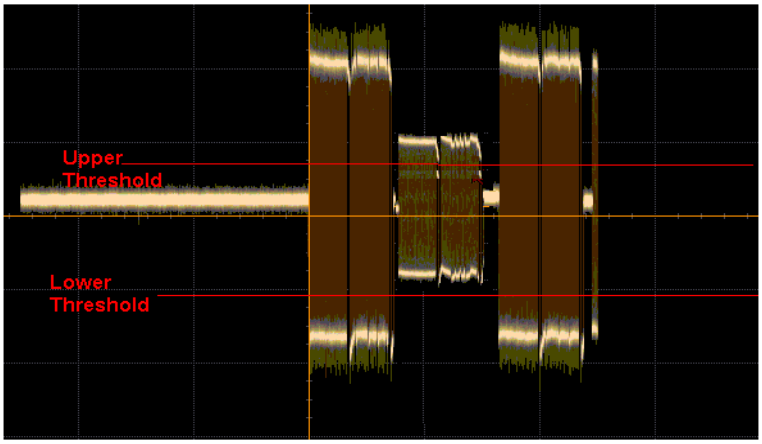


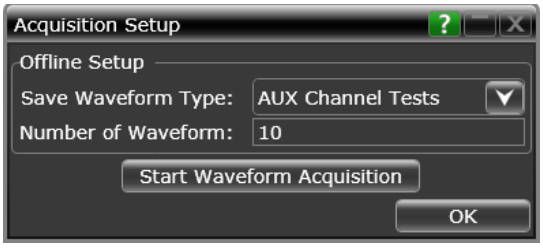
Figure 123 Wrong Thresholds set

- Click the **Learn** button to access the information guide about the trigger setup parameters. However, note that the learning guide may not necessarily work due to variation in the actual Auxiliary signals, owing to different manufacturers. Keysight recommends that you must check to make sure that the parameters are correctly set as previously described.
- Click **Verify** and follow the instructions, if you wish to check the AUX Channel trigger.
- You may **Save** or **Load** the trigger setup configuration as a **.tsf* file.

6 Click **OK** to exit the **Connection and Trigger Setup** window.

7 If you select the option **Offline** for the **Acquisition Mode** in the **Test Setup** window, the **Acquisition Setup** button appears in the **Test Environment Setup** area of the **Set Up** tab.

8 Click the **Acquisition Setup** button to save the waveform files so that you can avoid the manual process to initiate Auxiliary transactions during the time of test runs.



9 On the **Acquisition Setup** window,

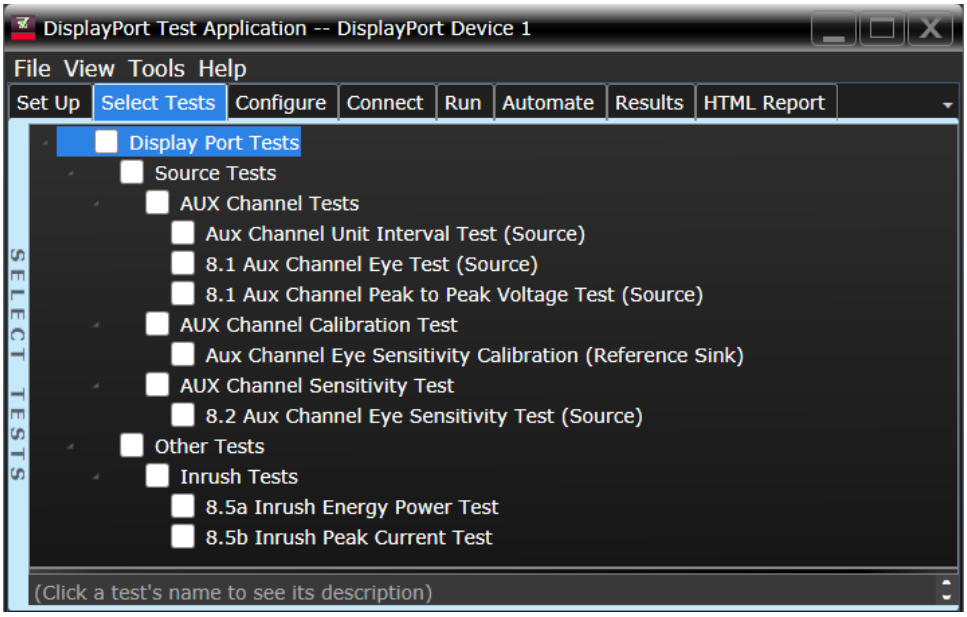
a select the type of waveforms to be saved from the **Save Waveform Type:** drop-down options.

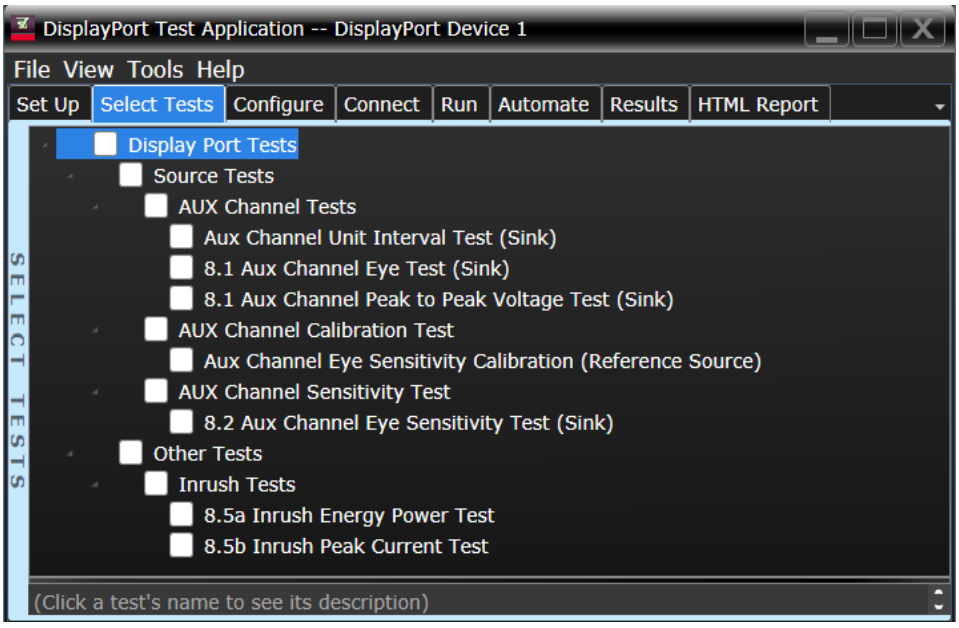
b define the number of waveforms to be saved in the **Number of Waveform:** field.

c Click the **Start Waveform Acquisition** button to start capturing and saving waveforms.

d Click **OK** to return to the **Set Up** tab.

10 Click the **Select Tests** tab where the AUX Channel tests for Source or Sink devices appear.


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Display Port Tests
Source Tests
AUX Channel Tests
Aux Channel Unit Interval Test (Source)
8.1 Aux Channel Eye Test (Source)
8.1 Aux Channel Peak to Peak Voltage Test (Source)
AUX Channel Calibration Test
Aux Channel Eye Sensitivity Calibration (Reference Sink)
AUX Channel Sensitivity Test
8.2 Aux Channel Eye Sensitivity Test (Source)
Other Tests
Inrush Tests
8.5a Inrush Energy Power Test
8.5b Inrush Peak Current Test
(Click a test's name to see its description)


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Display Port Tests
Source Tests
AUX Channel Tests
Aux Channel Unit Interval Test (Sink)
8.1 Aux Channel Eye Test (Sink)
8.1 Aux Channel Peak to Peak Voltage Test (Sink)
AUX Channel Calibration Test
Aux Channel Eye Sensitivity Calibration (Reference Source)
AUX Channel Sensitivity Test
8.2 Aux Channel Eye Sensitivity Test (Sink)
Other Tests
Inrush Tests
8.5a Inrush Energy Power Test
8.5b Inrush Peak Current Test
(Click a test's name to see its description)

Probing/Connection Set Up for AUX Channel Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests. When performing the Source AUX Channel tests, a Reference Sink device is required. Similarly, when performing the Sink AUX Channel tests, a Reference Source device is required.

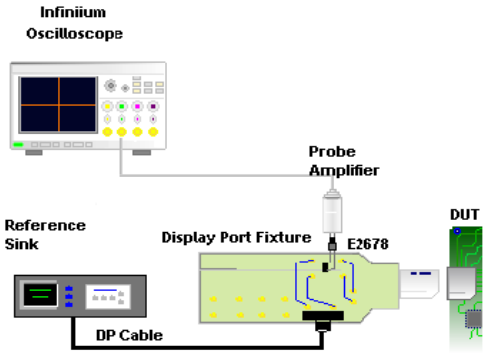


Figure 124 Sample connection diagram for source AUX channel tests with source DUT connected to a reference sink

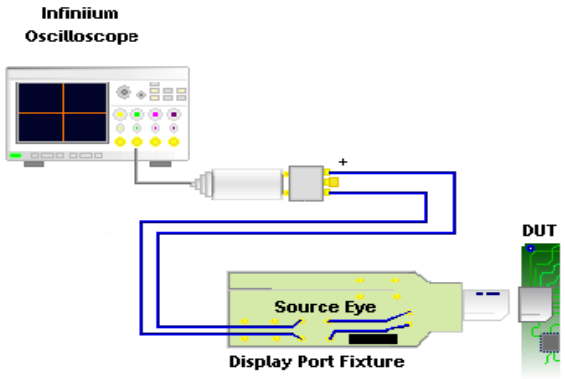


Figure 125 Sample connection diagram for source AUX channel tests without connecting to a reference sink

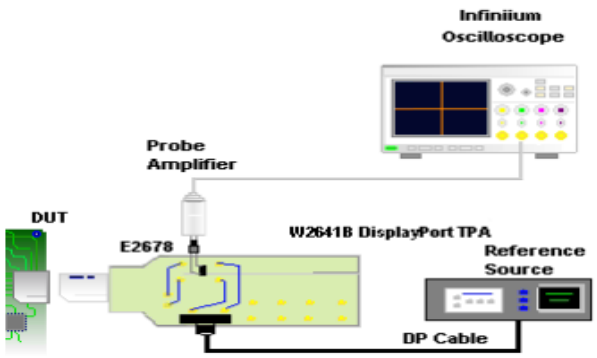


Figure 126 Sample connection diagram for sink AUX channel tests with sink DUT connected to a reference source

AUX Channel Unit Interval Test

Test ID

125000 – AUX Channel Unit Interval Test (Source)

125010 – AUX Channel Unit Interval Test (Sink)

Test Overview

The objective of the test is to evaluate the AUX Channel waveform, ensuring that the overall variation of the Manchester transaction Unit Interval stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1. Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.
2. Generate FUNC1 signal, which is the differential signal of the AUX Channel.
3. Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).
4. Set up the parameter of the measurement:
   - *a* Enable measurement of all edges to obtain a statistical value of the measurement.
   - *b* Set up the measurement threshold.
   - *c* Set up the Clock Recovery.
5. Set up the parameter of the measurement trend:
   - *a* Set up the Unit Interval measurement for the differential AUX Channel signal.
   - *b* Set up the frequency measurement for the Clock signal.
   - *c* Set up the measurement trend.
6. Set up the waveform Histogram on the measurement trend:
   - *a* Initialize AUX Channel transactions and acquire the differential AUX Channel signal.
   - *b* Identify the first and the last points for the desired transaction.
   - *c* Zoom-in on the desired transaction.
   - *d* Set up the Vertical Waveform Histogram on the measurement trend within the desired transaction.
   - *e* Obtain the measurement for the mean, maximum and minimum values of the waveform Histogram.
7. Repeat step 6 ten times.
8. Report the measurement results.

PASS Condition

Manchester Transaction Unit Interval (UI_{MAN}):

Minimum = 0.4 µsec

Maximum = 0.6 µsec

Test References

See:

- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.4.2, Table 3-4*

Expected/Observable Results

The measured unit interval for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Test

Test ID

125001 – AUX Channel Eye Test (Source)

125011 – AUX Channel Eye Test (Sink)

Test Overview

The objective of this test is to evaluate the transmitter AUX Channel waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

7 Set up the waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

8 Set up the parameters for the Mask Test.

   a Load the eye mask based on the settings in the Configuration Variable.

   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

   c Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.

9 Check for any signal trajectories entering into the mask.

10 Report the measurement results.

PASS Condition

PASS Value = 290mV_diff_pp or higher

FAIL Value = lower than 290mV_diff_pp

Table 139 Eye Mask Vertices for AUX Channel for Manchester Transactions

Mask Point	Time (from EYE Center)	Minimum Voltage Value at Six Vertices (mV)
1	-185ns	0
2	-135ns	145
3	135ns	145
4	185ns	0
5	135ns	-145
6	-135ns	-145

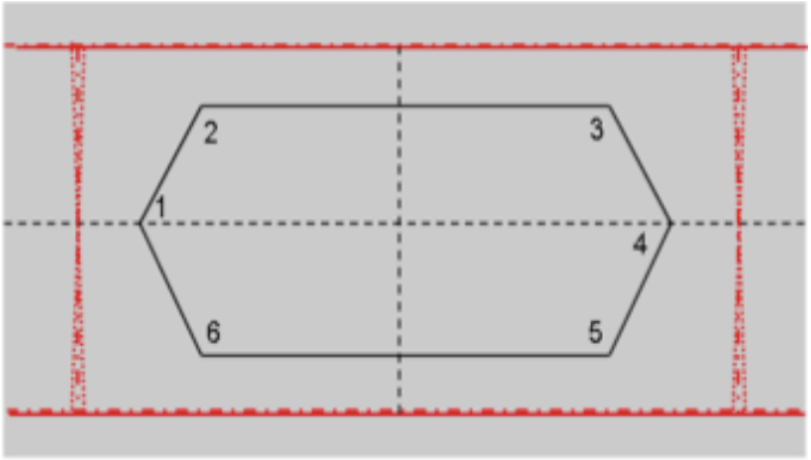


Figure 127 AUX Channel EYE Mask for Manchester Transactions

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.4.2.5, Figure 3-18 and Table 3-5*

Expected/Observable Results

The measured eye diagram for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

AUX Channel Peak-to-Peak Voltage Test

Test ID

125002 – AUX Channel Peak-to-Peak Voltage Test (Source)

125012 – AUX Channel Peak-to-Peak Voltage Test (Sink)

Test Overview

The objective of the test is to evaluate the transmitter AUX Channel Waveform, ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

a Enable measurement of all edges to obtain a statistical value of the measurement.

b Set up the measurement threshold.

c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

7 Set up the horizontal waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

8 If you have selected the “AUX Channel Eye Test” under the **Select Tests** tab of the compliance application:

a Set up the parameter of the Mask Test:

i Load the eye mask based on the settings in the Configuration Variable.

ii Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

iii Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.

b Check for any signal trajectories entering into the mask.

9 Report the measurement results.

PASS Condition

Table 140 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage at a transmitting device ($V_{AUX\text{-}DIFFp\text{-}p}$)	0.29V	1.38V

Test References

See:

- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.4.2, Table 3-4*

Expected/Observable Results

The measured peak-to-peak voltage for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Calibration Test

Test ID

125021 – AUX Channel Eye Sensitivity Calibration (Reference Sink)

125031 – AUX Channel Eye Sensitivity Calibration (Reference Source)

Test Overview

The objective of this test is to calibrate the peak-to-peak voltage of the transmitter AUX Channel waveform by reference device (reference source or reference sink), ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.

2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

4 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

5 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

6 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

7 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

8 Set up the waveform Histogram on the AUX Channel eye diagram:

   a Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.

   b Set up the vertical waveform Histogram of width 0.6 UI at the center of the AUX Channel eye diagram.

   c Measure the V_{TOP} and V_{BASE} using the waveform Histogram mean value.

9 Repeat Step 8 three times.

10 Report the measurement results.

PASS Condition

Table 141 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage for AUX Channel Eye Sensitivity	0.24V	0.28V

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.4.2, Table 3-4*

Expected/Observable Results

The measured peak-to-peak voltage for the AUX Channel signal by reference device (reference source or reference sink) shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Test

Test ID

125041 – AUX Channel Eye Sensitivity Test (Source)

125051 – AUX Channel Eye Sensitivity Test (Sink)

Test Overview

The objective of the test is to evaluate the sensitivity to the AUX Channel Eye Opening of the DUT as per the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.
2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.
3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery.
5 Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.
6 Check if the reference device could detect the transaction or not.
7 Decode the AUX Channel signal and check whether the transaction passed or failed.
8 Report the measurement results.

PASS Condition

Determine whether the AUX Channel communication is successful. For example, the Transmitter DUT sends an AUX Request to the Reference Receiver. The Reference Receiver acknowledges and the Transmitter DUT responds to the to indicate that the acknowledgment was successfully received.

PASS = No errors observed in the response

FAIL = One or more errors observed

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.4.2, Table 3-4*

Expected/Observable Results

The measured AUX Channel transaction shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

18 DisplayPort 1.4 Inrush Tests

Overview

This section describes the normative and informative inrush tests for compliance verification of DisplayPort1.4 source and sink (a power consumer).

Test Point

The test fixture for inrush tests implements the schematic shown in Figure 128.

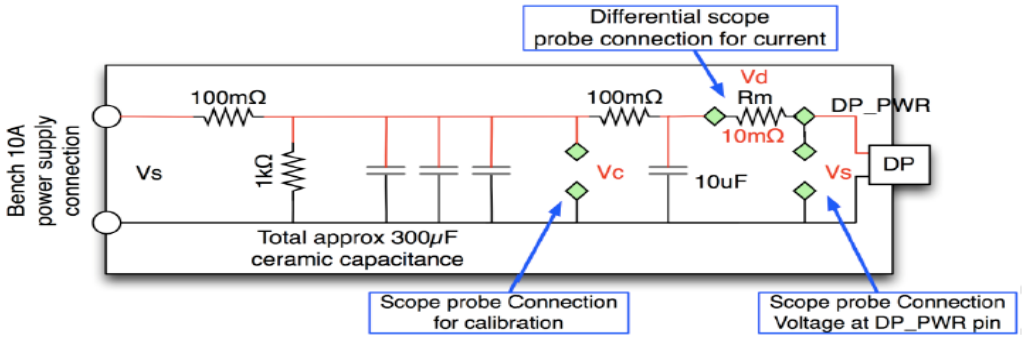


Figure 128 Schematics for testing a Power Consumer Device

The test fixture must be designed and used according to the following guidelines:

- A high gate voltage FET on the DP_PWR line is recommended to allow a fast connect capability, which allows a single connection event for testing. Without such an arrangement, multiple connections will be required to obtain a reasonable “worst-case” attachment event.
- Connection length between the power supply and the test fixture must be minimized. A maximum of four inches is recommended.
- The power supply must have enough outrush capability as to not negatively affect the test fixture’s outrush capability.
- The power supply must be run at 3.6V (3.3V + 10%) read across V_C.

Any Power Consumer test fixture must be calibrated using the Power User test fixture, as shown in Figure 128. Testing with the two fixtures combined should result in the approximate values given below. If required, the component values on the Power Consumer test fixture should be adjusted to match the expected results.

- V_C steady before connection = 3.6V
- V_C droop = ~3.1V
- Inrush Current = ~13.0A

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.4 Inrush Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort 1.4 Standards, select the option **1.4** in the **Test Specification** area.
5. Select the option **AUX PHY and Inrush Tests** in the **Test Selection** area.
6. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
7. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
8. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
9. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
10. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
11. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
12. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
13. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Refer to "Settings for AUX PHY and Inrush Tests" on page 389 for instructions on setting the DisplayPort 1.4 InRush tests.

Inrush Energy Power Test

Test ID

127000 – Inrush Energy Power Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush energy power measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Energy $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 13.5$ Amps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.5*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.2.3*

Expected/Observable Results

The measured worst case inrush energy power for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Inrush Peak Current Test

Test ID

127001 – Inrush Peak Current Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush peak current measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Energy $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 13.5$ Amps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.5*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.2.3*

Expected/Observable Results

The measured worst case inrush peak current for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

19 DPoC 1.4a Source Tests

Overview

The specifications and the conceptual information for the DPoC 1.4a standards are aligned with the DisplayPort 1.4a standards. For more information, refer to "Overview" on page 250.

Setting Up the DisplayPort Compliance Test Application for DPoC 1.4a Source Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort Standards with Type-C capability, select the option **DPoC 1.4a** in the **Test Specification** area.
5. The option **Physical Layer Tests** appears by default in the **Test Selection** area.
6. Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.
7. In the **Type-C Environment Setup** area, select **Enable Type-C Controller** to activate the **DUT Orientation** field and the **Setup Type-C Controller** button. To know about how to configure the Type-C Controller, refer to the *Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help*.
8. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
9. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
10. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
11. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
12. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
13. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
14. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
15. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DPoC 1.4a Source Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

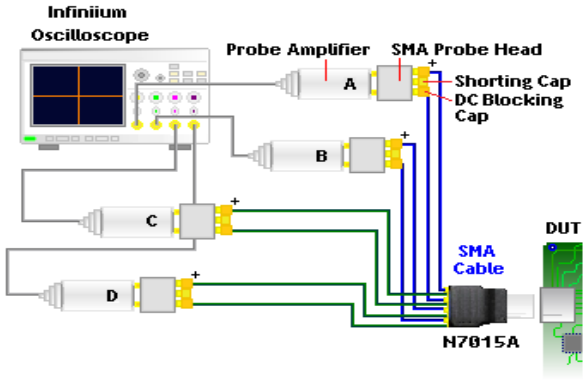


Figure 129 Sample connection diagram for DPoC 1.4a Source Differential Tests

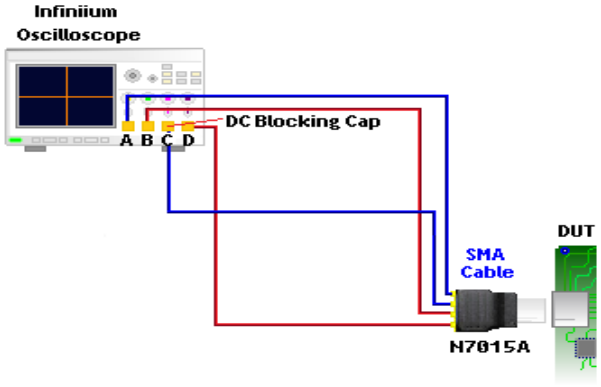


Figure 130 Sample connection diagram for DPoC 1.4a Source Single-Ended Tests

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Source tests (either differential or single-ended) to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1 In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.

2 On the **Test Setup** window,

a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b In the **DUT Info** area, the **Device Type** is selected as **Source** by default. The **Connector Type** is grayed out. From the drop-down options for **Alt Mode**, select either **Alt Mode: DP 4 Lanes** or **Alt Mode: DP 2 + 2**.

c In the **Test Info** area, the **Test Type** is selected as **Differential Tests** by default. Select **Single-Ended Tests** from the drop-down options for the respective tests to appear in the **Select Tests** tab. From the **Data Pattern** drop-down options, select **Standard DP Pattern** or **Arbitrary Pattern**, based on the type of pattern generated.

d In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.

e In the **Power Profile** area, select the **Provider Power Profile** or **Consumer Power Profile** or both options, to include the Voltage and Current specifications to be tested. The appearance of the options depends on the power profiles supported by the DUT.

3 Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1 Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.

2 On the **Connection Setup** window,

a Select the appropriate option (**Keysight N7015A** or **Other**) in the **Fixture Type** to indicate where the DUT is connected to.

b Select either **Without Cable** or **With Cable** to indicate the type of the connected **N7015A** fixture.

c Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.

d In the **Channel Selection** area, assign appropriate channels to lanes.

3 Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of source tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for DPoC 1.4a Source Tests" on page 668 to complete the task flow for DUT setup along with configuring the Compliance Application to run each test.

Source Eye Diagram Test

Test ID

For Standard DP Pattern:

- 1210001, 1210002, 1210003, 1210004 – Eye Diagram Test

For Arbitrary Pattern:

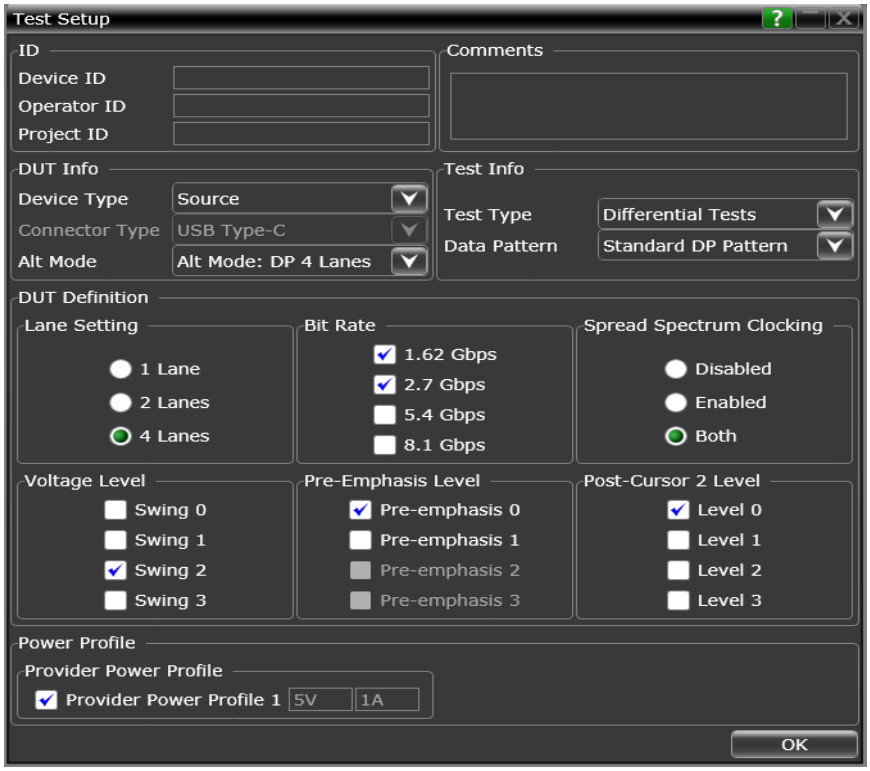
- 1310001, 1310002, 1310003, 1310004 – Eye Diagram Test

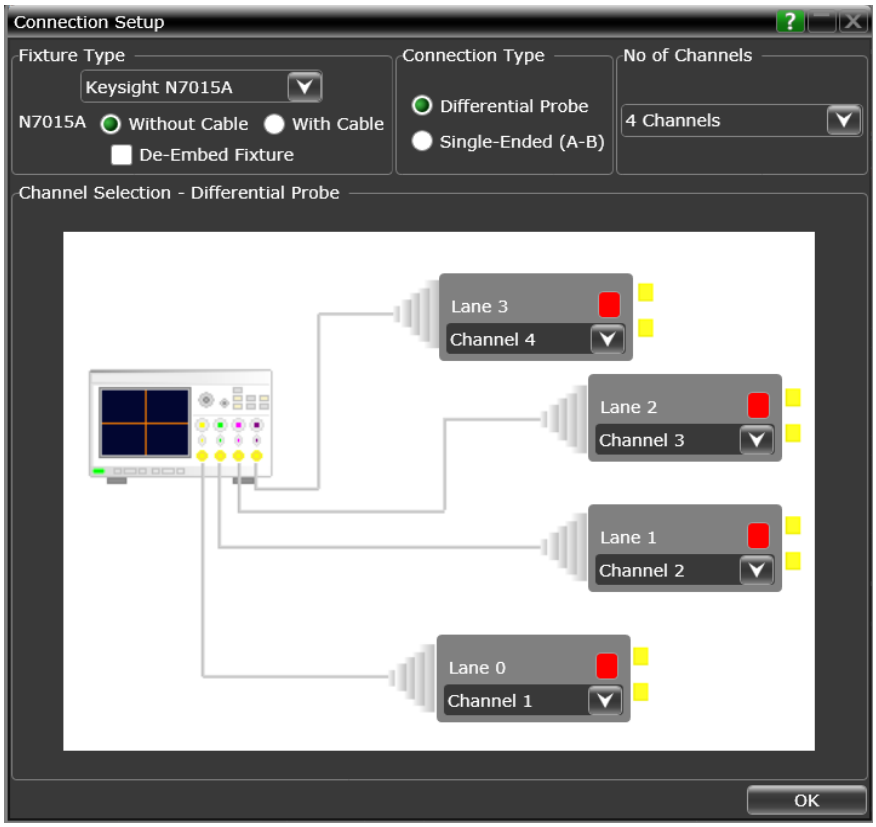
Test Overview

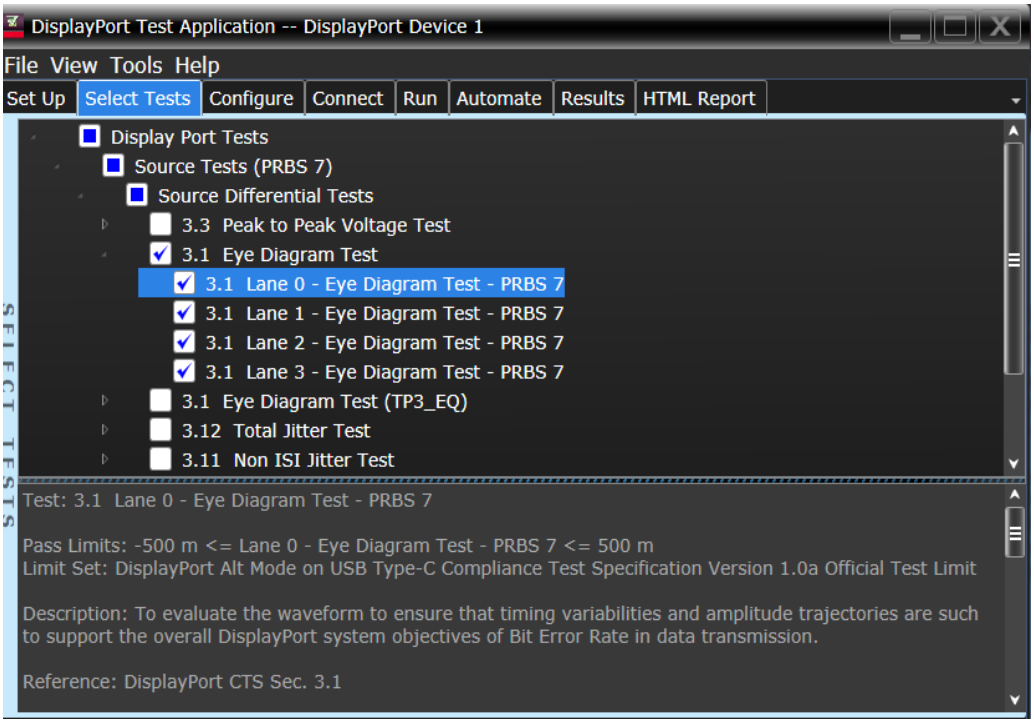
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Swing 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Measure V_{TOP} and V_{BASE} of the input signal using the pattern folding.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the input signal eye diagram to measure the left edge.
7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the eye height of the eye diagram using the Histogram.
9 Measure the jitter of the eye diagram using the Histogram.
10 Calculate the eye width based on the measured jitter of the eye diagram.

11 Check for any signal trajectories that may have entered into the mask.

12 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 142 shows the voltage and time coordinates for the mask used in the eye diagram.

Table 142 Eye Diagram Mask Coordinates

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	**High (2.7 Gb/s)**
1	0.127, 0.000	0.210, 0.000
2	0.291, 0.160	0.355, 0.140
3	0.500, 0.200	0.500, 0.175
4	0.709, 0.200	0.645, 0.175
5	0.873, 0.000	0.790, 0.000
6	0.709,-0.200	0.645,-0.175
7	0.500,-0.200	0.500,-0.175
8	0.291,-0.160	0.355,-0.140

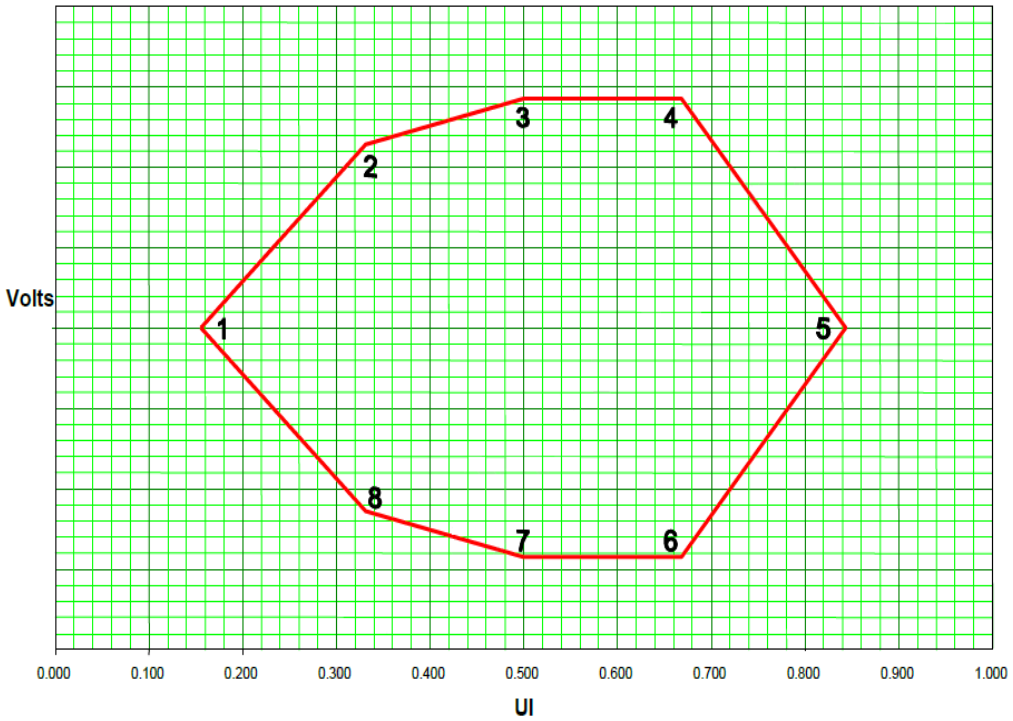


Figure 131 The Source Eye Mask

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.1*
- *VESA DisplayPort Standard Version 1.4a, Section 3.5.2.8.2, Table 3-31 for RBR, Table 3-30 for HBR*

Expected/Observable Results

The measured eye diagram for the source degraded signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test

Test ID

For Standard DP Pattern:

- 1220001, 1220002, 1220003, 1220004 – Total Jitter Test

For Arbitrary Pattern:

- 1320001, 1320002, 1320003, 1320004 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

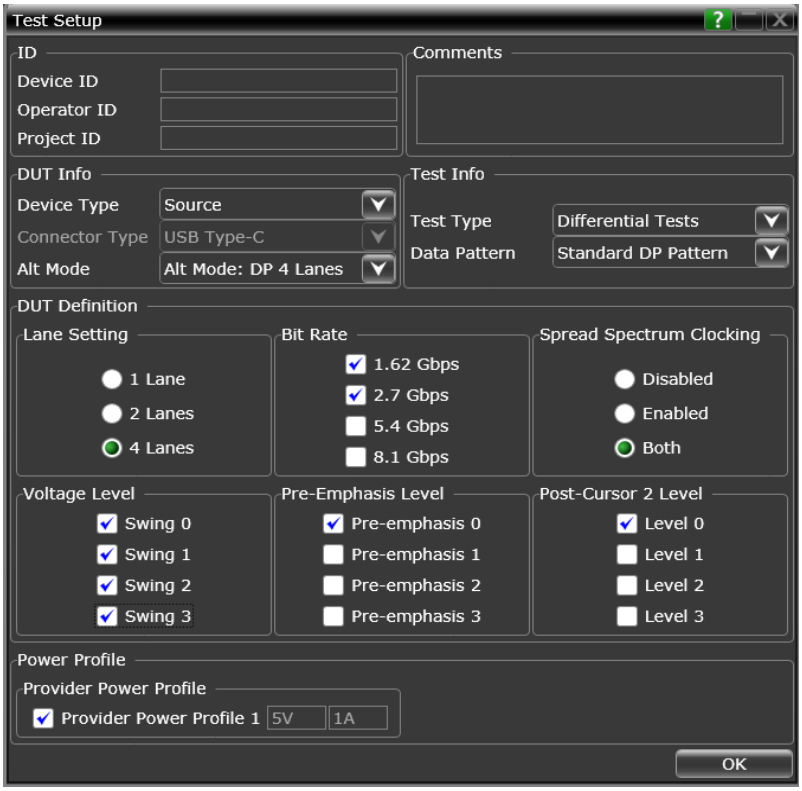
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

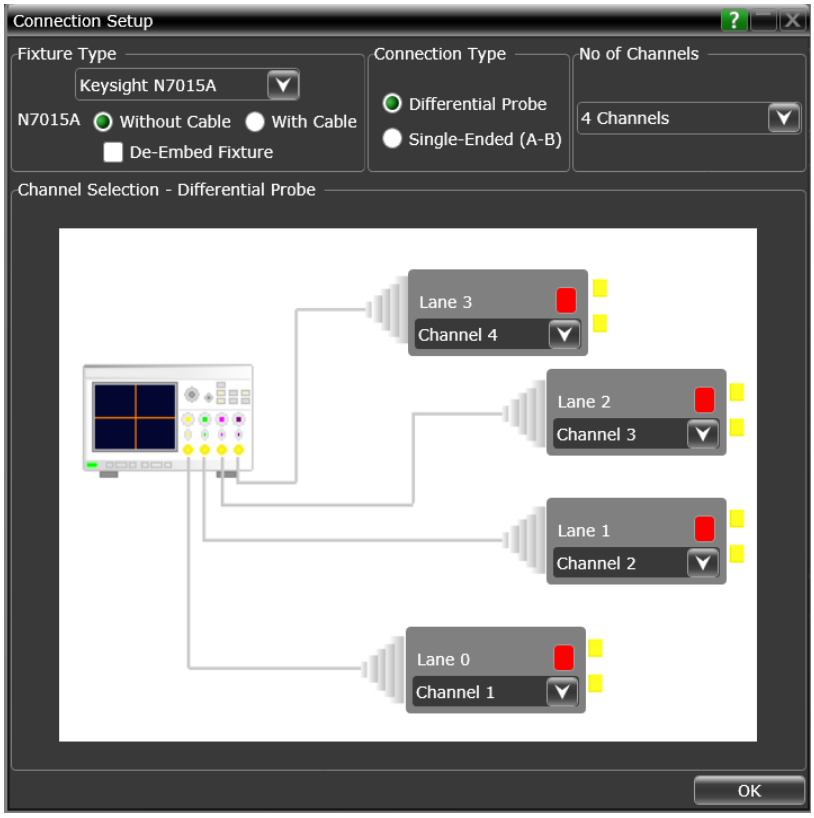
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

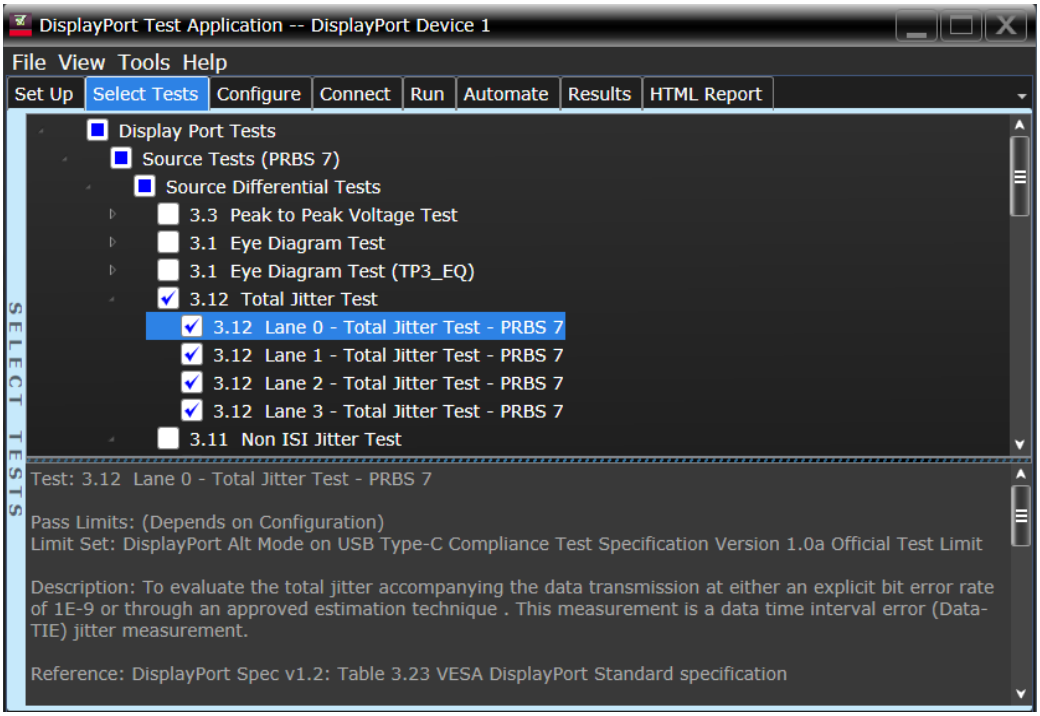
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Report the measurement results.

PASS Condition

Table 143 Total Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
Ap-p	0.294 UI	0.420 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
Ap-p	0.180 UI	0.270 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.1*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2.7.2*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non-ISI Jitter Test

Test ID

For Standard DP Pattern:

- 1230001, 1230002, 1230003, 1230004 – Non ISI Jitter Test - PRBS7
- 1233001, 1233002, 1233003, 1233004 – Non ISI Jitter Test - TPS4

For Arbitrary Pattern:

- 1330001, 1330002, 1330003, 1330004 – Non ISI Jitter Test

Test Overview

The objective of the test is to evaluate the amount of Non ISI jitter accompanying the data transmission.

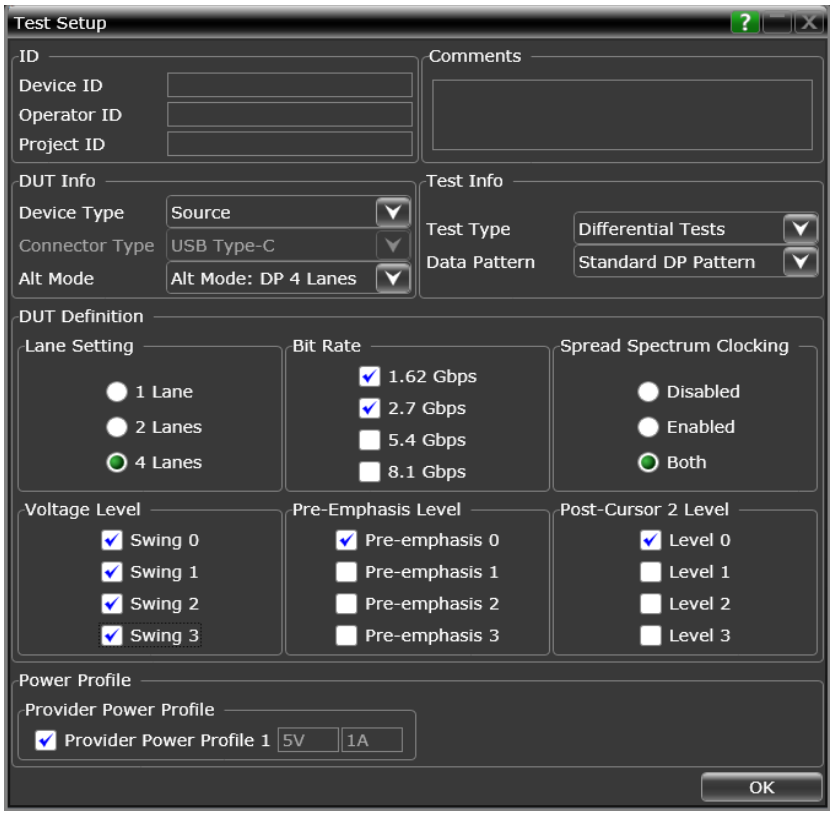
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

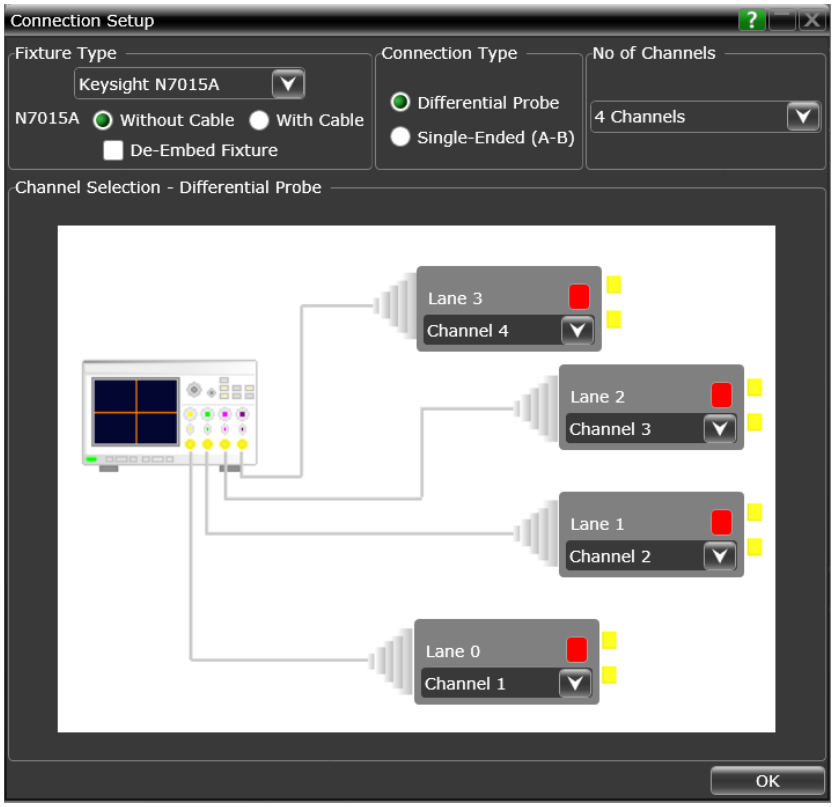
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

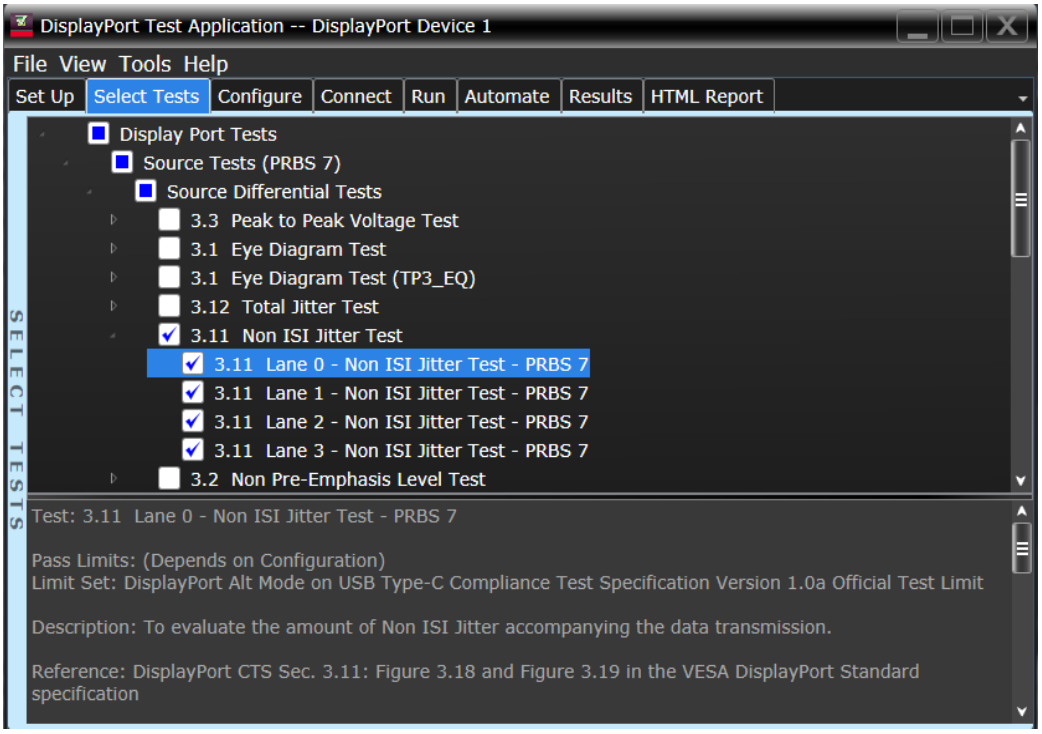
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR, and HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR - PRBS7 HBR3 - TPS4


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Calculate the Non ISI jitter using the following equation:

$$\text{Non ISI Jitter} = \text{TJ} - \text{ISI}$$

7 Report the measurement results.

PASS Condition

Table 144 Non-ISI Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate3 (8.1 Gb/s per lane)		
A_{TXp-p}	0.170 UI	0.230 UI
High-bit Rate (2.7 Gb/s per lane)		
A_{TXp-p}	0.260 UI	0.276 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{TXp-p}	0.160 UI	0.170 (DP 1.4a) 0.210 (PHY CTS 1.2b)

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.9*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2.7.2, Table 3-23*

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Pre-Emphasis Level Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1261001, 1261002, 1261003, 1261004 – Non Pre-Emphasis Level Test (Swing 1/Swing 0)
- 1262001, 1262002, 1262003, 1262004 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263001, 1263002, 1263003, 1263004 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

For Standard DP Pattern (HBR2 and HBR3):

- 1264101, 1264102, 1264103, 1264104 – Non Pre-Emphasis Level Test (Swing 2/Swing 0)
- 1262101, 1262102, 1262103, 1262104 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263101, 1263102, 1263103, 1263104 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

For Arbitrary Pattern:

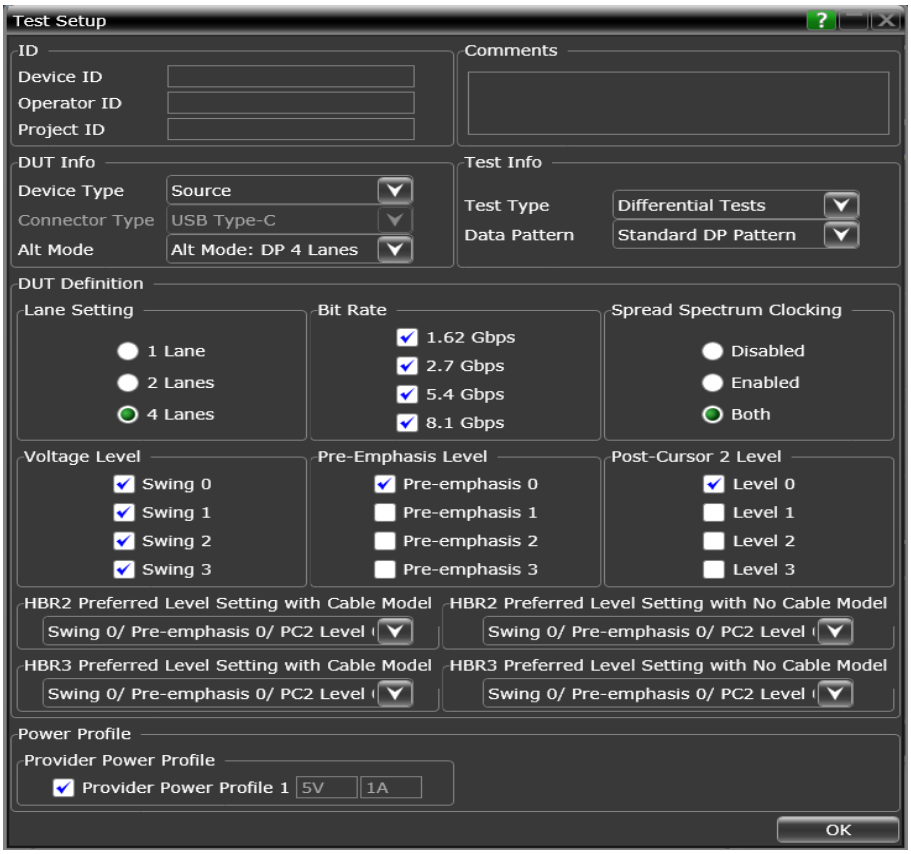
- 1364101, 1364102, 1364103, 1364104 – Non Pre-Emphasis Level Test (Swing 2/Swing 0)
- 1362101, 1362102, 1362103, 1362104 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1363101, 1363102, 1363103, 1363104 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

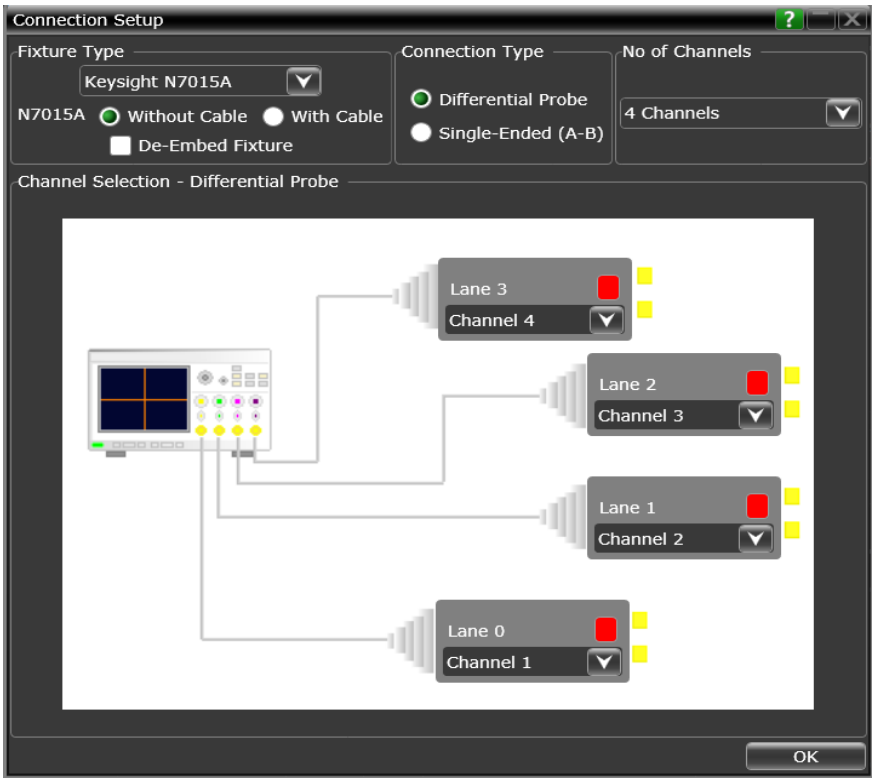
Test Overview

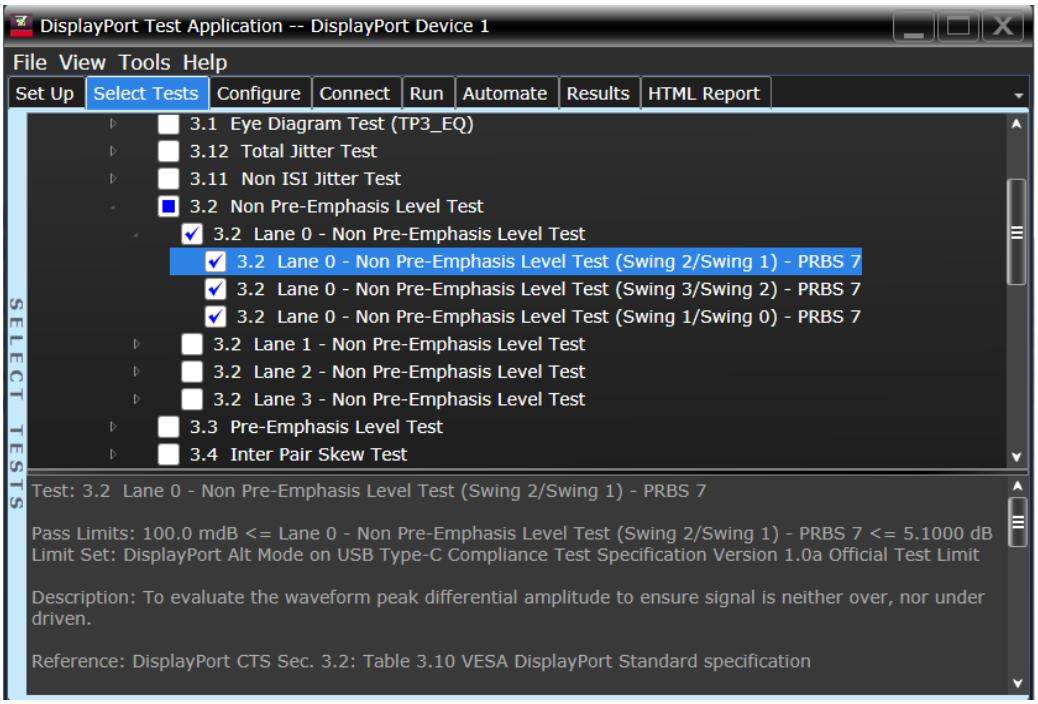
The objective of this test is to ensure that the system budget elements are obeyed and to ensure that the level settings are monotonic so that the sink relies on the source to incrementally increase upon request by the sink.

Test Conditions for Non Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR and HBR
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For Voltage Level A with no pre-emphasis level:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

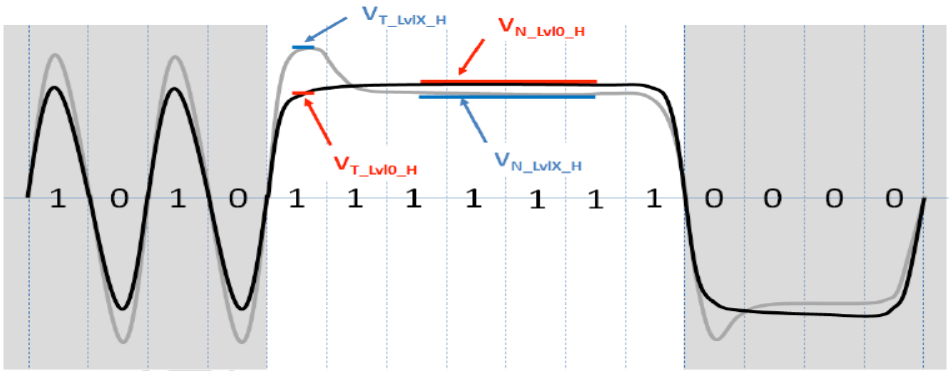


Figure 132 High Voltage measurement for RBR and HBR

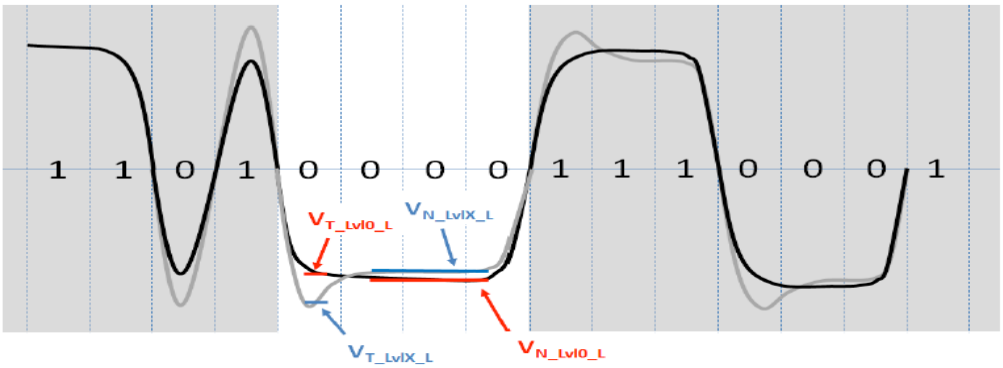


Figure 133 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR3 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted zeros of the pattern.

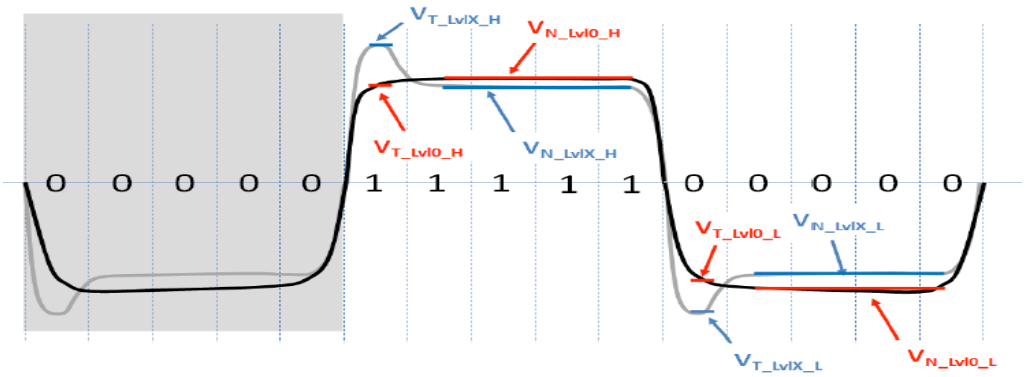


Figure 134 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_Lvl0\_PP} = V_{T\_Lvl0\_H} - V_{T\_Lvl0\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_Lvl0\_PP} = V_{N\_Lvl0\_H} - V_{N\_Lvl0\_L}$$

2 Repeat Step 1 for Voltage Level B with no pre-emphasis level.

3 Calculate the non pre-emphasis level output voltage ratio using the equation:

Non Pre-Emphasis Level = $20 * \text{Log}_{10}[\text{Voltage Level A } V_{N\_Lvl0\_PP} / \text{Voltage Level B } V_{N\_Lvl0\_PP}]$

4 Report the measurement results.

PASS Condition

For each level setting testes, the following equation should be used:

$\text{Resultant} = 20 * \text{Log}_{10}[\text{Voltage}_{\text{Peak-Peak\_LevelA}} / \text{Voltage}_{\text{Peak-Peak\_LevelB}}]$

Table 145 Compared Levels

Measurement#	$\text{Voltage}_{\text{Peak-Peak\_LevelA}}$	$\text{Voltage}_{\text{Peak-Peak\_LevelB}}$
RBR & HBR		
1	Level 1 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)
2	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
3*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)
* if device optionally capable of Level 3		

The resultants specifications are as identified below:

Measurement 1: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 2: 0.1 dB ≤ Resultant ≤ 5.1 dB

Measurement 3: 0.8 dB ≤ Resultant ≤ 6.0 dB

Table 146 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX\text{-}OUTPUT\text{-}RATIO\_RBR\_HBR}$*	Ratio of Output Voltage Level 1/Level 0	0.8	-	6.0	dB	Measured on non-transition bits at Pre-emphasis level 0 setting. Support for Voltage Level 3 is optional.
	Ratio of Output Voltage Level 2/Level 1	0.1	-	5.1	dB	
	Ratio of Output Voltage Level 3/Level 2	0.8	-	6.0	dB	

* Earlier versions of DisplayPort have the Main-Link DPTX output voltage ratios to ensure that the DPTX supports the required range of output voltage levels. For HBR2 and higher, you need not test or specify exclusively because the compliance test point is moved to TP3_EQ. So, the ratio of output voltage levels is removed from the table above for HBR2 and above.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.2*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-22*

Expected/Observable Results

The measured output voltage level ratio of the non pre-emphasis level test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Pre-Emphasis Level Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1270001, 1270002, 1270003, 1270004 – Pre-Emphasis Level Test

For Standard DP Pattern (HBR2 and HBR3):

- 1270501, 1270502, 1270503, 1270504 – Pre-Emphasis Level Test

For Arbitrary Pattern:

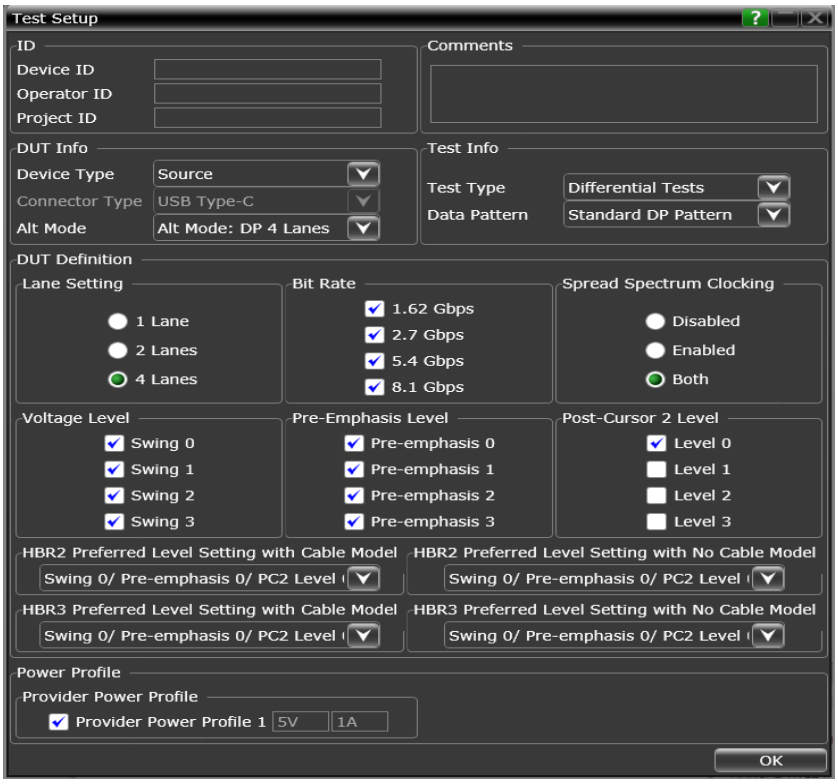
- 1370501, 1370502, 1370503, 1370504 – Pre-Emphasis Level Test

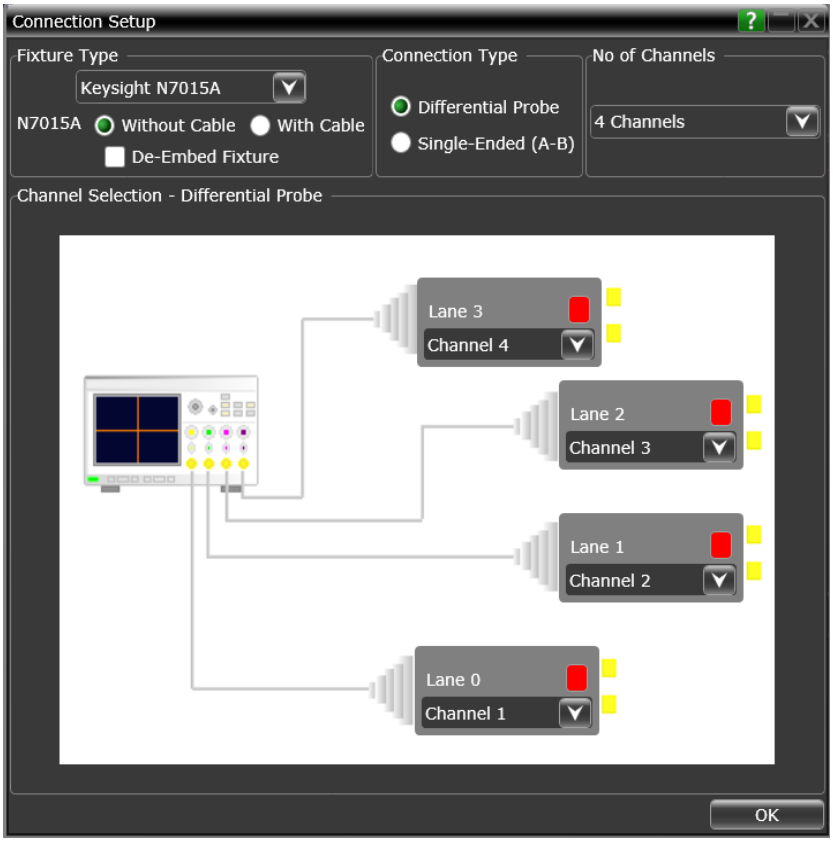
Test Overview

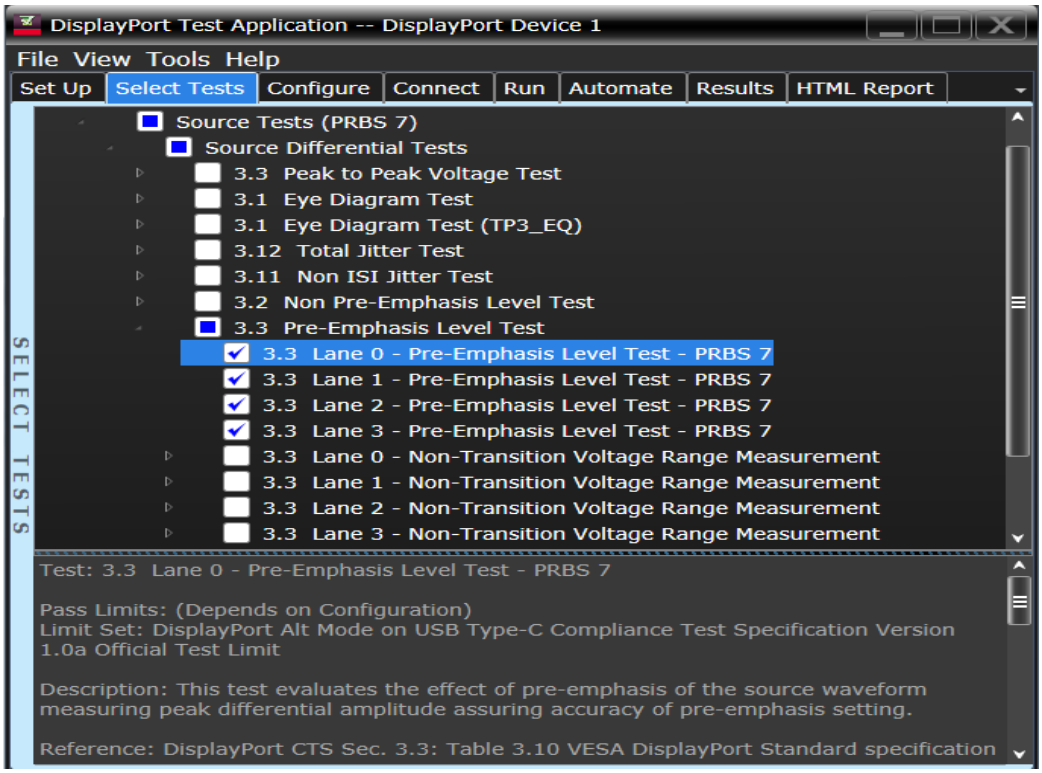
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings.

Test Conditions for Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR and HBR
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.4a Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given Voltage Level and a Pre-Emphasis Level X:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.

- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6th bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4th bit of the four successive transmitted zeros of the pattern.

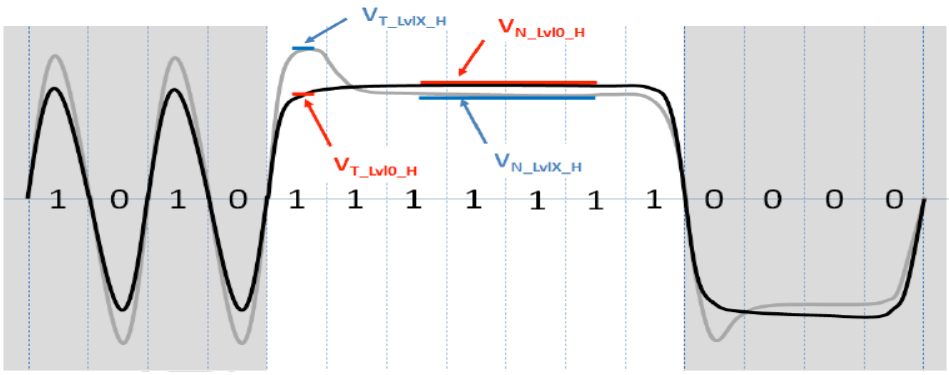


Figure 135 High Voltage measurement for RBR and HBR

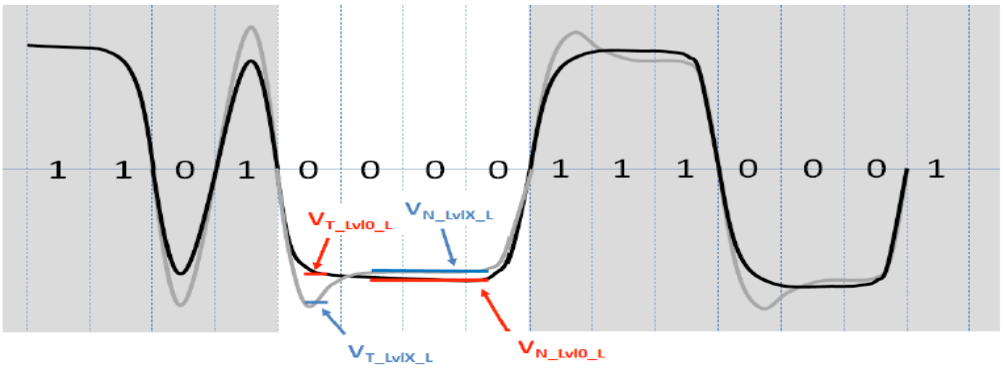


Figure 136 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR3 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

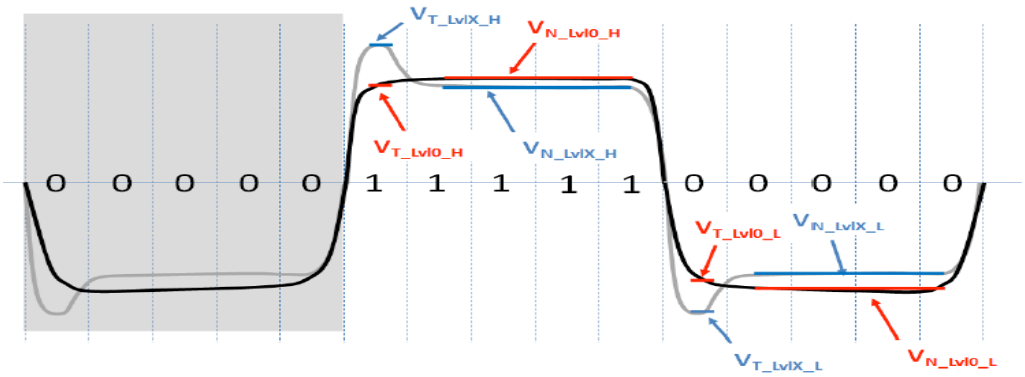


Figure 137 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

l Calculate the pre-emphasis level using the equation:

$$\text{Pre-Emphasis}_{LvlX} = 20 * \text{Log}_{10}[V_{T\_LvlX\_PP} / V_{N\_LvlX\_PP}]$$

2 For Pre-Emphasis Level 0 (no pre-emphasis level), the result for $\text{Pre-Emphasis}_{Lvl0}$ is compared with the maximum pre-emphasis disabled limit.

3 Repeat Step 1 for the next Pre-Emphasis level and for each Pre-Emphasis levels, compare the pre-emphasis delta with the pre-emphasis delta limits.

4 Calculate the pre-emphasis delta using the equation:

$$\text{Pre-Emphasis Delta (Level 1 vs Level 0)} = \text{Pre-Emphasis}_{Lvl1} - \text{Pre-Emphasis}_{Lvl0}$$

$$\text{Pre-Emphasis Delta (Level 2 vs Level 1)} = \text{Pre-Emphasis}_{Lvl2} - \text{Pre-Emphasis}_{Lvl1}$$

$$\text{Pre-Emphasis Delta (Level 3 vs Level 2)} = \text{Pre-Emphasis}_{Lvl3} - \text{Pre-Emphasis}_{Lvl2}$$

5 Report the measurement results.

PASS Condition

Pre-emphasis values for the Level 0 (OFF) state (Normative)

Level 0 (OFF) Pre-emphasis measurement:

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl0\_PP} / \text{Voltage}_{N\_Lvl0\_PP}]$ for all supported levels.

Level 0 (OFF) Pre-emphasis Measurement condition: +0.25 dB $\geq$ Resultant

Pre-emphasis Delta values for:

a Level 1 vs. Level 0 Pre-emphasis settings (NORMATIVE)

b Level 2 vs. Level 1 Pre-emphasis settings (NORMATIVE)

c Level 3 vs. Level 2 Pre-emphasis settings (NORMATIVE)

Pre-emphasis Delta measurements:

- Level 1 vs. Level 0

Resultant = 20 * Log [$Voltage_{T\_Lvl1\_PP}$ / $Voltage_{N\_Lvl1\_PP}$] - 20 * Log [$Voltage_{T\_Lvl0\_PP}$ / $Voltage_{N\_Lvl0\_PP}$] for Voltage Swing Levels 0, 1 and 2.

- Level 2 vs. Level 1

Resultant = 20 * Log [$Voltage_{T\_Lvl2\_PP}$ / $Voltage_{N\_Lvl2\_PP}$] - 20 * Log [$Voltage_{T\_Lvl1\_PP}$ / $Voltage_{N\_Lvl1\_PP}$] for Voltage Swing Levels 0 and 1.

- Level 3 vs. Level 2

Resultant = 20 * Log [$Voltage_{T\_Lvl3\_PP}$ / $Voltage_{N\_Lvl3\_PP}$] - 20 * Log [$Voltage_{T\_Lvl2\_PP}$ / $Voltage_{N\_Lvl2\_PP}$] for Voltage Swing Level 0, if supported.

Table 147 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX-PREEMP-OFF}$	Maximum Pre-emphasis when disabled	-	-	0.25	dB	Pre-emphasis Level 0 setting must not show any pre-emphasis at TP2 to prevent link training issues.
$V_{TX-PREEMP-DELTA}$	Delta of Pre-emphasis Level 1 vs. Level 0	2	-	-	dB	Applies to all valid voltage settings. Measured at Pre-emphasis Post Cursor2 Level 0. Support for Pre-emphasis Level 3 is optional.
	Delta of Pre-emphasis Level 2 vs. Level 1	1.6	-	-	dB	
	Delta of Pre-emphasis Level 3 vs. Level 2	1.6	-	-	dB	

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.3*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-22*

Expected/Observable Results

The measured pre-emphasis level or pre-emphasis delta for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Transition Voltage Range Measurement Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1272001, 1272002, 1272003, 1272004 – Non Transition Voltage Range Measurement (Swing 0)
- 1273001, 1273002, 1273003, 1273004 – Non Transition Voltage Range Measurement (Swing 1)
- 1274001, 1274002, 1274003, 1274004 – Non Transition Voltage Range Measurement (Swing 2)

For Standard DP Pattern (HBR2 and HBR3):

- 1272101, 1272102, 1272103, 1272104 – Non Transition Voltage Range Measurement (Swing 0)
- 1273101, 1273102, 1273103, 1273104 – Non Transition Voltage Range Measurement (Swing 1)
- 1274101, 1274102, 1274103, 1274104 – Non Transition Voltage Range Measurement (Swing 2)

For Arbitrary Pattern:

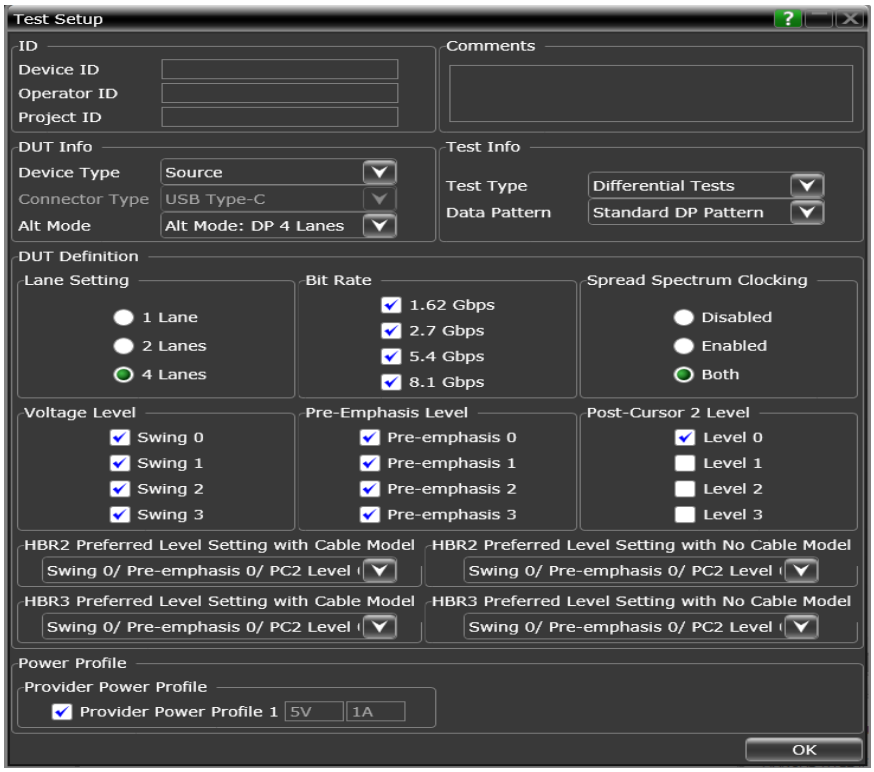
- 1372101, 1372102, 1372103, 1372104 – Non Transition Voltage Range Measurement (Swing 0)
- 1373101, 1373102, 1373103, 1373104 – Non Transition Voltage Range Measurement (Swing 1)
- 1374101, 1374102, 1374103, 1374104 – Non Transition Voltage Range Measurement (Swing 2)

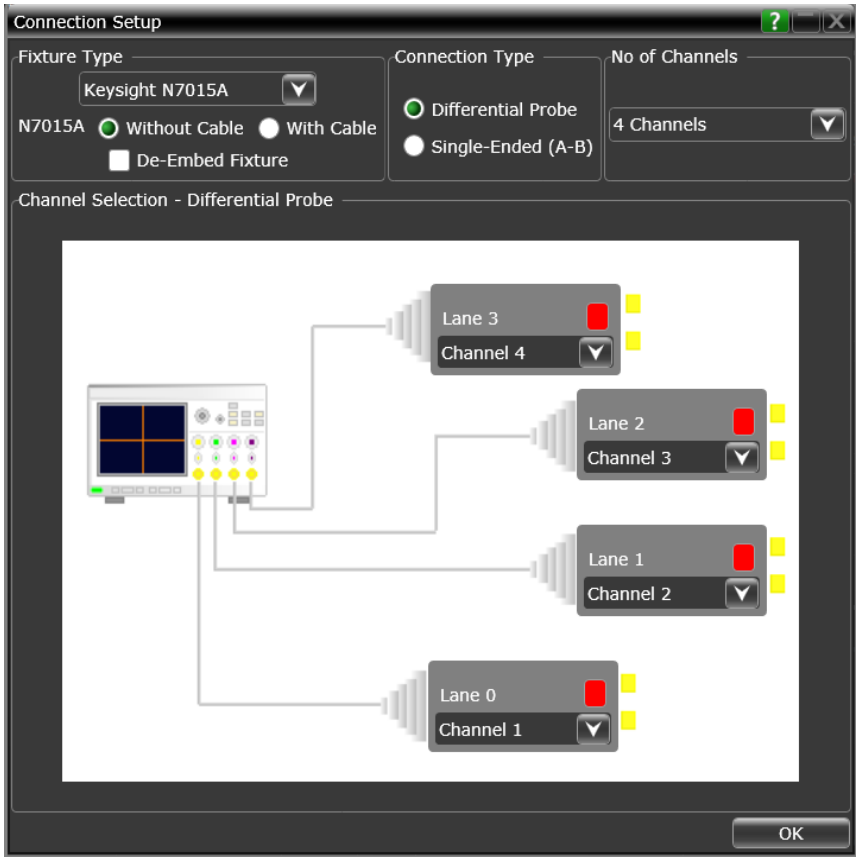
Test Overview

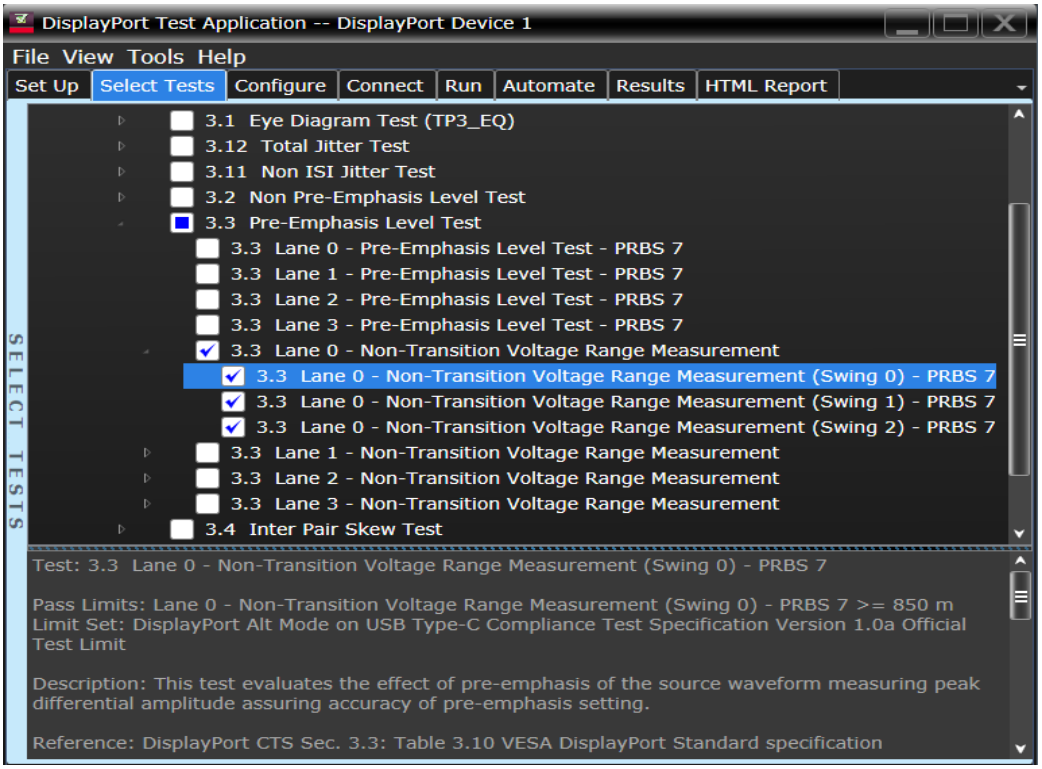
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings. Comparisons are also made for the Level 0 transition state as well as non-transition levels.

Test Conditions for Non-Transition Voltage Range Measurement Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR and HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.4 Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given Voltage Level, repeat the following steps for all pre-emphasis levels subjected to constraints specified in Table 3-1 of the VESA DisplayPort 1.4 Standard:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.

- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6th bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4th bit of the four successive transmitted zeros of the pattern.

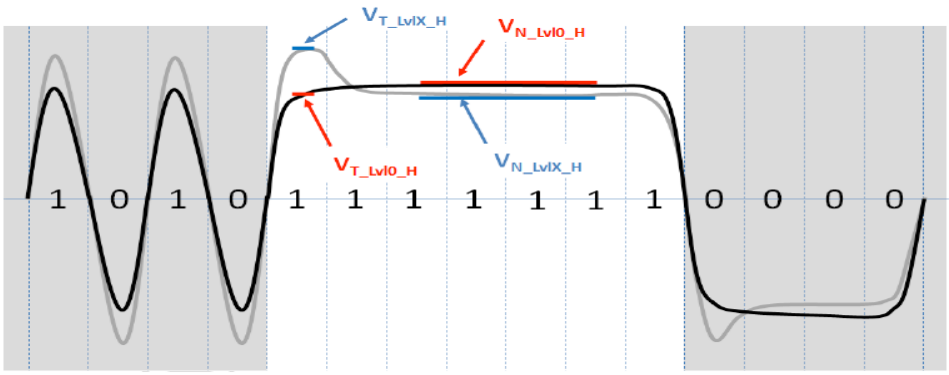


Figure 138 High Voltage measurement for RBR and HBR

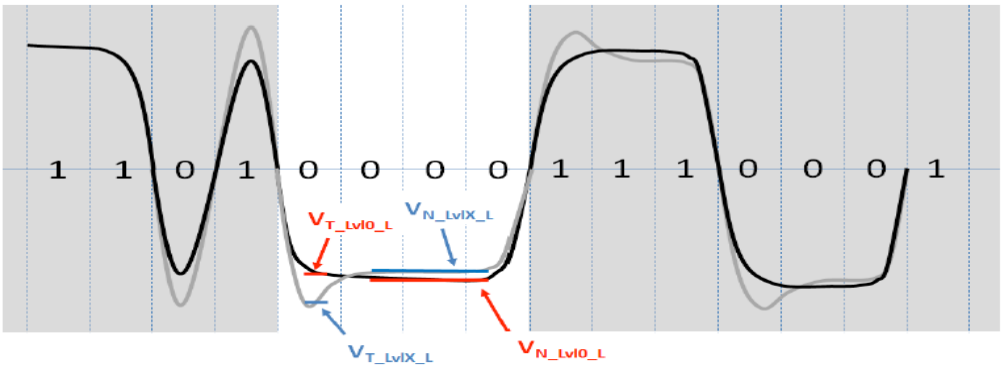


Figure 139 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR3 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

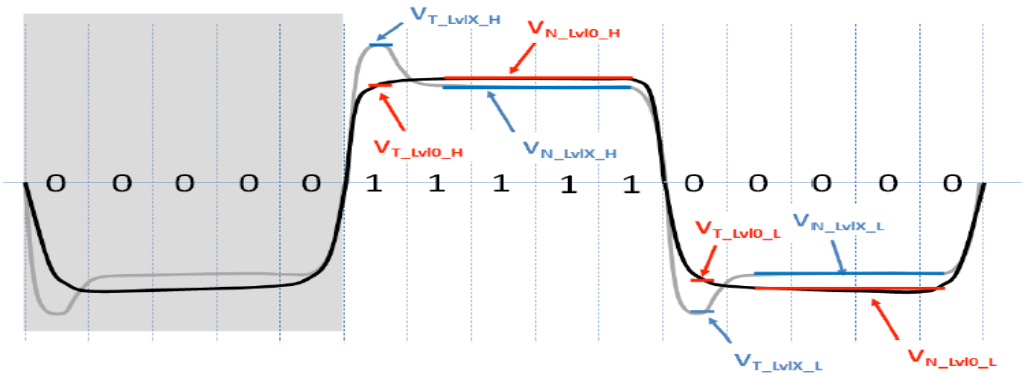


Figure 140 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

2 Calculate the non transition voltage range using the equation:

$$\text{Non Transition Voltage Range} = \text{Minimum } [(V_{N\_LvlX\_PP}) / (V_{N\_Lvl0\_PP})]$$

where, $V_{N\_LvlX\_PP}$) refers to all supported pre-emphasis levels (Level1, Level2, Level3 and so on up to Level X).

3 Report the measurement results.

PASS Condition

Non-Transition Voltage Range Measurements

For Level 2 voltage setting: Resultant > 0.708 OR 20*log(Resultant) > -3dB

For Level 1 voltage setting: Resultant > 0.708 OR 20*log(Resultant) > -3dB

For Level 0 voltage setting: Resultant > 0.85 OR 20*log(Resultant) > -1.4dB

Table 148 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX-DIFF\_REDUCTION}$	Non-transition reduction Output Voltage Level 2	-	-	3	dB	$V_{TX-DIFF}$ at each non-zero nominal pre-emphasis level must not be lower than the specified amount less than $V_{TX-DIFF}$ at the zero nominal pre-emphasis level.
	Non-transition reduction Output Voltage Level 1	-	-	3	dB	
	Non-transition reduction Output Voltage Level 0	-	-	1.4	dB	

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.3*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-22*

Expected/Observable Results

The measured output voltage level reduction of the non transition bit for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Peak to Peak Voltage Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1266001, 1266002, 1266003, 1266004 – Peak to Peak Voltage Test

For Standard DP Pattern (HBR2 and HBR3):

- 1266101, 1266102, 1266103, 1266104 – Peak to Peak Voltage Test

For Arbitrary Pattern:

- 1366101, 1366102, 1366103, 1366104 – Peak to Peak Voltage Test

Test Overview

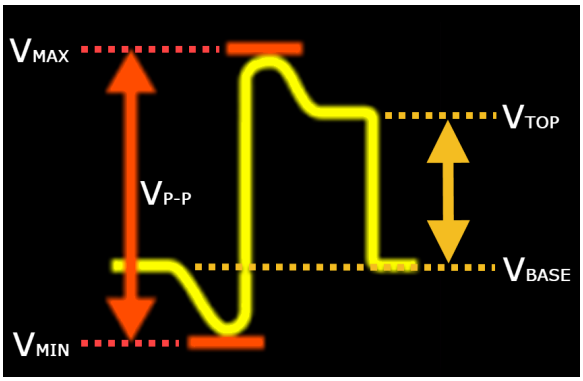
The objective of this test is to evaluate the maximum differential peak to peak voltage.

NOTE

The peak to peak voltage (V_{P-P}) formula is:

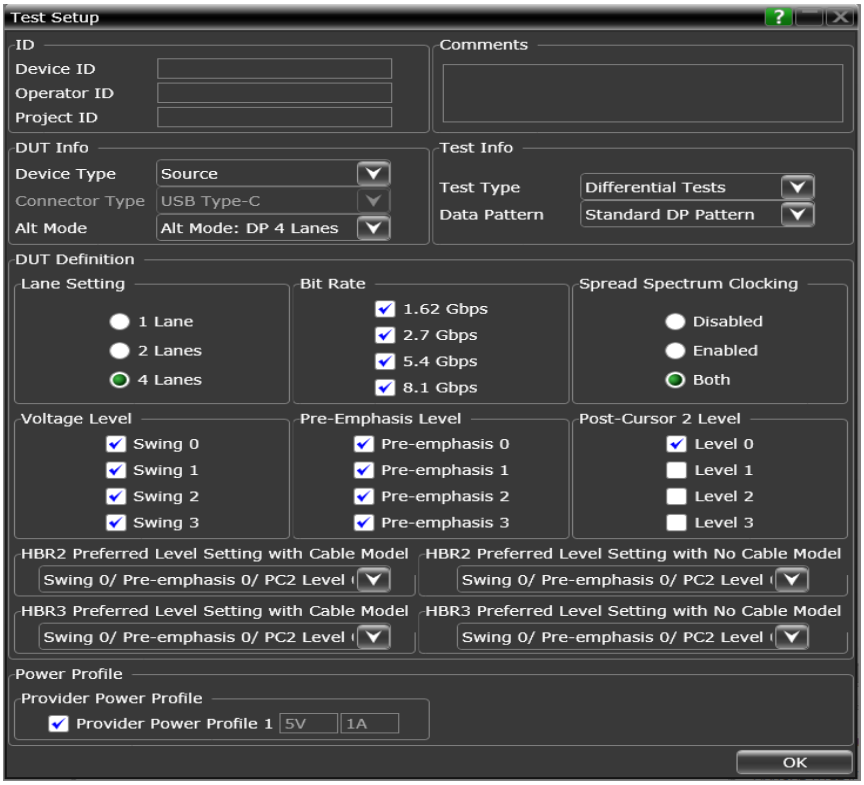
$$V_{P-P} = V_{MAX} - V_{MIN}$$

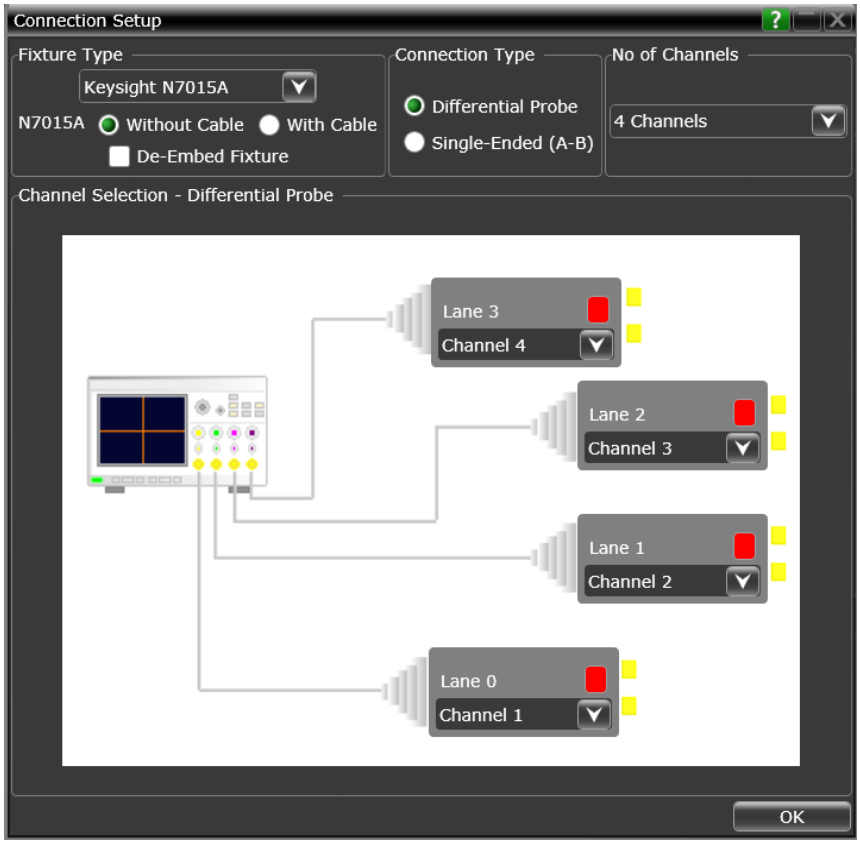
Please see the figure below for more info.

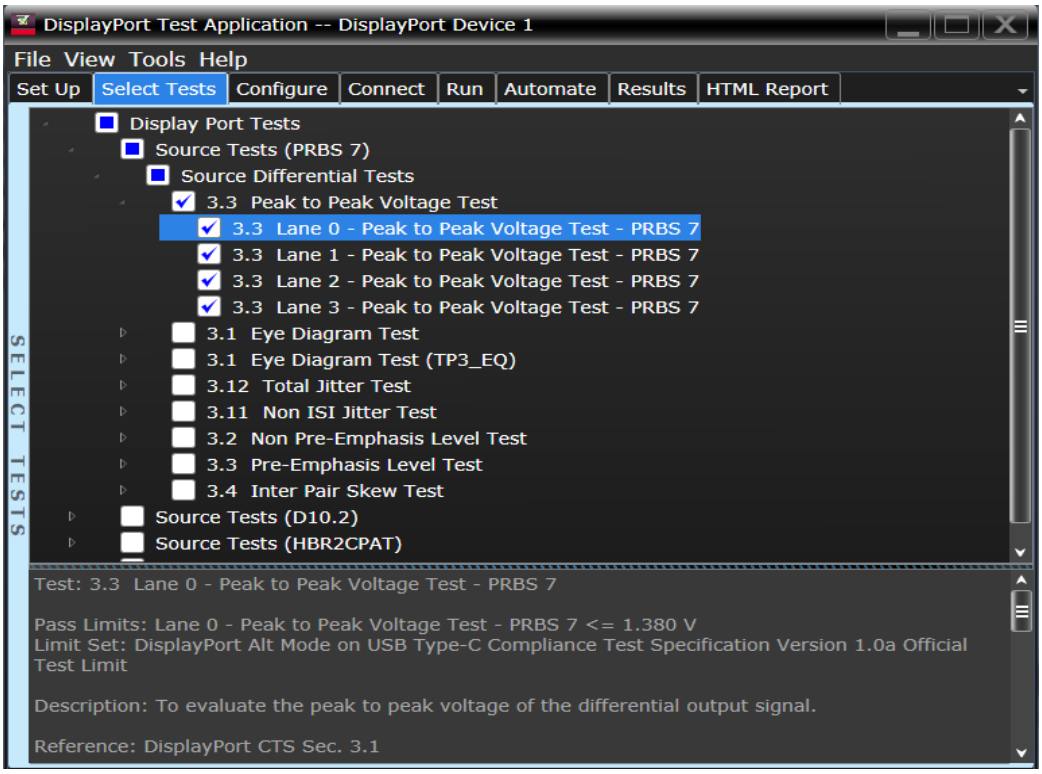


Test Conditions for Peak to Peak Voltage Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, and HBR3)
SSC	▪ For RBR/HBR using PRBS7 pattern, test with SSC Enabled only if that condition is supported by the DUT. ▪ For HBR2/HBR3 using PLTPAT pattern, test with SSC Disabled if that condition is supported by the DUT.
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.4 Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR3 – PLTPAT




Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Display Port Tests
Source Tests (PRBS 7)
Source Differential Tests
3.3 Peak to Peak Voltage Test
3.3 Lane 0 - Peak to Peak Voltage Test - PRBS 7
3.3 Lane 1 - Peak to Peak Voltage Test - PRBS 7
3.3 Lane 2 - Peak to Peak Voltage Test - PRBS 7
3.3 Lane 3 - Peak to Peak Voltage Test - PRBS 7
3.1 Eye Diagram Test
3.1 Eye Diagram Test (TP3_EQ)
3.12 Total Jitter Test
3.11 Non ISI Jitter Test
3.2 Non Pre-Emphasis Level Test
3.3 Pre-Emphasis Level Test
3.4 Inter Pair Skew Test
Source Tests (D10.2)
Source Tests (HBR2CPAT)
Test: 3.3 Lane 0 - Peak to Peak Voltage Test - PRBS 7
Pass Limits: Lane 0 - Peak to Peak Voltage Test - PRBS 7 <= 1.380 V
Limit Set: DisplayPort Alt Mode on USB Type-C Compliance Test Specification Version 1.0a Official Test Limit
Description: To evaluate the peak to peak voltage of the differential output signal.
Reference: DisplayPort CTS Sec. 3.1

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{MAX} and V_{MIN} of the input signal.
   d Measure the data rate of the input signal.
3 Measure the maximum and minimum voltage of the input signal.
4 Calculate the peak to peak voltage using the equation:

$$\text{Peak to Peak Voltage} = V_{MAX} - V_{MIN}$$

5 Report the measurement results.

PASS Condition

For all Data Rates:

Maximum Differential Peak to Peak Voltage $\leq$ 1.38V.

Table 149 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}DIFFp\text{-}p\_MAX}$	Max Output Voltage Level	-	-	1.38	V	For all Output Level and Pre-emphasis combinations.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.3*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-22*

Expected/Observable Results

The measured peak to peak voltage for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Inter-Pair Skew Test (Informative)

Test ID

For Standard DP Pattern:

- 1290001 – Lane0/Lane1 Inter-Pair Skew Test
- 1290002 – Lane0/Lane2 Inter-Pair Skew Test
- 1290003 – Lane0/Lane3 Inter-Pair Skew Test
- 1290004 – Lane1/Lane2 Inter-Pair Skew Test
- 1290005 – Lane1/Lane3 Inter-Pair Skew Test
- 1290006 – Lane2/Lane3 Inter-Pair Skew Test

For Arbitrary Pattern:

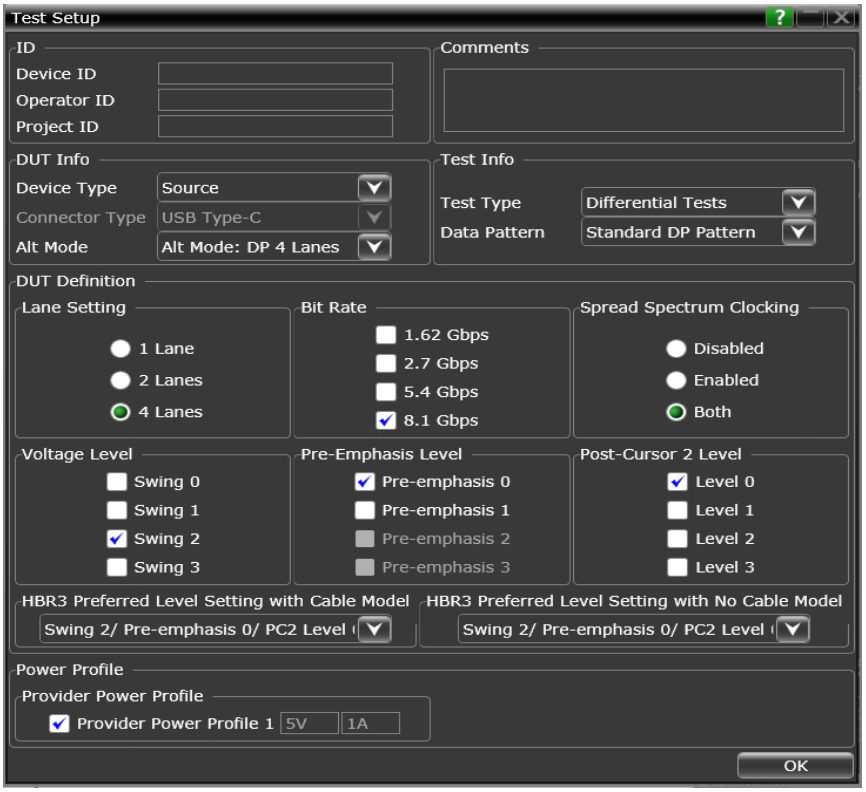
- Not applicable for arbitrary pattern

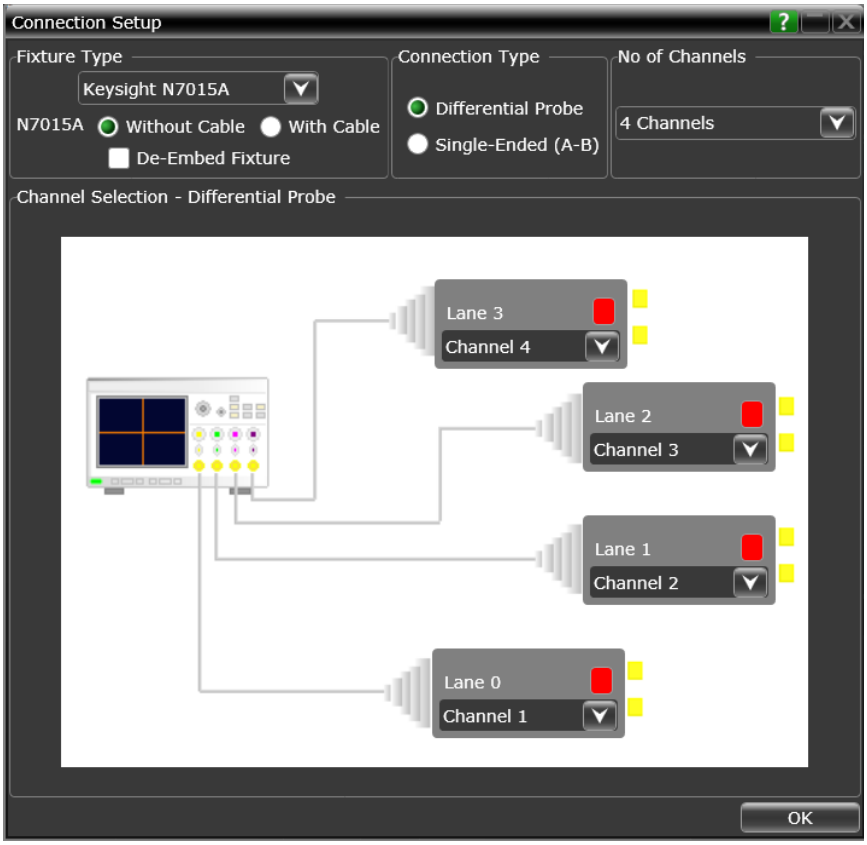
Test Overview

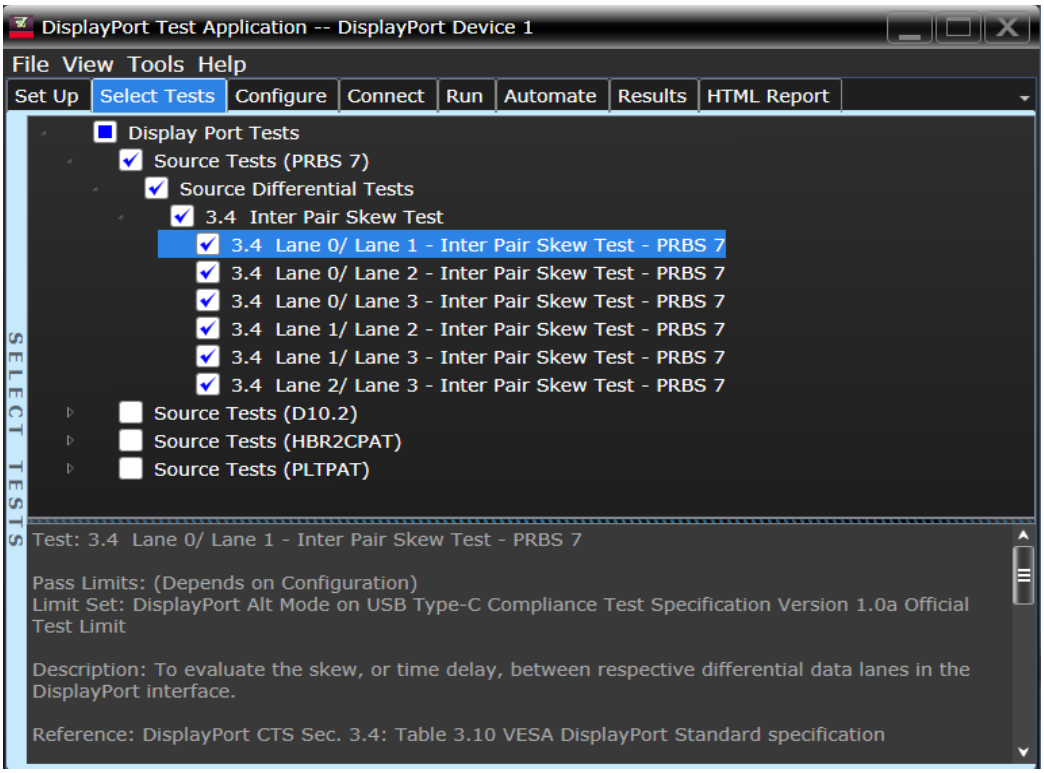
The objective of the test is to evaluate the skew or time delay between differential data lanes in the DisplayPort interface.

Test Conditions for Inter Pair Skew Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest Bit Rate supported (RBR, HBR, HBR2, or HBR3)
SSC	If DUT supports both SSC On and Off conditions, run tests using SSC Enabled only.
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported For two lane operation: Lane 0 to Lane 1 For four lane operation: Lane 0 to Lane 1 Lane 0 to Lane 2 Lane 0 to Lane 3 Lane 1 to Lane 2 Lane 1 to Lane 3 Lane 2 to Lane 3
Test Pattern	PRBS7 or DUT-dependent custom pattern


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Display Port Tests
Source Tests (PRBS 7)
Source Differential Tests
3.4 Inter Pair Skew Test
3.4 Lane 0/ Lane 1 - Inter Pair Skew Test - PRBS 7
3.4 Lane 0/ Lane 2 - Inter Pair Skew Test - PRBS 7
3.4 Lane 0/ Lane 3 - Inter Pair Skew Test - PRBS 7
3.4 Lane 1/ Lane 2 - Inter Pair Skew Test - PRBS 7
3.4 Lane 1/ Lane 3 - Inter Pair Skew Test - PRBS 7
3.4 Lane 2/ Lane 3 - Inter Pair Skew Test - PRBS 7
Source Tests (D10.2)
Source Tests (HBR2CPAT)
Source Tests (PLTPAT)
Test: 3.4 Lane 0/ Lane 1 - Inter Pair Skew Test - PRBS 7
Pass Limits: (Depends on Configuration)
Limit Set: DisplayPort Alt Mode on USB Type-C Compliance Test Specification Version 1.0a Official Test Limit
Description: To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
Reference: DisplayPort CTS Sec. 3.4: Table 3.10 VESA DisplayPort Standard specification

Measurement Procedure

1 For a given inter-pair skew measurement of Lane A to Lane B:
   a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   b Acquire and verify the input signal:
      i Verify the trigger and the amplitude of the Lane A input signal.
      ii Scale the vertical display of the Lane A input signal to optimum value.
      iii Measure V_{TOP} and V_{BASE} of the Lane A input signal.
      iv Verify the trigger and the amplitude of the Lane B input signal.
      v Scale the vertical display of the Lane B input signal to optimum value.
      vi Measure V_{TOP} and V_{BASE} of the Lane B input signal.
      vii Measure the data rate of the Lane A input signal.
      viii Measure the data rate of the Lane B input signal.
   c Set up the parameter of the measurement:
      i Enable measurement of all edges to obtain a statistical value of the measurement.
      ii Set up the measurement threshold.
   d Set up the parameter for the inter-pair skew measurement:
      i Set up two display grids such that each grid displays one test lane data signal.
      ii Set up the measurement threshold for each test lane data signal on the Transition Voltage = 0V.
      iii Decode the data signal for each test lane.
      iv Search the desired pattern from the decoded data signal.
      v Measure the time difference between the corresponding edges of both test lanes:

$$T_{Transition\_LaneA} - T_{Transition\_LaneB}$$

      vi Repeat the previous step until you measure 100 edges.
      vii VESA DisplayPort 1.4 Standard specifies 20 UI offset Lane 0 to Lane 1, Lane 1 to Lane 2 and Lane 2 to Lane 3. The resultant offset is cumulative.
      viii Calculate the inter-pair skew using the equation:

$$\text{Inter-Pair Skew} = \{1/\text{Number of Edges}\} \sum |T_{Transition\_LaneA} - T_{Transition\_LaneB}| - \text{Nominal Skew}$$

   where, Nominal Skew is the expected offset between tested lanes.
2 Report the measurement results.

PASS Condition

For HBR3,
-(6 UI + 500 ps) ≤ Inter-Lane Skew Tolerance ≤ (6 UI + 500 ps)
For HBR2,
-(4 UI + 500 ps) ≤ Inter-Lane Skew Tolerance ≤ (4 UI + 500 ps)
For HBR/RBR,
-2UI ≤ Inter-Lane Skew Tolerance ≤ 2UI

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.6*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-22*

Expected/Observable Results

The measured inter-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Main Link Frequency Compliance Test

Test ID

For Standard DP Pattern:

- 12193001 12193002 12193003 12193004 – Main Link Frequency Compliance

For Arbitrary Pattern:

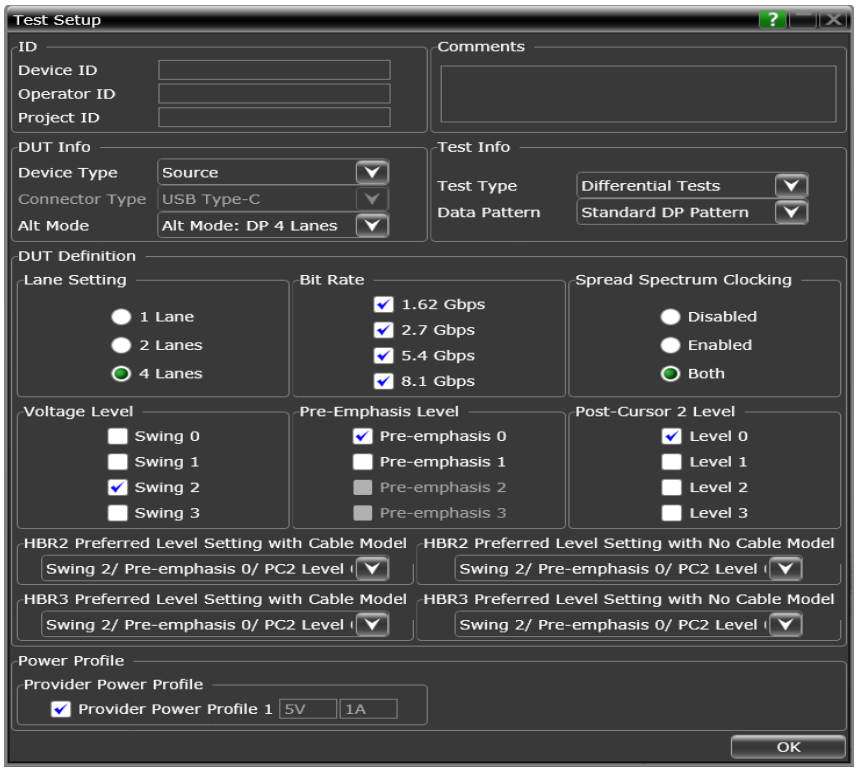
- 13193001 13193002 13193003 13193004 – Main Link Frequency Compliance

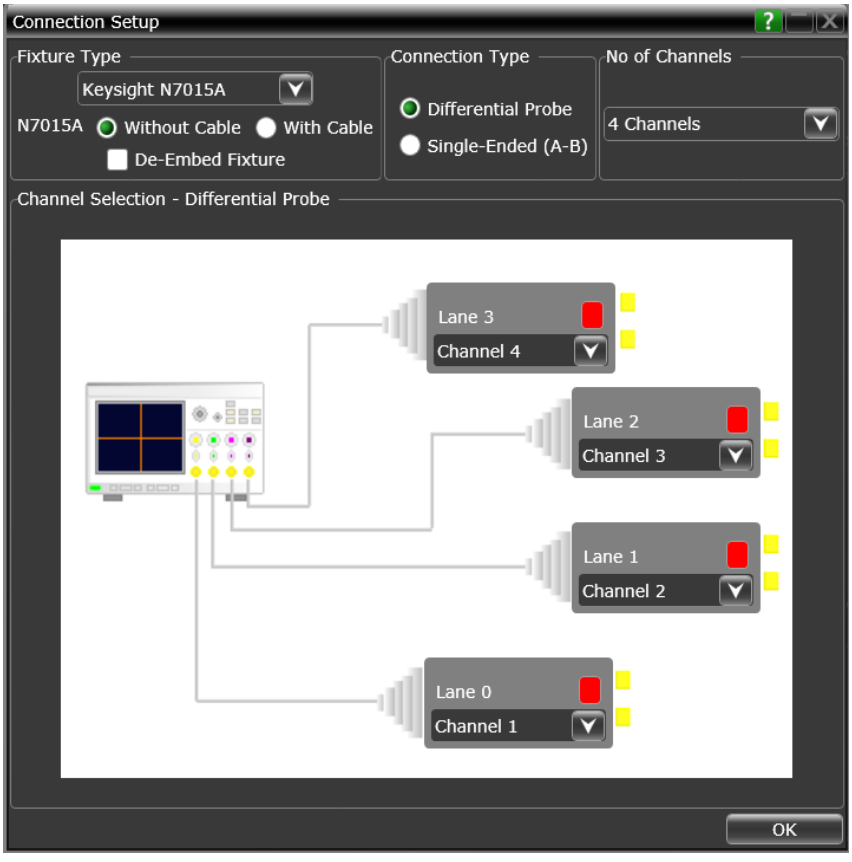
Test Overview

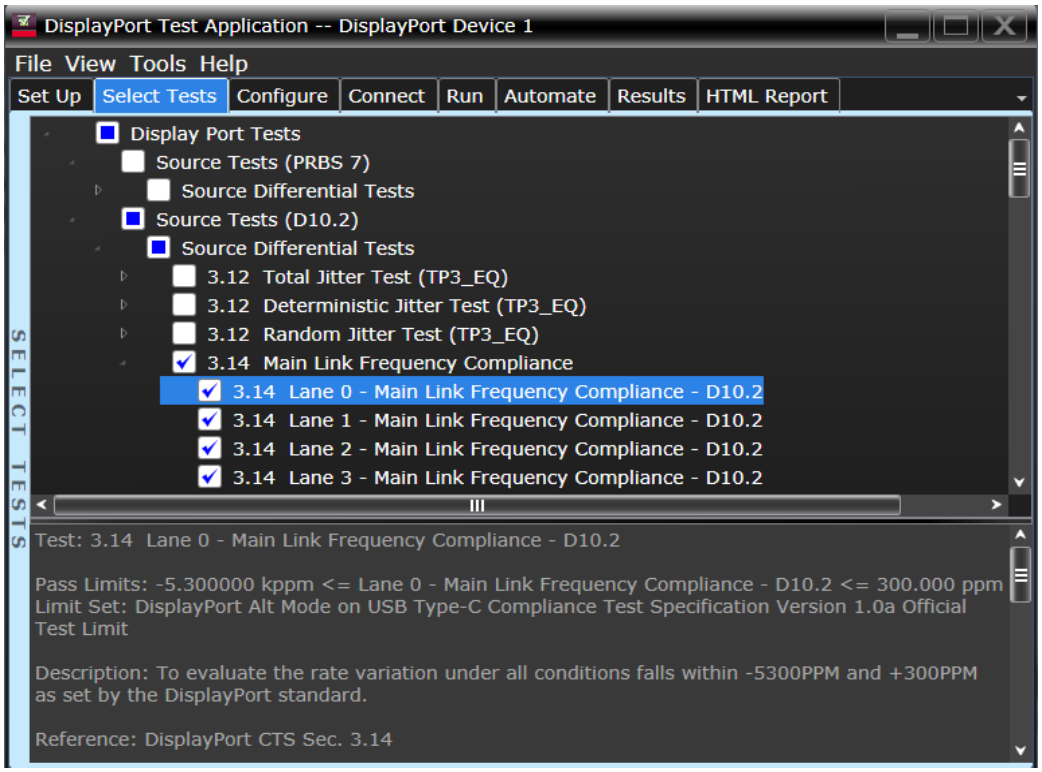
The objective of this test is to ensure that the average data rate under all conditions does not exceed the minimum and maximum values as set by the VESA DisplayPort 1.4 Standard.

Test Conditions for Main Link Frequency Compliance Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, and HBR3)
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.

5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and the minimum measurement levels for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurement levels for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e For SSC Enabled Test condition, check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butter worth Low Pass Filter with 3dB corner frequency of 5.0 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.
9 For the test condition “SSC Enabled”, set up the parameter of the SSC measurement:
   a Set up the memory depth and time-base to display one complete SSC cycle based on the measured SSC modulation frequency in Step 5.
   b Acquire the signal with one complete SSC cycle.
   c Get the minimum of FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

      Maximum Data Rate = 1 / (Minimum Unit Interval)

   d Get the maximum of FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

      Minimum Data Rate = 1 / (Maximum Unit Interval)

   e Repeat steps b, c and d until you acquire 10 SSC Cycles.
   f Calculate the mean value for the maximum and minimum data rates.
10 Report the measurement results.

PASS Condition

For SSC enabled:

Maximum Data Rate (Frequency Max_{ppm}) $\leq$ 300 ppm

Minimum Data Rate (Frequency Min_{ppm}) $\geq$ -5300 ppm

For SSC disabled:

Maximum Data Rate (Frequency Max_{ppm}) $\leq$ 300 ppm

Minimum Data Rate (Frequency Min_{ppm}) $\geq$ -300 ppm

Table 150 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
f_{HBR3}	Frequency for High Bit Rate 3	8.05707	8.1	8.10243	Gbps	
f_{HBR2}	Frequency for High Bit Rate 2	5.37138	5.4	5.40162	Gbps	Frequency high limit = +300ppm Frequency low limit = -5300ppm
f_{HBR}	Frequency for High Bit Rate	2.68569	2.7	2.70081	Gbps	
f_{RBR}	Frequency for Reduced Bit Rate	1.611414	1.62	1.620486	Gbps	

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.12*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-20*

Expected/Observable Results

The measured data rate for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Frequency Test

Test ID

For Standard DP Pattern:

- 12170001 12170002 12170003 12170004 – SSC Modulation Frequency Test

For Arbitrary Pattern:

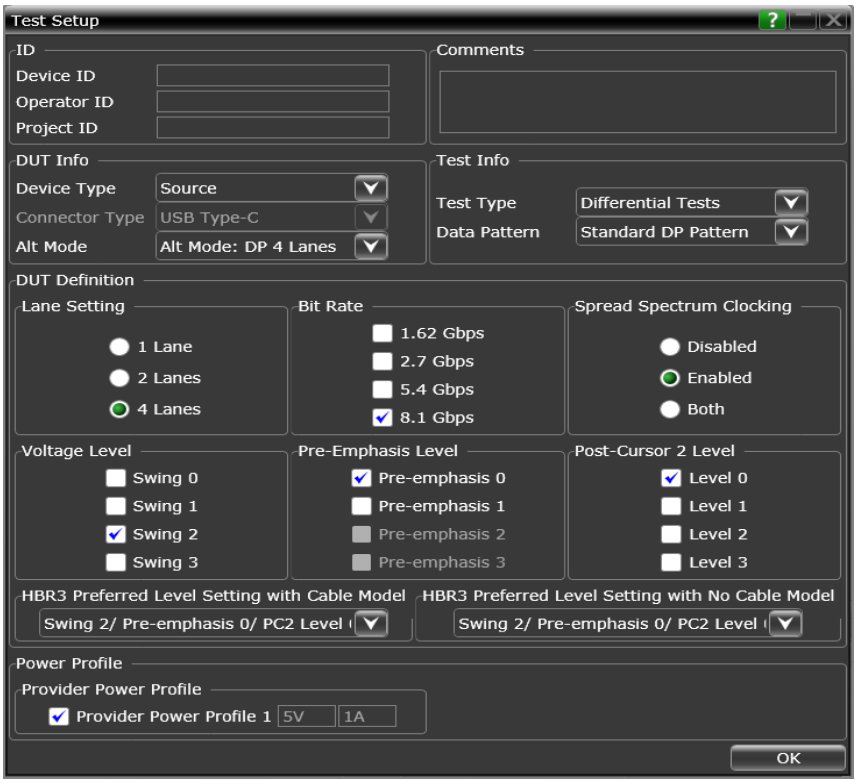
- 13170001 13170002 13170003 13170004 – SSC Modulation Frequency Test

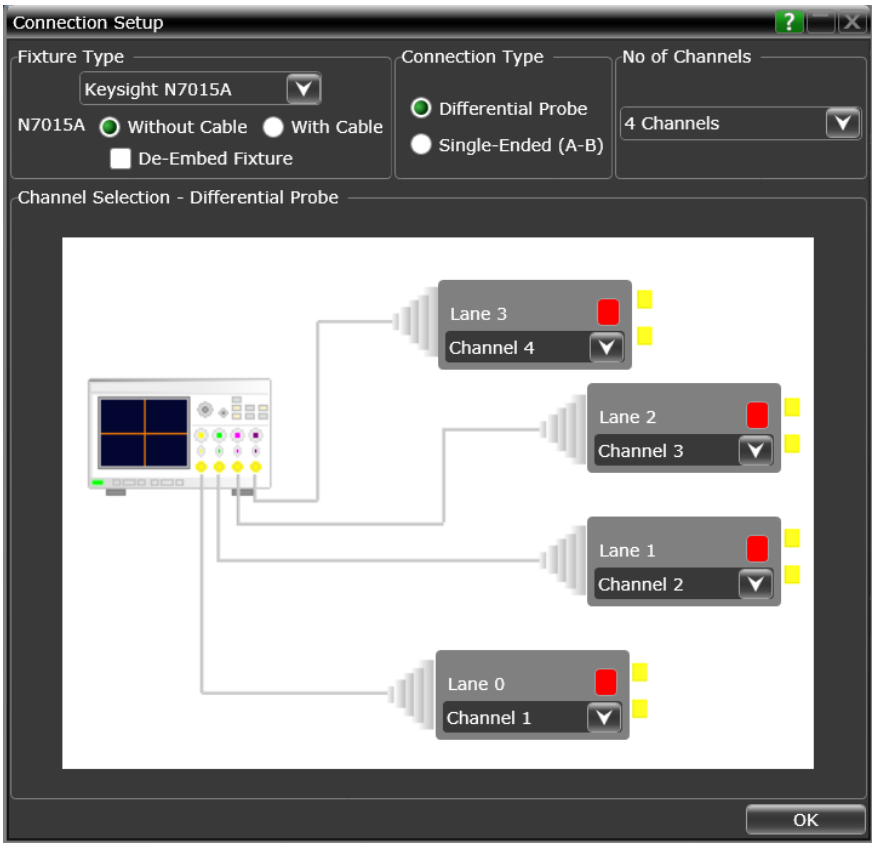
Test Overview

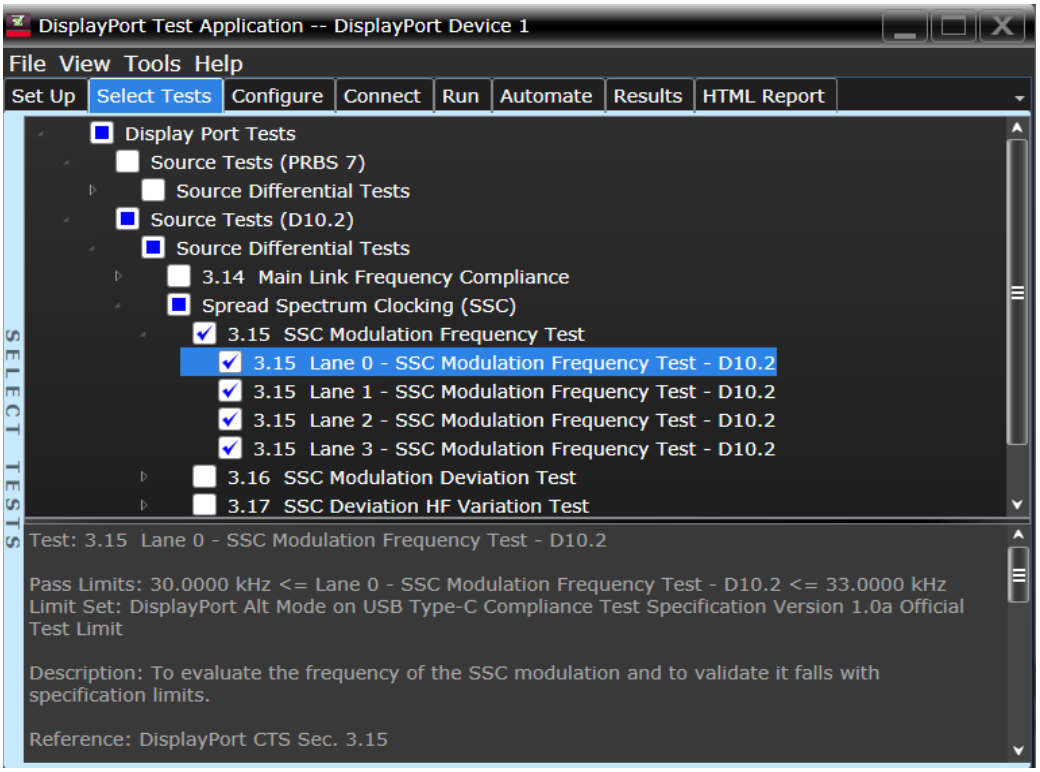
The objective of this test is to evaluate the frequency of the SSC modulation and to validate that the frequency is within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. Calculate the SSC modulation frequency from the average of the measured SSC modulation frequency for each cycle.

Test Conditions for SSC Modulation Frequency Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2, or HBR3)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.

5 Set up the parameters for the frequency measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 5.0 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.
   g Acquire the signal for 10 SSC Cycles.
6 Get the mean value for the SSC Modulation frequency.
7 Report the measurement results.

PASS Condition

30kHz $\leq$ SSC Modulation Frequency (f_{SSC}) $\leq$ 33kHz

Table 151 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
Down_Spread_Frequency	Link clock down-spreading frequency	30	-	33	kHz	Range: 30kHz ~ 33kHz when down-spread enabled

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.13*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-20*

Expected/Observable Results

The measured SSC modulation frequency for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Deviation Test

Test ID

For Standard DP Pattern:

- 12180001 12180002 12180003 12180004 – SSC Modulation Deviation Test

For Arbitrary Pattern:

- 13180001 13180002 13180003 13180004 – SSC Modulation Deviation Test

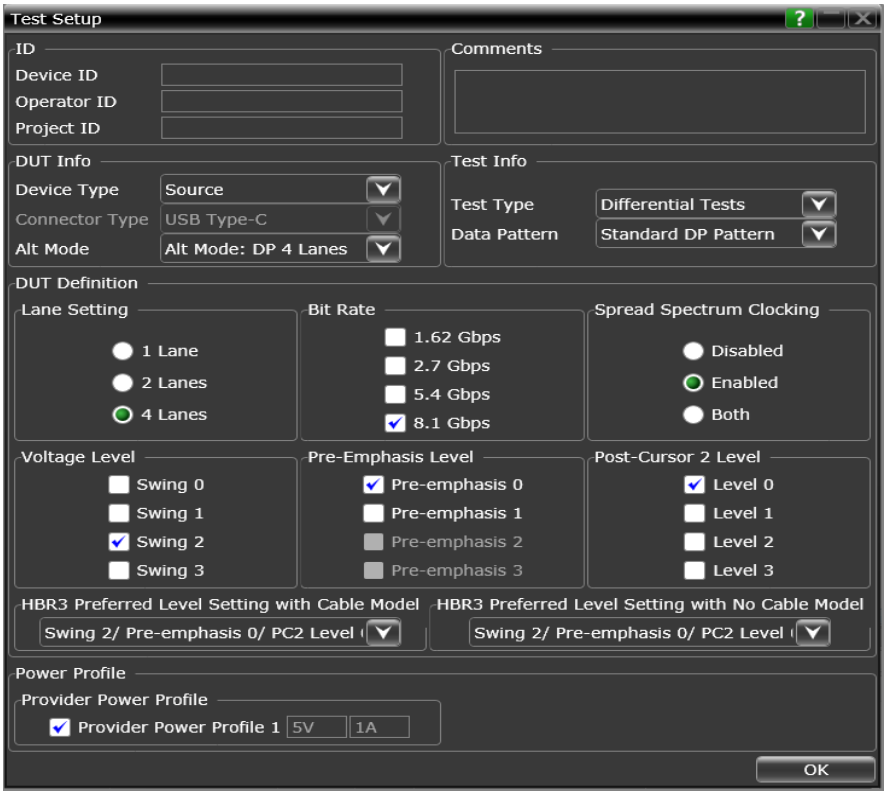
Test Overview

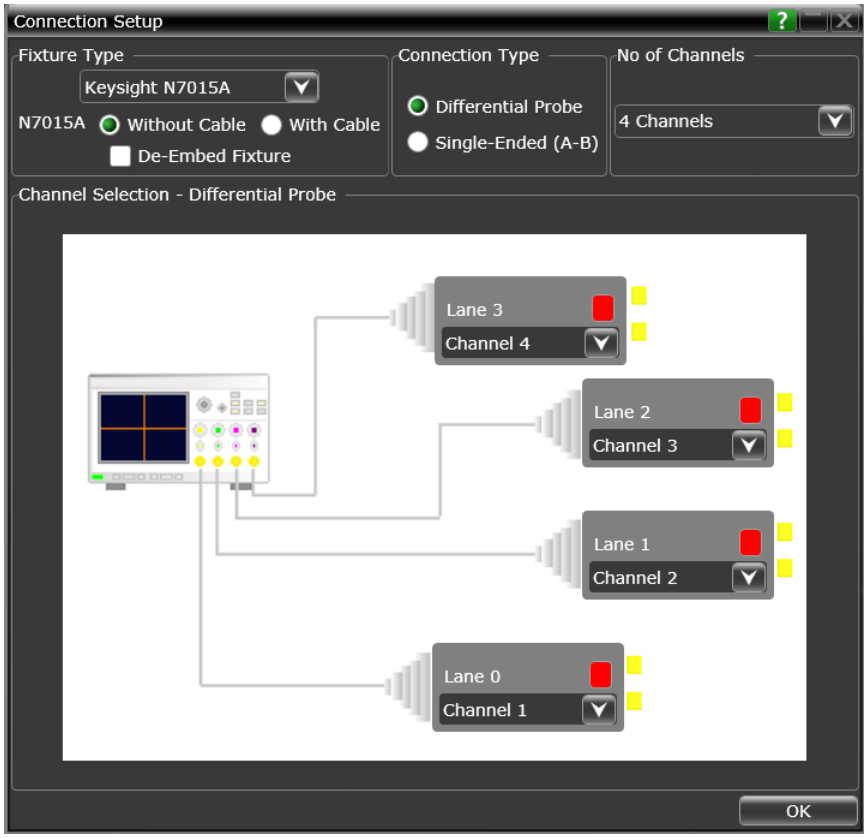
The objective of this test is to evaluate the range of SSC down-spreading of the transmitter signal in ppm and to validate that the values are within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. For each cycle, the minimum and maximum data rate is evaluated. Calculate the SSC modulation deviation from the average of the maximum minus the average of the minimum using the equation:

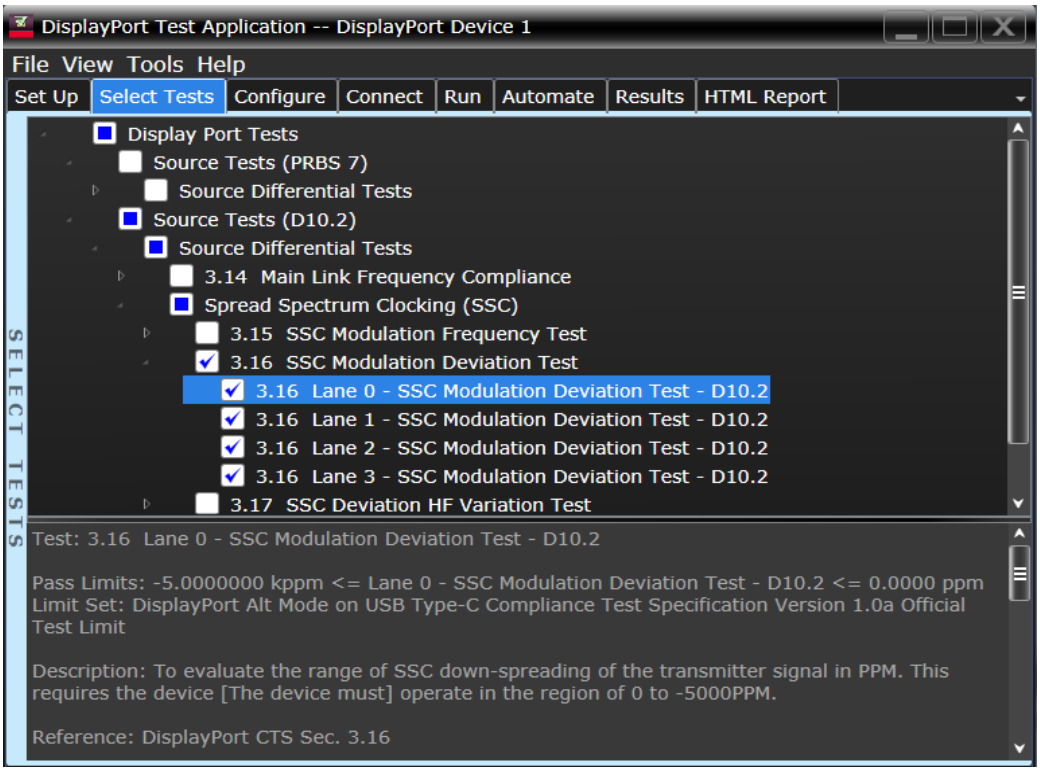
SSC Modulation Deviation = {[Average (Minimum Data Rate) - Average (Maximum Data Rate)] / Nominal Data Rate}*1E+6

Test Conditions for SSC Modulation Deviation Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2, or HBR3)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.

5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and minimum measurements for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurements for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e Check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point for three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 5.0 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 filtered unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurements for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.
9 Set up the parameters for SSC measurement.
   a Set up memory depth and time-base to display one complete SSC Cycle based on the measured SSC modulation frequency in step 5.
   b Acquire the signal with one complete SSC Cycle.
   c Get the minimum of the FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

      Maximum Data Rate = 1/Minimum Unit Interval

   d Get the maximum of the FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

      Minimum Data Rate = 1/Maximum Unit Interval

   e Repeat step b,c and d until you acquire 10 SSC Cycles.
   f Calculate the mean value for the maximum and minimum data rate.
10 Calculate the SSC Modulation Deviation using the equation:

   SSC Modulation Deviation = {[Average (Minimum Data Rate) - Average (Maximum Data Rate)] / Nominal Data Rate}*1E+6

11 Report the measurement results.

PASS Condition

-5300 ppm $\leq$ SSC Modulation Deviation (Resultant$_{SSC\ Range}$) $\leq$ 300 ppm

Table 152 DisplayPort Main Link Transmitter System Parameters

Symbol	Parameter	Min	Nom	Max	Unit	Comments
Down_Spread_Amplitude	Link clock down-spreading	0	-	0.5	%	Range: 0% ~ 0.5% when down-spread enabled

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.14*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-20*

Expected/Observable Results

The measured SSC modulation deviation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Deviation HF Variation Test (Informative)

Test ID

For Standard DP Pattern:

- 12200001 12200002 12200003 12200004 – SSC Deviation HF Variation Test (Informative)

For Arbitrary Pattern:

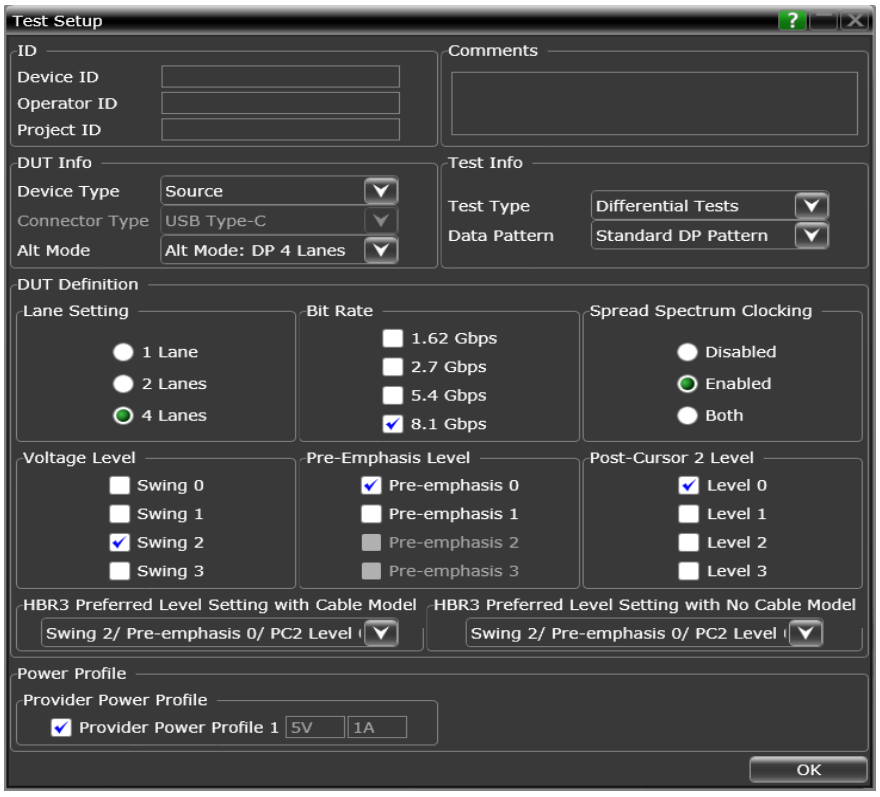
- 13200001 13200002 13200003 13200004 – SSC Deviation HF Variation Test (Informative)

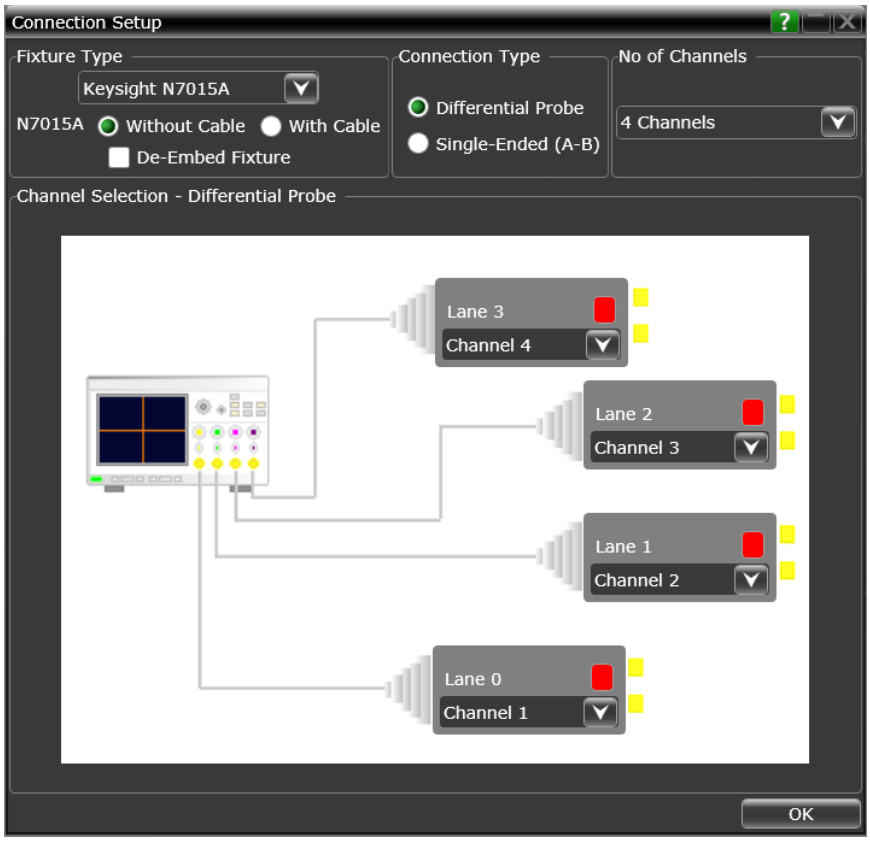
Test Overview

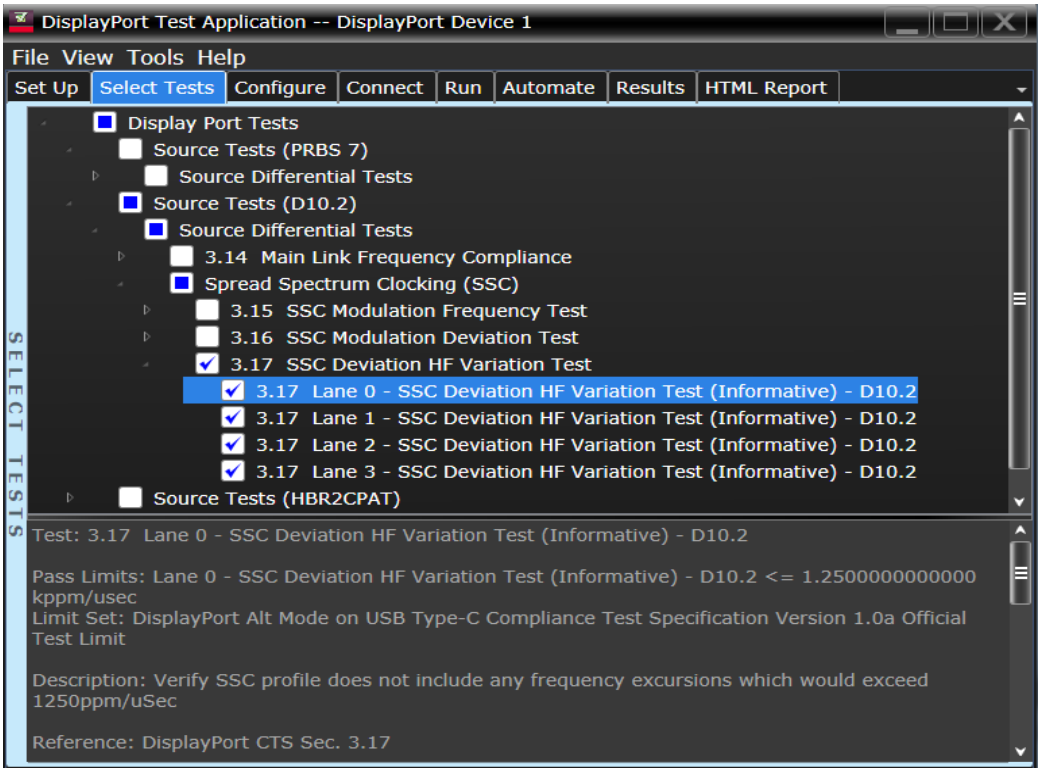
The objective of this test is to verify that the SSC profile does not include any frequency deviation that may exceed 1250 ppm/µsec. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles.

Test Conditions for SSC Deviation HF Variation Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2, or HBR3)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.

5 Set up the parameters for the frequency measurement.

a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 5.0 MHz.

b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.

c Set up the memory depth and time-base using the settings defined in the Configuration Variable.

d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.

e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).

f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.

6 Set up the parameters for the SSC measurement.

a Set up memory depth and time-base to display one complete SSC cycle using the measured SSC Modulation Frequency in Step 5.

b Acquire the signal with one complete SSC Cycles.

c Read the FUNC2 filtered unit interval measurement trend.

d Compute the slope using the “Sliding Window” with 0.5 µsec window width. Calculate the slope using the equation:

$$\text{Slope} = [f(t) - f(t-0.5\ \mu\text{sec})/0.5\ \mu\text{sec}$$

e Repeat step b, c and d until you acquire 10 SSC Cycles.

f Get the maximum value for the computed value of slope.

7 Report the measurement results.

PASS Condition

SSC_t dF/dt $\leq$ 1250ppm/µsec

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.15*

Expected/Observable Results

The measured SSC deviation high frequency variation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Eye Diagram Test (TP3_EQ)

Test ID

For Standard DP Pattern (HBR):

- 1211001, 1211002, 1211003, 1211004 – Eye Diagram Test (TP3_EQ) - PRBS7
- 1211011, 1211012, 1211013, 1211014 – Eye Diagram Test with No Cable Model (TP3_EQ) - PRBS7

For Standard DP Pattern (HBR2 and HBR3):

- 1215001, 1215002, 1215003, 1215004 – Eye Diagram Test (TP3_EQ) - HBR2CPAT
- 1215011, 1215012, 1215013, 1215014 – Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT

For Arbitrary Pattern:

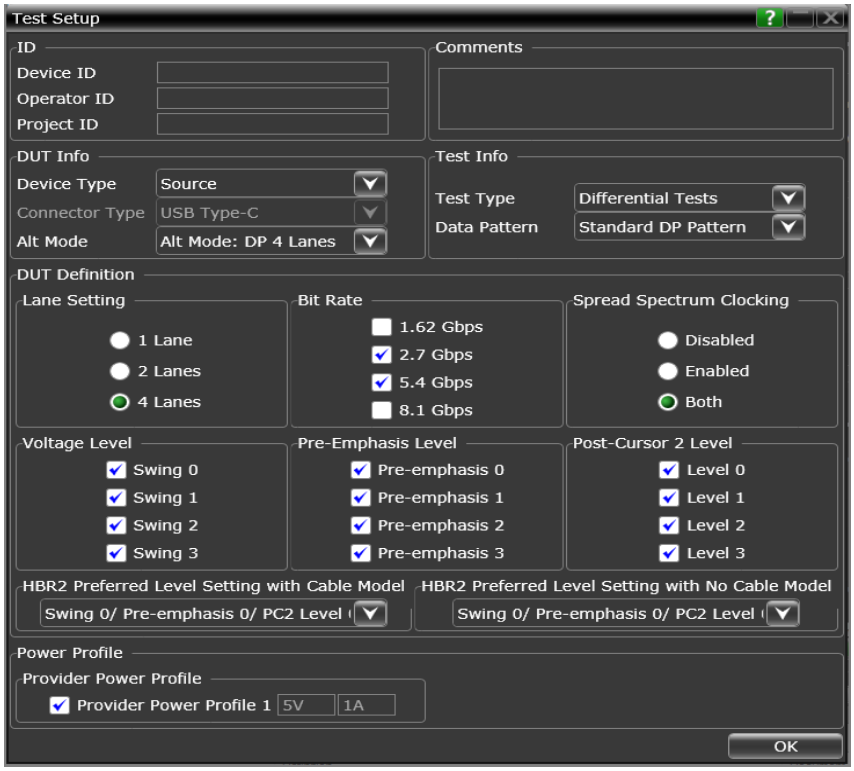
- 1315001, 1315002, 1315003, 1315004 – Eye Diagram Test (TP3_EQ)
- 1315011, 1315012, 1315013, 1315014 – Eye Diagram Test with No Cable Model (TP3_EQ)

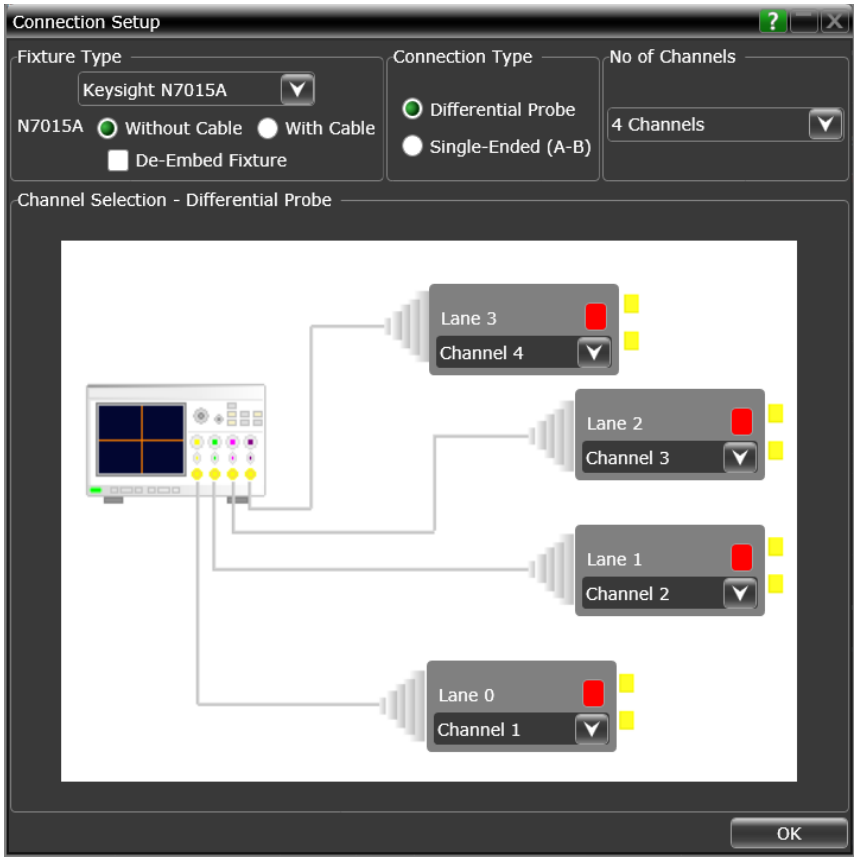
Test Overview

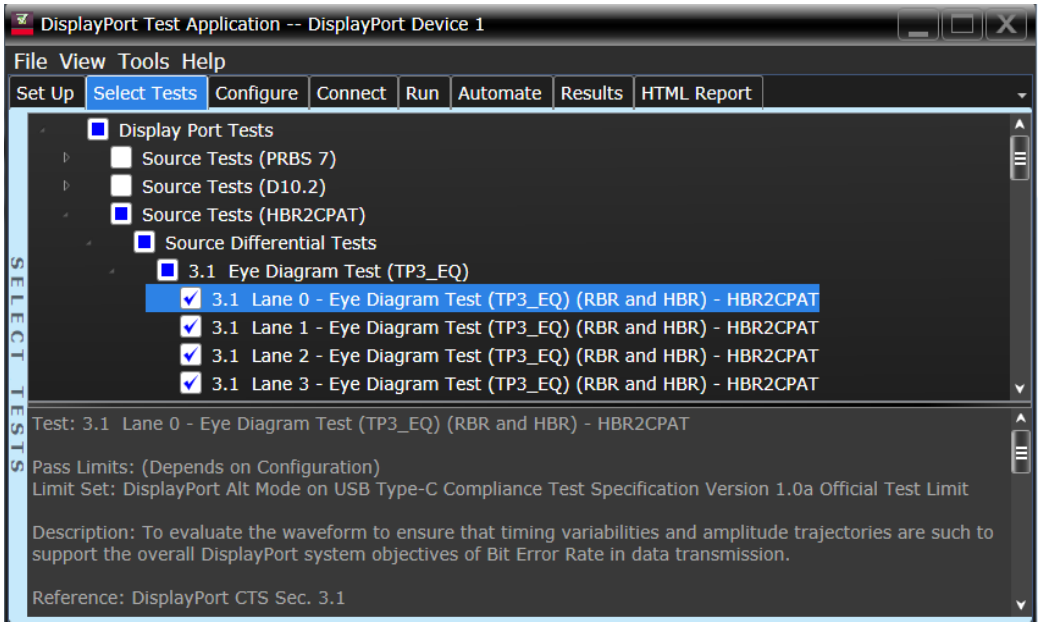
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions for Eye Diagram Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR (Informative) and HBR2
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	HBR – Level 2 HBR2 – Any Voltage Level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	HBR – Level 0 HBR2 – Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	HBR – Level 0 HBR2 – Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	HBR – PRBS7 HBR2 – HBR2CPAT
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure for HBR

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.

8 Measure the jitter of the eye diagram using the Histogram.
9 Check for any signal trajectories that may have entered into the mask.
10 Report the measurement results.

Measurement Procedure for HBR2

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]:
   a Pattern fold the equalized signal based on the High Level Voltage (V_{HIGH}) random noise configuration variable.
   b Set up the vertical waveform histogram on the equalized signal to measure random noise of High Level Voltage (V_{HIGH}).
   c Measure the High Level Voltage (V_{HIGH}) random noise based on the standard deviation of the waveform histogram.
   d Pattern fold the equalized signal based on the Low Level Voltage (V_{LOW}) random noise configuration variable.
   e Set up the vertical waveform histogram on the equalized signal to measure the random noise of Low Level Voltage (V_{LOW}).
   f Measure the Low Level Voltage (V_{LOW}) random noise based on the standard deviation of the waveform histogram.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge and right edge.
8 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.
9 Find the maximum eye height location of the eye diagram.

10 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:

a Set up the parameter of the jitter separation using the EZJIT Plus/Complete Software.

i Load the jitter separation parameter into EZJIT Plus/Complete Software based on the settings in the Configuration Variable.

ii Acquire the signal until 1,000,000 edges are analyzed.

b Note the value of the jitter component from the EZJIT Plus/Complete Software.

11 Create the eye mask based on the following criteria:

a If you select more than one lane (2 lanes or 4 lanes DUT configuration), the eye mask height and width is derate in the following manner, to include crosstalk as defined in DisplayPort 1.4 Compliance Test Specification:

i Eye Mask Width Derate (Crosstalk) = 0.04 UI

ii Eye Mask Height Derate (Crosstalk) = 0.014V

b If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]: eye mask height and width is derate as below to comprehend the noise/jitter extrapolated to BER 10^{-9} for an Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI:

i Calculate the Eye Mask Width Derate (Random Jitter) using the equation:

$$\text{Eye Mask Width Derate (Random Jitter)} = 2.5 * \text{Random Jitter}_{rms}$$

ii Calculate the Eye Mask Height Derate (Random Noise) using the equation:

$$V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{HIGH}\ \text{Random Noise}_{rms}$$

$$V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{LOW}\ \text{Random Noise}_{rms}$$

NOTE The factor 2.5 is the delta between BER 10^{-6} (9.507) and 10^{-9} (11.996) to comprehend the noise/jitter extrapolated to BER 10-9 as the Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI.

BER	N
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996

c Place the eye mask height at the point of the maximum eye height found in Step 9.

d Calculate the Eye Mask Width:

$$\text{Eye Mask Width} = \text{Eye Width Specification (0.38 UI)} + \text{Eye Mask Width Derate (Crosstalk)} + 2 * \text{Eye Mask Width Derate (Random Jitter)}$$

e Calculate the Eye Mask Height:

$$\text{Eye Mask Height} = \{\text{Eye Height Specification (0.09 V)} + \text{Eye Mask Height Derate (Crosstalk)}\}/2 + V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)}$$

$$\text{Eye Mask Height} = -\{\text{Eye Height Specification (0.09 V + Eye Mask Height Derate (Crosstalk)}\}/2 - V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)}$$

12 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram.
   c Run the eye mask until 1,000,000 UI are folded.
13 Measure the eye height of the eye diagram using the Histogram.
14 Measure the jitter of the eye diagram using the Histogram.
15 Calculate the eye width based on the measured jitter of the eye diagram.
16 Check for any signal trajectories that may have entered into the mask.
17 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 153 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 153 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	High (2.7 Gb/s)
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

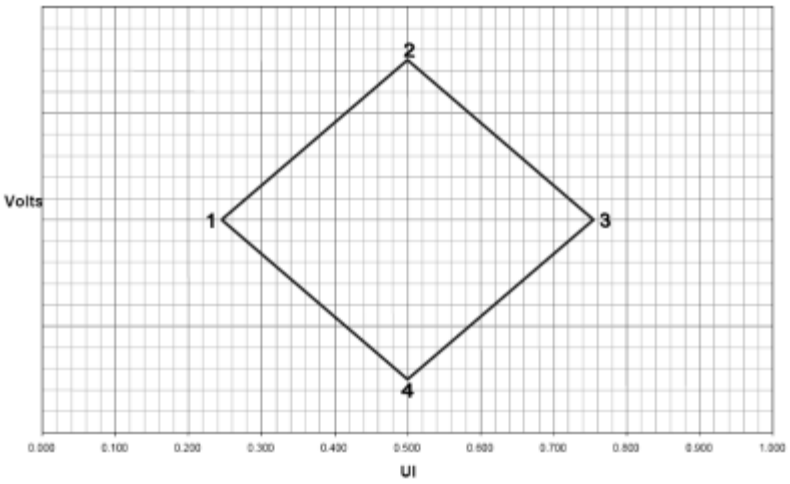


Figure 141 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 154 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.045*
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.045*

NOTE

*Eye height limit of 45 mV and -45 mV assumes cross-talk as 0, which is only possible in case of single lane testing.

In case of multi-lane testing, cross talk exists, and the eye height values deviate by ± 7 mV. Thus the eye height becomes (+45 +7) mV and (-45 -7) mV or +52 mV and -52 mV.

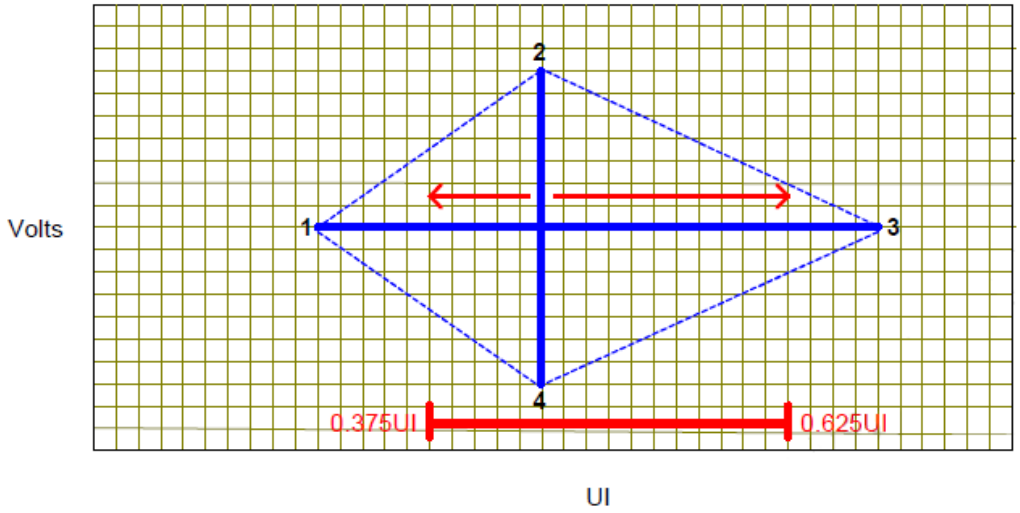


Figure 142 The Eye Mask at TP3_EQ (HBR2 and HBR3)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.1*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2.8.2, Table 3-32 for HBR and Section 3.5.2, Table 3-24 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Eye Diagram Test (TP3_CTLE)

Test ID

For Standard DP Pattern (HBR3):

- 1216001, 1216002, 1216003, 1216004 – Eye Diagram Test (TP3_CTLE)

For Arbitrary Pattern:

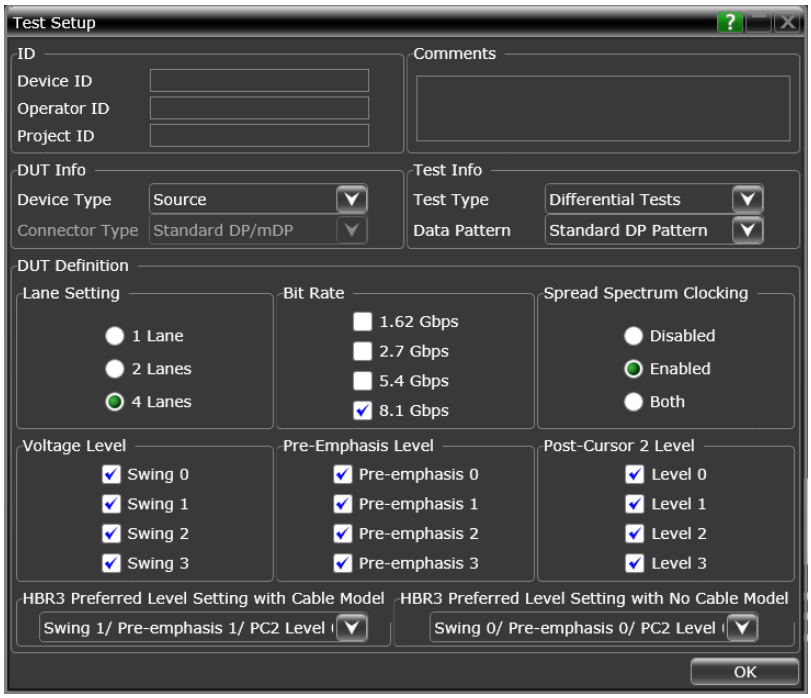
- 1316001, 1316002, 1316003, 1316004 – Eye Diagram Test (TP3_CTLE)

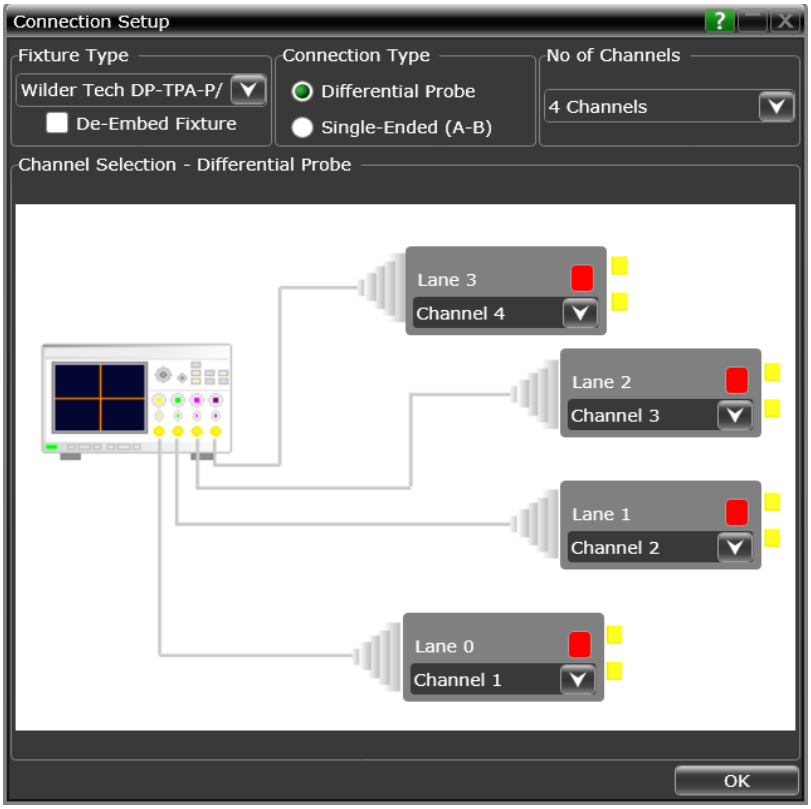
Test Overview

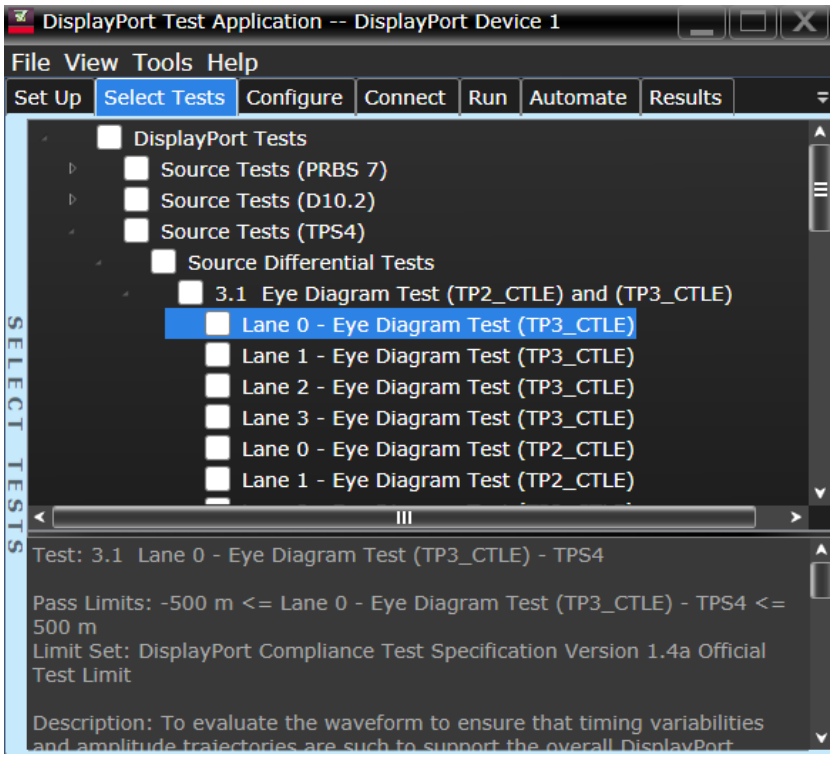
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions for Eye Diagram Test (TP3_CTLE)

Test Parameter	Condition
Test Point	TP3_CTLE
Bit Rate	HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any Voltage Level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	TPS4
Cable Model	“Worst Case”


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure for HBR3

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_CTLE): Use “Worst Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”, exclude the DFE.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.

5 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:
   a Pattern fold the equalized signal based on the High Level Voltage (V_{HIGH}) random noise configuration variable.
   b Set up the vertical waveform histogram on the equalized signal to measure random noise of High Level Voltage (V_{HIGH}).
   c Measure the High Level Voltage (V_{HIGH}) random noise based on the standard deviation of the waveform histogram.
   d Pattern fold the equalized signal based on the Low Level Voltage (V_{LOW}) random noise configuration variable.
   e Set up the vertical waveform histogram on the equalized signal to measure the random noise of Low Level Voltage (V_{LOW}).
   f Measure the Low Level Voltage (V_{LOW}) random noise based on the standard deviation of the waveform histogram.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge and right edge.
8 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.
9 Find the maximum eye height location of the eye diagram.
10 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:
   a Set up the parameter of the jitter separation using the EZJIT Plus/Complete Software.
      i Load the jitter separation parameter into EZJIT Plus/Complete Software based on the settings in the Configuration Variable.
      ii Acquire the signal until 2 million edges are analyzed.
   b Note the value of the jitter component from the EZJIT Plus/Complete Software.
11 Create the eye mask based on the following criteria:
   a If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]: eye mask height and width is derate as below to comprehend the noise/jitter extrapolated to BER 10^{-9} for an Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI:
      i Calculate the Eye Mask Width Derate (Random Jitter) using the equation:

$$\text{Eye Mask Width Derate (Random Jitter)} = 2.5 * \text{Random Jitter}_{rms}$$

      ii Calculate the Eye Mask Height Derate (Random Noise) using the equation:

$$V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{HIGH}\ \text{Random Noise}_{rms}$$

$$V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{LOW}\ \text{Random Noise}_{rms}$$

NOTE The factor 2.5 is the delta between BER 10^{-6} (9.507) and 10^{-9} (11.996) to comprehend the noise/jitter extrapolated to BER 10-9 as the Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI.

BER	N
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996

c Place the eye mask height at the point of the maximum eye height found in Step 9.

d Calculate the Eye Mask Width:

Eye Mask Width = Eye Width Specification + 2 * Eye Mask Width Derate (Random Jitter)

e Calculate the Eye Mask Height:

Eye Mask Height = {Eye Height Specification}/2 + V_{HIGH} Eye Mask Height Derate (Random Noise)

Eye Mask Height = -{Eye Height Specification}/2 - V_{LOW} Eye Mask Height Derate (Random Noise)

12 Set up the parameters for the Mask Test.

a Load the eye mask based on the settings in the Configuration Variable.

b Center the eye mask at the middle of the eye diagram.

c Run the eye mask until 2 million UI are folded.

13 Measure the eye height of the eye diagram using the Histogram.

14 Measure the jitter of the eye diagram using the Histogram.

15 Calculate the eye width based on the measured jitter of the eye diagram.

16 Check for any signal trajectories that may have entered into the mask.

17 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 153 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 155 Eye Diagram Mask Coordinates for TP3_CTLE (HBR3)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.53 UI	0.00000
2	Any passing UI location between 0.375 and 0.625 UI	0.0325
3	Point 1 + 0.53 UI	0.00000
4	Same as Point 2	-0.0325

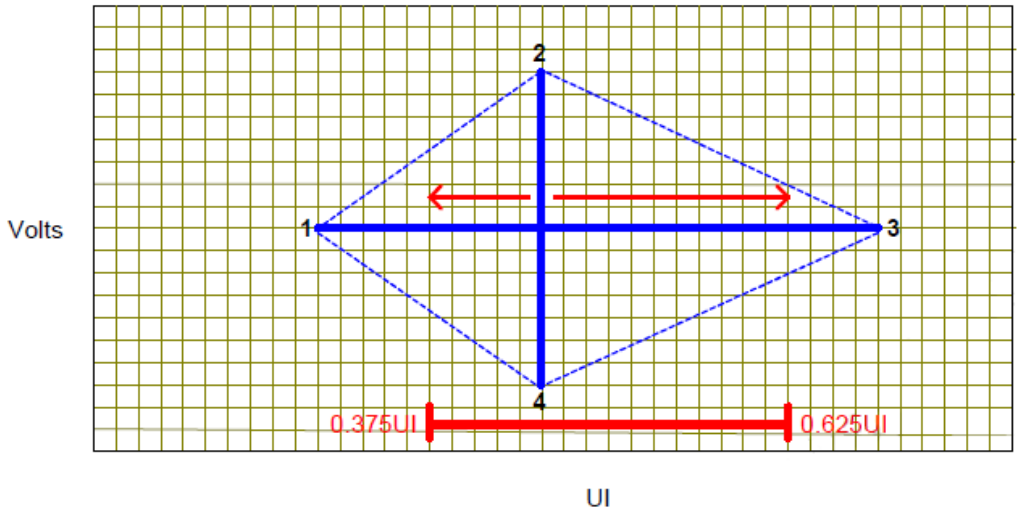


Figure 143 The Eye Mask at TP3_CTLE (HBR3)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.1*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2 and Table 3-23 for HBR3*

Expected/Observable Results

The measured eye diagram for the test signal at TP3_CTLE shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Eye Diagram Test (TP2_CTLE) (Informative)

Test ID

For Standard DP Pattern (HBR3):

- 1216011, 1216012, 1216013, 1216014 – Eye Diagram Test (TP2_CTLE)

For Arbitrary Pattern:

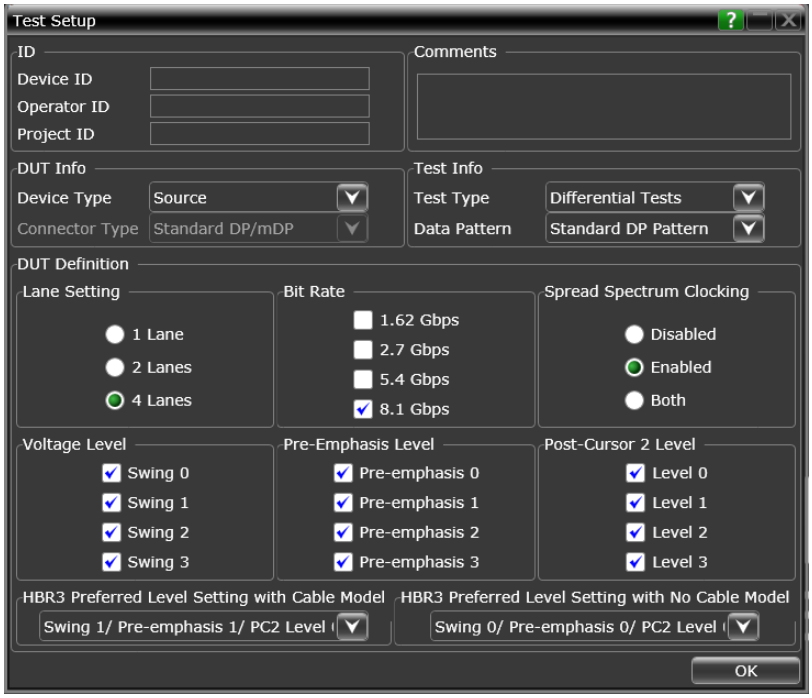
- 1316011, 1316012, 1316013, 1316014 – Eye Diagram Test (TP2_CTLE)

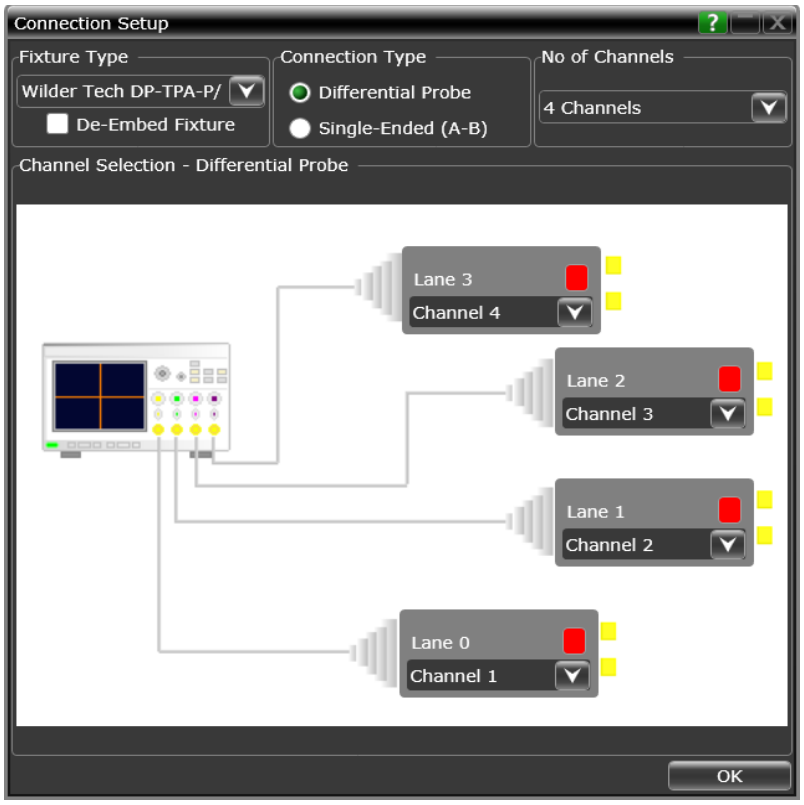
Test Overview

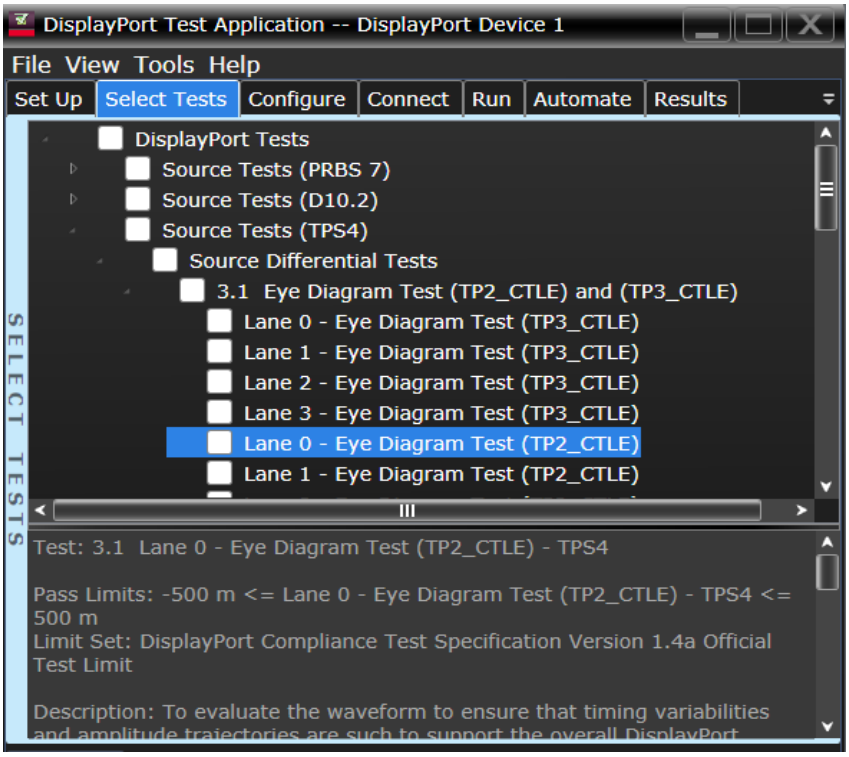
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions for Eye Diagram Test (TP2_CTLE)

Test Parameter	Condition
Test Point	TP2_CTLE
Bit Rate	HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any Voltage Level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	TPS4
Cable Model	“Zero Length”


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure for HBR3

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP2_CTLE): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”, exclude the DFE.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.

5 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:
   a Pattern fold the equalized signal based on the High Level Voltage (V_{HIGH}) random noise configuration variable.
   b Set up the vertical waveform histogram on the equalized signal to measure random noise of High Level Voltage (V_{HIGH}).
   c Measure the High Level Voltage (V_{HIGH}) random noise based on the standard deviation of the waveform histogram.
   d Pattern fold the equalized signal based on the Low Level Voltage (V_{LOW}) random noise configuration variable.
   e Set up the vertical waveform histogram on the equalized signal to measure the random noise of Low Level Voltage (V_{LOW}).
   f Measure the Low Level Voltage (V_{LOW}) random noise based on the standard deviation of the waveform histogram.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge and right edge.
8 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.
9 Find the maximum eye height location of the eye diagram.
10 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:
   a Set up the parameter of the jitter separation using the EZJIT Plus/Complete Software.
      i Load the jitter separation parameter into EZJIT Plus/Complete Software based on the settings in the Configuration Variable.
      ii Acquire the signal until 2 million edges are analyzed.
   b Note the value of the jitter component from the EZJIT Plus/Complete Software.
11 Create the eye mask based on the following criteria:
   a If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]: eye mask height and width is derate as below to comprehend the noise/jitter extrapolated to BER 10^{-9} for an Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI:
      i Calculate the Eye Mask Width Derate (Random Jitter) using the equation:

$$\text{Eye Mask Width Derate (Random Jitter)} = 2.5 * \text{Random Jitter}_{rms}$$

      ii Calculate the Eye Mask Height Derate (Random Noise) using the equation:

$$V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{HIGH}\ \text{Random Noise}_{rms}$$

$$V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{LOW}\ \text{Random Noise}_{rms}$$

NOTE The factor 2.5 is the delta between BER 10^{-6} (9.507) and 10^{-9} (11.996) to comprehend the noise/jitter extrapolated to BER 10-9 as the Eye Diagram Test (TP2_CTLE) only acquiring 1e6 UI.

BER	N
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996

c Place the eye mask height at the point of the maximum eye height found in Step 9.

d Calculate the Eye Mask Width:

Eye Mask Width = Eye Width Specification + 2 * Eye Mask Width Derate (Random Jitter)

e Calculate the Eye Mask Height:

Eye Mask Height = {Eye Height Specification}/2 + V_{HIGH} Eye Mask Height Derate (Random Noise)

Eye Mask Height = -{Eye Height Specification}/2 - V_{LOW} Eye Mask Height Derate (Random Noise)

12 Set up the parameters for the Mask Test.

a Load the eye mask based on the settings in the Configuration Variable.

b Center the eye mask at the middle of the eye diagram.

c Run the eye mask until 2 million UI are folded.

13 Measure the eye height of the eye diagram using the Histogram.

14 Measure the jitter of the eye diagram using the Histogram.

15 Calculate the eye width based on the measured jitter of the eye diagram.

16 Check for any signal trajectories that may have entered into the mask.

17 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 153 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 156 Eye Diagram Mask Coordinates for TP2_CTLE (HBR3)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.67UI	0.00000
2	Any passing UI location between 0.375 and 0.625UI	0.0325
3	Point 1 + 0.67UI	0.00000
4	Same as Point 2	-0.0325

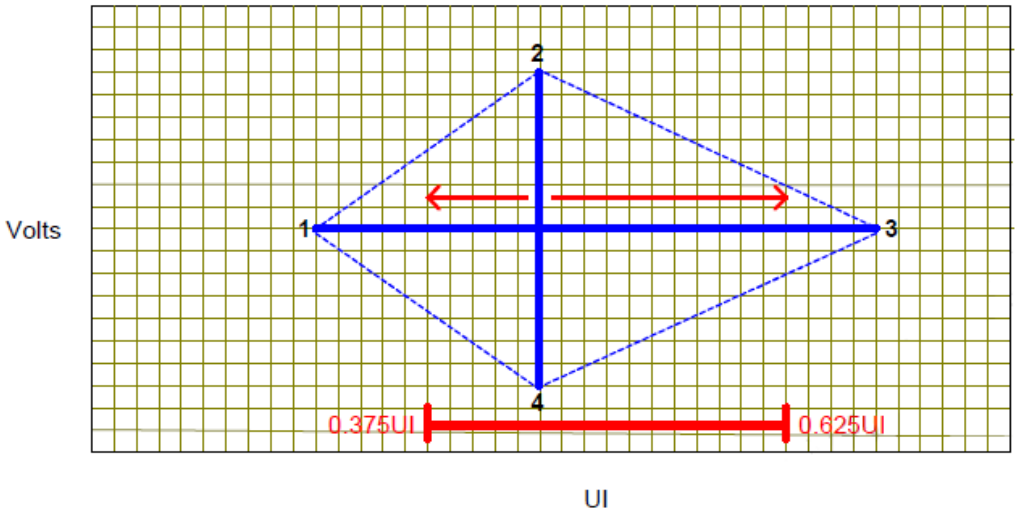


Figure 144 The Eye Mask at TP2_CTLE (HBR3)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.1*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2 and Table 3-23 for HBR3*

Expected/Observable Results

The measured eye diagram for the test signal at TP2_CTLE shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Eye Diagram Test (TP3_DFE) (VESA DFE Tool)

Test ID

For Standard DP Pattern (HBR3):

- 1218001, 1218002, 1218003, 1218004 - Eye Diagram Test (TP3_DFE)

For Arbitrary Pattern:

- 1318001, 1318002, 1318003, 1318004 - Eye Diagram Test (TP3_DFE)

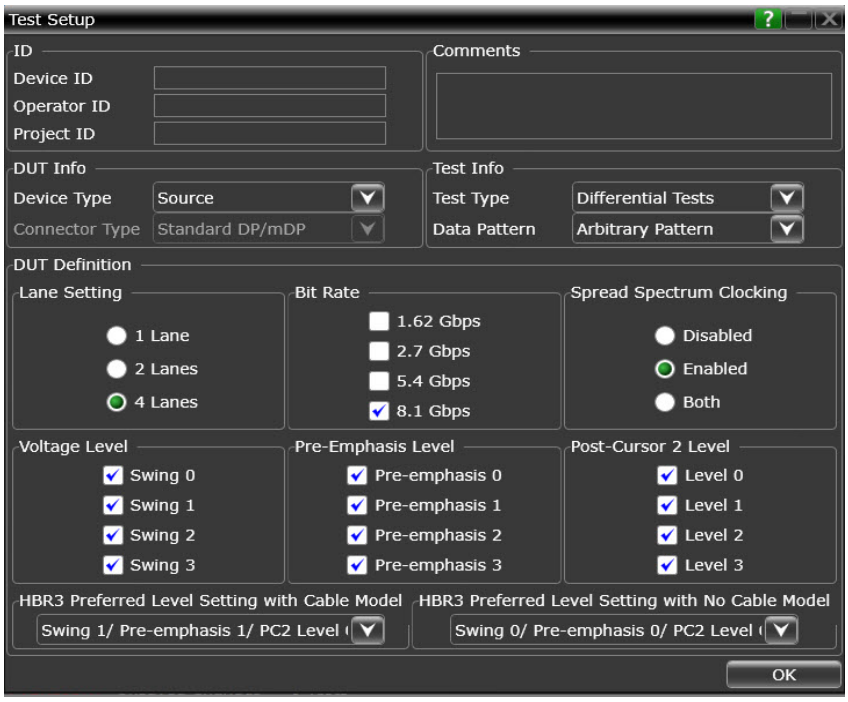
Test Overview

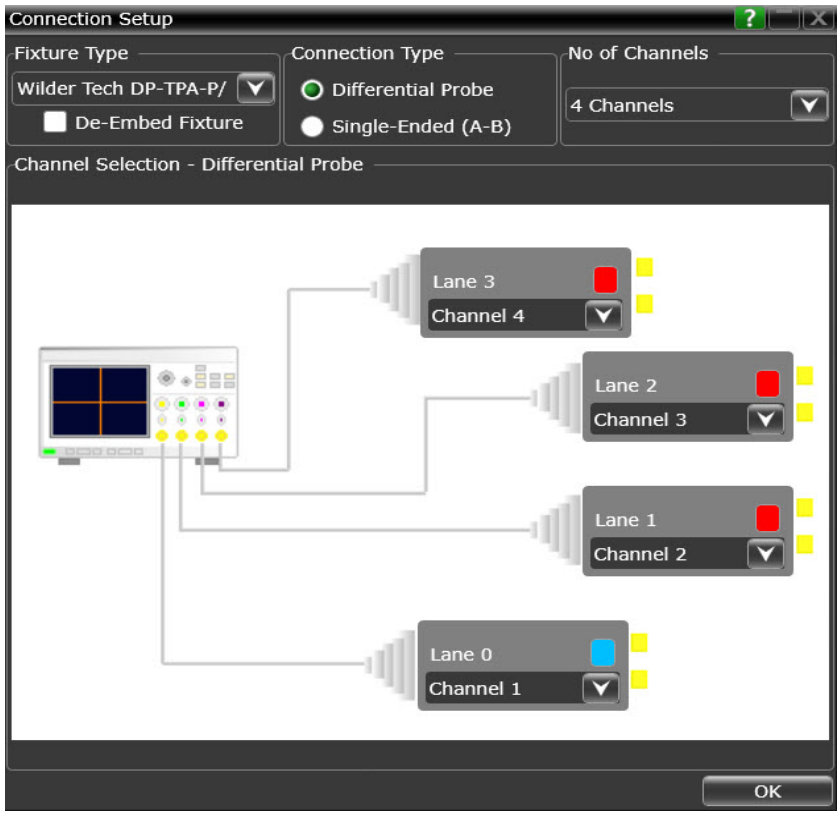
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

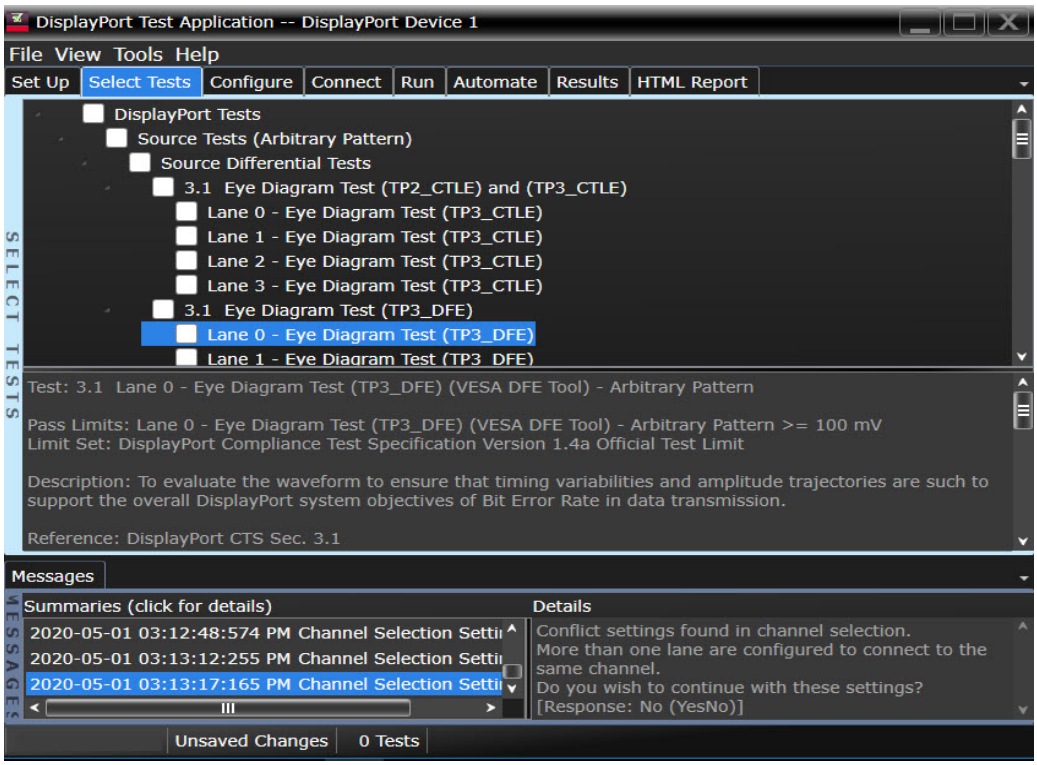
Test Conditions for Eye Diagram Test (TP3_DFE)

Test Parameter	Condition
Test Point	TP3_DFE
Bit Rate	HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any Voltage Level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	TPS4
Cable Model	“Worst Case”

NOTE The Eye Diagram Test (TP3_DFE) will only run if the Eye Diagram Test (TP3_CTLE) fails. The user must manually download the VESA DP Eye Test tool from VESA website.


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Arbitrary Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure for HBR3

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_DFE): Use “Worst Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”, exclude DFE.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Sweep the CTLE DC gain to generate different equalized signal
   a Generate the recovered clock for the given equalized signal.
   b Save both the waveform for equalized signal and recovered clock.
5 Load all the waveforms into the VESA DP Eye Test Tool and generate the eye height and eye width for different CTLE DC gain with DFE.
6 Report the optimum CTLE DC gain that will generate the highest eye height at TP3_DFE and measurement result.

PASS Condition

Eye Height at TP3_DFE with optimum CTLE DC Gain >= 100 mV

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1*, Section 3.1

Expected/Observable Results

The measured eye height for the optimum CTLE DC gain shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

Source Total Jitter Test (TP3_EQ)

Test ID

For Standard DP Pattern:

- 1225001, 1225002, 1225003, 1225004 – Total Jitter Test (TP3_EQ) - PRBS 7
- 1225011, 1225012, 1225013, 1225014 – Total Jitter Test with No Cable Model (TP3_EQ) - PRBS 7
- 1222001, 1222002, 1222003, 1222004 – Total Jitter Test (TP3_EQ) - HBR2CPAT
- 1222011, 1222012, 1222013, 1222014 – Total Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1221001, 1221002, 1221003, 1221004 – Total Jitter Test (TP3_EQ) - D10.2
- 1221011, 1221012, 1221013, 1221014 – Total Jitter Test with No Cable Model (TP3_EQ) - D10.2

For Arbitrary Pattern:

- 1322001, 1322002, 1322003, 1322004 – Total Jitter Test (TP3_EQ)
- 1322011, 1322012, 1322013, 1322014 – Total Jitter Test with No Cable Model (TP3_EQ)

Test Overview

The objective of this test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

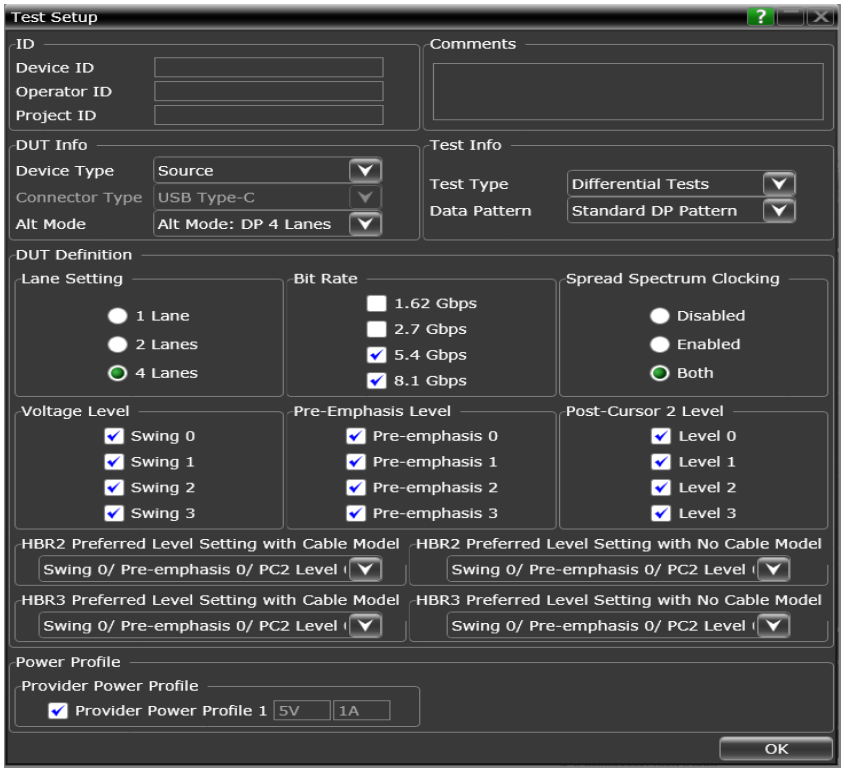
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

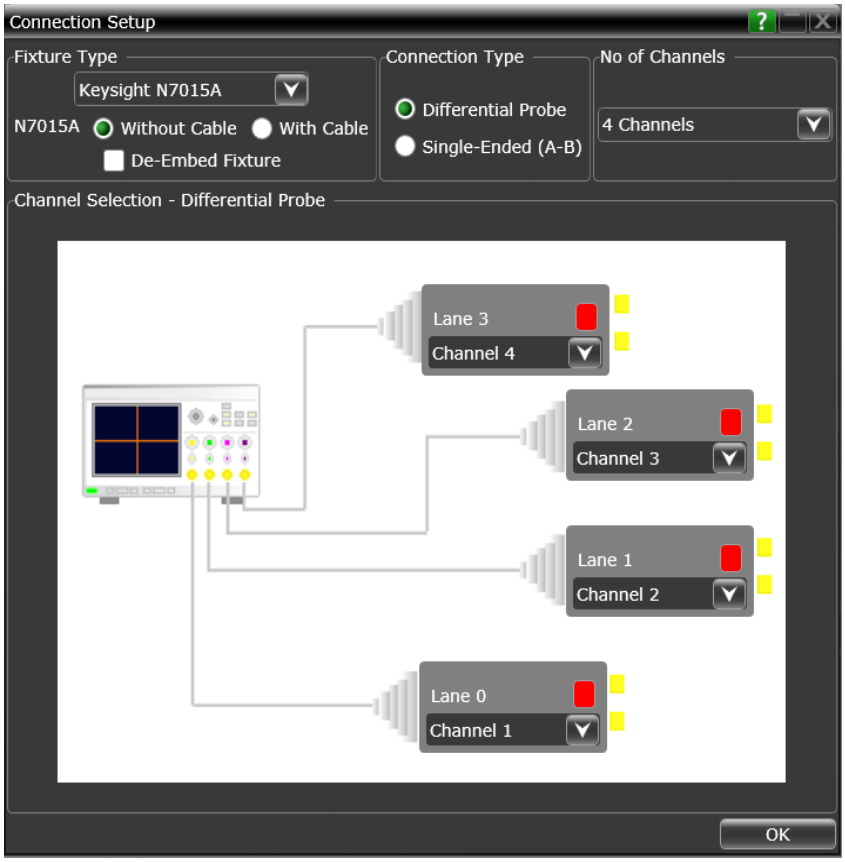
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

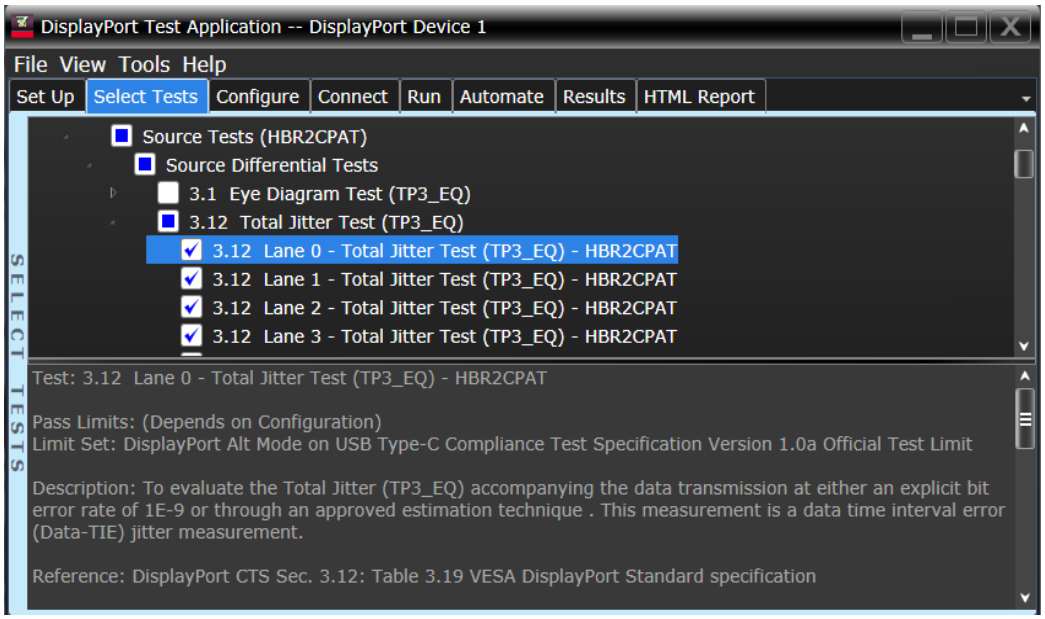
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR (Informative) and HBR2
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	HBR: PRBS7, HBR2: D10.2 and HBR2CPAT
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Total Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Total Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 157 Total Jitter at TP3_EQ

	Receiver Connector (TP3_EQ)
High-Bite Rate 2 (5.4 Gb/s per lane) - for D10.2 pattern	
A_{p-p}	≤ 0.40 UI
High-Bit Rate 2 (5.4 Gb/s per lane) - for HBR2CPAT (or CP2520) pattern	
A_{p-p}	≤ 0.580 UI*
High-Bite Rate (2.7 Gb/s per lane) - for PRBS7	
A_{p-p}	≤ 0.491 UI

The HBR2 limits for Total Jitter calculated at TP3_EQ include a de-rating of 0.04 UI to account for cable crosstalk effect.

UI is Unit Interval.

Test References

See:

For HBR (PRBS7)

- VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.1
- VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2.7.2, Table 3-23.

For HBR2 (HBR2CPAT)

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.1*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-24*

For HBR2 (D10.2)

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.3*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*

Expected/Observable Results

The measured total jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Total Jitter Test (TP2_CTLE (Informative) and TP3_CTLE)

Test ID

For Standard DP Pattern:

- 1223001, 1223002, 1223003, 1223004 – Total Jitter Test (TP3_CTLE) - TPS4
- 1223011, 1223012, 1223013, 1223014 – Total Jitter Test (TP2_CTLE) - TPS4

For Arbitrary Pattern:

- 1323001, 1323002, 1323003, 1323004 – Total Jitter Test (TP3_CTLE)
- 1323011, 1323012, 1323013, 1323014 – Total Jitter Test (TP2_CTLE)

Test Overview

The objective of this test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-6} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

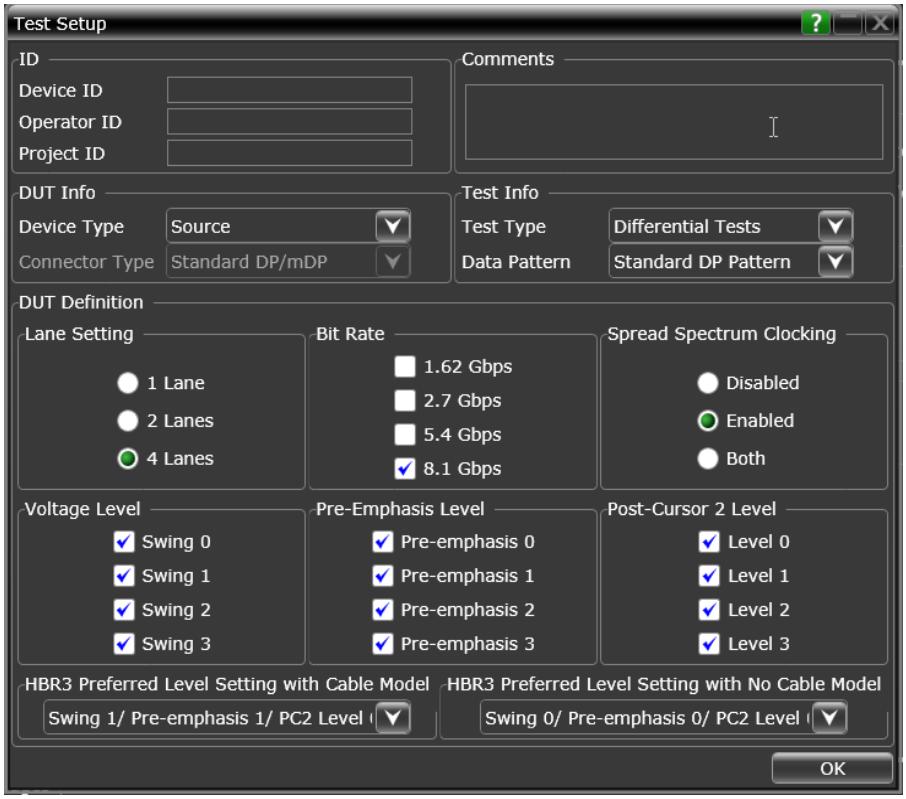
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-6} BER based on the Dual-Dirac Model:

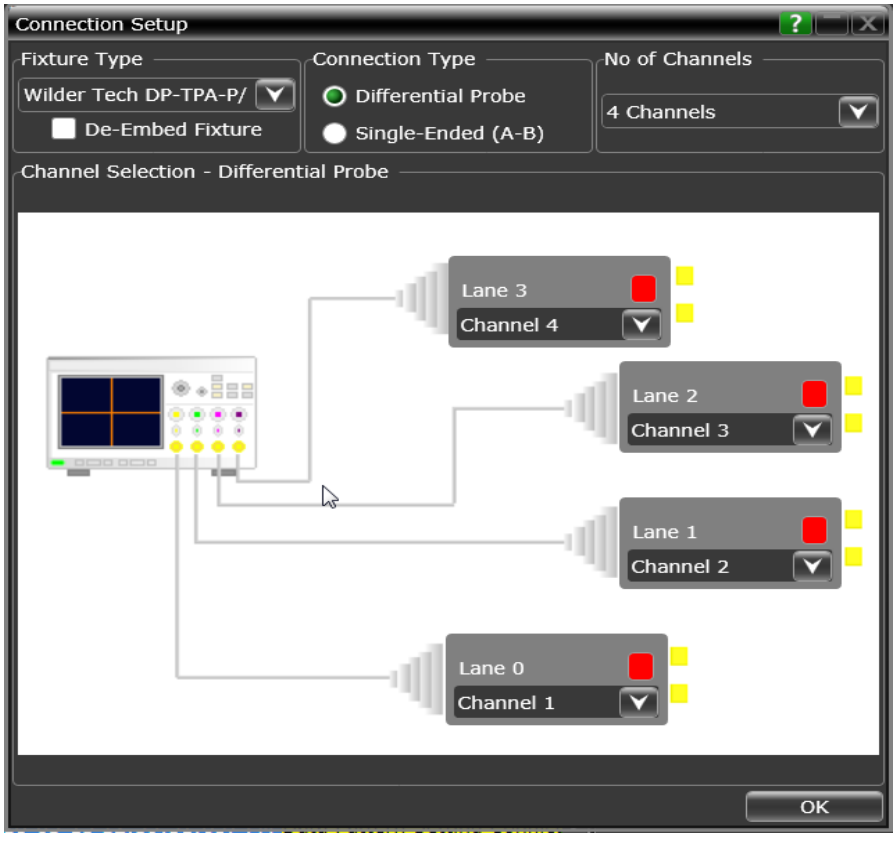
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

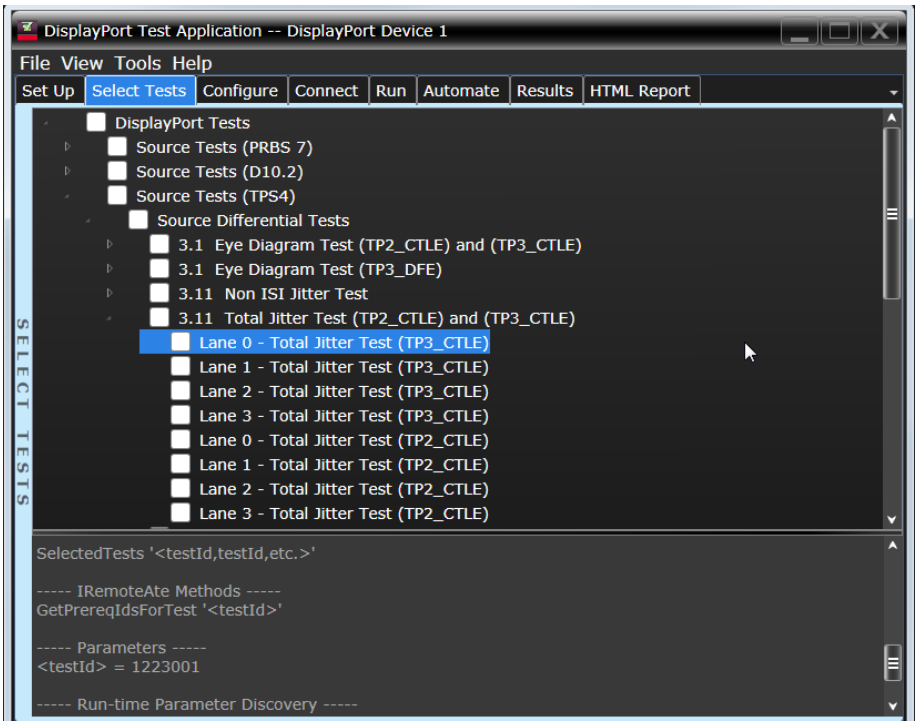
where,
DJ is the Deterministic Jitter and RJ is the Random Jitter.

Test Conditions for Total Jitter Test (TP2_CTLE and TP3_CTLE)

Test Parameter	Condition
Test Point	HBR3: TP3_CTLE HBR3: TP2_CTLE (Informative)
Bit Rate	HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	TPS4
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Total Jitter Test (TP3_CTLE): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Total Jitter Test (TP2_CTLE): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”, exclude the DFE.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 2 million UI edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 158 Total Jitter at TP3_CTLE

	Receiver Connector
High-Bite Rate 3 (8.1 Gb/s per lane)	
A_{p-p}	≤ 0.47 UI

Table 159 Total Jitter at TP2_CTLE

	Receiver Connector (TP2_CTLE)
High-Bit Rate 3 (8.1 Gb/s per lane)	
A_{p-p}	≤ 0.33 UI

UI is Unit Interval.

Test References

See:

For HBR3 (TPS4 pattern)

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.1*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-23*

Expected/Observable Results

The measured total jitter for the test signal at TP3_CTLE and TP2_CTLE shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non ISI Jitter Test (TP2_CTLE (Informative) and TP3_CTLE)

Test ID

For Standard DP Pattern:

- 1234001, 1234002, 1234003, 1234004 – Non ISI Jitter Test (TP3_CTLE) - TPS4
- 1234011, 1234012, 1234013, 1234014 – Non ISI Jitter Test (TP2_CTLE) - TPS4

For Arbitrary Pattern:

- 1334001, 1334002, 1334003, 1334004 – Non ISI Jitter Test (TP3_CTLE)
- 1334011, 1334012, 1334013, 1334014 – Non ISI Jitter Test (TP2_CTLE)

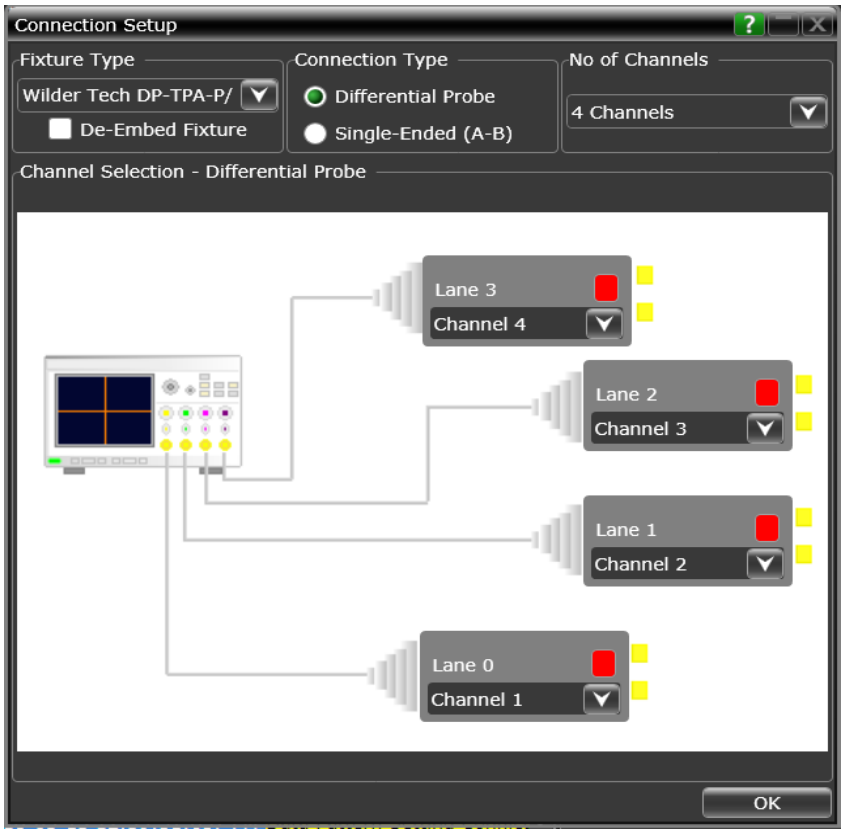
Test Overview

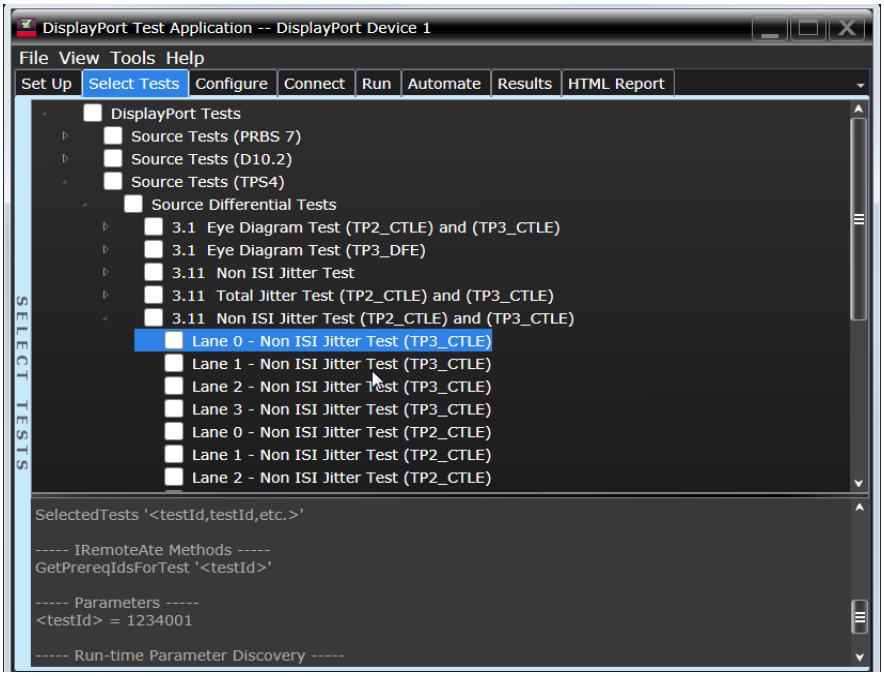
The objective of this test is to evaluate the non ISI jitter accompanying the data transmission.

Test Conditions for Non ISI Jitter Test (TP2_CTLE and TP3_CTLE)

Test Parameter	Condition
Test Point	TP2_CTLE (Informative) and TP3_CTLE
Bit Rate	HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	TPS4
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Non ISI Jitter Test (TP3_CTLE): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Non ISI Jitter Test (TP2_CTLE): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”, exclude the DFE.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 2 million UI edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.

7 Calculate the non ISI jitter base on following equation:
Non ISI Jitter = TJ - ISI

8 Report the measurement results.

PASS Condition

Table 160 Non ISI Jitter at TP3_CTLE

	Receiver Connector (TP3_CTLE)
High-Bit Rate 3 (8.1 Gb/s per lane)	
A_{p-p}	≤0.23 UI

Table 161 Non ISI Jitter at TP2_CTLE

	Receiver Connector (TP2_CTLE)
High-Bit Rate 3 (8.1 Gb/s per lane)	
A_{p-p}	≤0.23 UI

UI is Unit Interval.

See:

- VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.2
- VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-23

Expected/Observable Results

The measured non ISI jitter for the test signal at TP2_CTLE and TP3_CTLE shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Deterministic Jitter Test (TP3_EQ)

Test ID

For Standard DP Pattern:

- 1236001, 1236002, 1236003, 1236004 – Deterministic Jitter Test (TP3_EQ) - HBR2CPAT
- 1236011, 1236012, 1236013, 1236014 – Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1235001, 1235002, 1235003, 1235004 – Deterministic Jitter Test (TP3_EQ) - D10.2
- 1235011, 1235012, 1235013, 1235014 – Deterministic Jitter Test with No Cable Model (TP3_EQ) - D10.2

For Arbitrary Pattern:

- 1336001, 1336002, 1336003, 1336004 – Deterministic Jitter Test (TP3_EQ)
- 1336011, 1336012, 1336013, 1336014 – Deterministic Jitter Test with No Cable Model (TP3_EQ)

Test Overview

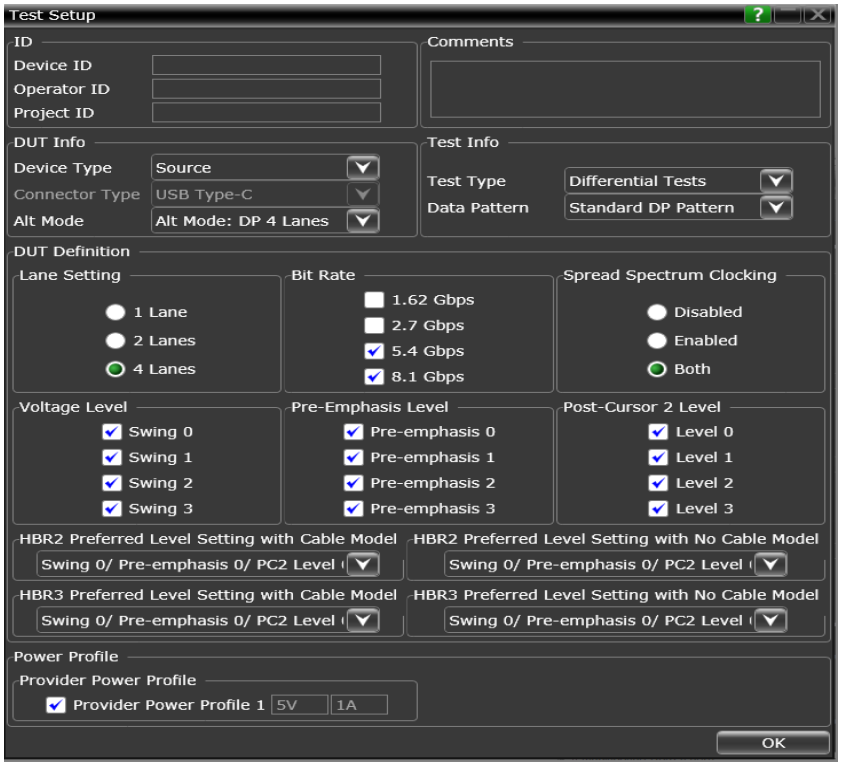
The objective of this test is to evaluate the deterministic jitter accompanying the data transmission. The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

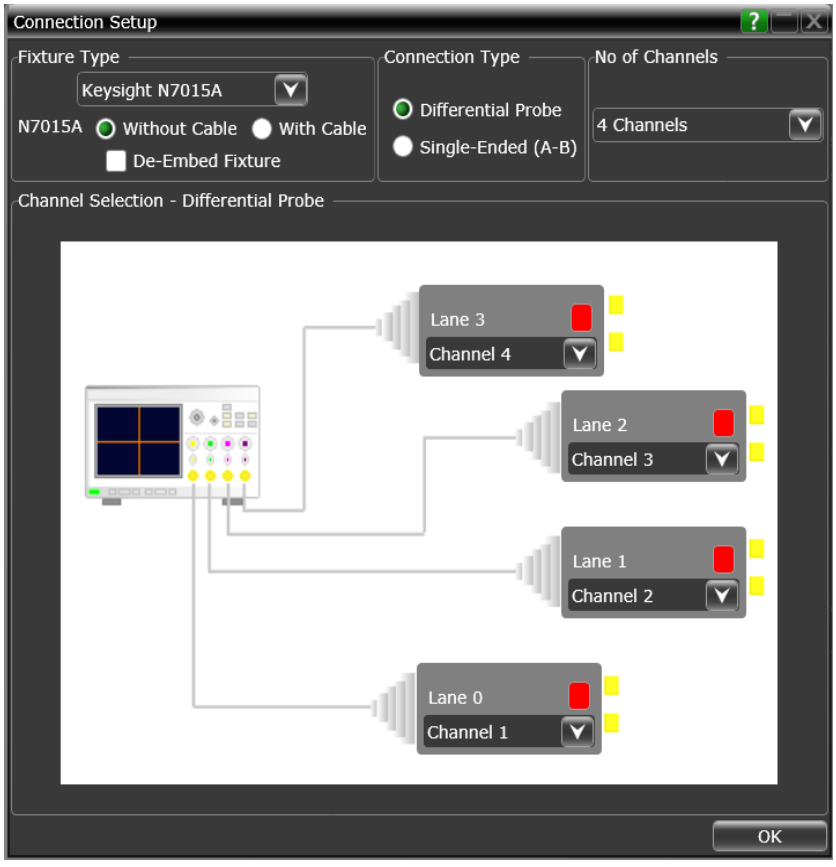
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

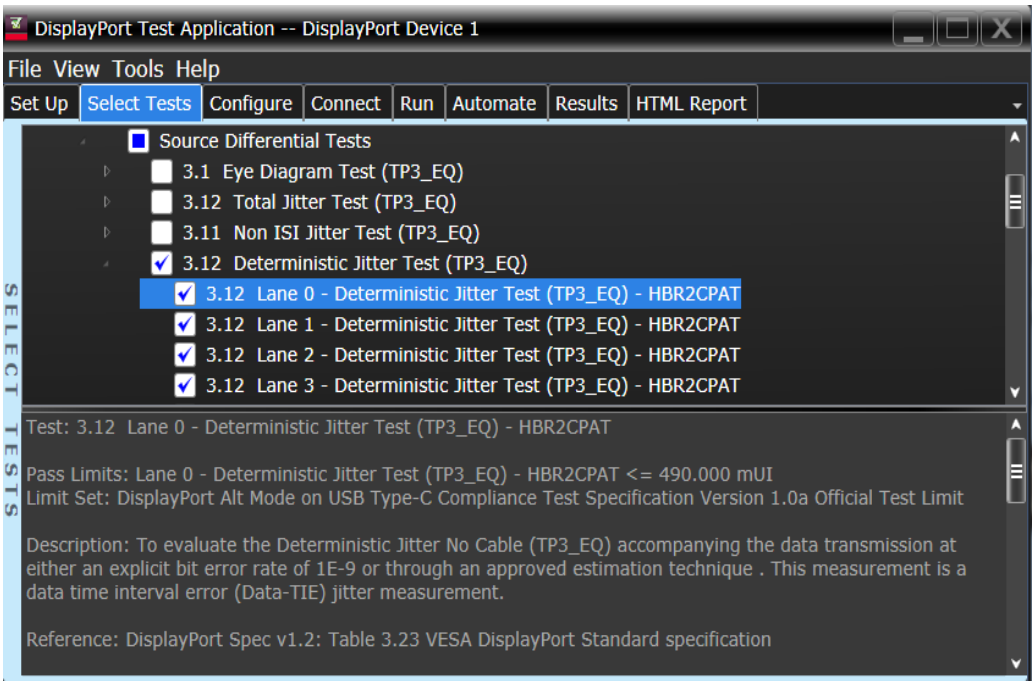
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Deterministic Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Deterministic Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Deterministic Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 162 Deterministic Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.49 UI

Table 163 Deterministic Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.27 UI

UI is Unit Interval.

Test References

See:

For HBR2CPAT

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*

For D10.2

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.3*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*

Expected/Observable Results

The measured deterministic jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Random Jitter Test (TP3_EQ)

Test ID

For Standard DP Pattern:

- 1238001, 1238002, 1238003, 1238004 – Random Jitter Test (TP3_EQ) - D10.2
- 1238011, 1238012, 1238013, 1238014 – Random Jitter Test with No Cable Model (TP3_EQ) - D10.2

For Arbitrary Pattern:

- 1338001, 1338002, 1338003, 1338004 – Random Jitter Test (TP3_EQ)
- 1338011, 1338012, 1338013, 1338014 – Random Jitter Test with No Cable Model (TP3_EQ)

Test Overview

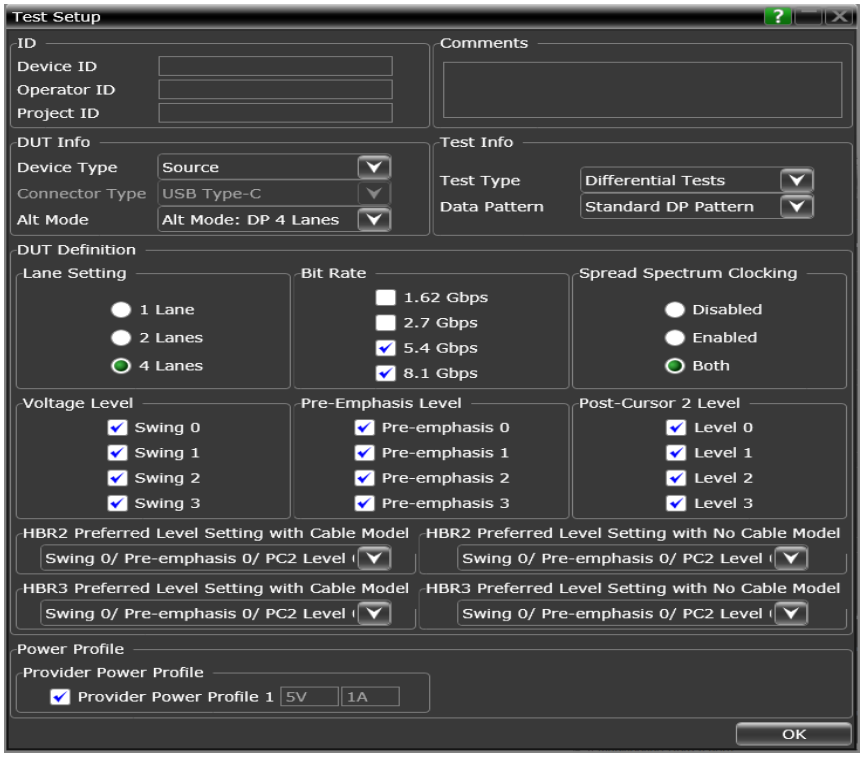
The objective of this test is to evaluate the random jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. The jitter is separated into each jitter components and the random jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

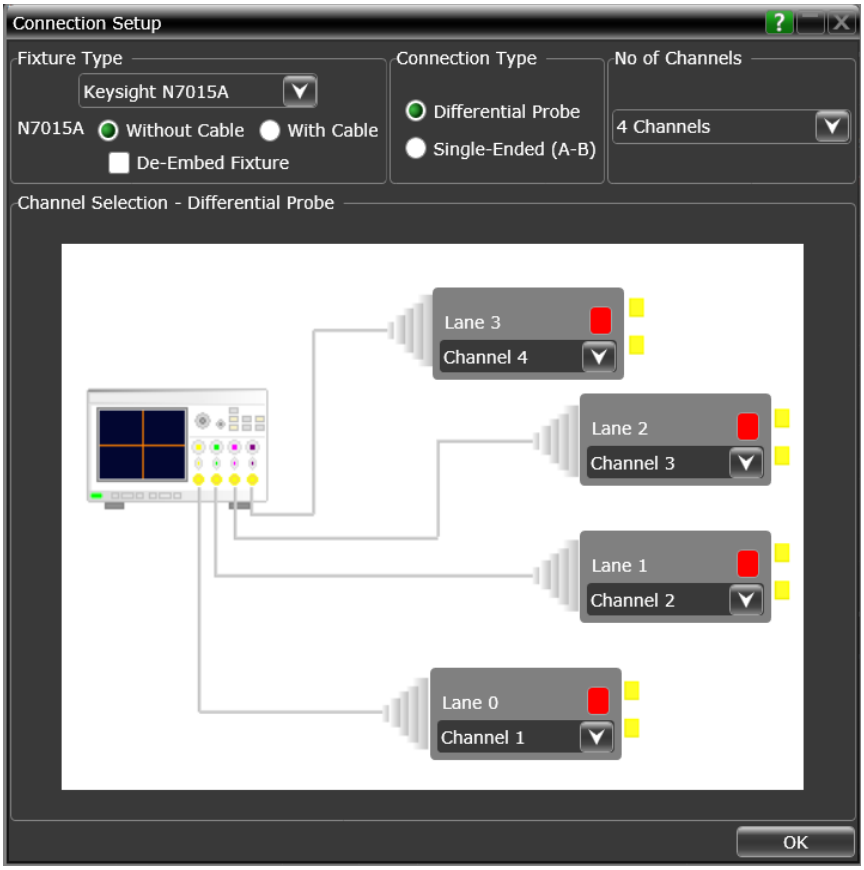
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

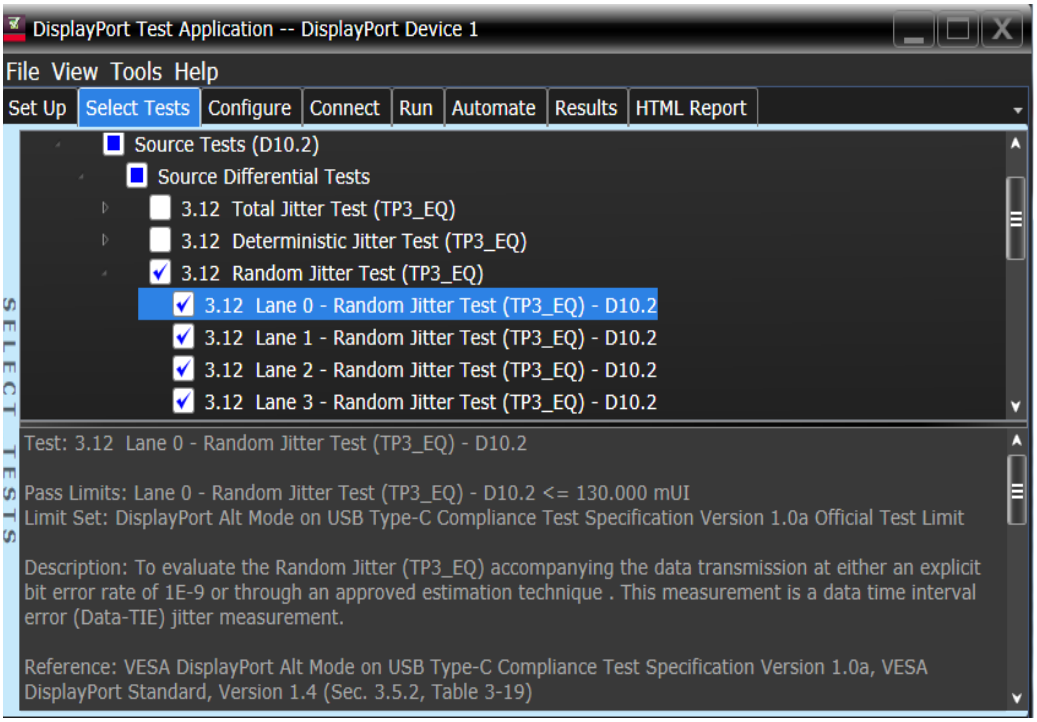
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Random Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	D10.2
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Random Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Random Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 164 Random Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.2304 UI*

UI is Unit Interval.
*Calculated based on RJ_{rms} = 19.2 mUI

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.11.3*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*
- VESA DisplayPort (DP) Standard Version 1.4a, HBR2 Rj SCR

Expected/Observable Results

The measured random jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Low Frequency Uncorrelated Deterministic Jitter Test (Informative)

Test ID

For Standard DP Pattern:

- 1239001, 1239002, 1239003, 1239004 – Low Frequency Uncorrelated Deterministic Jitter Test (Informative)

For Arbitrary Pattern:

- 1339001, 1339002, 1339003, 1339004 – Low Frequency Uncorrelated Deterministic Jitter Test (Informative)

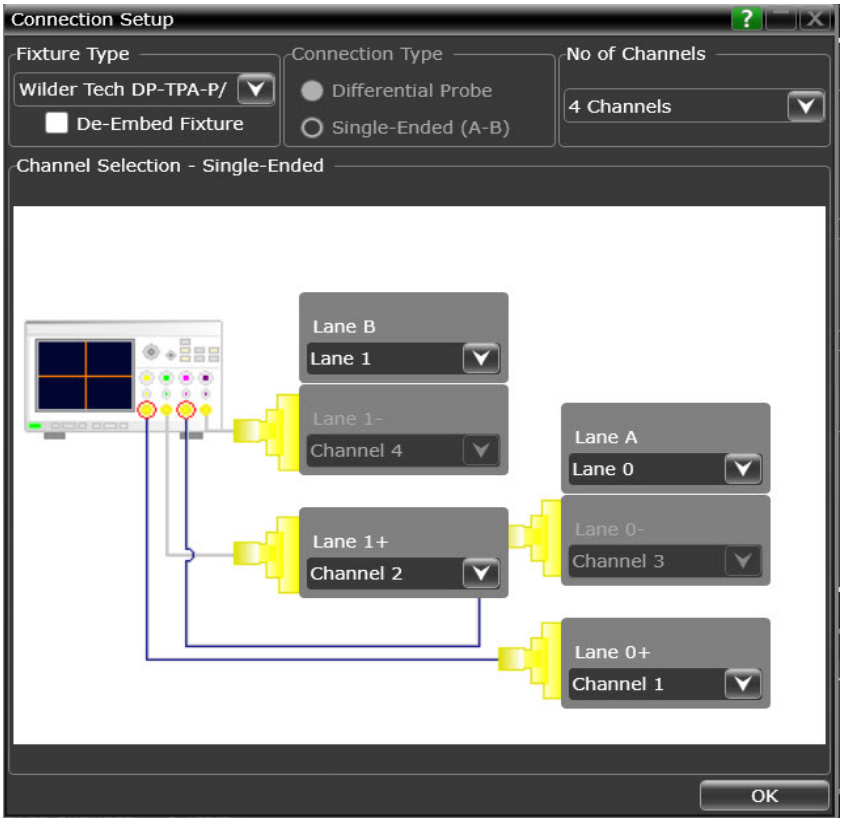
Test Overview

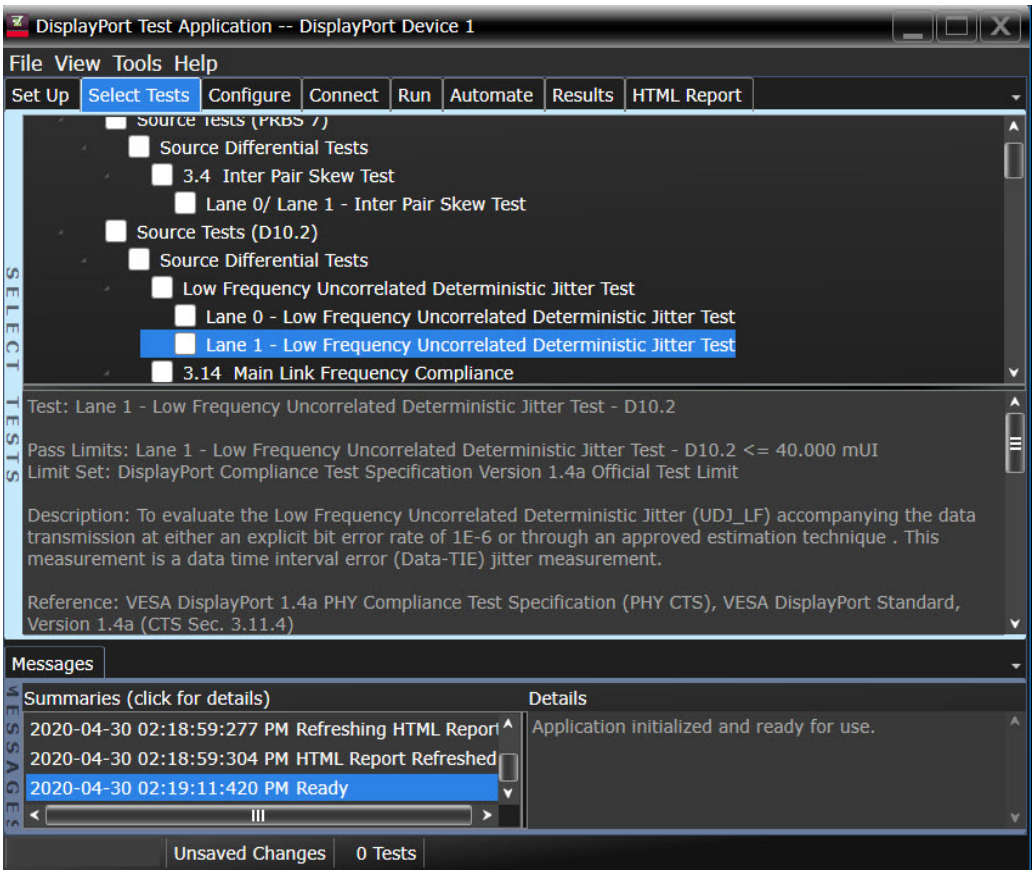
The objective of this test is to confirm that the transmitter low frequency uncorrelated deterministic jitter falls within the limits.

Test Conditions for Low Frequency Uncorrelated Deterministic Jitter Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Any Voltage Level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Both
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



NOTE

Acquisition length is set to capture 10 cycles of SSC at 30KHz. For 80 GSa/s sample rate, acquisition length shall be set to 27 MSa. For 100 GSa/s sample rate, acquisition length shall be 34 MSa.

The recommended maximum memory depth for UXR oscilloscope is 48M and for 90000 series and others is 30M.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.

4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable
   b Apply low pass filter (2^{nd} order, 3 dB cut-off at 500 KHz) to TIE data
   c UDJ_LF = measured TJ after low pass filter applied
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Report the measurement results. UDJ_LF is the measured TJ after applying low pass filter.

PASS Condition

Table 165 Low Frequency Uncorrelated Deterministic Jitter at Internal and Compliance Points.

	Transmitter Connector (TP2)
High-bit Rate (8.1 Gb/s per lane)	
$A_{p\text{-}pTX}$	40.0 mUI

UI stands for Unit Interval.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1*, Section 3.11.4.

Expected/Observable Results

The measured low frequency uncorrelated deterministic jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source AC Common Mode Test (Informative)

Test ID

For Standard DP Pattern:

- 12110001, 12110002, 12110003, 12110004 – AC Common Mode Test (Informative)

For Arbitrary Pattern:

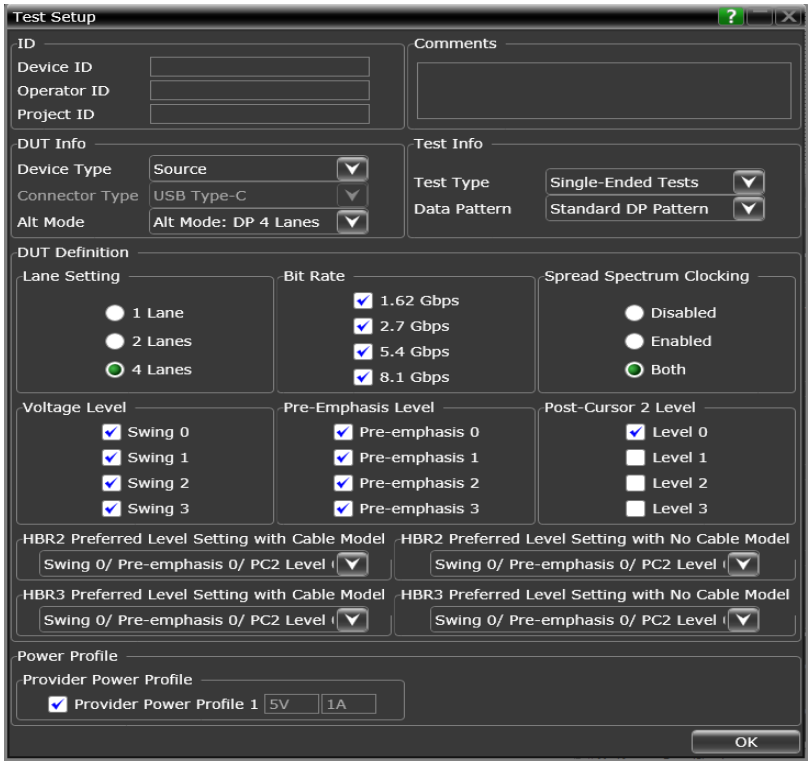
- 13110001, 13110002, 13110003, 13110004 – AC Common Mode Test (Informative)

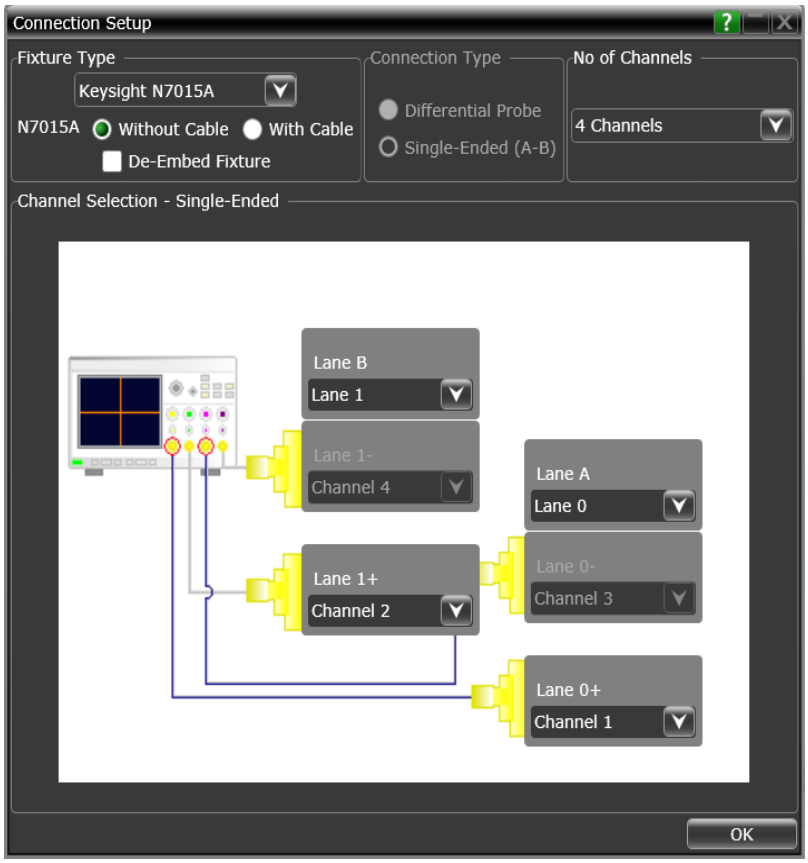
Test Overview

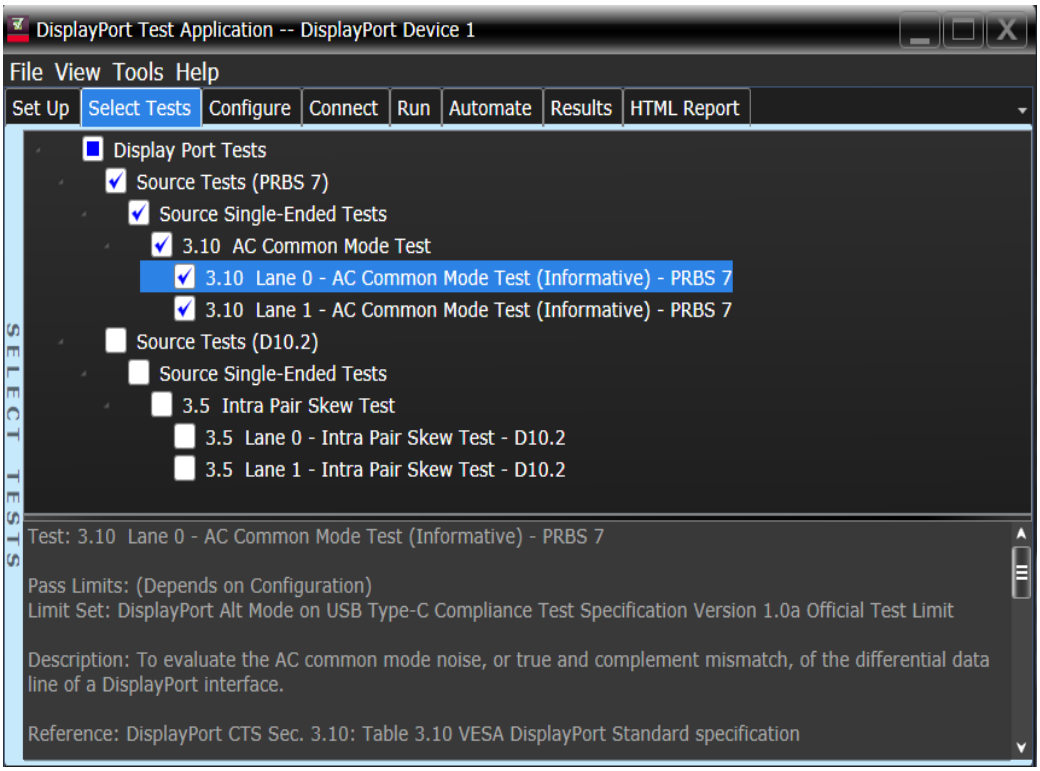
The objective of this test is to evaluate the AC Common Mode noise (unfiltered rms) of the differential data line of the DP interface.

Test Conditions for AC Common Mode Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR, and HBR2
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC enabled only.
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels supported subject to the constraints in Table 3-1 of the VESA DisplayPort 1.4a Standard
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Single-Ended Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Create FUNC3 signal, which is the common mode signal of the input single-ended signal.
4 If the filter is enabled ["Filter" configuration variable set to "High Pass Filter", "Low Pass Filter" or "None" (Default)]:
   a Create FUNC4 signal, which is the filtered FUNC3 signal by applying the High Pass filter or Low Pass filter on the FUNC3 signal based on the Configuration Variable.
5 Set up two display grids such that one grid displays the input single-ended signal while the other grid displays the common mode signal.
6 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.

7 Set up the parameters for RMS voltage measurement of the common mode signal.
   a Set up the V_{rms} measurement for the common mode signal.
   b Acquire the signal until 100,000 edges are measured.
8 Get the mean for the V_{rms} measurement.
9 Report the measurement results.

PASS Condition

For RBR and HBR:

AC Common Mode Voltage $\leq$ 20mV

For HBR2 and HBR3:

AC Common Mode Voltage $\leq$ 30mV

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.8.2*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section D.2, Table D-3*

Expected/Observable Results

The measured AC common mode noise for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source AC Common Mode Test (Informative - HBR3)

Test ID

For Standard DP Pattern:

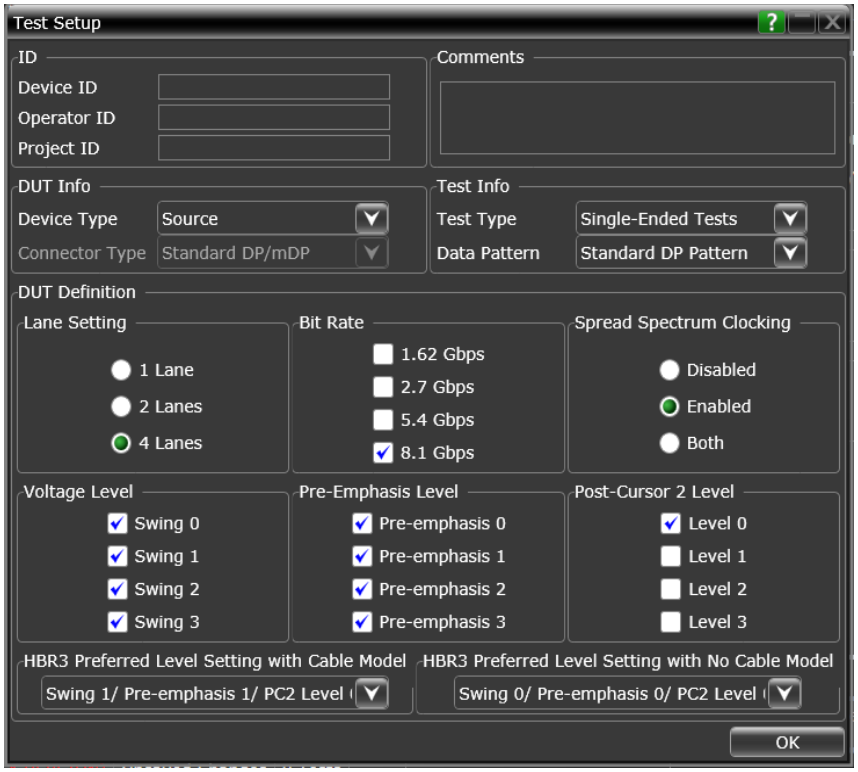
- 12110011, 12110012, 12110013, 12110014 – AC Common Mode Test (Informative)

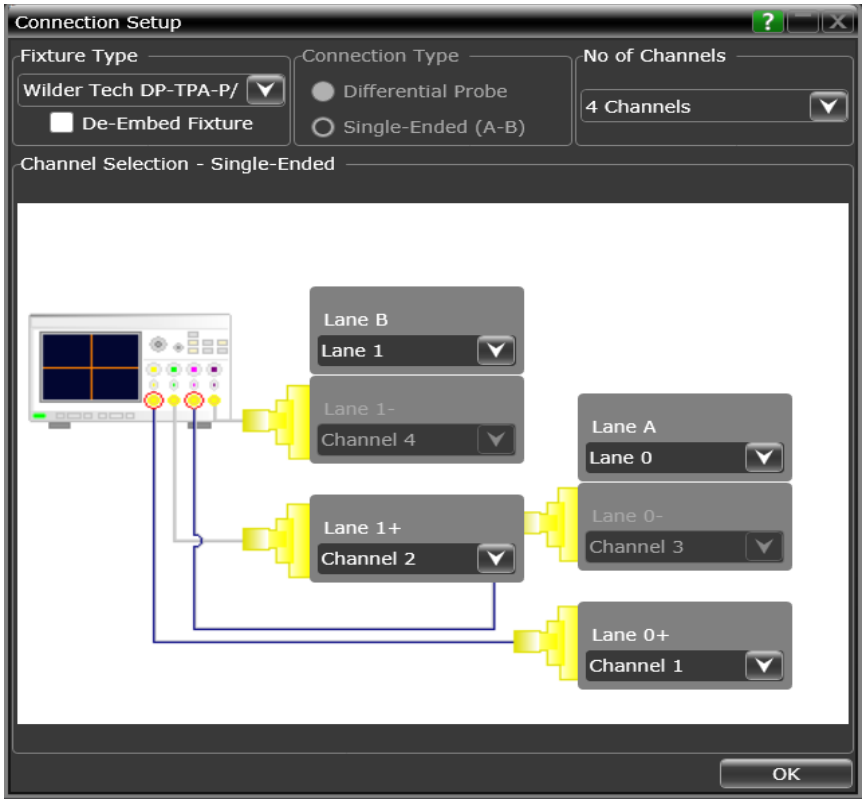
Test Overview

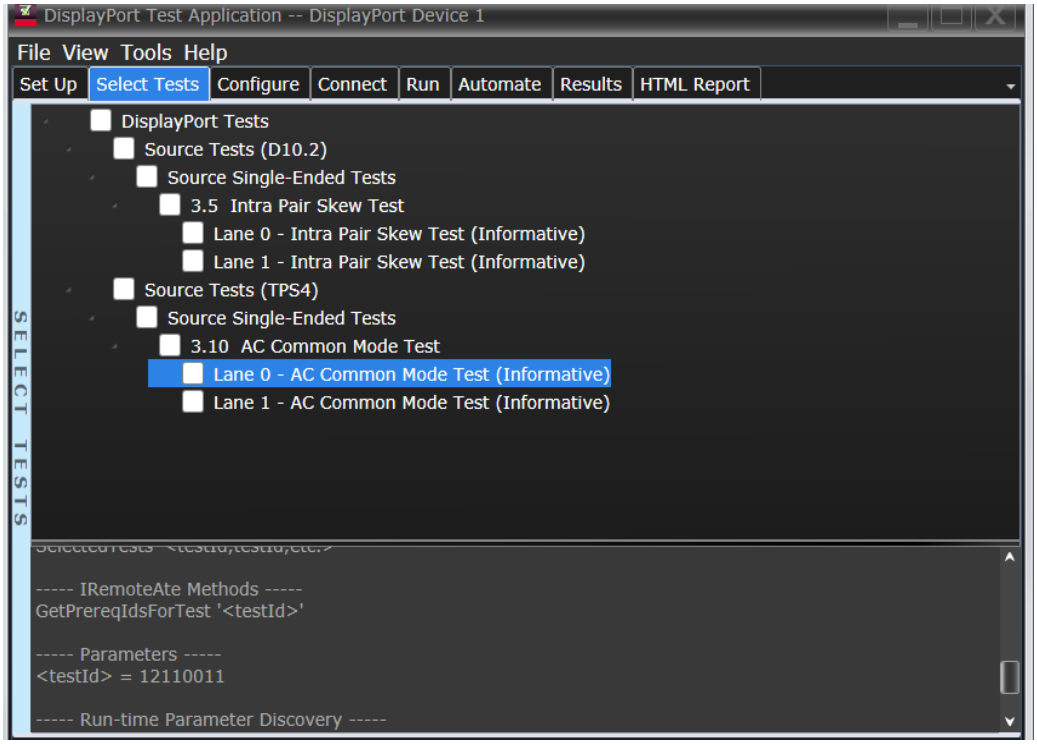
The objective of this test is to evaluate the AC Common Mode noise (unfiltered RMS) of the differential data line of the DP interface.

Test Conditions for AC Common Mode Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	HBR3 - Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	HBR3 - Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes are supported
Test Pattern	TPS4


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Single-Ended Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Create FUNC3 signal, which is the common mode signal of the input single-ended signal.
4 If the filter is enabled [“Filter” configuration variable set to “High Pass Filter”, “Low Pass Filter” or “None” (Default)]:
   a Create FUNC4 signal, which is the filtered FUNC3 signal by applying the High Pass filter or Low Pass filter on the FUNC3 signal based on the Configuration Variable.
5 Set up two display grids such that one grid displays the input single-ended signal while the other grid displays the common mode signal.
6 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
7 Set up the parameters for Peak to Peak voltage measurement of the common mode signal.
   a Set up the $V_{pk\text{-}pk}$ measurement for the common mode signal.
   b Acquire the signal until 100,000 edges are measured.

8 Get the mean for the V_{pk-pk} measurement.

9 Report the measurement results.

PASS Condition

For HBR3:

AC Common Mode Voltage < 100 mV_{pk-pk}

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.8.1*

Expected/Observable Results

The measured AC common mode noise for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Intra-Pair Skew Test (Informative)

Test ID

For Standard DP Pattern:

- 12100001, 12100002, 12100003, 12100004 – Intra-Pair Skew Test (Informative)

For Arbitrary Pattern:

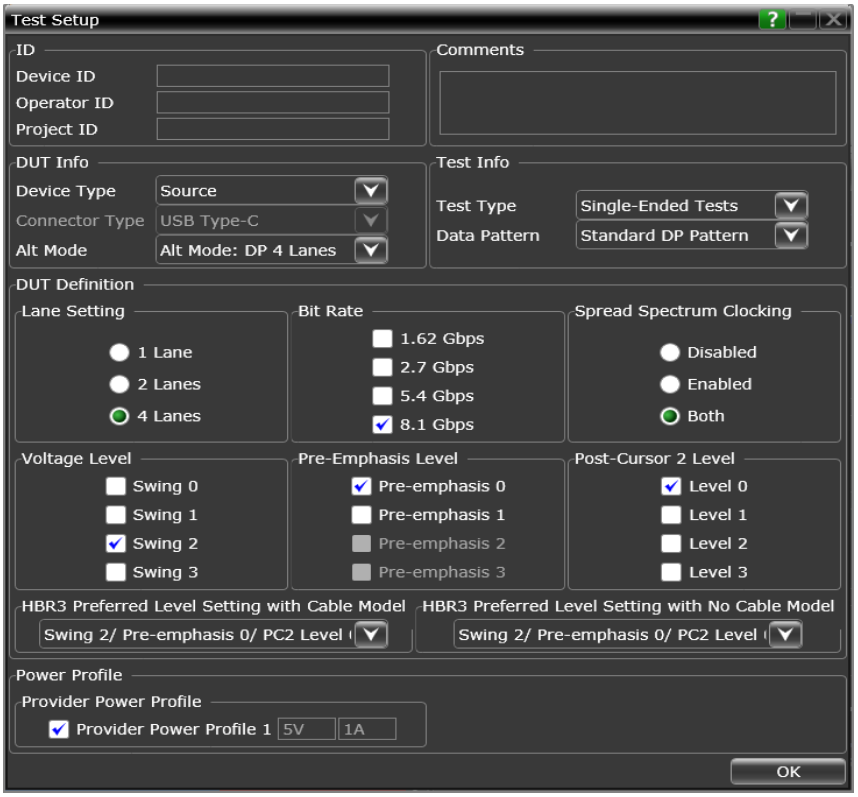
- 13100001, 13100002, 13100003, 13100004 – Intra-Pair Skew Test (Informative)

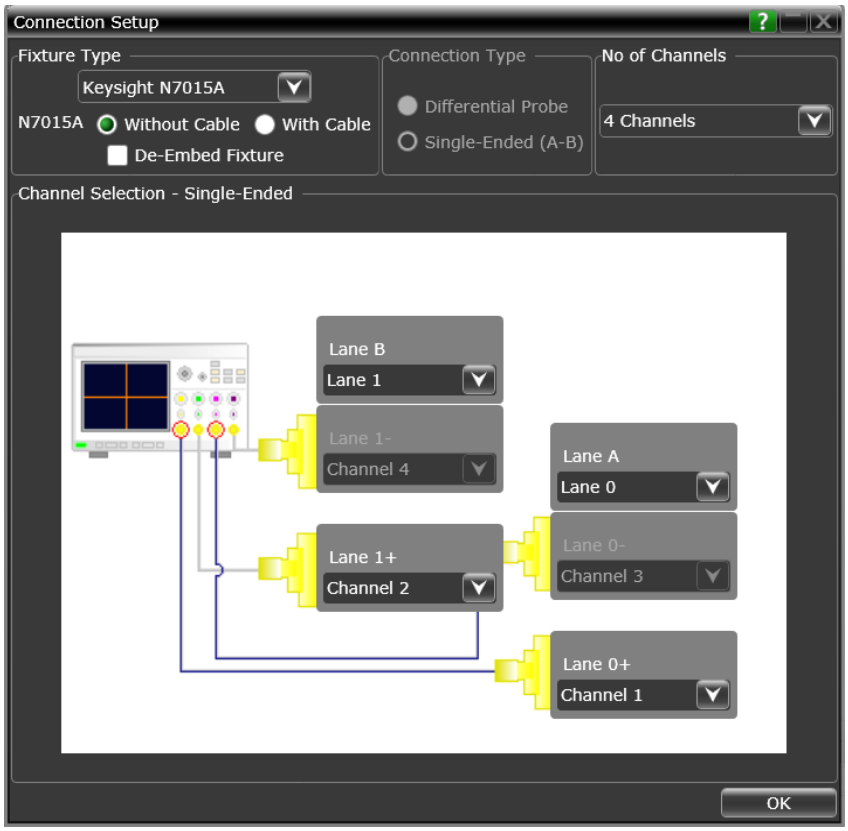
Test Overview

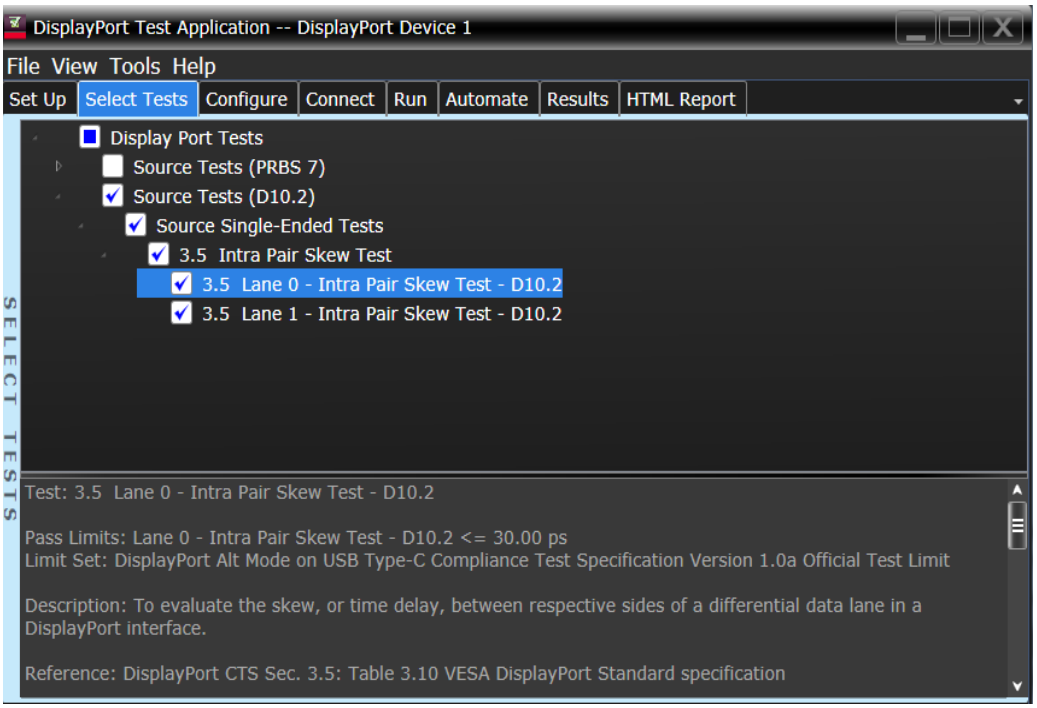
The objective of this test is to evaluate the skew or time delay between respective sides of a differential data lane in the DP interface.

Test Conditions for Intra-Pair Skew Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR3)
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC Enabled only.
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported For one lane operation: Lane 0+ to Lane 0- For two lane operation: Lane 0+ to Lane 0- Lane 1+ to Lane 1- For four lane operation: Lane 0+ to Lane 0- Lane 1+ to Lane 1- Lane 2+ to Lane 2- Lane 3+ to Lane 3-
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Single-Ended Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
4 Set up the parameters to perform High Level Voltage (V_{HIGH}) and Low Level Voltage (V_{LOW}) for each input single-ended signal.
   a Scale the vertical display of the input single-ended signal to optimum value.
   b Acquire the signal for 100 waveforms.
   c Find V_{HIGH} by measuring the average voltage at 0.06 UI to 0.75 UI of the High Level.
   d Find V_{LOW} by measuring the average voltage at 0.06 UI to 0.75 UI of the Low Level.
   e Calculate the Transition Voltage (V_{Trans}) using the equation:

$$V_{Trans} = (V_{HIGH} + V_{LOW}) / 2$$

5 Set up the parameters for the intra-pair skew measurement:

a Set up the measurement threshold for each single-ended data signal based on the measured Transition Voltage.

b Set up InfiniiScan to trigger on the desired pattern.

c Set up delta time measurement to measure time difference between the rising edge of the data true signal (D+) and the complement's (D-) falling edge:

$$D+_{Transition\_High} - D-_{Transition\_Low}$$

d Set up delta time measurement to measure time difference between the falling edge of the data true signal (D+) and the complement's (D-) rising edge:

$$D+_{Transition\_Low} - D-_{Transition\_High}$$

e Acquire the signal until you measure 100 edges.

f Calculate the intra-pair skew using the equation:

$$\text{Intra-Pair Skew} = \{1/\text{Number of Edges}\}$$

$$\sum \{[(D+_{Transition\_High} - D-_{Transition\_Low}) + (D+_{Transition\_Low} - D-_{Transition\_High})] / 2\}$$

6 Report the measurement results.

PASS Condition

Intra-Pair skew ≤ 30 ps

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.7*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.5.2, Table 3-22*

Expected/Observable Results

The measured intra-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

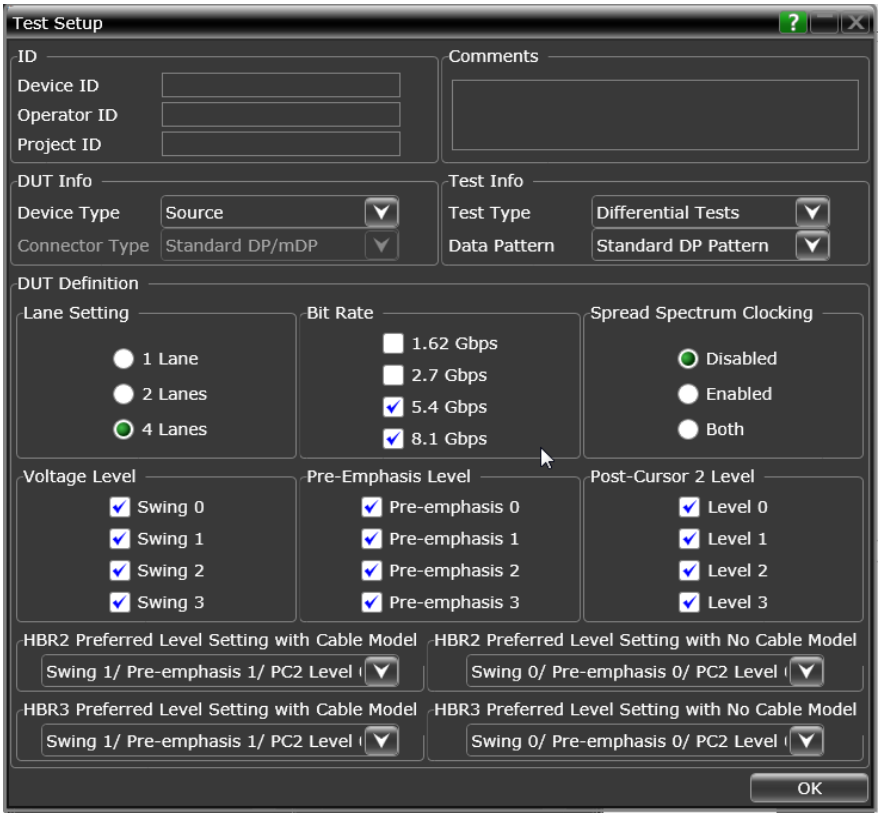
Source Level and Equalization Verification Tests

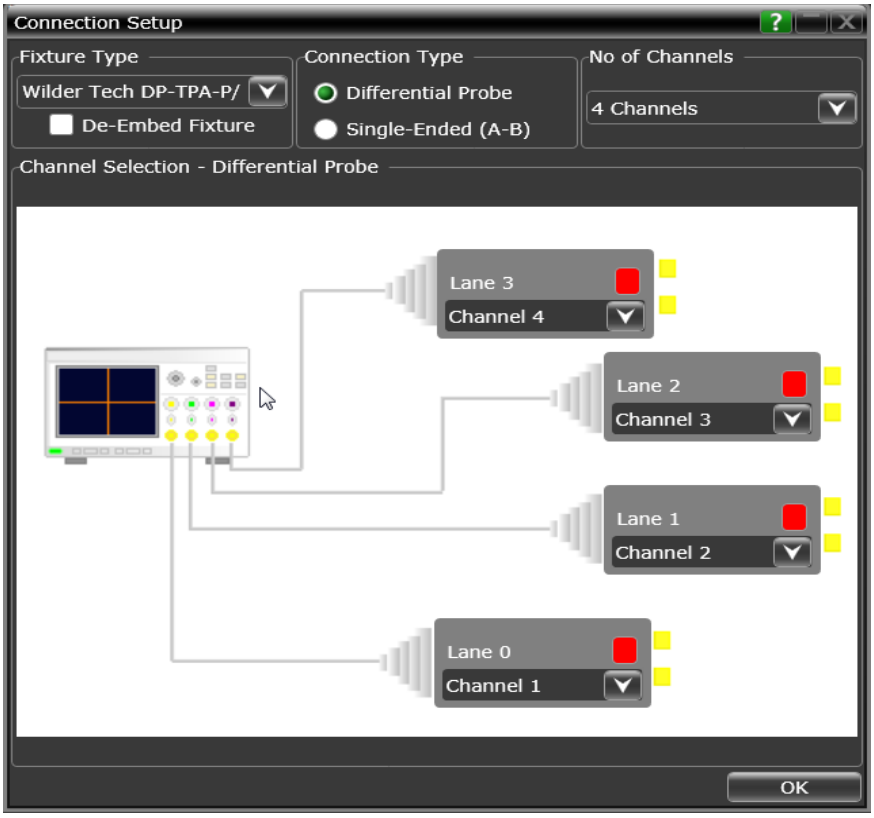
Test Overview

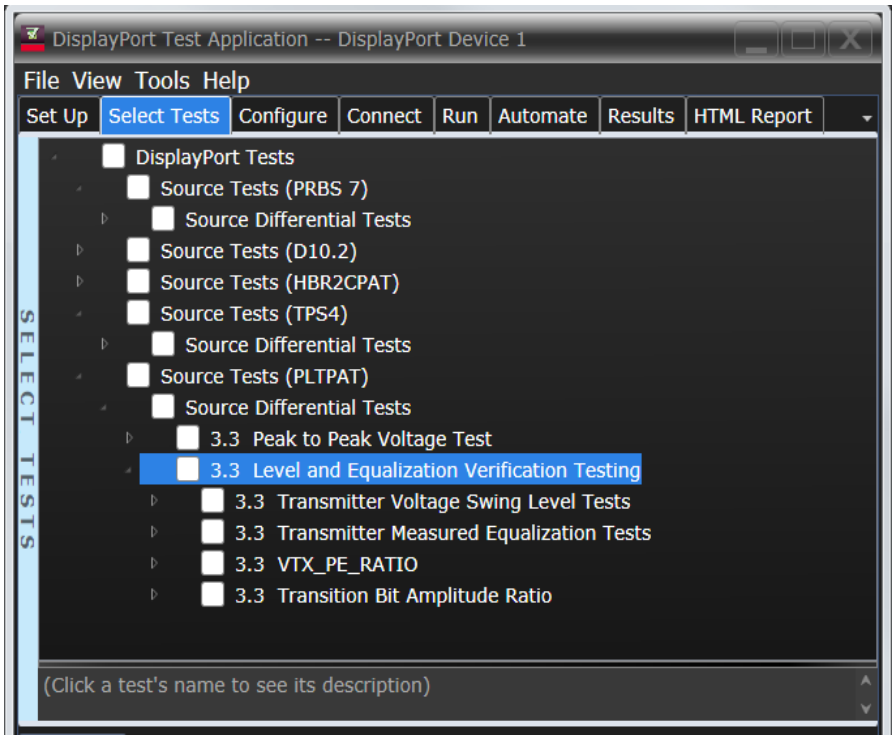
The objective of this test is to ensure that the DUT obeys the system budget also that the Voltage level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by Sink.

Test Conditions for Level and Equalization Verification Tests

Test Parameter	Condition
Test Point	TP2
Bit Rate	HBR2 HBR3
SSC	If DUT supports both SSC ON and OFF conditions, run tests using SSC disabled only.
Voltage Level	VSL[N], Transmitter Voltage Swing Level N, where N = 0,1,2, or 3
Pre-Emphasis Level	TX_EQL[N], Transmitter Equalization Level N, where N = 0,1,2, or 3
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	PLTPAT




Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
DisplayPort Tests
Source Tests (PRBS 7)
Source Differential Tests
Source Tests (D10.2)
Source Tests (HBR2CPAT)
Source Tests (TPS4)
Source Differential Tests
Source Tests (PLTPAT)
Source Differential Tests
3.3 Peak to Peak Voltage Test
3.3 Level and Equalization Verification Testing
3.3 Transmitter Voltage Swing Level Tests
3.3 Transmitter Measured Equalization Tests
3.3 VTX_PE_RATIO
3.3 Transition Bit Amplitude Ratio
(Click a test's name to see its description)

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities>Calibration** menu.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure VTOP and VBASE of the input signal.
   d Measure the data rate of the input signal.
3 Setup the parameter of spectral measurements:
   a Set Sampling Rate at > 40GSa/s.
   b Configure the FFT feature with the following parameters:
      i RBW* - 10 KHz
      ii Detector Type = Average
      iii Start frequency - 500 MHz
      iv Stop frequency - 4.5 GHz
      v Select the **Mark Peaks** check-box
      vi Set Hanning window

* To reduce the test time, the test will run the FFT using 10 kHz RBW by default. If the DUT has a low-frequency SJ that causes inconsistent pass/fail result, user may reduce the RBW to 1kHz.

4 Set the Source device's output to VSL[0] and TX_AEQ[0], where VSL is the Transmitter Voltage Swing Level and TX_AEQ is Transmitter's Applied Equalization Level.

5 Measure the peak FFT at the fundamental (first) and fifth harmonic levels (in dB) and denote them as f1 and f5.
6 Repeat step 5 to measure f1 and f5 for each value of VSL[0] and valid TX_AEQ[0] to TX_AEQ[3] values. The peak frequencies to obtain the FFT peak f1 and f5 locations are:

Bit Rate	Peak Frequencies	
	f1 (MHz)	f5 (GHz)
HBR3	810	4.05
HBR2	540	2.70

7 Calculate Δf [N] value for each setting of VSL[0] and valid TX_AEQ[0] to TX_AEQ[3] values using the equation: Δf [N] = f1-f5

8 Repeat steps 4 to 7 for all VSL[N] and TX_AEQ[N], where N = 1, 2, or 3.

NOTE

Not all combinations of VSL[N] and TX_AEQ[N] are valid to measure the harmonic levels. Refer to Table 166 for the valid combinations of swing level and pre-emphasis levels to derive valid values of Δf [N].

Table 166 FFT 1st and 5th harmonic amplitude (dB) for valid VSL[N] and TX_AEQ[N]

VSL[0]		f1	f5	f1-f5 (Δf [0])
TX_AEQ	P0	Available	Available	Δf [0] at VSL[0] and P0
	P1	Available	Available	Δf [0] at VSL[0] and P1
	P2	Available	Available	Δf [0] at VSL[0] and P2
	P3	Available	Available	Δf [0] at VSL[0] and P3
VSL[1]		f1	f5	f1-f5 (Δf [1])
TX_AEQ	P0	Available	Available	Δf [1] at VSL[1] and P0
	P1	Available	Available	Δf [1] at VSL[1] and P1
	P2	Available	Available	Δf [1] at VSL[1] and P2
	P3	Not Available	Not Available	Not Available
VSL[2]		f1	f5	f1-f5 (Δf [2])
TX_AEQ	P0	Available	Available	Δf [2] at VSL[2] and P0
	P1	Available	Available	Δf [2] at VSL[2] and P1
	P2	Not Available	Not Available	Not Available
	P3	Not Available	Not Available	Not Available
VSL[3]		f1	f5	f1-f5 (Δf [3])
TX_AEQ	P0	Available	Available	Δf [3] at VSL[3] and P0
	P1	Not Available	Not Available	Not Available
	P2	Not Available	Not Available	Not Available
	P3	Not Available	Not Available	Not Available

Transmitter Voltage Swing Level Tests

VTX_OUTPUT_LEVEL0_RATIO (VSL 1/VSL 0)

VTX_OUTPUT_LEVEL0_RATIO (VSL 2/VSL 0)

VTX_OUTPUT_LEVEL0_RATIO (VSL 3/VSL 0)

VTX_OUTPUT_RATIO (VSL 1/VSL 0)

VTX_OUTPUT_RATIO (VSL 2/VSL 1)

VTX_OUTPUT_RATIO (VSL 3/VSL 2)

Test ID

For Standard DP Pattern

1281101, 1281102, 1281103, 1281104 – VTX_OUTPUT_LEVEL0_RATIO (VSL 1/VSL 0) - PLTPAT

1282101, 1282102, 1282103, 1282104 – VTX_OUTPUT_LEVEL0_RATIO (VSL 2/VSL 0) - PLTPAT

1283101, 1283102, 1283103, 1283104 – VTX_OUTPUT_LEVEL0_RATIO (VSL 3/VSL 0) - PLTPAT

1285101, 1285102, 1285103, 1285104 – VTX_OUTPUT_RATIO (VSL 1/VSL 0) - PLTPAT

1286101, 1286102, 1286103, 1286104 – VTX_OUTPUT_RATIO (VSL 2/VSL 1) - PLTPAT

1287101, 1287102, 1287103, 1287104 – VTX_OUTPUT_RATIO (VSL 3/VSL 2) - PLTPAT

Procedure:

1 Perform the procedure for Spectral Measurements as a prerequisite.
2 Ensure that Pre-Emphasis is set to Level 0; that is, measurements are performed with TX_EQL[0].
3 For each value of f1 measured for each VSL[N], as calculated in Table 1, calculate $f1_{VSL[N]}$ - $f1_{VSL[0]}$.
4 Calculate $V_{TX\_OUTPUT\_LEVEL0\_RATIO}$ using the equation:
$V_{TX\_OUTPUT\_LEVEL0\_RATIO}$ = VSL[N] / VSL[0] = $f1_{VSL[N]}$ - $f1_{VSL[0]}$, where N = 1,2 or 3
5 Record each value for $V_{TX\_OUTPUT\_LEVEL0\_RATIO}$ in the following table:

VSL[N] value	Minimum	VSL[N] / VSL[0]	Maximum
1	1.6		4.5
2	3.2		7.0
3	4.8		10.5

6 For each value of f1 measured for each VSL[N], as calculated in Table 1, calculate $f1_{VSL[N]}$ - $f1_{VSL[N-1]}$.
7 Calculate $V_{TX\_OUTPUT\_RATIO}$ using the equation:
$V_{TX\_OUTPUT\_RATIO}$ = VSL[N] / VSL[N-1] = $f1_{VSL[N]}$ - $f1_{VSL[N-1]}$, where N = 1, 2, or 3

8 Record each value for $V_{TX\_OUTPUT\_RATIO}$ in the following table:

VSL[N] value	Minimum	VSL[N] / VSL[N-1]
1	1.6	
2	1.1	
3	1.1	

Pass Condition for Transmitter Voltage Swing Level Tests

Symbol	Parameter	Min.	Max.	Units	Comments
$V_{TX\_OUTPUT\_LEVEL0\_RATIO}$	Ratio of Voltage Swing VSL[1] / VSL[0]	1.6	4.5	dB	▪ Calculated using measured value of 1st harmonic of FFT at TX_EQL[0] ▪ VSL[3] mandatory
	Ratio of Voltage Swing VSL[2] / VSL[0]	3.2	7.0	dB	
	Ratio of Voltage Swing VSL[3] / VSL[0]	4.8	10.5	dB	
$V_{TX\_OUTPUT\_RATIO}$	Ratio of Voltage Swing VSL[1] / VSL[0]	1.6	-	dB	▪ Calculated using measured value of 1st harmonic of FFT at TX_EQL[0] ▪ VSL[3] mandatory
	Ratio of Voltage Swing VSL[2] / VSL[1]	1.1	-	dB	
	Ratio of Voltage Swing VSL[3] / VSL[2]	1.1	-	dB	

Transmitter Measured Equalization Tests

VTX_MEQ_LEVEL0_DELTA

VTX_MEQ_DELTA

Test ID:

For Standard DP Pattern

1291101, 1291102, 1291103, 1291104 – VTX_MEQ_LEVEL0_DELTA - PLTPAT

1295101, 1295102, 1295103, 1295104 – VTX_MEQ_DELTA - PLTPAT

Procedure:

1 Perform the procedure for Spectral Measurements as a prerequisite.

2 Ensure that Pre-Emphasis is set to Level 0; that is, measurements are performed with TX_EQL[0] as reference.

NOTE This test verifies that the TX_EQL[N] values increase monotonically within the specified ranges.

3 For each valid value of VSL[N] and TX_EQL[N] value, calculate $V_{TX\_MEQ\_LEVEL0\_DELTA[N]}$ using the equation:
$V_{TX\_MEQ\_LEVEL0\_DELTA}[N] = \Delta f_{[0]} - \Delta f_{[N]}$ (refer to Table 166 for values of $\Delta f_{[N]}$)

4 Calculate $V_{TX\_MEQ\_LEVEL0\_DELTA}$ using the equation:
$V_{TX\_MEQ\_LEVEL0\_DELTA[N]} = TX\_EQL[N] / TX\_EQL[0] = \Delta f_{[0]} - \Delta f_{[N]}$, where N = 1, 2, or 3

5 Record each value for $V_{TX\_MEQ\_LEVEL0\_DELTA}$ in the following table:

VSL[0]	Minimum	TX_EQL[N] / TX_EQL[0]	Maximum
P1	1.3		4.0
P2	2.4		6.0
P3	3.5		8.0
VSL[1]	Minimum	TX_EQL[N] / TX_EQL[0]	Maximum
P1	1.3		4.0
P2	2.4		6.0
VSL[2]	Minimum	TX_EQL[N] / TX_EQL[0]	Maximum
P1	1.3		4.0

6 Calculate $V_{TX\_MEQ\_DELTA}$ using the equation:
$V_{TX\_MEQ\_DELTA} = TX\_EQL[N] / TX\_EQL[N-1] = \Delta f_{[N-1]} - \Delta f_{[N]}$, where N = 1, 2, or 3

7 Record each value for $V_{TX\_OUTPUT\_RATIO}$ in the following table:

VSL[0]	Minimum	TX_EQL[N] / TX_EQL[N-1]
P1	1.3	
P2	0.7	
P3	0.7	
VSL[1]	Minimum	TX_EQL[N] / TX_EQL[N-1]
P1	1.3	
P2	0.7	
VSL[2]	Minimum	TX_EQL[N] / TX_EQL[N-1]
P1	1.3	

Pass Condition for Transmitter Measured Equalization Tests:

Symbol	Parameter	Min.	Max.	Units	Comments
$V_{TX\_MEQ\_LEVEL0\_DELTA}$	Delta of TX Emphasis TX_EQL[1] / TX_EQL[0]	1.3	4.0	dB	▪ Applies to all valid VSLs ▪ Calculated using measured value of 1st and 5th harmonics of FFT ▪ For a given VSL[N]: TX_EQL[N] / TX_EQL[0] = (5th - 1st)[N] - (5th - 1st)[0] ▪ TX_EQL[3] mandatory
	Delta of TX Emphasis TX_EQL[2] / TX_EQL[0]	2.4	6.0	dB	
	Delta of TX Emphasis TX_EQL[3] / TX_EQL[0]	3.5	8.0	dB	
$V_{TX\_MEQ\_DELTA}$	Delta of TX Pre-Emphasis TX_EQL[1] / TX_EQL[0]	1.3	-	dB	▪ Applies to all valid VSLs ▪ Calculated using measured value of 1st and 5th harmonics of FFT ▪ For a given VSL[N]: TX_EQL[N] / TX_EQL[N - 1] = (5th - 1st)[N] - (5th - 1st)[N - 1] ▪ TX_EQL[3] mandatory
	Delta of TX Pre-Emphasis TX_EQL[2] / TX_EQL[1]	0.7	-	dB	
	Delta of TX Pre-Emphasis TX_EQL[3] / TX_EQL[2]	0.7	-	dB	

VTX_PE_RATIO

Test ID:

For Standard DP Pattern

1298101, 1298102, 1298103, 1298104 – VTX_PE_RATIO- PLTPAT

Procedure:

1 Perform the procedure for Spectral Measurements and Transmitter Measured Equalization Tests as prerequisites.

2 For each valid value of VSL[N] and TX_EQL[N], calculate PE[N] using the equation:
PE[N] = f5[N] - f5[0] (refer to Table 1 for values of f5)

3 Record each value for PE[N] in the following table:

VSL[0]	PE[0]
P0	Reference
P1	
P2	
P3	
VSL[1]	PE[1]
P0	Reference
P1	
P2	
VSL[2]	PE[2]
P0	Reference
P1	

4 For each value of $V_{TX\_MEQ\_LEVEL0\_DELTA}$ calculated in the Transmitter Measured Equalization Tests, determine the closest adjacent TX_MEQ values in dB.

5 Using Linear Interpolation, calculate the normative minimum PE (minPE) that corresponds to each measured value of TX_MEQ.
minPE = [(TX_MEQ - X1) (Y2 - Y1) / (X2 - X1)] + Y1
where, (X1,Y1) and (X2,Y2) are adjacent TX_MEQ and Normative minPE values.

6 Verify that the actual calculated values of PE[N] are above those illustrated in the following Figure.

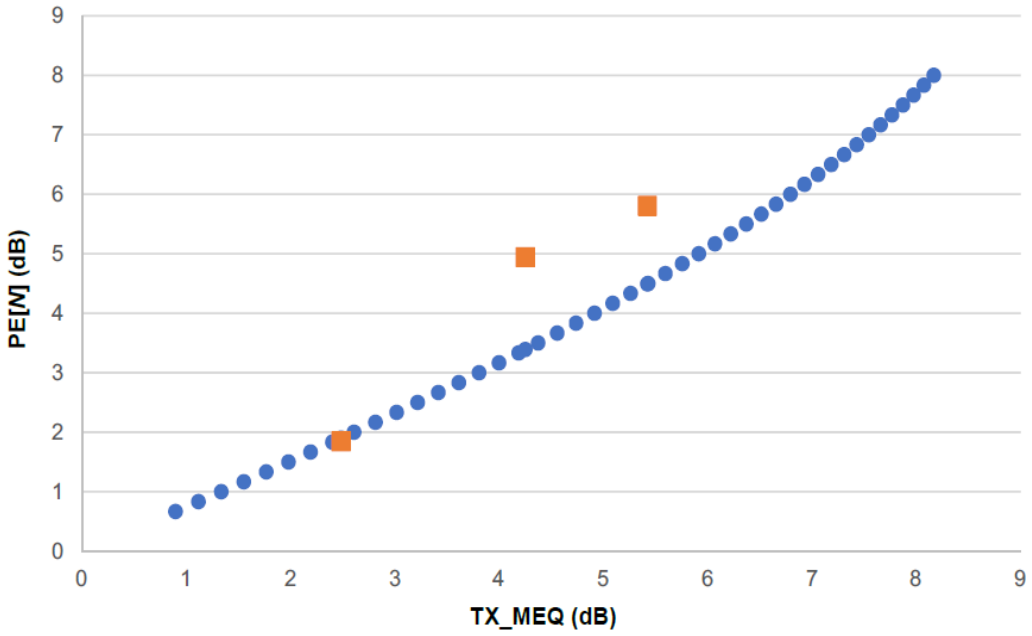


Figure 145 PE v/s TX_MEQ curve

Pass Condition for VTX_PE_RATIO Tests:

Symbol	Parameter	Min.	Max.	Units	Comments
$V_{TX\_PE\_RATIO}$	Ratio of PE[N] / TX_MEQL[N]	2/3	-		▪ Applies to all valid VSL and TX_EQL combinations ▪ PE[N] = 5th[N] - 5th[0] ▪ Pass/fail based on PE vs. MEQ curve

PE[N] > minPE calculated

Transmitter Bit Amplitude Ratio

VTX_TRANSITION_BIT_OUTPUT_RATIO

Test ID:

For Standard DP Pattern

1299101, 1299102, 1299103, 1299104 – VTX_TRANSITION_BIT_OUTPUT_RATIO - PLTPAT

Procedure:

1 Perform the procedure for Spectral Measurements as a prerequisite.

NOTE

The TX_EQL[N] transition bit amplitude shall be greater than or equal to TX_EQL[N-1] transition bit amplitude.

2 For a given value of VSL, calculate $V_{TX\_TRANSITION\_BIT\_OUTPUT\_RATIO}$ using the equation: $V_{TX\_TRANSITION\_BIT\_OUTPUT\_RATIO}$ = f5[N] - f5[N-1], where N = 1, 2, or 3 (refer to Table 166 for f5)

3 Record each value for $V_{TX\_TRANSITION\_BIT\_OUTPUT\_RATIO}$ in the following table:

VSL[0]	Minimum	Notes
P0	Not Available	Reference
P1	0	
P2	0	
P3	0	
VSL[1]	-	-
P0	Not Available	Reference
P1	0	
P2	0	
VSL[2]	-	-
P0	Not Available	Reference
P1	0	

Pass Condition for Transmitter Bit Amplitude Ratio Tests:

Symbol	Parameter	Min.	Max.	Units	Comments
$V_{TX\_TRANSITION\_BIT\_OUTPUT\_RATIO\_PEL[N]/PEL[N-1]}$	Transition bit amplitude ratio between TX_EQL[N] and TX_EQL[N - 1] for a given VSL[N]	0	-	dB	▪ TX_EQL[N] transition bit amplitude shall be greater than or equal to that of TX_EQL[N - 1] ▪ 5th (N) - 5th (N - 1)

Test References

See:

VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 3.4, Table 3-15.

VESA DisplayPort (DP) Standard, Version 1.4a, Section 3.5.2, Table 3-21.

Expected/Observable Results

The measured values for Level and Equalization testing shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for each test

20 DPoC 1.4a Sink Tests

Overview

The specifications and the conceptual information for the DPoC 1.4a standard are aligned with that for the DisplayPort 1.4 standard. For more information, refer to "Overview" on page 348.

Setting Up the DisplayPort Compliance Test Application for DPoC 1.4a Sink Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort Standards with Type-C capability, select the option **DPoC 1.4a** in the **Test Specification** area.
5. The option **Physical Layer Tests** appears by default in the **Test Selection** area.
6. Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.
7. In the **Type-C Environment Setup** area, select **Enable Type-C Controller** to activate the **DUT Orientation** field and the **Setup Type-C Controller** button. To know about how to configure the Type-C Controller, refer to the *Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help*.
8. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
9. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
10. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
11. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
12. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
13. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
14. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
15. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DPoC 1.4a Sink Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

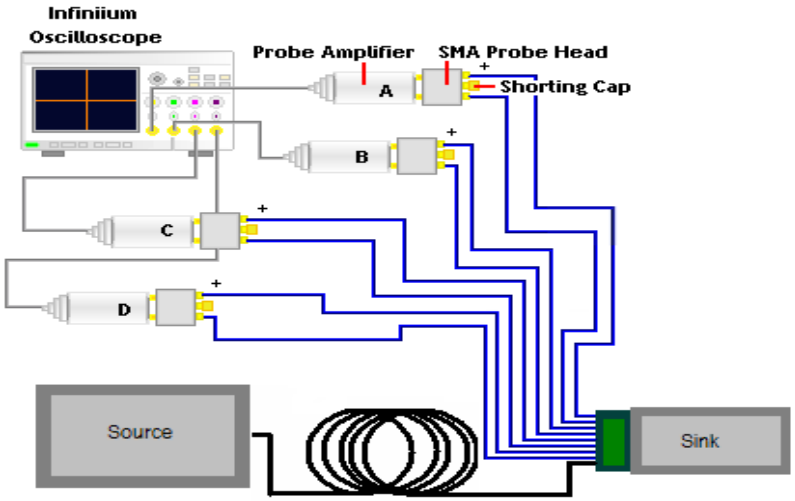


Figure 146 Sample connection diagram for DPoC 1.4a Sink Tests with Differential Probes

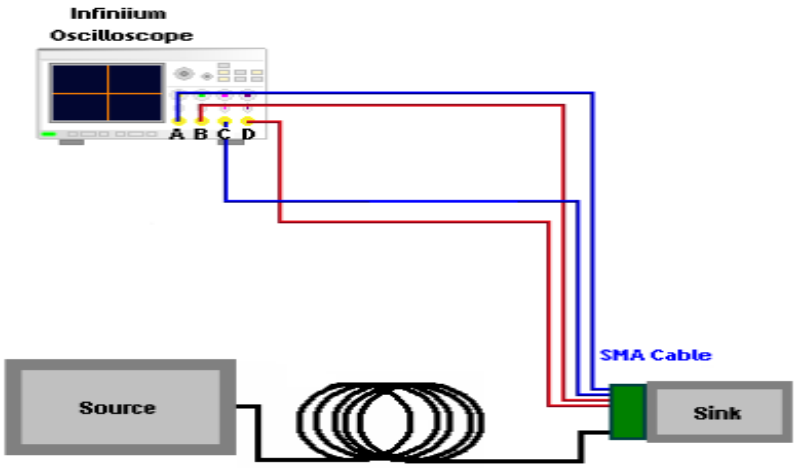


Figure 147 Sample connection diagram for DPoC 1.4a Sink Tests with Single-Ended Probes

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Sink tests to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1. In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.
2. On the **Test Setup** window,
   a. Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.
   b. In the **DUT Info** area, select **Device Type** as **Sink**. The **Connector Type** is grayed out. From the drop-down options for **Alt Mode**, select either **Alt Mode: DP 4 Lanes** or **Alt Mode: DP 2 + 2**.
   c. In the **Test Info** area, the **Test Type** is grayed out.
   d. In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.
3. Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1. Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.
2. On the **Connection Setup** window,
   a. The **Fixture Type** area is grayed out.
   b. Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.
   c. In the **Channel Selection** area, assign appropriate channels to lanes.
3. Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of sink tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for DPoC 1.4a Sink Tests" on page 808 to complete the task flow for DUT setup along with configuring the Compliance Application to run each test.

Sink Eye Diagram Test

Test ID

12140001, 12140002, 12140003, 12140004 – Eye Diagram Test

Test Overview

The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

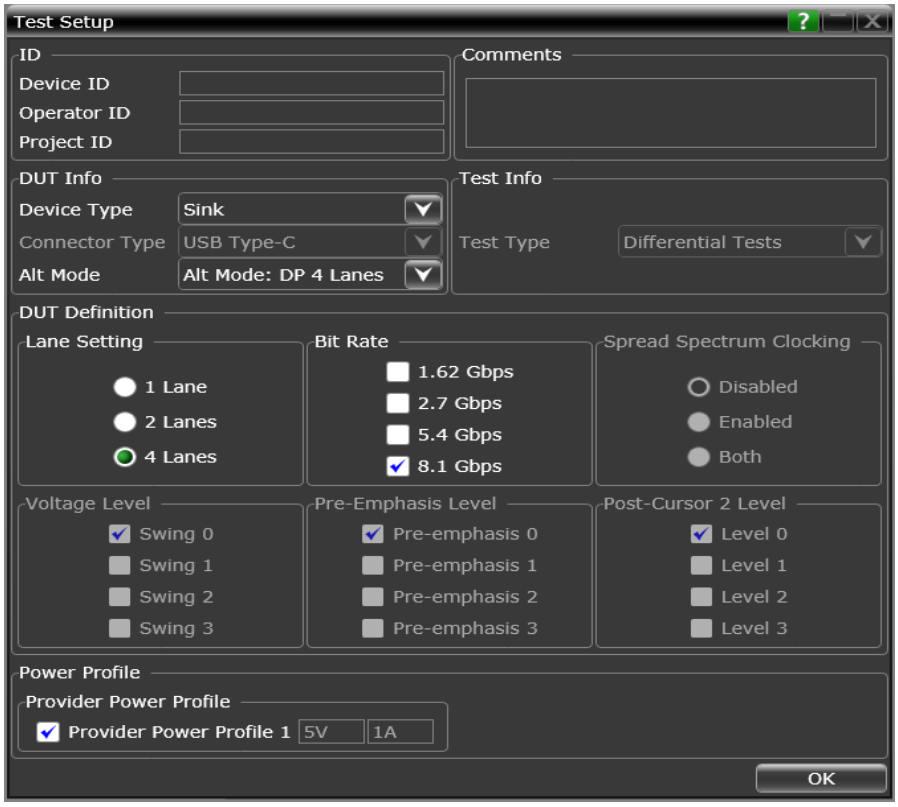
You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the following specifications for degradation:

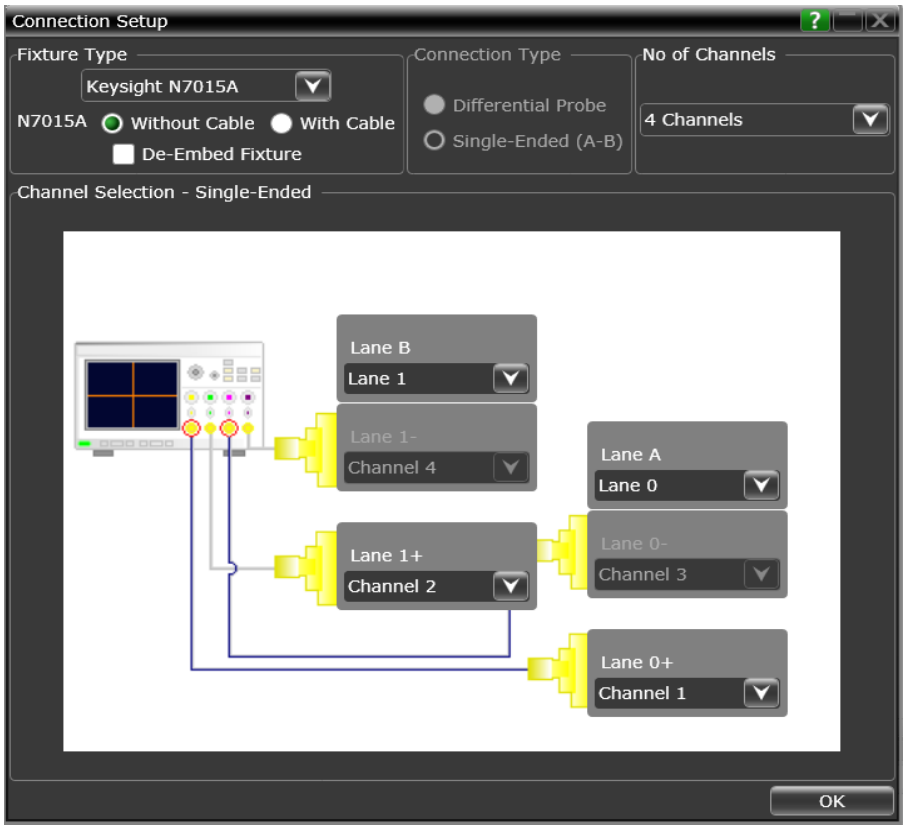
- Voltage Level:
  - 90mV peak to peak +/- 10% for HBR2 at TP3_EQ (Table 3-18, DP1.2a)
  - 150mV peak to peak +/- 10% for HBR at TP3_EQ (Table 3-25, DP1.2a)
  - 46mV peak to peak +/- 10% for RBR at TP3 (Table 3-26, DP1.2a

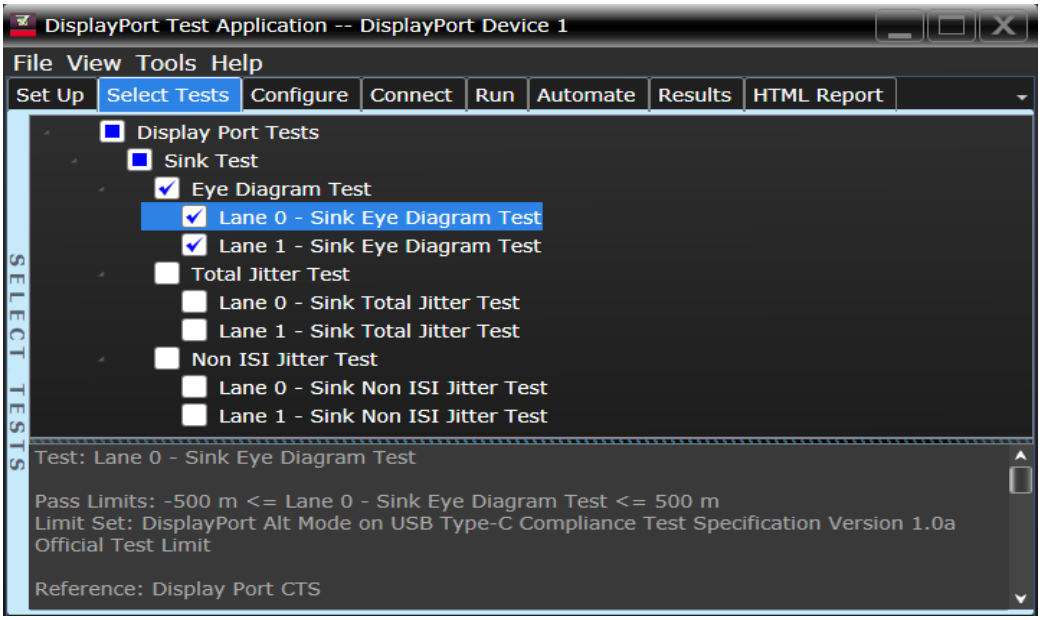
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR3–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR3)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR3–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
9 Measure the jitter of the eye diagram using the Histogram.

10 Check for any signal trajectories that may have entered into the mask.

11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 167 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 167 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

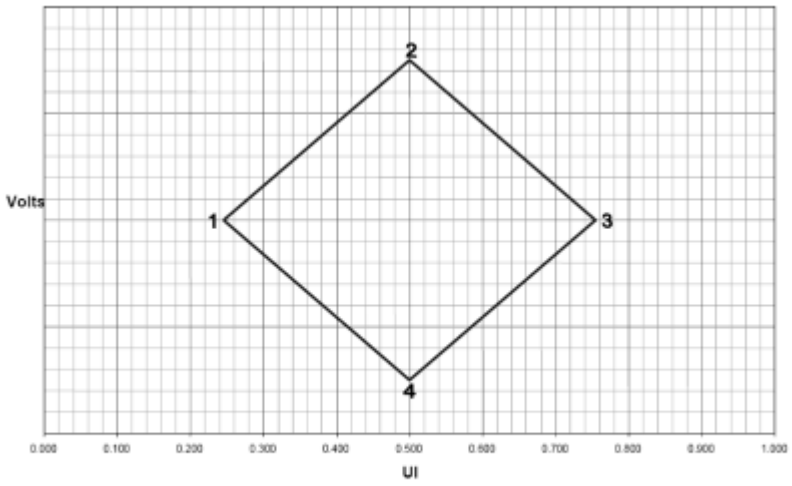


Figure 148 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 168 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.0045*
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.0045*

NOTE

*Eye height limit of 45 mV and -45 mV assumes cross-talk as 0, which is only possible in case of single lane testing.

In case of multi-lane testing, cross talk exists, and the eye height values deviate by ± 7 mV. Thus the eye height becomes (+45 +7) mV and (-45 -7) mV or +52 mV and -52 mV.

Table 169 Eye Diagram Mask Coordinates for TP3_EQ (HBR3)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.35UI	0.00000
2	Any passing UI location between 0.375 and 0.625UI	0.00375
3	Point 1 + 0.35UI	0.00000
4	Same as Point 2	-0.00375

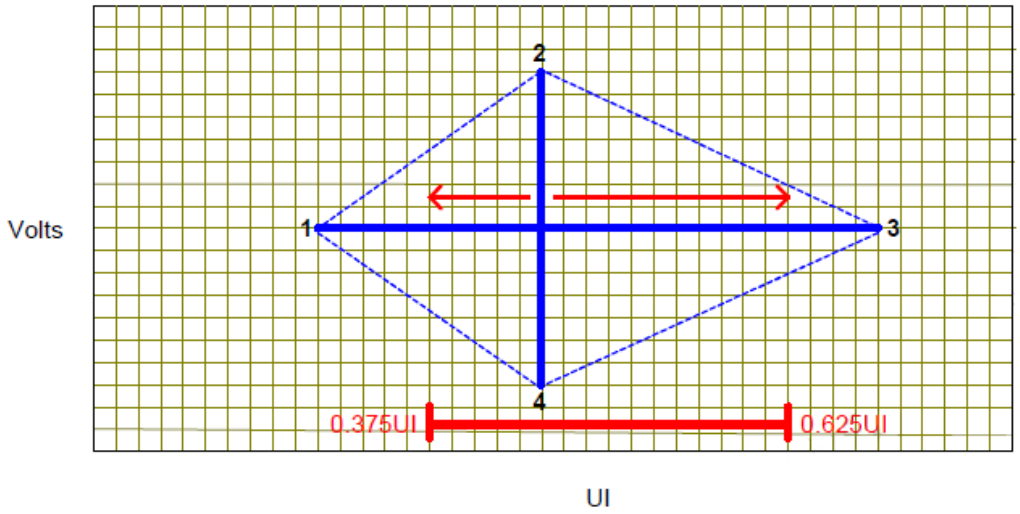


Figure 149 The Eye Mask at TP3_EQ (HBR2 and HBR3)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Sink Total Jitter Test

Test ID

12210001, 12210002, 12210003, 12210004 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

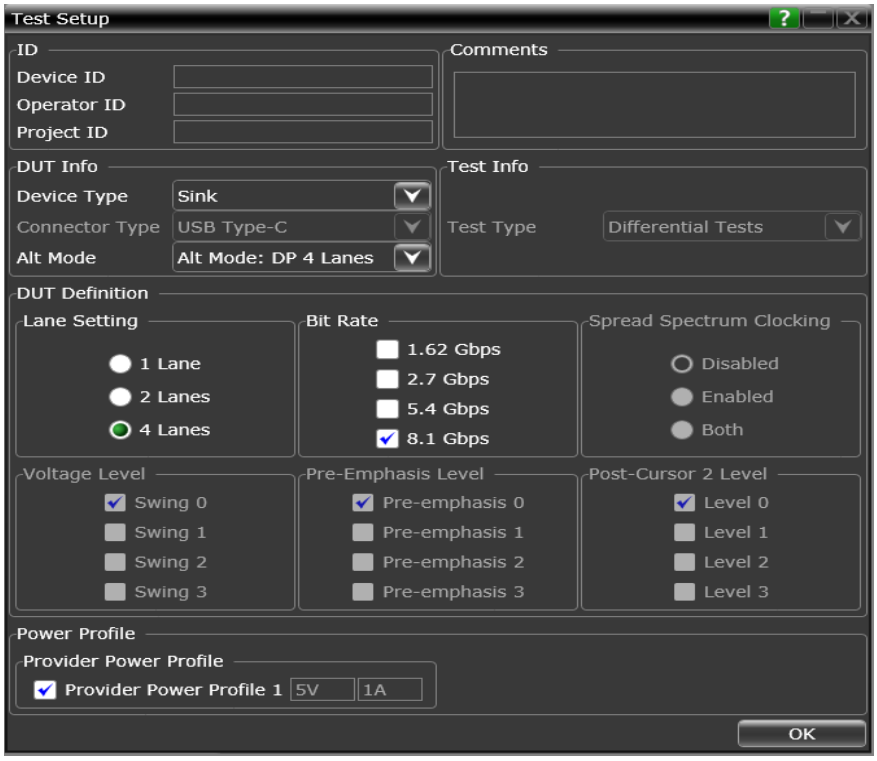
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

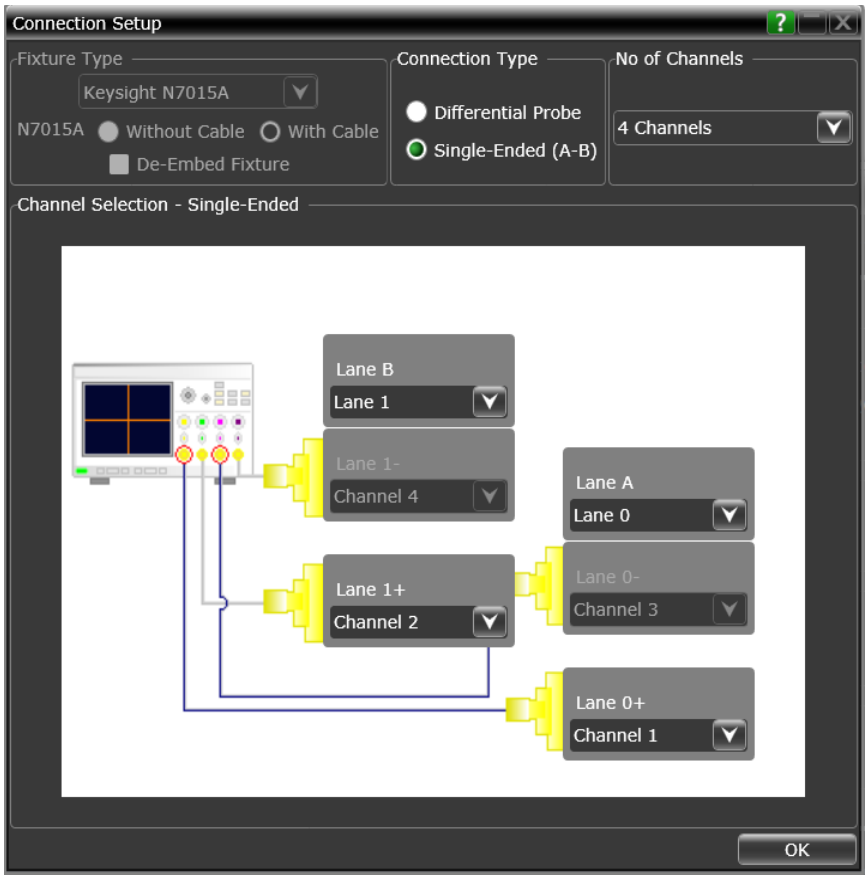
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

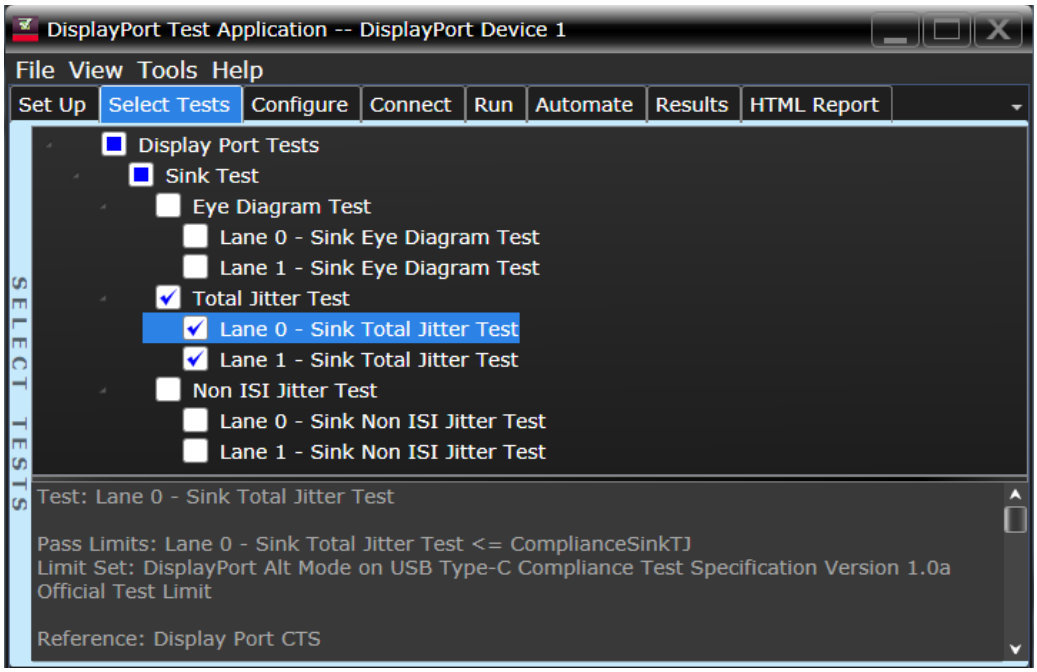
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR3–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR3)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR3–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 170 Total Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	0.580 UI*

* The limits for the Total Jitter are derated by 0.04 UI from 0.62 UI limit in DisplayPort 1.2a Standard.

Table 171 Total Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 4.1*
- VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Sink Non-ISI Jitter Test

Test ID

12220001, 12220002, 12220003, 12220004 – Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

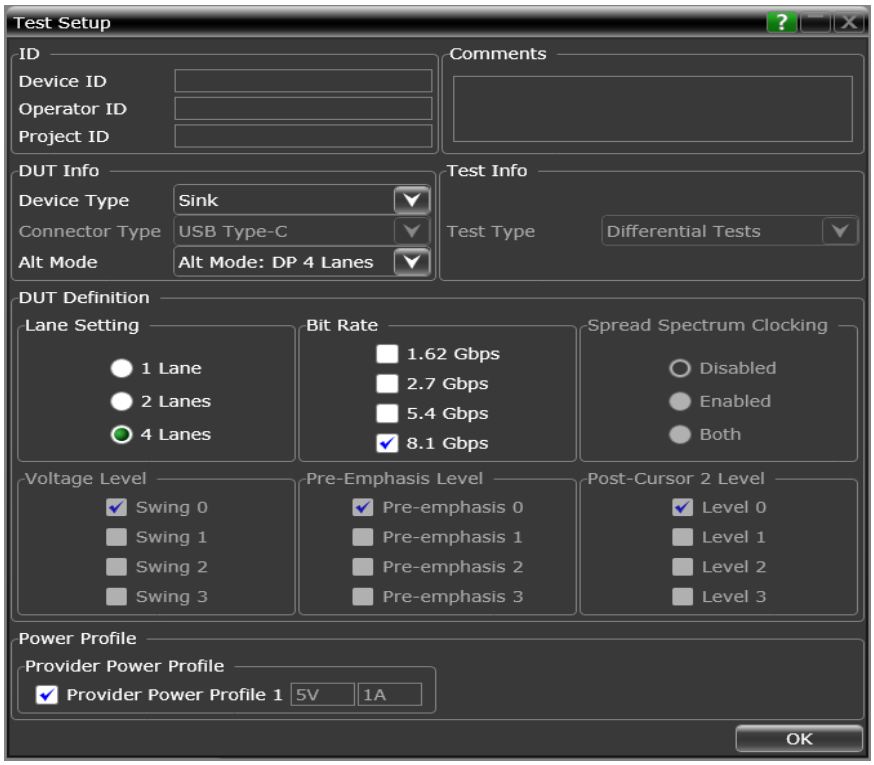
Calculate Non-ISI Jitter using the following equation:

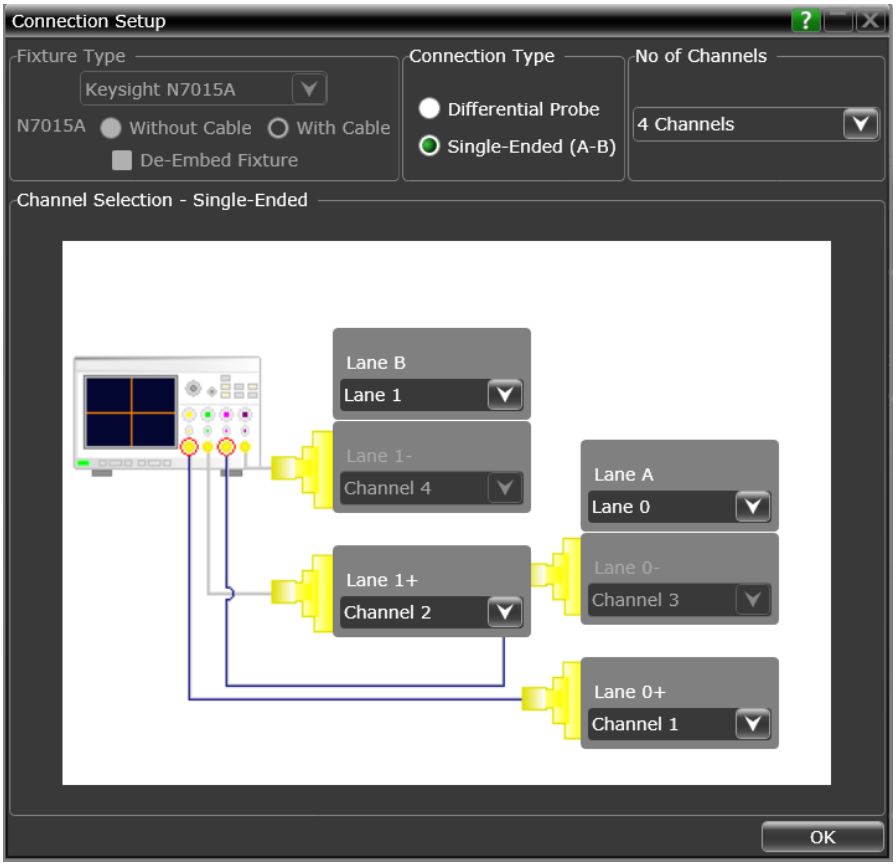
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

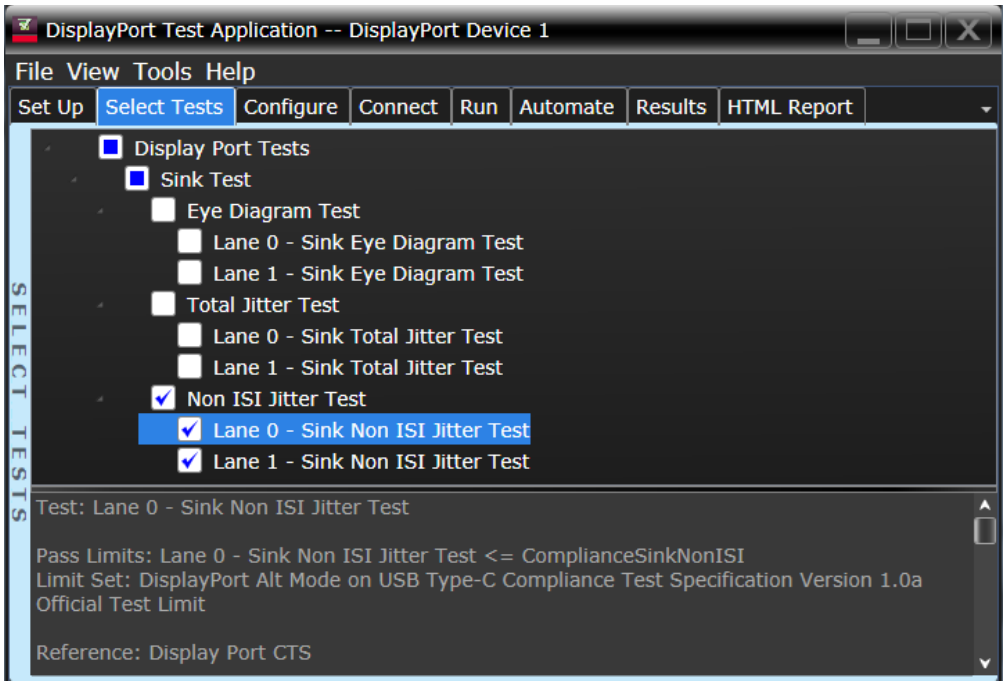
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR3–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR3)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR3–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 172 Non ISI Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	-

Table 173 Non ISI Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 4.1*
- VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

21 DPoC 1.4a Cable Tests

Overview

The specifications and the conceptual information for the DPoC standard are aligned with that for the DisplayPort 1.4 standard. For more information, refer to "Overview" on page 368.

Setting Up the DisplayPort Compliance Test Application for DPoC 1.4a Cable Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort Standards with Type-C capability, select the option **DPoC 1.4a** in the **Test Specification** area.
5. The option **Physical Layer Tests** appears by default in the **Test Selection** area.
6. Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.
7. In the **Type-C Environment Setup** area, select **Enable Type-C Controller** to activate the **DUT Orientation** field and the **Setup Type-C Controller** button. To know about how to configure the Type-C Controller, refer to the *Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help*.
8. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
9. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
10. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
11. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
12. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
13. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
14. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
15. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DPoC 1.4a Cable Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

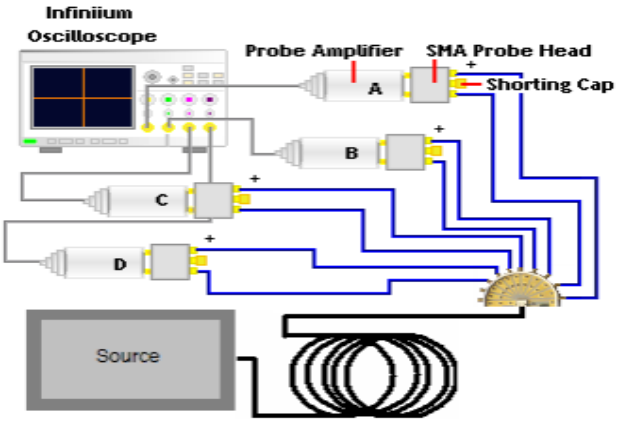


Figure 150 Sample connection diagram for DPoC 1.4a Cable Tests with Differential Probes

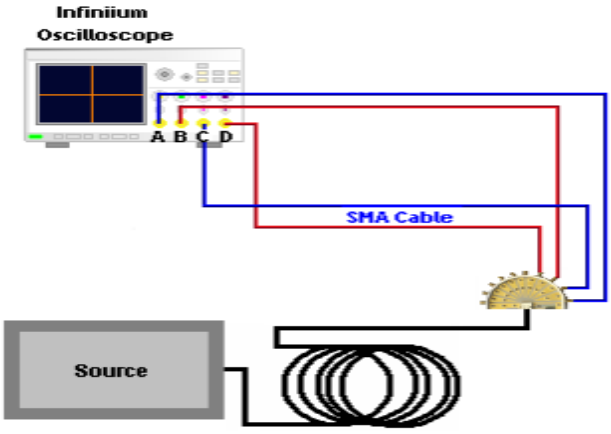


Figure 151 Sample connection diagram for DPoC 1.4a Cable Tests with Single-Ended Probes

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Cable tests to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1. In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.
2. On the **Test Setup** window,
   a. Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.
   b. In the **DUT Info** area, select **Device Type** as **Cable**. The **Connector Type** is grayed out. From the drop-down options for **Alt Mode**, select either **Alt Mode: DP 4 Lanes** or **Alt Mode: DP 2 + 2**.
   c. In the **Test Info** area, the **Test Type** is grayed out.
   d. In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.
3. Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1. Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.
2. On the **Connection Setup** window,
   a. The **Fixture Type** area is grayed out.
   b. Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.
   c. In the **Channel Selection** area, assign appropriate channels to lanes.
3. Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of cable tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for DPoC 1.4a Cable Tests" on page 826 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Cable Eye Diagram Test

Test ID

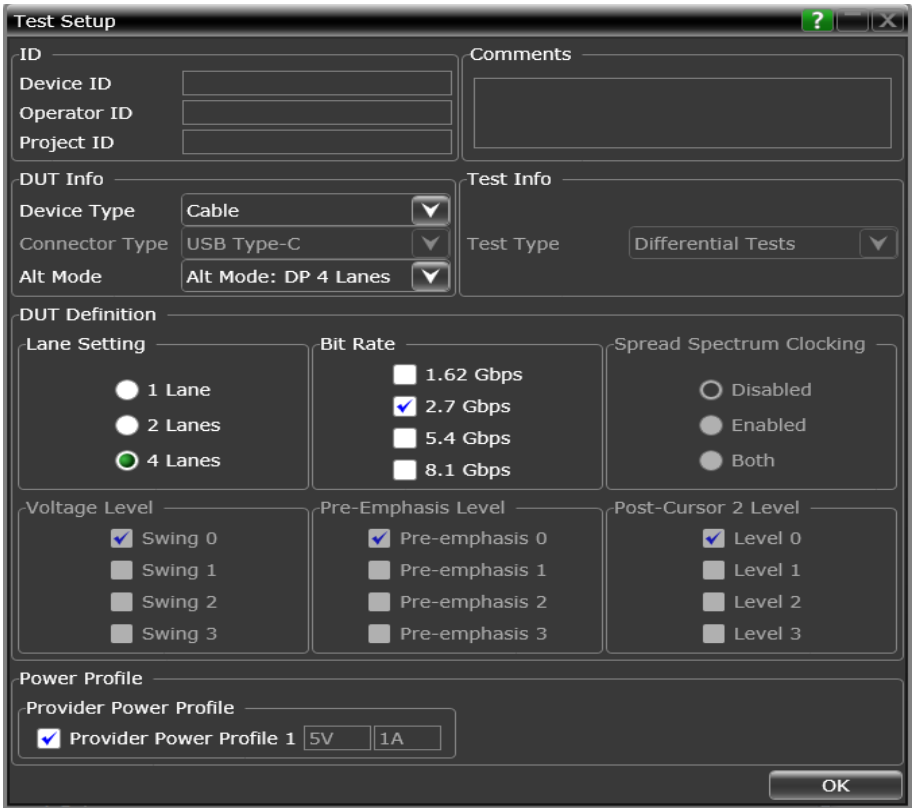
12150001, 12150002, 12150003, 12150004 – Eye Diagram Test

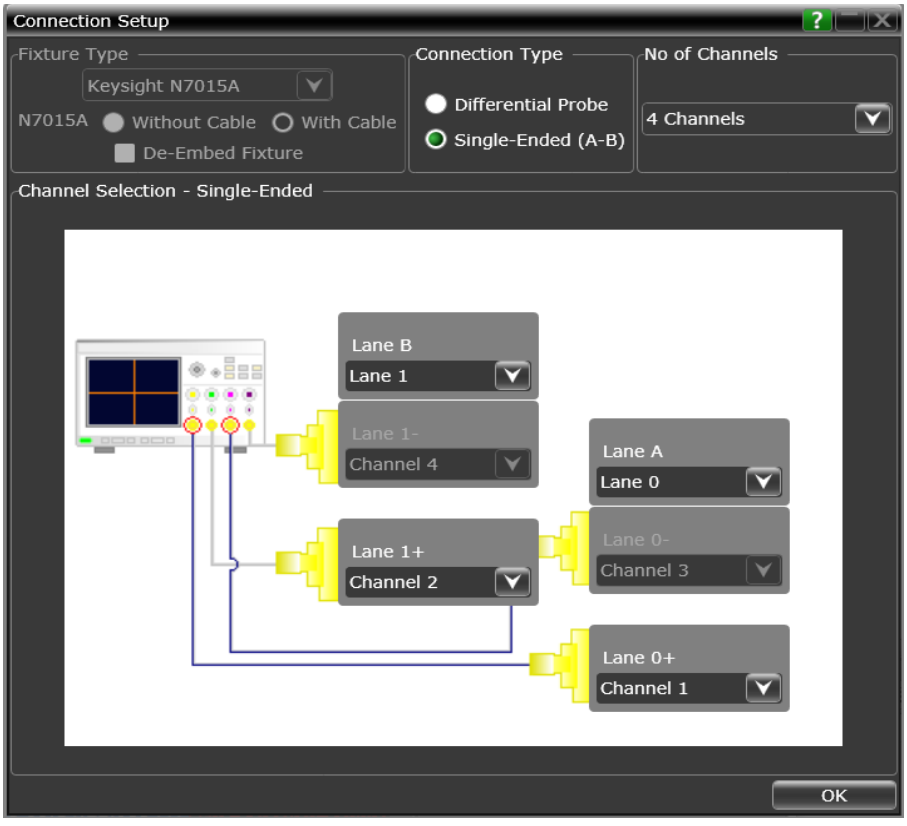
Test Overview

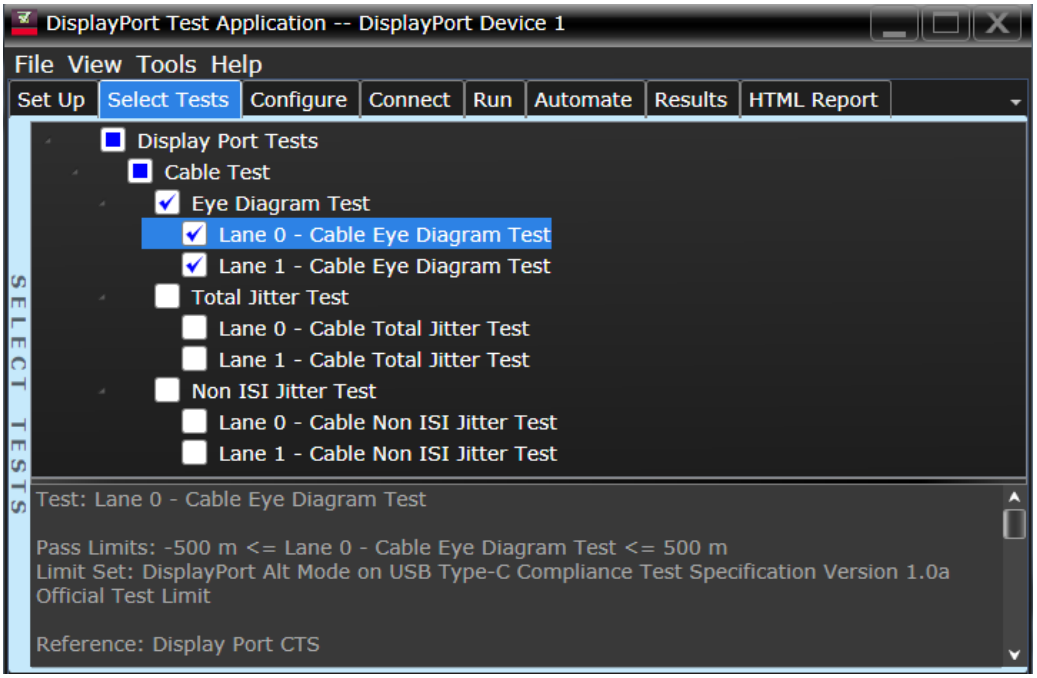
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 82
Crosstalk Signal Parameter	Quarter-rate clock signal (D24.3 pattern) is injected to lanes other than the lane under test. The characteristics of the aggressor signals are: Pattern–D24.3 Bit Rate–(Same as lane under test) Voltage Amplitude–(Same as lane under test) ▪ RBR-400mV ▪ HBR-350mV Edge Rate (20-80)–130ps at TP3


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.

9 Measure the jitter of the eye diagram using the Histogram.
10 Check for any signal trajectories that may have entered into the mask.
11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 174 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 174 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	High (2.7 Gb/s)
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

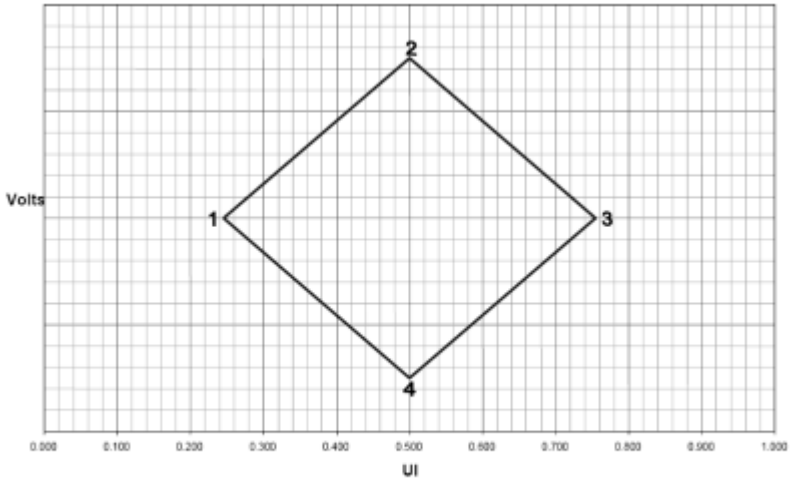


Figure 152 The Cable Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Cable Total Jitter Test

Test ID

12230001, 12230002, 12230003, 12230004 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

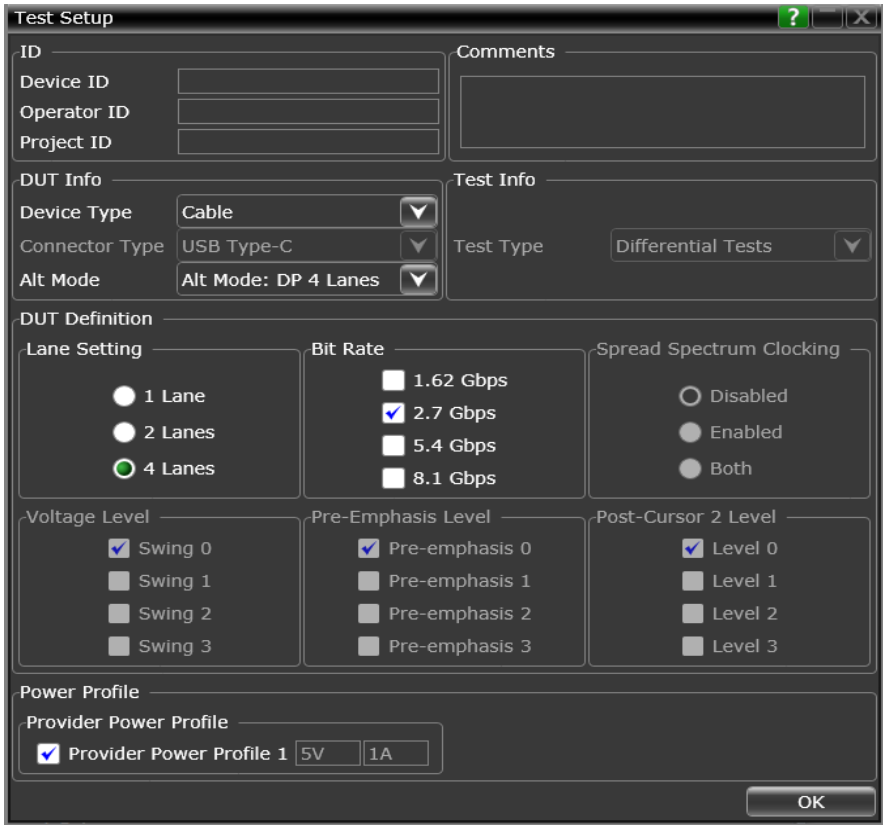
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

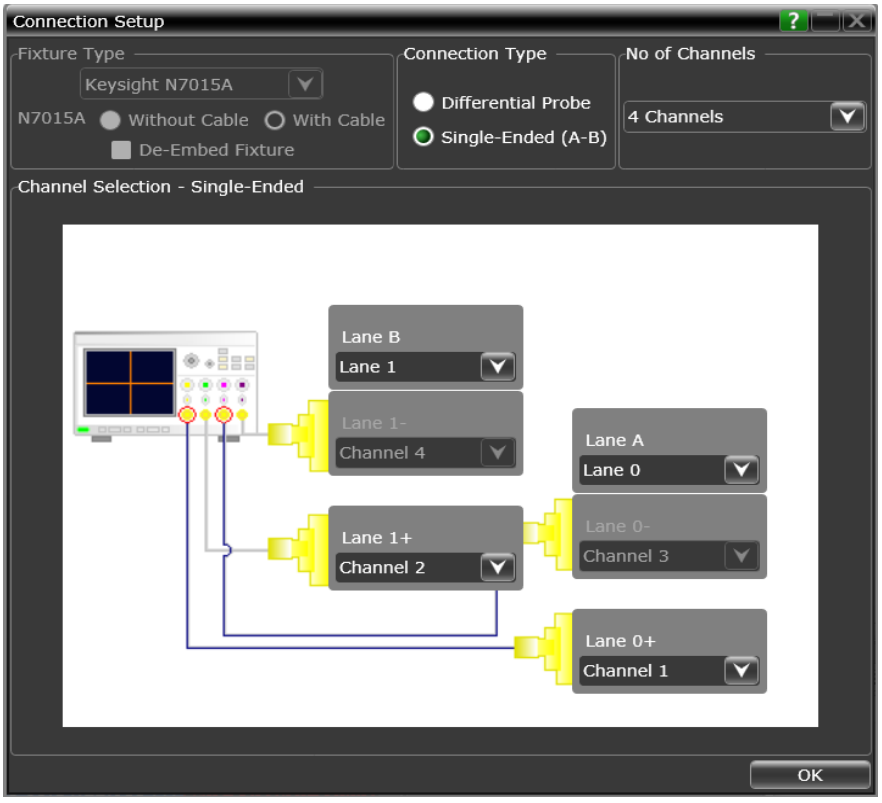
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

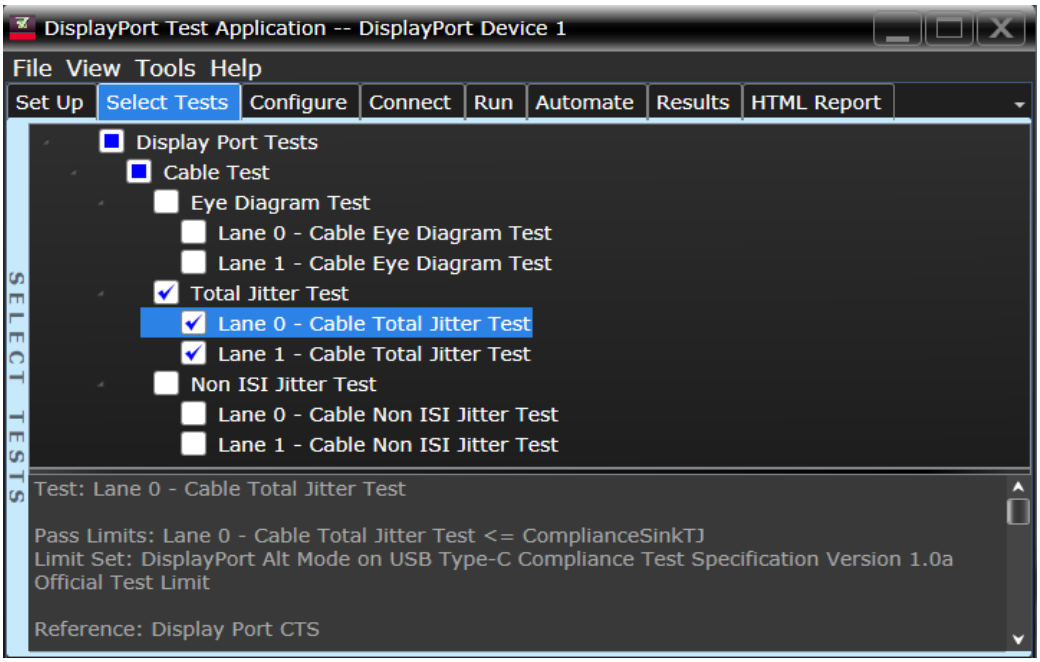
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 82


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 175 Total Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Cable Non-ISI Jitter Test

Test ID

12240001, 12240002, 12240003, 12240004 — Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

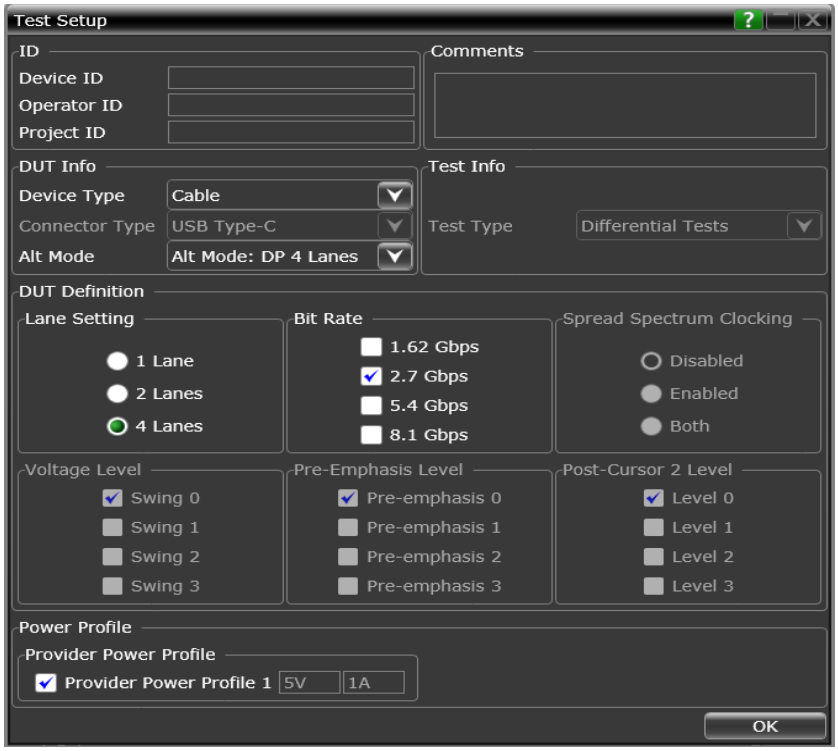
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

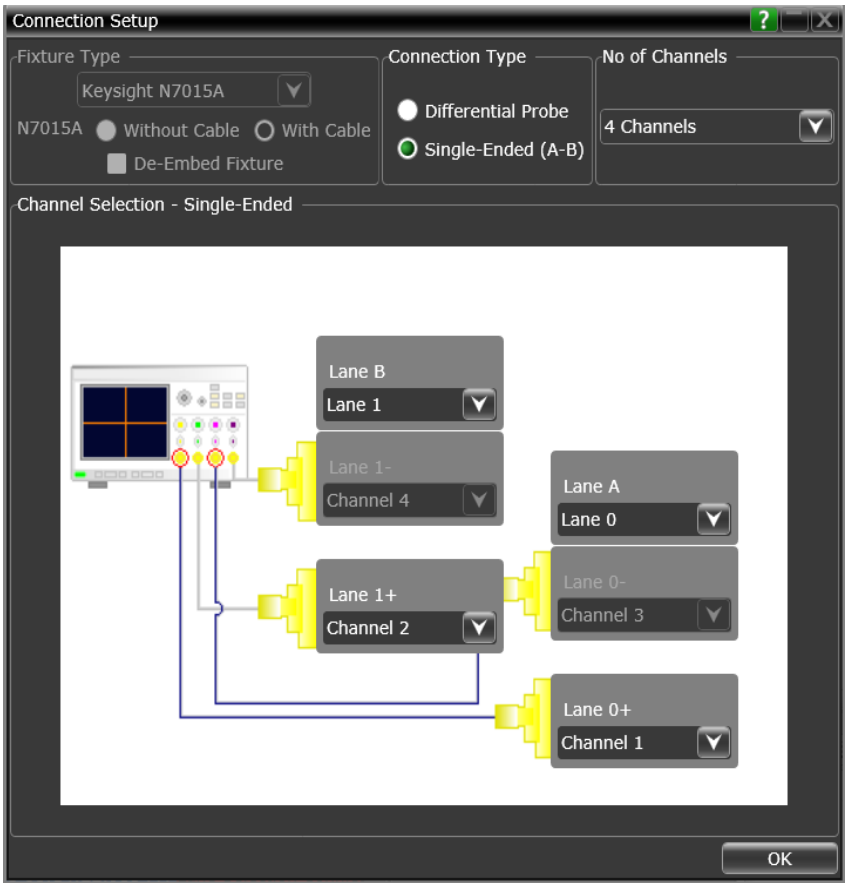
Calculate Non-ISI Jitter using the following equation:

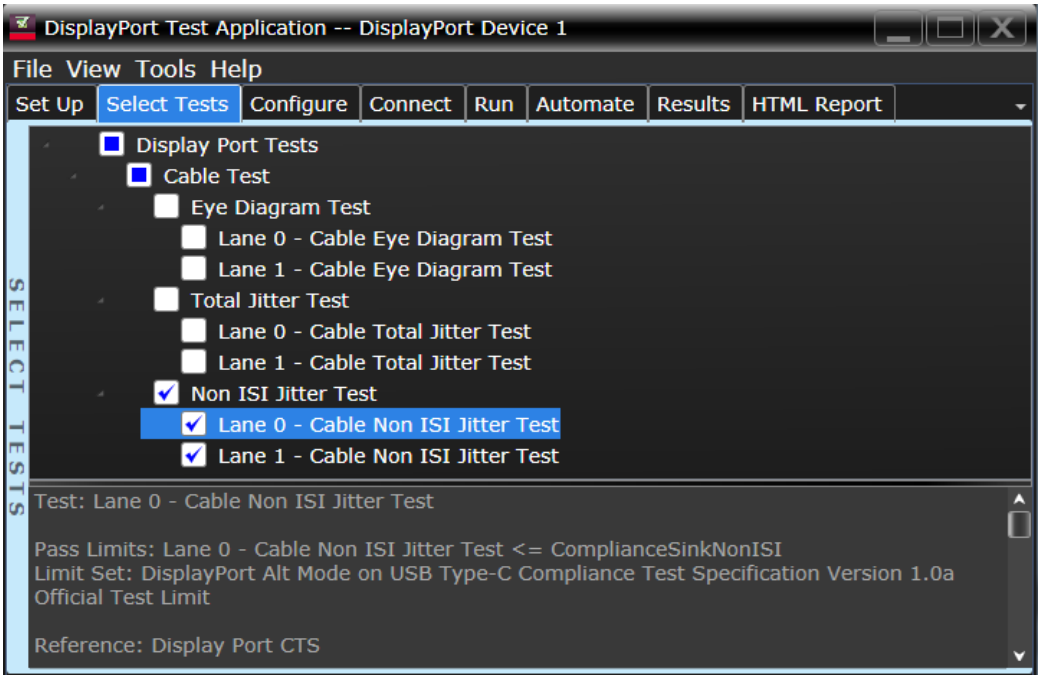
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 82


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 176 Non ISI Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non-ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

22 DPoC 1.4a AUX Channel Tests

Overview

The specifications and the conceptual information for the DPoC 1.4a standard are aligned with that for the DisplayPort 1.4 standard. For more information, refer to "Overview" on page 388.

Setting Up the DisplayPort Compliance Test Application for DPoC 1.4a AUX Channel Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort Standards with Type-C capability, select the option **DPoC 1.4a** in the **Test Specification** area.
5. Select the option **AUX PHY and Inrush Tests** in the **Test Selection** area.
6. In the **Type-C Environment Setup** area, select **Enable Type-C Controller** to activate the **DUT Orientation** field and the **Setup Type-C Controller** button. To know about how to configure the Type-C Controller, refer to the *Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help*.
7. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
8. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
9. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
10. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
11. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
12. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
13. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
14. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Settings for AUX PHY and Inrush Tests

Perform the following steps before you run the Auxiliary Channel and Inrush tests on the source or sink device:

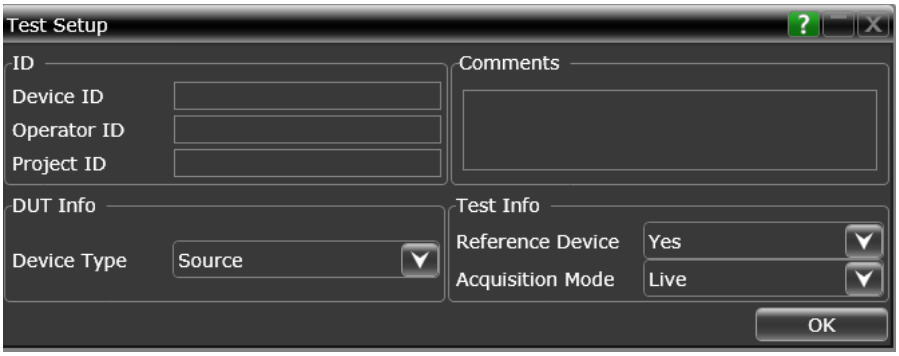
1 Click the **Test Setup** button on the **Set Up** tab to set up for Auxiliary Channel and Inrush tests.

2 From the **Device Type** drop-down options, select either **Source** or **Sink**.

3 From the **Reference Device** drop-down options, select **Yes** if a reference sink/source is attached to device under test during testing.

4 From the **Acquisition Mode** drop-down options, select **Live** if waveform acquisition and analysis will be performed on an online Infiniium Oscilloscope, else select **Offline**.

5 Click **OK** to exit the **Test Setup** window.

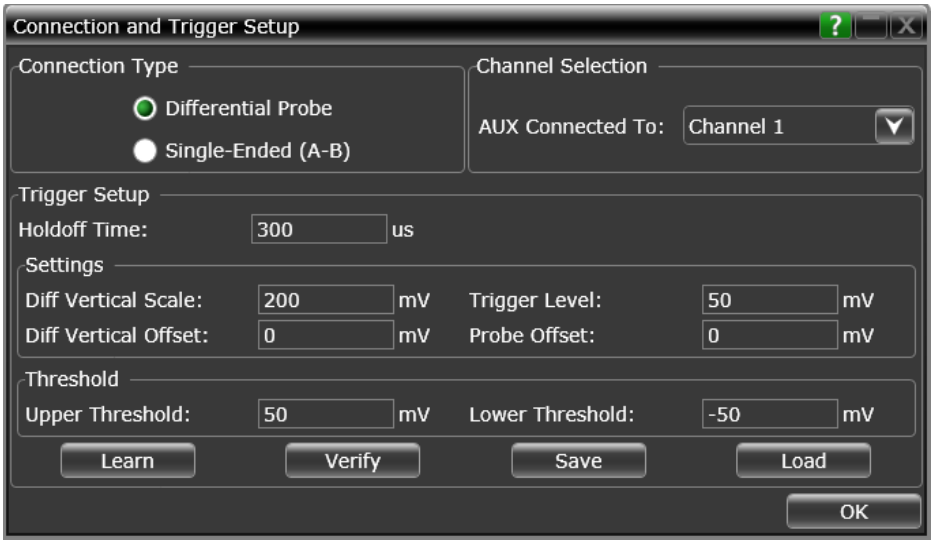


6 Click the **Connection Setup** button that now appears on the **Set Up** tab.

7 On the **Connection and Trigger Setup** window,

a Select either **Differential Probe** or **Single-Ended (A-B)** in the **Connection Type** area, depending on the probe connection you are using.

b From the **AUX Connected To:** drop-down options of the **Channel Selection** area, select the Oscilloscope Channel where the Auxiliary Lane is connected to.



c In the **Trigger Setup** area, define the Oscilloscope parameters to trigger on an Auxiliary signal during testing.

- **Hold Off Time** – The oscilloscope minimum hold off time before triggering the next waveform. Note that any Auxiliary transaction from the source must receive a reply from the sink in 400 us, else such a transaction is considered a timeout. Hold off time, in such cases, represents the minimum idle time before each Aux transaction is initialized. It is defaulted to 300 us which is a safe timing value for most devices tested in the lab. Most devices respond much faster than 300 us.
- **Trigger Level** – The AUX Channel signal level on which to trigger. Note that for a bi-directional signal (where a reference sink is attached), you must set the trigger level such that it crosses both the source command and the sink reply signal. Figure shows correct and incorrect trigger levels.

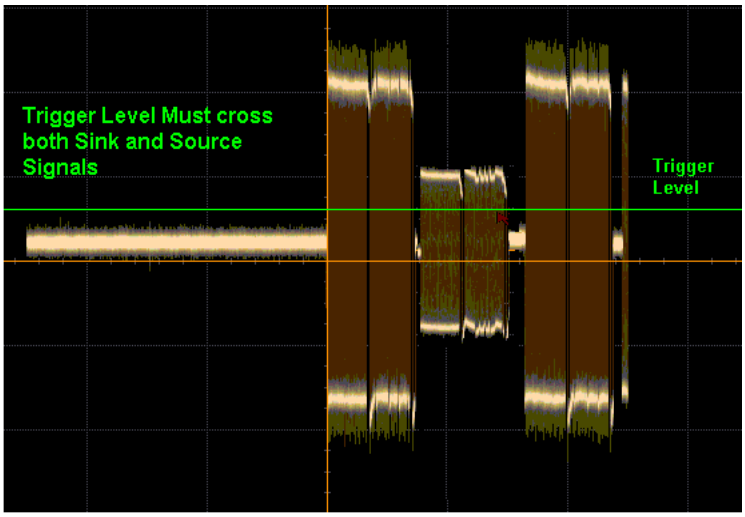


Figure 153 Correct Trigger Level

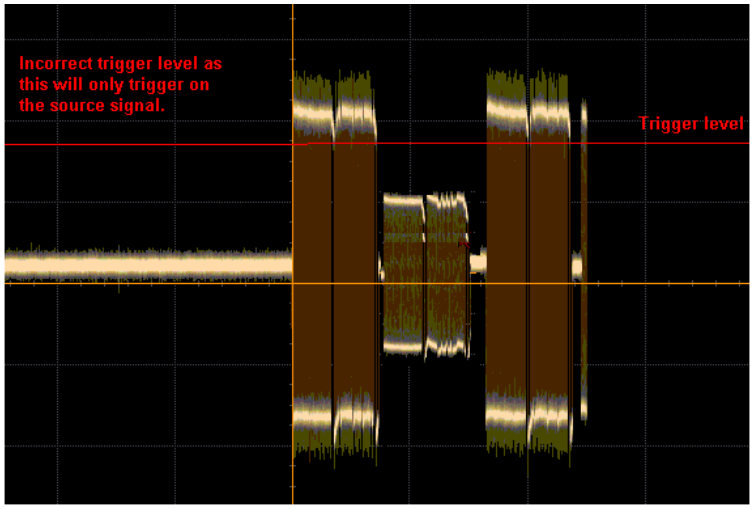


Figure 154 Incorrect Trigger Level

- **Vertical Scale** – The oscilloscope vertical scale. Set the vertical to make sure that all signals are visible on the oscilloscope display.

- **Vertical Offset** – The oscilloscope vertical offset. Set the offset so that the center point is aligned with the center of the oscilloscope display.
- **Upper Threshold/Lower Threshold** – The threshold level of signal must be set properly so that both upper and lower thresholds cross both the source and sink signals when the DUT is attached with a reference sink. The threshold levels are important parameters because they are used for edge detection when decoding a source command from a sink reply.

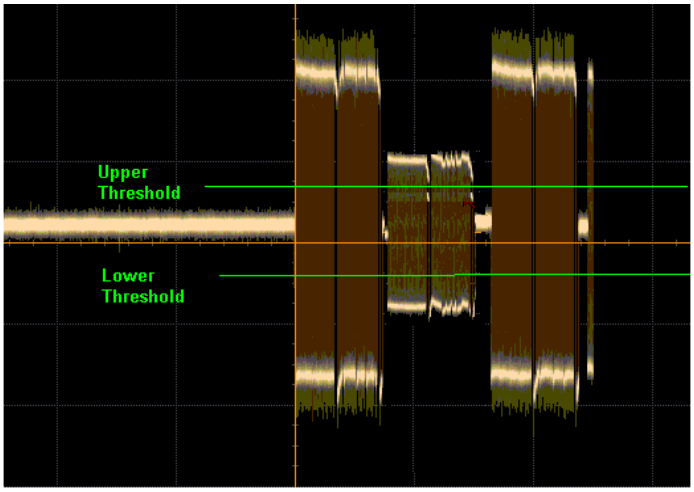
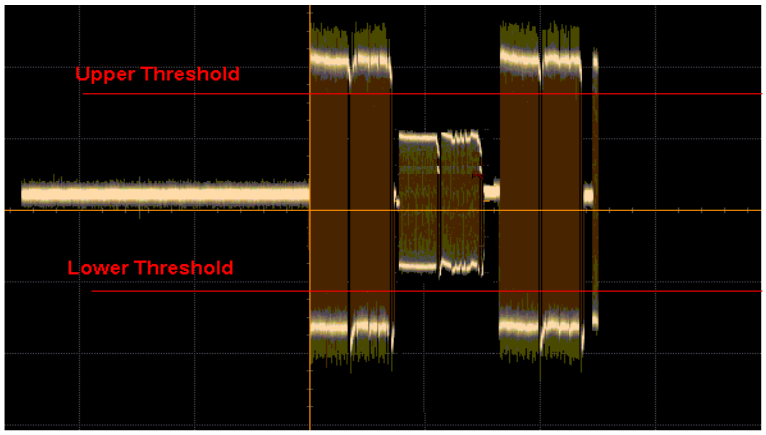


Figure 155 Correct Threshold set



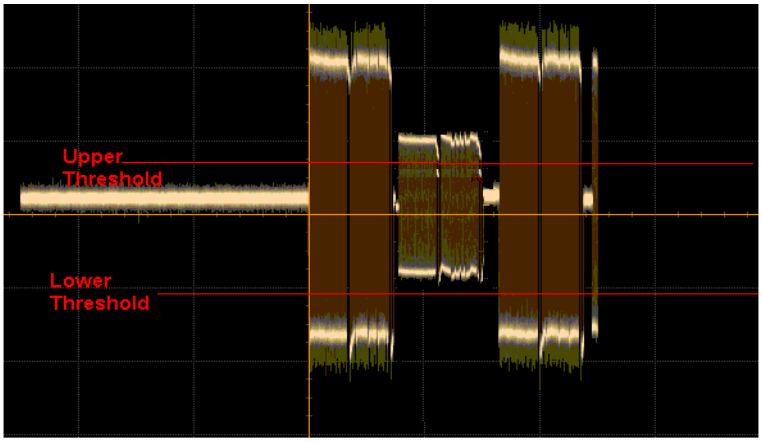


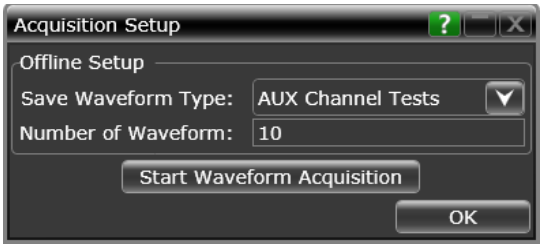
Figure 156 Wrong Thresholds set

- Click the **Learn** button to access the information guide about the trigger setup parameters. However, note that the learning guide may not necessarily work due to variation in the actual Auxiliary signals, owing to different manufacturers. Keysight recommends that you must check to make sure that the parameters are correctly set as previously described.
- Click **Verify** and follow the instructions, if you wish to check the AUX Channel trigger.
- You may **Save** or **Load** the trigger setup configuration as a **.tsf* file.

8 Click **OK** to exit the **Connection and Trigger Setup** window.

9 If you select the option **Offline** for the **Acquisition Mode** in the **Test Setup** window, the **Acquisition Setup** button appears in the **Test Environment Setup** area of the **Set Up** tab.

10 Click the **Acquisition Setup** button to save the waveform files so that you can avoid the manual process to initiate Auxiliary transactions during the time of test runs.



11 On the **Acquisition Setup** window,

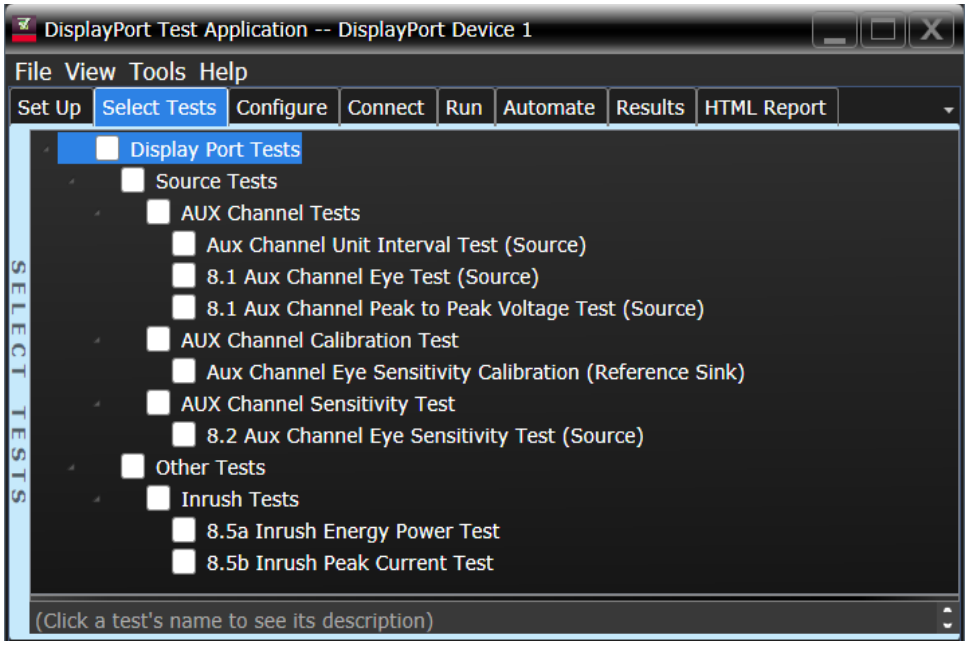
a select the type of waveforms to be saved from the **Save Waveform Type:** drop-down options.

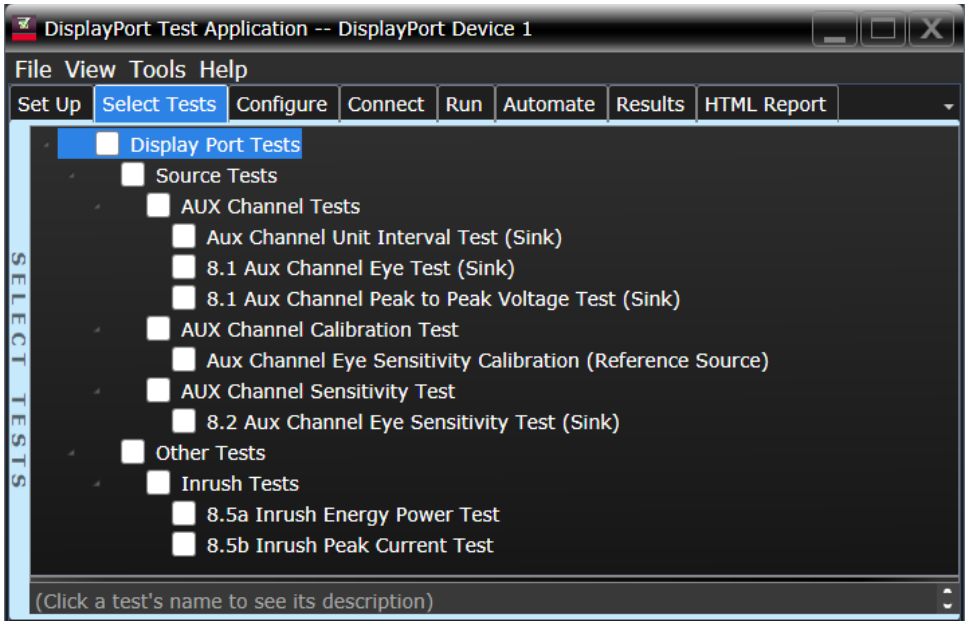
b define the number of waveforms to be saved in the **Number of Waveform:** field.

c Click the **Start Waveform Acquisition** button to start capturing and saving waveforms.

d Click **OK** to return to the **Set Up** tab.

12 Click the **Select Tests** tab where the AUX Channel tests for Source or Sink devices appear.


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Display Port Tests
Source Tests
AUX Channel Tests
Aux Channel Unit Interval Test (Source)
8.1 Aux Channel Eye Test (Source)
8.1 Aux Channel Peak to Peak Voltage Test (Source)
AUX Channel Calibration Test
Aux Channel Eye Sensitivity Calibration (Reference Sink)
AUX Channel Sensitivity Test
8.2 Aux Channel Eye Sensitivity Test (Source)
Other Tests
Inrush Tests
8.5a Inrush Energy Power Test
8.5b Inrush Peak Current Test
(Click a test's name to see its description)


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Display Port Tests
Source Tests
AUX Channel Tests
Aux Channel Unit Interval Test (Sink)
8.1 Aux Channel Eye Test (Sink)
8.1 Aux Channel Peak to Peak Voltage Test (Sink)
AUX Channel Calibration Test
Aux Channel Eye Sensitivity Calibration (Reference Source)
AUX Channel Sensitivity Test
8.2 Aux Channel Eye Sensitivity Test (Sink)
Other Tests
Inrush Tests
8.5a Inrush Energy Power Test
8.5b Inrush Peak Current Test
(Click a test's name to see its description)

Probing/Connection Set Up for AUX Channel Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests. When performing the Source AUX Channel tests, a Reference Sink device is required. Similarly, when performing the Sink AUX Channel tests, a Reference Source device is required.

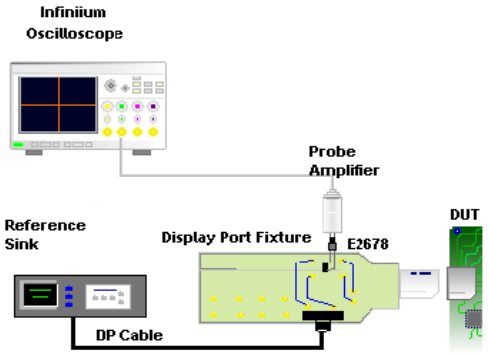


Figure 157 Sample connection diagram for source AUX channel tests with source DUT connected to a reference sink

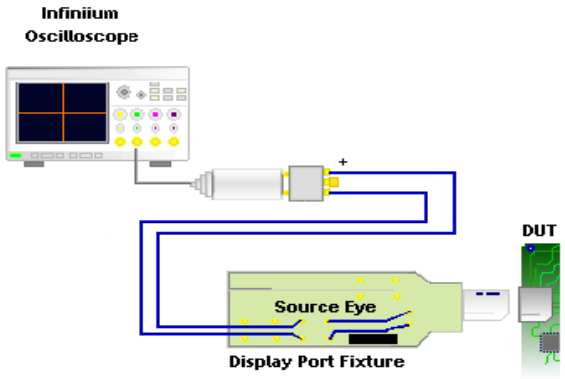


Figure 158 Sample connection diagram for source AUX channel tests without connecting to a reference sink

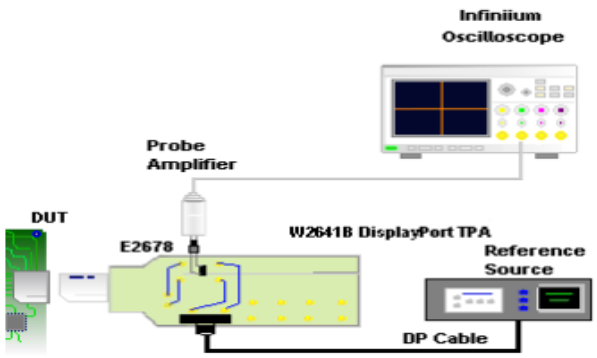


Figure 159 Sample connection diagram for sink AUX channel tests with sink DUT connected to a reference source

AUX Channel Unit Interval Test

Test ID

125000 – AUX Channel Unit Interval Test (Source)

125010 – AUX Channel Unit Interval Test (Sink)

Test Overview

The objective of the test is to evaluate the AUX Channel waveform, ensuring that the overall variation of the Manchester transaction Unit Interval stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Set up the parameter of the measurement trend:

   a Set up the Unit Interval measurement for the differential AUX Channel signal.

   b Set up the frequency measurement for the Clock signal.

   c Set up the measurement trend.

6 Set up the waveform Histogram on the measurement trend:

   a Initialize AUX Channel transactions and acquire the differential AUX Channel signal.

   b Identify the first and the last points for the desired transaction.

   c Zoom-in on the desired transaction.

   d Set up the Vertical Waveform Histogram on the measurement trend within the desired transaction.

   e Obtain the measurement for the mean, maximum and minimum values of the waveform Histogram.

7 Repeat step 6 ten times.

8 Report the measurement results.

PASS Condition

Manchester Transaction Unit Interval (UI_{MAN}):

Minimum = 0.4 µsec

Maximum = 0.6 µsec

Test References

See:

- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.4.2, Table 3-5*

Expected/Observable Results

The measured unit interval for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Test

Test ID

125001 – AUX Channel Eye Test (Source)

125011 – AUX Channel Eye Test (Sink)

Test Overview

The objective of this test is to evaluate the transmitter AUX Channel waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Apply a 300 kHz low-frequency cutoff (high-pass filter) to minimize impact caused due to baseline wander.

7 Apply a 500 MHz high-frequency cutoff (low-pass filter) to minimize impact caused due to instrument noise.

8 Apply measurement window on the AUX Channel signals, which starts immediately after the second pulse and ends immediately before auxiliary stop condition of the signal.

9 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

10 Set up the waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

11 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.
   c Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.
12 Check for any signal trajectories entering into the mask.
13 Report the measurement results.

PASS Condition

PASS Value = 290mV_diff_pp or higher

FAIL Value = lower than 290mV_diff_pp

Table 177 Eye Mask Vertices for AUX Channel for Manchester Transactions

Mask Point	Time (from EYE Center)	Minimum Voltage Value at Six Vertices (mV)
1	-185ns	0
2	-135ns	145
3	135ns	145
4	185ns	0
5	135ns	-145
6	-135ns	-145

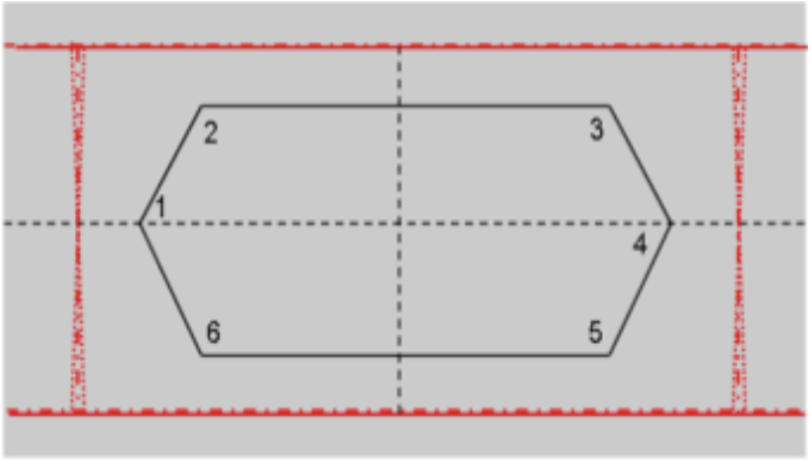


Figure 160 AUX Channel EYE Mask for Manchester Transactions

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.1*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.4.2.5, Figure 3-10 and Table 3-7*

Expected/Observable Results

The measured eye diagram for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

AUX Channel Peak-to-Peak Voltage Test

Test ID

125002 – AUX Channel Peak-to-Peak Voltage Test (Source)

125012 – AUX Channel Peak-to-Peak Voltage Test (Sink)

Test Overview

The objective of the test is to evaluate the transmitter AUX Channel Waveform, ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

7 Set up the horizontal waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

8 If you have selected the “AUX Channel Eye Test” under the **Select Tests** tab of the compliance application:

   a Set up the parameter of the Mask Test:

      i Load the eye mask based on the settings in the Configuration Variable.

      ii Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

      iii Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.

   b Check for any signal trajectories entering into the mask.

9 Report the measurement results.

PASS Condition

Table 178 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage at a transmitting device ($V_{AUX\text{-}DIFFp\text{-}p}$)	0.29V	1.38V

Test References

See:

- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.4.2, Table 3-5*

Expected/Observable Results

The measured peak-to-peak voltage for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Slew Rate Test

Test ID

125003 – AUX Channel Slew Rate Test (Source)

125013 – AUX Channel Slew Rate Test (Sink)

Test Overview

The objective of the test is to evaluate the AUX signaling edge rates, thereby ensuring that any crosstalk to the Main-Link signals are minimized.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

a Enable measurement of all edges to obtain a statistical value of the measurement.

b Set up the measurement threshold.

c Set up the Clock Recovery.

5 Set up the parameters to perform High Level Voltage (V_{HIGH}) and Low Level Voltage (V_{LOW}) for AUX Channel signal.

a Find V_{HIGH} by measuring the mode voltage of the high level of AUX Channel.

b Find V_{LOW} by measuring the mode voltage of the low level of AUX Channel.

c Calculate the peak-to-peak differential voltage of the AUX Channel signal and denote this value as $V_{Aux\_PP\_Diff\_Mean}$.
Note: Ignore any overshoot or ringing that follows the positive or negative transition.

d Calculate the time taken by the AUX Voltage to rise or fall between V20% and V80% levels. Denote this value at ΔT20-80%, which is either Rising Time at 20%-80% (RT20_80) or Falling Time at 20%-80% (FT20_80).

6 Calculate slew rate for all edges within the Capture window.

a The minimum value of Rising or Falling Time (in ns), denoted as ΔT20-80%_min, is measured as the worst-case slew rate.

b Multiply the value of $V_{Aux\_PP\_Diff\_Mean}$ (measured in step 5c) by 60% and denote the derived value as ΔV20-80%.

7 To determine the slew rate between the V20% and V80% vertices, calculate the rate of change using the following equation:
Slew Rate = Rate of Change = Rise/Run
= ΔV20-80% / ΔT20-80%
= ($V_{Aux\_PP\_Diff}$ x 0.6) / ΔT20-80%_min (V/ns)

8 Report the measurement results.

PASS Condition

The Slew Rate must be less than or equal to 375mV/ns for all transitions within the measurement window.

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.3*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.4.2, Table 3-5*

Expected/Observable Results

The measured Slew Rate for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Calibration Test

Test ID

125021 – AUX Channel Eye Sensitivity Calibration (Reference Sink)

125031 – AUX Channel Eye Sensitivity Calibration (Reference Source)

Test Overview

The objective of this test is to calibrate the peak-to-peak voltage of the transmitter AUX Channel waveform by reference device (reference source or reference sink), ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.

2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

4 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

5 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

6 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

7 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

8 Set up the waveform Histogram on the AUX Channel eye diagram:

   a Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.

   b Set up the vertical waveform Histogram of width 0.6 UI at the center of the AUX Channel eye diagram.

   c Measure the V_{TOP} and V_{BASE} using the waveform Histogram mean value.

9 Repeat Step 8 three times.

10 Report the measurement results.

PASS Condition

Table 179 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage for AUX Channel Eye Sensitivity	0.24V	0.28V

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.3*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.4.2, Table 3-5*

Expected/Observable Results

The measured peak-to-peak voltage for the AUX Channel signal by reference device (reference source or reference sink) shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Test

Test ID

125041 – AUX Channel Eye Sensitivity Test (Source)

125051 – AUX Channel Eye Sensitivity Test (Sink)

Test Overview

The objective of the test is to evaluate the sensitivity to the AUX Channel Eye Opening of the DUT as per the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.

2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

4 Set up the parameter of the measurement:

a Enable measurement of all edges to obtain a statistical value of the measurement.

b Set up the measurement threshold.

c Set up the Clock Recovery.

5 Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.

6 Check if the reference device could detect the transaction or not.

7 Decode the AUX Channel signal and check whether the transaction passed or failed.

8 Report the measurement results.

PASS Condition

Determine whether the AUX Channel communication is successful. For example, the Transmitter DUT sends an AUX Request to the Reference Receiver. The Reference Receiver acknowledges and the Transmitter DUT responds to the to indicate that the acknowledgment was successfully received.

PASS = No errors observed in the response

FAIL = One or more errors observed

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.3*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.4.2, Table 3-5*

Expected/Observable Results

The measured AUX Channel transaction shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

23 DPoC 1.4a Inrush Tests

Overview

The specifications and the conceptual information for the DPoC 1.4a standard are aligned with that for the DisplayPort 1.4 standard. For more information, refer to "Overview" on page 408.

Setting Up the DisplayPort Compliance Test Application for DPoC 1.4a Inrush Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort Standards with Type-C capability, select the option **DPoC 1.4a** in the **Test Specification** area.
5. Select the option **AUX PHY and Inrush Tests** in the **Test Selection** area.
6. In the **Type-C Environment Setup** area, select **Enable Type-C Controller** to activate the **DUT Orientation** field and the **Setup Type-C Controller** button. To know about how to configure the Type-C Controller, refer to the *Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help*.
7. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
8. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
9. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
10. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
11. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
12. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
13. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
14. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Refer to "Settings for AUX PHY and Inrush Tests" on page 1014 for instructions on setting the DPoC 1.4a InRush tests.

Inrush Energy Power Test

Test ID

127000 – Inrush Energy Power Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush energy power measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Energy $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 13.5$ Amps

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.6*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.2.3*

Expected/Observable Results

The measured worst case inrush energy power for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Inrush Peak Current Test

Test ID

127001 – Inrush Peak Current Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush peak current measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Energy $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 13.5$ Amps

Test References

See:

- *VESA DisplayPort Version 1.4a PHY Layer Compliance Test Specification Version 1.1, Section 9.6*
- *VESA DisplayPort (DP) Standard Version 1.4a, Section 3.2.3*

Expected/Observable Results

The measured worst case inrush peak current for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

24 DPoC Source Tests

Overview

The specifications and the conceptual information for the DPoC standard are aligned with that for the DisplayPort 1.4 standard. For more information, refer to "Overview" on page 250.

Setting Up the DisplayPort Compliance Test Application for DPoC Source Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort Standards with Type-C capability, select the option **DPoC** in the **Test Specification** area.
5. The option **Physical Layer Tests** appears by default in the **Test Selection** area.
6. Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.
7. In the **Type-C Environment Setup** area, select **Enable Type-C Controller** to activate the **DUT Orientation** field and the **Setup Type-C Controller** button. To know about how to configure the Type-C Controller, refer to the *Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help*.
8. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
9. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
10. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
11. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
12. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
13. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
14. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
15. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DPoC Source Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

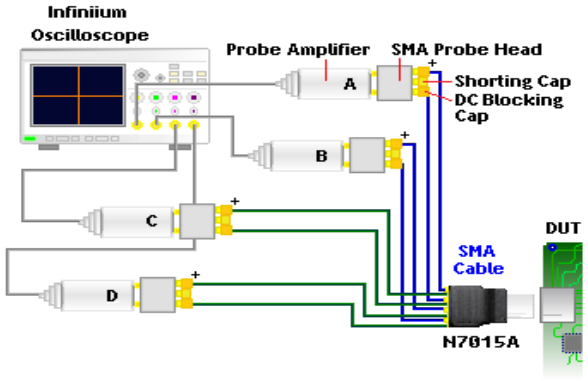


Figure 161 Sample connection diagram for DPoC Source Differential Tests

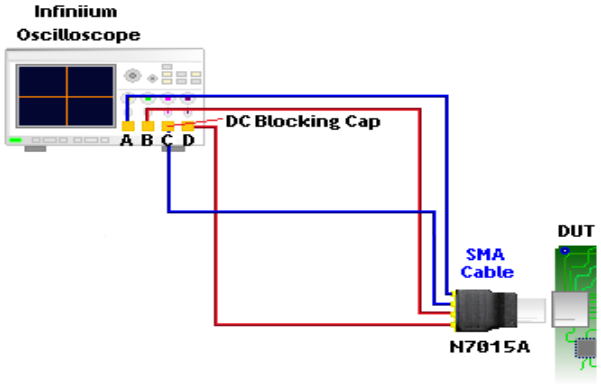


Figure 162 Sample connection diagram for DPoC Source Single-Ended Tests

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Source tests (either differential or single-ended) to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1 In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.

2 On the **Test Setup** window,

a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b In the **DUT Info** area, the **Device Type** is selected as **Source** by default. The **Connector Type** is grayed out. From the drop-down options for **Alt Mode**, select either **Alt Mode: DP 4 Lanes** or **Alt Mode: DP 2 + 2**.

c In the **Test Info** area, the **Test Type** is selected as **Differential Tests** by default. Select **Single-Ended Tests** from the drop-down options for the respective tests to appear in the **Select Tests** tab. From the **Data Pattern** drop-down options, select **Standard DP Pattern** or **Arbitrary Pattern**, based on the type of pattern generated.

d In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.

e In the **Power Profile** area, select the **Provider Power Profile** or **Consumer Power Profile** or both options, to include the Voltage and Current specifications to be tested. The appearance of the options depends on the power profiles supported by the DUT.

3 Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1 Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.

2 On the **Connection Setup** window,

a Select the appropriate option (**Keysight N7015A** or **Other**) in the **Fixture Type** to indicate where the DUT is connected to.

b Select either **Without Cable** or **With Cable** to indicate the type of the connected **N7015A** fixture.

c Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.

d In the **Channel Selection** area, assign appropriate channels to lanes.

3 Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of source tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for DPoC Source Tests" on page 872 to complete the task flow for DUT setup along with configuring the Compliance Application to run each test.

Source Eye Diagram Test

Test ID

For Standard DP Pattern:

- 1210001, 1210002, 1210003, 1210004 – Eye Diagram Test

For Arbitrary Pattern:

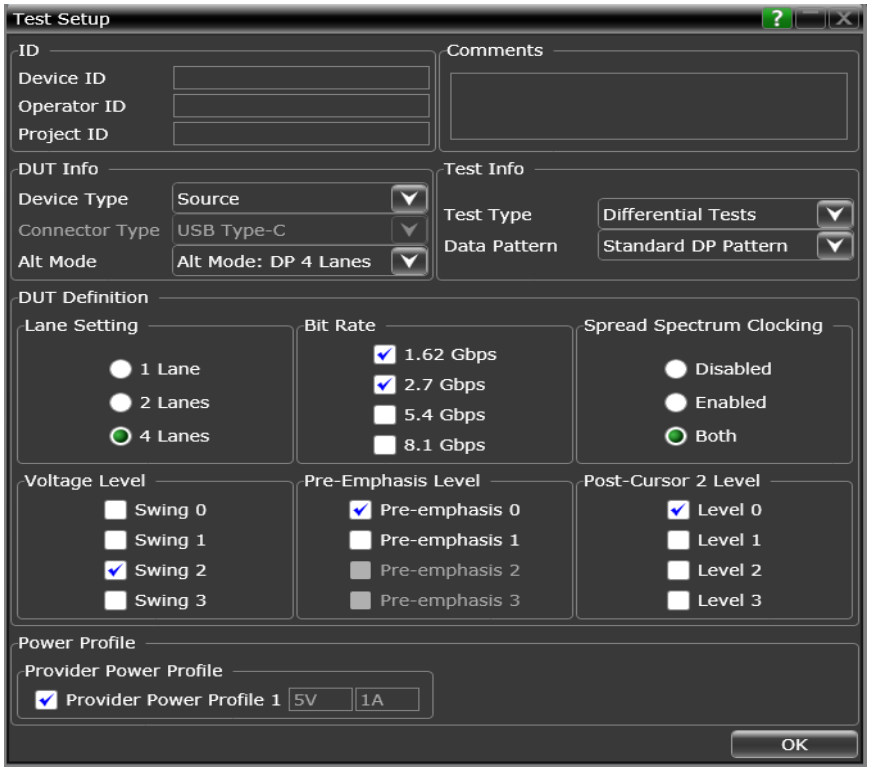
- 1310001, 1310002, 1310003, 1310004 – Eye Diagram Test

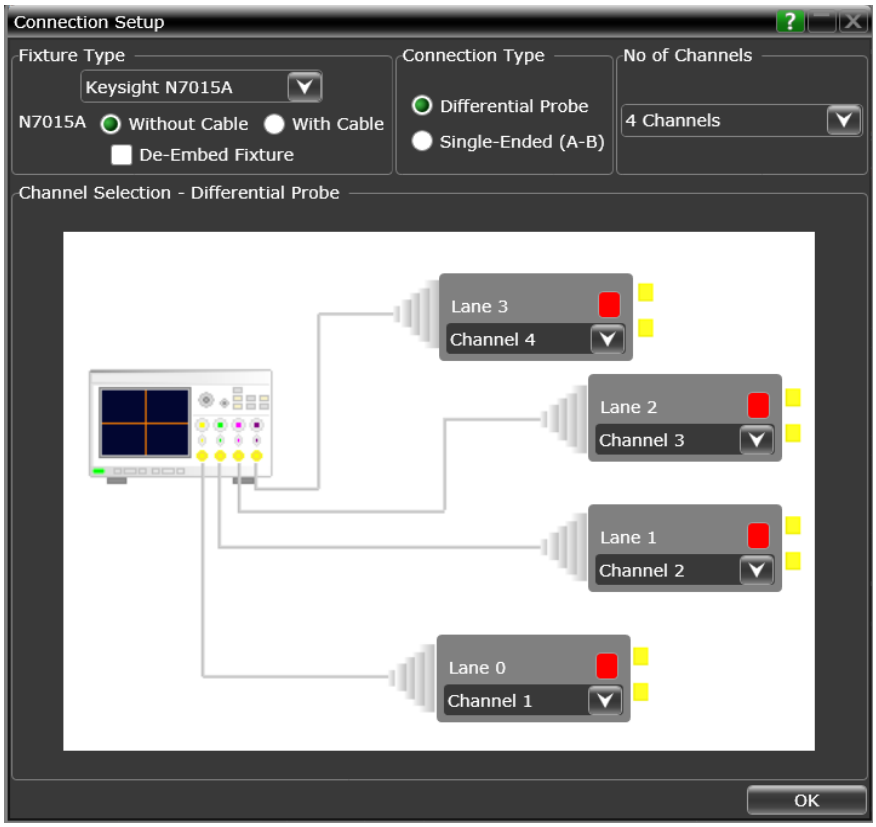
Test Overview

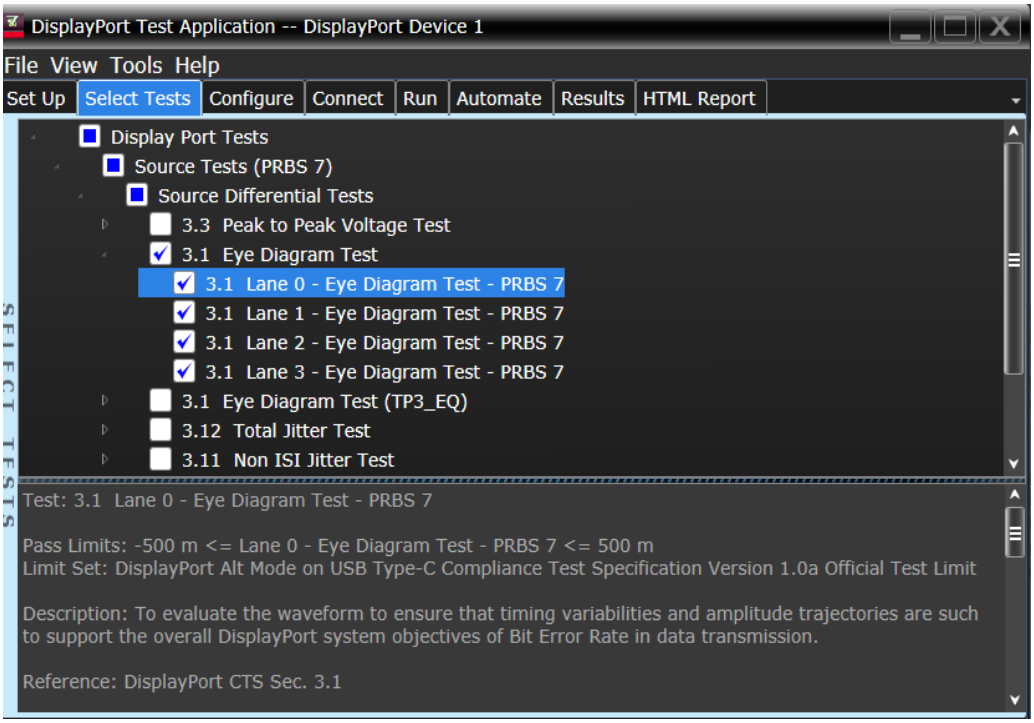
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Swing 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Measure V_{TOP} and V_{BASE} of the input signal using the pattern folding.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the input signal eye diagram to measure the left edge.
7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the eye height of the eye diagram using the Histogram.
9 Measure the jitter of the eye diagram using the Histogram.
10 Calculate the eye width based on the measured jitter of the eye diagram.

11 Check for any signal trajectories that may have entered into the mask.

12 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 180 shows the voltage and time coordinates for the mask used in the eye diagram.

Table 180 Eye Diagram Mask Coordinates

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	**High (2.7 Gb/s)**
1	0.127, 0.000	0.210, 0.000
2	0.291, 0.160	0.355, 0.140
3	0.500, 0.200	0.500, 0.175
4	0.709, 0.200	0.645, 0.175
5	0.873, 0.000	0.790, 0.000
6	0.709,-0.200	0.645,-0.175
7	0.500,-0.200	0.500,-0.175
8	0.291,-0.160	0.355,-0.140

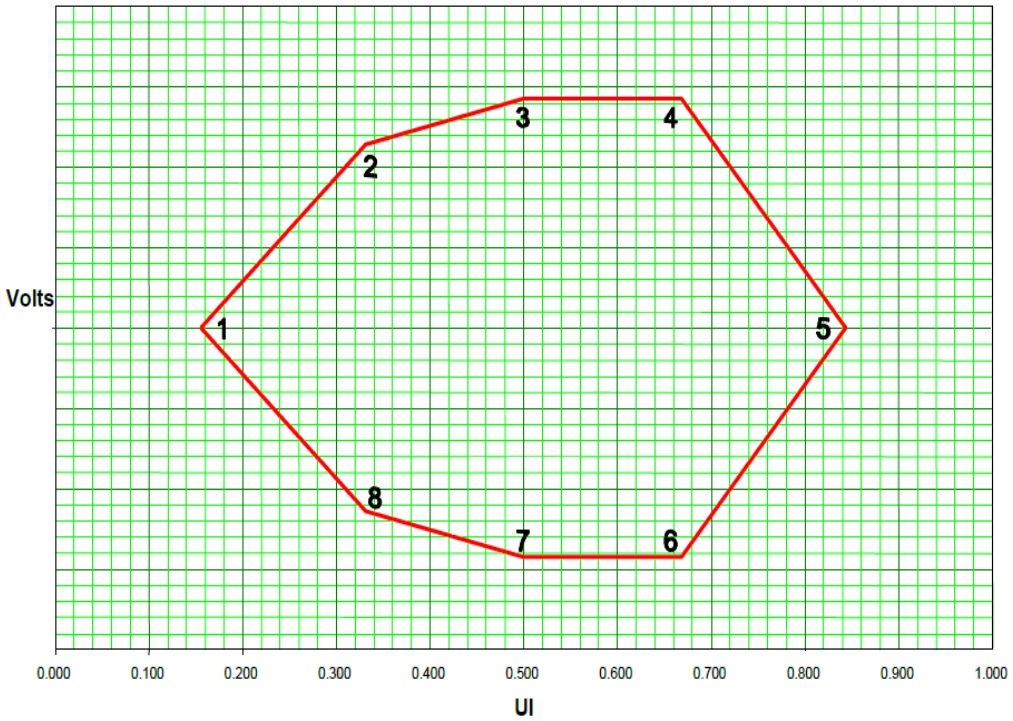


Figure 163 The Source Eye Mask

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort Standard Version 1.4, Section 3.5.2.8.2, Table 3-28 for RBR, Table 3-27 for HBR*

Expected/Observable Results

The measured eye diagram for the source degraded signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test

Test ID

For Standard DP Pattern:

- 1220001, 1220002, 1220003, 1220004 – Total Jitter Test

For Arbitrary Pattern:

- 1320001, 1320002, 1320003, 1320004 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

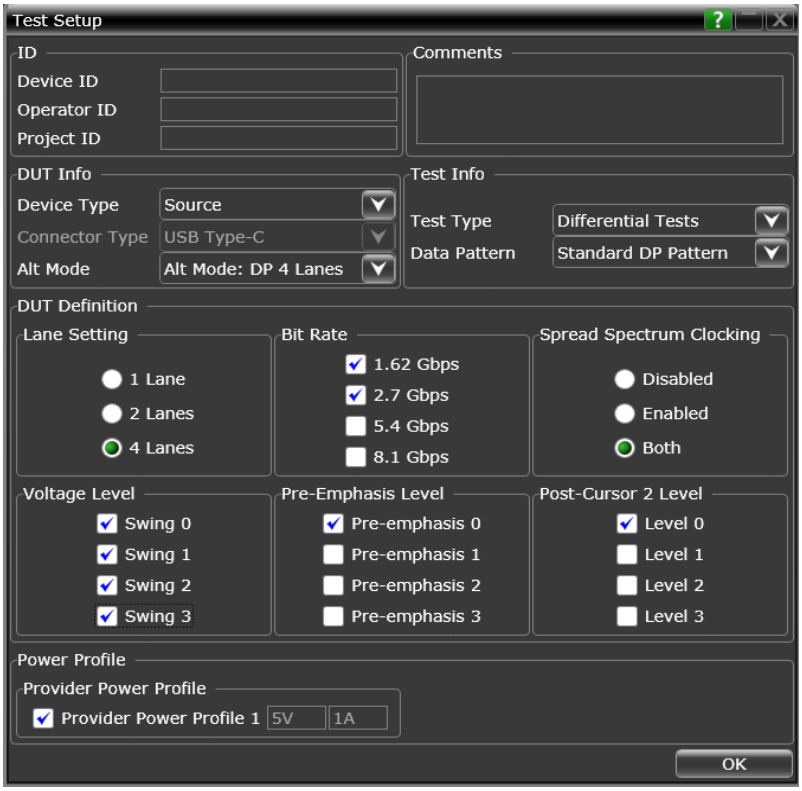
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

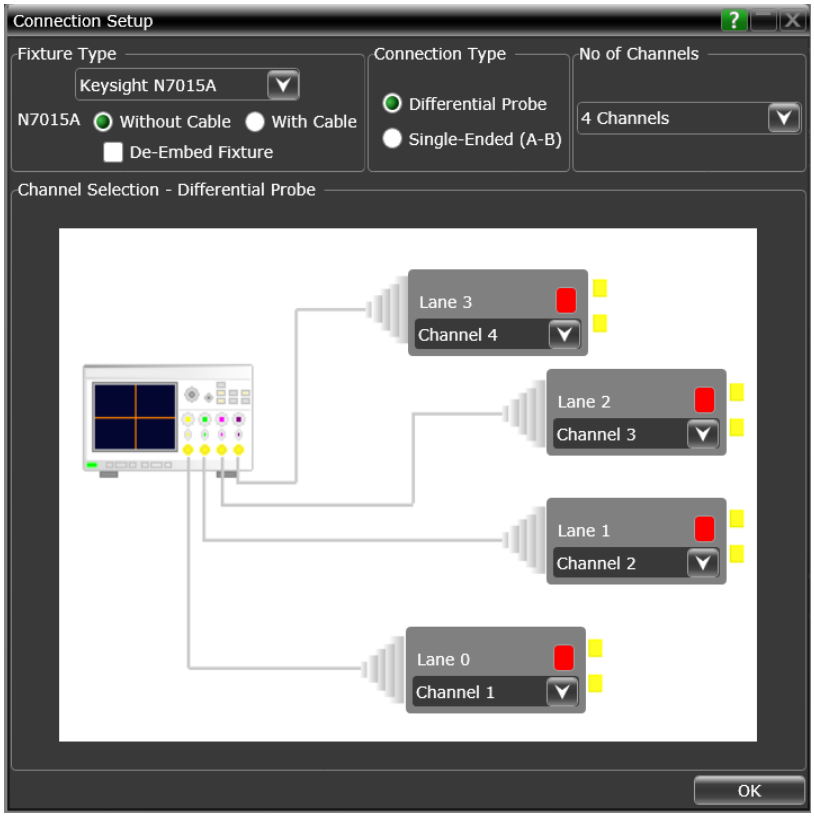
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

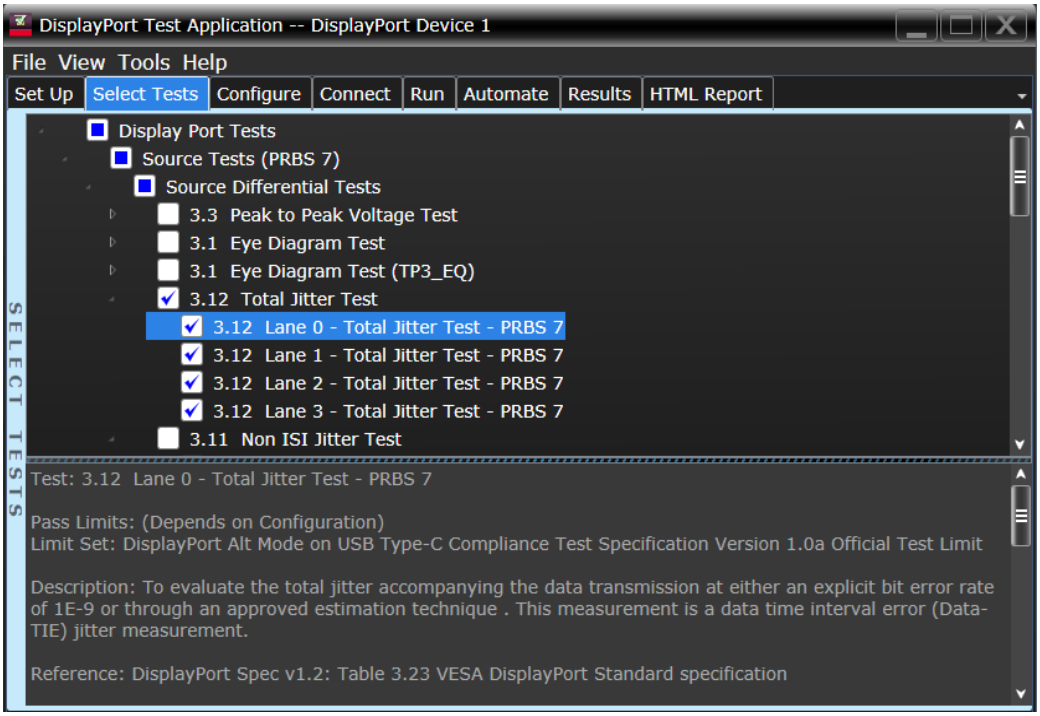
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Report the measurement results.

PASS Condition

Table 181 Total Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
Ap-p	0.294 UI	0.420 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
Ap-p	0.180 UI	0.270 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2.7.2, Table 3-23*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non-ISI Jitter Test

Test ID

For Standard DP Pattern:

- 1230001, 1230002, 1230003, 1230004 – Non ISI Jitter Test

For Arbitrary Pattern:

- 1330001, 1330002, 1330003, 1330004 – Non ISI Jitter Test

Test Overview

The objective of the test is to evaluate the amount of Non ISI jitter accompanying the data transmission.

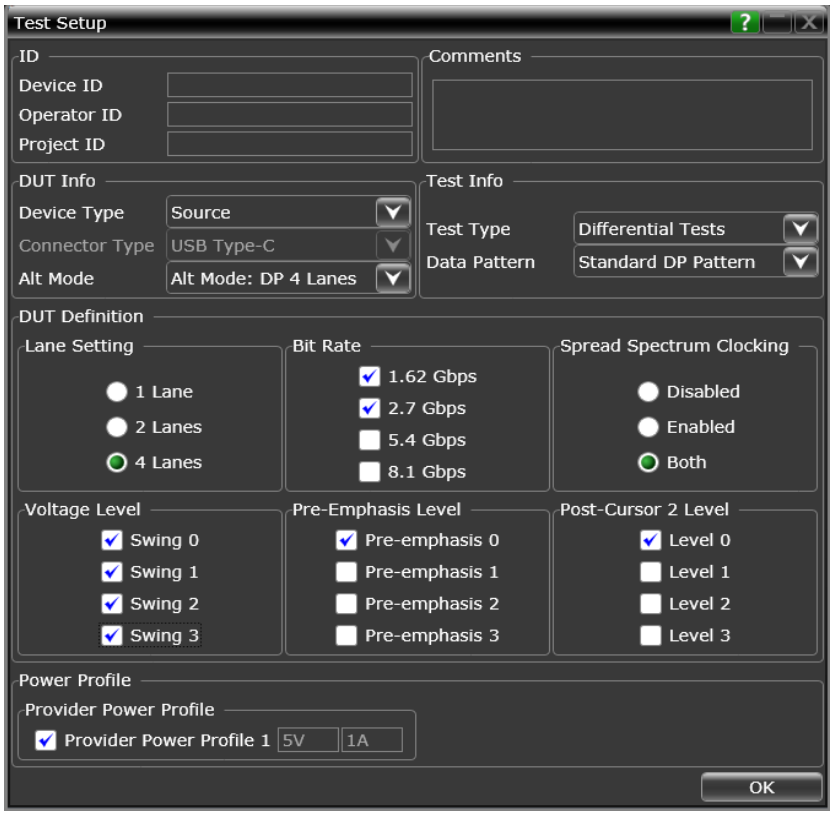
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

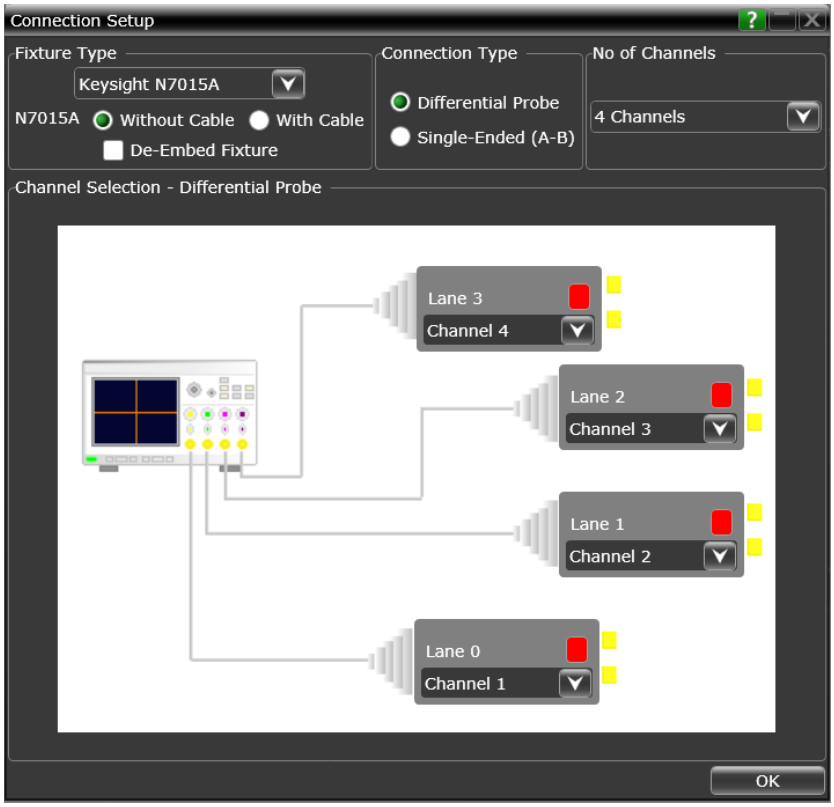
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

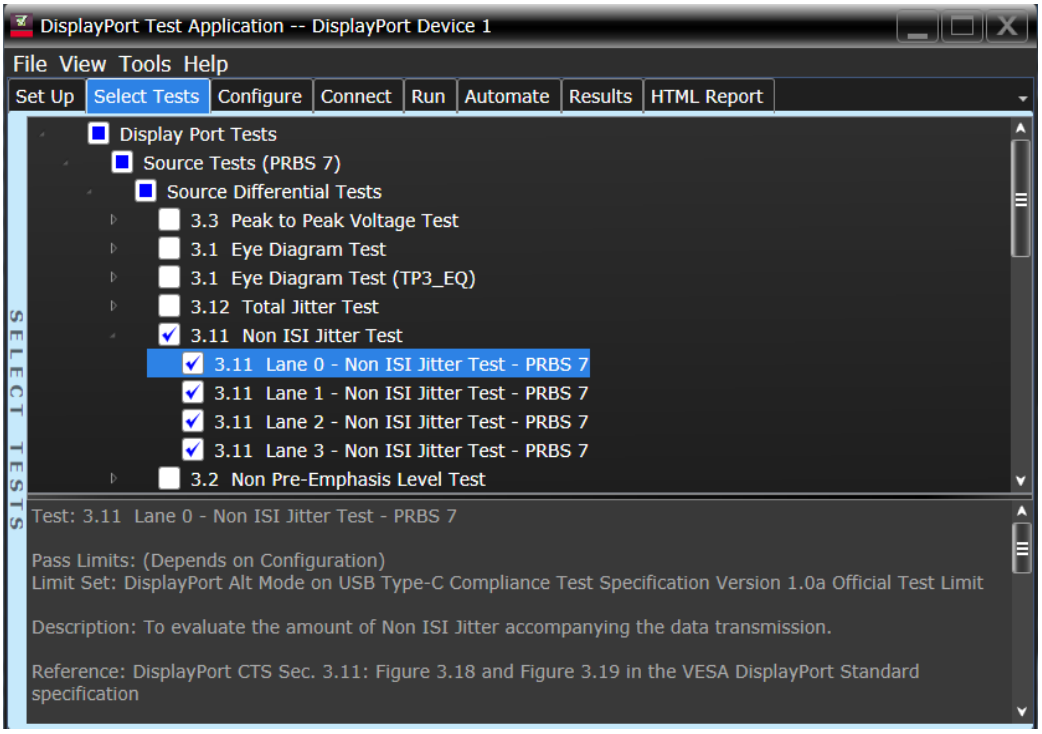
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Calculate the Non ISI jitter using the following equation:

$$\text{Non ISI Jitter} = \text{TJ} - \text{ISI}$$

7 Report the measurement results.

PASS Condition

Table 182 Non-ISI Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.260 UI	0.276 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.160 UI	0.170 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.11*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2.7.2, Table 3-23*

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Pre-Emphasis Level Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1261001, 1261002, 1261003, 1261004 – Non Pre-Emphasis Level Test (Swing 1/Swing 0)
- 1262001, 1262002, 1262003, 1262004 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263001, 1263002, 1263003, 1263004 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

For Standard DP Pattern (HBR2 and HBR3):

- 1264101, 1264102, 1264103, 1264104 – Non Pre-Emphasis Level Test (Swing 2/Swing 0)
- 1262101, 1262102, 1262103, 1262104 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263101, 1263102, 1263103, 1263104 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

For Arbitrary Pattern:

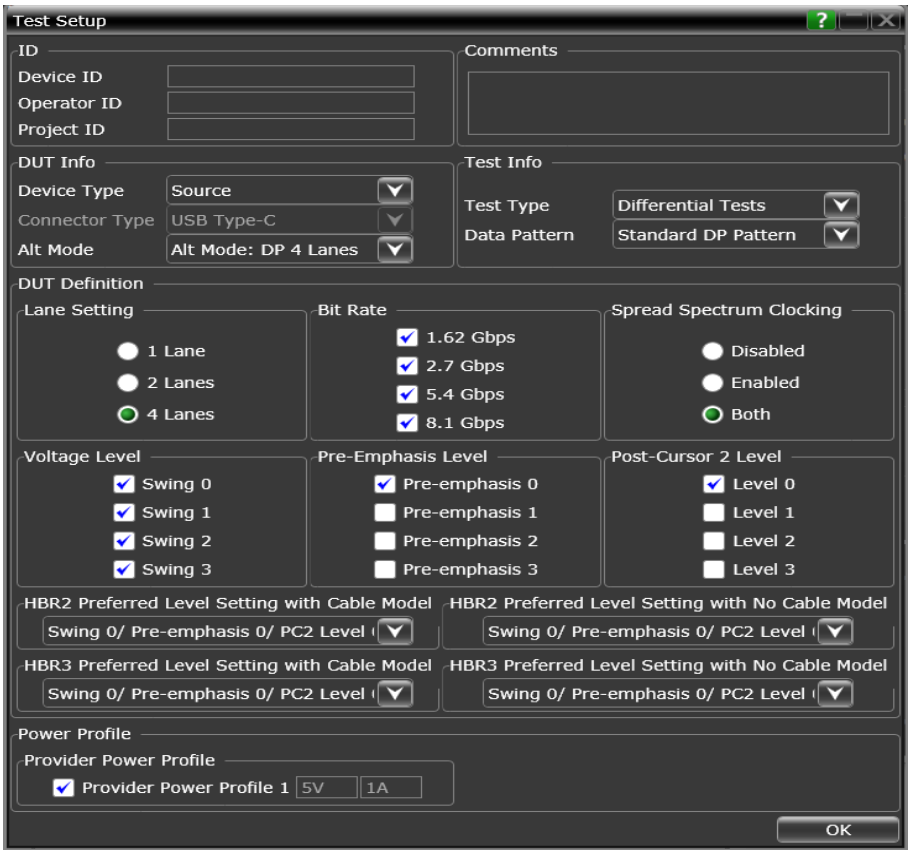
- 1364101, 1364102, 1364103, 1364104 – Non Pre-Emphasis Level Test (Swing 2/Swing 0)
- 1362101, 1362102, 1362103, 1362104 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1363101, 1363102, 1363103, 1363104 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

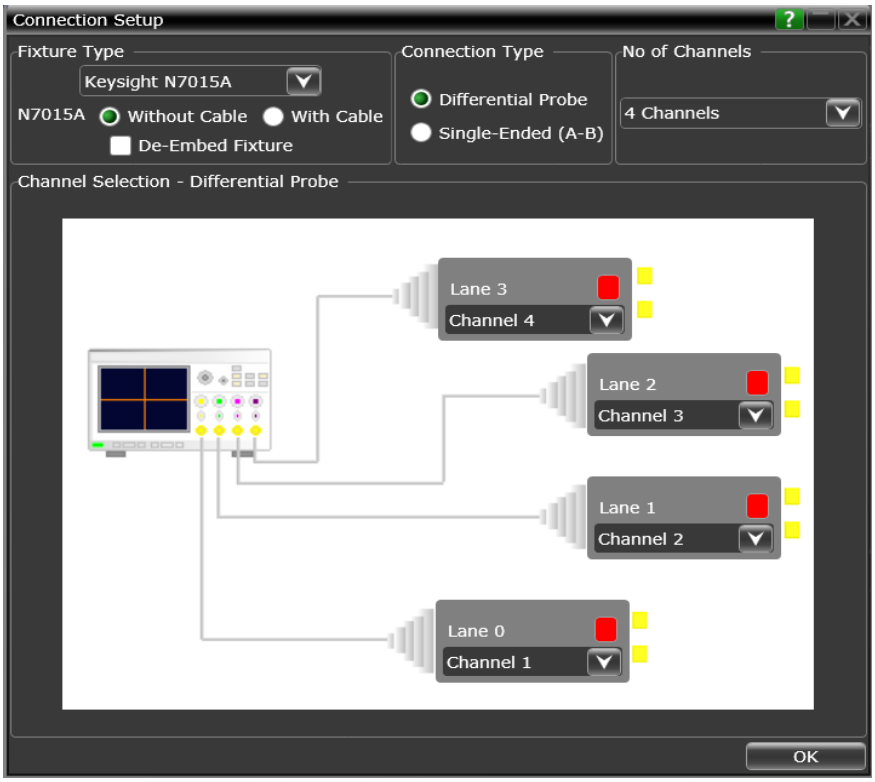
Test Overview

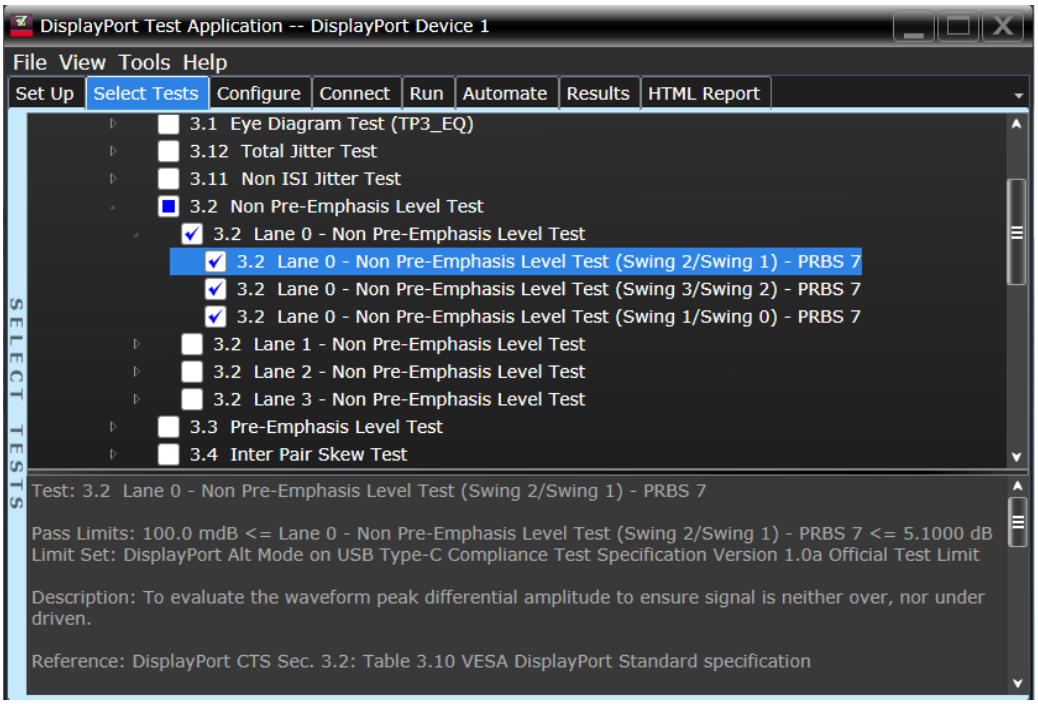
The objective of this test is to ensure that the system budget elements are obeyed and to ensure that the level settings are monotonic so that the sink relies on the source to incrementally increase upon request by the sink.

Test Conditions for Non Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR3 – PLTPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For Voltage Level A with no pre-emphasis level:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

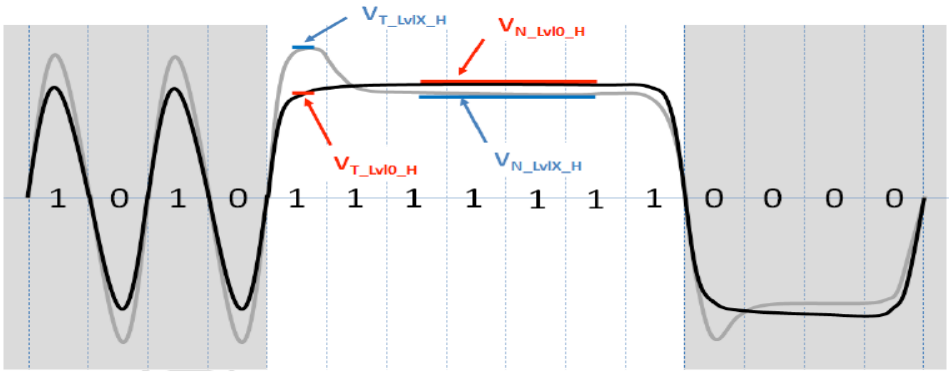


Figure 164 High Voltage measurement for RBR and HBR

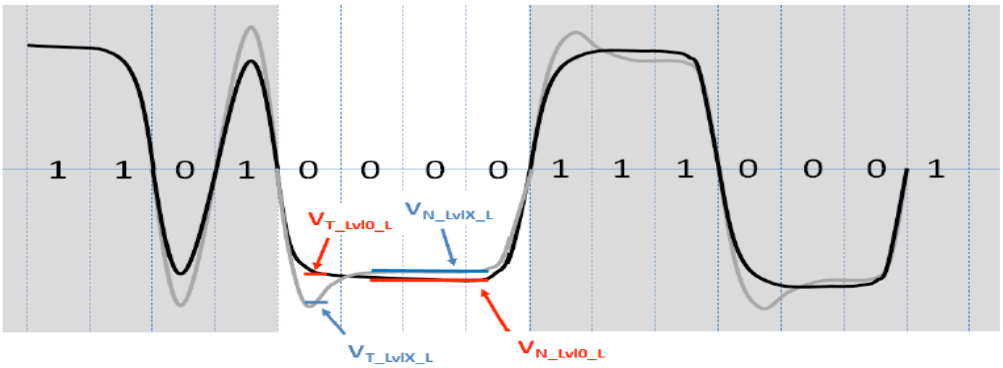


Figure 165 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR3 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted zeros of the pattern.

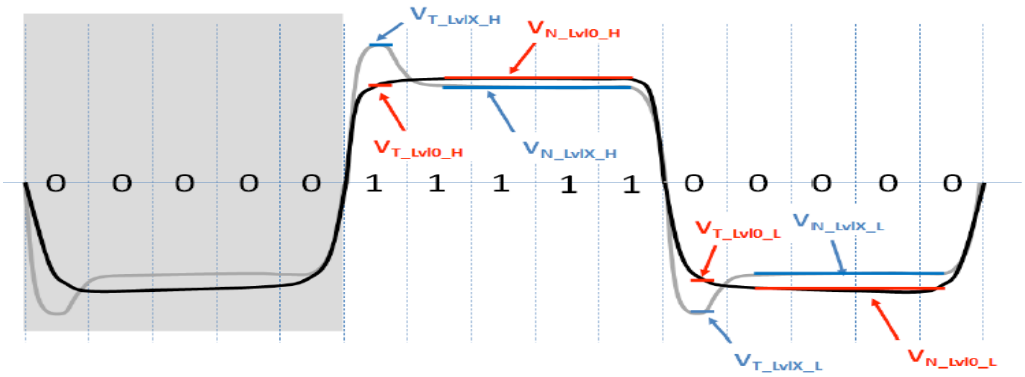


Figure 166 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_Lvl0\_PP} = V_{T\_Lvl0\_H} - V_{T\_Lvl0\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_Lvl0\_PP} = V_{N\_Lvl0\_H} - V_{N\_Lvl0\_L}$$

2 Repeat Step 1 for Voltage Level B with no pre-emphasis level.

3 Calculate the non pre-emphasis level output voltage ratio using the equation:

Non Pre-Emphasis Level = $20 * \text{Log}_{10}[\text{Voltage Level A } V_{N\_Lvl0\_PP} / \text{Voltage Level B } V_{N\_Lvl0\_PP}]$

4 Report the measurement results.

PASS Condition

For each level setting testes, the following equation should be used:

$\text{Resultant} = 20 * \text{Log}_{10}[\text{Voltage}_{\text{Peak-Peak\_LevelA}} / \text{Voltage}_{\text{Peak-Peak\_LevelB}}]$

Table 183 Compared Levels

Measurement#	$\text{Voltage}_{\text{Peak-Peak\_LevelA}}$	$\text{Voltage}_{\text{Peak-Peak\_LevelB}}$
RBR & HBR		
1	Level 1 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)
2	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
3*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)
HBR2 and HBR3		
4	Level 2 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)

Table 183 Compared Levels

Measurement#	$Voltage_{Peak\text{-}Peak\_LevelA}$	$Voltage_{Peak\text{-}Peak\_LevelB}$
5	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
6*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)

* if device optionally capable of Level 3

The resultants specifications are as identified below:

Measurement 1: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 2: 0.1 dB ≤ Resultant ≤ 5.1 dB

Measurement 3: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 4: 5.2 dB ≤ Resultant ≤ 6.9 dB

Measurement 5: 1.6 dB ≤ Resultant ≤ 3.5 dB

Measurement 6: 1 dB ≤ Resultant ≤ 4.4 dB

Table 184 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}OUTPUT\text{-}RATIO\_RBR\_HBR}$*	Ratio of Output Voltage Level 1/Level 0	0.8	-	6.0	dB	Measured on non-transition bits at Pre-emphasis level 0 setting. Support for Voltage Level 3 is optional.
	Ratio of Output Voltage Level 2/Level 1	0.1	-	5.1	dB	
	Ratio of Output Voltage Level 3/Level 2	0.8	-	6.0	dB	

* Earlier versions of DisplayPort have the Main-Link DPTX output voltage ratios to ensure that the DPTX supports the required range of output voltage levels. For HBR2 and higher, you need not test or specify exclusively because the compliance test point is moved to TP3_EQ. So, the ratio of output voltage levels is removed from the table above for HBR2 and above.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.2*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-18*

Expected/Observable Results

The measured output voltage level ratio of the non pre-emphasis level test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Pre-Emphasis Level Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1270001, 1270002, 1270003, 1270004 – Pre-Emphasis Level Test

For Standard DP Pattern (HBR2 and HBR3):

- 1270501, 1270502, 1270503, 1270504 – Pre-Emphasis Level Test

For Arbitrary Pattern:

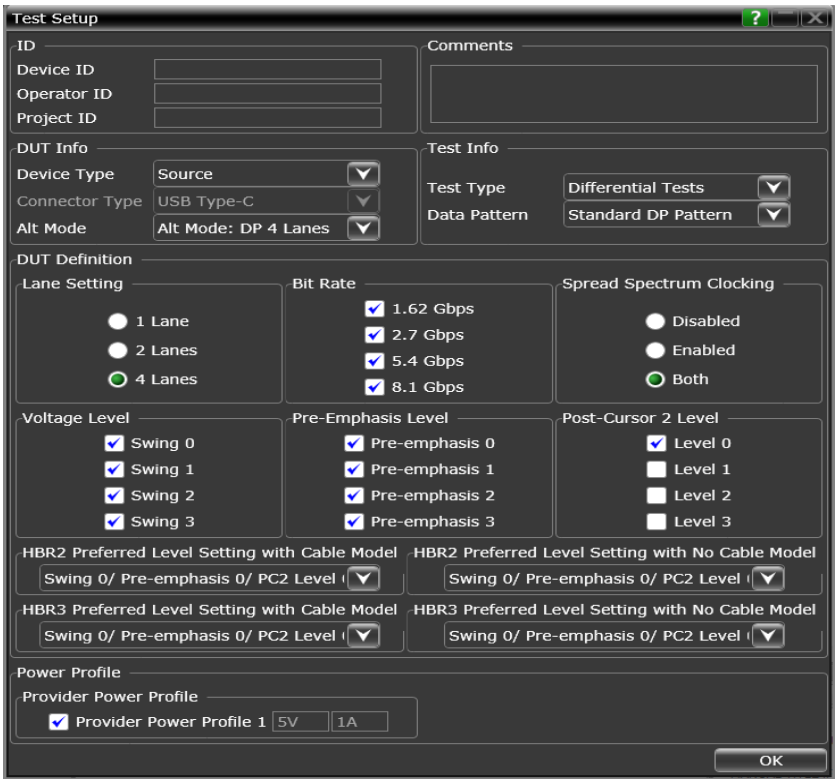
- 1370501, 1370502, 1370503, 1370504 – Pre-Emphasis Level Test

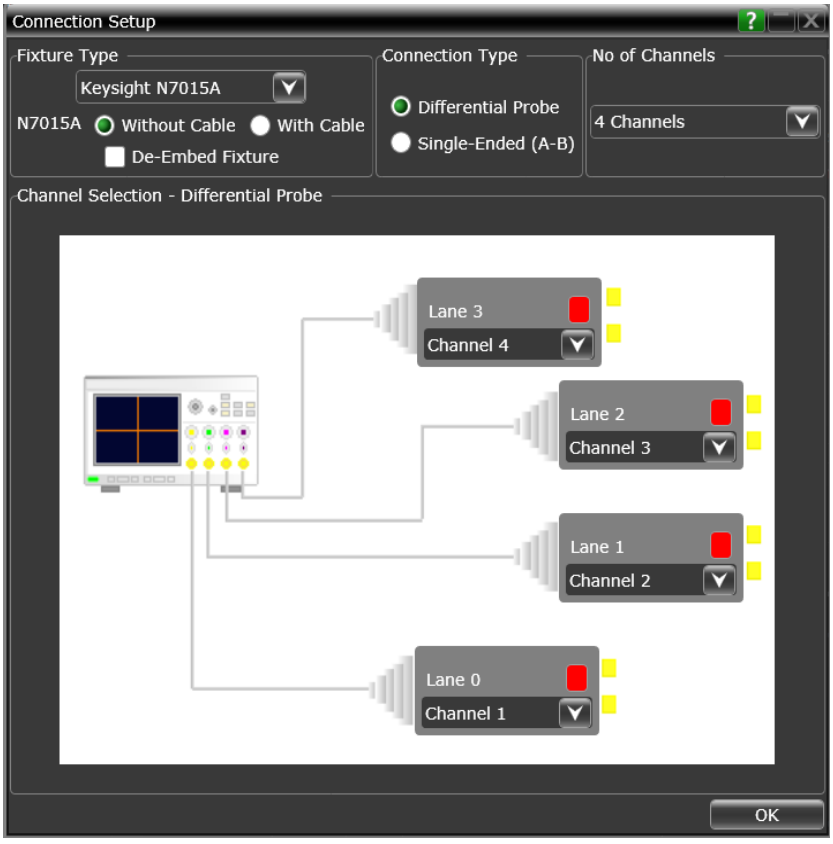
Test Overview

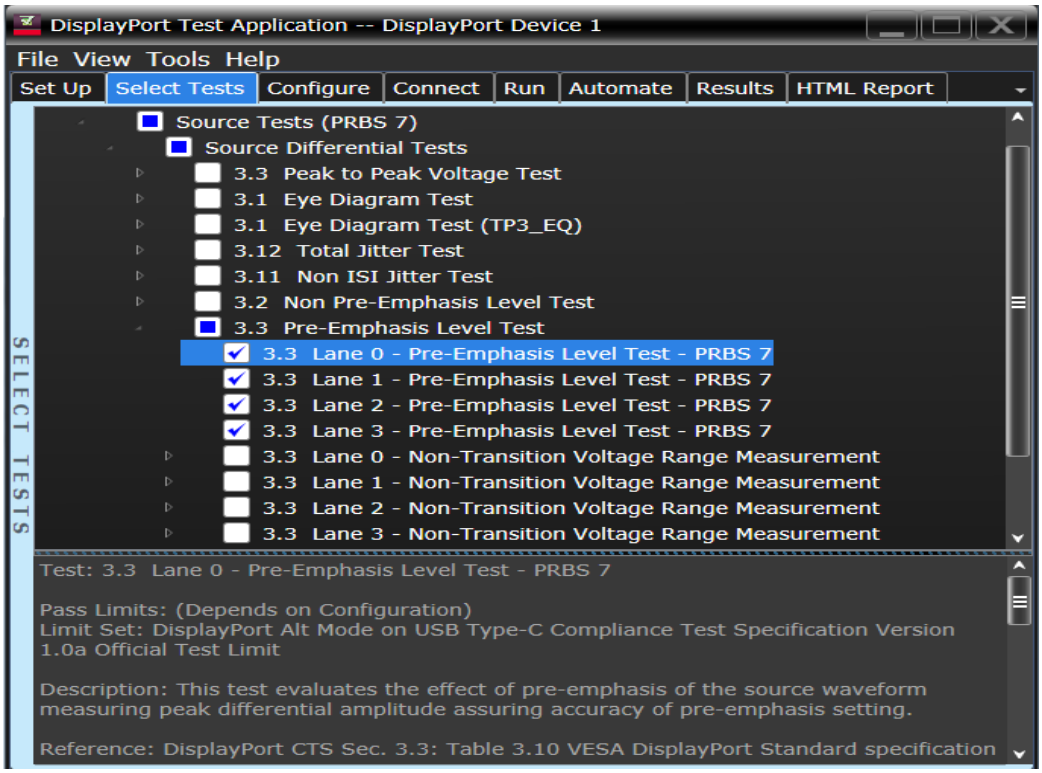
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings.

Test Conditions for Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.4 Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR3– PLTPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given Voltage Level and a Pre-Emphasis Level X:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.

- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6th bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4th bit of the four successive transmitted zeros of the pattern.

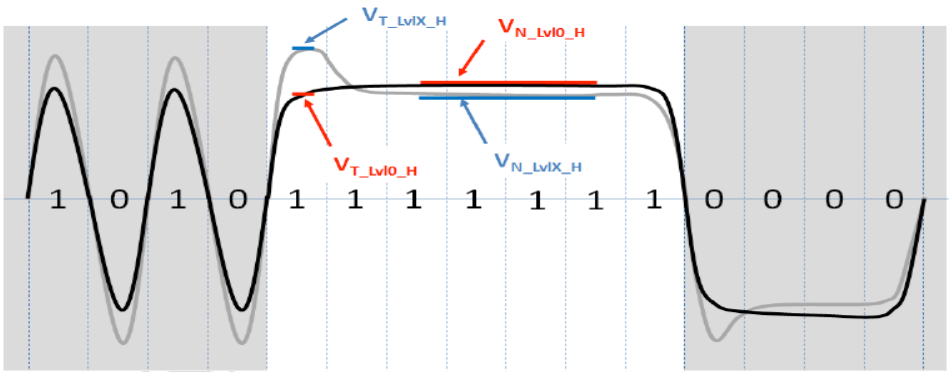


Figure 167 High Voltage measurement for RBR and HBR

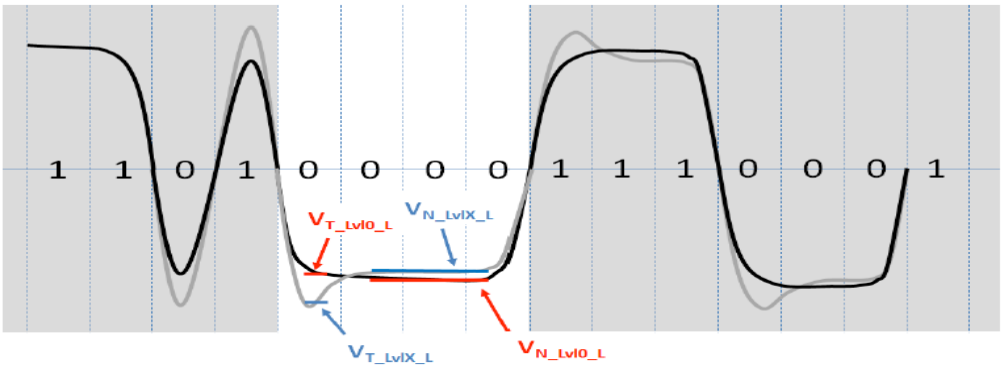


Figure 168 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR3 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

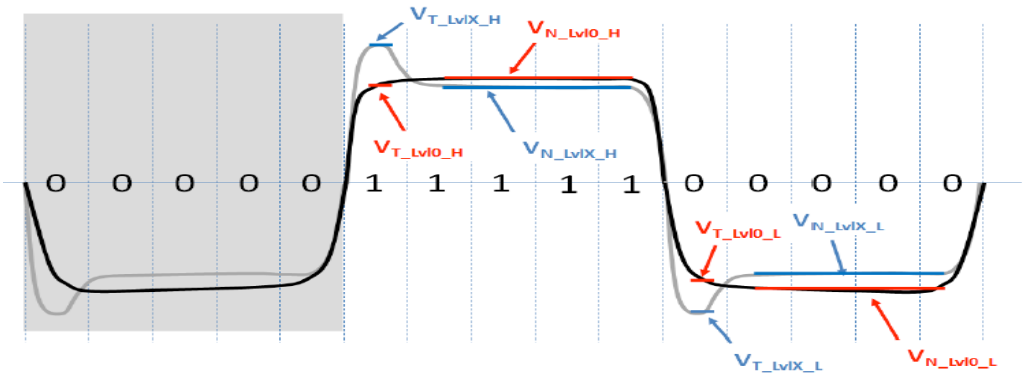


Figure 169 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

l Calculate the pre-emphasis level using the equation:

$$\text{Pre-Emphasis}_{LvlX} = 20 * \text{Log}_{10}[V_{T\_LvlX\_PP} / V_{N\_LvlX\_PP}]$$

2 For Pre-Emphasis Level 0 (no pre-emphasis level), the result for $\text{Pre-Emphasis}_{Lvl0}$ is compared with the maximum pre-emphasis disabled limit.

3 Repeat Step 1 for the next Pre-Emphasis level and for each Pre-Emphasis levels, compare the pre-emphasis delta with the pre-emphasis delta limits.

4 Calculate the pre-emphasis delta using the equation:

$$\text{Pre-Emphasis Delta (Level 1 vs Level 0)} = \text{Pre-Emphasis}_{Lvl1} - \text{Pre-Emphasis}_{Lvl0}$$

$$\text{Pre-Emphasis Delta (Level 2 vs Level 1)} = \text{Pre-Emphasis}_{Lvl2} - \text{Pre-Emphasis}_{Lvl1}$$

$$\text{Pre-Emphasis Delta (Level 3 vs Level 2)} = \text{Pre-Emphasis}_{Lvl3} - \text{Pre-Emphasis}_{Lvl2}$$

5 Report the measurement results.

PASS Condition

Pre-emphasis values for the Level 0 (OFF) state (Normative)

Level 0 (OFF) Pre-emphasis measurement:

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl0\_PP} / \text{Voltage}_{N\_Lvl0\_PP}]$ for all supported levels.

Level 0 (OFF) Pre-emphasis Measurement condition: +0.25 dB $\geq$ Resultant

Pre-emphasis Delta values for:

a Level 1 vs. Level 0 Pre-emphasis settings (NORMATIVE)

b Level 2 vs. Level 1 Pre-emphasis settings (NORMATIVE)

c Level 3 vs. Level 2 Pre-emphasis settings (NORMATIVE)

Pre-emphasis Delta measurements:

- Level 1 vs. Level 0

Resultant = 20 * Log [$Voltage_{T\_Lvl1\_PP}$ / $Voltage_{N\_Lvl1\_PP}$] - 20 * Log [$Voltage_{T\_Lvl0\_PP}$ / $Voltage_{N\_Lvl0\_PP}$] for Voltage Swing Levels 0, 1 and 2.

- Level 2 vs. Level 1

Resultant = 20 * Log [$Voltage_{T\_Lvl2\_PP}$ / $Voltage_{N\_Lvl2\_PP}$] - 20 * Log [$Voltage_{T\_Lvl1\_PP}$ / $Voltage_{N\_Lvl1\_PP}$] for Voltage Swing Levels 0 and 1.

- Level 3 vs. Level 2

Resultant = 20 * Log [$Voltage_{T\_Lvl3\_PP}$ / $Voltage_{N\_Lvl3\_PP}$] - 20 * Log [$Voltage_{T\_Lvl2\_PP}$ / $Voltage_{N\_Lvl2\_PP}$] for Voltage Swing Level 0, if supported.

Table 185 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX-PREEMP-OFF}$	Maximum Pre-emphasis when disabled	-	-	0.25	dB	Pre-emphasis Level 0 setting must not show any pre-emphasis at TP2 to prevent link training issues.
$V_{TX-PREEMP-DELTA}$	Delta of Pre-emphasis Level 1 vs. Level 0	2	-	-	dB	Applies to all valid voltage settings. Measured at Pre-emphasis Post Cursor2 Level 0. Support for Pre-emphasis Level 3 is optional.
	Delta of Pre-emphasis Level 2 vs. Level 1	1.6	-	-	dB	
	Delta of Pre-emphasis Level 3 vs. Level 2	1.6	-	-	dB	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-18*

Expected/Observable Results

The measured pre-emphasis level or pre-emphasis delta for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Transition Voltage Range Measurement Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1272001, 1272002, 1272003, 1272004 – Non Transition Voltage Range Measurement (Swing 0)
- 1273001, 1273002, 1273003, 1273004 – Non Transition Voltage Range Measurement (Swing 1)
- 1274001, 1274002, 1274003, 1274004 – Non Transition Voltage Range Measurement (Swing 2)

For Standard DP Pattern (HBR2 and HBR3):

- 1272101, 1272102, 1272103, 1272104 – Non Transition Voltage Range Measurement (Swing 0)
- 1273101, 1273102, 1273103, 1273104 – Non Transition Voltage Range Measurement (Swing 1)
- 1274101, 1274102, 1274103, 1274104 – Non Transition Voltage Range Measurement (Swing 2)

For Arbitrary Pattern:

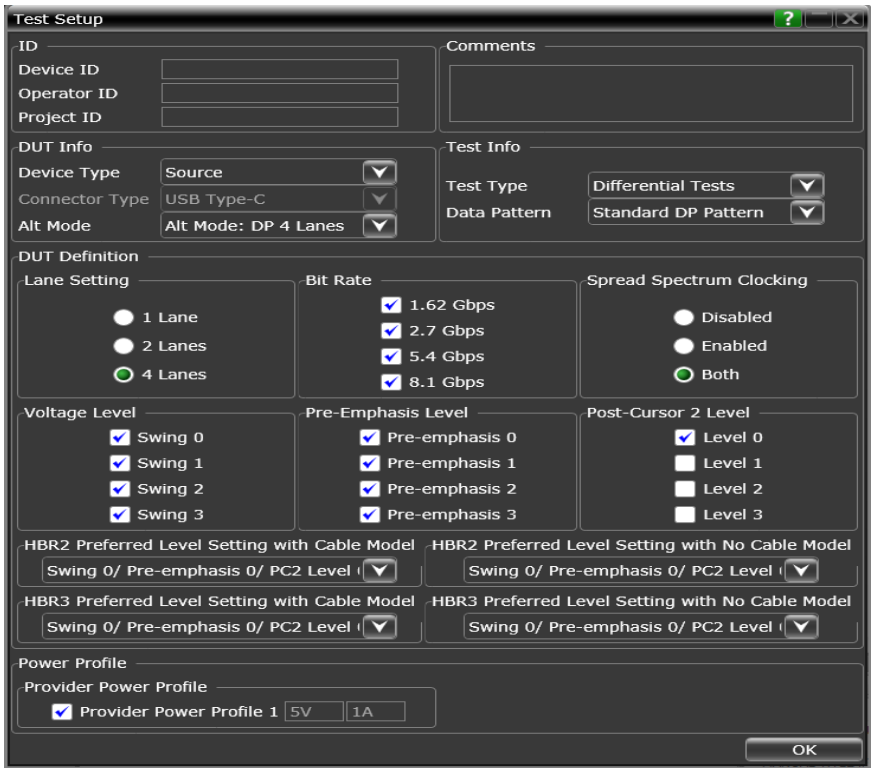
- 1372101, 1372102, 1372103, 1372104 – Non Transition Voltage Range Measurement (Swing 0)
- 1373101, 1373102, 1373103, 1373104 – Non Transition Voltage Range Measurement (Swing 1)
- 1374101, 1374102, 1374103, 1374104 – Non Transition Voltage Range Measurement (Swing 2)

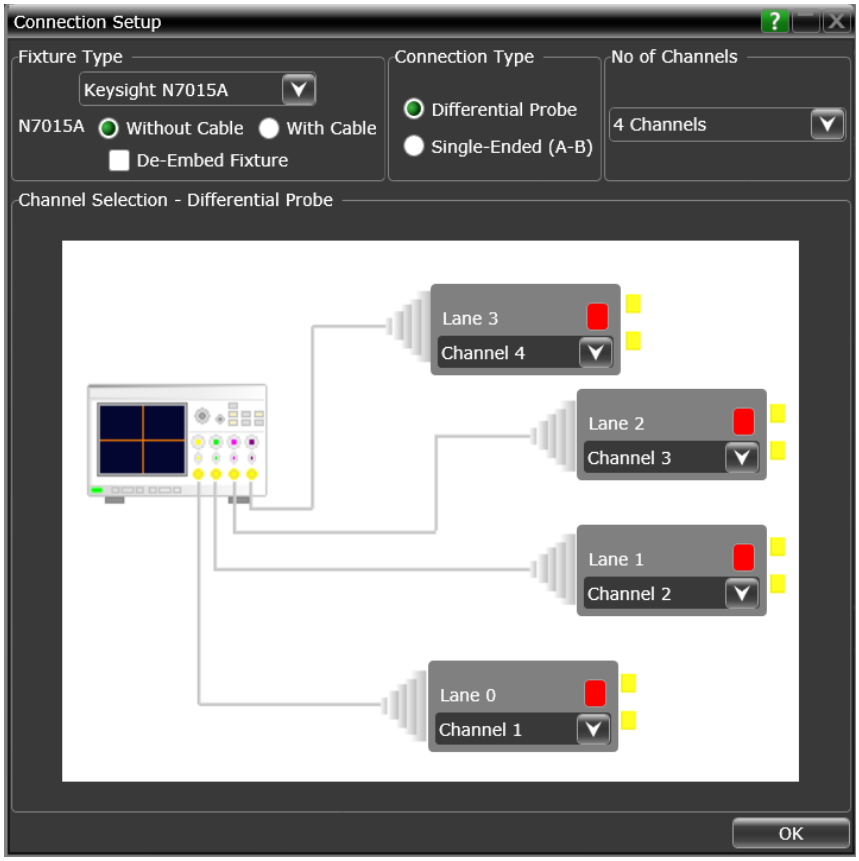
Test Overview

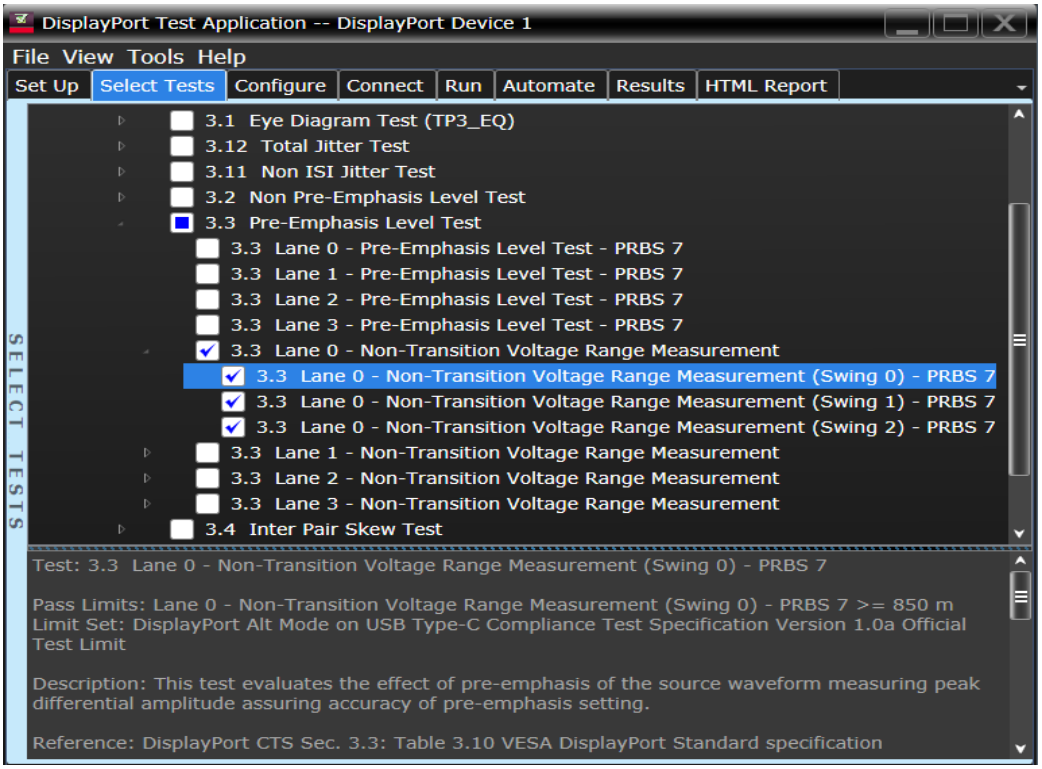
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings. Comparisons are also made for the Level 0 transition state as well as non-transition levels.

Test Conditions for Non-Transition Voltage Range Measurement Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.4 Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR3 – PLTPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given Voltage Level, repeat the following steps for all pre-emphasis levels subjected to constraints specified in Table 3-1 of the VESA DisplayPort 1.4 Standard:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.

- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6th bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4th bit of the four successive transmitted zeros of the pattern.

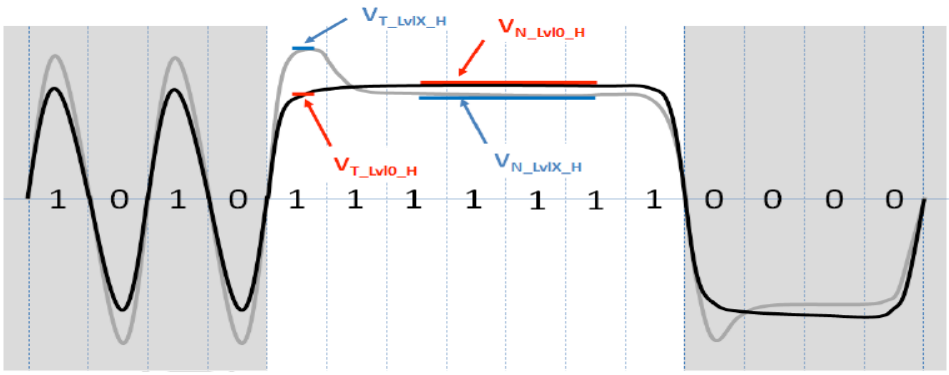


Figure 170 High Voltage measurement for RBR and HBR

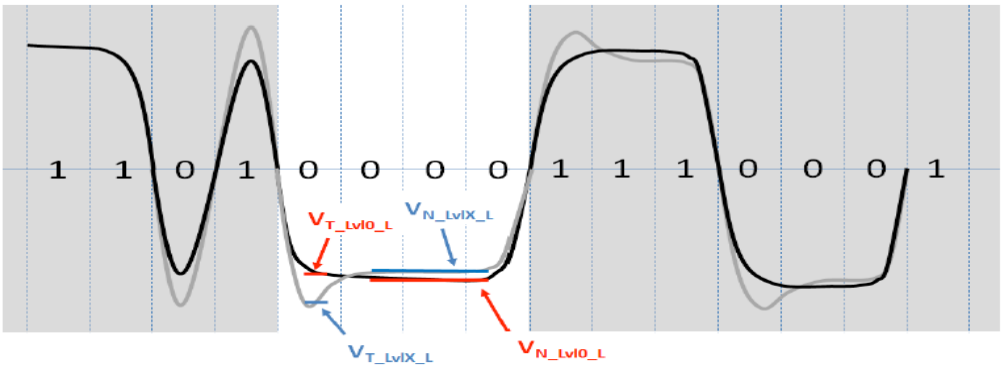


Figure 171 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR3 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

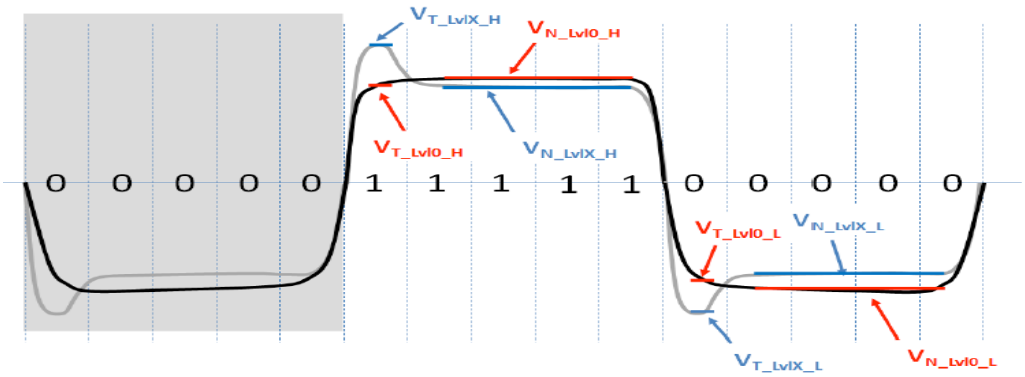


Figure 172 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

2 Calculate the non transition voltage range using the equation:

$$\text{Non Transition Voltage Range} = \text{Minimum } [(V_{N\_LvlX\_PP}) / (V_{N\_Lvl0\_PP})]$$

where, $V_{N\_LvlX\_PP}$) refers to all supported pre-emphasis levels (Level1, Level2, Level3 and so on up to Level X).

3 Report the measurement results.

PASS Condition

Non-Transition Voltage Range Measurements

For Level 2 voltage setting: Resultant > 0.708 OR 20*log(Resultant) > -3dB

For Level 1 voltage setting: Resultant > 0.708 OR 20*log(Resultant) > -3dB

For Level 0 voltage setting: Resultant > 0.85 OR 20*log(Resultant) > -1.4dB

Table 186 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX-DIFF\_REDUCTION}$	Non-transition reduction Output Voltage Level 2	-	-	3	dB	$V_{TX-DIFF}$ at each non-zero nominal pre-emphasis level must not be lower than the specified amount less than $V_{TX-DIFF}$ at the zero nominal pre-emphasis level.
	Non-transition reduction Output Voltage Level 1	-	-	3	dB	
	Non-transition reduction Output Voltage Level 0	-	-	1.4	dB	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-18*

Expected/Observable Results

The measured output voltage level reduction of the non transition bit for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Peak to Peak Voltage Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1266001, 1266002, 1266003, 1266004 – Peak to Peak Voltage Test

For Standard DP Pattern (HBR2 and HBR3):

- 1266101, 1266102, 1266103, 1266104 – Peak to Peak Voltage Test

For Arbitrary Pattern:

- 1366101, 1366102, 1366103, 1366104 – Peak to Peak Voltage Test

Test Overview

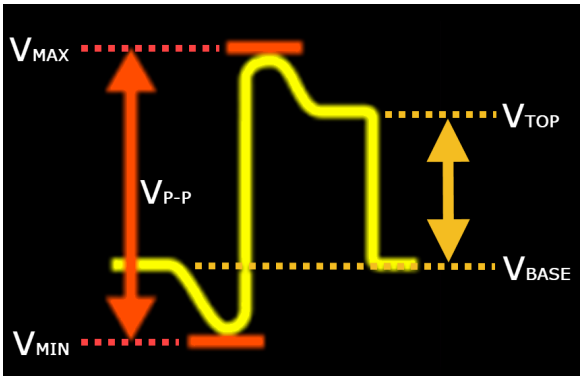
The objective of this test is to evaluate the maximum differential peak to peak voltage.

NOTE

The peak to peak voltage (V_{P-P}) formula is:

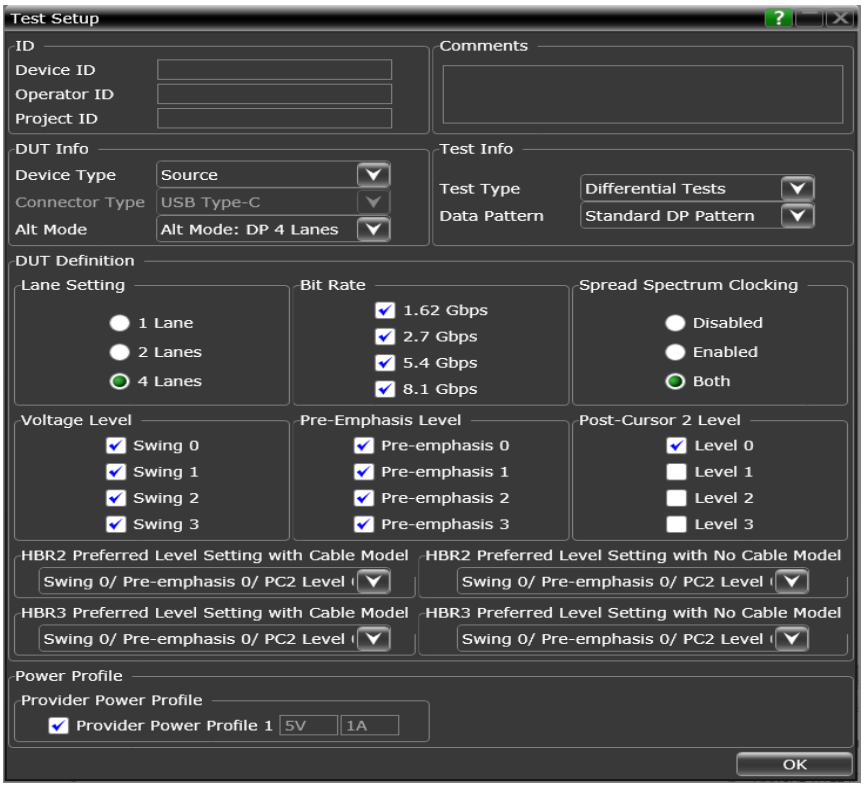
$$V_{P-P} = V_{MAX} - V_{MIN}$$

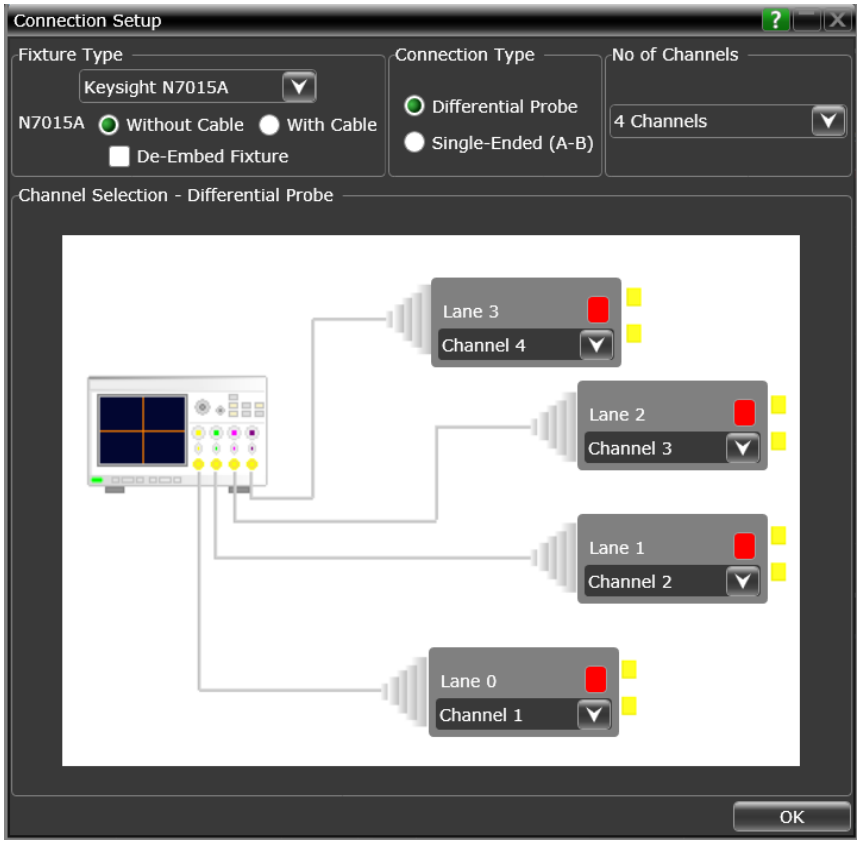
Please see the figure below for more info.

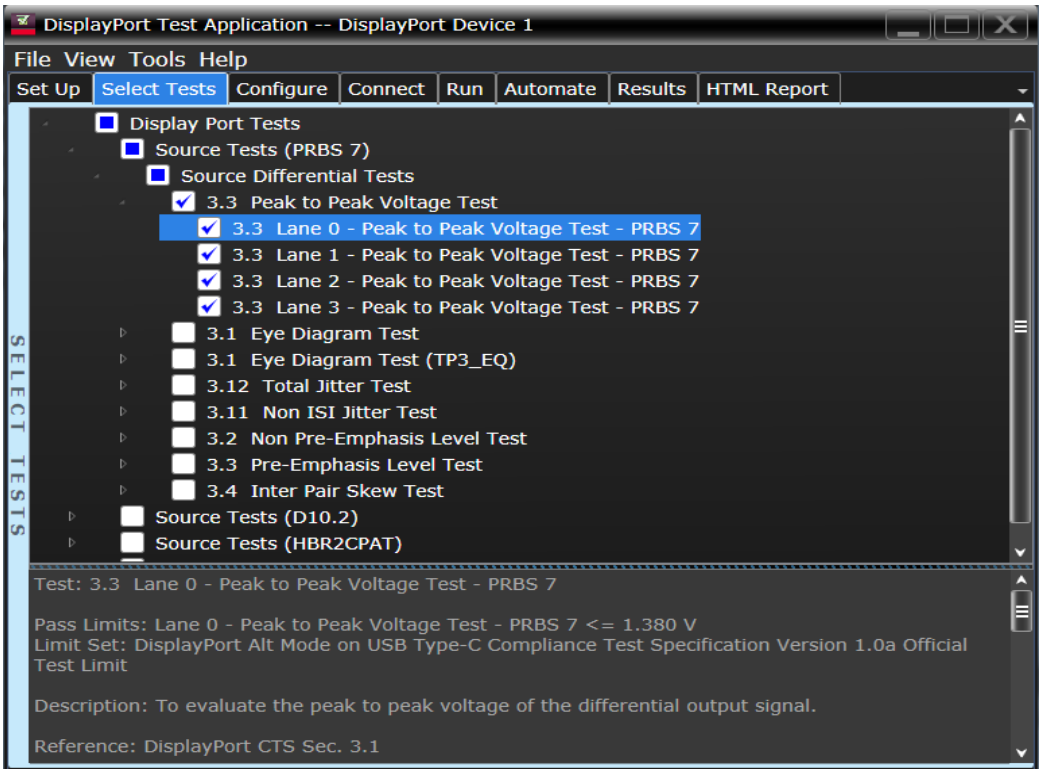


Test Conditions for Peak to Peak Voltage Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.4 Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR3 – PLTPAT




Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Display Port Tests
Source Tests (PRBS 7)
Source Differential Tests
3.3 Peak to Peak Voltage Test
3.3 Lane 0 - Peak to Peak Voltage Test - PRBS 7
3.3 Lane 1 - Peak to Peak Voltage Test - PRBS 7
3.3 Lane 2 - Peak to Peak Voltage Test - PRBS 7
3.3 Lane 3 - Peak to Peak Voltage Test - PRBS 7
3.1 Eye Diagram Test
3.1 Eye Diagram Test (TP3_EQ)
3.12 Total Jitter Test
3.11 Non ISI Jitter Test
3.2 Non Pre-Emphasis Level Test
3.3 Pre-Emphasis Level Test
3.4 Inter Pair Skew Test
Source Tests (D10.2)
Source Tests (HBR2CPAT)
Test: 3.3 Lane 0 - Peak to Peak Voltage Test - PRBS 7
Pass Limits: Lane 0 - Peak to Peak Voltage Test - PRBS 7 <= 1.380 V
Limit Set: DisplayPort Alt Mode on USB Type-C Compliance Test Specification Version 1.0a Official Test Limit
Description: To evaluate the peak to peak voltage of the differential output signal.
Reference: DisplayPort CTS Sec. 3.1

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{MAX} and V_{MIN} of the input signal.
   d Measure the data rate of the input signal.
3 Measure the maximum and minimum voltage of the input signal.
4 Calculate the peak to peak voltage using the equation:

$$\text{Peak to Peak Voltage} = V_{MAX} - V_{MIN}$$

5 Report the measurement results.

PASS Condition

For all Data Rates:

Maximum Differential Peak to Peak Voltage $\leq$ 1.38V.

Table 187 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}DIFFp\text{-}p\_MAX}$	Max Output Voltage Level	-	-	1.38	V	For all Output Level and Pre-emphasis combinations.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-18*

Expected/Observable Results

The measured peak to peak voltage for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Inter-Pair Skew Test

Test ID

For Standard DP Pattern:

- 1290001 – Lane0/Lane1 Inter-Pair Skew Test
- 1290002 – Lane0/Lane2 Inter-Pair Skew Test
- 1290003 – Lane0/Lane3 Inter-Pair Skew Test
- 1290004 – Lane1/Lane2 Inter-Pair Skew Test
- 1290005 – Lane1/Lane3 Inter-Pair Skew Test
- 1290006 – Lane2/Lane3 Inter-Pair Skew Test

For Arbitrary Pattern:

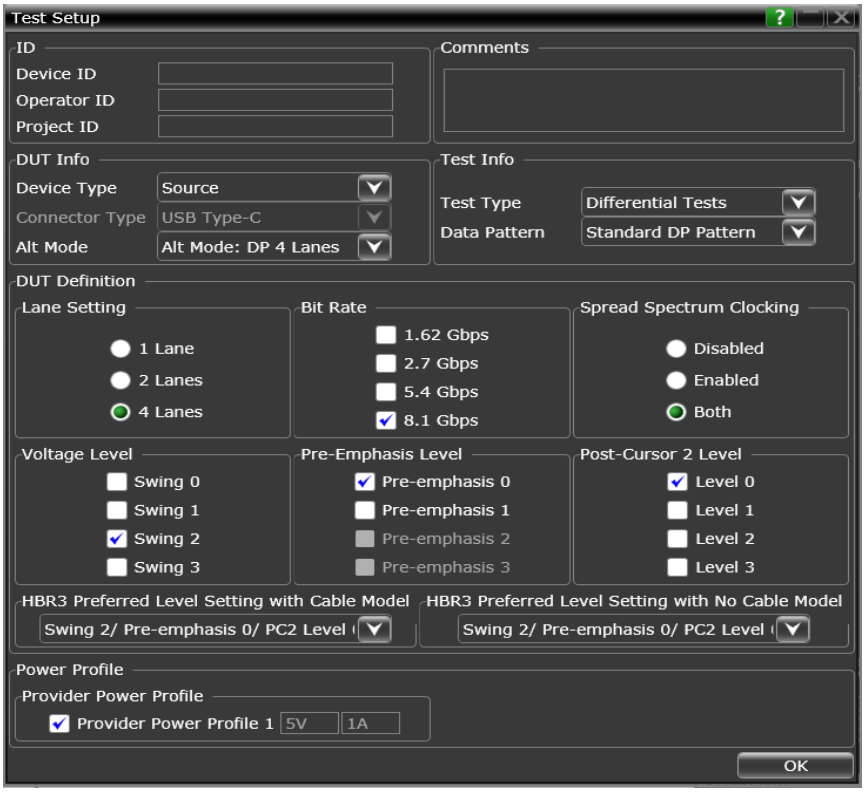
- Not applicable for arbitrary pattern

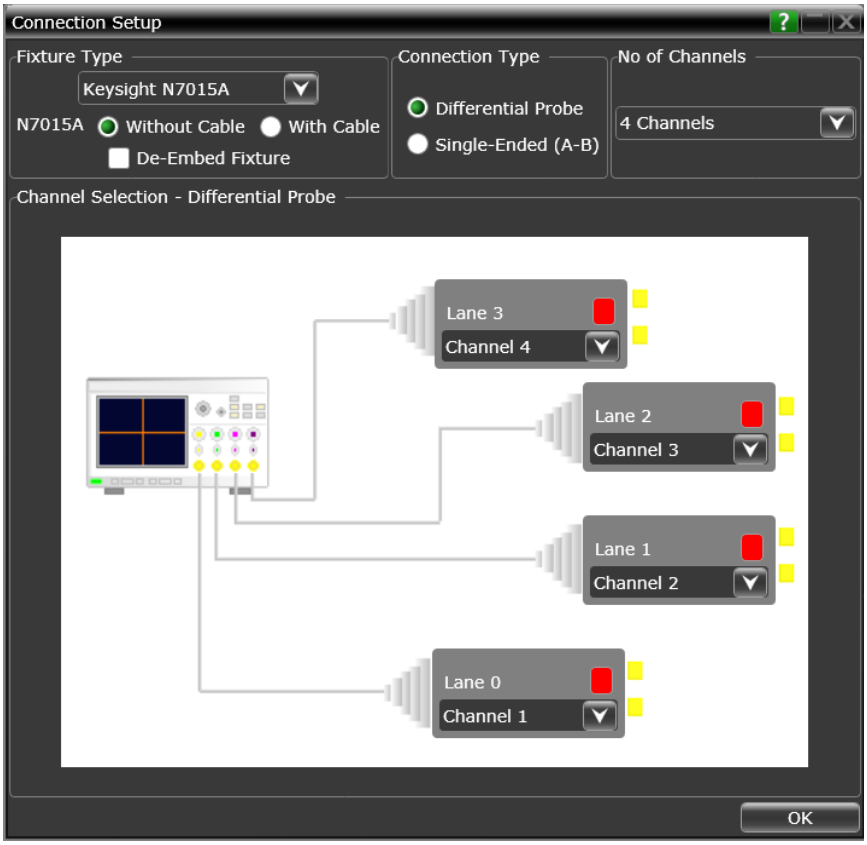
Test Overview

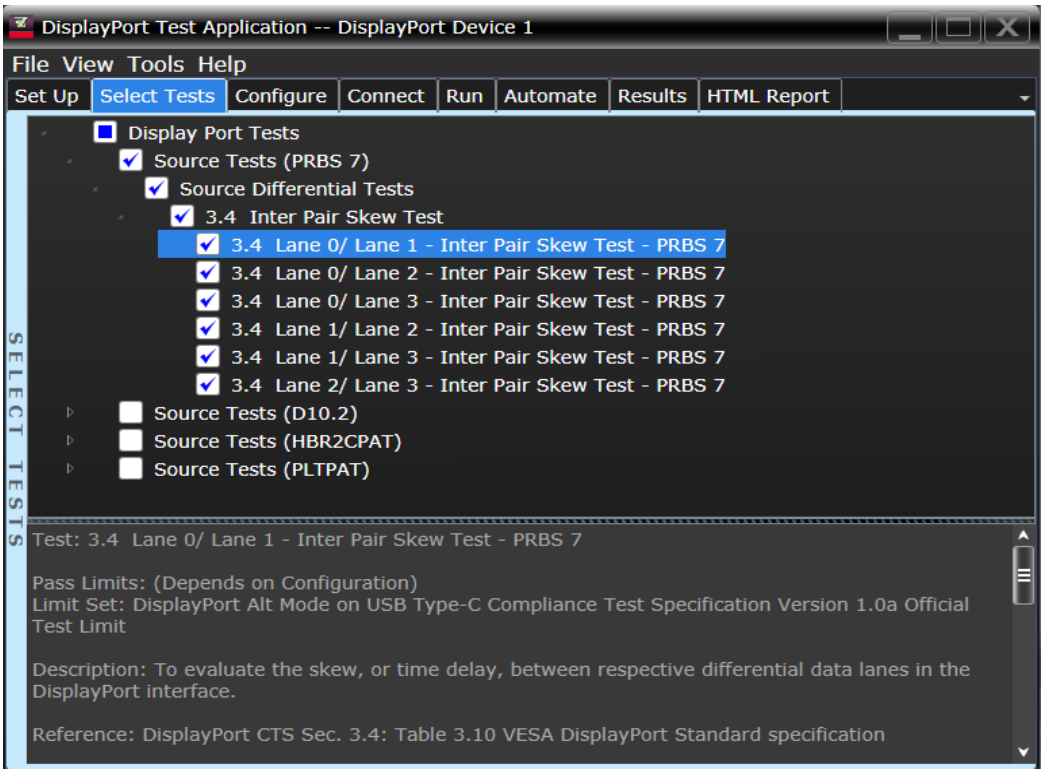
The objective of the test is to evaluate the skew or time delay between differential data lanes in the DisplayPort interface.

Test Conditions for Inter Pair Skew Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest Bit Rate supported (RBR, HBR, HBR2 or HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported For two lane operation: Lane 0 to Lane 1 For four lane operation: Lane 0 to Lane 1 Lane 0 to Lane 2 Lane 0 to Lane 3 Lane 1 to Lane 2 Lane 1 to Lane 3 Lane 2 to Lane 3
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Display Port Tests
Source Tests (PRBS 7)
Source Differential Tests
3.4 Inter Pair Skew Test
3.4 Lane 0/ Lane 1 - Inter Pair Skew Test - PRBS 7
3.4 Lane 0/ Lane 2 - Inter Pair Skew Test - PRBS 7
3.4 Lane 0/ Lane 3 - Inter Pair Skew Test - PRBS 7
3.4 Lane 1/ Lane 2 - Inter Pair Skew Test - PRBS 7
3.4 Lane 1/ Lane 3 - Inter Pair Skew Test - PRBS 7
3.4 Lane 2/ Lane 3 - Inter Pair Skew Test - PRBS 7
Source Tests (D10.2)
Source Tests (HBR2CPAT)
Source Tests (PLTPAT)
Test: 3.4 Lane 0/ Lane 1 - Inter Pair Skew Test - PRBS 7
Pass Limits: (Depends on Configuration)
Limit Set: DisplayPort Alt Mode on USB Type-C Compliance Test Specification Version 1.0a Official Test Limit
Description: To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
Reference: DisplayPort CTS Sec. 3.4: Table 3.10 VESA DisplayPort Standard specification

Measurement Procedure

1 For a given inter-pair skew measurement of Lane A to Lane B:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the Lane A input signal.

ii Scale the vertical display of the Lane A input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the Lane A input signal.

iv Verify the trigger and the amplitude of the Lane B input signal.

v Scale the vertical display of the Lane B input signal to optimum value.

vi Measure V_{TOP} and V_{BASE} of the Lane B input signal.

vii Measure the data rate of the Lane A input signal.

viii Measure the data rate of the Lane B input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

d Set up the parameter for the inter-pair skew measurement:

i Set up two display grids such that each grid displays one test lane data signal.

ii Set up the measurement threshold for each test lane data signal on the Transition Voltage = 0V.

iii Decode the data signal for each test lane.

iv Search the desired pattern from the decoded data signal.

v Measure the time difference between the corresponding edges of both test lanes:

$$T_{Transition\_LaneA} - T_{Transition\_LaneB}$$

vi Repeat the previous step until you measure 100 edges.

vii VESA DisplayPort 1.4 Standard specifies 20 UI offset Lane 0 to Lane 1, Lane 1 to Lane 2 and Lane 2 to Lane 3. The resultant offset is cumulative.

viii Calculate the inter-pair skew using the equation:

$$\text{Inter-Pair Skew} = \{1/\text{Number of Edges}\} \sum |T_{Transition\_LaneA} - T_{Transition\_LaneB}| - \text{Nominal Skew}$$

where, Nominal Skew is the expected offset between tested lanes.

2 Report the measurement results.

PASS Condition

-1250ps < Inter-Lane Skew Tolerance < 1250ps

Table 188 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$t_{TX-SKEW-INTER\_PAIR}$	Lane-to-Lane Output Skew	-	-	1250	ps	Applies to transmitters capable of 2- and 4-lane operation. Also, applies to all pairwise combinations of supported lanes for all data rates.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.4*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-18*

Expected/Observable Results

The measured inter-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Main Link Frequency Compliance Test

Test ID

For Standard DP Pattern:

- 12193001 12193002 12193003 12193004 – Main Link Frequency Compliance

For Arbitrary Pattern:

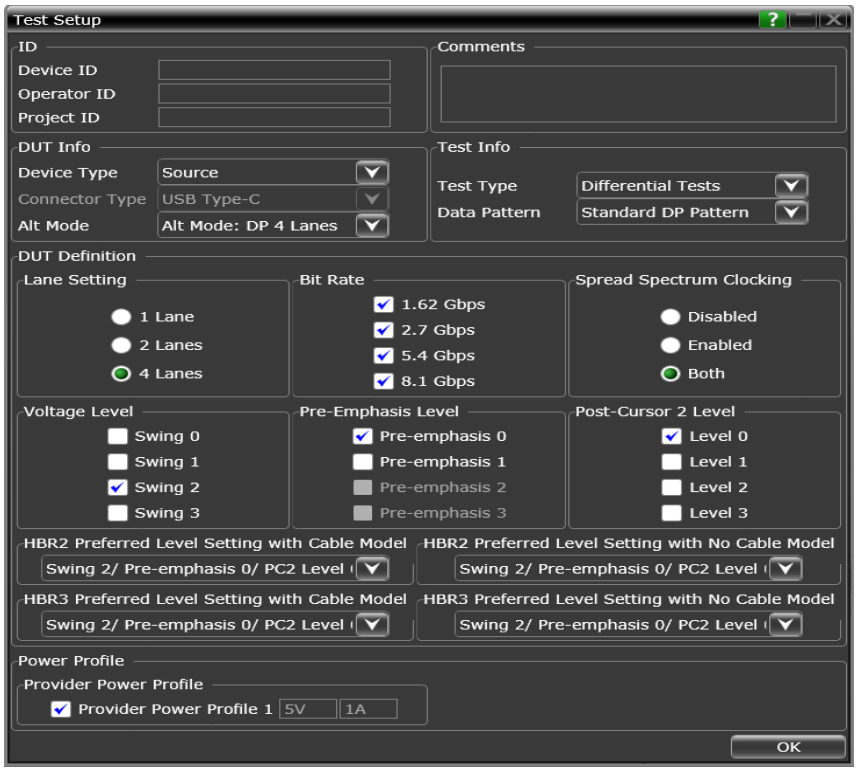
- 13193001 13193002 13193003 13193004 – Main Link Frequency Compliance

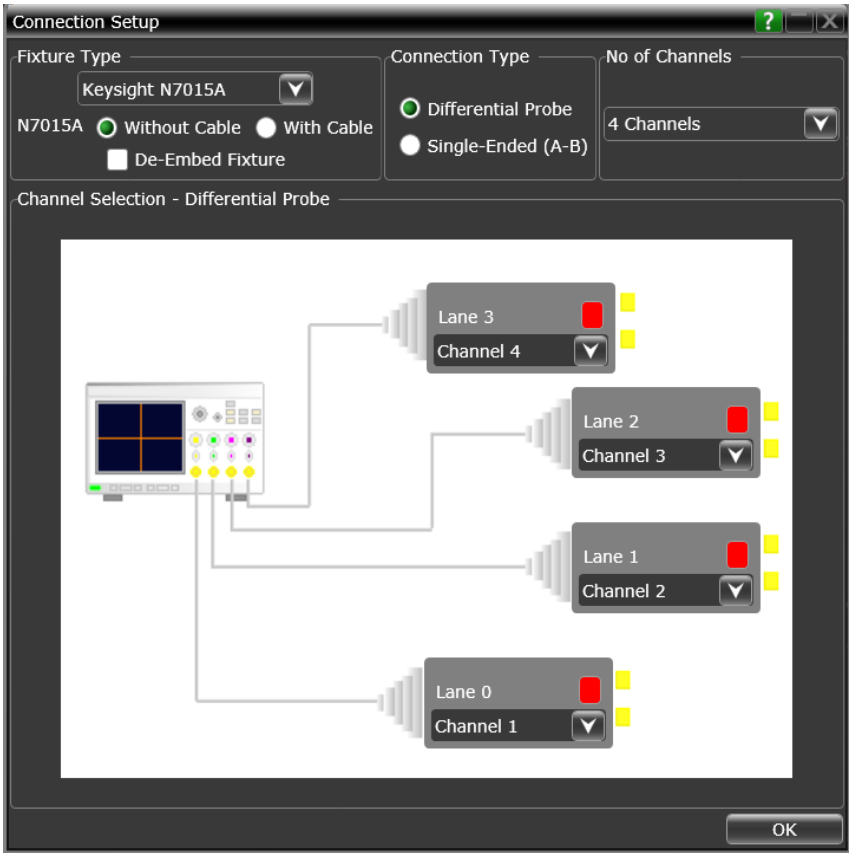
Test Overview

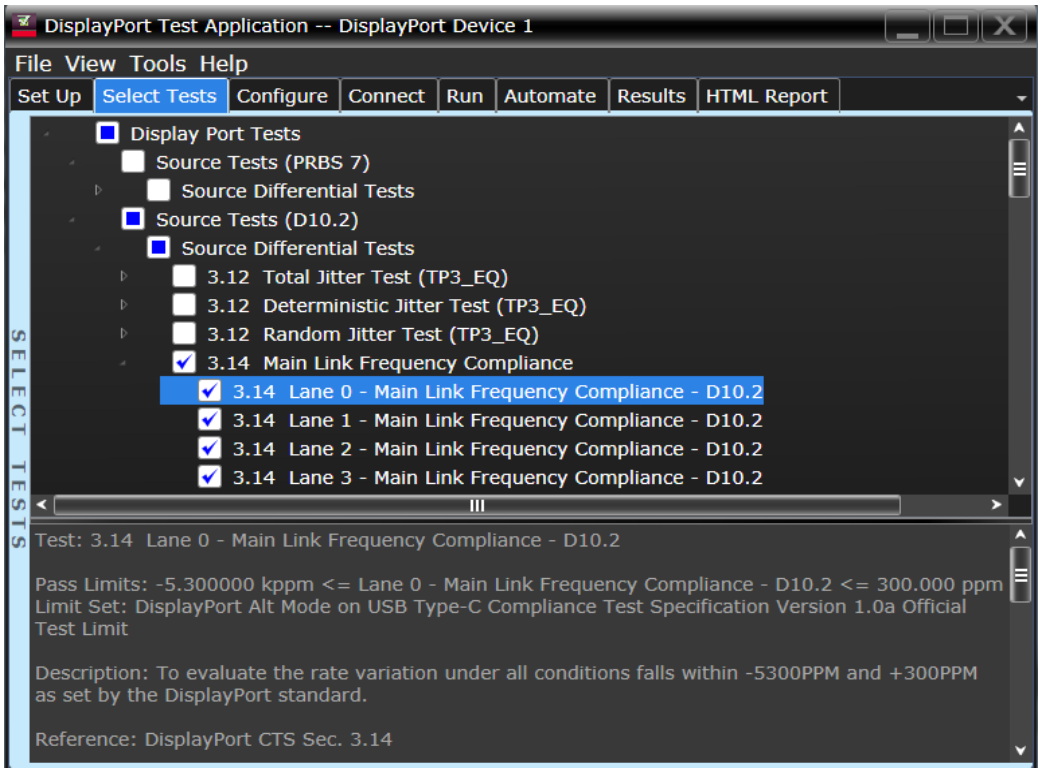
The objective of this test is to ensure that the average data rate under all conditions does not exceed the minimum and maximum values as set by the VESA DisplayPort 1.4 Standard.

Test Conditions for Main Link Frequency Compliance Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.

5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and the minimum measurement levels for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurement levels for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e For SSC Enabled Test condition, check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.
9 For the test condition “SSC Enabled”, set up the parameter of the SSC measurement:
   a Set up the memory depth and time-base to display one complete SSC cycle based on the measured SSC modulation frequency in Step 5.
   b Acquire the signal with one complete SSC cycle.
   c Get the minimum of FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

      Maximum Data Rate = 1 / (Minimum Unit Interval)

   d Get the maximum of FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

      Minimum Data Rate = 1 / (Maximum Unit Interval)

   e Repeat steps b, c and d until you acquire 10 SSC Cycles.
   f Calculate the mean value for the maximum and minimum data rates.
10 Report the measurement results.

PASS Condition

Maximum Data Rate (Frequency Max_{ppm}) $\leq$ 300 ppm

Minimum Data Rate (Frequency Min_{ppm}) $\geq$ -5300 ppm

Table 189 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
f_{HBR3}	Frequency for High Bit Rate 3	8.05707	8.1	8.10243	Gbps	Frequency high limit = +300ppm Frequency low limit = -5300ppm
f_{HBR2}	Frequency for High Bit Rate 2	5.37138	5.4	5.40162	Gbps	
f_{HBR}	Frequency for High Bit Rate	2.68569	2.7	2.70081	Gbps	
f_{RBR}	Frequency for Reduced Bit Rate	1.611414	1.62	1.620486	Gbps	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.14*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-17*

Expected/Observable Results

The measured data rate for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Frequency Test

Test ID

For Standard DP Pattern:

- 12170001 12170002 12170003 12170004 – SSC Modulation Frequency Test

For Arbitrary Pattern:

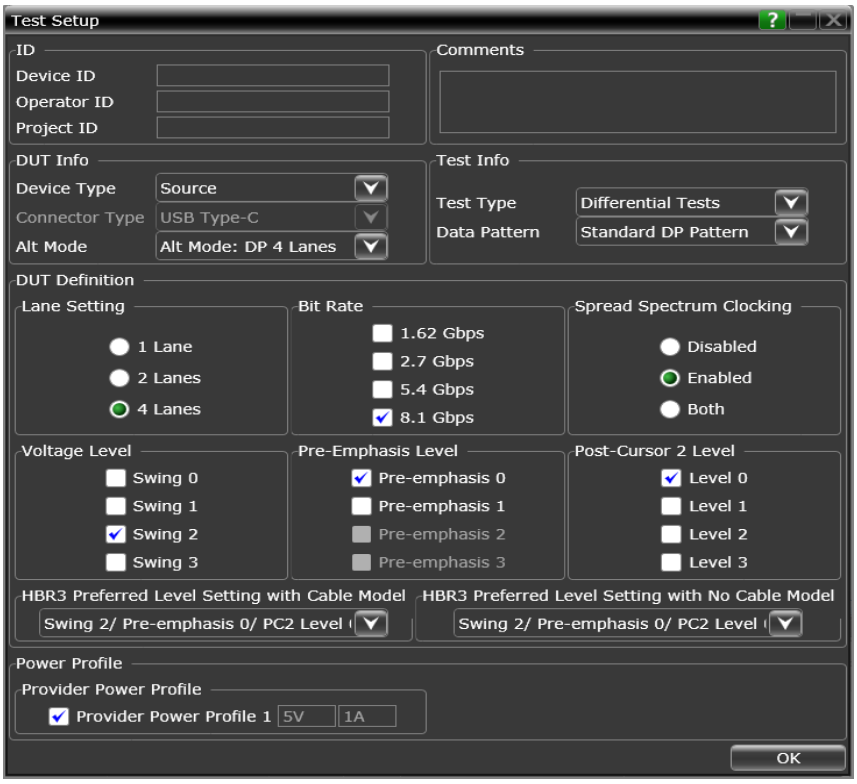
- 13170001 13170002 13170003 13170004 – SSC Modulation Frequency Test

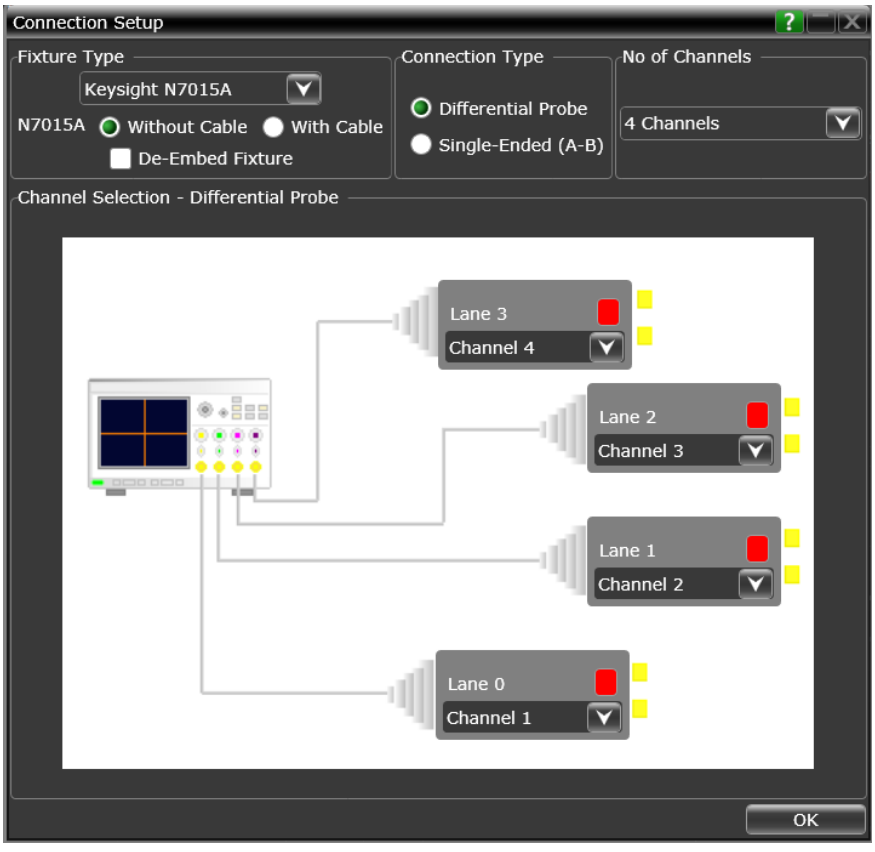
Test Overview

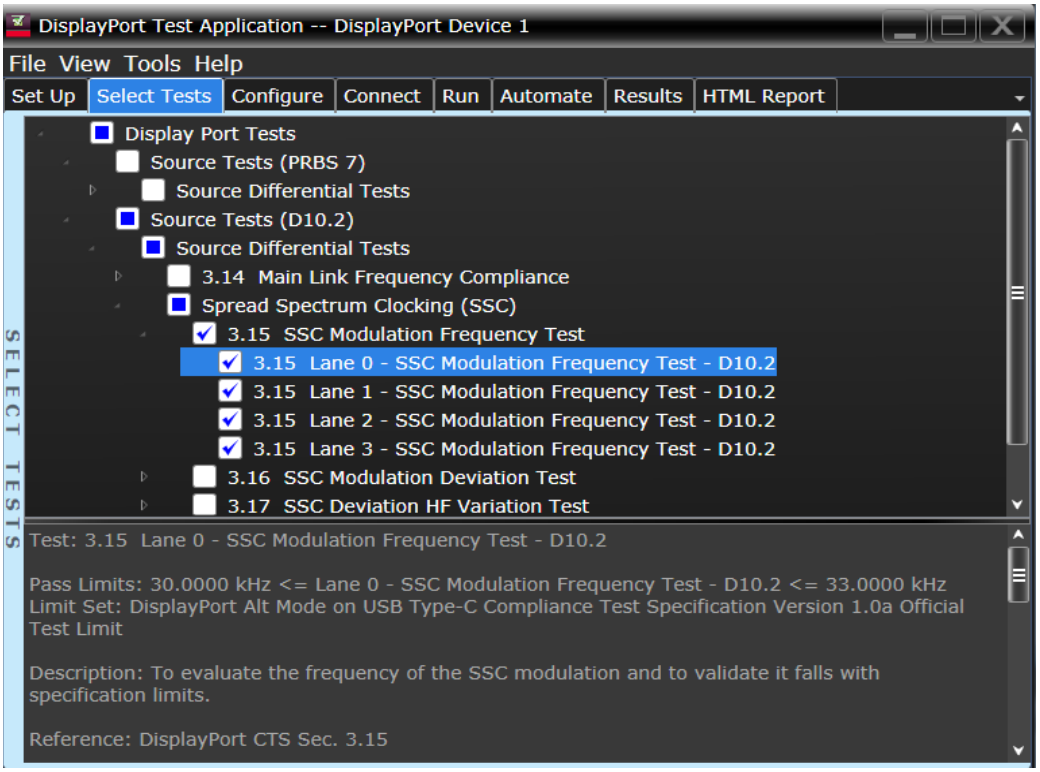
The objective of this test is to evaluate the frequency of the SSC modulation and to validate that the frequency is within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. Calculate the SSC modulation frequency from the average of the measured SSC modulation frequency for each cycle.

Test Conditions for SSC Modulation Frequency Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR3)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.

5 Set up the parameters for the frequency measurement.

a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.

b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.

c Set up the memory depth and time-base using the settings defined in the Configuration Variable.

d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.

e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).

f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.

g Acquire the signal for 10 SSC Cycles.

6 Get the mean value for the SSC Modulation frequency.

7 Report the measurement results.

PASS Condition

30kHz $\leq$ SSC Modulation Frequency (f_{SSC}) $\leq$ 33kHz

Table 190 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
Down_Spread_Frequency	Link clock down-spreading frequency	30	-	33	kHz	Range: 30kHz ~ 33kHz when down-spread enabled

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.15*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-17*

Expected/Observable Results

The measured SSC modulation frequency for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Deviation Test

Test ID

For Standard DP Pattern:

- 12180001 12180002 12180003 12180004 – SSC Modulation Deviation Test

For Arbitrary Pattern:

- 13180001 13180002 13180003 13180004 – SSC Modulation Deviation Test

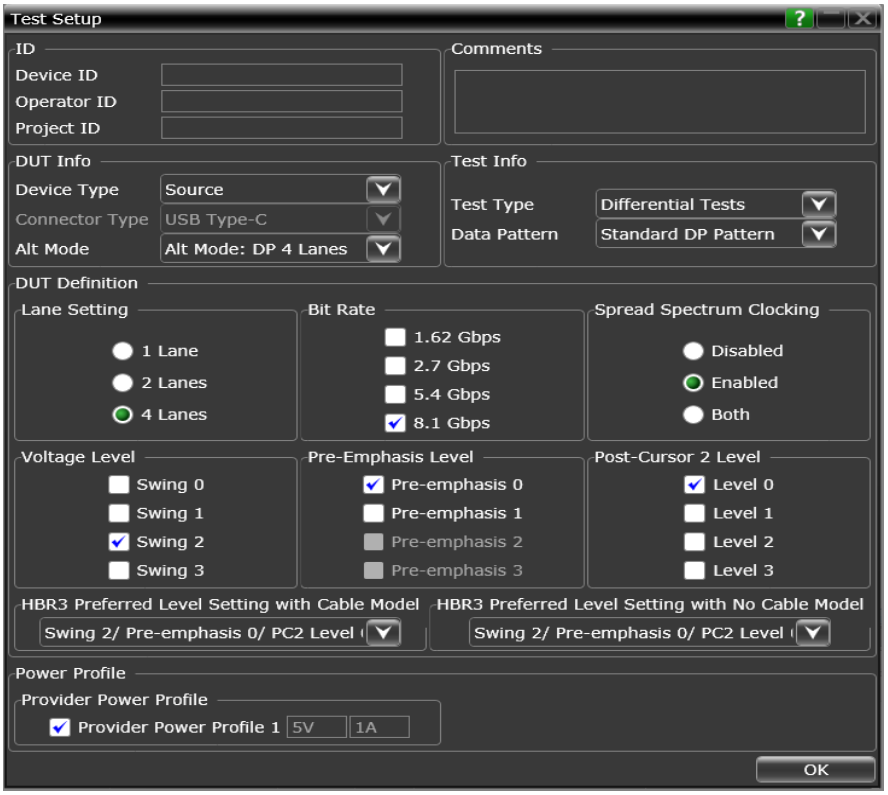
Test Overview

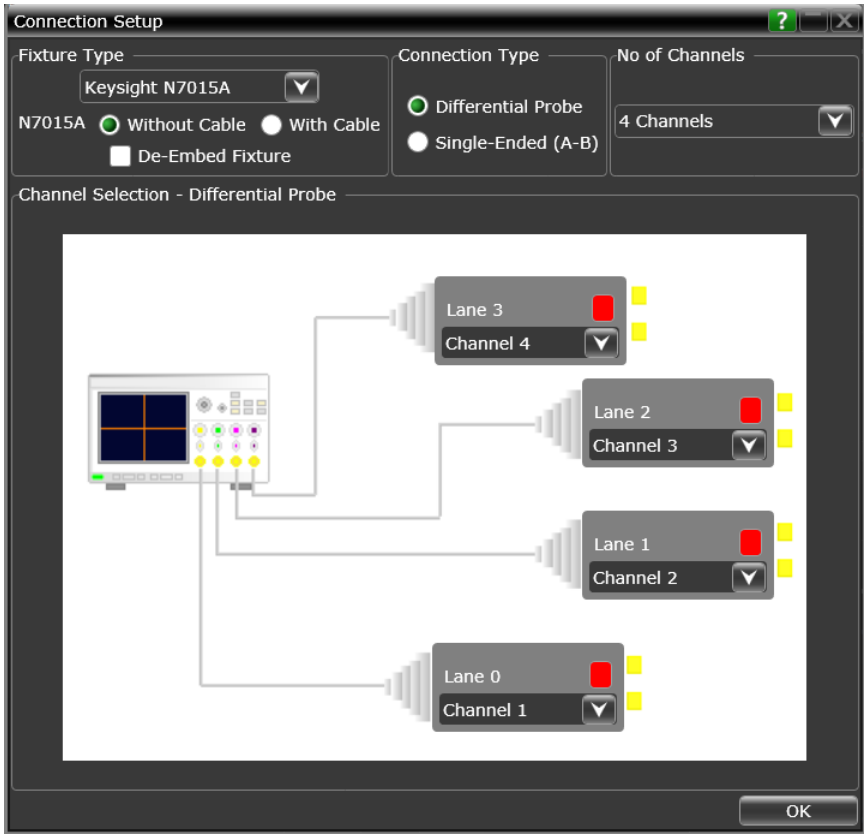
The objective of this test is to evaluate the range of SSC down-spreading of the transmitter signal in ppm and to validate that the values are within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. For each cycle, the minimum and maximum data rate is evaluated. Calculate the SSC modulation deviation from the average of the maximum minus the average of the minimum using the equation:

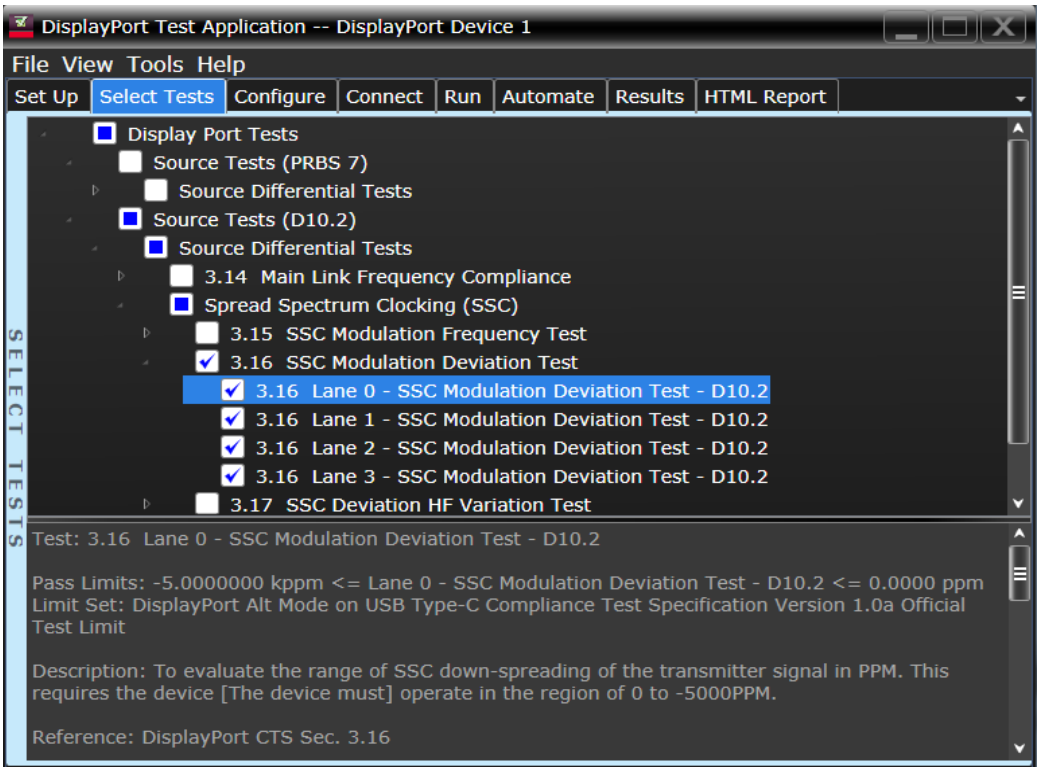
SSC Modulation Deviation = {[Average (Minimum Data Rate) - Average (Maximum Data Rate)] / Nominal Data Rate}*1E+6

Test Conditions for SSC Modulation Deviation Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR3)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.

5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and minimum measurements for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurements for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e Check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point for three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 filtered unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurements for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.
9 Set up the parameters for SSC measurement.
   a Set up memory depth and time-base to display one complete SSC Cycle based on the measured SSC modulation frequency in step 5.
   b Acquire the signal with one complete SSC Cycle.
   c Get the minimum of the FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

      Maximum Data Rate = 1/Minimum Unit Interval

   d Get the maximum of the FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

      Minimum Data Rate = 1/Maximum Unit Interval

   e Repeat step b,c and d until you acquire 10 SSC Cycles.
   f Calculate the mean value for the maximum and minimum data rate.
10 Calculate the SSC Modulation Deviation using the equation:

   SSC Modulation Deviation = {[Average (Minimum Data Rate) - Average (Maximum Data Rate)] / Nominal Data Rate}*1E+6

11 Report the measurement results.

PASS Condition

-5000ppm $\leq$ SSC Modulation Deviation (Resultant$_{SSC\ Range}$) $\leq$ 0ppm

Table 191 DisplayPort Main Link Transmitter System Parameters

Symbol	Parameter	Min	Nom	Max	Unit	Comments
Down_Spread_Amplitude	Link clock down-spreading	0	-	0.5	%	Range: 0% ~ 0.5% when down-spread enabled

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.16*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-17*

Expected/Observable Results

The measured SSC modulation deviation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Deviation HF Variation Test (Informative)

Test ID

For Standard DP Pattern:

- 12200001 12200002 12200003 12200004 – SSC Deviation HF Variation Test (Informative)

For Arbitrary Pattern:

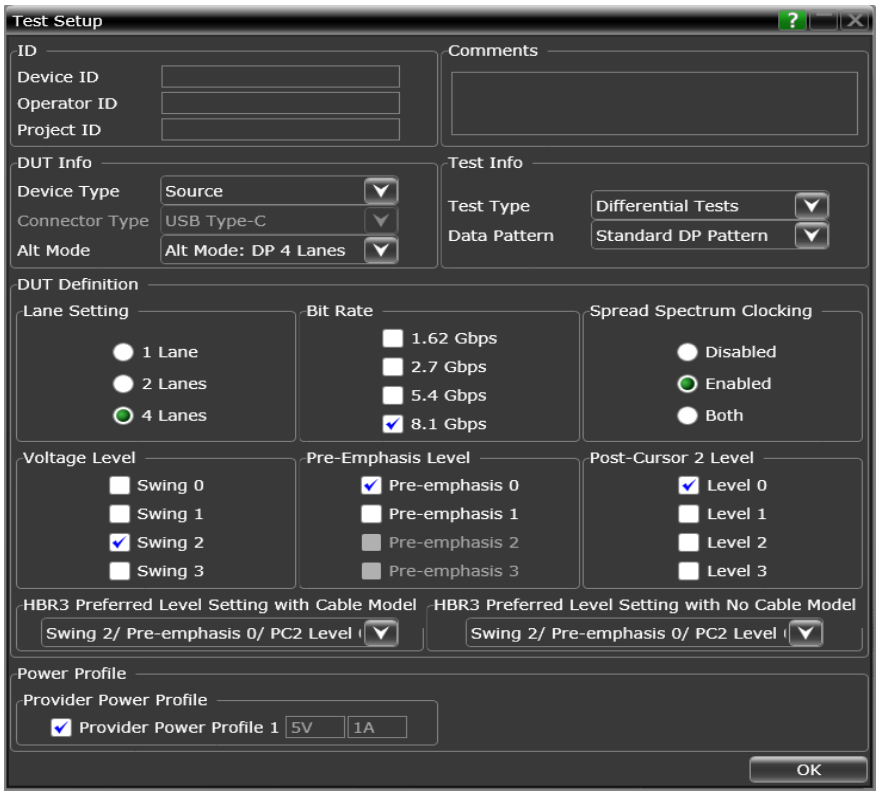
- 13200001 13200002 13200003 13200004 – SSC Deviation HF Variation Test (Informative)

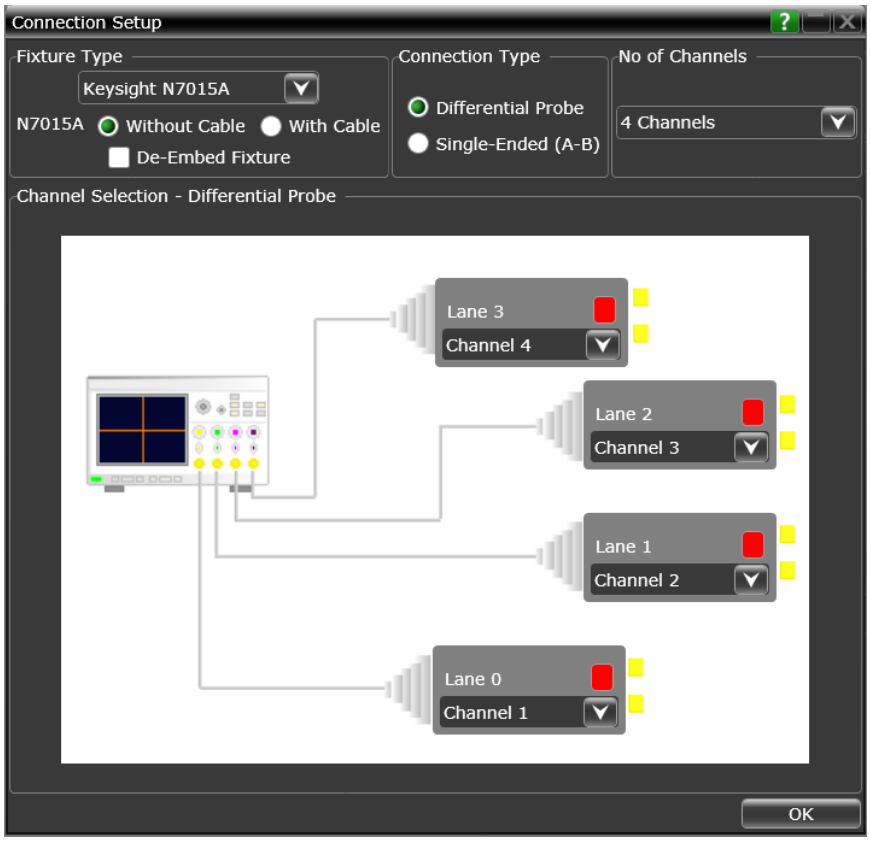
Test Overview

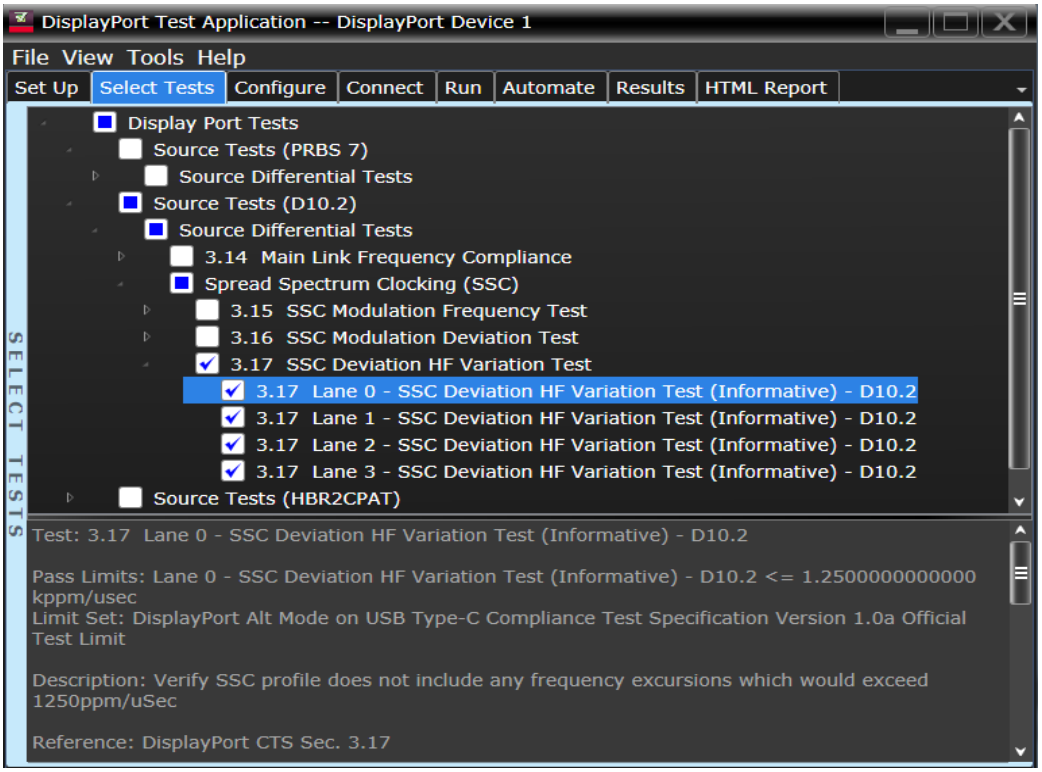
The objective of this test is to verify that the SSC profile does not include any frequency deviation that may exceed 1250 ppm/µsec. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles.

Test Conditions for SSC Deviation HF Variation Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR3)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.

5 Set up the parameters for the frequency measurement.

a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.

b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.

c Set up the memory depth and time-base using the settings defined in the Configuration Variable.

d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.

e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).

f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.

6 Set up the parameters for the SSC measurement.

a Set up memory depth and time-base to display one complete SSC cycle using the measured SSC Modulation Frequency in Step 5.

b Acquire the signal with one complete SSC Cycles.

c Read the FUNC2 filtered unit interval measurement trend.

d Compute the slope using the “Sliding Window” with 1.00 µsec window width. Calculate the slope using the equation:

$$\text{Slope} = [f(t) - f(t\text{-}1.00\ \mu\text{sec})/1.00\ \mu\text{sec}$$

e Repeat step b, c and d until you acquire 10 SSC Cycles.

f Get the maximum value for the computed value of slope.

7 Report the measurement results.

PASS Condition

SSC_t dF/dt $\leq$ 1250ppm/µsec

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.17*

Expected/Observable Results

The measured SSC deviation high frequency variation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Eye Diagram Test (TP3_EQ)

Test ID

For Standard DP Pattern (HBR):

- 1211001, 1211002, 1211003, 1211004 – Eye Diagram Test (TP3_EQ) - PRBS7
- 1211011, 1211012, 1211013, 1211014 – Eye Diagram Test with No Cable Model (TP3_EQ) - PRBS7

For Standard DP Pattern (HBR2):

- 1215001, 1215002, 1215003, 1215004 – Eye Diagram Test (TP3_EQ) - HBR2CPAT
- 1215011, 1215012, 1215013, 1215014 – Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT

For Arbitrary Pattern:

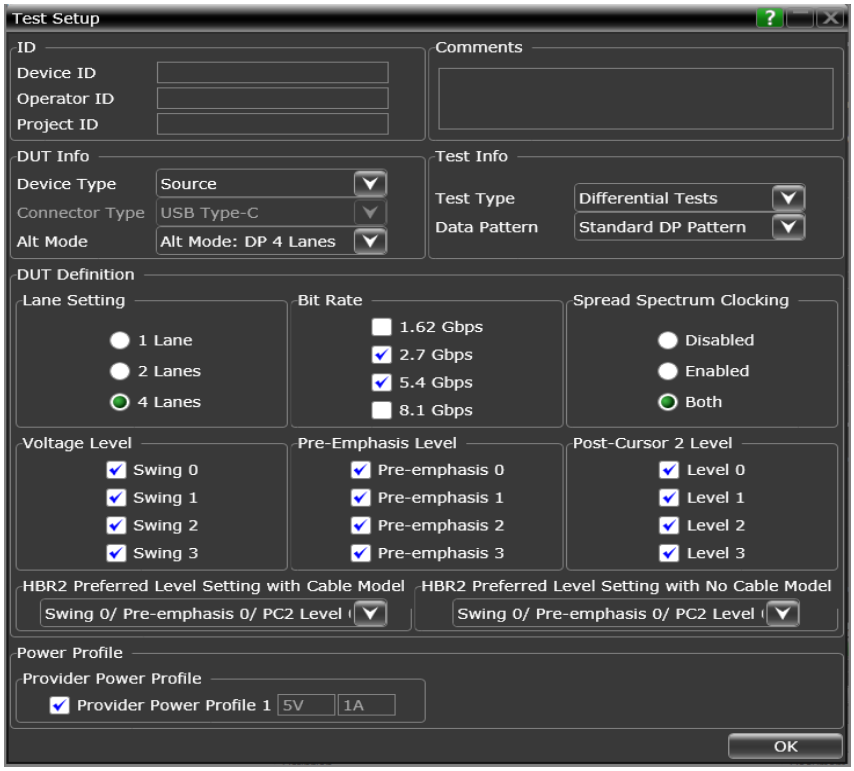
- 1315001, 1315002, 1315003, 1315004 – Eye Diagram Test (TP3_EQ)
- 1315011, 1315012, 1315013, 1315014 – Eye Diagram Test with No Cable Model (TP3_EQ)

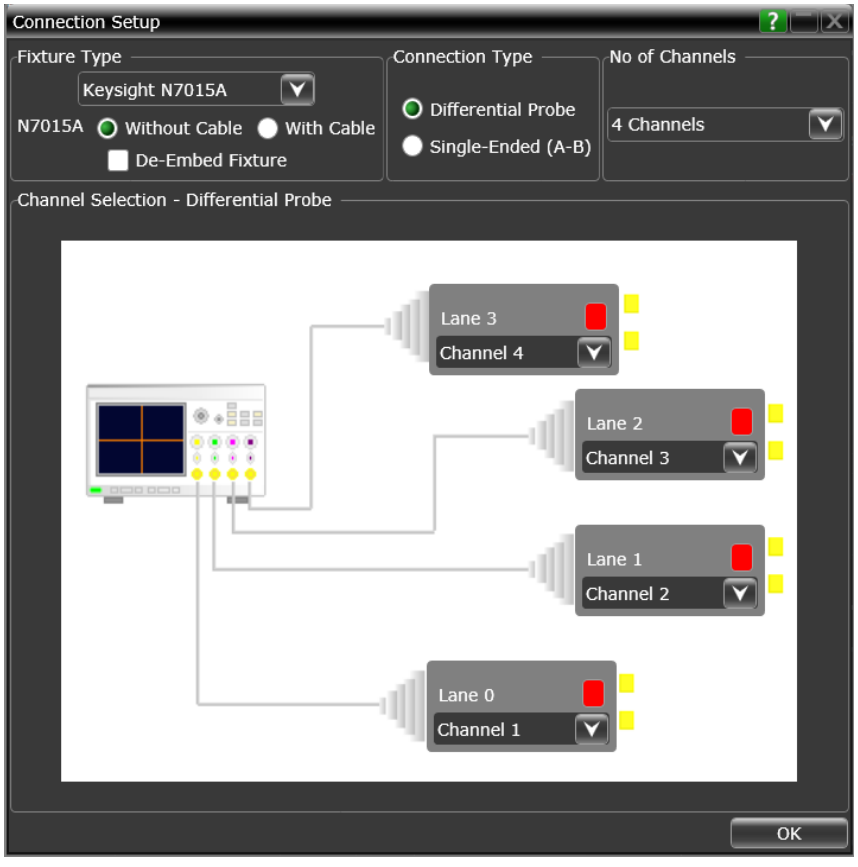
Test Overview

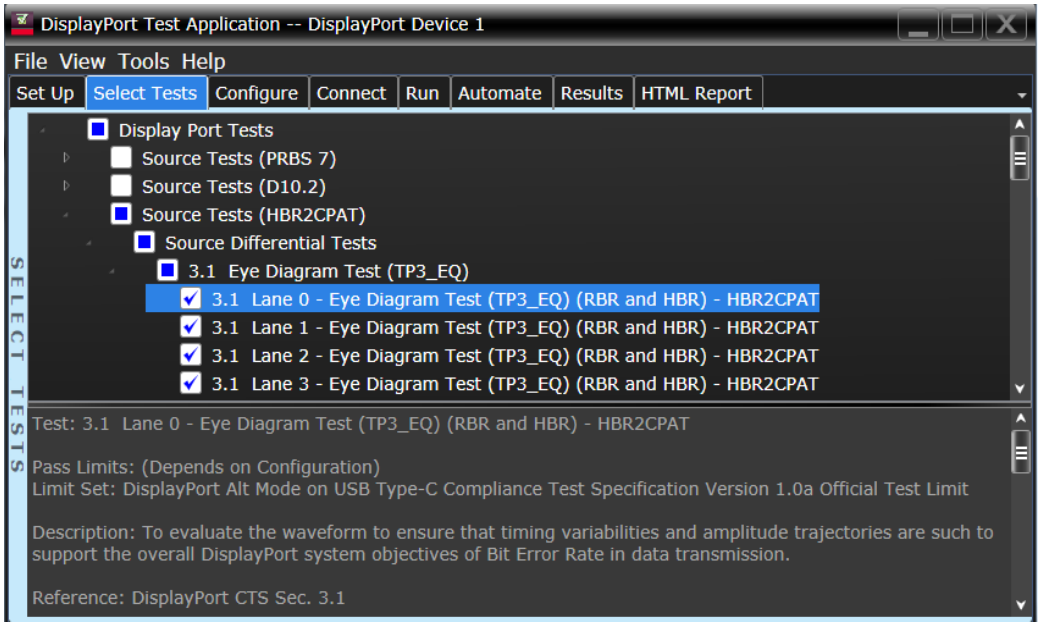
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions for Eye Diagram Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR (Informative) and HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	HBR – Level 2 HBR2 – Any Voltage Level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	HBR – Level 0 HBR2 – Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	HBR – Level 0 HBR2 – Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	HBR – PRBS7 HBR2 – HBR2CPAT
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure for HBR

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.

8 Measure the jitter of the eye diagram using the Histogram.
9 Check for any signal trajectories that may have entered into the mask.
10 Report the measurement results.

Measurement Procedure for HBR2

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]:
   a Pattern fold the equalized signal based on the High Level Voltage (V_{HIGH}) random noise configuration variable.
   b Set up the vertical waveform histogram on the equalized signal to measure random noise of High Level Voltage (V_{HIGH}).
   c Measure the High Level Voltage (V_{HIGH}) random noise based on the standard deviation of the waveform histogram.
   d Pattern fold the equalized signal based on the Low Level Voltage (V_{LOW}) random noise configuration variable.
   e Set up the vertical waveform histogram on the equalized signal to measure the random noise of Low Level Voltage (V_{LOW}).
   f Measure the Low Level Voltage (V_{LOW}) random noise based on the standard deviation of the waveform histogram.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge and right edge.
8 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.
9 Find the maximum eye height location of the eye diagram.

10 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:

a Set up the parameter of the jitter separation using the EZJIT Plus/Complete Software.

i Load the jitter separation parameter into EZJIT Plus/Complete Software based on the settings in the Configuration Variable.

ii Acquire the signal until 1,000,000 edges are analyzed.

b Note the value of the jitter component from the EZJIT Plus/Complete Software.

11 Create the eye mask based on the following criteria:

a If you select more than one lane (2 lanes or 4 lanes DUT configuration), the eye mask height and width is derate in the following manner, to include crosstalk as defined in DisplayPort 1.4 Compliance Test Specification:

i Eye Mask Width Derate (Crosstalk) = 0.04 UI

ii Eye Mask Height Derate (Crosstalk) = 0.014V

b If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]: eye mask height and width is derate as below to comprehend the noise/jitter extrapolated to BER 10^{-9} for an Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI:

i Calculate the Eye Mask Width Derate (Random Jitter) using the equation:

$$\text{Eye Mask Width Derate (Random Jitter)} = 2.5 * \text{Random Jitter}_{rms}$$

ii Calculate the Eye Mask Height Derate (Random Noise) using the equation:

V_{HIGH} Eye Mask Height Derate (Random Noise) = 2.5 * V_{HIGH} Random Noise_{rms}

V_{LOW} Eye Mask Height Derate (Random Noise) = 2.5 * V_{LOW} Random Noise_{rms}

NOTE The factor 2.5 is the delta between BER 10^{-6} (9.507) and 10^{-9} (11.996) to comprehend the noise/jitter extrapolated to BER 10-9 as the Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI.

BER	N
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996

c Place the eye mask height at the point of the maximum eye height found in Step 9.

d Calculate the Eye Mask Width:

Eye Mask Width = Eye Width Specification (0.38 UI) + Eye Mask Width Derate (Crosstalk) + 2 * Eye Mask Width Derate (Random Jitter)

e Calculate the Eye Mask Height:

Eye Mask Height = {Eye Height Specification (0.09 V) + Eye Mask Height Derate (Crosstalk)}/2 + V_{HIGH} Eye Mask Height Derate (Random Noise)

Eye Mask Height = -{Eye Height Specification (0.09 V) + Eye Mask Height Derate (Crosstalk)}/2 - V_{LOW} Eye Mask Height Derate (Random Noise)

12 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram.
   c Run the eye mask until 1,000,000 UI are folded.
13 Measure the eye height of the eye diagram using the Histogram.
14 Measure the jitter of the eye diagram using the Histogram.
15 Calculate the eye width based on the measured jitter of the eye diagram.
16 Check for any signal trajectories that may have entered into the mask.
17 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 192 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 192 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

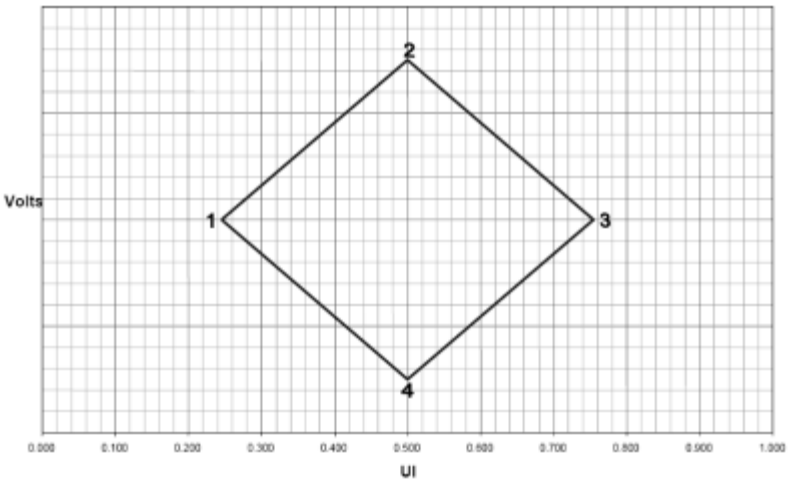


Figure 173 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 193 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.045*
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.045*

NOTE

*Eye height limit of 45 mV and -45 mV assumes cross-talk as 0, which is only possible in case of single lane testing.

In case of multi-lane testing, cross talk exists, and the eye height values deviate by ± 7 mV. Thus the eye height becomes (+45 +7) mV and (-45 -7) mV or +52 mV and -52 mV.

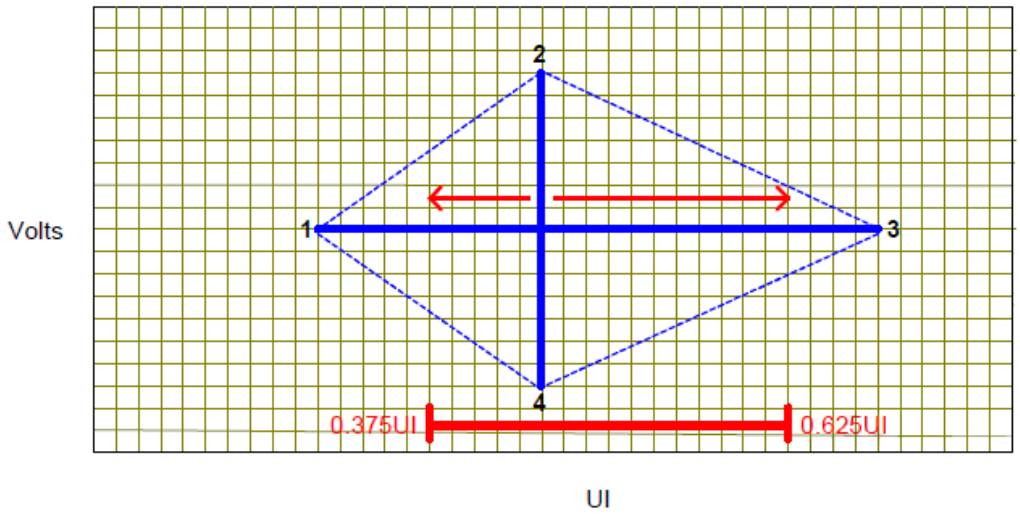


Figure 174 The Eye Mask at TP3_EQ (HBR2)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2.8.1, Table 3-29 for HBR, and Table 3-25 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Eye Diagram Test (TP3_DFE)

Test ID

For Standard DP Pattern (HBR3):

- 1217001, 1217002, 1217003, 1217004 – Eye Diagram Test (TP3_DFE)
- 1217011, 1217012, 1217013, 1217014 – Eye Diagram Test with No Cable Model (TP3_DFE)

For Arbitrary Pattern:

- 1317001, 1317002, 1317003, 1317004 – Eye Diagram Test (TP3_DFE)
- 1317011, 1317012, 1317013, 1317014 – Eye Diagram Test with No Cable Model (TP3_DFE)

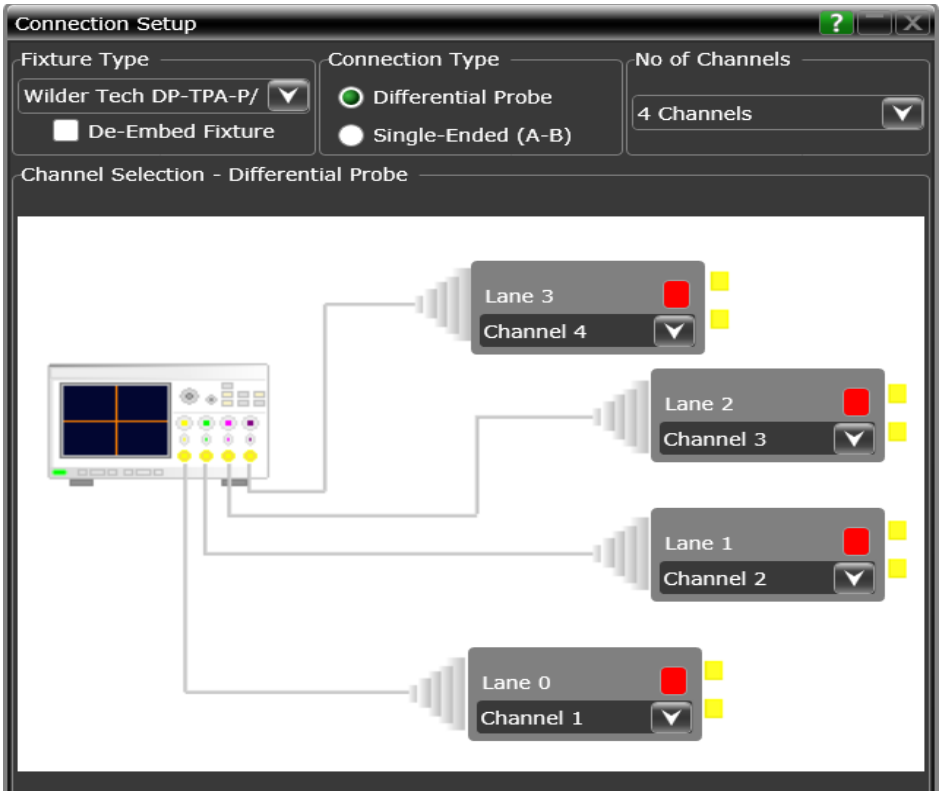
Test Overview

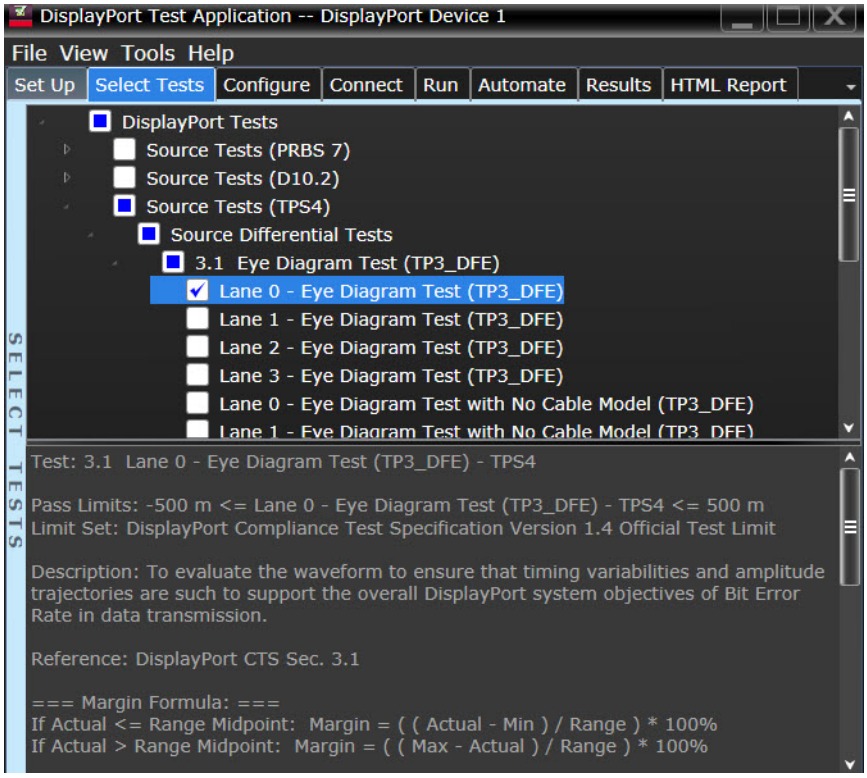
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions for Eye Diagram Test (TP3_DFE)

Test Parameter	Condition
Test Point	TP3_DFE
Bit Rate	HBR3
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any Voltage Level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	TPS4
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 3/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 3/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1



Measurement Procedure for HBR3

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_DFE): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_DFE): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.

5 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:
   a Pattern fold the equalized signal based on the High Level Voltage (V_{HIGH}) random noise configuration variable.
   b Set up the vertical waveform histogram on the equalized signal to measure random noise of High Level Voltage (V_{HIGH}).
   c Measure the High Level Voltage (V_{HIGH}) random noise based on the standard deviation of the waveform histogram.
   d Pattern fold the equalized signal based on the Low Level Voltage (V_{LOW}) random noise configuration variable.
   e Set up the vertical waveform histogram on the equalized signal to measure the random noise of Low Level Voltage (V_{LOW}).
   f Measure the Low Level Voltage (V_{LOW}) random noise based on the standard deviation of the waveform histogram.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left and right edge.
8 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.
9 Find the maximum eye height location of the eye diagram.
10 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:
   a Set up the parameter of the jitter separation using the EZJIT Plus/Complete Software.
      i Load the jitter separation parameter into EZJIT Plus/Complete Software based on the settings in the Configuration Variable.
      ii Acquire the signal until 1,000,000 edges are analyzed.
   b Note the value of the jitter component from the EZJIT Plus/Complete Software.
11 Create the eye mask based on the following criteria:
   a If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]: eye mask height and width is derate as below to comprehend the noise/jitter extrapolated to BER 10-9 for an Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI:
      i Calculate the Eye Mask Width Derate (Random Jitter) using the equation:

      Eye Mask Width Derate (Random Jitter) = 2.5 * Random Jitterrms

      ii Calculate the Eye Mask Height Derate (Random Noise) using the equation:

      VHIGH Eye Mask Height Derate (Random Noise) = 2.5 * V_{HIGH} Random Noiserms

      VLOW Eye Mask Height Derate (Random Noise) = 2.5 * V_{LOW} Random Noiserms

NOTE The factor 2.5 is the delta between BER 10^{-6} (9.507) and 10^{-9} (11.996) to comprehend the noise/jitter extrapolated to BER 10-9 as the Eye Diagram Test (TP3_DFE) only acquiring 1e6 UI.

BER	N
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996

b Place the eye mask height at the point of the maximum eye height found in Step 9.

c Calculate the Eye Mask Width:

Eye Mask Width = Eye Width Specification + 2 * Eye Mask Width Derate (Random Jitter)

d Calculate the Eye Mask Height:

Eye Mask Height = {Eye Height Specification}/2 + V_{HIGH} Eye Mask Height Derate (Random Noise)

Eye Mask Height = -{Eye Height Specification}/2 - V_{LOW} Eye Mask Height Derate (Random Noise)

12 Set up the parameters for the Mask Test.

a Load the eye mask based on the settings in the Configuration Variable.

b Center the eye mask at the middle of the eye diagram.

c Run the eye mask until 1,000,000 UI are folded.

13 Measure the eye hight of the eye diagram using the Histogram.

14 Measure the jitter of the eye diagram using the Histogram.

15 Calculate the eye width based on the measured jitter of the eye diagram.

16 Check for any signal trajectories that may have entered into the mask.

17 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 192 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 194 Eye Diagram Mask Coordinates for TP3_DFE (HBR3)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the eye width is open from x to x + 0.53 UI	0.00000
2	Any passing UI location between 0.375 and 0.625 UI	0.0375
3	Point 1 + 0.35 UI	0.00000
4	Same as point 2	- 0.0375

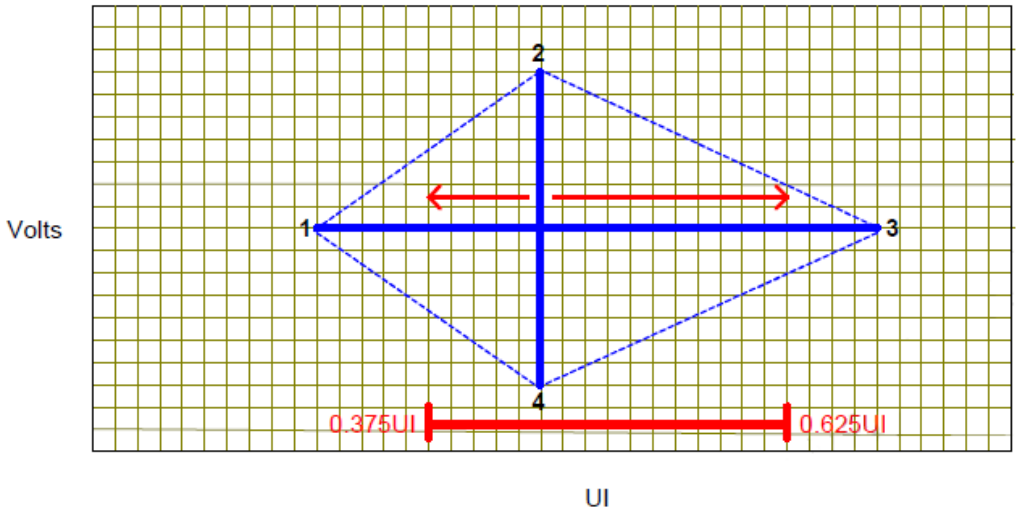


Figure 175 The Eye Mask at TP3_DFE (HBR3)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*

Expected/Observable Results

The measured eye diagram for the test signal at TP3_DFE shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test (TP3_EQ)

Test ID

For Standard DP Pattern:

- 1225001, 1225002, 1225003, 1225004 – Total Jitter Test (TP3_EQ) - PRBS 7
- 1225011, 1225012, 1225013, 1225014 – Total Jitter Test with No Cable Model (TP3_EQ) -PRBS 7
- 1222001, 1222002, 1222003, 1222004 – Total Jitter Test (TP3_EQ) - HBR2CPAT
- 1222011, 1222012, 1222013, 1222014 – Total Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1221001, 1221002, 1221003, 1221004 – Total Jitter Test (TP3_EQ) - D10.2
- 1221011, 1221012, 1221013, 1221014 – Total Jitter Test with No Cable Model (TP3_EQ) - D10.2

For Arbitrary Pattern:

- 1322001, 1322002, 1322003, 1322004 – Total Jitter Test (TP3_EQ)
- 1322011, 1322012, 1322013, 1322014 – Total Jitter Test with No Cable Model (TP3_EQ)

Test Overview

The objective of this test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

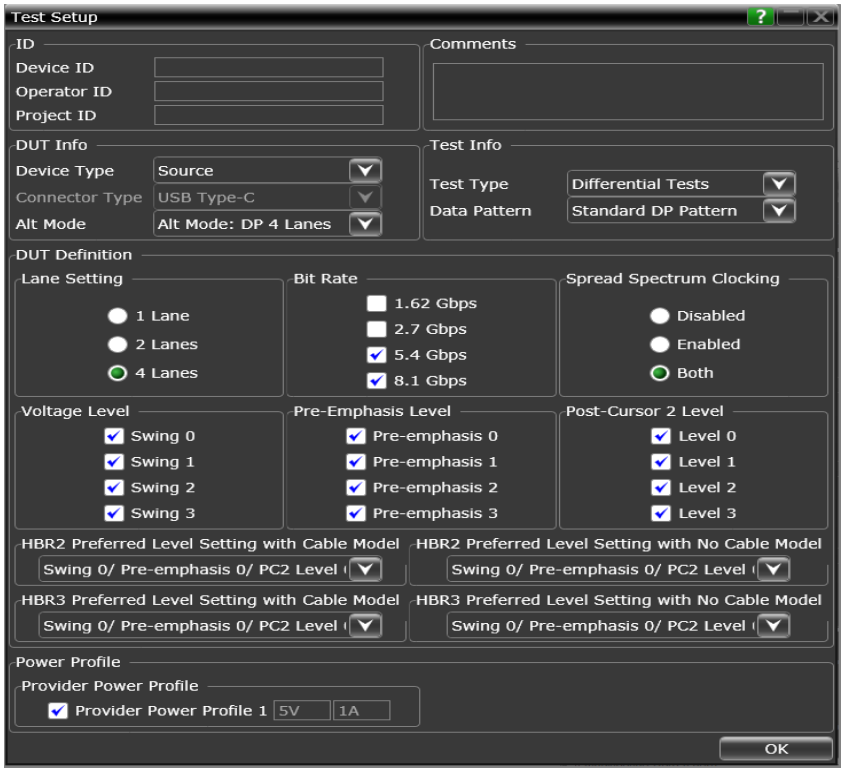
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

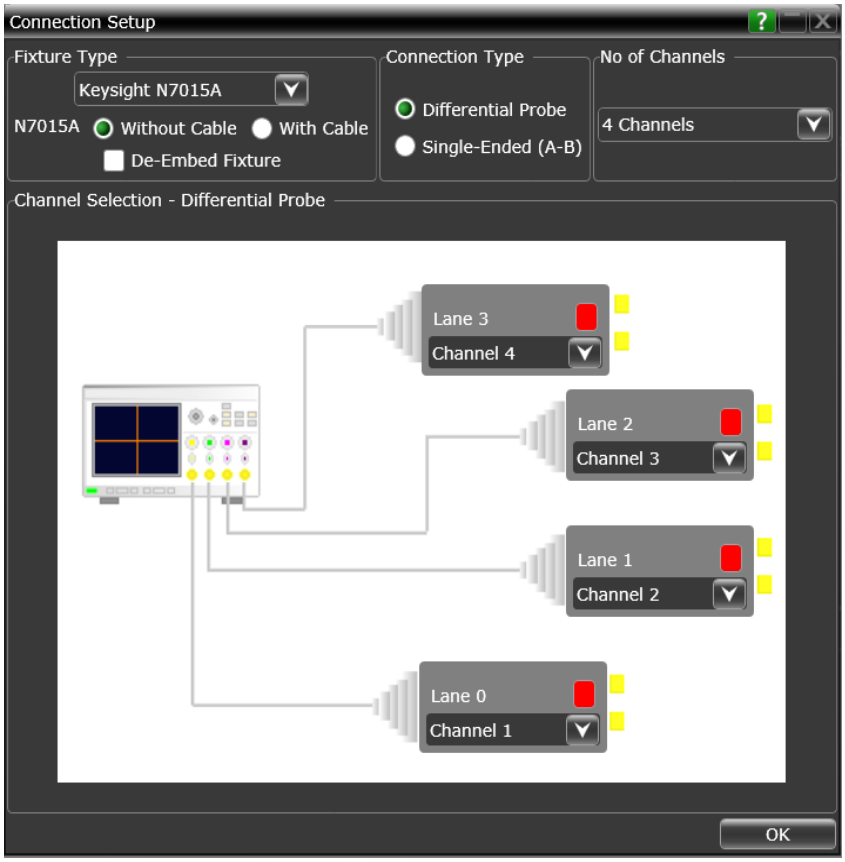
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

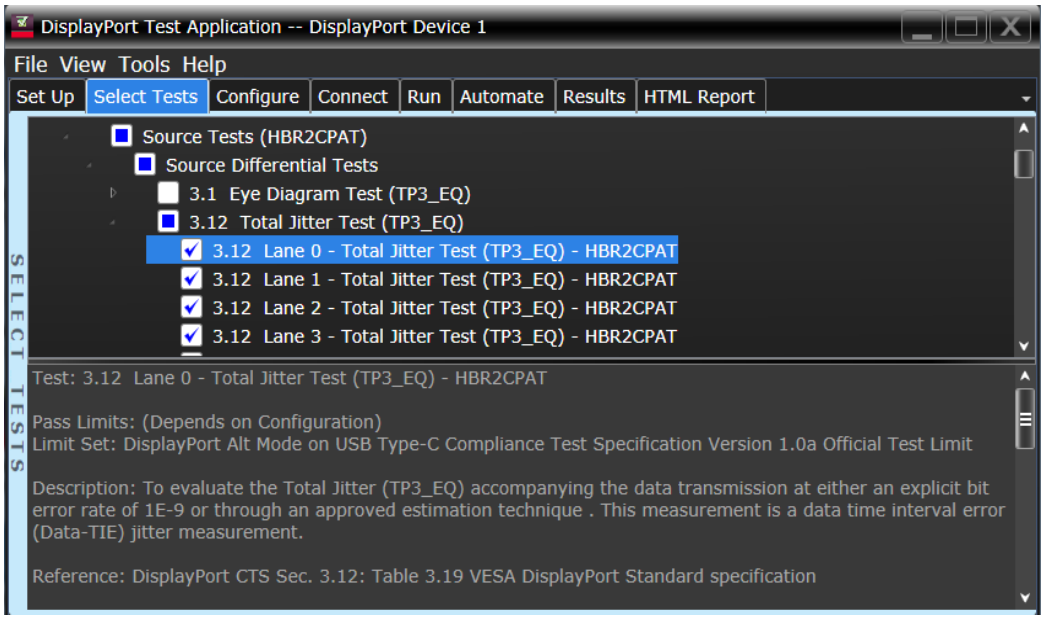
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR (Informative) and HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	HBR: PRBS 7, HBR2: D10.2, and HBR2CPAT
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Total Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Total Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 195 Total Jitter at TP3_EQ

	Receiver Connector (TP3_EQ)
High-Bite Rate 2 (5.4 Gb/s per lane) - for D10.2 pattern	
A_{p-p}	≤ 0.40 UI
High-Bit Rate 2 (5.4 Gb/s per lane) - for HBR2CPAT (or CP2520) pattern	
A_{p-p}	≤ 0.580 UI*
High-Bite Rate (2.7 Gb/s per lane) - for PRBS7	
A_{p-p}	≤ 0.491 UI

* The HBR2 limits for Total Jitter calculated at TP3_EQ include a de-rating of 0.04 UI to account for cable crosstalk effect.

UI is Unit Interval.

Test References

See:

For HBR (PRBS7)

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2.7.2, Table 3-23*

For HBR2CPAT

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2.7.2, Table 3-23*

For D10.2

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*

Expected/Observable Results

The measured total jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Total Jitter Test (TP3_DFE)

Test ID

For Standard DP Pattern:

- 1224001, 1224002, 1224003, 1224004 – Total Jitter Test (TP3_DFE)
- 1223011, 1223012, 1223013, 1223014 – Total Jitter Test (TP3_DFE)

For Arbitrary Pattern:

- 1324001, 1324002, 1324003, 1324004 – Total Jitter Test (TP3_DFE)
- 1324011, 1324012, 1324013, 1324014 – Total Jitter Test (TP3_DFE)

Test Overview

The objective of this test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

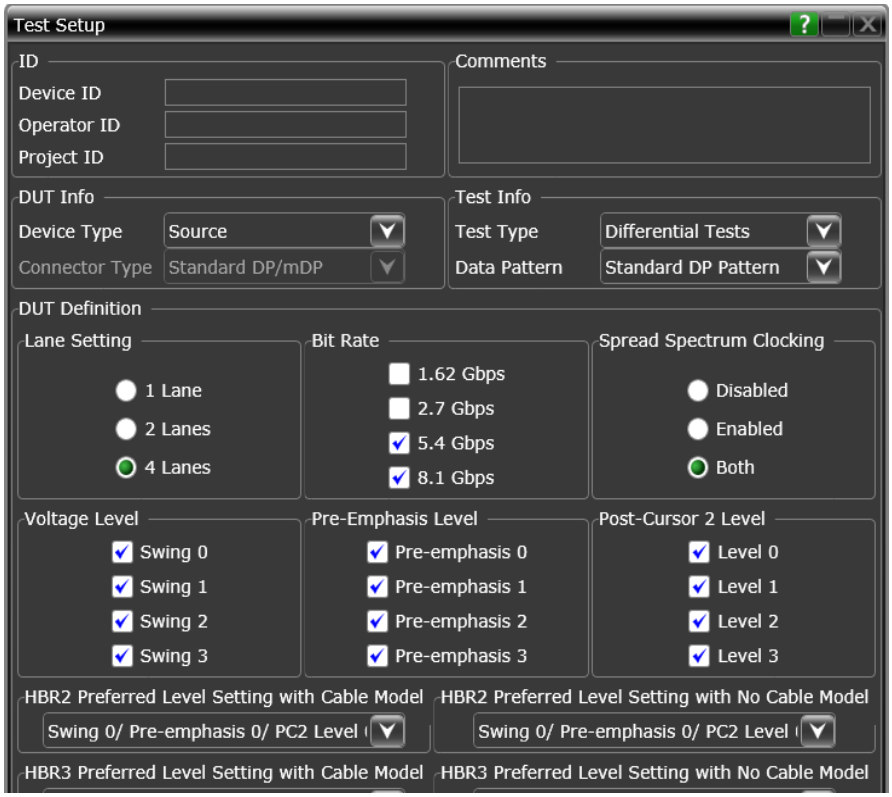
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

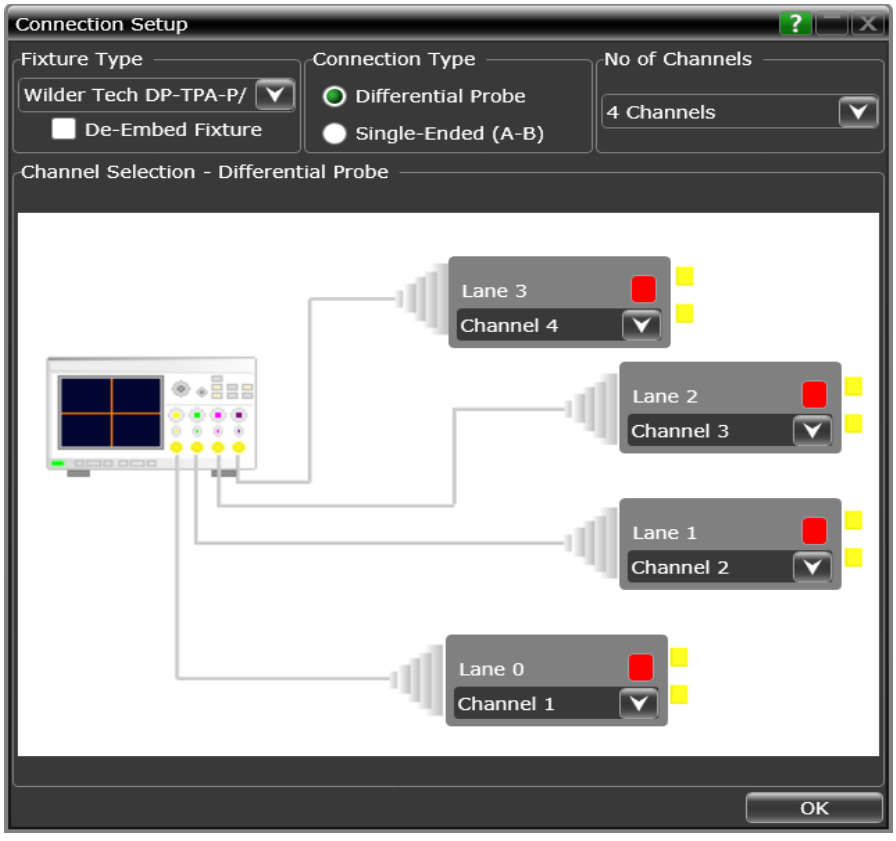
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

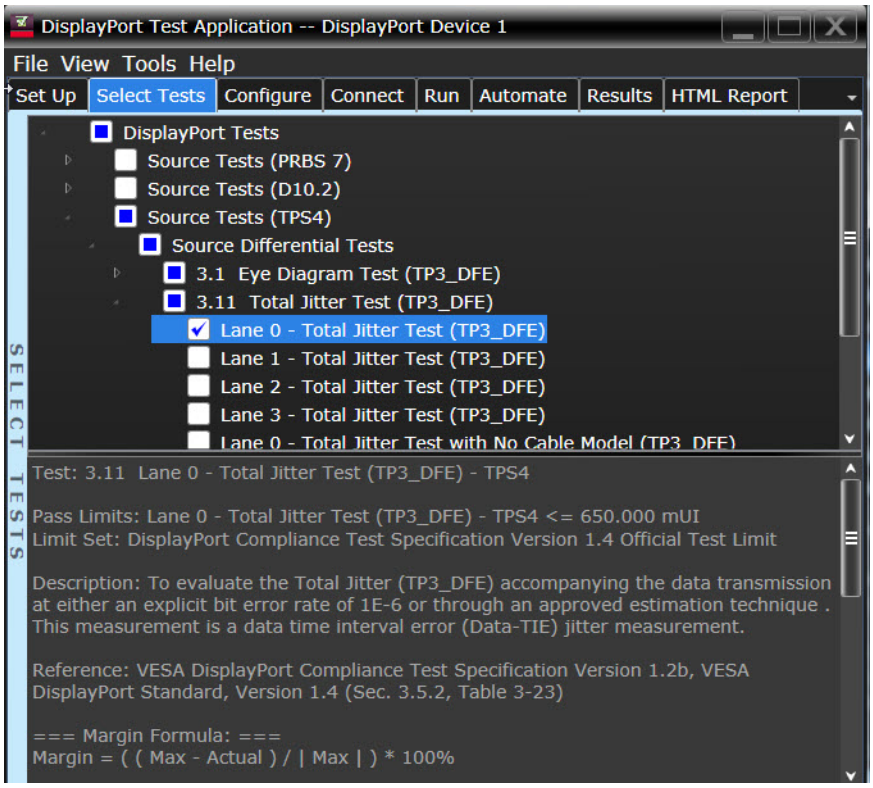
where, DJ is the Deterministic Jitter, RJ is the Random Jitter, and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test (TP3_DFE)

Test Parameter	Condition
Test Point	TP3_DFE
Bit Rate	HBR3
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	TPS4
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
HBR3 Preferred Level Setting with No Cable Model


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Total Jitter Test (TP3_DFE): Use "Worst Cable Model" as defined in the section "Cable Model".
   b For Total Jitter Test with No Cable Model (TP3_DFE): Use "Zero Length Cable Model" as defined in the section "Cable Model".
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”, exclude the DFE.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.

5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 196 Total Jitter at TP3_DFE

	Receiver Connector (TP3_DFE)
High-Bite Rate 3 (8.1 Gb/s per lane)	
A_{P-P}	0.65 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*

Expected/Observable Results

The measured total jitter for the test signal at TP3_DFE shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non ISI Jitter Test (TP3_DFE)

Test ID

For Standard DP Pattern:

- 1231001, 1231002, 1231003, 1231004 – Non ISI Jitter Test (TP3_DFE) - HBR2CPAT
- 1231011, 1231012, 1231013, 1231014 – Non ISI Jitter Test with No Cable Model (TP3_DFE) - HBR2CPAT

For Arbitrary Pattern:

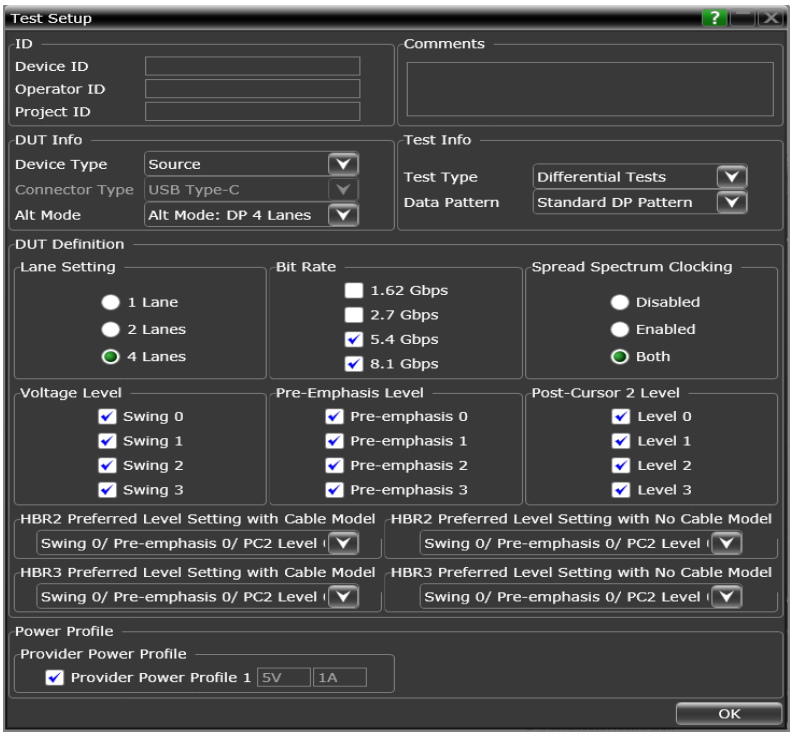
- 1331001, 1331002, 1331003, 1331004 – Non ISI Jitter Test (TP3_DFE)
- 1331011, 1331012, 1331013, 1331014 – Non ISI Jitter Test with No Cable Model (TP3_DFE)

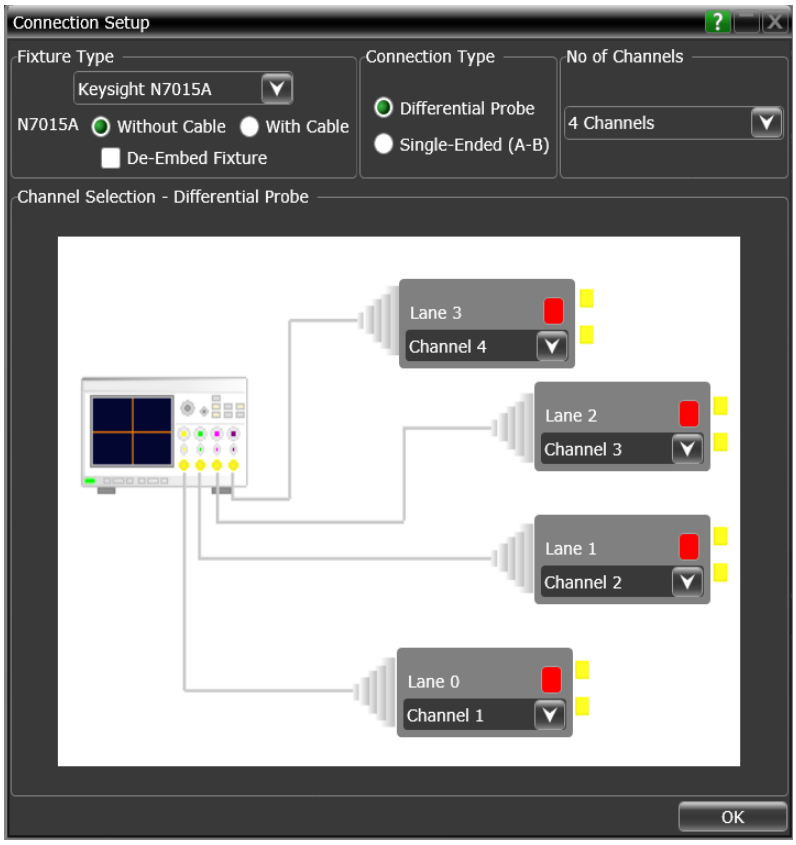
Test Overview

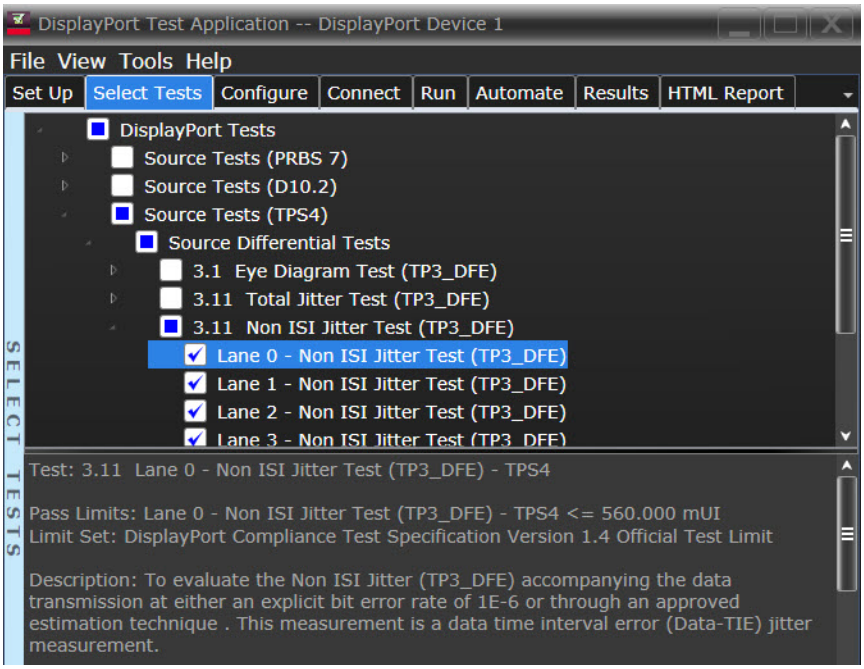
The objective of this test is to evaluate the non ISI jitter accompanying the data transmission.

Test Conditions for Non ISI Jitter Test (TP3_DFE)

Test Parameter	Condition
Test Point	TP3_DFE
Bit Rate	HBR3
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	TPS4
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Non ISI Jitter Test (TP3_DFE): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Non ISI Jitter Test with No Cable Model (TP3_DFE): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Calculate the non ISI jitter base on following equation:
   Non ISI Jitter = TJ - ISI

8 Report the measurement results.

PASS Condition

Table 197 Non ISI Jitter at TP3_DFE

	Receiver Connector (TP3_DFE)
High-Bit Rate 3 (8.1 Gb/s per lane)	
A_{p-p}	0.56 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2.7.2, Table 3-23*

Expected/Observable Results

The measured non ISI jitter for the test signal at TP3_DFE shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Deterministic Jitter Test (TP3_EQ)

Test ID

For Standard DP Pattern:

- 1236001, 1236002, 1236003, 1236004 – Deterministic Jitter Test (TP3_EQ) - HBR2CPAT
- 1236011, 1236012, 1236013, 1236014 – Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1235001, 1235002, 1235003, 1235004 – Deterministic Jitter Test (TP3_EQ) - D10.2
- 1235011, 1235012, 1235013, 1235014 – Deterministic Jitter Test with No Cable Model (TP3_EQ) - D10.2

For Arbitrary Pattern:

- 1336001, 1336002, 1336003, 1336004 – Deterministic Jitter Test (TP3_EQ)
- 1336011, 1336012, 1336013, 1336014 – Deterministic Jitter Test with No Cable Model (TP3_EQ)

Test Overview

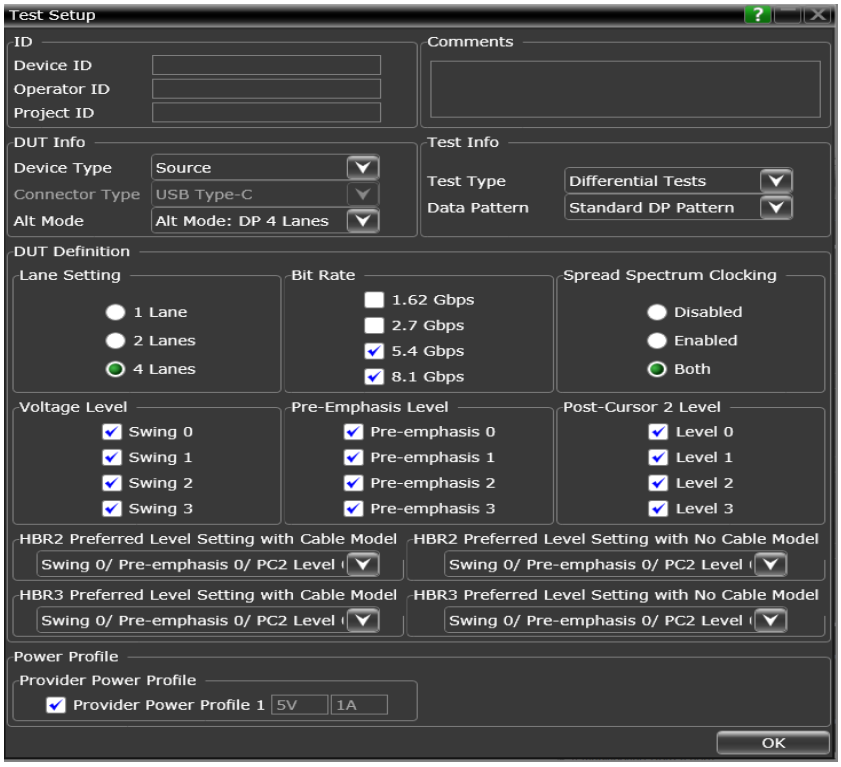
The objective of this test is to evaluate the deterministic jitter accompanying the data transmission. The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

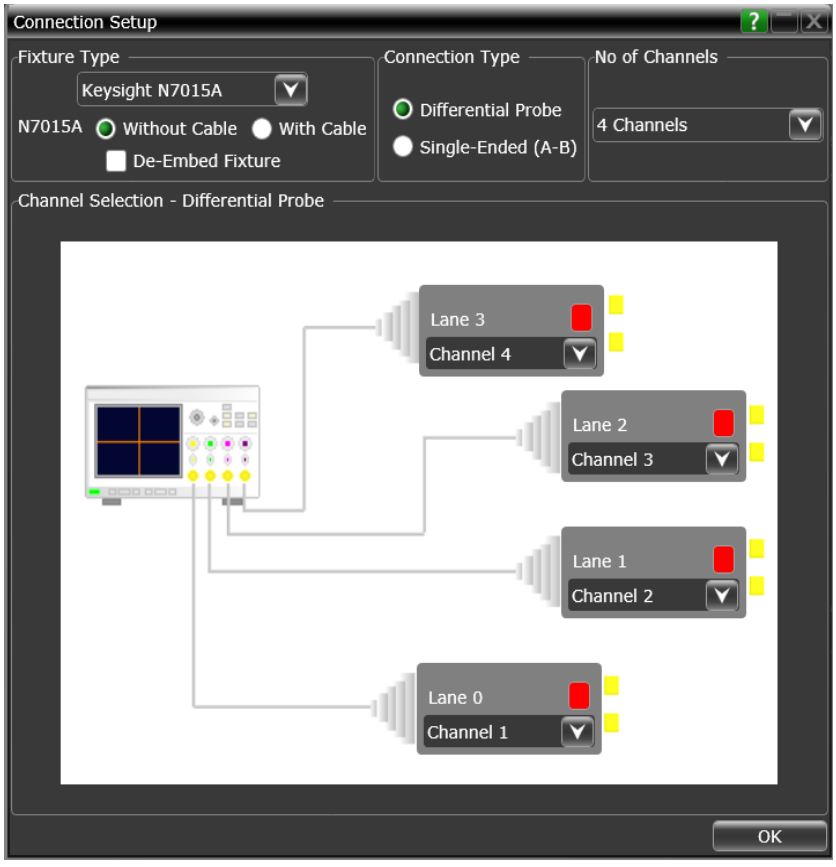
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

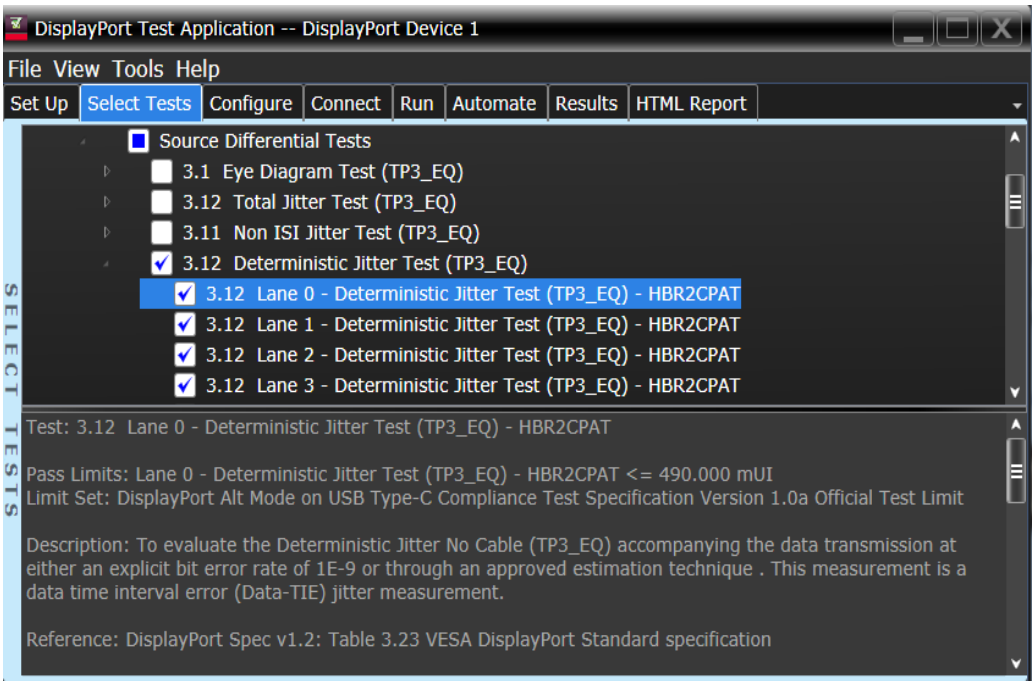
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Deterministic Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Deterministic Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Deterministic Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 198 Deterministic Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.49 UI

Table 199 Deterministic Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.27 UI

UI is Unit Interval.

Test References

See:

For HBR2CPAT

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2.7.2, Table 3-23*

For D10.2

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*

Expected/Observable Results

The measured deterministic jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Random Jitter Test (TP3_EQ)

Test ID

For Standard DP Pattern:

- 1238001, 1238002, 1238003, 1238004 – Random Jitter Test (TP3_EQ) - D10.2
- 1238011, 1238012, 1238013, 1238014 – Random Jitter Test with No Cable Model (TP3_EQ) - D10.2

For Arbitrary Pattern:

- 1338001, 1338002, 1338003, 1338004 – Random Jitter Test (TP3_EQ)
- 1338011, 1338012, 1338013, 1338014 – Random Jitter Test with No Cable Model (TP3_EQ)

Test Overview

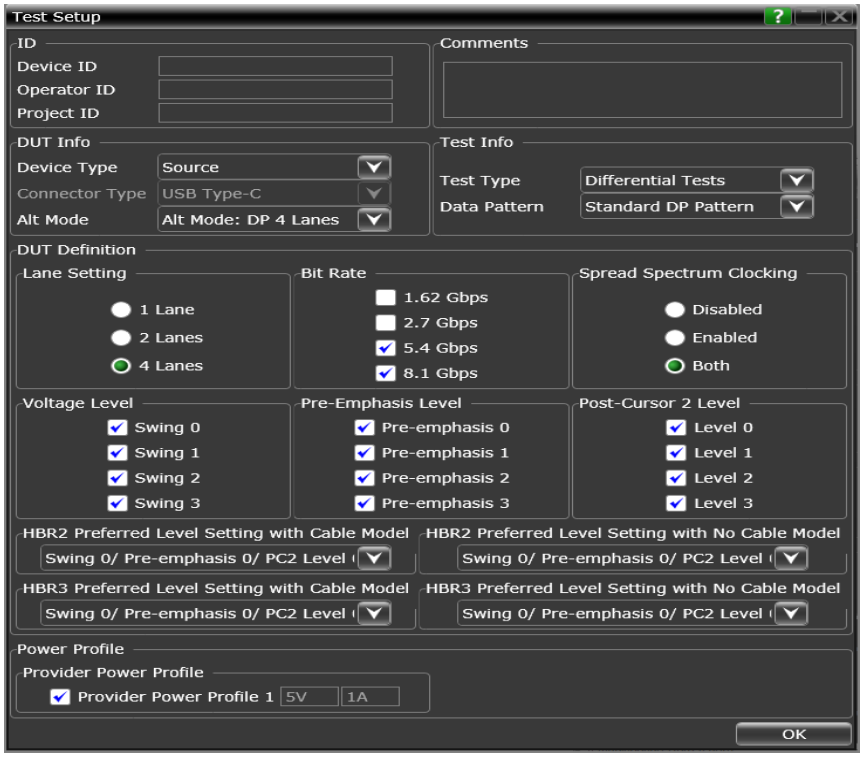
The objective of this test is to evaluate the random jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. The jitter is separated into each jitter components and the random jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

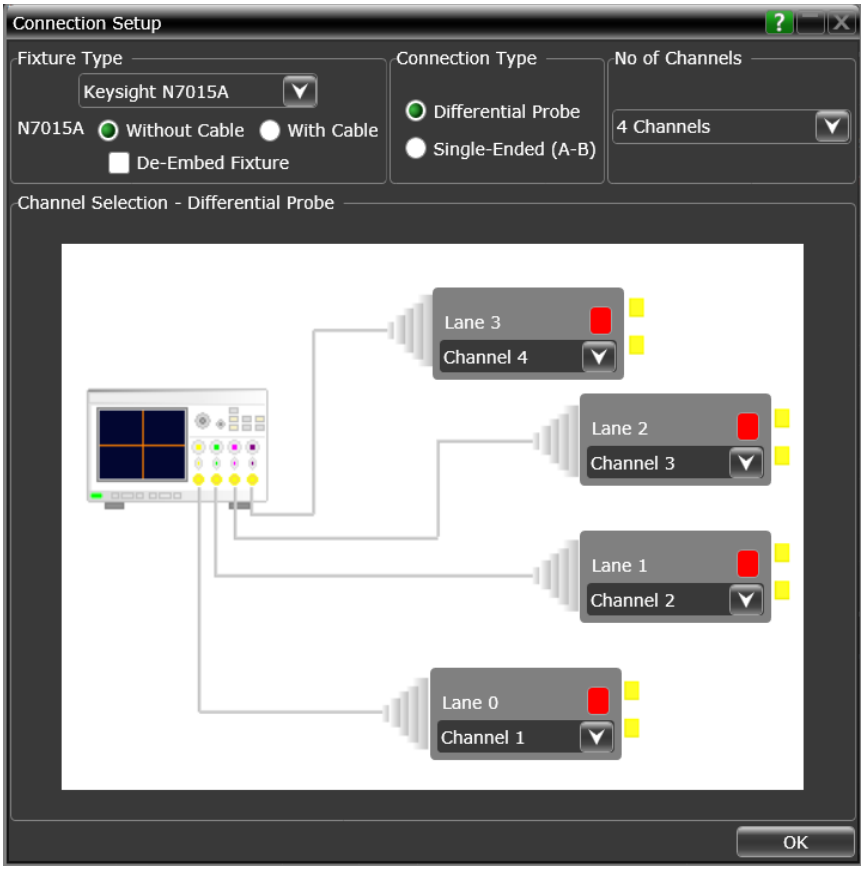
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

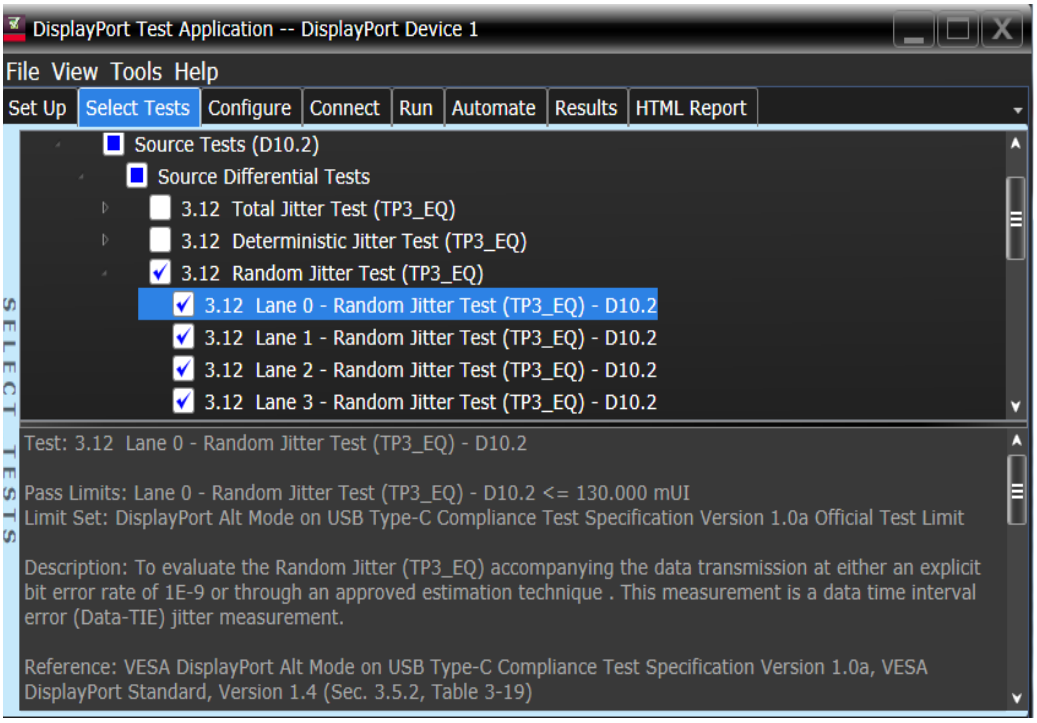
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Random Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	D10.2
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Random Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Random Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 200 Random Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.13 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-19*

Expected/Observable Results

The measured random jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source AC Common Mode Test (Informative)

Test ID

For Standard DP Pattern:

- 12110001, 12110002, 12110003, 12110004 – AC Common Mode Test (Informative)

For Arbitrary Pattern:

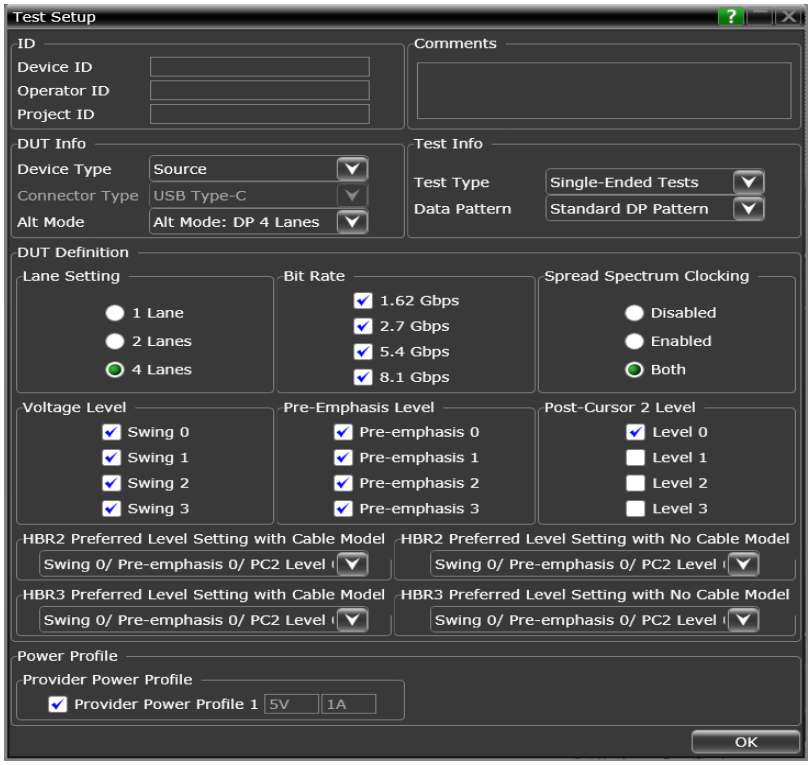
- 13110001, 13110002, 13110003, 13110004 – AC Common Mode Test (Informative)

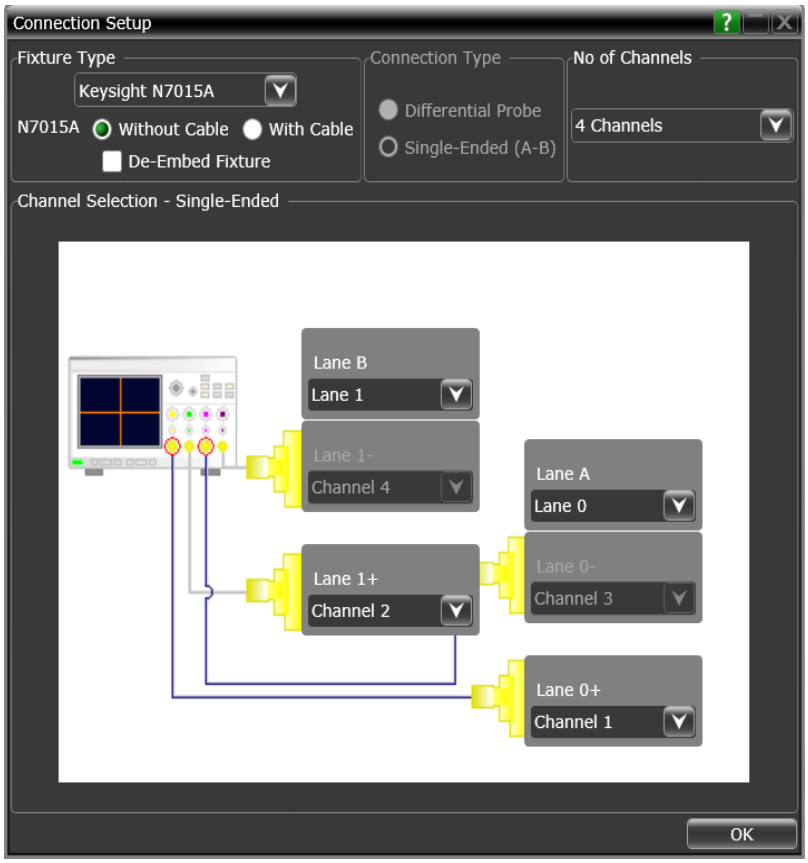
Test Overview

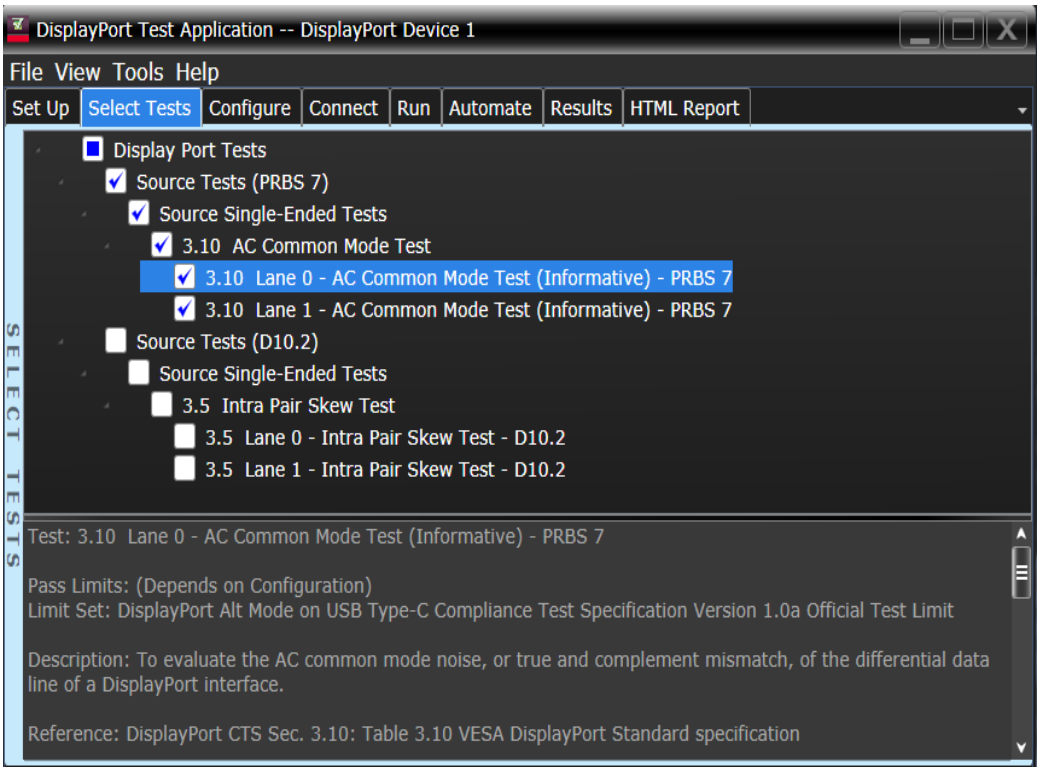
The objective of this test is to evaluate the AC Common Mode noise (unfiltered rms) of the differential data line of the DP interface.

Test Conditions for AC Common Mode Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels supported subject to the constraints in Table 3-1 of the VESA DisplayPort 1.4 Standard
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Single-Ended Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Create FUNC3 signal, which is the common mode signal of the input single-ended signal.
4 If the filter is enabled ["Filter" configuration variable set to "High Pass Filter", "Low Pass Filter" or "None" (Default)]:
   a Create FUNC4 signal, which is the filtered FUNC3 signal by applying the High Pass filter or Low Pass filter on the FUNC3 signal based on the Configuration Variable.
5 Set up two display grids such that one grid displays the input single-ended signal while the other grid displays the common mode signal.
6 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.

7 Set up the parameters for RMS voltage measurement of the common mode signal.
   a Set up the V_{rms} measurement for the common mode signal.
   b Acquire the signal until 100,000 edges are measured.
8 Get the mean for the V_{rms} measurement.
9 Report the measurement results.

PASS Condition

For RBR and HBR:

AC Common Mode Voltage $\leq$ 20mV

For HBR2 and HBR3:

AC Common Mode Voltage $\leq$ 30mV

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.10*
- *VESA DisplayPort (DP) Standard Version 1.4, Section D.2, Table D-3*

Expected/Observable Results

The measured AC common mode noise for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Intra-Pair Skew Test (Informative)

Test ID

For Standard DP Pattern:

- 12100001, 12100002, 12100003, 12100004 – Intra-Pair Skew Test (Informative)

For Arbitrary Pattern:

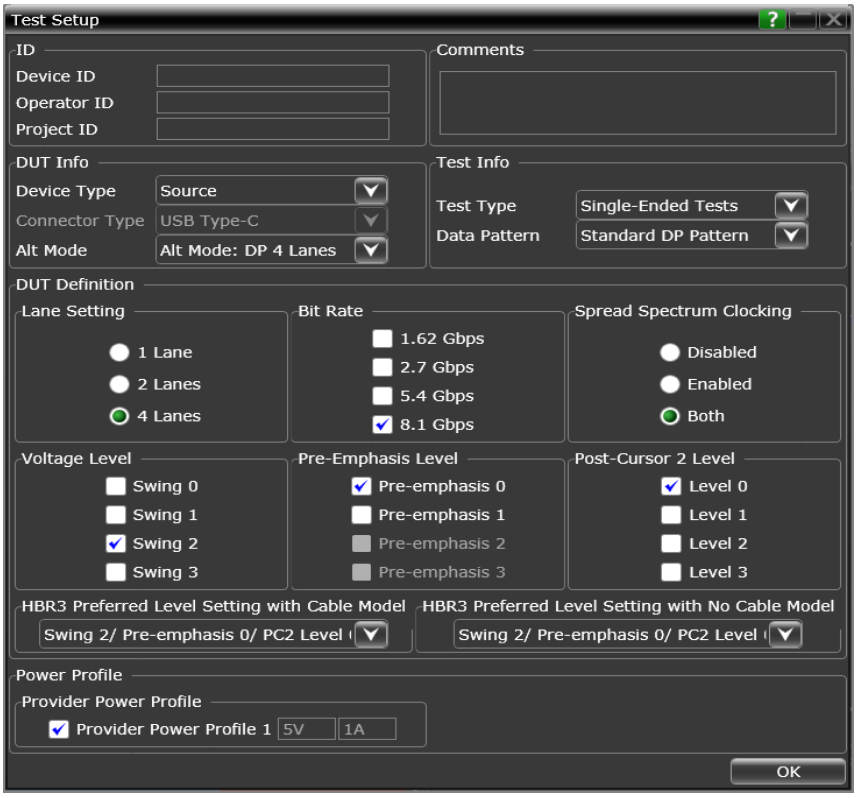
- 13100001, 13100002, 13100003, 13100004 – Intra-Pair Skew Test (Informative)

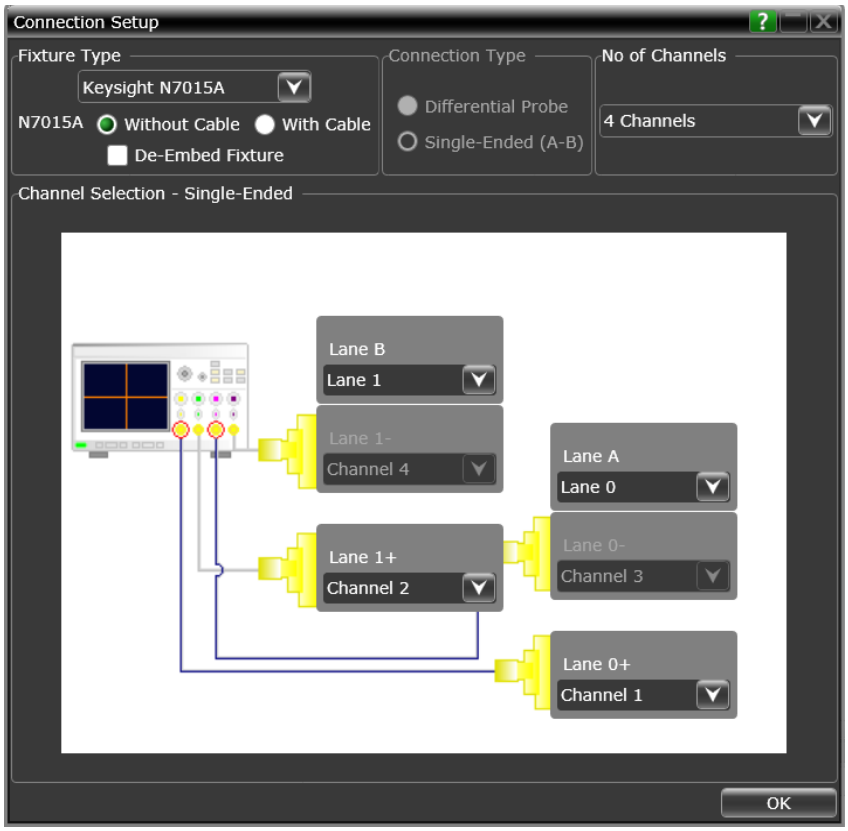
Test Overview

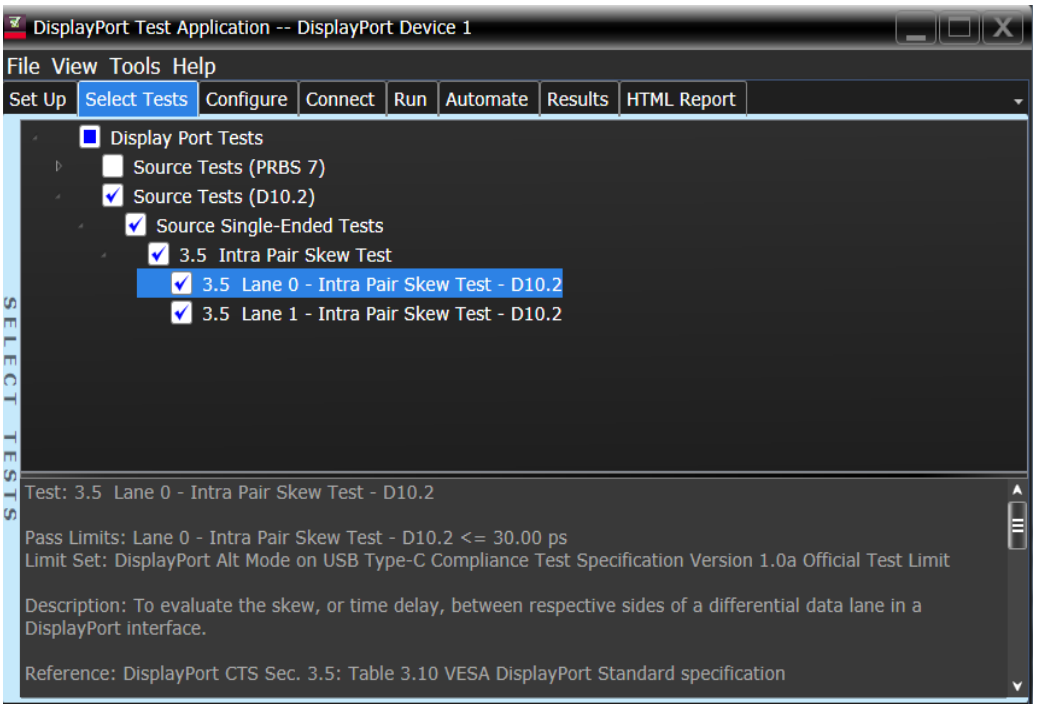
The objective of this test is to evaluate the skew or time delay between respective sides of a differential data lane in the DP interface.

Test Conditions for Intra-Pair Skew Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR3)
SSC	Both SSC conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported For one lane operation: Lane 0+ to Lane 0- For two lane operation: Lane 0+ to Lane 0- Lane 1+ to Lane 1- For four lane operation: Lane 0+ to Lane 0- Lane 1+ to Lane 1- Lane 2+ to Lane 2- Lane 3+ to Lane 3-
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Single-Ended Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR3 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
4 Set up the parameters to perform High Level Voltage (V_{HIGH}) and Low Level Voltage (V_{LOW}) for each input single-ended signal.
   a Scale the vertical display of the input single-ended signal to optimum value.
   b Acquire the signal for 100 waveforms.
   c Find V_{HIGH} by measuring the average voltage at 0.06 UI to 0.75 UI of the High Level.
   d Find V_{LOW} by measuring the average voltage at 0.06 UI to 0.75 UI of the Low Level.
   e Calculate the Transition Voltage (V_{Trans}) using the equation:

$$V_{Trans} = (V_{HIGH} + V_{LOW}) / 2$$

5 Set up the parameters for the intra-pair skew measurement:

a Set up the measurement threshold for each single-ended data signal based on the measured Transition Voltage.

b Set up InfiniiScan to trigger on the desired pattern.

c Set up delta time measurement to measure time difference between the rising edge of the data true signal (D+) and the complement's (D-) falling edge:

$$D+_{Transition\_High} - D-_{Transition\_Low}$$

d Set up delta time measurement to measure time difference between the falling edge of the data true signal (D+) and the complement's (D-) rising edge:

$$D+_{Transition\_Low} - D-_{Transition\_High}$$

e Acquire the signal until you measure 100 edges.

f Calculate the intra-pair skew using the equation:

$$\text{Intra-Pair Skew} = \{1/\text{Number of Edges}\}$$

$$\sum \{[(D+_{Transition\_High} - D-_{Transition\_Low}) + (D+_{Transition\_Low} - D-_{Transition\_High})] / 2\}$$

6 Report the measurement results.

PASS Condition

Intra-Pair skew ≤ 30 ps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.5*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.5.2, Table 3-18*

Expected/Observable Results

The measured intra-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

25 DPoC Sink Tests

Overview

The specifications and the conceptual information for the DPoC standard are aligned with that for the DisplayPort 1.4 standard. For more information, refer to "Overview" on page 348.

Setting Up the DisplayPort Compliance Test Application for DPoC Sink Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort Standards with Type-C capability, select the option **DPoC** in the **Test Specification** area.
5. The option **Physical Layer Tests** appears by default in the **Test Selection** area.
6. Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.
7. In the **Type-C Environment Setup** area, select **Enable Type-C Controller** to activate the **DUT Orientation** field and the **Setup Type-C Controller** button. To know about how to configure the Type-C Controller, refer to the *Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help*.
8. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
9. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
10. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
11. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
12. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
13. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
14. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
15. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DPoC Sink Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

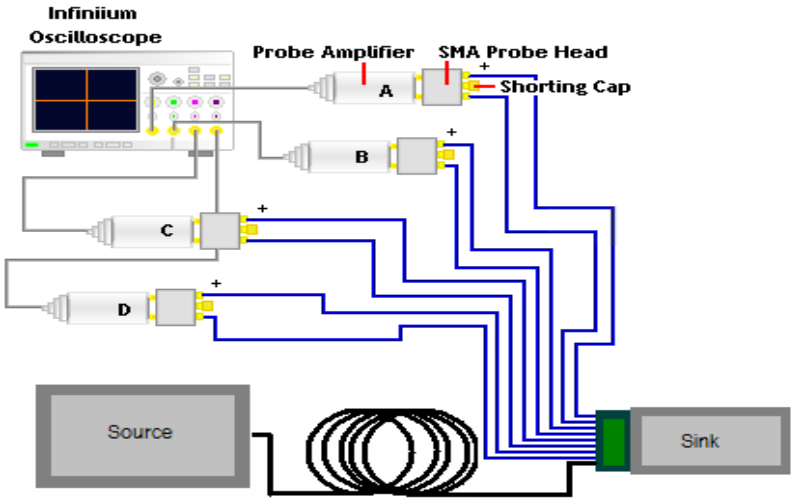


Figure 176 Sample connection diagram for DPoC Sink Tests with Differential Probes

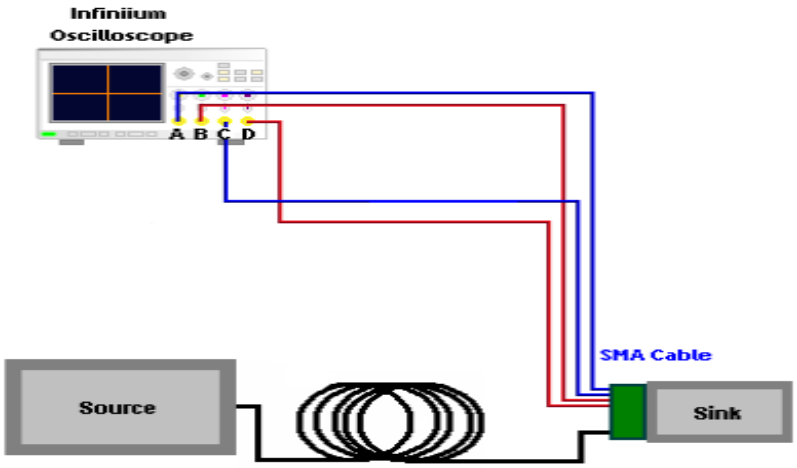


Figure 177 Sample connection diagram for DPoC Sink Tests with Single-Ended Probes

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Sink tests to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1. In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.
2. On the **Test Setup** window,
   a. Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.
   b. In the **DUT Info** area, select **Device Type** as **Sink**. The **Connector Type** is grayed out. From the drop-down options for **Alt Mode**, select either **Alt Mode: DP 4 Lanes** or **Alt Mode: DP 2 + 2**.
   c. In the **Test Info** area, the **Test Type** is grayed out.
   d. In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.
3. Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1. Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.
2. On the **Connection Setup** window,
   a. The **Fixture Type** area is grayed out.
   b. Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.
   c. In the **Channel Selection** area, assign appropriate channels to lanes.
3. Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of sink tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for DPoC Sink Tests" on page 976 to complete the task flow for DUT setup along with configuring the Compliance Application to run each test.

Sink Eye Diagram Test

Test ID

12140001, 12140002, 12140003, 12140004 – Eye Diagram Test

Test Overview

The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

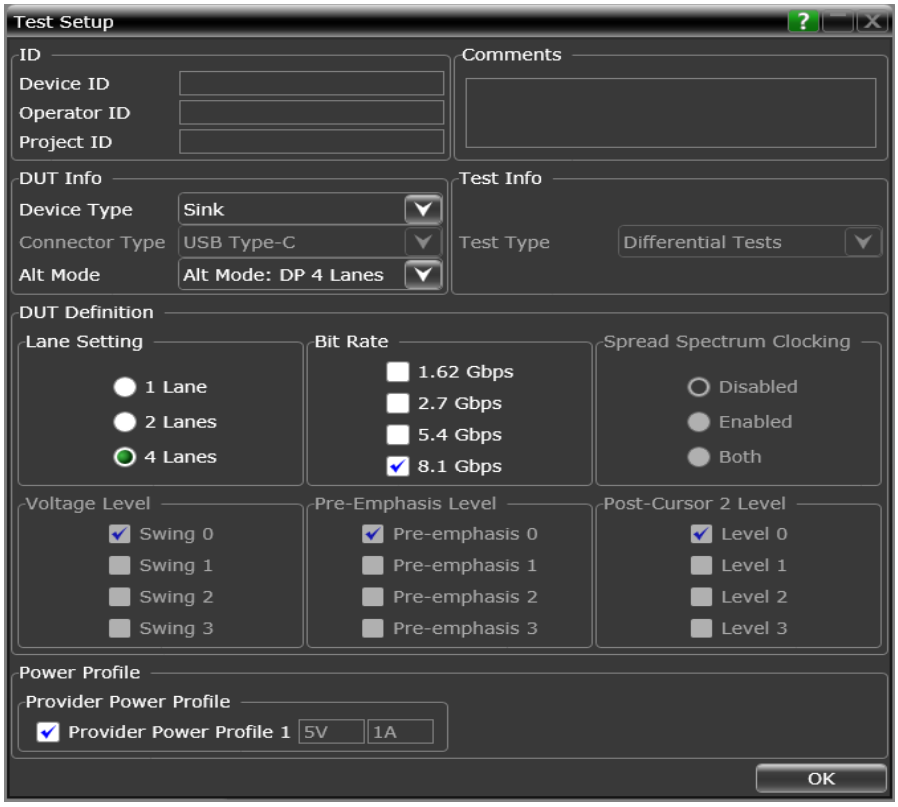
You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the following specifications for degradation:

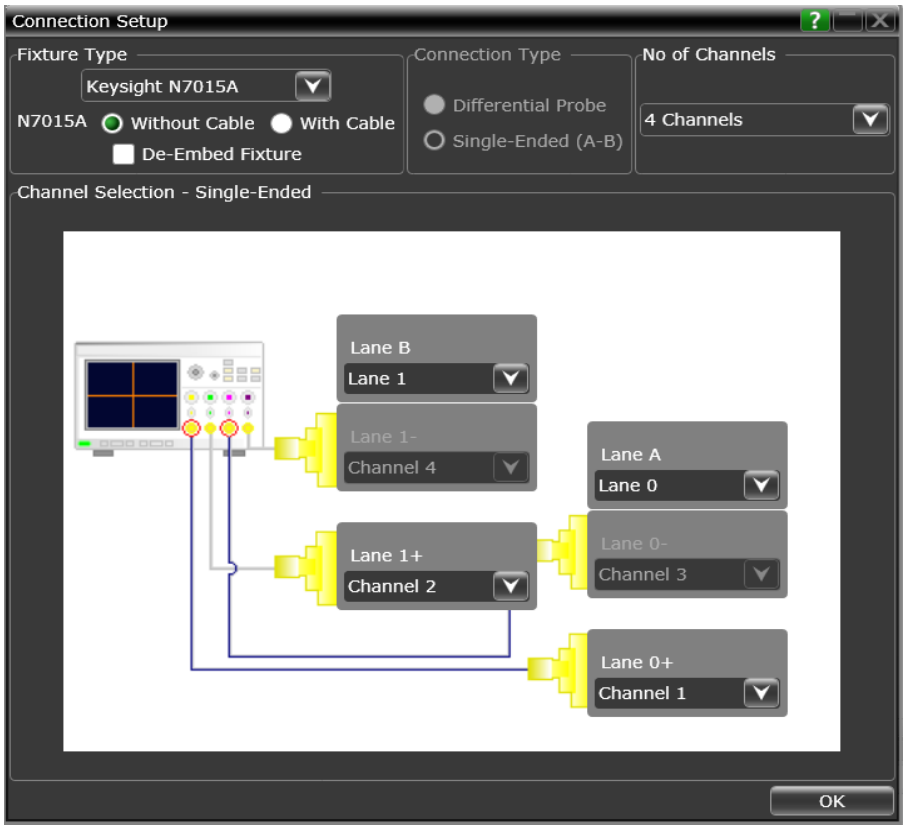
- Voltage Level:
  - 90mV peak to peak +/- 10% for HBR2 at TP3_EQ (Table 3-18, DP1.2a)
  - 150mV peak to peak +/- 10% for HBR at TP3_EQ (Table 3-25, DP1.2a)
  - 46mV peak to peak +/- 10% for RBR at TP3 (Table 3-26, DP1.2a

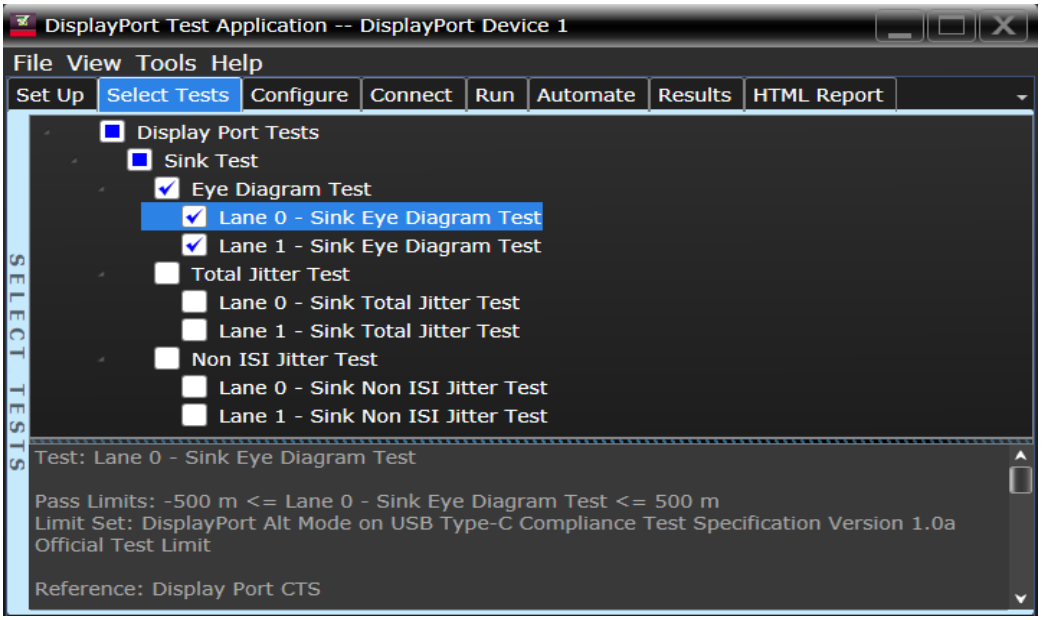
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR3–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR3)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR3–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
9 Measure the jitter of the eye diagram using the Histogram.

10 Check for any signal trajectories that may have entered into the mask.

11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 201 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 201 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

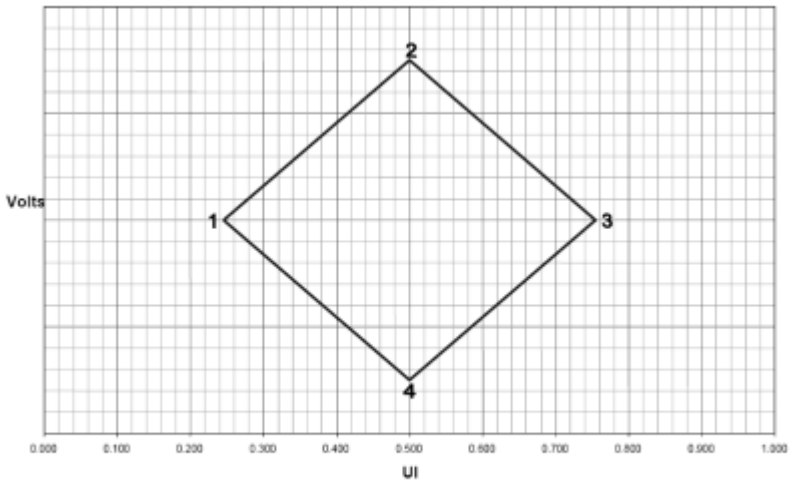


Figure 178 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 202 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.0045*
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.0045*

NOTE

*Eye height limit of 45 mV and -45 mV assumes cross-talk as 0, which is only possible in case of single lane testing.

In case of multi-lane testing, cross talk exists, and the eye height values deviate by ± 7 mV. Thus the eye height becomes (+45 +7) mV and (-45 -7) mV or +52 mV and -52 mV.

Table 203 Eye Diagram Mask Coordinates for TP3_EQ (HBR3)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.35UI	0.00000
2	Any passing UI location between 0.375 and 0.625UI	0.00375
3	Point 1 + 0.35UI	0.00000
4	Same as Point 2	-0.00375

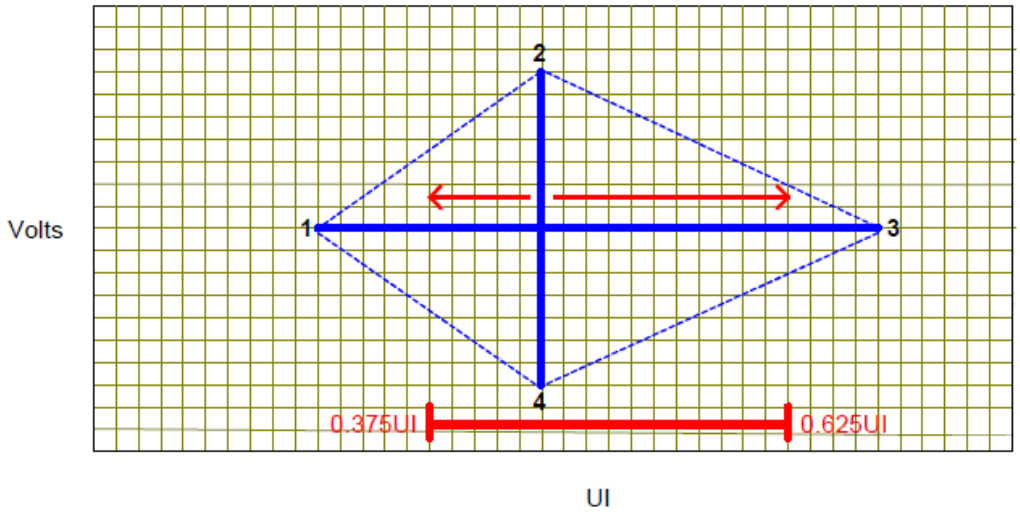


Figure 179 The Eye Mask at TP3_EQ (HBR2 and HBR3)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Sink Total Jitter Test

Test ID

12210001, 12210002, 12210003, 12210004 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

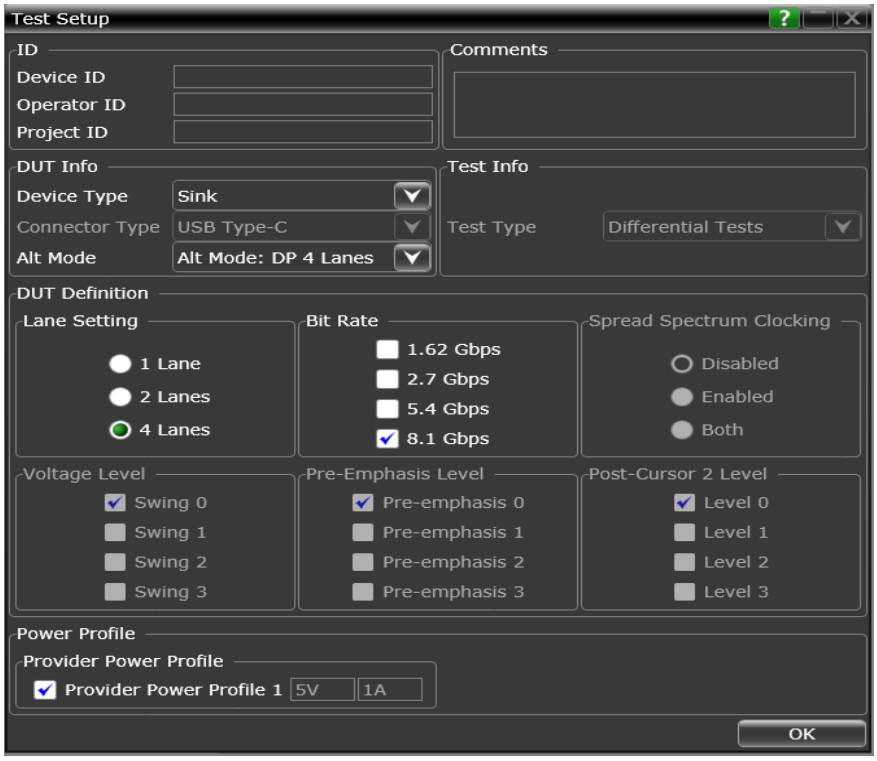
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

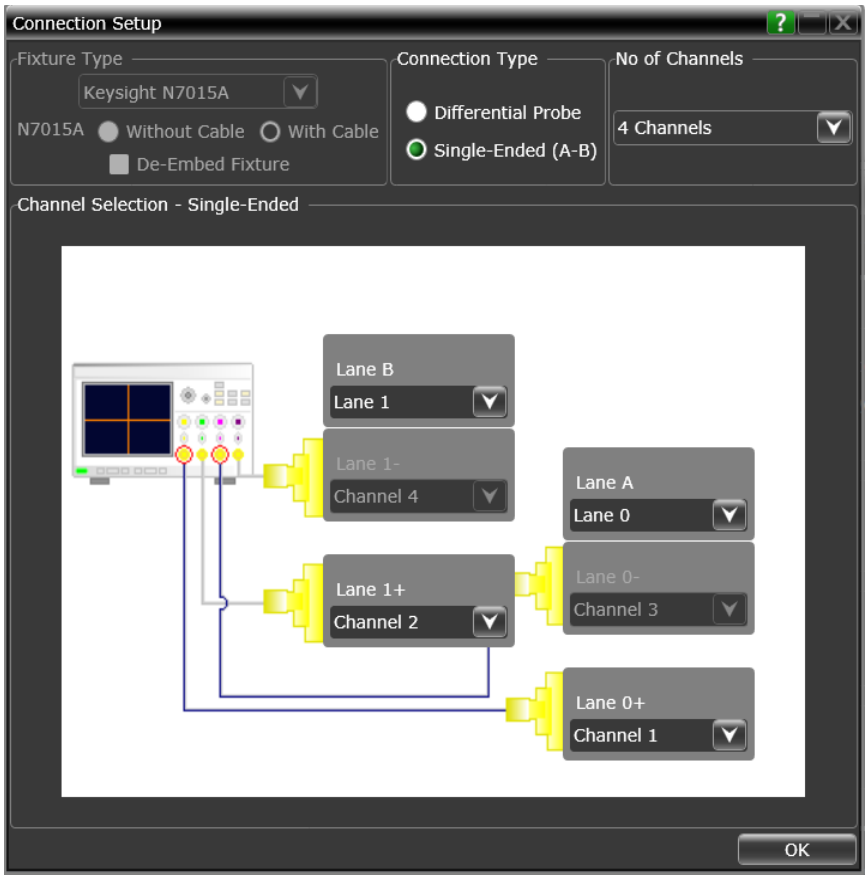
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

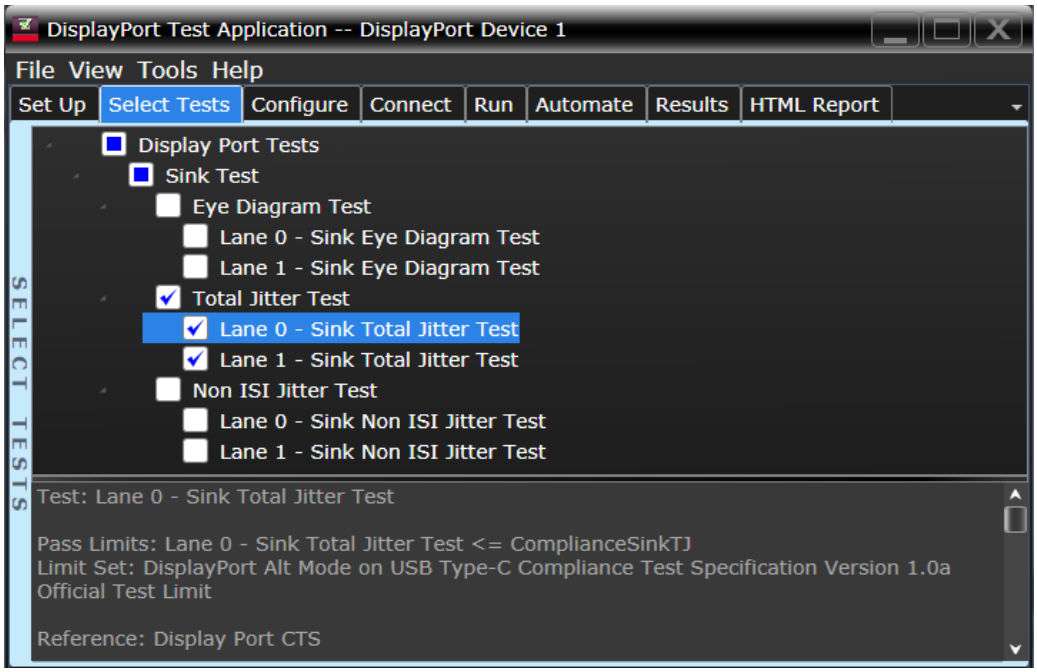
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR3–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR3)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR3–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 204 Total Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	0.580 UI*

* The limits for the Total Jitter are derated by 0.04 UI from 0.62 UI limit in DisplayPort 1.2a Standard.

Table 205 Total Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Sink Non-ISI Jitter Test

Test ID

12220001, 12220002, 12220003, 12220004 – Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

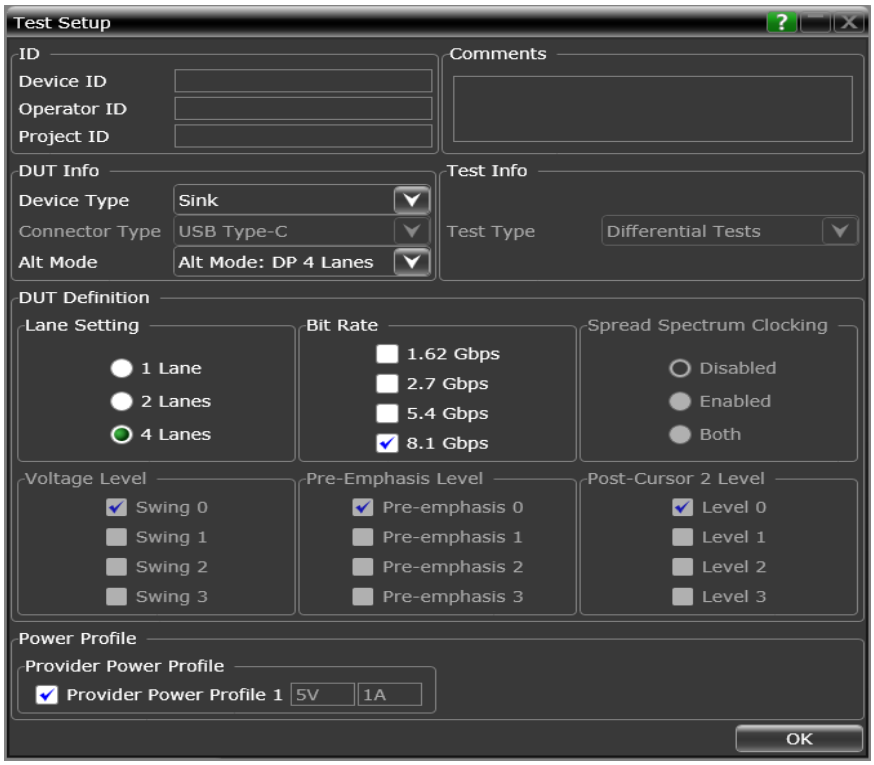
Calculate Non-ISI Jitter using the following equation:

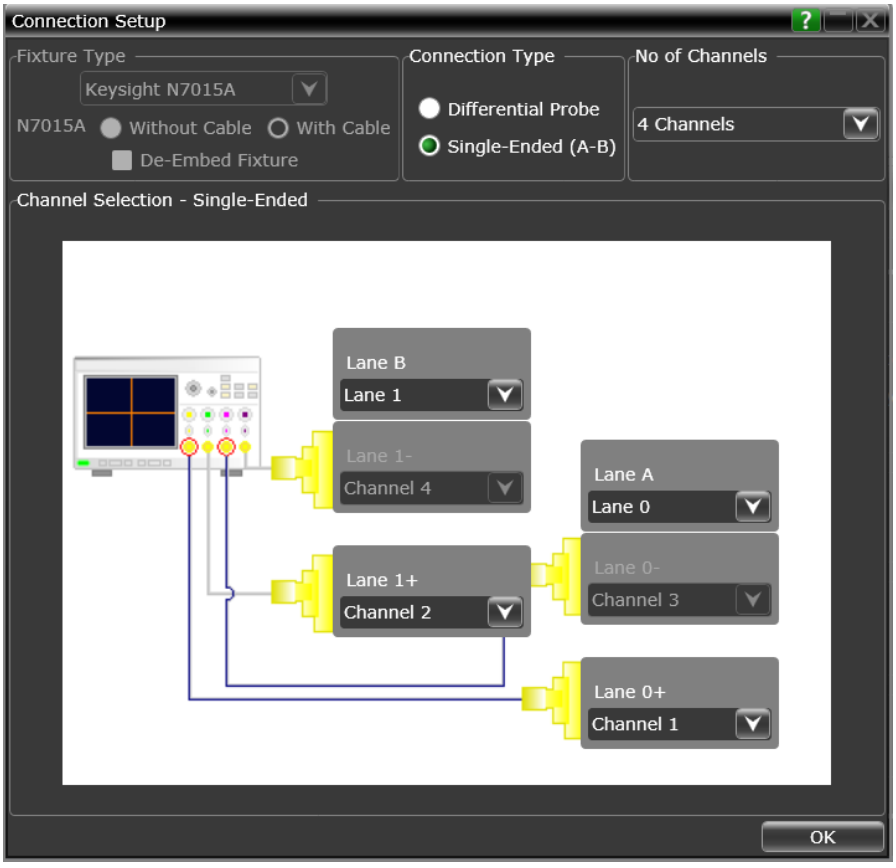
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

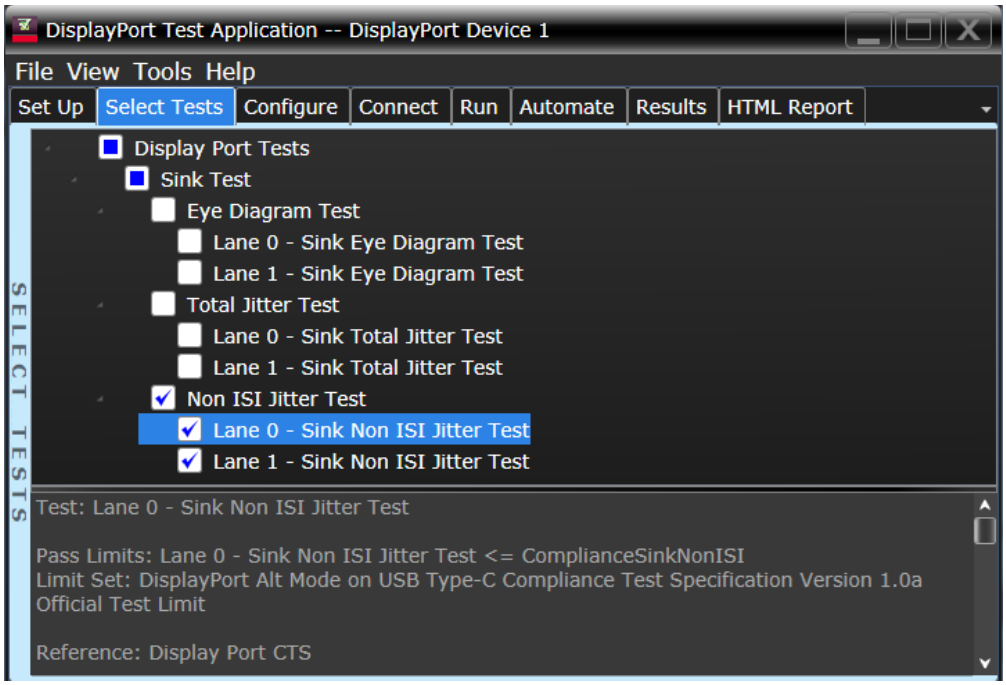
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR3–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR3)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR3–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 206 Non ISI Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	-

Table 207 Non ISI Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

26 DPoC Cable Tests

Overview

The specifications and the conceptual information for the DPoC standard are aligned with that for the DisplayPort 1.4 standard. For more information, refer to "Overview" on page 368.

Setting Up the DisplayPort Compliance Test Application for DPoC Cable Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort Standards with Type-C capability, select the option **DPoC** in the **Test Specification** area.
5. The option **Physical Layer Tests** appears by default in the **Test Selection** area.
6. Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.
7. In the **Type-C Environment Setup** area, select **Enable Type-C Controller** to activate the **DUT Orientation** field and the **Setup Type-C Controller** button. To know about how to configure the Type-C Controller, refer to the *Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help*.
8. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
9. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
10. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
11. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
12. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
13. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
14. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
15. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DPoC Cable Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

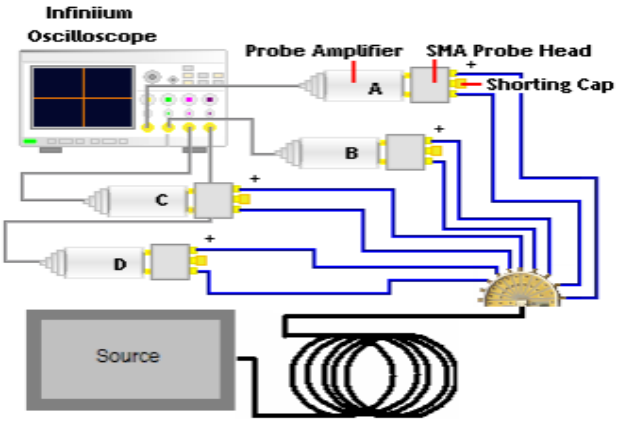


Figure 180 Sample connection diagram for DPoC Cable Tests with Differential Probes

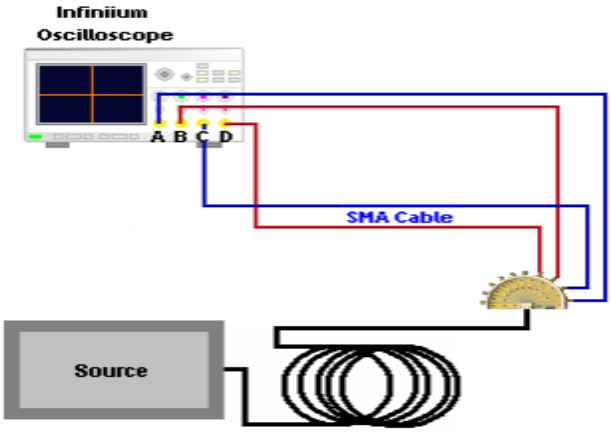


Figure 181 Sample connection diagram for DPoC Cable Tests with Single-Ended Probes

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Cable tests to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in “Test Conditions for <*test-name*>” section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1. In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.
2. On the **Test Setup** window,
   a. Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.
   b. In the **DUT Info** area, select **Device Type** as **Cable**. The **Connector Type** is grayed out. From the drop-down options for **Alt Mode**, select either **Alt Mode: DP 4 Lanes** or **Alt Mode: DP 2 + 2**.
   c. In the **Test Info** area, the **Test Type** is grayed out.
   d. In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.
3. Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1. Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.
2. On the **Connection Setup** window,
   a. The **Fixture Type** area is grayed out.
   b. Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.
   c. In the **Channel Selection** area, assign appropriate channels to lanes.
3. Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of cable tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for DPoC Cable Tests" on page 996 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Cable Eye Diagram Test

Test ID

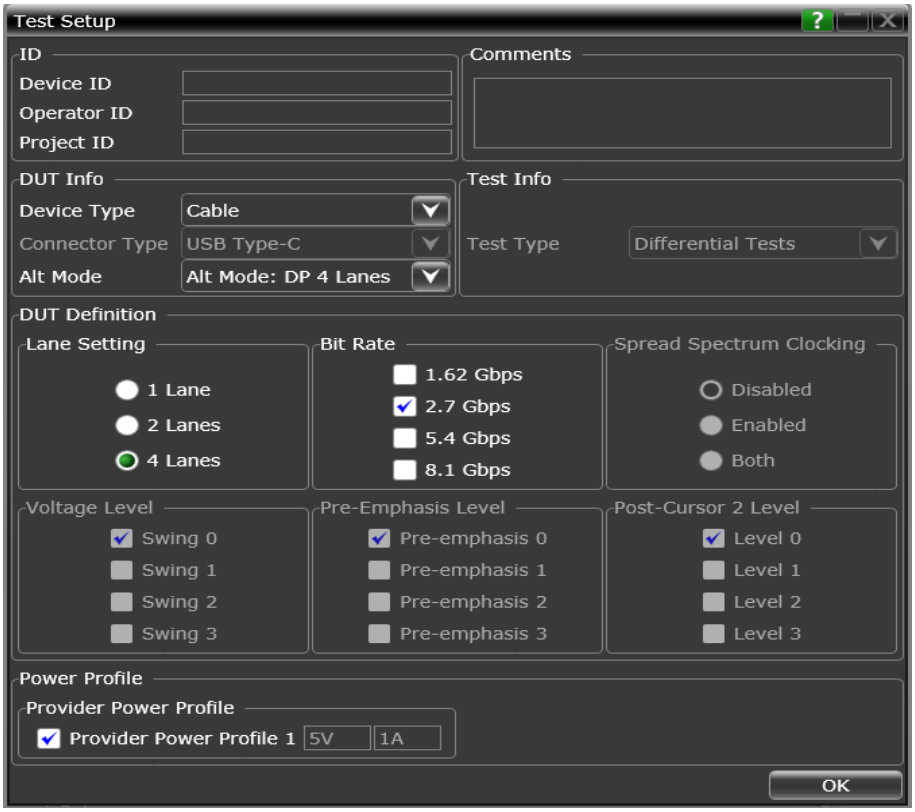
12150001, 12150002, 12150003, 12150004 – Eye Diagram Test

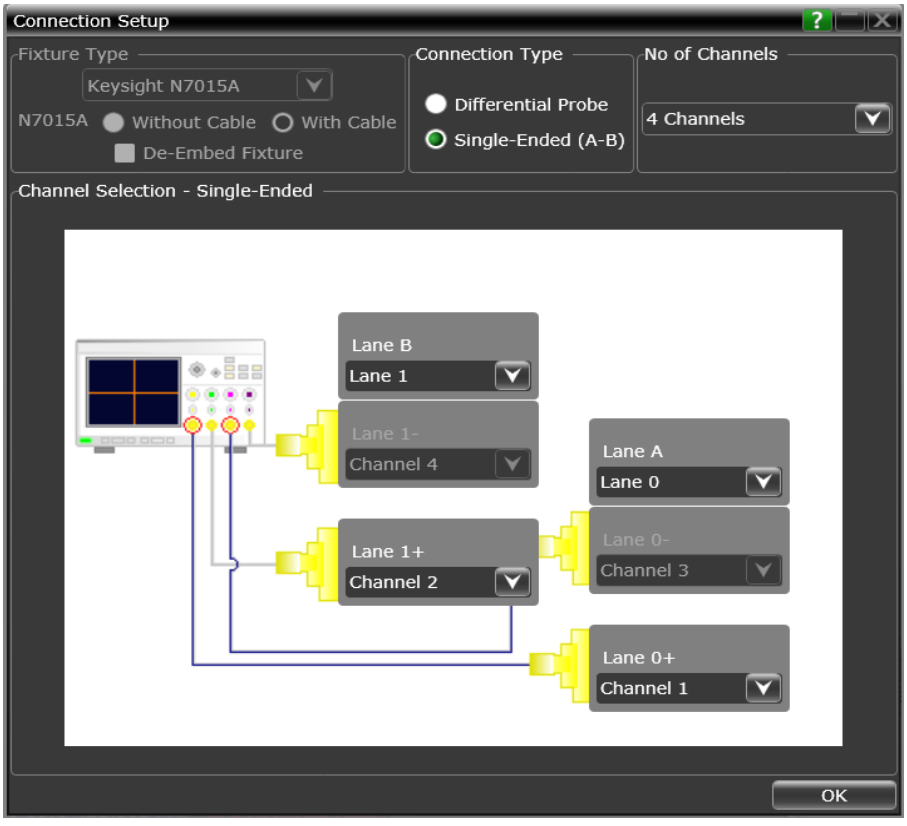
Test Overview

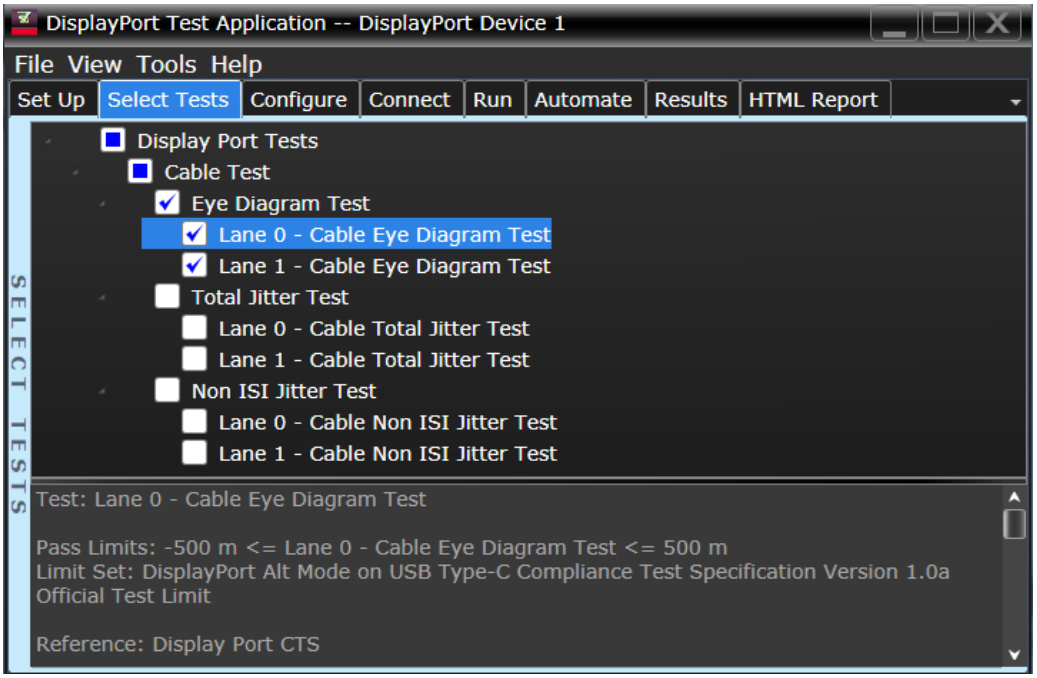
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 82
Crosstalk Signal Parameter	Quarter-rate clock signal (D24.3 pattern) is injected to lanes other than the lane under test. The characteristics of the aggressor signals are: Pattern–D24.3 Bit Rate–(Same as lane under test) Voltage Amplitude–(Same as lane under test) ▪ RBR-400mV ▪ HBR-350mV Edge Rate (20-80)–130ps at TP3


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.

9 Measure the jitter of the eye diagram using the Histogram.
10 Check for any signal trajectories that may have entered into the mask.
11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 208 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 208 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

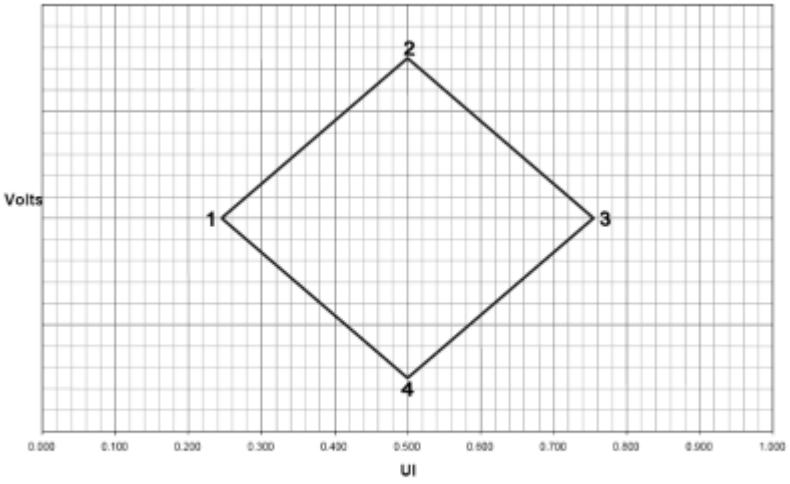


Figure 182 The Cable Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Cable Total Jitter Test

Test ID

12230001, 12230002, 12230003, 12230004 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

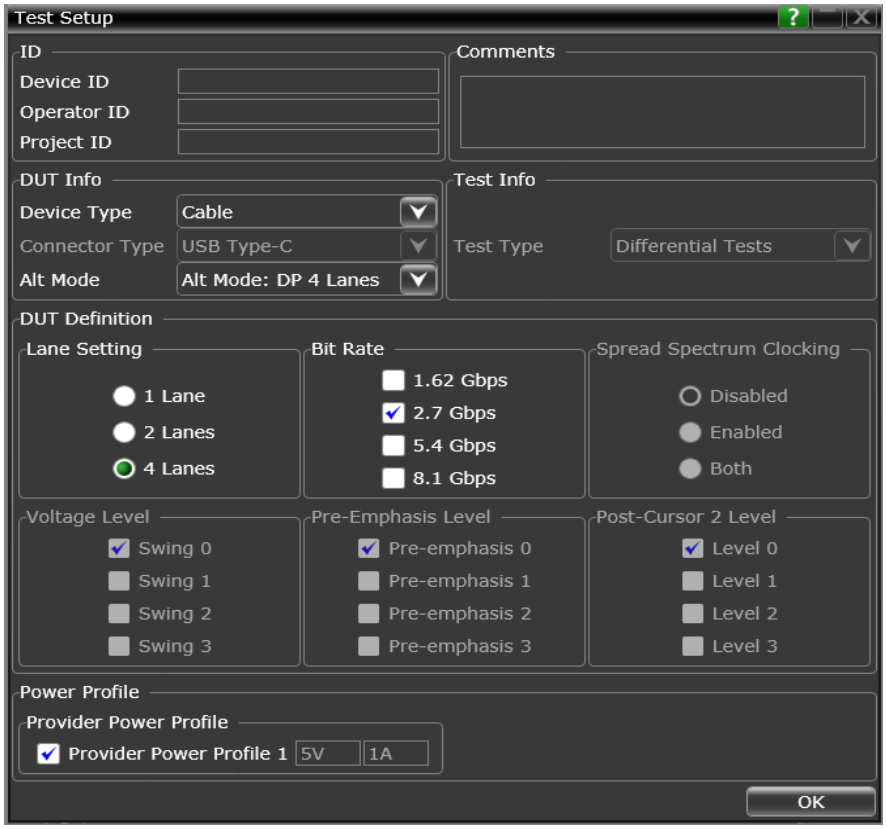
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

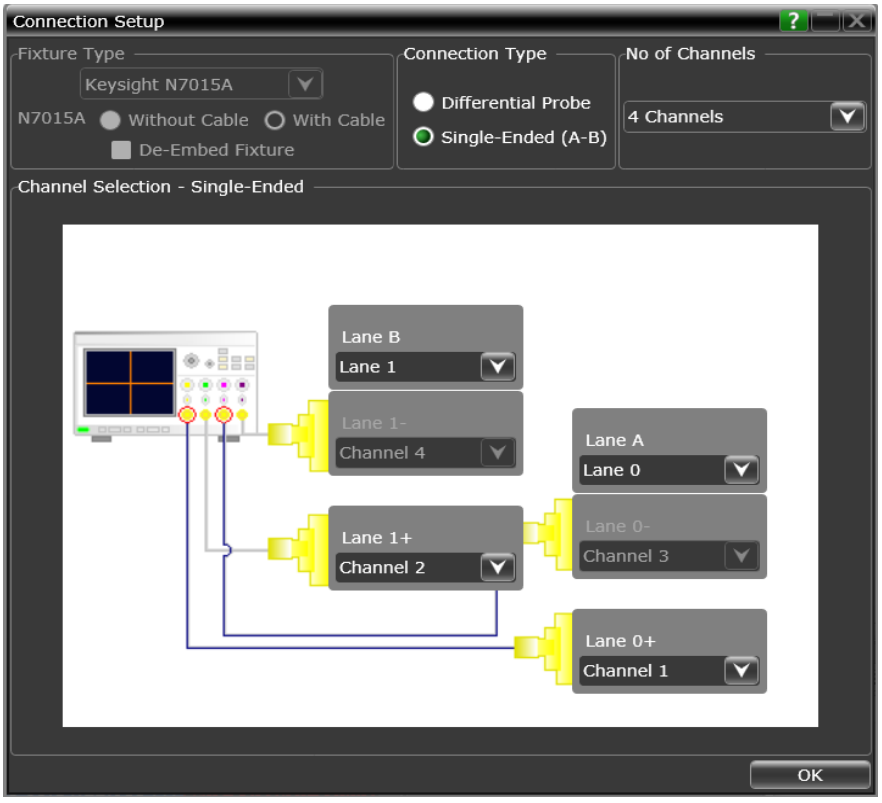
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

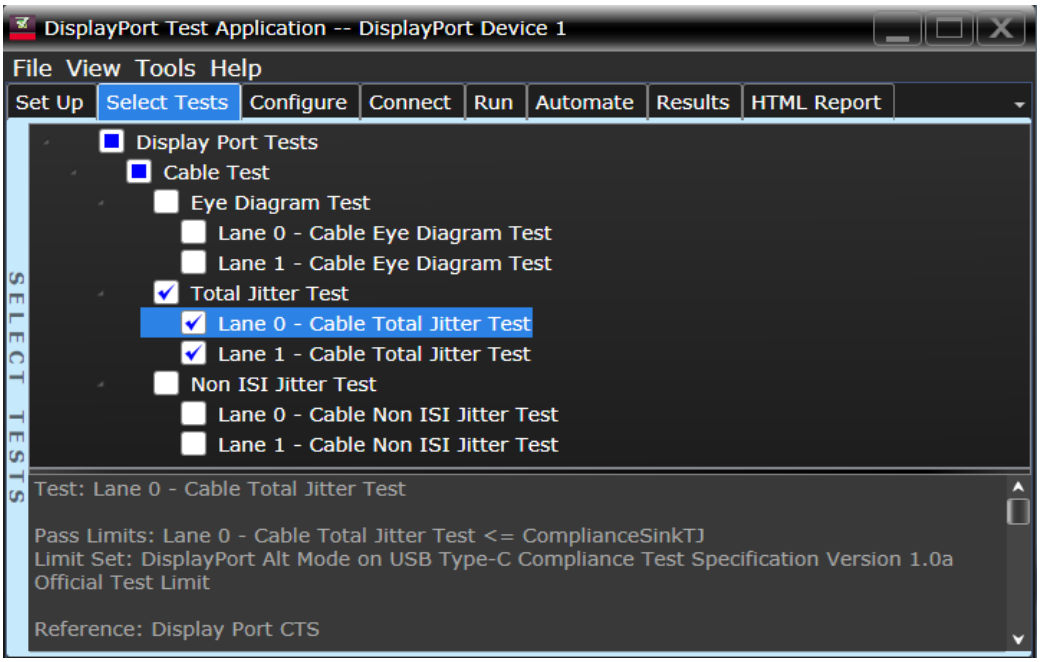
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 82


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 209 Total Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Cable Non-ISI Jitter Test

Test ID

12240001, 12240002, 12240003, 12240004 — Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

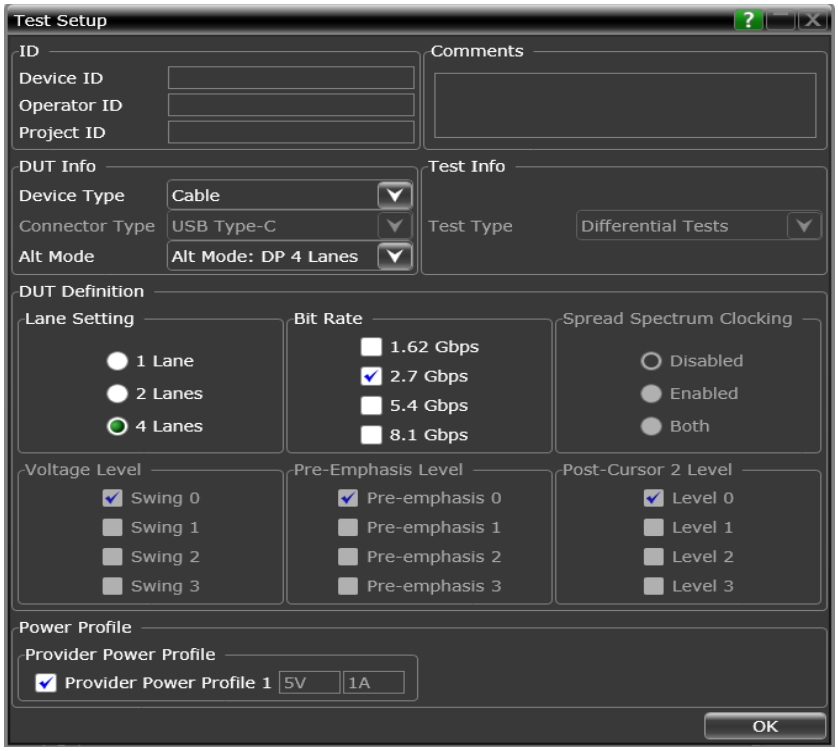
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

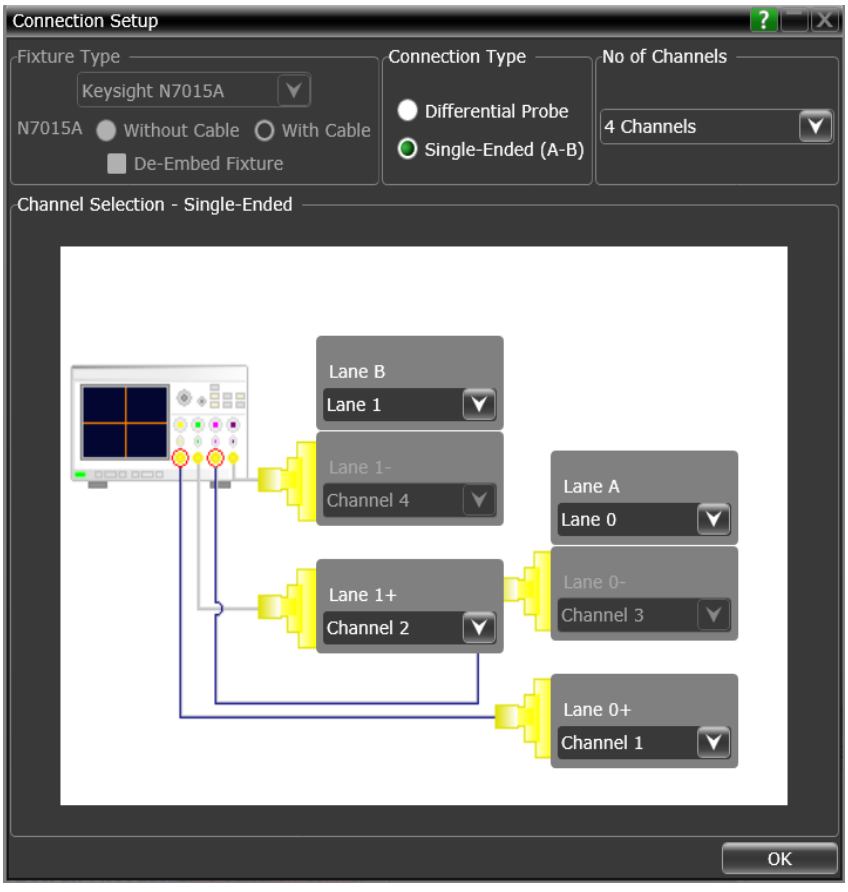
Calculate Non-ISI Jitter using the following equation:

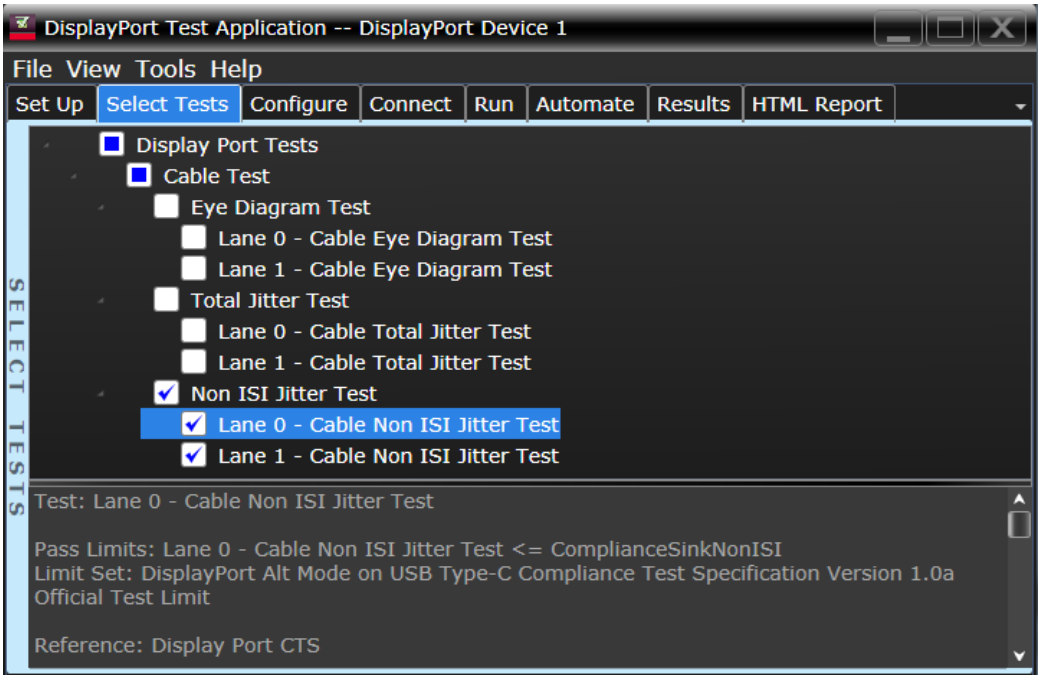
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 82


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Connector Type
USB Type-C
Alt Mode
Alt Mode: DP 4 Lanes
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
Power Profile
Provider Power Profile
Provider Power Profile 1
5V
1A
OK


Connection Setup
Fixture Type
Keysight N7015A
N7015A
Without Cable
With Cable
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Single-Ended
Lane B
Lane 1
Lane 1-
Channel 4
Lane A
Lane 0
Lane 1+
Channel 2
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 210 Non ISI Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non-ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

27 DPoC AUX Channel Tests

Overview

The specifications and the conceptual information for the DPoC standard are aligned with that for the DisplayPort 1.4 standard. For more information, refer to "Overview" on page 388.

Setting Up the DisplayPort Compliance Test Application for DPoC AUX Channel Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort Standards with Type-C capability, select the option **DPoC** in the **Test Specification** area.
5. Select the option **AUX PHY and Inrush Tests** in the **Test Selection** area.
6. In the **Type-C Environment Setup** area, select **Enable Type-C Controller** to activate the **DUT Orientation** field and the **Setup Type-C Controller** button. To know about how to configure the Type-C Controller, refer to the *Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help*.
7. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
8. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
9. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
10. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
11. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
12. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
13. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
14. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Settings for AUX PHY and Inrush Tests

Perform the following steps before you run the Auxiliary Channel and Inrush tests on the source or sink device:

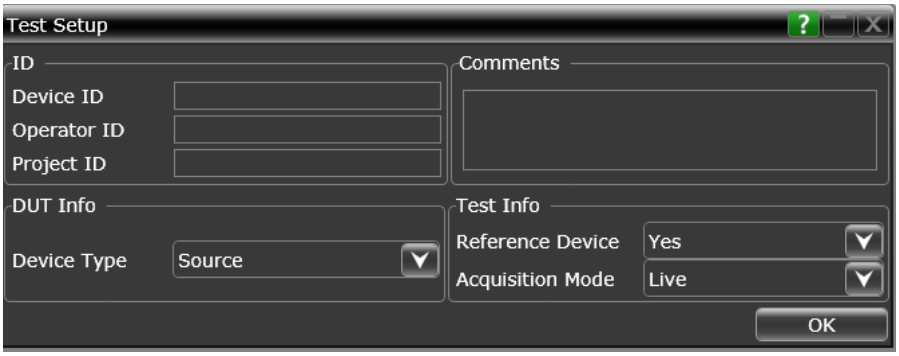
1 Click the **Test Setup** button on the **Set Up** tab to set up for Auxiliary Channel and Inrush tests.

2 From the **Device Type** drop-down options, select either **Source** or **Sink**.

3 From the **Reference Device** drop-down options, select **Yes** if a reference sink/source is attached to device under test during testing.

4 From the **Acquisition Mode** drop-down options, select **Live** if waveform acquisition and analysis will be performed on an online Infiniium Oscilloscope, else select **Offline**.

5 Click **OK** to exit the **Test Setup** window.

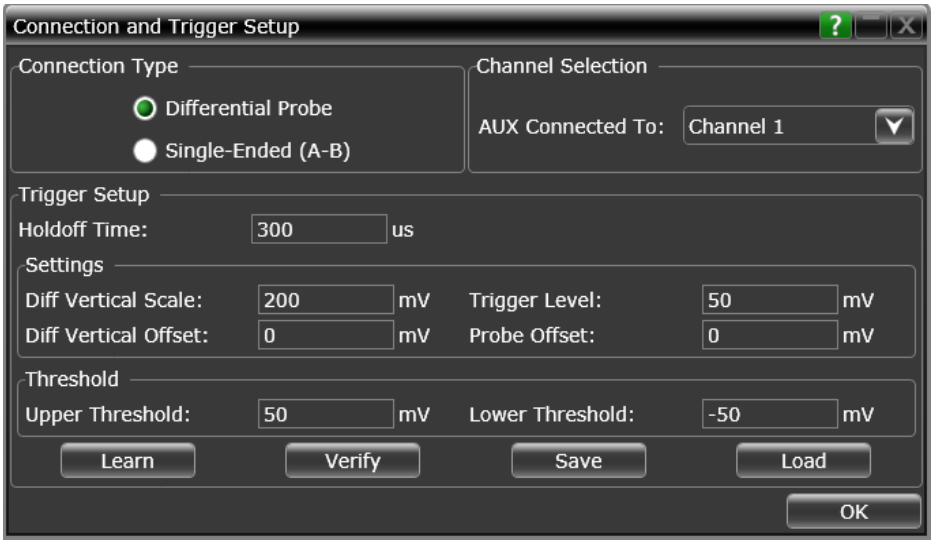


6 Click the **Connection Setup** button that now appears on the **Set Up** tab.

7 On the **Connection and Trigger Setup** window,

a Select either **Differential Probe** or **Single-Ended (A-B)** in the **Connection Type** area, depending on the probe connection you are using.

b From the **AUX Connected To:** drop-down options of the **Channel Selection** area, select the Oscilloscope Channel where the Auxiliary Lane is connected to.



c In the **Trigger Setup** area, define the Oscilloscope parameters to trigger on an Auxiliary signal during testing.

- **Hold Off Time** – The oscilloscope minimum hold off time before triggering the next waveform. Note that any Auxiliary transaction from the source must receive a reply from the sink in 400 us, else such a transaction is considered a timeout. Hold off time, in such cases, represents the minimum idle time before each Aux transaction is initialized. It is defaulted to 300 us which is a safe timing value for most devices tested in the lab. Most devices respond much faster than 300 us.
- **Trigger Level** – The AUX Channel signal level on which to trigger. Note that for a bi-directional signal (where a reference sink is attached), you must set the trigger level such that it crosses both the source command and the sink reply signal. Figure shows correct and incorrect trigger levels.

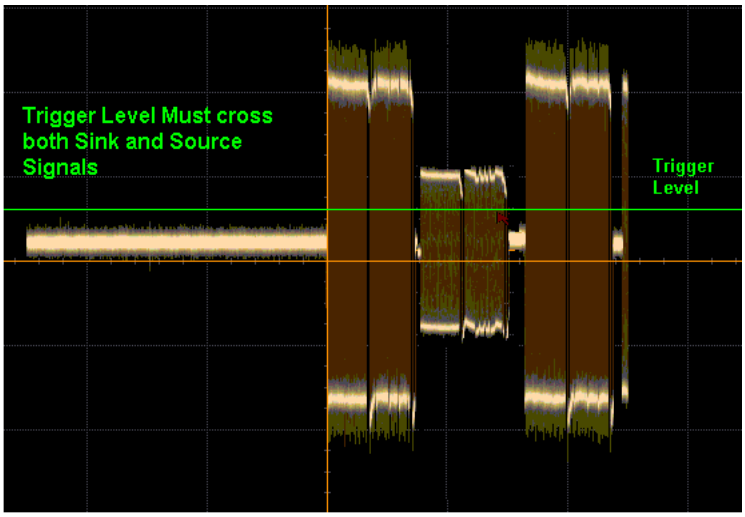


Figure 183 Correct Trigger Level

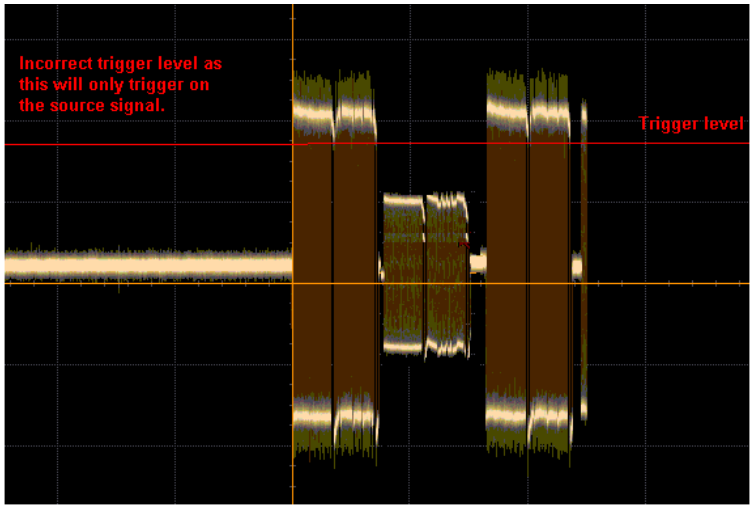


Figure 184 Incorrect Trigger Level

- **Vertical Scale** – The oscilloscope vertical scale. Set the vertical to make sure that all signals are visible on the oscilloscope display.

- **Vertical Offset** – The oscilloscope vertical offset. Set the offset so that the center point is aligned with the center of the oscilloscope display.
- **Upper Threshold/Lower Threshold** – The threshold level of signal must be set properly so that both upper and lower thresholds cross both the source and sink signals when the DUT is attached with a reference sink. The threshold levels are important parameters because they are used for edge detection when decoding a source command from a sink reply.

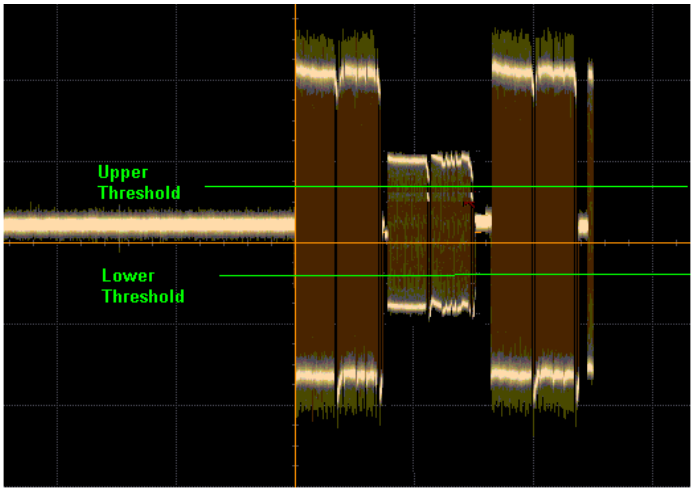
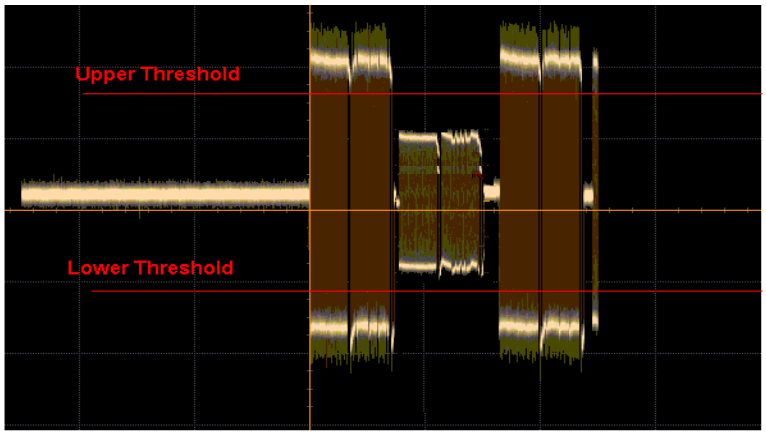


Figure 185 Correct Threshold set



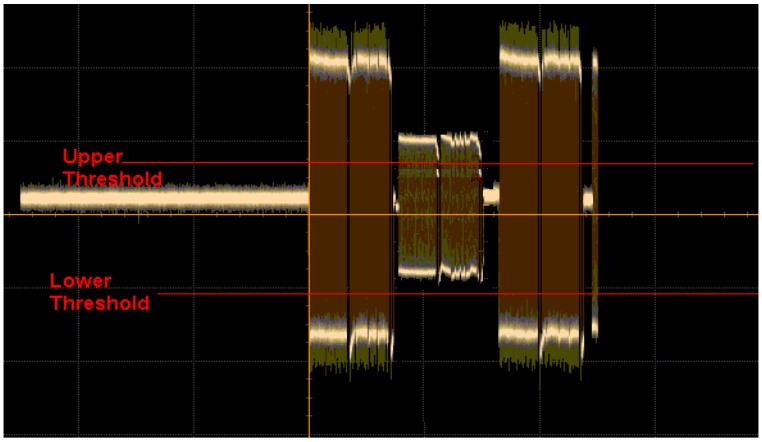


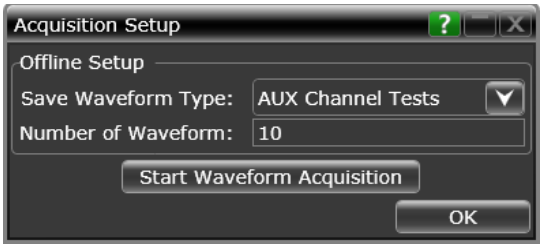
Figure 186 Wrong Thresholds set

- Click the **Learn** button to access the information guide about the trigger setup parameters. However, note that the learning guide may not necessarily work due to variation in the actual Auxiliary signals, owing to different manufacturers. Keysight recommends that you must check to make sure that the parameters are correctly set as previously described.
- Click **Verify** and follow the instructions, if you wish to check the AUX Channel trigger.
- You may **Save** or **Load** the trigger setup configuration as a **.tsf* file.

8 Click **OK** to exit the **Connection and Trigger Setup** window.

9 If you select the option **Offline** for the **Acquisition Mode** in the **Test Setup** window, the **Acquisition Setup** button appears in the **Test Environment Setup** area of the **Set Up** tab.

10 Click the **Acquisition Setup** button to save the waveform files so that you can avoid the manual process to initiate Auxiliary transactions during the time of test runs.



11 On the **Acquisition Setup** window,

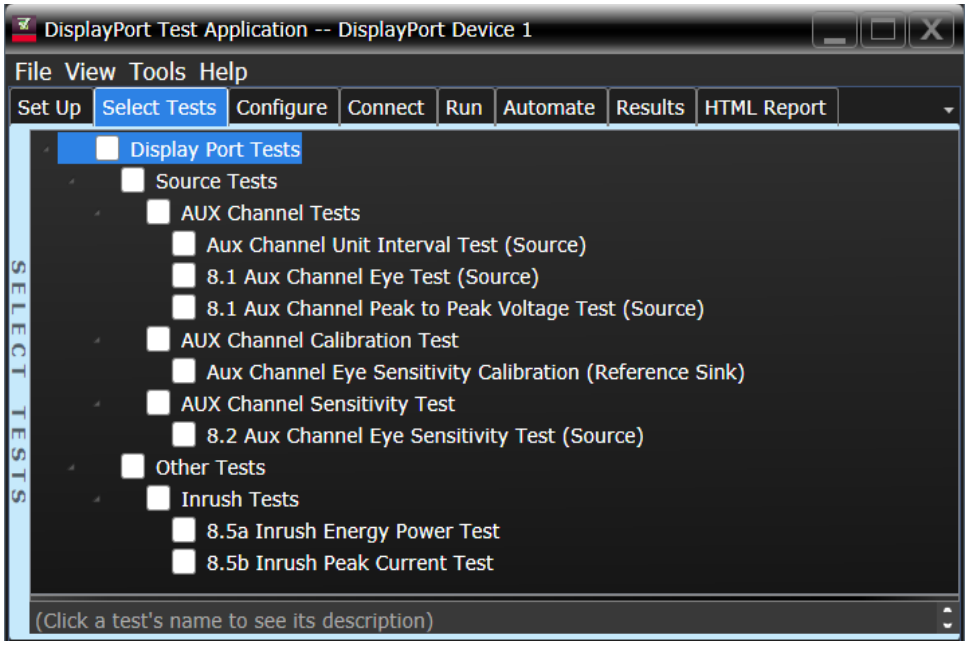
a select the type of waveforms to be saved from the **Save Waveform Type:** drop-down options.

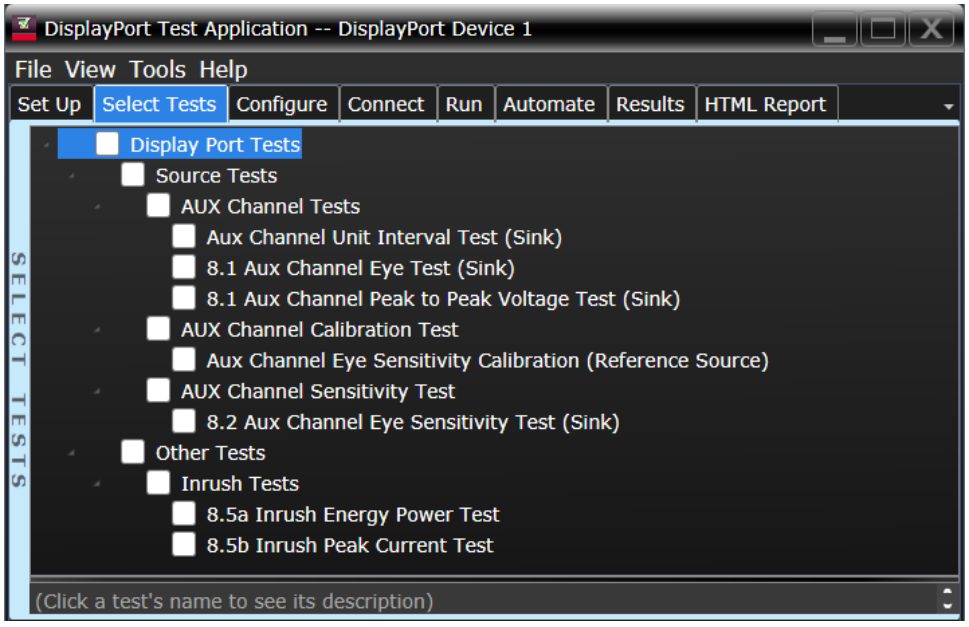
b define the number of waveforms to be saved in the **Number of Waveform:** field.

c Click the **Start Waveform Acquisition** button to start capturing and saving waveforms.

d Click **OK** to return to the **Set Up** tab.

12 Click the **Select Tests** tab where the AUX Channel tests for Source or Sink devices appear.


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Display Port Tests
Source Tests
AUX Channel Tests
Aux Channel Unit Interval Test (Source)
8.1 Aux Channel Eye Test (Source)
8.1 Aux Channel Peak to Peak Voltage Test (Source)
AUX Channel Calibration Test
Aux Channel Eye Sensitivity Calibration (Reference Sink)
AUX Channel Sensitivity Test
8.2 Aux Channel Eye Sensitivity Test (Source)
Other Tests
Inrush Tests
8.5a Inrush Energy Power Test
8.5b Inrush Peak Current Test
(Click a test's name to see its description)


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Display Port Tests
Source Tests
AUX Channel Tests
Aux Channel Unit Interval Test (Sink)
8.1 Aux Channel Eye Test (Sink)
8.1 Aux Channel Peak to Peak Voltage Test (Sink)
AUX Channel Calibration Test
Aux Channel Eye Sensitivity Calibration (Reference Source)
AUX Channel Sensitivity Test
8.2 Aux Channel Eye Sensitivity Test (Sink)
Other Tests
Inrush Tests
8.5a Inrush Energy Power Test
8.5b Inrush Peak Current Test
(Click a test's name to see its description)

Probing/Connection Set Up for AUX Channel Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests. When performing the Source AUX Channel tests, a Reference Sink device is required. Similarly, when performing the Sink AUX Channel tests, a Reference Source device is required.

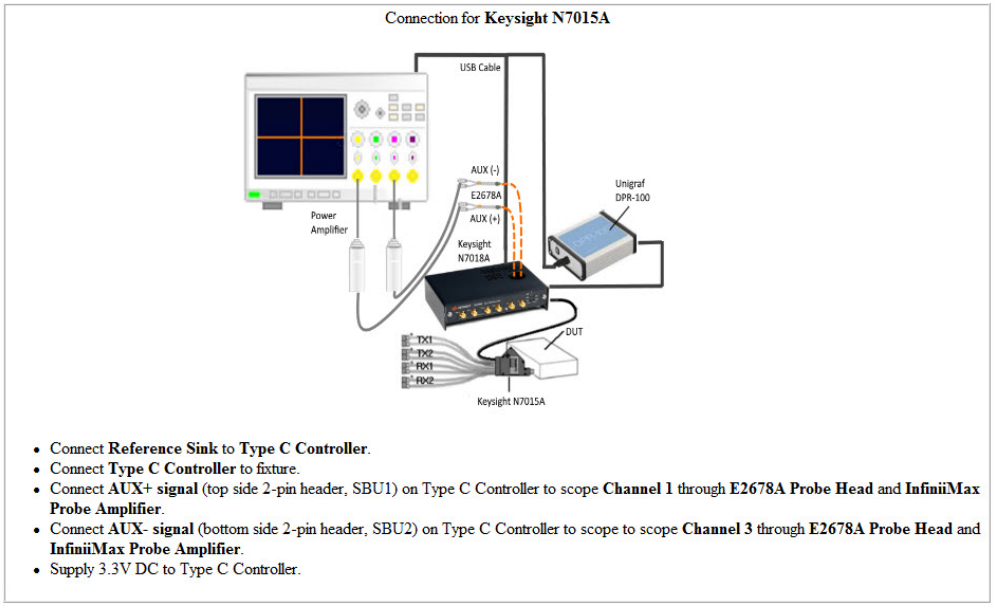


Figure 187 Connection for single-ended source AUX channel tests with DUT connected to a ref-sink

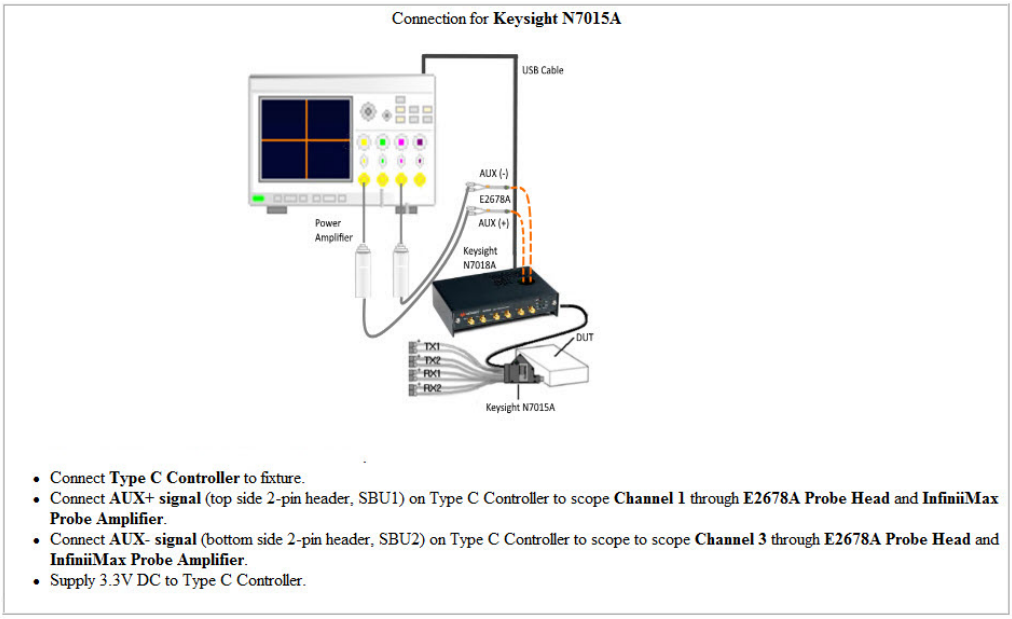


Figure 188 Connection for single-ended source AUX channel tests without DUT connected to a ref-sink

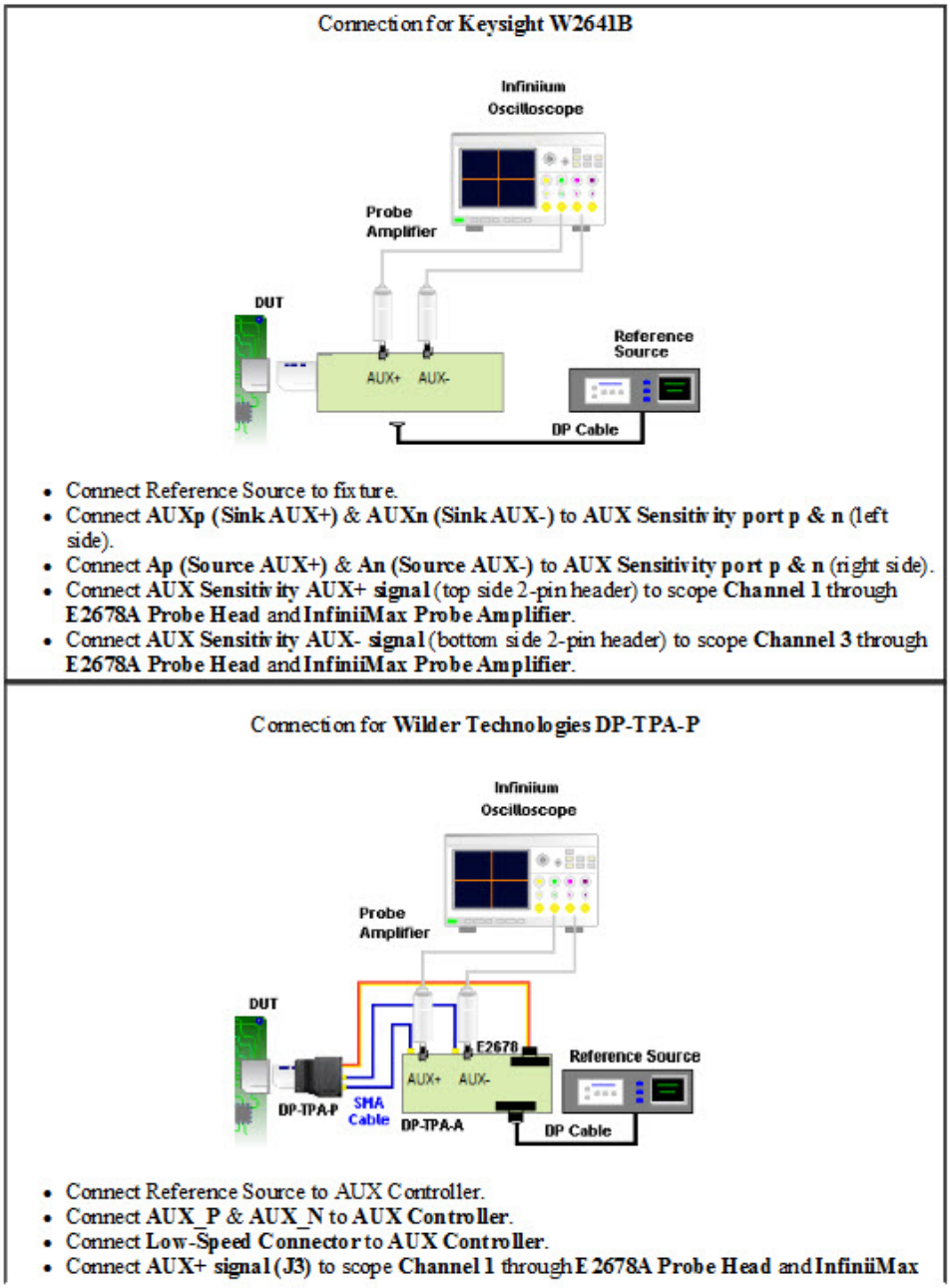


Figure 189 Connection diagram for single-ended sink AUX channel tests with a ref-source

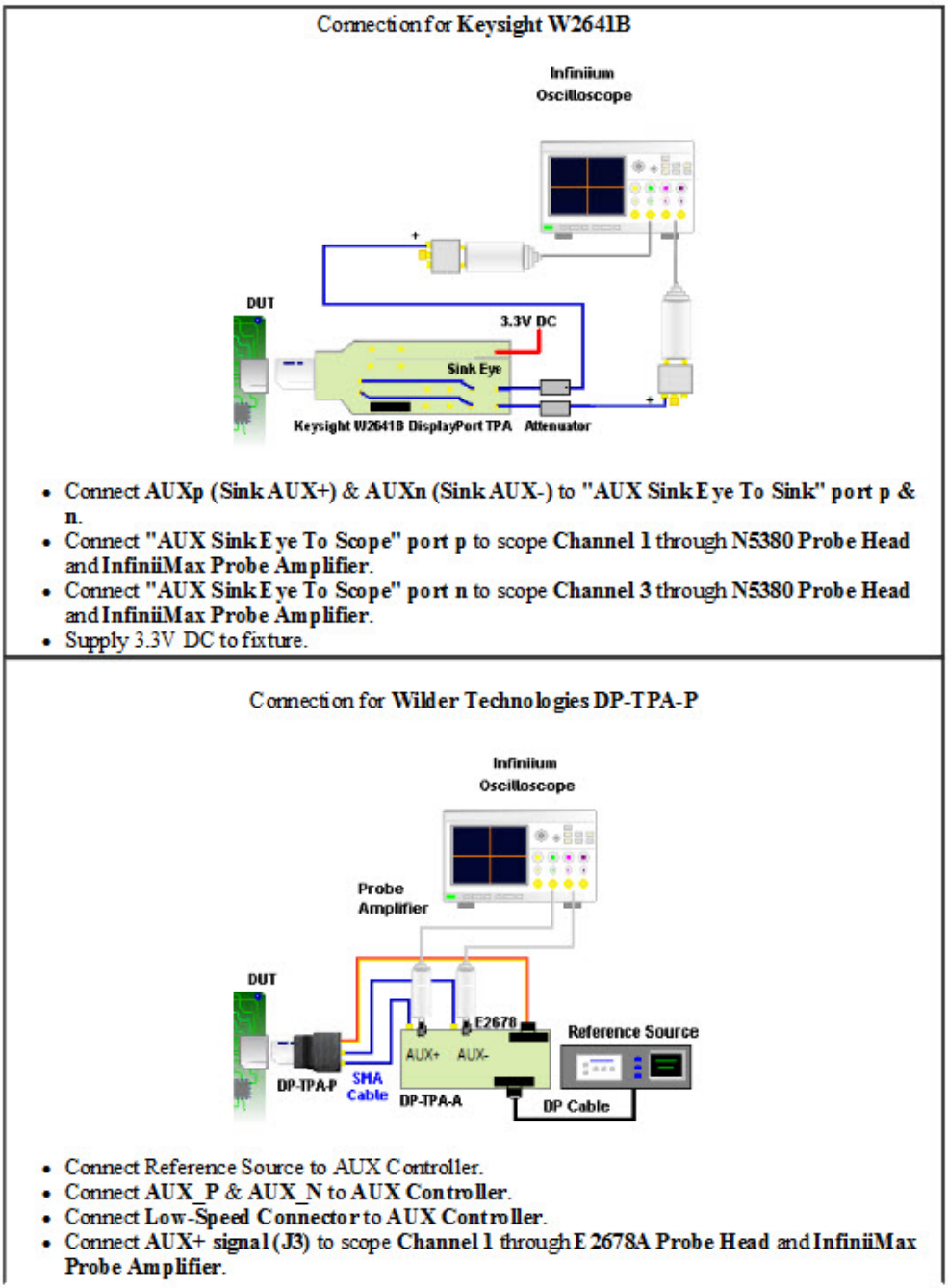


Figure 190 Connection diagram for single-ended sink AUX channel tests without a ref-source

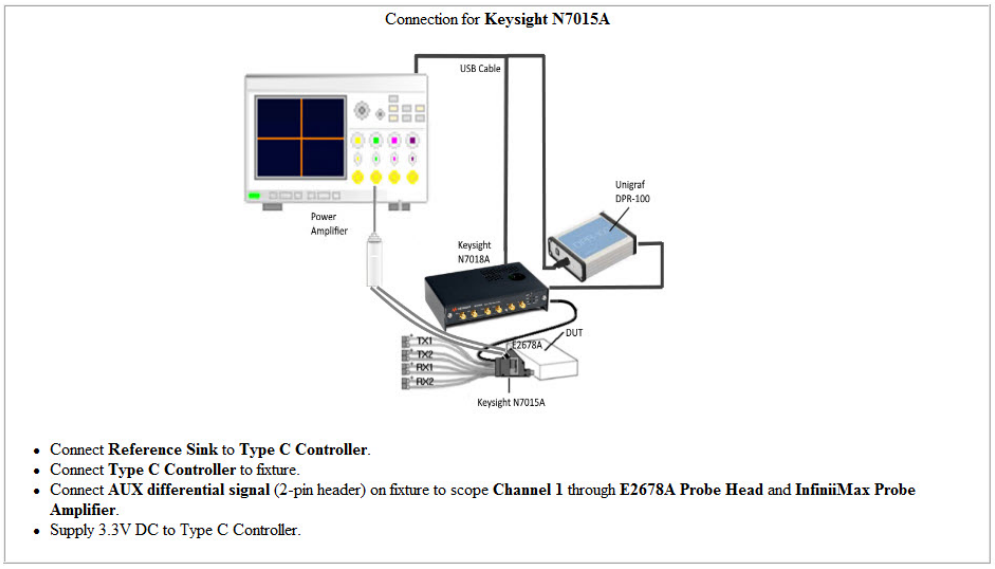


Figure 191 Connection for differential source AUX channel tests with DUT connected to a ref-sink

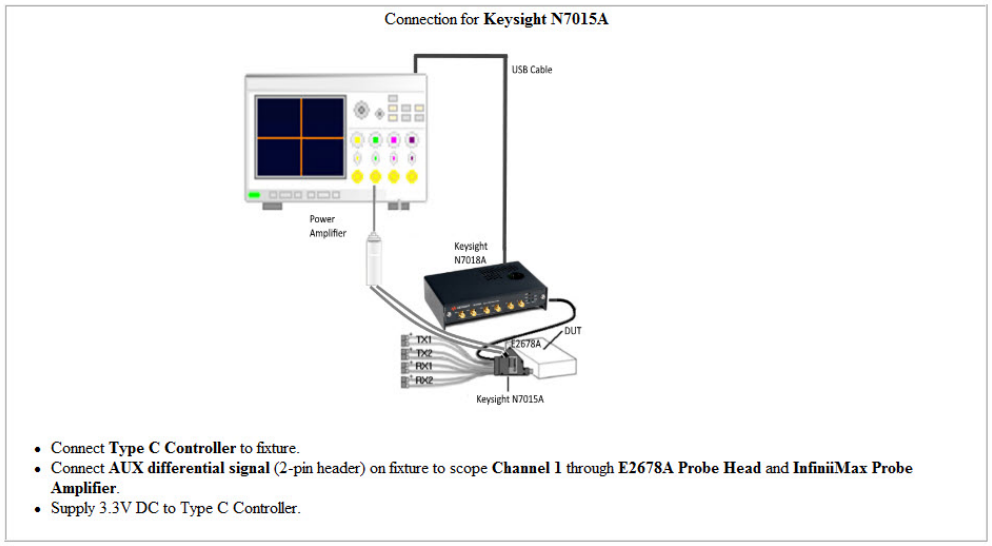


Figure 192 Connection for differential source AUX channel tests without DUT connected to a ref-sink

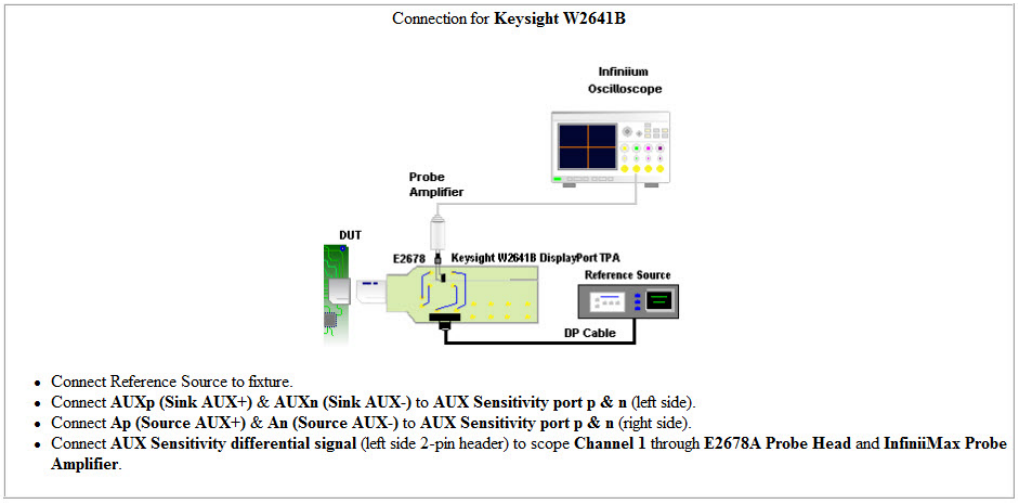


Figure 193 Connection diagram for differential sink AUX channel tests with a ref-source

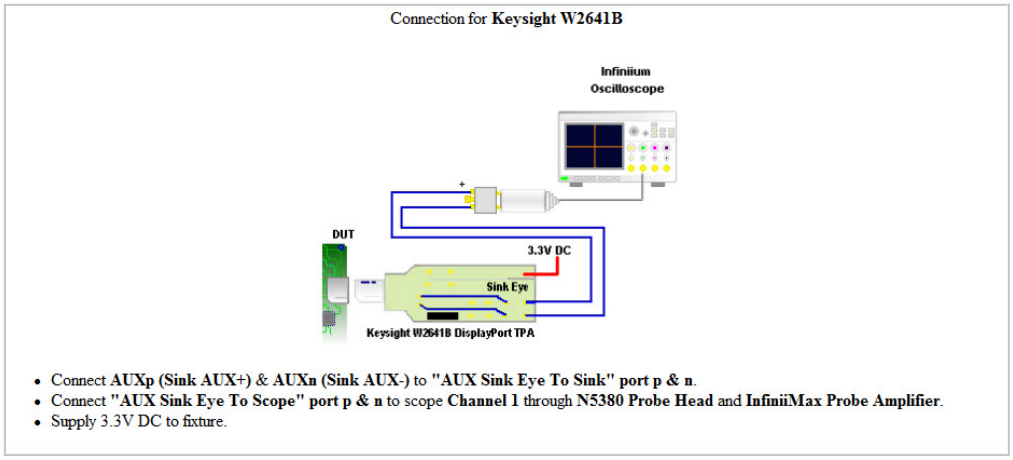


Figure 194 Connection diagram for differential sink AUX channel tests without a ref-source

AUX Channel Unit Interval Test

Test ID

125000 – AUX Channel Unit Interval Test (Source)

125010 – AUX Channel Unit Interval Test (Sink)

Test Overview

The objective of the test is to evaluate the AUX Channel waveform, ensuring that the overall variation of the Manchester transaction Unit Interval stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Set up the parameter of the measurement trend:

   a Set up the Unit Interval measurement for the differential AUX Channel signal.

   b Set up the frequency measurement for the Clock signal.

   c Set up the measurement trend.

6 Set up the waveform Histogram on the measurement trend:

   a Initialize AUX Channel transactions and acquire the differential AUX Channel signal.

   b Identify the first and the last points for the desired transaction.

   c Zoom-in on the desired transaction.

   d Set up the Vertical Waveform Histogram on the measurement trend within the desired transaction.

   e Obtain the measurement for the mean, maximum and minimum values of the waveform Histogram.

7 Repeat step 6 ten times.

8 Report the measurement results.

PASS Condition

Manchester Transaction Unit Interval (UI_{MAN}):

Minimum = 0.4 µsec

Maximum = 0.6 µsec

Test References

See:

- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.4.2, Table 3-4*

Expected/Observable Results

The measured unit interval for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Test

Test ID

125001 – AUX Channel Eye Test (Source)

125011 – AUX Channel Eye Test (Sink)

Test Overview

The objective of this test is to evaluate the transmitter AUX Channel waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

7 Set up the waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

8 Set up the parameters for the Mask Test.

   a Load the eye mask based on the settings in the Configuration Variable.

   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

   c Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.

9 Check for any signal trajectories entering into the mask.

10 Report the measurement results.

PASS Condition

PASS Value = 290mV_diff_pp or higher

FAIL Value = lower than 290mV_diff_pp

Table 211 Eye Mask Vertices for AUX Channel for Manchester Transactions

Mask Point	Time (from EYE Center)	Minimum Voltage Value at Six Vertices (mV)
1	-185ns	0
2	-135ns	145
3	135ns	145
4	185ns	0
5	135ns	-145
6	-135ns	-145

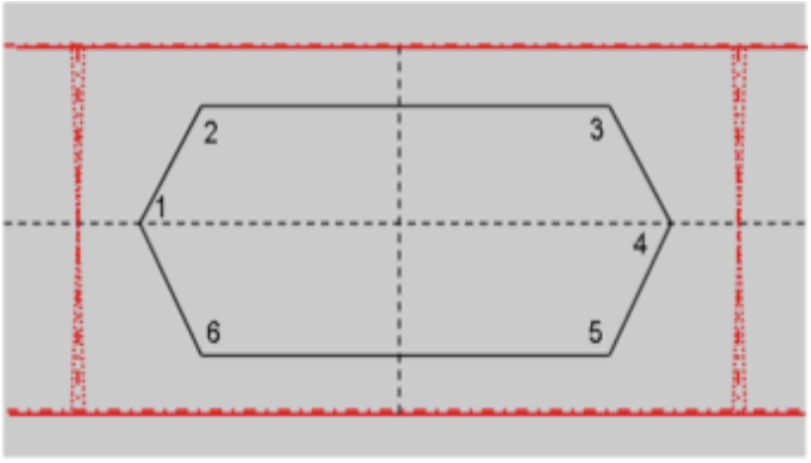


Figure 195 AUX Channel EYE Mask for Manchester Transactions

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.1*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.4.2.5, Figure 3-18 and Table 3-5*

Expected/Observable Results

The measured eye diagram for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

AUX Channel Peak-to-Peak Voltage Test

Test ID

125002 – AUX Channel Peak-to-Peak Voltage Test (Source)

125012 – AUX Channel Peak-to-Peak Voltage Test (Sink)

Test Overview

The objective of the test is to evaluate the transmitter AUX Channel Waveform, ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

a Enable measurement of all edges to obtain a statistical value of the measurement.

b Set up the measurement threshold.

c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

7 Set up the horizontal waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

8 If you have selected the “AUX Channel Eye Test” under the **Select Tests** tab of the compliance application:

a Set up the parameter of the Mask Test:

i Load the eye mask based on the settings in the Configuration Variable.

ii Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

iii Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.

b Check for any signal trajectories entering into the mask.

9 Report the measurement results.

PASS Condition

Table 212 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage at a transmitting device ($V_{AUX\text{-}DIFFp\text{-}p}$)	0.29V	1.38V

Test References

See:

- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.4.2, Table 3-4*

Expected/Observable Results

The measured peak-to-peak voltage for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Calibration Test

Test ID

125021 – AUX Channel Eye Sensitivity Calibration (Reference Sink)

125031 – AUX Channel Eye Sensitivity Calibration (Reference Source)

Test Overview

The objective of this test is to calibrate the peak-to-peak voltage of the transmitter AUX Channel waveform by reference device (reference source or reference sink), ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.

2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

4 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

5 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

6 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

7 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

8 Set up the waveform Histogram on the AUX Channel eye diagram:

   a Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.

   b Set up the vertical waveform Histogram of width 0.6 UI at the center of the AUX Channel eye diagram.

   c Measure the V_{TOP} and V_{BASE} using the waveform Histogram mean value.

9 Repeat Step 8 three times.

10 Report the measurement results.

PASS Condition

Table 213 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage for AUX Channel Eye Sensitivity	0.24V	0.28V

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.4.2, Table 3-4*

Expected/Observable Results

The measured peak-to-peak voltage for the AUX Channel signal by reference device (reference source or reference sink) shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Test

Test ID

125041 – AUX Channel Eye Sensitivity Test (Source)

125051 – AUX Channel Eye Sensitivity Test (Sink)

Test Overview

The objective of the test is to evaluate the sensitivity to the AUX Channel Eye Opening of the DUT as per the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.
2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.
3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery.
5 Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.
6 Check if the reference device could detect the transaction or not.
7 Decode the AUX Channel signal and check whether the transaction passed or failed.
8 Report the measurement results.

PASS Condition

Determine whether the AUX Channel communication is successful. For example, the Transmitter DUT sends an AUX Request to the Reference Receiver. The Reference Receiver acknowledges and the Transmitter DUT responds to the to indicate that the acknowledgment was successfully received.

PASS = No errors observed in the response

FAIL = One or more errors observed

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.4.2, Table 3-4*

Expected/Observable Results

The measured AUX Channel transaction shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

28 DPoC Inrush Tests

Overview

The specifications and the conceptual information for the DPoC standard are aligned with that for the DisplayPort 1.4 standard. For more information, refer to "Overview" on page 408.

Setting Up the DisplayPort Compliance Test Application for DPoC Inrush Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort Standards with Type-C capability, select the option **DPoC** in the **Test Specification** area.
5. Select the option **AUX PHY and Inrush Tests** in the **Test Selection** area.
6. In the **Type-C Environment Setup** area, select **Enable Type-C Controller** to activate the **DUT Orientation** field and the **Setup Type-C Controller** button. To know about how to configure the Type-C Controller, refer to the *Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help*.
7. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
8. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
9. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
10. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
11. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
12. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
13. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
14. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Refer to "Settings for AUX PHY and Inrush Tests" on page 1014 for instructions on setting the DPoC InRush tests.

Inrush Energy Power Test

Test ID

127000 – Inrush Energy Power Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush energy power measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Energy $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 13.5$ Amps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.5*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.2.3*

Expected/Observable Results

The measured worst case inrush energy power for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Inrush Peak Current Test

Test ID

127001 – Inrush Peak Current Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush peak current measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Energy $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 13.5$ Amps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.5*
- *VESA DisplayPort (DP) Standard Version 1.4, Section 3.2.3*

Expected/Observable Results

The measured worst case inrush peak current for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

29 CTLE Optimization Tests

Overview

The objective of the CTLE Optimization is to sweep the DC Gain of the CTLE model defined by the DisplayPort specification from 0dB to 9dB to find the optimum CTLE DC Gain.

The optimized CTLE DC gain is obtained based on the CTLE DC Gain that generates the eye diagram with maximum eye height. If there are two values of DC Gain with the same eye height, select the one with the greater eye width.

On the DisplayPort Compliance Test Application, these tests are available only for the 1.4 and DPoC standards.

Setting Up the DisplayPort Compliance Test Application for CTLE Optimization Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 In the **Test Specification** area, either select the option **1.4** to test for compliance with DisplayPort 1.4 Standards or select the option **DPoC** to test for compliance with DisplayPort Standards with Type-C capability.

5 Select the option **Test Tools** in the **Test Selection** area. The option **CTLE Optimization** appears by default.

6 If you select **DPoC**, the **Type-C Environment Setup** area appears. In this area, select **Enable Type-C Controller** to activate the **DUT Orientation** field and the **Setup Type-C Controller** button. To know about how to configure the Type-C Controller, refer to the *Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help*.

7 If required for either of the standards, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

8 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

9 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

10 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

11 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

12 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

13 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

14 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for CTLE Optimization Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

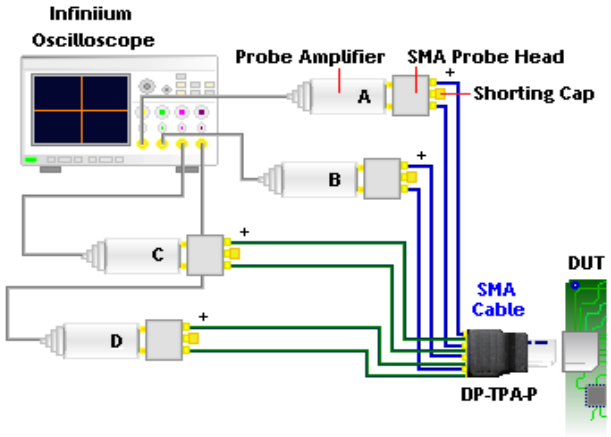


Figure 196 Sample connection diagram for DisplayPort CTLE Optimization Tests with Differential Probes

Configuration for Test Setup and Connection Setup

Configuring the Test Setup window

- For **Test Specification** selected as **1.4**, refer to "Configuring the Test Setup window" on page 257.
- For **Test Specification** selected as **DPoC**, refer to "Configuring the Test Setup window" on page 874.

Configuring the Connection Setup window

- For **Test Specification** selected as **1.4**, refer to "Configuring the Connection Setup window" on page 257.
- For **Test Specification** selected as **DPoC**, refer to "Configuring the Connection Setup window" on page 874.

After configuring the **Test Setup** and **Connection Setup** to run the CTLE tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for CTLE Optimization Tests" on page 1044 to complete the task flow for DUT setup along with configuring the Compliance Application to run each test.

CTLE Optimization with Cable Model and with no Cable Model Tests

Test ID

For Standard DP Pattern (HBR2CPAT):

- 12910011, 12910012, 12910013, 12910014 – CTLE Optimization with Cable Model (TP3_EQ) (0dB)
- 12910021, 12910022, 12910023, 12910024 – CTLE Optimization with Cable Model (TP3_EQ) (-1dB)
- 12910031, 12910032, 12910033, 12910034 – CTLE Optimization with Cable Model (TP3_EQ) (-2dB)
- 12910041, 12910042, 12910043, 12910044 – CTLE Optimization with Cable Model (TP3_EQ) (-3dB)
- 12910051, 12910052, 12910053, 12910054 – CTLE Optimization with Cable Model (TP3_EQ) (-4dB)
- 12910061, 12910062, 12910063, 12910064 – CTLE Optimization with Cable Model (TP3_EQ) (-5dB)
- 12910071, 12910072, 12910073, 12910074 – CTLE Optimization with Cable Model (TP3_EQ) (-6dB)
- 12910081, 12910082, 12910083, 12910084 – CTLE Optimization with Cable Model (TP3_EQ) (-7dB)
- 12910091, 12910092, 12910093, 12910094 – CTLE Optimization with Cable Model (TP3_EQ) (-8dB)
- 12920011, 12920012, 12920013, 12920014 – CTLE Optimization with No Cable Model (TP3_EQ) (0dB)
- 12920021, 12920022, 12920023, 12920024 – CTLE Optimization with No Cable Model (TP3_EQ) (-1dB)
- 12920031, 12920032, 12920033, 12920034 – CTLE Optimization with No Cable Model (TP3_EQ) (-2dB)
- 12920041, 12920042, 12920043, 12920044 – CTLE Optimization with No Cable Model (TP3_EQ) (-3dB)
- 12920051, 12920052, 12920053, 12920054 – CTLE Optimization with No Cable Model (TP3_EQ) (-4dB)
- 12920061, 12920062, 12920063, 12920064 – CTLE Optimization with No Cable Model (TP3_EQ) (-5dB)
- 12920071, 12920072, 12920073, 12920074 – CTLE Optimization with No Cable Model (TP3_EQ) (-6dB)
- 12920081, 12920082, 12920083, 12920084 – CTLE Optimization with No Cable Model (TP3_EQ) (-7dB)
- 12920091, 12920092, 12920093, 12920094 – CTLE Optimization with No Cable Model (TP3_EQ) (-8dB)

For Arbitrary Pattern:

- 13910011, 13910012, 13910013, 13910014 – CTLE Optimization with Cable Model (TP3_EQ) (0dB)
- 13910021, 13910022, 13910023, 13910024 – CTLE Optimization with Cable Model (TP3_EQ) (-1dB)
- 13910031, 13910032, 13910033, 13910034 – CTLE Optimization with Cable Model (TP3_EQ) (-2dB)
- 13910041, 13910042, 13910043, 13910044 – CTLE Optimization with Cable Model (TP3_EQ) (-3dB)

- 13910051, 13910052, 13910053, 13910054 – CTLE Optimization with Cable Model (TP3_EQ) (-4dB)
- 13910061, 13910062, 13910063, 13910064 – CTLE Optimization with Cable Model (TP3_EQ) (-5dB)
- 13910071, 13910072, 13910073, 13910074 – CTLE Optimization with Cable Model (TP3_EQ) (-6dB)
- 13910081, 13910082, 13910083, 13910084 – CTLE Optimization with Cable Model (TP3_EQ) (-7dB)
- 13910091, 13910092, 13910093, 13910094 – CTLE Optimization with Cable Model (TP3_EQ) (-8dB)
- 13920011, 13920012, 13920013, 13920014 – CTLE Optimization with No Cable Model (TP3_EQ) (0dB)
- 13920021, 13920022, 13920023, 13920024 – CTLE Optimization with No Cable Model (TP3_EQ) (-1dB)
- 13920031, 13920032, 13920033, 13920034 – CTLE Optimization with No Cable Model (TP3_EQ) (-2dB)
- 13920041, 13920042, 13920043, 13920044 – CTLE Optimization with No Cable Model (TP3_EQ) (-3dB)
- 13920051, 13920052, 13920053, 13920054 – CTLE Optimization with No Cable Model (TP3_EQ) (-4dB)
- 13920061, 13920062, 13920063, 13920064 – CTLE Optimization with No Cable Model (TP3_EQ) (-5dB)
- 13920071, 13920072, 13920073, 13920074 – CTLE Optimization with No Cable Model (TP3_EQ) (-6dB)
- 13920081, 13920082, 13920083, 13920084 – CTLE Optimization with No Cable Model (TP3_EQ) (-7dB)
- 13920091, 13920092, 13920093, 13920094 – CTLE Optimization with No Cable Model (TP3_EQ) (-8dB)

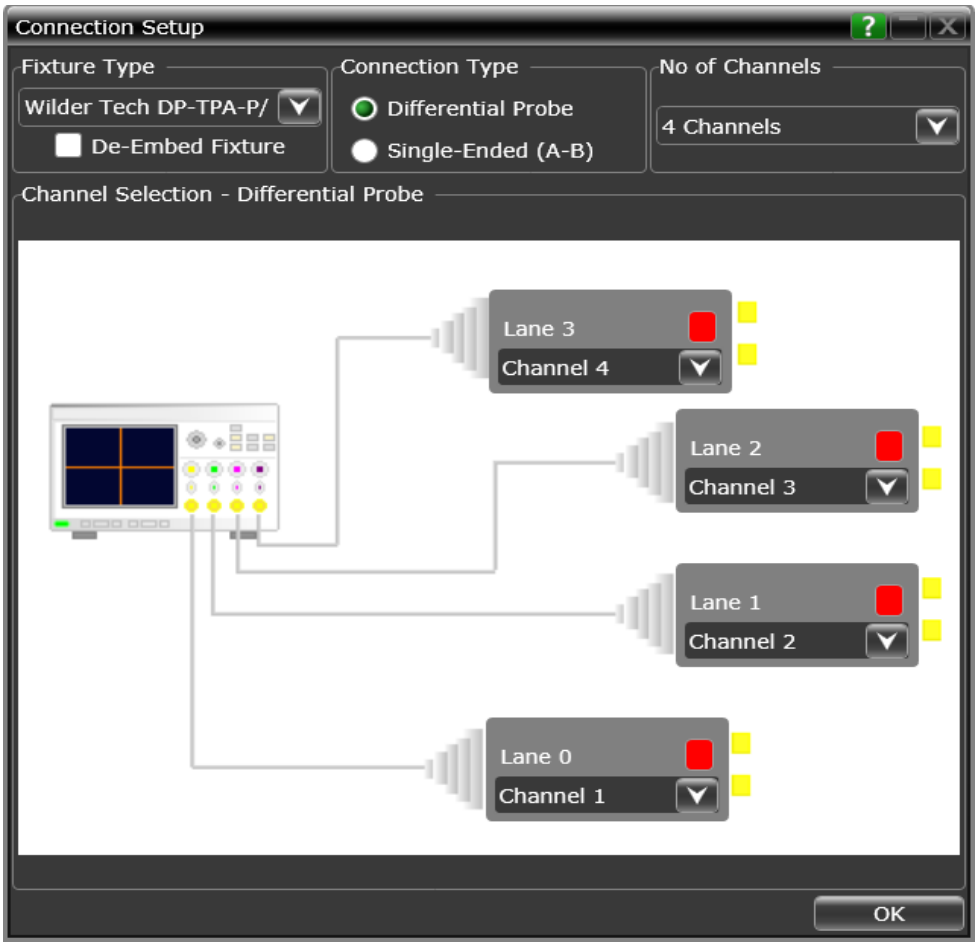
Test Overview

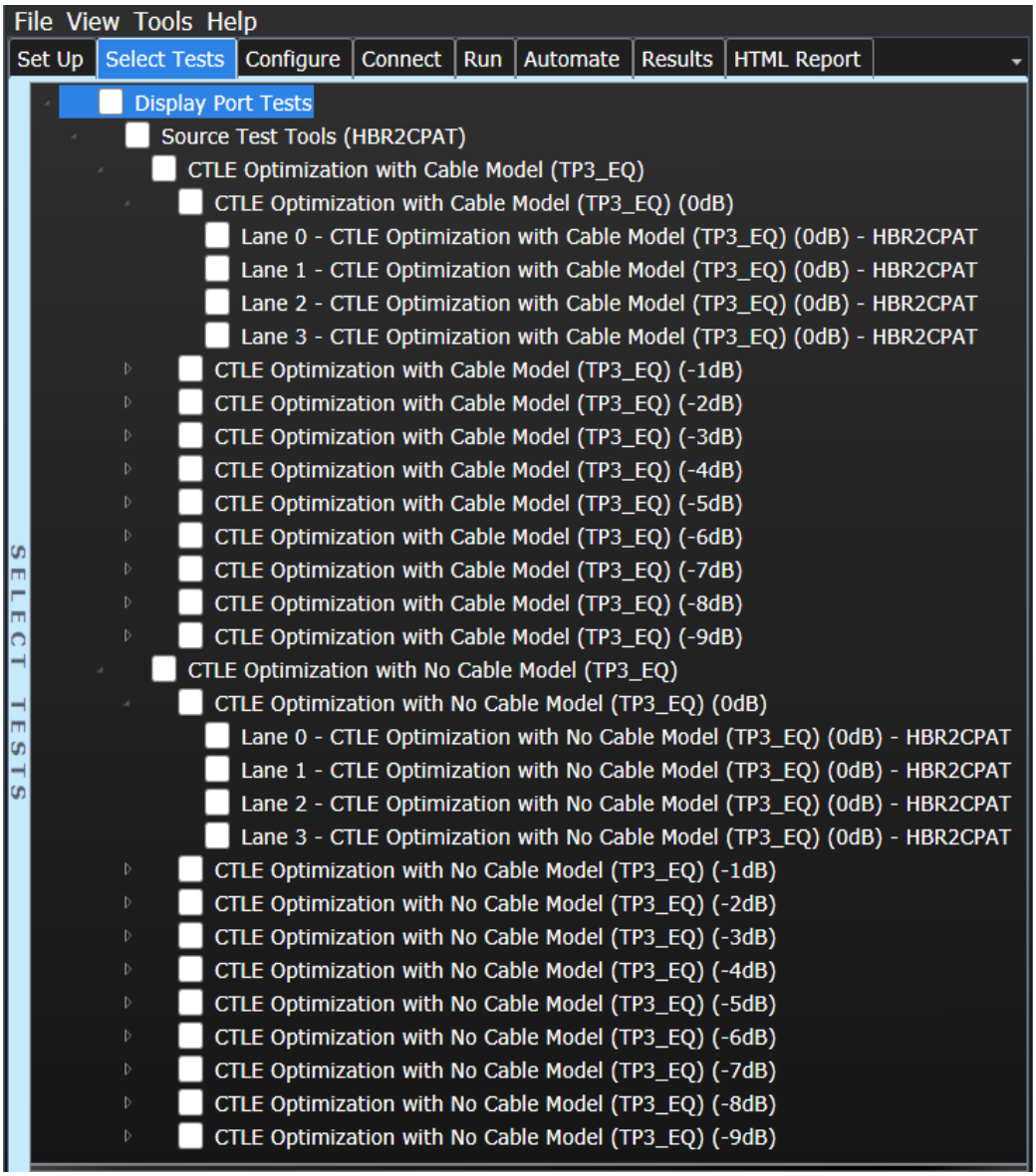
The objective of the test is to sweep the DC gain of the CTLE transfer function as defined in the "Equalization" on page 251 to find the optimal CTLE DC gain based on the eye height. Such values of the Optimal CTLE DC gain that generate the highest eye height must be used for the TP3_EQ tests.

Test Conditions for CTLE Optimization Tests

Test Parameter	Condition
Test Point	TP3_CTLE
Bit Rate	HBR2 (Informative), HBR3
Spread Spectrum Clocking	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria
Post Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria
Lane Setting	All test lanes supported
Test Pattern	HBR2: HBR2CPAT HBR3: TPS4
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Connector Type
Standard DP/mDP
Test Info
Test Type
Differential Tests
Data Pattern
Standard DP Pattern
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
8.1 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR3 Preferred Level Setting with Cable Model
Swing 1/ Pre-emphasis 1/ PC2 Level
HBR3 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech DP-TPA-P/
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
4 Channels
Channel Selection - Differential Probe
Lane 3
Channel 4
Lane 2
Channel 3
Lane 1
Channel 2
Lane 0
Channel 1
OK


File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Display Port Tests
Source Test Tools (HBR2CPAT)
CTLE Optimization with Cable Model (TP3_EQ)
CTLE Optimization with Cable Model (TP3_EQ) (0dB)
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (0dB) - HBR2CPAT
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (0dB) - HBR2CPAT
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (0dB) - HBR2CPAT
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (0dB) - HBR2CPAT
CTLE Optimization with Cable Model (TP3_EQ) (-1dB)
CTLE Optimization with Cable Model (TP3_EQ) (-2dB)
CTLE Optimization with Cable Model (TP3_EQ) (-3dB)
CTLE Optimization with Cable Model (TP3_EQ) (-4dB)
CTLE Optimization with Cable Model (TP3_EQ) (-5dB)
CTLE Optimization with Cable Model (TP3_EQ) (-6dB)
CTLE Optimization with Cable Model (TP3_EQ) (-7dB)
CTLE Optimization with Cable Model (TP3_EQ) (-8dB)
CTLE Optimization with Cable Model (TP3_EQ) (-9dB)
CTLE Optimization with No Cable Model (TP3_EQ)
CTLE Optimization with No Cable Model (TP3_EQ) (0dB)
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (0dB) - HBR2CPAT
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (0dB) - HBR2CPAT
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (0dB) - HBR2CPAT
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (0dB) - HBR2CPAT
CTLE Optimization with No Cable Model (TP3_EQ) (-1dB)
CTLE Optimization with No Cable Model (TP3_EQ) (-2dB)
CTLE Optimization with No Cable Model (TP3_EQ) (-3dB)
CTLE Optimization with No Cable Model (TP3_EQ) (-4dB)
CTLE Optimization with No Cable Model (TP3_EQ) (-5dB)
CTLE Optimization with No Cable Model (TP3_EQ) (-6dB)
CTLE Optimization with No Cable Model (TP3_EQ) (-7dB)
CTLE Optimization with No Cable Model (TP3_EQ) (-8dB)
CTLE Optimization with No Cable Model (TP3_EQ) (-9dB)

Measurement Procedure:

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For CTLE Optimization with Cable Model (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For CTLE Optimization with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in "Equalization" on page 251, without the DFE.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in "Clock Recovery" on page 254.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge and right edge.
7 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.
8 Find the maximum eye height location of the eye diagram.
9 Set up the parameters for the Mask Test.
   a Run the eye mask until 1,000,000 UI are folded.
10 Measure the eye height of the eye diagram using the Histogram.
11 Measure the jitter of the eye diagram using the Histogram.
12 Calculate the eye width based on the measured jitter of the eye diagram.
13 Record the eye height and eye width for the given CTLE DC gain.
14 Repeat steps 6 to 13 for all the CTLE DC gain selected.
15 Find the optimum CTLE DC gain based on the value of CTLE DC gain that provides the maximum eye height. If there are two values of CTLE DC gain with the same eye height, select the one with the greater eye width.
16 Report the optimum CTLE DC gain results.

PASS Condition

-

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort Standard Version 1.4, Section 3.5.2.8.2, Table 3-28 for RBR, Table 3-27 for HBR*

Expected/Observable Results

The optimum CTLE DC gain that generate the highest eye height will be reported.

30 MyDP 1.0 Source Tests

Overview

This section describes the normative and informative main link physical layer tests for compliance verification of Mobility DisplayPort (MyDP) sources.

Test Point Definition for MyDP Tests

Five different test points are identified for the physical layer measurement. See Figure 197.

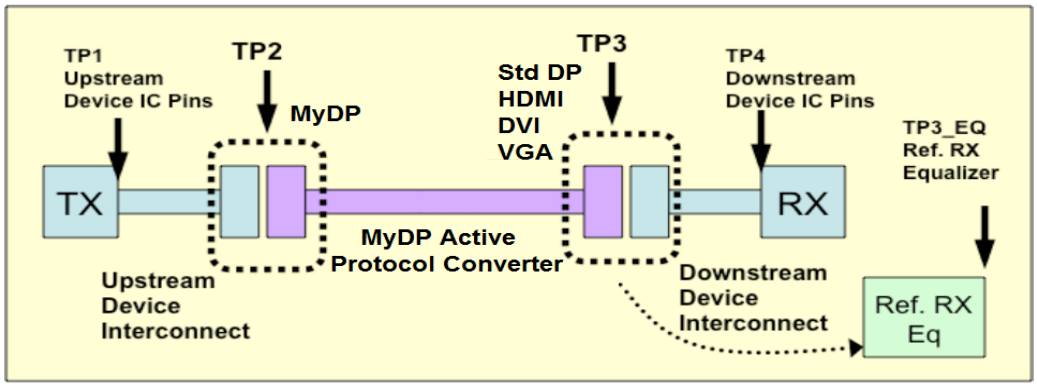


Figure 197 Test Points in a DisplayPort InterConnect System

Table 214 defines the Test Points used for MyDP 1.0 Tests:

Table 214 Test Points for DisplayPort Tests

Test Point	Description
TP1	At the pins of the Transmitter Device
TP2	At the test interface on a test access fixture as close as possible to the DP mated connection to a Source device
TP3	At the test interface on a test access fixture as close as possible to the DP mated connection to a Sink device
TP3_EQ	At TP3, when a defined cable model with equalizer is applied. There are two defined cable models: ▪ Worst Cable Model as defined in VESA DisplayPort 1.2a Standard, ▪ Zero length, zero loss cable. The equalizer is also defined in VESA DisplayPort 1.2a Standard
TP4	At the pins of a receiving device

Cable Models

The two cable models defined in VESA DisplayPort 1.2a Standard are:

1 Worst Case Cable Model—To achieve the TP3_EQ signal with the worst case cable model:

- Acquire the signal at TP2.
- Embed the TP2 signal with a “worst case” cable model using an InfiniiSim Waveform Transformation Toolset software to emulate the insertion loss as defined in Figure 4-10 of the VESA DisplayPort 1.2a Standard.
  - The “*CIC_rev0p6.s4p*” cable model transfer function is used.
- Finally, apply the HBR or HBR2 equalization using the Serial Data Equalization software as defined in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard for RBR, HBR, and HBR2.

2 Zero Length Cable Model—To achieve the TP3_EQ signal with the zero length cable model:

- Acquire the signal at TP2.
- No cable model is embedded for the Zero Length cable model.
- Finally, apply the HBR or HBR2 equalization using the Serial Data Equalization software as defined in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard.

Equalization

When equalization is required, use the CTLE (Continuous Time Linear Equalization) transfer function, as given in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard.

For main link, use the CTLE model with the following transfer function for HBR:

The HBR Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{\sqrt{\omega^2+\omega_z^2}}{\sqrt{\omega^2+\omega_{p1}^2}\cdot\sqrt{\omega^2+\omega_{p2}^2}}$$

where

$$\omega_z = 2\pi(0.725\times10^9)$$
$$\omega_{p1} = 2\pi(1.35\times10^9)$$
$$\omega_{p2} = 2\pi(2.5\times10^9)$$

Figure 198 Transfer Function of the CTLE model for HBR

For main link, use the CTLE model with the following transfer function for HBR2:

The HBR2 Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})(s+\omega_{p3})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{\sqrt{\omega^2+\omega_z^2}}{\sqrt{\omega^2+\omega_{p1}^2}\cdot\sqrt{\omega^2+\omega_{p2}^2}\cdot\sqrt{\omega^2+\omega_{p3}^2}}$$

where

$\omega z = 2\pi\ (0.64 \times 10^9)$ for upstream device compliance

and

$\omega p1 = 2\pi\ (2.7 \times 10^9)$

$\omega p2 = 2\pi\ (4.5 \times 10^9)$

$\omega p3 = 2\pi\ (13.5 \times 10^9)$

Figure 199 Transfer Function of the CTLE model for HBR2

Clock Recovery

When Clock Recovery is required, the clock recovery technique follows the definition of the receiver PLL as defined in Section 3.5.3.5 of the VESA DisplayPort 1.2a Standard. For main link, use the second-order clock recovery function with a closed loop tracking bandwidth and damping factor, with respect to the PRBS7 pattern, as shown in Table 215:

Table 215 Main Link Second-Order Clock Recovery Function

Bit Rate	Bandwidth	Damping Factor
HBR2	10 MHZ	1.00
HBR	10 MHz	1.51
RBR	5.4 MHz	1.51

Test Point Definition for MyDP 1.0 Source Tests

Test the Source DUT at Test Point 2 (TP2) as shown in Figure 200.

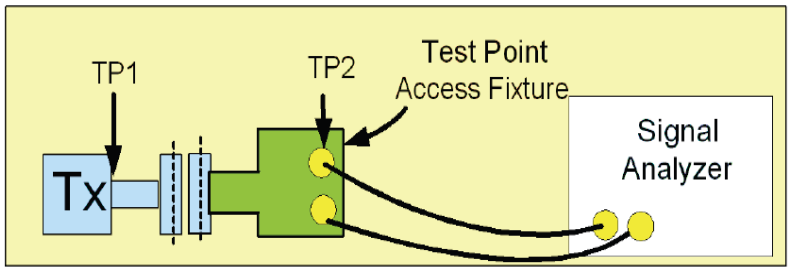


Figure 200 Test Point 2 Connection for MyDP 1.0 Source Tests

Use MyDP Test Fixtures (MyDP-to-DP type or MyDP-to-SMA type) to perform PHY compliance tests specific to MyDP. Figure 201 shows the layout of a MyDP passive cable adapter or a MyDP protocol converter:

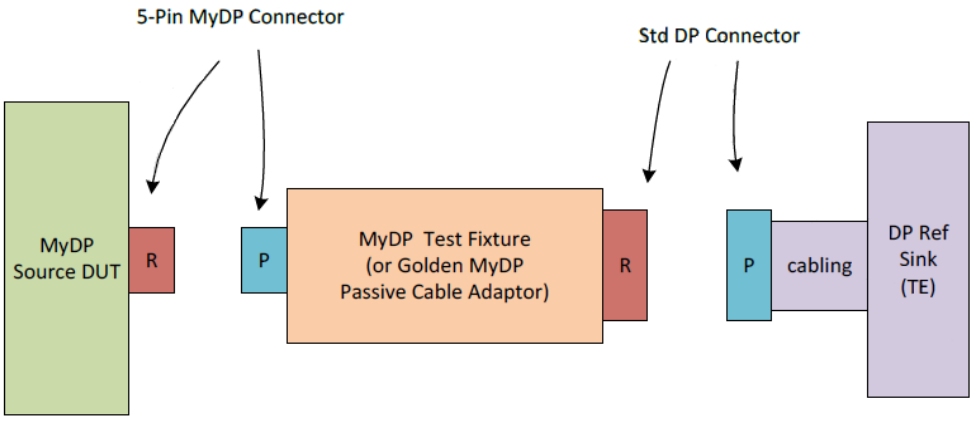


Figure 201 Schematics of MyDP to SMA Test Fixtures used for PHY Compliance Tests

Table 216 defines the test point fixtures and instruments used for MyDP 1.0 Source Tests:

Table 216 Test Point Fixtures and Instruments for MyDP 1.0 Source Tests

Test Requirement	Device Used
Test Point Access Fixture	Mobility DisplayPort Test Point Adapter For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort MyDP 1.0 Standards, select the option **MyDP 1.0** in the **Test Specification** area.

5 The option **Physical Layer Tests** appears by default in the **Test Selection** area.

6 Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.

7 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

8 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

9 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

10 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

11 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

12 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

13 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

14 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for MyDP 1.0 Source Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

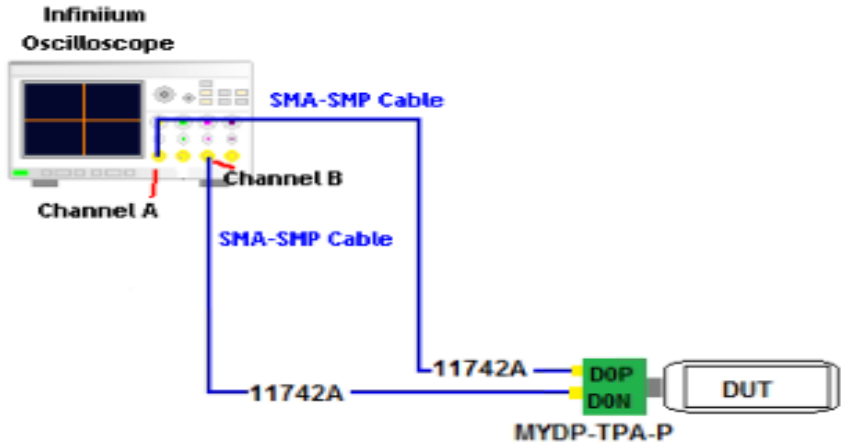


Figure 202 Sample connection diagram for MyDP 1.0 Source Tests

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Source tests (either differential or single-ended) to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1. In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.
2. On the **Test Setup** window,
   - *a* Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.
   - *b* In the **DUT Info** area, the **Device Type** is selected as **Source** by default.
   - *c* In the **Test Info** area, the **Test Type** is selected as **Differential Tests** by default. Select **Single-Ended Tests** from the drop-down options for the respective tests to appear in the **Select Tests** tab.
   - *d* In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.
3. Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1. Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.
2. On the **Connection Setup** window,
   - *a* Select the appropriate option in the **Fixture Type** to indicate where the DUT is connected to.
   - *b* Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.
   - *c* In the **Channel Selection** area, assign appropriate channels to lanes.
3. Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of source tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 1059 to complete the task flow for DUT setup along with configuring the Compliance Application to run each test.

Source Eye Diagram Test

Test ID

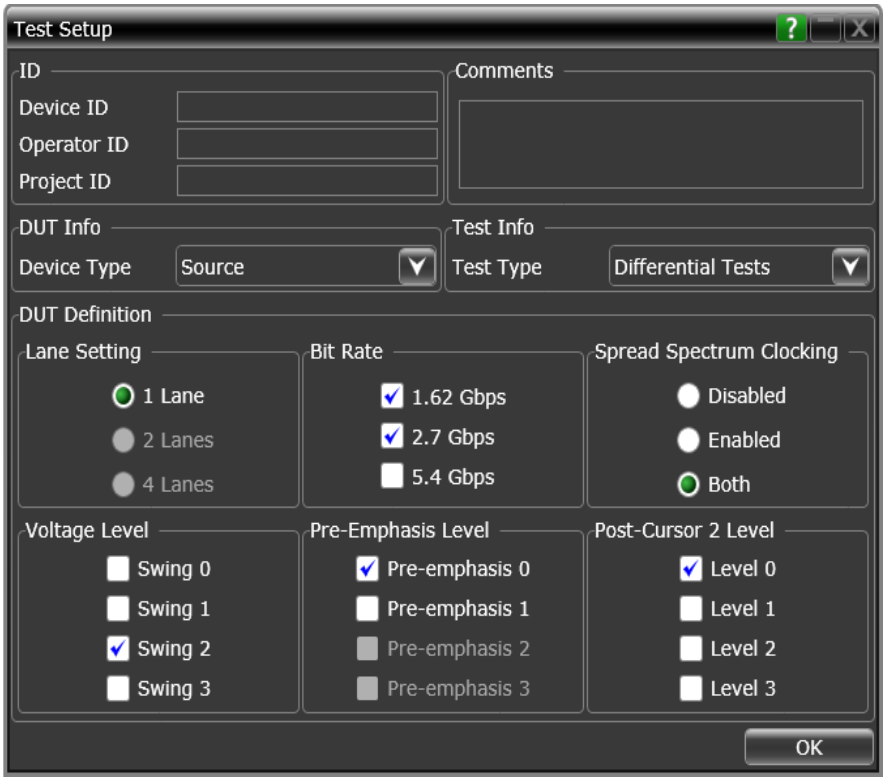
1210001 – Eye Diagram Test

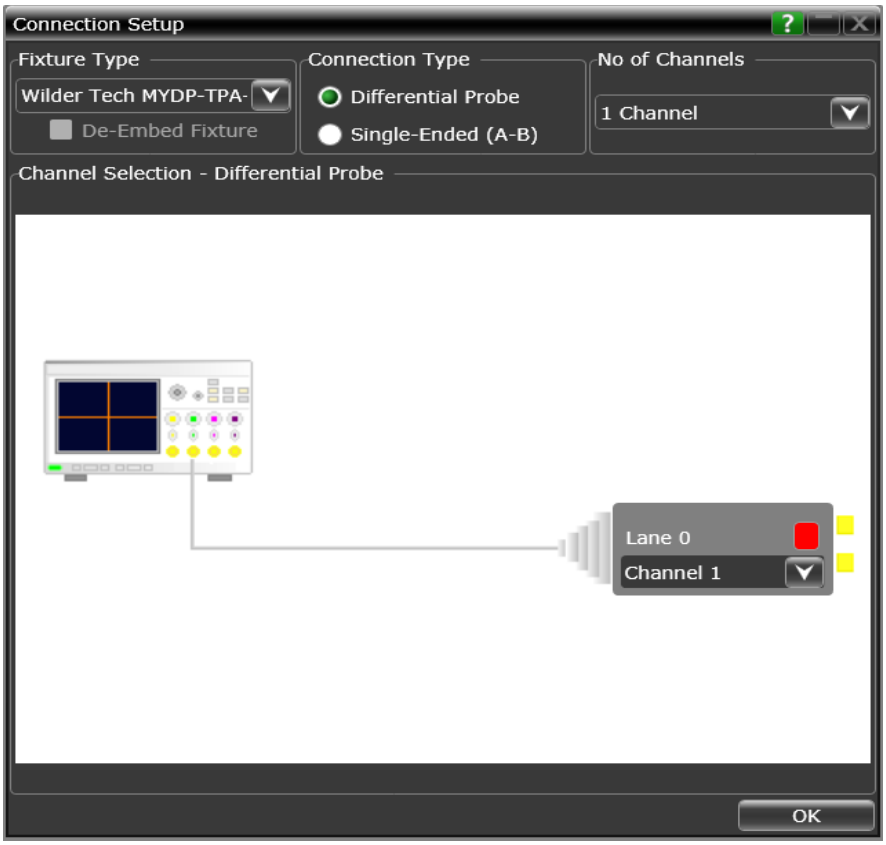
Test Overview

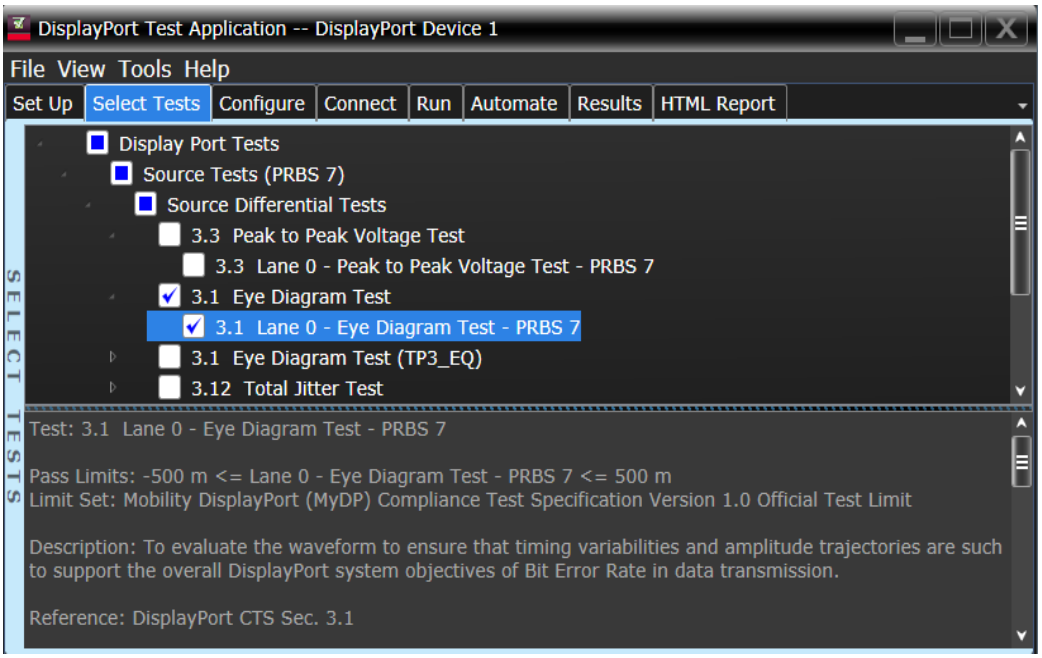
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Measure V_{TOP} and V_{BASE} of the input signal using the pattern folding.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the input signal eye diagram to measure the left edge.
7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the eye height of the eye diagram using the Histogram.
9 Measure the jitter of the eye diagram using the Histogram.
10 Calculate the eye width based on the measured jitter of the eye diagram.
11 Check for any signal trajectories that may have entered into the mask.
12 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 217 shows the voltage and time coordinates for the mask used in the eye diagram.

Table 217 Eye Diagram Mask Coordinates

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	High (2.7 Gb/s)
1	0.127, 0.000	0.210, 0.000
2	0.291, 0.160	0.355, 0.140
3	0.500, 0.200	0.500, 0.175
4	0.709, 0.200	0.645, 0.175
5	0.873, 0.000	0.790, 0.000
6	0.709,-0.200	0.645,-0.175
7	0.500,-0.200	0.500,-0.175
8	0.291,-0.160	0.355,-0.140

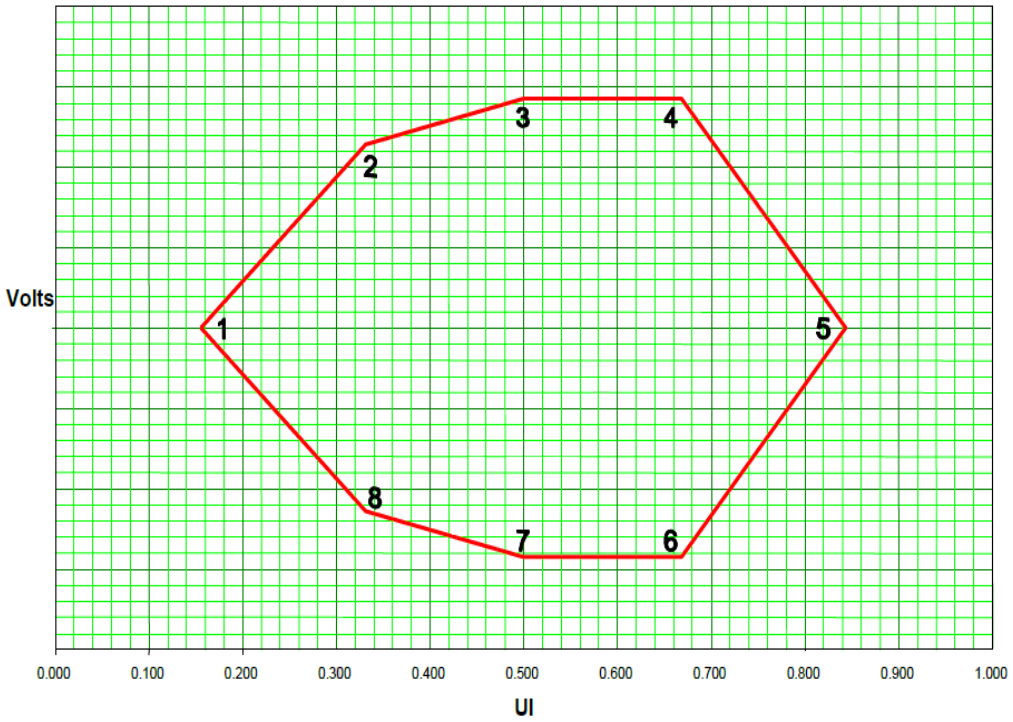


Figure 203 The Source Eye Mask

Mask Test: Zero mask failures.

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-24 for RBR and Table 3-23 for HBR*

Expected/Observable Results

The measured eye diagram for the source degraded signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test

Test ID

1220001 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

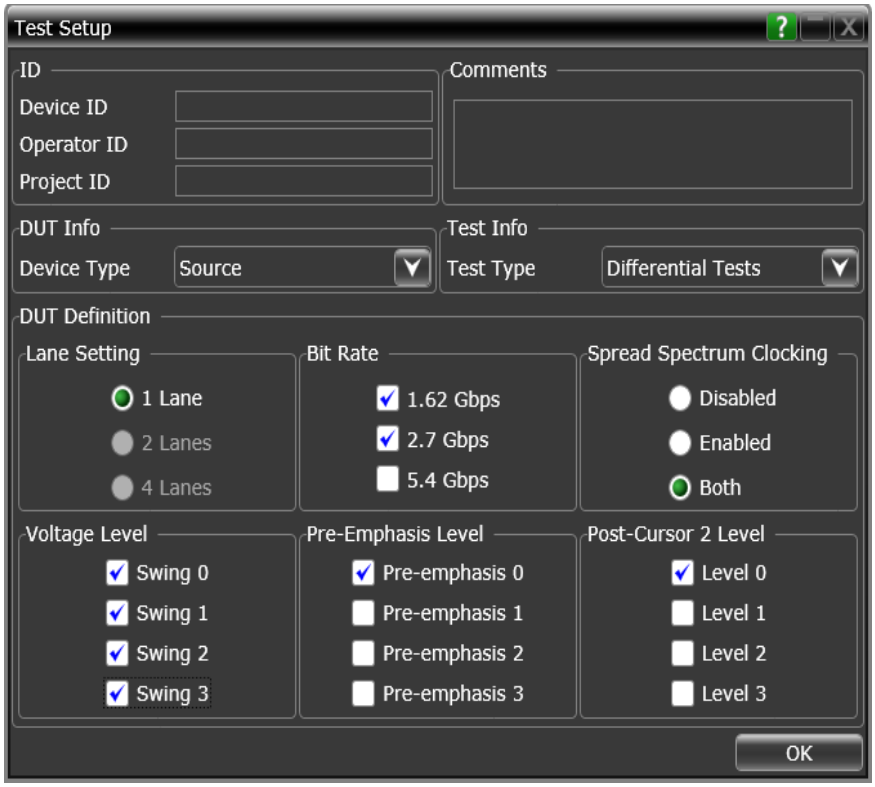
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

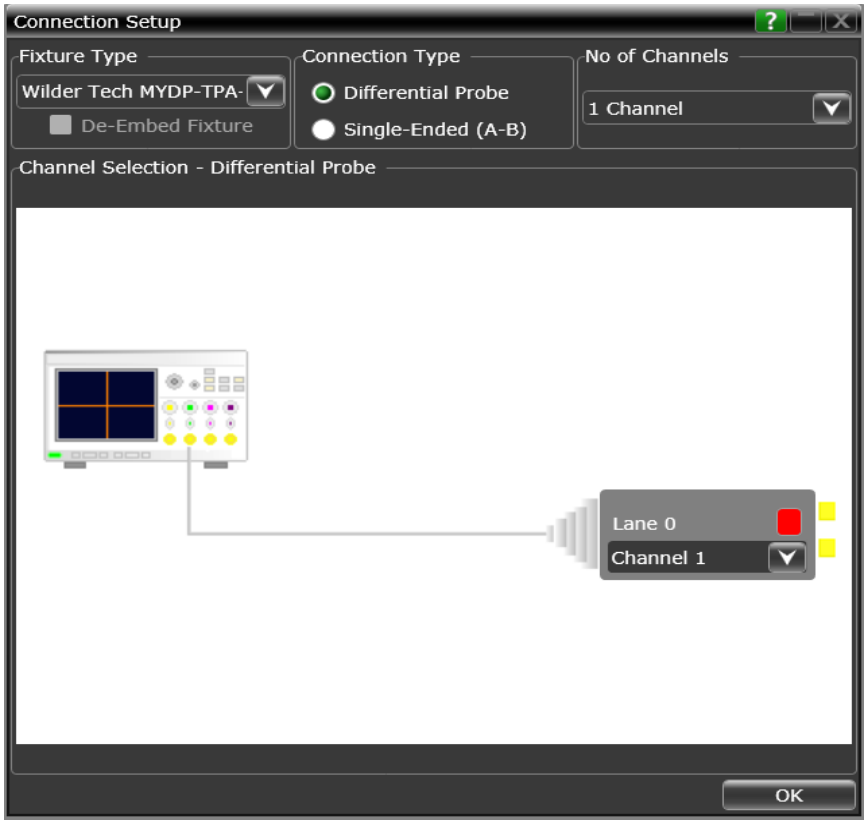
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

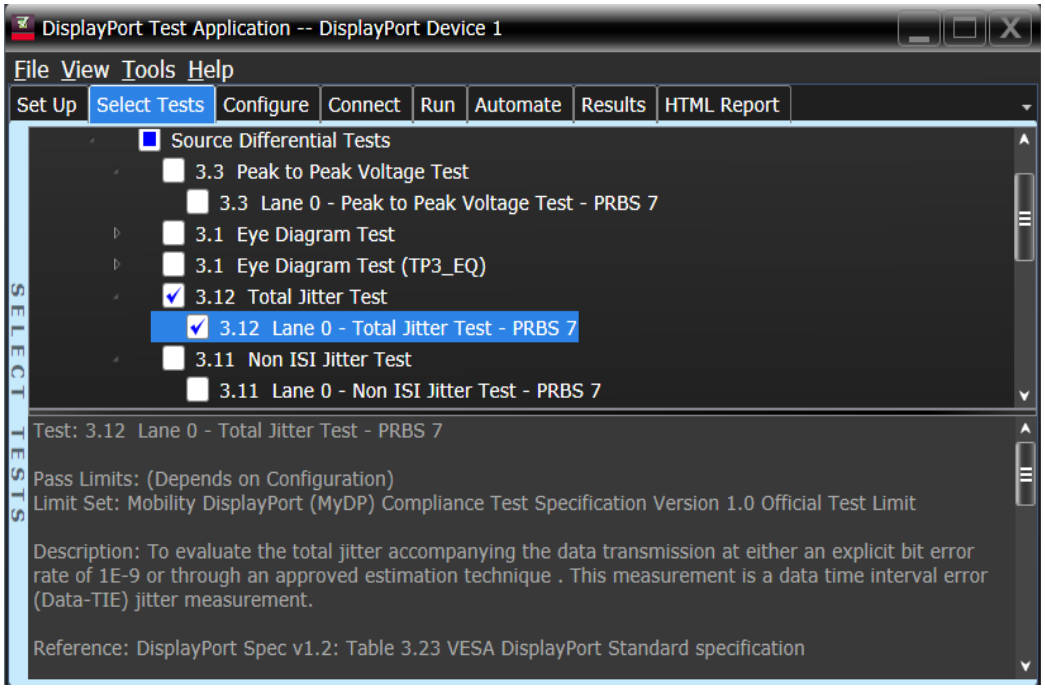
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Report the measurement results.

PASS Condition

Table 218 Total Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
Ap-p	0.294 UI	0.420 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
Ap-p	0.180 UI	0.270 UI

UI is Unit Interval.

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non-ISI Jitter Test

Test ID

1230001 – Non ISI Jitter Test

Test Overview

The objective of the test is to evaluate the amount of Non ISI jitter accompanying the data transmission.

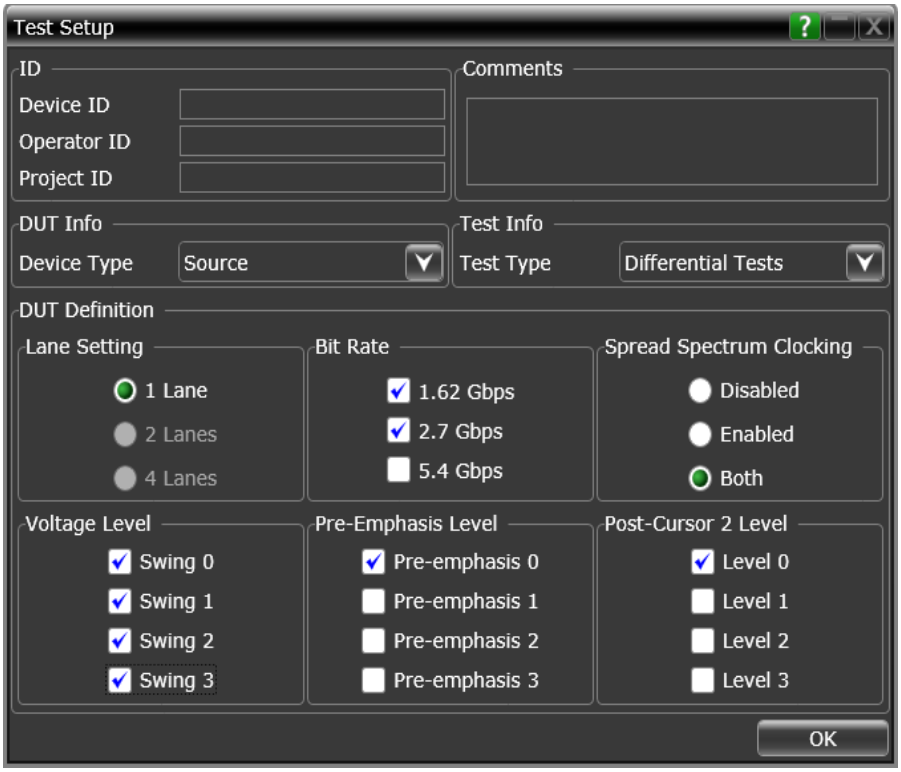
The jitter is separated into each jitter components based on the Dual-Dirac Model:

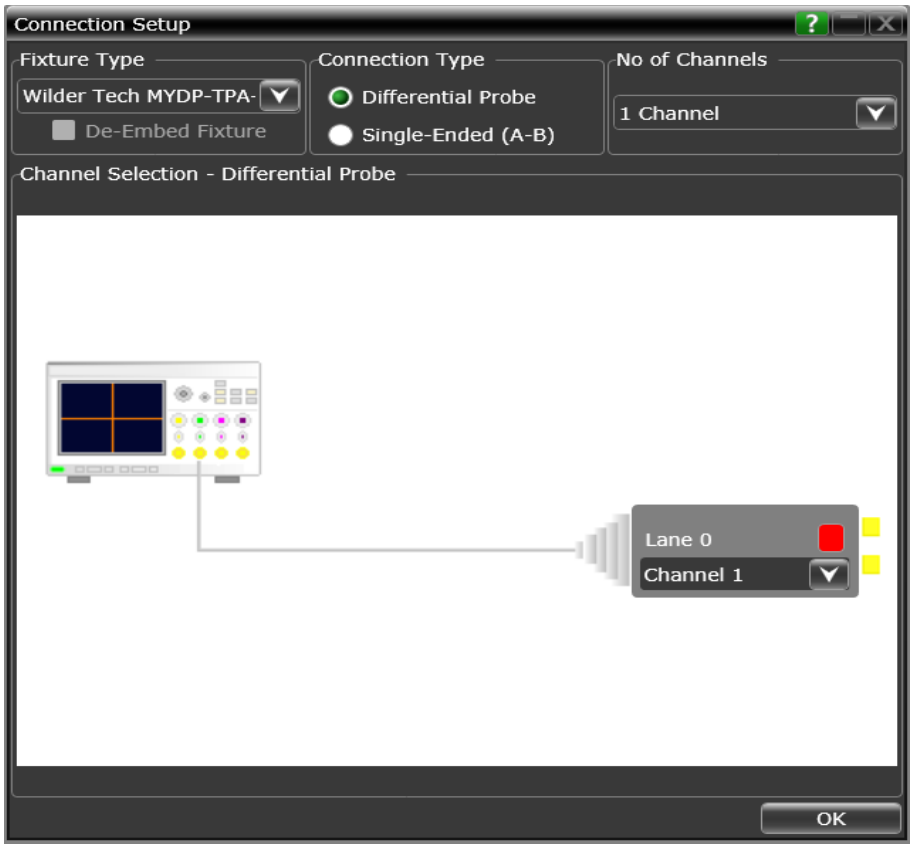
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

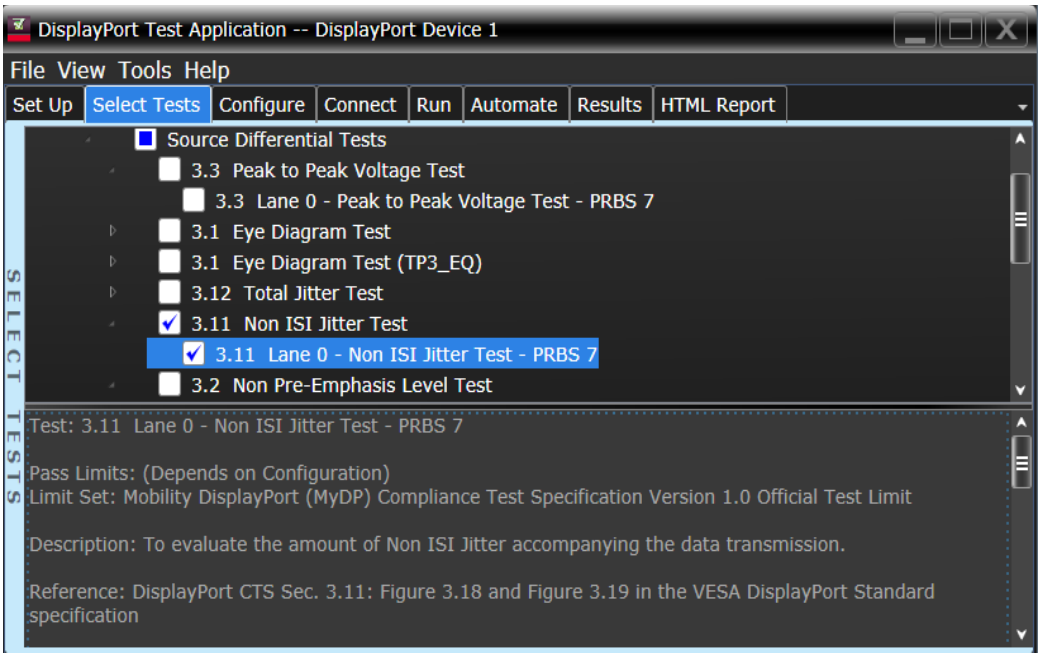
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Calculate the Non ISI jitter using the following equation:

$$\text{Non ISI Jitter} = \text{TJ} - \text{ISI}$$

7 Report the measurement results.

PASS Condition

Table 219 Non-ISI Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.260 UI	0.276 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.160 UI	0.210 UI

UI is Unit Interval.

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.11*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Pre-Emphasis Level Test

Test ID

For RBR and HBR:

- 1261001 – Non Pre-Emphasis Level Test (Swing 1/Swing 0)
- 1262001 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263001 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

For HBR2:

- 1264101 – Non Pre-Emphasis Level Test (Swing 2/Swing 0)
- 1262101 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263101 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

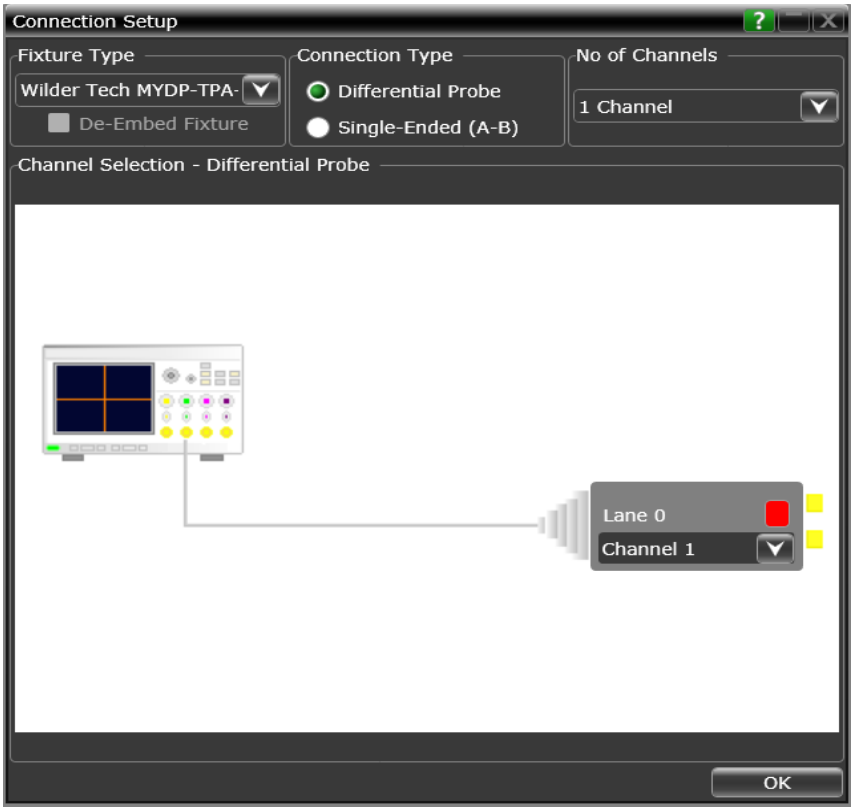
Test Overview

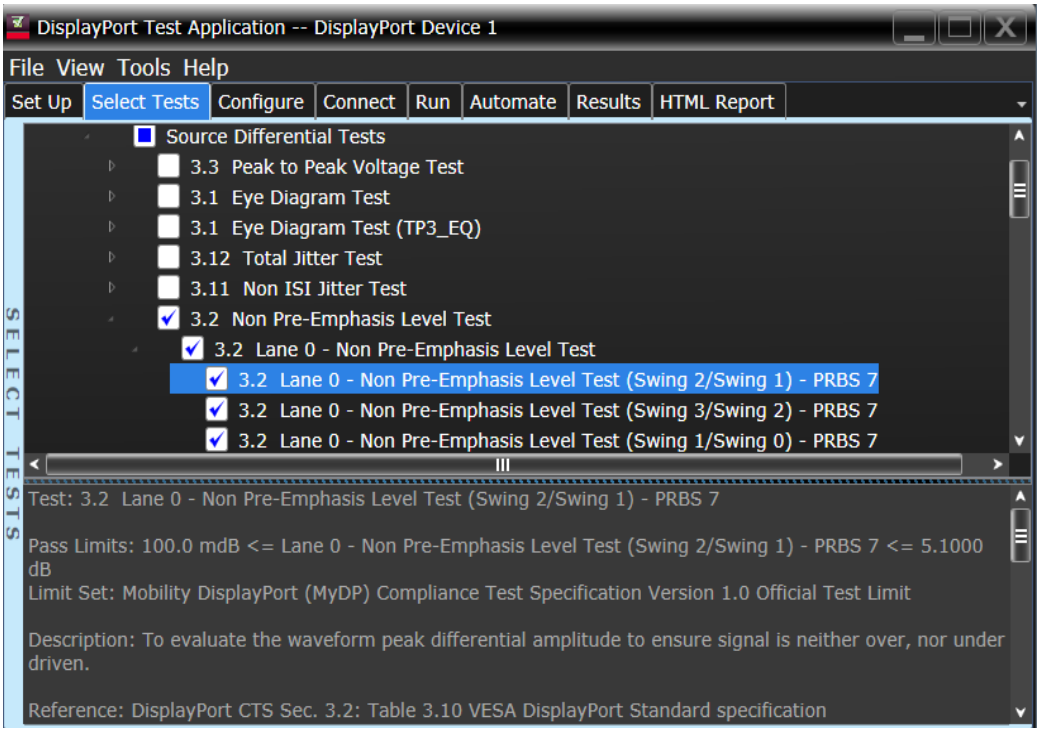
The objective of this test is to ensure that the system budget elements are obeyed and to ensure that the level settings are monotonic so that the sink relies on the source to incrementally increase upon request by the sink.

Test Conditions for Non Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR – PRBS7 HBR2 – PLTPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 For Voltage Level A with no pre-emphasis level:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

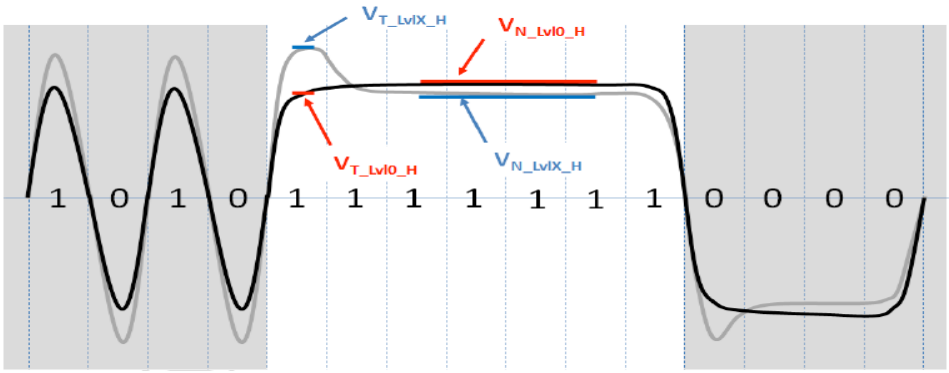


Figure 204 High Voltage measurement for RBR and HBR

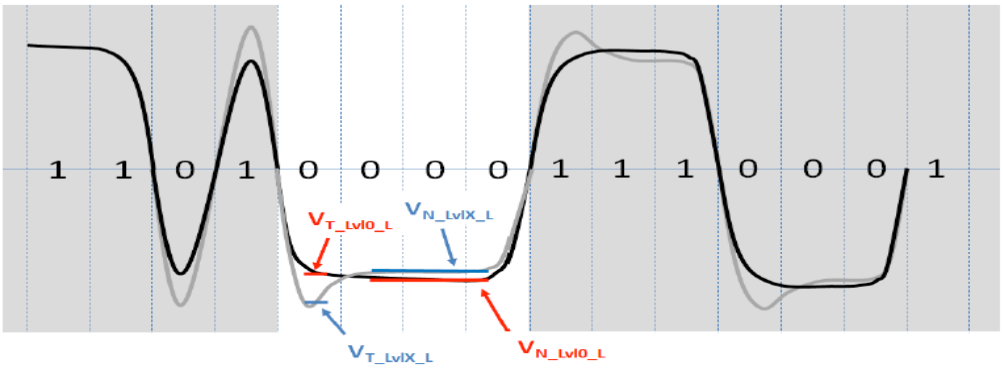


Figure 205 Low Voltage measurement for RBR and HBR

e For HBR2 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted zeros of the pattern.

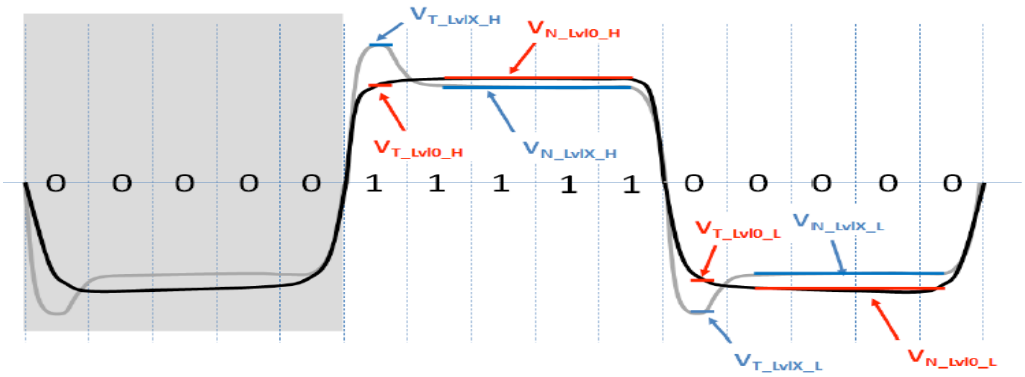


Figure 206 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_Lvl0\_PP} = V_{T\_Lvl0\_H} - V_{T\_Lvl0\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_Lvl0\_PP} = V_{N\_Lvl0\_H} - V_{N\_Lvl0\_L}$$

2 Repeat Step 1 for Voltage Level B with no pre-emphasis level.

3 Calculate the non pre-emphasis level output voltage ratio using the equation:

Non Pre-Emphasis Level = $20 * \text{Log}_{10}[\text{Voltage Level A } V_{N\_Lvl0\_PP} / \text{Voltage Level B } V_{N\_Lvl0\_PP}]$

4 Report the measurement results.

PASS Condition

For each level setting testes, the following equation should be used:

$\text{Resultant} = 20 * \text{Log}_{10}[\text{Voltage}_{\text{Peak-Peak\_LevelA}} / \text{Voltage}_{\text{Peak-Peak\_LevelB}}]$

Table 220 Compared Levels

Measurement#	$\text{Voltage}_{\text{Peak-Peak\_LevelA}}$	$\text{Voltage}_{\text{Peak-Peak\_LevelB}}$
RBR & HBR		
1	Level 1 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)
2	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
3*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)
HBR2		
4	Level 2 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)

Table 220 Compared Levels

Measurement#	$Voltage_{Peak\text{-}Peak\_LevelA}$	$Voltage_{Peak\text{-}Peak\_LevelB}$
5	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
6*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)

* if device optionally capable of Level 3

The resultants specifications are as identified below:

Measurement 1: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 2: 0.1 dB ≤ Resultant ≤ 5.1 dB

Measurement 3: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 4: 5.2 dB ≤ Resultant ≤ 6.9 dB

Measurement 5: 1.6 dB ≤ Resultant ≤ 3.5 dB

Measurement 6: 1 dB ≤ Resultant ≤ 4.4 dB

Table 221 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}OUTPUT\text{-}RATIO\_RBR\_HBR}$	Ratio of Output Voltage Level 1/Level 0	0.8	-	6.0	dB	Measured on non-transition bits at Pre-emphasis level 0 setting
	Ratio of Output Voltage Level 2/Level 1	0.1	-	5.1	dB	
	Ratio of Output Voltage Level 3/Level 2	0.8	-	6.0	dB	
$V_{TX\text{-}OUTPUT\text{-}RATIO\_HBR2}$	Ratio of Output Voltage Level 2/Level 0	5.2	-	6.9	dB	Measured on non-transition bits at Pre-emphasis level 0 setting
	Ratio of Output Voltage Level 2/Level 1	1.6	-	3.5	dB	
	Ratio of Output Voltage Level 3/Level 2	1	-	4.4	dB	

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured output voltage level ratio of the non pre-emphasis level test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Pre-Emphasis Level Differential Tests

Test ID

For RBR and HBR:

- 1270001 – Pre-Emphasis Level Test

For HBR2:

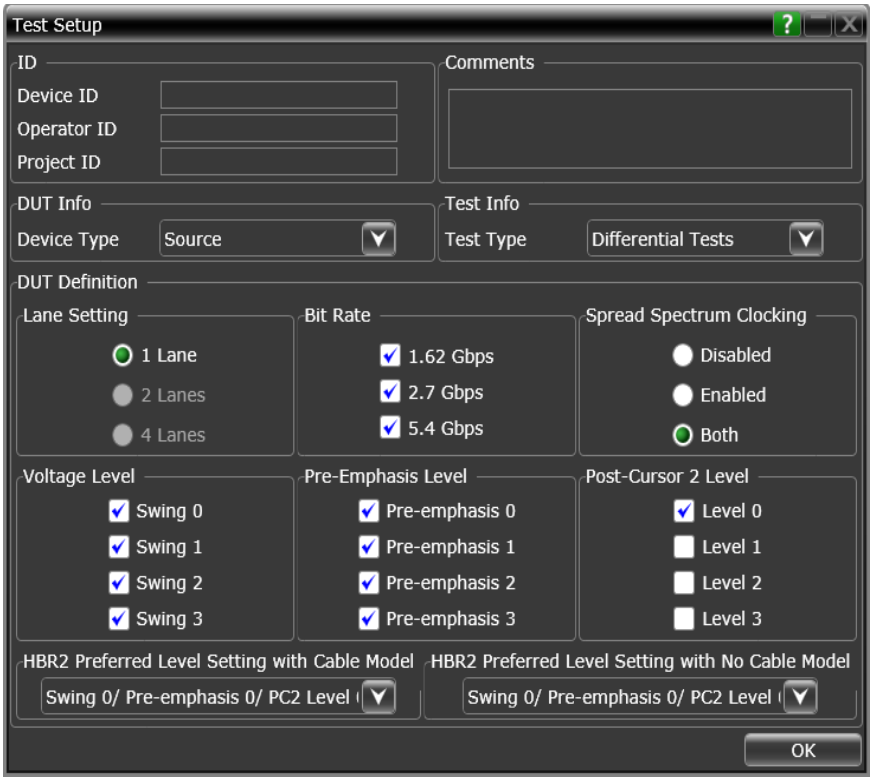
- 1270501 – Pre-Emphasis Level Test

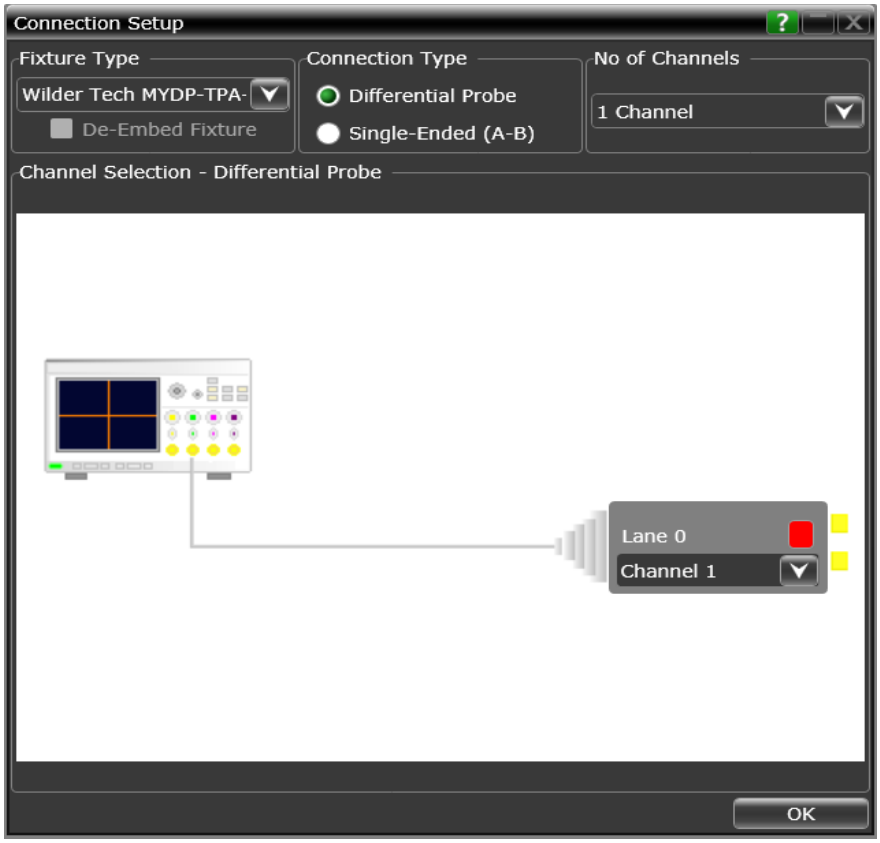
Test Overview

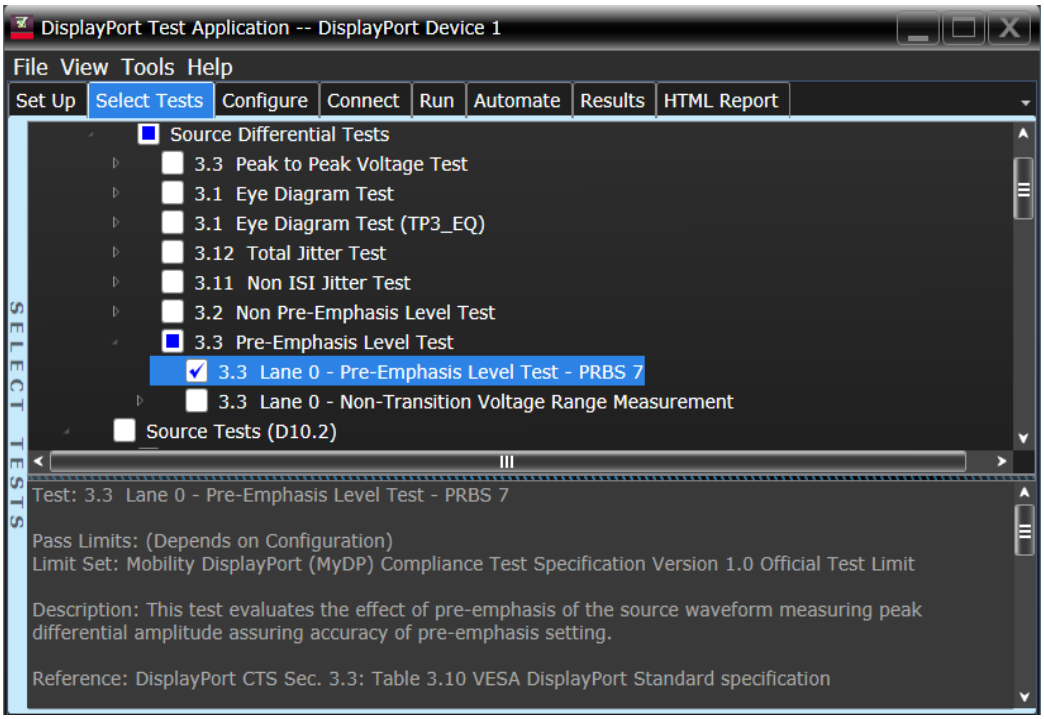
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings.

Test Conditions for Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR – PRBS7 HBR2 – PLTPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given Voltage Level and a Pre-Emphasis Level X:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

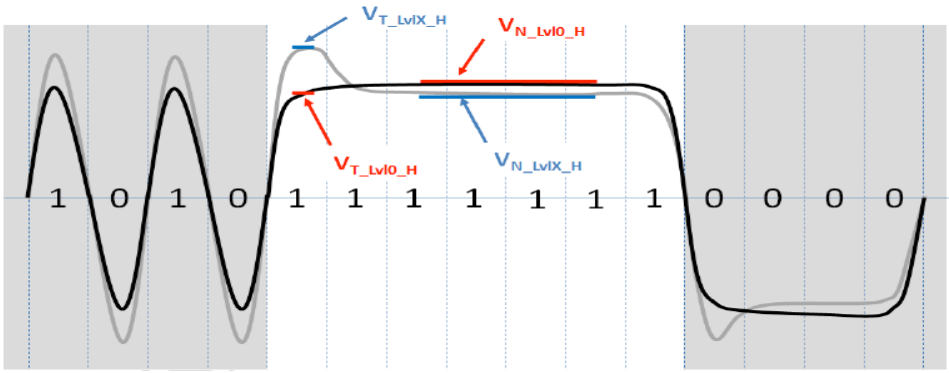


Figure 207 High Voltage measurement for RBR and HBR

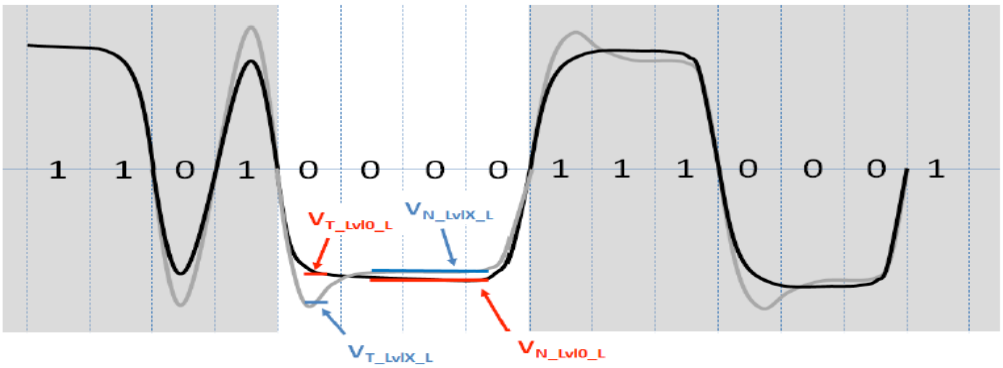


Figure 208 Low Voltage measurement for RBR and HBR

e For HBR2 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted zeros of the pattern.

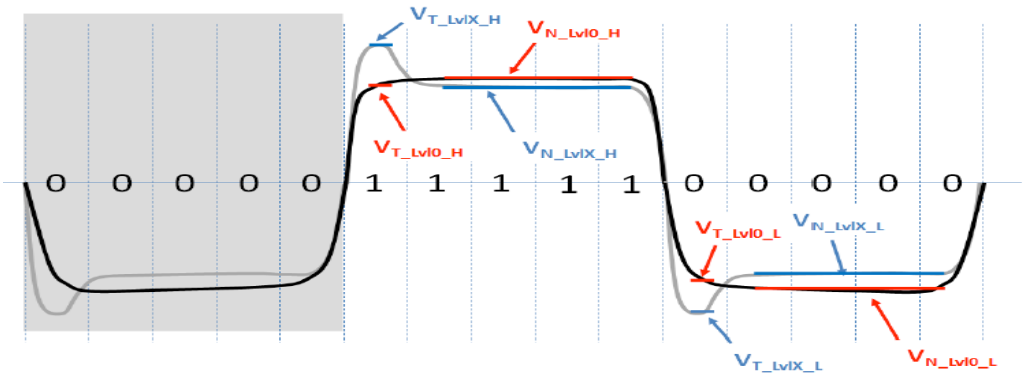


Figure 209 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

l Calculate the pre-emphasis level using the equation:

$$\text{Pre-Emphasis}_{LvlX} = 20 * \text{Log}_{10}[V_{T\_LvlX\_PP} / V_{N\_LvlX\_PP}]$$

2 For Pre-Emphasis Level 0 (no pre-emphasis level), the result for $\text{Pre-Emphasis}_{Lvl0}$ is compared with the maximum pre-emphasis disabled limit.

3 Repeat Step 1 for the next Pre-Emphasis level and for each Pre-Emphasis levels, compare the pre-emphasis delta with the pre-emphasis delta limits.

4 Calculate the pre-emphasis delta using the equation:

$$\text{Pre-Emphasis Delta (Level 1 vs Level 0)} = \text{Pre-Emphasis}_{Lvl1} - \text{Pre-Emphasis}_{Lvl0}$$

$$\text{Pre-Emphasis Delta (Level 2 vs Level 1)} = \text{Pre-Emphasis}_{Lvl2} - \text{Pre-Emphasis}_{Lvl1}$$

$$\text{Pre-Emphasis Delta (Level 3 vs Level 2)} = \text{Pre-Emphasis}_{Lvl3} - \text{Pre-Emphasis}_{Lvl2}$$

5 Report the measurement results.

PASS Condition

Pre-emphasis values for the Level 0 (OFF) state (Normative)

Level 0 (OFF) Pre-emphasis measurement:

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl0\_PP} / \text{Voltage}_{N\_Lvl0\_PP}]$ for all supported levels.

Level 0 (OFF) Pre-emphasis Measurement condition: +0.25 dB $\geq$ Resultant

Pre-emphasis Delta values for:

a Level 1 vs. Level 0 Pre-emphasis settings (NORMATIVE)

b Level 2 vs. Level 1 Pre-emphasis settings (NORMATIVE)

c Level 3 vs. Level 2 Pre-emphasis settings (NORMATIVE)

Pre-emphasis Delta measurements:

- Level 1 vs. Level 0

Resultant = 20 * Log [$Voltage_{T\_Lvl1\_PP}$ / $Voltage_{N\_Lvl1\_PP}$] - 20 * Log [$Voltage_{T\_Lvl0\_PP}$ / $Voltage_{N\_Lvl0\_PP}$] for Voltage Swing Levels 0, 1 and 2.

- Level 2 vs. Level 1

Resultant = 20 * Log [$Voltage_{T\_Lvl2\_PP}$ / $Voltage_{N\_Lvl2\_PP}$] - 20 * Log [$Voltage_{T\_Lvl1\_PP}$ / $Voltage_{N\_Lvl1\_PP}$] for Voltage Swing Levels 0 and 1.

- Level 3 vs. Level 2

Resultant = 20 * Log [$Voltage_{T\_Lvl3\_PP}$ / $Voltage_{N\_Lvl3\_PP}$] - 20 * Log [$Voltage_{T\_Lvl2\_PP}$ / $Voltage_{N\_Lvl2\_PP}$] for Voltage Swing Level 0, if supported.

Table 222 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX-PREEMP-OFF}$	Maximum Pre-emphasis when disabled	-	-	0.25	dB	Pre-emphasis Level 0 setting must not show any pre-emphasis at TP2 to prevent link training issues.
$V_{TX-PREEMP-DELTA}$	Delta of Pre-emphasis Level 1 vs. Level 0	2	-	-	dB	Applies to all valid voltage settings. Measured at Pre-emphasis Post Cursor2 Level 0. Support for Pre-emphasis Level 3 is optional.
	Delta of Pre-emphasis Level 2 vs. Level 1	1.6	-	-	dB	
	Delta of Pre-emphasis Level 3 vs. Level 2	1.6	-	-	dB	

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured pre-emphasis level or pre-emphasis delta for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Transition Voltage Range Measurement Test

Test ID

For RBR and HBR:

- 1272001 – Non-Transition Voltage Range Measurement (Swing 0)
- 1273001 – Non-Transition Voltage Range Measurement (Swing 1)
- 1274001 – Non-Transition Voltage Range Measurement (Swing 2)

For HBR2:

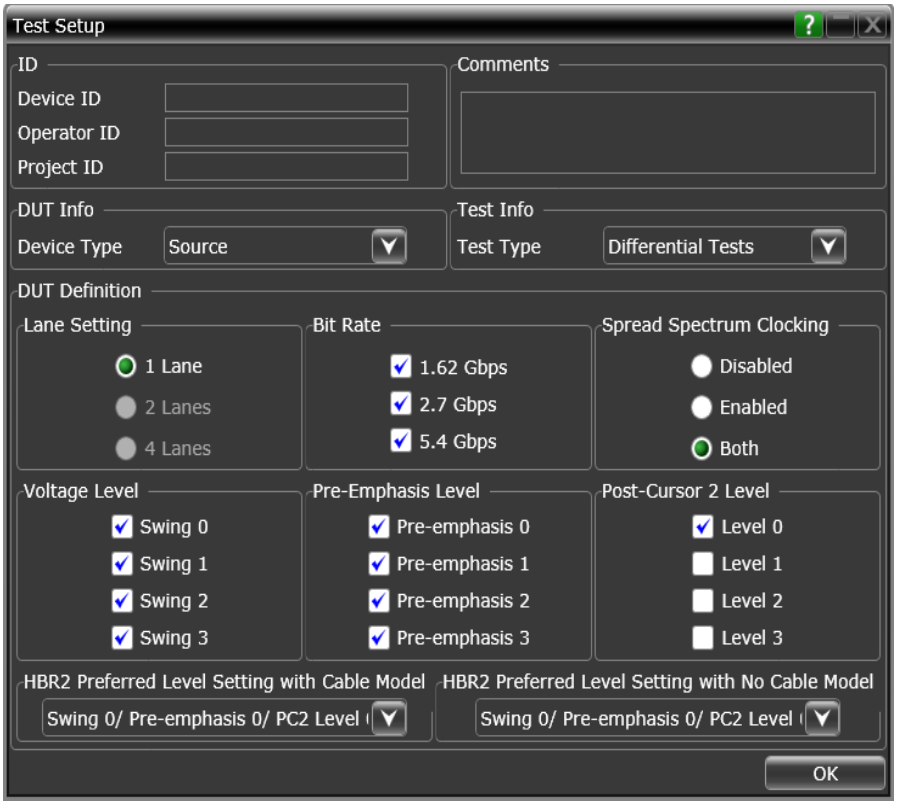
- 1272101 – Non-Transition Voltage Range Measurement (Swing 0)
- 1273101 – Non-Transition Voltage Range Measurement (Swing 1)
- 1274101 – Non-Transition Voltage Range Measurement (Swing 2)

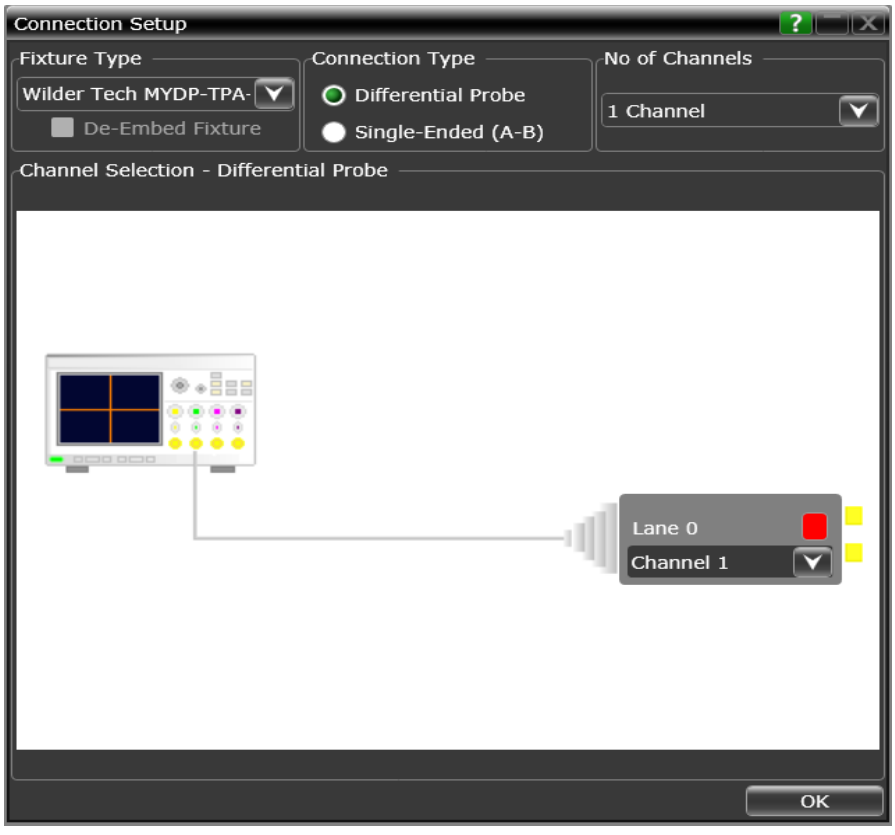
Test Overview

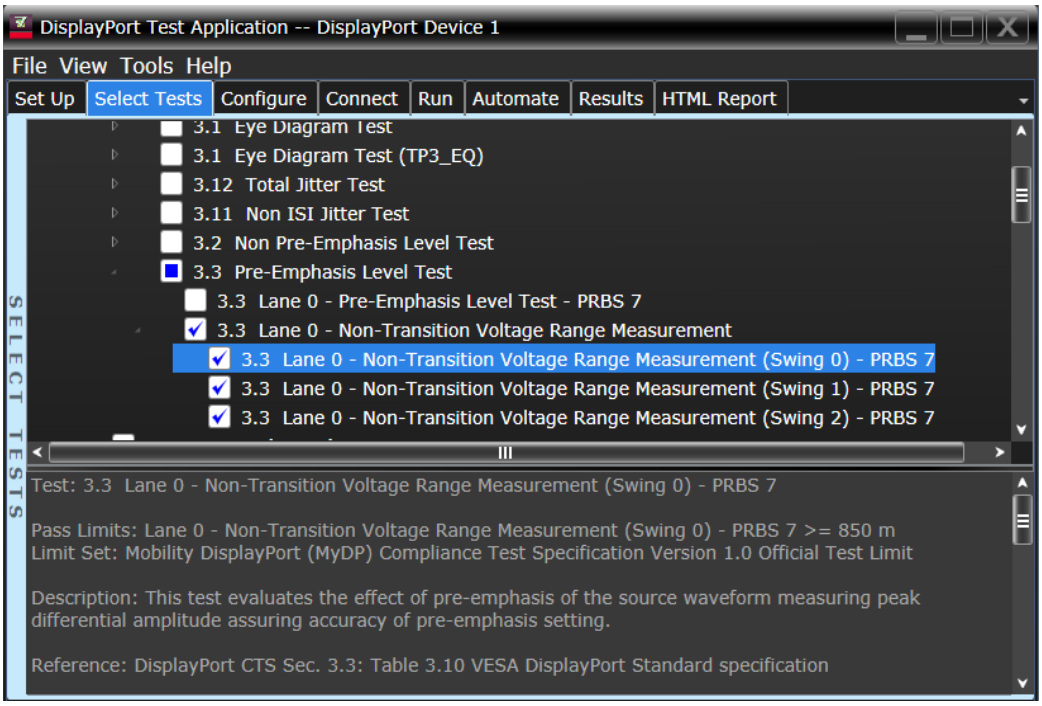
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings. Comparisons are also made for the Level 0 transition state as well as non-transition levels.

Test Conditions for Non Transition Voltage Range Measurement Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR – PRBS7 HBR2 – PLTPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given Voltage Level, repeat the following steps for all pre-emphasis levels subjected to constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

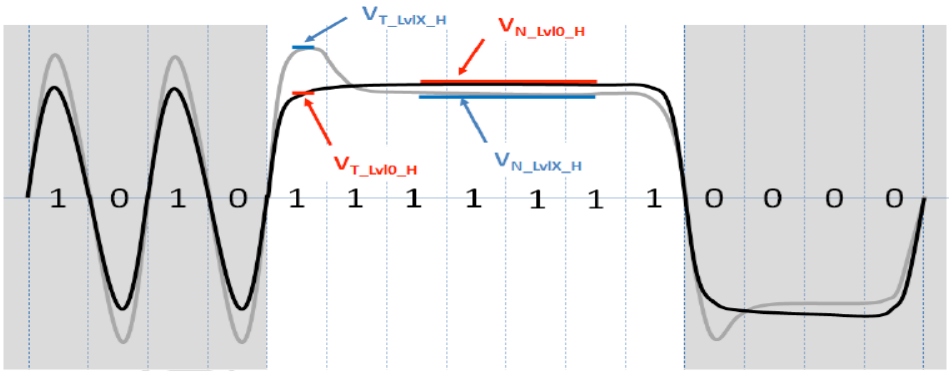


Figure 210 High Voltage measurement for RBR and HBR

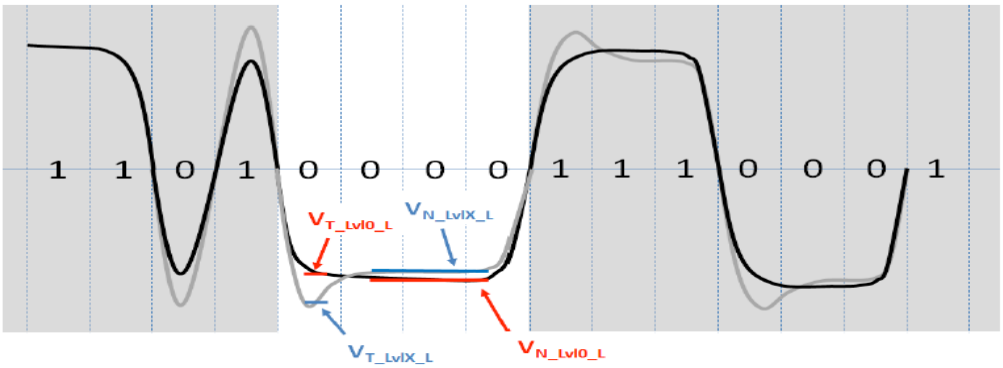


Figure 211 Low Voltage measurement for RBR and HBR

e For HBR2 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted zeros of the pattern.

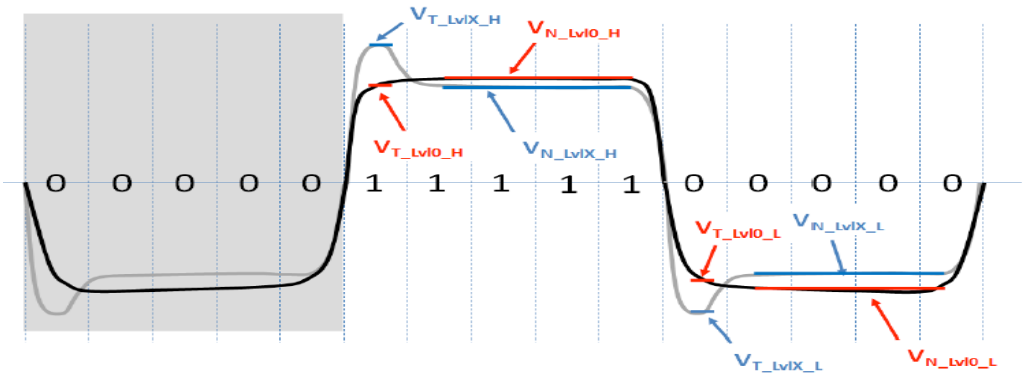


Figure 212 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

2 Calculate the non transition voltage range using the equation:

$$\text{Non Transition Voltage Range} = \text{Minimum } [(V_{N\_LvlX\_PP}) / (V_{N\_Lvl0\_PP})]$$

where, $V_{N\_LvlX\_PP}$) refers to all supported pre-emphasis levels (Level1, Level2, Level3 and so on up to Level X).

3 Report the measurement results.

PASS Condition

Non-Transition Voltage Range Measurements

For Level 2 voltage setting: Resultant $\geq$ 0.708 OR 20*log(Resultant) > -3dB

For Level 1 voltage setting: Resultant $\geq$ 0.708 OR 20*log(Resultant) > -3dB

For Level 0 voltage setting: Resultant $\geq$ 0.85 OR 20*log(Resultant) > -1.4dB

Table 223 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX-DIFF\_REDUCTION}$	Non-transition reduction Output Voltage Level 2	-	-	3	dB	$V_{TX-DIFF}$ at each non-zero nominal pre-emphasis level must not be lower than the specified amount less than $V_{TX-DIFF}$ at the zero nominal pre-emphasis level.
	Non-transition reduction Output Voltage Level 1	-	-	3	dB	
	Non-transition reduction Output Voltage Level 0	-	-	1.4	dB	

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured output voltage level reduction of the non transition bit for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Peak to Peak Voltage Test

Test ID

For RBR and HBR:

- 1266001 – Peak to Peak Voltage Test

For HBR2:

- 1266101 – Peak to Peak Voltage Test

Test Overview

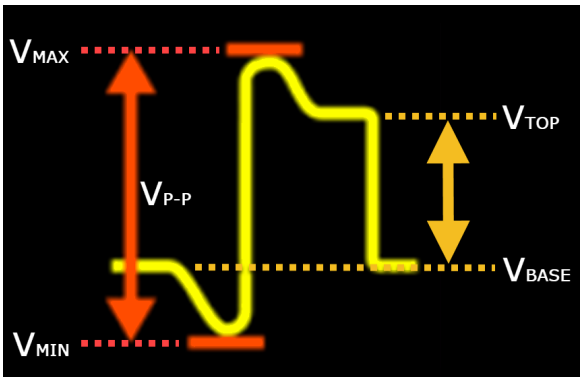
The objective of this test is to evaluate the maximum differential peak to peak voltage.

NOTE

The peak to peak voltage (V_{P-P}) formula is:

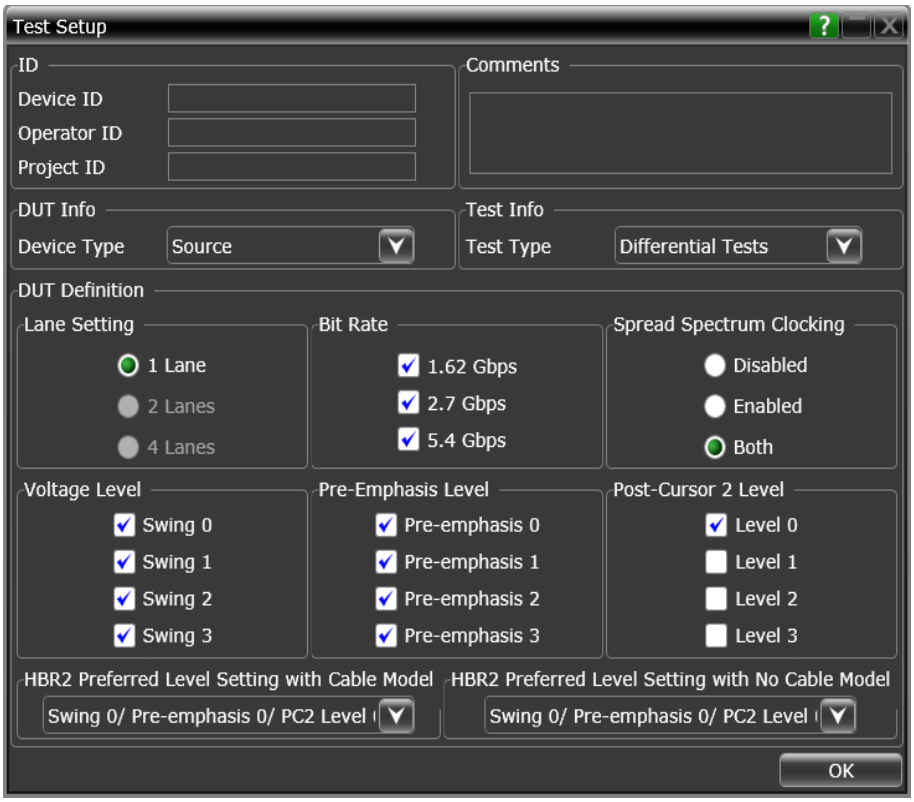
$$V_{P-P} = V_{MAX} - V_{MIN}$$

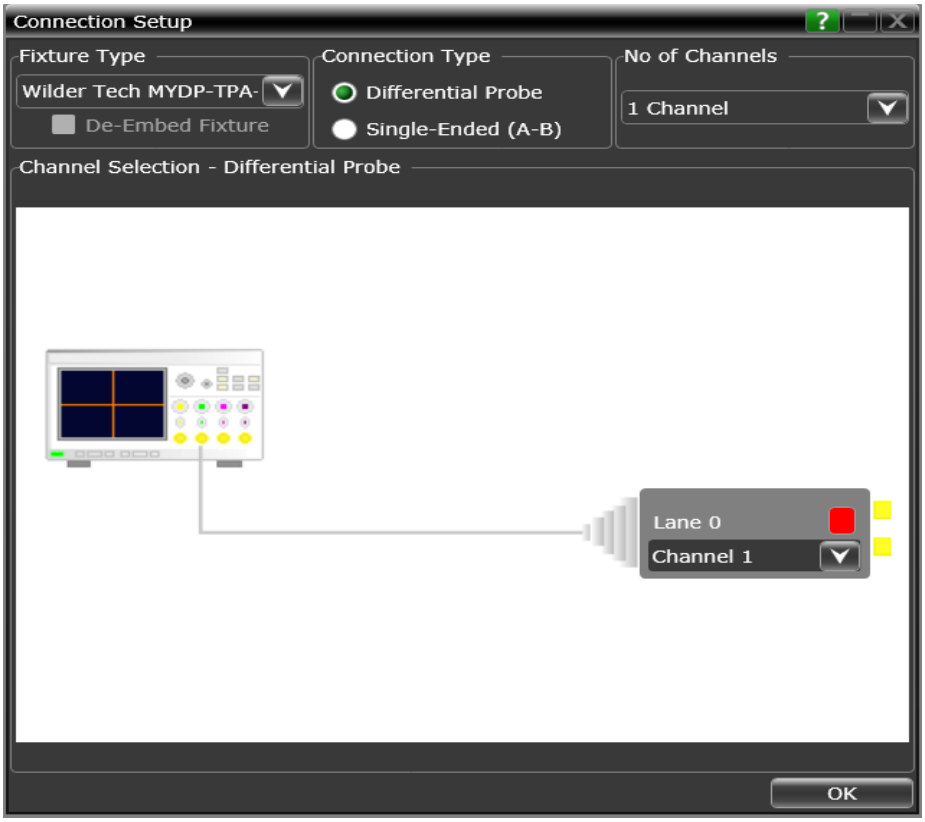
Please see the figure below for more info.

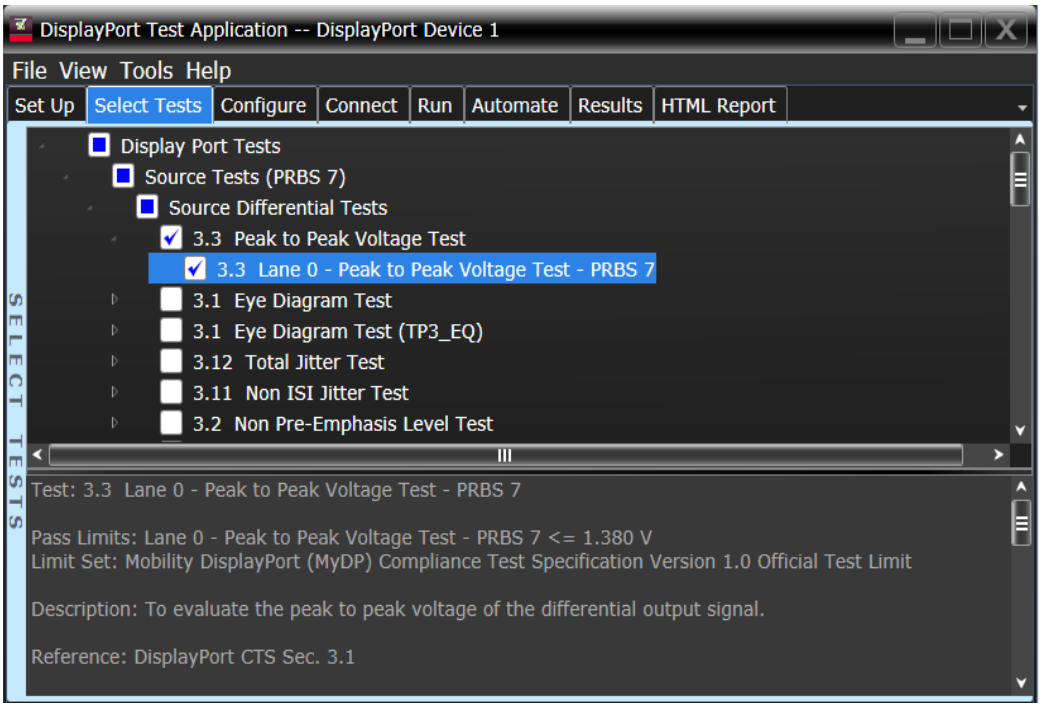


Test Conditions for Peak to Peak Voltage Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR – PRBS7 HBR2 – PLTPAT




Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
Display Port Tests
Source Tests (PRBS 7)
Source Differential Tests
3.3 Peak to Peak Voltage Test
3.3 Lane 0 - Peak to Peak Voltage Test - PRBS 7
3.1 Eye Diagram Test
3.1 Eye Diagram Test (TP3_EQ)
3.12 Total Jitter Test
3.11 Non ISI Jitter Test
3.2 Non Pre-Emphasis Level Test
SELECT TESTS
Test: 3.3 Lane 0 - Peak to Peak Voltage Test - PRBS 7
Pass Limits: Lane 0 - Peak to Peak Voltage Test - PRBS 7 <= 1.380 V
Limit Set: Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0 Official Test Limit
Description: To evaluate the peak to peak voltage of the differential output signal.
Reference: DisplayPort CTS Sec. 3.1

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{MAX} and V_{MIN} of the input signal.
   d Measure the data rate of the input signal.
3 Measure the maximum and minimum voltage of the input signal.
4 Calculate the peak to peak voltage using the equation:

$$\text{Peak to Peak Voltage} = V_{MAX} - V_{MIN}$$

5 Report the measurement results.

PASS Condition

For all Data Rates:

Maximum Differential Peak to Peak Voltage $\leq$ 1.38V

Table 224 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX\text{-}DIFFp\text{-}p\_MAX}$	Max Output Voltage Level	-	-	1.38	V	For all Output Level and Pre-emphasis combinations.

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured peak to peak voltage for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Main Link Frequency Compliance Test

Test ID

12193001 – Main Link Frequency Compliance

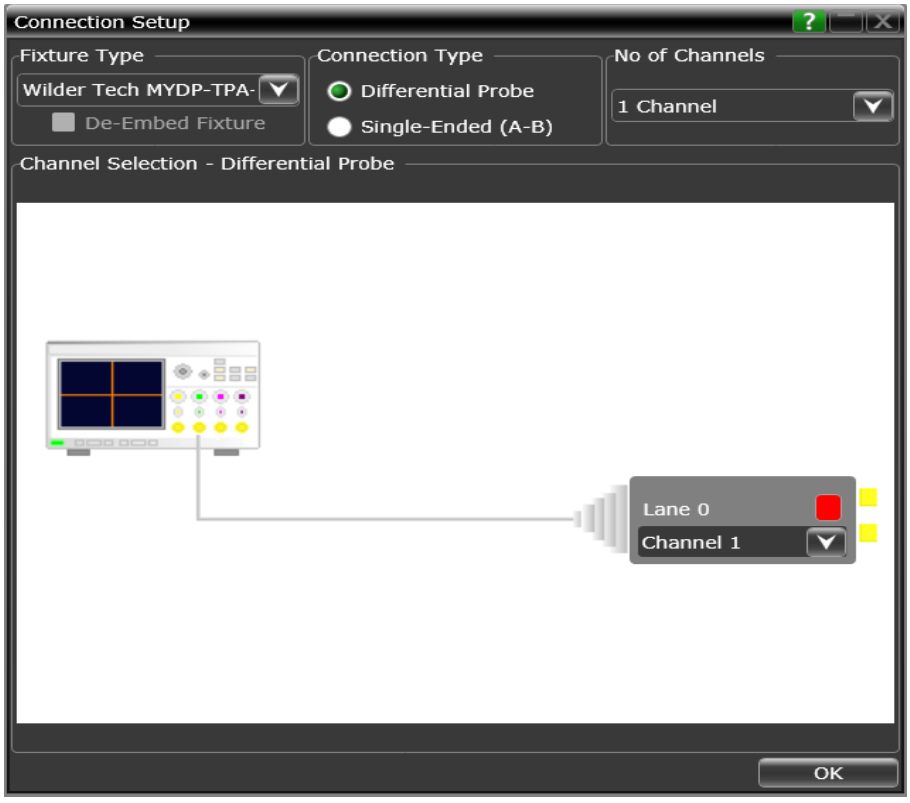
Test Overview

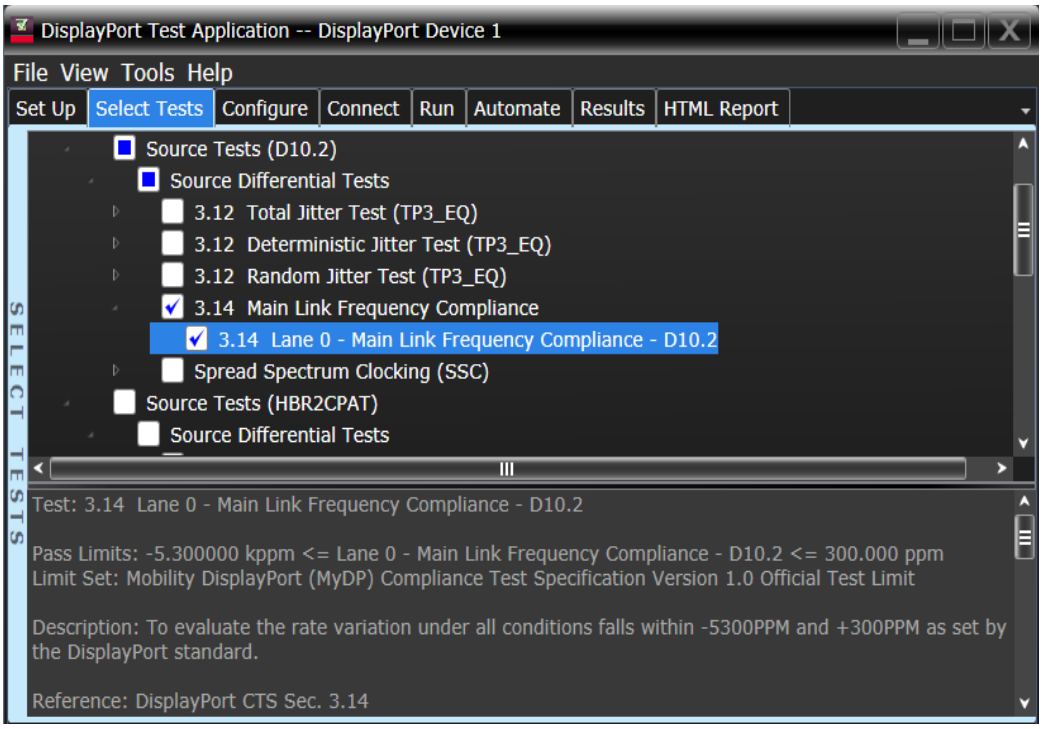
The objective of this test is to ensure that the average data rate under all conditions does not exceed the minimum and maximum values as set by the VESA DisplayPort 1.2a Standard.

Test Conditions for Main Link Frequency Compliance Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.

5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and the minimum measurement levels for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurement levels for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e For SSC Enabled Test condition, check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.
9 For the test condition “SSC Enabled”, set up the parameter of the SSC measurement:
   a Set up the memory depth and time-base to display one complete SSC cycle based on the measured SSC modulation frequency in Step 5.
   b Acquire the signal with one complete SSC cycle.
   c Get the minimum of FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

      Maximum Data Rate = 1 / (Minimum Unit Interval)

   d Get the maximum of FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

      Minimum Data Rate = 1 / (Maximum Unit Interval)

   e Repeat steps b, c and d until you acquire 10 SSC Cycles.
   f Calculate the mean value for the maximum and minimum data rates.
10 Report the measurement results.

PASS Condition

Maximum Data Rate (Frequency Max_{ppm}) $\leq$ 300 ppm

Minimum Data Rate (Frequency Min_{ppm}) $\geq$ -5300 ppm

Table 225 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
f_{HBR2}	Frequency for High Bit Rate 2	5.37138	5.4	5.40162	Gbps	Frequency high limit = +300ppm Frequency low limit = -5300ppm
f_{HBR}	Frequency for High Bit Rate	2.68569	2.7	2.70081	Gbps	
f_{RBR}	Frequency for Reduced Bit Rate	1.611414	1.62	1.620486	Gbps	

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.14*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured data rate for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Frequency Test

Test ID

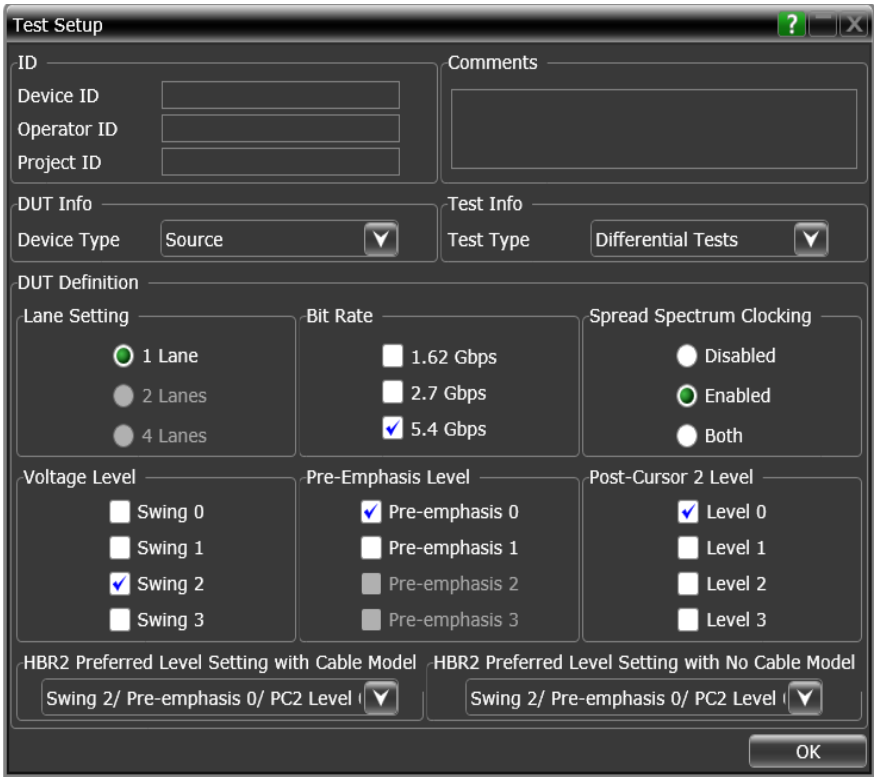
12170001 – SSC Modulation Frequency Test

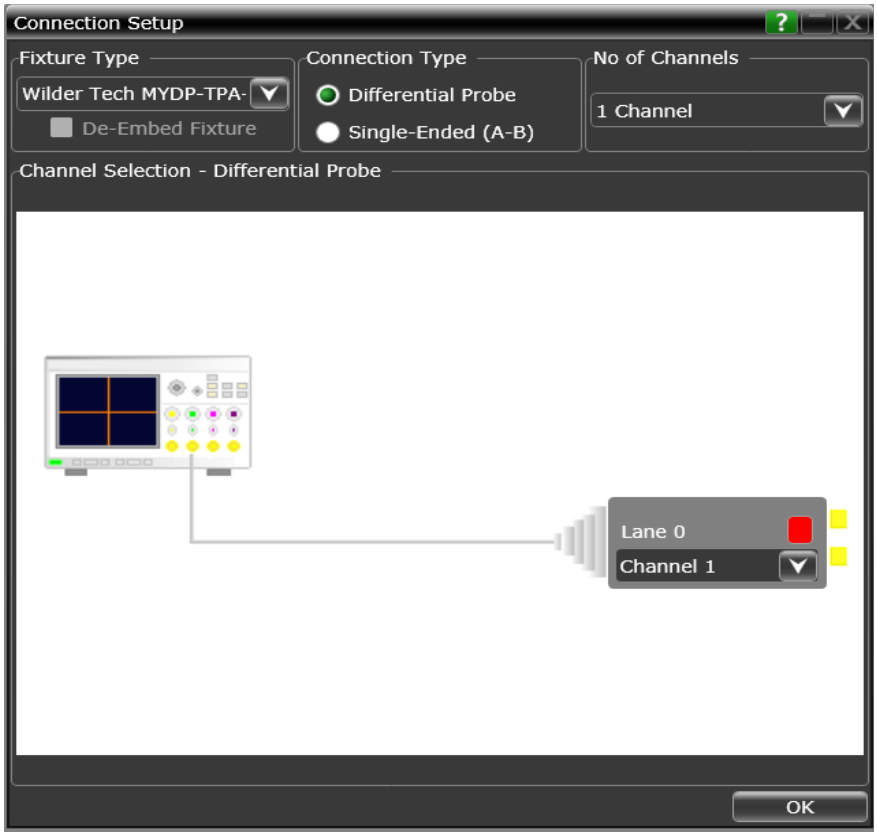
Test Overview

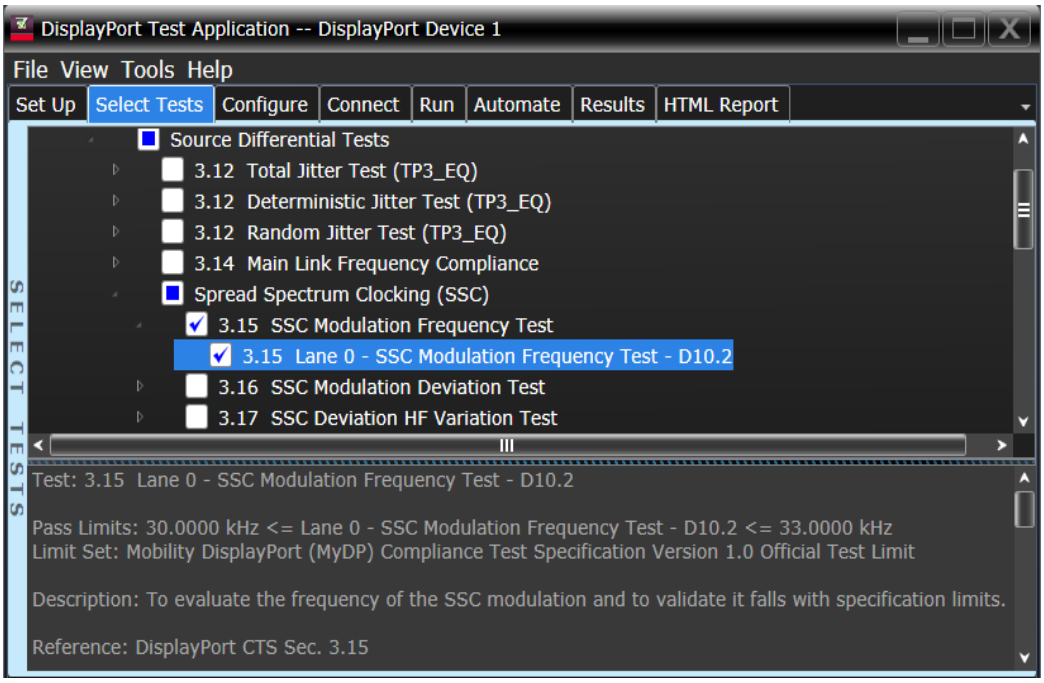
The objective of this test is to evaluate the frequency of the SSC modulation and to validate that the frequency is within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. Calculate the SSC modulation frequency from the average of the measured SSC modulation frequency for each cycle.

Test Conditions for SSC Modulation Frequency Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.

5 Set up the parameters for the frequency measurement.

a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.

b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.

c Set up the memory depth and time-base using the settings defined in the Configuration Variable.

d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.

e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).

f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.

g Acquire the signal for 10 SSC Cycles.

6 Get the mean value for the SSC Modulation frequency.

7 Report the measurement results.

PASS Condition

30kHz $\leq$ SSC Modulation Frequency (f_{SSC}) $\leq$ 33kHz

Table 226 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
Down_Spread_Frequency	Link clock down-spreading frequency	30	-	33	kHz	Range: 30kHz ~ 33kHz when down-spread enabled

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.15*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured SSC modulation frequency for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Deviation Test

Test ID

12180001 – SSC Modulation Deviation Test

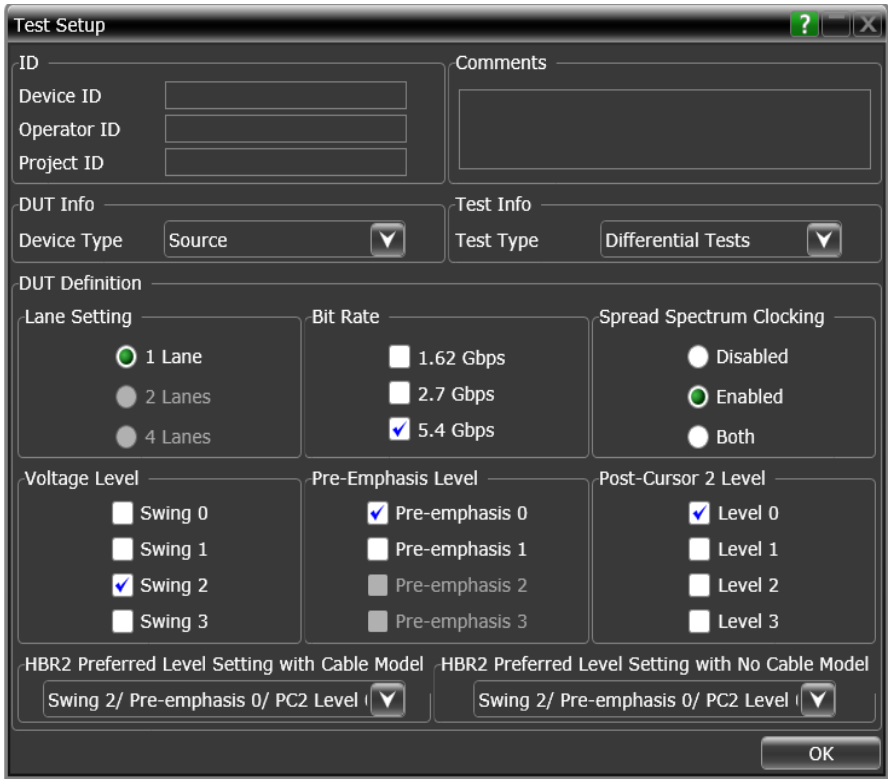
Test Overview

The objective of this test is to evaluate the range of SSC down-spreading of the transmitter signal in ppm and to validate that the values are within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. For each cycle, the minimum and maximum data rate is evaluated. Calculate the SSC modulation deviation from the average of the maximum minus the average of the minimum using the equation:

SSC Modulation Deviation = {[Average (Minimum Data Rate) - Average (Maximum Data Rate)] / Nominal Data Rate}*1E+6

Test Conditions for SSC Modulation Deviation Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	D10.2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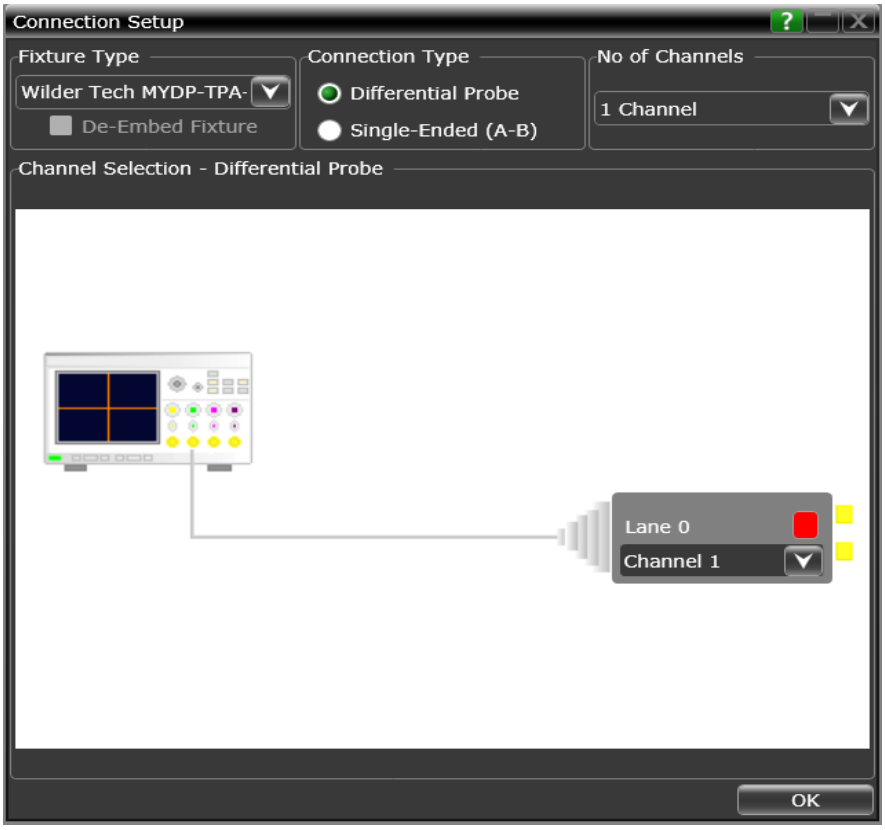
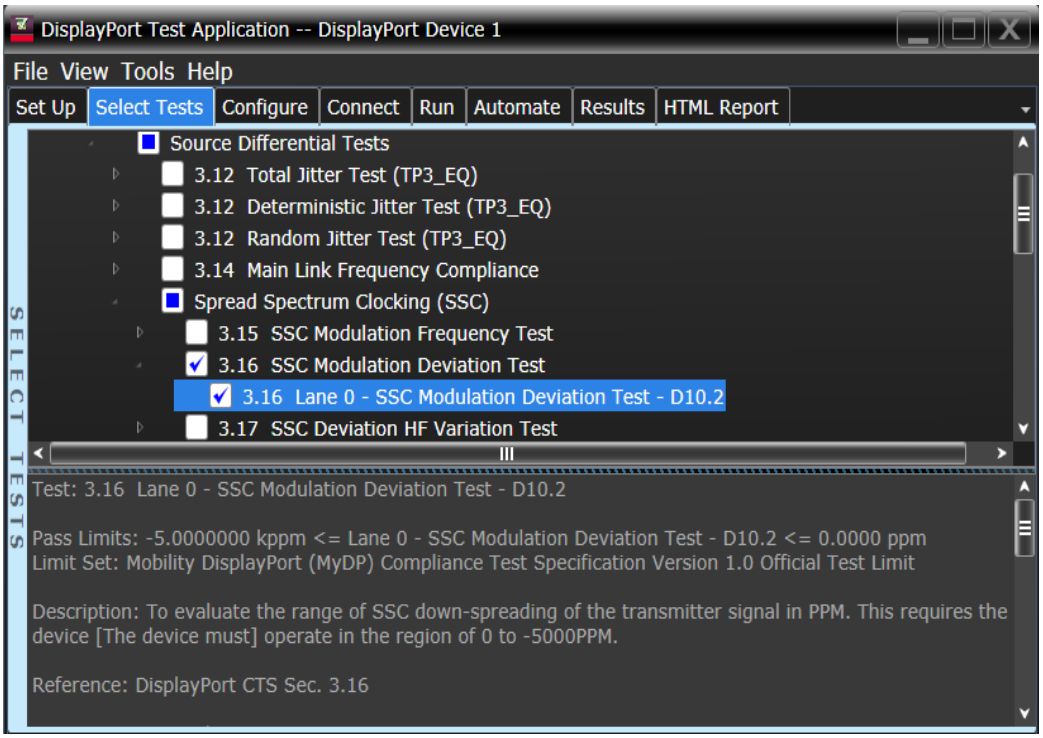
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.

5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and minimum measurements for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurements for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e Check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point for three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 filtered unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurements for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.
9 Set up the parameters for SSC measurement.
   a Set up memory depth and time-base to display one complete SSC Cycle based on the measured SSC modulation frequency in step 5.
   b Acquire the signal with one complete SSC Cycle.
   c Get the minimum of the FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

      Maximum Data Rate = 1/Minimum Unit Interval

   d Get the maximum of the FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

      Minimum Data Rate = 1/Maximum Unit Interval

   e Repeat step b,c and d until you acquire 10 SSC Cycles.
   f Calculate the mean value for the maximum and minimum data rate.
10 Calculate the SSC Modulation Deviation using the equation:

   SSC Modulation Deviation = {[Average (Minimum Data Rate) - Average (Maximum Data Rate)] / Nominal Data Rate}*1E+6

11 Report the measurement results.

PASS Condition

-5000ppm $\leq$ SSC Modulation Deviation (Resultant$_{SSC\ Range}$) $\leq$ 0ppm

Table 227 DisplayPort Main Link Transmitter System Parameters

Symbol	Parameter	Min	Nom	Max	Unit	Comments
Down_Spread_Amplitude	Link clock down-spreading	0	-	0.5	%	Range: 0% ~ 0.5% when down-spread enabled

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.16*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured SSC modulation deviation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Deviation HF Variation Test (Informative)

Test ID

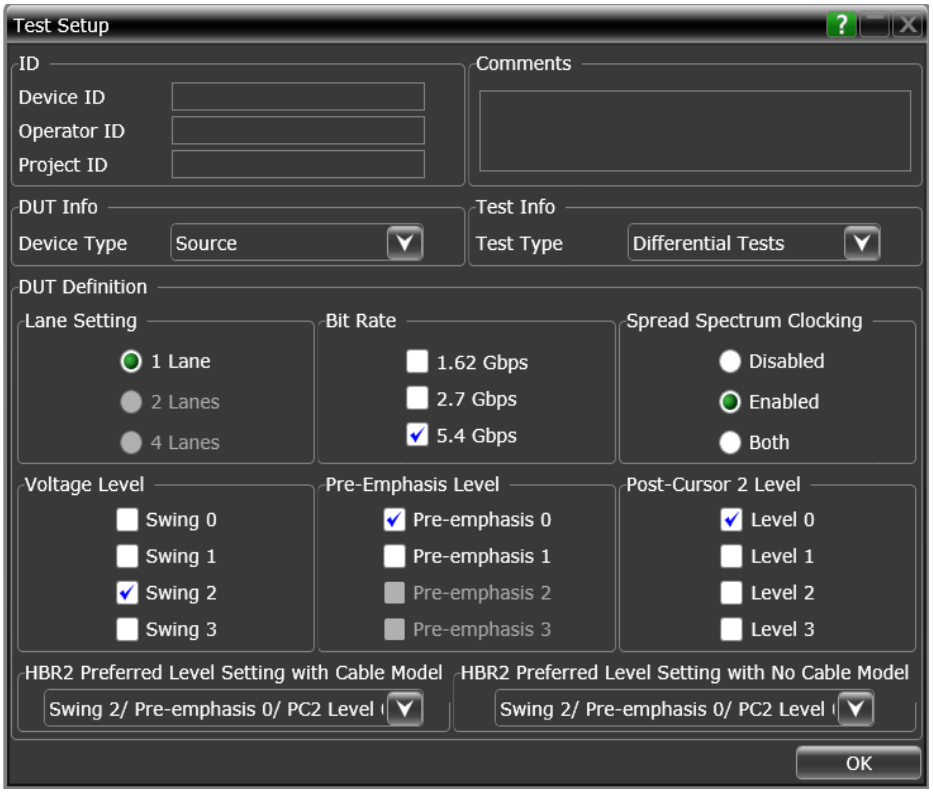
12200001 – SSC Deviation HF Variation Test (Informative)

Test Overview

The objective of this test is to verify that the SSC profile does not include any frequency deviation that may exceed 1250 ppm/µsec. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles.

Test Conditions for SSC Deviation HF Variation Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	D10.2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ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
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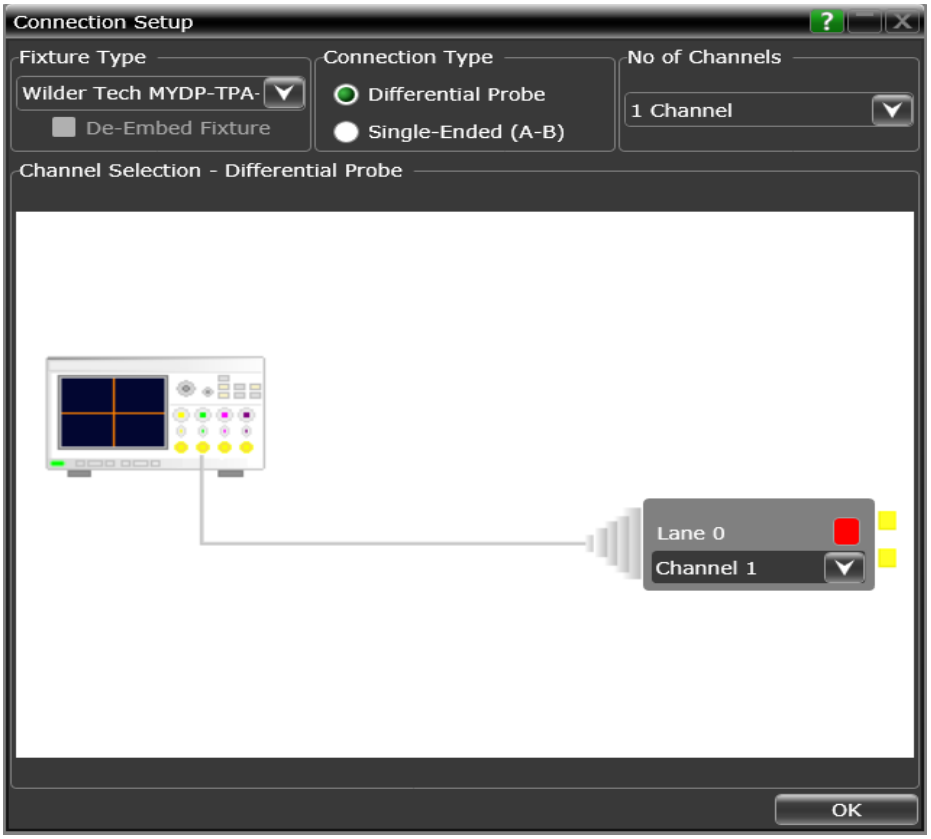
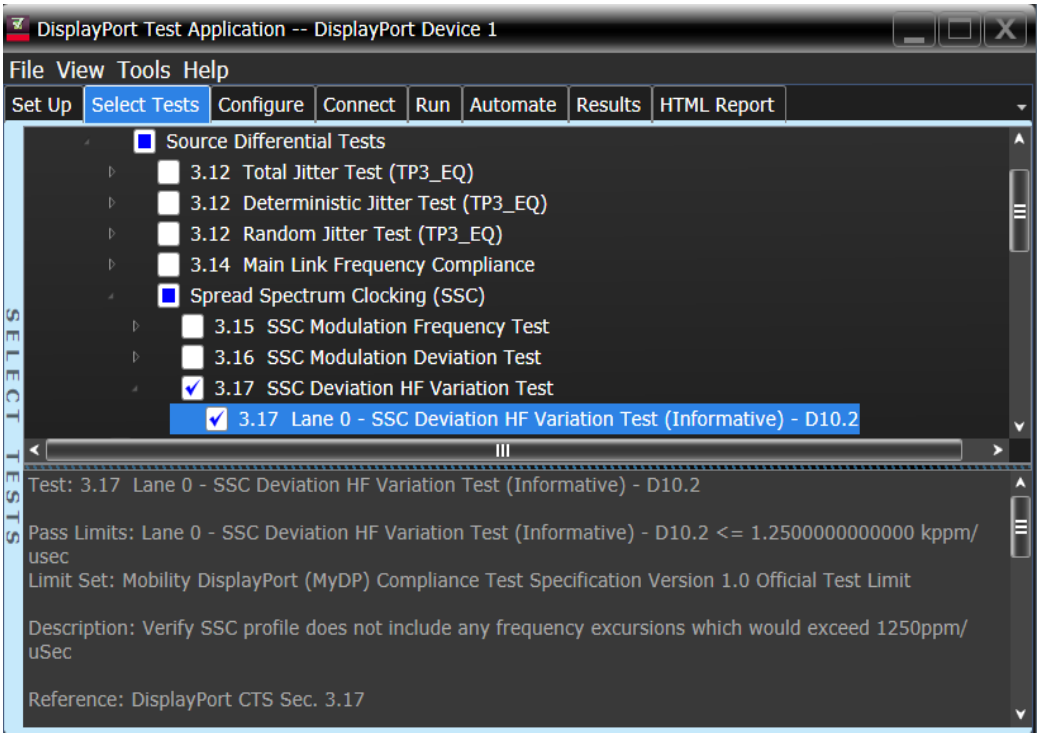
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.

5 Set up the parameters for the frequency measurement.

a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.

b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.

c Set up the memory depth and time-base using the settings defined in the Configuration Variable.

d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.

e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).

f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.

6 Set up the parameters for the SSC measurement.

a Set up memory depth and time-base to display one complete SSC cycle using the measured SSC Modulation Frequency in Step 5.

b Acquire the signal with one complete SSC Cycles.

c Read the FUNC2 filtered unit interval measurement trend.

d Compute the slope using the “Sliding Window” with 1.00 µsec window width. Calculate the slope using the equation:

$$\text{Slope} = [f(t) - f(t-1.00\ \mu\text{sec})/1.00\ \mu\text{sec}]$$

e Repeat step b, c and d until you acquire 10 SSC Cycles.

f Get the maximum value for the computed value of slope.

7 Report the measurement results.

PASS Condition

- SSC_t dF/dt $\leq$ 1250ppm/µsec

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.17*

Expected/Observable Results

The measured SSC deviation high frequency variation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Post-Cursor 2 Verification Test (Informative)

Test ID

1279001 – Post Cursor 2 Verification Test - Level 1/Level 0 (Informative)

1279101 – Post Cursor 2 Verification Test - Level 2/Level 1 (Informative)

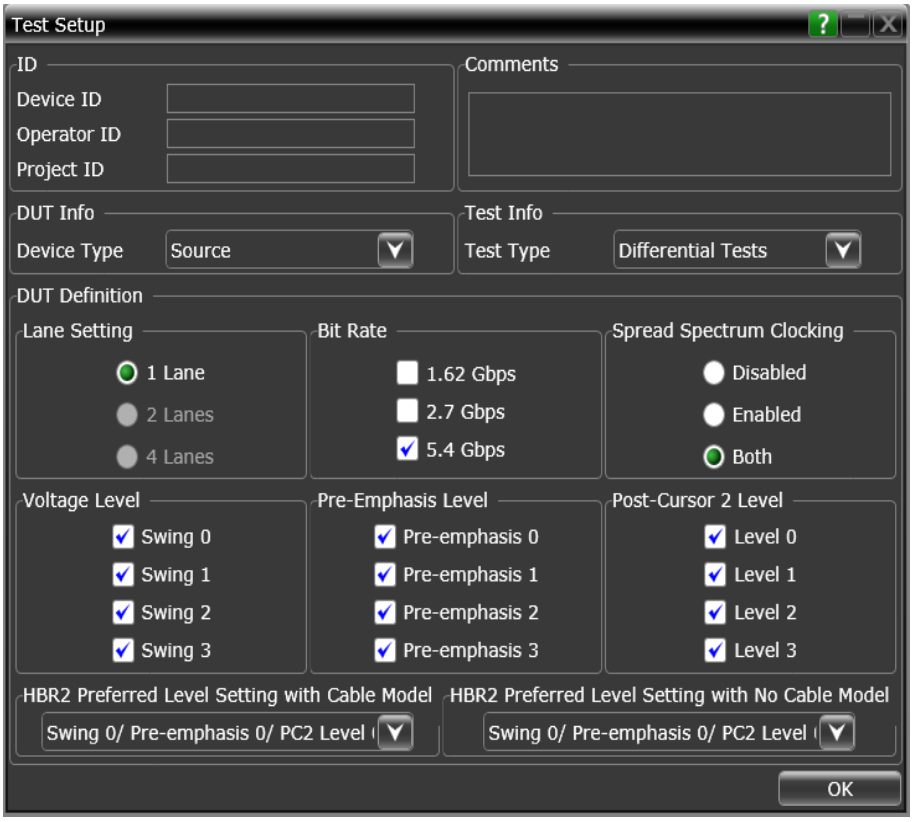
1279201 – Post Cursor 2 Verification Test - Level 3/Level 2 (Informative)

Test Overview

The objective of this test is to evaluate the effect of adding Post-Cursor 2 of the source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor 2 settings.

Test Conditions for Post-Cursor 2 Verification Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	HBR2
SSC	Both SSC conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels supported subject to constraints in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	All Post-Cursor 2 levels supported
Test Lane	Lane 0
Test Pattern	PCTPAT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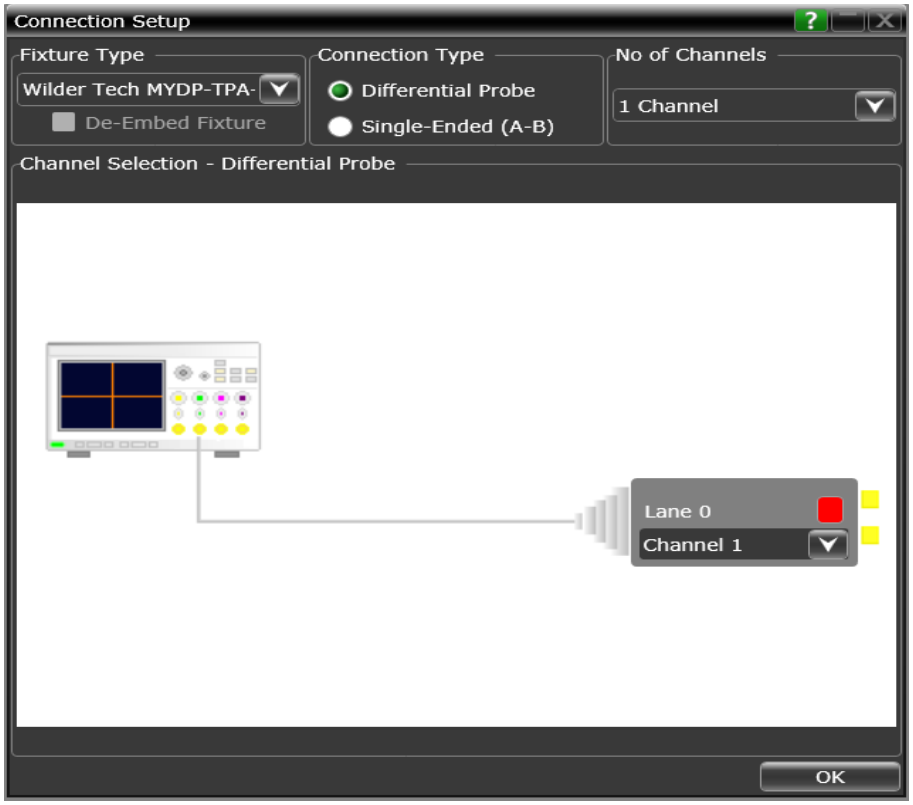
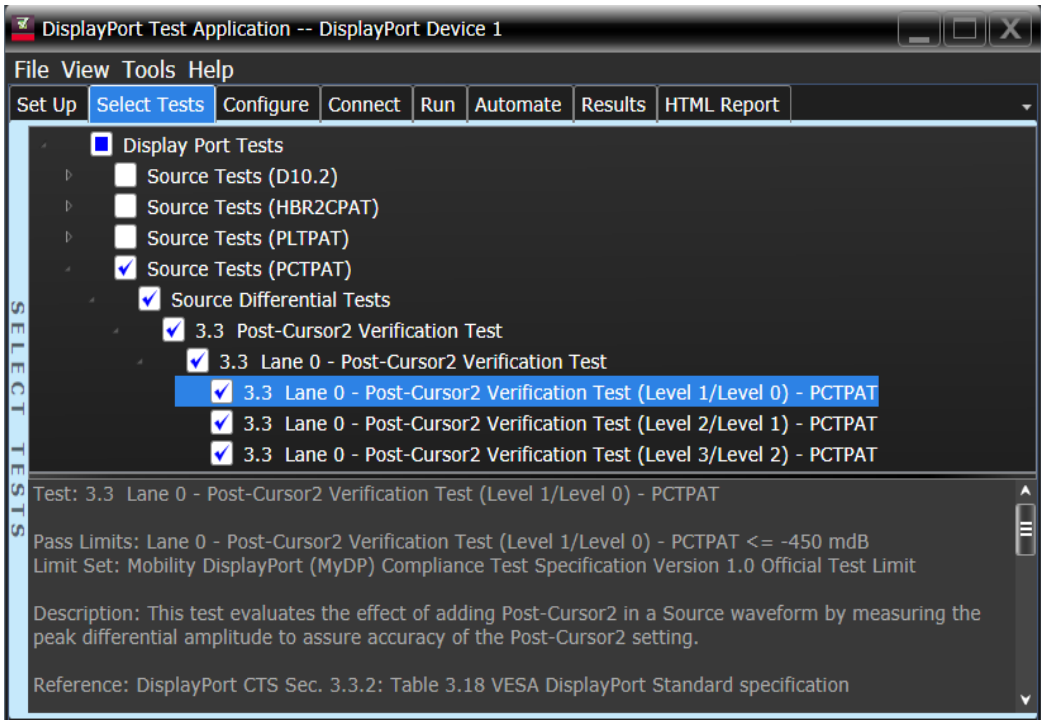
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given Voltage Level, Pre-Emphasis Level and Post-Cursor 2 Level X:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d Pattern fold the input signal based on the qualifying pattern 00101010 for the measurement of voltage $V_{T1010\_PC2\_LvlX\_PP}$ in the test pattern PLTPAT.

e Set up the vertical waveform histogram on the input signal at the points specified below to measure the High voltage $V_{T1010\_PC2\_LvlX\_H}$ and Low Voltage $V_{T1010\_PC2\_LvlX\_L}$.

i $V_{T1010\_PC2\_LvlX\_H}$ is the average value over the 40% to 70% UI points in the fifth relevant bit (1s bit) in the 1010 portion of the qualifying pattern.

ii $V_{T1010\_PC2\_LvlX\_L}$ is the average value over the 40% to 70% UI points in the sixth relevant bit (0s bit) in the 1010 portion of the qualifying pattern.

f Calculate the peak-to-peak voltage $V_{T1010\_PC2\_LvlX\_PP}$ using the equation:

$$V_{T1010\_PC2\_LvlX\_PP} = V_{T1010\_PC2\_LvlX\_H} - V_{T1010\_PC2\_LvlX\_L}$$

g Pattern fold the input signal based on the qualifying pattern 00011001100 for the measurement of voltage $V_{T1100\_PC2\_LvlX\_PP}$ in the test pattern PLTPAT.

h Set up the vertical waveform histogram on the input signal at the points specified below to measure the High voltage $V_{T1100\_PC2\_LvlX\_H}$ and Low Voltage $V_{T1100\_PC2\_LvlX\_L}$.

i $V_{T1100\_PC2\_LvlX\_H}$ is the average value over the 40% to 70% UI points in the fifth relevant bit (1s bit) in the 1100 portion of the qualifying pattern.

ii $V_{T1100\_PC2\_LvlX\_L}$ is the average value over the 40% to 70% UI points in the sixth relevant bit (0s bit) in the 1100 portion of the qualifying pattern.

i Calculate the peak-to-peak voltage $V_{T1100\_PC2\_LvlX\_PP}$ using the equation:

$$V_{T1100\_PC2\_LvlX\_PP} = V_{T1100\_PC2\_LvlX\_H} - V_{T1100\_PC2\_LvlX\_L}$$

j Calculate the Post-Cursor 2 ratio using the equation:

$$\text{Post-Cursor 2 Ratio}_{LvlX} = V_{T1100\_PC2\_LvlX\_PP} / V_{T1010\_PC2\_LvlX\_PP}$$

2 Compare the pre-emphasis delta of Post-Cursor 2 Level with the limits by repeating Step 1 with another Post-Cursor2 Level.

3 Calculate the pre-emphasis delta of Post-Cursor 2 Level using the equation:

$$\text{Post-Cursor 2 Delta (Level 1 vs Level 0)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl1} / \text{Post-Cursor 2 Ratio}_{Lvl0}]$$

$$\text{Post-Cursor 2 Delta (Level 2 vs Level 1)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl2} / \text{Post-Cursor 2 Ratio}_{Lvl1}]$$

$$\text{Post-Cursor 2 Delta (Level 3 vs Level 2)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl3} / \text{Post-Cursor 2 Ratio}_{Lvl2}]$$

4 Report the measurement results.

PASS Condition

Post Cursor 2 Verification Measurements

For Level 1 vs. Level 0 Pre-emphasis Post Cursor 2 settings: $\text{Resultant}_{Lvl0\_to\_Lvl1} < -0.45$ dB

For Level 2 vs. Level 1 Pre-emphasis Post Cursor 2 settings: $\text{Resultant}_{Lvl1\_to\_Lvl2} < -0.5$ dB

For Level 3 vs. Level 2 Pre-emphasis Post Cursor 2 settings: $\text{Resultant}_{Lvl2\_to\_Lvl3} < -0.6$ dB

Table 228 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX\text{-}PREEMP\_POST2\text{-}DELTA}$	Delta of Pre-emphasis Post Cursor2 Level 1 vs. Level 0	-0.45	-	-	dB	Measured on 2nd TBIT at Pre-emphasis Level 0
	Delta of Pre-emphasis Post Cursor2 Level 2 vs. Level 1	-0.5	-	-	dB	Support for Pre-emphasis Post Cursor2 is optional
	Delta of Pre-emphasis Post Cursor2 Level 3 vs. Level 2	-0.6	-	-	dB	

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2a, Section 3.3.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured pre-emphasis delta of Post-Cursor 2 for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Eye Diagram Test (TP3_EQ)

Test ID

For HBR

- 1211001 – Eye Diagram Test (TP3_EQ)
- 1211011 – Eye Diagram Test with No Cable Model (TP3_EQ)

For HBR2

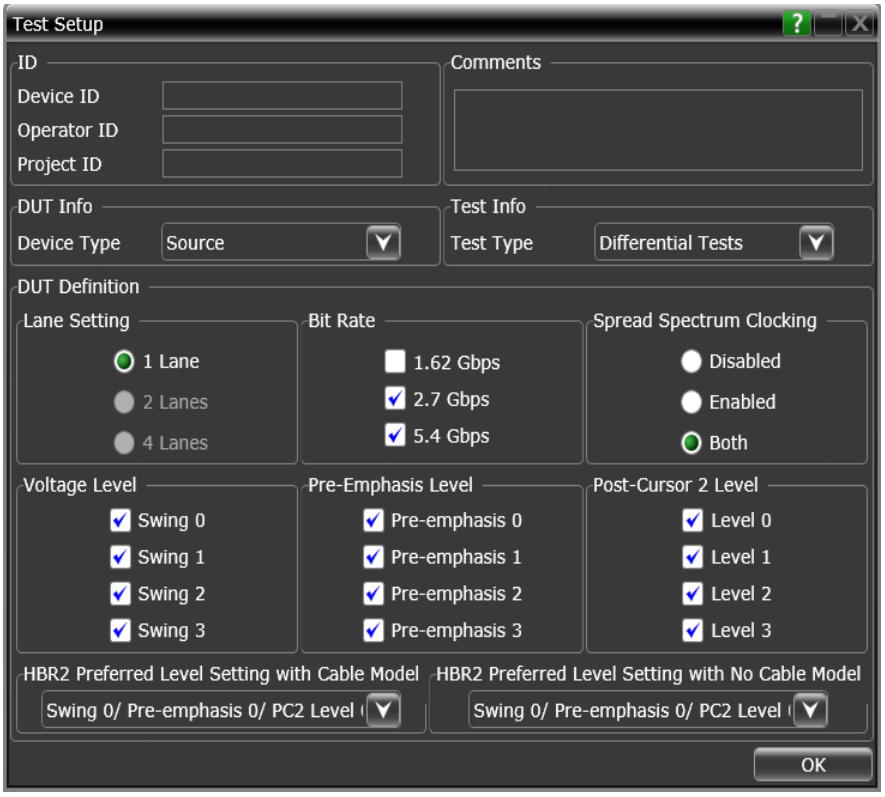
- 1215001 – Eye Diagram Test (TP3_EQ)
- 1215011 – Eye Diagram Test with No Cable Model (TP3_EQ)

Test Overview

The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions for Eye Diagram Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR (Informative) and HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	HBR – Level 2 HBR2 – Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	HBR – Level 0 HBR2 – Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	HBR – Level 0 HBR2 – Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	Lane 0
Test Pattern	HBR–PRBS7 HBR2–HBR2CPAT
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
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Operator ID
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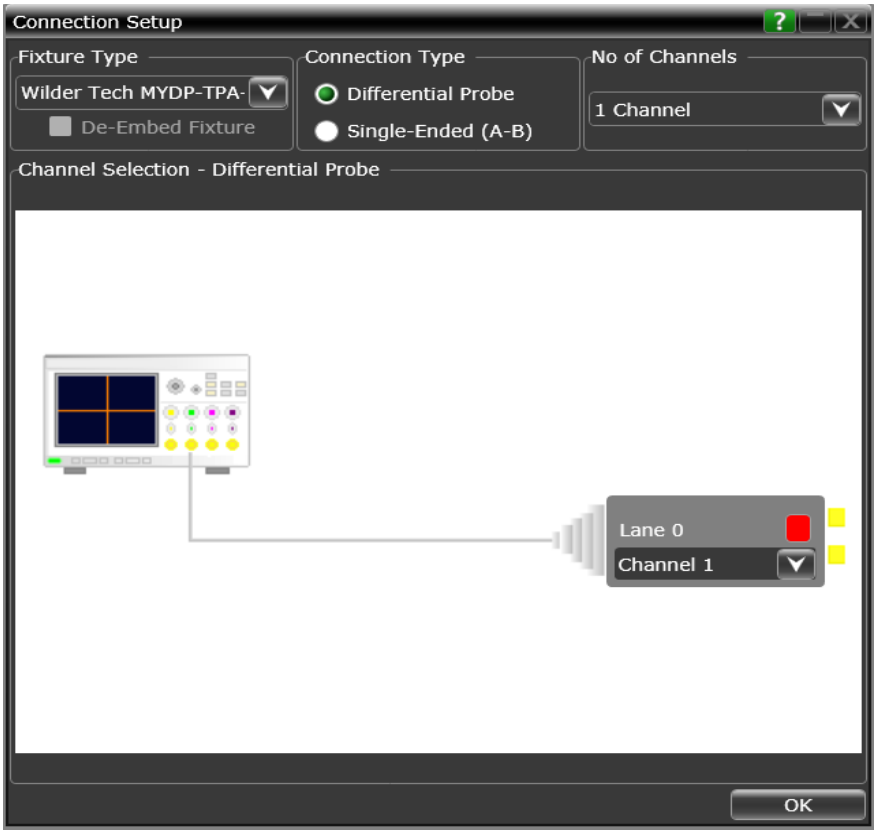
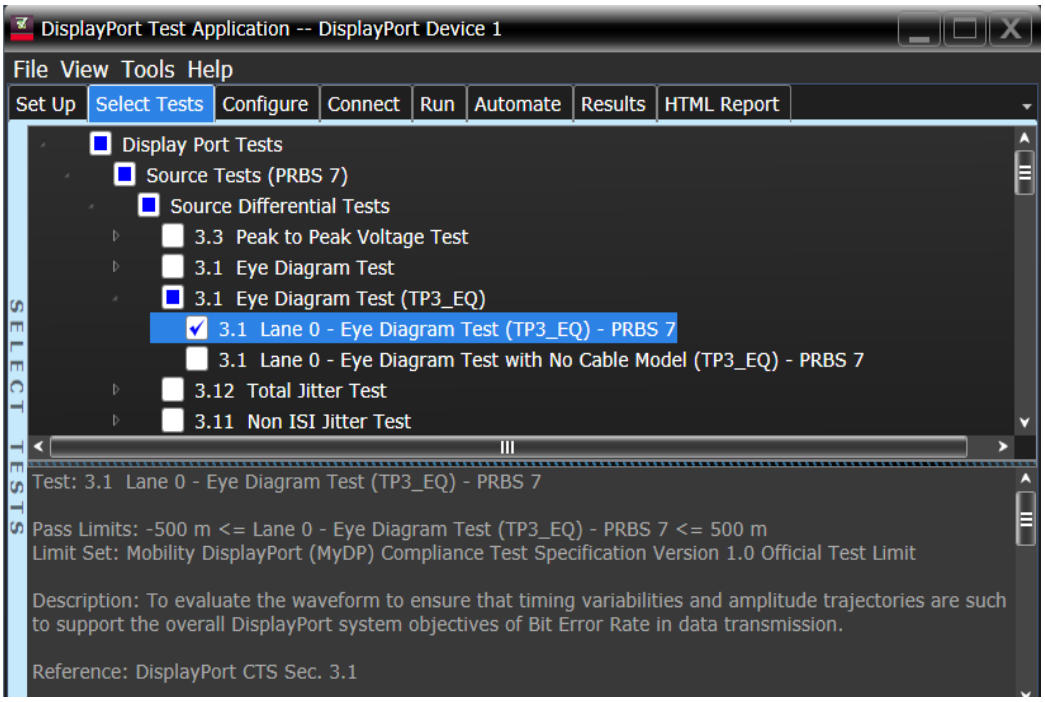
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure for HBR

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.

7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the jitter of the eye diagram using the Histogram.
9 Check for any signal trajectories that may have entered into the mask.
10 Report the measurement results.

Measurement Procedure for HBR2

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]:
   a Pattern fold the equalized signal based on the High Level Voltage (V_{HIGH}) random noise configuration variable.
   b Set up the vertical waveform histogram on the equalized signal to measure random noise of High Level Voltage (V_{HIGH}).
   c Measure the High Level Voltage (V_{HIGH}) random noise based on the standard deviation of the waveform histogram.
   d Pattern fold the equalized signal based on the Low Level Voltage (V_{LOW}) random noise configuration variable.
   e Set up the vertical waveform histogram on the equalized signal to measure the random noise of Low Level Voltage (V_{LOW}).
   f Measure the Low Level Voltage (V_{LOW}) random noise based on the standard deviation of the waveform histogram.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge and right edge.
8 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.

9 Find the maximum eye height location of the eye diagram.

10 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:

a Set up the parameter of the jitter separation using the EZJIT Plus/Complete Software.

i Load the jitter separation parameter into EZJIT Plus/Complete Software based on the settings in the Configuration Variable.

ii Acquire the signal until 1,000,000 edges are analyzed.

b Note the value of the jitter component from the EZJIT Plus/Complete Software.

11 Create the eye mask based on the following criteria:

a If you select more than one lane (2 lanes or 4 lanes DUT configuration), the eye mask height and width is derate in the following manner, to include crosstalk as defined in DisplayPort 1.2b Compliance Test Specification:

i Eye Mask Width Derate (Crosstalk) = 0.04 UI

ii Eye Mask Height Derate (Crosstalk) = 0.014V

b If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]: eye mask height and width is derate as below to comprehend the noise/jitter extrapolated to BER 10^{-9} for an Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI:

i Calculate the Eye Mask Width Derate (Random Jitter) using the equation:

$$\text{Eye Mask Width Derate (Random Jitter)} = 2.5 * \text{Random Jitter}_{rms}$$

ii Calculate the Eye Mask Height Derate (Random Noise) using the equation:

$$V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{HIGH}\ \text{Random Noise}_{rms}$$

$$V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{LOW}\ \text{Random Noise}_{rms}$$

NOTE The factor 2.5 is the delta between BER 10^{-6} (9.507) and 10^{-9} (11.996) to comprehend the noise/jitter extrapolated to BER 10-9 as the Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI.

BER	N
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996

c Place the eye mask height at the point of the maximum eye height found in Step 9.

d Calculate the Eye Mask Width:

$$\text{Eye Mask Width} = \text{Eye Width Specification (0.38 UI)} + \text{Eye Mask Width Derate (Crosstalk)} + 2 * \text{Eye Mask Width Derate (Random Jitter)}$$

e Calculate the Eye Mask Height:

$$\text{Eye Mask Height} = \{\text{Eye Height Specification (0.09 V)} + \text{Eye Mask Height Derate (Crosstalk)}\}/2 + V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)}$$

$$\text{Eye Mask Height} = -\{\text{Eye Height Specification (0.09 V)} + \text{Eye Mask Height Derate (Crosstalk)}\}/2 - V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)}$$

12 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram.
   c Run the eye mask until 1,000,000 UI are folded.
13 Measure the eye height of the eye diagram using the Histogram.
14 Measure the jitter of the eye diagram using the Histogram.
15 Calculate the eye width based on the measured jitter of the eye diagram.
16 Check for any signal trajectories that may have entered into the mask.
17 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 229 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 229 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

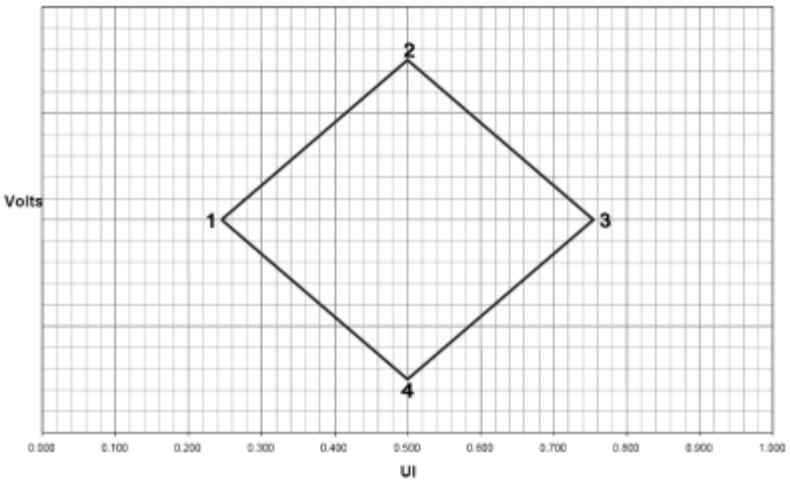


Figure 213 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 230 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	*0.045
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	*-0.045

NOTE

*Eye height limit of 45 mV and -45 mV assumes cross-talk as 0, which is only possible in case of single lane testing.

In case of multi-lane testing, cross talk exists, and the eye height values deviate by ± 7 mV. Thus the eye height becomes (+45 +7) mV and (-45 -7) mV or +52 mV and -52 mV.

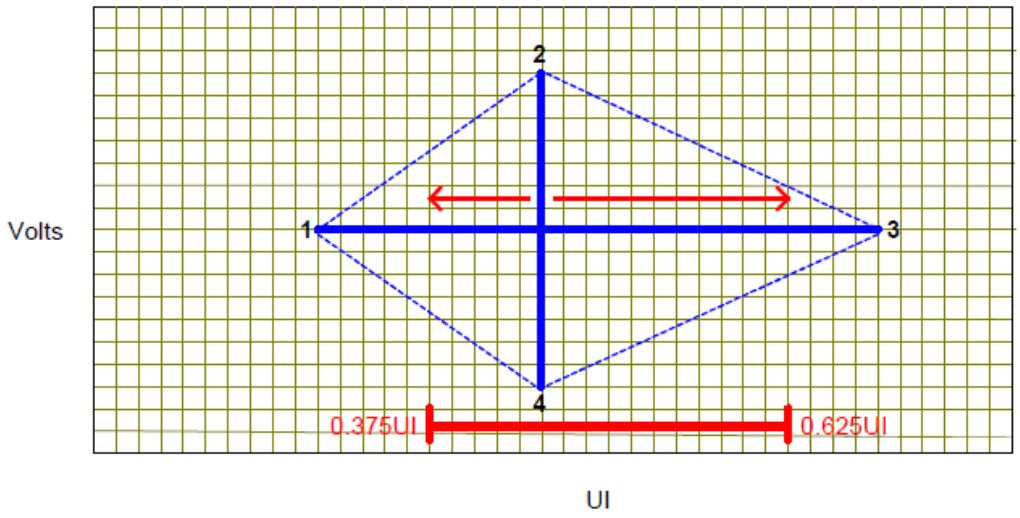


Figure 214 The Sink Eye Mask at TP3_EQ (HBR2)

Mask Test: Zero mask failures.

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test (TP3_EQ)

Test ID

For HBR2:

- 1222001 – Total Jitter Test (TP3_EQ) – HBR2CPAT
- 1222011 – Total Jitter Test with No Cable Model (TP3_EQ) – HBR2CPAT
- 1221001 – Total Jitter Test (TP3_EQ) – D10.2
- 1221011 – Total Jitter Test with No Cable Model (TP3_EQ) – D10.2

Test Overview

The objective of this test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

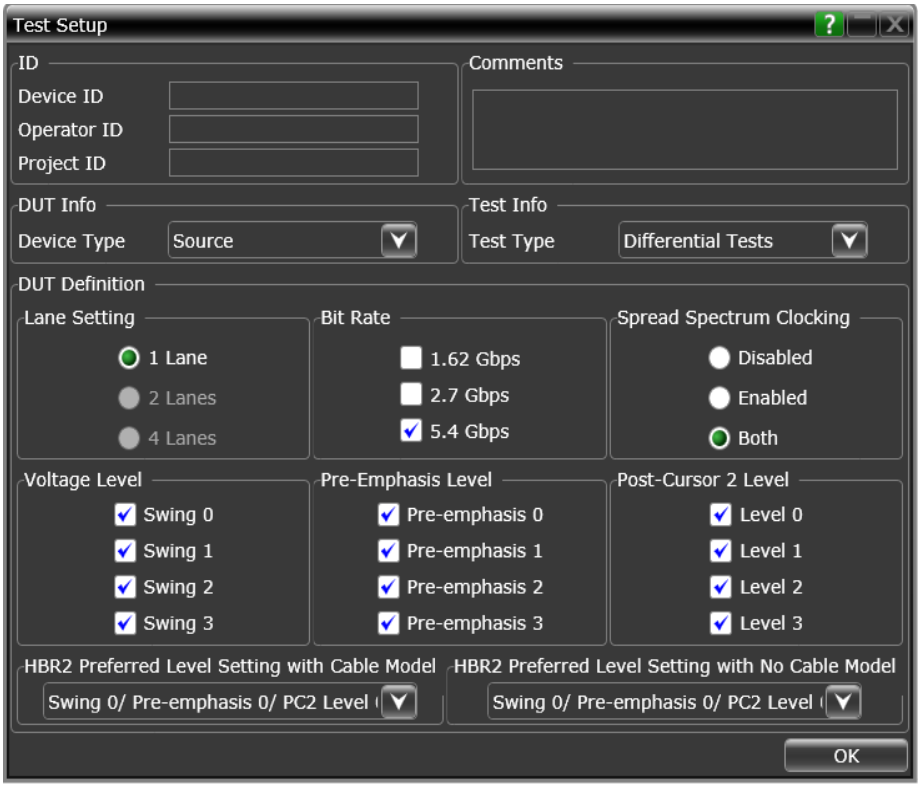
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

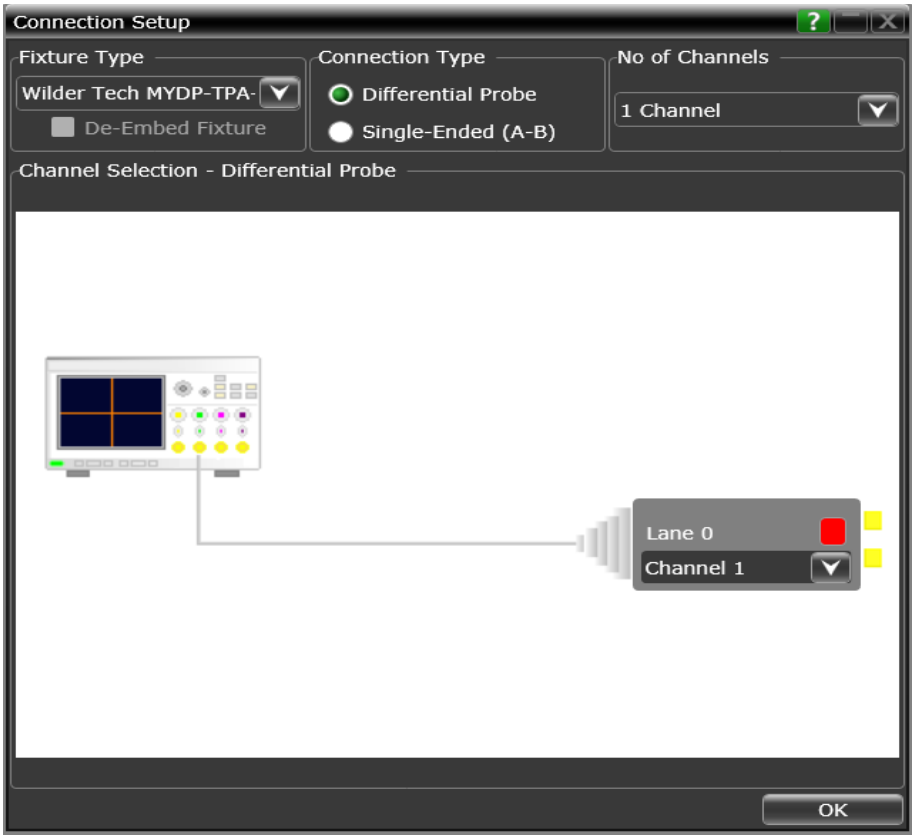
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

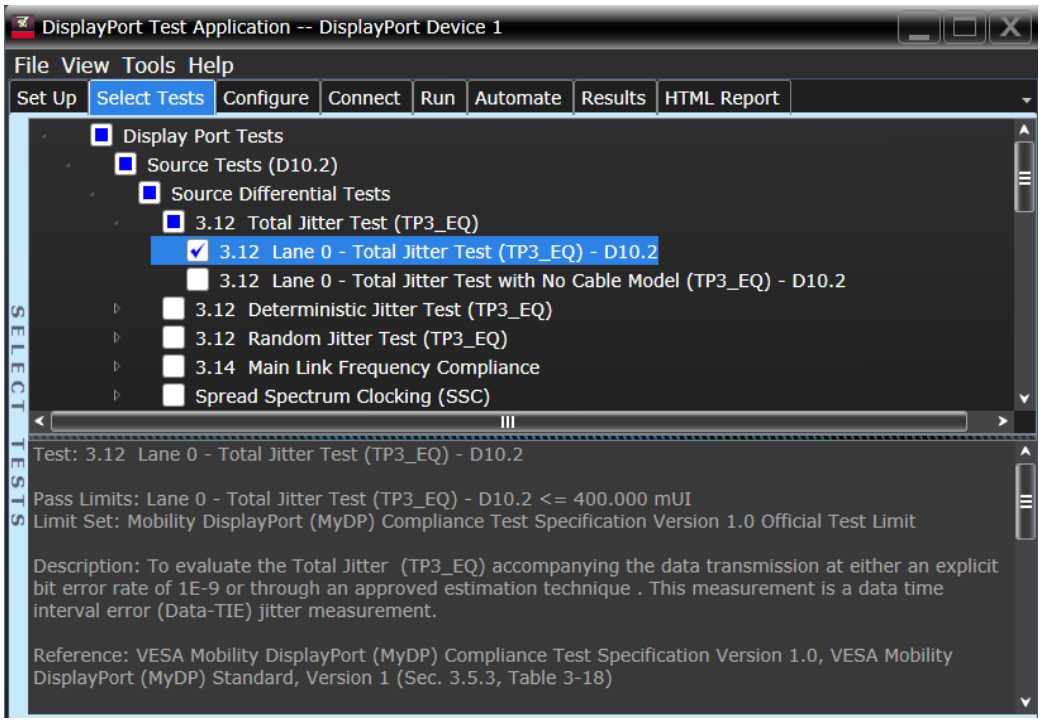
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	Lane 0
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Total Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Total Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.

7 Report the measurement results.

PASS Condition

Table 231 Total Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.580 UI*

* The limits for the Total Jitter are derated by 0.04 UI from 0.62 UI in DisplayPort 1.2a Standard.

Table 232 Total Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.40 UI

UI is Unit Interval.

Test References

See:

For HBR2CPAT

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22

For D10.2

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18

Expected/Observable Results

The measured total jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Deterministic Jitter Test (TP3_EQ)

Test ID

For HBR2:

- 1236001 – Deterministic Jitter Test (TP3_EQ) – HBR2CPAT
- 1236011 – Deterministic Jitter Test with No Cable Model (TP3_EQ) – HBR2CPAT
- 1235001 – Deterministic Jitter Test (TP3_EQ) – D10.2
- 1235011 – Deterministic Jitter Test with No Cable Model (TP3_EQ) – D10.2

Test Overview

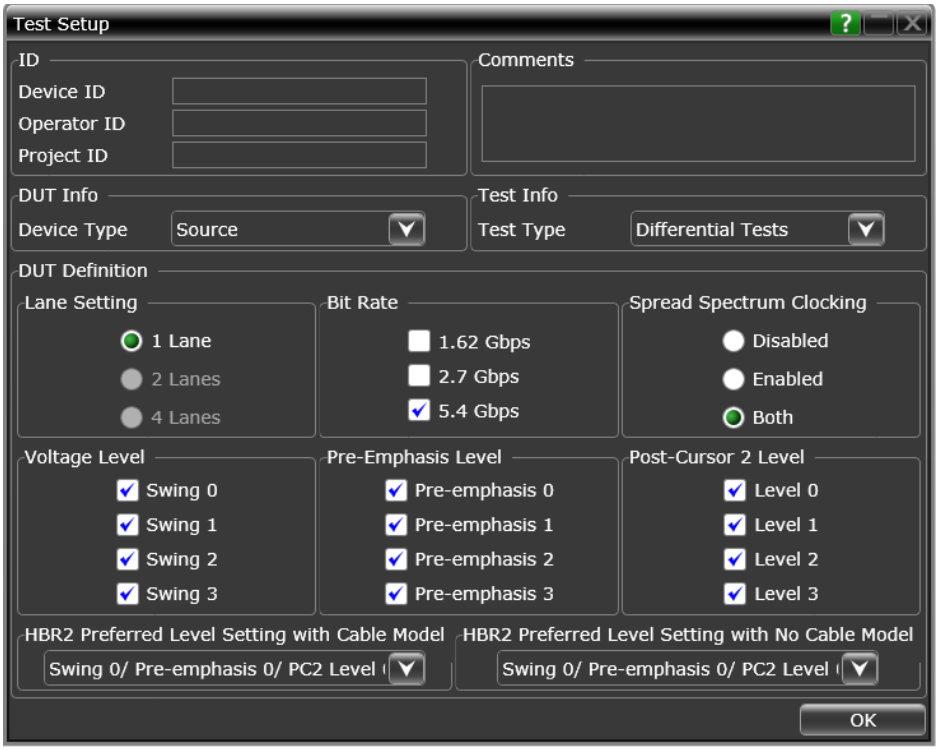
The objective of this test is to evaluate the deterministic jitter accompanying the data transmission. The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

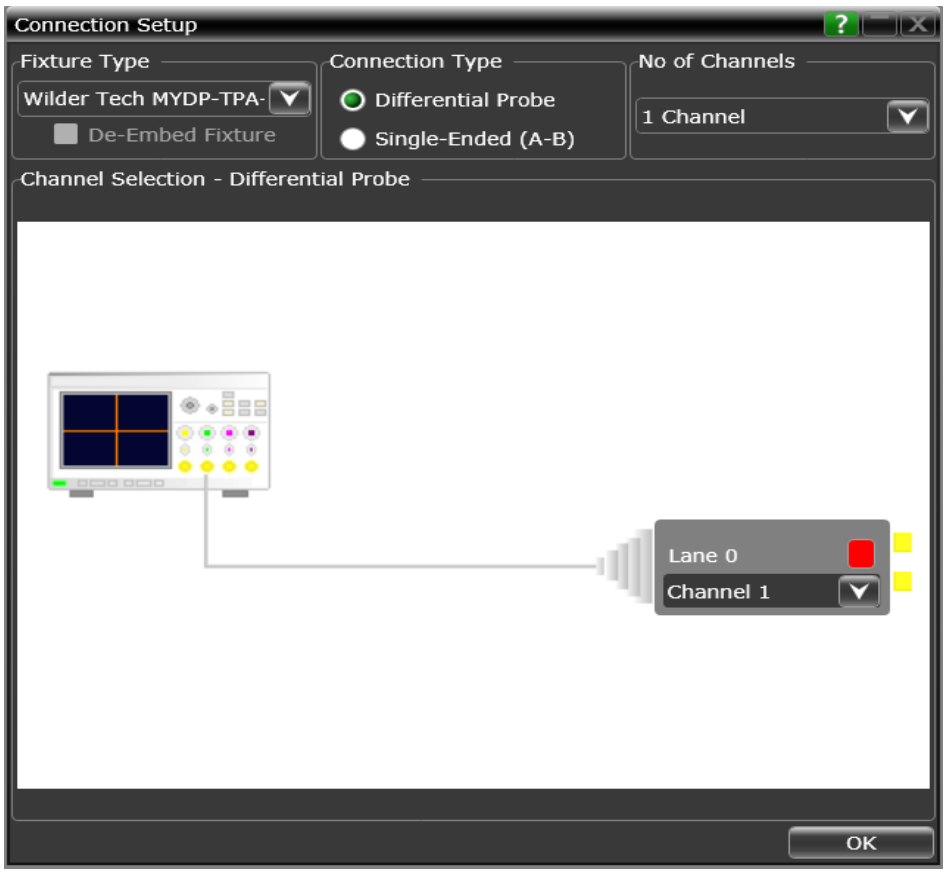
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

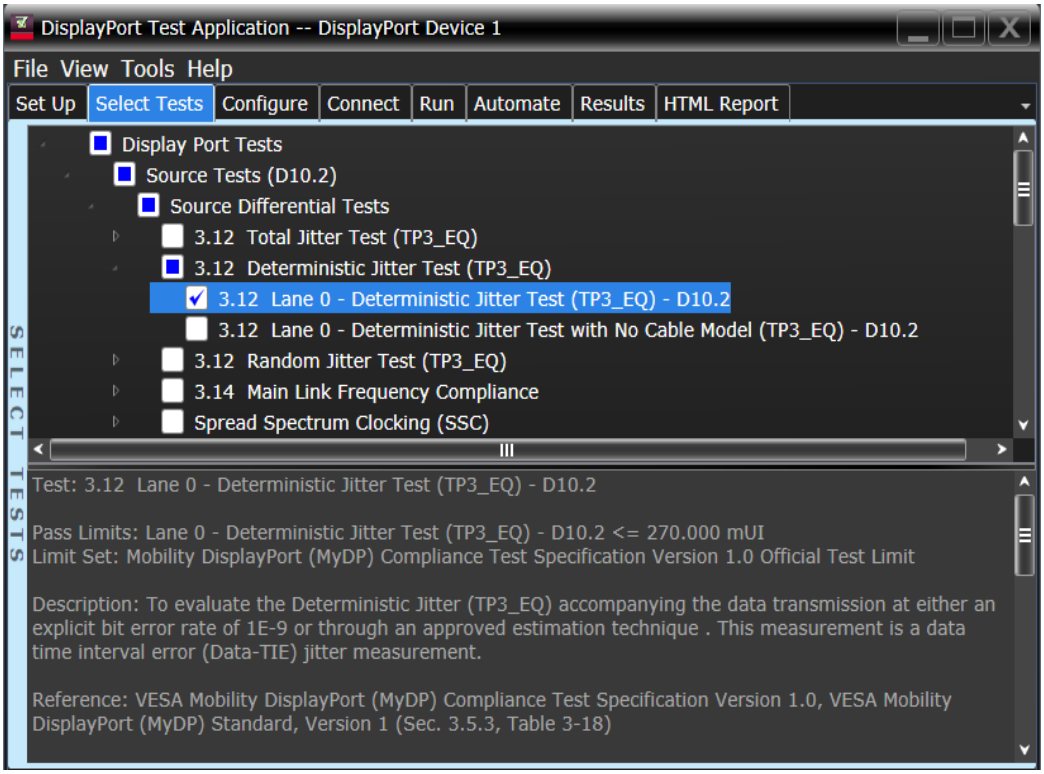
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Deterministic Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	Lane 0
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Deterministic Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Deterministic Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.

6 Note the jitter component value from the EZJIT Plus/Complete Software.

7 Report the measurement results.

PASS Condition

Table 233 Deterministic Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.49 UI

Table 234 Deterministic Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.25 UI

UI is Unit Interval.

Test References

See:

For HBR2CPAT

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

For D10.2

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18*

Expected/Observable Results

The measured deterministic jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Random Jitter Test (TP3_EQ)

Test ID

For HBR2:

- 1238001 – Random Jitter Test (TP3_EQ) – D10.2
- 1238011 – Random Jitter Test with No Cable Model (TP3_EQ) – D10.2

Test Overview

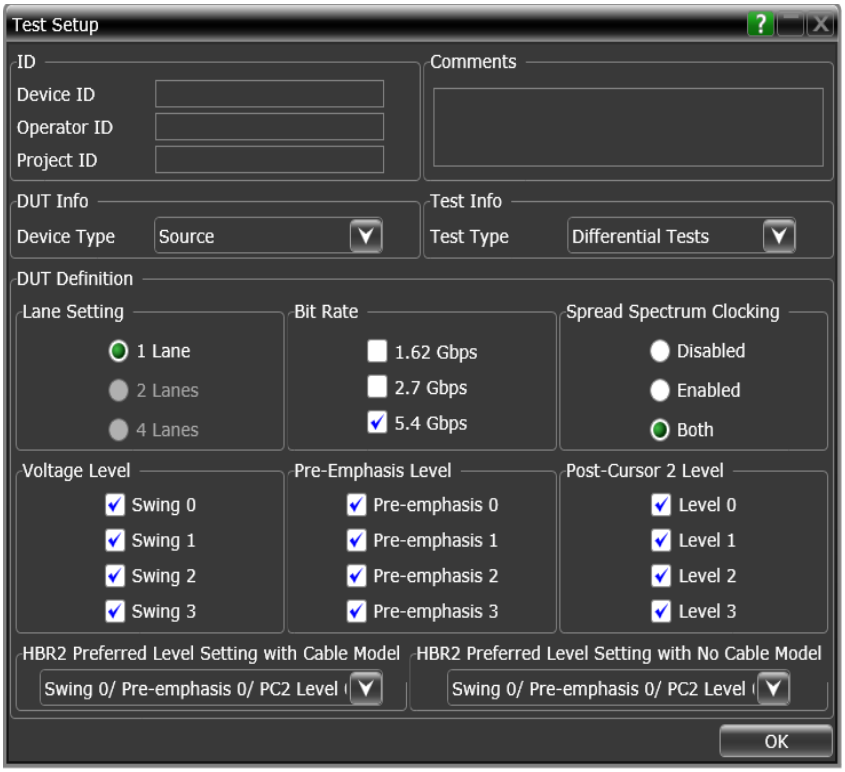
The objective of this test is to evaluate the random jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. The jitter is separated into each jitter components and the random jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

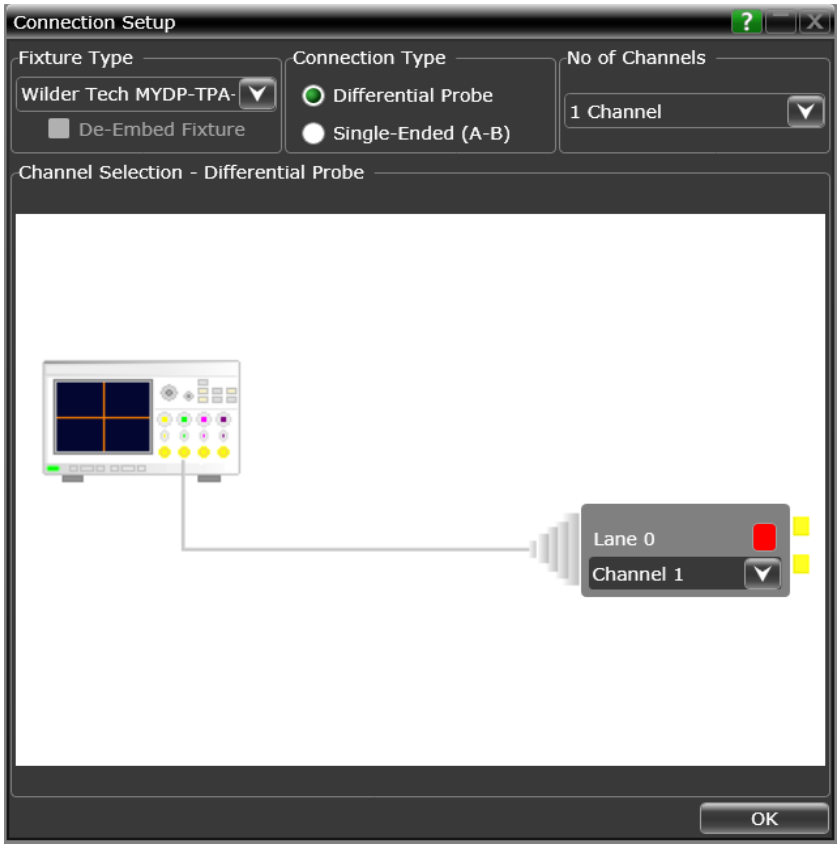
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

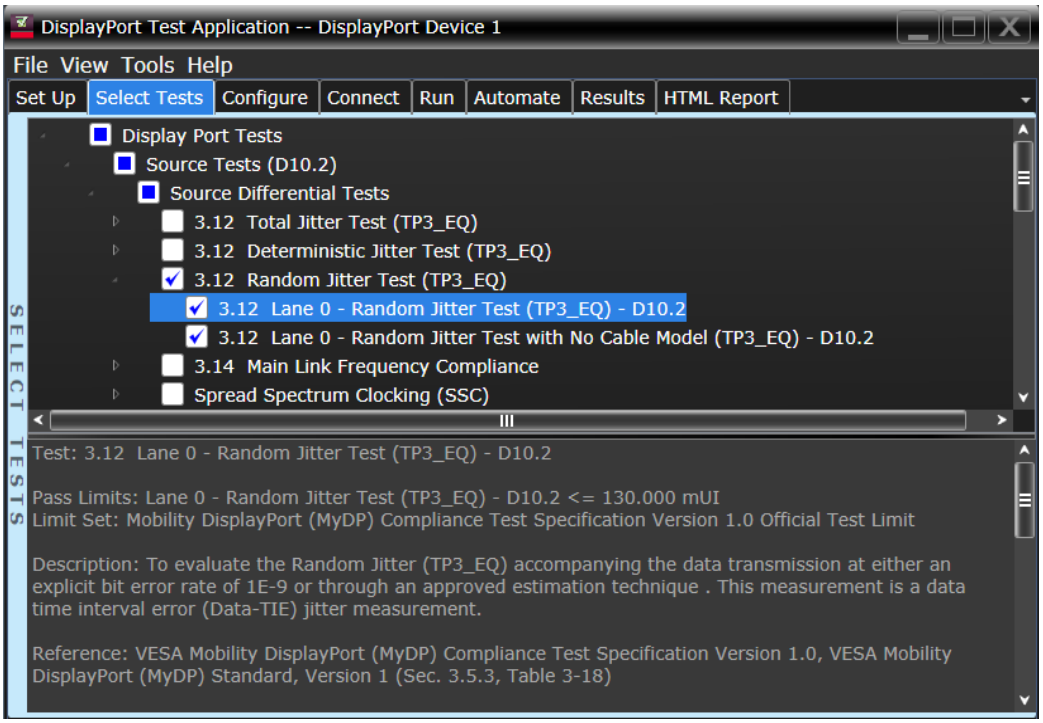
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Random Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	Lane 0
Test Pattern	D10.2
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Random Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Random Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.

7 Report the measurement results.

PASS Condition

Table 235 Random Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.23 UI

UI is Unit Interval.

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18*

Expected/Observable Results

The measured random jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source AC Common Mode Test (Informative)

Test ID

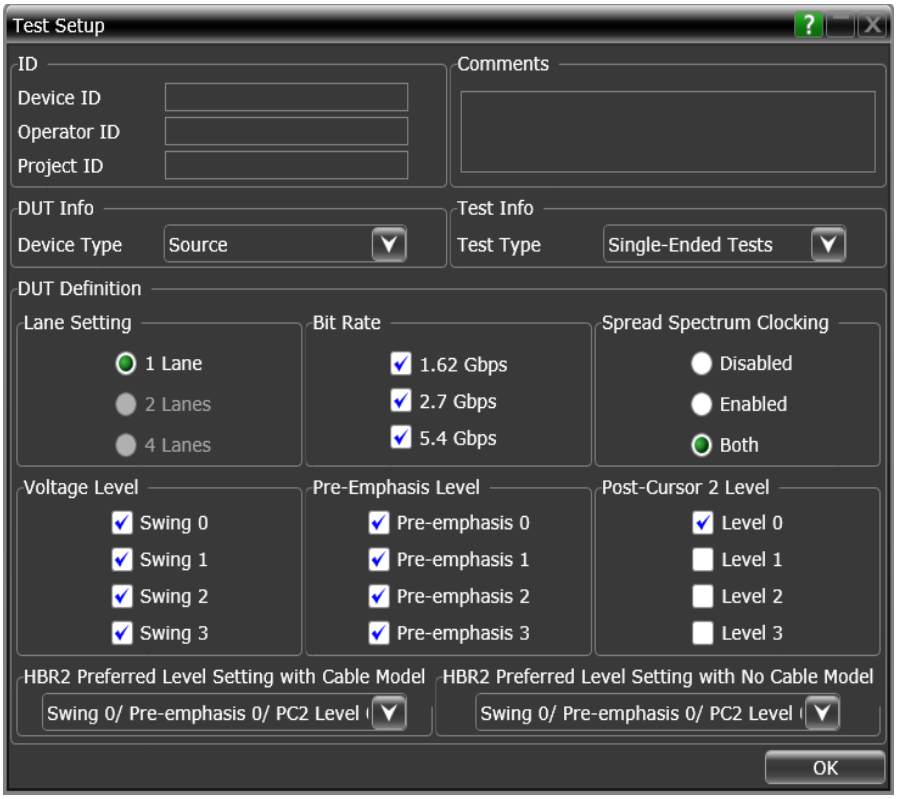
12110001 – AC Common Mode Test (Informative)

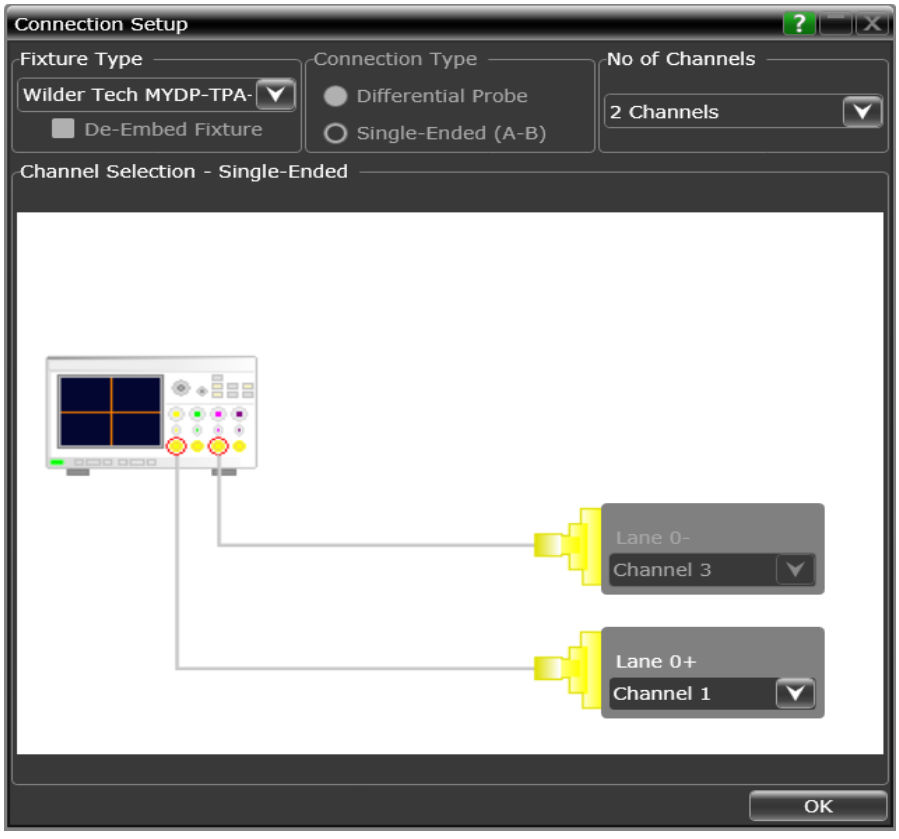
Test Overview

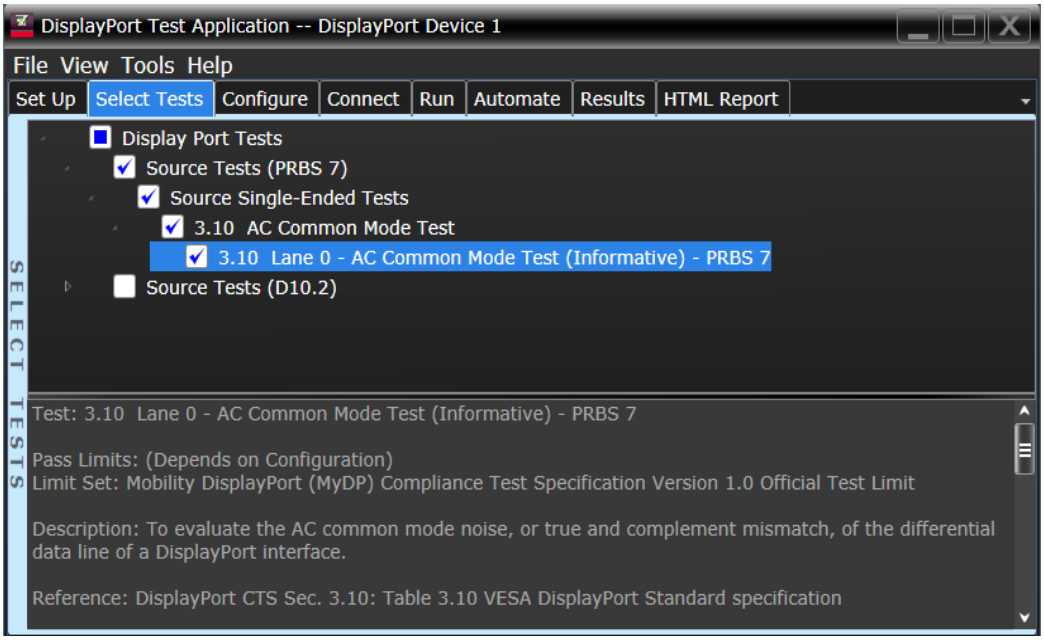
The objective of this test is to evaluate the AC Common Mode noise (unfiltered rms) of the differential data line of the DP interface.

Test Conditions for AC Common Mode Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates are supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis level supported subject to the constraints in Table 3-1 of the VESA DisplayPort 1.2a Standard
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Single-Ended Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
2 Channels
Channel Selection - Single-Ended
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Create FUNC3 signal, which is the common mode signal of the input single-ended signal.
4 If the filter is enabled ["Filter" configuration variable set to "High Pass Filter", "Low Pass Filter" or "None" (Default)]:
   a Create FUNC4 signal, which is the filtered FUNC3 signal by applying the High Pass filter or Low Pass filter on the FUNC3 signal based on the Configuration Variable.
5 Set up two display grids such that one grid displays the input single-ended signal while the other grid displays the common mode signal.
6 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
7 Set up the parameters for RMS voltage measurement of the common mode signal.
   a Set up the V_{rms} measurement for the common mode signal.
   b Acquire the signal until 100,000 edges are measured.
8 Get the mean for the V_{rms} measurement.
9 Report the measurement results.

PASS Condition

For RBR and HBR:

AC Common Mode Voltage $\leq$ 20mV

For HBR2:

AC Common Mode Voltage $\leq$ 30mV

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.10*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 9.2, Table 9-6*

Expected/Observable Results

The measured AC common mode noise for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Intra-Pair Skew Test (Informative)

Test ID

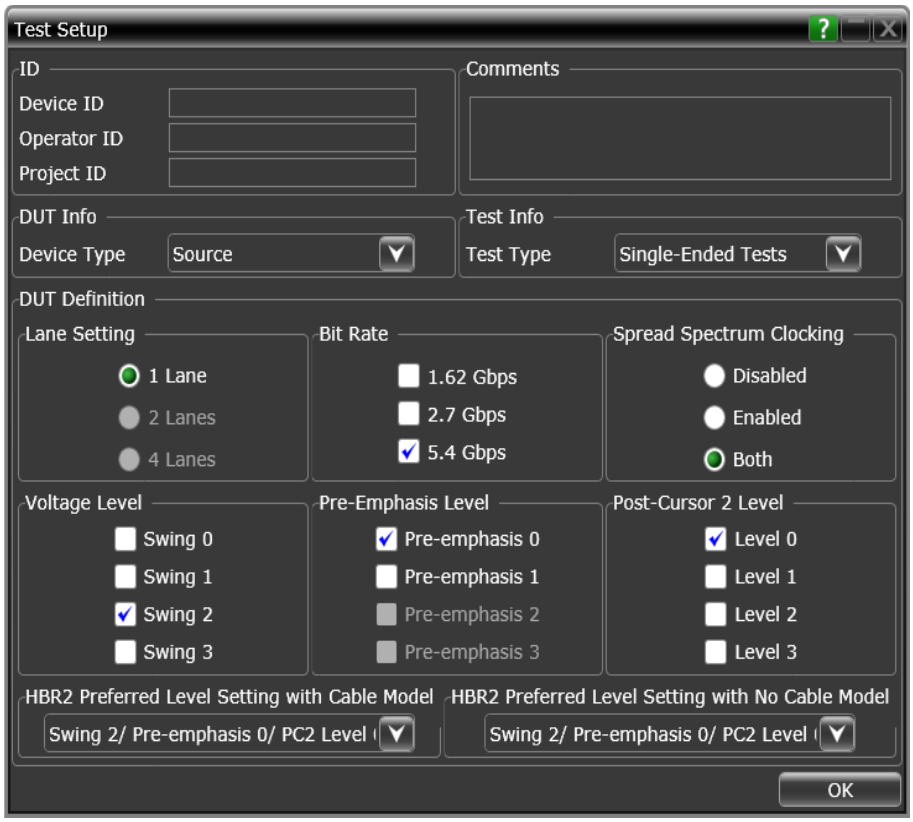
12100001 — Intra-Pair Skew Test (Informative)

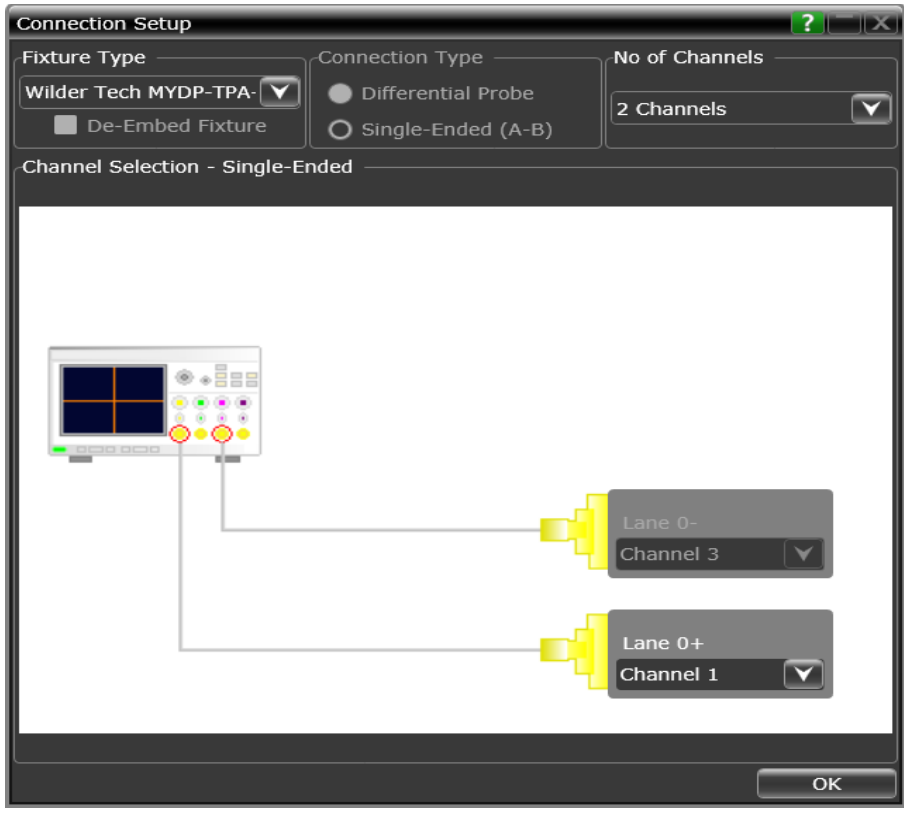
Test Overview

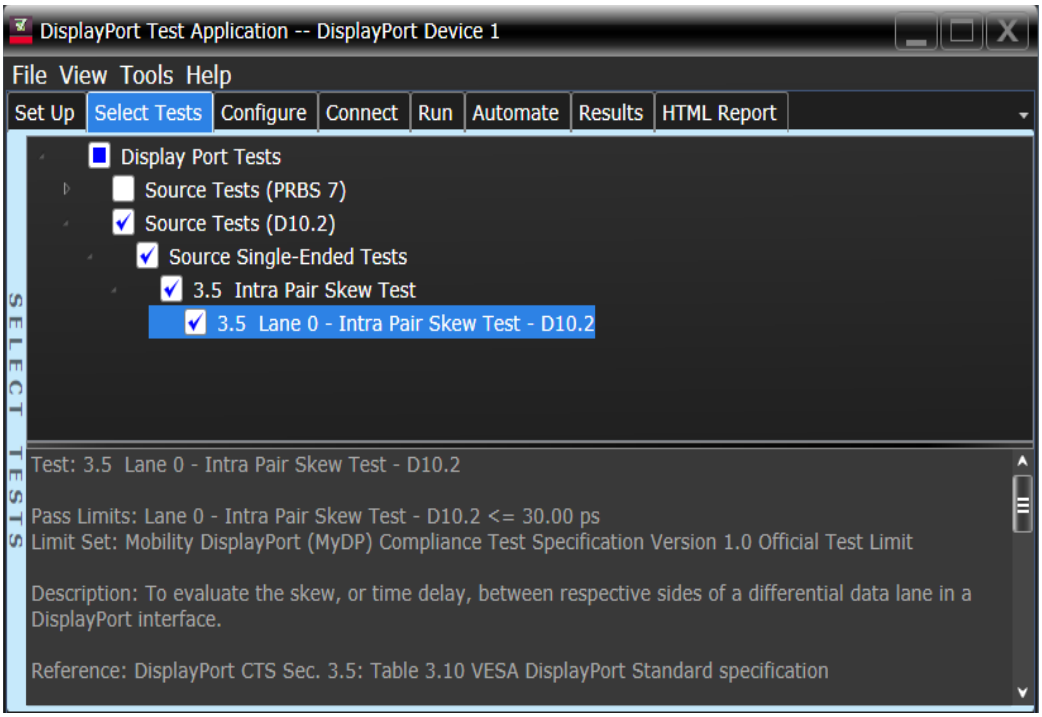
The objective of this test is to evaluate the skew or time delay between respective sides of a differential data lane in the DP interface.

Test Conditions for Intra-Pair Skew Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	Both SSC conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0 (Lane 0+ to Lane 0-)
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Single-Ended Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
2 Channels
Channel Selection - Single-Ended
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
4 Set up the parameters to perform High Level Voltage (V_{HIGH}) and Low Level Voltage (V_{LOW}) for each input single-ended signal.
   a Scale the vertical display of the input single-ended signal to optimum value.
   b Acquire the signal for 100 waveforms.
   c Find V_{HIGH} by measuring the average voltage at 0.06 UI to 0.75 UI of the High Level.
   d Find V_{LOW} by measuring the average voltage at 0.06 UI to 0.75 UI of the Low Level.
   e Calculate the Transition Voltage (V_{Trans}) using the equation:

$$V_{Trans} = (V_{HIGH} + V_{LOW}) / 2$$

5 Set up the parameters for the intra-pair skew measurement:

a Set up the measurement threshold for each single-ended data signal based on the measured Transition Voltage.

b Set up InfiniiScan to trigger on the desired pattern.

c Set up delta time measurement to measure time difference between the rising edge of the data true signal (D+) and the complement's (D-) falling edge:

$$D+_{Transition\_High} - D-_{Transition\_Low}$$

d Set up delta time measurement to measure time difference between the falling edge of the data true signal (D+) and the complement's (D-) rising edge:

$$D+_{Transition\_Low} - D-_{Transition\_High}$$

e Acquire the signal until you measure 100 edges.

f Calculate the intra-pair skew using the equation:

$$\text{Intra-Pair Skew} = \{1/\text{Number of Edges}\}$$

$$\sum \{[(D+_{Transition\_High} - D-_{Transition\_Low}) + (D+_{Transition\_Low} - D-_{Transition\_High})] / 2\}$$

6 Report the measurement results.

PASS Condition

Intra-Pair Skew ≤ 30 ps

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.5*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured intra-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

31 MyDP 1.0 Sink Tests

Overview

Test Point Definition for DisplayPort MyDP 1.0 Sink Tests

NOTE Sink Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Sink DUT at Test Point 3 (TP3) as shown in Figure 215. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

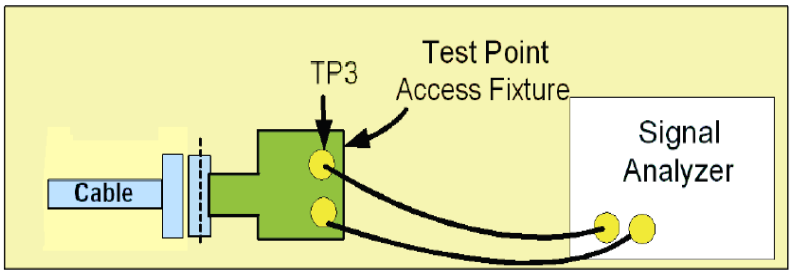


Figure 215 Test Point 3 Connection for MyDP 1.0 Sink Tests

Table 236 defines the test point fixtures and instruments used for MyDP 1.0 Sink Tests:

Table 236 Test Point Fixtures and Instruments for MyDP 1.0 Sink Tests

Test Requirement	Device Used
Test Point Access Fixture	Mobility DisplayPort Test Point Adapter For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Calibration of Stress Signal

For the calibration of the stress signal, you must test the stress signal in the manner shown in the Figure 216 for RBR and Figure 217 for HBR and HBR2.

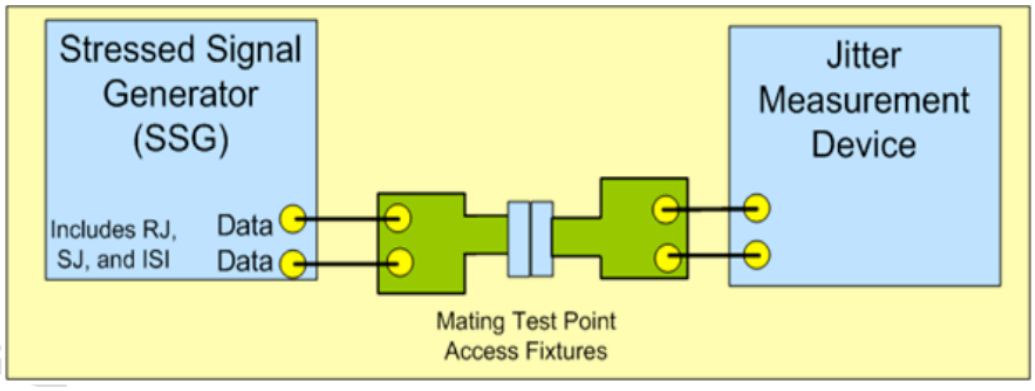


Figure 216 Test Point 3 Connection for Stress Signal Calibration of RBR

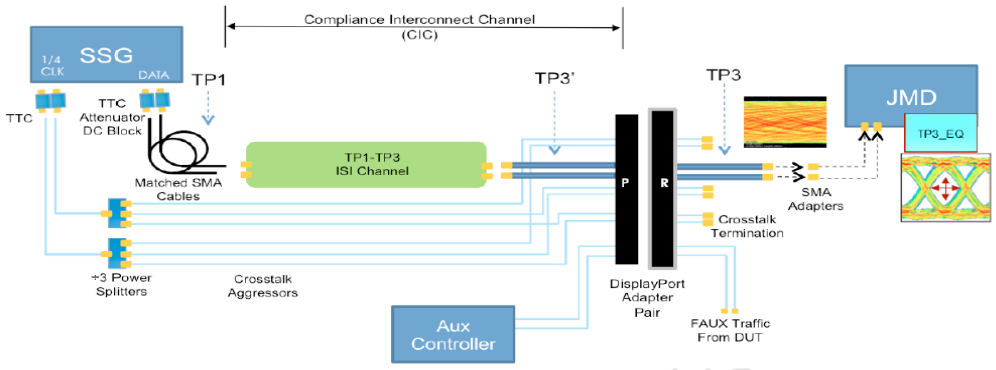


Figure 217 Test Point 3 Connection for Stress Signal Calibration of HBR and HBR2

Table 237 defines the Test Point 3 Connections for Stress Signal Calibration:

Table 237 Test Point Connections for Stress Signal Calibration

Test Requirement	Device Used
Stress Signal Generator (SSG)	Bit Error Rate Tester ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	Mobility DisplayPort Test Point Adapter For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters.
Jitter Measurement Device (JMD)	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for MyDP 1.0 Sink Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort MyDP 1.0 Standards, select the option **MyDP 1.0** in the **Test Specification** area.

5 The option **Physical Layer Tests** appears by default in the **Test Selection** area.

6 Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.

7 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

8 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

9 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

10 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

11 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

12 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

13 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

14 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for MyDP 1.0 Sink Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

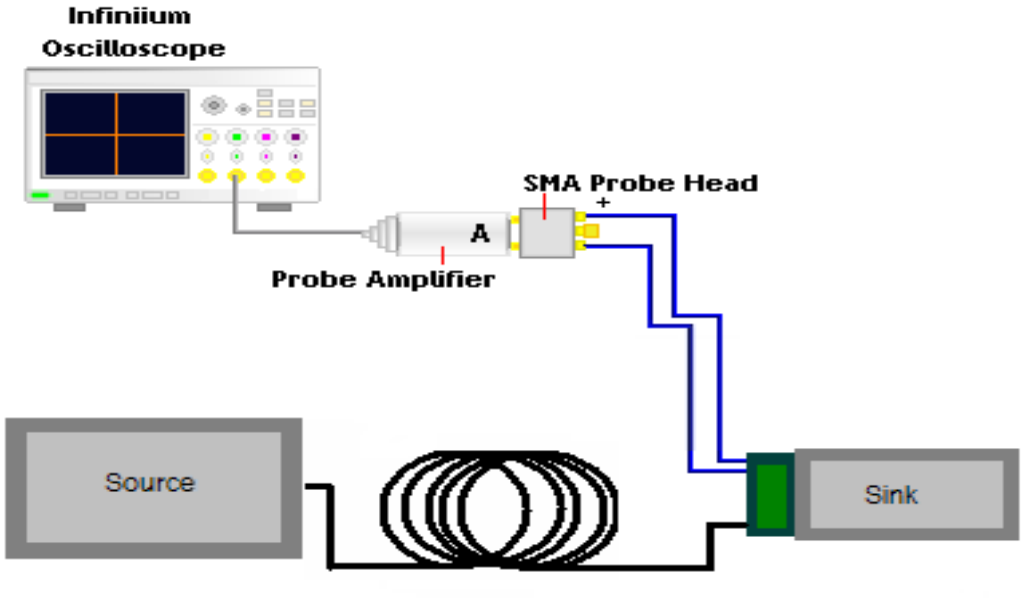


Figure 218 Sample connection diagram for MyDP 1.0 Sink Tests

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Sink tests to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1 In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.

2 On the **Test Setup** window,

a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b In the **DUT Info** area, select the **Device Type** as **Sink**.

c In the **Test Info** area, the **Test Type** options are grayed out.

d In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.

3 Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1 Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.

2 On the **Connection Setup** window,

a Select the appropriate option in the **Fixture Type** to indicate where the DUT is connected to.

b Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.

c In the **Channel Selection** area, assign appropriate channels to lanes.

3 Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of sink tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for MyDP 1.0 Sink Tests" on page 1152 to complete the task flow for DUT setup along with configuring the Compliance Application to run each test.

Sink Eye Diagram Test

Test ID

12140001 – Eye Diagram Test

Test Overview

The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

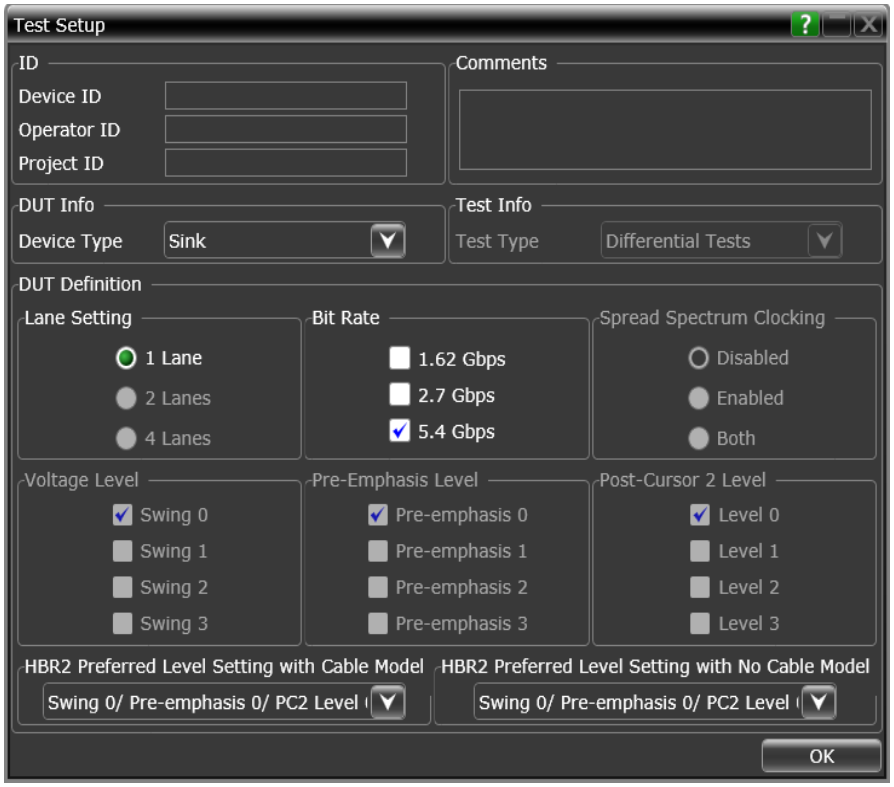
You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the following specifications for degradation:

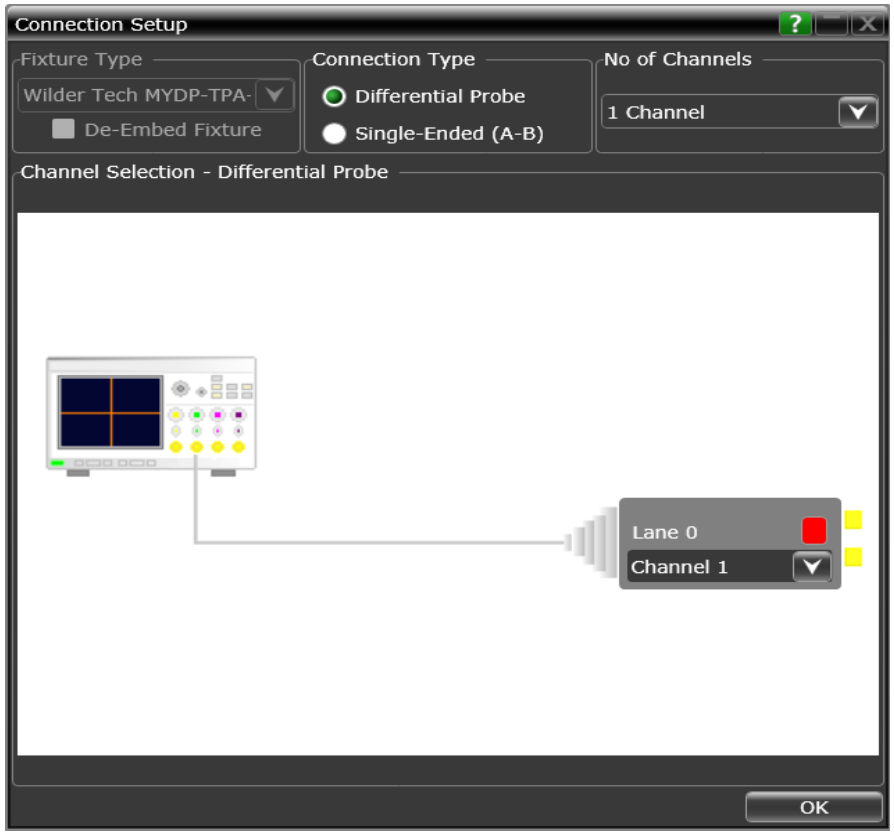
- Voltage Level:
  - 90mV peak to peak +/- 10% for HBR2 at TP3_EQ (Table 3-18, DP1.2a)
  - 150mV peak to peak +/- 10% for HBR at TP3_EQ (Table 3-25, DP1.2a)
  - 46mV peak to peak +/- 10% for RBR at TP3 (Table 3-26, DP1.2a

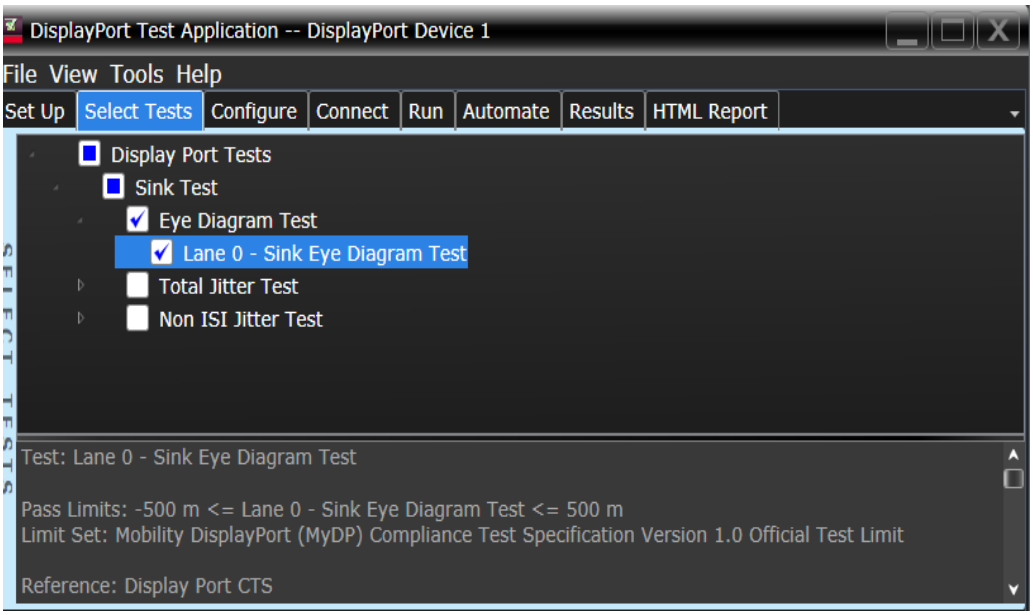
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR and HBR2)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR–PRBS7 HBR2–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
9 Measure the jitter of the eye diagram using the Histogram.

10 Check for any signal trajectories that may have entered into the mask.

11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 238 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 238 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

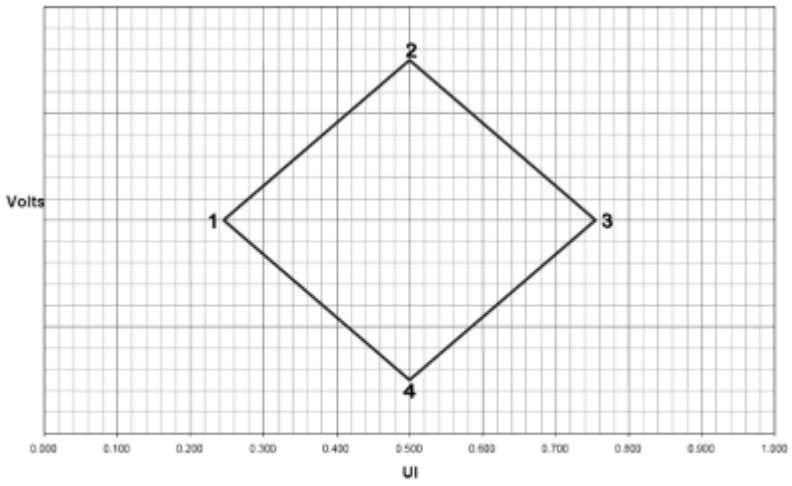


Figure 219 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 239 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.045*
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.045*

NOTE

*Eye height limit of 45 mV and -45 mV assumes cross-talk as 0, which is only possible in case of single lane testing.

In case of multi-lane testing, cross talk exists, and the eye height values deviate by ± 7 mV. Thus the eye height becomes (+45 +7) mV and (-45 -7) mV or +52 mV and -52 mV.

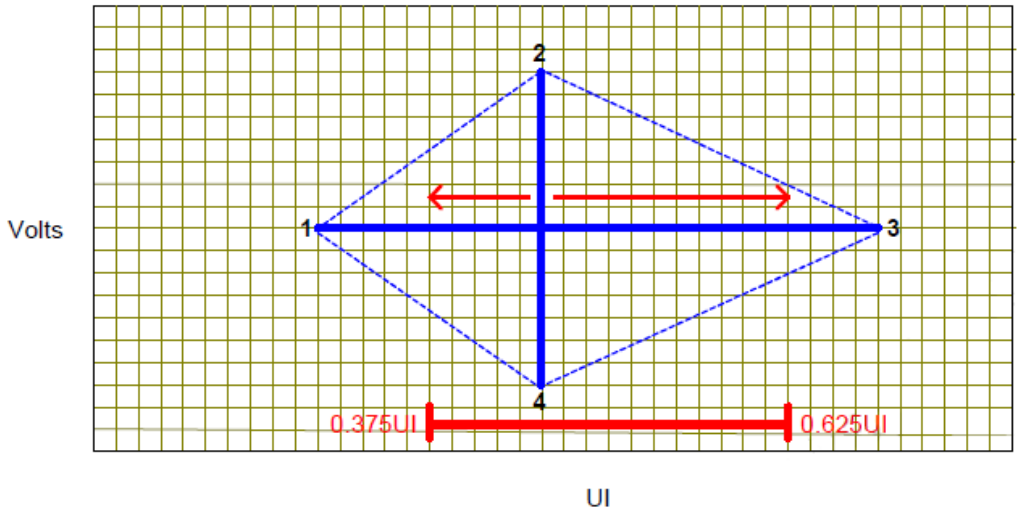


Figure 220 The Sink Eye Mask at TP3_EQ (HBR2)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Sink Total Jitter Test

Test ID

12210001 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

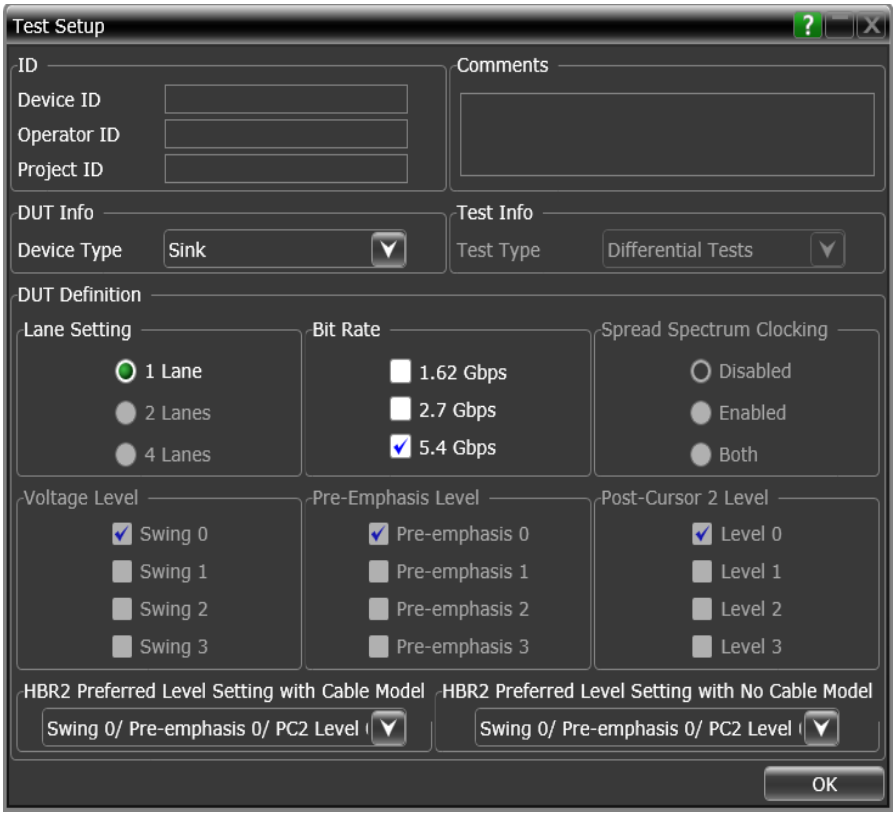
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

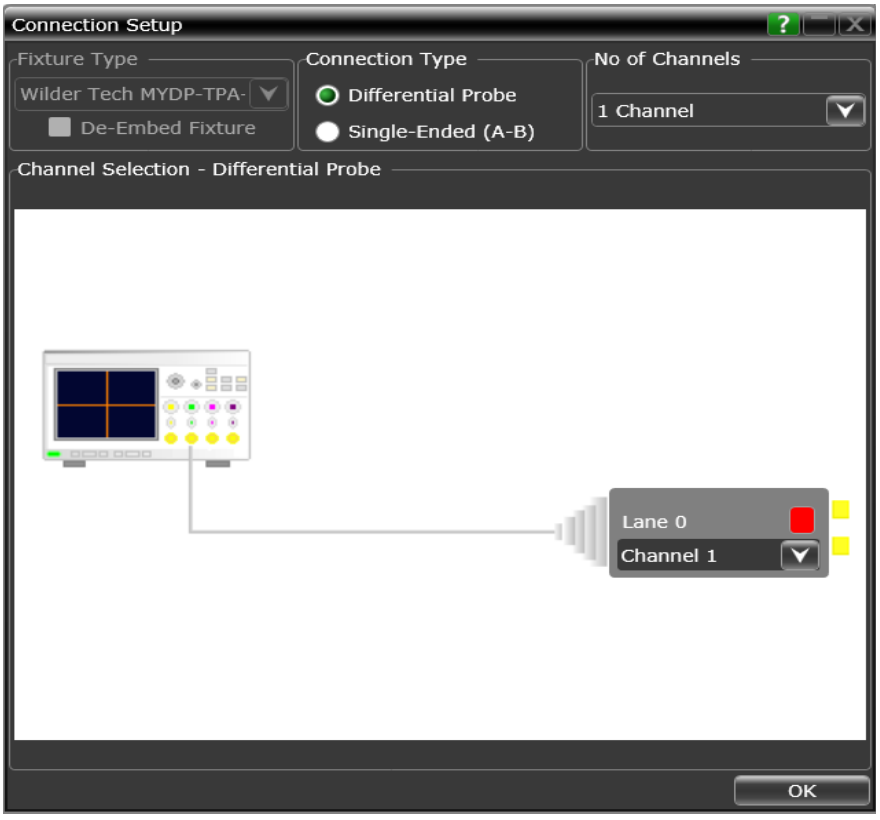
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

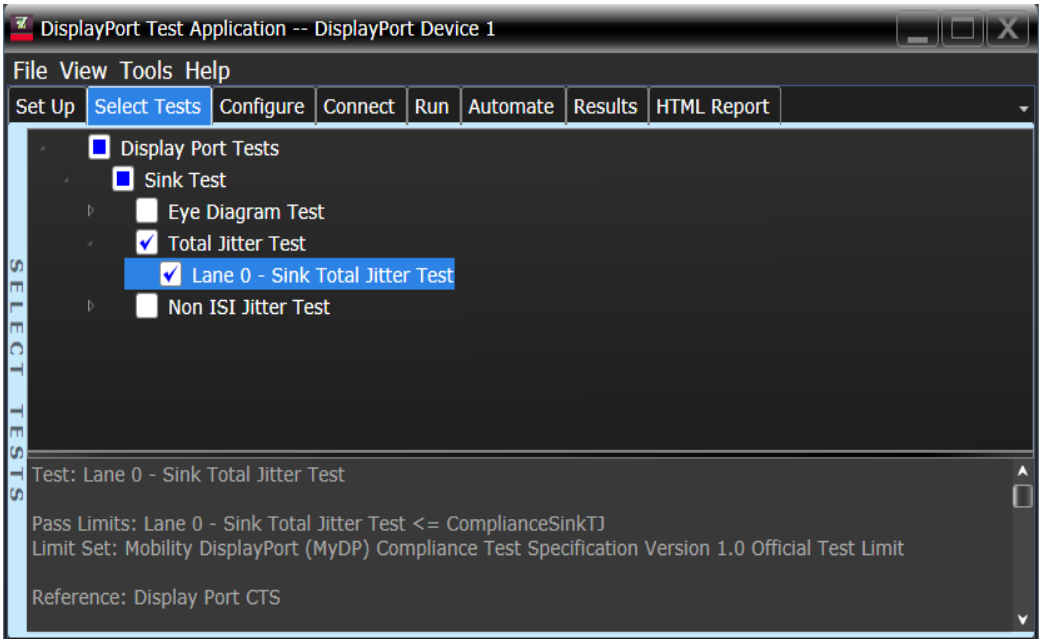
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR and HBR2)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR–PRBS7 HBR2–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 240 Total Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	0.580 UI*

* The limits for the Total Jitter are derated by 0.04 UI from 0.62 UI in DisplayPort 1.2a Standard.

Table 241 Total Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Sink Non-ISI Jitter Tests

Test ID

12220001 — Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the Non ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

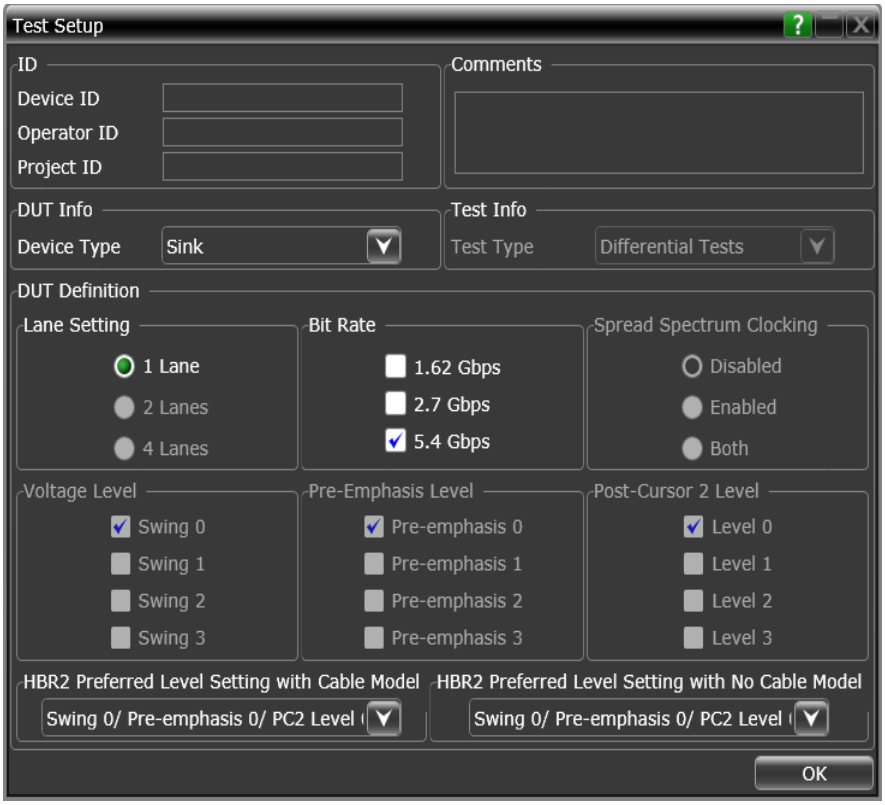
Calculate Non-ISI Jitter using the following equation:

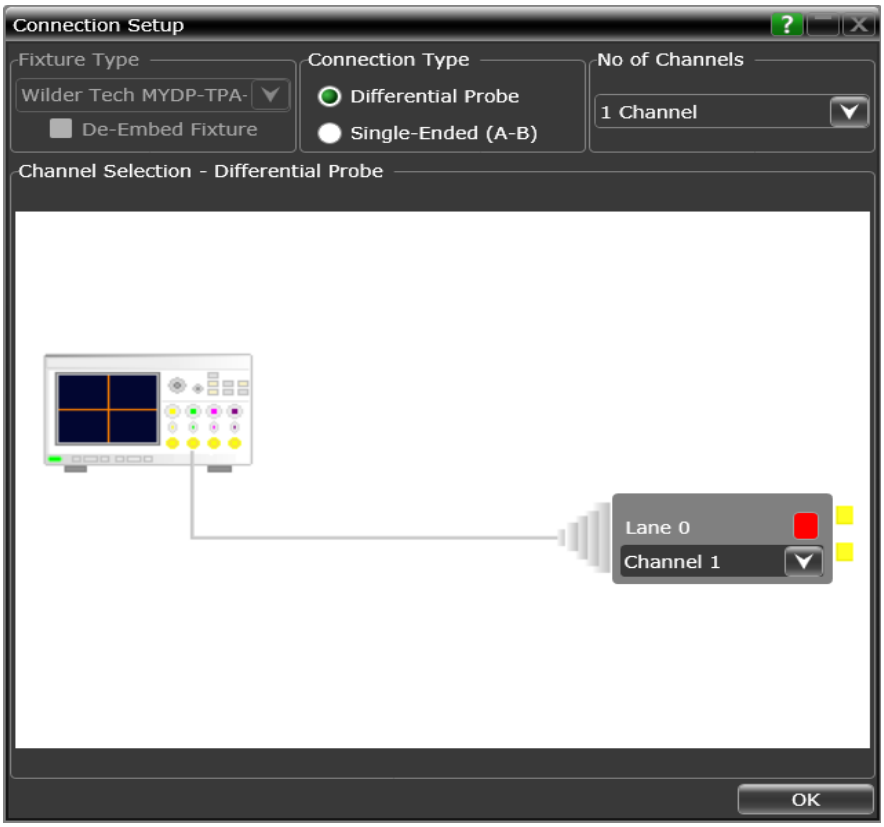
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

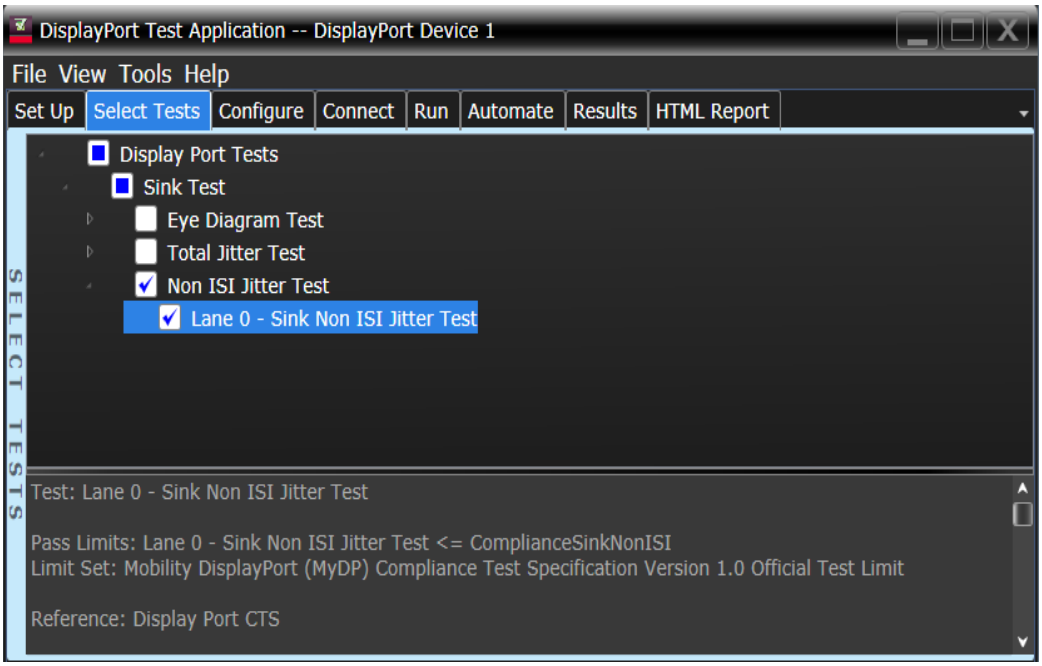
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR and HBR2)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR–PRBS7 HBR2–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 242 Non ISI Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	-

Table 243 Non ISI Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

32 MyDP 1.0 Cable Tests

Overview

Test Point Definition for MyDP 1.0 Cable Tests

NOTE Cable Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Cable DUT at Test Point 3 (TP3) as shown in Figure 221. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

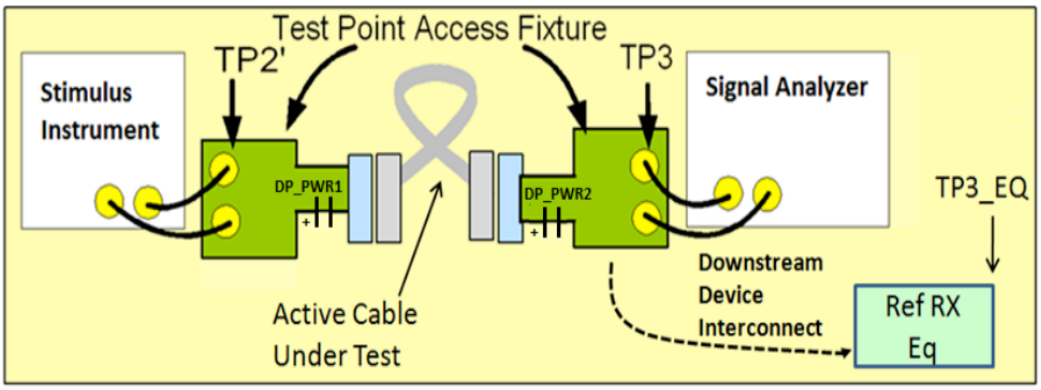


Figure 221 Test Point 3 Connection for MyDP 1.0 Cable Tests

Table 244 defines the test point fixtures and instruments used for MyDP 1.0 Cable Tests:

Table 244 Test Point Fixtures and Instruments for MyDP 1.0 Cable Tests

Test Requirement	Device Used
Stimulus Instrument	Pulse Pattern Generator ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Table 245 defines the input signal parameters applied by the stimulus instrument at TP2:

Table 245 Input Signal Parameters by Stimulus Instrument

RBR	▪ Reference Table 3-22 and Table 3-24, DP 1.2a ▪ Edge Rate (20-80): 155-165ps (260mUI) ▪ Eye Height: 400mV ▪ Total Jitter: 270mUI ▪ ISI: 100mUI ▪ Random Jitter (rms): 7.9mUI ▪ Sinusoidal Jitter: ~75mUI at 20MHz (Adjust to achieve Total Jitter)
HBR	▪ Reference Table 3-22 and Table 3-23, DP 1.2a ▪ Edge Rate (20-80): 90-100ps (260mUI) ▪ Eye Height: 350mV ▪ Total Jitter: 420mUI ▪ ISI: 144mUI ▪ Random Jitter (rms): 13.2mUI ▪ Sinusoidal Jitter: ~117mUI at 20MHz (Adjust to achieve Total Jitter)

Setting Up the DisplayPort Compliance Test Application for MyDP 1.0 Cable Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort MyDP 1.0 Standards, select the option **MyDP 1.0** in the **Test Specification** area.
5. The option **Physical Layer Tests** appears by default in the **Test Selection** area.
6. Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.
7. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
8. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
9. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
10. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
11. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
12. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
13. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
14. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for MyDP 1.0 Cable Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

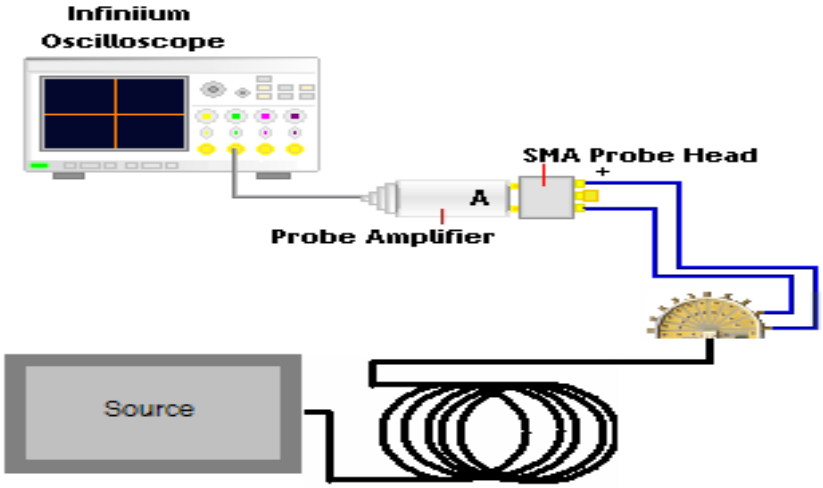


Figure 222 Sample connection diagram for MyDP 1.0 Cable Tests

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Cable tests to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1 In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.

2 On the **Test Setup** window,

a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b In the **DUT Info** area, select the **Device Type** as **Cable**.

c In the **Test Info** area, the **Test Type** options are grayed out.

d In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.

3 Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1 Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.

2 On the **Connection Setup** window,

a Select the appropriate option in the **Fixture Type** to indicate where the DUT is connected to.

b Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.

c In the **Channel Selection** area, assign appropriate channels to lanes.

3 Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of cable tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for MyDP 1.0 Cable Tests" on page 1172 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Cable Eye Diagram Test

Test ID

12150001 – Eye Diagram Test

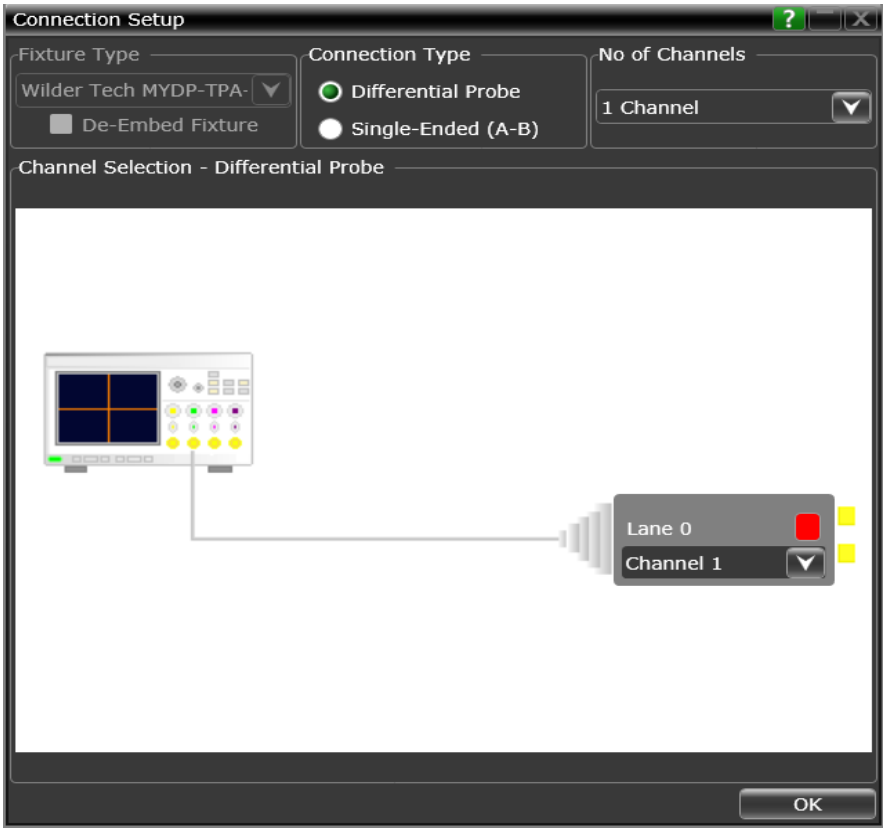
Test Overview

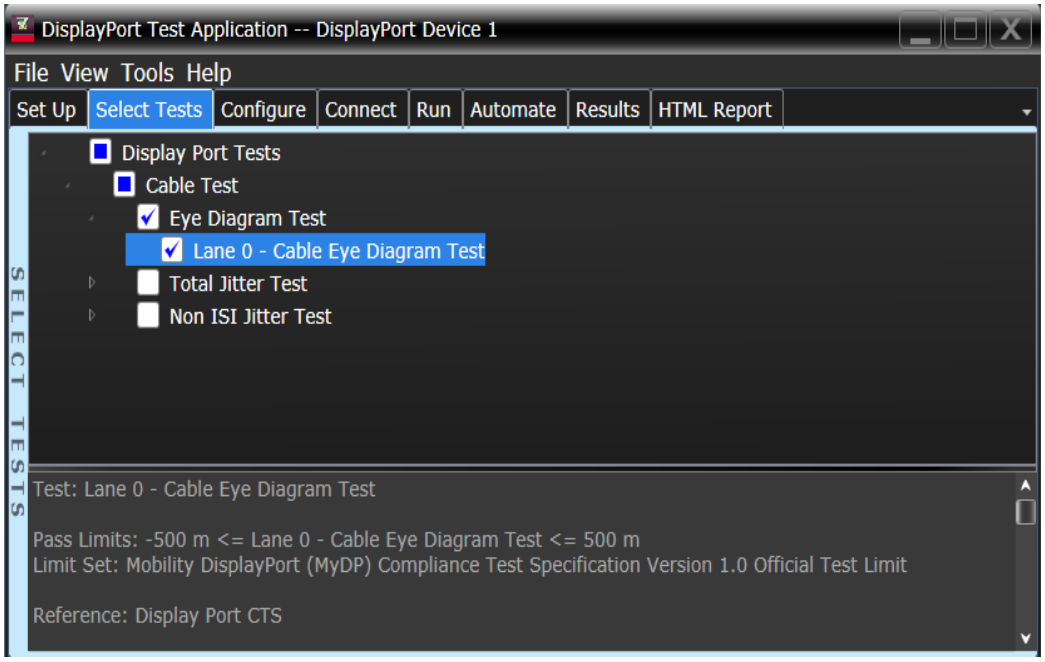
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 245
Crosstalk Signal Parameter	Quarter-rate clock signal (D24.3 pattern) is injected to lanes other than the lane under test. The characteristics of the aggressor signals are: Pattern–D24.3 Bit Rate–(Same as lane under test) Voltage Amplitude–(Same as lane under test) ▪ RBR-400mV ▪ HBR-350mV Edge Rate (20-80)–130ps at TP3


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.

9 Measure the jitter of the eye diagram using the Histogram.
10 Check for any signal trajectories that may have entered into the mask.
11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 246 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 246 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

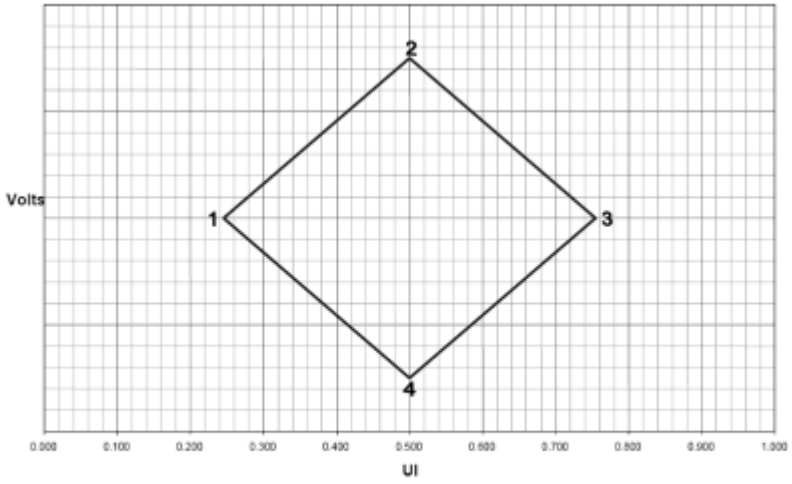


Figure 223 The Cable Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Cable Total Jitter Test

Test ID

12230001 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

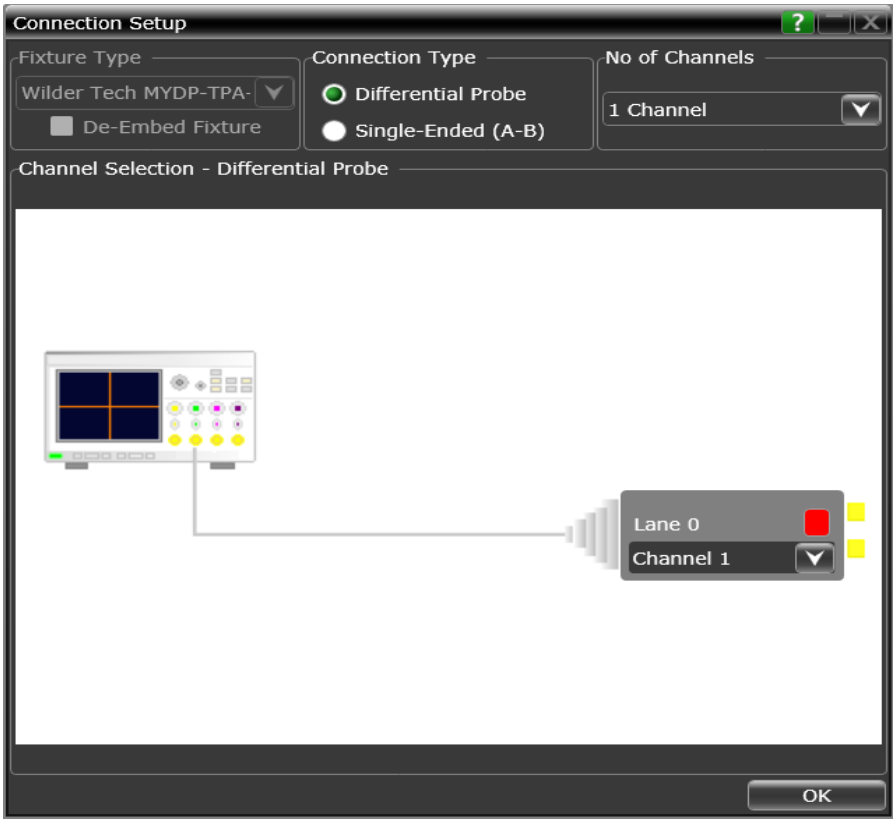
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

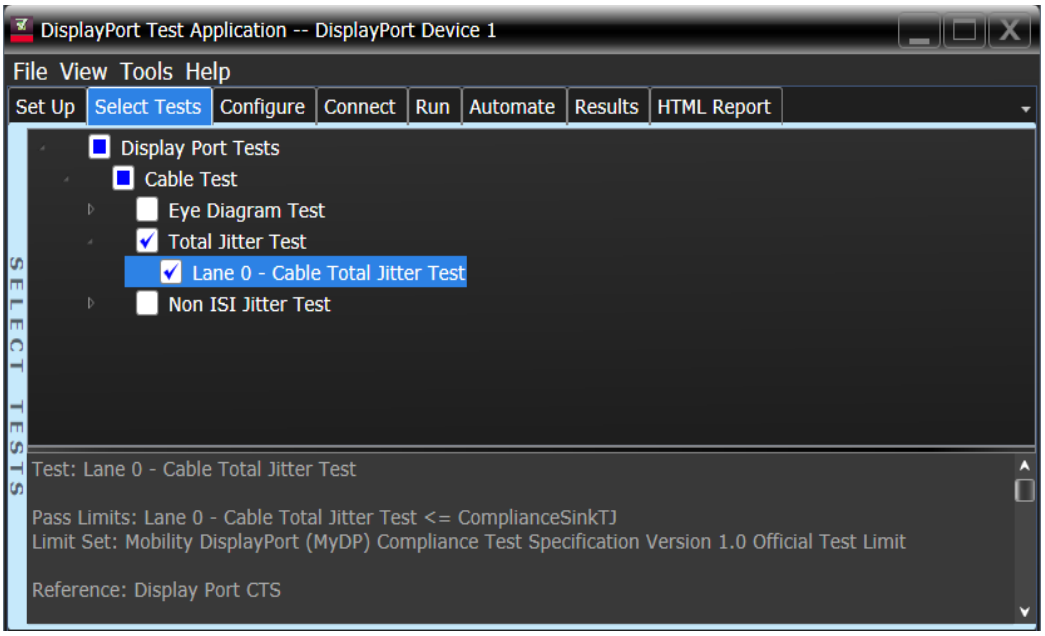
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 245


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 247 Total Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Cable Non-ISI Jitter Test

Test ID

12240001 — Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

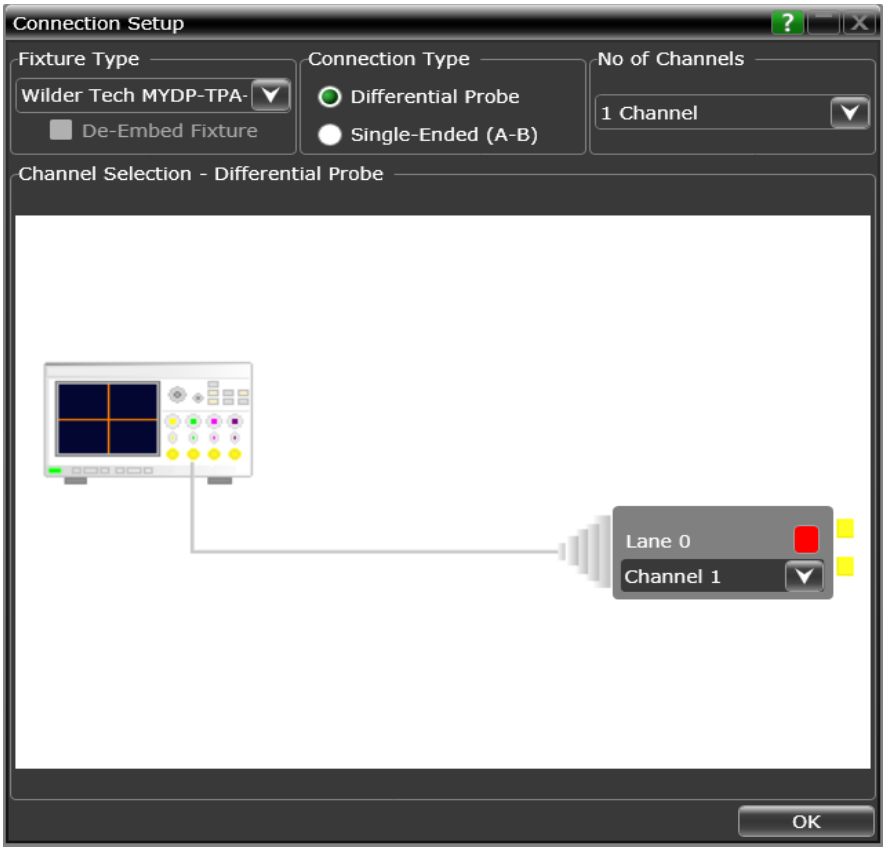
Calculate Non-ISI Jitter using the following equation:

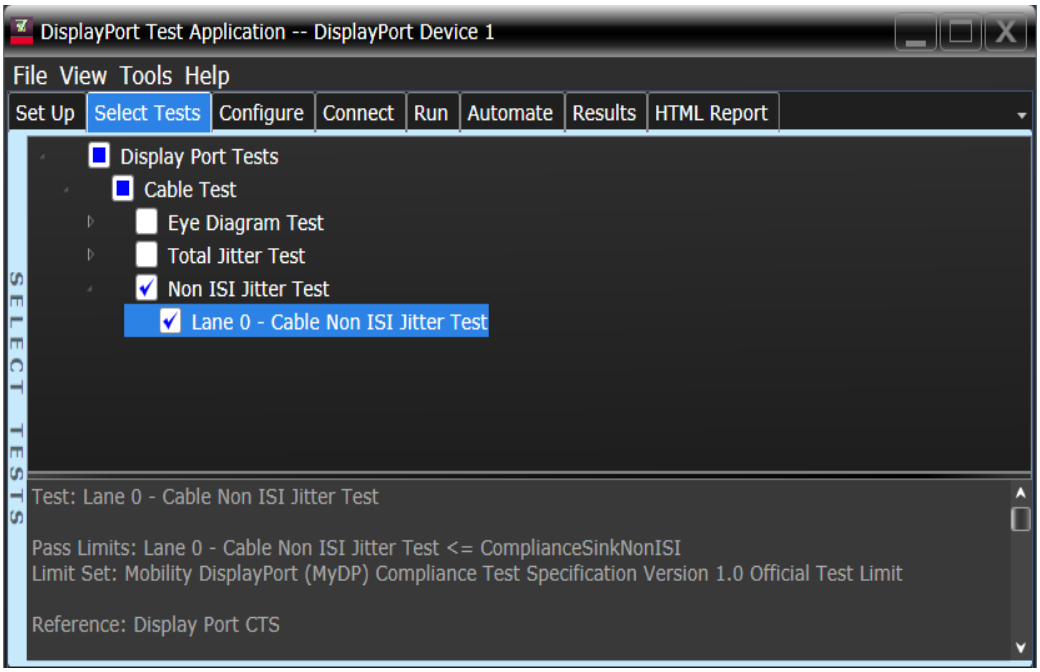
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 245


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 248 Non ISI Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non-ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

33 MyDP 1.0 AUX Channel Tests

Overview

Test Point for MyDP 1.0 AUX Channel Tests

You must test the Source devices at Test Point 2 (TP2) while the Sink devices must be tested at Test Point 3 (TP3). See Figure 224.

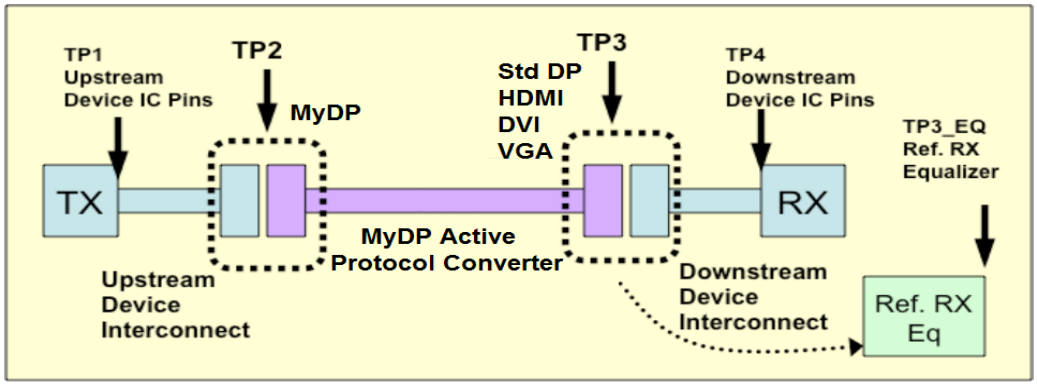


Figure 224 Test Points for MyDP 1.0 AUX Channel Tests

Table 249 defines the test point fixtures and instruments used for MyDP 1.0 AUX Channel Tests:

Table 249 Test Point Fixtures and Instruments for MyDP 1.0 AUX Channel Tests

Test Requirement	Device Used
Test Point Access Fixture	Mobility DisplayPort Test Point Adapter For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope
Stimulus	Stimulus must be applied to the DUT to cause AUX Channel transactions to occur. This stimulus shall not be included in or affect the measurements. Reference Sink needed as stimulus for the Source DUT: ▪ Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Reference Source needed as stimulus for the Sink DUT: ▪ Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Setting Up the DisplayPort Compliance Test Application for MyDP 1.0 AUX Channel Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort MyDP 1.0 Standards, select the option **MyDP 1.0** in the **Test Specification** area.

5 Select the option **AUX PHY and Inrush Tests** in the **Test Selection** area.

6 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

7 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

8 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

9 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

10 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

11 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

12 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

13 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Settings for AUX PHY and Inrush Tests

Perform the following steps before you run the Auxiliary Channel and Inrush tests on the source or sink device:

1 Click the **Test Setup** button on the **Set Up** tab to set up for Auxiliary Channel and Inrush tests.

2 On the **Test Setup** window,

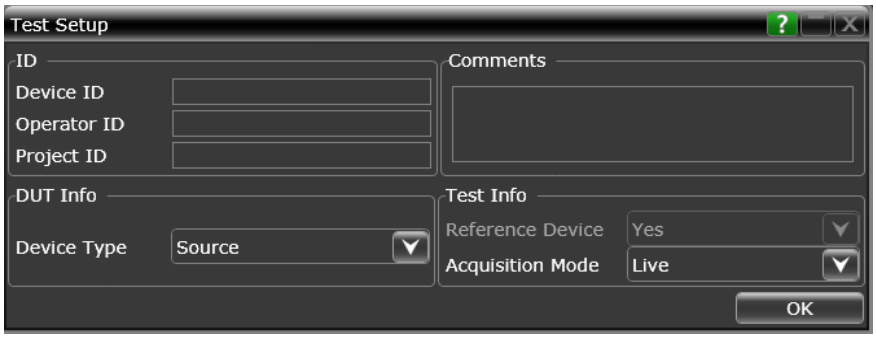
a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b From the **Device Type** drop-down options, select either **Source** or **Sink**.

c The **Reference Device** drop-down options are grayed out.

d From the **Acquisition Mode** drop-down options, select **Live** if waveform acquisition and analysis will be performed on an online Infiniium Oscilloscope, else select **Offline**.

3 Click **OK** to exit the **Test Setup** window.

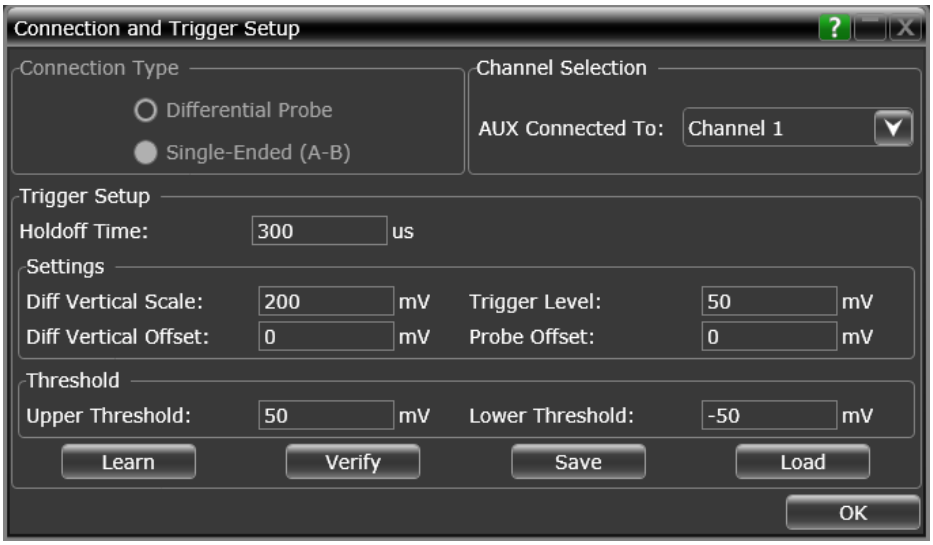


4 Click the **Connection Setup** button that now appears on the **Set Up** tab.

5 On the **Connection and Trigger Setup** window,

a The **Connection Type** area is grayed out.

b From the **AUX Connected To:** drop-down options of the **Channel Selection** area, select the Oscilloscope Channel where the Auxiliary Lane is connected to.



c In the **Trigger Setup** area, define the Oscilloscope parameters to trigger on an Auxiliary signal during testing.

- **Hold Off Time** – The Oscilloscope minimum hold off time before triggering the next waveform. Note that any Auxiliary transaction from the source must receive a reply from the sink in 400 us, else such a transaction is considered a timeout. Hold off time, in such cases, represents the minimum idle time before each AUX transaction is initialized. It is defaulted to 300 us which is a safe timing value for most devices tested in the lab. Most devices respond much faster than 300 us.
- **Trigger Level** – The AUX Channel signal level on which to trigger. Note that for a bi-directional signal (where a reference sink is attached), you must set the trigger level such that it crosses both the source command and the sink reply signal. Figure 225 and Figure 226 shows correct and incorrect trigger levels.

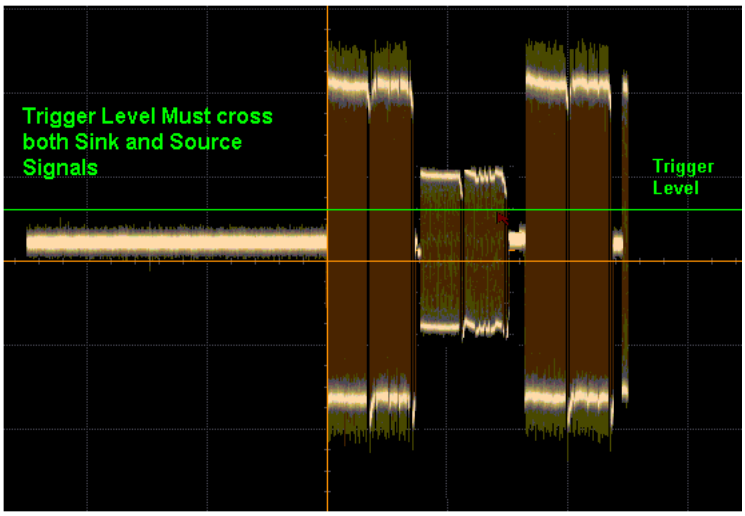


Figure 225 Correct Trigger Level

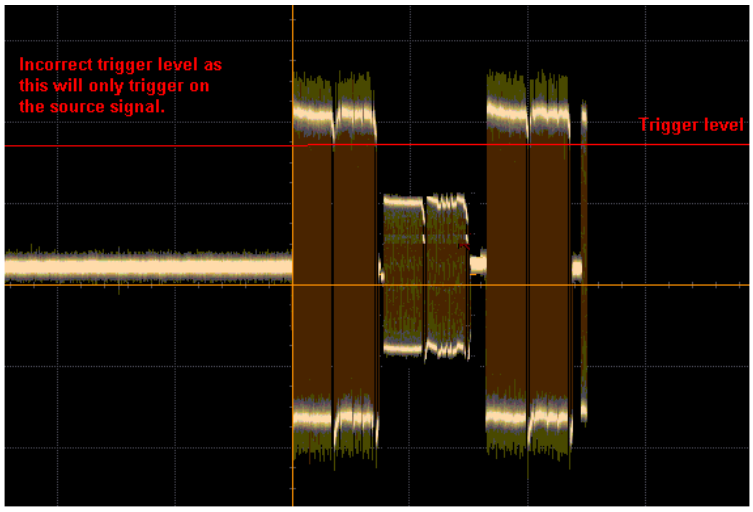


Figure 226 Incorrect Trigger Level

- **Vertical Scale** – The Oscilloscope vertical scale. Set the vertical to make sure that all signals are visible on the oscilloscope display.
- **Vertical Offset** – The Oscilloscope vertical offset. Set the offset so that the center point is aligned with the center of the oscilloscope display.
  Upper Threshold/Lower Threshold – The threshold level of signal must be set properly so that both upper and lower thresholds cross both the source and sink signals when the DUT is attached with a reference sink. The threshold levels are important parameters because they are used for edge detection when decoding a source command from a sink reply. Figure 227 and Figure 228 shows correct and incorrect threshold levels.

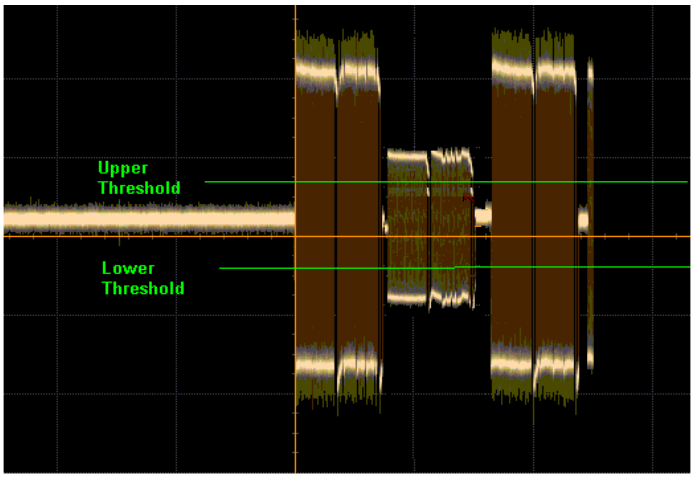


Figure 227 Correct Threshold set

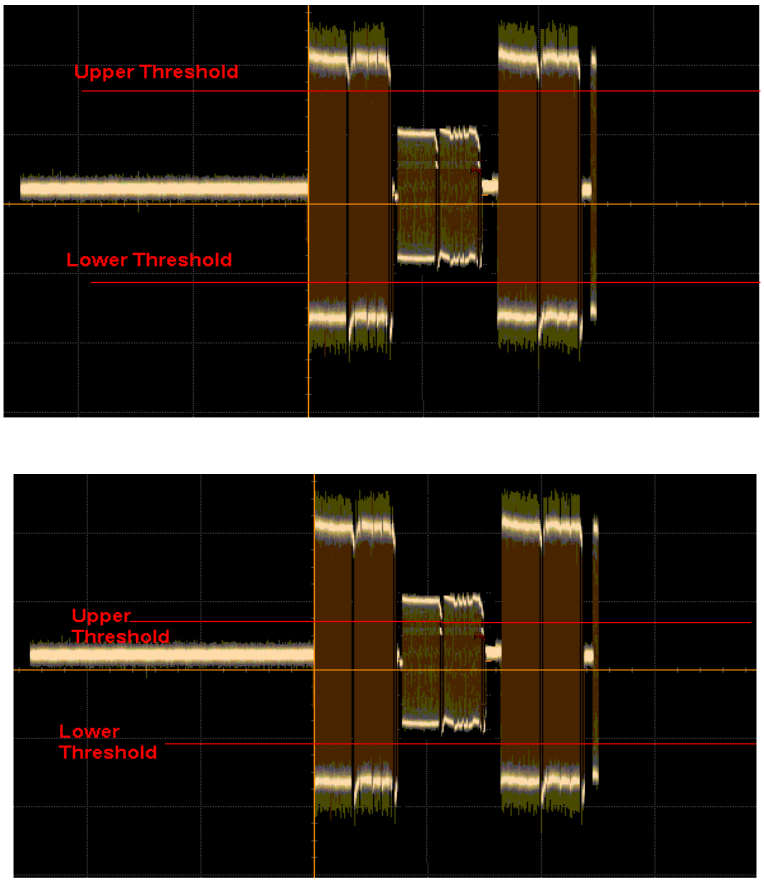


Figure 228 Wrong Thresholds set

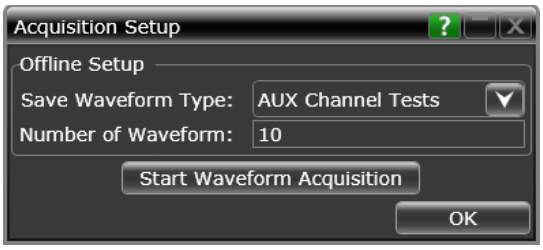
- Click the **Learn** button to access the information guide about the trigger setup parameters. However, note that the learning guide may not necessarily work due to variation in the actual Auxiliary signals, owing to different manufacturers. Keysight recommends that you must check to make sure that the parameters are correctly set as previously described.

- Click **Verify** and follow the instructions, if you wish to check the AUX Channel trigger.
- You may **Save** or **Load** the trigger setup configuration as a **.tsf* file.

6 Click **OK** to exit the **Connection and Trigger Setup** window.

7 If you select the option **Offline** for the **Acquisition Mode** in the **Test Setup** window, the **Acquisition Setup** button appears in the **Test Environment Setup** area of the **Set Up** tab.

8 Click the **Acquisition Setup** button to save the waveform files so that you can avoid the manual process to initiate Auxiliary transactions during the time of test runs.



9 On the **Acquisition Setup** window,

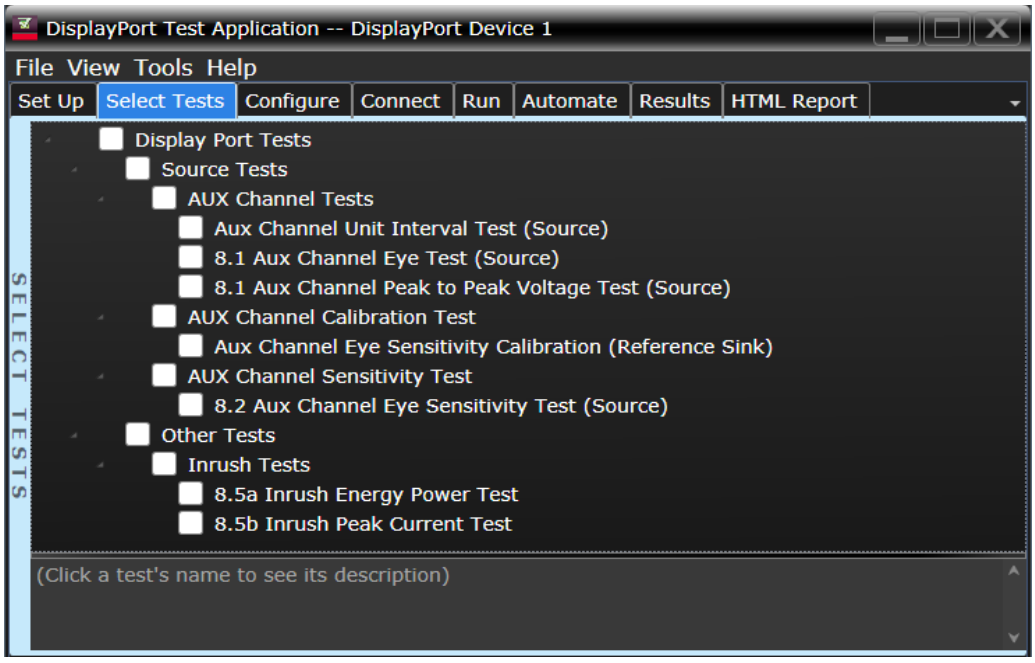
a select the type of waveforms to be saved from the **Save Waveform Type:** drop-down options.

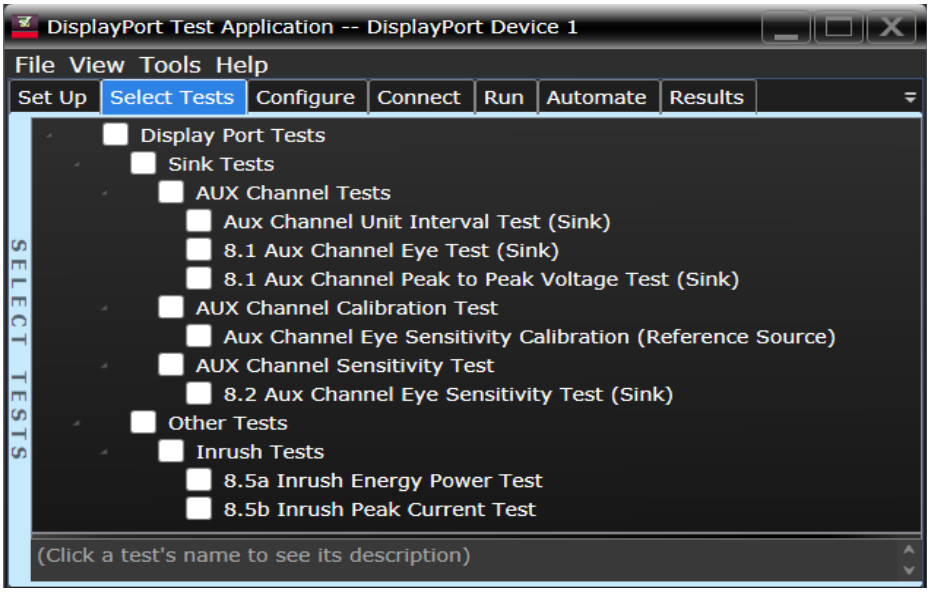
b define the number of waveforms to be saved in the **Number of Waveform:** field.

c Click the **Start Waveform Acquisition** button to start capturing and saving waveforms.

d Click **OK** to return to the **Set Up** tab.

10 Click the **Select Tests** tab where the AUX Channel tests for Source or Sink devices appear.





Probing/Connection Set Up for AUX Channel Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests. When performing the Source AUX Channel tests, a Reference Sink device is required. Similarly, when performing the Sink AUX Channel tests, a Reference Source device is required.

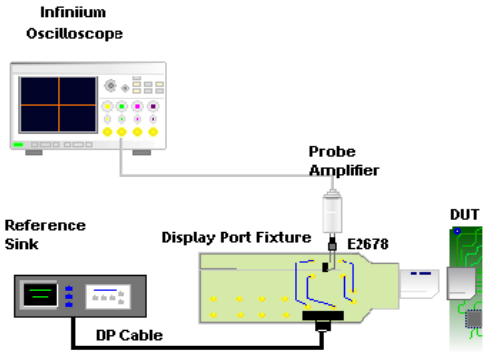


Figure 229 Sample connection diagram for source AUX channel tests with source DUT connected to a reference sink

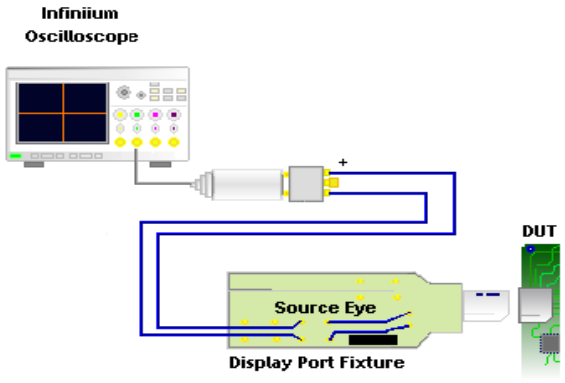


Figure 230 Sample connection diagram for source AUX channel tests without connecting to a reference sink

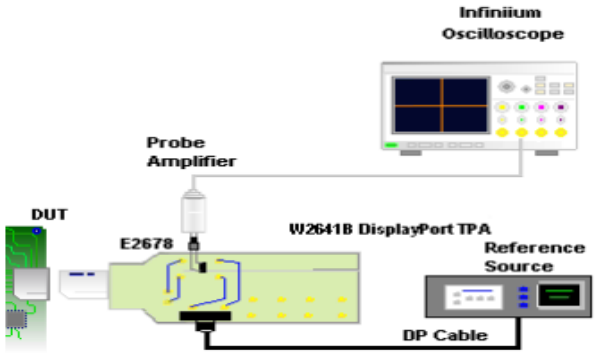


Figure 231 Sample connection diagram for sink AUX channel tests with sink DUT connected to a reference source

AUX Channel Unit Interval Test

Test ID

125000 – AUX Channel Unit Interval Test (Source)

125010 – AUX Channel Unit Interval Test (Sink)

Test Overview

The objective of the test is to evaluate the AUX Channel waveform, ensuring that the overall variation of the Manchester transaction Unit Interval stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Set up the parameter of the measurement trend:

   a Set up the Unit Interval measurement for the differential AUX Channel signal.

   b Set up the frequency measurement for the Clock signal.

   c Set up the measurement trend.

6 Set up the waveform Histogram on the measurement trend:

   a Initialize AUX Channel transactions and acquire the differential AUX Channel signal.

   b Identify the first and the last points for the desired transaction.

   c Zoom-in on the desired transaction.

   d Set up the Vertical Waveform Histogram on the measurement trend within the desired transaction.

   e Obtain the measurement for the mean, maximum and minimum values of the waveform Histogram.

7 Repeat step 6 ten times.

8 Report the measurement results.

PASS Condition

Manchester Transaction Unit Interval (UI_{MAN}):

Minimum = 0.4 µsec

Maximum = 0.6 µsec

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 2, Table 2-2*

Expected/Observable Results

The measured unit interval for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Test

Test ID

125001 – AUX Channel Eye Test (Source)

125011 – AUX Channel Eye Test (Sink)

Test Overview

The objective of this test is to evaluate the transmitter AUX Channel waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

7 Set up the waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

8 Set up the parameters for the Mask Test.

   a Load the eye mask based on the settings in the Configuration Variable.

   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

   c Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.

9 Check for any signal trajectories entering into the mask.

10 Report the measurement results.

PASS Condition

PASS Value = 290mV_diff_pp or higher

FAIL Value = lower than 290mV_diff_pp

Table 250 Eye Mask Vertices for AUX Channel for Manchester Transactions

Mask Point	Time (from EYE Center)	Minimum Voltage Value at Six Vertices (mV)
1	-185ns	0
2	-135ns	145
3	135ns	145
4	185ns	0
5	135ns	-145
6	-135ns	-145

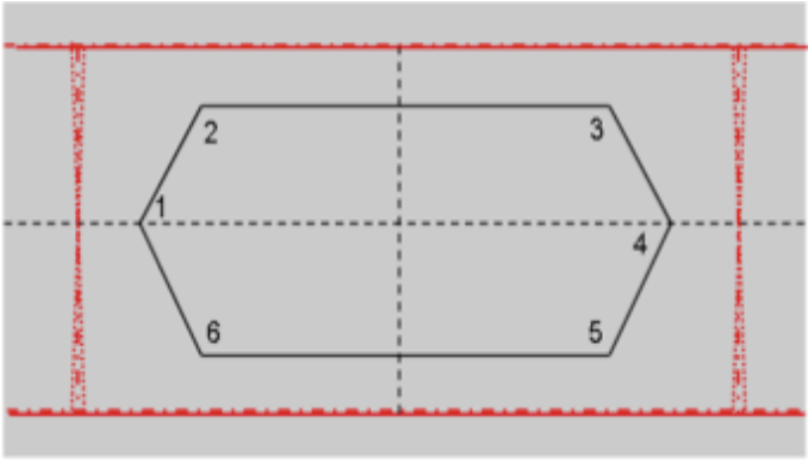


Figure 232 AUX Channel EYE Mask for Manchester Transactions

Mask Test: Zero mask failures.

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 2, Table 2-1 and Table 2-2*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2.6, Figure 3-29 and Table 3-8*

Expected/Observable Results

The measured eye diagram for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

AUX Channel Peak-to-Peak Voltage Test

Test ID

125002 – AUX Channel Peak-to-Peak Voltage Test (Source)

125012 – AUX Channel Peak-to-Peak Voltage Test (Sink)

Test Overview

The objective of the test is to evaluate the transmitter AUX Channel Waveform, ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1. Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.
2. Generate FUNC1 signal, which is the first differential signal of the AUX Channel.
3. Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).
4. Set up the parameter of the measurement:
   a. Enable measurement of all edges to obtain a statistical value of the measurement.
   b. Set up the measurement threshold.
   c. Set up the Clock Recovery.
5. Generate FUNC3 signal, which is the second differential signal of the AUX Channel.
6. Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7. Set up the horizontal waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.
8. If you have selected the “AUX Channel Eye Test” under the **Select Tests** tab of the compliance application:
   a. Set up the parameter of the Mask Test:
      i. Load the eye mask based on the settings in the Configuration Variable.
      ii. Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.
      iii. Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.
   b. Check for any signal trajectories entering into the mask.
9. Report the measurement results.

PASS Condition

Table 251 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage at a transmitting device ($V_{AUX-DIFFp-p}$)	0.29V	1.38V

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 2, Table 2-1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured peak-to-peak voltage for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Calibration Test

Test ID

125021 – AUX Channel Eye Sensitivity Calibration (Reference Sink)

125031 – AUX Channel Eye Sensitivity Calibration (Reference Source)

Test Overview

The objective of this test is to calibrate the peak-to-peak voltage of the transmitter AUX Channel waveform by reference device (reference source or reference sink), ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.

2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

4 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

5 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

6 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

7 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

8 Set up the waveform Histogram on the AUX Channel eye diagram:

   a Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.

   b Set up the vertical waveform Histogram of width 0.6 UI at the center of the AUX Channel eye diagram.

   c Measure the V_{TOP} and V_{BASE} using the waveform Histogram mean value.

9 Repeat Step 8 three times.

10 Report the measurement results.

PASS Condition

Table 252 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage for AUX Channel Eye Sensitivity	0.24V	0.28V

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured peak-to-peak voltage for the AUX Channel signal by reference device (reference source or reference sink) shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Test

Test ID

125041 – AUX Channel Eye Sensitivity Test (Source)

125051 – AUX Channel Eye Sensitivity Test (Sink)

Test Overview

The objective of the test is to evaluate the sensitivity to the AUX Channel Eye Opening of the DUT as per the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.
2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.
3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery.
5 Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.
6 Check if the reference device could detect the transaction or not.
7 Decode the AUX Channel signal and check whether the transaction passed or failed.
8 Report the measurement results.

PASS Condition

Determine whether the AUX Channel communication is successful. For example, the Transmitter DUT sends an AUX Request to the Reference Receiver. The Reference Receiver acknowledges and the Transmitter DUT responds to the to indicate that the acknowledgment was successfully received.

PASS = No errors observed in the response

FAIL = One or more errors observed

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured AUX Channel transaction shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

34 MyDP 1.0 Inrush Tests

Overview

This section describes the normative and informative inrush tests for compliance verification of Mobility DisplayPort source and sink, which is a power consumer.

Test Point for MyDP 1.0 Inrush Tests

The test fixture for inrush tests implements the schematic shown in Figure 233.

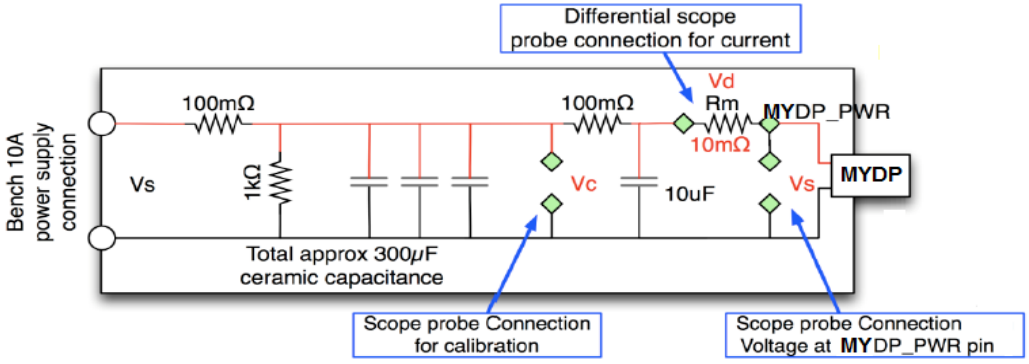


Figure 233 Schematics for testing a Power Consumer Device

The test fixture must be designed and used according to the following guidelines:

- A high gate voltage FET on the MyDP_PWR line is recommended to allow a fast connect capability, which allows a single connection event for testing. Without such an arrangement, multiple connections will be required to obtain a reasonable “worst-case” attachment event.
- Connection length between the power supply and the test fixture must be minimized. A maximum of four inches is recommended.
- The power supply must have enough outrush capability as to not negatively affect the test fixture’s outrush capability.
- The power supply must be run at 5.5V (5.0V + 10%) read across V_C.

Any Power Consumer test fixture must be calibrated using the Power User test fixture, as shown in Figure. Testing with the two fixtures combined should result in the approximate values given below. If required, the component values on the Power Consumer test fixture should be adjusted to match the expected results.

For Source:

- V_C steady before connection = 5.5V
- Inrush Current = ~9.0A

For Sink:

- V_C steady before connection = 3.6V
- Inrush Current = ~13.0A

Setting Up the DisplayPort Compliance Test Application for MyDP 1.0 Inrush Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort MyDP 1.0 Standards, select the option **MyDP 1.0** in the **Test Specification** area.
5. Select the option **AUX PHY and Inrush Tests** in the **Test Selection** area.
6. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
7. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
8. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
9. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
10. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
11. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
12. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
13. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Refer to "Settings for AUX PHY and Inrush Tests" on page 1191 for instructions on setting the MyDP 1.0 InRush tests.

Inrush Energy Power Test

Test ID

127000 – Inrush Energy Power Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush energy power measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Current $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 9$ Amps

Test References

See:

For Source:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.5*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 6*

For Sink:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 3.4*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 6*

Expected/Observable Results

The measured worst case inrush energy power for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Inrush Peak Current Test

Test ID

127001 – Inrush Peak Current Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush peak current measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Current $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 9$ Amps

Test References

See:

For Source:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.5*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 6*

For Sink:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 3.4*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 6*

Expected/Observable Results

The measured worst case inrush peak current for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

35 SlimPort Source Tests

Overview

This section describes the normative and informative tests for compliance verification of SlimPort source, sink and cable DUTs.

Test Point Definition for SlimPort

Five different test points are identified for the physical layer measurement. See Figure 234.

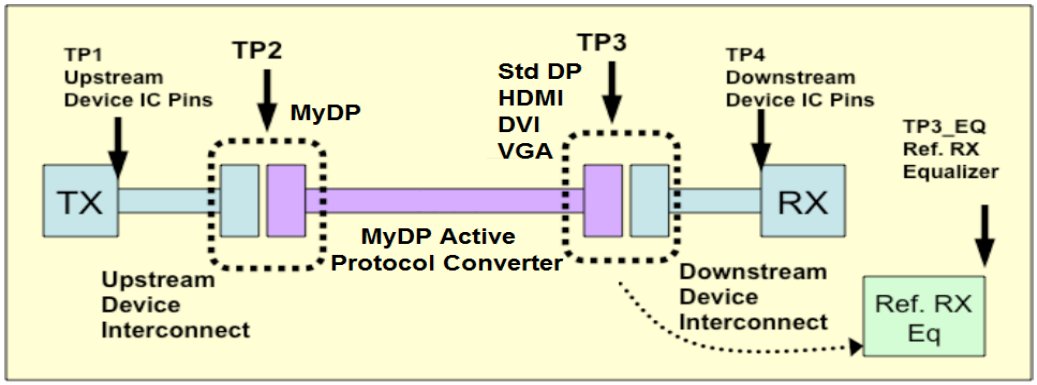


Figure 234 Test Points in a DisplayPort InterConnect System

Table 253 defines the Test Points used for SlimPort Tests:

Table 253 Test Points for DisplayPort Tests

Test Point	Description
TP1	At the pins of the Transmitter Device
TP2	At the test interface on a test access fixture as close as possible to the DP mated connection to a Source device
TP3	At the test interface on a test access fixture as close as possible to the DP mated connection to a Sink device
TP3_EQ	At TP3, when a defined cable model with equalizer is applied. There are two defined cable models: ▪ Worst Cable Model as defined in VESA DisplayPort 1.2a Standard, ▪ Zero length, zero loss cable. The equalizer is also defined in VESA DisplayPort 1.2a Standard
TP4	At the pins of a receiving device

Cable Models

The two cable models defined in VESA DisplayPort 1.2a Standard are:

1 Worst Case Cable Model—To achieve the TP3_EQ signal with the worst case cable model:

- Acquire the signal at TP2.
- Embed the TP2 signal with a “worst case” cable model using an InfiniiSim Waveform Transformation Toolset software to emulate the insertion loss as defined in Figure 4-10 of the VESA DisplayPort 1.2a Standard.
  - The “*CIC_rev0p6.s4p*” cable model transfer function is used.

- Finally, apply the HBR or HBR2 equalization using the Serial Data Equalization software as defined in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard.

2 Zero Length Cable Model—To achieve the TP3_EQ signal with the zero length cable model:

- Acquire the signal at TP2.
- No cable model is embedded for the Zero Length cable model.
- Finally, apply the HBR or HBR2 equalization using the Serial Data Equalization software as defined in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard.

Equalization

When equalization is required, use the CTLE (Continuous Time Linear Equalization) transfer function, as given in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard.

For main link, use the CTLE model with the following transfer function for HBR (2.7 Gbps):

The HBR Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s + \omega_z}{(s + \omega_{p1})(s + \omega_{p2})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{\sqrt{\omega^2 + \omega_z^2}}{\sqrt{\omega^2 + \omega_{p1}^2} \cdot \sqrt{\omega^2 + \omega_{p2}^2}}$$

where

$$\omega_z = 2\pi(0.725 \times 10^9)$$
$$\omega_{p1} = 2\pi(1.35 \times 10^9)$$
$$\omega_{p2} = 2\pi(2.5 \times 10^9)$$

Figure 235 Transfer Function of the CTLE model for HBR

Table 254 CTLE Model for HBR

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
Gain	1.0	1.0
Zero Frequency	0.725 GHz	0.725 GHz
Pole 1 Frequency	1.35 GHz	1.35 GHz
Pole 2 Frequency	2.5 GHz	2.5 GHz

For main link, use the CTLE model with the following transfer function for HBR2 (5.4 Gbps):

The HBR2 Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})(s+\omega_{p3})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{\sqrt{\omega^2+\omega_z^2}}{\sqrt{\omega^2+\omega_{p1}^2}\cdot\sqrt{\omega^2+\omega_{p2}^2}\cdot\sqrt{\omega^2+\omega_{p3}^2}}$$

where

$\omega z = 2\pi\ (0.64 \times 10^9)$ for upstream device compliance

and

$\omega p1 = 2\pi\ (2.7 \times 10^9)$

$\omega p2 = 2\pi\ (4.5 \times 10^9)$

$\omega p3 = 2\pi\ (13.5 \times 10^9)$

Figure 236 Transfer Function of the CTLE model for HBR2

Table 255 CTLE Model for HBR2

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
Gain	1.0	1.0
Zero Frequency	0.64 GHz	0.64 GHz
Pole 1 Frequency	2.7 GHz	2.7 GHz
Pole 2 Frequency	4.5 GHz	4.5 GHz
Pole 3 Frequency	13.5 GHz	13.5 GHz

For main link, use the following CTLE parameters for HBR25 (6.75 Gbps):

- DC-Gain = 1.0
- Zero = 1 GHz
- Pole1 = 3.75 GHz
- Pole2 = 13.5 GHz
- Pole3 $\geq$ 13.5 GHz

Table 256 CTLE Model for HBR25

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
Gain	1.0	1.0
Zero Frequency	1.0 GHz	2.0 GHz
Pole 1 Frequency	5.625 GHz	3.375 GHz
Pole 2 Frequency	13.5 GHz	5.625 GHz
Pole 3 Frequency	13.5 GHz	16.875 GHz

Clock Recovery

When Clock Recovery is required, the clock recovery technique follows the definition of the receiver PLL as defined in Section 3.5.3.5 of the VESA DisplayPort 1.2a Standard. For main link, use the second-order clock recovery function with a closed loop tracking bandwidth and damping factor, with respect to the PRBS7 pattern, as shown in Table 257:

Table 257 Main Link Second-Order Clock Recovery Function

Bit Rate	Bandwidth	Damping Factor
HBR25 (6.75 Gbps)	10 MHZ	1.00
HBR2 (5.4 Gbps)	10 MHz	1.00
HBR (2.7 Gbps)	10 MHz	1.51
RBR (1.62 Gbps)	5.4 MHz	1.51

Test Point Definition for SlimPort Source Tests

Test the Source DUT at Test Point 2 (TP2) as shown in Figure 237.

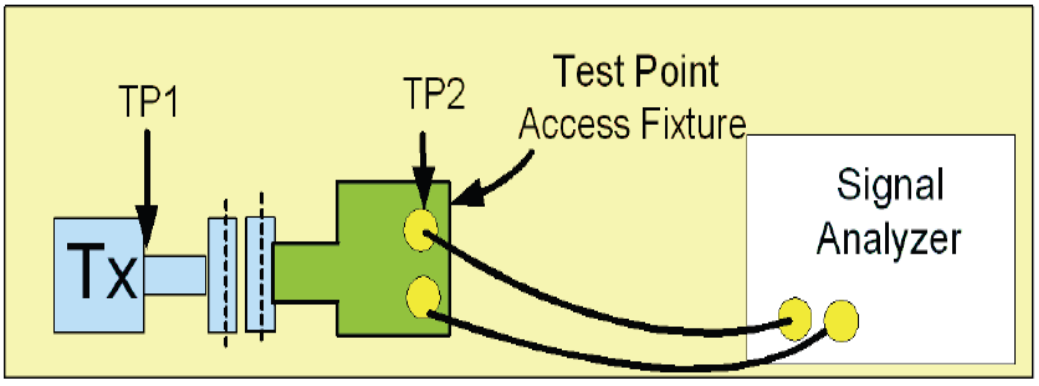


Figure 237 Test Point 2 Connection for SlimPort Source Tests

Use MyDP Test Fixtures (MyDP-to-DP type or MyDP-to-SMA type) to perform PHY compliance tests specific to SlimPort. Figure 238 shows the layout of a MyDP passive cable adapter or a MyDP protocol converter:

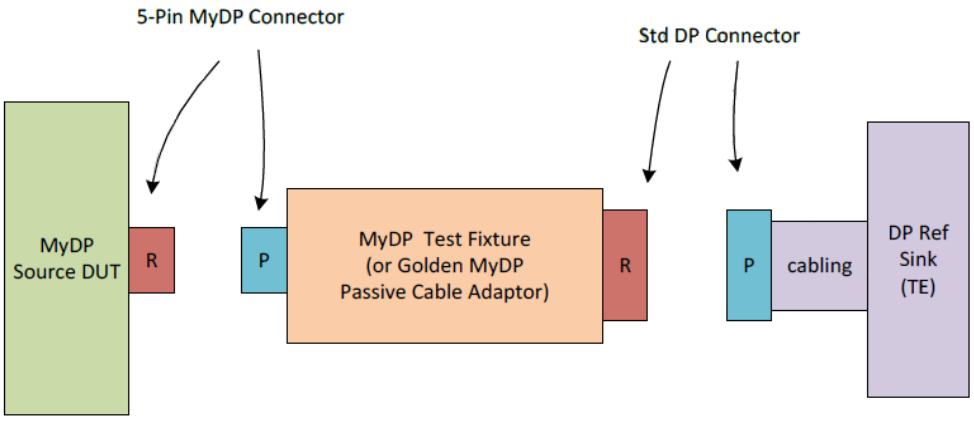


Figure 238 Schematics of SlimPort to SMA Test Fixtures used for PHY Compliance Tests

Table 258 defines the test point fixtures and instruments used for SlimPort (MyDP HBR25) Source Tests:

Table 258 Test Point Fixtures and Instruments for SlimPort (MyDP HBR25) Source Tests

Test Requirement	Device Used
Test Point Access Fixture	Mobility DisplayPort Test Point Adapter For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort SlimPort Standards, select the option **MyDP HBR25** in the **Test Specification** area.

5 The option **Physical Layer Tests** appears by default in the **Test Selection** area.

6 Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.

7 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

8 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

9 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

10 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

11 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

12 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

13 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

14 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for SlimPort Source Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

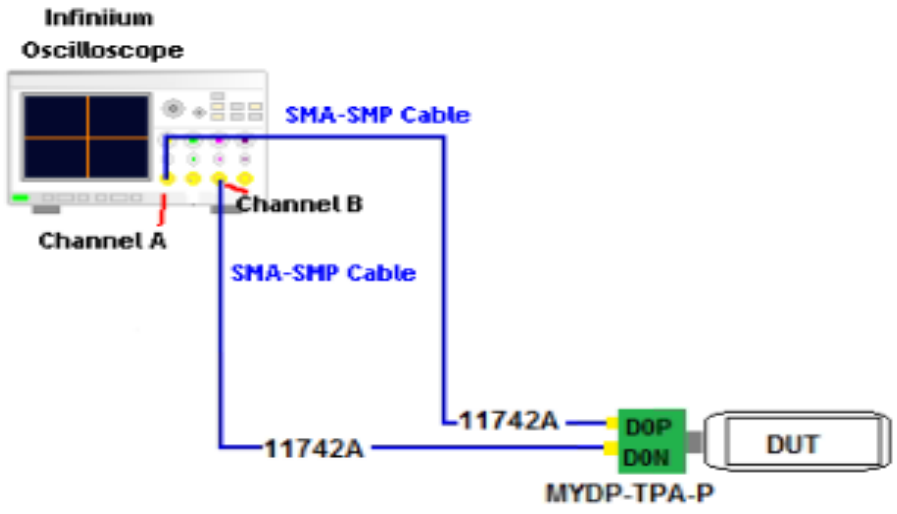


Figure 239 Sample connection diagram for SlimPort Source Tests

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Source tests (either differential or single-ended) to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1 In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.

2 On the **Test Setup** window,

a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b In the **DUT Info** area, the **Device Type** is selected as **Source** by default.

c In the **Test Info** area, the **Test Type** is selected as **Differential Tests** by default. Select **Single-Ended Tests** from the drop-down options for the respective tests to appear in the **Select Tests** tab.

d In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.

3 Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1 Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.

2 On the **Connection Setup** window,

a Select the appropriate option in the **Fixture Type** to indicate where the DUT is connected to.

b Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.

c In the **Channel Selection** area, assign appropriate channels to lanes.

3 Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of source tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 1222 to complete the task flow for DUT setup along with configuring the Compliance Application to run each test.

Source Eye Diagram Test

Test ID

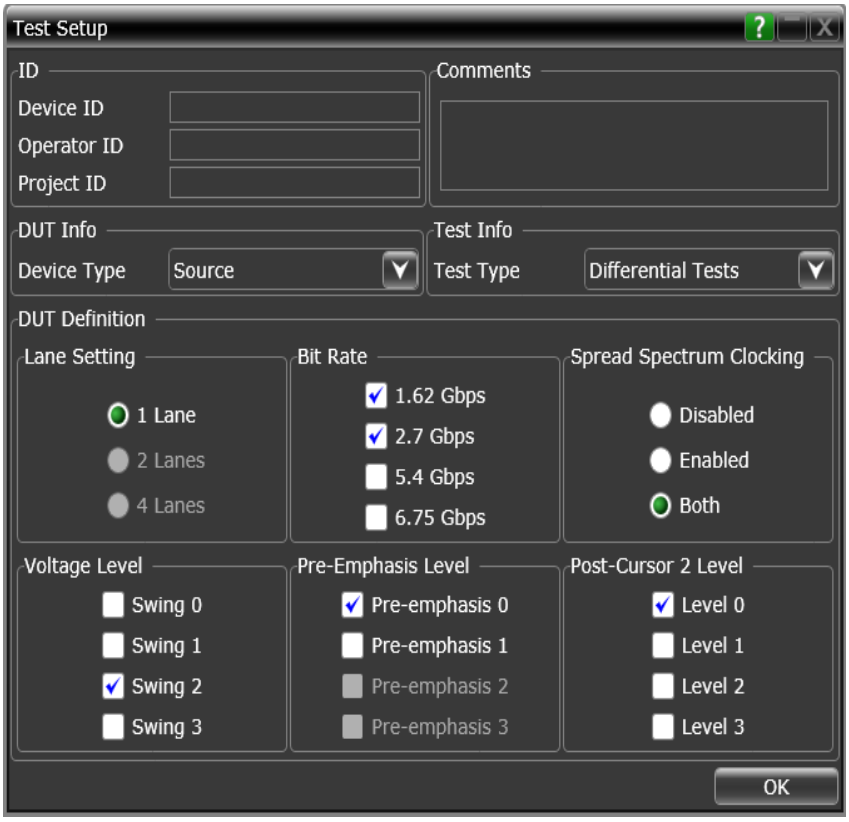
1210001 – Eye Diagram Test

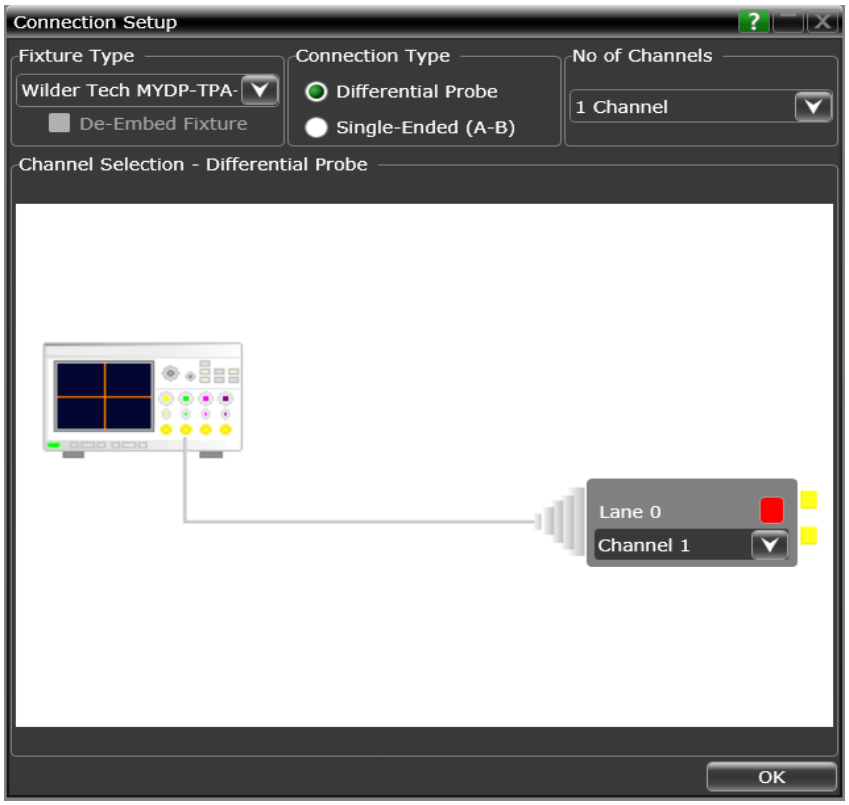
Test Overview

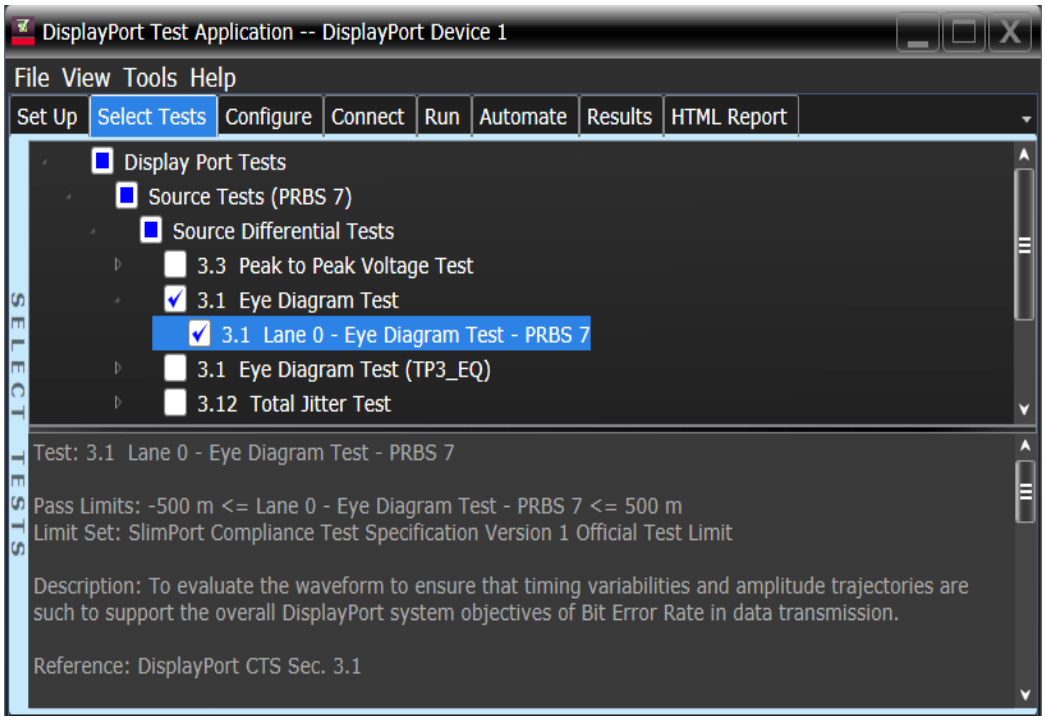
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Measure V_{TOP} and V_{BASE} of the input signal using the pattern folding.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the input signal eye diagram to measure the left edge.
7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the eye height of the eye diagram using the Histogram.
9 Measure the jitter of the eye diagram using the Histogram.
10 Calculate the eye width based on the measured jitter of the eye diagram.

11 Check for any signal trajectories that may have entered into the mask.

12 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 259 shows the voltage and time coordinates for the mask used in the eye diagram.

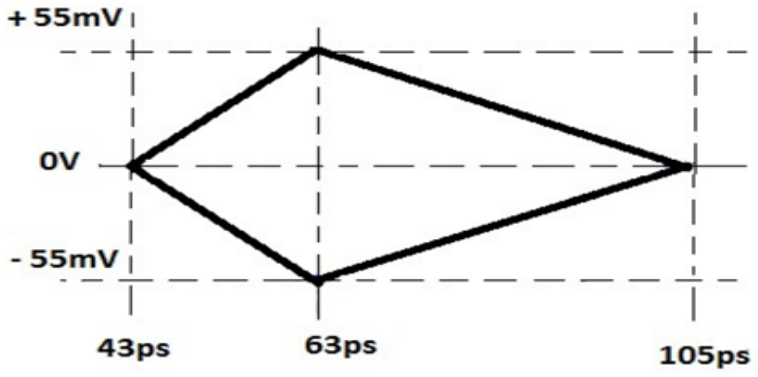


Figure 240 Eye Mask of Source at 6.75G

Table 259 Eye Diagram Mask Coordinates

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	High (2.7 Gb/s)
1	0.127, 0.000	0.210, 0.000
2	0.291, 0.160	0.355, 0.140
3	0.500, 0.200	0.500, 0.175
4	0.709, 0.200	0.645, 0.175
5	0.873, 0.000	0.790, 0.000
6	0.709,-0.200	0.645,-0.175
7	0.500,-0.200	0.500,-0.175
8	0.291,-0.160	0.355,-0.140

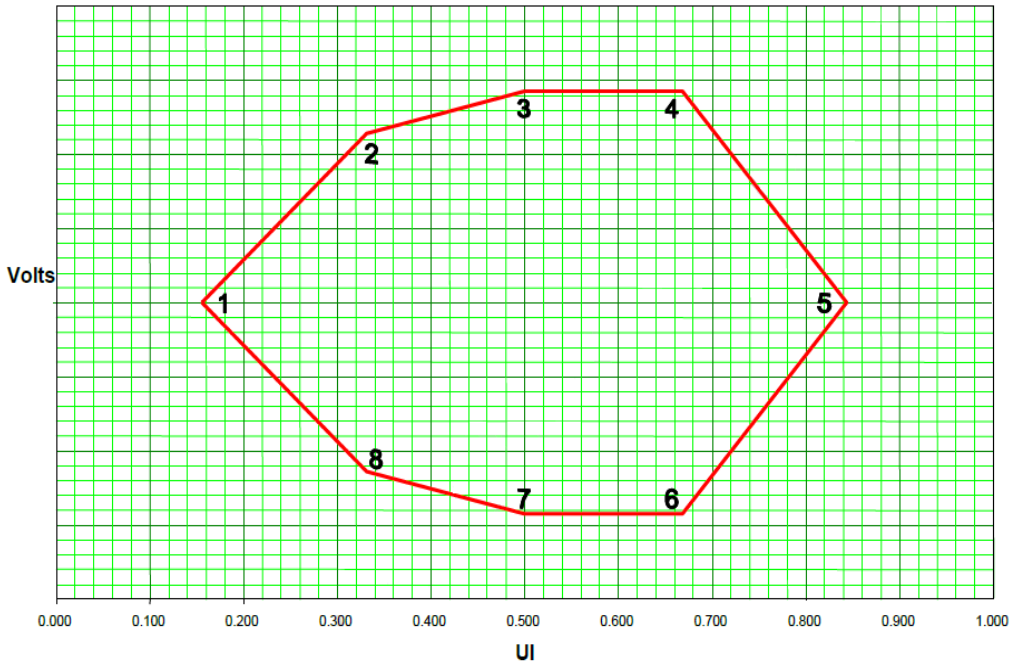


Figure 241 The Source Eye Mask

Mask Test: Zero mask failures.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-24 for RBR and Table 3-23 for HBR*

Expected/Observable Results

The measured eye diagram for the source degraded signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test

Test ID

1220001 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

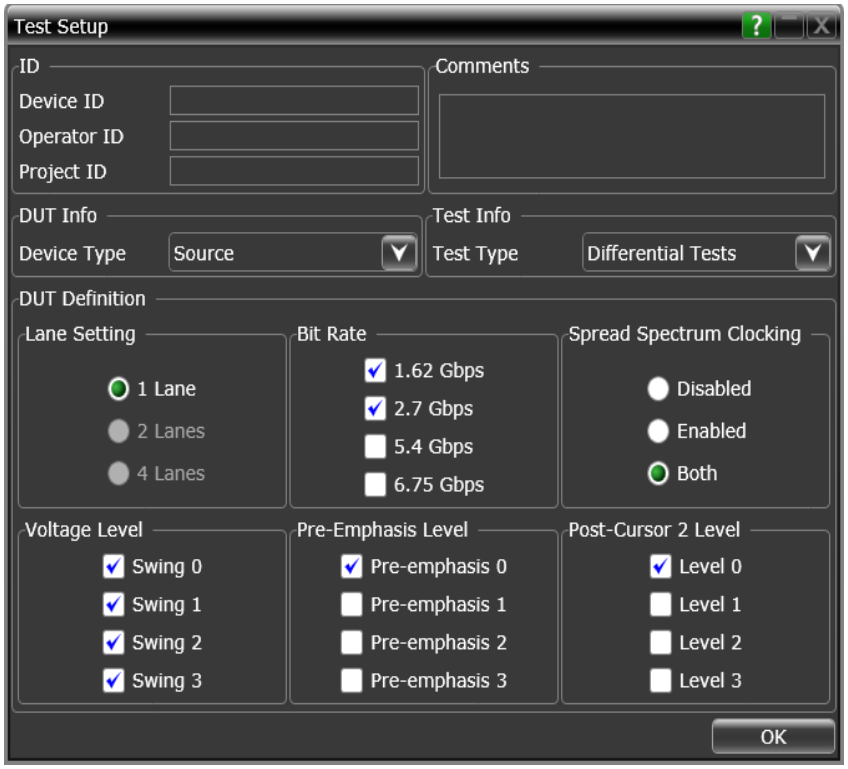
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

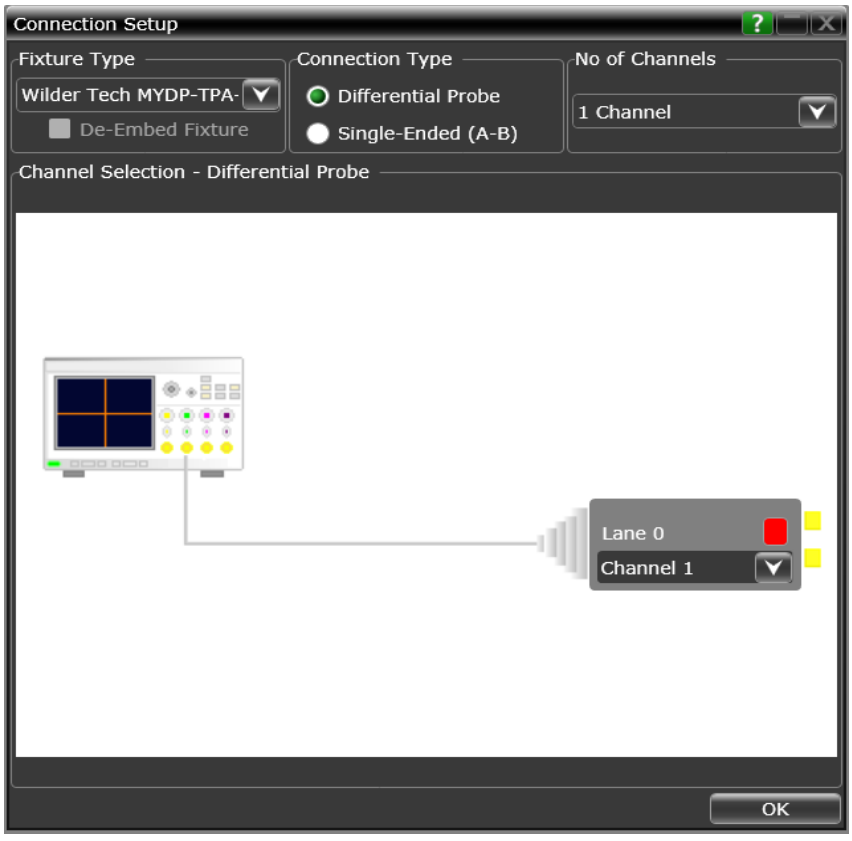
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

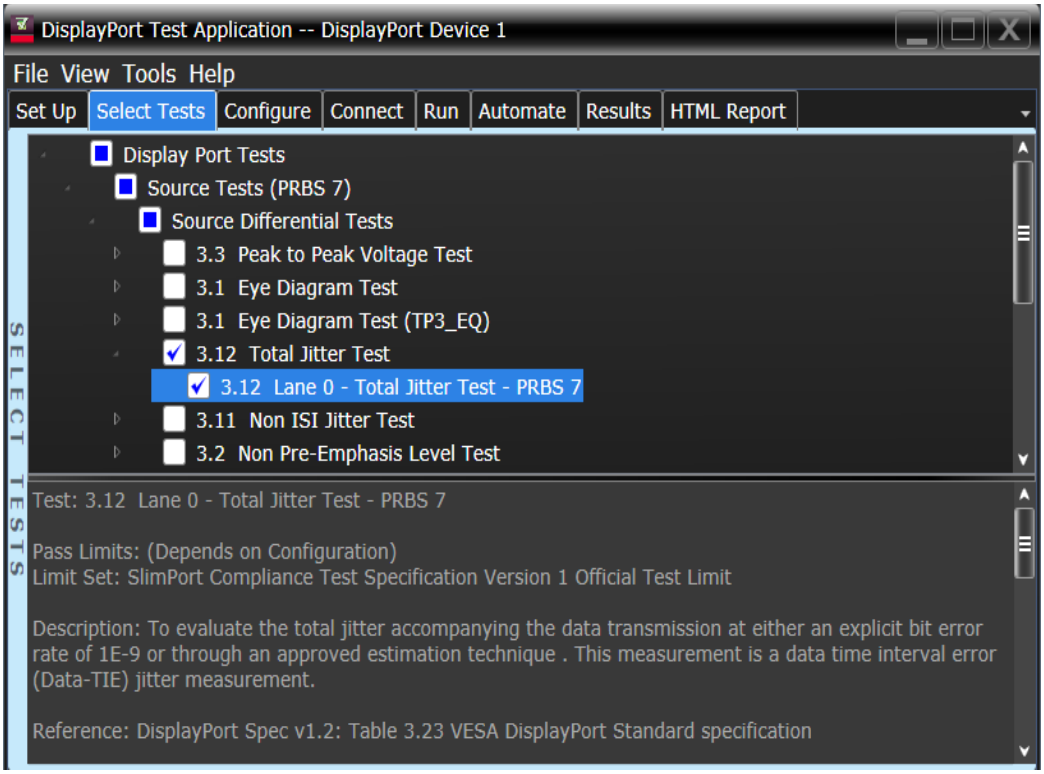
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Report the measurement results.

PASS Condition

Table 260 Total Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
Ap-p	0.294 UI	0.420 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
Ap-p	0.180 UI	0.270 UI

UI is Unit Interval.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non-ISI Jitter Test

Test ID

1230001 — Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the amount of Non ISI jitter accompanying the data transmission.

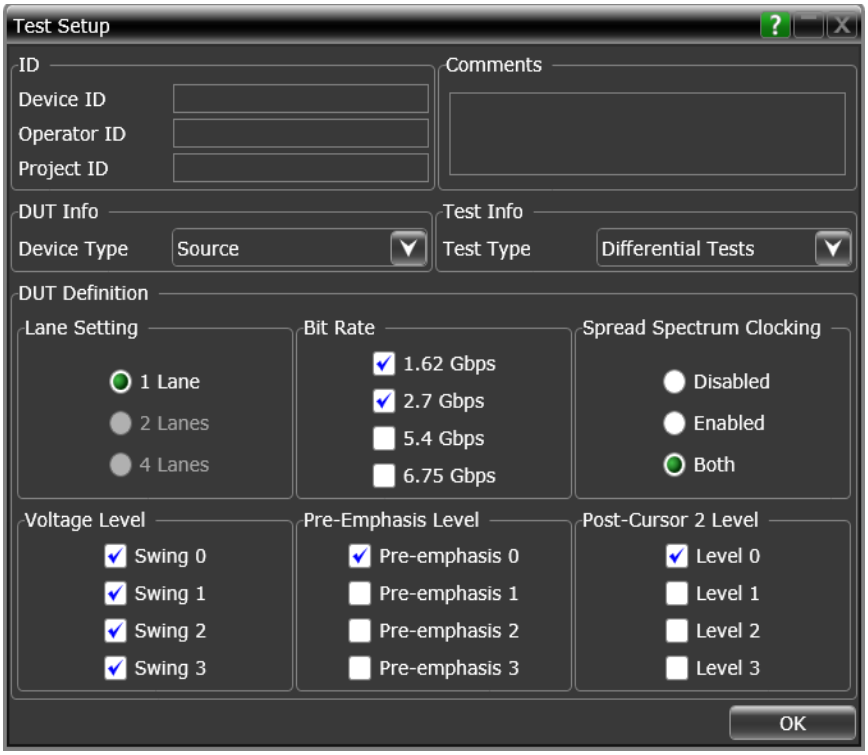
The jitter is separated into each jitter components based on the Dual-Dirac Model:

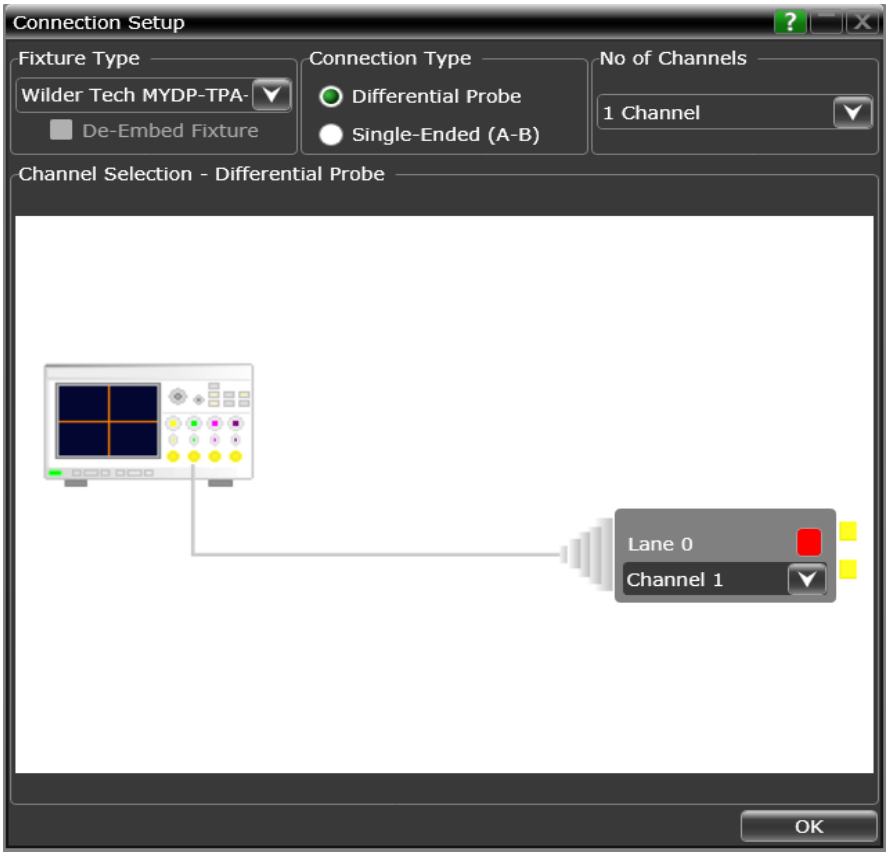
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

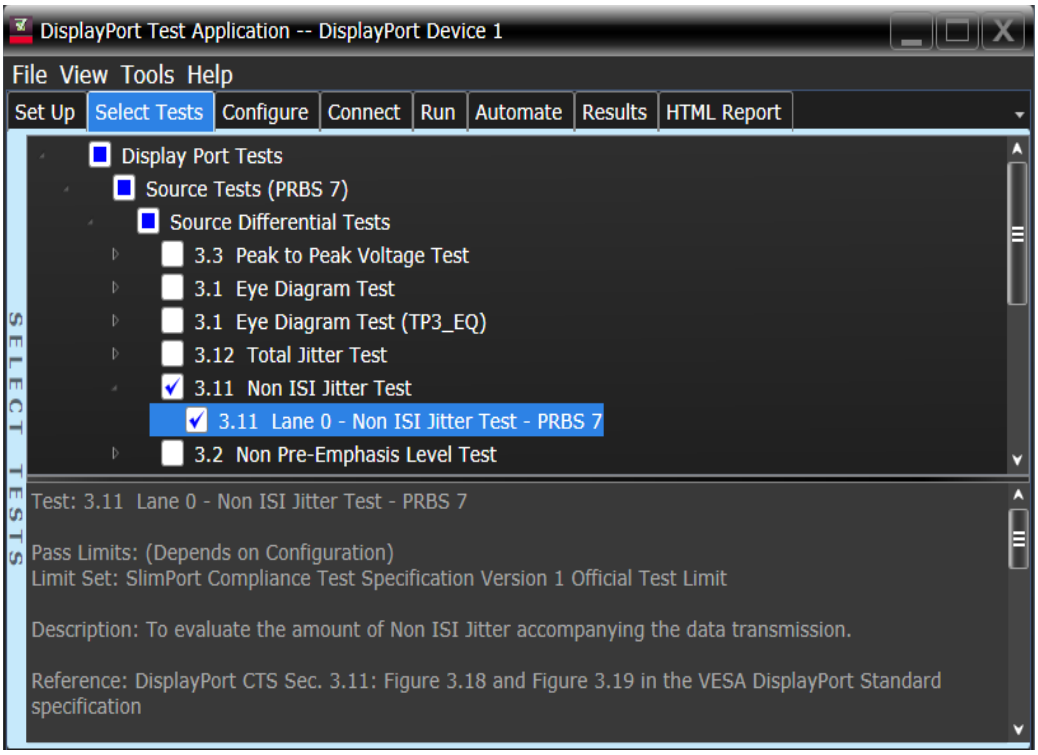
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Calculate the Non ISI jitter using the following equation:

$$\text{Non ISI Jitter} = \text{TJ} - \text{ISI}$$

7 Report the measurement results.

PASS Condition

Table 261 Non-ISI Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.260 UI	0.276 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.160 UI	0.210 UI

UI is Unit Interval.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.11*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Pre-Emphasis Level Test

Test ID

For RBR and HBR:

- 1261001 – Non Pre-Emphasis Level Test (Swing 1/Swing 0)
- 1262001 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263001 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

For HBR2 and HBR25:

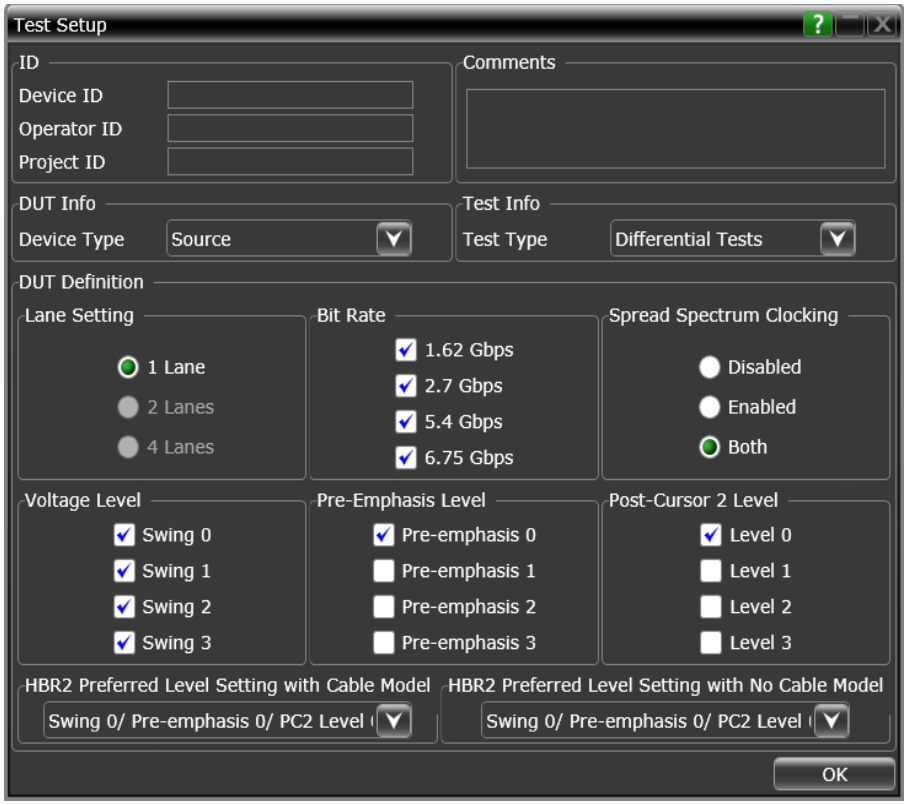
- 1264101 – Non Pre-Emphasis Level Test (Swing 2/Swing 0)
- 1262101 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263101 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

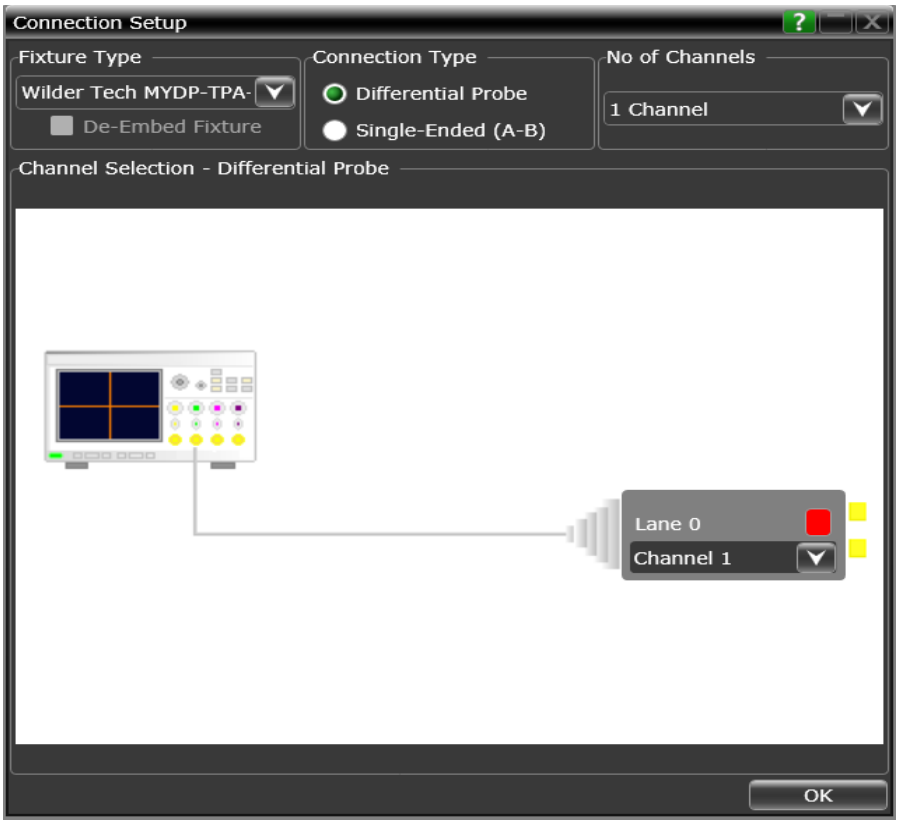
Test Overview

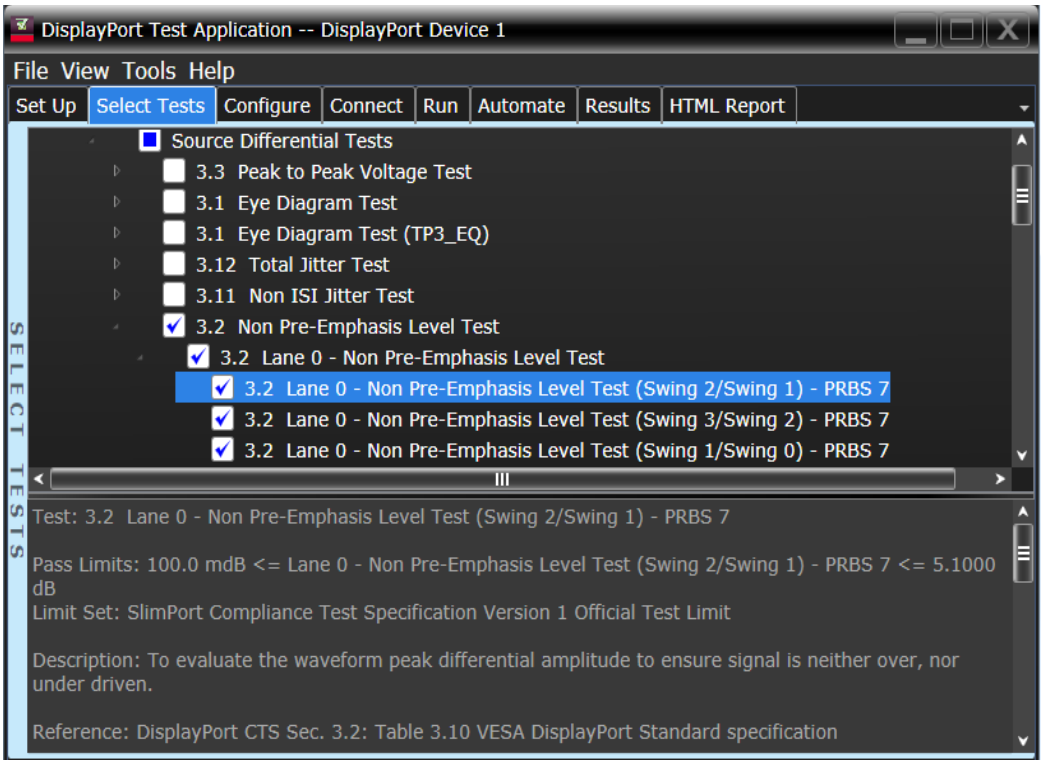
The objective of this test is to ensure that the system budget elements are obeyed and to ensure that the level settings are monotonic so that the sink relies on the source to incrementally increase upon request by the sink.

Test Conditions for Non Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR25)
SSC	Both SSC Conditions are supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR – PRBS7 HBR2 and HBR25 – PLTPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 For Voltage Level A with no pre-emphasis level:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.

- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6th bit of the seven successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4th bit of the four successive transmitted zeros of the pattern.

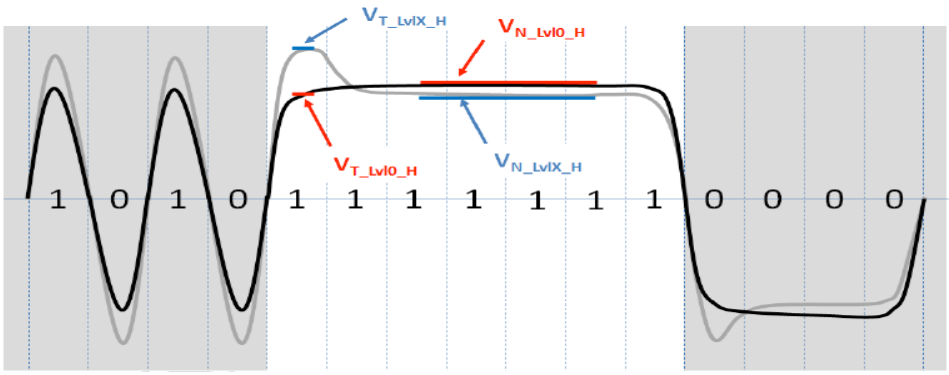


Figure 242 High Voltage measurement for RBR and HBR

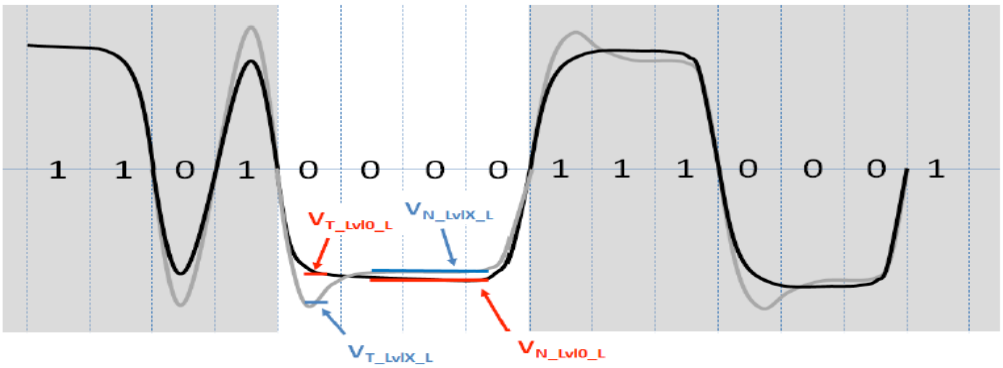


Figure 243 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR25 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

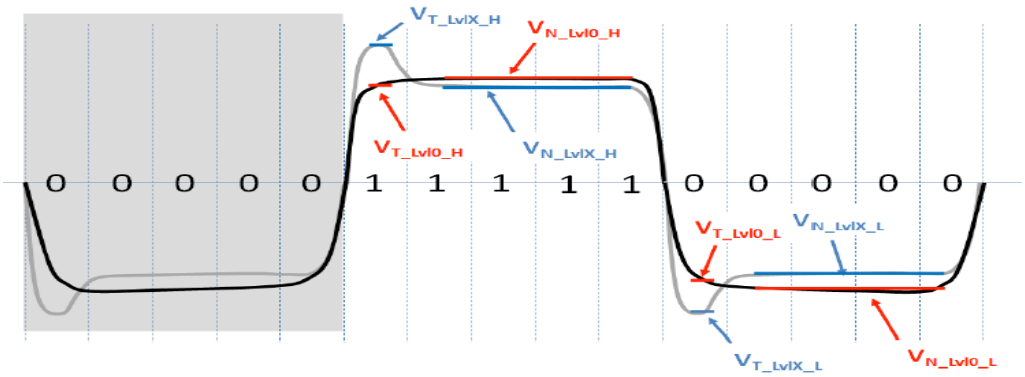


Figure 244 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_Lvl0\_PP} = V_{T\_Lvl0\_H} - V_{T\_Lvl0\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_Lvl0\_PP} = V_{N\_Lvl0\_H} - V_{N\_Lvl0\_L}$$

2 Repeat Step 1 for Voltage Level B with no pre-emphasis level.

3 Calculate the non pre-emphasis level output voltage ratio using the equation:

Non Pre-Emphasis Level = $20 * \text{Log}_{10}[\text{Voltage Level A } V_{N\_Lvl0\_PP} / \text{Voltage Level B } V_{N\_Lvl0\_PP}]$

4 Report the measurement results.

PASS Condition

For each level setting testes, the following equation should be used:

$\text{Resultant} = 20 * \text{Log}_{10}[\text{Voltage}_{\text{Peak-Peak\_LevelA}} / \text{Voltage}_{\text{Peak-Peak\_LevelB}}]$

Table 262 Compared Levels

Measurement#	$\text{Voltage}_{\text{Peak-Peak\_LevelA}}$	$\text{Voltage}_{\text{Peak-Peak\_LevelB}}$
RBR & HBR		
1	Level 1 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)
2	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
3*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)
HBR2 and HBR25		
4	Level 2 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)

Table 262 Compared Levels

Measurement#	$Voltage_{Peak\text{-}Peak\_LevelA}$	$Voltage_{Peak\text{-}Peak\_LevelB}$
5	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
6*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)

* if device optionally capable of Level 3

The resultants specifications are as identified below:

Measurement 1: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 2: 0.1 dB ≤ Resultant ≤ 5.1 dB

Measurement 3: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 4: 5.2 dB ≤ Resultant ≤ 6.9 dB

Measurement 5: 1.6 dB ≤ Resultant ≤ 3.5 dB

Measurement 6: 1 dB ≤ Resultant ≤ 4.4 dB

Table 263 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}OUTPUT\text{-}RATIO\_RBR\_HBR}$	Ratio of Output Voltage Level 1/Level 0	0.8	-	6.0	dB	Measured on non-transition bits at Pre-emphasis level 0 setting
	Ratio of Output Voltage Level 2/Level 1	0.1	-	5.1	dB	
	Ratio of Output Voltage Level 3/Level 2	0.8	-	6.0	dB	
$V_{TX\text{-}OUTPUT\text{-}RATIO\_HBR2}$	Ratio of Output Voltage Level 2/Level 0	5.2	-	6.9	dB	Measured on non-transition bits at Pre-emphasis level 0 setting
	Ratio of Output Voltage Level 2/Level 1	1.6	-	3.5	dB	
	Ratio of Output Voltage Level 3/Level 2	1	-	4.4	dB	

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured output voltage level ratio of the non pre-emphasis level test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Pre-Emphasis Level Test

Test ID

For RBR and HBR:

- 1270001 – Pre-Emphasis Level Test

For HBR2 and HBR25:

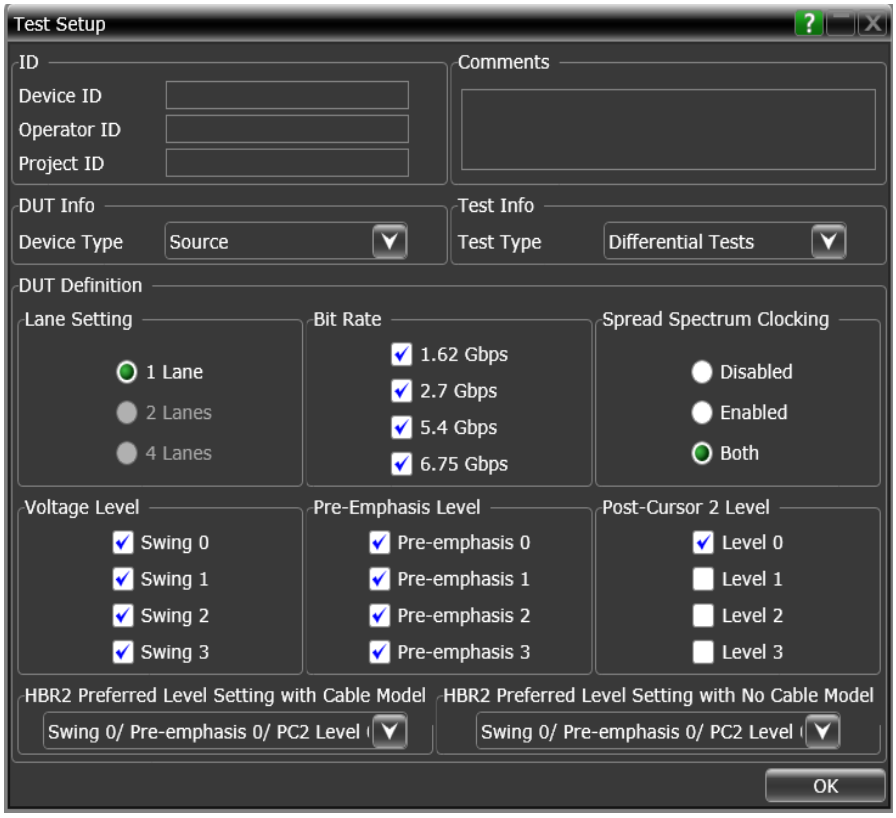
- 1270501 – Pre-Emphasis Level Test

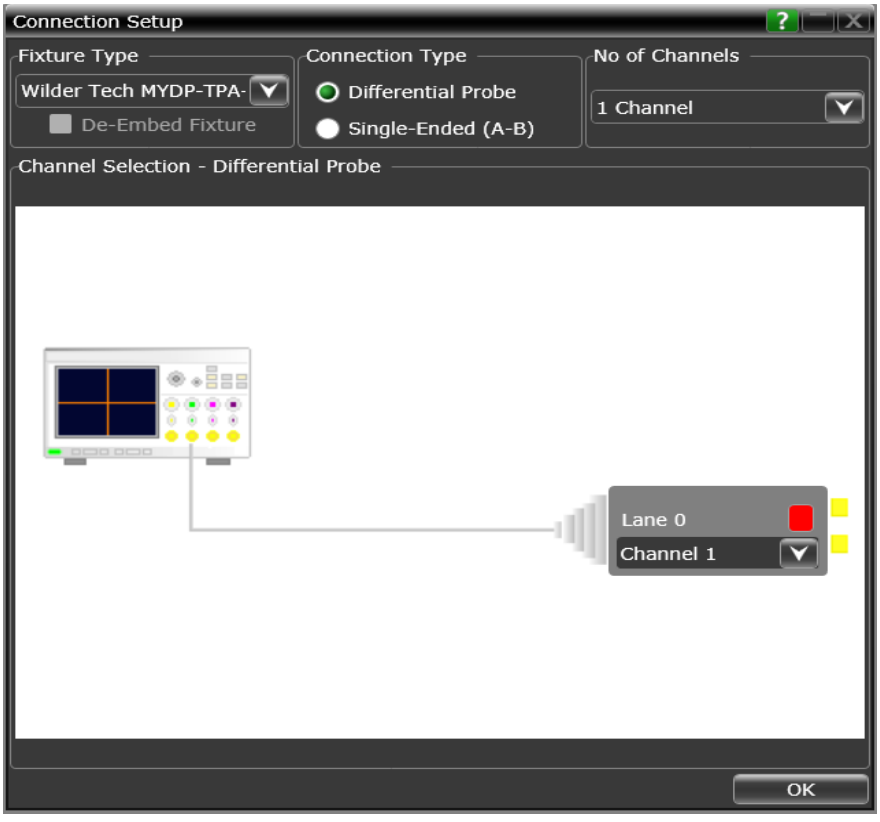
Test Overview

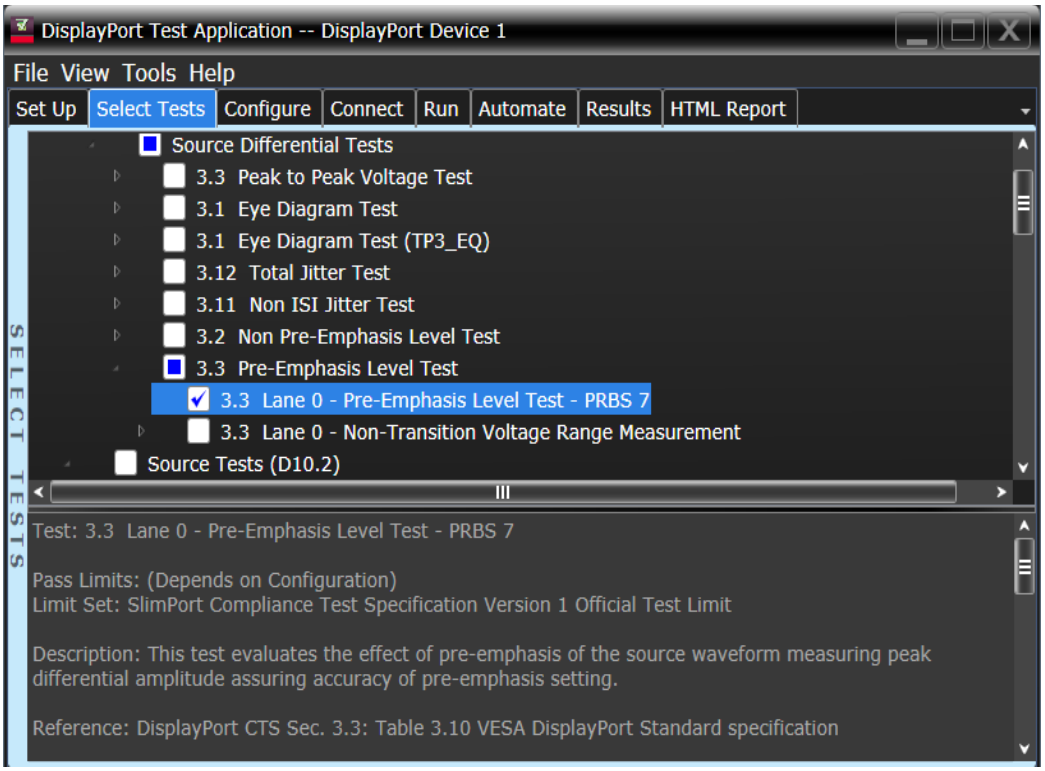
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings.

Test Conditions for Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR25)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels are supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR25 – PLTPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given Voltage Level and a Pre-Emphasis Level X:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.

- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6th bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4th bit of the four successive transmitted zeros of the pattern.

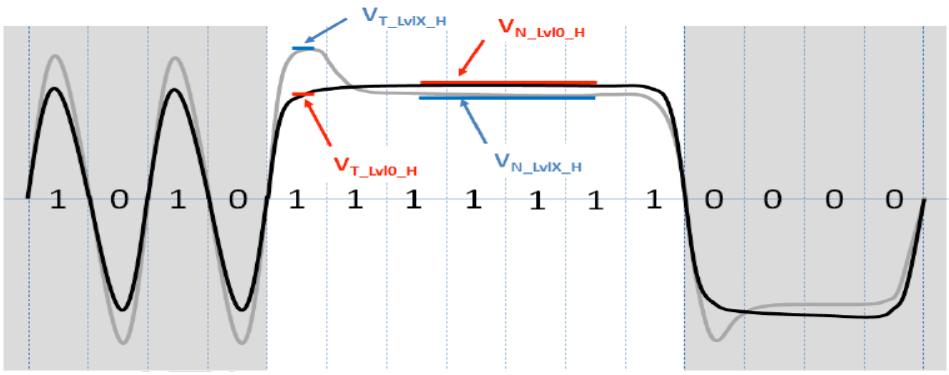


Figure 245 High Voltage measurement for RBR and HBR

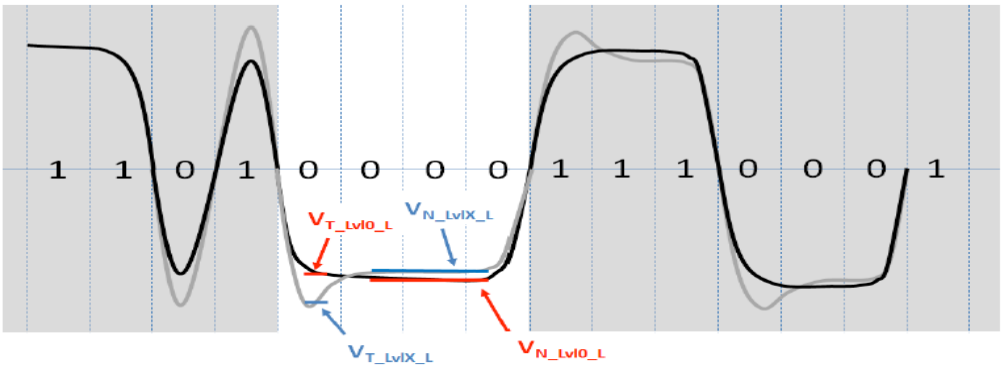


Figure 246 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR25 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

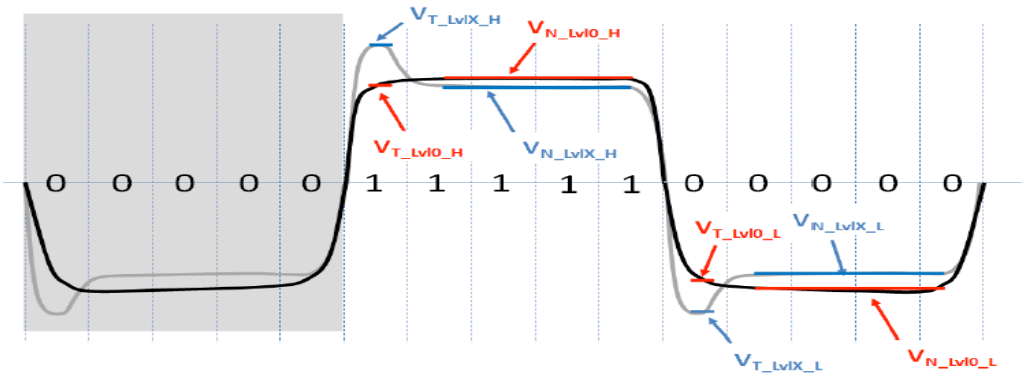


Figure 247 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

l Calculate the pre-emphasis level using the equation:

$$\text{Pre-Emphasis}_{LvlX} = 20 * \text{Log}_{10}[V_{T\_LvlX\_PP} / V_{N\_LvlX\_PP}]$$

2 For Pre-Emphasis Level 0 (no pre-emphasis level), the result for $\text{Pre-Emphasis}_{Lvl0}$ is compared with the maximum pre-emphasis disabled limit.

3 Repeat Step 1 for the next Pre-Emphasis level and for each Pre-Emphasis levels, compare the pre-emphasis delta with the pre-emphasis delta limits.

4 Calculate the pre-emphasis delta using the equation:

$$\text{Pre-Emphasis Delta (Level 1 vs Level 0)} = \text{Pre-Emphasis}_{Lvl1} - \text{Pre-Emphasis}_{Lvl0}$$

$$\text{Pre-Emphasis Delta (Level 2 vs Level 1)} = \text{Pre-Emphasis}_{Lvl2} - \text{Pre-Emphasis}_{Lvl1}$$

$$\text{Pre-Emphasis Delta (Level 3 vs Level 2)} = \text{Pre-Emphasis}_{Lvl3} - \text{Pre-Emphasis}_{Lvl2}$$

5 Report the measurement results.

PASS Condition

Pre-emphasis values for the Level 0 (OFF) state (Normative)

Level 0 (OFF) Pre-emphasis measurement:

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl0\_PP} / \text{Voltage}_{N\_Lvl0\_PP}]$ for all supported levels.

Level 0 (OFF) Pre-emphasis Measurement condition: +0.25 dB $\geq$ Resultant

Pre-emphasis Delta values for:

a Level 1 vs. Level 0 Pre-emphasis settings (NORMATIVE)

b Level 2 vs. Level 1 Pre-emphasis settings (NORMATIVE)

c Level 3 vs. Level 2 Pre-emphasis settings (NORMATIVE)

Pre-emphasis Delta measurements:

- Level 1 vs. Level 0

Resultant = 20 * Log [$Voltage_{T\_Lvl1\_PP}$ / $Voltage_{N\_Lvl1\_PP}$] - 20 * Log [$Voltage_{T\_Lvl0\_PP}$ / $Voltage_{N\_Lvl0\_PP}$] for Voltage Swing Levels 0, 1 and 2.

- Level 2 vs. Level 1

Resultant = 20 * Log [$Voltage_{T\_Lvl2\_PP}$ / $Voltage_{N\_Lvl2\_PP}$] - 20 * Log [$Voltage_{T\_Lvl1\_PP}$ / $Voltage_{N\_Lvl1\_PP}$] for Voltage Swing Levels 0 and 1.

- Level 3 vs. Level 2

Resultant = 20 * Log [$Voltage_{T\_Lvl3\_PP}$ / $Voltage_{N\_Lvl3\_PP}$] - 20 * Log [$Voltage_{T\_Lvl2\_PP}$ / $Voltage_{N\_Lvl2\_PP}$] for Voltage Swing Level 0, if supported.

Table 264 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX-PREEMP-OFF}$	Maximum Pre-emphasis when disabled	-	-	0.25	dB	Pre-emphasis Level 0 setting must not show any pre-emphasis at TP2 to prevent link training issues.
$V_{TX-PREEMP-DELTA}$	Delta of Pre-emphasis Level 1 vs. Level 0	2	-	-	dB	Applies to all valid voltage settings. Measured at Pre-emphasis Post Cursor2 Level 0. Support for Pre-emphasis Level 3 is optional.
	Delta of Pre-emphasis Level 2 vs. Level 1	1.6	-	-	dB	
	Delta of Pre-emphasis Level 3 vs. Level 2	1.6	-	-	dB	

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured pre-emphasis level or pre-emphasis delta for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Transition Voltage Range Measurement Test

Test ID

For RBR and HBR:

- 1272001 – Non Transition Voltage Range Measurement (Swing 0)
- 1273001 – Non Transition Voltage Range Measurement (Swing 1)
- 1274001 – Non Transition Voltage Range Measurement (Swing 2)

For HBR2 and HBR25:

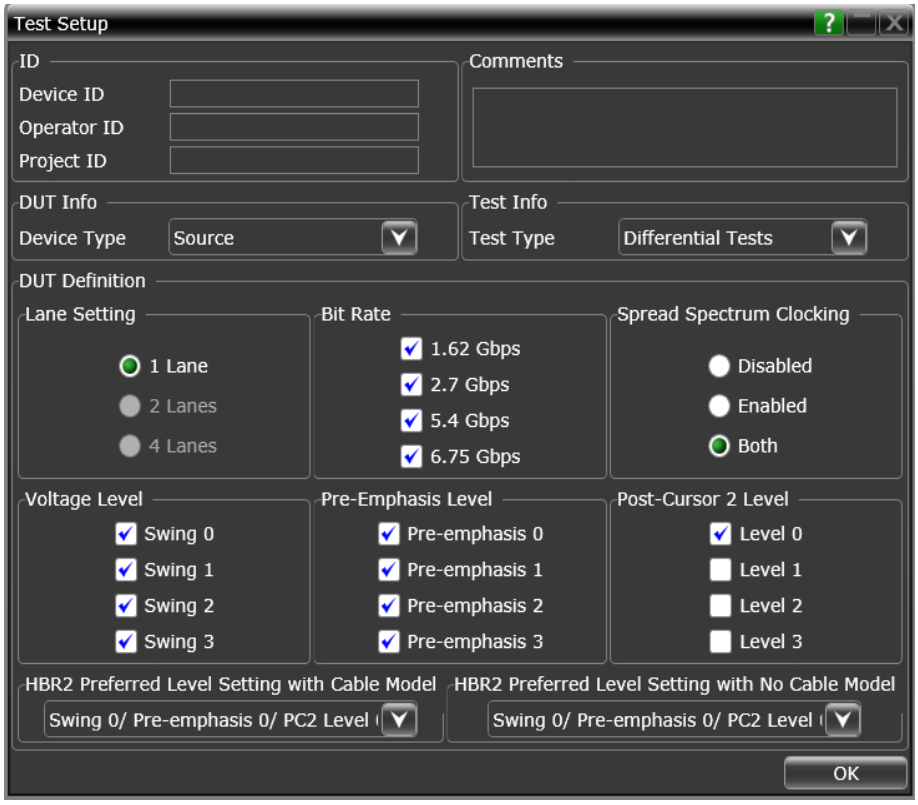
- 1272101 – Non Transition Voltage Range Measurement (Swing 0)
- 1273101 – Non Transition Voltage Range Measurement (Swing 1)
- 1274101 – Non Transition Voltage Range Measurement (Swing 2)

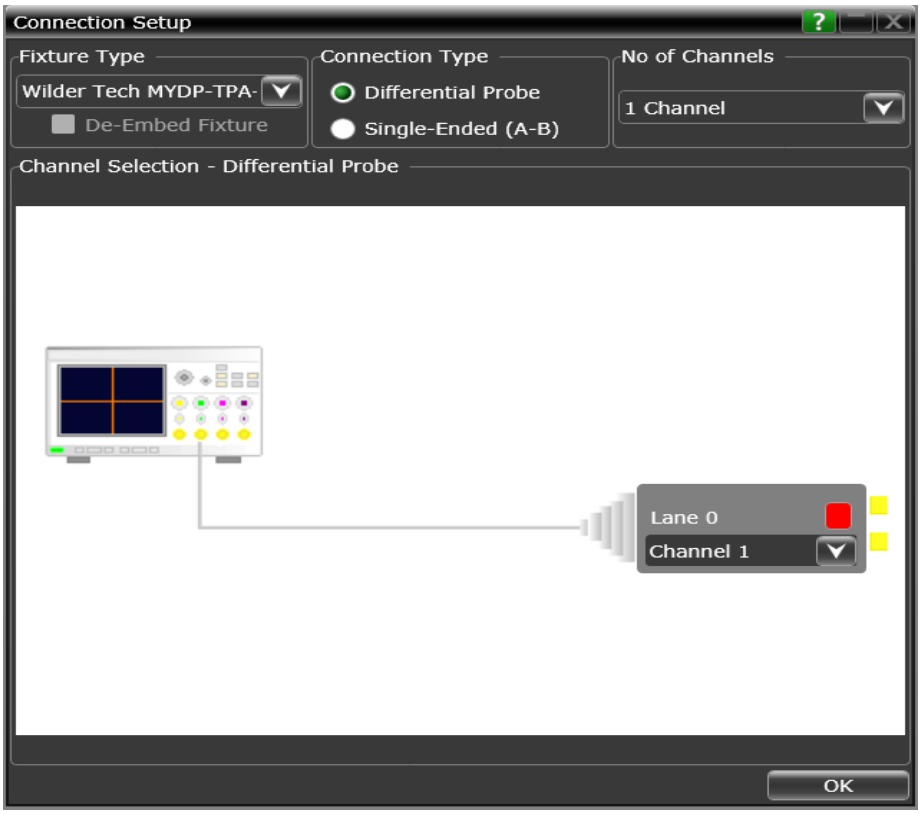
Test Overview

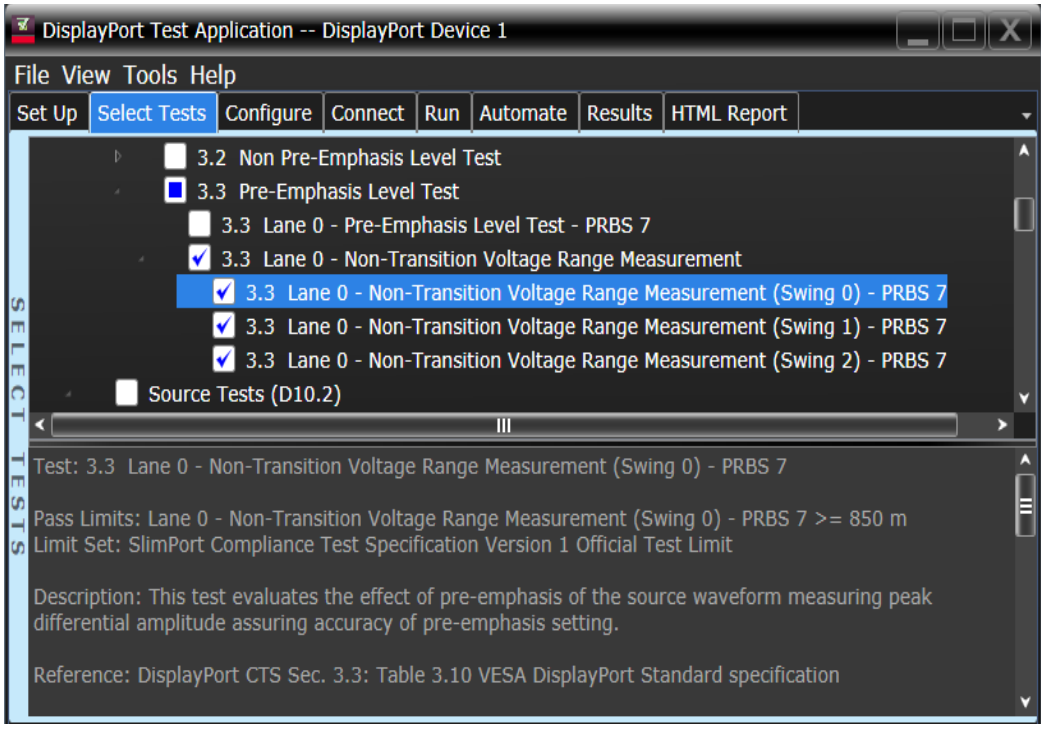
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings. Comparisons are also made for the Level 0 transition state as well as non-transition levels.

Test Conditions for Non Transition Voltage Range Measurement Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR25)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels are supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR25– PLTPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given Voltage Level, repeat the following steps for all pre-emphasis levels subjected to constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.

- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6th bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4th bit of the four successive transmitted zeros of the pattern.

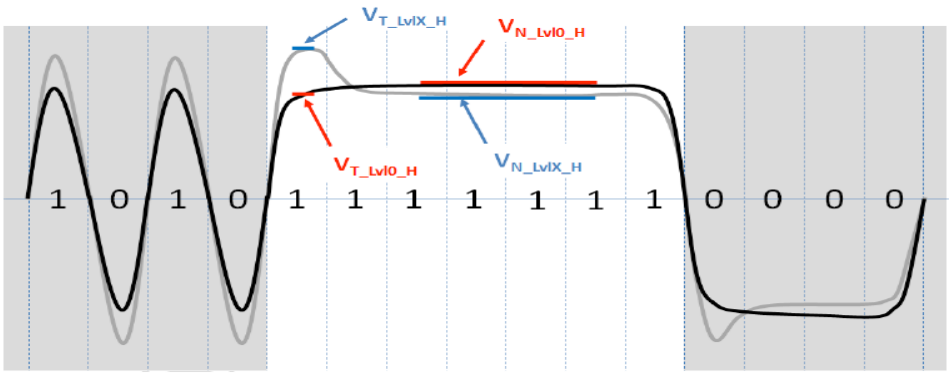


Figure 248 High Voltage measurement for RBR and HBR

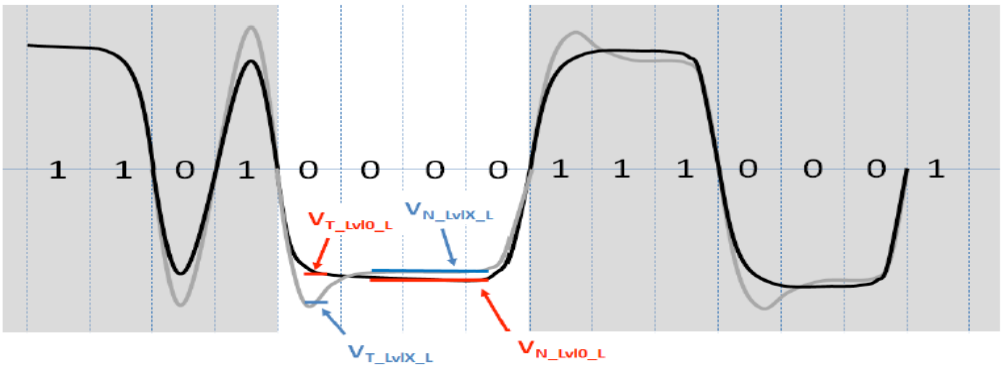


Figure 249 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR25 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

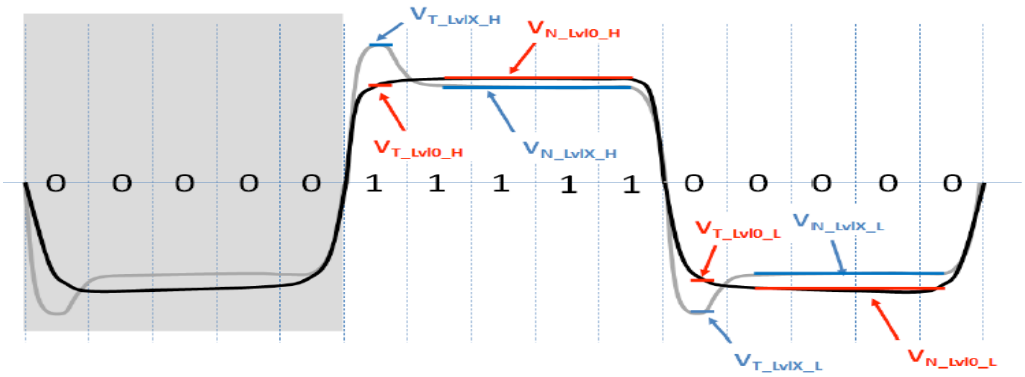


Figure 250 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

2 Calculate the non transition voltage range using the equation:

$$\text{Non Transition Voltage Range} = \text{Minimum } [(V_{N\_LvlX\_PP}) / (V_{N\_Lvl0\_PP})]$$

where, $V_{N\_LvlX\_PP}$) refers to all supported pre-emphasis levels (Level1, Level2, Level3 and so on up to Level X).

3 Report the measurement results.

PASS Condition

Non-Transition Voltage Range Measurements

For Level 2 voltage setting: Resultant $\geq$ 0.708 OR 20*log(Resultant) > -3dB

For Level 1 voltage setting: Resultant $\geq$ 0.708 OR 20*log(Resultant) > -3dB

For Level 0 voltage setting: Resultant $\geq$ 0.85 OR 20*log(Resultant) > -1.4dB

Table 265 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX-DIFF\_REDUCTION}$	Non-transition reduction Output Voltage Level 2	-	-	3	dB	$V_{TX-DIFF}$ at each non-zero nominal pre-emphasis level must not be lower than the specified amount less than $V_{TX-DIFF}$ at the zero nominal pre-emphasis level.
	Non-transition reduction Output Voltage Level 1	-	-	3	dB	
	Non-transition reduction Output Voltage Level 0	-	-	1.4	dB	

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured output voltage level reduction of the non transition bit for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Peak to Peak Voltage Test

Test ID

For RBR and HBR:

- 1266001 – Peak to Peak Voltage Test

For HBR2 and HBR25:

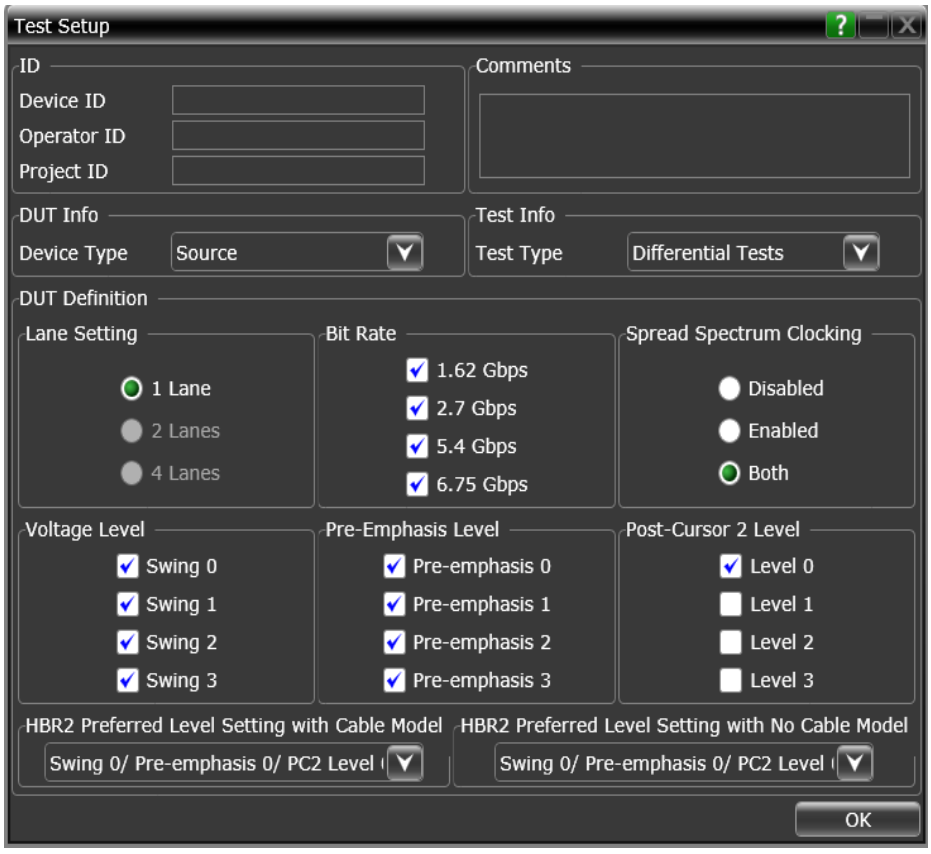
- 1266101 – Peak to Peak Voltage Test

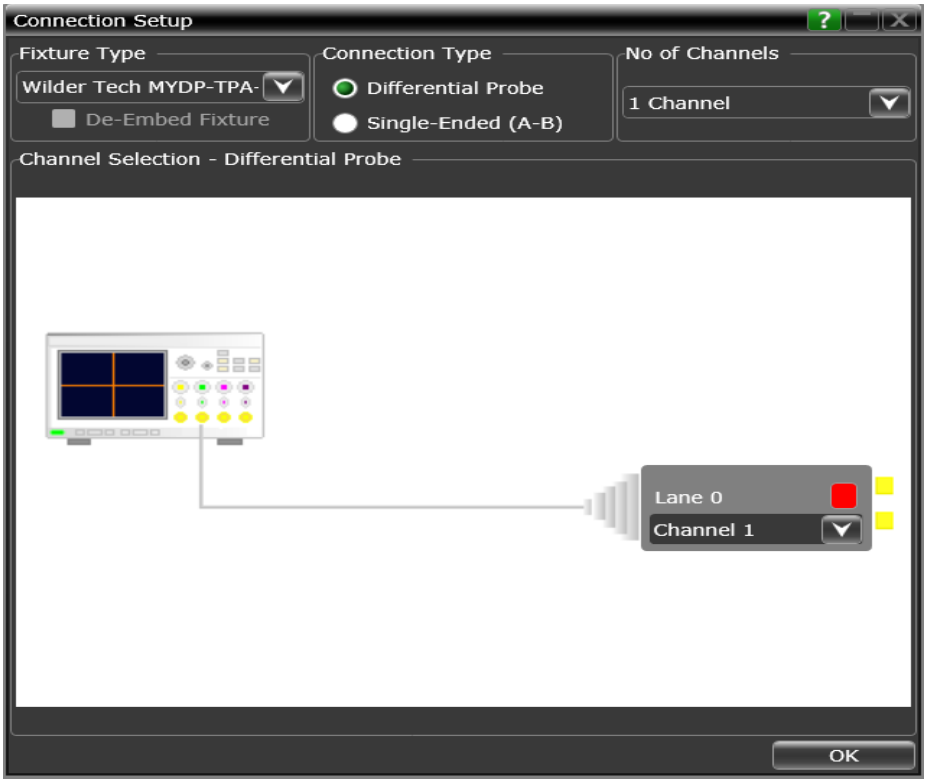
Test Overview

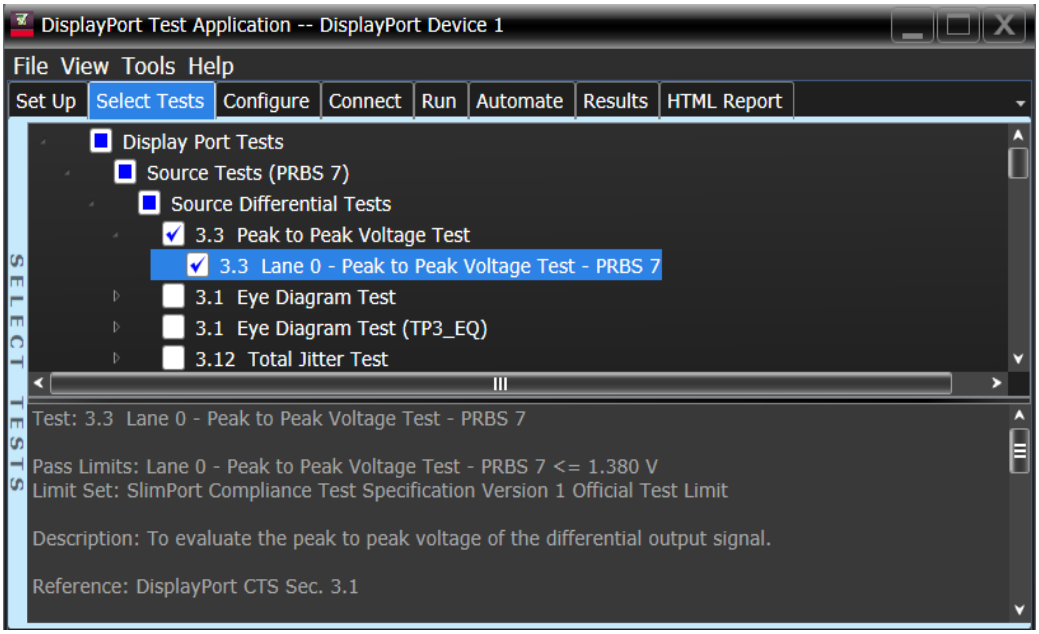
The objective of this test is to evaluate the maximum differential peak to peak voltage.

Test Conditions for Peak to Peak Voltage Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR25)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels are supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR25– PLTPAT




Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK


DisplayPort Test Application -- DisplayPort Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
Display Port Tests
Source Tests (PRBS 7)
Source Differential Tests
3.3 Peak to Peak Voltage Test
3.3 Lane 0 - Peak to Peak Voltage Test - PRBS 7
3.1 Eye Diagram Test
3.1 Eye Diagram Test (TP3_EQ)
3.12 Total Jitter Test
SELECT TESTS
Test: 3.3 Lane 0 - Peak to Peak Voltage Test - PRBS 7
Pass Limits: Lane 0 - Peak to Peak Voltage Test - PRBS 7 <= 1.380 V
Limit Set: SlimPort Compliance Test Specification Version 1 Official Test Limit
Description: To evaluate the peak to peak voltage of the differential output signal.
Reference: DisplayPort CTS Sec. 3.1

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{MAX} and V_{MIN} of the input signal.
   d Measure the data rate of the input signal.
3 Measure the maximum and minimum voltage of the input signal.
4 Calculate the peak to peak voltage using the equation:

$$\text{Peak to Peak Voltage} = V_{MAX} - V_{MIN}$$

5 Report the measurement results.

PASS Condition

For all Data Rates:

Maximum Differential Peak to Peak Voltage $\leq$ 1.38V.

Table 266 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX\text{-}DIFFp\text{-}p\_MAX}$	Max Output Voltage Level	-	-	1.38	V	For all Output Level and Pre-emphasis combinations.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured peak to peak voltage for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Main Link Frequency Compliance Test

Test ID

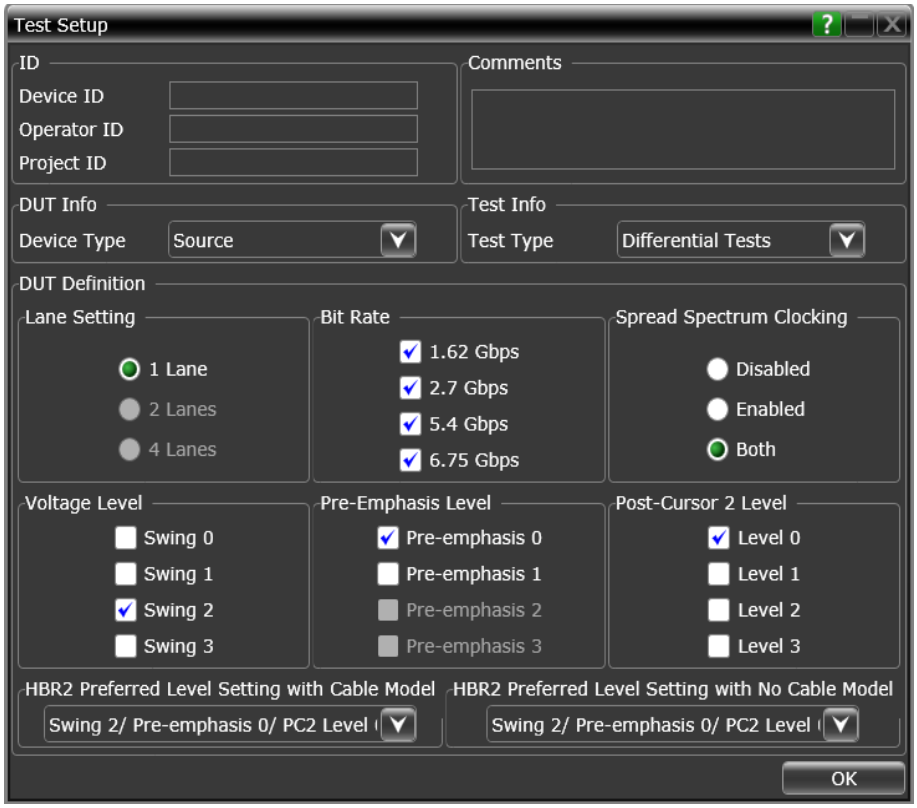
12193001 – Main Link Frequency Compliance

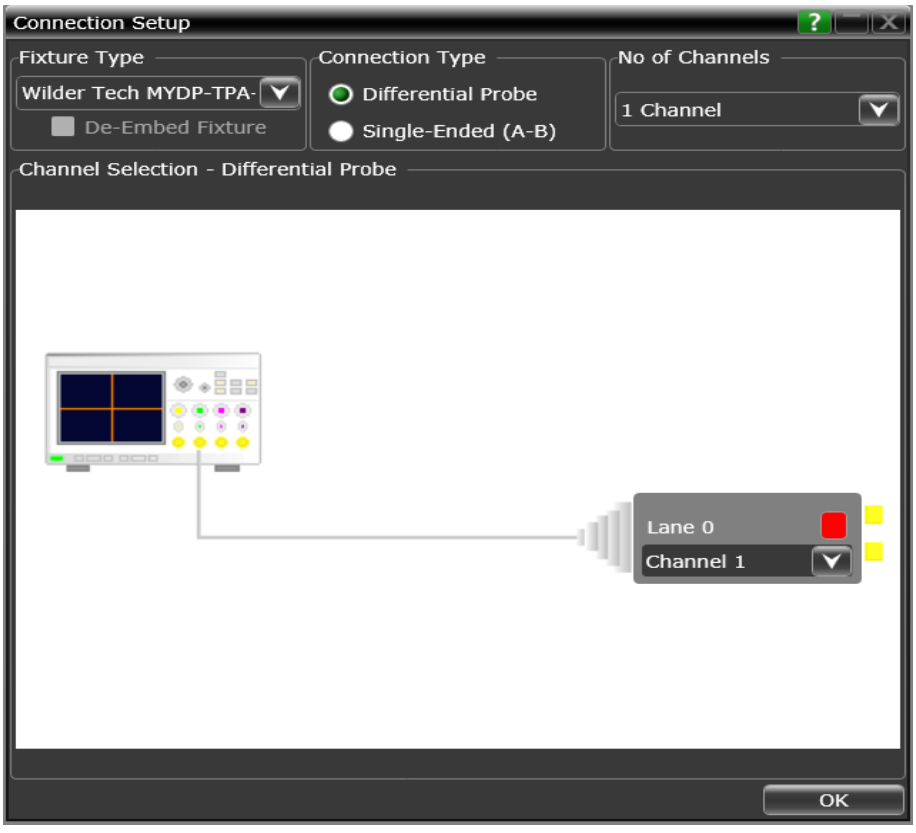
Test Overview

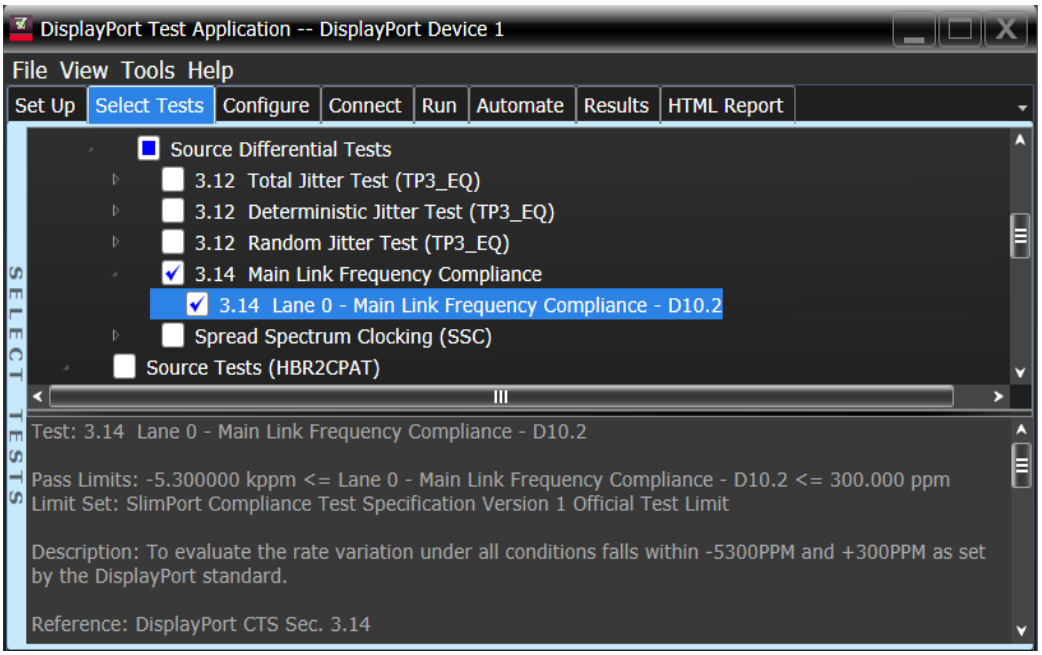
The objective of this test is to ensure that the average data rate under all conditions does not exceed the minimum and maximum values as set by the VESA DisplayPort 1.2a Standard.

Test Conditions for Main Link Frequency Compliance Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR25)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.

5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and the minimum measurement levels for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurement levels for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e For SSC Enabled Test condition, check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.
9 For the test condition “SSC Enabled”, set up the parameter of the SSC measurement:
   a Set up the memory depth and time-base to display one complete SSC cycle based on the measured SSC modulation frequency in Step 5.
   b Acquire the signal with one complete SSC cycle.
   c Get the minimum of FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

      Maximum Data Rate = 1 / (Minimum Unit Interval)

   d Get the maximum of FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

      Minimum Data Rate = 1 / (Maximum Unit Interval)

   e Repeat steps b, c and d until you acquire 10 SSC Cycles.
   f Calculate the mean value for the maximum and minimum data rates.
10 Report the measurement results.

PASS Condition

Maximum Data Rate (Frequency Max_{ppm}) $\leq$ 300 ppm

Minimum Data Rate (Frequency Min_{ppm}) $\geq$ -5300 ppm

Table 267 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
f_{HBR2}	Frequency for High Bit Rate 2	5.37138	5.4	5.40162	Gbps	Frequency high limit = +300ppm Frequency low limit = -5300ppm
f_{HBR}	Frequency for High Bit Rate	2.68569	2.7	2.70081	Gbps	
f_{RBR}	Frequency for Reduced Bit Rate	1.611414	1.62	1.620486	Gbps	

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.14*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured data rate for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Frequency Test

Test ID

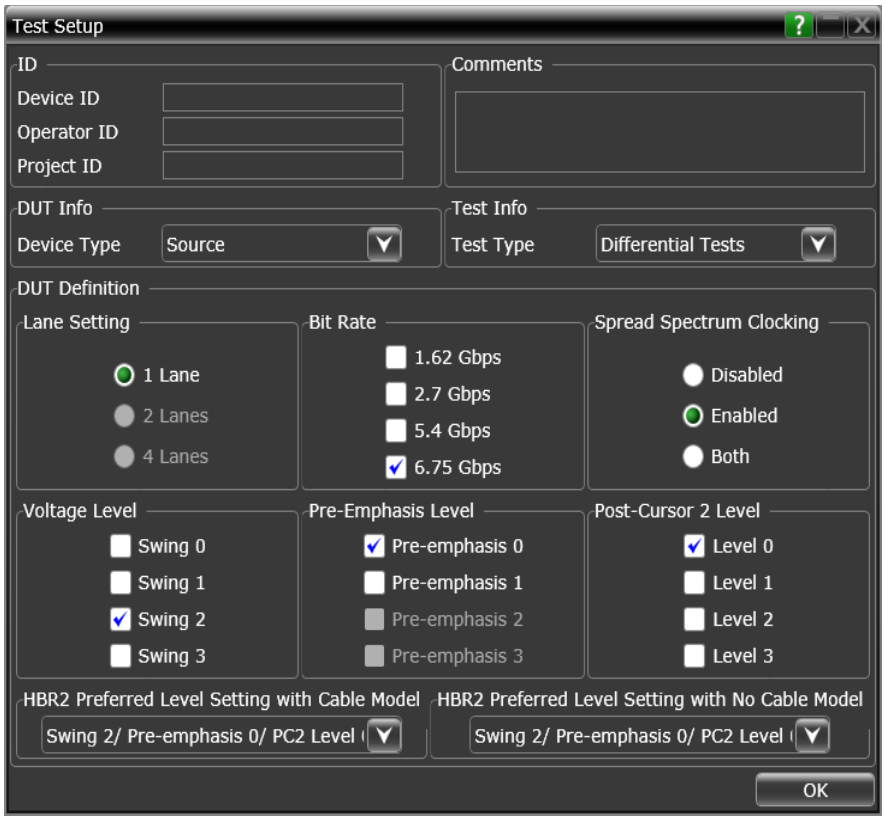
12170001 – SSC Modulation Frequency Test

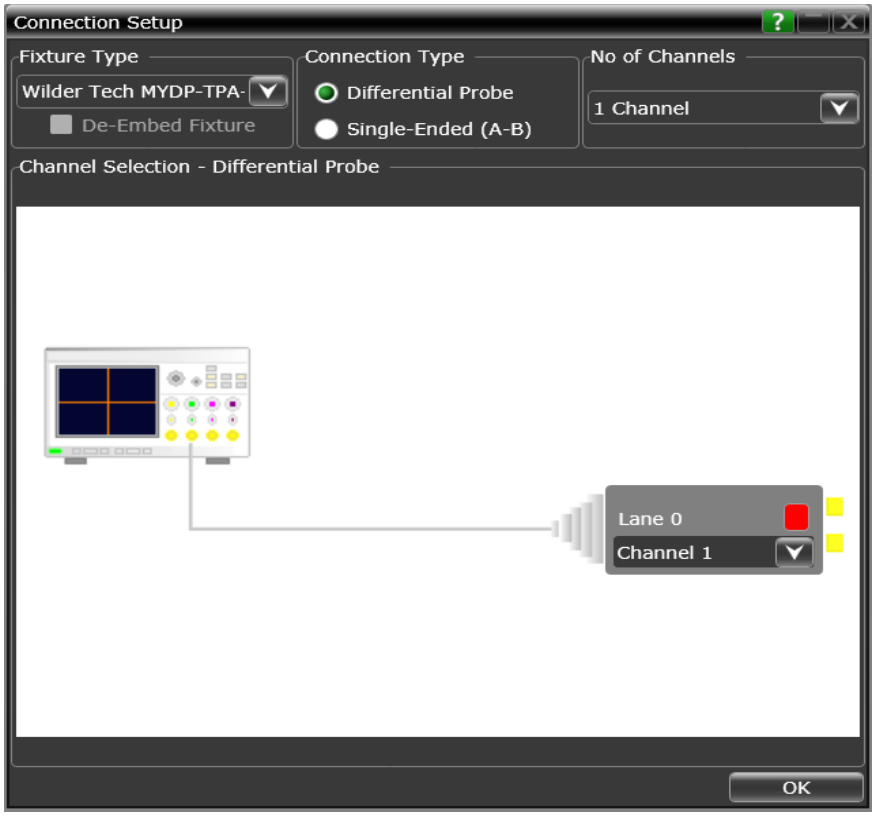
Test Overview

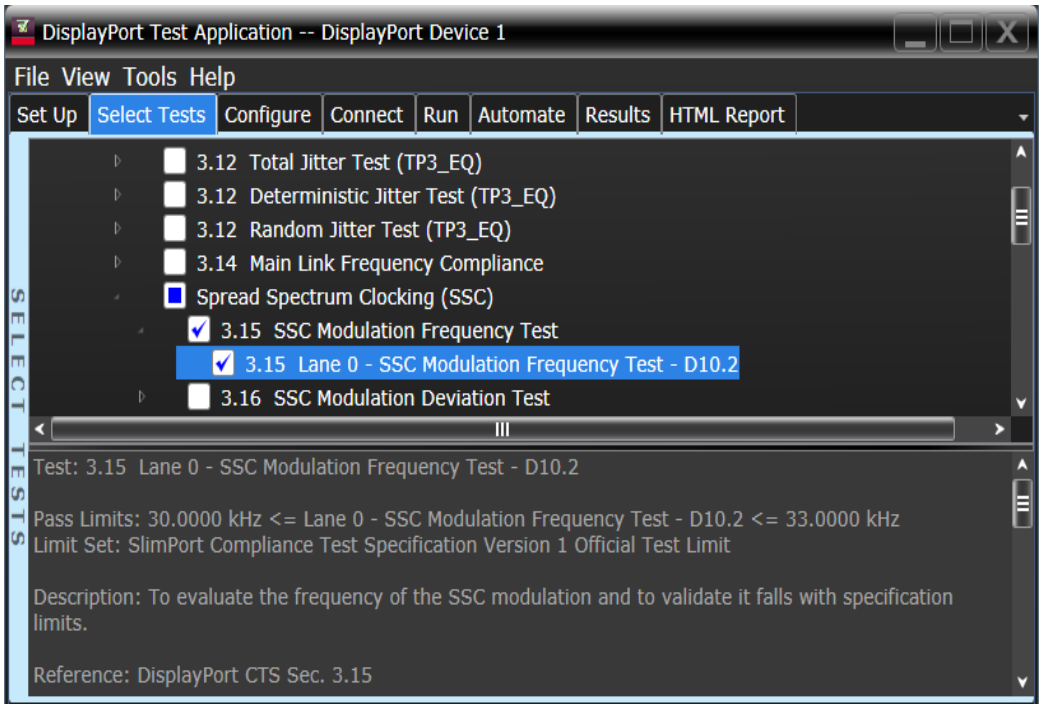
The objective of this test is to evaluate the frequency of the SSC modulation and to validate that the frequency is within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. Calculate the SSC modulation frequency from the average of the measured SSC modulation frequency for each cycle.

Test Conditions for SSC Modulation Frequency Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR25)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.

5 Set up the parameters for the frequency measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.
   g Acquire the signal for 10 SSC Cycles.
6 Get the mean value for the SSC Modulation frequency.
7 Report the measurement results.

PASS Condition

30kHz $\leq$ SSC Modulation Frequency (f_{SSC}) $\leq$ 33kHz

Table 268 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
Down_Spread_Frequency	Link clock down-spreading frequency	30	-	33	kHz	Range: 30kHz ~ 33kHz when down-spread enabled

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.15*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured SSC modulation frequency for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Deviation Test

Test ID

12180001 – SSC Modulation Deviation Test

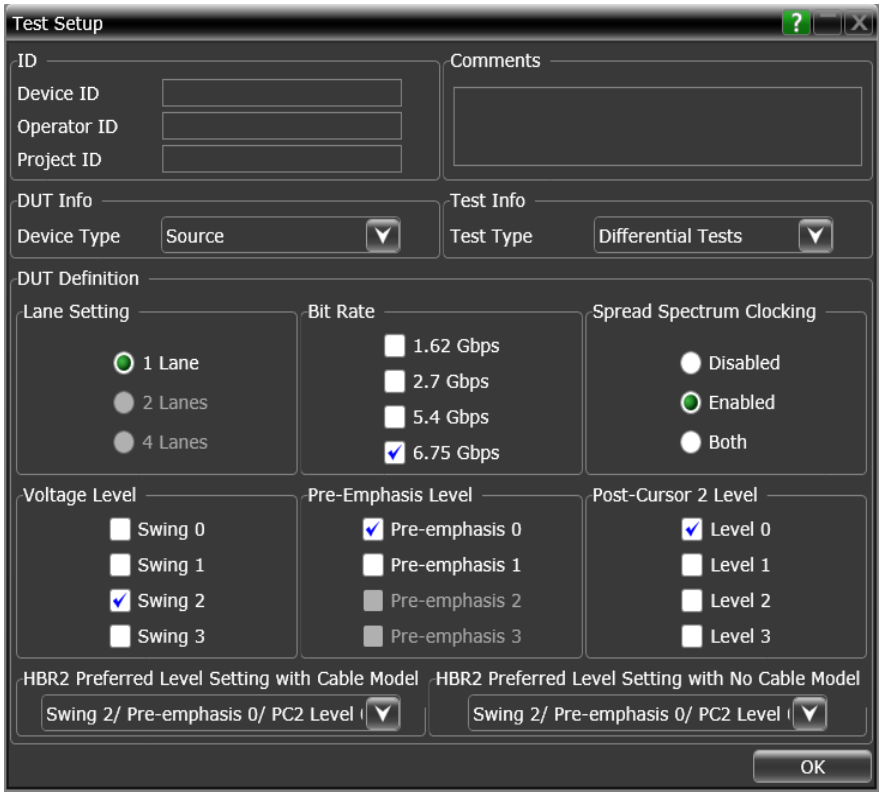
Test Overview

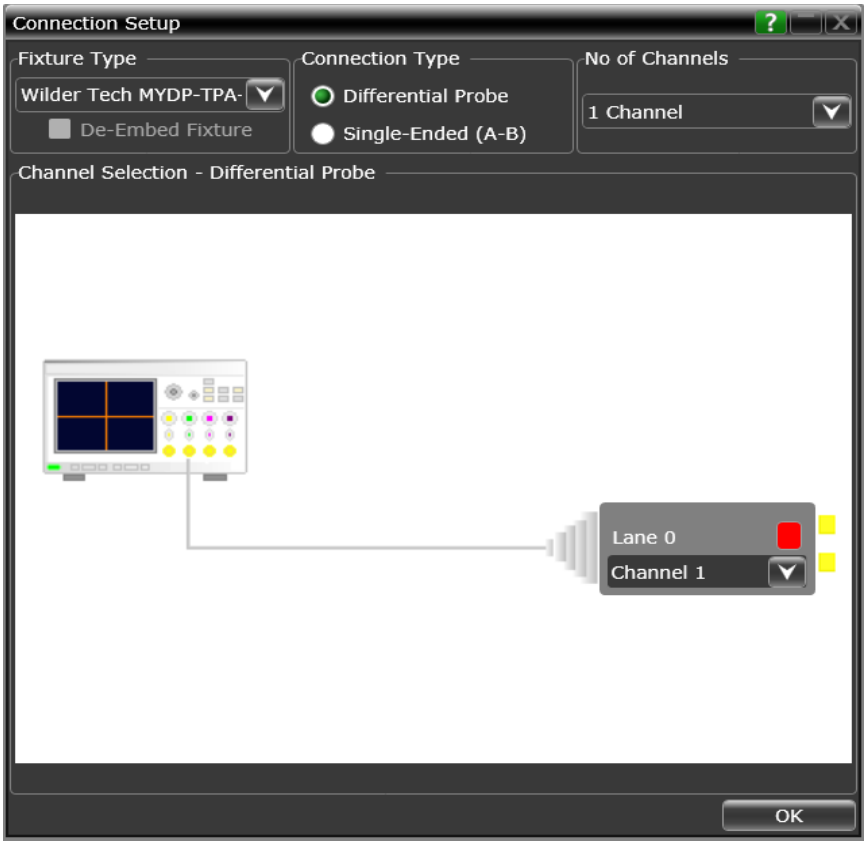
The objective of this test is to evaluate the range of SSC down-spreading of the transmitter signal in ppm and to validate that the values are within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. For each cycle, the minimum and maximum data rate is evaluated. Calculate the SSC modulation deviation from the average of the maximum minus the average of the minimum using the equation:

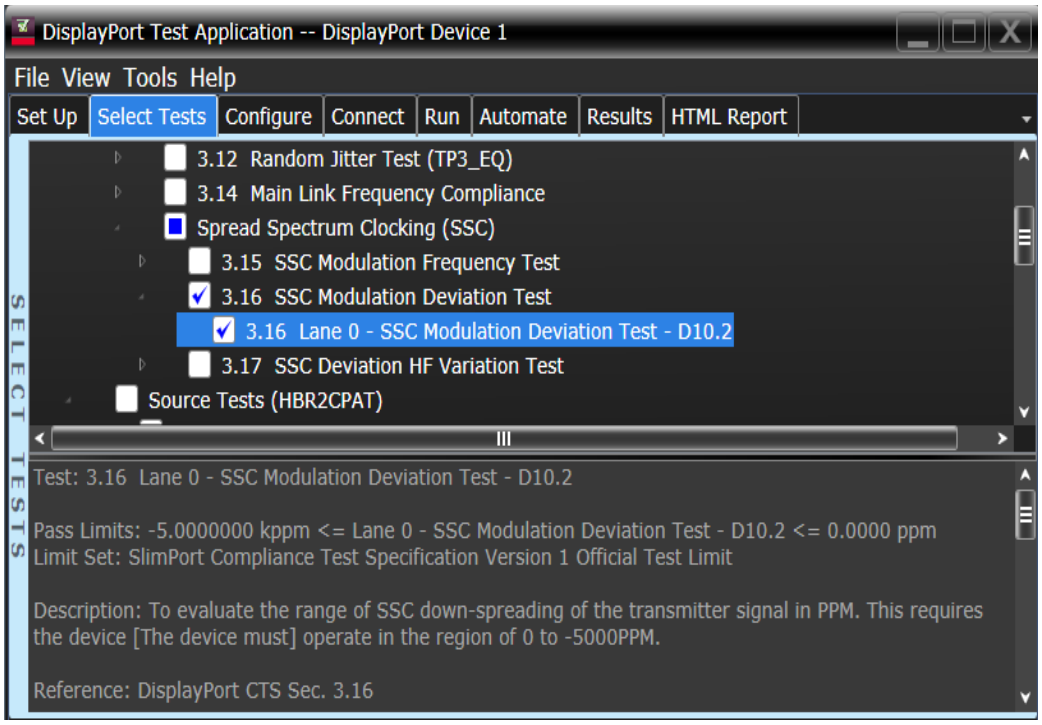
SSC Modulation Deviation = {[Average (Minimum Data Rate) - Average (Maximum Data Rate)] / Nominal Data Rate}*1E+6

Test Conditions for SSC Modulation Deviation Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR25)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.

5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and minimum measurements for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurements for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e Check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point for three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 filtered unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurements for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.
9 Set up the parameters for SSC measurement.
   a Set up memory depth and time-base to display one complete SSC Cycle based on the measured SSC modulation frequency in step 5.
   b Acquire the signal with one complete SSC Cycle.
   c Get the minimum of the FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

      Maximum Data Rate = 1/Minimum Unit Interval

   d Get the maximum of the FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

      Minimum Data Rate = 1/Maximum Unit Interval

   e Repeat step b,c and d until you acquire 10 SSC Cycles.
   f Calculate the mean value for the maximum and minimum data rate.
10 Calculate the SSC Modulation Deviation using the equation:

   SSC Modulation Deviation = {[Average (Minimum Data Rate) - Average (Maximum Data Rate)] / Nominal Data Rate}*1E+6

11 Report the measurement results.

PASS Condition

-5000ppm $\leq$ SSC Modulation Deviation (Resultant$_{SSC\ Range}$) $\leq$ 0ppm

Table 269 DisplayPort Main Link Transmitter System Parameters

Symbol	Parameter	Min	Nom	Max	Unit	Comments
Down_Spread_Amplitude	Link clock down-spreading	0	-	0.5	%	Range: 0% ~ 0.5% when down-spread enabled

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.16*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured SSC modulation deviation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Deviation HF Variation Test (Informative)

Test ID

12200001 – SSC Deviation HF Variation Test (Informative)

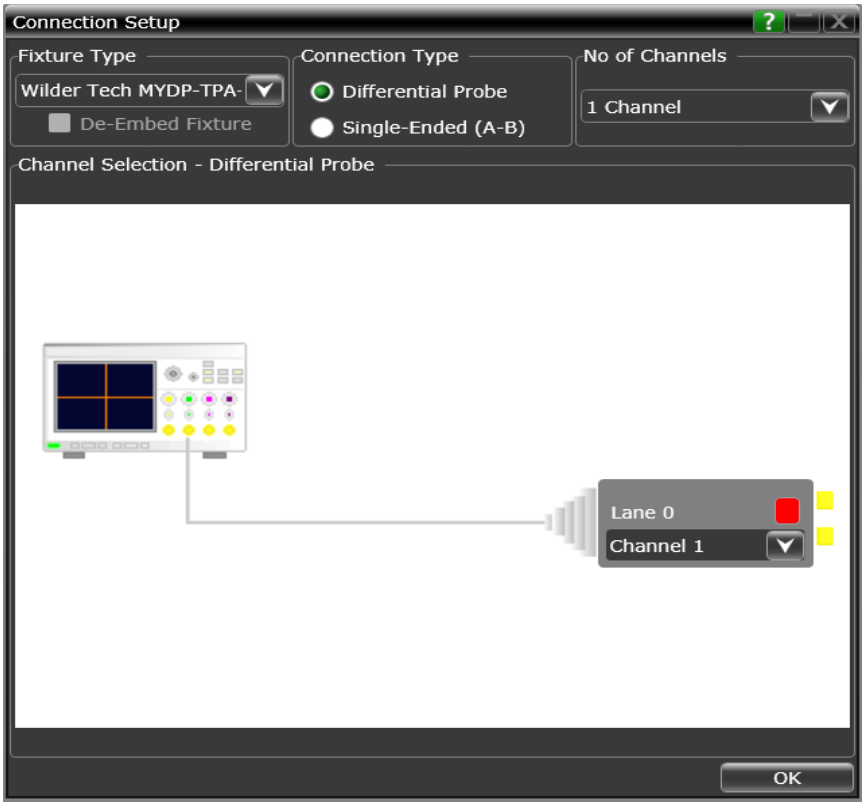
Test Overview

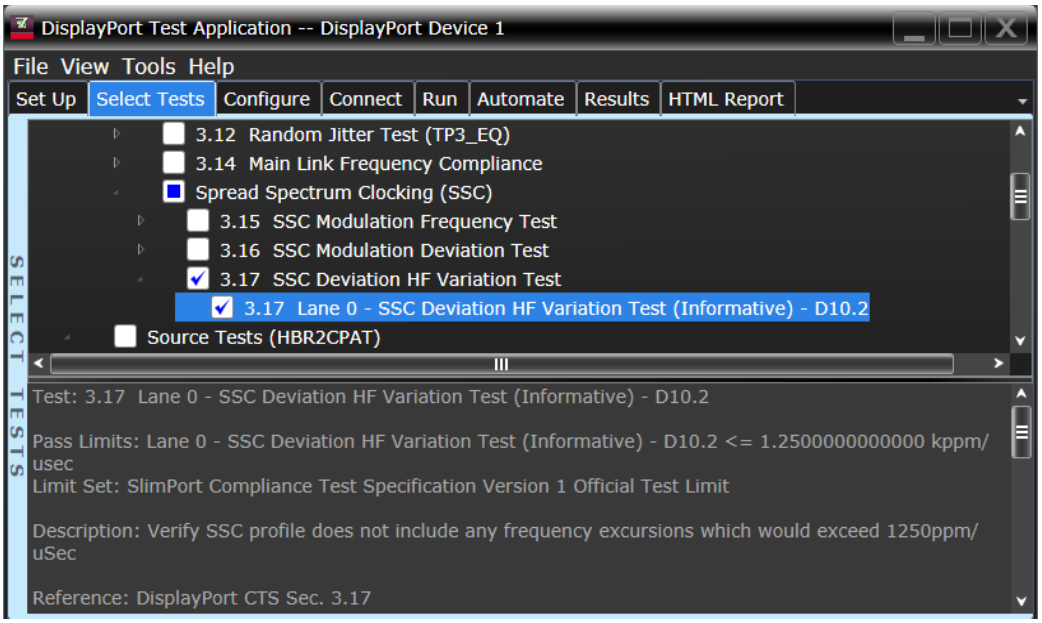
The objective of this test is to verify that the SSC profile does not include any frequency deviation that may exceed 1250 ppm/µsec. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles.

Test Conditions for SSC Deviation HF Variation Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR25)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.

5 Set up the parameters for the frequency measurement.

a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.

b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.

c Set up the memory depth and time-base using the settings defined in the Configuration Variable.

d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.

e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).

f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.

6 Set up the parameters for the SSC measurement.

a Set up memory depth and time-base to display one complete SSC cycle using the measured SSC Modulation Frequency in Step 5.

b Acquire the signal with one complete SSC Cycles.

c Read the FUNC2 filtered unit interval measurement trend.

d Compute the slope using the “Sliding Window” with 1.00 µsec window width. Calculate the slope using the equation:

$$\text{Slope} = [f(t) - f(t-1.00\ \mu\text{sec})/1.00\ \mu\text{sec}]$$

e Repeat step b, c and d until you acquire 10 SSC Cycles.

f Get the maximum value for the computed value of slope.

7 Report the measurement results.

PASS Condition

SSC_t dF/dt $\leq$ 1250ppm/µsec

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.17*

Expected/Observable Results

The measured SSC deviation high frequency variation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Post-Cursor 2 Verification Test (Informative)

Test ID

1279001 — Post Cursor 2 Verification Test - Level 1/Level 0 (Informative)

1279101 — Post Cursor 2 Verification Test - Level 2/Level 1 (Informative)

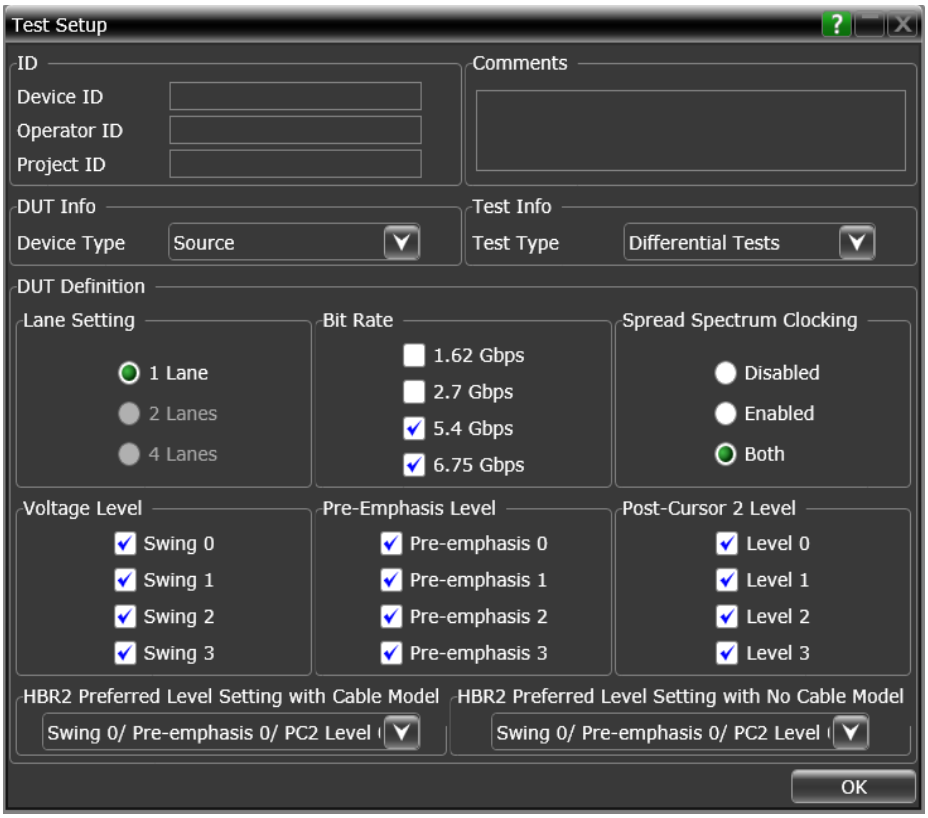
1279201 — Post Cursor 2 Verification Test - Level 3/Level 2 (Informative)

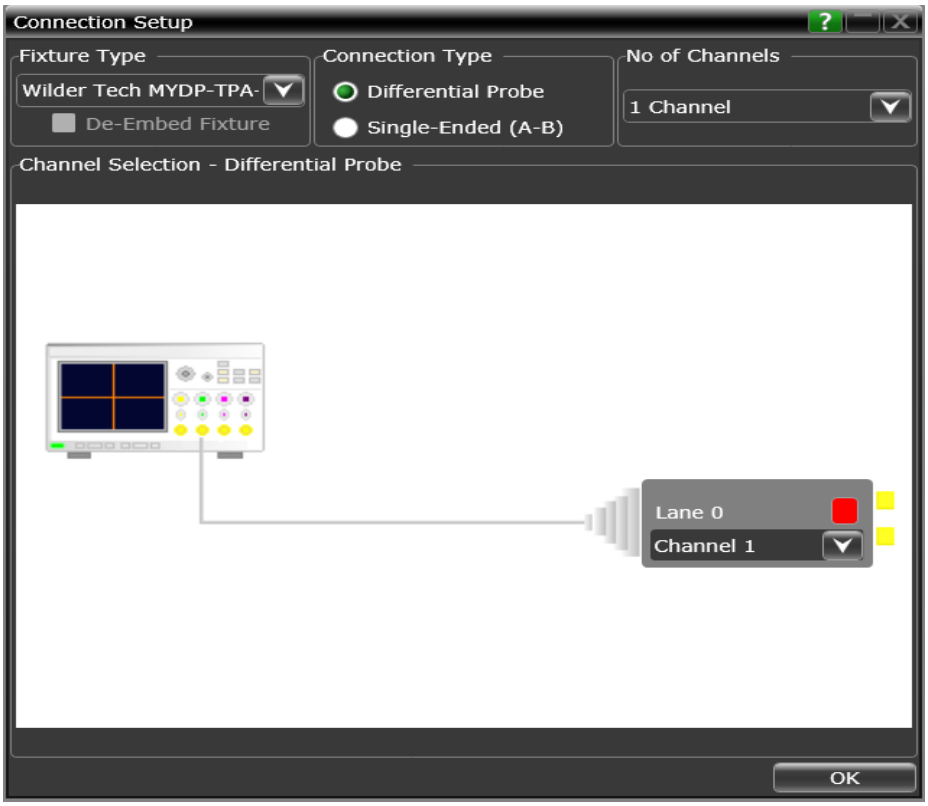
Test Overview

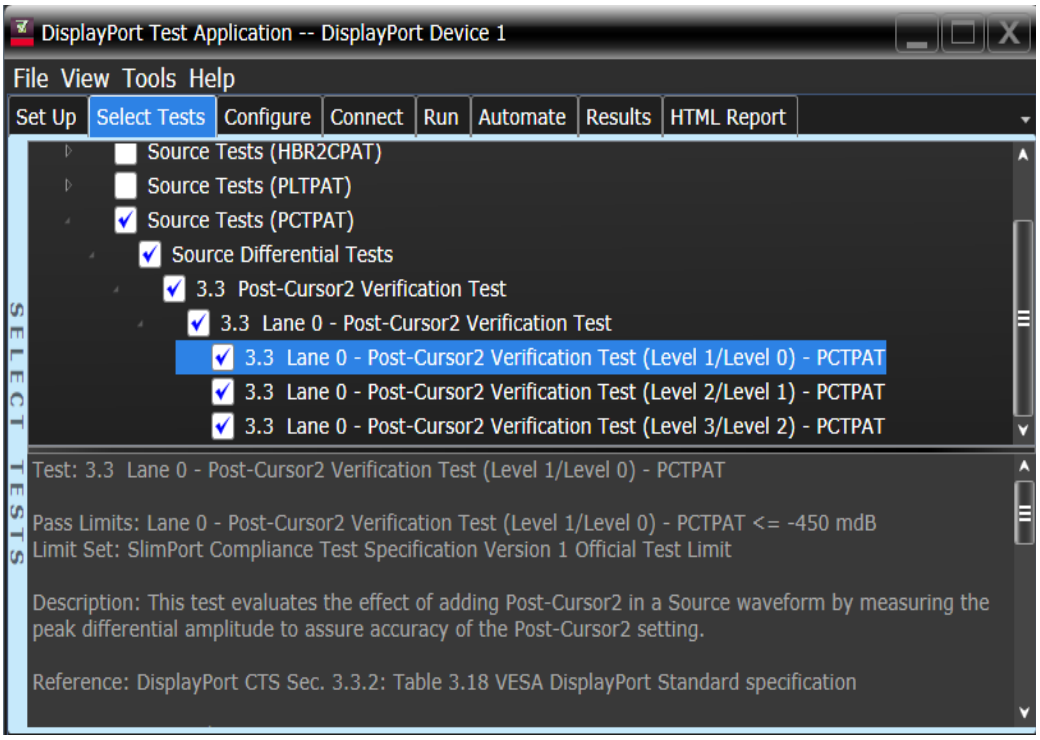
The objective of this test is to evaluate the effect of adding Post-Cursor 2 of the source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor 2 settings.

Test Conditions for Post-Cursor 2 Verification Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	HBR2, HBR25
SSC	Both SSC conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels supported subject to constraints in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	All Post-Cursor 2 levels supported
Test Lane	Lane 0
Test Pattern	PCTPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 For a given Voltage Level, Pre-Emphasis Level and Post-Cursor 2 Level X:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d Pattern fold the input signal based on the qualifying pattern 00101010 for the measurement of voltage $V_{T1010\_PC2\_LvlX\_PP}$ in the test pattern PLTPAT.

e Set up the vertical waveform histogram on the input signal at the points specified below to measure the High voltage $V_{T1010\_PC2\_LvlX\_H}$ and Low Voltage $V_{T1010\_PC2\_LvlX\_L}$.

i $V_{T1010\_PC2\_LvlX\_H}$ is the average value over the 40% to 70% UI points in the fifth relevant bit (1s bit) in the 1010 portion of the qualifying pattern.

ii $V_{T1010\_PC2\_LvlX\_L}$ is the average value over the 40% to 70% UI points in the sixth relevant bit (0s bit) in the 1010 portion of the qualifying pattern.

f Calculate the peak-to-peak voltage $V_{T1010\_PC2\_LvlX\_PP}$ using the equation:

$$V_{T1010\_PC2\_LvlX\_PP} = V_{T1010\_PC2\_LvlX\_H} - V_{T1010\_PC2\_LvlX\_L}$$

g Pattern fold the input signal based on the qualifying pattern 00011001100 for the measurement of voltage $V_{T1100\_PC2\_LvlX\_PP}$ in the test pattern PLTPAT.

h Set up the vertical waveform histogram on the input signal at the points specified below to measure the High voltage $V_{T1100\_PC2\_LvlX\_H}$ and Low Voltage $V_{T1100\_PC2\_LvlX\_L}$.

i $V_{T1100\_PC2\_LvlX\_H}$ is the average value over the 40% to 70% UI points in the fifth relevant bit (1s bit) in the 1100 portion of the qualifying pattern.

ii $V_{T1100\_PC2\_LvlX\_L}$ is the average value over the 40% to 70% UI points in the sixth relevant bit (0s bit) in the 1100 portion of the qualifying pattern.

i Calculate the peak-to-peak voltage $V_{T1100\_PC2\_LvlX\_PP}$ using the equation:

$$V_{T1100\_PC2\_LvlX\_PP} = V_{T1100\_PC2\_LvlX\_H} - V_{T1100\_PC2\_LvlX\_L}$$

j Calculate the Post-Cursor 2 ratio using the equation:

$$\text{Post-Cursor 2 Ratio}_{LvlX} = V_{T1100\_PC2\_LvlX\_PP} / V_{T1010\_PC2\_LvlX\_PP}$$

2 Compare the pre-emphasis delta of Post-Cursor 2 Level with the limits by repeating Step 1 with another Post-Cursor2 Level.

3 Calculate the pre-emphasis delta of Post-Cursor 2 Level using the equation:

$$\text{Post-Cursor 2 Delta (Level 1 vs Level 0)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl1} / \text{Post-Cursor 2 Ratio}_{Lvl0}]$$

$$\text{Post-Cursor 2 Delta (Level 2 vs Level 1)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl2} / \text{Post-Cursor 2 Ratio}_{Lvl1}]$$

$$\text{Post-Cursor 2 Delta (Level 3 vs Level 2)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl3} / \text{Post-Cursor 2 Ratio}_{Lvl2}]$$

4 Report the measurement results.

PASS Condition

Post Cursor2 Verification Measurements:

For Level 1 vs. Level 0 Pre-emphasis Post Cursor 2 settings: $\text{Resultant}_{Lvl0\_to\_Lvl1} < -0.45$ dB

For Level 2 vs. Level 1 Pre-emphasis Post Cursor 2 settings: $\text{Resultant}_{Lvl1\_to\_Lvl2} < -0.5$ dB

For Level 3 vs. Level 2 Pre-emphasis Post Cursor 2 settings: $\text{Resultant}_{Lvl2\_to\_Lvl3} < -0.6$ dB

Table 270 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX\text{-}PREEMP\_POST2\text{-}DELTA}$	Delta of Pre-emphasis Post Cursor2 Level 1 vs. Level 0	-0.45	-	-	dB	Measured on 2nd TBIT at Pre-emphasis Level 0
	Delta of Pre-emphasis Post Cursor2 Level 2 vs. Level 1	-0.5	-	-	dB	Support for Pre-emphasis Post Cursor2 is optional
	Delta of Pre-emphasis Post Cursor2 Level 3 vs. Level 2	-0.6	-	-	dB	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2a, Section 3.3.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured pre-emphasis delta of Post-Cursor 2 for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Eye Diagram Test (TP3_EQ)

Test ID

For HBR

- 1211001 – Eye Diagram Test (TP3_EQ)
- 1211011 – Eye Diagram Test with No Cable Model (TP3_EQ)

For HBR2 and HBR25

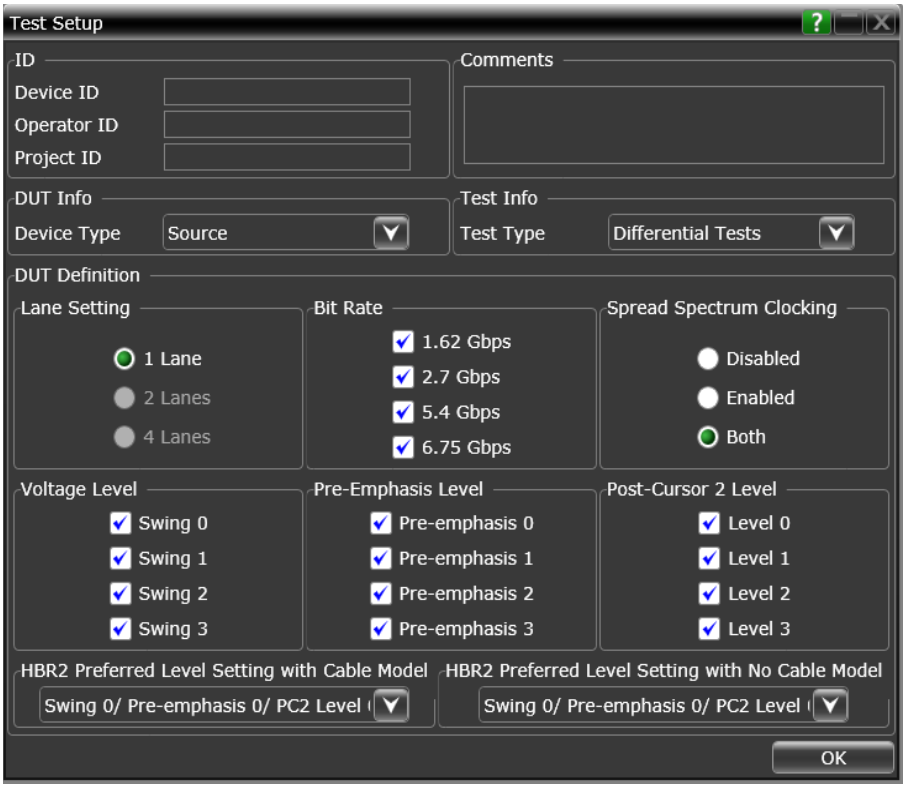
- 1215001 – Eye Diagram Test (TP3_EQ)
- 1215011 – Eye Diagram Test with No Cable Model (TP3_EQ)

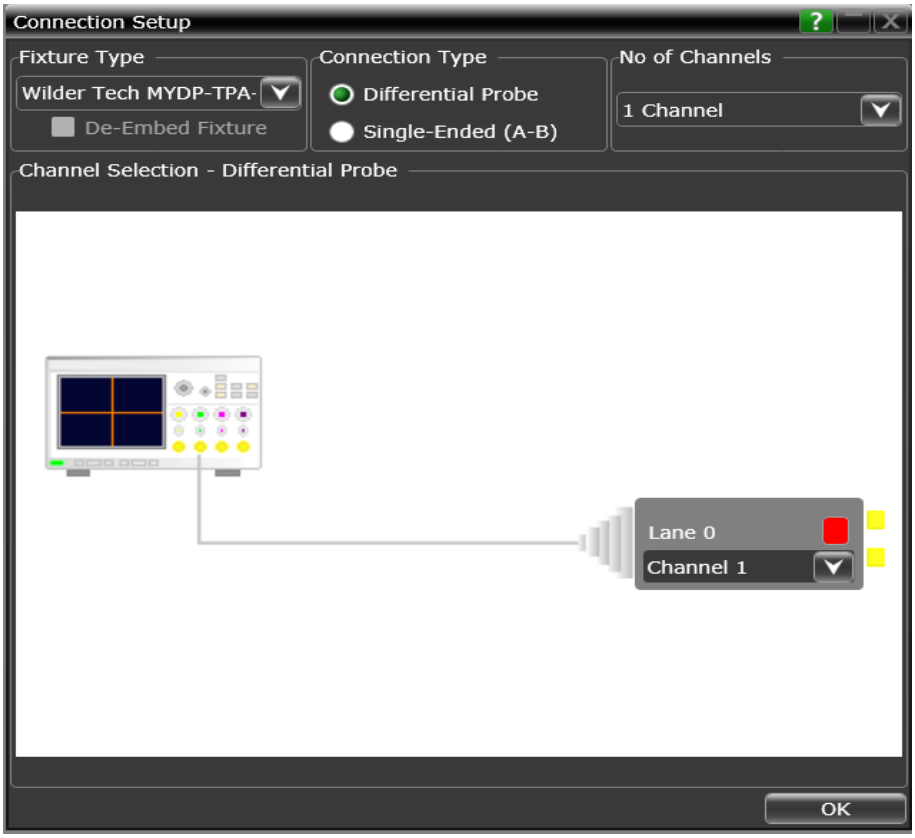
Test Overview

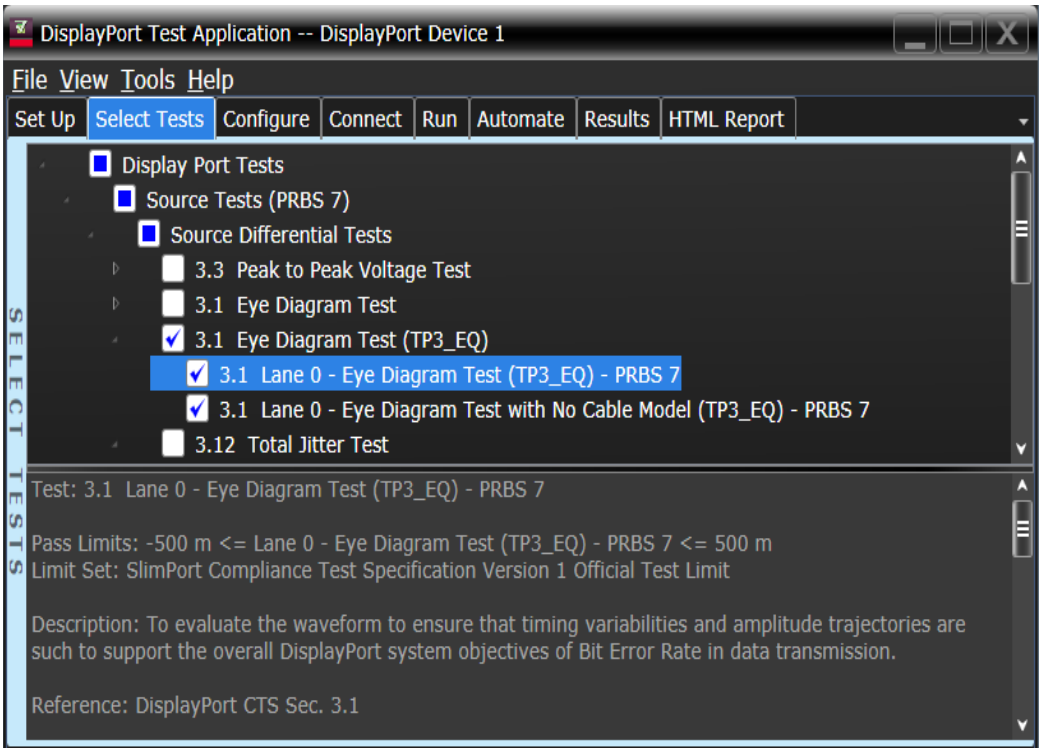
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions for Eye Diagram Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR (Informative), HBR2 and HBR25
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	HBR – Level 2 HBR2, HBR25 – Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	HBR – Level 0 HBR2, HBR25 – Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	HBR – Level 0 HBR2, HBR25 – Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	Lane 0
Test Pattern	HBR–PRBS7 HBR2, HBR25–HBR2CPAT
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure for HBR and HBR25

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.

7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the jitter of the eye diagram using the Histogram.
9 Check for any signal trajectories that may have entered into the mask.
10 Report the measurement results.

Measurement Procedure for HBR2

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]:
   a Pattern fold the equalized signal based on the High Level Voltage (V_{HIGH}) random noise configuration variable.
   b Set up the vertical waveform histogram on the equalized signal to measure random noise of High Level Voltage (V_{HIGH}).
   c Measure the High Level Voltage (V_{HIGH}) random noise based on the standard deviation of the waveform histogram.
   d Pattern fold the equalized signal based on the Low Level Voltage (V_{LOW}) random noise configuration variable.
   e Set up the vertical waveform histogram on the equalized signal to measure the random noise of Low Level Voltage (V_{LOW}).
   f Measure the Low Level Voltage (V_{LOW}) random noise based on the standard deviation of the waveform histogram.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge and right edge.
8 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.

9 Find the maximum eye height location of the eye diagram.

10 If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]:

a Set up the parameter of the jitter separation using the EZJIT Plus/Complete Software.

i Load the jitter separation parameter into EZJIT Plus/Complete Software based on the settings in the Configuration Variable.

ii Acquire the signal until 1,000,000 edges are analyzed.

b Note the value of the jitter component from the EZJIT Plus/Complete Software.

11 Create the eye mask based on the following criteria:

a If random noise/ jitter derate includes ["Exclude Random Noise" configuration variable set to "False" (Default)]: eye mask height and width is derate as below to comprehend the noise/jitter extrapolated to BER 10^{-9} for an Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI:

i Calculate the Eye Mask Width Derate (Random Jitter) using the equation:

$$\text{Eye Mask Width Derate (Random Jitter)} = 2.5 * \text{Random Jitter}_{rms}$$

ii Calculate the Eye Mask Height Derate (Random Noise) using the equation:

$$V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{HIGH}\ \text{Random Noise}_{rms}$$

$$V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{LOW}\ \text{Random Noise}_{rms}$$

NOTE The factor 2.5 is the delta between BER 10^{-6} (9.507) and 10^{-9} (11.996) to comprehend the noise/jitter extrapolated to BER 10-9 as the Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI.

BER	N
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996

b Place the eye mask height at the point of the maximum eye height found in Step 9.

c Calculate the Eye Mask Width:

$$\text{Eye Mask Width} = \text{Eye Width Specification (0.38 UI)} + \text{Eye Mask Width Derate (Crosstalk)} + 2 * \text{Eye Mask Width Derate (Random Jitter)}$$

d Calculate the Eye Mask Height:

$$\text{Eye Mask Height} = \{\text{Eye Height Specification (0.09 V)} + \text{Eye Mask Height Derate (Crosstalk)}\}/2 + V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)}$$

$$\text{Eye Mask Height} = -\{\text{Eye Height Specification (0.09 V)} + \text{Eye Mask Height Derate (Crosstalk)}\}/2 - V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)}$$

12 Set up the parameters for the Mask Test.

a Load the eye mask based on the settings in the Configuration Variable.

b Center the eye mask at the middle of the eye diagram.

c Run the eye mask until 1,000,000 UI are folded.

13 Measure the eye height of the eye diagram using the Histogram.

14 Measure the jitter of the eye diagram using the Histogram.
15 Calculate the eye width based on the measured jitter of the eye diagram.
16 Check for any signal trajectories that may have entered into the mask.
17 Report the measurement results.

PASS Condition

The following table and figures define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 271 shows the voltage and time coordinates for the mask used for the eye diagram.

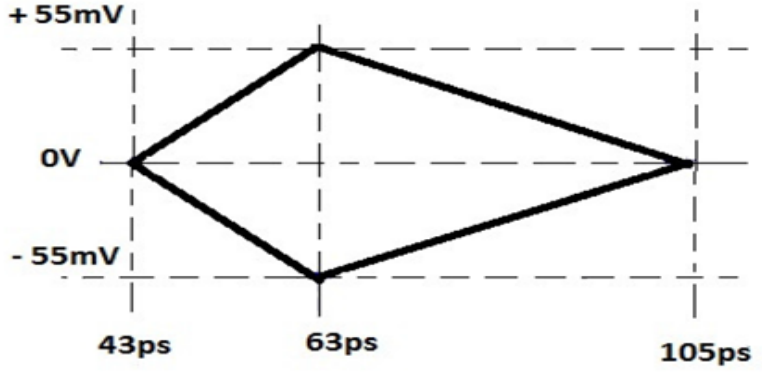


Figure 251 Eye Mask at TP3_EQ (HBR25)

Table 271 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

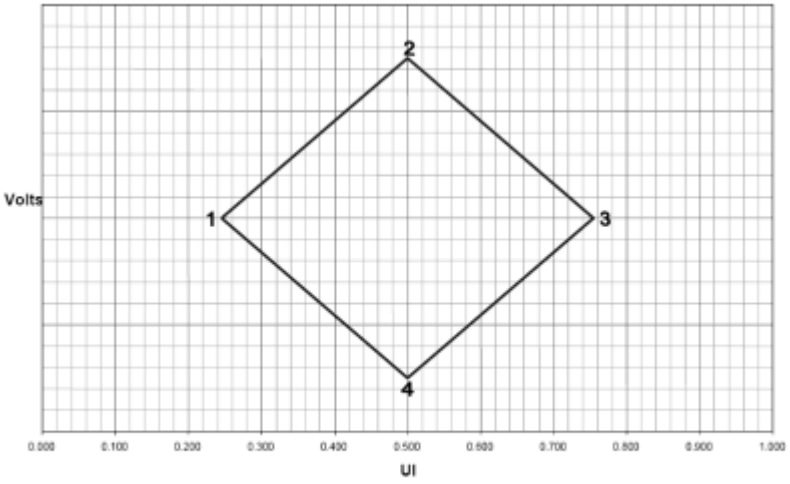


Figure 252 Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 272 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.045*
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.045*

NOTE

*Eye height limit of 45 mV and -45 mV assumes cross-talk as 0, which is only possible in case of single lane testing.

In case of multi-lane testing, cross talk exists, and the eye height values deviate by ± 7 mV. Thus the eye height becomes (+45 +7) mV and (-45 -7) mV or +52 mV and -52 mV.

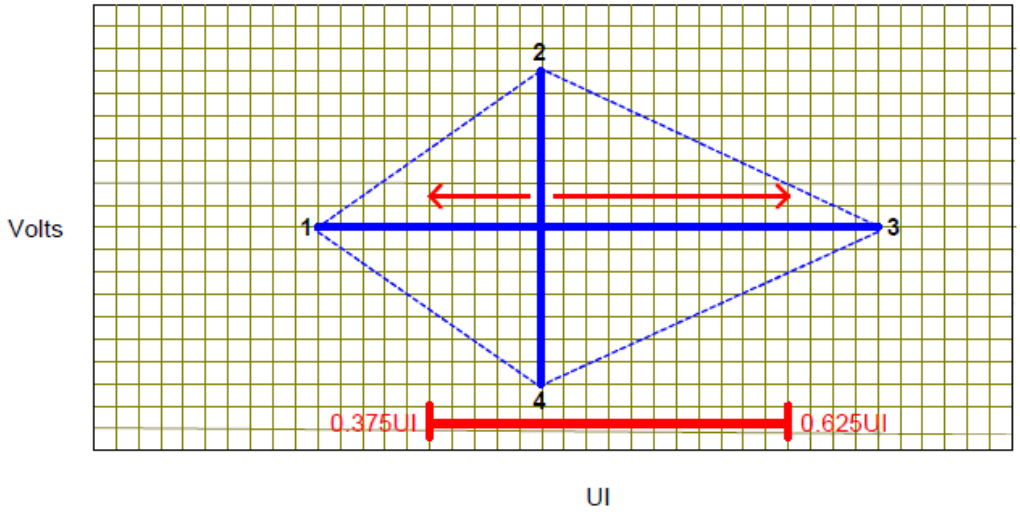


Figure 253 Eye Mask at TP3_EQ (HBR2)

Mask Test: Zero mask failures.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test (TP3_EQ)

Test ID

For HBR2 and HBR25

- 1222001 – Total Jitter Test (TP3_EQ) - HBR2CPAT
- 1222011 – Total Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1221001 – Total Jitter Test (TP3_EQ) - D10.2
- 1221011 – Total Jitter Test with No Cable Model (TP3_EQ) - D10.2

Test Overview

The objective of this test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

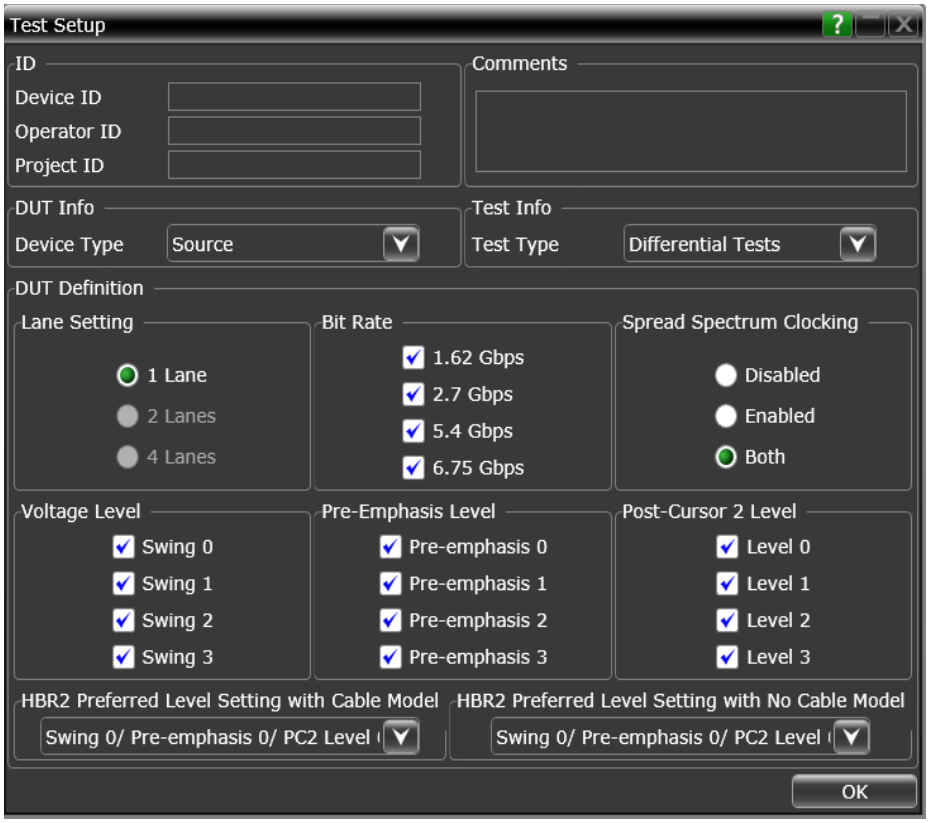
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

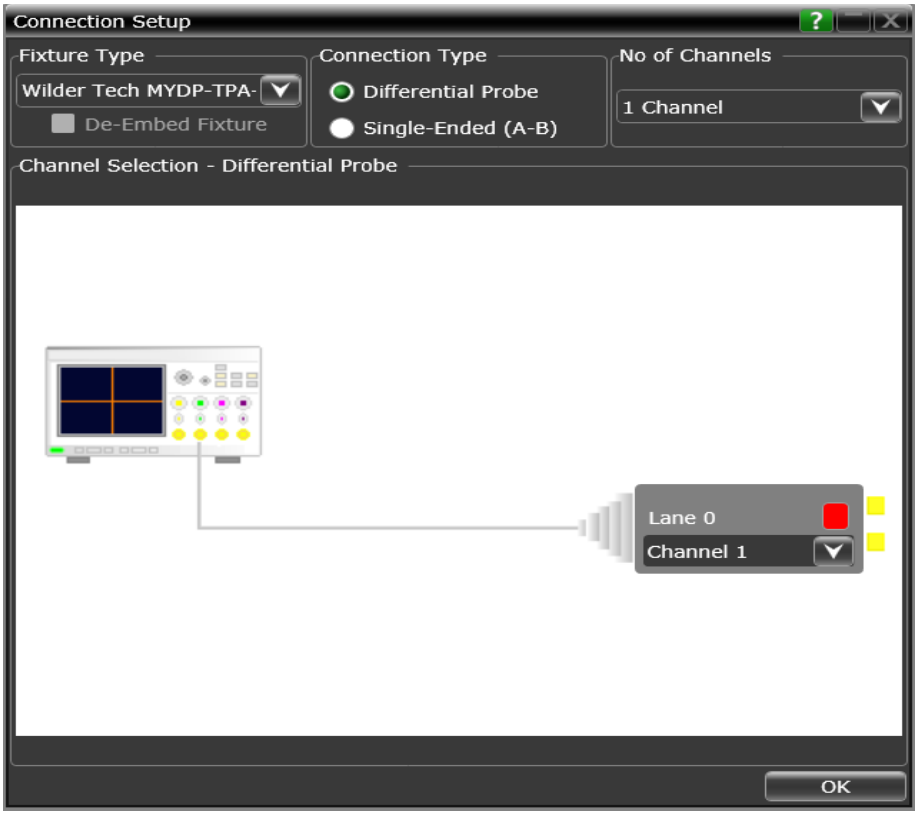
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

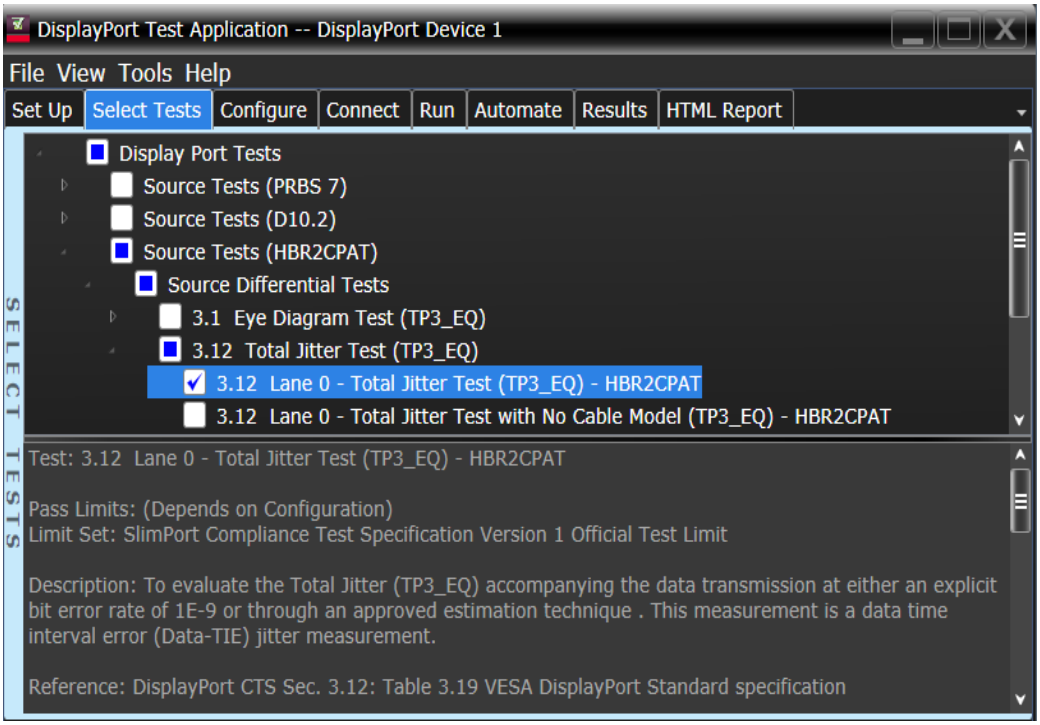
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2, HBR25
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	Lane 0
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Total Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Total Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.

7 Report the measurement results.

PASS Condition

Table 273 Total Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) and High-Bit Rate 25 (6.75 Gb/s per lane)	
A_{p-p}	0.580 UI*

* The limits for the Total Jitter are derated by 0.04 UI from 0.62 UI limit in DisplayPort 1.2a Standard.

Table 274 Total Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) and High-Bit Rate 25 (6.75 Gb/s per lane)	
$T_{TX-TJ\_D10.2\_HBR2}$	0.40 UI

UI is Unit Interval.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*

For HBR2CPAT

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

For D10.2

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18*

Expected/Observable Results

The measured total jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Deterministic Jitter Test (TP3_EQ)

Test ID

For HBR2 and HBR25

- 1236001 – Deterministic Jitter Test (TP3_EQ) - HBR2CPAT
- 1236011 – Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1235001 – Deterministic Jitter Test (TP3_EQ) - D10.2
- 1235011 – Deterministic Jitter Test with No Cable Model (TP3_EQ) - D10.2

Test Overview

The objective of this test is to evaluate the deterministic jitter accompanying the data transmission. The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

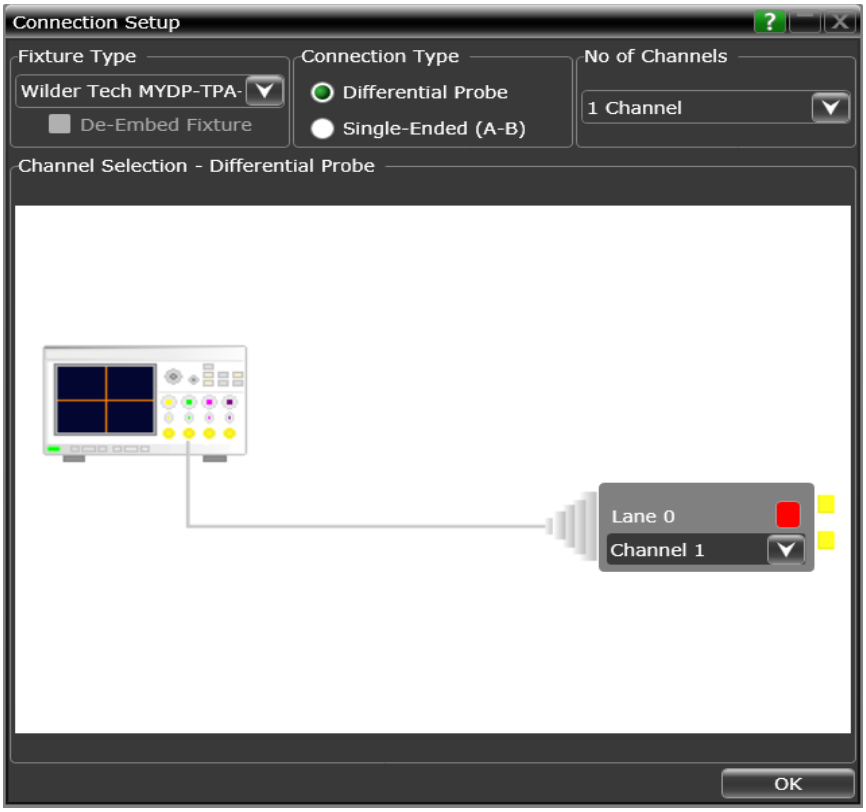
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

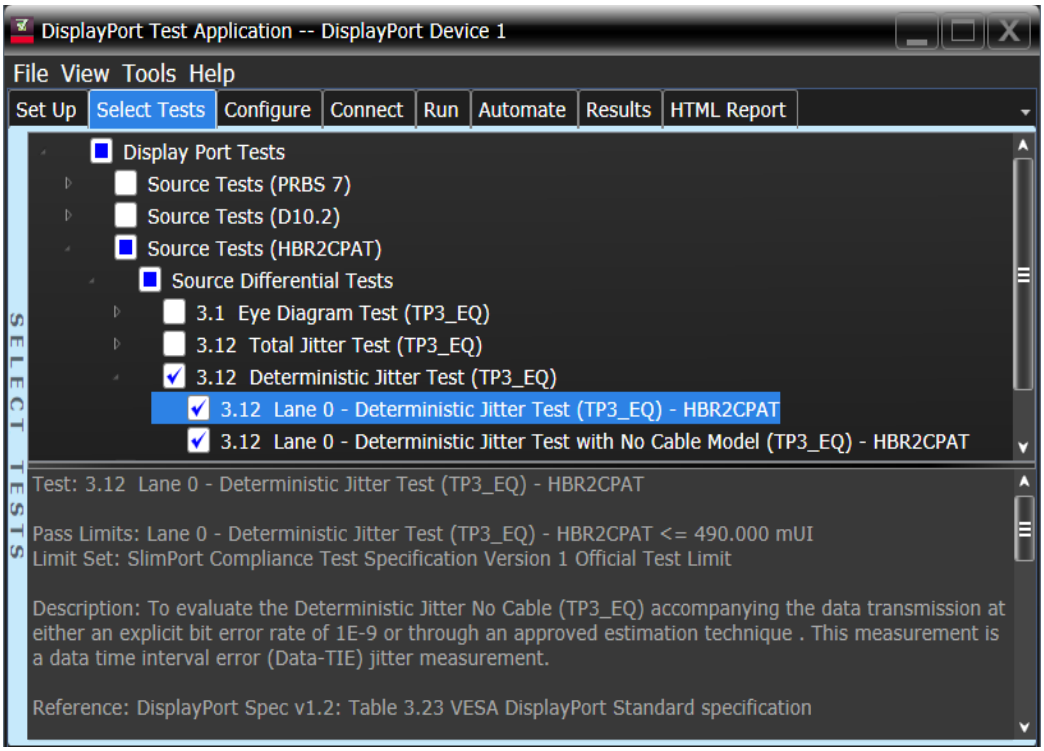
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Deterministic Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2, HBR25
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	Lane 0
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Deterministic Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Deterministic Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.

7 Report the measurement results.

PASS Condition

Table 275 Deterministic Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.49 UI

Table 276 Deterministic Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
$T_{TX-DJ\_D10.2\_HBR2}$	0.25 UI

UI is Unit Interval.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*

For HBR2CPAT

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

For D10.2

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18*

Expected/Observable Results

The measured deterministic jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Random Jitter Test (TP3_EQ)

Test ID

For HBR2 and HBR25

- 1238001 — Random Jitter Test (TP3_EQ) - D10.2
- 1238011 — Random Jitter Test with No Cable Model (TP3_EQ) - D10.2

Test Overview

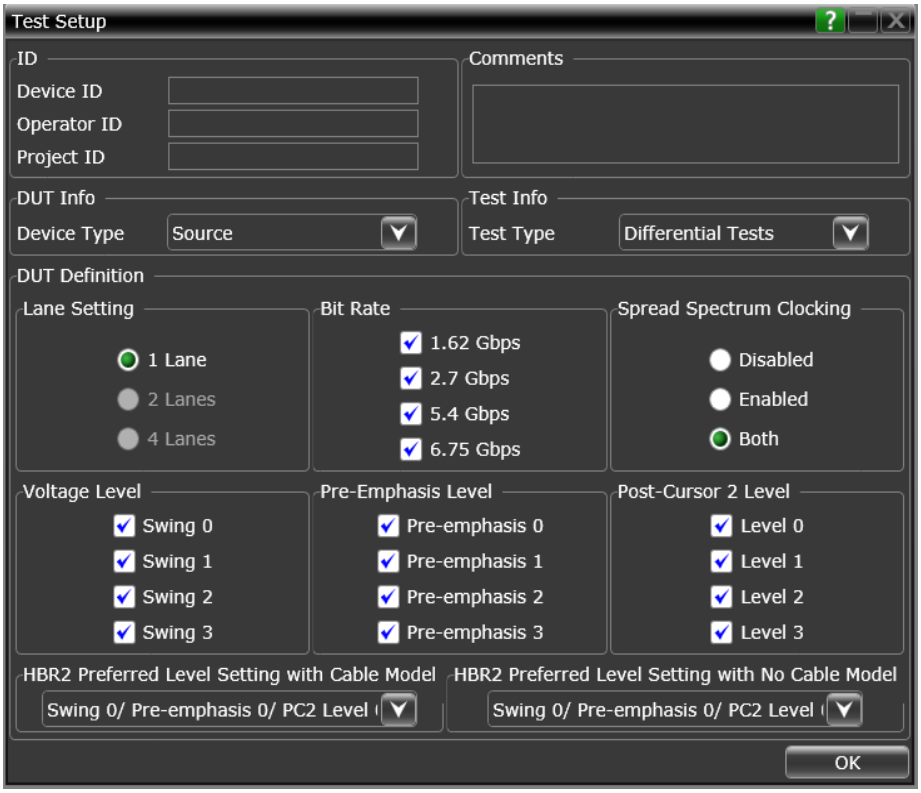
The objective of this test is to evaluate the random jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. The jitter is separated into each jitter components and the random jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

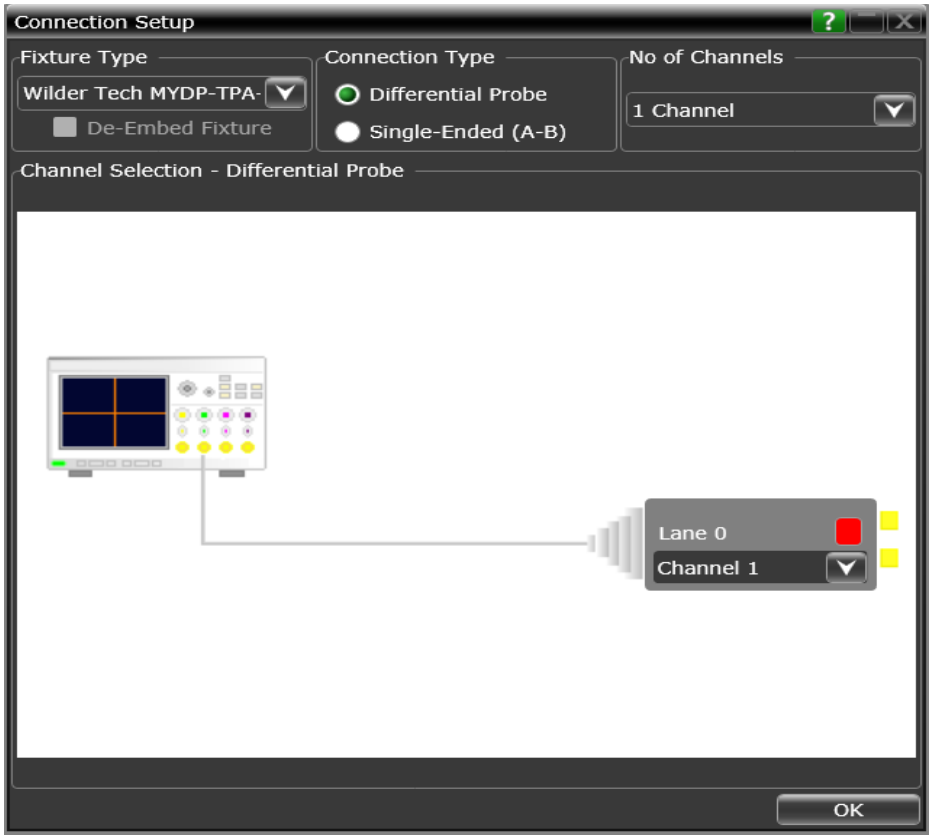
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

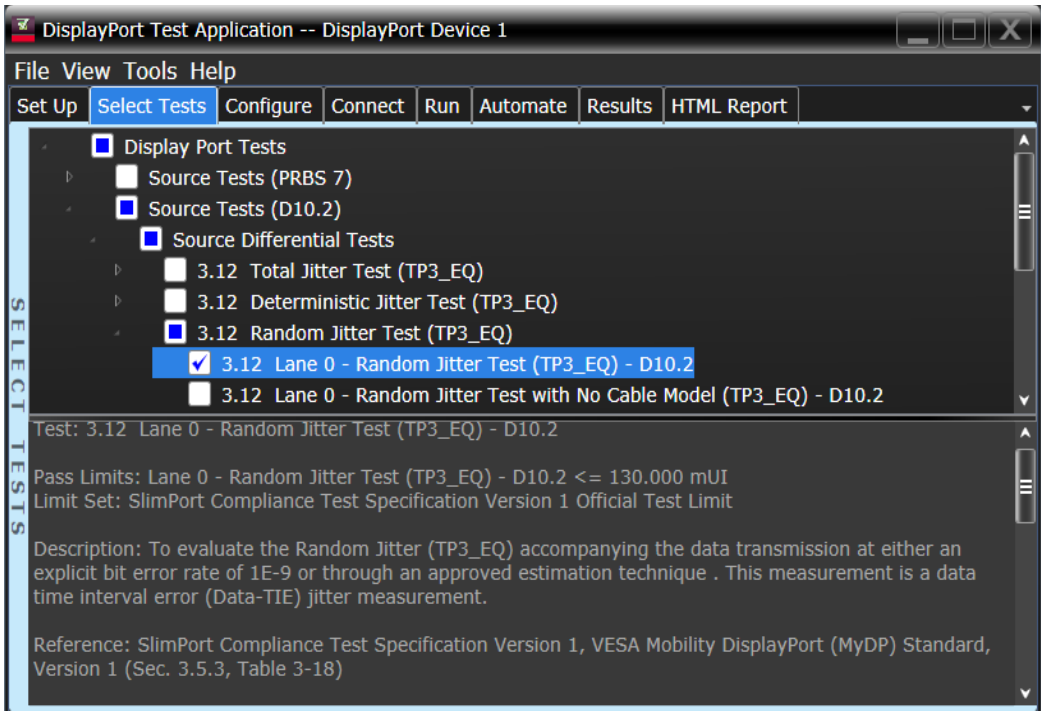
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Random Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2, HBR25
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	Lane 0
Test Pattern	D10.2
Cable Model	“Worst Case” and “Zero Length” conditions


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
1 Channel
Channel Selection - Differential Probe
Lane 0
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Random Jitter Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Random Jitter Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 277 Random Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
$T_{TX\text{-}RJ\_D10.2\_HBR2}$	0.23 UI

UI is Unit Interval.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18*

Expected/Observable Results

The measured random jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source AC Common Mode Test (Informative)

Test ID

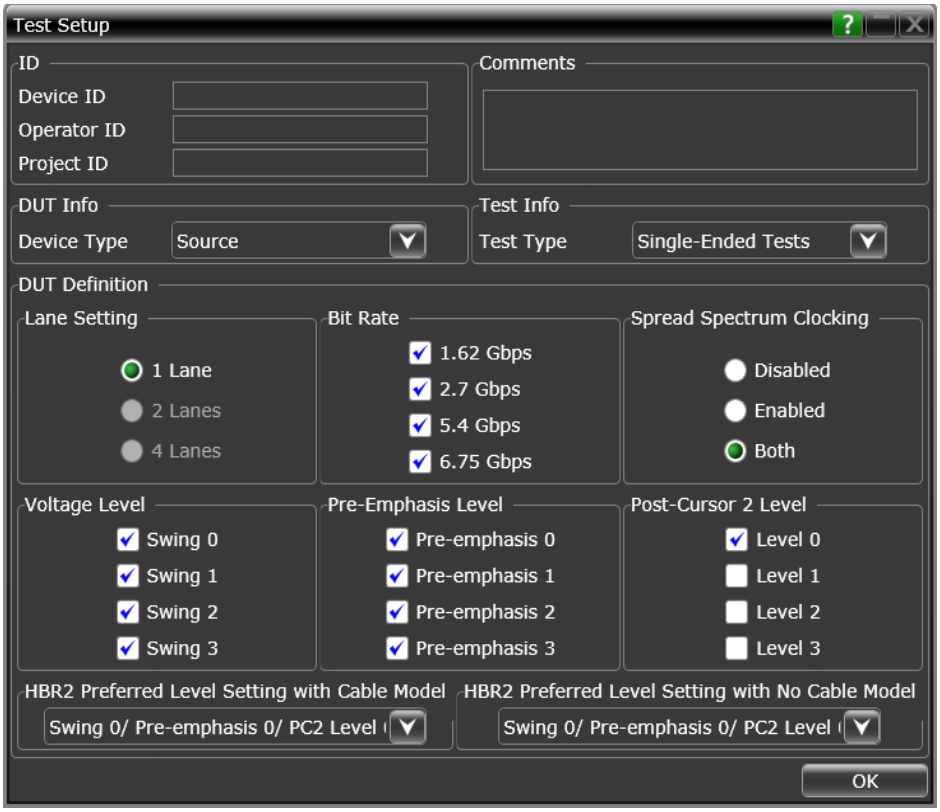
12110001 – AC Common Mode Test (Informative)

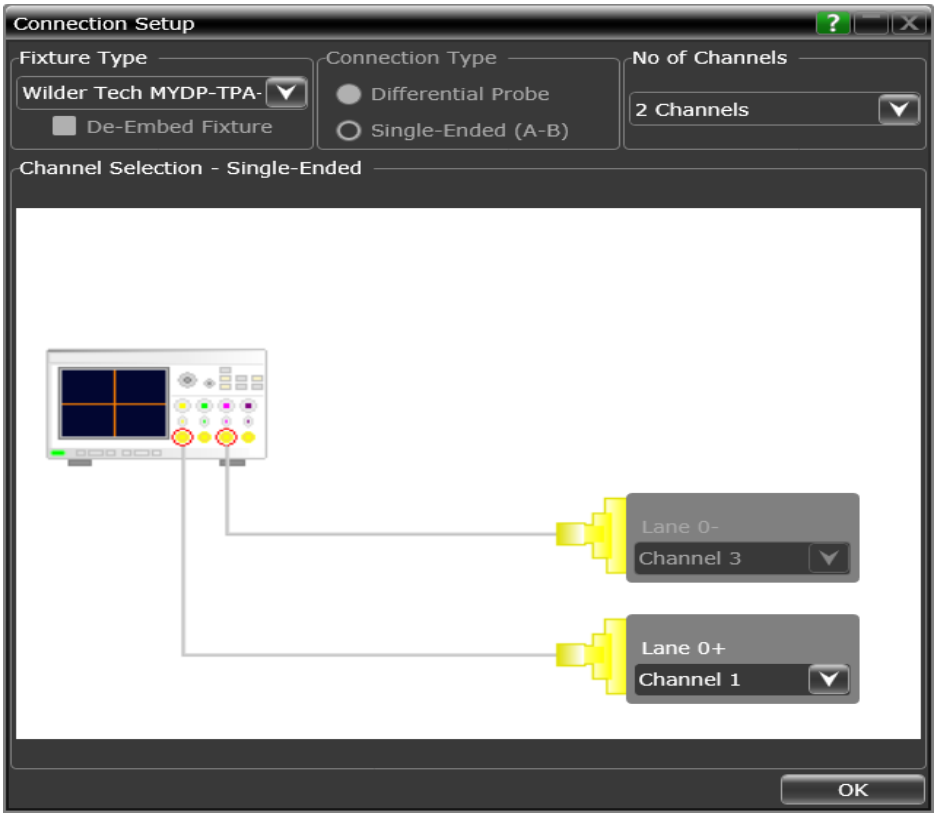
Test Overview

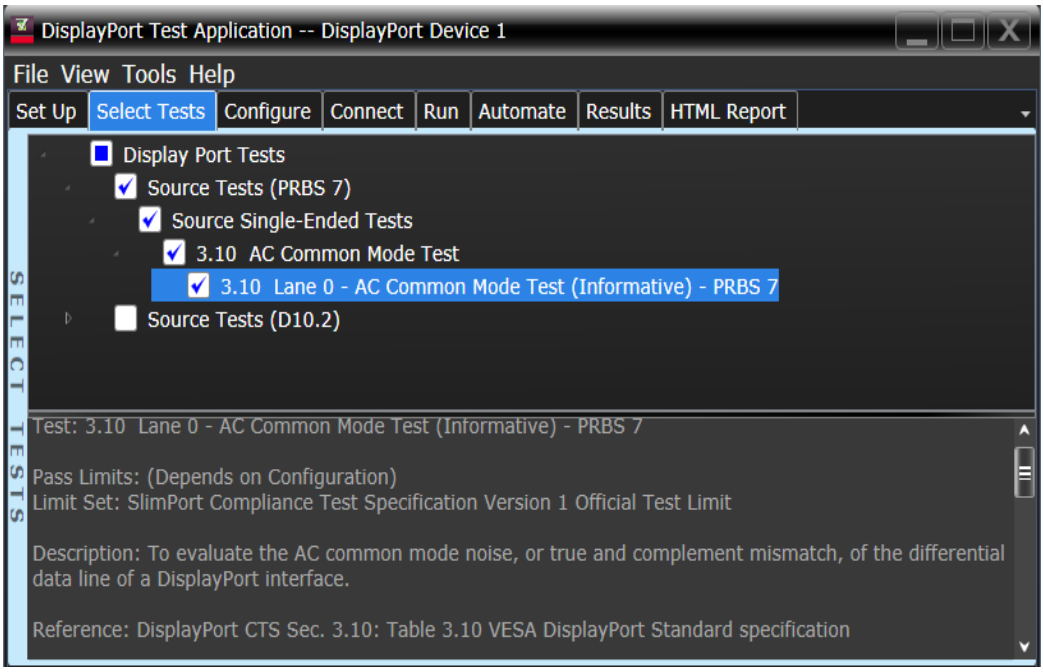
The objective of this test is to evaluate the AC Common Mode noise (unfiltered rms) of the differential data line of the DP interface.

Test Conditions for AC Common Mode Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR25)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage level supported
Pre-Emphasis Level	All pre-emphasis level supported subject to the constraints in Table 3-1 of the VESA DisplayPort 1.2a Standard
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Single-Ended Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
2 Channels
Channel Selection - Single-Ended
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Create FUNC3 signal, which is the common mode signal of the input single-ended signal.
4 If the filter is enabled ["Filter" configuration variable set to "High Pass Filter", "Low Pass Filter" or "None" (Default)]:
   a Create FUNC4 signal, which is the filtered FUNC3 signal by applying the High Pass filter or Low Pass filter on the FUNC3 signal based on the Configuration Variable.
5 Set up two display grids such that one grid displays the input single-ended signal while the other grid displays the common mode signal.
6 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
7 Set up the parameters for RMS voltage measurement of the common mode signal.
   a Set up the V_{rms} measurement for the common mode signal.
   b Acquire the signal until 100,000 edges are measured.
8 Get the mean for the V_{rms} measurement.
9 Report the measurement results.

PASS Condition

For RBR and HBR:

AC Common Mode Voltage $\leq$ 20mV

For HBR2, HBR25:

AC Common Mode Voltage $\leq$ 30mV

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.10*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 9.2, Table 9-6*

Expected/Observable Results

The measured AC common mode noise for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Intra-Pair Skew Test (Informative)

Test ID

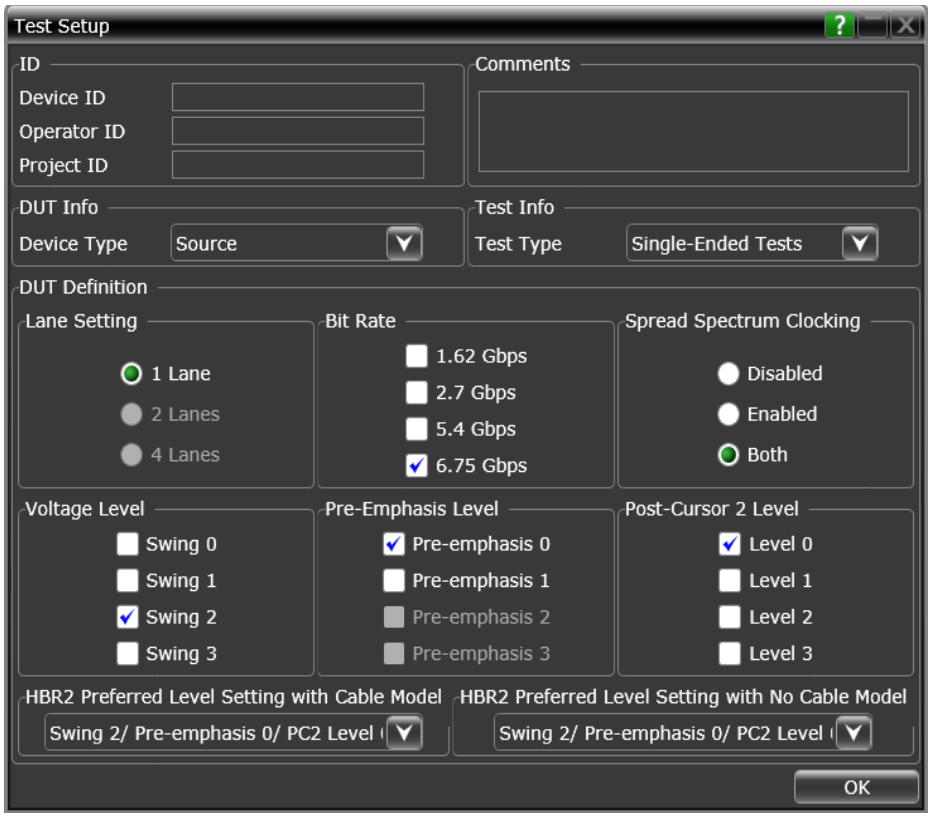
12100001 — Intra-Pair Skew Test (Informative)

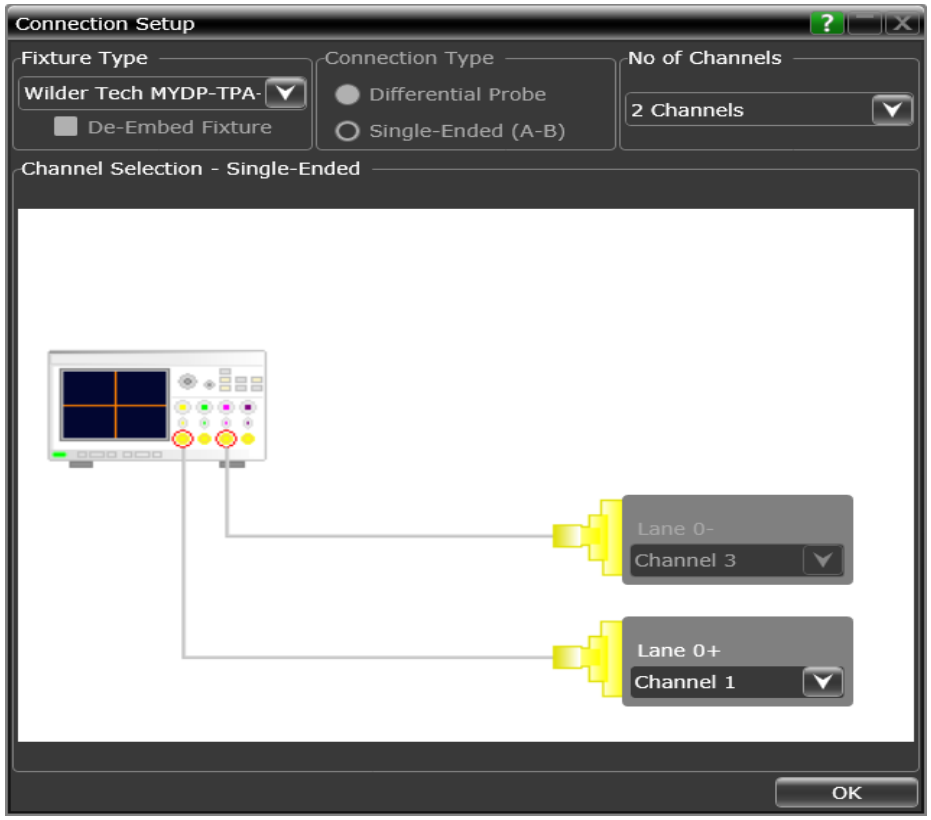
Test Overview

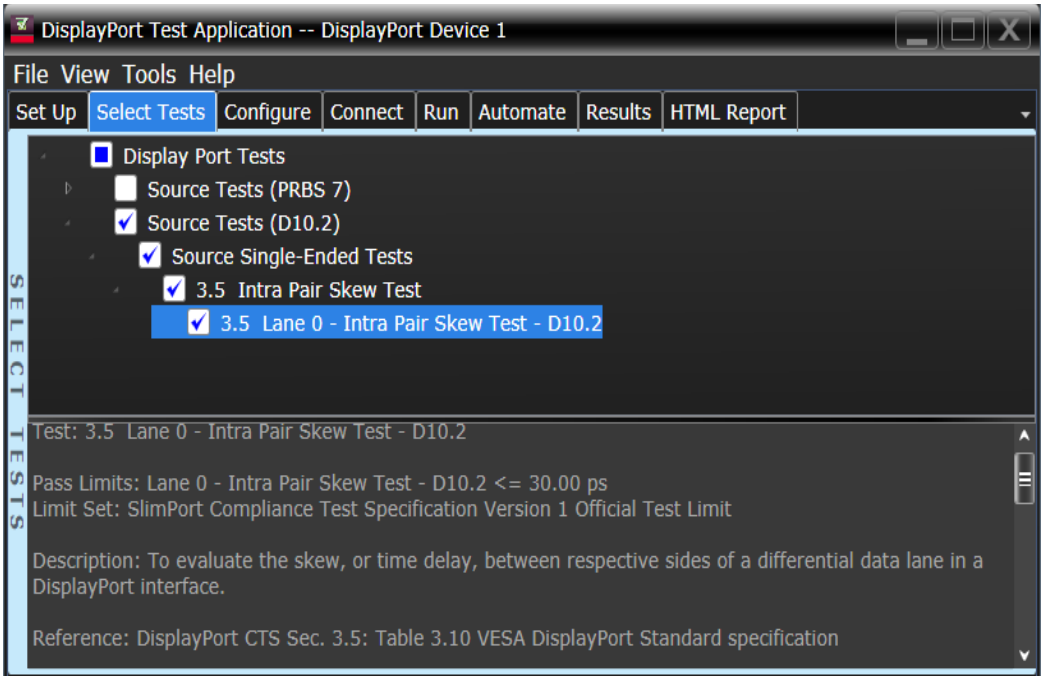
The objective of this test is to evaluate the skew or time delay between respective sides of a differential data lane in the DP interface.

Test Conditions for Intra-Pair Skew Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR25)
SSC	Both SSC conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0 (Lane 0+ to Lane 0-)
Test Pattern	D10.2


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Source
Test Info
Test Type
Single-Ended Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 2/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
2 Channels
Channel Selection - Single-Ended
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
4 Set up the parameters to perform High Level Voltage (V_{HIGH}) and Low Level Voltage (V_{LOW}) for each input single-ended signal.
   a Scale the vertical display of the input single-ended signal to optimum value.
   b Acquire the signal for 100 waveforms.
   c Find VHIGH by measuring the average voltage at 0.06 UI to 0.75 UI of the High Level.
   d Find VLOW by measuring the average voltage at 0.06 UI to 0.75 UI of the Low Level.
   e Calculate the Transition Voltage (V_{Trans}) using the equation:

$$V_{Trans} = (V_{HIGH} + V_{LOW}) / 2$$

5 Set up the parameters for the intra-pair skew measurement:

a Set up the measurement threshold for each single-ended data signal based on the measured Transition Voltage.

b Set up InfiniiScan to trigger on the desired pattern.

c Set up delta time measurement to measure time difference between the rising edge of the data true signal (D+) and the complement's (D-) falling edge:

$$D+_{Transition\_High} - D-_{Transition\_Low}$$

d Set up delta time measurement to measure time difference between the falling edge of the data true signal (D+) and the complement's (D-) rising edge:

$$D+_{Transition\_Low} - D-_{Transition\_High}$$

e Acquire the signal until you measure 100 edges.

f Calculate the intra-pair skew using the equation:

$$\text{Intra-Pair Skew} = \{1/\text{Number of Edges}\}$$

$$\sum \{[(D+_{Transition\_High} - D-_{Transition\_Low}) + (D+_{Transition\_Low} - D-_{Transition\_High})] / 2\}$$

6 Report the measurement results.

PASS Condition

Intra-Pair Skew ≤ 30 ps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.5*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured intra-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

36 SlimPort Sink Tests

Overview

Test Point Definition for SlimPort Sink Tests

NOTE Sink Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Sink DUT at Test Point 3 (TP3) as shown in Figure 254. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

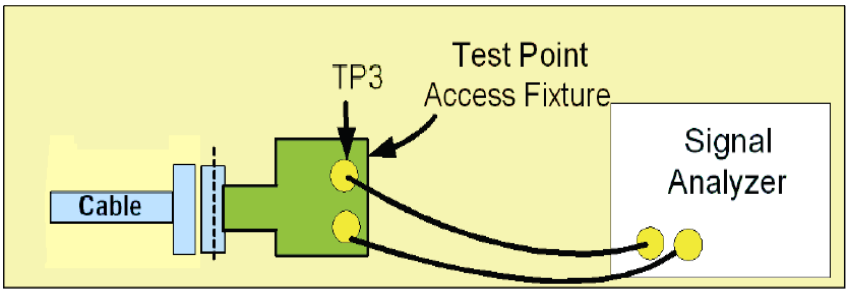


Figure 254 Test Point 3 Connection for SlimPort Sink Tests

Table 278 defines the test point fixtures and instruments used for SlimPort (MyDP HBR25) Sink Tests:

Table 278 Test Point Fixtures and Instruments for SlimPort (MyDP HBR25) Sink Tests

Test Requirement	Device Used
Test Point Access Fixture	Mobility DisplayPort Test Point Adapter For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Calibration of Stress Signal

For the calibration of the stress signal, you must test the stress signal in the manner shown in the Figure 255 for RBR and Figure 256 for HBR and HBR2.

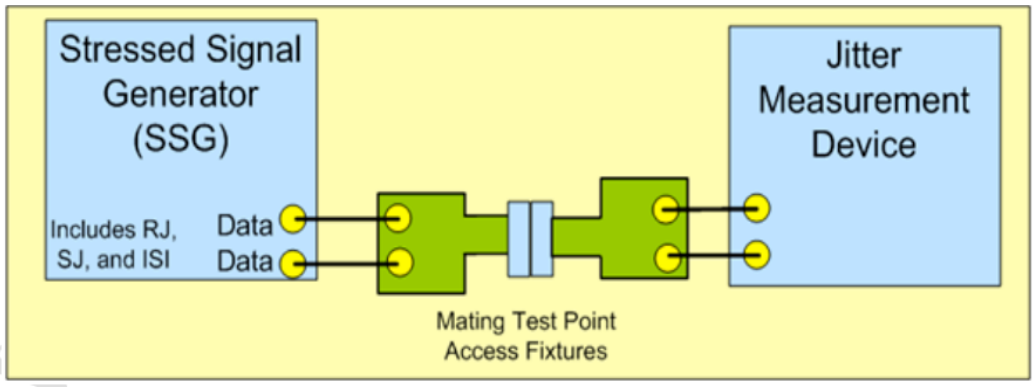


Figure 255 Test Point 3 Connection for Stress Signal Calibration of RBR

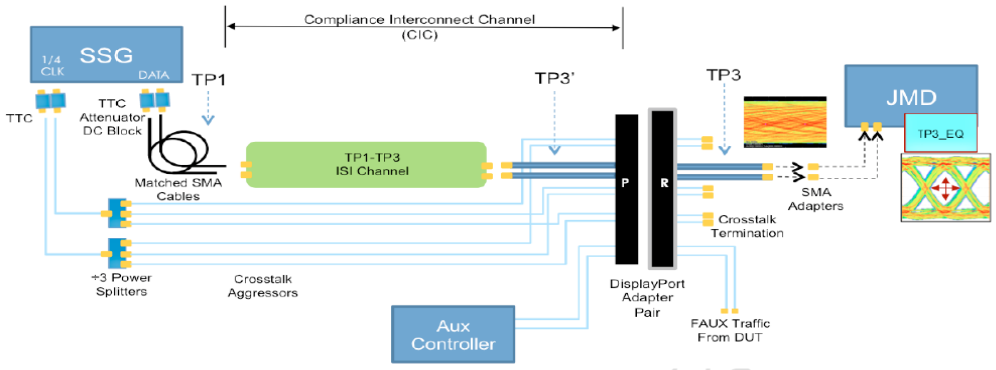


Figure 256 Test Point 3 Connection for Stress Signal Calibration of HBR and HBR2

Table 279 defines the Test Point Fixtures and Instruments for Stress Signal Calibration:

Table 279 Test Point Fixtures and Instruments for Stress Signal Calibration

Test Requirement	Device Used
Stress Signal Generator (SSG)	Bit Error Rate Tester ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	Mobility DisplayPort Test Point Adapter For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters.
Jitter Measurement Device (JMD)	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for SlimPort Sink Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort SlimPort Standards, select the option **MyDP HBR25** in the **Test Specification** area.

5 The option **Physical Layer Tests** appears by default in the **Test Selection** area.

6 Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.

7 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

8 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

9 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

10 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

11 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

12 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

13 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

14 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for SlimPort Sink Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

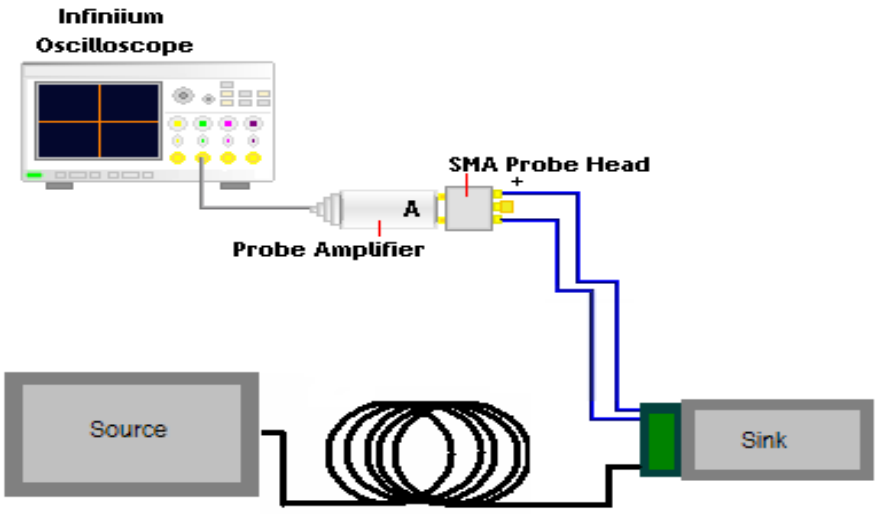


Figure 257 Sample connection diagram for SlimPort Sink Tests

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Sink tests to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1 In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.

2 On the **Test Setup** window,

a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b In the **DUT Info** area, select the **Device Type** as **Sink**.

c In the **Test Info** area, the **Test Type** options are grayed out.

d In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.

3 Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1. Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.
2. On the **Connection Setup** window,
   a The **Fixture Type** area is grayed out.
   b Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.
   c In the **Channel Selection** area, assign appropriate channels to lanes.
3. Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of sink tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for SlimPort Sink Tests" on page 1318 to complete the task flow for DUT setup along with configuring the Compliance Application to run each test.

Sink Eye Diagram Test

Test ID

12140001 — Eye Diagram Test

Test Overview

The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

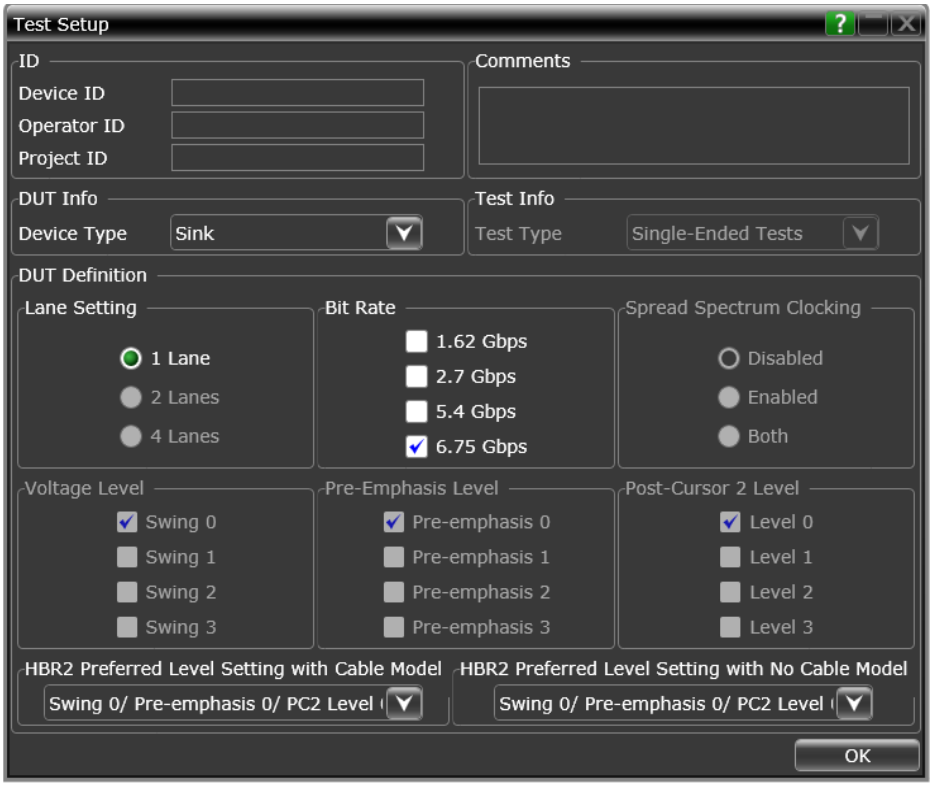
You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the following specifications for degradation:

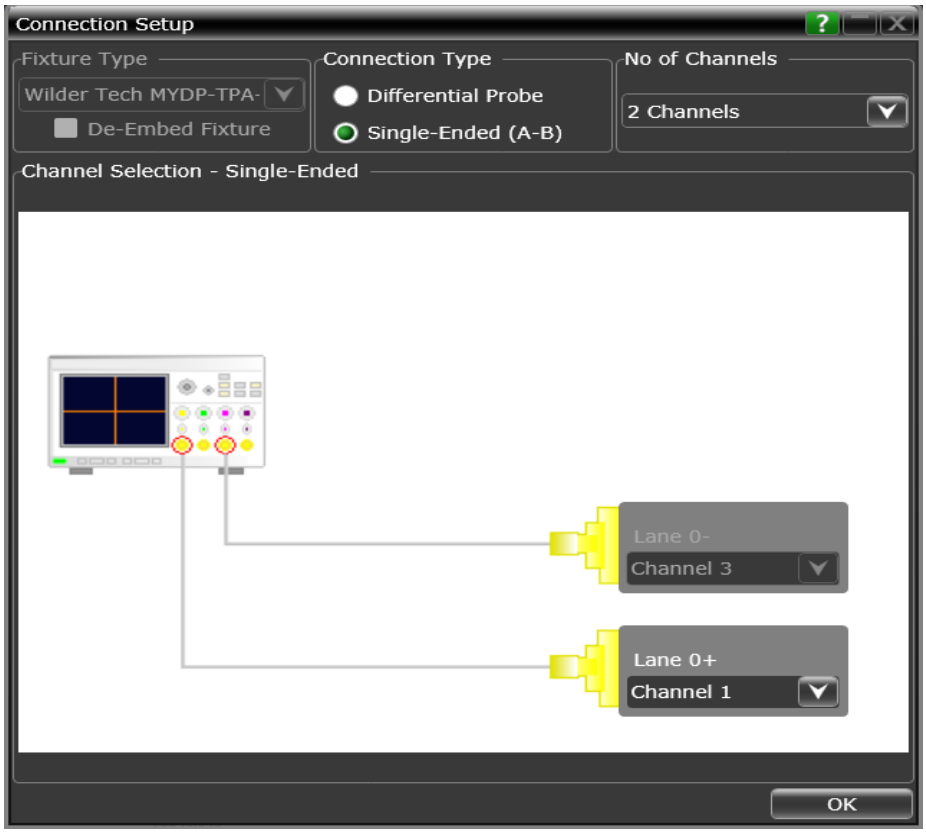
- Voltage Level:
  - 90mV peak to peak +/- 10% for HBR2 at TP3_EQ (Table 3-18, DP1.2a)
  - 150mV peak to peak +/- 10% for HBR at TP3_EQ (Table 3-25, DP1.2a)
  - 46mV peak to peak +/- 10% for RBR at TP3 (Table 3-26, DP1.2a)

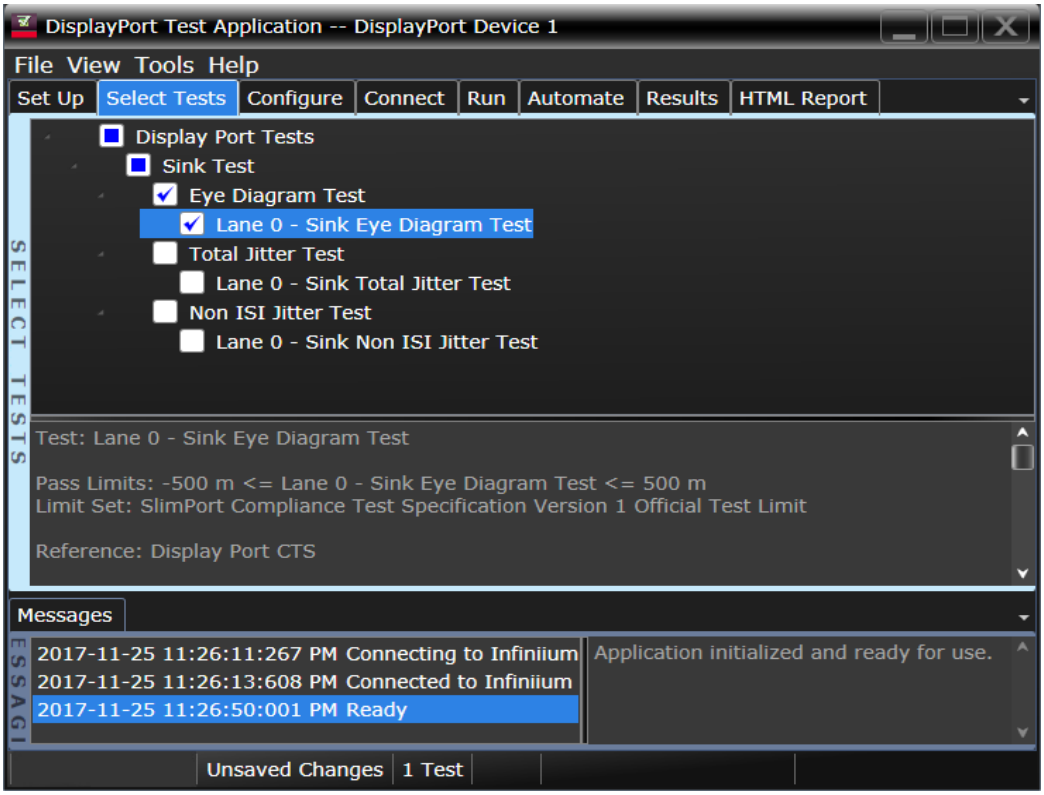
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR25–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR25)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR25–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Test Info
Test Type
Single-Ended Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
2 Channels
Channel Selection - Single-Ended
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.

8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
9 Measure the jitter of the eye diagram using the Histogram.
10 Check for any signal trajectories that may have entered into the mask.
11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 280 shows the voltage and time coordinates for the mask used for the eye diagram.

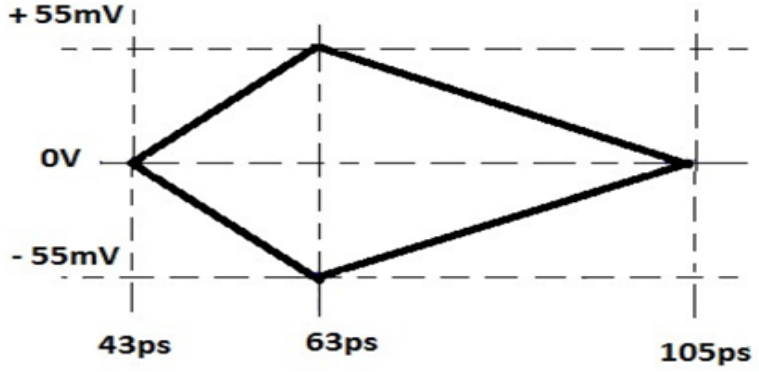


Figure 258 Eye Mask at TP3_EQ (HBR25)

Table 280 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

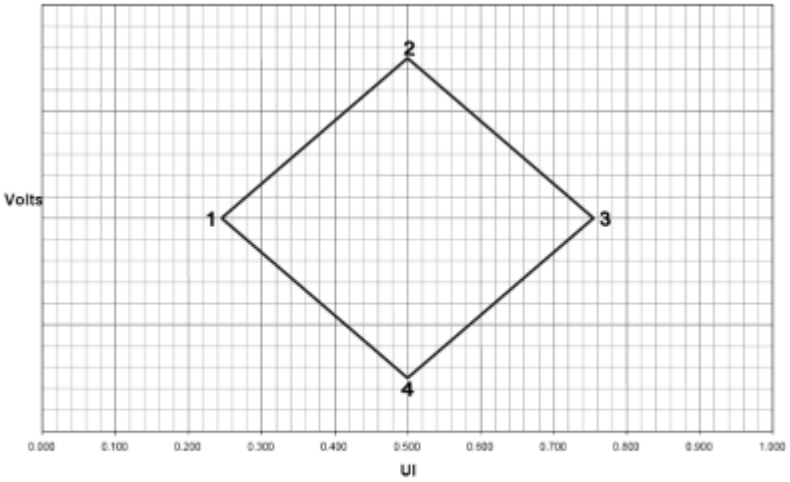


Figure 259 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 281 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.045*
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.045*

NOTE

*Eye height limit of 45 mV and -45 mV assumes cross-talk as 0, which is only possible in case of single lane testing.

In case of multi-lane testing, cross talk exists, and the eye height values deviate by ± 7 mV. Thus the eye height becomes (+45 +7) mV and (-45 -7) mV or +52 mV and -52 mV.

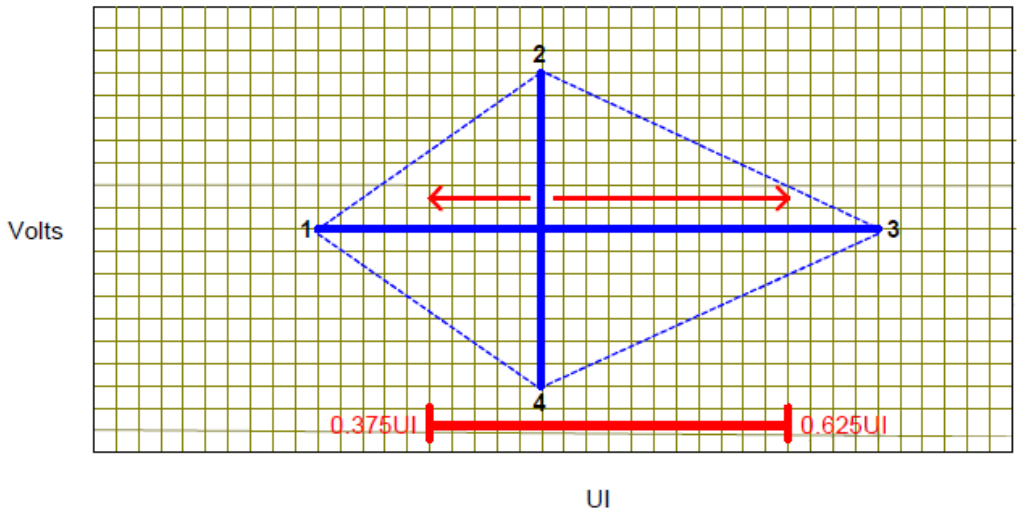


Figure 260 The Sink Eye Mask at TP3_EQ (HBR2)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Sink Total Jitter Test

Test ID

12210001 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

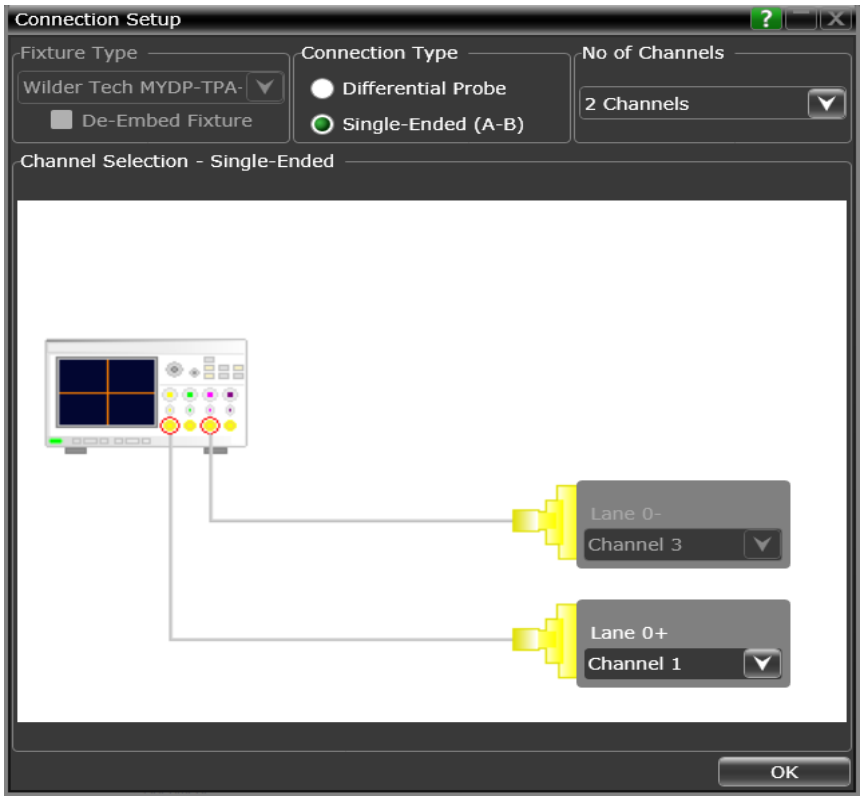
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

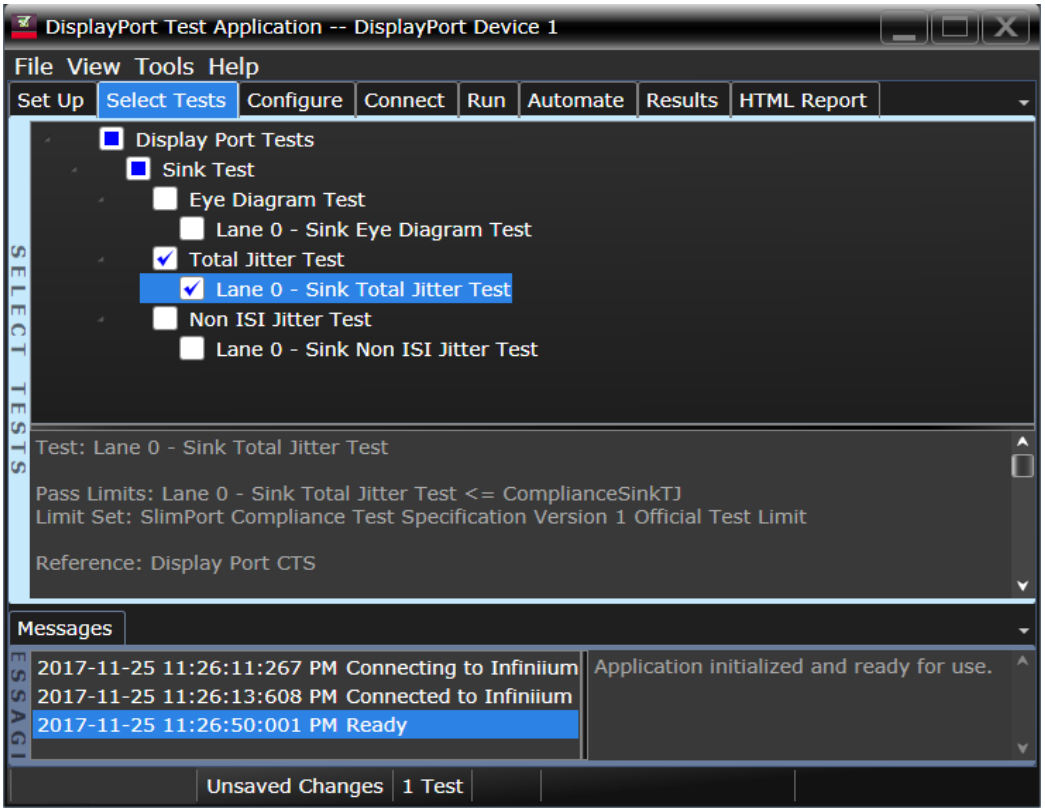
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR25–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR25)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR25–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Test Info
Test Type
Single-Ended Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
2 Channels
Channel Selection - Single-Ended
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.

7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:
- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 282 Total Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	0.580 UI*

* The limits for the Total Jitter are derated by 0.04 UI from 0.62 UI in DisplayPort 1.2a Standard.

Table 283 Total Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Sink Non-ISI Jitter Test

Test ID

12220001 — Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the Non ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Calculate Non-ISI Jitter using the following equation:

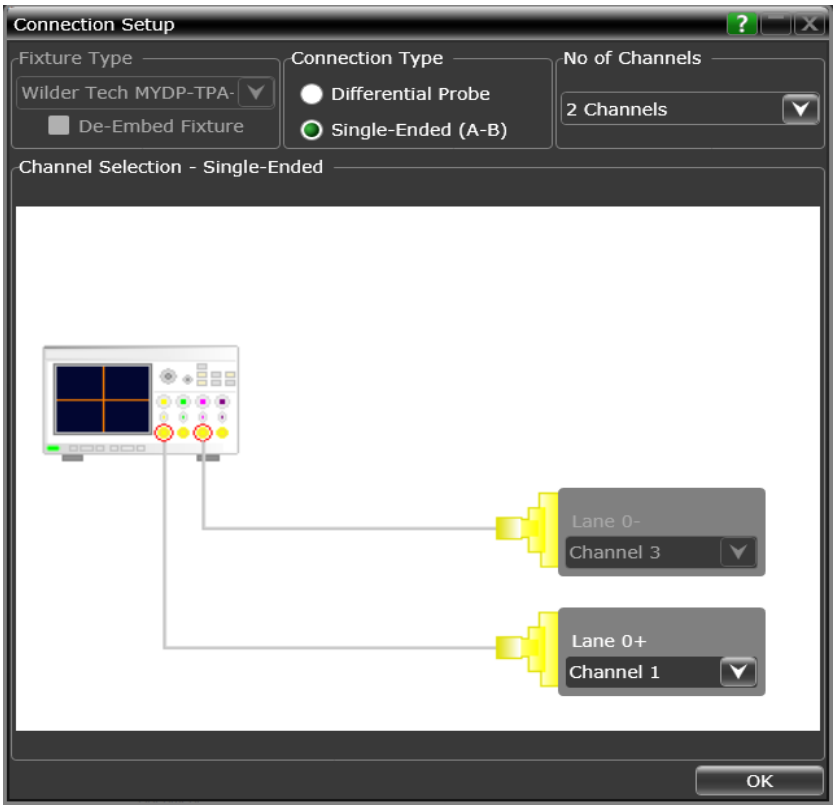
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

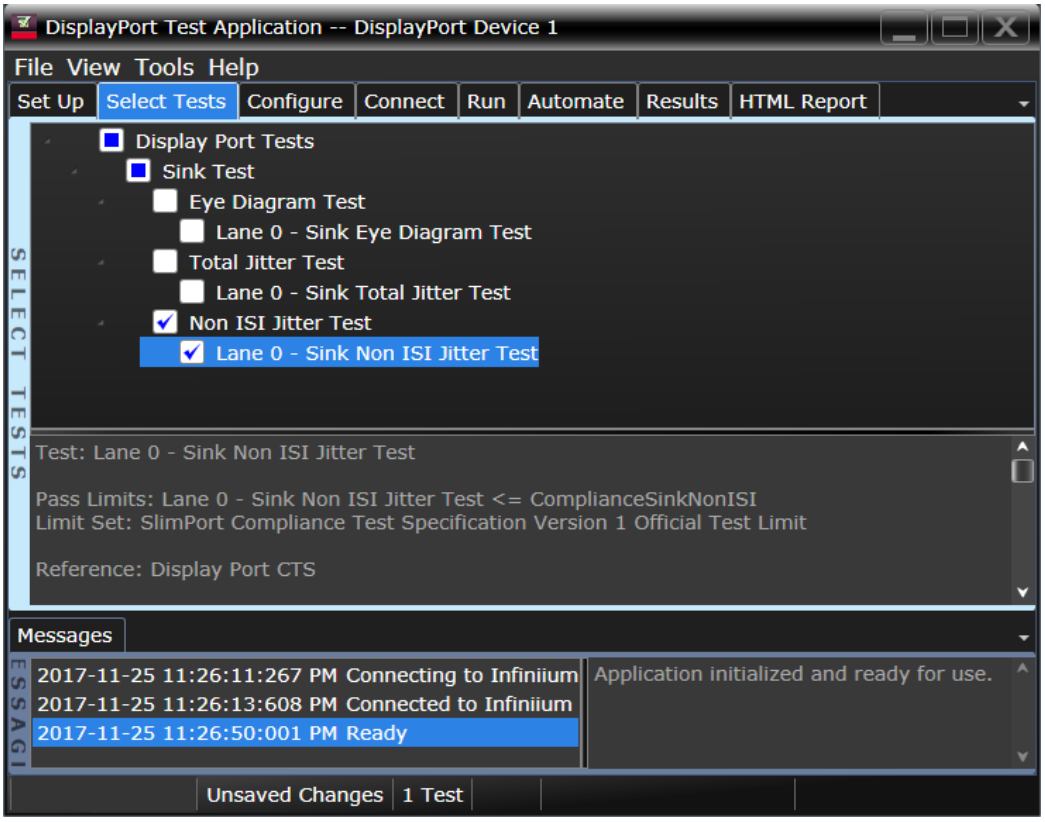
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR25–TP3_EQ
Bit Rate	All bit rates (for RBR, HBR, HBR2 and HBR25) supported
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR25–HBR2CPAT


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Sink
Test Info
Test Type
Single-Ended Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
HBR2 Preferred Level Setting with Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
HBR2 Preferred Level Setting with No Cable Model
Swing 0/ Pre-emphasis 0/ PC2 Level
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
2 Channels
Channel Selection - Single-Ended
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.

7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 284 Non ISI Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	-

Table 285 Non ISI Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

37 SlimPort Cable Tests

Overview

Test Point Definition for SlimPort Cable Tests

NOTE Cable Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Cable DUT at Test Point 3 (TP3) as shown in Figure 261. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

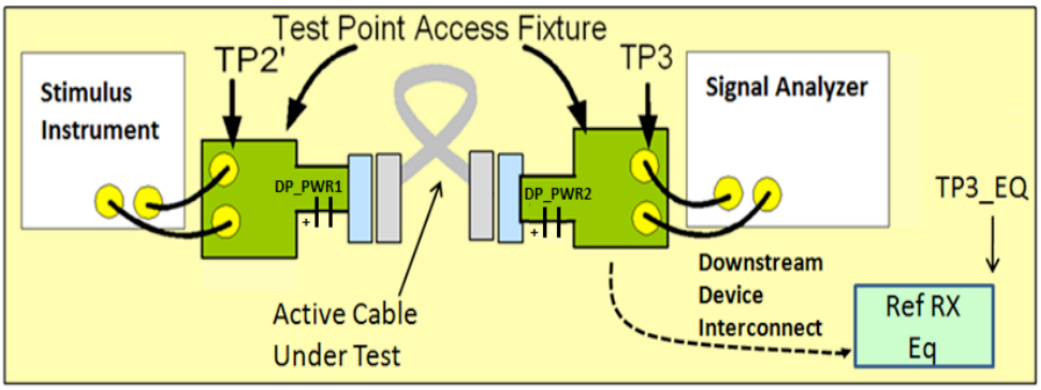


Figure 261 Test Point 3 Connection for SlimPort Cable Tests

Table 286 defines the test point fixtures and instruments used for SlimPort (MyDP HBR25) Cable Tests:

Table 286 Test Point Fixtures and Instruments for SlimPort (MyDP HBR25) Cable Tests

Test Requirement	Device Used
Stimulus Instrument	Pulse Pattern Generator ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Table 287 defines the input signal parameters applied by the stimulus instrument at TP2:

Table 287 Input Signal Parameters by Stimulus Instrument

RBR	▪ Reference Table 3-22 and Table 3-24, DP 1.2a ▪ Edge Rate (20-80): 155-165ps (260mUI) ▪ Eye Height: 400mV ▪ Total Jitter: 270mUI ▪ ISI: 100mUI ▪ Random Jitter (rms): 7.9mUI ▪ Sinusoidal Jitter: ~75mUI at 20MHz (Adjust to achieve Total Jitter)
HBR	▪ Reference Table 3-22 and Table 3-23, DP 1.2a ▪ Edge Rate (20-80): 90-100ps (260mUI) ▪ Eye Height: 350mV ▪ Total Jitter: 420mUI ▪ ISI: 144mUI ▪ Random Jitter (rms): 13.2mUI ▪ Sinusoidal Jitter: ~117mUI at 20MHz (Adjust to achieve Total Jitter)

Setting Up the DisplayPort Compliance Test Application for SlimPort Cable Tests

Before you run the compliance tests on the Device Under Test (DUT):

1. Connect the appropriate test fixture to the DUT.
2. Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.
3. The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).
4. To test for compliance with DisplayPort SlimPort Standards, select the option **MyDP HBR25** in the **Test Specification** area.
5. The option **Physical Layer Tests** appears by default in the **Test Selection** area.
6. Based on the waveform requirements, select the appropriate option in the **Capture and Analysis Mode** area.
7. If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.
8. Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.
9. Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.
10. De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.
11. After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.
12. Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.
13. Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.
14. Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for SlimPort Cable Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

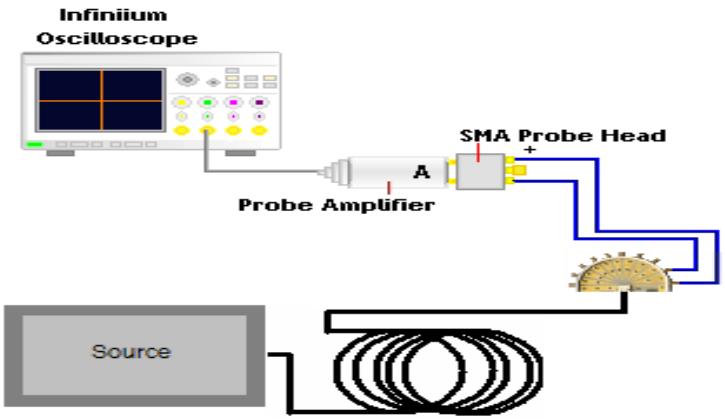


Figure 262 Sample connection diagram for SlimPort Cable Tests

Configuration for Test Setup and Connection Setup

Following steps describe the common settings that must be selected on the **Test Setup** and **Connection Setup** windows for the Cable tests to appear under the **Select Tests** tab. However, there are specific settings that must be configured on the **Test Setup** window, which can be found in "Test Conditions for <*test-name*>" section of each test. You shall also find images of the **Test Setup** and **Connection Setup** windows to view the options selected for the corresponding test.

Configuring the Test Setup window

1 In the **Test Environment Setup** area, click the **Test Setup** button. The **Test Setup** window appears.

2 On the **Test Setup** window,

a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b In the **DUT Info** area, select the **Device Type** as **Cable**.

c In the **Test Info** area, the **Test Type** options are grayed out.

d In the **DUT Definition** area, select options based on the settings defined in the Test Conditions section for each test.

3 Click **OK** to return to the **Set Up** tab.

Configuring the Connection Setup window

1. Click the **Connection Setup** button that appears in the **Test Environment Setup** area. The **Connection Setup** window is displayed.
2. On the **Connection Setup** window,
   a. The **Fixture Type** area is grayed out.
   b. Select the appropriate **Connection Type**, depending on whether you are using differential or single-ended probes and **No of Channels**, which must be assigned to the total number of lanes selected in the **Test Setup** window.
   c. In the **Channel Selection** area, assign appropriate channels to lanes.
3. Click **OK** to return to the **Set Up** tab.

After configuring the **Test Setup** and **Connection Setup** to run a specific type of cable tests, click the **Select Tests** tab to view and select the tests, which appear based on the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows. See "Setting Up the DisplayPort Compliance Test Application for SlimPort Cable Tests" on page 1338 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Cable Eye Diagram Test

Test ID

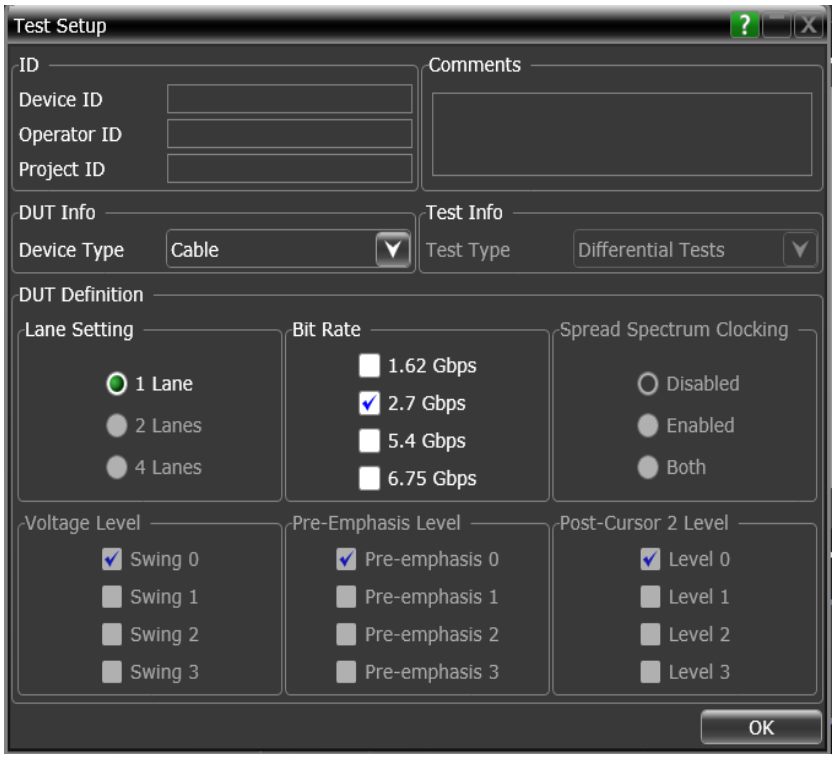
12150001 – Eye Diagram Test

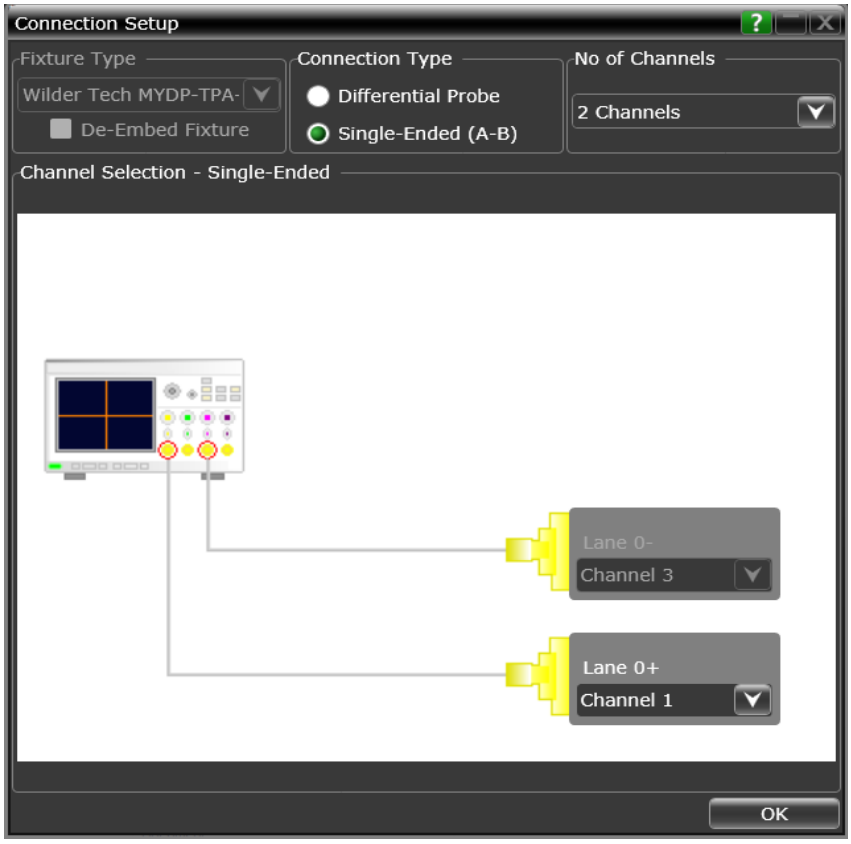
Test Overview

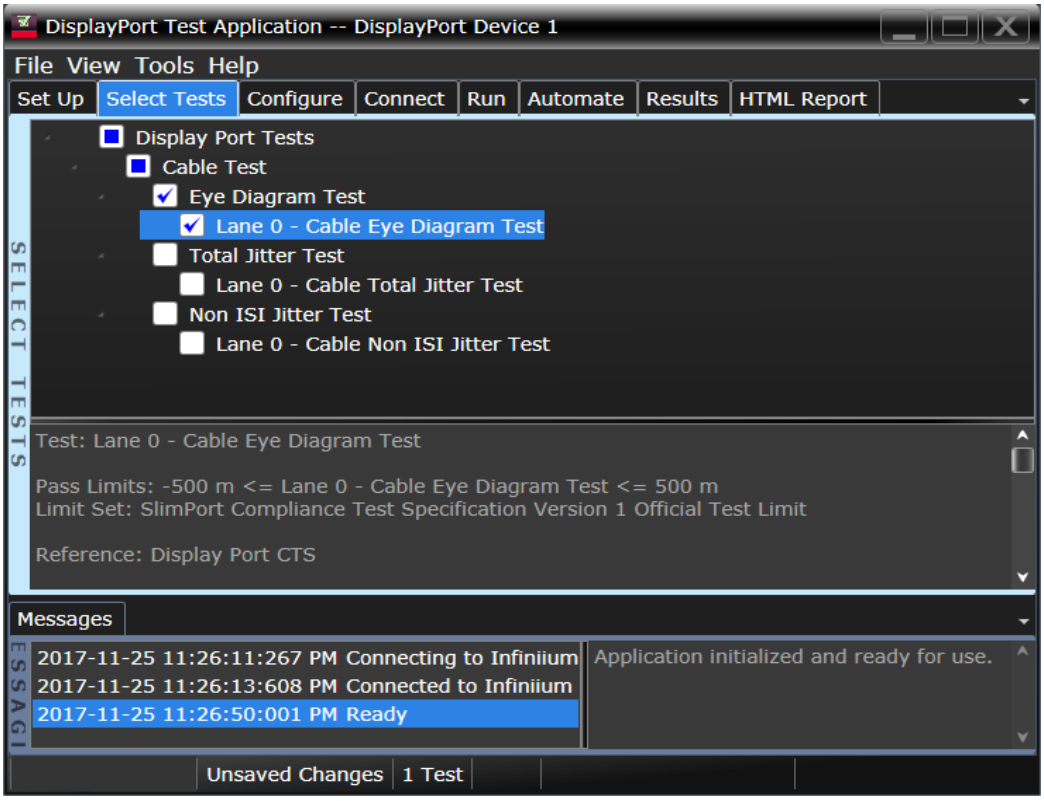
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 287
Crosstalk Signal Parameter	Quarter-rate clock signal (D24.3 pattern) is injected to lanes other than the lane under test. The characteristics of the aggressor signals are: Pattern–D24.3 Bit Rate–(Same as lane under test) Voltage Amplitude–(Same as lane under test) ▪ RBR-400mV ▪ HBR-350mV Edge Rate (20-80)–130ps at TP3


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
2 Channels
Channel Selection - Single-Ended
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure:

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.

8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
9 Measure the jitter of the eye diagram using the Histogram.
10 Check for any signal trajectories that may have entered into the mask.
11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 288 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 288 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

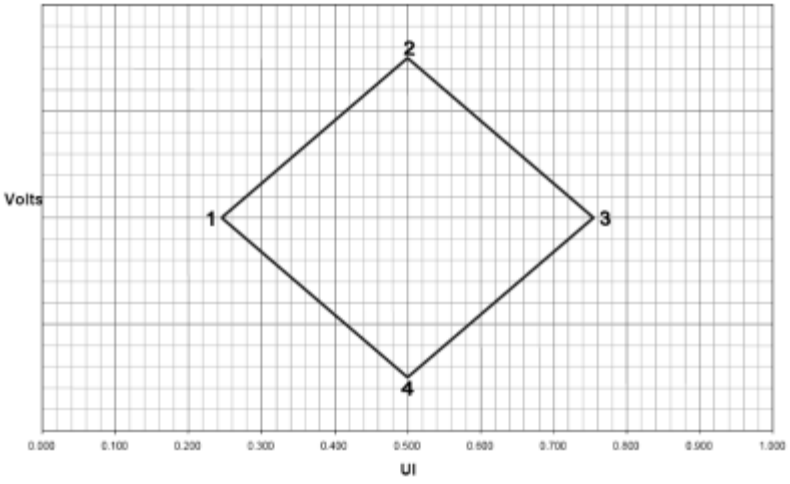


Figure 263 The Cable Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.3*

- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Cable Total Jitter Test

Test ID

12230001 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

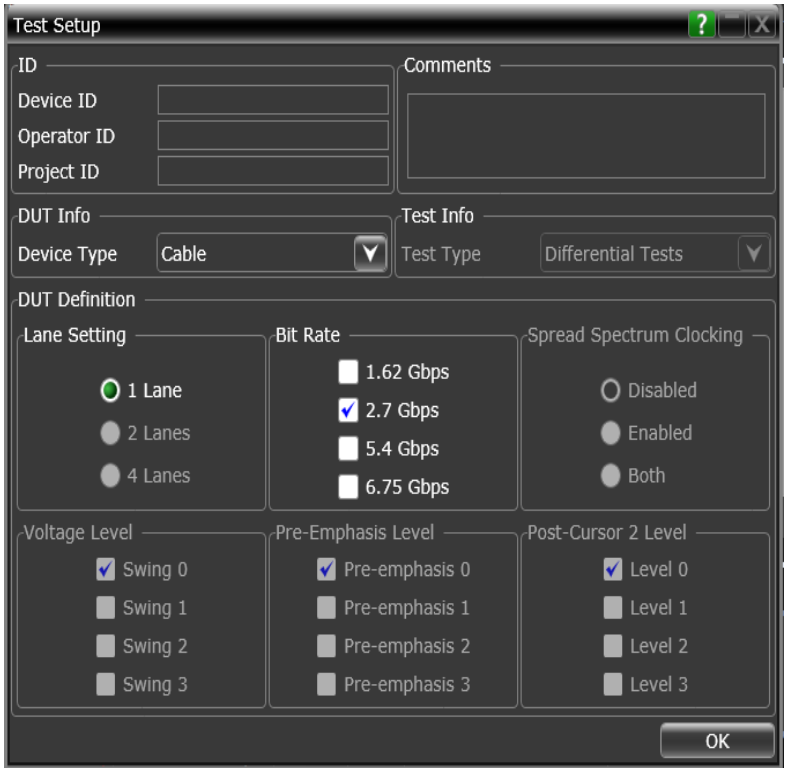
The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

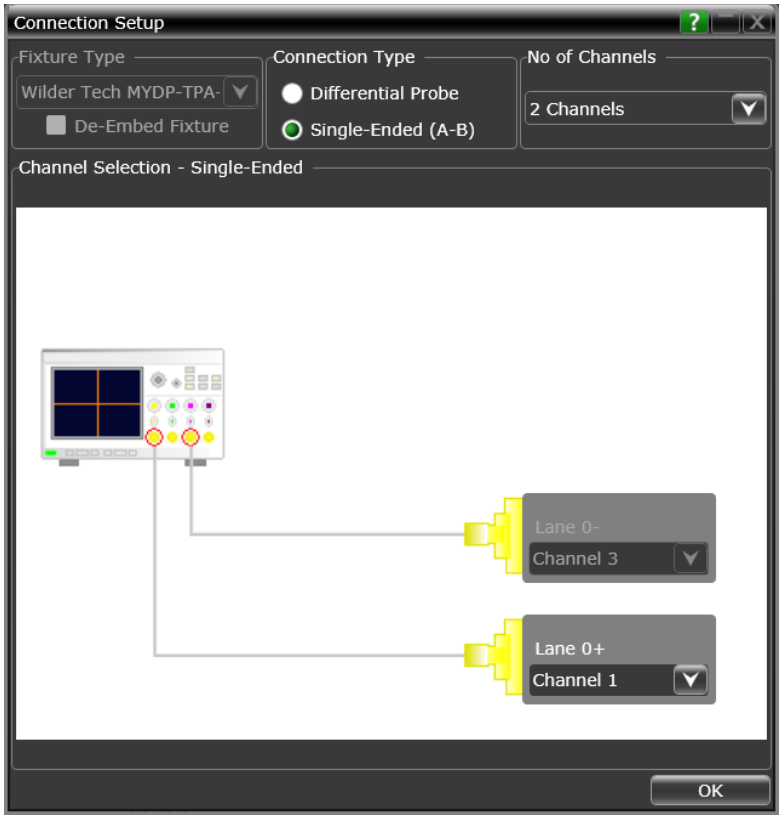
$$TJ = DJ_{dd} + n^* RJ_{rms}$$

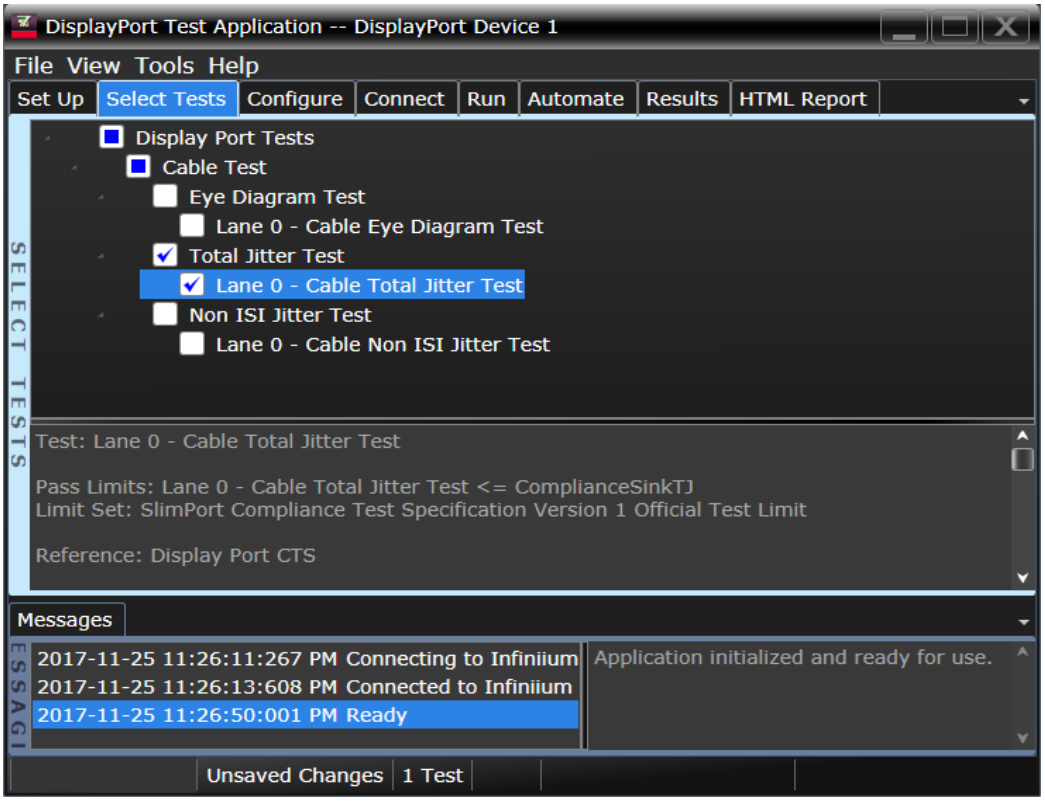
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 287


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
2 Channels
Channel Selection - Single-Ended
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.

7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 289 Total Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Cable Non-ISI Jitter Test

Test ID

12240001 — Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

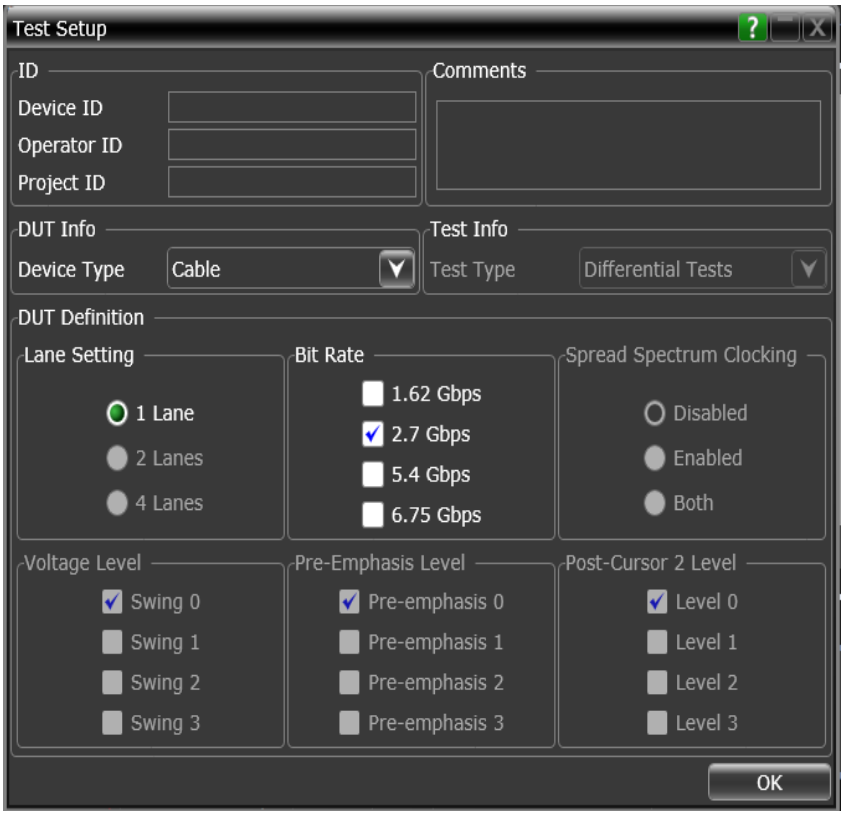
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

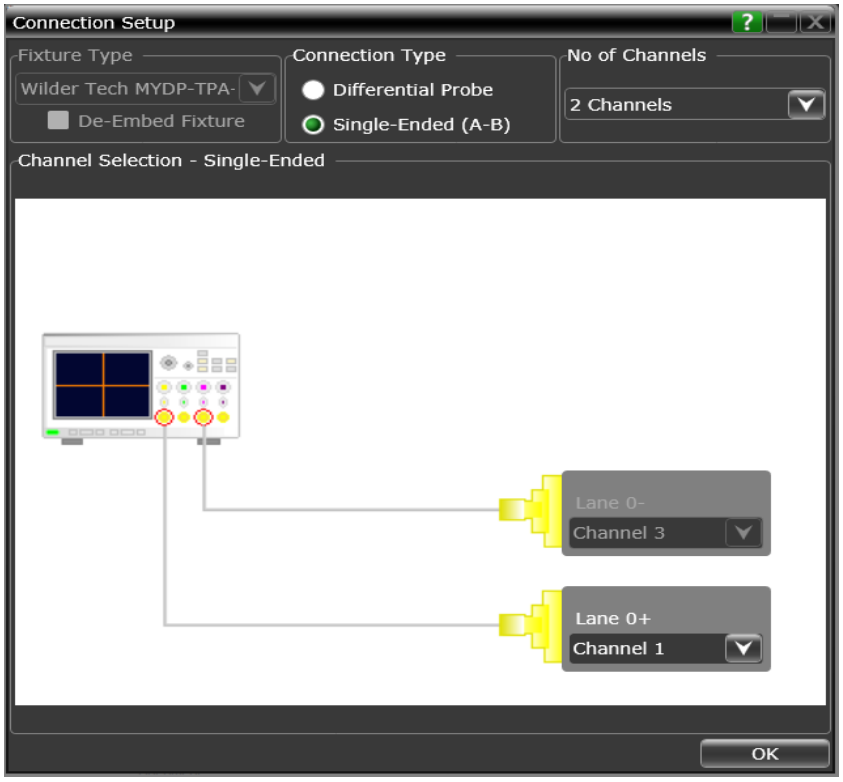
Calculate Non-ISI Jitter using the following equation:

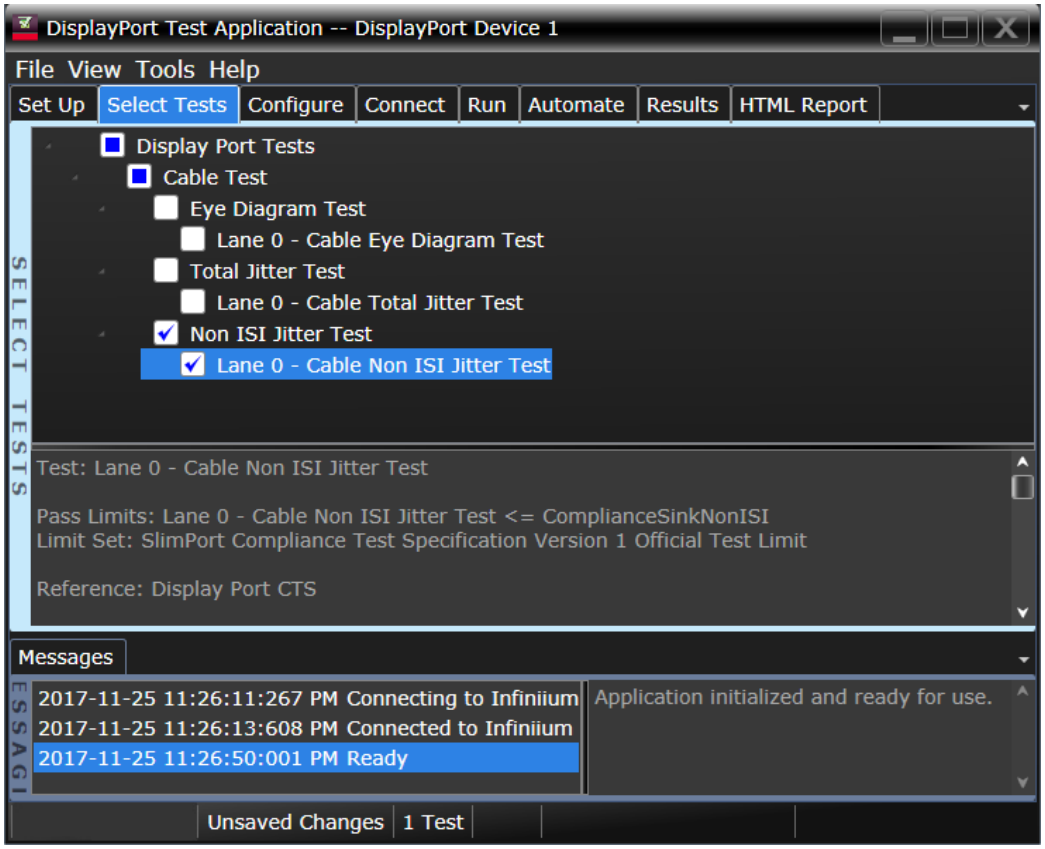
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 287


Test Setup
ID
Device ID
Operator ID
Project ID
Comments
DUT Info
Device Type
Cable
Test Info
Test Type
Differential Tests
DUT Definition
Lane Setting
1 Lane
2 Lanes
4 Lanes
Bit Rate
1.62 Gbps
2.7 Gbps
5.4 Gbps
6.75 Gbps
Spread Spectrum Clocking
Disabled
Enabled
Both
Voltage Level
Swing 0
Swing 1
Swing 2
Swing 3
Pre-Emphasis Level
Pre-emphasis 0
Pre-emphasis 1
Pre-emphasis 2
Pre-emphasis 3
Post-Cursor 2 Level
Level 0
Level 1
Level 2
Level 3
OK


Connection Setup
Fixture Type
Wilder Tech MYDP-TPA-
De-Embed Fixture
Connection Type
Differential Probe
Single-Ended (A-B)
No of Channels
2 Channels
Channel Selection - Single-Ended
Lane 0-
Channel 3
Lane 0+
Channel 1
OK



Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.

6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 290 Non ISI Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non-ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

38 SlimPort AUX Channel Tests

Overview

This section describes the normative and informative AUX Channel physical layer tests and inrush tests for compliance verification of SlimPort source and sink.

Test Point for SlimPort AUX Channel Tests

You must test the Source and Sink/Branch devices at Test Point 2 (TP2). See Figure 264.

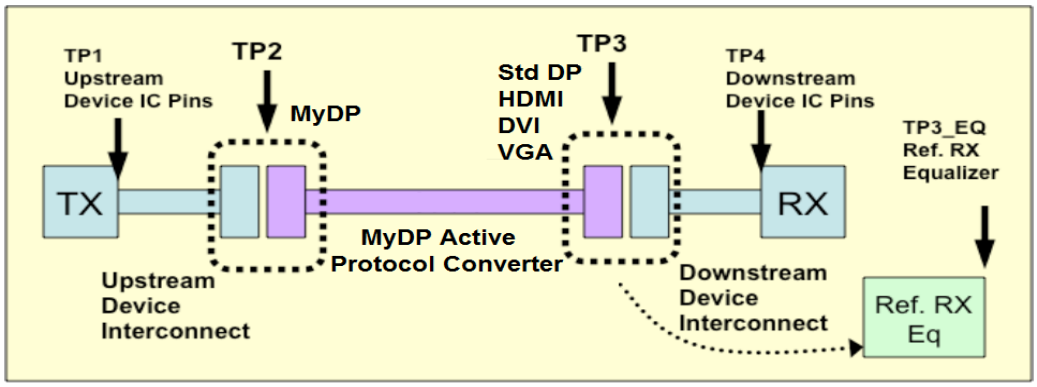


Figure 264 Test Point for SlimPort AUX Channel Tests

Table 291 defines the test point fixtures and instruments used for SlimPort (MyDP HBR25) AUX Channel Tests:

Table 291 Test Point Fixtures and Instruments for SlimPort (MyDP HBR25) AUX Channel Tests

Test Requirement	Device Used
Test Point Access Fixture	Mobility DisplayPort Test Point Adapter For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for SlimPort AUX Channel Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort SlimPort Standards, select the option **MyDP HBR25** in the **Test Specification** area.

5 Select the option **AUX PHY and Inrush Tests** in the **Test Selection** area.

6 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

7 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

8 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

9 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

10 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

11 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

12 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

13 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Settings for AUX PHY and Inrush Tests

Perform the following steps before you run the Auxiliary Channel and Inrush tests on the source or sink device:

1 Click the **Test Setup** button on the **Set Up** tab to set up for Auxiliary Channel and Inrush tests.

2 On the **Test Setup** window,

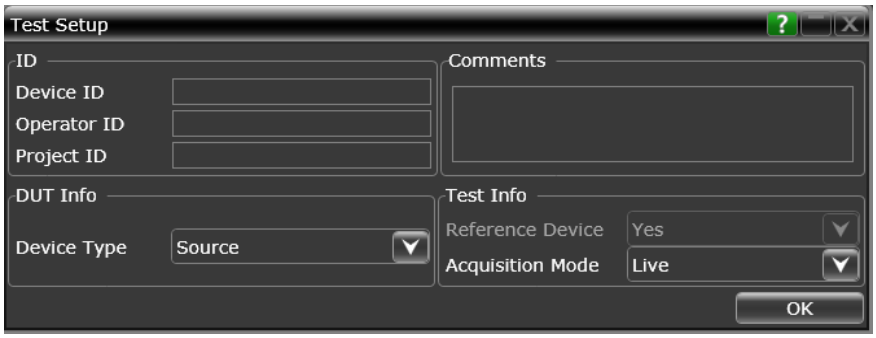
a Enter appropriate values in the various fields available in the **ID** and **Comments** areas to define your DUT, such that you can distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

b From the **Device Type** drop-down options, select either **Source** or **Sink**.

c The **Reference Device** drop-down options are grayed out.

d From the **Acquisition Mode** drop-down options, select **Live** if waveform acquisition and analysis will be performed on an online Infiniium Oscilloscope, else select **Offline**.

3 Click **OK** to exit the **Test Setup** window.

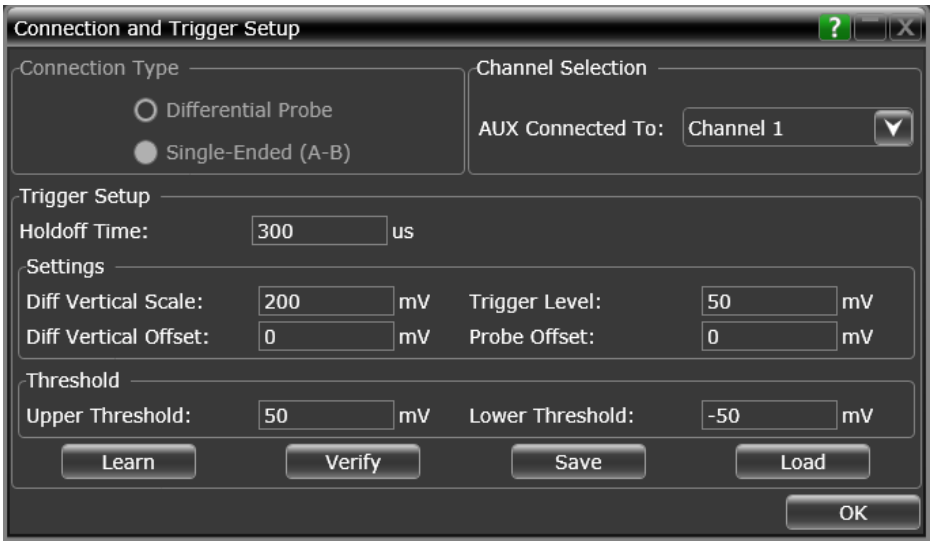


4 Click the **Connection Setup** button that now appears on the **Set Up** tab.

5 On the **Connection and Trigger Setup** window,

a The **Connection Type** area is grayed out.

b From the **AUX Connected To:** drop-down options of the **Channel Selection** area, select the Oscilloscope Channel where the Auxiliary Lane is connected to.



c In the **Trigger Setup** area, define the Oscilloscope parameters to trigger on an Auxiliary signal during testing.

- **Hold Off Time** – The Oscilloscope minimum hold off time before triggering the next waveform. Note that any Auxiliary transaction from the source must receive a reply from the sink in 400 us, else such a transaction is considered a timeout. Hold off time, in such cases, represents the minimum idle time before each AUX transaction is initialized. It is defaulted to 300 us which is a safe timing value for most devices tested in the lab. Most devices respond much faster than 300 us.
- **Trigger Level** – The AUX Channel signal level on which to trigger. Note that for a bi-directional signal (where a reference sink is attached), you must set the trigger level such that it crosses both the source command and the sink reply signal. Figure 265 and Figure 266 shows correct and incorrect trigger levels.

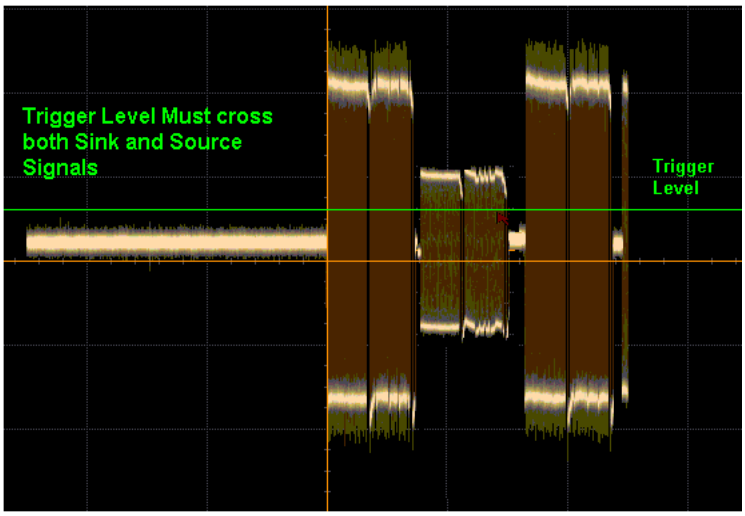


Figure 265 Correct Trigger Level

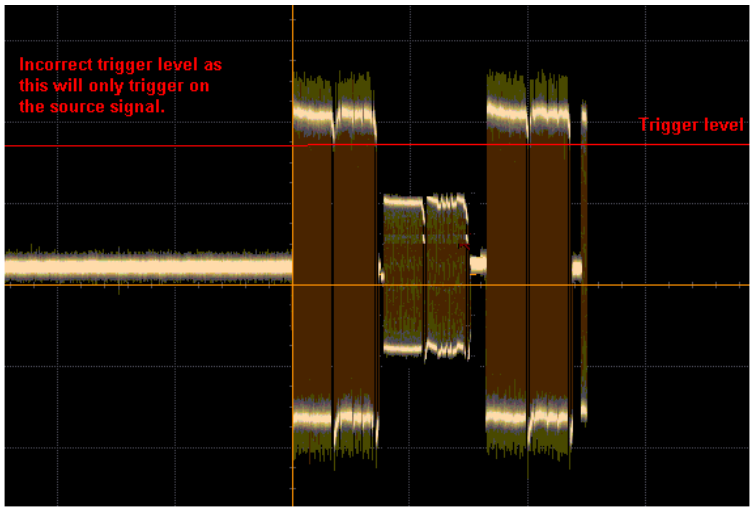


Figure 266 Incorrect Trigger Level

- **Vertical Scale** – The Oscilloscope vertical scale. Set the vertical to make sure that all signals are visible on the oscilloscope display.
- **Vertical Offset** – The Oscilloscope vertical offset. Set the offset so that the center point is aligned with the center of the oscilloscope display.
  Upper Threshold/Lower Threshold – The threshold level of signal must be set properly so that both upper and lower thresholds cross both the source and sink signals when the DUT is attached with a reference sink. The threshold levels are important parameters because they are used for edge detection when decoding a source command from a sink reply. Figure 267 and Figure 268 shows correct and incorrect threshold levels.

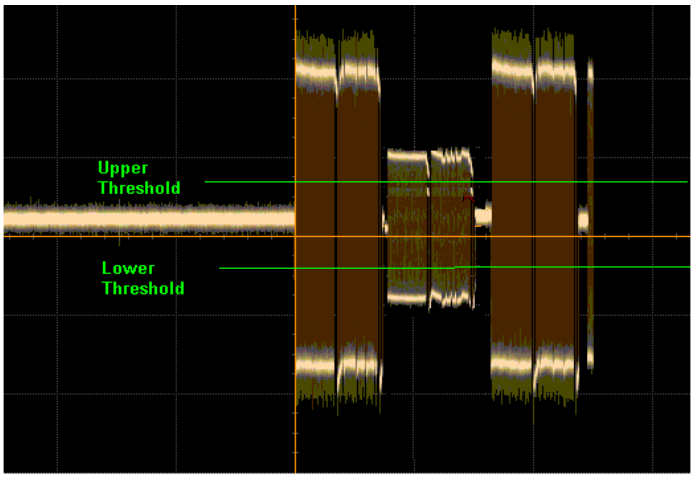


Figure 267 Correct Threshold set

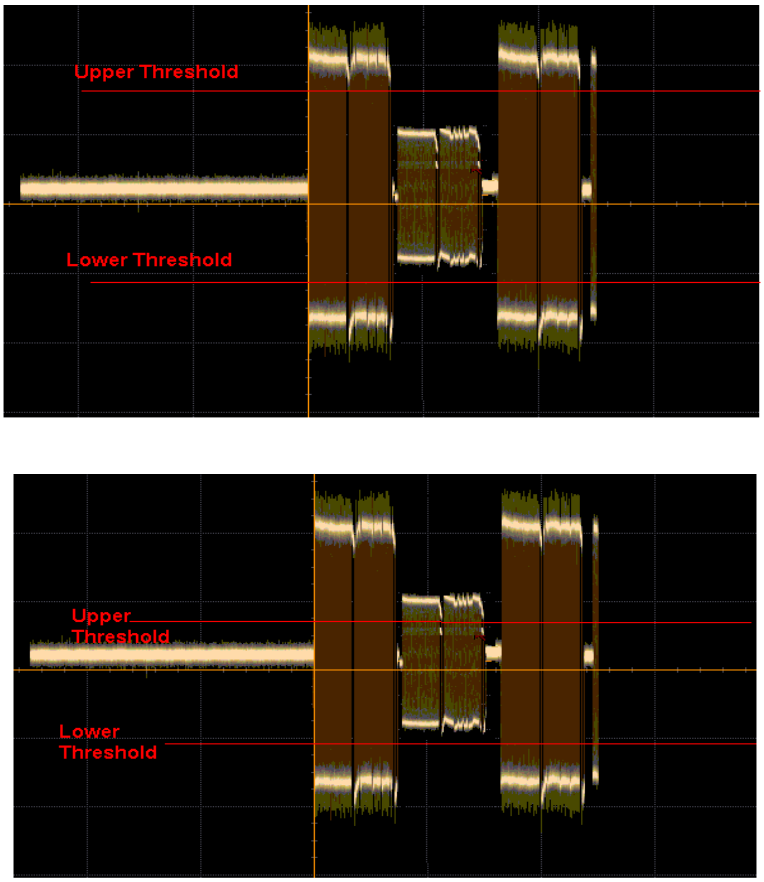


Figure 268 Wrong Thresholds set

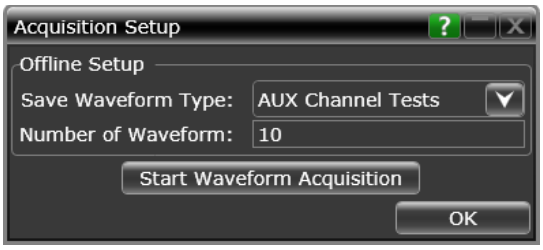
- Click the **Learn** button to access the information guide about the trigger setup parameters. However, note that the learning guide may not necessarily work due to variation in the actual Auxiliary signals, owing to different manufacturers. Keysight recommends that you must check to make sure that the parameters are correctly set as previously described.

- Click **Verify** and follow the instructions, if you wish to check the AUX Channel trigger.
- You may **Save** or **Load** the trigger setup configuration as a **.tsf* file.

6 Click **OK** to exit the **Connection and Trigger Setup** window.

7 If you select the option **Offline** for the **Acquisition Mode** in the **Test Setup** window, the **Acquisition Setup** button appears in the **Test Environment Setup** area of the **Set Up** tab.

8 Click the **Acquisition Setup** button to save the waveform files so that you can avoid the manual process to initiate Auxiliary transactions during the time of test runs.



9 On the **Acquisition Setup** window,

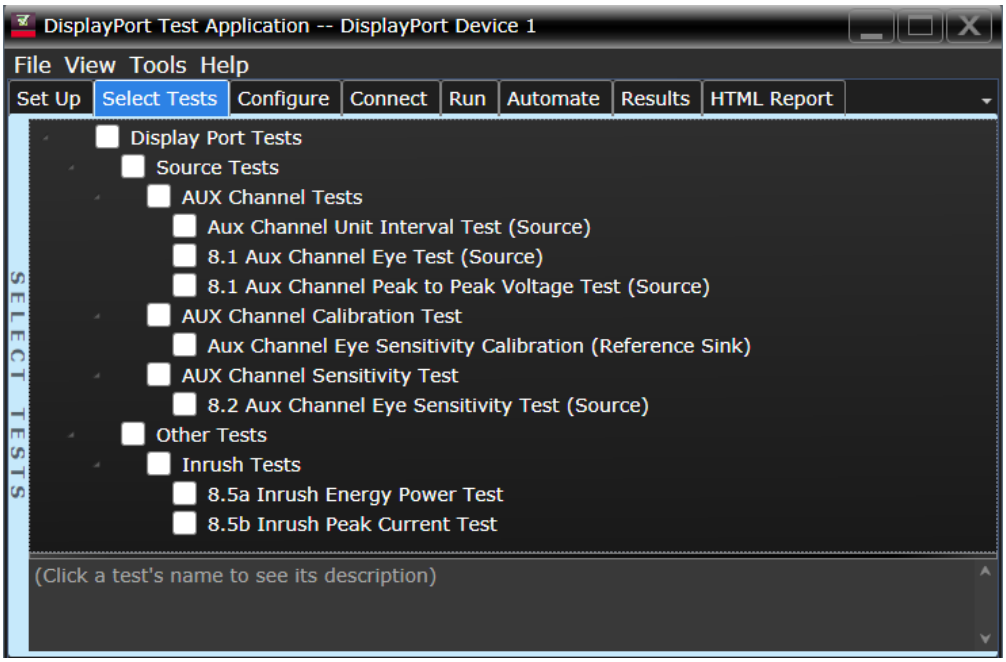
a select the type of waveforms to be saved from the **Save Waveform Type:** drop-down options.

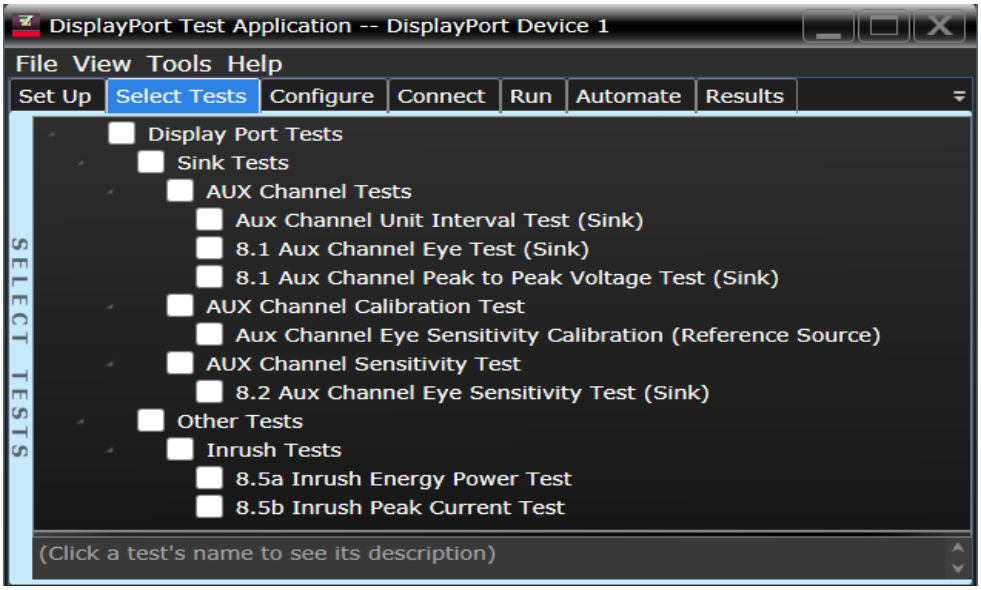
b define the number of waveforms to be saved in the **Number of Waveform:** field.

c Click the **Start Waveform Acquisition** button to start capturing and saving waveforms.

d Click **OK** to return to the **Set Up** tab.

10 Click the **Select Tests** tab where the AUX Channel tests for Source or Sink devices appear.





Probing/Connection Set Up for AUX Channel Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Compliance Test Application may prompt you to make/change the proper connections for certain type of tests. When performing the Source AUX Channel tests, a Reference Sink device is required. Similarly, when performing the Sink AUX Channel tests, a Reference Source device is required.

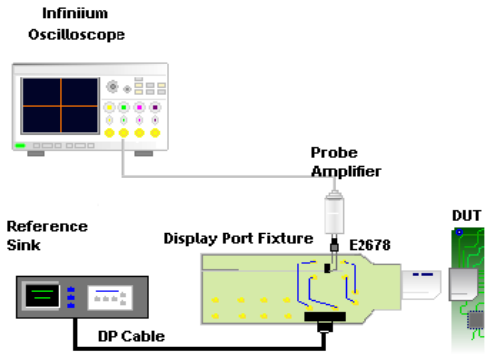


Figure 269 Sample connection diagram for source AUX channel tests with source DUT connected to a reference sink

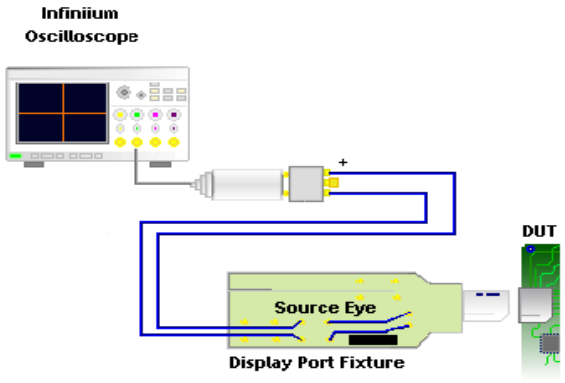


Figure 270 Sample connection diagram for source AUX channel tests without connecting to a reference sink

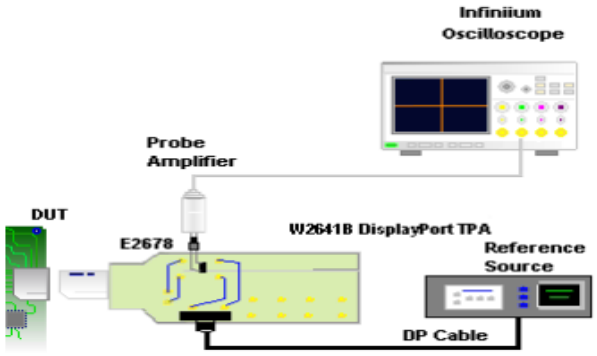


Figure 271 Sample connection diagram for sink AUX channel tests with sink DUT connected to a reference source

AUX Channel Unit Interval Test

Test ID

125000 – AUX Channel Unit Interval Test (Source)

125010 – AUX Channel Unit Interval Test (Sink)

Test Overview

The objective of the test is to evaluate the AUX Channel waveform, ensuring that the overall variation of the Manchester transaction Unit Interval stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Set up the parameter of the measurement trend:

   a Set up the Unit Interval measurement for the differential AUX Channel signal.

   b Set up the frequency measurement for the Clock signal.

   c Set up the measurement trend.

6 Set up the waveform Histogram on the measurement trend:

   a Initialize AUX Channel transactions and acquire the differential AUX Channel signal.

   b Identify the first and the last points for the desired transaction.

   c Zoom-in on the desired transaction.

   d Set up the Vertical Waveform Histogram on the measurement trend within the desired transaction.

   e Obtain the measurement for the mean, maximum and minimum values of the waveform Histogram.

7 Repeat step 6 ten times.

8 Report the measurement results.

PASS Condition

Manchester Transaction Unit Interval (UI_{MAN}):

Minimum = 0.4 µsec

Maximum = 0.6 µsec

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 2, Table 2-2*

Expected/Observable Results

The measured unit interval for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Test

Test ID

125001 – AUX Channel Eye Test (Source)

125011 – AUX Channel Eye Test (Sink)

Test Overview

The objective of this test is to evaluate the transmitter AUX Channel waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

7 Set up the waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

8 Set up the parameters for the Mask Test.

   a Load the eye mask based on the settings in the Configuration Variable.

   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

   c Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.

9 Check for any signal trajectories entering into the mask.

10 Report the measurement results.

PASS Condition

PASS Value = 290mV_diff_pp or higher

FAIL Value = lower than 290mV_diff_pp

Table 292 Eye Mask Vertices for AUX Channel for Manchester Transactions

Mask Point	Time (from EYE Center)	Minimum Voltage Value at Six Vertices (mV)
1	-185ns	0
2	-135ns	145
3	135ns	145
4	185ns	0
5	135ns	-145
6	-135ns	-145

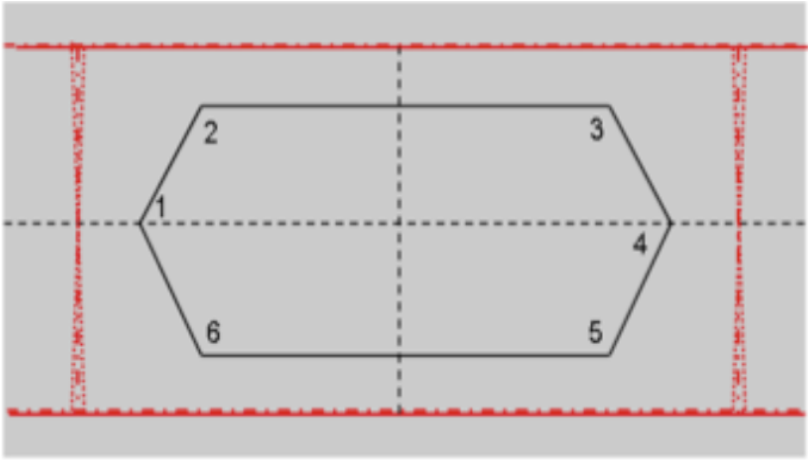


Figure 272 AUX Channel EYE Mask for Manchester Transactions

Mask Test: Zero mask failures.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.2*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 2, Table 2-1 and Table 2-2*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2.6, Figure 3-29 and Table 3-8*

Expected/Observable Results

The measured eye diagram for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

AUX Channel Peak-to-Peak Voltage Test

Test ID

125002 – AUX Channel Peak-to-Peak Voltage Test (Source)

125012 – AUX Channel Peak-to-Peak Voltage Test (Sink)

Test Overview

The objective of the test is to evaluate the transmitter AUX Channel Waveform, ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.
2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.
3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery.
5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.
6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.
8 If you have selected the “AUX Channel Eye Test” under the **Select Tests** tab of the compliance application:
   a Set up the parameter of the Mask Test:
      i Load the eye mask based on the settings in the Configuration Variable.
      ii Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.
      iii Initialize the AUX Channel transaction and run the eye mask until ten waveforms are folded.
   b Check for any signal trajectories entering into the mask.
9 Set up the waveform histogram on the AUX Channel eye diagram.
   a Set up the vertical waveform histogram on the AUX Channel eye diagram to measure the peak to peak voltage.
10 Report the measurement results.

PASS Condition

Table 293 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage at a transmitting device ($V_{AUX\text{-}DIFFp\text{-}p}$)	0.29V	1.38V

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 2, Table 2-1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured peak-to-peak voltage for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Calibration Test

Test ID

125021 – AUX Channel Eye Sensitivity Calibration (Reference Sink)

125031 – AUX Channel Eye Sensitivity Calibration (Reference Source)

Test Overview

The objective of this test is to calibrate the peak-to-peak voltage of the transmitter AUX Channel waveform by reference device (reference source or reference sink), ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.

2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

4 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

5 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

6 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

7 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

8 Set up the waveform Histogram on the AUX Channel eye diagram:

   a Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.

   b Set up the vertical waveform Histogram of width 0.6 UI at the center of the AUX Channel eye diagram.

   c Measure the V_{TOP} and V_{BASE} using the waveform Histogram mean value.

9 Repeat Step 8 three times.

10 Report the measurement results.

PASS Condition

Table 294 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage for AUX Channel Eye Sensitivity	0.24V	0.28V

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.2*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured peak-to-peak voltage for the AUX Channel signal by reference device (reference source or reference sink) shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Test

Test ID

125041 – AUX Channel Eye Sensitivity Test (Source)

125051 – AUX Channel Eye Sensitivity Test (Sink)

Test Overview

The objective of the test is to evaluate the sensitivity to the AUX Channel Eye Opening of the DUT as per the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.
2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.
3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery.
5 Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.
6 Check if the reference device could detect the transaction or not.
7 Decode the AUX Channel signal and check whether the transaction passed or failed.
8 Report the measurement results.

PASS Condition

Determine whether the AUX Channel communication is successful. For example, the Transmitter DUT sends an AUX Request to the Reference Receiver. The Reference Receiver acknowledges and the Transmitter DUT responds to the to indicate that the acknowledgment was successfully received.

PASS = No errors observed in the response

FAIL = One or more errors observed

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.2*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured AUX Channel transaction shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

39 SlimPort Inrush Tests

Overview

This section describes the normative and informative inrush tests for compliance verification of SlimPort source and sink, which is a power consumer.

Test Point

The test fixture for inrush tests implements the schematic shown in Figure 273.

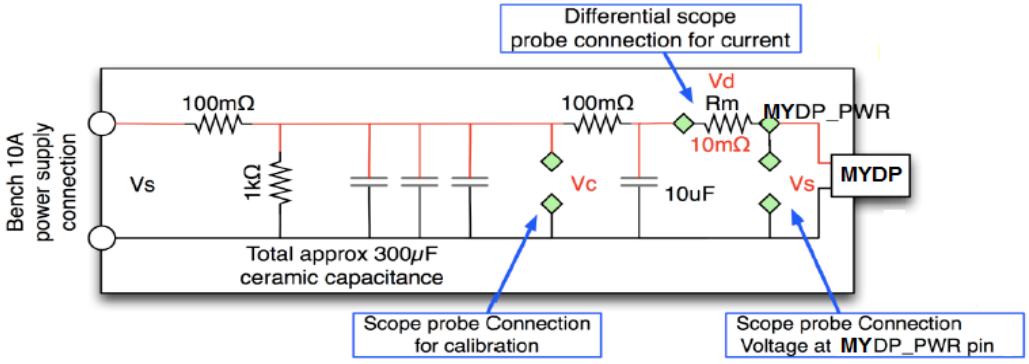


Figure 273 Schematics for testing a Power Consumer Device

The test fixture must be designed and used according to the following guidelines:

- A high gate voltage FET on the MyDP_PWR line is recommended to allow a fast connect capability, which allows a single connection event for testing. Without such an arrangement, multiple connections will be required to obtain a reasonable “worst-case” attachment event.
- Connection length between the power supply and the test fixture must be minimized. A maximum of four inches is recommended.
- The power supply must have enough outrush capability as to not negatively affect the test fixture’s outrush capability.
- The power supply must be run at 5.5V (5.0V + 10%) read across V_C.

Any Power Consumer test fixture must be calibrated using the Power User test fixture, as shown in Figure. Testing with the two fixtures combined should result in the approximate values given below. If required, the component values on the Power Consumer test fixture should be adjusted to match the expected results.

For Source:

- V_C steady before connection = 5.5V
- Inrush Current = ~9.0A

For Sink:

- V_C steady before connection = 3.6V
- Inrush Current = ~13.0A

Setting Up the DisplayPort Compliance Test Application for SlimPort Inrush Tests

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort Compliance Test Application" on page 79.

3 The **Set Up** tab on the DisplayPort Compliance Test Application is displayed by default (see Figure 6).

4 To test for compliance with DisplayPort SlimPort Standards, select the option **MyDP HBR25** in the **Test Specification** area.

5 Select the option **AUX PHY and Inrush Tests** in the **Test Selection** area.

6 If required, in the **DisplayPort Test Controller Setup** area, select the appropriate **DisplayPort Test Controller** from the drop-down options and click **Enable Automation** to activate the buttons required to connect and configure the selected DisplayPort Controller instrument.

7 Click the **Test Setup** button. On the **Test Setup** window, define the DUT parameters and test settings required to run the tests.

8 Once the Test Setup is complete, the **Connection Setup** button appears. Click this button to launch the **Connection Setup** window and to configure the fixture, probe and Oscilloscope Channel settings.

9 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

10 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

11 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

12 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

13 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the *Keysight D9040DPPC DisplayPort Compliance Test Application's Online Help* for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Refer to "Settings for AUX PHY and Inrush Tests" on page 1357 for instructions on setting the SlimPort InRush tests.

Inrush Energy Power Test

Test ID

127000 – Inrush Energy Power Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush energy power measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Current $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 9$ Amps

Test References

See:

For Source:

- *SlimPort Compliance Test Specification Version 1, Section 2.3*
- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.5*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 6*

For Sink:

- *SlimPort Compliance Test Specification Version 1, Section 5.2*
- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 3.4*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 6*

Expected/Observable Results

The measured worst case inrush energy power for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Inrush Peak Current Test

Test ID

127001 – Inrush Peak Current Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush peak current measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Current $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 9$ Amps

Test References

See:

For Source:

- *SlimPort Compliance Test Specification Version 1, Section 2.3*
- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.5*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 6*

For Sink:

- *SlimPort Compliance Test Specification Version 1, Section 5.2*
- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 3.4*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 6*

Expected/Observable Results

The measured worst case inrush peak current for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

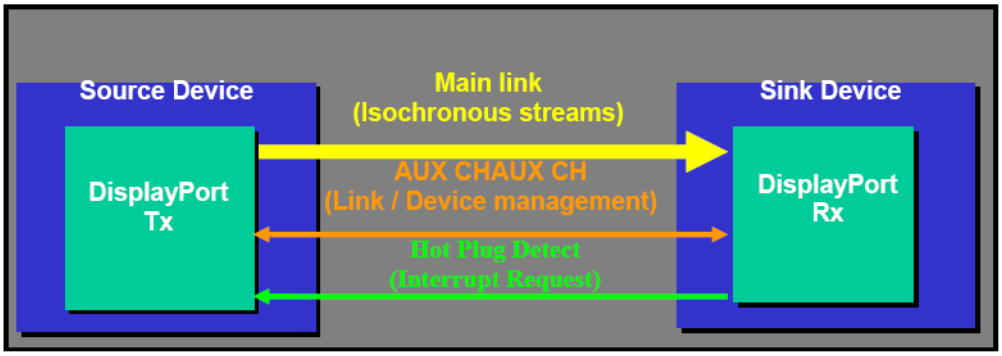
40 DisplayPort AUX Channel Cookbook for Tx Automated Test

This section describes what is required to implement the test automation features architected in the *DisplayPort Specification 1.1a*. Automated DisplayPort tests require a source device that is able to change test conditions such as data rate, level, pre-emphasis, test pattern, and SSC options as requested. This cookbook provides a guide on how to perform these tasks using a sink emulator such as Keysight W2642 DPTC controller.

AUX Channel and Hot Plug Detect (HPD)

DisplayPort devices communicate with each other through the AUX Channel. The DisplayPort port sink device provides memory that a source and a sink could read from or write to. The *DisplayPort Specification 1.1a* has reserved a set of DCPD registers for the purpose of test automation.

There is also a HPD line between a source and a sink. For automation purposes, the HPD pulse is used as an IRQ to notify the source about an automated test request.



DPTC Controller

The Keysight DPTC Controller can be used as a sink emulator that tells the source to output desired signals. Some fundamental functions provided which enable automation are:

- SetByte(Address, Value)
- Send HPDPulse(Length)
- PlugIn(Emulate Plug in event)
- PlugOut(Emulate Plug out event)

NOTE Function names listed are for informative purpose only. They are not reflected to actual API call.

Automated Test Sequence

This section provides information on how to enable test automation in DisplayPort Transmitter test. **You should specify the Max link rate, lane count, preEmphasis, Level, and SSC options from the compliance application.**

OPTION 1

Step 1: Emulate successful link training (For SSC)

1. This step emulates an unplug and plug in event to initiate a fake link training.
2. To do this, the DPTC controller initiates the sequence below:
   - *a* Emulate PlugOut Event to put HPD line in Low for at least 2 ms. Source should RESET.
   - *b* Set Link Capability fields.

     MAX_LINK_RATE = 0x0A.

     MAX_LANE_COUNT = 0x04.

     MAX_DOWNSPREAD = 0x01 to enable SSC / 0x00 to disable SSC.
   - *c* Set 0x202 (LANE0_1_STATUS) = 0x77.
   - *d* Set 0x203 (LANE2_3_STATUS) = 0x77.
   - *e* Set 0x204 (LANE_ALIGN__STATUS_UPDATED) = 0x81.
   - *f* Note: 0x202, 0x203 and 0x204 must be preset for automation purposes.
   - *g* Emulate PlugIn Event to put HPD line in High.
   - *h* Source clears Link Configuration field and reads Link Capability.
   - *i* Source enables/disables SSC based on the value of MAX_DOWNSPREAD (Enable SSC if value is 1).
   - *j* Source outputs 0x01 to TRAINING_PATTERN_SET.
   - *k* Source reads LANE0_1_STATUS, LANE2_3_STATUS and LANE_ALIGN__STATUS_UPDATED. Because these registers are already set in a previous step, the source exits the Clock Recovery Sequence for Link Training (Figure 274) and goes to the Channel Equalizer sequence for Link Training (Figure 275).
   - *l* Source set TRAINING_PATTERN_SET to 0x02.
   - *m* Source reads LANE0_1_STATUS, LANE2_3_STATUS and LANE_ALIGN__STATUS_UPDATED. Because these registers are already set in a previous step, the source exits the Channel Equalizer Sequence and ends the whole link training process.
3. From the state machine of link training of *Display Port Specification 1.1a*, these sequences cheat a Display Port source into thinking that link training has already been performed without looping through the actual link training. The Display Port Source device should exit link training successfully.
4. The AUX Controller then checks DOWNS_SPREAD_CTRL if SSC support is changed.

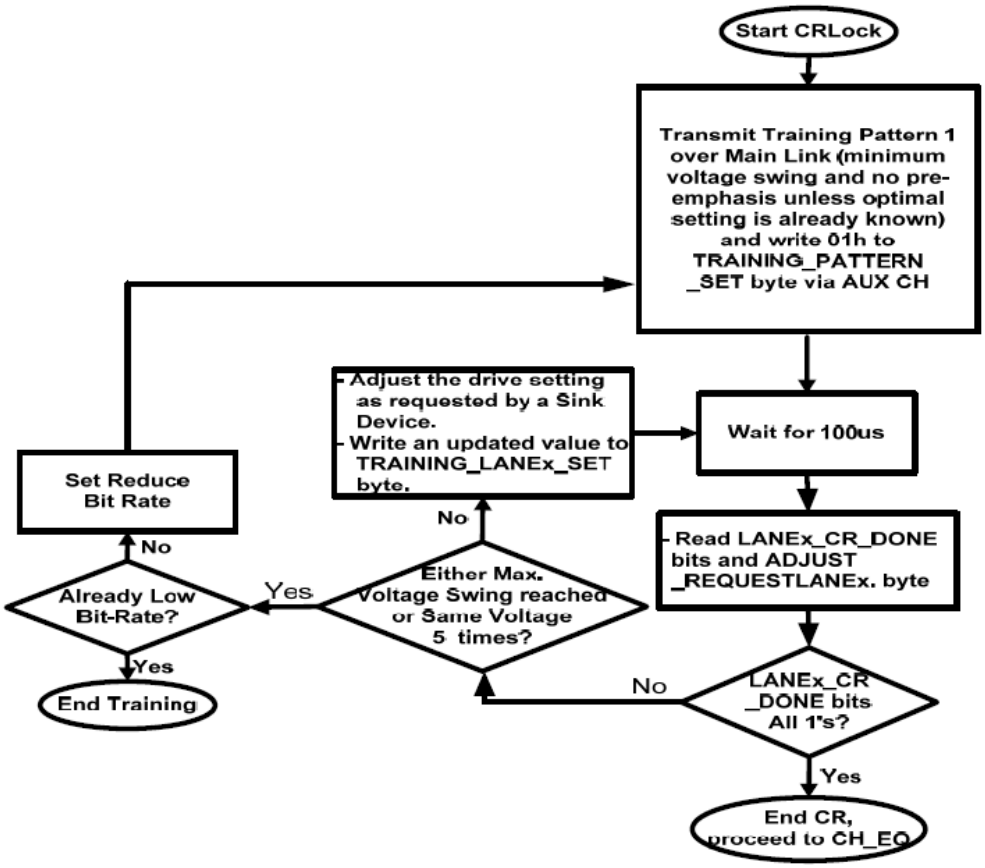


Figure 274 Clock Recovery Sequence

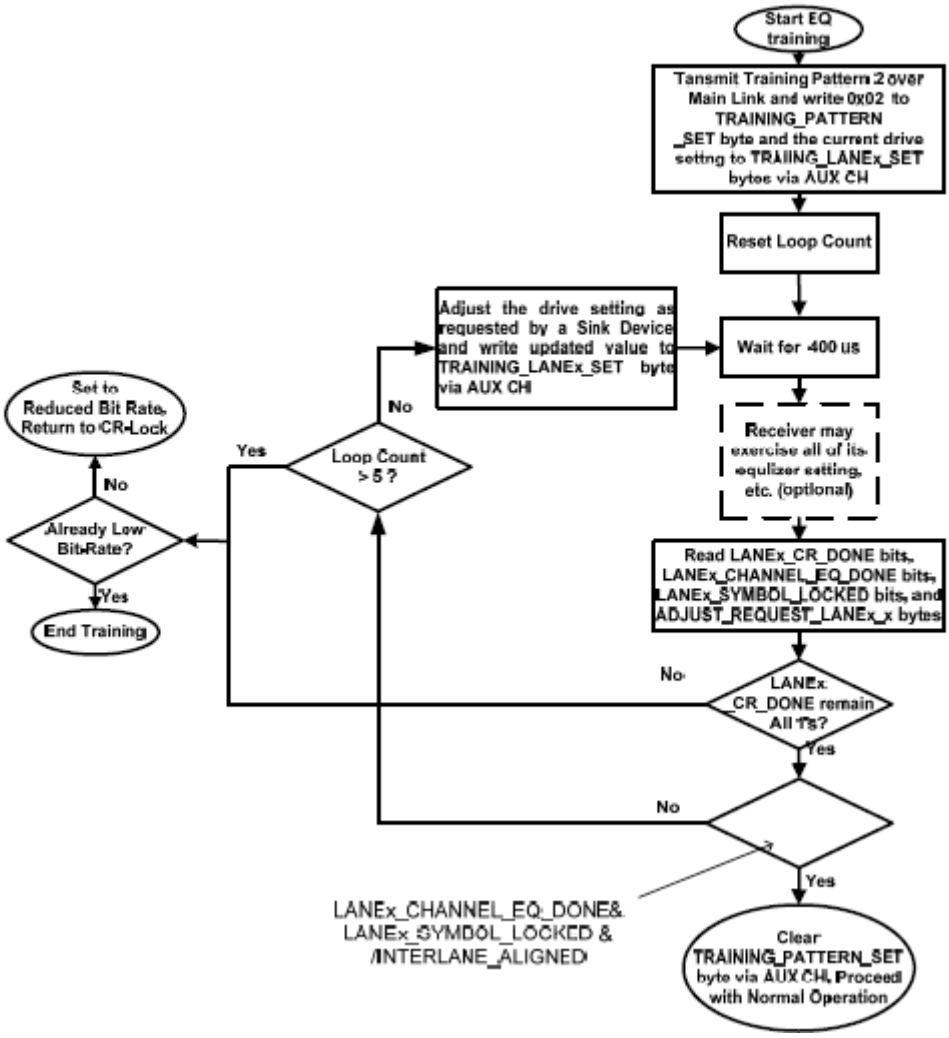


Figure 275 Clock Equalizer Sequence

Step 2: Change Bit Rate and Number of Lanes

1 To change the bit rate and Number of Lanes, the DPTC controller initiates the sequence below:

a Set 0x202 (LANE0_1_STATUS) = 0x77.

b Set 0x203 (LANE2_3_STATUS) = 0x77.

c Set 0x204 (LANE_ALIGN__STATUS_UPDATED) = 0x81.

d SetBit 0x201.1 (AUTOMATED_TEST_REQUEST).

e Clear 0x218 (TEST_REQUEST).

f SetBit 0x218.0 (TEST_LINK_TRAINING).

g SetByte 0x219 (TEST_LINK_RATE) to 0x0A (2.7 Gbps) or 0x06 (1.62 Gbps).

h SetByte 0x220 (TEST_LANE_COUNT) to the desired lane count.

i Trigger an IRQ Event (Send 1 ms HPD Pulse).

2 When a 1 ms HPD pulse is received:
   a Source reads bit 0x201.1 (AUTOMATED_TEST_REQUEST). If 0x201.1 is asserted go to 2.
   b If 0x218.0 is asserted, Source clears LINK_BW_SET and LANE_COUNT_SET.
   c Source reads 0x219 and 0x220 and output signals with desired lane count and data rate.

Step 3: Change PreEmphasis, Level, and Test pattern

1 To Change PreEmphasis, Level, and Test pattern, the DPTC initiates the following sequences:
   a Set 0x202 (LANE0_1_STATUS) = 0x77.
   b Set 0x203 (LANE2_3_STATUS) = 0x77.
   c Set 0x204 (LANE_ALIGN__STATUS_UPDATED) = 0x81.
   d SetBit 0x201.1 (AUTOMATED_TEST_REQUEST).
   e Set 0x206 (ADJUST_REQUEST_LANE0_1) and 0x207 (ADJUST_REQUEST_LANE2_3) with desired level and preemphasis.

Table 295 Mapping table for PreEmphasis and Level

VOLTAGE_SWING_LANEX (2 bits)	
00:	400 mV
01:	600 mV
10:	800 mV
11:	1200 mV

PREEMPHASIS_SWINT_LANEX (2 bits)	
00:	0 dB
01:	3.5 dB
10:	6 dB
11:	9.5 dB

   f Clear 0x218 and SetBit 0x218.3 (TEST_PATTERN_REQUEST).
   g Set 0x248 (PHY_TEST_PATTERN) to desired pattern.

Bits 1:0 = PHY_TEST_PATTERN_SEL	
00	= No test pattern selected
01	= D10.2 without scrambling
10	= Symbol_Error_Measurement_Count
11	= PRBS7V

   h Send IRQ to source (HPD 1 ms Pulse).

2 When a 1 ms HPD pulse is received:
   a Source reads bit 0x201.1 (AUTOMATED_TEST_REQUEST). If 0x201.1 is asserted, go to step 2.
   b Source reads 0x248, 0x206, 0x207 and outputs signals with desired pattern, PreEmphasis, and Level.

NOTE It might be necessary to repeat step 3 to set TEST_PATTERN back to “No pattern” (0x248=0h) before repeating whole automation sequence (step 1 to 3).

OPTION 2

This option provides a simple way to control test automation in one simple step, providing that a test mode is supplied. However, it is less consistent with DisplayPort Automation scheme.

Step 1:

1 Source should always Scan for 0x201.1 (AUTOMATED_TEST_REQUEST).
2 Sink sets the following:
   a SetByte 0x219 (TEST_LINK_RATE) to (2.7 Gbps) or 0x06 (1.62 Gbps)
   b SetBit 0x03.1 (TEST_DOWNSPREAD) to turn on SSC. Clear 0x21A.1 to turn off SSC.
   c SetByte 0x220 (TEST_LANE_COUNT) to desired lane count.
   d Set 0x206 (ADJUST_REQUEST_LANE0_1) and 0x207 (ADJUST_REQUEST_LANE2_3) with desired level and preemphasis.
   e Set 0x248 (PHY_TEST_PATTERN) to desired pattern.
3 Sink sets 0x201.1.
4 When the Source detects 0x201.1 being set, it should respond by outputting signals as in step 2.
5 Sink wait for 3 seconds.
6 Sink set bit 0x218.0 back to 0.
7 Alternatively, HPD_IRQ (1 ms) mechanism could be used instead of keep scanning 0x201.1.

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