D9040DDRC DDR4 and LPDDR4 Test Application - Methods of Implementation

KEYSIGHT

METHODS OF IMPLEMENTATION

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SW Version

Version 3.90.0.0

Edition

January 2024

Available in electronic format only

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Contents

1 Overview

DDR4 Automated Testing—At a Glance

The Keysight DDR4 Test Application helps you verify compliance of the SDRAM types (DDR4, LPDDR4 and LPDDR4X (Differential and Single-ended)) to the respective JEDEC specifications using Keysight Infiniium Oscilloscopes. The Keysight DDR4 Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE **The tests performed by the Keysight DDR4 Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.**

For each SDRAM type being tested, you may refer to the following specification documents for compliance testing measurements. For more information, see the JEDEC website: https://www.jedec.org/.

SDRAM Type	Reference Documents
DDR4	JEDEC Standard, DDR4 SDRAM, JESD79-4D, July 2021 (Revision of JESD79-4C, January 2020)
LPDDR4	JEDEC Standard, Low Power Double Date Rate 4 (LPDDR4), JESD209-4D, June 2021 (Revision of JESD209-4C, November 2019)
LPDDR4X	JEDEC Standard, Addendum No. 1 to JESD209-4 -1 Low Power Double Data Rate 4X (LPDDR4X), JESD209-4-1, January 2017 (Revision of JESD209-4A, November 2015) LPDDR4X single-ended mode for Clock and Strobe, JEDEC JC-42.6-1847.17, November 2017 LPDDR4X CK and DQS single-ended mode DQ & CA Rx parameters, JEDEC JC-42.6 TG426_1, December 2017

Required Equipment and Software

In order to run the DDR4/LPDDR4/LPDDR4X automated tests, you need the following equipment and software:

Hardware

- Use one of the following Oscilloscope models. Refer to www.keysight.com for the respective bandwidth ranges.
  - Keysight DSO9000A-Series, DSO90000A-Series and DSOX90000A/Q/Z/V-Series Oscilloscopes with a minimum bandwidth of 8GHz (recommended) for accurate measurements. For faster speed grade devices, a minimum bandwidth of 13GHz bandwidth is recommended.
  - Keysight UXR Oscilloscopes
  - Keysight MXR Oscilloscopes
- Any PC motherboard system that supports DDR4 memory DIMM(s)
- DUT: Saved waveform and PulseGen generated signal
- InfiniiMax probe amplifiers:
  - N1169A – 12GHz InfiniiMax II probe amplifier
  - MX0020A - 10GHz InfiniiMax Ultra Probe Amplifier
  - MX0021A - 13GHz InfiniiMax Ultra Probe Amplifier
  - MX0022A - 16GHz InfiniiMax Ultra Probe Amplifier
  - MX0023A - 25GHz InfiniiMax RC Probe Amp
  - MX0024A - 20GHz InfiniiMax Ultra Probe Amplifier
  - MX0025A - 25GHz InfiniiMax Ultra Probe Amplifier
- InfiniiMax probe heads – InfiniiMax II probe heads and accessories (compatible with 9000 Series and 90000 Series, use N5442A precision BNC adapter with 90000X/Q Series):
  - N5381A – InfiniiMax II 12GHz differential solder-in probe head and accessories
  - N5382A – InfiniiMax II 12GHz differential browser
  - E2677A – InfiniiMax II 12GHz differential solder-in probe head and accessories
  - N5425A – InfiniiMax II 12GHz ZIF probe head
  - N5426A – InfiniiMax II ZIF tips (×10)
- InfiniiMax Ultra/RC Probe Amplifiers probe heads and accessories:
  - MX0100A - InfiniiMax Micro Probe Head
  - MX0103A - Bullet Adapter
- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Precision 3.5 mm BNC to SMA male adapter, Keysight p/n 54855-67604, qty = 2 (provided with the Keysight 54855A and 80000B series oscilloscopes)
- 50-ohm Coax Cable with SMA Male Connectors – 24-inch or less RG-316/U or similar, qty = 2, matched length
- Keysight also recommends using a second monitor to view the test application.

Software

- The minimum version of Infiniium Oscilloscope Software (see the Keysight DDR4 Test Application Release Notes)
- Keysight DDR4 Test Application software

- Keysight E2688A Serial Data Analysis and Clock Recovery software (for clock recovery)

NOTE

You may configure and run DDR4 tests using the *Advanced Design System (ADS) 2019 Update 1* (or higher) software, which invokes the Keysight DDR4 Test Application remotely on the offline version of the N8900A Infiniium Application to run one or more tests.

For more information on how to use the ADS software along with the Keysight DDR4 Test Application, refer to the *Memory Designer* documentation in the *ADS 2019 Update 1 User Guide*.

Licensing information

Refer to the *Data Sheet* pertaining to Keysight DDR4 Test Application to know about the licenses you must install along with other optional licenses. Visit "http://www.keysight.com/find/D9040DDRC" and in the web page's **Document Library** tab, you may view the associated Data Sheet.

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

The licensing format for Keysight License Manager 6 differs from its predecessors. See "Installing the License Key" on page 15 to see the difference in installing a license key using either of the applications on your machine.

In This Book

This manual describes the tests that are performed by the Keysight DDR4 Test Application in more detail; it contains information from (and refers to) various DDR4/LPDDR4/LPDDR4X specifications and it describes how the tests are performed.

- Chapter 1, “Overview” shows how to install and license the automated test application (if it was purchased separately).
- Chapter 2, “Installing the Test Application and Licenses” explains how to obtain the installer for the automated test application and install the associated licenses (if it was purchased separately).
- Chapter 3, “Preparing to Take Measurements” describes how to launch the Keysight D9040DDRC DDR4 and LPDDR4 Test Application and gives a brief overview of how it is used.
- Chapter 4, “Electrical Tests” describes the methods of implementation for WRITE and READ cycle electrical tests performed on DDR4/LPDDR4/LPDDR4X devices.
- Chapter 5, “Timing Tests” describes the methods of implementation for timing tests performed on DDR4/LPDDR4/LPDDR4X devices.
- Chapter 6, “Eye Diagram Tests” describes the methods of implementation for eye diagram tests performed on DDR4/LPDDR4/LPDDR4X devices.
- Appendix A, “References” provides certain references from the specifications for DDR4/LPDDR4/LPDDR4X devices.

See Also

The Keysight DDR4 Test Application’s Online Help, which describes:

- Starting the DDR4 Test Application
- Creating or Opening a Test Project
- Setting Up the Test Environment
- Selecting Tests
- Configuring Tests
- Verifying Physical Connections
- Running Tests
- Configuring Automation in the Test Application
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
- Additional Settings in the Test App

2 Installing the Test Application and Licenses

If you purchased the D9040DDRC DDR4 Test Application separate from your Infiniium oscilloscope, you must install the software and license key.

Installing the Test Application

1. Make sure you have the minimum version of Infiniium Oscilloscope software (see the D9040DDRC release notes). To ensure that you have the minimum version, select **Help > About Infiniium...** from the main menu.
2. To obtain the DDR4 Test Application, go to Keysight website: "http://www.keysight.com/find/D9040DDRC".
3. In the web page's **Trials & Licenses** tab, click the **Details and Download** button to view instructions for downloading and installing the application software.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

1 Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.

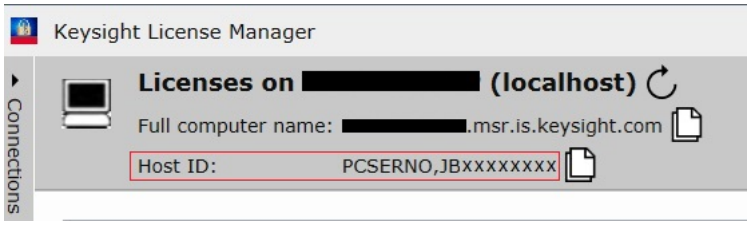


Figure 1 Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager.

3 From the configuration menu, use one of the options to install each license file.

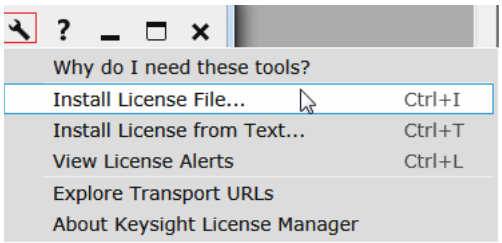


Figure 2 Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

1 Launch Keysight License Manager 6 on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID, which is the first set of alphanumeric value (as highlighted in Figure 3) that appears in the Environment tab of the application. Note that x indicates numeric values.

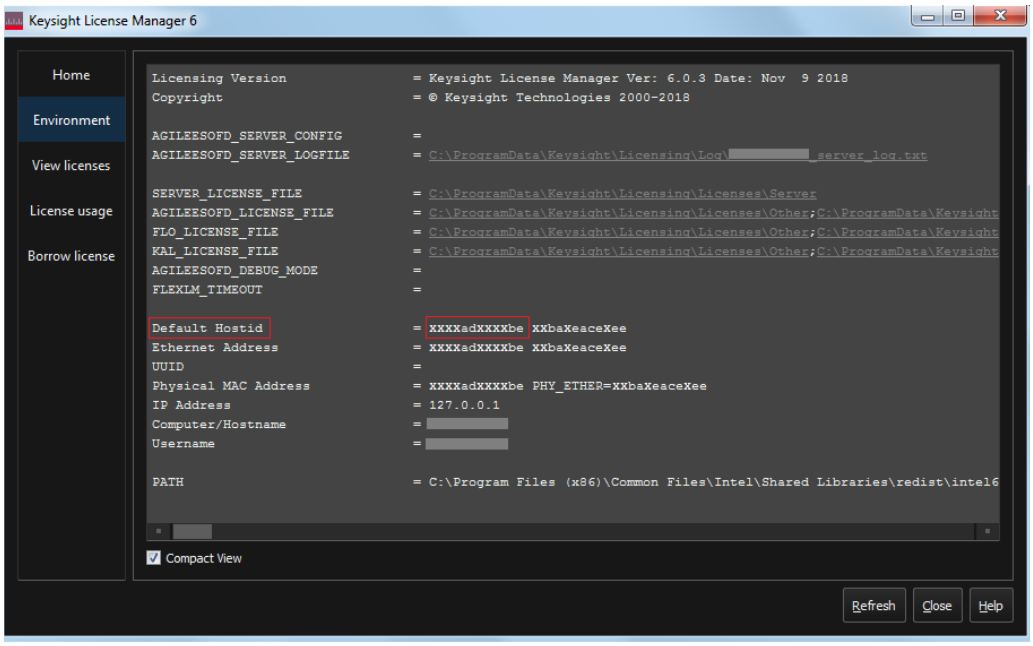


Figure 3 Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager 6.

3 From the Home tab, use one of the options to install each license file.

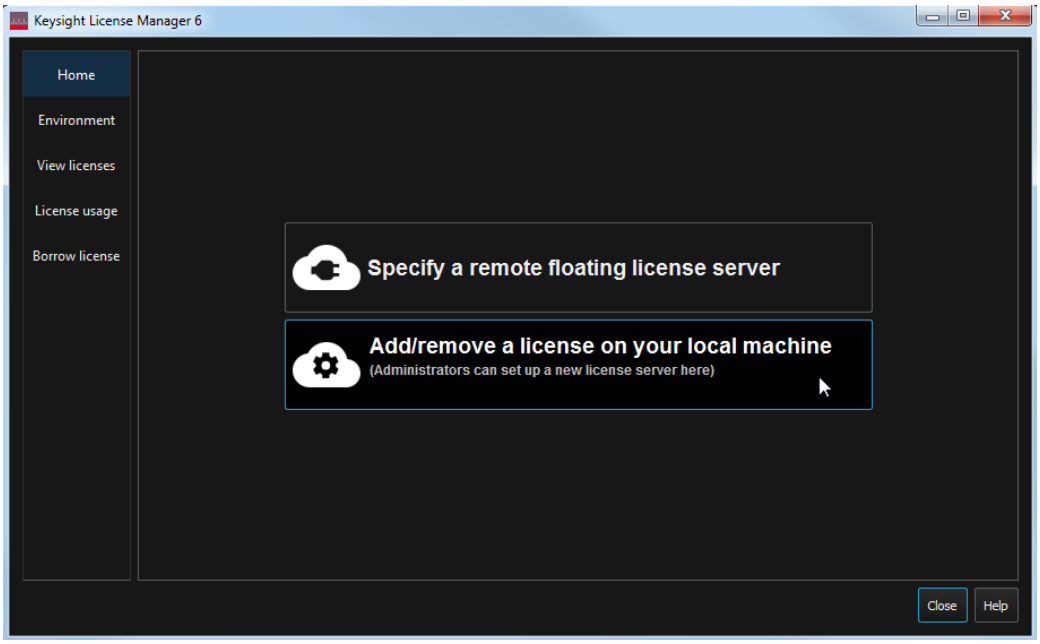


Figure 4 Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

3 Preparing to Take Measurements

Before running the automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this application. After the oscilloscope and probe have been calibrated, you are ready to start the DDR4 Test Application and perform the measurements.

Calibrating the Oscilloscope

If you have not already calibrated the oscilloscope, refer to the *User Guide* for the respective oscilloscope you are using.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

NOTE If the test signal falls outside the probe linear input range (that is, the dynamic range of the probe), the acquired signal may be clipped and the oscilloscope screen may not display the signal accurately during measurements. For more information regarding these settings, refer to the *Probe Linear Input Range* section in the Help manuals provided with the Infiniium oscilloscope you are using.

Starting the DDR4 Test Application

1 Ensure that the DDR4 Device Under Test (DUT) is operating and set to desired test modes. To start the DDR4 Test Application: From the Infiniium Oscilloscope's main menu, select **Analyze > Automated Test Apps > D9040DDRC DDR4 Test App**.

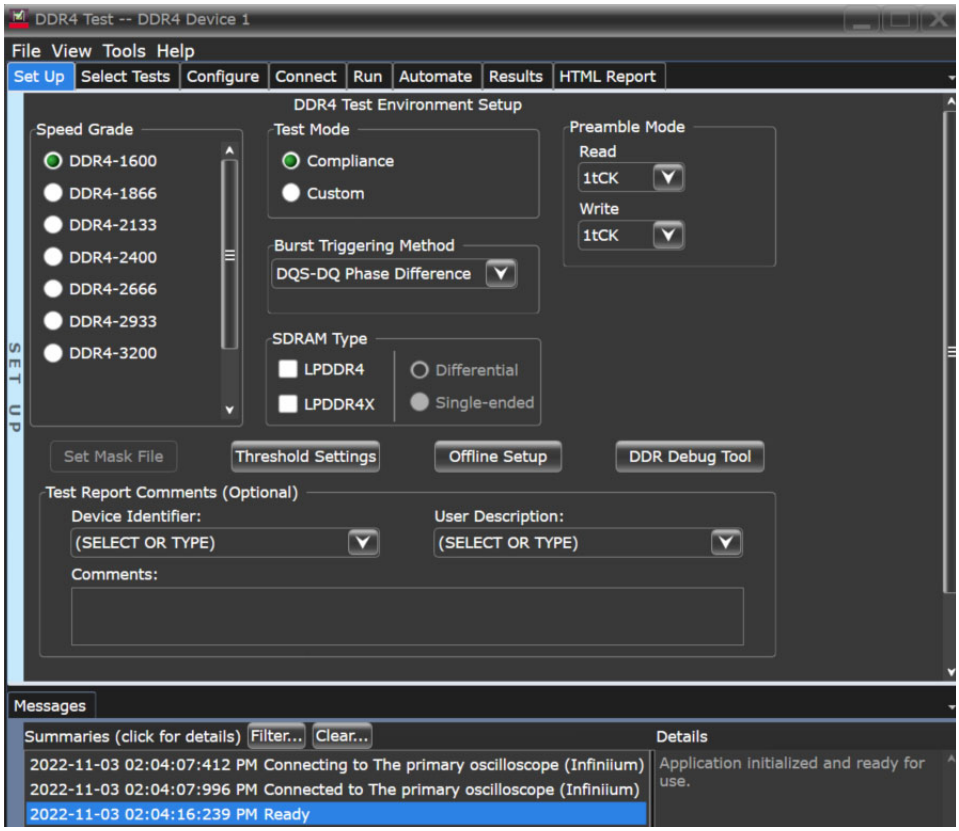


Figure 5 DDR4 Test Application default view after launch

To understand the functionality of the various features in the user interface of the Test Application, refer to the Keysight *D9040DDRC DDR4 Test Application Online Help* available in the Help menu.

The task flow pane and the tabs in the main pane show the steps you take in running the automated tests:

Tab	Description
Set Up	Lets you identify and set up the test environment, including information about the device under test. The Test App includes relevant information in the final HTML report.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (for example, channels used in test, voltage levels, etc.).
Connect	Shows you how to connect the oscilloscope to the device under test for the tests that are to be run.
Run	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automate	Lets you construct scripts of commands that drive execution of the application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE

In the **Configure** tab, the values for all such Configuration parameters that are oscilloscope-dependent, will correspond to the oscilloscope Model (DSOs or UXRs), where you are running the Test Application.

Configuring DQS Signal Type in Custom Test Mode

Some of the tests in the **Select Tests** tab of the DDR4 Compliance Test Application appear only when the **Test Mode** is selected as **Custom**. However, prior to running such tests, you must ensure that properties associated with the DQS test signal are configured properly under the **Set Up** tab. Figure 6 shows the features that appear when **Custom** is selected.

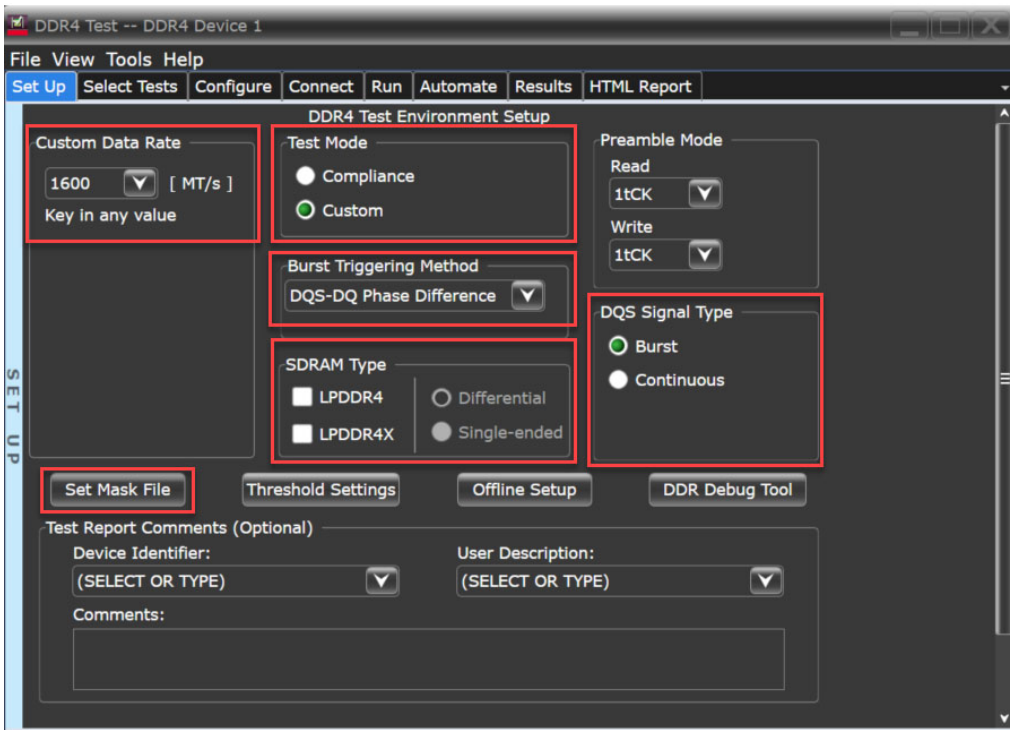


Figure 6 Configuration options under Set Up tab for Custom Test Mode

For accurate results, ensure that the following features are configured properly:

- **Custom Data Rate**—the value entered here must match the data rate of the DQS test signal.
- **DQS Signal Type**—select **Burst** to indicate whether the DQS test signal consists of READ/WRITE bursts or select **Continuous** if the test DQS test signal is continuous (having no bursts).
- **Burst Triggering Method**—all options for the selected SDRAM Type are available under Burst Triggering Method when **DQS Signal Type** is **Burst**. However, for **Continuous**, only the *Rd or Wrt Only* method for Burst Triggering is available, irrespective of the SDRAM Type selected.
- **Set Mask File**—the correct test mask file must be selected for Eye diagram tests.
- **SDRAM Type** —The differential and single-ended options are available only after you select LPDDR4X.

Support for 2tCK Preamble length

According to *JEDEC Standard, DDR4 SDRAM, JESD79-4D, July 2021 (Revision of JESD79-4C, January 2020)*, the DQS preamble in DDR4 can be programmed to either 1tCK or 2tCK read / write preamble. Refer to Figures 75 and 79 in the JESD79-4D document for the definition of 1tCK and 2tCK Write and Read Preamble, respectively, in DDR4 DQS signals.

As shown in Figure 7, the **Preamble Mode** feature in the DDR4 Test Application enables configuration of read / write cycle of the DQS signal with a preamble length of either 1tCK or 2tCK for specific DDR4 tests.

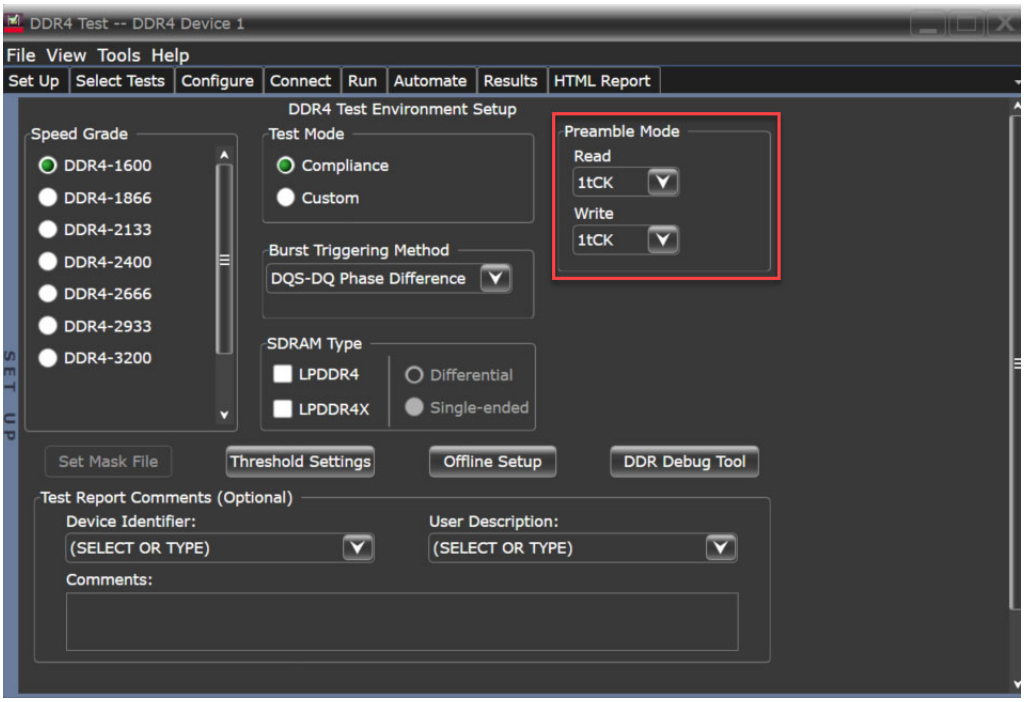


Figure 7 Preamble Mode configuration option for certain DDR4 tests only

4 Electrical Tests

Overview

The following group of tests pertains to the electrical operating conditions of a DDR4, LPDDR4 or LPDDR4X SDRAM as defined in JEDEC specifications. The tests are further divided into Single-Ended Signals Tests and Differential Signals Tests.

Single-Ended Signals (WRITE cycle tests)

Clocks Plus Tests

VSEH(Clock Plus)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

10333 [VSEH(Clock Plus)]

LPDDR4 Test Mode

50333 [VSEH(Clock Plus)]

LPDDR4X (Differential) Test Mode

60333 [VSEH(Clock Plus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.3	Table 124	VSEH [Single-ended high-level for CK_t - CK_c]

LPDDR4 / LPDDR4X (Differential) Test Modes

There is no reference available for this test in the JEDEC specifications. The measurement result is reported as “Information Only”.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the maximum voltage of high pulse.

LPDDR4 / LPDDR4X (Differential) Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 10333)**

1 Pre-condition the oscilloscope.
2 Trigger on the rising edge of the clock signal under test.
3 Find all valid Clock positive pulse in the entire waveform.
A valid Clock positive pulse starts at Half_V_{DD} crossing at valid Clock rising edge and ends at Half_V_{DD} crossing at the following valid Clock falling edge.
4 Zoom into the first pulse and perform T_{MAX}.
   a Perform V_{TIME} with the T_{MAX} obtained in the previous step to obtain the maximum voltage of the pulse.
   b Take the V_{TIME} measurement as the value of V_{SEH}.
5 Continue the previous step with the rest of the positive pulses found in the specified waveform.
6 Determine the worst result from the set of V_{SEH} measured.

LPDDR4 (for Test ID 50333) / LPDDR4X (Differential) (for Test ID 60333)

1 Pre-condition the oscilloscope.
2 Trigger on the rising edge of the clock signal under test.

3 Find all valid Clock positive pulse in the entire waveform.
A valid Clock positive pulse starts at Half_V_{DD2} crossing at valid Clock rising edge and ends at Half_V_{DD2} crossing at the following valid Clock falling edge.

4 Zoom into the first pulse and perform T_{MAX}.

   a Perform V_{TIME} with the T_{MAX} obtained in the previous step to obtain the maximum voltage of the pulse.

   b Take the V_{TIME} measurement as the value of V_{SEH}.

5 Continue the previous step with the rest of the positive pulses found in the specified waveform.

6 Determine the worst result from the set of V_{SEH} measured.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of V_{SEH} for the test signal is reported as “Information Only”.

VSEL(Clock Plus)

Test Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

10334 [VSEL(Clock Plus)]

LPDDR4 Test Mode

50334 [VSEL(Clock Plus)]

LPDDR4X (Differential) Test Mode

60334 [VSEL(Clock Plus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.3	Table 124	VSEL [Single-ended low-level for CK_t - CK_c]

LPDDR4 / LPDDR4X (Differential) Test Modes

There is no reference available for this test in the JEDEC specifications. The measurement result is reported as “Information Only”.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the minimum voltage of low pulse.

LPDDR4 / LPDDR4X (Differential) Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 10334)**

1 Pre-condition the oscilloscope.
2 Triggered on falling edge of the clock signal under test.
3 Find all valid Clock negative pulse in the entire waveform.
A valid Clock negative pulse starts at Half_V_{DD} crossing at valid Clock falling edge and end at Half_V_{DD} crossing at following valid Clock rising edge.
4 Zoom into the first pulse and perform T_{MIN}.
   a Perform V_{TIME} with the T_{MIN} obtained in the previous step to obtain the minimum voltage of the pulse.
   b Take the V_{TIME} measurement as the value of V_{SEL}.
5 Continue the previous step with the rest of the negative pulses found in the specified waveform.
6 Determine the worst result from the set of V_{SEL} measured.

LPDDR4 (for Test ID 50334) / LPDDR4X (Differential) (for Test ID 60334)

1 Pre-condition the oscilloscope.
2 Triggered on falling edge of the clock signal under test.
3 Find all valid Clock negative pulse in the entire waveform.
A valid Clock negative pulse starts at Half_V_{DD2} crossing at valid Clock falling edge and ends at Half_V_{DD2} crossing at following valid Clock rising edge.

4 Zoom into the first pulse and perform T_{MIN}.

a Perform V_{TIME} with the T_{MIN} obtained in the previous step to obtain the minimum voltage of the pulse.

b Take the V_{TIME} measurement as the value of V_{SEL}.

5 Continue the previous step with the rest of the negative pulses found in the specified waveform.

6 Determine the worst result from the set of V_{SEL} measured.

Expected/ Observable Results:

DDR4 / LPDDR4 LPDDR4X (Differential) Test Mode

The measured value of V_{SEL} for the test signal is reported as “Information Only”.

Vinse_CK_High(Clock Plus)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

50339 [Vinse_CK_High(Clock Plus)]

LPDDR4X (Differential) Test Mode

60339 [Vinse_CK_High(Clock Plus)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.3	Table 188	Vinse_CK_High [Clock Single-Ended input voltage High from VREFDQ]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the peak voltage of high pulse.

Test Procedure: **LPDDR4 (for Test ID 50339) / LPDDR4X (Differential) (for Test ID 60339)**

1 Pre-condition the oscilloscope.
2 Trigger on the rising edge of the clock signal under test.
3 Find all valid positive pulses of the Clock in the entire waveform.
A valid positive pulse on the Clock starts at the valid rising edge of the Clock and ends at the following valid falling edge of the Clock.
4 Zoom into the first pulse and measure V_{MAX}.
5 Calculate the value of Vinse_CK_High(Clock Plus) using the equation:

$$\text{Vinse\_CK\_High(Clock Plus)} = V_{MAX} - \text{VREFCA}$$

6 Continue the previous step with the rest of the positive pulses found in the specified waveform.
7 Determine the worst result from the set of Vinse_CK_High measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vinse_CK_High for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_CK_Low(Clock Plus)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

50340 [Vinse_CK_Low(Clock Plus)]

LPDDR4X (Differential) Test Mode

60340 [Vinse_CK_Low(Clock Plus)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.3	Table 188	Vinse_CK_Low [Clock Single-Ended input voltage Low from VREFDQ]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the peak voltage of low pulse.

Test Procedure: **LPDDR4 (for Test ID 50340) / LPDDR4X (Differential) (for Test ID 60340)**

1 Pre-condition the oscilloscope.
2 Trigger on the falling edge of the clock signal under test.
3 Find all valid negative pulses of the Clock in the entire waveform.
A valid negative pulse on the Clock starts at the valid falling edge of the Clock and ends at the following valid rising edge of the Clock.
4 Zoom into the first pulse and measure V_{MIN}.
5 Calculate the value of Vinse_CK_Low(Clock Plus) using the equation:
6 Vinse_CK_Low(Clock Plus) = VREFCA - V_{MIN}
7 Continue the previous step with the rest of the negative pulses found in the specified waveform.
8 Determine the worst result from the set of Vinse_CK_Low measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vinse_CK_Low for the test signal shall be within the conformance limits as per the JEDEC specification.

Clocks Minus Tests

VSEH(Clock Minus)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential Only)

Test ID: **DDR4 Test Mode**

10337 [VSEH(Clock Minus)]

LPDDR4 Test Mode

50337 [VSEH(Clock Minus)]

LPDDR4X (Differential) Test Mode

60337 [VSEH(Clock Minus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.3	Table 124	VSEH [Single-ended high-level for CK_t - CK_c]

LPDDR4 / LPDDR4X (Differential) Test Modes

There is no reference available for this test in the JEDEC specifications. The measurement result is reported as “Information Only”.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the maximum voltage of high pulse.

LPDDR4 / LPDDR4X (Differential) Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 10337)**

1 Pre-condition the oscilloscope.
2 Trigger on the rising edge of the clock signal under test.
3 Find all valid Clock positive pulse in the entire waveform.
A valid Clock positive pulse starts at Half_V_{DD} crossing at valid Clock rising edge and ends at Half_V_{DD} crossing at the following valid Clock falling edge.
4 Zoom into the first pulse and perform T_{MAX}.
   a Perform V_{TIME} with the T_{MAX} obtained in the previous step to obtain the maximum voltage of the pulse.
   b Take the V_{TIME} measurement as the value of V_{SEH}.
5 Continue the previous step with the rest of the positive pulses found in the specified waveform.
6 Determine the worst result from the set of V_{SEH} measured.

LPDDR4 (for Test ID 50337) / LPDDR4X (Differential) (for Test ID 60337)

1 Pre-condition the oscilloscope.
2 Trigger on the rising edge of the clock signal under test.
3 Find all valid Clock positive pulse in the entire waveform.
A valid Clock positive pulse starts at Half_V_{DD2} crossing at valid Clock rising edge and ends at Half_V_{DD2} crossing at the following valid Clock falling edge.

4 Zoom into the first pulse and perform T_{MAX}.

a Perform V_{TIME} with the T_{MAX} obtained in the previous step to obtain the maximum voltage of the pulse.

b Take the V_{TIME} measurement as the value of V_{SEH}.

5 Continue the previous step with the rest of the positive pulses found in the specified waveform.

6 Determine the worst result from the set of V_{SEH} measured.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of V_{SEH} for the test signal is reported as “Information Only”.

VSEL(Clock Minus)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

10338 [VSEL(Clock Minus)]

LPDDR4 Test Mode

50338 [VSEL(Clock Minus)]

LPDDR4X (Differential) Test Mode

60338 [VSEL(Clock Minus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.3	Table 124	VSEL [Single-ended low-level for CK_t - CK_c]

LPDDR4 / LPDDR4X (Differential) Test Modes

There is no reference available for this test in the JEDEC specifications. The measurement result is reported as “Information Only”.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the minimum voltage of low pulse.

LPDDR4 / LPDDR4X (Differential) Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 10338)**

1 Pre-condition the oscilloscope.
2 Triggered on falling edge of the clock signal under test.
3 Find all valid Clock negative pulse in the entire waveform.
A valid Clock negative pulse starts at Half_V_{DD} crossing at valid Clock falling edge and end at Half_V_{DD} crossing at following valid Clock rising edge.
4 Zoom into the first pulse and perform T_{MIN}.
   a Perform V_{TIME} with the T_{MIN} obtained in the previous step to obtain the minimum voltage of the pulse.
   b Take the V_{TIME} measurement as the value of V_{SEL}.
5 Continue the previous step with the rest of the negative pulses found in the specified waveform.
6 Determine the worst result from the set of V_{SEL} measured.

LPDDR4 (for Test ID 50338) / LPDDR4X (Differential) (for Test ID 60338)

1 Pre-condition the oscilloscope.
2 Triggered on falling edge of the clock signal under test.
3 Find all valid Clock negative pulse in the entire waveform.
A valid Clock negative pulse starts at Half_V_{DD2} crossing at valid Clock falling edge and ends at Half_V_{DD2} crossing at following valid Clock rising edge.

4 Zoom into the first pulse and perform T_{MIN}.

a Perform V_{TIME} with the T_{MIN} obtained in the previous step to obtain the minimum voltage of the pulse.

b Take the V_{TIME} measurement as the value of V_{SEL}.

5 Continue the previous step with the rest of the negative pulses found in the specified waveform.

6 Determine the worst result from the set of V_{SEL} measured.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of V_{SEL} for the test signal is reported as “Information Only”.

Vinse_CK_High(Clock Minus)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

50341 [Vinse_CK_High(Clock Minus)]

LPDDR4X (Differential) Test Mode

60341 [Vinse_CK_High(Clock Minus)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.3	Table 188	Vinse_CK_High [Clock Single-Ended input voltage High from VREFDQ]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the peak voltage of high pulse.

Test Procedure: **LPDDR4 (for Test ID 50341) / LPDDR4X (Differential) (for Test ID 60341)**

1 Pre-condition the oscilloscope.
2 Trigger on the rising edge of the clock signal under test.
3 Find all valid positive pulses of the Clock in the entire waveform.
A valid positive pulse on the Clock starts at the valid rising edge of the Clock and ends at the following valid falling edge of the Clock.
4 Zoom into the first pulse and measure V_{MAX}.
5 Calculate the value of Vinse_CK_High(Clock Minus) using the equation:

$$\text{Vinse\_CK\_High(Clock Minus)} = V_{MAX} - \text{VREFCA}$$

6 Continue the previous step with the rest of the positive pulses found in the specified waveform.
7 Determine the worst result from the set of Vinse_CK_High measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vinse_CK_High for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_CK_Low(Clock Minus)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

50342 [Vinse_CK_Low(Clock Minus)]

LPDDR4X (Differential) Test Mode

60342 [Vinse_CK_Low(Clock Minus)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.3	Table 188	Vinse_CK_Low [Clock Single-Ended input voltage Low from VREFDQ]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the peak voltage of low pulse.

Test Procedure: **LPDDR4 (for Test ID 50342) / LPDDR4X (Differential) (for Test ID 60342)**

1 Pre-condition the oscilloscope.
2 Trigger on the falling edge of the clock signal under test.
3 Find all valid negative pulses of the Clock in the entire waveform.
A valid negative pulse on the Clock starts at the valid falling edge of the Clock and ends at the following valid rising edge of the Clock.
4 Zoom into the first pulse and measure V_{MIN}.
5 Calculate the value of Vinse_CK_Low(Clock Minus) using the equation:

$$\text{Vinse\_CK\_Low(Clock Minus)} = \text{VREFCA} - V_{MIN}$$

6 Continue the previous step with the rest of the negative pulses found in the specified waveform.
7 Determine the worst result from the set of Vinse_CK_Low measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vinse_CK_Low for the test signal shall be within the conformance limits as per the JEDEC specification.

Clock Tests

Vinse_CK

Mode Supported: LPDDR4X (Single-Ended only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

Not available.

LPDDR4X (Differential) Test Mode

Not available.

LPDDR4X (Single-ended) Test Mode

70343 [Vinse_CK]

References: **DDR4 /LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4X SDRAM Specification, JEDEC JC-42.6-1847.17, 28 November 2017	2.1.8	Table 6	CK Single-ended input voltage [Vinse_CK_High – Vinse_CK_Low]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode

The purpose of this test is to verify the difference between the values of peak voltages of the high pulse and low pulse of the single-ended test signal.

Test Procedure: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode (for Test ID 70343)

1 Pre-condition the oscilloscope.
2 Trigger on the rising edge of the clock signal under test.
3 Find all valid positive and negative pulses of the Clock in the entire waveform.
A valid positive pulse of the Clock starts at the valid rising edge of the Clock and ends at the following valid falling edge of the Clock, whereas a valid negative pulse on the Clock starts at the valid falling edge of the Clock and ends at the following valid rising edge of the Clock.
4 Measure V_{MAX} of the first positive pulse and V_{MIN} of the first negative pulse.
5 Calculate the difference between the two measurements and denote the result as Vinse_CK #1.
6 Measure V_{MIN} of first negative pulse and V_{MAX} of the second positive pulse.
7 Calculate the difference of the two measurements and denote the result as Vinse_CK #2.
8 Continue steps 4 to 7 for measurements on the remaining pulse that was obtained.

9 Determine the worst result from the set of Vinse_CK values measured.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

Not available.

LPDDR4X (Single-ended) Test Mode

The difference in values of peak voltages between the high pulse and low pulse of the single-ended test signal shall be within the conformance limits as per the JEDEC specification.

SRIN_CK (rising edge)

Mode Supported: LPDDR4X (Single-Ended only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

Not available.

LPDDR4X (Differential) Test Mode

Not available.

LPDDR4X (Single-ended) Test Mode

70422 [SRIN_CK (rising edge)]

References: **DDR4 /LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC JC-42.6-1847.17, 28 November 2017	2.1.8	Table 6	SRIN_CK [Input Slew Rate for Clock]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode

The purpose of this test is to verify the difference in input slew rates for rising edge of the Clock signal.

Test Procedure: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode (for Test ID 70422)

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the clock signal under test.

3 Find all valid Clock rising edges in the entire waveform.
A valid clock rising edge starts at V_{IL} crossing and ends at the following V_{IH} crossing.

4 For all the valid Clock rising edges, find the transition time, T_R.
T_R is the time starting at V_{IL} crossing and ending at the following V_{IH} crossing.

5 Calculate SRIN_CK (rising edge) using the equation:
SRIN_CK (rising edge) = $[V_{IH} - V_{IL}] / T_R$

6 Determine the worst result from the set of SRIN_CK (rising edge) measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode

The difference in input slew rates for rising edge of the Clock signal shall be within the conformance limits as per the JEDEC specification.

SRIN_CK (falling edge)

Mode Supported: LPDDR4X (Single-Ended only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

Not available.

LPDDR4X (Differential) Test Mode

Not available.

LPDDR4X (Single-ended) Test Mode

70423 [SRIN_CK (falling edge)]

References: **DDR4 /LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4X SDRAM Specification, JEDEC JC-42.6-1847.17, 28 November 2017	2.1.8	Table 6	SRIN_CK [Input Slew Rate for Clock]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode

The purpose of this test is to verify the difference in input slew rates for falling edge of the Clock signal.

Test Procedure: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode (for Test ID 70423)

1 Pre-condition the oscilloscope.
2 Trigger on the falling edge of the clock signal under test.
3 Find all valid Clock falling edges in the entire waveform.
A valid clock falling edge starts at V_{IH} crossing and ends at the following V_{IL} crossing.
4 For all the valid Clock falling edges, find the transition time, T_F.
T_F is the time starting at V_{IH} crossing and ending at the following V_{IL} crossing.
5 Calculate SRIN_CK (falling edge) using the equation:
SRIN_CK (falling edge) = $[V_{IH} - V_{IL}] / T_F$
6 Determine the worst result from the set of SRIN_CK (falling edge) measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode

The difference in input slew rates for falling edge of the Clock signal shall be within the conformance limits as per the JEDEC specification.

Strobe Plus Tests

VSEH(Strobe Plus)

Test Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

10331 [VSEH(Strobe Plus)]

NOTE For SDRAM type DDR4, this test appears under the **Select Tests** tab only when you set the **Test Mode** to **Custom** in the under **Set Up** tab of the Test Application.

LPDDR4 Test Mode

50331 [VSEH(Strobe Plus)]

LPDDR4X (Differential) Test Mode

60331 [VSEH(Strobe Plus)]

References: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

There is no reference available for this test in the JEDEC specifications. The measurement result is reported as “Information Only”.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the maximum voltage of high pulse.

LPDDR4 / LPDDR4X (Differential) Test Modes

Not available.

Test Procedure: **DDR4 (for Test ID 10331) / LPDDR4 (for Test ID 50331) / LPDDR4X (Differential) (for Test ID 60331)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid Strobe positive pulse in the specified burst.
A valid Strobe positive pulse starts at Half_V_{DDQ} crossing at valid Strobe rising edge and ends at Half_V_{DDQ} crossing at the following valid Strobe falling edge.
4 Zoom into the first pulse and perform T_{MAX}.
   a Perform V_{TIME} with the T_{MAX} obtained in the previous step to obtain the maximum voltage of the pulse.
   b Take the V_{TIME} measurement as the value of V_{SEH}.
5 Continue the previous step with the rest of the positive pulses found in the specified burst.
6 Determine the worst result from the set of V_{SEH} measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of V_{SEH} for the test signal is reported as “Information Only”.

VSEL(Strobe Plus)

Test Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

10332 [VSEL(Strobe Plus)]

NOTE For SDRAM type DDR4, this test appears under the **Select Tests** tab only when you set the **Test Mode** to **Custom** in the under **Set Up** tab of the Test Application.

LPDDR4 Test Mode

50332 [VSEL(Strobe Plus)]

LPDDR4X (Differential) Test Mode

60332 [VSEL(Strobe Plus)]

References: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

There is no reference available for this test in the JEDEC specifications. The measurement result is reported as “Information Only”.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the minimum voltage of low pulse.

LPDDR4 / LPDDR4X (Differential) Test Modes

Not available.

Test Procedure: **DDR4 (for Test ID 10332) / LPDDR4 (for Test ID 50332) / LPDDR4X (Differential) (for Test ID 60332)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid Strobe negative pulse in the specified burst.
A valid Strobe negative pulse starts at Half_V_{DDQ} crossing at valid Strobe falling edge and ends at Half_V_{DDQ} crossing at the following valid Strobe rising edge.
4 Zoom into the first pulse and perform T_{MIN}.
Perform V_{TIME} with the T_{MIN} obtained in the previous step to obtain the minimum voltage of the pulse.
Take the V_{TIME} measurement as the value of V_{SEL}.
5 Continue the previous step with the rest of the negative pulses found in the specified burst.
6 Determine the worst result from the set of V_{SEL} measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of V_{SEL} for the test signal is reported as “Information Only”.

Vinse_DQS_High(Strobe Plus)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

50343 [Vinse_DQS_High(Strobe Plus)]

LPDDR4X (Differential) Test Mode

60343 [Vinse_DQS_High(Strobe Plus)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.8	Table 194	Vinse_DQS_High [DQS Single-Ended input voltage High from VREFDQ]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the peak voltage of the DQS_t high pulse.

Test Procedure: **LPDDR4 (for Test ID 50343) / LPDDR4X (Differential) (for Test ID 60343)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid DQS positive pulses in the entire waveform.
A valid positive pulse on the DQS_t signal starts at the valid rising edge of DQS_t and ends at the following valid falling edge of DQS_t.
4 Zoom into the first pulse that crosses VREFDQ and measure V_{MAX} from the VREFDQ crossing point.
5 Calculate the value of Vinse_DQS_High(Strobe Plus) using the equation:

$$\text{Vinse\_DQS\_High(Strobe Plus)} = V_{MAX} - \text{VREFDQ}$$

6 Continue the previous step with the rest of the positive pulses found in the specified waveform.
7 Determine the worst result from the set of Vinse_DQS_High values measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vinse_DQS_High for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_DQS_Low(Strobe Plus)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

50344 [Vinse_DQS_Low(Strobe Plus)]

LPDDR4X (Differential) Test Mode

60344 [Vinse_DQS_Low(Strobe Plus)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.8	Table 194	Vinse_DQS_Low [DQS Single-Ended input voltage Low from VREFDQ]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the peak voltage of the DQS_t low pulse.

Test Procedure: **LPDDR4 (for Test ID 50344) / LPDDR4X (Differential) (for Test ID 60344)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid DQS negative pulses in the entire waveform.
A valid negative pulse on the DQS_t signal starts at the valid falling edge of DQS_t and ends at the following valid rising edge of DQS_t.
4 Zoom into the first pulse that crosses VREFDQ and measure V_{MIN} from the VREFDQ crossing point.
5 Calculate the value of Vinse_DQS_Low(Strobe Plus) using the equation:

$$\text{Vinse\_DQS\_Low(Strobe Plus)} = \text{VREFDQ} - V_{MIN}$$

6 Continue the previous step with the rest of the negative pulses found in the specified waveform.
7 Determine the worst result from the set of Vinse_DQS_Low values measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vinse_DQS_Low for the test signal shall be within the conformance limits as per the JEDEC specification.

Strobe Minus Tests

VSEH(Strobe Minus)

Test Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

10335 [VSEH(Strobe Minus)]

NOTE For SDRAM type DDR4, this test appears under the **Select Tests** tab only when you set the **Test Mode** to **Custom** in the under **Set Up** tab of the Test Application.

LPDDR4 Test Mode

50335 [VSEH(Strobe Minus)]

LPDDR4X (Differential) Test Mode

60335 [VSEH(Strobe Minus)]

References: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

There is no reference available for this test in the JEDEC specifications. The measurement result is reported as “Information Only”.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the maximum voltage of high pulse.

LPDDR4 / LPDDR4X (Differential) Test Modes

Not available.

Test Procedure: **DDR4 (for Test ID 10335) / LPDDR4 (for Test ID 50335) / LPDDR4X (Differential) (for Test ID 60335)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid Strobe positive pulse in the specified burst.
A valid Strobe positive pulse starts at Half_V_{DDQ} crossing at valid Strobe rising edge and ends at Half_V_{DDQ} crossing at the following valid Strobe falling edge.
4 Zoom into the first pulse and perform T_{MAX}.
   a Perform V_{TIME} with the T_{MAX} obtained in the previous step to obtain the maximum voltage of the pulse.
   b Take the V_{TIME} measurement as the value of V_{SEH}.
5 Continue the previous step with the rest of the positive pulses found in the specified burst.
6 Determine the worst result from the set of V_{SEH} measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of V_{SEH} for the test signal is reported as “Information Only”.

VSEL(Strobe Minus)

Test Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

10336 [VSEL(Strobe Minus)]

NOTE For SDRAM type DDR4, this test appears under the **Select Tests** tab only when you set the **Test Mode** to **Custom** in the under **Set Up** tab of the Test Application.

LPDDR4 Test Mode

50336 [VSEL(Strobe Minus)]

LPDDR4X (Differential) Test Mode

60336 [VSEL(Strobe Minus)]

References: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

There is no reference available for this test in the JEDEC specifications. The measurement result is reported as “Information Only”.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the minimum voltage of low pulse.

LPDDR4 / LPDDR4X (Differential) Test Modes

Not available.

Test Procedure: **DDR4 (for Test ID 10336) / LPDDR4 (for Test ID 50336) / LPDDR4X (Differential) (for Test ID 60336)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid Strobe negative pulse in the specified burst.
A valid Strobe negative pulse starts at Half_V_{DDQ} crossing at valid Strobe falling edge and ends at Half_V_{DDQ} crossing at the following valid Strobe rising edge.
4 Zoom into the first pulse and perform T_{MIN}.
Perform V_{TIME} with the T_{MIN} obtained in the previous step to obtain the minimum voltage of the pulse.
Take the V_{TIME} measurement as the value of V_{SEL}.
5 Continue the previous step with the rest of the negative pulses found in the specified burst.
6 Determine the worst result from the set of V_{SEL} measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of V_{SEL} for the test signal is reported as “Information Only”.

Vinse_DQS_High(Strobe Minus)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

50345 [Vinse_DQS_High(Strobe Minus)]

LPDDR4X (Differential) Test Mode

60345 [Vinse_DQS_High(Strobe Minus)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.8	Table 194	Vinse_DQS_High [DQS Single-Ended input voltage High from VREFDQ]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the peak voltage of the DQS_c high pulse.

Test Procedure: **LPDDR4 (for Test ID 50343) / LPDDR4X (Differential) (for Test ID 60343)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid DQS positive pulses in the entire waveform.
A valid positive pulse on the DQS_c signal starts at the valid rising edge of DQS_c and ends at the following valid falling edge of DQS_c.
4 Zoom into the first pulse that crosses VREFDQ and measure V_{MAX} from the VREFDQ crossing point.
5 Calculate the value of Vinse_DQS_High(Strobe Minus) using the equation:

$$\text{Vinse\_DQS\_High(Strobe Minus)} = V_{MAX} - \text{VREFDQ}$$

6 Continue the previous step with the rest of the positive pulses found in the specified waveform.
7 Determine the worst result from the set of Vinse_DQS_High values measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vinse_DQS_High for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_DQS_Low(Strobe Minus)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

50346 [Vinse_DQS_Low(Strobe Minus)]

LPDDR4X (Differential) Test Mode

60346 [Vinse_DQS_Low(Strobe Minus)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.8	Table 194	Vinse_DQS_Low [DQS Single-Ended input voltage Low from VREFDQ]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the peak voltage of the DQS_t low pulse.

Test Procedure: **LPDDR4 (for Test ID 50344) / LPDDR4X (Differential) (for Test ID 60344)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid DQS negative pulses in the entire waveform.
A valid negative pulse on the DQS_c signal starts at the valid falling edge of DQS_c and ends at the following valid rising edge of DQS_c.
4 Zoom into the first pulse that crosses VREFDQ and measure V_{MIN} from the VREFDQ crossing point.
5 Calculate the value of Vinse_DQS_Low(Strobe Minus) using the equation:

$$\text{Vinse\_DQS\_Low(Strobe Minus)} = \text{VREFDQ} - V_{MIN}$$

6 Continue the previous step with the rest of the negative pulses found in the specified waveform.
7 Determine the worst result from the set of Vinse_DQS_Low values measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vinse_DQS_Low for the test signal shall be within the conformance limits as per the JEDEC specification.

Data Strobe Tests

Vinse_DQS

Mode Supported: LPDDR4X (Single-Ended only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

Not available.

LPDDR4X (Differential) Test Mode

Not available.

LPDDR4X (Single-ended) Test Mode

70346 [Vinse_DQS]

References: **DDR4 /LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC JC-42.6-1847.17, 28 November 2017	2.1.8	Table 6	DQS Single-ended input voltage [Vinse_DQS_High – Vinse_DQS_Low]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode

The purpose of this test is to verify the difference in values of peak voltages between the high pulse and low pulse of the single-ended test signal.

Test Procedure: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode (for Test ID 70346)

1 Pre-condition the oscilloscope.
2 Acquire and split read and write burst of the acquired signal.
3 Take the first valid write burst found.
4 Find all valid Strobe positive and negative pulses in the specified burst.
A valid Strobe positive pulse starts at the valid rising edge of the Strobe and ends at the following valid falling edge of the Strobe, whereas a valid negative pulse on the Strobe starts at the valid falling edge of the Strobe and ends at the following valid rising edge of the Strobe.
5 Measure V_{MAX} of the first positive pulse and V_{MIN} of the first negative pulse.
6 Calculate the difference between the two measurements and denote the result as Vinse_DQS #1.
7 Measure V_{MIN} of first negative pulse and V_{MAX} of the second positive pulse.
8 Calculate the difference between the two measurements and denote the result as Vinse_DQS #2.

9 Continue steps 4 to 7 for measurements on the remaining pulses in the said burst.

10 Determine the worst result from the set of Vinse_DQS values measured.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

Not available.

LPDDR4X (Single-ended) Test Mode

The difference in values of peak voltage between the high pulse and low pulse of the single-ended test signal shall be within the conformance limits as per the JEDEC specification.

SRIN_DQS (rising edge)

Mode Supported: LPDDR4X (Single-Ended only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

Not available.

LPDDR4X (Differential) Test Mode

Not available.

LPDDR4X (Single-ended) Test Mode

750508 [SRIN_DQS (rising edge)]

References: **DDR4 /LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC JC-42.6-1847.17, 28 November 2017	2.1.8	Table 6	SRIN_DQS [Input Slew Rate for DQS]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode

The purpose of this test is to verify the difference in input slew rates for rising edge of the Strobe signal.

Test Procedure: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode (for Test ID 750508)

1 Pre-condition the oscilloscope.
2 Acquire and split read and write burst of the acquired signal.
3 Take the first valid write burst found.
4 Find all valid Slock rising edges in the specified burst.
A valid Strobe rising edge starts at V_{IL} crossing and ends at the following V_{IH} crossing.
5 For all the valid Strobe rising edges, find the transition time, T_R.
T_R is the time starting at V_{IL} crossing and ending at the following V_{IH} crossing.
6 Calculate SRIN_DQS (rising edge) using the equation:
SRIN_DQS (rising edge) = $[V_{IH} - V_{IL}] / T_R$
7 Determine the worst result from the set of SRIN_DQS (rising edge) measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode

The difference in input slew rates for rising edge of the Strobe signal shall be within the conformance limits as per the JEDEC specification.

SRIN_DQS (falling edge)

Mode Supported: LPDDR4X (Single-Ended only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

Not available.

LPDDR4X (Differential) Test Mode

Not available.

LPDDR4X (Single-ended) Test Mode

750509 [SRIN_DQS (falling edge)]

References: **DDR4 /LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC JC-42.6-1847.17, 28 November 2017	2.1.8	Table 6	SRIN_DQS [Input Slew Rate for DQS]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode

The purpose of this test is to verify the difference in input slew rates for falling edge of the Strobe signal.

Test Procedure: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode (for Test ID 750509)

1 Pre-condition the oscilloscope.
2 Acquire and split read and write burst of the acquired signal.
3 Take the first valid write burst found.
4 Find all valid Strobe falling edges in the specified burst.
A valid Strobe falling edge starts at V_{IH} crossing and ends at the following V_{IL} crossing.
5 For all the valid Strobe falling edges, find the transition time, T_F.
T_F is the time starting at V_{IH} crossing and ending at the following V_{IL} crossing.
6 Calculate SRIN_DQS (falling edge) using the equation:
SRIN_DQS (falling edge) = $[V_{IH} - V_{IL}] / T_F$
7 Determine the worst result from the set of SRIN_DQS (falling edge) measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

Not available.

LPDDR4X (Single-ended) Test Mode

The difference in input slew rates for falling edge of the Strobe signal shall be within the conformance limits as per the JEDEC specification.

VIH/VIL for Command and Address

VIH.CA(AC)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

10311 [VIH.CA(AC)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.1	Table 121	VIH.CA(AC100) [AC Input Logic High]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 / LPDDR4 / LPDDR4X Test Modes**

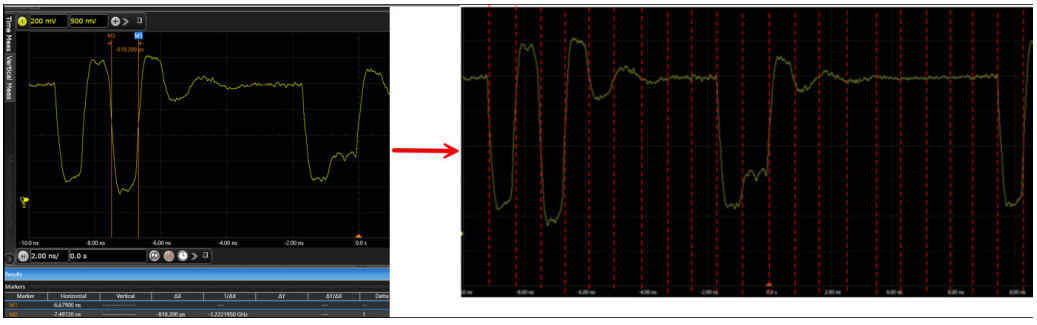
The purpose of this test is to verify the high level voltage value of the test signal within a valid sampling window.

Test Procedure: **DDR4 (for Test ID 10311)**

1 Sample/acquire signal data.

2 Find all valid positive pulses.
A valid positive pulse starts at V_{REF} crossing at valid rising edge and ends at V_{REF} crossing at the following valid falling edge.

3 For each pulse, do partition on measurement region where each region is about 1 clock cycle (as shown in the below reference image).



4 Zoom in on the first measurement region and perform VTOP measurement.
Note the V_{TOP} measurement results as $V_{IH.CA\ (AC)}$ value.

5 Continue the previous step with the rest measurement region on all positive pulse.

6 Determine the worst result from the set of $V_{IH.CA\ (AC)}$ measured.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results:

DDR4 Test Mode

The measured value of $V_{IH.CA(AC)}$ for the test signal shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

VIH.CA(DC)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

10312 [VIH.CA(DC)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.1	Table 121	VIH.CA(DC75) [DC Input Logic High]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 / LPDDR4 / LPDDR4X Test Modes**

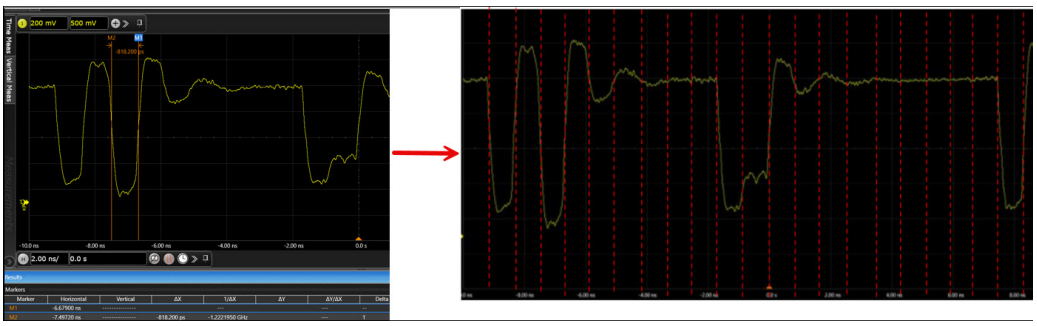
The purpose of this test is to verify the high level voltage value of the test signal within a valid sampling window.

Test Procedure: **DDR4 (for Test ID 10312)**

1 Sample/acquire signal data.

2 Find all valid positive pulses.
A valid positive pulse starts at V_{REF} crossing at valid rising edge and ends at V_{REF} crossing at the following valid falling edge.

3 For each pulse, do partition on measurement region where each region is about 1 clock cycle (as shown in the below reference image).



4 Zoom in on the first measurement region and perform VTOP measurement.
Note the V_{TOP} measurement results as $V_{IH.CA\ (DC)}$ value.

5 Continue the previous step with the rest measurement region on all positive pulse.

6 Determine the worst result from the set of $V_{IH.CA\ (DC)}$ measured.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results:

DDR4 Test Mode

The measured value of $V_{IH.CA(DC)}$ for the test signal shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

VIL.CA(AC)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

10321 [VIL.CA(AC)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.1	Table 121	VIL.CA(AC100) [AC Input Logic Low]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 / LPDDR4 / LPDDR4X Test Modes**

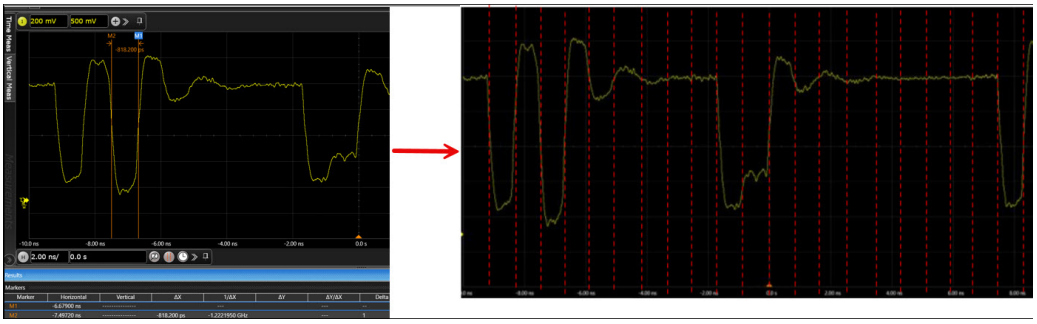
The purpose of this test is to verify the low level voltage value of the test signal within a valid sampling window.

Test Procedure: **DDR4 (for Test ID 10321)**

1 Sample/acquire signal data.

2 Find all valid negative pulses.
A valid negative pulse starts at V_{REF} crossing at valid falling edge and ends at V_{REF} crossing at the following valid rising edge.

3 For each pulse, do partition on measurement region where each region is about 1 clock cycle (as shown in the below reference image).



4 Zoom in on the first measurement region and perform V_{BASE} measurement.
Note the V_{BASE} measurement results as $V_{IL.CA\ (AC)}$ value.

5 Continue the previous step with the rest measurement region on all positive pulse.

6 Determine the worst result from the set of $V_{IL.CA\ (AC)}$ measured.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results:

DDR4 Test Mode

The measured value of $V_{IL.CA(AC)}$ for the test signal shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

VIL.CA(DC)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

10322 [VIL.CA(DC)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.1	Table 121	VIL.CA(DC75) [DC Input Logic Low]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 / LPDDR4 / LPDDR4X Test Modes**

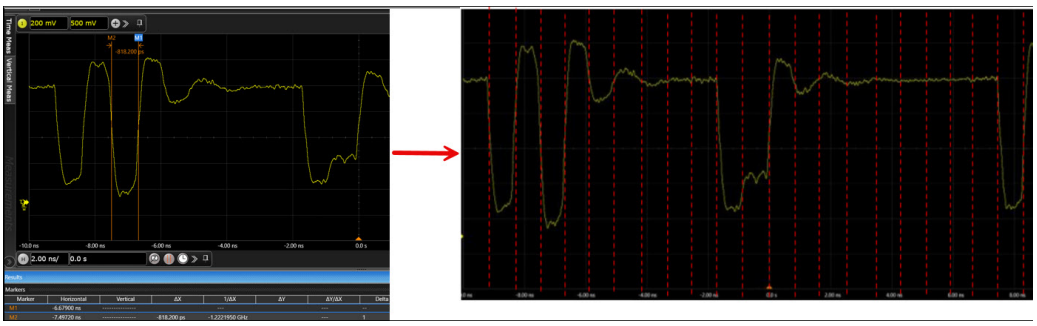
The purpose of this test is to verify the low level voltage value of the test signal within a valid sampling window.

Test Procedure: **DDR4 (for Test ID 10322)**

1 Sample/acquire signal data.

2 Find all valid negative pulses.
A valid negative pulse starts at V_{REF} crossing at valid falling edge and ends at V_{REF} crossing at the following valid rising edge.

3 For each pulse, do partition on measurement region where each region is about 1 clock cycle (as shown in the below reference image).



4 Zoom in on the first measurement region and perform V_{BASE} measurement.
Note the V_{BASE} measurement results as $V_{IL.CA\ (DC)}$ value.

5 Continue the previous step with the rest measurement region on all positive pulse.

6 Determine the worst result from the set of $V_{IL.CA\ (DC)}$ measured.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results:

DDR4 Test Mode

The measured value of $V_{IL.CA(DC)}$ for the test signal shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

Single-Ended Signals (READ cycle tests)

VOH/VOL

VOH(AC)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

11311 [VOH(AC)]

LPDDR4 Test Mode

51311 [VOH(AC)]

LPDDR4X (Differential) Test Mode

61311 [VOH(AC)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	9.2	Table 139	VOH(AC) [AC Output High Measurement Level (for output SR)]

LPDDR4 / LPDDR4X (Differential) Test Modes

There is no reference available for this test in the JEDEC specifications. The measurement result is reported as “Information Only”.

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the high level voltage value of the test signal within a valid read burst.

Test Procedure: **DDR4 (for Test ID 11311) / LPDDR4 (for Test ID 51311) / LPDDR4X (Differential) (for Test ID 61311)**

1 Acquire and split the read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid positive pulses in the specified burst.
A valid positive pulse starts at the middle crossing at valid rising edge and ends at middle crossing at the following valid falling edge.

NOTE

(For Test ID 11311)–The middle crossing for DDR4 is the user-entered value of V_{TT}.

(For Test ID 51311)–The middle crossing for LPDDR4 = 0.5 x [(user-entered value of $V_{OH(AC)}$ + user-entered value of $V_{OL(AC)}$)].

(For Test ID 61311)–The middle crossing for LPDDR4X = 0.5 x [(user-entered value of $V_{OH(AC)}$ + user-entered value of $V_{OL(AC)}$)].

4 Zoom in on the first valid positive pulse and perform V_{TOP} measurement.
Take the V_{TOP} measurement results as $V_{OH(AC)}$ value.

5 Continue the previous step with the rest of the valid positive pulses that were found in the burst.

6 Determine the worst result from the set of $V_{OH(AC)}$ measured.

Expected/ Observable Results:

DDR4 Test Mode

The measured value of $V_{OH(AC)}$ for the test signal shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of $V_{OH(AC)}$ for the test signal is reported as “Information Only”.

VOH(DC)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

11312 [VOH(DC)]

LPDDR4 Test Mode

51312 [VOH(DC)]

LPDDR4X (Differential) Test Mode

61312 [VOH(DC)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	9.2	Table 139	VOH(DC) [DC Output High Measurement Level (for IV Curve Linearity)]

LPDDR4 / LPDDR4X (Differential) Test Modes

There is no reference available for this test in the specification document. The measurement result is reported as “Information Only”.

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the high level voltage value of the test signal within a valid read burst.

Test Procedure: **DDR4 (for Test ID 11312) / LPDDR4 (for Test ID 51312) / LPDDR4X (Differential) (for Test ID 61312)**

1 Acquire and split the read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid positive pulses in the specified burst.
A valid positive pulse starts at the middle crossing at valid rising edge and ends at middle crossing at the following valid falling edge.

NOTE

(For Test ID 11312)–The middle crossing for DDR4 is the user-entered value of V_{TT}.

(For Test ID 51312)–The middle crossing for LPDDR4 = 0.5 x [(user-entered value of $V_{OH(AC)}$ + user-entered value of $V_{OL(AC)}$)]

(For Test ID 61312)–The middle crossing for LPDDR4X = 0.5 x [(user-entered value of $V_{OH(AC)}$ + user-entered value of $V_{OL(AC)}$)]

4 Zoom in on the first valid positive pulse and perform V_{TOP} measurement.
Take the V_{TOP} measurement results as $V_{OH(DC)}$ value.

5 Continue the previous step with the rest of the valid positive pulses that were found in the burst.

6 Determine the worst result from the set of $V_{OH(DC)}$ measured.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of $V_{OH(DC)}$ for the test signal shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of $V_{OH(DC)}$ for the test signal is reported as “Information Only”.

VOL(AC)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

11321 [VOL(AC)]

LPDDR4 Test Mode

51321 [VOL(AC)]

LPDDR4X (Differential) Test Mode

61321 [VOL(AC)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	9.2	Table 139	VOL(AC) [AC Output Low Measurement Level (for output SR)]

LPDDR4 / LPDDR4X (Differential) Test Modes

There is no reference available for this test in the JEDEC specifications. The measurement result is reported as “Information Only”.

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the low level voltage value of the test signal within a valid read burst.

Test Procedure: **DDR4 (for Test ID 11321) / LPDDR4 (for Test ID 51321) / LPDDR4X (Differential) (for Test ID 61321)**

1 Acquire and split the read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid negative pulses in the specified burst.
A valid negative pulse starts at the middle crossing at valid falling edge and ends at middle crossing at the following valid rising edge.

NOTE

(For Test ID 11321)–The middle crossing for DDR4 is the user-entered value of V_{TT}.

(For Test ID 51321)–The middle crossing for LPDDR4 = 0.5 x [(user-entered value of $V_{OH(AC)}$ + user-entered value of $V_{OL(AC)}$)].

(For Test ID 61321)–The middle crossing for LPDDR4X = 0.5 x [(user-entered value of $V_{OH(AC)}$ + user-entered value of $V_{OL(AC)}$)].

4 Zoom in on the first valid negative pulse and perform V_{BASE} measurement.
Take the V_{BASE} measurement results as $V_{OL(AC)}$ value.

5 Continue the previous step with the rest of the valid negative pulses that were found in the burst.

6 Determine the worst result from the set of $V_{OL(AC)}$ measured.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of $V_{OL(AC)}$ for the test signal shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of $V_{OL(AC)}$ for the test signal is reported as “Information Only”.

VOL(DC)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

11322 [VOL(DC)]

LPDDR4 Test Mode

51322 [VOL(DC)]

LPDDR4X (Differential) Test Mode

61322 [VOL(DC)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	9.2	Table 139	VOL(DC) [DC Output Low Measurement Level (for IV Curve Linearity)]

LPDDR4 / LPDDR4X (Differential) Test Modes

There is no reference available for this test in the JEDEC specifications. The measurement result is reported as “Information Only”.

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the low level voltage value of the test signal within a valid read burst.

Test Procedure: **DDR4 (for Test ID 11322) / LPDDR4 (for Test ID 51322) / LPDDR4X (Differential) (for Test ID 61322)**

1 Acquire and split the read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid negative pulses in the specified burst.
A valid negative pulse starts at the middle crossing at valid falling edge and ends at middle crossing at the following valid rising edge.

NOTE

(For Test ID 11322)–The middle crossing for DDR4 is the user-entered value of V_{TT}.

(For Test ID 51322)–The middle crossing for LPDDR4 = 0.5 x [(user-entered value of $V_{OH(AC)}$ + user-entered value of $V_{OL(AC)}$)]

(For Test ID 61322)–The middle crossing for LPDDR4X = 0.5 x [(user-entered value of $V_{OH(AC)}$ + user-entered value of $V_{OL(AC)}$)]

4 Zoom in on the first valid negative pulse and perform V_{BASE} measurement.
Take the V_{BASE} measurement results as $V_{OL(DC)}$ value.

5 Continue the previous step with the rest of the valid negative pulses that were found in the burst.

6 Determine the worst result from the set of $V_{OL(DC)}$ measured.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of $V_{OL(DC)}$ for the test signal shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of $V_{OL(DC)}$ for the test signal is reported as “Information Only”.

Output Slew Rate

SRQseR

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

11341 [SRQseR]

LPDDR4 Test Mode

51341 [SRQseR]

LPDDR4X (Differential) Test Mode

61341 [SRQseR]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	9.4	Table 142	SRQse [Single ended output slew rate]

LPDDR4 Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.4	Table 200	SRQse [Single ended output slew rate ($V_{OH} = V_{DDQ}/3$)]

LPDDR4X (Differential) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4X SDRAM Specification, JEDEC Standard no. 209-4-1, January 2017	4.2	Table 14	SRQse [Single ended output slew rate ($V_{OH} = V_{DDQ} * 0.5$)]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the rising slew rate value of the test signal within the read burst.

Test Procedure: **DDR4 (for Test ID 11341) / LPDDR4 (for Test ID 51341) / LPDDR4X (Differential) (for Test ID 61341)**

1 Acquire and split the read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all the valid rising edges in the specified burst.
A valid rising edge starts at $V_{OL(AC)}$ crossing and ends at the following $V_{OH(AC)}$ crossing.

4 For all the valid rising edges, find the transition time, T_R.
T_R is the time starting at $V_{OL(AC)}$ crossing and ending at the following $V_{OH(AC)}$ crossing.

5 Calculate SRQseR using the equation:

$$SRQseR = [V_{OH(AC)} - V_{OL(AC)}] / T_R$$

6 Determine the worst result from the set of SRQseR measured.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The calculated Rising Slew (SRQseR) value for the test signal shall be within the conformance limits as per the JEDEC specification.

SRQseF

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

11342 [SRQseF]

LPDDR4 Test Mode

51342 [SRQseF]

LPDDR4X (Differential) Test Mode

61342 [SRQseF]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	9.4	Table 142	SRQse [Single ended output slew rate]

LPDDR4 Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.4	Table 200	SRQse [Single ended output slew rate ($V_{OH} = V_{DDQ}/3$)]

LPDDR4X (Differential) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4X SDRAM Specification, JEDEC Standard no. 209-4-1, January 2017	4.2	Table 14	SRQse [Single ended output slew rate ($V_{OH} = V_{DDQ} * 0.5$)]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the falling slew rate value of the test signal within the read burst.

Test Procedure: **DDR4 (for Test ID 11342) / LPDDR4 (for Test ID 51342) / LPDDR4X (Differential) (for Test ID 61342)**

1 Acquire and split the read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all the valid falling edges in the specified burst.
A valid falling edge starts at $V_{OH(AC)}$ crossing and ends at the following $V_{OL(AC)}$ crossing.

4 For all the valid falling edges, find the transition time, T_F.
T_R is the time starting at $V_{OH(AC)}$ crossing and ending at the following $V_{OL(AC)}$ crossing.

5 Calculate SRQseF using the equation:

$$SRQseF = [V_{OH(AC)} - V_{OL(AC)}] / T_F$$

6 Determine the worst result from the set of SRQseF measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The calculated Falling Slew (SRQseF) value for the test signal shall be within the conformance limits as per the JEDEC specification.

Overshoot/Undershoot (Clock Plus)

Overshoot amplitude (Clock Plus)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

103024 [Overshoot amplitude (Clock Plus)]

LPDDR4 Test Mode

503016 [Overshoot amplitude (Clock Plus)]

LPDDR4X (Differential) Test Mode

603016 [Overshoot amplitude (Clock Plus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.5	Table 126	[Maximum peak amplitude above VCOS] [Maximum overshoot area per 1 UI above VCOS] [Maximum overshoot area per 1 UI between VDD and VDOS]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for overshoot area] [Maximum area above V_{DD}]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Test Procedure: **DDR4 (for Test ID 103024)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DD} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

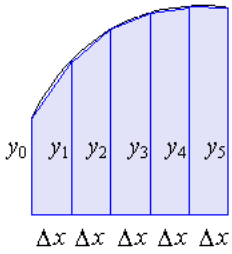
$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD}$$

b Evaluate Area_below_V_{DD} using the equation:

$$\text{Area\_below\_}V_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

The Trapezoidal Rule



$$\text{Area} \approx \frac{1}{2}(y_0 + y_1)\Delta x + \frac{1}{2}(y_1 + y_2)\Delta x + \frac{1}{2}(y_2 + y_3)\Delta x + \ldots$$

We can simplify this to give us the **Trapezoidal Rule**, for n trapezoids:

$$\text{Area} \approx \Delta x\left(\frac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + \frac{y_n}{2}\right)$$

Figure 8 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD} using the equation:

$$\text{Area\_Above\_}V_{DD} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD}$$

e Evaluate Area_Above_$V_{DDAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 15).

f Calculate Area_Between_V_{DD}_and_$V_{DDAbsMax}$ using the equation:

$$\text{Area\_Between\_}V_{DD}\text{\_and\_}V_{DDAbsMax} = \text{Area\_Above\_}V_{DD} - \text{Area\_Above\_}V_{DDAbsMax}$$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDAbsMax}$
- Area_Between_V_{DD}_and_$V_{DDAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

LPDDR4 (for Test ID 503016) / LPDDR4X (Differential) (for Test ID 603016)

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use T_{MAX} and V_{MAX} to get the time-stamp of maximum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to maximize the peak area.

5 Find the edges before and after the Overshoot Point at the Supply Reference Level in order to calculate the maximum overshoot length duration.
Table 2 shows the supply reference level for each pin group:

Table 1 Supply reference level

PIN	Supply Reference Level
Address and Control pin	V_{DD2}
Data, Strobe and Mask pin	V_{DDQ}
Clock	V_{DD2}

6 Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - \text{Supply Reference Level (refer to Table 2)}$$

7 Calculate Overshoot area (V-ns)

a By calculating area of a triangle using the overshoot width as the triangle base and the overshoot amplitude as the triangle height.

b For Overshoot area, use the equation:

$$\text{Area} = 0.5 \times \text{base} \times \text{height}$$

8 Compare test results with the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area above VDD Abs Max(Clock Plus)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103025 [Overshoot area above VDD Abs Max (Clock Plus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.5	Table 126	[Maximum peak amplitude above VCOS] [Maximum overshoot area per 1 UI above VCOS] [Maximum overshoot area per 1 UI between VDD and VDOS]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 (for Test ID 103025)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DD} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD}$$

b Evaluate Area_below_V_{DD} using the equation:

$$\text{Area\_below\_}V_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

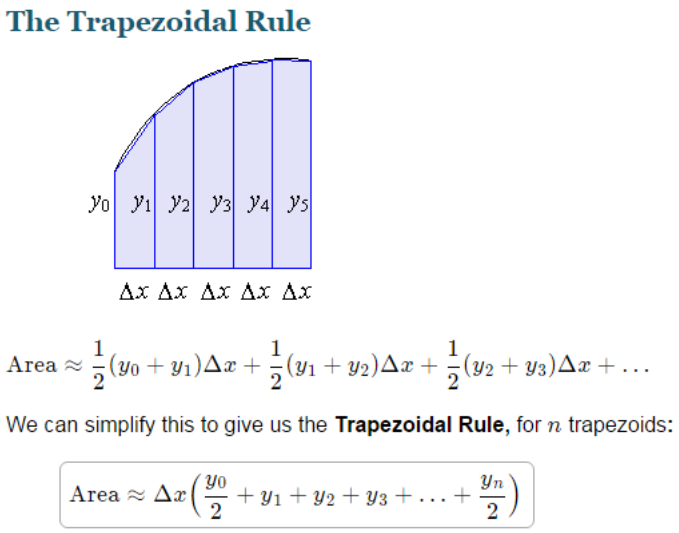


Figure 9 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD} using the equation:

$$\text{Area\_Above\_}V_{DD} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD}$$

e Evaluate Area_Above_$V_{DDAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 15).

f Calculate Area_Between_V_{DD}_and_$V_{DDAbsMax}$ using the equation:

$$\text{Area\_Between\_}V_{DD}\text{\_and\_}V_{DDAbsMax} = \text{Area\_Above\_}V_{DD} - \text{Area\_Above\_}V_{DDAbsMax}$$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDAbsMax}$
- Area_Between_V_{DD}_and_$V_{DDAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area between VDD and VDD Abs Max(Clock Plus)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103026 [Overshoot area between VDD and VDD Abs Max (Clock Plus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.5	Table 126	[Maximum peak amplitude above VCOS] [Maximum overshoot area per 1 UI above VCOS] [Maximum overshoot area per 1 UI between VDD and VDOS]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 (for Test ID 103026)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DD} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD}$$

b Evaluate Area_below_V_{DD} using the equation:

$$\text{Area\_below\_}V_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

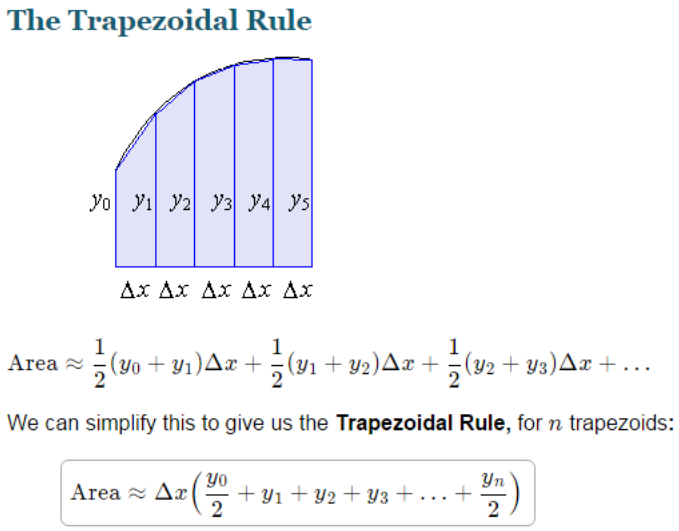


Figure 10 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD} using the equation:

$$\text{Area\_Above\_}V_{DD} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD}$$

e Evaluate Area_Above_$V_{DDAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 15).

f Calculate Area_Between_V_{DD}_and_$V_{DDAbsMax}$ using the equation:

$$\text{Area\_Between\_}V_{DD}\text{\_and\_}V_{DDAbsMax} = \text{Area\_Above\_}V_{DD} - \text{Area\_Above\_}V_{DDAbsMax}$$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDAbsMax}$
- Area_Between_V_{DD}_and_$V_{DDAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area (Clock Plus)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

503017 [Overshoot area (Clock Plus)]

LPDDR4X (Differential) Test Mode

603017 [Overshoot area (Clock Plus)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for overshoot area] [Maximum area above V_{DD}]

Test Overview: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Test Procedure: **LPDDR4 (for Test ID 503017) / LPDDR4X (Differential) (for Test ID 603017)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DD} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD}$$

b Evaluate Area_below_V_{DD} using the equation:

$$\text{Area\_below\_}V_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

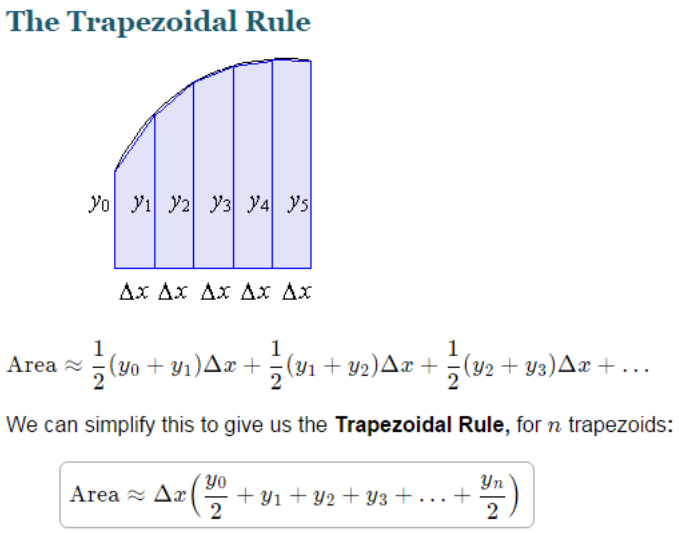


Figure 11 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD} using the equation:

Area_Above_V_{DD} = Total_Area_Above_0V - Area_below_V_{DD}

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DD}

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

LPDDR4 / LPDDR4X (Differential) Test Modes

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot amplitude (Clock Plus)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

103027 [Undershoot amplitude (Clock Plus)]

LPDDR4 Test Mode

503018 [Undershoot amplitude (Clock Plus)]

LPDDR4X (Differential) Test Mode

603018 [Undershoot amplitude (Clock Plus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.5	Table 126	[Maximum peak amplitude allowed for undershoot] [Maximum undershoot area per 1 UI below VSS]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for undershoot area] [Maximum area below V_{SS}]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Test Procedure: **DDR4 Test Mode (for Test ID 103027)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

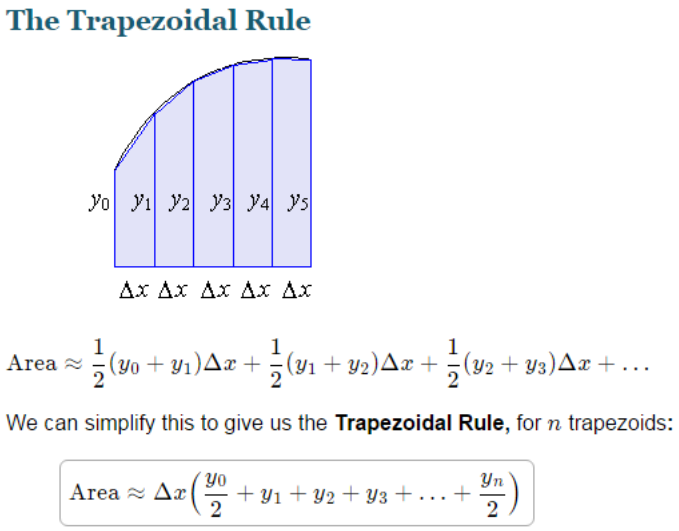


Figure 12 Equation for Total_Area_Above_0V

c To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Total_Area_Below_0V

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

LPDDR4 (for Test ID 503018) / LPDDR4X (Differential) (for Test ID 603018)

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use T_{MIN} and V_{MIN} to get the time-stamp of minimum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to minimize the peak area.

5 Find the edges before and after the Undershoot Point at the GND (~0V) level in order to calculate the maximum undershoot length duration.

6 Calculate Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

7 Calculate Undershoot area (V-ns)

a By calculating area of a triangle using the undershoot width as the triangle base and the undershoot amplitude as the triangle height.

b For Undershoot area, use the equation:

$$\text{Area} = 0.5 \times \text{base} \times \text{height}$$

8 Compare test results with the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area below VSS(Clock Plus)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103028 [Undershoot area below VSS (Clock Plus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.5	Table 126	[Maximum peak amplitude allowed for undershoot] [Maximum undershoot area per 1 UI below VSS]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 Test Mode (for Test ID 103028)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

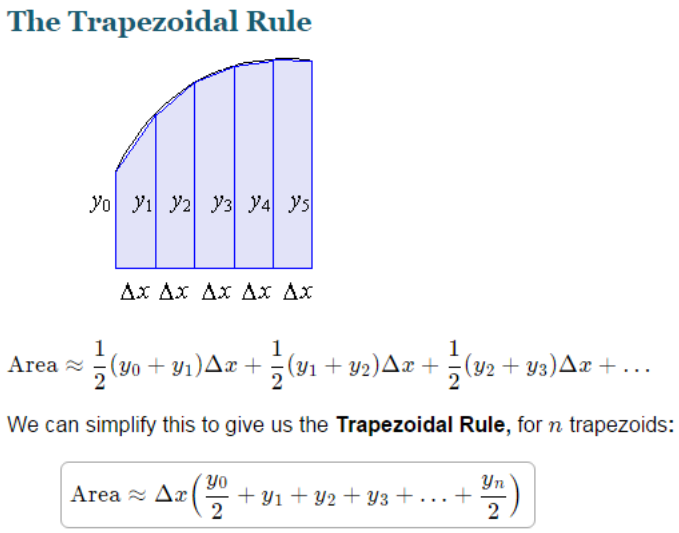


Figure 13 Equation for Total_Area_Above_0V

c To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Total_Area_Below_0V

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area (Clock Plus)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

503019 [Undershoot area (Clock Plus)]

LPDDR4X (Differential) Test Mode

603019 [Undershoot area (Clock Plus)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for undershoot area] [Maximum area below V_{SS}]

Test Overview: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Test Procedure: **LPDDR4 (for Test ID 503019) / LPDDR4X (Differential) (for Test ID 603019)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

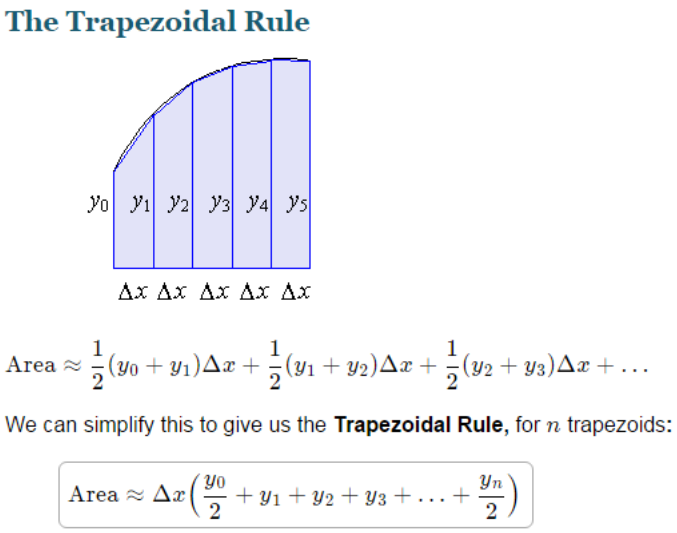


Figure 14 Equation for Total_Area_Above_0V

c To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Total_Area_Below_0V

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

LPDDR4 / LPDDR4X (Differential) Test Modes

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot/Undershoot (Clock Minus)

Overshoot amplitude (Clock Minus)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

103029 [Overshoot amplitude (Clock Minus)]

LPDDR4 Test Mode

503020 [Overshoot amplitude (Clock Minus)]

LPDDR4X (Differential) Test Mode

603020 [Overshoot amplitude (Clock Minus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.5	Table 126	[Maximum peak amplitude above VCOS] [Maximum overshoot area per 1 UI above VCOS] [Maximum overshoot area per 1 UI between VDD and VDOS]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for overshoot area] [Maximum area above V_{DD}]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Test Procedure: **DDR4 (for Test ID 103029)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DD} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

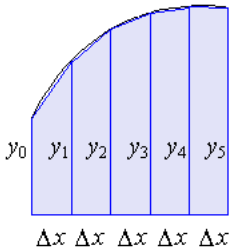
$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD}$$

b Evaluate Area_below_V_{DD} using the equation:

$$\text{Area\_below\_}V_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

The Trapezoidal Rule



$$\text{Area} \approx \frac{1}{2}(y_0 + y_1)\Delta x + \frac{1}{2}(y_1 + y_2)\Delta x + \frac{1}{2}(y_2 + y_3)\Delta x + \ldots$$

We can simplify this to give us the **Trapezoidal Rule**, for n trapezoids:

$$\text{Area} \approx \Delta x\left(\frac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + \frac{y_n}{2}\right)$$

Figure 15 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD} using the equation:

$$\text{Area\_Above\_}V_{DD} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD}$$

e Evaluate Area_Above_$V_{DDAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 15).

f Calculate Area_Between_V_{DD}_and_$V_{DDAbsMax}$ using the equation:

$$\text{Area\_Between\_}V_{DD}\text{\_and\_}V_{DDAbsMax} = \text{Area\_Above\_}V_{DD} - \text{Area\_Above\_}V_{DDAbsMax}$$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDAbsMax}$
- Area_Between_V_{DD}_and_$V_{DDAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

LPDDR4 (for Test IDs 503016 & 503020) / LPDDR4X (Differential) (for Test IDs 603016 & 603020)

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use T_{MAX} and V_{MAX} to get the time-stamp of maximum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to maximize the peak area.

5 Find the edges before and after the Overshoot Point at the Supply Reference Level in order to calculate the maximum overshoot length duration.
Table 2 shows the supply reference level for each pin group:

Table 2 Supply reference level

PIN	Supply Reference Level
Address and Control pin	V_{DD2}
Data, Strobe and Mask pin	V_{DDQ}
Clock	V_{DD2}

6 Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - \text{Supply Reference Level (refer to Table 2)}$$

7 Calculate Overshoot area (V-ns)

a By calculating area of a triangle using the overshoot width as the triangle base and the overshoot amplitude as the triangle height.

b For Overshoot area, use the equation:

$$\text{Area} = 0.5 \times \text{base} \times \text{height}$$

8 Compare test results with the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area above VDD Abs Max(Clock Minus)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103030 [Overshoot area above VDD Abs Max (Clock Minus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.5	Table 126	[Maximum peak amplitude above VCOS] [Maximum overshoot area per 1 UI above VCOS] [Maximum overshoot area per 1 UI between VDD and VDOS]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 (for Test ID 103030)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DD} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD}$$

b Evaluate Area_below_V_{DD} using the equation:

$$\text{Area\_below\_}V_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

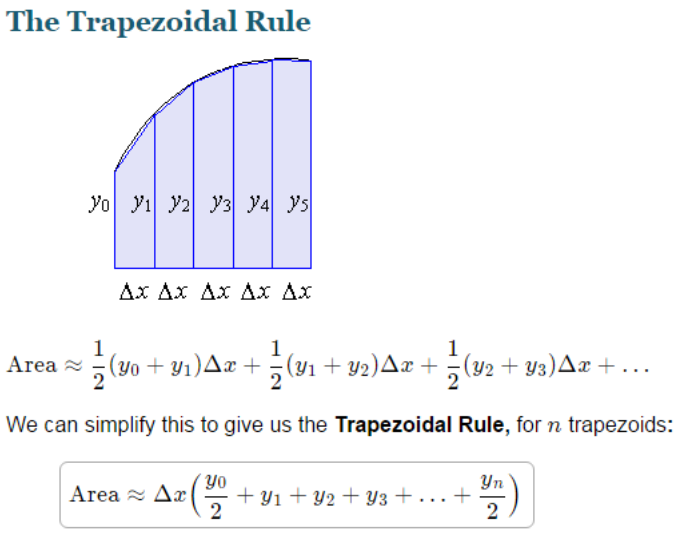


Figure 16 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD} using the equation:

$$\text{Area\_Above\_}V_{DD} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD}$$

e Evaluate Area_Above_$V_{DDAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 15).

f Calculate Area_Between_V_{DD}_and_$V_{DDAbsMax}$ using the equation:

$$\text{Area\_Between\_}V_{DD}\text{\_and\_}V_{DDAbsMax} = \text{Area\_Above\_}V_{DD} - \text{Area\_Above\_}V_{DDAbsMax}$$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDAbsMax}$
- Area_Between_V_{DD}_and_$V_{DDAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area between VDD and VDD Abs Max(Clock Minus)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103031 [Overshoot area between VDD and VDD Abs Max (Clock Minus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.5	Table 126	[Maximum peak amplitude above VCOS] [Maximum overshoot area per 1 UI above VCOS] [Maximum overshoot area per 1 UI between VDD and VDOS]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 (for Test ID 103031)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DD} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD}$$

b Evaluate Area_below_V_{DD} using the equation:

$$\text{Area\_below\_}V_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

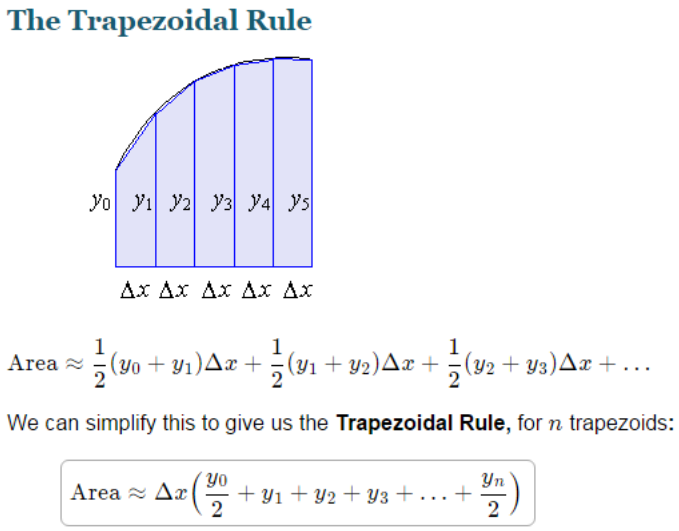


Figure 17 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD} using the equation:

$$\text{Area\_Above\_}V_{DD} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD}$$

e Evaluate Area_Above_$V_{DDAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 15).

f Calculate Area_Between_V_{DD}_and_$V_{DDAbsMax}$ using the equation:

$$\text{Area\_Between\_}V_{DD}\text{\_and\_}V_{DDAbsMax} = \text{Area\_Above\_}V_{DD} - \text{Area\_Above\_}V_{DDAbsMax}$$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDAbsMax}$
- Area_Between_V_{DD}_and_$V_{DDAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area (Clock Minus)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

503021 [Overshoot area (Clock Minus)]

LPDDR4X (Differential) Test Mode

603021 [Overshoot area (Clock Minus)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for overshoot area] [Maximum area above V_{DD}]

Test Overview: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Test Procedure: **LPDDR4 (for Test ID 503021) / LPDDR4X (Differential) (for Test ID 603021)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DD} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD}$$

b Evaluate Area_below_V_{DD} using the equation:

$$\text{Area\_below\_}V_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

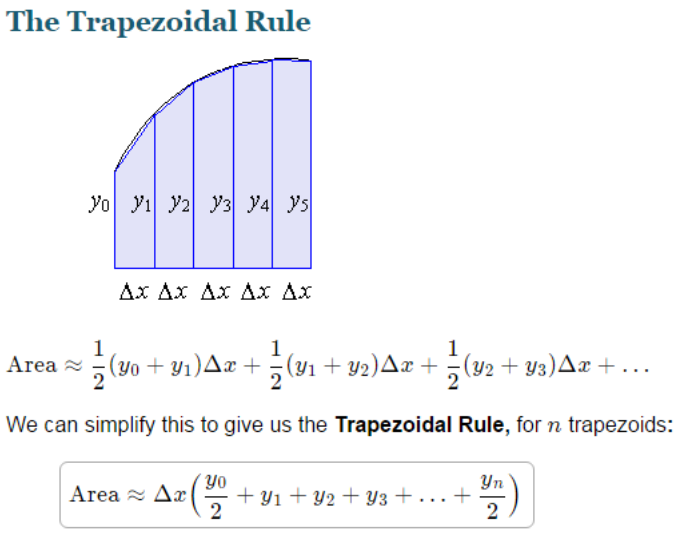


Figure 18 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD} using the equation:

Area_Above_V_{DD} = Total_Area_Above_0V - Area_below_V_{DD}

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DD}

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

LPDDR4 / LPDDR4X (Differential) Test Modes

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot amplitude (Clock Minus)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

103032 [Undershoot amplitude (Clock Minus)]

LPDDR4 Test Mode

503022 [Undershoot amplitude (Clock Minus)]

LPDDR4X (Differential) Test Mode

603022 [Undershoot amplitude (Clock Minus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.5	Table 126	[Maximum peak amplitude allowed for undershoot] [Maximum undershoot area per 1 UI below VSS]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for undershoot area] [Maximum area below V_{SS}]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Test Procedure: **DDR4 Test Mode (for Test ID 103032)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

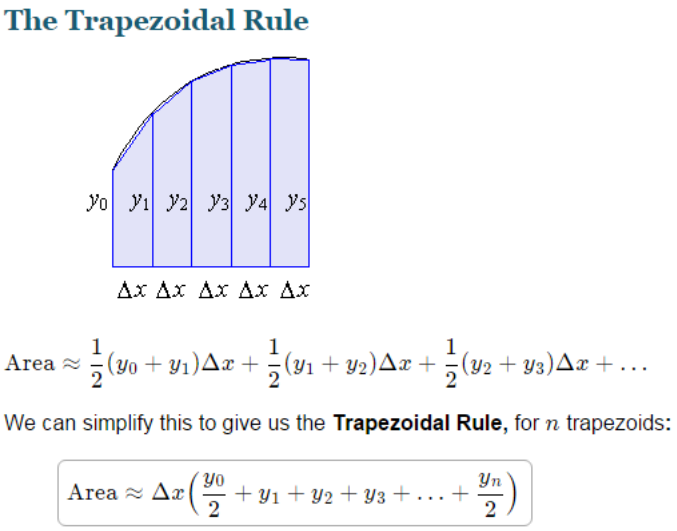


Figure 19 Equation for Total_Area_Above_0V

c To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Total_Area_Below_0V

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

LPDDR4 (for Test ID 503022) / LPDDR4X (Differential) (for Test ID 603022)

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use T_{MIN} and V_{MIN} to get the time-stamp of minimum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to minimize the peak area.

5 Find the edges before and after the Undershoot Point at the GND (~0V) level in order to calculate the maximum undershoot length duration.

6 Calculate Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

7 Calculate Undershoot area (V-ns)

a By calculating area of a triangle using the undershoot width as the triangle base and the undershoot amplitude as the triangle height.

b For Undershoot area, use the equation:

$$\text{Area} = 0.5 \times \text{base} \times \text{height}$$

8 Compare test results with the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area below VSS(Clock Minus)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103033 [Undershoot area below VSS (Clock Minus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.5	Table 126	[Maximum peak amplitude allowed for undershoot] [Maximum undershoot area per 1 UI below VSS]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 Test Mode (for Test ID 103033)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

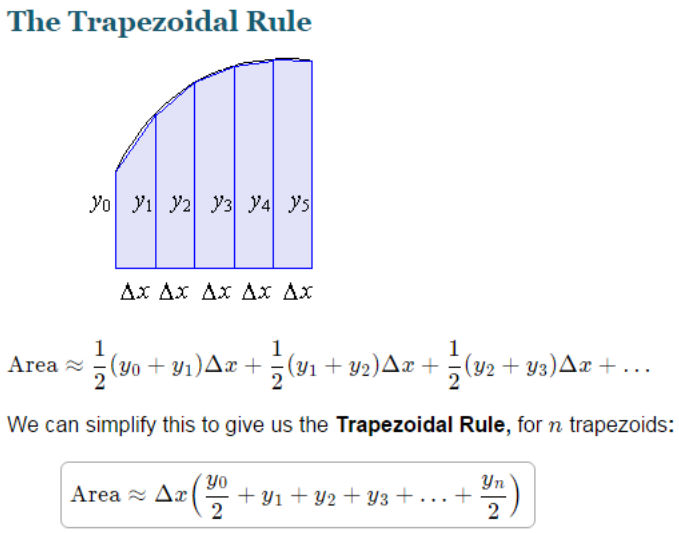


Figure 20 Equation for Total_Area_Above_0V

c To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Total_Area_Below_0V

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area (Clock Minus)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

503023 [Undershoot area (Clock Minus)]

LPDDR4X (Differential) Test Mode

603023 [Undershoot area (Clock Minus)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for undershoot area] [Maximum area below V_{SS}]

Test Overview: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Test Procedure: **LPDDR4 (for Test ID 503023) / LPDDR4X (Differential) (for Test ID 603023)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

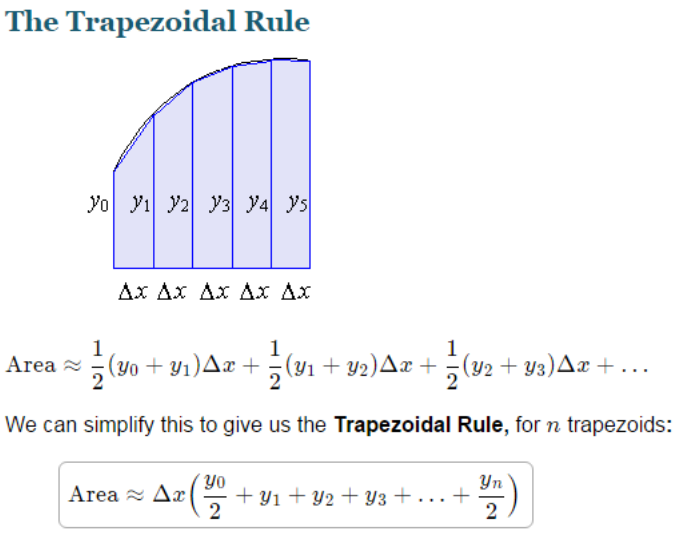


Figure 21 Equation for Total_Area_Above_0V

c To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Total_Area_Below_0V

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

LPDDR4 / LPDDR4X (Differential) Test Modes

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot/Undershoot (Strobe Plus)

Overshoot amplitude (Strobe Plus)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

103006 [Overshoot amplitude (Strobe Plus)]

LPDDR4 Test Mode

503004 [Overshoot amplitude (Strobe Plus)]

LPDDR4X (Differential) Test Mode

603004 [Overshoot amplitude (Strobe Plus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude above VDOS] [Maximum overshoot area per 1 UI above VDOS] [Maximum overshoot area per 1 UI between VDDQ and VDOS]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for overshoot area] [Maximum area above V_{DD}]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform. When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform. When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Test Procedure: **DDR4 (for Test ID 103006)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

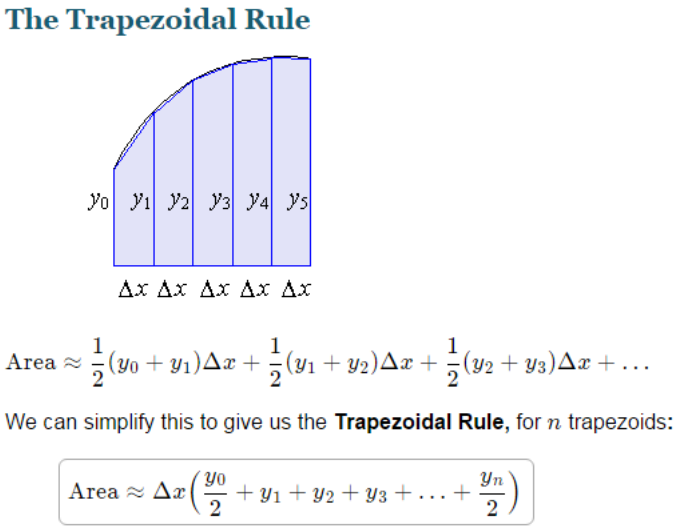


Figure 22 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

$$\text{Area\_Above\_}V_{DDQ} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DDQ}$$

e Evaluate Area_Above_$V_{DDQAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 22).

f Calculate Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ using the equation:

$$\text{Area\_Between\_}V_{DDQ}\text{\_and\_}V_{DDQAbsMax} = \text{Area\_Above\_}V_{DDQ} - \text{Area\_Above\_}V_{DDQAbsMax}$$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDQAbsMax}$
- Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

LPDDR4 (for Test ID 503004) / LPDDR4X (Differential) (for Test ID 603004)

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use T_{MAX} and V_{MAX} to get the time-stamp of maximum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to maximize the peak area.

5 Find the edges before and after the Overshoot Point at the Supply Reference Level in order to calculate the maximum overshoot length duration.
Table 2 shows the supply reference level for each pin group:

Table 3 Supply reference level

PIN	Supply Reference Level
Address and Control pin	V_{DD2}
Data, Strobe and Mask pin	V_{DDQ}
Clock	V_{DD2}

6 Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - \text{Supply Reference Level (refer to Table 2)}$$

7 Calculate Overshoot area (V-ns)

a By calculating area of a triangle using the overshoot width as the triangle base and the overshoot amplitude as the triangle height.

b For Overshoot area, use the equation:

$$\text{Area} = 0.5 \times \text{base} \times \text{height}$$

8 Compare test results with the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area above Max Abs Level(Strobe Plus)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103007 [Overshoot area above Max Abs Level(Strobe Plus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude above VDOS] [Maximum overshoot area per 1 UI above VDOS] [Maximum overshoot area per 1 UI between VDDQ and VDOS]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 (for Test ID 103007)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

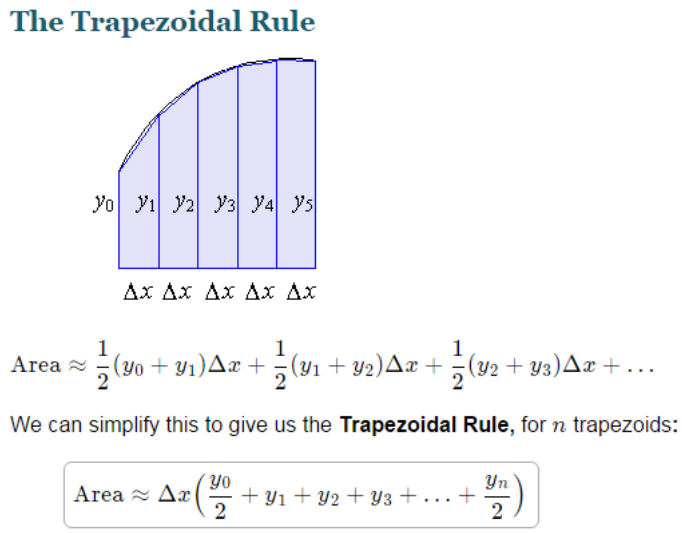


Figure 23 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_0V - Area_below_V_{DDQ}

e Evaluate Area_Above_$V_{DDQAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 23).

f Calculate Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ using the equation:

Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ = Area_Above_V_{DDQ} - Area_Above_$V_{DDQAbsMax}$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDQAbsMax}$
- Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area between VDDQ and Max Abs Level(Strobe Plus)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103008 [Overshoot area between VDDQ and Max Abs Level (Strobe Plus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude above VDOS] [Maximum overshoot area per 1 UI above VDOS] [Maximum overshoot area per 1 UI between VDDQ and VDOS]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform. When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 (for Test ID 103008)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

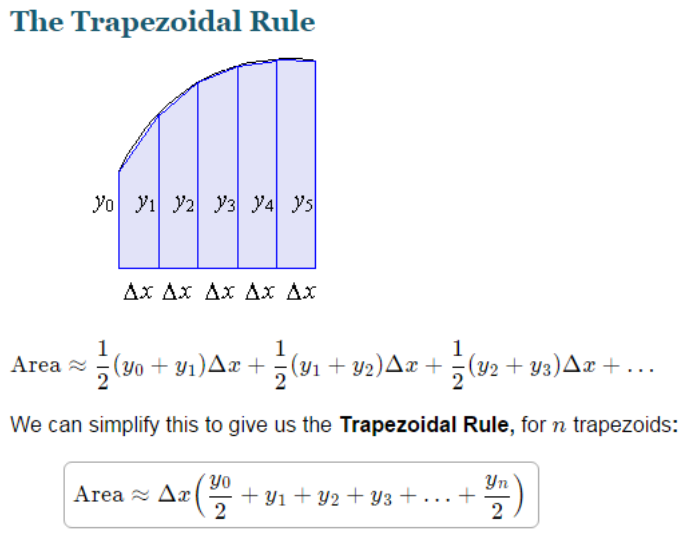


Figure 24 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_0V - Area_below_V_{DDQ}

e Evaluate Area_Above_$V_{DDQAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 24).

f Calculate Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ using the equation:

Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ = Area_Above_V_{DDQ} - Area_Above_$V_{DDQAbsMax}$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDQAbsMax}$
- Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area(Strobe Plus)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

503005 [Overshoot area(Strobe Plus)]

LPDDR4X (Differential) Test Mode

603005 [Overshoot area(Strobe Plus)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for overshoot area] [Maximum area above V_{DD}]

Test Overview: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Test Procedure: **LPDDR4 (for Test ID 503005) / LPDDR4X (Differential) (for Test ID 603005)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

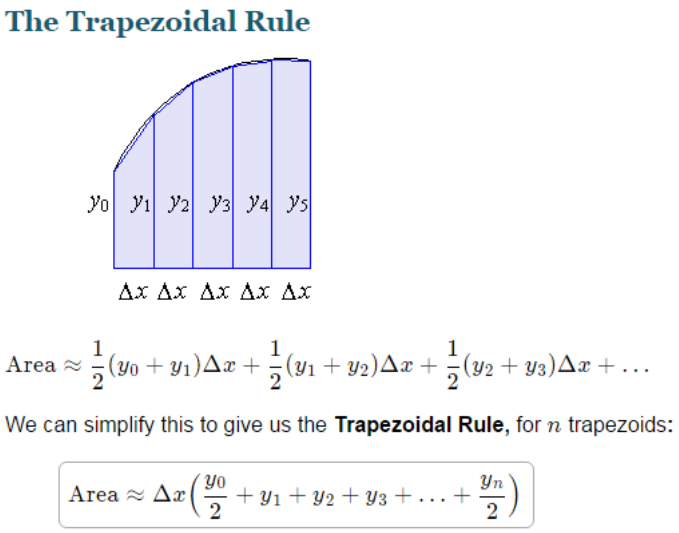


Figure 25 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_0V - Area_below_V_{DDQ}

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DDQ}

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limits.

Expected/ Observable Results:

LPDDR4 / LPDDR4X (Differential) Test Modes

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot amplitude (Strobe Plus)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

103009 [Undershoot amplitude (Strobe Plus)]

LPDDR4 Test Mode

503006 [Undershoot amplitude (Strobe Plus)]

LPDDR4X (Differential) Test Mode

603006 [Undershoot amplitude (Strobe Plus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude below VDUS] [Maximum undershoot area per 1 UI below VDUS] [Maximum undershoot area per 1 UI between VSSQ and VDUS1]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for undershoot area] [Maximum area below V_{SS}]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Test Procedure: **DDR4 Test Mode (for Test ID 103009)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

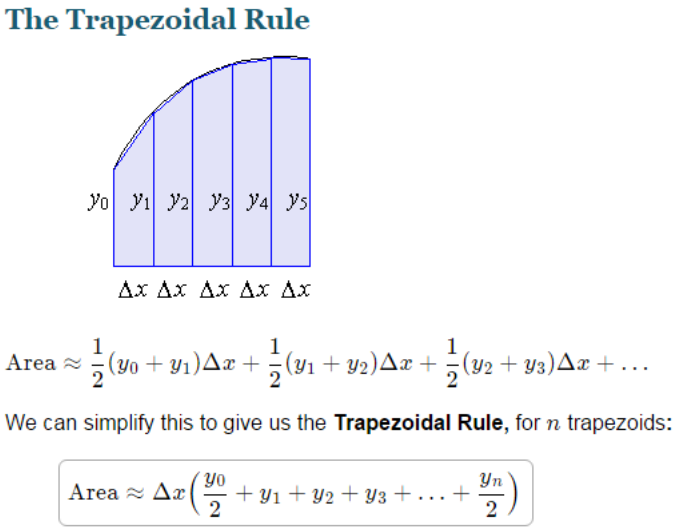


Figure 26 Equation for Total_Area_Above_0V

c Evaluate Area_Below_MinAbsLevel by using Trapezoidal Method Area Calculation (as shown in Figure 26).

d Calculate Area_Between_V_{SSQ}_and_MinAbsLevel using the equation:

Area_Between_V_{SSQ}_and_MinAbsLevel = Total_Area_Belowe_0V - Area_Below_MinAbsLevel

e To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Area_Below_MinAbsLevel
- Area_Between_V_{SSQ}_and_MinAbsLevel

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

LPDDR4 (for Test ID 503006) / LPDDR4X (Differential) (for Test ID 603006)

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use T_{MIN} and V_{MIN} to get the time-stamp of minimum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to minimize the peak area.

5 Find the edges before and after the Undershoot Point at the GND (~0V) level in order to calculate the maximum undershoot length duration.

6 Calculate Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

7 Calculate Undershoot area (V-ns)

a By calculating area of a triangle using the undershoot width as the triangle base and the undershoot amplitude as the triangle height.

b For Undershoot area, use the equation:

$$\text{Area} = 0.5 \times \text{base} \times \text{height}$$

8 Compare test results with the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area below Min Abs Level(Strobe Plus)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103010 [Undershoot area below Min Abs Level (Strobe Plus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude below VDUS] [Maximum undershoot area per 1 UI below VDUS] [Maximum undershoot area per 1 UI between VSSQ and VDUS1]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 Test Mode (for Test ID 103010)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

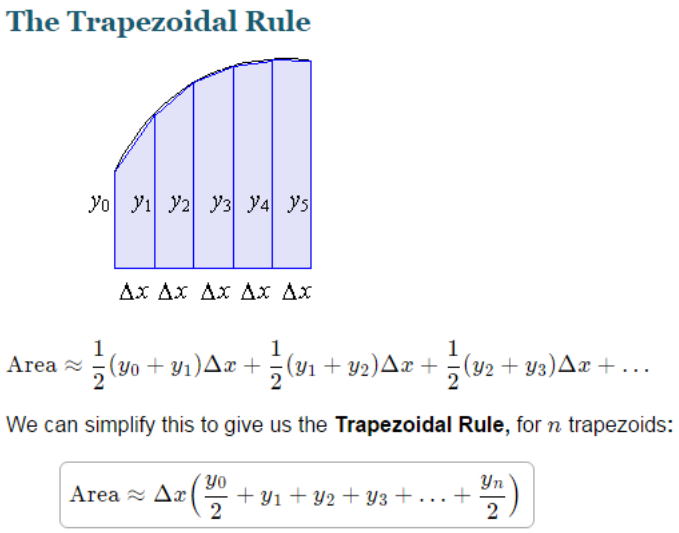


Figure 27 Equation for Total_Area_Above_0V

c Evaluate Area_Below_MinAbsLevel by using Trapezoidal Method Area Calculation (as shown in Figure 27).

d Calculate Area_Between_V_{SSQ}_and_MinAbsLevel using the equation:

Area_Between_V_{SSQ}_and_MinAbsLevel = Total_Area_Belowe_0V - Area_Below_MinAbsLevel

e To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Area_Below_MinAbsLevel
- Area_Between_V_{SSQ}_and_MinAbsLevel

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limits.

Expected/ Observable Results:

DDR4 Test Mode

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area between VSSQ and Min Abs Level(Strobe Plus)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103011 [Undershoot area between VSSQ and Min Abs Level (Strobe Plus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude below VDUS] [Maximum undershoot area per 1 UI below VDUS] [Maximum undershoot area per 1 UI between VSSQ and VDUS1]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 Test Mode (for Test ID 103011)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

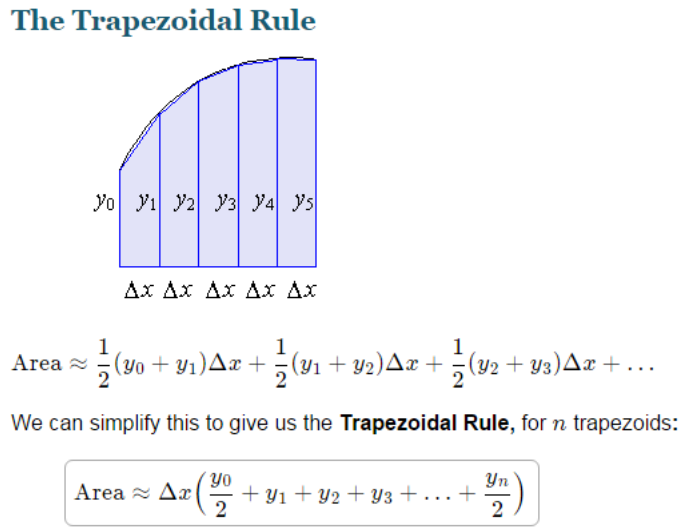


Figure 28 Equation for Total_Area_Above_0V

c Evaluate Area_Below_MinAbsLevel by using Trapezoidal Method Area Calculation (as shown in Figure 28).

d Calculate Area_Between_V_{SSQ}_and_MinAbsLevel using the equation:

Area_Between_V_{SSQ}_and_MinAbsLevel = Total_Area_Belowe_0V - Area_Below_MinAbsLevel

e To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Area_Below_MinAbsLevel
- Area_Between_V_{SSQ}_and_MinAbsLevel

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area (Strobe Plus)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

503007 [Undershoot area(Strobe Plus)]

LPDDR4X (Differential) Test Mode

603007 [Undershoot area(Strobe Plus)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for undershoot area] [Maximum area below V_{SS}]

Test Overview: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Test Procedure: **LPDDR4 (for Test ID 503007) / LPDDR4X (Differential) (for Test ID 603007)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

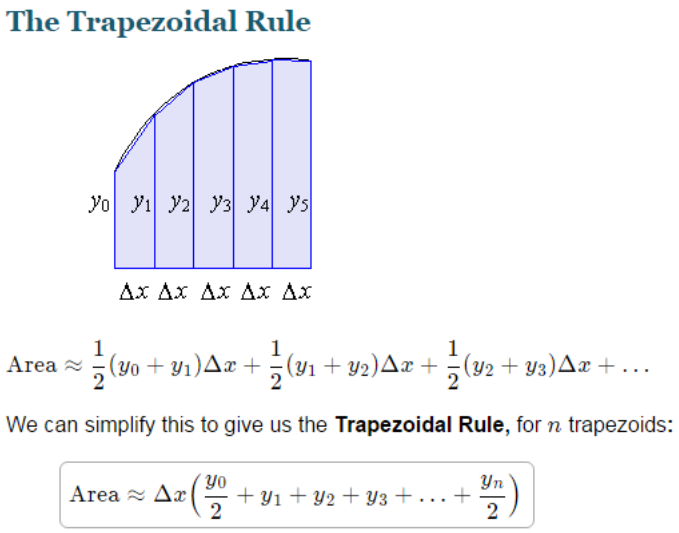


Figure 29 Equation for Total_Area_Above_0V

c Evaluate Area_Below_V_{SSQ} by using Trapezoidal Method Area Calculation (as shown in Figure 27).

d Calculate Area_Between_V_{SSQ}_and_MinAbsLevel using the equation:

Area_Between_V_{SSQ}_and_MinAbsLevel = Total_Area_Belowe_0V - Area_Below_MinAbsLevel

e To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Area_Below_V_{SSQ}

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limits.

Expected/ Observable Results:

LPDDR4 / LPDDR4X (Differential) Test Modes

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot/Undershoot (Strobe Minus)

Overshoot amplitude (Strobe Minus)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

103012 [Overshoot amplitude (Strobe Minus)]

LPDDR4 Test Mode

503008 [Overshoot amplitude (Strobe Minus)]

LPDDR4X (Differential) Test Mode

603008 [Overshoot amplitude (Strobe Minus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude above VDOS] [Maximum overshoot area per 1 UI above VDOS] [Maximum overshoot area per 1 UI between VDDQ and VDOS]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for overshoot area] [Maximum area above V_{DD}]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Test Procedure: **DDR4 (for Test ID 103012)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

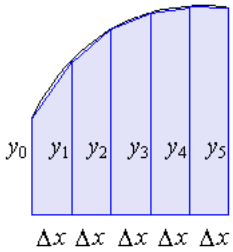
$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

The Trapezoidal Rule



$$\text{Area} \approx \frac{1}{2}(y_0 + y_1)\Delta x + \frac{1}{2}(y_1 + y_2)\Delta x + \frac{1}{2}(y_2 + y_3)\Delta x + \ldots$$

We can simplify this to give us the **Trapezoidal Rule**, for n trapezoids:

$$\text{Area} \approx \Delta x\left(\frac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + \frac{y_n}{2}\right)$$

Figure 30 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

$$\text{Area\_Above\_}V_{DDQ} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DDQ}$$

e Evaluate Area_Above_$V_{DDQAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 22).

f Calculate Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ using the equation:

$$\text{Area\_Between\_}V_{DDQ}\text{\_and\_}V_{DDQAbsMax} = \text{Area\_Above\_}V_{DDQ} - \text{Area\_Above\_}V_{DDQAbsMax}$$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDQAbsMax}$
- Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

LPDDR4 (for Test ID 503008) / LPDDR4X (Differential) (for Test ID 603008)

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use T_{MAX} and V_{MAX} to get the time-stamp of maximum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to maximize the peak area.

5 Find the edges before and after the Overshoot Point at the Supply Reference Level in order to calculate the maximum overshoot length duration.
Table 2 shows the supply reference level for each pin group:

Table 4 Supply reference level

PIN	Supply Reference Level
Address and Control pin	V_{DD2}
Data, Strobe and Mask pin	V_{DDQ}
Clock	V_{DD2}

6 Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - \text{Supply Reference Level (refer to Table 2)}$$

7 Calculate Overshoot area (V-ns)

a By calculating area of a triangle using the overshoot width as the triangle base and the overshoot amplitude as the triangle height.

b For Overshoot area, use the equation:

$$\text{Area} = 0.5 \times \text{base} \times \text{height}$$

8 Compare test results with the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area above Max Abs Level(Strobe Minus)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103013 [Overshoot area above Max Abs Level(Strobe Minus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude above VDOS] [Maximum overshoot area per 1 UI above VDOS] [Maximum overshoot area per 1 UI between VDDQ and VDOS]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 (for Test ID 103013)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

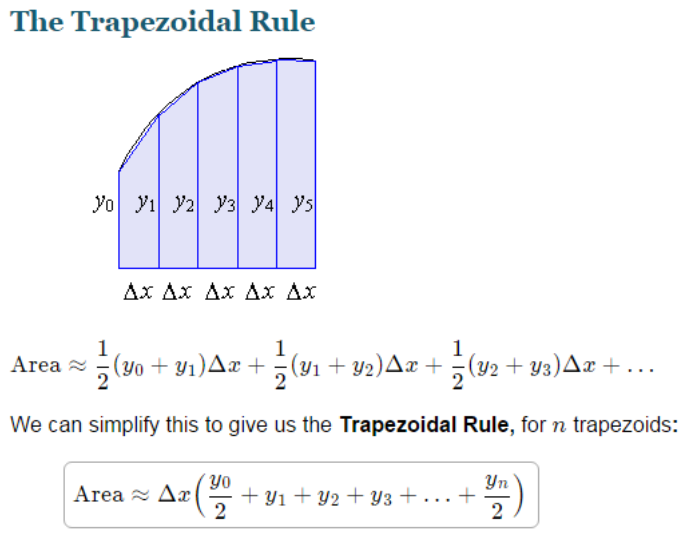


Figure 31 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_0V - Area_below_V_{DDQ}

e Evaluate Area_Above_$V_{DDQAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 23).

f Calculate Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ using the equation:

Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ = Area_Above_V_{DDQ} - Area_Above_$V_{DDQAbsMax}$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDQAbsMax}$
- Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area between VDDQ and Max Abs Level(Strobe Minus)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103014 [Overshoot area between VDDQ and Max Abs Level (Strobe Minus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude above VDOS] [Maximum overshoot area per 1 UI above VDOS] [Maximum overshoot area per 1 UI between VDDQ and VDOS]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 (for Test ID 103014)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

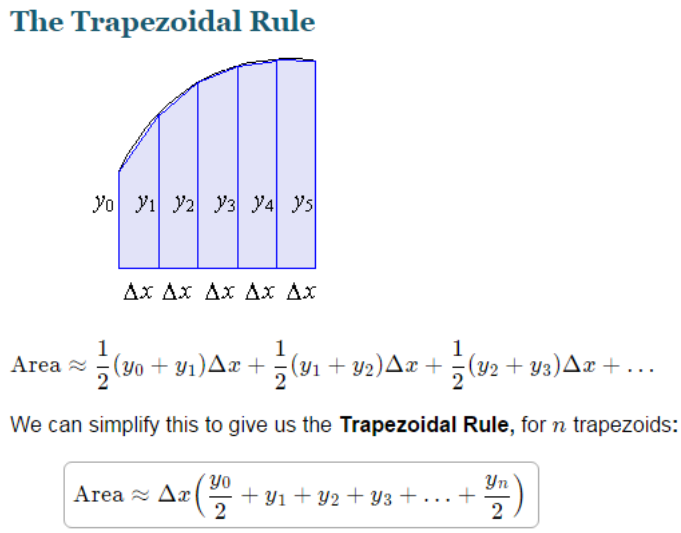


Figure 32 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_0V - Area_below_V_{DDQ}

e Evaluate Area_Above_$V_{DDQAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 24).

f Calculate Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ using the equation:

Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ = Area_Above_V_{DDQ} - Area_Above_$V_{DDQAbsMax}$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDQAbsMax}$
- Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area(Strobe Minus)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

503009 [Overshoot area(Strobe Minus)]

LPDDR4X (Differential) Test Mode

603009 [Overshoot area(Strobe Minus)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for overshoot area] [Maximum area above V_{DD}]

Test Overview: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Test Procedure: **LPDDR4 (for Test ID 503009) / LPDDR4X (Differential) (for Test ID 603009)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

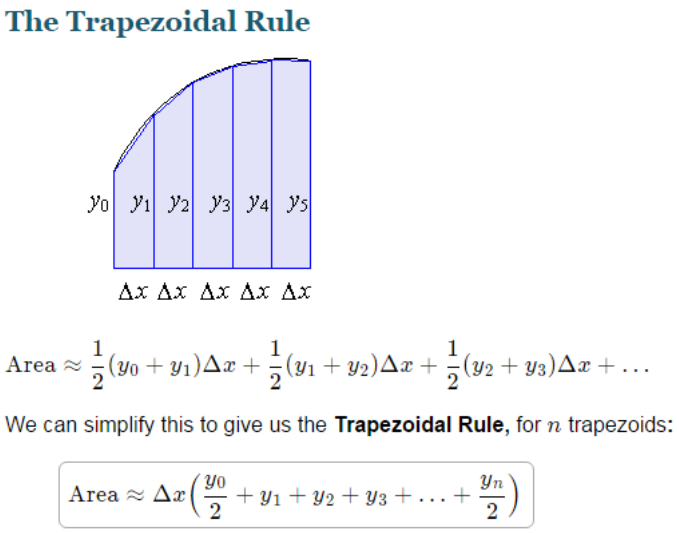


Figure 33 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_0V - Area_below_V_{DDQ}

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DDQ}

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limits.

Expected/ Observable Results:

LPDDR4 / LPDDR4X (Differential) Test Modes

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot amplitude (Strobe Minus)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

103015 [Undershoot amplitude (Strobe Minus)]

LPDDR4 Test Mode

503010 [Undershoot amplitude (Strobe Minus)]

LPDDR4X (Differential) Test Mode

603010 [Undershoot amplitude (Strobe Minus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude below VDUS] [Maximum undershoot area per 1 UI below VDUS] [Maximum undershoot area per 1 UI between VSSQ and VDUS1]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for undershoot area] [Maximum area below V_{SS}]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Test Procedure: **DDR4 Test Mode (for Test ID 103015)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

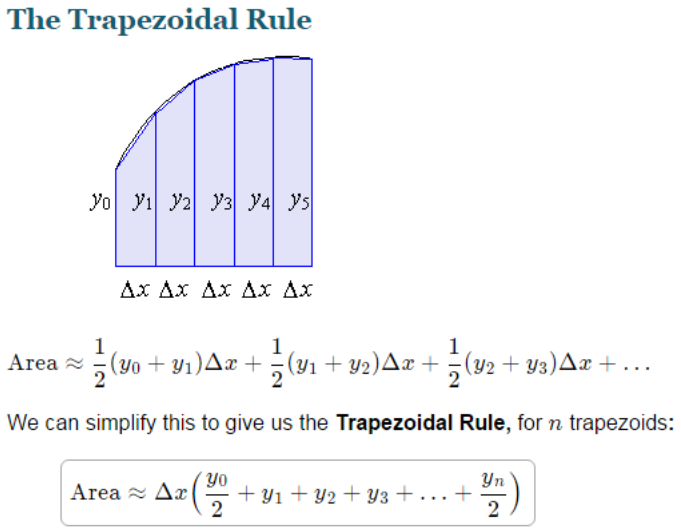


Figure 34 Equation for Total_Area_Above_0V

c Evaluate Area_Below_MinAbsLevel by using Trapezoidal Method Area Calculation (as shown in Figure 26).

d Calculate Area_Between_V_{SSQ}_and_MinAbsLevel using the equation:

Area_Between_V_{SSQ}_and_MinAbsLevel = Total_Area_Belowe_0V - Area_Below_MinAbsLevel

e To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Area_Below_MinAbsLevel
- Area_Between_V_{SSQ}_and_MinAbsLevel

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

LPDDR4 (for Test ID 503010) / LPDDR4X (Differential) (for Test ID 603010)

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use T_{MIN} and V_{MIN} to get the time-stamp of minimum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to minimize the peak area.

5 Find the edges before and after the Undershoot Point at the GND (~0V) level in order to calculate the maximum undershoot length duration.

6 Calculate Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

7 Calculate Undershoot area (V-ns)

a By calculating area of a triangle using the undershoot width as the triangle base and the undershoot amplitude as the triangle height.

b For Undershoot area, use the equation:

$$\text{Area} = 0.5 \times \text{base} \times \text{height}$$

8 Compare test results with the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area below Min Abs Level(Strobe Minus)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103016 [Undershoot area below Min Abs Level (Strobe Minus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude below VDUS] [Maximum undershoot area per 1 UI below VDUS] [Maximum undershoot area per 1 UI between VSSQ and VDUS1]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 Test Mode (for Test ID 103016)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

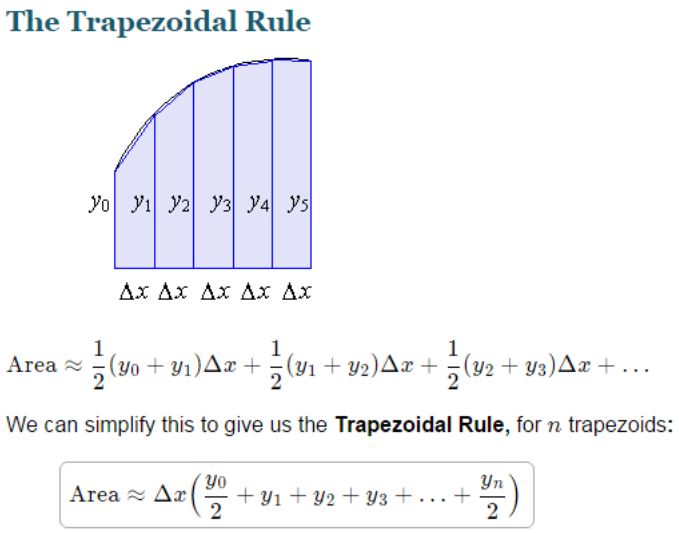


Figure 35 Equation for Total_Area_Above_0V

c Evaluate Area_Below_MinAbsLevel by using Trapezoidal Method Area Calculation (as shown in Figure 27).

d Calculate Area_Between_V_{SSQ}_and_MinAbsLevel using the equation:

Area_Between_V_{SSQ}_and_MinAbsLevel = Total_Area_Belowe_0V - Area_Below_MinAbsLevel

e To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Area_Below_MinAbsLevel
- Area_Between_V_{SSQ}_and_MinAbsLevel

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limits.

Expected/ Observable Results:

DDR4 Test Mode

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area between VSSQ and Min Abs Level(Strobe Minus)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103017 [Undershoot area between VSSQ and Min Abs Level (Strobe Minus)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude below VDUS] [Maximum undershoot area per 1 UI below VDUS] [Maximum undershoot area per 1 UI between VSSQ and VDUS1]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 Test Mode (for Test ID 103017)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

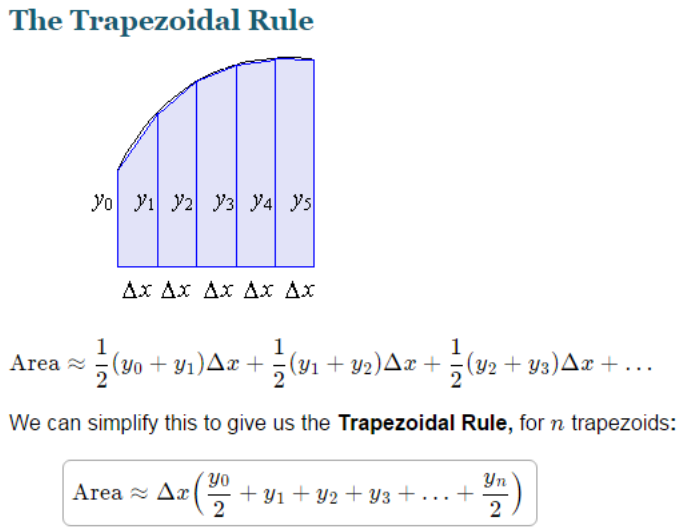


Figure 36 Equation for Total_Area_Above_0V

c Evaluate Area_Below_MinAbsLevel by using Trapezoidal Method Area Calculation (as shown in Figure 28).

d Calculate Area_Between_V_{SSQ}_and_MinAbsLevel using the equation:

Area_Between_V_{SSQ}_and_MinAbsLevel = Total_Area_Belowe_0V - Area_Below_MinAbsLevel

e To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Area_Below_MinAbsLevel
- Area_Between_V_{SSQ}_and_MinAbsLevel

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area (Strobe Minus)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

503011 [Undershoot area(Strobe Minus)]

LPDDR4X (Differential) Test Mode

603011 [Undershoot area(Strobe Minus)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for undershoot area] [Maximum area below V_{SS}]

Test Overview: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Test Procedure: **LPDDR4 (for Test ID 503011) / LPDDR4X (Differential) (for Test ID 603011)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

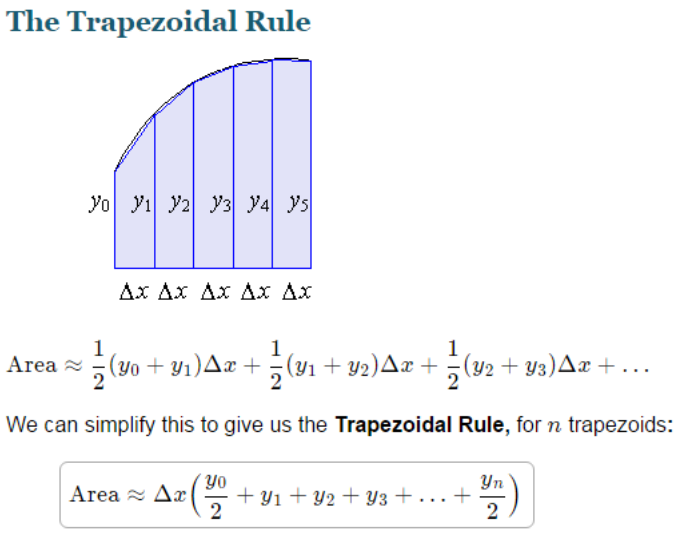


Figure 37 Equation for Total_Area_Above_0V

c Evaluate Area_Below_V_{SSQ} by using Trapezoidal Method Area Calculation (as shown in Figure 27).

d Calculate Area_Between_V_{SSQ}_and_MinAbsLevel using the equation:

Area_Between_V_{SSQ}_and_MinAbsLevel = Total_Area_Belowe_0V - Area_Below_MinAbsLevel

e To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Area_Below_V_{SSQ}

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limits.

Expected/ Observable Results:

LPDDR4 / LPDDR4X (Differential) Test Modes

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot/Undershoot (Data)

Overshoot amplitude (Data)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

103000 [Overshoot amplitude (Data)]

LPDDR4 Test Mode

503000 [Overshoot amplitude (Data)]

LPDDR4X (Differential) Test Mode

603000 [Overshoot amplitude (Data)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude above VDOS] [Maximum overshoot area per 1 UI above VDOS] [Maximum overshoot area per 1 UI between VDDQ and VDOS]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for overshoot area] [Maximum area above V_{DD}]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Test Procedure: **DDR4 (for Test ID 103000)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

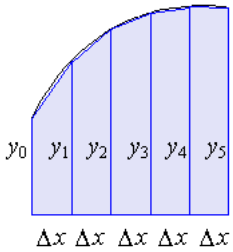
$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

The Trapezoidal Rule



$$\text{Area} \approx \frac{1}{2}(y_0 + y_1)\Delta x + \frac{1}{2}(y_1 + y_2)\Delta x + \frac{1}{2}(y_2 + y_3)\Delta x + \ldots$$

We can simplify this to give us the **Trapezoidal Rule**, for n trapezoids:

$$\text{Area} \approx \Delta x\left(\frac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + \frac{y_n}{2}\right)$$

Figure 38 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

$$\text{Area\_Above\_}V_{DDQ} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DDQ}$$

e Evaluate Area_Above_$V_{DDQAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 22).

f Calculate Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ using the equation:

$$\text{Area\_Between\_}V_{DDQ}\text{\_and\_}V_{DDQAbsMax} = \text{Area\_Above\_}V_{DDQ} - \text{Area\_Above\_}V_{DDQAbsMax}$$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDQAbsMax}$
- Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

LPDDR4 (for Test ID 503000) / LPDDR4X (Differential) (for Test ID 603000)

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use T_{MAX} and V_{MAX} to get the time-stamp of maximum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to maximize the peak area.

5 Find the edges before and after the Overshoot Point at the Supply Reference Level in order to calculate the maximum overshoot length duration.
Table 2 shows the supply reference level for each pin group:

Table 5 Supply reference level

PIN	Supply Reference Level
Address and Control pin	V_{DD2}
Data, Strobe and Mask pin	V_{DDQ}
Clock	V_{DD2}

6 Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = V_{MAX} - Supply Reference Level (refer to Table 2)

7 Calculate Overshoot area (V-ns)

a By calculating area of a triangle using the overshoot width as the triangle base and the overshoot amplitude as the triangle height.

b For Overshoot area, use the equation:

Area = 0.5 x base x height

8 Compare test results with the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area above Max Abs Level(Data)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103001 [Overshoot area above Max Abs Level(Data)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude above VDOS] [Maximum overshoot area per 1 UI above VDOS] [Maximum overshoot area per 1 UI between VDDQ and VDOS]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 (for Test ID 103001)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

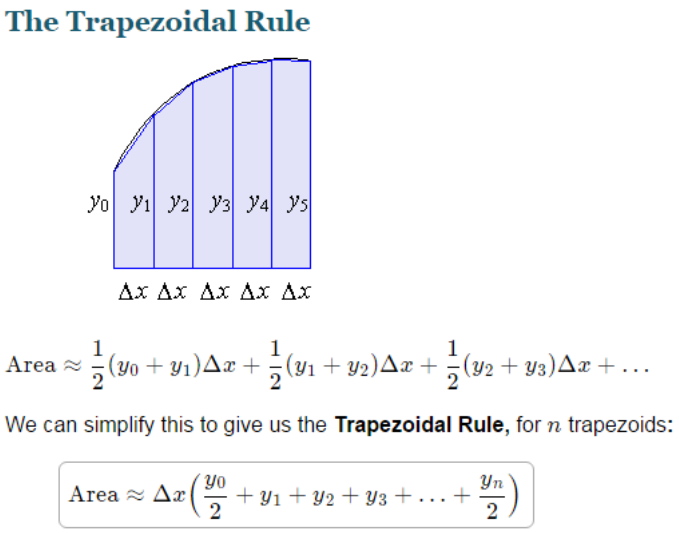


Figure 39 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_0V - Area_below_V_{DDQ}

e Evaluate Area_Above_$V_{DDQAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 23).

f Calculate Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ using the equation:

Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ = Area_Above_V_{DDQ} - Area_Above_$V_{DDQAbsMax}$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDQAbsMax}$
- Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area between VDDQ and Max Abs Level(Data)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103002 [Overshoot area between VDDQ and Max Abs Level (Data)]

103008 [Overshoot area between VDDQ and Max Abs Level (Strobe Plus)]

103014 [Overshoot area between VDDQ and Max Abs Level (Strobe Minus)]

103020 [Overshoot area between VDDQ and Max Abs Level (Data Mask)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude above VDOS] [Maximum overshoot area per 1 UI above VDOS] [Maximum overshoot area per 1 UI between VDDQ and VDOS]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 (for Test ID 103002)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

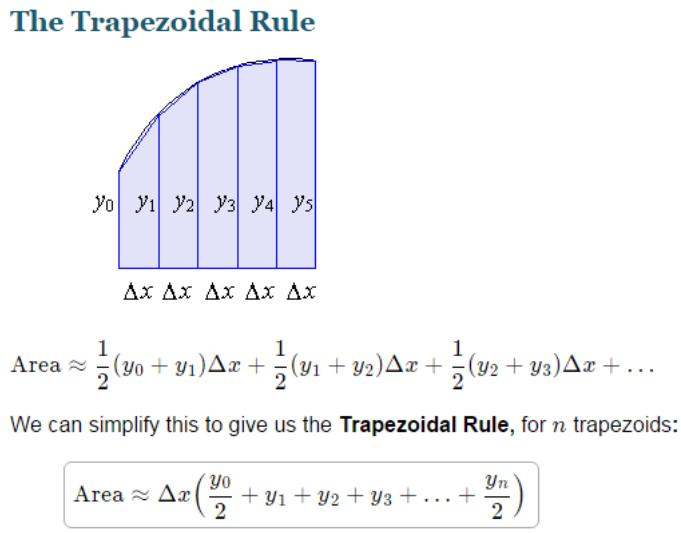


Figure 40 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_0V - Area_below_V_{DDQ}

e Evaluate Area_Above_$V_{DDQAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 24).

f Calculate Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ using the equation:

Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ = Area_Above_V_{DDQ} - Area_Above_$V_{DDQAbsMax}$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDQAbsMax}$
- Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area(Data)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

503001 [Overshoot area(Data)]

LPDDR4X (Differential) Test Mode

603001 [Overshoot area(Data)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for overshoot area] [Maximum area above V_{DD}]

Test Overview: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Test Procedure: **LPDDR4 (for Test ID 503001) / LPDDR4X (Differential) (for Test ID 603001)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

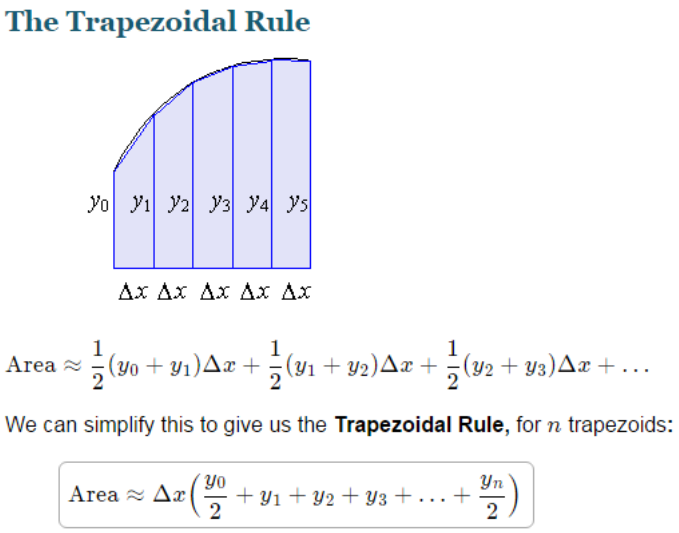


Figure 41 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_0V - Area_below_V_{DDQ}

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DDQ}

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limits.

Expected/ Observable Results:

LPDDR4 / LPDDR4X (Differential) Test Modes

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot amplitude (Data)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

103003 [Undershoot amplitude (Data)]

LPDDR4 Test Mode

503002 [Undershoot amplitude (Data)]

LPDDR4X (Differential) Test Mode

603002 [Undershoot amplitude (Data)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude below VDUS] [Maximum undershoot area per 1 UI below VDUS] [Maximum undershoot area per 1 UI between VSSQ and VDUS1]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for undershoot area] [Maximum area below V_{SS}]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Test Procedure: **DDR4 Test Mode (for Test ID 103003)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

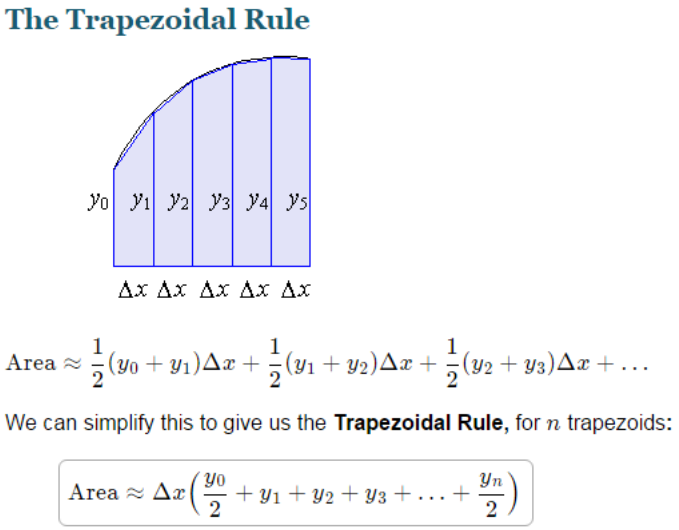


Figure 42 Equation for Total_Area_Above_0V

c Evaluate Area_Below_MinAbsLevel by using Trapezoidal Method Area Calculation (as shown in Figure 26).

d Calculate Area_Between_V_{SSQ}_and_MinAbsLevel using the equation:

Area_Between_V_{SSQ}_and_MinAbsLevel = Total_Area_Belowe_0V - Area_Below_MinAbsLevel

e To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Area_Below_MinAbsLevel
- Area_Between_V_{SSQ}_and_MinAbsLevel

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

LPDDR4 (for Test ID 503002) / LPDDR4X (Differential) (for Test ID 603002)

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use T_{MIN} and V_{MIN} to get the time-stamp of minimum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to minimize the peak area.

5 Find the edges before and after the Undershoot Point at the GND (~0V) level in order to calculate the maximum undershoot length duration.

6 Calculate Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

7 Calculate Undershoot area (V-ns)

a By calculating area of a triangle using the undershoot width as the triangle base and the undershoot amplitude as the triangle height.

b For Undershoot area, use the equation:

$$\text{Area} = 0.5 \times \text{base} \times \text{height}$$

8 Compare test results with the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area below Min Abs Level(Data)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103004 [Undershoot area below Min Abs Level (Data)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude below VDUS] [Maximum undershoot area per 1 UI below VDUS] [Maximum undershoot area per 1 UI between VSSQ and VDUS1]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 Test Mode (for Test ID 103004)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

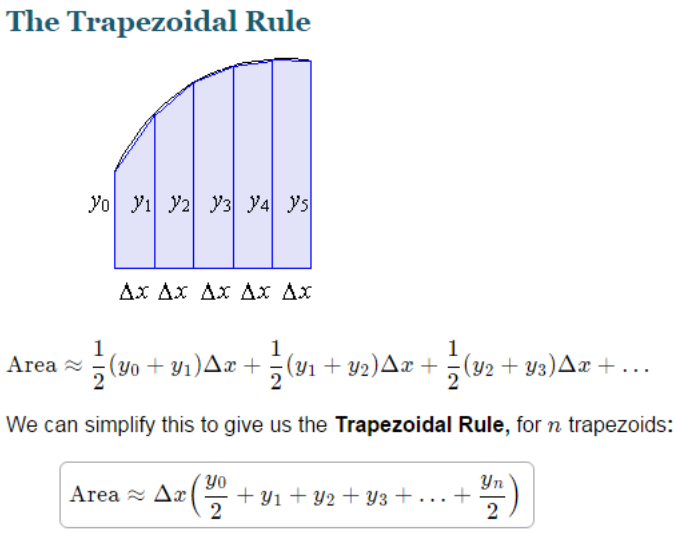


Figure 43 Equation for Total_Area_Above_0V

c Evaluate Area_Below_MinAbsLevel by using Trapezoidal Method Area Calculation (as shown in Figure 27).

d Calculate Area_Between_V_{SSQ}_and_MinAbsLevel using the equation:

Area_Between_V_{SSQ}_and_MinAbsLevel = Total_Area_Belowe_0V - Area_Below_MinAbsLevel

e To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Area_Below_MinAbsLevel
- Area_Between_V_{SSQ}_and_MinAbsLevel

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limits.

Expected/ Observable Results:

DDR4 Test Mode

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area between VSSQ and Min Abs Level(Data)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103005 [Undershoot area between VSSQ and Min Abs Level (Data)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude below VDUS] [Maximum undershoot area per 1 UI below VDUS] [Maximum undershoot area per 1 UI between VSSQ and VDUS1]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 Test Mode (for Test ID 103005)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

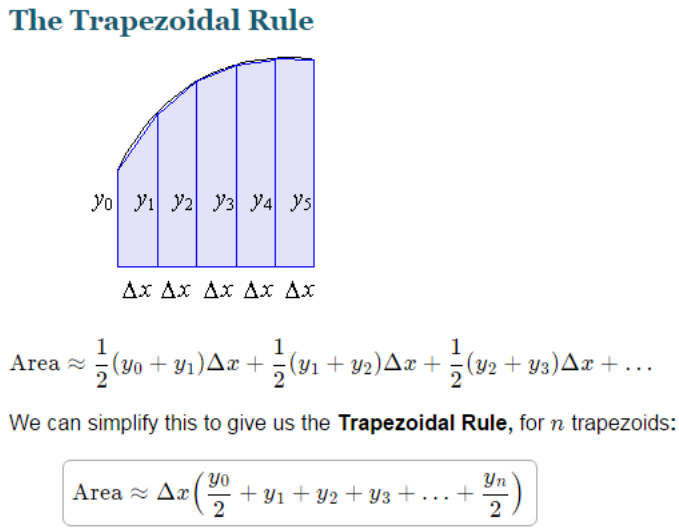


Figure 44 Equation for Total_Area_Above_0V

c Evaluate Area_Below_MinAbsLevel by using Trapezoidal Method Area Calculation (as shown in Figure 28).

d Calculate Area_Between_V_{SSQ}_and_MinAbsLevel using the equation:

Area_Between_V_{SSQ}_and_MinAbsLevel = Total_Area_Belowe_0V - Area_Below_MinAbsLevel

e To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Area_Below_MinAbsLevel
- Area_Between_V_{SSQ}_and_MinAbsLevel

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area (Data)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

503003 [Undershoot area(Data)]

LPDDR4X (Differential) Test Mode

603003 [Undershoot area(Data)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for undershoot area] [Maximum area below V_{SS}]

Test Overview: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Test Procedure: **LPDDR4 (for Test ID 503003) / LPDDR4X (Differential) (for Test ID 603003)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

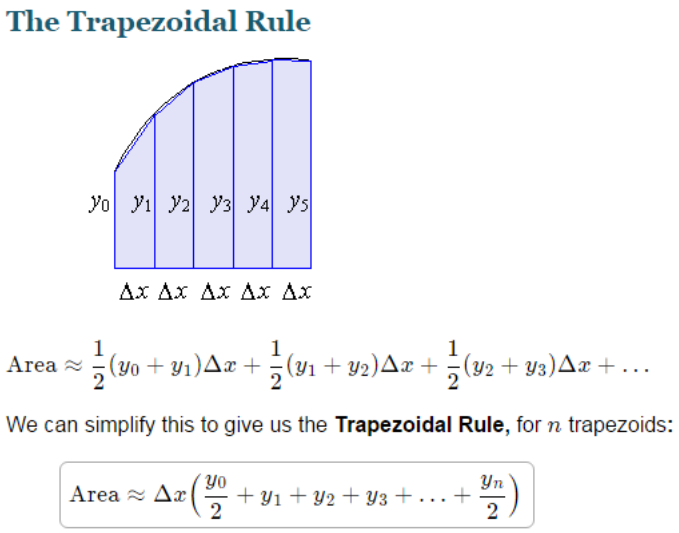


Figure 45 Equation for Total_Area_Above_0V

c Evaluate Area_Below_V_{SSQ} by using Trapezoidal Method Area Calculation (as shown in Figure 27).

d Calculate Area_Between_V_{SSQ}_and_MinAbsLevel using the equation:

Area_Between_V_{SSQ}_and_MinAbsLevel = Total_Area_Belowe_0V - Area_Below_MinAbsLevel

e To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Area_Below_V_{SSQ}

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limits.

Expected/ Observable Results:

LPDDR4 / LPDDR4X (Differential) Test Modes

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot/Undershoot (Data Mask)

Overshoot amplitude (Data Mask)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

103018 [Overshoot amplitude (Data Mask)]

LPDDR4 Test Mode

503012 [Overshoot amplitude (Data Mask)]

LPDDR4X (Differential) Test Mode

603012 [Overshoot amplitude (Data Mask)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude above VDOS] [Maximum overshoot area per 1 UI above VDOS] [Maximum overshoot area per 1 UI between VDDQ and VDOS]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for overshoot area] [Maximum area above V_{DD}]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Test Procedure: **DDR4 (for Test ID 103018)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

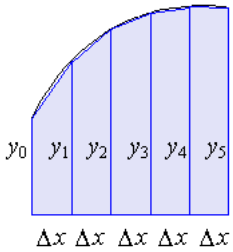
$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

The Trapezoidal Rule



$$\text{Area} \approx \frac{1}{2}(y_0 + y_1)\Delta x + \frac{1}{2}(y_1 + y_2)\Delta x + \frac{1}{2}(y_2 + y_3)\Delta x + \ldots$$

We can simplify this to give us the **Trapezoidal Rule**, for n trapezoids:

$$\text{Area} \approx \Delta x\left(\frac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + \frac{y_n}{2}\right)$$

Figure 46 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

$$\text{Area\_Above\_}V_{DDQ} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DDQ}$$

e Evaluate Area_Above_$V_{DDQAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 22).

f Calculate Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ using the equation:

$$\text{Area\_Between\_}V_{DDQ}\text{\_and\_}V_{DDQAbsMax} = \text{Area\_Above\_}V_{DDQ} - \text{Area\_Above\_}V_{DDQAbsMax}$$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDQAbsMax}$
- Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

LPDDR4 (for Test ID 503012) / LPDDR4X (Differential) (for Test ID 603012)

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use T_{MAX} and V_{MAX} to get the time-stamp of maximum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to maximize the peak area.

5 Find the edges before and after the Overshoot Point at the Supply Reference Level in order to calculate the maximum overshoot length duration.
Table 2 shows the supply reference level for each pin group:

Table 6 Supply reference level

PIN	Supply Reference Level
Address and Control pin	V_{DD2}
Data, Strobe and Mask pin	V_{DDQ}
Clock	V_{DD2}

6 Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - \text{Supply Reference Level (refer to Table 2)}$$

7 Calculate Overshoot area (V-ns)

a By calculating area of a triangle using the overshoot width as the triangle base and the overshoot amplitude as the triangle height.

b For Overshoot area, use the equation:

$$\text{Area} = 0.5 \times \text{base} \times \text{height}$$

8 Compare test results with the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area above Max Abs Level(Data Mask)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103019 [Overshoot area above Max Abs Level(Data Mask)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude above VDOS] [Maximum overshoot area per 1 UI above VDOS] [Maximum overshoot area per 1 UI between VDDQ and VDOS]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 (for Test ID 103019)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

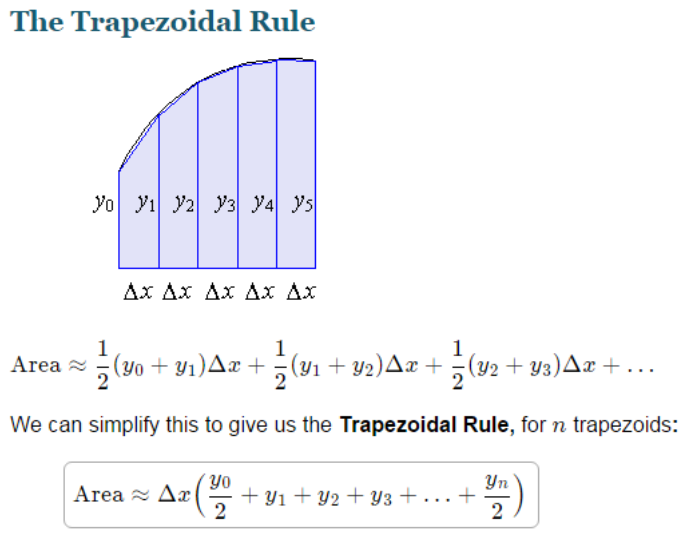


Figure 47 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_0V - Area_below_V_{DDQ}

e Evaluate Area_Above_$V_{DDQAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 23).

f Calculate Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ using the equation:

Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ = Area_Above_V_{DDQ} - Area_Above_$V_{DDQAbsMax}$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDQAbsMax}$
- Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area between VDDQ and Max Abs Level(Data Mask)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103020 [Overshoot area between VDDQ and Max Abs Level (Data Mask)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude above VDOS] [Maximum overshoot area per 1 UI above VDOS] [Maximum overshoot area per 1 UI between VDDQ and VDOS]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 (for Test ID 103020)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

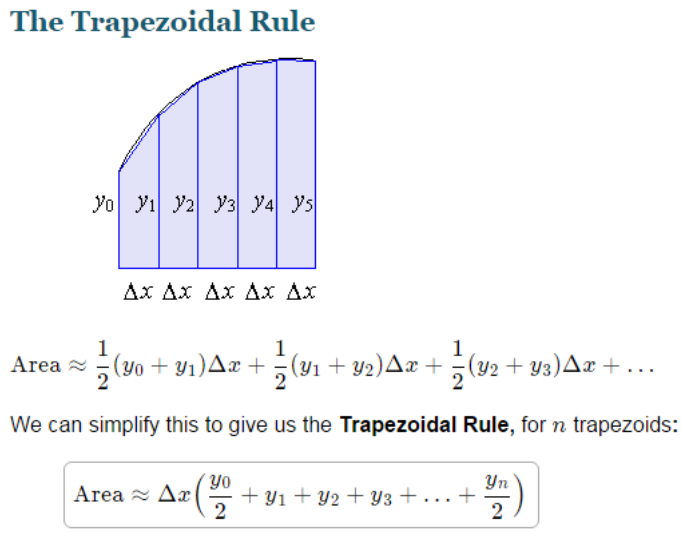


Figure 48 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_0V - Area_below_V_{DDQ}

e Evaluate Area_Above_$V_{DDQAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 24).

f Calculate Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ using the equation:

Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$ = Area_Above_V_{DDQ} - Area_Above_$V_{DDQAbsMax}$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDQAbsMax}$
- Area_Between_V_{DDQ}_and_$V_{DDQAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area(Data Mask)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

503013 [Overshoot area(Data Mask)]

LPDDR4X (Differential) Test Mode

603013 [Overshoot area(Data Mask)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for overshoot area] [Maximum area above V_{DD}]

Test Overview: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Test Procedure: **LPDDR4 (for Test ID 503013) / LPDDR4X (Differential) (for Test ID 603013)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

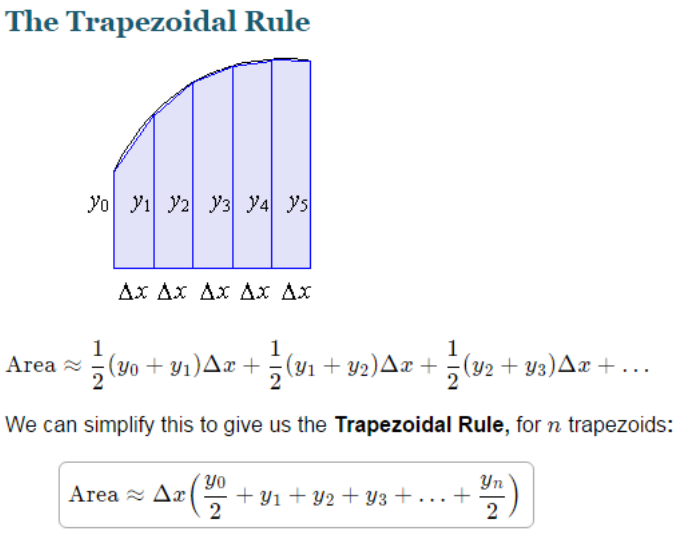


Figure 49 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_0V - Area_below_V_{DDQ}

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DDQ}

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limits.

Expected/ Observable Results:

LPDDR4 / LPDDR4X (Differential) Test Modes

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot amplitude (Data Mask)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

103021 [Undershoot amplitud=e (Data Mask)]

LPDDR4 Test Mode

503014 [Undershoot amplitude (Data Mask)]

LPDDR4X (Differential) Test Mode

603014 [Undershoot amplitude (Data Mask)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude below VDUS] [Maximum undershoot area per 1 UI below VDUS] [Maximum undershoot area per 1 UI between VSSQ and VDUS1]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for undershoot area] [Maximum area below V_{SS}]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Test Procedure: **DDR4 Test Mode (for Test ID 103021)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

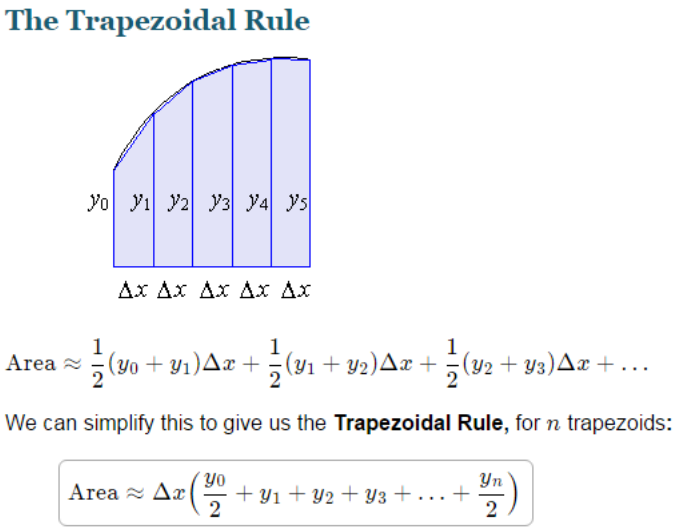


Figure 50 Equation for Total_Area_Above_0V

c Evaluate Area_Below_MinAbsLevel by using Trapezoidal Method Area Calculation (as shown in Figure 26).

d Calculate Area_Between_V_{SSQ}_and_MinAbsLevel using the equation:

Area_Between_V_{SSQ}_and_MinAbsLevel = Total_Area_Belowe_0V - Area_Below_MinAbsLevel

e To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Area_Below_MinAbsLevel
- Area_Between_V_{SSQ}_and_MinAbsLevel

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

LPDDR4 (for Test ID 503014) / LPDDR4X (Differential) (for Test ID 603014)

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use T_{MIN} and V_{MIN} to get the time-stamp of minimum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to minimize the peak area.

5 Find the edges before and after the Undershoot Point at the GND (~0V) level in order to calculate the maximum undershoot length duration.

6 Calculate Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

7 Calculate Undershoot area (V-ns)

a By calculating area of a triangle using the undershoot width as the triangle base and the undershoot amplitude as the triangle height.

b For Undershoot area, use the equation:

Area = 0.5 x base x height

8 Compare test results with the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area below Min Abs Level(Data Mask)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103022 [Undershoot area below Min Abs Level (Data Mask)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude below VDUS] [Maximum undershoot area per 1 UI below VDUS] [Maximum undershoot area per 1 UI between VSSQ and VDUS1]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 Test Mode (for Test ID 103022)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

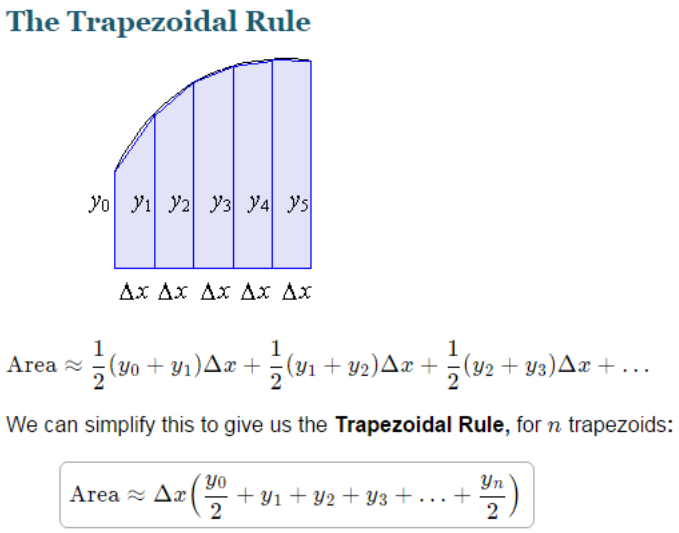


Figure 51 Equation for Total_Area_Above_0V

c Evaluate Area_Below_MinAbsLevel by using Trapezoidal Method Area Calculation (as shown in Figure 27).

d Calculate Area_Between_V_{SSQ}_and_MinAbsLevel using the equation:

Area_Between_V_{SSQ}_and_MinAbsLevel = Total_Area_Belowe_0V - Area_Below_MinAbsLevel

e To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Area_Below_MinAbsLevel
- Area_Between_V_{SSQ}_and_MinAbsLevel

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limits.

Expected/ Observable Results:

DDR4 Test Mode

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area between VSSQ and Min Abs Level(Data Mask)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

103023 [Undershoot area between VSSQ and Min Abs Level (Data Mask)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.6	Table 127	[Maximum peak amplitude below VDUS] [Maximum undershoot area per 1 UI below VDUS] [Maximum undershoot area per 1 UI between VSSQ and VDUS1]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 Test Mode (for Test ID 103023)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

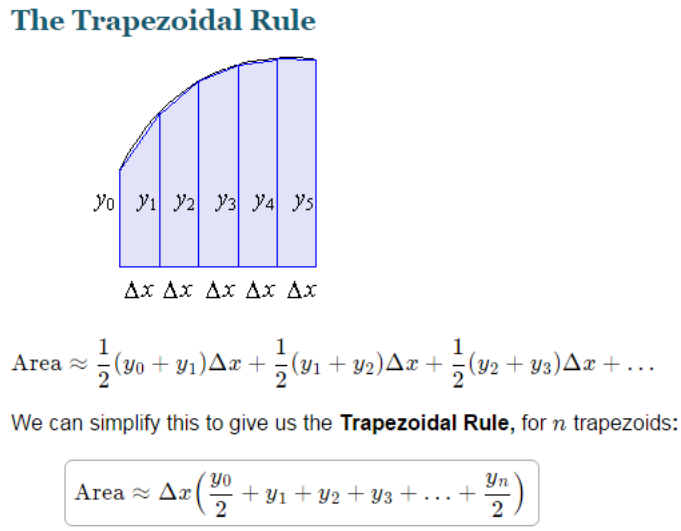


Figure 52 Equation for Total_Area_Above_0V

c Evaluate Area_Below_MinAbsLevel by using Trapezoidal Method Area Calculation (as shown in Figure 28).

d Calculate Area_Between_V_{SSQ}_and_MinAbsLevel using the equation:

Area_Between_V_{SSQ}_and_MinAbsLevel = Total_Area_Belowe_0V - Area_Below_MinAbsLevel

e To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Area_Below_MinAbsLevel
- Area_Between_V_{SSQ}_and_MinAbsLevel

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area (Data Mask)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

503015 [Undershoot area(Data Mask)]

LPDDR4X (Differential) Test Mode

603015 [Undershoot area(Data Mask)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for undershoot area] [Maximum area below V_{SS}]

Test Overview: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Test Procedure: **LPDDR4 (for Test ID 503015) / LPDDR4X (Differential) (for Test ID 603015)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

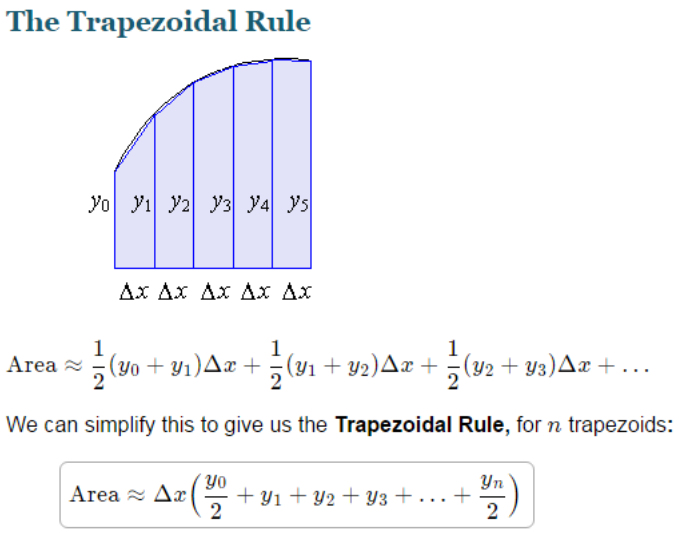


Figure 53 Equation for Total_Area_Above_0V

c Evaluate Area_Below_V_{SSQ} by using Trapezoidal Method Area Calculation (as shown in Figure 27).

d Calculate Area_Between_V_{SSQ}_and_MinAbsLevel using the equation:

Area_Between_V_{SSQ}_and_MinAbsLevel = Total_Area_Belowe_0V - Area_Below_MinAbsLevel

e To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Area_Below_V_{SSQ}

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limits.

Expected/ Observable Results:

LPDDR4 / LPDDR4X (Differential) Test Modes

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot/Undershoot (Address, Control)

Overshoot amplitude (Address, Control)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

10393 [Overshoot amplitude (Address, Control)]

LPDDR4 Test Mode

50351 [Overshoot amplitude (Address, Control)]

LPDDR4X (Differential) Test Mode

60351 [Overshoot amplitude (Address, Control)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.4	Table 125	[Maximum peak amplitude above VAOS] [Maximum overshoot area per 1 tCK above VAOS] [Maximum overshoot area per 1 tCK between VDD and VAOS]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for overshoot area] [Maximum area above V_{DD}]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Test Procedure: **DDR4 (for Test ID 10393)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DD} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

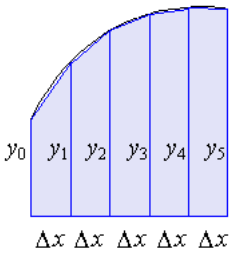
$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD}$$

b Evaluate Area_below_V_{DD} using the equation:

$$\text{Area\_below\_}V_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

The Trapezoidal Rule



$$\text{Area} \approx \frac{1}{2}(y_0 + y_1)\Delta x + \frac{1}{2}(y_1 + y_2)\Delta x + \frac{1}{2}(y_2 + y_3)\Delta x + \ldots$$

We can simplify this to give us the **Trapezoidal Rule**, for n trapezoids:

$$\text{Area} \approx \Delta x\left(\frac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + \frac{y_n}{2}\right)$$

Figure 54 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD} using the equation:

$$\text{Area\_Above\_}V_{DD} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD}$$

e Evaluate Area_Above_$V_{DDAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 15).

f Calculate Area_Between_V_{DD}_and_$V_{DDAbsMax}$ using the equation:

$$\text{Area\_Between\_}V_{DD}\text{\_and\_}V_{DDAbsMax} = \text{Area\_Above\_}V_{DD} - \text{Area\_Above\_}V_{DDAbsMax}$$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDAbsMax}$
- Area_Between_V_{DD}_and_$V_{DDAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

LPDDR4 (for Test IDs 50351) / LPDDR4X (Differential) (for Test ID 60351)

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use T_{MAX} and V_{MAX} to get the time-stamp of maximum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to maximize the peak area.

5 Find the edges before and after the Overshoot Point at the Supply Reference Level in order to calculate the maximum overshoot length duration.
Table 2 shows the supply reference level for each pin group:

Table 7 Supply reference level

PIN	Supply Reference Level
Address and Control pin	V_{DD2}
Data, Strobe and Mask pin	V_{DDQ}
Clock	V_{DD2}

6 Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = V_{MAX} - Supply Reference Level (refer to Table 2)

7 Calculate Overshoot area (V-ns)

a By calculating area of a triangle using the overshoot width as the triangle base and the overshoot amplitude as the triangle height.

b For Overshoot area, use the equation:

Area = 0.5 x base x height

8 Compare test results with the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area above VDD Abs Max(Address, Control)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

10394 [Overshoot area above VDD Abs Max (Address, Control)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.4	Table 125	[Maximum peak amplitude above VAOS] [Maximum overshoot area per 1 tCK above VAOS] [Maximum overshoot area per 1 tCK between VDD and VAOS]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 (for Test ID 10394)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DD} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD}$$

b Evaluate Area_below_V_{DD} using the equation:

$$\text{Area\_below\_}V_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

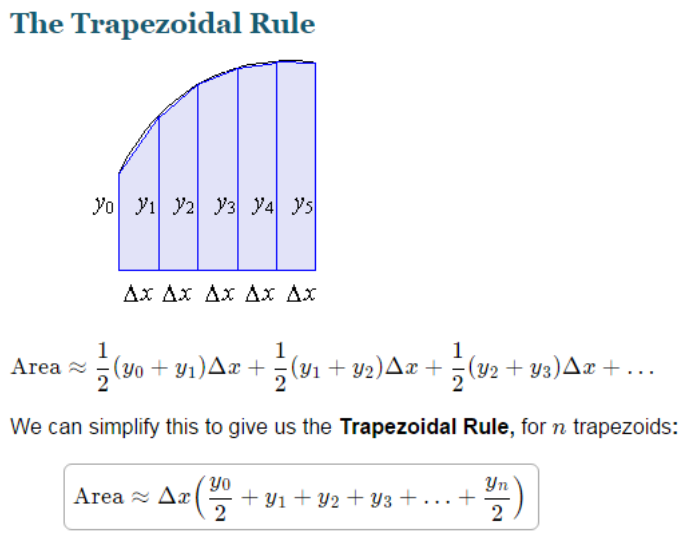


Figure 55 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD} using the equation:

$$\text{Area\_Above\_}V_{DD} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD}$$

e Evaluate Area_Above_$V_{DDAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 15).

f Calculate Area_Between_V_{DD}_and_$V_{DDAbsMax}$ using the equation:

$$\text{Area\_Between\_}V_{DD}\text{\_and\_}V_{DDAbsMax} = \text{Area\_Above\_}V_{DD} - \text{Area\_Above\_}V_{DDAbsMax}$$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDAbsMax}$
- Area_Between_V_{DD}_and_$V_{DDAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area between VDD and VDD Abs Max(Address, Control)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

10395 [Overshoot area between VDD and VDD Abs Max (Address, Control)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.4	Table 125	[Maximum peak amplitude above VAOS] [Maximum overshoot area per 1 tCK above VAOS] [Maximum overshoot area per 1 tCK between VDD and VAOS]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 (for Test ID 10395)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DD} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD}$$

b Evaluate Area_below_V_{DD} using the equation:

$$\text{Area\_below\_}V_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

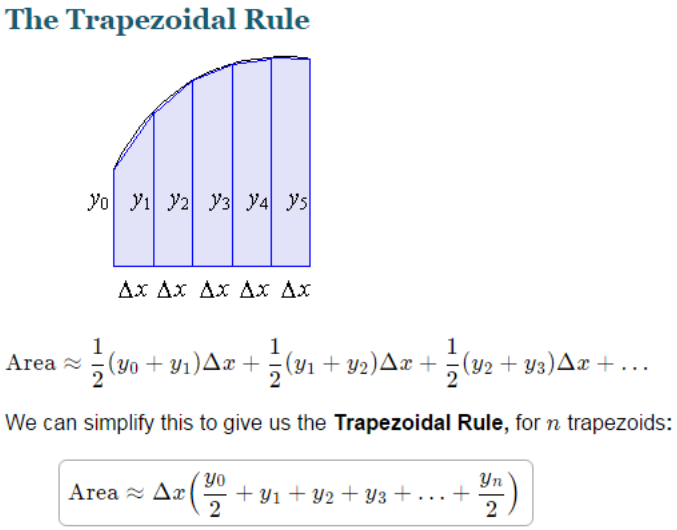


Figure 56 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD} using the equation:

$$\text{Area\_Above\_}V_{DD} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD}$$

e Evaluate Area_Above_$V_{DDAbsMax}$ by using Trapezoidal Method Area Calculation (as shown in Figure 15).

f Calculate Area_Between_V_{DD}_and_$V_{DDAbsMax}$ using the equation:

$$\text{Area\_Between\_}V_{DD}\text{\_and\_}V_{DDAbsMax} = \text{Area\_Above\_}V_{DD} - \text{Area\_Above\_}V_{DDAbsMax}$$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDAbsMax}$
- Area_Between_V_{DD}_and_$V_{DDAbsMax}$

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Overshoot area (Address, Control)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

50352 [Overshoot area (Address, Control)]

LPDDR4X (Differential) Test Mode

60352 [Overshoot area (Address, Control)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for overshoot area] [Maximum area above V_{DD}]

Test Overview: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Test Procedure: **LPDDR4 (for Test ID 50352) / LPDDR4X (Differential) (for Test ID 60352)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD2} crossing and ends at the falling edge of V_{DD} crossing.

4 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD2}$$

b Evaluate Area_below_V_{DD2} using the equation:

$$\text{Area\_below\_}V_{DD2} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD2}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

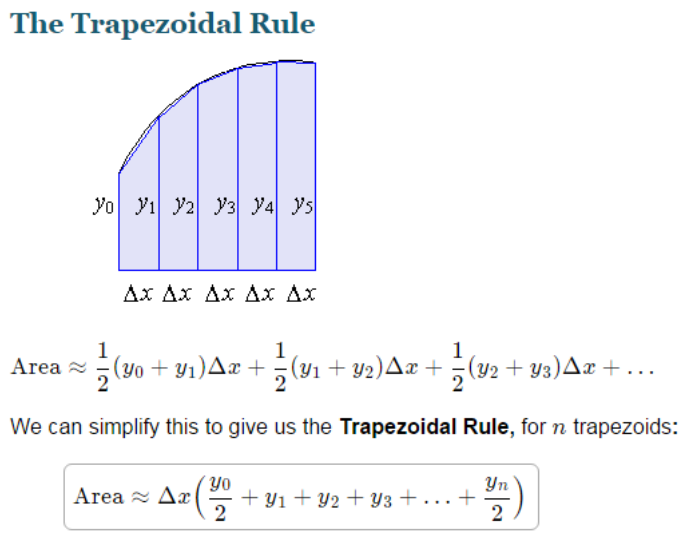


Figure 57 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD2} using the equation:

Area_Above_V_{DD2} = Total_Area_Above_0V - Area_below_V_{DD2}

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DD2}

5 Repeat step 4 for the rest of the “OvershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

LPDDR4 / LPDDR4X (Differential) Test Modes

The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot amplitude (Address, Control)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

10396 [Undershoot amplitude (Address, Control)]

LPDDR4 Test Mode

50361 [Undershoot amplitude (Address, Control)]

LPDDR4X (Differential) Test Mode

60361 [Undershoot amplitude (Address, Control)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.4	Table 125	[Maximum peak amplitude allowed for undershoot] [Maximum undershoot area per 1 tCK below VSS]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for undershoot area] [Maximum area below V_{SS}]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Test Procedure: **DDR4 Test Mode (for Test ID 10396)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

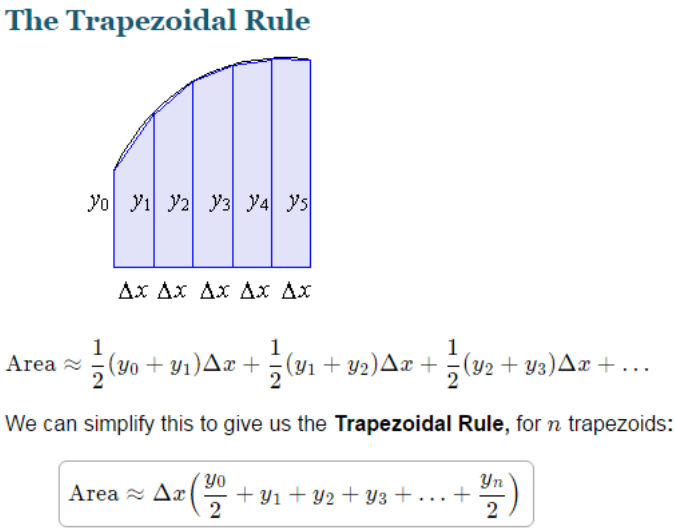


Figure 58 Equation for Total_Area_Above_0V

c To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Total_Area_Below_0V

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

LPDDR4 (for Test IDs 50361) / LPDDR4X (Differential) (for Test ID 60361)

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use T_{MIN} and V_{MIN} to get the time-stamp of minimum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to minimize the peak area.

5 Find the edges before and after the Undershoot Point at the GND (~0V) level in order to calculate the maximum undershoot length duration.

6 Calculate Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

7 Calculate Undershoot area (V-ns)

a By calculating area of a triangle using the undershoot width as the triangle base and the undershoot amplitude as the triangle height.

b For Undershoot area, use the equation:

$$\text{Area} = 0.5 \times \text{base} \times \text{height}$$

8 Compare test results with the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area below VSS(Address, Control)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

10397 [Undershoot area below VSS (Address, Control)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.4	Table 125	[Maximum peak amplitude allowed for undershoot] [Maximum undershoot area per 1 tCK below VSS]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: **DDR4 Test Mode (for Test ID 10397)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

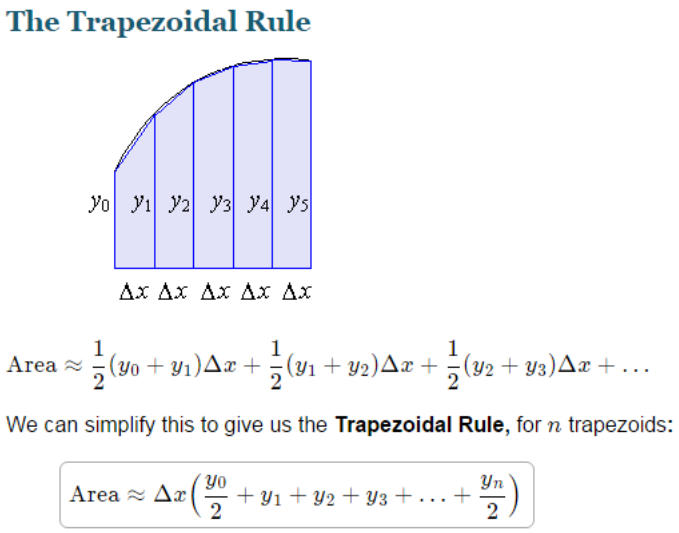


Figure 59 Equation for Total_Area_Above_0V

c To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Total_Area_Below_0V

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limit.

Expected/ Observable Results:

DDR4 Test Mode

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Undershoot area (Address, Control)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

50362 [Undershoot area (Address, Control)]

LPDDR4X (Differential) Test Mode

60362 [Undershoot area (Address, Control)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.6	Table 202	[Maximum peak amplitude allowed for undershoot area] [Maximum area below V_{SS}]

Test Overview: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Test Procedure: **LPDDR4 (for Test ID 50362) / LPDDR4X (Differential) (for Test ID 60362)**

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

4 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

b Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation:

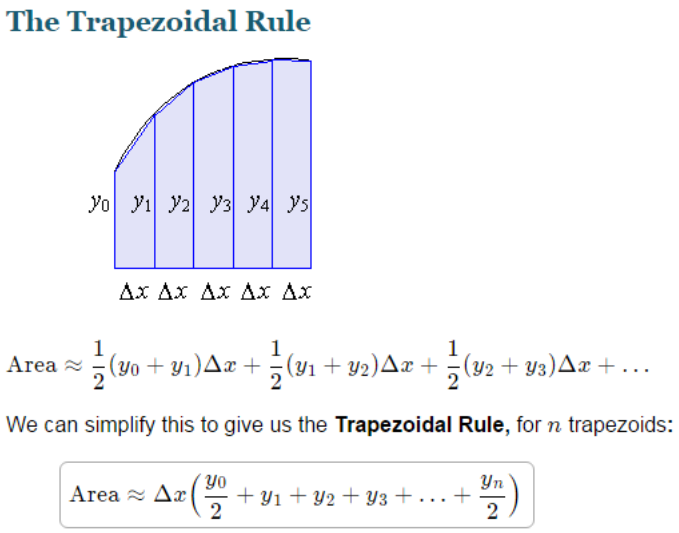


Figure 60 Equation for Total_Area_Above_0V

c To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Total_Area_Below_0V

5 Repeat step 4 for the rest of the “UndershootRegion” found in the acquired waveform.

6 Find the worst result from the stored results listed above.

7 Compare the test result with the compliance test limits.

Expected/ Observable Results:

LPDDR4 / LPDDR4X (Differential) Test Modes

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Vref Signal Test

VREF(DC) Measurement

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

10398 [VREF(DC) Measurement]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.1	Table 121	VREFCA(DC) [Reference Voltage for ADD, CMD inputs]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: The purpose of this test is to verify the voltage level value of the $V_{REF(DC)}$ signal.

Test Procedure: **DDR4 (for Test ID 10398)**

1 Set the number of sampling points to 2M samples and sampling rate for an acquisition length of 1 second.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Calculate the average voltage of the signal.
Record the resulting average measurement value as $V_{REF(DC)}$.

4 Compare test result to the compliance test limit.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of $V_{REF(DC)}$ shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

VREF(AC) Measurement

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

10399 [VREF(AC) Measurement]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.1	Table 121	VREF(AC) [Reference Voltage for ADD, CMD inputs]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the voltage level value of the $V_{REF(AC)}$ signal.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 (for Test ID 10399)**

1 Set the number of sampling points to 2M samples and sampling rate for an acquisition length of 1 second.

2 Sample/acquire signal data and then perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use T_{MAX}, V_{MAX} to obtain time-stamp of maximum voltage on all regions of the acquired waveform.

4 Use T_{MIN}, V_{MIN} to obtain time-stamp of minimum voltage on all regions of the acquired waveform.

5 Take V_{MIN} or V_{MAX} for the worst test result.

6 Compare test result to the compliance test limit.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of $V_{REF(AC)}$ shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

Differential Signals (WRITE cycle tests)

Differential AC Input Levels for Clock

VIHdiff.CK(AC)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

10411 [VIHdiff.CK(AC)]

LPDDR4 Test Mode

50411 [VIHdiff.CK(AC)]

LPDDR4X (Differential) Test Mode

60411 [VIHdiff.CK(AC)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.2	Table 122	VIHdiff(AC) [Differential input high AC]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.4	Table 190	VIHdiff_CK [Differential input high]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the high level voltage value of the test signal.

Test Procedure: **DDR4 (for Test ID 10411) / LPDDR4 (for Test ID 50411) / LPDDR4X (Differential) (for Test ID 60411)**

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the clock signal under test.

3 Find all valid Clock positive pulse in the triggered waveform.
A valid Clock positive pulse starts at the 0V crossing at valid Clock rising edge and ends at the 0V crossing at the following valid Clock falling edge.

4 Zoom into the first pulse and perform V_{TOP}.
Take the V_{TOP} measurement as $V_{IHdiff\ (AC)}$ value.

5 Continue the previous step with another nine valid positive pulses found in the specified waveform.

6 Determine the worst result from the set of $V_{IHdiff\ (AC)}$ values measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The worst measured $V_{IHdiff.CK\ (AC)}$ shall be within the conformance limits as per the JEDEC specification in the References section.

VIHdiff.CK(DC)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

10415 [VIHdiff.CK(DC)]

LPDDR4 Test Mode

50415 [VIHdiff.CK(DC)]

LPDDR4X (Differential) Test Mode

60415 [VIHdiff.CK(DC)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.2	Table 122	VIHdiff [Differential input high]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.4	Table 190	VIHdiff_CK [Differential input high]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the high level voltage value of the test signal.

Test Procedure: **DDR4 (for Test ID 10415) / LPDDR4 (for Test ID 50415) / LPDDR4X (Differential) (for Test ID 60415)**

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the clock signal under test.

3 Find all valid Clock positive pulse in the triggered waveform.
A valid Clock positive pulse starts at the 0V crossing at valid Clock rising edge and ends at the 0V crossing at the following valid Clock falling edge.

4 Zoom into the first pulse and perform V_{TOP}.
Take the V_{TOP} measurement as $V_{IHdiff\ (DC)}$ value.

5 Continue the previous step with another nine valid positive pulses found in the specified waveform.

6 Determine the worst result from the set of $V_{IHdiff\ (DC)}$ values measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The worst measured $V_{IHdiff.CK\ (DC)}$ shall be within the conformance limits as per the JEDEC specification in the References section.

VILdiff.CK(AC)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

10412 [VILdiff.CK(AC)]

LPDDR4 Test Mode

50412 [VILdiff.CK(AC)]

LPDDR4X (Differential) Test Mode

60412 [VILdiff.CK(AC)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.2	Table 122	VILdiff(AC) [Differential input low AC]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.4	Table 190	VILdiff_CK [Differential input low]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the low level voltage value of the test signal.

Test Procedure: **DDR4 (for Test ID 10412) / LPDDR4 (for Test ID 50412) / LPDDR4X (Differential) (for Test ID 60412)**

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the clock signal under test.

3 Find all valid Clock negative pulse in the triggered waveform.
A valid Clock negative pulse starts at the 0V crossing at valid Clock falling edge and ends at the 0V crossing at the following valid Clock rising edge.

4 Zoom into the first pulse and perform V_{BASE}.
Take the V_{BASE} measurement as $V_{ILdiff\ (AC)}$ value.

5 Continue the previous step with another nine valid positive pulses found in the specified waveform.

6 Determine the worst result from the set of $V_{ILdiff\ (AC)}$ values measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The worst measured $V_{ILdiff.CK\ (AC)}$ shall be within the conformance limits as per the JEDEC specification in the References section.

VILdiff.CK(DC)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

10416 [VILdiff.CK(DC)]

LPDDR4 Test Mode

50416 [VILdiff.CK(DC)]

LPDDR4X (Differential) Test Mode

60416 [VILdiff.CK(DC)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.3.2	Table 122	VILdiff [Differential input low]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.4	Table 190	VILdiff_CK [Differential input low]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the low level voltage value of the test signal.

Test Procedure: **DDR4 (for Test ID 10416) / LPDDR4 (for Test ID 50416) / LPDDR4X (Differential) (for Test ID 60416)**

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the clock signal under test.

3 Find all valid Clock negative pulse in the triggered waveform.
A valid Clock negative pulse starts at the 0V crossing at valid Clock falling edge and ends at the 0V crossing at the following valid Clock rising edge.

4 Zoom into the first pulse and perform V_{BASE}.
Take the V_{BASE} measurement as $V_{ILdiff\ (DC)}$ value.

5 Continue the previous step with another nine valid positive pulses found in the specified waveform.

6 Determine the worst result from the set of $V_{ILdiff\ (DC)}$ values measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The worst measured $V_{ILdiff.CK\ (DC)}$ shall be within the conformance limits as per the JEDEC specification in the References section.

Vindiff_CK

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

50421 [Vindiff_CK]

LPDDR4X (Differential) Test Mode

60421 [Vindiff_CK]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.1	Table 187	Vindiff_CK [CK differential input voltage]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the difference in values of peak voltage between the high pulse and low pulse of the test signal.

Test Procedure: **LPDDR4 (for Test ID 50421) / LPDDR4X (Differential) (for Test ID 60421)**

1 Pre-condition the oscilloscope.
2 Trigger on the rising edge of the clock signal under test.
3 Find all valid positive and negative pulses of the Clock in the entire waveform.
A valid positive pulse on the Clock starts at the valid rising edge of the Clock and ends at the following valid falling edge of the Clock, whereas a valid negative pulse on the Clock starts at the valid falling edge of the Clock and ends at the following valid rising edge of the Clock.
4 Measure Vmax of first positive pulse and Vmin of the first negative pulse.
5 Calculate the difference of the two measurements and denote the result as Vindiff_CK #1.
6 Measure Vmin of first negative pulse and Vmax of the second positive pulse.
7 Calculate the difference of the two measurements and denote the result as Vindiff_CK #2.
8 Continue steps 4 to 7 for measurements on the remaining pulse that was obtained.
9 Determine the worst result from the set of Vindiff_CK values measured.

Expected/ Observable Results: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vindiff_CK for the test signal shall be within the conformance limits as per the JEDEC specification.

Vindiff_CK/2 High Pulse

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

50417 [Vindiff_CK/2 High Pulse]

LPDDR4X (Differential) Test Mode

60417 [Vindiff_CK/2 High Pulse]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.1	Table 187	Vindiff_CK [CK differential input voltage]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the peak voltage of the high pulse.

Test Procedure: **LPDDR4 (for Test ID 50417) / LPDDR4X (Differential) (for Test ID 60417)**

1 Pre-condition the oscilloscope.
2 Trigger on the rising edge of the clock signal under test.
3 Find all valid positive pulses of the Clock in the entire waveform.
A valid positive pulse on the Clock starts at the valid rising edge of the Clock and ends at the following valid falling edge of the Clock.
4 Zoom into the first pulse and perform V_{MAX}. Consider the V_{MAX} measurement as the value of Vindiff_CK/2.
5 Continue the previous step with the rest of the positive pulses found in the specified waveform.
6 Determine the worst result from the set of Vindiff_CK/2 measured.

Expected/ Observable Results: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vindiff_CK/2 for the test signal shall be within the conformance limits as per the JEDEC specification.

Vindiff_CK/2 Low Pulse

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

50418 [Vindiff_CK/2 Low Pulse]

LPDDR4X (Differential) Test Mode

60418 [Vindiff_CK/2 Low Pulse]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.1	Table 187	Vindiff_CK [CK differential input voltage]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the peak voltage of the low pulse.

Test Procedure: **LPDDR4 (for Test ID 50418) / LPDDR4X (Differential) (for Test ID 60418)**

1 Pre-condition the oscilloscope.
2 Trigger on the falling edge of the clock signal under test.
3 Find all valid negative pulses of the Clock in the entire waveform.
A valid negative pulse on the Clock starts at the valid falling edge of the Clock and ends at the following valid rising edge of the Clock.
4 Zoom into the first pulse and perform V_{MIN}. Consider the V_{MIN} measurement as the value of Vindiff_CK/2.
5 Continue the previous step with the rest of the negative pulses found in the specified waveform.
6 Determine the worst result from the set of Vindiff_CK/2 measured.

Expected/ Observable Results: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vindiff_CK/2 for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_CK (Positive Pulse)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

50419 [Vinse_CK (Positive Pulse)]

LPDDR4X (Differential) Test Mode

60419 [Vinse_CK (Positive Pulse)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.3	Table 188	Vinse_CK [Clock Single-Ended input voltage]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the peak voltage of the high pulse.

Test Procedure: **LPDDR4 (for Test ID 50419) / LPDDR4X (Differential) (for Test ID 60419)**

1 Pre-condition the oscilloscope.
2 Trigger on the rising edge of the clock signal under test.
3 Find all valid positive pulses of the Clock in the entire waveform.
A valid positive pulse on the Clock starts at the valid rising edge of the Clock and ends at the following valid falling edge of the Clock.
4 Zoom into the first pulse and perform V_{MAX}. Consider the V_{MAX} measurement as the value of Vinse_CK.
5 Continue the previous step with the rest of the positive pulses found in the specified waveform.
6 Determine the worst result from the set of Vinse_CK measured.

Expected/ Observable Results: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vinse_CK for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_CK (Negative Pulse)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

50420 [Vinse_CK (Negative Pulse)]

LPDDR4X (Differential) Test Mode

60420 [Vinse_CK (Negative Pulse)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.3	Table 188	Vinse_CK [Clock Single-Ended input voltage]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the peak voltage of the low pulse.

Test Procedure: **LPDDR4 (for Test ID 50420) / LPDDR4X (Differential) (for Test ID 60420)**

1 Pre-condition the oscilloscope.
2 Trigger on the falling edge of the clock signal under test.
3 Find all valid negative pulses of the Clock in the entire waveform.
A valid negative pulse on the Clock starts at the valid falling edge of the Clock and ends at the following valid rising edge of the Clock.
4 Zoom into the first pulse and perform V_{MIN}. Consider the V_{MIN} measurement as the value of Vinse_CK.
5 Continue the previous step with the rest of the negative pulses found in the specified waveform.
6 Determine the worst result from the set of Vinse_CK measured.

Expected/ Observable Results: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vinse_CK for the test signal shall be within the conformance limits as per the JEDEC specification.

SRIdiffR for Clock

Mode Supported: LPDDR4/LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

50422 [SRIdiffR for Clock]

LPDDR4X (Differential) Test Mode

60422 [SRIdiffR for Clock]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.4	Table 191	SRIdiff_CK [Differential Input Slew Rate for Clock]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the differential input slew rate for rising edge of the Clock signal.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 50422) / LPDDR4X (Differential) (for Test ID 60422)

1 Pre-condition the oscilloscope.
2 Trigger on the rising edge of the clock signal under test.
3 Find all the valid Clock rising edges in the entire waveform.
A valid clock rising edge starts at $V_{ILdiff.CK(AC)}$ crossing and ends at the following $V_{IHdiff.CK(AC)}$ crossing.
4 For all the valid Clock rising edges, find the transition time, T_R.
T_R is the time starting at $V_{ILdiff.CK(AC)}$ crossing and ending at the following $V_{IHdiff.CK(AC)}$ crossing.
5 Calculate SRIdiffR using the equation:

$$SRIdiffR = [V_{IHdiff.CK(AC)} - V_{ILdiff.CK(AC)}] / T_R$$

6 Determine the worst result from the set of SRIdiffR measured.

Expected/ Observable Results: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of SRIdiffR for the Clock signal shall be within the conformance limits as per the JEDEC specification in the References section.

SRIdiffF for Clock

Mode Supported: LPDDR4/LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

50423 [SRIdiffF for Clock]

LPDDR4X (Differential) Test Mode

60423 [SRIdiffF for Clock]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.4	Table 191	SRIdiff_CK [Differential Input Slew Rate for Clock]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the differential input slew rate for falling edge of the Clock signal.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 50423) / LPDDR4X (Differential) (for Test ID 60423)

1 Pre-condition the oscilloscope.
2 Trigger on the falling edge of the clock signal under test.
3 Find all the valid Clock falling edges in the entire waveform.
A valid clock falling edge starts at $V_{IHdiff.CK(AC)}$ crossing and ends at the following $V_{ILdiff.CK(AC)}$ crossing.
4 For all the valid Clock falling edges, find the transition time, T_F.
T_F is the time starting at $V_{IHdiff.CK(AC)}$ crossing and ending at the following $V_{ILdiff.CK(AC)}$ crossing.
5 Calculate SRIdiffF using the equation:

$$SRIdiffF = [V_{ILdiff.CK(AC)} - V_{IHdiff.CK(AC)}] / T_F$$

6 Determine the worst result from the set of SRIdiffF measured.

Expected/ Observable Results: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of SRIdiffF for the Clock signal shall be within the conformance limits as per the JEDEC specification in the References section.

Clock Cross Point Voltage Test

VIX(CK)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

10381 [VIX(CK)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.5	Table 129	VIX (CK) [Differential Input Cross Point Voltage relative to V_{DD}/2 for CK_t, CK_c]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the value of the crossing point voltage on the input differential pair test signal.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 10381)**

1 Sample/Acquire data waveforms.
2 Use Subtract FUNC to generate the differential waveform from the 2-source input.
3 Find the time-stamp of all differential CLK crossings that cross 0V.
4 Use V_{Time} to get the actual crossing point voltage value using the time-stamp obtained in the previous step.
5 For each cross point voltage, calculate the final result using the equation:

$$V_{IX} = \text{cross point voltage} - V_{DD}/2.$$

6 Determine the worst result from the set of V_{IX} measured.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured crossing point value for the differential test signal pair shall be within the conformance limits as per the JEDEC specification in the References section.

LPDDR4 / LPDDR4X Test Modes

Not available.

Vix_CK_ratio

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

50381 [VIX_CK_ratio]

LPDDR4X (Differential) Test Mode

60381 [VIX_CK_ratio]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.5	Table 192	VIX_CK_Ratio [CK Differential Input Cross Point Voltage Ratio]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the ratio of the calculated crossing point voltage from the value of the measured crossing point voltage on the input differential pair test signals.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 50381) / LPDDR4X (Differential) (for Test ID 60381)

1 Sample/Acquire data waveforms.
2 Use Subtract FUNC to generate the differential waveform from the 2-source input.
3 Find the Vmax and VMin of the differential signal denoted as Max(f(t)) and Min(f(t)) respectively.
4 Find the time-stamp of all differential CLK crossing that crosses 0V.
5 Use V_{Time} to get the actual crossing point voltage value using the time-stamp obtained in the previous step.
6 At each crosspoint (rising and falling) found, find the voltage differential between the crosspoint and VRefCA. The rising and falling crosspoint voltage differential is denoted as Vix_CK_RF and Vix_CK_FR respectively.
7 For each cross point voltage, calculate the final result using the equation (for Rising):

$$V_{IX}\_CK\_ratio = 100\% \times [Vix\_CK\_RF/Max(f(t))]$$

8 For each cross point voltage, calculate the final result using the equation (for Falling):

$$V_{IX}\_CK\_ratio = 100\% \times [Vix\_CK\_FR/Min(f(t))]$$

9 Determine the worst result from the set of V_{IX}_CK_ratio measured.

Expected/ Observable Results:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The calculated value of the crossing point voltage ratio for the differential test signal pair shall be within the conformance limits as per the JEDEC specification in the References section.

Differential Input Level and Slew Rate For Strobe

NOTE This category of tests is available only for the LPDDR4 and LPDDR4X SDRAM Types.

VIHdiff_DQS

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

50501 [VIHdiff_DQS]

LPDDR4X (Differential) Test Mode

650501 [VIHdiff_DQS]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.9	Table 196	VIHdiff_DQS [Differential input high]

Test Overview: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the high level voltage value of the DQS signal.

Test Procedure: **LPDDR4 (for Test ID 50501) / LPDDR4X (Differential) (for Test ID 650501)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid Strobe positive pulses in the specified burst.
A valid Strobe positive pulse starts at 0V crossing at valid Strobe rising edge and ends at 0V crossing at the following valid Strobe falling edge.
4 Zoom into the first pulse and measure V_{TOP}.
Take the V_{TOP} measurement as V_{IHdiff_DQS} value.
5 Continue the previous step with the rest of the valid positive pulses found in the specified burst.
6 Determine the worst result from the set of V_{IHdiff_DQS} values measured.

Expected/ Observable Results: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The worst measured V_{IHdiff_DQS} shall be within the conformance limits as per the JEDEC specification in the References section.

VILdiff_DQS

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

50502 [VILdiff_DQS]

LPDDR4X (Differential) Test Mode

650502 [VILdiff_DQS]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.9	Table 196	VILdiff_DQS [Differential input low]

Test Overview: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the low level voltage value of the DQS signal.

Test Procedure: **LPDDR4 (for Test ID 50502) / LPDDR4X (Differential) (for Test ID 650502)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid Strobe negative pulses in the specified burst.
A valid Strobe negative pulse starts at 0V crossing at valid Strobe falling edge and ends at 0V crossing at the following valid Strobe rising edge.
4 Zoom into the first pulse and measure V_{BASE}.
Take the V_{BASE} measurement as V_{ILdiff_DQS} value.
5 Continue the previous step with the rest of the valid negative pulses found in the specified burst.
6 Determine the worst result from the set of V_{ILdiff_DQS} values measured.

Expected/ Observable Results: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The worst measured V_{ILdiff_DQS} shall be within the conformance limits as per the JEDEC specification in the References section.

Vindiff_DQS

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

50503 [Vindiff_DQS]

LPDDR4X (Differential) Test Mode

650503 [Vindiff_DQS]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.6	Table 193	Vindiff_DQS [DQS differential input voltage]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the difference in values of peak voltage between the high pulse and low pulse of the DQS signal.

Test Procedure: **LPDDR4 (for Test ID 50503) / LPDDR4X (Differential) (for Test ID 650503)**

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid Strobe positive and negative pulses in the specified burst.
A valid positive pulse starts at the valid Strobe rising edge and ends at the following valid Strobe falling edge, whereas a valid negative pulse starts at the valid Strobe falling edge and ends at the following valid Strobe rising edge.

4 Measure V_{MAX} of first positive pulse and V_{MIN} of the first negative pulse.

5 Calculate the difference of the two measurements and denote the result as Vindiff_DQS #1.

6 Measure V_{MIN} of first negative pulse and V_{MAX} of the second positive pulse.

7 Calculate the difference of the two measurements and denote the result as Vindiff_DQS #2.

8 Continue steps 4 to 7 for measurements on the remaining pulse that was obtained.

9 Determine the worst result from the set of Vindiff_DQS values measured.

Expected/ Observable Results: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vindiff_DQS for the test signal shall be within the conformance limits as per the JEDEC specification.

Vindiff_DQS/2 High Pulse

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

50504 [Vindiff_DQS/2 High Pulse]

LPDDR4X (Differential) Test Mode

650504 [Vindiff_DQS/2 High Pulse]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.6	Table 193	Vindiff_DQS [DQS differential input voltage]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the peak voltage of the DQS high pulse.

Test Procedure: **LPDDR4 (for Test ID 50504) / LPDDR4X (Differential) (for Test ID 650504)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid Strobe positive pulses in the specified burst.
A valid positive pulse starts at the valid Strobe rising edge and ends at the following valid Strobe falling edge.
4 Zoom into the first pulse and perform V_{MAX}. Consider the V_{MAX} measurement as the value of Vindiff_DQS/2.
5 Continue the previous step with the rest of the positive pulses found in the specified burst.
6 Determine the worst result from the set of Vindiff_DQS/2 measured.

Expected/ Observable Results: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vindiff_DQS/2 High Pulse for the test signal shall be within the conformance limits as per the JEDEC specification.

Vindiff_DQS/2 Low Pulse

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

50505 [Vindiff_DQS/2 Low Pulse]

LPDDR4X (Differential) Test Mode

650505 [Vindiff_DQS/2 Low Pulse]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.6	Table 193	Vindiff_DQS [DQS differential input voltage]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the peak voltage of the DQS low pulse.

Test Procedure: **LPDDR4 (for Test ID 50505) / LPDDR4X (Differential) (for Test ID 650505)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid Strobe negative pulses in the specified burst.
A valid negative pulse starts at the valid Strobe falling edge and ends at the following valid Strobe rising edge.
4 Zoom into the first pulse and perform V_{MIN}. Consider the V_{MIN} measurement as the value of Vindiff_DQS/2.
5 Continue the previous step with the rest of the negative pulses found in the specified burst.
6 Determine the worst result from the set of Vindiff_DQS/2 measured.

Expected/ Observable Results: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vindiff_DQS/2 Low Pulse for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_DQS (Positive Pulse)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

50506 [Vinse_DQS (Positive Pulse)]

LPDDR4X (Differential) Test Mode

650506 [Vinse_DQS (Positive Pulse)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.8	Table 194	Vinse_DQS [DQS Single-Ended input voltage]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the peak voltage of the DQS high pulse.

Test Procedure: **LPDDR4 (for Test ID 50506) / LPDDR4X (Differential) (for Test ID 650506)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid Strobe positive pulses in the specified burst.
A valid positive pulse starts at the valid Strobe rising edge and ends at the following valid Strobe falling edge.
4 Zoom into the first pulse and perform V_{MAX}. Consider the V_{MAX} measurement as the value of Vinse_DQS.
5 Continue the previous step with the rest of the positive pulses found in the specified burst.
6 Determine the worst result from the set of Vinse_DQS measured.

Expected/ Observable Results: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vinse_DQS (Positive Pulse) for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_DQS (Negative Pulse)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

50507 [Vinse_DQS (Negative Pulse)]

LPDDR4X (Differential) Test Mode

650507 [Vinse_DQS (Negative Pulse)]

References: **LPDDR4 / LPDDR4X (Differential) Test Modes**

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.8	Table 194	Vinse_DQS [DQS Single-Ended input voltage]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the peak voltage of the DQS low pulse.

Test Procedure: **LPDDR4 (for Test ID 50507) / LPDDR4X (Differential) (for Test ID 650507)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid Strobe negative pulses in the specified burst.
A valid negative pulse starts at the valid Strobe falling edge and ends at the following valid Strobe rising edge.
4 Zoom into the first pulse and measure V_{MIN}. Consider the V_{MIN} measurement as the value of Vinse_DQS.
5 Continue the previous step with the rest of the negative pulses found in the specified burst.
6 Determine the worst result from the set of Vinse_DQS measured.

Expected/ Observable Results: **LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of Vinse_DQS (Negative Pulse) for the test signal shall be within the conformance limits as per the JEDEC specification.

SRIdiffR for Strobe

Mode Supported: LPDDR4/LPDDR4X (Differential only)

Test ID:

LPDDR4 Test Mode

50508 [SRIdiffR for Strobe]

LPDDR4X (Differential) Test Mode

650508 [SRIdiffR for Strobe]

References:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.9	Table 197	SRIdiff [Differential Input Slew Rate for Strobe]

Test Overview:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the differential input slew rate for rising edge of the DQS signal.

Test Procedure:

DDR4 Test Mode

Not available.

LPDDR4 (for Test ID 50508) / LPDDR4X (Differential) (for Test ID 650508)

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid Strobe rising edges in the specified burst.
A valid Strobe rising edge starts at $V_{ILdiff.DQS(AC)}$ crossing and ends at following $V_{IHdiff.DQS(AC)}$ crossing.
4 For all the valid Strobe rising edges, find the transition time, T_R.
T_R is the time starting at $V_{ILdiff.DQS(AC)}$ crossing and ending at the following $V_{IHdiff.DQS(AC)}$ crossing.
5 Calculate SRIdiffR using the equation:

$$SRIdiffR = [V_{IHdiff.DQS(AC)} - V_{ILdiff.DQS(AC)}] / T_R$$

6 Determine the worst result from the set of SRIdiffR measured.

Expected/ Observable Results:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of SRIdiffR for the Strobe signal shall be within the conformance limits as per the JEDEC specification in the References section.

SRIdiffF for Strobe

Mode Supported: LPDDR4/LPDDR4X (Differential only)

Test ID: **LPDDR4 Test Mode**

50509 [SRIdiffF for Strobe]

LPDDR4X (Differential) Test Mode

650509 [SRIdiffF for Strobe]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.9	Table 197	SRIdiff [Differential Input Slew Rate for Strobe]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the differential input slew rate for falling edge of the DQS signal.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 50509) / LPDDR4X (Differential) (for Test ID 650509)

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid Strobe falling edges in the specified burst.
A valid Strobe falling edge starts at $V_{IHdiff.DQS(AC)}$ crossing and ends at following $V_{ILdiff.DQS(AC)}$ crossing.
4 For all the valid Strobe falling edges, find the transition time, T_F.
T_F is the time starting at $V_{IHdiff.DQS(AC)}$ crossing and ending at the following $V_{ILdiff.DQS(AC)}$ crossing.
5 Calculate SRIdiffF using the equation:

$$SRIdiffF = [V_{IHdiff.DQS(AC)} - V_{ILdiff.DQS(AC)}] / T_F$$

6 Determine the worst result from the set of SRIdiffF measured.

Expected/ Observable Results: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of SRIdiffF for the Strobe signal shall be within the conformance limits as per the JEDEC specification in the References section.

Differential AC Input Levels and Slew Rate tests for Strobe

NOTE This category of tests is available only for the DDR4 SDRAM Type.

VIHdiff.DQS(AC)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

10413 [VIHdiff.DQS(AC)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.7.5	Table 134	VIHDiff_DQS [Differential input high]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the high level voltage value of the test signal within the write burst.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 10413)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid Strobe positive pulses in the specified burst.
A valid Strobe positive pulse starts at 0V crossing at valid Strobe rising edge and ends at 0V crossing at the following valid Strobe falling edge.
4 Zoom into the first pulse and perform V_{TOP} measurement.
Take the value from V_{TOP} measurement as $V_{IHdiff.DQS\ (AC)}$ value.
5 Continue previous step with the rest of the positive pulses in the said burst.
6 Determine the worst result from the set of $V_{IHdiff.DQS\ (AC)}$ measured.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of $V_{IHdiff.DQS\ (AC)}$ for the test signal shall be within the conformance limits as per the JEDEC specification in the References section.

LPDDR4 / LPDDR4X Test Modes

Not available.

VIHdiff.DQS(DC)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

10417 [VIHdiff.DQS(DC)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.7.5	Table 134	VIHDiff_DQS [Differential input high]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the high level voltage value of the test signal within the write burst.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 10417)**

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid Strobe positive pulses in the specified burst.
A valid Strobe positive pulse starts at 0V crossing at valid Strobe rising edge and ends at 0V crossing at the following valid Strobe falling edge.

4 Zoom into the first pulse and perform V_{TOP} measurement.
Take the value from V_{TOP} measurement as $V_{IHdiff.DQS\ (DC)}$ value.

5 Continue previous step with the rest of the positive pulses in the said burst.

6 Determine the worst result from the set of $V_{IHdiff.DQS\ (DC)}$ measured.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of $V_{IHdiff.DQS\ (DC)}$ for the test signal shall be within the conformance limits as per the JEDEC specification in the References section.

LPDDR4 / LPDDR4X Test Modes

Not available.

VILdiff.DQS(AC)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

10414 [VILdiff.DQS(AC)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.7.5	Table 134	VILDiff_DQS [Differential input low]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the low level voltage value of the test signal within the write burst.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 10414)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid Strobe negative pulses in the specified burst.
A valid Strobe negative pulse starts at 0V crossing at valid Strobe falling edge and ends at 0V crossing at the following valid Strobe rising edge.
4 Zoom into the first pulse and perform V_{BASE} measurement.
Take the V_{BASE} measurement as $V_{ILdiff.DQS\ (AC)}$ value.
5 Continue previous step with the rest of the negative pulses in the specified burst.
6 Determine the worst result from the set of $V_{ILdiff.DQS\ (AC)}$ measured.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of $V_{ILdiff.DQS\ (AC)}$ for the test signal shall be within the conformance limits as per the JEDEC specification in the References section.

LPDDR4 / LPDDR4X Test Modes

Not available.

VILdiff.DQS(DC)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

10418 [VILdiff.DQS(DC)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.7.5	Table 134	VILDiff_DQS [Differential input low]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the low level voltage value of the test signal within the write burst.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 10418)**

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid Strobe negative pulses in the specified burst.
A valid Strobe negative pulse starts at 0V crossing at valid Strobe falling edge and ends at 0V crossing at the following valid Strobe rising edge.

4 Zoom into the first pulse and perform V_{BASE} measurement.
Take the V_{BASE} measurement as $V_{ILdiff.DQS\ (DC)}$ value.

5 Continue previous step with the rest of the negative pulses in the specified burst.

6 Determine the worst result from the set of $V_{ILdiff.DQS\ (DC)}$ measured.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of $V_{ILdiff.DQS\ (DC)}$ for the test signal shall be within the conformance limits as per the JEDEC specification in the References section.

LPDDR4 / LPDDR4X Test Modes

Not available.

VIHdiffPeak

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

10419 [VIHDiffPeak]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.7.2	Table 131	VIH.DIFF.Peak Voltage

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify that the high level peak input voltage value of the differential DQS test signal within the write burst. Refer to Figure 214 of the JESD79-4D document for the definition of differential DQS signal AC-swing level.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 10419)**

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid Differential Strobe positive pulse in the specified burst.
A valid Strobe positive pulse starts at 0V crossing at valid Strobe rising edge and ends at 0V crossing at the following valid Strobe falling edge.

4 Zoom into the first pulse and perform TMAX.

   a Perform VTIME with the TMAX obtained in the previous step to obtain the maximum voltage of the pulse.

   b Record the VTIME measurement as the value of VIHDiffPeak.

5 Continue the previous step with the rest of the positive pulses found in the specified burst.

6 Determine the worst result from the set of VIHDiffPeak measured.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of $V_{IHDIFFPEAK}$ for the test signal shall be within the conformance limits as per the JEDEC specification in the References section.

LPDDR4 / LPDDR4X Test Modes

Not available.

VILDiffPeak

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

10420 [VILDiffPeak]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.7.2	Table 131	VIL.DIFF.Peak Voltage

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify that the low level peak input voltage value of the differential DQS test signal within the write burst. Refer to Figure 214 of the JESD79-4D document for the definition of differential DQS signal AC-swing level.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 10420)**

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid Differential Strobe negative pulse in the specified burst.
A valid Strobe negative pulse starts at 0V crossing at valid Strobe falling edge and ends at 0V crossing at the following valid Strobe rising edge.

4 Zoom into the first pulse and perform TMIN.

a Perform VTIME with the TMIN obtained in the previous step to obtain the minimum voltage of the pulse.

b Record the VTIME measurement as the value of VILDiffPeak.

5 Continue the previous step with the rest of the negative pulses found in the specified burst.

6 Determine the worst result from the set of VILDiffPeak measured.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of $V_{ILDIFFPEAK}$ for the test signal shall be within the conformance limits as per the JEDEC specification in the References section.

LPDDR4 / LPDDR4X Test Modes

Not available.

SRIdiffR

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

11415 [SRIdiffR]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.7.5	Table 135	SRIDiff [Differential input slew rate]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the differential input slew rate for rising edge of the test signal.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 11415)**

1 Acquire and split the read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all the valid Strobe rising edges in the specified burst.
A valid Strobe rising edge starts at $V_{ILdiff.DQS(AC)}$ crossing and ends at the following $V_{IHdiff.DQS(AC)}$ crossing.

4 For all the valid Strobe rising edges, find the transition time, T_R.
T_R is the time starting at $V_{ILdiff.DQS(AC)}$ crossing and ending at the following $V_{IHdiff.DQS(AC)}$ crossing.

5 Calculate SRIdiffR using the equation:

$$SRIdiffR = [V_{IHdiff.DQS(AC)} - V_{ILdiff.DQS(AC)}] / T_R$$

6 Determine the worst result from the set of SRIdiffR measured.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of SRIdiffR for the test signal shall be within the conformance limits as per the JEDEC specification in the References section.

LPDDR4 / LPDDR4X Test Modes

Not available.

SRIdiffF

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

11416 [SRIdiffF]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.7.5	Table 135	SRIDiff [Differential input slew rate]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the differential input slew rate for falling edge of the test signal.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 11416)**

1 Acquire and split the read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all the valid Strobe falling edges in the specified burst.
A valid Strobe falling edge starts at $V_{IHdiff.DQS(AC)}$ crossing and ends at the following $V_{ILdiff.DQS(AC)}$ crossing.

4 For all the valid Strobe falling edges, find the transition time, T_R.
T_R is the time starting at $V_{IHdiff.DQS(AC)}$ crossing and ending at the following $V_{ILdiff.DQS(AC)}$ crossing.

5 Calculate SRIdiffF using the equation:

$$SRIdiffF = [V_{IHdiff.DQS(AC)} - V_{ILdiff.DQS(AC)}] / T_R$$

6 Determine the worst result from the set of SRIdiffF measured.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of SRIdiffF for the test signal shall be within the conformance limits as per the JEDEC specification in the References section.

LPDDR4 / LPDDR4X Test Modes

Not available.

Strobe Cross Point Voltage Test

VIX(DQS)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

10382 [VIX(DQS)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	8.7.4	Table 132	Vix_DQS_Ratio [DQS_t and DQS_c crossing relative to the midpoint of the DQS_t and DQS_c signal swings]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the value of the crossing point voltage on the input differential pair test signals within the write burst.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 10382)**

1 Sample/Acquire data waveforms.
2 Use Subtract FUNC to generate the differential waveform from the 2-source input.
3 Split the read and write burst of the acquired signal.
4 Take the first valid WRITE burst found.
5 Find time-stamp of all differential DQS crossings that cross 0V within the burst found above.
6 Use V_{Time} to get the actual crossing point voltage value using the time-stamp obtained in the previous step.
7 Find the DQS_t and DQS_c signal transition swing voltage as V_{DQS_trans}.
8 For each cross point voltage, calculate the crosspoint voltage difference between V_{DQS_trans} / 2 using the equation:

$$V_{IX} = \text{cross point voltage} - V_{DQS\_trans} / 2$$

9 Calculate the cross point ratio using the equation:

$$V_{IX\_DQS\_Ratio} = 100\% * (V_{IX} / V_{DQS\_trans})$$

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured crossing point value of $V_{IX\_DQS\_Ratio}$ for the differential test signal pair shall be within the conformance limits as per the JEDEC specification in the References section.

LPDDR4 / LPDDR4X Test Modes

Not available.

Vix_DQS_ratio

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

50382 [VIX_DQS_ratio]

LPDDR4X (Differential) Test Mode

60382 [VIX_DQS_ratio]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.2.10	Table 198	VIX_DQS_Ratio [DQS Differential Input Cross Point Voltage Ratio]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the ratio of the calculated crossing point voltage from the value of the measured crossing point voltage on the input differential pair test signals within the write burst.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 50382) / LPDDR4X (Differential) (for Test ID 60382)

1 Sample/Acquire data waveforms.
2 Use Subtract FUNC to generate the differential waveform from the 2-source input.
3 Split the read and write burst of the acquired signal.
4 Take the first valid WRITE burst found.
5 Find the time-stamp of all differential DQS crossings that cross 0V within the burst found above.
6 Use V_{Time} to get the actual crossing point voltage value using the time-stamp obtained in the previous step.
7 At each crosspoint (rising and falling) found, find the voltage differential between the crosspoint and VRefDQ. The rising and falling crosspoint voltage differential is denoted as Vix_DQS_RF and Vix_DQS_FR respectively.
8 For each cross point voltage, calculate the final result using the equation (for Rising):

$$V_{IX\_DQS\_Ratio} = 100\% \times [Vix\_DQS\_RF/Max(f(t))]$$

9 For each cross point voltage, calculate the final result using the equation (for Falling):

$$V_{IX\_DQS\_Ratio} = 100\% \times [Vix\_DQS\_FR/Min(f(t))]$$

10 Determine the worst result from the set of $V_{IX\_DQS\_Ratio}$ measured.

Expected/ Observable Results:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The calculated value of the crossing point voltage ratio ($V_{IX\_DQS\_Ratio}$) for the differential test signal pair shall be within the conformance limits as per the JEDEC specification in the References section.

Differential Signals (READ cycle tests)

Differential AC Output Levels and Slew Rate tests

VOHdiff(AC)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

11411 [VOHdiff(AC)]

LPDDR4 Test Mode

51411 [VOHdiff(AC)]

LPDDR4X (Differential) Test Mode

61411 [VOHdiff(AC)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	9.3	Table 140	VOHdiff (AC) [AC Differential output high measurement level (for output SR)]

LPDDR4 / LPDDR4X (Differential) Test Modes

There is no reference available for this test in the JEDEC specifications. The measurement result is reported as “Information Only”.

Test Overview: **DDR4 Test Mode / LPDDR4 / LPDDR4X (Differential) Test Mode**

The purpose of this test is to verify the high level voltage value of the test signal within the read burst.

Test Procedure: **DDR4 (for Test ID 11411) / LPDDR4 (for Test ID 51411) / LPDDR4X (Differential) (for Test ID 61411)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid Strobe positive pulse in the said burst.
A valid Strobe positive pulse starts at the 0V crossing at the valid Strobe rising edge and ends at the 0V crossing at the following valid Strobe falling edge.
4 Zoom into the first pulse and perform V_{TOP}.
Take the V_{TOP} measurement as $V_{OHdiff\ (AC)}$ value.
5 Repeat step 4 with the rest of the positive pulses in the specified burst.
6 Determine the worst result from the set of $V_{OHdiff\ (AC)}$ measured.

Expected/ Observable Results: **DDR4 Test Mode**

The worst measured $V_{OHdiff\ (AC)}$ shall be within the conformance limits as per the JEDEC specification in the References section.

LPDDR4 / LPDDR4X (Differential) Test Modes

The worst measured $V_{OHdiff\ (AC)}$ value for the test signal is reported as “Information Only”.

VOLdiff(AC)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

11412 [VOLdiff(AC)]

LPDDR4 Test Mode

51412 [VOLdiff(AC)]

LPDDR4X (Differential) Test Mode

61412 [VOLdiff(AC)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	9.3	Table 140	VOLdiff (AC) [AC Differential output low measurement level (for output SR)]

LPDDR4 / LPDDR4X (Differential) Test Modes

There is no reference available for this test in the JEDEC specifications. The measurement result is reported as “Information Only”.

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the low level voltage value of the test signal within the read burst.

Test Procedure: **DDR4 (for Test ID 11412) / LPDDR4 (for Test ID 51412) / LPDDR4X (Differential) (for Test ID 61412)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid Strobe negative pulses in the specified burst.
A valid Strobe negative pulse starts at the 0V crossing at the valid Strobe falling edge and ends at the 0V crossing at the following valid Strobe rising edge.
4 Zoom into the first pulse and perform V_{BASE}.
Take the V_{BASE} measurement as $V_{OLdiff\ (AC)}$ value.
5 Repeat step 4 with the rest of the negative pulses in the specified burst.
6 Determine the worst result from the set of $V_{OLdiff\ (AC)}$ measured.

Expected/ Observable Results: **DDR4 Test Mode**

The worst measured $V_{OLdiff\ (AC)}$ shall be within the conformance limits as per the JEDEC specification in the References section.

LPDDR4 / LPDDR4X (Differential) Test Modes

The worst measured $V_{OLdiff\ (AC)}$ value for the test signal is reported as “Information Only”.

SRQdiffR

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

11413 [SRQdiffR]

LPDDR4 Test Mode

51413 [SRQdiffR]

LPDDR4X (Differential) Test Mode

61413 [SRQdiffR]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	9.5	Table 144	SRQdiff [Differential output slew rate]

LPDDR4 Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.5	Table 201	SRQdiff [Differential output slew rate ($V_{OH} = V_{DDQ} / 3$)]

LPDDR4X (Differential) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4X SDRAM Specification, JEDEC Standard no. 209-4-1, January 2017	4.3	Table 15	SRQdiff [Differential output slew rate ($V_{OH} = V_{DDQ} * 0.5$)]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the differential output slew rate for rising edge of the test signal within the read burst.

Test Procedure: **DDR4 (for Test ID 11413) / LPDDR4 (for Test ID 51413) / LPDDR4X (Differential) (for Test ID 61413)**

1 Acquire and split the read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all the valid Strobe rising edges in the specified burst.
A valid Strobe rising edge starts at $V_{OLdiff(AC)}$ crossing and ends at the following $V_{OHdiff(AC)}$ crossing.

4 For all the valid Strobe rising edges, find the transition time, T_R.
T_R is the time starting at $V_{OLdiff(AC)}$ crossing and ending at the following $V_{OHdiff(AC)}$ crossing.

5 Calculate SRQdiffR using the equation:

$$SRQdiffR = [V_{OHdiff(AC)} - V_{OLdiff(AC)}] / T_R$$

6 Determine the worst result from the set of SRQdiffR measured.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of SRQdiffR for the test signal shall be within the conformance limits as per the JEDEC specification.

SRQdiffF

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

11414 [SRQdiffF]

LPDDR4 Test Mode

51414 [SRQdiffF]

LPDDR4X (Differential) Test Mode

61414 [SRQdiffF]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	9.5	Table 144	SRQdiff [Differential output slew rate]

LPDDR4 Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	7.5	Table 201	SRQdiff [Differential output slew rate ($V_{OH} = V_{DDQ} / 3$)]

LPDDR4X (Differential) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4X SDRAM Specification, JEDEC Standard no. 209-4-1, January 2017	4.3	Table 15	SRQdiff [Differential output slew rate ($V_{OH} = V_{DDQ} * 0.5$)]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the differential output slew rate for falling edge of the test signal within the read burst.

Test Procedure: **DDR4 (for Test ID 11414) / LPDDR4 (for Test ID 51414) / LPDDR4X (Differential) (for Test ID 61414)**

1 Acquire and split the read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all the valid Strobe falling edges in the specified burst.
A valid Strobe falling edge starts at $V_{OHdiff(AC)}$ crossing and ends at the following $V_{OLdiff(AC)}$ crossing.

4 For all the valid Strobe falling edges, find the transition time, T_F.
T_R is the time starting at $V_{OHdiff(AC)}$ crossing and ending at the following $V_{OLdiff(AC)}$ crossing.

5 Calculate SRQdiffF using the equation:

$$SRQdiffF = [V_{OHdiff(AC)} - V_{OLdiff(AC)}] / T_F$$

6 Determine the worst result from the set of SRQdiffF measured.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of SRQdiffF for the test signal shall be within the conformance limits as per the JEDEC specification.

5 Timing Tests

Overview

The following groups of tests pertain to the timing operating conditions of a DDR4 DRAM as defined in JEDEC specifications. The tests consist of a simple triggering test, which is further divided into Clock Timing tests, Data Strobe Timing tests, Data Mask Timing tests and Command & Address Timing tests.

DDR Read/Write Separation [Electrical and Timing Tests]

Most of the tests must be run on specific Read burst or Write burst region. Therefore, it becomes essential to separate read and write bursts. Table 8 shows a list of Burst Triggering Methods for Read/Write Separation.

Table 8 Burst Triggering Methods for Read/Write Separation

Burst Triggering Method	Description	Signals used to evaluate Read or Write	Available in DDR4	Available in LPDDR4	Available in LPDDR4X
DQS-DQ Phase Difference	Use phase difference between DQS and DQ to differentiate Read and Write	DQS and DQ	Yes	Yes	Yes
Pre-Amble Pattern	Use DQS preamble pattern to differentiate Read and Write	DQS Only	No	Yes	Yes
Rd or Wrt Only	Does not differentiate Read and Write. It assumes that all available bursts in acquisition are bursts of interest.	DQS Only	Yes	Yes	Yes
MSOx Logic Triggering	Uses digital logic state to define burst type (Read/Write) and start and end location of the burst	DQS, DQ, and digital signal (from the oscilloscope)	Yes	No	No

Figure 61 to Figure 63 show flowcharts depicting the process of read and write separation.

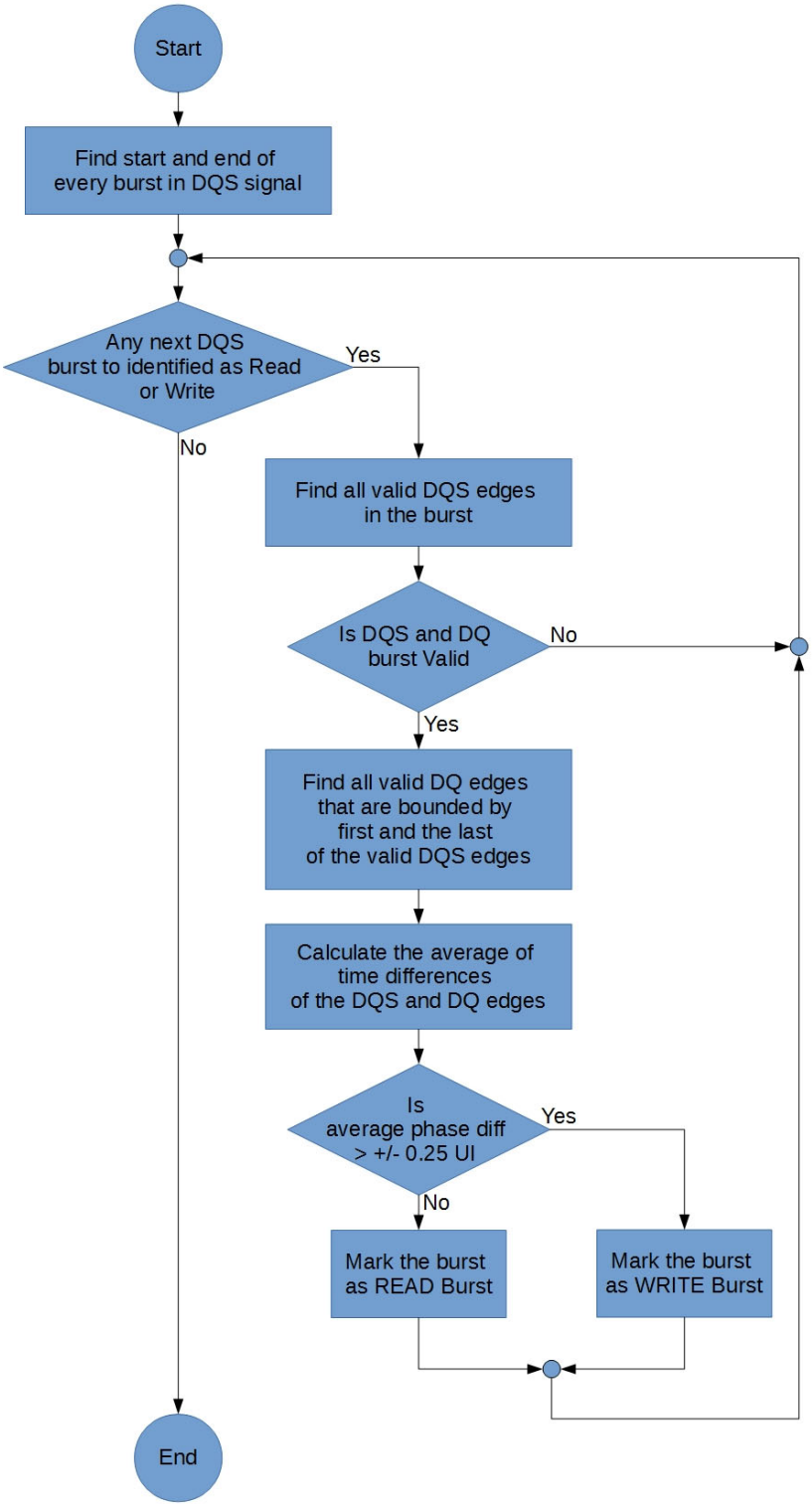


Figure 61 Flowchart depicting DQS-DQ Phase Difference

NOTE

A DQS burst is considered valid when the first edge has more than 2.5 UI of spacing from the start of the signal and the last edge must have more than 2.0 UI spacing towards the end of the signal.

A DQ burst is considered valid if at least one transition occurs. A valid transition must be at a minimum of 250mV.

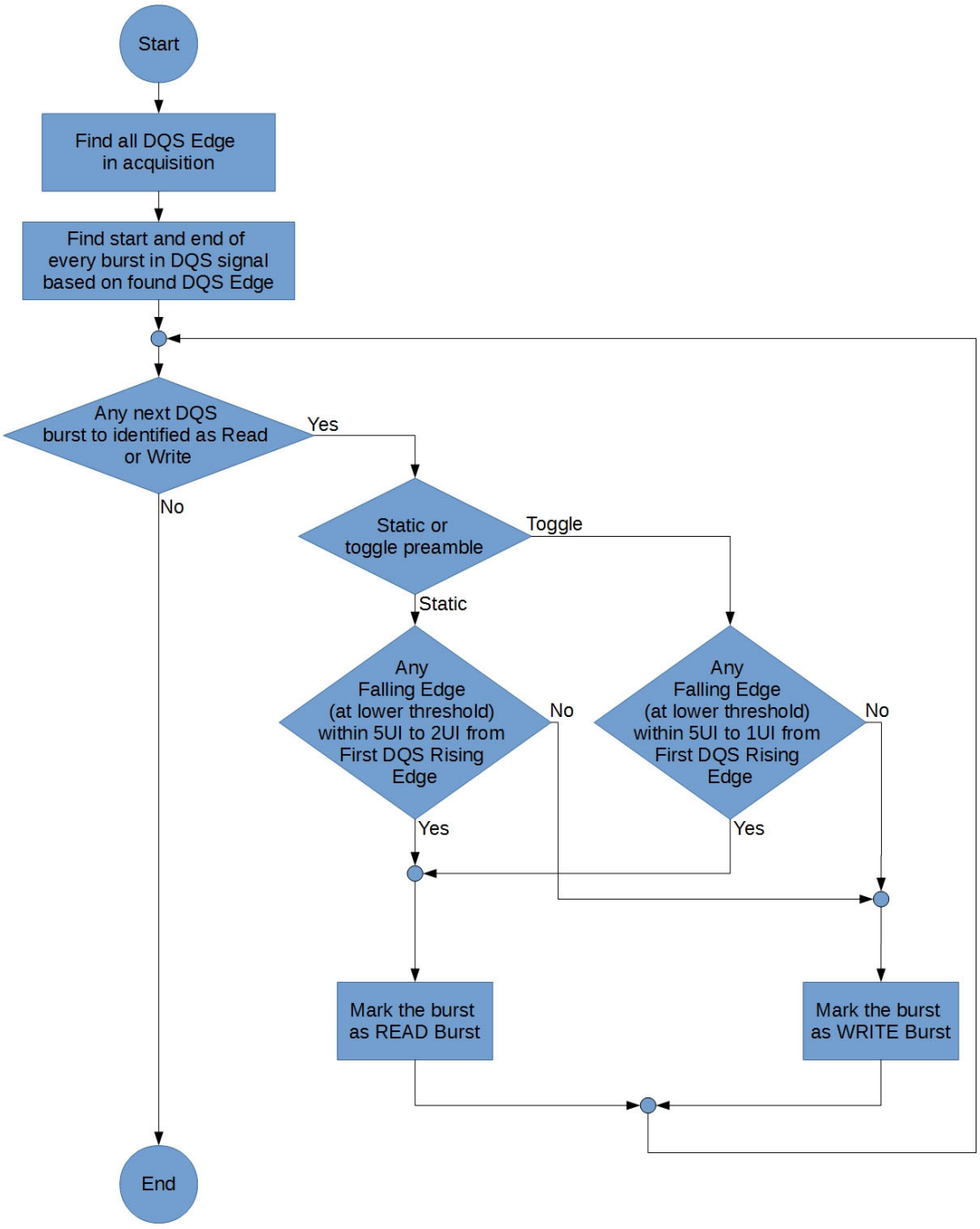


Figure 62 Flowchart depicting Pre-Amble pattern

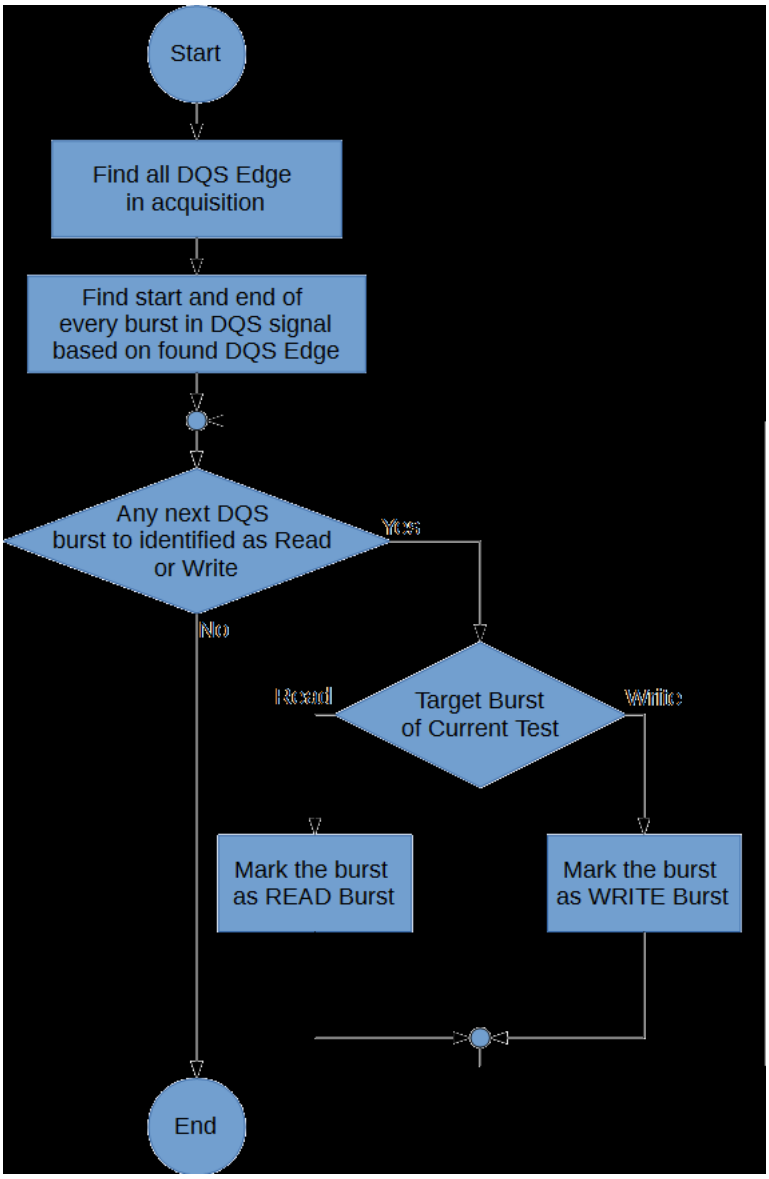


Figure 63 Flowchart depicting Read/Write Only process

Handling DDR4 “2T timing”

You may either enable or disable the “2T timing” mode using the label “Clocking Method” under the Configure tab of the Compliance test application. To access this label in the compliance test application, select **Configure > Timing Tests > Command Address Timing**.

To enable the “2T timing” support feature, the compliance test application uses the second closest rising clock edge (instead of using the closest rising edge in the typical “1T timing” feature) with reference to the CA (Command/Address) edge, when processing the tIS(base) test. Figure 64 shows the screen capture of sample waveforms that display the impact of enabling the “2T timing” feature.

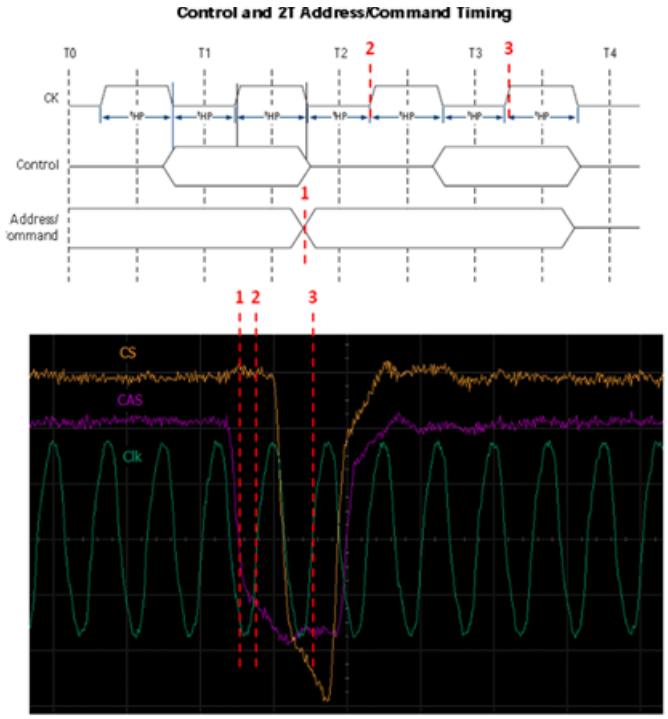


Figure 64 Impact of enabling the “2T Timing” feature

Based on Figure 64, the tIS(base) test measures the time difference between line position:

- #1(CA) and #2(Clock), for normal “1T timing” mode
- #1(CA) and #3(Clock), for “2T Timing” mode

One of the primary assumptions in this approach is that the transition edge of the CA PUT occurs after line position #2 (as designed). The limitation to this approach is in those situations when the CA transition edge occurs before line position #2 due to any reason, such as extremely bad slew or issues with signal integrity. In such cases, this approach is not successful. However, Keysight has not yet faced any such challenges and is unaware of the existence of any such scenarios.

NOTE **The approach described above works well with any typical DDR4 DUT system operating under the “2T Timing” mode.**

Threshold Settings

The DDR4/LPDDR4 Compliance Test Application consists of two groups of threshold settings in the Configure tab:

- Burst Trigger Threshold Settings

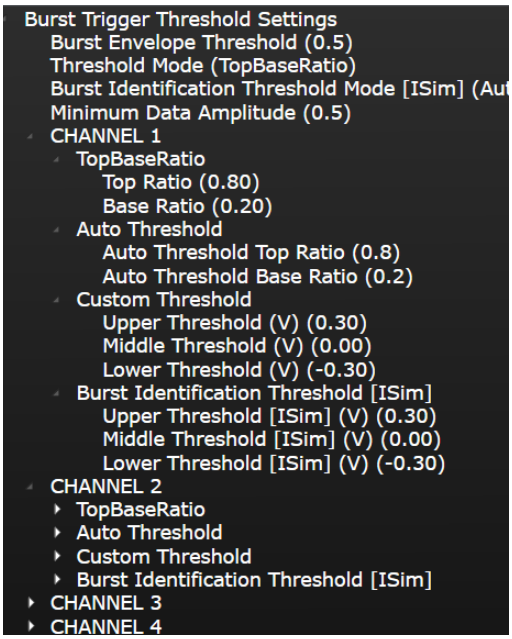


Figure 65 Burst Trigger Threshold Settings under Configure tab

The Burst Trigger Threshold settings are hidden when the MSOx Logic Triggering method is selected. Instead, MSOx Logic Input Settings are defined. The logic state, latency, and burst length settings can completely define the burst start and end location.

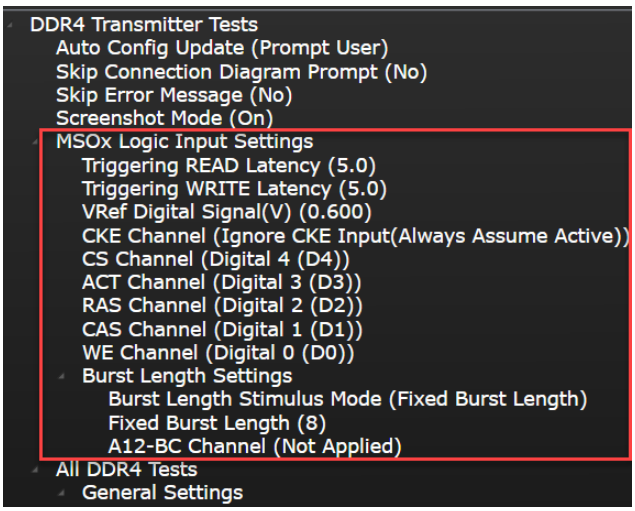


Figure 66 MSOx Logic Input Settings under Configure tab

- Signal Measurement Threshold Settings

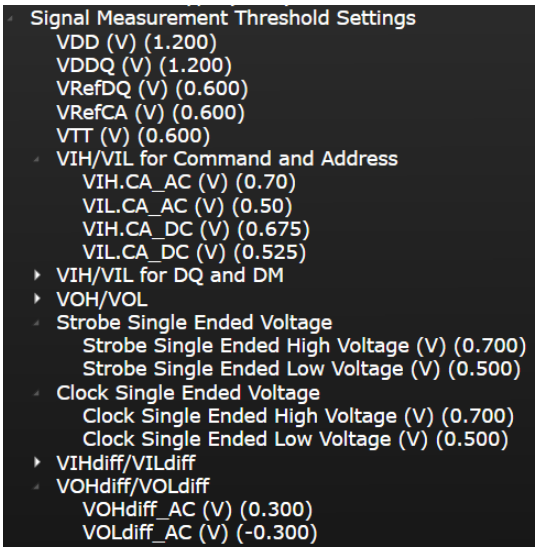


Figure 67 Signal Measurement Threshold Settings (for DDR4)

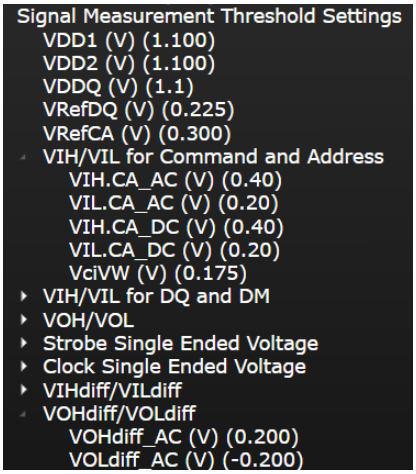


Figure 68 Signal Measurement Threshold Settings (for LPDDR4)

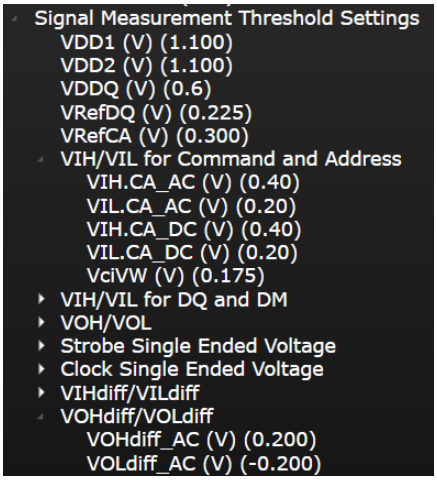


Figure 69 Signal Measurement Threshold Settings (for LPDDR4X)

Threshold Settings for tests that require Read/Write Separation

- All DDR4 Tests
  - Electrical Tests
    - Single-Ended Signals
      - WRITE cycle tests
        - VSEH/VSEL for Strobes Plus
        - VSEH/VSEL for Strobes Minus
      - READ cycle tests
        - VOH/VOL
        - Output Slew Rate
    - Differential Signals
      - WRITE cycle tests
        - Differential AC Input Levels for Strobe
        - Strobe Cross Point Voltage Test
      - READ cycle tests
        - Differential AC Output Levels and Slew Rate tests
  - Timing Tests
    - WRITE cycle tests
      - Data Strobe Timing
    - READ cycle tests
      - Data Timing
      - Data Strobe Timing
- All LPDDR4 Tests
  - Electrical Tests
    - Single-Ended Signals
      - WRITE cycle tests
        - VSEH/VSEL for Strobes Plus
        - VSEH/VSEL for Strobes Minus
      - READ cycle tests
        - VOH/VOL
        - Output Slew Rate
    - Differential Signals
      - WRITE cycle tests
        - Strobe Cross Point Voltage Test
      - READ cycle tests
        - Differential AC Output Levels and Slew Rate tests
  - Timing Tests
    - WRITE cycle tests
      - Data Strobe Timing
    - READ cycle tests
      - Data Timing
      - Data Strobe Timing

Both Burst Trigger Threshold Settings and Signal Measurement Threshold Settings affect the test runs on the category of tests listed above.

Basic process flow for tests that require Read/Write Separation

To understand the concept mentioned in the previous section in a better manner, refer to the block diagram shown in Figure 70 to understand the process flow of tests that require Read/Write Separation:

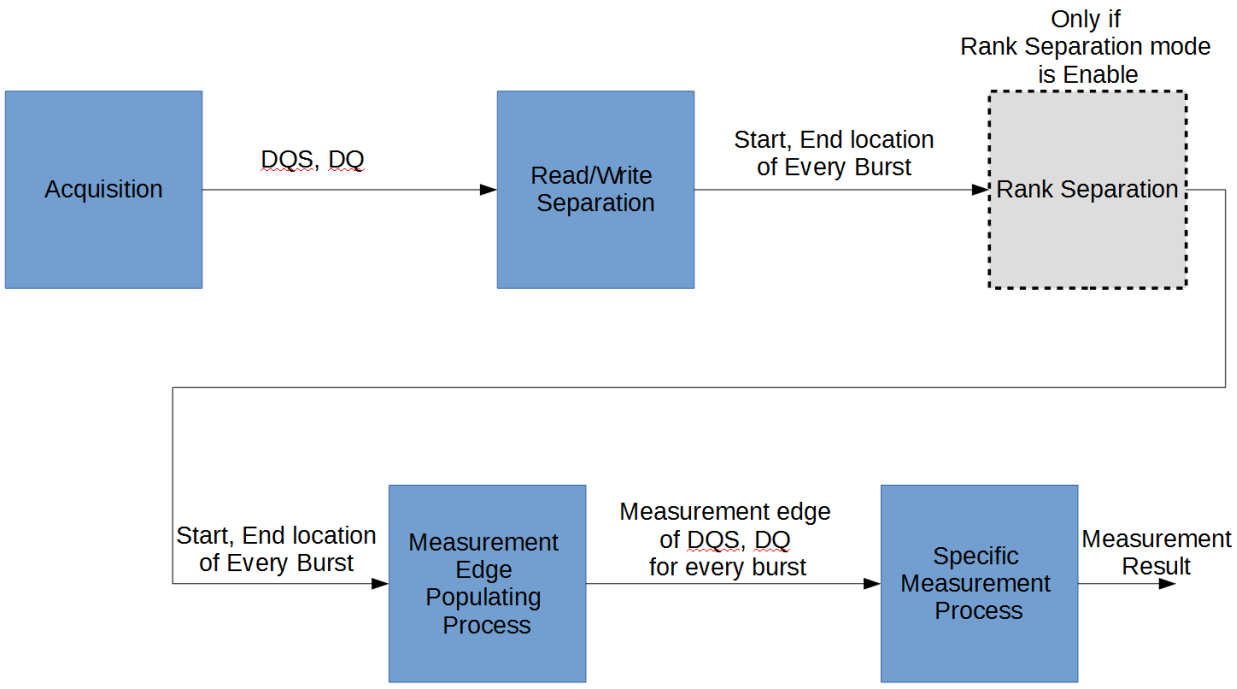


Figure 70 Process flow for tests requiring Read/Write Separation

Each threshold setting has a separate impact on each block in the process flow shown in Figure 70. Table 9 gives a better understanding about whether or not the threshold settings impacts a certain block in the process flow.

Table 9 Impact of Threshold Settings on the Process Flow

Threshold Settings	Acquisition	Read/Write Separation	Rank Separation	Measurement Edge Populating Process	Specific Measurement Process
Burst Trigger Threshold Settings	No Impact	Impacts	No Impact	No Impact	No Impact
Signal Measurement Threshold Settings	No Impact	No Impact	No Impact	Impacts	Impacts

In a nutshell, Table 9 indicates that Burst Trigger Threshold Settings affect the Read/Write Separation block only and the Signal Measurement Threshold Settings affect the Measurement Edge Populating Process and Specific Measurement Process blocks.

Burst Trigger Threshold Settings

NOTE

1. Due to legacy development of the DDR4 Compliance Test Application, the configuration that relates to TopBase and Custom Threshold modes are applied only when “Burst Triggering Method” is set to “DQS-DQ Phase Difference” or “Rd or Wrt ONLY”. The Auto Threshold mode configurations are applied only when “Burst Triggering Method” is set to “DQS-DQ Phase Difference”. The TopBase and Custom Threshold modes are not applied when “Burst Triggering Method” is set to “Pre-Amble Pattern”.
2. If you set “Burst Triggering Method” to “Pre-Amble Pattern”, the configuration applied is:
   - DQS Upper Threshold for Burst Trigger Method
   - DQS Middle Threshold for Burst Trigger Method
   - DQS Lower Threshold for Burst Trigger Method

   In a future version of the DDR4 Compliance Test Application, the three configuration values listed above may be removed and all Burst Trigger Threshold settings will be defined by the configuration of TopBase and Custom Threshold.

The objective of using Burst Threshold Settings is to define the upper, middle and lower threshold settings on DQS and DQ signals for Read/Write Separation so as to produce a series of bursts. In other words, the correct configuration for Burst Trigger Threshold Settings yields number of Bursts detected, as shown in Figure 71.

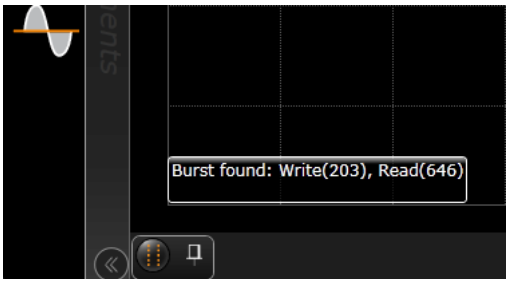


Figure 71 Burst detected for correct Burst Trigger Threshold Settings

While the signal may have actual bursts, an incorrect configuration for Burst Trigger Threshold Settings does not yield any burst, as shown in Figure 72.

Figure 72 Burst not detected for incorrect Burst Trigger Threshold Settings

The Burst Trigger Threshold Settings consists of three modes, namely, TopBase Ratio, Custom Threshold, and Auto Threshold. Figure 73 shows the appearance of the Threshold Mode configuration variable under the Configure tab when TopBaseRatio mode is selected. Figure 77 shows the appearance of the Threshold Mode configuration variable under the Configure tab when Custom Threshold mode is selected. Figure 84 shows the appearance of the Threshold Mode configuration variable under the Configure tab when Auto Threshold mode is selected.

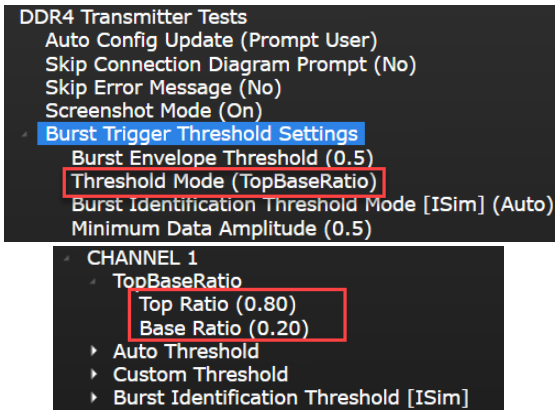


Figure 73 TopBase Ratio mode under Burst Trigger Threshold Settings

TopBase Ratio mode In the TopBase Ratio mode, the Compliance Test Application performs VTop and VBase measurements on the DQS and DQ signals. Further, the application calculates the threshold using the equations:

For DQS signals:

$$UpperThreshold_{DQS} = TopRatio_{DQS} \times [(VTop_{DQS} - VBase_{DQS}) + VBase_{DQS}]$$

$$LowerThreshold_{DQS} = BaseRatio_{DQS} \times [(VTop_{DQS} - VBase_{DQS}) + VBase_{DQS}]$$

$$MiddleThreshold_{DQS} = 0.5 \times (UpperThreshold_{DQS} + LowerThreshold_{DQS})$$

For DQ signals:

$$UpperThreshold_{DQ} = TopRatio_{DQ} \times [(VTop_{DQ} - VBase_{DQ}) + VBase_{DQ}]$$

$$LowerThreshold_{DQ} = BaseRatio_{DQ} \times [(VTop_{DQ} - VBase_{DQ}) + VBase_{DQ}]$$

$$MiddleThreshold_{DQ} = 0.5 \times (UpperThreshold_{DQ} + LowerThreshold_{DQ})$$

The TopBase Ratio mode is useful because you do not have to manually evaluate the threshold levels of the signals, which otherwise, may be time consuming. However, in order for this mode to function properly, you must ensure that the following requirements are met:

1 The sufficient amplitude for DQS (Typical minimum range is from 200mV to -200mV. Preferred range is from 400mV to -400mV).

2 The sufficient amplitude for DQ (Typical minimum value is the 200mVpp center at Compliance Vref/Vcent. Preferred value is the 400mVpp center at Compliance Vref/Vcent).

3 The amplitude for Read and Write must be approximately the same, within 20% tolerance.

4 The High Impedance (Idle) level is around the middle level of the burst. If that level is at a higher or lower level than the burst amplitude (as shown in Figure 74), TopBase Ratio mode may not be effective.

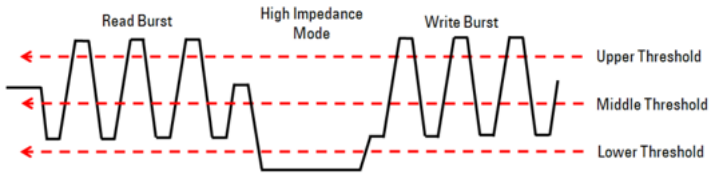


Figure 74 High Impedance (Idle) Level

5 The voltage across High Impedance (Idle) Level should not vary more than 10% of the burst amplitude.

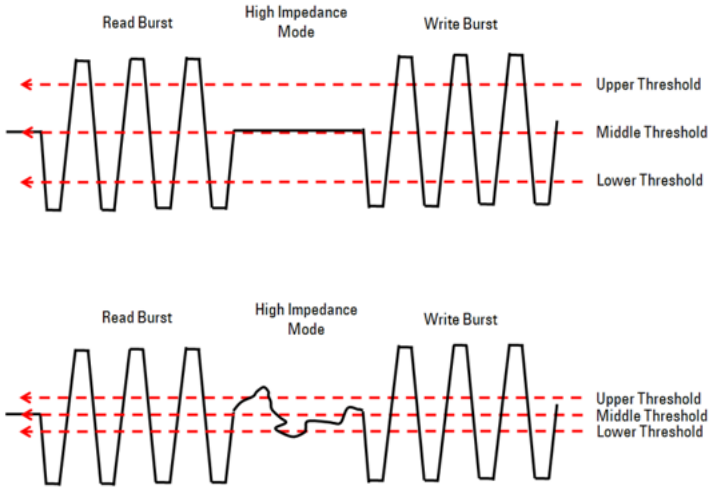


Figure 75 Voltage across High Impedance (Idle) Level

6 Ringing after the burst must be small; preferably within 10% of the burst amplitude.

Figure 76 shows an ideal signal with TopBase Ratio mode set for Burst Trigger Threshold Settings.

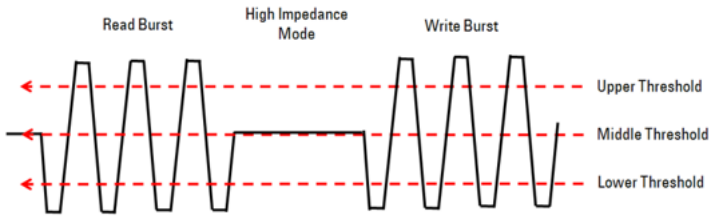


Figure 76 Sample of an ideal signal for TopBase Ratio mode

In case there is an actual burst on the signal but no burst is detected under TopBase Ratio mode of the Burst Trigger Threshold Settings, it indicates that any one of the six conditions defined above have not been met. Therefore, Keysight recommends implementing the Custom Threshold mode in Burst Trigger Threshold Settings.

Custom Threshold mode Custom Threshold mode relies on your inputs to define the threshold levels of the signals, specially for such signals where applying any algorithm becomes challenging.

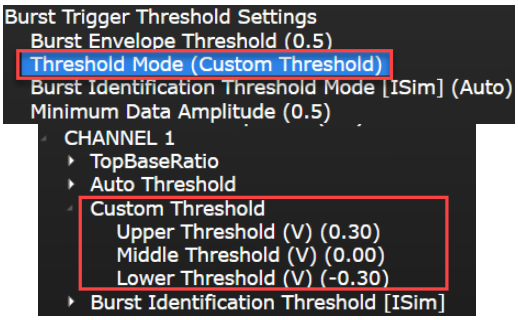


Figure 77 Custom Threshold mode under Burst Trigger Threshold Settings

In order to implement this mode, you must manually define the upper, middle and lower threshold levels for each Channel according to the configuration value that you have entered.

To understand the advantage of using Custom Threshold mode, let us consider two cases:

1 Non-Ideal High Impedance Voltage – In the signal shown in Figure 78, the amplitude of the high impedance voltage is below the Read and Write amplitude. In such a situation, when the Compliance Test Application automatically determines the appropriate threshold level using the TopBase Ratio mode, the high impedance voltage complicates the algorithm within the application. The upper, middle and lower threshold levels, which are calculated under the TopBase Ratio mode, do not meet the requirements for valid Read and Write bursts. Hence, the application is unable to determine any valid Read or Write bursts. Eventually, the application is unable to perform any measurements or the measurements are erroneous.

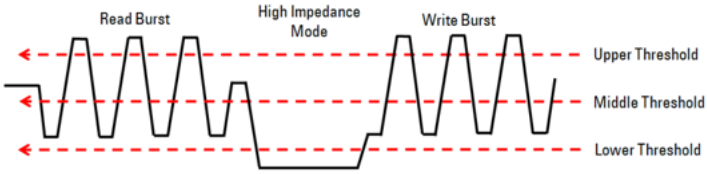


Figure 78 Signal with a non-ideal high impedance voltage amplitude

To avoid such a situation, use the Custom Threshold mode to re-define the Trigger threshold levels that enables the Compliance Test Application to trigger on both Read and Write bursts.

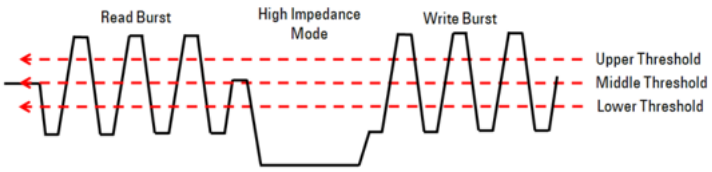


Figure 79 Signal with custom threshold levels defined

2 Different Amplitudes of Read and Write Bursts – In the signal shown in Figure 80, the amplitude of the Read burst is significantly higher than that of the Write burst. In this situation, the Compliance Test Application uses the TopBase Ratio mode to automatically determine the upper, middle and lower threshold levels according to the VTop and VBase measurements performed on the actual signal. With the calculated threshold levels, the application triggers on only the Read burst because the edge meets the threshold condition. However, it does not trigger on the Write burst. Therefore, when the application runs the Write cycle tests, it is unable to find the required Write signals. Eventually, the application performs invalid or erroneous measurements. Note that there may be signals where the amplitude of the Write burst is

significantly higher than that of the Read burst. In such cases, the application is unable to find the required Read signals when running tests.

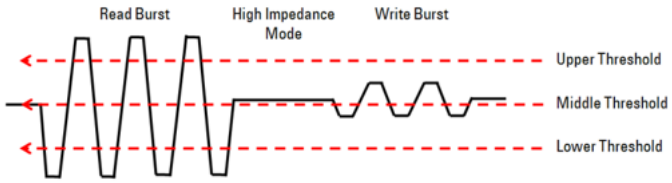


Figure 80 Signal with a non-ideal high impedance voltage amplitude

To avoid such a situation, use the Custom Threshold mode to re-define the Trigger threshold levels that enables the Compliance Test Application to trigger on both Read and Write bursts.

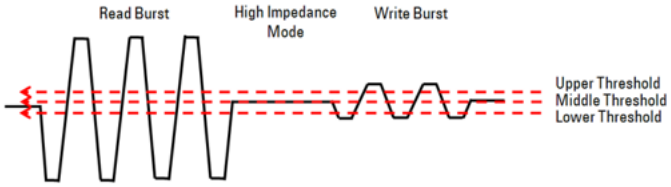


Figure 81 Signal with custom threshold levels defined

Burst Envelope Threshold is used for burst detection in Read Write Separation. In the early processing of Read Write Separation, the application performs an enveloping process on the DQS signal. Therefore, a DQS enveloped signal indicates better recognition of burst. Any enveloped burst that is above 50% of Vmode (the default Burst Envelope Threshold in 0.5) of the “All Enveloped Burst” is considered as the “recognized burst”, whereas anything below the 50% threshold is considered “noise” even if it is a very small amplitude burst. Consider the waveform in Figure 82.

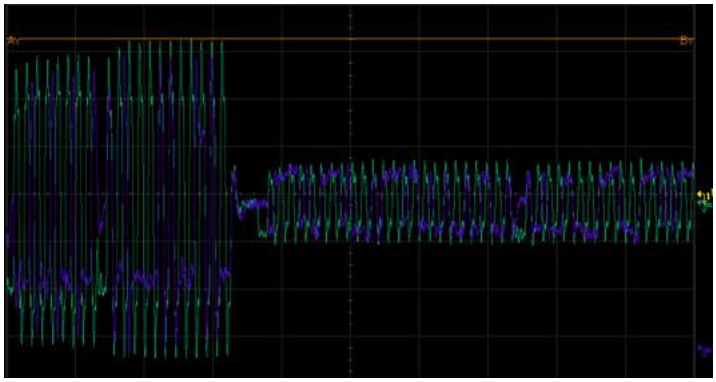


Figure 82 Example of a Waveform with an All Enveloped Burst

In the sample waveform shown in Figure 82, the larger burst has a DQS amplitude of 500mV and the smaller burst has a DQS amplitude of 150mV.

The default Burst Envelope Threshold, which is 0.5, yields to a threshold at 250mV, which is calculated as (50% x 500mV). Eventually, the smaller burst, which has a DQS amplitude at 150mV, is not recognized as a burst since it is not bigger than the calculated threshold of 250mV.

In such cases, reduce the threshold level in order to include even the smaller burst as a “recognized burst”. The equations for the recommended calculation are:

BurstEnvelopeThreshold < AmplitudeSmallerBurst / AmplitudeBiggerBurst

BurstEnvelopeThreshold < (150mV) / (500mV)

BurstEnvelopeThreshold < 0.3

Therefore, you may use a BurstEnvelopeThreshold value of 0.25, which is slightly lesser than the calculated 0.3.

By changing the BurstEnvelopeThreshold to 0.25, the threshold level in this case is 125mV, which is calculated as (25% x 500mV). Eventually, the smaller burst is also recognized since its amplitude is 150mV, which is above 125mV.

Minimum Data Amplitude is used to filter the recognized burst for further processing. If the recognized burst has a DQ amplitude, which is larger than 0.5V (the default minimum data amplitude), this burst is used for further processing. It means that any recognized burst that has a DQ amplitude lower than 0.5V is discarded from further processing. You may configure the Minimum Data Amplitude to suit a custom signal, which may have a DQ amplitude lower than 0.5V.

Auto Threshold mode The Auto Threshold mode combines a clustering algorithm with a machine learning model to predict the correct thresholds for a given signal. No manual threshold setting is needed in this case. The mode consists of two steps:

1 Run a clustering algorithm on the signal. This builds clusters of similar data points that help determine the lower and upper threshold values (see Figure 83). For nearly symmetrical signals, these thresholds can detect bursts even though the amplitude between Read and Write differ by more than 20%.

2 If the cluster algorithm detects an unsymmetrical signal, the machine learning model takes over the prediction of the thresholds. The model was trained on features of variously shaped signal data. These features include a histogram of the signal, statistical moments such as mean and variance and percentile ranks.

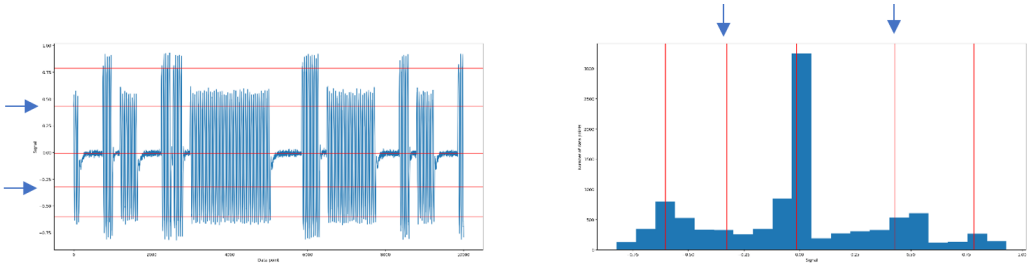


Figure 83 Clustering algorithm used in Auto Threshold mode

The machine learning model was explicitly also trained on signal data where the High Impedance (Idle) level is not around the middle level of the burst but that level is at a higher or lower level than the burst amplitude itself. Therefore, the model can predict reasonable thresholds for this kind of signals.

Similar to the TopBase Ratio mode, the Auto Threshold Mode also offers a possibility to change the threshold calculation for DQS and DQ signal via the Auto Threshold parameter (see Figure 84).

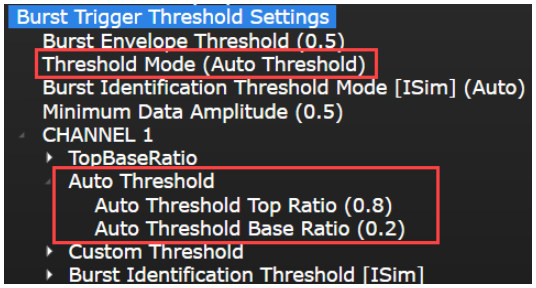


Figure 84 Auto Threshold mode under Burst Trigger Threshold Settings

The thresholds predicted by the clustering algorithm/the machine learning model are calculated using the equations:

For DQS signal:

$UpperThreshold_{DQS} = AutoThresholdTopRatio_{DQS} \times [(PredictedUpperThreshold_{DQS} - PredictedLowerThreshold_{DQS}) + PredictedLowerThreshold_{DQS}]$

$LowerThreshold_{DQS} = AutoThresholdBaseRatio_{DQS} \times [(PredictedUpperThreshold_{DQS} - PredictedLowerThreshold_{DQS}) + PredictedLowerThreshold_{DQS}]$

$MiddleThreshold_{DQS} = 0.5 \times (UpperThreshold_{DQS} + LowerThreshold_{DQS})$

For DQ signals:

$UpperThreshold_{DQ} = AutoThresholdTopRatio_{DQ} \times [(PredictedUpperThreshold_{DQ} - PredictedLowerThreshold_{DQ}) + PredictedLowerThreshold_{DQ}]$

$LowerThreshold_{DQ} = AutoThresholdBaseRatio_{DQ} \times [(PredictedUpperThreshold_{DQ} - PredictedLowerThreshold_{DQ}) + PredictedLowerThreshold_{DQ}]$

$MiddleThreshold_{DQ} = 0.5 \times (UpperThreshold_{DQ} + LowerThreshold_{DQ})$

Signal Measurement Threshold Settings

For tests that require Read/Write Separation, the Compliance Test Application uses some of the configuration done under Signal Measurement Threshold Settings as the threshold to define the measurement edge, which is used further for specific measurements.

Figure 85 to Figure 89 show the configuration that is used to define the edge threshold for each type of signal:

1 For Differential DQS signal (Write Burst)

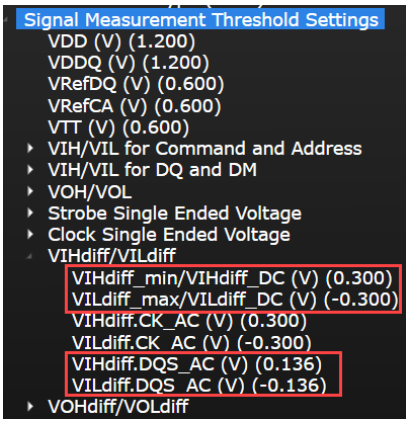


Figure 85 Signal Measurement Threshold Settings for Differential DQS signal (Write Burst)

2 For Differential DQS signal (Read Burst)

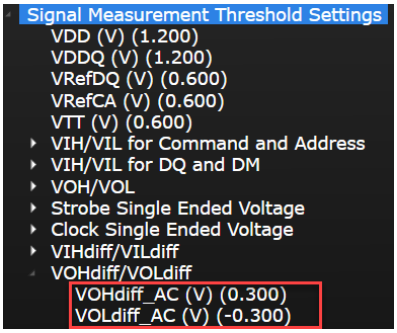


Figure 86 Signal Measurement Threshold Settings for Differential DQS signal (Read Burst)

3 For DQ and Single-ended DQS signals (Write Burst)

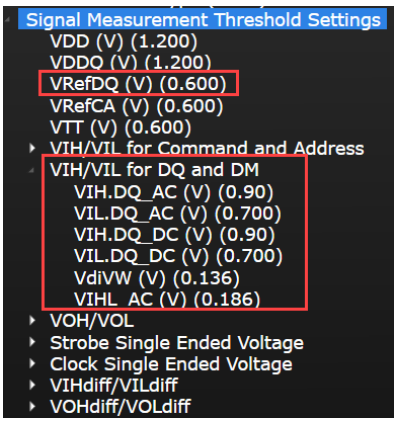


Figure 87 Signal Measurement Threshold Settings for DQ and Single-ended DQS signals (Write Burst)

4 For DQ and Single-ended DQS signals (Read Burst)

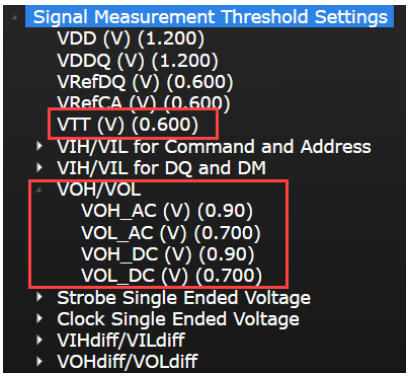


Figure 88 Signal Measurement Threshold Settings for DQ and Single-ended DQS signals (Read Burst)

5 For Clock signal

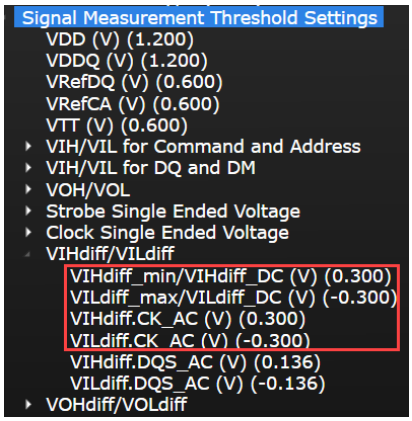


Figure 89 Signal Measurement Threshold Settings for Clock signal

Following examples describe the dependency of certain tests on the configuration variables:

- Example 1: tDQSH (Write Burst; DQS and DQ signal)

The test procedure for tDQSH states:

1 Acquire and split the read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising and falling DQS crossings in the specified burst.
4 tDQSH is the time starting from a rising edge of the DQS and ending at the following falling edge.
5 Collect all values of the tDQSH measured.
6 Determine the worst result from the set of tDQSH measured.

After identifying the target burst in step 2 of the procedure, it is required that the measurement edge be populated in step 3. Therefore, the configuration variables that defines the measurement edge in step 3 are:

- VIHdiff.DQS_AC
- VILdiff.DQS_AC
- VIHdiff_min/VIHdiff_DC
- VILdiff_min/VILdiff_DC

The middle cross-point level of differential DQS is 0V. Notice that in this case, VIHdiff is considered instead of VOHdiff, as this test involves the Write burst.

Besides, the configuration for DQ signal is also used to check the validity of the burst. If the DQ transition is unable to meet the threshold settings listed below, that burst is considered invalid and is not considered or used for measurements, even if the DQS edge is valid.

- VIH.DQ_AC
- VIL.DQ_AC
- VIH.DQ_DC
- VIL.DQ_DC
- VRefDQ

- Example 2: tDQSQ (Read Burst; DQS and DQ signal)

The test procedure for tDQSQ states:

1 Acquire and split the read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQ crossings at Vref / V_{TT} in the specified burst.
4 For all DQ crossings found in the previous step, locate the nearest DQS crossing (Rising or Falling).
5 tDQSQ is measured as the time difference from DQ crossing to DQS crossing.
6 Determine the worst result from the set of tDQSQ measured.

After identifying the target burst in step 2 of the procedure, it is required that the measurement edge be populated in step 3. Therefore, the configuration variables that defines the measurement edge in step 3 are:

- VOH_AC
- VOL_AC
- VOH_DC
- VOL_DC
- VTT

Notice that in this case, VOH is considered instead of VIH, as this test involves the Read burst.

Besides, the configuration for DQS signal is also used to check the validity of the burst. If the DQS transition is unable to meet the threshold settings listed below, that burst is considered invalid and is not considered or used for measurements, even if the DQ edge is valid.

- VOHdiff_AC
- VOLdiff_AC

- Example 3: tDQSCK (Read Burst; DQS, DQ and CLK signal)

The test procedure for tDQSCK states:

1 Acquire and split the read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising DQS crossings at 0V in the specified burst.
4 For all DQS crossings found in the previous step, locate the nearest rising Clock crossing at 0V.
5 tDQSCK is measured as the time difference from DQS crossing to the corresponding Clock crossing.
6 Report the measured value of tDQSCK.

After identifying the target burst in step 2 of the procedure, it is required that the measurement edge be populated in step 3. Therefore, the configuration variables that defines the measurement edge in step 3 are:

- VOHdiff_AC
- VOLdiff_AC

Notice that in this case, VOHdiff is considered instead of VIHdiff, as this test involves the Read burst.

This test also requires the clock edge in step 4. Therefore, the configuration variables that defines the measurement edge for the clock signal in step 4 are:

- VIHdiff.CK_AC
- VILdiff.CK_AC
- VIHdiff_min/VIHdiff_DC
- VILdiff_min/VILdiff_DC

Besides, the configuration for DQ signal is also used to check the validity of the burst. If the DQ transition is unable to meet the threshold settings listed below, that burst is considered invalid and is not considered or used for measurements, even if the DQS edge is valid.

- VOH_AC
- VOL_AC
- VOH_DC
- VOL_DC
- VTT

Threshold Settings for tests that do not require Read/Write Separation

- All DDR4 Tests
  - Electrical Tests
    - Single-Ended Signals
      - WRITE cycle tests
        - VSEH/VSEL for Clocks Plus
        - VSEH/VSEL for Clocks Minus
        - VIH/VIL for Command and Address
      - Overshoot/Undershoot (Address, Control)
      - Overshoot/Undershoot (Data, Strobe, Mask)
      - Overshoot/Undershoot (Clock)
      - Vref Signal Test
    - Differential Signals
      - WRITE cycle tests
        - Differential AC Input Levels for Clock
        - Clock Cross Point Voltage Test
  - Timing Tests
    - Clock Timing
      - Rising Edge Measurements
      - Pulse Measurements
    - Command Address Timing
- All LPDDR4 Tests
  - Electrical Tests
    - Single-Ended Signals
      - WRITE cycle tests
        - VSEH/VSEL for Clocks Plus

        - VSEH/VSEL for Clocks Minus
      - Overshoot/Undershoot (Address, Control)
      - Overshoot/Undershoot (Data, Strobe, Mask)
      - Overshoot/Undershoot (Clock)
    - Differential Signals
      - WRITE cycle tests
        - Differential AC Input Levels for Clock
        - Clock Cross Point Voltage Test
- Timing Tests
  - Clock Timing
    - Rising Edge Measurements
    - Pulse Measurements

The Burst Trigger Threshold Settings do not impact the test runs on the category of tests listed above, since the test measurements are not burst related. Only Signal Measurement Threshold Settings impact this category of tests.

Signal Measurement Threshold Settings

For tests that do not require Read/Write Separation, the Compliance Test Application uses some of the configuration done under Signal Measurement Threshold Settings only:

- as threshold to define the measurement edge, which is used further for specific measurements.
- as threshold to check the transition requirement of signal. For example, Overshoot tests for DQ that requires signal to be measured have at least one transition.

Figure 90 to Figure 92 show the configuration that is used to define the edge threshold for each type of signal:

1 For DQ and Single-ended DQS signals

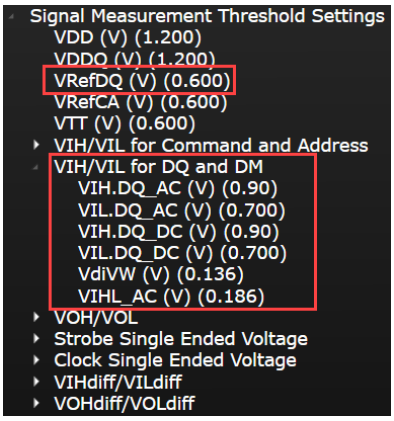


Figure 90 Signal Measurement Threshold Settings for DQ and Single-ended DQS signals

2 For Differential Clock signal

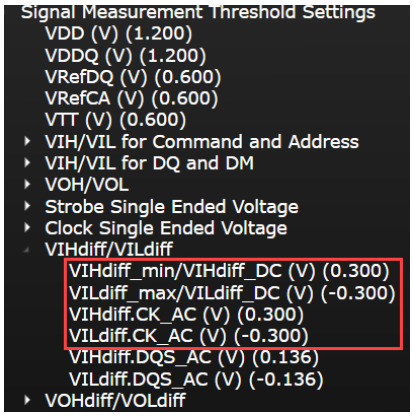


Figure 91 Signal Measurement Threshold Settings for Differential Clock signal

3 For Command/Address and Single-ended Clock signals

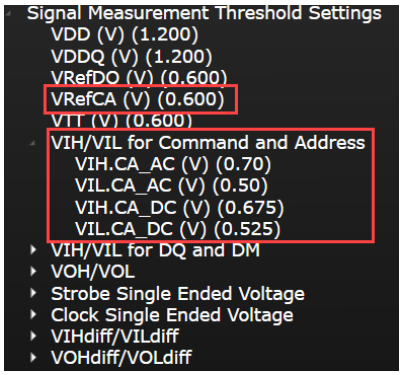


Figure 92 Signal Measurement Threshold Settings for Command/Address and Single-ended Clock signals

Following example describes the dependency of certain tests on the configuration variables:

- Example 1: tIS(base)

The test procedure for tIS(base) states:

1 Acquire and validate that the Clock and CA signals cross the thresholds.
2 Find all the edges on the Clock and CA signals.
3 Perform the setup time measurement:
   a At every rising edge of the acquired and the valid CA signal on the upper threshold, find:
   - the first closest rising edge of the Clock at the middle threshold for 1T clocking method
   - the second closest rising edge of the Clock at the middle threshold for 2T clocking method

   b To manually configure the clocking method, you may modify the label “Clocking Method” in the Configure tab of the Compliance Test Application.
4 Report the minimum value of the measurement as the test result.

The configuration variables that define the measurement edge for clock signal in step 2 of the procedure are:

- VIHdiff.CK_AC
- VILdiff.CK_AC
- VIHdiff_min/VIHdiff_DC
- VILdiff_min/VILdiff_DC

The middle cross-point level of differential DQS is 0V.

For the CA signal, the measurement threshold used are:

- VIH.CA_AC
- VIL.CA_AC
- VIH.CA_DC
- VIL.CA_DC
- VRefCA

High-Z / Low-Z Begin Point

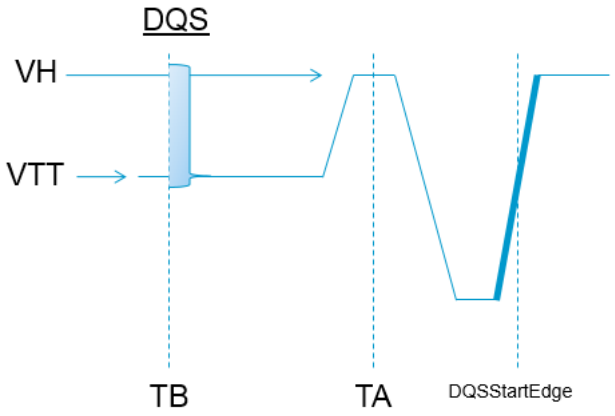
Table 10 lists the compliance tests of interest.

Table 10 Compliance tests of interest for DDR4 and LPDDR4 technology

Technology	Compliance Tests of Interest	Test ID
DDR4	tWPRE	30111
	tWPST	30112
	tLZDQ	30102
	tHZDQ	30101
	tRPRE	30113
	tRPST	30114
	tLZDQS	30118
	tHZDQS	30181
LPDDR4	tWPRE	50111
	tWPST	50112
	tRPRE	50113
	tRPST	50114

Finding tLZBeginPoint(DQS) for READ data burst

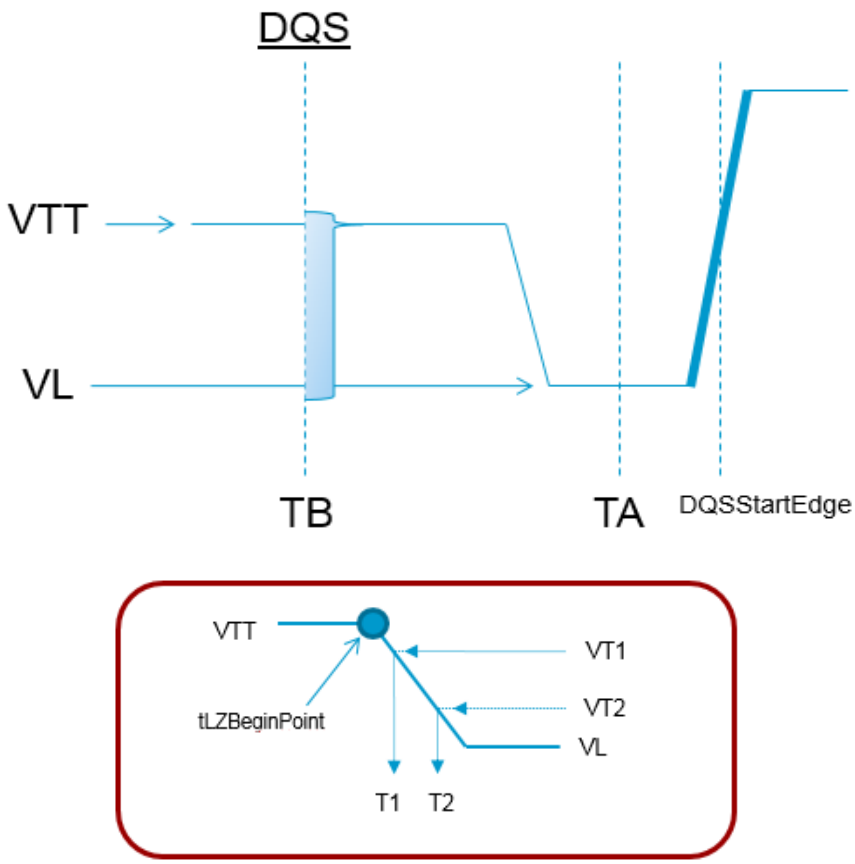
- Supported Test Mode: DDR4 (tRPRE Test)



Steps:

1 TA = DQSStartEdge – 1.5UI
2 TB = DQSStartEdge – 3.0UI
3 Form a histogram(vert) bounded by TA & TB
4 VTT = Histogram Min
5 VT1 = 0.26 * VDDQ
6 VT2 = 0.34 * VDDQ
7 tLZBeginPoint = [(T2 - T1) / (VT2 - VT1)] * [(VTT - VT2) + T2]

- Supported Test Mode: LPDDR4 (tRPRE Test)



Steps:

1 TA = DQSStartEdge – 0.5UI
2 TB = DQSStartEdge – 5.5UI
3 Form a histogram(vert) bounded by TA & TB
4 VTT = Histogram Max
5 VT1 = -0.3*VOH_AC
6 VT2 = -0.7*VOH_AC
7 tLZBeginPoint = [(T2 - T1) / (VT2 - VT1)] * [(VTT - VT2) + T2]

- Supported Test Mode: DDR4 (tLZ(DQS_c) Test)

  Refer to Figure 87 of the JESD79-4D document for tLZ(DQS_c) and tHZ(DQS_t) method for calculating transitions and begin points.

  Steps:

  i Vsw1 = 0.66 * VDD

  ii Vsw2 = 0.74 * VDDQ

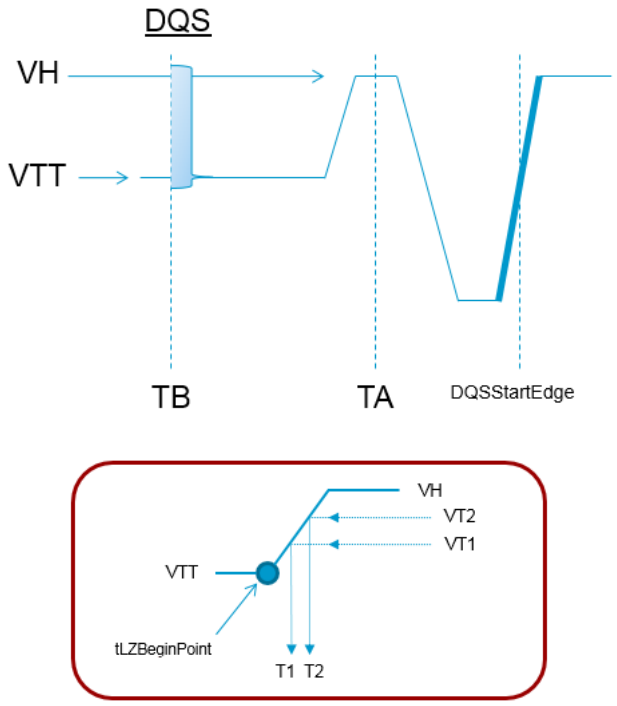
  iii On the first falling edge on the preamble region, find Tsw1 and Tsw2

  iv tLZBeginPoint = ((Tsw1 - Tsw2) / (Vsw1 - Vsw2)) * (VDDQ - Vsw1) + Tsw1;

  The measurement is made on DQS_C.

Finding tLZBeginPoint(DQS) for WRITE data burst

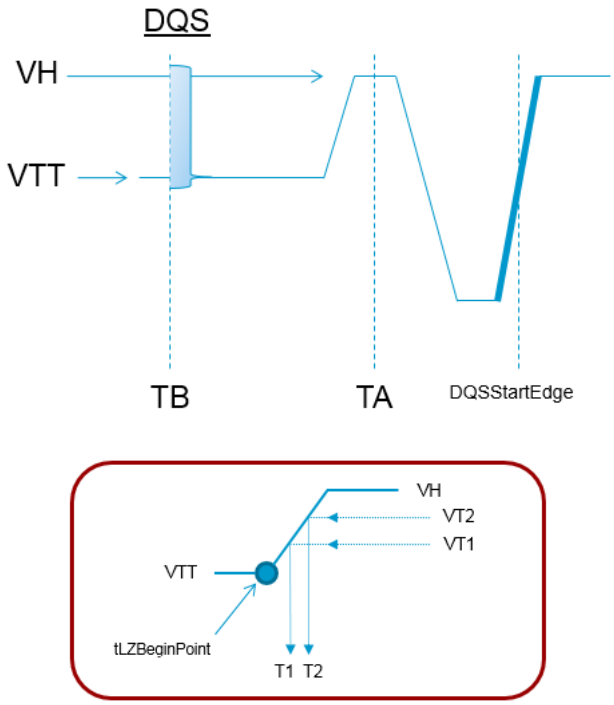
- Supported Test Mode: DDR4 (tWPRE Test)



Steps:

1 TA = DQSStartEdge – 1.5UI
2 TB = DQSStartEdge – 3.0UI
3 Form a histogram(vert) bounded by TA & TB
4 VTT = Histogram Min
5 VT1 = 0.1 * VIHDiff_DQS
6 VT2 = 0.9 * VIHDiff_DQS
7 tLZBeginPoint = [(T2 - T1) / (VT2 - VT1)] * [(VTT - VT2) + T2]

- Supported Test Mode: LPDDR4 (tWPRE Test)

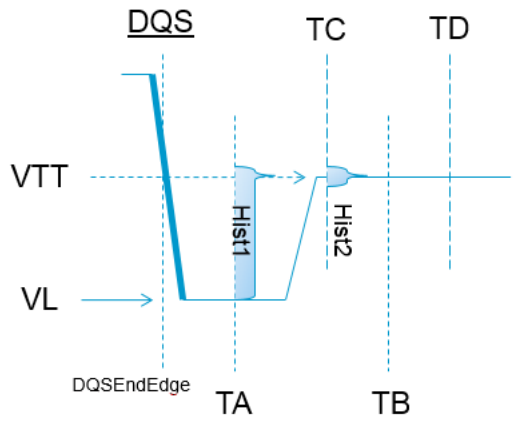


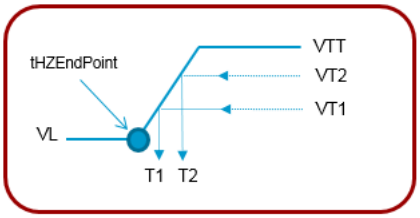
Steps:

1 TA = DQSStartEdge – 1.5UI
2 TB = DQSStartEdge – 3.0UI
3 Form a histogram(vert) bounded by TA & TB
4 VTT = Histogram Min
5 VT1 = 0.3*VIHL_AC
6 VT2 = 0.7*VIHL_AC
7 tLZBeginPoint = [(T2 - T1) / (VT2 - VT1)] * [(VTT - VT2) + T2]

Finding tHZEndPoint(DQS) for READ / WRITE data burst

- Supported Test Mode: DDR4 (tRPST Test)

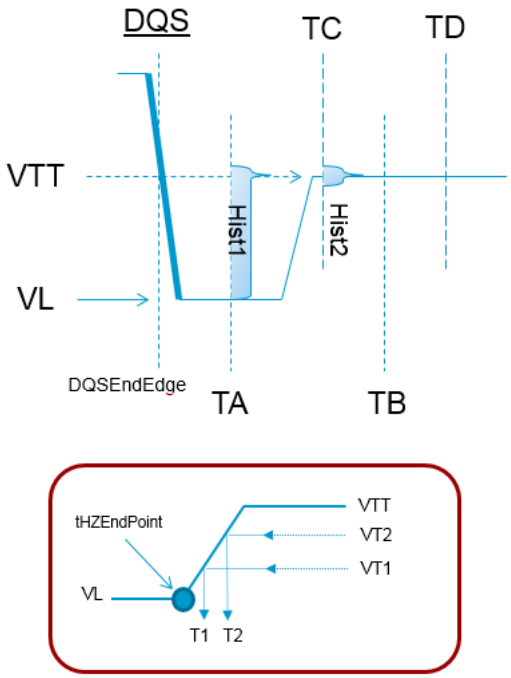




Steps:

1 TA = DQSEndEdge + 0.5 UI
2 TB = DQSEndEdge + 1.5 UI
3 Form a histogram(vert) bounded by TA & TB
4 VL = Histogram Min
5 VT1 = -0.34 * VDDQ
6 VT2 = -0.26 * VDDQ
7 tHZEndPoint = [(T2 - T1) / (VT2 - VT1)] * [(VL - VT2)] + T2

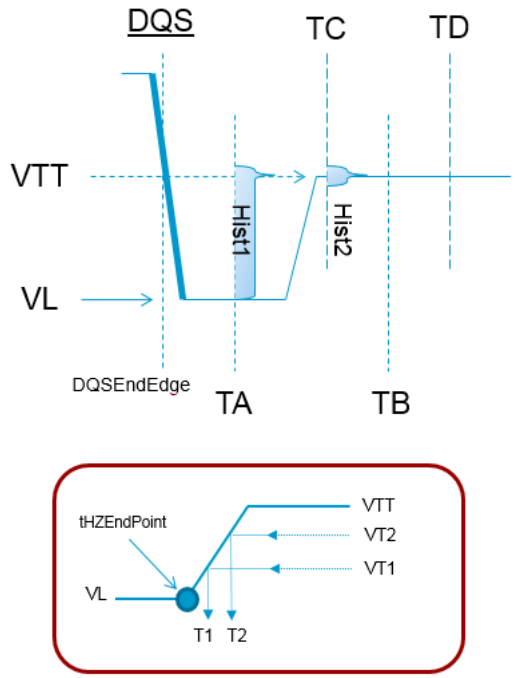
- Supported Test Mode: LPDDR4 (tRPST Test)



Steps:

1 TA = DQSEndEdge + 0.5 UI
2 TB = DQSEndEdge + 1.0 UI
3 Form a histogram(vert) bounded by TA & TB
4 VL = Histogram Min
5 VT1 = -0.7 * VOH_AC
6 VT2 = -0.3 * VOH_AC
7 tHZEndPoint = [(T2 - T1) / (VT2 - VT1)] * [(VL - VT2)] + T2

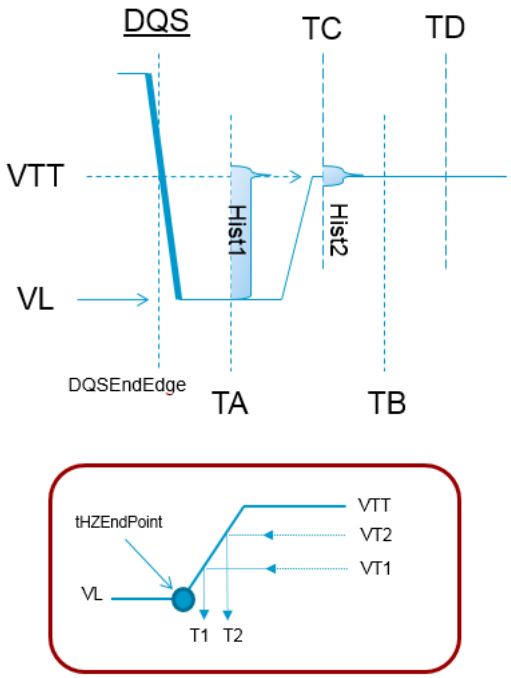
- Supported Test Mode: DDR4 (tWPST Test)



Steps:

1 TA = DQSEndEdge + 0.5 UI
2 TB = DQSEndEdge + 1.5 UI
3 Form a histogram(vert) bounded by TA & TB
4 VL = Histogram Min
5 VT1 = 0.9 * VILDiff_DQS
6 VT2 = 0.1 * VILDiff_DQS
7 tHZEndPoint = [(T2 - T1) / (VT2 - VT1)] * [(VL - VT2)] + T2

- Supported Test Mode: LPDDR4 (tWPST Test)



Steps:

1 TA = DQSEndEdge + 0.5 UI
2 TB = DQSEndEdge + 1.0 UI
3 Form a histogram(vert) bounded by TA & TB
4 VL = Histogram Min
5 VT1 = -0.7*VIHL_AC
6 VT2 = -0.3*VIHL_AC
7 tHZEndPoint = [(T2 - T1) / (VT2 - VT1)] * [(VL - VT2)] + T2

- Supported Test Mode: DDR4 (tHZ(DQS_t) Test)

  Refer to Figure 87 of the JESD79-4D document for tLZ(DQS_c) and tHZ(DQS_t) method for calculating transitions and begin points.

  Steps:

  i Vsw1 = 0.66 * VDD

  ii Vsw2 = 0.74 * VDDQ

  iii VL = 0.4 * VDDQ

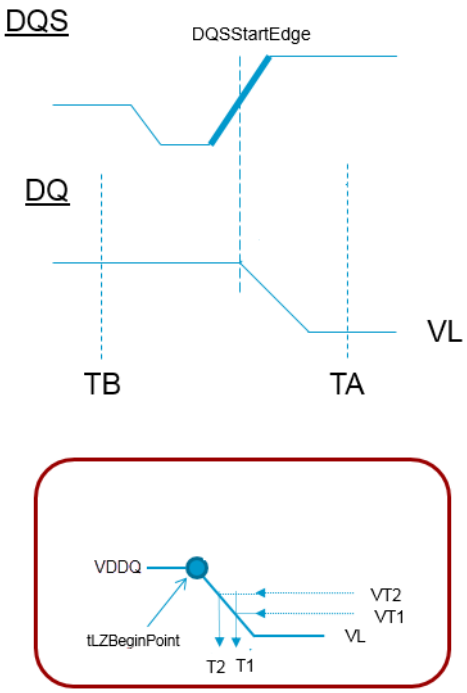
  iv On the last rising edge of the burst, find Tsw1 and Tsw2

  v tHZEndPoint = ((Tsw2 - Tsw1) / (Vsw2 - Vswl)) * (VL - Vsw2) + Tsw2;

  The measurement is made on DQS_t.

Finding tLZBeginPoint(DQ) for READ/WRITE data burst

- Supported Test Mode: DDR4 (tLZDQ Test)



Steps:

1 TA = DQSStartEdge + 0.5UI

2 TB = DQSStartEdge – 1.0UI

3 Find VTA, which is the Voltage of DQ at TA

4 If VTA < Vref,

a VT1 = 0.66 * VDDQ

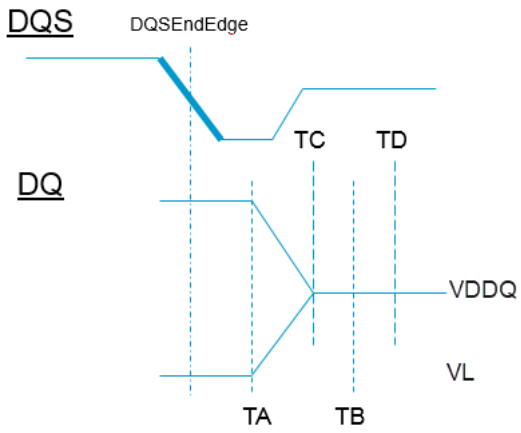
b VT2 = 0.74 * VDDQ

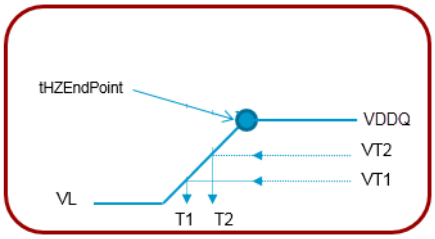
c tLZBeginPoint = [(T2 - T1) / (VT2 - VT1)] * [(VDDQ - VT2) + T2]

The VTA < Vref check ensures that the first bit is falling. If this condition cannot be satisfied, tLZ DQ test cannot be performed and might yield an invalid measurement.

Find tHZEndPoint(DQ) for READ/WRITE data burst

- Supported Test Mode: DDR4 (tHZDQ Test)





Steps:

1 TA = DQSEndEdge + 0.5UI

2 TB = DQSEndEdge + 1.5UI

3 Find VTA, which is the Voltage of DQ at TA

4 If VTA < Vref, (check falling edge)

d VL = 0.4 * VDDQ

e VT1 = 0.66 * VDDQ

f VT2 = 0.74 * VDDQ

5 tHZEndPoint = [(T2 - T1) / (VT2 - VT1)] * [(VL - VT2) + T2]

The VTA < Vref check ensures that the last bit is rising. If this condition cannot be satisfied, tHZ DQ test cannot be performed and might yield an invalid measurement.

Timing tests (WRITE cycle tests)

Data Strobe Timing

tDQSS

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

30106 [tDQSS]

30127 [tDQSS2]

NOTE For SDRAM type DDR4, the tDQSS2 test appears under the Select Tests tab only when you set the Write Preamble Mode as 2tCK under the Set Up tab of the Test Application.

LPDDR4 Test Mode

50106 [tDQSS]

LPDDR4X (Differential) Test Mode

60106 [tDQSS]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tDQSS [DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)] tDQSS2 [DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	4.11.2	Table 99	tDQSS [Write command to first DQS latching]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the time interval from the data strobe output (DQS rising edge) access time to the associated clock (crossing point).

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the time interval from the first latch of the data strobe output (first DQS latching edge) access time to the associated clock (crossing point).

Test Procedure: **DDR4 (for Test ID 30106 and 30127)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQS crossings in the specified burst.

4 For all DQS crossings found, locate the nearest crossing at the rising edge of the Clock.

5 Measure the time difference from the DQS crossing to the Clock crossing (found in the previous step) as tDQSS.

6 Determine the worst result from the set of tDQSS measured.

LPDDR4 (for Test ID 50106) / LPDDR4X (Differential) (for Test ID 60106)

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Identify the crossing on the rising edge of the DQS signal, which is nearest to the first DQ crossing within the burst found in the previous step.
The identified DQS crossing is considered as the first latch DQS crossing.

4 Prior to the first latch DQS crossing, locate the nearest crossing on the rising edge of the Clock.

5 If the time difference between the Clock crossing (found in the previous step) and the first latch DQS crossing is more than 0.5 UI, consider that time difference as tDQSS.

However, if the calculated time difference is less than 0.5 UI, locate the crossing on the rising edge of the Clock, which is one cycle before the previously located Clock crossing.

6 Measure the time difference between the newly located Clock crossing and the first latch DQS crossing. This time difference is denoted as tDQSS.

7 Report the measured tDQSS.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of tDQSS value for the test signal shall be within the conformance limits as per the JEDEC specification.

tDSS

Mode Supported: DDR4, LPDDR4, LPDDR4X (Both Differential and Single-Ended)

Test ID: **DDR4 Test Mode**

30109 [tDSS]

LPDDR4 Test Mode

50109 [tDSS]

LPDDR4X (Differential) Test Mode

60109 [tDSS]

LPDDR4X (Single-ended) Test Mode

70109 [tDSS]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tDSS [DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	4.11.2	Table 99	tDSS [DQS falling edge to CK setup time]

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC JC-42.6-1847.17, 28 November 2017	2.1.8	Table 6	tDSS [DQS falling edge to CK setup time]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the time interval from the falling edge of the data strobe (DQS falling edge) output access time to the clock (CLK rising edge) setup time.

LPDDR4 / LPDDR4X Test Modes

The purpose of this test is to verify the time interval from the falling edge of the data strobe (DQS falling edge) output access time to the clock (CLK falling edge) setup time.

Test Procedure: **DDR4 (for Test ID 30109)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid crossings on the falling edges of DQS in the specified burst.
4 For all crossings found on the falling edges of DQS, locate all the next nearest rising edges of the Clock.

5 Measure tDSS as the time between crossings on the falling edges of DQS and the rising edges of the Clock found in the previous step.

6 Collect all values of tDSS.

7 Report all values of tDSS measured.

LPDDR4 (for Test ID 50109) / LPDDR4X (for Test IDs 60109 and 70109)

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid crossings on the falling edges of DQS in the specified burst.

4 For all crossings found on the falling edges of DQS, locate all the next nearest falling edges of the Clock.

5 Measure tDSS as the time between crossings on the falling edges of DQS and the falling edges of the Clock found in the previous step.

6 Collect all values of tDSS.

7 Determine the worst result from the set of tDSS measured.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X Test Modes

The measured value of tDSS shall be within the conformance limits as per the JEDEC specification.

tDSH

Mode Supported: DDR4, LPDDR4, LPDDR4X (Both Differential and Single-Ended)

Test ID: **DDR4 Test Mode**

30110 [tDSH]

LPDDR4 Test Mode

50110 [tDSH]

LPDDR4X (Differential) Test Mode

60110 [tDSH]

LPDDR4X (Single-ended) Test Mode

70110 [tDSH]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tDSH [DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	4.11.2	Table 99	tDSH [DQS falling edge hold time from CK]

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC JC-42.6-1847.17, 28 November 2017	2.1.8	Table 6	tDSH [DQS falling edge hold time from CK]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X Test Modes**

The purpose of this test is to verify the time interval from the falling edge of the data strobe output hold time from clock.

Test Procedure: **DDR4 (for Test ID 30110) / LPDDR4 (for Test ID 50110) / LPDDR4X (for Test IDs 60110 and 70110)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid falling DQS crossings in the specified burst.
4 For all the falling DQS crossings found, locate all nearest preceding rising Clock edges.
5 Measure tDSH as the time between falling DQS crossings and the crossing point of the Clock rising edges found.
6 Collect all tDSH.
7 Determine the worst result from the set of tDSH measured.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X Test Modes

The measured value of tDSH shall be within the conformance limits as per the JEDEC specification.

tDQSH2PRE

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30124 [tDQSH2PRE]

NOTE For SDRAM type DDR4, the tDQSH2PRE test appears under the Select Tests tab only when you set the Write Preamble Mode as 2tCK under the Set Up tab of the Test Application.

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	4.25.4	Table 84	tDQSH2PRE [DQS_t, DQS_c differential input high pulse width at 2tCK Preamble]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the high level width of the Data Strobe signal at 2tCK Preamble.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 (for Test ID 30124)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find tLZBeginPoint(tWPPRE) on DQS signal of the said burst.
4 Find the first falling edge on preamble region on DQS of the found burst.
5 tDQSH2PRE is the time interval between the tLZBeginPoint and the found first falling edge on preamble region.
6 Report tDQSH2PRE.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of tDQSH2PRE shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

tDQSH

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

30107 [tDQSH]

LPDDR4 Test Mode

50107 [tDQSH]

LPDDR4X (Differential) Test Mode

60107 [tDQSH]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tDQSH [DQS_t, DQS_c differential input high pulse width]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	4.11.2	Table 99	tDQSH [DQS input high-level]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X Test Mode**

The purpose of this test is to verify the high level width of the Data Strobe signal.

Test Procedure: **DDR4 (for Test ID 30107) / LPDDR4 (for Test ID 50107) / LPDDR4X (Differential) (for Test ID 60107)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising and falling DQS crossings in the specified burst.
4 Measure tDQSH as the time starting from the rising edge of DQS and ending at the following falling edge.
5 Collect all tDQSH values.
6 Determine the worst result from the set of tDQSH measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of tDQSH shall be within the conformance limits as per the JEDEC specification.

tDQSL

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

30108 [tDQSL]

LPDDR4 Test Mode

50108 [tDQSL]

LPDDR4X (Differential) Test Mode

60108 [tDQSL]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tDQSL [DQS_t, DQS_c differential input low pulse width]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	4.11.2	Table 99	tDQSL [DQS input low-level width]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the low level width of the Data Strobe signal.

Test Procedure: **DDR4 (for Test ID 30108) / LPDDR4 (for Test ID 50108) / LPDDR4X (Differential) (for Test ID 50109)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising and falling DQS crossings in the specified burst.
4 Measure tDQSL as the time starting from the falling edge of DQS and ending at the following rising edge.
5 Collect all tDQSL values.
6 Determine the worst result from the set of tDQSL measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of tDQSL shall be within the conformance limits as per the JEDEC specification.

tWPRE

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

30111 [tWPRE]

LPDDR4 Test Mode

50111 [tWPRE]

LPDDR4X (Differential) Test Mode

60111 [tWPRE]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tWPRE [DQS_t, DQS_c differential WRITE Preamble]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	4.11.2	Table 99	tWPRE [Write Preamble]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the time when DQS starts driving a high (*preamble behavior) to the first DQS signal rising edge crossing for the write cycle. You may customize the limits for evaluation tests usage.

Test Procedure: **DDR4 (for Test ID 30111) / LPDDR4 (for Test ID 50111) / LPDDR4X (Differential) (for Test ID 60111)**

1 Acquire and split the Read and Write bursts of the acquired signal.
2 Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3 Take the first valid WRITE burst found.
4 Find tLZBeginPoint on DQS signal of the said burst.
5 Find the first rising edge (excluding preamble pattern) on DQS of the found burst.
6 tWPRE is the time interval between the rising DQS edge and tLZBeginPoint.
7 Report tWPRE.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of tWPRE for the test signal shall be within the conformance limits as per the JEDEC specification.

tWPRE2

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30122 [tWPRE2]

NOTE For SDRAM type DDR4, the tWPRE2 test appears under the Select Tests tab only when you set the Write Preamble Mode as 2tCK under the Set Up tab of the Test Application.

LPDDR4 / LPDDR4X Test Modes

Not available

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tWPRE2 [DQS_t, DQS_c differential WRITE Preamble (2 clock preamble)]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the time when DQS starts driving a high (*preamble behavior) to the first DQS signal rising edge crossing for the write cycle (for preamble mode 2tCK). You may customize the limits for evaluation tests usage. Refer to Figure 126 of the JESD79-4D document for the method for calculating tWPRE transitions and endpoints.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 (for Test ID 30122)**

1 Acquire and split the Read and Write bursts of the acquired signal.
2 Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3 Take the first valid WRITE burst found.
4 Find tLZBeginPoint on DQS signal of the said burst.
5 Find the first rising edge (excluding preamble pattern) on DQS of the found burst.
6 tWPRE2 is the time interval between the rising DQS edge and tLZBeginPoint.
7 Report tWPRE2.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of tWPRE2 for the test signal shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

tWPST

NOTE This test does not support WDQS mode because there is no reference available in the JEDEC specification to measure the tWPST in WDQS mode.

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID:

DDR4 Test Mode

30112 [tWPST]

LPDDR4 Test Mode

50112 [tWPST]

LPDDR4X (Differential) Test Mode

60112 [tWPST]

References:

DDR4 Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tWPST [DQS_t, DQS_c differential WRITE Postamble]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	4.11.2	Table 99	tWPST [0.5 tCK Write Postamble]

Test Overview:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Mode

The purpose of this test is to verify the time when DQS is no longer driving (from High/Low state to Hi-Impedance) from the last DQS signal crossing (last bit of the Write data burst) for Write Cycle. You may customize the limits for evaluation tests usage.

Test Procedure:

DDR4 (for Test ID 30112) / LPDDR4 (for Test ID 50112) / LPDDR4X (Differential) (for Test ID 60112)

1 Acquire and split the Read and Write burst of the acquired signal.
2 Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3 Take the first valid WRITE burst found.
4 Find tHZEndPoint of the said burst.
5 Find the last falling edge on DQS prior to the tHZEndPoint that was found in the previous step.
6 tWPST is the time interval between the falling DQS edge's crossing and tHZEndPoint.
7 Report tWPST.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of tWPST for the test signal shall be within the conformance limits as per the JEDEC specification.

tDVAC(Strobe)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30117 [tDVAC(Strobe)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the time of the strobe signal above VIHdiff(AC) and below VILdiff(AC).

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 30117)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising and falling DQS crossings on the VIHdiff(AC) and VILdiff(AC) levels in the specified burst.
4 Measure tDVAC(Strobe) as the time starting from a rising VIHdiff(AC) cross-point of the DQS and ending at the following falling VIHdiff(AC) cross-point of DQS.
5 Measure tDVAC(Strobe) as the time starting from a falling VILdiff(AC) cross-point of the DQS and ending at the following rising VILdiff(AC) cross-point of DQS.
6 Collect all tDVAC(Strobe).
7 Determine the worst result from the set of tDVAC(Strobe) measured.
8 Report the value of the worst tDVAC(Strobe).

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of tDVAC(Strobe) for the test signal is reported as “Information Only”.

LPDDR4 / LPDDR4X Test Modes

Not available.

Timing tests (READ cycle tests)

Data Timing

tDQSQ

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

30104 [tDQSQ]

LPDDR4 Test Mode

50104 [tDQSQ]

LPDDR4X (Differential) Test Mode

60104 [tDQSQ]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tDQSQ [DQS_t, DQS_c to DQ Skew, per group, per access]

LPDDR4 / LPDDR4X (Differential) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.5	Table 221	tDQSQ [DQS_t, DQS_c to DQ Skew total, per group, per access (DBI Disabled)]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the time interval from the data strobe output (DQS rising and falling edges) access time to the associated data (DQ rising and falling) signal.

Test Procedure: **DDR4 (for Test ID 30104)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQ crossings at V_{TT} level in the specified burst.
4 For all DQ crossings found, locate the nearest DQS crossings (Rising or Falling).
5 Measure tDQSQ as the time difference from the DQ crossing to the DQS crossing.
6 Determine the worst result from the set of tDQSQ measured.

LPDDR4 (for Test ID 50104) / LPDDR4X (Differential) (for Test ID 60104)

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQ crossings at V_{ref} level in the specified burst.
4 For all DQ crossings found, locate the nearest DQS crossings (Rising or Falling).
5 Measure tDQSQ as the time difference from the DQ crossing to the DQS crossing.
6 Determine the worst result from the set of tDQSQ measured.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of tDQSQ shall be within the conformance limits as per the JEDEC specification.

tQH

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

30105 [tQH]

LPDDR4 Test Mode

50105 [tQH]

LPDDR4X (Differential) Test Mode

60105 [tQH]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tQH [DQ output hold time from DQS_t, DQS_c]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.5	Table 221	tQH [DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the time interval from the data output hold time (DQ rising and falling edges) to DQS (rising/falling edges).

Test Procedure: **DDR4 (for Test ID 30105) / LPDDR4 (for Test ID 50105) / LPDDR4X (Differential) (for Test ID 60105)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQ crossings at Vref level in the specified burst.
4 For all DQ crossings found, locate the nearest DQS crossings (Rising or Falling).
5 Locate the DQS crossing that occurs before the DQS crossings found in the previous step.
6 Measure tQH as the time difference from the DQ crossing to the DQS crossing (found in the previous step).
7 Determine the worst result from the set of tQH measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of tQH shall be within the conformance limits as per the JEDEC specification.

tDQSQ_DBI

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

30119 [tDQSQ_DBI]

LPDDR4 Test Mode

30501 [tDQSQ_DBI]

LPDDR4X (Differential) Test Mode

60501 [tDQSQ_DBI]

References: **DDR4 Test Mode**

There is no reference available for this test in the JEDEC specifications. The measurement result is reported as “Information Only”.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.5	Table 221	tDQSQ_DBI [DQS_t, DQS_c to DQ Skew total, per group, per access (DBI enabled)]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the time interval from the data strobe output (DQS rising and falling edges) access time to the associated data (DQ rising and falling) signal while DBI mode is enabled.

Test Procedure: **DDR4 (for Test ID 30119)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQ crossings at V_{TT} level in the specified burst.
4 For all DQ crossings found, locate the nearest DQS crossings (Rising or Falling).
5 Measure tDQSQ_DBI as the time difference from the DQ crossing to the DQS crossing.
6 Determine the worst result from the set of tDQSQ_DBI measured.

LPDDR4 (for Test ID 30501) / LPDDR4X (Differential) (for Test ID 60501)

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQ crossings at Vref level in the specified burst.
4 For all DQ crossings found, locate the nearest DQS crossings (Rising or Falling).
5 Measure tDQSQ_DBI as the time difference from the DQ crossing to the DQS crossing.
6 Determine the worst result from the set of tDQSQ_DBI measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of tDQSQ_DBI shall be within the conformance limits as per the JEDEC specification.

tQH_DBI

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

30120 [tQH_DBI]

LPDDR4 Test Mode

30502 [tQH_DBI]

LPDDR4X (Differential) Test Mode

60502 [tQH_DBI]

References: **DDR4 Test Mode**

There is no reference available for this test in the JEDEC specifications. The measurement result is reported as “Information Only”.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.5	Table 221	tQH_DBI [DQ output hold time from DQS_t, DQS_c (DBI enabled)]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the time interval from the data output hold time (DQ rising and falling edges) to the associated data strobe (DQS rising and falling edge) signal while DBI mode is enabled.

Test Procedure: **DDR4 (for Test ID 30120) / LPDDR4 (for Test ID 30502) / LPDDR4X (Differential) (for Test ID 60502)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQ crossings at Vref level in the specified burst.
4 For all DQ crossings found, locate the nearest DQS crossing (Rising or Falling).
5 Locate the DQS crossing that occurs before the DQS crossings found in the previous step.
6 Measure tQH_DBI as the time difference from the DQ crossing to the DQS crossing (found in the previous step).
7 Determine the worst result from the set of tQH_DBI measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of tQH_DBI shall be within the conformance limits as per the JEDEC specification.

tLZDQ

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30102 [tLZDQ]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tLZ(DQ) [DQ low impedance time from CK_t, CK_c]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the time when DQ starts driving (*from High-impedance state to High/Low state) to the clock signal crossing. You may customize the limits for evaluation tests usage.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (30102)**

1 Acquire and split Read and Write burst of the acquired signal.
2 Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3 Take the first valid READ burst found.
4 Find tLZBeginPoint on the DQ signal of the said burst.
5 Find the nearest Clock rising edge.
6 tLZ(DQ) is the time interval between the clock rising edge's crossing point and tLZBeginPoint.
7 Report tLZ(DQ).

NOTE In order to differentiate between the Hi-Z and the Lo-Z regions, a voltage transition must occur. The automated Test Application expects this DQ transition to take place at the associated first valid DQS edge (within the range from 1.0UI prior to the edge and 0.5UI after the edge). This transition in DQ signal at the first valid DQS edge is required to correctly identify the tLZBeginPoint on DQ signal.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of tLZ(DQ) for the test signal shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

tHZDQ

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30101 [tHZDQ]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tHZ(DQ) [DQ high impedance time from CK_t, CK_c]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the time when DQ no longer is driving (*from High state OR Low state to the High-impedance state) to the clock signal crossing. You may customize the limits for evaluation tests usage.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for 30101)**

1 Acquire and split read and write burst of the acquired signal.
2 Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3 Take the first valid READ burst found.
4 Find tLZBeginPoint on the DQ signal of the specified burst.
5 Find the nearest Clock rising edge.
6 tHZ(DQ) is the time interval between the Clock rising edge's crossing point to tHZEndPoint.
7 Report tHZ(DQ).

NOTE In order to differentiate between the Hi-Z and the Lo-Z regions, a voltage transition must occur. The automated Test Application expects this DQ transition to take place at the associated last valid DQS edge (within the range from 0.5UI to 1.5UI after the edge). This transition in DQ signal at the last valid DQS edge is required to correctly identify the tHZBeginPoint on DQ signal.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of tHZ(DQ) for the test signal shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

tDVWp

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30123 [tDVWp]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tDVWp [DQ input pulse width]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the minimum input pulse width of DQ on Read Burst.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for 30101)**

1 Acquire and identify the READ and WRITE burst data of the acquired signal.
2 Use all valid READ bursts that are found to perform tDVWp measurement.
3 Find all valid rising and falling DQ edges, which are defined as the crossings at VTT in the READ data burst.
4 Measure tDVWp as the time starting from a rising/falling edge of the DQ to the time ending at the following falling/rising edge.
5 Process all valid edges in the READ data burst.
6 Collect all values of tDVWp.
7 Determine the worst result from the set of tDVWp values measured and report it as the final test result.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of tDVWp for the test signal shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

Data Strobe Timing

tDQSCK

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

30021 [tDQSCK]

LPDDR4 Test Mode

50021 [tDQSCK]

LPDDR4X (Differential) Test Mode

60021 [tDQSCK]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tDQSCK [DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	4.8	Table 95	tDQSCK [DQS Output Access time from CK_t/CK_c]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the time interval from the data strobe output (DQS rising edge) access time to the nearest rising edge of the clock.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the time interval from the data strobe output (DQS) first rising edge to the rising edge of the clock, that is the tDQSCK delay (cycle) before the nearest rising edge of the Clock (the clock edge that is nearest to the first rising edge of DQS).

Test Procedure: **DDR4 Test Mode (for Test ID 30021)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising DQS crossings at 0V in the specified burst.
4 For all DQS crossings found, locate the nearest crossing at the rising edge of the Clock at 0V.
5 Measure as tDQSCK the time difference from the DQS crossing to the corresponding Clock crossing (found in the previous step).
6 Report the measured tDQSCK.

LPDDR4 (for Test ID 50021) / LPDDR4X (Differential) (for Test ID 60021)

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all the mid-cross points for DQS at 0V in the specified burst.

4 Find all the mid-cross points for Clock at 0V in the specified burst.

5 Locate the first crossing of the DQS rising edge in the burst. Consider this point (that is, first rising edge of DQS) as tDQSCK strobe point.

6 Find the “closest Clock - DQS”, which is the crossing of the Clock rising edge that is closest to the first crossing of the DQS rising edge.

7 Find tDQSCK clock point, which is the mid-cross point of the Clock before “closest Clock - DQS” at the tDQSCK Delay (cycle). By default, tDQSCK Delay has three cycles.

   For example, when tDQSCK Delay = 3, the tDQSCK clock point is the mid-cross point of the Clock, which is three clocks before “closest Clock - DQS”. Similarly, when tDQSCK Delay = 5, the tDQSCK clock point is the mid-cross point of the Clock, which is five clocks before “closest Clock - DQS”. You may configure tDQSCK Delay in the Configure tab of the Compliance Test Application.

8 Compare the tDQSCK strobe point to the tDQSCK clock point as a test result.

   Mathematically, test result = tDQSCK strobe point - tDQSCK clock point.

9 Display the test result by spotting the measurement location on the waveform and locate the marker to tDQSCK strobe point and tDQSCK clock point.

10 Compare the test results with the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of tDQSCK shall be within the conformance limits as per the JEDEC specification.

tQSH

Mode Supported: DDR4, LPDDR4, LPDDR4X (Both Differential and Single-Ended)

Test ID: **DDR4 Test Mode**

30115 [tQSH]

LPDDR4 Test Mode

50115 [tQSH]

LPDDR4X (Differential) Test Mode

60115 [tQSH]

LPDDR4X (Single-ended) Test Mode

70115 [tQSH]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tQSH [DQS_t, DQS_c differential output high time]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.5	Table 221	tQSH [DQS, DQS# differential output high time (DBI-disabled)]

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC JC-42.6-1847.17, 28 November 2017	2.1.8	Table 6	tQSH [DQS, DQS# Single-ended output high time (DBI-disabled)]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X Test Modes**

The purpose of this test is to verify the width of the high level of the Data Strobe signal.

Test Procedure: **DDR4 (for Test ID 30115) / LPDDR4 (for Test ID 50115) / LPDDR4X (for Test IDs 60115 and 70115)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQS crossings in the specified burst.
4 Measure tQSH as the time starting from a rising edge of the DQS and ending at the following falling edge.
5 Collect all tQSH.
6 Determine the worst result from the set of tQSH measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X Test Modes**

The measured value of tQSH shall be within the conformance limits as per the JEDEC specification.

tQSL

Mode Supported: DDR4, LPDDR4, LPDDR4X (Both Differential and Single-Ended)

Test ID: **DDR4 Test Mode**

30116 [tQSL]

LPDDR4 Test Mode

50116 [tQSL]

LPDDR4X (Differential) Test Mode

60116 [tQSL]

LPDDR4X (Single-ended) Test Mode

70116 [tQSL]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tQSL [DQS_t, DQS_c differential output low time]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.5	Table 221	tQSL [DQS, DQS# differential output low time (DBI-disabled)]

LPDDR4X (Single-ended) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC JC-42.6-1847.17, 28 November 2017	2.1.8	Table 6	tQSL [DQS Single-ended output low time (DBI-disabled)]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X Test Modes**

The purpose of this test is to verify the width of the low level of the Data Strobe signal.

Test Procedure: **DDR4 (for Test ID 30116) / LPDDR4 (for Test ID 50116) / LPDDR4X (for Test IDs 60116 and 70116)**

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQS crossings in the specified burst.
4 Measure tQSL as the time starting from a falling edge of the DQS and ending at the following rising edge.
5 Collect all tQSL.
6 Determine the worst result from the set of tQSL measured.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X Test Mode**

The measured value of tQSL shall be within the conformance limits as per the JEDEC specification.

tQSH_DBI

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

30503 [tQSH_DBI]

LPDDR4X (Differential) Test Mode

60503 [tQSH_DBI]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.5	Table 221	tQSH_DBI [DQS, DQS# differential output high time (DBI-enabled)]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the width of the high level of the Data Strobe signal while DBI mode is enabled.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 30503) / LPDDR4X (Differential) (for Test ID 60503)

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQS crossings in the specified burst.
4 Measure tQSH_DBI as the time starting from a rising edge of the DQS and ending at the following falling edge.
5 Collect all tQSH_DBI.
6 Determine the worst result from the set of tQSH_DBI measured.

Expected/ Observable Results: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of tQSH_DBI shall be within the conformance limits as per the JEDEC specification.

tQSL_DBI

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

30504 [tQSL_DBI]

LPDDR4X (Differential) Test Mode

60504 [tQSL_DBI]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.5	Table 221	tQSL_DBI [DQS, DQS# differential output low time (DBI-enabled)]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the width of the low level of the Data Strobe signal while DBI mode is enabled.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 30504) / LPDDR4X (Differential) (for Test ID 60504)

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQS crossings in the specified burst.
4 Measure tQSL_DBI as the time starting from a falling edge of the DQS and ending at the following rising edge.
5 Collect all tQSL_DBI.
6 Determine the worst result from the set of tQSL_DBI measured.

Expected/ Observable Results: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of tQSL_DBI shall be within the conformance limits as per the JEDEC specification.

tRPRE

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

30113 [tRPRE]

LPDDR4 Test Mode

50113 [tRPRE]

LPDDR4X (Differential) Test Mode

60113 [tRPRE]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tRPRE [DQS_t, DQS_c Differential READ Preamble]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	4.7.5	Table 94	tRPRE [READ Preamble]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the time when DQS starts driving low (*preamble behavior) to the first DQS signal crossing for the Read Cycle. You may customize the limits for evaluation tests usage.

Test Procedure: **DDR4 (for Test ID 30113) / LPDDR4 (for Test ID 50113) / LPDDR4X (Differential) (for Test ID 60113)**

1 Acquire and split read and write burst of the acquired signal.
2 Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3 Take the first valid READ burst found.
4 Find tLZBeginPoint on the DQS signal of the specified burst.
5 Find the first rising edge (excluding preamble pattern) on DQS of the found burst. tRPRE is the time interval between the rising DQS edge and tLZBeginPoint.
6 Report tRPRE.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of tRPRE shall be within the conformance limits as per the JEDEC specification.

tRPRE2

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30121 [tRPRE2]

NOTE For SDRAM type DDR4, the tRPRE2 test appears under the Select Tests tab only when you set the Read Preamble Mode as 2tCK under the Set Up tab of the Test Application.

LPDDR4 / LPDDR4X Test Modes

Not available

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tRPRE2 [DQS_t, DQS_c differential READ Preamble (2 clock preamble)]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the time when DQS starts driving low (*preamble behavior) to the first DQS signal crossing for the Read Cycle (for preamble mode 2tCK). You may customize the limits for evaluation tests usage. Refer to Figure 88 of the JESD79-4D document for the method for calculating tRPRE transitions and endpoints.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 (for Test ID 30121)**

1 Acquire and split read and write burst of the acquired signal.
2 Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3 Take the first valid READ burst found.
4 Find tLZBeginPoint on the DQS signal of the specified burst.
5 Find the first rising edge (excluding preamble pattern) on DQS of the found burst. tRPRE2 is the time interval between the rising DQS edge and tLZBeginPoint.
6 Report tRPRE2.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of tRPRE2 shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

tRPST

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

30114 [tRPST]

LPDDR4 Test Mode

50114 [tRPST]

LPDDR4X (Differential) Test Mode

60114 [tRPST]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tRPST [DQS_t, DQS_c Differential READ Postamble]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	4.7.4	Table 94	tRPST [0.5 tCK READ postamble]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the time when DQS is no longer driving (from High/Low state to Hi-Impedance) from the last DQS signal crossing (last bit of the Read data burst) for Read Cycle. You may customize the limits for evaluation tests usage.

Test Procedure: **DDR4 (for Test ID 30114) / LPDDR4 (for Test ID 50114) / LPDDR4X (Differential) (for Test ID 60114)**

1 Acquire and split the Read and Write burst of the acquired signal.
2 Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3 Take the first valid READ burst found.
4 Find tHZBeginPoint on the DQS signal of the specified burst.
5 Find the last falling edge on DQS prior to tHZEndPoint found.
tRPST is the time interval between the falling DQS edge's crossing and tHZEndPoint.
6 Report tRPST.

Expected/ Observable Results: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The measured value of tRPST shall be within the conformance limits as per the JEDEC specification.

tLZ(DQS_c)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30125 [tLZ(DQS_c)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tLZ(DQS) [DQS_t and DQS_c low-impedance time]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the time when DQS starts driving (*from High-impedance state to High/Low state) to the nearest rising clock signal crossing. You may customize the limits for evaluation tests usage.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (30125)**

1 Acquire and split Read and Write burst of the acquired signal.
2 Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3 Take the first valid READ burst found.
4 Find tLZBeginPoint on the DQS signal of the said burst.
5 Find the nearest Clock rising edge.
tLZ(DQS_c) is the time interval between the Clock rising edge's crossing point and tLZBeginPoint.
6 Report tLZ(DQS_c).

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The value of measured tLZ(DQS_c) shall be within the conformance limits as specified in the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

tHZ(DQS_t)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30126 [tHZ(DQS_t)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tHZ(DQS) [DQS_t and DQS_c high-impedance time]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the time when DQS is no longer driving (from High state OR Low state to the High-impedance state) to the reference clock signal crossing. You may customize the limits for evaluation tests usage.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 30126)**

1 Acquire and split read and write burst of the acquired signal.
2 Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3 Take the first valid READ burst found.
4 Find tHZEndPoint on the DQS signal of the said burst.
5 Find the nearest Clock rising edge.
tHZ(DQS_t) is the time interval between Clock rising edge's crossing point and tHZEndPoint.
6 Report tHZ(DQS_t).

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The value of measured tHZ(DQS_t) shall be within the conformance limits as specified in the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

tDVAC(Clock)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30022 [tDVAC(Clock)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

NOTE This test is regarded as “Information Only” because the test limits defined in the specification are not fully defined.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the time of the clock signal above VIHdiff(AC) and below VILdiff(AC).

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 30022)**

1 Pre-condition the oscilloscope.
2 Trigger on the rising edge of the Clock signal under test.
3 Find all crossings on the rising/falling edge of the signal under test that cross VILdiff(AC).
4 Find all crossings on the rising/falling edge of the signal under test that cross VIHdiff(AC).
5 Measure tDVAC(Clock) as the time starting from a rising VIHdiff(AC) cross-point of the DQS and ending at the following falling VIHdiff(AC) cross-point of DQS.
6 Measure tDVAC(Strobe) as the time starting from a falling VILdiff(AC) cross-point of the DQS and ending at the following rising VILdiff(AC) cross-point of DQS.
7 Collect all tDVAC(Clock).
8 Determine the worst result from the set of tDVAC(Clock) measured.
9 Report the value of the worst tDVAC(Clock).

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of tDVAC(Clock) for the test signal is reported as “Information Only”.

LPDDR4 / LPDDR4X Test Modes

Not available.

Timing tests (Clock Timing)

Rising Edge Measurements

tCK(abs) Rising Edge Measurements

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

2 [tCK(abs) Rising Edge Measurements]

LPDDR4 Test Mode

50002 [tCK(abs) Rising Edge Measurements]

LPDDR4X (Differential) Test Mode

60002 [tCK(abs) Rising Edge Measurements]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.3.1	-	tCK(abs) [Absolute Clock Period]

NOTE The measurement result is reported as “Information Only” because the JEDEC specification does not have properly defined test limits.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.1.2	-	-

NOTE This test is regarded as “Information Only” because this parameter is not subject to production tests as mentioned in section 10.1.2 of the JEDEC specification.

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

tCK(abs) is the absolute clock period within a waveform window. The tCK(abs) Rising Edge Measurement measures the period from the rising edge of a cycle to the next rising edge within the waveform window.

Test Procedure: **DDR4 (for Test ID 2) / LPDDR4 (for Test ID 50002) / LPDDR4X (Differential) (for Test ID 60002)**

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

1 Find the maximum period value for period 1-202.
2 Find the minimum period value for period 1-202.
3 Check the two results for the worst case values.
4 Compare the worst case values to the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of tCK(abs) for the test signal is reported as “Information Only”.

tjit(CC) Rising Edge Measurements

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

100 [tjit(CC) Rising Edge Measurements]

LPDDR4 Test Mode

50100 [tjit(CC) Rising Edge Measurements]

LPDDR4X (Differential) Test Mode

60100 [tjit(CC) Rising Edge Measurements]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tJIT(CC)_total [Cycle to Cycle Period Jitter]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.1.6	-	-

NOTE This test is regarded as “Information Only” because this parameter is not subject to production tests as mentioned in section 10.1.6 of the JEDEC specification.

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to measure the difference in the clock period between two consecutive clock cycles. The tJIT(cc) Rising Edge Measurement measures the clock period from the rising edge of a clock cycle to the next rising edge.

Test Procedure: **DDR4 (for Test ID 100) / LPDDR4 (for Test ID 50100) / LPDDR4X (Differential) (for Test ID 60100)**

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

1 Measure the difference between every adjacent pair of periods.
2 Generate a total of 201 measurement results.
3 Check the results for the smallest and largest values, which are recorded as the worst case values.
4 Compare the worst case values to the compliance test limits.

Expected/ Observable Results: **DDR4 Test Mode**

The measured value of tJIT(cc) shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of tJIT(cc) for the test signal is reported as “Information Only”.

tCK(avg) Rising Edge Measurements

Mode Supported: DDR4, LPDDR4, LPDDR4X (Both Differential and Single-Ended)

Test ID: **DDR4 Test Mode**

200 [tCK(avg) Rising Edge Measurements]

LPDDR4 Test Mode

50200 [tCK(avg) Rising Edge Measurements]

LPDDR4X (Differential) Test Mode

60200 [tCK(avg) Rising Edge Measurements]

LPDDR4X (Single-ended) Test Mode

70200 [tCK(avg) Rising Edge Measurements]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tCK(avg) [Average Clock Period]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.2	Table 218	tCK(avg) [Average Clock Period]

LPDDR4X (Single-ended) Test Mode

There is no reference available for this test in the specification document. The measurement result is reported as “Information Only”.

Test Overview: **DDR4 / LPDDR4 / LPDDR4X Test Modes**

tCK(avg) is the average clock period within a 200 consecutive cycle window. The tCK(avg) Rising Edge Measurement measures the period from the rising edge of a cycle to the next rising edge within the waveform window.

Test Procedure: **DDR4 (for Test ID 200) / LPDDR4 (for Test ID 50200) / LPDDR4X (for Test IDs 60200 and 70200)**

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

1 Measure a sliding “window” of 200 cycles.
2 Calculate the average period value for periods 1-200.
3 Calculate the average period value for periods 2-201.
4 Calculate the average period value for periods 3-202.
Three measurement results are generated after step 4 is complete.
5 Check the three measured results for the smallest and largest values, which are recorded as the worst case values.
6 Compare the worst case values to the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of tCK(avg) shall be within the conformance limits as per the JEDEC specification.

LPDDR4X (Single-ended) Test Mode

The measured value of tCK(avg) is reported as “Information Only”.

tjit(per) Rising Edge Measurements

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

300 [tjit(per) Rising Edge Measurements]

LPDDR4 Test Mode

50300 [tjit(per) Rising Edge Measurements]

LPDDR4X (Differential) Test Mode

60300 [tjit(per) Rising Edge Measurements]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tJIT(per)_tot [Clock Period Jitter - total]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.1.5	-	-

NOTE This test is regarded as “Information Only” because this parameter is not subject to production tests as mentioned in section 10.1.5 of the JEDEC specification.

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock.

Test Procedure: **DDR4 (for Test ID 300) / LPDDR4 (for test ID 50300) / LPDDR4X (Differential) (for test ID 60300)**

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

1 Measure the difference between every period inside a 200 cycle window with the average of the whole window.
2 Calculate the average for periods 1 to 200.
3 Measure the difference between period #1, period #2 and so on up to period #200; with the average and save the resulting value as a measurement result.
A total of 200 measurement results are generated.
4 For the next set of measurement values, slide the window by one period and the application measures the average of period #2 up to period #201.
5 Compare period #2 with the new average.
Continue the comparison for period #3, #4 and so on up to period #201.
A total of 200 additional measurement results are generated such that there are 400 measured values overall.

6 For the next set of measurement values, slide the window by one more period and the application measures the average of period #3 up to period #202.

7 Compare period #3 with the new average.
Continue the comparison for period #4, #5 and so on up to period #202.
A total of 200 additional measurement results are generated such that there are 600 measured values overall.

8 Check the 600 results for the smallest and largest values, which are recorded as the worst case values.

9 Compare the worst case values to the compliance test limits.

Expected/ Observable Results:

DDR4 Test Mode

The measured value of tJIT(per) shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of tJIT(per) for the test signal is reported as “Information Only”.

tERR(nper) Rising Edge Measurements

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: 400 [tERR(2per) Rising Edge Measurements]

500 [tERR(3per) Rising Edge Measurements]

600 [tERR(4per) Rising Edge Measurements]

700 [tERR(5per) Rising Edge Measurements]

800 [tERR(6per) Rising Edge Measurements]

900 [tERR(7per) Rising Edge Measurements]

1000 [tERR(8per) Rising Edge Measurements]

1100 [tERR(9per) Rising Edge Measurements]

1200 [tERR(10per) Rising Edge Measurements]

1300 [tERR(11per) Rising Edge Measurements]

1400 [tERR(12per) Rising Edge Measurements]

1500 [tERR(13per) Rising Edge Measurements]

1600 [tERR(14per) Rising Edge Measurements]

1700 [tERR(15per) Rising Edge Measurements]

1800 [tERR(16per) Rising Edge Measurements]

1900 [tERR(17per) Rising Edge Measurements]

1901 [tERR(18per) Rising Edge Measurements]

3000 [tERR(nper) Rising Edge Measurements]

LPDDR4 Test Mode

50400 [tERR(2per) Rising Edge Measurements]

50500 [tERR(3per) Rising Edge Measurements]

50600 [tERR(4per) Rising Edge Measurements]

50700 [tERR(5per) Rising Edge Measurements]

50800 [tERR(6per) Rising Edge Measurements]

50900 [tERR(7per) Rising Edge Measurements]

51000 [tERR(8per) Rising Edge Measurements]

51100 [tERR(9per) Rising Edge Measurements]

51200 [tERR(10per) Rising Edge Measurements]

51300 [tERR(11per) Rising Edge Measurements]

51400 [tERR(12per) Rising Edge Measurements]

53000 [tERR(nper) Rising Edge Measurements]

LPDDR4X (Differential) Test Mode

60400 [tERR(2per) Rising Edge Measurements]

60500 [tERR(3per) Rising Edge Measurements]

60600 [tERR(4per) Rising Edge Measurements]

60700 [tERR(5per) Rising Edge Measurements]

60800 [tERR(6per) Rising Edge Measurements]

60900 [tERR(7per) Rising Edge Measurements]

61000 [tERR(8per) Rising Edge Measurements]

61100 [tERR(9per) Rising Edge Measurements]

61200 [tERR(10per) Rising Edge Measurements]

61300 [tERR(11per) Rising Edge Measurements]

61400 [tERR(12per) Rising Edge Measurements]

63000 [tERR(nper) Rising Edge Measurements]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tERR(2per) [Cumulative error across 2 cycles] tERR(3per) [Cumulative error across 3 cycles] tERR(4per) [Cumulative error across 4 cycles] tERR(5per) [Cumulative error across 5 cycles] tERR(6per) [Cumulative error across 6 cycles] tERR(7per) [Cumulative error across 7 cycles] tERR(8per) [Cumulative error across 8 cycles] tERR(9per) [Cumulative error across 9 cycles] tERR(10per) [Cumulative error across 10 cycles] tERR(11per) [Cumulative error across 11 cycles] tERR(12per) [Cumulative error across 12 cycles] tERR(13per) [Cumulative error across 13 cycles] tERR(14per) [Cumulative error across 14 cycles] tERR(15per) [Cumulative error across 15 cycles] tERR(16per) [Cumulative error across 16 cycles] tERR(17per) [Cumulative error across 17 cycles] tERR(18per) [Cumulative error across 18 cycles] tERR(nper) [Cumulative error across n = 13, 14, 15 . . . 49, 50 cycles]

LPDDR4 / LPDDR4X (Differential) Test Modes

There is no reference available for this test in the specification document. The measurement result is reported as “Information Only”.

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock. Supported measurements include multiple cycle windows with values of “n” (for “n” cycles) where, n is greater than 13 but less than 50.

Test Procedure: **DDR4 (for Test ID 400, 500, 600, 700, 800, 900, 1000, 1100, 1200, 3000)**

LPDDR4 (for Test ID 50400, 50500, 50600, 50700, 50800, 50900, 51000, 51100, 51200, 53000)

LPDDR4X (for Test ID 60400, 60500, 60600, 60700, 60800, 60900, 61000, 61100, 61200, 63000)

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

tERR(2per) is very similar to tJIT(per), except that a small 2-cycle window is formed inside a large 200-cycle window. The width of the total consecutive cycles for the small window (denoted as W) is compared against equivalent number of consecutive average cycles (denoted as C) obtained from

the large 200-cycle window (n x C), where C is the average value of the 200 cycle large window and n is the number of cycles. In the case of tERR(2per), n = 2. The steps described in the following procedure cover for all cycles, when n is replaced by the respective number of cycles.

1 Calculate the average period inside the first large 200-cycle window, denote as C_1.

2 Calculate the small window width, W (total width of 2 consecutive cycles). The first small window would cover period #1 and period #2.

3 Calculate the cumulative error value from C_1 and W found above using the equation below, where n=2 for tERR(2 per).

tERR(nper) = W - n x C_1, where n is the number of consecutive cycles

4 Sweep the small window across by one period and find the width of the next 2 consecutive cycles (the next small window would cover period #2 and period #3).

5 Repeat step 3 with the new value of W.

6 Repeat the process described in steps 1 to 5 until the last small window within C_1 (from period#199 to period#200) is covered.

7 Find the worst error from step 4 and denote it as CumErr1.

8 Repeat steps 1 to 7 to derive CumErr2 (for the second large 200-cycle window of period cycle #2 to #201) and CumErr3 (for the third large 200-cycle window of period cycle #3 to #202).

9 Determine the worst error CumErr1, CumErr2 and CumErr3. Report the worst value as the result for tERR(2per).

tERR(3per) is the same as tERR(2per) except that the small window size is 3-cycle wide. tERR(4per) uses a smaller window size of 4-cycle period and tERR(5per) uses an even smaller window size of 5-cycle period. The same pattern is applied for tERR(6per), tERR(7per), tERR(8per), tERR(9per), tERR(10per), tERR(11per), tERR(12per), tERR(13per), tERR(14per), tERR(15per), tERR(16per), tERR(17per), tERR(18per) and tERR(nper), which follows the same principle for tERR(13per) through tERR(50per).

Expected/ Observable Results:

DDR4 Test Mode

All measured values of tERR(nper) for the test signal shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X (Differential) Test Modes

All measured values of tERR(nper) for the test signal as reported as “Information Only”.

Pulse Measurements

tCH(abs) Absolute clock HIGH Pulse Width

Mode Supported: DDR4, LPDDR4, LPDDR4X (Both Differential and Single-Ended)

Test ID: **DDR4 Test Mode**

2200 [tCH(abs) Absolute Clock HIGH pulse width]

LPDDR4 Test Mode

52200 [tCH(abs) Absolute Clock HIGH pulse width]

LPDDR4X (Differential) Test Mode

62200 [tCH(abs) Absolute Clock HIGH pulse width]

LPDDR4X (Single-ended) Test Mode

72200 [tCH(abs) Absolute Clock HIGH pulse width]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tCH(abs) [Absolute Clock HIGH Pulse Width]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.1.4	-	-

NOTE This test is regarded as “Information Only” because this parameter is not subject to production tests as mentioned in section 10.1.4 of the JEDEC specification.

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC JC-42.6-1847.17, 28 November 2017	2.1.8	6	tCH(abs) [Absolute High clock pulse width]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X Test Modes**

The purpose of this test is to measure the absolute duty cycle of all positive pulse widths within a window of 200 consecutive cycles.

Test Procedure: **DDR4 (for Test ID 2200) / LPDDR4 (for Test ID 52200) / LPDDR4X (for Test IDs 62200 and 72200) /**

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

1 Find the maximum high pulses width value for positive pulses #1 to #202.
2 Find the minimum high pulses width value for positive pulses #1 to #202.
3 Check these two results for the worst case values.
4 Compare the worst case values to the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4X (Single-ended) Test Mode

The measured value of tCH(abs) shall be within the conformance limits as specified in the JEDEC specification.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of tCH(abs) for the test signal is reported as “Information Only”.

tCL(abs) Absolute clock LOW pulse width

Mode Supported: DDR4, LPDDR4, LPDDR4X (Both Differential and Single-Ended)

Test ID: **DDR4 Test Mode**

2250 [tCL(abs) Absolute Clock LOW pulse width]

LPDDR4 Test Mode

52250 [tCL(abs) Absolute Clock LOW pulse width]

LPDDR4X (Differential) Test Mode

62250 [tCL(abs) Absolute Clock LOW pulse width]

LPDDR4X (Single-ended) Test Mode

72250 [tCL(abs) Absolute Clock LOW pulse width]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tCL(abs) [Absolute Clock LOW Pulse Width]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.1.4	-	-

NOTE This test is regarded as “Information Only” because this parameter is not subject to production tests as mentioned in section 10.1.4 of the JEDEC specification.

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC JC-42.6-1847.17, 28 November 2017	2.1.8	6	tCL(abs) [Absolute Low clock pulse width]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X Test Modes**

The purpose of this test is to measure the absolute duty cycle of all negative pulse widths within a window of 200 consecutive cycles.

Test Procedure: **DDR4 (for Test ID 2250) / LPDDR4 (for Test ID 52250) / LPDDR4X (for Test IDs 62250 and 72250)**

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

1 Find the maximum low pulses width value for negative pulses #1 to #202.

2 Find the minimum low pulses width value for negative pulses #1 to #202.

3 Check these two results for the worst case values.

4 Compare the worst case values to the compliance test limits.

Expected/ Observable Results:

DDR4 Test Mode / LPDDR4X (Single-ended)

The measured value of tCL(abs) shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of tCL(abs) for the test signal is reported as “Information Only”.

tCH Average High Measurements

Mode Supported: DDR4, LPDDR4, LPDDR4X (Both Differential and Single-Ended)

Test ID: **DDR4 Test Mode**

2000 [tCH Average High Measurements]

LPDDR4 Test Mode

52000 [tCH Average High Measurements]

LPDDR4X (Differential) Test Mode

62000 [tCH Average High Measurements]

LPDDR4X (Single-ended) Test Mode

72000 [tCH Average High Measurements]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tCH(avg) [Average High Pulse Width]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.2	Table 218	tCH(avg) [Average High Pulse Width]

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC JC-42.6-1847.17, 28 November 2017	2.1.8	Table 6	tCH(avg) [Average High Pulse Width]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X Test Modes**

The purpose of this test is to measure the average duty cycle of all positive pulse widths within a window of 200 consecutive cycles.

Test Procedure: **DDR4 (for Test ID 2000) / LPDDR4 (for Test ID 52000) / LPDDR4X (for Test IDs 62000 and 72000)**

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

1 Measure a sliding “window” of 200 cycles.
2 Measure the width of the high pulses from cycle #1 to cycle #200 and determines the average value for this window. This generates one measurement result.
3 Measure the width of the high pulses from cycle #2 to cycle #201 and determines the average value for this window. This generates one more measurement result and two measurement values, overall.

4 Measure the width of the high pulses from cycle #3 to cycle #202 and determines the average value for this window.This generates one more measurement result and three measurement results, overall.

5 Check the three measured values for the smallest and largest values, which are recorded as the worst case values.

6 Compare the worst case values to the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X Test Modes

The measured value of tCH(avg) shall be within the conformance limits as per the JEDEC specification.

tCL Average Low Measurements

Mode Supported: DDR4, LPDDR4, LPDDR4X (Both Differential and Single-Ended)

Test ID: **DDR4 Test Mode**

2050 [tCL Average Low Measurements]

LPDDR4 Test Mode

52050 [tCL Average Low Measurements]

LPDDR4X (Differential) Test Mode

62050 [tCL Average Low Measurements]

LPDDR4X (Single-ended) Test Mode

72050 [tCL Average Low Measurements]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tCL(avg) [Average low Pulse Width]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.2	Table 218	tCL(avg) [Average low Pulse Width]

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC JC-42.6-1847.17, 28 November 2017	2.1.8	Table 6	tCL(avg) [Average low Pulse Width]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X Test Modes**

The purpose of this test is to measure the average duty cycle of all negative pulse widths within a window of 200 consecutive cycles.

Test Procedure: **DDR4 (for Test ID 2050) / LPDDR4 (for Test ID 52050) / LPDDR4X (for Test IDs 62050 and 72050)**

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

1 Measure a sliding “window” of 200 cycles.
2 Measure the width of the low pulses 1 to 200 and determines the average value for this window. This generates one measurement result.
3 Measure the width of the low pulses from 2 to 201 and determines the average value for this window. This generates one more measurement result and two measurement values overall.
4 Measure the width of the low pulses 3 to 202 and determines the average value for this window. This generates one more measurement result and three measurement results overall.

5 Check the three measured values for the smallest and largest values, which are recorded as the worst case values.

6 Compare the worst case values to the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X Test Mode

The measured value of tCL(avg) shall be within the conformance limits as per the JEDEC specification.

tjit(duty-high) Jitter Average High Measurements

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

2100 [tjit(duty-high) Jitter Average High Measurements]

NOTE For SDRAM type DDR4, this test appears under the Select Tests tab only when you set the Test Mode to Custom under the Set Up tab of the Test Application.

LPDDR4 Test Mode

52100 [tjit(duty-high) Jitter Average High Measurements]

LPDDR4X (Differential) Test Mode

62100 [tjit(duty-high) Jitter Average High Measurements]

References: **DDR4 Test Mode**

NOTE This test is regarded as “Information Only” because the test limits defined in the specification are not fully defined.

LPDDR4 / LPDDR4X (Differential) Test Modes

There is no reference available for this test in the specification document. The measurement result is reported as “Information Only”.

Test Overview: **DDR4/ LPDDR4 / LPDDR4X (Differential) Test Modes**

The tJIT(duty-high) Jitter Average High Measurement measures the time period between a positive pulse width of a cycle in the waveform and the average positive pulse width of all cycles in a 200 consecutive cycle window.

Test Procedure: **DDR4 (for Test ID 2100) / LPDDR4 (for Test ID 52100) / LPDDR4X (Differential) (for Test ID 62100)**

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

- For tJIT(duty-high) measurement, the Compliance Test Application:

1 Measures the difference between every high pulse width inside a 200 cycle window with the average of the whole window.

2 Calculates the average for high pulse width from 1 to 200.

3 Measures the difference between high pulse width #1, high pulse width #2 and so on up to high pulse width #200; with the average and saves the resulting value as a measurement result. A total of 200 measurement results are generated.

4 For the next set of measurement values, slide the window by one period and the application measures the average of high pulse width #2 up to high pulse width #201.

5 Compares high pulse width #2 with the new average. Continue the comparison for high pulse width #3, #4 and so on up to high pulse width #201. A total of 200 additional measurement results are generated such that there are 400 measured values overall.

6 For the next set of measurement values, slide the window by one more period and the application measures the average of high pulse width #3 up to high pulse width #202.

7 Compares high pulse width #3 with the new average.
Continue the comparison for high pulse width #4, #5 and so on up to high pulse width #202.
A total of 200 additional measurement results are generated such that there are 600 measured values overall.

8 Check the 600 measured values for the smallest and largest values, which are recorded as the worst case values.

9 Compare the worst case values to the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of tJIT(duty-high) for the test signal is reported as “Information Only”.

tjit(duty-low) Jitter Average Low Measurements

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

2150 [tjit(duty-low) Jitter Average Low Measurements]

NOTE For SDRAM type DDR4, this test appears under the Select Tests tab only when you set the Test Mode to Custom under the Set Up tab of the Test Application.

LPDDR4 Test Mode

52150 [tjit(duty-low) Jitter Average Low Measurements]

LPDDR4X (Differential) Test Mode

62150 [tjit(duty-low) Jitter Average Low Measurements]

References: **DDR4 Test Mode**

NOTE This test is regarded as “Information Only” because the test limits defined in the specification are not fully defined.

LPDDR4 / LPDDR4X (Differential) Test Modes

There is no reference available for this test in the specification document. The measurement result is reported as “Information Only”.

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The tJIT(duty-low) Jitter Average Low Measurement measures the time period between a negative pulse width of a cycle in the waveform and the average negative pulse width of all cycles in a 200 consecutive cycle window.

Test Procedure: **DDR4 (for Test ID 2150) / LPDDR4 (for Test ID 52150) / LPDDR4X (Differential) (for Test ID 62150)**

Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

- For tJIT(duty-low) measurement, the Compliance Test Application:

1 Measures the difference between every low pulse width inside a 200 cycle window with the average of the whole window.

2 Calculates the average for low pulse width from 1 to 200.

3 Measures the difference between low pulse width #1, low pulse width #2 and so on up to low pulse width #200; with the average and saves the resulting value as a measurement result. A total of 200 measurement results are generated.

4 For the next set of measurement values, slide the window by one period and the application measures the average of low pulse width #2 up to low pulse width #201.

5 Compares low pulse width #2 with the new average. Continue the comparison for low pulse width #3, #4 and so on up to low pulse width #201. A total of 200 additional measurement results are generated such that there are 400 measured values overall.

6 For the next set of measurement values, slide the window by one more period and the application measures the average of low pulse width #3 up to low pulse width #202.

7 Compares low pulse width #3 with the new average.
Continue the comparison for low pulse width #4, #5 and so on up to low pulse width #202.
A total of 200 additional measurement results are generated such that there are 600 measured values overall.

8 Check the 600 measured values for the smallest and largest values, which are recorded as the worst case values.

9 Compare the worst case values to the compliance test limits.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of tJIT(duty-low) for the test signal is reported as “Information Only”.

Timing tests (Command Address timing)

tIS(base)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30201 [tIS (base)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tIS (base) [Command and Address setup time to CK_t, CK_c referenced to Vih(ac)/Vil(ac) levels]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the time interval from the address or control (Add/Ctrl Rising/Falling edge) set up time to the associated clock rising edge.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 (for Test ID 30201)**

1 Acquire and validate that the Clock and CA signal crosses the thresholds.
2 Find all edges of the Clock and CA signals.
3 Perform the setup time measurement.
   a On every rising or falling edge (or both edges) of the acquired and valid CA signal on the upper threshold, find:
      i The first closest rising edge of the Clock on the middle threshold for 1T clocking method
      ii The second closest rising edge of the Clock on the middle threshold for 2T clocking method
   b Under the Configure tab of the Compliance Test Application, use the label “Edge Type for SetupTime measurements” to configure the required rising edge or falling edge (or both edges) on the CA signal.
   c Also, use the label “Clocking Method” in the Configure tab to configure the clocking method.
4 The minimum value of the measurement is reported as the test result.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured values of tIS (base) shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

tIH(base)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30202 [tIH (base)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tIH (base) [Command and Address hold time to CK_t, CK_c referenced to Vih(dc)/Vil(dc) levels]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the time interval from the address or control (Add/Ctrl Rising/Falling edge) hold time to the associated clock crossing edge.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 30202)**

1 Acquire and validate that the Clock and CA signals cross the thresholds.
2 Find all edges of the Clock and CA signals.
3 Perform hold time measurement.
At every rising edge of the Clock signal on the middle threshold, find the closest rising or falling edge (or both edges) of the acquired and valid CA signal on the upper threshold.
4 Under the Configure tab of the Compliance Test Application, use the label “Edge Type for HoldTime measurements” to configure the required rising edge or falling edge (or both edges) on the CA signal.
5 The minimum value of the measurement is reported as the test result.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured values of tIH (base) shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

tIS(derate)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30203 [tIS (derate)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.7	Table 175, 177 and 178	tIS(base, AC100) tIS(base, AC 90) ΔtIS

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify that the time interval from address or control (Add/Ctrl Rising/Falling edge) set up time to the associated clock crossing edge is within the conformance limits as specified in the JEDEC Specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 30203)**

1 Acquire and validate that the Clock and CA signals cross the thresholds.

2 Find all edges of the Clock and CA signals.

3 Perform the setup time measurement.

   a On every rising or falling edge (or both edges) of the acquired and valid CA signal on the upper threshold, find:

      i The first closest rising edge of the Clock on the middle threshold for 1T clocking method

      ii The second closest rising edge of the Clock on the middle threshold for 2T clocking method

   b Under the **Configure** tab of the Compliance Test Application, use the label “Edge Type for SetupTime measurements” to configure the required rising edge or falling edge (or both edges) on the CA signal.

   c Also, use the label “Clocking Method” in the **Configure** tab to configure the clocking method.

4 The minimum value of the measurement is reported as the test result.

5 The mean slew rate is measured for all Add/Ctrl and CK edges for determining the ΔtIS derating value based on the derating table.

6 The test limit for tIS(derate) test = tIS(base) + ΔtIS

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results:

DDR4 Test Mode

The measured values of tIS(derate) shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

tIH(derate)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30204 [tIH (derate)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.7	Table 175, 177 and 178	tIH(base, DC75) tIH(base, DC 65) ΔtIH

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify that the time interval from address or control (Add/Ctrl Rising/Falling edge) hold time to the associated clock crossing edge is within the conformance limits as specified in the JEDEC Specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 30204)**

1 Acquire and validate that the Clock and CA signals cross the thresholds.

2 Find all edges of the Clock and CA signals.

3 Perform hold time measurement.

At every rising edge of the Clock signal on the middle threshold, find the closest rising or falling edge (or both edges) of the acquired and valid CA signal on the upper threshold.

4 Under the **Configure** tab of the Compliance Test Application, use the label “Edge Type for HoldTime measurements” to configure the required rising edge or falling edge (or both edges) on the CA signal.

5 The minimum value of the measurement is reported as the test result.

6 The mean slew rate is measured for all Add/Ctrl and CK edges for determining the ΔtIH derating value based on the derating table.

7 The test limit for tIH(derate) test = tIH(base) + ΔtIH

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured values of tIH(derate) shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

tCKE

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30206 [tCKE]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tCKE [CKE minimum pulse width]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify that the pulse width of the Clock Enable (CKE) signal must be within the conformance limit as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 (for Test ID 30206)**

1 Acquire and validate that the Clock signal crosses the thresholds.
2 Find all edges on the Clock signals.
3 With all crossings found on the rising/falling edge of the CKE signal and all crossings found on the rising edge of the Clock signal:
   a On the rising/falling edge of the CKE signal, find the nearest rising edge of the Clock signal to the right and denote it as ClkEdge1.
   b On the next rising/falling edge of the CKE signal, find the nearest rising edge of the Clock signal to the right and denote it as ClkEdge2.
4 Calculate the time difference and repeat steps 3a and 3b for all CKE edges found earlier.
5 Determine the worst time difference measured.
6 Report the value of tCKE for the final test result.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured tCKE value for the test signal shall be within the conformance limits as per the JEDEC specification mentioned in the References section.

LPDDR4 / LPDDR4X Test Modes

Not Available.

tIPW

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30207 [tIPW]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	tIPW [Control and Address Input pulse width for each input]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify that the pulse width of the high level or low level of address and control signal must be within the conformance limit as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 (for Test ID 30207)**

1 Pre-condition the oscilloscope.
2 Trigger on either the rising or the falling edge of the address or control signal under test.
3 Find all such crossings on the rising/falling edge of the signal under test that cross VrefCA.
4 On the signal under test, measure tIPW as the time starting from the rising edge and ending at the consecutive falling edge and as the time starting from the falling edge and ending at the consecutive rising edge.
5 Collect all values of tIPW.
6 Determine the worst result from the set of tIPW values measured.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured tIPW value for the test signal shall be within the conformance limits as per the JEDEC specification mentioned in the References section.

LPDDR4 / LPDDR4X Test Modes

Not Available.

tIS(Vref)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30208 [tIS(Vref)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	Command and Address setup time to CK_t, CK_c referenced to Vref levels

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the time interval from the address or control (Add/Ctrl Rising/Falling edge) set up time to the associated clock rising edge.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 (for Test ID 30208)**

1 Acquire and validate that the Clock and CA signal crosses the thresholds.
2 Find all edges of the Clock and CA signals.
3 Perform the setup time measurement.
   a On every rising or falling edge (or both edges) of the acquired and valid CA signal at VrefCA level, find:
      i The first closest rising edge of the Clock on the middle threshold for 1T clocking method
      ii The second closest rising edge of the Clock on the middle threshold for 2T clocking method
   b Under the Configure tab of the Compliance Test Application, use the label “Edge Type for SetupTime measurements” to configure the required rising edge or falling edge (or both edges) on the CA signal.
   c Also, use the label “Clocking Method” in the Configure tab to configure the clocking method.
4 The minimum value of the measurement is reported as the test result.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured values of tIS(Vref) shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

tIH(Vref)

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

30209 [tIH(Vref)]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.4	Table 172	Command and Address hold time to CK_t, CK_c referenced to Vref levels

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the time interval from the address or control (Add/Ctrl Rising/Falling edge) hold time to the associated clock crossing edge.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 Test Mode (for Test ID 30209)**

1 Acquire and validate that the Clock and CA signals cross the thresholds.

2 Find all edges of the Clock and CA signals.

3 Perform hold time measurement.
At every rising edge of the Clock signal on the middle threshold, find the closest rising or falling edge (or both edges) of the acquired and valid CA signal at VrefCA level.

4 Under the Configure tab of the Compliance Test Application, use the label “Edge Type for Hold Time measurements” to configure the required rising edge or falling edge (or both edges) on the CA signal.

5 The minimum value of the measurement is reported as the test result.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured values of tIH(Vref) shall be within the conformance limits as per the JEDEC specification.

LPDDR4 / LPDDR4X Test Modes

Not available.

6 Eye Diagram Tests

Overview

The following group pertains to tests that require the generating and processing of an eye diagram when performing test measurements.

Threshold Settings for R/W Separation [Eye Diagram Tests]

Table 11, Table 12. and Table 13 list the threshold settings that are used to process the acquired bursts and that separate the Read and Write bursts. These settings affect the results of Read/Write Separation. There are three threshold modes under 'Threshold Mode' in the Configure tab that determine the threshold values that are used by the Compliance Test Application for Read/Write Separation.

Table 11 Threshold Settings - TopBaseRatio (Auto)

Burst Separation Method	Threshold values used by Compliance Application	Config Variable Names	Note
DQS-DQ Phase Difference	DQS Upper Threshold	DQS Channel Top Ratio	1
	DQS Middle Threshold	DQS Channel Middle Ratio	1
	DQ Middle Threshold	DQ Channel Middle Ratio	2
	DQ-DQS Phase-Shift Threshold	DQ to DQS Phase Shift for Read (%) or DQ to DQS Phase Shift for Write (%)	
Pre-Amble Pattern	DQS Upper Threshold	DQS Upper Threshold for Burst Trigger Method (V)	
	DQS Middle Threshold	DQS Middle Threshold for Burst Trigger Method (V)	
	DQS Lower Threshold	DQS Lower Threshold for Burst Trigger Method (V)	
	DQ Middle Threshold	VRefDQ (V)	
Rd or Wrt Only	DQS Upper Threshold	DQS Channel Top Ratio	1
	DQS Middle Threshold	DQS Channel Middle Ratio	1
	DQ Middle Threshold	DQ Channel Middle Ratio	2

Note 1 – Example: If DQS signal is fed to Channel 1 of the Oscilloscope, Channel 1's Top and Base Ratios are used internally as threshold values by the Compliance Application (see Figure 93). For Middle Ratio, 0V is used for differential signals. Otherwise, the Middle Ratio value used is the average of Top and Base Ratio values for single-ended signals. The threshold is set based on the ratio of the peak-to-peak voltage DQS signal.

Note 2 – Example: The same behavior mentioned above applies for DQ Channel signal.

NOTE The MSOx Logic Triggering method is supported for Electrical and Timing Tests only, and not for Eye Diagram tests.

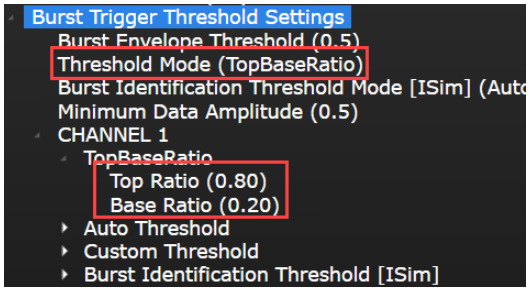


Figure 93 TopBaseRatio Threshold settings

Table 12 Custom Threshold Settings (Manual)

Burst Separation Method	Threshold values used by Compliance Application	Config Variable Names	Note
DQS-DQ Phase Difference	DQS Upper Threshold	DQS Channel Upper Threshold (V)	1
	DQS Middle Threshold	DQS Channel Middle Threshold (V)	1
	DQ Middle Threshold	DQ Channel Middle Threshold (V)	2
	DQ-DQS Phase-Shift Threshold	DQ to DQS Phase Shift for Read (%) or DQ to DQS Phase Shift for Write (%)	
Pre-Amble Pattern	DQS Upper Threshold	DQS Upper Threshold for Burst Trigger Method (V)	
	DQS Middle Threshold	DQS Middle Threshold for Burst Trigger Method (V)	
	DQS Lower Threshold	DQS Lower Threshold for Burst Trigger Method (V)	
	DQ Middle Threshold	VRefDQ (V)	
Rd or Wrt Only	DQS Upper Threshold	DQS Channel Upper Threshold (V)	1
	DQS Middle Threshold	DQS Channel Middle Threshold (V)	1
	DQ Middle Threshold	DQ Channel Middle Threshold (V)	2

Note 1 – Example: If DQS signal is fed to Channel 1 of the Oscilloscope, Channel 1's Upper, Middle and Lower Thresholds are used internally as threshold values by the Compliance Application (see Figure 94).

Note 2 – Example: The same behavior mentioned above applies for DQ Channel signal.

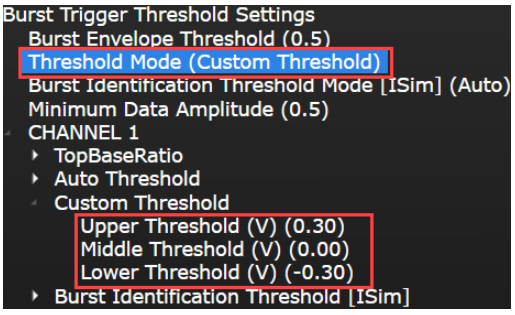


Figure 94 Manual Threshold settings

Table 13 Auto Threshold Settings

Burst Separation Method	Threshold values used by Compliance Application	Config Variable Names	Note
DQS-DQ Phase Difference	DQS Upper Threshold	DQS Channel Top Ratio	1
	DQS Middle Threshold	DQS Channel Middle Ratio	1
	DQ Middle Threshold	DQ Channel Middle Ratio	2
	DQ-DQS Phase-Shift Threshold	DQ to DQS Phase Shift for Read (%) or DQ to DQS Phase Shift for Write (%)	

Note 1 – Example: If DQS signal is fed to Channel 1 of the Oscilloscope, Channel 1's Top and Base Ratios are used internally as threshold values by the Compliance Application (see Figure 95). For Middle Ratio, 0V is used for differential signals. Otherwise, the Middle Ratio value used is the average of Top and Base Ratio values for single-ended signals. The threshold is set based on the ratio of the peak-to-peak voltage DQS signal.

Note 2 – Example: The same behavior mentioned above applies for DQ Channel signal.

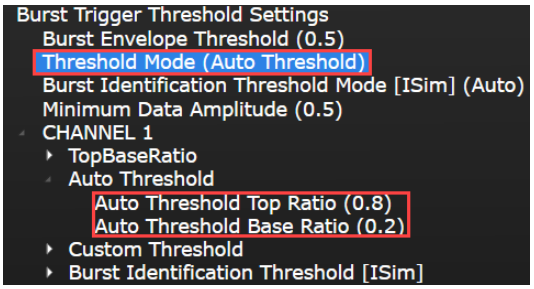


Figure 95 Auto Threshold settings

DDR Read/Write Separation [Eye Diagram Tests]

It is essential to separate the Read and Write bursts for most tests that must be performed on specific Read burst or Write burst region. Table 14 lists the Burst Trigger Method for Read/Write Separation.

Table 14 Burst Trigger Methods for Read/Write Separation

Burst Separation Method	Description	Signal to evaluate Read or Write	Available in DDR4	Available in LPDDR4
DQS-DQ Phase Difference	Uses phase difference between DQS and DQ to differentiate Read and Write bursts	DQS and DQ	Yes	Yes
Pre-Amble Pattern	Use DQS preamble pattern to differentiate Read and Write bursts	DQS Only	No	Yes
Rd or Wrt Only	Does not differentiate Read and Write bursts. All the bursts in the acquisition are presumed to be the burst of interest.	DQS Only	Yes	Yes

Figure 96 to Figure 98 show flowcharts depicting the process of Read/Write Separation.

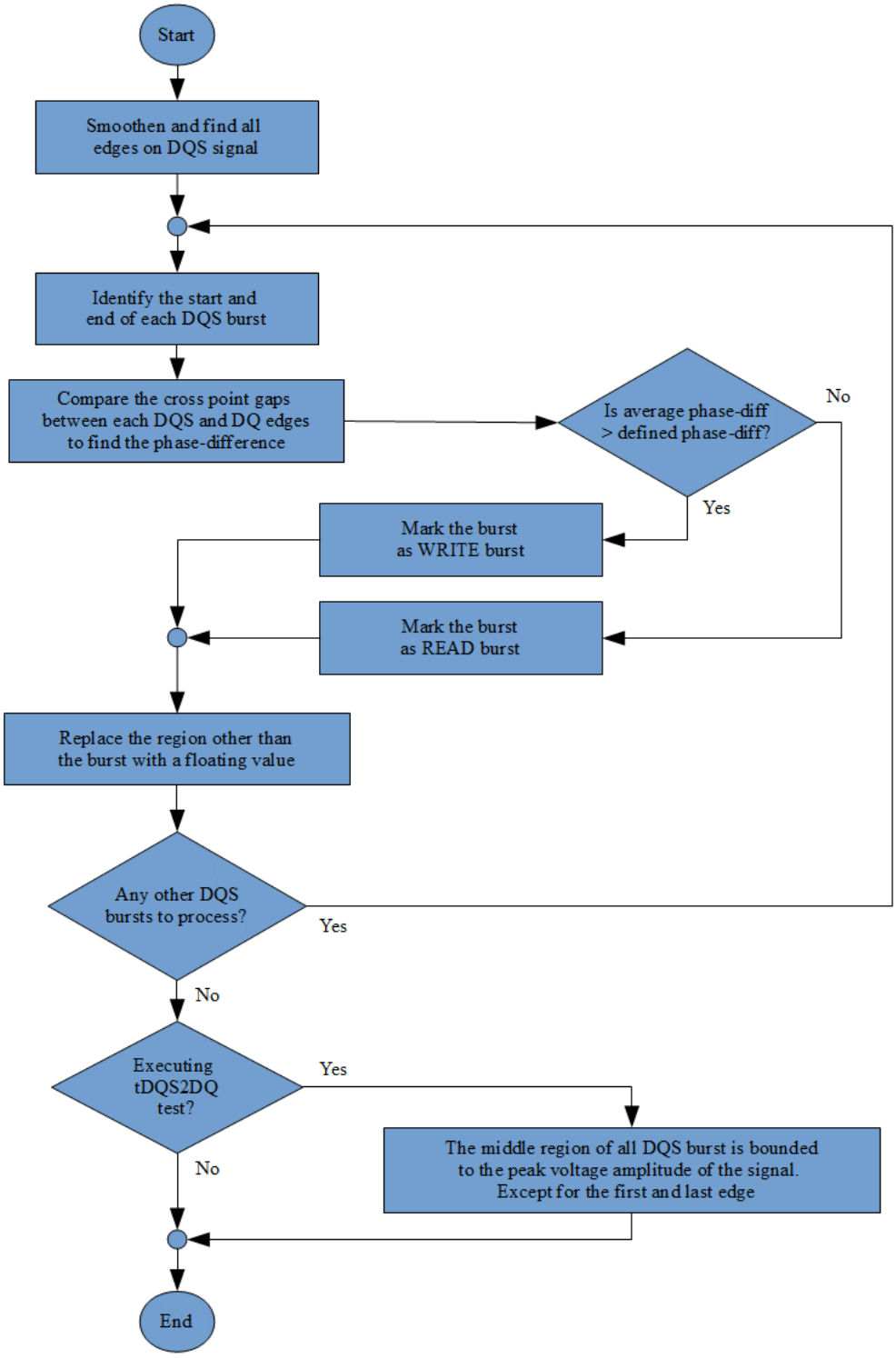


Figure 96 DQS-DQ Phase Difference (Eye Diagram Tests)

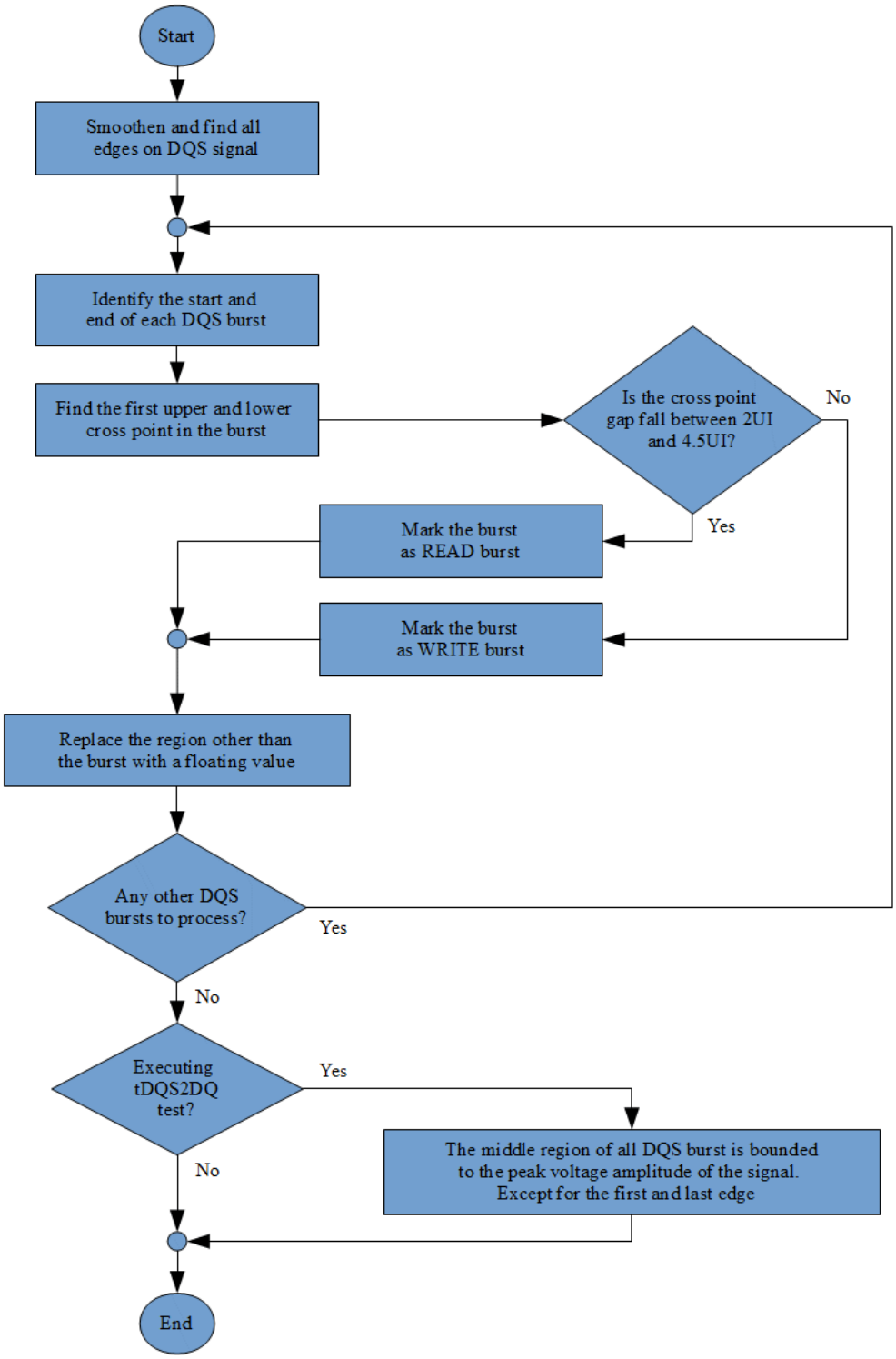


Figure 97 Pre-Amble Pattern (Eye Diagram Tests)

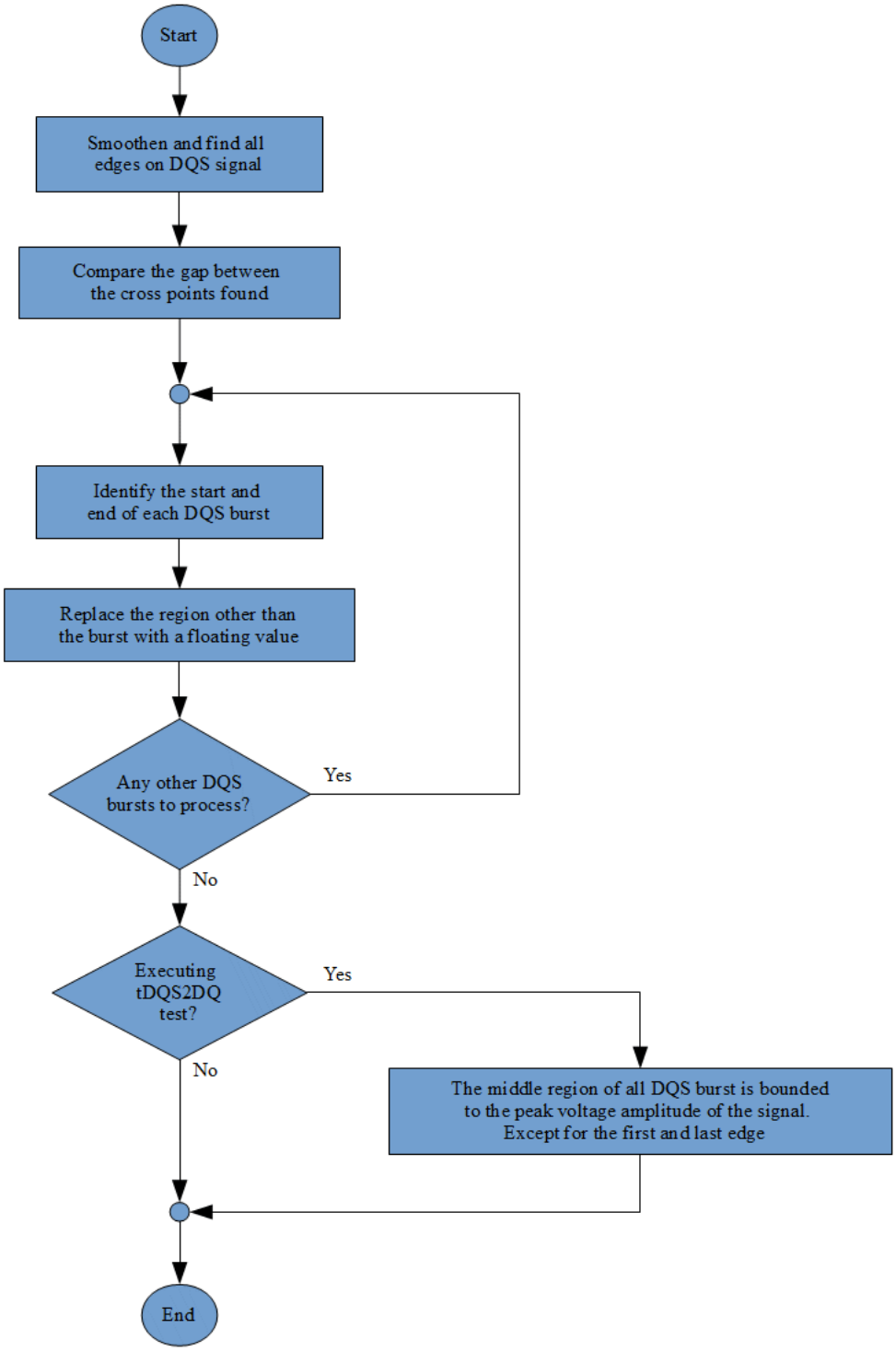


Figure 98 Read or Write Only (Eye Diagram Tests)

Eye-Diagram for Data and Data Strobe (WRITE)

WRITE cycle tests

Eye Diagram Test for Write Cycle

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

20402 [Eye Diagram Test for Write Cycle]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Not available.

NOTE For SDRAM type DDR4, this test appears under the **Select Tests** tab only when you set the **Test Mode** to **Custom** under the **Set Up** tab of the Test Application.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to generate an eye diagram for the WRITE cycle.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 (for Test ID 20402)**

1 Calculate initial time scale value based on selected DDR4 speed grade options.
2 Calculate number of sampling points according to the time scale value.
3 Check for valid DQS input test signals by verifying its frequency and amplitude values.
4 Set up the oscilloscope:
   a Using UDF methodology, separate Write burst and return the filtered DQS signals in the form of recovered clock for eye folding later.
   b Set up measurement threshold values for the DQ channel and the DQS channel input.
   c Set up vertical scale values for DQ channel and DQS channel input.
   d Set the Color Grade Display option to ON.
   e Set up Mask Test settings.
   f Set up Clock Recovery settings on SDA.

   : Explicit clock, Source = Filtered DQS, Rise/Fall Edge
   g Set Real Time Eye on SDA to ON.
5 Perform Eye Folding:
   a Set the Mask Test Run setting to ‘Forever’.
   b Load the mask file and start the Mask Test.
   c Stop the Mask Test when the counter for ‘Total Waveforms’ exceeds the number of required waveforms specified in the configuration option ‘Total Waveform’.

6 Once the count for required waveforms is reached, it marks the end of test.

Expected/ Observable Results:

LPDDR4 / LPDDR4X Test Modes

Not available.

DDR4 Test Mode

This test is reported as “Information Only”.

LPDDR4 / LPDDR4X Test Modes

Not available.

tDIVW Margin

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

20403 [tDIVW Margin]

LPDDR4 Test Mode

50403 [tDIVW Margin]

LPDDR4X (Differential) Test Mode

60403 [tDIVW Margin]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.6	Table 174	TdIVW [Rx timing window]

NOTE This test does not measure the tdIVW parameter directly (which is, otherwise, documented in the DDR4 JESD79-4B specifications). This test is customized based on user inputs during the DDR4 application development initially.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.6	Table 222	TdIVW_total [Rx timing window total (at VdIVW voltage levels)]

NOTE This test does not measure the tDIVW_total parameter directly (which is, otherwise, documented in the LPDDR4 JESD209-4D specifications). This test is customized based on user inputs during the DDR4 application development initially.

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to measure the minimum tDIVW Margin of the WRITE eye diagram generated.

Test Procedure: **DDR4 (for Test ID 20403)**

1 Calculate the initial time scale value based on selected speed grade options in the Compliance Test Application.

2 Calculate the number of sampling points based on the time scale value calculated in the previous step.

3 Check for valid DQS input test signals by verifying its frequency and amplitude values.

4 Set up the oscilloscope:

a Using UDF methodology, separate Write burst and return the filtered DQS signals as Recovered Clock, which is used for eye folding later.

b Set up measurement threshold values for the DQx channel and the DQSx channel input.

c Set up fixed vertical scale values for DQx channel and DQSx channel input.

d Set the Color Grade Display option to ON.

e Set up Mask Test.

f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered DQS, Rise/Fall Edge

g Set the Real Time Eye on SDA to ON.

5 Perform Mask Testing:

a Set the Mask Test Run Until setting to 'Forever'.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

6 Determine and store the Vcent value.

There is an option to derive Vcent depending on the "Vcent Evaluation Mode" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "Widest eye opening level", the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

The detailed procedure for the "Widest eye opening level" requires that:

a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.

7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width of 0.2UI and a Test Mask height of 136mV.

8 Use the Histogram feature in the Infiniium Application to measure the tDIVW Margin value for all the four corners of the Test Mask.
The tDIVW Margin for each Test Mask corner is denoted by tDIVW_m1, tDIVW_m2, tDIVW_m3 and tDIVW_m4, as shown in Figure 99.

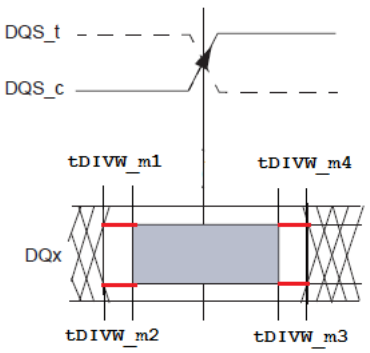


Figure 99 tDIVW Margins

9 Find the minimum value between tDIVW_m1, tDIVW_m2, tDIVW_m3 and tDIVW_m4. Use the minimum value as the worst time gap.

10 Calculate the margin (in percentage) using the equation:

$$\text{Margin (\%)} = [(\text{Worst\_time\_gap}) / (\text{Half of mask width})] \times 100\%$$

where, Worst_time_gap is the time gap between the mask and the eye at four corners m1, m2, m3, m4.

11 Report the worst time gap and margin percentage as test results.

LPDDR4 (for Test ID 50403) / LPDDR4X (Differential) (for Test ID 60403)

1 Calculate the initial time scale value based on selected speed grade options in the Compliance Test Application.

2 Calculate the number of sampling points based on the time scale value calculated in the previous step.

3 Check for valid DQS input test signals by verifying its frequency and amplitude values.

4 Set up the oscilloscope:

a Using UDF methodology, separate Write burst and return the filtered DQS signals as Recovered Clock, which is used for eye folding later.

b Set up measurement threshold values for the DQx channel and the DQSx channel input.

c Set up fixed vertical scale values for DQx channel and DQSx channel input.

d Set the Color Grade Display option to ON.

e Set up Mask Test.

f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered DQS, Rise/Fall Edge

g Set the Real Time Eye on SDA to ON.

5 Perform Mask Testing:

a Set the Mask Test Run Until setting to ‘Forever’.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for ‘Total Waveforms’ exceeds the number of required waveforms specified in the configuration option ‘Total Waveform’.

6 Determine and store the Vcent value.

There is an option to derive Vcent depending on the “Vcent Evaluation Mode” configuration option in the Compliance Test Application.

If the “Vcent Evaluation Mode” configuration option is set to “User defined Vcent”, the value of Vcent follows the value of the “User Defined Vcent” configuration option in the Compliance Test Application.

If the “Vcent Evaluation Mode” configuration option is set to “Widest eye opening level”, the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

The detailed procedure for the “Widest eye opening level” requires that:

a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.

7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width and a Test Mask height, which uses the values of the following configuration options in the Compliance Test Application:

Test Mask Width = tDIVW configuration option

Test Mask Height = vDIVW (V) configuration option

8 Use the Histogram feature in the Infiniium Application to measure the tDIVW Margin value for all the four corners of the Test Mask.
The tDIVW Margin for each Test Mask corner is denoted by tDIVW_m1, tDIVW_m2, tDIVW_m3 and tDIVW_m4, as shown in Figure 99.

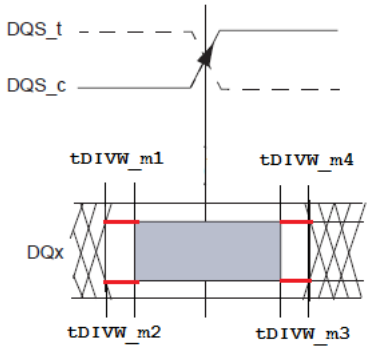


Figure 100 tDIVW Margins

9 Find the minimum value between tDIVW_m1, tDIVW_m2, tDIVW_m3 and tDIVW_m4. Use the minimum value as the worst time gap.

10 Calculate the margin (in percentage) using the equation:

$$\text{Margin (\%)} = [(\text{Worst\_time\_gap}) / (\text{Half of mask width})] \times 100\%$$

where, Worst_time_gap is the time gap between the mask and the eye at four corners m1, m2, m3, m4.

11 Report the worst time gap and margin percentage as test results.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured tDIVW Margin value for the test signal indicates if there is a violation in the mask region.

tDIVW

Mode Supported: DDR4, LPDDR4, LPDDR4X (Both Differential and Single-Ended)

Test ID: **DDR4 Test Mode**

120403 [tDIVW]

LPDDR4 Test Mode

150403 [tDIVW]

LPDDR4X (Differential) Test Mode

650403 [tDIVW]

LPDDR4X (Single-ended) Test Mode

750403 [tDIVW]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.6	Table 174	TdIVW [Rx timing window]

NOTE For SDRAM type DDR4, this test appears under the **Select Tests** tab only when you set the **Test Mode** to **Custom** in the under **Set Up** tab of the Test Application.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.6	Table 222	TdIVW_total [Rx timing window total (at VdIVW voltage levels)]

NOTE For SDRAM type LPDDR4/LPDDR4X (Differential), this test appears under the **Select Tests** tab only when you set the **Test Mode** to **Custom** in the under **Set Up** tab of the Test Application.

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC Standard No. 42.6, Item 1847.17, 28 Nov 2017	2.1.8	Table 6	TdIVW_total [Rx timing window total (at VdIVW voltage levels)]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X Test Modes**

The purpose of this test is to verify if there is any violation in the WRITE Eye Diagram with reference to the defined tDIVW_total parameter. Refer to Figure 188 of the JESD209-4D document.

Test Procedure: **DDR4 (for Test ID 120403)**

1 Calculate the initial time scale value based on selected speed grade options in the Compliance Test Application.

2 Calculate the number of sampling points based on the time scale value calculated in the previous step.

3 Check for valid DQS input test signals by verifying its frequency and amplitude values.

4 Set up the oscilloscope:

a Using UDF methodology, separate Write burst and return the filtered DQS signals as Recovered Clock, which is used for eye folding later.

b Set up measurement threshold values for the DQx channel and the DQSx channel input.

c Set up fixed vertical scale values for DQx channel and DQSx channel input.

d Set the Color Grade Display option to ON.

e Set up Mask Test.

f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered DQS, Rise/Fall Edge

g Set the Real Time Eye on SDA to ON.

5 Perform Mask Testing:

a Set the Mask Test Run Until setting to 'Forever'.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

6 Determine and store the Vcent value.

There is an option to derive Vcent depending on the "Vcent Evaluation Mode" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "Widest eye opening level", the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

The detailed procedure for the "Widest eye opening level" requires that:

a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.

7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width of 0.2UI and a Test Mask height of 136mV.

8 Measure the Eye Width at the Test Mask top level (tDIVW_top) and Eye Width at the Test Mask bottom level (tDIVW_bottom).

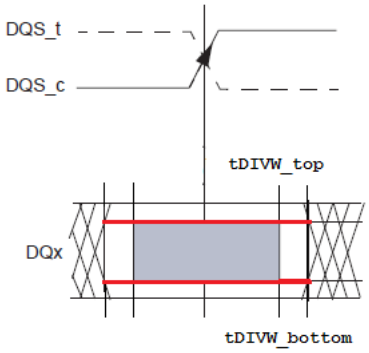


Figure 101 tDIVW_top and tDIVW_bottom

9 Find the minimum value between tDIVW_top and tDIVW_bottom. Use the minimum value as the worst test result.

10 Report the worst test result.

LPDDR4 (for Test ID 150403) / LPDDR4X (for Test IDs 650403 and 750403)

1 Calculate the initial time scale value based on selected speed grade options in the Compliance Test Application.

2 Calculate the number of sampling points based on the time scale value calculated in the previous step.

3 Check for valid DQS input test signals by verifying its frequency and amplitude values.

4 Set up the oscilloscope:

a Using UDF methodology, separate Write burst and return the filtered DQS signals as Recovered Clock, which is used for eye folding later.

b Set up measurement threshold values for the DQx channel and the DQSx channel input.

c Set up fixed vertical scale values for DQx channel and DQSx channel input.

d Set the Color Grade Display option to ON.

e Set up Mask Test.

f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered DQS, Rise/Fall Edge

g Set the Real Time Eye on SDA to ON.

5 Perform Mask Testing:

a Set the Mask Test Run setting to ‘Forever’.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for ‘Total Waveforms’ exceeds the number of required waveforms specified in the configuration option ‘Total Waveform’.

6 Determine and store the Vcent value.

There is an option to derive Vcent depending on the “Vcent Evaluation Mode” configuration option in the Compliance Test Application.

If the “Vcent Evaluation Mode” configuration option is set to “User defined Vcent”, the value of Vcent follows the value of the “User Defined Vcent” configuration option in the Compliance Test Application.

If the “Vcent Evaluation Mode” configuration option is set to “Widest eye opening level”, the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

The detailed procedure for the “Widest eye opening level” requires that:

a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.

7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width and a Test Mask height, which uses the values of the following configuration options in the Compliance Test Application:

Test Mask Width = tDIVW configuration option

Test Mask Height = vDIVW (V) configuration option

8 Measure the Eye Width at the Test Mask top level (tDIVW_top) and Eye Width at the Test Mask bottom level (tDIVW_bottom).

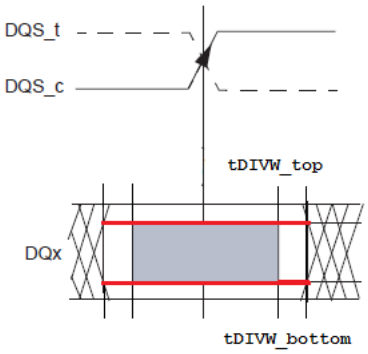


Figure 102 tDIVW_top and tDIVW_bottom

9 Find the minimum value between tDIVW_top and tDIVW_bottom. Use the minimum value as the worst test result.

10 Report the worst test result.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X Test Modes

The measured value of tDIVW for the test signal must be within the conformance limit as per the specification mentioned under the References section.

vDIVW Margin

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

20404 [vDIVW Margin]

LPDDR4 Test Mode

50404 [vDIVW Margin]

LPDDR4X (Differential) Test Mode

60404 [vDIVW Margin]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.6	Table 174	VdIVW [Rx Mask Voltage p-p]

NOTE This test does not measure the VdIVW parameter directly (which is, otherwise, documented in the DDR4 JESD79-4D specifications). This test is customized based on user inputs during the DDR4 application development initially.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.6	Table 222	VdIVW_total [Rx Mask Voltage p-p total]

NOTE This test does not measure the vDIVW_total parameter directly (which is, otherwise, documented in the LPDDR4 JESD209-4D specifications). This test is customized based on user inputs during the DDR4 application development initially.

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to measure the minimum vDIVW Margin of the WRITE eye diagram generated.

Test Procedure: **DDR4 (for Test ID 20404)**

1 Calculate the initial time scale value based on selected speed grade options in the Compliance Test Application.

2 Calculate the number of sampling points based on the time scale value calculated in the previous step.

3 Check for valid DQS input test signals by verifying its frequency and amplitude values.

4 Set up the oscilloscope:

a Using UDF methodology, separate Write burst and return the filtered DQS signals as Recovered Clock, which is used for eye folding later.

b Set up measurement threshold values for the DQx channel and the DQSx channel input.

c Set up fixed vertical scale values for DQx channel and DQSx channel input.

d Set the Color Grade Display option to ON.

e Set up Mask Test.

f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered DQS, Rise/Fall Edge

g Set the Real Time Eye on SDA to ON.

5 Perform Mask Testing:

a Set the Mask Test Run Until setting to 'Forever'.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

6 Determine and store the Vcent value.

There is an option to derive Vcent depending on the "Vcent Evaluation Mode" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "Widest eye opening level", the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

The detailed procedure for the "Widest eye opening level" requires that:

a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.

7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width of 0.2UI and a Test Mask height of 136mV.

8 Use the Histogram feature in the Infiniium Application to measure the vDIVW Margin value for the top and the bottom area of the Test Mask.
The measured vDIVW margin is denoted as vDIVW Margin upper and vDIVW Margin lower.

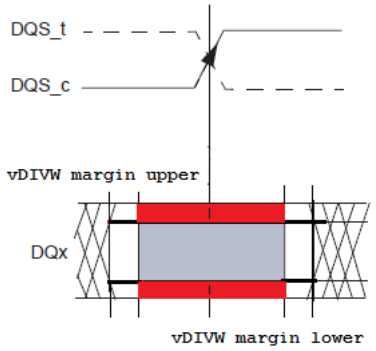


Figure 103 vDIVW Margin Upper and vDIVW Margin Lower

9 Find the minimum value between vDIVW Margin Upper and vDIVW Margin lower. Use this value as the worst voltage gap.

10 Calculate the worst margin (in percentage) using the equation:

$$\text{Margin (\%)} = [(\text{Worst\_voltage\_gap}) / (\text{Half of mask height})] \times 100\%$$

where, Worst_voltage_gap is the voltage gap between the mask and the eye at the top and bottom.

11 Report the worst voltage gap and the margin percentage as test results.

LPDDR4 (for Test ID 50404) / LPDDR4X (Differential) (for Test ID 60404)

1 Calculate the initial time scale value based on selected speed grade options in the Compliance Test Application.

2 Calculate the number of sampling points based on the time scale value calculated in the previous step.

3 Check for valid DQS input test signals by verifying its frequency and amplitude values.

4 Set up the oscilloscope:

a Using UDF methodology, separate Write burst and return the filtered DQS signals as Recovered Clock, which is used for eye folding later.

b Set up measurement threshold values for the DQx channel and the DQSx channel input.

c Set up fixed vertical scale values for DQx channel and DQSx channel input.

d Set the Color Grade Display option to ON.

e Set up Mask Test.

f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered DQS, Rise/Fall Edge

g Set the Real Time Eye on SDA to ON.

5 Perform Mask Testing:

a Set the Mask Test Run setting to ‘Forever’.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for ‘Total Waveforms’ exceeds the number of required waveforms specified in the configuration option ‘Total Waveform’.

6 Determine and store the Vcent value.

There is an option to derive Vcent depending on the “Vcent Evaluation Mode” configuration option in the Compliance Test Application.

If the “Vcent Evaluation Mode” configuration option is set to “User defined Vcent”, the value of Vcent follows the value of the “User Defined Vcent” configuration option in the Compliance Test Application.

If the “Vcent Evaluation Mode” configuration option is set to “Widest eye opening level”, the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

The detailed procedure for the “Widest eye opening level” requires that:

a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.

7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width and a Test Mask height, which uses the values of the following configuration options in the Compliance Test Application:

Test Mask Width = tDIVW configuration option

Test Mask Height = vDIVW (V) configuration option

8 Use the Histogram feature in the Infiniium Application to measure the vDIVW Margin value for the top and the bottom area of the Test Mask.
The measured vDIVW margin is denoted as vDIVW Margin upper and vDIVW Margin lower.

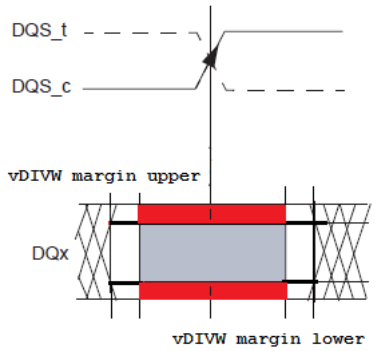


Figure 104 vDIVW Margin Upper and vDIVW Margin Lower

9 Find the minimum value between vDIVW Margin Upper and vDIVW Margin lower. Use this value as the worst voltage gap.

10 Calculate the worst margin (in percentage) using the equation:

$$\text{Margin (\%)} = [(\text{Worst\_voltage\_gap}) / (\text{Half of mask height})] \times 100\%$$

where, Worst_voltage_gap is the voltage gap between the mask and the eye at the top and bottom.

11 Report the worst voltage gap and the margin percentage as test results.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of vDIVW Margin for the test signal indicates if there is a violation in the mask region.

vDIVW

Mode Supported: DDR4, LPDDR4, LPDDR4X (Both Differential and Single-Ended)

Test ID: **DDR4 Test Mode**

120404 [vDIVW]

LPDDR4 Test Mode

150404 [vDIVW]

LPDDR4X (Differential) Test Mode

650404 [vDIVW]

LPDDR4X (Single-ended) Test Mode

750404 [vDIVW]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.6	Table 174	VdIVW [Rx Mask Voltage p-p]

NOTE For SDRAM type DDR4, this test appears under the **Select Tests** tab only when you set the **Test Mode** to **Custom** in the under **Set Up** tab of the Test Application.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.6	Table 222	VdIVW_total [Rx Mask Voltage p-p total]

NOTE For SDRAM type LPDDR4/LPDDR4X, this test appears under the **Select Tests** tab only when you set the **Test Mode** to **Custom** in the under **Set Up** tab of the Test Application.

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC Standard No. 42.6, Item 1847.17, 28 Nov 2017	2.1.8	Table 6	VdIVW_total [Rx Mask Voltage p-p total]

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify if there is any violation in the WRITE eye diagram with reference to the defined VdiVW parameter.

LPDDR4 / LPDDR4X Test Modes

The purpose of this test is to verify if there is any violation in the WRITE eye diagram with reference to the defined VdiVW_total parameter. Refer to Figure 188 of the JESD209-4D document.

Test Procedure: **DDR4 (for Test ID 120404)**

1 Calculate the initial time scale value based on selected speed grade options in the Compliance Test Application.

2 Calculate the number of sampling points based on the time scale value calculated in the previous step.

3 Check for valid DQS input test signals by verifying its frequency and amplitude values.

4 Set up the oscilloscope:

a Using UDF methodology, separate Write burst and return the filtered DQS signals as Recovered Clock, which is used for eye folding later.

b Set up measurement threshold values for the DQx channel and the DQSx channel input.

c Set up vertical scale values for DQx channel and DQSx channel input.

d Set the Color Grade Display option to ON.

e Set up Mask Test.

f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered DQS, Rise/Fall Edge

g Set the Real Time Eye on SDA to ON.

5 Perform Mask Testing:

a Set the Mask Test Run Until setting to 'Forever'.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

6 Determine and store the Vcent value.

There is an option to derive Vcent depending on the "Vcent Evaluation Mode" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "Widest eye opening level", the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

The detailed procedure for the "Widest eye opening level" requires that:

a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.

7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width of 0.2UI and a Test Mask height of 136mV.

8 Measure the minimum value of the eye diagram above the Test Mask. Denote it as vDIVW_top.

9 Measure the maximum value of the eye diagram below the Test Mask. Denote it as vDIVW_bottom.

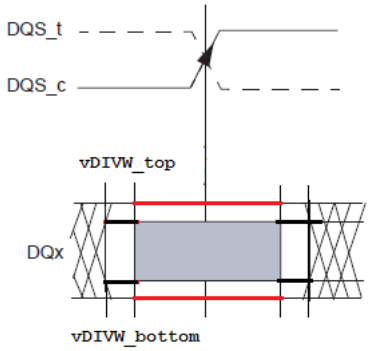


Figure 105 vDIVW_top and vDIVW_bottom

10 The difference between vDIVW_top and vDIVW_bottom is used as the final test result.

11 Report the vDIVW test result.

LPDDR4 (for Test ID 150404) / LPDDR4X (for Test IDs 650404 and 750404)

1 Calculate the initial time scale value based on selected speed grade options in the Compliance Test Application.

2 Calculate the number of sampling points based on the time scale value calculated in the previous step.

3 Check for valid DQS input test signals by verifying its frequency and amplitude values.

4 Set up the oscilloscope:

a Using UDF methodology, separate Write burst and return the filtered DQS signals as Recovered Clock, which is used for eye folding later.

b Set up measurement threshold values for the DQx channel and the DQSx channel input.

c Set up vertical scale values for DQx channel and DQSx channel input.

d Set the Color Grade Display option to ON.

e Set up Mask Test.

f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered DQS, Rise/Fall Edge

g Set the Real Time Eye on SDA to ON.

5 Perform Mask Testing:

a Set the Mask Test Run setting to ‘Forever’.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for ‘Total Waveforms’ exceeds the number of required waveforms specified in the configuration option ‘Total Waveform’.

6 Determine and store the Vcent value.

There is an option to derive Vcent depending on the “Vcent Evaluation Mode” configuration option in the Compliance Test Application.

If the “Vcent Evaluation Mode” configuration option is set to “User defined Vcent”, the value of Vcent follows the value of the “User Defined Vcent” configuration option in the Compliance Test Application.

If the “Vcent Evaluation Mode” configuration option is set to “Widest eye opening level”, the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

The detailed procedure for the “Widest eye opening level” requires that:

a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.

7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width and a Test Mask height, which uses the values of the following configuration options in the Compliance Test Application:

Test Mask Width = tDIVW configuration option

Test Mask Height = vDIVW (V) configuration option

8 Measure the minimum value of the eye diagram above the Test Mask. Denote it as vDIVW_top.

9 Measure the maximum value of the eye diagram below the Test Mask. Denote it as vDIVW_bottom.

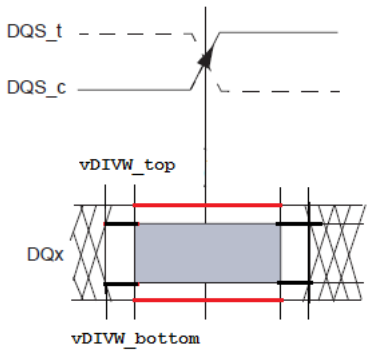


Figure 106 vDIVW_top and vDIVW_bottom

10 The difference between vDIVW_top and vDIVW_bottom is used as the final test result.

11 Report the vDIVW test result.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X Test Modes

The measured value of vDIVW for the test signal must be within the conformance limit as per the specification mentioned under the References section.

SRIN_diVW

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

20411 [SRIN_diVW]

LPDDR4 Test Mode

20409 [SRIN_diVW]

LPDDR4X (Differential) Test Mode

60409 [SRIN_diVW]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.6	Table 174	srr1, srf1 [Input Slew Rate over VdIVW]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.6	Table 222	SRIN_dIVW [Input Slew Rate over VdIVW_total]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the input slew rate over VdIVW Mask centered at Vcent_DQ. Refer to Figure 191 of the JESD209-4D document.

Test Procedure: **DDR4 (for Test ID 20411)**

1 Calculate initial time scale value based on selected DDR4 speed grade options.
2 Calculate number of sampling points according to the time scale value.
3 Check for valid DQS input test signals by verifying its frequency and amplitude values.
4 Set up the oscilloscope:
   a Using UDF methodology, separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.
   b Set up measurement threshold values for the DQx channel and the DQSx channel input.
   c Set up fix vertical scale values for DQx channel and DQSx channel input.
   d Turn ON Color Grade Display option.
   e Set up Mask Test settings.
   f Set up Clock Recovery settings on SDA.

   : Explicit clock, Source = filtered DQS, Rise/Fall Edge
   g Turn ON Real Time Eye on SDA.
5 Perform Mask Testing:
   a Set the Mask Test Run setting to ‘Forever’.
   b Load the mask file and start the Mask Test.
   c Stop the Mask Test when the counter for ‘Total Waveforms’ exceeds the number of required waveforms specified in the configuration option ‘Total Waveform’.

6 Determine and store the Vcent value.

There is an option to derive Vcent, which depends on the “Vcent Evaluation Mode” configuration option.

If the “Vcent Evaluation Mode” option is set to “User defined Vcent”, the value of Vcent follows the value of the “User Defined Vcent” configuration option.

If the “Vcent Evaluation Mode” option is set to “Widest eye opening level”, the application evaluates Vcent value from the level of widest eye opening on the generated eye diagram.

The detailed procedure for “Widest eye opening level” is:

a The Vcent level search ranges from 40% to 60% of the eye amplitude (eye height measured at the center of the eye diagram).

b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. The voltage level at the widest eye opening is used as Vcent.

7 Re-position the Test Mask so that it is centered on the Vcent value with a Test Mask width of 0.2UI and a Test Mask height of 136mV.

8 Acquire and split READ and WRITE bursts of the acquired signal.

9 Take the first valid WRITE burst found.

10 Measure the falling slew rate and rising slew rate of the WRITE DQ signal over VdiVW_Total window height at Vcent.

11 The worst value between the WorstRisingSlewRate and WorstFallingSlewRate will be used as the final test result for SRIN_dIVW.

12 The worst value between the WorstRisingSlewRate and WorstFallingSlewRate is used as the final test result for SRIN_dIVW.

LPDDR4 (for Test ID 20409) / LPDDR4X (Differential) (for Test ID 60409)

1 Calculate initial time scale value based on selected speed grade options.

2 Calculate number of sampling points according to the time scale value.

3 Check for valid DQS input test signals by verifying its frequency and amplitude values.

4 Set up the oscilloscope:

a Using UDF methodology, separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.

b Set up measurement threshold values for the DQx channel and the DQSx channel input.

c Set up fix vertical scale values for DQx channel and DQSx channel input.

d Turn ON Color Grade Display option.

e Set up Mask Test settings.

f Set up Clock Recovery settings on SDA.

: Explicit clock, Source = filtered DQS, Rise/Fall Edge

g Turn ON Real Time Eye on SDA.

5 Perform Mask Testing:

a Set the Mask Test Run setting to ‘Forever’.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for ‘Total Waveforms’ exceeds the number of required waveforms specified in the configuration option ‘Total Waveform’.

6 Determine and store the Vcent value.

There is an option to derive Vcent depending on the “Vcent Evaluation Mode” configuration option in the Compliance Test Application.

If the “Vcent Evaluation Mode” configuration option is set to “User defined Vcent”, the value of Vcent follows the value of the “User Defined Vcent” configuration option in the Compliance Test Application.

If the “Vcent Evaluation Mode” configuration option is set to “Widest eye opening level”, the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

The detailed procedure for the “Widest eye opening level” requires that:

a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.

7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width and a Test Mask height, which uses the values of the following configuration options in the Compliance Test Application:

Test Mask Width = tDIVW configuration option

Test Mask Height = vDIVW (V) configuration option

8 Acquire and split READ and WRITE burst of the acquired signal.

9 Take the first valid WRITE burst found.

10 Measure the falling slew rate and rising slew rate of the WRITE DQ signal over VdiVW_Total window height at Vcent.

11 The worst value between the WorstRisingSlewRate and WorstFallingSlewRate will be used as the final test result for SRIN_dIVW.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured SRIN_dIVW value for the test signal shall be within the conformance limit as per the JEDEC specifications mentioned under the References section.

tDIPW

Mode Supported: DDR4, LPDDR4, LPDDR4X (Both Differential and Single-Ended)

Test ID: **DDR4 Test Mode**

30305 [tDIPW]

LPDDR4 Test Mode

20410 [tDIPW]

LPDDR4X (Differential) Test Mode

60410 [tDIPW]

LPDDR4X (Single-ended) Test Mode

70410 [tDIPW]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.6	Table 174	TdIPW [DQ input pulse width]

LPDDR4 / LPDDR4X (Differential) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.6	Table 222	TdIPW DQ [Input pulse width (At Vcent_DQ)]

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC JC-42.6 TG426_1, 6 December 2017	1.0.0	-	TdIPW DQ [Input pulse width (At Vcent_DQ)]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X Test Modes**

The purpose of this test is to verify the minimum input pulse width defined at the Vcent_DQ. Refer to Figure 191 of the JESD209-4D document.

Test Procedure: **DDR4 (For Test ID 30305)**

1 This test requires the following pre-requisite test:

- tDIVW Margin (Test ID: 20403)

  Location for Vcent is determined and its value is stored.

2 Acquire and identify the READ and WRITE burst data of the acquired signal.

3 Use all valid WRITE bursts that are found to perform TDIPW measurement.

4 Find all valid rising and falling DQ edges, which are defined as the crossings at Vcent in the WRITE data burst.

5 Measure tDIPW as the time starting from a rising/falling edge of the DQ to the time ending at the following falling/rising edge.

6 Process all valid edges in the WRITE data burst.

7 Collect all tDIPW.

8 Determine the worst result from the set of tDIPW values measured and report it as the final test result.

LPDDR4 (for Test ID 20410) / LPDDR4X (for Test IDs 60410 and 70410)

1 This test requires the following pre-requisite test:

- tDIVW Margin (Test ID: 50403)

  Location for Vcent is determined and its value is stored.

2 Repeat steps 2 to 8 for Test ID 30305 (in DDR4 Test Mode) to determine the final test result for tDIPW.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X Test Modes

The measured value of tDIPW for the test signal shall be within the conformance limit as per the JEDEC specification.

tDQS2DQ

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

20415 [tDQS2DQ]

LPDDR4 Test Mode

20407 [tDQS2DQ]

LPDDR4X (Differential) Test Mode

60407 [tDQS2DQ]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.6	Table 174	tDQS2DQ [Rx mask DQS to DQ offset]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.6	Table 222	tDQS2DQ [Rx mask DQS to DQ offset]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the tDQS2DQ parameter.

NOTE To obtain a valid measurement result, this test requires a transitioning bit at the first valid bit in the DQ bus. Otherwise, this test uses the first opening in the eye diagram as the first transition bit, which may yield undesirable results.

Test Procedure: **DDR4 (for Test ID 20415) / LPDDR4 (for Test ID 20407) / LPDDR4X (Differential) (for Test ID 60407)**

1 Calculate initial time scale value based on the selected speed grade options.
2 Calculate number of sampling points according to the time scale value.
3 Check for valid DQS input test signals by verifying its frequency and amplitude values.
4 Set up the oscilloscope:
   a Using UDF methodology, separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.
   b Set up measurement threshold values for the DQ channel and the DQS channel input.
   c Set up vertical scale values for DQ channel and DQS channel input.
   d Turn ON Color Grade Display option.
   e Set up Mask Test settings.
   f Set up Clock Recovery on SDA.

   : Explicit clock, Source = filtered DQS, Rise Edge
   g Turn ON Real Time Eye on SDA.

5 Realign the eye opening of the first transition DQ bit to the center of the screen:
   a Increase the search range on the screen to the range specified in the 'First DQ Transition Search Range (ps)', so that the crossing point of the eye is visible on the screen.
   b Use the Histogram feature to find the first crossing point at 'VRefDQ' level horizontally across the screen.
   c Skip/pad the number of bit/bits by the value specified in the configuration option **Padding for First DQ Bit**.
   d Realign the center of the eye to the middle time position.

NOTE If the Compliance Test Application is unable to find any cross point within the search range, it prompts an error and this test run is canceled.

6 Perform Mask Testing:
   a Set the Mask Test Run setting to 'Forever'.
   b Load the mask file and start the Mask Test.
   c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
7 Determine and store the Vcent value.

   There is an option to derive Vcent, which depends on the "Vcent Evaluation Mode" configuration option.

   If the "Vcent Evaluation Mode" option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option.

   If the "Vcent Evaluation Mode" option is set to "Widest eye opening level", the application evaluates Vcent value from the level of widest eye opening on the generated eye diagram.

   The detailed procedure for "Widest eye opening level" is:
   a The Vcent level search ranges from 40% to 60% of the eye amplitude (eye height measured at the center of the eye diagram).
   b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. The voltage level at the widest eye opening is used as Vcent.
8 Use Histogram measurements to determine the center location of the eye diagram at Vcent level and denote it as EyeCenterLoc.
9 Determine the location of the filtered DQS rising edges used in the recovered clock and denote it as FilteredDQSLoc.
10 Compute the final test result using the equation:

$$tDQS2DQ = EyeCenterLoc - FilteredDQSLoc$$

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured tDQS2DQ value for the test signal shall be within the conformance limit as per the JEDEC specifications mentioned under the References section.

DQ VIHL(ac)

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

20416 [DQ VIHL(ac)]

LPDDR4 Test Mode

20408 [DQ VIHL(ac)]

LPDDR4X (Differential) Test Mode

60408 [DQ VIHL(ac)]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.6	Table 174	VIHL_AC [DQ AC input pulse amplitude pk-pk]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.6	Table 222	VIHL_AC [DQ AC input pulse amplitude pk-pk]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to verify the VIHL AC parameter, which is defined as the peak to peak voltage centered around Vcent_DQ such that the minimum value of (VIHL_AC / 2) is met both above and below Vcent_DQ. Refer to Figure 192 of the JESD209-4D document.

Test Procedure: **DDR4 (for Test ID 20416) / LPDDR4 (for Test ID 20408) / LPDDR4X (Differential) (for Test ID 60408)**

1 Calculate initial time scale value based on the selected speed grade options.
2 Calculate number of sampling points according to the time scale value.
3 Check for valid DQS input test signals by verifying its frequency and amplitude values.
4 Set up the oscilloscope:
   a Using UDF methodology, separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.
   b Set up measurement threshold values for the DQ channel and the DQS channel input.
   c Set up vertical scale values for DQ channel and DQS channel input.
   d Turn ON Color Grade Display option.
   e Set up Mask Test settings.
   f Set up Clock Recovery settings on SDA.

   : Explicit clock, Source = DQS, Rise/Fall Edge
   g Turn ON Real Time Eye on SDA.
5 Perform Mask Testing:
   a Set the Mask Test Run setting to 'Forever'.
   b Load the mask file and start the Mask Test.
   c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

6 Determine and store the Vcent value. Depending on the “Vcent Evaluation Mode” configuration, use one of the options to derive at Vcent value:

If the “Vcent Evaluation Mode” option is set to “User defined Vcent”, the value of Vcent follows the value of the “User Defined Vcent” configuration option.

If the “Vcent Evaluation Mode” option is set to “Widest eye opening level”, the application evaluates the VCent value based on the level of widest eye opening on the generated eye diagram. The detailed procedure for “Widest eye opening level” is:

a The Vcent level search ranges from 40% to 60% of the eye amplitude, which is the eye height measured at the center of the eye diagram.

b Scan for the widest eye opening within the search range specified above with a scan resolution of 5mV.
The voltage level at the widest eye opening is used as Vcent.

7 Determine the horizontal center location of the eye opening based on the measured Vcent.

8 Scan the top and bottom of the eye diagram from the location of 0.25 UI to 0.75 UI at an interval of 10ps to measure the peak to peak voltage centered around Vcent.

9 Denote the maximum value scanned for the top of the eye diagram as VIHLTop.

10 Denote the minimum value scanned for the bottom of the eye diagram as VIHLBot.

11 The minimum of VIHLTop and VILBot determines the final test result, VIHL((ac).

12 VIHL(ac) is compared with VIHL_AC, where peak to peak voltage is centered around Vcent_DQ(pin_mid) such that the minimum of VIHL_AC/2 must be met both above and below Vcent_DQ.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X Test Modes

The measured VIHL(ac) value for the test signal shall be within the conformance limit as per the JEDEC specifications.

srr2

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

20412 [srr2]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.6	Table 174	srr2 [Rising Input Slew Rate over 1/2 VIHL_AC]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the input slew rate over VdIVW Mask centered at Vcent_DQ. Refer to Figure 231 of the JESD79-4D document.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 (for Test ID 20412)**

1 This test requires the following pre-requisite test:

- vDIVW Margin (Test ID: 20404)

  Location for Vcent is determined and its value is stored.

2 Acquire and split the read and write burst of the acquired signal.

3 Take the first valid WRITE burst found.

4 Find all the rising edges on the upper DQ part in the specified burst.

  This edge starts at “VCENT+0.5*VdiVW” crossing and ends at the following “VCENT+0.5*VIHL_AC” crossing.

5 For all edges that have been identified, find the transition time, T_R.

  TR is the time starting at “VCENT+0.5*VdiVW” crossing and ending at the following “VCENT+0.5*VIHL_AC” crossing.

6 Calculate srr2 using the equation:

$$srr2 = [VIHL\_AC(min) - VdIVW(max)] / (2*T_R)$$

7 Determine the worst result from the set of srr2 measured.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results: **DDR4 Test Mode**

The measured srr2 value for the test signal shall be within the conformance limit as per the JEDEC specifications mentioned under the References section.

LPDDR4 / LPDDR4X Test Modes

Not available.

srf2

Test ID: **DDR4 Test Mode**

20413 [srf2]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.6	Table 174	srf2 [Falling Input Slew Rate over 1/2 VIHL_AC]

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to verify the input slew rate under VdIVW Mask centered at Vcent_DQ. Refer to Figure 232 of the JESD79-4D document.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 (for Test ID 20412)**

1 This test requires the following pre-requisite test:

- vDIVW Margin (Test ID: 20404)

  Location for Vcent is determined and its value is stored.

2 Acquire and split the read and write burst of the acquired signal.

3 Take the first valid WRITE burst found.

4 Find all the falling edges on the bottom DQ part in the specified burst.

  This edge starts at “VCENT-0.5*VdiVW” crossing and ends at the following “VCENT-0.5*VIHL_AC” crossing.

5 For all edges that have been identified, find the transition time, T_F.

  TF is the time starting at “VCENT-0.5*VdiVW” crossing and ending at the following “VCENT-0.5*VIHL_AC” crossing.

6 Calculate srf2 using the equation:

$$srf2 = [VIHL\_AC(min) - VdIVW(max)] / (2*T_F)$$

7 Determine the worst result from the set of srf2 measured.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results:

DDR4 Test Mode

The measured srf2 value for the test signal shall be within the conformance limit as per the JEDEC specifications mentioned under the References section.

LPDDR4 / LPDDR4X Test Modes

Not available.

tDQ2DQ

Mode Supported: DDR4, LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

20414 [tDQ2DQ]

LPDDR4 Test Mode

50405 [tDQ2DQ]

LPDDR4X (Differential) Test Mode

60405 [tDQ2DQ]

References: **DDR4 Test Mode**

Specifications document	Section#	Table#	Symbol [Parameter]
DDR4 SDRAM Specification, JESD79-4D, July 2021	13.6	Table 174	tDQ2DQ [DQ to DQ offset]

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.6	Table 222	tDQ2DQ [DQ to DQS offset]

Test Overview: **DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes**

The purpose of this test is to measure the DQ to DQ offset.

Test Procedure: **DDR4 (for Test ID 20414) / LPDDR4 (for Test ID 50405) / LPDDR4X (Differential) (for Test ID 60405)**

1 Calculate initial time scale value based on selected speed grade options.
2 Calculate number of sampling points according to the time scale value.
3 Check for valid DQS input test signals by verifying its frequency and amplitude values.
4 Connect DQ Lanes to scope channels as defined in the Configure tab of the Test Application. By default, “Data Source” parameter is set to ‘Channel 3’ for “Data Lane” set to ‘DQ0’; whereas, “Data Lane 2 Source” is set to ‘Channel 1’.

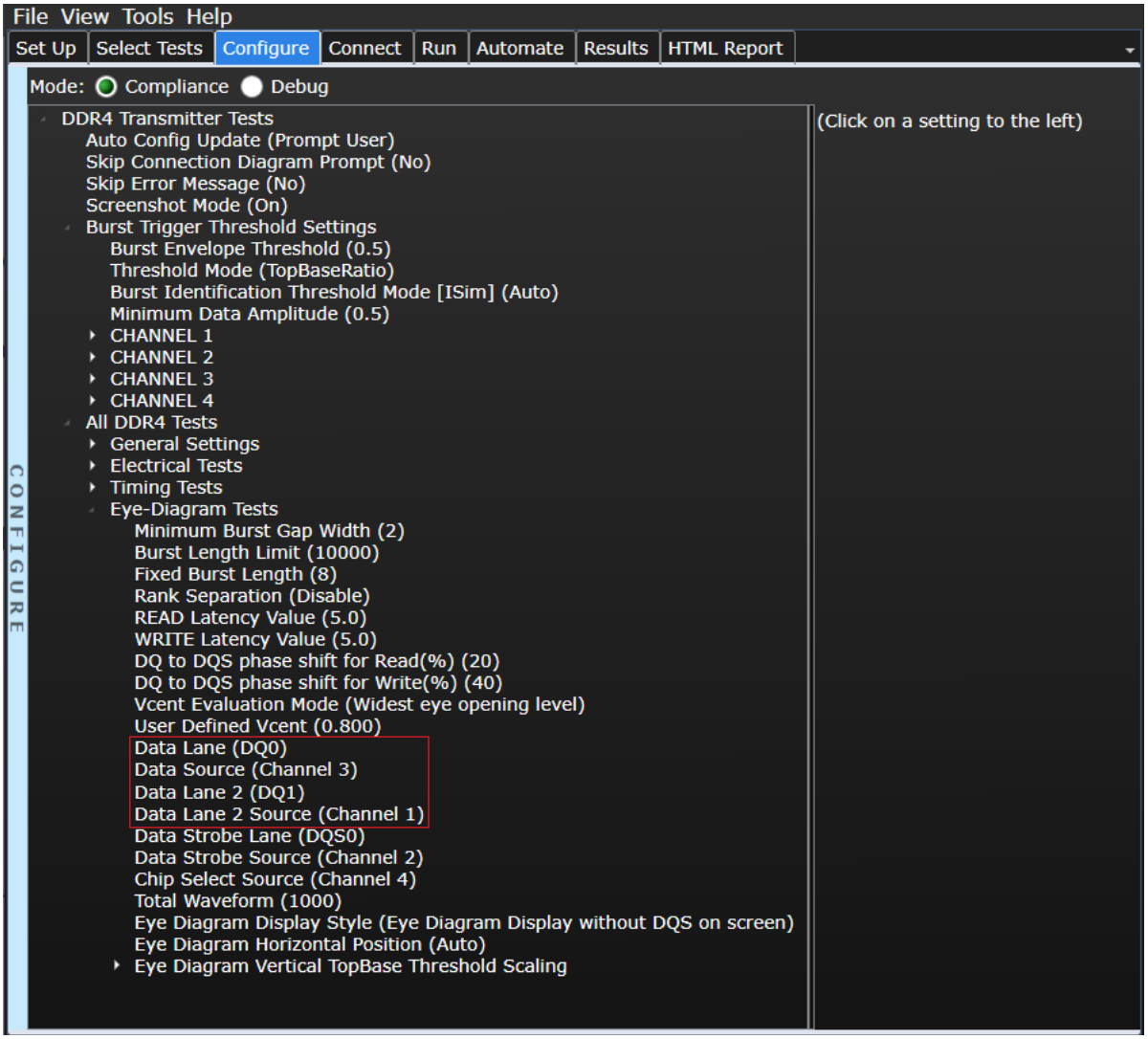


Figure 107 Default settings of Configure tab for tDQ2DQ

5 Set up the oscilloscope:

a Using UDF methodology, separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.

b Set up measurement threshold values for the DQ channels and the DQS channel input.

c Set up vertical scale values for DQ channels and DQS channel input.

d Turn ON Color Grade Display option.

e Set up Mask Test settings.

f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered DQS, Rise Edge

g Turn ON Real Time Eye on SDA.

6 Perform Mask Testing:
   a Set the Mask Test Run setting to 'Forever'.
   b Load the mask file and start the Mask Test.
   c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
7 Determine and store the Vcent value.

   There is an option to derive Vcent, which depends on the "Vcent Evaluation Mode" configuration option.

   If the "Vcent Evaluation Mode" option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option.

   If the "Vcent Evaluation Mode" option is set to "Widest eye opening level", the application evaluates Vcent value from the level of widest eye opening on the generated eye diagram.

   The detailed procedure for "Widest eye opening level" is:
   a The Vcent level search ranges from 40% to 60% of the eye amplitude (eye height measured at the center of the eye diagram).
   b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. The voltage level at the widest eye opening is used as Vcent.
8 Use Histogram measurements to determine the center location of the eye diagram at Vcent level and denote it as EyeCenterLoc1 (for Data Source 1) and EyeCenterLoc2 (for Data Source 2).
9 Position the scope marker (M1) at EyeCenterLoc1. Note the value as t_{M1}.
10 Position another marker (M2) at EyeCenterLoc2. Note the value as t_{M2}.
11 Measure tDQ2DQ as the difference of the two marker positions.

$$tDQ2DQ = t_{M1} - t_{M2}$$

12 Report the difference as the final value of tDQ2DQ.

Expected/ Observable Results:

DDR4 / LPDDR4 / LPDDR4X (Differential) Test Modes

The measured tDQ2DQ value for the test signal shall be within the conformance limit as per the JEDEC specifications mentioned under the References section.

Write_Eye_Width

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available

LPDDR4 Test Mode

52010 [Write_Eye_Width]

LPDDR4X (Differential) Test Mode

62010 [Write_Eye_Width]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Not available.

NOTE For SDRAM type LPDDR4/LPDDR4X, this test appears under the **Select Tests** tab only when you set the **Test Mode** to **Custom** in the under **Set Up** tab of the Test Application.

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to identify the Eye Width of the Write Cycle at Vcent.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 52010) / LPDDR4X (Differential) (for Test ID 62010)

1 Calculate the initial time scale value based on selected speed grade options in the Compliance Test Application.
2 Calculate the number of sampling points based on the time scale value calculated in the previous step.
3 Check for valid DQS input test signals by verifying its frequency and amplitude values.
4 Set up the oscilloscope:
   a Using UDF methodology, separate Write burst and return the filtered DQS signals as Recovered Clock, which is used for eye folding later.
   b Set up measurement threshold values for the DQx channel and the DQSx channel input.
   c Set up vertical scale values for DQx channel and DQSx channel input.
   d Set the Color Grade Display option to ON.
   e Set up Mask Test.
   f Set up Clock Recovery on SDA.

   : Explicit clock, Source = filtered DQS, Rise/Fall Edge
   g Set the Real Time Eye on SDA to ON.

5 Perform Mask Testing:

a Set the Mask Test Run setting to 'Forever'.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

6 Determine and store the Vcent value.

There is an option to derive Vcent depending on the "Vcent Evaluation Mode" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "Widest eye opening level", the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

The detailed procedure for the "Widest eye opening level" requires that:

a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.

7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width and a Test Mask height, which uses the values of the following configuration options in the Compliance Test Application:

Test Mask Width = tDIVW configuration option

Test Mask Height = vDIVW (V) configuration option

8 Use the Histogram feature in the Infiniium application to measure $t_{Write\_Eye\_Width\_Right}$ and $t_{Write\_Eye\_Width\_Left}$ values:

a Set Histogram X1=t_{Mask_Center}, X2=t_{Eye_Right}, Y1=Y2=Vcent

b $t_{Write\_Eye\_Width\_Right}$=value of HorizontalHistogramMin

c Set Histogram X1=t_{Eye_Left}, X2=t_{Mask_Center}, Y1=Y2=Vcent

d $t_{Write\_Eye\_Width\_Left}$=value of HorizontalHistogramMax

9 Calculate Write_Eye_Width using the equation:

$$Write\_Eye\_Width=t_{Write\_Eye\_Width\_Right}-t_{Write\_Eye\_Width\_Left}$$

10 Report the Write_Eye_Width measured.

Expected/ Observable Results:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of Write_Eye_Width for the test signal is considered as 'Information Only'.

Write_Eye_Height

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available

LPDDR4 Test Mode

52011 [Write_Eye_Height]

LPDDR4X (Differential) Test Mode

62011 [Write_Eye_Height]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Not available.

NOTE For SDRAM type LPDDR4/LPDDR4X, this test appears under the **Select Tests** tab only when you set the **Test Mode** to **Custom** in the under **Set Up** tab of the Test Application.

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to identify the Eye Height of the Write Cycle at Vcent.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 52011) / LPDDR4X (Differential) (for Test ID 62011)

1 Calculate the initial time scale value based on selected speed grade options in the Compliance Test Application.
2 Calculate the number of sampling points based on the time scale value calculated in the previous step.
3 Check for valid DQS input test signals by verifying its frequency and amplitude values.
4 Set up the oscilloscope:
   a Using UDF methodology, separate Write burst and return the filtered DQS signals as Recovered Clock, which is used for eye folding later.
   b Set up measurement threshold values for the DQx channel and the DQSx channel input.
   c Set up vertical scale values for DQx channel and DQSx channel input.
   d Set the Color Grade Display option to ON.
   e Set up Mask Test.
   f Set up Clock Recovery on SDA.

   : Explicit clock, Source = filtered DQS, Rise/Fall Edge
   g Set the Real Time Eye on SDA to ON.

5 Perform Mask Testing:
   a Set the Mask Test Run setting to 'Forever'.
   b Load the mask file and start the Mask Test.
   c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
6 Determine and store the Vcent value.

   There is an option to derive Vcent depending on the "Vcent Evaluation Mode" configuration option in the Compliance Test Application.

   If the "Vcent Evaluation Mode" configuration option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option in the Compliance Test Application.

   If the "Vcent Evaluation Mode" configuration option is set to "Widest eye opening level", the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

   The detailed procedure for the "Widest eye opening level" requires that:
   a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
   b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.
7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width and a Test Mask height, which uses the values of the following configuration options in the Compliance Test Application:

   Test Mask Width = tDIVW configuration option

   Test Mask Height = vDIVW (V) configuration option
8 Use the Histogram feature in the Infiniium application to measure $t_{Write\_Eye\_Height\_Top}$ and $t_{Write\_Eye\_Height\_Bottom}$ values:
   a Set Histogram X1=X2=t_{Eye_Pos}, Y1=Vcent, Y2=TopOfWindow
   b $t_{Write\_Eye\_Height\_Top}$=value of VerticalHistogramMin
   c Set Histogram X1=X2=t_{Eye_Pos}, Y1=BottomOfWindow, Y2=Vcent
   d $t_{Write\_Eye\_Height\_Bottom}$=value of VerticalHistogramMax
9 Calculate Write_Eye_Height using the equation:

$$Write\_Eye\_Height = t_{Write\_Eye\_Height\_Top} - t_{Write\_Eye\_Height\_Bottom}$$

10 Report the Write_Eye_Height measured.

Expected/ Observable Results:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of Write_Eye_Height for the test signal is considered as 'Information Only'.

Eye-Diagram for Data and Data Strobe (READ)

READ cycle tests

Eye Diagram Test for Read Cycle

Mode Supported: DDR4

Test ID: **DDR4 Test Mode**

20401 [Eye Diagram Test for Read Cycle]

LPDDR4 / LPDDR4X Test Modes

Not available.

References: **DDR4 Test Mode**

Not available.

NOTE For SDRAM type DDR4, this test appears under the **Select Tests** tab only when you set the **Test Mode** to **Custom** in the under **Set Up** tab of the Test Application.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Overview: **DDR4 Test Mode**

The purpose of this test is to generate an eye diagram for the READ cycle.

LPDDR4 / LPDDR4X Test Modes

Not available.

Test Procedure: **DDR4 (for Test ID 20401)**

1 Calculate initial time scale value based on selected DDR4 speed grade options.
2 Calculate number of sampling points according to the time scale value.
3 Check for valid DQS input test signals by verifying its frequency and amplitude values.
4 Set up the oscilloscope:
   a Using UDF methodology, separate Read burst and return the filtered DQS signals in the form of recovered clock for eye folding later.
   b Set up measurement threshold values for the DQ channel and the DQS channel input.
   c Set up vertical scale values for DQ channel and DQS channel input.
   d Set the Color Grade Display option to ON.
   e Set up Mask Test settings.
   f Set up Clock Recovery settings on SDA.

   : Explicit clock, Source = Filtered DQS, Rise/Fall Edge
   g Set Real Time Eye on SDA to ON.
5 Perform Eye Folding:
   a Set the Mask Test Run setting to ‘Forever’.
   b Load the mask file and start the Mask Test.
   c Stop the Mask Test when the counter for ‘Total Waveforms’ exceeds the number of required waveforms specified in the configuration option ‘Total Waveform’.

6 Once the count for required waveforms is reached, it marks the end of test.

LPDDR4 / LPDDR4X Test Modes

Not available.

Expected/ Observable Results:

DDR4 Test Mode

This test is reported as “Information Only”.

LPDDR4 / LPDDR4X Test Modes

Not available.

tQW_total_DBI

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

30506 [tQW_total_DBI]

LPDDR4X (Differential) Test Mode

60506 [tQW_total_DBI]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.5	Table 221	tQW_total_DBI [DQ output window time total, per pin (DBI-enabled)]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4/ LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the tQW_total_DBI parameter. Refer to Figure 187 of the JESD209-4D document.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 30506) / LPDDR4X (Differential) (for Test ID 60506)

1 Calculate initial time scale value based on the selected speed grade options.
2 Calculate number of sampling points according to the time scale value.
3 Check for valid DQS input test signals by verifying its frequency and amplitude values.
4 Set up the oscilloscope:
   a Using UDF methodology, separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.
   b Set up measurement threshold values for the DQ channel and the DQS channel input.
   c Set up vertical scale values for DQ channel and DQS channel input.
   d Turn ON Color Grade Display option.
   e Set up Mask Test settings.
   f Set up Clock Recovery settings on SDA.

   : Explicit clock, Source = filtered DQS, Rise/Fall Edge
   g Turn ON Real Time Eye on SDA.

5 Perform Mask Testing:

a Set the Mask Test Run setting to 'Forever'.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

6 Determine and store the Vcent value.

There is an option to derive Vcent depending on the "Vcent Evaluation Mode" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "Widest eye opening level", the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

The detailed procedure for the "Widest eye opening level" requires that:

a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.

7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width set to 1 UI width, which is based on the selected test data rate value. The Test Mask height is set to 0V.

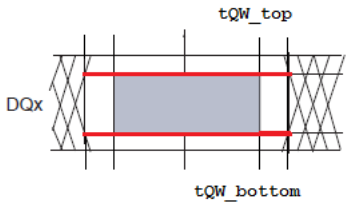


Figure 108 tCIVW values

8 Use the Histogram feature to measure the eye width at the top level (tQW_top) of the Test Mask and the eye width at the bottom level (tQW_bottom) of the Test Mask.

9 Find the minimum value between tQW_top and tQW_bottom.
Use this minimum value as the worst test result for the tQW_total_DBI measurement.

10 Report the worst test result.

Expected/ Observable Results:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured tQW_total_DBI value for the test signal shall be within the conformance limits as per the JEDEC specification.

tQW_total

Mode Supported: LPDDR4, LPDDR4X (Both Differential and Single-Ended)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

30505 [tQW_total]

LPDDR4X (Differential) Test Mode

60505 [tQW_total]

LPDDR4X (Single-ended) Test Mode

70505 [tQW_total]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.5	Table 221	tQW_total [DQ output window time total, per pin (DBI-disabled)]

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC JC-42.6-1847.17, 28 November 2017	2.1.8	Table 6	tQW_total [DQ output window time total, per pin (DBI-disabled)]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X Test Modes

The purpose of this test is to verify the tQW_total parameter. Refer to Figure 187 of the JESD209-4D document.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 30505) / LPDDR4X (for Test IDs 60505 and 70505)

1 Calculate initial time scale value based on the selected speed grade options.
2 Calculate number of sampling points according to the time scale value.
3 Check for valid DQS input test signals by verifying its frequency and amplitude values.

4 Set up the oscilloscope:
   a Using UDF methodology, separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.
   b Set up measurement threshold values for the DQ channel and the DQS channel input.
   c Set up vertical scale values for DQ channel and DQS channel input.
   d Turn ON Color Grade Display option.
   e Set up Mask Test settings.
   f Set up Clock Recovery settings on SDA.

   : Explicit clock, Source = filtered DQS, Rise/Fall Edge

   g Turn ON Real Time Eye on SDA.
5 Perform Mask Testing:
   a Set the Mask Test Run setting to 'Forever'.
   b Load the mask file and start the Mask Test.
   c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
6 Determine and store the Vcent value.

   There is an option to derive Vcent depending on the "Vcent Evaluation Mode" configuration option in the Compliance Test Application.

   If the "Vcent Evaluation Mode" configuration option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option in the Compliance Test Application.

   If the "Vcent Evaluation Mode" configuration option is set to "Widest eye opening level", the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

   The detailed procedure for the "Widest eye opening level" requires that:
   a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
   b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.
7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width set to 1UI width, which is based on the selected test data rate value. The Test Mask height is set to 0V.

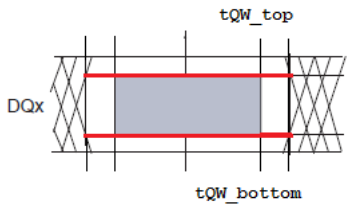


Figure 109 tCIVW values

8 Use the Histogram feature to measure the eye width at the top level (tQW_top) of the Test Mask and the eye width at the bottom level (tQW_bottom) of the Test Mask.
9 Find the minimum value between tQW_top and tQW_bottom.
   Use this minimum value as the worst test result for the tQW_total measurement.
10 Report the worst test result.

Expected/ Observable Results:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X Test Modes

The measured tQW_total value for the test signal shall be within the conformance limits as per the JEDEC specification.

Read_Eye_Width

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available

LPDDR4 Test Mode

52020 [Read_Eye_Width]

LPDDR4X (Differential) Test Mode

62020 [Read_Eye_Width]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Not available.

NOTE For SDRAM type LPDDR4/LPDDR4X, this test appears under the **Select Tests** tab only when you set the **Test Mode** to **Custom** in the under **Set Up** tab of the Test Application.

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to identify the Eye Width of the Read Cycle at Vcent.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 52020) / LPDDR4X (Differential) (for Test ID 62020)

1 Calculate the initial time scale value based on selected speed grade options in the Compliance Test Application.
2 Calculate the number of sampling points based on the time scale value calculated in the previous step.
3 Check for valid DQS input test signals by verifying its frequency and amplitude values.
4 Set up the oscilloscope:
   a Using UDF methodology, separate Read burst and return the filtered DQS signals as Recovered Clock, which is used for eye folding later.
   b Set up measurement threshold values for the DQx channel and the DQSx channel input.
   c Set up vertical scale values for DQx channel and DQSx channel input.
   d Set the Color Grade Display option to ON.
   e Set up Mask Test.
   f Set up Clock Recovery on SDA.

   : Explicit clock, Source = filtered DQS, Rise/Fall Edge
   g Set the Real Time Eye on SDA to ON.

5 Perform Mask Testing:
   a Set the Mask Test Run setting to 'Forever'.
   b Load the mask file and start the Mask Test.
   c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
6 Determine and store the Vcent value.

   There is an option to derive Vcent depending on the "Vcent Evaluation Mode" configuration option in the Compliance Test Application.

   If the "Vcent Evaluation Mode" configuration option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option in the Compliance Test Application.

   If the "Vcent Evaluation Mode" configuration option is set to "Widest eye opening level", the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

   The detailed procedure for the "Widest eye opening level" requires that:
   a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
   b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.
7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width and a Test Mask height, which uses the values of the following configuration options in the Compliance Test Application:

   Test Mask Width = tDIVW configuration option

   Test Mask Height = vDIVW (V) configuration option
8 Use the Histogram feature in the Infiniium application to measure $t_{Read\_Eye\_Width\_Right}$ and $t_{Read\_Eye\_Width\_Left}$ values:
   a Set Histogram X1=t_{Mask_Center}, X2=t_{Eye_Right}, Y1=Y2=Vcent
   b $t_{Read\_Eye\_Width\_Right}$=value of HorizontalHistogramMin
   c Set Histogram X1=t_{Eye_Left}, X2=t_{Mask_Center}, Y1=Y2=Vcent
   d $t_{Read\_Eye\_Width\_Left}$=value of HorizontalHistogramMax
9 Calculate Read_Eye_Width using the equation:

$$Read\_Eye\_Width=t_{Read\_Eye\_Width\_Right}-t_{Read\_Eye\_Width\_Left}$$

10 Report the Read_Eye_Width measured.

Expected/ Observable Results:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of Read_Eye_Width for the test signal is considered as 'Information Only'.

Read_Eye_Height

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available

LPDDR4 Test Mode

52021 [Read_Eye_Height]

LPDDR4X (Differential) Test Mode

62021 [Read_Eye_Height]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Not available.

NOTE For SDRAM type LPDDR4/LPDDR4X, this test appears under the **Select Tests** tab only when you set the **Test Mode** to **Custom** in the under **Set Up** tab of the Test Application.

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to identify the Eye Height of the Read Cycle at Vcent.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 52021) / LPDDR4X (Differential) (for Test ID 62021)

1 Calculate the initial time scale value based on selected speed grade options in the Compliance Test Application.
2 Calculate the number of sampling points based on the time scale value calculated in the previous step.
3 Check for valid DQS input test signals by verifying its frequency and amplitude values.
4 Set up the oscilloscope:
   a Using UDF methodology, separate Read burst and return the filtered DQS signals as Recovered Clock, which is used for eye folding later.
   b Set up measurement threshold values for the DQx channel and the DQSx channel input.
   c Set up vertical scale values for DQx channel and DQSx channel input.
   d Set the Color Grade Display option to ON.
   e Set up Mask Test.
   f Set up Clock Recovery on SDA.

   : Explicit clock, Source = filtered DQS, Rise/Fall Edge
   g Set the Real Time Eye on SDA to ON.

5 Perform Mask Testing:
   a Set the Mask Test Run setting to 'Forever'.
   b Load the mask file and start the Mask Test.
   c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
6 Determine and store the Vcent value.

   There is an option to derive Vcent depending on the "Vcent Evaluation Mode" configuration option in the Compliance Test Application.

   If the "Vcent Evaluation Mode" configuration option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option in the Compliance Test Application.

   If the "Vcent Evaluation Mode" configuration option is set to "Widest eye opening level", the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

   The detailed procedure for the "Widest eye opening level" requires that:
   a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
   b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.
7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width and a Test Mask height, which uses the values of the following configuration options in the Compliance Test Application:

   Test Mask Width = tDIVW configuration option

   Test Mask Height = vDIVW (V) configuration option
8 Use the Histogram feature in the Infiniium application to measure $t_{Read\_Eye\_Height\_Top}$ and $t_{Read\_Eye\_Height\_Bottom}$ values:
   a Set Histogram X1=X2=t_{Eye_Pos}, Y1=Vcent, Y2=TopOfWindow
   b $t_{Read\_Eye\_Height\_Top}$=value of VerticalHistogramMin
   c Set Histogram X1=X2=t_{Eye_Pos}, Y1=BottomOfWindow, Y2=Vcent
   d $t_{Read\_Eye\_Height\_Bottom}$=value of VerticalHistogramMax
9 Calculate Read_Eye_Height using the equation:

$$Read\_Eye\_Height=t_{Read\_Eye\_Height\_Top}-t_{Read\_Eye\_Height\_Bottom}$$

10 Report the Read_Eye_Height measured.

Expected/ Observable Results:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of Read_Eye_Height for the test signal is considered as 'Information Only'.

Eye-Diagram for Command Address

tCIVW Margin

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

30400 [tCIVW Margin]

LPDDR4X (Differential) Test Mode

630401 [tCIVW Margin]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.4	Table 220	TcIVW [Rx timing window]

NOTE This test does not measure the TcIVW parameter directly (which is, otherwise, documented in the LPDDR4 JESD209-4D specifications). The measurement result is reported as “Failed” if the eye diagram violates the defined mask. This test is customized based on user inputs during the LPDDR4 application development initially.

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to measure the minimum tCIVW Margin of the CA eye diagram.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 30400) / LPDDR4X (Differential) (for Test ID 630401)

1 Calculate the value of the initial time scale based on the selected speed grade options.
2 Calculate the number of sampling points according to the time scale value.
3 Check for valid Clock and CA input test signals by verifying its frequency and amplitude values.

4 On the Oscilloscope:
   a Trigger on the Clock signal with the Falling Edge condition.
   b Set the Sampling Rate of the Oscilloscope to the maximum value and set the Sampling Points to the user defined 'Sampling Points (Pts) for Eye Diagram Tests Only'.
   c Set Function 1 to duplicate the Clock signal.
   d Set the Color Grade Display option to ON.
   e Set up Mask Test settings.
   f Set up Clock Recovery settings on SDA.

   : Explicit clock, Source = Function 1, Rising Edge
   g Set the Real Time Eye on SDA to ON.
   h Set up measurement threshold values for Function 1 and CA input signals.
   i Change trigger source to 'CA input signal' on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CA bus.
5 Perform Mask Testing:
   a Set the Mask Test Run setting to 'Forever'.
   b Load the mask file and start the Mask Test.
   c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total CA Waveform'.
6 Determine and store the Vcent value.

   There is an option to derive Vcent depending on the "Vcent Evaluation Mode" configuration option in the Compliance Test Application.

   If the "Vcent Evaluation Mode" configuration option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option in the Compliance Test Application.

   If the "Vcent Evaluation Mode" configuration option is set to "Widest eye opening level", the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

   The detailed procedure for the "Widest eye opening level" requires that:
   a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
   b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.
7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width and a Test Mask height. Test Mask width is a user-defined value of 'tCIVW' and Test Mask height is a user-defined value of 'vCIVW(V)', configured in the Compliance Test Application.
8 Use the Histogram feature in the Infiniium application to measure the tCIVW Margin value on all the four corners of the Test Mask.
   The tCIVW Margin for each Test Mask corner is denoted as tCIVW_m1, tCIVW_m2, tCIVW_m3 and tCIVW_m4.

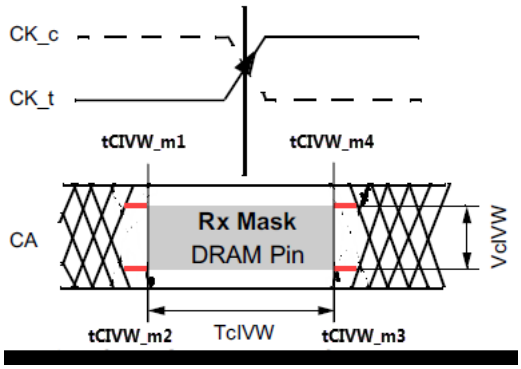
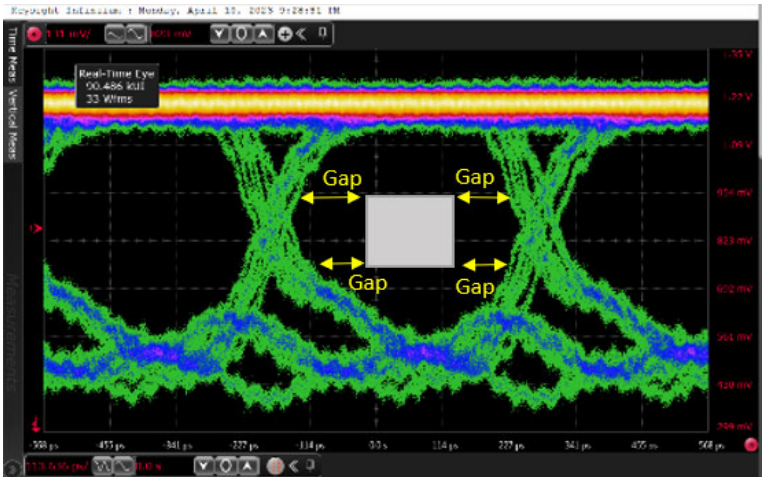


Figure 110 tCIVW values

9 Calculate the margin (in percentage) using the equation:

Margin (%) = [(Time - Half of mask width) / (Half of mask width)] x 100%

where, “Time - Half of mask width” is the gap between the mask corner and the left or right of the eye (as shown in the below reference image).



10 Find the minimum value between tCIVW_m1, tCIVW_m2, tCIVW_m3 and tCIVW_m4. Use the minimum value as the worst test result.

11 Report the worst test result.

Expected/ Observable Results:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of tCIVW Margin for the test signal must be greater than 0% to indicate that there is no mask violation.

tCIVW

Mode Supported: LPDDR4, LPDDR4X (Both Differential and Single-Ended)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

130400 [tCIVW]

LPDDR4X (Differential) Test Mode

630400 [tCIVW]

LPDDR4X (Single-ended) Test Mode

730400 [tCIVW]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.4	Table 220	TcIVW [Rx timing window]

NOTE For SDRAM type LPDDR4/LPDDR4X, this test appears under the **Select Tests** tab only when you set the **Test Mode** to **Custom** in the under **Set Up** tab of the Test Application.

LPDDR4X (Single-ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC JC-42.6-1847.17, 28 November 2017	2.1.8	Table 6	TcIVW [Rx timing window]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X Test Mode

The purpose of this test is to measure the minimum tCIVW of the CA eye diagram generated.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 130400) / LPDDR4X (for Test IDs 630400 and 730400)

1 Calculate the value of the initial time scale based on the selected speed grade options.
2 Calculate the number of sampling points according to the time scale value.

3 Check for valid Clock and CA input test signals by verifying its frequency and amplitude values.

4 On the Oscilloscope:

a Trigger on the Clock signal with the Falling Edge condition.

b Set the Sampling Rate of the Oscilloscope to the maximum value and set the Sampling Points to the user defined 'Sampling Points (Pts) for Eye Diagram Tests Only'.

c Set Function 1 to duplicate the Clock signal.

d Set the Color Grade Display option to ON.

e Set up Mask Test settings.

f Set up Clock Recovery settings on SDA.

: Explicit clock, Source = Function 1, Rising Edge

g Set the Real Time Eye on SDA to ON.

h Set up measurement threshold values for Function 1 and CA input signals.

i Change trigger source to 'CA input signal' on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CA bus.

5 Perform Mask Testing:

a Set the Mask Test Run setting to 'Forever'.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total CA Waveform'.

6 Determine and store the Vcent value.

There is an option to derive Vcent depending on the "Vcent Evaluation Mode" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "Widest eye opening level", the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

The detailed procedure for the "Widest eye opening level" requires that:

a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.

7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width and a Test Mask height. Test Mask width is a user-defined value of 'tCIVW' and Test Mask height is a user-defined value of 'vCIVW(V)', configured in the Compliance Test Application.

8 Measure the eye width at the top level of the Test Mask (tCIVW_Top) and the eye width at the bottom level of the Test mask (tCIVW_Bottom).

Refer to Figure 183 of the JESD209-4D document.

9 Find the minimum value between tCIVW_Top and tCIVW_Bottom.
Use the minimum value as the worst test result.

10 Report the worst test result.

Expected/ Observable Results:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X Test Modes

The measured value of tCIVW for the test signal shall be within the conformance limit as per the JEDEC specification mentioned under the References section.

vCIVW Margin

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

30402 [vCIVW Margin]

LPDDR4X (Differential) Test Mode

60402 [vCIVW Margin]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.4	Table 220	VcIVW [Rx Mask Voltage p-p]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify if there is any violation in the CA eye diagram with reference to the defined vCIVW parameter. Refer to Figure 181 of the JESD209-4D document.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 30402) / LPDDR4X (Differential) (for Test ID 60402)

1 Calculate the value of the initial time scale based on the selected speed grade options.
2 Calculate the number of sampling points according to the time scale value.
3 Check for valid Clock and CA input test signals by verifying its frequency and amplitude values.
4 On the Oscilloscope:
   a Trigger on the Clock signal with the Falling Edge condition.
   b Set the Sampling Rate of the Oscilloscope to the maximum value and set the Sampling Points to the user defined 'Sampling Points (Pts) for Eye Diagram Tests Only'.
   c Set Function 1 to duplicate the Clock signal.
   d Set the Color Grade Display option to ON.
   e Set up Mask Test settings.
   f Set up Clock Recovery settings on SDA.

   : Explicit clock, Source = Function 1, Rising Edge
   g Set the Real Time Eye on SDA to ON.
   h Set up measurement threshold values for Function 1 and CA input signals.
   i Change trigger source to 'CA input signal' on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CA bus.

5 Perform Mask Testing:

a Set the Mask Test Run Until setting to ‘Forever’.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for ‘Total Waveforms’ exceeds the number of required waveforms specified in the configuration option ‘Total CA Waveform’.

6 Determine and store the Vcent value.

There is an option to derive Vcent depending on the “Vcent Evaluation Mode” configuration option in the Compliance Test Application.

If the “Vcent Evaluation Mode” configuration option is set to “User defined Vcent”, the value of Vcent follows the value of the “User Defined Vcent” configuration option in the Compliance Test Application.

If the “Vcent Evaluation Mode” configuration option is set to “Widest eye opening level”, the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

The detailed procedure for the “Widest eye opening level” requires that:

a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.

7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width and a Test Mask height. Test Mask width is a user-defined value of ‘tCIVW’ and Test Mask height is a user-defined value of ‘vCIVW (V)’, configured in the Compliance Test Application.

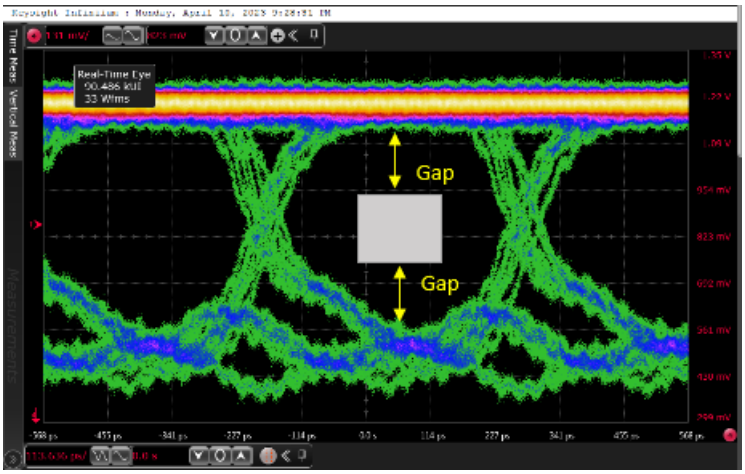
8 Measure the vCIVW margin value for the top and bottom area of the Test Mask using the Histogram feature in the Infiniium application. The vCIVW margin measured are denoted as vCIVW margin upper and vCIVW margin lower.

Refer to Figure 183 of the JESD209-4D document.

9 Calculate the margin (in percentage) using the equation:

$$\text{Margin (\%)} = [(\text{Voltage} - \text{Half of mask height}) / (\text{Half of mask height})] \times 100\%$$

where, “Voltage - Half of mask height” is the gap between the mask Top/Bottom and the eye at the Top/Bottom (as shown in the below reference image).



10 Find the minimum value between vCIVW margin upper and vCIVW margin lower and that will be used as the worst test result.

11 Report the worst test result.

Expected/ Observable Results:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of vCIVW Margin for the test signal shall be within the conformance limit as per the JEDEC specification mentioned under the References section.

vCIVW

Mode Supported: LPDDR4, LPDDR4X (Both Differential and Single-Ended)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

130402 [vCIVW]

LPDDR4X (Differential) Test Mode

630402 [vCIVW]

LPDDR4X (Single-ended) Test Mode

730402 [vCIVW]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.4	Table 220	VcIVW [Rx Mask Voltage p-p]

NOTE For SDRAM type LPDDR4/LPDDR4X, this test appears under the **Select Tests** tab only when you set the **Test Mode** to **Custom** in the under **Set Up** tab of the Test Application.

LPDDR4X (Single-ended) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC JC-42.6-1847.17, 28 November 2017	2.1.8	Table 6	VcIVW [Rx Mask Voltage p-p]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X Test Modes

The purpose of this test is to verify if there is any violation in the CA eye diagram with reference to the defined vCIVW parameter. Refer to Figure 181 of the JESD209-4D document.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 130402) / LPDDR4X (for Test IDs 630402 and 730402)

1 Calculate the value of the initial time scale based on the selected speed grade options.
2 Calculate the number of sampling points according to the time scale value.

3 Check for valid Clock and CA input test signals by verifying its frequency and amplitude values.

4 On the Oscilloscope:

a Trigger on the Clock signal with the Falling Edge condition.

b Set the Sampling Rate of the Oscilloscope to the maximum value and set the Sampling Points to the user defined 'Sampling Points (Pts) for Eye Diagram Tests Only'.

c Set Function 1 to duplicate the Clock signal.

d Set the Color Grade Display option to ON.

e Set up Mask Test settings.

f Set up Clock Recovery settings on SDA.

: Explicit clock, Source = Function 1, Rising Edge

g Set the Real Time Eye on SDA to ON.

h Set up measurement threshold values for Function 1 and CA input signals.

i Change trigger source to 'CA input signal' on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CA bus.

5 Perform Mask Testing:

a Set the Mask Test Run setting to 'Forever'.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total CA Waveform'.

6 Determine and store the Vcent value.

There is an option to derive Vcent depending on the "Vcent Evaluation Mode" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "Widest eye opening level", the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

The detailed procedure for the "Widest eye opening level" requires that:

a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.

7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width and a Test Mask height. Test Mask width is a user-defined value of 'tCIVW' and Test Mask height is a user-defined value of 'vCIVW (V)', configured in the Compliance Test Application.

8 Measure the minimum value of the eye diagram above the Test Mask and denote it as vCIVW_Top.

9 Measure the minimum value of the eye diagram below the Test Mask and denote it as vCIVW_Bottom.

10 Use the difference between vCIVW_Top and vCIVW_Bottom as the final test result.

11 Report the vCIVW test result.

Expected/ Observable Results:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X Test Modes

The measured value of vCIVW for the test signal shall be within the conformance limit as per the JEDEC specification mentioned under the References section.

CA VIHL(ac)

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

30403 [CA VIHL(ac)]

LPDDR4X (Differential) Test Mode

630403 [CA VIHL(ac)]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.4	Table 220	VIHL_AC [CA AC input pulse amplitude pk-pk]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the VIHL AC parameter, which is defined as the peak to peak voltage centered around Vcent_CA, such that the minimum value of (VIHL_AC / 2) is met both above and below Vcent_CA. Refer to Figure 185 of the JESD209-4D document.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 30403) / LPDDR4X (Differential) (for Test ID 630403)

1 Calculate the value of the initial time scale based on the selected speed grade options.
2 Calculate the number of sampling points according to the time scale value.
3 Check for valid Clock and CA input test signals by verifying its frequency and amplitude values.
4 On the Oscilloscope:
   a Trigger on the Clock signal with the Falling Edge condition.
   b Set the Sampling Rate of the Oscilloscope to the maximum value and set the Sampling Points to the user defined 'Sampling Points (Pts) for Eye Diagram Tests Only'.
   c Set Function 1 to duplicate the Clock signal.
   d Set the Color Grade Display option to ON.
   e Set up Mask Test settings.
   f Set up Clock Recovery settings on SDA.

: Explicit clock, Source = Function 1, Rising Edge

g Set the Real Time Eye on SDA to ON.

h Set up measurement threshold values for Function 1 and CA input signals.

i Change trigger source to 'CA input signal' on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CA bus.

5 Perform Mask Testing:

a Set the Mask Test Run setting to 'Forever'.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total CA Waveform'.

6 Determine and store the Vcent value.

There is an option to derive Vcent depending on the "Vcent Evaluation Mode" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option in the Compliance Test Application.

If the "Vcent Evaluation Mode" configuration option is set to "Widest eye opening level", the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

The detailed procedure for the "Widest eye opening level" requires that:

a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.

7 Reposition the Test Mask so that it is centered on the Vcent value with a Test Mask width and a Test Mask height. Test Mask width is a user-defined value of 'tCIVW' and Test Mask height is a user-defined value of 'vCIVW(V)', configured in the Compliance Test Application.

8 The peak to peak voltage centered around Vcent is measured by scanning the top and bottom of the eye diagram from the point of 0 UI to 1 UI at an interval of 10ps.

9 The minimum value scanned for the top of the eye diagram is denoted as VIHLTop and the maximum value scanned for the bottom of the eye diagram is denoted as VIHLBot.

10 Use the difference between VIHLTop and VIHLBot as the final test result VIHL(ac).

Expected/ Observable Results:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of VIHL(ac) for the test signal shall be within the conformance limit as per the JEDEC specification mentioned under the References section.

SRIN_ciVW

Mode Supported: LPDDR4, LPDDR4X (Differential only)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

130404 [SRIN_ciVW]

LPDDR4X (Differential) Test Mode

630404 [SRIN_ciVW]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.4	Table 220	SRIN_cIVW [Input Slew Rate over VcIVW]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The purpose of this test is to verify the input slew rate over VcIVW Mask centered at Vcent_CA. Refer to Figure 184 of the JESD209-4D document for the definition of SRIN_ciVW.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (for Test ID 130404) / LPDDR4X (Differential) (for Test ID 630404)

1 Calculate the value of the initial time scale based on the selected speed grade options.
2 Calculate the number of sampling points according to the time scale value.
3 Check for valid Clock and CA input test signals by verifying its frequency and amplitude values.
4 On the Oscilloscope:
   a Trigger on the Clock signal with the Falling Edge condition.
   b Set the Sampling Rate of the Oscilloscope to the maximum value and set the Sampling Points to the user defined 'Sampling Points (Pts) for Eye Diagram Tests Only'.
   c Set Function 1 to duplicate the Clock signal.
   d Set the Color Grade Display option to ON.
   e Set up Mask Test settings.
   f Set up Clock Recovery settings on SDA.

   : Explicit clock, Source = Function 1, Rising Edge
   g Set the Real Time Eye on SDA to ON.
   h Set up measurement threshold values for Function 1 and CA input signals.
   i Change trigger source to 'CA input signal' on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CA bus.

5 Perform Mask Testing:
   a Set the Mask Test Run Until setting to 'Forever'.
   b Load the mask file and start the Mask Test.
   c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total CA Waveform'.
6 Determine and store the Vcent value.

   There is an option to derive Vcent depending on the "Vcent Evaluation Mode" configuration option in the Compliance Test Application.

   If the "Vcent Evaluation Mode" configuration option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option in the Compliance Test Application.

   If the "Vcent Evaluation Mode" configuration option is set to "Widest eye opening level", the Compliance Application evaluates the Vcent value based on the level of widest eye opening on the generated eye diagram.

   The detailed procedure for the "Widest eye opening level" requires that:
   a The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
   b Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. Use the voltage level at the widest eye opening as the value for Vcent.
7 Set the measurement thresholds - Upper, Middle, Lower to Mask Top Voltage, Vcent and Mask Bottom Voltage, respectively.
8 Set up Slew Rate Rising measurement on the CA signal to achieve the SRIN_ciVW Rise Time Maximum and SRIN_ciVW Rise Time Minimum. The worst value between maximum and minimum values obtained is set to WorstRisingSlewRate.
9 Set up Slew Rate Falling measurement on the DQ signal to achieve the SRIN_ciVW Fall Time Maximum and SRIN_ciVW Fall Time Minimum. The worst value between maximum and minimum values obtained is set to WorstFallingSlewRate.
10 The worst value between the WorstRisingSlewRate and WorstFallingSlewRate will be used as the final test result for SRIN_cIVW.

Expected/ Observable Results:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

The measured value of SRIN_cIVW for the test signal shall be within the conformance limit as per the JEDEC specification mentioned under the References section.

tCIPW

Mode Supported: LPDDR4, LPDDR4X (Both Differential and Single-Ended)

Test ID: **DDR4 Test Mode**

Not available.

LPDDR4 Test Mode

30401 [tCIPW]

LPDDR4X (Differential) Test Mode

60401 [tCIPW]

LPDDR4X (Single-ended) Test Mode

70401 [tCIPW]

References: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X (Differential) Test Modes

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JESD209-4D, June 2021	10.4	Table 220	TcIPW [CA Input pulse width]

LPDDR4X (Single-Ended) Test Mode

Specifications document	Section#	Table#	Symbol [Parameter]
LPDDR4 SDRAM Specification, JEDEC JC-42.6 TG426_1, 6 December 2017	1.0.0	-	TcIPW [CA Input pulse width]

Test Overview: **DDR4 Test Mode**

Not available.

LPDDR4 / LPDDR4X Test Modes

The purpose of this test is to verify the minimum input pulse width defined at Vcent_CA. Refer to Figure 184 of the JESD209-4D document.TCIPW rising and falling edges.

Test Procedure: **DDR4 Test Mode**

Not available.

LPDDR4 (For Test ID 30401) / LPDDR4X (For Test IDs 60401 and 70401)

1 This test requires the following pre-requisite test:

- tCIVW Margin (Test ID: 30400): The location of Vcent_CA is determined and the its value is stored.

2 Perform the pulse width on the CA signal:
   a Set to ON the positive pulse width measurement and jitter statistics to measure all the edges.
   b Set the measurement threshold to a hysteresis of +/- 150mV at the threshold level of Vcent_CA.
   c Obtain the minimum result from the measurements as the worst positive pulse width.
   d Repeat steps a to c for negative pulse width and store the minimum result from the measurement as the worst negative pulse width.
3 Compare the minimum values from the positive and negative pulse width results.
   Convert the unit for the values from seconds to UI.
   Report the resulting value as the final test result.

Expected/ Observable Results:

DDR4 Test Mode

Not available.

LPDDR4 / LPDDR4X Test Modes

The measured tCIPW value for the test signal shall be within the conformance limit as per the JEDEC specification.

A References

Documents

- Infiniium Oscilloscope Operation Manual
- Infiniium Oscilloscopes Programmer's Guide
- JESD79-4D Specification, July 2021
- JESD209-4D Specification, June 2021
- JESD209-4 -1 Specification, January 2017
- JEDEC JC-42.6-1847.17, November 2017
- JEDEC JC-42.6 TG426_1, December 2017

Typical DDR4 Signals Reference

- Section 2.8 of the JESD79-4D document for DDR4 SDRAM Addressing

Typical LPDDR4 Signals Reference

- Section 3.1 of the JESD209-4D document for the available Pin-Out/Signals on LPDDR4 DIMM

Reference Figures from JESD79-4D Document

- Figure 83 for READ timing definition
- Figure 84 for Clock to Data Strobe relationship
- Figure 88 for the method for calculating tRPRE transitions and endpoints
- Figure 89 for the method for calculating tRPST transitions and endpoints
- Figure 124 for the Write timing definition and parameters with 1tCK Preamble
- Figure 125 for the Write timing definition and parameters with 2tCK Preamble
- Figure 126 for the method for calculating tWPRE transitions and endpoints
- Figure 127 for the method for calculating tWPST transitions and endpoints
- Figure 212 for the Vix definition (CK)
- Figure 216 for the Vix definition (DQS)
- Figure 221 for the Single-ended output slew rate definition
- Figure 207 for the Address, Command and Control overshoot and undershoot definition
- Figure 209 for the Data, Strobe and Mask overshoot and undershoot definition

Reference Figures from JESD209-4D Document

- Figure 17 for Read Timing
- Figure 20 for tLZ(DQ) method for calculating transitions and end point
- Figure 21 for tHZ(DQ) method for calculating transitions and end point
- Figure 22 for Method for calculating tRPRE transitions and endpoints
- Figure 23 for Method for calculating tRPRE transitions and endpoints
- Figure 24 for Method for calculating tRPST transitions and endpoints
- Figure 29 for Write Timing
- Figure 168 for Vix Definition (Clock)
- Figure 173 for Vix Definition (DQS)
- Figure 174 for Single Ended Output Slew Rate Definition
- Figure 175 for Differential Output Slew Rate Definition
- Figure 176 for the Overshoot and Undershoot Definition

NOTE All references other than from the JESD209-4D document that correspond to LPDDR4 are applicable for LPDDR4X also.

Index

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January 2024
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