Agilent Logic Analyzer

Online Help

Agilent Technologies

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Using the Agilent Logic Analyzer

The *Agilent Logic Analyzer* application is used on 16900-series logic analysis systems (see page 561), 16800-series logic analyzers (see page 558), and 1680/1690-series logic analyzers (see page 552). It can also be used by itself on a Windows XP/2000 computer for *remote access* (see page 63) of 16900- or 1680/1690-series logic analyzers on the network, or for *offline analysis* (see page 197) of data captured on 16900-, 1680/1690-, or 16700-series logic analyzers.

- Comparing Captured Data to Reference Data (see page 268)
- Viewing Source Code Associated with Captured Data (see page 272)
- Analyzing Packet Data (see page 280)
- Analyzing the Same Data in Different Ways (Using the Overview Window) (see page 297)
- Setting the System Trigger and Skew Between Modules (see page 303)
- Using Display Windows (see page 305)
- Printing Captured Data (see page 306)
- Extending Data Visualization/Analysis with VBA (see page 309)

- "**Using Tools**" (in the online help)
- "**External Oscilloscope Time Correlation and Data Display**" (in the online help)
- "**Using the Pattern Generator**" (in the online help)
- **Managing Software Licenses** (see page 311)
- **Updating Software** (see page 319)
- **Solving Problems** (see page 321)
- **Concepts** (see page 363)
- **Reference** (see page 403)
- **Glossary** (see page 647)
- "**COM Automation**" (in the online help)
- "**XML Format**" (in the online help)

See Also

- "*16900-Series Logic Analysis System Installation Guide*"
- "*16800-Series Logic Analyzers Installation/Quick Start Guide*"
- "*1680-Series Logic Analyzers Quick Start/Installation Guide*"
- "*1690-Series Logic Analyzers Quick Start/Installation Guide*"

Contents

6 Capturing Data from the Device Under Test

7 Analyzing the Captured Data

1
What's New

In this release, version 03.67, of the *Agilent Logic Analyzer* application:

- The new Add or Remove Agilent Logic Analyzer Software tool helps you manage your logic analyzer software and keep it up to date. See Updating Software (see page 319).
- The "Xilinx FPGA Dynamic Probe" (in the online help) now supports connecting to JTAG cables on remote PCs or logic analysis systems. Also, Spartan-3 FPGAs are now supported.
- The pattern generator has been enhanced to: let you find instructions or vectors in the sequence, let you use macro, loop, and comment instructions when importing vectors from CSV format files (exporting to CSV format files still gives compiled sequences), and let you change the colors associated with instructions and macros. See "Using the Pattern Generator" (in the online help).
- The Add External Oscilloscope wizard now sets up an external oscilloscope module that can import digital channel data from mixed-signal oscilloscopes as well as analog channel data. Also, external oscilloscope modules can now be correlated with split logic analyzer modules. See "External Oscilloscope Time Correlation and Data Display" (in the online help).
- The external protocol analyzer correlation software now supports the N5319A interconnect cable that provides more flexible cross-triggering (via flags). See "External Protocol Analyzer Time Correlation" (in the online help).
- The Status dialog now shows more information in the columns of the display and lets you choose which columns are displayed. See Status Dialog (see page 490).
- There is now a oscilloscope data format (.bin) to logic analyzer format (.alb) converter. When converted to .alb format, oscilloscope data can be imported and viewed in the *Agilent Logic Analyzer* application. To run the converter, choose **Start>All Programs>Agilent Logic Analyzer>Utilities>Scope BIN to ALB Translator** from the Windows Start menu.

See Also

- Version 03.65 What's New (see page 21)
- Version 03.60 What's New (see page 22)
- Version 03.55 What's New (see page 23)

- Version 03.50 What's New (see page 24)
- Version 03.30 What's New (see page 26)
- Version 03.20 What's New (see page 28)
- Version 03.00 What's New (see page 29)
- Version 02.50 What's New (see page 30)
- Version 02.00 What's New (see page 31)
- Version 01.40 What's New (see page 32)
- Version 01.20 What's New (see page 34)
- Version 01.10 What's New (see page 35)

Version 03.65 What's New

In version 03.65 of the *Agilent Logic Analyzer* application:

- The new 16951B logic analyzer card was supported in the 16900-series logic analysis system. See 16950/51 Logic Analyzer Notes (see page 593).
- The new "Protocol Development Kit (PDK)" (in the online help) lets you edit and create protocol description files in order to decode, display, and trigger on customized packet data.

See Also

- Version 03.60 What's New (see page 22)
- Version 03.55 What's New (see page 23)
- Version 03.50 What's New (see page 24)
- Version 03.30 What's New (see page 26)
- Version 03.20 What's New (see page 28)
- Version 03.00 What's New (see page 29)
- Version 02.50 What's New (see page 30)
- Version 02.00 What's New (see page 31)
- Version 01.40 What's New (see page 32)
- Version 01.20 What's New (see page 34)
- Version 01.10 What's New (see page 35)

Version 03.60 What's New

In version 03.60 of the *Agilent Logic Analyzer* application:

- You could control the new 16901A logic analysis system. See 16900-Series Logic Analysis System Product Overview (see page 561).
- The new 16950B logic analyzer card was supported in the 16900-series logic analysis system. See 16950/51 Logic Analyzer Notes (see page 593).
- The "FPGA Dynamic Probe for Altera FPGAs" (in the online help) add-in software was introduced; it lets you probe signals internal to FPGAs.
- You could set up an external protocol analyzer and a logic analyzer to cross-trigger and make time-correlated measurements (using markers). See "External Protocol Analyzer Time Correlation" (in the online help).
- You could open ALA format configuration files "read-only" in any *Agilent Logic Analyzer* application instance (without licenses for tools, windows, etc. that may be in the configuration). See ALA vs. XML, When to Use Each Format (see page 399).

See Also

- Version 03.55 What's New (see page 23)
- Version 03.50 What's New (see page 24)
- Version 03.30 What's New (see page 26)
- Version 03.20 What's New (see page 28)
- Version 03.00 What's New (see page 29)
- Version 02.50 What's New (see page 30)
- Version 02.00 What's New (see page 31)
- Version 01.40 What's New (see page 32)
- Version 01.20 What's New (see page 34)
- Version 01.10 What's New (see page 35)

Version 03.55 What's New

In version 03.55 of the *Agilent Logic Analyzer* application:

- The E9524A MicroBlaze trace toolset updated the "inverse assembler" (in the online help) to support MicroBlaze version 5.

See Also

- Version 03.50 What's New (see page 24)
- Version 03.30 What's New (see page 26)
- Version 03.20 What's New (see page 28)
- Version 03.00 What's New (see page 29)
- Version 02.50 What's New (see page 30)
- Version 02.00 What's New (see page 31)
- Version 01.40 What's New (see page 32)
- Version 01.20 What's New (see page 34)
- Version 01.10 What's New (see page 35)

Version 03.50 What's New

In version 03.50 of the *Agilent Logic Analyzer* application:

- You could control the new 16800-series logic analyzers (see page 558).
- You could view decoded packet data in the new Packet Viewer window. See Analyzing Packet Data (see page 280).
- The "Xilinx FPGA Dynamic Probe" (in the online help) added support for MicroBlaze trace cores (MTC) and there was a new E9524A MicroBlaze trace toolset that provides "inverse assembly" (in the online help).
- You could use the new Demo Center (see page 56) application to view logic analysis system feature demonstrations.
- You could use the new "Signal Extractor" (in the online help) tool to extract data from one input bus/signal and place it on multiple output buses/signals. This is useful for extracting I and Q data from simple serial protocols or remultiplexing high-speed digital data that has been demultiplexed onto additional logic analyzer channels.
- You could connect to another logic analysis system without having to go *offline* first. See Connecting to a Logic Analysis System (see page 63).
- There were improvements for multiframe logic analysis systems (see page 400), especially for *performance multiframe configurations*.
- You could rename the bits of a bus and view them when the bus is expanded in the Waveform display window. See To rename the bits of a bus (see page 86).
- You could add separator rows to the Waveform display window. See To insert separator rows (see page 212).
- A graphical trigger overview was added when viewing module details in the Status dialog (see page 490).
- You could import external data into the logic analysis system from module binary (ALB) format files as well as module CSV format text files. See Using Data Import Modules (see page 191).
- There was a "Force Prestore" option to ensure that the specified percentage of pre-trigger memory is is filled before the logic analyzer begins looking for a trigger. Timing mode used to behave this way while state mode did not. With the "Force Prestore" option, you can choose the desired behavior for both sampling modes. See To specify the trigger position (see page 111).
- You could use the logic analysis system's 10 MHz CLOCK IN input to keep a logic analyzer and an external oscilloscope in sync over long acquisitions. See " Correlation Drift Over Long Acquisitions" (in the online help).

- You could export Listing display window data to 16700 ASCII format files. See To export data to 16700 ASCII format files (see page 180).

See Also

- Version 03.30 What's New (see page 26)
- Version 03.20 What's New (see page 28)
- Version 03.00 What's New (see page 29)
- Version 02.50 What's New (see page 30)
- Version 02.00 What's New (see page 31)
- Version 01.40 What's New (see page 32)
- Version 01.20 What's New (see page 34)
- Version 01.10 What's New (see page 35)

Version 03.30 What's New

In version 03.30 of the *Agilent Logic Analyzer* application:

- You could add an external oscilloscope without the time correlation fixture. Default (typical) deskew values for your logic analyzer and oscilloscope models were used. You could still use the time correlation fixture to get the most accurate deskew values for the actual instruments being used. See " External Oscilloscope Time Correlation and Data Display" (in the online help).
- You could import external oscilloscope data and view it faster with import and waveform drawing performance improvements.
- You could activate software licenses, access floating license servers, and borrow floating licenses much easier using the new license manager interface. See Managing Software Licenses (see page 311).
- You could import external data into the logic analysis system and analyze it just like data acquired by logic analyzer modules. See Using Data Import Modules (see page 191).
- You could use these new VBA (Microsoft Visual Basic for Applications) macros and VbaView windows:
  - *SendToExcel* VBA macro that sends captured data to Microsoft Excel.
  - *SendToPatternGeneratorModule* VBA macro that sends captured data to a pattern generator module.
  - *Timing Compare* VbaView window that compares timing analyzer data with a specified tolerance (plus or minus a number of samples).

  See Tools Menu (see page 410), Windows Menu (see page 417), and the online help included with the macro or VbaView window.
- You could use MatLab in conjunction with the logic analysis system more easily with the new MatLab Connectivity and Analysis package. This licensed package contains these VBA macros and VbaView windows:
  - *SendToMatLab* VBA macro that sends logic analyzer data to MatLab.
  - *MatLab Analysis* VbaView window that sends logic analyzer data to MatLab for processing and displays the results in an XY scattergram chart.
  - *FFT* VbaView window that performs a Fast Fourier Transform on logic analyzer data and displays the results in a line chart.

  See the online help included with the VBA macro and VbaView windows.
- You could use additional remote programming commands with the updated Remote Programming Interface (RPI) compatibility package. See "Using the Remote Programming Interface (RPI)" (in the online help).

See Also

- Version 03.20 What's New (see page 28)
- Version 03.00 What's New (see page 29)
- Version 02.50 What's New (see page 30)
- Version 02.00 What's New (see page 31)
- Version 01.40 What's New (see page 32)
- Version 01.20 What's New (see page 34)
- Version 01.10 What's New (see page 35)

Version 03.20 What's New

In version 03.20 of the *Agilent Logic Analyzer* application:

- The 16760A logic analyzer card was supported in the 16900-series logic analysis system. See 16760 Logic Analyzer Notes (see page 582).
- You could import data from external oscilloscopes. The Agilent 6000-series oscilloscopes were added to the list of supported oscilloscopes. Also, a new VbaView window let you use the oscilloscope's web interface from within the *Agilent Logic Analyzer* application. See " External Oscilloscope Time Correlation and Data Display" (in the online help).
- The "Serial To Parallel" (in the online help) tool for converting serial data streams into parallel bus data was introduced.
- The "Xilinx FPGA Dynamic Probe" (in the online help) add-in software was updated to support automatic set up features.
- Pattern generator compiled vectors were saved in XML format configuration files as well as ALA format configuration files. See "Using the Pattern Generator" (in the online help).
- Microsoft Visual Basic for Applications (VBA) macros and VbaView windows were saved in XML format configuration files as well as ALA format files. See "Distributing VBA Code" (in the online help).
- You could disable multiple modules at the same time and choose whether or not to remove their connections to tools and display windows. When you leave connections, buses/signals associated with disabled modules remain in display windows, but they have no data. See To disable and enable modules (see page 76).

See Also

- Version 03.00 What's New (see page 29)
- Version 02.50 What's New (see page 30)
- Version 02.00 What's New (see page 31)
- Version 01.40 What's New (see page 32)
- Version 01.20 What's New (see page 34)
- Version 01.10 What's New (see page 35)

Version 03.00 What's New

In version 03.00 of the *Agilent Logic Analyzer* application:

- The 16720A pattern generator card was supported in the 16900-series logic analysis system. See "Using the Pattern Generator" (in the online help).
- The *eye finder* feature for automatically adjusting state mode sampling positions was enhanced to automatically determine optimal threshold voltage settings as well. See Understanding State Mode Sampling Positions (see page 378).
- Microsoft Visual Basic for Applications (VBA) was been integrated into the *Agilent Logic Analyzer* application to let you easily automate measurements and add custom control and data visualization tools. See Extending Capture Capability with VBA (see page 182) and Extending Data Visualization/Analysis with VBA (see page 309).

See Also

- Version 02.50 What's New (see page 30)
- Version 02.00 What's New (see page 31)
- Version 01.40 What's New (see page 32)
- Version 01.20 What's New (see page 34)
- Version 01.10 What's New (see page 35)

Version 02.50 What's New

In version 02.50 of the *Agilent Logic Analyzer* application:

- The *eye finder* feature for automatically adjusting sampling positions in state mode was made available for 1680- and 1690-series logic analyzers (this feature was previously only available for logic analyzers in the 16900-series logic analysis system).
- The "Xilinx FPGA Dynamic Probe" (in the online help) add-in software was introduced; it lets you probe signals internal to FPGAs.
- The "General Purpose Probe" (in the online help) add-in software was added; it lets you set up probe definitions in order to:
  - Cause device under test pin/pad numbers to appear in the Buses/Signals setup tab.
  - Document logic analyzer pod connections.
  - Prepare for importing netlist files to automatically define buses/signals.
- The "PCI Express Analysis Probe" (in the online help) add-in software (for the N4220A/B PCI Express analysis probe) was introduced, and the new Packet Decoder tool was used to decode PCI Express bus data.
- In the Overview window, a separate column for probes (general purpose, FPGA dynamic, PCI Express, etc.) was added, and you were able to access probe properties from there.

See Also

- Version 02.00 What's New (see page 31)
- Version 01.40 What's New (see page 32)
- Version 01.20 What's New (see page 34)
- Version 01.10 What's New (see page 35)

Version 02.00 What's New

In version 02.00 of the *Agilent Logic Analyzer* application:

- You could control the new 16900-series logic analysis system (see page 561) and access the new features associated with it. The same *Agilent Logic Analyzer* application controls the 1680- and 1690-series logic analyzers and can be used by itself on Windows XP/2000 computers for *remote access* (see page 63) or *offline analysis* (see page 197).
- The ability to split logic analyzer modules was added. This is useful for analyzing buses with different clocks.

  With multiple logic analyzer modules, the ability to identify which is the system trigger and specify the skew between the modules was added.
- The *eye finder* feature for automatically adjusting sampling positions in state mode was added for logic analyzers in the 16900-series logic analysis system.
- The ability to load program symbols from compiler-generated output files was added.
- The ability to display the high-level language source code associated with captured data and set up triggers based on source code locations was added in the new Source display window.
- A new dual-sample state sampling clock mode, often used to capture DDR memory bus activity, was added.
- The Netlist Import dialog was reorganized and a separate dialog for defining probes was added.
- New System Summary and Status dialogs for displaying information about the logic analysis system were added.
- Performance improvements were made: waveform drawing became much faster, and the *Agilent Logic Analyzer* application was made into a multi-threaded application.

See Also

- Version 01.40 What's New (see page 32)
- Version 01.20 What's New (see page 34)
- Version 01.10 What's New (see page 35)

Version 01.40 What's New

Version 01.40 of the *Agilent Logic Analyzer* application:

- Let you display the same data in multiple windows by using the Overview window (which replaced the previous Tool Overview dialog); for example, you could display the same data filtered in one Listing window and unfiltered in another Listing window.
- In the Buses/Signals dialog, you could reorder bits assigned to a bus/signal name. This is useful in cases where buses in the device under test are not probed by consecutive logic analyzer channels.
- Also in the Buses/Signals dialog, you could import bus/signal names and assignments from a netlist file.
- Let you time-correlate data captured by the logic analyzer to data captured by external Infiniium oscilloscopes using the E5850A time-correlation fixture.
- Let you control logic analyzers with remote programs that communicate with the Instrument COM Automation Server, included with the *Agilent Logic Analyzer* application.
- Let you save more logic analyzer configuration information to generic XML configuration files. You could save trigger specifications in XML format and transfer them between different logic analyzers. Also, you could use portions of generic XML configuration files with several of the COM automation commands.
- Let you show statistics in interval markers and stop a repetitive measurement or send an e-mail message on particular statistic values.
- Let you use the Compare window's properties, and the Difference Properties tab, to specify the run until options. (The Compare window's Run Until button was removed.)
- Let you use the *quick pick* bus/signal name selection feature to quickly select from recently used names. This feature was added to the Filter/Colorize tool properties dialog and to the advanced trigger setup dialog.

- When exporting data to comma-separated value (CSV) files, you could choose to export data from selected buses/signals. Also, you could select the number base of the data that is exported.
- In the advanced trigger setup dialog, you could re-group events.

- Let you lock the scrolling on display windows (for example, Waveform, Listing, or Compare) so that when one window is scrolled, all locked windows are scrolled as well. You can find the *Lock* property with other windows property settings.
- Let you set the delay between repetitive measurements so that you could look at the captured data before deciding whether to stop the measurement.

See Also

- Version 01.20 What's New (see page 34)
- Version 01.10 What's New (see page 35)

Version 01.20 What's New

Version 01.20 of the *Agilent Logic Analyzer* application:

- Let you, in the timing (asynchronous) sampling mode, trigger on multiple glitches/edges.
- Let you perform a simple compare of captured data sets.
- Added the ability to save/load user-defined symbols to/from XML format logic analyzer configuration files.

  This meant you could use text processing tools to re-format symbol information from software development tools, insert them into an XML format configuration file, and load them into the *Agilent Logic Analyzer* application.
- Contained an API and documentation to enable inverse assembler and analysis tool development.
- Extended its offline analysis capability to 16700-series logic analyzers.

See Also

- Version 01.10 What's New (see page 35)

Version 01.10 What's New

Version 01.10 of the *Agilent Logic Analyzer* application:

- Added a Japanese version of the online help.

2
Getting Started

- Tutorial - Getting to know your logic analyzer (see page 38)
- Measurement Examples (see page 50)
- Demo Center (see page 56)

Tips for Experienced Users

- "*Quick Start for 16700-Series Users*"

Tutorial - Getting to know your logic analyzer

The following tutorial is intended to give you a quick overview of logic analyzer basics. In addition to learning the concepts of logic analysis, you will see some of the logic analyzer's more common features by going through a measurement overview. Finally, you are shown some easy time saving tasks that can quickly make you as productive as a more experienced user.

Logic analysis basics

- When should you use an oscilloscope? (see page 364)
- When should you use a logic analyzer? (see page 365)
- What is a logic analyzer? (see page 366)

  Timing analyzer:

  - Sampling clock (see page 366)
  - Sampling (see page 367)
  - Triggering (see page 368)

  State analyzer:

  - Sampling clock (see page 369)
  - Sampling (see page 370)
  - Triggering (see page 370)

Measurement overview

The following overview does not require an active device under test. However, in order to show features that work on data, you are asked to load a configuration file between steps 5 and 6 that contains data to finish the exercise.

- Turning on the logic analyzer (see page 39)
- Connecting to the device under test (see page 39)
- Setting up bus/signal names (see page 40)
- Setting the acquisition mode (see page 42)
- Setting up a simple trigger (see page 42)
- Open the tutorial configuration file (see page 43)
- Using markers (see page 44)
- Zooming in on the data (see page 45)

Time saving tasks

- Loading and saving configuration files (see page 45)
- Saving and recalling trigger setups (see page 46)
- Quick marker measurements (see page 47)
- Searching data (see page 48)
- Toolbars, tool tips, and mouse shortcuts (see page 49)

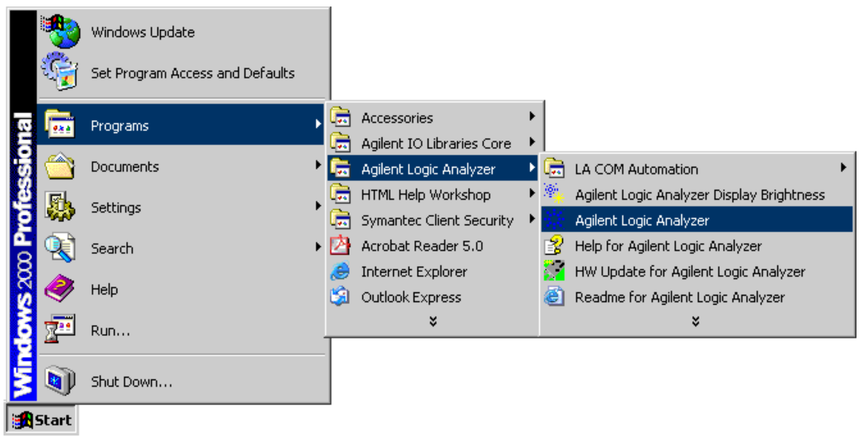
See Also • Product Overviews (see page 552)

Turning on the logic analyzer

[Tutorial Home (see page 38)] [Next Topic (see page 39)] [Previous Topic (see page 370)]

1 Plug in the power cable and press the front-panel On/Off button.

2 From the Windows Start bar, click **Start>Programs>Agilent Logic Analyzer>Agilent Logic Analyzer**.



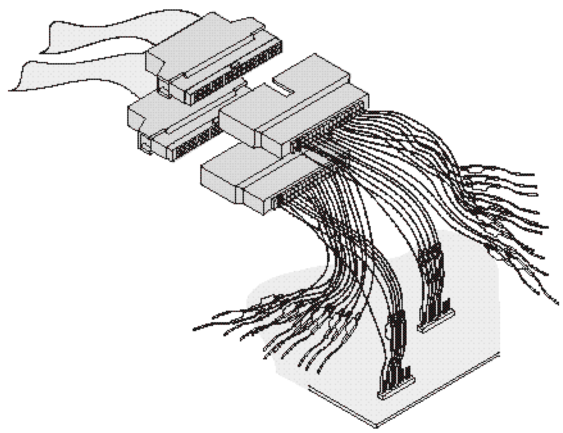
NOTE  Optional: If you have a logic analyzer shortcut icon on screen, double-click the icon.

Connecting to the device under test

[Tutorial Home (see page 38)] [Next Topic (see page 40)] [Previous Topic (see page 39)]

The first step in using a logic analyzer is to probe signals in the device under test.

NOTE In this tutorial, no probe connections are required. Later on in this tutorial, you are asked to load a configuration file containing data to simulate the results of a probed device under test.



For more information about probing options, see Probing the Device Under Test (see page 59).

Setting up bus/signal names

[Tutorial Home (see page 38)] [Next Topic (see page 42)] [Previous Topic (see page 39)]

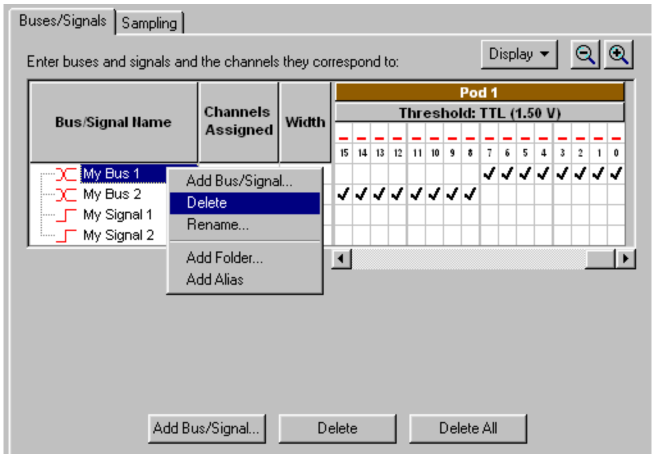
By default, the analyzer has one bus (My Bus 1) set up in the interface. The following exercise cleans up the display defaults and re-configures the bus/signal setup for a new measurement.

Delete bus/signal names

1 In the menu bar click **Setup>(Logic Analyzer Module)>Bus/Signal...**.

2 In the Analyzer Setup dialog that appears, right-click on **My Bus 1**, then select **Delete**. Repeat until all bus signal names are deleted. After the last bus/signal is deleted, "My Bus 1" appears again as a default name.

TIP You can delete all bus/signal configurations at once with the **Delete All** button.

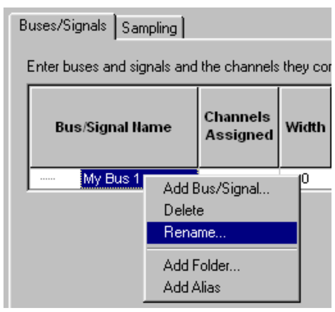


Add new bus/signal name

1 In the Analyzer Setup dialog, right-click on **My Bus 1**, then select **Rename**.

2 From the popup keypad that appears, type in the new name "counter".

3 Select **OK**.



Map signals into the analyzer

The logic analyzer must be told which probed signals from the device under test are to be included in the measurement, and how you want them grouped. In this exercise, you assign channels 0 - 7 on Pod 1 under the name "counter". Notice that when more than one channel is assigned to "counter" it becomes a bus.

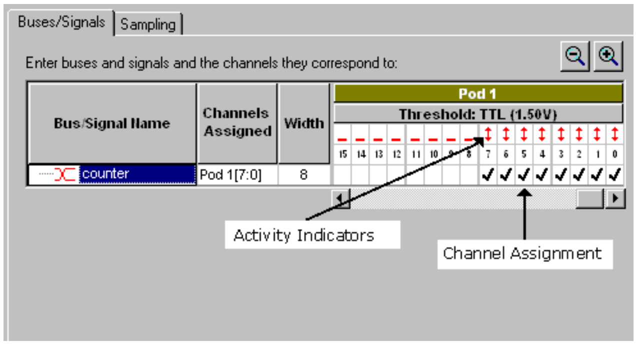
1 Check the activity indicators for verification of proper connection to the device under test. You should see a transition arrow on all 8 channels.

NOTE

If you have real device under test hardware, you will see activity indicators as shown below. If you are loading the demo configuration file (later in this tutorial) you will not see activity.

2 Click each **channel assignment box** under channels 0 - 7 on Pod 1. Notice that as you assign channels, the configuration information is updated for the bus/signal.

3 Click **OK**.



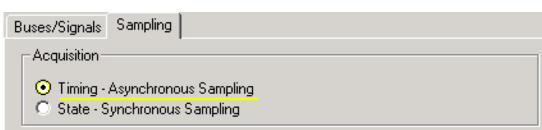
Setting the acquisition mode

[Tutorial Home (see page 38)] [Next Topic (see page 42)] [Previous Topic (see page 40)]

Under the Sampling tab of the Analyzer Setup dialog is where you set the analyzer to be either a timing or state analyzer. You also set either the timing options, such as memory depth or sampling period, or the state clocking options.

1 From the menu bar, click **Setup>(Logic Analyzer Module)>Timing/State (Sampling)...**, or click the  icon in the toolbar.

2 Select **Timing - Asynchronous Sampling**.



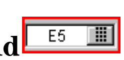
3 Click **OK**.

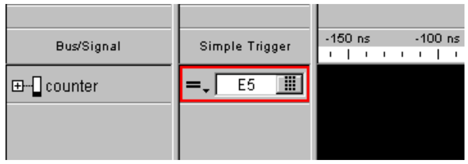
Setting up a simple trigger

[Tutorial Home (see page 38)] [Next Topic (see page 43)] [Previous Topic (see page 42)]

The Simple Trigger is a quick way to configure the analyzer to trigger on either a data pattern on a bus, or an attribute of a single signal such as a rising edge or a low logic level.

1 In the Simple Trigger column, click on the **pattern qualifier**  and set it to **Equal**.

2 Click in the **text entry field**  and enter the data pattern "E5".



Open the tutorial configuration file

[Tutorial Home (see page 38)] [Next Topic (see page 44)] [Previous Topic (see page 42)]

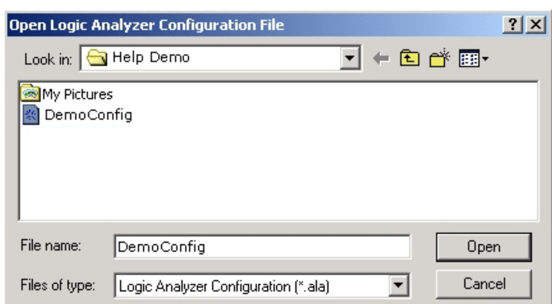
At this point in a measurement, you would normally run the logic analyzer. However, because you are not connected to a device under test, you cannot capture real data. You will have to load a configuration file that contains this data.

Load the configuration file

1 Select **File>Open**.

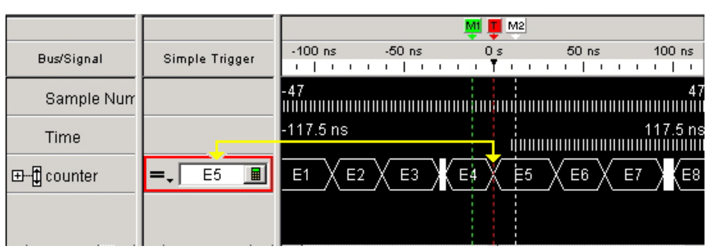
2 From the file manager dialog, select the file named **DemoConfig.ala** from the following directory: **C:\Documents and Settings\All Users\Documents\Agilent Technologies\Logic Analyzer\Default Configs\Agilent\Help Demo**

3 Select **Open**.



View the data

Notice how the logic analyzer triggered on data pattern E5 and placed it in the center of the display. The red line shows that the trigger point is at the start of the data pattern E5.



Using markers

[Tutorial Home (see page 38)] [Next Topic (see page 45)] [Previous Topic (see page 43)]

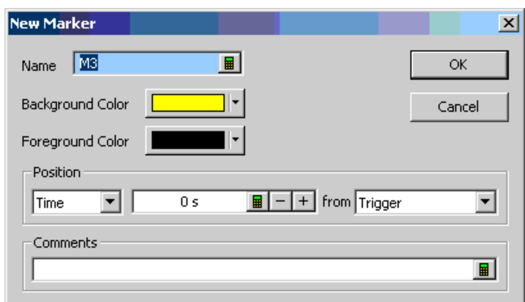
Markers are used for creating reference points in data. Once markers are placed in data, you can use them to quickly see what time, sample, or data value the marker is set on.

To create a marker

1 From the menu bar, click **Markers>New**.

2 From the New Marker dialog that appears, configure the new marker and if desired, specifically a position it in data. When you do not position the marker, by default it is placed at the trigger point.

3 Select **OK**.



To place a marker in data

When you first create a new marker, you have the option to place it in data at a specific point in time or a specific sample number. The following exercise shows you other ways to position markers in data.

1 In the display, click on marker M3 (your new marker) and while holding the mouse button down, drag maker M3 to -100ns before trigger, then release. Notice that the marker position value changes as you move it.

2 From the menu bar, click **Markers>Place On Screen**, then select M1 and click **OK**. Notice how M1 is placed at center screen at the red trigger line.

3 Point the mouse cursor at any desired point in data, then right-click and select **Place Marker**. From the Place Marker dialog that appears, choose the M2 marker. Notice that the marker is placed where the mouse was pointing.

Go To a marker in data

Once you have markers set in data, you can quickly find any of them as follows.

1 From the menu bar, click **Markers>GoTo**.

2 Select the marker you want to find, and click **OK**.

Zooming in on the data

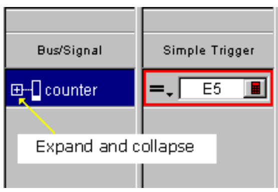
[Tutorial Home (see page 38)] [Next Topic (see page 45)] [Previous Topic (see page 44)]

Data from a timing analyzer is displayed (as on an oscilloscope) as waveforms on a horizontal time axis. To zoom in or out on a waveform, change the Scale (time/division) of the time axis of the waveform.

Both state and timing analyzers can have multiple signals grouped together in a bus. To get a view of all signals, you can expand a bus into individual signals.

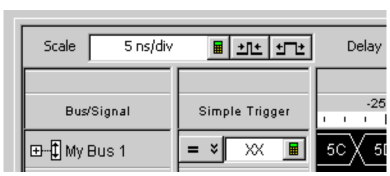
Expand a bus

Click the "+" symbol just to the left of the bus named "counter". The collection of signals under "counter" breaks out into individual signals named counter[0] - counter[7].



Change the scale

Click the zoom out icon to expand the signals to where you want them.



Loading and saving configuration files

[Tutorial Home (see page 38)] [Next Topic (see page 46)] [Previous Topic (see page 45)]

Many times it is quicker to open an existing configuration file with a similar setup than to create a new configuration from scratch. You simply open a similar file, make the appropriate changes to the setup, then save the file as a new filename.

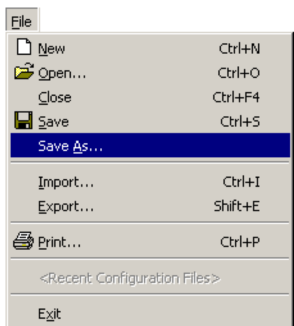
NOTE

When you rename an existing configuration file, you retain the saved trigger setups and "Find" search favorites from the first configuration file.

You already have learned how to open a configuration file. In the following exercise, you will save the "democonfig" file to a new name.

1 From the menu bar, click **File>Save As...**.

2 From the file manager dialog that appears, type in the new name "myconfig", then click **Save**.



Saving and recalling trigger setups

[Tutorial Home (see page 38)] [Next Topic (see page 47)] [Previous Topic (see page 45)]

Each time you set up a new trigger and run the measurement, the trigger setup is saved in the logic analyzer. It is quicker to recall a trigger setup rather than re-configure the trigger setup each time.

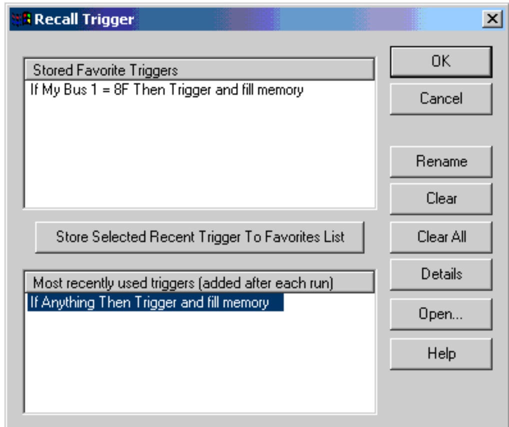
NOTE The logic analyzer must be run before the trigger setup is stored. Also, trigger setups are stored as part of the configuration file. If you load a new configuration file, the trigger setups will be overwritten by trigger setups stored with the new file.

To recall a trigger setup

1 From the menu bar, click **Setup>(Logic Analyzer Module)>Recall Trigger...**.

2 From the lower list, select the desired trigger setup, then click **OK**.

TIP When the list of most recently used triggers get long, you can store the most often used triggers in the upper favorites list.

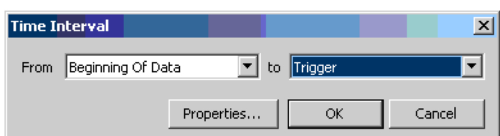


Quick marker measurements

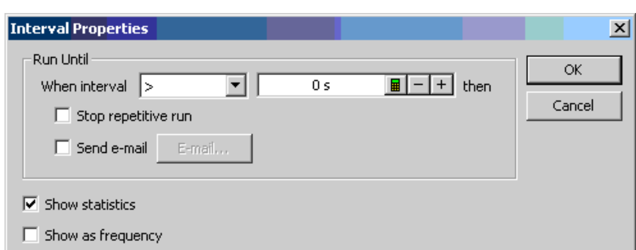
[Tutorial Home (see page 38)] [Next Topic (see page 48)] [Previous Topic (see page 46)]

You can quickly read the time or number of samples between markers.

1 Click **Markers>New Time Interval Measurement**.
2 Configure the Interval dialog to display the time from **Beginning of Data** to **Trigger** as shown below.



To show statistics with the time interval measurement (after repetitive runs, click **Properties**; then, in the Interval Properties dialog, check **Show statistics**.

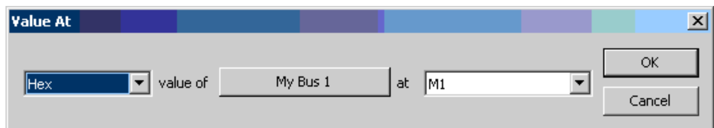


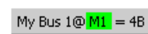
Click **OK** to close the Interval Properties dialog, and click **OK** to close the Time Interval dialog.

After a repetitive run, the result of the time interval measurement is displayed in the marker measurements display bar.

3 Click **Markers>New Value At Measurement**.

4 Configure the Value At dialog to display the **Hex** value of **My Bus 1** at **M1** as shown below; then, click **OK**.



The result of the value at measurement 

is displayed in the marker measurement display bar.

Searching data

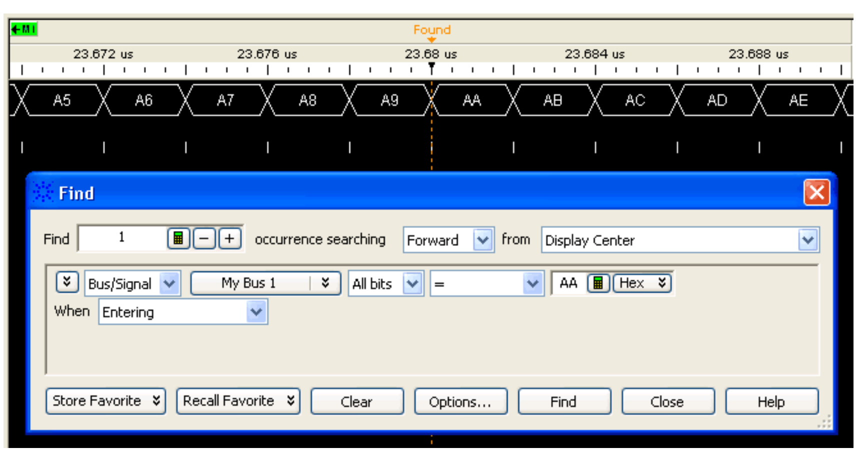
[Tutorial Home (see page 38)] [Next Topic (see page 49)] [Previous Topic (see page 47)]

You can search for a data pattern on a bus or a signal. You can also choose when the search begins and ends. Finally, you can save the search criterion in a favorites list.

1 From the menu bar, click **Edit>Find...**.

2 In the Find dialog, configure the search criterion as shown below to find "AA".

3 Select **Find**.



As you configure the Find dialog, try to think of it as constructing a sentence that reads left-to-right.

"**Find** the **1st** occurrence searching **Forward** from **Display Center**, on a bus named **My Bus 1**, including **All bits**, a pattern that **Equals AA**".

Toolbars, tool tips, and mouse shortcuts

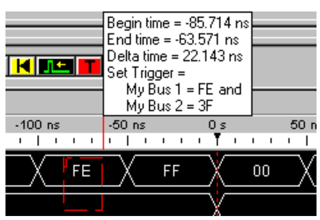
[Tutorial Home (see page 38)] [Previous Topic (see page 48)]

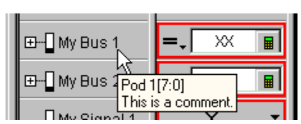
Throughout this tutorial, the menu bar has been used to access features. There are two other ways to access features as well as other useful tips that can save you time.

Toolbars Below the menu bar are groups of icons that represent shortcuts to many dialogs and features. For more information refer to Toolbars (see page 420) in the main help.

Mouse Shortcuts There are many mouse shortcuts available. To access them simply point the mouse over a screen element such as a marker, or screen area, then right-click the mouse. Mouse shortcuts are especially useful within the waveform and listing data display areas.

Tool Tips Tool tips are small information displays that appear during operations such as moving markers, setting a trigger with the mouse, or hovering the mouse over a bus/signal name. Use them as comments (see page 95), or to monitor your progress or current positions.





Measurement Examples

The following measurement examples show you the typical order of steps to set up and run a measurement. As you go through the examples, you will encounter steps such as probing or triggering where alternative choices are available. In these steps, select the probing or trigger example that best fits your measurement.

- Making a timing analyzer measurement (see page 50)
- Making a state analyzer measurement (see page 51)
- To trigger on one of multiple edges or glitches (see page 52)
- To trigger on ranges (see page 53)

See Also

- Tutorial - Getting to know your logic analyzer (see page 38)
- Timing Mode Trigger Functions (see page 504)
- State Mode Trigger Functions (see page 517)

Making a timing analyzer measurement

The following measurement example shows you the steps necessary to configure and run the logic analyzer for a typical timing analyzer measurement. As you go through the example, make the appropriate choices from the selection lists that best match the kind of configuration you need.

TIP

If you are new to logic analysis, refer to "Tutorial - Getting to know your logic analyzer (see page 38)" for a quick tutorial on logic analysis concepts and measurements.

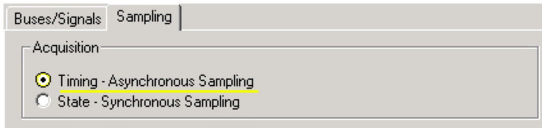
1. Connect the probing to the device under test (see Probing the Device Under Test (see page 59) for more information).
2. Turn on the logic analyzer.

Bus and signal setup

1. In the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**.
2. From the Buses/Signals tab, assign bus/signal names to the device under test signals probed. You do this by either renaming (see page 85) existing names, or deleting (see page 84) and creating (see page 83) new names.
3. From the Buses/Signals tab, define buses and signals (see page 82) under the appropriate pods for all probed buses/signals on the device under test.

Acquisition mode setup

1. In the Analyzer Setup dialog, select the **Sampling** tab.
2. From the Sampling tab, set the acquisition mode to Timing - Asynchronous Sampling.



3 Set the Sampling Options (see page 98).

4 Set the timing mode Sampling Period (see page 99).

Trigger setup

1 The trigger required to capture specific data depends on the measurement. However, the trigger is generally set in two ways.

- From within the data display, set up a simple trigger (see page 133).
- From the Advanced Trigger dialog (see page 445), set up a timing mode advanced trigger (see page 504) function.

Run the measurement

1 Run (see page 168) the measurement.

See Also

- To specify the trigger position (see page 111)
- To set acquisition memory depth (see page 112)

Making a state analyzer measurement

The following measurement example shows you the steps necessary to configure and run the logic analyzer for a typical state analyzer measurement. As you go through the example, make the appropriate choices from the selection lists that best match the kind of configuration you need.

TIP

If you are new to logic analysis, refer to "Tutorial - Getting to know your logic analyzer (see page 38)" for a quick tutorial on logic analysis concepts and measurements.

1 Connect the probing to the device under test (see Probing the Device Under Test (see page 59) for more information).

NOTE

Be sure that the clock signals of your device under test are connected to clock channels on the pods. Any unused clock channels can be used for additional data channels and will not feed into the state clock setup.

2 Turn on the logic analyzer.

Bus and signal setup

1 In the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...** .

2 From the Buses/Signals tab, assign bus/signal names to the device under test signals probed. You do this by either renaming (see page 85)

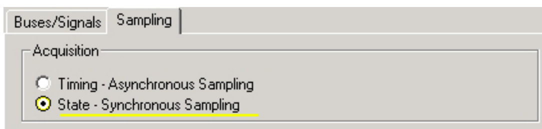
existing names, or deleting (see page 84) and creating (see page 83) new names.

3 From the Buses/Signals tab, define buses and signals (see page 82) under the appropriate pods for all probed buses/signals on the device under test.

Acquisition mode setup

1 In the Analyzer Setup dialog, click the Sampling tab.

2 From the Sampling tab, set the acquisition mode to State - Synchronous Sampling.



3 Set the state clock mode (see page 101).

4 Set the state sampling clock (see page 106).

5 If necessary, set the advanced state clocking (see page 107).

Trigger setup

1 The trigger required to capture specific data depends on the measurement. However, the trigger is generally set in two ways.

- From within the data display, set up a simple trigger (see page 133).
- From the Advanced Trigger dialog (see page 445), set up an advanced trigger (see page 517) function.

Run the measurement

1 Run (see page 168) the measurement.

See Also

- To specify the trigger position (see page 111)
- To set acquisition memory depth (see page 112)

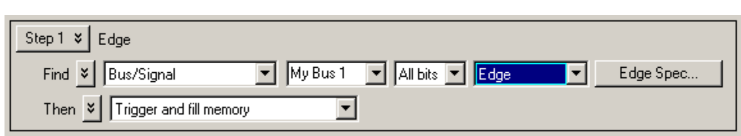
To trigger on one of multiple edges or glitches

1 In the timing sampling mode, set up an Advanced Trigger.

2 Select the bus on which you're looking for one of multiple edges or glitches.

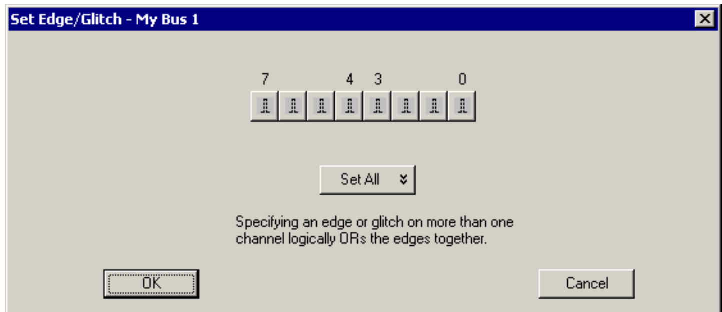
3 Select **All bits** in the bus.

4 Select **Edge**.



5 Click **Edge Spec...**.

6 In the Set Edge/Glitch dialog, specify edges or glitches you are looking for; use the **Set All** button to make a selection for all signals in the bus.



7 Click **OK** to close the Set Edge/Glitch dialog.

8 Click **OK** to close the Advanced Trigger dialog.

NOTE Glitches are not drawn on the screen. You need an oscilloscope to further troubleshoot glitches and find out when they occur.

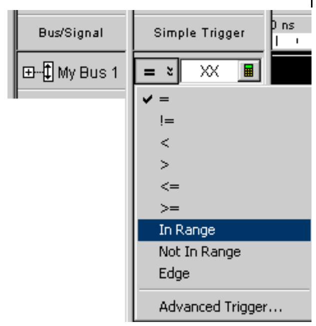
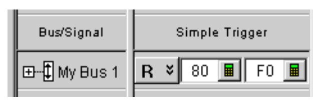
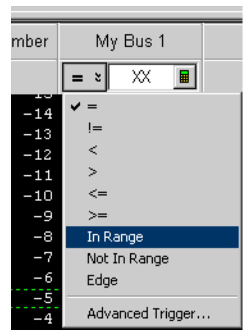
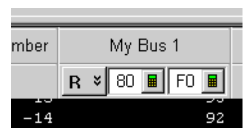
To trigger on ranges

NOTE In order to trigger on ranges of bus values, the bus:

- Must not have reordered bits.
- Must not contain clock bits that span pod pairs.
- Must span 2 or fewer pod pairs (up to 64 bits wide).

When setting up simple triggers (see page 133)

1 In the Simple Trigger field for a bus, click the operator button; then, choose either **In Range** or **Not In Range**.

	Waveform Display Window	Listing/Compare/Source Display Window
Bus Range Trigger	 	 

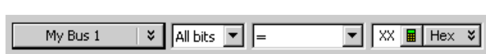
2 Specify the range values, either by entering values in the low range and high range text entry fields or, when the **Symbol** number base is selected, by using the Select Symbol dialog (see page 477).

3 From the menu bar, choose **Run/Stop>Run**, or click the icon from the run/stop toolbar (see page 424).

When setting up advanced triggers (see page 138)

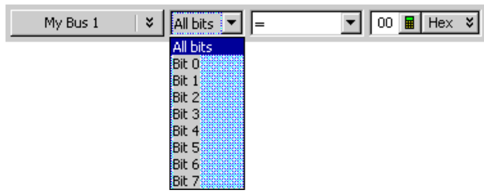
1 Click in the analyzer setup toolbar, or choose **Setup>(Logic Analyzer Module)>Advanced Trigger...** from the menu bar.

2 In the Advanced Trigger dialog, select the bus.

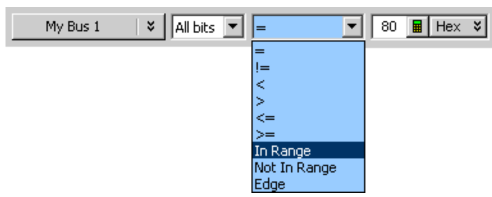


Clicking lets you select from recently used bus/signal names. Clicking elsewhere on a bus/signal name button opens a Select dialog for selecting a different name.

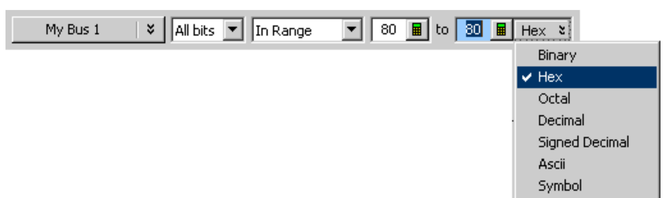
3 Select **All bits** on the bus.



4 Select either the **In Range** or **Not In Range** operator.



5 Select the number base (**Binary**, **Hex**, **Octal**, **Decimal**, **Signed Decimal**, **Ascii**, or **Symbol**).



6 Specify the range values, either by entering values in the low range and high range text entry fields or, when the **Symbol** number base is selected, by using the Select Symbol dialog (see page 477).

7 From the menu bar, choose **Run/Stop>Run**, or click the  icon from the run/stop toolbar (see page 424).

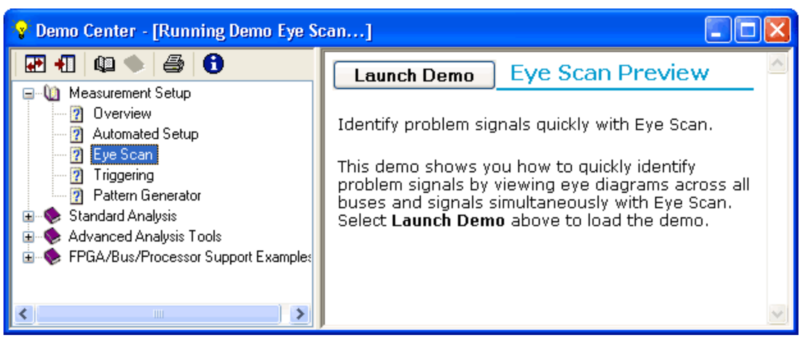
Demo Center

Demo Center is an application that demonstrates logic analysis system features. It loads illustrative configurations into the *Agilent Logic Analyzer* application's *offline-demo* mode and highlights feature capabilities.

To launch Demo Center

- From the *Agilent Logic Analyzer* application's main menu, choose **Help>Show Demo...**.
- From the *Agilent Logic Analyzer* application's Demo Center toolbar, click the Show Demo icon.
- From the Windows Start bar, click **Start>All Programs>Agilent Logic Analyzer>Run Logic Analyzer Demo Center**.

The Demo Center application and the *Agilent Logic Analyzer* application are tiled horizontally on the desktop.



The Float button maximizes the *Agilent Logic Analyzer* application's window lets the Demo Center application window float over it. The Locate button returns to horizontally tiled windows. The What is Demo Center button displays more information.

To use Demo Center

1 Use the left pane to navigate to the feature demonstration you want to view.

The Expand and Collapse buttons affect the feature hierarchy tree.

2 Select the feature you want to learn about by clicking it.

Information about the feature appears in the right pane.

3 Click **Launch Demo**.

A configuration file that illustrates the feature is loaded into the *Agilent Logic Analyzer* application, and more information about the feature appears in Demo Center's right pane. The Print button lets you print the information.

4 When you are done exploring the feature, click **Press to Select Another Demo**.

3
Probing the Device Under Test

Before you can make logic analysis measurements on a device under test, you must connect the logic analyzer channels to (in other words, probe) the device under test.

There are several options for probing a device under test:

- Connecting to individual IC pins or test points. — This is called ***general purpose probing*** and is accomplished with flying-lead probe sets. Accessories that help with general purpose probing are also available.
- Connecting to all the pins of a specific QFP package. — This is called ***QFP package probing*** and is accomplished with optional elastomeric probe adapter and 1/4 flex adapter products available for several types of QFP packages.
- Designing connectors (or pads and mounting holes for soft-touch connectorless probes and retention modules) into the device under test. — This is called ***target connector probing*** or ***soft-touch connectorless probing*** and is accomplished with optional probes available for various signal and connector types.
- Using processor- or bus-specific probes. — These are called ***analysis probes*** (formerly called *preprocessors*) and are available for many processors and buses. Analysis probes include configuration files for setting up the logic analyzer, and they may include inverse assemblers or other post-processing tools for decoding captured data.

See Also For more information on general-purpose probing, QFP package probing, target connector and connectorless probing, and other probing options, see:

- "*Probing Selection Quick Reference Card*"
- "*Probing Solutions for Logic Analyzers*" ("latest version on web")
- "*Logic Analyzer Probing Solutions*"

For more information on analysis probes and other processor and bus solutions, see:

- "*Processor and Bus Support for Logic Analyzers*" ("latest version on web")
- "*Processor, Bus, and FPGA Support for Logic Analyzers*"

For more information on probing signals internal to an FPGA or setting up definitions for the probes used, see:

- "Setting Up Probes" (in the online help)

For more information on controlling signals in the device under test from a logic analysis system, see:

- To control signals in the device under test (see page 61)

To control signals in the device under test

The 16900A, 16902A, and 16903A logic analysis system *frames* (see page 649) have a *target control port*, an 8-bit, 3.3V port that can be used to send signals to a device under test. The target control port does not function like a pattern generator, but more like a remote control for switches in the device under test.

To use the target control port outputs:

1 Connect the target control port cable to the logic analysis system frame.

   The target control cable is keyed, so it can be inserted only one way. Plug it into the target control port with the key up and the cable hanging down.

   The wires on the target control port cable are color-coded. Bit 0 is brown, bit 1 is red, bit 2 is orange, and so on up to bit 7 (gray). The black and white wires are both ground. Pins 0, 2, 4, and 6 are on the top of the connector and arranged in the same order as the wires.

2 If you plan on using open collector, remember to install pull-up resistors to a maximum 4V. The maximum sink current into the Target Control port is 12 mA and includes a 51 ohm series resistor.

Example: Resetting Your Device Under Test

This example also applies to other types of signals you may want to send to your device under test. The reset line in this case is active low.

1 Attach one of the wires from the target control port cable to the reset line, using proper termination.

2 In the *Agilent Logic Analyzer* application, choose **Setup>Target Control Port...**.

3 In the Target Control Port dialog (see page 496), check **Enabled** for the target control port signal you are using.

4 Click **1** to output an active high.

5 When the device under test needs to be reset, click **Pulse**.

4
Connecting to a Logic Analysis System

If you opened the *Agilent Logic Analyzer* application on a logic analyzer or logic analysis system frame, you are most likely already connected to the local frame. (The right-most part of the status bar shows "Local".)

However, if you are offline (the right-most part of the status bar shows "Offline") and you want to connect to the local frame, or if you want to connect to a different, remote logic analysis system frame, you can do so from the **File** menu.

To connect to the local frame

• Choose the **File>Go Online To Local Frame** menu command.

To connect to a remote frame

1 Choose the **File>Go Online To...** menu command.

2 In the Select System to Use dialog (see page 479), select the system to access; then, click **Connect**.

   The logic analysis system can be:

   • *Local* — connected to the same computer or logic analyzer running the *Agilent Logic Analyzer* application.

   • *Remote* — somewhere else on the local area network.

3 If you are connecting to a remote logic analysis system that requires a password (see Setting Up Passwords for Remote Access (see page 72)), enter the password in the "Please enter connection password:" dialog, and click **OK**.

When you are connected to a remote logic analysis system frame, the right-most part of the status bar shows "Remote".

For more on using the Select System to Use dialog, see:

• To add a logic analysis system to the list (see page 65)
• To delete a logic analysis system from the list (see page 66)
• To refresh the logic analysis system list (see page 67)
• To view logic analysis system details (see page 68)
• To enter your "System In Use" comments (see page 69)
• To select a logic analysis system for auto-connect (see page 70)
• To chat with another logic analysis system user (see page 71)

See Also

- Offline Analysis (see page 197)

To add a logic analysis system to the list

1 In the Select System to Use dialog (see page 479) (which appears after choosing **File>Go Online To...**), click **Add**.

2 Enter the logic analysis system frame hostname or IP address in the dialog, and click **OK**.

See Also

- Returning to Online Analysis (see page 63)

To delete a logic analysis system from the list

1 In the Select System to Use dialog (see page 479) (which appears after choosing **File>Go Online To...**), select the logic analysis system you wish to delete.

2 Click **Delete**.

See Also

- Returning to Online Analysis (see page 63)

To refresh the logic analysis system list

1 In the Select System to Use dialog (see page 479) (which appears after choosing **File>Go Online To...**), click **Refresh**.

The logic analysis system status and detailed information is updated. Status can be:

Status	Description
Available	
Host offline	The logic analysis system has been powered down or taken off the network.
In use	The "System In Use" comment is displayed in parentheses.
Incompatible remote service version	The version information is displayed in parentheses. The *Agilent Logic Analyzer* application software on the logic analysis system frame needs to be updated to match the version of software installed on the machine displaying this dialog.

See Also

- Returning to Online Analysis (see page 63)

To view logic analysis system details

1 In the Select System to Use dialog (see page 479) (which appears after choosing **File>Go Online To...**), select the logic analysis system whose details you wish to view.

2 Click **Details...** (you may have to click **More >>** first).

The logic analysis system details are displayed in the Frame/Module Information dialog (see page 462).

See Also

- Returning to Online Analysis (see page 63)

To enter your "System In Use" comments

1 In the Select System to Use dialog (see page 479) (which appears after choosing **File>Go Online To...**), select the logic analysis system whose details you wish to view.

2 Click **Set My Comments** (you may have to click **More >>** first).

3 In the dialog that opens, enter your "system in use" comments.

   These comments usually contain your contact information.

See Also

- Returning to Online Analysis (see page 63)

To select a logic analysis system for auto-connect

1 In the Select System to Use dialog (see page 479) (which appears after choosing **File>Go Online To...**), select the logic analysis system that you wish to auto connect to.

2 Click **Set As Auto-Connect** (you may have to click **More >>** first).

See Also

- Returning to Online Analysis (see page 63)

To chat with another logic analysis system user

1 In the Select System to Use dialog (see page 479) (which appears after choosing **File>Go Online To...**), select the logic analysis system to which you want to send a chat message.

2 Click **Chat** (you may have to click **More >>** first).

3 In the Chat Select Destination dialog (see page 451), select whether you want to chat with the person logged into the logic analysis system or the person connected to the frame; then, click **OK**.

4 In the Chat dialog (see page 450), enter your message; then, click **Send**.

5 When you are finished with the chat session, click **Close**.

See Also

- Returning to Online Analysis (see page 63)

Setting Up Passwords for Remote Access

The *Agilent Logic Analyzer* application lets you connect to and remotely control logic analysis systems on the network.

If you have a logic analysis system you want to restrict remote frame connections to, you can set up a remote access password. You can password-protect hosted instruments too, by setting a password on the host PC. Because any user on the network with the *Agilent Logic Analyzer* application software installed can force any other user off of a frame, you may wish to protect your local system with a password to prevent this from happening.

NOTE For multiframe logic analysis systems, the remote access password must be the same on every frame. If this is not the case, you will not be able to connect to to the multiframe set. If a password is not set (blank) on one frame, then you will be able to connect to the entire set of frames so long as the remaining frames have identical passwords or a blank password. In other words, a blank password is a don't care condition.

On the logic analysis systems that you want to restrict remote connections to:

1 From the Windows Start menu, choose **Start>Programs>Agilent Logic Analyzer>Utilities>Remote Access Password Utility**.

   (You can also run this utility by clicking **Set Local Password** in the Select System to Use dialog (see page 479).)

2 In the Remote Access Password Utility dialog, if a password is currently set, click **Clear Password**.

3 Enter the new password in the **Enter New Password** and **Re-enter New Password** fields; then, click **Set Password**.

4 Click **OK** to make the password changes and close the dialog.

Password changes take effect immediately; however, they do not affect users currently connected to the local frame.

Clicking **Cancel** closes the dialog without making any password changes.

Notes:

- The remote access password is completely separate from Windows user logon passwords. Setting or clearing remote access passwords does not affect Windows user logon passwords.
- Remote access passwords are encrypted using a one-way encryption algorithm and securely stored.
- In order to set or clear remote access passwords using this utility, the currently logged-on user must have administrative credentials.
- Establishing a remote access password does not password-protect access via Windows Remote Desktop.

See Also

- Returning to Online Analysis (see page 63)

5
Setting Up the Logic Analyzer

Configuring Logic Analyzer Modules

A logic analyzer *module* is a logical collection of channels on a single timebase and trigger. A module can be a single *card* (see page 648) or several cards, and a single card or several card module can be split into two modules. Modules give you the flexibility to:

- Increase logic analyzer channel count by using more than one card.
- Probe buses that have different time domains by splitting a single card into two modules.

Combining cards to increase channel count is done when installing cards into a *frame* (see page 649). Cables are connected between the cards. For more information, see the "*16900-Series Logic Analysis System Installation Guide*".

Splitting a single card (or cards that were combined during installation) is done from the Setup menu or in the Overview window. To split logic analyzer channels into two modules:

1 Choose **Setup>(Logic Analyzer Module)>Split Analyzer...**.

2 In the Split Analyzer Setup dialog (see page 489), drag the channel assignment slider to specify the number of channels in each analyzer.

   If you'd like to assign particular *pods* (see page 651) or *pod pairs* (see page 651) to a module, check **Advanced Pod Assignment Mode**.

3 Click **OK**.

See Also

- To disable and enable modules (see page 76)
- To unsplit a split analyzer (see page 78)
- Memory Depth and Channel Count Trade-offs (see page 374)

To disable and enable modules

By default, all modules in a logic analysis system are enabled; however, you can disable modules to stop them from participating in measurements.

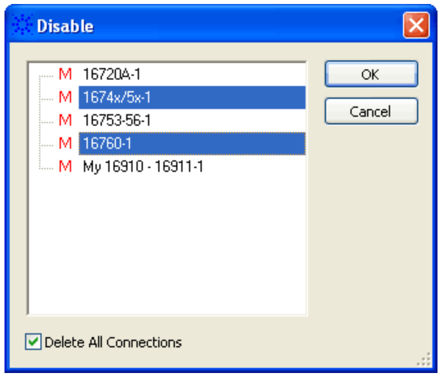
NOTE Disabling a module in a split analyzer causes both modules of the split analyzer to be disabled.

To disable modules

1 In the Overview window, choose **Disable...** from the module's menu.

   Or, choose **Setup>(Logic Analyzer Module)>Disable...** from the main menu.

2 In the Disable dialog:



a Select the modules you want to disable.

b Check **Delete All Connections** if you want to delete module connections to tools and windows. This causes tools and windows connected only to the disabled modules to be deleted as well.

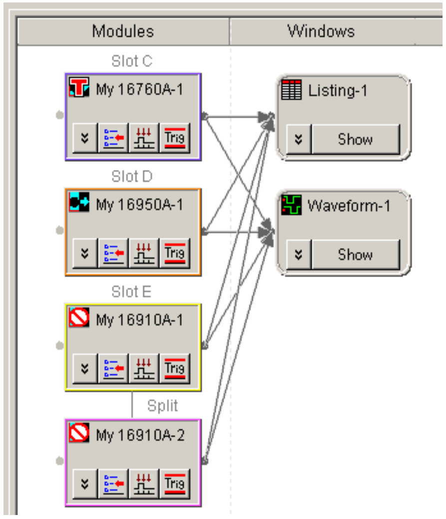
Uncheck **Delete All Connections** if you want to leave module connections to tools and windows. The disabled modules' buses and signals are hidden from tools and windows, but they will reappear when the modules are re-enabled.

c Click **OK**.

When a module is disabled:

- It no longer runs or sends data to downstream tools or windows, and no data is saved to configuration files.
- The buses and signals defined in the module are hidden from windows and tools.
- You cannot change the setup of the module.

In the Overview widow, disabled modules have the icon:

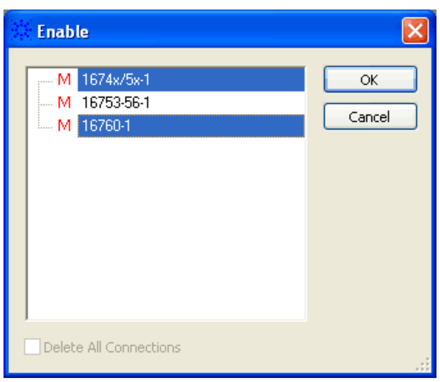


To enable modules

1 In the Overview window, choose **Enable...** from the module's menu.

Or, choose **Setup>(Logic Analyzer Module)>Enable...** from the main menu.

2 In the Enable dialog:



a Select the modules you want to enable.

b Click **OK**.

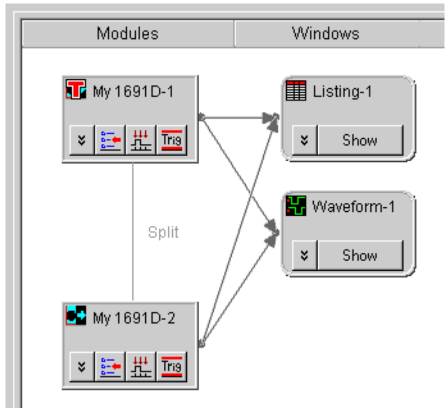
See Also

- Configuring Logic Analyzer Modules (see page 76)

To unsplit a split analyzer

When logic analyzer pods have been split into two modules, you can undo the split and recombine the pods into a single module again.

You can identify a split analyzer in the Overview window by the word "Split" between the modules and an extra line between them.



When looking at the Overview widow, the bottom module shown is the one that will be deleted in an unsplit.

CAUTION

When you unsplit an analyzer, all the bus/signal definitions you have set up for the module are deleted throughout the system, including in Windows, triggers, filters, etc. Be sure you are not using the split analyzer before you delete it.

If you are not sure how the unsplit will affect your setup, save your configuration before you unsplit; you cannot "undo" after an unsplit.

To unsplit a split analyzer:

1 Choose **Setup>(Logic Analyzer Module)>Unsplit Analyzer...**.

2 In the warning dialog that appears, click **Yes**.

See Also

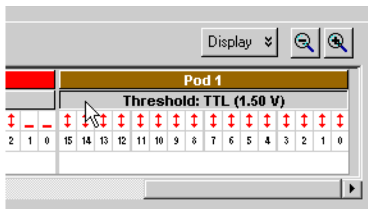
- Configuring Logic Analyzer Modules (see page 76)

Setting the Logic Analyzer Threshold Voltage

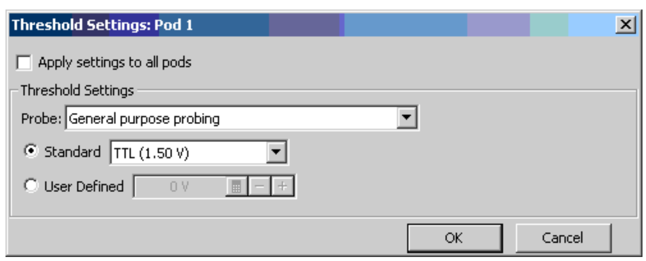
It is very important that you specify a threshold voltage that matches what your device under test is using. Incorrectly specified threshold voltages result in incorrect data.

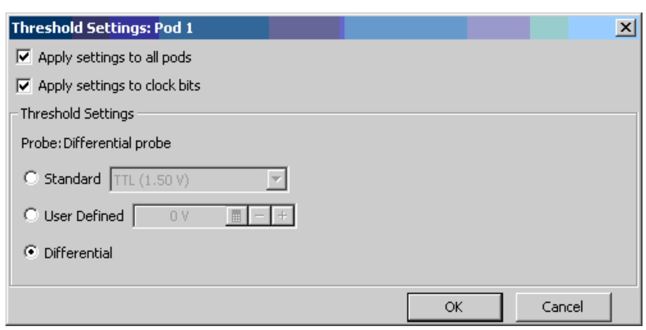
1 From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**.

2 In the Buses/Signals Setup dialog, click any **Threshold** button. The Threshold buttons are located under the Pod or Clocks label.

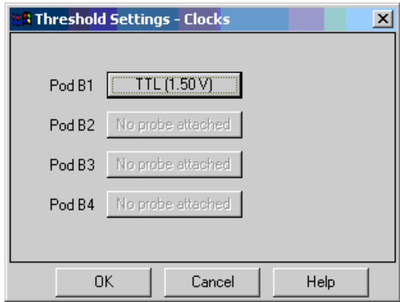


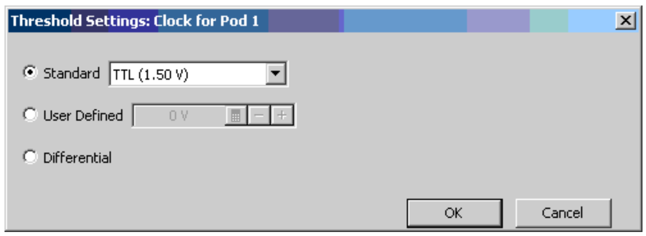
3 In the Threshold Settings dialog:





Some logic analyzers let you specify threshold voltages for clock channels individually. This may be useful in situations, for example, where the clock channels are probing differential signals while the data channels are probing single-ended signals.





a Check **Apply settings to all pods** if you want the settings to apply to all pods; otherwise, the settings apply only to the selected pod.

b Check **Apply settings to clock bits** if you want the settings to apply to clock bits; otherwise, the settings apply only to the data channels.

c Select the **Probe** type; this may affect the settings that can be selected.

d Specify the threshold level. Choices are:

- Standard — you can select from a list of pre-defined threshold levels (which are shown in parentheses).
- User Defined — you can enter a value from -6.00 to 6.00 V.
- Differential.

See Also

- Pod and Channel Naming Conventions (see page 372)

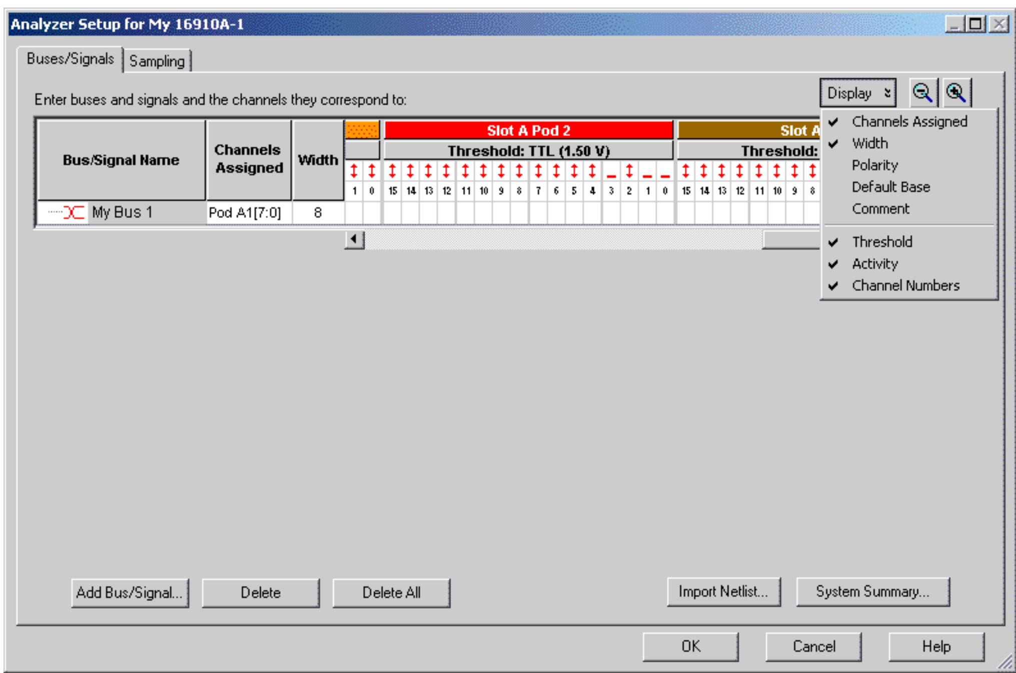
Defining Buses and Signals

Before you can use the logic analyzer, you must define buses and signals by:

1 Adding bus/signal names.

2 Assigning logic analyzer channels to bus/signal names.

Click  in the analyzer setup toolbar, or choose **Setup>(Logic Analyzer Module)>Bus/Signal...** from the menu bar to open the Buses/Signals setup tab (see page 448).



The following tasks are performed in the Buses/Signals setup tab:

- To add a new bus or signal (see page 83)
- To delete a bus or signal (see page 84)
- To rename a bus or signal (see page 85)
- To rename the bits of a bus (see page 86)
- To assign channels in the default bit order (see page 88)
- To assign channels, selecting the bit order (see page 89)
- To use clock channels as extra data channels (see page 90)
- To define buses and signals by importing netlist files (see page 91)
- To reorder bits by editing the Channels Assigned string (see page 92)
- To set the default number base (see page 94)

- To set polarity (see page 95)
- To add user comments (see page 95)
- To add a folder (see page 96)
- To alias a bus/signal name (see page 96)
- To sort bus/signal names (see page 96)

Through the **Display** button, you can select what bus/signal setup information is displayed (channels assigned, width, polarity, default base, comment, threshold, activity, or channel numbers).

The bus and signal icons in the **Bus/Signal Name** column are normally red, but they turn gray if the bus/signal is locked by an inverse assembler.

NOTE In previous versions of the *Agilent Logic Analyzer* application, the Buses/Signals setup tab had a **Define Probes...** button; now, probes are defined differently (see "To define probes" (in the online help)).

See Also

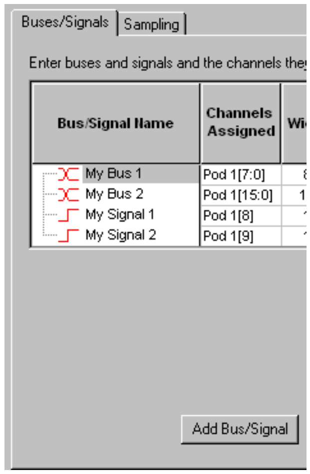
- Setting the Logic Analyzer Threshold Voltage (see page 80)
- Why Are Pods Missing? (see page 373)

To add a new bus or signal

The add bus/signal feature allows you to add new buses and signals to the configuration. Once added to the configuration, the new bus/signal is automatically inserted into the data displays and also becomes available in any bus/signal insert function.

1. From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**.
2. Select **Add Bus/Signal** to add a new bus or signal.
3. The new bus/signal will appear with a system generated default name. Rename (see page 85) the new bus/signal if desired.

NOTE Before a new bus/signal can be added to the configuration, at least one channel must be assigned to the bus/signal.



See Also

- To delete a bus or signal (see page 84)
- To rename a bus or signal (see page 85)
- To assign channels in the default bit order (see page 88)
- To assign channels, selecting the bit order (see page 89)
- Defining Buses and Signals (see page 82)

To delete a bus or signal

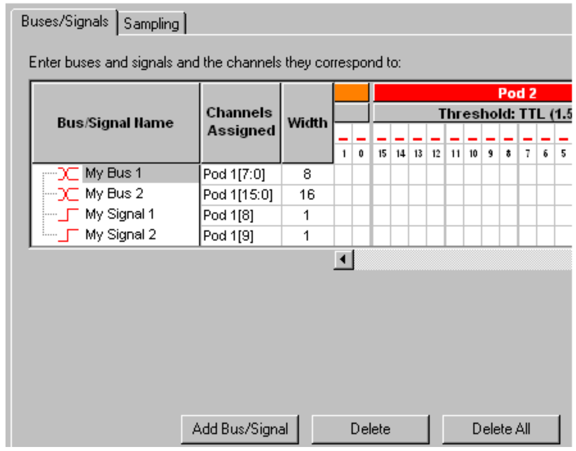
The delete bus or signal feature allows you to remove buses and signals individually or all at once. The delete bus or signal feature is accessed through the setup menu or the setup toolbar.

- To delete an individual bus or signal (see page 84)
- To delete all buses and signals (see page 85)

To delete an individual bus or signal

1. From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**.
2. Highlight the bus or signal you want to delete.

3 Click **Delete.**



To delete all buses and signals

1 From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**.

2 Click **Delete All**.

NOTE

Some tools "lock" buses and signals because they use the bus or signal to produce their own output. Delete and Delete All will not delete these locked buses and signals. A locked bus or signal has a gray icon to the left of the name instead of a red icon.

See Also

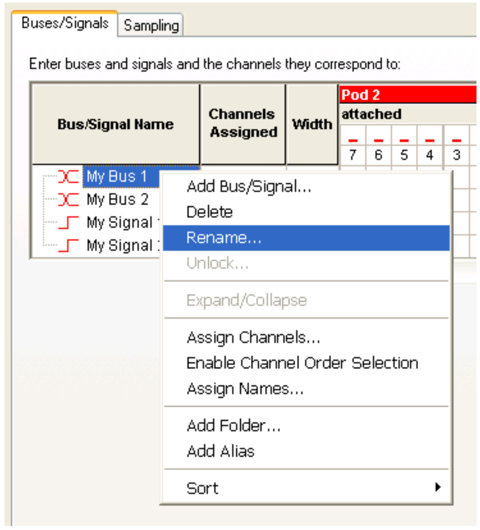
- Defining Buses and Signals (see page 82)

To rename a bus or signal

The rename bus/signal feature allows you to change bus and signal names. All channel, pod, and clock assignments for the renamed bus/signal remain unchanged.

1 From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**, or click the icon in the setup toolbar (see page 422).

2 Right-click the bus or signal name and choose **Rename...**



3 Enter the new bus or signal name.

4 Select **OK**.

See Also

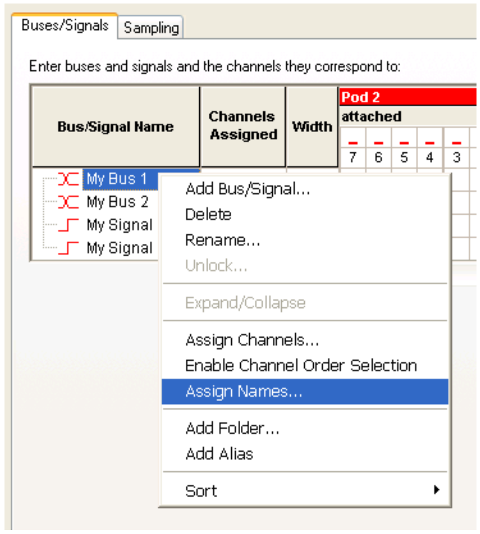
- To add a new bus or signal (see page 83)
- To delete a bus or signal (see page 84)
- To rename the bits of a bus (see page 86)
- Defining Buses and Signals (see page 82)

To rename the bits of a bus

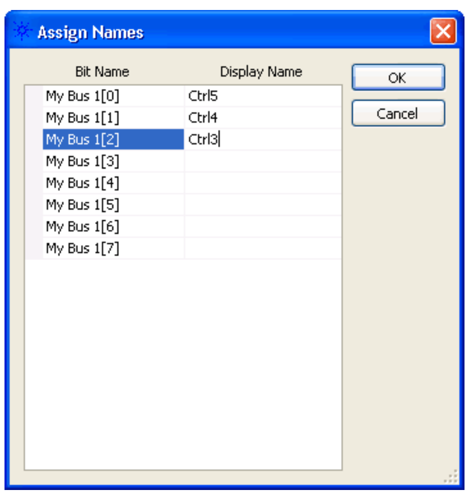
When a bus is expanded in the Waveform display window, the names of the signals within the bus are like Bus[0], Bus[1], etc., by default. However, you can assign your own names to the bits within a bus.

1 From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**, or click the icon in the setup toolbar (see page 422).

2 Right-click the bus name and choose **Assign Names...**.

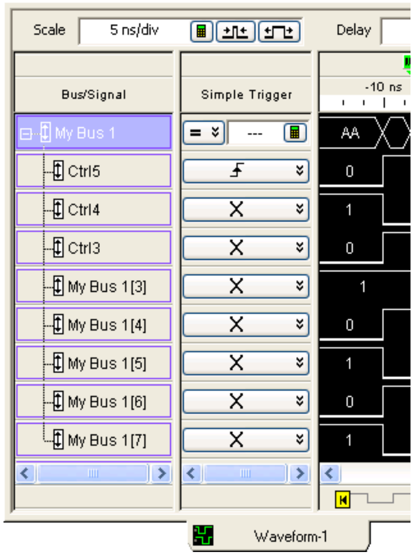


3 In the Assign Names dialog, enter the new names of bits within the bus.



4 Click **OK**.

Now, you see your names when the bus is expanded in the Waveform window.



See Also

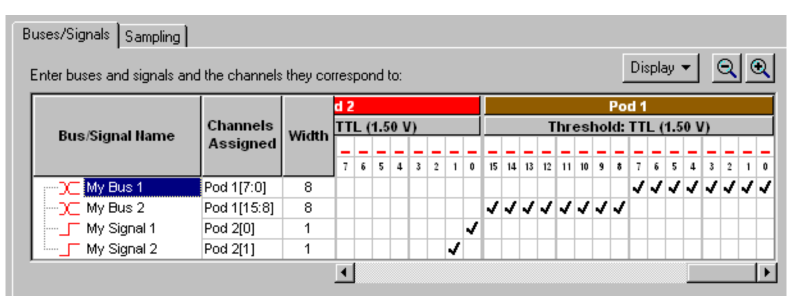
- To rename a bus or signal (see page 85)
- To add a new bus or signal (see page 83)
- Defining Buses and Signals (see page 82)

To assign channels in the default bit order

To make the logic analyzer display match your system's design, assign the physical channels of the logic analyzer to bus and signal names.

1. From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**.
2. In the Buses/Signals tab, select squares in the grid to assign channels to bus and signal names. For each signal probed in your device under test, you should have a black check mark mapping the channel to a pod and to a signal name in the interface.

   Example: In the picture below, channels 0-7 (pod 1) are mapped to My Bus 1, channels 8-15 (pod 1) are mapped to My Bus 2, and channels 8 and 9 (pod 2) are mapped to My Signal 1 & 2, respectively.



TIP

If clock channels are not connected to clock signals, they can be used as extra data channels. Clock channels are grouped together after the last pod in the channel assignment area.

See Also

- To define buses and signals by importing netlist files (see page 91)
- To reorder bits by editing the Channels Assigned string (see page 92)
- Pod and Channel Naming Conventions (see page 372)

To assign channels, selecting the bit order

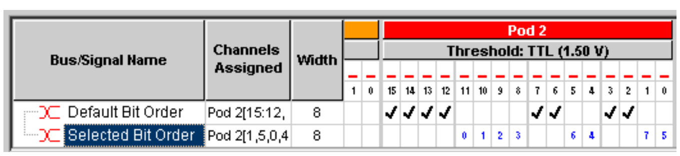
In cases where buses in the device under test haven't been probed with consecutive logic analyzer channels, you can assign channels to a bus name in a selected bit order.

1 From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**.

2 In the Buses/Signals tab, right-click the bus name, and choose **Enable Channel Order Selection**.

3 Start selecting squares in the grid to assign channels from the low order bit of the bus to the high order bit.

The bit numbers are displayed as you select squares.

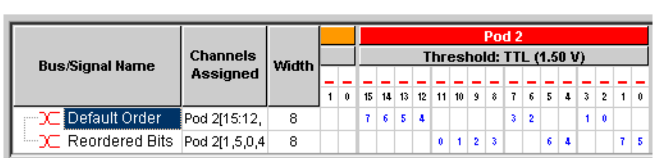


NOTE

When you select a bit order other than the default, you can only trigger on a sample equal to (=) or not equal (!=) to some value on that bus. You lose the ability to trigger on a sample less than (<), greater than (>), less than or equal to (<=), or greater than or equal to (>=) some value, and you lose the ability to trigger on a sample "in range" or "not in range" of two values.

To reset the default bit order

The default bit order of assigned channels has higher bits on the left and lower on the right (in the Bus/Signal Setup dialog).



To reset to the default bit order:

- Right-click the bus name, and uncheck **Enable Channel Order Selection**.

See Also

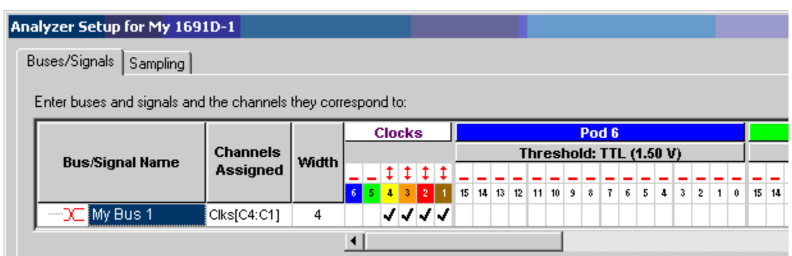
- To define buses and signals by importing netlist files (see page 91)
- To reorder bits by editing the Channels Assigned string (see page 92)
- Pod and Channel Naming Conventions (see page 372)

To use clock channels as extra data channels

When clock channels are not used for state mode sampling clock inputs, they can be used as extra data channels and assigned to bus/signal names just like ordinary data channels (see To assign channels in the default bit order (see page 88) or To assign channels, selecting the bit order (see page 89)).

NOTE When clock channels are used for state mode sampling clock inputs, it is not useful to assign them to bus/signal names.

Each pod in a logic analyzer module has a clock channel. In the Buses/Signals Setup dialog, all the clock channels are grouped together in a virtual **Clocks** pod. (Only ordinary data channels appear under the columns for each pod.)



NOTE There is no separate physical clock pod. Each pod has a single clock channel.

The clock pod can grow to include as many channels as there are pods in the system. In other words, the clock pod can have more than 16 channels if there are more than 16 pods.

In the **Channels Assigned** string, the clock pod name is "Clks" and the channels are named "C1", "C2", etc.

See Also

- To reorder bits by editing the Channels Assigned string (see page 92)
- Pod and Channel Naming Conventions (see page 372)

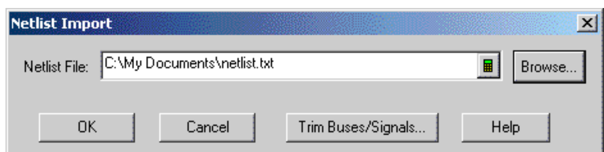
To define buses and signals by importing netlist files

You can create bus/signal names and assign logic analyzer probe channels by importing netlist files. These netlist files come from the Electronic Design Automation (EDA) tools used to design the device under test, and they contain information about the signals on the connectors built into the device under test for the logic analyzer probes.

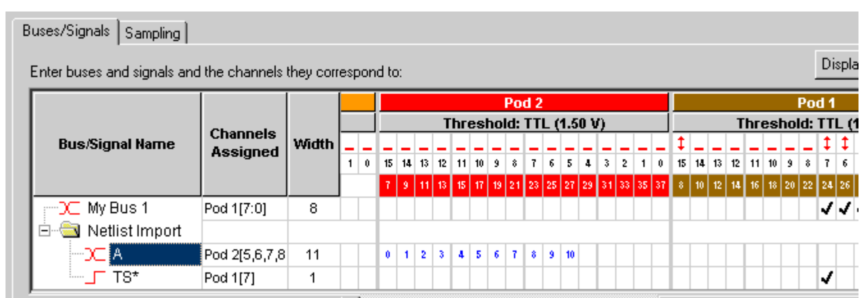
1 If you haven't already defined probes, choose **Setup>(Logic Analyzer Module)>New Probe>General Purpose Probe Set** and define the probes whose connectors are mapped in the netlist file (see "To define probes" (in the online help)).

2 In the Bus/Signal Setup dialog, click **Netlist Import...**.

3 Then, enter the netlist file to import bus/signal assignments from, and click **OK**.



After importing netlist files, connector pin numbers are displayed in the Bus/Signal Setup dialog.



Imported bus/signal definitions are placed in the "Netlist Import" folder.

CAUTION The "Netlist Import" folder is deleted and re-created on each import. If you want to keep definitions from the "Netlist Import" folder, either rename the folder or move bus/signal definitions out of the folder before the next netlist import.

Example Line from Netlist File: Netlist files created by Electronic Design Automation (EDA) tools have lines in the following format:

NET '/Bus1(3)' J1-7

Where:

- **Bus1** = Four bit bus.
- **(3)** = Bit 3.
- **J1-7** = Connector J1, pin 7.

See Also

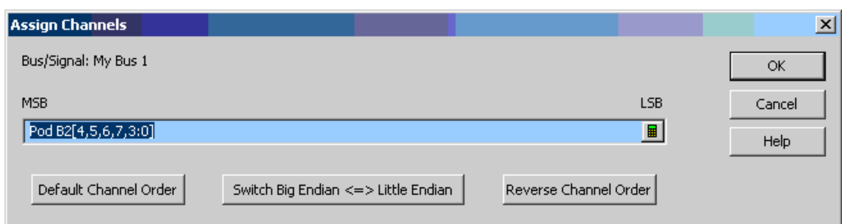
- To assign channels in the default bit order (see page 88)
- To assign channels, selecting the bit order (see page 89)
- To reorder bits by editing the Channels Assigned string (see page 92)
- Pod and Channel Naming Conventions (see page 372)

To reorder bits by editing the Channels Assigned string

You can change the order of the bits in a bus name (assigned in either the default order (see page 88) or a selected order (see page 89)) by editing the **Channels Assigned** text string.

1 In the Buses/Signals tab of the Analyzer Setup dialog, click the **Channels Assigned** to the bus name.

2 In the Assign Channels dialog, enter the appropriate order of bits in the bus.



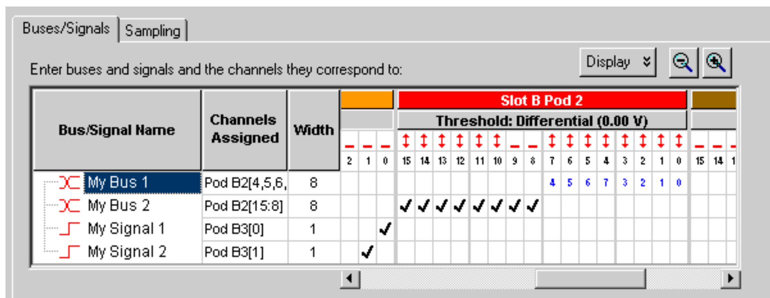
Example	Description
Pod B1[0]	Signal consisting of the first channel in the first pod of slot B.
Pod B1[15:0]	Bus consisting of all sixteen channels in Pod B1 in default order.
Pod B1[7:0], Pod B2[15:8]	Bus with seven channels from first pod in slot B followed by seven channels from second pod in slot B.
Pod B1[7:0,15:8]	Big endian, little endian switch on a 16-bit bus.
Pod B1[0,1,2,3]	Bus with bits in reverse order.
Clks[C2:C1], Pod B1[0], Pod B2[0]	Four bit bus including two clock pod channels.
Clks[C2M:C1S], Pod B1M[0], Pod B1S[0]	Four bit bus with demultiplex.

See Pod and Channel Naming Conventions (see page 372) to understand naming conventions like "Pod B2".

You can easily **Switch Big Endian <=> Little Endian** or **Reverse Channel Order** by clicking these buttons.

3 Click **OK**.

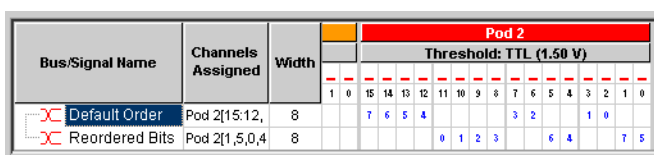
Channel numbers are displayed for reordered bits in the Bus/Signal Setup dialog.



NOTE When bits have been reordered, you can only trigger on a sample equal to (=) or not equal (!=) to some value on that bus. You lose the ability to trigger on a sample less than (<), greater than (>), less than or equal to (<=), or greater than or equal to (>=) some value, and you lose the ability to trigger on a sample "in range" or "not in range" of two values.

To reset the default bit order

The default bit order of assigned channels has higher bits on the left and lower on the right (in the Bus/Signal Setup dialog).



To reset to the default bit order:

1 Click the **Channels Assigned** to the bus name.

2 In the Assign Channels dialog, click **Default Channel Order**.

3 Click **OK**.

See Also

- To assign channels in the default bit order (see page 88)
- To assign channels, selecting the bit order (see page 89)
- Pod and Channel Naming Conventions (see page 372)

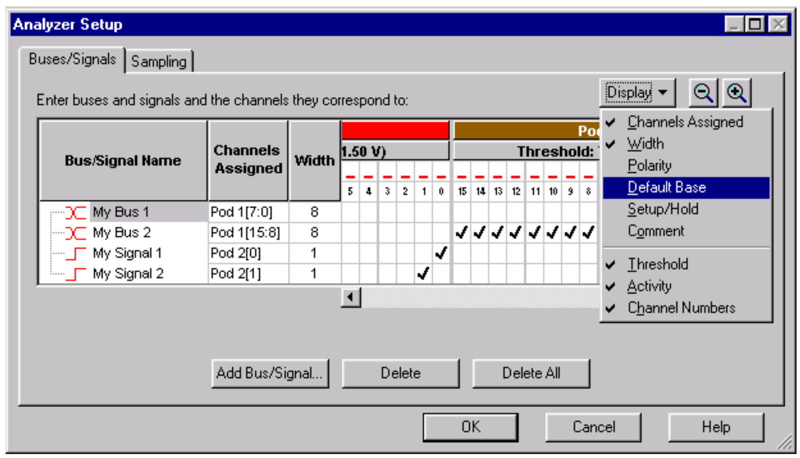
To set the default number base

You can set the default number base for a bus when you create the bus. The default base is used to display bus and signal values in the listing (see page 230) and waveform (see page 218) views. Default base only affects new buses and signals; if you change default base for an existing bus or signal you will not see a change unless you add a new copy of the bus or signal to a listing or waveform view.

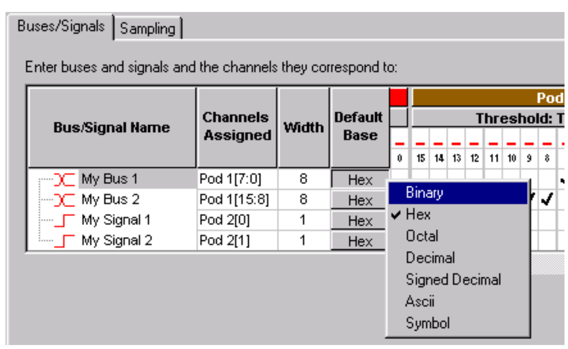
1 From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**.

2 In the bus/signal setup dialog, select **Display**.

3 Select **Default Base**.



4 To change the default base for a bus or signal, click the default base value.



5 Select a new value.

6 Click **OK** to close the bus/signal dialog.

To set polarity

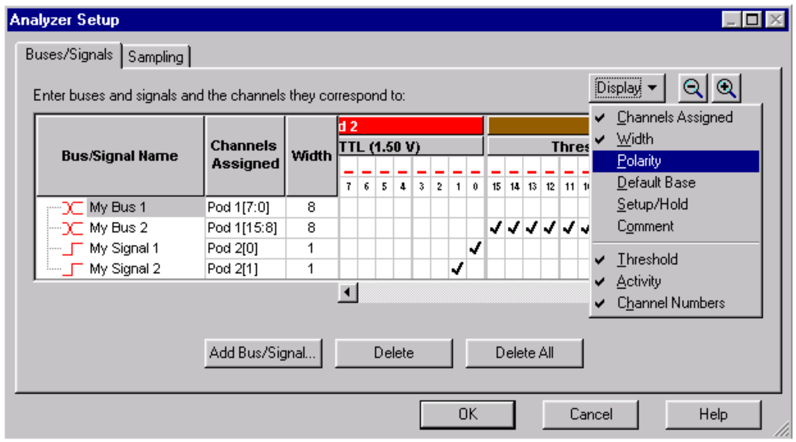
You can define buses and signals to display with negative or positive polarity. This affects the display of values and waveforms. When a bus or signal is set to negative polarity, an incoming high voltage will be shown with a low waveform and a logical value of 0. The polarity is reflected in all places that use values, such as trigger and symbols.

The default polarity is positive (high = 1).

1 From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**.

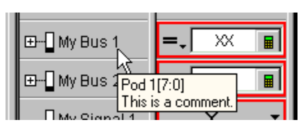
2 In the bus/signal setup dialog, select **Display**.

3 Select **Polarity**.



4 In the polarity column that appears, toggle between + (positive) and — (negative).

To add user comments



You can attach comments to buses and signals. The comments show up in the tool tip when you hover the mouse over a bus or signal name in both the waveform and listing windows.

1 From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**.

2 In the Buses/Signals setup tab that appears, select **Display**.

3 Select **Comment**. A new column labeled Comment appears.

4 In the Comment column, type your comment for the bus or signal.

5 Click **OK** to close the Analyzer Setup dialog.

NOTE Comments are intended as a descriptor to embellish a bus/signal name and not as a notepad. Comments can be up to 64 character in length.

To add a folder

The **Add Folder...** feature adds a windows style folder to the bus/signal list. Use folders to help organize bus and signal names when using many bus/signal names with inverse assemblers.

1 From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**.

2 Right-click on a bus/signal name, then select **Add Folder.**

3 The new folder appears directly below the highlighted name. By default, the new folder has a system generated default name. If desired, rename (see page 85) the new folder in the same way you would a bus/signal name.

See Also
- To alias a bus/signal name (see page 96)

To alias a bus/signal name

The **Add Alias...** feature adds an exact duplicate bus or signal name (same channel, polarity, etc. assignments). Use alias names along with folders (see page 96) to help organize the many bus and signal names with inverse assembly.

1 From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**.

2 Right-click on the desired bus/signal name, then select **Add Alias.**

3 The new alias name appears directly below the highlighted name. The new alias name can be renamed (see page 85), however, the new name will also be applied to the original name.

See Also
- To add a folder (see page 96)

To sort bus/signal names

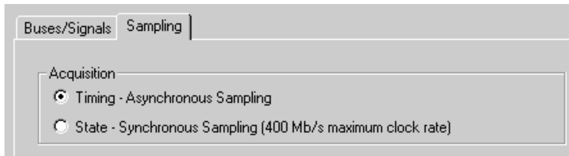
You can sort bus/signal names and folder names to help organize them.

1 From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**.

2 Right-click on one of the bus/signal or folder names to be sorted; then, select either **Sort>Ascending** or **Sort>Descending**.

See Also
- To add a folder (see page 96)

Choosing the Sampling Mode



The Sampling tab is accessed through the menu bar's **Setup>(Logic Analyzer Module)>Timing/State (Sampling)...** item. The Sampling setup tab is used to select and configure the acquisition mode.

In the **Timing - Asynchronous Sampling** acquisition mode, you set the sampling option and the sampling period. The device under test is sampled at regular intervals (the sampling period).

In the **State - Synchronous Sampling** acquisition mode, you set the sampling option, you set up the clocking signal(s) from the device under test that tells the logic analyzer when to sample data, and you adjust sampling positions on each channel relative to the sampling clock to make sure data is sampled when it is valid.

In both state and timing mode, you can set the acquisition (memory) depth and the position of the trigger event within the acquisition memory.

Some logic analyzers have the timing zoom feature which collects additional high-speed timing data around the logic analyzer trigger.

The following tasks are performed in the Sampling setup tab.

- Selecting the Timing Mode (Asynchronous Sampling) (see page 98)
  - To select the timing acquisition mode (see page 98)
  - To select the timing sampling option (see page 98)
  - To set the timing mode sampling period (see page 99)
- Selecting the State Mode (Synchronous Sampling) (see page 100)
  - To select the state acquisition mode (see page 100)
  - To select the state sampling option (see page 100)
  - Selecting the State Sampling Clock Mode (see page 101)
  - To set up the state sampling clock (see page 106)
  - To automatically adjust state sampling positions and threshold voltages (see page 107)
  - To manually adjust state sampling positions (see page 110)
- In Either Timing Mode or State Mode (see page 111)
  - To specify the trigger position (see page 111)

    - To set acquisition memory depth (see page 112)
- Using Timing Zoom (see page 112)
    - To turn timing zoom on or off (see page 114)
    - To specify the timing zoom sample period (on some logic analyzers) (see page 114)
    - To specify the timing zoom trigger position (see page 114)
    - To align timing zoom in a split analyzer (see page 115)

See Also
- Memory Depth and Channel Count Trade-offs (see page 374)

Selecting the Timing Mode (Asynchronous Sampling)

In *timing mode*, the logic analyzer samples asynchronously, based on an internally-generated sampling clock.

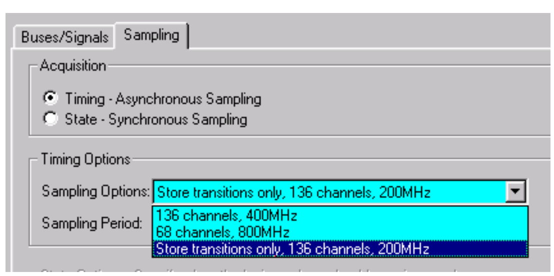
- To select the timing acquisition mode (see page 98)
- To select the timing sampling option (see page 98)
- To set the timing mode sampling period (see page 99)

To select the timing acquisition mode

1 From the menu bar select **Setup>(Logic Analyzer Module)>Timing/State (Sampling)...**, or click the icon from the setup toolbar (see page 422).

2 In the Acquisition area of the Sampling setup dialog, select the **Timing - Asynchronous Sampling** option.

To select the timing sampling option



In the timing (asynchronous) sampling mode, you can:

- Trade-off channel width for faster sampling. That is, if you want a smaller sampling period, you can set up the logic analyzer to use half of the maximum channels available.
- Get the most out of acquisition memory and measure an overall greater amount of time by choosing to store only transitions or other store-qualified patterns.

NOTE Changing the sampling option will affect the sampling period and may affect bus assignments.

To select the timing mode sampling option:

1 From the menu bar, select **Setup>(Logic Analyzer Module)>State/Timing (Sampling)...**.
2 Select **Timing** acquisition mode. Timing Options become selectable.
3 Select the sampling option you prefer. Your channel count may be different depending on the logic analyzer model.

Full Channel Timing Mode (see page 573)	Default. All channels are available.
Half Channel Timing Mode (see page 573)	Uses one pod from each pod pair.
Transitional / Store Qualified Timing Mode (see page 573)	Provides maximum duration of acquisition because data is only stored when a change from the last value is detected. See transitional timing (see page 376).

See Also

- Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 573)

To set the timing mode sampling period

In timing mode, a logic analyzer takes a sample of the device under test's activity once per sample period. You can set this sample period in the Sampling Setup tab.

1 From the menu bar select **Setup>(Logic Analyzer Module)>Timing/State (Sampling)...**, or click the  icon from the setup toolbar (see page 422).
2 Select **Timing - Asynchronous Sampling**.
3 In the Timing Mode area of the Sampling setup dialog, increase or decrease the Sample Period.

NOTE To capture signal level changes reliably, the sample period should be less than half of the period of the fastest signal you want to measure. Time interval measurements are made by counting the number of samples in the desired waveform area. These measurements are made to a +/- one sample error, so measurement accuracy is improved if the number of samples is maximized.

See Also

- Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 573)

Selecting the State Mode (Synchronous Sampling)

In *state mode*, the logic analyzer samples synchronously, based on a sampling clock signal from the device under test. Typically, the signal used for sampling in state mode is a state machine or microprocessor clock signal.

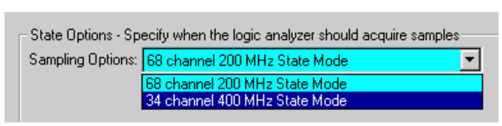
- To select the state acquisition mode (see page 100)
- To select the state sampling option (see page 100)
- Selecting the State Sampling Clock Mode (see page 101)
- To set up the state sampling clock (see page 106)
- To automatically adjust state sampling positions and threshold voltages (see page 107)
- To manually adjust state sampling positions (see page 110)

To select the state acquisition mode

1 From the menu bar select **Setup>(Logic Analyzer Module)>Timing/State (Sampling)...**, or click the  icon from the setup toolbar (see page 422).

2 In the Acquisition area of the Sampling setup dialog, select the **State - Synchronous Sampling** option.

To select the state sampling option



In the state (synchronous) sampling mode, the sampling option specifies the speed up to which the state mode sampling clock will match input clock edges from the device under test. You can trade-off triggering and clocking capability to allow faster state mode sampling speeds.

To select the state mode sampling option:

1 From the menu bar, select **Setup>(Logic Analyzer Module)>State/Timing (Sampling)...**.

2 Select the **State** acquisition mode. State Sampling Options becomes selectable.

3 Select the sampling option you prefer.

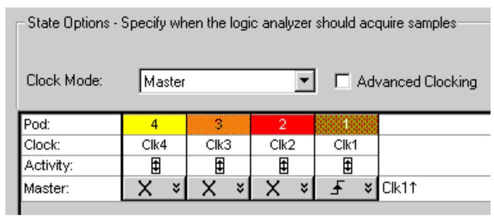
General State Mode (see page 574)	Default.
Turbo State Mode (see page 574)	Faster state mode sampling speeds are supported, but triggering and clocking are restricted.

See Also

- Logic Analyzer Notes, State Mode Sampling Options (see page 574)

Selecting the State Sampling Clock Mode

The state sampling clock inputs let signals from the device under test specify when data should be captured.



The state sampling clock *mode* specifies how the clock inputs are used for sampling. There are four state sampling clock modes to choose from:

- Master Only (see page 101) — all pods sampled on one master clock.
- Master/Slave (see page 102) — some pods sampled on master clock; other sampled on slave clock.
- Demultiplex (see page 102) — one pod of pair sampled on master and slave clocks.
- Dual Sample (see page 103) — one pod of pair sampled on one master clock but with different delays.

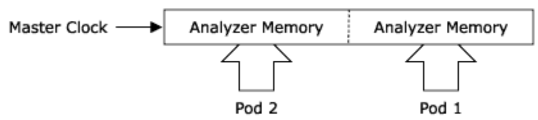
For instructions on setting up these state sampling clock modes, see:

- To set up the master only sampling clock mode (see page 103)
- To set up the master/slave sampling clock mode (see page 103)
- To set up the demultiplex sampling clock mode (see page 104)
- To set up the dual sample sampling clock mode (see page 105)

See Also

- To set up the state sampling clock (see page 106)
- To set up advanced clocking (see page 107)
- Pod and Channel Naming Conventions (see page 372)

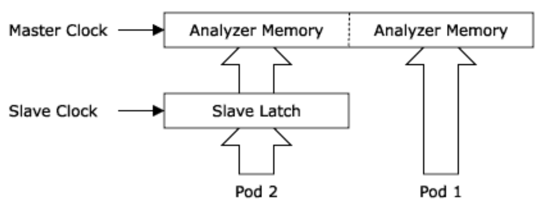
Master Only Sampling Clock Mode In the Master only state sampling clock mode, there is one sampling clock signal. When a clock edge occurs, data is captured and saved into one sample of logic analyzer memory.



See Also

- To set up the master only sampling clock mode (see page 103)

Master/Slave Sampling Clock Mode In the Master/Slave state sampling clock mode, you can save data captured on different clock edges into the same sample of logic analyzer memory.

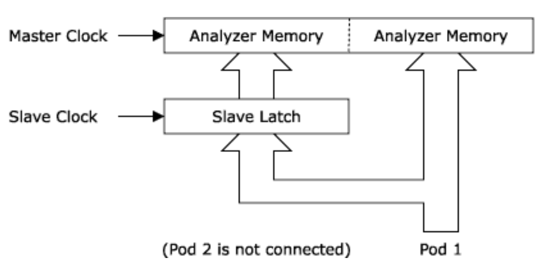


When the slave clock occurs, data captured on the pods that use the slave clock is saved in a slave latch. Then, when the master clock occurs, data captured on the pods that use the master clock, as well as the slave latch data, are saved into logic analyzer memory. If multiple slave clocks occur before the next master clock, only the most recently acquired slave data is saved into logic analyzer memory.

See Also

- To set up the master/slave sampling clock mode (see page 103)

Demultiplex Sampling Clock Mode In the Demultiplex state sampling clock mode, you can demultiplex data being probed by one pod into the logic analyzer memory that is normally used for two pods. Demultiplex mode uses the master and slave clocks to demultiplex the data.

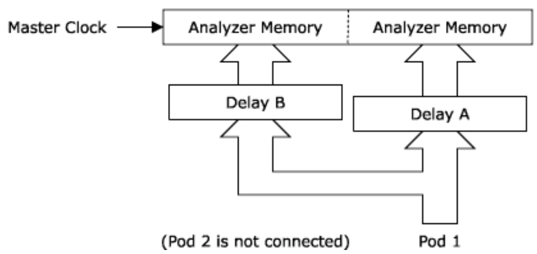


When the slave clock occurs, data captured on the pod is saved into the slave latch for the other pod in the pod pair. Then, when the master clock occurs, data captured on the pod, as well as the slave latch data, are saved in logic analyzer memory. As with master/slave mode, if multiple slave clocks occur before the next master clock, only the most recently acquired slave data is saved into logic analyzer memory.

See Also

- To set up the demultiplex sampling clock mode (see page 104)

Dual Sample Sampling Clock Mode In the Dual Sample state sampling clock mode, you can save data captured using the master clock at each of two different sample times into the same sample of analyzer memory.



When the master clock occurs, data on the pod is sampled twice using two independent sampling positions. Each of the two sample positions can be set using the Thresholds and Sample Positions dialog (see page 497).

The Dual Sample mode is often used to capture DDR memory bus activity using the common bus clock as the master clock. One sample position is used to capture write data and another is used to capture read data.

See Also

- To set up the dual sample sampling clock mode (see page 105)

To set up the master only sampling clock mode

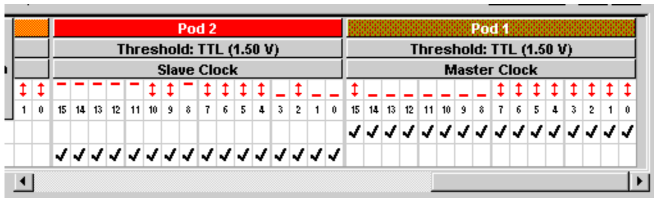
1 From the menu bar, select **Setup>(Logic Analyzer Module)>Timing/State (Sampling)...**.
2 Select **State**.
3 In the State Options, change Clock Mode to **Master**.
4 Set up your master clock (see To set up the state sampling clock (see page 106)).

See Also

- Master Only Sampling Clock Mode (see page 101)

To set up the master/slave sampling clock mode

1 From the menu bar, select **Setup>(Logic Analyzer Module)>Timing/State (Sampling)...**.
2 Select **State**.
3 In the State Options, change Clock Mode to **Master/Slave/Demux**.
4 Set up your master and slave clocks (see To set up the state sampling clock (see page 106)).
5 Select the **Buses/Signals** tab.
6 For each pod, click the clock button under the pod heading and choose either **Master Clock** or **Slave Clock**.



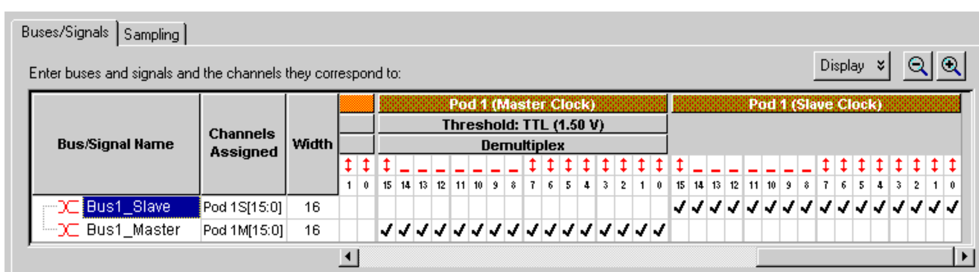
See Also

- Master/Slave Sampling Clock Mode (see page 102)

To set up the demultiplex sampling clock mode

NOTE To capture demultiplexed data, use only one pod of a pod pair.

1 From the menu bar, select **Setup>(Logic Analyzer Module)>Timing/State (Sampling)...**.
2 Select the **State** acquisition mode.
3 In the State Options, change Clock Mode to **Master/Slave/Demux**.
4 Set up your master and slave clocks (see To set up the state sampling clock (see page 106)).
5 Select the **Buses/Signals** tab.
6 Click the clock button under the pod heading and choose **Demultiplex**.



The display of the pod and the other pod in the pair changes. For example, if you set Pod 1 to demultiplex, Pod 2 goes away and you see two Pod 1 columns. The first Pod 1 column is labeled Pod 1 (Master Clock), and the second column is Pod 1 (Slave Clock).

Note that you can adjust sampling positions relative to the master clock and to the slave clock by assigning master and slave bus/signal names. (Note the "M" and "S" suffixes on pods in the **Channels Assigned** column to indicate "master clock" and "slave clock".) For more information on adjusting sampling positions, see To automatically adjust state sampling positions and threshold voltages (see page 107) or To manually adjust state sampling positions (see page 110).

See Also

- Demultiplex Sampling Clock Mode (see page 102)

To set up the dual sample sampling clock mode

NOTE To capture dual sample data, use only one pod of a pod pair.

1 From the menu bar, select **Setup>(Logic Analyzer Module)>Timing/State (Sampling)...**.

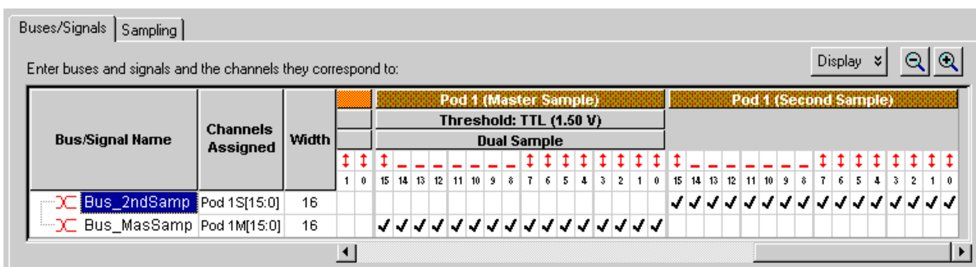
2 Select **State**.

3 In the State Options, change Clock Mode to **Dual Sample**.

4 Set up your master clock (see To set up the state sampling clock (see page 106)).

5 Select the **Buses/Signals** tab.

6 Click the clock button under the pod heading, and choose **Dual Sample**.



The display of the pod and the other pod in the pair changes. For example, if you set Pod 1 to dual sample, Pod 2 goes away and you see two Pod 1 columns. The first Pod 1 column is labeled Pod 1 (Master Sample), and the second column is Pod 1 (Second Sample).

NOTE Note that timing zoom data is only valid for the selected pod.

7 Assign bus/signal names to the channels in the master sample and to the channels the second sample.

Bus/signal names assigned to the master sample can have different sampling positions than the bus/signal names assigned to the second sample.

8 Adjust the state sampling positions differently for the bus/signals associated with the master sample and the buses/signals associated with the second sample (see To automatically adjust state sampling positions and threshold voltages (see page 107) or To manually adjust state sampling positions (see page 110)).

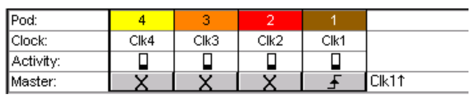
Note the "M" and "S" suffixes on pods in the **Channels Assigned** column to indicate "master sample" and "second sample".

See Also

- Dual Sample Sampling Clock Mode (see page 103)

To set up the state sampling clock

The state clock should be set to match the clock signal on your device under test. The logic analyzer can handle clock signals comprised of up to four lines. Clocks can be as simple as a single rising edge, or a complicated combination of edges and highs or lows.



In the picture above, the clocks refer to the clock signal lines on pods 1 through 4. Depending on model, your logic analyzer may have more pods. However, only the clock lines on the first 4 pods can be used to generate the state clock signal. Clock lines on extra pods can be used like normal data lines.

1 Attach logic analyzer pods to your device under test. Clock signals must be connected to the clock lines on pods 1 through 4.

2 From the menu bar, select **Setup>(Logic Analyzer Module)>Timing/State (Sampling)...**.

3 Select **State - Synchronous Sampling**. The State Options area becomes active.

4 Select the state clock mode (see page 101). Most measurements use only the master clock.

5 Set up a clock description to match the clock(s) in your device under test.

X	Don't care. Clock line not used in this clock.
	Rising edge.
	Falling edge.
	Both edges.
1	Qualifier - high.
0	Qualifier - low.

A clock description must have at least one edge.

See Also

- Selecting the State Sampling Clock Mode (see page 101)

- To automatically adjust state sampling positions and threshold voltages (see page 107)
- To manually adjust state sampling positions (see page 110)
- To set up advanced clocking (see page 107)

To set up advanced clocking If you want to specify more complex clock setups than you can with the normal Master or Slave selections (for example, if you want to use a specific clock channel both as an edge and a qualifier in the same clock description), you need to use advanced clocking.

1 From the menu bar, select **Setup>(Logic Analyzer Module)>State/Timing (Sampling)...**.
2 Select **State** mode. The state options become selectable.
3 Next to the clock mode, select **Advanced Clocking**. The clock controls are replaced by a button.
4 Select **Master Clock...** or **Slave Clock...** as appropriate.
5 In the Advanced Clocking Setup Dialog (see page 444), choose settings as appropriate.

   Clock channels can be used both as primary clocks and as clock qualifiers.
6 Click **OK** to close the dialog. The clock description in the Analyzer Setup window updates.

NOTE If you un-check advanced clocking, all qualifiers are erased.

See Also

- Pod and Channel Naming Conventions (see page 372)

To automatically adjust state sampling positions and threshold voltages

When adjusting the state mode sampling position with *eye finder*, the logic analyzer looks at signals from the device under test, figures out the threshold voltage that results in the widest possible data valid window, then figures out the location of the data valid window in relation to the sampling clock, and automatically sets the threshold voltage and sampling position.

Because *eye finder* automatically sets the sample position on individual channels, it can correct for the small skew effects caused by probe cables and circuit board traces. This makes the logic analyzer's setup/hold window smaller and lets you accurately capture data at higher clock speeds.

Eye finder requires:

- At least 10 transitions on each signal during its run. (You can use the advanced *eye finder* settings to cause longer or shorter runs.)
- All devices which can drive each signal should contribute to the stimulus.
- All device under test operating modes relevant to the eventual logic analysis measurement should contribute to the stimulus as well.

NOTE *Eye finder* measurements and normal logic analyzer measurements cannot run simultaneously.

To run eye finder

1 Probe the device under test by connecting the logic analyzer channels.

2 Assign bus/signal names to those logic analyzer channels.

3 Make sure that the device under test and the logic analyzer have warmed up to their normal operating temperatures.

4 Select the state (synchronous sampling) mode (see To select the state acquisition mode (see page 100)).

5 In the Sampling Setup dialog, click **Thresholds and Sample Positions...**.

6 In the Thresholds and Sample Positions dialog (see page 497), select the buses/signals on which you wish to run *eye finder*.

   You may want to run *eye finder* on channel subsets, for example, when certain bus signals transition in one operating mode (of the device under test) and other bus signals transition in a different operating mode.

7 Select the type of *eye finder* run you want:

   - **Auto Sample Position Setup** (performs a full time scan at the currently specified threshold voltage to determine the optimal sampling position).
   - **Auto Threshold and Sample Position Setup** (adjusts the threshold voltages while watching activity indicators to find the signal activity envelope and optimal threshold voltage setting; then, performs a full time scan at that threshold, to automatically determine the optimal sampling position).
   - **Eye Scan with Threshold and Sample Position Setup** (performs full time scans across the full signal activity envelope to display oscilloscope-like eye diagrams along with optimal threshold voltage and sampling position settings).
   - **Eye Scan with Sample Position Setup Only** (performs full time scans across the full signal activity envelope to display oscilloscope-like eye diagrams along with sampling position settings only).

8 Click **Run**.

After checking clock and qualifier inputs for activity and the appropriate thresholds, the *eye finder* measurement runs.

When *eye finder* finds more than one stable region on a channel, it uses the current sampling position as a hint about which stable region it should suggest a position for.

If *eye finder* picks the wrong stable region, you can expand the bus/signal and drag the Sampling Position bar or dotted line (blue in stable regions, red in transitioning regions) into the correct stable region. The suggested sampling position for that region will be shown (see How Selected/Suggested Positions Behave (see page 502)).

You can also adjust the threshold voltage setting by dragging the Threshold bar or dotted line. Note that this affects all channels on the same pod (and sometimes the clock input on the pod as well).

9 If you have moved the sampling position and wish to return to the suggested positions, go to the Thresholds and Sample Positions dialog, right-click on a bus/signal, and choose the **Set Sampling Position to Suggested** command.

If you have moved the threshold voltage setting and wish to return to the suggested positions, go to the Thresholds and Sample Positions dialog, right-click on a bus/signal, and choose the **Set Threshold to Suggested** command.

For more information on the *eye finder* measurement results, right-click on a bus/signal and choose **Properties...** to open the Eye Finder Properties dialog (see page 501). For more information on informational messages in the Thresholds and Sample Positions dialog, see Eye Finder Info Messages (see page 338).

Eye finder finds optimal threshold voltages and sample positions for the actual specific conditions -- amplitude, offset, slew rates, and ambient temperature. Therefore, you will get the best results by running *eye finder* under the same conditions that will be present when logic analysis measurements are made.

When running normal logic analyzer measurements, you will be warned if the sampling clock setup, clock thresholds, or sampling clock mode has changed since the last *eye finder* measurement.

To run eye finder repetitively

1 In the Thresholds and Sample Positions dialog, click **Advanced...**.
2 In the Eye Finder Advanced Options dialog (see page 500), select the **Run Mode** tab.
3 Check **Run Repetitively**.
4 Click **OK**.
5 In the Thresholds and Sample Positions dialog, click **Run**.

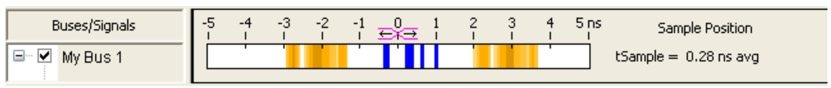
In the Thresholds and Sample Positions dialog, you can see how the stable and transitioning areas vary over time.

6 To stop the repetitive run, click **Stop**.

To view eye finder data as a bus composite

When you want a compressed, high-level view of the *eye finder* data:

1 In the Thresholds and Sample Positions dialog, right-click on the sampling position diagram for a bus, and choose the **View Bus As Composite** command.



Average sampling positions as well as stable and transitioning areas are displayed for the whole bus. This is the default. Stable areas show positions where every channel in the bus is stable.

To view eye finder data as a stack of channels

When you want more resolution in your view of the *eye finder* data:

1 In the Thresholds and Sample Positions dialog, right-click on the sampling position diagram for a bus, and choose the **View Bus As Stack Of Channels** command.

Individual sampling positions and stable and transitioning areas for all the channels in a bus are shown.

To clear eye finder measurement data

1 In the Thresholds and Sample Positions dialog, right-click on a bus/signal name, and choose **Clear Measurement**.

See Also

- Understanding State Mode Sampling Positions (see page 378)
- Eye Finder Advanced Options Dialog (see page 500)
- To manually adjust state sampling positions (see page 110)

To manually adjust state sampling positions

In the Thresholds and Sample Positions dialog, you can manually adjust state mode sampling positions without running *eye finder* (which automatically adjusts state sampling positions).

1 Select the state (synchronous sampling) mode (see To select the state acquisition mode (see page 100)).

2 In the Sampling Setup dialog, click **Thresholds and Sample Positions...**.

3 In the Thresholds and Sample Positions dialog (see page 497), drag the blue sampling position bars to the proper locations.

You can expand or collapse the channels in a bus.

TIP To adjust the sample position and/or threshold voltage for multiple buses and signals at the same time, you can group those buses and signals into a folder in the Buses/Signals Setup dialog; then, in the Thresholds and Sample Positions dialog, you can adjust the composite for the folder.

Sampling positions are saved with the logic analyzer configuration (see To save a configuration file (see page 171)).

See Also

- Understanding State Mode Sampling Positions (see page 378)
- To automatically adjust state sampling positions and threshold voltages (see page 107)

In Either Timing Mode or State Mode

- To specify the trigger position (see page 111)
- To set acquisition memory depth (see page 112)

To specify the trigger position

The trigger position specifies the amount of trace memory used for samples captured after the trigger. For example, when 10% poststore is selected, 90% of trace memory is used for samples captured before the trigger. When 90% poststore is selected, 10 % of trace memory is used for samples captured before the trigger.

When **Force Prestore** is checked, the amount of pre-trigger and post-trigger memory is always what you expect because, after a run, the logic analyzer fills pre-trigger memory before it starts looking for a trigger. If the event you want to trigger on occurs while pre-trigger memory is being filled, the logic analyzer does not trigger.

When **Force Prestore** is unchecked, the trigger position may not end up being where you expect because the logic analyzer starts looking for a trigger immediately after a run (it does not wait for pre-trigger memory to be filled). For example, if you set the trigger position to 50%, but the logic analyzer finds the trigger right away, the amount of pre-trigger memory is less than you expect.

1 From the menu bar select **Setup>(Logic Analyzer Module)>Timing/State (Sampling)...**, or click the  icon from the setup toolbar (see page 422).

2 Select the trigger position, and check or uncheck **Force Prestore** as desired.

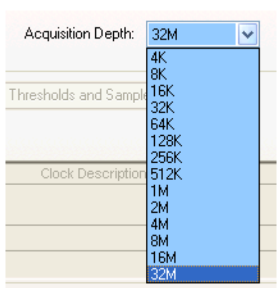
See Also

- Understanding Logic Analyzer Triggering, The Conveyor Belt Analogy (see page 385)
- To set the acquisition memory depth (see page 112)

To set acquisition memory depth

The acquisition depth control lets you set the amount of memory that is filled with data on an acquisition. The choices available depend on the maximum memory depth available in the analyzer that is being used.

1 From the menu bar select **Setup>(Logic Analyzer Module)>Timing/State (Sampling)...**.
2 Set the acquisition mode and any state or timing options. These will affect the available memory choices.
3 In the Options box to the right, set Acquisition Depth.



See Also

- Memory Depth and Channel Count Trade-offs (see page 374)
- Logic Analyzer Notes, Channels and Memory Depth (see page 573)
- Understanding Logic Analyzer Triggering, The Conveyor Belt Analogy (see page 385)
- To specify the trigger position (see page 111)

Using Timing Zoom

Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer.

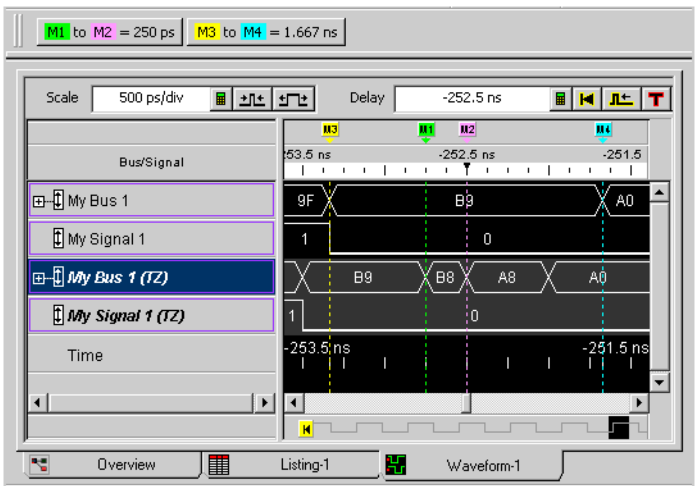
The timing zoom settings are accessed through the TimingZoom box in the Sampling tab.

- To turn timing zoom on or off (see page 114)
- To specify the timing zoom sample period (on some logic analyzers) (see page 114)
- To specify the timing zoom trigger position (see page 114)
- To align timing zoom in a split analyzer (see page 115)

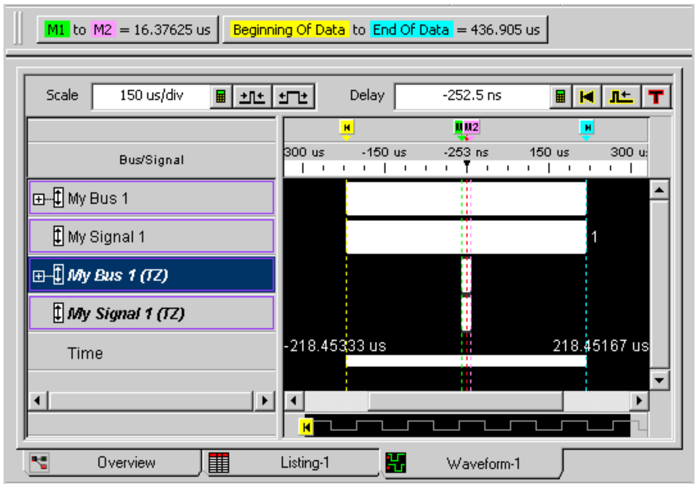
What is Timing Zoom?

Timing zoom collects a window of additional high-speed timing data around the trigger of the logic analyzer.

Because of timing zoom's faster sample rate, you get a higher-resolution view of transitions than with the normal timing mode. Timing zoom data appears in rows with "(TZ)" after bus/signal names.



Because of the faster sample rate and the relatively smaller amount of memory for samples, the overall window of time captured by timing zoom is smaller. Timing zoom data is captured around the trigger.



See Also

- Logic Analyzer Notes, Timing Zoom (see page 574)

To turn timing zoom on or off

If you are not interested in the timing zoom data for a measurement, you can improve logic analyzer performance by turning off timing zoom.

1 In the Sampling tab, check or uncheck **Enable** in the TimingZoom box.

To specify the timing zoom sample period (on some logic analyzers)

With some logic analyzers (see Logic Analyzer Notes, Timing Zoom (see page 574)), you can change the sampling period to see more or less sampling resolution around the trigger.

1 In the Sampling tab, check **Enable** in the TimingZoom box.

2 Click **Setup...** in the TimingZoom box.

3 In the TimingZoom Setup dialog (see page 502), select the **Sampling Period**.

See Also

- Logic Analyzer Notes, Timing Zoom (see page 574)

To specify the timing zoom trigger position

1 In the Sampling tab, check **Enable** in the TimingZoom box.

2 Click **Setup...** in the TimingZoom box.

3 In the TimingZoom Setup dialog (see page 502), drag the **Trigger Position** slider bar to the desired setting.

   The trigger position specifies the amount of timing zoom memory used for samples captured after the trigger. For example when "10% poststore" is selected, 90% of timing zoom memory is used for samples captured before the trigger.

See Also

- Logic Analyzer Notes, Timing Zoom (see page 574)

To align timing zoom in a split analyzer

On some older logic analyzer modules, if you have split the analyzer, you need to specify which analyzer's trigger timing zoom should be aligned with.

1 In the Sampling tab, check **Enable** in the TimingZoom box.

2 Click **Setup...** in the TimingZoom box.

3 In the TimingZoom Setup dialog (see page 502), select the logic analyzer to **Align Trigger With**.

Setting Up Symbols

You can use symbol names in place of bus/signal data values when:

- Setting up triggers.
- Displaying captured data.
- Searching for bus/signal values in the display windows.
- Setting up the Filter/Colorize tool.

Symbol names can be: variable names, procedure names, function names, source file line numbers, etc.

You can enter user-defined symbol names, or you can load symbol name definitions from a program's object file or from a general-purpose ASCII format symbol file.

- To create user-defined symbols (see page 116)
- To load symbols from a file (see page 118)
- To run the symbol reader outside the application (see page 119)
- To create an ASCII symbol file (see page 120)
- To change symbol reader options (see page 120)

Multiple user-defined symbols can have the same name and different values. Symbol value lookups are based on the name and the value.

Multiple symbols with the same name are not allowed when loading symbols from a file. When a symbol file has multiple symbols with the same name, the first is accepted and the rest are ignored.

When two or more symbols have the same value, the first symbol name matching the value is used (even though you may have selected one of the others).

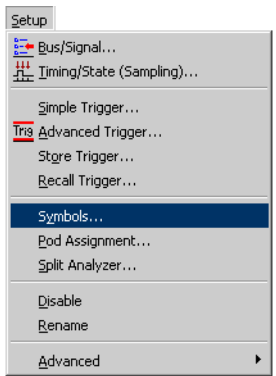
See Also
- To enter symbolic bus/signal values (see page 123)

To create user-defined symbols

You can create and edit user-defined symbols for bus/signal values.

To add a user-defined symbol

1 Select **Setup>(Logic Analyzer Module)>Symbols...**.

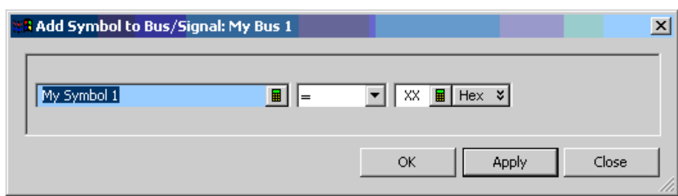


2 In the Symbols dialog (see page 492), select the bus or signal for which the new symbol should be displayed.

Each symbol is defined for a particular bus/signal.

3 Click **Add...**.

4 In the Add Symbol dialog, define a value or range of values.



There are no restrictions on the characters you can use in the name of a symbol.

Many identical symbols for a bus/signal can be entered, all with unique or identical values. During symbol lookup by a window or tool, the first symbol that matches the pattern is used. This is why the Symbol dialog has **Move Up** and **Move Down** buttons for reordering symbols.

5 Click **Apply**.

To see the symbols in the listing or waveform display, click OK in the Symbols dialog and change the base (see page 230) for the bus/signal to Symbols.

NOTE Because XML format logic analyzer configuration files save and load user-defined symbols, you can also add symbols by (1) using text processing tools to re-format symbol information from software development tools, (2) inserting them into an XML format configuration file, and (3) loading the configuration file into the *Agilent Logic Analyzer* application (see "XML Format" (in the online help)).

To edit a user-defined symbol

1 Select **Setup>(Logic Analyzer Module)>Symbols...**.
2 Select the symbol you want to edit.
3 Click **Edit**.

To delete a user-defined symbol

1 Select **Setup>(Logic Analyzer Module)>Symbols...**.
2 Select the symbol you want to delete.
3 Click **Delete**.

To save symbols

Save symbols as part of a configuration file (see page 171). Symbols are saved in the configuration whether or not you select **Setup only** in the Save As dialog.

You can move user-defined symbols from one bus/signal to another by saving to an XML format configuration file, editing, then reloading the file.

See Also

- Displaying Names (Symbols) for Bus/Signal Values (see page 232)

To load symbols from a file

You can load symbols from object files, which are created by your compiler/linker or other software development tools, or you can load symbols from a general-purpose ASCII (GPA) format symbol files.

1 Create the symbol file:
   - Generate an object file with symbolic information using your software development tools (see Object File Formats Supported by the Symbol Reader (see page 544)).
   - Generate an Agilent Symbol Reader ".sym" file by running the symbol reader outside of the *Agilent Logic Analyzer* application (see page 119); loading symbols from ".sym" files is faster than loading them from object files.
   - If your language tools cannot generate object file formats that are supported by the logic analyzer, create an ASCII symbol file (see page 120).
2 From the *Agilent Logic Analyzer* application's main menu bar, choose **Setup>(Logic Analyzer Module)>Symbols...**.
3 In the Symbols dialog (see page 492), select the bus/signal name you want to load object file symbols for.

   In most cases, you will select the bus/signal representing the address bus of the processor you are analyzing.
4 Click **Load...**.
5 In the Select Symbol File dialog, select the file from which you want to load symbols.
6 Click **Open**.

The name of the symbol file is saved when a configuration file is saved. The symbol file will be reloaded when the configuration is loaded.

To reload symbols from a file

1 Choose **Setup>(Logic Analyzer Module)>Symbols...**.

2 In the Symbols dialog (see page 492), select the symbol file whose symbols you want to reload.

3 Click **Load...**.

The values of the symbols being used in the trigger sequence are updated automatically each time a symbol file is reloaded.

To delete a symbol file

1 Choose **Setup>(Logic Analyzer Module)>Symbols...**.

2 In the Symbols dialog (see page 492), select the symbol file whose symbols you want to delete.

3 Click **Delete**.

See Also

- Object File Formats Supported by the Symbol Reader (see page 544)

To run the symbol reader outside the application

You can run the symbol reader outside the *Agilent Logic Analyzer* application to create an Agilent Symbol Reader ".sym" file that loads faster than the object file.

1 Open a Command Prompt window.

2 Run the command:

```
agSymbolBuild.exe [-r <readers.ini>] <object_file> <dest_file>.sym
```

For example:

```
agSymbolBuild.exe q.elf q.sym
```

The **agSymbolBuild.exe** symbol reader program is located in the directory:

```
<Drive letter>:\<Install directory>\SymbolReaders\
```

For example:

```
C:\Program Files\Agilent Technologies\Logic Analyzer\SymbolReaders\
```

To change the symbol reader options, copy the readers.ini file from the SymbolReaders directory, edit it, and use the `-r <readers.ini>` option when running the **agSymbolBuild.exe** program.

For more information on the symbol reader program, see the README.txt file in the SymbolReaders directory.

See Also

- To load symbols from a file (see page 118)
- To change symbol reader options (see page 120)

To create an ASCII symbol file

General-purpose ASCII (GPA) symbol files are created by converting object file symbols to a GPA format symbol files and/or by using text editing/processing tools.

To convert object file symbols to GPA format symbol files

When you need to apply different offsets to different symbols or sections of code, you can convert object file symbols to general-purpose ASCII (GPA) format symbol files. Then, you can use text editing/processing tools to adjust the symbol or section offset values in the GPA format file before loading the file into the *Agilent Logic Analyzer* application.

1 Open a Command Prompt window.
2 Run the command:

```
agSymbolQuery.exe -a <object_file> <dest_file>.sym > GPA_file
```

For example:

```
agSymbolQuery.exe -a q.elf q.sym > q.gpa
```

The **agSymbolQuery.exe** program is located in the directory:

```
<Drive letter>:\<Install directory>\SymbolReaders\
```

For example:

```
C:\Program Files\Agilent Technologies\Logic Analyzer\SymbolReaders\
```

For more information on the **agSymbolQuery.exe** program, see the README.txt file in the SymbolReaders directory.

See Also

- General-Purpose ASCII (GPA) Symbol File Format (see page 545)

To change symbol reader options

You can change how ELF/Stabs, Ticoff, or Coff/Stabs symbol files are processed by editing the readers.ini file.

1 Make a backup copy of the readers.ini file.

The readers.ini file is located in the directory:

```
<Drive letter>:\<Install directory>\SymbolReaders\
```

For example:

```
C:\Program Files\Agilent Technologies\Logic Analyzer\SymbolReaders\
```

2 Edit the readers.ini file.

For more information on the symbol reader options, see the comments in the readers.ini file.

Reader Options

SectionReloc

Use the following options to specify the relocation. Replace <sectionname> with the name of your section. Replace <hex_relocation_value> with the hex relocation amount (32-bit max). You can set the relocation for section to an absolute value or you can add a relative relocation amount. The relocation value will be calculated using unsigned 32-bit math.

```
[SectionReloc]
  Place this before all relocation options.

AddReloc_AllSections=<hex_relocation_value>
  Relocates all sections by an amount specified.
  If this command is used with subsequent relocation commands
  the subsequent commands will override this operation.

AddReloc_<sectionname>=<hex_relocation_value>
  Adds a relative relocation value.

SetReloc_<sectionname>=<hex_relocation_value>
  Relocates the section to the absolute address specified.

NonReloc_<sectionname>=TRUE
  Inhibits a section from being relocated.
  It is only useful when it follows a AddRloc+AllSections.
```

C++Demangle

```
1= Turn on C++ Demangling (Default)
0= Turn off C++ Demangling
```

C++DemOptions

```
803= Standard Demangling
203= GNU Demangling      (Default Elf/Stabs)
403= Lucid Demangling
800= Standard Demangling without function parameters
200= GNU Demangling without function parameters
400= Lucid Demangling without function parameters
```

MaxSymbolWidth

```
80= Column width max of a function or variable symbol
    Wider symbols names will be truncated.
    (Default 80 columns)
```

OutSectionSymbolValid

```
0= Symbols whose addresses aren't within the
    defined sections are invalid (Default)
1= Symbols whose addresses aren't within the
    defined sections are valid
```

This option must be specified in the Nsr section of the Readers.ini file:

```
[Nsr]
OutSectionSymbolValid=1
```

ReadElfSection

```
2= Process all globals from ELF section (Default)
   Get size information of local variables
1= Get size information of global and local variables
   Symbols for functions will not be read, and
   only supplemental information for those symbols in
   the Dwarf or stabs section will be read.
0= Do not read the Elf Section
```

If a file only has an ELF section this will have no effect and the ELF section will be read completely. This can occur if the file was created without a "generate debugger information" flag (usually -g). Using the -g will create a Dwarf or Stabs debug section in addition to the ELF section.

StabsType

```
StabsType=0  Reader will determine stabs type (Default)
StabsType=1  Older style stabs
             (Older style stabs have individual symbol
             tables for each file that was linked into
             the target executable, the indexes of each
             symbol table restart at 0 for each file.)
StabsType=2  Newer style stabs
             (New style stabs have a single symbol table
             where all symbols are merged into a large
             symbol array).
```

ReadOnlyTicoffPage

ReadOnlyTicoffPage tells the ticoff reader to read only the symbols associated with the specified page (as an example 'ReadOnlyTicoffPage=0' reads only page 0 symbols). A value of -1 tells the ticoff readers to read symbols associated with all pages.

```
ReadOnlyTicoffPage=-1 Read all symbols associated will all
                      ticoff pages (Default)
ReadOnlyTicoffPage=p  Read only symbols associated with
                      page 'p' (where p is any integer
                      between 0 and n the last page of
                      the object file).
```

AppendTicoffPage

AppendTicoffPage tells the ticoff reader to append the page number to the symbol value. This assumes that the symbol value is 16-bits wide and that that page number is a low positive number which can be ORed into the upper 16 bits of an address to create a new 32-bit symbol address. For example, if the page is 10 decimal and the symbol address is 0xF100 then the new symbol address will be 0xAF100.

```
AppendTicoffPage=1  Append the ticoff page to the symbol
                    address
AppendTicoffPage=0  Do not append the ticoff page to the
                    symbol address (Default)
```

Examples

Example for Elf/Stabs

```
[ReadersElf]
C++Demangle=0
C++DemOptions=203
MaxSymbolWidth=60
StabsType=2
```

Example for Coff/Stabs (using Ticoff reader)

```
[ReadersTicoff]
C++Demangle=0
C++DemOptions=203
MaxSymbolWidth=60
StabsType=2
```

Example for Ticoff

```
[ReadersTicoff]
C++Demangle=0
```

```
C++DemOptions=203
MaxSymbolWidth=60
ReadOnlyTicoffPage=4
AppendTicoffPage=1
```

To enter symbolic bus/signal values

When entering bus/signal values while setting up triggers, searching display windows, or setting up the Filter/Colorize tool:

1. Select the desired operator for the bus/signal value.
2. Select the **Symbol** number base.
3. Click the value button.
4. In the Select Symbol dialog (see page 477), select the symbol you want to use.

   All of the symbols for the current bus/signal, regardless of type, are available in the dialog.
5. Click **OK**.

See Also

- Select Symbol Dialog (see page 477)

Installing Licensed Hardware Upgrades

Some of the newer logic analysis system cards (like the 16910/11A and 16950 logic analyzers) have hardware features (like state speed and memory depth) that can be upgraded by purchasing a license.

NOTE When installing licensed hardware upgrades, you must run the *Hardware Update Utility* program on the frame that contains the cards you want to upgrade. In other words:

- In a multiframe logic analysis system, you must run the *Hardware Update Utility* program on each frame that has cards to be upgraded.
- You cannot install module upgrades over a remote connection (including remote connections via Remote Desktop, NetOp, or RealVNC).

To install a licensed hardware upgrade:

1 After you have ordered the hardware upgrade product/option and have received your license file, copy the license file to the directory:

```
C:\Program Files\Agilent Technologies\Logic Analyzer\License\
```

If you have installed the *Agilent Logic Analyzer* application in a different directory, copy the license file to the directory:

```
<Drive letter>:\<Install directory>\License\
```

If upgrade options were ordered for several cards at the same time, there will be one license file for all submitted serial numbers.

License file names must have the ".lic" extension in order to work.

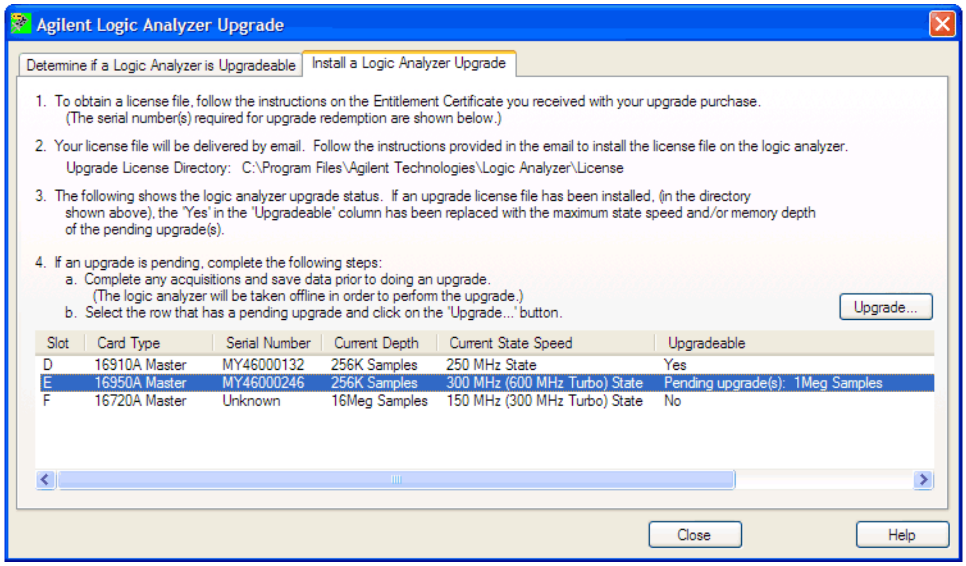
2 In the *Agilent Logic Analyzer* application, choose **Help>Logic Analyzer Upgrade...**.

Or, from the Windows Start bar, click **Start>All Programs>Agilent Logic Analyzer>Utilities>Hardware Update Utility**.

NOTE The Agilent Logic Analyzer Upgrade dialog will read "No Hardware Found" for 1680/1690-series logic analyzers because they do not contain upgradeable modules. This is not an indication of a problem with your hardware.

---

3 In the Agilent Logic Analyzer Upgrade dialog's "Install a Logic Analyzer Upgrade" tab, select the card that has an upgrade pending.



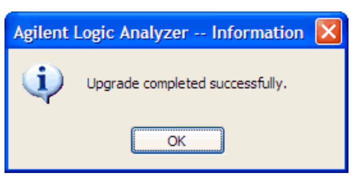
CAUTION

The *Agilent Logic Analyzer* application will be taken offline in order to perform the upgrade. Therefore, complete any acquisitions and save data before performing the upgrade.

---

4 Click **Upgrade...**.

5 When the upgrade completed information dialog appears, click **OK**.



The Agilent Logic Analyzer Upgrade dialog shows the upgraded hardware.

6 Click **Close** to close the Agilent Logic Analyzer Upgrade dialog.

Once you complete the hardware upgrade, the hardware will retain its new settings and can be moved to any 16900-series logic analysis system frame.

6
Capturing Data from the Device Under Test

After you have probed the device under test (see page 59) and set up the logic analyzer (see page 75) (by defining buses and signals (see page 82) and choosing the sampling mode (see page 97)), you are ready to tell the logic analyzer when to capture/acquire data (in other words, set up a trigger) and run the measurement.

You can set up:

- *Quick Triggers* by drawing a box in a display window around the data to trigger on,
- *Simple Triggers* in a display window by specifying bus/signal values to trigger on, or
- *Advanced Triggers* by opening a dialog box and choosing from collections of predefined *trigger functions (see page 504)*.

Advanced triggers let you trigger the logic analyzer after a sequence of events occur in the device under test.

Once you have set up a trigger, you can run the measurement. When the measurement completes, you can view the captured data (see page 183) and save it (along with the logic analyzer setup).

See Also

- Probing the Device Under Test (see page 59)
- Setting Up the Logic Analyzer (see page 75)
- Defining Buses and Signals (see page 82)
- Choosing the Sampling Mode (see page 97)
- Analyzing the Captured Data (see page 183)

Setting Up Quick (Draw Box) Triggers

Within the Waveform, Listing, and Source windows, you can quickly set up a simple trigger by drawing a rectangle with the mouse or right-clicking on a source line.

After the simple trigger has been defined, and the analyzer is run, the trigger saved in the most recently used triggers list and can be recalled (see page 167) at any time.

- To set a Quick Trigger in the Waveform window (see page 129)
- To set a Quick Trigger in the Listing window (see page 130)
- To set a Quick Trigger in the Source window (see page 131)

To set a Quick Trigger in the Waveform window

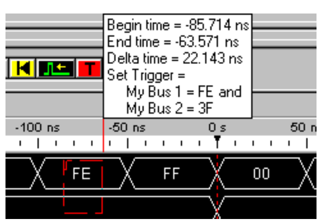
In the Waveform window, you can quickly set up a simple trigger by drawing a rectangle with the mouse.

1 Make sure the Waveform window's Fast Zoom In (see page 215) option is not selected.

2 Using the mouse, point to the upper-left corner of your desired trigger rectangle.

3 While holding down the mouse button, drag the mouse pointer to the lower-right corner of your desired rectangle, then release the mouse button.

   As you draw the rectangle, you can monitor the trigger as it is set with the tool tip readout that appears.



   As you move the mouse left-to-right and top-to-bottom, the signal edge/level or bus value in contact with the **left of the rectangle** becomes the trigger.

   Only one edge can be set.

If a bus is expanded into its separate signals, three conditions apply:

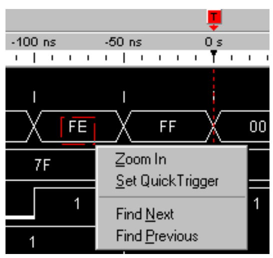
a If drawing starts on a bus, none of its expanded signals can be included.

b If drawing starts on a signal, the bus cannot be included.

c Edges and levels are mutually exclusive. That is, either one edge can be set, or all levels can be set, but not both at the same time.

NOTE In the Waveform display window, it may be necessary to redraw the rectangle if you do not get your desired trigger points dictated by the left-side line of the rectangle. You could also try drawing the rectangle backwards leaving the left-side rectangle line set last.

4 Select **Set Quick Trigger**.



General Guidelines

- Any bus/signals with overlapping bits are not included within the trigger specification.

  Example: Bus_1 has channels 0 through 7 of pod 1 assigned and Bus_2 has channels 3 through 6 of pod 1 assigned. At this point, you have the same probed signals (channels 3 through 6 of pod 1) assigned in both Bus_1 and Bus_2. Now you draw the rectangle over both bus_1 and bus_2. Since Bus_1 channels 3 through 6 are repeated (overlapped) on Bus_2, they will not be included in the trigger specification.

- Only a single sequence step can be defined by a drawn rectangle.
- As you draw the rectangle, a tool tip is displayed showing the current trigger specification that would be set.

To set a Quick Trigger in the Listing window

In the Listing window, you can quickly set up a simple trigger by drawing a rectangle with the mouse.

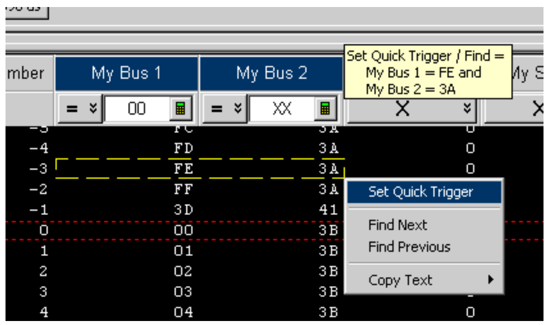
1 Using the mouse, point to the sample that you want to use as the quick trigger.

2 While holding down the mouse button, drag the mouse pointer horizontally to draw a rectangle around the buses/signals you want to include in the trigger; then, release the mouse button.

As you draw the rectangle, a tool tip shows the trigger that will be set.

Dragging the mouse pointer vertically does not affect the sample used for the quick trigger; the sample used is always the one from which the drawn rectangle originates.

3 Select **Set Quick Trigger**.



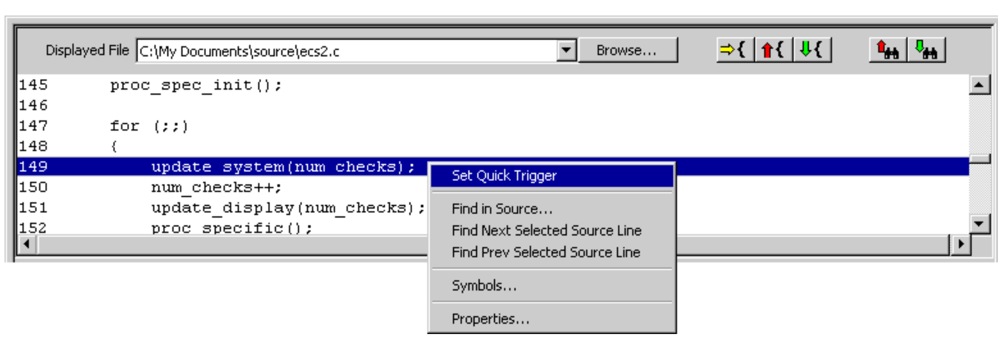
General Guidelines

- Any bus/signals with overlapping bits are not included within the trigger specification.

  Example: Bus_1 has channels 0 through 7 of pod 1 assigned and Bus_2 has channels 3 through 6 of pod 1 assigned. At this point, you have the same probed signals (channels 3 through 6 of pod 1) assigned in both Bus_1 and Bus_2. Now you draw the rectangle over both bus_1 and bus_2. Since Bus_1 channels 3 through 6 are repeated (overlapped) on Bus_2, they will not be included in the trigger specification.
- Only a single sequence step can be defined by a drawn rectangle.
- As you draw the rectangle, a tool tip is displayed showing the current trigger specification that would be set.

To set a Quick Trigger in the Source window

1 In the Source window's source pane, right-click the source line you want to set a Quick Trigger on, and choose **Set Quick Trigger**.

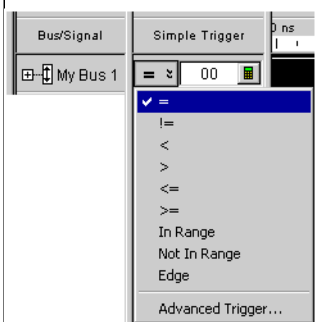
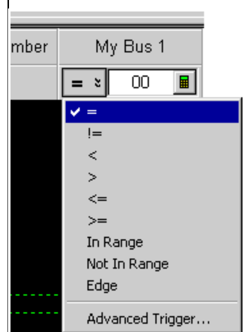
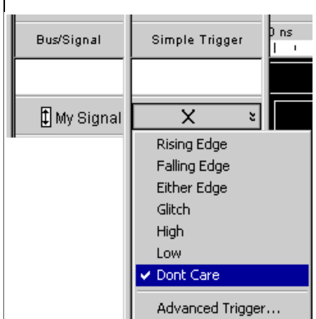
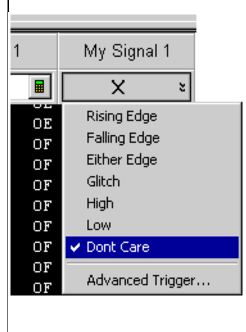


See Also

- To change the "Set Quick Trigger" alignment (see page 279)
- Starting/Stopping Measurements (see page 168)
- Viewing Source Code Associated with Captured Data (see page 272)

Specifying Simple Triggers

Simple triggers let you quickly set up triggers on edges and bus/signal patterns from within display windows.

<table>
<tr><th></th><th>Waveform Display Window</th><th>Listing/Compare/Source Display Window</th></tr>
<tr><td>Bus Trigger</td><td>
</td><td>
</td></tr>
<tr><td>Signal Trigger</td><td>
</td><td>
</td></tr>
</table>

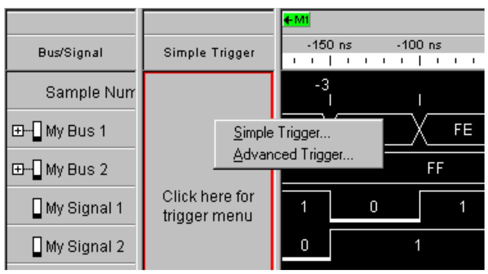
Buses are compared to entered pattern values using a relational operator (**=**, **!=**, **<**, **>**, **<=**, **>=**, **In Range**, **Not In Range**) or to one of multiple edges or glitches (**Edge**, available in timing mode).

Signals are compared to edges (**Rising Edge**, **Falling Edge**, **Either Edge**, **Glitch**, available in timing mode) or a logic level pattern (**High**, **Low**).

You can specify multiple bus/signal pattern values and one edge, all of which must evaluate to true for a sample to trigger the logic analyzer. (If you try to specify multiple edges, the last edge specified has priority, and the previously specified edge is changed to don't care.)

When buses/signals overlap (that is, the same logic analyzer channels are assigned to multiple buses/signals), the last change has highest priority. For example, if you specify a pattern on Bus A and then specify a rising edge on Signal B, which is bit 0 on Bus A, the previously specified pattern is erased.

When the desired trigger condition requires more than a simple AND expression (for example, one pattern OR another pattern on a bus, patterns in a sequence of samples, testing timer or counter values, etc.), you can choose **Advanced Trigger...** to specify an advanced trigger (see page 138). When an advanced trigger surpasses the functional limits of a simple trigger, the simple trigger fields go away; to restore them, you must either change the advanced trigger so that it doesn't surpass the limits of a simple trigger, or click **Click here for trigger menu** and choose **Simple Trigger...** to reset the trigger.



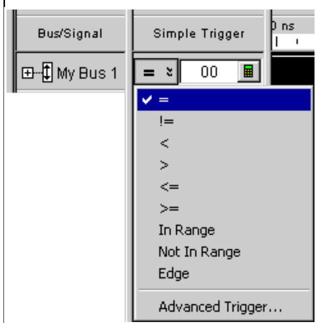
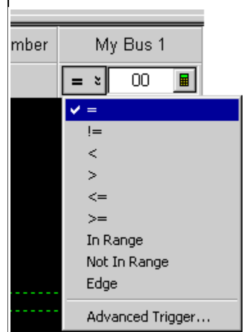
- To specify bus patterns or edges in a simple trigger (see page 134)
- To specify signal edges or levels in a simple trigger (see page 136)

See Also

- Setting Up Quick Triggers (see page 129)
- Specifying Advanced Triggers (see page 138)
- To store a trigger (see page 166)
- To recall a trigger (see page 476)

To specify bus patterns or edges in a simple trigger

When specifying simple triggers (see page 133), you can specify bus patterns or edges to trigger on.

	Waveform Display Window	Listing/Compare/Source Display Window
Bus Trigger		

To specify a bus pattern

1 In the Simple Trigger field for a bus, click the = operator button; then, choose from one of the following operators:

- = (Equal To)
- != (Not Equal To)
- < (Less Than)
- > (Greater Than)
- <= (Less Than Or Equal To)
- >= (Greater Than Or Equal To)
- **In Range**
- **Not In Range**

NOTE

The <, >, <=, >=, **In Range**, and **Not In Range** operators are not available when a bus with reordered bits has been selected. Also, these operators cannot be used when the selected bus contains clock bits that span pod pairs. The **In Range** and **Not In Range** operators are limited to buses that span 2 or fewer pod pairs (up to 64 bits wide).

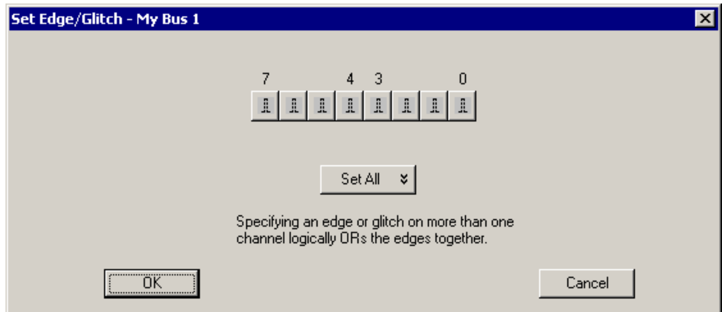
2 In the text entry field XX, enter the bus pattern value to compare.

To specify one of multiple edges or glitches on a bus

1 In the Simple Trigger field for a bus, click the = operator button; then, choose **Edge**.

2 Click **Edge Spec...**.

3 In the Set Edge/Glitch dialog, specify edges or glitches you are looking for; use the **Set All** button to make a selection for all signals in the bus.



4 Click **OK** to close the Set Edge/Glitch dialog.

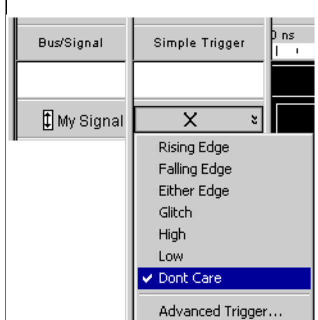
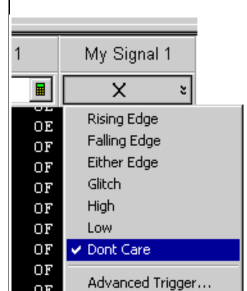
NOTE Glitches are not drawn on the screen. You need an oscilloscope to further troubleshoot glitches and find out when they occur.

See Also

- To specify signal edges or levels in a simple trigger (see page 136)
- To trigger on one of multiple edges or glitches (see page 52)

To specify signal edges or levels in a simple trigger

When specifying simple triggers (see page 133), you can specify signal edges or levels to trigger on.

	Waveform Display Window	Listing/Compare/Source Display Window
Signal Trigger		

To specify a signal edge/glitch

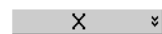
NOTE In state acquisition mode, edge options are not available.

1 In the Simple Trigger field for a signal, click the  edge/level button; then, choose from:

- **Rising Edge**
- **Falling Edge**
- **Either Edge**
- **Glitch** — the logic analyzer can trigger when a glitch of *minimum detectable width* appears on the signal. Refer to the characteristics (see page 595) of your logic analyzer to find the minimum detectable glitch width.

NOTE Glitches are not drawn on the screen. You need an oscilloscope to further troubleshoot glitches and find out when they occur.

To specify a signal level

1 In the Simple Trigger field for a signal, click the  edge/level button; then, choose from:

- **High**
- **Low**

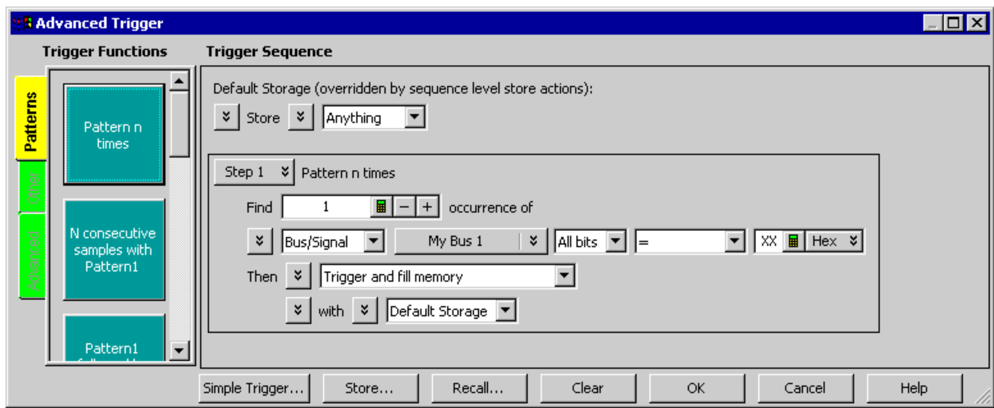
See Also

- To specify bus patterns or edges in a simple trigger (see page 134)

Specifying Advanced Triggers

When you need to set up triggers that are more complex than just finding particular bus/signal values (for example, when you need to trigger on a sequence of events in the device under test), you set up advanced triggers.

To open the Advanced Trigger dialog, click  in the analyzer setup toolbar, or choose **Setup>(Logic Analyzer Module)>Advanced Trigger...** from the menu bar.



Advanced triggers are specified by dragging-and-dropping predefined *trigger functions (see page 504)* into trigger sequence steps. If the trigger function you need doesn't exist, start with a trigger function that is close, convert the trigger sequence step to advanced If/Then trigger functions, and edit the If/Then trigger functions.

Each step in the trigger sequence looks for *events (see page 139)* in data samples captured from the device under test (or in logic analyzer timers, counters, or flags), and when those events are found, takes some *action (see page 139)* (like triggering or going to another step in the sequence). You can also insert actions for timers, counters, or flags.

Default storage lets you ignore the question, in individual trigger sequence steps, of which captured samples should be stored in logic analyzer memory. However, you can insert *storage control* actions in individual trigger sequence steps to specify whether samples should be stored or to specify whether default storage should be turned on or off. Sequence step storage control actions override the default storage specification.

- To replace or insert trigger functions into trigger sequence steps (see page 143)
- To specify bus/signal patterns or edges (see page 144)
- To specify packet events (in "Find a packet" trigger function) (see page 145)

- To specify a trigger sequence step's goto or trigger action (see page 148)
- To specify default storage (see page 149)
- To insert or delete events (see page 150)
  - To insert a timer event (see page 152) (see also Using Timers (see page 140))
  - To insert a counter event (see page 152) (see also Using Counters (see page 141))
  - To insert a flag event (see page 153) (see also Using Flags (see page 142))
  - To insert an "Arm in from" event (see page 153)
- To negate events (see page 154)
- To change the evaluation order of AND/OR'ed events (see page 155)
- To insert or delete actions (in a trigger sequence step) (see page 155)
  - To insert a timer action (see page 156) (see also Using Timers (see page 140))
  - To insert a counter action (see page 156) (see also Using Counters (see page 141))
  - To insert a reset occurrence counter action (see page 157)
  - To insert a flag action (see page 157) (see also Using Flags (see page 142))
  - To insert a storage control action (see page 158)
- To show a trigger sequence step as Advanced If/Then trigger functions (see page 158)
- To convert a trigger sequence step to Advanced If/Then trigger functions (see page 159)
- To choose between a duration or occurrence count for events (timing mode) (see page 160)
- To delete trigger sequence steps (see page 161)
- To clear the trigger sequence (see page 161)

See Also

- Understanding Logic Analyzer Triggering (see page 385)
- State Mode Trigger Functions (see page 517)
- Timing Mode Trigger Functions (see page 504)
- Specifying Simple Triggers (see page 133)

Reading Event and Action Statements

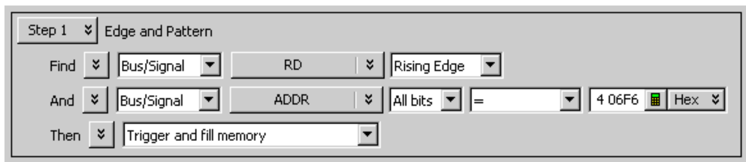
Event and action statements in trigger sequence steps read from left-to-right like:

Find an event in the device under test; when the event is found, take some action.

Or:

If an event is found in the device under test; then, take an action.

For example, suppose you want to see what happens after a read from the address 406F6H. To do this, set up the trigger to look for a rising edge on the RD (memory read) signal and an address bus pattern of 406F6H (hexadecimal):



As you set up the trigger, think of it as constructing a sentence that reads left-to-right. For example:

Find a **Signal** named **RD** with a **Rising Edge** And a **Bus** named **ADDR** with **All bits= (equal)** to the pattern **406F6 Hex**. When found, then **Trigger and fill memory**.

See Also

- Specifying Advanced Triggers (see page 138)
- Understanding Logic Analyzer Triggering, Sequence Steps (see page 387)

Using Timers

Timers are like stopwatches. Use timers to create either a user-defined delay or a time standard which valid data duration is evaluated against. The timer can **Start** from reset, **Stop** and reset, **Pause**, or **Resume**.

Timer considerations:

- It takes a certain amount of time for timers to reset; this is called the *timer reset latency*. To find the timer reset latency for your logic analyzer, see the description of its characteristics (see page 595).
- The number of timers available in a module depends on the selected acquisition mode and sampling option:

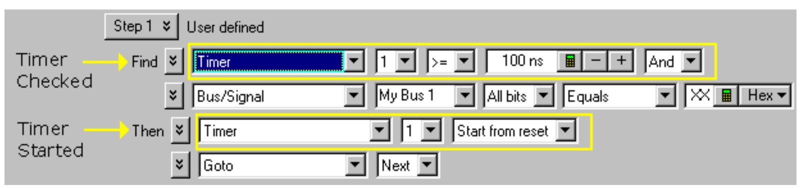
Acquisition Mode	Sampling Option	# Timers Available

State mode (synchronous sampling)	*General State Mode*	# pod pairs not reserved for time tag storage
	Turbo State Mode	0
Timing mode (asynchronous sampling)	all	# pod pairs not reserved for time tag storage

Refer to your logic analyzer characteristics (see page 595) for the actual number of timers available. For information on when pod pairs are reserved for time tag storage, see Why Are Pods Missing? (see page 373).

- Timers are checked in event statements, and started in action statements.
- Timers must be started before they can be checked. This is done by either including the timer start action with the timer check event within the same trigger step or starting the timer in a preceding trigger step.

  The following example shows the timer start action and check event within the same trigger step.



- Once a timer event is configured, you can reuse the timer by selecting its identification number. The same timer must always be checked against the same value. To check for different durations, use different timers.

See Also

- To insert a timer action (see page 156)
- To insert a timer event (see page 152)
- Understanding Logic Analyzer Triggering, Timers (see page 392)

Using Counters

Counters are available in both Event and Action statements, and like other events, they evaluate to either true or false. Use counters to create a user-defined delay, or to create a standard against which valid data duration is evaluated. Once configured, a counter persists throughout all the steps of the trigger sequence.

Counter considerations:

- Maximum counters available is 2.
- When using counters in the transitional timing mode, one counter is used internally so only one counter is available in a sequence step.
- Once a counter is configured, you can reuse the counter by selecting its identification number. Each use of the counter must check it for the same value.

NOTE The logic analyzer also has occurrence counters, and a **reset occurrence counter** action. Occurrence counters only exist within steps that contain the "occurs" phrase and are not affected by the other counter actions described on this page.

See Also

- To insert a counter action (see page 156)
- To insert a counter event (see page 152)
- Understanding Logic Analyzer Triggering, Counters (see page 391)

Using Flags

Flags can be used to signal between modules in the logic analysis system (including a multiframe logic analysis system).

NOTE Flags are not available in 1680/1690-series logic analyzers.

There are 4 flags that are shared across all connected logic analysis system frames. A flag may be driven or received by multiple modules.

Using flags, logic analyzer modules can communicate back and forth with each other multiple times during a data acquisition, both before and after their trigger events occur. (By comparison, a module can arm another module one time when its trigger occurs.)

By default, flags are cleared. You can insert *actions* to set, clear, pulse set, or pulse clear a flag. You can insert flag *events* in different logic analyzer modules to test whether a flag is set or clear.

NOTE Flag actions are not available in *Turbo State Mode*; however, you can still check flags with flag events.

A flag that is set by a module remains set until that module clears it. If multiple modules set the same flag, all of those modules must clear the flag before it becomes clear.

Flags can also be used to drive the logic analysis system's Port Out signal.

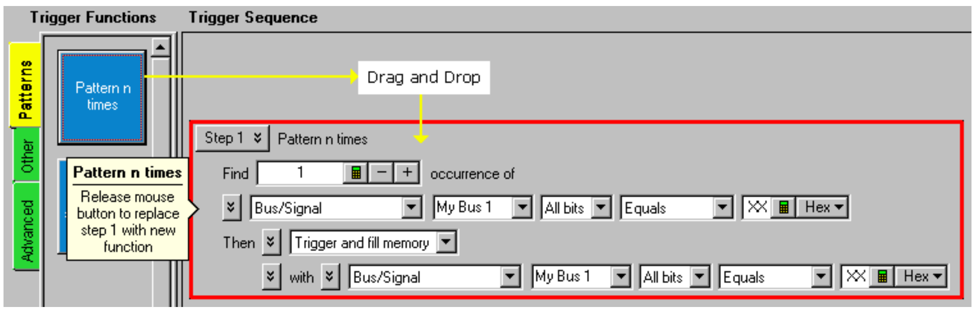
See Also

- To insert a flag action (see page 157)
- To insert a flag event (see page 153)
- Understanding Logic Analyzer Triggering, Flags (see page 391)

To replace or insert trigger functions into trigger sequence steps

Multiple steps in the trigger sequence are necessary when you want to trigger on a sequence of events in the device under test. When you want to trigger on one event in (that is, a single sample from) the device under test, a single step in the trigger sequence is all you need.

1 In the Advanced Trigger dialog, **drag-and-drop** the desired Trigger Function (see page 504) into the Trigger Sequence display area.



To replace an existing step:

- Drag-and-drop the trigger function on top of an existing step in the trigger sequence. A red box around the old function indicates the replace operation.

To insert a trigger function as a new step:

- Drag-and-drop the trigger function above or below an existing step in the trigger sequence. When the mouse is positioned above or below an existing step, a red insert bar appears to indicate the relative insert location of the trigger function.

See Also

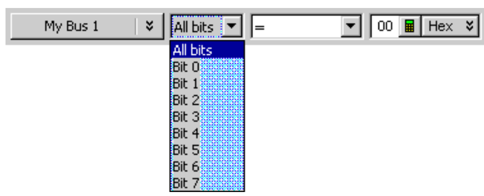
- Understanding Logic Analyzer Triggering, Sequence Steps (see page 387)
- To delete trigger sequence steps (see page 161)
- State Mode Trigger Functions (see page 517)
- Timing Mode Trigger Functions (see page 504)

To specify bus/signal patterns or edges

1 In the Advanced Trigger dialog, select the bus or signal.

Clicking  lets you select from recently used bus/signal names. Clicking elsewhere on a bus/signal name button opens a Select dialog for selecting a different name.

2 If a bus has been selected, either select **All bits** on the bus or select an individual bit.

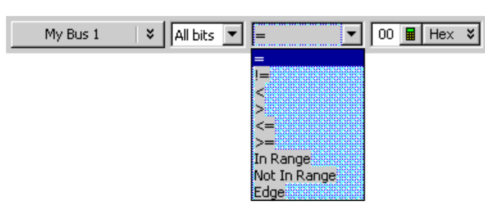


3 Specify the bus/signal value:

If a signal or one bit of a bus has been selected, select the signal pattern value (**High**, **Low**, or **Dont Care**) or edge value (**Rising Edge**, **Falling Edge**, **Either Edge**, or **Glitch**). You can only select edge values in the timing mode (asynchronous sampling).

If all bits of a bus have been selected:

a Select one of the operators: **=** (equal to), **!=** (not equal to), **<** (less than), **>** (greater than), **<=** (less than or equal to), **>=** (greater than or equal to), **In Range**, **Not In Range**, or **Edge**.



NOTE

The <, >, <=, >=, **In Range**, and **Not In Range** operators are not available when a bus with reordered bits has been selected. Also, these operators cannot be used when the selected bus contains clock bits that span pod pairs. The **In Range** and **Not In Range** operators are limited to buses that span 2 or fewer pod pairs (up to 64 bits wide).

When the **Edge** operator is selected (only available in timing mode), the **Edge Spec...** button opens the Set Edge/Glitch dialog for specifying multiple edges or glitches on a bus (see To trigger on one of multiple edges or glitches (see page 52)).

b Select the number base (**Binary**, **Hex**, **Octal**, **Decimal**, **Signed Decimal**, **Ascii**, or **Symbol**).

c Enter the pattern value(s).

When the **Symbol** number base is selected, you use the Select Symbol dialog (see page 477) to specify the pattern values.

See Also

- To specify default storage (see page 149)
- To insert or delete events (see page 150)
- Understanding Logic Analyzer Triggering, Edges (see page 390)
- Understanding Logic Analyzer Triggering, Ranges (see page 391)

To specify packet events (in "Find a packet" trigger function)

1 In the Advanced Trigger dialog, replace or insert the Find a packet (see page 524) trigger function into the trigger sequence (see To replace or insert trigger functions into trigger sequence steps (see page 143)).

2 In the "Find a packet" trigger sequence step, click **Select a bus**.

3 In the Choose a Protocol Family and Bus dialog (see page 451), select the protocol family and the type of bus being probed; then, click **OK**.

4 In the "Find a packet" trigger sequence step, click **Select a packet**.

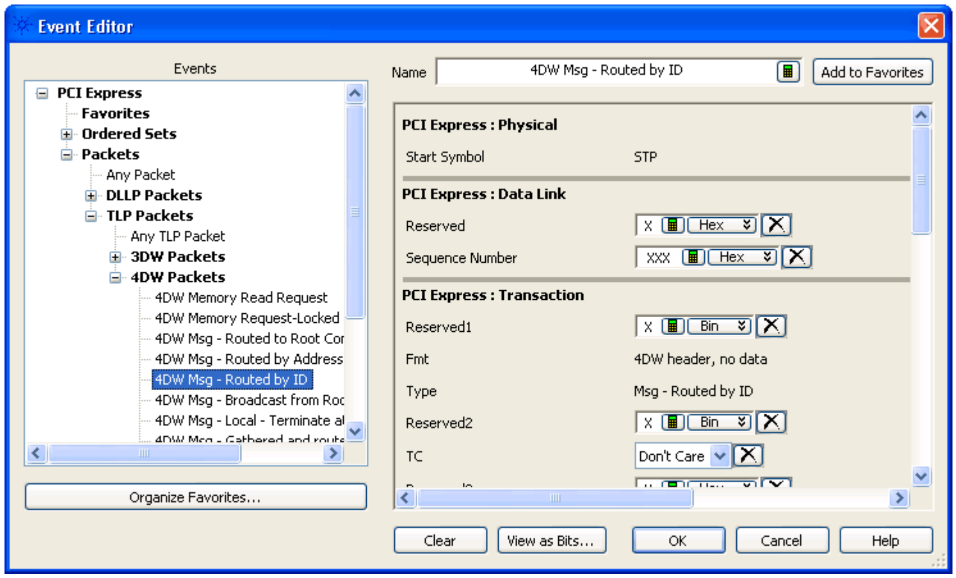
5 In the Event Editor Dialog (see page 454), select the type of packet event and enter packet field values to trigger on; then, click **OK**.

See Also

- Using the Packet Event Editor (see page 146)

Using the Packet Event Editor

The packet event editor lets you specify packet events in the "Find a packet" trigger function.



To use the packet event editor:

1 Select the event type from the left side of the dialog.

2 Enter or select field values on the right side of the dialog.

   To clear a field value, click ☒.

3 If desired, you can enter or modify the **Name** of the event.

4 When you are done editing the packet event, click **OK**.

The packet event editor also allows you:

- To view a packet event as bits (see page 146)
- To save favorite packet events (see page 147)
- To organize favorite packet events (see page 148)

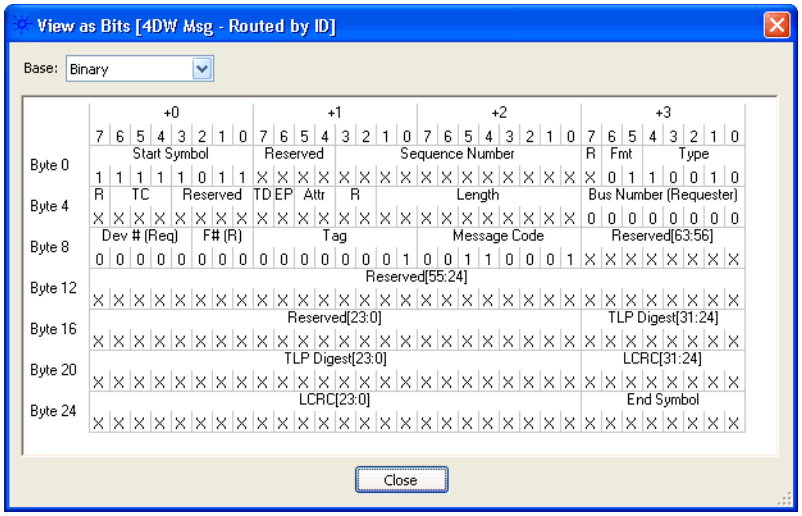
See Also

- Find a packet (see page 524) trigger function

To view a packet event as bits

1 While specifying packet events using the Event Editor Dialog (see page 454), click **View as Bits...**.

   The packet event is displayed in format similar to packet descriptions in specification documents.



2 If desired, you can select a different number **Base**.

3 When you are finished viewing the packet event as bits, click **Close**.

See Also

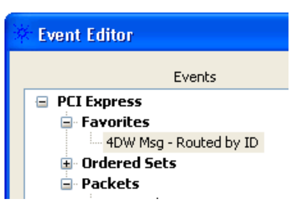
- To specify packet events (in "Find a packet" trigger function) (see page 145)

To save favorite packet events While specifying packet events using the Event Editor Dialog (see page 454), you can save the event as a favorite.

1 If desired, enter or modify the **Name** of the event.

2 Click **Add to Favorites**.

The packet event appears in the event list tree on the left side of the dialog.



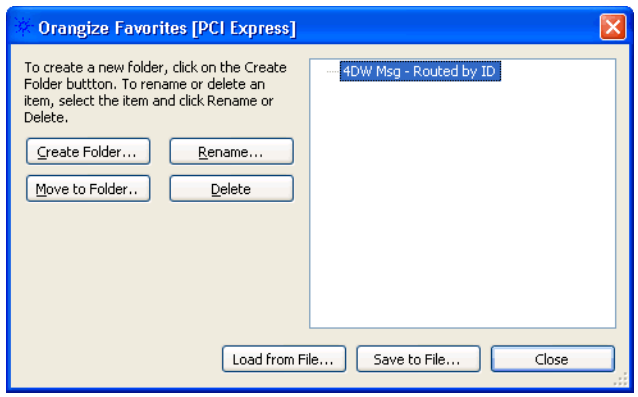
See Also

- To organize favorite packet events (see page 148)
- To specify packet events (in "Find a packet" trigger function) (see page 145)

To organize favorite packet events While specifying packet events using the Event Editor Dialog (see page 454), you can organize saved packet event favorites.

1 Click **Organize Favorites...**.

2 In the Organize Favorites dialog, you can:



- Create folders, move selected events to folders, and rename or delete selected events.
- Save favorites to a file, or load saved favorites from a file.

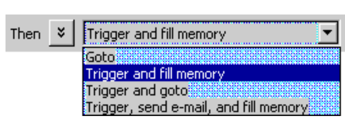
3 When you are done organizing packet event favorites, click **Close**.

See Also

- To save favorite packet events (see page 147)
- To specify packet events (in "Find a packet" trigger function) (see page 145)

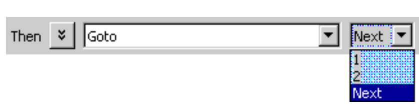
To specify a trigger sequence step's goto or trigger action

1 In the Advanced Trigger dialog, within a sequence step, select the desired trigger action:

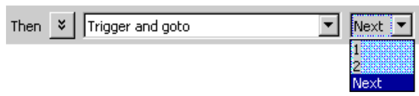


You can select:

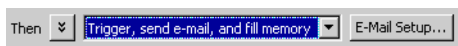
- **Goto**–To go to another trigger sequence step.



- **Trigger and fill memory**—To trigger the logic analyzer and fill memory, without going to any other steps in the trigger sequence.
- **Trigger and goto**—To trigger the logic analyzer and go to another trigger sequence step. (This can be useful when you use trigger sequence steps to specify what samples get stored.)



- **Trigger, send e-mail, and fill memory**—To trigger the logic analyzer, send e-mail, and fill memory, without going to any other trigger sequence steps. Clicking **E-Mail Setup...** opens the E-mail dialog (see page 453) for entering the e-mail address, subject, and message.



2 If you selected one of the actions that specify **fill memory** and you are in the state mode or in the store qualified timing mode with custom storage selected, enter the storage qualifier used to fill memory.

See Also

- To insert or delete events (see page 150)
- To specify default storage (see page 149)
- To insert or delete actions (in a trigger sequence step) (see page 155)

To specify default storage

Storage qualifiers are used to specify which samples (captured from the device under test) are stored in logic analyzer memory. By storing only the samples you are interested in, you can make better use of the available memory and capture activity for a greater amount of time.

Default Storage means "unless *storage control* actions or *fill memory* storage qualifiers in trigger sequence steps specify otherwise, this is what should be stored". Storage qualifiers in trigger sequence steps always override default storage.

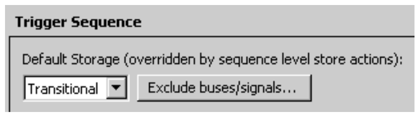
The default storage qualifier is available in state sampling mode and in the store qualified (transitional) timing mode.

In Transitional / Store Qualified Timing Mode

1 Select the type of storage qualification: either **Transitional** or **Custom**.

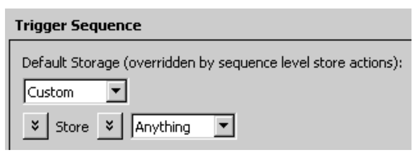
2

- When **Transitional** is selected, samples that have transitions from the previous sample are stored.



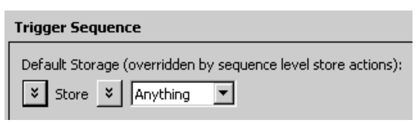
If you want exclude certain bus/signal transitions from being stored, click **Exclude buses/signals...**, and specify which buses/signals should be excluded.

- When **Custom** is selected, edit or insert events that should be stored (or not stored) in logic analyzer memory.



In State Mode

1 Edit or insert events that should be stored (or not stored) in logic analyzer memory.



See Also

- To insert or delete events (see page 150)
- To negate events (see page 154)
- To change the evaluation order of AND/OR'ed events (see page 155)
- To insert a storage control action (see page 158) (in a trigger sequence step)
- To specify a trigger sequence step's goto or trigger action (see page 148)
- Understanding Logic Analyzer Triggering, Storage Qualification (see page 393)

To insert or delete events

1 In the Advanced Trigger dialog, in a trigger sequence step, click the button associated with an event (after **Find** or **If** in trigger sequence step conditions, or after **Store** or **with** in storage qualifiers), and

choose **Insert Event After (AND/OR)**, **Insert Event Before (AND/OR)**, or **Delete Event**.

2 If inserting an event, select the type of event.

Depending on where you are inserting the event, the following event types may be available:

- **Bus/Signal**—Bus/signal value, To specify bus/signal patterns or edges (see page 144).
- **Anything**—Any sample.
- **Nothing**—No sample.
- **Timer**—A timer value, see To insert a timer event (see page 152).
- **Counter**—A counter value, see To insert a counter event (see page 152).
- **Flag**—A flag value, see To insert a flag event (see page 153).
- **Arm in from**—An arming signal from another logic analyzer module or an external instrument, see To insert an "Arm in from" event (see page 153).

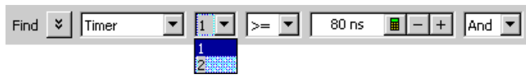
3 If inserting an event, specify whether the event should be **And**'ed or **Or**'ed with the other events.

See Also

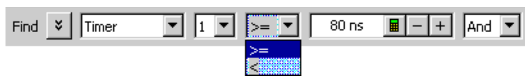
- To negate events (see page 154)
- To change the evaluation order of AND/OR'ed events (see page 155)
- Understanding Logic Analyzer Triggering, Boolean Expressions (see page 389)

To insert a timer event

1 Select the timer that you want to check.



2 Select the timer compare operator.



3 Enter the timer value to compare against.

NOTE

The **Start from reset** timer action can be placed in either the same sequence step as the timer check event, or it can be placed in a preceding trigger step. Checking a timer without starting it will generate an error.

For more information on timers, see Using Timers (see page 140).

See Also

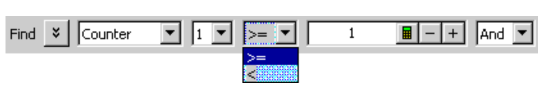
- To insert or delete events (see page 150)

To insert a counter event

A counter must be started with a counter action before it can be evaluated with a counter event.

1 Select the counter that you want to check.

2 Select the counter compare operator.



3 Enter the counter value to compare against.

For more information on counters, see Using Counters (see page 141).

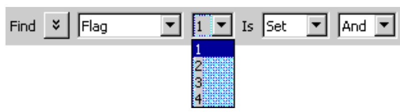
See Also

- To insert or delete events (see page 150)

To insert a flag event

NOTE Flags are not available in 1680/1690-series logic analyzers.

1 Select the flag that you want to check.



2 Enter the flag value to compare against.

There is approximately 100 ns of delay before a flag action can be seen by a flag event.

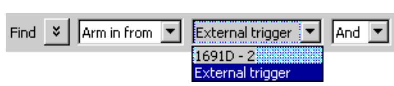
For more information on flags, see Using Flags (see page 142).

See Also

- To insert or delete events (see page 150)

To insert an "Arm in from" event

1 Specify the source of the arming signal by selecting another module or **External trigger**.



For more information on triggering on signals from other logic analyzer modules or external instruments, see Triggering From, and Sending Triggers To, Other Modules/Instruments (see page 162).

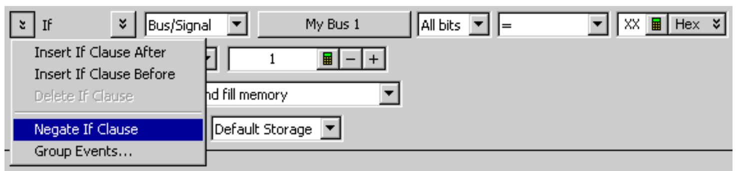
See Also

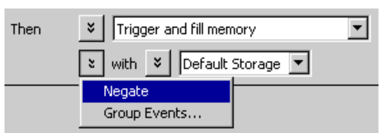
- To insert or delete events (see page 150)

To negate events

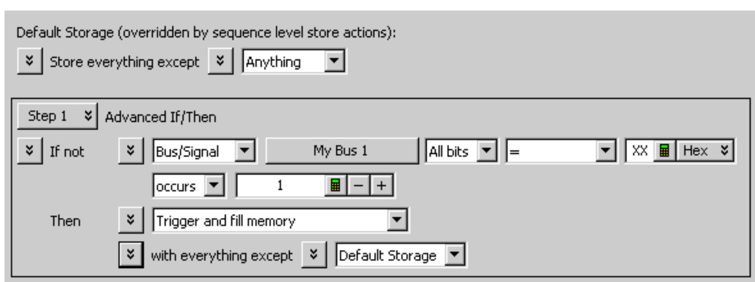
Everywhere in the Advanced Trigger dialog where you can edit or insert events, you can also negate the events.

1 Click the button associated with the events, and choose **Negate**.





Text in the dialog changes to indicate that events are negated.



NOTE

Negate is not available for storage qualifier events in the *Turbo State Mode* (see page 100).

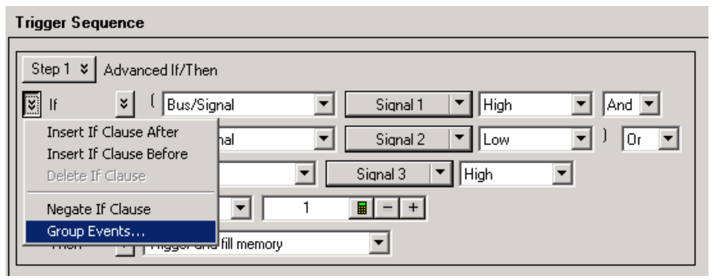
See Also

- To insert or delete events (see page 150)

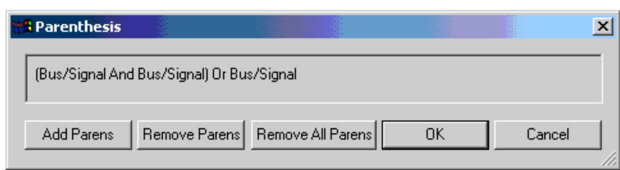
To change the evaluation order of AND/OR'ed events

When specifying advanced triggers (or after converting trigger functions to advanced *if/then* steps) and there are multiple events in an event list, you can specify their evaluation order by grouping the events.

1 In the Trigger tab's Trigger Sequence area, select the *If*, *If not*, *Else if*, or *Else if not* button; then, choose **Group Events...**.



2 In the Parenthesis dialog, either select **Add Parens** button to group events or select **Remove Parens** to ungroup events.

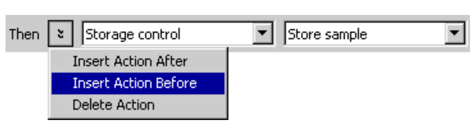


3 When you have finished grouping events, click **OK**.

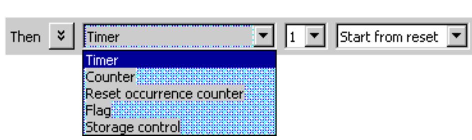
See Also • To insert or delete events (see page 150)

To insert or delete actions (in a trigger sequence step)

1 In the Advanced Trigger dialog, in a trigger sequence step, click the button associated with an action (after **Then**), and choose **Insert Action After**, **Insert Action Before**, or **Delete Action**.



2 If inserting an action, select the type of action.



The following action types are available:

- **Timer**—For starting, stopping, pausing, or resuming a timer, see To insert a timer action (see page 156).
- **Counter**—For incrementing or resetting a counter, see To insert a counter action (see page 156).
- **Reset occurrence counter**—For resetting the occurrence counter, see To insert a reset occurrence counter action (see page 157).
- **Flag**—For setting or clearing a flag, see To insert a flag action (see page 157).
- **Storage control**—For storing samples or not or for turning on/off default storage, see To insert a storage control action (see page 158).

See Also

- To insert or delete events (see page 150)

To insert a timer action

1 Select the timer that you want to specify an action for.

2 Specify the timer action by selecting either **Start from reset**, **Stop and reset**, **Pause**, or **Resume**.

NOTE

The **Start from reset** timer action can be placed in either the same sequence step as the timer check event, or it can be placed in a preceding trigger step. Checking a timer without starting it will generate an error.

For more information on timers, see Using Timers (see page 140).

See Also

- To insert or delete actions (in a trigger sequence step) (see page 155)

To insert a counter action

1 Select the counter that you want to specify an action for.

2 Specify the counter action by selecting either **Increment** or **Reset**.

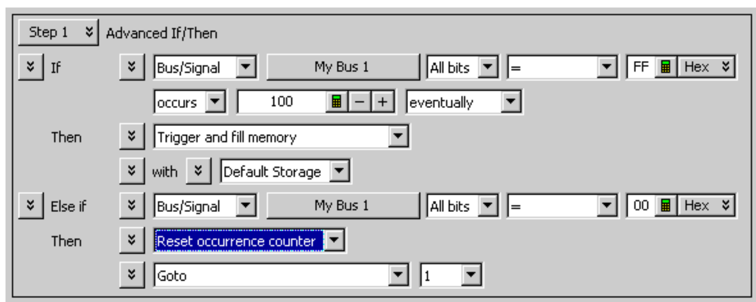
For more information on counters, see Using Counters (see page 141).

See Also

- To insert or delete actions (in a trigger sequence step) (see page 155)

To insert a reset occurrence counter action

The trigger sequence step below shows how the **Reset occurrence counter** action is used.



While searching for a number of occurrences of one event, if some other event is found, you can reset the occurrence counter and restart the search.

See Also

- To insert or delete actions (in a trigger sequence step) (see page 155)
- Understanding Logic Analyzer Triggering, Occurrence Counters (see page 391)

To insert a flag action

NOTE

Flags are not available in 1680/1690-series logic analyzers.

---

1 Select the flag that you want to specify an action for.

2 Specify the flag action by selecting either **Set**, **Clear**, **Pulse set**, or **Pulse clear**.

Flags in pulse mode sit in the opposite state when not being pulsed. If you insert a **Pulse set** action for a flag in one module, you cannot insert a **Pulse clear** action for the same flag in a different module.

NOTE Within a module, the same flag cannot be used in both pulse and level (**Set**/**Clear**) modes. If a flag action is inserted or modified with a different mode than other actions for the same flag, all actions for that flag will change to match the new mode.

3 If you selected **Pulse set** or **Pulse clear**, enter the pulse width.

NOTE Within a module, a flag's pulse width must be the same in every action for that flag. Whenever the pulse width is changed in a flag action, it changes in all other actions for that flag.

For more information on flags, see Using Flags (see page 142).

See Also

- To insert or delete actions (in a trigger sequence step) (see page 155)

To insert a storage control action

1 Specify the storage control action by selecting either **Store sample**, **Don't store sample**, **Turn on default storage**, or **Turn off default storage**.

For more information on sequence step storage and storage control actions, see Understanding Logic Analyzer Triggering, Storage Qualification (see page 393).

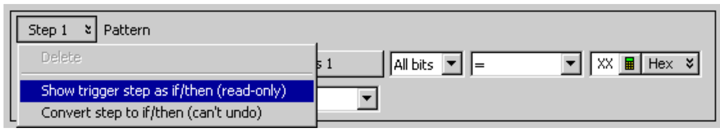
See Also

- To insert or delete actions (in a trigger sequence step) (see page 155)

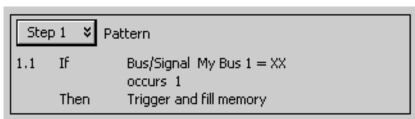
To show a trigger sequence step as Advanced If/Then trigger functions

NOTE The Advanced (If/Then or N-Way Branch) trigger functions do not allow alternative display types. By default, they are in the expanded graphical form that cannot be changed.

1 In a trigger sequence step, click **Step N** and choose **Show trigger step as if/then (read-only)**.

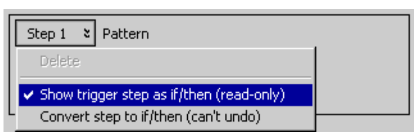


The trigger sequence step will be shown as the equivalent Advanced If/Then trigger functions in read-only form.



To undo a trigger sequence step shown as Advanced If/Then trigger functions

1 In a trigger sequence step, click **Step N** and choose the checked **Show trigger step as if/then (read-only)** item to return to the normal view of the trigger function.



See Also

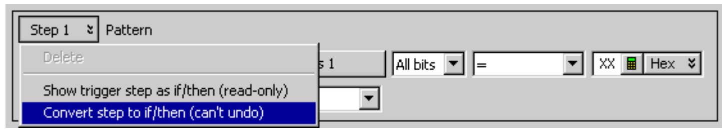
- To convert a trigger sequence step to Advanced If/Then trigger functions (see page 159)

To convert a trigger sequence step to Advanced If/Then trigger functions

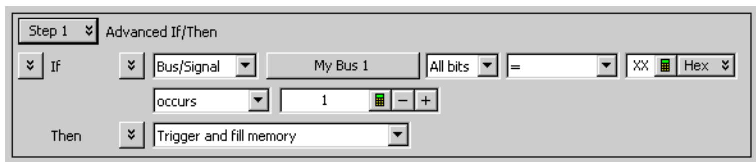
If the trigger function you need doesn't exist, start with a trigger function that is close, convert the trigger sequence step to advanced If/Then trigger functions, and edit the If/Then trigger functions.

NOTE The Advanced (If/Then or N-Way Branch) trigger functions do not allow alternative display types. By default, they are in the expanded graphical form that cannot be changed.

1 In a trigger sequence step, click **Step N** and choose **Convert trigger step to if/then (can't undo)**.



The trigger sequence step will be converted to the equivalent Advanced If/Then trigger functions.



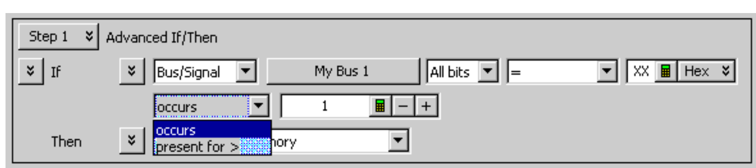
See Also

- To show a trigger sequence step as Advanced If/Then trigger functions (see page 158)
- Understanding Logic Analyzer Triggering, Branches (see page 390)

To choose between a duration or occurrence count for events (timing mode)

When specifying advanced triggers in the timing mode, you can choose between specifying an occurrence count for events or a time that the events must be present for.

1 In the trigger sequence step, select either **occurs** or **present for >** to change the setting.

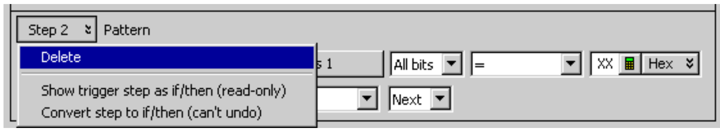


See Also

- To convert a trigger sequence step to Advanced If/Then trigger functions (see page 159)

To delete trigger sequence steps

1 In a trigger sequence step, click **Step N** and choose **Delete**.



There must be at least one trigger sequence step.

To clear the trigger sequence

1 In the Advanced Trigger dialog, click **Clear** at the bottom of the dialog.

Triggering From, and Sending Triggers To, Other Modules/Instruments

When there are multiple modules in a logic analysis system, you can cause the trigger from one module to arm another module. You can also send a module's trigger signal to an external instrument, or you can allow a signal from an external instrument to arm a module.

There are **Trigger In** and **Trigger Out** BNC connectors located on the logic analyzer (rear panel of 1680-series, front panel of 1690-series, rear panel of 16900-series). Use them to connect the analyzer to an external instrument and either send or receive a trigger signal.

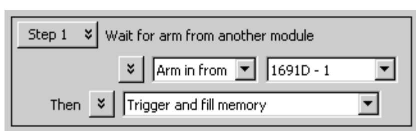
- To arm one module with another module's trigger (see page 162)
- To trigger other instruments - trigger out (see page 163)
- To trigger analyzer from another instrument - trigger in (see page 164)

To arm one module with another module's trigger

1 Click 

in the analyzer setup toolbar, or choose **Setup>(Logic Analyzer Module)>Advanced Trigger...** from the menu bar.

2 In the Advanced Trigger dialog (see page 445), select the **Other** trigger functions tab; then, drag-and-drop the **Wait for arm from another module** trigger function into the trigger sequence area.



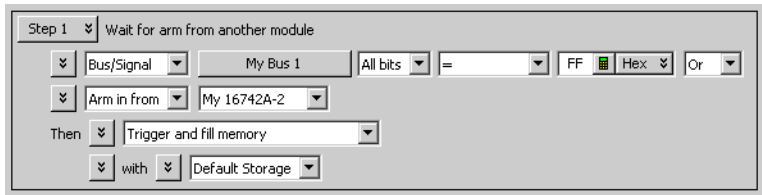
3 From the module name drop-down, select the module whose trigger will arm this module (and satisfy the event condition in the trigger sequence step).

4 Click **OK** in the Advanced Trigger dialog, and run the measurement (see Starting/Stopping Measurements (see page 168)).

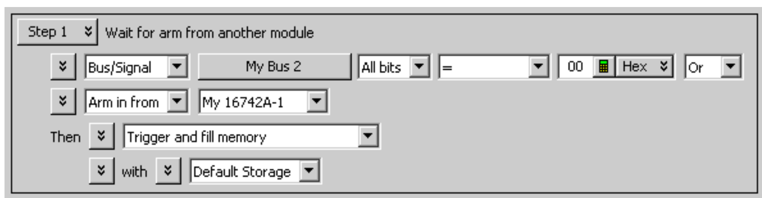
When the arm from another module is received, this module takes the actions described in the trigger sequence step.

And vice-versa You may have a situation where you have two modules looking for trigger events, and when either module finds its trigger event, the other should be armed. To do this:

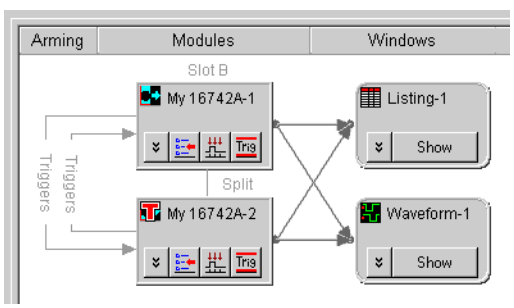
1 Set up the first module's trigger (for example, for My 16742A-1):



2 Set up the second module's trigger (for example, for My 16742A-2):



The arming setup in the Overview window looks like:



3 Run the measurement.

See Also
- Wait for arm from another module (state) (see page 526)
- Wait for arm from another module (timing) (see page 513)

To trigger other instruments - Trigger Out

1 Connect a BNC cable from the **Trigger Out** BNC to the external instrument you want to trigger.

2 Choose **Setup>External Trigger...**.

3 In the External Trigger dialog (see page 459):

   a If you are using a 1680/1690-series logic analyzer, specify whether the trigger will appear as a rising or falling edge on the **Trigger Out** BNC.

   If you are using a 16800-series logic analyzer or a 16900-series logic analysis system:

   - Enable the output.
   - Select the polarity (active high or active low).
   - Select the output mode (use feedthrough to see flag settings on the output).
   - Select the trigger and flag events that cause **Trigger Out**.

   b Click **OK**.

4 Configure the logic analyzer as you would normally for any other measurement.

5 When the analyzer's trigger sequence becomes true and the analyzer triggers, a trigger signal is sent out through the **Trigger Out** BNC to the external instrument.

See Also • External Trigger Dialog (see page 459)

To trigger analyzer from another instrument - Trigger In

1 Connect a BNC cable from the **Trigger In** BNC to the external instrument that will send the trigger signal.

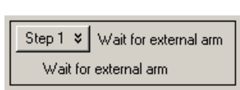
2 Choose **Setup>External Trigger...**.

3 In the External Trigger dialog (see page 459), specify whether a rising or falling edge on the **Trigger In** BNC will indicate a trigger; then, click OK.

4 Click 

in the analyzer setup toolbar, or choose **Setup>(Logic Analyzer Module)>Advanced Trigger...** from the menu bar.

5 In the Advanced Trigger dialog (see page 445), select the **Other** trigger functions tab; then, drag-and-drop the **Wait for external arm** trigger function into the trigger sequence area.



6 Click **OK** in the Advanced Trigger dialog, and run the measurement (see Starting/Stopping Measurements (see page 168)).

7 Run the measurement on the external instrument.

When the arm from the external instrument is received, the logic analyzer takes the actions described in the trigger sequence step.

See Also

- Wait for external arm (state) (see page 526)
- Wait for external arm (timing) (see page 513)
- External Trigger Dialog (see page 459)

Storing and Recalling Triggers

Triggers are stored in three ways:

- Automatically, after measurements are run, to the recently-used list.
- By storing them (see page 166) to the favorites list.
- By storing them (see page 166) to XML format trigger specification files.

You can recall triggers (see page 167) from the recently-used list, the favorites list, or from XML-format trigger specification files.

You can move recently-used triggers to the favorites list (see page 167).

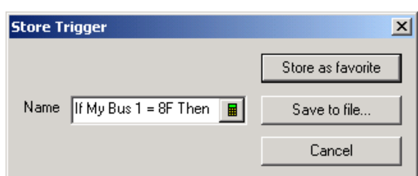
You can control the length of the recently-used and favorites list by setting the trigger history depth (see page 167).

NOTE The current trigger setup (and the favorites list) are stored as part of the logic analyzer configuration. If you load a new configuration file, the trigger setup (and the favorites list) will be overwritten.

To store a trigger

1 Choose the **Setup>(Logic Analyzer Module)>Store Trigger...** command, or in the Advanced Trigger dialog, click **Store...**.

2 In the Store Trigger dialog:



To store the trigger in the favorites list:

a Enter the name of the trigger.

b Click **Store as favorite**.

To store the trigger in an XML format file:

a Click **Save to file...**.

b In the Save As dialog, enter the name of the file, and click **Save**.

See Also

- To recall a trigger (see page 167)
- To set the trigger history depth (see page 167)

To recall a trigger

1 Choose **Setup>(Logic Analyzer Module)>Recall Trigger...** from the menu, or in the Advanced Trigger dialog, click **Recall...**.

2 In the Recall Trigger dialog (see page 476):

- Select the desired trigger from the favorites or recently-used list; then, click **OK**.
- Or, to recall a trigger from a previously saved XML format trigger specification file, click **Open...** and select the file.

To move a recently-used trigger to the favorites list

1 Choose **Setup>(Logic Analyzer Module)>Recall Trigger...** from the menu.

2 In the Recall Trigger dialog (see page 476), select the trigger from the recently-used list.

3 Click **Store Selected Recent Trigger To Favorites List**.

See Also

- To store a trigger (see page 166)

To set the trigger history depth

1 Choose the **Edit>Options...** command.

2 In the Options dialog, enter the **Trigger History Depth**.

The number you enter is used for both the recently-used trigger list and the favorites list.

See Also

- To store a trigger (see page 166)
- To recall a trigger (see page 167)

Starting/Stopping Measurements

To run the analyzer in single mode

The single run measurement captures data and fills trace memory one time. The amount of data stored during a single run is equal to the amount of trace memory allotted. For example, if trace memory is equal to 2M, the amount of data stored after one run is equal to 2M.

- From the menu bar, choose **Run/Stop>Run**, or click the icon from the run/stop toolbar (see page 424).

To run the analyzer in repetitive run mode

The run repetitive measurement captures data and fills trace memory repetitively. The amount of data stored in a repetitive run is the same as a single run. During a repetitive run, once the trace memory is full, the system clears the trace memory and begins to refill with new data. This cycle continues until the run is stopped.

- From the menu bar, choose **Run/Stop>Run Repetitive**, or click the icon from the run/stop toolbar (see page 424).

NOTE

If you are repeatedly making measurements and looking at data some fixed time after the trigger (for example), you can change the "go to trigger on run" behavior (see page 168) so that the location being displayed doesn't change after each measurement.

To view analyzer run status

- From the menu bar, choose **Run/Stop>Status...**, or click **Status...** in the status bar.

  The run status is displayed in the System Status tab of the Status dialog (see page 490).

To stop the analyzer

When a measurement is stopped, the amount of data gathered is equal to the amount of trace memory used up until the stop occurred. For example, if trace memory is equal to 2M and the measurement is stopped exactly half way through the run, the amount of data in trace memory would equal 1M.

- From the menu bar, choose **Run/Stop>Stop**, or click the icon from the run/stop toolbar (see page 424).

See Also

- To change the "Go to Trigger on Run" option (see page 168)

To change the "Go to Trigger on Run" option

After a measurement is run and it completes, the default behavior of the *Agilent Logic Analyzer* application is to display the data captured around the system trigger.

If you are repeatedly making measurements and looking at data some fixed time after the trigger (for example), you can change the "go to trigger on run" behavior so that the location being displayed doesn't change after each measurement.

1 Choose **Edit>Options...**.

2 In the Options dialog (see page 470), check or uncheck the **Go to Trigger on Run** box.

   Option settings are saved in the registry; this means your changes will be present the next time you start the *Agilent Logic Analyzer* application.

Saving Captured Data (and Logic Analyzer Setups)

You can save logic analyzer setups and captured data to configuration files. Later, the configuration files can be opened to set up the logic analyzer and re-load the data. When saving configuration files, you can choose to save only the logic analyzer setup (that is, without the data).

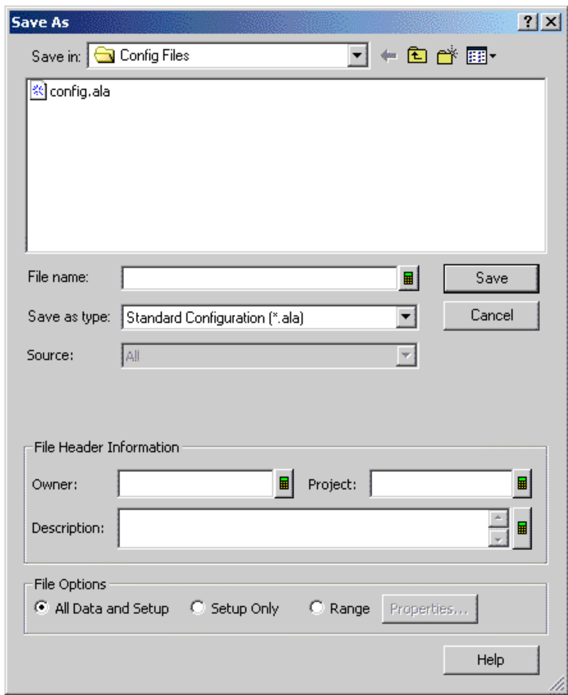
You can also save captured data to comma-separated value (CSV) files. CSV files can be imported into spreadsheet, database, or other data analysis programs.

- To save a configuration file (see page 171)
- To export data to standard CSV format files (see page 172)
- To export data to module CSV format files (see page 175)
- To export data to module binary (ALB) format files (see page 178)
- To export data to 16700 ASCII format files (see page 180)

To save a configuration file

The save feature allows you to save a configuration file for later use. The first time a file is saved the logic analyzer configuration file dialog box will appear. The **Save As...** feature allows an existing configuration file to be saved under a different name.

1 From the menu bar, select **File>Save** or select the  icon in the standard toolbar (see page 420).



2 Enter the **File name**.

CAUTION When writing to a 16900A, 16902A, or 16903A logic analysis system's DVD-ROM & CD-R/RW combination drive, the logic analysis system must be oriented horizontally; otherwise, the resulting CD-R/RW disc may not be readable on *any* CD-ROM drive.

3 Select the **Save as type**.

For information on when to use the ALA (*.ala) format and when to use the XML (*.xml) format, see ALA vs. XML, When to Use Each Format (see page 399).

4 If you are saving as an XML format file, select the **Source**.

You can save configuration information and data from all modules or individual modules.

5 If desired, fill-in the **Owner**, **Project**, and **Description** fields under the file header information. These fields help identify the configuration file when it is reopened.

6 Select the file options:

- **All Data and Setup** — if you wish to save captured data and instrument settings.
- **Setup Only** — if you wish to save only the instrument settings and not the captured data.
- **Range** — if you wish to save instrument settings and a range of captured data. Click **Properties...**; in the Range Properties dialog, specify the range.

NOTE Configuration files that include data are much larger than files that do not contain data.

7 Click **Save**.

NOTE If you are using the logic analyzer without a keyboard, you can access an on-screen keyboard by selecting **Start>Programs>Accessories>Accessibility>On-Screen Keyboard**.

See Also

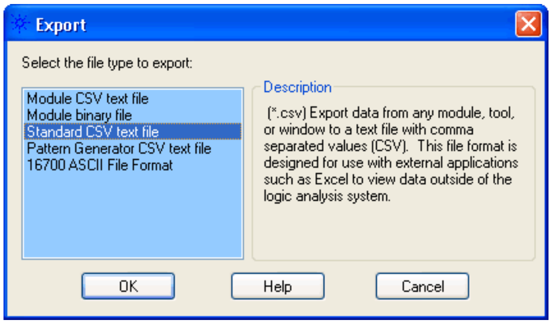
- To open a configuration file (see page 184)
- Offline Analysis (see page 197)
- ALA vs. XML, When to Use Each Format (see page 399)
- ALA Format (see page 532)
- "XML Format" (in the online help)

To export data to standard CSV format files

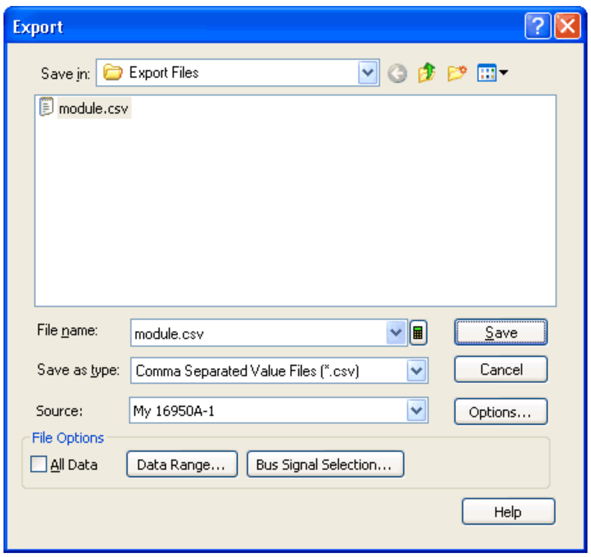
You can export captured data to standard comma-separated value (CSV) files. Standard CSV files can be imported into spreadsheet, database, or other data analysis programs.

1 From the menu bar, select **File>Export...**.

2 In the Export dialog, select **Standard CSV text file**; then, click **OK**.



3 In the following Export dialog:



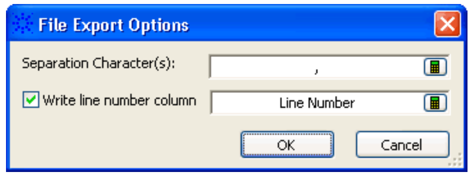
a Enter the CSV file name.

CAUTION

When writing to a 16900A, 16902A, or 16903A logic analysis system's DVD-ROM & CD-R/RW combination drive, the logic analysis system must be oriented horizontally; otherwise, the resulting CD-R/RW disc may not be readable on *any* CD-ROM drive.

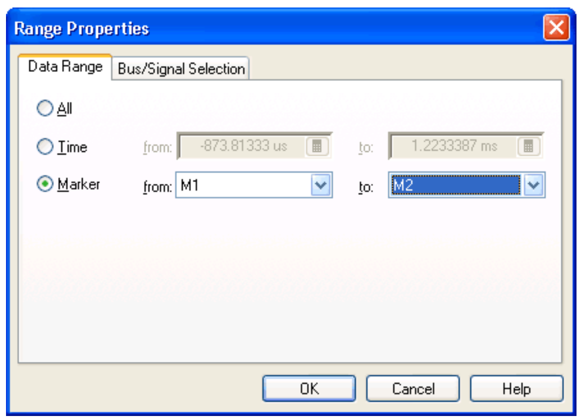
b Select the **Source** module, tool, or display window from which to export data.

c If you want to use a delimiter other than a comma, or if you want to specify that line numbers be written, click **Options...**. In the File Export Options dialog, make your selections; then, click **OK**.

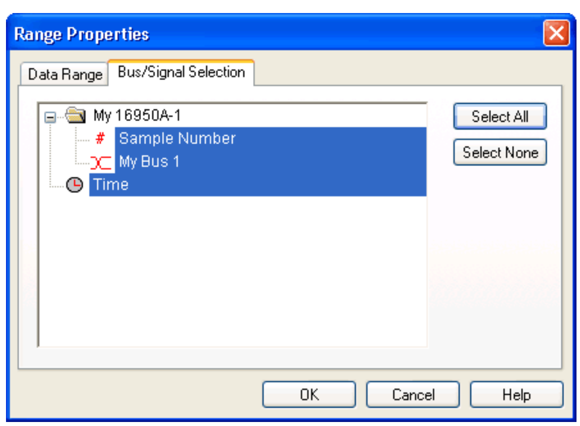


d If you want to export a range of data and/or selected bus/signal data, uncheck **All Data**.

e To specify a range of data to export, click **Data Range...**. In the Data Range tab of the Range Properties dialog, select the range by time or by markers; then, click **OK**.



f To select certain bus/signal data to export, click **Bus Signal Selection...**. In the Bus/Signal Selection tab of the Range Properties dialog, select the buses/signals whose data you want to export; then, click **OK**.



NOTE

You can only choose particular buses/signals when a module or tool is selected as the **Source** of the data export. When a display window is selected as the **Source**, all buses/signals are exported. (You can, however, delete unwanted buses/signals from a display window before exporting its data.)

4 Click **Save**.

See Also

- Standard CSV Format (see page 532)

To export data to module CSV format files

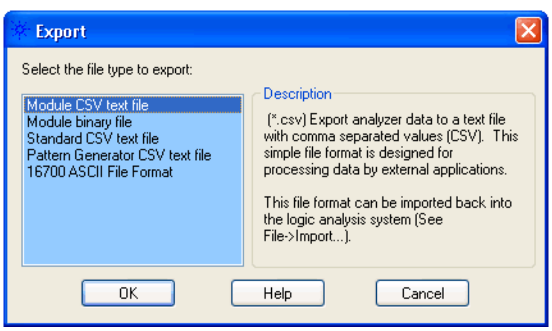
You can export captured data to module comma-separated value (CSV) files. Module CSV files can be post-processed and re-imported into the logic analysis system using a *data import module*.

CAUTION

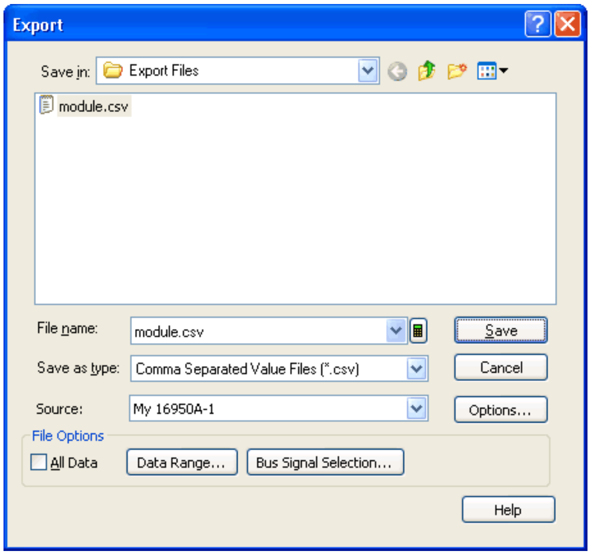
Do not modify module CSV files with Microsoft Excel. When it saves the file, Excel will change the CSV format so that the data cannot be re-imported into the logic analysis system without a lot of manual text editing.

1 From the menu bar, select **File>Export...**.

2 In the Export dialog, select **Module CSV text file**; then, click **OK**.



3 In the following Export dialog:



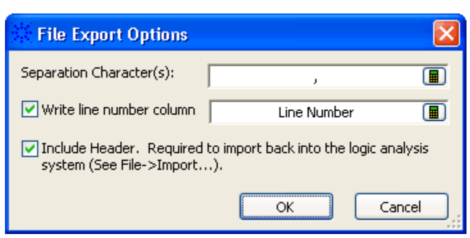
a Enter the CSV file name.

CAUTION When writing to a 16900A, 16902A, or 16903A logic analysis system's DVD-ROM & CD-R/RW combination drive, the logic analysis system must be oriented horizontally; otherwise, the resulting CD-R/RW disc may not be readable on *any* CD-ROM drive.

b Select the **Source** module from which to export data.

You can export data to module CSV format files from logic analyzer and import modules only. You can export timing zoom data from a logic analyzer module, but it must be exported separately from the module's main data.

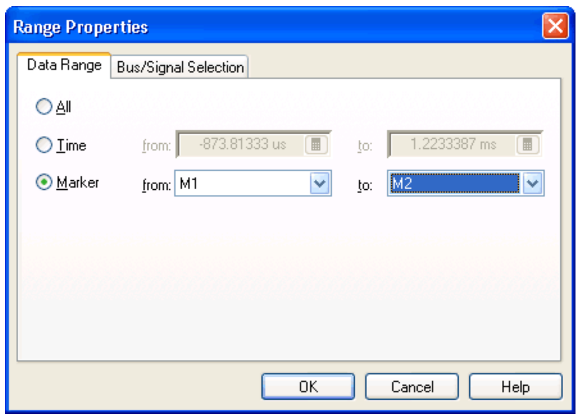
c If you want to use a delimiter other than a comma, if you want to specify that line numbers be written, or if you want to exclude the header information, click **Options...**. In the File Export Options dialog, make your selections; then, click **OK**.



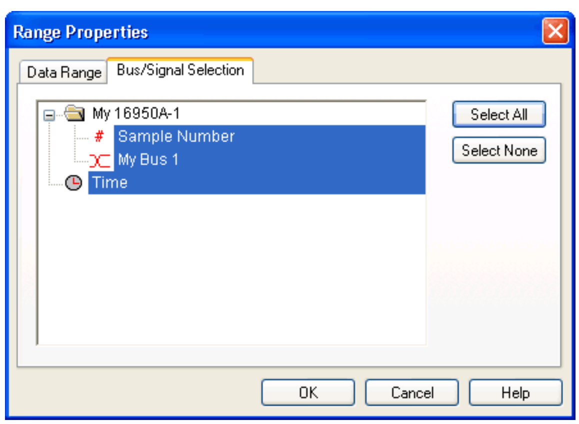
Header information must be included in order to re-import the data into the logic analysis system; however, header-less files may be easier for external tools to use.

d If you want to export a range of data and/or selected bus/signal data, uncheck **All Data**.

e To specify a range of data to export, click **Data Range...**. In the Data Range tab of the Range Properties dialog, select the range by time or by markers; then, click **OK**.



f To select certain bus/signal data to export, click **Bus Signal Selection...**. In the Bus/Signal Selection tab of the Range Properties dialog, select the buses/signals whose data you want to export; then, click **OK**.



4 Click **Save**.

See Also

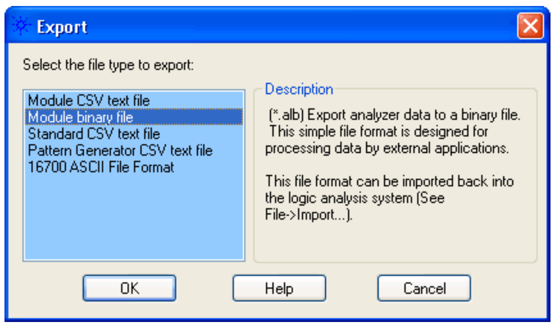
- To create a data import module (see page 191)
- Module CSV Format (see page 533)

To export data to module binary (ALB) format files

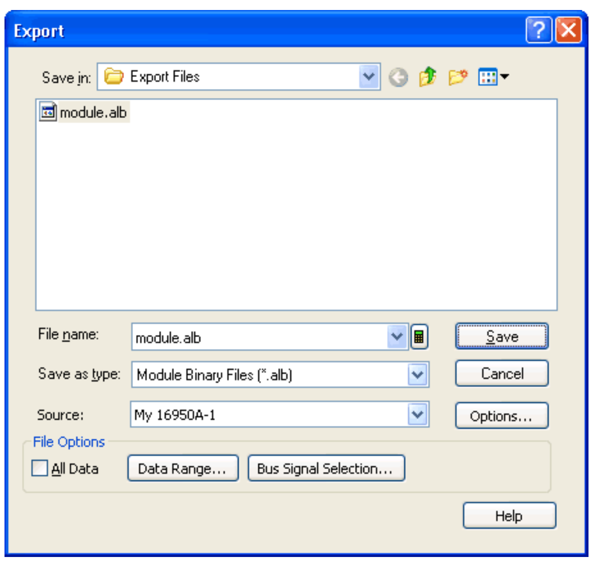
You can export captured data to module binary files. Future releases of the *Agilent Logic Analyzer* application will be able to import module binary files into the logic analysis system using a *data import module*.

1 From the menu bar, select **File>Export...**.

2 In the Export dialog, select **Module binary file**; then, click **OK**.



3 In the following Export dialog:



a Enter the ALB file name.

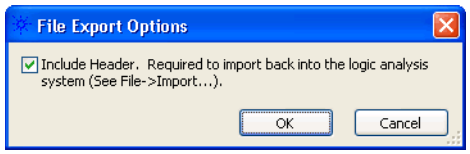
CAUTION

When writing to a 16900A, 16902A, or 16903A logic analysis system's DVD-ROM & CD-R/RW combination drive, the logic analysis system must be oriented horizontally; otherwise, the resulting CD-R/RW disc may not be readable on *any* CD-ROM drive.

b Select the **Source** module from which to export data.

You can export data to module binary format files from logic analyzer modules only. You can export timing zoom data from a logic analyzer module, but it must be exported separately from the module's main data.

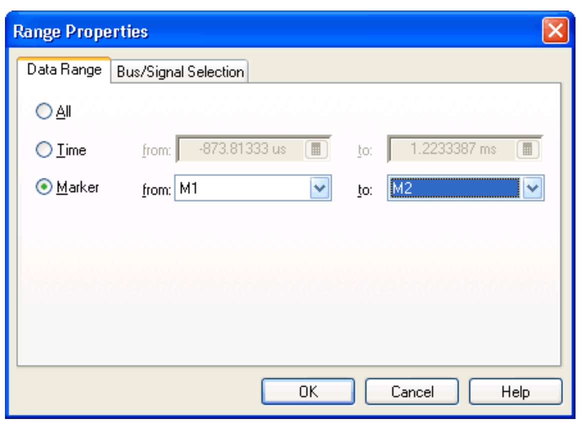
c If you want to exclude the header information, click **Options...**. In the File Export Options dialog, make your selections; then, click **OK**.



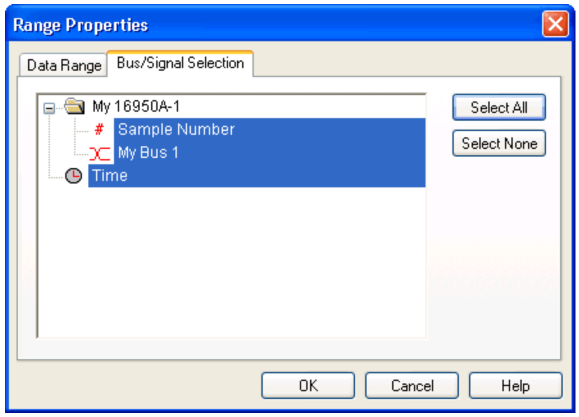
Header information must be included in order to re-import the data into the logic analysis system; however, header-less files may be easier for external tools to use.

d If you want to export a range of data and/or selected bus/signal data, uncheck **All Data**.

e To specify a range of data to export, click **Data Range...**. In the Data Range tab of the Range Properties dialog, select the range by time or by markers; then, click **OK**.



f To select certain bus/signal data to export, click **Bus Signal Selection...**. In the Bus/Signal Selection tab of the Range Properties dialog, select the buses/signals whose data you want to export; then, click **OK**.



4 Click **Save**.

See Also

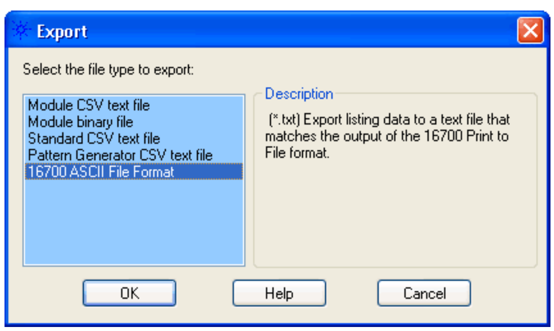
- Module Binary (ALB) Format (see page 542)

To export data to 16700 ASCII format files

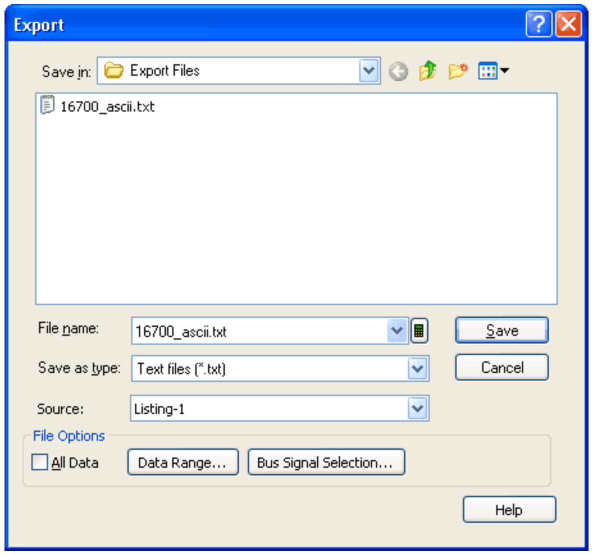
You can export captured data to a text file that matches the output of the 16700 logic analysis system's "Print to File" format.

1 From the menu bar, select **File>Export...**.

2 In the Export dialog, select **16700 ASCII File Format**; then, click **OK**.



3 In the following Export dialog:



a Enter the 16700 ASCII text file name.

CAUTION

When writing to a 16900A, 16902A, or 16903A logic analysis system's DVD-ROM & CD-R/RW combination drive, the logic analysis system must be oriented horizontally; otherwise, the resulting CD-R/RW disc may not be readable on *any* CD-ROM drive.

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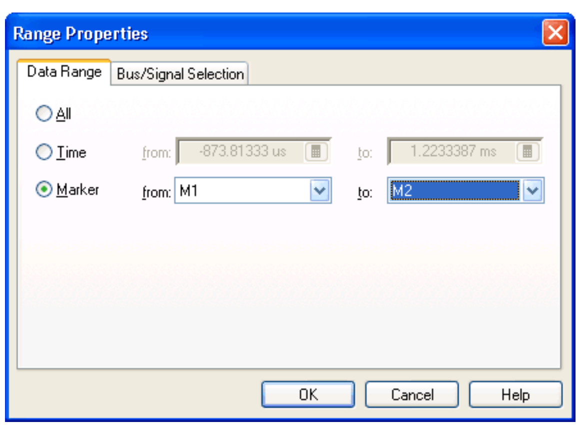
b Select the **Source** Listing display window from which to export data.

c If you want to export a range of data, uncheck **All Data**.

d To specify a range of data to export, click **Data Range...**. In the Data Range tab of the Range Properties dialog, select the range by time or by markers; then, click **OK**.



4 Click **Save**.

Extending Capture Capability with VBA

With the integrated Microsoft Visual Basic for Applications (VBA), you can extend the data capture capabilities of the logic analyzer. For example:

- In the case that the logic analyzer isn't able to trigger on the event of interest, VBA can be used to do a run, analyze the captured data looking for the event and if not found, run again. For events that are relatively frequent, this allows the logic analyzer to find events that are too complex to be able to define a trigger.
- In situations where you need a lot of data to find an elusive fault, you can set up the logic analyzer to repetitively run and save data.
- You can create dynamic triggers between repetitive runs by performing a run, modifying the trigger based on analysis of the captured data, and then running again.

These are all things you could previously do with the logic analyzer's COM automation capabilities; however, it's easier and more convenient now that VBA is integrated with the *Agilent Logic Analyzer* application.

See Also

- "Using the Advanced Customization Environment (ACE)" (in the online help)

7
Analyzing the Captured Data

Loading Saved Data and Setups

You can set up the logic analyzer and load data by opening previously saved configuration files. This lets you return to the stopping point of a previous logic analysis session, load previously saved data for *offline analysis*, or just load saved logic analyzer setups. When opening configuration files that contain data, you can choose to load only the logic analyzer setup (that is, without the data).

You can import 167xx fast binary data for *offline analysis* of data captured on 16700-series logic analyzers.

- To open a configuration file (see page 184)
- To recall a recently used configuration file (see page 186)
- To import 167xx fast binary data (see page 187)
- To transfer module setups to/from multi-module systems (see page 188)
- To set up multiple-modules with XML-format configurations (see page 188)
- Using Data Import Modules (see page 191)
  - To create a data import module (see page 191)
  - To edit data import module bus/signal definitions (see page 193)
  - To view data import module file information (see page 195)
  - To re-read data import module files (see page 196)

See Also

- Offline Analysis (see page 197)

To open a configuration file

You can open configuration files to return to a previous logic analysis session, to load previously saved data for *offline analysis*, or to load saved logic analyzer setups.

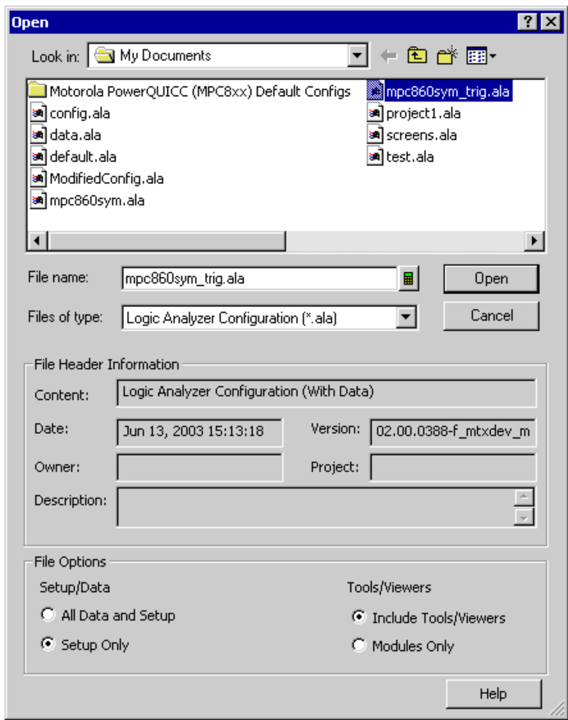
NOTE

To avoid *pod truncation* (see page 651) when opening configuration files for offline analysis, open the configuration file in a second instance of the *Agilent Logic Analyzer* application (which runs in *Offline* mode).

A quick way to start the *Agilent Logic Analyzer* application and open a configuration file is by double-clicking an ALA format configuration file in Windows Explorer. (An association for the .ala file extension was set up when the application was installed.) When you do this, however, there are no options for partial loading (setup only, modules only, etc.).

To open a configuration file from within the *Agilent Logic Analyzer* application:

1 From the menu bar, select **File>Open...** or select the icon in the standard toolbar (see page 405).



The file browser portion of the Open dialog behaves the same as other standard Windows file browser dialogs (that is, you can rename files, use right- mouse operations, etc.).

2 Select the type of configuration file you wish to open (either *.ala or *.xml).

For information on when ALA (*.ala) and XML (*.xml) formats are used, see ALA vs. XML, When to Use Each Format (see page 399).

3 Select the name of the configuration file you wish to open.

The **Content**, **Date**, **Version**, **Owner**, **Project**, and **Description** fields show information about the selected configuration file. The file was created with the *Agilent Logic Analyzer* version shown in the **Version** field. The **Date** field displays the date the configuration file was created.

4 Select the appropriate Setup/Data option.

- Select **All Data and Setup** to load the logic analyzer setup and data.
- Select **Setup Only** to load only the logic analyzer setup.

5 Select the appropriate Tools/Viewers option.

- Select **Include Tools/Viewers** to load tools and viewers, as well as modules, from the configuration file.
- Select **Modules Only** to load only the module information from the configuration file.

6 Select **Open**.

NOTE If you are using the logic analyzer without a keyboard, you can access an on-screen keyboard by selecting **Start>Programs>Accessories>Accessibility>On-Screen Keyboard**.

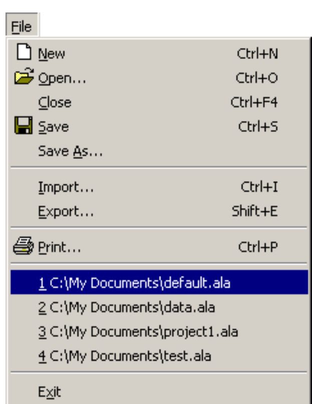
See Also

- To recall a recently used configuration file (see page 186)
- To save a configuration file (see page 171)
- To transfer module setups to/from multi-module systems (see page 188)
- Offline Analysis (see page 197)
- ALA vs. XML, When to Use Each Format (see page 399)
- ALA Format (see page 532)
- "XML Format" (in the online help)

To recall a recently used configuration file

1 From the menu bar, select **File**.

2 Select the configuration file you wish to open from the list provided.

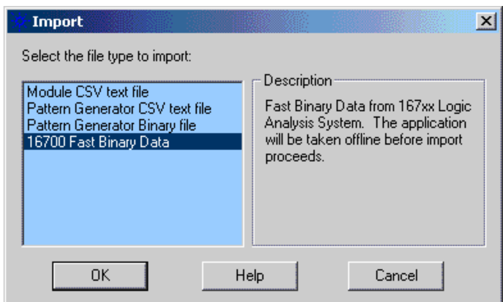


To import 167xx fast binary data

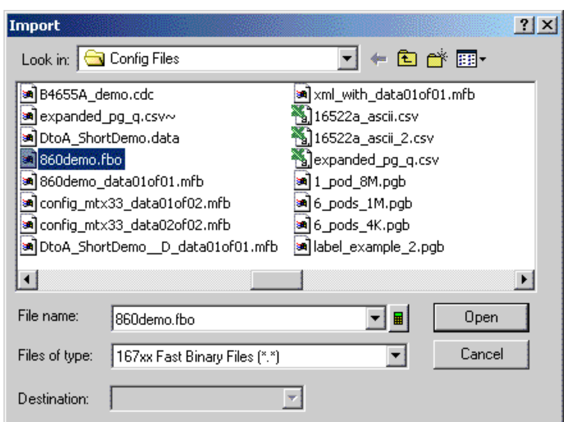
NOTE Copy 167xx Fast Binary Files to the local hard disk before importing them. Performance of the *Agilent Logic Analyzer* application is much better when fast binary data files are on the local hard disk than when they are on the network.

1 From the menu bar, select **File>Import...**.

2 In the Import dialog, select **16700 Fast Binary Data**, and click **OK**.



3 In the next Import dialog, select or enter the **File name** of the 167xx fast binary data file you wish to import.



4 Click **Open**.

Bus/signal names from a 16700-series logic analyzer fast binary data file are organized into a hierarchy of folders based on the module, analyzer, and bus/signal names.

See Also

- Analyzing 16700-Series Logic Analyzer Data (see page 198)
- 16700 Pod and Bit Association in Offline Analysis (see page 199)
- Offline Analysis (see page 197)

To transfer module setups to/from multi-module systems

You can move logic analyzer setups from one logic analysis system to another by saving/opening setups to/from configuration files. When systems have multiple modules, you must map which module setup from the configuration file gets loaded into which module in the logic analysis system.

1. Make sure the setup (configuration file) you want to load is in the proper format:
   - If the modules are compatible (for example, in the same or similar logic analyzer families like the 16740/41/42A and 16750/51/52A/B), you can use ALA format configuration files to move a setup from one module to another.
   - If the modules are not compatible, you must use XML format configuration files to move a setup from one module to another.
2. Open the configuration file (see To open a configuration file (see page 184)).
3. Answer the question about clearing all modules before loading.
4. In the Module Mapping dialog (see page 466), select **Manually specify module mapping**; then, click **Specify Mapping...**.
5. In the Specify Mapping dialog (see page 488), for the module you want load the setup into, select the module setup from the configuration file to load.
6. Click **OK** to close the Specify Mapping dialog.
7. Click **OK** to close the Module Mapping dialog and load the setup.

   When loading module setups from XML format configuration files, an information dialog describes any parsing errors or warnings.

See Also

- To save a configuration file (see page 171)
- To open a configuration file (see page 184)
- ALA vs. XML, When to Use Each Format (see page 399)

To set up multiple-modules with XML-format configurations

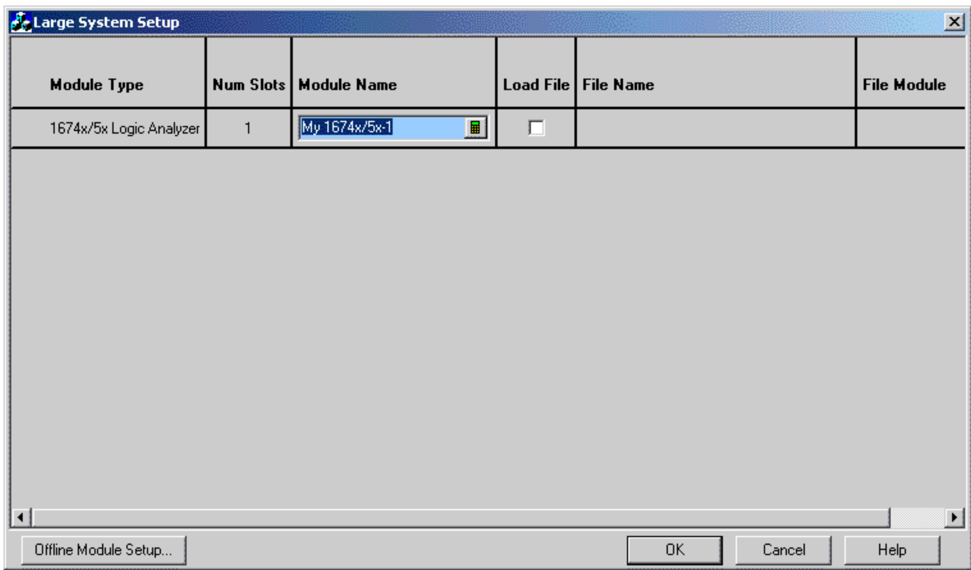
Included with the *Agilent Logic Analyzer* application is the Large System Setup utility program which makes it easy to set up large, multiple-module logic analysis systems using XML-format configuration files. For example, if your logic analysis system has several logic analyzer modules, each probing the same kind of bus, you can use the Large System Setup utility to set up each module with the same XML-format configuration file. (Doing the same thing in the main application requires many time-consuming steps.)

The Large System Setup utility program can also be used in *offline* mode. In this case, you can add as many logic analyzer modules as desired and specify XML-format configurations for each.

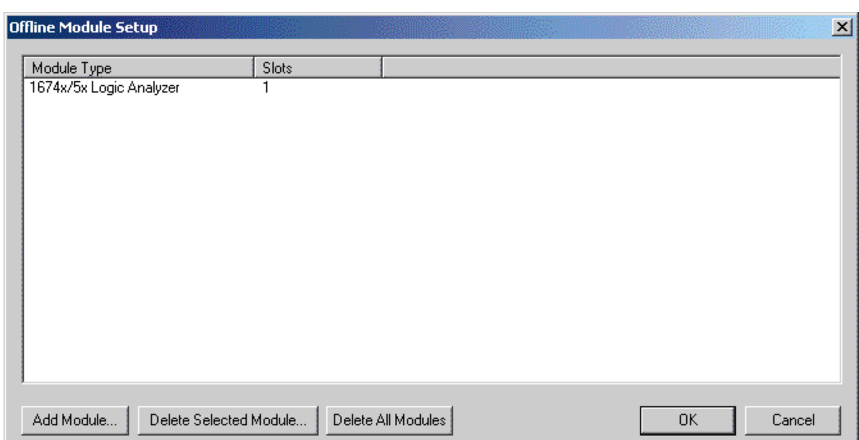
To use the Large System Setup utility program:

1 If the *Agilent Logic Analyzer* application hasn't already been started, start it, and connect to the logic analysis system you want to set up, or go offline if you want to set up in *offline* mode.

2 From the Windows Start menu, choose **Start>All Programs>Agilent Logic Analyzer>Utilities>Large System Setup**.



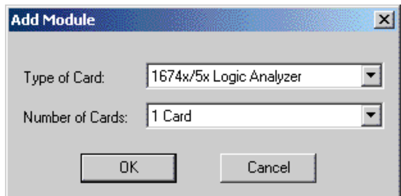
3 If you have connected to the logic analysis system you want to set up, go to step 5; otherwise, in offline mode, click **Offline Module Setup...** in the Large System Setup dialog.



4 In the Offline Module Setup dialog, for each module that you want to add:

   a Click **Add Module...**.

   b In the Add Module dialog, choose the type of card the module is made up of and the number of cards in the module.



   c Click **OK**.

   You can delete all or selected modules by clicking **Delete All Modules** or **Delete Selected Module**.

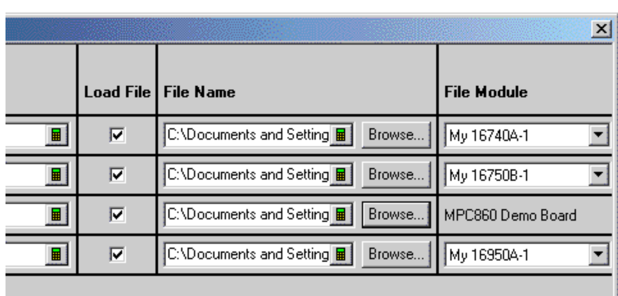
   When you are finished adding modules, click **OK** to close the Offline Module Setup dialog.

5 In the Large System Setup dialog, enter the **Module Name** for each module.

   (The module name from the XML-format configuration file is not used because the same XML file can be used to set up multiple modules.)

6 For each module that you want to configure with an XML-format configuration file, make sure the **Load File** box is checked, and click **Browse...** to select the configuration file name.

7 If the XML-format configuration files contain setups for multiple logic analyzer modules, select the file's module setup you want to use.



8 Click **OK** to close the Large System Setup dialog and set up the logic analysis system as specified.

Using Data Import Modules

Data import modules read data from module CSV or module binary (ALB) files and make it available to tools and display windows. Module CSV or module binary (ALB) files can be created by external tools or saved from any module using the main menu's **File>Export...** command.

NOTE

Data import modules are a licensed feature. You can use data import modules without a license, but the amount of data that can be imported is limited to 16 rows.

- To create a data import module (see page 191)
- To edit data import module bus/signal definitions (see page 193)
- To view data import module file information (see page 195)
- To re-read data import module files (see page 196)

Data import modules (and import file names) are saved with logic analyzer configurations (both ALA and XML format). If a configuration is saved "with data" and then opened again, the import module's data is present, and is not re-read from the import file. If a configuration is saved "without data" (setup only) and opened again, you must re-read the data import module file (see To re-read data import module files (see page 196)).

See Also

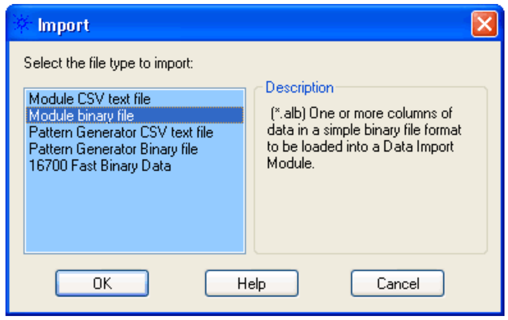
- To export data to module CSV format files (see page 175)
- Module CSV Format (see page 533)
- To export data to module binary (ALB) format files (see page 178)
- Module Binary (ALB) Format (see page 542)

To create a data import module

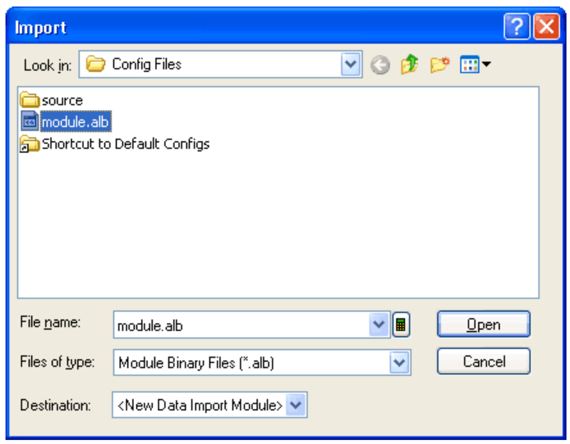
NOTE

Copy module CSV or module binary (ALB) files to the local hard disk before importing them. Performance of the *Agilent Logic Analyzer* application is much better when importing files from the local hard disk than when importing them from a network drive.

1 From the menu bar, select **File>Import...**.
2 In the Import dialog, select **Module CSV text file** or **Module binary file**, and click **OK**.



3 In the following Import dialog:

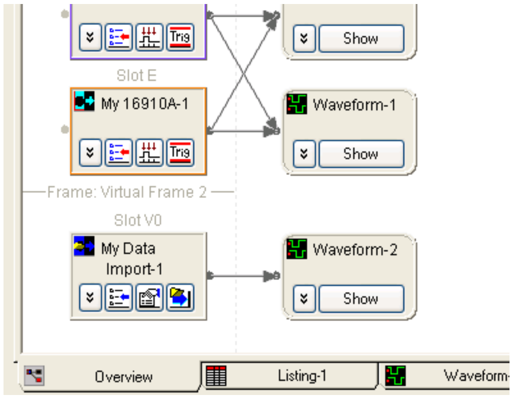


a Select or enter the **File name** of the data file you wish to import.

b Select the **Destination** of the data file you wish to import. You can choose an existing data import module or "<New Data Import Module>".

c Click **Open**.

Data import modules appear in the Overview window like other logic analyzer modules. Because the data does not come from acquisition hardware in a logic analysis system frame, a *virtual* frame is created for data import modules. You can add tools and display windows to data import modules just like you add them to logic analyzer modules.



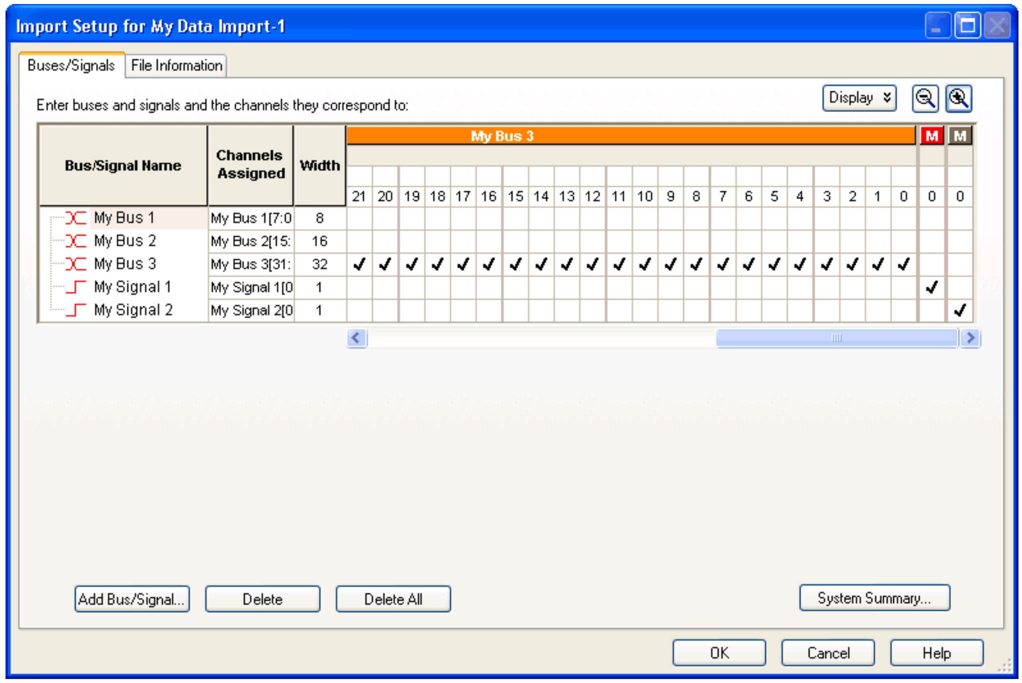
See Also

- To edit data import module bus/signal definitions (see page 193)
- To view data import module file information (see page 195)
- To re-read data import module files (see page 196)
- Module CSV Format (see page 533)
- To export data to module CSV format files (see page 175)
- Module Binary (ALB) Format (see page 542)
- To export data to module binary (ALB) format files (see page 178)

To edit data import module bus/signal definitions

1 Click in the data import toolbar, or choose **Setup>(Data Import Module)>Bus/Signals...** from the menu bar.

2 In the Import Setup dialog's Buses/Signals tab (see page 464):



Notice that *pods* are created for data value columns in the imported data file. These are like pods in logic analyzer modules except they can be any bit width.

When editing bus/signal definitions in an import module, you can:

- Add a new bus or signal.
- Delete a bus or signal.
- Rename a bus or signal.
- Assign channels in the default bit order.
- Assign channels, selecting the bit order.
- Reorder bits by editing the Channels Assigned string.
- Set the default number base.
- Set the polarity.
- Add comments.
- Add a folder.
- Alias a bus/signal name.
- Sort bus/signal names.

These operations are just like defining buses and signals in logic analyzer modules (see Defining Buses and Signals (see page 82)).

Through the **Display** button, you can select what bus/signal setup information is displayed (channels assigned, width, polarity, default base, comment, or channel numbers).

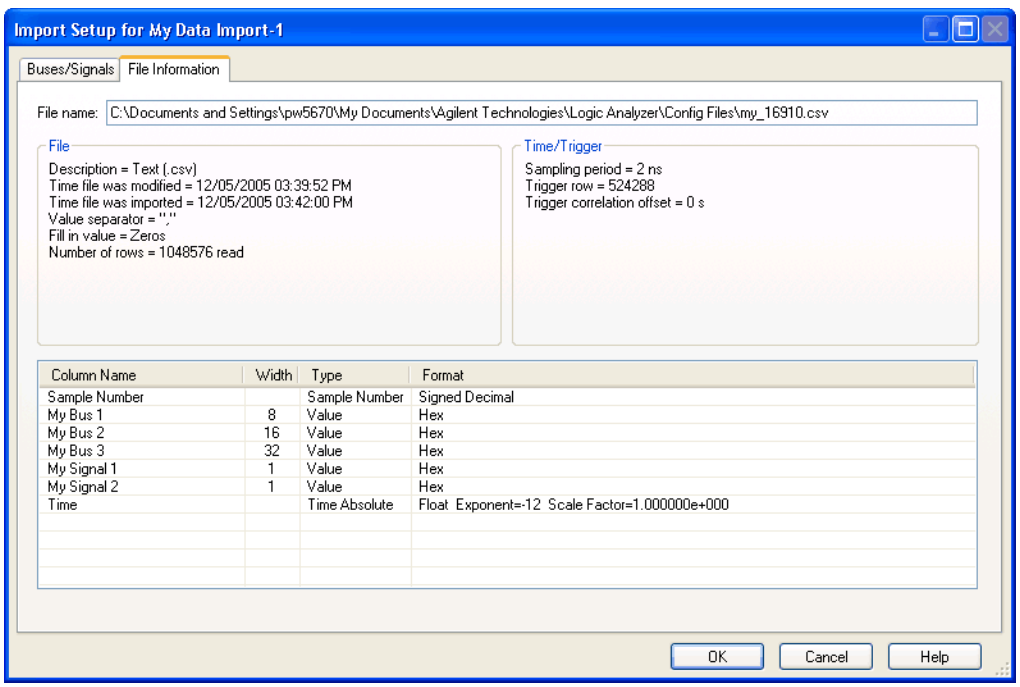
The bus and signal icons in the **Bus/Signal Name** column are normally red, but they turn gray if the bus/signal is locked by an inverse assembler.

See Also

- To view data import module file information (see page 195)
- To re-read data import module files (see page 196)
- Module CSV Format (see page 533)

To view data import module file information

1. Click in the data import toolbar, or choose **Setup>(Data Import Module)>File Info...** from the menu bar.
2. In the Import Setup dialog's File Information tab (see page 466):



- The file name and other file information is displayed.
- The time column and trigger row are displayed. The trigger correlation offset is displayed.
- The module data import file's column name, width, type, and format are displayed.

See Also

- To edit data import module bus/signal definitions (see page 193)
- To re-read data import module files (see page 196)

- Module CSV Format (see page 533)

To re-read data import module files

When you create a data import module, data is read from the imported file. You can also cause the data import file to be re-read without going through the file selection dialog again.

To re-read the data import file

Do one of the following:

- From the menu bar, choose **Run/Stop>(Data Import Module)>Read**.
- Click the  icon from the data import toolbar (see page 422) or from the data import module in the Overview window.

To view data import module read status

- From the menu bar, choose **Run/Stop>Status...**, or click **Status...** in the status bar.

  The read status is displayed in the System Status tab of the Status dialog (see page 490).

See Also

- To view data import module file information (see page 195)

Offline Analysis

Offline analysis lets you analyze captured data while the logic analyzer's data acquisition hardware is used for making other measurements.

You can use the *Agilent Logic Analyzer* application on stand-alone personal computers, 16800-series or 1680/1690-series logic analyzers, or 16900-series logic analysis systems to perform offline analysis.

By placing configuration/data files on shared file systems, offline analysis can be performed from remote locations on the network.

Example: A typical scenario is to capture data in a 16700-series logic analysis system, load the data file into the *Agilent Logic Analyzer* application for offline analysis, and then continue using the 16700-series logic analysis system to look for the next elusive defect or crash. By analyzing the data offline, you can keep your logic analyzer hardware busy making new measurements while you analyze the last one.

Example: Another scenario is to use the *Agilent Logic Analyzer* application to configure and exchange logic analyzer configuration files containing trigger setups with a team of colleagues located on-site or in remote locations.

General offline analysis considerations

- To analyze data from 16700-series logic analyzers, the data must be saved in the fast binary data format. This is done using the File Out Tool (see Analyzing 16700-Series Logic Analyzer Data (see page 198)).
- When analyzing data offline, there is no data acquisition hardware, so functions such as triggering, hardware assist, and run functions are not available.
- Multiple instances of the *Agilent Logic Analyzer* application can be displayed side-by-side on a logic analyzer or a personal computer, but their data cannot be time-correlated.
- You can install the *Agilent Logic Analyzer* on any computer meeting the minimum PC requirements (see page 201); however, licensed tools require a license for each computer they run on.

For more specific information about offline analysis, see:

- Analyzing 16700-Series Logic Analyzer Data (see page 198)
- Offline Analysis on Logic Analyzers (see page 199)
- Offline Analysis on Personal Computers (see page 200)

To return to online analysis, see:

- Connecting to a Logic Analysis System (see page 63)

See Also

- Offline File Formats (see page 201)

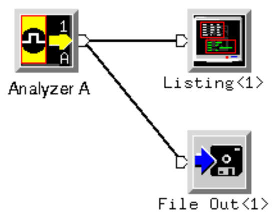
Analyzing 16700-Series Logic Analyzer Data

Before you can analyze 16700-series logic analyzer data with the *Agilent Logic Analyzer* application, you must save the measurement data in fast binary out format using the File Out Tool.

The following example shows the general process to use. Refer to the 16700-series logic analysis system online help for any specific information.

1 Configure the 16700-series logic analyzer to capture the desired data.

2 Connect a File Out Tool.



Data loaded for offline analysis must appear as one data set. Data from a two-machine measurement (as with Pentium 4 processor solution data, for example) must be merged before saving as fast binary output data; in other words, both machines must feed into the same File Out tool.

3 Configure the File Out tool to save the measurement data in fast binary out format.

For better search performance, limit the size of fast binary data files by using the partial fast binary out option.

NOTE If you want the File Out Tool to save the fast binary out file directly to a shared drive, be sure to configure all LAN connections (see page 307) to enable file sharing.

4 Run the 16700-series logic analyzer to capture the data.

5 Copy the fast binary data file to the local hard disk of the personal computer or logic analyzer on which the *Agilent Logic Analyzer* application runs.

Performance of the *Agilent Logic Analyzer* application is much better when fast binary data files are on the local hard disk than when they are on the network.

6 In the *Agilent Logic Analyzer* application, use the **File>Import...** command to import from the fast binary data (see page 187) file.

More 16700 considerations

- Only bus/signal names and measurement data are saved in the fast binary out format.

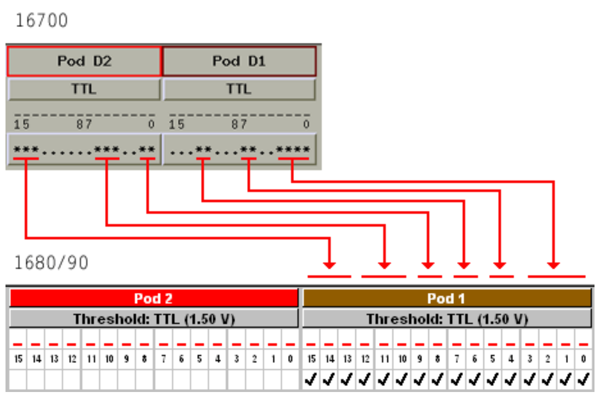
- The 16700 pod and bit association is collapsed (see page 199) when viewed in the *Agilent Logic Analyzer* application.
- After importing fast binary data files, you cannot use the Bus/Signal Setup dialog to add new bus/signal names or change the channel assignments of the imported bus/signal names. You can, however, change bus/signal polarity, rename or delete buses/signals, and add comments.
- Because 16700-series logic analyzer sampling mode options cannot be used to set up a 1680/1690-, 16800-, or 16900-series logic analyzer, the Timing/State Sampling Mode Setup dialog is not available.

See Also

- 16700 Pod/Bit Association in Offline Analysis (see page 199)

16700 Pod and Bit Association in Offline Analysis

The offline analysis application will display the 16700 pod and bit association differently. For any given bus/signal, all assigned bits across all pods in the 16700 interface is converted to sequentially ordered bits under sequentially ordered pods, starting with pod 1.



Offline Analysis on Logic Analyzers

You can perform offline analysis with 16800-series or 1680/1690-series logic analyzers or 16900-series logic analysis systems, in general, by running a second instance of the *Agilent Logic Analyzer* application and loading previously saved data into that instance. With two instances of the application running, one in online (either *Local* or *Remote*) mode and one in *Offline* mode, you can continue making measurements in one instance while you perform offline analysis in the other.

You can perform offline analysis on fast binary data files saved from 16700-series logic analyzers as well as configuration files (.ala format) from any 16800-series or 1680/1690-series logic analyzer or 16900-series logic analysis system.

Keep these things in mind when performing offline analysis with a logic analyzer or logic analysis system:

- You can start multiple instances of the *Agilent Logic Analyzer* application.

  If logic analyzer acquisition hardware is present, the first instance opens in online (either *Local* or *Remote*) mode. If acquisition hardware is not present, the first instance opens in *Offline* mode.
- Logic analyzer run functions do not work in *Offline* mode.
- In the *Offline* mode, you can continue to create triggers and save them in configuration files that can be opened by other instances of the *Agilent Logic Analyzer* application.
- If you import 167xx fast binary data into an online (either *Local* or *Remote*) instance of the *Agilent Logic Analyzer* application, the application automatically switches to *Offline* mode, and all hardware functions are automatically turned off.
- If you open a logic analyzer configuration (.ala) file for offline analysis in an online (either *Local* or *Remote*) instance of the *Agilent Logic Analyzer* application, run functions will overwrite the data that has been loaded.

NOTE To open, copy, or save files directly from shared disk drives, make sure to configure all LAN connections (see page 307) to enable file sharing.

See Also

- To open a configuration file (see page 184)
- To import 167xx fast binary data (see page 187)
- To save a configuration file (see page 171)

Offline Analysis on Personal Computers

A personal computer (PC) with the *Agilent Logic Analyzer* application installed can perform offline analysis on fast binary data files saved from a 16700-series logic analyzer as well as configuration files (.ala format) from any 16800-series or 1680/1690-series logic analyzer or 16900-series logic analysis system.

When using the *Agilent Logic Analyzer* application by itself on a PC for offline analysis:

- The logic analyzer run functions are not available (because there is no acquisition hardware).

- You can save logic analyzer setups (including trigger sequences) to .ala format configuration files, and you can pass these files between personal computers (running the *Agilent Logic Analyzer* application) and other 16800-series or 1680/1690-series logic analyzers or 16900-series logic analysis systems.
- You can have more than one instance of the *Agilent Logic Analyzer* application running.
- Licensed tools require a license for each computer they run on.

NOTE To open, copy, or save files directly from shared disk drives, make sure to configure all LAN connections (see page 307) to enable file sharing.

See Also

- To open a configuration file (see page 184)
- To import 167xx fast binary data (see page 187)
- To save a configuration file (see page 171)
- Minimum PC Requirements (see page 201)

Minimum PC Requirements

Minimum PC requirements for offline analysis:

- Processor and Memory: 1 GHz processor, 512 M RAM.
- Operating System: Windows® XP/2000.
- Service Pack: Windows XP Service Pack 2 or Windows 2000 Service Pack 3.

Offline File Formats

.ala Format You can open logic analyzer configuration files (.ala (see page 532) extension) for offline analysis. These files are saved by the *Agilent Logic Analyzer* application.

The logic analyzer configuration (.ala) file format is an internal format used by the *Agilent Logic Analyzer* application for saving and re-opening setups and data. ALA format configuration files contain everything that is needed to restore a session (in other words, the information necessary to reconstruct the display appearance, instrument settings, and optionally, captured data).

.xml Format Generic configuration files (".xml" (in the online help) extension) can be used when setting up the logic analysis system configuration when importing fast binary data format files for offline analysis. XML format configuration files are saved by the *Agilent Logic Analyzer* application.

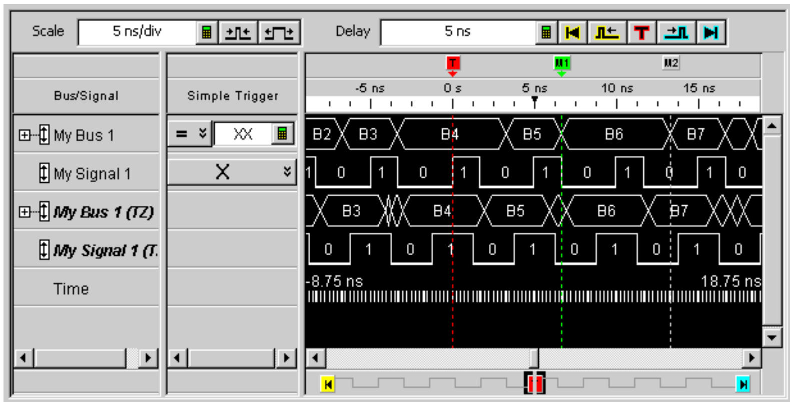
The generic configuration (.xml) file format is an eXtensible Markup Language format that can be edited (using an ASCII text editor) and post-processed by scripts (or other tools) and re-opened by the *Agilent Logic Analyzer* application. These files contain buses/signals, channels assigned to buses/signals, and user-defined symbols.

Fast Binary Data Format You can import Fast Binary Data Format files (no common file extension) for offline analysis. These files are created on a 16700-series logic analysis system using the *File Out* tool. These files contain buses/signals and data from the 16700-series logic analyzer.

CSV Format You can export captured data to CSV (Comma-Separated Values) Format (see page 532) files (.csv extension) for offline analysis in other applications like Excel. These files contain buses/signals and data.

Analyzing Waveform Data

The Waveform window displays captured data as a digital waveform. You can configure the window to display selected buses and signals with time or pattern markers in the data. You can also set up bus pattern triggers and signal trigger options.



The Waveform window is accessed through the menu bar's **Window>Waveform** command. If you have Tabbed Windows (see page 305) turned on, you can also select a tab at the bottom of the window.

- To change the display scale (time/division) (see page 204)
- To go to different locations in the captured data (see page 206)
- To re-arrange waveforms (see page 207)
- To overlay waveforms (see page 207)
- To find a bus/signal row (see page 208)
- To view bus data as a chart (see page 209)
- To show/hide parts of the waveform display (see page 211)
- To insert or delete buses/signals (see page 211)
- To group signals into a bus (see page 212)
- To expand/collapse buses (see page 212)
- To insert separator rows (see page 212)
- Changing Waveform Window Properties (see page 213)
  - To change the waveform background color (see page 214)
  - To change the overlaid waveform color (see page 214)
  - To change the filtered data color (see page 214)
  - To change the timing zoom background color (see page 215)
  - To change the waveform font size (see page 215)

  - To change the Fast Zoom In option (see page 215)
  - To lock scrolling with other display windows (see page 216)
  - To change the waveform tool tip display (see page 216)
- Changing Bus/Signal Row Properties (see page 216)
  - To change a waveform's color (see page 218)
  - To change a waveform's height (see page 218)
  - To change a bus/signal's number base (see page 218)
  - To show/hide a bus/signal's numeric data values (see page 219)
- Changing Analog Signal Row Properties (see page 219)
  - To change the analog properties (see page 220)

See Also

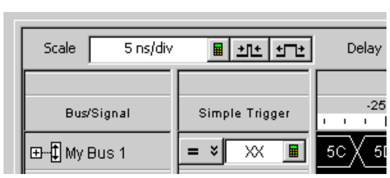
- Defining Buses and Signals (see page 82)
- Setting Up Quick (Draw Box) Triggers (see page 129)
- Specifying Simple Triggers (see page 133)
- Marking, and Measuring Between, Data Points (see page 234)
- Setting Up Symbols (see page 116)
- Displaying Names (Symbols) for Bus/Signal Values (see page 232)
- Searching the Captured Data (see page 257)

To change the display scale (time/division)

The Waveform window displays data similarly to an oscilloscope, that is, waveforms on a horizontal time axis. Therefore, to zoom in or out on a waveform, you simply change the Scale (time/division) of the time axis that the waveform is viewed with.

To change the scale by clicking the zoom out/in buttons

1 Click the zoom out/in buttons to raise/lower the time/division scale.



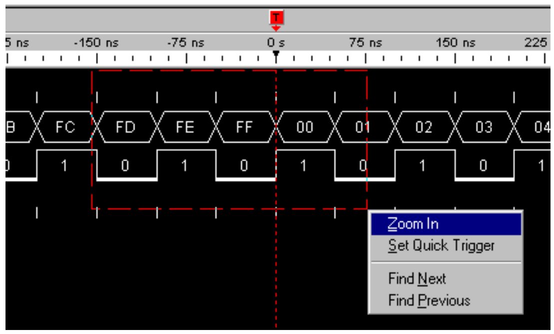
The scale ranges from 1 ps/div to 1 ks/div.

You can also change the time/division by entering a numeric value in the **Scale** field.

To zoom in by drawing a rectangle in the data

1 Point the mouse to the upper-left corner of the desired view area; then, click and hold while moving the mouse to the lower-right corner; then, release the mouse button.

2 If the Fast Zoom In (see page 215) option is not selected, choose **Zoom In** from the popup menu.

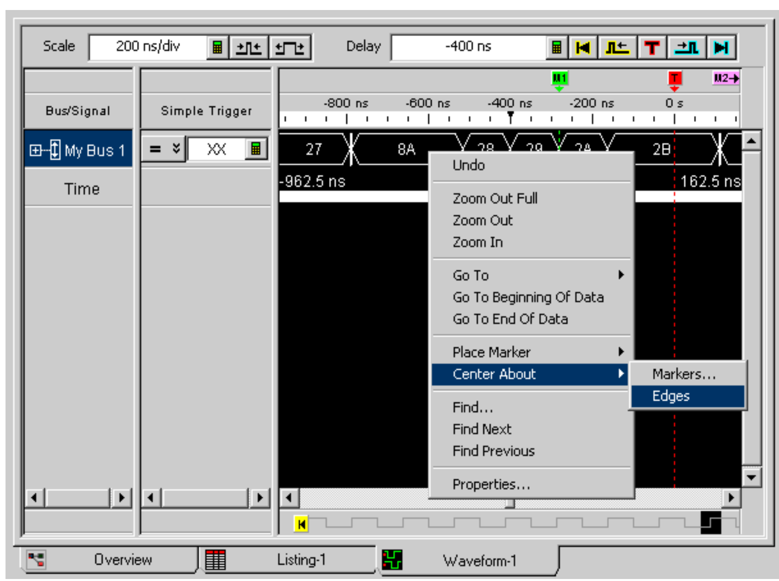


The new display scale is adjusted to the width of the box drawn.

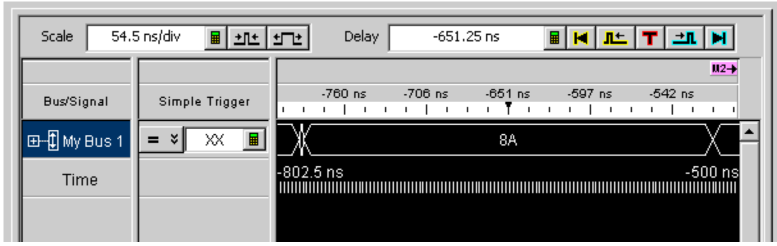
To center about edges

1 Position the mouse cursor over a waveform, between the edges you want to center the display about.

2 Right-click and choose **Center About>Edges**.



The new display scale is adjusted to the width of the waveform edges.

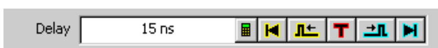


To go to different locations in the captured data

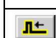
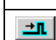
In the Waveform display window, you can go to different locations in the captured data by using the horizontal scroll bars, by using the Delay field and buttons, or by choosing Go To commands from popup menus.

To go to different locations by changing the delay

1 Click one of the buttons in the Delay field or enter a delay value.

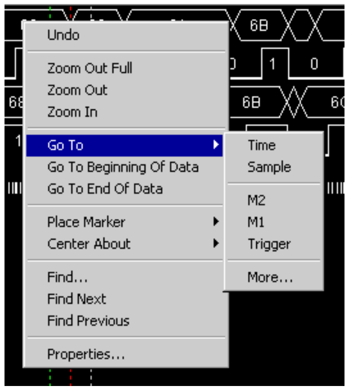


The delay adjusts the display window relative to the waveform data. The display window's relative position in time is dependent on the trigger point, and the beginning and end of data. Use the following delay controls to position the display window over the desired data.

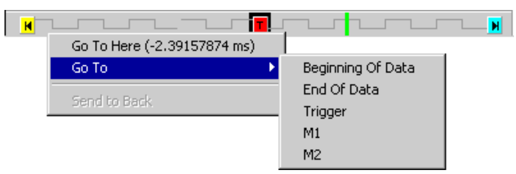
	Use the keypad to enter a numeric value. If the value you enter is greater than or less than the time of the data range, the window will be moved to the beginning or end limit.
	Moves the window over the beginning of data.
	Scrolls the window towards the beginning of data.
	Moves the window over the trigger point.
	Scrolls the window towards the end of data.
	Moves the window over the end of data.

To go to different locations using popup menus

1 Right-click in the waveform display area, and choose one of the **Go To** commands.



Or, click in the marker overview bar, and choose one of the **Go To** commands.



You can choose **Beginning Of Data**, **End Of Data**, **Trigger**, a marker, a **Time**, or a **Sample**.

To re-arrange waveforms

1 Position the mouse pointer over the bus/signal name associated with the waveform you want to move.
2 Click and hold the mouse button.
3 Drag-and-drop the bus/signal to its new position.

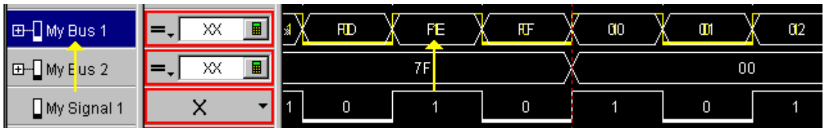
The name is placed above the red position indicator that appears.

See Also

- To overlay waveforms (see page 207)
- To expand/collapse buses (see page 212)

To overlay waveforms

Use the Overlay feature to place multiple bus or signals into one row of displayed data. When multiple signals are overlaid, you can see the relationships visually between all signals. The overlaid bus or signal is drawn first, then the main bus/signal is drawn last as to overwrite the overlaid bus/signals for clarity.



1 Right-click on the bus or signal you want to overlay another bus or signal onto, then select **Overlay...** .

2 From the Overlay selection dialog that appears, select the bus or signal you want to overlay onto the highlighted bus or signal.

   You can overlay analog signals (from an " external oscilloscope module" (in the online help)) with digital signals or with other analog signals.

NOTE The scaling for an original analog signal is used for *all* signals overlaid onto its row; therefore, if user-defined scaling and offset values are used, it is possible that overlaid signals may not be visible. When automatic scaling is used, it will take into account the minimum and maximum voltages of *all* overlaid signals, and all signals will be visible.

3 If you want to change the color of the overlaid bus or digital signal, see To change the overlaid waveform color (see page 214).

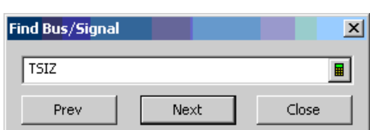
   When analog signals are overlaid onto other signals, the overlay signal color comes from the external oscilloscope module's setup options (which you can access by right-clicking the analog signal name, choosing **Assign Channels...**, and selecting the " Options tab" (in the online help)) instead of the Waveform window's overlay color setting.

To find a bus/signal row

When there are many bus/signal rows in the Waveform display window, you can search for a particular bus/signal row instead of scrolling through all the rows.

1 In the Waveform display window, right-click in the Bus/Signal column, and choose **Find Bus/Signal...**.

2 In the Find Bus/Signal dialog, enter the name (or part of the name) of the bus/signal you wish to find.



3 Then, click:

- **Prev** — to search for the string backward in the bus/signal rows.
- **Next** — to search for the string forward in the bus/signal rows.

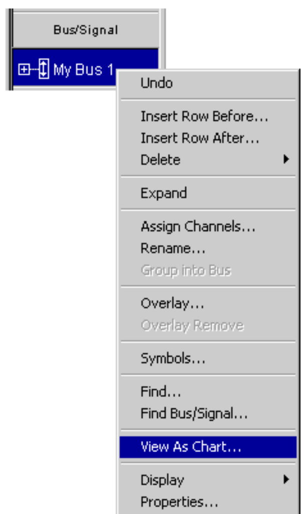
- **Close** – to close the Find Bus/Signal dialog.

To view bus data as a chart

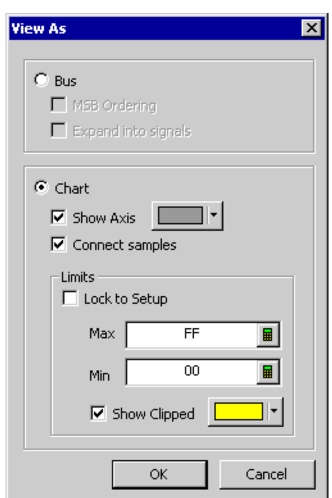
You can view bus data values as a chart instead of the conventional bus shape.

1 In the Waveform display window, right-click on a bus name, and choose **View As Chart...**.

Or, in the Waveform Properties dialog's Row Properties tab, for the **Bus** property, click **View As...**.



2 In the View As dialog, set the following options:



- **Show Axis** — causes a small axis, which represents the center of the range of values being displayed, to be drawn in the center of the waveform. When checked, you can also change the axis color.
- **Connect Samples** — causes lines to be drawn between samples.
- **Lock to Setup** — sets the range limits based on the width of the bus. For example, an 8-bit bus is set to a range of 0-255.
- **Max/Min** — sets the range limits of the displayed axis.
- **Show Clipped** — enables out-of-range data values to be displayed in a user-defined color.

NOTE Because there is no hardware to accelerate chart drawing, Waveform windows that have charts draw slowly. You may want to place buses viewed as charts in a separate Waveform window.

To view bus data as a bus

You can return the bus waveform appearance to a conventional bus shape.

1 In the Waveform display window, right-click on a bus name, and choose **View As Bus...**.

Or, in the Waveform Properties dialog's Row Properties tab, for the **Bus** property, click **View As...**.

2 In the View As dialog, check or uncheck the following options as desired:

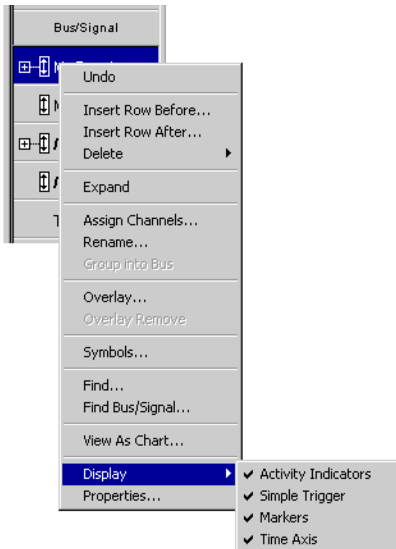
- **MSB Ordering** — the ordering of the signals in the bus are changed from least significant bit first to most significant bit first.
- **Expand into signals** — expands the bus into individual signals (as if you selected the Expand (+) field to the left of the bus name).

See Also

- Changing Bus/Signal Row Properties (see page 216)

To show/hide parts of the waveform display

1 Right-click in the Bus/Signal column of the Waveform display, and choose **Display>**.



Then, check or uncheck one of the following to show or hide that part of the Waveform display window:

- **Activity Indicators** — either a low bar (low level), high bar (high level), or a transition arrow (transitioning signal) displayed to the left of bus/signal names.
- **Simple Trigger** — the Simple Trigger column.
- **Markers** — the markers display bar (see page 431).
- **Time Axis** — the time axis (and column headings).

You can also make these selections in the **Display Options** area of the Waveform Properties dialog's Window Properties tab.

See Also • Changing Waveform Window Properties (see page 213)

To insert or delete buses/signals

To insert buses/signals

1 In the Waveform display window, right-click in the Bus/Signal column; then, choose **Insert Row**.

2 In the Insert dialog, select the buses/signals you want to insert; then, click **OK**.

To delete selected buses/signals

1 In the Bus/Signal column, highlight the buses/signals you want to delete (by clicking, Shift-clicking, or Ctrl-clicking the bus/signal names).

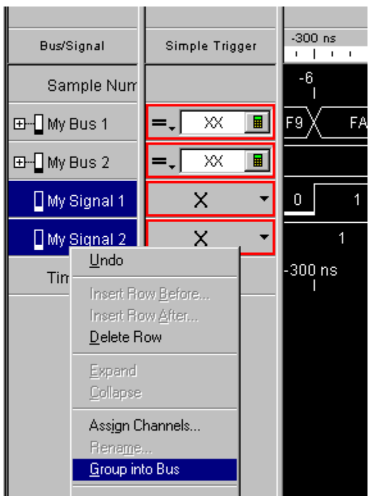
2 Right-click in the Bus/Signal column; then, choose **Delete>Row**.

See Also • Defining Buses and Signals (see page 82)

To group signals into a bus

1 While holding the shift key down, click on all desired signals.

2 With the mouse pointer over any one of the highlighted signals, right-click and select **Group into Bus**.



To expand/collapse buses

In the Waveform display window's Bus/Signal column:

- Click the "+" or "-" symbol associated with a bus.
- Right-click the bus, and choose **Expand** or **Collapse**.

See Also • Defining Buses and Signals (see page 82)

To insert separator rows

To add distance between waveforms, you can add separator rows to the Waveform display window.

1 In the Waveform display window, right-click in the Bus/Signal column; then, choose **Insert Separator**.

Separator rows can be sized, colored, re-arranged, and deleted just like bus/signal waveform rows.

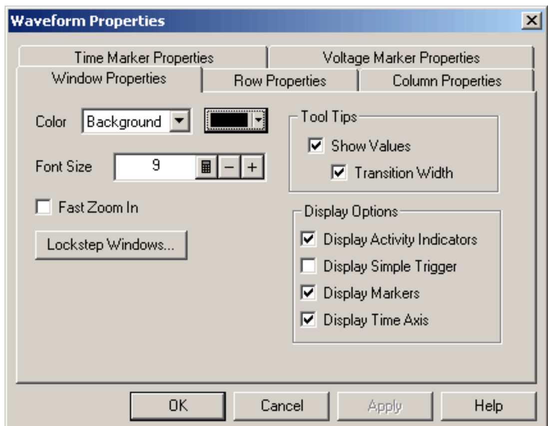
Changing Waveform Window Properties

You can change properties that affect the entire Waveform display window.

1 Right-click in a blank area of the waveform display, and choose **Properties...**.

   Or, with no bus/signal names selected, choose **Edit>Window Properties...** from the main menu.

2 In the Waveform Properties dialog's Window Properties tab:



   You can:

   - Change the waveform background color (see page 214)
   - Change the overlaid waveform color (see page 214)
   - Change the filtered data color (see page 214)
   - Change the timing zoom background color (see page 215)
   - Change the waveform font size (see page 215)
   - To change the Fast Zoom In option (see page 215)
   - Lock scrolling with other display windows (see page 216)
   - Change the waveform tool tip display (see page 216)
   - Show/hide parts of the waveform display (see page 211)

3 Click **OK** to apply the changes and close the Waveform Properties dialog.

See Also • Changing Bus/Signal Row Properties (see page 216)

To change the waveform background color

1 In the Waveform Properties dialog's Window Properties tab, select the **Background** color, click the selection button, and select the desired background color from the palette.

   If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Waveform Properties dialog.

To change the overlaid waveform color

When buses/signals are overlaid (see To overlay waveforms (see page 207)), the overlay property specifies the color used for the overlaid waveforms.

1 In the Waveform Properties dialog's Window Properties tab, select the **Overlay** color, click the selection button, and select the desired overlaid waveform color from the palette.

   If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Waveform Properties dialog.

To change the filtered data color

When a filter tool is used to hide data from the Waveform display window, cross-hatching appears at locations where data is hidden; the filter property specifies the color used for the cross-hatched areas.

1 In the Waveform Properties dialog's Window Properties tab, select the **Filter** color, click the selection button, and select the desired filter color from the palette.

   If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Waveform Properties dialog.

To change the timing zoom background color

You can give waveforms from the timing zoom feature a different background color than other waveforms.

1 In the Waveform Properties dialog's Window Properties tab, select the **TimingZoom** color, click the selection button, and select the desired timing zoom background color from the palette.

  If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Waveform Properties dialog.

To change the waveform font size

The font size property adjusts the data display, bus/signal, and simple trigger text size.

1 In the Waveform Properties dialog's Window Properties tab, enter the desired **Font Size**.

  Fonts can range from size 6 through 72 points.

2 Click **OK** to apply the changes and close the Waveform Properties dialog.

As the font size is changed, the row height may be automatically increased to fit the new text size.

To change the Fast Zoom In option

When the Fast Zoom In option is selected, you can drag the mouse cursor over the area you want to zoom in on, and when you release the mouse button, the zoom happens immediately, without having to select **Zoom In** from a popup menu.

1 In the Waveform Properties dialog's Window Properties tab, select or deselect the **Fast Zoom In** option.

2 Click **OK** to apply the changes and close the Waveform Properties dialog.

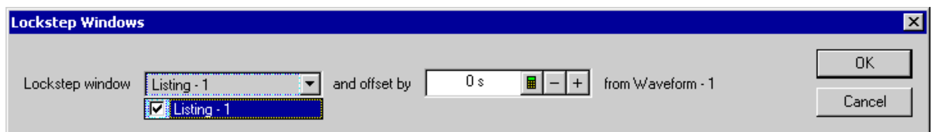
See Also

- To change the display scale (time/division) (see page 204)
- To set a Quick Trigger in the Waveform window (see page 129)
- To quickly find bus signal patterns (see page 257)

To lock scrolling with other display windows

You can lock display windows (for example, Waveform, Listing, Compare, etc.) so that when one window is scrolled, others are scrolled as well, such that the same time is centered in each display.

1 In the Waveform Properties dialog's Window Properties tab, click **Lockstep Windows...**.
2 In the Lockstep Windows dialog, select the display windows whose scrolling should be locked with this window and specify any offset from this window.



3 Click **OK** to close the Lockstep Windows dialog.
4 Click **OK** to apply the changes and close the Waveform Properties dialog.

To change the waveform tool tip display

A *tool tip* (that is, a small box with text) can appear when the mouse pointer is over a waveform and held motionless for a second.

1 In the Waveform Properties dialog's Window Properties tab's Tool Tip area, check or uncheck **Show Values** to specify whether bus/signal values are shown as tool tips.

   If **Show Values** is checked, check or uncheck **Transition Width** to specify whether transition (or pulse) width values are included in the tool tips.
2 Click **OK** to apply the changes and close the Waveform Properties dialog.

Changing Bus/Signal Row Properties

In the Waveform display window, you can change the color or size of a waveform, and you can choose whether numeric values are displayed with the waveform.

NOTE

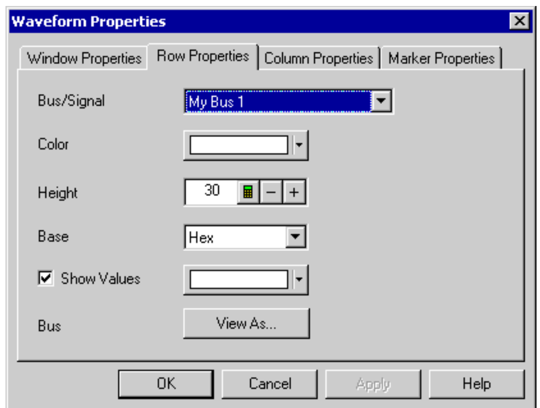
Property changes to a bus affect all signals within the bus. For example, if you change the color of a bus and then expand the bus, you will see that the color is changed for all signals in the bus.

To change the properties of a waveform in the Waveform window:

1 Right-click on a bus/signal name or on a waveform, and choose **Properties...**.

   Or, highlight the buses/signals whose properties you want to change (by clicking, Shift-clicking, or Ctrl-clicking the bus/signal names), and choose **Edit>Window Properties...** from the main menu.

2 In the Waveform Properties dialog's Row Properties tab:



   You can:

   - Select the **Bus/Signal** to which the property changes apply. You can select:
     - Any bus/signal name that has been assigned (see Defining Buses and Signals (see page 82)
     -).
     - **<all>** buses/signals.
     - **<selected>** buses/signals if more than one is highlighted in the Bus/Signal column.
   - Change a waveform's color (see page 218)
   - Change a waveform's height (see page 218)
   - Change a bus/signal's number base (see page 218)
   - Show/hide a bus/signal's numeric data values (see page 219)
   - View bus data as a chart or a bus (see page 209)

3 Click **OK** to apply the changes and close the Waveform Properties dialog.

See Also

- Changing Waveform Window Properties (see page 213)

To change a waveform's color

1 In the Waveform Properties dialog's Row Properties tab, click the **Color** selection button and select the desired waveform color from the palette.

  If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Waveform Properties dialog.

See Also

- Changing Analog Signal Row Properties (see page 219)

To change a waveform's height

1 In the Bus/Signal column of the Waveform display window, position the mouse pointer over a row separator line; when the cursor changes to a resizing cursor, drag the row border.

Or:

1 In the Waveform Properties dialog's Row Properties tab, enter the **Height** value in pixels.

  The minimum row height is set by the font size (see To change the waveform font size (see page 215)). The maximum height is 1000 pixels.

2 Click **OK** to apply the changes and close the Waveform Properties dialog.

See Also

- Changing Analog Signal Row Properties (see page 219)

To change a bus/signal's number base

When a bus/signal's numeric data values are displayed (see To show/hide a bus/signal's numeric data values (see page 219)), the base property specifies the number base to use.

1 In the Waveform Properties dialog's Row Properties tab, select the desired number **Base** from:

  - **Binary**
  - **Hex**
  - **Octal**
  - **Decimal**
  - **Signed Decimal**
  - **Ascii**
  - **Symbol** (see Displaying Names (Symbols) for Bus/Signal Values (see page 232))

2 Click **OK** to apply the changes and close the Waveform Properties dialog.

To show/hide a bus/signal's numeric data values

You can display (and specify the color of) numeric data values with a waveform.

NOTE If the waveform time scale is small, "..." may appear in the data value to indicate that more text will be displayed if you expand the scale.

1 In the Waveform Properties dialog's Row Properties tab, check or uncheck **Show Values** to show or hide numeric data values with the waveform.

   If **Show Values** is checked, click the color selection button and select the desired data value color from the palette.

   If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Waveform Properties dialog.

See Also

- Changing Analog Signal Row Properties (see page 219)

Changing Analog Signal Row Properties

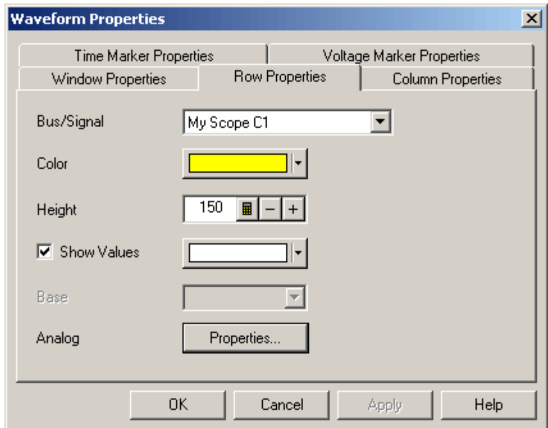
In the Waveform display window, you can change the color or size of an analog signal waveform, and you can choose whether voltage and volts/division values are displayed with the waveform. Analog signals come from an external oscilloscope module (see " External Oscilloscope Time Correlation and Data Display" (in the online help)).

To change the properties of an analog signal waveform in the Waveform window:

1 Right-click on an analog signal name or on a waveform, and choose **Properties...**.

   Or, highlight the analog signals whose properties you want to change (by clicking, Shift-clicking, or Ctrl-clicking the analog signal names), and choose **Edit>Window Properties...** from the main menu.

2 In the Waveform Properties dialog's Row Properties tab:



You can:

- Select the **Bus/Signal** to which the property changes apply. You can select:
  - Any bus/signal name that has been assigned (see Defining Buses and Signals (see page 82)).
  - **<all>** buses/signals.
  - **<selected>** buses/signals if more than one is highlighted in the Bus/Signal column.
- Change a waveform's color (see page 218)
- Change a waveform's height (see page 218)
- Show/hide a signal's numeric data values (see page 219)
- Change the analog properties (see page 220)

3 Click **OK** to apply the changes and close the Waveform Properties dialog.

See Also

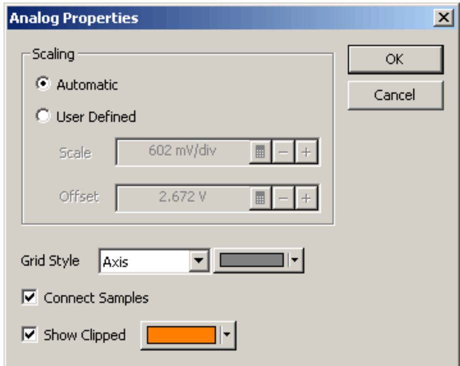
- Changing Waveform Window Properties (see page 213)

To change the analog properties

You can change the properties of an analog signal in the Waveform display window.

1 In the Waveform Properties dialog's Row Properties tab, for the **Analog** property, click **Properties...**.

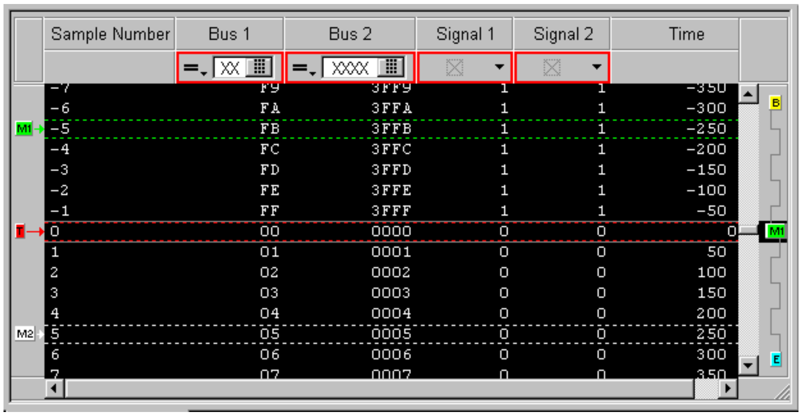
2 In the Analog Properties dialog, set the following options:



- **Scaling** — you can select **Automatic** (to have the voltage scale and offset automatically set) or **User Defined** (to be able to set your own voltage scale and offset values). Be careful not to enter scale and offset values that will move the waveform out of the display area.
- **Grid Style/Color** — you can select **None**, **Axis** (to have axis lines drawn through the center of the waveform display area), or **Grid** (to have grid lines drawn for voltage and time divisions). If you choose axis or grid, you can specify its color.
- **Connect Samples** — specifies whether lines are drawn between waveform data sample points.
- **Show Clipped** — enables out-of-range data values to be displayed in a user-defined color.

Analyzing Listing Data

The Listing window displays your captured data as a state listing. You configure the window to display selected buses and signals in columns. Within the listed data, you can insert time or pattern markers. You can also configure the bus pattern triggers and signal trigger options.



The Listing window is accessed through the menu bar's **Window>Listing**. If you have Tabbed Windows (see page 305) turned on, you can also select a tab at the bottom of the window.

- To go to different locations in the captured data (see page 223)
- To re-arrange bus/signal columns (see page 224)
- To find a bus/signal column (see page 224)
- To show/hide parts of the listing display (see page 225)
- To insert or delete buses/signals (see page 225)
- Changing Listing Window Properties (see page 226)
  - To change the listing background color (see page 226)
  - To change the timing zoom background color (see page 227)
  - To change the listing font size (see page 227)
  - To lock scrolling with other display windows (see page 227)
  - To show/hide the center rectangle (see page 228)
- Changing Bus/Signal Column Properties (see page 228)
  - To change a bus/signal's data color (see page 229)
  - To change the width of a bus/signal column (see page 229)
  - To change the alignment of a bus/signal column (see page 230)
  - To change a bus/signal's number base (see page 230)
  - To select the marker for marker-relative times (see page 231)

- To select fixed time units (see page 231)

See Also

- Defining Buses and Signals (see page 82)
- Setting Up Quick (Draw Box) Triggers (see page 129)
- Specifying Simple Triggers (see page 133)
- Marking, and Measuring Between, Data Points (see page 234)
- Setting Up Symbols (see page 116)
- Displaying Names (Symbols) for Bus/Signal Values (see page 232)
- Searching the Captured Data (see page 257)

To go to different locations in the captured data

In the Listing display window, you can go to different locations in the captured data by using the vertical scroll bars, by using the Go To buttons on the standard toolbar, or by choosing Go To commands from popup menus.

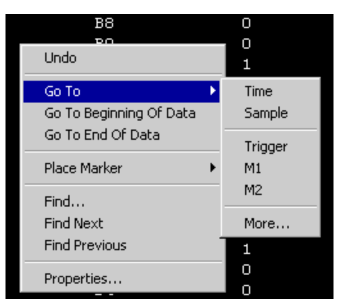
To go to different locations using toolbar buttons

1 Click one of the Go To buttons in the standard toolbar.

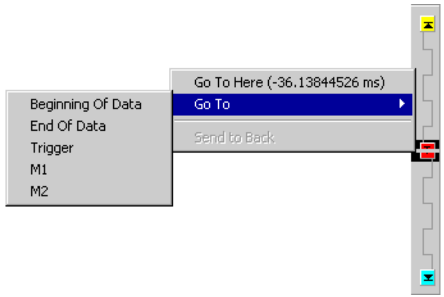
	Go to Beginning — centers the beginning of the acquisition data.
	Go to Trigger — centers the trigger point of the acquisition.
	Go to End — centers the end of the acquisition data.

To go to different locations using popup menus

1 Right-click in the waveform display area, and choose one of the **Go To** commands.



Or, click in the marker overview bar, and choose one of the **Go To** commands.



You can choose **Beginning Of Data**, **End Of Data**, **Trigger**, a marker, a **Time**, or a **Sample**.

To re-arrange bus/signal columns

1 Position the mouse pointer over the bus/signal name associated with the column you want to move.

2 Click and hold the mouse button.

3 Drag-and-drop the bus/signal to its new position.

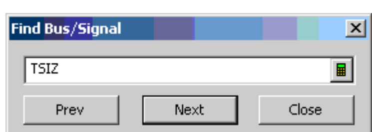
The name is placed to the left of the red position indicator that appears.

To find a bus/signal column

When there are many bus/signal columns in the Listing display window, you can search for a particular bus/signal column instead of scrolling through all the columns.

1 In the Listing display window, right-click in any Bus/Signal column heading, and choose **Find Bus/Signal...**.

2 In the Find Bus/Signal dialog, enter the name (or part of the name) of the bus/signal you wish to find.

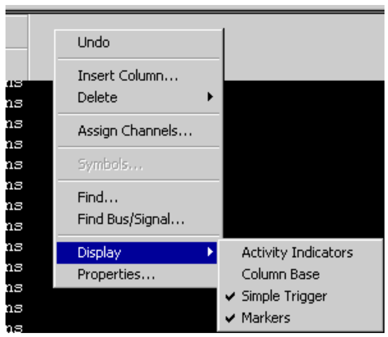


3 Then, click:

- **Prev** — to search for the string backward in the bus/signal columns.
- **Next** — to search for the string forward in the bus/signal columns.
- **Close** — to close the Find Bus/Signal dialog.

To show/hide parts of the listing display

1 Right-click in the Bus/Signal column heading of the Listing display, and choose **Display>**.



Then, check or uncheck one of the following to show or hide that part of the Listing display window:

- **Activity Indicators** — either a low bar (low level), high bar (high level), or a transition arrow (transitioning signal) displayed to the left of bus/signal names.
- **Column Base** — the number base row in the column headings.
- **Simple Trigger** — the Simple Trigger row in the column headings (see Specifying Simple Triggers (see page 133)).
- **Markers** — the markers display bar (see page 431).

You can also make these selections in the **Display Options** area of the Listing Properties dialog's Window Properties tab.

See Also

- Changing Listing Window Properties (see page 226)

To insert or delete buses/signals

To insert buses/signals

1 In the Listing display window, right-click in the Bus/Signal column headings; then, choose **Insert Column**.

2 In the Insert dialog, select the buses/signals you want to insert; then, click **OK**.

To delete selected buses/signals

1 Highlight the headings of the bus/signal columns you want to delete (by clicking, Shift-clicking, or Ctrl-clicking the bus/signal names).

2 Right-click in an empty area of the column headings row; then, choose **Delete>Column**.

To delete all buses/signals

1 Right-click anywhere in the column headings row; then, choose **Delete>All Columns**.

See Also

- Defining Buses and Signals (see page 82)

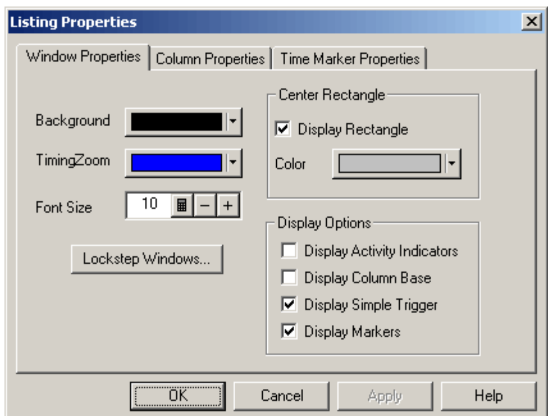
Changing Listing Window Properties

You can change properties that affect the entire Listing display window.

1 Right-click in a blank area of the listing display, and choose **Properties...**.

Or, with no bus/signal names selected, choose **Edit>Window Properties...** from the main menu.

2 In the Listing Properties dialog's Window Properties tab:



You can:

- Change the listing background color (see page 226)
- Change the timing zoom background color (see page 227)
- Change the listing font size (see page 227)
- Lock scrolling with other display windows (see page 227)
- Show/hide the center rectangle (see page 228)
- Show/hide parts of the listing display (see page 225)

3 Click **OK** to apply the changes and close the Listing Properties dialog.

See Also

- Changing Bus/Signal Column Properties (see page 228)

To change the listing background color

1 In the Listing Properties dialog's Window Properties tab, click the **Background** color selection button and select the desired background color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Listing Properties dialog.

To change the timing zoom background color

In the Listing display window, you can give columns from the timing zoom feature a different background color than other bus/signal data columns.

1 In the Listing Properties dialog's Window Properties tab, click the **TimingZoom** color selection button and select the desired timing zoom background color from the palette.

   If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Listing Properties dialog.

To change the listing font size

The font size property adjusts the data display, bus/signal, and simple trigger text size.

1 In the Listing Properties dialog's Window Properties tab, enter the desired **Font Size**.

   Fonts can range from size 6 through 72 points.

2 Click **OK** to apply the changes and close the Listing Properties dialog.

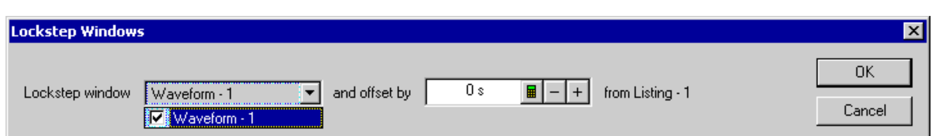
As the font size is changed, the column width may be automatically increased to fit the new text size.

To lock scrolling with other display windows

You can lock display windows (for example, Waveform, Listing, Compare, etc.) so that when one window is scrolled, others are scrolled as well, such that the same time is centered in each display.

1 In the Listing Properties dialog's Window Properties tab, click **Lockstep Windows...**.

2 In the Lockstep Windows dialog, select the display windows whose scrolling should be locked with this window and specify any offset from this window.



3 Click **OK** to close the Lockstep Windows dialog.

4 Click **OK** to apply the changes and close the Listing Properties dialog.

To show/hide the center rectangle

The center rectangle is the box that is drawn around the one sample displayed at center of the screen.

1 In the Listing Properties dialog's Window Properties tab's Center Rectangle area, check or uncheck **Display Rectangle** to specify whether the center rectangle is shown or hidden.

   If **Display Rectangle** is checked, click the color selection button and select the desired center rectangle color from the palette.

   If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Listing Properties dialog.

Changing Bus/Signal Column Properties

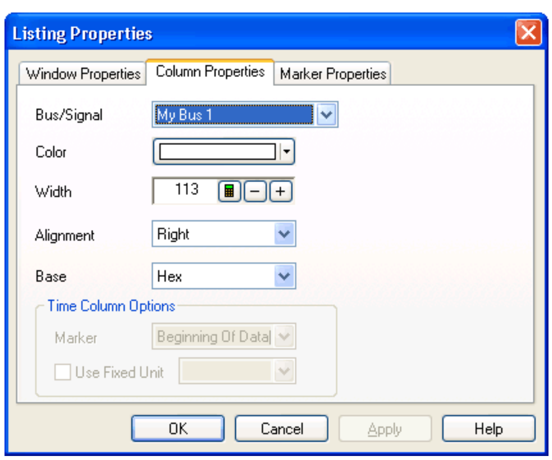
In the Listing display window, you can change the color, width, alignment, or number base of bus/signal data columns.

To change the properties of a bus/signal data column in the Listing window:

1 Right-click on a bus/signal name or on a waveform, and choose **Properties...**.

   Or, highlight the buses/signals whose properties you want to change (by clicking, Shift-clicking, or Ctrl-clicking the bus/signal names), and choose **Edit>Window Properties...** from the main menu.

2 In the Listing Properties dialog's Column Properties tab:



   You can:

   - Select the **Bus/Signal** to which the property changes apply. You can select:

    - Any bus/signal name that has been assigned (see Defining Buses and Signals (see page 82)).
    - **<all>** buses/signals.
    - **<selected>** buses/signals if more than one column is highlighted.
  - Change a bus/signal's data color (see page 229)
  - Change the width of a bus/signal column (see page 229)
  - Change the alignment of a bus/signal column (see page 230)
  - Change a bus/signal's number base (see page 230)
  - Select the marker for marker-relative times (see page 231)
  - Select fixed time units (see page 231)

3 Click **OK** to apply the changes and close the Listing Properties dialog.

See Also

- Changing Listing Window Properties (see page 226)

To change a bus/signal's data color

1 In the Listing Properties dialog's Column Properties tab, click the **Color** selection button and select the desired bus/signal data color from the palette.

  If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Listing Properties dialog.

To change the width of a bus/signal column

TIP You can autosize individual columns by placing the mouse pointer over the right border of the column header box; then, when the pointer icon changes to a resizing pointer, double-click.

TIP If your keyboard has a numeric keypad, you can autosize all columns by selecting any column header box (to highlight it) and by pressing **Ctrl** and "+" on the numeric keypad.

1 In the bus/signal headings row of the listing display window, position the mouse pointer over a column separator line; when the cursor changes to a resizing cursor, drag the column border.

Or:

1 In the Listing Properties dialog's Column Properties tab, enter the **Width** value in pixels.

  The minimum column width is 1 pixel, while the maximum width is 1000 pixels.

2 Click **OK** to apply the changes and close the Listing Properties dialog.

To change the alignment of a bus/signal column

The Alignment property sets the display of data to be left-justified, right-justified, or centered within the column.

1 In the Listing Properties dialog's Column Properties tab, select the **Alignment** from:

- **Left**
- **Center**
- **Right**

2 Click **OK** to apply the changes and close the Listing Properties dialog.

To change a bus/signal's number base

The base property specifies the number base to use when displaying the captured data.

1 In the Listing Properties dialog's Column Properties tab, select the desired number **Base** from:

- **Binary**
- **Hex**
- **Octal**
- **Decimal**
- **Signed Decimal**
- **Ascii**
- **Symbol** (see Displaying Names (Symbols) for Bus/Signal Values (see page 232))

NOTE

If the **Time** column has been selected instead of a data column, your choices change from a numeric format to **Absolute**, **Relative Previous**, or **Relative Marker**.

NOTE

If an analog signal from an external oscilloscope module (see " External Oscilloscope Time Correlation and Data Display" (in the online help)) column has been selected instead of a data column, **Voltage** is the only choice for number base.

2 Click **OK** to apply the changes and close the Listing Properties dialog.

To select the marker for marker-relative times

In the Listing window, you can display times relative to a marker.

1 In the Listing Properties dialog's Column Properties tab, use the **Bus/Signal** selection to select the **Time** column.
2 For the **Base** property, select **Relative Marker**.
3 For the **Marker** property, select the marker to which relative times should be displayed.
4 Click **OK** to apply the changes and close the Listing Properties dialog.

To select fixed time units

In the Listing window, you can display time column values with a fixed unit.

1 In the Listing Properties dialog's Column Properties tab, use the **Bus/Signal** selection to select the **Time** column.
2 In the Time Column Properties box, check **Use Fixed Unit**; then, select the desired time unit from the drop-down list.
3 Click **OK** to apply the changes and close the Listing Properties dialog.

Displaying Names (Symbols) for Bus/Signal Values

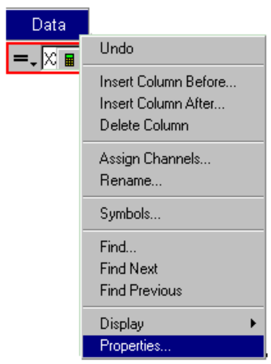
You can display a bus or signal using meaningful names rather than numeric values.

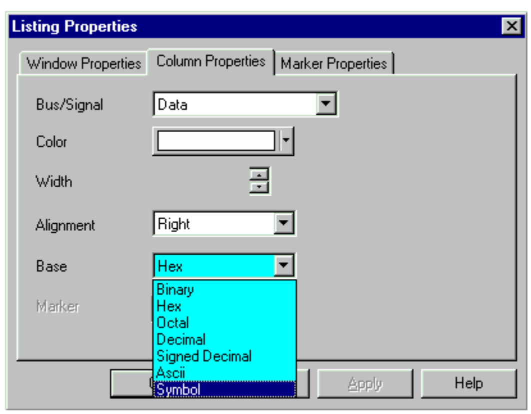
Symbols can be displayed in Waveform, Listing, Compare, and Source windows.

To display symbols:

1 Set up the symbols (see page 116).

2 Change the number base (see page 230) of the bus or signal to Symbols.





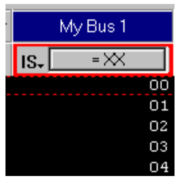
If the symbol is defined as a range, values in the range will be displayed with an offset from the lowest end of the range.

If the definitions of several symbols overlap, the first one listed in the Symbols dialog has precedence over the others.

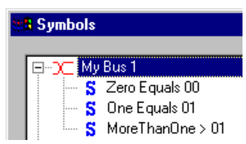
In the Waveform display, "..." will be shown when the full name of the symbol will not fit into the space available.

Once you have set up symbols, it's usually a good idea to save (see page 171) the logic analyzer configuration. The symbol definitions will be stored as part of the configuration.

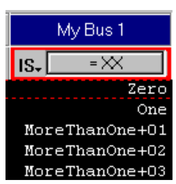
Example Here is what "My Bus 1" looks like before defining any symbols:



When the symbols have been defined, they are shown in the Symbols dialog:



Here is what the bus looks like after the symbols are defined:



Marking, and Measuring Between, Data Points

Once a marker is created, you can use it as a reference point in the data when measuring intervals or viewing the data value at the marker.

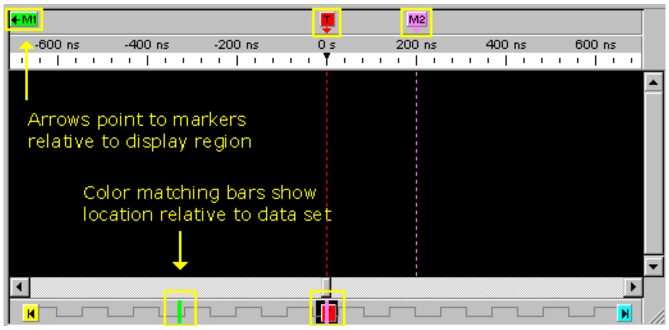
- To read the markers display and overview bars (see page 235)
- To create new markers (see page 235)
- To place markers in data (see page 237)
- To go to a marker (see page 239)
- To center the display about a marker pair (see page 240)
- To change a marker's snap to edge setting (see page 240)
- To delete a marker (see page 241)
- To create a new time interval measurement (see page 242)
- To create a new sample interval measurement (see page 243)
- To create a new value at measurement (see page 245)
- To rename a marker (see page 245)
- To send a marker to the back (see page 246)
- Changing Marker Properties (see page 247)
  - To change a marker's background color (see page 248)
  - To change a marker's foreground color (see page 248)
  - To hide/show a marker (see page 248)
  - To change a marker's lock in viewer setting (see page 248)
  - To lock a marker relative to another marker (see page 249)
  - To add comments to a marker (see page 249)
- Using Voltage Markers for Analog Signals (in the Waveform Display) (see page 249)
  - To create new voltage markers (see page 250)
  - To place voltage markers (see page 251)
  - To delete voltage markers (see page 252)
  - To create a new voltage interval measurement (see page 253)
  - To rename a voltage marker (see page 254)
  - To send a voltage marker to the back (see page 254)
  - To change voltage marker properties (see page 255)

See Also

- Markers Display Bar (see page 431)
- Marker Measurement Display Bar (see page 426)
- Markers Menu (see page 412)

- Markers Toolbar (see page 423)

To read the markers display and overview bars



In the upper markers display bar (see page 431), markers are color coded and displayed with arrows that point to the marker's location relative to the displayed data.

In the lower markers overview bar (see page 432), markers are displayed as color coded bars that show the location relative to the complete captured data set.

In the Waveform window (as shown above), the markers display and overview bars appear on the top and bottom of the window. In the Listing window, the markers display and overview bars appear on the left and right sides of the window in a similar way.

TIP You can quickly display a different region of data by clicking on the markers overview bar at the bottom (waveform) or right side (listing) and selecting **Go To Here** from the popup menu.

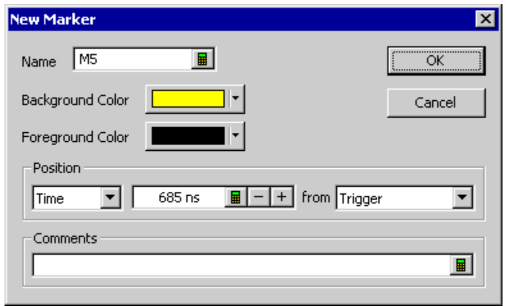
To create new markers

When creating a new marker, you can give it a name, specify its color, position it in the data, and add comments. Up to 1024 markers can be created.

1 From the menu bar, select **Markers>New...**.

2 In the New Marker dialog, enter the marker name.

   You can specify both a *long name* and an *abbreviated name* by using the "Long name[abbreviated name]" syntax; for example, "Location A[A]". When an abbreviated name is used, it appears on the marker in the marker display bar (see page 431) while the long name appears in the marker *tool tip* (see page 655).



3 Select the marker's background and foreground colors.

4 Specify the position of the new marker in the data by:

- **Time** - positions the marker by a time value from a reference point. Reference points are the Trigger, Beginning of Data, End of Data, or another marker.
- **Sample** - positions the marker by a number of samples from a reference point. Reference points are the Trigger, Beginning of Data, End of Data, or another marker.
- **Value** - positions the marker at an occurrence of a bus/signal pattern. Click **Occurs...** to specify the bus/signal pattern value.

  Bus/signal pattern specification is the same as when searching the captured data (see page 257).

5 Enter comments for the marker.

Comments appear in the marker's *tool tip* (see page 655).

6 Click **OK**.

See Also

- To place markers in data (see page 237)
- To go to a marker (see page 239)
- To read the markers display and overview bars (see page 235)
- To center the display about a marker pair (see page 240)
- To delete a marker (see page 241)
- To rename a marker (see page 245)
- To send a marker to the back (see page 246)
- To change a marker's snap to edge setting (see page 240)
- Changing Marker Properties (see page 247)

To place markers in data

Use Place Markers to quickly position a marker in the data. Depending on how you access the Place Markers feature, the marker is placed in the data a little differently. You can also move markers by dragging them with the mouse or by using the front-panel knobs.

NOTE An enabled **Snap to Edge** property affects a marker's placement in the Waveform window if the mouse cursor is over a waveform when dragging and dropping or when placing at the mouse cursor.

- To drag and drop markers in data (see page 237)
- To place marker at the mouse cursor (see page 237)
- To place marker at center screen (see page 237)
- To change a marker's position property (see page 238)
- You can also place markers where data is found when searching (see To specify "found" marker placement (see page 267)).

To drag and drop markers in data

Using the drag and drop feature you can move markers to new positions in the data.

1 Click and hold down the mouse button on the marker you wish to move.

2 Move the mouse cursor to the new position.

   When moving a marker in the Waveform display window, if the mouse cursor is over a waveform and the marker's **Snap to Edge** property is enabled, the cursor changes to a green "direction arrow" indicating the direction of the next valid edge. A yellow "cross hair" target is placed on the edge at which the marker will be placed if you decide to release the mouse button. If you don't want the marker to snap to an edge, move the mouse cursor so that it is not over any waveforms before releasing the mouse button.

3 Release the mouse button to reposition the marker.

To place marker at the mouse cursor

1 Point the mouse to the desired data point in the display.

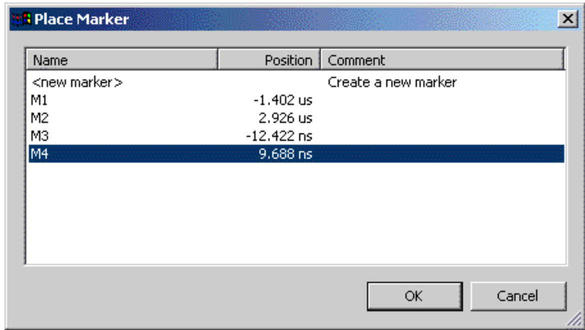
2 Right-click, and select **Place Marker>Time>(desired marker)**.

   If the mouse cursor is over a waveform and the marker's **Snap to Edge** property is enabled, the marker is placed at nearest waveform edge; otherwise, the marker is placed at the mouse cursor location.

To place marker at center screen

1 From the menu bar click **Markers>Place On Screen...**.

2 In the Place Marker dialog, select the desired marker.



You can sort the list of markers by clicking on the Name, Position, or Comment column headings.

3 Click **OK**.

The marker will be placed at mid-screen.

To change a marker's position property

1 Right-click on a marker, and choose **Properties...**.

Or, when viewing a display window that has markers, choose **Markers>Properties...** from the main menu.

2 In the display window properties dialog's Time Marker Properties tab, select the **Marker** to which the property changes apply.

3 In the **Position** box, select what to position the marker by:

- **Time** - positions the marker by a time value from a reference point. Reference points are the Trigger, Beginning of Data, End of Data, or another marker.
- **Sample** - positions the marker by a number of samples from a reference point. Reference points are the Trigger, Beginning of Data, End of Data, or another marker.
- **Value** - positions the marker at an occurrence of a bus/signal pattern. Click **Occurs...** to specify the bus/signal pattern value.

  Bus/signal pattern specification is the same as when searching the captured data (see page 257), except you can click **Properties...** to open the Value Properties dialog. In the Value Properties dialog:

  - Check **Stop repetitive run** if you want to stop a repetitive run when the specified bus/signal pattern is found (or not found).
  - Check **Send e-mail** if you want to send an e-mail when the specified bus/signal pattern is found (or not found); then, click the **E-mail...** button. In the E-mail dialog (see page 453), enter the address to which e-mail will be sent, the subject, and the text of the message.

4 Click **OK** to apply the changes and close the properties dialog.

See Also

- To specify "found" marker placement (see page 267) (for placing markers where data is found)
- To create new markers (see page 235)
- To go to a marker (see page 239)
- To read the markers display and overview bars (see page 235)
- To center the display about a marker pair (see page 240)
- To delete a marker (see page 241)
- To rename a marker (see page 245)
- To send a marker to the back (see page 246)
- To change a marker's snap to edge setting (see page 240)
- Changing Marker Properties (see page 247)

To go to a marker

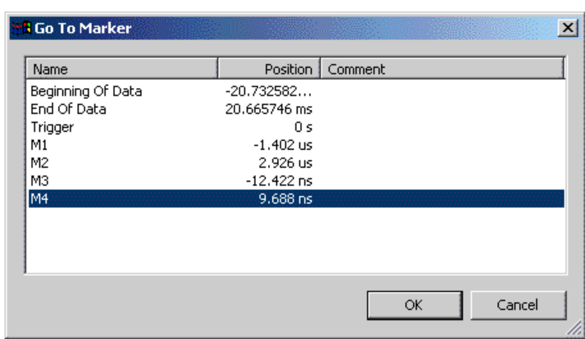
To quickly find a previously set marker in the data, or to go to the beginning of data, end of data, or the trigger point:

- Click in the markers display bar (see page 431) or the markers overview bar (see page 432), and choose **Go To** from the popup menu.

Or:

1 From the menu bar, select **Markers>Go To...** or select the icon in the markers toolbar (see page 423).

2 In the Go To Marker dialog, select the marker you wish to find from the list provided.



You can sort the list of markers by clicking on the Name, Position, or Comment column headings.

3 Click **OK**.

The selected marker appears at the center of the display.

See Also

- To create new markers (see page 235)

- To place markers in data (see page 237)
- To center the display about a marker pair (see page 240)
- To delete a marker (see page 241)
- To rename a marker (see page 245)
- To send a marker to the back (see page 246)
- To change a marker's snap to edge setting (see page 240)
- Changing Marker Properties (see page 247)

To center the display about a marker pair

Use the center about feature to center the display around a selected marker pair. If the marker pair is separated by a large time or sample amount, the scale of the display is automatically changed so both markers appear on screen.

Since the center about feature centers the display around a pair (two) markers, if you have three or more markers defined, you will have available choices for all possible combinations of two.

1. From the menu bar, select **Markers>Center About...**.
2. In the Center About dialog, select the desired marker combination.
3. Click **OK**.

   The data between the two markers is displayed.

See Also

- To create new markers (see page 235)
- To place markers in data (see page 237)
- To go to a marker (see page 239)
- To delete a marker (see page 241)
- To rename a marker (see page 245)
- To send a marker to the back (see page 246)
- To change a marker's snap to edge setting (see page 240)
- Changing Marker Properties (see page 247)

To change a marker's snap to edge setting

1. In a display window with markers, right-click on the marker, and choose **Snap to Edge**.

   Or, in the display window properties dialog's Time Marker Properties tab, check or uncheck **Snap to Edge** to enable or disable the marker's snap to edge behavior.

See Also

- To place markers in data (see page 237)

- Changing Marker Properties (see page 247)

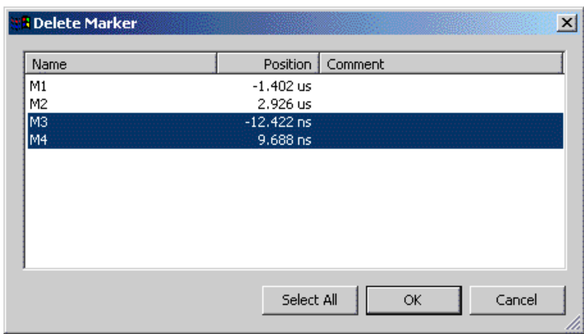
To delete a marker

- In the markers display bar (see page 431), click the marker you want to delete, and choose **Delete** from the popup menu (or choose **Delete All** to delete all markers).

Or:

1 From the menu bar, select **Markers>Delete...**.

2 In the Delete Marker dialog, select the markers you wish to delete.



You can sort the list of markers by clicking on the Name, Position, or Comment column headings.

3 Click **OK**.

See Also

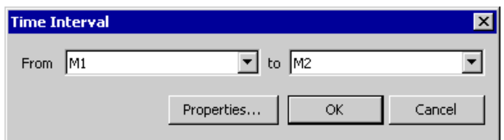
- To create new markers (see page 235)
- To place markers in data (see page 237)
- To go to a marker (see page 239)
- To center the display about a marker pair (see page 240)
- To rename a marker (see page 245)
- To send a marker to the back (see page 246)
- To change a marker's snap to edge setting (see page 240)
- Changing Marker Properties (see page 247)

To create a new time interval measurement

Use the new time interval measurement feature to measure a time interval between two specified points in the captured data. Measurement results are displayed in the marker measurement display bar (see page 426).

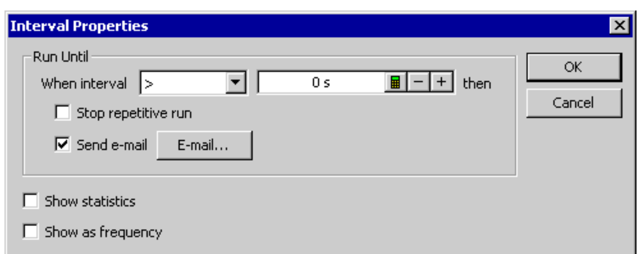
1 From the menu bar select **Markers>New Time Interval Measurement**, or click the icon in the markers toolbar (see page 423).

2 In the Time Interval dialog, select the markers you want to measure time between.



NOTE If you have selected a "System Trigger - (module)" or "Trigger - (module)" marker, make sure you uncheck the **First module to trigger designates the System Trigger** option in the Module Skew and System Trigger dialog (see page 468). Otherwise, during a run, the system trigger could switch from one module to another, causing the module markers to be re-assigned and any measurements using these markers to be deleted.

3 To specify interval properties, click **Properties...**.



In the Interval Properties dialog:

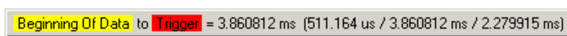
- Check **Stop repetitive run** if you want to stop a repetitive run when the specified interval value is measured.
- Check **Send e-mail** if you want to send an e-mail when the specified interval value is measured; then, click the **E-mail...** button. In the E-mail dialog (see page 453), enter the address to which e-mail will be sent, the subject, and the text of the message.
- Check **Show statistics** if you want to show repetitive run statistics.

CAUTION If you have selected a "System Trigger - (module)" or "Trigger - (module)" marker as one of the markers you want to measure time between, make sure you uncheck the **First module to trigger designates the System Trigger** option in the Module Skew and System Trigger dialog (see page 468). Otherwise, during the repetitive run, the system trigger could switch from one module to another, causing you to lose all the statistical data you have accumulated.

- Check **Show as frequency** if you want to show the measured frequency of changes in the interval.
- Click **OK** when you are done specifying interval properties.

4 Click **OK** to close the Time Interval dialog.

The result of the interval measurement is displayed in the marker measurements display bar:



If statistics are shown, the low, high, and average interval measurements are included.

See Also

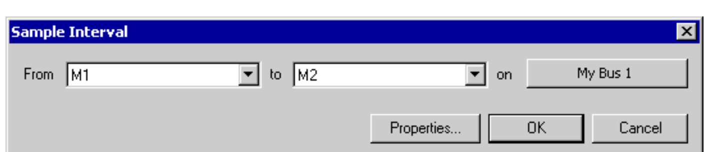
- To create a new sample interval measurement (see page 243)
- To create a new value at measurement (see page 245)

To create a new sample interval measurement

Use the new sample interval measurement feature to measure the number of samples between two specified points in the captured data. Measurement results are displayed in the marker measurement display bar (see page 426).

1 From the menu bar select **Markers>New Sample Interval Measurement**, or click the icon in the markers toolbar (see page 423).

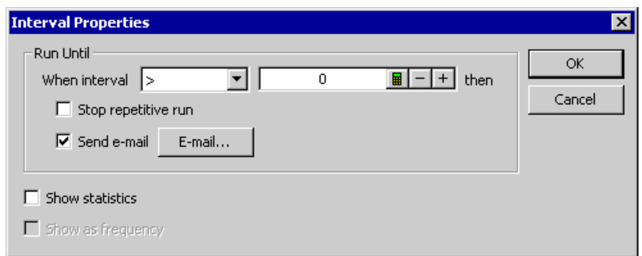
2 In the Sample Interval dialog, select the markers you want to measure samples between, and select the bus/signal.



NOTE

If you have selected a "System Trigger - (module)" or "Trigger - (module)" marker, make sure you uncheck the **First module to trigger designates the System Trigger** option in the Module Skew and System Trigger dialog (see page 468). Otherwise, during a run, the system trigger could switch from one module to another, causing the module markers to be re-assigned and any measurements using these markers to be deleted.

3 To specify interval properties, click **Properties...**.



In the Interval Properties dialog:

- Check **Stop repetitive run** if you want to stop a repetitive run when the specified interval value is measured.
- Check **Send e-mail** if you want to send an e-mail when the specified interval value is measured; then, click the **E-mail...** button. In the E-mail dialog (see page 453), enter the address to which e-mail will be sent, the subject, and the text of the message.
- Check **Show statistics** if you want to show repetitive run statistics.

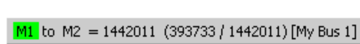
CAUTION

If you have selected a "System Trigger - (module)" or "Trigger - (module)" marker as one of the markers you want to measure samples between, make sure you uncheck the **First module to trigger designates the System Trigger** option in the Module Skew and System Trigger dialog (see page 468). Otherwise, during the repetitive run, the system trigger could switch from one module to another, causing you to lose all the statistical data you have accumulated.

- Click **OK** when you are done specifying interval properties.

4 Click **OK** to close the Sample Interval dialog.

The result of the interval measurement is displayed in the marker measurements display bar:



If statistics are shown, the low and high interval measurements are included.

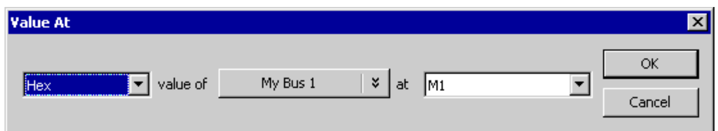
See Also

- To create a new time interval measurement (see page 242)
- To create a new value at measurement (see page 245)

To create a new value at measurement

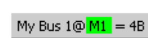
Use the new value at measurement feature to measure the value of a bus/signal at a specified marker location in the captured data. Measurement results are displayed in the marker measurement display bar (see page 426).

1. From the menu bar select **Markers>New Value At Measurement**, or click the icon in the markers toolbar (see page 423).
2. In the Value At dialog, select the numeric base of the data, the bus/signal, and the marker.



NOTE If you have selected a "System Trigger - (module)" or "Trigger - (module)" marker, make sure you uncheck the **First module to trigger designates the System Trigger** option in the Module Skew and System Trigger dialog (see page 468). Otherwise, during a run, the system trigger could switch from one module to another, causing the module markers to be re-assigned and any measurements using these markers to be deleted.

3. Click **OK**.

   The result of the value at measurement  is displayed in the marker measurement display bar.

See Also

- To create a new time interval measurement (see page 242)
- To create a new sample interval measurement (see page 243)

To rename a marker

You can give markers any name you choose.

1. In a display window with markers, right-click on the marker, and choose **Rename...**.

   Or, in the display window properties dialog's Time Marker Properties tab, select the **Marker**, and click **Rename...**.

2. In the Rename dialog, enter the new marker name.

You can specify both a *long name* and an *abbreviated name* by using the "Long name[abbreviated name]" syntax; for example, "Location A[A]". When an abbreviated name is used, it appears on the marker in the marker display bar (see page 431) while the long name appears in the marker *tool tip* (see page 655).

3 Click **OK**.

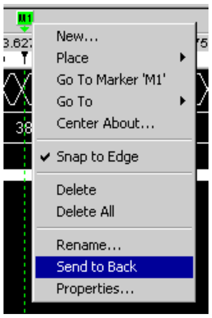
See Also

- To create new markers (see page 235)
- To place markers in data (see page 237)
- To go to a marker (see page 239)
- To center the display about a marker pair (see page 240)
- To delete a marker (see page 241)
- To send a marker to the back (see page 246)
- To change a marker's snap to edge setting (see page 240)
- Changing Marker Properties (see page 247)

To send a marker to the back

When markers overlap on the display, you can send the visible marker to the back in order to see the marker underneath.

1 Click the marker you wish to send to the back, and choose **Send to Back** from the pop-up menu.



See Also

- To create new markers (see page 235)
- To place markers in data (see page 237)
- To go to a marker (see page 239)
- To center the display about a marker pair (see page 240)
- To delete a marker (see page 241)
- To rename a marker (see page 245)
- To change a marker's snap to edge setting (see page 240)
- Changing Marker Properties (see page 247)

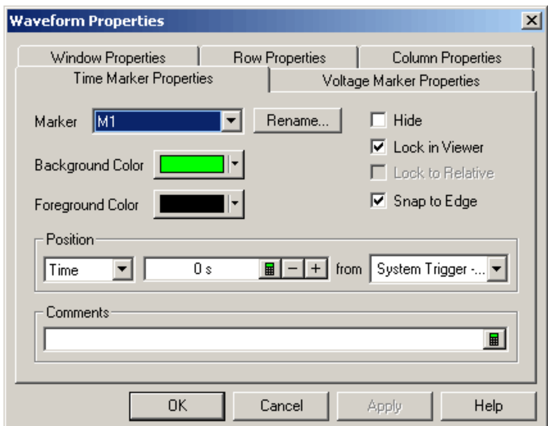
Changing Marker Properties

Once a marker is created, you can modify any of its attributes from the Time Marker Properties tab..

1 Right-click on a marker, and choose **Properties...**.

   Or, when viewing a display window that has markers, choose **Markers>Properties...** from the main menu.

2 In the display window properties dialog's Time Marker Properties tab:



   You can:

   - Select the **Marker** to which the property changes apply.
   - Rename a marker (see page 245)
   - Change a marker's background color (see page 248)
   - Change a marker's foreground color (see page 248)
   - Change a marker's position property (see page 238)
   - Hide/show a marker (see page 248)
   - Change a marker's lock in viewer setting (see page 248)
   - Lock a marker relative to another marker (see page 249)
   - Change a marker's snap to edge setting (see page 240)
   - Add comments to a marker (see page 249)

3 Click **OK** to apply the changes and close the properties dialog.

See Also

- To create new markers (see page 235)
- To place markers in data (see page 237)
- To go to a marker (see page 239)
- To center the display about a marker pair (see page 240)
- To delete a marker (see page 241)

- To rename a marker (see page 245)
- To send a marker to the back (see page 246)
- To read the markers display and overview bars (see page 235)

To change a marker's background color

1. In the Marker Properties tab, click the **Background Color** selection button and select the desired color from the palette.

   If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.
2. Click **OK** to apply the changes and close the properties dialog.

See Also

- To change voltage marker properties (see page 255)

To change a marker's foreground color

1. In the Marker Properties tab, click the **Foreground Color** selection button and select the desired color from the palette.

   If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.
2. Click **OK** to apply the changes and close the properties dialog.

See Also

- To change voltage marker properties (see page 255)

To hide/show a marker

1. In the Marker Properties tab, check or uncheck **Hide** to hide or show the marker.

   When a marker is hidden, all other marker properties are retained; the marker is just hidden from view in the display.
2. Click **OK** to apply the changes and close the properties dialog.

See Also

- To change voltage marker properties (see page 255)

To change a marker's lock in viewer setting

When a marker's **Lock in Viewer** setting is enabled, moving or placing the marker in one display window causes other display windows to be updated so that the marker appears in them as well.

NOTE

The lock in viewer behavior applies only when a marker is dragged within the immediate data viewing area. If a marker is moved by defining a new position in the Time Markers Properties tab, the marker is not guaranteed to be visible in other display windows.

1 In the Time Marker Properties tab, check or uncheck **Lock in Viewer** to enable or disable the setting.

2 Click **OK** to apply the changes and close the properties dialog.

To lock a marker relative to another marker

When a marker is positioned relative to another marker and the marker's **Lock to Relative** setting is enabled, moving or placing either marker causes both to move such that the time between the markers remains the same. Both markers must be movable.

1 In the Marker Properties tab's **Position** box:

   a Select **Time**.

   b Select the relative marker.

   c Enter the relative time between markers.

2 Check or uncheck **Lock to Relative** to lock or unlock relative marker movements.

3 Click **OK** to apply the changes and close the properties dialog.

To add comments to a marker

You can add comments to a marker that appear in the marker's *tool tip* (see page 655).

1 In the Marker Properties tab's **Comments** box, enter your comments.

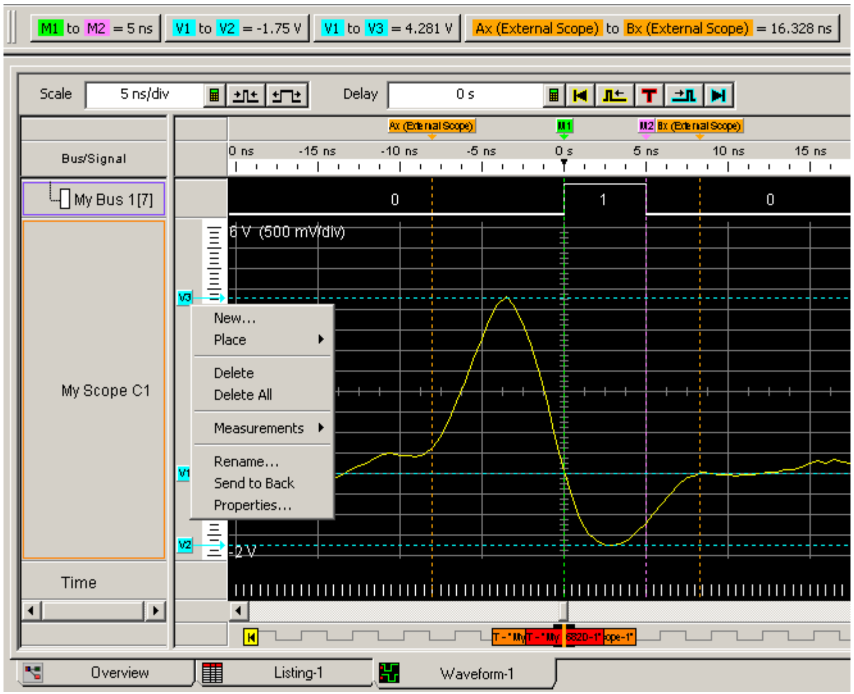
2 Click **OK** to apply the changes and close the properties dialog.

See Also

- To change voltage marker properties (see page 255)

Using Voltage Markers for Analog Signals (in the Waveform Display)

When analog signals are added to the Waveform display window (from an external oscilloscope module), you can add voltage markers and voltage interval measurements.



- To create new voltage markers (see page 250)
- To place voltage markers (see page 251)
- To delete voltage markers (see page 252)
- To create a new voltage interval measurement (see page 253)
- To rename a voltage marker (see page 254)
- To send a voltage marker to the back (see page 254)
- To change voltage marker properties (see page 255)

See Also

- " External Oscilloscope Time Correlation and Data Display" (in the online help)

To create new voltage markers

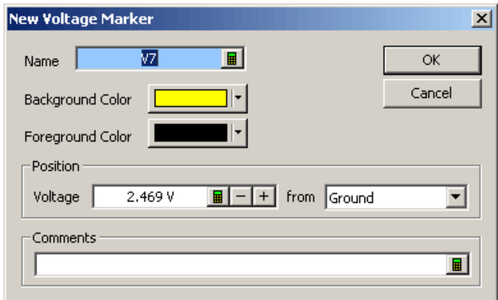
When creating a new voltage marker, you can give it a name, specify its color, position it, and add comments.

1. In an analog signal row's voltage marker/vertical scale display bar (to the left of the waveform), click (where you would like to place the marker) and choose **New...**.

   Or, right-click on an analog signal waveform (where you would like to place the marker) and choose **Place Marker>Voltage>New Marker...**.

2. In the New Voltage Marker dialog, enter the marker name.

You can specify both a *long name* and an *abbreviated name* by using the "Long name[abbreviated name]" syntax; for example, "Location A[A]". When an abbreviated name is used, it appears on the marker in the voltage marker display bar while the long name appears in the marker *tool tip* (see page 655).



3 Select the marker's background and foreground colors.

4 Specify the position of the new voltage marker by its voltage from ground or another voltage marker.

5 Enter comments for the voltage marker.

Comments appear in the marker's *tool tip* (see page 655).

6 Click **OK**.

See Also

- To place voltage markers (see page 251)
- To delete voltage markers (see page 252)
- To create a new voltage interval measurement (see page 253)
- To rename a voltage marker (see page 254)
- To send a voltage marker to the back (see page 254)
- To change voltage marker properties (see page 255)

To place voltage markers

Use Place Markers to quickly position a voltage marker. Depending on how you access the Place Markers feature, the marker is placed in the data a little differently. You can also move markers by dragging them with the mouse or by using the front-panel knobs. Where voltage markers intersect time markers, you can drag both markers at the same time.

- To drag and drop voltage markers (see page 252)
- To place a voltage marker at the mouse cursor (see page 252)
- To change a voltage marker's position property (see page 252)

To drag and drop voltage markers

Using the drag and drop feature you can move voltage markers to new positions in the data.

1. Click and hold down the mouse button on the marker you wish to move.
2. Move the mouse cursor to the new position.
3. Release the mouse button to reposition the marker.

To place a voltage marker at the mouse cursor

1. Point the mouse to the desired data point in the display.
2. Right-click, and select **Place Marker>Voltage>(desired marker)**.

To change a voltage marker's position property

1. Right-click on a voltage marker, and choose **Properties...**.

   Or, when viewing a display window that has voltage markers, choose **Markers>Properties...** from the main menu.
2. In the Waveform Properties dialog's Voltage Marker Properties tab, select the **Marker** to which the property changes apply.
3. In the **Position** box, position the marker by its voltage from ground or another voltage marker.
4. Click **OK** to apply the changes and close the properties dialog.

See Also

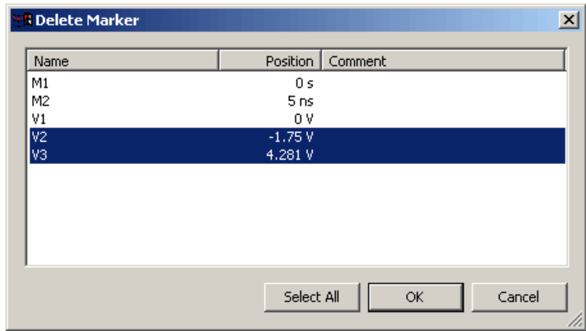
- To create new voltage markers (see page 250)
- To delete voltage markers (see page 252)
- To create a new voltage interval measurement (see page 253)
- To rename a voltage marker (see page 254)
- To send a voltage marker to the back (see page 254)
- To change voltage marker properties (see page 255)

To delete voltage markers

- In an analog signal's voltage markers/vertical scale display bar (to the left of the waveform), click the voltage marker you want to delete, and choose **Delete** from the popup menu (or choose **Delete All** to delete all voltage markers).

Or:

1. From the menu bar, select **Markers>Delete...**.
2. In the Delete Marker dialog, select the markers you wish to delete.



You can sort the list of markers by clicking on the Name, Position, or Comment column headings.

3 Click **OK**.

See Also

- To create new voltage markers (see page 250)
- To place voltage markers (see page 251)
- To create a new voltage interval measurement (see page 253)
- To rename a voltage marker (see page 254)
- To send a voltage marker to the back (see page 254)
- To change voltage marker properties (see page 255)

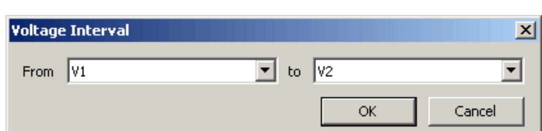
To create a new voltage interval measurement

Use the voltage interval measurement feature to measure a voltage between two voltage markers. Measurement results are displayed in the marker measurement display bar (see page 426).

1 In an analog signal row's voltage marker/vertical scale display bar (to the left of the waveform), click and choose **Measurements>New Voltage Interval Measurement**.

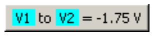
   Or, right-click in the marker measurement display bar and choose **New Voltage Interval Measurement>(analog signal name)**.

2 In the Voltage Interval dialog, select the markers you want to measure voltage between.



3 Click **OK** to close the Voltage Interval dialog.

The result of the interval measurement is displayed in the marker measurements display bar:



To rename a voltage marker

You can give voltage markers any name you choose.

1 In a Waveform window with voltage markers, right-click on the marker, and choose **Rename...**.

   Or, in the display window properties dialog's Voltage Marker Properties tab, select the **Marker**, and click **Rename...**.

2 In the Rename dialog, enter the new marker name.

   You can specify both a *long name* and an *abbreviated name* by using the "Long name[abbreviated name]" syntax; for example, "Location A[A]". When an abbreviated name is used, it appears on the marker in the voltage marker display bar while the long name appears in the marker *tool tip* (see page 655).

3 Click **OK**.

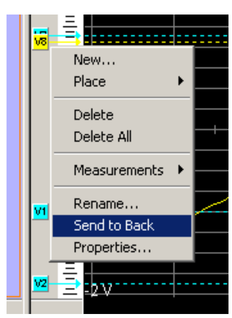
See Also

- To create new voltage markers (see page 250)
- To place voltage markers (see page 251)
- To delete voltage markers (see page 252)
- To create a new voltage interval measurement (see page 253)
- To send a voltage marker to the back (see page 254)
- To change voltage marker properties (see page 255)

To send a voltage marker to the back

When voltage markers overlap on the display, you can send the visible marker to the back in order to see the marker underneath.

1 Click the voltage marker you wish to send to the back, and choose **Send to Back** from the pop-up menu.



See Also

- To create new voltage markers (see page 250)

- To place voltage markers (see page 251)
- To delete voltage markers (see page 252)
- To create a new voltage interval measurement (see page 253)
- To rename a voltage marker (see page 254)
- To change voltage marker properties (see page 255)

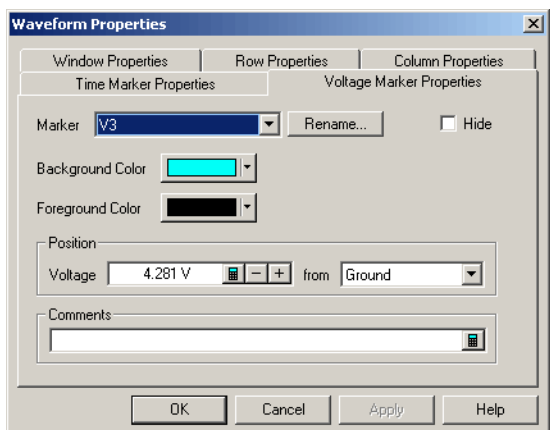
To change voltage marker properties

Once a voltage marker is created, you can modify any of its attributes from the Voltage Marker Properties tab..

1 Right-click on a voltage marker, and choose **Properties...**.

  Or, when viewing a Waveform display window that has voltage markers, choose **Markers>Properties...** from the main menu.

2 In the Waveform Properties dialog's Voltage Marker Properties tab:



  You can:

  - Select the **Marker** to which the property changes apply.
  - Rename a voltage marker (see page 254)
  - Change a marker's background color (see page 248)
  - Change a marker's foreground color (see page 248)
  - Change a voltage marker's position property (see page 252)
  - Hide/show a marker (see page 248)
  - Add comments to a marker (see page 249)

3 Click **OK** to apply the changes and close the properties dialog.

See Also

- To create new voltage markers (see page 250)
- To place voltage markers (see page 251)

- To delete voltage markers (see page 252)
- To create a new voltage interval measurement (see page 253)
- To rename a voltage marker (see page 254)
- To send a voltage marker to the back (see page 254)

Searching the Captured Data

You can search for bus/signal patterns in the captured data.

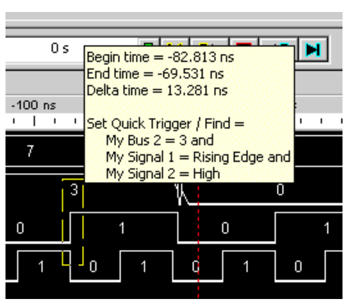
- To quickly find bus/signal patterns (see page 257)
- To find bus/signal patterns in the captured data (see page 259)
- To find packet patterns in the captured data (see page 261)
- To find complex patterns in the captured data (see page 265)
- To store, recall, or delete favorite find patterns (see page 266)
- To specify "found" marker placement (see page 267)

To quickly find bus/signal patterns

In the Waveform or Listing windows, you can quickly draw a rectangle and find the next or previous occurrence of that bus/signal pattern.

1. In the Waveform window, make sure the Fast Zoom In (see page 215) option is not selected.
2. Using the mouse, point to the upper-left corner of your desired bus/signal pattern.
3. While holding down the mouse button, drag the mouse pointer to the lower-right corner of your bus/signal pattern.

   As you draw the rectangle, a tool tip shows the selected bus/signal pattern.



   As you move the mouse left-to-right and top-to-bottom, the signal edge/level or bus value in contact with the **left of the rectangle** becomes the bus/signal pattern.

   Only one edge can be set.

If a bus is expanded into its separate signals, three conditions apply:

a If drawing starts on a bus, none of its expanded signals can be included.

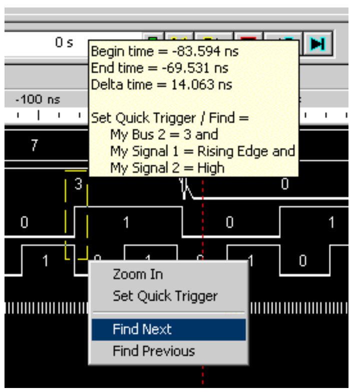
b If drawing starts on a signal, the bus cannot be included.

c Edges and levels are mutually exclusive. That is, either one edge can be set, or all levels can be set, but not both at the same time.

NOTE In the Waveform display window, it may be necessary to redraw the rectangle if you do not get your desired bus/signal pattern dictated by the left-side line of the rectangle. You could also try drawing the rectangle backwards leaving the left-side rectangle line set last.

---

4 When the desired bus/signal pattern has been selected, release the mouse button, and select **Find Next** or **Find Previous** from the popup menu.



5 Click the Previous or Next icons to see more occurrences.

General Guidelines

- Any bus/signals with overlapping bits are not included within the bus/signal pattern.

  Example: Bus_1 has channels 0 through 7 of pod 1 assigned and Bus_2 has channels 3 through 6 of pod 1 assigned. At this point, you have the same probed signals (channels 3 through 6 of pod 1) assigned in both Bus_1 and Bus_2. Now, you draw the rectangle over both bus_1 and bus_2. Because Bus_1 channels 3 through 6 are repeated (overlapped) on Bus_2, they will not be included in the bus/signal pattern.

See Also

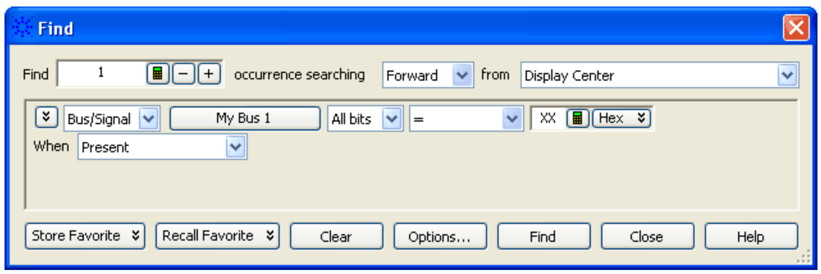
- To find bus/signal patterns in the captured data (see page 259)
- To find packet patterns in the captured data (see page 261)
- To find complex patterns in the captured data (see page 265)
- To store, recall, or delete favorite find patterns (see page 266)

To find bus/signal patterns in the captured data

This search option locates a specified data pattern. You can qualify your search by specific bits, data patterns, equality, and range operators. The search result is placed at the center of the display.

1 From the menu bar, choose **Edit>Find...**, or click the icon in the standard toolbar (see page 420).

2 In the **Find** dialog, enter the number of the occurrences you wish to find, select whether you want to search forward or backward from the start location; then, select the start location.



3 In the event specification area, select the **Bus/Signal** pattern type.

4 Specify the bus/signal pattern event you wish to locate.

In addition to the usual pattern matching operators (**=**, **!=**, **<**, **>**, **<=**, **>=**, **In Range**, and **Not In Range**), there are three additional operators you can use:

- **Entering** — the first sample of one or more consecutive samples that match the pattern. (By comparison, the "**=**" equals operator considers every sample that matches the pattern as an occurrence.)
- **Exiting** — the sample after one or more consecutive samples that match the pattern.
- **Transitioning** — entering or exiting one or more consecutive samples that match the pattern.

You can find analog signal values as well as digital signal values.

5 Select the desired **When** find qualifier (which further qualifies the find criteria with a time duration or other operator):

- **Present**
- **Not Present**
- **Present>** (time duration)
- **Present>=** (time duration)
- **Present<** (time duration)
- **Present<=** (time duration)

- **Present for Range** (of time)
- **Not Present for Range** (of time)
- **Entering**
- **Exiting**
- **Transitioning**

6 Click **Find**.

7 Click the Previous or Next icons to see more occurrences.

TIP

As you configure the find function, try to think of it as constructing a sentence that reads left-to-right. For example: "Find **1** occurrence **Forward** from the **Display Center** of a bus named **My Bus 1**, and on **All bits** a pattern that **Equals XX Hex**, display the event When all criteria is **Present**."

NOTE

The find qualifiers:

- **Present>**
- **Present>=**
- **Present<**
- **Present<=**
- **Present for Range**
- **Not Present for Range**

allow you to specify a time duration. This means that the find event specified in the expression area will be found based upon the given time and operator.

The other qualifiers:

- **Present**
- **Not Present**
- **Entering**
- **Exiting**
- **Transitioning**

do not allow a time duration.

See Also

- To quickly find bus/signal patterns (see page 257)
- To find packet patterns in the captured data (see page 261)
- To find complex patterns in the captured data (see page 265)
- To store, recall, or delete favorite find patterns (see page 266)
- To specify "found" marker placement (see page 267)

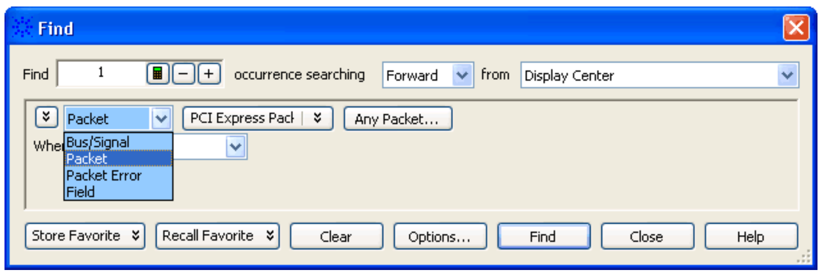
To find packet patterns in the captured data

In the Packet Viewer window, you can search for packets, packet errors, and field values.

1 With the Packet Viewer window open, choose **Edit>Find...** from the menu bar or click the icon in the standard toolbar (see page 420).

2 In the **Find** dialog, enter the number of the occurrences you wish to find, select whether you want to search forward or backward from the start location; then, select the start location.

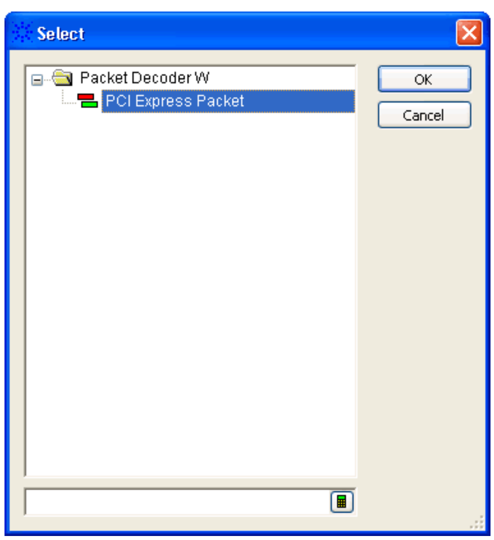
3 In the event specification area, select the **Packet**, **Packet Error**, or **Field** pattern type.



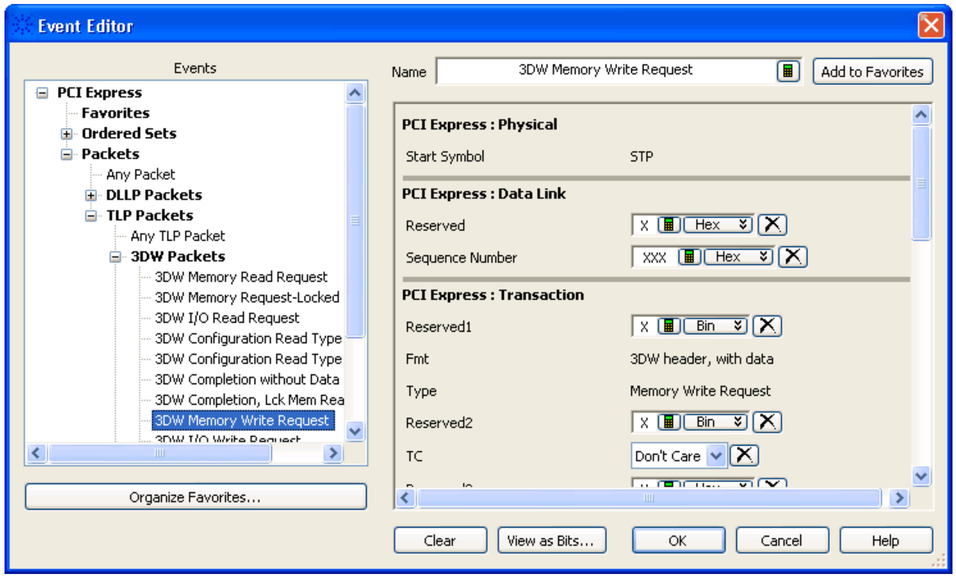
- To find packet events (see page 261)
- To find packet errors (see page 262)
- To find field values (see page 263)

To find packet events

1 You can click packet type button to open a selection dialog.



2 Click the packet event button to open the Event Editor dialog.



For more information, see Using the Packet Event Editor (see page 146)

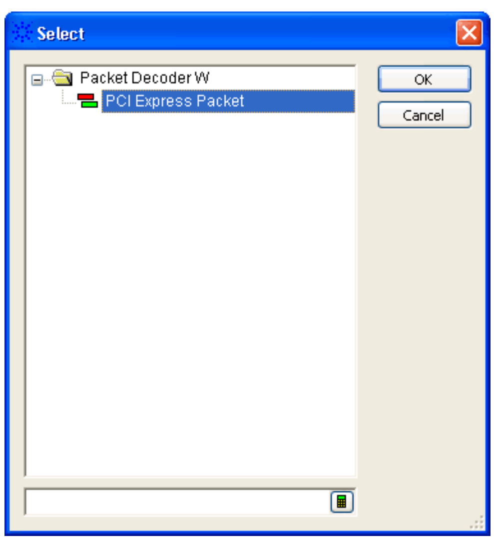
3 Select the desired **When** find qualifier (which further qualifies the find criteria with a time duration or other operator). For more information, see To find bus/signal patterns in the captured data (see page 259).

4 Click **Find**.

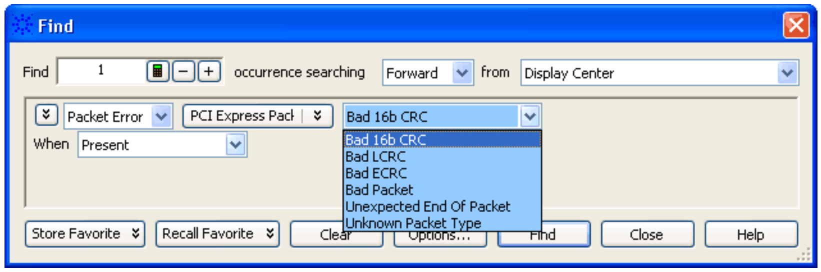
5 Click the Previous or Next icons to see more occurrences.

To find packet errors

1 You can click packet type button to open a selection dialog.



2 Select the packet error value:



3 Select the desired **When** find qualifier (which further qualifies the find criteria with a time duration or other operator). For more information, see To find bus/signal patterns in the captured data (see page 259).

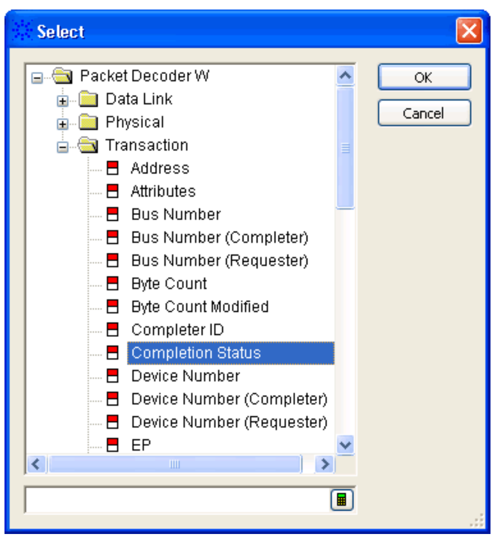
4 Click **Find**.

5 Click the Previous  or Next  icons to see more occurrences.

To find field values

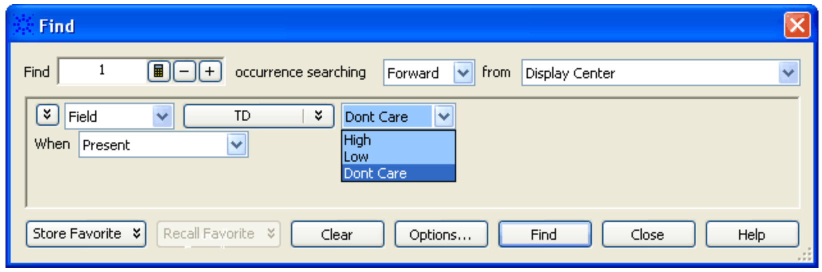
1 Select the field name.

Clicking  lets you select from recently used field names. Clicking elsewhere on a field name button opens a Select dialog for selecting a different name.



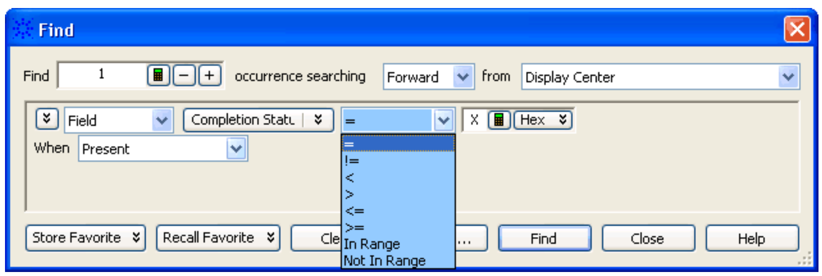
2 Specify the field value:

If a single-bit field has been selected, select the signal pattern value (**High**, **Low**, or **Dont Care**).

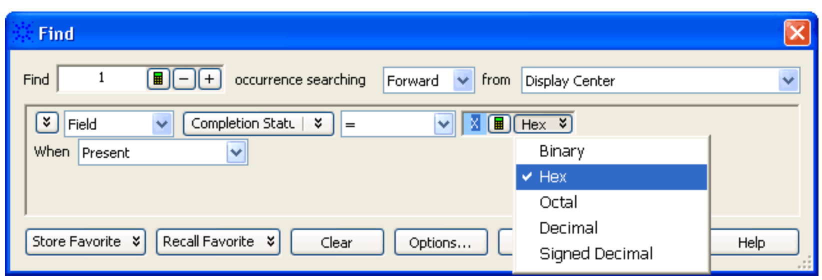


If a multiple-bit field has been selected:

a Select one of the operators: **=** (equal to), **!=** (not equal to), **<** (less than), **>** (greater than), **<=** (less than or equal to), **>=** (greater than or equal to), **In Range**, or **Not In Range**.



b Select the number base (**Binary**, **Hex**, **Octal**, **Decimal**, or **Signed Decimal**).



c Enter the pattern value(s).

3 Select the desired **When** find qualifier (which further qualifies the find criteria with a time duration or other operator). For more information, see To find bus/signal patterns in the captured data (see page 259).

4 Click **Find**.

5 Click the Previous  or Next  icons to see more occurrences.

See Also

- To quickly find bus/signal patterns (see page 257)
- To find bus/signal patterns in the captured data (see page 259)
- To find complex patterns in the captured data (see page 265)

- To store, recall, or delete favorite find patterns (see page 266)
- To specify "found" marker placement (see page 267)

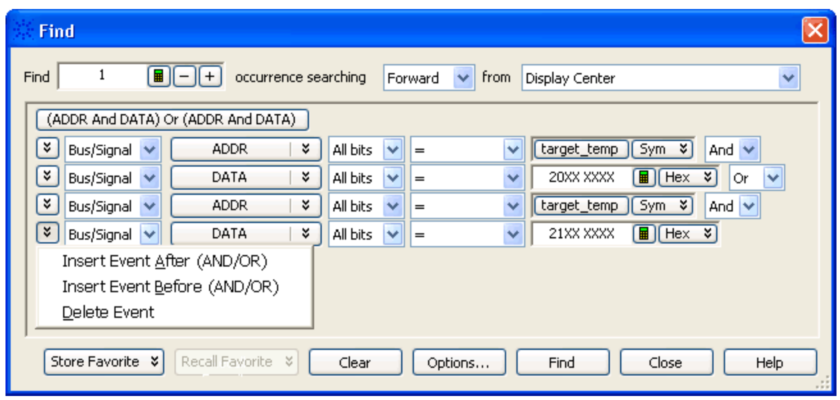
To find complex patterns in the captured data

You can expand search criteria to include more than one event describing data patterns.

1 From the menu bar, choose **Edit>Find...**, or click the icon in the standard toolbar (see page 420).

2 In the **Find** dialog, select the number of the occurrences you wish to find, select whether you want to search forward or backward from the start location; then, select the start location.

3 Select the pattern event drop down menu to choose **Insert Event After (AND/OR)** or **Insert Event Before (AND/OR)** to insert new find events.



The **Delete Event** option will delete the current event only if there is more than one event present.

4 For each event you add, select either **And** or **Or** to specify how the event patterns are combined.

AND'ed searches find occurrences of both events, while OR'ed searches find occurrences of either event.

When you have AND'ed and OR'ed events, a button appears above the events for changing the event evaluation order.

5 For each event, select the bus or signal name and enter the value you want to locate.

6 Click **Find**.

See Also

- To quickly find bus signal patterns (see page 257)
- To find bus/signal patterns in the captured data (see page 259)

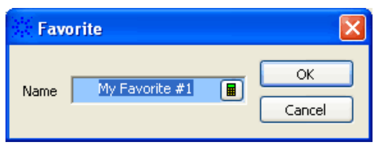
- To find packet patterns in the captured data (see page 261)
- To store, recall, or delete favorite find patterns (see page 266)
- To specify "found" marker placement (see page 267)

To store, recall, or delete favorite find patterns

- To store a favorite pattern (see page 266)
- To recall a favorite pattern (see page 266)
- To delete a favorite pattern (see page 267)

To store a favorite pattern

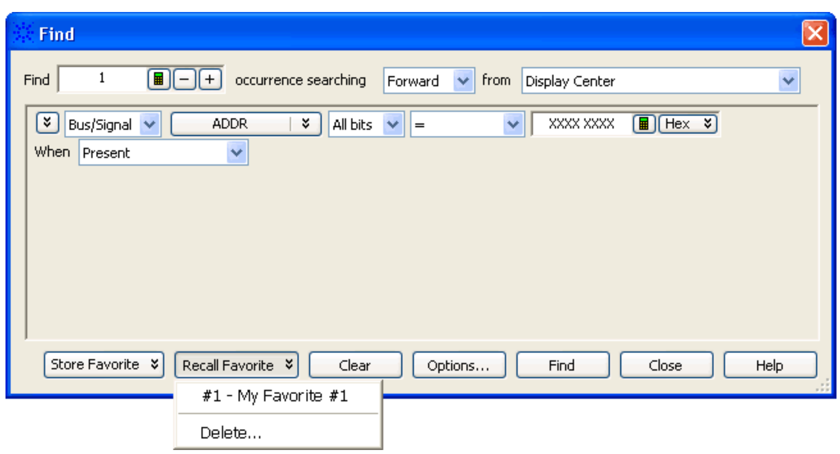
1. From the menu bar select, **Edit>Find...**, or click the icon.
2. Set up the pattern you want to find (see To find bus/signal patterns in the captured data (see page 259) or To find complex bus/signal patterns in the captured data (see page 265)).
3. Click **Store Favorite**.



4. Enter the name of the find pattern.
5. Click **OK** to save the find pattern.

To recall a favorite pattern

1. From the menu bar select, **Edit>Find...**, or click the icon.
2. Select **Recall Favorite**; then, select the find pattern you want to use from the drop down menu.



3. Click **Find**.

To delete a favorite pattern

1 From the menu bar select, **Edit>Find...**, or click the icon.
2 Select **Recall Favorite**; then, select **Delete...**.
3 In the Delete Favorites dialog, select the find patterns you wish to delete; then, click **Delete**.

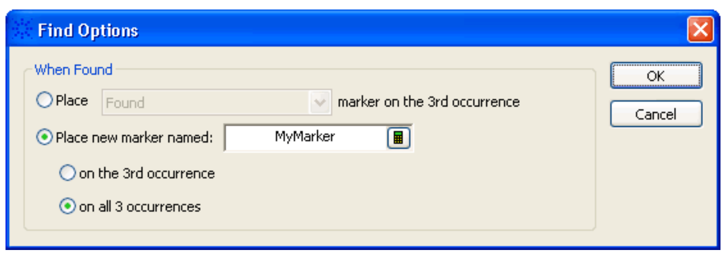
See Also

- Searching the Captured Data (see page 257)
- To specify "found" marker placement (see page 267)

To specify "found" marker placement

When searching for a pattern, you can place an existing marker on the last occurrence, or you can place a new marker on the last occurrence or on all occurrences.

1 From the menu bar select, **Edit>Find...**, or click the icon in the standard toolbar (see page 420).
2 In the Find dialog, set up the pattern you want to find.
3 Click **Options...**.



To place an existing marker on the last occurrence

1 Select the **Place** option.
2 Select the marker you want to place from the drop down menu.
3 Click **OK**.

To place a new marker

1 Select **Place new marker named:**.
2 Enter the name of the new marker.
3 Select whether you want to place the new marker **on the last occurrence** or **on all occurrences**.

   The **on all occurrences** option is only available when you are finding more than one occurrence.
4 Click **OK**.

See Also

- Searching the Captured Data (see page 257)
- To store, recall, or delete favorite find patterns (see page 266)
- To place markers in data (see page 237)

Comparing Captured Data to Reference Data

By comparing data from different acquisitions, you can look for differences between a known-good device under test and a device under test with a problem or one that is operating under different conditions.

To compare captured to reference data:

1. Capture (or load) the data you want to use as the reference data.
2. Select **Window>New Compare...** to open a new Compare display window.
3. In the Compare display window, click the **Copy...** button to select the current data that should be copied to the reference buffer.
4. Capture (or load) the data that you want to compare to the reference.

   Differences are highlighted in the Compare window.

For more information on comparing captured data to reference data, see:

- To copy data to the reference buffer (see page 268)
- To find differences in the compared data (see page 269)
- To compare only a range of samples (see page 269)
- To offset the reference data (see page 270)
- To run until a number of compare differences (see page 270)
- To set Compare window properties (see page 270)

See Also

- Compare Display Window (see page 436)
- Capturing Data from the Device Under Test (see page 127)
- Loading Saved Data and Setups (see page 184)

To copy data to the reference buffer

1. In the Compare display window, click the **Copy...** button.
2. In the Select Buses/Signals dialog:
   a. From the available buses and signals, select the ones to be copied to the reference buffer and click **Add>>**.

      To remove buses and signals from the selected list, select them and click **<<Remove**.

   b. Select either *All* data or a range of data using markers.
3. When you are ready to begin the copy, click **OK**.

NOTE Copying generated bus/signal columns, such as those created by an inverse assembler or an analysis tool, takes longer because of the extra processing to re-create the data.

NOTE

If your logic analyzer has deep memory, it takes a while to copy data to the reference buffer.

To find differences in the compared data

In the Compare display window:

- Click the >> button to find the next difference (below the center reference).
- Click the << button to find the previous difference (above the center reference).
- Click a blue tick mark in the **Compare Overview** bar (between the vertical scroll bar and the Marker Overview bar on the right side of the window) to go to that difference.

NOTE

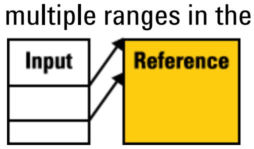
When a difference occurs on a subrow (for example, when the data is inverse-assembled or decoded by an analysis tool), the next and previous buttons go to the sample row instead of the subrow.

To compare only a range of samples

1 In the Compare display window, click the **Range & Offset...** button.
2 In the Range & Reference dialog, select either *All* data or a range of data using markers.
3 Click **OK**.

NOTE

When you specify a range to compare, the range is compared to the *top* of the reference buffer (unless the reference data has been offset (see page 270) by a number of samples) and not the same range in the reference buffer as you might expect. This behavior allows multiple ranges in the input data to be compared with the reference data.



To offset the reference data

When there are differences in the number of samples captured before the trigger, or when you are comparing a range of samples, you can offset the reference data so that the samples being compared are properly aligned.

1 In the Compare display window, click the **Range & Offset...** button.
2 In the Range & Reference Offset dialog, enter the number of samples to offset the reference by.
3 Click **OK**.

See Also

- To compare only a range of samples (see page 269)

To run until a number of compare differences

The Compare display lets you stop comparing, stop a repetitive run, or send e-mail after a run has more than a specified number of differences when compared to the reference data.

1 In the Compare display window, click **Compare Until...**.
2 In the Difference Properties tab of the Compare Properties dialog, enter the number of differences that will stop comparing, stop a repetitive run, or send an e-mail message.
3 To stop a compare after the number of differences have been found, select the **Stop comparing** check box.
4 To stop a repetitive run after the number of differences have been found, select the **Stop repetitive run** check box.
5 To send e-mail after the number of differences have been found, select the **Send e-mail** check box; then, click the **E-mail...** button. In the E-mail dialog (see page 453), enter the address to which e-mail will be sent, the subject, and the text of the message.
6 Click **OK** in the Compare Properties dialog.
7 Start the repetitive run measurement.

See Also

- Starting/Stopping Measurements (see page 168)

To set Compare window properties

1 In the Compare display window, right-click on the bus/signal column name; then, select **Properties...** from the popup menu.
2 In the Compare Properties dialog:
   - The **Window Properties** tab lets you select the reference data background color, the background color that indicates no reference data, and the difference foreground and background colors.

- The **Column Properties** tab's Display field lets you display **All** of the reference data, just the reference data where a difference was found (**Difference Pair**), or only the highlighted differences in the data being compared (**Input Only**).
- The **Difference Properties** tab lets you select the options for running until a number of compare differences are found.

All other Compare property options are the same as in the Listing window.

See Also

- To set Listing window properties (see page 226)
- To run until a number of compare differences (see page 270)

Viewing Source Code Associated with Captured Data

1 Add and configure the appropriate inverse assembler tool (see "Using Inverse Assembler Tools" (in the online help)).

2 Load line number symbols (see To load symbols from a file (see page 118)).

3 Select **Window>New Source...** to open a new Source display window.

4 In the Add New Window after dialog, select the inverse assembler or filter/colorize tool that the Source window should be added after.

   Generally, you want the Source window getting the same data as other display windows (Listing, Waveform, etc.).

5 In the source display pane of the Source window, right-click, and choose **Properties...**.

6 In the Source Viewer Properties dialog's Source Code Directories tab, click **Add...** tab.

7 In the Browse for Folder dialog, select the directory that contains the source files, and click **OK**.

8 Click **OK** to close the Source Viewer Properties dialog.

For more information on viewing the source code associated with captured data, see:

- To step through captured data by source lines (see page 273)
- To go to captured data associated with a source line (see page 273)
- To browse source files (see page 274)
- To search for text in source files (see page 274)
- To set a Quick Trigger in the Source window (see page 131)
- To go to the source line associated with the listing center rectangle (see page 275)
- To edit the source code directory list (see page 275)
- To select the correlation bus (see page 276)
- Changing Source Window Properties (see page 277)
  - To change the source background color (see page 277)
  - To change the source text color (see page 278)
  - To change the source font size (see page 278)
  - To change the source tab width (see page 278)
  - To show/hide source line numbers (see page 278)
  - To change the "Set Quick Trigger" alignment (see page 279)

See Also

- Analyzing Listing Data (see page 222)

- Source Display Window (see page 437)

To step through captured data by source lines

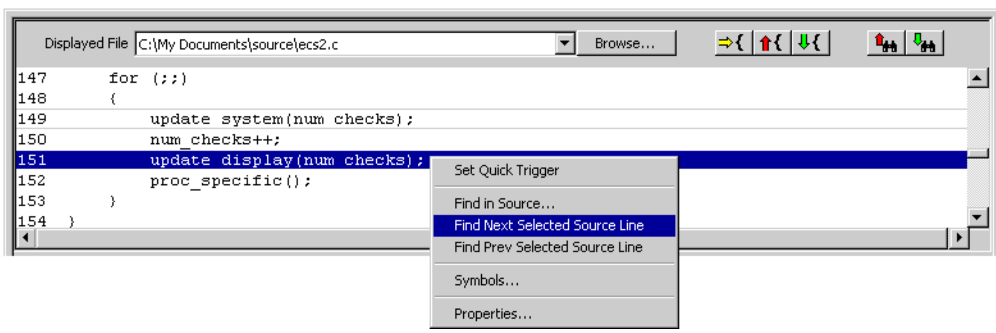
1 In the Source window's source pane, click the step to next source line or step to previous source line buttons.

  The listing pane is updated to show the captured data associated with the next or previous source line, and the source pane is updated to show the next or previous source line.

See Also

- Viewing Source Code Associated with Captured Data (see page 272)

To go to captured data associated with a source line



1 In the Source window's source pane, click the source line whose associated captured data you want to view.

2 Click the find next selected source line or find previous selected source line buttons.

  Or, right-click the selected source line and choose **Find Next Selected Source Line** or **Find Prev Selected Source Line**.

  If captured data associated with the source line is found, the listing pane is updated to show the captured data, and the source pane is updated to show the selected source line.

  If captured data associated with the source line is not found, an information dialog is displayed.

See Also • Viewing Source Code Associated with Captured Data (see page 272)

To browse source files

1 In the Source window's source pane, click **Browse...**.

2 In the Select Source File to Open dialog, select the source file to browse, and click **Open**.

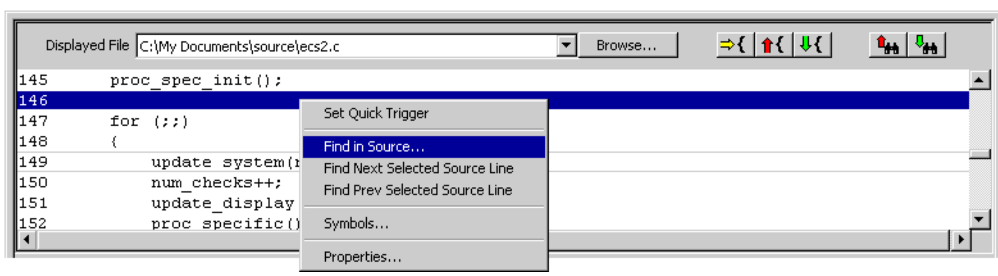
The selected source file appears in the source pane.

See Also

- To search for text in source files (see page 274)
- To set a Quick Trigger in the Source window (see page 131)
- To go to the source line associated with the listing center rectangle (see page 275)
- Viewing Source Code Associated with Captured Data (see page 272)

To search for text in source files

1 In the Source window's source pane, right-click choose **Find in Source...**.



2 In the Find dialog, enter the text to search for, select the direction to search, and click **Find Next**.

If the text is found, the source line is highlighted.

If the text is not found, an information dialog is displayed.

See Also

- To set a Quick Trigger in the Source window (see page 131)
- To go to the source line associated with the listing center rectangle (see page 275)
- Viewing Source Code Associated with Captured Data (see page 272)

To go to the source line associated with the listing center rectangle

After browsing or searching for text in source files, you may want to return to displaying the source line associated with the captured data displayed in the listing pane.

1 In the Source window's source pane, click the  show correlated source line button.

   The source pane is updated to show either the source line associated with the listing center rectangle or "No matching symbol found.".

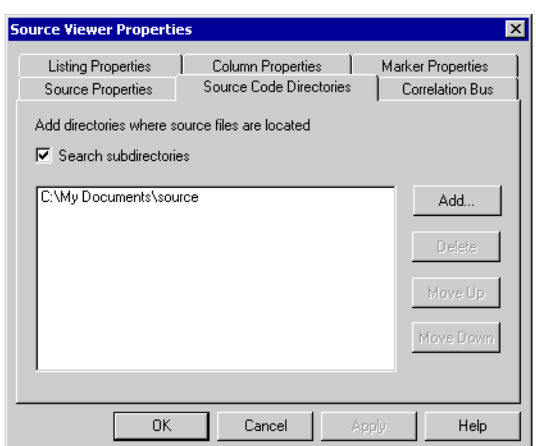
See Also

- Viewing Source Code Associated with Captured Data (see page 272)

To edit the source code directory list

Because source file paths specified in the symbol file may not be valid if you compile on one computer and debug on another, you can specify the directories where source code is located.

1 In the Source window display areas, right-click, and choose **Properties...**.
2 Or, choose **Edit>Window Properties...** from the main menu.
3 In the Source Viewer Properties dialog's Source Code Directories tab:



You can:

- Add a directory to the search list by clicking **Add...**.
- Specify whether subdirectories are included in or excluded from the search by checking or unchecking **Search subdirectories**.
- Change a directory's order in the search list by highlighting a directory and clicking **Move Up** or **Move Down**.
- Delete directory from the search list by highlighting a directory and clicking **Delete**.

4 Click **OK** to apply the changes and close the Source Viewer Properties dialog.

See Also

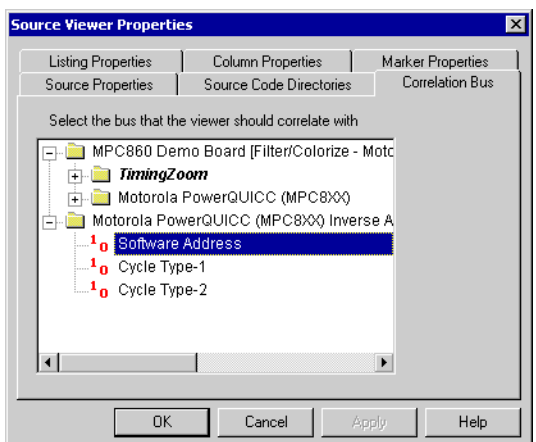
- Viewing Source Code Associated with Captured Data (see page 272)

To select the correlation bus

1 In the Source window display areas, right-click, and choose **Properties...**.

2 Or, choose **Edit>Window Properties...** from the main menu.

3 In the Source Viewer Properties dialog's Correlation Bus tab, select the bus on which the Source window should look for line number symbols.



Typically, you will select the "software address" bus generated by an inverse assembler tool or another address bus.

4 Click **OK** to apply the changes and close the Source Viewer Properties dialog.

See Also

- Viewing Source Code Associated with Captured Data (see page 272)

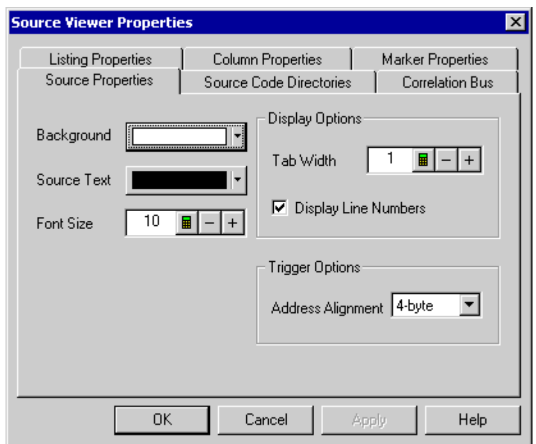
Changing Source Window Properties

You can change properties that affect the source code pane of the Source display window.

1 In the source display pane of the Source window, right-click, and choose **Properties...**.

2 Or, choose **Edit>Window Properties...** from the main menu.

3 In the Source Viewer Properties dialog's Source Properties tab:



You can:

- Change the source background color (see page 277)
- Change the source text color (see page 278)
- Change the source font size (see page 278)
- Change the source tab width (see page 278)
- Show/hide source line numbers (see page 278)
- Change the "Set Quick Trigger" alignment (see page 279)

4 Click **OK** to apply the changes and close the Source Viewer Properties dialog.

See Also

- Changing Listing Window Properties (see page 226)
- Changing Bus/Signal Column Properties (see page 228)

To change the source background color

1 In the Source Viewer Properties dialog's Source Properties tab, click the **Background** color selection button and select the desired background color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Source Viewer Properties dialog.

To change the source text color

1 In the Source Viewer Properties dialog's Source Properties tab, click the **Source Text** selection button and select the desired color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Source Viewer Properties dialog.

To change the source font size

1 In the Source Viewer Properties dialog's Source Properties tab, enter the desired **Font Size**.

Fonts can range from size 6 through 72 points.

2 Click **OK** to apply the changes and close the Source Viewer Properties dialog.

To change the source tab width

1 In the Source Viewer Properties dialog's Source Properties tab, enter the desired **Tab Width**.

Tab widths can range from 1 to 10 spaces.

2 Click **OK** to apply the changes and close the Source Viewer Properties dialog.

To show/hide source line numbers

1 In the Source Viewer Properties dialog's Source Properties tab, check or uncheck **Display Line Numbers** to specify whether source file line numbers are shown or hidden.

2 Click **OK** to apply the changes and close the Source Viewer Properties dialog.

To change the "Set Quick Trigger" alignment

For microprocessors that fetch blocks of instructions at a time (from block boundary addresses only), the address alignment property lets you adjust the source line symbol values to be on block boundary addresses when setting up Quick Triggers on a source line.

1 In the Source Viewer Properties dialog's Source Properties tab, select the desired **Address Alignment**.

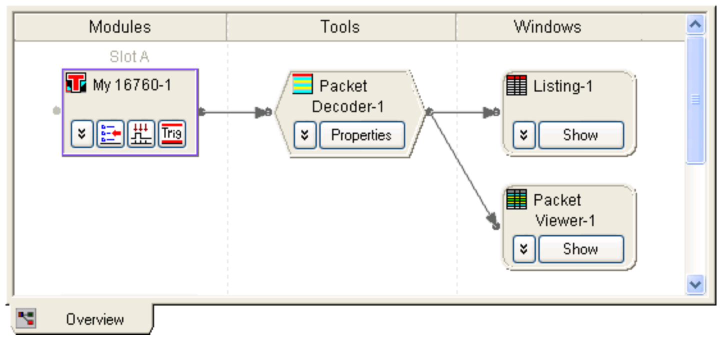
2 Click **OK** to apply the changes and close the Source Viewer Properties dialog.

See Also

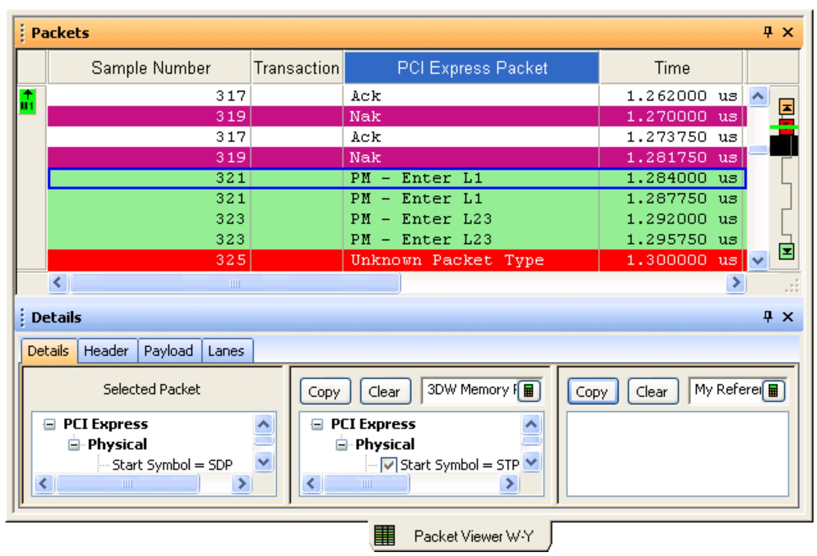
• To set a Quick Trigger in the Source window (see page 131)

Analyzing Packet Data

You can use a Packet Viewer window to display data from a Packet Decoder tool.



Unlike the Listing window, the Packet Viewer window lets you view summarized and detailed packet information at the same time within two *panes*.



The upper packet summary pane is similar to a Listing window except that its columns display decoded packets and fields instead of bus/signal values. Like a Listing window, you can insert time or pattern markers.

The lower pane contains tabs for viewing selected packet details, header, payload, and lane information.

The Packer Viewer window is customized for the protocol family being decoded.

The **Window** menu lets you add new Packet Viewer windows or view Packet Viewer windows that have already been added (by choosing from the open window names at the bottom of the menu). If tabbed windows (see page 305) are turned on, you can also view Packet Viewer windows by selecting the tab at the bottom of the window.

- Viewing the Packet Summary (see page 282)
  - To go to different locations in the decoded data (see page 282)
  - To re-arrange packet decode columns (see page 284)
  - To insert or delete packet decode columns (see page 284)
  - To find a packet decode column (see page 284)
  - To show/hide parts of the packet summary display (see page 285)
- Viewing a Selected Packet (see page 285)
  - To view and compare packet details (see page 286)
  - To view a packet header (see page 287)
  - To view a packet payload (see page 287)
  - To view a packet's lanes (see page 288)
  - To show/hide Packet Viewer panes (see page 289)
- Changing Packet Summary Event Colors (see page 289)
- Changing Packet Viewer Window Properties (see page 290)
  - To change the Packet Viewer background color (see page 291)
  - To change the selected row box color (see page 292)
  - To change the Packet Viewer font size (see page 292)
  - To lock scrolling with other display windows (see page 292)
- Changing Packet Summary Column Properties (see page 293)
  - To change a packet decode column's data color (see page 294)
  - To change the width of a packet decode column (see page 294)
  - To change the alignment of a packet decode column (see page 294)
  - To change a packet decode column's number base (see page 295)
  - To select the marker for marker-relative times (see page 296)
  - To select fixed time units (see page 296)
- "Customizing Protocol Descriptions for Packet Viewer" (in the online help)

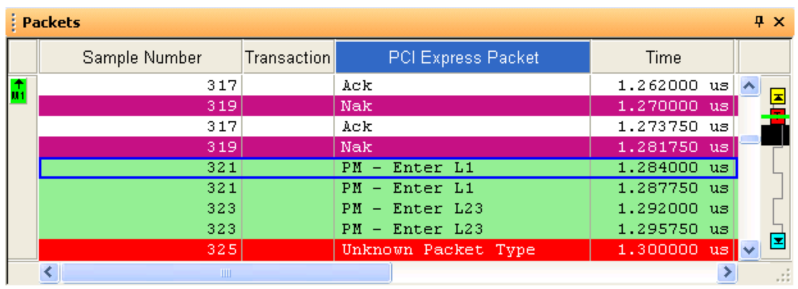
See Also

- To specify packet events (in "Find a packet" trigger function) (see page 145)
- To find packet patterns in the captured data (see page 261)
- "To specify packet patterns to filter" (in the online help)

- Marking, and Measuring Between, Data Points (see page 234)
- Displaying Names (Symbols) for Packet Summary Column Values (see page 232)
- Searching the Captured Data (see page 257)

Viewing the Packet Summary

The upper packet summary pane of the Packet Viewer window is similar to a Listing window except that its columns display decoded packets and fields instead of bus/signal values. Like a Listing window, you can insert time or pattern markers.



Click a line to select a packet. Notice that a colored box highlights the selected line. You can use the up-arrow or down-arrow keys to select the previous or next packets.

- To go to different locations in the decoded data (see page 282)
- To re-arrange packet decode columns (see page 284)
- To insert or delete packet decode columns (see page 284)
- To find a packet decode column (see page 284)
- To show/hide parts of the packet summary display (see page 285)

See Also

- Changing Packet Summary Event Colors (see page 289)
- Changing Packet Viewer Window Properties (see page 290)
- Changing Packet Summary Column Properties (see page 293)
- Viewing a Selected Packet (see page 285)
- Marking, and Measuring Between, Data Points (see page 234)
- Searching the Captured Data (see page 257)

To go to different locations in the decoded data

In the Packet Viewer window, you can go to different locations in the captured data by using the vertical scroll bars, by using the Go To buttons on the standard toolbar, or by choosing Go To commands from popup menus.

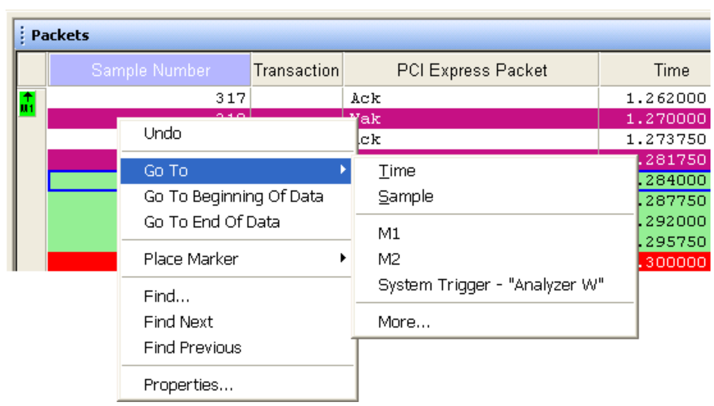
To go to different locations using toolbar buttons

1 Click one of the Go To buttons in the standard toolbar.

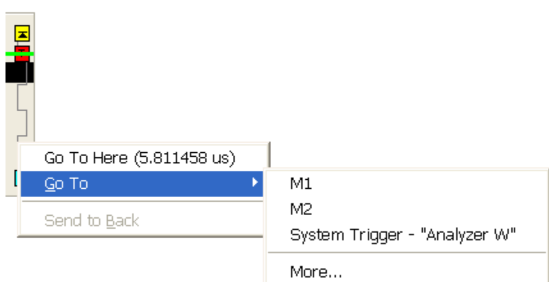
	Go to Beginning — centers the beginning of the decoded data.
	Go to Trigger — centers the trigger point in the decoded data.
	Go to End — centers the end of the decoded data.

To go to different locations using popup menus

1 Right-click in the packet summary display area, and choose one of the **Go To** commands.



Or, click in the marker overview bar, and choose one of the **Go To** commands.



You can choose **Beginning Of Data**, **End Of Data**, **Trigger**, a marker, a **Time**, or a **Sample**.

To re-arrange packet decode columns

1 Position the mouse pointer over the packet field column you want to move.

2 Click and hold the mouse button.

3 Drag-and-drop the packet decode column to its new position.

The column is placed to the left of the red position indicator that appears.

To insert or delete packet decode columns

To insert packet decode columns

1 In the Packet Viewer window, right-click in the column headings; then, choose **Insert Column...**, **Insert Column Before...**, or **Insert Column After...**.

2 In the Insert dialog, select the packet decode column you want to insert; then, click **OK**.

To delete selected packet decode columns

1 Highlight the headings of the columns you want to delete (by clicking, Shift-clicking, or Ctrl-clicking the column names).

2 Right-click in (one of) the selected column heading(s); then, choose **Delete>Column(s)**.

See Also

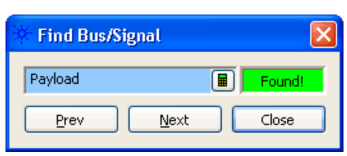
- "Using the Packet Decoder Tool" (in the online help)

To find a packet decode column

When there are many columns in the Packet Viewer window, you can search for a particular column instead of scrolling through all the columns.

1 In the Packet Viewer window, right-click in any column heading, and choose **Find Bus/Signal...**.

2 In the Find Bus/Signal dialog, enter the name (or part of the name) of the column you wish to find.

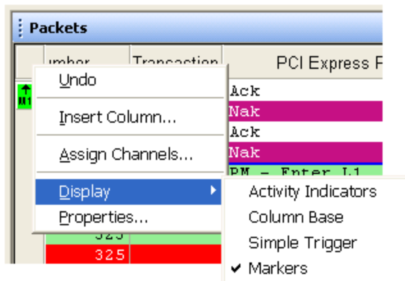


3 Then, click:

- **Prev** — to search for the string backward in the columns.
- **Next** — to search for the string forward in the columns.
- **Close** — to close the Find Bus/Signal dialog.

To show/hide parts of the packet summary display

1 Right-click in the column heading of the Packet Viewer display, and choose **Display>**.



Then, check or uncheck one of the following to show or hide that part of the Packet Viewer display window:

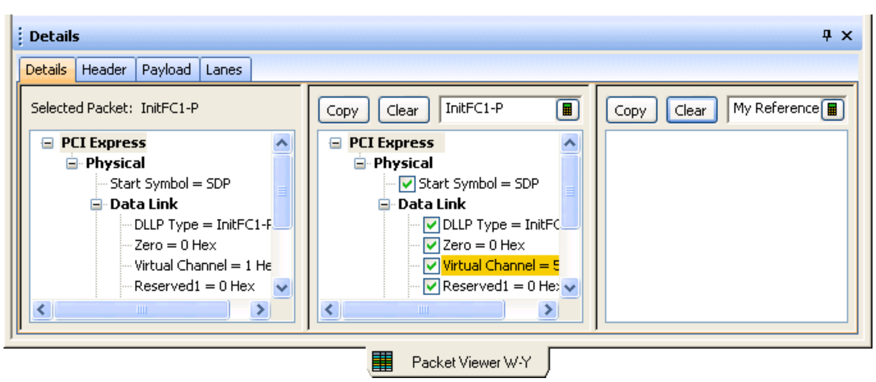
- **Activity Indicators** — not applicable to the Packet Viewer window.
- **Column Base** — the number base row in the column headings.
- **Simple Trigger** — not applicable to the Packet Viewer window.
- **Markers** — the markers display bar (see page 431).

You can also make these selections in the **Display Options** area of the Packet Viewer Properties dialog's Window Properties tab.

See Also • Changing Packet Viewer Window Properties (see page 290)

Viewing a Selected Packet

When a packet is selected in the upper packet summary portion of the Packet Viewer window (by clicking on a line or by using the up arrow or down arrow keys to highlight the previous or next line), information about the selected packet appears in the lower part of the window.



• To view and compare packet details (see page 286)

- To view a packet header (see page 287)
- To view a packet payload (see page 287)
- To view a packet's lanes (see page 288)
- To show/hide Packet Viewer panes (see page 289)

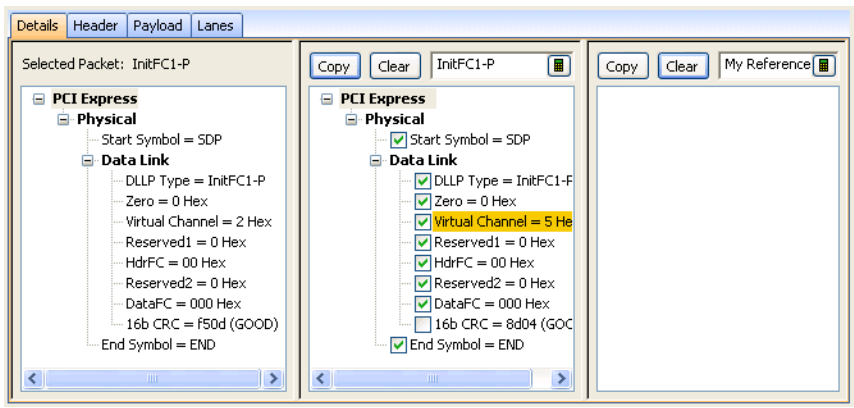
See Also

- Using the Packet Summary Pane (see page 228)

To view and compare packet details

To view packet details

1. Select a packet in the upper packet summary portion of the Packet Viewer window (by clicking on a line or by using the up arrow or down arrow keys to highlight the previous or next line).
2. Select the **Details** tab in the lower portion of the window.



Packet details appear under "Selected Packet" at the left.

If you hold the mouse pointer motionless for a second over one of the packet details, a *tool tip* (that is, a small box with text) appears with more information.

3. You can expand or collapse the displayed information by clicking "+" or "-" in the packet hierarchy tree.

To compare packet details

1. Click **Copy** to copy the selected packet information to one of the compare buffers at the right.
2. If desired, you can enter a name for the compare buffer.
3. Select another packet in the upper packet summary portion of the Packet Viewer window.

   Differences between packets of a similar type are highlighted in the packet buffer.
4. If you don't want differences in certain fields to be highlighted, you can uncheck the fields by clicking the check box.

Click **Clear** to clear a compare buffer.

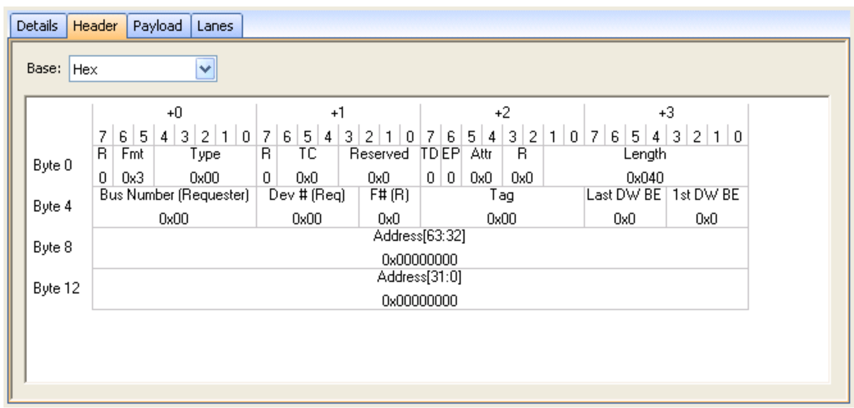
See Also

- To view a packet header (see page 287)
- To view a packet payload (see page 287)
- To view a packet's lanes (see page 288)

To view a packet header

1 Select a packet in the upper packet summary portion of the Packet Viewer window (by clicking on a line or by using the up arrow or down arrow keys to highlight the previous or next line).

2 Select the **Header** tab in the lower portion of the window.



If you hold the mouse pointer motionless for a second over one of the header fields, a *tool tip* (that is, a small box with text) appears with more information about the field.

3 If desired, you can select a different number **Base**.

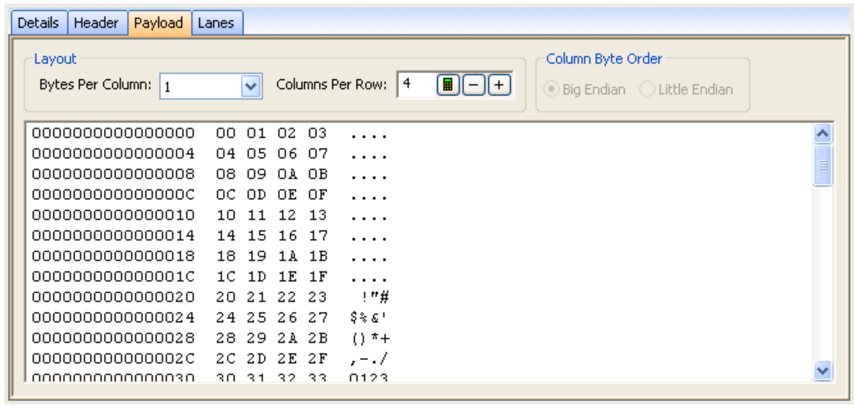
See Also

- To view and compare packet details (see page 286)
- To view a packet payload (see page 287)
- To view a packet's lanes (see page 288)

To view a packet payload

1 Select a packet in the upper packet summary portion of the Packet Viewer window (by clicking on a line or by using the up arrow or down arrow keys to highlight the previous or next line).

2 Select the **Payload** tab in the lower portion of the window.



Payload data bytes are displayed in the selected number of bytes per column and columns per row. The right-most column displays the row data in ASCII format.

3 You can format the display of payload bytes by selecting the **Bytes Per Column**, **Columns Per Row**, and **Column Byte Order** (when there is more than one byte per column).

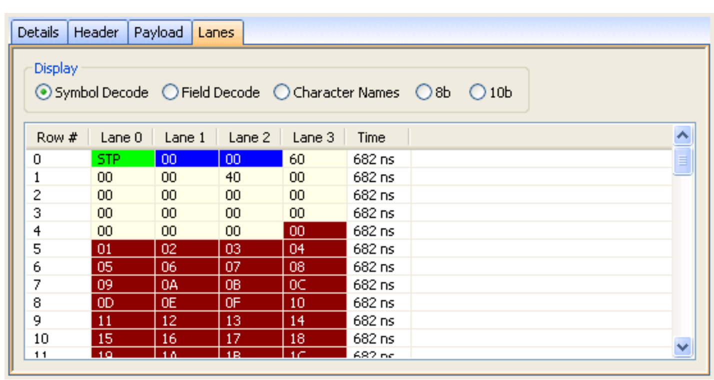
See Also

- To view and compare packet details (see page 286)
- To view a packet header (see page 287)
- To view a packet's lanes (see page 288)

To view a packet's lanes

1 Select a packet in the upper packet summary portion of the Packet Viewer window (by clicking on a line or by using the up arrow or down arrow keys to highlight the previous or next line).

2 Select the **Lanes** tab in the lower portion of the window.



If you hold the mouse pointer motionless for a second over one of the data values, a *tool tip* (that is, a small box with text) appears with more information about the data.

3 You can choose the format of the display by selecting one if the **Display** options:

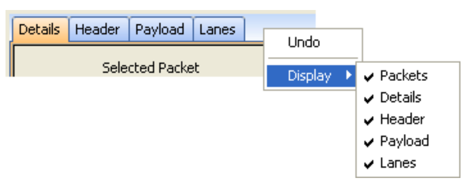
- **Symbol Decode**
- **Field Decode**
- **Character Names**
- **8b**
- **10b**

See Also

- To view and compare packet details (see page 286)
- To view a packet header (see page 287)
- To view a packet payload (see page 287)

To show/hide Packet Viewer panes

1 Right-click in the packet details area of the Packet Viewer window, and choose **Display>**.



Then, check or uncheck one of the following to show or hide that pane in the Packet Viewer window:

- **Packets**
- **Details**
- **Header**
- **Payload**
- **Lanes**

You can also make these selections in the **Pane Display Options** area of the Packet Viewer Properties dialog's Window Properties tab.

See Also

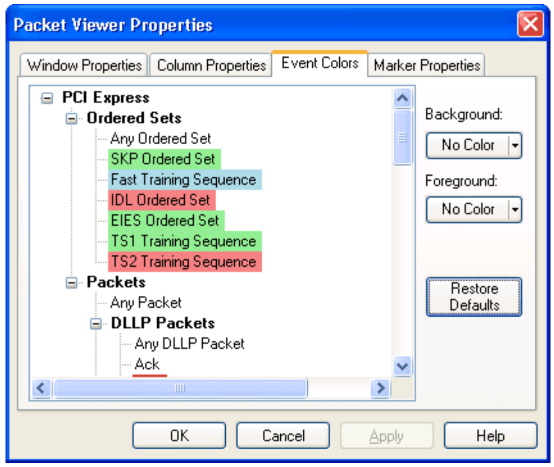
- Changing Packet Viewer Window Properties (see page 290)

Changing Packet Summary Event Colors

To change the colors associated with events in the Packet Viewer window:

1 Right-click in the packet summary portion of the window, and choose **Properties...**.

2 In the Packet Viewer Properties dialog, select the **Event Colors** tab.



3 In the Event Colors tab:

  a Select the packet event type whose color you want to change.

  b Select the **Background** color.

  c Select the **Foreground** color.

4 Click **OK** to apply the changes and close the Packet Viewer Properties dialog.

To restore event color defaults

1 In the Packet Viewer Properties dialog's Event Colors tab, click **Restore Defaults**.

2 Click **OK** to apply the changes and close the Packet Viewer Properties dialog.

See Also

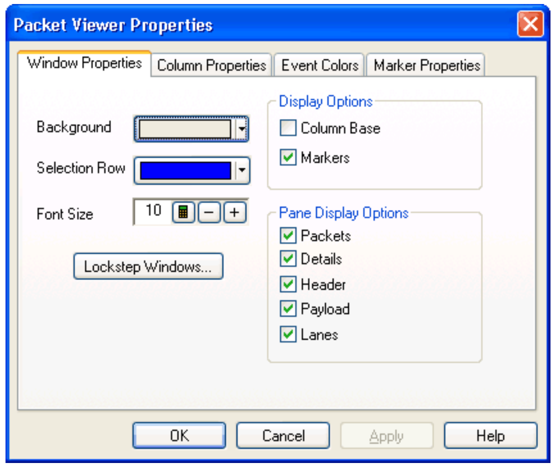
- Changing Packet Viewer Window Properties (see page 290)
- Changing Packet Summary Column Properties (see page 293)

Changing Packet Viewer Window Properties

You can change properties that affect the entire Packet Viewer display window.

1 Right-click in the packet summary portion of the window, and choose **Properties...**.

2 In the Packet Viewer Properties dialog, select the **Window Properties** tab.



3 In the Window Properties tab, you can:

- Change the Packet Viewer background color (see page 291)
- Change the selected row box color (see page 292)
- Change the Packet Viewer font size (see page 292)
- Lock scrolling with other display windows (see page 292)
- Show/hide parts of the packet summary display (see page 285)
- Show/hide Packet Viewer panes (see page 289)

4 Click **OK** to apply the changes and close the Packet Viewer Properties dialog.

See Also

- Changing Packet Summary Event Colors (see page 289)
- Changing Packet Summary Column Properties (see page 293)

To change the Packet Viewer background color

1 In the Packet Viewer Properties dialog's Window Properties tab, click the **Background** color selection button and select the desired background color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Packet Viewer Properties dialog.

To change the selected row box color

To highlight the selected line in the upper packet summary area of the Packet Viewer window, a box is drawn around it.

1 In the Packet Viewer Properties dialog's Window Properties tab, click the **Selection Row** color selection button and select the desired highlight box color from the palette.

   If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Packet Viewer Properties dialog.

To change the Packet Viewer font size

The font size property adjusts the data display and packet decode column heading text size.

1 In the Packet Viewer Properties dialog's Window Properties tab, enter the desired **Font Size**.

   Fonts can range from size 6 through 72 points.

2 Click **OK** to apply the changes and close the Packet Viewer Properties dialog.

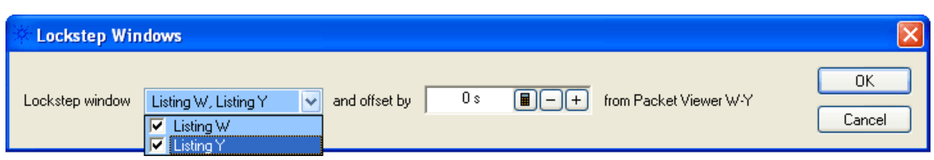
As the font size is changed, the column width may be automatically increased to fit the new text size.

To lock scrolling with other display windows

You can lock display windows (for example, Waveform, Listing, Compare, etc.) so that when one window is scrolled, others are scrolled as well, such that the same time is centered in each display.

1 In the Packet Viewer Properties dialog's Window Properties tab, click **Lockstep Windows...**.

2 In the Lockstep Windows dialog, select the display windows whose scrolling should be locked with this window and specify any offset from this window.



3 Click **OK** to close the Lockstep Windows dialog.

4 Click **OK** to apply the changes and close the Packet Viewer Properties dialog.

Changing Packet Summary Column Properties

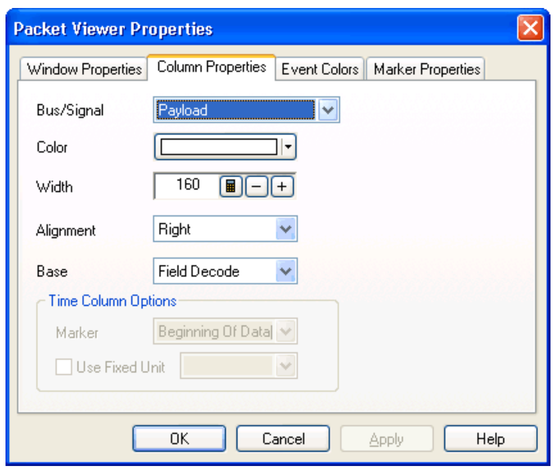
In the Packet Viewer display window, you can change the color, width, alignment, or number base of bus/signal data columns.

To change the properties of a bus/signal data column in the Packet Viewer window:

1 Right-click on a packet decode column, and choose **Properties...**.

   Or, highlight the packet decode columns whose properties you want to change (by clicking, Shift-clicking, or Ctrl-clicking the column headings), and choose **Edit>Window Properties...** from the main menu.

2 In the Packet Viewer Properties dialog's Column Properties tab:



   You can:

   - Select the **Bus/Signal** (really the packet decode column) to which the property changes apply. You can select:
     - Any packet decode column that is being displayed.
     - **<all>** packet decode columns.
     - **<selected>** packet decode columns if more than one column is highlighted.
   - Change a packet decode column's data color (see page 294)
   - Change the width of a packet decode column (see page 294)
   - Change the alignment of a packet decode column (see page 294)
   - Change a packet decode column's number base (see page 295)
   - Select the marker for marker-relative times (see page 296)
   - Select fixed time units (see page 296)

3 Click **OK** to apply the changes and close the Packet Viewer Properties dialog.

See Also

- Changing Packet Summary Event Colors (see page 289)
- Changing Packet Viewer Window Properties (see page 290)

To change a packet decode column's data color

1. In the Packet Viewer Properties dialog's Column Properties tab, click the **Color** selection button and select the desired packet decode column data color from the palette.

   If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2. Click **OK** to apply the changes and close the Packet Viewer Properties dialog.

To change the width of a packet decode column

TIP You can autosize individual columns by placing the mouse pointer over the right border of the column header box; then, when the pointer icon changes to a resizing pointer, double-click.

TIP If your keyboard has a numeric keypad, you can autosize all columns by selecting any column header box (to highlight it) and by pressing **Ctrl** and "+" on the numeric keypad.

1. In the packet decode headings row of the Packet Viewer window, position the mouse pointer over a column separator line; when the cursor changes to a resizing cursor, drag the column border.

Or:

1. In the Packet Viewer Properties dialog's Column Properties tab, enter the **Width** value in pixels.

   The minimum column width is 1 pixel, while the maximum width is 1000 pixels.

2. Click **OK** to apply the changes and close the Packet Viewer Properties dialog.

To change the alignment of a packet decode column

The Alignment property sets the display of data to be left-justified, right-justified, or centered within the column.

1. In the Packet Viewer Properties dialog's Column Properties tab, select the **Alignment** from:
   - **Left**
   - **Center**

- **Right**

2 Click **OK** to apply the changes and close the Packet Viewer Properties dialog.

To change a packet decode column's number base

The base property specifies the number base to use when displaying the decoded packet values.

1 In the Packet Viewer Properties dialog's Column Properties tab, select the desired number **Base** from:

- **Binary**
- **Hex**
- **Octal**
- **Decimal**
- **Signed Decimal** (the only choice for the "Sample Number" column)
- **Ascii**
- **Symbol** (see Displaying Names (Symbols) for Bus/Signal Values (see page 232))
- **Hardware Address**
- **Dot Notation**
- **Field Decode**

For the main packet decode information column, you can select from:

- **Packet Summary**
- **Packet Bytes**

For other generated packet decode columns, the only choice may be:

- **String**

If the "Time" column has been selected instead of a data column, your choices change from a numeric format to:

- **Absolute**
- **Relative Previous**
- **Relative Marker**

2 Click **OK** to apply the changes and close the Packet Viewer Properties dialog.

To select the marker for marker-relative times

In the Packet Viewer window, you can display times relative to a marker.

1 In the Packet Viewer Properties dialog's Column Properties tab, use the **Bus/Signal** selection to select the **Time** column.
2 For the **Base** property, select **Relative Marker**.
3 For the **Marker** property, select the marker to which relative times should be displayed.
4 Click **OK** to apply the changes and close the Packet Viewer Properties dialog.

To select fixed time units

In the Packet Viewer window, you can display time column values with a fixed unit.

1 In the Packet Viewer Properties dialog's Column Properties tab, use the **Bus/Signal** selection to select the **Time** column.
2 In the Time Column Properties box, check **Use Fixed Unit**; then, select the desired time unit from the drop-down list.
3 Click **OK** to apply the changes and close the Packet Viewer Properties dialog.

Analyzing the Same Data in Different Ways (Using the Overview Window)

The Overview window lets you specify how the data is sent from the logic analyzer data acquisition module to post-processing tools and display windows. For example, you can display the same data filtered in one Listing window and unfiltered in another Listing window.

To analyze the same data in different ways:

1. Open or display the Overview window.
2. Add new windows.

   If the Add New Window After dialog appears, select the module or tool that the new window should be placed after.
3. Add new tools.

   If the New Tool dialog appears, select where the new tool should be placed.

For more information on using the Overview window, see:

- To open or display the Overview window (see page 297)
- To add, duplicate, or delete windows and tools (see page 298)
- To edit window or tool properties (see page 300)
- To rename windows, tools, and modules (see page 301)
- To redraw the Overview window (see page 302)
- To delete the Overview window (see page 302)

See Also

- Overview Window (see page 440)
- Waveform Display Window (see page 427)
- Listing Display Window (see page 433)
- Compare Display Window (see page 436)
- Source Display Window (see page 437)
- "Filter/Colorize Tool" (in the online help)
- "Inverse Assembly Tools" (in the online help)
- "Bus Analysis Tools" (in the online help)
- "Tools" (in the online help)

To open or display the Overview window

- Select **Tools>Overview**.
- Select **Window>Overview**.

- If the Overview window is already open and you have Tabbed Windows (see page 305) turned on, you can display the Overview window by selecting the Overview tab at the bottom of the window.

See Also

- Analyzing the Same Data in Different Ways (Using the Overview Window) (see page 297)

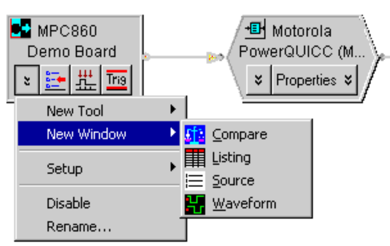
To add, duplicate, or delete windows and tools

You can add new listing and waveform display windows to the interface. As new windows are added, they appear in the list under **Window** in the menu bar. The active window will have a check mark. All available windows can be accessed either through the menu bar or through the use of tabs.

When you add a new tool to the logic analyzer's measurement configuration, its name appears at the bottom of the Tools menu. The tools interact with each other, so that you can progressively filter data or color parts of an inverse-assembled listing.

To add new windows

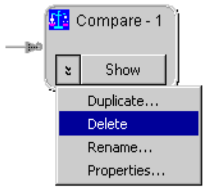
- From the menu bar, select **Window>New *type***....
- If the windows are tabbed, you can also right-click on the tab and select **Window>New *type***....
- In the Overview window, right-click in the background, and select **New Window** from the popup menu.
- In the Overview window, select **New Window** from a module or tool menu.



The new window is placed after the module or tool.

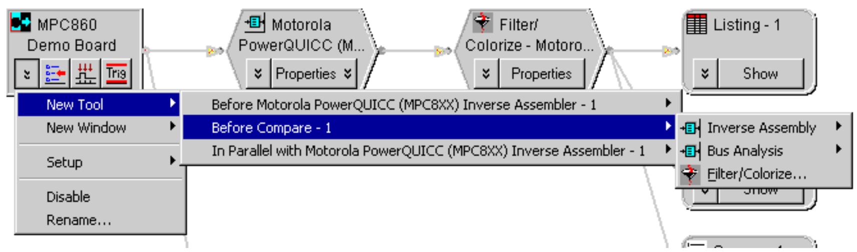
To delete windows

- From the window's menu in the menu bar, select **Delete**.
- If the windows are tabbed, you can right-click on the tab and select **Delete**.
- In the Overview window, select **Delete** from the window's menu.



To add new tools

- From the menu bar, select **Tools>New *type*...**.
- In the Overview window, right-click in the background, and select **New Tool** from the popup menu.
- In the Overview window, select **New Tool** from a module or tool menu.



The new tool is placed after the module or tool.

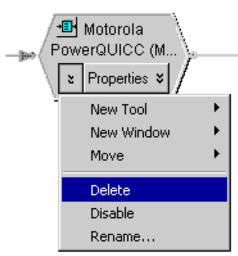
If the tool you want is not listed, make sure that you have "installed" (in the online help) and licensed (see page 313) the tool.

TIP

Many tools come with a configuration file. Loading the configuration file will add the tool, as well as set up the bus names, symbols, or filters used by the tool.

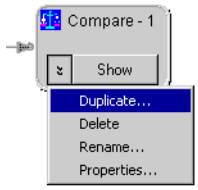
To delete tools

- In the Overview window, select **Delete** from the tool's menu.



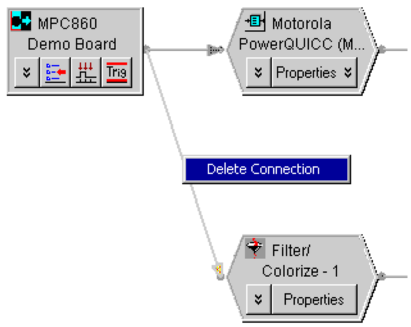
To duplicate windows

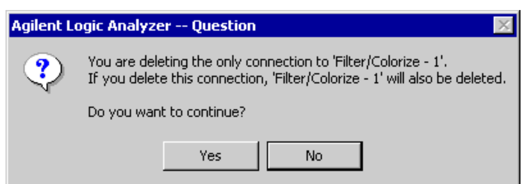
In the Overview window, you can duplicate windows from window menus. Duplicating a window is the same as adding a new window except that the new window has the same properties of the duplicated window.



To delete connections

1 In the Overview window, select the connection you wish to delete.
2 Select **Delete Connection**.





Deleting a connection has the effect of deleting the window or tool at the end of the connection.

To add connections There is no way to draw connections between modules, tools, and windows other than by adding new windows or tools. See: Connection Rules (see page 440).

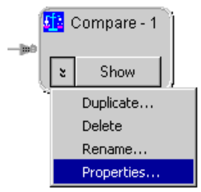
See Also

- Analyzing the Same Data in Different Ways (Using the Overview Window) (see page 297)
- To turn window tabs on/off (see page 305)

To edit window or tool properties

To edit window properties

- In the Overview window, select the **Properties...** command from the window menu.



Or, from the menu bar, select the **Properties...** command from the window's menu.

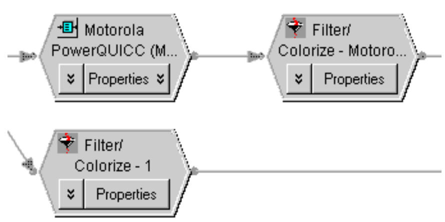
Or, right-click in the display window and select the **Properties...** command from the popup menu.

- In the window's properties dialog, make the desired changes.
- Select **OK** to apply the changes and close the dialog.

To edit tool properties

After adding a new tool such as a filter or inverse assembler, you can modify its properties as you refine your analysis of the data.

1 In the Overview window, click **Properties** on the tool.



Or, from the menu bar, select **Tools>*tool name***.

2 In the tool dialog box, change properties.

3 Select **OK** to apply the changes and close the box.

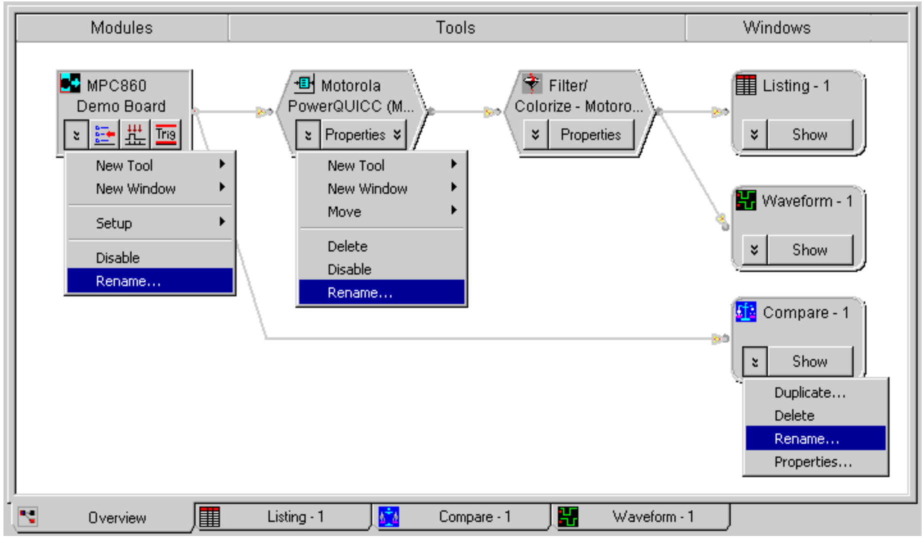
See Also

- Analyzing the Same Data in Different Ways (Using the Overview Window) (see page 297)
- To set waveform window properties (see page 213)
- To set listing window properties (see page 226)
- To set Compare window properties (see page 270)

To rename windows, tools, and modules

1 Display the Overview window.

2 Select the **Rename...** command from the window, tool, or module menu.



See Also

- Analyzing the Same Data in Different Ways (Using the Overview Window) (see page 297)

To redraw the Overview window

1 Display the Overview window.

2 Select the **Overview>Redraw** command, or:

Right-click in the Overview window and select **Redraw**.

See Also

- Analyzing the Same Data in Different Ways (Using the Overview Window) (see page 297)

To delete the Overview window

1 Display the Overview window.

2 Select the **Overview>Delete** command, or:

If Tabbed Windows (see page 305) are turned on, right-click the Overview tab and select **Delete**.

See Also

- Analyzing the Same Data in Different Ways (Using the Overview Window) (see page 297)

Setting the System Trigger and Skew Between Modules

When there are multiple *module* (see page 650)s in a logic analyzer or logic analysis system, there is a single *Time=0* point for all modules. If one module arms another, the second module has a trigger that is not at *Time=0* with respect to the first module. Because there is a single *Time=0* point, when you see one module captures an event at Time=-435 ns and another module captures an event at -835 ns, you know the two events occurred 400 ns apart.

This means one module's trigger reference point must be designated the *system trigger* (which is *Time=0*).

You can specify the skew between the *system trigger* and the trigger reference points of other modules. When two modules are looking at the same data, you may want to specify skew so that the waveforms from the two modules line up.

In all display windows, there are global, immovable trigger markers for each module. The marker for the *system trigger* has a special icon.

Each display window has its own *Beginning Of Data* and *End Of Data* markers based upon the buses and signals displayed in that window. For example, if Bus1 is acquired on Logic Analyzer-1 and Bus2 is acquired on Logic Analyzer-2 and both buses are included in Viewer1, then the *Beginning Of Data* will be the earliest sample in either Logic Analyzer-1 or Logic Analyzer-2, and the *End Of Data* will be the latest sample in either Logic Analyzer-1 or Logic Analyzer-2. If Viewer1 only contains buses from Logic Analyzer-1, then its beginning and end of data are only based upon Logic Analyzer-1.

To set the system trigger and skew between modules:

1 From the main menu, choose **Setup>Skew & System Trigger...**.
2 In the Module Skew and System Trigger dialog (see page 468), select the module whose trigger reference point is to be *Time=0* as the **System Trigger**.
3 To specify skew for other modules, enter the appropriate values in their **Skew** fields.
4 If you want the *system trigger* to be changed after the next run to the first module that triggers, check **First module to trigger designates the System Trigger**.
5 Click **OK**.

If a module is not the *system trigger*, the module icon in the Overview window is the standard logic analyzer icon:

When a module is designated the *system trigger*, an additional red "T" icon appears:

Using Display Windows

- To add or delete display windows (see page 305)
- To turn window tabs on/off (see page 305)

See Also
- To change the "Go to Trigger on Run" option (see page 168)

To add or delete display windows

You can add new listing and waveform display windows to the interface. As new windows are added, they appear in the list under **Window** in the menu bar. The active window will have a check mark. All available windows can be accessed either through the menu bar or through the use of tabs.

To add a new display windows

1 In the menu bar, click **Window>New Listing or New Waveform**. If the windows are tabbed, you can also right-click on the tab, then select New Listing or New Waveform.

To delete display windows

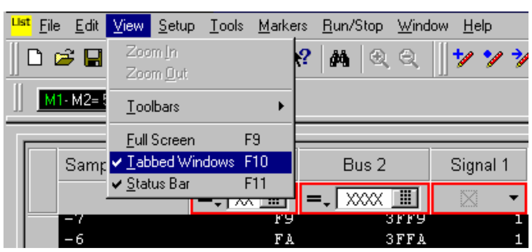
1 From the menu bar, click **Window>Close**. If windows are tabbed, you can also right-click on the tab, then select Close.

See Also
- To turn window tabs on/off (see page 305)

To turn window tabs on/off

By default, the Listing and Waveform display windows are tabbed for ease of switching between displays.

To turn on or off window tabs, select **View>Tabbed Windows**.



To switch display windows when tabs are turned off, you must select **Window>"*display window name*"**.

See Also
- To add or delete display windows (see page 305)

Printing Captured Data

There are three ways to create printed documentation of your measurement:

- To print captured data (see page 306)
- To copy text to the clip board (see page 307)
- To copy a screen to the clip board (see page 307)

See Also

- To install a printer (see page 307)
- To connect a LAN (see page 307)

To print captured data

1 From the menu bar, select **File>Print...**.

NOTE The first time you access the print dialog, you are asked to install a printer (see page 307). Follow the directions in the printer install dialogs that appear.

2 In the **Print What** section, select the desired display window.

3 To change the headers, footers, or margins, click **Options...** and specify the changes in the resulting dialog box. When you are done, click **OK**.

4 In the **Print range** section, select either:

- **All**
- **Time** range
- **Sample** range
- **Marker** range

If you selected **Time**, **Sample**, or **Marker**, set the desired range by entering or selecting the **from** and **to** values.

5 Click **OK** to print the specified data.

Data is printed from the smallest time/sample to the largest.

To print captured data to ASCII text files

Set up a generic/text only printer that prints to the "FILE:" port. In the Windows **Add Printer Wizard**:

1 Select a **Local** printer. (Do not automatically detect and install a plug and play printer.)

2 Select the **FILE:** port.

3 Select the **Generic** manufacturer and the **Generic / Text Only** printer model.

After you have set up the generic/text only printer, you can print captured data to it just like any other printer.

Note that you can also export captured data to CSV format ASCII text files (see page 172).

See Also

- To export data to CSV format files (see page 172)
- To install a printer (see page 307)

To copy text to the clip board

1. From the listing display area, position the mouse cursor over the upper-left corner of the desired display region.
2. Click and hold the left mouse button, then drag the mouse cursor to the lower-right corner. Release the mouse button. A rectangle is drawn around the defined region (snaps to state lines and bus/signal columns).
3. From the shortcut list that appears, click **Copy Text**.
4. Open a word processor or spreadsheet program, paste the text into the program, and print the pasted data text.

To copy a screen to the clip board

1. Click **Edit>Copy Screen**. The currently displayed window is copied into the windows clip board buffer.
2. Paste the contents of the clip board buffer into a graphics editing program of your choice.
3. Print the screen from the graphics program.

To install a printer

Local and network printers are installed outside of the logic analyzer environment using the Windows printer install wizard.

1. Click **Start>Settings>Printers**.
2. Click on an **existing printer**, or click **Add Printer**.
3. Follow the Windows printer install wizard instructions.

See Also

- To connect a LAN (see page 307)

To connect a LAN

Local area networks (LAN) are installed outside of the logic analyzer environment using the Windows network configuration wizard.

1. Click **Start>Settings>Network and Dial-up Connections**.
2. Click an **existing connection**, or click **Make New Connection**.

3 Follow the Windows network install wizard instructions.

See Also

- "*16900-Series Logic Analysis System Installation Guide*"
- "*16800-Series Logic Analyzers Installation/Quick Start Guide*"
- "*1680-Series Logic Analyzers Quick Start/Installation Guide*"
- "Changing the Windows XP Firewall Settings" (in the online help)
- Network Troubleshooting Guide (see page 355)

Extending Data Visualization/Analysis with VBA

With the integrated Microsoft Visual Basic for Applications (VBA), you can extend the data visualization and analysis capabilities of the logic analyzer. For example:

- You can graph captured data in the VbaView window. You can create:
  - Line graphs.
  - XY scattergrams.
  - Horizontal and vertical bar charts.
  - Stacked horizontal and vertical bar charts.
  - Pie charts.

  These charts are created in the VbaView window using the new VbaViewWindow and VbaViewChart COM automation objects.

  Bar charts let you create histograms of bus values which can be helpful in analyzing system performance.
- You can create macros that perform analysis and compute statistics on captured data. For example, to detect setup and hold problems, you could look at two edges throughout a trace, compute the delta time between them, list the average, minimum, and maximum delta times. You could also automatically place markers on unusual events.
- You can export captured data to external applications (like Microsoft Excel, Microsoft Access, the Agilent 89600 Vector Signal Analyzer, MathWorks MATLAB, etc.) for post-processing and analysis. Using the VbaView window, you can plot post-processed data on the logic analyzer.

See Also

- "Displaying Data in VbaView Windows" (in the online help)
- "Using the Advanced Customization Environment (ACE)" (in the online help)

8
Managing Software Licenses

- To view active software license information (see page 312)
- To activate software licenses (see page 313)
- To access floating license servers (see page 314)
- To borrow floating licenses and return them early (see page 316)

Starting with the 3.20 release of the *Agilent Logic Analyzer* application, you are able to order *floating* (also known as *counted*) licenses for tools and other add-in software. (Previously, all licenses were *node-locked*.)

NOTE

With the 3.20 release of the *Agilent Logic Analyzer* application, you had to set up the LM_LICENSE_FILE environment variable to access floating license servers. Starting with the 3.30 release, license servers are accessed from within the *Agilent Logic Analyzer* application, and you *must not* use the LM_LICENSE_FILE environment variable any more.

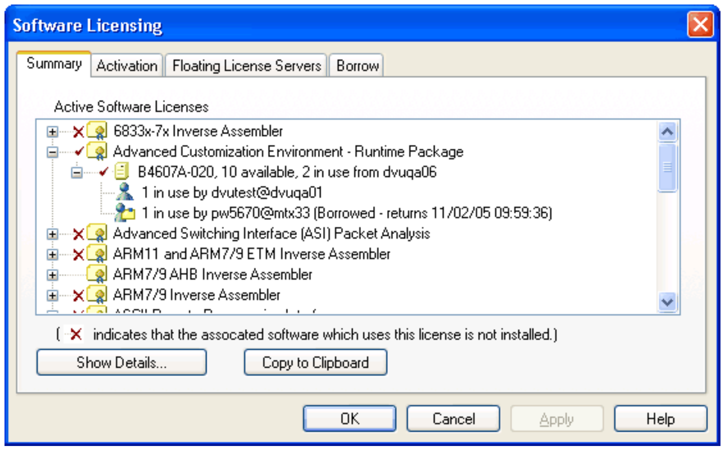
Before you can use floating licenses, you need to set up a license server.

See Also

- "*License Server Administration Guide*" for more information on setting up license servers for the Agilent 16900-series logic analysis systems and the 16800-series or 1680/1690-series logic analyzers.
- Software Licensing Dialog (see page 481)

To view active software license information

1 From the main menu, choose **Help>Software Licensing...**.
2 In the Software Licensing dialog's Summary tab (see page 482):



- You see all the software licenses that can be used.
- Red check marks show floating licenses that are already in use.
- Red "X"s show that software is not installed.
- You can select a license and click **Show Details...** to see detailed information about the license.
- You can copy all licensing summary information to the clip board.

NOTE When an "Advanced Customization Environment - Development Package" floating license is used, it is taken for the whole session. You must open a new configuration to return the license.

NOTE When an "ASCII Remote Programming Interface Package" floating license is used, it is taken for as long as the *Agilent Logic Analyzer* application runs. You must close the application to return the license.

See Also

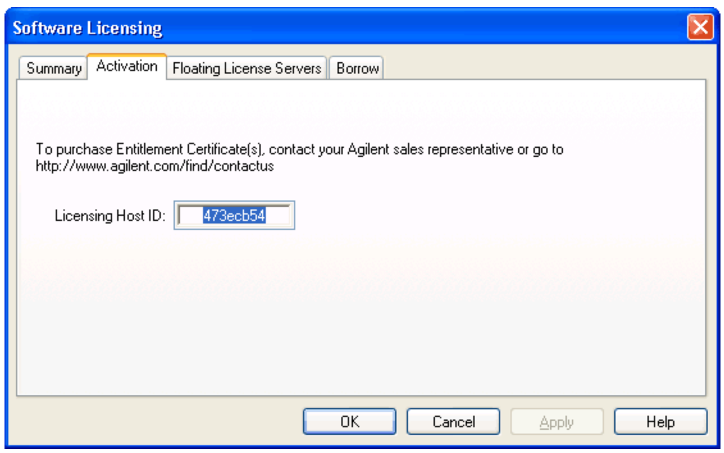
- To activate software licenses (see page 313)
- To access floating license servers (see page 314)
- To borrow floating licenses and return them early (see page 316)

To activate software licenses

1 Follow the instructions on the Entitlement Certificate you received with your software purchase.

2 From the *Agilent Logic Analyzer* application's main menu, choose **Help>Software Licensing...**.

3 In the Software Licensing dialog's Activation tab (see page 482), copy the **Licensing Host ID**. You will need this when activating licenses.



4 Visit the Agilent license redemption web site. The URL should be printed on the Entitlement Certificate.

The license redemption web site will use the order number or other license activation code which is printed on the certificate, along with the Licensing Host ID, to generate a license file. The license file will be e-mailed to you.

5 To install the license file and enable the software, follow the instructions in the e-mail that contains the license file.

Those instructions will tell you to install the license file in the proper directory on the logic analysis system or floating license server and restart the *Agilent Logic Analyzer* application or license server. On a logic analysis system, the license directory is usually "C:\Program Files\Agilent Technologies\Logic Analyzer\License\". For the proper directory on a license server, see the "*License Server Administration Guide*".

The license file must have a .lic extension.

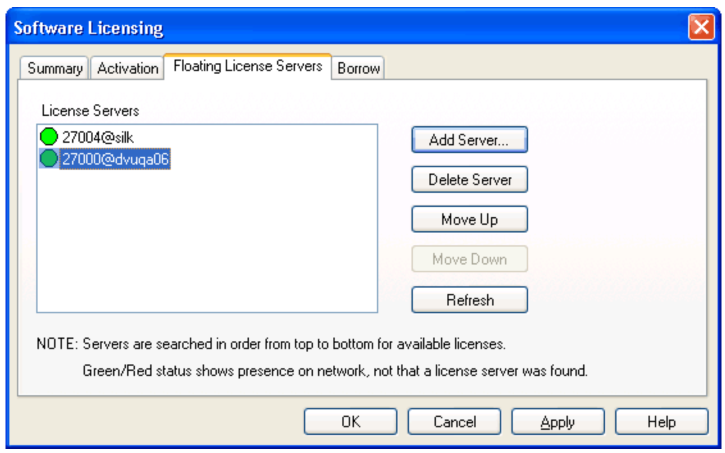
See Also

- To view active software license information (see page 312)
- To access floating license servers (see page 314)
- To borrow floating licenses and return them early (see page 316)

To access floating license servers

Before you can use floating licenses, you need to set up a license server (see "*License Server Administration Guide*").

1 Open the *Agilent Logic Analyzer* application (with the default configuration) so that no floating licenses are in use.
2 From the main menu, choose **Help>Software Licensing...**.
3 Select the Software Licensing dialog's Floating License Servers tab (see page 483).



To add a floating license server

1 Click **Add Server...**.
2 In the Add License Server dialog, enter the port number and name of the floating license server.

The port number is typically 27000, but it can be different depending on how the floating license server was set up.

CAUTION Only enter names of computers (or logic analyzers) that are floating license servers. Otherwise, the license manager interface hangs up for many minutes trying to determine if the computer is really a floating license server.

3 Click **OK** to close the Add License Server dialog.

4 In the Software Licensing dialog, click **Apply**.

To move a server up or down in the search order

1 In the License Servers list, select the license server you want to move.
2 Click **Move Up** or **Move Down**.
3 Click **Apply**.

To refresh floating license server status

1 Click **Refresh**.

The green or red server availability indicators are only a check of whether the computer is on the network, not of whether the license server software is running on that computer.

To delete a floating license server

1 In the License Servers list, select the license server you want to delete.
2 Click **Delete Server**.
3 Click **Apply**.

See Also

- "*License Server Administration Guide*"
- To view active software license information (see page 312)
- To activate software licenses (see page 313)
- To borrow floating licenses and return them early (see page 316)

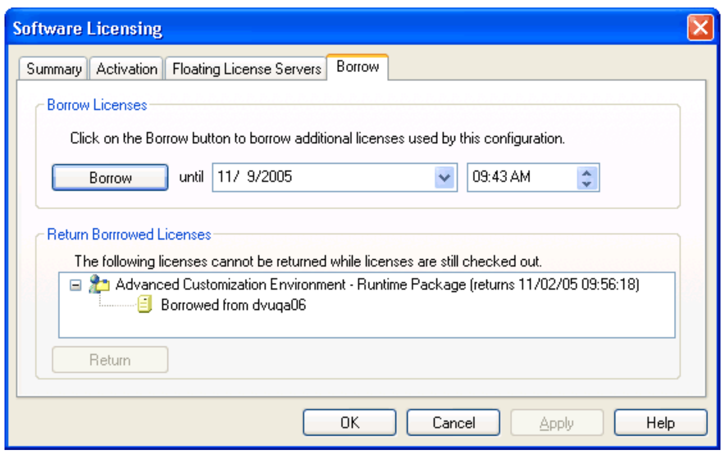
To borrow floating licenses and return them early

You can borrow floating licenses from a server for a period of time, for example, if you're taking a logic analyzer (or a computer running the *Agilent Logic Analyzer* application) out of the office (or just off the network). When a borrowed license's time expires, the license is automatically returned to the server. However, you can also return licenses early.

To access the Software Licensing dialog's Borrow tab

1 From the main menu, choose **Help>Software Licensing...**.

2 Select the Software Licensing dialog's Borrow tab (see page 484).



To borrow floating licenses

1 Set up the configuration (or open a configuration file) that uses the software you need to borrow licenses for.

2 Access the Software Licensing dialog's Borrow tab.

3 In the Borrow Licenses area, enter the date and time when the borrowed license will be returned.

The default time is seven days. The minimum time is ten minutes.

4 Click **Borrow**.

Repeat these steps to borrow additional licenses.

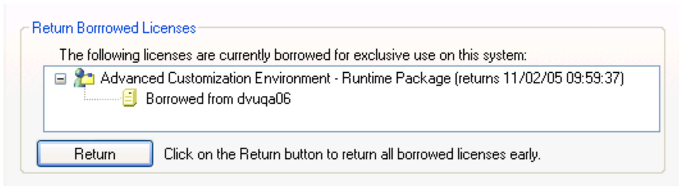
To return floating licenses early

When returning borrowed floating licenses early, all borrowed licenses must be returned. You are not able to return borrowed licenses while any licenses are checked out.

1 Open the *Agilent Logic Analyzer* application (with the default configuration).

2 Access the Software Licensing dialog's Borrow tab.

3 In the Return Borrowed Licenses area, click **Return**.



See Also

- To view active software license information (see page 312)
- To activate software licenses (see page 313)
- To access floating license servers (see page 314)

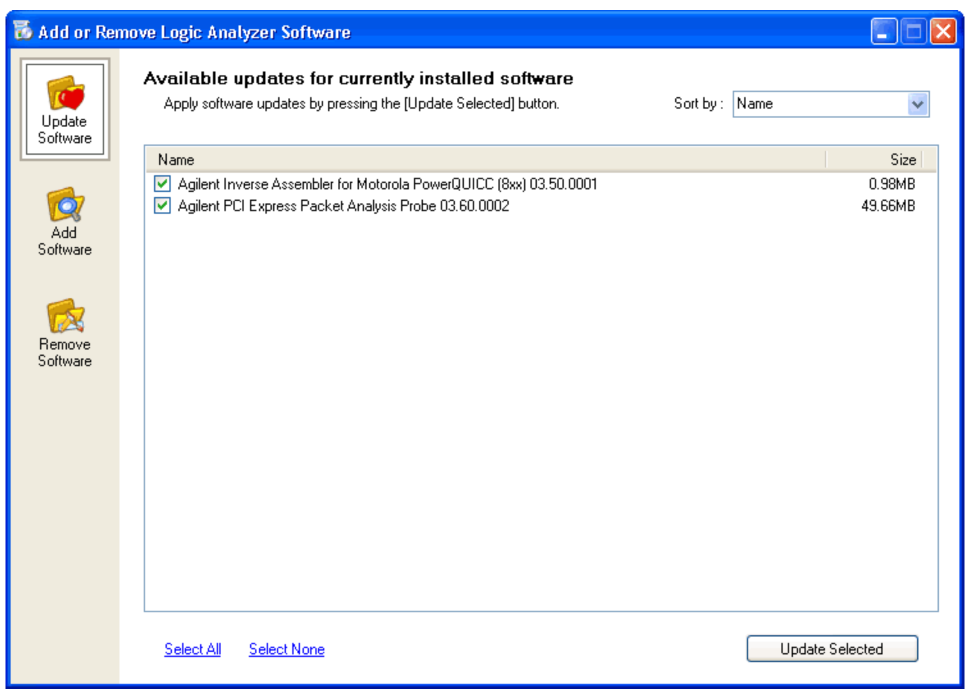
9
Updating Software

You may be able to install logic analyzer software from the logic analysis system's hard disk (depending on when it shipped from the factory or the application install CD that was last used).

To update, add, or remove logic analyzer software:

1 In the *Agilent Logic Analyzer* application, choose **Help>Software Update...**.

2 In the Add or Remove Agilent Logic Analyzer Software tool:



- To update software: click **Update Software** and select the software you want to update; then, click **Update Selected**.
- To add software: click **Add New Software** and select the software you want to add; then, click **Add Selected**.
- To remove software: click **Remove Software** and select the software you want to remove; then, click **Remove Selected**.

Note that you can select all software or none, and you can sort the software list by name, version, size, or date. When adding new software, you can show all versions or just the latest version.

See Also You can also download and install the latest versions of logic analyzer software from the Agilent web site:

- "http://www.agilent.com/find/la-sw-download"

10
Solving Problems

When troubleshooting problems or looking for more information, see:

- Software Installation Problems (see page 322)
- If starting in offline mode is unexpected (see page 323)
- If an ALA format configuration file won't open (see page 324)
- Interpreting Error Messages (see page 325)
- License Problems (see page 340)
- Translating Configuration Files from Other Logic Analyzers (see page 342)
- Running Self Tests (see page 345)
- Accessing Japanese Online Help (Windows XP) (see page 347)
- Accessing Japanese Online Help (Windows 2000) (see page 350)
- Network Troubleshooting Guide (see page 355)
- Remote Desktop Set Up (see page 358)
- If there are problems writing CDs on a 16900A, 16902A, or 16903A frame (see page 353)
- Hibernation Is Not Supported (see page 354)

See Also

- For More Information (see page 359)
- Intrinsic Support (see page 361)

- Agilent Logic Analyzer Readme

Software Installation Problems

Some problems that can occur when installing the *Agilent Logic Analyzer* application are:

- Installation Errors on 1680-Series Logic Analyzers (see page 322)

Installation Errors on 1680-Series Logic Analyzers

When installing the *Agilent Logic Analyzer* application on a 1680-series logic analyzer, a fragmented hard disk drive can cause installation errors; for example, the version of the acquisition card FPGAs can be reported too slowly, resulting in an error.

Try defragmenting the 1680-series logic analyzer disk and performing the installation again.

If starting in offline mode is unexpected

When starting the *Agilent Logic Analyzer* application on a logic analysis system or logic analyzer, you expect to connect to local hardware. If you have set up to auto-connect to a remote logic analysis system or logic analyzer, you expect to connect to the remote hardware. If the *Agilent Logic Analyzer* application starts in offline mode instead:

- It could be that the *Agilent Logic Analyzer* application is already running a local session. You can run multiple instances of the application, but if there's a local session is already running, additional instances start in offline mode.
- In the case of 1690-series logic analyzers (either local or remote), it could be:
  - Power to the logic analyzer is off.
  - An unplugged or loose IEEE 1394 cable.
  - A problem with the IEEE 1394 interface card in the personal computer.
- In the case where you have set up to auto-connect to a remote logic analysis system or logic analyzer, it could be:
  - The remote system is powered-down or off the network. In this case, you are given an information dialog about the system being offline before starting in offline mode.
  - The remote system is in the process of having its software updated.
  - The remote system software has been updated, resulting in an "incompatible remote service". In this case, make sure the same version of software is installed on the local computer or logic analysis system.

If an ALA format configuration file won't open

If an ALA format configuration file won't open because modules are incompatible (that is, not in the same or similar logic analyzer families like the 16740/41/42A and 16750/51/52A/B), you can still load the setup information from the ALA format configuration file:

1 Load the incompatible ALA format configuration file in offline mode.

  (If you're only interested in looking at the data, you can ignore the following steps.)

2 Save the configuration's setup information as an XML format configuration file (see To save a configuration file (see page 171)).

3 Go back online (see Returning to Online Analysis (see page 63)).

4 Open the XML format configuration file (see To open a configuration file (see page 184) and possibly To transfer module setups to/from multi-module systems (see page 188)).

5 Save the loaded setup information to an ALA format configuration file.

This procedure converts an incompatible ALA format configuration file into one that is compatible.

Interpreting Error Messages

To locate the error you received, use the help window's Search tab to search for key words in the error message.

- Error Messages (see page 325)
- Warning Messages (see page 336)
- Informational Messages (see page 338)
- Eye Finder Info Messages (see page 338)

See Also

- Solving Problems (see page 321)

Error Messages

- Acquisition Errors (see page 326)
- Bus/Signal Errors (see page 326)
- File Errors (see page 329)
- Hardware Errors (see page 329)
- Help File Errors (see page 330)
- Import/Export and Translator Errors (see page 330)
- Naming Errors (see page 332)
- Tool Errors (see page 333)
- Trigger Errors (see page 334)

See Also

- Interpreting Error Messages (see page 325)

Acquisition Errors

An acquisition error has occurred due to state clock edges occurring too close together. This could be the result of: - Poor state clock quality (signal integrity). - Inadequate probe grounding (try multiple grounds around clock signals). - State clock edges spaced closer than specifications allow. - Multiple clocks selected and spaced closer than specifications allow.

When in the state acquisition mode, the logic analyzer requires a clear clock signal no faster than the maximum state clock speed (see Specifications and Characteristics (see page 595)). Poor state clock quality may be caused by loading in the device under test. It may also be caused by a clock setup (see page 106) in the Sampling Setup dialog that is a combination of several signals which combined together violate the clock specification. When your clock setup uses multiple edges, the logic analyzer's setup/hold time typically increases (see Specifications and Characteristics (see page 595)). When you are using a clock speed near the specification, grounding every second or third probe connection is recommended.

Bus/Signal Errors

Maximum of 128 channels per Bus.

The logic analyzer cannot handle buses that contain more than 128 channels (signals). If you require wider buses, try breaking the bus into two or more buses, for example Data_HI and Data_LO.

Cannot group into Bus. Maximum of 128 channels per Bus.

The logic analyzer cannot handle buses that contain more than 128 channels (signals). If you require wider buses, try breaking the bus into two or more buses, for example Data_HI and Data_LO.

The following Bus/Signals are required to have a specific number of assigned channels because they are locked. Please correct the following Bus/Signals: *name* (has *num1* channels, requires *num2* channels)

Some tools may "lock" buses and signals that are necessary to produce their output. The locked buses and signals may have their specific channel assignments changed, but the total number of channels on each bus or signal must stay the same. Please change the channel assignment for each indicated bus or signal so that the width is *num2*. This message sometimes appears in combination with the next one. In these cases, you may have changed a configuration to use half the pods for sampling. Check the sampling tab.

Every Bus/Signal requires at least one assigned channel. Please assign channels to the following Bus/Signals:

Every bus or signal requires at least one channel. If you do not see the Bus/Signal named in the error dialog, try scrolling the Bus/Signal listing. Certain tools may also have created buses or signals within folders. If you are trying to avoid showing extra information on the viewer, delete the row (see page 211) or column (see page 225) the bus or signal is in. This removes the information from the viewer without losing the bus/signal setup information. This message sometimes appears in combination with the previous one. In these cases, you may have changed a configuration to use half the pods for sampling. Check the sampling tab.

Minimum of one Bus/Signal with assigned channels required. Please add a Bus/Signal.

The bus/signal setup cannot be closed because you have deleted all buses and signals. Folders only contain buses and signals, but do not represent data mappings of themselves. In order to close the dialog, select **Add Bus/Signal**. Assign at least one channel to the new bus or signal. Alternatively, you can select **Cancel** and revert to the previous bus and signal assignments.

name* is locked and cannot be deleted because it is required by another tool in the application. In order to unlock it, the following tools must be deleted: *tool

Some tools may "lock" buses and signals that are necessary to produce their output. Until the tool is deleted via **Tools>Overview**, you cannot delete or rename the bus or signal.

name* is locked and cannot be renamed because it is required by another tool in the application. In order to unlock it, the following tools must be deleted: *tool

Some tools may "lock" buses and signals that are necessary to produce their output. Until the tool is deleted via **Tools>Overview**, you cannot delete or rename the bus or signal.

Cannot change pod selection while there are locked Bus/Signals.

Some tools may "lock" buses and signals that are necessary to produce their output. Until the tool is deleted via **Tools>Overview**, you cannot modify the bus or signal by changing the pod in use.

Cannot delete *folder* because it contains one or more locked children.

Some tools may "lock" buses and signals that are necessary to produce their output. The folder you have tried to delete contains a unique copy of at least one locked bus or signal. You can move the locked buses or signals outside the folder, and then delete the folder. Alternatively, you can delete the tool locking the buses or signals via **Tools>Overview**, and then delete the folder.

Unable to set setup and hold times for this Bus/Signal since no channels have been assigned. Please assign channels before using setup and hold.

The possible valid range of setup and hold values depends on the clock setup used by the pods that the channels are attached to. Without knowing which pods' channels are part of the bus or signal, it is impossible for the logic analyzer to set appropriate ranges. Please assign channels to the bus or signal, and then set setup and hold.

Please enter a user threshold value.

All pods will be set to the same threshold value. If you select OK without setting a value, the current threshold values (at least one of which is different from the rest) are retained. Please check the dialog and be sure all fields are filled in.

Please enter a threshold value.

All pods will be set to the same threshold value. If you select OK without setting a value, the current threshold values (at least one of which is different from the rest) are retained. Please check the dialog and be sure all fields are filled in.

File Errors

Error trying to remove file: "*directory*/hardware_log.txt". When the logic analyzer is started up, it replaces the old hardware_log.txt file. For some reason, this time the old hardware log was not able to be deleted. This could indicate a problem with the disk that the file is stored on.

File "*filename*" could not be opened. When the logic analyzer is started up, it creates a new hardware_log.txt file. For some reason, this time the log was not able to be opened after creation. This could indicate a file system or disk problem.

Hardware Errors

Analyzer Calibration Failed [*time*] - Instrument may need service. The logic analyzer's pre-measurement calibration failed. Any data collected after receiving this error message is possibly incorrect. If the failure is transient, cycling power may fix the problem. If the failure is persistent, run **Help>Self Test...** or call your Agilent Sales Office to arrange for service.

High speed system clock failure - Instrument may need service. Sleep Duration and Count: *duration, counted*. The internal 100 MHz clock did not pass initialization tests. Any measurements are likely to be faulty. Please contact Agilent Technologies sales or support at "http://www.agilent.com/find/contactus" for information on getting the instrument repaired.

Contact with the analyzer hardware has been lost. This application will be terminated. You will have an opportunity to save your configuration. [1690A-series analyzers only] Something has interrupted the IEEE-1394 connection between the computer and the logic analyzer. Save your current work in a configuration (*.ala) file, then check the power to the logic analyzer hardware and the connections. A lost connection cannot be resumed; you will need to re-start the logic analyzer application.

I/O Channel Error: Invalid Request Argument. [1690A-series analyzers only] There is a problem with the data being sent via the IEEE-1394 connection.

I/O Channel Error: Offset Out of Bounds. [1690A-series analyzers only] There is a problem with the data being sent via the IEEE-1394 connection.

I/O Channel Error: Timeout. [1690A-series analyzers only] There is a problem with the data being sent via the IEEE-1394 connection.

I/O Channel Error: System I/O Error. [1690A-series analyzers only] There is a problem with the data being sent via the IEEE-1394 connection.

I/O Channel Error. [1690A-series analyzers only] There is an unspecified problem with the data being sent via the IEEE-1394 connection.

Help File Errors

Help file information was not found in the registry. You may need to reinstall the tool. The logic analyzer could not find a registry entry for the help file associated with the tool. If you have done a custom installation of the tool, you must also install the help file to access help. If the problem persists after re-installing, please contact Agilent Technologies sales or support at "http://www.agilent.com/find/contactus" for assistance.

Help file information not found in registry. Cannot display help. The logic analyzer could not find a registry entry for the help file associated with the tool. If you have done a custom installation of the tool, you must also install the help file to access help. If the problem persists after re-installing, please contact Agilent Technologies sales or support at "http://www.agilent.com/find/contactus" for assistance.

Help file not found. Cannot display help. The help file was not found where specified by the registry. It may have been deleted or moved. You can search the drive where the logic analyzer software is installed for .chm files, or re-install the tool.

The HTML Help file "*filename*" was not found. You may need to re-install the product. The help file was not found where specified by the registry. It may have been deleted or moved. You can search the drive where the logic analyzer software is installed for the file, or re-install. To re-install, close the logic analyzer application and run the setup program on the logic analyzer CD.

The HTML Help file "*filename*" was not found. You may need to re-install the tool. The help file for the tool was not found where specified by the registry. It may have been deleted or moved. You can search the drive where the logic analyzer software is installed for .chm files, or re-install the tool.

Import/Export and Translator Errors

Refer to the import files: *file1* and *file2* for more details. The configuration translator could not complete the translation. An explanation will be listed in *file1* or *file2* between "<!--" and ">" delimiters.

The specified file is NOT a 167xG Analyzer configuration file: *filename* The configuration translator was not able to translate the specified file because it was not in an understood format. The configuration translator only translates configuration files generated by 1670G, 1671G, 1672G, and 1673G logic analyzers.

Cannot read configuration file *filename*

The configuration translator was unable to read the configuration file indicated due to an internal error in the configuration file.

Cannot import an empty file. Import terminated.

The file you tried to import has no content.

Invalid non-ascii character read. Import terminated.

The logic analyzer only imports ASCII files. The file you tried to import contains a non-ascii character. You can edit the file in any text editing program, such as Notepad, to remove the character. Be careful to not change header data or the number of samples.

There are one or more locked bus/signals required by tool(s) currently loaded in the application. In order to unlock any of these bus/signals, you must unload every tool listed for that bus/signal. ... Import terminated.

Some tools may "lock" buses and signals that are necessary to produce their output. Until the tool is deleted via **Tools>Overview**, you cannot delete, rename, or modify the bus or signal. A side effect of this is that you cannot import a file that uses different buses and signals, or analyzer channel count.

There were fewer time data samples than indicated by the NumberOfSamples attribute of Module tag. Import terminated.

When you import a saved data file, the logic analyzer verifies that the data is consistent. To fix this error, you can edit the file in any text editing program, such as Notepad.

Syntax error in import file: *error*. Import terminated.

The error description indicates the syntax problem. Most often, it results from mismatched tags. Check the import file for any accidental deletions.

No bus/signals were valid for importing. Import terminated.

The import file was created on a logic analyzer model with more pod pairs than this one, and all the buses and signals were defined on pod pairs this model does not possess. You can attempt to modify the file by changing the assigned channels for the buses and signals. You can use any text editing program (such as Notepad) to edit import files. For more information on the format of import files, see "XML Format" (in the online help) .

Could not create file for export The logic analyzer was unable to create the file. Possible reasons include not enough disk space or insufficient permissions to create the file where indicated.

Could not find required *tag1* section contained within *tag2* section The import file is required to have a section with the heading *tag1* completely contained within the section delimited by <*tag2*> and </*tag2*>. You can repair the import file by adding <*tag1*></*tag1*> at the beginning of the *tag2* section. You can use any text editing program (such as Notepad) to edit import files. For more information on the format of import files, see "XML Format" (in the online help) .

Invalid or missing *attribute* in *tag* XML tag The import file requires the XML tag to include the keyword *attribute* and a value. For example, if *attribute* is Acquisition and *tag* is Sampling, the file has an XML tag of the form **<Sampling></Sampling>** but requires **<Sampling Acquisition="State"></Sampling>**. You can repair the import file by adding *attribute* to the specified tag and giving it a value. (Try exporting a similar configuration to see standard values.) You can use any text editing program (such as Notepad) to edit import files. For more information on the format of import files, see "XML Format" (in the online help) .

Invalid attribute value for attribute in *tag* XML tag The import file requires the XML tag to include the keyword *attribute* and a value. For example, if *attribute* is Acquisition and *tag* is Sampling, the file might have an XML tag of the form **<Sampling Acquisition="Time"></Sampling>** but requires **<Sampling Acquisition="Timing"></Sampling>**. You can repair the import file by editing the value. (Try exporting a similar configuration to see standard values.) You can use any text editing program (such as Notepad) to edit import files. For more information on the format of import files, see "XML Format" (in the online help) .

Naming Errors

The *object* name cannot be an empty string. When you rename a viewer, tool, or bus, you must give it a name at least one character in length. The blank or empty name you tried was not accepted by the logic analyzer.

***Object* name must be unique.** You have tried to rename a viewer, tool, or bus, but the name you entered is already being used and so was not accepted by the logic analyzer. You may appear to have identical names on some buses or signals, but these either are truncated or refer to the same bus (aliases).

The name "*toolname*" is already in use. Please choose a different name.

You have tried to rename a tool, but the name you selected is already in use. If you do not rename the tool, it will revert back to its previous name.

Tool Errors

For errors generated by specific inverse assemblers or bus analysis tools, go to the appropriate tool help.

Could not load the component - you may need to reinstall

This error occurs when there is a problem with the tool file. Possible reasons are the tool file was renamed, or permissions changed so that the logic analyzer cannot open it. To reinstall the tool file, close the logic analyzer and run the setup program on the logic analyzer CD.

Could not get license information for component

The logic analyzer attempted to determine if the tool was licensed or freely available, but could not find the information. Try re-installing the tool.

Could not obtain license information for component

This error means the logic analyzer is missing some information it needs in order to check the license. Licenses are created by the lmtools.exe program. You can run this to see what information is missing, and to check licenses.

Could not obtain a license for component

This error occurs when the license is not in the expected directory. When the tool is installed, the license is written into a predefined directory. Moving or deleting the file prevents you from using the component. If you do not believe the license was deleted, check your hard drive for *.lic files.

License for component is invalid

This error means that a license file exists, but that the information in it does not match. Licenses are specific to equipment; you cannot transfer a license for a tool or a logic analyzer between tools or logic analyzers.

Could not create licensed component

There was a valid license for the tool earlier in the install process, but something has gone wrong. Start the tool installation process over again. If this error persists, please contact Agilent Technologies sales or support at "http://www.agilent.com/find/contactus" for assistance.

Could not create component - unknown error

A license for the tool exists in the proper directory, but the internal information is inconsistent. Licenses are specific to equipment; you cannot transfer a license between tools or between logic analyzers. If this is a corrupt license, try reinstalling the tool again.

The stored tool could not be restored from file. The tool may have been uninstalled.

The configuration file you are trying to load includes a licensed tool. The logic analyzer was not able to find this tool, so some information will be missing. All buses and signals that were based on physical data will be loaded; buses and signals created by the tool will not.

The selected tool: *Name* could not be loaded.

The configuration file you are trying to load includes a licensed tool. The logic analyzer was not able to find this tool, so some information will be missing. All buses and signals that were based on physical data will be loaded; buses and signals created by the tool will not.

The selected tool could not be loaded.

The configuration file you are trying to load includes a licensed tool. The logic analyzer was not able to find this tool, so some information will be missing. All buses and signals that were based on physical data will be loaded; buses and signals created by the tool will not.

The tool could not be created - you may need to reinstall the tool.

The configuration file you are trying to load includes a licensed tool. The logic analyzer was not able to find this tool, so some information will be missing. All buses and signals that were based on physical data will be loaded; buses and signals created by the tool will not.

The analysis tool (*toolname*) could not be restored from the configuration file.

The configuration file you are trying to load includes a licensed tool. The logic analyzer was not able to find this tool, so some information will be missing. All buses and signals that were based on physical data will be loaded; buses and signals created by the tool will not.

Trigger Errors

Only one action per timer per branch is allowed.

A branch is the collection of actions after a "Then" in an Advanced Trigger step. Some steps, such as Advanced 2-Way Branch (see page 528), may have multiple branches. Within a branch, only one of Start from reset, Stop and reset, Pause, or Resume is allowed per timer. For more on timers, see To configure a timer (see page 140).

Only one action per counter per branch is allowed.

A branch is the collection of actions after a "Then" in an Advanced Trigger step. Some steps, such as Advanced 2-Way Branch (see page 528), may have multiple branches. Within a branch, you can not both Increment and Reset the same counter. You can increment one and reset the other. For more on counters, see To configure a counter (see page 141).

Only one store action per branch is allowed.

A branch is the collection of actions after a "Then" in an Advanced Trigger step. Some steps, such as Advanced 2-Way Branch (see page 528), may have multiple branches. Within a branch, you can set Store sample or Don't store sample but not both in the same branch. If you do not specify any store actions, default storage (see page 149) is used.

Only one reset occurrence counter action per branch is allowed.

A branch is the collection of actions after a "Then" in an Advanced Trigger step. Some steps, such as Advanced 2-Way Branch (see page 528), may have multiple branches. Within a branch, you can only specify Reset occurrence counter once.

No more edge resources available for this pod pair.

The logic analyzer hardware can only handle two edge statements per pod pair in *Full Channel Timing Mode* (see page 573) or *Half Channel Timing Mode* (see page 573), or one edge statement per pod pair in *Transitional / Store Qualified Timing Mode* (see page 573). If the edges are on different signals, try probing one of the signals with another channel on another pod pair. If all the edges are being used on the same signal, replace the "either edge" terms with "rising edge OR falling edge". See To insert events (see page 155) for how to replace "either edge".

No more pattern resources available for this pod pair

The logic analyzer hardware has a limited number of pattern (bus value) variables per pod pair. If the values you are checking for are on different buses, try probing one of the buses with another pod pair.

Branch expression is too complex

The expression in one of the branches of the trigger specification is too complicated for the logic analyzer. The logic analyzer first combines all AND terms and then ORs the expressions together. AND terms that have more than 4 events use twice the resources. Try rewriting the branch expression to use more OR terms, or delete some events.

One situation that leads to this error is using the **In Range** and **Not In Range** operators with buses that span more than 2 pod pairs. These operators are limited to buses that span 2 or fewer pod pairs (up to 64 bits wide).

Trigger Specification is too complex

Although no single branch expression is too complex, the total number of ANDs and ORs has exceeded the logic analyzer's resources. Try simplifying some expressions in some steps, or removing steps altogether.

Replacement failed. Maximum number of sequence steps exceeded.

The logic analyzer translates the trigger you specified into internal sequence steps. Different trigger functions use different numbers of internal sequence steps. Also, the "trigger and fill memory" action requires an additional internal sequence step each time it is used in state acquisition mode. One possible way to simplify the trigger specification is to replace all other "trigger and fill memory" actions with a "goto N" action that points to a "Find anything then trigger and fill memory" step.

Unable to insert step. The maximum number of sequence steps are already allocated.

The logic analyzer translates the trigger you specified into internal sequence steps. Different trigger functions use different numbers of internal sequence steps. Also, the "trigger and fill memory" action requires an additional internal sequence step each time it is used in state acquisition mode. One possible way to simplify the trigger specification is to replace all other "trigger and fill memory" actions with a "goto N" action that points to a "Find anything then trigger and fill memory" step.

Too many sequence steps.

The logic analyzer translates the trigger you specified into internal sequence steps. Different trigger functions use different numbers of internal sequence steps. Also, the "trigger and fill memory" action requires an additional internal sequence step each time it is used in state acquisition mode. One possible way to simplify the trigger specification is to replace all other "trigger and fill memory" actions with a "goto N" action that points to a "Find anything then trigger and fill memory" step.

Goto action specifies an undefined step.

The last step in the trigger sequence includes the action "Goto next". Because there is no next step, the logic analyzer cannot run and look for a trigger. Select **Setup>(Logic Analyzer Module)>Advanced Trigger...**, and change the action for the last trigger step.

Counter event specified both true and false in the same product term

In the trigger specification, at least one branch ANDs together "bus equals X" and "bus not equal X". Because this condition can never be true, the logic analyzer will not trigger and does not start the acquisition. If you intend to have it run until you press stop, use the trigger function Run Until User Stop, found under the "Other" tab in advanced trigger.

Cannot use <, <=, >, >= for a bus with clock bits that spans pod pairs

You have defined a bus that both spans pod pairs and includes a clock bit. The clock bits are numbered the same as the pod they are located on, and it is possible for them to be the channel that is not on the same pod pair as the others. Check the channel assignment in the Buses/Signals (see page 448) tab of the Setup dialog. The logic analyzer will not run until this problem is corrected.

Cannot specify a range on a bus with clocks bits that spans pod pairs

You have defined a bus that both spans pod pairs and includes a clock bit. The clock bits are numbered the same as the pod they are located on, and it is possible for them to be the channel that is not on the same pod pair as the others. Check the channel assignment in the Buses/Signals (see page 448) tab of the Setup dialog. The logic analyzer will not run until this problem is corrected.

Warning Messages

You are currently running "Offline," so running the analyzer is not possible. If you wish to create "fake" data while offline, go to "Edit -> Options" and select "Create Data When Offline". Note: This setting is persistent from session to session.

The logic analyzer is running in offline mode. Offline mode means that the logic analyzer software does not have access to logic analyzer or logic analysis system hardware. If you have a logic analyzer attached, please check the connection. For more on running with fake data, see Options Dialog (see page 470). Fake data is useful when learning how to use the logic analyzer software.

This module is already being used by another instance of the application. You are now working Offline.

The logic analyzer hardware is attached to an open instance of the logic analyzer software. If you need to acquire data, locate that instance from the Windows taskbar. The Local/Remote/Offline indicator is at the bottom of the application window. In offline mode, the software can still work with saved data.

Event specified both true and false in the same product term

In the Advanced Trigger dialog, one of the branches for one of the steps checks that an event is both true and not true. An event may be a bus or signal equal to a value, a timer expiring, or a count exceeding some value. Because of the AND combination, the branch cannot be true. You may want to modify the trigger to use either an OR combination of the events, or separate them into different branches or steps. For more on constructing complex triggers, see To replace or insert trigger functions into trigger sequence steps (see page 143). For more on how to interpret the trigger sequence, see Reading Event and Action Statements (see page 139).

Timer *n* value checked as an event, but no start action specified.

In the Advanced Trigger dialog, the trigger sequence checks the value of a timer that was never started. Timers need to be explicitly started in a previous trigger step. See To configure a timer (see page 140) for more information.

Counter *n* value checked as an event, but no increment action specified.

In the Advanced Trigger dialog, the trigger sequence checks the value of a counter that is never incremented. Counters need to be incremented in the action statements of a trigger step. See To configure a counter (see page 141) for more information.

The Bus/Signals listed below could not be loaded from the configuration file. Please recheck your Trigger since it may have changed.

The configuration file you just loaded was created on a logic analyzer with more pods than this model. Because of this, some buses and signals which rely on the additional pods could not be loaded. If these buses or signals were used in the trigger sequence, the trigger sequence will have changed. You may be able to work around this by assigning different channels to the affected buses and signals, and re-creating the trigger sequence.

Slow or missing clock in Trigger Step *n*...

The logic analyzer is not able to detect the state clock, and is therefore unable to take samples and evaluate the trigger sequence. If your device under test's clock is bursty, this may be expected behavior. If it is not, please check all probing connections. To verify the clock signal is being received, you can assign the clock channels to a bus in timing acquisition mode and acquire data.

Informational Messages

Filling memory after trigger... The logic analyzer has triggered and is filling memory. Due to either a slow clock or storage qualification in state acquisition mode, or infrequent transitions in transitions-only timing acquisition mode, the logic analyzer is taking enough time to fill memory that this message is showing.

Trigger inhibited during prestore... The logic analyzer is in timing acquisition mode. In timing acquisition mode, the logic analyzer fills the designated amount of memory before searching for the trigger. If this message is showing, the logic analyzer is filling memory and has not yet begun to compare data to the trigger sequence. To capture triggers that happen during the beginning of a device under test's boot sequence, be sure to set the trigger position in the Sampling tab to 100% poststore.

Waiting in Trigger Step *n* The logic analyzer is waiting for a sample that matches the events defined in step *n* of the trigger sequence. Sometimes the event is rare, causing long waits. If you feel that the logic analyzer should have triggered already, check the trigger sequence in Advanced Trigger. For more on triggering, see Specifying Advanced Triggers (see page 138).

Eye Finder Info Messages

These messages appear in the Thresholds and Sample Positions dialog (see page 497) after an *eye finder* measurement is run.

"Clock signal in Fast State Mode is divided by two." This message only appears with 16753/54/55/56 and 16950 logic analyzers.

"Demo: Results will not be used for analysis." This channel was measured when "Demo Mode (no probes required)" was selected in the Run Mode tab of the Eye Finder Advanced Options dialog (see page 500). The data shown are typical of *eye finder* operation, but the sample position setting shown is NOT used. (The manual setting is still in use.)

"No signal activity. Check connection, threshold, and stimulus." This channel appears to be completely quiet.

- Check the probe connection between the analyzer and the device under test.
- Check the threshold voltage setting (see Setting the Logic Analyzer Threshold Voltage (see page 80)).
- Check that the device under test is turned on and is running the appropriate diagnostic or other stimulus program.

If all these things are set up correctly, activity will be shown in the Analyzer Setup dialog's Buses/Signals tab (see page 448).

"No stable regions. Check clock and thresholds."

Two common possibilities exist:

1 The signal on this channel is asynchronous to the clock defined for the logic analyzer. If this is the case, there is no stable relationship between the times when the signal switches and when the clock arrives.

   If you expect the signal to be sampled synchronously you must redefine the clock for this signal.

2 The stable region(s) are too small for *eye finder* to detect.

   In this case you must resort to adjusting the sample position manually and checking its validity by running an ordinary analyzer measurement to see if the data values you expect are sampled. You can adjust the sample position manually by selecting the arrow buttons or by dragging the blue sampling position indicator in the display.

"No voltage scan: Channel in pod with assigned clock."

"One or more stable regions found."

"Only a few transitions detected. Change stimulus or increase measurement duration."

The signal on this channel was observed to toggle fewer than 500 times. The characterization may be accepted as it stands or you may wish to change the stimulus program or diagnostic in the device under test to increase the toggle rate.

Another option is to select "Long" in the Measurement Duration tab of the Eye Finder Advanced Options dialog (see page 500). Using the "Long" setting won't necessarily make the message go away, but it will ensure that *eye finder* has the opportunity to observe a more significant number of transitions on the channel.

"Stable region at N ns is an estimate."

This message only appears for certain bus probes (not general purpose probes).

"The stable region extends beyond the limits of the display."

This channel is active, but the signal does not switch within 5 ns before or after the clock. For example, this could occur if the propagation delay in the device under test from clock to data is greater than 5 ns and the clock period is greater than 10 ns (slower than 100 MHz).

License Problems

Some problems that can occur with licenses are:

- License Not Available (see page 340)
- Floating License Server Communication Timeout (see page 340)

License Not Available

If you attempt to use a software feature that requires a license, and a license is not available, the License Not Available dialog appears.

Depending on the situation, there are several ways to solve this problem:

- If all licenses are in use, you can wait until one of them becomes available again. If there is only one license, the License Not Available dialog shows you who is using the license. If there are multiple licenses, you can view the active software license information (see page 312) to see the license users.
- If all licenses are in use or there are no licenses, you may be able to get a license from another license server (see To access floating license servers (see page 314)).
- If the license management software detects that one of your license servers is unavailable, make sure the computer or logic analyzer hosting the license server is running, is accessible over the network, and is running the license service. For more information, see the "*License Server Administration Guide*".
- If an expected node-locked license is not found, make sure the license file is located in the "License" subdirectory under the installation directory (typically C:\Program Files\Agilent Technologies\Logic Analyzer), and make sure the license file has the .lic extension.
- If you decide to purchase additional licenses, contact Agilent Technologies (see "http://www.agilent.com/find/contactus"). When you get your Entitlement Certificate, activate your licenses by using the License Activation Wizard (see To activate software licenses (see page 313)).

See Also

- Managing Software Licenses (see page 311)

Floating License Server Communication Timeout

When floating licenses are used, the license subsystem checks for communication with the license server every two minutes.

After 10 minutes of communication loss (6 checks), licenses are considered lost, and you are given a message about the server that is no longer communicating and the features that are disabled.

Depending on the feature, you may be able to continue working in the *Agilent Logic Analyzer* application, or you may be forced to exit the application. In either case, you are able to save your setup and data to a configuration file.

If you are able to continue using the *Agilent Logic Analyzer* application with disabled features, the communication checks continue every two minutes. If communication with the license server is re-established, an information dialog tells you about the server and features that have been re-enabled.

When communication with a floating license server is lost, make sure the computer or logic analyzer hosting the license server is running, is accessible over the network, and is running the license service. For more information, see the "*License Server Administration Guide*".

Translating Configuration Files from Other Logic Analyzers

Included with the *Agilent Logic Analyzer* application are utilities for translating configuration files from 167xG and 16700-series logic analyzers. These configuration file translators move setup information from other logic analyzer configuration files into generic XML format configuration files that can be loaded into the *Agilent Logic Analyzer* application.

The configuration file translators can be run without any logic analyzer hardware.

NOTE Only setup information is translated, not saved data.

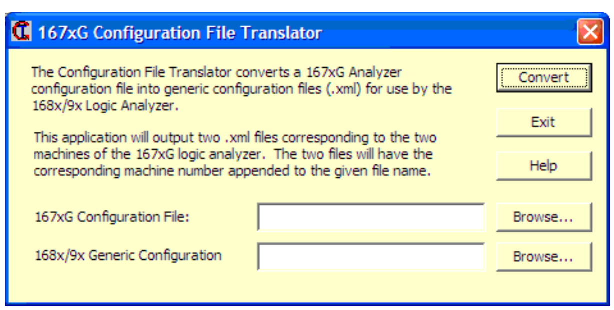
- To translate 167xG logic analyzer configuration files (see page 342)
- To translate 16700-series logic analyzer configuration files (see page 343)

See Also

- "XML Format" (in the online help)
- To open a configuration file (see page 184)

To translate 167xG logic analyzer configuration files

1. From the Windows Start menu, choose **Start>All Programs>Agilent Logic Analyzer>Utilities>167xG Configuration File Translator**.
2. In the 167xG Configuration File Translator dialog, enter the name of the 167xG configuration file you want to translate.



NOTE 167xG configuration files end in ._A, but this suffix is also used by other models. If possible, confirm that it has a file type of 167xdn_config when viewed on a 1670-series logic analyzer.

3. Type in the name you want to save the new configuration files under.

- Because the 1670-series logic analyzers split resources between two measurement engines by default, two output files are created. The default filename is the same as the 167xG configuration file, but has 1.txt or 2.txt appended. Both files are created even if the configuration only used one of the measurement engines.
- Files are saved in the same directory as the input file unless otherwise specified.
- The output files are in XML format, and can be opened like other XML configuration files.

4 Click **Convert**.

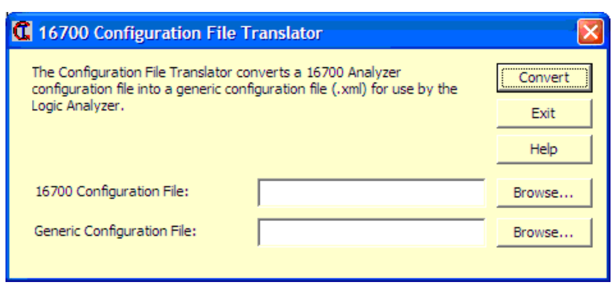
Information not converted from file:

- In timing acquisition mode, the sampling period and sampling option.
- In state acquisition mode, the clock mode and clock description.
- All data.
- Any tool information.
- Interface layout.
- Marker information.

To translate 16700-series logic analyzer configuration files

1 From the Windows Start menu, choose **Start>All Programs>Agilent Logic Analyzer>Utilities>167xx Configuration File Translator**.

2 In the 16700 Configuration File Translator dialog, enter the name of the 16700 configuration file you want to translate.



When you have a 16700-series logic analysis system with modules in slots B and C, you get three files when you save a configuration: an xxx.__B, xxx.__C, and xxx.___. Of these three files, only the xxx.__B and xxx.__C can be translated into XML. The xxx.___ cannot be translated.

3 Type in the name you want to save the new configuration files under.

- Files are saved in the same directory as the input file unless otherwise specified.

- The output files are in XML format, and can be opened like other XML configuration files.

4 Click **Convert**.

Information not converted from file:

- All data.
- Any tool information.
- Interface layout.
- Marker information.

To translate multi-module configurations

For example, if you have a 16700-series logic analysis system with modules in slots B and C:

1 On the 16700-series logic analysis system, save the configuration to file "setup1". This generates files setup1.__B, setup1.__C and setup1.___.

(The setup1.__B and setup1.__C files each contain the setup for a single module. In order to translate the entire two-module configuration, you need to translate both files.)

2 Copy the setup1.__B and setup1.__C files to the logic analyzer or personal computer on which the *Agilent Logic Analyzer* application runs. (You can ignore the setup1.___ file.)

3 Use the configuration file translator (as described above) on setup1.__B and setup1.__C to generate the files setup1B.XML and setup1C.XML.

4 In the *Agilent Logic Analyzer* application, open the setup1B.XML file. When asked "Do you want to clear all modules before loading?", click **Yes**.

5 Open the setup1C.XML file. When asked "Do you want to clear all modules before loading?", click **No**.

In general, clear all modules when loading the first XML file, and do not clear all modules when loading subsequent XML files.

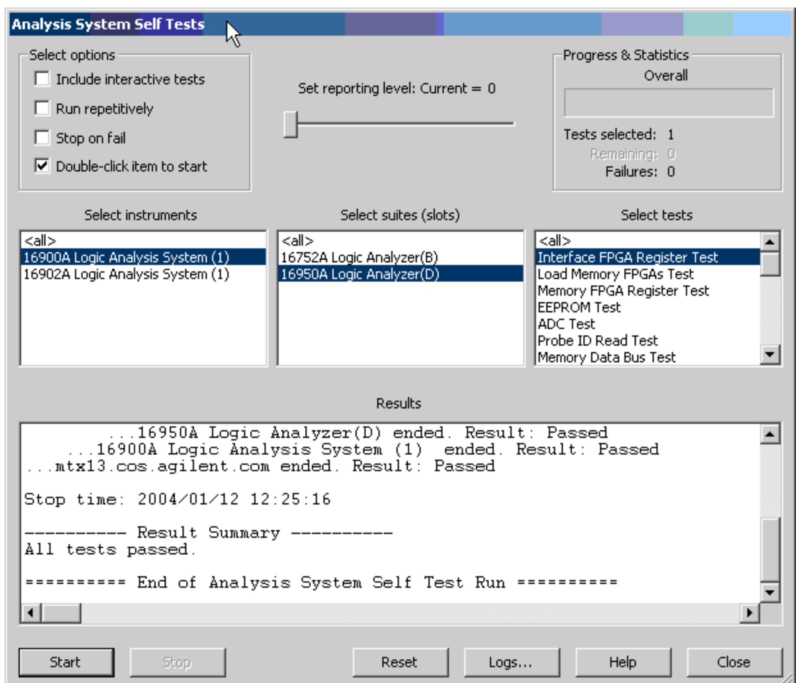
Running Self Tests

The Self Test menu checks the major hardware functions of the logic analysis system to verify that it is working correctly.

CAUTION Because the most recently acquired data will be lost, be sure to save important data before running self tests.

1 From the menu bar select **Help>Self Test...**.

If you have acquired data, a warning message appears, "Running self-tests will invalidate acquired data"; click **OK** to continue.



2 In the Analysis System Self Tests dialog, select the self test options:

- **Include interactive tests** — causes interactive tests to appear in the selection lists.
- **Run repetitively** — runs the selected tests repetitively until you click **Stop**.
- **Stop on fail** — if you are running multiple tests or running tests repetitively, this causes the tests to stop if there is a failure.
- **Double-click item to start** — lets you double-click a test to start it.

3 Set the reporting level.

Higher levels produce increasingly verbose output.

4 If you have a multiframe configuration, select the instruments you want to test.

5 If you have a slotted instrument, select the suites you want to run.

6 Select the tests you want to run.

7 Click **Start**.

   As the tests are running, the results are reported in the lower part of the dialog and saved to a log file.

   To stop running test, click **Stop**.

   To reset the self-test options, click **Reset**.

   To view the log file, click **Logs...**, select the log file you want to view, and click **Open**.

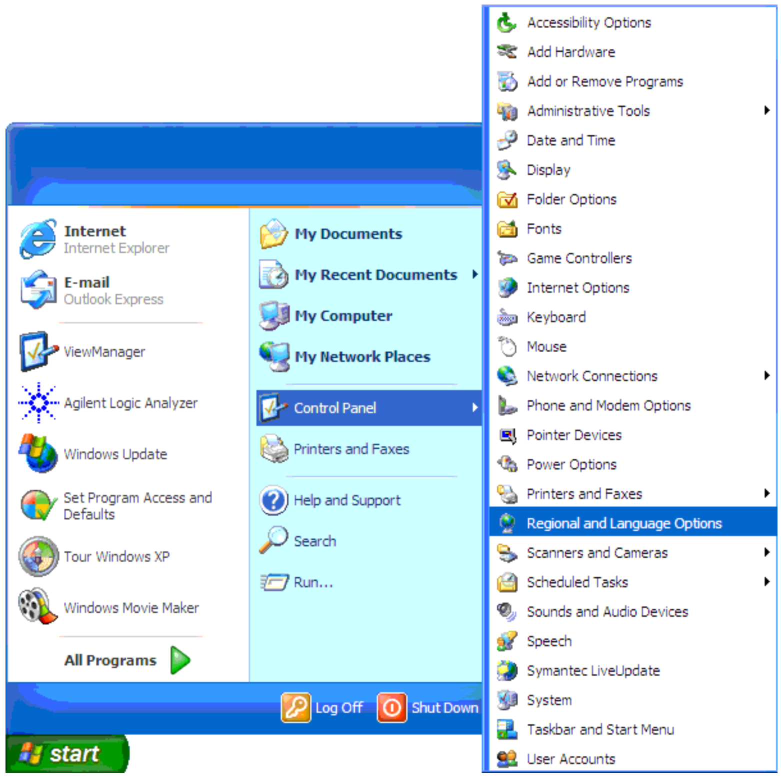
If, after completing the self tests, you have failures or you have questions about the performance of the logic analysis system, contact Agilent Technologies sales or support at "http://www.agilent.com/find/contactus".

See Also

- For More Information (see page 359)

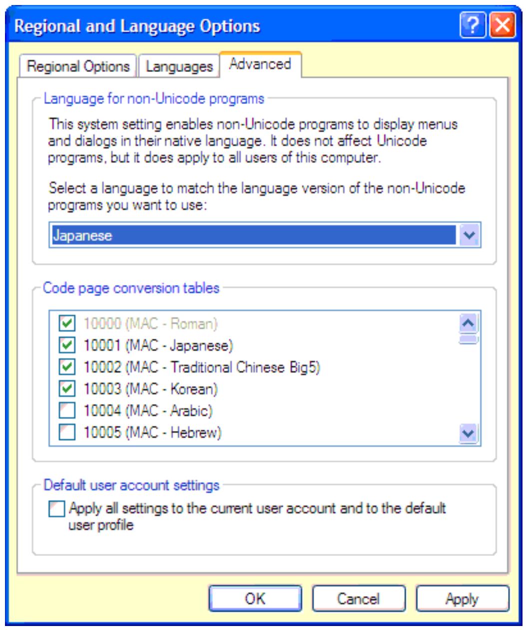
Accessing Japanese Online Help (Windows XP)

1 From the Windows Start menu, choose **Start>Control Panel>Regional and Language Options**.



2 In the Advanced tab of the Regional and Language Options dialog:

a In the "Language for non-Unicode programs" box, select **Japanese**.



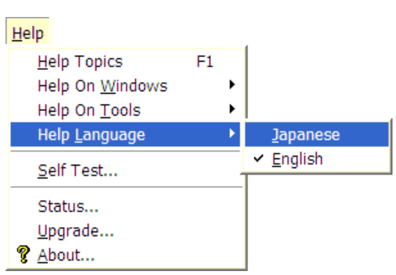
b Click **OK** to close the Regional and Language Options dialog.

3 In the dialog that appears, select the files to copy:

- On a logic analyzer or logic analysis system, the dialog asks if you would like to use existing files or recopy files from the Windows CD-ROM; click **Yes** to use the existing files.
- On a personal computer running the *Agilent Logic Analyzer* application for a 1690-series logic analyzer, offline analysis, or remote connection to a logic analysis system, you may have to copy files from your Windows CD-ROM.

4 A dialog appears asking if you would like to restart your computer; click **Yes** to restart your computer.

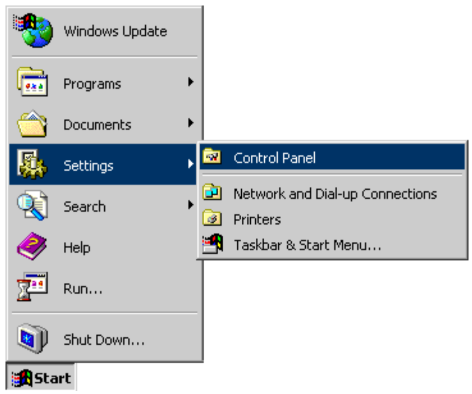
5 After your computer restarts, start the *Agilent Logic Analyzer* application, and choose **Help>Help Language>Japanese**.



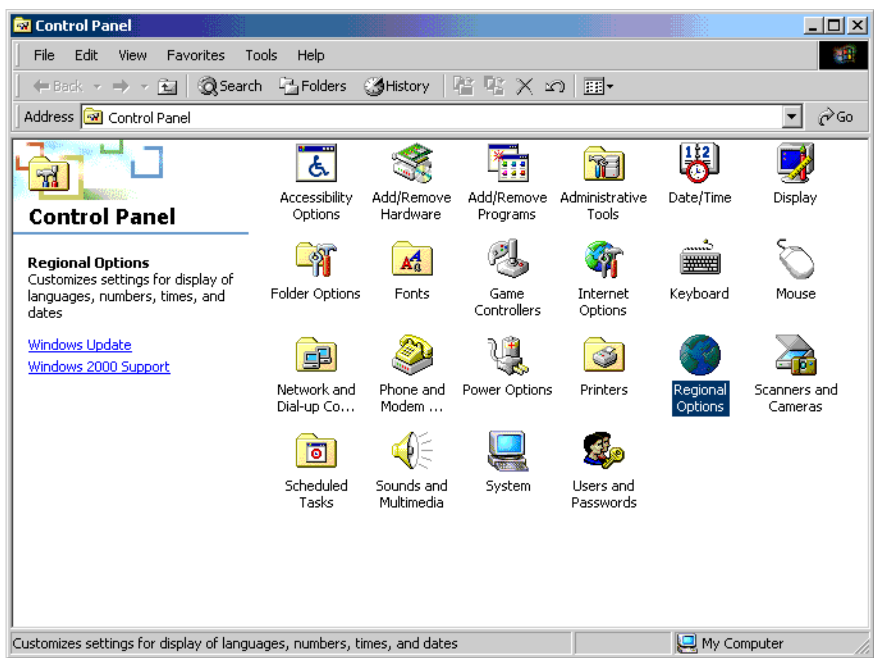
Now, when you access the online help, you get the Japanese version.

Accessing Japanese Online Help (Windows 2000)

1 From the Windows Start menu, choose **Start>Settings>Control Panel**.

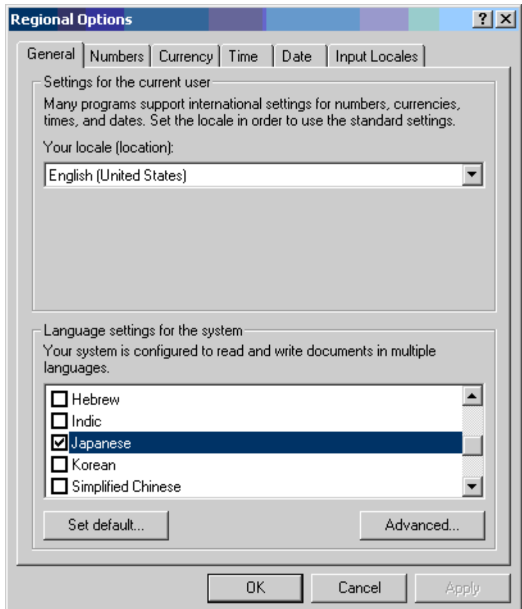


2 In the Control Panel window, double-click **Regional Options**.



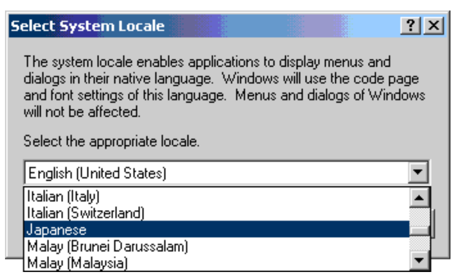
3 In the Regional Options dialog:

a In the "Language settings for the system" box, select **Japanese**.



b Click **Set default...**.

c In the Select System Locale dialog, select **Japanese**.



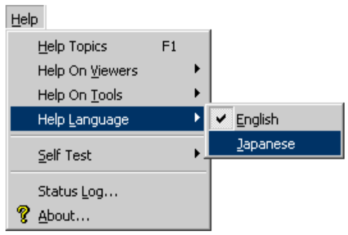
d Click **OK** to close the Regional Options dialog.

4 In the dialog that appears, select the files to copy:

- On a logic analyzer or logic analysis system, the dialog asks if you would like to use existing files or recopy files from the Windows CD-ROM; click **Yes** to use the existing files.
- On a personal computer running the *Agilent Logic Analyzer* application for a 1690-series logic analyzer, offline analysis, or remote connection to a logic analysis system, you may have to copy files from your Windows CD-ROM.

5 A dialog appears asking if you would like to restart your computer; click **Yes** to restart your computer.

6 After your computer restarts, start the *Agilent Logic Analyzer* application, and choose **Help>Help Language>Japanese**.



Now, when you access the online help, you get the Japanese version.

If there are problems writing CDs on a 16900A, 16902A, or 16903A frame

CAUTION When writing to a 16900A, 16902A, or 16903A logic analysis system's DVD-ROM & CD-R/RW combination drive, the logic analysis system must be oriented horizontally; otherwise, the resulting CD-R/RW disc may not be readable on *any* CD-ROM drive.

The 16900A, 16902A, or 16903A logic analysis system's DVD-ROM & CD-R/RW combination drive supports:

- 24x speed CD-R writing.
- 24x speed CD-RW writing.
- 24x speed CD-ROM reading.
- 8x speed DVD-ROM reading.
- Can read DVD-RAM, DVD-R, and DVD-RW.

And it supports the following writing methods:

- Disc at Once.
- Session at Once.
- Track at Once.
- Multi-Session.
- Fixed/Variable Packet Writing.

Hibernation Is Not Supported

No standalone Agilent logic analysis system supports Windows *hibernation* power state.

Power management is controlled through the "Power Options" icon under the control panel. In the "Power Options" dialogs you will find a tab entitled, "Hibernate." Within this window is a check box that lets you turn on/off hibernation. Please do not check this box. The logic analysis system ships from the factory with hibernation disabled.

If you enable hibernation and the logic analysis system attempts to enter hibernation when the *Agilent Logic Analyzer* application is installed, Windows will produce a dialog stating something like the following:

> "The device driver for the 'Agilent 16800/16900 Logic Analyzer' device is preventing the machine from entering hibernation. Please close all applications and try again. If the problem persists, you may need to update this driver."

Please note that this message only indicates that the logic analysis system does not support hibernation—not that there is something wrong with the software or drivers.

Network Troubleshooting Guide

Network Setup

For information on setting up 16900-series logic analysis systems on the network (and in multiframe configurations), refer to the "*16900-Series Logic Analysis System Installation Guide*".

- Is the logic analysis system registered with DNS?
- Is the logic analysis system registered with DHCP?

Network Access Issues

- The link activity light must be on. If these LEDs are not on, the LAN segment may be dead.
- Can system be accessed on the network from another computer?
- Note: if on a network without a DHCP server, it can take up to 5 minutes before auto-negotiation configures an IP address. Use **ipconfig** to verify that the IP address is not 0.0.0.0 before trying to do any network activity.
- What IP address does **ping *hostname*** yield?
- What IP address does **nslookup *hostname*** yield?
- Can system be accessed via UNC in a Windows Explorer (**hostname**)?
- Are the systems all in the same subnet? If not, do they have normal IP address (that is, not one of the following 'unroutable' IP addresses):
  - 10.x.x.x
  - 172.16.x.x
  - 192.168.x.x
  - 224.0.0.0 (multicast-reserved)
- Is the Windows XP Network Firewall enabled? If so, is it configured correctly? (See "Changing the Windows XP Firewall Settings" (in the online help))

Login Issues

- How are you logged-in? (Workgroup vs. Domain).
- Are there different behaviors between workgroup and domain logins?

Using with Multiframe

- Is the agLogicSvc.exe service running on each system?
- If you changed any network cables, you need to re-initialize the agLogicSvc.exe service by stopping it and restarting it or by rebooting. Has this been done?
- All Gbit LAN cards on a Gbit LAN must use the same "Jumbo Frames" setting (see the LAN cards' advanced properties dialog). Also, if a switch/hub is used, you must make sure it supports the same size "Jumbo Frames" setting.

Network Hardware and Configuration

- Which OS is running? (Windows 2000 or Windows XP)
- How many network cards? (Motherboard built-in 100Base-T, gigabit LAN)
- From command prompt, run **ipconfig /all** for detailed configuration info.
- From command prompt, run **ipconfig /release** to release current IP addresses.
- From command prompt, run **ipconfig /renew** to re-obtain IP addresses.

Network Topology

- On public LAN? On private LAN? Cross-over cable? Multiple networks?
- Configurations:
  - Stand-alone
  - 1 network adapter - LAN.
  - 1 network adapter - cross-over cable.
  - 1 network adapter - private (switch or hub).
  - 2 network adapters - LAN + cross-over cable.
  - 2 network adapters - LAN + private (switch or hub).

Known OS Issues

- Are the **SSDP** and **UPnP** services running? (SSDP = Manual, UPnP = Automatic).

  On some systems, the SSDP Discovery Service suddenly wakes up and starts using a lot of CPU time. This is a 'manual' service, which listens for a Universal Plug-n-Play request, and is thus started when a particular packet is received.

  When this happens, the SSDPSRW task starts, stops, and starts again in a loop.

  To disable the service, choose **My Computer>Manage>Services>SSDP Discovery Service>Properties** and set to **Disable**.

  Then, set the SSDP service back to manual.

  Failure to do this can cause the system logger to fill up and other nasty side effects.

- Is the **Computer Browser** service running? If all systems are Windows XP, or if there is a DHCP server on the network, it may not be necessary for Computer Browser to be running. Furthermore, if the domain name server is NT 4.0, running computer browser on the network can lock out the 'real' domain server making it impossible for people on the network to log in reliably.

Logic Analyzer Specific Issues

- Are there any *Agilent Logic Analyzer* application specific problems (application or service) being seen? (Connection error dialogs, crashes, other).

Keep System Protected, Up-To-Date

- Use Windows Update to keep up-to-date on critical updates and service packs.
- Keep the virus definitions up-to-date in your anti-virus software.
- Install any *Agilent Logic Analyzer* application updates using their InstallShield packages.
- The local Administrator password should not be empty.

Remote Desktop Set Up

If your logic analysis system has the Windows XP Professional operating system, it supports Remote Desktop Protocol (RDP) connections.

To enable Remote Desktop connections to the logic analysis system, see the Remote Desktop topics in the Windows XP online help:

1. From the Windows Start menu, choose **Start>Help and Support**.
2. In the Help and Support Center window, enter "Remote Desktop" in the Search field; then, click the green arrow button to start the search.
3. Go to the topic on setting up the computer to use Remote Desktop, and follow its instructions.

When you set up a computer to use Remote Desktop, it is enabled as an exception in the operating system's firewall.

See Also

- " Changing Windows Firewall Settings, XP Service Pack 2" (in the online help)
- " Changing Firewall Settings, XP Service Pack 1" (in the online help)

For More Information

Documentation

Quick Start/Installation Guide

The *Quick Start/Installation Guide* gives you information on how to connect system peripherals and probing. Also included is an overview of the interface and information on installing software upgrades. Use this guide to quickly get familiar with the analyzer and also as a future reference for keeping your analyzer up-to-date and running properly.

- "*16900-Series Logic Analysis System Installation Guide*"
- "*16800-Series Logic Analyzers Installation/Quick Start Guide*"
- "*1680-Series Logic Analyzers Quick Start/Installation Guide*"
- "*1690-Series Logic Analyzers Quick Start/Installation Guide*"

Probing Documentation

For more information on general-purpose probing, QFP package probing, target connector and connectorless probing, and other probing options, see:

- "*Probing Selection Quick Reference Card*"
- "*Probing Solutions for Logic Analyzers*" ("latest version on web")
- "*Logic Analyzer Probing Solutions*"

For more information on analysis probes and other processor and bus solutions, see:

- "*Processor and Bus Support for Logic Analyzers*" ("latest version on web")
- "*Processor, Bus, and FPGA Support for Logic Analyzers*"

Online Help System

The online help gives you product reference and feature information. Also included is a tutorial (see page 38) showing you how to make a basic measurement and containing links to time-saving features and concepts.

Agilent Technologies Web Sites

Corporation/Contact

- Corporation - "http://www.agilent.com"
- Contact Us - "http://www.agilent.com/find/contactus"
- Email Updates - "http://www.agilent.com/find/emailupdates"

Product Information

- Logic Analysis - "http://www.agilent.com/find/logic"
- Logic Analysis Software Download - "http://www.agilent.com/find/la-sw-download"
- Software on CD - "http://software.cos.agilent.com/LogicAnalyzerSW"

See Also

- Tutorial - Getting to know your logic analyzer (see page 38)

- Intrinsic Support (see page 361)

Intrinsic Support

Because the Agilent 16900-series logic analysis systems and 1680A/AD-series logic analyzers operate in a Microsoft Windows XP Professional environment, intrinsic support shall only cover the *Agilent Logic Analyzer* application. Intrinsic support shall also cover any Windows XP Professional operating system services utilized by the *Agilent Logic Analyzer* application:

- Print from the *Agilent Logic Analyzer* application.
- Networking.
- File management from the *Agilent Logic Analyzer* application.

Because the Agilent 1690A/AD-series logic analyzers operate on a hosted desktop PC, support shall only cover the *Agilent Logic Analyzer* application and the IEEE 1394 interface to the host PC. Intrinsic support shall not cover any other Windows XP Professional operating system issues other than those listed above. Other Windows XP Professional issues shall be considered Microsoft issues.

NOTE Any customer-installed applications on an Agilent 1680A,AD-series product shall not be supported by Agilent. Customers must contact the software vendor for support.

See Also

- Solving Problems (see page 321)
- For More Information (see page 359)

11
Concepts

Logic Analysis Basics

Other Logic Analysis Concepts

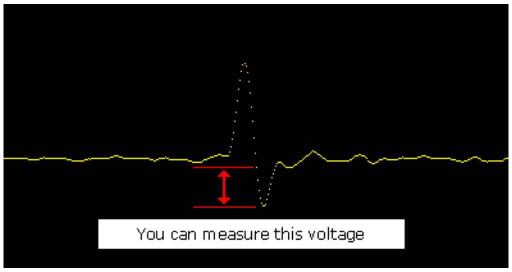
When should you use an oscilloscope?

[Tutorial Home (see page 38)] [Next Topic (see page 365)] [Previous Topic (see page 38)]

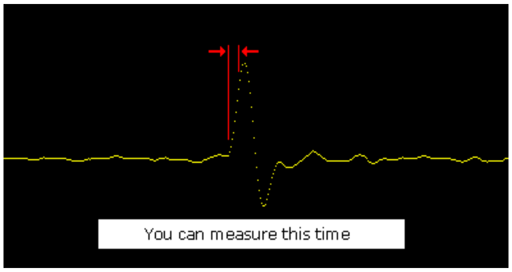
Generally, an oscilloscope is used when you need precise parametric information such as time intervals and voltage readings.

More specifically:

- When you need to measure small voltage excursions on your signals such as undershoot or overshoot.



- When you need high time-interval accuracy. Oscilloscopes can capture precise parametric information such as the time between two points on a rising edge of a pulse with very high accuracy.



When should you use a logic analyzer?

[Tutorial Home (see page 38)] [Next Topic (see page 366)] [Previous Topic (see page 364)]

Generally, a logic analyzer is used to view timing relationships among many signals, or if you need to trigger on patterns of logic highs and lows. A logic analyzer reacts the same way as the logic circuits do when a voltage threshold is crossed by a signal in the device under test. It will recognize the signal to be either low or high.

More specifically:

- When you need to see many signals at once.

  Logic analyzers are very good at organizing and displaying multiple signals. A common task is to group multiple signals into a bus and assign a custom name. Good examples are address, data, and control buses.

- When you need to look at signals in your system the same way your hardware does.

  Signals are displayed on a time axis so you can see when transitions occur relative to other bus signals or clock signals.

- When you need to trigger on a unique bus pattern or signal edge.

  Logic analyzers can be configured to store data when the high or low values of a group (bus) of signals match a predefined pattern.

  Logic analyzers can be configured to store data when a specific edge or level is detected on a single signal.

What is a logic analyzer?

[Tutorial Home (see page 38)] [Next Topic (see page 366)] [Previous Topic (see page 365)]

Now that we've talked a little about when to use a logic analyzer, let's look in more detail at what a logic analyzer is. Up to now, we've used the term "logic analyzer" rather loosely. In fact, most logic analyzers are really two analyzers in one.

What is a timing analyzer?

A timing analyzer is the part of a logic analyzer that is analogous to an oscilloscope. As a matter of fact, they can be thought of as close cousins.

The timing analyzer displays information in the same general form as an oscilloscope, with the horizontal axis representing time and the vertical axis as voltage amplitude. Because the waveforms on both instruments are time-dependent, the displays are said to be in the "time domain".

The basic areas of functionality in a timing analyzer are as follows:

- Sampling clock in the timing analyzer (see page 366)
- Sampling in the timing acquisition mode (see page 367)
- Triggering the timing analyzer (see page 368)

What is a state analyzer?

A state analyzer is very good at tracking down bugs in software or defective components in hardware. It can help eliminate the question whether a problem is in the software code or some hardware device.

Most often, state analyzers are used to find out what logic levels are present on a bus when a particular clock signal occurs. In other words, you want to know what "state of activity" is present when the clock occurs and data is suppose to be valid. Data captured in memory is displayed in a listing format with a time tag attached to every state.

The basic areas of functionality in a state analyzer are as follows:

- Sampling clock in the state analyzer (see page 369)
- Sampling in the state acquisition mode (see page 370)
- Triggering the state analyzer (see page 370)

Sampling clock in the timing analyzer

[Tutorial Home (see page 38)] [Next Topic (see page 367)] [Previous Topic (see page 366)]

The timing analyzer uses its own internal clock to control the sampling of data. This type of clocking makes the sampling of data in the logic analyzer *asynchronous* to the clocking in the device under test.

More specifically:

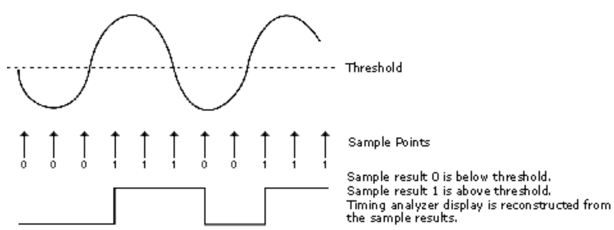
- A timing analyzer is good at showing you "When" signal activity occurs "Relative to other signals".
- A timing analyzer is more interested in viewing the timing relationships between individual signals, than the timing relationships to the signals that are controlling execution in the device under test.
- This is why a timing analyzer can sample data "out of sync", or asynchronous to the device under test clock signals.

Sampling in the timing acquisition mode

[Tutorial Home (see page 38)] [Next Topic (see page 368)] [Previous Topic (see page 366)]

In the timing acquisition mode, the logic analyzer works by sampling the input waveforms to determine whether they are high or low. It determines a high or low by comparing the voltage level of the incoming signal to a user-defined voltage threshold. If the signal is above that threshold when it samples, it will be displayed as a 1 or high by the analyzer. By the same criterion, any signal sampled that is below threshold is displayed as a 0 or low.

The figure below illustrates how a logic analyzer samples a sine wave as it crosses the threshold level.

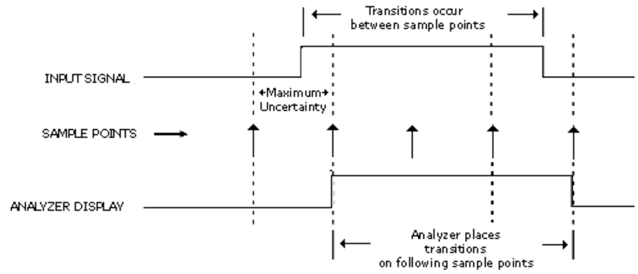


The sample points are then stored in memory and used to reconstruct a more squared-off digital waveform.

This tendency to square everything up would seem to limit the usefulness of a timing analyzer. However, a timing analyzer is not intended as a parametric instrument. If you want to check rise time of a signal, use an oscilloscope. If you need to verify timing relationships among several or hundreds of signals by seeing them all together, a timing analyzer is the right choice.

Sampling accuracy

When the timing analyzer samples an input channel, it is either high or low. If the channel is at one state (high or low) on one sample, and the opposite state on the next sample, the analyzer "knows" that the input signal has transitioned sometime between the two samples. It doesn't know when, so it places the transition point at the next sample, as shown in the figure below.



This presents some ambiguity as to when the transition actually occurred and when it is displayed by the analyzer.

Worst case for this ambiguity is one sample period, assuming that the transition occurred immediately after the previous sample point.

With this technique however, there is a trade-off between resolution and total acquisition time. Remember that every sampling point uses one memory location. Thus, the higher the resolution (faster sampling rate), the shorter the acquisition window.

Triggering the timing analyzer

[Tutorial Home (see page 38)] [Next Topic (see page 369)] [Previous Topic (see page 367)]

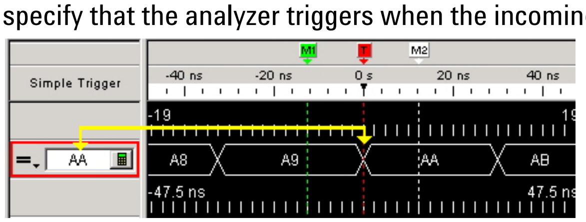
At some point in a measurement, the logic analyzer has to know when to capture (store) the data that is flowing through its memory. This is know as the trigger point.

One way to get the analyzer to trigger is to configure the analyzer to look for either a pattern of highs and lows from a group of signals (bus), or a rising or falling edge from a single signal. When the analyzer sees the specified patterns or edges in data, it triggers.

Pattern Trigger Pattern triggers are used to find specific patterns of highs and lows across a bus. You can specify different kinds of criteria such as equal, not equal, in or out of a range, or greater than/less than.

NOTE

Example: You have a bus containing 8 signal lines. You configure the *Simple Trigger* to specify that the analyzer triggers when the incoming data is equal to a pattern of "AA".



To make things easier for some users, the trigger point on most analyzers can be set not only in Hex, but in binary (1's and 0's), octal, ASCII, or decimal. For instance, the Hex trigger value of AA could also be set to an equivalent binary trigger value of 1010 1010. However, using hex for the trigger point is particularly helpful when looking at buses that are 16, 24, 32, or 64 bits wide.

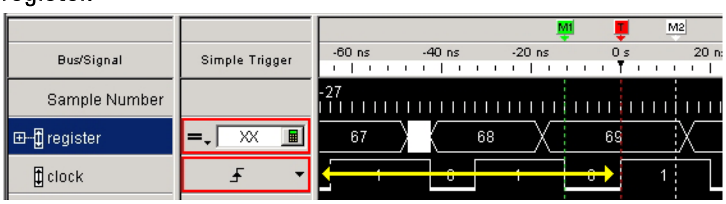
Edge Trigger

Edge triggering is a familiar concept to those accustomed to using an oscilloscope. When adjusting the "trigger level" knob on an oscilloscope, you could think of it as setting the level of a voltage comparator that tells the oscilloscope to trigger when the input voltage crosses that level. A timing analyzer works essentially the same on edge triggering except that the trigger level is preset to a logic threshold.

While many logic devices are level dependent, clock and control signals of these devices are often edge-sensitive. Edge triggering allows you to start capturing data as the device is clocked.

NOTE

Example: Take the case of an edge-triggered shift register that is not shifting data correctly. Is the problem with the data or the clock edge? In order to check the device, we need to verify the data when it is clocked – on the clock edge. The analyzer can be told to capture data when the clock edge occurs (rising or falling) and catch all of the outputs of the shift register.



Sampling clock in the state analyzer

[Tutorial Home (see page 38)] [Next Topic (see page 370)] [Previous Topic (see page 368)]

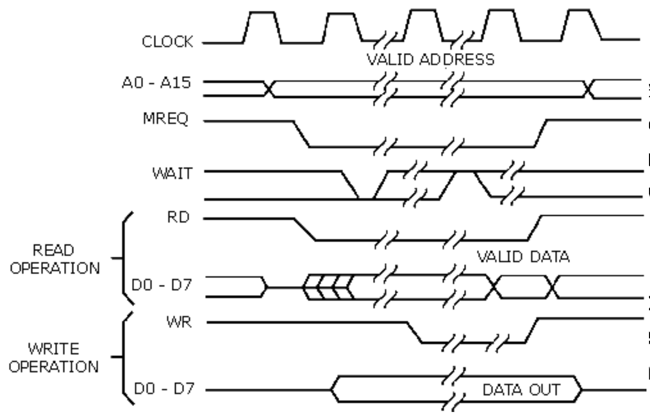
The state analyzer requires a sampling clock signal from the device under test. This type of clocking makes the sampling of data in the logic analyzer *synchronous* to the clocked events on the device under test.

More specifically:

- A state analyzer is good at showing you "What" the signal activity is during a "Valid clock or control signal".
- A state analyzer is more interested in viewing signal activity during specified times of execution, than signal activity unrelated to the timing.
- This is why a state analyzer wants to sample data that is "synchronized" or synchronous to the device under test clock signals.

Sampling in the state acquisition mode

[Tutorial Home (see page 38)] [Next Topic (see page 370)] [Previous



both data and address
the correct data, the logic
o times when only the
l lines. It does this by
with different sampling

NOTE

pture addresses, we want the
data, we want the analyzer to
RD goes low (read cycle).

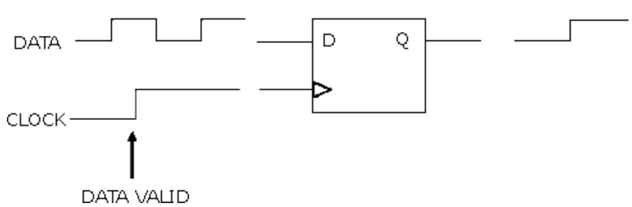
Triggering the state analyzer

[Tutorial Home (see page 38)] [Next Topic (see page 39)] [Previous Topic (see page 370)]

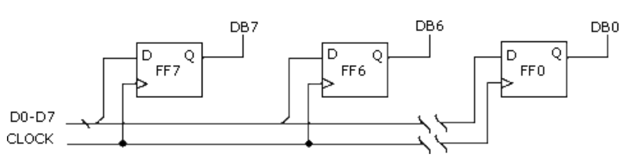
Similar to a timing analyzer, a state analyzer has the capability to qualify the data we want to store. If we are looking for a specific pattern of highs and lows on the address bus, we can tell the analyzer to start storing when it finds that pattern and to continue storing until the analyzer's memory is full.

Simple Trigger Example

Looking at the "D" flip-flop shown below, data on the "D" input is not valid until after a positive-going clock edge occurs. Thus, a valid state for the flip-flop is when the clock input is high.

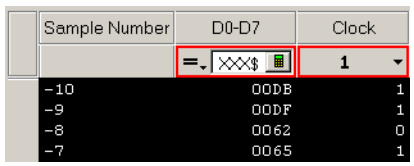


Now imagine that we have eight of these flip-flops in parallel. All eight are connected to the same clock signal as shown below.



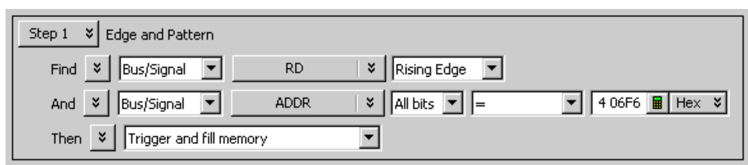
When a high level occurs on the clock line, all eight capture data at their "D" inputs. Again, a valid state occurs each time there is a positive level on the clock line.

The following simple trigger tells the analyzer to collect data on lines D0 - D7 when a high level is on the clock line.



Advanced Trigger Example

You want to see what data is stored in memory at the address value 406F6. You configure the advanced trigger to look for the pattern 406F6 (hexadecimal) on the address bus and a high level on the RD (memory read) clock line.



As you configure the Edge And Pattern trigger dialog, try to think of it as constructing a sentence that reads left-to-right.

"Find the first occurrence of a **Bus** named **ADDR,** and on **All bits** a pattern that **Equals406F6 Hex**, And a **Signal** named **RD** with a **High** level. Then **Trigger and fill memory** with **Anything**.

Pod and Channel Naming Conventions

In 16900-series logic analysis systems:

- Slots are named "A" through "F" starting with the top slot.
- There is a cable marked "Pod 2" connected to every logic analyzer card. It is important to know which slot a pod is connected to because if you have logic analyzer cards in slots A and B, there will be two pod cables labeled "Pod 2", but the *Agilent Logic Analyzer* application will refer to one as "Slot A Pod 2" and the other as "Slot B Pod 2". It's important not to mix up the two cables.
- Slot A Pod 2 is the same as "Pod A2". "A2" is used interchangeably with "Slot A Pod 2"; likewise, "D1" is used interchangeably with "Slot D Pod 1".

In 16900-series logic analysis systems and 1680/1690-series logic analyzers:

- The Clock Pod consists of the all of the clock channels for all of the pods in this module.
- Each pod has a clock channel. All of the clock channels are numbered Clk1, Clk2, Clk3, etc. If there is a logic analyzer module with two logic analyzer cards with four pods each, the clocks will be labeled Clk1 through Clk8.
- Clock channels are also labeled "C1" as well as "Clk1". "C1" and "Clk1" are the same.

In 16900-series logic analysis systems, don't confuse clock channel "C2" with Pod 2 in Slot C which is referred to as "Pod C2". For clock channels, the "C" is short for "Clock" and not Slot C.

Why Are Pods Missing?

There are a number of reasons all pods are not available to a logic analyzer module:

- In the state sampling mode, with the *General State Mode* (see page 574) sampling option selected, choosing the maximum acquisition memory depth requires one pod pair to be reserved for time tag storage. In this case, setting the memory depth to half of the maximum (or less) will return the pods.
- In the state sampling mode, with the *Turbo State Mode* (see page 574) sampling option selected, one pod pair is reserved for time tag storage.
- In the timing sampling mode, with the *Transitional / Store Qualified Timing Mode* (see page 573) sampling option selected:
  - When the smallest sampling period is selected, one pod pair is reserved for time tag storage.
  - When sampling periods other than the smallest are selected, choosing the maximum acquisition memory depth requires one pod pair to be reserved for time tag storage. In this case, setting the memory depth to half of the maximum (or less) will return the pods.
- The module is part of a logic analyzer that has been split. In this case, the pods are in the module that is the other half of the split analyzer.

See Also

- Memory Depth and Channel Count Trade-offs (see page 374)
- Configuring Logic Analyzer Modules (see page 76)

Memory Depth and Channel Count Trade-offs

This topic describes the interaction between channel count, memory depth, and triggering in the:

- State Sampling Mode (see page 374)
- Transitional Timing Sampling Mode (see page 375)

NOTE The memory depth and channel count trade-offs are somewhat different in the 16760 logic analyzer (see 16760 Logic Analyzer Memory Depth and Channel Count Tradeoffs (see page 585)).

State Sampling Mode

Time Tag Storage Requires 1 Pod Pair or 1/2 Acquisition Memory

- In the *Agilent Logic Analyzer* application, all modules are time-correlated; you cannot turn off *time tag storage* (as you could with previous Agilent logic analysis systems).
- To use more than 1/2 of a module's acquisition memory, one *pod pair* must be *reserved for time tag storage*. To use all pod pairs, you must use 1/2 (or less) of a module's acquisition memory.
- In general, the number of timers available = the number of pod pairs not reserved for time tag storage (refer to your logic analyzer characteristics (see page 595) for the actual number of timers available).

Default Settings

- Time tag storage is always on (and cannot be turned off).
- Memory depth is set at 1/2 of the total acquisition memory.
- All pod pairs are available for capturing data.
- If full memory is selected, the default pod pair to be used for time tag storage is the leftmost, but any pod pair without buses or signals assigned can be used.

Selecting Full Memory Depth when No Channels Assigned to a Pod Pair

- The pod pair is automatically reserved for time tag storage.

Selecting Full Memory Depth when Channels Assigned to All Pod Pairs

A dialog appears to caution you that:

- Bus/signals will lose assigned channels.
- Trigger specifications that use timer resources may be affected.

Going from Full Memory Depth to Half Memory Depth

- The pod pair reserved for time tag storage is automatically freed (assigned to the logic analyzer) so it can be used to capture data.

Splitting an Analyzer

In the Split Analyzer Setup dialog (see page 489) you can:

- Specify whether pod pairs should be reserved for time tag storage.

Transitional Timing Sampling Mode

Time Tag Storage Requires 1 Pod Pair or 1/2 Acquisition Memory

- The transitional timing sampling mode also requires *time tag storage*.
- When the smallest sampling period is chosen, one *pod pair* must be *reserved for time tag storage*. In this case, you cannot use 1/2 (or less) of a module's acquisition memory to gain back the *pod pair*.
- With other sampling periods, the memory depth and channel count trade-offs are the same as in the state sampling mode. That is, to use more than 1/2 of a module's acquisition memory, one *pod pair* must be *reserved for time tag storage*. To use all pod pairs, you must use 1/2 (or less) of a module's acquisition memory.
- In general, the number of timers available = the number of pod pairs not reserved for time tag storage (refer to your logic analyzer characteristics (see page 595) for the actual number of timers available).

Default Settings

- Time tag storage is required.
- If full memory is selected, the default pod pair to be used for time tag storage is the leftmost, but any pod pair without buses or signals assigned can be used.

See Also

- Configuring Logic Analyzer Modules (see page 76)
- To set acquisition memory depth (see page 112)
- Choosing the Sampling Mode (see page 97)
- Logic Analyzer Notes, Channels and Memory Depth (see page 573)

Transitional Timing

In the **Transitional / Store qualified** timing mode, the timing analyzer samples data at regular intervals, but only stores data when there is a signal transition across the threshold voltage level. Each time a transition occurs on any of the bits in the defined buses/signals (that haven't been excluded), data on all channels is stored. A *time tag* is stored with each stored data sample so the measurement can be reconstructed and displayed later.

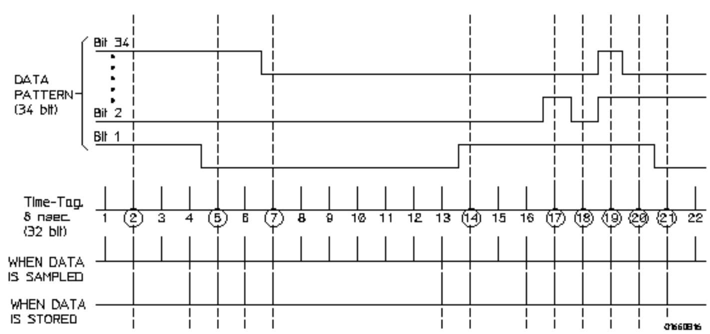
More on Storing Transitions

Minimum Transitions Stored

Normally, transitions do not occur at each sample point. This is illustrated below with time tags 2, 5, 7, and 14. When transitions do occur, two samples are stored for every transition. Therefore, with 2K samples of memory, 1K transitions are stored. You must subtract one, which is necessary for a starting point, for a minimum of 1023 stored transitions.

Maximum Transitions Stored

If transitions occur at a fast rate, such that there is a transition at each sample point, only one sample is stored for each transition as shown by time tags 17 through 21 below. If this continues for the entire trace, the number of transitions stored is 2K samples. Again, you must subtract the starting point sample, which then yields a maximum of 2047 stored transitions.



In most cases a transitional timing trace is stored by a mixture of the minimum and maximum cases. Therefore, in this example the actual number of transitions stored will be between 1023 and 2047.

Transitional Timing Considerations

Data Storage When an edge is detected, two samples are stored across all channels assigned to the timing analyzer. Two samples are needed to avoid data loss if a second edge occurs (after the first edge) before the edge detectors can reset.

Sequence Step Branching In transitional timing, only 2 branches are available per sequence step.

Global Counters In transitional timing, only one global counter is available.

Storing Time Tags Transitional timing requires time tags to recreate the data. Time tags are stored by interleaving them with measurement data in memory.

Increasing Duration of Storage (Amount of Time Measured) By default, the analyzer looks for transitions on all buses/signals defined for the logic analyzer module. However, to increase usable memory depth and acquisition time, you can, in the Advanced Trigger dialog (see page 445), exclude certain bus/signal transitions from being stored (like clock or strobe signal transitions that add little useful information to the measurement).

Data on Unassigned Channels When you run a measurement, data is captured on all logic analyzer channels, whether buses/signals are defined and assigned to those channels or not. In the transitional timing mode, captured samples are saved if there are transitions on the *defined* buses/signals (that haven't been excluded).

After a transitional timing measurement has been run, if you define new buses/signals for previously unassigned logic analyzer channels, the data captured on those channels appears, but it is unlikely that all transitions on those buses/signals have been stored; the data that appears is as if the new buses/signals had been excluded before the measurement was run.

Trigger Position In transitional timing, no data prestore (samples acquired before trigger) is required. Therefore, much like state mode, the trigger position (start/center/end) indicates the percentage of memory filled with samples after the trigger. The number of samples acquired/displayed before the trigger will vary between measurements.

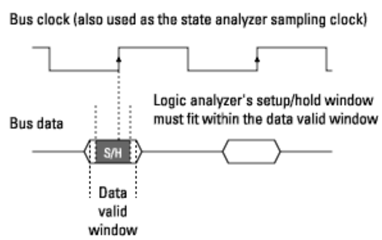
Understanding State Mode Sampling Positions

Synchronous sampling (state mode) logic analyzers are like edge-triggered flip-flops in that they require input logic signals to be stable for a period of time before the clock event (setup time) and after the clock event (hold time) in order to properly interpret the logic level. The combined setup and hold time is known as the setup/hold window.

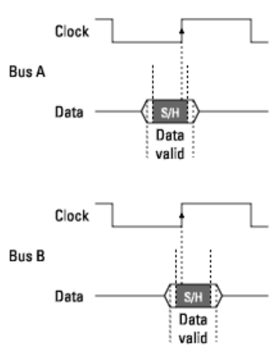
A device under test (because of its own setup/hold requirements) specifies that data be valid on a bus for a certain length of time. This is known as the data valid window. The data valid window on most buses is generally less than half of the bus clock period.

To accurately capture data on a bus:

- The logic analyzer's setup/hold time must fit within the data valid window.



- Because the location of the data valid window relative to the bus clock is different for different types of buses, the position of the logic analyzer's setup/hold window must be adjustable (relative to the sampling clock, and with fine resolution) within the data valid window. For example:



To position the setup/hold window (sampling position) within the data valid window, a logic analyzer has an adjustable delay on each sampling input (to position the setup/hold window for each channel).

Sample Position Adjustments on Individual Channels

When you can make sampling position adjustments on individual channels, you can make the logic analyzer's setup/hold window smaller because you can correct for the skew effects caused by the probe cables and the logic analyzer's internal circuit board traces, and you are left with the setup/hold requirements of the logic analyzer's internal sampling circuitry.

However, the process of manually positioning the setup/hold window for each channel is time consuming. For each signal in the device under test and each logic analyzer channel, you must measure the data valid window in relation to the bus clock (with an oscilloscope), repeatedly position the setup/hold window and run measurements to see if the logic analyzer captures data correctly, and finally position the setup/hold window in between the positions where data was captured incorrectly.

With Agilent Technologies logic analyzers that have the *eye finder* feature, in a small fraction of the time that it takes to make the adjustments manually (and without the extra test equipment), you can automatically:

- Position the setup/hold window on each channel.
- Adjust the threshold voltage setting for the widest possible data valid window.

Eye finder is an easy way to get the smallest possible logic analyzer setup/hold window.

Eye Finder Overview

For the state sampling clock specified, *eye finder* locates data signal transitions (threshold voltage crossings) in a fixed range of time before and the after clock edges and gives you a display that helps set up the best sampling positions.

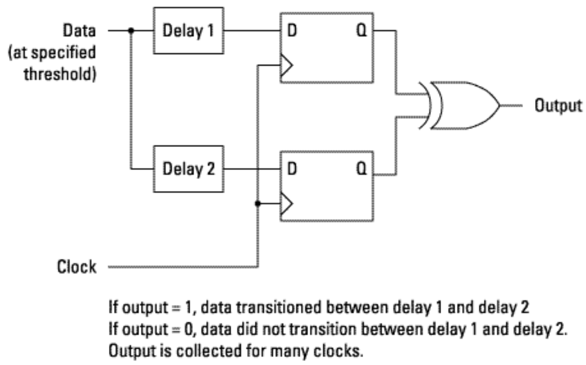
To understand the *eye finder* display, imagine, for each active clock edge, one "picture" of the data signal transitions around that edge is taken. Think of this as a snapshot or freeze-frame or stroboscope (centered on, or synchronized with, the clock edge). The time of arrival of the clock edge is T=0.

For example, if you select the rising edge of the clock input on Pod 1 as the state sampling clock, imagine a "picture" is snapped each time a rising edge on the Pod 1 clock arrives. It doesn't matter if the time between Pod 1 clock edges is the same or not. If you elect to sample on both rising and falling edges, then a "picture" is snapped on each. Again, it doesn't matter how much time elapses between active edges. A "picture" is taken on each one.

To build the *eye finder* display, hundreds of thousands of these "pictures" are stacked on top of each other. Each "picture" is aligned at T=0, which is when the active clock edge arrived. It doesn't matter if the pictures are from rising edges or falling edges; they are aligned at T=0. Once the display is built, you cannot tell whether a given signal transition region is associated with clock rising edges or falling edges (or both).

How Eye Finder Works

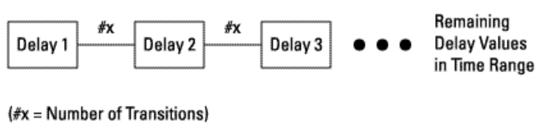
Eye finder measurements are made possible by the logic analyzer's ability to double-sample each channel using slightly offset delays and by comparing the delayed samples using an exclusive-OR operation.



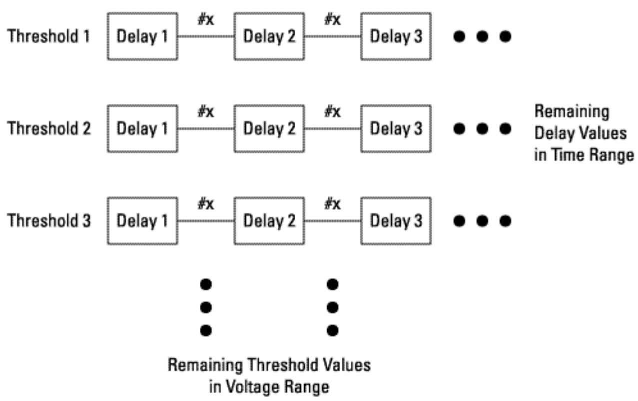
When the exclusive-OR output is high, the delayed samples are different, and a transition is detected between the delay times.

Because of jitter and other variations in the sampled signal, an *eye finder* measurement checks many clocks for each pair of delay values so that it can report how often transitions occur between the two delay times.

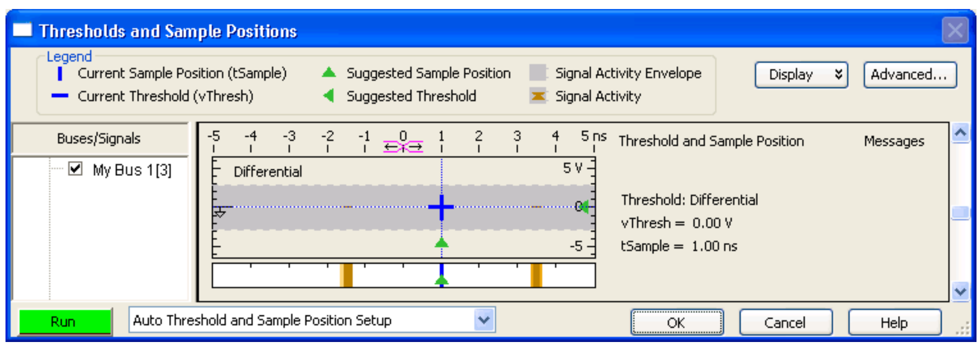
Then, another pair of delay values is checked, and so on, until a whole range of time is scanned for transitions.



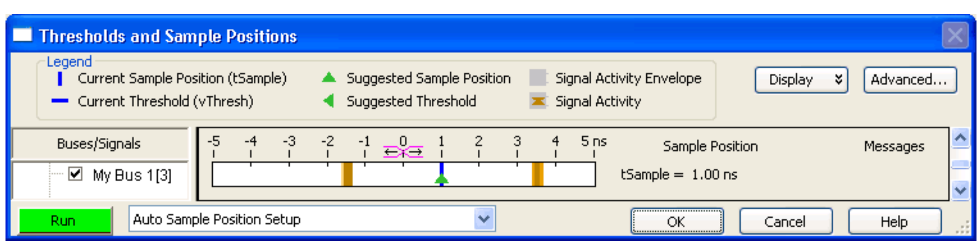
Because the logic analyzer is able to adjust the threshold voltage for channels, an *eye finder* measurement is able to repeat the scan for transitions over time at many threshold voltage levels.



By adjusting threshold voltages and watching activity indicators, *eye finder* is able to find the signal activity envelope and determine the optimal threshold voltage; then, by performing a full time scan at that threshold, *eye finder* is able to suggest the sample position.

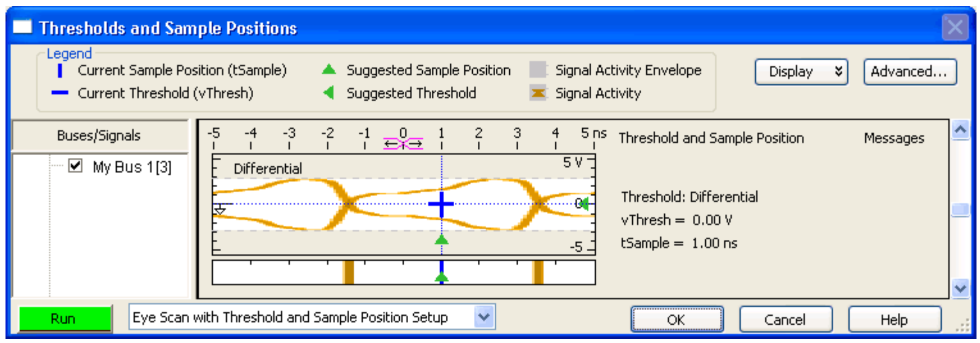


You can also run a full time scan at the current threshold voltage setting to automatically set sampling positions only.



The Auto Threshold and Sample Position Setup scan is usually enough to make sure data is captured accurately, but it may also identify signals that you want to look at in more detail (for example, if you notice delay, damping, etc.).

By performing full time scans across the full signal activity envelope, *eye finder* is able to give you a map of transitions detected in small windows of time and voltage. These scans are called *eye scans*. Oscilloscope-like eye diagrams are used to display the measurement data. The number of transitions in each window is indicated by brightness. This gives you a rough picture of the data eye and may tell you whether you need to look at signals in even more detail with an oscilloscope.



You can run *eye scans* that result in the automatic setting of threshold voltages and sampling positions or *eye scans* that result only in automatic setting of sampling positions.

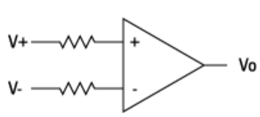
The number of channels on which an *eye finder* measurement collects data affects how long the measurement takes. The exception is when there are multiple logic analyzer cards in a module; in this case, measurements run simultaneously in parallel.

See Also

- To automatically adjust state sampling positions and threshold voltages (see page 107)
- To manually adjust state sampling positions (see page 110)
- Selecting the State Mode (Synchronous Sampling) (see page 100)
- Thresholds and Sample Positions Dialog (see page 497)

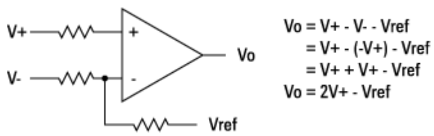
Eye Scan in Logic Analyzers that Support Differential Signals

Logic analyzers that support differential signals (like the 16753/54/55/56, 16760, and 16950 logic analyzers) use true differential receivers on their inputs:

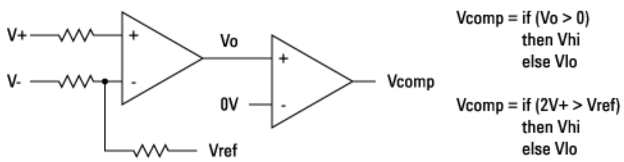


Vo = V+ - V-
= V+ - (-V+) [ideal diff signal]
= V+ + V+
Vo = 2V+

A programmable reference voltage is summed into the negative input. This is the threshold voltage when the analyzer is used with single ended probes. The reference is normally programmed to 0V for operation with differential probing:

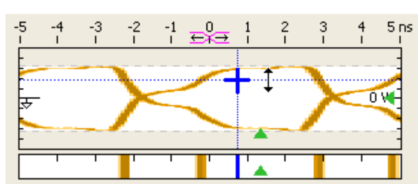


The output of the receiver is then compared to 0V to produce the internal logical signal from the differential input signal. Note that the final comparison produces the answer to the question "Is the differential signal above or below Vref?":



The *eye scan* measurement of the eye opening is performed by doing a series of *eye finder* measurements with different Vref settings. The default *eye finder* measurement for a differential input uses Vref=0V. By raising Vref above zero, we find where the signal crosses the elevated Vref value. If Vref is raised high enough, then the top rail of the signal goes through Vref, and we see the top of the eye. Raising Vref a bit more causes Vcomp to be constant at Vlo, meaning the signal never rises to that level. Conversely, moving Vref below zero finds the lower half of the eye.

The *eye scan/eye finder* display shows this relationship between *eye finder* and *eye scan* by showing the *eye finder* cross section below the *eye scan* diagram for each signal. By moving the horizontal Vth line in the *eye scan* diagram up and down you can obtain the *eye finder* view at that offset from the center of the eye.



The differential inputs to the logic analyzer are *always* applied to the receiver, regardless of threshold setting in the user interface. This means you can allow for a common mode voltage in the differential pair by manually setting the threshold voltage to a nonzero value. *Eye scan* will do this automatically if the center of the signal swing is more than about 100 mV from ground.

Understanding Logic Analyzer Triggering

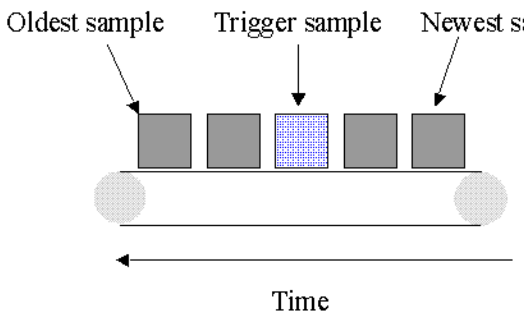
Setting up logic analyzer triggers can be difficult and time-consuming. You could assume that if you know how to program, you should be able to set up a logic analyzer trigger with no difficulty. However, this is not true because there are many concepts that are unique to logic analysis. The purpose of this section is to describe these key concepts and how to use them effectively.

See Also

- Capturing Data from the Device Under Test (see page 127)

The Conveyor Belt Analogy

The memory of a logic analyzer can be compared to a very long conveyor belt, and the samples acquired from the device under test (DUT) as boxes on the conveyor belt. At one end, new boxes are placed on the conveyor belt, and at the other end the boxes fall off. In other words, because logic analyzer memory is limited in depth (number of samples), whenever a new sample is acquired the oldest sample currently in memory is thrown away if the memory is full. This is shown in the following figure.



The conveyor belt analogy

A logic analyzer trigger is similar to someone standing at the beginning of the conveyor belt placing more boxes on it. They are told to "look for a special box and to stop the conveyor belt when that box reaches a particular position on the belt". Using this analogy, the special box is the trigger. Once a logic analyzer detects a sample that matches the trigger condition, this is the indication that it should stop acquiring more samples when the trigger is located appropriately in memory.

The location of the trigger in memory is known as the *trigger position*. Normally, the trigger position is set to the middle so that the maximum number of samples that occurred before and after the trigger are in memory. However, you can set the trigger position to any point in memory.

The concepts in this analogy are summed up in the following table.

Mapping of concepts in the Conveyor Belt Analogy to a Logic Analyzer

Conveyor Belt Analogy	Logic Analyzer
Boxes on the belt	Samples acquired from the device under test
Number of boxes that will fit on the belt	Memory depth
Special box	Trigger point

Next: Summary of Triggering Capabilities (see page 386)

Summary of Triggering Capabilities

Because logic analyzer triggering provides a great deal of functionality, the following table provides a brief summary of the capabilities covered in this article. Each of these capabilities will be described.

Summary of Logic Analyzer Triggering Capabilities

Capability	Examples
Edges	`If there is rising edge on SIG1 then Trigger` `If there is falling edge on SIG1 then Trigger`
Boolean expressions	`If ADDR = 1000 and DATA = 2000`
Ranges	`If ADDR in range 1000 to 2000`

Storage qualification	`1. If..`
	`   Else If ADDR in range 1000 to 2000 then`
	`     Store Sample`
	`     Go to 1`
	`   Else If ADDR not in range 1000 to 2000 then`
	`     Don't Store Sample`
	`     Go to 1`

Counters	`1. If DATA = 1000 Then`
	`     Increment Counter 1`
	`     Go to 2`
	`2. If Counter 1 > 2 Then`
	`     Trigger`

Timers	`1. If DATA = 1000 Then`
	`     Start Timer 1`
	`     Go to 2`
	`2. If Timer 1 > 500 ns Then`
	`     Trigger`

Next: Sequence Steps (see page 387)

Sequence Steps

While logic analyzer triggers are often simple, they can require complex programming. For example, you may want to trigger on the rising edge of one signal that is followed by the rising edge of another signal. This means that the logic analyzer must first find the first rising edge before it begins looking for the next rising edge. Because there is a sequence of steps to find the trigger, this is known as a *trigger sequence*. Each step of the sequence is called a *sequence step*.

Each sequence step consists of two parts; the conditions and the actions. The conditions are Boolean expressions such as "If ADDR = 1000" or "If there is a rising edge on SIG1". The actions are what the logic analyzer should do if the condition is met. Examples of actions include triggering the logic analyzer, going to another sequence step, or starting a timer. This is similar to an If/Then statement in programming.

Each step in the trigger sequence is assigned a number. The first sequence step to be executed is always Sequence Step 1, but because of the Go To actions, the rest of the sequence steps can be executed in any order.

When a sequence step is executed and none of the Boolean expressions are true, the logic analyzer acquires the next sample and executes the same sequence step again. As a simple example, consider the following trigger sequence:

```
1. If DATA = 7000 then Trigger
```

If the following samples were acquired, the logic analyzer would trigger on sample #6.

```
Sample #   ADDR  DATA
   1       1000  2000
   2       1010  3000
   3       1020  4000
   4       1030  5000
   5       1040  6000
   6       1050  7000  <- This is where the logic analyzer triggers
   7       1060  2000
```

In essence, Sequence Step 1 is equivalent to "Keep acquiring more samples until DATA=7000, then trigger".

If a Boolean expression in a sequence step is met, another sample is always acquired before the next sequence step is executed. In other words, if a sample meets the condition in Sequence Step 1, another sample will be acquired before executing Sequence Step 2. This means that it is not possible for a single sample to be used to meet the conditions of more than one sequence step. Each sequence step can be thought of as representing events that occur at different points in time. Two sequence steps can never be used to specify two events that happen simultaneously.

For example, consider the following trigger sequence:

```
1. If ADDR = 1000 then Go to 2
2. If DATA = 2000 then Trigger
```

If the following samples were acquired, the logic analyzer would trigger on sample #7.

```
Sample #   ADDR  DATA
   1       1000  2000  <- This meets the condition in Sequence step #1
   2       1010  3000
   3       1020  4000
   4       1030  5000
   5       1040  6000
   6       1050  7000
   7       1060  2000  <- This is where the logic analyzer triggers
```

Note that the logic analyzer will not trigger on Sample #1 because a new sample is acquired between the time that the condition in Sequence Step 1 is met and when the condition in Sequence Step #2 is tested. A good way to think of this trigger sequence is "Find ADDR = 1000 followed by DATA = 2000 and then trigger". Multiple sequence steps in a trigger sequence imply a "followed by".

Once a logic analyzer triggers, it does not trigger again. In other words, even if more than one sample meets the trigger condition, the logic analyzer still only triggers once. For example, using "ADDR=1000" as our trigger, if the logic analyzer acquires the following samples, it will trigger on Sample #2 and only on Sample #2.

```
Sample #   ADDR
   1       0000
   2       1000  <- The logic analyzer triggers here
   3       2000
   4       1000  <- The logic analyzer does NOT trigger again here
   5       1040
```

A frequently asked question is "What happens if the conditions in a sequence step are not met?" For example, if there is a condition that says "If ADDR = 1000 Then Trigger", what happens if the current sample has ADDR = 2000? The logic analyzer simply acquires the next sample and tries to execute this sequence step again. In essence, if the trigger condition is "ADDR = 1000", this is equivalent to "Keep acquiring more samples until you find one that has ADDR=1000". Therefore, if you set up a trigger condition that is never met, the logic analyzer will never trigger.

When the conditions are met in a sequence step, it is clear which sequence step will be executed next when a "Go To" action is used, but it is not necessarily clear if there is no "Go To". On some logic analyzers, if there is no "Go To", this means that the next sequence step should be executed. On other logic analyzers, it means the same sequence step should be executed again. Because of this confusion, it is good practice to always use a "Go To" action rather than relying on the default. The state and timing modules deal with this problem by automatically including a "Go To" or "Trigger" action in every sequence step. For example:

```
If ADDR = 1000 and DATA = 2000 then
Go to 1   <- This is automatically added
```

Next: Boolean Expressions (see page 389)

Boolean Expressions

While multiple sequence steps imply a "followed by", within a sequence step Boolean expressions can be used. An example is:

```
If ADDR = 1000 and DATA = 2000
```

This expression means that for this expression to be met, ADDR must equal 1000 in the same sample that DATA equals 2000. In other words, ADDR equals 1000 at the same time that DATA equals 2000. Therefore, if you want to trigger on two events that occur at the same time, a Boolean expression should be used.

It's a common mistake to try to use two sequence steps when a Boolean expression should be used or to use a Boolean expression when two sequence steps should be used.

NOTE Boolean expressions are used for events that happen at the same time, and multiple sequence steps are used when one event follows another.

Next: Branches (see page 390)

Branches

Branches are similar to the *Switch* statement in the C programming language and the *Select Case* statement in Basic. They provide a method for testing multiple conditions. Each branch has its own actions. An example of multiple branches is shown below:

```
1. If ADDR < 1000 then Go To 2         <- This is a branch of Level 1
   Else If ADDR > 2000 then Go To 3    <- This is a 2nd branch of Level 1
   Else If DATA = 2000 then Trigger    <- This is a 3rd branch of Level 1
2. If DATA <= 7000 then Trigger
3. If there is a Rising Edge on SIG1, then Trigger
```

In sequence step 1, there are three branches, so there are three possible actions that can be taken.

When the condition of one branch is met, none of the branches below it are tested. In other words, there is no way for more than one branch to be executed based upon a single sample, even if the sample causes the conditions for more than one branch to be met. In other words, each branch is an "Else If".

Next: Edges (see page 390)

Edges

Edges represent a transition from low to high or high to low on a single signal. Typically, edges are specified as "rising edge", "falling edge", or "either edge", where "rising edge" indicates a transition from a low to a high. On most logic analyzers, up to two edges can be included in the trigger sequence although some allow only one.

Next: Ranges (see page 391)

Ranges

Ranges are a convenient method for specifying a range of values, such as "ADDR in range 1000 to 2000". Most logic analyzers also support a "not in range" function as well. Ranges are a convenient shortcut so that you don't have to specify "ADDR >= 1000 and ADDR <= 2000".

Next: Flags (see page 391)

Flags

Flags are Boolean variables that are used to send signals from one module to another. They can be set when a condition occurs in one module and tested later by another module. In the example below, flag 1 is used to keep track of what happens in the trigger sequence of Module 1 so that this information can be used in Module 2.

Trigger Sequence for Module 1:

```
1. If ADDR < 5000 then
     Set Flag 1
     Trigger and fill memory
```

Trigger Sequence for Module 2:

```
1. If DATA = 5000 and Flag 1 is set then Trigger
   Else if DATA = 1000 and not Flag 1 then Trigger
```

NOTE Flags are not available in 1680/1690-series logic analyzers.

Next: Occurrence Counters and Global Counters (see page 391)

Occurrence Counters and Global Counters

Occurrence Counters are used in situations where you want to find the Nth occurrence of an event. For example, if you want to trigger on the 5th time that ADDR = 1000, you could set up the trigger as:

```
If ADDR = 1000 occurs 5 times then Trigger
```

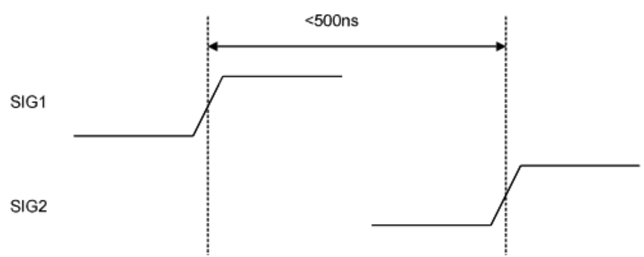
Global Counters are like integer variables. They are more flexible than Occurrence Counters because they can be used to count complex events such as an edge followed by another edge. Global Counters can be incremented, tested, and reset. By default, Global Counters begin with zero and don't need to be reset unless they have already been used in the trigger sequence. In general, Occurrence Counters should be used in place of Global Counters, if possible, because they are easier to use and because there is a limited number of Global Counters.

Next: Timers (see page 392)

Timers

Timers are used to check the amount of time that has elapsed between events. For example, if you want to trigger on one edge followed by another edge that occurs within 500 ns, use a timer. The most critical point to remember in using timers is that they need to be started before they are tested. In other words, timers do not start automatically.

The key to setting up a timer is to identify where it should be started and where it should be tested. Consider the example in the following figure. The timer should be started when the rising edge on SIG1 is detected and it should be tested when the rising edge occurs on SIG2.



An edge followed by an edge with a time limit

An example trigger sequence to set up this measurement is:

```
1. If there is a Rising Edge on SIG1, then
     Start Timer1
     Go to 2
2. If there is a Rising Edge on SIG2 AND Timer1 < 500ns then
     Trigger
```

While the above trigger sequence seems correct, it actually has a critical flaw. What happens if there is a rising edge on SIG1 but SIG2 doesn't occur within 500 ns? The logic analyzer will never trigger, because timer1 will keep running and condition "Timer1 < 500 ns" will never be met. There might be another rising edge on SIG1 that is followed within 500 ns by the rising edge on SIG2 that occurs later on, so this situation is unacceptable.

To fix this problem, whenever the timer exceeds 500 ns without triggering, the sequence should loop back to Level 1 to look for another rising edge on SIG1. The following shows an example of the correct sequence:

```
1. If there is a Rising Edge on SIG1, then
     Start Timer1
     Go to 2
2. If there is a Rising Edge on SIG2 AND Timer1 < 500ns then
     Trigger
```

```
Else If Timer1 >= 500ns then
  Reset Timer1
  Go to 1
```

Occasionally, you may run out of timers. A counter can be used in place of a timer if the logic analyzer is sampling at regular intervals (that is, if it's in the timing sampling mode). A timer can be simulated by counting the number of samples that are acquired. For example, if the logic analyzer acquires a new sample every 10 ns and seven samples are acquired, this represents 70 ns.

Next: Storage Qualification (see page 393)

Storage Qualification

Storage qualification is used to determine if an acquired sample should be stored (that is, placed in memory) or thrown away. This keeps the logic analyzer memory from being filled with samples that are not needed.

Default Storage The simplest method to set up storage qualification is by setting up the Default Storage. Default Storage means "unless a sequence step specifies otherwise, this is what should be stored". As an example, you may want to only store samples if ADDR is in the range 1000 to 2000, so you should set the Default Storage to:

```
ADDR In Range 1000 to 2000
```

By default, the Default Storage is set to store all samples acquired. You can also set the Default Storage to store nothing, which means that no samples will be stored unless a sequence step overrides the default storage.

Sequence Step Storage Sequence step storage qualification means that within a particular sequence step only certain samples will be stored. This means that until a "Go To" or "Trigger" action is used to leave this sequence step, the storage qualification applies. This is useful when you want different storage qualification for each sequence step. For example, you may want to store nothing until ADDR = 1000 and then store only samples with ADDR in the range 1000 to 2000 for the rest of the measurement.

Setting up sequence step storage requires the use of an additional branch. For example, if you want to store only samples with ADDR in the range 5000 to 6FFF while looking for DATA = 005E, the following sequence step could be used in some situations:

```
1. If DATA = 005E then Trigger
   Else If ADDR in range 5000 to 6FFF then
     Store Sample
     Go to 1
```

Note the use of the store sample action. This means "store the most recently acquired sample in memory now". It does *not* mean, "From now on, start storing". It should be noted that since the store sample action is never executed unless ADDR is in the range 5000 to 6FFF, this branch essentially means "While in this sequence step, store only samples with ADDR between 5000 and 6FFF".

The above example seems to imply that only samples with ADDR between 5000 and 6FFF will be stored. However, this depends upon how the default storage has been set up. Using the previous example, if the default storage is set to "Store Everything", and a sample is outside of the range 5000 to 6FFF, then the Else If branch is not executed and the Default Storage is applied. In essence, the sequence step has said what to do when a sample has a value in a particular range, but it doesn't say what to do for samples outside the range. Therefore, if you want to specify the sequence step storage unambiguously, use the following:

```
1. If DATA = 005E then Trigger
   Else If ADDR in range 5000 to 6FFF then
     Store Sample
     Go to 1
   Else If ADDR not in range 5000 to 6FFF then
     Don't Store Sample
     Go to 1
```

Alternatively, if the default storage is set to "Store Everything", use the following:

```
1. If DATA = 005E then Trigger
   Else If ADDR not in range 5000 to 6FFF then
     Don't Store Sample
     Go to 1
```

In summary, Sequence Step Storage always overrides the Default Storage, but only for the conditions specifically mentioned in the Sequence Step Storage. You must be very careful that you account for the interaction between Default Storage and Sequence Step Storage.

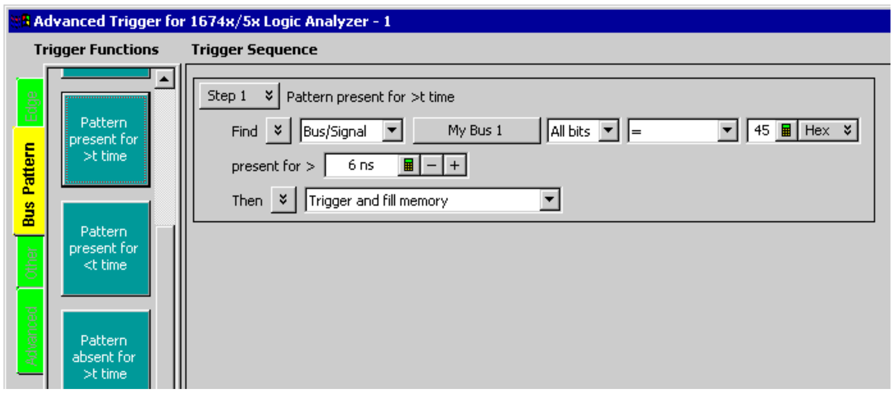
Next: Strategies for Setting Up Triggers (see page 394)

Strategies for Setting Up Triggers

- Trigger Functions (see page 394)
- Setting Up Complex Triggers (see page 397)
- Save and Document Your Trigger Sequences (see page 397)

Trigger Functions

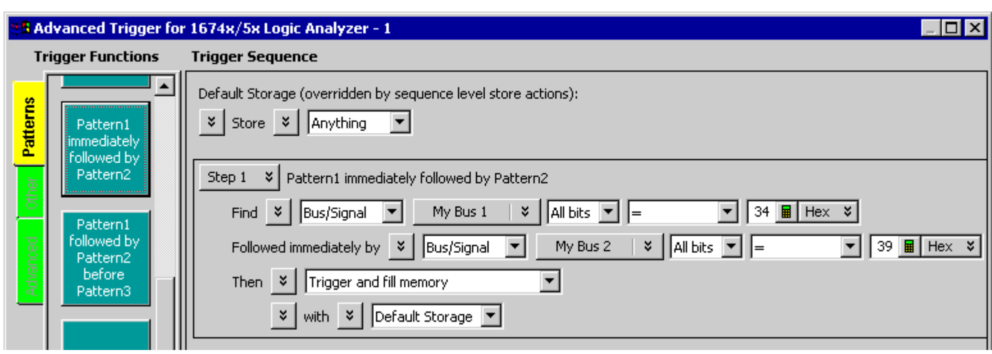
While setting up logic analyzer triggers can be difficult, *trigger functions* can greatly simplify the process. Trigger functions are commonly-needed building blocks that can be combined to set up a trigger. Because the functions cover most common triggers, you can set up your trigger simply by selecting the appropriate function and filling in the data. The logic analyzer trigger user interface is shown in the following figure. Note that trigger functions are prominently located at the left of the screen.



The trigger user interface

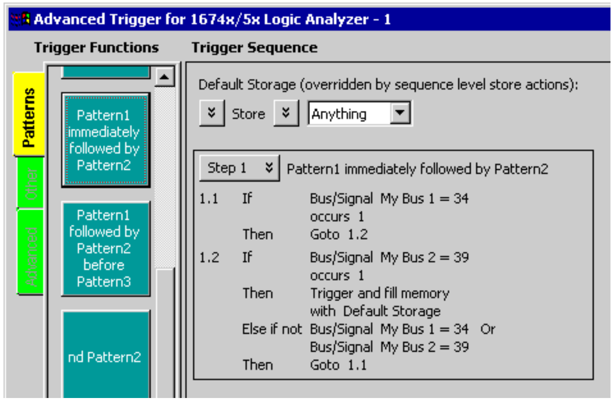
Note that a picture (which corresponds to the selected function) is provided by hovering over the trigger function button.

For example, if you want to trigger when a bus pattern is immediately followed by another bus pattern, you can drag-and-drop the "Pattern1 immediately followed by Pattern2" trigger function onto a trigger sequence step, as shown in the following figure.



Pattern1 immediately followed by Pattern2

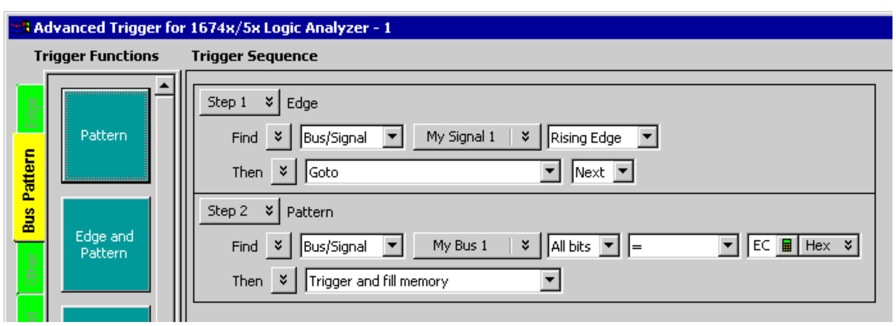
Once you have selected this function, you simply fill in the names of the buses and the patterns. Contrast the previous figure with the following figure, which is the same trigger created using If/Then statements. The trigger function is easier to use because the additional details of the If/Then statements have been hidden. However, if you want to see the details, you can *show trigger step as if/then.*



The same trigger as If/Then statements

Trigger functions can be modified. For example, if you start with the function "Find Edge", you can add another event, and it becomes the same as "Find Edge and Pattern". Therefore, a function that is not exactly correct can often be converted into the desired trigger. It is also possible to convert a trigger sequence step to advanced If/Then trigger functions and modify them.

Trigger functions are like building blocks because they can be used together in a trigger sequence. For example, if you want to set up a trigger as "Find edge followed by pattern", you can use a "Find Edge" function for Level 1 and a "Find Pattern" function for Sequence Level 2 (see the following figure). So, functions are useful both as an entire trigger sequence and as one step in a trigger sequence.



"Find Edge" and "Find Pattern" together

Next: Setting Up Complex Triggers (see page 397)

Setting Up Complex Triggers

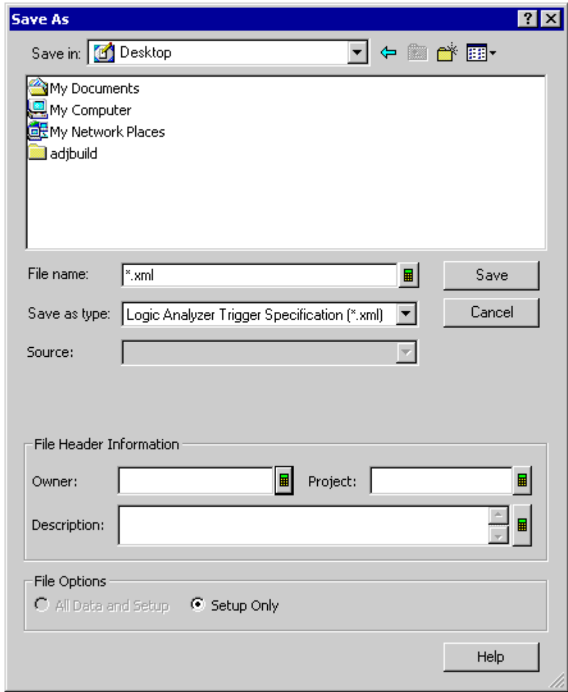
Frequently, the most difficult part of setting up a complex trigger is breaking down the problem. In other words, how do you map a complex trigger into sequence steps, branches, and Boolean expressions? Here are step by step instructions:

1. Break down the problem into events that don't happen simultaneously. These correspond to the sequence steps.
2. Scan the list of trigger functions to try to find some that match the events identified in Step #1.
3. Within all remaining events, break them down into Boolean expressions and their corresponding actions. Each Boolean expression/Action pair corresponds to a separate branch within a sequence step. Remember that "Store" branches may exist that are used only to handle storage qualification for that sequence step.

Next: Save and Document Your Trigger Sequences (see page 397)

Save and Document Your Trigger Sequences

If a trigger sequence is important at one time, it is likely to be important again. This is why saving and documenting trigger sequences is so valuable. Complex trigger sequences generally are too difficult to understand without some accompanying explanation. When saving a trigger specification to a file, you can enter a description of the trigger sequence in the file header information (see the following figure). Also, because the trigger specification file is in XML format, you edit the file and annotate steps with additional HTML-style comments (for example, <!-- Comment. -->).



Trigger specification Description when saving to a file

Next: Conclusions (see page 398)

Conclusions

Setting up logic analyzer triggers is very different than writing software. The job can be greatly simplified if other work can be leveraged by using pre-defined trigger functions and well-documented triggers that were written earlier. Only write your own trigger setup if there's nothing else available. Finally, when faced with a difficult trigger to set up, break down the problem into smaller chunks and deal with each one individually.

ALA vs. XML, When to Use Each Format

If you want to:	Then use:
Save and load sessions from a logic analysis system.	**ALA Format** — ALA format files are more complete, and the format is more efficient for saving and loading logic analyzer information.
Share captured data.	**ALA Format** — In *offline* mode, you can read ALA format configuration files in any instance of the *Agilent Logic Analyzer* application, without having licenses for licensed tools, windows, etc. that may be used in the configuration. This provides "read-only" capability; licenses are required to go *online* or add any licensed tools, windows, etc. **XML Format** — You can also share captured data using XML format configuration files. When loading an XML format file with data, you are forced into *offline* mode. Also, when viewing data from XML format configuration files, you need licenses for any licensed tools that may be used in the configuration.
Transfer module setup information between similar logic analyzers.	**ALA Format** — ALA format configuration files can only be loaded by logic analysis systems with compatible modules (for example, modules in the same or similar logic analyzer families like the 16740/41/42A and 16750/51/52A/B).
Transfer module setup information between different logic analyzers.	**XML Format** — If you want to transfer setup information between incompatible modules, you must use XML format configuration files.
Transfer only part of a logic analyzer setup.	**XML Format** — You can load edited XML format configuration files.
Control the logic analysis system remotely using COM automation.	**XML Format** — The COM automation interface has commands for setting up parts of the logic analysis system with XML format strings. You can get these strings from XML format configuration files. (You can also load complete setups from ALA format configuration files using COM automation.)
Insert symbol information from software development tools.	**XML Format** — When a compiler-generated output file can't be loaded, you can save the configuration to an XML format file, edit it to include the symbol information (which has been translated into the logic analyzer's XML format), and open the XML format file again.

See Also

- To save a configuration file (see page 171)
- To open a configuration file (see page 184)
- To transfer module setups to/from multi-module systems (see page 188)
- ALA Format (see page 532)
- "XML Format" (in the online help)

Multiframe Logic Analysis Systems

If you need to make time-correlated measurements with more logic analysis channels than can be installed in a single frame, you can connect multiple 16900A, 16901A, and 16902A logic analysis system frames together.

NOTE

Not all logic analysis systems have multiframe capability. If the back of your instrument does not have an "Input" and "Output" connector, it does not support multiframe. For example, the 16903A logic analysis system and the 1680/1690-series logic analyzers do not support multiframe.

The "*16900-Series Logic Analysis System Installation Guide*" shows you how to connect multiple frames. Basically, each 16900A, 16901A, or 16902A frame has two multiframe connectors, labeled "Input" and "Output". A multiframe cable connects the output of one frame to the input of another frame. You can chain as many frames as you like together this way. The *master frame* is the one with the open input connector; all other frames are *slave frames*, and the one with the open output connector is the *terminating slave frame*.

CAUTION

Failing to follow one of the recommended multiframe configurations in the installation guide can result in unpredictable software behavior and/or poor analyzer performance!

In addition to the multiframe cables, the frames must also be connected to a network. Usually, this is a Gbit LAN network. It can be a private or public network (see installation guide). The multiframe cable is used for time correlation, cross-triggering, and multiframe setup; all other inter-frame communication and data transfer take place over the network.

NOTE

If (and only if) you encounter problems after changing multiframe connections, try rebooting all frames in the multiframe set. However, this should not be necessary. All frames will automatically adjust to multiframe cable changes and/or network changes.

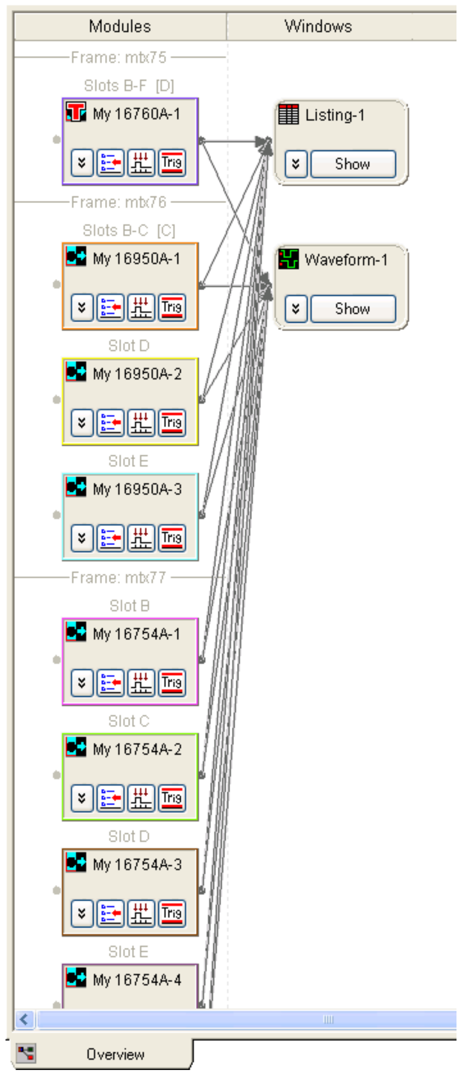
CAUTION

Changing multiframe cables and/or network cables while a user is connected (online) with the multiframe set will force them offline—losing any unsaved changes.

The *Agilent Logic Analyzer* application can run on the *master frame*, a *slave frame*, or another personal computer.

Some things to consider when using multiframe logic analysis systems:

- Use the Overview window to tell which frames are connected and which modules are in each frame.



- When triggering from, or sending a trigger to, an external, non-multiframe instrument, you must use the **Trigger In** or **Trigger Out** BNC connectors on the *master frame*.
- When you arm between modules in different frames, an unused flag line is implicitly used to facilitate the arming. (Flag lines already used in the trigger setup or to arm the external Trigger Out are not used.)
- The *Agilent Notification Center Icon* (lower, right-hand corner of the desktop) will be present when logged onto any standalone instrument. You can double-click this icon to get frame and module details on all frames in the multiframe set. If connected remotely from a PC, this information is available via the Overview window (mentioned above) and the System Summary dialog.

Agilent Logic Analyzer vs. 16700 Terminology

If you are familiar with the 16700-series logic analysis system, note that some of the terminology in the *Agilent Logic Analyzer* application is different:

16700 Term	***Agilent Logic Analyzer*** Term
label	bus or signal (see page 82)
Workspace	Overview window (see page 440)
machine	analyzer, module, and split analyzer (see page 76)
IMB	arming (see page 162) (Advanced Trigger dialog)
Source Correlation Toolset	Source window (see page 437)
Compare tool	Compare window (see page 436)
trigger level	trigger step (see page 138)
trigger *macro* (see page 650)	trigger function (see page 504)
Config	pod assignment (see page 76)
load	open (see page 184)
Filter tool	"Filter/Colorize tool" (in the online help)
Chart tool, Chart display tool, Chart window, chart mode	view waveform bus data as chart (see page 209), or "chart data in VbaView windows" (in the online help)

See Also

- "*Quick Start for 16700-Series Users*"

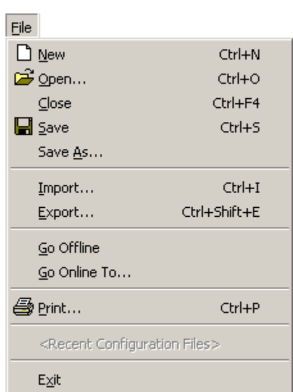
12
Reference

- 16750/51/52 Logic Analyzer Specifications and Characteristics (see page 603)
- 16753/54/55/56 Logic Analyzer Specifications and Characteristics (see page 607)
- 16760 Logic Analyzer Specifications and Characteristics (see page 614)
- 16800-Series Logic Analyzer Specifications and Characteristics (see page 621)
- 16910/11 Logic Analyzer Specifications and Characteristics (see page 628)
- 16950/51 Logic Analyzer Specifications and Characteristics (see page 636)
- 16900-Series Logic Analysis System Frame Characteristics (see page 643)

Menus

- File Menu (see page 405)
- Edit Menu (see page 406)
- View Menu (see page 408)
- Setup Menu (see page 408)
- Tools Menu (see page 410)
- Markers Menu (see page 412)
- Run/Stop Menu (see page 413)
- Overview Menu (see page 413)
- Listing Menu (see page 414)
- Waveform Menu (see page 414)
- Compare Menu (see page 415)
- Source Menu (see page 415)
- PacketViewer Menu (see page 416)
- VbaView Menu (see page 416)
- Window Menu (see page 417)
- Help Menu (see page 418)

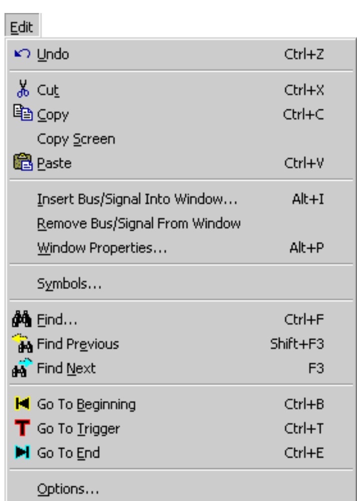
File Menu



New	Creates a new logic analyzer configuration file.
Open...	Opens a previously saved logic analyzer configuration file.
Close	Closes the active window after asking whether to save its data.
Save (see page 171)	Saves changes to the currently open configuration file.

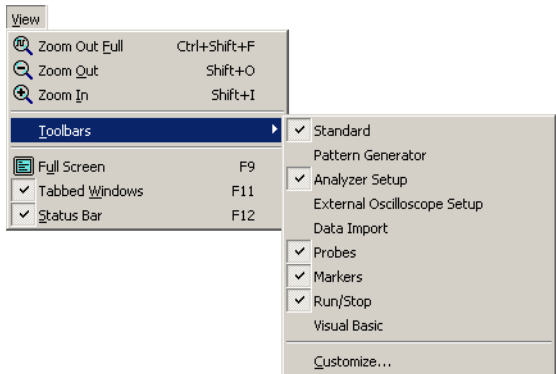
Save As... (see page 171)	Saves the currently open configuration file to a new name.
Import...	Opens the Import Dialog (see page 463) for importing fast binary output data from 16700-series logic analyzers (for offline analysis) or for importing pattern generator stimulus vectors.
Export... (see page 172)	Saves captured data to comma-separated value (CSV) files. CSV files can be imported into spreadsheet, database, or other data analysis programs.
Go Offline	Disconnects the *Agilent Logic Analyzer* application from the currently connected frame.
Go Online To Local Frame	Connects the *Agilent Logic Analyzer* application to the local frame. If there is no local frame, the Offline Startup Options dialog (see page 469) opens.
Go Online To...	Opens the Select System to Use dialog (see page 479) for choosing a frame to connect the *Agilent Logic Analyzer* application to.
Print...	Opens the Printing Data dialog (see page 473) for printing displayed data within a defined range.
Recent Configuration Files (see page 186)	Lists recently opened files for quick reference or access.
Exit	Closes the logic analyzer user interface window.

Edit Menu



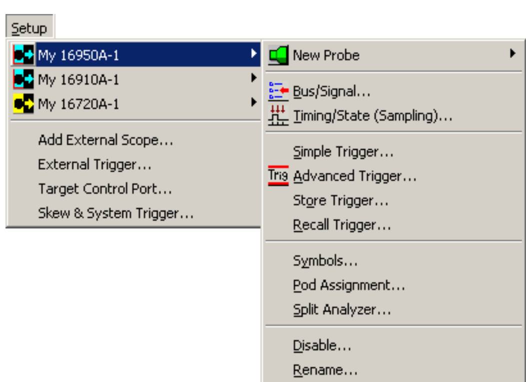
Undo	Undo the last user action. This includes any properties that have changed such as column color, column width, column move, column insert, column delete, etc. Items that cannot be undone include scrolling, acquisition runs and simple trigger modifications.
Cut	Cuts the selection from alphanumeric fields in listing and waveform windows. Alphanumeric fields in lower level modal dialogs are cut using keyboard commands (see page 571) (accelerator keys). Cut selections are pasted to the clip board.
Copy	Copies the selection from alphanumeric fields in listing and waveform windows. Alphanumeric fields in lower level modal dialogs are copied using keyboard commands (see page 571) (accelerator keys). Copied selections are pasted to the clip board.
Copy Screen (see page 307)	Copies the current screen to a bitmap and places it on the system clip board.
Paste	Pastes the cut or copied data that is stored in the clip board into the alphanumeric field. Alphanumeric data is pasted into fields in lower level modal dialogs using keyboard commands (see page 571) (accelerator keys).
Insert Bus/Signal Into Window...	Inserts a predefined bus or signal into the display.
Remove Bus/Signal From Window	Deletes the highlighted bus or signal from the display window.
Window Properties... (see page 475)	Accesses the window properties dialog.
Symbols...	Opens the Symbols dialog (see page 492) for setting up symbols for the selected bus/signal.
Find... (see page 257)	Locates specific data in the acquisition.
Find Previous (see page 257)	Locates the previous occurrence of the specified data.
Find Next (see page 257)	Locates the next occurrence of the specified data.
Go To Beginning (see page 239)	Places the beginning of the captured data trace at center screen.
Go To Trigger (see page 239)	Places the trigger point at center screen.
Go To End (see page 239)	Places the end of the captured data trace at center screen.
Options...	Accesses the System Options dialog (see page 470).

View Menu



Zoom Out Full	Zooms out on an active window as far as possible.
Zoom Out (see page 204)	Zooms out on an active window.
Zoom In (see page 204)	Zooms in on an active window.
Toolbars (see page 420)	Access the Toolbar dialog window.
Full Screen	Enables or disables full screen display.
Tabbed Windows (see page 305)	Enables or disables Listing and Waveform tabs.
Status Bar	Enables or disables the status bar.

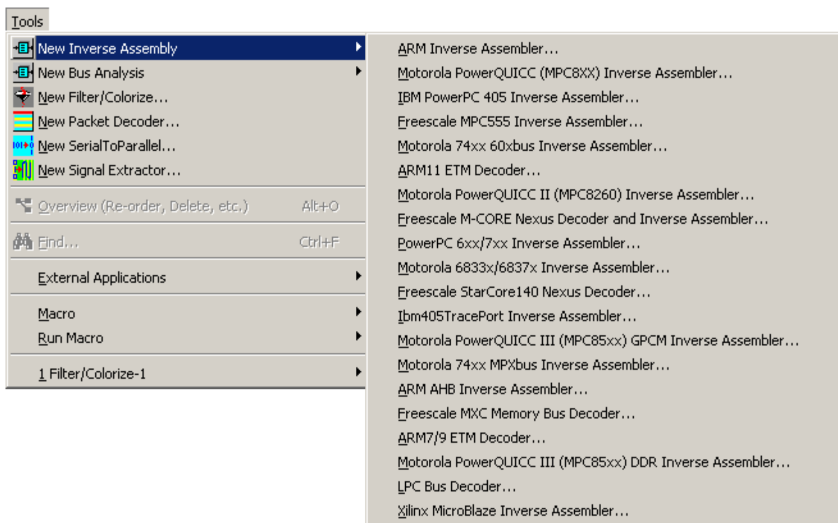
Setup Menu

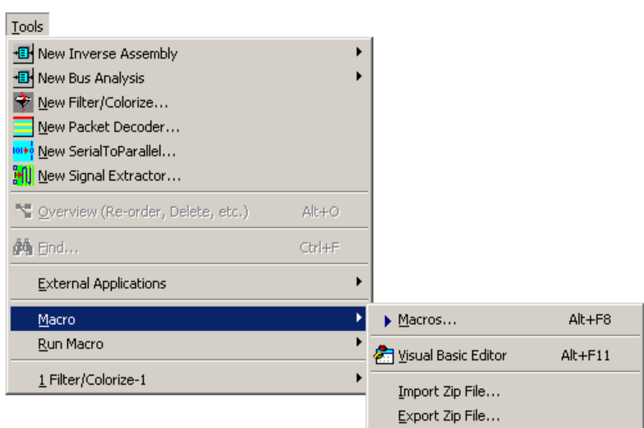


New Probe	Lets you set up the FPGA Dynamic Probe (for probing signals internal to an FPGA) or set up definitions for other probes that are used (see "Setting Up Probes" (in the online help)).
Bus/Signal...	Accesses the Buses/Signals (see page 448) tab of the Analyzer Setup dialog (see page 447).
Timing/State (Sampling)...	Accesses the Sampling (see page 449) tab of the Analyzer Setup dialog (see page 447).
Simple Trigger...	See Specifying Simple Triggers (see page 133).
Advanced Trigger...	Accesses the Advanced Trigger (see page 445) dialog.
Store Trigger...	Stores current trigger.
Recall Trigger... (see page 476)	Accesses a list of most recently used triggers.
Symbols...	Opens the Symbols dialog (see page 492) for setting up symbols for the selected bus/signal.
Pod Assignment...	Opens the Pod Assignment dialog (see page 472) for reserving pods or pod pairs for time tag storage. When a *module* (see page 650) has been split into two modules, this dialog can also be used to re-assign channels to the split modules.
Split Analyzer...	Opens the Split Analyzer Setup dialog (see page 489) for splitting a logic analyzer module into two modules.
Unsplit Analyzer...	This item appears when a logic analyzer module has been split into two modules; it re-combines the split modules (see page 78) into one module.
Disable.../ Enable...	Disabling a module prevents its captured data from being sent to tools and display windows; this will speed up the processing of data from other modules.
Rename...	Lets you rename the logic analyzer module.
" Add External Scope..." (in the online help)	Runs the *Add External Oscilloscope* wizard for connecting an external oscilloscope to the logic analyzer.
Delete External Scope...	Removes the setup for an externally connected oscilloscope.
External Trigger...	Opens the External Trigger dialog (see page 459) for setting up triggers between the logic analyzer and other, external instruments.

Target Control Port...	Opens the Target Control Port dialog (see page 496) for outputting signals on the logic analysis system frame's *target control port*.
Skew & System Trigger...	Opens the Module Skew and System Trigger dialog (see page 468) for specifying which *module* (see page 650) is the *system trigger* (that is, which module's trigger reference point is *Time=0*) and for specifying the trigger reference point skew for modules that are not the *system trigger*.

Tools Menu





All add-in tools are grouped under the tools menu. The *Agilent Logic Analyzer* application comes with a filter/colorize tool built in. If you are using inverse assemblers, bus analysis tools, or other third-party tools, the tools will show up in the Tools menu under New.

As tools are created, they are added to the bottom of the Tools menu. The menus above show one active tool.

New ... (see page 298)	Creates a new inverse assembly, bus analysis, filter/colorize, packet decoder, serial to parallel, or signal extractor tool.
Overview (see page 297)	Lets you manage the active tools.
Find... (see page 257)	Locates specific data in the acquisition.
External Applications>	Lets you run external applications from the *Agilent Logic Analyzer* application's menu. **Setup...** on the submenu opens the External Application Setup dialog (see page 457) that lets you add, edit, arrange, or remove items from the submenu.
Macro>	Lets you: • Open the Macros dialog for "choosing a Visual Basic macro to run" (in the online help). • Open the Visual Basic Editor for "editing programs" (in the online help). • "Import VBA project code from .zip files" (in the online help). • "Export VBA project code to .zip files" (in the online help). For more information, refer to the Visual Basic online help.

Run Macro>	Opens the Add-In Manager dialog which lets you register an add-in (a customized tool that adds capabilities to the Visual Basic development environment), load or unload it, and set its load behavior. For more information, click **Help** in the Add-In Manager dialog.
	Runs a sample macro. As shipped from the factory, the submenu contains:
	• FindEdgesSample (macro for displaying the time between two edges and placing markers on certain edge pairs).
	• RepetitiveSaveToFileSample (macro for saving data from repetitive runs to incrementing file names).
	• SendToExcel (macro for sending logic analyzer data to Microsoft Excel).
	• SendToPatternGeneratorModule (macro for sending logic analyzer data to a pattern generator module as stimulus vectors).
	You can add your own VBA macros to this submenu by placing VBA project code .zip files in the directory:
	`<Drive letter>:\<Install directory>\VBA\`
	For example:
	`C:\Program Files\Agilent Technologies\`
	`Logic Analyzer\VBA\`

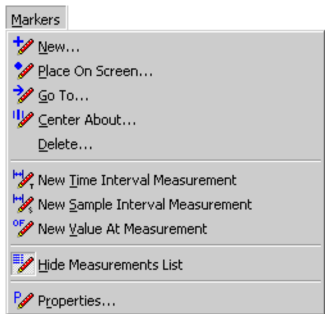
1 *tool name* (see page 300)	Edit an existing tool.

See Also

- To add a new tool (see page 298)
- To change a tool (see page 300)
- To delete a tool (see page 298)

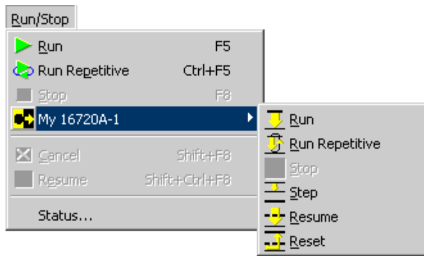
- "Using the Filter/Colorize Tool" (in the online help)

Markers Menu



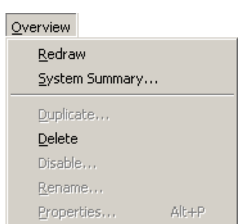
New... (see page 235)	Creates a new marker.
Place on Screen... (see page 237)	Places a new or selected (existing) marker at the middle of the screen.
Go To... (see page 239)	Goes to a selected marker.
Center About... (see page 240)	Centers the display around a selected marker.
Delete...	Deletes selected markers.
New Time Interval Measurement (see page 242)	Creates a new time interval measurement.
New Sample Interval Measurement (see page 243)	Creates a new sample interval measurement.
New Value At Measurement (see page 245)	Creates a new value at measurement.
Hide/Show Measurements List	Hides or shows the marker measurement display bar.
Properties... (see page 247)	Accesses the markers properties dialog

Run/Stop Menu



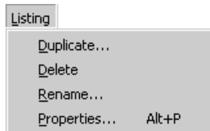
Run	Starts sampling, fills logic analyzer memory with samples around the trigger, and stops.
Run Repetitive	Starts sampling, fills logic analyzer memory with samples around the trigger, and repeats.
Stop	Stops a logic analyzer measurement that is in progress.
(Pattern Generator Module)>	Provides access to the " pattern generator module's run/stop commands" (in the online help).
Cancel	When searching, using a filter, or exporting captured data, Cancel stops the operation.
Resume	If you have used Cancel to stop a filter tool operation, Resume continues the filter operation.
Status...	Accesses the Status dialog (see page 490).

Overview Menu



Redraw	Re-paints the Overview window.
System Summary...	Opens the System Summary dialog (see page 493) which displays information about the *frames* (see page 649), *modules* (see page 650), *cards* (see page 648), and *slots* (see page 653) in the logic analysis system.
Delete	Closes the Overview window.

Listing Menu

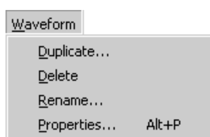


Duplicate...	Adds a new Listing window with the same properties as the window being displayed.
Delete	Closes the Listing window.
Rename...	Lets you rename the Listing window.
Properties...	Lets you change Listing window properties.

See Also

- Analyzing Listing Data (see page 222)
- To set listing window properties (see page 226)

Waveform Menu

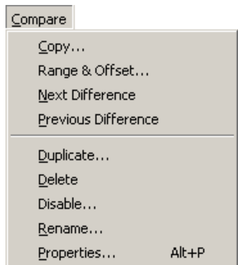


Duplicate...	Adds a new Waveform window with the same properties as the window being displayed.
Delete	Closes the Waveform window.
Rename...	Lets you rename the Waveform window.
Properties...	Lets you change Waveform window properties.

See Also

- Analyzing Waveform Data (see page 203)
- To set waveform window properties (see page 213)

Compare Menu

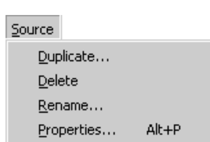


Copy...	Copies data to the reference buffer.
Range & Offset...	Lets you compare a range of samples and offset the reference data.
Next Difference	Finds the next difference (below the center reference).
Previous Difference	Finds the previous difference (above the center reference).
Duplicate...	Adds a new Compare window with the same properties as the window being displayed.
Delete	Closes the Compare window.
Disable..., Enable...	Lets you disable or re-enable the Compare window.
Rename...	Lets you rename the Compare window.
Properties...	Lets you change Compare window properties.

See Also

- Compare Display Window (see page 436)
- Comparing Captured Data to Reference Data (see page 268)
- To set Compare window properties (see page 270)

Source Menu



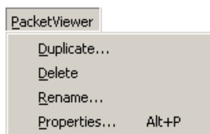
Duplicate...	Adds a new Source window with the same properties as the window being displayed.
Delete	Closes the Source window.

Rename...	Lets you rename the Source window.
Properties...	Lets you change Source window properties.

See Also

- Source Display Window (see page 437)
- Viewing Source Code Associated with Captured Data (see page 272)
- To set Source window properties (see page 277)

PacketViewer Menu

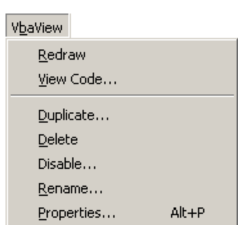


Duplicate...	Adds a new PacketViewer window with the same properties as the window being displayed.
Delete	Closes the PacketViewer window.
Rename...	Lets you rename the PacketViewer window.
Properties...	Lets you change PacketViewer window properties.

See Also

- Packet Viewer Display Window (see page 438)
- Analyzing Packet Data (see page 280)
- Changing Packet Viewer Window Properties (see page 290)

VbaView Menu



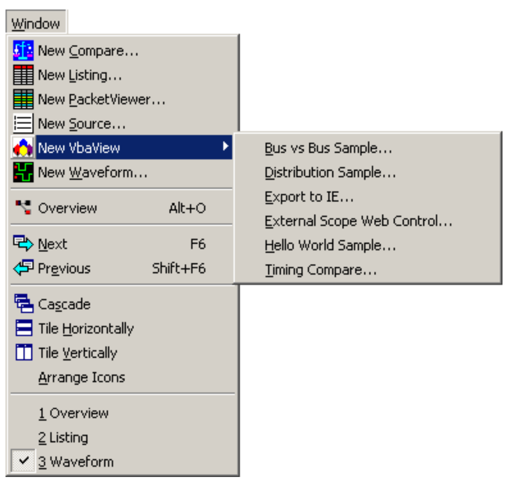
Redraw	Redraws the chart in the VbaView window.
View Code...	Views the code associated with the VbaView window in the Visual Basic Editor.

Duplicate...	Adds a new VbaView window with the same properties as the window being displayed.
Delete	Closes the VbaView window.
Disable..., Enable...	Lets you disable or re-enable the VbaView window.
Rename...	Lets you rename the VbaView window.
Properties...	Lets you change VbaView window properties.

See Also

- VbaView Window (see page 439)

Window Menu

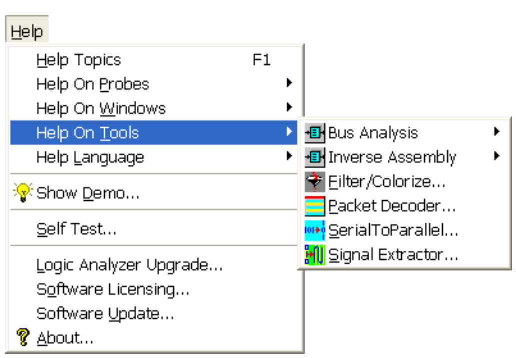


New Compare...	Creates a new Compare window (see page 436).
New Listing...	Creates an additional Listing window (see page 433).
New PacketViewer...	Creates an additional Packet Viewer window (see page 438).
New Source...	Creates a new Source window (see page 437).

New VbaView>	Creates a new VbaView window (see page 439) and populates it with custom code. As shipped from the factory, the submenu contains:
	• Bus vs Bus Sample... (simple XY scattergram chart example).
	• Distribution Sample... (simple data distribution bar chart example).
	• Export to IE Sample... (simple export data to another application example).
	• External Scope Web Control... (opens web control window for external oscilloscope).
	• Hello World Sample... (simple text output example).
	• Timing Compare... (compares timing analyzer data with a specified tolerance).
	You can add your own VbaView windows (and code) to this submenu by placing VBA project code .zip files in the directory:
	`<Drive letter>:\<Install directory>\VBA\`
	For example:
	`C:\Program Files\Agilent Technologies\ Logic Analyzer\VBA\`

New Waveform...	Creates an additional Waveform window (see page 427).
Overview	Opens or displays the Overview window (see page 440).
Next	Displays the next window.
Previous	Displays the previous window.
Cascade	Displays all opened windows in an overlaid and offset format.
Tile Horizontally	Displays all opened windows so the horizontal display space is equally divided.
Tile Vertically	Displays all opened windows so the vertical display space is equally divided.
Arrange Icons	All minimized listing and waveform windows are arranged at the bottom of the analyzer window.

Help Menu



Help Topics	Accesses the online help.
Help On Probes	Opens online help for probes.
Help On Windows	Opens online help for the Waveform, Listing, Compare, or Source windows.
Help On Tools	Opens online help for tools.
Help Language	Lets you choose between the English and Japanese versions of the online help (see Accessing Japanese Online Help (Windows XP) (see page 347) or Accessing Japanese Online Help (Windows 2000) (see page 350)).
Show Demo...	Launches the Demo Center (see page 56) application that demonstrates logic analysis system features.
Self Test...	Accesses the Logic Analyzer Self-Tests dialog (see Running Self Tests (see page 345)).
Logic Analyzer Upgrade...	Accesses the Agilent Logic Analyzer Upgrade dialog (see page 446) which provides information for upgrading hardware in logic analyzer modules.
Software Licensing...	Opens the Software Licensing dialog (see page 481) for managing software licenses used by the logic analysis system.
Software Update...	Opens the Add or Remove Agilent Logic Analyzer Software (see page 319) tool for managing your logic analyzer software and keeping it up to date.
About...	Displays product version and copyright information.

Toolbars

Toolbars are located under the menu bar, and are used to quickly access a function or perform a task. By default, not all toolbars, or individual tools within a given toolbar are displayed. For a complete list of all available toolbars, choose **View>Toolbars>**. For a complete list of all tools within a given toolbar, choose **View>Toolbars>Customize...**; then, select the **Commands** tab in the Customize dialog.

- Standard (see page 420)
- Pattern Generator (see page 421)
- Analyzer Setup (see page 422)
- External Oscilloscope Setup (see page 422)
- Data Import (see page 422)
- Probes (see page 423)
- Markers (see page 423)
- Run/Stop (see page 424)
- Visual Basic (see page 424)
- Customize... (see page 424)

Standard Toolbar

	New - Creates a new logic analyzer configuration file.
	Open - Opens a previously saved logic analyzer configuration file.
	Save - Saves changes to the currently open configuration file.
	Print (see page 473) - Prints displayed data within a defined range.
	Find (see page 257) - Locates specific data in the acquisition.
	Find Previous (see page 257) - Locates the previous occurrence of the specified data.
	Find Next (see page 257) - Locates the next occurrence of the specified data.
	Go to Beginning (see page 239) - Centers the beginning of the acquisition data.
	Go to Trigger (see page 239) - Centers the trigger point of the acquisition.
	Go to End (see page 239) - Centers the end of the acquisition data.
	Zoom Out (see page 204) - Zooms in on an active window.

	Zoom In (see page 204) - Zooms out on an active window.
	Overview - Opens or displays the Overview window (see page 440).

NOTE The following are optional standard toolbar icons.

	Cuts the selection and places it on the clip board.
	Copies the selection and places it on the clip board.
	Pastes the data that is stored on the clip board.
	Provides online help information about the *Agilent Logic Analyzer* application.
	Undo last user action.
	Enables or disables full screen display.
	Activate the next window.
	Activates the previous window.
	Arranges windows as cascaded overlapping tiles.
	Arranges windows as non-overlapping horizontal tiles.
	Arranges windows as non-overlapping vertical tiles.

See Also

- To create a custom toolbar (see page 424)

Pattern Generator Toolbar

	Sets up the pattern generator bus/signal attributes attributes.
	Sets up the pattern generator clocking attributes.
	Sets up the pattern generator sequence.
	Sets up the pattern generator macros.
	Runs the pattern generator.
	Runs the pattern generator repetitively.
	Stops the pattern generator.
	Steps through the pattern generator vector sequence.

	Resumes pattern generator vector sequence output.
	Resets the pattern generator vector sequence to the beginning.

See Also

- "Using the Pattern Generator" (in the online help)

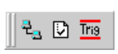
Analyzer Setup Toolbar

	Bus/Signal - Accesses the Buses/Signals (see page 448) tab of the Setup dialog.
	Timing/State (Sampling) - Accesses the Sampling (see page 449) tab of the Setup dialog.
	Advanced Trigger - Accesses the Advanced Trigger (see page 445) dialog.

See Also

- To create a custom toolbar (see page 424)

External Oscilloscope Setup Toolbar

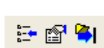


	Sets up the external oscilloscope connection attributes.
	Sets up the external oscilloscope option attributes.
	Sets up the external oscilloscope trigger attributes.

See Also

- "Infiniium Oscilloscope Time Correlation" (in the online help)

Data Import Toolbar



	Lets you edit the data import module bus/signal definitions.
	Displays data import module file information.
	Re-reads the data import module file.

See Also • Using Data Import Modules (see page 191)

Probes Toolbar

	Opens the properties dialog for a particular probe. • "Using the Xilinx FPGA Dynamic Probe" (in the online help) • "Using the FPGA Dynamic Probe for Altera FPGAs" (in the online help) • "Using General Purpose Probes" (in the online help) • "PCI Express Analysis Probe" (in the online help) • "Serial ATA Analysis Probe" (in the online help)

Markers Toolbar

	New (see page 235) - Creates a new marker.
	Go To (see page 239) - Centers the display around the selected marker.
	Creates a new value at a measurement (see page 245).
	Creates a new time interval measurement (see page 242).

NOTE The following are optional markers toolbar icons.

	Place Maker (see page 237) - Places a new or selected (existing) marker at the middle of the screen.
	Center About (see page 240) - Centers the display around two selected markers.
	Creates a new sample interval measurement (see page 243).
	Hides or shows the marker measurement display bar.
	Accesses the markers properties (see page 247) dialog.

See Also • To create a custom toolbar (see page 424)

Run/Stop Toolbar

	Starts sampling, fills logic analyzer memory with samples.
	Starts Sampling, fills logic analyzer memory with samples around the trigger, and repeats.
	Stops a logic analyzer measurement in progress, for example, when the trigger condition is not found.
	Cancels the current operation.
	Resumes the cancelled operation.

See Also

- To create a custom toolbar (see page 424)

Visual Basic Toolbar

	Runs a Visual Basic for Applications (VBA) macro.
	Opens the Visual Basic Editor.

See Also

- "Using the Advanced Customization Environment (ACE)" (in the online help)

To customize toolbars

- To add icons to a toolbar (see page 424)
- To remove icons from a toolbar (see page 425)
- To create a new toolbar (see page 425)
- To restore a toolbar to its original icons (see page 425)

To add icons to a toolbar

1. From the menu bar, select **View>Toolbars>Customize...**.
2. Select the **Commands** tab.
3. Select the **Category** that you want to add icons from.
4. Drag the desired icon from the **Buttons** area to the desired position on the toolbar; then, release the mouse button to insert the tool icon.
5. Repeat for any other icons you wish to add.

To remove icons from a toolbar

1 From the menu bar, select **View>Toolbars>Customize...**.
2 Select the **Commands** tab.
3 Drag the icon from the toolbar and drop it onto the **Buttons** area of the Customize dialog.
4 Repeat for any other icons you wish to remove.

To create a new toolbar

1 From the menu bar, select **View>Toolbars>Customize...**.
2 In the Customize dialog's Toolbars tab, click **New...**.
3 In the New Toolbar dialog, enter the name of the new toolbar, and click **OK**.
4 Drag the new toolbar window to the desired position in the toolbar dock.

   A second row of toolbars can be created by dragging a toolbar to the bottom of an existing toolbar row.

   If a toolbar is hidden off-screen, drag a visible toolbar to create a second row of toolbars; that should then reveal the hidden toolbar.

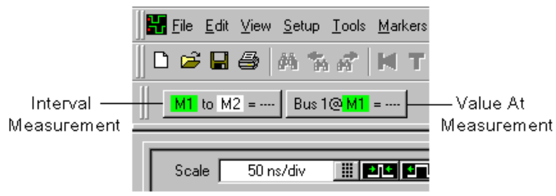
Once you have created a new toolbar, you can add or remove icons as described above.

To restore a toolbar to its original icons

1 From the menu bar, select **View>Toolbars>Customize...**.
2 In the Customize dialog's Toolbars tab, select the name of the **Toolbar** you want to restore.
3 Click **Reset**.

Marker Measurement Display Bar

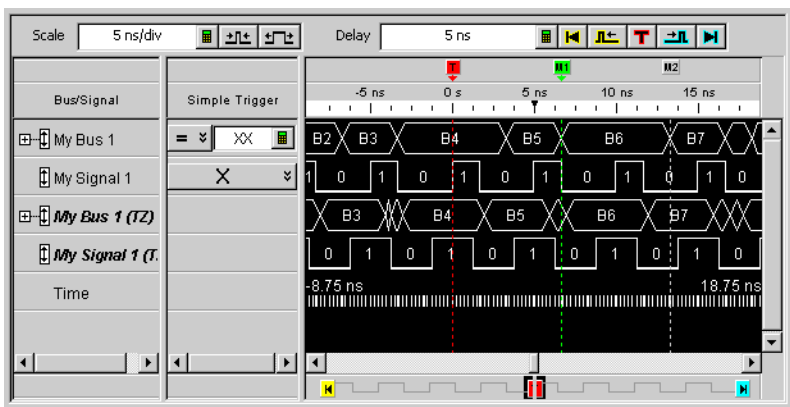
Marker "interval" and "value at" measurements are displayed below the menu bar with the other toolbars.



- To create a new time interval measurement (see page 242)
- To create a new sample interval measurement (see page 243)
- To create a new value at measurement (see page 245)
- To hide/show measurement display bar (see page 412)

Windows

Waveform Display Window



The Waveform window is accessed through the menu bar's **Window>Waveform**. If you have Tabbed Windows (see page 305) turned on, you can also select a tab at the bottom of the window.

The Waveform window displays captured data as a digital waveform. You can configure the window to display selected buses and signals with time or pattern markers in the data. You can also set up bus pattern triggers and signal trigger options.

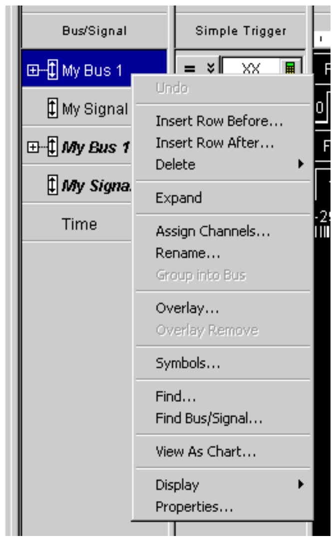
The Waveform window consists of the following areas:

- Bus/Signal Configuration (see page 428)
- Simple Trigger (see page 133)
- Markers Display Bar (see page 431)
- Waveform Display Area (see page 429)
- Markers Overview Bar (see page 432)

- Delay Controls (see page 206)
- Scale (time/division) Controls (see page 204)

Bus/Signal Configuration

To access the following Bus/Signal configuration options, right-click on any bus or signal name in the Bus/Signal column.

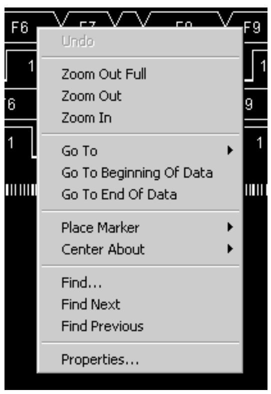


Undo	Undo the last action performed.
Insert Row Before...	Inserts a bus/signal before the highlighted row.
Insert Row After...	Inserts a bus/signal after the highlighted row.
Delete>	Deletes the bus/signal in the highlighted row or deletes all buses/signals.
Expand	Expands the highlighted bus into separate displayed channels.
Collapse	Collapses displayed channels to a single displayed bus.
Assign Channels...	Access to the Buses/Signals tab of the Analyzer Setup dialog for mapping (assigning) the highlighted bus/signal to the desired pod and channel connection of the probes.
Rename...	Access a keypad to rename the highlighted bus/signal.
Group into Bus (see page 212)	Groups highlighted signals into a bus.
Overlay... (see page 207)	Overlays the highlighted bus or signal with another selected bus or signal.
Overlay Remove	Separates overlaid bus/signals.
Symbols...	Opens the Symbols dialog (see page 492) for setting up symbols for the selected bus/signal.

Find...	Opens the Find dialog for searching the captured data (see page 257).
Find Bus/Signal...	Searches for a bus/signal row.
View As Chart... (see page 209)	Opens the View As dialog for viewing the bus data as a chart or a bus.
Display>	Lets you show or hide parts of the Waveform window (see page 211).
Properties... (see page 213)	Access to properties dialog for waveform window, bus/signal row, bus/signal column, and marker properties.

Waveform Display Area

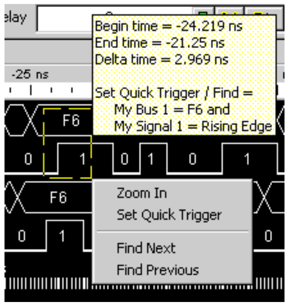
To access waveform display options, right-click anywhere in the display area.



Undo	Undo the last action performed.
Zoom Out (see page 204)	
Zoom In (see page 204)	
Go To (see page 206)	
Place Marker> (see page 237)	
Center About>	Centers the display about a marker pair (see page 240) or waveform edges (see page 205).
Find... (see page 257)	
Find Next (see page 257)	

Find Previous (see page 257)	
Properties... (see page 213)	

Drawing Rectangle in Data

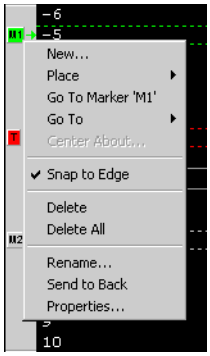


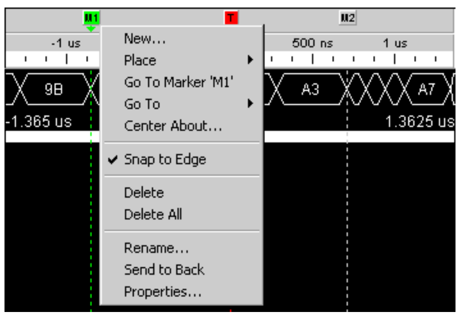
Zoom In (see page 205)	
Set Quick Trigger (see page 129)	Alternative way to set a Simple Trigger.
Find Next	Data value on left edge of rectangle becomes Find search (see page 257) criteria and next occurrence of that data value is placed at center screen.
Find Previous	Data value on left edge of rectangle becomes Find search (see page 257) criteria and previous occurrence of that data value is placed at center screen.

See Also

- Analyzing Waveform Data (see page 203)
- Marking, and Measuring Between, Data Points (see page 234)
- Specifying Advanced Triggers (see page 138)
- Setting Up Symbols (see page 116)
- To add or delete display windows (see page 305)
- To turn window tabs on/off (see page 305)

Markers Display Bar





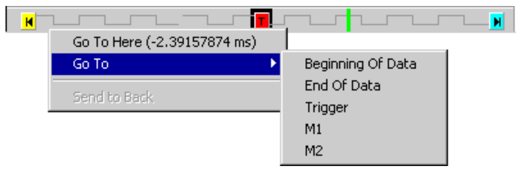
To access these tasks, right-click anywhere in the marker display bar.

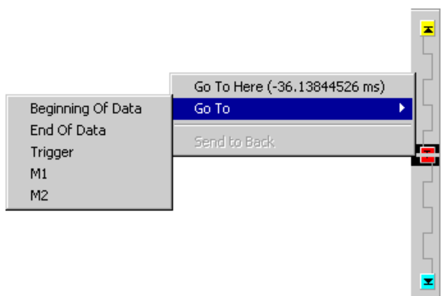
New... (see page 235)	To create new markers.
Place (see page 237)	To place markers in data.
Go To (see page 239)	To go to a marker.
Center About... (see page 240)	To center the display about a marker pair.
Snap to Edge (see page 240)	To toggle a marker's snap to edge property.
Delete (see page 241)	To delete a marker.
Delete All (see page 241)	To delete all markers.
Rename... (see page 245)	To rename a marker.
Send to Back (see page 246)	To send a marker to the back.
Properties... (see page 247)	To set marker properties.

See Also

- To read the markers display and overview bars (see page 235)
- Markers Menu (see page 412)
- Markers Toolbar (see page 423)
- Markers Overview Bar (see page 432)

Markers Overview Bar





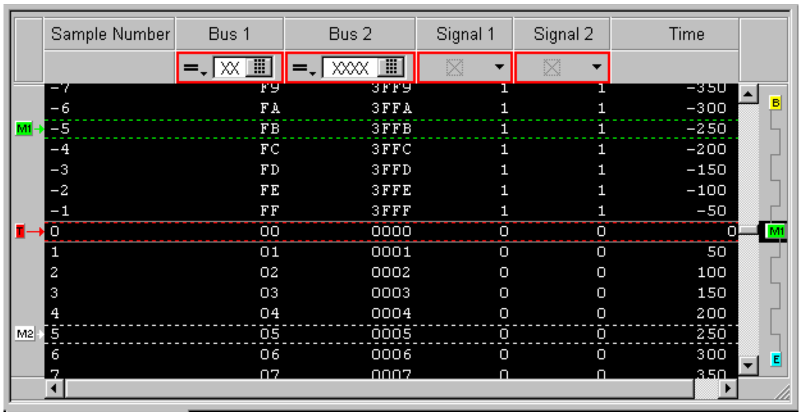
To access these menus, click anywhere in the marker overview bar.

Go To (see page 239)	To go to a marker.
Send to back (see page 246)	To send a marker to the back.

See Also

- To read the markers display and overview bars (see page 235)
- Markers menu (see page 412)
- Markers toolbar (see page 423)

Listing Display Window



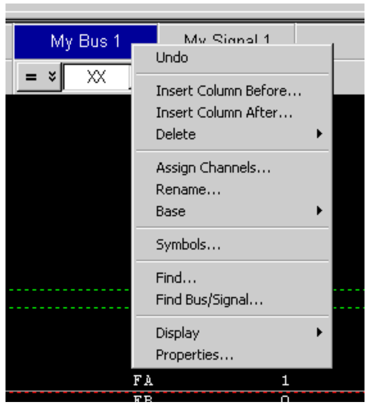
The Listing window is accessed through the menu bar's **Window>Listing**. If you have Tabbed Windows (see page 305) turned on, you can also select a tab at the bottom of the window.

The Listing window displays your captured data as a state listing. You configure the window to display selected buses and signals in columns. Within the listed data, you can insert time or pattern markers. You can also configure the bus pattern triggers and signal trigger options.

The Listing window consists of the following areas:

- Column Configuration (see page 433)
- Simple Trigger (see page 133)
- Markers Display Bar (see page 431)
- Listing Display Area (see page 434)
- Markers Overview Bar (see page 432)

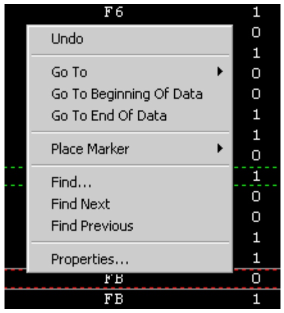
Column Configuration To access the following column configuration options, right-click on any bus or signal name in the column head.



Undo	Undo the last action performed.
Insert Column Before... (see page 225)	
Insert Column After... (see page 225)	
Delete> (see page 225)	
Assign Channels... (see page 82)	
Rename...	Access a keypad to rename the highlighted bus/signal.
Base> (see page 230)	
Symbols...	Opens the Symbols dialog (see page 492) for setting up symbols for the selected bus/signal.
Find...	Opens the Find dialog for searching the captured data (see page 257).
Find Bus/Signal...	Searches for a bus/signal column.
Display>	Lets you show or hide parts of the Listing window (see page 225).
Properties... (see page 226)	Access to properties dialog for Listing window, bus/signal column, and marker properties.

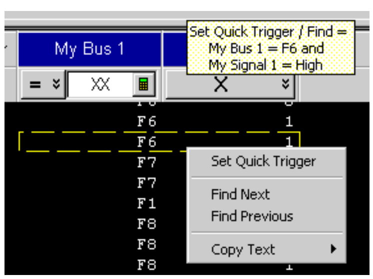
Listing Display Area

To access the Listing display options, right-click anywhere in the display area.



Undo	Same as Edit>Undo (see page 406).
Go To (see page 223)	
Place Marker> (see page 237)	
Find... (see page 257)	
Find Next (see page 257)	
Find Previous (see page 257)	
Properties... (see page 226)	

Draw Rectangle in Data

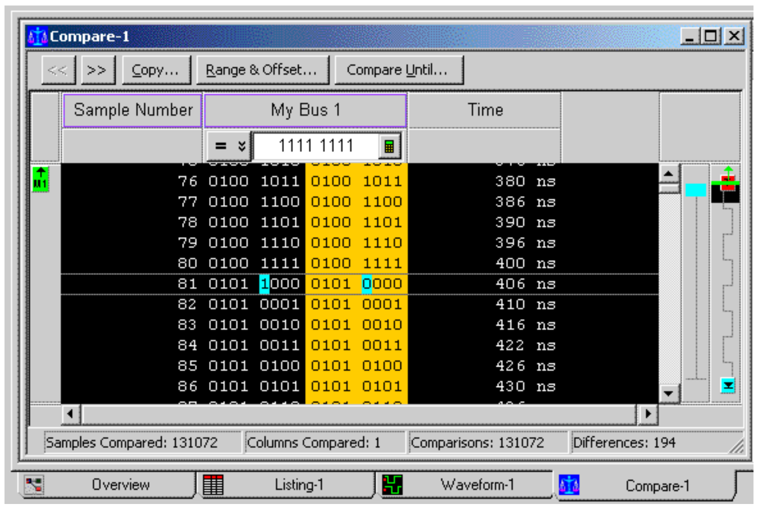


Set Quick Trigger (see page 129)	Alternative way to set a simple trigger.
Find Next	Data value on top edge of rectangle becomes Find search (see page 257) criteria and next occurrence of that data value is placed at center screen.
Find Previous	Data value on top edge of rectangle becomes Find search (see page 257) criteria and previous occurrence of that data value is placed at center screen.
Copy Text (see page 306)	Copies data as text into the system clip board.

See Also

- Analyzing Listing Data (see page 222)
- Setting Up Symbols (see page 116)
- Marking, and Measuring Between, Data Points (see page 234)
- To add or delete display windows (see page 305)
- To turn window tabs on/off (see page 305)

Compare Display Window



The Compare window lets you compare acquired (input) data to data that has been saved in a reference buffer. The reference data has a colored background, and differences between between the input data and the reference data are highlighted.

The Compare window is accessed through the menu bar's **Window>Compare**. If you have Tabbed Windows (see page 305) turned on, you can also select a tab at the bottom of the window.

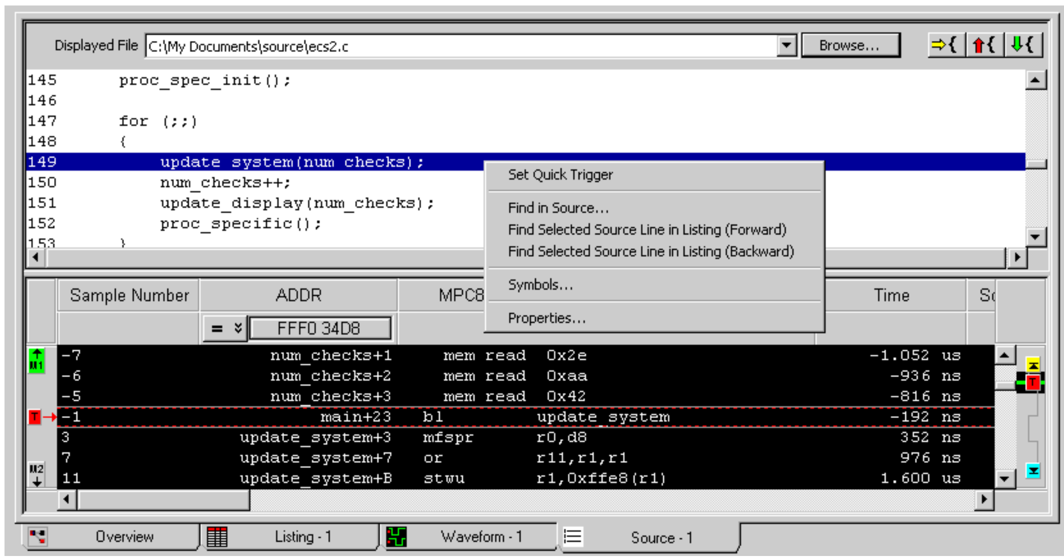
Except for the Compare window's ability to display the differences between captured data and reference data, and its inability display colorized data (from the Filter/Colorize tool), the Compare window is just like the Listing window.

See Also

- Comparing Captured Data to Reference Data (see page 268)
  - To copy data to the reference buffer (see page 268)
  - To find differences in the compared data (see page 269)
  - To compare only a range of samples (see page 269)
  - To offset the reference data (see page 270)
  - To run until a number of compare differences (see page 270)

- To set Compare window properties (see page 270)
- Analyzing Listing Data (see page 222)

Source Display Window



The Source window lets you view the high-level source code that is associated with captured data.

The Source window is accessed through the menu bar's **Window>Source** command. If you have Tabbed Windows (see page 305) turned on, you can also select a tab at the bottom of the window.

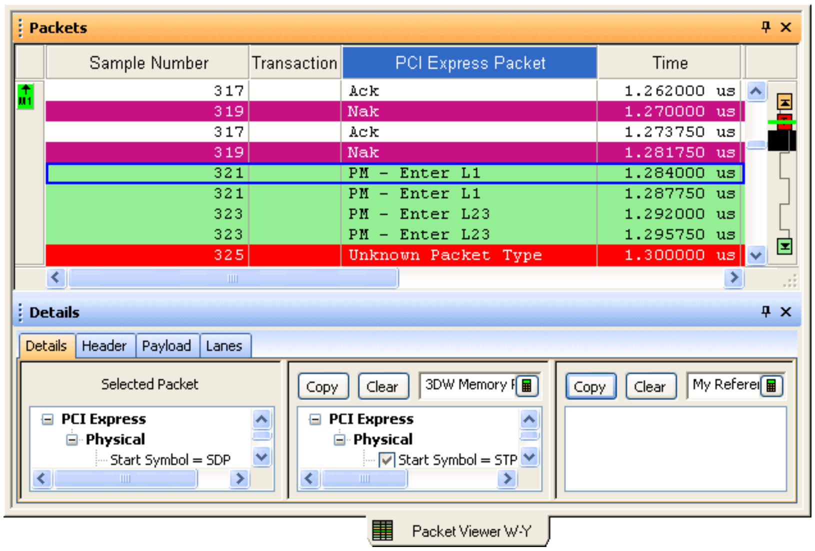
The Source window has two panes: the top pane displays the high-level source code associated with the captured data, and the bottom pane is the same as a Listing window.

See Also

- Viewing Source Code Associated with Captured Data (see page 272)
  - To step through captured data by source lines (see page 273)
  - To go to captured data associated with a source line (see page 273)
  - To browse source files (see page 274)
  - To search for text in source files (see page 274)
  - To set a Quick Trigger in the Source window (see page 131)
  - To go to the source line associated with the listing center rectangle (see page 275)
  - To edit the source code directory list (see page 275)
  - To select the correlation bus (see page 276)
  - Changing Source Window Properties (see page 277)

- Analyzing Listing Data (see page 222)

Packet Viewer Display Window



You can use a Packet Viewer window to display data from a Packet Decoder tool.

Unlike the Listing window, the Packet Viewer window lets you view summarized and detailed packet information at the same time within two *panes*.

The upper packet summary pane is similar to a Listing window except that its columns display decoded packets and fields instead of bus/signal values. Like a Listing window, you can insert time or pattern markers.

The lower pane contains tabs for viewing selected packet details, header, payload, and lane information.

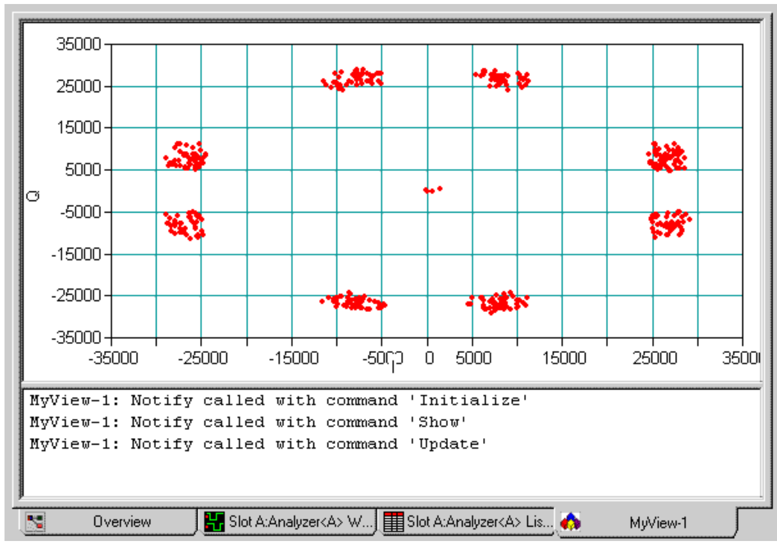
The Packer Viewer window is customized for the protocol family being decoded.

The Packet Viewer window is accessed through the menu bar's **Window>Packet Viewer** items. If you have Tabbed Windows (see page 305) turned on, you can also select a tab at the bottom of the window.

See Also

- Analyzing Packet Data (see page 280)
  - Viewing the Packet Summary (see page 228)
  - Viewing a Selected Packet (see page 285)
  - Changing Packet Viewer Window Properties (see page 290)
  - Changing Packet Summary Column Properties (see page 228)

VbaView Window



The VbaView window works with the integrated Microsoft Visual Basic for Applications (VBA) to provide custom data visualization charts.

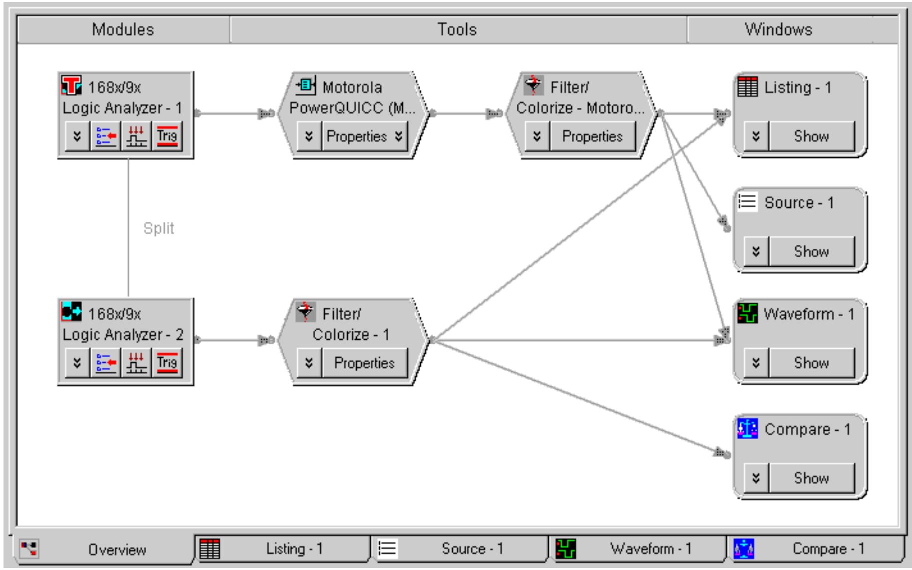
The VbaView window is accessed through the menu bar's **Window>VbaView** command. If you have Tabbed Windows (see page 305) turned on, you can also select a tab at the bottom of the window.

The VbaView window has two panes: the top pane displays the chart, and the bottom pane displays text output.

See Also

- Extending Data Visualization/Analysis with VBA (see page 309)
- "Displaying Data in VbaView Windows" (in the online help)

Overview Window



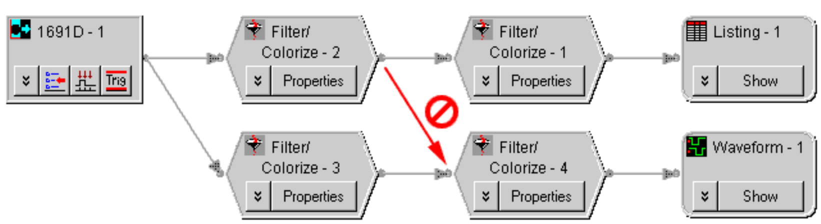
The Overview window lets you specify how the data is sent from the logic analyzer data acquisition module to post-processing tools and display windows.

The Overview window is accessed through the menu bar's **Window>Overview** command. If you have Tabbed Windows (see page 305) turned on, you can also select a tab at the bottom of the window.

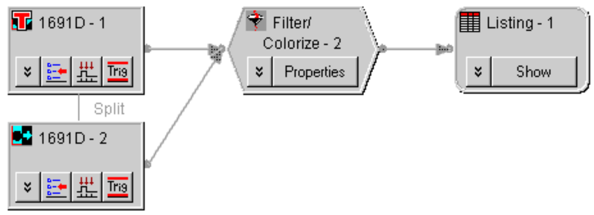
Connection Rules

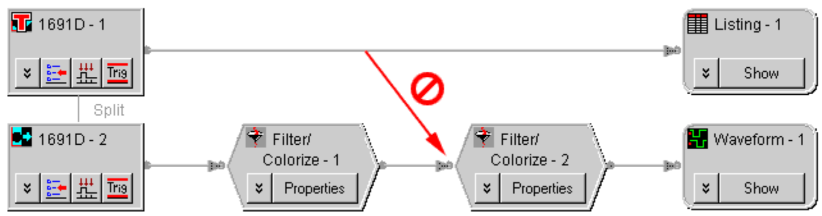
There are a few rules that govern how you are able to add/connect tools and display data.

- **Rule 1: Fan out to tools only occurs directly after modules.**

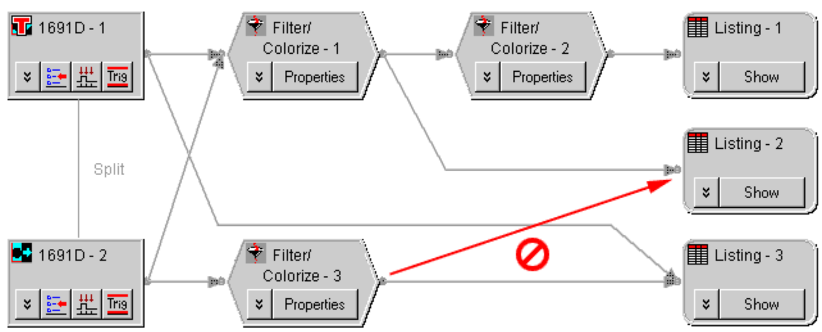


- **Rule 2: Fan in to tools occurs only directly after modules.**





- **Rule 3: Display windows cannot show two versions of the same bus/signal.**



Not allowed because "1691D - 2" buses/signals already in data from "Filter/Colorize - 1".

See Also

- Analyzing the Same Data in Different Ways (Using the Overview Window) (see page 297)
- To open or display the Overview window (see page 297)
- To add, duplicate, or delete windows and tools (see page 298)
  - To add new windows (see page 298)
  - To delete windows (see page 298)
  - To add new tools (see page 299)
  - To delete tools (see page 299)
  - To duplicate windows (see page 299)
  - To delete connections (see page 300)

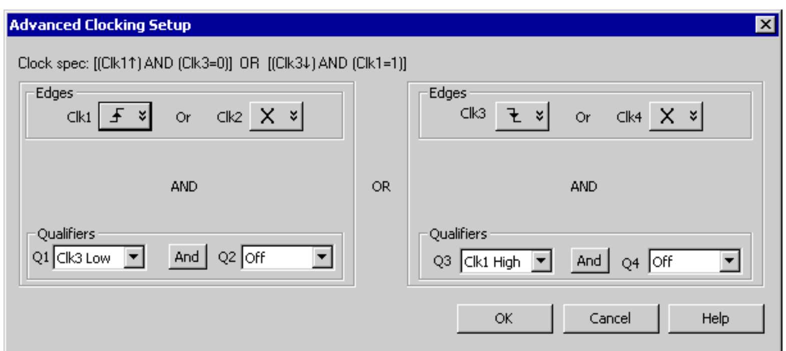
    - To add connections (see page 300)
- To edit window or tool properties (see page 300)
- To rename windows, tools, and modules (see page 301)
- To redraw the Overview window (see page 302)
- To delete the Overview window (see page 302)

Dialogs

- Software Licensing Dialog (see page 481)
- Source Viewer Properties Dialog (see page 486)
- Specify Mapping Dialog (see page 488)
- Split Analyzer Setup Dialog (see page 489)
- Status Dialog (see page 490)
- Symbols Dialog (see page 492)
- System Summary Dialog (see page 493)
- Target Control Port Dialog (see page 496)
- Thresholds and Sample Positions Dialog (see page 497)
- TimingZoom Setup Dialog (see page 502)

Advanced Clocking Setup Dialog

The Advanced Clocking Setup dialog lets you specify more complex clock setups than you can with the normal Master or Slave selections. If you want to use a specific clock channel both as an edge and a qualifier in the same clock description, you need to use advanced clocking.



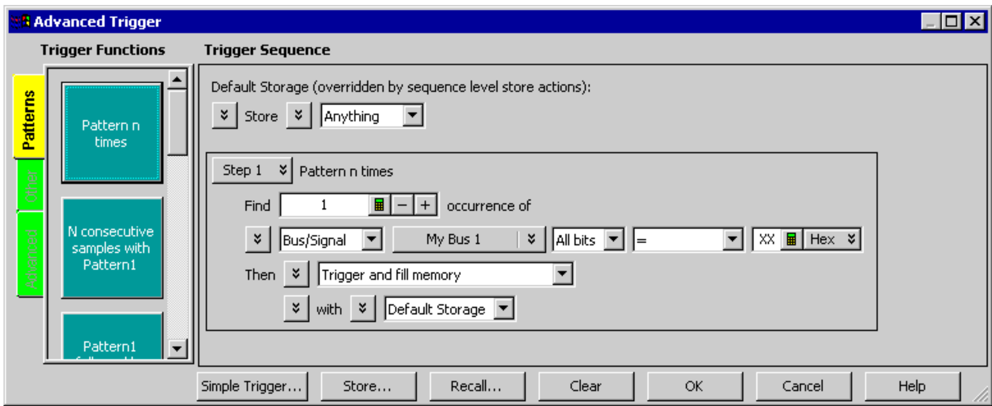
Clock spec:	A textual description of the clocking setup.
Edges	Lets you choose from **Don't Care**, **Rising Edge**, **Falling Edge**, or **Both Edges** for each of the available clock inputs.
Qualifiers	Lets you turn **Off** clock qualifiers or select **Low** or **High** levels from the available clock inputs for each of the clock qualifier resources (Q1-Q4).
And/Or	Lets you toggle the boolean operators for the clock qualifiers.

See Also

- To set up advanced clocking (see page 107)
- Pod and Channel Naming Conventions (see page 372)

Advanced Trigger Dialog

The Advanced Trigger dialog lets you set up complex trigger specifications that cannot be set up with simple triggers (for example, you can trigger on a sequence of events in the device under test).



Trigger Functions	Trigger functions are pre-defined trigger setups for common measurements. Trigger functions are drag-and-dropped into the Trigger Sequence area in the desired order; then, you fill-in the fields that specify the *events* to look for in the sampled data and the *actions* to take when the events are found.
Trigger Sequence	The trigger sequence describes the steps to take when searching for a sequence of events that will trigger the logic analyzer. *Default storage* specifies which samples to store unless there are overriding *storage control* actions within the trigger sequence steps.
Simple Trigger...	Opens an information dialog that explains how to specify simple triggers (see page 133).
Store...	Opens the Store Trigger dialog for saving a trigger sequence setup as a favorite or saving it to a file.
Recall...	Opens the Recall Trigger dialog (see page 476) for recalling favorite, recently used, and stored trigger sequence setups.
Clear	Clears the current trigger sequence and sets up a default trigger sequence.

See Also

- Specifying Advanced Triggers (see page 138)
- Trigger Functions (see page 504)
- Specifying Simple Triggers (see page 133)
- Storing and Recalling Triggers (see page 166)

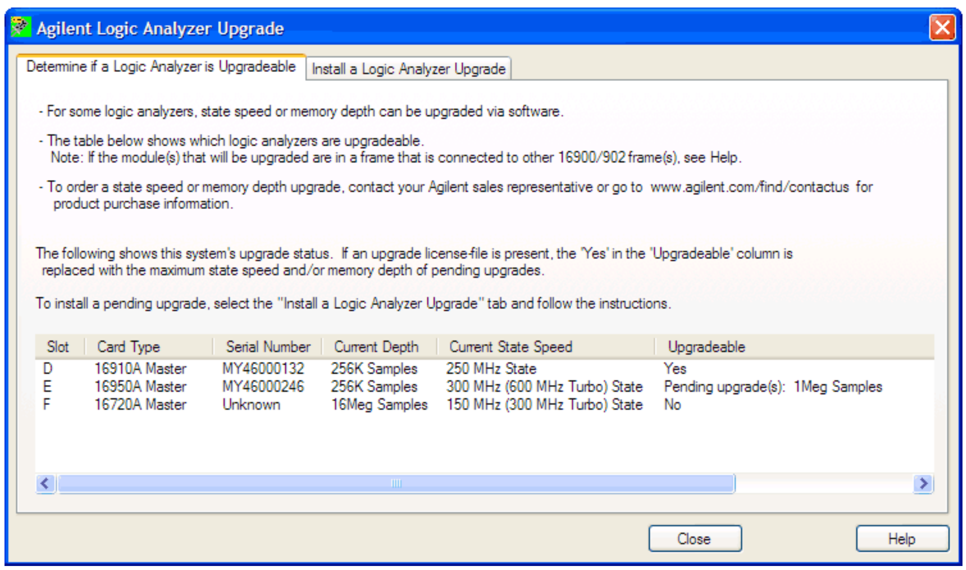
Agilent Logic Analyzer Upgrade Dialog

NOTE

When installing licensed hardware upgrades, you must run the *Hardware Update Utility* program on the frame that contains the cards you want to upgrade. In other words:

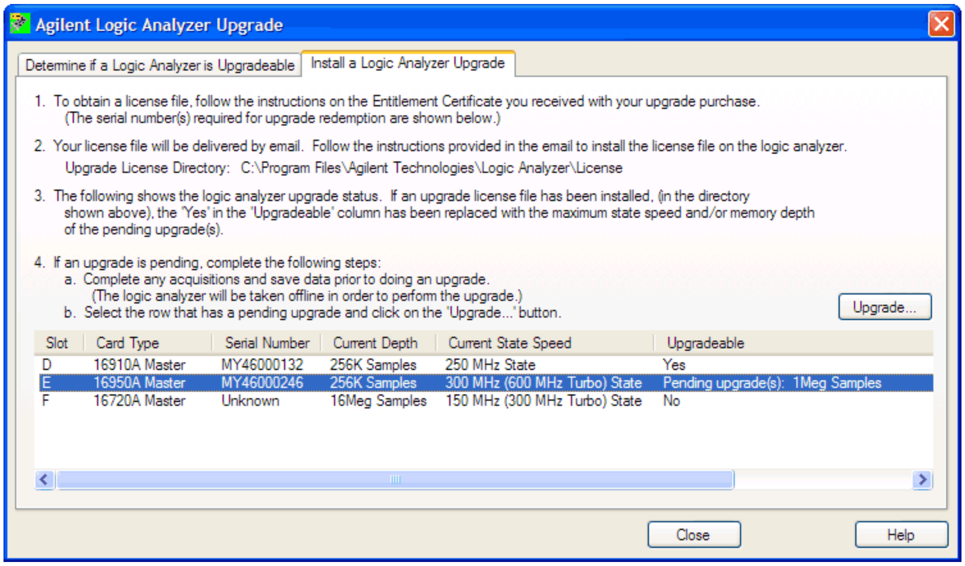
- In a multiframe logic analysis system, you must run the *Hardware Update Utility* program on each frame that has cards to be upgraded.
- You cannot install module upgrades over a remote connection (including remote connections via Remote Desktop, NetOp, or RealVNC).

Determine if a Logic Analyzer is Upgradeable Tab



This tab lists the logic analyzers and other cards in a frame and shows you whether they are upgradeable or if an upgrade is pending.

Install a Logic Analyzer Upgrade Tab

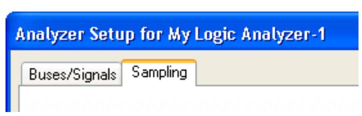


Upgrade...	Performs the pending upgrade for the selected card.

See Also

- Installing Licensed Hardware Upgrades (see page 124)

Analyzer Setup Dialog



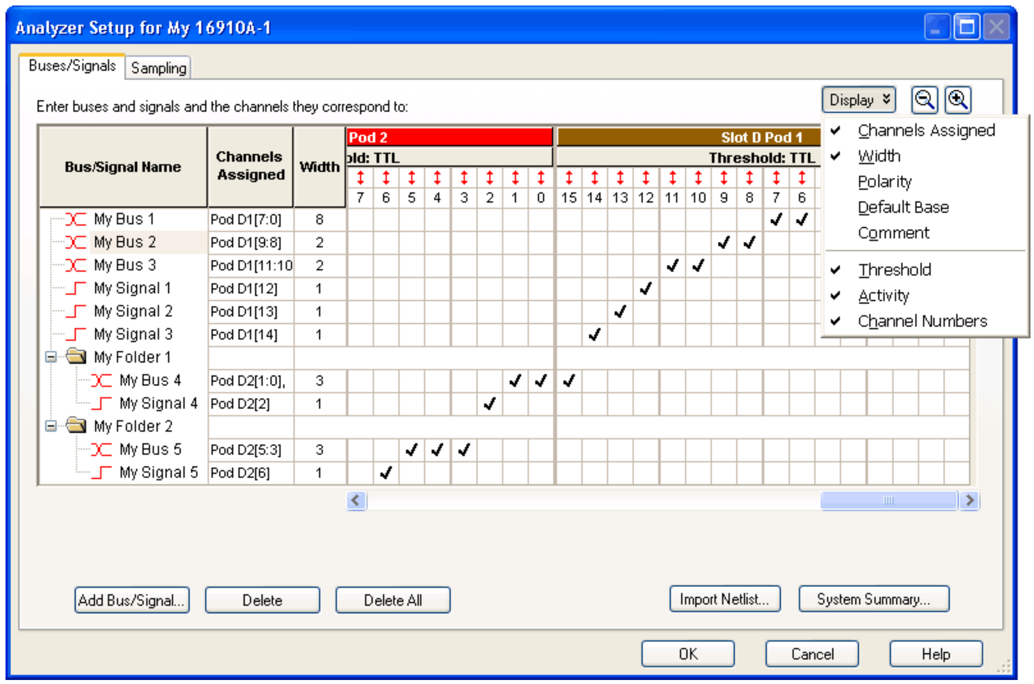
The Analyzer Setup dialog is accessed through the main menu's **Setup>(Logic Analyzer Module)>Bus/Signal...** or **Setup>(Logic Analyzer Module)>Timing/State (Sampling)...** commands.

The dialog consists of the following two tabs.

- **Buses/Signals** - The Buses/Signals tab is used to map bus and signal names in the interface to the pod and channel connections of the probes. Also, you can set a pod threshold, and assign a default number base and polarity to the bus or signal. See Buses/Signals Tab (see page 448).
- **Sampling** - The Sampling tab is used to name the analyzer, and select and configure the acquisition mode. In the timing acquisition mode, you set the channel width and sampling rate. In the state acquisition mode you configure the state clocks and qualifiers. See Sampling Tab (see page 449).

Buses/Signals Tab

The Buses/Signals tab is used to map (assign) bus and signal names in the interface to the pod and channel connections of the probes. You also use the Buses/Signal tab to set up thresholds, polarity, default number base, and enter user comments.



The Buses/Signals tab is accessed through the menu bar's **Setup>(Logic Analyzer Module)>Bus/Signal...** command.

Through the **Display** button, you can select what bus/signal setup information is displayed.

The bus and signal icons in the **Bus/Signal Name** column are normally red, but they turn gray if the bus/signal is locked by an inverse assembler.

Read Only Options The following fields are read only and cannot be edited. The display of these items can be turned on/off under the **Display** button.

Width	The Width column displays the number of assigned channels on each bus.
Activity	The Activity row displays the type of signal activity on each channel. • Low bar = A stable low level. • High bar = A stable high level. • Transition arrows = An active signal transition between low and high.
Channel Numbers	The Channel Numbers row displays pod channel numbers

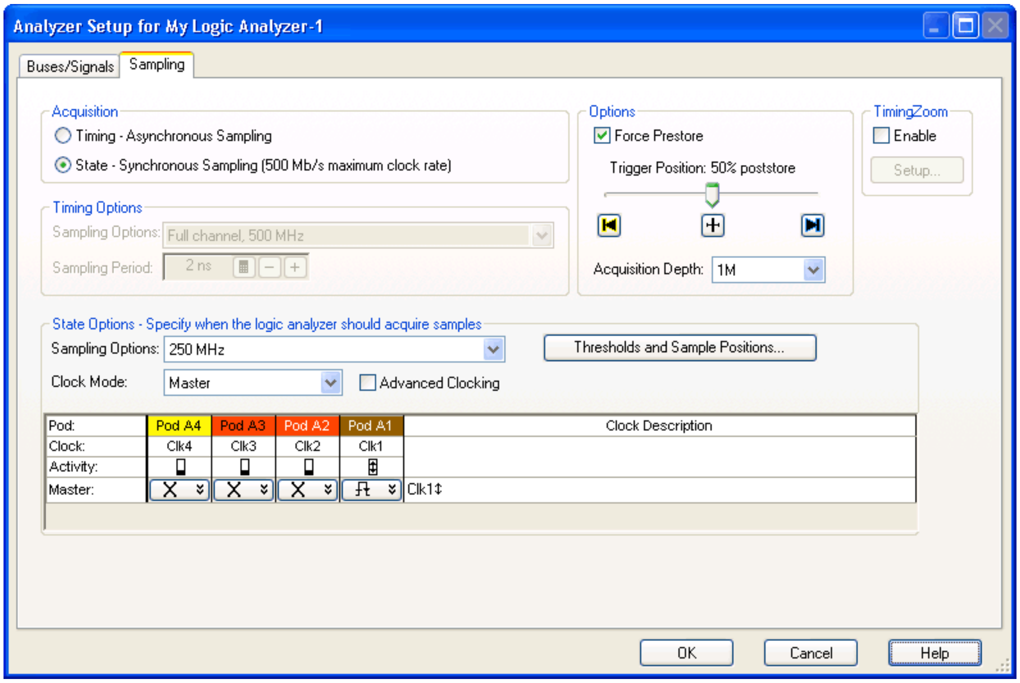
NOTE In previous versions of the *Agilent Logic Analyzer* application, the Buses/Signals setup tab had a **Define Probes...** button; now, probes are defined differently (see "To define probes" (in the online help)).

See Also

- Defining Buses and Signals (see page 82)
  - To add a new bus or signal (see page 83)
  - To delete a bus or signal (see page 84)
  - To rename a bus or signal (see page 85)
  - To assign channels in the default bit order (see page 88)
  - To assign channels, selecting the bit order (see page 89)
  - To define buses and signals by importing netlist files (see page 91)
  - To reorder bits by editing the Channels Assigned string (see page 92)
  - To set the default number base (see page 94)
  - To set polarity (see page 95)
  - To add user comments (see page 95)
  - To add a folder (see page 96)
  - To alias a bus/signal name (see page 96)
  - To sort bus/signal names (see page 96)
- Pod and Channel Naming Conventions (see page 372)
- Why Are Pods Missing? (see page 373)

Sampling Tab

The Sampling tab is access through the menu bar's **Setup>(Logic Analyzer Module)>Timing/State (Sampling)...** command. The Sampling setup tab is used to select and configure the sampling mode.



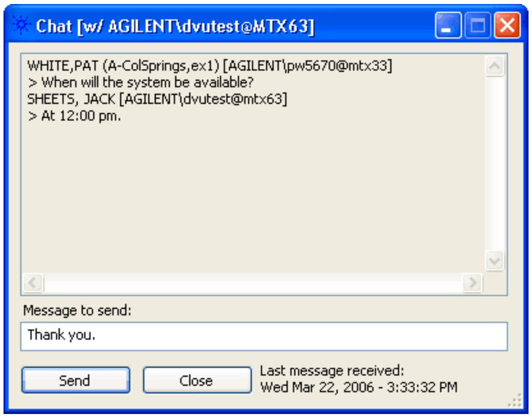
Acquisition	Lets you select the Timing or State acquisition mode (see Choosing the Sampling Mode (see page 97)).
Timing Options	When the Timing acquisition mode is selected, you can specify its options (see Selecting the Timing Mode (Asynchronous Sampling) (see page 98)).
State Options	When the State acquisition mode is selected, you can specify its options (see Selecting the State Mode (Synchronous Sampling) (see page 100)).
Options	Lets you specify options that apply to both the Timing and State acquisition modes (see To specify the trigger position (see page 111) and To set acquisition memory depth (see page 112)).
TimingZoom	Lets you turn the timing zoom feature on or off and specify its settings (see Using Timing Zoom (see page 112)).

See Also

- Choosing the Sampling Mode (see page 97)

Chat Dialog

The Chat dialog lets you enter and send messages to other logic analysis system users.



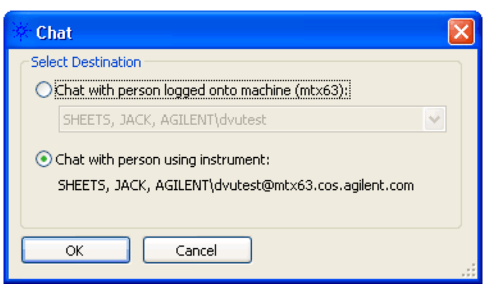
Message to send	Lets you enter a message to send.
Send	Sends the message.
Close	Closes the dialog and the chat session.

See Also

- Select System to Use Dialog (see page 479)
- Chat Select Destination Dialog (see page 451)

Chat Select Destination Dialog

The Chat Select Destination dialog lets you select either the person logged into or the person connected to the logic analysis system.



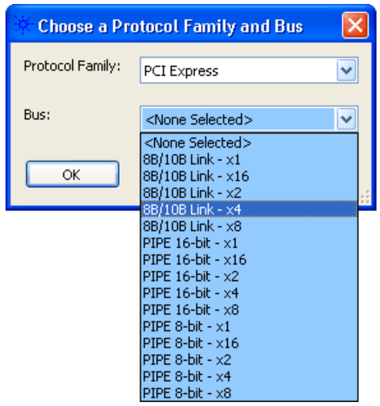
Clicking **OK** opens the Chat dialog (see page 450) where you can enter and send your message.

See Also

- Select System to Use Dialog (see page 479)

Choose a Protocol Family and Bus Dialog

The Choose a Protocol Family and Bus dialog lets you select a protocol family and bus for the "Find a packet" trigger function.



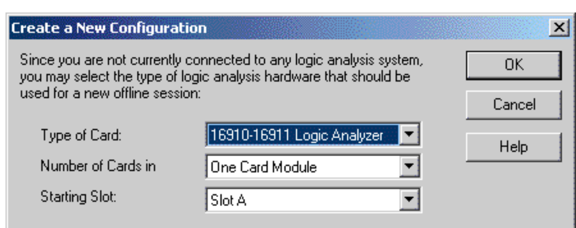
Protocol Family	Lets you select the protocol family.
Bus	Lets you select the type of bus within the protocol family.

See Also

- Find a packet (see page 524) trigger function
- To specify packet events (in "Find a packet" trigger function) (see page 145)

Create a New Configuration Dialog

The Select Offline Hardware dialog appears when you are in *offline mode* and you choose the **File>New** command to create a new logic analyzer configuration file. This dialog lets you specify the type of logic analyzer hardware to model in the configuration file.



Type of Card	Selects the type of logic analysis hardware to use in the new offline configuration file. A Virtual Analyzer is a generic logic analyzer with no hardware options; it is the type of logic analyzer that is used when fast binary format data from 16700-series logic analyzers is imported for offline analysis.
Number of Cards in	Specifies the number of cards in the hardware module.
Starting Slot	Selects the starting slot of the cards used in the new offline configuration file.

See Also

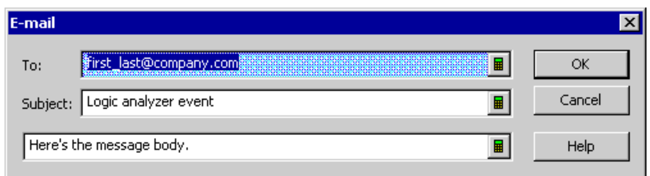
- Offline Analysis (see page 197)
- To set up multiple-modules with XML-format configurations (see page 188)

E-mail Dialog

NOTE

E-mail must be set up on the computer running the *Agilent Logic Analyzer* application before this feature will work. Refer to the operating system online help or your mail application's online help for information on setting up e-mail. See also Setting Up Outlook Express on the Logic Analysis System (see page 453).

Some mail applications block e-mail that is sent by running programs, so test this feature with your mail application before you use it.



To	Address(es) to which e-mail will be sent. You can specify multiple recipients by separating each e-mail address with a semicolon (;).
Subject	Subject of the e-mail.
(message)	Text of the message.

See Also

- To specify a trigger sequence step's goto or trigger action (see page 148)
- To create a new time interval measurement (see page 242)
- To create a new sample interval measurement (see page 243)
- To change a marker's position property (see page 238)
- To run until a number of compare differences (see page 270)

Setting Up Outlook Express on the Logic Analysis System

Outlook Express is installed on logic analyzers and logic analysis systems along with Internet Explorer and the Windows XP operating system. If you want to use the logic analysis system's "e-mail on" features (on trigger, on measured interval, on number of compare differences), you can use Outlook Express.

To set up Outlook Express on the logic analysis system:

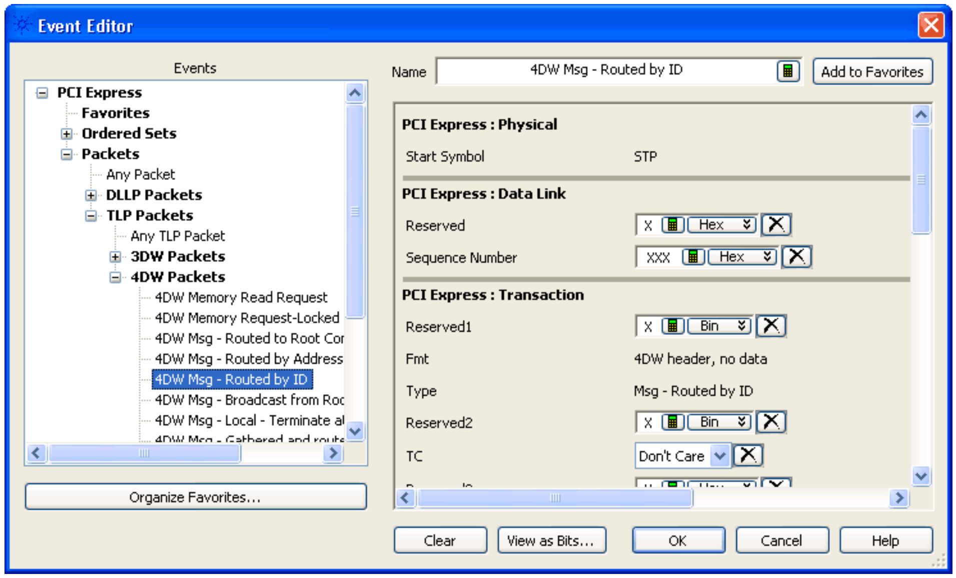
1. Make Outlook Express the default e-mail program in Internet Explorer:
   a. In Internet Explorer, choose **Tools>Internet Options...**.
   b. In the Internet Options dialog's Programs tab, for the **E-mail** service, select **Outlook Express**.
2. Get e-mail server and account information from your network or system administrator, and configure a mail account in Outlook Express:
   a. In Outlook Express, choose **Tools>Accounts...**.
   b. In the Internet Accounts dialog's Mail tab, click **Add>Mail...**.
   c. In the **Internet Connection Wizard**, follow the instructions, using the e-mail account information from your system or network administrator.
3. Make sure the Security tab settings are set correctly:
   a. In Outlook Express, choose **Tools>Options...**.
   b. In the Options dialog's Security tab, uncheck **Warn me when other applications try to send mail as me**.
4. Send a test e-mail from Outlook Express.
5. Test one of the logic analysis system's "e-mail on" features.

See Also

- E-mail Dialog (see page 453)

Event Editor Dialog

The Event Editor dialog lets you specify packet events in the "Find a packet" trigger function.



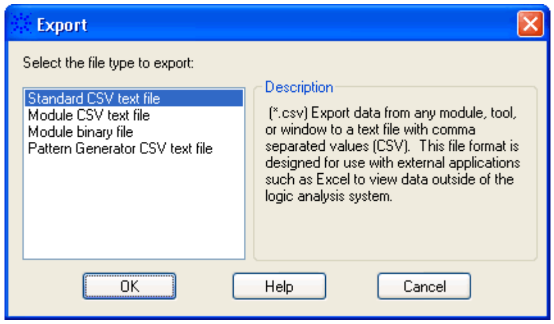
Events	Hierarchically lists protocol event types that you can select.
(Fields)	(On the right side of the dialog). Lets you enter, select, or clear ( ) packet field values.
Name	Lets you enter or modify the name of the packet event.
Add to Favorites	Adds the packet event to the favorites list.
Organize Favorites...	Opens the Organize Favorites dialog for organizing the packet event favorites list (see To organize favorite packet events (see page 148)).
Clear	Clears all packet field values.
View as Bits...	Opens the View as Bits dialog for viewing the packet event in a format similar to specifications documents (see To view a packet event as bits (see page 146)).

See Also

- Using the Packet Event Editor (see page 146)
- Find a packet (see page 524) trigger function
- To specify packet events (in "Find a packet" trigger function) (see page 145)
- To find packet patterns in the captured data (see page 261)
- "To specify packet patterns to filter" (in the online help)

Export Dialog

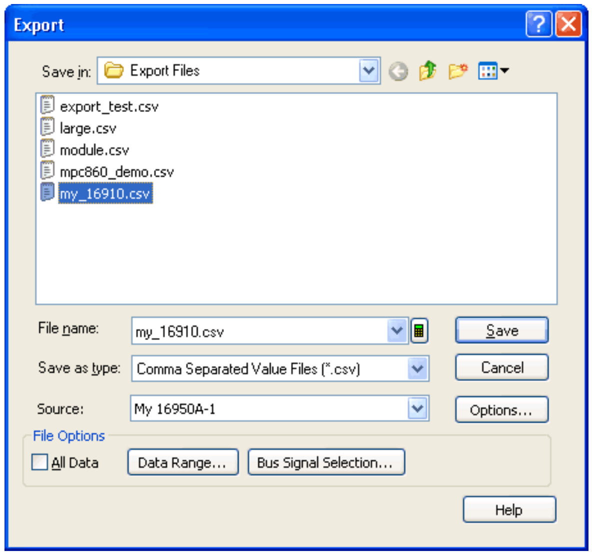
The Export dialog lets you export certain kinds of data into the *Agilent Logic Analyzer* application.



Standard CSV text file	Lets you export data from modules, tools, or windows to a comma separated value (CSV) format text file. This file type is for logic analyzer data that will be imported and viewed in external applications like Microsoft Excel (see To export data to standard CSV format files (see page 172)).
Module CSV text file	Lets you export module data only to a comma separated value (CSV) format text file. This file type is for post-processing tools and can be re-imported into the logic analysis system using a *data import module* (see To export data to module CSV format files (see page 175)).
Module binary file	Lets you export module data only to a binary format file (see To export data to module binary (ALB) format files (see page 178)). Future releases of the *Agilent Logic Analyzer* application will be able to import module binary files into the logic analysis system using a *data import module*.
Pattern Generator CSV text file	Lets you export pattern generator vector sequences to a comma separated value (CSV) format file (see "Exporting Vector Sequences to CSV Format Files" (in the online help)).

Export File Selection Dialog

The Export file selection dialog lets you select the file to which data is exported, the data source, the export options, the range of data samples, and the buses/signals to export.



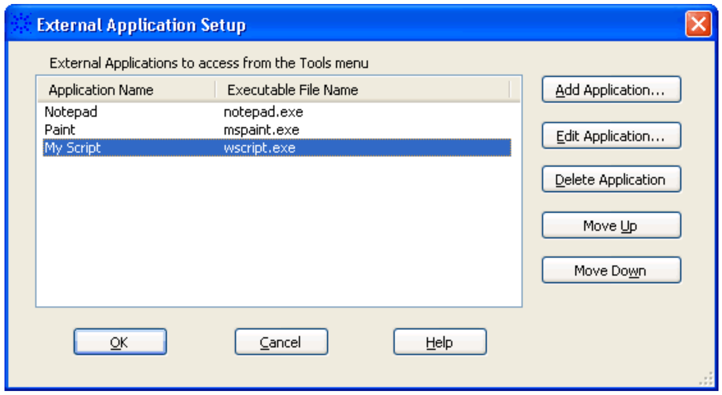
File name	Lets you select the file to which data is exported.
Save as type	The appropriate type is already selected, based on the file type selected in the previous Export dialog (see page 455).
Source	Lets you select the data source. The list of sources you can select from is determined by the file type selected in the previous Export dialog (see page 455).
Options...	Opens the File Export Options dialog where you can select the appropriate options for the file type selected in the previous Export dialog (see page 455).
All Data	When checked, data from all samples and all buses/signals is exported.
Data Range...	When **All Data** is not checked, this button opens a Range Properties dialog for selecting the range of data samples to export.
Bus Signal Selection...	When **All Data** is not checked, this button opens a Range Properties dialog for selecting the buses/signals to be included in the export.

See Also

- To export data to standard CSV format files (see page 172)
- To export data to module CSV format files (see page 175)
- To export data to module binary (ALB) format files (see page 178)
- "Exporting Vector Sequences to CSV Format Files" (in the online help)

External Application Setup Dialog

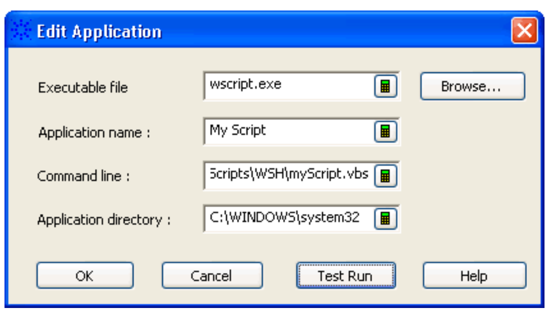
The External Application Setup dialog lets you add, edit, arrange, or remove items from the **Tools>External Applications>** menu.



Add Application...	Opens the Add Application dialog (see page 458) for specifying a new menu item's parameters.
Edit Application...	Opens the Edit Application dialog (see page 458) for changing the selected menu item's parameters.
Delete Application	Deletes the selected application from the menu item list.
Move Up Move Down	Moves the selected application up or down within the menu item list.

External Application Add/Edit Dialog

The Add/Edit Application dialog lets you enter or modify the parameters for an item in the **Tools>External Applications>** menu.



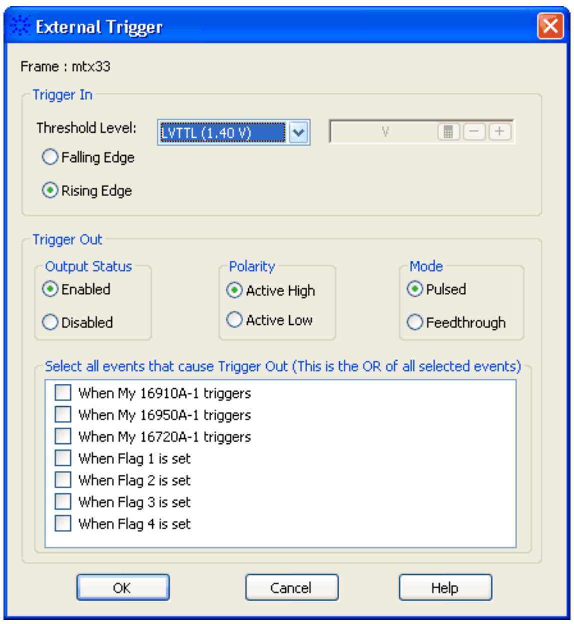
Executable file	The name of the file to execute when the menu item is selected.
Application name	The name that appears on the menu item.
Command line	Command line options for the executable file.
Application directory	The directory that contains the executable file.
Test Run	For quick testing, this executes the application with the given parameters.

External Trigger Dialog

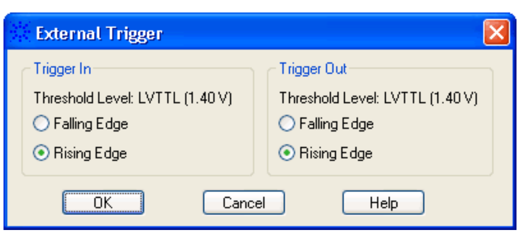
There are **Trigger In** and **Trigger Out** BNC connectors located on the logic analysis system (rear panel of 16900-series, 16800-series, or 1680-series, front panel of 1690-series). These BNC connectors are used to connect the analyzer to an external instrument and either send or receive a trigger signal.

The External Trigger dialog is used for setting up triggers between the logic analyzer or logic analysis system and other, external instruments.

The 16900-series or 16800-series External Trigger dialog looks like:



The 1680/90-series External Trigger dialog looks like:



Trigger In Lets you trigger the logic analyzer from another source. You can select whether a rising or falling edge indicates a trigger.

Input Signal Characteristic	16900-Series	16800-Series	1680/1690-Series
Input signal level:	Selectable, ±5.5 V Max.	Selectable, ±5 V Max.	TTL, 5.5 V Max.
Minimum signal amplitude:	500 mV	200 mV	500 mV

Trigger Out Sends a signal to another device when the logic analyzer triggers. You can select whether the trigger will appear as a rising or falling edge.

The trigger out signal is designed to drive a 50 Ohm load. It is recommended that for good signal quality, the trigger out signal be terminated in 50 Ohms to ground.

With a 16900-series logic analysis system frame or 16800-series logic analyzer, you can:

- Enable or disable (3-state high-impedance) the output.
- Choose the polarity of the output.
- Choose whether the output mode is **Pulsed** or **Feedthrough** (for observing flag settings).
- Select the events that will cause a trigger signal to be output.

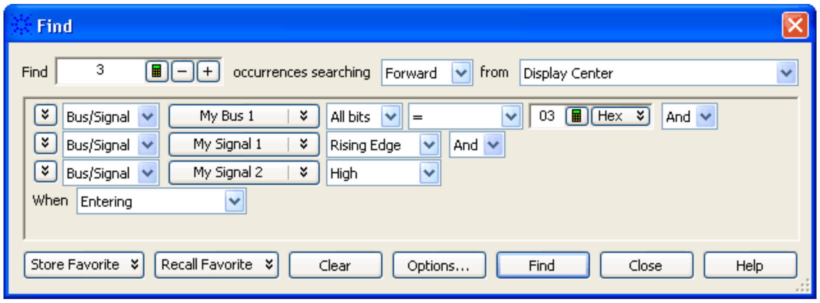
Output Signal Characteristic	16900-Series	16800-Series	1680/1690-Series
VOH (output high level):	>2.0 V (3.3 V avg.)	>2.0 V (3.3 V avg.)	>2.0 V (3.3 V avg.)
VOL (output low level):	<0.5 V (0 V avg.)	<0.5 V (0 V avg.)	<0.5 V (0 V avg.)
Pulse width:	Approx. 60-140 ns	Approx. 80-160 ns	Approx. 60-140 ns

See Also

- To trigger other instruments - trigger out (see page 163)
- To trigger analyzer from another instrument - trigger in (see page 164)

Find Dialog

The Find dialog lets you search for patterns in captured data. You can qualify your search by specific bits, data patterns, equality, and range operators. The search result is placed at the center of the display.



Find N occurrences	Specifies the number of occurrences to search for.
searching	Specifies whether to search Forward or Backward.
from	Specifies the starting location (Display Center, Beginning Of Data, End Of Data, Trigger, or a marker).
(pattern event)	Specifies the pattern event you wish to locate. In addition to the usual pattern matching operators (**=**, **!=**, **<**, **>**, **<=**, **>=**, **In Range**, and **Not In Range**), there are three additional operators you can use: • **Entering** — the first sample of one or more consecutive samples that match the pattern. (By comparison, the "**=**" equals operator considers every sample that matches the pattern as an occurrence.) • **Exiting** — the sample after one or more consecutive samples that match the pattern. • **Transitioning** — entering or exiting one or more consecutive samples that match the pattern.
When	A find qualifier (which further qualifies the find criteria with a time duration or other operator): • **Present** • **Not Present** • **Present>** (time duration) • **Present>=** (time duration) • **Present<** (time duration) • **Present<=** (time duration) • **Present for Range** (of time) • **Not Present for Range** (of time) • **Entering** • **Exiting** • **Transitioning** The find qualifiers **Present>**, **Present>=**, **Present<**, **Present<=**, **Present for Range**, and **Not Present for Range** let you specify a time duration. This means the find event specified in the expression area will be found based upon the given time and operator. The other qualifiers (**Present**, **Not Present**, **Entering**, **Exiting**, and **Transitioning**) do not allow a time duration.
Store Favorite	Lets you store favorite find patterns.

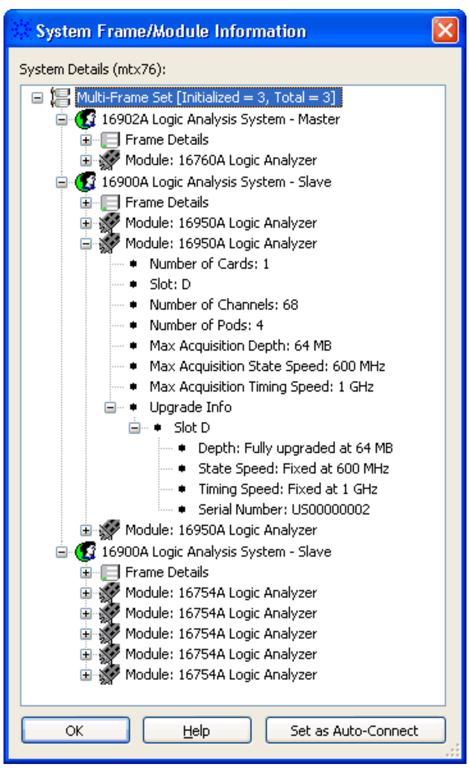
Recall Favorite	Lets you recall or delete favorite find patterns.
Clear	Clears the current find pattern.
Options...	Opens the Find Options dialog that lets you specify "found" marker placement.
Find	Performs the find without closing the Find dialog.
Close	Closes the Find dialog.

See Also

- To quickly find bus signal patterns (see page 257)
- To find bus/signal patterns in the captured data (see page 259)
- To find packet patterns in the captured data (see page 261)
- To find complex patterns in the captured data (see page 265)
- To store, recall, or delete favorite find patterns (see page 266)
- To specify "found" marker placement (see page 267)

Frame/Module Information Dialog

The Frame/Module Information dialog displays detailed information about a logic analysis system *frame* (see page 649).



System Details	Displays the detailed information about the logic analysis system. This includes both information on the frame as a whole and information on each module. If the frame is participating in a multiframe set (as is the case in the example above), frame and module details on each frame is shown. In the example above, the in-use icon shows a user is currently using the multiframe set. If module depth or speed is upgradeable (via hardware licensing), module upgrade information is also provided. Under the "Frame Details" category, you can find information about the frame's software version, host IP address, host name, whether or not the frame is password protected from remote-access, etc.
Set as Auto-Connect	Selects the logic analysis system frame as the one to use when the *Agilent Logic Analyzer* application starts. The words "auto-connect" will show up next to the frame selected as an auto-connect in the Select System to Use dialog (see page 479). This button will change to "Clear Auto-Connect" if this frame is already set as an auto-connect.
Clear Auto-Connect	When pressed, specifies that the logic analysis system frame not be automatically connected to when the *Agilent Logic Analyzer* application starts.

Notes:

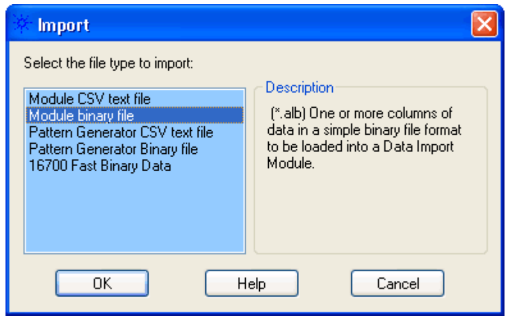
- When no auto-connect is established, the *Agilent Logic Analyzer* application attempts to go online with the local frame or starts offline if there is no local frame.
- The auto-connect frame selection is stored on a per-user basis-so each logged on user can establish a different auto-connect frame.
- If you are running the *Agilent Logic Analyzer* application on a standalone instrument or you are running the *Agilent Logic Analyzer* application on your PC with hosted instruments attached to your PC, the *Agilent Notification Center Icon* will be present on the taskbar (lower, right-hand corner of your desktop). This icon can be right-clicked to open an *instrument details* dialog showing the same type of information as the above dialog—but only for the local hardware.

See Also

- To view logic analysis system details (see page 68)

Import Dialog

The Import dialog lets you import certain kinds of data into the *Agilent Logic Analyzer* application.



Module CSV text file	Lets you import data from a CSV format text file into the logic analysis system using a *data import module* (see To create a data import module (see page 191)).
Module binary file	Lets you import data from a module binary (ALB) format file into the logic analysis system using a *data import module* (see To create a data import module (see page 191)).
Pattern Generator CSV text file	Lets you import vectors of stimulus to a pattern generator module (see " Importing Vector Sequences from CSV Format Files" (in the online help)).
Pattern Generator binary file	Lets you import setup information and a large number of stimulus vectors to a pattern generator module (see "Importing PattGen Binary (PGB) Format Files" (in the online help)).
16700 Fast Binary Data	Lets you import fast binary data from the 16700-series logic analysis system (see To import 167xx fast binary data (see page 187)).

Import Setup Dialog

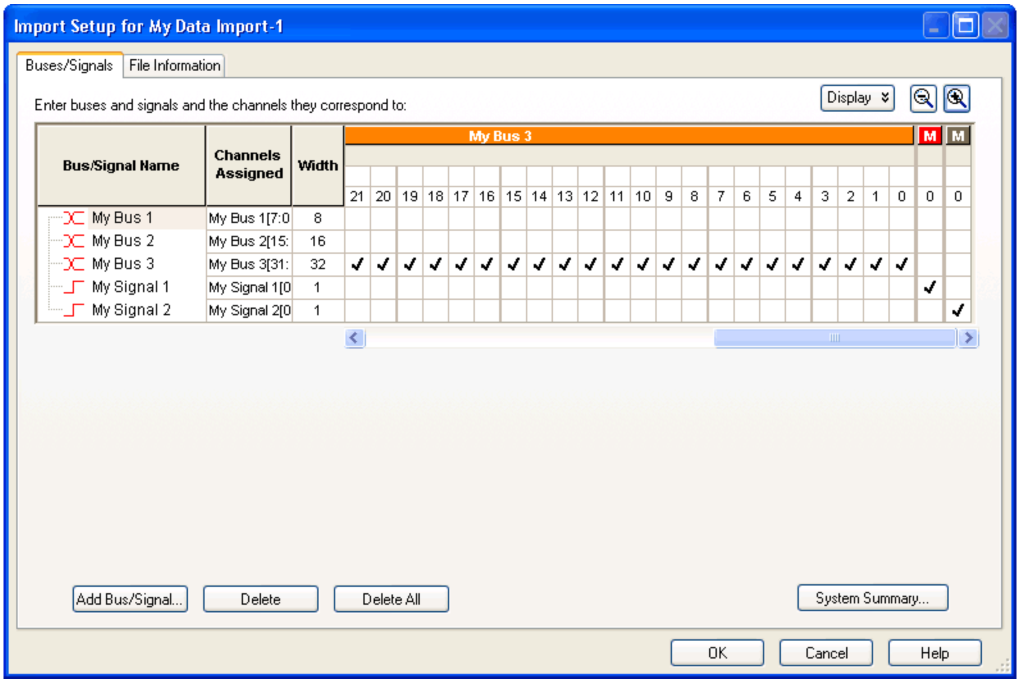
The Import Setup dialog is accessed through the menu bar's **Setup>(Data Import Module)>Bus/Signals...**.

The dialog consists of the following two tabs.

- **Buses/Signals** - The Buses/Signals tab is used to edit bus and signal names in the data import module. Also, you can assign a default number base and polarity to the bus or signal. See Buses/Signals Tab (see page 464).
- **File Information** - The File Information tab describes the contents of the file that has been imported. See File Information Tab (see page 466).

Buses/Signals Tab

The Buses/Signals tab is used to edit bus and signal names in the data import module. You also use the Buses/Signal tab to set the polarity, set the default number base, and enter user comments.



The Buses/Signals tab is accessed through the menu bar's **Setup>(Data Import Module)>Bus/Signals...** command.

Through the **Display** button, you can select what bus/signal setup information is displayed.

The bus and signal icons in the **Bus/Signal Name** column are normally red, but they turn gray if the bus/signal is locked by an inverse assembler.

Read Only Options

The following fields are read only and cannot be edited. The display of these items can be turned on/off under the **Display** button.

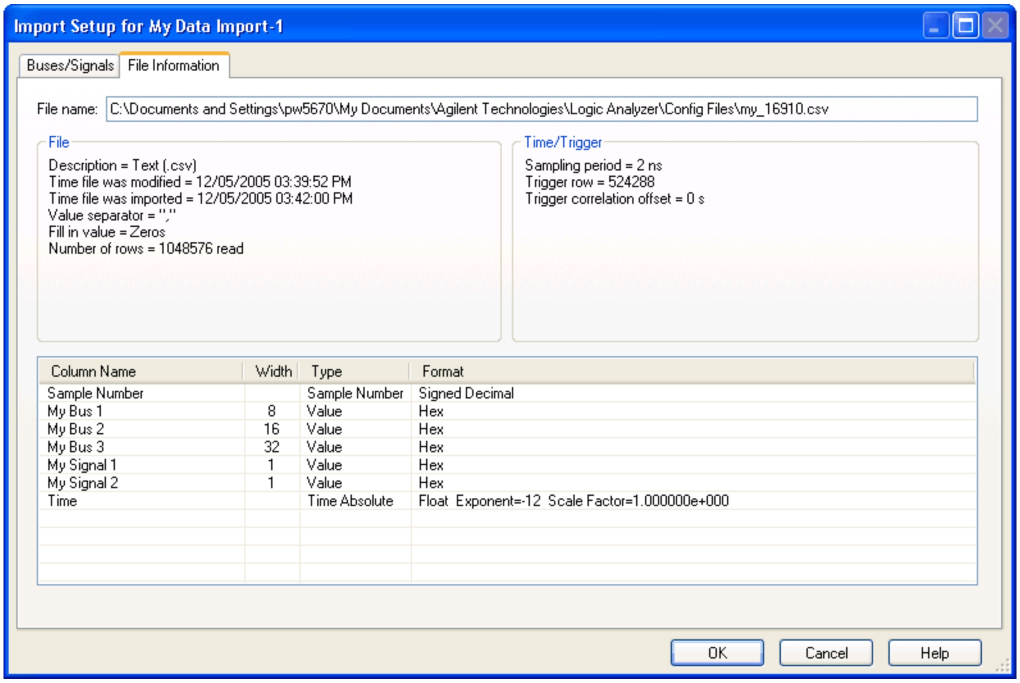
Width	The Width column displays the number of assigned channels on each bus.
Activity	The Activity row displays the type of signal activity on each channel. • Low bar = A stable low level. • High bar = A stable high level. • Transition arrows = An active signal transition between low and high.
Channel Numbers	The Channel Numbers row displays pod channel numbers

See Also

- To edit data import module bus/signal definitions (see page 193)
- Using Data Import Modules (see page 191)

File Information Tab

The File Information tab describes the contents of the file that has been imported.



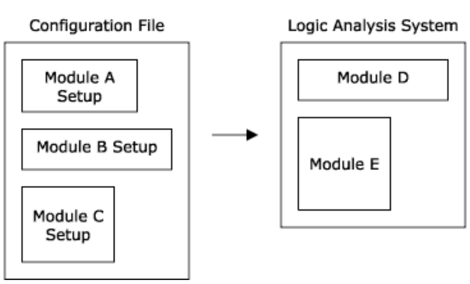
The File Information tab is accessed through the menu bar's **Setup>(Data Import Module)>File Info...** command.

See Also

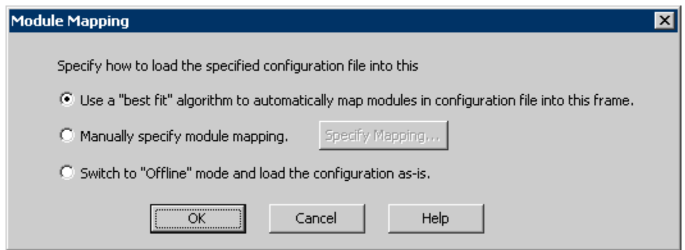
- To view data import module file information (see page 195)
- Using Data Import Modules (see page 191)

Module Mapping Dialog

The Module Mapping dialog helps you map module setup information from the configuration file you are opening to the modules in the logic analysis system you are using.



If you are opening an ALA format configuration file, modules must be compatible in order to setup a module with information from the configuration file. If you are opening an XML format configuration file, you can use setup information from any module; however, because of module differences, some settings may not transfer.



Best-fit algorithm (see page 467)	Automatically maps configuration file modules into the current frame.
Manually map	The **Specify Mapping...** button opens the Specify Mapping dialog (see page 488) to specify how configuration file modules should be mapped into the current frame.
Offline mode	Loads the configuration file as-is in the *offline mode*.

See Also

- To transfer module setups to/from multi-module systems (see page 188)

Best-Fit Algorithm for Automatic Module Mapping

The best-fit algorithms differ slightly, depending on whether you're loading XML or ALA format configuration files.

When Loading XML Format Configuration Files:

For any given module in the configuration file:

1 Is the module split?

2 Look for a module in the Overview window with the same name. If one is found, load the configuration into that module.

3 Look for the first module (based on the top to bottom order as shown in the Overview window) of the same *specific* type as the configuration file module. If one is found, load the configuration into that module.

   In this case, "specific" means, for example, a 16750/1/2A/B logic analyzer vs. a 16753/4/5/6A logic analyzer.

4 Look for the first module of the same *general* type as the configuration file module.

   In this case, "general" means, for example, "logic analyzer" vs. "pattern generator").

5 If not found with any of the above, then:

  a In online (either *Local* or *Remote*) mode, don't load the module.

  b In offline mode, *create* the module.

When Loading ALA Format Configuration Files

For any given module in the configuration file:

1 Look for the first module (based on the top to bottom order as shown in the Overview window) of the same *specific* type as the configuration file module. If one is found, load the configuration into that module.

   In this case, "specific" means, for example, a 16750/1/2A/B logic analyzer vs. a 16753/4/5/6A logic analyzer.

2 If not found, skip it.

NOTE

In offline mode:

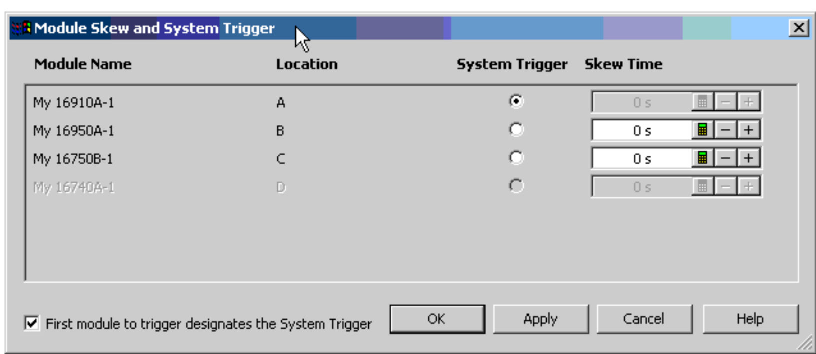
When loading an ALA format configuration file, there is *always* a "clear" performed in the Overview window. Therefore, no matching algorithm is needed.

When loading an XML format configuration file, the XML best-fit algorithm is used.

See Also

- Module Mapping Dialog (see page 466)

Module Skew and System Trigger Dialog



This dialog is available when there are multiple *module* (see page 650)s in a logic analyzer or logic analysis system. It lets you:

- Specify which module is the *system trigger* (that is, which module's trigger reference point is *Time=0*).
- Specify the trigger reference point skew for modules that are not the *system trigger*.

When **First module to trigger designates the System Trigger** is checked, the first module to trigger after the next run is selected as the *system trigger*. Unchecking this option and checking it again causes the module that has currently triggered first to become the selected *system trigger*.

Disabled modules are grayed out.

See Also

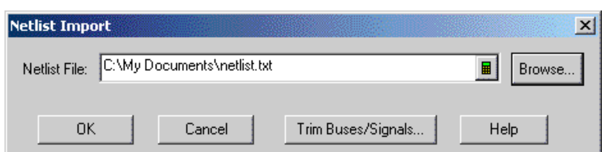
- Setting the System Trigger and Skew Between Modules (see page 303)
- To disable and enable modules (see page 76)

Netlist Import Dialog

The Netlist Import dialog lets you set up bus/signal names and assign them to logic analyzer channels by importing netlist files. Netlist files come from the Electronic Design Automation (EDA) tools used to design the device under test, and they contain information about the signals on the connectors built into the device under test for the logic analyzer probes.

NOTE

Before you can import bus/signal names from netlist files and assign them to logic analyzer channels, you must use the Define Probes dialog to identify the probes that are used with the logic analyzer.



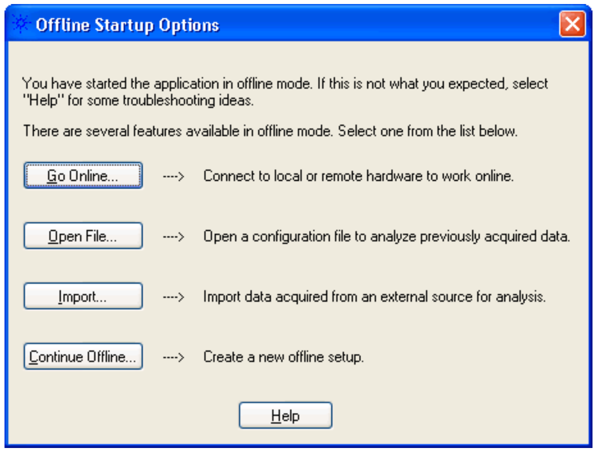
Netlist File	Lets you enter or browse for the name of the netlist file to import.
Trim Buses/Signals...	Opens the Trim Bus/Signal Names dialog which lets you trim the bus/signal names imported from the netlist file.

See Also

- To define buses and signals by importing netlist files (see page 91)

Offline Startup Options Dialog

The Offline Startup Options dialog appears when you start the *Agilent Logic Analyzer* application and it wants to start in the *offline mode* (see page 197) (if this is unexpected, see If starting in offline mode is unexpected (see page 323)). This dialog presents options for the tasks you can perform in the offline mode.



Go Online...	Opens the Select System to Use dialog (see page 479) for choosing a frame to connect the *Agilent Logic Analyzer* application to.
Open File...	Lets you open a logic analyzer configuration file (see page 184).
Import...	Opens the Import dialog (see page 463) for importing data from an external source into the logic analysis system.
Continue Offline...	Opens the Create a New Configuration dialog (see page 452) for creating a new logic analyzer configuration file.

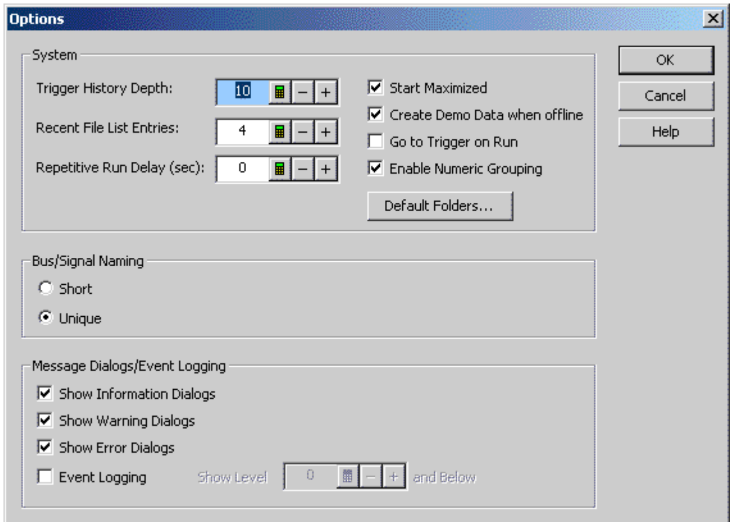
See Also

- If starting in offline mode is unexpected (see page 323)

Options Dialog

To change your system options, select **Edit>Options...** from the menu bar. System options are written in the Windows registry file and persist across sessions.

- System Options (see page 471)
- Bus/Signal Naming Options (see page 471)
- Message Dialogs/Event Logging Options (see page 472)



System Options

Trigger History Depth	You can keep as many as 50 of the most recently used triggers. See To store a trigger (see page 166) for more information on re-using triggers. Trigger history is saved in the configuration files. The default is 10.
Recent File List Entries	This sets how many recently-loaded configuration files are shown in the **File** menu. The default is 4.
Repetitive Run Delay	Delay between repetitive measurements allows you to look at the captured data and decide whether to stop the measurement before the next run occurs.
Start Maximized	Specifies whether the *Agilent Logic Analyzer* application's main window is maximized when the application is started.
Create Demo Data when offline	When you run the analyzer, fake data will be created. This mode is useful when learning how to use the logic analyzer software. **NOTE:** The logic analyzer does not trigger with fake data. You can set the triggers, but will not get the same results you would with a real acquisition.
Go to Trigger on Run	Specifies, when a logic analyzer measurement is run, whether display windows are automatically positioned around the data that triggered the analyzer.
Enable Numeric Grouping	Numeric grouping adds spaces between every four hexadecimal and binary digits, spaces between every three octal digits, and commas between every three decimal digits (for example, FFFF FFFF, 1111 1111, 777 777, and 999,999).
Default Folders...	Opens the Default Folders dialog for specifying the default folder locations for configuration files, export files, and import files.

Bus/Signal Naming Option

When you have defined the same bus/signal name in more than one module:

Short	Bus/signal names are shown without the module name even if they are the same. In other words, it is possible to display two buses called "ADDR" that are not the same physical bus. (You can still see the module name in a tool tip by hovering over the bus/signal name.)
Unique	Module names are pre-pended to identical bus/signal names, for example, "Module 1:ADDR" and "Module 2:ADDR".

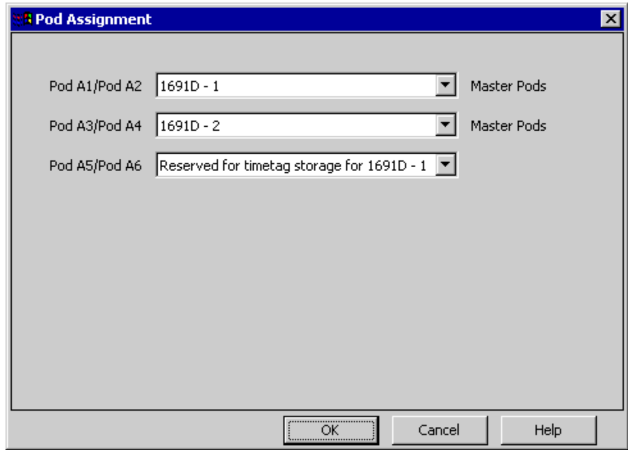
Message Dialogs/Event Logging Options As with any other program, the *Agilent Logic Analyzer* application generates messages about events. You can choose which messages are displayed. Check the appropriate box to indicate you wish the dialogs displayed.

Show Information Dialogs	Information dialogs offer tips such as the location of Simple Trigger, and do not indicate a failure.
Show Warning Dialogs	Warning dialogs occur when some setting may affect your data, such as being offline.
Show Error Dialogs	Error dialogs occur when an operation cannot be completed as specified.
Event Logging	You can choose to have all events recorded in a log file. Event logging will slow down your logic analyzer. Event logs can be viewed through **Help>Status Log**. Set the event logging level according to the directions of your Agilent Technologies support person. Be sure to turn off event logging when resuming normal use.

Pod Assignment Dialog

The Pod Assignment dialog lets you reserve a *pod* (see page 651) or *pod pair* (see page 651) for time tag storage. When a logic analyzer *module* (see page 650) has been split into two modules, you can also use this dialog to re-assign pods or pod pairs.

If you choose the highest acquisition memory depth (see page 112) and there is a pod pair that has no buses or signals assigned to it, that pod pair is automatically reserved for time tag storage, and there is no need to use this dialog.



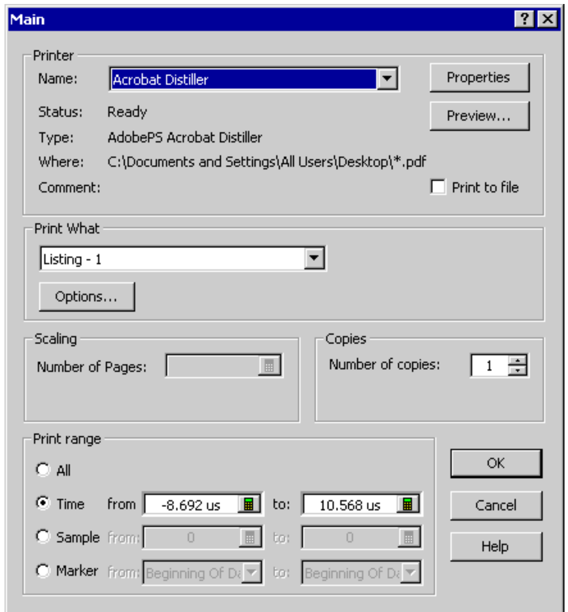
Pod/Pod Pair	Indicates the pod or pod pair to be assigned or reserved.
(Module Selection)	For each pod or pod pair, selects the module to which it is assigned or reserves it for time tag storage.
Master Pods	Indicates that the pod or pod pair is on the master card.

See Also

- Split Analyzer Setup Dialog (see page 489)
- Memory Depth and Channel Count Trade-offs (see page 374)
- Pod and Channel Naming Conventions (see page 372)

Printing Data Dialog

After choosing **File>Print...**, this dialog lets you print the current measurement data from a display window.



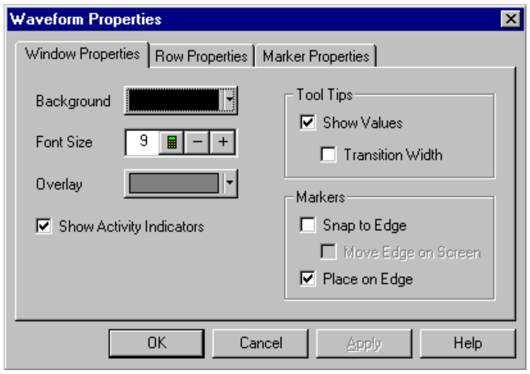
NOTE The first time you access the print dialog, you are asked to install a printer. Follow the directions in the printer install dialogs that appear.

Printer	Lets you select the printer, change its properties, and preview the print out.
Print What	Lets you select which display window to print from and specify printing options.
Scaling	Lets you specify the number of pages to print per sheet.
Copies	Lets you specify the number of copies to print.
Print range	You can print All data, or print just a defined range between times, sample numbers, or marker locations. Data is printed from the smallest time/sample to the largest.

See Also

- Printing Captured Data (see page 306)
- To install a printer (see page 307)
- To connect a LAN (see page 307)

Properties Dialog

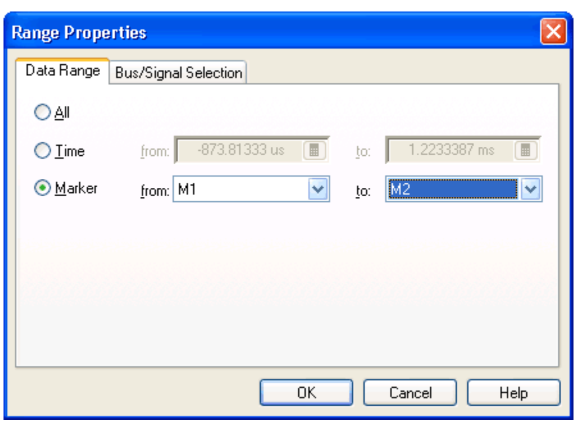


The Properties dialog is accessed through the menu bar's **Window>Properties...**. Use it to set up how the window and the displayed data appear.

- Changing Waveform Window Properties (see page 213)
- Changing Listing Window Properties (see page 226)
- To set Compare window properties (see page 270)
- Changing Source Window Properties (see page 277)
- Changing Marker Properties (see page 247)

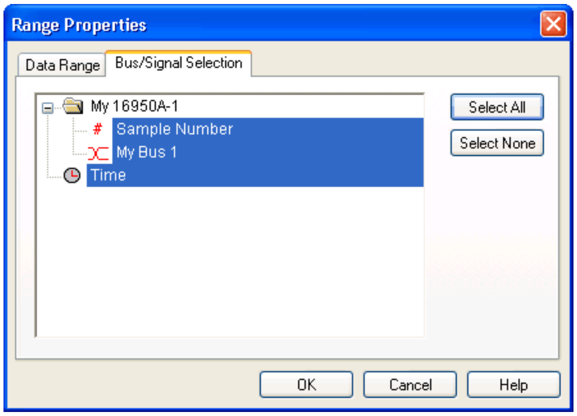
Range Properties Dialog

Data Range Tab Specifies the range of data to export.



Time	Lets you specify the range of data to export by time.
Marker	Lets you specify the range of data to export by markers.

Bus/Signal Selection Tab Specifies the buses/signals to export data from.



Select All	Selects all buses/signals.
Select None	De-selects all buses/signals.

See Also

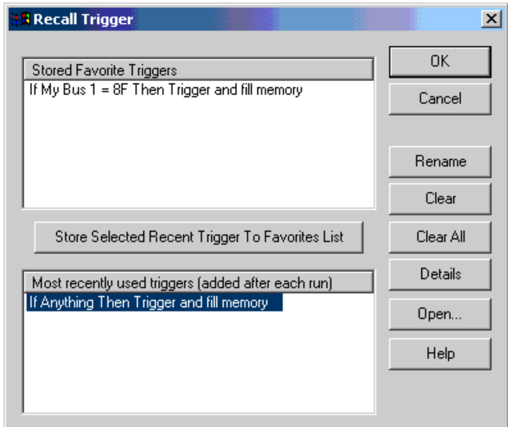
- To export data to CSV format files (see page 172)

Recall Trigger Dialog

The Recall Trigger dialog lets you:

- Recall a previously-used trigger from:
  - The favorites list.
  - The recently used list.
  - An XML format trigger specification file.
- Move a recently used trigger to the favorites list.
- Rename the trigger.
- Clear triggers from the favorites or recently-used list.
- View trigger details.

NOTE The favorites list is saved with the logic analyzer configuration. If you load a new configuration file, the favorites list is overwritten.



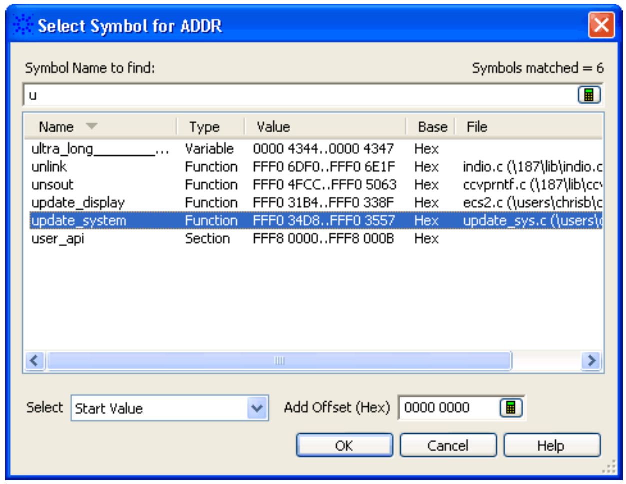
Rename	Lets you edit the name of the highlighted trigger.
Clear	Clears the highlighted trigger from the list.
Clear All	Clears all triggers from recall lists.
Details	Shows complete definition of the highlighted trigger.
Open...	Lets you recall a trigger that was previously saved to an XML format trigger specification file. **NOTE:** When a trigger is stored to an XML format trigger specification file, trigger sequence steps are converted to advanced If/Then trigger functions. Therefore, the trigger may look different when you recall it from an XML format file; however, it is equivalent to the trigger that was saved.

See Also

- To store a trigger (see page 166)
- To recall a trigger (see page 167)
- To set the trigger history depth (see page 167)

Select Symbol Dialog

Use the Select Symbol dialog to choose a symbol to use when the numeric base (see page 230) is set to Symbols.



The Select Symbol dialog becomes available when you use the Symbols number base in the following dialogs:

- Find (see page 259)
- "Filter/Colorize" (in the online help)
- Specifying Simple Triggers (see page 133)
- Advanced Trigger Dialog (see page 445)

In the Select Symbol dialog:

Symbol Name to find	Filter the list of symbols by typing characters in this field. You can also use the wildcard characters: • * (asterisk) to represent zero or more characters. • ? (question mark) to represent a single character. You can sort on any column in the symbol list by clicking the column header.
Name	Lists the symbol names defined or loaded for the bus (see Setting Up Symbols (see page 116)).
Type	Lists the symbol types (for example, section, variable, function, etc.). When sorting on this column, the symbols associated with each type are sorted by name.
Value	Lists the symbol values.
Base	Shows the number base for the symbol value.
File	Shows the high-level source file that the symbol is from. When sorting on this column, the symbols associated with each file are sorted by value.

Select	When there is a range of values associated with the selected symbol, you can choose the **Start Value** of the range, the **End Value** of the range, and if you are selecting a symbol for a range setting, the **Start and End Values** of the range.

Add Offset (Hex)	Lets you add an offset to the selected symbol value, for example, in the case where code is relocated.
	Note that when you use offsets, the system stores the "real" value, not the fact that it is a symbol plus an offset. This can cause the display of the symbol+offset to be different than what you entered. For example, for:
	•
	`Symbol          Value`
	`------------    ------`
	`RangeSymbol1    00..10`
	`RangeSymbol2    11..20`
	`Symbol3         21`
	`Symbol4         22`
	`Symbol5         FF`
	• If you enter "Symbol3 + 1", the system interprets this as 22, which is also Symbol4. So, even though you entered "Symbol3 + 1", the system displays "Symbol4".
	• If you enter "RangeSymbol2(end value) + 1", it will be displayed as "Symbol3".
	• If you enter "RangeSymbol1(start value) + 12", it will be displayed as "RangeSymbol2+1".
	• Symbol values can "wrap", such as "Symbol5 + 1" where the result is 00. In this case, the you enter "Symbol5 + 1" and the resulting symbol is "RangeSymbol1".

See Also

- Setting Up Symbols (see page 116)
- Symbols Dialog (see page 492)

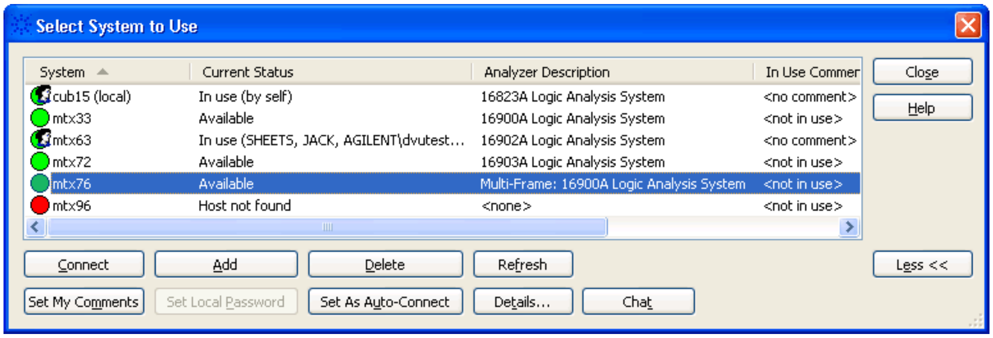
Select System to Use Dialog

The Select System to Use dialog lets you select a logic analysis system *frame* (see page 649) to connect to, and it lets you manage the list of frames.

A local system is a frame connected to the machine that runs the *Agilent Logic Analyzer* application. Remote systems are frames connected to machines elsewhere on your network. The remote system list can be managed any way you wish. The list of remote systems is stored on a per-user basis (each user has their own customizable list of remote systems).

The information in the dialog can be sorted by any of the columns by clicking on the column header.

You can right-click on any row in the dialog to get quick access to a menu of system-specific actions.



System	Displays the hostname or IP address of a frame in the list. A green, yellow, or red indicator indicates whether you can connect to or obtain information from this frame (green), the frame hardware is initializing (yellow), or some other problem (red)—such as the host not having any frames, the host is offline, or the software on the target machine is incompatible.
Current Status	Displays whether a frame is available, offline (that is, powered down), currently in use, or has an incompatible remote service (that is, its software needs to be upgraded to match the version of software installed on the machine displaying this dialog).
Analyzer Description	Displays the type of logic analyzer frame.
In Use Comment	Displays the "system in use" comments set by the user currently using the frame.
Connect	Connects to the selected logic analysis system (either local or remote). You can connect to a frame even if it is in use. You will be warned if you elect to connect to a frame that is already in-use before bumping the other user offline. Taking a user offline by connecting to an in-use frame will result in the other user losing any unsaved acquisition data (included in the warning message). For this reason, it is always preferable to contact the user (perhaps using the chat feature) and ask them to gracefully take themselves offline—saving any important data. If the user is not reachable—this ability to claim the system remotely is a powerful feature.
Add	Lets you enter the hostname or IP address of a remote system to be added to the list.
Delete	Removes the selected system from the system list.
Refresh	Forces an immediate refresh of all information in this dialog. This dialog is auto-updating—so you should not need to push this button. It is provided as a fail-safe only.
More >> Less <<	Shows or hides the bottom row of buttons.

Set My Comments	Opens a dialog that lets you enter some in-use comments. If another *Agilent Logic Analyzer* application attempts to connect to the system that you are currently connected to, your "system in-use" comments will be displayed. These comments can be used to explain why you are using a particular system, give your contact information, etc. These comments can be changed before going online with a frame or while online with a frame. The changes will take effect immediately.
Set Local Password	Opens the Remote Access Password Utility dialog for establishing a remote-connect password (see page 72). The icon next to a *remote* system will have a padlock superimposed on it if a password is required to connect to that machine. A remote-access password forces remote users to enter this password before connecting to any local instrument. The local system icon will never have a padlock on it because a remote-access password is never required for the local client. This button will change to "Clear Local Password" if a remote-access password is already set. Only Windows users with administrative credentials will have the ability to set or clear remote-access passwords.
Set as Auto-Connect	Selects the logic analysis system frame as the one to use when the *Agilent Logic Analyzer* application starts. The words "auto-connect" will show up next to the frame selected as an auto-connect. This button will change to "Clear Auto-Connect" if this frame is already set as an auto-connect.
Details...	Opens the Frame/Module Information dialog (see page 462) which displays detailed information about the selected logic analysis system. If the selected frame is a member of a multiframe set, frame and module information on all frames in the set is presented in this dialog.
Chat	Opens the Chat Select Destination dialog (see page 451) for communicating with someone on the selected system. You have the option of opening a two-way, interactive chat with any person logged on to the selected system or the user that is currently using the selected frame (if different).
Close	Closes the dialog without connecting to a local or remote system.

Notes:

- If the systems in this dialog are slow to update, try removing any machines in the list that are unresponsive (red) or not used.
- Slow network conditions can also slow the update rate of this dialog.
- This dialog is auto-updating—so it is not necessary to push the refresh button to see status changes. The refresh button is provided as a fail-safe only.

See Also

- Connecting to a Logic Analysis System (see page 63)

Software Licensing Dialog

The Software Licensing dialog is used to manage the software licenses used by a logic analysis system. This dialog has four tabs:

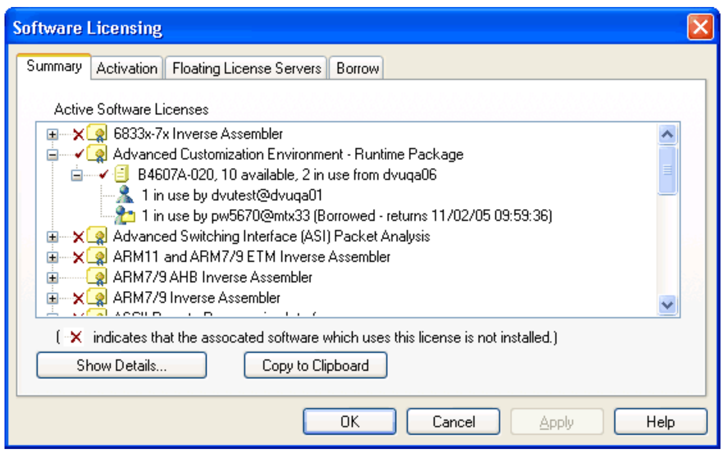
- Summary Tab (see page 482)
- Activation Tab (see page 482)
- Floating License Servers Tab (see page 483)
- Borrow Tab (see page 484)

See Also

- Managing Software Licenses (see page 311)

Summary Tab

The Software Licensing dialog's Summary tab displays information about the licenses that can be used in the logic analysis system.



Folders in the **Active Software Licenses** hierarchy show the licensed software that can be used. Red check marks show floating licenses are in use. A red "X" next to a folder shows that the software is not installed.

Within a folder, the status of individual licenses is displayed.

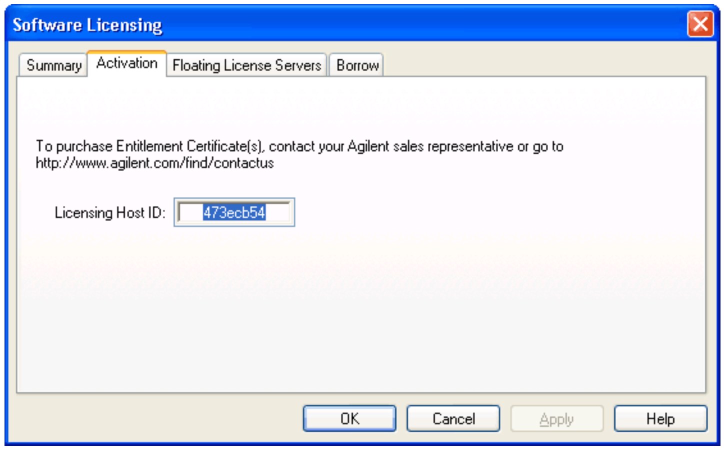
Show Details...	Opens a dialog that displays detailed information about the selected license.
Copy to Clipboard	Copies software licensing summary information to the clip board.

See Also

- To view active software license information (see page 312)

Activation Tab

The Software Licensing dialog's Activation tab contains the Licensing Host ID which is needed to activate software licenses.



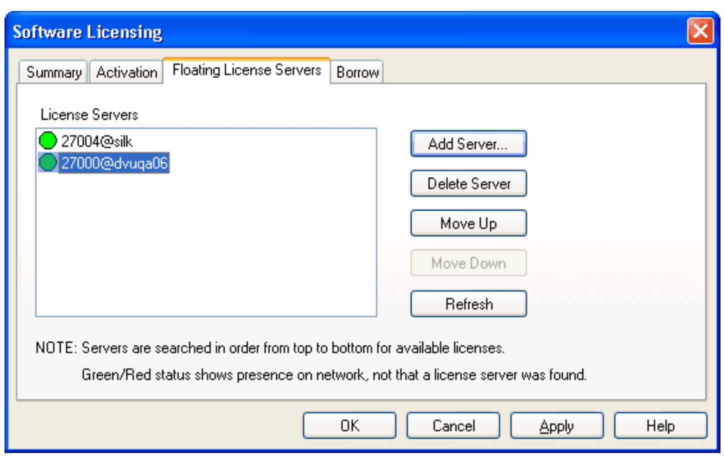
Licensing Host ID	This ID is used when obtaining license files for software tools.

See Also

- To activate software licenses (see page 313)

Floating License Servers Tab

The Software Licensing dialog's Floating License Servers tab lets you identify and order the servers that floating licenses can be obtained from.



When licenses need to be checked out, the list of **License Servers** is searched in order, and the license is checked out from the first server having an available license.

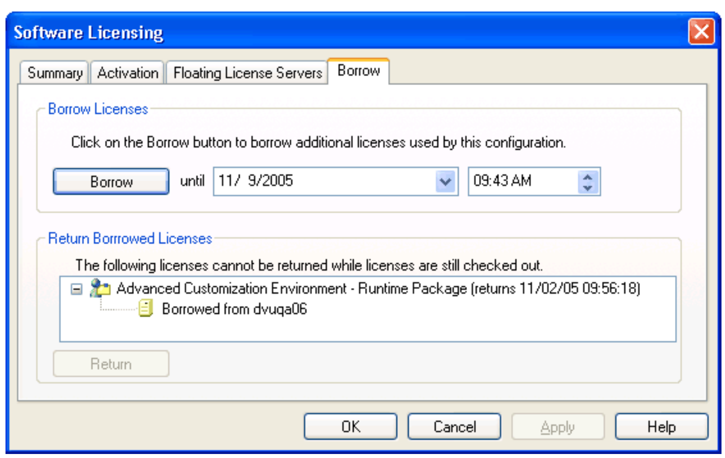
Add Server...	Opens a dialog for entering the computer name and port number of the floating license server. CAUTION Only enter names of computers (or logic analyzers) that are floating license servers. Otherwise, the license manager interface hangs up for many minutes trying to determine if the computer is really a floating license server.
Delete Server	Removes the selected server from the list.
Move Up	Raises the selected server in the search order.
Move Down	Lowers the selected server in the search order.
Refresh	Updates the green or red server availability indicators. This is only a check of whether the computer is on the network, not of whether the license server software is running on that computer.
Apply	License server changes must be applied before you can go to the Summary or Borrow tabs.

See Also

- To access floating license servers (see page 314)

Borrow Tab

The Software Licensing dialog's Borrow tab lets you borrow floating licenses from a server for a period of time, for example, if you're taking a logic analyzer (or a computer running the *Agilent Logic Analyzer* application) out of the office (or just off the network). When a borrowed license's time expires, the license is automatically returned to the server. However, you can also use the Borrow tab to return licenses early.



Borrow Licenses	Lets you enter the amount of time you want to borrow a license for and borrow the license. The default time is seven days. The minimum time is ten minutes. See also Messages in the Borrow Licenses Area (see page 485).
Return Borrowed Licenses	Lets you return borrowed licenses early. All borrowed licenses must be returned at the same time. You are not able to return borrowed licenses while any licenses are checked out. See also Messages in the Return Borrowed Licenses Area (see page 486).

See Also

- To borrow floating licenses and return them early (see page 316)

Messages in the Borrow Licenses Area These messages can appear in the Software Licensing dialog's Borrow tab.

Borrowing is not supported while in Demo Center Mode.

Licenses cannot be borrowed while using the Demo Center feature.

This configuration is not using any licenses. There is nothing to borrow.

No licenses are currently in use, so there is nothing to borrow.

This configuration is not using any floating licenses. There is nothing to borrow.

If all licenses being used are node-locked, there are no licenses that can be borrowed.

The licenses for this configuration cannot be borrowed because some are node-locked.

You cannot borrow licenses when floating licenses and node-locked licenses are in use at the same time.

Click on the Borrow button to borrow licenses used by this configuration.

When this message is displayed, you can borrow the licenses used by the current configuration.

Click on the Borrow button to borrow additional licenses used by this configuration.

When this message is displayed, some licenses are already borrowed, and you can borrow the additional licenses used by the current configuration.

All licenses needed by this configuration are already borrowed.

When this message is displayed, all licenses in use are already borrowed. To borrow additional licenses, open the feature that requires the license, and return to the Software Licensing dialog's Borrow tab.

Messages in the Return Borrowed Licenses Area These messages can appear in the Software Licensing dialog's Borrow tab.

The following licenses cannot be returned while some servers are not configured.

If a license was checked out from a server that is not currently configured, licenses cannot be returned early.

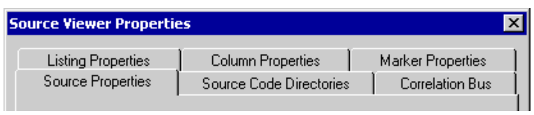
The following licenses cannot be returned while licenses are still checked out.

If any licenses are checked out (and not borrowed), borrowed licenses cannot be returned early.

The following licenses are currently borrowed for exclusive use on this system.

When this message is displayed, borrowed licenses can be returned early.

Source Viewer Properties Dialog



- Source Properties Tab (see page 486)
- Source Code Directories Tab (see page 487)
- Correlation Bus Tab (see page 488)

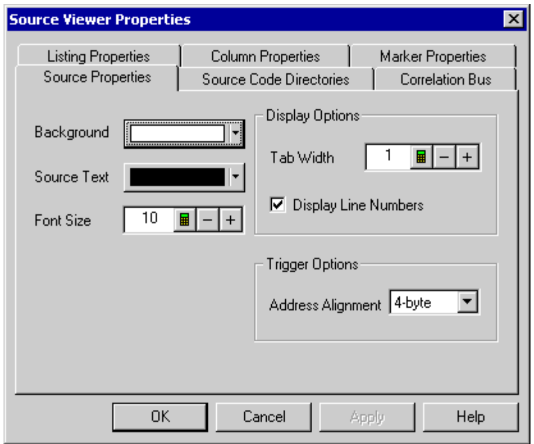
The **Listing Properties**, **Column Properties**, and **Marker Properties** tabs are the same as in the Listing window.

See Also

- Changing Listing Window Properties (see page 226)
- Changing Bus/Signal Column Properties (see page 228)

Source Properties Tab

The Source Viewer Properties dialog's Source Properties tab lets you set the background color and font size as well as display options like the number of spaces to use for tabs and whether or not to display line numbers.

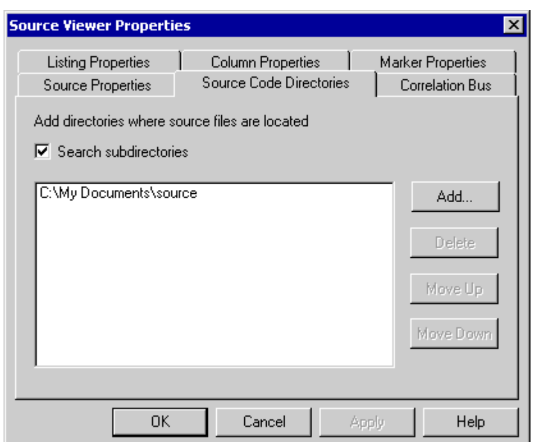


See Also

- Changing Source Window Properties (see page 277)
- Source Viewer Properties Dialog (see page 486)

Source Code Directories Tab

The Source Viewer Properties dialog's Source Code Directories tab lets you specify the directories where the source code is located. This is necessary because source file paths specified in the symbol file may not be valid if you compile on one computer and debug on another. You can specify multiple directories and change their order. Directories are searched in order, and you can specify whether subdirectories are searched.

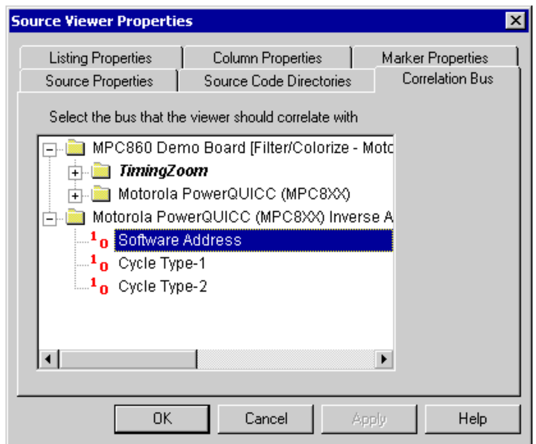


See Also

- To edit the source code directory list (see page 275)
- Source Viewer Properties Dialog (see page 486)

Correlation Bus Tab

The Source Viewer Properties dialog's Correlation Bus tab lets you specify the bus whose line number symbols will be used for source correlation. Typically, you will select the "software address" bus generated by an inverse assembler tool or another address bus.

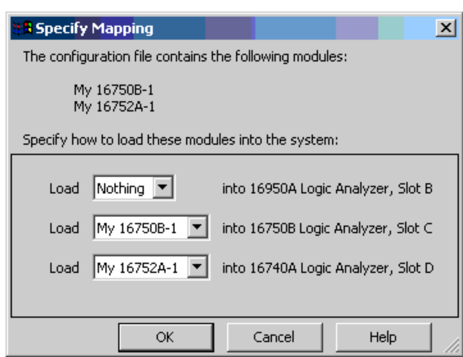


See Also

- To select the correlation bus (see page 276)
- Source Viewer Properties Dialog (see page 486)

Specify Mapping Dialog

The Specify Mapping dialog lets you manually map modules from a configuration file to modules in the logic analysis system.



The top of the Specify Mapping dialog lists the module configurations in the file being loaded. The bottom part of the dialog lists modules in the logic analysis system. The **Nothing** selection says not to use any of the module configurations being loaded.

NOTE

If you cannot load setup information from an ALA format configuration file into a particular module, the modules are not compatible, and you need to use an XML format configuration file to transfer the module setup information (see If an ALA format configuration file won't open (see page 324)).

See Also

- Module Mapping Dialog (see page 466)
- To transfer module setups to/from multi-module systems (see page 188)
- ALA vs. XML, When to Use Each Format (see page 399)

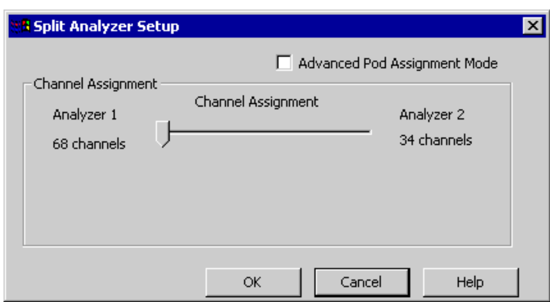
Split Analyzer Setup Dialog

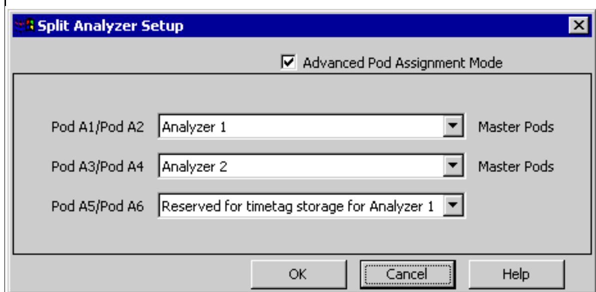
A logic analyzer *module* (see page 650) can be split into two logic analyzer modules, for example, to probe two buses with different clock signals.

NOTE

When you split a logic analyzer module, one of the resulting modules must be in the state sampling mode (they cannot both be in the timing sampling mode).

The Split Analyzer Setup dialog lets you specify how many channels are used in each module.



<table>
<tr><td>Channel Assignment</td><td>Drag the slider bar to split channels between the logic analyzer modules.</td></tr>
<tr><td>Advanced Pod Assignment Mode</td><td>Select this option for finer control over which pods (see page 651) or pod pairs (see page 651) are assigned to each module or are reserved for time tag storage.


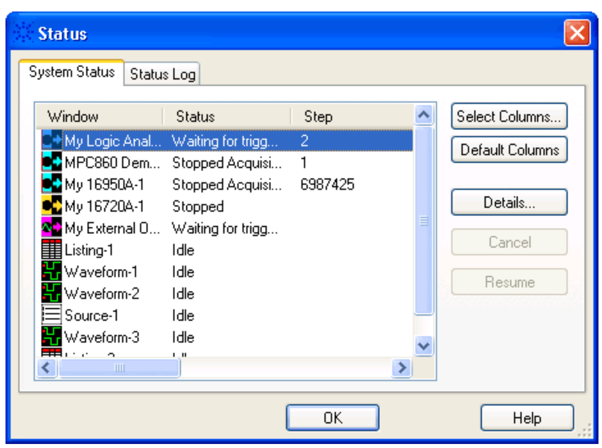
Master Pods indicate that the pod or pod pair is on the master card.</td></tr>
</table>

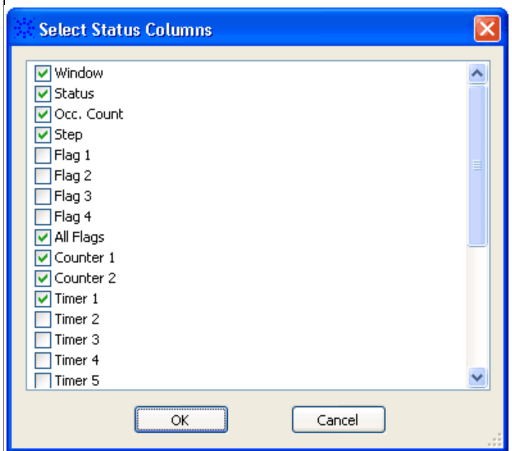
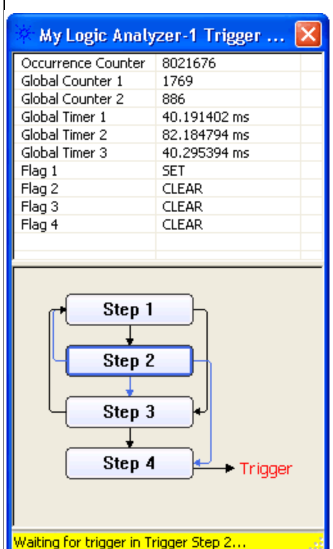
See Also

- Configuring Logic Analyzer Modules (see page 76)
- Memory Depth and Channel Count Trade-offs (see page 374)
- Pod and Channel Naming Conventions (see page 372)

Status Dialog

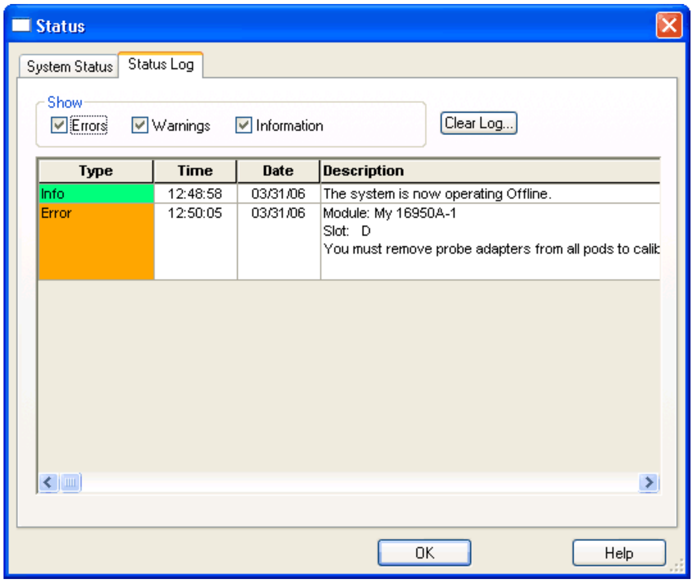
System Status Tab Displays the logic analysis system status.



Select Columns...	For logic analyzer modules, opens the Select Status Columns dialog for selecting the columns to be displayed. 
Default Columns	Resets the columns displayed in the System Status tab to the default set.
Details...	Displays details for the selected module, tool, or window.  For example, module details include: graphical trigger overview, occurrence counter, global counter, flags, and timer status.
Cancel	Cancels processing for the selected module, tool, or window.
Resume	Resumes canceled processing for the selected module, tool, or window.

You can copy a module, tool, or window's status to the clip board by right-clicking and choosing **Copy** from the popup menu.

Status Log Tab Displays the logic analysis system status log.



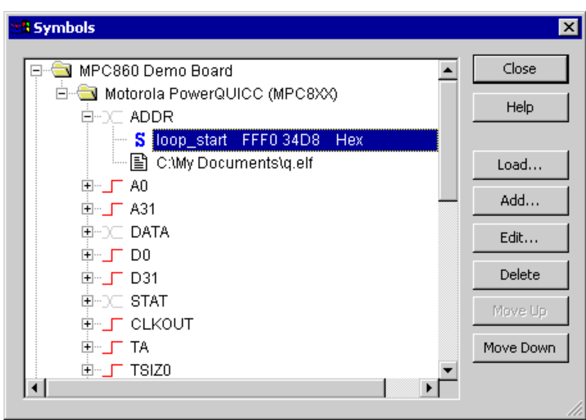
You can select the types of log messages to display, and you can clear the log.

See Also

- Options Dialog (see page 470)

Symbols Dialog

The Symbols dialog lets you to define, copy, and edit symbols for the entire system.



User-defined symbols are indicated by S.

Symbols files are indicated by 🗎. Symbol files can be either compiler-generated object files containing symbols or general-purpose ASCII (GPA) format symbol files.

Load...	If a bus/signal is selected, this opens the Select Symbol File dialog for loading symbols from a compiler-generated object file or a general-purpose ASCII (GPA) format symbol file. If symbol file is selected, it is reloaded.
Add...	Adds a user-defined symbol to the selected bus/signal.
Edit...	Edits the selected user-defined symbol.
Delete Delete All	Removes the selected user-defined symbol or symbol file (or all symbols if a bus/signal is selected) from the list.
Move Up Move Down	Moves the selected user-defined symbol or symbol file up or down within the list. When the system looks for a symbol that corresponds to a bus/signal value, the first match is used. (More than one symbol can match a given value.)

See Also

- Setting Up Symbols (see page 116)
- Displaying Names (Symbols) for Bus/Signal Values (see page 232)

System Summary Dialog

The System Summary dialog is used to see summary information about all modules in the system including a physical view of the cards in the system (Slot Summary (see page 493)), a list of all of the modules and their trigger times (Module Summary (see page 494)), and a list of how to connect all of the probes (Probe Summary (see page 495)).

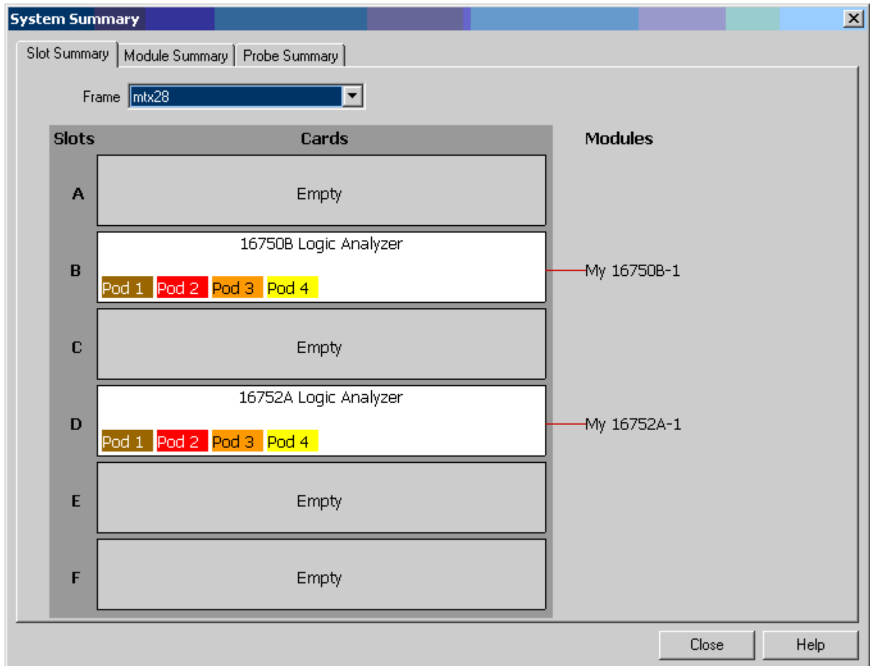
- Slot Summary Tab (see page 493)
- Module Summary Tab (see page 494)
- Probe Summary Tab (see page 495)

See Also

- Analyzer Setup Dialog (see page 447)

Slot Summary Tab

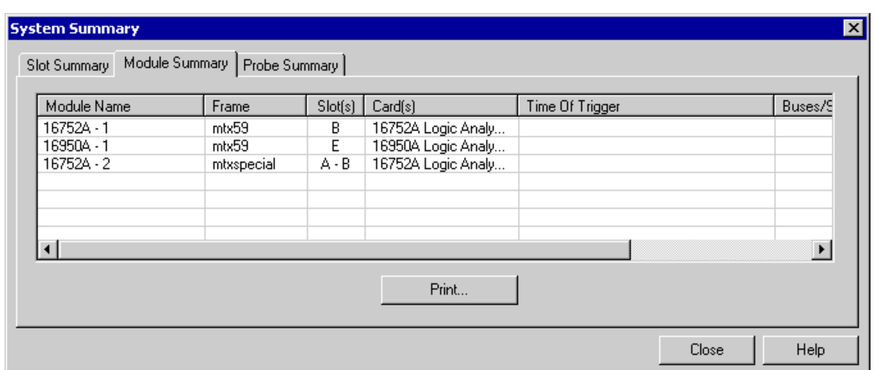
For the selected *frame* (see page 649) (if there are multiple frames), the Slot Summary tab shows: the *slots* (see page 653), *cards* (see page 648), and *modules* (see page 650) in the logic analysis system frame, or the *cards* (see page 648) and *modules* (see page 650) in the standalone logic analyzer.



See Also • System Summary Dialog (see page 493)

Module Summary Tab

For each *module* (see page 650) in the logic analysis system, the Module Summary tab shows the *frame* (see page 649) in which the module resides, the *cards* (see page 648) that make up the module, the *slots* (see page 653) in which these cards reside, and the time that a trigger occurred.



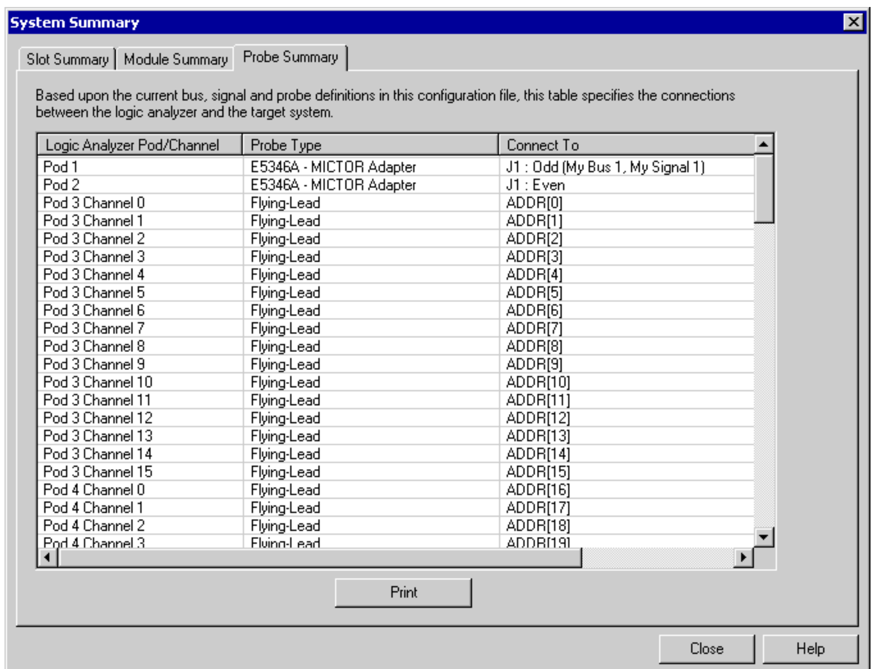
See Also • System Summary Dialog (see page 493)

Probe Summary Tab

The Probe Summary tab shows logic analyzer pods and channels, probe types, and the connectors or signals in the device under test to which the pods and channels should be connected.

Probe types can be defined by themselves, in XML configuration files, or while importing netlists (see page 91) (to assign bus/signal names to logic analyzer channels). If you haven't defined probe types, the flying-lead probe type is assumed.

NOTE When connecting differential probe channel pin/pad/lead pairs to single-ended signals, make sure the negative pin/pad/lead is connected to ground and the positive pin/pad/lead is connected to the single-ended signal.



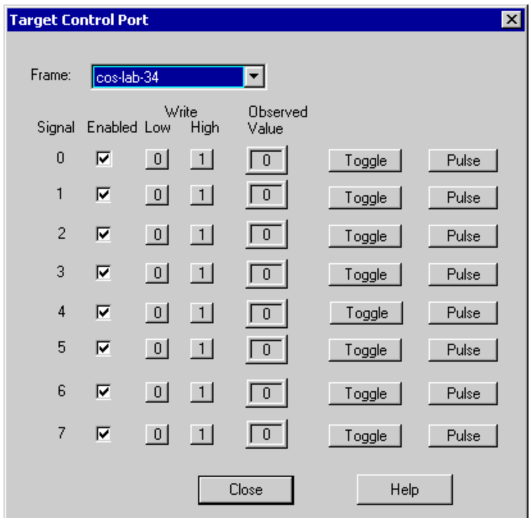
See Also

- "To define probes" (in the online help)
- System Summary Dialog (see page 493)
- "Connecting Probes Using the Probe Summary" (in the online help)

Target Control Port Dialog

The 16900A, 16902A, and 16903A logic analysis system *frames* (see page 649) have a *target control port*, an 8-bit, 3.3V port that can be used to send signals to a device under test. The target control port does not function like a pattern generator, but more like a remote control for switches in the device under test.

For the selected frame (if there are multiple frames), the Target Control Port dialog lets you set the output signal levels on the port.



Signal	Identifies the target control port signal.
Enabled	Lets you enable or disable an output signal on the target control port. When disabled, the signal has a tri-state high-impedance output. When enabled, the signal outputs a standard 3.3V logic level with 1 high and 0 low.
Write	Gives you two buttons, **0** and **1**, for changing the signal output value to a standard 3.3V logic low or high, respectively.
Observed Value	Displays the signal value observed on the target control port signal.
Toggle	Flips the settings of the signal and leaves them that way. For example, if your signal is set to 1 and you click **Toggle**, the setting changes to 0.
Pulse	Flips the settings for one clock cycle, which is at least 16 ms. The pulse may last longer. You cannot specify the duration of the pulse.

See Also

- To control signals in the device under test (see page 61)

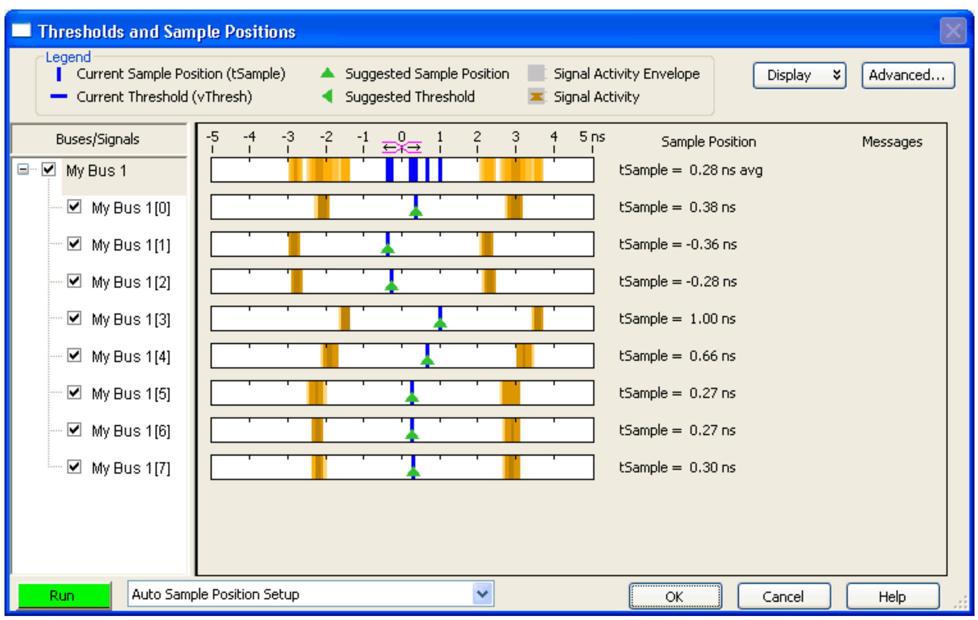
Thresholds and Sample Positions Dialog

The Thresholds and Sample Positions dialog lets you position the logic analyzer's setup/hold window (or sampling position) and specify the threshold voltage so that data on high-speed buses is captured accurately, in other words, so that data is sampled when it is valid.

When the device under test's data valid window is less than 2.5 ns (roughly, for clock speeds >= 200 MHz), it's easiest to use *eye finder* to locate the stable and transitioning regions of signals and to automatically adjust sampling positions.

Eye finder measures the location of the stable region boundaries and places the logic analyzer's sampling position in the center of the stable region. *Eye finder* also adjusts the threshold voltage setting to maximize the width of the measured stable regions.

When the device under test's data valid window is greater than 2.5 ns (roughly, for clock speeds < 200 MHz), it's easiest to adjust the sampling position manually, without using the logic analyzer to locate the stable and transitioning regions of signals.

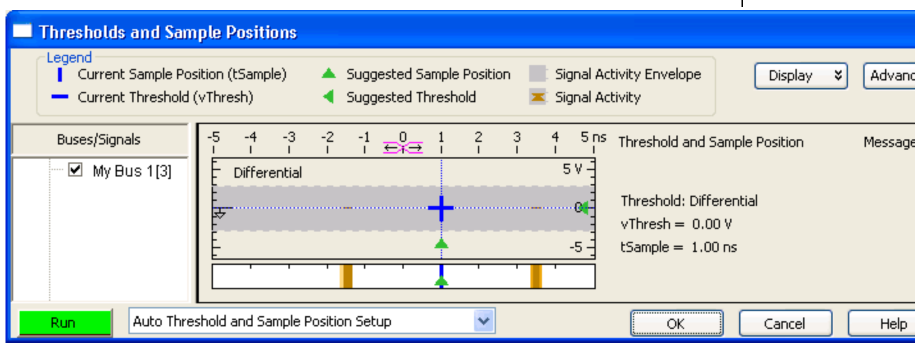


Legend	Describes items you see in the bus/signal diagram.
Display	Lets you display or hide: • Threshold and Sample Position column. • Messages column. • Voltage information.

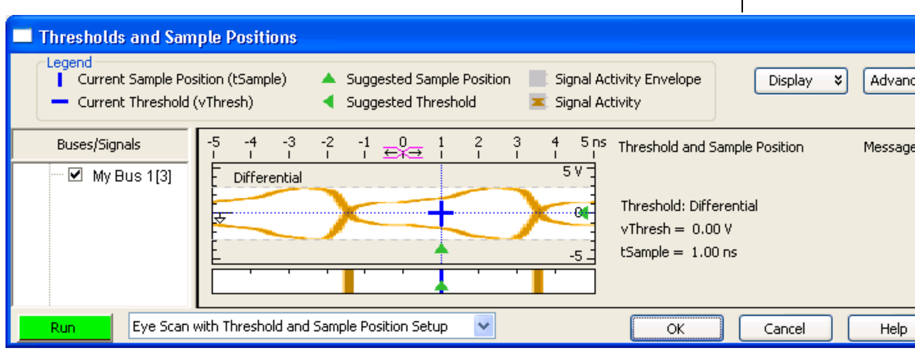
Advanced...	Opens the Eye Finder Advanced Options dialog (see page 500) for setting measurement duration and run mode options.
Buses/Signals	Lets you choose the buses/signals to run *eye finder* on. You can expand or overlay the signals in a bus, select all or select none of the signals, select individual signals, or select multiple signals. If a channel appears in multiple buses/signals, selecting that channel will select it in each of those buses/signals. After *eye finder* is run, you can right-click on a bus/signal name and choose **Properties...** to open the Eye Finder Properties dialog (see page 501) for viewing additional information about the measurement results.
Bus/Signal Diagram	Displays a digital "eye" diagram that represents many samples of data captured in relation to the sampling clock. The transitioning edges measured before and after the sampling clock result in a picture that is eye-shaped. The display area shows: • Transitioning (dark) and stable (light) regions on the signals. Intensity shows where transitions are more prevalent (darker orange) and less prevalent (lighter). • Suggested sampling positions (green triangles). • The current sampling positions (vertical blue lines in stable regions, red lines in transitioning regions). • When voltage information is displayed, the current threshold voltage settings are shown (horizontal blue lines in stable regions, red lines in transitioning regions). If you click and drag the "+" formed by the sampling position and threshold setting lines, both are adjusted; to adjust the settings individually, click and drag the appropriate dotted line. Note that adjusting threshold settings affects all channels on the same pod (and sometimes the clock input on the pod as well). To give you more information about the signals, the display covers +/-5 ns even though the sampling position may only be set to +/-3.25 ns.
Threshold and Sample Position	Shows the numeric values of the threshold voltage and sample position settings. Clicking in this column gives you entry fields for adjusting the settings. You can also drag the sample position and threshold voltage bars to new locations.
Messages	This column displays: • Informational message icons. You can move the mouse pointer over the icon to cause the message to pop up. • Time stamp information that shows when the last *eye finder* measurement was run.

<table>
<tr><td>Run</td><td>Runs eye finder to automatically adjust state sampling positions and threshold voltage settings.</td></tr>
<tr><td>(Type of Run)</td><td>Specifies the type of eye finder run. You can choose from:

Auto Sample Position Setup. Tells eye finder to perform a scan that will result in the automatic setting of sample positions only. Threshold voltage settings are not changed.
Auto Threshold and Sample Position Setup. Tells eye finder to find the signal activity envelope and optimal threshold voltage (by adjusting threshold voltages and watching activity indicators) and then to perform a scan at that threshold that will result in the automatic setting of sample positions. For example:



Eye Scan with Threshold and Sample Position Setup. Tells eye finder to perform scans across the full signal activity envelope that will result in a bus/signal "eye" diagram (that has more voltage information) and the automatic setting of threshold voltages and sample positions. For example, here is the eye scan for one signal:



Eye Scan with Sample Position Setup Only. Tells eye finder to perform scans across the full signal activity envelope that will result in a bus/signal "eye" diagram (that has more voltage information) and the automatic setting of sample positions only. Threshold voltage settings are not changed.
</td></tr>
</table>

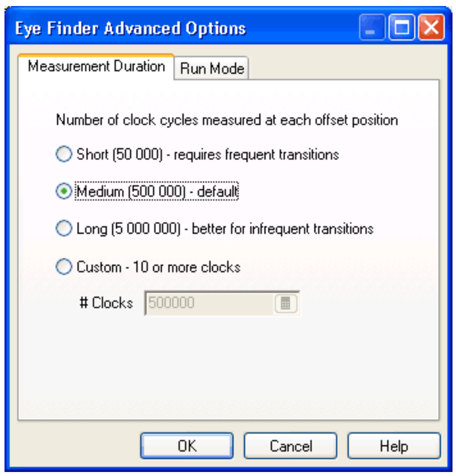
See Also

- Understanding State Mode Sampling Positions (see page 378)

- How Selected/Suggested Positions Behave (see page 502)
- Eye Finder Info Messages (see page 338)
- To automatically adjust state sampling positions and threshold voltages (see page 107)
- To manually adjust state sampling positions (see page 110)

Eye Finder Advanced Options Dialog

Measurement Duration



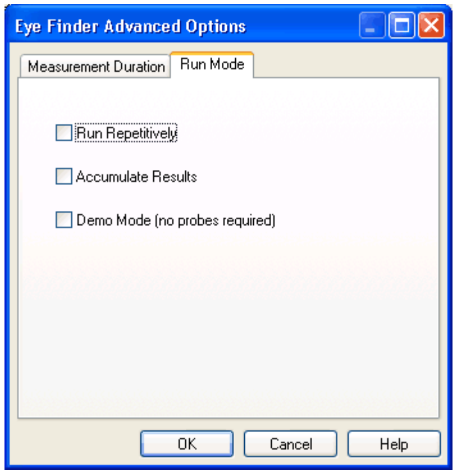
Short	*Eye finder* looks at 50,000 clock cycles on each channel to determine the suggested sampling positions. This setting requires frequent transitions on all channels.
Medium	*Eye finder* looks at 500,000 clock cycles on each channel to determine the suggested sampling positions. Use this for channels that transition at a normal rate.
Long	*Eye finder* looks at 5 million clock cycles on each channel to determine the suggested sampling positions. Use this setting if some channels have sporadic transitions.
Custom	Lets you specify the number of clock cycles to sample on each channel at each sampling position (each point in time).

Some things to consider when selecting among the *eye finder* advanced settings are:

- Upper address bits that don't transition as frequently as lower address bits and require more clock cycles.
- Data buses that are driven by different circuitry at different times require enough clock cycles to observe the effects of each driver on the bus.

When different channels require different settings, you can run *eye finder* on channel subsets to avoid using the Long setting on a large number of channels.

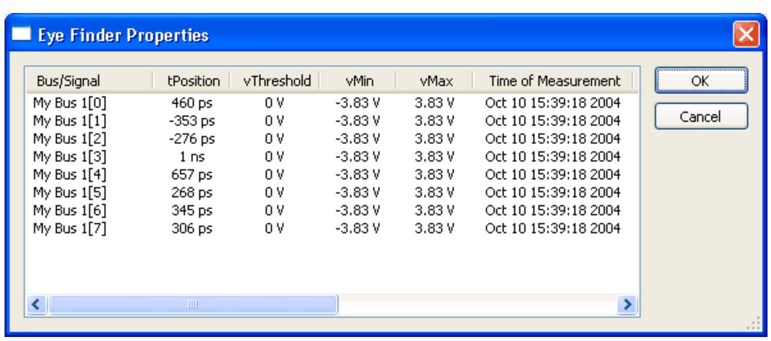
Run Mode



Run Repetitively	Runs the *eye finder* repetitively, so you can see how stable and transitioning signals vary over time.
Accumulate Results	When selected, *eye finder* data is accumulated from run-to-run. When unselected, *eye finder* data is erased before each run.
Demo Mode	Lets you look at *eye finder* with demo data. Demo mode does not generate full eye scan data.

Eye Finder Properties Dialog

The Eye Finder Properties dialog displays information about the *eye finder* measurement results.



Bus/Signal	The bus/signal name.
tPosition	The sample position.

vThreshold	The threshold voltage.
vMin	The minimum voltage in the signal activity envelope.
vMax	The maximum voltage in the signal activity envelope.
Time of Measurement	When *eye finder* was run.
# Accum	The number of accumulations that the data represents.
Status	The status information message from *eye finder* (see Eye Finder Info Messages (see page 338)).
Clock Spec	Identifies the sampling clock setup.
Sampling Mode	Identifies the slot and pod that the sampling clock comes from, as well as the state sampling clock mode used.

How Selected/Suggested Positions Behave

The *eye finder*'s selected and suggested sampling positions behave as follows:

How the Selected Position Behaves

1 The selected position (blue line in stable regions or red line in transitioning regions) can be dragged to the desired position without running *eye finder*.

2 The selected position is "snapped" to the suggested position (green triangle) each time *eye finder* is run on a channel.

How the Suggested Position Behaves

1 The suggested position (green triangle) is only shown in displays of a single channel.

2 There is only a suggested position on channels that have been measured.

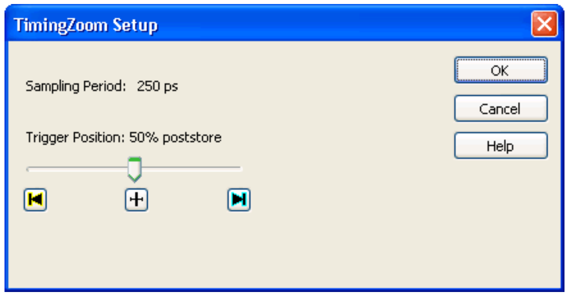
3 The suggested position is always in the center of the stable region closest to the selected position (blue or red line).

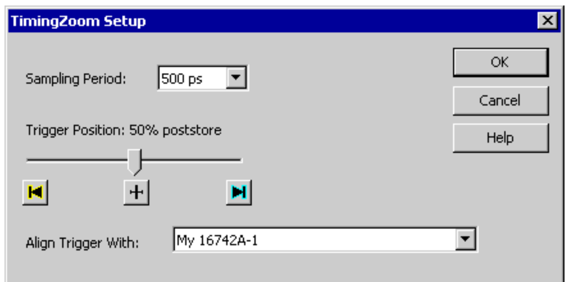
4 If the selected position is moved to a different stable region, the suggested position "hops" to the center of that region.

5 If a stable region is open-ended, the suggested position is placed a fixed distance from the closed end (the visible boundary); if more than one clock edge is active, the fixed distance is greater.

TimingZoom Setup Dialog

Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer.





Sampling Period	Displays the timing zoom sampling period. With some logic analyzers (see Logic Analyzer Notes, Timing Zoom (see page 574)), you can change the sampling period to see more or less sampling resolution around the trigger.
Trigger Position	Lets you position the timing zoom acquisition memory around the event that triggers the logic analyzer.
Align Trigger With	In some older logic analyzer modules, if the logic analyzer is split, this lets you specify which analyzer's trigger timing zoom should be aligned with.

See Also

- Using Timing Zoom (see page 112)
- Logic Analyzer Notes, Timing Zoom (see page 574)

Trigger Functions

The trigger functions available in the Advanced Trigger dialog give you pre-configured trigger setups for common measurements. If the trigger function you need is not available, start with a trigger function that is close, convert the trigger sequence step to advanced If/Then trigger functions, and edit the If/Then trigger functions.

- Timing Mode Trigger Functions (see page 504)
- State Mode Trigger Functions (see page 517)

See Also

- To show a trigger sequence step as Advanced If/Then trigger functions (see page 158)
- To convert a trigger sequence step to Advanced If/Then trigger functions (see page 159)
- Triggering From, and Sending Triggers To, Other Modules/Instruments (see page 162)

Timing Mode Trigger Functions

The following trigger setup examples are available as Trigger Functions in the Advanced Trigger dialog when in the timing acquisition mode. To see these trigger setups in the context of an example measurement refer to Making a timing analyzer measurement (see page 50).

Edge

- Edge (see page 505)
- "N" number of edges (see page 506)
- Edge and Pattern (see page 506)
- Edge followed by edge (see page 507)
- Edges too far apart (see page 507)
- Edge followed by pattern (see page 508)
- Pattern too late after edge (see page 508)

Bus Pattern

- Pattern (see page 509)
- Edge and Pattern (see page 506)
- Pattern present for > "T" time (see page 509)
- Pattern present for < "T" time (see page 510)
- Pattern absent for > "T" time (see page 510)
- Pattern absent for < "T" time (see page 511)
- Edge followed by pattern (see page 508)
- Pattern too late after edge (see page 508)

Other

- Find anything "N" times (see page 511)

- Width violation on pattern or pulse (see page 512)
- Wait "T" seconds (see page 512)
- Run until user stop (see page 513)
- Wait for external arm (see page 513)
- Wait for arm from another module (see page 513)

Advanced

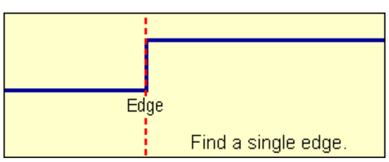
- Advanced If/Then (see page 514)
- Advanced 2-Way Branch (see page 514)
- Advanced 3-Way Branch (see page 515)
- Advanced 4-Way Branch (see page 516)
- Pattern "AND" Pattern (see page 516)
- Pattern "OR" Pattern (see page 517)

See Also

- To replace or insert trigger functions into trigger sequence steps (see page 143)
- State Mode Trigger Functions (see page 517)
- To store a trigger (see page 166)
- To recall a trigger (see page 167)

Edge

This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a user-defined edge occurs.

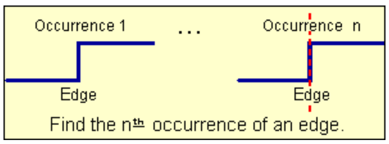


To edit this function

- Specifying Advanced Triggers (see page 138)

"N" number of edges

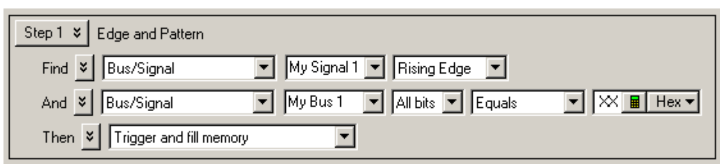
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when the "Nth" occurrence of a user-defined edge occurs.



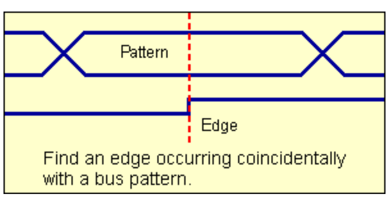
To edit this function

- Specifying Advanced Triggers (see page 138)

Edge and Pattern



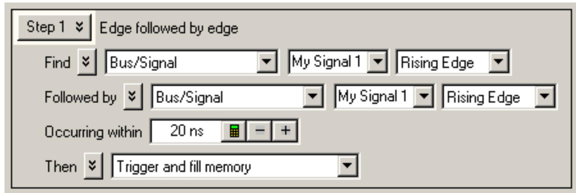
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when both a user-defined edge and bus pattern occur at the same time.



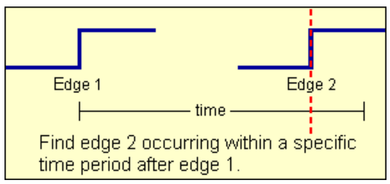
To edit this function

- Specifying Advanced Triggers (see page 138)

Edge followed by edge



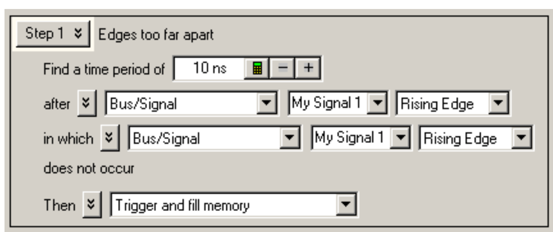
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when edge 2 occurs within a specified time period after edge 1.



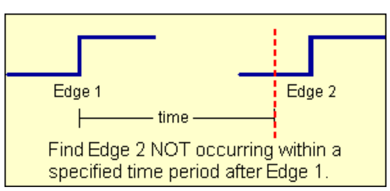
To edit this function

- Specifying Advanced Triggers (see page 138)

Edges too far apart



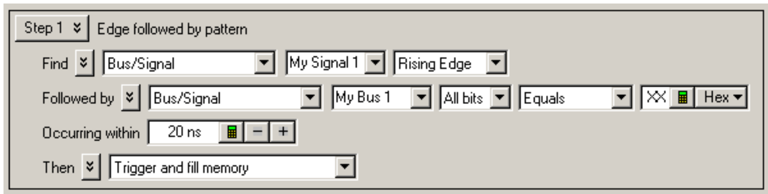
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when edge 2 does not occur within a specified time period after edge 1.



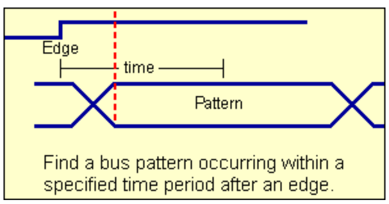
To edit this function

- Specifying Advanced Triggers (see page 138)

Edge followed by pattern



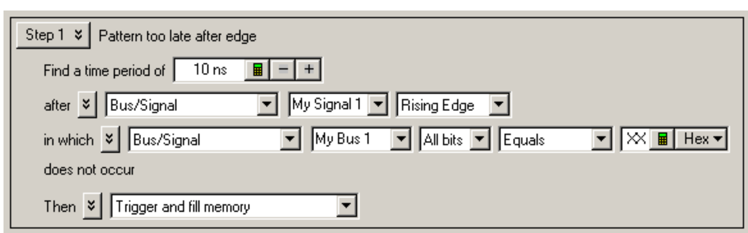
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a bus pattern occurs within a specified time period after an edge.



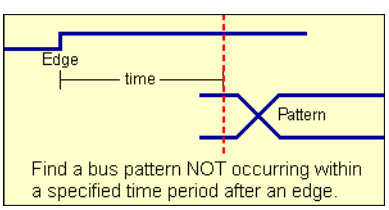
To edit this function

- Specifying Advanced Triggers (see page 138)

Pattern too late after edge



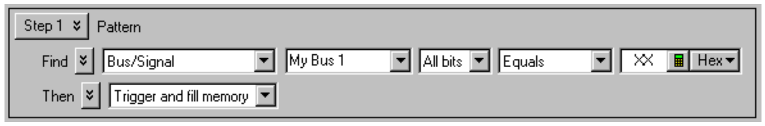
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a specified bus pattern does not occur within a specified time period after an edge.



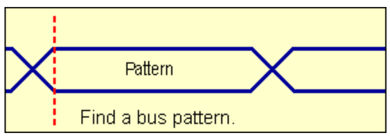
To edit this function

- Specifying Advanced Triggers (see page 138)

Pattern



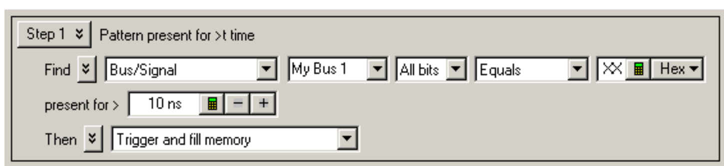
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a designated bus pattern occurs.



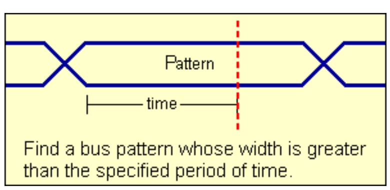
To edit this function

- Specifying Advanced Triggers (see page 138)

Pattern present for > "T" time



This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a user-defined bus pattern is present greater than a specified time period.

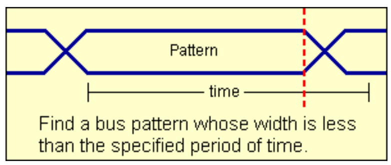


To edit this function

- Specifying Advanced Triggers (see page 138)

Pattern present for < "T" time

This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a user-defined bus pattern is present less than a specified time period.

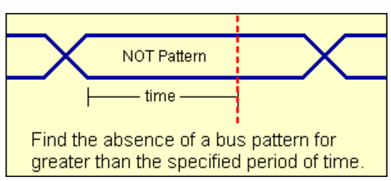


To edit this function

- Specifying Advanced Triggers (see page 138)

Pattern absent for > "T" time

This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a user-defined bus pattern is absent greater than a specified time period.

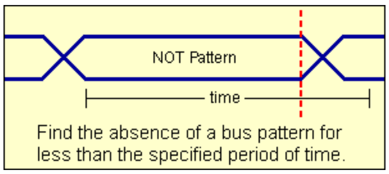


To edit this function

- Specifying Advanced Triggers (see page 138)

Pattern absent for < "T" time

This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a user-defined bus pattern is absent less than a specified time period.

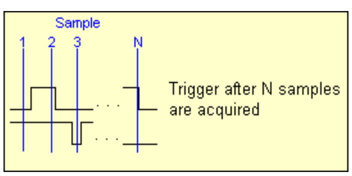


To edit this function

- Specifying Advanced Triggers (see page 138)

Find anything "N" times (timing)

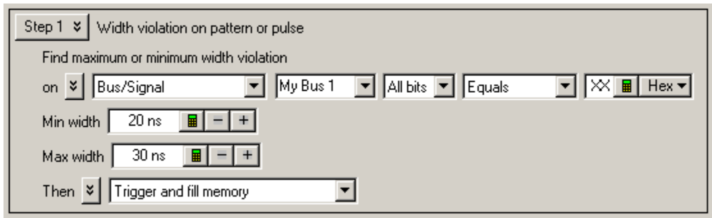
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when it sees any data (Anything) for the Nth time.



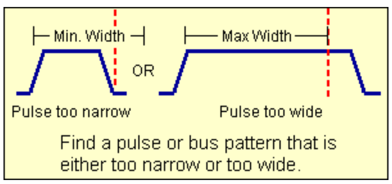
To edit this function

- Specifying Advanced Triggers (see page 138)

Width violation on pattern or pulse



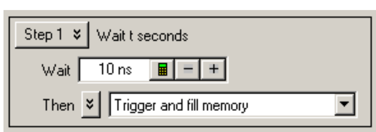
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a pulse or bus pattern is found that is either too narrow or too wide.



To edit this function

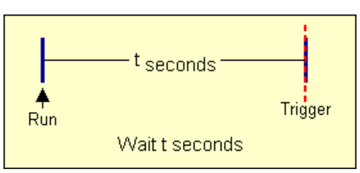
- Specifying Advanced Triggers (see page 138)

Wait "T" seconds



This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers after the specified time period expires.

The maximum amount of time you can enter is based on the logic analyzer's sampling period. If you need to wait longer than the maximum time allowed, you can use a timer (see page 140) instead.

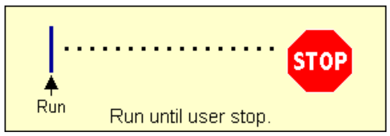


To edit this function

- Specifying Advanced Triggers (see page 138)

Run until user stop (timing)

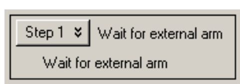
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. This trigger function sets up to never trigger. You must select the stop button to view the captured data.



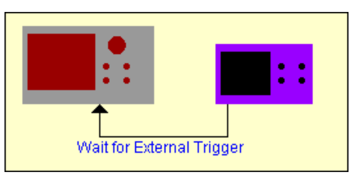
To edit this function

- Specifying Advanced Triggers (see page 138)

Wait for external arm (timing)



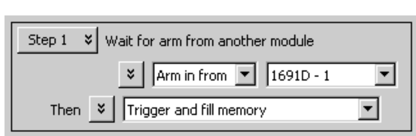
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when an external arming signal appears through the external **Trigger In** port (see Triggering From, and Sending Triggers To, Other Modules/Instruments (see page 162)). The **Trigger In** BNC connector is located on the rear panel of the 16800-series logic analyzers, 1680-series logic analyzers, and 16900-series logic analysis systems; it is located on the front panel of the 1690-series logic analyzers.



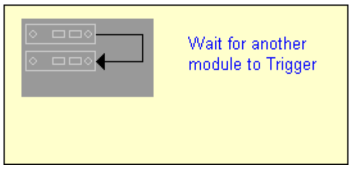
To edit this function

- Specifying Advanced Triggers (see page 138)

Wait for arm from another module (timing)



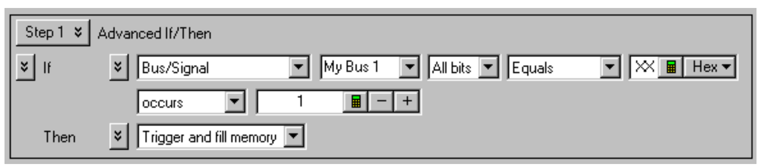
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when an arming signal from another module occurs (see Triggering From, and Sending Triggers To, Other Modules/Instruments (see page 162)).



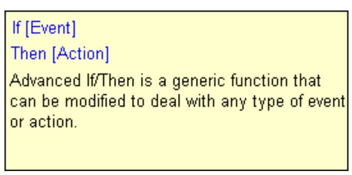
To edit this function

- Specifying Advanced Triggers (see page 138)

Advanced If/Then (timing)



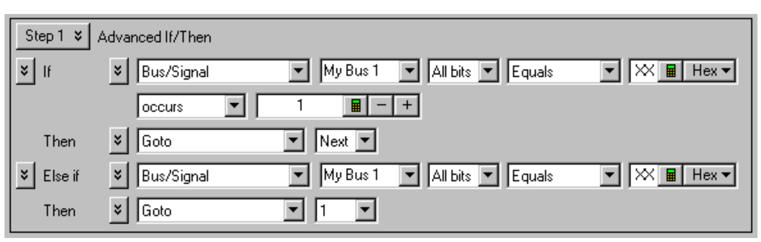
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when the "If" clause becomes true.



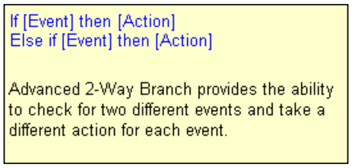
To edit this function

- Specifying Advanced Triggers (see page 138)

Advanced 2-Way Branch (timing)



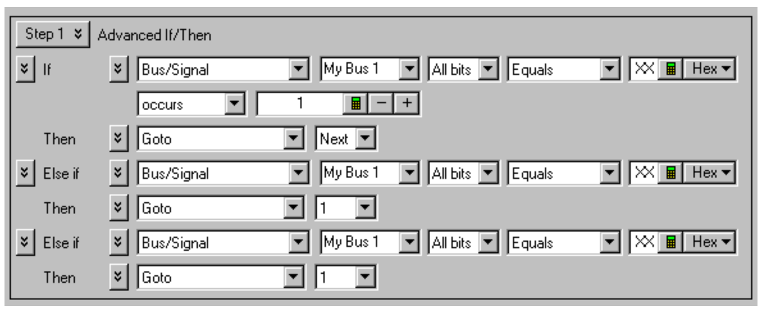
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The two-way branch is evaluated true when either of two patterns (if or Else if) are found. Depending on which pattern is found true, the appropriate "Then" action is executed.



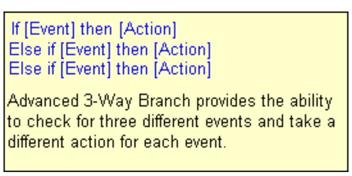
To edit this function

- Specifying Advanced Triggers (see page 138)

Advanced 3-Way Branch (timing)



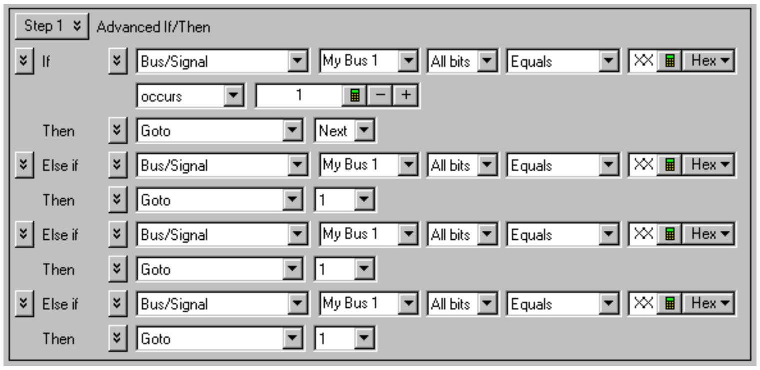
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The three-way branch is evaluated true when either of three patterns (If or Else if) are found. Depending on which pattern is found true, the appropriate "Then" action is executed.



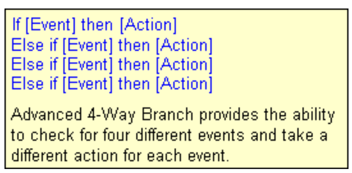
To edit this function

- Specifying Advanced Triggers (see page 138)

Advanced 4-Way Branch (timing)



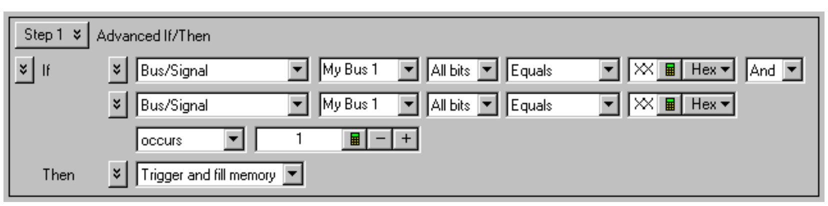
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The four-way branch is evaluated true when either of four patterns (If or Else if) are found. Depending on which pattern is found true, the appropriate "Then" action is executed.



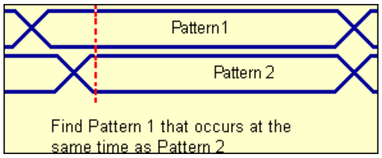
To edit this function

- Specifying Advanced Triggers (see page 138)

Pattern "AND" Pattern (timing)



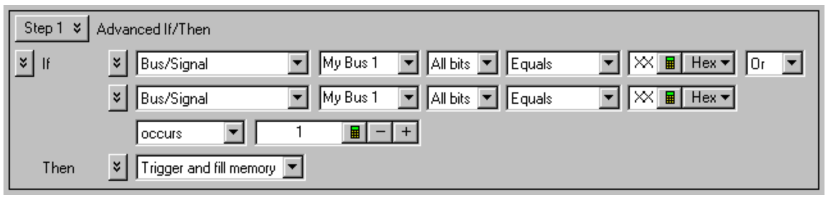
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when both pattern1 "AND" pattern2 occur at the same time, and for the specified numbers of samples (occurs).



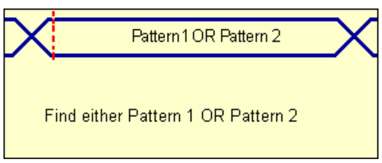
To edit this function

- Specifying Advanced Triggers (see page 138)

Pattern "OR" Pattern (timing)



This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when either pattern1 "OR" pattern2 occurs for the specified numbers of samples (occurs).



To edit this function

- Specifying Advanced Triggers (see page 138)

State Mode Trigger Functions

The following trigger setup examples are available as Trigger Functions in the Advanced Trigger dialog when in the state acquisition mode. To see these trigger setups in the context of an example measurement refer to Making a state analyzer measurement (see page 51).

Patterns

- Pattern "N" times (see page 518)
- "N" consecutive samples with Pattern1 (see page 519)
- Pattern1 followed by Pattern2 (see page 519)
- Pattern1 immediately followed by Pattern2 (see page 520)
- Pattern1 followed by Pattern2 before Pattern3 (see page 520)
- Too few states between Pattern1 and Pattern2 (see page 521)
- Too many states between Pattern1 and Pattern2 (see page 522)

- Pattern2 occurring too soon after Pattern1 (see page 522)
- Pattern2 occurring too late after Pattern1 (see page 523)
- Find a packet (see page 524)

Other

- Reset and start timer (see page 524)
- Find anything "N" times (see page 525)
- Run until user stop (see page 525)
- Wait for external arm (see page 526)
- Wait for arm from another module (see page 526)
- Wait "N" external clock states (see page 527)

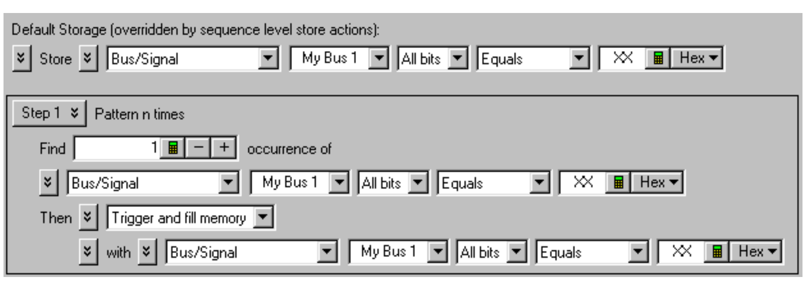
Advanced

- Advanced If/Then (see page 527)
- Advanced 2-Way Branch (see page 528)
- Advanced 3-Way Branch (see page 529)
- Advanced 4-Way Branch (see page 529)
- Pattern "AND" Pattern (see page 530)
- Pattern "OR" Pattern (see page 531)

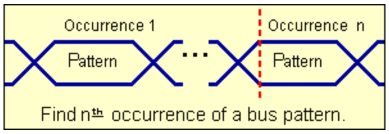
See Also

- To replace or insert trigger functions into trigger sequence steps (see page 143)
- Timing Mode Trigger Functions (see page 504)
- To specify default storage (see page 149)
- To store a trigger (see page 166)
- To recall a trigger (see page 167)

Pattern "N" times



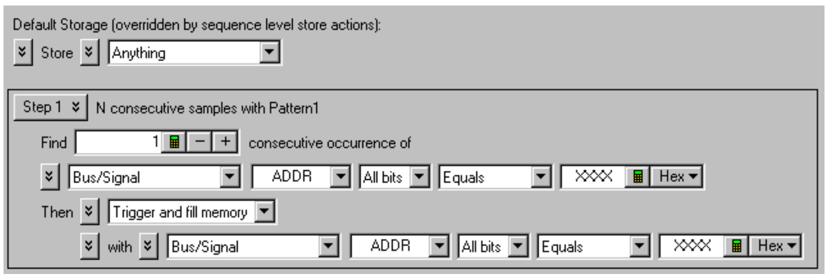
This trigger function is available when the acquisition mode is set to **State - Synchronous**. It will trigger the logic analyzer when it finds the nth occurrence of a bus pattern as shown below.



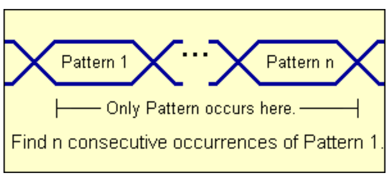
To edit this function

- Specifying Advanced Triggers (see page 138)

"N" consecutive samples with Pattern1



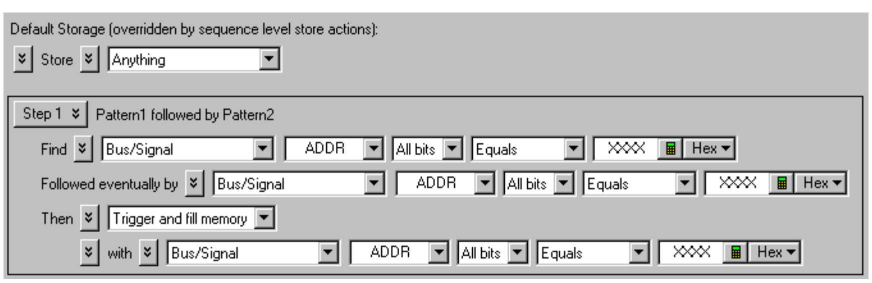
This trigger function is available when the acquisition mode is set to **State - Synchronous**. It will trigger the logic analyzer when a bus pattern occurs a specified number times.



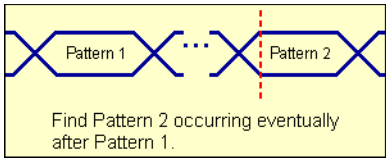
To edit this function

- Specifying Advanced Triggers (see page 138)

Pattern1 followed by Pattern2



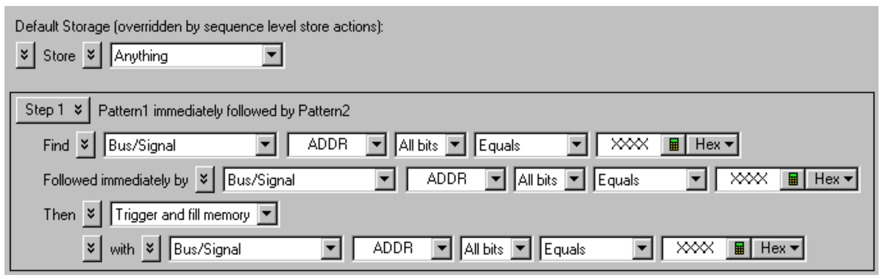
This trigger function is available when the acquisition mode is set to **State - Synchronous**. It will trigger the logic analyzer when pattern2 occurs eventually after pattern 1.



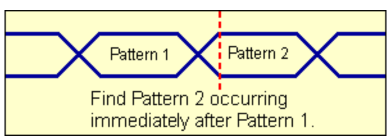
To edit this function

- Specifying Advanced Triggers (see page 138)

Pattern1 immediately followed by Pattern2



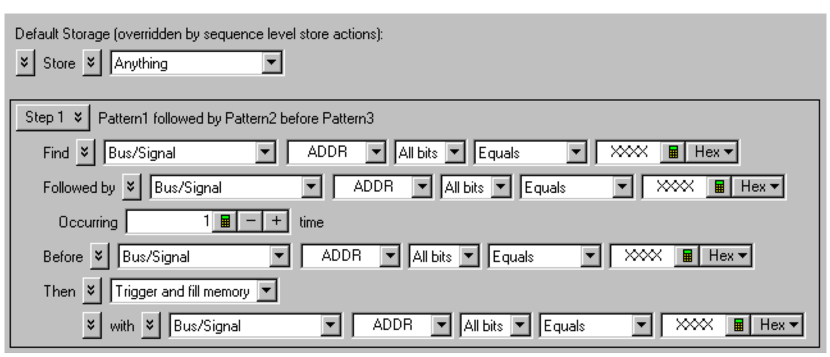
This trigger function is available when the acquisition mode is set to **State - Synchronous**. It will trigger the logic analyzer when pattern 2 is found immediately after exiting pattern 1.



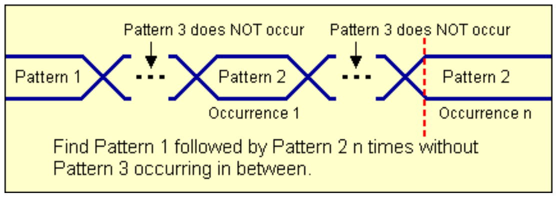
To edit this function

- Specifying Advanced Triggers (see page 138)

Pattern1 followed by Pattern2 before Pattern3



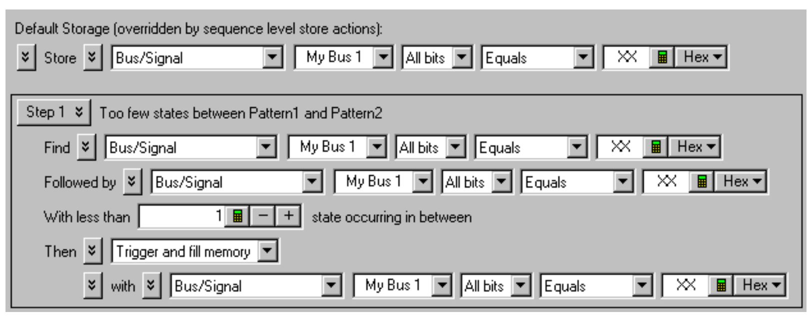
This trigger function is available when the acquisition mode is set to **State - Synchronous**. It will trigger the logic analyzer when pattern2 occurs eventually after pattern1, for a specified number of times, without pattern3 occurring in between.



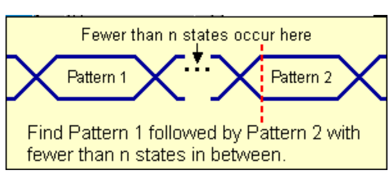
To edit this function

• Specifying Advanced Triggers (see page 138)

Too few states between Pattern1 and Pattern2



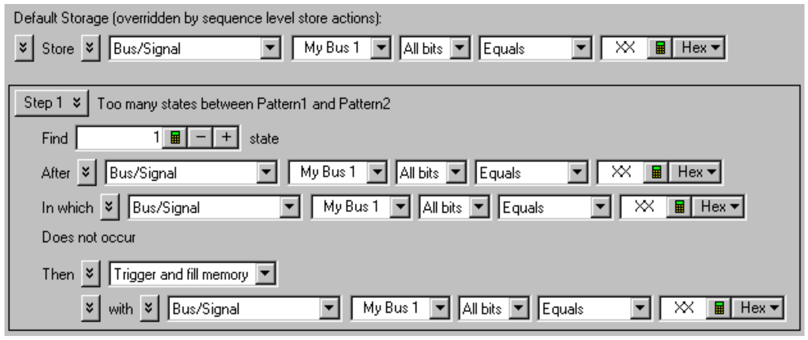
This trigger function is available when the acquisition mode is set to **State - Synchronous**. It will trigger the logic analyzer when pattern1 is followed by pattern2 with fewer than "N" specified states in between.



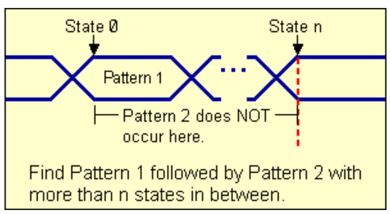
To edit this function

• Specifying Advanced Triggers (see page 138)

Too many states between Pattern1 and Pattern2



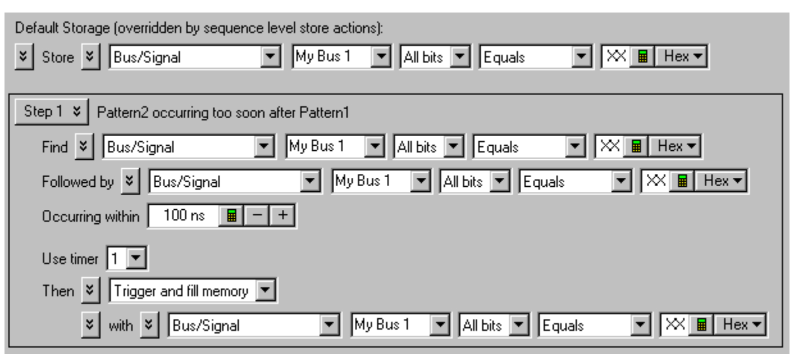
This trigger function is available when the acquisition mode is set to **State - Synchronous**. It will trigger the logic analyzer when pattern1 is followed by pattern2 with more than "N" specified states in between.



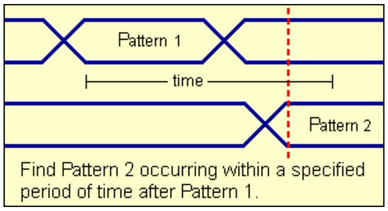
To edit this function

- Specifying Advanced Triggers (see page 138)

Pattern2 occurring too soon after Pattern1



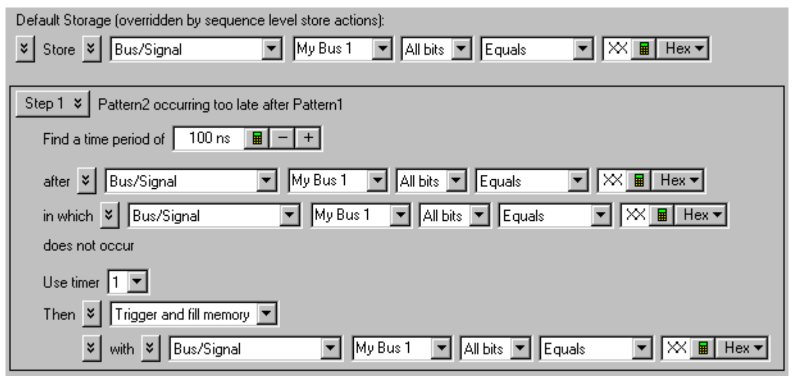
This trigger function is available when the acquisition mode is set to **State - Synchronous**. It will trigger the logic analyzer when pattern2 occurs within a specified time period after pattern1.



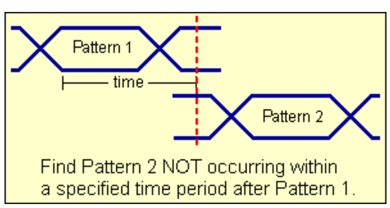
To edit this function

- Specifying Advanced Triggers (see page 138)

Pattern2 occurring too late after Pattern1



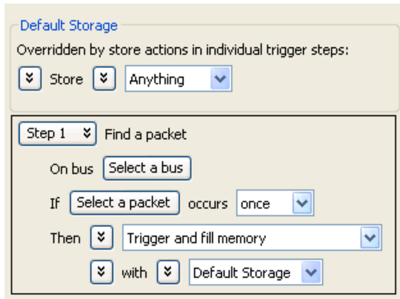
This trigger function is available when the acquisition mode is set to **State - Synchronous**. It will trigger the logic analyzer when pattern2 does not occur within a specified time period after pattern1.



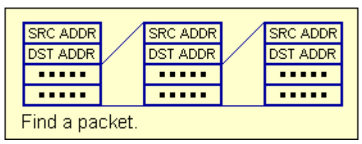
To edit this function

- Specifying Advanced Triggers (see page 138)

Find a packet



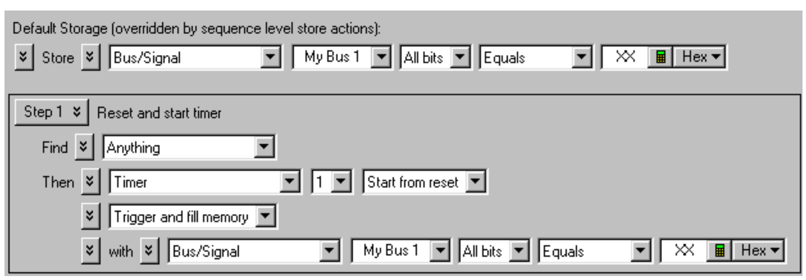
This trigger function is available when the acquisition mode is set to **State - Synchronous**. It will trigger the logic analyzer when the selected packet and occurrence is found.



To edit this function

- Specifying Advanced Triggers (see page 138)

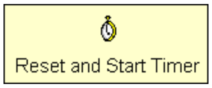
Reset and start timer (state)



NOTE

This trigger function is not available in the 1683A/AD and 1693A/AD models because they do not have timers available.

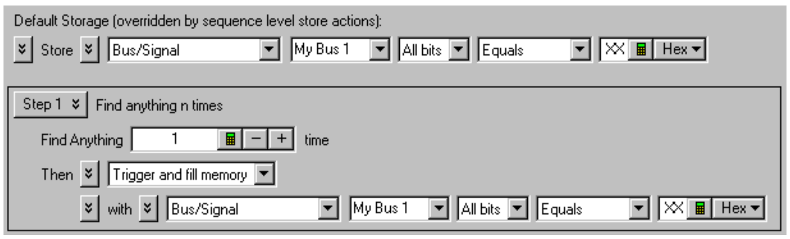
This trigger function is available when the acquisition mode is set to **State - Synchronous**. This trigger function resets a timer, then starts the timer for a specified period of time. This trigger function requires that the timer value be set in either the same trigger step, or another trigger step that follows. When the timer stops, the analyzer triggers. For more information refer to "To configure a timer (see page 140)".



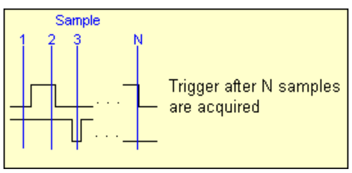
To edit this function

- Specifying Advanced Triggers (see page 138)

Find anything "N" times (state)



This trigger function is available when the acquisition mode is set to **State - Synchronous**. It will trigger the logic analyzer when any data (Anything) is seen for the Nth time. It is commonly used to create an immediate trigger, or a trigger after a user-defined delay.

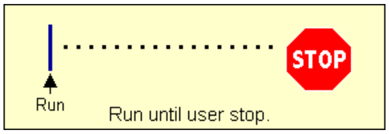


To edit this function

- Specifying Advanced Triggers (see page 138)

Run until user stop (state)

This trigger function is available when the acquisition mode is set to **State - Synchronous**. This trigger function sets up to never trigger. You must select the stop button to view the captured data.

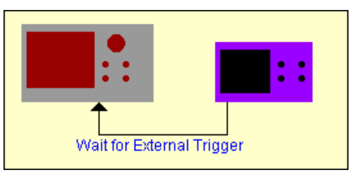


To edit this function

- Specifying Advanced Triggers (see page 138)

Wait for external arm (state)

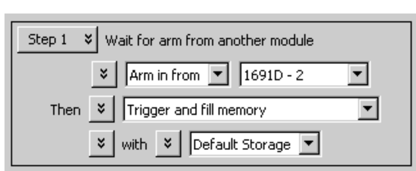
This trigger function is available when the acquisition mode is set to **State - Synchronous**. The analyzer triggers when an external arming signal appears through the external **Trigger In** port (see Triggering From, and Sending Triggers To, Other Modules/Instruments (see page 162)). The **Trigger In** BNC connector is located on the rear panel of the 16800-series logic analyzers, 1680-series logic analyzers, and 16900-series logic analysis systems; it is located on the front panel of the 1690-series logic analyzers.



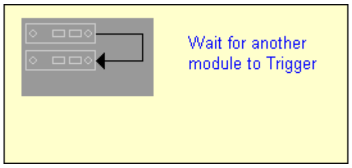
To edit this function

- Specifying Advanced Triggers (see page 138)

Wait for arm from another module (state)



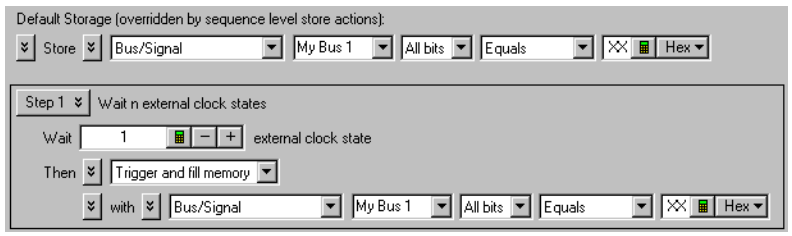
This trigger function is available when the acquisition mode is set to **State - Synchronous**. The analyzer triggers when an arming signal from another module occurs (see Triggering From, and Sending Triggers To, Other Modules/Instruments (see page 162)).



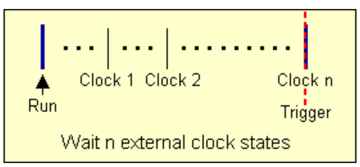
To edit this function

- Specifying Advanced Triggers (see page 138)

Wait "N" external clock states



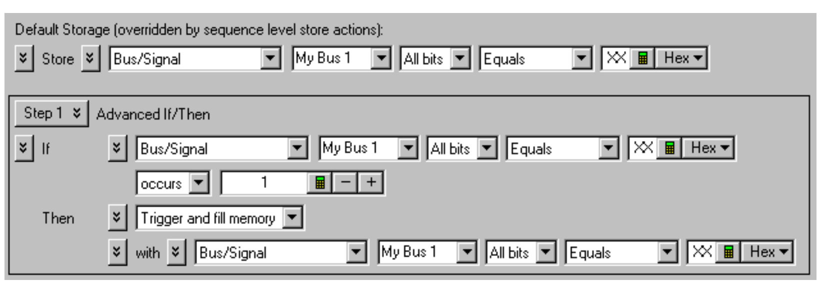
This trigger function is available when the acquisition mode is set to **State - Synchronous**. The analyzer triggers on the "Nth" occurrence of the external clock signal (plus any user-defined clock qualification) from the device under test.



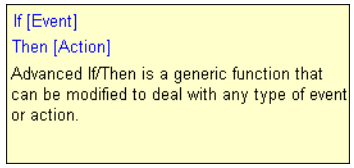
To edit this function

- Specifying Advanced Triggers (see page 138)

Advanced If/Then (state)



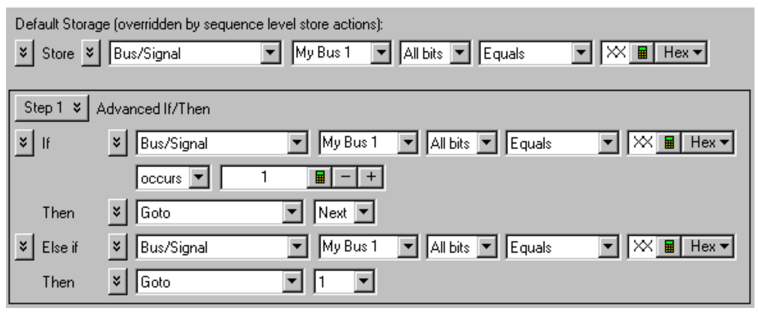
This trigger function is available when the acquisition mode is set to **State - Synchronous**. The analyzer triggers when the "If" clause becomes true.



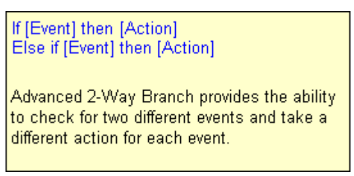
To edit this function

- Specifying Advanced Triggers (see page 138)

Advanced 2-Way Branch (state)



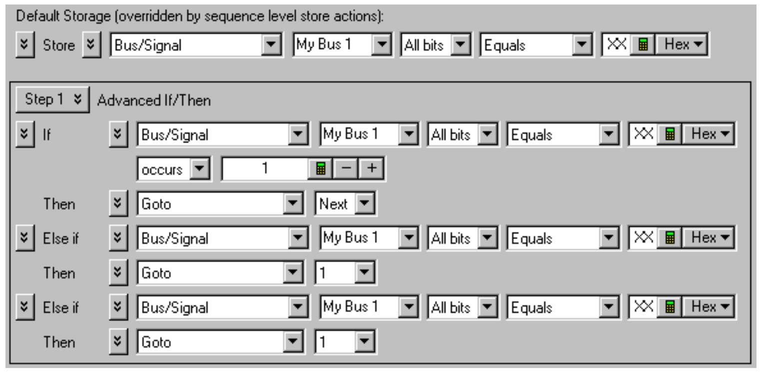
This trigger function is available when the acquisition mode is set to **State - Synchronous**. The two-way branch is evaluated true when either of two patterns (if or Else if) are found. Depending on which pattern is found true, the appropriate "Then" action is executed.



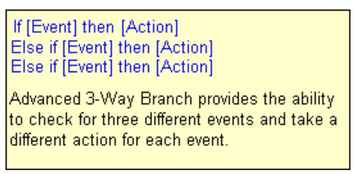
To edit this function

- Specifying Advanced Triggers (see page 138)

Advanced 3-Way Branch (state)



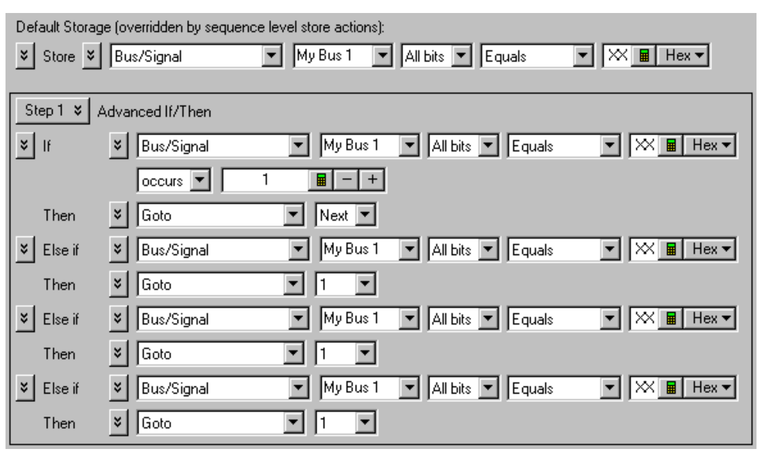
This trigger function is available when the acquisition mode is set to **State - Synchronous**. The three-way branch is evaluated true when either of three patterns (If or Else if) are found. Depending on which pattern is found true, the appropriate "Then" action is executed.



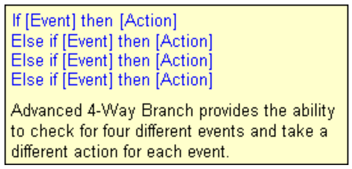
To edit this function

- Specifying Advanced Triggers (see page 138)

Advanced 4-Way Branch (state)



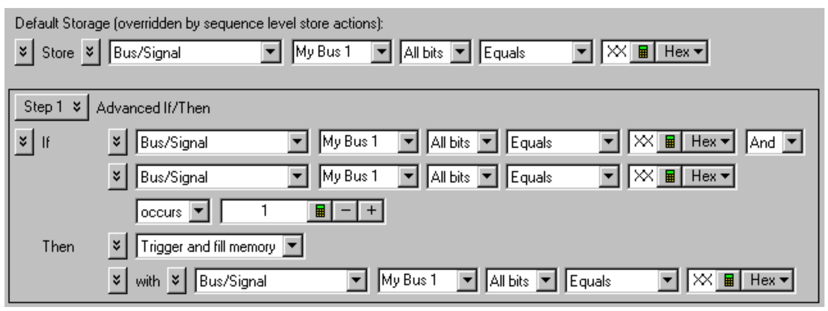
This trigger function is available when the acquisition mode is set to **State - Synchronous**. The four-way branch is evaluated true when either of four patterns (If or Else if) are found. Depending on which pattern is found true, the appropriate "Then" action is executed.



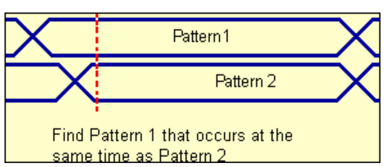
To edit this function

- Specifying Advanced Triggers (see page 138)

Pattern "AND" Pattern (state)



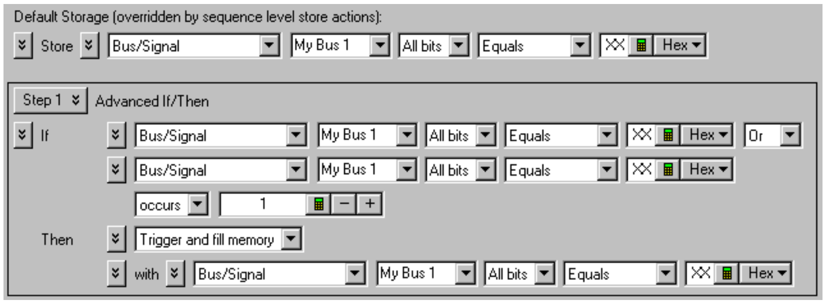
This trigger function is available when the acquisition mode is set to **State - Synchronous**. The analyzer triggers when both pattern1 "AND" pattern2 occur at the same time, and for the specified numbers of samples (occurs).



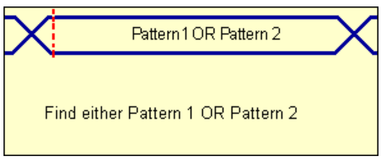
To edit this function

- Specifying Advanced Triggers (see page 138)

Pattern "OR" Pattern (state)



This trigger function is available when the acquisition mode is set to **State - Synchronous**. The analyzer triggers when either pattern1 "OR" pattern2 occurs for the specified numbers of samples (occurs).



To edit this function

- Specifying Advanced Triggers (see page 138)

Data Formats

Configuration File Formats

- ALA Format (see page 532)
- "XML Format" (in the online help)

Data Export/Import Formats

- Standard CSV Format (see page 532)
- Module CSV Format (see page 533)
- Module Binary (ALB) Format (see page 542)

ALA Format

The Agilent Logic Analyzer (ALA) format is the default format for saving configuration files. The ALA format is proprietary; ALA format configuration files are not intended to be read by programs other than the *Agilent Logic Analyzer* application.

ALA format configuration files contain everything that is needed to restore a session (in other words, the information necessary to reconstruct the display appearance, instrument settings, and optionally, captured data).

Configuration files are saved (see page 171) and opened (see page 184) through the File menu (see page 405).

Standard CSV Format

You can export captured data to CSV (Comma-Separated Values) format files which can then be imported by other applications like Excel.

Output is standard CSV format where the first row is the headings for the columns you have chosen to export (for example, buses/signal names, sample number, or time), and each successive row contains data for those columns, in the range specified, separated by commas (or other specified separation characters). For example:

```
"Sample Number","My Bus 1","My Signal 1","Time"
-10,FE,1,-13 ns
-9,FE,1,-10.5 ns
-8,FE,1,-8 ns
-7,FE,1,-5.5 ns
-6,FE,1,-3 ns
-5,FE,1,-500 ps
-4,FE,1,2 ns
-3,FE,1,4.5 ns
-2,FE,1,7 ns
-1,FE,1,9.5 ns
0,FF,1,12 ns
1,FF,1,14.5 ns
2,FF,1,17 ns
3,FF,1,19.5 ns
4,FF,1,22 ns
```

```
5,FF,1,24.5 ns
6,FF,1,27 ns
7,FF,1,29.5 ns
8,FF,1,32 ns
9,FF,1,34.5 ns
10,FF,1,37 ns
```

Module CSV Format

You can export captured data to module CSV (Comma-Separated Values) format files which can then be post-processed and re-imported into the logic analysis system using a *data import module*.

CAUTION Do not modify module CSV files with Microsoft Excel. When it saves the file, Excel will change the CSV format so that the data cannot be re-imported into the logic analysis system without a lot of manual text editing.

Module CSV format files contain a header section (see page 534) followed by comma separated values. For example:

```
AGILENT_CSV_DATA
HEADER_BEGIN
#
# -------------------------------------------------
#  Created: Dec 5, 2005 15:38:38
#  By: Agilent Logic Analyzer
# -------------------------------------------------
#
VALUE_SEPARATOR=","
VALUE_FILL_IN=ZEROS  # ZEROS, ONES, PREVIOUS, or ERROR
TRIGGER_CORRELATION_OFFSET=0.000000000000000e+000
TRIGGER_ROW=524288
NUM_ROWS=1048576
TIME_SOURCE PERIOD=2.000000000000000e-009
COLUMN "Sample Number" SAMPLE_NUMBER INTEGER
COLUMN "My Bus 1" VALUE UNSIGNED_INTEGER HEX WIDTH_BITS=8
COLUMN "My Bus 2" VALUE UNSIGNED_INTEGER HEX WIDTH_BITS=16
COLUMN "My Bus 3" VALUE UNSIGNED_INTEGER HEX WIDTH_BITS=32
COLUMN "My Signal 1" VALUE UNSIGNED_INTEGER HEX WIDTH_BITS=1
COLUMN "My Signal 2" VALUE UNSIGNED_INTEGER HEX WIDTH_BITS=1
COLUMN "Time" TIME FLOAT EXPONENT=-12 ABSOLUTE
HEADER_END
-524288,53,FFF0,004103E7,1,1,-1048576000
-524287,53,FFF0,004103E7,1,1,-1048574000
-524286,53,FFF0,004103E7,1,1,-1048572000
-524285,53,FFF0,004103E7,1,1,-1048570000
.
.
.
```

See Also

- Module CSV and Module Binary File Header Format (see page 534)
- Module CSV Format File Characteristics (see page 540)

Module CSV and Module Binary File Header Format

The header section comes at the beginning of the module CSV or module binary (ALB) file. The header definition is slightly different in the two cases.

`AGILENT_CSV_DATA AGILENT_BINARY_DATA`

REQUIRED: Key word tag to confirm the file type. The first is for module CSV text files. The second is for module binary (ALB) files. This tag must be the first characters 16 (or 19) characters in the file.

`#`

OPTIONAL: Comment character. All text following a # is ignored to the end of the line. Any line (except the first) may be a comment, except in module binary (ALB) files, where comments are only allowed in the header.

`HEADER_BEGIN`

REQUIRED: Key word tag to delimit the beginning of the header.

`TABLE_BEGIN "<name>" <TableType>`

A table represents data sampled at a specified timebase and sampling depth. A table can only represent a single timebase and sample depth.

OPTIONAL: If only one timebase and sample depth is needed, this keyword is not needed.

REQUIRED: If multiple timebases and sampling depths are needed, this keyword is needed to delimit the beginning of a table. The name may contain most printable characters, including embedded quote marks single or double), provided they are escaped with a backslash. For example, `TABLE_BEGIN "my \"perfect\" table" . . .`

Generally, each analog waveform channel has its own table, and there is only one table for digital channels.

When multiple tables are used, the binary data associated with each table is concatenated after the header.

`<TableType>:`

- `ANALOG`
- `DIGITAL`

An identifier is needed to explicitly determine what the table contains. There are specific fields that are required depending on the type of table. Analog requires the X/Y_INC/ORG/REF.

TIME_SOURCE PERIOD = <n.nnne-nn>

TIME_SOURCE FREQUENCY = <n.nnne+nn>

TIME_SOURCE COLUMN = "<columnName>"

OPTIONAL: How to assign a time tag to each sample row. PERIOD gives the sampling period; FREQUENCY gives the sample rate. COLUMN indicates which time column contains the time tags to use (ignored if PERIOD or FREQUENCY is given).

TRIGGER_ROW = <nnnn>

OPTIONAL: Row number containing the trigger sample, relative to the first data row in the file, which is row 0. The trigger row may be outside the range of rows in a file with a time line defined by a period or frequency, in which case it will be negative (trigger occurred before the first data row) or positive and greater than or equal to the number of data rows in the file (trigger occurred after the last data row in the file).

TRIGGER_CORRELATION_OFFSET = <n.nnne-nn>

OPTIONAL: Time offset in seconds (positive or negative) to apply to trigger (that is, to the T=0 reference) when correlating with data from other modules. If not given, 0.0 is assumed. The offset is rounded to the nearest picosecond.

NUM_ROWS = <nnn>

REQUIRED: If TABLE_BEGIN is present. Indicates the total number of data rows that will be read in from the file.

OPTIONAL: The expected number of data rows in the file. A warning is given if the number given does not match the actual number of rows in the file. This is provided as an optional sanity check to detect file truncation.

X_INC = <nnn.nnn>

OPTIONAL: Used for oscilloscope data processing.

X_ORG = <nnn.nnn>

OPTIONAL: Used for oscilloscope data processing.

`X_REF = <nnn>`

OPTIONAL: Used for oscilloscope data processing.

`Y_INC = <nnn.nnn>`

OPTIONAL: Used for oscilloscope data processing.

`Y_ORG = <nnn.nnn>`

OPTIONAL: Used for oscilloscope data processing.

`Y_REF = <nnn>`

OPTIONAL: Used for oscilloscope data processing.

`Y_MIN = <nnn.nnn>`

OPTIONAL: Used for oscilloscope data processing--the minimum voltage value represented in the data.

`Y_MAX = <nnn.nnn>`

OPTIONAL: Used for oscilloscope data processing--the maximum voltage value represented in the data.

`VALUE_SEPARATOR = "<ccc>"`

OPTIONAL, Module CSV only: One or more characters to be used as the separation character(s) between values in each row. If not given, the comma character is used. If the value for a column is missing (for example, two consecutive commas), its value is determined by the VALUE_FILL_IN property. The separation string may contain any printable character, and/or the blank and tab characters, except the following ambiguous characters:

- '#' — the comment character.
- '-', '+' — sign characters (signed decimal and floats).
- '.' — the period, used in floating point.
- a-f, A-F — hex.
- 0-9 — digits.

`VALUE_FILL_IN = PREVIOUS | ZEROS | ONES | ERROR`

OPTIONAL, Module CSV only: The value to be used for a skipped cell in a row. This attribute is optional. The default is `ZEROS`. `PREVIOUS` is consistent with the VCD file format and means "use the value from the cell above". ERROR indicates that any missing value should be treated as an error. This setting applies to all columns except TIME. Any missing time tag is an error.

BYTE_ORDER = LITTLE_ENDIAN | BIG_ENDIAN

OPTIONAL, Module binary (ALB) only: The order of bytes in a multi-byte value. An Intel-compatible system uses little endian as its internal format. This applies to both integer and floating point values. The default is LITTLE_ENDIAN.

LABEL "<name>" CHANNELS = "<ChannelDescription>" [HEX | DECIMAL | OCTAL | BINARY | SYMBOL]

OPTIONAL: As described below, a COLUMN represents a pod. If there are no LABELs defined, a LABEL is created by default which has the same characteristics as the COLUMN. If a LABEL is defined, it represents a subset of the data defined by the COLUMN. Another way to look at it is that a COLUMN defines the physical data that was exported and a LABEL is an interpretation of the data. The "<name>" may contain most printable characters, including embedded quote marks (single or double), provided they are escaped with a backslash. For example, LABEL "my \"perfect\" label". It is required that LABEL names be unique. If a duplicated name is found, only the first instance of the LABEL definition will be processed. There is an optional base which, if specified, will be the default label base. The default is HEX.

<ChannelDescription>

A channel description consists of the following format: <COLUMN_NAME>[bit position] with multiple channel descriptions separated by a comma. A <COLUMN_NAME> corresponds to the COLUMN name attribute. If there are multiple COLUMNs by the same name, the first one will be used. The bit position list is enclosed in [ ] and is order dependent. The MSB is on the left-hand side and the LSB is on the right-hand side For example, [7:0] represents bits 0-7 and [7,4,3,1] represents individual bits. 1, 3, 4, and 7. Bit patterns that are not monotonically increasing from right to left are considered reordered. For example, [1,3,4,7] represents bits 7 as the LSB and bit 1 as the MSB.

SYMBOL "<name>" LABEL = "<label or column name>" VALUE = "<value> | <value..value>" [HEX | DECIMAL | OCTAL | BINARY]

TABLE_END

REQUIRED: If TABLE_BEGIN is used.

```
HEADER_END
```

REQUIRED: The explicit end of the header. Information obtained from the header is evaluated at this point to determine if the file makes sense (for example, that a time base and one or more columns were defined).

Each line of a module CSV file (including sample rows following the header) are processed by first stripping the comment character and all characters following it, and then removing all leading whitespace (except blanks or tabs if a blank or tab is part of the delimiter string). If the resulting line is then empty, it is silently skipped. Otherwise, each data row is parsed using the definitions provided by the `COLUMN` definitions in the header, defined below.

COLUMN Syntax

One or more `COLUMN` definitions are required. The order of definitions in the header corresponds to the order of the columns in the data section. At least one of these must define a `VALUE` column. `COLUMN` syntax is more complicated than the other statements, so it is given in pieces:

```
COLUMN "<name>" <CSVcolumnType> | <ALBcolumnType>
```

These are the major parts of a `COLUMN` definition. The details are different for module CSV versus module binary (ALB) files. The name may contain most printable characters, including embedded quote marks (single or double), provided they are escaped with a backslash. For example, `COLUMN "my \"perfect\" data" . . .`

```
<CSVcolumnType>:
```

- `VALUE <CSVformat> WIDTH_BITS = <nnn>`
- `TIME <CSVformat> <timeUnit> ABSOLUTE | RELATIVE`
- `LINE_NUMBER <CSVformat>`
- `SAMPLE_NUMBER <CSVformat>`
- `IGNORE`

The column type gives the purpose of the values in the column.

Line numbers begin at 0 on the first row and increase by 1 for each subsequent row.

Sample numbers begin at 0 on the trigger row, decreasing by one for each row above the trigger row and increasing by one for each row after it.

Time columns give the time position for the sample. Absolute time positions are referenced to T=0 on the trigger row. Relative time positions give the amount of time elapsed from the arrival of the previous sample to the arrival of the sample on the row with the time tag.

Value columns contain data samples to be displayed in viewers in the application. The width in bits of a value is the width assigned to the pod which represents this column in the Bus/Signal setup page. Values are truncated (or expanded) to fit the width. Signed values are sign extended. Floating point values are converted to integers of the appropriate size (after applying the scale factor, if given).

`<ALBcolumnType>:`

- `VALUE NBYTES = <nnn> <ALBformat> WIDTH_BITS = <nnn>`
- `TIME NBYTES = <nnn> <ALBformat> <timeUnit> ABSOLUTE | RELATIVE`
- `LINE_NUMBER NBYTES = <nnn> <ALBformat>`
- `SAMPLE_NUMBER NBYTES = <nnn> <ALBformat>`
- `IGNORE NBYTES = <nnn>`

This is the same as `<CSVcolumnType>`, with the addition of an `NBYTES` attribute that gives the number of bytes in the binary data that are assigned to the column.

`<CSVformat>:`

- `INTEGER [HEX | DECIMAL | OCTAL | BINARY]`
- `UNSIGNED_INTEGER [HEX | DECIMAL | OCTAL | BINARY]`
- `FLOAT [SCALE = <nnn.nnn>]`

The column format describes the way the value is represented in the file. The base is optional, and defaults to hex if not given. `SCALE` is also optional, and defaults to 1.0; it allows the values in the column to be scaled before loading into the data import module. The final value loaded is the value in the column, multiplied by the scale factor, rounded to the nearest integer (except for time values, which are rounded to the nearest 10^{-24} sec). All values are checked for overflow with respect to the field's `WIDTH_BITS`. Line numbers and sample numbers are treated as 32-bit quantities.

`<ALBformat>:`

- INTEGER
- UNSIGNED_INTEGER
- FLOAT [SCALE = <nnn.nnn>]

The same as <CSVformat>, except there is no numeric base. Floating point values must be in IEEE Standard 754, and so must be either four bytes or eight bytes wide.

<timeUnit>:

- EXPONENT = <nnn>
- EXPONENT = -<nnn>

The unit to apply to time tag values (in addition to the scale factor, if used with floating point values). For example, EXPONENT = -12 is equivalent to picosecond time ticks.

Header Example

```
AGILENT_CSV_DATA
#
# ---------------------------- #
#  Created: 2008 Sep 21 21:18  #
#  By: Agilent Logic Analyzer  #
# ---------------------------- #
#
HEADER BEGIN
TIME COLUMN="tSample"
TRIGGER_ROW=100
TRIGGER_CORRELATION_OFFSET=1.24e-9
COLUMN "Sample" SAMPLE_NUMBER INTEGER DECIMAL
COLUMN "Address" VALUE INTEGER HEX WIDTH_BITS=24
COLUMN "Data" VALUE INTEGER HEX WIDTH_BITS=16
COLUMN "Status" VALUE INTEGER BIN WIDTH_BITS=8
COLUMN "DigRF" VALUE FLOAT SCALE=16.0e+3 WIDTH_BITS=16
COLUMN "tSample" TIME INTEGER DECIMAL EXPONENT=-12 RELATIVE
VALUE_SEPARATOR ","
VALUE_FILL_IN PREVIOUS
HEADER END
# Start data
0afc38,ff98,01000110,0.114,5000
0afc3c,055a,,,2500
# embedded comment
0afc38,ff98,01010001,0.116,2500
```

Module CSV Format File Characteristics

The file must define a time line so that each sample can be associated with a time tag. To do this, a periodic rate, or a time column with absolute or relative time tags, is required (see the TIME_SOURCE property in the file header). Time tags in the file are verified to be monotonically increasing. The specification of a periodic rate overrides the presence of time tag columns, if any.

The file must have one or more data value columns. Data value columns have the data to load. Other columns, such as line numbers, sample numbers, and time tags, annotate that data, but are not loaded as data.

Data rows in the file are indexed beginning with row 0 first, then 1, and so on. Row numbers are file-centric. They are not the same as the sample numbers in the module's listing. Sample numbers are always relative to the location of the trigger row, not the first row in the file.

The file header has a property, `TRIGGER_ROW`, giving the row number, in the file, associated with logic analyzer trigger. The trigger row is defined as the time origin, and contains T=0.

In a multi-module logic analyzer, only one module's trigger is at T=0. All the others are offset by hardware delays associated with the propagation of the trigger signal from the originating module to the receiving modules. The time delay is indicated by the `TRIGGER_CORRELATION_OFFSET` property. This is the amount of time that must be added to the time of each sample in the file to correctly position each sample on a time line with samples from another module in the system. By including this property, a file containing data exported from a module can be imported into the same system and will be positioned (correlated) correctly with data from the other modules.

An interesting case arises if the trigger sample is not included in the export range. This can legitimately occur if the time source is periodic. In this case, the `TRIGGER_ROW` value will indicate a row not in the file. For example, if the first data row in the file is the first sample after the trigger in the module, then `TRIGGER_ROW=-1`. Conversely, if the trigger was the first sample after the last row in the exported data, `TRIGGER_ROW` is equal to the number of rows in the file. If the trigger was two samples after the last row, `TRIGGER_ROW` is the number of rows in the file plus one, and so on. With these adjustments, the export file can now be imported and positioned correctly relative to the original master trigger without misrepresenting the location of the trigger sample (which was not in the file). Sample numbers are handled in a similar manner, with sample 0 on the trigger row. If the trigger row is not in the file, sample 0 is not in the file either.

These statements about the contents of a module CSV file will always be true:

- The first data row in the file is row 0. The next is 1, then 2, and so on.
- The `TRIGGER_ROW` is always relative to the first row in the file (row 0). The trigger row may or may not be in the file.
- The time associated with the `TRIGGER_ROW` is always 0. The `TRIGGER_CORRELATION_OFFSET` property allows correct correlation to other data sets.

- The sample number on the TRIGGER_ROW (if a sample number column is present) is always 0. Sample numbers increase by one for each row after the trigger row; they decrease by one for each row before the trigger. Sample numbers are not the same as row numbers.
- Line numbers, if exported to the file, always begin at 0 on row 0, then increase by one for each row thereafter: lineNumber = rowNumber.

Inconsistencies between a T=0 time tag, sample numbers and the TRIGGER_ROW property are resolved in this order:

1. The data row containing an absolute time tag of 0 is the trigger row and sample numbers are re-aligned if necessary to begin at zero on that row.
2. If the time line is defined by a period or frequency, and a sample number column is given, then the data row with sample number 0 is the trigger row. (This may or may not be within the span of the file itself).
3. Finally, the TRIGGER_ROW property is used. If time tags (relative or absolute) are used, the trigger row will be moved if it is not within the file.

See Also

- Module CSV and Module Binary File Header Format (see page 534)

Module Binary (ALB) Format

You can export captured data to module binary files or import module binary files into the logic analysis system using a *data import module*.

Module binary format files contain a header section (see page 534) followed by binary data. For example:

```
AGILENT_BINARY_DATA
HEADER_BEGIN
#
# --------------------------------------------------
#  Created: Dec 5, 2005 16:14:36
#  By: Agilent Logic Analyzer
# --------------------------------------------------
#
BYTE_ORDER=LITTLE_ENDIAN
TRIGGER_CORRELATION_OFFSET=0.000000000000000e+000
TRIGGER_ROW=524288
NUM_ROWS=1048576
TIME_SOURCE PERIOD=2.000000000000000e-009
COLUMN "Sample Number" SAMPLE_NUMBER NBYTES=4 INTEGER
COLUMN "My Bus 1" VALUE NBYTES=1 UNSIGNED_INTEGER WIDTH_BITS=8
COLUMN "My Bus 2" VALUE NBYTES=2 UNSIGNED_INTEGER WIDTH_BITS=16
COLUMN "My Bus 3" VALUE NBYTES=4 UNSIGNED_INTEGER WIDTH_BITS=32
COLUMN "My Signal 1" VALUE NBYTES=1 UNSIGNED_INTEGER WIDTH_BITS=1
COLUMN "My Signal 2" VALUE NBYTES=1 UNSIGNED_INTEGER WIDTH_BITS=1
COLUMN "Time" TIME NBYTES=8 FLOAT EXPONENT=-12 ABSOLUTE
```

```
HEADER_END
<binary data>
```

The binary data section of the file contains only binary data. Binary data is organized by rows, where there are a fixed number of columns within a row (the number of COLUMN definitions in the header) and a fixed number of bytes per column (1, 2, 4, 8, or 16 as specified by NBYTES in the COLUMN definition). This simplifies reading the data, because these sizes match the native C language sizes of `char`, `short`, `long`, and `long long` (__int64). Values of 16 bytes contain 128 bits which is the widest bus supported in the logic analysis system. By restricting exported sizes to these values, an ALB file with no header and only one bus/signal becomes a simple dump of an array of integers.

See Also

- Module CSV and Module Binary File Header Format (see page 534)

Object File Formats Supported by the Symbol Reader

The logic analysis system can read symbol files in the following formats:

- OMF96
- OMFx86
- IEEE-695
- ELF/DWARF
- ELF/stabs
- TI COFF

For ELF/DWARF1, ELF/stabs, and ELF/stabs/Mdebug files, C++ symbols are demangled so that they can be displayed in the original C++ notation. To improve performance for these ELF symbol files, type information is not associated with variables. Hence, some variables (typically a few local static variables) may not have the proper size associated with them. They may show a size of 1 byte and not the correct size of 4 bytes or even more. All other information function ranges, line numbers, global variables and filenames will be accurate. These behaviors may be changed by editing the readers.ini (see page 120) file.

See Also

- To load symbols from a file (see page 118)
- To change symbol reader options (see page 120)
- To create an ASCII symbol file (see page 120)

General-Purpose ASCII (GPA) Symbol File Format

General-purpose ASCII (GPA) format files are loaded into a logic analyzer just like other object files.

If your compiler does not produce object files in a supported format, or if you want to define symbols that are not included in the object file, you can create an ASCII format symbol file.

Typically, ASCII format symbol files are created using text processing tools that convert the symbol table information from a compiler or linker map output file.

Different types of symbols are defined in different records in the GPA file. Record headers are enclosed in square brackets, for example, [USER]. For a summary of GPA file records and associated symbol definition syntax, refer to the General-Purpose ASCII (GPA) Record Format Summary (see page 546).

Each entry in the symbol file must consist of a symbol name followed by an address or address range.

The address or address range must be a hexadecimal number. It must appear on the same line as the symbol name, and it must be separated from the symbol name by one or more blank spaces or tabs. Address ranges must be in the following format:

```
beginning address..ending address
```

The following example defines two symbols that correspond to address ranges and one symbol that corresponds to a single address.

```
main     00001000..00001009
test     00001010..0000101F
var1     00001E22     #this is a variable
```

For more detailed descriptions of GPA file records and associated symbol definition syntax, refer to the following topics:

- SECTIONS (see page 547)
- FUNCTIONS (see page 548)
- USER (see page 548)
- VARIABLES (see page 549)
- SOURCE LINES (see page 550)
- START ADDRESS (see page 550)
- Comments (see page 550)

General-Purpose ASCII (GPA) Record Format Summary

Format

```
[SECTIONS (see page 547)]
section_name  start..end  attribute

[FUNCTIONS (see page 548)]
func_name  start..end

[USER (see page 548)]
sym_name   value                   base
sym_name   start_value   [size]    base
sym_name   start_value..end_value  base

[VARIABLES (see page 549)]
var_name   start [size]
var_name   start..end

[SOURCE LINES (see page 550)]
File: file_name
line#  address

[START ADDRESS (see page 550)]
address

#comment text (see page 550)
```

Lines without a preceding header are assumed to be symbol definitions in one of the [USER] formats.

Example This is an example GPA file that contains several different kinds of records.

```
[SECTIONS]
prog      00001000..0000101F
data      40002000..40009FFF
common    FFFF0000..FFFF1000

[FUNCTIONS]
main      00001000..00001009
test      00001010..0000101F

[USER]
bdontcare    00x1     binary
hvalue       00EF     hex
drange       0..99    decimal
srange      -23  20   signed decimal   # The 20 is a decimal value for s
ize.

[VARIABLES]
total     40002000  4
value     40008000  4

[SOURCE LINES]
File: main.c
10        00001000
11        00001002
```

```
14       0000100A
22       0000101E

File: test.c
 5       00001010
 7       00001012
11       0000101A
```

SECTIONS

Use SECTIONS to define symbols for regions of memory, such as sections, segments, or classes.

NOTE To enable section relocation, section definitions must appear before any other definitions in the file.

NOTE If you use section definitions in a GPA symbol file, any subsequent function or variable definitions must be within the address ranges of one of the defined sections. Functions and variables that are not within the range are ignored.

Format

```
[SECTIONS]
section_name  start..end  attribute
```

section_name	A symbol representing the name of the section.
start	The first address of the section, in hexadecimal.
end	The last address of the section, in hexadecimal.
attribute	(optional) Attribute may be one of the following: • NORMAL (default) - The section is a normal, relocatable section, such as code or data. • NONRELOC - The section contains variables or code that cannot be relocated. In other words, this is an absolute segment. • AddReloc reloc_offset - Lets you specify an offset value (up to 32-bit) for a relocated section. • SetReloc reloc_value - Lets you specify a new base value (up to 32-bit) for a relocated section.

Example

```
[SECTIONS]
prog          00001000..00001FFF
data          00002000..00003FFF
display_io    00008000..0000801F   NONRELOC
sect3         00003000..00003FFF   AddReloc    1000
sect4         00005000..00005FFF   SetReloc    0000F000
```

FUNCTIONS

Use FUNCTIONS to define symbols for program functions, procedures or subroutines.

Format

```
[FUNCTIONS]
func_name  start..end
```

func_name	A symbol representing the function name.
start	The first address of the function, in hexadecimal.
end	The last address of the function, in hexadecimal.

Example

```
[FUNCTIONS]
main     00001000..00001009
test     00001010..0000101F
```

USER

Under the [USER] record header, you can create symbols with don't care values, and you can use value number bases other than hex.

USER is the default record type; this means symbols defined without any record header ([USER], [VARIABLE], etc.) are assumed to be USER symbols.

USER symbol definitions can have 128-bit values; symbol definitions in all other record types are limited to 32-bit values.

Format

```
[USER]
sym_name   value                       base
sym_name   start_value    [size]       base
sym_name   start_value..end_value      base

* use quotes(") around names or values with spaces.
```

sym_name	A symbol name.
value	The value of the symbol.
base	The number base of the value(s); can be: • binary • octal • hex (or hexadecimal or blank) • decimal • signed decimal
start_value	The low value of the range.

end_value	The high value of the range.
size	The size of the range of values, in decimal.

Example

```
[USER]
bdontcare     00x1           binary
bvalue        0011           binary
brange        0000..0011     binary
brange2       0011    9      binary   # The 9 is a decimal value for size
.
odontcare     00x7           octal
ovalue        0077           octal
orange        0000..0077     octal
orange2       0000    99     octal    # The 99 is a decimal value for siz
e.
hdontcare     00xF           hex
hvalue        00EF           hex
hrange        0000..00FF     hex
hrange3       0000     99    hex      # The 99 is a decimal value for siz
e.
dvalue        1090           decimal
drange        0..99          decimal
drange2       0    100       decimal    # The 100 is a decimal value for
size.
svalue       -23             signed decimal
srange       -23..-5         signed decimal
srange       -23   20        signed decimal   # The 20 is a decimal value
for size.
"hvalue with space"  "01XX FFFF" hex
"hrange with space"  "0100 FFFF".."0400 FFFF" hex  # Applies to other bas
es also.
```

VARIABLES

You can specify symbols for variables using:

- The address of the variable.
- The address and the size of the variable.
- The range of addresses occupied by the variable.

If you specify only the address of a variable, the size is assumed to be 1 byte.

Format

```
[VARIABLES]
var_name   start [size]
var_name   start..end
```

var_name	A symbol representing the variable name.
start	The first address of the variable, in hexadecimal.

end	The last address of the variable, in hexadecimal.
size	(optional) The size of the variable, in bytes, in decimal.

Example

```
[VARIABLES]
subtotal     40002000    4
total        40002004    4
data_array   40003000..4000302F
status_char  40002345
```

SOURCE LINES

Use SOURCE LINES to associate addresses with lines in your source files.

Format

```
[SOURCE LINES]
File: file_name
line#   address
```

file_name	The name of a file.
line#	The number of a line in the file, in decimal.
address	The address of the source line, in hexadecimal.

Example

```
[SOURCE LINES]
File: main.c
10        00001000
11        00001002
14        0000100A
22        0000101E
```

See Also

- Viewing Source Code Associated with Captured Data (see page 272)

START ADDRESS

Format

```
[START ADDRESS]
address
```

address	The address of the program entry point, in hexadecimal.

Example

```
[START ADDRESS]
00001000
```

Comments

Use the # character to include comments in a file. Any text following the # character is ignored. You can put comments on a line alone or on the same line following a symbol entry.

Format `#comment text`

Example `#This is a comment`

Product Overviews

- 1680/1690-Series Logic Analyzer Product Overview (see page 552)
- 16800-Series Logic Analyzer Product Overview (see page 558)
- 16900-Series Logic Analysis System Product Overview (see page 561)
- *Agilent Logic Analyzer* Application Product Overview (see page 569)

See Also

- Tutorial - Getting to know your logic analyzer (see page 38)

1680/1690-Series Logic Analyzer Product Overview

The Agilent Technologies 1680/1690-series logic analyzers provide a variety of channel widths, memory depths, and state and timing acquisition speeds (see tables below).

- The 1680A/AD-series comes with a large integrated 12.1-inch color flat panel display which can show up to 22 waveforms on screen simultaneously.

- The 1690A/AD-series is a PC-hosted model which connects to a personal computer via an IEEE 1394 interface; this lets you carry out measurement and debug work in your own PC environment. (One 1690-series logic analyzer per PC is supported.)

Both model series have the familiar Windows-based user interface which takes the complexity out of making logic analyzer measurements. You can perform all operations directly from one window. See Intrinsic Support (see page 361).

- 1680-Series Front Panel Operation (see page 553)
- 1680-Series Display Brightness (see page 558)

Supplied Accessories

1680A/AD-series logic analyzers:

- PS/2 mouse.
- PS/2 mini keyboard.
- Front panel cover.
- Accessory pouch.

1690A/AD-series logic analyzers:

- IEEE 1394 PCI card and cable.
- Laptop IEEE 1394 cable.
- Accessory pouch.

Optional Accessories

- Rack Mount Kit - Option 1CM.
- Additional IEEE 1394 PCI card and cable.

See Also

- Tutorial - Getting to know your logic analyzer (see page 38)
- 1680/1690-Series Logic Analyzer Characteristics (see page 596)
- 1680/1690-Series Logic Analyzer Specifications (see page 595)

1680-Series Front Panel Operation

The front panel interface consists of knobs and buttons that you use to set up and run measurements. There are also shortcut buttons that quickly access commonly used dialogs in the interface. When a front panel action is not valid, an audible "beep" will sound.

NOTE When multiple instances of the *Agilent Logic Analyzer* application are running on the logic analyzer, the front panel knobs and buttons only work for the application that is connected to the *local* acquisition hardware.

All functions available with the front panel knobs and buttons can also be performed in the graphical user interface (GUI).

- Run/Stop Buttons (see page 554)
- Open/Save/Default Setup Buttons (see page 554)
- General Purpose Knob (see page 555)
- Alphanumeric Keypad (see page 555)
- Shortcut Buttons (see page 555)
- Vertical Knobs (see page 556)
- Horizontal Knobs (see page 557)
- Marker Knob/Button (see page 557)

Run/Stop Buttons

Item	Description
Run Single	Runs a single acquisition (see page 168). The Run Single button turns green indicating when a Run action is valid. While the analyzer is running, the light goes out.
Run Rep. (Repetitive)	Runs a repetitive acquisition (see page 168). The Run Repetitive button turns green indicating when a Run Repetitive action is valid. While the analyzer is running, the light goes out.
Stop	Stops (see page 168) the current acquisition. The Stop button turns red during a Run cycle indicating when the Stop action is valid.

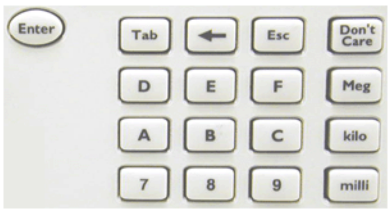
Open/save/Default Setup Buttons

Item	Description
Open Setup	Accesses the Open Configuration (see page 184) dialog.
Save Setup	Accesses the Save Configuration (see page 171) dialog.
Default Setup	Resets setup to the default power up configuration.

General Purpose Knob

The general purpose knob acts on the field that has the current focus. Fields that have the current focus have the blue background. The general purpose knob is typically used to increase/decrease numeric values such as waveform scale and delay.

Alphanumeric Keypad



In OK/Cancel dialogs, the escape key acts as a cancel operation and exits the dialog.

Item	Description
Enter	Accepts value or configuration change and exits dialog.
Tab	Scrolls configuration fields left-to-right and top-to-bottom.
Backspace (left arrow)	Backspaces cursor in an alphanumeric assignment field.
Esc	
Keypad	Used for alphanumeric entry.
Units	Sets unit of measure.

Shortcut Buttons

Item	Description
Setup	Accesses the Buses/Signals (see page 448) tab in the Analyzer Setup dialog.
Waveform	Accesses Waveform display (see page 427) window. When the Waveform display is active, the button turns green.
Listing	Accesses Listing display (see page 433) window. When the Listing display is active, the button turns green.
Find	Accesses advanced search (see page 257) dialog.
Trigger	Accesses advanced trigger (see page 445) dialog.
File Mgr	Accesses the Explore file manager dialog.
Print	Accesses the Printing Data dialog (see page 473).
Help	Accesses the online help system's main window. Same as F1 key.

Vertical Knobs

Item	Description
Size	Adjusts height of all waveform rows. The selection lights up green indicating it's part of the waveform group, and that the waveform group is currently active.
Page	Scrolls a page at a time of Listing data. The selection lights up green indicating it's part of the listing group, and that the listing group is currently active.
Scroll	Scrolls row at a time of Waveform data. The selection lights up green indicating it's part of the waveform group, and that the waveform group is currently active.
Line	Scrolls a line at a time of Listing data. The selection lights up green indicating it's part of the listing group, and that the listing group is currently active.

Horizontal Knobs

Item	Description
Time/Div	Changes time/division (see page 204) scale of Waveform display. The selection lights up green indicating it's part of the waveform group, and that the waveform group is currently active.
Bus/Sig	Scrolls first column to last column in Listing Display. The selection lights up green indicating it's part of the listing group, and that the listing group is currently active.
Delay	Changes delay (see page 206) of Waveform display. The selection lights up green indicating it's part of the waveform group, and that the waveform group is currently active.
Column	Scrolls a column at a time of Listing data. The selection lights up green indicating it's part of the listing group, and that the listing group is currently active.

Marker/Knob Button

Item	Description
Move marker knob	Moves selected marker in the display.
Choose marker button	Selects marker for "Move" operation. Press button to scroll through available markers. If no markers are defined, pressing Choose will create an M1 marker.

For more marker information, refer to Marking, and Measuring Between, Data Points (see page 234).

1680-Series Display Brightness

Included with the 1680-series logic analyzers is a *display brightness control*.

You can double-click the  icon in the Windows taskbar to toggle between high and low brightness settings.

16800-Series Logic Analyzer Product Overview

The Agilent Technologies 16800-series logic analyzers are standalone benchtop logic analyzers that range from 34 to 204 logic acquisition channels and 48 pattern generator channels, depending on the model.

Model Comparison

Agilent model number:	16801A	16802A	16803A	16804A	16806A	16821A	16822A	16823A
Logic acquisition channels:	34	68	102	136	204	34	68	102
Pattern generator channels:	0	0	0	0	0	48	48	48

Features, Logic Acquisition

- 1 M to 32 M memory depth per channel (depending on memory option), software upgradeable.
- 250 MHz or 500 Mb/s maximum state data rate (depending on state speed option), software upgradeable. The 500 Mb/s maximum state data rate option is available on the 68-, 120-, 136-, and 204-channel logic analyzer models.
- 1 GHz, 64 M deep timing analysis on half channels.
- Automated threshold and sample position setup.
- 4 GHz timing zoom with 64 K memory depth.

Features, Mainframe

- Built-in 15 inch TFT color LCD display, 1,024 x 768 (XGA) resolution. Touch screen with Option 103. See Tips for Using the Touch Screen (see page 562).
- Front panel knob and buttons. See 16800 Series Front Panel Operation (see page 560).
- 80 GB hard disk drive (or external hard drive Option 109).

- 10/100 Base-T LAN port.
- USB 2.0 ports (six total, two on front, four on back).
- One PCI expansion slot.
- One PCI Express x1 expansion slot.
- Windows® XP Professional operating system.
- *Agilent Logic Analyzer* application which takes the complexity out of making logic analyzer measurements. You can perform all operations directly from one window. See Intrinsic Support (see page 361).

CAUTION When powering off the 16800-series logic analyzer, wait until the fans stop turning (about 15 seconds) before turning the logic analyzer back on. This ensures that internal circuitry restarts in a known state. (For more information on powering off the logic analyzer, see the "*16800-Series Logic Analyzer Installation/Quick Start Guide*".)

Features, Pattern Generator

- 24 channels at 300 MHz clock; 48 channels at 180 MHz clock.
- Memory Depth: 16,777,216 vectors.
- Logic Level (data pods): TTL, 3-state TTL/3.3v, 3-state TTL/CMOS, ECL/PECL/LVPECL terminated, ECL unterminated, and differential ECL (without pod).
- Data Inputs: 3-bit pattern level sensing (clock pod).
- Clock Output: Synchronized to output data, delay of 7 ns in 14 steps (clock pod).
- Clock Input: DC to 300 MHz (clock pod).
- Internal Clock Period: Programmable from 1 MHz to 300 MHz in 1 MHz steps.
- External Clock Period: DC to 300 MHz.
- External Clock Duty Cycle: 1.3 ns minimum high time.

Supplied Accessories

- PS/2 mouse.
- PS/2 mini keyboard.
- Accessory pouch.
- Power cord.

Optional Accessories

- Probes.

See Also

- Tutorial - Getting to know your logic analyzer (see page 38)
- 16800-Series Logic Analyzer Specifications and Characteristics (see page 621)

16800-Series Front Panel Operation

The front panel interface consists of a knob and buttons that you use to set up and run measurements. There are also shortcut buttons that quickly access commonly used dialogs in the interface. When a front panel action is not valid, an audible "beep" will sound.

NOTE When multiple instances of the *Agilent Logic Analyzer* application are running on the logic analyzer, the front panel knobs and buttons only work for the application that is connected to the *local* acquisition hardware.

All functions available with the front panel knobs and buttons can also be performed in the graphical user interface (GUI).

- Run/Stop Buttons (see page 560)
- General Purpose Knob (see page 560)
- Touch Off Button (see page 561)

Run/Stop Buttons

Item	Description
Run Single	Runs a single acquisition (see page 168). The Run Single button turns green indicating when a Run action is valid. While the analyzer is running, the light goes out.
Run Rep. (Repetitive)	Runs a repetitive acquisition (see page 168). The Run Repetitive button turns green indicating when a Run Repetitive action is valid. While the analyzer is running, the light goes out.
Stop	Stops (see page 168) the current acquisition. The Stop button turns red during a Run cycle indicating when the Stop action is valid.

General Purpose Knob

The general purpose knob acts on the field that has the current focus. Fields that have the current focus have the blue background. The general purpose knob is typically used to increase/decrease numeric values such as waveform scale and delay.

Touch Off Button

Item	Description
Touch Off	Turns off the touch screen so that accidental touches don't affect the instrument.

See Also

- Tips for Using the Touch Screen (see page 562)

16900-Series Logic Analysis System Product Overview

The Agilent Technologies 16900-series logic analysis systems are modular systems with slots for logic analyzer and other types of measurement instrument cards.

	16900A	16901A	16902A	16903A
Number of instrument card slots:	6	2	6	3
Multiframe connectors:	Yes	Yes	Yes	No
Display and resolution:	Uses external monitor. Supports up to four external monitors at up to 1600 x 1200 (with PCI video card)	Built-in color touch screen display, 15 inch at 1024 x 768, supports external monitor (without additional PCI video card)	Built-in color touch screen display, 12.1 inch at 800 x 600, supports up to four external monitors at up to 1600 x 1200 (with PCI video card)	Built-in color touch screen display, 12.1 inch at 800 x 600, supports up to four external monitors at up to 1600 x 1200 (with PCI video card)
Front panel knobs and buttons:	No	Yes	Yes	Yes
PCI expansion slots:	2 full profile, 1 low profile	1 full profile, 1 PCI Express x1	2 full profile, 1 low profile	1 full profile, 1 low profile

All models have the familiar Windows-based user interface which takes the complexity out of making logic analyzer measurements. You can perform all operations directly from one window. See Intrinsic Support (see page 361).

- Tips for Using the Touch Screen (see page 562)

- 16901 Front Panel Operation (see page 564)
- 16902/903 Front Panel Operation (see page 565)

CAUTION When powering off the 16900-series logic analysis system, wait until the fans stop turning (about 15 seconds) before turning the logic analysis system back on. This ensures that internal circuitry restarts in a known state. (For more information on powering off the logic analysis system, see the "*16900-Series Logic Analysis System Installation Guide*".)

Supplied Accessories

- PS/2 mouse.
- PS/2 mini keyboard.
- Accessory pouch.
- Power cord.
- Ten-conductor flying-lead cable for the *target control port* (see page 61) (on 16900A, 16902A, and 16903A models).

Optional Accessories

- Multiframe cable (E5861A).
- 1 Gbit low-profile LAN card (option 014 or E5860A for 16900A, 16902A, and 16903A models).
- Probes.

See Also

- Tutorial - Getting to know your logic analyzer (see page 38)
- 16900-Series Logic Analysis System Frame Characteristics (see page 643)

Tips for Using the Touch Screen

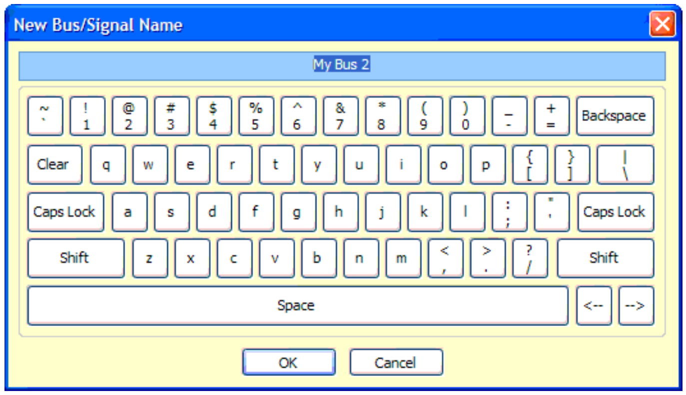
The 16901A, 16902A, and 16903A logic analysis system frames and 16800-series logic analyzer frames with Option 103 have a touch screen. Here are some tips for using the touch screen:

- Use firm, even pressure on the touch screen.
- You may prefer to use a stylus.
- Use the front panel marker knobs to place markers. Placing markers is hard to do accurately using the touch screen. (Any marker can be selected using the Marker **Choose** button.)
- For trees, the touchable area around the +/- buttons is expanded.
- For option selections, both the option and the caption are active.

To open a keyboard dialog

Inside the *Agilent Logic Analyzer* application:

- Press the keyboard button in any edit field. This opens a dialog for entering field values.



Outside the *Agilent Logic Analyzer* application:

- Press the front panel **Keyboard** button. This opens the Microsoft On-Screen Keyboard and the touch screen Event Selector.

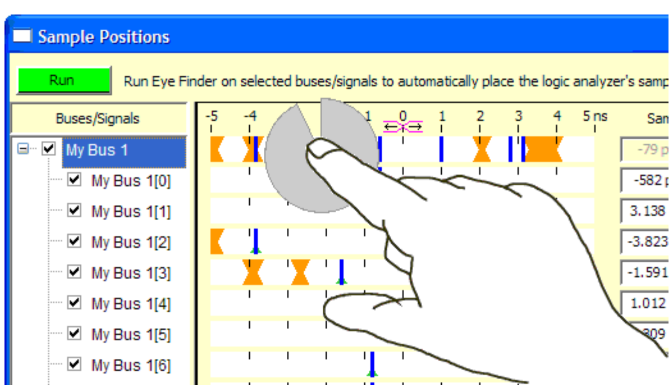
(You can also choose **Start>All Programs>Accessories>Accessibility>On-Screen Keyboard**.)

To access right mouse button behavior

Inside the *Agilent Logic Analyzer* application, most right mouse button behavior is accessible just by touching the screen.

Outside the *Agilent Logic Analyzer* application:

- Press down on the touch screen until a full circle is drawn around your finger; then, a right-click occurs.



- Or, you can choose **Start>All Programs>Agilent Logic Analyzer>Utilities>Touch Screen>Event Selector** to open the window:

Touching inside this window causes your next touch to act as a right-click.

To recalibrate the touch screen

- If the touch screen needs to be recalibrated, choose **Start>All Programs>Agilent Logic Analyzer>Utilities>Touch Screen>Calibrate**.

See Also

- 16800-Series Panel Operation (see page 560)
- 16901 Front Panel Operation (see page 564)
- 16902/903 Front Panel Operation (see page 565)

16901 Front Panel Operation

The front panel interface consists of a knob and buttons that you use to set up and run measurements. There are also shortcut buttons that quickly access commonly used dialogs in the interface. When a front panel action is not valid, an audible "beep" will sound.

NOTE

When multiple instances of the *Agilent Logic Analyzer* application are running on the logic analyzer, the front panel knobs and buttons only work for the application that is connected to the *local* acquisition hardware.

All functions available with the front panel knobs and buttons can also be performed in the graphical user interface (GUI).

- Run/Stop Buttons (see page 564)
- General Purpose Knob (see page 565)
- Touch Off Button (see page 565)

Run/Stop Buttons

Item	Description
Run Single	Runs a single acquisition (see page 168). The Run Single button turns green indicating when a Run action is valid. While the analyzer is running, the light goes out.

Run Rep. (Repetitive)	Runs a repetitive acquisition (see page 168). The Run Repetitive button turns green indicating when a Run Repetitive action is valid. While the analyzer is running, the light goes out.
Stop	Stops (see page 168) the current acquisition. The Stop button turns red during a Run cycle indicating when the Stop action is valid.

General Purpose Knob

The general purpose knob acts on the field that has the current focus. Fields that have the current focus have the blue background. The general purpose knob is typically used to increase/decrease numeric values such as waveform scale and delay.

Touch Off Button

Item	Description
Touch Off	Turns off the touch screen so that accidental touches don't affect the instrument.

See Also

- Tips for Using the Touch Screen (see page 562)

16902/903 Front Panel Operation

The front panel interface consists of a touch screen, knobs, and buttons that you use to set up and run measurements. There are also shortcut buttons that quickly access commonly used windows/dialogs in the interface. When a front panel action is not valid, an audible "beep" will sound.

NOTE When multiple instances of the *Agilent Logic Analyzer* application are running on the logic analyzer, the front panel knobs and buttons only work for the application that is connected to the *local* acquisition hardware. Likewise, in a multiframe configuration, the front panel knobs and buttons only work for the application running on the *master frame*.

All functions available with the front panel knobs and buttons can also be performed in the graphical user interface (GUI).

- Run/Stop Buttons (see page 566)

- Open/Save/New File Buttons (see page 566)
- General Purpose Knob and Enter Button (see page 566)
- Shortcut Buttons (see page 567)
- Vertical Knobs (see page 568)
- Horizontal Knobs (see page 568)
- Marker Knob/Button (see page 569)
- Touch Off Button (see page 569)

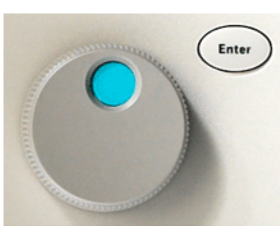
Run/Stop Buttons

Item	Description
Run Single	Runs a single acquisition (see page 168). The Run Single button turns green indicating when a Run action is valid. While the analyzer is running, the light goes out.
Run Rep. (Repetitive)	Runs a repetitive acquisition (see page 168). The Run Repetitive button turns green indicating when a Run Repetitive action is valid. While the analyzer is running, the light goes out.
Stop	Stops (see page 168) the current acquisition. The Stop button turns red during a Run cycle indicating when the Stop action is valid.

Open/Save/New File Buttons

Item	Description
Open File	Accesses the Open Configuration (see page 184) dialog.
Save File	Accesses the Save Configuration (see page 171) dialog.
New File	Resets setup to the default power up configuration.

General Purpose Knob and Enter Button

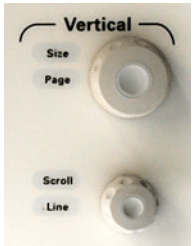


Item	Description
General purpose knob	The general purpose knob acts on the field that has the current focus. Fields that have the current focus have the blue background. The general purpose knob is typically used to increase/decrease numeric values such as waveform scale and delay.
Enter button	Accepts value or configuration change and exits dialog.

Shortcut Buttons

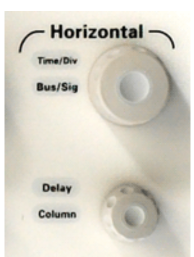
Item	Description
Waveform	Accesses Waveform display (see page 427) window. When the Waveform display is active, the button turns green.
Listing	Accesses Listing display (see page 433) window. When the Listing display is active, the button turns green.
Scope	Runs the "*Add External Oscilloscope* wizard" (in the online help) for connecting an external Infiniium oscilloscope to the logic analyzer using the E5850A time correlation fixture.
Mixed	Enables full screen display and tiles windows horizontally or disables the mixed window setup.
Full Screen	Enables or disables full screen display.
Setup	Accesses the Buses/Signals (see page 448) tab in the Analyzer Setup dialog.
Trigger	Accesses advanced trigger (see page 445) dialog.
Find	Accesses advanced search (see page 257) dialog.
Keyboard	Opens a keyboard dialog for entering information.
Help	Accesses the online help system's main window. Same as F1 key.

Vertical Knobs



Item	Description
Size	Adjusts height of all waveform rows. The selection lights up green indicating it's part of the waveform group, and that the waveform group is currently active.
Page	Scrolls a page at a time of Listing data. The selection lights up green indicating it's part of the listing group, and that the listing group is currently active.
Scroll	Scrolls row at a time of Waveform data. The selection lights up green indicating it's part of the waveform group, and that the waveform group is currently active.
Line	Scrolls a line at a time of Listing data. The selection lights up green indicating it's part of the listing group, and that the listing group is currently active.

Horizontal Knobs



Item	Description
Time/Div	Changes time/division (see page 204) scale of Waveform display. The selection lights up green indicating it's part of the waveform group, and that the waveform group is currently active.
Bus/Sig	Scrolls first column to last column in Listing Display. The selection lights up green indicating it's part of the listing group, and that the listing group is currently active.

Delay	Changes delay (see page 206) of Waveform display. The selection lights up green indicating it's part of the waveform group, and that the waveform group is currently active.
Column	Scrolls a column at a time of Listing data. The selection lights up green indicating it's part of the listing group, and that the listing group is currently active.

Marker Knob/Button

Item	Description
Move marker knob	Moves selected marker in the display.
Choose marker button	Selects marker for "Move" operation. Press button to scroll through available markers. If no markers are defined, pressing Choose will create an M1 marker.

For more marker information, refer to Marking, and Measuring Between, Data Points (see page 234).

Touch Off Button

Item	Description
Touch Off	Turns off the touch screen so that accidental touches don't affect the instrument.

See Also

- Tips for Using the Touch Screen (see page 562)

Agilent Logic Analyzer Application Product Overview

The *Agilent Logic Analyzer* application is a familiar Windows-based user interface which takes the complexity out of making logic analyzer measurements. You can perform all operations directly from one window. See Intrinsic Support (see page 361).

Agilent's Simple, Quick and Advanced Trigger functions take the complexity out of triggering. Use Simple Trigger's pull down menus to define events in terms of edges and patterns. With Quick Trigger you can see if a suspect event ever reoccurs by just drawing a box around the event in the display. Quick trigger will do the rest! Use Advanced Trigger's drag and drop graphical icons with sentence-like structures to customize complex trigger scenarios.

- Keyboard Commands (see page 570)

Keyboard Commands

- Access Menus (see page 570)
- File Operations (see page 570)
- Edit Operations (see page 571)
- Search Operations (see page 571)
- View operations (see page 571)
- Run/Stop Operations (see page 572)
- Compare Operations (see page 572)
- Listing Operations (see page 572)
- Waveform Operations (see page 572)
- Window Operations (see page 572)
- Help Operations (see page 572)
- Miscellaneous (see page 572)

Access Menus

Alt+F	Access to File menu
Alt+E	Access to Edit menu
Alt+V	Access to View menu
Alt+S	Access to Setup menu
Alt+T	Access to Tools menu
Alt+M	Access to Markers menu
Alt+R	Access to Run/Stop menu
Alt+W	Access to Window menu
Alt+H	Access to Help menu

File Operations

The following operations are located under **File** in the menu bar.

Ctrl+N	File - New
Ctrl+O	File - Open
Ctrl+F4	File - Close
Ctrl+S	File - Save
Ctrl+I	File - Import
Shift+E	File - Export
Ctrl+P	File - Print

Edit Operations

The following operations are located under **Edit** in the menu bar.

Ctrl+Z	Edit - Undo
Ctrl+X	Edit - Cut
Ctrl+C	Edit - Copy
Ctrl+V	Edit - Paste
Alt+I	Edit - Insert Bus/Signal into Window
Alt+P	Edit - Current Window Properties

Search Operations

The following operations are located under **Edit** in the menu bar.

Ctrl+F	Edit - Find
Shift+F3	Edit - Find Previous
F3	Edit - Find Next
Ctrl+B	Edit - Go To Beginning
Ctrl+T	Edit - Go To Trigger
Ctrl+E	Edit - Go To End
Ctrl+G	Edit - Go To

View Operations

The following operations are located under **View** in the menu bar.

Shift+F	View - Zoom Out Full
Shift+O	View - Zoom Out
Shift+I	View - Zoom In
F9	View - Full Screen

F11	View - Toggle Tabbed Windows
F12	View - Toggle Status Bar

Run/Stop Operations

The following operations are located under **Run/Stop** in the menu bar.

F5	Run/Stop - Run
Ctrl+F5	Run/Stop - Run Repetitive
F8	Run/Stop - Stop
Shift+F8	Run/Stop - Cancel
Shift+Ctrl+F8	Run/Stop - Resume

Compare Operations

The following operations are located under **Compare** in the menu bar.

Alt+P	Compare - Properties

Listing Operations

The following operations are located under **Listing** in the menu bar.

Alt+P	Listing - Properties

Waveform Operations

The following operations are located under **Waveform** in the menu bar.

Alt+P	Waveform - Properties

Window Operations

The following operations are located under **Window** in the menu bar.

F6	Window - Toggle to Next
Shift+F6	Window - Toggle to Previous

Help Operations

The following operations are located under **Help** in the menu bar.

F1	Help - Help Topics

Miscellaneous

The following operations are located throughout the interface.

Ctrl+esc	Shows Windows Start bar

Logic Analyzer Notes

- Channels and Memory Depth (see page 573)
- Timing Mode Sampling Options (see page 573)
- State Mode Sampling Options (see page 574)
- Timing Zoom (see page 574)

Channels and Memory Depth

- 1680/1690-Series Logic Analyzer Notes, Channels and Memory Depth (see page 575)
- 16740/41/42 Logic Analyzer Notes, Channels and Memory Depth (see page 576)
- 16750/51/52 Logic Analyzer Notes, Channels and Memory Depth (see page 578)
- 16753/54/55/56 Logic Analyzer Notes, Channels and Memory Depth (see page 580)
- 16760 Logic Analyzer Notes, Channels and Memory Depth (see page 582)
- 16800-Series Logic Analyzer Notes, Channels and Memory Depth (see page 588)
- 16910/11 Logic Analyzer Notes, Channels and Memory Depth (see page 591)
- 16950/51 Logic Analyzer Notes, Channels and Memory Depth (see page 593)

Timing Mode Sampling Options/Period

The timing mode sampling options let you choose between *Full Channel Timing Mode* (default), *Half Channel Timing Mode* (faster sampling), or *Transitional / Store Qualified Timing Mode* (greater measurement length). For notes on these modes in a particular logic analyzer, see:

- 1680/1690-Series Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 575)
- 16740/41/42 Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 576)
- 16750/51/52 Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 578)
- 16753/54/55/56 Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 580)
- 16760 Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 582)
- 16800-Series Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 589)

- 16910/11 Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 591)
- 16950/51 Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 593)

State Mode Sampling Options

The state mode sampling options let you choose between *General State Mode* (default) or *Turbo State Mode* (faster sampling). For notes on these modes in a particular logic analyzer, see:

- 1680/1690-Series Logic Analyzer Notes, State Mode (see page 575)
- 16740/41/42 Logic Analyzer Notes, State Mode (see page 577)
- 16750/51/52 Logic Analyzer Notes, State Mode Sampling Options (see page 579)
- 16753/54/55/56 Logic Analyzer Notes, State Mode Sampling Options (see page 581)
- 16760 Logic Analyzer Notes, State Mode Sampling Options (see page 583)
- 16800-Series Logic Analyzer Notes, State Mode Sampling Options (see page 590)
- 16910/11 Logic Analyzer Notes, State Mode Sampling Options (see page 592)
- 16950/51 Logic Analyzer Notes, State Mode Sampling Options (see page 594)

Timing Zoom

- 1680/1690-Series Logic Analyzers don't have the timing zoom feature.
- 16740/41/42 Logic Analyzer Notes, Timing Zoom (see page 577)
- 16750/51/52 Logic Analyzer Notes, Timing Zoom (see page 580)
- 16753/54/55/56 Logic Analyzer Notes, Timing Zoom (see page 581)
- 16760 Logic Analyzers don't have the timing zoom feature.
- 16800-Series Logic Analyzer Notes, Timing Zoom (see page 591)
- 16910/11 Logic Analyzer Notes, Timing Zoom (see page 593)
- 16950/51 Logic Analyzer Notes, Timing Zoom (see page 594)

1680/1690-Series Logic Analyzer Notes

- Channels and Memory Depth (see page 575)
- Timing Mode Sampling Options/Period (see page 575)
- State Mode (see page 575)

Channels and Memory Depth

	1680A 1690A	1680AD 1690AD	1681A 1691A	1681AD 1691AD	1682A 1692A	1682AD 1692AD	1683A 1693A	1683AD 1693AD
Memory depth	512 K	2 M	512 K	2 M	512 K	2 M	512 K	2 M
Channels	136	136	102	102	68	68	34	34

Timing Mode Sampling Options/Period

- **Full channel (see page 575), 400 MHz** = *Full Channel Timing Mode*

  With this sampling option, you can use the full memory depth (see page 575) of your logic analyzer card, with data being sampled and stored as often as every 2.5 ns. You can set the sample rate to go slower with the Sample Period control.

- **Half channel (see page 575), 800 MHz** = *Half Channel Timing Mode*

  With this sampling option, only one pod of each pod pair is available, and the memory depth (see page 575) is doubled. Channels assigned to unavailable pods are ignored. You can specify which pod to use by toggling the Pod field in Format.

  Data is sampled and stored every 1.25 ns; this rate cannot be changed.

- **Transitional / Store qualified, Full channel 400 MHz** = *Transitional / Store Qualified Timing Mode*

  At the 400 MHz sample rate (2.5 ns sampling period), one *pod pair* (34 channels) must be *reserved for time tag storage*. At slower sample rates, you can get full channels (see page 575) by using 1/2 (or less) of a module's acquisition memory depth (see page 575) (for more information, see Memory Depth and Channel Count Trade-offs (see page 374)).

  Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period ranges from 2.5 ns to 1 ms. See transitional timing (see page 376).

NOTE

When you select the timing sampling mode's 400 MHz option (800 MHz option), the trigger marker in captured data may be off by 1 sample (3 samples). This occurs because the logic analyzer hardware uses 2 pipelines (4 pipelines). When triggering on a pattern, the actual sample that causes the trigger may be 1 sample before (within 3 samples before) the trigger marker. When triggering on an edge, the actual sample that causes the trigger may be within +/-1 sample (+/-2 samples) of the trigger marker.

State Mode

- **200 Mb/s maximum clock rate** = *General State Mode*

In the state (synchronous sampling) mode, you can have full channels (see page 575) and half memory depth (see page 575), or you can get full memory depth by reserving one pod pair (34 channels) for time tag storage (for more information, see Memory Depth and Channel Count Trade-offs (see page 374)).

State sampling speed matches your device under test's clock rate, up to 200 MHz.

See Also

- 1680/1690-Series Logic Analyzer Specifications (see page 595)
- 1680/1690-Series Logic Analyzer Characteristics (see page 596)

16740/41/42 Logic Analyzer Notes

- Channels and Memory Depth (see page 576)
- Timing Mode Sampling Options/Period (see page 576)
- State Mode (see page 577)
- Timing Zoom (see page 577)

Channels and Memory Depth

	16740A	16741A	16742A
Memory depth	1 M	4 M	16 M
Channels	68 channels/card * number of cards in module		

Timing Mode Sampling Options/Period

- **Full channel (see page 576), 400 MHz** = *Full Channel Timing Mode*

  With this sampling option, you can use the full memory depth (see page 576) of your logic analyzer card, with data being sampled and stored as often as every 2.5 ns. You can set the sample rate to go slower with the Sample Period control.

NOTE

When the Sample Period is 2.5 ns, data is acquired at two times the trigger sequencer rate. This means that data must be present for at least two samples before the trigger sequencer can reliably detect it. The trigger sequencer could miss data present for less than two sample periods.

The trigger sequencer treats the data as a group of two samples for each sequencer clock. This means that the trigger point indication could be off by one sample.

Although the trigger sequencer cannot detect all data, the analyzer will correctly capture all data present for at least one sample period.

- **Half channel (see page 576), 800 MHz** = *Half Channel Timing Mode*

With this sampling option, only one pod of each pod pair is available, and the memory depth (see page 576) is doubled. Channels assigned to unavailable pods are ignored. You can specify which pod to use by toggling the Pod field in Format.

Data is sampled and stored every 1.25 ns; this rate cannot be changed.

NOTE When the Sample Period is 1.25 ns, data is acquired at four times the trigger sequencer rate. This, along with other half-channel mode characteristics, means that data must be present for at least five samples before the trigger sequencer can reliably detect it. The trigger sequencer cannot detect data present for less than two sample periods, and could miss data present for less than five sample periods.

The trigger sequencer treats the data as a group of four samples for each sequencer clock. This means that the trigger point indication could be off by up to three samples.

Although the trigger sequencer cannot detect all data, the analyzer will correctly capture all data present for at least one sample period.

- **Transitional / Store qualified, Full channel 400 MHz** = *Transitional / Store Qualified Timing Mode*

  At the 400 MHz sample rate (2.5 ns sampling period), one *pod pair* (34 channels) must be *reserved for time tag storage*. At slower sample rates, you can get full channels (see page 576) by using 1/2 (or less) of a module's acquisition memory depth (see page 576) (for more information, see Memory Depth and Channel Count Trade-offs (see page 374)).

  Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period ranges from 2.5 ns to 1 ms. See transitional timing (see page 376).

State Mode

- **200 Mb/s maximum clock rate** = *General State Mode*

  In the state (synchronous sampling) mode, you can have full channels (see page 576) and half memory depth (see page 576), or you can get full memory depth by reserving one pod pair (34 channels) for time tag storage (for more information, see Memory Depth and Channel Count Trade-offs (see page 374)).

  State sampling speed matches your device under test's clock rate, up to 200 MHz.

Timing Zoom Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer. It uses a 16K-sample, 2 GHz timing analyzer to sample data as closely as every 500 ps on all channels.

See Also

- 16740/41/42 Logic Analyzer Specifications (see page 598)
- 16740/41/42 Logic Analyzer Characteristics (see page 599)

16750/51/52 Logic Analyzer Notes

- Channels and Memory Depth (see page 578)
- Timing Mode Sampling Options/Period (see page 578)
- State Mode Sampling Options (see page 579)
- Timing Zoom (see page 580)

Channels and Memory Depth

	16750A/B	16751A/B	16752A/B
Memory depth	4 M	16 M	32 M
Channels	68 channels/card * number of cards in module		

Timing Mode Sampling Options/Period

- **Full channel (see page 578), 400 MHz** = *Full Channel Timing Mode*

  With this sampling option, you can use the full memory depth (see page 578) of your logic analyzer card, with data being sampled and stored as often as every 2.5 ns. You can set the sample rate to go slower with the Sample Period control.

NOTE

When the Sample Period is 2.5 ns, data is acquired at two times the trigger sequencer rate. This means that data must be present for at least two samples before the trigger sequencer can reliably detect it. The trigger sequencer could miss data present for less than two sample periods.

The trigger sequencer treats the data as a group of two samples for each sequencer clock. This means that the trigger point indication could be off by one sample.

Although the trigger sequencer cannot detect all data, the analyzer will correctly capture all data present for at least one sample period.

- **Half channel (see page 578), 800 MHz** = *Half Channel Timing Mode*

  With this sampling option, only one pod of each pod pair is available, and the memory depth (see page 578) is doubled. Channels assigned to unavailable pods are ignored. You can specify which pod to use by toggling the Pod field in Format.

  Data is sampled and stored every 1.25 ns; this rate cannot be changed.

NOTE

When the Sample Period is 1.25 ns, data is acquired at four times the trigger sequencer rate. This, along with other half-channel mode characteristics, means that data must be present for at least five samples before the trigger sequencer can reliably detect it. The trigger sequencer cannot detect data present for less than two sample periods, and could miss data present for less than five sample periods.

The trigger sequencer treats the data as a group of four samples for each sequencer clock. This means that the trigger point indication could be off by up to three samples.

Although the trigger sequencer cannot detect all data, the analyzer will correctly capture all data present for at least one sample period.

- **Transitional / Store qualified, Full channel 400 MHz** = *Transitional / Store Qualified Timing Mode*

  At the 400 MHz sample rate (2.5 ns sampling period), one *pod pair* (34 channels) must be *reserved for time tag storage*. At slower sample rates, you can get full channels (see page 578) by using 1/2 (or less) of a module's acquisition memory depth (see page 578) (for more information, see Memory Depth and Channel Count Trade-offs (see page 374)).

  Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period ranges from 2.5 ns to 1 ms. See transitional timing (see page 376).

State Mode Sampling Options

- **200 MHz** = *General State Mode*

  With this sampling option, you can have full channels (see page 578) and half memory depth (see page 578), or you can get full memory depth by reserving one pod pair (34 channels) for time tag storage (for more information, see Memory Depth and Channel Count Trade-offs (see page 374)).

  State sampling speed matches your device under test's clock rate, up to 200 MHz.

- **400 MHz** = *Turbo State Mode*

  With this sampling option, one pod pair (34 channels) is reserved for time tag storage, and you have full memory depth (see page 578). Clocking is restricted to the J clock on Pod 1 of the *master card* of the *module*, and triggering is restricted to two trigger functions.

  State sampling speed matches your device under test's clock rate, up to 400 MHz.

NOTE

When Store Qualification is performed in the 400 MHz State mode, there may be the case where data occupying memory is further disqualified. As a result, you may see a non-contiguous listing of states as well as a reduction of usable memory.

Timing Zoom Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer. It uses a 16K-sample, 2 GHz timing analyzer to sample data as closely as every 500 ps on all channels.

NOTE

When in the Turbo State Mode, the start of timing zoom data may occur after the actual trigger point. The reason for this data mis-alignment is due to how the trigger sequencer functions when in this mode.

The analyzer sequencer works on *pairs* of samples. It will not evaluate the first sample of the pair until the second sample has entered the sequencer. If, for example, the trigger point is determined to be on the first sample, the analyzer displays the timing zoom data relative to the evaluation of the second sample. Whatever time difference is seen between the two samples (of the pair) is reflected in the data display between the trigger point and the start of the timing zoom data.

This time difference can be noticeable if your measurement is using bursted clocks and the first sample (actual trigger point) is clocked on the last clock signal of a burst, and the second sample (of the pair) is clocked with the first clock of the next burst. The time difference between the clock bursts is reflected as a mis-alignment between the trigger point and the start of the timing zoom data.

The best thing to do to help mitigate this situation is to set the timing zoom to "0% poststore" to capture as much data near the first sample as possible.

See Also

- 16750/51/52 Logic Analyzer Specifications (see page 603)
- 16750/51/52 Logic Analyzer Characteristics (see page 603)

16753/54/55/56 Logic Analyzer Notes

- Channels and Memory Depth (see page 580)
- Timing Mode Sampling Options/Period (see page 580)
- State Mode Sampling Options (see page 581)
- Timing Zoom (see page 581)

Channels and Memory Depth

	16753A	16754A	16755A	16756A
Memory depth	1 M	4 M	16 M	64 M
Channels	68 channels/card * number of cards in module			

Timing Mode Sampling Options/Period

- **Full channel (see page 580), 600 MHz** = *Full Channel Timing Mode*

  With this sampling option, you can use the full memory depth (see page 580) of your logic analyzer card, with data being sampled and stored as often as every 1.67 ns. You can set the sample rate to go slower with the Sample Period control.

- **Half channel (see page 580), 1.2 GHz** = *Half Channel Timing Mode*

  With this sampling option, only one pod of each pod pair is available, and the memory depth (see page 580) is doubled. Channels assigned to unavailable pods are ignored. You can specify which pod to use by toggling the Pod field in Format.

  Data is sampled and stored every 833 ps; this rate cannot be changed.

- **Transitional / Store qualified, Full channel 600 MHz** = *Transitional / Store Qualified Timing Mode*

  At the 600 MHz sample rate (1.667 ns sampling period), one *pod pair* (34 channels) must be *reserved for time tag storage*. At slower sample rates, you can get full channels (see page 580) by using 1/2 (or less) of a module's acquisition memory depth (see page 580) (for more information, see Memory Depth and Channel Count Trade-offs (see page 374)).

  Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period ranges from 1.667 ns to 500 us. See transitional timing (see page 376).

State Mode Sampling Options

- **300 MHz** = *General State Mode*

  With this sampling option, you can have full channels (see page 580) and half memory depth (see page 580), or you can get full memory depth by reserving one pod pair (34 channels) for time tag storage (for more information, see Memory Depth and Channel Count Trade-offs (see page 374)).

  State sampling speed matches your device under test's clock rate, up to 300 MHz.

- **600 MHz** = *Turbo State Mode*

  With this sampling option, one pod pair (34 channels) is reserved for time tag storage, and you have full memory depth (see page 580). Clocking is restricted to the J clock on Pod 1 of the *master card* of the *module*, and triggering is restricted to two trigger functions.

  State sampling speed matches your device under test's clock rate, up to 600 MHz.

Timing Zoom

Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer. It uses a 64K-sample, 4 GHz timing analyzer to sample data every 250 ps on all channels.

See Also

- Eye Scan in Logic Analyzers that Support Differential Signals (see page 382)
- 16753/54/55/56 Logic Analyzer Specifications and Characteristics (see page 607)

16760 Logic Analyzer Notes

- Differences from Other Logic Analyzers (see page 582)
- Channels and Memory Depth (see page 582)
- Timing Mode Sampling Options/Period (see page 582)
- State Mode Sampling Options (see page 583)

Differences from Other Logic Analyzers

Compared to most other logic analyzers supported in the 16900-series logic analysis system, the 16760 logic analyzer differs in the following ways:

- There are three additional state mode sampling options beyond the normal *General State Mode* and *Turbo State Mode* options.
- In state mode, the clock input is always from pod 1 (on the master card in multi-card modules). You cannot qualify the sampling clock input with signals from the other pods clock inputs.
- You cannot split a 16760 logic analyzer module.
- Pods are assigned individually instead of in *pod pairs* (and you can only assign a pod to the module or reserve it for time tag storage).
- There is no *Half Channel Timing Mode*.
- There is no timing zoom feature.

Channels and Memory Depth

	16760A
Memory depth	64 M
Channels	34 channels/card * number of cards in module

Timing Mode Sampling Options/Period

- **Full channel (see page 582), 800 MHz** = *Full Channel Timing Mode*

  With this sampling option, you can use the full memory depth (see page 582) of your logic analyzer card, with data being sampled and stored every 1.25 ns.

NOTE

With the Sample Period at 1.25 ns, data is acquired at four times the trigger sequencer rate. This means that data must be present for at least four samples before the trigger sequencer can reliably detect it. The trigger sequencer could miss data present for less than four sample periods.

The trigger sequencer treats the data as a group of four samples for each sequencer clock. This means that the trigger point indication could be off by three samples and bus/signal occurrence counts could be off by up to a factor of four.

Although the trigger sequencer cannot detect all data, the analyzer will correctly capture all data present for at least one sample period.

- **Transitional / Store qualified, Full channel 400 MHz** = *Transitional / Store Qualified Timing Mode*

  At the 400 MHz sample rate (2.5 ns sampling period), one *pod* (17 channels) must be *reserved for time tag storage*. At slower sample rates, you can get full channels (see page 582) by using 1/2 (or less) of a module's acquisition memory depth (see page 582) (for more information, see 16760 Logic Analyzer Memory Depth and Channel Count Trade-offs (see page 585)).

  Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period ranges from 2.5 ns to 1 ms. You can set the sample rate to go slower with the Sample Period control. See transitional timing (see page 376).

NOTE

With the Sample Period at 2.5 ns, data is acquired at two times the trigger sequencer rate. This means that data must be present for at least two samples before the trigger sequencer can reliably detect it. The trigger sequencer could miss data present for less than two sample periods.

The trigger sequencer treats the data as a group of two samples for each sequencer clock. This means that the trigger point indication could be off by one sample and bus/signal occurrence counts could be off by up to a factor of two.

Although the trigger sequencer cannot detect all data, the analyzer will correctly capture all data present for at least one sample period.

State Mode Sampling Options

For all state mode sampling options, clocking is restricted to the J clock on Pod 1 of the *master card* of the *module*.

- **200 Mb/s** = *General State Mode*

  With this sampling option:

  - You can have full channels (see page 582) and quarter memory depth (see page 582), or you can get half memory depth by reserving one pod (17 channels) for time tag storage (for more information, see 16760 Logic Analyzer Memory Depth and Channel Count Trade-offs (see page 585)).
  - You can have clocks where the rising edge, the falling edge, or both edges indicate valid data.
  - You have full trigger resources (16 patterns, 15 ranges, timers, global counters, occurrence counters) and full trigger actions.
  - State sampling speed matches your device under test's clock rate, up to 200 MHz.

- **400 Mb/s** = *Turbo State Mode*

  With this sampling option:

- One pod (17 channels) is reserved for time tag storage.
- You have half memory depth (see page 582).
- You can have clocks where the rising edge, the falling edge, or both edges indicate valid data.
- Trigger resources are limited to 8 patterns, 4 ranges, and 2 occurrence counters. Trigger actions are limited to: goto and trigger and fill memory.
- State sampling speed matches your device under test's clock rate, up to 400 MHz.

• **800 Mb/s** = *800 Mb/s State Mode*

With this sampling option:

- One pod (17 channels) is reserved for time tag storage.
- You have full memory depth (see page 582).
- You must specify whether the input clock signal is periodic or aperiodic. You can have clocks where the rising edge, the falling edge, or both edges indicate valid data.
- Trigger resources are limited to 4 patterns or 2 ranges on each pod. Trigger actions are limited to trigger and fill memory. You can have a maximum of 4 sequence steps.
- State sampling speed matches your device under test's clock rate, up to 800 MHz.

• **1250 Mb/s Half Channel** = *1250 Mb/s State Mode*

With this sampling option:

- One pod (17 channels) is reserved for time tag storage. Data is only acquired from the even-numbered channels (0, 2, 4, etc.).
- You have double memory depth (see page 582).
- The input clock signal must be periodic, and both edges indicate valid data. Clock inputs on *expander cards* of a multi-card *module* cannot be used as extra data channels.
- Trigger resources are limited to 3 patterns or 1 range on each pod. Trigger actions are limited to trigger and fill memory. You can have a maximum of 2 sequence steps.
- State sampling speed matches your device under test's clock rate, up to 1250 MHz.

• **1500 Mb/s Half Channel** = *1500 Mb/s State Mode*

With this sampling option:

- One pod (17 channels) is reserved for time tag storage. Data is only acquired from the even-numbered channels (0, 2, 4, etc.).
- You have double memory depth (see page 582).

- The input clock signal must be periodic, and both edges indicate valid data. Clock inputs on *expander cards* of a multi-card *module* cannot be used as extra data channels.
- Trigger resources are limited to 3 patterns or 1 range on each pod. Trigger actions are limited to trigger and fill memory. You can have a maximum of 2 sequence steps.
- State sampling speed matches your device under test's clock rate, up to 1500 MHz.

See Also

- 16760 Logic Analyzer Memory Depth and Channel Count Trade-offs (see page 585)
- Eye Finder Operation in the 16760 Logic Analyzer (see page 586)
- Eye Scan in Logic Analyzers that Support Differential Signals (see page 382)
- 16760 Logic Analyzer Specifications and Characteristics (see page 614)

16760 Logic Analyzer Memory Depth and Channel Count Trade-offs

This topic describes the interaction between channel count, memory depth, and triggering in the 16760 logic analyzer's:

- State Sampling Mode (see page 585)
- Transitional Timing Sampling Mode (see page 586)

200 Mb/s General State Sampling Mode

(With all other state mode sampling options, one pod (17 channels) is reserved for time tag storage.)

Time Tag Storage Requires 1 Pod or 16M Acquisition Memory

- In the *Agilent Logic Analyzer* application, all modules are time-correlated; you cannot turn off *time tag storage* (as you could with previous Agilent logic analysis systems).
- To use 32M of a module's acquisition memory, one *pod* must be *reserved for time tag storage*. To use all pods, you must use 16M (or less) of a module's acquisition memory.
- In the 16760 logic analyzer's 200 Mb/s State Mode, the number of timers available = 2 x (number of cards) - 1.

Default Settings

- Time tag storage is always on (and cannot be turned off).
- Memory depth is set at 16M.
- All pods are available for capturing data.
- If 32M memory is selected, the default pod to be used for time tag storage is the leftmost, but any pod without buses or signals assigned can be used.

Selecting 32M Memory Depth when No Channels Assigned to a Pod

- The pod is automatically reserved for time tag storage.

Selecting 32M Memory Depth when Channels Assigned to All Pods

A dialog appears to caution you that:

- Bus/signals will lose assigned channels.
- Trigger specifications that use timer resources may be affected.

Going from 32M Memory Depth to 16M Memory Depth

- The pod reserved for time tag storage is automatically freed (assigned to the logic analyzer) so it can be used to capture data.

Transitional Timing Sampling Mode

Time Tag Storage Requires 1 Pod or 16M Acquisition Memory

- The transitional timing sampling mode also requires *time tag storage*.
- When the smallest sampling period (2.5 ns) is chosen, one *pod* must be *reserved for time tag storage*. In this case, you cannot use 16M (or less) of a module's acquisition memory to gain back the *pod*.
- With other sampling periods, the memory depth and channel count trade-offs are the same as in the state sampling mode. That is, to use 32M of a module's acquisition memory, one *pod* must be *reserved for time tag storage*. To use all pods, you must use 16M (or less) of a module's acquisition memory.
- In the 16760 logic analyzer's timing modes, the number of timers available = 2 x (number of cards) - 1.

Default Settings

- Time tag storage is required.
- If full memory is selected, the default pod to be used for time tag storage is the leftmost, but any pod without buses or signals assigned can be used.

See Also

- 16760 Logic Analyzer Notes (see page 582)
- Configuring Logic Analyzer Modules (see page 76)
- To set acquisition memory depth (see page 112)
- Choosing the Sampling Mode (see page 97)

Eye Finder Operation in the 16760 Logic Analyzer

For a general description of *eye finder* see Eye Finder Overview (see page 379).

In the 16760 Logic Analyzer...

Eye finder operation in the 16760 logic analyzer can be confusing because there are five state mode sampling options:

State Sampling Option	Sampling Clock Edges	Edges-To-Edge Timing
200 Mb/s = *General State Mode*	Rising edge, Falling edge, or Both edges	Aperiodic or Periodic
400 Mb/s = *Turbo State Mode*	Rising edge, Falling edge, or Both edges	Aperiodic or Periodic
800 Mb/s = *800 Mb/s State Mode*	Rising edge, Falling edge, or Both edges	Aperiodic or Periodic
1250 Mb/s Half Channel = *1250 Mb/s State Mode*	Both edges	Periodic
1500 Mb/s Half Channel = *1500 Mb/s State Mode*	Both edges	Periodic

The 200 and 400 Mb/s modes support single clock edge sampling (either rising or falling) as well as sampling on both edges. There is no restriction on variability in edge-to-edge timing.

The 800 Mb/s mode also supports single and dual edge clocking. An option appears to let you indicate whether the clock is periodic (time between active edges is constant) or aperiodic (time between active edges can vary). This option does not affect the sampling operation. It tells the software how to process time tags.

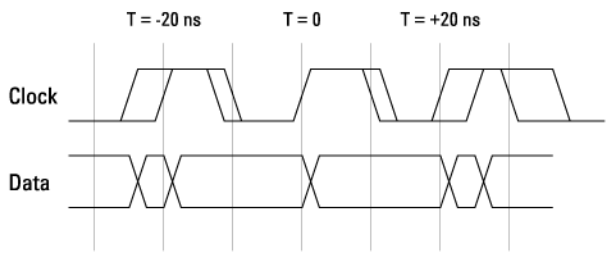
The 1250 and 1500 Mb/s modes require a periodic clock and only support sampling on both clock edges.

16760 Logic Analyzer Eye Finder Example

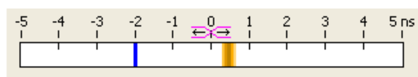
For example, if the device under test operates with an aperiodic clock that alternates between a 20 ns and a 25 ns period, then the 200, 400, or 800 Mb/s modes can be used. The 1250 and 1500 Mb/s modes cannot be used because they require a periodic clock.

What you'll see in *eye finder* is bounded by the *eye finder* scan range. In the 200 or 400 Mb/s mode, the *eye finder* scan range is +/- 5 ns around the clock edge (T=0). Because the minimum clock period is 20 ns, the *eye finder* scan will not see the data transitions for the previous and next clock cycles.

Consider a rising edge active flip flop clocked by with a dual mode 20/25 ns clock. If you look at the clock and data with an oscilloscope in infinite persistence mode at 10 ns/div, you might see:



In *eye finder*, in the 200 or 400 Mb/s mode, you'd see the transitions related to the active clock edge at T=0 because the *eye finder* scan range is +/- 5 ns.



If you set the sample position (blue bar in the *eye finder* display) at about T=-2 ns, you will sample good data before the clock edge in this example. To sample data after the clock, place the blue bar at T=+2 ns.

The signals in your device under test may have a different delay from the clock, which will shift the location of the detected transitions in the sample *eye finder* display above. If the delay exceeds 5 ns, *eye finder* won't show you the transition at all. In this case, sampling at T=0 is as good as any other position.

See Also

- Eye Scan in Logic Analyzers that Support Differential Signals (see page 382)

16800-Series Logic Analyzer Notes

- Channels and Memory Depth (see page 588)
- Maximum State Sampling Speed (see page 589)
- Timing Mode Sampling Options/Period (see page 589)
- State Mode Sampling Options (see page 590)
- Timing Zoom (see page 591)

Channels and Memory Depth

	Option 001	Option 004*	Option 016*	Option 032*
Memory depth	1 M	4 M	16 M	32 M

Channels	16801A, 16821A: 34 channels 16802A, 16822A: 68 channels 16803A, 16823A: 102 channels 16804A: 136 channels 16806A: 204 channels
*Upgrades for the 16800 Series logic analyzers can be ordered using these model numbers: - For 16801A or 16821A, use E5876A. - For 16802A or 16822A, use E5877A. - For 16803A or 16823A, use E5878A. - For 16804A, use E5879A. - For 16806A, use E5880A. (See also Installing Licensed Hardware Upgrades (see page 124).)	

See also Memory Depth and Channel Count Trade-offs (see page 374).

Maximum State Sampling Speed

	Option 250	Option 500*
Max. state clock rate	250 MHz	450 MHz
Max. state data rate	250 Mb/s	500 Mb/s
*Upgrades for the 16800 Series logic analyzers can be ordered using these model numbers: - For 16802A or 16822A, use E5877A. - For 16803A or 16823A, use E5878A. - For 16804A, use E5879A. - For 16806A, use E5880A. (See also Installing Licensed Hardware Upgrades (see page 124).)		

Timing Mode Sampling Options/Period

- **Full channel (see page 589), 500 MHz** = *Full Channel Timing Mode*

  With this sampling option, you can use the full memory depth (see page 589) of your logic analyzer card, with data being sampled and stored as often as every 2.0 ns. You can set the sample rate to go slower with the Sample Period control.

- **Half channel (see page 589), 1 GHz** = *Half Channel Timing Mode*

  With this sampling option, only one pod of each pod pair is available, and the memory depth (see page 589) is doubled. Channels assigned to unavailable pods are ignored. You can specify which pod to use by toggling the Pod field in Format.

  Data is sampled and stored every 1 ns; this rate cannot be changed.

  This option is not available with the 16801A and 16821A 34-channel logic analyzer models.

- **Transitional / Store qualified, Full channel 500 MHz** = *Transitional / Store Qualified Timing Mode*

  At the 500 MHz sample rate (2.0 ns sampling period), one *pod pair* (34 channels) must be *reserved for time tag storage*. At slower sample rates, you can get full channels (see page 589) by using 1/2 (or less) of a module's acquisition memory depth (see page 589) (for more information, see Memory Depth and Channel Count Trade-offs (see page 374)).

Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period ranges from 2.0 ns to 500 us. See transitional timing (see page 376).

The maximum sample rate with this option for the 16801A and 16821A 34-channel logic analyzer models is 250 MHz, and you must use 1/2 (or less) of the module's acquisition memory.

State Mode Sampling Options

- **250 MHz** = *General State Mode*

  With this sampling option, you can have full channels (see page 589) and half memory depth (see page 589), or you can get full memory depth by reserving one pod pair (34 channels) for time tag storage (for more information, see Memory Depth and Channel Count Trade-offs (see page 374)).

  State sampling speed matches your device under test's clock rate, up to 250 MHz.

  In the 16801A and 16821A 34-channel logic analyzer models, you are limited to half memory depth.

- **450 MHz** = *Turbo State Mode*

  With this sampling option (available with Option 500), one pod pair (34 channels) is reserved for time tag storage, and you have full memory depth (see page 589). Clocking is restricted to the J clock on Pod 1 of the *master card* of the *module*, and triggering is restricted to two trigger functions.

  State sampling speed matches your device under test's clock rate, up to 450 MHz.

  This option is not available with the 16801A and 16821A 34-channel logic analyzer models.

- **500 MHz** = *Turbo State Mode* (requires sampling on both clock edges)

  This sampling option is similar to the 450 MHz Turbo State Mode, except that the logic analyzer can only sample on both edges of the input clock.

  State sampling speed matches your device under test's clock rate, up to 500 MHz.

  This option is not available with the 16801A and 16821A 34-channel logic analyzer models.

Timing Zoom Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer. It uses a 64K-sample, 4 GHz timing analyzer to sample data every 250 ps on all channels.

See Also

- 16800 Series Logic Analyzer Specifications and Characteristics (see page 621)

16910/11 Logic Analyzer Notes

- Channels and Memory Depth (see page 591)
- Maximum State Sampling Speed (see page 591)
- Timing Mode Sampling Options/Period (see page 591)
- State Mode Sampling Options (see page 592)
- Timing Zoom (see page 593)

Channels and Memory Depth

	Option 256	Option 001*	Option 004*	Option 016*	Option 032*
Memory depth	256 K	1 M	4 M	16 M	32 M
Channels	16910A: 102 channels/card * number of cards in module 16911A: 68 channels/card * number of cards in module				
*Upgrades for the 16910A and 16911A logic analyzers can be ordered using model numbers E5865A and E5866A, respectively. (See also Installing Licensed Hardware Upgrades (see page 124).)					

See also Memory Depth and Channel Count Trade-offs (see page 374).

Maximum State Sampling Speed

	Option 250	Option 500*
Max. state clock rate	250 MHz	450 MHz
Max. state data rate	250 Mb/s	500 Mb/s
*Upgrades for the 16910A and 16911A logic analyzers can be ordered using model numbers E5865A and E5866A, respectively. (See also Installing Licensed Hardware Upgrades (see page 124).)		

Timing Mode Sampling Options/Period

- **Full channel (see page 591), 500 MHz** = *Full Channel Timing Mode*

  With this sampling option, you can use the full memory depth (see page 591) of your logic analyzer card, with data being sampled and stored as often as every 2.0 ns. You can set the sample rate to go slower with the Sample Period control.

- **Half channel (see page 591), 1 GHz** = *Half Channel Timing Mode*

With this sampling option, only one pod of each pod pair is available, and the memory depth (see page 591) is doubled. Channels assigned to unavailable pods are ignored. You can specify which pod to use by toggling the Pod field in Format.

Data is sampled and stored every 1 ns; this rate cannot be changed.

- **Transitional / Store qualified, Full channel 500 MHz** = *Transitional / Store Qualified Timing Mode*

  At the 500 MHz sample rate (2.0 ns sampling period), one *pod pair* (34 channels) must be *reserved for time tag storage*. At slower sample rates, you can get full channels (see page 591) by using 1/2 (or less) of a module's acquisition memory depth (see page 591) (for more information, see Memory Depth and Channel Count Trade-offs (see page 374)).

  Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period ranges from 2.0 ns to 500 us. See transitional timing (see page 376).

State Mode Sampling Options

- **250 MHz** = *General State Mode*

  With this sampling option, you can have full channels (see page 591) and half memory depth (see page 591), or you can get full memory depth by reserving one pod pair (34 channels) for time tag storage (for more information, see Memory Depth and Channel Count Trade-offs (see page 374)).

  State sampling speed matches your device under test's clock rate, up to 250 MHz.

- **450 MHz** = *Turbo State Mode*

  With this sampling option (available with Option 500), one pod pair (34 channels) is reserved for time tag storage, and you have full memory depth (see page 591). Clocking is restricted to the J clock on Pod 1 of the *master card* of the *module*, and triggering is restricted to two trigger functions.

  State sampling speed matches your device under test's clock rate, up to 450 MHz.

- **500 MHz** = *Turbo State Mode* (requires sampling on both clock edges)

  This sampling option is similar to the 450 MHz Turbo State Mode, except that the logic analyzer can only sample on both edges of the input clock.

  State sampling speed matches your device under test's clock rate, up to 500 MHz.

Timing Zoom Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer. It uses a 64K-sample, 4 GHz timing analyzer to sample data every 250 ps on all channels.

See Also

- 16910/11 Logic Analyzer Specifications and Characteristics (see page 628)

16950/51 Logic Analyzer Notes

- Channels and Memory Depth (see page 593)
- Timing Mode Sampling Options/Period (see page 593)
- State Mode Sampling Options (see page 594)
- Timing Zoom (see page 594)

Channels and Memory Depth

16950A/B Memory depth	**Option 256**[**]	**Option 001**[*]	**Option 004**[*]	**Option 016**[*]	**Option 032**[*]	**Option 064**[*]
	256 K	1 M	4 M	16 M	32 M	64 M
16951B Memory depth	256 M (no memory depth options)					
Channels	68 channels/card * number of cards in module					

[*]Upgrades for the 16950 logic analyzer can be ordered using model number E5875A. (See also Installing Licensed Hardware Upgrades (see page 124).)
[**]Available on the 16950A logic analyzer only.

Timing Mode Sampling Options/Period

- **Full channel (see page 593), 600 MHz** = *Full Channel Timing Mode*

  With this sampling option, you can use the full memory depth (see page 593) of your logic analyzer card, with data being sampled and stored as often as every 1.67 ns. You can set the sample rate to go slower with the Sample Period control.

- **Half channel (see page 593), 1.2 GHz** = *Half Channel Timing Mode*

  With this sampling option, only one pod of each pod pair is available, and the memory depth (see page 593) is doubled. Channels assigned to unavailable pods are ignored. You can specify which pod to use by toggling the Pod field in Format.

  Data is sampled and stored every 833 ps; this rate cannot be changed.

- **Transitional / Store qualified, Full channel 600 MHz** = *Transitional / Store Qualified Timing Mode*

  At the 600 MHz sample rate (1.667 ns sampling period), one *pod pair* (34 channels) must be *reserved for time tag storage*. At slower sample rates, you can get full channels (see page 593) by using 1/2 (or less) of a module's acquisition memory depth (see page 593) (for more information, see Memory Depth and Channel Count Trade-offs (see page 374)).

Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period ranges from 1.667 ns to 500 us. See transitional timing (see page 376).

State Mode Sampling Options

- **300 MHz** = *General State Mode*

  With this sampling option, you can have full channels (see page 593) and half memory depth (see page 593), or you can get full memory depth by reserving one pod pair (34 channels) for time tag storage (for more information, see Memory Depth and Channel Count Trade-offs (see page 374)).

  State sampling speed matches your device under test's clock rate, up to 300 MHz.

- **600 MHz** (16950A) or **667 MHz** (16950B, 16951B) = *Turbo State Mode*

  With this sampling option, one pod pair (34 channels) is reserved for time tag storage, and you have full memory depth (see page 593). Clocking is restricted to the J clock on Pod 1 of the *master card* of the *module*, and triggering is restricted to two trigger functions.

  State sampling speed matches your device under test's clock rate, up to 600 MHz (16950A) or 667 MHz (16950B, 16951B).

Timing Zoom

Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer. It uses a 64K-sample, 4 GHz timing analyzer to sample data every 250 ps on all channels.

See Also

- Eye Scan in Logic Analyzers that Support Differential Signals (see page 382)
- 16950/51 Logic Analyzer Specifications and Characteristics (see page 636)

Specifications and Characteristics

Describes the specifications, characteristics, and requirements of supported logic analyzers and logic analysis systems.

- 1680/1690-Series Logic Analyzer Specifications and Characteristics (see page 595)
- 16740/41/42 Logic Analyzer Specifications and Characteristics (see page 598)
- 16750/51/52 Logic Analyzer Specifications and Characteristics (see page 603)
- 16753/54/55/56 Logic Analyzer Specifications and Characteristics (see page 607)
- 16760 Logic Analyzer Specifications and Characteristics (see page 614)
- 16800-Series Logic Analyzer Specifications and Characteristics (see page 621)
- 16910/11 Logic Analyzer Specifications and Characteristics (see page 628)
- 16950/51 Logic Analyzer Specifications and Characteristics (see page 636)
- 16900-Series Logic Analysis System Frame Characteristics (see page 643)

See Also

- What is a Specification (see page 644)
- What is a Characteristic (see page 645)

1680/1690-Series Logic Analyzer Specifications and Characteristics

Describes the specifications, characteristics, and requirements of the 1680A/AD-series and 1690A/AD-series logic analyzers.

- 1680/1690-Series Logic Analyzer Specifications (see page 595)
- 1680/1690-Series Logic Analyzer Characteristics (see page 596)

See Also

- What is a Specification (see page 644)
- What is a Characteristic (see page 645)

1680/1690-Series Logic Analyzer Specifications

Threshold Accuracy	±(65 mV +1.5 % of setting)
Minimum Master-to-Master Clock Time	5.0 ns

Setup/Hold Time (Single Clock, Single Edge)	2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100 ps increments per channel
Setup/Hold Time (Multiple Clock, Multiple Edge)	3.0 ns window adjustable from 5.0/-2.0 ns to -1.5/4.5 ns in 100 ps increments per channel

1680/1690-Series Logic Analyzer Characteristics

- General Information (see page 596)
- State Analysis (see page 596)
- Timing Analysis (see page 597)
- Triggering (see page 597)
- Operating Environment Characteristics (see page 598)

General Information

State/timing channels:	1680A/AD, 1690A/AD: 136 1681A/AD, 1691A/AD: 102 1682A/AD, 1692A/AD: 68 1683A/AD, 1693A/AD: 34
User interface:	Windows® XP Professional
Printers:	Can print to any local or network printer supported by Windows® XP Professional.
Dimensions:	1680 - 257 mm height (10.14 in), 443 mm width (17.45 in), 385 mm depth (15.15 in) 1690 - 153 mm height (6.05 in), 438 mm width (17.23 in), 335 mm depth (13.16 in)
Weight:	1680 - 13.2 kg (29.1 lbs) 1690 - 7.5 kg (16.5 lbs)

State Analysis

Maximum state speed:	200 MHz
State memory depth:	1680/1690A-series: 256K 1680/1690AD-series: 1 M
Minimum state clock pulse width:	1.2 ns
Time tag resolution:	4ns or ±0.1% (whichever is greater)
Maximum time count between states:	17 seconds
State clock/qualifiers	4 (2 on 34 channel models)

Minimum master-to-master clock:	5.0 ns
Minimum master-to-slave clock:	2.0 ns
Minimum slave-to-slave clock:	5.0 ns

Timing Analysis

Maximum timing sample rate:	Half channel: 800 MHz Full channel: 400 MHz
Timing memory depth:	1680/1690A-series, half channel: 1 M 1680/1690A-series, full channel: 512 K 1680/1690AD-series, half channel: 4 M 1680/1690AD-series, full channel: 2 M
Sample period, full channels:	2.5 ns to 1 ms
Sample period, half channels:	1.25 ns
Sample period accuracy:	±0.01% of sample period ±100 ps
Channel-to-channel skew:	<1.5 ns typical
Time interval accuracy:	±(sample period + channel-to-channel skew + 0.01% of time interval reading)

Triggering

Sequencer speed:	200 MHz
Maximum occurrence count value:	16,777,215
Range width:	32 bits
Timer value range:	100 ns to 5497 seconds
Timer resolution:	5 ns
Timer accuracy:	±10 ns + 0.01%
Trigger resources:	16 patterns 15 patterns
Timers:	1680A/AD, 1690A/AD: 3 1681A/AD, 1691A/AD: 2 1682A/AD, 1692A/AD: 1 1683A/AD, 1693A/AD: 0

Occurrence counters:	1 per sequence step
Trigger sequence steps:	16
Minimum detectable glitch:	1.5 ns
Trigger in arms logic analyzer:	15 ns, typical delay
Trigger to trigger out:	150 ns, typical delay

Operating Environment Characteristics

Temperature:	Instrument: 5°C to 50°C Disk media: 10°C to 40°C Probe lead sets and cables: 0°C to 65°C
Humidity:	Instrument: Up to 95% relative humidity at 40°C Disk media and hard drive: 8% to 85% relative humidity
Altitude:	4,572 m (15,000 ft) operating 15,300 m (50,000 ft) non-operating

16740/41/42 Logic Analyzer Specifications and Characteristics

Describes the specifications and characteristics of the 16740/41/42 logic analyzers.

- 16740/41/42 Logic Analyzer Specifications (see page 598)
- 16740/41/42 Logic Analyzer Characteristics (see page 599)

See Also

- What is a Specification (see page 644)
- What is a Characteristic (see page 645)

16740/41/42 Logic Analyzer Specifications

Maximum State Clock Speed	200 MHz
Threshold Accuracy	±(65 mV + 1.5% of threshold setting)
Minimum Master-to-Master Clock Time	5.0 ns at 200 MHz
Setup/Hold Time (Single Clock, Single Edge) [1] (see page 599)	2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100 ps increments per channel

Setup/Hold Time (Multiple Clock, Multiple Edge) [1] (see page 599)	3.0 ns window adjustable from 5.0/-2.0 ns to -1.5/4.5 ns in 100 ps increments per channel
[1]Specified for an input signal VH = -0.9 V, VL = -1.7 V, threshold = -1.3 V, slew rate = 1 V/ns.	

16740/41/42 Logic Analyzer Characteristics

- General Information (see page 599)
- State Analysis (see page 599)
- Timing Analysis (see page 600)
- Triggering (see page 601)
- Power Requirements (see page 602)
- Operating Environment Characteristics (see page 602)
- Storage (see page 602)

General Information

Channel counts:	1-card module = 64 data, 4 clock 2-card module = 132 data, 4 clock 3-card module = 200 data, 4 clock 4-card module = 268 data, 4 clock 5-card module = 336 data, 4 clock

State Analysis

Maximum state clock speed:	200 MHz
Maximum memory depth:	16740A = 1 M 16741A = 4 M 16742A = 16 M
Minimum setup/hold time [1] (see page 600) :	2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100–ps increments per channel
Minimum state clock pulse width:	1.2 ns
Minimum master-to-master clock:	5.0 ns at 200 MHz
Minimum master-to-slave clock:	2 ns
Minimum slave-to-slave clock:	5.0 ns at 200 MHz
State clocks:	4

State clock qualifiers:	4
Time tag resolution [2] (see page 600) :	4 ns
Maximum time count between states:	17 seconds
Maximum state tag count [2] (see page 600) :	2e32
Store qualification:	Default and per sequence step
[1]Specified for single-edge, single-clock acquisition. Multi-edge setup/hold window is 3.0 ns. [2]When all pods are being used, time or state tags halve the memory depth.	

Timing Analysis

- Timing Zoom (see page 600)
- Conventional Timing (see page 600)
- Transitional Timing (see page 601)

Timing Zoom

Sample rates:	2 GHz, 1 GHz, 500 MHz, 250 MHz
Sample period accuracy:	±50 ps
Channel-to-channel skew:	<1.0 ns
Timing interval accuracy:	±(sample period + channel-to-channel skew + 0.01% of time interval reading)
Trigger position:	Start, center, end, or user-defined
Memory depth:	16 K

Conventional Timing

Maximum sample rate:	Half channel = 800 MHz Full channel = 400 MHz
Memory depth:	16740A, half channel = 2 M samples per channel 16740A, full channel = 1 M samples per channel 16741A, half channel = 8 M samples per channel 16741A, full channel = 4 M samples per channel 16742A, half channel = 32 M samples per channel 16742A, full channel = 16 M samples per channel
Sample period accuracy:	±(250 ps + 0.01% of sample period)
Channel-to-channel skew:	<1.5 ns, typical

Timing interval accuracy:	±(sample period + channel-to-channel skew + 0.01% of time interval reading)
Minimum data pulse width:	1.5 ns for data capture 5.0 ns for trigger sequencing

Transitional Timing

Maximum timing analysis sample rate:	400 MHz
Minimum data pulse width:	3.8 ns for data capture 5.1 ns for trigger sequencing
Number of channels:	For sample rates < 400 MHz: 68 x (number of cards) For sample rates = 400 MHz: 68 x (number of cards) - 34
Global counters:	1
Glitch/edge recognizers:	1 per pod pair

Triggering

Maximum trigger sequencer speed:	200 MHz
State sequence steps:	16
Timing sequence steps:	16
Sequence step branching:	Arbitrary 4-way "If/then/else"
Maximum occurrence count value:	16,777,215
Pattern recognizers:	16
Range recognizers:	15
Range width:	32
Occurrence counters:	1 per sequence step
Global counters:	2
Flags:	4, shared across all connected logic analysis system frames
Flag set/reset to evaluation:	110 ns, typical
Timers:	200 MHz state: 2 x number of cards timing: (2 x number of cards) - 1
Timer value range:	100 ns to 5497 seconds
Timer resolution:	5 ns

Timer accuracy:	±10 ns + 0.01%
Timer reset latency:	70 ns
Glitch/edge recognizers:	2 per pod pair (timing only)
Minimum detectable glitch:	1.5 ns
Greater than duration:	6 ns to 100 ms in 6–ns increments
Less than duration:	12 ns to 100 ms in 6–ns increments
Data in to trigger out:	150 ns, typical

Power Requirements

All necessary power is supplied by the backplane connector of the logic analysis system mainframe.

Operating Environment Characteristics

Indoor use only.	
Temperature:	Instrument (except disk and media): 0°C to 50°C (+32°F to 122°F) Probe lead sets and cables: 0°C to 65°C (+32°F to 149°F)
Humidity:	Instrument, probe lead sets, and cables: Up to 80% relative humidity at 40°C (+104°F)
Altitude:	Operating: 4,600 m (15,000 ft) Non-operating: 15,300 m (50,000 ft)
Vibration:	Operating: Random vibration 5-500 Hz, 10 minutes per axis, approximately 0.2 g rms Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 2.41 g rms; and swept sine resonant search, 5 to 500 Hz, 0.50 g (0-peak), 5-minute resonant dwell at 4 resonances per axis.

Reliability is enhanced when operating within the following ranges:

Temperature:	+20°C to 35°C (+68°F to 95°F)
Humidity:	20% to 80% non-condensing

Storage

Store or ship the logic analyzer in environments with the following limits:

Temperature:	-40°C to +75°C
Humidity:	Up to 90% relative humidity at 65°C
Altitude:	Up to 15,300 m (50,000 ft)

Protect the module from temperature extremes which cause condensation on the instrument.

16750/51/52 Logic Analyzer Specifications and Characteristics

Describes the specifications and characteristics of the 16750/51/52 logic analyzers.

- 16750/51/52 Logic Analyzer Specifications (see page 603)
- 16750/51/52 Logic Analyzer Characteristics (see page 603)

See Also

- What is a Specification (see page 644)
- What is a Characteristic (see page 645)

16750/51/52 Logic Analyzer Specifications

Maximum State Clock Speed	400 MHz
Threshold Accuracy	±(65 mV + 1.5% of threshold setting)
Minimum Master-to-Master Clock Time	5.0 ns at 200 MHz 2.5 ns at 400 MHz
Setup/Hold Time (Single Clock, Single Edge) [1] (see page 603)	2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100 ps increments per channel
Setup/Hold Time (Multiple Clock, Multiple Edge) [1] (see page 603)	3.0 ns window adjustable from 5.0/-2.0 ns to -1.5/4.5 ns in 100 ps increments per channel
[1]Specified for an input signal VH = -0.9 V, VL = -1.7 V, threshold = -1.3 V, slew rate = 1 V/ns.	

16750/51/52 Logic Analyzer Characteristics

- General Information (see page 604)
- State Analysis (see page 604)
- Timing Analysis (see page 604)
- Triggering (see page 606)
- Power Requirements (see page 606)
- Operating Environment Characteristics (see page 607)
- Storage (see page 607)

General Information

Channel counts:	1-card module = 64 data, 4 clock 2-card module = 132 data, 4 clock 3-card module = 200 data, 4 clock 4-card module = 268 data, 4 clock 5-card module = 336 data, 4 clock

State Analysis

Maximum state clock speed:	400 MHz
Maximum memory depth:	16750A/B = 4 M 16751A/B = 16 M 16752A/B = 32 M
Minimum setup/hold time [1] (see page 604) :	2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100–ps increments per channel
Minimum state clock pulse width:	1.2 ns
Minimum master-to-master clock:	5.0 ns at 200 MHz 2.5 ns at 400 MHz
Minimum master-to-slave clock:	2 ns
Minimum slave-to-slave clock:	5.0 ns at 200 MHz 2.5 ns at 400 MHz
State clocks:	4
State clock qualifiers:	4
Time tag resolution [2] (see page 604) :	4 ns
Maximum time count between states:	17 seconds
Maximum state tag count [2] (see page 604) :	2e32
Store qualification:	Default and per sequence step
[1]Specified for single-edge, single-clock acquisition. Multi-edge setup/hold window is 3.0 ns. [2]When all pods are being used, time or state tags halve the memory depth.	

Timing Analysis

- Timing Zoom (see page 605)
- Conventional Timing (see page 605)
- Transitional Timing (see page 605)

Timing Zoom

Sample rates:	2 GHz, 1 GHz, 500 MHz, 250 MHz
Sample period accuracy:	±50 ps
Channel-to-channel skew:	<1.0 ns
Timing interval accuracy:	±(sample period + channel-to-channel skew + 0.01% of time interval reading)
Memory depth:	16 K

Conventional Timing

Maximum sample rate:	Half channel = 800 MHz Full channel = 400 MHz
Memory depth:	16750A/B, half channel = 8 M samples per channel 16750A/B, full channel = 4 M samples per channel 16751A/B, half channel = 32 M samples per channel 16751A/B, full channel = 16 M samples per channel 16752A/B, half channel = 64 M samples per channel 16752A/B, full channel = 32 M samples per channel
Sample period accuracy:	±(250 ps + 0.01% of sample period)
Channel-to-channel skew:	<1.5 ns, typical
Timing interval accuracy:	±(sample period + channel-to-channel skew + 0.01% of time interval reading)
Minimum data pulse width:	1.5 ns for data capture 5.0 ns for trigger sequencing

Transitional Timing

Maximum timing analysis sample rate:	400 MHz
Minimum data pulse width:	3.7 ns for data capture 5.0 ns for trigger sequencing
Number of channels:	For sample rates < 400 MHz: 68 x (number of cards) For sample rates = 400 MHz: 68 x (number of cards) - 34
Global counters:	1
Glitch/edge recognizers:	1 per pod pair

Triggering

Maximum trigger sequencer speed:	200 MHz
State sequence steps:	16
Timing sequence steps:	16
Sequence step branching:	Arbitrary 4-way "If/then/else"
Maximum occurrence count value:	16,777,215
Pattern recognizers:	16
Range recognizers:	15
Range width:	32
Occurrence counters:	1 per sequence step
Global counters:	2
Flags:	4, shared across all connected logic analysis system frames
Flag set/reset to evaluation:	110 ns, typical
Timers:	200 MHz state: 2 x number of cards timing: (2 x number of cards) - 1
Timer value range:	100 ns to 4397 seconds
Timer resolution:	4 ns
Timer accuracy:	±10 ns + 0.01%
Timer reset latency:	60 ns
Glitch/edge recognizers:	2 per pod pair (timing only)
Minimum detectable glitch:	1.5 ns
Greater than duration:	6 ns to 100 ms in 6–ns increments
Less than duration:	12 ns to 100 ms in 6–ns increments
Data in to trigger out:	150 ns, typical

Power Requirements

All necessary power is supplied by the backplane connector of the logic analysis system mainframe.

Operating Environment Characteristics

Indoor use only.	
Temperature:	Instrument (except disk and media): 0°C to 50°C (+32°F to 122°F) Probe lead sets and cables: 0°C to 65°C (+32°F to 149°F)
Humidity:	Instrument, probe lead sets, and cables: Up to 80% relative humidity at 40°C (+104°F)
Altitude:	Operating: 4,600 m (15,000 ft) Non-operating: 15,300 m (50,000 ft)
Vibration:	Operating: Random vibration 5-500 Hz, 10 minutes per axis, approximately 0.2 g rms Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 2.41 g rms; and swept sine resonant search, 5 to 500 Hz, 0.50 g (0-peak), 5-minute resonant dwell at 4 resonances per axis.

Reliability is enhanced when operating within the following ranges:

Temperature:	+20°C to 35°C (+68°F to 95°F)
Humidity:	20% to 80% non-condensing

Storage Store or ship the logic analyzer in environments with the following limits:

Temperature:	-40°C to +75°C
Humidity:	Up to 90% relative humidity at 65°C
Altitude:	Up to 15,300 m (50,000 ft)

Protect the module from temperature extremes which cause condensation on the instrument.

16753/54/55/56 Logic Analyzer Specifications and Characteristics

Describes the specifications and characteristics of the 16753/54/55/56 logic analyzers.

NOTE

Items marked with an asterisk (*) are specifications. All others are characteristics.

"Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

- Module Channel Counts (see page 608)
- Probes (see page 608)
- Timing Zoom (see page 608)

- State (Synchronous) Analysis Mode (see page 608)
- Timing (Asynchronous) Analysis Mode (see page 611)
- Power Requirements (see page 613)
- Environmental Characteristics (see page 613)

Module Channel Counts

	State Analysis	Timing Analysis
1-card module:	64 data + 4 clocks	68
2-card module:	132 data + 4 clocks	136
3-card module:	200 data + 4 clocks	204
4-card module:	268 data + 4 clocks	272
5-card module:	336 data + 4 clocks	340

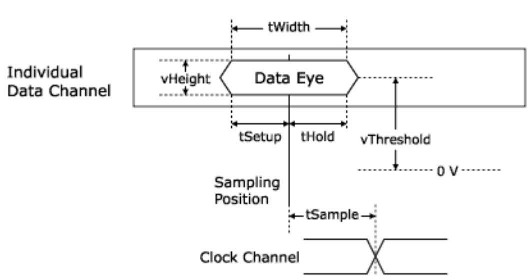
Probes

A probe must be used to connect the logic analyzer to your device under test. For specifications and characteristics of a particular probe, see the documentation that is supplied with your probe or search for the probe's model number at "www.agilent.com".

Timing Zoom

Timing analysis sample rate:	4 GHz
Timing interval accuracy:	Within a pod pair: ±(750 ps + 0.01% of time interval reading) Between pod pairs: ±(1.5 ns + 0.01% of time interval reading)
Memory depth:	64 K
Trigger position:	Start, center, end, or user-defined
Minimum data pulse width:	750 ps

State (Synchronous) Analysis Mode



	300 Mb/s State Mode	600 Mb/s State Mode
tWidth* (see page 611), 1 (see page 611), 2 (see page 611) :	1 ns* (see page 611) , 600 ps typical	1 ns* (see page 611) , 600 ps typical

tSetup:	0.5 tWidth	0.5 tWidth
tHold:	0.5 tWidth	0.5 tWidth
tSample range [3] (see page 611) :	-4 ns to +4 ns	-4 ns to +4 ns
tSample adjustment resolution:	80 ps typical	80 ps typical
tSample accuracy, manual adjustment:	±300 ps	±300 ps [4] (see page 611)
Maximum state data rate on each channel:	300 Mb/s	800 Mb/s
Maximum channels on a single time base and trigger: [5] (see page 611) :	340 - (number of clocks)	306 - (1 clock)
Memory depth [5] (see page 611) :	16753A: 1 M samples 16754A: 4 M samples 16755A: 16 M samples 16756A: 64 M samples	16753A: 1 M samples 16754A: 4 M samples 16755A: 16 M samples 16756A: 64 M samples
Number of independent analyzers [6] (see page 611) :	2	1
Number of clocks [7] (see page 611) :	4	1
Number of clock qualifiers [7] (see page 611) :	4	N/A
Minimum time between active clock edges [*] (see page 611), 8 (see page 611) :	3.33 ns	1.67 ns
Minimum master-to-slave clock time:	1 ns	N/A
Minimum slave-to-master clock time:	1 ns	N/A
Minimum slave-to-slave clock time:	3.33 ns	N/A
Minimum state clock pulse width:	Single edge: 1.0 ns Multiple edge: 1.0 ns	Single edge: 500 ps Multiple edge: 1.67 ns
Clock qualifier setup time:	500 ps	N/A
Clock qualifier hold time:	0	N/A
Time tag resolution [5] (see page 611) :	2 ns	1.5 ns
Maximum time count between stored states:	32 days	32 days

Maximum trigger sequence speed:	300 MHz	600 MHz
Maximum trigger sequence steps:	16	16
Trigger sequence step branching:	Arbitrary 4-way if/then/else	2-way if/then/else
Trigger position:	Start, center, end, or user-defined	Start, center, end, or user-defined
Trigger resources:	• 16 patterns evaluated as =, ≠, >, >=, <, <= • 14 double-bounded ranges evaluated as in range, not in range • 2 timers per card • 2 global counters • 1 occurrence counter per sequence step • 4 flags	• 14 patterns evaluated as =, ≠, >, >=, <, <= • 7 double-bounded ranges evaluated as in range, not in range • 1 occurrence counter per sequence step • 4 flags
Trigger resource conditions:	Arbitrary Boolean combinations	Arbitrary Boolean combinations
Trigger actions:	• Go To • Trigger, send email, and fill memory • Trigger and Go To • Store/don't store sample • Turn on/off default storing • Timer start/stop/pause/resume • Global counter increment/decrement/reset • Occurrence counter reset • Flag set/clear	• Go To • Trigger and fill memory
Store qualification:	Default (global) and per sequence step	Default (global)
Maximum global counter:	2E+24	N/A
Maximum occurrence counter:	2E+24	2E+24
Maximum pattern width:	128 bits	128 bits
Maximum range width:	32 bits	32 bits
Timer value range:	40 ns to 2199 seconds	N/A
Timer resolution:	2 ns	N/A

Timer accuracy:	±(5 ns + 0.01%)	N/A
Timer reset latency:	40 ns	N/A
[*]Items marked with an asterisk (*) are specifications. All others are characteristics. "Typical" represents the average or median value of the parameter based on measurements from a significant number of units. [1]Minimum eye width in system under test. [2]Your choice of probe can limit system bandwidth. Choose a probe rated at 600 Mb/s or greater to maintain system bandwidth. [3]Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes the input to be synchronously sampled coincident with each clock edge. [4]Use of eye finder is recommended in 600 Mb/s state mode. [5]In 300 Mb/s state mode, with all pods assigned, memory depth is half the maximum memory depth. With one pod pair (34 channels) unassigned, the memory depth is full One pod pair (34 channels) must remain unassigned for time tags in 600 Mb/s state mode. [6]Independent analyzers may be either state or timing. When the 600 Mb/s state mode is selected, only one analyzer may be used. [7]In the 300 Mb/s state mode, the total number of clocks and qualifiers is 4. All clock and qualifier inputs must be on the master modules. [8]Tested with input signal Vh = 0.9 V, Vl = -1.7 V, slew rate = 1 V/ns, threshold = -1.3 V. [9]Transitional timing speed and memory depth are halved unless a spare pod pair (34 channels) is unassigned.		

Timing (Asynchronous) Analysis Mode

	Conventional Timing	**Transitional Timing** [9] (see page 611)
Sample rate on all channels:	600 MHz	600 MHz
Sample rate in half channel mode:	1200 MHz	N/A
Number of channels:	68 x (number of cards)	For sample rates <600 MHz: 68 x (number of cards). For 600 MHz sample rate: 68 x (number of cards) - 34.
Maximum channels on a single time base and trigger:	340	340
Number of independent analyzers [6] (see page 611) :	2	2
Sample period (half channel):	833 ps	N/A
Sample period (full channel):	1.67 ns	1.67 ns
Minimum data pulse width:	1 sample period + 500 ps	1 sample period + 500 ps

Time interval accuracy:	±(1 sample period + 1.25 ns + 0.01% of time interval reading)	±(1 sample period + 1.25 ns + 0.01% of time interval reading)
Memory depth in full channel mode:	16753A: 1 M 16754A: 4 M 16755A: 16 M 16756A: 64 M	16753A: 1 M 16754A: 4 M 16755A: 16 M 16756A: 64 M
Memory depth in half channel mode:	16753A: 2 M 16754A: 8 M 16755A: 32 M 16756A: 128 M	N/A
Maximum trigger sequence speed:	300 MHz	300 MHz
Maximum trigger sequence steps:	16	16
Trigger sequence step branching:	Arbitrary 4-way if/then/else	Arbitrary 4-way if/then/else
Trigger position:	Start, center, end, or user-defined	Start, center, end, or user-defined
Trigger resources:	• 16 patterns evaluated as =, ≠, >, >=, <, <= • 14 double-bounded ranges evaluated as in range, not in range • 2 edge/glitch • 2 timers per card • 2 global counters • 1 occurrence counter per sequence step • 4 flags	• 16 patterns evaluated as =, ≠, >, >=, <, <= • 14 double-bounded ranges evaluated as in range, not in range • 3 edge/glitch • 2 timers per card • 2 global counters • 1 occurrence counter per sequence step • 4 flags
Trigger resource conditions:	Arbitrary Boolean combinations	Arbitrary Boolean combinations
Trigger actions:	• Go To • Trigger, send email, and fill memory • Trigger and Go To • Turn on/off default storing • Timer start/stop/pause/resume • Global counter increment/decrement/reset • Occurrence counter reset • Flag set/clear	• Go To • Trigger, send email, and fill memory • Trigger and Go To • Turn on/off default storing • Timer start/stop/pause/resume • Global counter increment/decrement/reset • Occurrence counter reset • Flag set/clear
Maximum global counter:	2E+24	2E+24

Maximum occurrence counter:	2E+24	2E+24
Maximum range width:	32 bits	32 bits
Maximum pattern width:	128 bits	128 bits
Timer value range:	40 ns to 2199 seconds	40 ns to 2199 seconds
Timer resolution:	2 ns	2 ns
Timer accuracy:	±(5 ns + 0.01%)	±(5 ns + 0.01%)
Greater than duration:	3.33 ns to 55 ms in 3.3 ns increments	3.33 ns to 55 ms in 3.3 ns increments
Less than duration:	6.67 ns to 55 ms in 3.3 ns increments	6.67 ns to 55 ms in 3.3 ns increments
Timer reset latency:	40 ns	40 ns

Power Requirements

All necessary power is supplied by the backplane connector of the logic analysis system mainframe.

Environmental Characteristics

Indoor use only.

See individual probe Specifications and Characteristics for probe environmental characteristics.

- Operating Environment (see page 613)
- Non-operating Environment (see page 613)

Operating Environment

Temperature:	0°C to 50°C (+32°F to 122°F). Reliability is enhanced when operating within the following range +20°C to 35°C (+68°F to 95°F).
Humidity:	0 to 80% relative humidity at 40°C (+104°F). Reliability is enhanced when operating within the range 20% to 80% non-condensing.
Altitude:	0 to 3,000 m (10,000 ft)
Vibration:	Random vibration 5-500 Hz, 10 minutes per axis, approximately 0.2 g rms

Non-operating Environment

Temperature:	-40°C to +75°C (-40°F to +167°F). Protect the instrument from temperature extremes which cause condensation on the instrument.
Humidity:	0 to 90% relative humidity at 65°C (149°F)
Altitude:	0 to 15,300 m (50,000 ft)
Vibration (in shipping carton):	Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 2.41 g rms; and swept sine resonant search, 5 to 500 Hz, 0.50 g (0-peak), 5-minute resonant dwell at 4 resonances per axis.

See Also

- What is a Specification (see page 644)
- What is a Characteristic (see page 645)

16760 Logic Analyzer Specifications and Characteristics

Describes the specifications and characteristics of the 16760 logic analyzer.

NOTE Items marked with an asterisk (*) are specifications. All others are characteristics.

- Module Channel Counts (see page 614)
- Probes (see page 614)
- State (Synchronous) Analysis Mode (see page 614)
- Timing (Asynchronous) Analysis Mode (see page 619)
- Power Requirements (see page 621)
- Environmental Characteristics (see page 621)

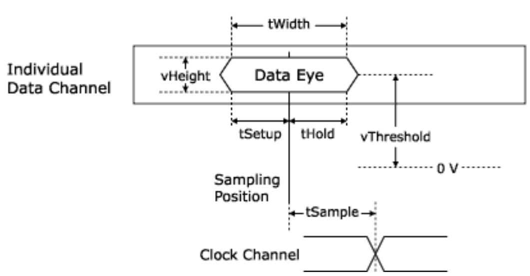
Module Channel Counts

	State Analysis	Timing Analysis
1-card module:	32 data + 2 clocks	34
2-card module:	66 data + 2 clocks	68
3-card module:	100 data + 2 clocks	102
4-card module:	134 data + 2 clocks	136
5-card module:	168 data + 2 clocks	170

Probes

A probe must be used to connect the logic analyzer to your device under test. For specifications and characteristics of a particular probe, see the documentation that is supplied with your probe or search for the probe's model number at "www.agilent.com".

State (Synchronous) Analysis Mode



Specifications for Each Input

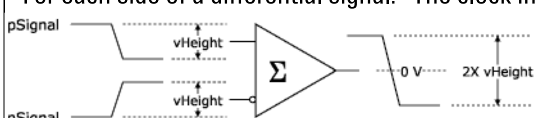
	800, 1250, 1500 Mb/s Modes	200, 400 Mb/s Modes	Description/Notes
Minimum tWidth (data to clock):	500 ps	1.25 ns	Eye width in system under test. [2] (see page 615)
Minimum tSetup (data to clock):	250 ps	625 ps	Data setup time required before tSample.
Minimum tHold (data to clock):	250 ps	625 ps	Data hold time required after tSample.
Minimum vHeight [1] (see page 615) (all inputs):	100 mV	100 mV	E5379A 100-pin differential probe. [3] (see page 615)
	250 mV	250 mV	E5378A 100-pin single-ended probe [4] (see page 615), E5382A single-ended flying-lead probe set
	300 mV	300 mV	E5380A 38-pin single-ended probe

[*]All specifications noted by an asterisk are the performance standards against which the product is tested.

[1]The analyzer can be configured to sample on the rising edge, the falling edge, or both edges of the clock. If both edges are used with a single-ended clock input, take care to set the clock threshold accurately to avoid phase error.

[2]Eye width and height are specified at the probe tip. Eye width as measured by eye finder in the analyzer may be less, and still sample reliably.

[3]For each side of a differential signal: [4]The clock inputs in the E5378A probe and the E5382A



probe set may be connected differentially or single ended. Use the E5379A probe vHeight specification for clock channel(s) connected differentially.

User Adjustable Settings for Each Input

	Adjustment Range				
	1500 Mb/s State Mode	1250 Mb/s State Mode	800 Mb/s State Mode	400 Mb/s State Mode	200 Mb/s State Mode

tSample [5] (see page 616) (data to clock):	0 ns to +4 ns, 10 ps resolution	-2.5 ns to +2.5 ns, 10 ps resolution	-2.5 ns to +2.5 ns, 10 ps resolution	-3.2 ns to +3.2 ns, 100 ps resolution	-3.5 ns to +3 ns, 100 ps resolution
vThreshold [6] (see page 616) (all inputs):	-3 V to +5 V, 10 mV resolution	-3 V to +5 V, 10 mV resolution	-3 V to +5 V, 10 mV resolution	-3 V to +5 V, 10 mV resolution	-3 V to +5 V, 10 mV resolution
[5]Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes synchronous sampling coincident with each active clock edge. [6]Threshold applies to single-ended input signals. Thresholds are independently adjustable for the clock input of each pod and for each set of 16 data inputs for each pod. Threshold limits apply to both the internal reference and to the external reference input on the E5378A probe.					

Synchronous State Analysis

	1500 Mb/s State Mode	**1250 Mb/s State Mode**	**800 Mb/s State Mode**	**400 Mb/s State Mode**	**200 Mb/s State Mode**
Maximum data rate on each channel 9 (see page 619).	1.5 Gb/s	1.25 Gb/s	800 Mb/s	400 Mb/s	200 Mb/s
Minimum clock interval, active edge to active edge * (see page 619), 9 (see page 619).	667 ps	800 ps	1.25 ns	2.5 ns	5 ns
Minimum state clock pulse width with clock polarity rising or falling 9 (see page 619).	N/A	N/A	600 ps	1.5 ns	1.5 ns
Clock periodicity:	Clock must be periodic	Clock must be periodic	Periodic or aperiodic	Periodic or aperiodic	Periodic or aperiodic
Number of clocks:	1	1	1	1	1
Clock polarity:	Both edges	Both edges	Rising, falling, or both	Rising, falling, or both	Rising, falling, or both

Minimum data pulse width * (see page 619).	600 ps	750 ps	E5378A, E5379A, E5382A probes: 750 ps E5380A probe: 1.5 ns	1.5 ns	1.5 ns
Number of channels [7] (see page 619).	16 x (number of cards) - 8	16 x (number of cards) - 8	34 x (number of cards) - 16	34 x (number of cards) - 16	34 x (number of cards)
Maximum channels on a single time base and trigger:	72 (5 cards)	72 (5 cards)	154 (5 cards)	154 (5 cards)	170 (5 cards)
Maximum memory depth:	128 M samples	128 M samples	64 M samples	32 M samples	32 M samples
Time tag resolution:	4 ns [8] (see page 619)	4 ns [8] (see page 619)	4 ns [8] (see page 619)	4 ns [8] (see page 619)	4 ns
Maximum time count between states:	17 seconds	17 seconds	17 seconds	17 seconds	17 seconds
Trigger resources:	• 3 patterns evaluated as =, ≠, >, >=, <, <= on one pod; or evaluated as =, ≠ across multiple pods; or 1 ranges on each pod • 4 flags • Arm in	• 3 patterns evaluated as =, ≠, >, >=, <, <= on one pod; or evaluated as =, ≠ across multiple pods; or 1 ranges on each pod • 4 flags • Arm in	• 4 patterns evaluated as =, ≠, >, >=, <, <= on one pod; or evaluated as =, ≠ across multiple pods; or 2 ranges on each pod • 4 flags • Arm in	• 8 patterns evaluated as =, ≠, >, >=, <, <= • 4 ranges evaluated as in range, not in range • 2 occurrence counters • 4 flags • Arm in	• 16 patterns evaluated as =, ≠, >, >=, <, <= • 15 ranges evaluated as in range, not in range • 2 timers per card - 1 • 2 global counters • 1 occurrence counter per sequence step • 4 flags • Arm in

Trigger actions:	• Trigger and fill memory	• Trigger and fill memory	• Trigger and fill memory	• Go To • Trigger and fill memory	• Go To • Trigger, send email, and fill memory • Trigger and Go To • Store/don't store sample • Turn on/off default storing • Timer start/stop /pause/re sume • Global counter increment /reset • Occurrence counter reset • Flag set/clear
Maximum trigger sequence steps:	2	2	4	16	16
Maximum trigger sequence speed:	1.5 Gb/s	1.25 Gb/s	800 MHz	400 MHz	200 MHz
Store qualification:	Default	Default	Default	Default	Default and per sequence step
Maximum global counter:	N/A	N/A	N/A	N/A	16,777,215
Maximum occurrence counter:	N/A	N/A	N/A	N/A	16,777,215
Maximum pattern/rang e term width:	32 bits [10] (see page 619)	32 bits [10] (see page 619)	32 bits [10] (see page 619)	32 bits [10] (see page 619)	32 bits [10] (see page 619)

Timer value range:	N/A	N/A	N/A	N/A	100 ns to 4397 seconds
Timer resolution:	N/A	N/A	N/A	N/A	4 ns
Timer accuracy:	N/A	N/A	N/A	N/A	±(10 ns + 0.01%)
Timer reset latency:	N/A	N/A	N/A	N/A	65 ns
Data in to BNC port out delay latency:	150 ns	150 ns	150 ns	150 ns	150 ns
Flag set/reset to evaluation latency:	N/A	N/A	N/A	N/A	110 ns

[*]All specifications noted by an asterisk are the performance standards against which the product is tested.
[7]In 1.25 Gb/s and 1.5 Gb/s modes, only the even numbered channels (0, 2, 4, etc.) are acquired.
[8]The resolution of the hardware used to assign time tags is 4 ns. Times of intermediate states are calculated.
[9]The choice of probe can limit system performance. Select a probe rated at the speed of the selected mode (or greater) to maintain system bandwidth.
[10]Maximum bus/signal width is 32 bits. Wider patterns can be created by "Anding" multiple bus/signals together.

Timing (Asynchronous) Analysis Mode

	Conventional Timing	Transitional Timing
Maximum timing analysis sample rate:	800 MHz	400 MHz
Number of channels:	34 x (number of cards)	For sample rates <400 MHz: 34 x (number of cards). For sample rates =400 MHz: 34 x (number of cards) - 17 [11] (see page 621).
Maximum channels on a single time base and trigger:	170 (5 cards)	170 (5 cards)
Sample period:	1.25 ns	2.5 ns to 1 ms [11] (see page 621)
Memory depth:	64 M samples	32 M samples [11] (see page 621)
Sample period accuracy:	±(250 ps + 0.01% of sample period)	±(250 ps + 0.01% of sample period)
Channel-to-channel skew:	<1.5 ns	<1.5 ns

Time interval accuracy:	±[sample period + (channel-to-channel skew) + (0.01% of time interval)]	±[sample period + (channel-to-channel skew) + (0.01% of time interval)]
Minimum data pulse width:	1.5 ns for data capture 5.1 ns for trigger sequencing	3.8 ns for data capture 5.1 ns for trigger sequencing
Maximum trigger sequence speed:	200 MHz	200 MHz
Trigger resources:	• 16 patterns evaluated as =, ≠, >, >=, <, <= • 15 ranges evaluated as in range, not in range • 2 edge/glitch • (2 timers per card) - 1 • 2 global counters • 1 occurrence counter per sequence step • 4 flags, arm in	• 16 patterns evaluated as =, ≠, >, >=, <, <= • 15 ranges evaluated as in range, not in range • 2 edge/glitch • (2 timers per card) - 1 • 2 global counters • 1 occurrence counter per sequence step • 4 flags, arm in
Trigger resource conditions:	Arbitrary Boolean combinations	Arbitrary Boolean combinations
Trigger actions:	• Go To • Trigger, send email, and fill memory • Trigger and Go To • Turn on/off default storing • Timer start/stop/pause/resume • Global counter increment/decrement/reset • Occurrence counter reset • Flag set/clear	• Go To • Trigger, send email, and fill memory • Trigger and Go To • Turn on/off default storing • Timer start/stop/pause/resume • Global counter increment/decrement/reset • Occurrence counter reset • Flag set/clear
Maximum global counter:	16,777,215	16,777,215
Maximum occurrence counter:	16,777,215	16,777,215
Timer value range:	100 ns to 4397 seconds	100 ns to 4397 seconds
Timer resolution:	4 ns	4 ns
Timer accuracy:	±(10 ns + 0.01%)	±(10 ns + 0.01%)
Greater than duration:	5 ns to 83 ms in 5 ns increments	5 ns to 83 ms in 5 ns increments
Less than duration:	10 ns to 83 ms in 5 ns increments	10 ns to 83 ms in 5 ns increments
Timer reset latency:	60 ns	60 ns

Data in to BNC port out delay latency:	150 ns	150 ns
Flag set/reset to evaluation latency:	110 ns	110 ns
[11]With all pods assigned in transitional/store qualified timing, minimum sample period is 5 ns and maximum memory depth is 16 M samples.		

Power Requirements

All necessary power is supplied by the backplane connector of the logic analysis system mainframe.

Environmental Characteristics

Indoor use only.

See individual probe Specifications and Characteristics for probe environmental characteristics.

Operating Environment

Temperature:	0°C to 45°C (+32°F to 113°F).

See Also

- What is a Specification (see page 644)
- What is a Characteristic (see page 645)

16800-Series Logic Analyzer Specifications and Characteristics

Describes the specifications and characteristics of the 16800-series logic analyzers.

NOTE

Items marked with an asterisk (*) are specifications. All others are characteristics.

"Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

- Channel Count per Measurement Mode (see page 622)
- Probes (see page 622)
- Timing Zoom (see page 622)
- Other (see page 622)
- State (Synchronous) Analysis Mode (see page 623)
- Timing (Asynchronous) Analysis Mode (see page 625)
- General Information (see page 627)
- Environmental Characteristics (see page 628)

Channel Count per Measurement Mode

	16801A/ 16821A	16802A/ 16822A	16803A/ 16823A	16804A	16806A
State analysis [11] (see page 622).	32 data + 2 clocks	64 data + 4 clocks	98 data + 4 clocks	132 data + 4 clocks	200 data + 4 clocks
Conventional timing:	34	68	102	136	204
Transitional timing for sample rates < 500 MHz:	34	68	102	136	204
Transitional timing for 500 MHz sample rate:	—	34	68	102	170
[11]Unused clock channels can be used as data channels.					

Probes

A probe must be used to connect the logic analyzer to your device under test. For specifications and characteristics of a particular probe, see the documentation that is supplied with your probe or search for the probe's model number at "www.agilent.com".

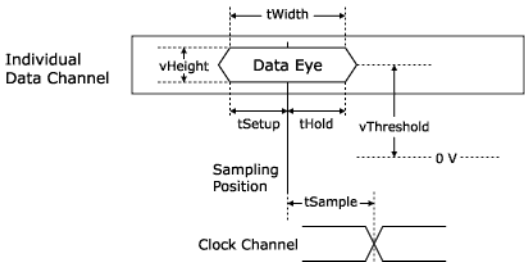
Timing Zoom

Timing analysis sample rate:	4 GHz (250 ps sample period)
Timing interval accuracy:	Within a pod pair: ±(1 ns + 0.01% of time interval reading) Between pod pairs: ±(1.75 ns + 0.01% of time interval reading)
Memory depth:	64 K
Trigger position:	Start, center, end, or user-defined
Minimum data pulse width:	1 ns

Other

Voltage threshold:	-5 V to 5 V (10 mV increments)
Threshold accuracy:	±50 mV + 1% of setting

State (Synchronous) Analysis Mode



	Option 250	Option 500 10 (see page 625)
tWidth* (see page 625), 1 (see page 625) :	1.5 ns* (see page 625) ("latest data sheet")	1.5 ns* (see page 625) ("latest data sheet")
tSetup:	0.5 tWidth	0.5 tWidth
tHold:	0.5 tWidth	0.5 tWidth
tSample range 2 (see page 625) :	-3.2 ns to +3.2 ns	-3.2 ns to +3.2 ns
tSample adjustment resolution:	80 ps typical	80 ps typical
Maximum state data rate on each channel:	250 Mb/s	500 Mb/s
Memory depth 4 (see page 625) :	Option 001: 1 M samples Option 004: 4 M samples Option 016: 16 M samples Option 032: 32 M samples	Option 001: 1 M samples Option 004: 4 M samples Option 016: 16 M samples Option 032: 32 M samples
Number of independent analyzers 5 (see page 625) :	2 (1 for 16801A or 16821A)	1
Number of clocks 6 (see page 625) :	4 (2 for 16801A or 16821A)	1
Number of clock qualifiers 6 (see page 625) :	4 (2 for 16801A or 16821A)	N/A
Minimum time between active clock edges* (see page 625), 7 (see page 625) :	4.0 ns	2.0 ns
Minimum master-to-slave clock time:	1 ns	N/A
Minimum slave-to-master clock time:	1 ns	N/A
Minimum slave-to-slave clock time:	4.0 ns	N/A
Minimum state clock pulse width:	Single edge: 1.0 ns Multiple edge: 1.0 ns	Single edge: 1.0 ns Multiple edge: 2.0 ns

Clock qualifier setup time:	500 ps	N/A
Clock qualifier hold time:	0	N/A
Time tag resolution:	2 ns	1.5 ns
Maximum time count between stored states:	32 days	32 days
Maximum trigger sequence speed:	250 MHz	500 MHz
Maximum trigger sequence steps:	16	16
Trigger sequence step branching:	Arbitrary 4-way if/then/else	2-way if/then/else
Trigger position:	Start, center, end, or user-defined	Start, center, end, or user-defined
Trigger resources:	• 16 patterns evaluated as =, ≠, >, >=, <, <= • 14 double-bounded ranges evaluated as in range, not in range • 1 timer for every 34 channels • 2 global counters • 1 occurrence counter per sequence step • 4 flags	• 14 patterns evaluated as =, ≠, >, >=, <, <= • 7 double-bounded ranges evaluated as in range, not in range • 1 occurrence counter per sequence step • 4 flags
Trigger resource conditions:	Arbitrary Boolean combinations	Arbitrary Boolean combinations
Trigger actions:	• Go To • Trigger, send email, and fill memory • Trigger and Go To • Store/don't store sample • Turn on/off default storing • Timer start/stop/pause/resume • Global counter increment/decrement/reset • Occurrence counter reset • Flag set/clear	• Go To • Trigger and fill memory
Store qualification:	Default (global) and per sequence step	Default (global)
Maximum global counter:	2E+24	N/A

Maximum occurrence counter:	2E+24	2E+24
Maximum pattern width:	Smaller of 128 bits or maximum number of channels	Smaller of 128 bits or maximum number of channels
Maximum range width:	Smaller of 64 bits or maximum number of channels	Smaller of 64 bits or maximum number of channels
Timer value range:	60 ns to 2199 seconds	N/A
Timer resolution:	2 ns	N/A
Timer accuracy:	±(5 ns + 0.01%)	N/A
Timer reset latency:	60 ns	N/A

[*]Items marked with an asterisk (*) are specifications. All others are characteristics. "Typical" represents the average or median value of the parameter based on measurements from a significant number of units.
[1]Minimum eye width in system under test.
[2]Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes the input to be synchronously sampled coincident with each clock edge.
[3]Use of eye finder is recommended in 500 Mb/s state mode.
[4]In 250 Mb/s state mode, with all pods assigned, memory depth is half the maximum memory depth. With one pod pair (34 channels) unassigned, the memory depth is full One pod pair (34 channels) must remain unassigned for time tags in 500 Mb/s state mode.
[5]Independent analyzers may be either state or timing. When the 500 Mb/s state mode is selected, only one analyzer may be used.
[6]In the 250 Mb/s state mode, the total number of clocks and qualifiers is 4. All clock and qualifier inputs must be on the master modules.
[7]Tested with input signal Vh = 1.25 V, Vl = 0.75 V, threshold = 1.0 V, tr/tf = 180 ps ±30 ps (10%, 90%).
[8]Transitional timing speed and memory depth are halved unless a spare pod pair (34 channels) is unassigned.
[9]For sample rates <500 MHz. For 500 MHz sample, subtract 34 channels.
[10]This option is not available for the 16801A and 16821A 34-channel logic analyzer models.

Timing (Asynchronous) Analysis Mode

	Conventional Timing	**Transitional Timing** [8] (see page 625)
Sample rate on all channels:	500 MHz	500 MHz
Sample rate in half channel mode:	1 GHz	N/A
Number of independent analyzers [5] (see page 625) :	2 (1 for 16801A or 16821A)	2 (1 for 16801A or 16821A)
Sample period (half channel):	1.0 ns	N/A

Sample period (full channel):	2.0 ns	2.0 ns
Minimum data pulse width:	1 sample period + 1.0 ns	1 sample period + 1.0 ns
Time interval accuracy:	±(1 sample period + 1.25 ns + 0.01% of time interval reading)	±(1 sample period + 1.25 ns + 0.01% of time interval reading)
Memory depth in full channel mode:	Option 001: 1 M Option 004: 4 M Option 016: 16 M Option 032: 32 M	Option 001: 1 M Option 004: 4 M Option 016: 16 M Option 032: 32 M
Memory depth in half channel mode:	Option 000: 512 K Option 001: 2 M Option 004: 8 M Option 016: 32 M Option 032: 64 M	N/A
Maximum trigger sequence speed:	250 MHz	250 MHz
Maximum trigger sequence steps:	16	16
Trigger sequence step branching:	Arbitrary 4-way if/then/else	Arbitrary 4-way if/then/else
Trigger position:	Start, center, end, or user-defined	Start, center, end, or user-defined
Trigger resources:	• 16 patterns evaluated as =, ≠, >, >=, <, <= • 14 double-bounded ranges evaluated as in range, not in range • 3 edge/glitch • 1 timer for every 34 channels • 2 global counters • 1 occurrence counter per sequence step • 4 flags	• 15 patterns evaluated as =, ≠, >, >=, <, <= • 14 double-bounded ranges evaluated as in range, not in range • 3 edge/glitch • 1 timer for every 34 channels • 2 global counters • 1 occurrence counter per sequence step • 4 flags
Trigger resource conditions:	Arbitrary Boolean combinations	Arbitrary Boolean combinations

Trigger actions:	• Go To • Trigger, send email, and fill memory • Trigger and Go To • Turn on/off default storing • Timer start/stop/pause/resume • Global counter increment/decrement/reset • Occurrence counter reset • Flag set/clear	• Go To • Trigger, send email, and fill memory • Trigger and Go To • Turn on/off default storing • Timer start/stop/pause/resume • Global counter increment/decrement/reset • Occurrence counter reset • Flag set/clear
Maximum global counter:	2E+24	2E+24
Maximum occurrence counter:	2E+24	2E+24
Maximum range width:	32 bits	32 bits
Maximum pattern width:	Smaller of 128 bits or maximum number of channels	Smaller of 128 bits or maximum number of channels
Timer value range:	60 ns to 2199 seconds	60 ns to 2199 seconds
Timer resolution:	2 ns	2 ns
Timer accuracy:	±(5 ns + 0.01%)	±(5 ns + 0.01%)
Greater than duration:	4.0 ns to 67 ms in 4.0 ns increments	4.0 ns to 67 ms in 4.0 ns increments
Less than duration:	8.0 ns to 67 ms in 4.0 ns increments	8.0 ns to 67 ms in 4.0 ns increments
Timer reset latency:	60 ns	60 ns

General Information

Power:

16801A, 16802A, 16803A: 115/230 V, 48 to 66 Hz, 615 W max.

16804A, 16806A, 16821A, 16822A, 16823A: 115/230 V, 48 to 66 Hz, 775 W max.

Dimensions:

288.22 mm height (11.347 in), 443.23 mm width (17.450 in), 330.32 mm depth (13.005 in)

Weight:

	Max Net	Max Shipping
16801A:	12.9 kg (28.5 lbs)	19.7 kg (43.5 lbs)

16802A:	13.2 kg (28.9 lbs)	19.9 kg (43.9 lbs)
16803A:	13.7 kg (30.3 lbs)	20.5 kg (45.3 lbs)
16804A:	14.2 kg (31.3 lbs)	21.0 kg (46.3 lbs)
16806A:	14.6 kg (32.1 lbs)	21.4 kg (47.1 lbs)
16821A:	14.2 kg (31.2 lbs)	20.9 kg (46.2 lbs)
16822A:	14.2 kg (31.6 lbs)	21.1 kg (46.6 lbs)
16823A:	14.5 kg (32.0 lbs)	21.3 kg (47.0 lbs)

User interface:

Windows® XP Professional

Printers:

Can print to any local or network printer supported by Windows® XP Professional.

Environmental Characteristics

Indoor use only.

See individual probe Specifications and Characteristics for probe environmental characteristics.

- Operating Environment (see page 628)

Operating Environment

Temperature:	0°C to 50°C (+32°F to 122°F).
Humidity:	0 to 80% relative humidity at 40°C (+104°F).
Altitude:	0 to 3,000 m (10,000 ft)

See Also

- What is a Specification (see page 644)
- What is a Characteristic (see page 645)

16910/11 Logic Analyzer Specifications and Characteristics

Describes the specifications and characteristics of the 16910/11 logic analyzer.

NOTE

Items marked with an asterisk (*) are specifications. All others are characteristics.

"Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

- Module Channel Counts (see page 629)

- Probes (see page 629)
- Timing Zoom (see page 629)
- State (Synchronous) Analysis Mode (see page 630)
- Timing (Asynchronous) Analysis Mode (see page 633)
- Power Requirements (see page 635)
- Environmental Characteristics (see page 635)

Module Channel Counts

	State Analysis 16910A	State Analysis 16911A	Timing Analysis 16910A	Timing Analysis 16911A
1-card module:	98 data + 4 clocks	64 data + 4 clocks	102	68
2-card module:	200 data + 4 clocks	132 data + 4 clocks	204	136
3-card module:	302 data + 4 clocks	200 data + 4 clocks	306	204
4-card module:	404 data + 4 clocks	268 data + 4 clocks	408	272
5-card module:	506 data + 4 clocks	336 data + 4 clocks	510	340

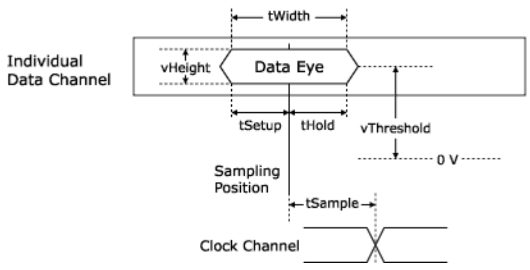
Probes

A probe must be used to connect the logic analyzer to your device under test. For specifications and characteristics of a particular probe, see the documentation that is supplied with your probe or search for the probe's model number at "www.agilent.com".

Timing Zoom

Timing analysis sample rate:	4 GHz
Timing interval accuracy:	Within a pod pair: ±(1 ns + 0.01% of time interval reading) Between pod pairs: ±(1.75 ns + 0.01% of time interval reading)
Memory depth:	64 K
Trigger position:	Start, center, end, or user-defined
Minimum data pulse width:	1 ns

State (Synchronous) Analysis Mode



	Option 250	Option 500
tWidth* (see page 633), 1 (see page 633) :	1.5 ns* (see page 633) ("latest data sheet")	1.5 ns* (see page 633) ("latest data sheet")
tSetup:	0.5 tWidth	0.5 tWidth
tHold:	0.5 tWidth	0.5 tWidth
tSample range 2 (see page 633) :	-3.2 ns to +3.2 ns	-3.2 ns to +3.2 ns
tSample adjustment resolution:	80 ps typical	80 ps typical
Maximum state data rate on each channel:	250 Mb/s	500 Mb/s
Number of channels on a single time base and trigger 4 (see page 633) :	16910A: 510 - (number of clocks) 16911A: 340 - (number of clocks)	16910A: 510 - (number of clocks) 16911A: 340 - (number of clocks)
Memory depth 4 (see page 633) :	Option 256: 256 K samples Option 001: 1 M samples Option 004: 4 M samples Option 016: 16 M samples Option 032: 32 M samples	Option 256: 256 K samples Option 001: 1 M samples Option 004: 4 M samples Option 016: 16 M samples Option 032: 32 M samples
Number of independent analyzers 5 (see page 633) :	2	1
Number of clocks 6 (see page 633) :	4	1
Number of clock qualifiers 6 (see page 633) :	4	N/A
Minimum time between active clock edges* (see page 633), 7 (see page 633) :	4.0 ns	2.0 ns
Minimum master-to-slave clock time:	1 ns	N/A

Minimum slave-to-master clock time:	1 ns	N/A
Minimum slave-to-slave clock time:	4.0 ns	N/A
Minimum state clock pulse width:	Single edge: 1.0 ns Multiple edge: 1.0 ns	Single edge: 1.0 ns Multiple edge: 2.0 ns
Clock qualifier setup time:	500 ps	N/A
Clock qualifier hold time:	0	N/A
Time tag resolution:	2 ns	1.5 ns
Maximum time count between stored states:	32 days	32 days
Maximum trigger sequence speed:	250 MHz	500 MHz
Maximum trigger sequence steps:	16	16
Trigger sequence step branching:	Arbitrary 4-way if/then/else	2-way if/then/else
Trigger position:	Start, center, end, or user-defined	Start, center, end, or user-defined
Trigger resources:	• 16 patterns evaluated as =, ≠, >, >=, <, <= • 14 double-bounded ranges evaluated as in range, not in range • 1 timer for every 34 channels • 2 global counters • 1 occurrence counter per sequence step • 4 flags	• 14 patterns evaluated as =, ≠, >, >=, <, <= • 7 double-bounded ranges evaluated as in range, not in range • 1 occurrence counter per sequence step • 4 flags
Trigger resource conditions:	Arbitrary Boolean combinations	Arbitrary Boolean combinations

Trigger actions:	• Go To • Trigger, send email, and fill memory • Trigger and Go To • Store/don't store sample • Turn on/off default storing • Timer start/stop/pause/resume • Global counter increment/decrement/reset • Occurrence counter reset • Flag set/clear	• Go To • Trigger and fill memory
Store qualification:	Default (global) and per sequence step	Default (global)
Maximum global counter:	2E+24	N/A
Maximum occurrence counter:	2E+24	2E+24
Maximum pattern width:	128 bits	128 bits
Maximum range width:	64 bits	64 bits
Timer value range:	60 ns to 2199 seconds	N/A
Timer resolution:	2 ns	N/A
Timer accuracy:	±(5 ns + 0.01%)	N/A

Timer reset latency:	60 ns	N/A

[*]Items marked with an asterisk (*) are specifications. All others are characteristics. "Typical" represents the average or median value of the parameter based on measurements from a significant number of units.
[1]Minimum eye width in system under test.
[2]Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes the input to be synchronously sampled coincident with each clock edge.
[3]Use of eye finder is recommended in 500 Mb/s state mode.
[4]In 250 Mb/s state mode, with all pods assigned, memory depth is half the maximum memory depth. With one pod pair (34 channels) unassigned, the memory depth is full One pod pair (34 channels) must remain unassigned for time tags in 500 Mb/s state mode.
[5]Independent analyzers may be either state or timing. When the 500 Mb/s state mode is selected, only one analyzer may be used.
[6]In the 250 Mb/s state mode, the total number of clocks and qualifiers is 4. All clock and qualifier inputs must be on the master modules.
[7]Tested with input signal Vh = 1.25 V, Vl = 0.75 V, threshold = 1.0 V,
tr/tf = 180 ps ±30 ps (10%, 90%).
[8]Transitional timing speed and memory depth are halved unless a spare pod pair (34 channels) is unassigned.

Timing (Asynchronous) Analysis Mode

	Conventional Timing	**Transitional Timing** [8] (see page 633)
Sample rate on all channels:	500 MHz	500 MHz
Sample rate in half channel mode:	1000 MHz	N/A
Number of channels:	16910A: 102 x (number of cards)	16910A: For sample rates <500 MHz: 102 x (number of cards). For 500 MHz sample rate: 102 x (number of cards) - 34.
	16911A: 68 x (number of cards)	16911A: For sample rates <500 MHz: 68 x (number of cards). For 500 MHz sample rate: 68 x (number of cards) - 34.
Maximum channels on a single time base and trigger:	16910A: 510 16911A: 340	16910A: 510 16911A: 340
Number of independent analyzers [5] (see page 633) :	2	2
Sample period (half channel):	1.0 ns	N/A

Sample period (full channel):	2.0 ns	2.0 ns
Minimum data pulse width:	1 sample period + 1.0 ns	1 sample period + 1.0 ns
Time interval accuracy:	±(1 sample period + 1.25 ns + 0.01% of time interval reading)	±(1 sample period + 1.25 ns + 0.01% of time interval reading)
Memory depth in full channel mode:	Option 256: 256 K Option 001: 1 M Option 004: 4 M Option 016: 16 M Option 032: 32 M	Option 256: 256 K Option 001: 1 M Option 004: 4 M Option 016: 16 M Option 032: 32 M
Memory depth in half channel mode:	Option 000: 512 K Option 001: 2 M Option 004: 8 M Option 016: 32 M Option 032: 64 M	N/A
Maximum trigger sequence speed:	250 MHz	250 MHz
Maximum trigger sequence steps:	16	16
Trigger sequence step branching:	Arbitrary 4-way if/then/else	Arbitrary 4-way if/then/else
Trigger position:	Start, center, end, or user-defined	Start, center, end, or user-defined
Trigger resources:	• 16 patterns evaluated as =, ≠, >, >=, <, <= • 14 double-bounded ranges evaluated as in range, not in range • 3 edge/glitch • 1 timer for every 34 channels • 2 global counters • 1 occurrence counter per sequence step • 4 flags	• 15 patterns evaluated as =, ≠, >, >=, <, <= • 14 double-bounded ranges evaluated as in range, not in range • 3 edge/glitch • 1 timer for every 34 channels • 2 global counters • 1 occurrence counter per sequence step • 4 flags
Trigger resource conditions:	Arbitrary Boolean combinations	Arbitrary Boolean combinations

Trigger actions:	• Go To • Trigger, send email, and fill memory • Trigger and Go To • Turn on/off default storing • Timer start/stop/pause/resume • Global counter increment/decrement/reset • Occurrence counter reset • Flag set/clear	• Go To • Trigger, send email, and fill memory • Trigger and Go To • Turn on/off default storing • Timer start/stop/pause/resume • Global counter increment/decrement/reset • Occurrence counter reset • Flag set/clear
Maximum global counter:	2E+24	2E+24
Maximum occurrence counter:	2E+24	2E+24
Maximum range width:	32 bits	32 bits
Maximum pattern width:	128 bits	128 bits
Timer value range:	60 ns to 2199 seconds	60 ns to 2199 seconds
Timer resolution:	2 ns	2 ns
Timer accuracy:	±(5 ns + 0.01%)	±(5 ns + 0.01%)
Greater than duration:	4.0 ns to 67 ms in 4.0 ns increments	4.0 ns to 67 ms in 4.0 ns increments
Less than duration:	8.0 ns to 67 ms in 4.0 ns increments	8.0 ns to 67 ms in 4.0 ns increments
Timer reset latency:	60 ns	60 ns

Power Requirements

All necessary power is supplied by the backplane connector of the logic analysis system mainframe.

Environmental Characteristics

Indoor use only.

See individual probe Specifications and Characteristics for probe environmental characteristics.

- Operating Environment (see page 635)
- Non-operating Environment (see page 636)

Operating Environment

Temperature:	0°C to 40°C (+32°F to 104°F) when operating in a 16900A or 16902A mainframe. 0°C to 50°C (+32°F to 122°F) when operating in a 16901A or 16903A mainframe.
Humidity:	0 to 80% relative humidity at 40°C (+104°F). Reliability is enhanced when operating within the range 20% to 80% non-condensing.

Altitude:	0 to 3,000 m (10,000 ft)
Vibration:	Random vibration 5-500 Hz, 10 minutes per axis, approximately 0.2 g rms

Non-operating Environment

Temperature:	-40°C to +75°C (-40°F to +167°F). Protect the instrument from temperature extremes which cause condensation on the instrument.
Humidity:	0 to 90% relative humidity at 65°C (149°F)
Altitude:	0 to 15,300 m (50,000 ft)
Vibration (in shipping carton):	Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 2.41 g rms; and swept sine resonant search, 5 to 500 Hz, 0.50 g (0-peak), 5-minute resonant dwell at 4 resonances per axis.

See Also

- What is a Specification (see page 644)
- What is a Characteristic (see page 645)

16950/51 Logic Analyzer Specifications and Characteristics

Describes the specifications and characteristics of the 16950/51 logic analyzer.

NOTE

Items marked with an asterisk (*) are specifications. All others are characteristics.

"Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

- Module Channel Counts (see page 636)
- Probes (see page 637)
- Timing Zoom (see page 637)
- State (Synchronous) Analysis Mode (see page 637)
- Timing (Asynchronous) Analysis Mode (see page 640)
- Power Requirements (see page 642)
- Environmental Characteristics (see page 642)

Module Channel Counts

	State Analysis	Timing Analysis
1-card module:	64 data + 4 clocks	68
2-card module:	132 data + 4 clocks	136
3-card module:	200 data + 4 clocks	204

4-card module:	268 data + 4 clocks	272
5-card module:	336 data + 4 clocks	340

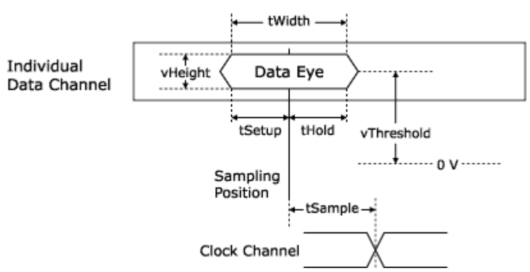
Probes

A probe must be used to connect the logic analyzer to your device under test. For specifications and characteristics of a particular probe, see the documentation that is supplied with your probe or search for the probe's model number at "www.agilent.com".

Timing Zoom

Timing analysis sample rate:	4 GHz
Timing interval accuracy:	Within a pod pair: ±(750 ps + 0.01% of time interval reading) Between pod pairs: ±(1.5 ns + 0.01% of time interval reading)
Memory depth:	64 K
Trigger position:	Start, center, end, or user-defined
Minimum data pulse width:	750 ps

State (Synchronous) Analysis Mode



	300 Mb/s State Mode	600 Mb/s State Mode (16950A) 667 Mb/s State Mode (16950B, 16951B)
tWidth[*] (see page 640), [1] (see page 640), [2] (see page 640) :	16950A: 1 ns[*] (see page 640) , 600 ps typical 16950B: 850 ps[*] (see page 640) , 550 ps typical 16951B: 850 ps[*] (see page 640) , 550 ps typical	16950A: 1 ns[*] (see page 640) , 600 ps typical 16950B: 850 ps[*] (see page 640) , 550 ps typical 16951B: 850 ps[*] (see page 640) , 550 ps typical
tSetup:	0.5 tWidth	0.5 tWidth
tHold:	0.5 tWidth	0.5 tWidth
tSample range [3] (see page 640) :	-4 ns to +4 ns	-4 ns to +4 ns

tSample adjustment resolution:	80 ps typical	80 ps typical
tSample accuracy, manual adjustment:	±300 ps	±300 ps [4] (see page 640)
Maximum state data rate on each channel:	300 Mb/s	16950A: 800 Mb/s 16950B: 1066 Mb/s 16951B: 1066 Mb/s
Maximum channels on a single time base and trigger: [5] (see page 640) :	340 - (number of clocks)	306 - (1 clock)
Memory depth [5] (see page 640) :	Option 256: 256 K samples [10] (see page 640) Option 001: 1 M samples Option 004: 4 M samples Option 016: 16 M samples Option 032: 32 M samples Option 064: 64 M samples 16951B: 256 M samples	Option 256: 256 K samples [10] (see page 640) Option 001: 1 M samples Option 004: 4 M samples Option 016: 16 M samples Option 032: 32 M samples Option 064: 64 M samples 16951B: 256 M samples
Number of independent analyzers [6] (see page 640) :	2	1
Number of clocks [7] (see page 640) :	4	1
Number of clock qualifiers [7] (see page 640) :	4	N/A
Minimum time between active clock edges [*] (see page 640), 8 (see page 640) :	3.33 ns	16950A: 1.67 ns 16950B: 1.50 ns 16951B: 1.50 ns
Minimum master-to-slave clock time:	1 ns	N/A
Minimum slave-to-master clock time:	1 ns	N/A
Minimum slave-to-slave clock time:	3.33 ns	N/A
Minimum state clock pulse width:	Single edge: 1.0 ns Multiple edge: 1.0 ns	Single edge: 500 ps Multiple edge, 16950A: 1.67 ns Multiple edge, 16950B: 1.50 ns Multiple edge, 16951B: 1.50 ns
Clock qualifier setup time:	500 ps	N/A
Clock qualifier hold time:	0	N/A
Time tag resolution [5] (see page 640) :	2 ns	1.5 ns

Maximum time count between stored states:	32 days	32 days
Maximum trigger sequence speed:	300 MHz	16950A: 600 MHz 16950B: 667 MHz 16951B: 667 MHz
Maximum trigger sequence steps:	16	16
Trigger sequence step branching:	Arbitrary 4-way if/then/else	2-way if/then/else
Trigger position:	Start, center, end, or user-defined	Start, center, end, or user-defined
Trigger resources:	• 16 patterns evaluated as =, ≠, >, >=, <, <= • 14 double-bounded ranges evaluated as in range, not in range • 1 timer for every 34 channels • 2 global counters • 1 occurrence counter per sequence step • 4 flags	• 14 patterns evaluated as =, ≠, >, >=, <, <= • 7 double-bounded ranges evaluated as in range, not in range • 1 occurrence counter per sequence step • 4 flags
Trigger resource conditions:	Arbitrary Boolean combinations	Arbitrary Boolean combinations
Trigger actions:	• Go To • Trigger, send email, and fill memory • Trigger and Go To • Store/don't store sample • Turn on/off default storing • Timer start/stop/pause/resume • Global counter increment/decrement/reset • Occurrence counter reset • Flag set/clear	• Go To • Trigger and fill memory
Store qualification:	Default (global) and per sequence step	Default (global)
Maximum global counter:	2E+24	N/A
Maximum occurrence counter:	2E+24	2E+24
Maximum pattern width:	128 bits	128 bits

Maximum range width:	32 bits	32 bits
Timer value range:	50 ns to 2199 seconds	N/A
Timer resolution:	2 ns	N/A
Timer accuracy:	±(5 ns + 0.01%)	N/A
Timer reset latency:	50 ns	N/A

[*]Items marked with an asterisk (*) are specifications. All others are characteristics. "Typical" represents the average or median value of the parameter based on measurements from a significant number of units.
[1]Minimum eye width in system under test.
[2]Your choice of probe can limit system bandwidth. Choose a probe rated at 600 Mb/s or greater to maintain system bandwidth.
[3]Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes the input to be synchronously sampled coincident with each clock edge.
[4]Use of eye finder is recommended in 600 Mb/s (16950A) or 667 Mb/s (16950B, 16951B) state mode.
[5]In 300 Mb/s state mode, with all pods assigned, memory depth is half the maximum memory depth. With one pod pair (34 channels) unassigned, the memory depth is full One pod pair (34 channels) must remain unassigned for time tags in 600 Mb/s (16950A) or 667 Mb/s (16950B, 16951B) state mode.
[6]Independent analyzers may be either state or timing. When the 600 Mb/s (16950A) or 667 Mb/s (16950B, 16951B) state mode is selected, only one analyzer may be used.
[7]In the 300 Mb/s state mode, the total number of clocks and qualifiers is 4. All clock and qualifier inputs must be on the master modules.
[8]Tested with input signal Vh = 1.125 V, Vl = 0.875 V, threshold = 1.0 V, tr/tf = 180 ps ±30 ps (10%, 90%).
[9]Transitional timing speed and memory depth are halved unless a spare pod pair (34 channels) is unassigned.
[10]Available on 16950A only.

Timing (Asynchronous) Analysis Mode

	Conventional Timing	**Transitional Timing** [9] (see page 640)
Sample rate on all channels:	600 MHz	600 MHz
Sample rate in half channel mode:	1200 MHz	N/A
Number of channels:	68 x (number of cards)	For sample rates <600 MHz: 68 x (number of cards). For 600 MHz sample rate: 68 x (number of cards) - 34.
Maximum channels on a single time base and trigger:	340	340

Number of independent analyzers [6] (see page 640) :	2	2
Sample period (half channel):	833 ps	N/A
Sample period (full channel):	1.67 ns	1.67 ns
Minimum data pulse width:	1 sample period + 500 ps	1 sample period + 500 ps
Time interval accuracy:	±(1 sample period + 1.25 ns + 0.01% of time interval reading)	±(1 sample period + 1.25 ns + 0.01% of time interval reading)
Memory depth in full channel mode:	Option 256: 256 K [10] (see page 640) Option 001: 1 M Option 004: 4 M Option 016: 16 M Option 032: 32 M Option 064: 64 M 16951B: 256 M	Option 256: 256 K [10] (see page 640) Option 001: 1 M Option 004: 4 M Option 016: 16 M Option 032: 32 M Option 064: 64 M 16951B: 256 M
Memory depth in half channel mode:	Option 000: 512 K [10] (see page 640) Option 001: 2 M Option 004: 8 M Option 016: 32 M Option 032: 64 M Option 064: 128 M 16951B: 512 M	N/A
Maximum trigger sequence speed:	300 MHz	300 MHz
Maximum trigger sequence steps:	16	16
Trigger sequence step branching:	Arbitrary 4-way if/then/else	Arbitrary 4-way if/then/else
Trigger position:	Start, center, end, or user-defined	Start, center, end, or user-defined
Trigger resources:	• 16 patterns evaluated as =, ≠, >, >=, <, <= • 14 double-bounded ranges evaluated as in range, not in range • 3 edge/glitch • 1 timer for every 34 channels • 2 global counters • 1 occurrence counter per sequence step • 4 flags	• 15 patterns evaluated as =, ≠, >, >=, <, <= • 14 double-bounded ranges evaluated as in range, not in range • 3 edge/glitch • 1 timer for every 34 channels • 2 global counters • 1 occurrence counter per sequence step • 4 flags

Trigger resource conditions:	Arbitrary Boolean combinations	Arbitrary Boolean combinations
Trigger actions:	• Go To • Trigger, send email, and fill memory • Trigger and Go To • Turn on/off default storing • Timer start/stop/pause/resume • Global counter increment/decrement/reset • Occurrence counter reset • Flag set/clear	• Go To • Trigger, send email, and fill memory • Trigger and Go To • Turn on/off default storing • Timer start/stop/pause/resume • Global counter increment/decrement/reset • Occurrence counter reset • Flag set/clear
Maximum global counter:	2E+24	2E+24
Maximum occurrence counter:	2E+24	2E+24
Maximum range width:	32 bits	32 bits
Maximum pattern width:	128 bits	128 bits
Timer value range:	50 ns to 2199 seconds	50 ns to 2199 seconds
Timer resolution:	2 ns	2 ns
Timer accuracy:	±(5 ns + 0.01%)	±(5 ns + 0.01%)
Greater than duration:	3.33 ns to 55 ms in 3.3 ns increments	3.33 ns to 55 ms in 3.3 ns increments
Less than duration:	6.67 ns to 55 ms in 3.3 ns increments	6.67 ns to 55 ms in 3.3 ns increments
Timer reset latency:	50 ns	50 ns

Power Requirements

All necessary power is supplied by the backplane connector of the logic analysis system mainframe.

Environmental Characteristics

Indoor use only.

See individual probe Specifications and Characteristics for probe environmental characteristics.

- Operating Environment (see page 643)
- Non-operating Environment (see page 643)

Operating Environment

Temperature:	0°C to 40°C (+32°F to 104°F) when operating in a 16900A or 16902A mainframe. 0°C to 50°C (+32°F to 122°F) when operating in a 16901A or 16903A mainframe.
Humidity:	0 to 80% relative humidity at 40°C (+104°F). Reliability is enhanced when operating within the range 20% to 80% non-condensing.
Altitude:	0 to 3,000 m (10,000 ft)
Vibration:	Random vibration 5-500 Hz, 10 minutes per axis, approximately 0.2 g rms

Non-operating Environment

Temperature:	-40°C to +75°C (-40°F to +167°F). Protect the instrument from temperature extremes which cause condensation on the instrument.
Humidity:	0 to 90% relative humidity at 65°C (149°F)
Altitude:	0 to 15,300 m (50,000 ft)
Vibration (in shipping carton):	Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 2.41 g rms; and swept sine resonant search, 5 to 500 Hz, 0.50 g (0-peak), 5-minute resonant dwell at 4 resonances per axis.

See Also

- What is a Specification (see page 644)
- What is a Characteristic (see page 645)

16900-Series Logic Analysis System Frame Characteristics

- General Information (see page 643)
- Operating Environment Characteristics (see page 644)

General Information

Power:

16900A: 115/230 V, 48 to 66 Hz, 1300 W max.

16901A: 115/230 V, 48 to 66 Hz, 775 W max.

16902A: 115/230 V, 48 to 66 Hz, 1300 W max.

16903A: 115/230 V, 48 to 66 Hz, 900 W max.

Dimensions:

16900A/16902A/16903A - 254 mm height (9.99 in), 442 mm width (17.38 in), 559 mm depth (22.0 in)

16901A - 288.22 mm height (11.347 in), 443.23 mm width (17.450 in), 330.32 mm depth (13.005 in)

Weight:

	Max Net	Max Shipping
16900A:	16 kg (35.2 lbs)	24.6 kg (54.2 lbs)
16901A:	13.6 kb (30.0 lbs)	20.4 kg (45.0 lbs)
16902A:	17.2 kb (37.8 lbs)	25.8 kg (56.8 lbs)
16903A:	14.5 kg (32.0 lbs)	23.2 kg (51.0 lbs)

* Logic analyzer or other instrument cards ordered with mainframes will add 0.9 kg (2.0 lb per card).

User interface:

Windows® XP Professional.

Printers:

Can print to any local or network printer supported by Windows® XP Professional.

Operating Environment Characteristics

Temperature:	16900A and 16902A: 0°C to 40°C (32°F to 104°F) 16901A and 16903A: 0°C to 50°C (32°F to 122°F)
Humidity:	8 to 80% relative humidity at 40°C (104°F)
Altitude:	3000 m (10,000 ft)

See Also

- What is a Specification (see page 644)
- What is a Characteristic (see page 645)

What is a Specification?

A specification is a numeric value, or range of values, that bounds the performance of a product parameter. The product warranty covers the performance of parameters described by specifications. Products shipped from the factory meet all specifications. Additionally, products sent to Agilent Customer Service Centers for calibration, and returned, meet all specifications. Specifications are verified by *calibration procedures*.

What is a Calibration Procedure?

Calibration procedures verify that products or systems operate within the specifications. Parameters covered by specifications have a corresponding calibration procedure. Calibration procedures include both performance tests and system verification procedure. Calibration procedures are traceable and must specify adequate calibration standards.

Calibration procedures verify products meet the specifications by comparing measured parameters against a pass-fail limit. The pass-fail limit is the specification less any required guardband.

The term "calibration" refers to the process of measuring parameters and referencing the measurement to a calibration standard rather than the process of adjusting products for optimal performance.

NOTE Self-tests are not a substitute for calibration.

See Also

- What is a Characteristic (see page 645)

What is a Characteristic?

Characteristics describe product performance that is useful in the application of the product, but that is not covered by the product warranty. Characteristics describe performance that is typical of the majority of a given product, but not subject to the same rigor associated with specifications. Characteristics are verified by *function tests*.

What is a Function Test? Function tests are quick tests designed to verify basic operation of a product. Function tests include operator's checks and operation verification procedures. An operator's check is normally a fast test used to verify basic operation of a product. An operation verification procedure verifies some, but not all, specifications, and often at a lower confidence level than a calibration procedure.

See Also

- What is a Specification (see page 644)

Glossary

A

acquisition Denotes one complete cycle of data gathering by a measurement module. For example, if you are using an analyzer with 200K memory depth, one complete acquisition will capture and store 200K states in acquisition memory.

acquisition depth The acquisition depth is the amount of memory that is filled with data on an acquisition. The choices available depend on the maximum memory depth available in the analyzer that is being used.

action Actions are things that the analyzer does as a part of triggering, for example "Then Trigger and Fill Memory" or "Start Timer."

activity indicator Symbols next to logic analyzer channels that indicate whether a signal is a logic-high, or logic-low, or whether the signal is changing between highs and lows.

advanced trigger Advanced triggers provide more power than simple triggers, but are more complex.

analysis probe A probe connected to a microprocessor or standard bus in the device under test. An analysis probe provides an interface between the signals of the microprocessor or standard bus and the inputs of the logic analyzer.

arming Typically, instruments are armed immediately when Run or Run Repetitive is selected. For example, logic analyzers are commonly used to arm oscilloscopes.

asynchronous sampling When the logic analyzer acquires samples from the device under test asynchronously, that is, at regular intervals, such as every 100 ns. Also known as timing mode.

B

beginning of acquisition The beginning of the acquisition is the point in time where the collection of data begins.

bits A bit is a single signal in a bus. Numbering of bits begins with 0.

bus A bus is a group of associated signals, such as ADDR or DATA.

C

captured data Signal values that have been sampled by the logic analyzer and stored in its memory.

card A logic analyzer that can be inserted into a slot (see page 653) in a frame (see page 649). Cards can be combined with others to increase the channel count available in a single time domain.

channel A single line of input to the logic analyzer. Each channel corresponds to a lead that is connected to the device under test. Each channel is used to acquire one and only one signal from the device under test.

clock channel A special logic analyzer input channel that can be used to determine the analyzer's sampling. Clock channels are identified on a pod by CLK.

D

data channel A channel that carries data. Data channels cannot be used to clock logic analyzers. Data channels are numbered as opposed to clock channels which are labeled CLK.

default storage Default storage means "unless sequence step storage specifies otherwise, this is what should be stored". Sequence step storage always overrides default storage.

delay Delay is the horizontal position of the waveform on the screen for the timing analyzer. Delay time is measured from the trigger point in seconds.

device under test The system under development whose digital signals are captured by the logic analyzer.

don't care A "don't care" means that the state of the signal (high or low) is not relevant to the measurement. The analyzer ignores the state of this signal when determining whether a match occurs on an input bus/signal.

double-click When using a mouse as a pointing device, to double-click an item, position the cursor over the item, and then quickly press and release the left mouse button twice.

drag and drop Position the cursor over the item, and then press and hold the left mouse button. While holding the left mouse button down, move the mouse to drag the item to a new location. When the item is positioned where you want it, release the mouse button.

E

edge Logic analyzer trigger resources that allow detection of transitions on a signal. An edge term can be set to detect a rising edge, falling edge, or either edge or glitch.

event Events are the things you are looking for in your device under test, for example ADDR=0 or ADDR=5.

external trigger A signal outside the logic analyzer that is used to synchronize measurements between instruments. For example, the logic analyzer can be armed (activated) by a signal that comes from another instrument. Logic analyzers are commonly used to trigger oscilloscopes through a BNC connection.

F

frame A modular logic analysis system that has slot (see page 653)s in the back for the insertion of logic analyzer card (see page 648)s. Multiple frames can be connected together to form a multiframe logic analysis system.

G

glitch A glitch occurs when two or more transitions cross the logic threshold between consecutive timing analyzer samples.

I

inverse assembler A tool that displays the assembly language instructions for captured machine code.

L

logic analyzer An instrument that captures and displays digital signal values. A logic analyzer is like an oscilloscope, except that it only displays two voltage levels (a logic high or 1, and a logic low or 0) instead of many voltage levels. Because a logic analyzer only captures 1s and 0s, its sample rate can be slower than an oscilloscope that needs to capture move voltage detail. Consequently, a logic analyzer can capture a greater amount of overall execution time.

M

macro

- In pattern generator modules, "macros" (in the online help) are like subroutines in a programming language; they can have parameters and they can be called multiple times in the vector sequence to generate repeated or similar output vectors.
- In Microsoft Visual Basic for Applications (VBA), "macros" (in the online help) are **Sub** procedures that can be run from the user interface to automate an application.
- In previous Agilent logic analysis systems, macros, or *trigger macros* (see page 402), were what are now called trigger function (see page 655)s: preprogrammed components that are used to build trigger sequences.

marker A relocatable reference point in the data display. Markers can be used to measure time intervals or sample intervals. Markers are assigned to patterns in order to find patterns or track sequences of state in the data.

menu bar The menu bar is located at the top of all windows. Use it to select drop down menus that contain tool or system options.

module A logical collection of logic analyzer card (see page 648)s that are connected together. This gives you the flexibility to increase channel count by using more than one card. A module can be a single card or several cards, and a single card or several card module can be split into two modules. By definition, a module consists of a single time domain. While a module can consist of a single card, a module is not a physical entity.

O

occurrence Occurrence is used in triggering to define how many times something happens during the acquisition.

offline analysis Analyzing previously captured and saved logic analysis data without data acquisition hardware. In other words, you can use the *Agilent Logic Analyzer* application by itself on a Windows XP/2000 computer to analyze data in the waveform, listing, and compare windows.

P

pattern Logic analyzer resources that represent single states to be found on buses/signals; for example, an address on the address bus or a status on the status lines.

pod A physical collection of logic analyzer channels within a card (see page 648). Pods are numbered relative to cards only. Pods are used to physically connect data and clock signals from the device under test to the analyzer.

pod index A logical number for a pod (see page 651). If a module (see page 650) has 20 pods, the pod indexes are 1 through 20 with no renumbering at card boundaries. In a multi-card module, numbering begins with the master card then continues from the bottom card up. Pod indexes can be used without considering how many pods are on each card (see page 648), or in which slot (see page 653)s the cards are located.

pod pair A group of two pods containing 16 data channels and 1 clock channel each. Pod pairs are used to physically connect data and clock signals from the device under test to the analyzer. Pods are assigned by pairs in the analyzer interface. The number of pod pairs available is determined by the channel width of the instrument.

pod truncation This occurs when opening a configuration file that was saved from a logic analyzer module that had more pods. Because the current module has fewer pods, truncation occurs. Any buses/signals assigned to truncated pods are unusable.

point To point to an item, move the mouse cursor over the item.

polarity Positive polarity is when an incoming low voltage is shown with a high waveform and a logical value of 1. Negative polarity is when an incoming high voltage is shown with a low waveform and a logical value of 0. Polarity affects the display of values and waveforms, and does not affect the trigger.

preprocessor See analysis probe (see page 647).

probe A device to connect the various instruments of the logic analysis system to the device under test. There are many types of probes and the one you should use depends on the instrument and your data requirements. As a verb, "to probe" means to attach a probe to the device under test.

protocol An agreed-upon format for transmitting data between two devices. The protocol determines: the type of error checking, data compression, encoding, how sending devices indicate they have finished sending a message, and how receiving devices indicate they have received a message.

Q

quick trigger Quick trigger allows you to quickly set up a simple trigger within the waveform and listing displays, by drawing a rectangle in the display area with the mouse. After a simple trigger has been defined, and the analyzer is run, the trigger is stored and can be recalled at any time.

R

range pattern Logic analyzer resources which let you set up patterns that represent a range of values, such as "ADDR in range 1000 to 2000". Most logic analyzers support a "not in range" operator as well as the "in range" operator. Range patterns are a convenient shortcut that can be used instead of AND'ing or OR'ing two patterns, such as "ADDR >= 1000 and ADDR <= 2000".

repetitive measurement A measurement in which the logic analyzer's trigger condition is searched for, and data storage is filled, repetitively.

right-click When using a mouse for a pointing device, to right-click an item, position the cursor over the item, and then quickly press and release the right mouse button.

run The single run measurement will save captured data to trace memory one time. The amount of data stored during a single run is equal to the amount of trace memory allotted.

run repetitive The run repetitive measurement will save the captured data to trace memory repetitively. The amount of data stored in a repetitive run is the same as a single run. During a repetitive run once the trace memory is full the system clears the trace memory and begins to refill with new data. This cycle will continue until the run is stopped.

S

sample A data sample is a single measurement. When an instrument samples the device under test, it takes a single measurement as part of its data acquisition cycle. The number of samples acquired is equal to the logic analyzers memory depth.

sample period The sample period is the period of time between samples. The sample period can be based on an internal sampling clock (also known as timing analysis or asynchronous sampling). Or, the sampling can be based on a signal in the device under test (also known as state analysis, or synchronous sampling).

sampled data Signal values that are sampled by the logic analyzer (not necessarily stored).

sampling The process by which the logic analyzer looks at digital signals.

search Searches through the acquired data for specified data pattern or value, time value, sample number, or marker. Search criteria can range from specific bits to multiple events, depending on which search option you choose.

simple trigger Simple triggers include triggers such as edges and bus patterns.

single measurement A measurement in which the logic analyzer's trigger condition is searched for, and data storage is filled, once.

skew Skew is the difference in channel delays between measurement channels.

slot An opening in the back of a frame (see page 649) where card (see page 648)s can be inserted. The slots are lettered from A to F with A being the topmost slot. Slots are physical entities and are always referred to by slot letter.

snap to edge markers Snap to edge markers enable easy placement of markers on waveform edges. When a marker is moved in the data display area, the cursor changes to a green "direction arrow" indicating the direction of the next valid edge. A red "valid edge" bar is placed on the next edge that the marker will be placed on.

state analyzer A logic analyzer that samples based on a clock signal in the device under test.

state measurement In a state measurement, the logic analyzer is clocked by a signal from the system under test. Each time the clock signal becomes valid, the analyzer samples data from the system under test. Since the analyzer is clocked by the system, state measurements are synchronous with the test system.

state mode When the logic analyzer acquires samples from the device under test synchronously, in other words, when a signal or signals from the device under test indicates when to acquire a sample. For example, the logic analyzer might take a sample whenever there is a rising edge on a signal from the device under test. Typically, the signal used to set up the sampling is a state machine clock signal or microprocessor clock signal. Also know as synchronous sampling.

stop Stops the measurement currently in progress.

storage qualification Storage qualification is only available in a state measurement, not timing measurements. Store qualification allows you to specify the type of data (all samples, no samples, or selected states) to be stored in memory. Use store qualification to prevent memory from being filled with unwanted activity such as wait-loops. Storage qualification lets you filter out specific types of data as the acquisition is running, which saves memory. In contrast filters can hide data after it has been collected.

symbols Names assigned to particular bus or signal values. Symbols in a display of captured data values are easy to read. Also, symbols make it easy to set up triggers on particular values. For example, in a communication protocol you could display the value FF as "end of file."

synchronous sampling When the logic analyzer acquires samples from the device under test synchronously, in other words, when a signal or signals from the device under test indicates when to acquire a sample. For example, the logic analyzer might take a sample whenever there is a rising edge on a signal from the device under test. Typically, the signal used to set up the sampling is a state machine clock signal or microprocessor clock signal. Also know as state mode.

T

target system See device under test (see page 648).

threshold voltage The voltage level that the signal must cross before the logic analyzer recognizes a change in voltage levels. A high voltage level is indicated by a "1" and a low voltage level is indicated by a "0." TTL and ECL are two examples of voltage levels that the signal must cross.

time/division Time/division controls the "zooming" of a waveform display. Increasing the time/division zooms out, while decreasing the time/division zooms in.

timer Timers are used to create either a user-defined delay or a time standard which valid data duration is evaluated against.

timing analyzer A logic analyzer that samples at regular intervals based on an internal clock signal.

timing measurement In a timing measurement, the logic analyzer samples data at regular intervals according to a clock signal internal to the timing analyzer. Since the analyzer is clocked by a signal that is not related to the device under test, timing measurements capture traces of electrical activity over time. These measurements are asynchronous with the device under test.

timing mode When the logic analyzer samples from the device under test asynchronously, that is, at regular intervals, such as every 100 ns. Also known as asynchronous sampling.

tool tip Small information display (text readout) that appears during mouse operations such as hovering over a waveform or bus/signal name, moving markers, or drawing a rectangle in data. Use them as comments (see page 95) or to read current positions, waveform transition widths, or trigger specifications (when setting up quick triggers (see page 129) with mouse).

trace See acquisition (see page 647).

transitional timing When the logic analyzer is in transitional timing mode, the timing analyzer samples data at regular intervals, but only stores data when there is a threshold level transition (high-to-low transition, or low-to-high transition). Each time a level transition occurs on any of the bits, data on all channels is stored. A time tag is stored with each stored data sample so the measurement can be reconstructed and displayed later.

trigger The event about which acquired data is stored; in other words, the event that you are looking for. For example, you may want to trigger on an edge in order to see the events that lead up to it and the events that happen after it. The event that triggers the logic analyzer becomes a reference point in the data display.

trigger function Trigger functions are preprogrammed components that are used to build trigger sequences.

trigger history Each time you set up a new trigger and run the measurement, the trigger setup is saved in the configuration file. Each saved trigger can be retrieved and reused. The default number of triggers saved is 10.

trigger position The location of the trigger event in trace memory. If you want to view data after, about, or before the trigger event, you set the trigger position to the start, center, or end of trace memory, respectively.

trigger sequence A trigger sequence is a sequence of events that you specify. The logic analyzer compares this sequence with the samples it is collecting to determine when to trigger.

V

value at measurement The value at measurement measures the value of a bus or a single signal at a specified marker location in data. Measurement results are displayed in the marker measurement display bar.

Z

zooming To expand and contract the waveform along the time base by varying the value in the time/div field. This action allows you to view specific portions of a particular waveform.

Index

Symbols

Numerics

A

B

C

G

H

N

O

P

U

V

W

X

Z