# Keysight D9050PCIC PCIe Gen5 Compliance Application

KEYSIGHT

PROGRAMMER'S REFERENCE

# Notices



## Revision

Version 5.1.0.0

## Edition

September 2023

Available in electronic format only

Published by:
Keysight Technologies, Inc.
1900 Garden of the Gods Road
Colorado Springs, CO 80907 USA

## Warranty

**The material contained in this document is provided "as is," and is subject to being changed, without notice, in future editions. Further, to the maximum extent permitted by applicable law, Keysight disclaims all warranties, either express or implied, with regard to this manual and any information contained herein, including but not limited to the implied warranties of merchantability and fitness for a particular purpose. Keysight shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein. Should Keysight and the user have a separate written agreement with warranty terms covering the material in this document that conflict with these terms, the warranty terms in the separate agreement shall control.**

## Technology License

The hardware and/or software described in this document are furnished under a license and may be used or copied only in accordance with the terms of such license.

## U.S. Government Rights

The Software is "commercial computer software," as defined by Federal Acquisition Regulation ("FAR") 2.101. Pursuant to FAR 12.212 and 27.405-3 and Department of Defense FAR Supplement ("DFARS") 227.7202, the U.S. government acquires commercial computer software under the same terms by which the software is customarily provided to the public. Accordingly, Keysight provides the Software to U.S. government customers under its standard commercial license, which is embodied in its End User License Agreement (EULA), a copy of which can be found at www.keysight.com/find/sweula. The license set forth in the EULA represents the exclusive authority by which the U.S. government may use, modify, distribute, or disclose the Software. The EULA and the license set forth therein, does not require or permit, among other things, that Keysight: (1) Furnish technical information related to commercial computer software or commercial computer software documentation that is not customarily provided to the public; or (2) Relinquish to, or otherwise provide, the government rights in excess of these rights customarily provided to the public to use, modify, reproduce, release, perform, display, or disclose commercial computer software or commercial computer software documentation. No additional government requirements beyond those set forth in the EULA shall apply, except to the extent that those terms, rights, or licenses are explicitly required from all providers of commercial computer software pursuant to the FAR and the DFARS and are set forth specifically in writing elsewhere in the EULA. Keysight shall be under no obligation to update, revise or otherwise modify the Software. With respect to any technical data as defined by FAR 2.101, pursuant to FAR 12.211 and 27.404.2 and DFARS 227.7102, the U.S. government acquires no greater than Limited Rights as defined in FAR 27.401 or DFAR 227.7103-5 (c), as applicable in any technical data.

## Safety Notices

**CAUTION**

A **CAUTION** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a **CAUTION** notice until the indicated conditions are fully understood and met.

**WARNING**

**A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.**

# In This Book

This book is your guide to programming the Keysight Technologies D9050PCIC PCIe Gen5 Compliance Application.

- Chapter 1, “Introduction to Programming,” starting on page 7, describes compliance application programming basics.
- Chapter 2, “Configuration Variables and Values,” starting on page 9, Chapter 3, “Test Names and IDs,” starting on page 39, Chapter 4, “Instruments,” starting on page 91, and Chapter 5, “Message IDs,” starting on page 93 provide information specific to programming the D9050PCIC PCIe Gen5 Compliance Application.

## How to Use This Book

Programmers who are new to compliance application programming should read all of the chapters in order. Programmers who are already familiar with this may review chapters 2, 3, 4, and 5 for changes.

# Contents

In This Book / 3

1 Introduction to Programming

Remote Programming Toolkit / 8

2 Configuration Variables and Values

3 Test Names and IDs

4 Instruments

5 Message IDs

Index

# 1 Introduction to Programming

Remote Programming Toolkit / 8

This chapter introduces the basics for remote programming a compliance/test application. The programming commands provide the means of remote control. Basic operations that you can do remotely with a computer and a compliance/test app running on an oscilloscope include:

- Launching and closing the application.
- Configuring the options.
- Running tests.
- Getting results.
- Controlling when and were dialogs get displayed
- Saving and loading projects.

You can accomplish other tasks by combining these functions.

# Remote Programming Toolkit

The majority of remote interface features are common across all the Keysight Technologies, Inc. family of compliance/test applications. Information on those features is provided in the N5452A Compliance Application Remote Programming Toolkit available for download from Keysight here: www.keysight.com/find/rpi. The D9050PCIC PCIe Gen5 Compliance Application uses Remote Interface Revision 7.120. The help files provided with the toolkit indicate which features are supported in this version.

In the toolkit, various documents refer to "application-specific configuration variables, test information, and instrument information". These are provided in Chapters 2, 3, and 4 of this document, and are also available directly from the application's user interface when the remote interface is enabled (View>Preferences::Remote tab::Show remote interface hints). See the toolkit for more information.

# 2 Configuration Variables and Values

The following table contains a description of each of the D9050PCIC PCIe Gen5 Compliance Application options that you may query or set remotely using the appropriate remote interface method. The columns contain this information:

- GUI Location – Describes which graphical user interface tab contains the control used to change the value.
- Label – Describes which graphical user interface control is used to change the value.
- Variable – The name to use with the SetConfig method.
- Values – The values to use with the SetConfig method.
- Description – The purpose or function of the variable.

For example, if the graphical user interface contains this control on the **Set Up** tab:

- Enable Advanced Features

then you would expect to see something like this in the table below:

**Table 1** Example Configuration Variables and Values

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Set Up | Enable Advanced Features | EnableAdvanced | True, False | Enables a set of optional features. |

and you would set the variable remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SetConfig 'EnableAdvanced' 'True'"

C# syntax
```

```
---------
remoteAte.SetConfig("EnableAdvanced", "True");
```

Here are the actual configuration variables and values used by this application:

**NOTE** Some of the values presented in the table below may not be available in certain configurations. Always perform a "test run" of your remote script using the application's graphical user interface to ensure the combinations of values in your program are valid.

**NOTE** The file, "ConfigInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

**Table 2** Configuration Variables and Values

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Configure | Bandwidth Setup for PAM4 | BandwidthFilterPAM4_64G | BESSEL4 | This is the setup for PAM4's bandwidth setting. |
| Configure | CTLE Equalization Method | CTLEEqualizationMethod_32G | SigTest, Infiniium | Specify the CTLE equalization method to use for 32GT/s Base Transmitter Tests (Jitter Tests only). By default, SigTest method is used to measure CTLE equalization. |
| Configure | CTLE Equalization Method | CTLEEqualizationMethod_64G | SigTest, Infiniium | Specify the CTLE equalization method to use for 64GT/s Base Transmitter Tests (Jitter Tests only). By default, Infiniium method is used to measure CTLE equalization. |
| Configure | Clock Recovery Method | ClockRecoveryMethod_64G | PCIe6CXLBehavioralSRIS, SecondOrderPLLOJTF | This is the setting to enable user to select clock recovery method in 64GT/s. |
| Configure | Compliance Signal Check | EnableSignalCheck_16G | 1.0, 0.0 | When signal check is enabled, the input signal is pre-tested and verified to be within a reasonable range of timing and voltage limits. This can be useful for detecting problems like cabling errors before a test is run. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Configure | Compliance Signal Check | EnableSignalCheck_2P5G | 1.0, 0.0 | When signal check is enabled, the input signal is pre-tested and verified to be within a reasonable range of timing and voltage limits. This can be useful for detecting problems like cabling errors before a test is run. |
| Configure | Compliance Signal Check | EnableSignalCheck_32G | 1.0, 0.0 | When signal check is enabled, the input signal is pre-tested and verified to be within a reasonable range of timing and voltage limits. This can be useful for detecting problems like cabling errors before a test is run. |
| Configure | Compliance Signal Check | EnableSignalCheck_5G | 1.0, 0.0 | When signal check is enabled, the input signal is pre-tested and verified to be within a reasonable range of timing and voltage limits. This can be useful for detecting problems like cabling errors before a test is run. |
| Configure | Compliance Signal Check | EnableSignalCheck_8G | 1.0, 0.0 | When signal check is enabled, the input signal is pre-tested and verified to be within a reasonable range of timing and voltage limits. This can be useful for detecting problems like cabling errors before a test is run. |
| Configure | Gen 2 Ref Clock Transfer Function (Common Clock) | Gen2CommonRefClkTF | H1: 5MHz, 1.0dB peaking \| H2: 16MHz, 3.0dB peaking, H1: 8MHz, 3.0dB peaking \| H2: 16MHz, 3.0dB peaking | Select the transfer function for Gen 2 reference clock signal. |
| Configure | Linear Fit Pulse Delay, Dp | LinearFitPulseDelay_64G | (Accepts user-defined text), 4 | This is the setting for linear fit pulse delay. |
| Configure | Linear Fit Pulse Length, Np | LinearFitPulseLength_64G | (Accepts user-defined text), 600 | This is the setting for linear fit pulse length. |
| Configure | Low Pass Filter | EnableLowPassFilter | 1, 0 | This configuration will enable low pass filter option for PCIE-SIG Clock Jitter Tools. When this is enabled, an additional low pass filter will be enabled. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Configure | Manual Input Pattern File | ManualInputPatternFile_64G | Disabled, Enabled | This is the setting to enable user to manually input the pattern file. |
| Configure | Manual Input Scope Random Noise | ManualInputScopeRNValue_64G | Disabled, Enabled | This is the setting to enable user to manually input the scope random noise values. |
| Configure | Noise Floor Deembed | EnableNFDeembed | 1, 0 | This configuration will enable noise floor deembedding for PCIE-SIG Clock Jitter Tools. When this is enabled, the noise floor waveform will be analyzed to remove the phase jitter impacts from the test environment. |
| Configure | Noise Reduction BW, Hz | EBW_16G_BASE | (Accepts user-defined text), 50.0E+9, 25.0E+9, 20.0E+9, 16.0E+9 | Specify the noise reduction bandwidth to use for all 16GT/s Base Transmitter Tests. The acceptable range of bandwidth is from 16.0GHz to 63.0Hz. |
| Configure | Noise Reduction BW, Hz | EBW_16G_EP | (Accepts user-defined text), 50.0E+9, 25.0E+9, 20.0E+9, 16.0E+9 | Specify the noise reduction bandwidth to use for all 16GT/s CEM End Point Tests. The acceptable range of bandwidth is from 16.0GHz to 63.0Hz. |
| Configure | Noise Reduction BW, Hz | EBW_16G_RC | (Accepts user-defined text), 50.0E+9, 25.0E+9, 20.0E+9, 16.0E+9 | Specify the noise reduction bandwidth to use for all 16GT/s CEM Root Complex Tests. The acceptable range of bandwidth is from 16.0GHz to 63.0Hz. |
| Configure | Noise Reduction BW, Hz | EBW_2P5G_BASE | (Accepts user-defined text), 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9, 8.0E+9, 7.0E+9, 6.5E+9, 6.0E+9 | Specify the noise reduction bandwidth to use for all tests. The acceptable range of bandwidth is from 2.5GHz to 63.0Hz. |
| Configure | Noise Reduction BW, Hz | EBW_2P5G_EP | (Accepts user-defined text), 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9, 8.0E+9, 7.0E+9, 6.5E+9, 6.0E+9 | Specify the noise reduction bandwidth to use for all tests. The acceptable range of bandwidth is from 2.5GHz to 63.0Hz. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Configure | Noise Reduction BW, Hz | EBW_2P5G_RC | (Accepts user-defined text), 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9, 8.0E+9, 7.0E+9, 6.5E+9, 6.0E+9 | Specify the noise reduction bandwidth to use for all tests. The acceptable range of bandwidth is from 2.5GHz to 63.0Hz. |
| Configure | Noise Reduction BW, Hz | EBW_32G_BASE | (Accepts user-defined text), 50.0E+9, 33.0E+9 | Specify the noise reduction bandwidth to use for all 32GT/s Base Transmitter Tests. The acceptable range of bandwidth is from 32.0GHz to 63.0Hz. |
| Configure | Noise Reduction BW, Hz | EBW_32G_EP | (Accepts user-defined text), 50.0E+9, 33.0E+9 | Specify the noise reduction bandwidth to use for all 32GT/s CEM End Point Tests. The acceptable range of bandwidth is from 32.0GHz to 63.0Hz. |
| Configure | Noise Reduction BW, Hz | EBW_32G_RC | (Accepts user-defined text), 50.0E+9, 33.0E+9 | Specify the noise reduction bandwidth to use for all 32GT/s CEM Root Complex Tests. The acceptable range of bandwidth is from 32.0GHz to 63.0Hz. |
| Configure | Noise Reduction BW, Hz | EBW_5G_BASE | (Accepts user-defined text), 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9, 8.0E+9 | Specify the noise reduction bandwidth to use for all tests. The acceptable range of bandwidth is from 5.0GHz to 63.0Hz. |
| Configure | Noise Reduction BW, Hz | EBW_5G_EP | (Accepts user-defined text), 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9, 8.0E+9 | Specify the noise reduction bandwidth to use for all tests. The acceptable range of bandwidth is from 5.0GHz to 63.0Hz. |
| Configure | Noise Reduction BW, Hz | EBW_5G_RC | (Accepts user-defined text), 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9, 8.0E+9 | Specify the noise reduction bandwidth to use for all tests. The acceptable range of bandwidth is from 5.0GHz to 63.0Hz. |
| Configure | Noise Reduction BW, Hz | EBW_64G_BASE | (Accepts user-defined text), 33.0E+9 | Specify the noise reduction bandwidth to use for all 64GT/s Base Transmitter Tests. The acceptable range of bandwidth is from 32.0GHz to 63.0Hz. Note: This bandwidth setting is set on the applied filter response. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Configure | Noise Reduction BW, Hz | EBW_8G_BASE | (Accepts user-defined text), 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9 | Specify the noise reduction bandwidth to use for all tests. The acceptable range of bandwidth is from 8.0GHz to 63.0Hz. |
| Configure | Noise Reduction BW, Hz | EBW_8G_EP | (Accepts user-defined text), 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9 | Specify the noise reduction bandwidth to use for all tests. The acceptable range of bandwidth is from 8.0GHz to 63.0Hz. |
| Configure | Noise Reduction BW, Hz | EBW_8G_RC | (Accepts user-defined text), 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9 | Specify the noise reduction bandwidth to use for all tests. The acceptable range of bandwidth is from 8.0GHz to 63.0Hz. |
| Configure | Number of UI | NumUI_16G | (Accepts user-defined text), 8.0E+6, 2.5E+6, 2.0E+6, 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3 | This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests. |
| Configure | Number of UI | NumUI_2P5G | (Accepts user-defined text), 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3 | This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Configure | Number of UI | NumUI_32G | (Accepts user-defined text), 8.0E+6, 2.5E+6, 2.0E+6, 1.6E+6 | This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests. |
| Configure | Number of UI | NumUI_5G | (Accepts user-defined text), 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3 | This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests. |
| Configure | Number of UI | NumUI_64G | (Accepts user-defined text), 4.5E+6, 2.0E+6 | This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Configure | Number of UI | NumUI_8G | (Accepts user-defined text), 2.4E+6, 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3 | This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests. |
| Configure | Number of UI | NumUI_RefClk | (Accepts user-defined text), 200000, 100000, 50000, 25000 | This is the minimum number of unit intervals used in reference clock tests. |
| Configure | Number of UI for PWJ Tests | NumUI_PWJ_16G | (Accepts user-defined text), 2.0E+6, 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3 | This is the minimum number of unit intervals used in PWJ tests. These measurements should be made using the clock pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests. |
| Configure | OJTF Damping Factor | OJTFDampingFactor_64G | (Accepts user-defined text), 0.707 | This is the setting to enable user to define OJTF damping factor in 64GT/s. |
| Configure | OJTF Loop Bandwidth, Hz | OJTFLoopBandwidth_64G | (Accepts user-defined text), 10000000 | This is the setting to enable user to define OJTF loop bandwidth (Hz) in 64GT/s. |
| Configure | Points per UI, M | PointsPerUI_64G | (Accepts user-defined text), 32 | This is the setting for sample points per UI. |
| Configure | RefClk Noise Reduction BW, Hz | ClockEBW | 0.0, 8.0E+9, 7.0E+9, 6.0E+9, 5.0E+9, 4.5E+9, 4.0E+9, 3.5E+9, 3.0E+9, 2.5E+9, 2.0E+9, 1.5E+9, 1.0E+9 | Select the bandwidth to acquire reference clock signal. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Configure | RefClk Settings Precedence | ReferenceClockPrecedence | Number of Clock UI Cycles, Sampling Rate | When memory depth is insufficient (Application limits to 200 Mpts), select which setting takes precedence. Number of Clock UI Cycles takes precedence means sampling rate is limited. Sampling rate takes precedence means Number of Clock UI Cycles is limited. When memory depth is sufficient, no changes are made. If "Use Real Edge Connection" is enabled, precedence will be set to Sampling Rate since Real-Edge connection sample rate of 160GSa/s has been configured. |
| Configure | SSC Removal | EnableSSCRemoval | 1, 0 | This configuration will enable SSC removal for PCIE-SIG Clock Jitter Tools. When this is enabled, SSC spikes will be removed from the phase jitter spectrum. Per the PCIe* 5.0 base spec, this feature must be enabled for PCIe* 5.0 and 4.0. |
| Configure | Sample Rate, GSa/s | SRate_16G | 160.0E+9, 80.0E+9, 256.0E+9, 128.0E+9 | (Limited availability*) Specify the sample rate to use for all PCIE 2.0 (5.0 GT/s) tests or PCIE 3.0 (8.0 GT/s) tests. |
| Configure | Sample Rate, GSa/s | SRate_2P5G | 160.0E+9, 80.0E+9, 40.0E+9, 20.0E+9, 128.0E+9, 64.0E+9, 32.0E+9 | (Limited availability*) Specify the sample rate to use for all PCIE 2.0 (5.0 GT/s) tests or PCIE 3.0 (8.0 GT/s) tests. |
| Configure | Sample Rate, GSa/s | SRate_32G | 160.0E+9, 80.0E+9, 256.0E+9 | (Limited availability*) Specify the sample rate to use for all PCIE 2.0 (5.0 GT/s) tests or PCIE 3.0 (8.0 GT/s) tests. |
| Configure | Sample Rate, GSa/s | SRate_5G | 160.0E+9, 80.0E+9, 40.0E+9, 128.0E+9, 64.0E+9 | (Limited availability*) Specify the sample rate to use for all PCIE 2.0 (5.0 GT/s) tests or PCIE 3.0 (8.0 GT/s) tests. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Configure | Sample Rate, GSa/s | SRate_64G | 160.0E+9, 80.0E+9, 256.0E+9 | (Limited availability*) Specify the sample rate to use for all PCIE 6.0 (64.0 GT/s) tests. |
| Configure | Sample Rate, GSa/s | SRate_8G | 160.0E+9, 80.0E+9, 40.0E+9, 256.0E+9, 128.0E+9, 64.0E+9 | (Limited availability*) Specify the sample rate to use for all PCIE 2.0 (5.0 GT/s) tests or PCIE 3.0 (8.0 GT/s) tests. |
| Configure | Sample Rate, GSa/s | SRate_RefClk | Maximum, 80.0E+9, 40.0E+9, 20.0E+9, 256.0E+9, 128.0E+9, 64.0E+9, 32.0E+9 | Select the sample rate to acquire reference clock signal. |
| Configure | Show Jitter Filter Plot | ShowJitterFilterPlot | 0, 2, 3, 4, 5 | Select the clock jitter plot to display. Generating plots will increase test runtime. |
| Configure | SigTest Version | AddIn_SigTestVer16GT | (Accepts user-defined text), 4.0.52 | Specify the version of the SigTest for 16.0 GT/s Add-In Card Tests. Setting is defined according to Data Rate. |
| Configure | SigTest Version | AddIn_SigTestVer2P5GT | (Accepts user-defined text), 3.2.0.3 | Specify the version of the SigTest for 2.5 GT/s Add-In Card Tests. Setting is defined according to Data Rate. |
| Configure | SigTest Version | AddIn_SigTestVer32GT | (Accepts user-defined text), 5.1.04 | Specify the version of the SigTest for 32.0 GT/s Add-In Card Tests. Setting is defined according to Data Rate. |
| Configure | SigTest Version | AddIn_SigTestVer5GT | (Accepts user-defined text), 3.2.0.3 | Specify the version of the SigTest for 5.0 GT/s Add-In Card Tests. Setting is defined according to Data Rate. |
| Configure | SigTest Version | AddIn_SigTestVer8GT | (Accepts user-defined text), 3.2.0.3 | Specify the version of the SigTest for 8.0 GT/s Add-In Card Tests. Setting is defined according to Data Rate. |
| Configure | SigTest Version | Base_SigTestVer16GT | (Accepts user-defined text), 4.0.52 | Specify the version of the SigTest for 16.0 GT/s Base Transmitter Tests. Setting is defined according to Data Rate. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Configure | SigTest Version | Base_SigTestVer2P5GT | (Accepts user-defined text), 4.0.52 | Specify the version of the SigTest for 2.5 GT/s Base Transmitter Tests. Setting is defined according to Data Rate. |
| Configure | SigTest Version | Base_SigTestVer32GT | (Accepts user-defined text), 5.1.04 | Specify the version of the SigTest for 32.0 GT/s Base Transmitter Tests. Setting is defined according to Data Rate. |
| Configure | SigTest Version | Base_SigTestVer5GT | (Accepts user-defined text), 4.0.52 | Specify the version of the SigTest for 5.0 GT/s Base Transmitter Tests. Setting is defined according to Data Rate. |
| Configure | SigTest Version | Base_SigTestVer8GT | (Accepts user-defined text), 4.0.52 | Specify the version of the SigTest for 8.0 GT/s Base Transmitter Tests. Setting is defined according to Data Rate. |
| Configure | SigTest Version | Preset_SigTestVer16GT | (Accepts user-defined text), 4.0.52 | Specify the version of the SigTest for 16.0 GT/s Base Transmitter Tests (Equalization Preset Test). Setting is defined according to Data Rate. |
| Configure | SigTest Version | Preset_SigTestVer32GT | (Accepts user-defined text), 5.1.04 | Specify the version of the SigTest for 32.0 GT/s Base Transmitter Tests (Equalization Preset Test). Setting is defined according to Data Rate. |
| Configure | SigTest Version | Preset_SigTestVer8GT | (Accepts user-defined text), 4.0.52 | Specify the version of the SigTest for 8.0 GT/s Base Transmitter Tests (Equalization Preset Test). Setting is defined according to Data Rate. |
| Configure | SigTest Version | System_SigTestVer16GT | (Accepts user-defined text), 4.0.52 | Specify the version of the SigTest for 16.0 GT/s System Tests. Setting is defined according to Data Rate. |
| Configure | SigTest Version | System_SigTestVer2P5GT | (Accepts user-defined text), 3.2.0.3 | Specify the version of the SigTest for 2.5 GT/s System Tests. Setting is defined according to Data Rate. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Configure | SigTest Version | System_SigTestVer32GT | (Accepts user-defined text), 5.1.04 | Specify the version of the SigTest for 32.0 GT/s System Tests. Setting is defined according to Data Rate. |
| Configure | SigTest Version | System_SigTestVer5GT | (Accepts user-defined text), 3.2.0.3 | Specify the version of the SigTest for 5.0 GT/s System Tests. Setting is defined according to Data Rate. |
| Configure | SigTest Version | System_SigTestVer8GT | (Accepts user-defined text), 3.2.0.3 | Specify the version of the SigTest for 8.0 GT/s System Tests. Setting is defined according to Data Rate. |
| Configure | SigTest Version (DC Calculation Method) | Preset_SigTestVer32GT_DC | (Accepts user-defined text), 4.0.52 | Specify the version of the SigTest for 32.0 GT/s Base Transmitter Tests (Equalization Preset Test) with DC calculation method. Setting is defined according to Data Rate. |
| Configure | Sine(x)/x Interpolation | SineXInterpolation_16G | ON, OFF, INT1, INT2, INT4 | Sine(x)/x Interpolation for data rate 16GT/s. If "Use Real Edge Connection" is enabled, interpolation will be set to OFF since Real-Edge connection already uses a high sample rate of 160GSa/s. Note: Interpolation shouldn't be applied to PWJ tests if Number of UI, Sample Rate and Noise Reduction BW are not set to default values as it will cause Sigtest to have memory allocation issue. |
| Configure | Sine(x)/x Interpolation | SineXInterpolation_2P5G | ON, OFF, INT1, INT2, INT4 | Sine(x)/x Interpolation for data rate 2.5GT/s. If "Use Real Edge Connection" is enabled, interpolation will be set to OFF since Real-Edge connection already uses a high sample rate of 160GSa/s. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Configure | Sine(x)/x Interpolation | SineXInterpolation_32G | ON, OFF, INT1, INT2, INT4 | Sine(x)/x Interpolation for data rate 32GT/s. If "Use Real Edge Connection" is enabled, interpolation will be set to OFF since Real-Edge connection already uses a high sample rate of 160GSa/s. |
| Configure | Sine(x)/x Interpolation | SineXInterpolation_5G | ON, OFF, INT1, INT2, INT4 | Sine(x)/x Interpolation for data rate 5GT/s. If "Use Real Edge Connection" is enabled, interpolation will be set to OFF since Real-Edge connection already uses a high sample rate of 160GSa/s. |
| Configure | Sine(x)/x Interpolation | SineXInterpolation_64G | ON, OFF, INT1, INT2, INT4 | Sine(x)/x Interpolation for data rate 64GT/s. |
| Configure | Sine(x)/x Interpolation | SineXInterpolation_64G | ON, OFF, INT1, INT2, INT4 | Sine(x)/x Interpolation for data rate 64GT/s. If "Use Real Edge Connection" is enabled, interpolation will be set to OFF since Real-Edge connection already uses a high sample rate of 160GSa/s. |
| Configure | Sine(x)/x Interpolation | SineXInterpolation_8G | ON, OFF, INT1, INT2, INT4 | Sine(x)/x Interpolation for data rate 8GT/s. If "Use Real Edge Connection" is enabled, interpolation will be set to OFF since Real-Edge connection already uses a high sample rate of 160GSa/s. |
| Configure | Use Real Edge Connection | UseRealEdgeConnection | Enabled, Disabled | Use the Real Edge Channels when performing tests for 32GT/s data rate. By default Real-Edge Connection will be disabled. |
| Configure | Voltage Test Histogram Window | VoltageHistogramWindow2 P5G_BASE | (Accepts user-defined text in Debug mode), 0.01, 0.1 | Specify the histogram window from centre 0.5 UI to use for 2.5GT/s Base Transmitter Tests (Deemphasized Voltage Ratio Test and Peak Differential Output Voltage Test only). By default, +-0.01 UI window from centre 0.5 UI is used. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Configure | Voltage Test Histogram Window | VoltageHistogramWindow2P5G_EP | (Accepts user-defined text in Debug mode), 0.01, 0.1 | Specify the histogram window from centre 0.5 UI to use for 2.5GT/s End Point Tests (Deemphasized Voltage Ratio Test and Peak Differential Output Voltage Test only). By default, +-0.01 UI window from centre 0.5 UI is used. |
| Configure | Voltage Test Histogram Window | VoltageHistogramWindow2P5G_RC | (Accepts user-defined text in Debug mode), 0.01, 0.1 | Specify the histogram window from centre 0.5 UI to use for 2.5GT/s Root Complex Tests (Deemphasized Voltage Ratio Test and Peak Differential Output Voltage Test only). By default, +-0.01 UI window from centre 0.5 UI is used. |
| Configure | Voltage Test Histogram Window | VoltageHistogramWindow5G_BASE | (Accepts user-defined text in Debug mode), 0.01, 0.1 | Specify the histogram window from centre 0.5 UI to use for 5GT/s Base Transmitter Tests (Deemphasized Voltage Ratio Test and Peak Differential Output Voltage Test only). By default, +-0.01 UI window from centre 0.5 UI is used. |
| Configure | Voltage Test Histogram Window | VoltageHistogramWindow5G_EP | (Accepts user-defined text in Debug mode), 0.01, 0.1 | Specify the histogram window from centre 0.5 UI to use for 5GT/s End Point Tests (Deemphasized Voltage Ratio Test and Peak Differential Output Voltage Test only). By default, +-0.01 UI window from centre 0.5 UI is used. |
| Configure | Voltage Test Histogram Window | VoltageHistogramWindow5G_RC | (Accepts user-defined text in Debug mode), 0.01, 0.1 | Specify the histogram window from centre 0.5 UI to use for 5GT/s Root Complex Tests (Deemphasized Voltage Ratio Test and Peak Differential Output Voltage Test only). By default, +-0.01 UI window from centre 0.5 UI is used. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Configure | Voltage Test Interpolation Ratio | VoltageInterpolationRatio2P5G_BASE | OFF, INT2, INT4 | Specify the interpolation ratio during load waveform to use for 2.5GT/s Base Transmitter Tests (Deemphasized Voltage Ratio and Peak Differential Output Voltage Test only). By default, interpolation ratio of 4 is used. |
| Configure | Voltage Test Interpolation Ratio | VoltageInterpolationRatio2P5G_EP | OFF, INT2, INT4 | Specify the interpolation ratio during load waveform to use for 2.5GT/s End Point Tests (Deemphasized Voltage Ratio and Peak Differential Output Voltage Test only). By default, interpolation ratio of 4 is used. |
| Configure | Voltage Test Interpolation Ratio | VoltageInterpolationRatio2P5G_RC | OFF, INT2, INT4 | Specify the interpolation ratio during load waveform to use for 2.5GT/s Root Complex Tests (Deemphasized Voltage Ratio and Peak Differential Output Voltage Test only). By default, interpolation ratio of 4 is used. |
| Configure | Voltage Test Interpolation Ratio | VoltageInterpolationRatio5G_BASE | OFF, INT2, INT4 | Specify the interpolation ratio during load waveform to use for 5GT/s Base Transmitter Tests (Deemphasized Voltage Ratio and Peak Differential Output Voltage Test only). By default, interpolation ratio of 4 is used. |
| Configure | Voltage Test Interpolation Ratio | VoltageInterpolationRatio5G_EP | OFF, INT2, INT4 | Specify the interpolation ratio during load waveform to use for 5GT/s End Point Tests (Deemphasized Voltage Ratio and Peak Differential Output Voltage Test only). By default, interpolation ratio of 4 is used. |
| Configure | Voltage Test Interpolation Ratio | VoltageInterpolationRatio5G_RC | OFF, INT2, INT4 | Specify the interpolation ratio during load waveform to use for 5GT/s Root Complex Tests (Deemphasized Voltage Ratio and Peak Differential Output Voltage Test only). By default, interpolation ratio of 4 is used. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Configure | Voltage Test Measurement Method | VoltageMeasurementMethod2P5G_BASE | SigTest, Infiniium | Specify the measurement method to use for 2.5GT/s Base Transmitter Tests (Deemphasized Voltage Ratio Test and Peak Differential Output Voltage Test only). By default, SigTest is used for the measurement. |
| Configure | Voltage Test Measurement Method | VoltageMeasurementMethod2P5G_EP | SigTest, Infiniium | Specify the measurement method to use for 2.5GT/s CEM End Point Tests (Deemphasized Voltage Ratio Test and Peak Differential Output Voltage Test only). By default, SigTest is used for the measurement. |
| Configure | Voltage Test Measurement Method | VoltageMeasurementMethod2P5G_RC | SigTest, Infiniium | Specify the measurement method to use for 2.5GT/s CEM Root Complex Tests (Deemphasized Voltage Ratio Test and Peak Differential Output Voltage Test only). By default, SigTest is used for the measurement. |
| Configure | Voltage Test Measurement Method | VoltageMeasurementMethod5G_BASE | SigTest, Infiniium | Specify the measurement method to use for 5GT/s Base Transmitter Tests (Deemphasized Voltage Ratio Test and Peak Differential Output Voltage Test only). By default, SigTest is used for the measurement. |
| Configure | Voltage Test Measurement Method | VoltageMeasurementMethod5G_EP | SigTest, Infiniium | Specify the measurement method to use for 5GT/s CEM End Point Tests (Deemphasized Voltage Ratio Test and Peak Differential Output Voltage Test only). By default, SigTest is used for the measurement. |
| Configure | Voltage Test Measurement Method | VoltageMeasurementMethod5G_RC | SigTest, Infiniium | Specify the measurement method to use for 5GT/s CEM Root Complex Tests (Deemphasized Voltage Ratio Test and Peak Differential Output Voltage Test only). By default, SigTest is used for the measurement. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Run Tests | Event | RunEvent | (None), Fail, Margin < N, Pass | Names of events that can be used with the StoreMode=Event or RunUntil RunEventAction options |
| Run Tests | RunEvent=Margin < N: Minimum required margin % | RunEvent_Margin < N_MinPercent | Any integer in range: 0 <= value <= 99 | Specify N using the 'Minimum required margin %' control. |
| Set Up | 16GT/s Preset P0 | 16G P00 | 0.0, 1.0 | Enable 16GT/s Preset P0. |
| Set Up | 16GT/s Preset P1 | 16G P01 | 0.0, 1.0 | Enable 16GT/s Preset P1. |
| Set Up | 16GT/s Preset P10 | 16G P10 | 0.0, 1.0 | Enable 16GT/s Preset P10. |
| Set Up | 16GT/s Preset P2 | 16G P02 | 0.0, 1.0 | Enable 16GT/s Preset P2. |
| Set Up | 16GT/s Preset P3 | 16G P03 | 0.0, 1.0 | Enable 16GT/s Preset P3. |
| Set Up | 16GT/s Preset P4 | 16G P04 | 0.0, 1.0 | Enable 16GT/s Preset P4. |
| Set Up | 16GT/s Preset P5 | 16G P05 | 0.0, 1.0 | Enable 16GT/s Preset P5. |
| Set Up | 16GT/s Preset P6 | 16G P06 | 0.0, 1.0 | Enable 16GT/s Preset P6. |
| Set Up | 16GT/s Preset P7 | 16G P07 | 0.0, 1.0 | Enable 16GT/s Preset P7. |
| Set Up | 16GT/s Preset P8 | 16G P08 | 0.0, 1.0 | Enable 16GT/s Preset P8. |
| Set Up | 16GT/s Preset P9 | 16G P09 | 0.0, 1.0 | Enable 16GT/s Preset P9. |
| Set Up | 32GT/s Preset P0 | 32G P00 | 0.0, 1.0 | Enable 32GT/s Preset P0. |
| Set Up | 32GT/s Preset P1 | 32G P01 | 0.0, 1.0 | Enable 32GT/s Preset P1. |
| Set Up | 32GT/s Preset P10 | 32G P10 | 0.0, 1.0 | Enable 32GT/s Preset P10. |
| Set Up | 32GT/s Preset P2 | 32G P02 | 0.0, 1.0 | Enable 32GT/s Preset P2. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Set Up | 32GT/s Preset P3 | 32G P03 | 0.0, 1.0 | Enable 32GT/s Preset P3. |
| Set Up | 32GT/s Preset P4 | 32G P04 | 0.0, 1.0 | Enable 32GT/s Preset P4. |
| Set Up | 32GT/s Preset P5 | 32G P05 | 0.0, 1.0 | Enable 32GT/s Preset P5. |
| Set Up | 32GT/s Preset P6 | 32G P06 | 0.0, 1.0 | Enable 32GT/s Preset P6. |
| Set Up | 32GT/s Preset P7 | 32G P07 | 0.0, 1.0 | Enable 32GT/s Preset P7. |
| Set Up | 32GT/s Preset P8 | 32G P08 | 0.0, 1.0 | Enable 32GT/s Preset P8. |
| Set Up | 32GT/s Preset P9 | 32G P09 | 0.0, 1.0 | Enable 32GT/s Preset P9. |
| Set Up | 64GT/s Preset P0 | 64G Q00 | 0.0, 1.0 | Enable 64GT/s Preset P0. |
| Set Up | 64GT/s Preset P1 | 64G Q01 | 0.0, 1.0 | Enable 64GT/s Preset P1. |
| Set Up | 64GT/s Preset P10 | 64G Q10 | 0.0, 1.0 | Enable 64GT/s Preset P10. |
| Set Up | 64GT/s Preset P2 | 64G Q02 | 0.0, 1.0 | Enable 64GT/s Preset P2. |
| Set Up | 64GT/s Preset P3 | 64G Q03 | 0.0, 1.0 | Enable 64GT/s Preset P3. |
| Set Up | 64GT/s Preset P4 | 64G Q04 | 0.0, 1.0 | Enable 64GT/s Preset P4. |
| Set Up | 64GT/s Preset P5 | 64G Q05 | 0.0, 1.0 | Enable 64GT/s Preset P5. |
| Set Up | 64GT/s Preset P6 | 64G Q06 | 0.0, 1.0 | Enable 64GT/s Preset P6. |
| Set Up | 64GT/s Preset P7 | 64G Q07 | 0.0, 1.0 | Enable 64GT/s Preset P7. |
| Set Up | 64GT/s Preset P8 | 64G Q08 | 0.0, 1.0 | Enable 64GT/s Preset P8. |
| Set Up | 64GT/s Preset P9 | 64G Q09 | 0.0, 1.0 | Enable 64GT/s Preset P9. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Set Up | 8GT/s Preset P0 | 8G P00 | 0.0, 1.0 | Enable 8GT/s Preset P0. |
| Set Up | 8GT/s Preset P1 | 8G P01 | 0.0, 1.0 | Enable 8GT/s Preset P1. |
| Set Up | 8GT/s Preset P10 | 8G P10 | 0.0, 1.0 | Enable 8GT/s Preset P10. |
| Set Up | 8GT/s Preset P2 | 8G P02 | 0.0, 1.0 | Enable 8GT/s Preset P2. |
| Set Up | 8GT/s Preset P3 | 8G P03 | 0.0, 1.0 | Enable 8GT/s Preset P3. |
| Set Up | 8GT/s Preset P4 | 8G P04 | 0.0, 1.0 | Enable 8GT/s Preset P4. |
| Set Up | 8GT/s Preset P5 | 8G P05 | 0.0, 1.0 | Enable 8GT/s Preset P5. |
| Set Up | 8GT/s Preset P6 | 8G P06 | 0.0, 1.0 | Enable 8GT/s Preset P6. |
| Set Up | 8GT/s Preset P7 | 8G P07 | 0.0, 1.0 | Enable 8GT/s Preset P7. |
| Set Up | 8GT/s Preset P8 | 8G P08 | 0.0, 1.0 | Enable 8GT/s Preset P8. |
| Set Up | 8GT/s Preset P9 | 8G P09 | 0.0, 1.0 | Enable 8GT/s Preset P9. |
| Set Up | All CTLE Equalization | CTLE32GAlldB | 0.0, 1.0 | Enable/disable All CTLE Equalization. |
| Set Up | All CTLE Equalization | CTLE64GJitter52UIAlldB | 0.0, 1.0 | Enable/disable All CTLE Equalization. |
| Set Up | All CTLE Equalization | CTLE64GPWJAlldB | 0.0, 1.0 | Enable/disable All CTLE Equalization. |
| Set Up | Auto Tune CTLE Equalization | CTLE64GJitter52UIAutoTunedB | 0.0, 1.0 | Enable/disable Auto Tune CTLE Equalization. |
| Set Up | Auto Tune CTLE Equalization | CTLE64GPWJAutoTunedB | 0.0, 1.0 | Enable/disable Auto Tune CTLE Equalization. |
| Set Up | Browse for the Jitter pattern file. | JitterBrowseConfigVar | 1 | This button is to browse for the Jitter pattern file. Browse for the Jitter pattern file. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Set Up | Browse for the compliance pattern file. | ComplianceBrowseConfigVar | 1 | This button is to browse for the compliance pattern file. Browse for the compliance pattern file. |
| Set Up | CTLE 10dB Embedding | CTLE32G10dB | 0.0, 1.0 | Enable CTLE 10dB Embedding. |
| Set Up | CTLE 10dB Embedding | CTLE64GJitter52UI10dB | 0.0, 1.0 | Enable CTLE 10dB Embedding. |
| Set Up | CTLE 10dB Embedding | CTLE64GPWJ10dB | 0.0, 1.0 | Enable CTLE 10dB Embedding. |
| Set Up | CTLE 11dB Embedding | CTLE32G11dB | 0.0, 1.0 | Enable CTLE 11dB Embedding. |
| Set Up | CTLE 11dB Embedding | CTLE64GJitter52UI11dB | 0.0, 1.0 | Enable CTLE 11dB Embedding. |
| Set Up | CTLE 11dB Embedding | CTLE64GPWJ11dB | 0.0, 1.0 | Enable CTLE 11dB Embedding. |
| Set Up | CTLE 12dB Embedding | CTLE32G12dB | 0.0, 1.0 | Enable CTLE 12dB Embedding. |
| Set Up | CTLE 12dB Embedding | CTLE64GJitter52UI12dB | 0.0, 1.0 | Enable CTLE 12dB Embedding. |
| Set Up | CTLE 12dB Embedding | CTLE64GPWJ12dB | 0.0, 1.0 | Enable CTLE 12dB Embedding. |
| Set Up | CTLE 13dB Embedding | CTLE32G13dB | 0.0, 1.0 | Enable CTLE 13dB Embedding. |
| Set Up | CTLE 13dB Embedding | CTLE64GJitter52UI13dB | 0.0, 1.0 | Enable CTLE 13dB Embedding. |
| Set Up | CTLE 13dB Embedding | CTLE64GPWJ13dB | 0.0, 1.0 | Enable CTLE 13dB Embedding. |
| Set Up | CTLE 14dB Embedding | CTLE32G14dB | 0.0, 1.0 | Enable CTLE 14dB Embedding. |
| Set Up | CTLE 14dB Embedding | CTLE64GJitter52UI14dB | 0.0, 1.0 | Enable CTLE 14dB Embedding. |
| Set Up | CTLE 14dB Embedding | CTLE64GPWJ14dB | 0.0, 1.0 | Enable CTLE 14dB Embedding. |
| Set Up | CTLE 15dB Embedding | CTLE32G15dB | 0.0, 1.0 | Enable CTLE 15dB Embedding. |
| Set Up | CTLE 15dB Embedding | CTLE64GJitter52UI15dB | 0.0, 1.0 | Enable CTLE 15dB Embedding. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Set Up | CTLE 15dB Embedding | CTLE64GPWJ15dB | 0.0, 1.0 | Enable CTLE 15dB Embedding. |
| Set Up | CTLE 5dB Embedding | CTLE32G5dB | 0.0, 1.0 | Enable CTLE 5dB Embedding. |
| Set Up | CTLE 5dB Embedding | CTLE64GJitter52UI5dB | 0.0, 1.0 | Enable CTLE 5dB Embedding. |
| Set Up | CTLE 5dB Embedding | CTLE64GPWJ5dB | 0.0, 1.0 | Enable CTLE 5dB Embedding. |
| Set Up | CTLE 6dB Embedding | CTLE32G6dB | 0.0, 1.0 | Enable CTLE 6dB Embedding. |
| Set Up | CTLE 6dB Embedding | CTLE64GJitter52UI6dB | 0.0, 1.0 | Enable CTLE 6dB Embedding. |
| Set Up | CTLE 6dB Embedding | CTLE64GPWJ6dB | 0.0, 1.0 | Enable CTLE 6dB Embedding. |
| Set Up | CTLE 7dB Embedding | CTLE32G7dB | 0.0, 1.0 | Enable CTLE 7dB Embedding. |
| Set Up | CTLE 7dB Embedding | CTLE64GJitter52UI7dB | 0.0, 1.0 | Enable CTLE 7dB Embedding. |
| Set Up | CTLE 7dB Embedding | CTLE64GPWJ7dB | 0.0, 1.0 | Enable CTLE 7dB Embedding. |
| Set Up | CTLE 8dB Embedding | CTLE32G8dB | 0.0, 1.0 | Enable CTLE 8dB Embedding. |
| Set Up | CTLE 8dB Embedding | CTLE64GJitter52UI8dB | 0.0, 1.0 | Enable CTLE 8dB Embedding. |
| Set Up | CTLE 8dB Embedding | CTLE64GPWJ8dB | 0.0, 1.0 | Enable CTLE 8dB Embedding. |
| Set Up | CTLE 9dB Embedding | CTLE32G9dB | 0.0, 1.0 | Enable CTLE 9dB Embedding. |
| Set Up | CTLE 9dB Embedding | CTLE64GJitter52UI9dB | 0.0, 1.0 | Enable CTLE 9dB Embedding. |
| Set Up | CTLE 9dB Embedding | CTLE64GPWJ9dB | 0.0, 1.0 | Enable CTLE 9dB Embedding. |
| Set Up | Calibrate scope noise for PWJ (L0-L3) pattern | CalPwj | 0.0, 1.0 | Calibrate scope noise for PWJ (L0-L3) pattern. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Set Up | Calibrate scope noise for all pattern | CalibrateAll | 0.0, 1.0 | Calibrate scope noise for all pattern. |
| Set Up | Calibrate scope noise for compliance pattern Q0 | CalQ0 | 0.0, 1.0 | Calibrate scope noise for compliance pattern Q0. |
| Set Up | Calibrate scope noise for jitter pattern | CalJitter | 0.0, 1.0 | Calibrate scope noise for jitter pattern. |
| Set Up | Calibration Handling Option | CalHandlingOpt | Run calibration, Ignore missing scope noise | Select the Scope Noise Calibration Handling Option. Select the Scope Noise Calibration Handling Option |
| Set Up | Calibration Option | ScopeNoiseOpt | Enable, Disable | Select the option of Compensate for Scope Noise. Select the option of Compensate for Scope Noise |
| Set Up | Clear for Jitter pattern file selection. | JitterClearConfigVar | 1 | This button is to clear the selected Jitter pattern file. Clear for Jitter pattern file selection. |
| Set Up | Clear for compliance pattern file selection. | ComplianceClearConfigVar | 1 | This button is to clear the selected compliance pattern file. Clear for compliance pattern file selection. |
| Set Up | Connect to 81150A/8116 0A (PFAG) now. | ConnectNowButton | 1 | Connect to 81150A/81160A (PFAG) is required before starts DUT Automation. Connect to 81150A/81160A (PFAG) now. |
| Set Up | Connection Differential Partner | OptConnectionDifferentialPa rtner | Every Other Channel, Adjacent Channels | Select Connection Differential Partner. |
| Set Up | Connection Type | OptConnectionType | Single-Ended, Differential | Select Connection Type. |
| Set Up | Deselect all 16GT/s presets. | DeselectAllPreset16GConfig Var | 1 | This button is to deselect all 16GT/s presets. Deselect all 16GT/s presets. |
| Set Up | Deselect all 32GT/s presets. | DeselectAllPreset32GConfig Var | 1 | This button is to deselect all 32GT/s presets. Deselect all 32GT/s presets. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Set Up | Deselect all 64GT/s presets. | DeselectAllPreset64GConfigVar | 1 | This button is to deselect all 64GT/s presets. Deselect all 64GT/s presets. |
| Set Up | Deselect all 8GT/s presets. | DeselectAllPreset8GConfigVar | 1 | This button is to deselect all 8GT/s presets. Deselect all 8GT/s presets. |
| Set Up | Device Directory | OfflineDeviceDirectoryName | New Device1 | Available directories to run Analyze Captured Waveforms operation. |
| Set Up | Device Name | DeviceName | (Accepts user-defined text) | Name for the DUT in testing. |
| Set Up | DevicePCIERev | DevicePCIERev | PCIE 4.0, PCIE 5.0, PCIE 6.0 | Select the PCI Express device specification to use. |
| Set Up | Enable Collective Data Acquisition | PresetWfmCollectiveAcqConfigVar | 0.0, 1.0 | Enable Collective Data Acquisition. |
| Set Up | Enable DUT Automation | DutAutomation | 0.0, 1.0 | Enable DUT Automation. |
| Set Up | Enable Workshop Compliance Mode | Workshop Compliance Mode | 0.0, 1.0 | Enable Workshop Compliance Mode. |
| Set Up | IP Address of 81150A/81160A (PFAG) | PFAGIPAddress | (Accepts user-defined text) | Speficies the IP address of 81150A/81160A (PFAG). Speficies the IP address of 81150A/81160A (PFAG) |
| Set Up | Manual Input Compliance Pattern File Directory | ManualInputCompliancePatternFileDirectory | (Accepts user-defined text) | Directory of manual input Compliance pattern file. |
| Set Up | Manual Input Jitter Pattern File Directory | ManualInputJitterPatternFileDirectory | (Accepts user-defined text) | Directory of manual input Jitter pattern file. |
| Set Up | OfflineDataLane | cbOfflineDataLane | 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12, 13, 14, 15 | |
| Set Up | OfflineDataRate | OfflineDataRate | 2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s, 32.0 GT/s, 64.0 GT/s | |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Set Up | OfflineDeemphasis | OfflineDeemphasis | -3.5dB, -6.0dB | |
| Set Up | OfflinePowerLevel | cbOfflinePowerLevel | Full, Half | |
| Set Up | OfflinePreset | OfflinePreset | Q00, Q01, Q02, Q03, Q04, Q05, Q06, Q07, Q08, Q09, Q10, PWJClock, JitterData, HighLowSwingData | |
| Set Up | OfflineRefClk | cbOfflineRefClk | Clean Clock, SSC | |
| Set Up | OfflineSRIS | cbOfflineSRIS | None, Enabled | |
| Set Up | OfflineSignalType | OfflineSignalType | Data, UI03, UI12 | |
| Set Up | OfflineTestPoint | cbOfflineTestPoint | Base - Transmitter Tests, CEM - End Point Tests, CEM - Root Complex Tests, Reference Clock Tests | |
| Set Up | OfflineTestPointChannel | cbOfflineTestPointChannel | Min, Max | |
| Set Up | PFAG Connection Option | PFAGConnectionOpt | IP Address, SICL Address | Select the PFAG Connection Option. Select the PFAG Connection Option |
| Set Up | Perform Done operation to apply all setting changes. | DoneConnectionSetupConfigVar | 1 | This button is required to click/set in order to apply on all the settings have been set in this Connection Setup window. Perform Done operation to apply all setting changes. |
| Set Up | Perform Done operation to apply all setting changes. | DoneDeviceDefConfigVar | 1 | This button is required to click/set in order to apply on all the settings have been set in this Device Definition window. Perform Done operation to apply all setting changes. |
| Set Up | Perform Done operation to apply all setting changes. | DoneScopeNoiseCalibrationSetupConfigVar | 1 | This button is required to click/set in order to apply on all the settings have been set in this Scope Noise Calibration Setup window. Perform Done operation to apply all setting changes. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Set Up | Perform scope noise calibration. | StartScopeNoiseCalibration ConfigVar | 1 | This button is required to start to calibrate scope noise operation. Perform scope noise calibration. |
| Set Up | SICL Address of 81150A/8116 0A (PFAG) | PFAGSiclAddress | (Accepts user-defined text) | Speficies the SICL address of 81150A/81160A (PFAG). Speficies the SICL address of 81150A/81160A (PFAG) |
| Set Up | Saved Files Directory | SavedFilesDirectory | (Accepts user-defined text) | Directory to save output files from Workshop Mode Test. |
| Set Up | Select 16.0 GT/s related tests | 16.0 GT/s | 0.0, 1.0 | Select 16.0 GT/s related tests. |
| Set Up | Select 2.5 GT/s related tests | 2.5 GT/s | 0.0, 1.0 | Select 2.5 GT/s related tests. |
| Set Up | Select 32.0 GT/s related tests | 32.0 GT/s | 0.0, 1.0 | Select 32.0 GT/s related tests. |
| Set Up | Select 5.0 GT/s related tests | 5.0 GT/s | 0.0, 1.0 | Select 5.0 GT/s related tests. |
| Set Up | Select 64.0 GT/s related tests | 64.0 GT/s | 0.0, 1.0 | Select 64.0 GT/s related tests. |
| Set Up | Select 8.0 GT/s related tests | 8.0 GT/s | 0.0, 1.0 | Select 8.0 GT/s related tests. |
| Set Up | Select De-Emphasis -3.5dB for data speed 5GT/s | DeEmphasis3P5dBConfigVar | 0.0, 1.0 | Select De-Emphasis -3.5dB for data speed 5GT/s Select De-Emphasis -3.5dB for data speed 5GT/s |
| Set Up | Select De-Emphasis -6.0dB for data speed 5GT/s | DeEmphasis6P0dBConfigVar | 0.0, 1.0 | Select De-Emphasis -6.0dB for data speed 5GT/s Select De-Emphasis -6.0dB for data speed 5GT/s |
| Set Up | Select Lane 0 | Lane0 | 0.0, 1.0 | Select Lane 0 Select Lane 0 |
| Set Up | Select Lane 1 | Lane1 | 0.0, 1.0 | Select Lane 1 Select Lane 1 |
| Set Up | Select Lane 10 | Lane10 | 0.0, 1.0 | Select Lane 10 Select Lane 10 |
| Set Up | Select Lane 11 | Lane11 | 0.0, 1.0 | Select Lane 11 Select Lane 11 |
| Set Up | Select Lane 12 | Lane12 | 0.0, 1.0 | Select Lane 12 Select Lane 12 |
| Set Up | Select Lane 13 | Lane13 | 0.0, 1.0 | Select Lane 13 Select Lane 13 |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Set Up | Select Lane 14 | Lane14 | 0.0, 1.0 | Select Lane 14 Select Lane 14 |
| Set Up | Select Lane 15 | Lane15 | 0.0, 1.0 | Select Lane 15 Select Lane 15 |
| Set Up | Select Lane 2 | Lane2 | 0.0, 1.0 | Select Lane 2 Select Lane 2 |
| Set Up | Select Lane 3 | Lane3 | 0.0, 1.0 | Select Lane 3 Select Lane 3 |
| Set Up | Select Lane 4 | Lane4 | 0.0, 1.0 | Select Lane 4 Select Lane 4 |
| Set Up | Select Lane 5 | Lane5 | 0.0, 1.0 | Select Lane 5 Select Lane 5 |
| Set Up | Select Lane 6 | Lane6 | 0.0, 1.0 | Select Lane 6 Select Lane 6 |
| Set Up | Select Lane 7 | Lane7 | 0.0, 1.0 | Select Lane 7 Select Lane 7 |
| Set Up | Select Lane 8 | Lane8 | 0.0, 1.0 | Select Lane 8 Select Lane 8 |
| Set Up | Select Lane 9 | Lane9 | 0.0, 1.0 | Select Lane 9 Select Lane 9 |
| Set Up | Select Switch Matrix. | optSwitchMatrix | No Switch Matrix, BitifEye BIT 2100, Keysight U3020A S26 | Select SwitchMatrix. |
| Set Up | Select all 16GT/s presets. | SelectAllPreset16GConfigVar | 1 | This button is to select all 16GT/s presets. Select all 16GT/s presets. |
| Set Up | Select all 32GT/s presets. | SelectAllPreset32GConfigVar | 1 | This button is to select all 32GT/s presets. Select all 32GT/s presets. |
| Set Up | Select all 64GT/s presets. | SelectAllPreset64GConfigVar | 1 | This button is to select all 64GT/s presets. Select all 64GT/s presets. |
| Set Up | Select all 8GT/s presets. | SelectAllPreset8GConfigVar | 1 | This button is to select all 8GT/s presets. Select all 8GT/s presets. |
| Set Up | Select clock channel | DiffClockChannelConfigVar | Channel-1, Channel-2, Channel-3, Channel-4 | Select clock channel |
| Set Up | Select clock channel + | SingleEndedClockChannelPConfigVar | Channel-1, Channel-2 | Select clock channel +. |
| Set Up | Select clock channel - | SingleEndedClockChannelNConfigVar | Channel-3, Channel-4 | Select clock channel -. |
| Set Up | Select data channel | DiffDataChannelConfigVar | Channel-1, Channel-2, Channel-3, Channel-4 | Select data channel |
| Set Up | Select data channel + | SingleEndedDataChannelPConfigVar | Channel-1, Channel-2 | Select data channel +. |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Set Up | Select data channel - | SingleEndedDataChannelNConfigVar | Channel-3, Channel-4 | Select data channel -. |
| Set Up | Select if DUT is enable lane reversal | ChkReverseLaneDUT | 0.0, 1.0 | Select if DUT is enable lane reversal. |
| Set Up | Select switching modules in BIT2100 Frame. | BIT2100Modules | 2xSP4T, 2xSP6T, 2xSP8T | Select switching modules in BIT2100 Frame. |
| Set Up | Select the Power Level. | PowerLevelConfigVar | Full, Half | Select the Power Level. |
| Set Up | Select the Reference Clock Type. | RefClkConfigVar | Clean Clock, SSC | Select the Reference Clock Type. |
| Set Up | Select the SRIS type. | SRISEnabledConfigVar | None, Enabled | Select the SRIS type. |
| Set Up | Setup toggle source now. | ToggleSetupButton | 1 | Setup the toggle source for DUT Automation now. Setup toggle source now. |
| Set Up | Test Point | TestPoint | Base - Transmitter Tests, CEM - End Point Tests, CEM - Root Complex Tests, Reference Clock Tests | Select the PCIExpress device test point to be tested. |
| Set Up | Test Point Preset Test | TestPointPresetTest | 0.0, 1.0 | Select to run Equalization Preset Tests. |
| Set Up | Toggle Source | ToggleSourceOpt | 81150A / 81160A, CAL OUT (100MHz) | Select the toggle source to toggle your DUT. Select the toggle source to toggle your DUT |
| Set Up | Transfer Function Path for 32GT/s Lane 0 | TFPath32GLane0 | -, NRC_TL_5dB.tf4, NRC_TL_5p5dB.tf4, NRC_TL_6dB.tf4, NRC_TL_6p5dB.tf4, NRC_TL_7dB.tf4, NRC_TL_7p5dB.tf4 | Transfer Function Path for 32GT/s Lane 0 Transfer Function Path for 32GT/s Lane 0 |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Set Up | Transfer Function Path for 32GT/s Lane 1 | TFPath32GLane1 | -, NRC_TL_5dB.tf4, NRC_TL_5p5dB.tf4, NRC_TL_6dB.tf4, NRC_TL_6p5dB.tf4, NRC_TL_7dB.tf4, NRC_TL_7p5dB.tf4 | Transfer Function Path for 32GT/s Lane 1 Transfer Function Path for 32GT/s Lane 1 |
| Set Up | Transfer Function Path for 32GT/s Lane 10 | TFPath32GLane10 | -, NRC_TL_5dB.tf4, NRC_TL_5p5dB.tf4, NRC_TL_6dB.tf4, NRC_TL_6p5dB.tf4, NRC_TL_7dB.tf4, NRC_TL_7p5dB.tf4 | Transfer Function Path for 32GT/s Lane 10 Transfer Function Path for 32GT/s Lane 10 |
| Set Up | Transfer Function Path for 32GT/s Lane 11 | TFPath32GLane11 | -, NRC_TL_5dB.tf4, NRC_TL_5p5dB.tf4, NRC_TL_6dB.tf4, NRC_TL_6p5dB.tf4, NRC_TL_7dB.tf4, NRC_TL_7p5dB.tf4 | Transfer Function Path for 32GT/s Lane 11 Transfer Function Path for 32GT/s Lane 11 |
| Set Up | Transfer Function Path for 32GT/s Lane 12 | TFPath32GLane12 | -, NRC_TL_5dB.tf4, NRC_TL_5p5dB.tf4, NRC_TL_6dB.tf4, NRC_TL_6p5dB.tf4, NRC_TL_7dB.tf4, NRC_TL_7p5dB.tf4 | Transfer Function Path for 32GT/s Lane 12 Transfer Function Path for 32GT/s Lane 12 |
| Set Up | Transfer Function Path for 32GT/s Lane 13 | TFPath32GLane13 | -, NRC_TL_5dB.tf4, NRC_TL_5p5dB.tf4, NRC_TL_6dB.tf4, NRC_TL_6p5dB.tf4, NRC_TL_7dB.tf4, NRC_TL_7p5dB.tf4 | Transfer Function Path for 32GT/s Lane 13 Transfer Function Path for 32GT/s Lane 13 |
| Set Up | Transfer Function Path for 32GT/s Lane 14 | TFPath32GLane14 | -, NRC_TL_5dB.tf4, NRC_TL_5p5dB.tf4, NRC_TL_6dB.tf4, NRC_TL_6p5dB.tf4, NRC_TL_7dB.tf4, NRC_TL_7p5dB.tf4 | Transfer Function Path for 32GT/s Lane 14 Transfer Function Path for 32GT/s Lane 14 |
| Set Up | Transfer Function Path for 32GT/s Lane 15 | TFPath32GLane15 | -, NRC_TL_5dB.tf4, NRC_TL_5p5dB.tf4, NRC_TL_6dB.tf4, NRC_TL_6p5dB.tf4, NRC_TL_7dB.tf4, NRC_TL_7p5dB.tf4 | Transfer Function Path for 32GT/s Lane 15 Transfer Function Path for 32GT/s Lane 15 |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Set Up | Transfer Function Path for 32GT/s Lane 2 | TFPath32GLane2 | -, NRC_TL_5dB.tf4, NRC_TL_5p5dB.tf4, NRC_TL_6dB.tf4, NRC_TL_6p5dB.tf4, NRC_TL_7dB.tf4, NRC_TL_7p5dB.tf4 | Transfer Function Path for 32GT/s Lane 2 Transfer Function Path for 32GT/s Lane 2 |
| Set Up | Transfer Function Path for 32GT/s Lane 3 | TFPath32GLane3 | -, NRC_TL_5dB.tf4, NRC_TL_5p5dB.tf4, NRC_TL_6dB.tf4, NRC_TL_6p5dB.tf4, NRC_TL_7dB.tf4, NRC_TL_7p5dB.tf4 | Transfer Function Path for 32GT/s Lane 3 Transfer Function Path for 32GT/s Lane 3 |
| Set Up | Transfer Function Path for 32GT/s Lane 4 | TFPath32GLane4 | -, NRC_TL_5dB.tf4, NRC_TL_5p5dB.tf4, NRC_TL_6dB.tf4, NRC_TL_6p5dB.tf4, NRC_TL_7dB.tf4, NRC_TL_7p5dB.tf4 | Transfer Function Path for 32GT/s Lane 4 Transfer Function Path for 32GT/s Lane 4 |
| Set Up | Transfer Function Path for 32GT/s Lane 5 | TFPath32GLane5 | -, NRC_TL_5dB.tf4, NRC_TL_5p5dB.tf4, NRC_TL_6dB.tf4, NRC_TL_6p5dB.tf4, NRC_TL_7dB.tf4, NRC_TL_7p5dB.tf4 | Transfer Function Path for 32GT/s Lane 5 Transfer Function Path for 32GT/s Lane 5 |
| Set Up | Transfer Function Path for 32GT/s Lane 6 | TFPath32GLane6 | -, NRC_TL_5dB.tf4, NRC_TL_5p5dB.tf4, NRC_TL_6dB.tf4, NRC_TL_6p5dB.tf4, NRC_TL_7dB.tf4, NRC_TL_7p5dB.tf4 | Transfer Function Path for 32GT/s Lane 6 Transfer Function Path for 32GT/s Lane 6 |
| Set Up | Transfer Function Path for 32GT/s Lane 7 | TFPath32GLane7 | -, NRC_TL_5dB.tf4, NRC_TL_5p5dB.tf4, NRC_TL_6dB.tf4, NRC_TL_6p5dB.tf4, NRC_TL_7dB.tf4, NRC_TL_7p5dB.tf4 | Transfer Function Path for 32GT/s Lane 7 Transfer Function Path for 32GT/s Lane 7 |
| Set Up | Transfer Function Path for 32GT/s Lane 8 | TFPath32GLane8 | -, NRC_TL_5dB.tf4, NRC_TL_5p5dB.tf4, NRC_TL_6dB.tf4, NRC_TL_6p5dB.tf4, NRC_TL_7dB.tf4, NRC_TL_7p5dB.tf4 | Transfer Function Path for 32GT/s Lane 8 Transfer Function Path for 32GT/s Lane 8 |

**Table 2** Configuration Variables and Values (continued)

| GUI Location | Label | Variable | Values | Description |
|---|---|---|---|---|
| Set Up | Transfer Function Path for 32GT/s Lane 9 | TFPath32GLane9 | -, NRC_TL_5dB.tf4, NRC_TL_5p5dB.tf4, NRC_TL_6dB.tf4, NRC_TL_6p5dB.tf4, NRC_TL_7dB.tf4, NRC_TL_7p5dB.tf4 | Transfer Function Path for 32GT/s Lane 9 Transfer Function Path for 32GT/s Lane 9 |
| Set Up | Try toggle DUT now. | ToggleNowButton | 1 | Try toggle DUT to next state. Try toggle DUT now. |
| Set Up | Use Local Saved Waveform | UseLocalSavedWaveform | 0.0, 1.0 | Use Local Saved Waveform. |
| Set Up | User Comment | UserComments | (Accepts user-defined text) | Additional comments for the DUT in testing. Additional comments for the DUT in testing. |
| *Limited availability: Availability of this setting depends upon the oscilloscope model and installed license options. | | | | |

# 3 Test Names and IDs

The following table shows the mapping between each test's numeric ID and name. The numeric ID is required by various remote interface methods.

- Name – The name of the test as it appears on the user interface **Select Tests** tab.
- Test ID – The number to use with the RunTests method.
- Description – The description of the test as it appears on the user interface **Select Tests** tab.

For example, if the graphical user interface displays this tree in the **Select Tests** tab:

- All Tests
  - Rise Time
  - Fall Time

then you would expect to see something like this in the table below:

**Table 3** Example Test Names and IDs

| Name | Test ID | Description |
|---|---|---|
| Fall Time | 110 | Measures clock fall time. |
| Rise Time | 100 | Measures clock rise time. |

and you would run these tests remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SelectedTests '100,110'"
arsl -a ipaddress -c "Run"

C# syntax
---------
remoteAte.SelectedTests = new int[]{100,110};
remoteAte.Run();
```

Here are the actual Test names and IDs used by this application. Listed at the end, you may also find:

- Deprecated IDs and their replacements.
- Macro IDs which may be used to select multiple related tests at the same time.

**NOTE** The file, "TestInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

**Table 4** Test IDs and Names

| Name | TestID | Description |
|---|---|---|
| Base Tx Test - Workshop Mode Test (16.0 GT/s) | 4049000 | |
| Base Tx Test - Workshop Mode Test (16.0 GT/s) | 5049000 | |
| Base Tx Test - Workshop Mode Test (16.0 GT/s) | 6049000 | |
| Base Tx Test - Workshop Mode Test (2.5 GT/s) | 4019000 | |
| Base Tx Test - Workshop Mode Test (2.5 GT/s) | 5019000 | |
| Base Tx Test - Workshop Mode Test (2.5 GT/s) | 6019000 | |
| Base Tx Test - Workshop Mode Test (32.0 GT/s) | 5059000 | |
| Base Tx Test - Workshop Mode Test (32.0 GT/s) | 6059000 | |
| Base Tx Test - Workshop Mode Test (5.0 GT/s) | 4029000 | |
| Base Tx Test - Workshop Mode Test (5.0 GT/s) | 5029000 | |
| Base Tx Test - Workshop Mode Test (5.0 GT/s) | 6029000 | |
| Base Tx Test - Workshop Mode Test (64.0 GT/s) | 6069000 | |
| Base Tx Test - Workshop Mode Test (8.0 GT/s) | 4039000 | |
| Base Tx Test - Workshop Mode Test (8.0 GT/s) | 5039000 | |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Base Tx Test - Workshop Mode Test (8.0 GT/s) | 6039000 | |
| EndPoint Tests - Workshop Mode Test (2.5 GT/s) | 5019200 | System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-8 of section 4.8.13 of the PCI Express Card Electromechanical (CEM) Specification, Rev 5.0, as measured after the connector with an ideal load. |
| EndPoint Tests - Workshop Mode Test (8.0 GT/s) | 5039200 | System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-13 of section 4.8.3 of the PCI Express Card Electromechanical (CEM) Specification, Rev 5.0, as measured after the connector with an ideal load. |
| EndPoint Tests - Workshop Mode Test - 3.5dB (5.0 GT/s) | 5029200 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-10 of section 4.8.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in figure 4-7. |
| EndPoint Tests - Workshop Mode Test - 6.0dB (5.0 GT/s) | 5029201 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-12 of section 4.8.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in figure 4-7. |
| EndPoint Tests - Workshop Mode Test - Max Channel (16.0 GT/s) | 5049201 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.4 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers. |
| EndPoint Tests - Workshop Mode Test - Max Channel - Signal Quality Test (32.0 GT/s) | 5059201 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |
| EndPoint Tests - Workshop Mode Test - Min Channel (16.0 GT/s) | 5049200 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.4 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers. |
| EndPoint Tests - Workshop Mode Test - Min Channel - Base Jitter Test (32.0 GT/s) | 5059200 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| EndPoint Tests, Eye-Width (16.0 GT/s) | 5042009 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |
| EndPoint Tests, Eye-Width (2.5 GT/s) | 5012009 | This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter]. |
| EndPoint Tests, Eye-Width (32.0 GT/s) | 5052009 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |
| EndPoint Tests, Eye-Width (8.0 GT/s) | 5032009 | This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] -[TJ at BER -12]. |
| EndPoint Tests, Eye-Width -3.5dB with crosstalk (5.0 GT/s) | 5022009 | This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [TJ at BER-12]. |
| EndPoint Tests, Eye-Width -3.5dB without crosstalk (5.0 GT/s) | 5022010 | This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [TJ at BER-12]. |
| EndPoint Tests, Eye-Width -6.0dB with crosstalk (5.0 GT/s) | 5022011 | This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter]. |
| EndPoint Tests, Eye-Width -6.0dB without crosstalk (5.0 GT/s) | 5022012 | This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter]. |
| EndPoint Tests, Maximum Deterministic Jitter -3.5dB with crosstalk (5.0 GT/s) | 5022017 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |
| EndPoint Tests, Maximum Deterministic Jitter -3.5dB without crosstalk (5.0 GT/s) | 5022018 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |
| EndPoint Tests, Maximum Deterministic Jitter -6.0dB with crosstalk (5.0 GT/s) | 5022019 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |
| EndPoint Tests, Maximum Deterministic Jitter -6.0dB without crosstalk (5.0 GT/s) | 5022020 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |
| EndPoint Tests, Median to Max Jitter (2.5 GT/s) | 5012004 | This test measures the maximum time between the jitter median and maximum deviation from the median. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| EndPoint Tests, Peak Differential Output Voltage (Non-Transition)(16.0 GT/s) | 5042006 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |
| EndPoint Tests, Peak Differential Output Voltage (Non-Transition)(2.5 GT/s) | 5012006 | This test verifies that the Peak Differential Output Voltage (Non-Transition) is within the allowed range. |
| EndPoint Tests, Peak Differential Output Voltage (Non-Transition)(32.0 GT/s) | 5052006 | This test verifies that the Peak Differential Output Voltage (Non-Transition) is within the allowed range. |
| EndPoint Tests, Peak Differential Output Voltage (Non-Transition)(8.0 GT/s) | 5032006 | This test verifies that the Peak Differential Output Voltage (Non-Transition) is within the allowed range. |
| EndPoint Tests, Peak Differential Output Voltage (Transition)(16.0 GT/s) | 5042005 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |
| EndPoint Tests, Peak Differential Output Voltage (Transition)(2.5 GT/s) | 5012005 | This test verifies that the Peak Differential Output Voltage (Transition) is within the allowed range. |
| EndPoint Tests, Peak Differential Output Voltage (Transition)(32.0 GT/s) | 5052005 | This test verifies that the Peak Differential Output Voltage (Transition) is within the allowed range. |
| EndPoint Tests, Peak Differential Output Voltage (Transition)(8.0 GT/s) | 5032005 | This test verifies that the Peak Differential Output Voltage (Transition) is within the allowed range. |
| EndPoint Tests, Peak Differential Output Voltage -3.5dB (Non-Transition)(5.0 GT/s) | 5022006 | This test verifies that the Peak Differential Output Voltage (Non-Transition) is within the allowed range. |
| EndPoint Tests, Peak Differential Output Voltage -3.5dB (Transition)(5.0 GT/s) | 5022005 | This test verifies that the Peak Differential Output Voltage (Transition) is within the allowed range. |
| EndPoint Tests, Peak Differential Output Voltage -6.0dB (Non-Transition)(5.0 GT/s) | 5022008 | This test verifies that the Peak Differential Output Voltage (Non-Transition) is within the allowed range. |
| EndPoint Tests, Peak Differential Output Voltage -6.0dB (Transition)(5.0 GT/s) | 5022007 | This test verifies that the Peak Differential Output Voltage (Transition) is within the allowed range. |
| EndPoint Tests, RMS Random Jitter -3.5dB with crosstalk (5.0 GT/s) | 5022013 | This test verifies RMS Random Jitter, it is informative only. |
| EndPoint Tests, RMS Random Jitter -3.5dB without crosstalk (5.0 GT/s) | 5022014 | This test verifies RMS Random Jitter, it is informative only. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| EndPoint Tests, RMS Random Jitter -6.0dB with crosstalk (5.0 GT/s) | 5022015 | This test verifies RMS Random Jitter, it is informative only. |
| EndPoint Tests, RMS Random Jitter -6.0dB without crosstalk (5.0 GT/s) | 5022016 | This test verifies RMS Random Jitter, it is informative only. |
| EndPoint Tests, Template Tests (16.0 GT/s) | 5042002 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |
| EndPoint Tests, Template Tests (2.5 GT/s) | 5012002 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications. |
| EndPoint Tests, Template Tests (32.0 GT/s) | 5052002 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |
| EndPoint Tests, Template Tests (8.0 GT/s) | 5032002 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |
| EndPoint Tests, Template Tests -3.5dB (5.0 GT/s) | 5022002 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications. |
| EndPoint Tests, Template Tests -6.0dB (5.0 GT/s) | 5022003 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications. |
| EndPoint Tests, Total Jitter at BER-12 -3.5dB with crosstalk (5.0 GT/s) | 5022021 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |
| EndPoint Tests, Total Jitter at BER-12 -3.5dB without crosstalk (5.0 GT/s) | 5022022 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| EndPoint Tests, Total Jitter at BER-12 -6.0dB with crosstalk (5.0 GT/s) | 5022023 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |
| EndPoint Tests, Total Jitter at BER-12 -6.0dB without crosstalk (5.0 GT/s) | 5022024 | Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |
| EndPoint Tests, Uncorrelated Deterministic Jitter (32.0 GT/s) | 5052013 | This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range. |
| EndPoint Tests, Uncorrelated Deterministic Pulse Width Jitter (16.0 GT/s) | 5042011 | This test verifies maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD, it is informative only. |
| EndPoint Tests, Uncorrelated Deterministic Pulse Width Jitter (32.0 GT/s) | 5052011 | This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range. This test required PWJ clock pattern. |
| EndPoint Tests, Uncorrelated Total Jitter (32.0 GT/s) | 5052012 | This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range. |
| EndPoint Tests, Uncorrelated Total Pulse Width Jitter (16.0 GT/s) | 5042010 | This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range. This test required PWJ clock pattern. |
| EndPoint Tests, Uncorrelated Total Pulse Width Jitter (32.0 GT/s) | 5052010 | This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range. This test required PWJ clock pattern. |
| EndPoint Tests, Unit Interval (16.0 GT/s) | 5042000 | A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The mean recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only. |
| EndPoint Tests, Unit Interval (32.0 GT/s) | 5052000 | A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The mean recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only. |
| EndPoint Tests, Unit interval (2.5 GT/s) | 5012000 | A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The mean recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only. |
| EndPoint Tests, Unit interval (8.0 GT/s) | 5032000 | A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The mean recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| EndPoint Tests, Unit interval -3.5dB (5.0 GT/s) | 5022000 | A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The mean recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only. |
| EndPoint Tests, Unit interval -6.0dB (5.0 GT/s) | 5022001 | A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The mean recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only. |
| Reference Clock, Absolute Crossing Point Voltage | 4014008 | This test verifies that the absolute crossing point voltage of the reference clock single-ended waveforms is within the allowed range. |
| Reference Clock, Absolute Crossing Point Voltage | 5014008 | This test verifies that the absolute crossing point voltage of the reference clock single-ended waveforms is within the allowed range. |
| Reference Clock, Absolute Crossing Point Voltage | 6014008 | This test verifies that the absolute crossing point voltage of the reference clock single-ended waveforms is within the allowed range. |
| Reference Clock, Absolute Max Input Voltage | 4014014 | This test verifies that the absolute maximum input voltage of the reference clock is within the allowed range. |
| Reference Clock, Absolute Max Input Voltage | 5014014 | This test verifies that the absolute maximum input voltage of the reference clock is within the allowed range. |
| Reference Clock, Absolute Max Input Voltage | 6014014 | This test verifies that the absolute maximum input voltage of the reference clock is within the allowed range. |
| Reference Clock, Absolute Min Input Voltage | 4014016 | This test verifies that the absolute minimum input voltage of the reference clock is within the allowed range. |
| Reference Clock, Absolute Min Input Voltage | 5014016 | This test verifies that the absolute minimum input voltage of the reference clock is within the allowed range. |
| Reference Clock, Absolute Min Input Voltage | 6014016 | This test verifies that the absolute minimum input voltage of the reference clock is within the allowed range. |
| Reference Clock, Average Clock Period | 4014004 | This test verifies that the average clock period accuracy of the differential waveform is within the allowed range. |
| Reference Clock, Average Clock Period | 5014004 | This test verifies that the average clock period accuracy of the differential waveform is within the allowed range. |
| Reference Clock, Average Clock Period | 6014004 | This test verifies that the average clock period accuracy of the differential waveform is within the allowed range. |
| Reference Clock, Average Clock Period (32.0GT/s) | 5054004 | This test verifies that the average clock period accuracy of the differential waveform is within the allowed range. This test is applicable for devices that support 32.0GT/s data speed. |
| Reference Clock, Average Clock Period (32.0GT/s) | 6054004 | This test verifies that the average clock period accuracy of the differential waveform is within the allowed range. This test is applicable for devices that support 32.0GT/s data speed. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Reference Clock, Average Clock Period (32.0GT/s, SRIS) | 5054005 | This test verifies that the average clock period accuracy of the differential waveform is within the allowed range. This test is applicable for devices that support 32.0GT/s speed with SRIS mode. |
| Reference Clock, Average Clock Period (32.0GT/s, SRIS) | 6054005 | This test verifies that the average clock period accuracy of the differential waveform is within the allowed range. This test is applicable for devices that support 32.0GT/s speed with SRIS mode. |
| Reference Clock, Average Clock Period (64.0GT/s) | 6064004 | This test verifies that the average clock period accuracy of the differential waveform is within the allowed range. This test is applicable for devices that support 64.0GT/s data speed. |
| Reference Clock, Average Clock Period (64.0GT/s, SRIS) | 6064005 | This test verifies that the average clock period accuracy of the differential waveform is within the allowed range. This test is applicable for devices that support 64.0GT/s speed with SRIS mode. |
| Reference Clock, Clock Frequency (Common Clk) | 5014024 | This test verifies that the measured reference clock frequency, FREFCLK, is within than the allowed frequency range. |
| Reference Clock, Clock Frequency (Common Clk) | 6014024 | This test verifies that the measured reference clock frequency, FREFCLK, is within than the allowed frequency range. |
| Reference Clock, Clock Frequency (Common Clk) (16.0 GT/s) | 4044024 | This test verifies that the measured reference clock frequency, FREFCLK, is within than the allowed frequency range. |
| Reference Clock, Clock Frequency (Common Clk) (8.0 GT/s) | 4034024 | This test verifies that the measured reference clock frequency, FREFCLK, is within than the allowed frequency range. |
| Reference Clock, Clock Frequency (Common Clk)(32.0 GT/s) | 5054024 | This test verifies that the measured reference clock frequency, FREFCLK, is within than the allowed frequency range. |
| Reference Clock, Clock Frequency (Common Clk)(32.0 GT/s) | 6054024 | This test verifies that the measured reference clock frequency, FREFCLK, is within than the allowed frequency range. |
| Reference Clock, Clock Frequency (Common Clk)(64.0 GT/s) | 6064024 | This test verifies that the measured reference clock frequency, FREFCLK, is within than the allowed frequency range. |
| Reference Clock, Differential Input High Voltage | 4014006 | This test verifies that the high voltage of the reference clock differential waveform is greater than the minimum allowed value. |
| Reference Clock, Differential Input High Voltage | 5014006 | This test verifies that the high voltage of the reference clock differential waveform is greater than the minimum allowed value. |
| Reference Clock, Differential Input High Voltage | 6014006 | This test verifies that the high voltage of the reference clock differential waveform is greater than the minimum allowed value. |
| Reference Clock, Differential Input Low Voltage | 4014007 | This test verifies that the low voltage of the reference clock differential waveform is greater than the maximum allowed value. |
| Reference Clock, Differential Input Low Voltage | 5014007 | This test verifies that the low voltage of the reference clock differential waveform is greater than the maximum allowed value. |
| Reference Clock, Differential Input Low Voltage | 6014007 | This test verifies that the low voltage of the reference clock differential waveform is greater than the maximum allowed value. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Reference Clock, Duty Cycle | 4014005 | This test verifies that the duty cycle of the reference clock differential waveform is within the allowed range. |
| Reference Clock, Duty Cycle | 5014005 | This test verifies that the duty cycle of the reference clock differential waveform is within the allowed range. |
| Reference Clock, Duty Cycle | 6014009 | This test verifies that the duty cycle of the reference clock differential waveform is within the allowed range. |
| Reference Clock, Falling Edge Rate | 4014003 | This test verifies that the falling edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing. |
| Reference Clock, Falling Edge Rate | 5014003 | This test verifies that the rising edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing. |
| Reference Clock, Falling Edge Rate | 6014003 | This test verifies that the rising edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing. |
| Reference Clock, Max SSC df/dt (Common Clk) | 5014021 | This test verifies that the reference clock maximum SSC df/dt is within the allowed range. |
| Reference Clock, Max SSC df/dt (Common Clk) | 6014021 | This test verifies that the reference clock maximum SSC df/dt is within the allowed range. |
| Reference Clock, PCI-SIG Reference Clock Jitter (16.0 GT/s) | 5044013 | This test will run PCI-SIG Reference Clock Jitter for PCIe 5.0 Generation. |
| Reference Clock, PCI-SIG Reference Clock Jitter (2.5 GT/s) | 5014013 | This test will run PCI-SIG Reference Clock Jitter for PCIe 5.0 Generation. |
| Reference Clock, PCI-SIG Reference Clock Jitter (32.0 GT/s) | 5054013 | This test will run PCI-SIG Reference Clock Jitter for PCIe 5.0 Generation. |
| Reference Clock, PCI-SIG Reference Clock Jitter (5.0 GT/s) | 5024013 | This test will run PCI-SIG Reference Clock Jitter for PCIe 5.0 Generation. |
| Reference Clock, PCI-SIG Reference Clock Jitter (8.0 GT/s) | 5034013 | This test will run PCI-SIG Reference Clock Jitter for PCIe 5.0 Generation. |
| Reference Clock, Peak to Peak Jitter (Common Clk) (2.5 GT/s) | 5014011 | This test verifies that the measured Peak to Peak jitter, TREFCLK-PP, is less than the maximum allowed value. |
| Reference Clock, Peak to Peak Jitter (Common Clk) (2.5 GT/s) | 6014011 | This test verifies that the measured Peak to Peak jitter, TREFCLK-PP, is less than the maximum allowed value. |
| Reference Clock, Peak to Peak Jitter (Common Clk) (PCIE4 2.5 GT/s) | 4014011 | This test verifies that the measured Peak to Peak jitter, TREFCLK-PP, is less than the maximum allowed value. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Reference Clock, RMS Jitter (Common Clk) (16.0 GT/s) | 4044011 | This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value. |
| Reference Clock, RMS Jitter (Common Clk) (16.0 GT/s) | 5044011 | This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value. |
| Reference Clock, RMS Jitter (Common Clk) (16.0 GT/s) | 6044011 | This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value. |
| Reference Clock, RMS Jitter (Common Clk) (32.0 GT/s) | 5054011 | This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value. |
| Reference Clock, RMS Jitter (Common Clk) (32.0 GT/s) | 6054011 | This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value. |
| Reference Clock, RMS Jitter (Common Clk) (5.0 GT/s) | 4024011 | This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value. |
| Reference Clock, RMS Jitter (Common Clk) (5.0 GT/s) | 5024011 | This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value. |
| Reference Clock, RMS Jitter (Common Clk) (5.0 GT/s) | 6024011 | This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value. |
| Reference Clock, RMS Jitter (Common Clk) (64.0 GT/s) | 6064011 | This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value. |
| Reference Clock, RMS Jitter (Common Clk) (8.0 GT/s) | 4034011 | This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value. |
| Reference Clock, RMS Jitter (Common Clk) (8.0 GT/s) | 5034011 | This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value. |
| Reference Clock, RMS Jitter (Common Clk) (8.0 GT/s) | 6034011 | This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value. |
| Reference Clock, Rise-Fall Matching | 4014018 | This test verifies that the rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching is within the allowed range. |
| Reference Clock, Rise-Fall Matching | 5014018 | This test verifies that the rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching is within the allowed range. |
| Reference Clock, Rise-Fall Matching | 6014018 | This test verifies that the rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching is within the allowed range. |
| Reference Clock, Rising Edge Rate | 4014002 | This test verifies that the rising edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing. |
| Reference Clock, Rising Edge Rate | 5014002 | This test verifies that the rising edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Reference Clock, Rising Edge Rate | 6014002 | This test verifies that the rising edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing. |
| Reference Clock, SSC deviation (Common Clk) | 5014020 | This test verifies that the reference clock SSC deviation is within the allowed range. |
| Reference Clock, SSC deviation (Common Clk) | 6014020 | This test verifies that the reference clock SSC deviation is within the allowed range. |
| Reference Clock, SSC deviation (Common Clk) (16.0 GT/s) | 4044020 | This test verifies that the reference clock SSC deviation is within the allowed range. |
| Reference Clock, SSC deviation (Common Clk) (5.0 GT/s) | 4024020 | This test verifies that the reference clock SSC deviation is within the allowed range. |
| Reference Clock, SSC deviation (Common Clk) (8.0 GT/s) | 4034020 | This test verifies that the reference clock SSC deviation is within the allowed range. |
| Reference Clock, SSC frequency range (Common Clk) | 5014019 | This test verifies that the reference clock SSC frequency is within the allowed range. |
| Reference Clock, SSC frequency range (Common Clk) | 6014019 | This test verifies that the reference clock SSC frequency is within the allowed range. |
| Reference Clock, SSC frequency range (Common Clk) (16.0 GT/s) | 4044019 | This test verifies that the reference clock SSC frequency is within the allowed range. |
| Reference Clock, SSC frequency range (Common Clk) (5.0 GT/s) | 4024019 | This test verifies that the reference clock SSC frequency is within the allowed range. |
| Reference Clock, SSC frequency range (Common Clk) (8.0 GT/s) | 4034019 | This test verifies that the reference clock SSC frequency is within the allowed range. |
| Reference Clock, Variation of VCross | 4014010 | This test verifies that the variation of VCross over all rising clock edges is within the allowed range. |
| Reference Clock, Variation of VCross | 5014010 | This test verifies that the variation of VCross over all rising clock edges is within the allowed range. |
| Reference Clock, Variation of VCross | 6014010 | This test verifies that the variation of VCross over all rising clock edges is within the allowed range. |
| RootComplex Tests - Workshop Mode Test (2.5 GT/s) | 5019100 | System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-8 of section 4.8.13 of the PCI Express Card Electromechanical (CEM) Specification, Rev 5.0, as measured after the connector with an ideal load. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| RootComplex Tests - Workshop Mode Test (5.0 GT/s) | 5029100 | System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-25 of section 4.8.14 of the PCI Express Card Electromechanical (CEM) Specification, Rev 5.0, as measured after the connector with an ideal load. |
| RootComplex Tests - Workshop Mode Test (8.0 GT/s) | 5039100 | System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-27 of section 4.8.15 of the PCI Express Card Electromechanical (CEM) Specification, Rev 5.0, as measured after the connector with an ideal load. |
| RootComplex Tests - Workshop Mode Test - Max Channel (16.0 GT/s) | 5049101 | System Board must meet the System Board Transmitter Path Compliance Eye Requirements specified section 4.8.15 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0. This test is run without InfiniiSim embedding and without an ISI channel added to the CBB. |
| RootComplex Tests - Workshop Mode Test - Max Channel - Signal Quality Test (32.0 GT/s) | 5059101 | System Board must meet the System Board Transmitter Path Compliance Eye Requirements specified section 4.8.15 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0. This test is run without InfiniiSim embedding and without an ISI channel added to the CBB. |
| RootComplex Tests - Workshop Mode Test - Min Channel (16.0 GT/s) | 5049100 | System Board must meet the System Board Transmitter Path Compliance Eye Requirements specified section 4.8.15 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0. This test is run without InfiniiSim embedding and without an ISI channel added to the CBB. |
| RootComplex Tests - Workshop Mode Test - Min Channel - Base Jitter Test (32.0 GT/s) | 5059100 | System Board must meet the System Board Transmitter Path Compliance Eye Requirements specified section 4.8.15 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0. This test is run without InfiniiSim embedding and without an ISI channel added to the CBB. |
| RootComplex Tests, Eye-Width (16.0 GT/s) | 5043009 | System Board must meet the System Board Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM). |
| RootComplex Tests, Eye-Width (2.5 GT/s) | 5013009 | This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter]. |
| RootComplex Tests, Eye-Width (32.0 GT/s) | 5053009 | System Board must meet the System Board Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM). |
| RootComplex Tests, Eye-Width (8.0 GT/s) | 5033009 | This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] -[TJ at BER -12]. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| RootComplex Tests, Eye-Width with crosstalk (5.0 GT/s) | 5023009 | This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter]. |
| RootComplex Tests, Eye-Width without crosstalk (5.0 GT/s) | 5023010 | This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter]. |
| RootComplex Tests, Maximum Deterministic Jitter with crosstalk (5.0 GT/s) | 5023017 | This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range. |
| RootComplex Tests, Maximum Deterministic Jitter without crosstalk (5.0 GT/s) | 5023018 | This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range. |
| RootComplex Tests, Median to Max Jitter (2.5 GT/s) | 5013004 | This test measures the maximum time between the jitter median and maximum deviation from the median. |
| RootComplex Tests, Peak Differential Output Voltage (Non-Transition)(16.0 GT/s) | 5043006 | This test verifies that the Peak Differential Output Voltage (Non-Transition) is within the allowed range. |
| RootComplex Tests, Peak Differential Output Voltage (Non-Transition)(2.5 GT/s) | 5013006 | This test verifies that the Peak Differential Output Voltage (Non-Transition) is within the allowed range. |
| RootComplex Tests, Peak Differential Output Voltage (Non-Transition)(32.0 GT/s) | 5053006 | This test verifies that the Peak Differential Output Voltage (Non-Transition) is within the allowed range. |
| RootComplex Tests, Peak Differential Output Voltage (Non-Transition)(5.0 GT/s) | 5023006 | This test verifies that the Peak Differential Output Voltage (Non-Transition) is within the allowed range. |
| RootComplex Tests, Peak Differential Output Voltage (Non-Transition)(8.0 GT/s) | 5033006 | This test verifies that the Peak Differential Output Voltage (Non-Transition) is within the allowed range. |
| RootComplex Tests, Peak Differential Output Voltage (Transition)(16.0 GT/s) | 5043005 | This test verifies that the Peak Differential Output Voltage (Transition) is within the allowed range. |
| RootComplex Tests, Peak Differential Output Voltage (Transition)(2.5 GT/s) | 5013005 | This test verifies that the Peak Differential Output Voltage (Transition) is within the allowed range. |
| RootComplex Tests, Peak Differential Output Voltage (Transition)(32.0 GT/s) | 5053005 | This test verifies that the Peak Differential Output Voltage (Transition) is within the allowed range. |
| RootComplex Tests, Peak Differential Output Voltage (Transition)(5.0 GT/s) | 5023005 | This test verifies that the Peak Differential Output Voltage (Transition) is within the allowed range. |
| RootComplex Tests, Peak Differential Output Voltage (Transition)(8.0 GT/s) | 5033005 | This test verifies that the Peak Differential Output Voltage (Transition) is within the allowed range. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| RootComplex Tests, RMS Random Jitter with crosstalk (5.0 GT/s) | 5023013 | This test verifies RMS Random Jitter, it is informative only. |
| RootComplex Tests, RMS Random Jitter without crosstalk (5.0 GT/s) | 5023014 | This test verifies RMS Random Jitter, it is informative only. |
| RootComplex Tests, Template Tests (16.0 GT/s) | 5043002 | System Board must meet the System Board Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM). |
| RootComplex Tests, Template Tests (2.5 GT/s) | 5013002 | System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in PCI Express Card Electromechanical (CEM) Specification, as measured after the connector with an ideal load. |
| RootComplex Tests, Template Tests (32.0 GT/s) | 5053002 | System Board must meet the System Board Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM). |
| RootComplex Tests, Template Tests (5.0 GT/s) | 5023002 | System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in PCI Express Card Electromechanical (CEM) Specification, as measured after the connector with an ideal load. |
| RootComplex Tests, Template Tests (8.0 GT/s) | 5033002 | System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical Specification (CEM), as measured at the card edge-fingers. |
| RootComplex Tests, Total Jitter at BER-12 with crosstalk (5.0 GT/s) | 5023021 | System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical (CEM) Specification, as measured after the connector with an ideal load. |
| RootComplex Tests, Total Jitter at BER-12 without crosstalk (5.0 GT/s) | 5023022 | System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in the PCI Express Card Electromechanical (CEM) Specification, as measured after the connector with an ideal load. |
| RootComplex Tests, Uncorrelated Deterministic Pulse Width Jitter (32.0 GT/s) | 5053011 | This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range. This test required PWJ clock pattern. |
| RootComplex Tests, Uncorrelated Total Pulse Width Jitter (32.0 GT/s) | 5053010 | This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range. This test required PWJ clock pattern. |
| RootComplex Tests, Uncorrelated deterministic jitter (32.0 GT/s) | 5053013 | This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range. |
| RootComplex Tests, Uncorrelated total jitter (32.0 GT/s) | 5053012 | This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| RootComplex Tests, Unit Interval (16.0 GT/s) | 5043000 | A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The mean recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only. |
| RootComplex Tests, Unit Interval (32.0 GT/s) | 5053000 | A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The mean recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only. |
| RootComplex Tests, Unit interval (2.5 GT/s) | 5013000 | A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The mean recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only. |
| RootComplex Tests, Unit interval (5.0 GT/s) | 5023000 | A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The mean recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only. |
| RootComplex Tests, Unit interval (8.0 GT/s) | 5033000 | A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The mean recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only. |
| Tx, AC common mode voltage - 1.25GHz (LPF) (2.5 GT/s) | 5011026 | The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load. |
| Tx, AC common mode voltage - 1.25GHz (LPF) (2.5 GT/s) | 6011026 | The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load. |
| Tx, AC common mode voltage - 16GHz (LPF) (32.0 GT/s) | 5051026 | The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load. |
| Tx, AC common mode voltage - 16GHz (LPF) (32.0 GT/s) | 6051026 | The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load. |
| Tx, AC common mode voltage - 16GHz (LPF) (64.0 GT/s) | 6061026 | The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load. |
| Tx, AC common mode voltage - 2.5GHz (LPF) (5.0 GT/s) | 4021026 | The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load. |
| Tx, AC common mode voltage - 2.5GHz (LPF) (5.0 GT/s) | 5021026 | The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, AC common mode voltage - 2.5GHz (LPF) (5.0 GT/s) | 6021026 | The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load. |
| Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (16.0 GT/s) | 4041027 | This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here. |
| Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (16.0 GT/s) | 5041027 | This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here. |
| Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (16.0 GT/s) | 6041027 | This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here. |
| Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (32.0 GT/s) | 5051027 | This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here. |
| Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (32.0 GT/s) | 6051027 | This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here. |
| Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (5.0 GT/s) | 4021027 | This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here. |
| Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (5.0 GT/s) | 5021027 | This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here. |
| Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (5.0 GT/s) | 6021027 | This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here. |
| Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (64.0 GT/s) | 6061027 | This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (8.0 GT/s) | 4031027 | This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here. |
| Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (8.0 GT/s) | 5031027 | This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here. |
| Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (8.0 GT/s) | 6031027 | This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here. |
| Tx, AC common mode voltage - 4GHz (LPF) (8.0 GT/s) | 5031026 | The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load. |
| Tx, AC common mode voltage - 4GHz (LPF) (8.0 GT/s) | 6031026 | The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load. |
| Tx, AC common mode voltage - 4GHz (LPF) (8.0 GT/s) | 4031026 | This test verify the AC common mode, VTX-CM-AC-PP (4GHz LPF) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here. |
| Tx, AC common mode voltage - 8GHz (LPF) (16.0 GT/s) | 4041026 | The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load. |
| Tx, AC common mode voltage - 8GHz (LPF) (16.0 GT/s) | 5041026 | The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load. |
| Tx, AC common mode voltage - 8GHz (LPF) (16.0 GT/s) | 6041026 | The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load. |
| Tx, Absolute delta of DC common mode voltage between D+ and D- (16.0 GT/s) | 4041028 | This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-. |
| Tx, Absolute delta of DC common mode voltage between D+ and D- (16.0 GT/s) | 5041028 | This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Absolute delta of DC common mode voltage between D+ and D- (16.0 GT/s) | 6041028 | This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-. |
| Tx, Absolute delta of DC common mode voltage between D+ and D- (2.5 GT/s) | 5011028 | This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-. |
| Tx, Absolute delta of DC common mode voltage between D+ and D- (2.5 GT/s) | 6011028 | This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-. |
| Tx, Absolute delta of DC common mode voltage between D+ and D- (32.0 GT/s) | 5051028 | This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-. |
| Tx, Absolute delta of DC common mode voltage between D+ and D- (32.0 GT/s) | 6051028 | This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-. |
| Tx, Absolute delta of DC common mode voltage between D+ and D- (5.0 GT/s) | 5021028 | This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-. |
| Tx, Absolute delta of DC common mode voltage between D+ and D- (5.0 GT/s) | 6021028 | This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-. |
| Tx, Absolute delta of DC common mode voltage between D+ and D- (64.0 GT/s) | 6061028 | This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Absolute delta of DC common mode voltage between D+ and D- (8.0 GT/s) | 4031028 | This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-. |
| Tx, Absolute delta of DC common mode voltage between D+ and D- (8.0 GT/s) | 5031028 | This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-. |
| Tx, Absolute delta of DC common mode voltage between D+ and D- (8.0 GT/s) | 6031028 | This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-. |
| Tx, Absolute delta of DC common mode voltage during L0 and Idle (16.0 GT/s) | 4041029 | This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle. |
| Tx, Absolute delta of DC common mode voltage during L0 and Idle (16.0 GT/s) | 5041029 | This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle. |
| Tx, Absolute delta of DC common mode voltage during L0 and Idle (16.0 GT/s) | 6041029 | This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle. |
| Tx, Absolute delta of DC common mode voltage during L0 and Idle (2.5 GT/s) | 5011029 | This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle. |
| Tx, Absolute delta of DC common mode voltage during L0 and Idle (2.5 GT/s) | 6011029 | This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Absolute delta of DC common mode voltage during L0 and Idle (32.0 GT/s) | 5051029 | This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle. |
| Tx, Absolute delta of DC common mode voltage during L0 and Idle (32.0 GT/s) | 6051029 | This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle. |
| Tx, Absolute delta of DC common mode voltage during L0 and Idle (5.0 GT/s) | 4021029 | This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle. |
| Tx, Absolute delta of DC common mode voltage during L0 and Idle (5.0 GT/s) | 5021029 | This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle. |
| Tx, Absolute delta of DC common mode voltage during L0 and Idle (5.0 GT/s) | 6021029 | This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle. |
| Tx, Absolute delta of DC common mode voltage during L0 and Idle (64.0 GT/s) | 6061029 | This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle. |
| Tx, Absolute delta of DC common mode voltage during L0 and Idle (8.0 GT/s) | 4031029 | This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle. |
| Tx, Absolute delta of DC common mode voltage during L0 and Idle (8.0 GT/s) | 5031029 | This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Absolute delta of DC common mode voltage during L0 and Idle (8.0 GT/s) | 6031029 | This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle. |
| Tx, Auto Tune Optimized CTLE (52UI Jitter Pattern) (64.0 GT/s) | 6061050 | This test finds the optimized CTLE in 52UI Jitter pattern. |
| Tx, Auto Tune Optimized CTLE (PWJ Pattern) (64.0 GT/s) | 6061051 | This test finds the optimized CTLE in PWJ pattern. |
| Tx, Avg DC Common Mode Output Voltage (2.5 GT/s) | 4011025 | This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification. |
| Tx, Avg DC common mode voltage (5.0 GT/s) | 4021025 | This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification. |
| Tx, DC Common Mode Line Delta (2.5 GT/s) | 4011028 | This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-. |
| Tx, DC Common Mode Line Delta (5.0 GT/s) | 4021028 | This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-. |
| Tx, DC common mode voltage (16.0 GT/s) | 4041025 | This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification. |
| Tx, DC common mode voltage (16.0 GT/s) | 5041025 | This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification. |
| Tx, DC common mode voltage (16.0 GT/s) | 6041025 | This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification. |
| Tx, DC common mode voltage (2.5 GT/s) | 5011025 | This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification. |
| Tx, DC common mode voltage (2.5 GT/s) | 6011025 | This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification. |
| Tx, DC common mode voltage (32.0 GT/s) | 5051025 | This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification. |
| Tx, DC common mode voltage (32.0 GT/s) | 6051025 | This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification. |
| Tx, DC common mode voltage (5.0 GT/s) | 5021025 | This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, DC common mode voltage (5.0 GT/s) | 6021025 | This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification. |
| Tx, DC common mode voltage (64.0 GT/s) | 6061025 | This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification. |
| Tx, DC common mode voltage (8.0 GT/s) | 4031025 | This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification. |
| Tx, DC common mode voltage (8.0 GT/s) | 5031025 | This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification. |
| Tx, DC common mode voltage (8.0 GT/s) | 6031025 | This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification. |
| Tx, Data dependent jitter (16.0 GT/s) | 4041016 | This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range. |
| Tx, Data dependent jitter (16.0 GT/s) | 5041016 | This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range. |
| Tx, Data dependent jitter (2.5 GT/s) | 4011016 | This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range. |
| Tx, Data dependent jitter (2.5 GT/s) | 5011016 | This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range. |
| Tx, Data dependent jitter (32.0 GT/s) | 5051016 | This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range. |
| Tx, Data dependent jitter (5.0 GT/s) | 4021016 | This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range. |
| Tx, Data dependent jitter (5.0 GT/s) | 5021016 | This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range. |
| Tx, Data dependent jitter (8.0 GT/s) | 4031016 | This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range. |
| Tx, Data dependent jitter (8.0 GT/s) | 5031016 | This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range. |
| Tx, De-emphasis Preset #0 (16.0 GT/s) | 4041100 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #0 (16.0 GT/s) | 5041100 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #0 (16.0 GT/s) | 6041100 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, De-emphasis Preset #0 (32.0 GT/s) | 5051100 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #0 (32.0 GT/s) | 6051100 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #0 (8.0 GT/s) | 4031100 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #0 (8.0 GT/s) | 5031100 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #0 (8.0 GT/s) | 6031100 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #1 (16.0 GT/s) | 4041101 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #1 (16.0 GT/s) | 5041101 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #1 (16.0 GT/s) | 6041101 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #1 (32.0 GT/s) | 5051101 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #1 (32.0 GT/s) | 6051101 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #1 (64.0 GT/s) | 6061202 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q1 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #1 (8.0 GT/s) | 4031101 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #1 (8.0 GT/s) | 5031101 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, De-emphasis Preset #1 (8.0 GT/s) | 6031101 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #10 (16.0 GT/s) | 4041111 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #10 (16.0 GT/s) | 5041111 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #10 (16.0 GT/s) | 6041111 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #10 (32.0 GT/s) | 5051111 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #10 (32.0 GT/s) | 6051111 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #10 (64.0 GT/s) | 6061229 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q10 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #10 (8.0 GT/s) | 4031111 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #10 (8.0 GT/s) | 5031111 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #10 (8.0 GT/s) | 6031111 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #2 (16.0 GT/s) | 4041102 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #2 (16.0 GT/s) | 5041102 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #2 (16.0 GT/s) | 6041102 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, De-emphasis Preset #2 (32.0 GT/s) | 5051102 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #2 (32.0 GT/s) | 6051102 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #2 (64.0 GT/s) | 6061205 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q2 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #2 (8.0 GT/s) | 4031102 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #2 (8.0 GT/s) | 5031102 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #2 (8.0 GT/s) | 6031102 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #3 (16.0 GT/s) | 4041103 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #3 (16.0 GT/s) | 5041103 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #3 (16.0 GT/s) | 6041103 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #3 (32.0 GT/s) | 5051103 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #3 (32.0 GT/s) | 6051103 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #3 (64.0 GT/s) | 6061208 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q3 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #3 (8.0 GT/s) | 4031103 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, De-emphasis Preset #3 (8.0 GT/s) | 5031103 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #3 (8.0 GT/s) | 6031103 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #4 (64.0 GT/s) | 6061211 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q4 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #5 (32.0 GT/s) | 5051116 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #5 (32.0 GT/s) | 6051116 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #5 (64.0 GT/s) | 6061214 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q5 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #6 (32.0 GT/s) | 5051117 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #6 (32.0 GT/s) | 6051117 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #6 (64.0 GT/s) | 6061217 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q6 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #7 (16.0 GT/s) | 4041107 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #7 (16.0 GT/s) | 5041107 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #7 (16.0 GT/s) | 6041107 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #7 (32.0 GT/s) | 5051107 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, De-emphasis Preset #7 (32.0 GT/s) | 6051107 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #7 (64.0 GT/s) | 6061220 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q7 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #7 (8.0 GT/s) | 4031107 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #7 (8.0 GT/s) | 5031107 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #7 (8.0 GT/s) | 6031107 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #8 (16.0 GT/s) | 4041109 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #8 (16.0 GT/s) | 5041109 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #8 (16.0 GT/s) | 6041109 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #8 (32.0 GT/s) | 5051109 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #8 (32.0 GT/s) | 6051109 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #8 (64.0 GT/s) | 6061223 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q8 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #8 (8.0 GT/s) | 4031109 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #8 (8.0 GT/s) | 5031109 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, De-emphasis Preset #8 (8.0 GT/s) | 6031109 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #9 (32.0 GT/s) | 5051118 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #9 (32.0 GT/s) | 6051118 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, De-emphasis Preset #9 (64.0 GT/s) | 6061226 | The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q9 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Deemphasized Voltage Ratio (2.5 GT/s) | 4011001 | The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, VTX-DE-RATIO = -20log10 (VTX-DIFF-PP/VTX-DE-EMPH-PP). This measurement is for de-emphasis level settings of -3.5dB. |
| Tx, Deemphasized Voltage Ratio (2.5 GT/s) | 5011001 | The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, VTX-DE-RATIO = -20log10 (VTX-DIFF-PP/VTX-DE-EMPH-PP). This measurement is for de-emphasis level settings of -3.5dB. |
| Tx, Deemphasized Voltage Ratio (2.5 GT/s) | 6011001 | The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, VTX-DE-RATIO = -20log10 (VTX-DIFF-PP/VTX-DE-EMPH-PP). This measurement is for de-emphasis level settings of -3.5dB. |
| Tx, Deemphasized Voltage Ratio -3.5dB (5.0 GT/s) | 4021001 | The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, VTX-DE-RATIO = -20log10 (VTX-DIFF-PP/VTX-DE-EMPH-PP). This measurement is for de-emphasis level settings of -3.5dB. |
| Tx, Deemphasized Voltage Ratio -3.5dB (5.0 GT/s) | 5021001 | The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, VTX-DE-RATIO = -20log10 (VTX-DIFF-PP/VTX-DE-EMPH-PP). This measurement is for de-emphasis level settings of -3.5dB. |
| Tx, Deemphasized Voltage Ratio -3.5dB (5.0 GT/s) | 6021001 | The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, VTX-DE-RATIO = -20log10 (VTX-DIFF-PP/VTX-DE-EMPH-PP). This measurement is for de-emphasis level settings of -3.5dB. |
| Tx, Deemphasized Voltage Ratio -6.0dB (5.0 GT/s) | 4021002 | The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, VTX-DE-RATIO = -20log10 (VTX-DIFF-PP/VTX-DE-EMPH-PP). This measurement is for de-emphasis level settings of -6dB. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Deemphasized Voltage Ratio -6.0dB (5.0 GT/s) | 5021002 | The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, VTX-DE-RATIO = -20log10 (VTX-DIFF-PP/VTX-DE-EMPH-PP). This measurement is for de-emphasis level settings of -6dB. |
| Tx, Deemphasized Voltage Ratio -6.0dB (5.0 GT/s) | 6021002 | The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, VTX-DE-RATIO = -20log10 (VTX-DIFF-PP/VTX-DE-EMPH-PP). This measurement is for de-emphasis level settings of -6dB. |
| Tx, Deterministic DjDD uncorrelated PWJ (16.0 GT/s) | 4041015 | This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range. This test required PWJ clock pattern. |
| Tx, Deterministic DjDD uncorrelated PWJ (16.0 GT/s) | 5041015 | This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range. This test required PWJ clock pattern. |
| Tx, Deterministic DjDD uncorrelated PWJ (16.0 GT/s) | 6041015 | This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range. This test required PWJ clock pattern. |
| Tx, Deterministic DjDD uncorrelated PWJ (2.5 GT/s) | 4011015 | This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range. |
| Tx, Deterministic DjDD uncorrelated PWJ (32.0 GT/s) | 5051015 | This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range. This test required PWJ clock pattern. |
| Tx, Deterministic DjDD uncorrelated PWJ (32.0 GT/s) | 6051015 | This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range. This test required PWJ clock pattern. |
| Tx, Deterministic DjDD uncorrelated PWJ (5.0 GT/s) | 4021015 | This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range. |
| Tx, Deterministic DjDD uncorrelated PWJ (5.0 GT/s) | 5021015 | This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range. |
| Tx, Deterministic DjDD uncorrelated PWJ (5.0 GT/s) | 6021015 | This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range. |
| Tx, Deterministic DjDD uncorrelated PWJ (64.0 GT/s) | 6061015 | This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range. This test required PWJ clock pattern. |
| Tx, Deterministic DjDD uncorrelated PWJ (8.0 GT/s) | 4031015 | This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range. |
| Tx, Deterministic DjDD uncorrelated PWJ (8.0 GT/s) | 5031015 | This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range. |
| Tx, Deterministic DjDD uncorrelated PWJ (8.0 GT/s) | 6031015 | This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Eye-Width (2.5 GT/s) | 4011006 | This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter]. |
| Tx, Eye-Width (5.0 GT/s) | 4021006 | This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter]. |
| Tx, Eye-Width (Low Power) (2.5 GT/s) | 4011009 | This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter]. |
| Tx, Full swing Tx voltage with no TxEQ (16.0 GT/s) | 4041010 | This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range. This test required Preset 04. |
| Tx, Full swing Tx voltage with no TxEQ (16.0 GT/s) | 5041010 | This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range. This test required Preset 04. |
| Tx, Full swing Tx voltage with no TxEQ (16.0 GT/s) | 6041010 | This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range. This test required Preset 04. |
| Tx, Full swing Tx voltage with no TxEQ (32.0 GT/s) | 5051010 | This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range. This test required Preset 04. |
| Tx, Full swing Tx voltage with no TxEQ (32.0 GT/s) | 6051010 | This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range. This test required Preset 04. |
| Tx, Full swing Tx voltage with no TxEQ (64.0 GT/s) | 6061010 | This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range. This test required Preset 00. |
| Tx, Full swing Tx voltage with no TxEQ (8.0 GT/s) | 4031010 | This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range. This test required Preset 04. |
| Tx, Full swing Tx voltage with no TxEQ (8.0 GT/s) | 5031010 | This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range. This test required Preset 04. |
| Tx, Full swing Tx voltage with no TxEQ (8.0 GT/s) | 6031010 | This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range. This test required Preset 04. |
| Tx, Level Separation Mismatch Ratio (64.0 GT/s) | 6061046 | This test verifies that the Level Separation Mismatch Ratio is within the allowed range. This test required Preset 00. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Maximum nominal Tx boost ratio for full swing (16.0 GT/s) | 6041040 | This test verifies that the maximum nominal Tx boost ratio for full swing, VTX-BOOST-FS is within the allowed range. This test required Preset 10. |
| Tx, Maximum nominal Tx boost ratio for full swing (16.0 GT/s) | 4041040 | This test verifies that the maximum nominal Tx boost ratio for full swing, VTX-BOOST-RS is within the allowed range. This test required Preset 10. |
| Tx, Maximum nominal Tx boost ratio for full swing (16.0 GT/s) | 5041040 | This test verifies that the maximum nominal Tx boost ratio for full swing, VTX-BOOST-RS is within the allowed range. This test required Preset 10. |
| Tx, Maximum nominal Tx boost ratio for full swing (32.0 GT/s) | 6051040 | This test verifies that the maximum nominal Tx boost ratio for full swing, VTX-BOOST-FS is within the allowed range. This test required Preset 10. |
| Tx, Maximum nominal Tx boost ratio for full swing (32.0 GT/s) | 5051040 | This test verifies that the maximum nominal Tx boost ratio for full swing, VTX-BOOST-RS is within the allowed range. This test required Preset 10. |
| Tx, Maximum nominal Tx boost ratio for full swing (64.0 GT/s) | 6061040 | This test verifies that the maximum nominal Tx boost ratio for full swing, VTX-BOOST-FS is within the allowed range. This test required Preset Q10. |
| Tx, Maximum nominal Tx boost ratio for full swing (8.0 GT/s) | 4031040 | This test verifies that the maximum nominal Tx boost ratio for full swing, VTX-BOOST-RS is within the allowed range. This test required Preset 10. |
| Tx, Maximum nominal Tx boost ratio for full swing (8.0 GT/s) | 5031040 | This test verifies that the maximum nominal Tx boost ratio for full swing, VTX-BOOST-RS is within the allowed range. This test required Preset 10. |
| Tx, Maximum nominal Tx boost ratio for full swing (8.0 GT/s) | 6031040 | This test verifies that the maximum nominal Tx boost ratio for full swing, VTX-BOOST-RS is within the allowed range. This test required Preset 10. |
| Tx, Maximum nominal Tx boost ratio for reduced swing (16.0 GT/s) | 4041039 | This test verifies that the maximum nominal Tx boost ratio for reduced swing, VTX-BOOST-RS is within the allowed range. This test required Preset 01. |
| Tx, Maximum nominal Tx boost ratio for reduced swing (16.0 GT/s) | 5041039 | This test verifies that the maximum nominal Tx boost ratio for reduced swing, VTX-BOOST-RS is within the allowed range. This test required Preset 01. |
| Tx, Maximum nominal Tx boost ratio for reduced swing (16.0 GT/s) | 6041039 | This test verifies that the maximum nominal Tx boost ratio for reduced swing, VTX-BOOST-RS is within the allowed range. This test required Preset 01. |
| Tx, Maximum nominal Tx boost ratio for reduced swing (32.0 GT/s) | 5051039 | This test verifies that the maximum nominal Tx boost ratio for reduced swing, VTX-BOOST-RS is within the allowed range. This test required Preset 01. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Maximum nominal Tx boost ratio for reduced swing (32.0 GT/s) | 6051039 | This test verifies that the maximum nominal Tx boost ratio for reduced swing, VTX-BOOST-RS is within the allowed range. This test required Preset 01. |
| Tx, Maximum nominal Tx boost ratio for reduced swing (64.0 GT/s) | 6061039 | This test verifies that the maximum nominal Tx boost ratio for reduced swing, VTX-BOOST-RS is within the allowed range. This test required Preset Q4. |
| Tx, Maximum nominal Tx boost ratio for reduced swing (8.0 GT/s) | 4031039 | This test verifies that the maximum nominal Tx boost ratio for reduced swing, VTX-BOOST-RS is within the allowed range. This test required Preset 01. |
| Tx, Maximum nominal Tx boost ratio for reduced swing (8.0 GT/s) | 5031039 | This test verifies that the maximum nominal Tx boost ratio for reduced swing, VTX-BOOST-RS is within the allowed range. This test required Preset 01. |
| Tx, Maximum nominal Tx boost ratio for reduced swing (8.0 GT/s) | 6031039 | This test verifies that the maximum nominal Tx boost ratio for reduced swing, VTX-BOOST-RS is within the allowed range. This test required Preset 01. |
| Tx, Median to Max Jitter (2.5 GT/s) | 4011005 | This test measures the maximum time between the jitter median and maximum deviation from the median. |
| Tx, Median to Max Jitter (Low Power) (2.5 GT/s) | 4011008 | This test measures the maximum time between the jitter median and maximum deviation from the median. |
| Tx, Min swing during EIEOS for full swing (16.0 GT/s) | 4041019 | This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range. |
| Tx, Min swing during EIEOS for full swing (16.0 GT/s) | 5041019 | This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range. |
| Tx, Min swing during EIEOS for full swing (16.0 GT/s) | 6041019 | This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range. |
| Tx, Min swing during EIEOS for full swing (32.0 GT/s) | 5051019 | This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range. |
| Tx, Min swing during EIEOS for full swing (32.0 GT/s) | 6051019 | This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range. |
| Tx, Min swing during EIEOS for full swing (64.0 GT/s) | 6061019 | This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range. This test required Preset 10. |
| Tx, Min swing during EIEOS for full swing (8.0 GT/s) | 4031019 | This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range. |
| Tx, Min swing during EIEOS for full swing (8.0 GT/s) | 5031019 | This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range. |
| Tx, Min swing during EIEOS for full swing (8.0 GT/s) | 6031019 | This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Min swing during EIEOS for reduced swing (16.0 GT/s, Low Power) | 4041020 | This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range. This test required Preset 01. |
| Tx, Min swing during EIEOS for reduced swing (16.0 GT/s, Low Power) | 5041020 | This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range. This test required Preset 01. |
| Tx, Min swing during EIEOS for reduced swing (16.0 GT/s, Low Power) | 6041020 | This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range. This test required Preset 01. |
| Tx, Min swing during EIEOS for reduced swing (32.0 GT/s, Low Power) | 5051020 | This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range. This test required Preset 01. |
| Tx, Min swing during EIEOS for reduced swing (32.0 GT/s, Low Power) | 6051020 | This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range. This test required Preset 01. |
| Tx, Min swing during EIEOS for reduced swing (64.0 GT/s, Low Power) | 6061020 | This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range. This test required Preset 04. |
| Tx, Min swing during EIEOS for reduced swing (8.0 GT/s, Low Power) | 4031020 | This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range. This test required Preset 01. |
| Tx, Min swing during EIEOS for reduced swing (8.0 GT/s, Low Power) | 5031020 | This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range. This test required Preset 01. |
| Tx, Min swing during EIEOS for reduced swing (8.0 GT/s, Low Power) | 6031020 | This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range. This test required Preset 01. |
| Tx, Peak Differential Output Voltage (Non-Transition)(2.5 GT/s) | 4011035 | This test verifies that the Peak Differential Output Voltage (Non-Transition) is within the allowed range. |
| Tx, Peak Differential Output Voltage (Non-Transition)(2.5 GT/s) | 5011035 | This test verifies that the Peak Differential Output Voltage (Non-Transition) is within the allowed range. |
| Tx, Peak Differential Output Voltage (Non-Transition)(2.5 GT/s) | 6011035 | This test verifies that the Peak Differential Output Voltage (Non-Transition) is within the allowed range. |
| Tx, Peak Differential Output Voltage (Non-Transition)(2.5 GT/s, Low Power) | 4011036 | This test verifies that the Peak Differential Output Voltage (Non-Transition) (Low Power) is within the allowed range. |
| Tx, Peak Differential Output Voltage (Non-Transition)(2.5 GT/s, Low Power) | 5011036 | This test verifies that the Peak Differential Output Voltage (Non-Transition) (Low Power) is within the allowed range. |
| Tx, Peak Differential Output Voltage (Non-Transition)(2.5 GT/s, Low Power) | 6011036 | This test verifies that the Peak Differential Output Voltage (Non-Transition) (Low Power) is within the allowed range. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Peak Differential Output Voltage (Non-Transition)(5.0 GT/s, Low Power) | 4021036 | This test verifies that the Peak Differential Output Voltage (Non-Transition) (Low Power) is within the allowed range. |
| Tx, Peak Differential Output Voltage (Non-Transition)(5.0 GT/s, Low Power) | 5021036 | This test verifies that the Peak Differential Output Voltage (Non-Transition) (Low Power) is within the allowed range. |
| Tx, Peak Differential Output Voltage (Non-Transition)(5.0 GT/s, Low Power) | 6021036 | This test verifies that the Peak Differential Output Voltage (Non-Transition) (Low Power) is within the allowed range. |
| Tx, Peak Differential Output Voltage (Transition) (5.0 GT/s, Low Power) | 4021011 | This test verifies that the Peak Differential Output Voltage (Transition) (Low Power) is within the allowed range. |
| Tx, Peak Differential Output Voltage (Transition) (5.0 GT/s, Low Power) | 5021011 | This test verifies that the Peak Differential Output Voltage (Transition) (Low Power) is within the allowed range. |
| Tx, Peak Differential Output Voltage (Transition) (5.0 GT/s, Low Power) | 6021011 | This test verifies that the Peak Differential Output Voltage (Transition) (Low Power) is within the allowed range. |
| Tx, Peak Differential Output Voltage (Transition)(2.5 GT/s) | 4011010 | This test verifies that the Peak Differential Output Voltage (Transition) is within the allowed range. |
| Tx, Peak Differential Output Voltage (Transition)(2.5 GT/s) | 5011010 | This test verifies that the Peak Differential Output Voltage (Transition) is within the allowed range. |
| Tx, Peak Differential Output Voltage (Transition)(2.5 GT/s) | 6011010 | This test verifies that the Peak Differential Output Voltage (Transition) is within the allowed range. |
| Tx, Peak Differential Output Voltage (Transition)(2.5 GT/s, Low Power) | 4011011 | This test verifies that the Peak Differential Output Voltage (Transition) (Low Power) is within the allowed range. |
| Tx, Peak Differential Output Voltage (Transition)(2.5 GT/s, Low Power) | 5011011 | This test verifies that the Peak Differential Output Voltage (Transition) (Low Power) is within the allowed range. |
| Tx, Peak Differential Output Voltage (Transition)(2.5 GT/s, Low Power) | 6011011 | This test verifies that the Peak Differential Output Voltage (Transition) (Low Power) is within the allowed range. |
| Tx, Peak Differential Output Voltage -3.5dB (Non-Transition)(5.0 GT/s) | 4021035 | This test verifies that the Peak Differential Output Voltage -3.5dB (Non-Transition) is within the allowed range. |
| Tx, Peak Differential Output Voltage -3.5dB (Non-Transition)(5.0 GT/s) | 5021035 | This test verifies that the Peak Differential Output Voltage -3.5dB (Non-Transition) is within the allowed range. |
| Tx, Peak Differential Output Voltage -3.5dB (Non-Transition)(5.0 GT/s) | 6021035 | This test verifies that the Peak Differential Output Voltage -3.5dB (Non-Transition) is within the allowed range. |
| Tx, Peak Differential Output Voltage -3.5dB (Transition) (5.0 GT/s) | 4021010 | This test verifies that the Peak Differential Output Voltage -3.5dB (Transition) is within the allowed range. |
| Tx, Peak Differential Output Voltage -3.5dB (Transition)(5.0 GT/s) | 5021010 | This test verifies that the Peak Differential Output Voltage -3.5dB (Transition) is within the allowed range. |
| Tx, Peak Differential Output Voltage -3.5dB (Transition)(5.0 GT/s) | 6021010 | This test verifies that the Peak Differential Output Voltage -3.5dB (Transition) is within the allowed range. |
| Tx, Peak Differential Output Voltage -6.0dB (Non-Transition)(5.0 GT/s) | 4021038 | This test verifies that the Peak Differential Output Voltage -6.0dB (Non-Transition) is within the allowed range. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Peak Differential Output Voltage -6.0dB (Non-Transition)(5.0 GT/s) | 5021038 | This test verifies that the Peak Differential Output Voltage -6.0dB (Non-Transition) is within the allowed range. |
| Tx, Peak Differential Output Voltage -6.0dB (Non-Transition)(5.0 GT/s) | 6021038 | This test verifies that the Peak Differential Output Voltage -6.0dB (Non-Transition) is within the allowed range. |
| Tx, Peak Differential Output Voltage -6.0dB (Transition) (5.0 GT/s) | 4021037 | This test verifies that the Peak Differential Output Voltage -6.0dB (Transition) is within the allowed range. |
| Tx, Peak Differential Output Voltage -6.0dB (Transition)(5.0 GT/s) | 5021037 | This test verifies that the Peak Differential Output Voltage -6.0dB (Transition) is within the allowed range. |
| Tx, Peak Differential Output Voltage -6.0dB (Transition)(5.0 GT/s) | 6021037 | This test verifies that the Peak Differential Output Voltage -6.0dB (Transition) is within the allowed range. |
| Tx, Preshoot 1 Preset #1 (64.0 GT/s) | 6061201 | The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q1 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 1 Preset #10 (64.0 GT/s) | 6061228 | The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q10 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 1 Preset #2 (64.0 GT/s) | 6061204 | The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q2 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 1 Preset #3 (64.0 GT/s) | 6061207 | The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q3 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 1 Preset #4 (64.0 GT/s) | 6061210 | The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q4 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 1 Preset #5 (64.0 GT/s) | 6061213 | The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q5 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 1 Preset #6 (64.0 GT/s) | 6061216 | The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q6 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 1 Preset #7 (64.0 GT/s) | 6061219 | The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q7 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 1 Preset #8 (64.0 GT/s) | 6061222 | The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q8 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 1 Preset #9 (64.0 GT/s) | 6061225 | The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q9 is within the conformance limits specified in the PCI Express Base Specification. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Preshoot 2 Preset #1 (64.0 GT/s) | 6061200 | The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q1 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 2 Preset #10 (64.0 GT/s) | 6061227 | The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q10 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 2 Preset #2 (64.0 GT/s) | 6061203 | The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q2 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 2 Preset #3 (64.0 GT/s) | 6061206 | The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q3 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 2 Preset #4 (64.0 GT/s) | 6061209 | The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q4 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 2 Preset #5 (64.0 GT/s) | 6061212 | The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q5 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 2 Preset #6 (64.0 GT/s) | 6061215 | The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q6 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 2 Preset #7 (64.0 GT/s) | 6061218 | The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q7 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 2 Preset #8 (64.0 GT/s) | 6061221 | The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q8 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot 2 Preset #9 (64.0 GT/s) | 6061224 | The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q9 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #0 (32.0 GT/s) | 5051112 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #0 (32.0 GT/s) | 6051112 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #1 (32.0 GT/s) | 5051113 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Preshoot Preset #1 (32.0 GT/s) | 6051113 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #10 (32.0 GT/s) | 5051119 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #10 (32.0 GT/s) | 6051119 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #2 (32.0 GT/s) | 5051114 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #2 (32.0 GT/s) | 6051114 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #3 (32.0 GT/s) | 5051115 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #3 (32.0 GT/s) | 6051115 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #5 (16.0 GT/s) | 4041104 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #5 (16.0 GT/s) | 5041104 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #5 (16.0 GT/s) | 6041104 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #5 (32.0 GT/s) | 5051104 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #5 (32.0 GT/s) | 6051104 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #5 (8.0 GT/s) | 4031104 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Preshoot Preset #5 (8.0 GT/s) | 5031104 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #5 (8.0 GT/s) | 6031104 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #6 (16.0 GT/s) | 4041105 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #6 (16.0 GT/s) | 5041105 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #6 (16.0 GT/s) | 6041105 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #6 (32.0 GT/s) | 5051105 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #6 (32.0 GT/s) | 6051105 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #6 (8.0 GT/s) | 4031105 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #6 (8.0 GT/s) | 5031105 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #6 (8.0 GT/s) | 6031105 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #7 (16.0 GT/s) | 4041106 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #7 (16.0 GT/s) | 5041106 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #7 (16.0 GT/s) | 6041106 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Preshoot Preset #7 (32.0 GT/s) | 5051106 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #7 (32.0 GT/s) | 6051106 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #7 (8.0 GT/s) | 4031106 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #7 (8.0 GT/s) | 5031106 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #7 (8.0 GT/s) | 6031106 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #8 (16.0 GT/s) | 4041108 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #8 (16.0 GT/s) | 5041108 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #8 (16.0 GT/s) | 6041108 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #8 (32.0 GT/s) | 5051108 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #8 (32.0 GT/s) | 6051108 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #8 (8.0 GT/s) | 4031108 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #8 (8.0 GT/s) | 5031108 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #8 (8.0 GT/s) | 6031108 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Preshoot Preset #9 (16.0 GT/s) | 4041110 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #9 (16.0 GT/s) | 5041110 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #9 (16.0 GT/s) | 6041110 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #9 (32.0 GT/s) | 5051110 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #9 (32.0 GT/s) | 6051110 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #9 (8.0 GT/s) | 4031110 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #9 (8.0 GT/s) | 5031110 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Preshoot Preset #9 (8.0 GT/s) | 6031110 | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification. |
| Tx, Pseudo package loss, Non-Root Device (32.0 GT/s) | 5051018 | This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 04. |
| Tx, Pseudo package loss, Non-Root Device (32.0 GT/s) | 6051018 | This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 04. |
| Tx, Pseudo package loss, Non-Root Device (64.0 GT/s) | 6061018 | This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 00. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Pseudo package loss, Non-Root Device (8.0 GT/s) | 4031018 | This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 04. |
| Tx, Pseudo package loss, Non-Root Device (8.0 GT/s) | 5031018 | This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 04. |
| Tx, Pseudo package loss, Non-Root Device (8.0 GT/s) | 6031018 | This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 04. |
| Tx, Pseudo package loss, Non-Root Device, Captive Channel (16.0 GT/s) | 4041018 | This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 04. |
| Tx, Pseudo package loss, Non-Root Device, Captive Channel (16.0 GT/s) | 5041018 | This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 04. |
| Tx, Pseudo package loss, Non-Root Device, Captive Channel (16.0 GT/s) | 6041018 | This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 04. |
| Tx, Pseudo package loss, Non-Root Device, No Captive Channel (16.0 GT/s) | 4041031 | This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 04. |
| Tx, Pseudo package loss, Non-Root Device, No Captive Channel (16.0 GT/s) | 5041031 | This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 04. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Pseudo package loss, Non-Root Device, No Captive Channel (16.0 GT/s) | 6041031 | This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 04. |
| Tx, Pseudo package loss, Root Device (16.0 GT/s) | 5041030 | This test verifies that the maximum pseudo package loss for all devices with root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 04. |
| Tx, Pseudo package loss, Root Device (16.0 GT/s) | 6041030 | This test verifies that the maximum pseudo package loss for all devices with root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 04. |
| Tx, Pseudo package loss, Root Device (16.0 GT/s) | 4041030 | This test verifies that the maximum pseudo package loss for all devices with root ports, ps21TX is within the allowed range. This test required Preset 04. |
| Tx, Pseudo package loss, Root Device (32.0 GT/s) | 5051030 | This test verifies that the maximum pseudo package loss for all devices with root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 04. |
| Tx, Pseudo package loss, Root Device (32.0 GT/s) | 6051030 | This test verifies that the maximum pseudo package loss for all devices with root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 04. |
| Tx, Pseudo package loss, Root Device (64.0 GT/s) | 6061030 | This test verifies that the maximum pseudo package loss for all devices with root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 00. |
| Tx, Pseudo package loss, Root Device (8.0 GT/s) | 5031030 | This test verifies that the maximum pseudo package loss for all devices with root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 04. |
| Tx, Pseudo package loss, Root Device (8.0 GT/s) | 6031030 | This test verifies that the maximum pseudo package loss for all devices with root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11. This test required Preset 04. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Pseudo package loss, Root Device (8.0 GT/s) | 4031030 | This test verifies that the maximum pseudo package loss of all devices with root ports, ps21TX is within the allowed range. This test required Preset 04. |
| Tx, RMS AC Peak Common Mode Output Voltage (2.5 GT/s) | 4011033 | The maximum allowable RMS AC (>30Khz) common mode voltage is 20mV (Vtx-cm-acp) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load. |
| Tx, Random jitter (16.0 GT/s) | 4041017 | This test verifies random jitter, it is informative only. |
| Tx, Random jitter (16.0 GT/s) | 5041017 | This test verifies random jitter, it is informative only. |
| Tx, Random jitter (16.0 GT/s) | 6041017 | This test verifies random jitter, it is informative only. |
| Tx, Random jitter (2.5 GT/s) | 4011017 | This test verifies random jitter, it is informative only. |
| Tx, Random jitter (32.0 GT/s) | 5051017 | This test verifies random jitter, it is informative only. |
| Tx, Random jitter (32.0 GT/s) | 6051017 | This test verifies random jitter, it is informative only. |
| Tx, Random jitter (5.0 GT/s) | 4021017 | This test verifies random jitter, it is informative only. |
| Tx, Random jitter (5.0 GT/s) | 5021017 | This test verifies random jitter, it is informative only. |
| Tx, Random jitter (5.0 GT/s) | 6021017 | This test verifies random jitter, it is informative only. |
| Tx, Random jitter (64.0 GT/s) | 6061017 | This test verifies random jitter, it is informative only. |
| Tx, Random jitter (8.0 GT/s) | 4031017 | This test verifies random jitter, it is informative only. |
| Tx, Random jitter (8.0 GT/s) | 5031017 | This test verifies random jitter, it is informative only. |
| Tx, Random jitter (8.0 GT/s) | 6031017 | This test verifies random jitter, it is informative only. |
| Tx, Reduced swing Tx voltage with no TxEQ (16.0 GT/s, Low Power) | 4041011 | This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range. This test required Preset 04. |
| Tx, Reduced swing Tx voltage with no TxEQ (16.0 GT/s, Low Power) | 5041011 | This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range. This test required Preset 04. |
| Tx, Reduced swing Tx voltage with no TxEQ (16.0 GT/s, Low Power) | 6041011 | This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range. This test required Preset 04. |
| Tx, Reduced swing Tx voltage with no TxEQ (32.0 GT/s, Low Power) | 5051011 | This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range. This test required Preset 04. |
| Tx, Reduced swing Tx voltage with no TxEQ (32.0 GT/s, Low Power) | 6051011 | This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range. This test required Preset 04. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Reduced swing Tx voltage with no TxEQ (64.0 GT/s, Low Power) | 6061011 | This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range. This test required Preset 00. |
| Tx, Reduced swing Tx voltage with no TxEQ (8.0 GT/s, Low Power) | 4031011 | This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range. This test required Preset 04. |
| Tx, Reduced swing Tx voltage with no TxEQ (8.0 GT/s, Low Power) | 5031011 | This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range. This test required Preset 04. |
| Tx, Reduced swing Tx voltage with no TxEQ (8.0 GT/s, Low Power) | 6031011 | This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range. This test required Preset 04. |
| Tx, SSC Df/Dt (Max)(PCIE 4.0 16.0GT/s) | 4041024 | This test verifies that the SSC maximum slew rate is within the allowed range. |
| Tx, SSC Df/Dt (Max)(PCIE 4.0 8.0GT/s) | 4031024 | This test verifies that the SSC maximum slew rate is within the allowed range. |
| Tx, SSC Df/Dt (Max)(PCIE 5.0 16.0GT/s) | 5041024 | This test verifies that the SSC maximum slew rate is within the allowed range. |
| Tx, SSC Df/Dt (Max)(PCIE 5.0 2.5GT/s) | 5011024 | This test verifies that the SSC maximum slew rate is within the allowed range. |
| Tx, SSC Df/Dt (Max)(PCIE 5.0 32.0GT/s) | 5051024 | This test verifies that the SSC maximum slew rate is within the allowed range. |
| Tx, SSC Df/Dt (Max)(PCIE 5.0 5.0GT/s) | 5021024 | This test verifies that the SSC maximum slew rate is within the allowed range. |
| Tx, SSC Df/Dt (Max)(PCIE 5.0 8.0GT/s) | 5031024 | This test verifies that the SSC maximum slew rate is within the allowed range. |
| Tx, SSC Df/Dt (Max)(PCIE 6.0 16.0GT/s) | 6041024 | This test verifies that the SSC maximum slew rate is within the allowed range. |
| Tx, SSC Df/Dt (Max)(PCIE 6.0 2.5GT/s) | 6011024 | This test verifies that the SSC maximum slew rate is within the allowed range. |
| Tx, SSC Df/Dt (Max)(PCIE 6.0 32.0GT/s) | 6051024 | This test verifies that the SSC maximum slew rate is within the allowed range. |
| Tx, SSC Df/Dt (Max)(PCIE 6.0 5.0GT/s) | 6021024 | This test verifies that the SSC maximum slew rate is within the allowed range. |
| Tx, SSC Df/Dt (Max)(PCIE 6.0 64.0GT/s) | 6061024 | This test verifies that the SSC maximum slew rate is within the allowed range. |
| Tx, SSC Df/Dt (Max)(PCIE 6.0 8.0GT/s) | 6031024 | This test verifies that the SSC maximum slew rate is within the allowed range. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, SSC Modulation Frequency (PCIE 4.0 16.0GT/s) | 4041021 | This test verifies that the SSC frequency range is in the allowable range. This test required Preset 04. |
| Tx, SSC Modulation Frequency (PCIE 4.0 8.0GT/s) | 4031021 | This test verifies that the SSC frequency range is in the allowable range. This test required Preset 04. |
| Tx, SSC Modulation Frequency (PCIE 5.0 16.0GT/s) | 5041021 | This test verifies that the SSC frequency range is in the allowable range. This test required Preset 04. |
| Tx, SSC Modulation Frequency (PCIE 5.0 2.5GT/s) | 5011021 | This test verifies that the SSC frequency range is in the allowable range. |
| Tx, SSC Modulation Frequency (PCIE 5.0 32.0GT/s) | 5051021 | This test verifies that the SSC frequency range is in the allowable range. This test required Preset 04. |
| Tx, SSC Modulation Frequency (PCIE 5.0 5.0GT/s) | 5021021 | This test verifies that the SSC frequency range is in the allowable range. |
| Tx, SSC Modulation Frequency (PCIE 5.0 8.0GT/s) | 5031021 | This test verifies that the SSC frequency range is in the allowable range. This test required Preset 04. |
| Tx, SSC Modulation Frequency (PCIE 6.0 16.0GT/s) | 6041021 | This test verifies that the SSC frequency range is in the allowable range. This test required Preset 04. |
| Tx, SSC Modulation Frequency (PCIE 6.0 2.5GT/s) | 6011021 | This test verifies that the SSC frequency range is in the allowable range. |
| Tx, SSC Modulation Frequency (PCIE 6.0 32.0GT/s) | 6051021 | This test verifies that the SSC frequency range is in the allowable range. This test required Preset 04. |
| Tx, SSC Modulation Frequency (PCIE 6.0 5.0GT/s) | 6021021 | This test verifies that the SSC frequency range is in the allowable range. |
| Tx, SSC Modulation Frequency (PCIE 6.0 64.0GT/s) | 6061021 | This test verifies that the SSC frequency range is in the allowable range. |
| Tx, SSC Modulation Frequency (PCIE 6.0 8.0GT/s) | 6031021 | This test verifies that the SSC frequency range is in the allowable range. This test required Preset 04. |
| Tx, SSC Peak Deviation (Max) (PCIE 4.0 16.0GT/s) | 4041022 | This test verifies that the SSC maximum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Max) (PCIE 4.0 8.0GT/s) | 4031022 | This test verifies that the SSC maximum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Max) (PCIE 5.0 16.0GT/s) | 5041022 | This test verifies that the SSC maximum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Max) (PCIE 5.0 2.5GT/s) | 5011022 | This test verifies that the SSC maximum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Max) (PCIE 5.0 32.0GT/s) | 5051022 | This test verifies that the SSC maximum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Max) (PCIE 5.0 5.0GT/s) | 5021022 | This test verifies that the SSC maximum deviation within the allowed range. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, SSC Peak Deviation (Max) (PCIE 5.0 8.0GT/s) | 5031022 | This test verifies that the SSC maximum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Max) (PCIE 6.0 16.0GT/s) | 6041022 | This test verifies that the SSC maximum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Max) (PCIE 6.0 2.5GT/s) | 6011022 | This test verifies that the SSC maximum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Max) (PCIE 6.0 32.0GT/s) | 6051022 | This test verifies that the SSC maximum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Max) (PCIE 6.0 5.0GT/s) | 6021022 | This test verifies that the SSC maximum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Max) (PCIE 6.0 64.0GT/s) | 6061022 | This test verifies that the SSC maximum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Max) (PCIE 6.0 8.0GT/s) | 6031022 | This test verifies that the SSC maximum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Min) (PCIE 4.0 16.0GT/s) | 4041023 | This test verifies that the SSC minimum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Min) (PCIE 4.0 8.0GT/s) | 4031023 | This test verifies that the SSC minimum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Min) (PCIE 5.0 16.0GT/s) | 5041023 | This test verifies that the SSC minimum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Min) (PCIE 5.0 2.5GT/s) | 5011023 | This test verifies that the SSC minimum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Min) (PCIE 5.0 32.0GT/s) | 5051023 | This test verifies that the SSC minimum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Min) (PCIE 5.0 5.0GT/s) | 5021023 | This test verifies that the SSC minimum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Min) (PCIE 5.0 8.0GT/s) | 5031023 | This test verifies that the SSC minimum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Min) (PCIE 6.0 16.0GT/s) | 6041023 | This test verifies that the SSC minimum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Min) (PCIE 6.0 2.5GT/s) | 6011023 | This test verifies that the SSC minimum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Min) (PCIE 6.0 32.0GT/s) | 6051023 | This test verifies that the SSC minimum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Min) (PCIE 6.0 5.0GT/s) | 6021023 | This test verifies that the SSC minimum deviation within the allowed range. |
| Tx, SSC Peak Deviation (Min) (PCIE 6.0 64.0GT/s) | 6061023 | This test verifies that the SSC minimum deviation within the allowed range. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, SSC Peak Deviation (Min) (PCIE 6.0 8.0GT/s) | 6031023 | This test verifies that the SSC minimum deviation within the allowed range. |
| Tx, Signal-to-Noise-Distortion Ratio (64.0 GT/s) | 6061045 | This test verifies that the Signal-to-Noise-Distortion Ratio is within the allowed range. This test required Preset 00. |
| Tx, Template Tests (2.5 GT/s) | 4011004 | This test verifies transmitter eye diagram, it is informative only. |
| Tx, Template Tests (Low Power) (2.5 GT/s) | 4011007 | This test verifies transmitter eye diagram, it is informative only. |
| Tx, Template Tests (Low Power) (5.0 GT/s) | 4021007 | This test verifies transmitter eye diagram, it is informative only. |
| Tx, Template Tests -3.5dB (5.0 GT/s) | 4021004 | This test verifies transmitter eye diagram, it is informative only. |
| Tx, Template Tests -6.0dB (5.0 GT/s) | 4021032 | This test verifies transmitter eye diagram, it is informative only. |
| Tx, Total uncorrelated PWJ (16.0 GT/s) | 4041014 | This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range. This test required PWJ clock pattern. |
| Tx, Total uncorrelated PWJ (16.0 GT/s) | 5041014 | This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range. This test required PWJ clock pattern. |
| Tx, Total uncorrelated PWJ (16.0 GT/s) | 6041014 | This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range. This test required PWJ clock pattern. |
| Tx, Total uncorrelated PWJ (2.5 GT/s) | 4011014 | This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range. |
| Tx, Total uncorrelated PWJ (32.0 GT/s) | 5051014 | This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range. This test required PWJ clock pattern. |
| Tx, Total uncorrelated PWJ (32.0 GT/s) | 6051014 | This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range. This test required PWJ clock pattern. |
| Tx, Total uncorrelated PWJ (5.0 GT/s) | 4021014 | This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range. |
| Tx, Total uncorrelated PWJ (5.0 GT/s) | 5021014 | This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range. |
| Tx, Total uncorrelated PWJ (5.0 GT/s) | 6021014 | This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range. |
| Tx, Total uncorrelated PWJ (64.0 GT/s) | 6061014 | This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range. This test required PWJ clock pattern. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Total uncorrelated PWJ (8.0 GT/s) | 4031014 | This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range. |
| Tx, Total uncorrelated PWJ (8.0 GT/s) | 5031014 | This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range. |
| Tx, Total uncorrelated PWJ (8.0 GT/s) | 6031014 | This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range. |
| Tx, Uncorrelated deterministic jitter (16.0 GT/s) | 4041013 | This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range. |
| Tx, Uncorrelated deterministic jitter (16.0 GT/s) | 5041013 | This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range. |
| Tx, Uncorrelated deterministic jitter (16.0 GT/s) | 6041013 | This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range. |
| Tx, Uncorrelated deterministic jitter (2.5 GT/s) | 4011013 | This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range. |
| Tx, Uncorrelated deterministic jitter (2.5 GT/s) | 5011013 | This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range. |
| Tx, Uncorrelated deterministic jitter (2.5 GT/s) | 6011013 | This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range. |
| Tx, Uncorrelated deterministic jitter (32.0 GT/s) | 5051013 | This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range. |
| Tx, Uncorrelated deterministic jitter (32.0 GT/s) | 6051013 | This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range. |
| Tx, Uncorrelated deterministic jitter (5.0 GT/s) | 4021013 | This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range. |
| Tx, Uncorrelated deterministic jitter (5.0 GT/s) | 5021013 | This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range. |
| Tx, Uncorrelated deterministic jitter (5.0 GT/s) | 6021013 | This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range. |
| Tx, Uncorrelated deterministic jitter (64.0 GT/s) | 6061013 | This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range. |
| Tx, Uncorrelated deterministic jitter (8.0 GT/s) | 4031013 | This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range. |
| Tx, Uncorrelated deterministic jitter (8.0 GT/s) | 5031013 | This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range. |
| Tx, Uncorrelated deterministic jitter (8.0 GT/s) | 6031013 | This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range. |
| Tx, Uncorrelated total jitter (16.0 GT/s) | 4041012 | This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Uncorrelated total jitter (16.0 GT/s) | 5041012 | This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range. |
| Tx, Uncorrelated total jitter (16.0 GT/s) | 6041012 | This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range. |
| Tx, Uncorrelated total jitter (2.5 GT/s) | 4011012 | This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range. |
| Tx, Uncorrelated total jitter (2.5 GT/s) | 5011012 | This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range. |
| Tx, Uncorrelated total jitter (2.5 GT/s) | 6011012 | This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range. |
| Tx, Uncorrelated total jitter (32.0 GT/s) | 5051012 | This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range. |
| Tx, Uncorrelated total jitter (32.0 GT/s) | 6051012 | This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range. |
| Tx, Uncorrelated total jitter (5.0 GT/s) | 4021012 | This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range. |
| Tx, Uncorrelated total jitter (5.0 GT/s) | 5021012 | This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range. |
| Tx, Uncorrelated total jitter (5.0 GT/s) | 6021012 | This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range. |
| Tx, Uncorrelated total jitter (64.0 GT/s) | 6061012 | This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range. |
| Tx, Uncorrelated total jitter (8.0 GT/s) | 4031012 | This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range. |
| Tx, Uncorrelated total jitter (8.0 GT/s) | 5031012 | This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range. |
| Tx, Uncorrelated total jitter (8.0 GT/s) | 6031012 | This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range. |
| Tx, Unit interval (16.0 GT/s) | 4041000 | The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification. |
| Tx, Unit interval (16.0 GT/s) | 5041000 | The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification. |
| Tx, Unit interval (16.0 GT/s) | 6041000 | The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification. |

**Table 4** Test IDs and Names (continued)

| Name | TestID | Description |
|---|---|---|
| Tx, Unit interval (2.5 GT/s) | 4011000 | A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The mean recovered TX UI is reported here. |
| Tx, Unit interval (2.5 GT/s) | 5011000 | The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification. |
| Tx, Unit interval (2.5 GT/s) | 6011000 | The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification. |
| Tx, Unit interval (32.0 GT/s) | 5051000 | The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification. |
| Tx, Unit interval (32.0 GT/s) | 6051000 | The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification. |
| Tx, Unit interval (5.0 GT/s) | 4021000 | A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The mean recovered TX UI is reported here. |
| Tx, Unit interval (5.0 GT/s) | 5021000 | The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification. |
| Tx, Unit interval (5.0 GT/s) | 6021000 | The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification. |
| Tx, Unit interval (64.0 GT/s) | 6061000 | The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification. |
| Tx, Unit interval (8.0 GT/s) | 4031000 | The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 4-19 of the PCI Express Base Specification. |
| Tx, Unit interval (8.0 GT/s) | 5031000 | The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification. |
| Tx, Unit interval (8.0 GT/s) | 6031000 | The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification. |

# 4 Instruments

The following table shows the instruments used by this application. The name is required by various remote interface methods.

- Instrument Name — The name to use as a parameter in remote interface commands.
- Description — The description of the instrument.

For example, if an application uses an oscilloscope and a pulse generator, then you would expect to see something like this in the table below:

**Table 5** Example Instrument Information

| Name | Description |
|---|---|
| scope | The primary oscilloscope. |
| Pulse | The pulse generator used for Gen 2 tests. |

and you would be able to remotely control an instrument using:

```
ARSL syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
arsl -a ipaddress -c "SendScpiCommandCustom 'Command=[scpi
command];Timeout=100;Instrument=pulsegen'"

arsl -a ipaddress -c "SendScpiQueryCustom 'Command=[scpi
query];Timeout=100;Instrument=pulsegen'"


C# syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
SendScpiCommandOptions commandOptions = new SendScpiCommandOptions();
commandOptions.Command = "[scpi command]";
commandOptions.Instrument = "[instrument name]";
commandOptions.Timeout = [timeout];
remoteAte.SendScpiCommand(commandOptions);

SendScpiQueryOptions queryOptions = new SendScpiQueryOptions();
queryOptions.Query = "[scpi query]";
queryOptions.Instrument = "[instrument name]";
```

```
queryOptions.Timeout = [timeout];
remoteAte.SendScpiQuery(queryOptions);
```

Here are the actual instrument names used by this application:

**NOTE** The file, "InstrumentInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

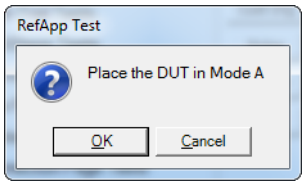
**Table 6** Instrument Names

| Instrument Name | Description |
|---|---|
| Infiniium | The primary oscilloscope |
| PFAGenerator | PFAGenerator |

# 5 Message IDs

During the normal course of operation, an application displays multiple message prompts. The application's remote interface exposes a callback capability which enables remote clients to receive the text found in the prompt and to programmatically select the desired response (OK, Cancel, etc.). In order to determine which message is being received, the remote program could parse the message and look for key words. However, because message text is subject to change, a more reliable approach is to use the "message ID" that is attached to the more frequently-seen messages. The following table shows the IDs of the messages that this application may prompt during nominal operation.

For example, if the application may display the following prompt:




then you would expect to see something like this in the table below:

| Message | ID | Responses | Usage |
|---|---|---|---|
| DUT mode message | 313AEE2F-9EF0-476f-A2EB-29A5C7DE686F | OK=action completed and proceed, Cancel = abort test | App |

- Message – A summary of the message in the prompt.
- ID – A unique code that will never change for this prompt, even if the message text changes (assuming the underlying purpose is maintained).
- Responses – The buttons on the prompt and their actions.
- Usage – The scope of the message:
  - "Common" – This message/ID may be used by other apps.

- "App" — This message/ID is unique to this app.
- "<testID>" — This message/ID is unique to this test ID.

A remote client would then structure the code in its message callback handler as shown below to manage message identification:

```
private static void OnSimpleMessage(object sender, MessageEventArgs e)
{
  if (e.ID == "313AEE2F-9EF0-476f-A2EB-29A5C7DE686F")
  {
    // Add code here to set the DUT in Mode A

    e.Response = DialogResult.OK;
  }
}
```

Here are actual message IDs used by this application:

**NOTE** The file, "MessageInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

**Table 7** Message IDs

| Message | ID | Responses | Usage |
|---|---|---|---|
| Acq Limit: Can't determine minimum bandwidth | 25A86458-151E-413D-B890-FC30CFD5ECAA | OK | Instrument |
| Activating limit will conflict with existing results | 31A39751-6019-41de-89DF-59DB239DF978 | OK=delete conflicting results, Cancel=cancel activation | Instrument |
| Already running tests | 022467B0-6E08-40eb-B4D4-BBB018FBFBC7 | OK | Instrument |
| App startup aborted | C2B67F67-E5D5-4845-8B63-443781223010 | OK | Instrument |
| Can't set memory depth | FFFF1129-BD83-4318-993E-64C94033CEC4 | OK=skip step and continue, Cancel=abort test | Instrument |
| Channel Setup: Unknown scope channel | CDE944EB-F440-4CB1-AFDC-7596461BCD86 | OK | Instrument |
| Compliance/Debug mode change | 9C72A970-8D7D-4b37-9787-48AEEA5DC3F1 | OK=change mode, Cancel=abort action | Instrument |
| Confirmation Required | 37437505-160C-4cc8-BA06-093C12994C1E | OK=continue, Cancel=abort test | Instrument |
| Connection change | 879629E6-78FA-4a87-B247-A9DB4F0D7330 | Abort=abort run, Retry=connection changed - continue run, Ignore=connection not chagned - continue run | Instrument |

**Table 7** Message IDs (continued)

| Message | ID | Responses | Usage |
|---|---|---|---|
| Debug pause (messages vary) | 50B66A97-A6A9-413f-8329-76DFAC492FD6 | OK=resume, Cancel=abort run | Instrument |
| End of run summary | 602F9866-F975-42b7-842C-D8447E5E3FCB | OK | Instrument |
| End of run summary (test aborted) | 124580E4-4486-42d4-B908-C6D0FB2AEE93 | OK | Instrument |
| Error during CSV file generation | C88B1C64-8334-4b15-8727-81F5E2BA2ED4 | OK | Instrument |
| Error during app exit | 81112706-F720-4787-81D3-B22A9B692B41 | OK | Instrument |
| Expected signal not found | 86C74779-322E-4585-A07A-26A2C8FAAC84 | Abort=abort test, Retry=retry failed action, Ignore=skip failed step | Instrument |
| Expected signal not found | 7957D5B8-E62D-4224-A7DD-70361E816A43 | Retry=retry failed action, Cancel=abort test | Instrument |
| InfiniiSim: Not available because scope default prevented | B8461A2C-9F5F-4AF3-94C1-DF77080D517A | OK | Instrument |
| InfiniiSim: Scope doesn't support settings found in project | C9BC2205-8041-448b-AF31-CF602183E989 | OK | Instrument |
| InfiniiSim: Unknown scope channel | 4E5ECAF6-867C-47B3-982D-5F07E2090703 | OK | Instrument |
| Measurement Server no Measure Workers declared | 54A8428D-8E22-4286-AC88-7495821ABA77 | OK=retry, Cancel=abort run | Instrument |
| No test selected | B5D233AD-9EB4-4ac2-A443-A30A13643978 | OK | Instrument |
| PrecisionProbe and InfiniiSim controllers turned off after config change | B4477006-D6D1-4375-9FF7-D8177FFC1BF9 | OK | Instrument |
| PrecisionProbe/PrecisionCable: Not available because scope default prevented | 6E60C9F8-8FBF-419C-B70A-B666FBDE3677 | OK | Instrument |
| PrecisionProbe/PrecisionCable: Scope doesn't support settings found in project | 2FC3B6FA-E28C-4700-9F46-4ABBA86A0D90 | OK | Instrument |
| PrecisionProbe/PrecisionCable: Switch Controller is enabled | 22F46DA8-89AE-4370-A57C-571DCF5BB87E | OK | Instrument |
| PrecisionProbe/PrecisionCable: Unknown scope channel | 6788685B-9E88-47E6-BAE6-862F5BF3C9BA | OK | Instrument |

**Table 7** Message IDs (continued)

| Message | ID | Responses | Usage |
|---|---|---|---|
| Project loaded as read-only (reason) | 98C785F8-D24F-4758-A18D-1CCE61F25371 | OK | Instrument |
| Project loaded with errors | 58AD7A02-1E63-4d77-BC6C-6EF3E37AAD5B | OK | Instrument |
| Project not loaded | B2615E9C-5ED7-4db7-AEAF-2BC25C62B656 | OK | Instrument |
| Project save failed (unauthorized access) | 89DCC194-6254-4902-AE63-B7CCD12C8B2A | OK | Instrument |
| Run paused | FE2CF871-6D4A-4080-8FF9-770075590D9F | OK=resume, Cancel=abort run | Instrument |
| Setting change requires result deletion | 8732A3AB-142C-47e5-86EA-DB737F415DDE | OK=delete results; Cancel=abort change | Instrument |
| Store mode change requires result deletion | 884CDFDE-605E-4d04-B8FD-9B181E7FA468 | OK=delete results, Cancel=abort change | Instrument |
| Switch Matrix controller turned off after config change | FC95EBAA-F33F-4eae-90BB-6A6A8F16E2DF | OK | Instrument |
| Switch Matrix: Auto mode unavailable after config change | 6E5589DC-E073-4818-9E8A-782A75898475 | OK | Instrument |
| Switch Matrix: Auto mode unavailable for model, all settings will be reset | F78BD2E2-BF29-42e0-98F8-23B6CE565B08 | OK=go auto do reset, Cancel=abort action | Instrument |
| Switch Matrix: Confirm Auto mode | D5E1A12E-6218-4416-8451-5F9415D924BF | OK=go auto, Cancel=stay manual | Instrument |
| Switch Matrix: Obsolete items in settings discarded | 0C45BD20-E0C2-481e-A3B6-9C1A26C2103A | OK | Instrument |
| Switch Matrix: Reconnect drivers | 047FE44F-B251-49fa-B3C7-5590317230CD | Yes=use saved addresses, No=prompt for new addresses, Cancel=reset all settings | Instrument |
| Switch Matrix: Remove all InfiniiSim settings | C5560182-73BE-4901-941E-3DAEC9F07B33 | OK=remove, Cancel=abort action | Instrument |
| Switch Matrix: User cancelled settings load | 50F3FB70-AA6B-488e-8CFA-62CDA756F746 | OK | Instrument |
| SwitchMatrix: Correction reset due to application route change | 95FEA629-3BE1-4288-BA34-426516018B07 | OK=Accept new routing, Cancel=Reset switch matrix settings | Instrument |
| SwitchMatrix: Instrument already connected to another driver | 08556148-4D63-4edd-B894-22916F39849A | OK | Instrument |

**Table 7** Message IDs (continued)

| Message | ID | Responses | Usage |
|---|---|---|---|
| SwitchMatrix: Max num drivers exceeded | 7D8994AB-FCC2-4294-87B3-19B972BB6510 | OK | Instrument |
| SwitchMatrix: Reset after drive reconnect fail | CF3E93B6-77FA-4FD7-B656-D286BE1C7C75 | OK | Instrument |
| SwitchMatrix: Reset after drive reconnect fail | D298A4B8-F077-49BE-9CB2-AE6C14FB4705 | OK | Instrument |
| SwitchMatrix: Unexpected multi-SPDT module | 2723591D-55A9-44F3-9318-B732995D9427 | OK | Instrument |
| SwitchMatrix: Unknown current switch state | ECE6535B-5C1A-4688-9E45-FB255435CC92 | OK | Instrument |
| SwitchMatrix: Will reset due to requested change | 420FCEA9-0FF4-4088-B47A-3189413EA0AD | OK=Allow the reset, Cancel=Abort the original requested change | Instrument |
| Unknown EEyeLocation parameter | FCA1C61B-D2EA-4671-AD48-9C080A6C6039 | OK | Instrument |
| Upgrade app to open project | 794C6148-ADF4-4b24-895D-74D94B76F8AE | OK | Instrument |

# Index


## C

configuration variables and values, 9
copyright, 2

## I

IDs and names of tests, 39
IDs, message, 93
instrument names, 91

## M

message IDs, 93

## N

names and IDs of tests, 39
names of instruments, 91
notices, 2

## P

programming, introduction to, 7

## R

Remote Programming Toolkit, 8

## T

test names and IDs, 39

## V

variables and values, configuration, 9

## W

warranty, 2