D9050DDRC DDR5 Test Application - Methods of Implementation

KEYSIGHT

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Warranty

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CAUTION

A CAUTION notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

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Keysight D9050DDRC DDR5 Test Application

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1 Overview

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DDR5 Automated Testing—At a Glance

The Keysight D9050DDRC DDR5 Test Application helps you verify that the transmitter device under test (DUT) conforms to the pre-defined limits using the supported Keysight Infiniium Oscilloscopes. The Keysight D9050DDRC DDR5 Test Application:

· Lets you select individual or multiple tests to run.
· Lets you identify the device being tested and its configuration.
· Shows you how to make oscilloscope connections to the device under test.
· Automatically checks for proper oscilloscope configuration.
· Automatically sets up the oscilloscope for each test.
· Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
· Creates a printable HTML report of the tests that have been run.

NOTE | **The tests performed by the Keysight D9050DDRC DDR5 Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.**

Required Equipment and Software

In order to run the DDR5 automated tests, you need the following equipment and software:

Hardware

- Use one of the following Oscilloscope models. Refer to www.keysight.com for the respective bandwidth ranges.
  - Keysight DSO9000A-Series, DSO90000A-Series and DSOX90000A/Q/Z/V-Series
    - Oscilloscopes with a minimum bandwidth of 8GHz (recommended) for accurate measurements. For faster speed grade devices, a minimum bandwidth of 13GHz bandwidth is recommended.
  - Keysight UXR Oscilloscopes
- Any PC motherboard system that supports DDR5 memory DIMM(s)
- DUT: Saved waveform and PulseGen generated signal
- InfiniiMax probe amplifiers:
  - N1169A – 12GHz InfiniiMax II probe amplifier
  - MX0020A - 10GHz InfiniiMax Ultra Probe Amplifier
  - MX0021A - 13GHz InfiniiMax Ultra Probe Amplifier
  - MX0022A - 16GHz InfiniiMax Ultra Probe Amplifier
  - MX0023A - 25GHz InfiniiMax RC Probe Amp
  - MX0024A - 20GHz InfiniiMax Ultra Probe Amplifier
  - MX0025A - 25GHz InfiniiMax Ultra Probe Amplifier
- InfiniiMax probe heads – InfiniiMax II probe heads and accessories (compatible with 9000 Series and 90000 Series, use N5442A precision BNC adapter with 90000X/Q Series):
  - N5381A – InfiniiMax II 12GHz differential solder-in probe head and accessories
  - N5382A – InfiniiMax II 12GHz differential browser
  - E2677A – InfiniiMax II 12GHz differential solder-in probe head and accessories
  - N5425A – InfiniiMax II 12GHz ZIF probe head
  - N5426A – InfiniiMax II ZIF tips (×10)
- InfiniiMax Ultra/RC Probe Amplifiers probe heads and accessories:
  - MX0100A - InfiniiMax Micro Probe Head
  - MX0103A - Bullet Adapter
- Precision 3.5 mm BNC to SMA male adapter, Keysight p/n 54855-67604, qty = 2 (provided with the Keysight 54855A and 80000B series oscilloscopes)
- 50-ohm Coax Cable with SMA Male Connectors – 24-inch or less RG-316/U or similar, qty = 2, matched length
- Keyboard, qty = 1, (provided with the Keysight Infiniium Oscilloscope)
- Mouse, qty = 1, (provided with the Keysight Infiniium Oscilloscope)
- Keysight also recommends using a second monitor to view the test application.

Software

- The minimum version of Infiniium Oscilloscope Software (see the Keysight D9050DDRC DDR5 Test Application Release Notes)
- Keysight D9050DDRC DDR5 Test Application software
- Keysight E2688A Serial Data Analysis and Clock Recovery software (for clock recovery)

Licensing information

Refer to the *Data Sheet* for the DDR5 Test Application to know about the licenses you must install along with other optional licenses. Visit "http://www.keysight.com/find/D9050DDRC" and in the web page's **Document Library** tab, you may view the associated Data Sheet.

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

The licensing format for Keysight License Manager 6 differs from its predecessors. See "Installing the License Key" on page 15 to see the difference in installing a license key using either of the applications on your machine.

NOTE   To launch the DDR5 Validation Test Application, you must have the SDA and DDR5 licenses installed.

Additional Licenses

1   InfiniiSim feature requires the following licenses:
- InfiniiSim Basic or InfiniiSim Advanced

2   Precision Probe/Cable feature requires the following licenses:
- Precision Probe or Precision Probe Advanced

In This Book

This manual describes the tests that are performed by the Keysight D9050DDRC DDR5 Test Application in more detail.

- Chapter 2, "Installing the Test Application and Licenses" shows how to install the automated test application software and licenses (if it was purchased separately).
- Chapter 3, "Preparing to Take Measurements" shows how to start the Keysight D9050DDRC DDR5 Test Application and gives a brief overview of the required preparation and how the application is used.
- Chapter 4, "Burst Data tests" describes the methods of implementation for electrical and timing tests performed on READ and WRITE bursts of the DDR5 differential signals.
- Chapter 5, "Continuous Data tests" describes the methods of implementation for electrical and jitter tests performed on continuous DDR5 differential and single-ended Data Strobe signals.
- Chapter 6, "Clock (Single Ended) tests" describes the methods of implementation for tests performed on continuous DDR5 single-ended Clock signals.
- Chapter 7, "CA (Command Address) tests" describes the methods of implementation for tests performed on DDR5 Command & Address signals.
- Chapter 8, "Stressed Eye tests" describes the methods of implementation for DDR5 stressed eye tests .

See Also

The Keysight D9050DDRC DDR5 Test Application's Online Help, which describes:

- Starting the DDR5 Test Application
- Creating or Opening a Test Project
- Setting Up the Test Environment
- Selecting Tests
- Configuring Tests
- Verifying Physical Connections
- Running Tests
- Configuring Automation in the Test Application
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
- Additional Settings in the Test App

2 Installing the Test Application and Licenses

If you purchased the D9050DDRC DDR5 Test Application separate from your Infiniium oscilloscope, you must install the software and license key.

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Installing the Test Application

1 Make sure you have the minimum version of Infiniium Oscilloscope software (see the D9050DDRC release notes). To ensure that you have the minimum version, select **Help > About Infiniium...** from the main menu.

2 To obtain the DDR5 Test Application, go to Keysight website: "http://www.keysight.com/find/D9050DDRC".

3 In the web page's **Free Trials** tab, click the **Details and Download** button to view instructions for downloading and installing the application software.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

1 Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.
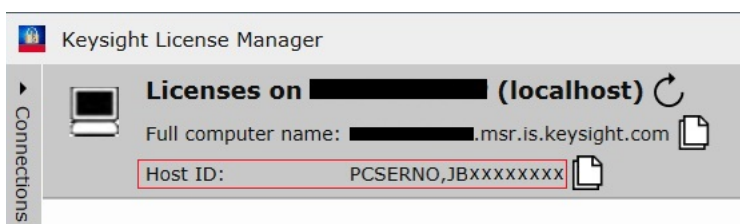
Figure 1   Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch **Keysight License Manager**.

3 From the **Configuration** menu, use one of the options to install each license file.
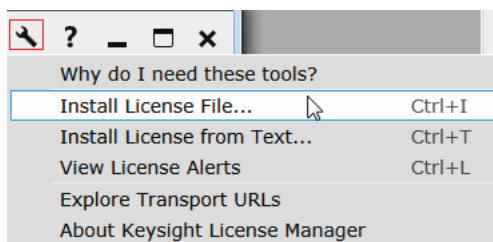
Figure 2   Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

1   Launch **Keysight License Manager 6** on your machine, where you wish to run the Test Application and its features.

2   Copy the **Host ID**, which is the first set of alphanumeric value (as highlighted in Figure 3) that appears in the **Environment** tab of the application. Note that x indicates numeric values.
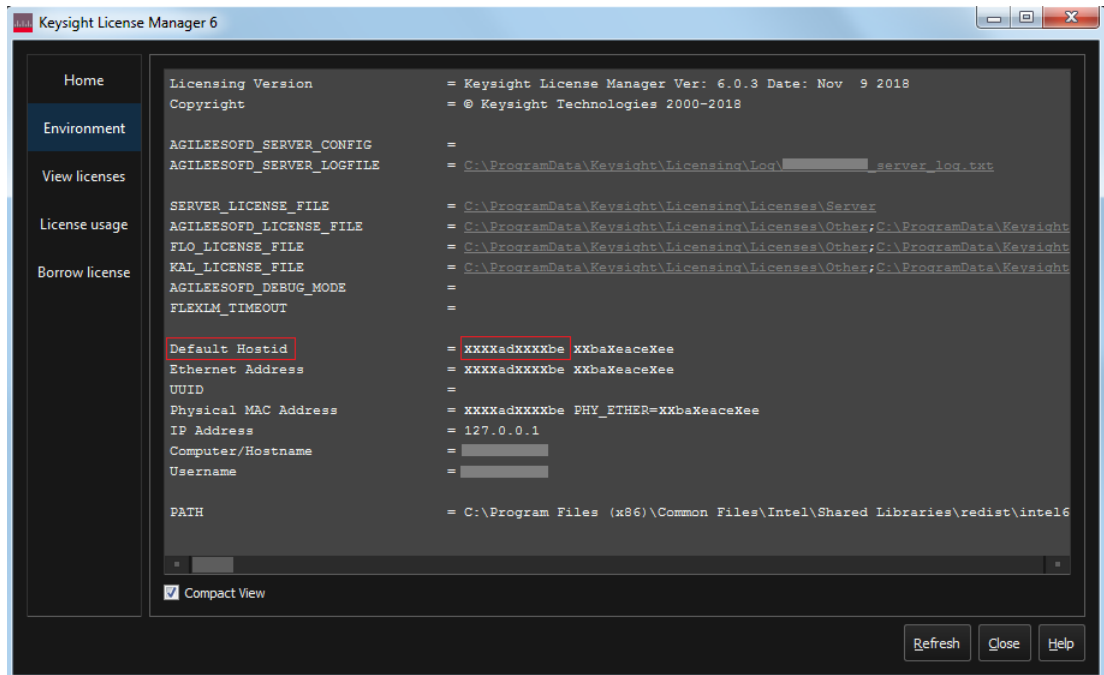
Figure 3   Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

1   Save the license files on the machine, where you wish to run the Test Application and its features.

2   Launch **Keysight License Manager 6**.

3   From the **Home** tab, use one of the options to install each license file.
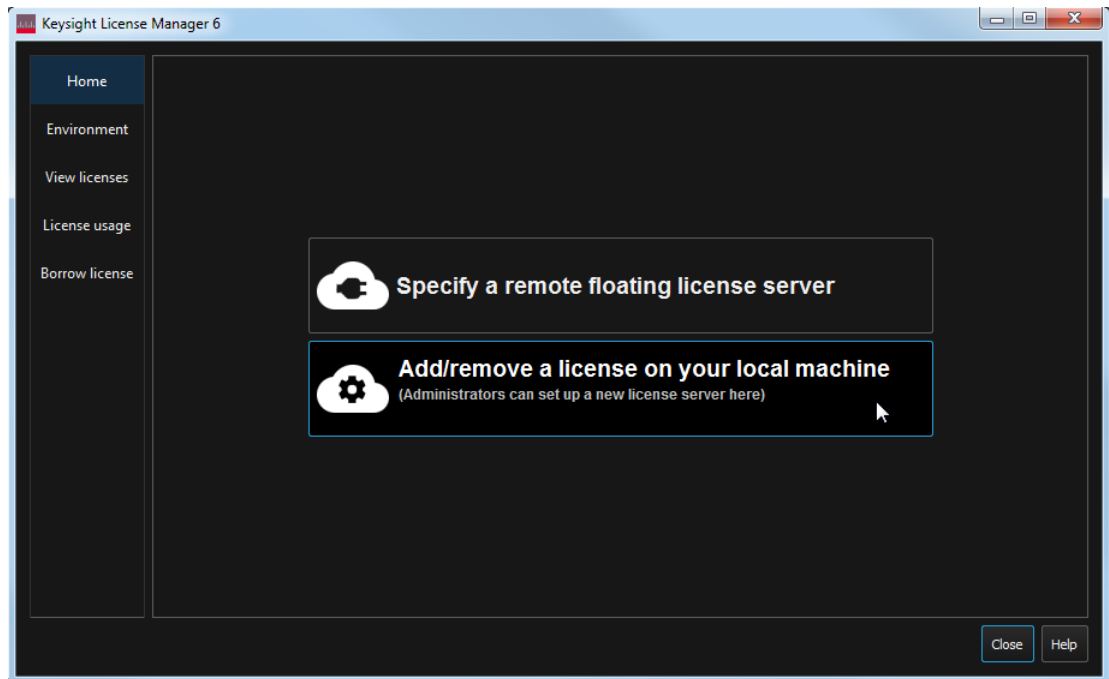
Figure 4   Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

3 Preparing to Take Measurements

Before running the automated tests, you must calibrate the oscilloscope and probe. No test fixture is required for this application. After the oscilloscope and probe have been calibrated, you are ready to start the DDR5 Test Application and perform the measurements.

Calibrating the Oscilloscope

If you have not already calibrated the oscilloscope, refer to the *User Guide* for the respective Oscilloscope you are using.

> **NOTE**   If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.

> **NOTE**   If you switch cables between channels or other Oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the DDR5 Test Application

1   Ensure that the DDR5 Device Under Test (DUT) is operating and set to desired test modes. To start the DDR5 Test Application: From the Infiniium Oscilloscope's main menu, select **Analyze > Automated Test Apps > D9050DDRC DDR5 Test App**.
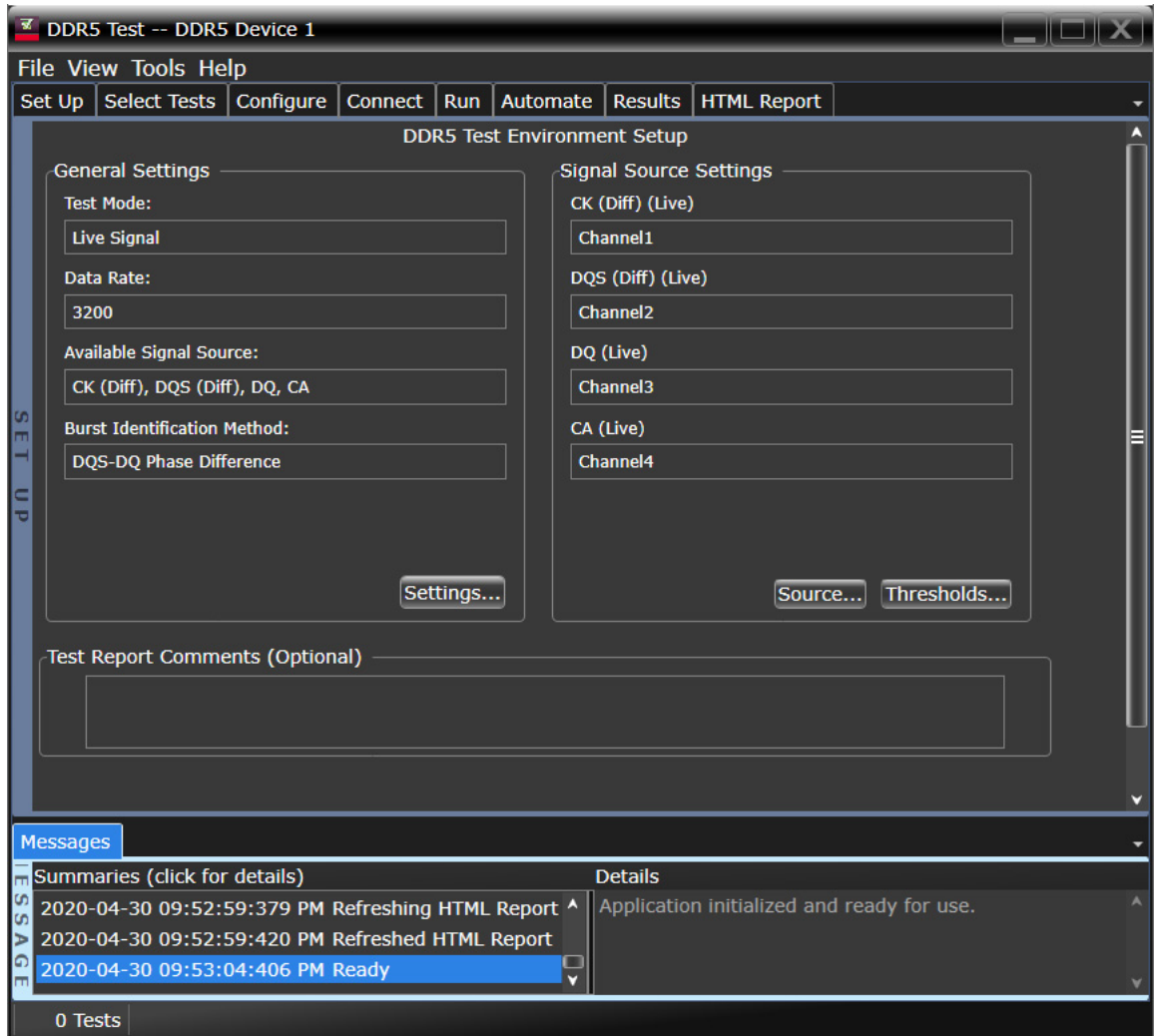
Figure 5   DDR5 Test Application Main Window

To understand the functionality of the various features in the user interface of the Test Application, refer to the *Keysight D9050DDRC DDR5 Test Application Online Help* available in the **Help** menu.

The task flow pane and the tabs in the main pane show the steps you take in running the automated tests:

Tab	Description
Set Up	Lets you identify and set up the test environment, including information about the device under test. The Test App includes relevant information in the final HTML report.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (for example, channels used in test, voltage levels, etc.).
Connect	Shows you how to connect the oscilloscope to the device under test for the tests that are to be run.
Run	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automate	Lets you construct scripts of commands that drive execution of the application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE   In the **Configure** tab, the values for all such Configuration parameters that are Oscilloscope-dependent, will correspond to the Oscilloscope Model (DSOs or UXRs), where you are running the Test Application.

Filtering tests in the DDR5 Test Application

The DDR5 Test Application filters the list of tests based on the options you select in the **Signal Source** and **Signal Operation Mode** features.

1   In the **Set Up** tab, click **Settings...**.
2   In the **DDR5 General Setup** window that appears,

Figure 6   DDR5 General Setup window

    a   Select a set of signal combinations from the options that appear in the **Signal Source** drop-down field.
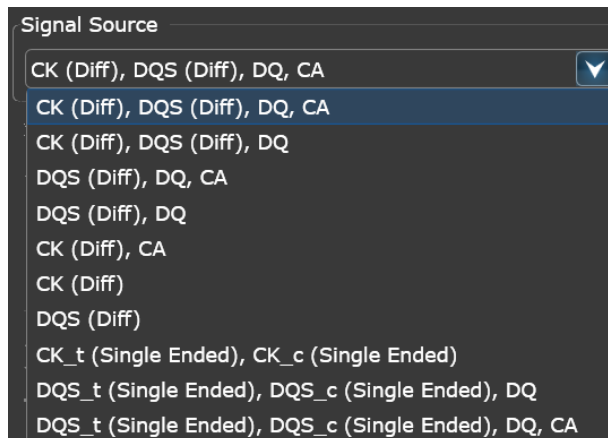
Figure 7   Set of signal combinations in Signal Source drop-down

b   In the **Signal Operation Mode** area,

· For the differential Clock and Data Strobe signals, set the mode either as **Burst** or as **Continuous**.

· By default, **DQS (Diff)** is set to **Burst**, so that you may configure DQS Burst data mode options by clicking the **Burst DQS Options...** button. For more information regarding setting Burst DQS Options, refer to the *Keysight D9050DDRC DDR5 Test Application Online Help*.

· For single ended Clock and Data Strobe signal source options, only **Continuous** mode can be applied.

· If **DQS (Diff)** is set to **Continuous**, the **DQ** mode options become available. By default, the DDR5 Test Application sets the DQ signal operation mode to **DataPattern**. All Jitter and Stressed Eye tests appear for this mode. For the DQ Jitter tests (that require Continuous DQ signal for processing) to appear, select **Continuous1010**.

Connections for Compliance Tests

To run tests using the DDR5 Test Application, you must make proper connections between the Oscilloscope and the DUT. Once you select the tests that you want to run, refer to the **Connect** tab in the DDR5 Test Application for connection instructions and the connection diagram, similar to the one shown in Figure 8.
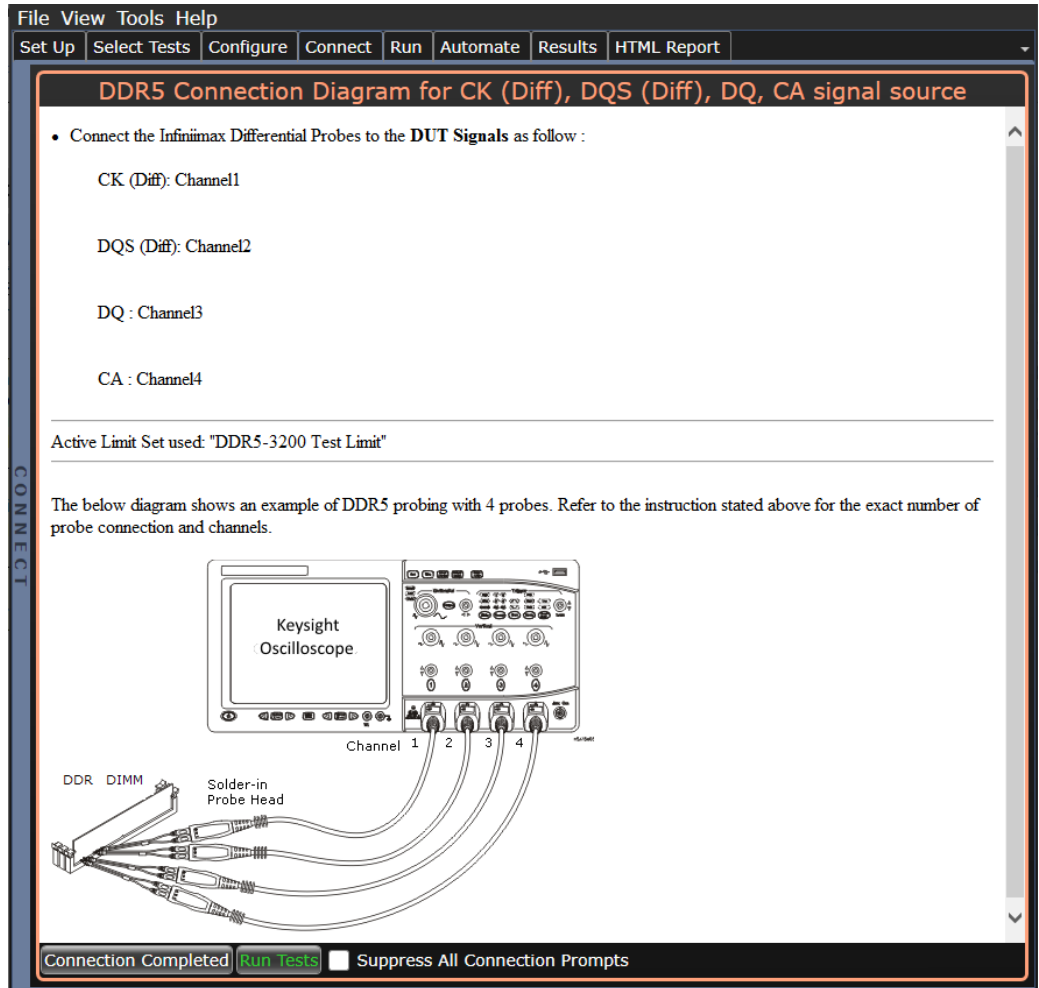
Figure 8   Physical connection diagram and instructions for compliance tests

4 Burst Data tests

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READ Burst

Test Availability Conditions

All tests in this test group appear for the following configuration in DDR5 General Setup window:

Signal Source:

- Any signal set including CK (Diff), DQS (Diff), DQ

> **NOTE**   Some tests appear only when CK (Diff) is included in the Signal Source along with DQS (Diff) and DQ.

Signal Operation Mode:

- CK (Diff) — Burst
- DQS (Diff) — Burst
- DQ — Not applicable

Burst DQS options:

- Read Preamble Mode
    - DDR5_1tCK
    - DDR5_2tCK_0010
    - DDR5_2tCK_1110
    - DDR5_3tCK
    - DDR5_4tCK
- Read Postamble Mode
    - DDR5_0.5tCK
    - DDR5_1.5tCK
- Read Vsw1 (V)
- Read Vsw2 (V)

tDQSCK

> **NOTE**   This test appears only when CK (Diff) is included in the Signal Source along with DQS (Diff) and DQ.

Test ID: 14500

Test Overview: The purpose of this test is to verify the time interval from the data strobe output (DQS rising edge) access time to the nearest rising edge of the clock.

Test Procedure:
1   Acquire and split read and write burst of the acquired signal.
2   Take the first valid READ burst found.
3   Find all valid rising DQS crossings at 0V in the specified burst.
4   For all DQS crossings found, locate the nearest crossing at the rising edge of the Clock at 0V.
5   Measure as tDQSCK the time difference from the DQS crossing to the corresponding Clock crossing (found in the previous step).

6   Report the measured tDQSCK.

Expected/
Observable Results: The measured value of tDQSCK shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tRPRE

Test ID: 14530

Test Overview: The purpose of this test is to verify the Read preamble region of the DQS signal.

Test Procedure: 1   Acquire and split read and write burst of the acquired signal.
2   Validate the Read and Write bursts obtained in the previous step. Disregard the invalid bursts.
3   Take the first valid READ burst found.
4   Find tLZBeginPoint on the DQS signal of the specified burst.
5   Find the first rising edge (excluding preamble pattern) on DQS of the found burst.
tRPRE is the time interval between the rising DQS edge and tLZBeginPoint.
6   Report tRPRE.

Expected/
Observable Results: The measured value of tRPRE shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tRPST

Test ID: 14540

Test Overview: The purpose of this test is to verify the Read postamble region of the DQS signal.

Test Procedure: 1   Acquire and split the Read and Write burst of the acquired signal.
2   Validate the Read and Write bursts obtained in the previous step. Disregard the invalid bursts.
3   Take the first valid READ burst found.
4   Find tHZEndPoint on the DQS signal of the specified burst.
5   Find the last falling edge on DQS prior to tHZEndPoint found.
tRPST is the time interval between the falling DQS edge's crossing and tHZEndPoint.
6   Report tRPST.

Expected/
Observable Results: The measured value of tRPST shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tLZDQS

> **NOTE**   This test appears only when CK (Diff) is included in the Signal Source along with DQS (Diff) and DQ.

Test ID: 14510

Test Overview: The purpose of this test is to verify the time when DQS starts driving (*from High-impedance state to High/Low state) to the nearest rising clock signal crossing.

Test Procedure: 1   Acquire and split Read and Write burst of the acquired signal.

2   Validate the Read and Write bursts obtained in the previous step. Disregard the invalid bursts.

3   Take the first valid READ burst found.

4   Find tLZBeginPoint on the DQS signal of the said burst.

5   Find the nearest Clock rising edge.
tLZ(DQS) is the time interval between the Clock rising edge's crossing point and tLZBeginPoint.

6   Report tLZ(DQS).

Expected/ Observable Results: The value of measured tLZ(DQS) shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tHZDQS

NOTE   This test appears only when CK (Diff) is included in the Signal Source along with DQS (Diff) and DQ.

Test ID: 14520

Test Overview: The purpose of this test is to verify the time when DQS is no longer driving (from High state OR Low state to the High-impedance state) to the reference clock signal crossing.

Test Procedure: 1   Acquire and split read and write burst of the acquired signal.

2   Validate the Read and Write bursts obtained in the previous step. Disregard the invalid bursts.

3   Take the first valid READ burst found.

4   Find tHZEndPoint on the DQS signal of the said burst.

5   Find the nearest Clock rising edge.
tHZ(DQS) is the time interval between Clock rising edge's crossing point and tHZEndPoint.

6   Report tHZ(DQS).

Expected/ Observable Results: The value of measured tHZ(DQS) shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

VOHdiff(AC)

Test ID: 13510

Test Overview: The purpose of this test is to verify the high level differential output voltage value of the test signal within the read burst.

Test Procedure: 1   Acquire and split read and write burst of the acquired signal.

2   Take the first valid READ burst found.

3   Find all valid Strobe positive pulses in the said burst.
A valid Strobe positive pulse starts at the 0V crossing at the valid Strobe rising edge and ends at the 0V crossing at the following valid Strobe falling edge.

4   Zoom into the first pulse and perform V_{TOP}.
Take the V_{TOP} measurement as $V_{OHdiff (AC)}$ value.

5   Repeat step 4 with the rest of the positive pulses in the specified burst.

6   Determine the worst result from the set of $V_{OHdiff (AC)}$ measured.

Expected/
Observable Results: The worst measured $V_{OHdiff\ (AC)}$ shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

VOLdiff(AC)

Test ID: 13515

Test Overview: The purpose of this test is to verify the low level differential output voltage value of the test signal within the read burst.

Test Procedure:

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid Strobe negative pulses in the specified burst.
   A valid Strobe negative pulse starts at the 0V crossing at the valid Strobe falling edge and ends at the 0V crossing at the following valid Strobe rising edge.

4 Zoom into the first pulse and perform V_{BASE}.
   Take the V_{BASE} measurement as $V_{OLdiff\ (AC)}$ value.

5 Repeat step 4 with the rest of the negative pulses in the specified burst.

6 Determine the worst result from the set of $V_{OLdiff\ (AC)}$ measured.

Expected/
Observable Results: The worst measured $V_{OLdiff\ (AC)}$ shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

SRQdiffR

Test ID: 13500

Test Overview: The purpose of this test is to verify the differential output slew rate for rising edge of the test signal within the read burst.

Test Procedure:

1 Acquire and split the read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Calculate $V_{OLdiff(AC)}$ and $V_{OHdiff(AC)}$ using the equation:

   $V_{OHdiff(AC)} = 0.75 * Vdiffpk\text{-}pk$

   $V_{OLdiff(AC)} = 0.25 * Vdiffpk\text{-}pk$

   Then use calculated $V_{OHdiff(AC)}$ and $V_{OLdiff(AC)}$ to defined strobe edge level requirement.

4 Find all the valid Strobe rising edges in the specified burst.
   A valid Strobe rising edge starts at $V_{OLdiff(AC)}$ crossing and ends at the following $V_{OHdiff(AC)}$ crossing.

5 Calculate SRQdiffR using the equation:

$$SRQdiffR = [V_{OHdiff(AC)} - V_{OLdiff(AC)}] / DeltaTRdiff$$

6 Determine the worst result from the set of SRQdiffR measured.

Expected/
Observable Results: The measured value of SRQdiffR for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

SRQdiffF

Test ID:	13505
Test Overview:	The purpose of this test is to verify the differential output slew rate for falling edge of the test signal within the read burst.

Test Procedure:

1   Acquire and split the read and write burst of the acquired signal.

2   Take the first valid READ burst found.

3   Calculate $V_{OLdiff(AC)}$ and $V_{OHdiff(AC)}$ using the equation:

$V_{OHdiff(AC)} = 0.75 * Vdiffpk\text{-}pk$

$V_{OLdiff(AC)} = 0.25 * Vdiffpk\text{-}pk$

Then use calculated $V_{OHdiff(AC)}$ and $V_{OLdiff(AC)}$ to defined strobe edge level requirement.

4   Find all the valid Strobe falling edges in the specified burst.
A valid Strobe falling edge starts at $V_{OHdiff(AC)}$ crossing and ends at the following $V_{OLdiff(AC)}$ crossing.

5   Calculate SRQdiffF using the equation:

$$SRQdiffF = [V_{OHdiff(AC)} - V_{OLdiff(AC)}] / DeltaTFdiff$$

6   Determine the worst result from the set of SRQdiffF measured.

Expected/ Observable Results:	The measured value of SRQdiffF for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

VOH(AC)

Test ID:	13520
Test Overview:	The purpose of this test is to verify the high level DQ output voltage value of the test signal within a valid read burst.

Test Procedure:

1   Acquire and split the read and write burst of the acquired signal.

2   Take the first valid READ burst found.

3   Find all valid positive pulses in the specified burst.
A valid positive pulse starts at the VREFDQ configured in the app and ends at middle crossing at the following valid falling edge.

4   Zoom in on the first valid positive pulse and perform V_{TOP} measurement.
Take the V_{TOP} measurement results as $V_{OH(AC)}$ value.

5   Continue the previous step with the rest of the valid positive pulses that were found in the burst.

6   Determine the worst result from the set of $V_{OH(AC)}$ measured.

Expected/ Observable Results:	The measured value of $V_{OH(AC)}$ for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

VOH(DC)

Test ID:	13525
Test Overview:	The purpose of this test is to verify the high level DQ output voltage value of the test signal within a valid read burst.

Test Procedure:

1   Acquire and split the read and write burst of the acquired signal.

2   Take the first valid READ burst found.

3   Find all valid positive pulses in the specified burst.
    A valid positive pulse starts at the middle crossing at valid rising edge and ends at middle crossing at the following valid falling edge.

4   Zoom in on the first valid positive pulse and perform V_{TOP} measurement.
    Take the V_{TOP} measurement results as $V_{OH(DC)}$ value.

5   Continue the previous step with the rest of the valid positive pulses that were found in the burst.

6   Determine the worst result from the set of $V_{OH(DC)}$ measured.

Expected/ Observable Results: The measured value of $V_{OH(DC)}$ for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

VOL(AC)

Test ID: 13530

Test Overview: The purpose of this test is to verify the low level DQ output voltage value of the test signal within a valid read burst.

Test Procedure:
1   Acquire and split the read and write burst of the acquired signal.

2   Take the first valid READ burst found.

3   Find all valid negative pulses in the specified burst.
    A valid negative pulse starts at the middle crossing at valid falling edge and ends at middle crossing at the following valid rising edge.

4   Zoom in on the first valid negative pulse and perform V_{BASE} measurement.
    Take the V_{BASE} measurement results as $V_{OL(AC)}$ value.

5   Continue the previous step with the rest of the valid negative pulses that were found in the burst.

6   Determine the worst result from the set of $V_{OL(AC)}$ measured.

Expected/ Observable Results: The measured value of $V_{OL(AC)}$ for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

VOL(DC)

Test ID: 13535

Test Overview: The purpose of this test is to verify the DQ output low level voltage value of the test signal within a valid read burst.

Test Procedure:
1   Acquire and split the read and write burst of the acquired signal.

2   Take the first valid READ burst found.

3   Find all valid negative pulses in the specified burst.
    A valid negative pulse starts at the middle crossing at valid falling edge and ends at middle crossing at the following valid rising edge.

4   Zoom in on the first valid negative pulse and perform V_{BASE} measurement.
    Take the V_{BASE} measurement results as $V_{OL(DC)}$ value.

5   Continue the previous step with the rest of the valid negative pulses that were found in the burst.

6   Determine the worst result from the set of $V_{OL(DC)}$ measured.

Expected/ Observable Results: The measured value of $V_{OL(DC)}$ for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

SRQseR

Test ID:	13540
Test Overview:	The purpose of this test is to verify the single-ended output slew rate for rising edge of the test signal within the read burst.

Test Procedure:

1. Acquire and split the read and write burst of the acquired signal.
2. Take the first valid READ burst found.
3. Find all the valid rising edges in the specified burst.
   A valid rising edge starts at $V_{OL(AC)}$ crossing and ends at the following $V_{OH(AC)}$ crossing.
4. For all the valid rising edges, find the transition time, DeltaTRdiff.
   DeltaTRdiff is the time starting at $V_{OL(AC)}$ crossing and ending at the following $V_{OH(AC)}$ crossing.
5. Calculate SRQseR using the equation:

$$SRQseR = [V_{OH(AC)} - V_{OL(AC)}] / DeltaTRdiff$$

6. Determine the worst result from the set of SRQseR measured.

Expected/ Observable Results: The calculated Rising Slew (SRQseR) value for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

SRQseF

Test ID:	13545
Test Overview:	The purpose of this test is to verify that the single-ended output slew rate for falling edge of the test signal within the read burst.

Test Procedure:

1. Acquire and split the read and write burst of the acquired signal.
2. Take the first valid READ burst found.
3. Find all the valid falling edges in the specified burst.
   A valid falling edge starts at $V_{OH(AC)}$ crossing and ends at the following $V_{OL(AC)}$ crossing.
4. For all the valid falling edges, find the transition time, DeltaTFdiff.
   DeltaTFdiff is the time starting at $V_{OH(AC)}$ crossing and ending at the following $V_{OL(AC)}$ crossing.
5. Calculate SRQseF using the equation:

$$SRQseF = [V_{OL(AC)} - V_{OH(AC)}] / DeltaTFdiff$$

6. Determine the worst result from the set of SRQseF measured.

Expected/ Observable Results: The calculated Falling Slew (SRQseF) value for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

WRITE Burst

Test Availability Conditions

All tests in this test group appear for the following configuration in DDR5 General Setup window:

Signal Source:

· Any signal set including CK (Diff), DQS (Diff), DQ

NOTE Some tests appear only when CK (Diff) is included in the Signal Source along with DQS (Diff) and DQ.

Signal Operation Mode:

· CK (Diff) — Burst
· DQS (Diff) — Burst
· DQ — Not applicable

Burst DQS options:

· Write Preamble Mode
  · DDR5_2tCK
  · DDR5_3tCK
  · DDR5_4tCK
· Write Postamble Mode
  · DDR5_0.5tCK
  · DDR5_1.5tCK
· Write Vsw1 (V)
· Write Vsw2 (V)

tDQS2DQ

Test ID: 14050

Test Overview: The purpose of this test is to verify the tDQS2DQ parameter.

NOTE To obtain a valid measurement result, this test requires a transitioning bit at the first valid bit in the DQ bus. Otherwise, this test uses the first opening in the eye diagram as the first transition bit, which may yield undesirable results.

Test Procedure: 1   Set up the oscilloscope:

a   Using UDF methodology, separate Write burst and return the filtered DQS signals as recovered clock for eye folding later.

b   Set up measurement threshold values for the DQ channel and the DQS channel input.

c   Set up vertical scale values for DQ channel and DQS channel input.

d   Turn ON Color Grade Display option.

e   Set up Mask Test settings.

f   Set up Clock Recovery on SDA.
Explicit clock, Source = filtered DQS, Rise Edge

g   Turn ON Real Time Eye on SDA.

2   Realign the eye opening of the first transition DQ bit to the center of the screen:

a   Increase the search range on the screen to the range specified in the 'First DQ Transition Search Range (ps)', so that the crossing point of the eye is visible on the screen.

b   Use the Histogram feature to find the first crossing point at 'VRefDQ' level horizontally across the screen.

c   Skip/pad the number of bit/bits by the value specified in the configuration option Padding for First DQ Bit.

d   Realign the center of the eye to the middle time position.

3   Perform Mask Testing:

a   Set the Mask Test Run setting to 'Forever'.

b   Load the mask file and start the Mask Test.

c   Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

4   Determine and store the Vcent value.

There is an option to derive Vcent, which depends on the "Vcent Evaluation Mode" configuration option.

- If the "Vcent Evaluation Mode" option is set to "User defined Vcent", the value of Vcent follows the value of the "User Defined Vcent" configuration option.

- If the "Vcent Evaluation Mode" option is set to "Widest eye opening level", the application evaluates Vcent value from the level of widest eye opening on the generated eye diagram.

The detailed procedure for "Widest eye opening level" is:

a   The Vcent level search ranges from 40% to 60% of the eye amplitude (eye height measured at the center of the eye diagram).

b   Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV. The voltage level at the widest eye opening is used as Vcent.

5   Use Histogram measurements to determine the center location of the eye diagram at Vcent level and denote it as EyeCenterLoc.

6   Determine the location of the filtered DQS rising edges used in the recovered clock and denote it as FilteredDQSLoc.

7   Compute the final test result using the equation:
tDQS2DQ = EyeCenterLoc - FilteredDQSLoc

Expected/
Observable Results: The measured value of tDQS2DQ for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

Write Eye Diagram

Test ID: 14090

Test Overview: The purpose of this test is to automate all the required setup procedures required in order to generate an eye diagram for the DDR5 data WRITE cycle.
The additional feature of having a mask test is that it allows users to perform evaluations and debugging on the eye diagram created.

NOTE   To obtain a valid measurement result, this test requires a transitioning bit at the first valid bit in the DQ bus. Otherwise, this test uses the first opening in the eye diagram as the first transition bit, which may yield undesirable results.

Test Procedure: 1   Acquire and split read and write burst of the acquired signal.

2   Gather the list of start time of each Write Burst.

3   Gather the list of end time of each Write Burst.

4   Save acquired DQS into new waveform file in BIN format. Name it "DQS.bin".

5   Measure VMinDQS which is the minimum voltage of DQS for the whole acquisition.

6   Modify "DQS.bin" waveform file to ignore unwanted region. It is done where within each of the region below, set the sampling voltage at VMinDQS.

- Region #1: from start of acquisition to start time of Write burst #1.

- Region #2: from end time of Write burst #1 to start time of Write burst #2. Continue this until from end time of Write burst #n-1 to start time of Write burst #n. note n=number of Write burst.

- Region #3: from end time of the last Write burst to the end of acquisition.

7   Rename modified "DQS.bin" into "DQSEyeFilt.bin".

8   If DFE mode is Auto/Manual

- Load acquired DQ signal into WMemory3.

- Perform DFE setting where source is WMemory3. Set Display as function.

- Save equalization output as BIN file.

9   If DFE mode is Auto/Manual

- Load BIN file(post DFE DQ) into WMemory2.

  If DFE is OFF

- Load acquired DQ signal into WMemory2.

10   Load "DQSEyeFilt.bin" into WMemory4. Then use Function2 as "Magnify/Duplicate" of Loaded Waveform Memory.

11   Setup Clock Recovery settings on SDA.

- Explicit clock, Source = Function2(DQSEyeFilt), Rise/Fall Edge

12   Setup measurement threshold values for the Function3(Data) and the Function2(DQSEyeFilt).

13   Setup fix time scale and time position values for Function3(Data) and Function2(DQSEyeFilt).

14   Turn ON Color Grade Display option.

15   Identify the X1 value for re-adjustment of selected test mask.

16   Setup Mask Test settings.

17   Turn ON Real Time Eye on SDA.

18   Start mask test until eye diagram folded.

19 Perform Eye Width Measurement:

  a   Set Histogram orientation into Horizontal

  b   Set:

  X1= left boundary of screen

  X2= Center of "widest opening voltage"

  Y1= widest opening voltage

  Y2= widest opening voltage

  c   EyeWidthT1= Histogram Max

  d   Set:

  X1= Center of "widest opening voltage"

  X2= right boundary of screen

  Y1= widest opening voltage

  Y2= widest opening voltage

  e   EyeWidthT2= Histogram Min

  f   Calculate EyeWidth = EyeWidthT2 - EyeWidthT1

20 Perform Eye Height Measurement:

  a   Set Histogram orientation into Vertical

  b   Set:

  X1= Center of "widest opening voltage"

  X2= Center of "widest opening voltage"

  Y1= widest opening voltage

  Y2= Bottom Level of display

  c   EyeHeightV1= Histogram Max

  d   Set:

  X1= Center of "widest opening voltage"

  X2= Center of "widest opening voltage"

  Y1= Top Level of display

  Y2= widest opening voltage

  e   EyeHeightV2= Histogram Min

  f   Calculate EyeHeight = EyeHeightV2 - EyeHeightV1

21 Return total failed UnitInterval as a test result.

Expected/
Observable Results: The measured value of Write Eye Diagram for the test signal is considered for 'Information-Only' purpose.

tDSS

NOTE   This test appears only when CK (Diff) is included in the Signal Source along with DQS (Diff) and DQ.

Test ID: 14000

Test Overview: The purpose of this test is to verify the time interval from the falling edge of the data strobe (DQS falling edge) output access time to the clock (CLK rising edge) setup time.

Test Procedure:
1   Acquire and split read and write burst of the acquired signal.
2   Take the first valid WRITE burst found.
3   Find all valid crossings on the falling edges of DQS in the specified burst.
4   For all crossings found on the falling edges of DQS, locate all the next nearest rising edges of the Clock.
5   Measure tDSS as the time between crossings on the falling edges of DQS and the rising edges of the Clock found in the previous step.
6   Collect all values of tDSS.
7   Report all values of tDSS measured.

Expected/ Observable Results: The measured value of tDSS shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tDSH

NOTE   This test appears only when CK (Diff) is included in the Signal Source along with DQS (Diff) and DQ.

Test ID: 14010

Test Overview: The purpose of this test is to verify the time interval from the falling edge of the data strobe (DQS falling edge) to clock (CLK rising edge) hold time.

Test Procedure:
1   Acquire and split read and write burst of the acquired signal.
2   Take the first valid WRITE burst found.
3   Find all valid falling DQS crossings in the specified burst.
4   For all the falling DQS crossings found, locate all nearest preceding rising Clock edges.
5   Measure tDSH as the time between falling DQS crossings and the crossing point of the Clock rising edges found.
6   Collect all tDSH.
7   Determine the worst result from the set of tDSH measured.

Expected/ Observable Results: The measured value of tDSH shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tWPRE_2

NOTE   This test appears only when the DDR5_2tCK is selected as the Write Preamble mode in the DQS Burst Options Setup window.

Test ID:	14031
Test Overview:	The purpose of this test is to verify the Write preamble region of the DQS signal (for 2tCK Preamble mode).
Test Procedure:	1 Acquire and split the Read and Write bursts of the acquired signal.
	2 Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
	3 Take the first valid WRITE burst found.
	4 Find tLZBeginPoint on DQS signal of the said burst.
	5 Find the first rising edge (excluding preamble pattern) on DQS of the found burst.
	6 tWPRE_2 is the time interval between the rising DQS edge and tLZBeginPoint.
	7 Report tWPRE_2.
Expected/ Observable Results:	The measured value of tWPRE_2 for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tWPRE_3

NOTE   This test appears only when the DDR5_3tCK is selected as the Write Preamble mode in the DQS Burst Options Setup window.

Test ID:	14032
Test Overview:	The purpose of this test is to verify the Write preamble region of the DQS signal (for 3tCK Preamble mode).
Test Procedure:	1 Acquire and split the Read and Write bursts of the acquired signal.
	2 Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
	3 Take the first valid WRITE burst found.
	4 Find tLZBeginPoint on DQS signal of the said burst.
	5 Find the first rising edge (excluding preamble pattern) on DQS of the found burst.
	6 tWPRE_3 is the time interval between the rising DQS edge and tLZBeginPoint.
	7 Report tWPRE_3.
Expected/ Observable Results:	The measured value of tWPRE_3 for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tWPRE_4

NOTE   This test appears only when the DDR5_4tCK is selected as the Write Preamble mode in the DQS Burst Options Setup window.

Test ID: 14033

Test Overview: The purpose of this test is to verify the Write preamble region of the DQS signal (for 4tCK Preamble mode).

Test Procedure:
1   Acquire and split the Read and Write bursts of the acquired signal.
2   Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3   Take the first valid WRITE burst found.
4   Find tLZBeginPoint on DQS signal of the said burst.
5   Find the first rising edge (excluding preamble pattern) on DQS of the found burst.
6   tWPRE_4 is the time interval between the rising DQS edge and tLZBeginPoint.
7   Report tWPRE_4.

Expected/ Observable Results: The measured value of tWPRE_4 for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tWPST_0_5

NOTE   This test appears only when the DDR5_0.5tCK is selected as the Write Postamble Mode in the DQS Burst Options Setup window.

Test ID: 14041

Test Overview: The purpose of this test is to verify the Write postamble region of the DQS signal (for 0.5tCK Postamble mode).

Test Procedure:
1   Acquire and split the Read and Write burst of the acquired signal.
2   Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3   Take the first valid WRITE burst found.
4   Find tHZEndPoint of the said burst.
5   Find the last falling edge on DQS prior to the tHZEndPoint that was found in the previous step.
6   tWPST_0_5 is the time interval between the falling DQS edge's crossing and tHZEndPoint.
7   Report tWPST_0_5.

Expected/ Observable Results: The measured value of tWPST_0_5 for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tWPST_1_5

NOTE   This test appears only when the DDR5_1.5tCK is selected as the Write Postamble Mode in the DQS Burst Options Setup window.

Test ID: 14042

Test Overview: The purpose of this test is to verify the Write postamble region of the DQS signal (for 1.5tCK Postamble mode).

Test Procedure:
1   Acquire and split the Read and Write burst of the acquired signal.
2   Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3   Take the first valid WRITE burst found.
4   Find tHZEndPoint of the said burst.
5   Find the last falling edge on DQS prior to the tHZEndPoint that was found in the previous step.
6   tWPST_1_5 is the time interval between the falling DQS edge's crossing and tHZEndPoint.
7   Report tWPST_1_5.

Expected/ Observable Results: The measured value of tWPST_1_5 for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tDQSH_pre

Test ID: 14060

Test Overview: The purpose of this test is to verify the positive pulse width of DQS within preamble region.

Test Procedure:
1   Acquire and split the Read and Write burst of the acquired signal.
2   Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3   Take the first valid WRITE burst found.
4   Find tLZBeginPoint on DQS signal of the said burst.
5   Find tLZEndPoint. It is defined as first rising edge (excluding preamble pattern) on DQS of the found burst where first data bit is latching.
6   Find all valid rising and falling DQS crossings within "tLZBeginPoint + 0.5UI" and "tLZEndPoint + 0.5UI".
7   Measure tDQSH_pre as the time starting from the rising edge of DQS and ending at the following falling edge.
8   Collect all tDQSH_pre values.
9   Determine the worst result from the set of tDQSH_pre measured.

Expected/ Observable Results: The measured value of tDQSH_pre for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tDQSL_pre

Test ID: 14070

Test Overview: The purpose of this test is to verify the negative pulse width of DQS within preamble region.

Test Procedure:
1. Acquire and split the Read and Write burst of the acquired signal.
2. Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3. Take the first valid WRITE burst found.
4. Find tLZBeginPoint on DQS signal of the said burst.
5. Find tLZEndPoint. It is defined as first rising edge (excluding preamble pattern) on DQS of the found burst where first data bit is latching.
6. Find all valid rising and falling DQS crossings within "tLZBeginPoint + 0.5UI" and "tLZEndPoint + 0.5UI".
7. Measure tDQSL_pre as the time starting from the falling edge of DQS and ending at the following rising edge.
8. Collect all tDQSL_pre values.
9. Determine the worst result from the set of tDQSL_pre measured.

Expected/ Observable Results: The measured value of tDQSL_pre for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tDQSL2PRE

Test ID: 14081

Test Overview: The purpose of this test is to verify the initial low pulse width during Write Preamble region of the DQS signal (for 2tCK Preamble mode).

Test Procedure:
1. Acquire and split the Read and Write burst of the acquired signal.
2. Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3. Take the first valid WRITE burst found.
4. Find tLZBeginPoint on DQS signal of the said burst.
5. Find the first rising edge on DQS after the tLZEndPoint.
6. tDQSL2PRE is the time interval between the tLZBeginPoint and rising edge found in step 5.
7. Report tDQSL2PRE values.

Expected/ Observable Results: The measured value of tDQSL2PRE for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tDQSL3PRE

NOTE   This test appears only when the DDR5_3tCK is selected as the Write Preamble Mode in the DQS Burst Options Setup window.

Test ID: 14082

Test Overview: The purpose of this test is to verify the initial low pulse width during Write Preamble region of the DQS signal (for 3tCK Preamble mode).

Test Procedure:
1   Acquire and split the Read and Write burst of the acquired signal.
2   Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3   Take the first valid WRITE burst found.
4   Find tLZBeginPoint of the said burst.
5   Find the first rising edge on DQS after the tLZEndPoint.
6   tDQSL3PRE is the time interval between the tLZBeginPoint and rising edge found in step 5.
7   Report tDQSL3PRE values.

Expected/ Observable Results: The measured value of tDQSL3PRE for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tDQSL4PRE

NOTE   This test appears only when the DDR5_4tCK is selected as the Write Preamble Mode in the DQS Burst Options Setup window.

Test ID: 14083

Test Overview: The purpose of this test is to verify the initial low pulse width during Write Preamble region of the DQS signal (for 4tCK Preamble mode).

Test Procedure:
1   Acquire and split the Read and Write burst of the acquired signal.
2   Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3   Take the first valid WRITE burst found.
4   Find tLZBeginPoint of the said burst.
5   Find the first rising edge on DQS after the tLZEndPoint.
6   tDQSL4PRE is the time interval between the tLZBeginPoint and rising edge found in step 5.
7   Report tDQSL4PRE values.

Expected/ Observable Results: The measured value of tDQSL4PRE for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

SRIdiffR_DQS

Test ID: 13000

Test Overview: The purpose of this test is to verify the differential input slew rate for rising edge of the test signal.

Test Procedure:
1   Acquire and split the read and write burst of the acquired signal.
2   Take the first valid WRITE burst found.
3   Calculate $V_{ILdiff(AC)}$ and $V_{IHdiff(AC)}$ using the equation:

$V_{IHdiff(AC)}$ = 0.75 * Vdiffpk-pk
$V_{ILdiff(AC)}$ = 0.25 * Vdiffpk-pk
Then use calculated $V_{IHdiff(AC)}$ and $V_{ILdiff(AC)}$ to defined strobe edge level requirement.

4   Find all the valid Strobe rising edges in the specified burst.
A valid Strobe rising edge starts at $V_{ILdiff.DQS(AC)}$ crossing and ends at the following $V_{IHdiff.DQS(AC)}$ crossing.

5   For all the valid Strobe rising edges, find the transition time, T_R.
T_R is the time starting at $V_{ILdiff.DQS(AC)}$ crossing and ending at the following $V_{IHdiff.DQS(AC)}$ crossing.

6   Calculate SRIdiffR_DQS using the equation:

$$SRIdiffR\_DQS = [V_{IHdiff.DQS(AC)} - V_{ILdiff.DQS(AC)}] / T_R$$

7   Determine the worst result from the set of SRIdiffR_DQS measured.

Expected/ Observable Results: The measured value of SRIdiffR_DQS for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

SRIdiffF_DQS

Test ID: 13005

Test Overview: The purpose of this test is to verify the differential input slew rate for falling edge of the test signal.

Test Procedure:
1   Acquire and split the read and write burst of the acquired signal.
2   Take the first valid WRITE burst found.
3   Calculate $V_{ILdiff(AC)}$ and $V_{IHdiff(AC)}$ using the equation:

$V_{IHdiff(AC)}$ = 0.75 * Vdiffpk-pk
$V_{ILdiff(AC)}$ = 0.25 * Vdiffpk-pk
Then use calculated $V_{IHdiff(AC)}$ and $V_{ILdiff(AC)}$ to defined strobe edge level requirement.

4   For all the valid Strobe falling edges, find the transition time, T_R.
T_R is the time starting at $V_{IHdiff.DQS(AC)}$ crossing and ending at the following $V_{ILdiff.DQS(AC)}$ crossing.

5   Calculate SRIdiffF_DQS using the equation:

$$SRIdiffF\_DQS = [V_{IHdiff.DQS(AC)} - V_{ILdiff.DQS(AC)}] / T_R$$

6   Determine the worst result from the set of SRIdiffF_DQS measured.

Expected/ Observable Results: The measured value of SRIdiffF_DQS for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

5 Continuous Data tests

KEYSIGHT
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Clock (Diff) tests

Test Availability Conditions

All tests in this test group appear for the following configuration in DDR5 General Setup window:

Signal Source:
- CK (Diff)
- Any set including CK (Diff)

Signal Operation Mode:
- CK (Diff) — Continuous
- DQS (Diff) — Any
- DQ — Any

VIHdiff.CK(AC)

Test ID: 10000

Test Overview: The purpose of this test is to verify the high level differential input voltage value of the test signal.

Test Procedure:
1. Pre-condition the oscilloscope.
2. Trigger on the rising edge of the clock signal under test.
3. Find all valid Clock positive pulses in the triggered waveform.
   A valid Clock positive pulse starts at the 0V crossing at valid Clock rising edge and ends at the 0V crossing at the following valid Clock falling edge.
4. Zoom into the first pulse and measure the top voltage V_{TOP}. Here, V_{TOP} is the voltage value on the rising edge after which the signal loses the monotonicity of the slope.
   Take the V_{TOP} measurement as $V_{IHdiff\ (AC)}$ value.
5. Continue the previous step for all positive pulses found in the specified waveform.
6. Determine the worst result from the set of $V_{IHdiff\ (AC)}$ values measured.

**Expected/
Observable Results:** The worst measured $V_{IHdiff.CK\ (AC)}$ shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

VIHdiff.CK(DC)

Test ID: 10005

Test Overview: The purpose of this test is to verify the high level differential input voltage value of the test signal.

Test Procedure:
1. Pre-condition the oscilloscope.
2. Trigger on the rising edge of the clock signal under test.
3. Find all valid Clock positive pulses in the triggered waveform.
   A valid Clock positive pulse starts at the 0V crossing at valid Clock rising edge and ends at the 0V crossing at the following valid Clock falling edge.
4. Zoom into the first pulse and measure the top voltage V_{TOP}. Here, V_{TOP} is the voltage value on the rising edge after which the signal loses the monotonicity of the slope.
   Take the V_{TOP} measurement as $V_{IHdiff\ (DC)}$ value.
5. Continue the previous step for all positive pulses found in the specified waveform.
6. Determine the worst result from the set of $V_{IHdiff\ (DC)}$ values measured.

Expected/
Observable Results: The worst measured $V_{IHdiff.CK\ (DC)}$ shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

VILdiff.CK(AC)

Test ID: 10010

Test Overview: The purpose of this test is to verify the low level differential input voltage value of the test signal.

Test Procedure: 1   Pre-condition the oscilloscope.

2   Trigger on the rising edge of the clock signal under test.

3   Find all valid Clock negative pulses in the triggered waveform.
A valid Clock negative pulse starts at the 0V crossing at valid Clock falling edge and ends at the 0V crossing at the following valid Clock rising edge.

4   Zoom into the first pulse and measure the base voltage V_{BASE}. Here, V_{BASE} is the voltage value on the falling edge after which the signal loses the monotonicity of the slope.
Take the V_{BASE} measurement as $V_{ILdiff\ (AC)}$ value.

5   Continue the previous step for all the negative pulses found in the specified waveform.

6   Determine the worst result from the set of $V_{ILdiff\ (AC)}$ values measured.

Expected/
Observable Results: The worst measured $V_{ILdiff.CK\ (AC)}$ shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

VILdiff.CK(DC)

Test ID: 10015

Test Overview: The purpose of this test is to verify the low level differential input voltage value of the test signal.

Test Procedure: 1   Pre-condition the oscilloscope.

2   Trigger on the rising edge of the clock signal under test.

3   Find all valid Clock negative pulses in the triggered waveform.
A valid Clock negative pulse starts at the 0V crossing at valid Clock falling edge and ends at the 0V crossing at the following valid Clock rising edge.

4   Zoom into the first pulse and measure the base voltage V_{BASE}. Here, V_{BASE} is the voltage value on the falling edge after which the signal loses the monotonicity of the slope.
Take the V_{BASE} measurement as $V_{ILdiff\ (DC)}$ value.

5   Continue the previous step for all the negative pulses found in the specified waveform.

6   Determine the worst result from the set of $V_{ILdiff\ (DC)}$ values measured.

Expected/
Observable Results: The worst measured $V_{ILdiff.CK\ (DC)}$ shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

SRIdiffR.CK

Test ID:	10100
Test Overview:	The purpose of this test is to verify that the differential input slew rate for rising edge of the test signal.

Test Procedure:

1 Trigger on the rising edge of the clock signal under test.

2 Find all the valid Clock rising edges in the entire waveform.

3 A valid clock rising edge starts at VILdiff_CK crossing and ends at the following VIHdiff_CK crossing.

4 For all the valid Clock rising edges, measure the transition time, DeltaTRdiff.
   DeltaTRdiff is the time starting at VILdiff_CK crossing and ending at the following VIHdiff_CK crossing.

5 Calculate SRIdiffR_CK using the equation:

   SRIdiffR_CK = [VIHdiff_CK - VILdiff_CK] / DeltaTRdiff.

6 Determine the worst result from the set of SRIdiffR_CK measured.

Expected/ Observable Results: The worst measured SRIdiffR_CK shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

SRIdiffF.CK

Test ID:	10105
Test Overview:	The purpose of this test is to verify that the differential input slew rate for falling edge of the test signal.

Test Procedure:

1 Trigger on the falling edge of the clock signal under test.

2 Find all the valid Clock falling edges in the entire waveform.
   A valid clock falling edge starts at VIHdiff_CK crossing and ends at the following VILdiff_CK crossing.

3 For all the valid Clock falling edges, measure the transition time, DeltaTFdiff.
   DeltaTFdiff is the time starting at VIHdiff_CK crossing and ending at the following VILdiff_CK crossing.

4 Calculate SRIdiffF_CK using the equation:

   SRIdiffF_CK = [VILdiff_CK - VIHdiff_CK] / DeltaTFdiff.

5 Determine the worst result from the set of SRIdiffF_CK measured.

Expected/ Observable Results: The worst measured SRIdiffF_CK shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

Clock Jitter tests

Test Availability Conditions

All tests in this test group appear for the following configuration in DDR5 General Setup window:

Signal Source:
- CK_t (Single Ended), CK_c (Single Ended)
- CK (Diff)
- Any signal set including CK (Diff)

Signal Operation Mode:
- CK (Diff) — Continuous
- DQS (Diff) — Not applicable
- DQ — Not applicable

tCK

Test ID:	15000
Test Overview:	The purpose of this test is to measure the DRAM Reference clock frequency.
Test Procedure:	1 Measure the average period cycle width for the entire test signal. A period cycle is the time difference from the rising edge of a cycle to the next rising edge.
	2 Calculate the average frequency of the test signal value using the following equation. average freq = 1 / average period
	3 Use the calculated average frequency value as the final measurement result.
Expected/ Observable Results:	The calculated average frequency value shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tCK_Duty_UI_High

Test ID:	15010
Test Overview:	The purpose of this test is to measure the duty cycle of all high pulse widths.
Test Procedure:	

> **NOTE** This test is expected to use continuous 101010... pattern for the test signal.

1 Perform signal conditioning on the test signal.
2 Measure the width of all the high pulses of the test signal. A high pulse width is the time difference from the rising edge of a pulse to the next falling edge.
3 Find the average high pulse width value for all the pulses found.
4 Measure the width of all the low pulses of the test signal. A low pulse width is the time difference from the falling edge of a pulse to the next rising edge.
5 Find the average low pulse width value for all the pulses found.
6 The average UI is calculated as the average of all the high pulse widths and low pulse widths measured.

7   The average duty high pulse width is calculated as follows.
average duty high pulse width = average high pulse width / average UI

Expected/
Observable Results: The calculated average duty high pulse width shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tCK_Duty_UI_Low

Test ID: 15015

Test Overview: The purpose of this test is to measure the duty cycle of all low pulse widths.

Test Procedure:

> **NOTE**   This test is expected to use continuous 101010... pattern for the test signal.

1   Perform signal conditioning on the test signal.
2   Measure the width of all the high pulses of the test signal. A high pulse width is the time difference from the rising edge of a pulse to the next falling edge.
3   Find the average high pulse width value for all the pulses found.
4   Measure the width of all the low pulses of the test signal. A low pulse width is the time difference from the falling edge of a pulse to the next rising edge.
5   Find the average low pulse width value for all the pulses found.
6   The average UI is calculated as the average of all the high pulse widths and low pulse widths measured.
7   The average duty low pulse width is calculated as follows.
average duty low pulse width = average low pulse width / average UI

Expected/
Observable Results: The calculated average duty low pulse width value shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

tCK_Duty_UI_Error

Test ID: 15020

Test Overview: The purpose of this test is to measure the duty cycle error.

Test Procedure:

> **NOTE**   This test is expected to use continuous 101010... pattern for the test signal.

1   Perform signal conditioning on the test signal.
2   Measure the width of all the high pulses of the test signal. A high pulse width is the time difference from the rising edge of a pulse to the next falling edge.
3   Find the average high pulse width value for all the pulses found.
4   Measure the width of all the low pulses of the test signal. A low pulse width is the time difference from the falling edge of a pulse to the next rising edge.
5   Find the average low pulse width value for all the pulses found.
6   The average UI is calculated as the average of all the high pulse widths and low pulse widths measured.

7   The average duty high pulse width is calculated as follows.
average duty high pulse width = average high pulse width / average UI

8   The average duty low pulse width is calculated as follows.
average duty low pulse width = average low pulse width / average UI

9   The duty error for the average high pulse and average low pulse is calculated as follows.
duty high error = abs(average UI – average duty high pulse width)
duty low error = abs(average UI – average duty low pulse width)

10   The worst duty error is derived from the largest value between duty high error and duty low error.
worst duty error = max(duty high error, duty low error)

11   Report the worst duty error as the final measurement result.

Expected/ Observable Results: The calculated worst duty error value shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

(nUI) tCK_nUI_Rj_NoBUJ

Test ID: (1UI) tCK_1UI_Rj_NoBUJ (Test ID: 15301)

(2UI) tCK_2UI_Rj_NoBUJ (Test ID: 15302)

(3UI) tCK_3UI_Rj_NoBUJ (Test ID: 15303)

(4UI) tCK_4UI_Rj_NoBUJ (Test ID: 15304)

(5UI) tCK_5UI_Rj_NoBUJ (Test ID: 15305)

(6UI) tCK_6UI_Rj_NoBUJ (Test ID: 15306)

(7UI) tCK_7UI_Rj_NoBUJ (Test ID: 15307)

(8UI) tCK_8UI_Rj_NoBUJ (Test ID: 15308)

(9UI) tCK_9UI_Rj_NoBUJ (Test ID: 15309)

(10UI) tCK_10UI_Rj_NoBUJ (Test ID: 15310)

(11UI) tCK_11UI_Rj_NoBUJ (Test ID: 15311)

(12UI) tCK_12UI_Rj_NoBUJ (Test ID: 15312)

(13UI) tCK_13UI_Rj_NoBUJ (Test ID: 15313)

(14UI) tCK_14UI_Rj_NoBUJ (Test ID: 15314)

(15UI) tCK_15UI_Rj_NoBUJ (Test ID: 15315)

(16UI) tCK_16UI_Rj_NoBUJ (Test ID: 15316)

(17UI) tCK_17UI_Rj_NoBUJ (Test ID: 15317)

(18UI) tCK_18UI_Rj_NoBUJ (Test ID: 15318)

(19UI) tCK_19UI_Rj_NoBUJ (Test ID: 15319)

(20UI) tCK_20UI_Rj_NoBUJ (Test ID: 15320)

(21UI) tCK_21UI_Rj_NoBUJ (Test ID: 15321)

(22UI) tCK_22UI_Rj_NoBUJ (Test ID: 15322)

(23UI) tCK_23UI_Rj_NoBUJ (Test ID: 15323)

(24UI) tCK_24UI_Rj_NoBUJ (Test ID: 15324)

(25UI) tCK_25UI_Rj_NoBUJ (Test ID: 15325)

(26UI) tCK_26UI_Rj_NoBUJ (Test ID: 15326)

(27UI) tCK_27UI_Rj_NoBUJ (Test ID: 15327)

(28UI) tCK_28UI_Rj_NoBUJ (Test ID: 15328)

(29UI) tCK_29UI_Rj_NoBUJ (Test ID: 15329)

(30UI) tCK_30UI_Rj_NoBUJ (Test ID: 15330)

Test Overview: The purpose of these tests is to measure the Rj RMS value of nUI Jitter without BUJ.

Test Procedure:

> **NOTE** This test is expected to use continuous 101010... pattern for the test signal.

1   Perform signal conditioning on the test signal.
2   Set up the Recovery Clock method to use "Constant Frequency" method.
3   The reference measurement threshold used must be 0V.
4   Perform UI width checking on the test signal. (This feature can be enabled or disabled by configuring the "JitterTests_UIWidthCheck" option under the Configure tab of the application.)
5   Configure the EZJIT feature settings in the Infiniium application to perform "N-Unit Interval" measurement with the specified number of UI.
6   Perform the removal of scope random jitter. (This feature can be enabled or disabled by configuring the "JItterTests_RemoveScopeRJ_Mode" option under the Configure tab of the application.)
7   Sample the required number of data waveforms to meet the total number of UI needed in a test run. (The number of UI needed in a test run is configurable using the "JitterTest_NumOfUI_PerTest" option under the Configure tab of the application.)
8   For RJ measurement, use the extrapolated RJrms measurement results from EZJIT.

Expected/ Observable Results: The calculated Rj RMS value of nUI Jitter without BUJ shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

(nUI) tCK_nUI_Dj_NoBUJ

Test ID: (1UI) tCK_1UI_Dj_NoBUJ (Test ID: 15401)

(2UI) tCK_2UI_Dj_NoBUJ (Test ID: 15402)

(3UI) tCK_3UI_Dj_NoBUJ (Test ID: 15403)

(4UI) tCK_4UI_Dj_NoBUJ (Test ID: 15404)

(5UI) tCK_5UI_Dj_NoBUJ (Test ID: 15405)

(6UI) tCK_6UI_Dj_NoBUJ (Test ID: 15406)

(7UI) tCK_7UI_Dj_NoBUJ (Test ID: 15407)

(8UI) tCK_8UI_Dj_NoBUJ (Test ID: 15408)

(9UI) tCK_9UI_Dj_NoBUJ (Test ID: 15409)

(10UI) tCK_10UI_Dj_NoBUJ (Test ID: 15410)

(11UI) tCK_11UI_Dj_NoBUJ (Test ID: 15411)

(12UI) tCK_12UI_Dj_NoBUJ (Test ID: 15412)

(13UI) tCK_13UI_Dj_NoBUJ (Test ID: 15413)

(14UI) tCK_14UI_Dj_NoBUJ (Test ID: 15414)

(15UI) tCK_15UI_Dj_NoBUJ (Test ID: 15415)

(16UI) tCK_16UI_Dj_NoBUJ (Test ID: 15416)

(17UI) tCK_17UI_Dj_NoBUJ (Test ID: 15317)

(18UI) tCK_18UI_Dj_NoBUJ (Test ID: 15418)

(19UI) tCK_19UI_Dj_NoBUJ (Test ID: 15419)

(20UI) tCK_20UI_Dj_NoBUJ (Test ID: 15420)

(21UI) tCK_21UI_Dj_NoBUJ (Test ID: 15421)

(22UI) tCK_22UI_Dj_NoBUJ (Test ID: 15422)

(23UI) tCK_23UI_Dj_NoBUJ (Test ID: 15423)

(24UI) tCK_24UI_Dj_NoBUJ (Test ID: 15424)

(25UI) tCK_25UI_Dj_NoBUJ (Test ID: 15425)

(26UI) tCK_26UI_Dj_NoBUJ (Test ID: 15426)

(27UI) tCK_27UI_Dj_NoBUJ (Test ID: 15427)

(28UI) tCK_28UI_Dj_NoBUJ (Test ID: 15428)

(29UI) tCK_29UI_Dj_NoBUJ (Test ID: 15429)

(30UI) tCK_30UI_Dj_NoBUJ (Test ID: 15430)

Test Overview: The purpose of these tests is to measure the Dj pp value of nUI Jitter without BUJ.

Test Procedure:

> **NOTE** This test is expected to use continuous 101010... pattern for the test signal.

1 Perform signal conditioning on the test signal.

2 Set up the Recovery Clock method to use "Constant Frequency" method.

3 The reference measurement threshold used must be 0V.

4 Perform UI width checking on the test signal. (This feature can be enabled or disabled by configuring the "JitterTests_UIWidthCheck" option under the Configure tab of the application.)

5 Configure the EZJIT feature settings in the Infiniium application to perform "N-Unit Interval" measurement with the specified number of UI.

6 Perform the removal of scope random jitter. (This feature can be enabled or disabled by configuring the "JItterTests_RemoveScopeRJ_Mode" option under the Configure tab of the application.)

7 Sample the required number of data waveforms to meet the total number of UI needed in a test run. (The number of UI needed in a test run is configurable using the "JitterTest_NumOfUI_PerTest" option under the Configure tab of the application.)

8 For Dj measurement, use the extrapolated DJdd measurement results from EZJIT.

Expected/ Observable Results: The calculated Dj pp value of nUI Jitter without BUJ shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

(nUI) tCK_nUI_Tj_NoBUJ

Test ID: (1UI) tCK_1UI_Tj_NoBUJ (Test ID: 15501)

(2UI) tCK_2UI_Tj_NoBUJ (Test ID: 15502)

(3UI) tCK_3UI_Tj_NoBUJ (Test ID: 15503)

(4UI) tCK_4UI_Tj_NoBUJ (Test ID: 15504)

(5UI) tCK_5UI_Tj_NoBUJ (Test ID: 15505)

(6UI) tCK_6UI_Tj_NoBUJ (Test ID: 15506)

(7UI) tCK_7UI_Tj_NoBUJ (Test ID: 15507)

(8UI) tCK_8UI_Tj_NoBUJ (Test ID: 15508)

(9UI) tCK_9UI_Tj_NoBUJ (Test ID: 15509)

(10UI) tCK_10UI_Tj_NoBUJ (Test ID: 15510)

(11UI) tCK_11UI_Tj_NoBUJ (Test ID: 15511)

(12UI) tCK_12UI_Tj_NoBUJ (Test ID: 15512)

(13UI) tCK_13UI_Tj_NoBUJ (Test ID: 15513)

(14UI) tCK_14UI_Tj_NoBUJ (Test ID: 15514)

(15UI) tCK_15UI_Tj_NoBUJ (Test ID: 15515)

(16UI) tCK_16UI_Tj_NoBUJ (Test ID: 15516)

(17UI) tCK_17UI_Tj_NoBUJ (Test ID: 15517)

(18UI) tCK_18UI_Tj_NoBUJ (Test ID: 15518)

(19UI) tCK_19UI_Tj_NoBUJ (Test ID: 15519)

(20UI) tCK_20UI_Tj_NoBUJ (Test ID: 15520)

(21UI) tCK_21UI_Tj_NoBUJ (Test ID: 15521)

(22UI) tCK_22UI_Tj_NoBUJ (Test ID: 15522)

(23UI) tCK_23UI_Tj_NoBUJ (Test ID: 15523)

(24UI) tCK_24UI_Tj_NoBUJ (Test ID: 15524)

(25UI) tCK_25UI_Tj_NoBUJ (Test ID: 15525)

(26UI) tCK_26UI_Tj_NoBUJ (Test ID: 15526)

(27UI) tCK_27UI_Tj_NoBUJ (Test ID: 15527)

(28UI) tCK_28UI_Tj_NoBUJ (Test ID: 15528)

(29UI) tCK_29UI_Tj_NoBUJ (Test ID: 15529)

(30UI) tCK_30UI_Tj_NoBUJ (Test ID: 15530)

Test Overview: The purpose of these tests is to measure the Tj value of nUI Jitter without BUJ.

Test Procedure:

NOTE   This test is expected to use continuous 101010... pattern for the test signal.

1   Perform signal conditioning on the test signal.

2   Set up the Recovery Clock method to use "Constant Frequency" method.

3   The reference measurement threshold used must be 0V.

4   Perform UI width checking on the test signal. (This feature can be enabled or disabled by configuring the "JitterTests_UIWidthCheck" option under the Configure tab of the application.)

5   Configure the EZJIT feature settings in the Infiniium application to perform "N-Unit Interval" measurement with the specified number of UI.

6   Perform the removal of scope random jitter. (This feature can be enabled or disabled by configuring the "JItterTests_RemoveScopeRJ_Mode" option under the Configure tab of the application.)

7   Sample the required number of data waveforms to meet the total number of UI needed in a test run. (The number of UI needed in a test run is configurable using the "JitterTest_NumOfUI_PerTest" option under the Configure tab of the application.)

8   For Tj measurement, use the extrapolated TJ(p-p) measurement results from EZJIT.

Expected/ Observable Results: The calculated Tj value of nUI Jitter without BUJ shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

DQ Jitter tests

Test Availability Conditions

All tests in this test group appear for the following configuration in DDR5 General Setup window:

Signal Source:
- DQS_t (Single Ended), DQS_c (Single Ended), DQ
- Any other signal set including DQ

Signal Operation Mode:
- CK (Diff) — Not applicable
- DQS (Diff) — Continuous
- DQ — Continuous1010

tTx_DQ_Duty_UI

Test ID: 17000

Test Overview: The purpose of this test is to measure the DQ Duty Cycle Error.

Test Procedure:

> **NOTE**   This test is expected to use continuous 101010... pattern for the test signal.

1   Perform signal conditioning on the test signal.
2   Measure the width of all the high pulses of the test signal. A high pulse width is the time difference from the rising edge of a pulse to the next falling edge.
3   Find the average high pulse width value for all the pulses found.
4   Measure the width of all the low pulses of the test signal. A low pulse width is the time difference from the falling edge of a pulse to the next rising edge.
5   Find the average low pulse width value for all the pulses found.
6   The average UI is calculated as the average of all the high pulse widths and low pulse widths measured.
7   The average duty high pulse width is calculated as follows.
average duty high pulse width = average high pulse width / average UI
8   The average duty low pulse width is calculated as follows.
average duty low pulse width = average low pulse width / average UI
9   The duty error for the average high pulse and average low pulse is calculated as follows.
duty high error = abs(average UI - average duty high pulse width)
duty low error = abs(average UI - average duty low pulse width)
10   The worst duty error is derived from the largest value between duty high error and duty low error.
worst duty error = max(duty high error, duty low error)
11   Report the worst duty error as the final measurement result.

Expected/ Observable Results: The calculated worst duty error value shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

(nUI) tTX_DQ_nUI_Rj_NoBUJ

Test ID: (1UI) tTX_DQ_1UI_Rj_NoBUJ (Test ID: 17301)

(2UI) tTX_DQ_2UI_Rj_NoBUJ (Test ID: 17302)

(3UI) tTX_DQ_3UI_Rj_NoBUJ (Test ID: 17303)

(4UI) tTX_DQ_4UI_Rj_NoBUJ (Test ID: 17304)

Test Overview: The purpose of these tests is to measure the Rj RMS value of nUI Jitter without BUJ.

Test Procedure:

NOTE   This test is expected to use continuous 101010... pattern for the test signal.

1   Perform signal conditioning on the test signal.
2   Set up the Recovery Clock method to use "Constant Frequency" method.
3   The reference measurement threshold used must be the VrefDQ value (a configuration setting in the application).
4   Perform UI width checking on the test signal. (This feature can be enabled or disabled by configuring the "JitterTests_UIWidthCheck" option under the Configure tab of the application.)
5   Configure the EZJIT feature settings in the Infiniium application to perform "N-Unit Interval" measurement with the specified number of UI.
6   Perform the removal of scope random jitter. (This feature can be enabled or disabled by configuring the "JItterTests_RemoveScopeRJ_Mode" option under the Configure tab of the application.)
7   Sample the required number of data waveform to meet the total number of UI needed in a test run. (The number of UI needed in a test run is configurable using the "JitterTest_NumOfUI_PerTest" option under the Configure tab of the application.)
8   For RJ measurement, use the extrapolated RJrms measurement results from EZJIT.

Expected/ Observable Results: The calculated Rj RMS value of nUI Jitter without BUJ shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

(nUI) tTX_DQ_nUI_Dj_NoBUJ

Test ID: (1UI) tTX_DQ_1UI_Dj_NoBUJ (Test ID: 17401)

(2UI) tTX_DQ_2UI_Dj_NoBUJ (Test ID: 17402)

(3UI) tTX_DQ_3UI_Dj_NoBUJ (Test ID: 17403)

(4UI) tTX_DQ_4UI_Dj_NoBUJ (Test ID: 17404)

Test Overview: The purpose of these tests is to measure the Dj pp value of nUI Jitter without BUJ.

Test Procedure:

NOTE   This test is expected to use continuous 101010... pattern for the test signal.

1   Perform signal conditioning on the test signal.
2   Set up the Recovery Clock method to use "Constant Frequency" method.

3   The reference measurement threshold used must be the VrefDQ value (a configuration setting in the application).

4   Perform UI width checking on the test signal. (This feature can be enabled or disabled by configuring the "JitterTests_UIWidthCheck" option under the Configure tab of the application.)

5   Configure the EZJIT feature settings in the Infiniium application to perform "N-Unit Interval" measurement with the specified number of UI.

6   Perform the removal of scope random jitter. (This feature can be enabled or disabled by configuring the "JItterTests_RemoveScopeRJ_Mode" option under the Configure tab of the application.)

7   Sample the required number of data waveform to meet the total number of UI needed in a test run. (The number of UI needed in a test run is configurable using the "JitterTest_NumOfUI_PerTest" option under the Configure tab of the application.)

8   For DJ measurement, use the extrapolated DJdd measurement results from EZJIT.

Expected/ Observable Results: The calculated Dj pp value of nUI Jitter without BUJ shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

DQS Jitter tests

Test Availability Conditions

All tests in this test group appear for the following configuration in DDR5 General Setup window:

Signal Source:
- DQS_t (Single Ended), DQS_c (Single Ended), DQ
- Any set including DQS (Diff)

Signal Operation Mode:
- CK (Diff) — Not applicable
- DQS (Diff) — Continuous
- DQ — Either DataPattern, Continuous1010 or both

tTx_DQS_Duty_UI

Test ID: 16000

Test Overview: The purpose of this test is to measure the DQS Duty Cycle Error.

Test Procedure:

> **NOTE**   This test is expected to use continuous 101010... pattern for the test signal.

1. Perform signal conditioning on the test signal.
2. Measure the width of all the high pulses of the test signal. A high pulse width is the time difference from the rising edge of a pulse to the next falling edge.
3. Find the average high pulse width value for all the pulses found.
4. Measure the width of all the low pulses of the test signal. A low pulse width is the time difference from the falling edge of a pulse to the next rising edge.
5. Find the average low pulse width value for all the pulses found.
6. The average UI is calculated as the average of all the high pulse widths and low pulse widths measured.
7. The average duty high pulse width is calculated as follows.
   average duty high pulse width = average high pulse width / average UI
8. The average duty low pulse width is calculated as follows.
   average duty low pulse width = average low pulse width / average UI
9. The duty error for the average high pulse and average low pulse is calculated as follows.
   duty high error = abs(average UI - average duty high pulse width)
   duty low error = abs(average UI - average duty low pulse width)
10. The worst duty error is derived from the largest value between duty high error and duty low error.
    worst duty error = max(duty high error, duty low error)
11. Report the worst duty error as the final measurement result.

Expected/ Observable Results: The calculated worst duty error value shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

(nUI) tTX_DQS_nUI_Rj_NoBUJ

Test ID: (1UI) tTX_DQS_1UI_Rj_NoBUJ (Test ID: 16301)

(2UI) tTX_DQS_2UI_Rj_NoBUJ (Test ID: 16302)

(3UI) tTX_DQS_3UI_Rj_NoBUJ (Test ID: 16303)

(4UI) tTX_DQS_4UI_Rj_NoBUJ (Test ID: 16304)

Test Overview: The purpose of these tests is to measure the Rj RMS value of nUI Jitter without BUJ.

Test Procedure:

> **NOTE**   This test is expected to use continuous 101010... pattern for the test signal.

1   Perform signal conditioning on the test signal.
2   Set up the Recovery Clock method to use "Constant Frequency" method.
3   The reference measurement threshold used must be 0V.
4   Perform UI width checking on the test signal. (This feature can be enabled or disabled by configuring the "JitterTests_UIWidthCheck" option under the Configure tab of the application.)
5   Configure the EZJIT feature settings in the Infiniium application to perform "N-Unit Interval" measurement with the specified number of UI.
6   Perform the removal of scope random jitter. (This feature can be enabled or disabled by configuring the "JItterTests_RemoveScopeRJ_Mode" option under the Configure tab of the application.)
7   Sample the required number of data waveform to meet the total number of UI needed in a test run. (The number of UI needed in a test run is configurable using the "JitterTest_NumOfUI_PerTest" option under the Configure tab of the application.)
8   For RJ measurement, use the extrapolated RJrms measurement results from EZJIT.

Expected/ Observable Results: The calculated Rj RMS value of nUI Jitter without BUJ shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

(nUI) tTX_DQS_nUI_Dj_NoBUJ

Test ID: (1UI) tTX_DQS_1UI_Dj_NoBUJ (Test ID: 16401)

(2UI) tTX_DQS_2UI_Dj_NoBUJ (Test ID: 16402)

(3UI) tTX_DQS_3UI_Dj_NoBUJ (Test ID: 16403)

(4UI) tTX_DQS_4UI_Dj_NoBUJ (Test ID: 16404)

Test Overview: The purpose of these tests is to measure the Dj pp value of nUI Jitter without BUJ.

Test Procedure:

> **NOTE**   This test is expected to use continuous 101010... pattern for the test signal.

1   Perform signal conditioning on the test signal.
2   Set up the Recovery Clock method to use "Constant Frequency" method.
3   The reference measurement threshold used must be 0V.

4   Perform UI width checking on the test signal. (This feature can be enabled or disabled by configuring the "JitterTests_UIWidthCheck" option under the Configure tab of the application.)

5   Configure the EZJIT feature settings in the Infiniium application to perform "N-Unit Interval" measurement with the specified number of UI.

6   Perform the removal of scope random jitter. (This feature can be enabled or disabled by configuring the "JItterTests_RemoveScopeRJ_Mode" option under the Configure tab of the application.)

7   Sample the required number of data waveform to meet the total number of UI needed in a test run. (The number of UI needed in a test run is configurable using the "JitterTest_NumOfUI_PerTest" option under the Configure tab of the application.)

8   For DJ measurement, use the extrapolated DJdd measurement results from EZJIT.

Expected/
Observable Results: The calculated Dj pp value of nUI Jitter without BUJ shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

6 Clock (Single Ended) tests

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Test Availability Conditions

All tests in this test group appear for the following configuration in DDR5 General Setup window:

Signal Source:
- CK_t (Single Ended), CK_c (Single Ended)

Signal Operation Mode:
- CK (Diff) — Continuous
- DQS (Diff) — Unavailable
- DQ — Unavailable

Overshoot/Undershoot (CK_t)

Overshoot amplitude (CK_t)

Test ID: 11000

Test Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: 1   Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2   Find the "OvershootRegion" across the acquired waveform.
An "OvershootRegion" starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DD} crossing.

3   Within OvershootRegion # 1:

a   Evaluate Overshoot Amplitude by:

i   Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii   Calculating Overshoot Amplitude using the equation:

$$Overshoot\ Amplitude = V_{MAX} - V_{DD}$$

b   Evaluate Area_below_V_{DD} using the equation:

$$Area\_below\_V_{DD} = (OvershootRegion\_End - OvershootRegion\_Start) \times V_{DD}$$

c   Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation

The Trapezoidal Rule

$$Area \approx \frac{1}{2}(y_0 + y_1)\Delta x + \frac{1}{2}(y_1 + y_2)\Delta x + \frac{1}{2}(y_2 + y_3)\Delta x + \dots$$

We can simplify this to give us the **Trapezoidal Rule**, for n trapezoids:

$$Area \approx \Delta x \left(\frac{y_0}{2} + y_1 + y_2 + y_3 + \dots + \frac{y_n}{2} \right)$$

d   Calculate Area_Above_V_{DD} using the equation:

$$Area\_Above\_V_{DD} = Total\_Area\_Above\_0V - Area\_below\_V_{DD}$$

e   Evaluate Area_Above_$V_{DDAbsMax}$ by using Trapezoidal Method Area Calculation.

f   Calculate Area_Between_V_{DD}_and_$V_{DDAbsMax}$ using the equation:

$$Area\_Between\_V_{DD}\_and\_V_{DDAbsMax} = Area\_Above\_V_{DD} - Area\_Above\_V_{DDAbsMax}$$

g   To find the worst case, save the following calculated results for later use:

·   Overshoot Amplitude

·   Area_Above_$V_{DDAbsMax}$

·   Area_Between_V_{DD}_and_$V_{DDAbsMax}$

4   Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.

5   Find the worst result from the stored results listed above.

6   Compare the test result with the compliance test limit.

Expected/
Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.
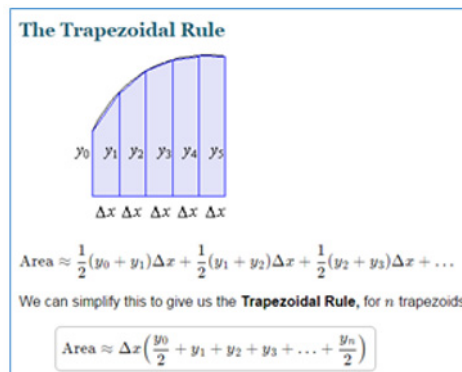
Overshoot area above VDD Abs Max(CK_t)

Test ID: 11010

Test Overview: The purpose of this test is to verify the overshoot area value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: 1   Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2   Find the "OvershootRegion" across the acquired waveform.
An "OvershootRegion" starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DD} crossing.

3   Within OvershootRegion # 1:

    a   Evaluate Overshoot Amplitude by:

        i   Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

        ii   Calculating Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD}$$

    b   Evaluate Area_below_V_{DD} using the equation:

$$\text{Area\_below\_}V_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD}$$

    c   Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation.

The Trapezoidal Rule

$$\text{Area} \approx \frac{1}{2}(y_0 + y_1)\Delta x + \frac{1}{2}(y_1 + y_2)\Delta x + \frac{1}{2}(y_2 + y_3)\Delta x + \dots$$

We can simplify this to give us the **Trapezoidal Rule**, for n trapezoids:

$$\text{Area} \approx \Delta x \left(\frac{y_0}{2} + y_1 + y_2 + y_3 + \dots + \frac{y_n}{2} \right)$$

    d   Calculate Area_Above_V_{DD} using the equation:

$$\text{Area\_Above\_}V_{DD} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD}$$

    e   Evaluate Area_Above_$V_{DDAbsMax}$ by using Trapezoidal Method Area Calculation.

    f   Calculate Area_Between_V_{DD}_and_$V_{DDAbsMax}$ using the equation:

$$\text{Area\_Between\_V}_{DD}\text{\_and\_V}_{DDAbsMax} = \text{Area\_Above\_V}_{DD} - \text{Area\_Above\_V}_{DDAbsMax}$$

    g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V$_{DDAbsMax}$
- Area_Between_V$_{DD}$_and_V$_{DDAbsMax}$

4   Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.

5   Find the worst result from the stored results listed above.

6   Compare the test result with the validation test limit.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

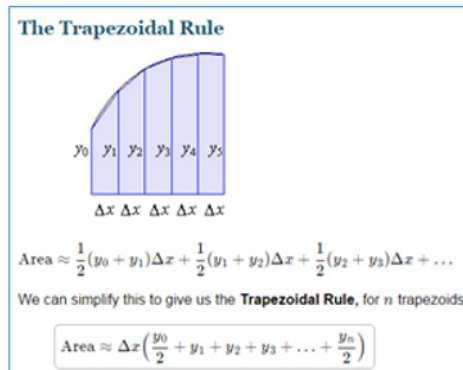Overshoot area between VDD and VDD Abs Max(CK_t)

Test ID: 11020

Test Overview: The purpose of this test is to verify the overshoot area of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: 1   Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2   Find the "OvershootRegion" across the acquired waveform.
An "OvershootRegion" starts at the rising edge of V$_{DD}$ crossing and ends at the falling edge of V$_{DD}$ crossing.

3   Within OvershootRegion # 1:

    a Evaluate Overshoot Amplitude by:

        i   Using T$_{MAX}$, V$_{MAX}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.

        ii   Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = \text{V}_{MAX} - \text{V}_{DD}$$

    b Evaluate Area_below_V$_{DD}$ using the equation:

$$\text{Area\_below\_V}_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times \text{V}_{DD}$$

c   Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation

d   Calculate Area_Above_V_{DD} using the equation:

$$\text{Area\_Above\_V}_{DD} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_V}_{DD}$$

e   Evaluate Area_Above_$V_{DDAbsMax}$ by using Trapezoidal Method Area Calculation.

f   Calculate Area_Between_V_{DD}_and_$V_{DDAbsMax}$ using the equation:

$$\text{Area\_Between\_V}_{DD}\text{\_and\_V}_{DDAbsMax} = \text{Area\_Above\_V}_{DD} - \text{Area\_Above\_V}_{DDAbsMax}$$

g   To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDAbsMax}$
- Area_Between_V_{DD}_and_$V_{DDAbsMax}$

4   Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.

5   Find the worst result from the stored results listed above.

6   Compare the test result with the validation test limit.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

Undershoot amplitude (CK_t)

Test ID: 11005

Test Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.
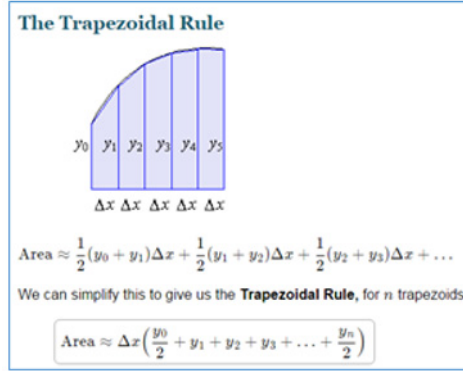
In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: 1   Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2   Find the "UndershootRegion" across the acquired waveform.
An "UndershootRegion" starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

3   Within UndershootRegion # 1:

  a   Evaluate Undershoot Amplitude by:

   i   Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

   ii   Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

  c   Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation

The Trapezoidal Rule

$$\text{Area} \approx \tfrac{1}{2}(y_0 + y_1)\Delta x + \tfrac{1}{2}(y_1 + y_2)\Delta x + \tfrac{1}{2}(y_2 + y_3)\Delta x + \dots$$

We can simplify this to give us the **Trapezoidal Rule**, for *n* trapezoids:

$$\text{Area} \approx \Delta x \left(\frac{y_0}{2} + y_1 + y_2 + y_3 + \dots + \frac{y_n}{2} \right)$$

  d   To find the worst case, save the following calculated results for later use:

   · Undershoot Amplitude

   · Total_Area_Below_0V

4   Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.

5   Find the worst result from the stored results listed above.

6   Compare the test result with the validation test limit.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

Undershoot area below VSS(CK_t)

Test ID: 11015

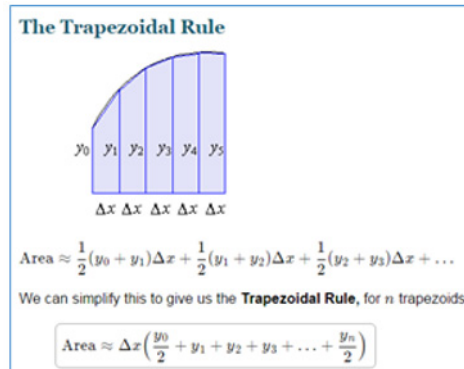**Test Overview:**   The purpose of this test is to verify the undershoot area value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: 1   Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2   Find the "UndershootRegion" across the acquired waveform.
An "UndershootRegion" starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

3   Within UndershootRegion # 1:

  a   Evaluate Undershoot Amplitude by:

   i   Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

   ii   Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

    c Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation

    d To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Total_Area_Below_0V

4   Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.

5   Find the worst result from the stored results listed above.

6   Compare the test result with the validation test limit.

Expected/
Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

Overshoot/Undershoot (CK_c)

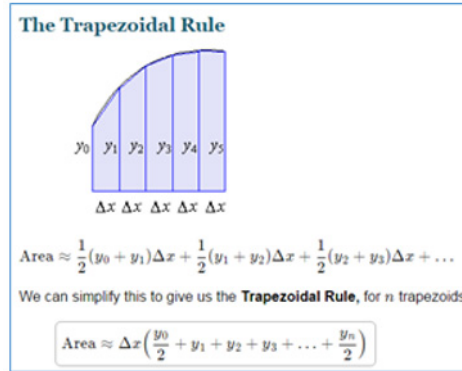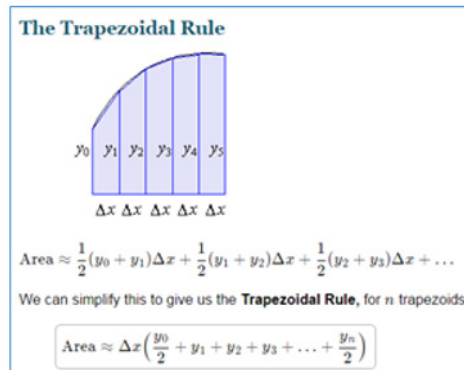## Overshoot amplitude (CK_c)

Test ID: 11050

Test Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: 1   Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2   Find the "OvershootRegion" across the acquired waveform.
An "OvershootRegion" starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DD} crossing.

3   Within OvershootRegion # 1:

    a   Evaluate Overshoot Amplitude by:

        i   Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

        ii   Calculating Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD}$$

    b   Evaluate Area_below_V_{DD} using the equation:

$$\text{Area\_below\_}V_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD}$$

    c   Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation

The Trapezoidal Rule

$$\text{Area} \approx \frac{1}{2}(y_0 + y_1)\Delta x + \frac{1}{2}(y_1 + y_2)\Delta x + \frac{1}{2}(y_2 + y_3)\Delta x + \ldots$$

We can simplify this to give us the **Trapezoidal Rule**, for *n* trapezoids:

$$\text{Area} \approx \Delta x \left(\frac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + \frac{y_n}{2} \right)$$

    d   Calculate Area_Above_V_{DD} using the equation:

$$\text{Area\_Above\_}V_{DD} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD}$$

    e   Evaluate Area_Above_$V_{DDAbsMax}$ by using Trapezoidal Method Area Calculation.

    f   Calculate Area_Between_V_{DD}_and_$V_{DDAbsMax}$ using the equation:

$$\text{Area\_Between\_}V_{DD}\text{\_and\_}V_{DDAbsMax} = \text{Area\_Above\_}V_{DD} - \text{Area\_Above\_}V_{DDAbsMax}$$

    g   To find the worst case, save the following calculated results for later use:

       ·   Overshoot Amplitude

       ·   Area_Above_$V_{DDAbsMax}$

       ·   Area_Between_V_{DD}_and_$V_{DDAbsMax}$

4   Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.

5   Find the worst result from the stored results listed above.

6   Compare the test result with the validation test limit.

Expected/
Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

Overshoot area above VDD Abs Max(CK_c)
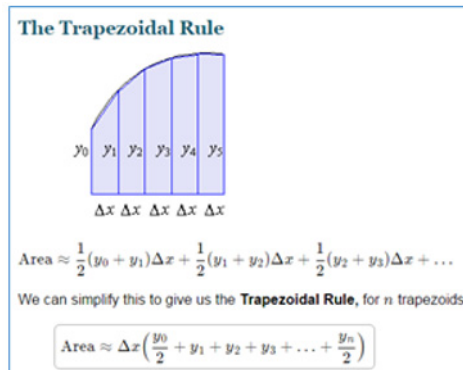
Test ID: 11060

Test Overview: The purpose of this test is to verify the overshoot area value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: 1   Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2   Find the "OvershootRegion" across the acquired waveform.
An "OvershootRegion" starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DD} crossing.

3   Within OvershootRegion # 1:

a   Evaluate Overshoot Amplitude by:

i   Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii   Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD}$$

b   Evaluate Area_below_V_{DD} using the equation:

$$\text{Area\_below\_}V_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD}$$

c   Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation

d   Calculate Area_Above_V_{DD} using the equation:

$$\text{Area\_Above\_}V_{DD} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD}$$

e   Evaluate Area_Above_$V_{DDAbsMax}$ by using Trapezoidal Method Area Calculation.

f   Calculate Area_Between_V_{DD}_and_$V_{DDAbsMax}$ using the equation:

$$\text{Area\_Between\_V}_{DD}\text{\_and\_V}_{DDAbsMax} = \text{Area\_Above\_V}_{DD} - \text{Area\_Above\_V}_{DDAbsMax}$$

g To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude

- Area_Above_V$_{DDAbsMax}$

- Area_Between_V$_{DD}$_and_V$_{DDAbsMax}$

4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the validation test limit.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

Overshoot area between VDD and VDD Abs Max(CK_c)

Test ID: 11070

Test Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the "OvershootRegion" across the acquired waveform.
An "OvershootRegion" starts at the rising edge of V$_{DD}$ crossing and ends at the falling edge of V$_{DD}$ crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

  i Using T$_{MAX}$, V$_{MAX}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.

  ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD}$$

b Evaluate Area_below_V$_{DD}$ using the equation:

$$\text{Area\_below\_V}_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD}$$

c   Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation

d   Calculate Area_Above_V_{DD} using the equation:

$$\text{Area\_Above\_V}_{DD} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_V}_{DD}$$

e   Evaluate Area_Above_$V_{DDAbsMax}$ by using Trapezoidal Method Area Calculation.

f   Calculate Area_Between_V_{DD}_and_$V_{DDAbsMax}$ using the equation:

$$\text{Area\_Between\_V}_{DD}\text{\_and\_V}_{DDAbsMax} = \text{Area\_Above\_V}_{DD} - \text{Area\_Above\_V}_{DDAbsMax}$$

g   To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_$V_{DDAbsMax}$
- Area_Between_V_{DD}_and_$V_{DDAbsMax}$

4   Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.

5   Find the worst result from the stored results listed above.

6   Compare the test result with the validation test limit.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

Undershoot amplitude (CK_c)

Test ID: 110055

Test Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.
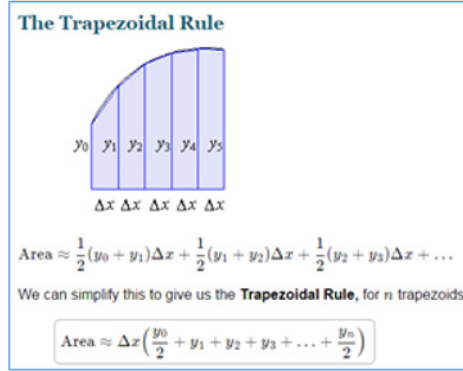
In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure: 1   Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2   Find the "UndershootRegion" across the acquired waveform.
An "UndershootRegion" starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

3 Within UndershootRegion # 1:

 a Evaluate Undershoot Amplitude by:

  i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

  ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

 c Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation

 d To find the worst case, save the following calculated results for later use:

  · Undershoot Amplitude

  · Total_Area_Below_0V

4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the validation test limit.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.
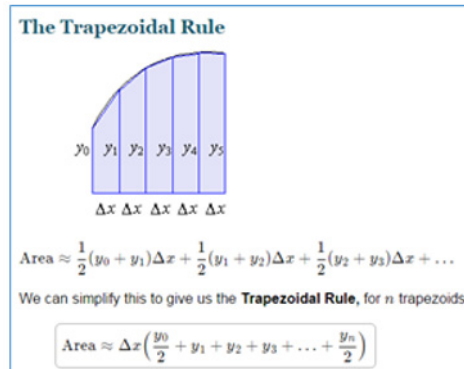
Undershoot area below VSS(CK_c)

Test ID: 11065

Test Procedure: 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the "UndershootRegion" across the acquired waveform.
An "UndershootRegion" starts at the falling edge of 0V crossing and ends at the rising edge of 0V crossing.

3 Within UndershootRegion # 1:

 a Evaluate Undershoot Amplitude by:

  i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

  ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = 0 - V_{MIN}$$

   c   Evaluate Total_Area_Below_0V by using Trapezoidal Method Area Calculation

   d   To find the worst case, save the following calculated results for later use:

- Undershoot Amplitude
- Total_Area_Below_0V

4   Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.

5   Find the worst result from the stored results listed above.

6   Compare the test result with the validation test limit.

**Expected/
Observable Results:**   The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.
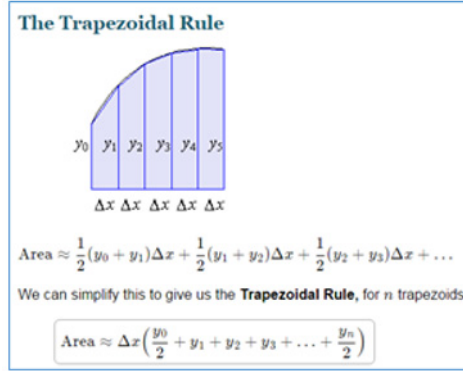
Clock Cross Point Voltage Test

Vix_CK_ratio

Test ID:	11100
Test Overview:	The purpose of this test is to verify the differential input crosspoint voltage ratio, Vix_CK_ratio parameter.

Test Procedure:

1   Sample/Acquire data waveforms.

2   Use Subtract FUNC to generate the differential waveform from the 2-source input, CK_diff.

3   Measure the VRMS of the CK_diff and denote it as VCK_RMS.

4   Find the time-stamp of all differential Clock crossing that crosses 0V.

5   Use VTime to get the actual crossing point voltage value using the timestamp obtained.

6   Find the CK_t and CK_c signal transition swing voltage as VCK_trans. VCK_trans is the difference between the highest and lowest peak voltages of the transitioning CK signals.

7   Find the midpoint of the VCK_trans and denote it as VCKmid.

8   At each crosspoint (rising and falling) found, find the voltage differential between the crosspoint and VCKmid. The rising and falling crosspoint voltage differential is denoted as Vix_CK.

9   Calculate the crosspoint ratio using all the VIX_CK measured.

   Vix_CK_ratio = 100% * VIX_CK / VCK_RMS

10 Determine the worst result from the set of Vix_CK_ratio measured.

Expected/ Observable Results: The calculated value of the differential input crosspoint voltage ratio shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

7 CA (Command Address) tests

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Test Availability Conditions

All tests in this test group appear for the following configuration in DDR5 General Setup window:

Signal Source:
- Any set including CK (Diff) and CA

Signal Operation Mode:
- CK (Diff) — Any
- DQS (Diff) — Any
- DQ — Any

tCIVW Margin

Test ID: 12000

Test Overview: The purpose of this test is to measure the minimum tCIVW Margin of the CA eye diagram.
This test does not measure the tCIVW parameter directly. The measurement result is reported as "Failed" if the eye diagram violates the defined mask.

Test Procedure:

1   Pre-condition the oscilloscope.

2   Check for valid Clock and CA input test signals by verifying its frequency and amplitude values.

3   Trigger on the falling edge of the Clock signal under test.

4   Set up Eye folding and Mask Test settings to use the Clock signal as the clock recovery source.

5   Acquire the number of waveforms specified in the configuration option "Total CA Waveform".

6   Determine and store the Vcent value. Vcent can be derived depending on the "Vcent Evaluation Mode" configuration option in the application.

7   Reposition the Test Mask so that it is centered on the Vcent value.

8   Use the Histogram feature in the Infiniium application to measure the tCIVW Margin value on all the four corners of the Test Mask.
The tCIVW Margin for each Test Mask corner is denoted as tCIVW_m1, tCIVW_m2, tCIVW_m3 and tCIVW_m4.

9   Calculate the margin (in percentage) using the equation:
Margin (%) = [(Time - Half of mask width) / (Half of mask width)] x 100% where,
"Time - Half of mask width" is the gap between the mask corner and the left or right of the eye (as shown in the below reference image).
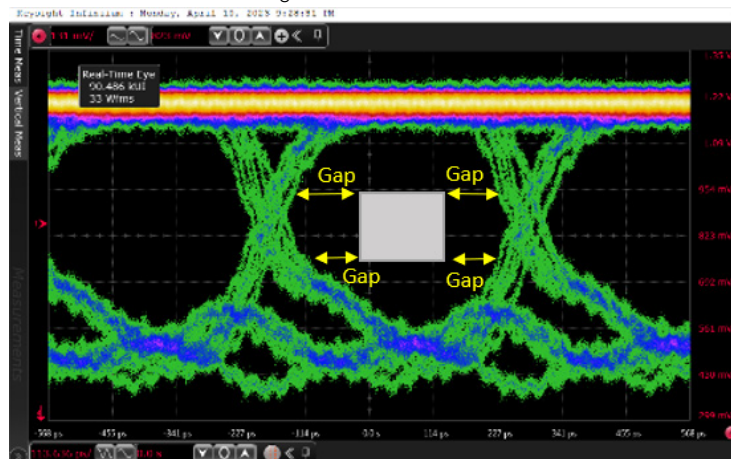
10 Find the minimum value between tCIVW_m1, tCIVW_m2, tCIVW_m3 and tCIVW_m4.

11 Report the minimum value as the worst test result.

**Expected/
Observable Results:** The measured value of tCIVW Margin for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

vCIVW Margin

Test ID: 12005

Test Overview: The purpose of this test is to verify if there is any violation in the CA eye diagram with reference to the defined vCIVW parameter.

Test Procedure: 1 Pre-condition the oscilloscope.

2 Check for valid Clock and CA input test signals by verifying its frequency and amplitude values.

3 Trigger on the falling edge of the Clock signal under test.

4 Set up Eye folding and Mask Test settings to use the Clock signal as the clock recovery source.

5 Acquire the number of waveforms specified in the configuration option 'Total CA Waveform'.

6 Determine and store the Vcent value. Vcent can be derived depending on the "Vcent Evaluation Mode" configuration option in the application.

7 Reposition the Test Mask so that it is centered on the Vcent value.

8 Measure the vCIVW margin value for the top and bottom area of the Test Mask using the Histogram feature in the Infiniium application. The vCIVW margin measured are denoted as vCIVW margin upper and vCIVW margin lower.
Refer to Figure 181 in the JESD79-5 specification.

9 Calculate the margin (in percentage) using the equation:
Margin (%) = [(Voltage - Half of mask height) / (Half of mask height)] x 100% where,
"Voltage - Half of mask height" is the gap between the mask Top/Bottom and the eye at the Top/Bottom (as shown in the below reference image).

10 Find the minimum value between vCIVW margin upper and vCIVW margin lower

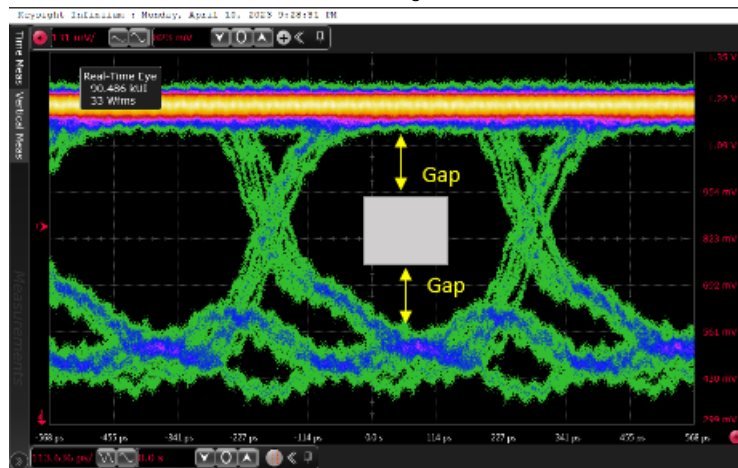11 Report the minimum value as the worst test result.

**Expected/
Observable Results:** The measured value of vCIVW Margin for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

CA VIHL(ac)

Test ID: 12010

Test Overview: The purpose of this test is to verify the VIHL AC parameter, which is defined as the peak to peak voltage centered around Vcent_CA, such that the minimum value of (VIHL_AC / 2) is met both above and below Vcent_CA.
Refer to Figure 181 in the JESD79-5 specification.

Test Procedure: 1   Pre-condition the oscilloscope.

2   Check for valid Clock and CA input test signals by verifying its frequency and amplitude values.

3   Trigger on the falling edge of the Clock signal under test.

4   Set up Eye folding and Mask Test settings to use the Clock signal as the clock recovery source.

5   Acquire the number of waveforms specified in the configuration option 'Total CA Waveform'.

6   Determine and store the Vcent value. Vcent can be derived depending on the "Vcent Evaluation Mode" configuration option in the application.

7   Reposition the Test Mask so that it is centered on the Vcent value.

8   The peak to peak voltage centered around Vcent is measured by scanning the top and bottom of the eye diagram from the point of 0 UI to 1 UI.

9   The minimum value scanned for the top of the eye diagram is denoted as VIHLTop and the maximum value scanned for the bottom of the eye diagram is denoted as VIHLBot.

10 Use the difference between VIHLTop and VIHLBot as the final test result VIHL(ac).

Expected/   The measured value of CA VIHL(ac) for the test signal shall be within the conformance limits as
Observable Results: defined in the Keysight D9050DDRC DDR5 Test Application.

SRIN_cIVW

Test ID: 12020

Test Overview: The purpose of this test is to verify the input slew rate over VcIVW Mask centered at Vcent_CA.
Refer to Figure 182 in the JESD79-5 specification.

Test Procedure: 1   Pre-condition the oscilloscope.

2   Check for valid Clock and CA input test signals by verifying its frequency and amplitude values.

3   Trigger on the falling edge of the Clock signal under test.

4   Set up Eye folding and Mask Test settings to use the Clock signal as the clock recovery source.

5   Acquire the number of waveforms specified in the configuration option 'Total CA Waveform'.

6   Determine and store the Vcent value. Vcent can be derived depending on the "Vcent Evaluation Mode" configuration option in the application.

7   Set the measurement thresholds - Upper, Middle, Lower to Mask Top Voltage, Vcent and Mask Bottom Voltage, respectively.

8   Set up Slew Rate Rising measurement on the CA signal to achieve the SRIN_ciVW Rise Time Maximum and SRIN_ciVW Rise Time Minimum. The worst value between maximum and minimum values obtained is set to WorstRisingSlewRate.

9   Set up Slew Rate Falling measurement on the DQ signal to achieve the SRIN_ciVW Fall Time Maximum and SRIN_ciVW Fall Time Minimum. The worst value between maximum and minimum values obtained is set to WorstFallingSlewRate.

10 The worst value between the WorstRisingSlewRate and WorstFallingSlewRate will be used as the final test result for SRIN_cIVW.

Expected/   The measured value of SRIN_cIVW for the test signal shall be within the conformance limits as
Observable Results: defined in the Keysight D9050DDRC DDR5 Test Application.

tCIPW

Test ID:	12030
Test Overview:	The purpose of this test is to verify the minimum input pulse width defined at Vcent_CA. Refer to Figure 182 in the JESD79-5 specification.

Test Procedure:

1 This test requires the following pre-requisite test:

· tCIVW Margin (Test ID: 12000): The location of Vcent_CA is determined and the its value is stored.

2 Perform the pulse width on the CA signal:

    a Set to ON the positive pulse width measurement and jitter statistics to measure all the edges.

    b Set the measurement threshold to a hysteresis of +/- 150mV at the threshold level of Vcent_CA.

    c Obtain the minimum result from the measurements as the worst positive pulse width.

    d Repeat steps a to c for negative pulse width and store the minimum result from the measurement as the worst negative pulse width.

3 Compare the minimum values from the positive and negative pulse width results.
Convert the unit for the values from seconds to UI.
Report the resulting value as the final test result.

Expected/ Observable Results: The measured tCIPW value for the test signal shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

Eye Diagram for Command Address

Test ID:	12050
Test Overview:	The purpose of this test is to automate all the required setup procedures required in order to generate an eye diagram for the Command Address signal. The additional feature of having a mask test is that it allows users to perform evaluations and debugging on the eye diagram created.

Test Procedure:

1 Acquire the Clock and CommandAddress signal.

2 Load acquired CommandAddress signal into WMemory4. Then use Function4 as "Magnify/Duplicate" of Loaded Waveform Memory.

3 Load Clock signal into WMemory1. Then use Function1 as "Magnify/Duplicate" of Loaded Waveform Memory.

4 Setup Clock Recovery settings on SDA.

    · Explicit clock, Source = Clock, Rise/Fall Edge

5 Setup measurement threshold values for the Function4(CommandAddress) and the Function1(Clock).

6 Setup fix time scale and time position values for Function4(CommandAddress) and Function1(Clock).

7 Turn ON Color Grade Display option.

8 Identify the X1 value for re-adjustment of selected test mask.

9 Setup Mask Test settings.

10 Turn ON Real Time Eye on SDA.

11 Start mask test until eye diagram folded.

12 Perform Eye Width Measurement:

a Set Histogram orientation into Horizontal

b Set:

X1= left boundary of screen

X2= Center of "widest opening voltage"

Y1= widest opening voltage

Y2= widest opening voltage

c EyeWidthT1= Histogram Max

d Set:

X1= Center of "widest opening voltage"

X2= right boundary of screen

Y1= widest opening voltage

Y2= widest opening voltage

e EyeWidthT2= Histogram Min

f Calculate EyeWidth = EyeWidthT2 - EyeWidthT1

13 Perform Eye Height Measurement:

a Set Histogram orientation into Vertical

b Set:

X1= Center of "widest opening voltage"

X2= Center of "widest opening voltage"

Y1= widest opening voltage

Y2= Bottom Level of display

c EyeHeightV1= Histogram Max

d Set:

X1= Center of "widest opening voltage"

X2= Center of "widest opening voltage"

Y1= Top Level of display

Y2= widest opening voltage

e EyeHeightV2= Histogram Min

f Calculate EyeHeight = EyeHeightV2 - EyeHeightV1

14 Return total failed UnitInterval as a test result.

Expected/
Observable Results: The measured Eye Diagram for CA value for the test signal is considered for 'Information-Only' purpose.

8 Stressed Eye tests

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Test Availability Conditions

All tests in this test group appear for the following configuration in DDR5 General Setup window:

Signal Source:

· Any set including DQS and DQ

Signal Operation Mode:

· CK (Diff) — Any
· DQS (Diff) — Continuous
· DQ — Any

TxEH_DQ_SES_1UI

Test ID: 18010

Test Overview: The purpose of this test is to measure the Eye Height specified at the transmitter with a skew of 1UI between DQ and DQS.

Test Procedure: 1   Perform signal conditioning on the DQ and DQS test signals.

2   Use continuous 101010... pattern for the DQS test signal and a typical data pattern for the DQ test signal.

3   Set up the Recovery Clock method to use "Explicit Clock" method with the DQS test signal as the clock source.

4   Use 0V as the reference measurement threshold for the DQS_diff test signal while for the DQ test, use the VrefDQ value (a configuration setting in the compliance application).

5   Configure the EZJIT feature settings in the Infiniium application to perform "TIE(Phase)" measurement with the Clock Reference setup based on the specified number of UI skew between DQS and DQ.

6   Perform the removal of scope random jitter. This feature can be enabled or disabled by configuring the "SESTest_RemoveScopeRJ_Mode" parameter under the Configure tab of the application.

7   Sample the required number of data waveforms to meet the total number of UI needed in a test run. The number of UI needed in a test run is configurable using the "SESTest_NumOfUI_PerTest" option under the Configure tab of the application.

8   For Eye Height measurement, use the "Eye Height" result from EZJIT.

Expected/ Observable Results: The measured value of Eye Height shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

TxEW_DQ_SES_1UI

Test ID: 18015

Test Overview: The purpose of this test is to measure the Eye Width specified at the transmitter with a skew of 1UI between DQ and DQS.

Test Procedure: 1   Perform signal conditioning on the DQ and DQS test signals.

2   Use continuous 101010... pattern for the DQS test signal and a typical data pattern for the DQ test signal.

3   Setup the Recovery Clock method to use "Explicit Clock" method with the DQS test signal as the clock source.

4   Use 0V as the reference measurement threshold for the DQS_diff, while for the DQ test, use the VrefDQ value (a configuration setting in the compliance application).

5   Configure the EZJIT feature settings in the Infiniium application to perform "TIE(Phase)" measurement with the Clock Reference setup based on the specified number of UI skew between DQS and DQ.

6   Perform the removal of scope random jitter. This feature can be enabled or disabled by configuring the "SESTest_RemoveScopeRJ_Mode" parameter under the Configure tab of the application.

7   Sample the required number of data waveforms to meet the total number of UI needed in a test run. The number of UI needed in a test run is configurable using the "SESTest_NumOfUI_PerTest" option under the Configure tab of the application.

8   For Eye Width measurement, use the TJ(p-p) measurement results from EZJIT. The Eye width will then be calculated as
EW = UI (ideal value based on data rate used) –TJ (measured result from EZJIT)

Expected/ Observable Results: The measured value of Eye Width shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

TxEH_DQ_SES_2UI

Test ID: 18020

Test Overview: The purpose of this test is to measure the Eye Height specified at the transmitter with a skew of 2UI between DQ and DQS.

Test Procedure: 1   Perform signal conditioning on the DQ and DQS test signals.

2   Use continuous 101010... pattern for the DQS test signal and a typical data pattern for the DQ test signal.

3   Setup the Recovery Clock method to use "Explicit Clock" method with the DQS test signal as the clock source.

4   Use 0V as the reference measurement threshold for the DQS_diff test signal while for the DQ test, use the VrefDQ value (a configuration setting in the compliance application).

5   Configure the EZJIT feature settings in the Infiniium application to perform "TIE(Phase)" measurement with the Clock Reference setup based on the specified number of UI skew between DQS and DQ.

6   Perform the removal of scope random jitter. This feature can be enabled or disabled by configuring the "SESTest_RemoveScopeRJ_Mode" parameter under the Configure tab of the application.

7   Sample the required number of data waveforms to meet the total number of UI needed in a test run. The number of UI needed in a test run is configurable using the "SESTest_NumOfUI_PerTest" option under the Configure tab of the application.

8   For Eye Height measurement, use the "Eye Height" result from EZJIT.

Expected/ Observable Results: The measured value of Eye Height shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

TxEW_DQ_SES_2UI

Test ID: 18025

Test Overview: The purpose of this test is to measure the Eye Width specified at the transmitter with a skew of 2UI between DQ and DQS.

Test Procedure:
1   Perform signal conditioning on the DQ and DQS test signals.
2   Use continuous 101010... pattern for the DQS test signal and a typical data pattern for the DQ test signal.
3   Setup the Recovery Clock method to use "Explicit Clock" method with the DQS test signal as the clock source.
4   Use 0V as the reference measurement threshold for the DQS_diff, while for the DQ test, use the VrefDQ value (a configuration setting in the compliance application).
5   Configure the EZJIT feature settings in the Infiniium application to perform "TIE(Phase)" measurement with the Clock Reference setup based on the specified number of UI skew between DQS and DQ.
6   Perform the removal of scope random jitter. This feature can be enabled or disabled by configuring the "SESTest_RemoveScopeRJ_Mode" parameter under the Configure tab of the application.
7   Sample the required number of data waveforms to meet the total number of UI needed in a test run. The number of UI needed in a test run is configurable using the "SESTest_NumOfUI_PerTest" option under the Configure tab of the application.
8   For Eye Width measurement, use the TJ(p-p) measurement results from EZJIT. The Eye width will then be calculated as
EW = UI (ideal value based on data rate used) –TJ (measured result from EZJIT)

Expected/ Observable Results: The measured value of Eye Width shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

TxEH_DQ_SES_3UI

Test ID: 18030

Test Overview: The purpose of this test is to measure the Eye Height specified at the transmitter with a skew of 3UI between DQ and DQS.

Test Procedure:
1   Perform signal conditioning on the DQ and DQS test signals.
2   Use the continuous 101010... pattern for the DQS test signal and a typical data pattern for the DQ test signal.
3   Setup the Recovery Clock method to use "Explicit Clock" method with the DQS test signal as the clock source.
4   Use 0V as the reference measurement threshold for the DQS_diff test signal, while for the DQ test, use the VrefDQ value (a configuration setting in the compliance application).
5   Configure the EZJIT feature settings in the Infiniium application to perform "TIE(Phase)" measurement with the Clock Reference setup based on the specified number of UI skew between DQS and DQ.
6   Perform the removal of scope random jitter. This feature can be enabled or disabled by configuring the "SESTest_RemoveScopeRJ_Mode" parameter under the Configure tab of the application.
7   Sample the required number of data waveforms to meet the total number of UI needed in a test run. The number of UI needed in a test run is configurable using the "SESTest_NumOfUI_PerTest" option under the Configure tab of the application.
8   For Eye Height measurement, use the "Eye Height" result from EZJIT.

**Expected/
Observable Results:** The measured value of Eye Height shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

TxEW_DQ_SES_3UI

Test ID: 18035

Test Overview: The purpose of this test is to measure the Eye Width specified at the transmitter with a skew of 3UI between DQ and DQS.

Test Procedure:
1 Perform signal conditioning on the DQ and DQS test signals.
2 Use continuous 101010... pattern for the DQS test signal and a typical data pattern for the DQ test signal.
3 Setup the Recovery Clock method to use "Explicit Clock" method with the DQS test signal as the clock source.
4 Use 0V as the reference measurement threshold for the DQS_diff, while for the DQ test, use the VrefDQ value (a configuration setting in the compliance application).
5 Configure the EZJIT feature settings in the Infiniium application to perform "TIE(Phase)" measurement with the Clock Reference setup based on the specified number of UI skew between DQS and DQ.
6 Perform the removal of scope random jitter. This feature can be enabled or disabled by configuring the "SESTest_RemoveScopeRJ_Mode" parameter under the Configure tab of the application.
7 Sample the required number of data waveforms to meet the total number of UI needed in a test run. The number of UI needed in a test run is configurable using the "SESTest_NumOfUI_PerTest" option under the Configure tab of the application.
8 For Eye Width measurement, use the TJ(p-p) measurement results from EZJIT. The Eye width will then be calculated as
EW = UI (ideal value based on data rate used) -TJ (measured result from EZJIT)

**Expected/
Observable Results:** The measured value of Eye Width shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

TxEH_DQ_SES_4UI

Test ID: 18040

Test Overview: The purpose of this test is to measure the Eye Height specified at the transmitter with a skew of 4UI between DQ and DQS.

Test Procedure:
1 Perform signal conditioning on the DQ and DQS test signals.
2 Use the continuous 101010... pattern for the DQS test signal and a typical data pattern for the DQ test signal.
3 Setup the Recovery Clock method to use "Explicit Clock" method with the DQS test signal as the clock source.
4 Use 0V as the reference measurement threshold for the DQS_diff test signal, while for the DQ test, use the VrefDQ value (a configuration setting in the compliance application).
5 Configure the EZJIT feature settings in the Infiniium application to perform "TIE(Phase)" measurement with the Clock Reference setup based on the specified number of UI skew between DQS and DQ.

6   Perform the removal of scope random jitter. This feature can be enabled or disabled by configuring the "SESTest_RemoveScopeRJ_Mode" parameter under the Configure tab of the application.

7   Sample the required number of data waveforms to meet the total number of UI needed in a test run. The number of UI needed in a test run is configurable using the "SESTest_NumOfUI_PerTest" option under the Configure tab of the application.

8   For Eye Height measurement, use the "Eye Height" result from EZJIT.

**Expected/
Observable Results:**   The measured value of Eye Height shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

TxEW_DQ_SES_4UI

Test ID: 18045

Test Overview: The purpose of this test is to measure the Eye Width specified at the transmitter with a skew of 4UI between DQ and DQS.

Test Procedure: 1   Perform signal conditioning on the DQ and DQS test signals.

2   Use continuous 101010... pattern for the DQS test signal and a typical data pattern for the DQ test signal.

3   Setup the Recovery Clock method to use "Explicit Clock" method with the DQS test signal as the clock source.

4   Use 0V as the reference measurement threshold for the DQS_diff, while for the DQ test, use the VrefDQ value (a configuration setting in the compliance application).

5   Configure the EZJIT feature settings in the Infiniium application to perform "TIE(Phase)" measurement with the Clock Reference setup based on the specified number of UI skew between DQS and DQ.

6   Perform the removal of scope random jitter. This feature can be enabled or disabled by configuring the "SESTest_RemoveScopeRJ_Mode" parameter under the Configure tab of the application.

7   Sample the required number of data waveforms to meet the total number of UI needed in a test run. The number of UI needed in a test run is configurable using the "SESTest_NumOfUI_PerTest" option under the Configure tab of the application.

8   For Eye Width measurement, use the TJ(p-p) measurement results from EZJIT. The Eye width will then be calculated as
EW = UI (ideal value based on data rate used) -TJ (measured result from EZJIT)

**Expected/
Observable Results:**   The measured value of Eye Width shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

TxEH_DQ_SES_5UI

Test ID: 18050

Test Overview: The purpose of this test is to measure the Eye Height specified at the transmitter with a skew of 5UI between DQ and DQS.

Test Procedure: 1   Perform signal conditioning on the DQ and DQS test signals.

2   Use continuous 101010... pattern for the DQS test signal and a typical data pattern for the DQ test signal.

3   Setup the Recovery Clock method to use "Explicit Clock" method with the DQS test signal as the clock source.

4   Use 0V as the reference measurement threshold for the DQS_diff test signal, while for the DQ test, use the VrefDQ value (a configuration setting in the compliance application).

5   Configure the EZJIT feature settings in the Infiniium application to perform "TIE(Phase)" measurement with the Clock Reference setup based on the specified number of UI skew between DQS and DQ.

6   Perform the removal of scope random jitter. This feature can be enabled or disabled by configuring the "SESTest_RemoveScopeRJ_Mode" parameter under the Configure tab of the application.

7   Sample the required number of data waveforms to meet the total number of UI needed in a test run. The number of UI needed in a test run is configurable using the "SESTest_NumOfUI_PerTest" option under the Configure tab of the application.

8   For Eye Height measurement, use the "Eye Height" result from EZJIT.

Expected/ Observable Results: The measured value of Eye Height shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

TxEW_DQ_SES_5UI

Test ID: 18055

Test Overview: The purpose of this test is to measure the Eye Width specified at the transmitter with a skew of 5UI between DQ and DQS.

Test Procedure: 1   Perform signal conditioning on the DQ and DQS test signals.

2   Use continuous 101010... pattern for the DQS test signal and a typical data pattern for the DQ test signal.

3   Setup the Recovery Clock method to use "Explicit Clock" method with the DQS test signal as the clock source.

4   Use 0V as the reference measurement threshold for the DQS_diff, while for the DQ test, use the VrefDQ value (a configuration setting in the compliance application).

5   Configure the EZJIT feature settings in the Infiniium application to perform "TIE(Phase)" measurement with the Clock Reference setup based on the specified number of UI skew between DQS and DQ.

6   Perform the removal of scope random jitter. This feature can be enabled or disabled by configuring the "SESTest_RemoveScopeRJ_Mode" parameter under the Configure tab of the application.

7   Sample the required number of data waveforms to meet the total number of UI needed in a test run. The number of UI needed in a test run is configurable using the "SESTest_NumOfUI_PerTest" option under the Configure tab of the application.

8   For Eye Width measurement, use the TJ(p-p) measurement results from EZJIT. The Eye width will then be calculated as
EW = UI (ideal value based on data rate used) −TJ (measured result from EZJIT)

Expected/ Observable Results: The measured value of Eye Width shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

9   DQS (Single Ended) tests

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Test Availability Conditions

All tests in this test group appear for the following configuration in DDR5 General Setup window:

Signal Source:
- DQS_t (Single Ended), DQS_c (Single Ended), DQ
- DQS_t (Single Ended), DQS_c (Single Ended), DQ, CA

Signal Operation Mode:
- CK (Diff) — Not Applicable
- DQS (Diff) — Burst
- DQ — Not Applicable

DQS Cross Point Voltage Test

Vix_DQS_ratio

Test ID: 19100

Test Overview: The purpose of this test is to verify the differential input crosspoint voltage ratio, Vix_DQS_ratio parameter.

Test Procedure:
1 Sample/Acquire data waveforms.
2 Split the read and write burst of the acquired signal.
3 Take the first valid WRITE burst found.
4 Use Subtract FUNC to generate the differential waveform from the 2 source input, DQS_diff.
5 Measure the VRMS of the DQS_diff and denote it as VDQS_RMS.
6 Find the time-stamp of all differential DQS crossing that crosses 0V within the burst found.
7 Use VTime to get the actual crossing point voltage value using the timestamp obtained.
8 Find the mean value of the burst data and denote it as the VDQSmid.
9 At each crosspoint (rising and falling) found, find the voltage differential between the crosspoint and VDQSmid. The rising and falling crosspoint voltage differential is denoted as Vix_DQS.
10 Calculate the crosspoint ratio using all the VIX_CK measured.

$$Vix\_DQS\_ratio = 100\% * VIX\_DQS / VDQS\_RMS$$

11 Determine the worst result from the set of Vix_DQS_ratio measured.

Expected/ Observable Results: The calculated value of the differential input crosspoint voltage ratio (Vix_DQS_ratio) shall be within the conformance limits as defined in the Keysight D9050DDRC DDR5 Test Application.

9   CA (Command Address) tests

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