Keysight D9040PCIC PCI Express® Compliance Test Application

Methods of Implementation

KEYSIGHT TECHNOLOGIES

Notices

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Keysight Technologies, Inc.
1900 Garden of the Gods Road
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PCI Express Automated Testing—At A Glance

The Keysight D9040PCIC PCI Express® Compliance Test Application helps you verify PCI Express device under test (DUT) compliance to specifications with the Keysight Infiniium oscilloscopes. The PCI Express® Compliance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE **The tests performed by the PCI Express® Compliance Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.**

Required Equipment and Software

In order to run the PCI Express automated tests, you need the following equipment and software:

- D9040PCIC PCI Express® Compliance Test Application software.
- Use one of the following oscilloscope models:
  - Keysight 90000 Series, 90000 X-Series, 90000 Q-Series, or Z-Series Infiniium oscilloscopes
  - Keysight UXR Series Infiniium Oscilloscopes
- Probes and/or test fixtures. For more information on the specific probes and test fixtures required, refer to the chapters that describe tests.
- N5380B Hi-BW differential SMA probe heads.
- Keyboard, qty = 1, (provided with the Keysight 90000X oscilloscope).
- Mouse, qty = 1, (provided with the Keysight 90000X oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, qty = 2 (provided with Keysight Infiniium oscilloscope).
- 50-ohm Coax Cable with SMA Male Connectors – 24-inch or less RG-316/U or similar, qty = 2, matched length.

NOTE **D9040PCIC PCI Express Compliance Test Application supports two channel scope.**

In This Book

This manual describes the tests that are performed by the PCI Express® Compliance Test Application in more detail; it contains information from (and refers to) the Base Specification, Card Electromechanical Specification, and ExpressCard Standard, and it describes how the tests are performed.

The chapters in this book are:

- Chapter 1, “Installing the PCI Express Compliance Test Application shows how to install and license the automated test application software (if it was purchased separately).
- Chapter 2, “Preparing to Take Measurements shows how to start the PCI Express® Compliance Test Application and gives a brief overview of how it is used.
- Chapter 3, “Probing the Link for Compliance” contains more information on link probing for Tx, Rx, CEM EndPoint, CEM RootComplex, and Reference Clock compliance.
- Chapter 4, “Compliance Tests” contains more information on the procedures for PCI Express Gen 1.0a, 1.1, 2.0, 3.0, and 4.0 compliance tests.
- Chapter 5, “Preset Equalization Tests at 8.0 GT/s and 16.0 GT/s for PCI-E 3.0 and PCI-E 4.0” contains more information on the required preset equalization tests.
- Chapter 6, “Compliance Test List” contains generation wise list of tests as per the application. Each test in the list is linked to its complete test procedure described in the chapter “Compliance Tests”
- .Chapter 7, “Specification Notes” contains generation wise list of specification notes for all the tables that have been referenced for pass limits.
- Appendix A, “Calibrating the Digital Storage Oscilloscope describes how to calibrate the oscilloscope in preparation for running the PCI Express automated tests.
- Appendix B, “InfiniiMax Probing Options describes the probe amplifier and probe head recommendations for PCI Express testing.
- Appendix C, “INF_SMA_Deskew.set Setup File Details describes a setup used when performing channel de-skew calibration.

See Also,

The PCI Express® Compliance Test Application's online help, which describes:

- PCI Express Automated Testing — At a Glance
- Starting the D9040PCIC PCI Express® Compliance Test Application
- Creating or Opening a Test Project
- Setting Up the Test Environment
- Selecting Tests
- Configuring Tests
- Verifying Physical Connections
- Running Tests
- Configuring Automation in the Test Application
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
- Additional Settings in the Test App

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1 Installing the PCI Express Compliance Test Application

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If you purchased the D9040PCIC PCI Express Compliance Test Application separately, you need to install the software and license key.

Installing the Software

1. To obtain the PCI Express Compliance Test Application, go to Keysight website: http://keysight.com/find/D9040PCIC
2. The link for PCI Express Compliance Test Application will appear. Double-click on it and follow the instructions to download and install the application software.

   Be sure to accept the installation of the .NET Framework software; it is required in order to run the PCI Express Compliance Test Application.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

1 Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.

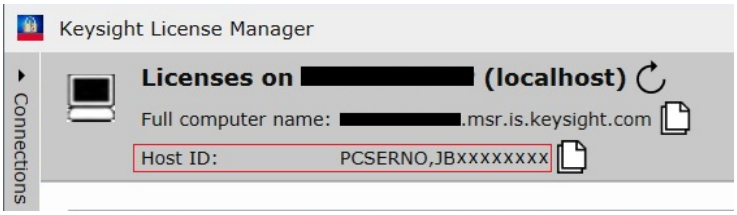


Figure 1 Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager.

3 From the configuration menu, use one of the options to install each license file.

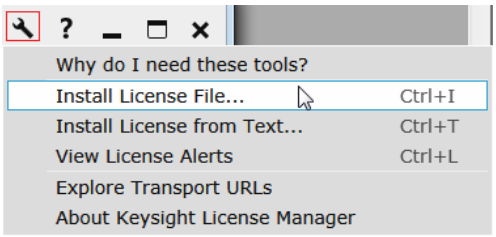


Figure 2 Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

1. Launch Keysight License Manager 6 on your machine, where you wish to run the Test Application and its features.
2. Copy the Host ID, which is the first set of alphanumeric value (as highlighted in Figure 3) that appears in the Environment tab of the application. Note that x indicates numeric values.

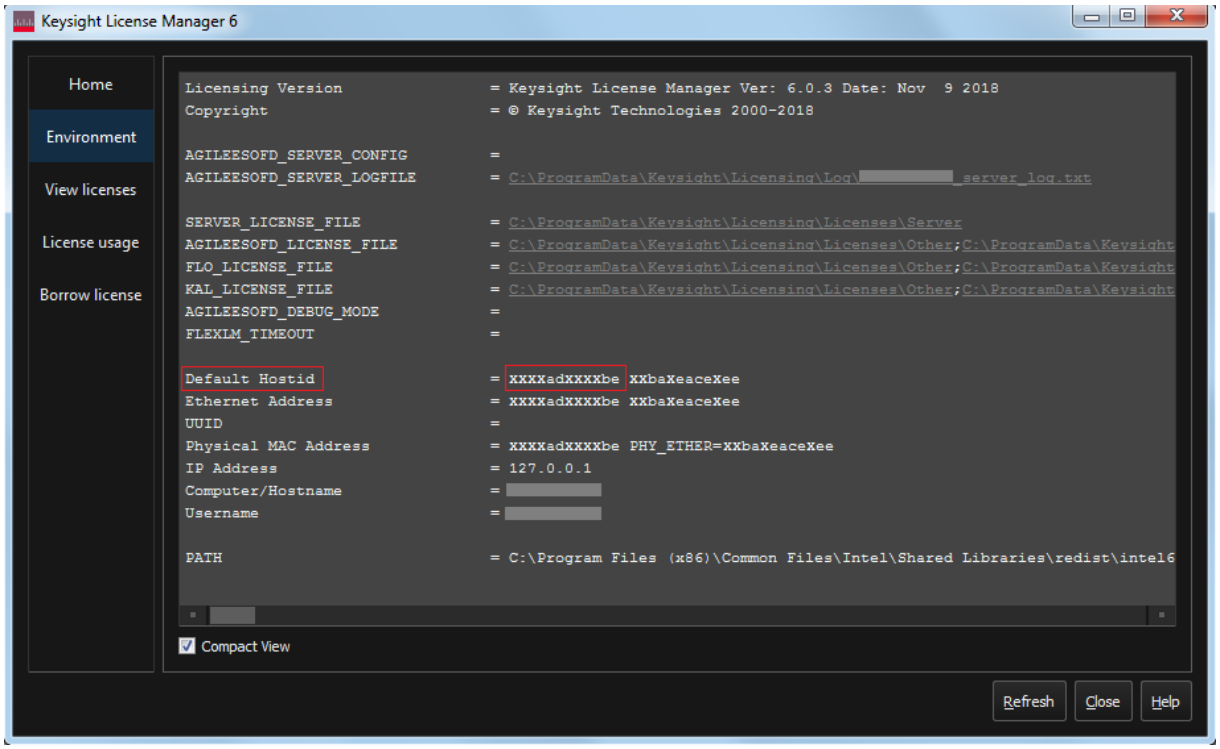


Figure 3 Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.
2 Launch Keysight License Manager 6.
3 From the Home tab, use one of the options to install each license file.

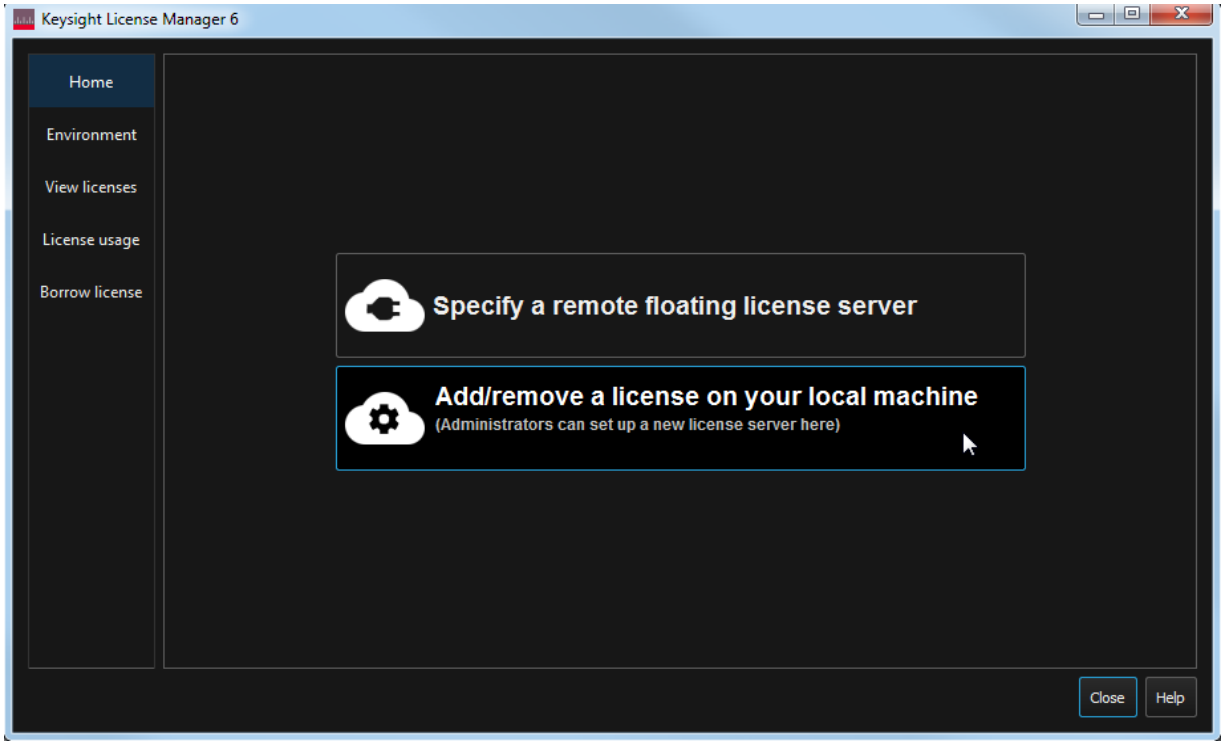


Figure 4 Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

2 Preparing to Take Measurements

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Before running the PCI Express automated tests, you should calibrate the oscilloscope. After the oscilloscope has been calibrated, you are ready to start the PCI Express Compliance Test Application and perform measurements.

Calibrating the Oscilloscope

If you haven't already calibrated the oscilloscope, see Appendix A, "Calibrating the Digital Storage Oscilloscope.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration and channel de-skew calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel they were calibrated for.

Starting the PCI Express Compliance Test Application

1 From the Infiniium oscilloscope's main menu, choose **Analyze > Automated Test Apps > D9040PCIC PCIExpress Test App.**

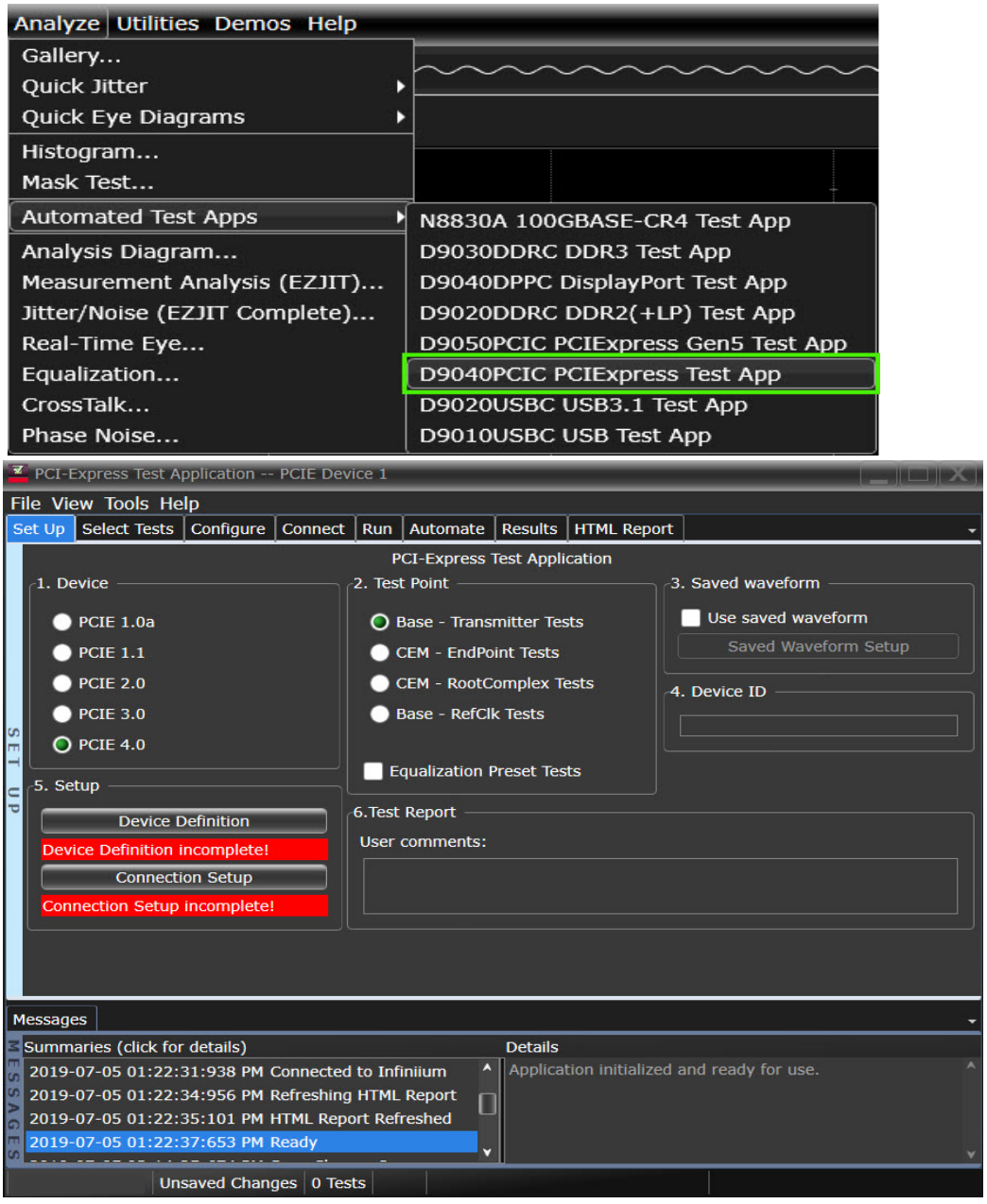


Figure 5 The PCI Express Compliance Test Application

NOTE If PCI Express does not appear in the Automated Test Apps menu, the PCI Express Compliance Test Application has not been installed (see Chapter 1, "Installing the PCI Express Compliance Test Application).

Figure 5 shows the PCI Express Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Tab	Description
Set Up	Lets you identify and set up the test environment, including information about the device under test.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure the test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automate	Allows to automate tests through automation commands.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

Online Help Topics

For information on using the PCI Express Compliance Test Application, see its online help (which you can access by choosing **Help > Help Contents...** from the application's main menu).

The PCI Express Compliance Test Application's online help describes:

- Starting the PCI Express Compliance Test Application.
  - To view or minimize the task flow pane.
  - To view or hide the toolbar.
- Creating or opening a test project.
- Setting up the test environment.
  - To set up InfiniiSim.
  - To load saved waveforms.
- Selecting tests.
- Configuring selected tests.
- Connecting the oscilloscope to the Device Under Test (DUT).
- Running tests.
  - To select the "store mode".
  - To run multiple times.
  - To send email on pauses or stops.
  - To specify the event.
  - To set the display preferences.
  - To set the run preferences.
- Viewing test results.
  - To delete trials from the results.
  - To show reference images and flash mask hits.
  - To change margin thresholds.
  - To change the test display order.
  - To set trial display preferences.
- Viewing/exporting/printing the HTML test report.
  - To export the report.
  - To print the report.
- Saving test projects.
  - To set AutoRecovery preferences.
- Controlling the application via a remote PC.
  - To check for the App Remote license.
  - To identify the remote interface version.
  - To enable the remote interface.
  - To enable remote interface hints.
- Using a second monitor.

Clock Recovery and Analysis (Applicable to PCI Express 1.0a Only)

As described in Section 4.3.3.1 of the Base Specification, the following methodology is used to define the data set for all PCI Express eye and jitter measurements.

- The clock recovery window is 3500 consecutive Unit Intervals and the Mean of the UIs is used as the reference clock. The first 3500 UIs in the acquisition are used.
- An analysis window is established to be 250 bits centered in the 3500 UI clock recovery window. The mask is placed based on the median of the 250 bit analysis window.
- If there are enough data points in the record, the clock recovery window is advanced by 100 UI, a new mean UI is computed, and analysis is repeated over the middle 250 UI. This process is repeated until the advancing clock recovery window passes the end of the data record.

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Probing the Link for Tx Compliance

Transmitter tests are done by connecting the device under test to a test fixture and probing the SMA connectors on the test fixture. To probe the transmitter link, you can:

- Use two 50-ohm coax cables with SMA male connectors, two precision 3.5 mm BNC to SMA male adapters (included with the oscilloscope), and the channel 1 and channel 3 inputs of Keysight 90000X series Infiniium oscilloscope with 20 GSa/s or Keysight UXR oscilloscope with 16 GSa/s sample rate, available on two channels.
- Use two differential probe heads with two 1134A/B probe amplifiers (with the negative lead grounded for single-ended measurements) and the channel 1 and channel 3 inputs of Keysight 90000X series Infiniium oscilloscope with 20 GSa/s or Keysight UXR oscilloscope with 16 GSa/s sample rate, available on two channels.
- Use one differential probe head with the 1134A/B probe amplifier and the channel 2 input of Keysight 90000X series Infiniium oscilloscope with 20 GSa/s or Keysight UXR oscilloscope with 16 GSa/s sample rate, available on that channel.

When the link is broken and terminated into a 50 ohm load (by the test load), the Compliance Pattern defined in Base Specification will be transmitted.

Table 1 Probing Options for Transmitter Testing at 2.5 GT/s

	Probing Configurations			Captured Waveforms		Oscilloscope Specifications	
	Probing Method	Break Serial Link	Channels Used	Differential Mode	Common Mode	System Band Width	Rise* Time (20-80)
	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	6 GHz	70 ps
	Single-Ended (2 x 1134A/B w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	6 GHz	70 ps
	Differential (1 x 1134A/B w/ Differential Probe Head)	Y/N	1	True	No	6 GHz	70 ps

*Typical

Table 2 Probing Options for Transmitter Testing at 5.0 GT/s

	Probing Configurations			Captured Waveforms		Oscilloscope Specifications	
	Probing Method	Break Serial Link	Channels Used	Differential Mode	Common Mode	System Band Width	Rise* Time (20-80)
	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	12 GHz	70 ps
	Single-Ended (2 x 1134A/B w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	12 GHz	70 ps
	Differential (1 x 1134A/B w/ Differential Probe Head)	Y/N	1	True	No	12 GHz	70 ps
*Typical							

Table 3 Probing Options for Transmitter Testing at 8.0 GT/s

	Probing Configurations			Captured Waveforms		Oscilloscope Specifications	
	Probing Method	Break Serial Link	Channels Used	Differential Mode	Common Mode	System Band Width	Rise* Time (20-80)
	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	12 GHz	70 ps
	Single-Ended (2 x 1134A/B w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	12 GHz	70 ps
	Differential (1 x 1134A/B w/ Differential Probe Head)	Y/N	1	True	No	12 GHz	70 ps
*Typical							

Table 4 Probing Options for Transmitter Testing at 16.0 GT/s

	Probing Configurations			Captured Waveforms		Oscilloscope Specifications	
	Probing Method	Break Serial Link	Channels Used	Differential Mode	Common Mode	System Band Width	Rise* Time (20-80)
	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	12 GHz	70 ps
	Single-Ended (2 x 1134A/B w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	12 GHz	70 ps
	Differential (1 x 1134A/B w/ Differential Probe Head)	Y/N	1	True	No	12 GHz	70 ps
*Typical							

Single-Ended SMA Probing

The differential signal is created by the PCI Express Compliance Test Application software from the math waveform Source 1 - Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

This probing technique requires breaking the link and terminating into the 50 ohm/side termination into the oscilloscope. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

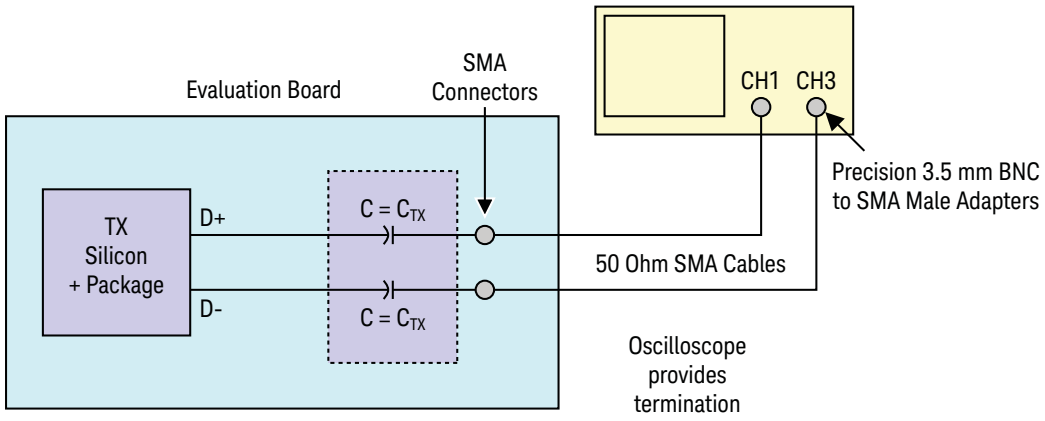


Figure 6 Single-Ended SMA Probing

Single-Ended Probing

The differential signal is created by the PCI Express Compliance Test Application software from the math waveform Source 1 - Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

For more information on the probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 565.

Place single-ended grounds as close to the signal line’s reference ground as possible.

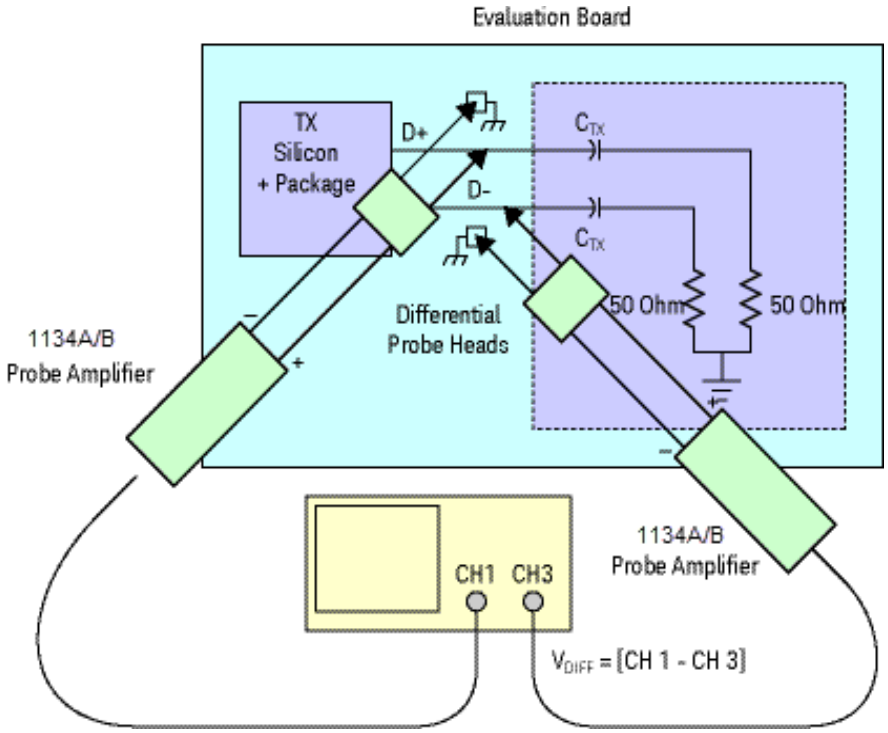


Figure 7 Single-Ended Probing

Differential Probing

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Only one channel of the oscilloscope is used.

For more information on the probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 565.

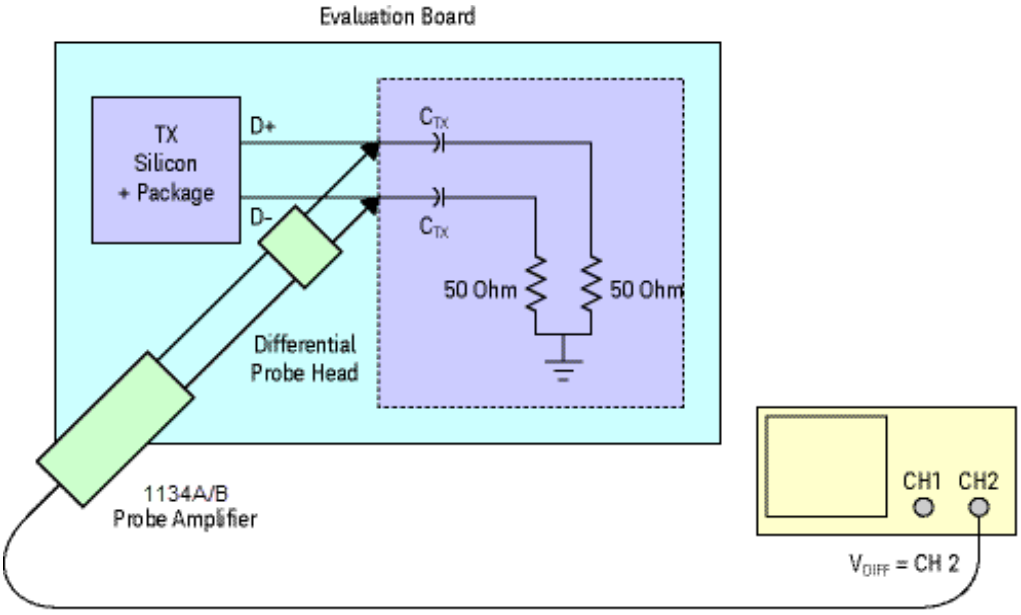


Figure 8 Differential Probing

NOTE

At 2.5 GT/s and 5.0 GT/s data rates, a coupling capacitor may or may not be needed depending on the transmitters.

At 8.0 GT/s and 16.0 GT/s data rate, a coupling capacitor is not required.

Tx Compliance Test Load

The compliance test load for driver compliance is shown in Figure 4-25 (Base Specification)

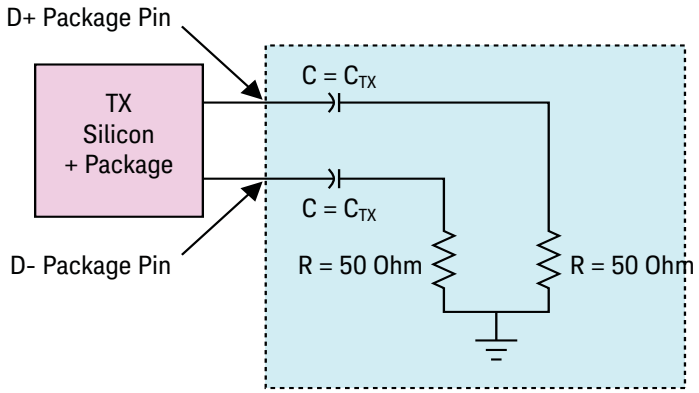


Figure 9 Driver Compliance Test Load.

Probing the Link for Rx Compliance

Receiver tests are done by probing the link as close as is feasibly possible to the pins of the receiver device. Alternatively, a dummy load can be used for the termination of the link. To probe the receiver link, you can:

- Use two differential probe heads with two 1169A/B probe amplifiers (with the negative lead grounded for single-ended measurements) and the Ch1 and Ch3 inputs of Keysight 90000X series Infiniium oscilloscope with 40 GSa/s or Keysight UXR oscilloscope with 32 GSa/s sample rate, available on two channels.
- Use one differential probe head with the 1169A/B probe amplifier and the Ch2 input of Keysight 90000X series Infiniium oscilloscope with 40 GSa/s or Keysight UXR oscilloscope with 32 GSa/s sample rate, available on that channel.
-

Table 5 Probing Options for Receiver Testing at 2.5 GT/s

	Probing Configurations			Captured Waveforms	
	Probing Method	Break Serial Link	Channels Used	Differential Mode	Common Mode
	Single-Ended (2 x 1134A/B w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes
	Differential (1 x 1134A/B w/ Differential Probe Head)	Y/N	1	True	No

Table 6 Probing Options for Receiver Testing at 5.0 GT/s

	Probing Configurations			Captured Waveforms		System Specifications	
						90000X	
	Probing Method	Break Serial Link	Channels Used	Differential Mode	Common Mode	System Band Width	Rise* Time (20-80)
	Single-Ended (2 x 1169A/B w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	12 GHz	70 ps
	Differential (1 x 1169A/B w/ Differential Probe Head)	Y/N	1	True	No	12 GHz	70 ps
*Typical							

Single-Ended Probing (Ch1) and (Ch3)

The differential signal is created by the PCI Express Compliance Test Application software from the math waveform Ch1-Ch3. The Common mode measurements are also available in this configuration from the common mode waveform (Ch1+Ch3)/2.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a “dummy load.”

Channel-to-channel de-skew is required using this technique because two channels are used.

For more information on the 1169A/B probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 565.

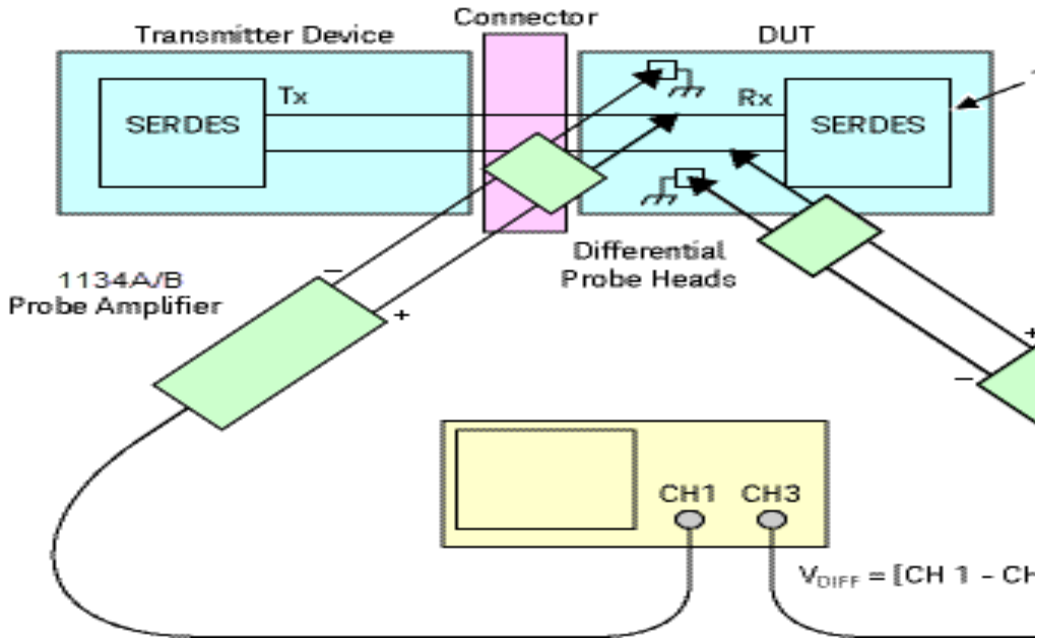


Figure 10 Single-Ended Probing

Differential Probing (Ch2)

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a “dummy load.”

A single channel of the oscilloscope is used, so de-skew is not necessary.

For more information on the 1169A/B probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 565.

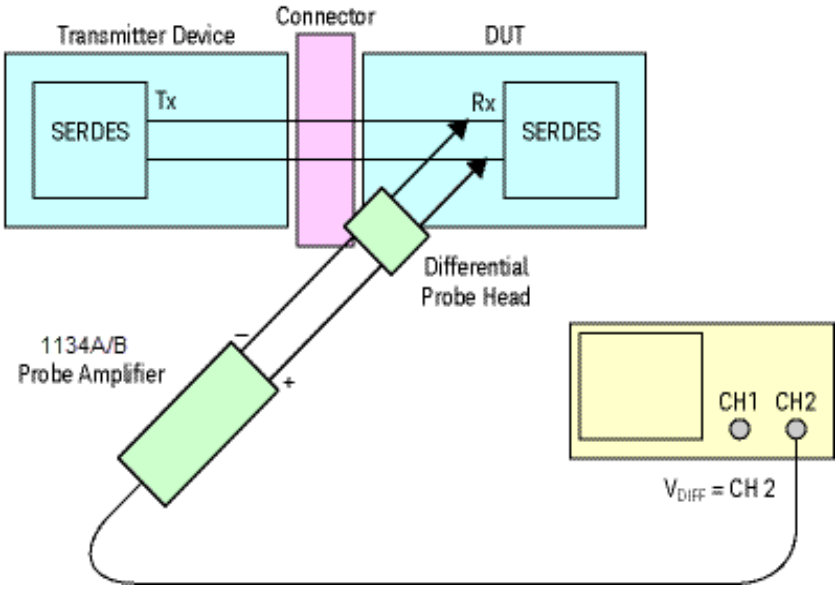


Figure 11 Differential Probing

Probing the Link for CEM-EndPoint Compliance

Connecting the Compliance Base Board for CEM-EndPoint Testing

There are multiple pairs of SMP connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the Add-in card fixture power supply powered off, connect the power supply connector to the Add-in card test fixture, and connect the device under test add-in card to the by-16 connector slot.

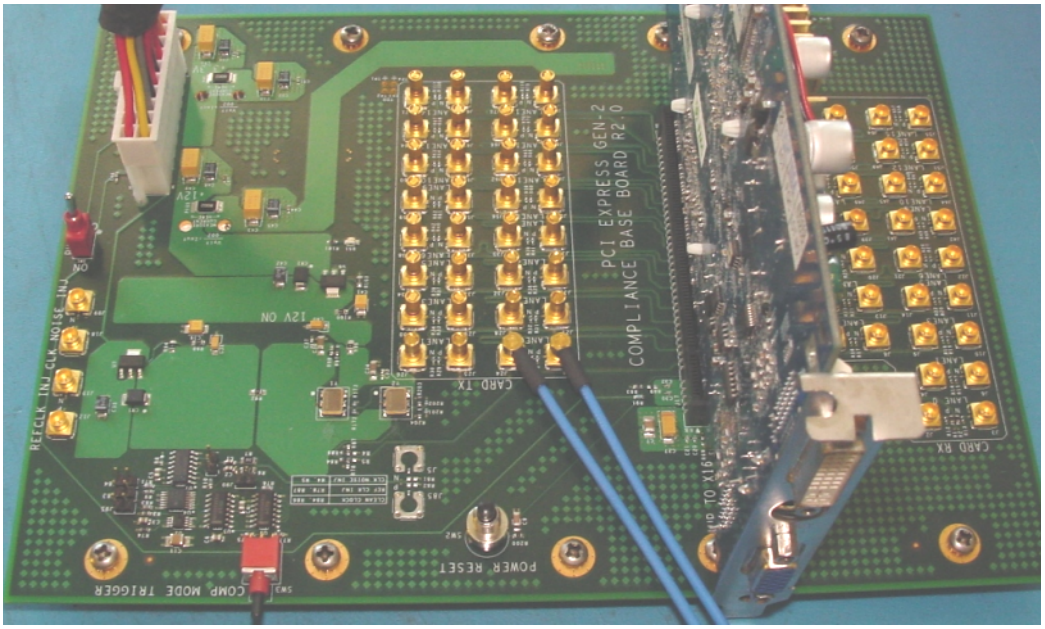


Figure 12 Compliance Base Board (CBB) Add-in Card Fixture

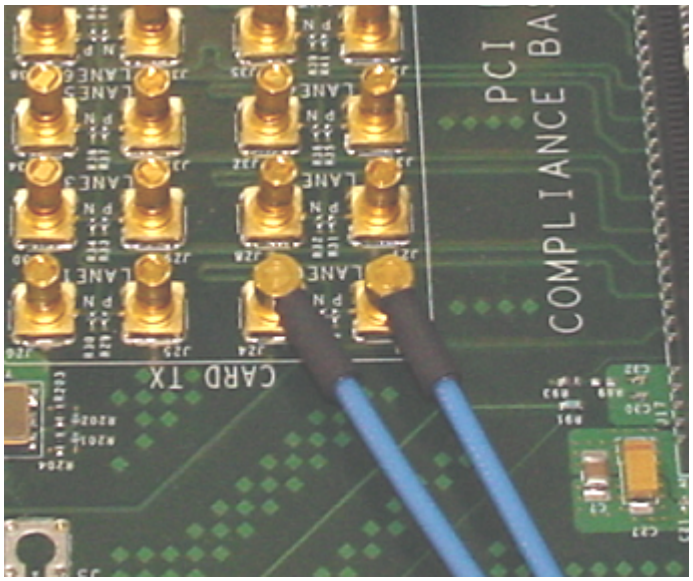


Figure 13 Compliance Base Board (CBB) 2.0 SMP Probing Option

2 Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB and 5.0 GHz at 6.0 dB.

3 Connect cables up as follows:

a Digital Storage Oscilloscope channel 1 to the D+ (where Lane 1 is under test in this example shown in Figure 13 above).

b Digital Storage Oscilloscope channel 3 to the D- (where Lane 1 is under test in this example shown in Figure 13 above).

When SMP probing and two channels are used, channel-to-channel deskew is required (see "Channel-to-Channel De-skew" on page 559).

Not all lanes have SMP probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes. For more information on the probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 565.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

4 Connect adequate load to the power supply to assure it is regulating and turned on. Generally, one IDE hard drive will provide adequate load.

5 Turn on the power supply. DS1 LED (located near the ATX power supply connector) should turn on. If the LED is on, but the power supply does not turn on, check that the jumper J7 is installed between J7-1 and J7-2.

Probing the Link for CEM-RootComplex Compliance

Connecting the Signal Quality Load Board for System/Motherboard Testing

There are multiple pairs of SMP connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the system/motherboard powered off, connect the Compliance PCI Express Signal Quality Load Board into the connector under test. The are 2 types of PCI Express Signal Quality Load Board edge fingers combination available - x1 and x16 connectors, as well as x4 and x8 connectors.

The PCI Express Signal Quality Load Board will cause a PCI Express 2.0 Base Specification System/motherboard to enter the compliance sub-state of the polling state. During this state the device under test will repeatedly send out the compliance pattern defined in the PCI Express Base Specification.

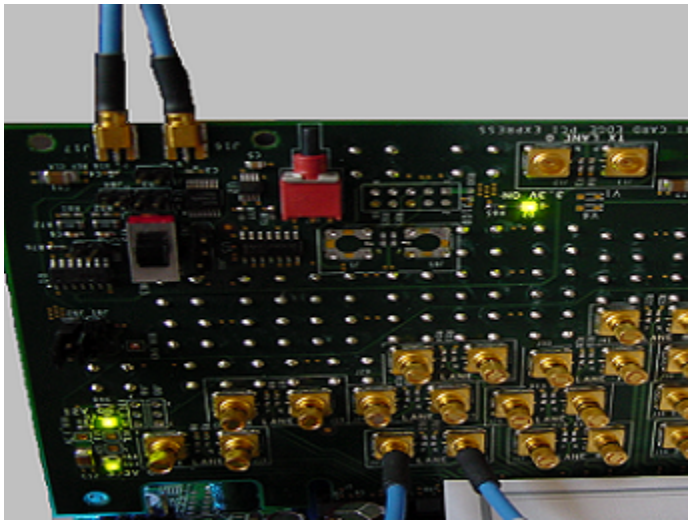


Figure 14 SMP Probing Option

2 Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB and 5.0 GHz at 6.0 dB.

3 Connect cables up as follows:

a Digital Storage Oscilloscope channel 1 to Data and Channel 3 to Clock OR

b Digital Storage Oscilloscope channel 2 to Data and Channel 4 to Clock.

When SMP probing and two channels are used, channel-to-channel deskew is required (see "Channel-to-Channel De-skew" on page 559).

Not all lanes have SMP probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes. For more information on the probe amplifiers and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 565.

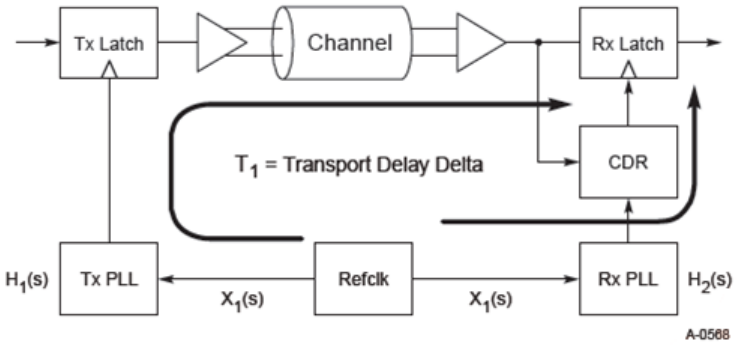
When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

Reference Clock Architectures

For PCI-E 2.0, there are two main reference clock architectures – common clock architecture and data clock architecture.

Common Clock Architecture

This section describes the common Refclk Rx architecture.



$$X_{CC}(s) = X_1(s) * H_{CC}(s)$$

$$H_{CC}(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2} e^{-sT_1} - \frac{2s\zeta_2\omega_{n2} + \omega_{n2}^2}{s^2 + 2s\zeta_2\omega_{n2} + \omega_{n2}^2} \right]$$

Jitter contribution from H_1 Jitter contribution from H_2

Table 7 Difference Function Parameters Applied to the Refclk Measurement

Symbol	Parameter	Min	Max	Units	Comments
T_1	Data/clock transport delay delta		12	ns	See Note 1.
ω_1	PLL #1 natural frequency	4.31*2π or 1.82*2π		Mrad/s	See Notes 1, 2, and 3.
ζ_1	PLL #1 damping factor	0.54 or 1.16	1.75 (0.5 dB)		See Notes 1 and 2.
ω_2	PLL #2 natural frequency		8.61*2π	Mrad/s	See Note 1.
ζ_2	PLL #2 damping factor	0.54 or 1.16	1.75 (0.5 dB)		See Notes 1, 2, and 4.

NOTES:

T1 defines the cumulative transport delay delta of the data and Refclk paths as shown in the above diagram and includes both off-chip and on-chip delay terms. The maximum internal transport delay for Tx and Rx is 2.0 ns.

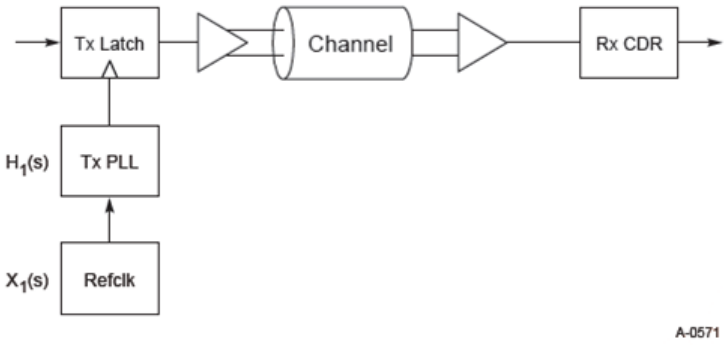
For the common Refclk Rx architecture, two possible combinations of minimum PLL BW and corresponding peaking are specified. If the min PLL BW is ³5 MHz, then a max peaking of 1.0 dB (corresponding to z = 1.16) is required. If the min PLL BW is ³8 MHz, then 3 dB of peaking (corresponding to z = 0.54) is allowed.

The natural frequency limits for PLL #1 correspond to –3 dB cut-off frequencies of 8.0 MHz (4.31e6*2p) and 5.0 MHz (1.82e6*2p).

The natural frequency limit for PLL #2 corresponds to a –3 dB cut-off frequency of 16 MHz.

Data Clock Architecture

This section describes the data driving architecture.



$$X_{DC}(s) = X_1(s) * H_1(s)$$

$$H_1(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2} \right]$$

Table 8 PLL Parameters for the Data Clocked Rx Architecture

Symbol	Parameter	Min	Max	Units	Comments
ω_1	Tx PLL natural frequency		8.61*2π	Mrad/s	See Note 1.
ζ_1	Tx PLL damping factor	0.54 (3.0 dB)	1.75 (0.5 dB)		See Notes 1 and 2.

NOTES:

1 The ω_1 and ζ_1 correspond to 16 MHz with 3.0 dB of peaking. Note that for the data driving architecture, we cannot take advantage of the differencing function for two PLLs and must instead apply the full
0-16 MHz/3.0 dB peaking PLL transfer function. Similarly, the lack of an Rx PLL obviates the need for defining a transport delay parameter.

2 A minimum peaking is also specified in order to place an upper limit on the amount of energy in the rolloff of the PLL. Since ζ_1 defines both the peaking and rolloff, a minimum and maximum for ζ_1 uniquely defines the amount of BW in the rolloff region.

Probing the Link for Reference Clock Compliance

Reference Clock tests are done by connecting the device under test to a test fixture and probing the SMA connectors on the test fixture. To probe the reference clock link, you can:

- Use two 50-ohm coax cables with SMA male connectors, two precision 3.5 mm BNC to SMA male adapters (included with the oscilloscope), and the channel 1 and channel 3 inputs of Keysight 90000X series Infiniium oscilloscope with 20 GSa/s or Keysight UXR oscilloscope with 16 GSa/s sample rate, available on two channels.
- Use two differential probe heads with two 1134A/B probe amplifiers (with the negative lead grounded for single-ended measurements) and the channel 1 and channel 3 inputs of Keysight 90000X series Infiniium oscilloscope with 20 GSa/s or Keysight UXR oscilloscope with 16 GSa/s sample rate, available on two channels.
- Use one differential probe head with the 1134A/B probe amplifier and the channel 2 input of Keysight 90000X series Infiniium oscilloscope with 20 GSa/s or Keysight UXR oscilloscope with 16 GSa/s sample rate, available on that channel.

Table 9 Probing Options for Reference Clock Testing at 2.5 GT/s

	Probing Configurations			Captured Waveforms		Oscilloscope Specifications	
	Probing Method	Break Serial Link	Channels Used	Differential Mode	Common Mode	System Band Width	Rise* Time (20-80)
	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	6 GHz	70 ps
	Single-Ended (2 x 1134A/B w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	6 GHz	70 ps
	Differential (1 x 1134A/B w/ Differential Probe Head)	Y/N	1	True	No	6 GHz	70 ps

*Typical

Table 10 Probing Options for Reference Clock Testing at 5.0 GT/s

	Probing Configurations			Captured Waveforms		Oscilloscope Specifications	
	Probing Method	Break Serial Link	Channels Used	Differential Mode	Common Mode	System Band Width	Rise* Time (20-80)
	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	6 GHz	70 ps
	Single-Ended (2 x 1134A/B w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	6 GHz	70 ps
	Differential (1 x 1134A/B w/ Differential Probe Head)	Y/N	1	True	No	6 GHz	70 ps
*Typical							

Table 11 Probing Options for Reference Clock Testing at 8.0 GT/s

	Probing Configurations			Captured Waveforms		Oscilloscope Specifications	
	Probing Method	Break Serial Link	Channels Used	Differential Mode	Common Mode	System Band Width	Rise* Time (20-80)
	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	6 GHz	70 ps
	Single-Ended (2 x 1134A/B w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	6 GHz	70 ps
	Differential (1 x 1134A/B w/ Differential Probe Head)	Y/N	1	True	No	6 GHz	70 ps
*Typical							

Table 12 Probing Options for Reference Clock Testing 16.0 GT/s

	Probing Configurations			Captured Waveforms		Oscilloscope Specifications	
	Probing Method	Break Serial Link	Channels Used	Differential Mode	Common Mode	System Band Width	Rise* Time (20-80)
	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	6 GHz	70 ps
	Single-Ended (2 x 1134A/B w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	6 GHz	70 ps
	Differential (1 x 1134A/B w/ Differential Probe Head)	Y/N	1	True	No	6 GHz	70 ps
*Typical							

Single-Ended SMA Probing

The differential signal is created by the PCI Express Compliance Test Application software from the math waveform Source 1 – Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

This probing technique requires breaking the link and terminating into the 50 ohm/side termination into the oscilloscope. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

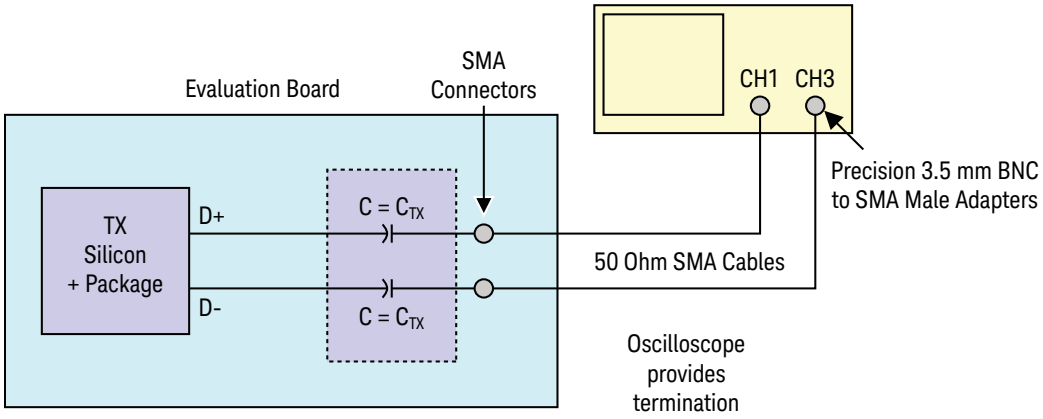


Figure 15 Single-Ended SMA Probing using Channel 1 and Channel 3

Single-Ended Probing

The differential signal is created by the PCI Express Compliance Test Application software from the math waveform Source 1 – Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

Make sure to probe equal distances from the reference clock, as close as possible to the reference clock. Place single-ended grounds as close to the signal line's reference ground as possible. Channel-to-Channel deskew is required using this probing technique because two channels are used.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

For more information on the 1134A/B probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 565.

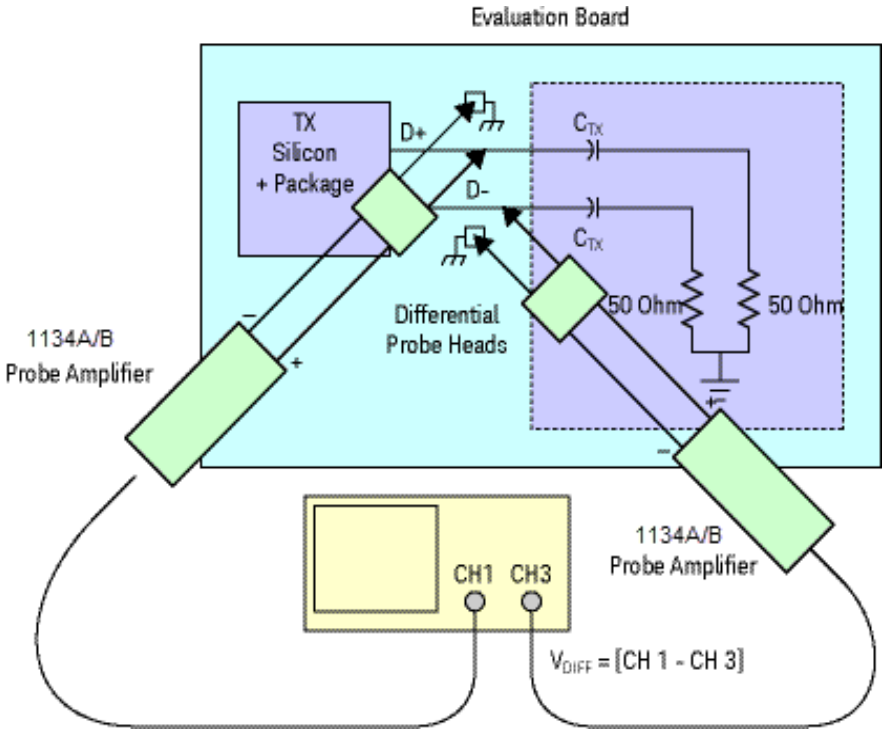


Figure 16 Single-Ended Probing

Differential Probing

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the reference clock, as close as possible to the reference clock.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Only one channel of the oscilloscope is used.

For more information on the 1134A/B probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 565.

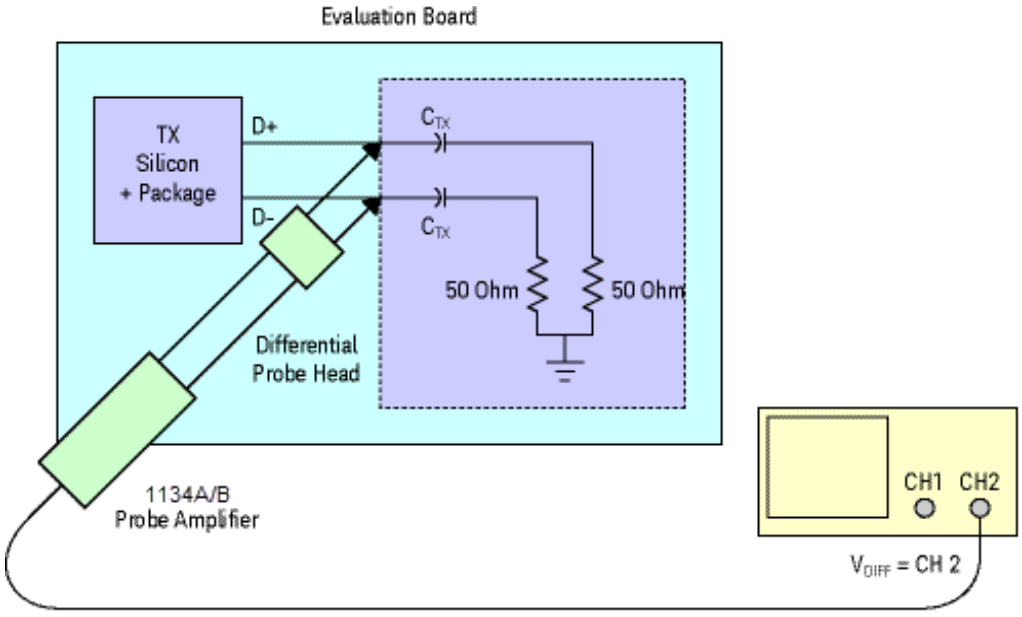


Figure 17 Differential Probing

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in Figure 4-25 of the Card Electromechanical Specification.

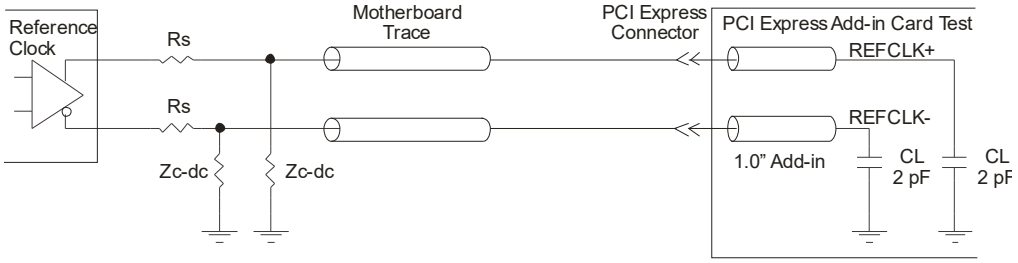


Figure 18 Driver Compliance Test Load

4 Compliance Tests

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This section provides the Methods of Implementation (MOIs) for PCI Express compliance tests using a Keysight Q-Series, Z-Series, or UXR-Series (13 GHz – 33 GHz) Infiniium Oscilloscope,1134A/B or 1169A/B probes, and the PCI Express Compliance Test Application.

NOTE Two lane tests in case of single-ended connections can also be run without using/enabling Switch Matrix. This feature is applicable only to Base - Transmitter Tests and the CEM - EndPoint Tests in case of four channel scope. Also, it is not supported on a two channel scope.

NOTE In this document, the terms Half Power or Low Power should be considered equivalent. Similarly, the terms, Full Power and High Power should be considered as one and the same.

Running Signal Quality Tests

Please see the PCI Express Online Help for steps to run the tests.

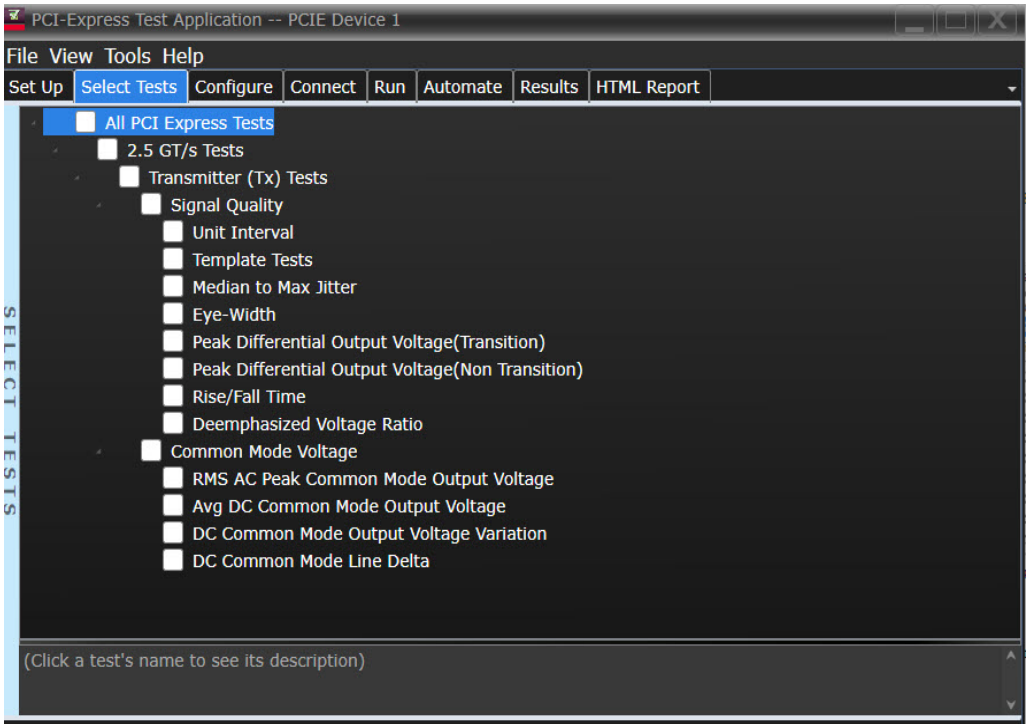


Figure 19 Select Tests Tab

Unit Interval Test

A recovered receiver/transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$R_x \qquad UI(p) = Mean \qquad (UI(n))$$

OR

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The Rx/Tx UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another Rx/Tx UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case Rx/Tx UI is reported.

Pass Limits

Table 13 Passing Limits Table for Unit Interval Test (Parameter: UI)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) **(Min to Nom to Max)**	Reference
PCIe1.0a	Base - Transmitter Tests	2.5 GT/s	Clean Clock	399.88 to 400 to 400.12	Base Spec 1.0a, Table 4-5
			SSC	399.88 to 400 to 400.12	Base Spec 1.0a, Table 4-5
	Base - Receiver Tests	2.5 GT/s	Clean Clock	399.88 to 400 to 400.12	Base Spec 1.0a, Table 4-6
			SSC	399.88 to 400 to 400.12	Base Spec 1.0a, Table 4-6
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	399.88 to 400 to 400.12	N/A (Information Only Test)
			SSC	399.88 to 400 to 400.12	N/A (Information Only Test)
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	399.88 to 400 to 400.12	N/A (Information Only Test)
			SSC	399.88 to 400 to 400.12	N/A (Information Only Test)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Nom to Max)	Reference

Table 13 Passing Limits Table for Unit Interval Test (Parameter: UI)

PCIe1.1	Base - Transmitter Tests	2.5 GT/s	Clean Clock	399.88 to 400 to 400.12	Base Spec 1.1, Table 4-5
			SSC	399.88 to 400 to 400.12	Base Spec 1.1, Table 4-5
	Base - Receiver Tests	2.5 GT/s	Clean Clock	399.88 to 400 to 400.12	Base Spec 1.1, Table 4-6
			SSC	399.88 to 400 to 400.12	Base Spec 1.1, Table 4-6
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	399.88 to 400 to 400.12	N/A (Information Only Test)
			SSC	399.88 to 400 to 400.12	N/A (Information Only Test)
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	399.88 to 400 to 400.12	N/A (Information Only Test)
			SSC	399.88 to 400 to 400.12	N/A (Information Only Test)
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A (Not Applicable)	N/A (Not Applicable)
			SSC	N/A (Not Applicable)	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference
PCIe2.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	399.88 to 400.12	Base Spec 2.0, Table 4-9
			SSC	399.88 to 400.12	Base Spec 2.0, Table 4-9
	Base - Receiver Tests	2.5 GT/s	Clean Clock	399.88 to 400.12	Base Spec 2.0, Table 4-12
			SSC	399.88 to 400.12	Base Spec 2.0, Table 4-12
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	399.88 to 400.12	N/A (Information Only Test)
			SSC	399.88 to 400.12	N/A (Information Only Test)
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	399.88 to 400.12	N/A (Information Only Test)
			SSC	399.88 to 400.12	N/A (Information Only Test)
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A (Not Applicable)	N/A (Not Applicable)
			SSC	N/A (Not Applicable)	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference

Table 13 Passing Limits Table for Unit Interval Test (Parameter: UI)

PCIe2.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	199.94 to 200.06	Base Spec 2.0, Table 4-9
			SSC	199.94 to 200.06	Base Spec 2.0, Table 4-9
	Base - Receiver Tests	5.0 GT/s	Clean Clock	Data Clk: 199.94 to 200.06 Ref Clk: 199.94 to 200.06	Data Clk: Base Spec 2.0, Table 4-12 Ref Clk: Base Spec 2.0, Table 4-12
			SSC	Data Clk: 199.94 to 200.06 Ref Clk: 199.94 to 200.06	Data Clk: Base Spec 2.0, Table 4-12 Ref Clk: Base Spec 2.0, Table 4-12
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	For -3.5 dB: 199.94 to 200.06 For -6.0 dB: 199.94 to 200.06	For -3.5 dB: N/A (Information Only Test) For -6.0 dB: N/A (Information Only Test)
			SSC	For -3.5 dB: 199.94 to 200.06 For -6.0 dB: 199.94 to 200.06	For -3.5 dB: N/A (Information Only Test) For -6.0 dB: N/A (Information Only Test)
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	199.94 to 200.06	N/A (Information Only Test)
			SSC	199.94 to 200.06	N/A (Information Only Test)
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A (Not Applicable)	N/A (Not Applicable)
			SSC	N/A (Not Applicable)	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference
PCIe3.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	399.88 to 400.12	Base Spec 3.0, Table 4-18
			SSC	399.88 to 400.12	Base Spec 3.0, Table 4-18
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	399.88 to 400.12	N/A (Information Only Test)
			SSC	399.88 to 400.12	N/A (Information Only Test)
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	399.88 to 400.12	N/A (Information Only Test)
			SSC	399.88 to 400.12	N/A (Information Only Test)
	U.2 - EndPoint Tests	2.5 GT/s	Clean Clock	399.88 to 400.12	N/A (Information Only Test)
			SSC	399.88 to 400.12	N/A (Information Only Test)
	U.2 - RootComplex Tests	2.5 GT/s	Clean Clock	399.88 to 400.12	N/A (Information Only Test)
			SSC	399.88 to 400.12	N/A (Information Only Test)
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A (Not Applicable)	N/A (Not Applicable)
			SSC	N/A (Not Applicable)	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference

Table 13 Passing Limits Table for Unit Interval Test (Parameter: UI)

PCIe3.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	199.94 to 200.06	Base Spec 3.0, Table 4-18
			SSC	199.94 to 200.06	Base Spec 3.0, Table 4-18
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	For -3.5 dB: 199.94 to 200.06 For -6.0 dB: 199.94 to 200.06	For -3.5 dB: N/A (Information Only Test) For -6.0 dB: N/A (Information Only Test)
			SSC	For -3.5 dB: 199.94 to 200.06 For -6.0 dB: 199.94 to 200.06	For -3.5 dB: N/A (Information Only Test) For -6.0 dB: N/A (Information Only Test)
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	199.94 to 200.06	N/A (Information Only Test)
			SSC	199.94 to 200.06	N/A (Information Only Test)
	U.2 - EndPoint Tests	5.0 GT/s	Clean Clock	For -3.5 dB: 199.94 to 200.06 For -6.0 dB: 199.94 to 200.06	For -3.5 dB: N/A (Information Only Test) For -6.0 dB: N/A (Information Only Test)
			SSC	For -3.5 dB: 199.94 to 200.06 For -6.0 dB: 199.94 to 200.06	For -3.5 dB: N/A (Information Only Test) For -6.0 dB: N/A (Information Only Test)
	U.2 - RootComplex Tests	5.0 GT/s	Clean Clock	199.94 to 200.06	N/A (Information Only Test)
			SSC	199.94 to 200.06	N/A (Information Only Test)
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A (Not Applicable)	N/A (Not Applicable)
			SSC	N/A (Not Applicable)	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference
PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	124.9625 to 125.0375	Base Spec 3.0, Table 4-18
			SSC	124.9625 to 125.0375	Base Spec 3.0, Table 4-18
	CEM - EndPoint Tests	8.0 GT/s	Clean Clock	124.9600 to 125.0400	N/A (Information Only Test)
			SSC	124.9600 to 125.0400	N/A (Information Only Test)
	CEM - RootComplex Tests	8.0 GT/s	Clean Clock	124.9600 to 125.0400	N/A (Information Only Test)
			SSC	124.9600 to 125.0400	N/A (Information Only Test)
	U.2 - EndPoint Tests	8.0 GT/s	Clean Clock	124.9600 to 125.0400	N/A (Information Only Test)
			SSC	124.9600 to 125.0400	N/A (Information Only Test)
	U.2 - RootComplex Tests	8.0 GT/s	Clean Clock	124.9600 to 125.0400	N/A (Information Only Test)
			SSC	124.9600 to 125.0400	N/A (Information Only Test)
	Base - RefClk Tests	8.0 GT/s	Clean Clock	N/A (Not Applicable)	N/A (Not Applicable)
			SSC	N/A (Not Applicable)	N/A (Not Applicable)

Table 13 Passing Limits Table for Unit Interval Test (Parameter: UI)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference
PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	399.88 to 400.12	Base Spec 4.0, Table 8-7
			SSC	399.88 to 400.12	Base Spec 4.0, Table 8-7
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	399.88 to 400.12	N/A (Information Only Test)
			SSC	399.88 to 400.12	N/A (Information Only Test)
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	399.88 to 400.12	N/A (Information Only Test)
			SSC	399.88 to 400.12	N/A (Information Only Test)
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A (Not Applicable)	N/A (Not Applicable)
			SSC	N/A (Not Applicable)	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference
PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	199.94 to 200.06	Base Spec 4.0, Table 8-7
			SSC	199.94 to 200.06	Base Spec 4.0, Table 8-7
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	199.94 to 200.06	N/A (Information Only Test)
			SSC	199.94 to 200.06	N/A (Information Only Test)
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	199.94 to 200.06	N/A (Information Only Test)
			SSC	199.94 to 200.06	N/A (Information Only Test)
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A (Not Applicable)	N/A (Not Applicable)
			SSC	N/A (Not Applicable)	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	124.96250 to 125.03750	Base Spec 4.0, Table 8-7
			SSC	124.96250 to 125.03750	Base Spec 4.0, Table 8-7
	CEM - EndPoint Tests	8.0 GT/s	Clean Clock	124.9600 to 125.0400	N/A (Information Only Test)
			SSC	124.9600 to 125.0400	N/A (Information Only Test)
	CEM - RootComplex Tests	8.0 GT/s	Clean Clock	124.9600 to 125.0400	N/A (Information Only Test)
			SSC	124.9600 to 125.0400	N/A (Information Only Test)
	Base - RefClk Tests	8.0 GT/s	Clean Clock	N/A (Not Applicable)	N/A (Not Applicable)
			SSC	N/A (Not Applicable)	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference

Table 13 Passing Limits Table for Unit Interval Test (Parameter: UI)

PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	62.48125 to 62.51875	Base Spec 4.0, Table 8-7
			SSC	62.48125 to 62.51875	Base Spec 4.0, Table 8-7
	CEM - EndPoint Tests	16.0 GT/s	Clean Clock	62.4813 to 62.5188	N/A (Information Only Test)
			SSC	62.4813 to 62.5188	N/A (Information Only Test)
	CEM - RootComplex Tests	16.0 GT/s	Clean Clock	62.4813 to 62.5188	N/A (Information Only Test)
			SSC	62.4813 to 62.5188	N/A (Information Only Test)
	Base - RefClk Tests	16.0 GT/s	Clean Clock	N/A (Not Applicable)	N/A (Not Applicable)
			SSC	N/A (Not Applicable)	N/A (Not Applicable)

Table 14 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications
Comment	Each UI is 400 ps +/-300 ppm. UI does not account for SSC dictated variations.
Notes	No test load is necessarily associated with this value.
Section 4.3.4	Differential Receiver (RX) Input Specifications
Table 4-6	Differential Receiver (RX) Input Specifications
Comment	The UI is 400 ps +/-300 ppm. UI does not account for SSC dictated variations.
Notes	No test load is necessarily associated with this value.

Table 15 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications
Comment	Each UI is 400 ps +/-300 ppm. UI does not account for SSC dictated variations.
Notes	No test load is necessarily associated with this value.
Section 4.3.4	Differential Receiver (RX) Input Specifications
Table 4-6	Differential Receiver (RX) Input Specifications
Comment	The UI is 400 ps +/-300 ppm. UI does not account for SSC dictated variations.
Notes	No test load is necessarily associated with this value.

Table 16 PCI Express Gen 2.0 References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.3.5	Transmitter Specifications
Table 4-9	2.5 and 5.0 GT/s Transmitter Specifications
Comment	The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC induced variations.
Notes	SSC permits a +0, - 5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz.
Section 4.3.4.4	Receiver Specifications
Table 4-12	2.5 and 5.0 GT/s Receiver Specifications
Comment	UI does not account for SSC caused variations.
Notes	N/A (Not Available)

Table 17 PCI Express Gen 3.0 References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications
Comment	The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC induced variations.
Notes	SSC permits a +0, - 5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz.

Table 18 PCI Express Gen 4.0 References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters
Comment	The specified UI is equivalent to a tolerance of ±300 ppm. Does not include SSC variations.
Notes	N/A

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

.

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

Table 19 Compliance Patterns in Various Encodings

PCI Express™ Base Specification Revision 1.0a			
Section 4.2.8	Compliance Pattern	8b/10b Encoding	2.5 GT/s
PCI Express™ Base Specification Revision 1.1			
Section 4.2.8	Compliance Pattern	8b/10b Encoding	2.5 GT/s
PCI Express™ Base Specification Revision 2.0			
Section 4.2.8	Compliance Pattern	8b/10b Encoding	2.5 or 5.0 GT/s
PCI Express™ Base Specification Revision 3.0			
Section 4.2.10	Compliance Pattern	128b/130b Encoding	8.0 GT/s
Section 4.2.8	Compliance Pattern	8b/10b Encoding	2.5 or 5.0 GT/s
PCI Express™ Base Specification Revision 4.0			
Section 4.2.10	Compliance Pattern	128b/130b Encoding	8.0 or 16 GT/s
Section 4.2.8	Compliance Pattern	8b/10b Encoding	2.5 or 5.0 GT/s

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the Number of UI and
2 Sample Rate configuration parameters using Automated Test Engine.
3 Fits and displays all sample data on screen.
4 Analyzes unit interval of the test signal using the Measurement Analysis (EZJIT)... option.
   a Selects Unit Interval as data measurement analysis unit.
   b Configures the Smoothing Points to 3499 in the Measurement Trend dialog box.
5 Indicate the upper and lower limit of the measured data using markers.
6 Measures the minimum, mean, and maximum values of the UI.
7 Reports mean UI as the measurement result, and verifies that the value of UI is as per the conformance limits specified in the specific revision of PCI Express Base Specification.

Viewing Test Results

For each test trial, its result is displayed on the Results tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to Viewing Results in the online help.

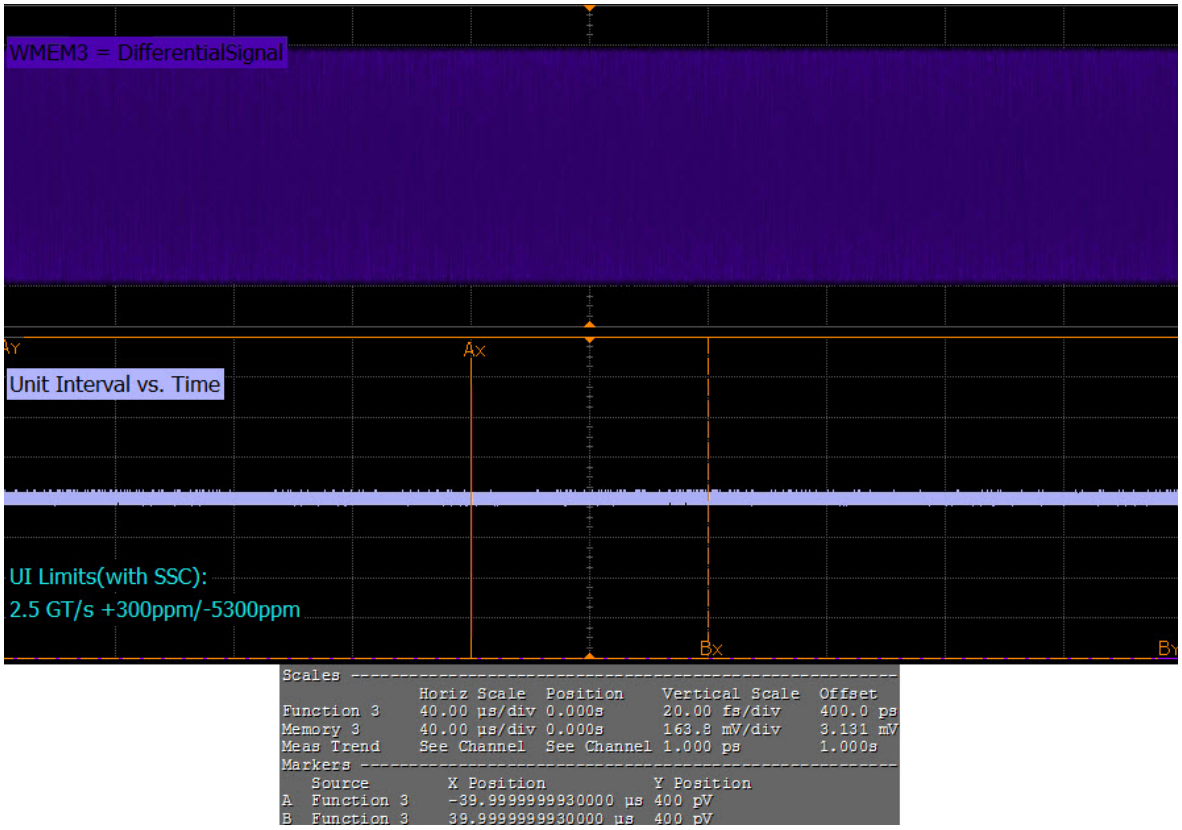


Figure 20 Reference Image for Unit Interval Test

Template Test

All PCIE devices must meet the transmitter eye diagram as specified in the PCI Express Base Specifications.

Pass Limits

Table 20 Passing Limits Table for Template Test (Parameter: $V_{TX-DIFF-PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference
PCIe1.0a	Base - Transmitter Tests	2.5 GT/s	Clean Clock	HP: Pass/Fail	High Power: N/A (Information Only Test)
				LP: Pass/Fail	Low Power: N/A (Information Only Test)
			SSC	HP: Pass/Fail	High Power: N/A (Information Only Test)
				LP: Pass/Fail	Low Power: N/A (Information Only Test)
	Base - Receiver Tests	2.5 GT/s	Clean Clock	Pass/Fail	Base Spec 1.0a, Figure 4-26
			SSC	Pass/Fail	Base Spec 1.0a, Figure 4-26
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	Pass/Fail	CEM Spec 1.0a, Table 4-6
			SSC	Pass/Fail	CEM Spec 1.0a, Table 4-6
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	Pass/Fail	CEM Spec 1.0a, Table 4-8
			SSC	Pass/Fail	CEM Spec 1.0a, Table 4-8
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference
PCIe1.1	Base - Transmitter Tests	2.5 GT/s	Clean Clock	HP: Pass/Fail	High Power: N/A (Information Only)
				LP: Pass/Fail	Low Power: N/A (Information Only)
			SSC	HP: Pass/Fail	High Power: N/A (Information Only)
				LP: Pass/Fail	Low Power: N/A (Information Only)
	Base - Receiver Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	Pass/Fail	CEM Spec 1.1, Table 4-7
			SSC	Pass/Fail	CEM Spec 1.1, Table 4-7
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	Pass/Fail	CEM Spec 1.1, Table 4-9
			SSC	Pass/Fail	CEM Spec 1.1, Table 4-9
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 20 Passing Limits Table for Template Test (Parameter: $V_{TX-DIFF-PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference
PCIe2.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	HP: Pass/Fail	High Power: N/A (Information Only)
				LP: Pass/Fail	Low Power: N/A (Information Only)
			SSC	HP: Pass/Fail	High Power: N/A (Information Only)
				LP: Pass/Fail	Low Power: N/A (Information Only)
	Base - Receiver Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	Pass/Fail	CEM Spec 2.0, Table 4-7
			SSC	Pass/Fail	CEM Spec 2.0, Table 4-7
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	Pass/Fail	CEM Spec 2.0, Table 4-14
			SSC	Pass/Fail	CEM Spec 2.0, Table 4-14
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference

Table 20 Passing Limits Table for Template Test (Parameter: $V_{TX-DIFF-PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference
PCIe2.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	HP(-3.5dB): Pass/Fail	High Power - For -3.5dB: Base Spec 2.0, Table 4-9
				HP(-6.0dB): Pass/Fail	High Power - For -6.0dB: Base Spec 2.0, Table 4-9
				LP: Pass/Fail	Low Power: Base Spec 2.0, Table 4-9
			SSC	HP(-3.5dB): Pass/Fail	High Power - For -3.5dB: Base Spec 2.0, Table 4-9
				HP(-6.0dB): Pass/Fail	High Power - For -6.0dB: Base Spec 2.0, Table 4-9
				LP: Pass/Fail	Low Power: Base Spec 3.0, Table 4-18
	Base - Receiver Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	Pass/Fail	For -3.5dB: CEM Spec 2.0, Table 4-8 For -6.0dB: CEM Spec 2.0, Table 4-10
			SSC	Pass/Fail	For -3.5dB: CEM Spec 2.0, Table 4-8 For -6.0dB: CEM Spec 2.0, Table 4-10
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	Pass/Fail	CEM Spec 2.0, Table 4-15
			SSC	Pass/Fail	CEM Spec 2.0, Table 4-15
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 20 Passing Limits Table for Template Test (Parameter: $V_{TX-DIFF-PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference
PCIe3.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	HP: Pass/Fail	High Power: N/A (Information Only)
				LP: Pass/Fail	Low Power: N/A (Information Only)
			SSC	HP: Pass/Fail	High Power: N/A (Information Only)
				LP: Pass/Fail	Low Power: N/A (Information Only)
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	Pass/Fail	CEM Spec 3.0, Table 4-6
			SSC	Pass/Fail	CEM Spec 3.0, Table 4-6
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	Pass/Fail	CEM Spec 3.0, Table 4-16
			SSC	Pass/Fail	CEM Spec 3.0, Table 4-16
	U.2 - EndPoint Tests	2.5 GT/s	Clean Clock	Pass/Fail	U.2 Spec
			SSC	Pass/Fail	U.2 Spec
	U.2 - RootComplex Tests	2.5 GT/s	Clean Clock	Pass/Fail	U.2 Spec
			SSC	Pass/Fail	U.2 Spec
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 20 Passing Limits Table for Template Test (Parameter: $V_{TX-DIFF-PP}$)

PCIe3.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	HP(-3.5dB): Pass/Fail	High Power - For -3.5dB: Base Spec 3.0, Table 4-18
				HP(-6.0dB): Pass/Fail	High Power - For -6.0dB: Base Spec 3.0, Table 4-18
				LP: Pass/Fail	Low Power: Base Spec 3.0, Table 4-18
			SSC	HP(-3.5dB): Pass/Fail	High Power - For -3.5dB: Base Spec 3.0, Table 4-18
				HP(-6.0dB): Pass/Fail	High Power - For -6.0dB: Base Spec 3.0, Table 4-18
				LP: Pass/Fail	Low Power: Base Spec 3.0, Table 4-18
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	Pass/Fail	For -3.5dB: CEM Spec 3.0, Table 4-7 For -6.0dB: CEM Spec 3.0, Table 4-9
			SSC	Pass/Fail	For -3.5dB: CEM Spec 3.0, Table 4-7 For -6.0dB: CEM Spec 3.0, Table 4-9
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	Pass/Fail	CEM Spec 3.0, Table 4-17
			SSC	Pass/Fail	CEM Spec 3.0, Table 4-17
	U.2 - EndPoint Tests	5.0 GT/s	Clean Clock	Pass/Fail	U.2 Spec (for -3.5dB) U.2 Spec (for -6.0dB)
			SSC	Pass/Fail	U.2 Spec (for -3.5dB) U.2 Spec (for -6.0dB)
	U.2 - RootComplex Tests	5.0 GT/s	Clean Clock	Pass/Fail	U.2 Spec
			SSC	Pass/Fail	U.2 Spec
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference
PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	8.0 GT/s	Clean Clock	Pass/Fail	CEM Spec 3.0, Table 4-11
			SSC	Pass/Fail	CEM Spec 3.0, Table 4-11
	CEM - RootComplex Tests	8.0 GT/s	Clean Clock	Pass/Fail	CEM Spec 3.0, Table 4-19
			SSC	Pass/Fail	CEM Spec 3.0, Table 4-19
	U.2 - EndPoint Tests	8.0 GT/s	Clean Clock	Pass/Fail	CEM Spec 3.0, Table 4-11
			SSC	Pass/Fail	CEM Spec 3.0, Table 4-11

Table 20 Passing Limits Table for Template Test (Parameter: $V_{TX-DIFF-PP}$)

	U.2 - RootComplex Tests	8.0 GT/s	Clean Clock	Pass/Fail	CEM Spec 3.0, Figure 4-14
			SSC	Pass/Fail	CEM Spec 3.0, Figure 4-14
	Base - RefClk Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference
PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	N/A	N/A (Information Only)
			SSC	N/A	N/A (Information Only)
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	Pass/Fail	CEM Spec 4.0, Figure 20, Table 11
			SSC	Pass/Fail	CEM Spec 4.0, Figure 20, Table 11
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	Pass/Fail	CEM Spec 4.0, Table 24
			SSC	Pass/Fail	CEM Spec 4.0, Table 24
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference

Table 20 Passing Limits Table for Template Test (Parameter: $V_{TX-DIFF-PP}$)

PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	HP(-3.5dB): Info Only	High Power - For -3.5dB: N/A (Information Only)
				HP(-6.0dB): Info Only	High Power - For -6.0dB: N/A (Information Only)
				LP: Info Only	Low Power: N/A (Information Only)
			SSC	HP(-3.5dB): Info Only	High Power - For -3.5dB: N/A (Information Only)
				HP(-6.0dB): Info Only	High Power - For -6.0dB: N/A (Information Only)
				LP: Info Only	Low Power: N/A (Information Only)
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	Pass/Fail	For -3.5dB: CEM Spec 4.0, Table 12, Figure 21 For -6.0dB: CEM Spec 4.0, Table 14, Figure 21
			SSC	Pass/Fail	For -3.5dB: CEM Spec 4.0, Table 12, Figure 21 For -6.0dB: CEM Spec 4.0, Table 14, Figure 21
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	Pass/Fail	CEM Spec 4.0, Table 25
			SSC	Pass/Fail	CEM Spec 4.0, Table 25
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	8.0 GT/s	Clean Clock	Pass/Fail	CEM Spec 4.0, Table 16
			SSC	Pass/Fail	CEM Spec 4.0, Table 16
	CEM - RootComplex Tests	8.0 GT/s	Clean Clock	Pass/Fail	CEM Spec 4.0, Table 27
			SSC	Pass/Fail	CEM Spec 4.0, Table 27
	Base - RefClk Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Min to Max)	Reference

Table 20 Passing Limits Table for Template Test (Parameter: $V_{TX-DIFF-PP}$)

PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	16.0 GT/s	Clean Clock	Pass/Fail	CEM Spec 4.0, Table 17
			SSC	Pass/Fail	CEM Spec 4.0, Table 17
	CEM - RootComplex Tests	16.0 GT/s	Clean Clock	Pass/Fail	CEM Spec 4.0, Table 28
			SSC	Pass/Fail	CEM Spec 4.0, Table 28
	Base - RefClk Tests	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 21 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
Section 4.3.3.1	Differential Transmitter (TX) Output Specifications
Figure 4-24	Minimum Transmitter Timing and Voltage Output Compliance Specifications
PCI Express™ Base Specification Revision 1.0a	
Section 4.3.4	Differential Receiver (RX) Input Specifications
Figure 4-26	Minimum Receiver Eye Timing and Voltage Compliance Specification
Table 4-6	Differential Receiver (RX) Input Specifications
PCI Express™ CEM Specification Revision 1.0a	
Section 4.7.1	Add-in Card Transmitter Path Compliance Eye-Diagram
Figure 4-8	Add-in Card Transmitter Path Compliance Eye Diagram
Table 4-6	Add-in Card Transmitter Path Compliance Eye Requirements
PCI Express™ CEM Specification Revision 1.0a	
Section 4.7.3	System Board Transmitter Path Compliance Eye Diagram
Figure 4-10	System Board Transmitter Path Composite Compliance Eye Diagram
Table 4-8	System Board Transmitter Path Compliance Eye Requirements

Table 22 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
Section 4.3.3.1	Transmitter Compliance Eye Diagrams
Figure 4-24	Minimum Transmitter Timing and Voltage Output Compliance Specifications
PCI Express™ CEM Specification Revision 1.1	
Section 4.7.1	Add-in Card Transmitter Path Compliance Eye-Diagram
Figure 4-8	Add-in Card Transmitter Path Compliance Eye Diagram
Table 4-7	Add-in Card Transmitter Path Compliance Eye Requirements
PCI Express™ CEM Specification Revision 1.1	
Section 4.7.3	System Board Transmitter Path Compliance Eye Diagram
Figure 4-10	System Board Transmitter Path Composite Compliance Eye Diagram
Table 4-9	System Board Transmitter Path Compliance Eye Requirements

Table 23 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
Section 4.3.3.1	Transmitter Compliance Eye Diagrams
Figure 4-24	Minimum Transmitter Timing and Voltage Output Compliance Specifications
PCI Express™ Base Specification Revision 1.1	
Section 4.3.4	Differential Receiver (RX) Input Specifications
Figure 4-26	Minimum Receiver Eye Timing and Voltage Compliance Specification
PCI Express™ CEM Specification Revision 2.0	
Section 4.7.1	Add-in Card Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 4-7	Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s
PCI Express™ CEM Specification Revision 2.0	
Section 4.7.5	System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 4-14	System Board Transmitter Path Compliance Eye Requirements 2.5 GT/s

Table 24 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.3.5	Transmitter Specification
Table 4-9	2.5 and 5.0 GT/s Transmitter Specifications
PCI Express™ CEM Specification Revision 2.0	

Table 24 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

Section 4.7.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5 GT/s
Figure 4-7	Add-in Card Transmitter Path Compliance Eye Diagram
Table 4-8	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s and 3.5 dB De-emphasis
Table 4-10	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s at 6.0 dB De-emphasis
PCI Express™ CEM Specification Revision 2.0	
Section 4.7.6	System Board Transmitter Path Compliance Eye Diagram at 5 GT/s
Figure 4-12	System Board Transmitter Path Composite Compliance Eye Diagram
Table 4-15	System Board Transmitter Path Compliance Eye Requirements at 5 GT/s

Table 25 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base and CEM Specification Revision 1.1	
Please refer to Table 23, “PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes,”.	
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.1	Add-in Card Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 4-6	Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.7	System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 4-16	System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s

Table 26 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications
PCI Express™ CEM Specification Revision 2.0	
Section 4.7.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5 GT/s
Figure 4-7	Add-in Card Transmitter Path Compliance Eye Diagram
Table 4-8	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s and 3.5 dB De-emphasis
Table 4-10	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s at 6.0 dB De-emphasis
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.8	System Board Transmitter Path Compliance Eye Diagram at 5.0 GT/s
Figure 4-12	System Board Transmitter Path Composite Compliance Eye Diagram
Table 4-17	System Board Transmitter Path Compliance Eye Requirements at 5.0 GT/s

Table 27 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
Section 4.8.3	Add-in Card Transmitter Path Compliance Eye Diagrams at 8.0 GT/s
Table 4-11	Add-in Card Transmitter Path Compliance Eye Requirements at 8.0 GT/s
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.9	System Board Transmitter Path Compliance Eye Diagram at 8.0 GT/s
Figure 4-14	System Board Transmitter Path Composite Compliance Eye Diagram
Table 4-19	System Board Transmitter Path Compliance Eye Requirements at 8.0 GT/s with Ideal Adaptive TX Equalization

Table 28 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base and CEM Specification Revision 1.1	
Please refer to Table 23, “PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes,”.	
PCI Express™ BASE Specification Revision 4.0	
Section 4.8.1	Add-in Card Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Figure 20	2.5 GT/s Add-in Card Transmitter Path Compliance Eye Diagram
Table 24	Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.1	Add-in Card Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Figure 20	2.5 GT/s Add-in Card Transmitter Path Compliance Eye Diagram
Table 11	Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.10	System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 24	System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s

Table 29 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
Section 4.8.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5.0 GT/s
Table 12	Add-in Card Transmitter Path Compliance Eye Requirements at 5.0 GT/s and 3.5 dB De-emphasis
Figure 21	5.0 GT/s Add-in Card Transmitter Path Compliance Eye Diagram
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5.0 GT/s
Table 14	Add-in Card Transmitter Path Compliance Eye Requirements at 5.0 GT/s at 6.0 dB De-emphasis
Figure 21	5.0 GT/s Add-in Card Transmitter Path Compliance Eye Diagram

Table 29 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
Section 4.8.11	System Board Transmitter Path Compliance Eye Diagram at 5.0 GT/s
Table 25	System Board Transmitter Path Compliance Eye Requirements at 5.0 GT/s

Table 30 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
Section 4.8.3	Add-in Card Transmitter Path Compliance Eye Diagrams at 8.0 GT/s
Table 16	Add-in Card Transmitter Path Compliance Eye Requirements at 8.0 GT/s
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.12	System Board Transmitter Path Compliance Eye Diagram at 8.0 GT/s
Table 27	System Board Transmitter Path Compliance Eye Requirements at 8.0 GT/s with Ideal Adaptive TX Equalization

Table 31 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
Section 4.8.4	Add-in Card Transmitter Path Compliance Eye Diagrams at 16.0 GT/s
Table 17	Add-in Card Transmitter Path Compliance Eye Requirements at 16.0 GT/s
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.13	System Board Transmitter Path Compliance Eye Diagram at 16.0 GT/s
Table 28	System Board Transmitter Path Compliance Eye Requirements at 16.0 GT/s with Ideal Adaptive TX Equalization

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTest tools.

   a Calls the add-in card compliance test function from the SigTest tools.

   b Gets transition failure and non-transition failure test results from the SigTest tools.

3 Identifies mask failures using SigTest.exe, and reports the results as Pass or Fail. In addition, also generates both the transition and non-transition eye diagrams.

4 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the respective PCI Express Specification and the total number of mask violations is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

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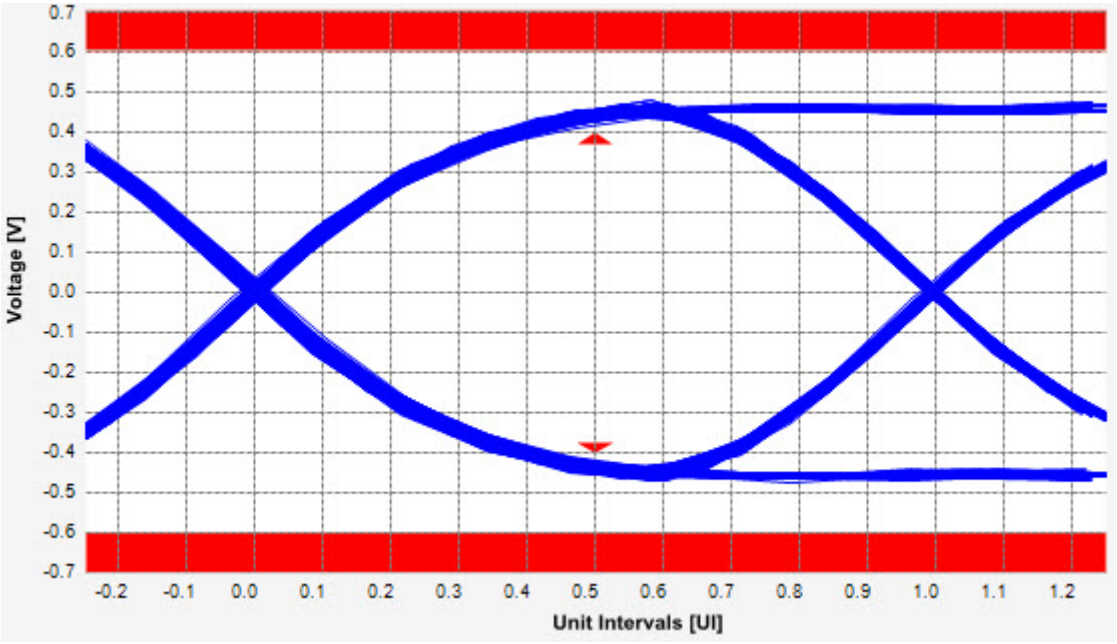


Figure 21 Reference Image for Template (Transition) Test

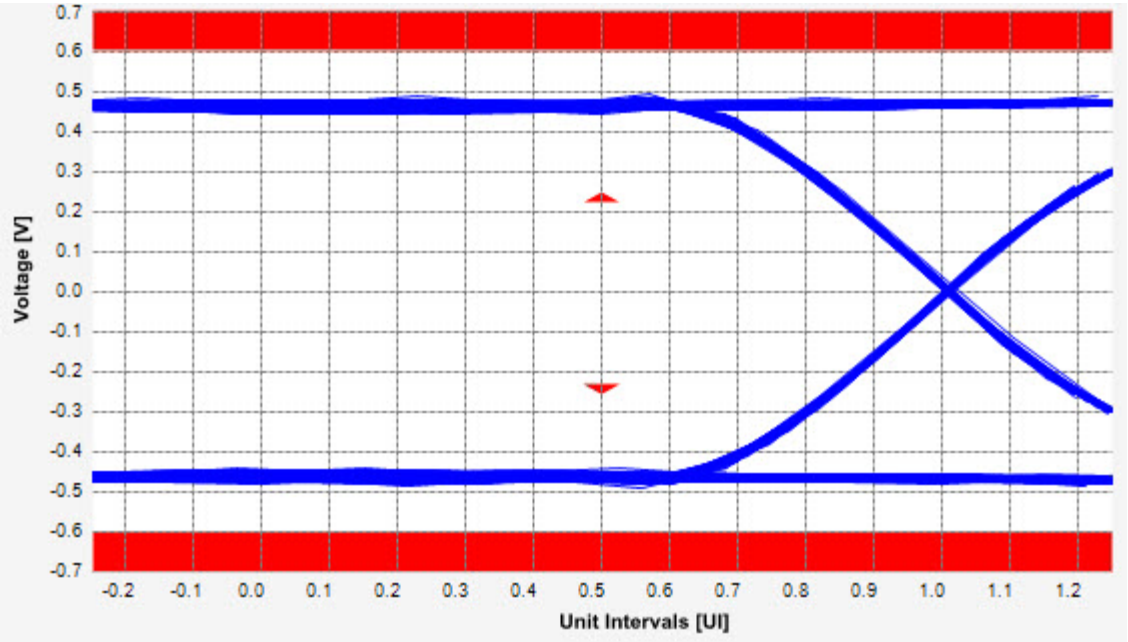


Figure 22 Reference Image for Template (Non-transition) Test

Median to Max Jitter Test

Jitter is defined as the measurement variation of the crossing points (VTX-DIFFp-p = 0 V) in relation to the recovered TX UI. The purpose of this test is to measure the median to max jitter between the jitter median and max deviation from the median.

Pass Limits

Table 32 Passing Limits Table for Median to Max Jitter Test (Parameter: $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits Max (ps)	Reference
PCIe1.0a	Base - Transmitter Tests	2.5 GT/s	Clean Clock	HP: 150.00 mUI	High Power: Base Spec 1.0a, Table 4-5
				LP: 150.00 mUI	Low Power: Base Spec 1.0a, Table 4-5
			SSC	HP: 150.00 mUI	High Power: Base Spec 1.0a, Table 4-5
				LP: 150.00 mUI	Low Power: Base Spec 1.0a, Table 4-5
	Base - Receiver Tests	2.5 GT/s	Clean Clock	300.00 mUI	Base Spec 1.0a, Table 4-6
			SSC	300.00 mUI	Base Spec 1.0a, Table 4-6
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	118.50	CEM Spec 1.0a, Table 4-6
			SSC	118.50	CEM Spec 1.0a, Table 4-6
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	91.5	CEM Spec 1.0a, Table 4-8
			SSC	91.5	CEM Spec 1.0a, Table 4-8
Device	Test Point	Data Rate	Ref. Clock	Pass Limits Max (ps)	Reference
PCIe1.1	Base - Transmitter Tests	2.5 GT/s	Clean Clock	HP: 125.00 mUI	High Power: Base Spec 1.1, Table 4-5
				LP: 125.00 mUI	Low Power: Base Spec 1.1, Table 4-5
			SSC	HP: 125.00 mUI	High Power: Base Spec 1.1, Table 4-5
				LP: 125.00 mUI	Low Power: Base Spec 1.1, Table 4-5
	Base - Receiver Tests	2.5 GT/s	Clean Clock	300.00 mUI	Base Spec 1.1, Table 4-6
			SSC	300.00 mUI	Base Spec 1.1, Table 4-6
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	56.50	CEM Spec 1.1, Table 4-7
			SSC	56.50	CEM Spec 1.1, Table 4-7
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	77.00	CEM Spec 1.1, Table 4-9
			SSC	77.00	CEM Spec 1.1, Table 4-9

Table 32 Passing Limits Table for Median to Max Jitter Test (Parameter: $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$)

	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits Max (ps)	Reference
PCIe2.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	HP: 125.00 mUI	High Power: Base Spec 1.1, Table 4-5
				LP: 125.00 mUI	Low Power: Base Spec 1.1, Table 4-5
			SSC	HP: 125.00 mUI	High Power: Base Spec 1.1, Table 4-5
				LP: 125.00 mUI	Low Power: Base Spec 1.1, Table 4-5
	Base - Receiver Tests	2.5 GT/s	Clean Clock	300.00 mUI	Base Spec 1.1, Table 4-6
			SSC	300.00 mUI	Base Spec 1.1, Table 4-6
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	56.50	CEM Spec 2.0, Table 4-7
			SSC	56.50	CEM Spec 2.0, Table 4-7
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	77.00	CEM Spec 2.0, Table 4-14
			SSC	77.00	CEM Spec 2.0, Table 4-14
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits Max (ps)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits Max (ps)	Reference

Table 32 Passing Limits Table for Median to Max Jitter Test (Parameter: $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$)

PCIe3.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	HP: 125.00 mUI	High Power: Base Spec 1.1, Table 4-5
				LP: 125.00 mUI	Low Power: Base Spec 1.1, Table 4-5
			SSC	HP: 125.00 mUI	High Power: Base Spec 1.1, Table 4-5
				LP: 125.00 mUI	Low Power: Base Spec 1.1, Table 4-5
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	56.50	CEM Spec 3.0, Table 4-6
			SSC	56.50	CEM Spec 3.0, Table 4-6
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	77.00	CEM Spec 3.0, Table 4-16
			SSC	77.00	CEM Spec 3.0, Table 4-16
	U.2 - EndPoint Tests	2.5 GT/s	Clean Clock	56.50	U.2 Spec
			SSC	56.50	U.2 Spec
	U.2 - RootComplex Tests	2.5 GT/s	Clean Clock	77.00	U.2 Spec
			SSC	77.00	U.2 Spec
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits Max (ps)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits Max (ps)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits Max (ps)	Reference
PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	N/A	N/A (Information Only)
			SSC	N/A	N/A (Information Only)
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	56.50	CEM Spec 4.0, Table 11
			SSC	56.50	CEM Spec 4.0, Table 11
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	77.00	CEM Spec 4.0, Table 24
			SSC	77.00	CEM Spec 4.0, Table 24
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits Max (ps)	Reference

Table 32 Passing Limits Table for Median to Max Jitter Test (Parameter: $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$)

PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits Max (ps)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits Max (ps)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 33 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
Section 4.3.3.1	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications
Comments	The specified UI is equivalent to a tolerance of ±300 ppm. Does not include SSC variations.
Notes	N/A
PCI Express™ Base Specification Revision 1.0a	
Section 4.3.4	Differential Receiver (RX) Input Specifications
Figure 4-26	Minimum Receiver Eye Timing and Voltage Compliance Specification
Table 4-6	Differential Receiver (RX) Input Specifications
Comments	Jitter is defined as the measurement variation of the crossing points (VRXDIFFp-p = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.
Notes	Notes 7 and 8; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 1.0a	
Section 4.7.1	Add-in Card Transmitter Path Compliance Eye-Diagram
Table 4-6	Add-in Card Transmitter Path Compliance Eye Requirements
Comments	All Links are assumed active while generating this eye diagram. Transition and non transition bits must be distinguished in order to measure compliance against the deemphasized voltage level (V_{txA_d}).
Notes	For more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 1.0a	
Section 4.7.3	System Board Transmitter Path Compliance Eye Diagram

Table 33 PCI Express Gen 1.0a References and Specification Notes

Table 4-8	System Board Transmitter Path Compliance Eye Requirements
Comments	All Links are assumed active while generating this eye diagram. Transition and non transition bits must be distinguished in order to measure compliance against the deemphasized voltage level (V_{txs_d}).
Notes	For more info, please visit the chapter “Specification Notes” on page 527.

Table 34 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications
Comments	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFF}$ = 0 V) in relation to recovered TX UI. To be measured after the clock recovery function in Section 4.3.3.2.
Notes	Notes 2 and 3; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ Base Specification Revision 1.1	
Section 4.3.4	Differential Receiver (RX) Input Specifications
Table 4-6	Differential Receiver (RX) Input Specifications
Comments	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to recovered TX UI. To be measured after the clock recovery function in Section 4.3.3.2.
Notes	Notes 8 and 9; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 1.1	
Section 4.7.1	Add-in Card Transmitter Path Compliance Eye-Diagram
Table 4-7	Add-in Card Transmitter Path Compliance Eye Requirements
Comments	N/A
Notes	Notes 1, 4, and 5; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 1.1	
Section 4.7.3	System Board Transmitter Path Compliance Eye Diagram
Table 4-9	System Board Transmitter Path Compliance Eye Requirements
Comments	
Notes	Notes 1, 4, and 5; for more info, please visit the chapter “Specification Notes” on page 527.

Table 35 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base and CEM Specification Revision 1.1	
Please refer to Table 34, “PCI Express Gen 1.1 References and Specification Notes,”.	
PCI Express™ CEM Specification Revision 2.0	
Section 4.7.1	Add-in Card Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 4-7	Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Comments	N/A
Notes	Notes 1, 4, and 5; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 2.0	
Section 4.7.5	System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s

Table 35 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

Table 4-14	System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Comments	
Notes	Notes 1, 4, and 5; for more info, please visit the chapter “Specification Notes” on page 527.

Table 36 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base and CEM Specification Revision 1.1	
Please refer to Table 34, “PCI Express Gen 1.1 References and Specification Notes,”.	
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.1	Add-in Card Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 4-6	Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Notes	Notes 1, 4, and 5; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.7	System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 4-16	System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Comments	
Notes	Notes 1, 4, and 5; for more info, please visit the chapter “Specification Notes” on page 527.

Table 37 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ CEM Specification Revision 1.1	
Please refer to Table 34, “PCI Express Gen 1.1 References and Specification Notes,”.	
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.1	Add-in Card Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 11	Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Notes	Notes 1, 4, and 5; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.10	System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 24	System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Comments	
Notes	Notes 1, 4, and 5; for more info, please visit the chapter “Specification Notes” on page 527.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test.

1 Obtains the value for the maximum peak to peak jitter after filter parameter from the SigTest tools.

2 Computes the median to max jitter using the following formula:

$$\text{Median to max jitter} = \text{Maximum peak to peak jitter after filter} / 2$$

3 Reports the median to max jitter as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER - 12]$$

Pass Limits

Table 38 Passing Limits Table for Eye-Width Test (Parameter: T_{TX-EYE})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe1.0a	Base - Transmitter Tests	2.5 GT/s	Clean Clock	HP: 700 mUI LP: 700 mUI	High Power: Base Spec 1.0a, Table 4-5 Low Power: Base Spec 1.0a, Table 4-5
			SSC	HP: 700 mUI LP: 700 mUI	High Power: Base Spec 1.0a, Table 4-5 Low Power: Base Spec 1.0a, Table 4-5
	Base - Receiver Tests	2.5 GT/s	Clean Clock	400 mUI	Base Spec 1.0a, Table 4-6
			SSC	400 mUI	Base Spec 1.0a, Table 4-6
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	237.00 ps	CEM Spec 1.0a, Table 4-6
			SSC	237.00 ps	CEM Spec 1.0a, Table 4-6
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	183.00 ps	CEM Spec 1.0a, Table 4-8
			SSC	183.00 ps	CEM Spec 1.0a, Table 4-8
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe1.1	Base - Transmitter Tests	2.5 GT/s	Clean Clock	HP: 750 mUI LP: 750 mUI	High Power: Base Spec 1.1, Table 4-5 Low Power: Base Spec 1.1, Table 4-5
			SSC	HP: 750 mUI LP: 750 mUI	High Power: Base Spec 1.1, Table 4-5 Low Power: Base Spec 1.1, Table 4-5
	Base - Receiver Tests	2.5 GT/s	Clean Clock	400 mUI	Base Spec 1.1, Table 4-6
			SSC	400 mUI	Base Spec 1.1, Table 4-6
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	287.00 ps	CEM Spec 1.1, Table 4-7
			SSC	287.00 ps	CEM Spec 1.1, Table 4-7
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	246.00 ps	CEM Spec 1.1, Table 4-9
			SSC	246.00 ps	CEM Spec 1.1, Table 4-9

Table 38 Passing Limits Table for Eye-Width Test (Parameter: T_{TX-EYE})

	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe2.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	HP: 750 mUI	High Power: Base Spec 2.0, Table 4-9
				LP: 750 mUI	Low Power: Base Spec 2.0, Table 4-9
			SSC	HP: 750 mUI	High Power: Base Spec 2.0, Table 4-9
				LP: 750 mUI	Low Power: Base Spec 2.0, Table 4-9
	Base - Receiver Tests	2.5 GT/s	Clean Clock	400 mUI	Base Spec 2.0, Table 4-12
			SSC	400 mUI	Base Spec 2.0, Table 4-12
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	287.00 ps	CEM Spec 2.0, Table 4-7
			SSC	287.00 ps	CEM Spec 2.0, Table 4-7
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	246.00 ps	CEM Spec 2.0, Table 4-14
			SSC	246.00 ps	CEM Spec 2.0, Table 4-14
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference

Table 38 Passing Limits Table for Eye-Width Test (Parameter: T_{TX-EYE})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe2.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	750 mUI	Base Spec 2.0, Table 4-9
			SSC	750 mUI	Base Spec 2.0, Table 4-9
	Base - Receiver Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	123.00 ps	For -3.5dB with cross talk: CEM Spec 2.0, Table 4-8
				126.00 ps	For -3.5dB without cross talk: CEM Spec 2.0, Table 4-8
				123.00 ps	For -6.0dB with cross talk: CEM Spec 2.0, Table 4-10
				126.00 ps	For -6.0dB without cross talk: CEM Spec 2.0, Table 4-10
			SSC	123.00 ps	For -3.5dB with cross talk: CEM Spec 2.0, Table 4-8
				126.00 ps	For -3.5dB without cross talk: CEM Spec 2.0, Table 4-8
				123.00 ps	For -6.0dB with cross talk: CEM Spec 2.0, Table 4-10
				126.00 ps	For -6.0dB without cross talk: CEM Spec 2.0, Table 4-10
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	95.00 ps	With cross talk: CEM Spec 2.0, Table 4-15
				108.00 ps	Without cross talk: CEM Spec 2.0, Table 4-15
			SSC	95.00 ps	With cross talk: CEM Spec 2.0, Table 4-15
				108.00 ps	Without cross talk: CEM Spec 2.0, Table 4-15
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 38 Passing Limits Table for Eye-Width Test (Parameter: T_{TX-EYE})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe3.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	HP: 750.00 mUI	High Power: Base Spec 3.0, Table 4-18
				LP: 750.00 mUI	Low Power: Base Spec 3.0, Table 4-18
			SSC	HP: 750.00 mUI	High Power: Base Spec 3.0, Table 4-18
				LP: 750.00 mUI	Low Power: Base Spec 3.0, Table 4-18
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	287.00 ps	CEM Spec 3.0, Table 4-6
			SSC	287.00 ps	CEM Spec 3.0, Table 4-6
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	246.00 ps	CEM Spec 3.0, Table 4-16
			SSC	246.00 ps	CEM Spec 3.0, Table 4-16
	U.2 - EndPoint Tests	2.5 GT/s	Clean Clock	287.00 ps	U.2 Spec
			SSC	287.00 ps	U.2 Spec
	U.2 - RootComplex Tests	2.5 GT/s	Clean Clock	246.00 ps	U.2 Spec
			SSC	246.00 ps	U.2 Spec
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 38 Passing Limits Table for Eye-Width Test (Parameter: T_{TX-EYE})

PCIe3.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	750.00 mUI	For -3.5dB: Base Spec 3.0, Table 4-18
				750.00 mUI	For -6.0dB: Base Spec 3.0, Table 4-18
			SSC	750.00 mUI	For -3.5dB: Base Spec 3.0, Table 4-18
				750.00 mUI	For -6.0dB: Base Spec 3.0, Table 4-18
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	123.00 ps	For -3.5dB with cross talk: CEM Spec 3.0, Table 4-7
				126.00 ps	For -3.5dB without cross talk: CEM Spec 3.0, Table 4-7
				123.00 ps	For -6.0dB with cross talk: CEM Spec 3.0, Table 4-9
				126.00 ps	For -6.0dB without cross talk: CEM Spec 3.0, Table 4-9
			SSC	123.00 ps	For -3.5dB with cross talk: CEM Spec 3.0, Table 4-7
				126.00 ps	For -3.5dB without cross talk: CEM Spec 3.0, Table 4-7
				123.00 ps	For -6.0dB with cross talk: CEM Spec 3.0, Table 4-9
				126.00 ps	For -6.0dB without cross talk: CEM Spec 3.0, Table 4-9
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	95.00 ps	With Crosstalk: CEM Spec 3.0, Table 4-17
				108.00 ps	Without Crosstalk: CEM Spec 3.0, Table 4-17
			SSC	95.00 ps	With Crosstalk: CEM Spec 3.0, Table 4-17
				108.00 ps	Without Crosstalk: CEM Spec 3.0, Table 4-17
	U.2 - EndPoint Tests	5.0 GT/s	Clean Clock	123.00 ps	For -3.5dB with Crosstalk: U.2 Spec
				126.00 ps	For -3.5dB without Crosstalk: U.2 Spec
			SSC	123.00 ps	For -3.5dB with Crosstalk: U.2 Spec
				126.00 ps	For -3.5dB without Crosstalk: U.2 Spec

Table 38 Passing Limits Table for Eye-Width Test (Parameter: T_{TX-EYE})

	U.2 - RootComplex Tests	5.0 GT/s	Clean Clock	95.00 ps	With Crosstalk: U.2 Spec
				108.00 ps	Without Crosstalk: U.2 Spec
			SSC	95.00 ps	With Crosstalk: U.2 Spec
				108.00 ps	Without Crosstalk: U.2 Spec
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	8.0 GT/s	Clean Clock	41.250 ps	CEM Spec 3.0, Table 4-11
			SSC	41.250 ps	CEM Spec 3.0, Table 4-11
	CEM - RootComplex Tests	8.0 GT/s	Clean Clock	41.25 ps	CEM Spec 3.0, Figure 4-14, Table 4-19
			SSC	41.25 ps	CEM Spec 3.0, Figure 4-14, Table 4-19
	U.2 - EndPoint Tests	8.0 GT/s	Clean Clock	41.250 ps	CEM Spec 3.0, Table 4-11
			SSC	41.250 ps	CEM Spec 3.0, Table 4-11
	U.2 - RootComplex Tests	8.0 GT/s	Clean Clock	41.25 ps	CEM Spec 3.0, Figure 4-14, Table 4-19
			SSC	41.25 ps	CEM Spec 3.0, Figure 4-14, Table 4-19
	Base - RefClk Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference

Table 38 Passing Limits Table for Eye-Width Test (Parameter: T_{TX-EYE})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	HP: N/A	High Power: Base Spec 4.0 (Information Only Test)
				LP: N/A	Low Power: Base Spec 4.0 (Information Only Test)
			SSC	HP: N/A	High Power: Base Spec 4.0 (Information Only Test)
				LP: N/A	Low Power: Base Spec 4.0 (Information Only Test)
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	287.00 ps	CEM Spec 4.0, Table 11
			SSC	287.00 ps	CEM Spec 4.0, Table 11
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	246.00 ps	CEM Spec 4.0, Table 24
			SSC	246.00 ps	CEM Spec 4.0, Table 24
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 38 Passing Limits Table for Eye-Width Test (Parameter: T_{TX-EYE})

PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	HP: N/A	High Power: Base Spec 4.0 (Information Only Test)
				LP: N/A	Low Power: Base Spec 4.0 (Information Only Test)
			SSC	HP: N/A	High Power: Base Spec 4.0 (Information Only Test)
				LP: N/A	Low Power: Base Spec 4.0 (Information Only Test)
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	123.00 ps	For -3.5dB with cross talk: CEM Spec 3.0, Table 12
				126.00 ps	For -3.5dB without cross talk: CEM Spec 3.0, Table 12
				123.00 ps	For -6.0dB with cross talk: CEM Spec 3.0, Table 14
				126.00 ps	For -6.0dB without cross talk: CEM Spec 3.0, Table 14
			SSC	123.00 ps	For -3.5dB with cross talk: CEM Spec 3.0, Table 12
				126.00 ps	For -3.5dB without cross talk: CEM Spec 3.0, Table 12
				123.00 ps	For -6.0dB with cross talk: CEM Spec 3.0, Table 14
				126.00 ps	For -6.0dB without cross talk: CEM Spec 3.0, Table 14
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	95.00 ps	With Crosstalk: CEM Spec 4.0, Table 25
				108.00 ps	Without Crosstalk: CEM Spec 4.0, Table 25
			SSC	95.00 ps	With Crosstalk: CEM Spec 4.0, Table 25
				108.00 ps	Without Crosstalk: CEM Spec 4.0, Table 25
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	8.0 GT/s	Clean Clock	41.250 ps	CEM Spec 4.0, Table 16
			SSC	41.250 ps	CEM Spec 4.0, Table 16
	CEM - RootComplex Tests	8.0 GT/s	Clean Clock	41.25 ps	CEM Spec 4.0, Table 27
			SSC	41.25 ps	CEM Spec 4.0, Table 27
	Base - RefClk Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 38 Passing Limits Table for Eye-Width Test (Parameter: T_{TX-EYE})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	16.0 GT/s	Clean Clock	24.750 ps	CEM Spec 4.0, Table 17
			SSC	24.750 ps	CEM Spec 4.0, Table 17
	CEM - RootComplex Tests	16.0 GT/s	Clean Clock	21.750 ps	CEM Spec 4.0, Table 28
			SSC	21.750 ps	CEM Spec 4.0, Table 28
	Base - RefClk Tests	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

NOTE U.2 Root Complex, Eye Width Test requires Root Complex Template Test.

Table 39 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications
Comments	The maximum Transmitter jitter can be derived as $T_{TXMAX-JITTER}$ = 1 - T_{TX-EYE}= .3 UI
Notes	Notes 2 and 3; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ Base Specification Revision 1.0a	
Section 4.3.4	Differential Receiver (RX) Input Specifications
Table 4-6	Differential Receiver (RX) Input Specifications
Comments	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 - T_{RX-EYE}=0.6 UI
Notes	Notes 7 and 8; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 1.0a	
Section 4.7.1	Add-in Card Transmitter Path Compliance Eye-Diagram
Table 4-6	Add-in Card Transmitter Path Compliance Eye Requirements
Comments	All Links are assumed active while generating this eye diagram. Transition and nontransition bits must be distinguished in order to measure compliance against the deemphasized voltage level (V_{txA_d}).
Notes	For more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 1.0a	
Section 4.7.3	System Board Transmitter Path Compliance Eye Diagram

Table 39 PCI Express Gen 1.0a References and Specification Notes

Table 4-8	System Board Transmitter Path Compliance Eye Requirements
Comments	All Links are assumed active while generating this eye diagram. Transition and nontransition bits must be distinguished in orderto measure compliance against the deemphasized voltage level (T_{txS_d}).
Notes	For more info, please visit the chapter “Specification Notes” on page 527.

Table 40 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications
Comments	The maximum Transmitter jitter can be derived as $T_{TX\text{-}MAX\text{-}JITTER}$ = 1 - $T_{TX\text{-}EYE}$ = 0.25 UI. This parameter is measured with the equivalent of a zero jitter reference clock.
Notes	Notes 2 and 3; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ Base Specification Revision 1.1	
Section 4.3.4	Differential Receiver (RX) Input Specifications
Table 4-6	Differential Receiver (RX) Input Specifications
Comments	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX\text{-}MAX\text{-}JITTER}$ = 1 - $T_{RX\text{-}EYE}$ = 0.6 UI.
Notes	Notes 8, 9, and 10; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 1.1	
Section 4.7.1	Add-in Card Transmitter Path Compliance Eye-Diagram
Table 4-7	Add-in Card Transmitter Path Compliance Eye Requirements
Comments	N/A
Notes	Notes 1, 3, and 5; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 1.1	
Section 4.7.3	System Board Transmitter Path Compliance Eye Diagram
Table 4-9	System Board Transmitter Path Compliance Eye Requirements
Comments	N/A
Notes	Notes 1, 3, and 5; for more info, please visit the chapter “Specification Notes” on page 527.

Table 41 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base and CEM Specification Revision 1.1	
Please refer to Table 40, “PCI Express Gen 1.1 References and Specification Notes,”.	
PCI Express™ Base Specification Revision 2.0	
Section 4.3.4.4	Receiver Specifications
Table 4-12	2.5 and 5.0 GT/s Receiver Specifications
Comments	Minimum eye time at Rx pins to yield a 10^{-12} BER.
Notes	Notes 1; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ Base Specification Revision 2.0	
Section 4.3.3.5	Transmitter Specification
Table 4-9	2.5 and 5.0 GT/s Transmitter Specifications

Table 41 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

Comments	Does not include SSC or Refclk jitter. Includes Rj at 10^{-12}. See Notes 2, 3, 4, and 10. Note that 2.5 GT/s and 5.0 GT/s use different jitter determination methods.
Notes	Notes 2, 3, 4, and 10; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 2.0	
Section 4.7.1	Add-in Card Transmitter Path Compliance Eye-Diagram at 2.5 GT/s
Table 4-7	Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Comments	N/A
Notes	Notes 1, 3, and 5; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 2.0	
Section 4.7.5	System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 4-14	System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Comments	N/A
Notes	Notes 1, 3, and 5; for more info, please visit the chapter “Specification Notes” on page 527.

Table 42 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications
Comments	Does not include SSC or Refclk jitter. Includes Rj at 10^{-12}. Note that 2.5 GT/s and 5.0 GT/s use different jitter determination methods.
Notes	Notes 2, 3, 4, and 10; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 2.0	
Section 4.7.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5 GT/s
Table 4-8	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s and 3.5 dB De-emphasis
Comments	N/A
Notes	With cross talk: Notes 1, 3, and 4; for more info, please visit the chapter “Specification Notes” on page 527. Without cross talk: N/A
Table 4-10	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s and 6.0 dB De-emphasis
Comments	N/A
Notes	With cross talk: Notes 1, 3, and 4; for more info, please visit the chapter “Specification Notes” on page 527. Without cross talk: N/A
PCI Express™ CEM Specification Revision 2.0	
Section 4.7.6	System Board Transmitter Path Compliance Eye Diagram at 5 GT/s

Table 42 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

Table 4-15	System Board Transmitter Path Compliance Eye Requirements at 5 GT/s
Comments	N/A
Notes	With cross talk: Notes 1, 3, and 4; for more info, please visit the chapter “Specification Notes” on page 527. Without cross talk: N/A

Table 43 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base and CEM Specification Revision 1.1	
Please refer to Table 40, “PCI Express Gen 1.1 References and Specification Notes,”.	
PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications
Comments	Does not include SSC or Refclk jitter. Includes Rj at 10^{-12}. Note that 2.5 GT/s and 5.0 GT/s use different jitter determination methods.
Notes	Notes 2, 3, 4, and 10; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.1	Add-in Card Transmitter Path Compliance Eye-Diagram at 2.5 GT/s
Table 4-6	Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Comments	N/A
Notes	Notes 1, 3, and 5; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.7	System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 4-16	System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Comments	N/A
Notes	With cross talk: Notes 1, 3, and 5; for more info, please visit the chapter “Specification Notes” on page 527. Without cross talk: N/A

Table 44 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
Please refer to Table 42, "PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes,".	
PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications
Comments	Does not include SSC or Refclk jitter. Includes Rj at 10^{-12}. Note that 2.5 GT/s and 5.0 GT/s use different jitter determination methods.
Notes	Notes 2, 3, 4, and 10; for more info, please visit the chapter "Specification Notes" on page 527.
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5 GT/s
Table 4-7	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s and 3.5 dB De-emphasis
Comments	N/A
Notes	With cross talk: Notes 1, 3, and 4; for more info, please visit the chapter "Specification Notes" on page 527. Without cross talk: N/A
Table 4-9	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s and 6.0 dB De-emphasis
Comments	N/A
Notes	With cross talk: Notes 1, 3, and 4; for more info, please visit the chapter "Specification Notes" on page 527. Without cross talk: N/A
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.8	System Board Transmitter Path Compliance Eye Diagram at 5.0 GT/s
Table 4-17	System Board Transmitter Path Compliance Eye Requirements at 5.0 GT/s
Comments	N/A
Notes	With cross talk: Notes 1, 3, and 4; for more info, please visit the chapter "Specification Notes" on page 527. Without cross talk: N/A

Table 45 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
Section 4.8.3	Add-in Card Transmitter Path Compliance Eye Diagrams at 8.0 GT/s
Table 4-11	Add-in Card Transmitter Path Compliance Eye Requirements at 8.0 GT/s
Comments	N/A
Notes	1, 3, and 4; for more info, please visit the chapter "Specification Notes" on page 527.
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.9	System Board Transmitter Path Compliance Eye Diagram at 8.0 GT/s
Table 4-19	System Board Transmitter Path Compliance Eye Requirements at 8.0 GT/s with Ideal Adaptive TX Equalization
Comments	N/A
Notes	1, 3, and 4; for more info, please visit the chapter "Specification Notes" on page 527.

Table 46 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base and CEM Specification Revision 1.1	
Please refer to Table 40, "PCI Express Gen 1.1 References and Specification Notes,".	
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.1	Add-in Card Transmitter Path Compliance Eye-Diagram at 2.5 GT/s
Table 11	Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Comments	N/A
Notes	Notes 1, 3, and 5; for more info, please visit the chapter "Specification Notes" on page 527.
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.10	System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 24	System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Comments	N/A
Notes	1, 3, and 5; for more info, please visit the chapter "Specification Notes" on page 527.

Table 47 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
Section 4.8.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5 GT/s
Table 12	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s and 3.5 dB De-emphasis
Comments	N/A
Notes	With cross talk: Notes 1, 3, and 4; for more info, please visit the chapter "Specification Notes" on page 527. Without cross talk: N/A
Table 14	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s and 6.0 dB De-emphasis
Comments	N/A
Notes	With cross talk: Notes 1, 3, and 4; for more info, please visit the chapter "Specification Notes" on page 527. Without cross talk: N/A
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.11	System Board Transmitter Path Compliance Eye Diagram at 5 GT/s
Table 25	System Board Transmitter Path Compliance Eye Requirements at 5 GT/s
Comments	N/A
Notes	With cross talk: Notes 1, 3, and 4; for more info, please visit the chapter "Specification Notes" on page 527. Without cross talk: N/A

Table 48 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
Section 4.8.3	Add-in Card Transmitter Path Compliance Eye Diagrams at 8.0 GT/s
Table 16	Add-in Card Transmitter Path Compliance Eye Requirements at 8.0 GT/s
Comments	N/A
Notes	Note 1, 3, and 4; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.12	System Board Transmitter Path Compliance Eye Diagram at 8.0 GT/s
Table 27	System Board Transmitter Path Compliance Eye Requirements at 8.0 GT/s with Ideal Adaptive TX Equalization
Comments	N/A
Notes	Note 1, 3, and 4; for more info, please visit the chapter “Specification Notes” on page 527.

Table 49 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
Section 4.8.4	Add-in Card Transmitter Path Compliance Eye Diagrams at 16.0 GT/s
Table 17	Add-in Card Transmitter Path Compliance Eye Requirements at 16.0 GT/s
Comments	N/A
Notes	1, 3, and 4; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.13	System Board Transmitter Path Compliance Eye Diagram at 16.0 GT/s
Table 28	System Board Transmitter Path Compliance Eye Requirements at 16.0 GT/s with Ideal Adaptive TX Equalization
Comments	N/A
Notes	Note 1, 3, and 4; for more info, please visit the chapter “Specification Notes” on page 527.

NOTE The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test.

1 Obtains the eye-width test results from SigTest tools.

2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express Base Specification.

3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output/Input Voltage (Transition) Test

The **Peak Differential Output Voltage (Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

The **Peak Differential Input Voltage** test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the standard specifications.

$$V_{RX-DIFFp-p} = 2*|V_{RX-D+} - V_{RX-D-}|$$

Pass Limits

Table 50 Passing Limits Table for Peak Differential Output/Input Voltage (Transition) Test (Parameter: $V_{RX-DIFF-PP}$ or $V_{TX-DIFF-PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe1.0a	Base - Transmitter Tests	2.5 GT/s	Clean Clock	HP: 800.0 mV /1.2000 V	High Power: Base Spec 1.0a, Table 4-5
				LP: Info Only	Low Power: Base Spec 1.0a, Table 4-5
			SSC	HP: 800.0 mV /1.2000 V	High Power: Base Spec 1.0a, Table 4-5
				LP: Info Only	Low Power: Base Spec 1.0a, Table 4-5
	Base - Receiver Tests	2.5 GT/s	Clean Clock	175.0 mV/ 1.2000 V	Base Spec 1.0a, Table 4-6
			SSC	175.0 mV/ 1.2000 V	Base Spec 1.0a, Table 4-6
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	514.0 mV/ N/A	CEM Spec 1.0a, Table 4-6
			SSC	514.0 mV/ N/A	CEM Spec 1.0a, Table 4-6
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	274.0 mV/ N/A	CEM Spec 1.0a, Table 4-8
			SSC	274.0 mV/ N/A	CEM Spec 1.0a, Table 4-8
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference

Table 50 Passing Limits Table for Peak Differential Output/Input Voltage (Transition) Test (Parameter: $V_{RX-DIFF-PP}$ or $V_{TX-DIFF-PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe1.1	Base - Transmitter Tests	2.5 GT/s	Clean Clock	HP: 800.0 mV/ 1.2000 V	High Power: Base Spec 1.1, Table 4-5
				LP: 400.0 mV/ 1.2000 V	Low Power: Mobile Graphic Low Power Addendum to the Base Spec 1.0
			SSC	HP: 800.0 mV/ 1.2000 V	High Power: Base Spec 1.1, Table 4-5
				LP: 400.0 mV/ 1.2000 V	Low Power: Mobile Graphic Low Power Addendum to the Base Spec 1.0
	Base - Receiver Tests	2.5 GT/s	Clean Clock	175.0 mV/ 1.2000 V	Base Spec 1.1, Table 4-6
			SSC	175.0 mV/ 1.2000 V	N/A (Not Applicable)
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	514.0 mV/ N/A	CEM Spec 1.1, Table 4-7
			SSC	514.0 mV/ N/A	CEM Spec 1.1, Table 4-7
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	274.0 mV/ N/A	CEM Spec 1.1, Table 4-9
			SSC	274.0 mV/ N/A	CEM Spec 1.1, Table 4-9
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 50 Passing Limits Table for Peak Differential Output/Input Voltage (Transition) Test (Parameter: $V_{RX-DIFF-PP}$ or $V_{TX-DIFF-PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe2.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	HP: 800.0 mV/ 1.2000 V	High Power: Base Spec 2.0, Table 4-9
				LP: 400.0 mV/ 1.2000 V	Low Power: Base Spec 2.0, Table 4-9
			SSC	HP: 800.0 mV/ 1.2000 V	High Power: Base Spec 2.0, Table 4-9
				LP: 400.0 mV/ 1.2000 V	Low Power: Base Spec 2.0, Table 4-9
	Base - Receiver Tests	2.5 GT/s	Clean Clock	175.0 mV/ 1.2000 V	Base Spec 2.0, Table 4-12
			SSC	175.0 mV/ 1.2000 V	Base Spec 2.0, Table 4-12
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	514.0 mV/ 1.2000 V	CEM Spec 2.0, Table 4-7
			SSC	514.0 mV/ 1.2000 V	CEM Spec 2.0, Table 4-7
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	274.0 mV/ 1.2000 V	CEM Spec 2.0, Table 4-14
			SSC	274.0 mV/ 1.2000 V	CEM Spec 2.0, Table 4-14
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 50 Passing Limits Table for Peak Differential Output/Input Voltage (Transition) Test (Parameter: $V_{RX-DIFF-PP}$ or $V_{TX-DIFF-PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe2.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	HP (-3.5dB): 800.0 mV/ 1.2000 V	High Power: Base Spec 2.0, Table 4-9
				HP (-6.0dB): 800.0 mV/ 1.2000 V	High Power: Base Spec 2.0, Table 4-9
				LP: 400.0 mV/ 1.2000 V	Low Power: Base Spec 2.0, Table 4-9
			SSC	HP (-3.5dB): 800.0 mV/ 1.2000 V	High Power: Base Spec 2.0, Table 4-9
				HP (-6.0dB): 800.0 mV/ 1.2000 V	High Power: Base Spec 2.0, Table 4-9
				LP: 400.0 mV/ 1.2000 V	Low Power: Base Spec 2.0, Table 4-9
	Base - Receiver Tests	5.0 GT/s	Clean Clock	For DClk: 100.0 mV/ 1.2000 V	For Data Clk: Base Spec 2.0, Table 4-12
				For CRefClk: 120.0 mV/ 1.2000 V	For Common RefClk: Base Spec 2.0, Table 4-12
			SSC	For DClk: 100.0 mV/ 1.2000 V	For Data Clk: Base Spec 2.0, Table 4-12
				For CRefClk: 120.0 mV/ 1.2000 V	For Common RefClk: Base Spec 2.0, Table 4-12
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	380.0 mV/ 1.2000 V	For -3.5dB: CEM Spec 2.0, Table 4-8
				306.0 mV/ 1.2000 V	For -6.0dB: CEM Spec 2.0, Table 4-10
			SSC	380.0 mV/ 1.2000 V	For -3.5dB: CEM Spec 2.0, Table 4-8
				306.0 mV/ 1.2000 V	For -6.0dB: CEM Spec 2.0, Table 4-10
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	300.0 mV/ 1.2000 V	CEM Spec 2.0, Table 4-15
			SSC	300.0 mV/ 1.2000 V	CEM Spec 2.0, Table 4-15
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 50 Passing Limits Table for Peak Differential Output/Input Voltage (Transition) Test (Parameter: $V_{RX-DIFF-PP}$ or $V_{TX-DIFF-PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe3.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	HP: 800.0 mV /1.2000 V	High Power: Base Spec 3.0, Table 4-18
				LP: 400.0 mV /1.2000 V	Low Power: Base Spec 3.0, Table 4-18
			SSC	HP: 800.0 mV /1.2000 V	High Power: Base Spec 3.0, Table 4-18
				LP: 400.0 mV /1.2000 V	Low Power: Base Spec 3.0, Table 4-18
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	514.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-6
			SSC	514.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-6
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	274.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-16
			SSC	274.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-16
	U.2 - EndPoint Tests	2.5 GT/s	Clean Clock	514.0 mV/ 1.2000 V	U.2 Spec
			SSC	514.0 mV/ 1.2000 V	U.2 Spec
	U.2 - RootComplex Tests	2.5 GT/s	Clean Clock	274.0 mV/ 1.2000 V	U.2 Spec
			SSC	274.0 mV/ 1.2000 V	U.2 Spec
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 50 Passing Limits Table for Peak Differential Output/Input Voltage (Transition) Test (Parameter: $V_{RX-DIFF-PP}$ or $V_{TX-DIFF-PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe3.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	HP: 800.0 mV/ 1.2000 V	High Power: Base Spec 3.0, Table 4-18
				LP: 400.0 mV/ 1.2000 V	Low Power: Base Spec 3.0, Table 4-18
			SSC	HP: 800.0 mV/ 1.2000 V	High Power: Base Spec 3.0, Table 4-18
				LP: 400.0 mV/ 1.2000 V	Low Power: Base Spec 3.0, Table 4-18
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	380.0 mV/ 1.2000 V	For -3.5dB: CEM Spec 3.0, Table 4-7
				306.0 mV/ 1.2000 V	For -6.0dB: CEM Spec 3.0, Table 4-9
			SSC	380.0 mV/ 1.2000 V	For -3.5dB: CEM Spec 3.0, Table 4-7
				306.0 mV/ 1.2000 V	For -6.0dB: CEM Spec 3.0, Table 4-9
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	225.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-17
			SSC	225.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-17
	U.2 - EndPoint Tests	5.0 GT/s	Clean Clock	380.0 mV/ 1.2000 V	U.2 Spec (for -3.5dB)
				306.0 mV/ 1.2000 V	U.2 Spec (for -6.0dB)
			SSC	380.0 mV/ 1.2000 V	U.2 Spec (for -3.5dB)
				306.0 mV/ 1.2000 V	U.2 Spec (for -6.0dB)
	U.2 - RootComplex Tests	5.0 GT/s	Clean Clock	225.0 mV/ 1.2000 V	U.2 Spec
			SSC	225.0 mV/ 1.2000 V	U.2 Spec
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 50 Passing Limits Table for Peak Differential Output/Input Voltage (Transition) Test (Parameter: $V_{RX-DIFF-PP}$ or $V_{TX-DIFF-PP}$)

PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	8.0 GT/s	Clean Clock	34.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-11
			SSC	34.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-11
	CEM - RootComplex Tests	8.0 GT/s	Clean Clock	34.0 mV/ 1.2000 V	CEM Spec 3.0, Figure 4-14, Table 4-19
			SSC	34.0 mV/ 1.2000 V	CEM Spec 3.0, Figure 4-14, Table 4-19
	U.2 - EndPoint Tests	8.0 GT/s	Clean Clock	34.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-11
			SSC	34.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-11
	U.2 - RootComplex Tests	8.0 GT/s	Clean Clock	34.0 mV/ 1.2000 V	CEM Spec 3.0, Figure 4-14, Table 4-19
			SSC	34.0 mV/ 1.2000 V	CEM Spec 3.0, Figure 4-14, Table 4-19
	Base - RefClk Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	800.0 mV/ 1.2000 V	Base Spec 4.0, Table 8-7
			SSC	800.0 mV/ 1.2000 V	Base Spec 4.0, Table 8-7
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	514.0 mV/ 1.2000 V	CEM Spec 4.0, Table 11
			SSC	514.0 mV/ 1.2000 V	CEM Spec 4.0, Table 11
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	274.0 mV/ 1.2000 V	CEM Spec 4.0, Table 24
			SSC	274.0 mV/ 1.2000 V	CEM Spec 4.0, Table 24
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference

Table 50 Passing Limits Table for Peak Differential Output/Input Voltage (Transition) Test (Parameter: $V_{RX-DIFF-PP}$ or $V_{TX-DIFF-PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	HP(-3.5dB): 800.0 mV/ 1.2000 V	High Power(-3.5dB): Base Spec 4.0, Table 8-7
				HP(-6.0dB): 800.0 mV/ 1.2000 V	High Power(-6.0dB): Base Spec 4.0, Table 8-7
				LP: 400.0 mV/ 1.2000 V	Low Power: Base Spec 4.0, Table 8-7
			SSC	HP(-3.5dB): 800.0 mV/ 1.2000 V	High Power(-3.5dB): Base Spec 4.0, Table 8-7
				HP(-6.0dB): 800.0 mV/ 1.2000 V	High Power(-6.0dB): Base Spec 4.0, Table 8-7
				LP: 400.0 mV/ 1.2000 V	Low Power: Base Spec 4.0, Table 8-7
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	380.0 mV/ 1.2000 V	For -3.5dB: CEM Spec 4.0, Table 12
				306.0 mV/ 1.2000 V	For -6.0dB: CEM Spec 4.0, Table 14
			SSC	380.0 mV/ 1.2000 V	For -3.5dB: CEM Spec 4.0, Table 12
				306.0 mV/ 1.2000 V	For -6.0dB: CEM Spec 4.0, Table 14
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	225.0 mV/ 1.2000 V	CEM Spec 4.0, Table 25
			SSC	225.0 mV/ 1.2000 V	CEM Spec 4.0, Table 25
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 50 Passing Limits Table for Peak Differential Output/Input Voltage (Transition) Test (Parameter: $V_{RX-DIFF-PP}$ or $V_{TX-DIFF-PP}$)

PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	8.0 GT/s	Clean Clock	34.0 mV/ 1.3000 V	CEM Spec 4.0, Table 16
			SSC	34.0 mV/ 1.3000 V	CEM Spec 4.0, Table 16
	CEM - RootComplex Tests	8.0 GT/s	Clean Clock	34.0 mV/ 1.2000 V	CEM Spec 4.0, Table 27
			SSC	34.0 mV/ 1.2000 V	CEM Spec 4.0, Table 27
	Base - RefClk Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	16.0 GT/s	Clean Clock	23.0 mV/ 1.3000 V	CEM Spec 4.0, Table 17
			SSC	23.0 mV/ 1.3000 V	CEM Spec 4.0, Table 17
	CEM - RootComplex Tests	16.0 GT/s	Clean Clock	19.0 mV/ 1.2000 V	CEM Spec 4.0, Table 28
			SSC	19.0 mV/ 1.2000 V	CEM Spec 4.0, Table 28
	Base - RefClk Tests	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 51 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications
Comments	$V_{TX-DIFFp-p} = 2*\|V_{TX-D+} - V_{TX-D-}\|$
Notes	Note 2; for more info, please visit the chapter “Specification Notes” on page 428.
PCI Express™ Base Specification Revision 1.0a	
Section 4.3.4	Differential Receiver (RX) Input Specifications
Table 4-6	Differential Receiver (RX) Input Specifications
Comments	$V_{RX-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$
Notes	Note 7; for more info, please visit the chapter “Specification Notes” on page 428.

Table 51 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ CEM Specification Revision 1.0a	
Section 4.7.1	Add-in Card Transmitter Path Compliance Eye-Diagram
Table 4-6	Add-in Card Transmitter Path Compliance Eye Requirements
Comments	All Links are assumed active while generating this eye diagram. Transition and nontransition bits must be distinguished in order to measure compliance against the deemphasized voltage level (V_{txA_d}).
Notes	Please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 1.0a	
Section 4.7.3	System Board Transmitter Path Compliance Eye Diagram
Table 4-8	System Board Transmitter Path Compliance Eye Requirements
Comments	All Links are assumed active while generating this eye diagram. Transition and nontransition bits must be distinguished in order to measure compliance against the deemphasized voltage level (T_{txS_d}).
Notes	Please visit the chapter “Specification Notes” on page 527.

Table 52 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications
Comments	$V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{TX\text{-}D+} - V_{TX\text{-}D-}\rvert$
Notes	Note 2; for more info, please visit the chapter “Specification Notes” on page 428.
PCI Express™ Base Specification Revision 1.1	
Section 4.3.4	Differential Receiver (RX) Input Specifications
Table 4-6	Differential Receiver (RX) Input Specifications
Comments	$V_{RX\text{-}DIFFp\text{-}p} = 2*\lvert V_{RX\text{-}D+} - V_{RX\text{-}D-}\rvert$
Notes	Note 8; for more info, please visit the chapter “Specification Notes” on page 428.
PCI Express™ CEM Specification Revision 1.1	
Section 4.7.1	Add-in Card Transmitter Path Compliance Eye-Diagram
Table 4-7	Add-in Card Transmitter Path Compliance Eye Requirements
Comments	N/A
Notes	Note 1, 2, and 5; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 1.1	
Section 4.7.3	System Board Transmitter Path Compliance Eye Diagram
Table 4-9	System Board Transmitter Path Compliance Eye Requirements
Comments	N/A
Notes	Note 1, 2, and 5; for more info, please visit the chapter “Specification Notes” on page 527.

Table 53 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.3.5	Transmitter Specification
Table 4-9	2.5 and 5.0 GT/s Transmitter Specifications
Comments	As measured with compliance test load. Defined as $2*\lvert V_{TXD+} - V_{TXD-}\rvert$.
Notes	Note 9; for more info, please visit the chapter “Specification Notes” on page 428.
PCI Express™ Base Specification Revision 2.0	
Section 4.3.4.4	Receiver Specifications
Table 4-12	2.5 and 5.0 GT/s Receiver Specifications
Comments	See Section 4.3.7.2.2. of the PCI Express Base Specification Revision 2.0.
Notes	N/A

Table 53 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
Section 4.7.1	Add-in Card Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 4-7	Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Comments	N/A
Notes	Note 1, 2, and 5; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 2.0	
Section 4.7.5	System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 4-14	System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Comments	N/A
Notes	Note 1, 2, and 5; for more info, please visit the chapter “Specification Notes” on page 527.

Table 54 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.3.5	Transmitter Specification
Table 4-9	2.5 and 5.0 GT/s Transmitter Specifications
Comments	As measured with compliance test load. Defined as $2*\|V_{TXD+} - V_{TXD-}\|$.
Notes	Note 9; for more info, please visit the chapter “Specification Notes” on page 428.
PCI Express™ Base Specification Revision 2.0	
4.3.4.4	Receiver Specifications
Table 4-12	2.5 and 5.0 GT/s Receiver Specifications
Comments	See Section 4.3.7.2.2. of the PCI Express Base Specification Revision 2.0.
Notes	N/A
PCI Express™ CEM Specification Revision 2.0	
Section 4.7.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5 GT/s
Table 4-8	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s and 3.5 dB De-emphasis
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter “Specification Notes” on page 527.
Table 4-10	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s at 6.0 dB De-emphasis
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 2.0	
Section 4.7.6	System Board Transmitter Path Compliance Eye Diagram at 5 GT/s

Table 54 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

Table 4-15	System Board Transmitter Path Compliance Eye Requirements at 5 GT/s
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter “Specification Notes” on page 527.

Table 55 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base and CEM Specification Revision 1.1	
Please refer to Table 53, “PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes,”.	
PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications
Comments	As measured with compliance test load. Defined as $2*\|V_{TXD+} - V_{TXD-}\|$.
Notes	N/A
PCI Express™ Base and CEM Specification Revision 3.0	
Section 4.8.1	Add-in Card Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 4-6	Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Comments	N/A
Notes	Note 1, 2, and 5; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ Base and CEM Specification Revision 3.0	
Section 4.8.7	System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 4-16	System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Comments	N/A
Notes	Note 1, 2, and 5; for more info, please visit the chapter “Specification Notes” on page 527.

Table 56 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications
Comments	As measured with compliance test load. Defined as $2*\|V_{TXD+} - V_{TXD-}\|$.
Notes	N/A
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5.0 GT/s
Table 4-7	Add-in Card Transmitter Path Compliance Eye Requirements at 5.0 GT/s and 3.5 dB De-emphasis
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter “Specification Notes” on page 527.

Table 56 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

Table 4-9	Add-in Card Transmitter Path Compliance Eye Requirements at 5.0 GT/s at 6.0 dB De-emphasis
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.8	System Board Transmitter Path Compliance Eye Diagram at 5.0 GT/s
Table 4-17	System Board Transmitter Path Compliance Eye Requirements at 5.0 GT/s
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter “Specification Notes” on page 527.

Table 57 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
Section 4.8.3	Add-in Card Transmitter Path Compliance Eye Diagrams at 8.0 GT/s
Table 4-11	Add-in Card Transmitter Path Compliance Eye Requirements at 8.0 GT/s
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.9	System Board Transmitter Path Compliance Eye Diagram at 8.0 GT/s
Figure 4-14	System Board Transmitter Path Composite Compliance Eye Diagram
Table 4-19	System Board Transmitter Path Compliance Eye Requirements at 8.0 GT/s with Ideal Adaptive TX Equalization
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter “Specification Notes” on page 527.

Table 58 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
Please refer to Table 53, “PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes,”.	
PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters
Comments	As measured with compliance test load. Defined as $2*\lvert V_{TXD+} - V_{bTXD-}\rvert$.
Notes	Note 3; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.1	Add-in Card Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 11	Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Comments	N/A

Table 58 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

Notes	Note 1, 2, and 5; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.10	System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 24	System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Comments	N/A
Notes	Note 1, 2, and 5; for more info, please visit the chapter “Specification Notes” on page 527.

Table 59 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base and CEM Specification Revision 2.0 and 3.0	
Please refer to Table 56, "PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes,".	
PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters
Comments	As measured with compliance test load. Defined as $2*\|V_{TXD+} - V_{bTXD-}\|$.
Notes	Note 3; for more info, please visit the chapter "Specification Notes" on page 527.
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5 GT/s
Table 12	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s and 3.5 dB De-emphasis
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter "Specification Notes" on page 527.
Table 14	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s at 6.0 dB De-emphasis
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter "Specification Notes" on page 527.
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.11	System Board Transmitter Path Compliance Eye Diagram at 5.0 GT/s
Table 25	System Board Transmitter Path Compliance Eye Requirements at 5.0 GT/s
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter "Specification Notes" on page 527.

Table 60 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
Please refer to Table 57, "PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes,".	
Section 4.8.3	Add-in Card Transmitter Path Compliance Eye Diagrams at 8.0 GT/s
Table 16	Add-in Card Transmitter Path Compliance Eye Requirements at 8.0 GT/s
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter "Specification Notes" on page 527.
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.12	System Board Transmitter Path Compliance Eye Diagram at 8.0 GT/s
Table 27	System Board Transmitter Path Compliance Eye Requirements at 8.0 GT/s with Ideal Adaptive TX Equalization
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter "Specification Notes" on page 527.

Table 61 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
Section 4.8.4	Add-in Card Transmitter Path Compliance Eye Diagrams at 16.0 GT/s
Table 17	Add-in Card Transmitter Path Compliance Eye Requirements at 16.0 GT/s
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.13	System Board Transmitter Path Compliance Eye Diagram at 16.0 GT/s
Table 28	System Board Transmitter Path Compliance Eye Requirements at 16.0 GT/s with Ideal Adaptive TX Equalization
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter “Specification Notes” on page 527.

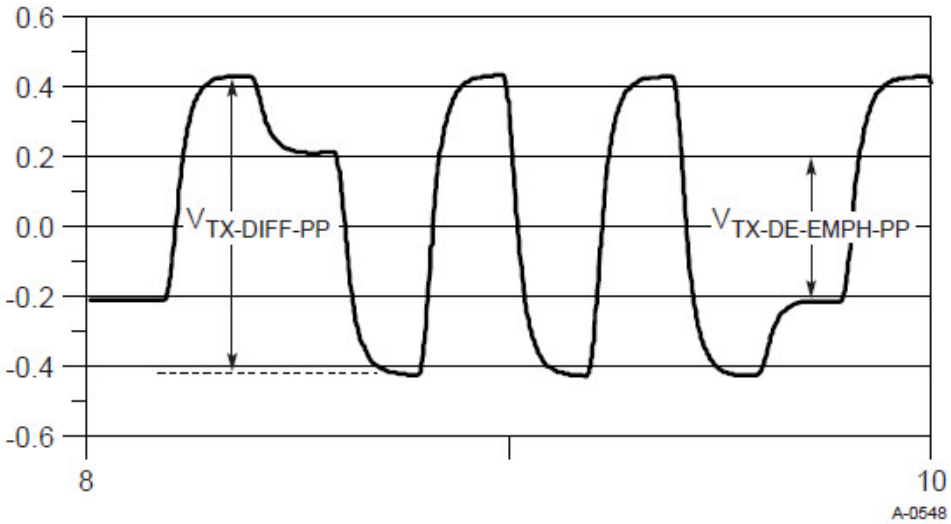


Figure 23 Full Swing Signaling Voltage Parameters Showing -6dB De-emphasis

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test.

1 Extracts the transition eye diagram data from the SigTest tools.

2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTest tools.

3 Finds the peak differential output/input voltage (transition) mean value from the center of UI.

4 Compares the measured peak differential output/input voltage (transition) value to the compliance test limits.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

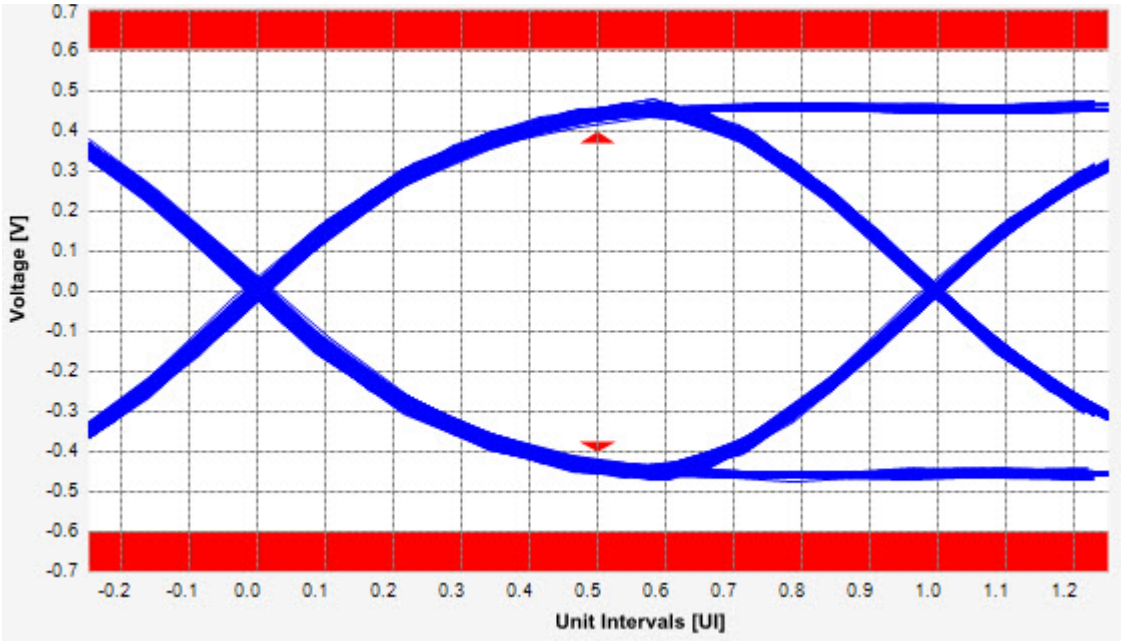


Figure 24 Reference Image for Peak Differential Output Voltage (Transition) Test

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (Non-Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Pass Limits

Table 62 Passing Limits Table for Peak Differential Output Voltage (Non-Transition) Test (Parameter: $V_{TX-DIFF-PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe1.0a	Base - Transmitter Tests	2.5 GT/s	Clean Clock	504.0 mV /1.2000 V	Base Spec 1.0a, Table 4-5
			SSC	504.0 mV /1.2000 V	Base Spec 1.0a, Table 4-5
	Base - Receiver Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	360.0 mV/ N/A	CEM Spec 1.0a, Table 4-6
			SSC	360.0 mV/ N/A	CEM Spec 1.0a, Table 4-6
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	253.0/ N/A	CEM Spec 1.0a, Table 4-8
			SSC	253.0/ N/A	CEM Spec 1.0a, Table 4-8
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference

Table 62 Passing Limits Table for Peak Differential Output Voltage (Non-Transition) Test (Parameter: $V_{TX-DIFF-PP}$)

PCIe1.1	Base - Transmitter Tests	2.5 GT/s	Clean Clock	504.0 mV/ 1.2000 V	Base Spec 1.1, Table 4-5
			SSC	504.0 mV/ 1.2000 V	Base Spec 1.1, Table 4-5
	Base - Receiver Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	360.0 mV/ N/A	CEM Spec 1.1, Table 4-7
			SSC	360.0 mV/ N/A	CEM Spec 1.1, Table 4-7
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	253.0 mV/ N/A	CEM Spec 1.1, Table 4-9
			SSC	253.0 mV/ N/A	CEM Spec 1.1, Table 4-9
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe2.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	504.0 mV/ 1.2000 V	Base Spec 2.0, Table 4-9
			SSC	504.0 mV/ 1.2000 V	Base Spec 2.0, Table 4-9
	Base - Receiver Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	360.0 mV/ 1.2000 V	CEM Spec 2.0, Table 4-7
			SSC	360.0 mV/ 1.2000 V	CEM Spec 2.0, Table 4-7
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	253.0 mV/ 1.2000 V	CEM Spec 2.0, Table 4-14
			SSC	253.0 mV/ 1.2000 V	CEM Spec 2.0, Table 4-14
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference

Table 62 Passing Limits Table for Peak Differential Output Voltage (Non-Transition) Test (Parameter: $V_{TX-DIFF-PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe2.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	HP (-3.5dB): 504.77 mV/ 1.2000 V	High Power: Base Spec 2.0, Table 4-9
				HP (-6.0dB): 378.50 mV/ 1.2000 V	High Power: Base Spec 2.0, Table 4-9
				LP: 400.0 mV/ 1.2000 V	Low Power: Base Spec 2.0, Table 4-9
			SSC	HP (-3.5dB): 504.77 mV/ 1.2000 V	High Power: Base Spec 2.0, Table 4-9
				HP (-6.0dB): 378.50 mV/ 1.2000 V	High Power: Base Spec 2.0, Table 4-9
				LP: 400.0 mV/ 1.2000 V	Low Power: Base Spec 2.0, Table 4-9
	Base - Receiver Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	380.0 mV/ 1.2000 V	For -3.5dB: CEM Spec 2.0, Table 4-8
				260.0 mV/ 1.2000 V	For -6.0dB: CEM Spec 2.0, Table 4-10
			SSC	380.0 mV/ 1.2000 V	For -3.5dB: CEM Spec 2.0, Table 4-8
				260.0 mV/ 1.2000 V	For -6.0dB: CEM Spec 2.0, Table 4-10
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	300.0 mV/ 1.2000 V	CEM Spec 2.0, Table 4-15
			SSC	300.0 mV/ 1.2000 V	CEM Spec 2.0, Table 4-15
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 62 Passing Limits Table for Peak Differential Output Voltage (Non-Transition) Test (Parameter: $V_{TX-DIFF-PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe3.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	476.5 mV/ 1.2000 V	Base Spec 3.0, Table 4-18
			SSC	476.5 mV/ 1.2000 V	Base Spec 3.0, Table 4-18
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	360.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-6
			SSC	360.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-6
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	253.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-16
			SSC	253.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-16
	U.2 - EndPoint Tests	2.5 GT/s	Clean Clock	360.0 mV/ 1.2000 V	U.2 Spec
			SSC	360.0 mV/ 1.2000 V	U.2 Spec
	U.2 - RootComplex Tests	2.5 GT/s	Clean Clock	253.0 mV/ 1.2000 V	U.2 Spec
			SSC	253.0 mV/ 1.2000 V	U.2 Spec
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 62 Passing Limits Table for Peak Differential Output Voltage (Non-Transition) Test (Parameter: $V_{TX-DIFF-PP}$)

PCIe3.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	HP(-3.5dB): 476.50 mV/ 1.2000 V	High Power(-3.5dB): Base Spec 3.0, Table 4-18
				HP(-6.0dB): 337.4 mV/ 1.2000 V	High Power(-6.0dB): Base Spec 3.0, Table 4-18
				LP: 400.0 mV/ 1.2000 V	Low Power: Base Spec 3.0, Table 4-18
			SSC	HP(-3.5dB): 476.50 mV/ 1.2000 V	High Power(-3.5dB): Base Spec 3.0, Table 4-18
				HP(-6.0dB): 337.4 mV/ 1.2000 V	High Power(-6.0dB): Base Spec 3.0, Table 4-18
				LP: 400.0 mV/ 1.2000 V	Low Power: Base Spec 3.0, Table 4-18
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	380.0 mV/ 1.2000 V	For -3.5dB: CEM Spec 3.0, Table 4-7
				260.0 mV/ 1.2000 V	For -6.0dB: CEM Spec 3.0, Table 4-9
			SSC	380.0 mV/ 1.2000 V	For -3.5dB: CEM Spec 3.0, Table 4-7
				260.0 mV/ 1.2000 V	For -6.0dB: CEM Spec 3.0, Table 4-9
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	225.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-17
			SSC	225.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-17
	U.2 - EndPoint Tests	5.0 GT/s	Clean Clock	380.0 mV/ 1.2000 V	U.2 Spec (for -3.5dB)
				260.0 mV/ 1.2000 V	U.2 Spec (for -6.0dB)
			SSC	380.0 mV/ 1.2000 V	U.2 Spec (for -3.5dB)
				260.0 mV/ 1.2000 V	U.2 Spec (for -6.0dB)
	U.2 - RootComplex Tests	5.0 GT/s	Clean Clock	225.0 mV/ 1.2000 V	U.2 Spec
			SSC	225.0 mV/ 1.2000 V	U.2 Spec
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 62 Passing Limits Table for Peak Differential Output Voltage (Non-Transition) Test (Parameter: $V_{TX-DIFF-PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	8.0 GT/s	Clean Clock	34.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-11
			SSC	34.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-11
	CEM - RootComplex Tests	8.0 GT/s	Clean Clock	34.0 mV/ 1.2000 V	CEM Spec 3.0, Figure 4-14, Table 4-19
			SSC	34.0 mV/ 1.2000 V	CEM Spec 3.0, Figure 4-14, Table 4-19
	U.2 - EndPoint Tests	8.0 GT/s	Clean Clock	34.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-11
			SSC	34.0 mV/ 1.2000 V	CEM Spec 3.0, Table 4-11
	U.2 - RootComplex Tests	8.0 GT/s	Clean Clock	34.0 mV/ 1.2000 V	CEM Spec 3.0, Figure 4-14, Table 4-19
			SSC	34.0 mV/ 1.2000 V	CEM Spec 3.0, Figure 4-14, Table 4-19
	Base - RefClk Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	476.5 mV/ 1.2000 V	Base Spec 4.0, Table 8-7
			SSC	476.5 mV/ 1.2000 V	Base Spec 4.0, Table 8-7
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	360.0 mV/ 1.2000 V	CEM Spec 4.0, Table 11
			SSC	360.0 mV/ 1.2000 V	CEM Spec 4.0, Table 11
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	253.0 mV/ 1.2000 V	CEM Spec 4.0, Table 24
			SSC	253.0 mV/ 1.2000 V	CEM Spec 4.0, Table 24
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference

Table 62 Passing Limits Table for Peak Differential Output Voltage (Non-Transition) Test (Parameter: $V_{TX-DIFF-PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	HP(-3.5dB): 476.50 mV/ 1.2000 V	High Power(-3.5dB): Base Spec 4.0, Table 8-7
				HP(-6.0dB): 337.4 mV/ 1.2000 V	High Power(-6.0dB): Base Spec 4.0, Table 8-7
				LP: 400.0 mV/ 1.2000 V	Low Power: Base Spec 4.0, Table 8-7
			SSC	HP(-3.5dB): 476.50 mV/ 1.2000 V	High Power(-3.5dB): Base Spec 4.0, Table 8-7
				HP(-6.0dB): 337.4 mV/ 1.2000 V	High Power(-6.0dB): Base Spec 4.0, Table 8-7
				LP: 400.0 mV/ 1.2000 V	Low Power: Base Spec 4.0, Table 8-7
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	380.0 mV/ 1.2000 V	For -3.5dB: CEM Spec 4.0, Table 12
				260.0 mV/ 1.2000 V	For -6.0dB: CEM Spec 4.0, Table 14
			SSC	380.0 mV/ 1.2000 V	For -3.5dB: CEM Spec 4.0, Table 12
				260.0 mV/ 1.2000 V	For -6.0dB: CEM Spec 4.0, Table 14
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	225.0 mV/ 1.2000 V	CEM Spec 4.0, Table 25
			SSC	225.0 mV/ 1.2000 V	CEM Spec 4.0, Table 25
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 62 Passing Limits Table for Peak Differential Output Voltage (Non-Transition) Test (Parameter: $V_{TX-DIFF-PP}$)

PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	8.0 GT/s	Clean Clock	34.0 mV/ 1.3000 V	CEM Spec 4.0, Table 16
			SSC	34.0 mV/ 1.3000 V	CEM Spec 4.0, Table 16
	CEM - RootComplex Tests	8.0 GT/s	Clean Clock	34.0 mV/ 1.2000 V	CEM Spec 4.0, Table 27
			SSC	34.0 mV/ 1.2000 V	CEM Spec 4.0, Table 27
	Base - RefClk Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	16.0 GT/s	Clean Clock	23.0 mV/ 1.3000 V	CEM Spec 4.0, Table 17
			SSC	23.0 mV/ 1.3000 V	CEM Spec 4.0, Table 17
	CEM - RootComplex Tests	16.0 GT/s	Clean Clock	19.0 mV/ 1.2000 V	CEM Spec 4.0, Table 28
			SSC	19.0 mV/ 1.2000 V	CEM Spec 4.0, Table 28
	Base - RefClk Tests	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 63 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications
PCI Express™ CEM Specification Revision 1.0a	
Section 4.7.1	Add-in Card Transmitter Path Compliance Eye-Diagram
Table 4-6	Add-in Card Transmitter Path Compliance Eye Requirements
Comments	All Links are assumed active while generating this eye diagram. Transition and nontransition bits must be distinguished in order to measure compliance against the deemphasized voltage level (V_{txA_d}).
Notes	Please visit the chapter “Specification Notes” on page 527.

Table 63 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ CEM Specification Revision 1.0a	
Section 4.7.3	System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 4-8	System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s

Table 64 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications
PCI Express™ CEM Specification Revision 1.1	
Section 4.7.1	Add-in Card Transmitter Path Compliance Eye-Diagram
Table 4-7	Add-in Card Transmitter Path Compliance Eye Requirements
PCI Express™ CEM Specification Revision 1.1	
Section 4.7.3	System Board Transmitter Path Compliance Eye Diagram
Table 4-9	System Board Transmitter Path Compliance Eye Requirements
Comments	N/A
Notes	Notes 1, 2, and 5; please visit the chapter “Specification Notes” on page 527.

Table 65 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.3.5	Transmitter Specification
Table 4-9	2.5 and 5.0 GT/s Transmitter Specifications
Comments	As measured with compliance test load. Defined as $2*\|V_{TXD+} - V_{TXD-}\|$.
Notes	Note 9; for more info, please visit the chapter “Specification Notes” on page 428.
PCI Express™ CEM Specification Revision 2.0	
Section 4.7.1	Add-in Card Transmitter Path Compliance Eye-Diagram at 2.5 GT/s
Table 4-7	Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s
PCI Express™ CEM Specification Revision 2.0	
Section 4.7.5	System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 4-14	System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Comments	N/A
Notes	Notes 1, 2, and 5; please visit the chapter “Specification Notes” on page 527.

Table 66 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.3.5	Transmitter Specification
Table 4-9	2.5 and 5.0 GT/s Transmitter Specifications
Comments	As measured with compliance test load. Defined as $2*\|V_{TXD+} - V_{TXD-}\|$.
Notes	Note 9; for more info, please visit the chapter “Specification Notes” on page 428.
PCI Express™ CEM Specification Revision 2.0	
Section 4.7.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5 GT/s
Table 4-8	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s and 3.5 dB De-emphasis
Table 4-10	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s at 6.0 dB De-emphasis
PCI Express™ CEM Specification Revision 2.0	
Section 4.7.6	System Board Transmitter Path Compliance Eye Diagram at 5.0 GT/s
Table 4-15	System Board Transmitter Path Compliance Eye Requirements at 5.0 GT/s
Notes	Notes 1, 2, and 4; please visit the chapter “Specification Notes” on page 527.

Table 67 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 1.1 and CEM Specification Revision 1.1 and 3.0	
Please refer to Table 65, “PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes,”.	
PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications
Comments	As measured with compliance test load. Defined as $2*\|V_{TXD+} - V_{TXD-}\|$.
Notes	N/A
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.7	System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 4-16	System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Notes	Notes 1, 2, and 5; please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.1	Add-in Card Transmitter Path Compliance Eye-Diagram 2.5 GT/s
Table 4-6	Add-in Card Transmitter Path Compliance Eye Requirements 2.5 GT/s
Notes	Notes 1, 2, and 5; please visit the chapter “Specification Notes” on page 527.

Table 68 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5 GT/s
Table 4-7	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s and 3.5 dB De-emphasis
Table 4-9	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s at 6.0 dB De-emphasis
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.8	System Board Transmitter Path Compliance Eye Diagram at 5.0 GT/s
Table 4-17	System Board Transmitter Path Compliance Eye Requirements at 5.0 GT/s

Table 69 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
Section 4.8.3	Add-in Card Transmitter Path Compliance Eye Diagrams at 8.0 GT/s
Table 4-11	Add-in Card Transmitter Path Compliance Eye Requirements at 8.0 GT/s
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.9	System Board Transmitter Path Compliance Eye Diagram at 8.0 GT/s
Figure 4-14	System Board Transmitter Path Composite Compliance Eye Diagram
Table 4-19	System Board Transmitter Path Compliance Eye Requirements at 8.0 GT/s with Ideal Adaptive TX Equalization

Table 70 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ CEM Specification Revision 1.1 and 3.0	
Please refer to Table 65, “PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes,”.	
PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters
Comments	As measured with compliance test load. Defined as $2*\|V_{TXD+} - V_{bTXD-}\|$.
Notes	Note 3; for more info, please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.1.	Add-in Card Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 11	Add-in Card Transmitter Path Compliance Eye Diagram Requirements at 2.5 GT/s
Notes	Notes 1, 2, and 5; please visit the chapter “Specification Notes” on page 527.
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.10	System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s
Table 24	System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s
Notes	Notes 1, 2, and 5; please visit the chapter “Specification Notes” on page 527.

Table 71 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base and CEM Specification Revision 2.0 and 3.0	
Please refer to Table 68, "PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes,".	
PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters
Comments	As measured with compliance test load. Defined as $2*\|V_{TXD+} - V_{bTXD-}\|$.
Notes	Note 3; for more info, please visit the chapter "Specification Notes" on page 527.
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5 GT/s
Table 12	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s and 3.5 dB De-emphasis
Table 14	Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s at 6.0 dB De-emphasis
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.11	System Board Transmitter Path Compliance Eye Diagram at 5.0 GT/s
Table 25	System Board Transmitter Path Compliance Eye Requirements at 5.0 GT/s
Notes	Notes 1, 2, and 4; please visit the chapter "Specification Notes" on page 527.

Table 72 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
Section 4.8.3	Add-in Card Transmitter Path Compliance Eye Diagrams at 8.0 GT/s
Table 16	Add-in Card Transmitter Path Compliance Eye Requirements at 8.0 GT/s
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter "Specification Notes" on page 527.
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.12	System Board Transmitter Path Compliance Eye Diagram at 8.0 GT/s
Table 27	System Board Transmitter Path Compliance Eye Requirements at 8.0 GT/s with Ideal Adaptive TX Equalization
Comments	N/A
Notes	Note 1, 2, and 4; for more info, please visit the chapter "Specification Notes" on page 527.

Table 73 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
Section 4.8.4	Add-in Card Transmitter Path Compliance Eye Diagrams at 16.0 GT/s
Table 17	Add-in Card Transmitter Path Compliance Eye Requirements at 16.0 GT/s
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.13	System Board Transmitter Path Compliance Eye Diagram at 16.0 GT/s
Table 28	System Board Transmitter Path Compliance Eye Requirements at 16.0 GT/s with Ideal Adaptive TX Equalization

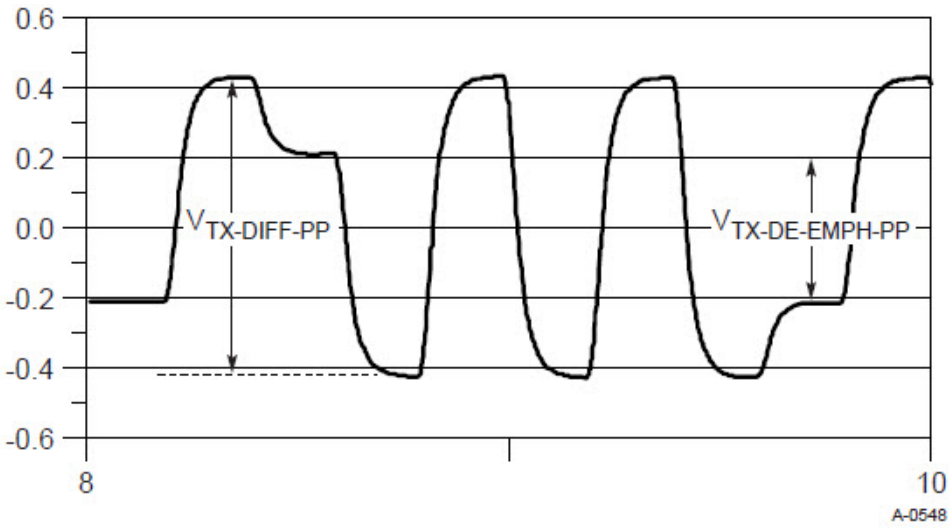


Figure 25 Full Swing Signaling Voltage Parameters Showing -6dB De-emphasis

Understanding the Test Flow

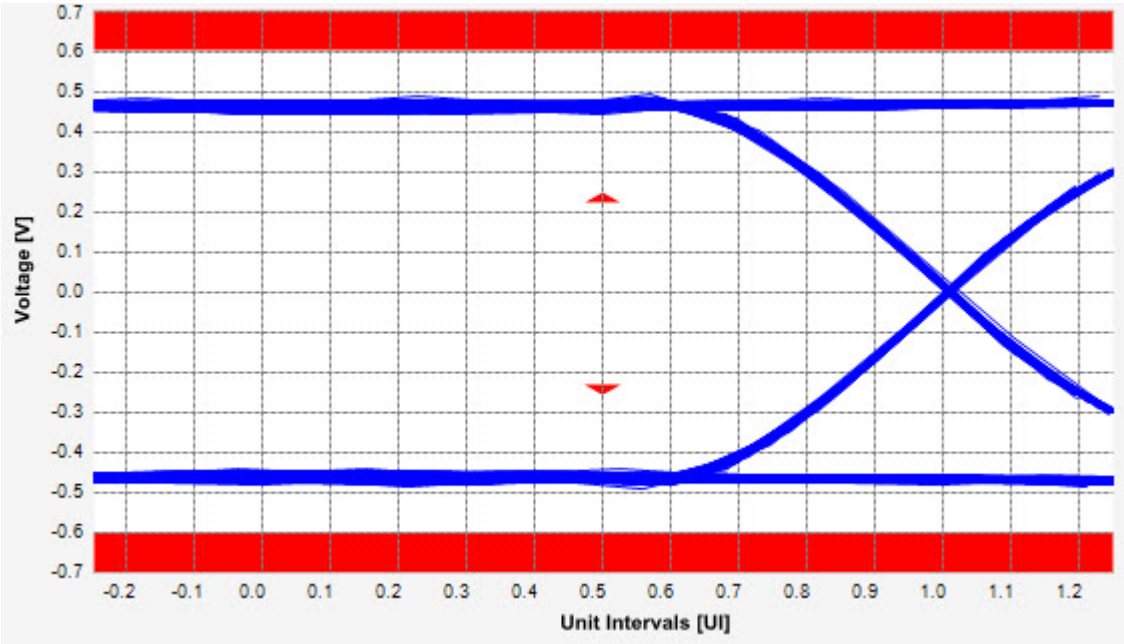
The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test.

1 Extracts the non transition eye diagram data from the SigTest tools.
2 Gets largest non transition amplitude (outer eye), smallest non transition amplitude (inner eye) test results from SigTest tools.
3 Finds the peak differential output voltage (non transition) mean value from the center of UI.
4 Compares the measured peak differential output voltage (non transition) value to the compliance test limits.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Rise/Fall Time Test

Rise/Fall time is taken independently on each single ended waveform source when you use two single ended probes or two SMA cables as the signal source. Differential signal rise/fall time shows up when you select differential probe type measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform.

Rise Time

This measurement is the time difference of the values observed when the V_{REF-HI} and the V_{REF-LO} reference level are crossed on the rising edge of the waveform.

$$t_{RISE}(n) = t_{HI+}(i) - t_{LO+}(j)$$

Where:

't_{RISE}' is a rise time measurement.

't_{HI+}' is a set of t_{HI} for rising edges only.

't_{LO+} is a set of t_{LO} for rising edges only.

'i' and 'j' are indexes for nearest adjacent pairs of t_{LO+} and t_{HI+}.

'n' is the index of rising edges in the waveform.

Rise time for $v_{D+}(t)$ is as follows:

$$t_{D+RISE}(n) = t_{D+HI+}(i) - t_{D+LO+}(j)$$

and for $v_{D-}(t)$:

$$t_{D-FALL}(n) = t_{D-LO-}(i) - t_{D-HI-}(j)$$

Fall Time

This measurement is the time difference of the values observed when the V_{REF-HI} and the V_{REF-LO} reference level are crossed on the falling edge of the waveform.

$t_{FALL}(n) = t_{LO-}(i) - t_{HI-}(j)$

Where:

't_{FALL}' is a fall time measurement.

't_{HI-}' is set of t_{HI} for falling edge only.

't_{LO-}' is set of t_{LO} for falling edge only.

'i' and j' are indexes for nearest adjacent pairs of t_{LO-} and t_{HI-}.

'n' is the index of falling edges in the waveform.

Pass Limits

Table 74 Passing Limits Table for Rise/Fall Time Test (Parameter: $T_{TX-RISE-FALL}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (min) (ps)	Reference
PCIe1.0a	Base - Transmitter Tests	2.5 GT/s	Clean Clock	125.00 mUI	Base Spec 1.0a, Table 4-5
			SSC	125.00 mUI	Base Spec 1.0a, Table 4-5
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (min) (ps)	Reference
PCIe1.1	Base - Transmitter Tests	2.5 GT/s	Clean Clock	125.00 mUI	Base Spec 1.1, Table 4-5
			SSC	125.00 mUI	Base Spec 1.1, Table 4-5
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (min) (ps)	Reference
PCIe2.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	125.00 mUI	Base Spec 2.0, Table 4-9
			SSC	125.00 mUI	Base Spec 2.0, Table 4-9
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (min) (ps)	Reference
PCIe2.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	30.00	Base Spec 2.0, Table 4-9
			SSC	30.00	Base Spec 2.0, Table 4-9
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 74 Passing Limits Table for Rise/Fall Time Test (Parameter: $T_{TX-RISE-FALL}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (min) (ps)	Reference
PCIe3.0	All	All GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (min) (ps)	Reference
PCIe4.0	All	All GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 75 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications

Table 76 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications

Table 77 PCI Express Gen 2.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 2.0
Please refer to Table 78, “PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes,”.

Table 78 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.3.5	Transmitter Specification
Table 4-9	2.5 and 5.0 GT/s Transmitter Specifications

Table 79 PCI Express Gen 3.0, All GT/s, References and Specification Notes

PCI Express™ Base and CEM Specification Revision
N/A (Not Applicable)

Table 80 PCI Express Gen 4.0, All GT/s, References and Specification Notes

PCI Express™ Base and CEM Specification Revision
N/A (Not Applicable)

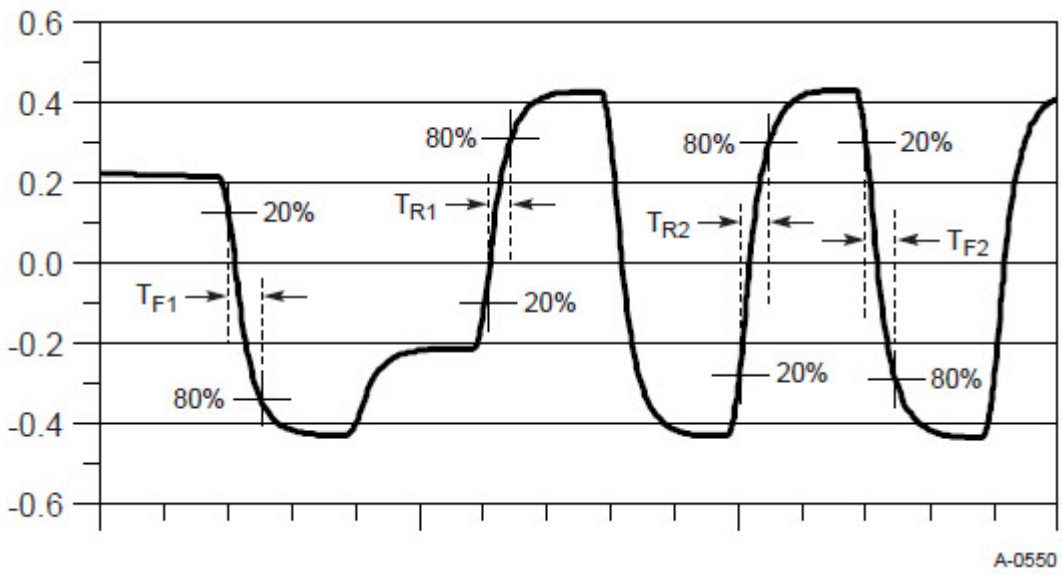


Figure 26 Rise and Fall Time Definition

Understanding the Test Flow

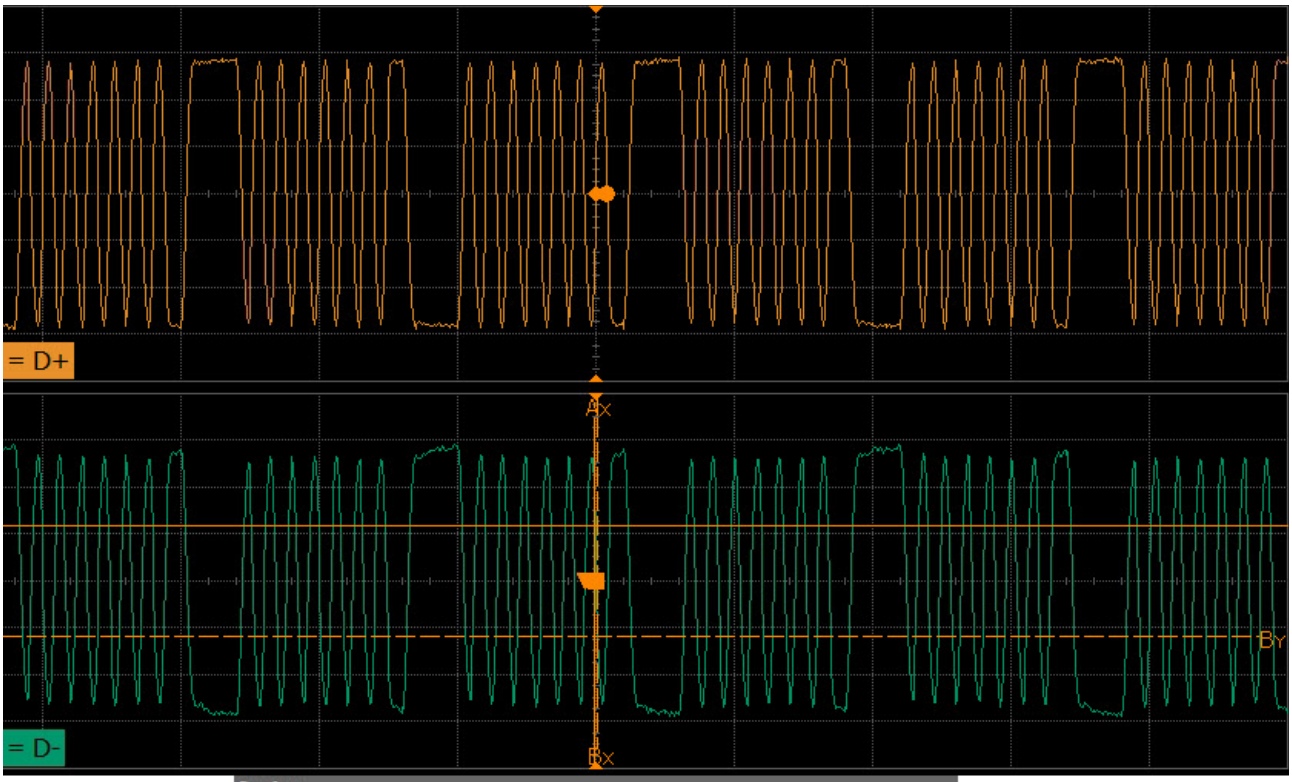
NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:
   a Sets the value of **Clock Recovery Method** as **First Order PLL**.
   b Sets the value of **Nominal Data Rate** as **2.500000000Gb/s**.
   c Sets the value of **Loop Bandwidth** as **1.500MHz**.
3 Enables **Real-Time Eye** using **De-emphasis** as **Real-Time Eye Bits**.
4 Measures the non - transition bits eye top and base.
5 Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.
6 Measures the transition bits eye top and base.
7 Configures **Thresholds** using **Measurement Analysis (EZJIT)** as follows:
   a Sets **Thresholds** as **20%,50%,80% of Top, Base**.
   b Defines **Top/Base** values using the previously measured eye top and base as **Histogram**.
8 If the **Transition Time Threshold** is configured as **Variable** using Automated Test Engine, then:
   a Configures the value for **Setup Horizontal** to 50ps and **Center Reference** to 180ps.
   b Configures **Real-Time Eye Setup** using **Serial Data**.
   c Selects **Real-Time Eye Bits** as **Pattern Qualify** and measures the fall time de-emphasis bits.
   d **Real-Time Eye Bits** as **Pattern Qualify** and measures the rise time de-emphasis bits.
   e **Real-Time Eye Bits** as **Pattern Qualify** and measures the fall time transition bits.
   f **Real-Time Eye Bits** as **Pattern Qualify** and measures the rise time transition bits.
   g Reports the maximum and minimum value for rise and fall time.
   h Reports the worst value as actual result.
9 Finds the minimum value from the minimum rise time and the minimum fall time. Compares the obtained value with the value as per the conformance limits specified in the PCI Express Base Specification.
10 Reports the worst case measured rise/fall time value as the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales				
	Horiz Scale	Position	Vertical Scale	Offset
Memory 1	5.000 ns/div	0.000s	83.75 mV/div	3.515 mV
Memory 2	5.000 ns/div	0.000s	82.00 mV/div	465.4 µV
Markers				

Figure 27 Reference Image for Rise/Fall Time Test

Deemphasized Voltage Ratio Test

This test measures the ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. The average de-emphasis value is tested against the specified value.

Pass Limits

Table 81 Passing Limits Table for Deemphasized Voltage Ratio Test (Parameter: $V_{TX\text{-}DE\text{-}RATIO}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max) (dB)	Reference
PCIe1.0a	Base - Transmitter Tests	2.5 GT/s	Clean Clock	-4.0/-3.0	Base Spec 1.0a, Table 4-5
			SSC	-4.0/-3.0	Base Spec 1.0a, Table 4-5
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max) (dB)	Reference
PCIe1.1	Base - Transmitter Tests	2.5 GT/s	Clean Clock	-4.0/-3.0	Base Spec 1.1, Table 4-5
			SSC	-4.0/-3.0	Base Spec 1.1, Table 4-5
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max) (dB)	Reference
PCIe2.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	-4.0/-3.0	Base Spec 2.0, Table 4-9
			SSC	-4.0/-3.0	Base Spec 2.0, Table 4-9
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max) (dB)	Reference
PCIe2.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	-4.0/-3.0 -6.5/-5.5	For -3.5dB: Base Spec 2.0, Table 4-9 For -6.0dB: Base Spec 2.0, Table 4-9
			SSC	-4.0/-3.0 -6.5/-5.5	For -3.5dB: Base Spec 2.0, Table 4-9 For -6.0dB: Base Spec 2.0, Table 4-9
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 81 Passing Limits Table for Deemphasized Voltage Ratio Test (Parameter: $V_{TX-DE-RATIO}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max) (dB)	Reference
PCIe3.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	-4.5/-2.5*	Base Spec 3.0, Section 4.3.2.1.3 *Pass limits not referenced to Table 4-18
			SSC	-4.5/-2.5*	Base Spec 3.0, Section 4.3.2.1.3 *Pass limits not referenced to Table 4-18
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max) (dB)	Reference
PCIe3.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	-4.5/-2.5* -7.0/-5.0*	For -3.5dB: Base Spec 3.0, Section 4.3.2.1.3 For -6.0dB: Base Spec 3.0, Section 4.3.2.1.3 *Pass limits not referenced to Table 4-18
			SSC	-4.5/-2.5* -7.0/-5.0*	For -3.5dB: Base Spec 3.0, Section 4.3.2.1.3 For -6.0dB: Base Spec 3.0, Section 4.3.2.1.3 *Pass limits not referenced to Table 4-18
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max) (dB)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max) (dB)	Reference
PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	-4.5/-2.5	Base Spec 4.0, Table 8-7
			SSC	-4.5/-2.5	Base Spec 4.0, Table 8-7
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max) (dB)	Reference

Table 81 Passing Limits Table for Deemphasized Voltage Ratio Test (Parameter: $V_{TX-DE-RATIO}$)

PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	-4.5/-2.5 -7.5/-4.5	For -3.5dB: Base Spec 4.0, Table 8-7 For -6.0dB: Base Spec 4.0, Table 8-7
			SSC	-4.5/-2.5 -7.5/-4.5	For -3.5dB: Base Spec 4.0, Table 8-7 For -6.0dB: Base Spec 4.0, Table 8-7
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max) (dB)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max) (dB)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 82 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications

Table 83 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications

Table 84 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.3.5	Transmitter Specifications
Table 4-9	2.5 and 5.0 GT/s Transmitter Specifications

Table 85 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.3.5	Transmitter Specifications
Table 4-9	2.5 and 5.0 GT/s Transmitter Specifications

Table 86 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.2.1.3	Tx Equalization Tolerance

Table 87 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0
Please refer to Table 86, “PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes,”.

Table 88 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision	
N/A	Not Applicable

Table 89 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters

Table 90 PCI Express Gen 4.0, 5.0 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters

Table 91 PCI Express Gen 4.0, 8.0 GT/s References and Specification Notes

PCI Express™ Base Specification Revision	
N/A	Not Applicable

Table 92 PCI Express Gen 4.0, 16.0 GT/s References and Specification Notes

PCI Express™ Base Specification Revision	
N/A	Not Applicable

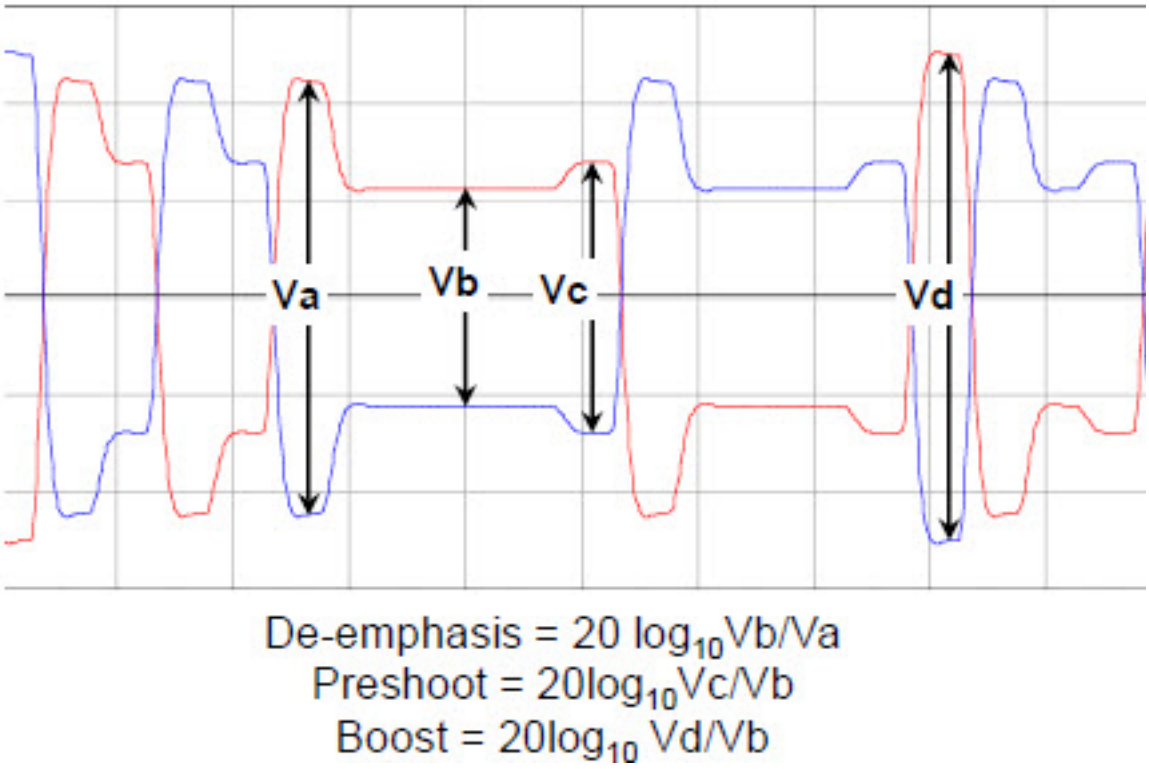


Figure 28 De-emphasized Voltage Ratio (Base Spec 4.0, Figure 8-5)

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 "Compliance Patterns in Various Encodings".

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:

   a Sets the value of **Clock Recovery Method** as **First Order PLL**.

   b Sets the value of **Nominal Data Rate** as **5.000000000 Gb/s**.

   c Sets the value of **Loop Bandwidth** as **1.500 MHz**.

3 Enables **Real-Time Eye** using **De-emphasis** as **Real-Time Eye Bits**.

4 Measures the non-transition bits eye top and base.

5 Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.

6 Measures the transition bits eye top and bases.

7 Finds the differential value between the transition bits eye top and base as $V_{TX\text{-}DIFF\text{-}PP}$ using **Histogram**.

8 Finds the differential value between the non-transition bits eye top and base as $V_{TX\text{-}DE\text{-}EMPH\text{-}PP}$ using **Histogram**.

9 Calculates de-emphasis ratio using the following formula:

$$\text{De-emphasis ratio} = -20*\log 10(V_{TX-DIFF-PP}/V_{TX-DE-EMPH-PP})$$

10 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Tmin-Pulse

This test verifies that the minimum pulse width is no less than the specified value. An oscilloscope and probe with at least 13 GHz bandwidth is recommended for accurate characterization of PCI-Express rise times less than 50 ps. If the number is close to the specified value, you may need to verify this measurement with a higher bandwidth oscilloscope.

Pass Limits

Table 93 Passing Limits Table for Tmin-Pulse Test (Parameter: $T_{MIN-PULSE}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI)	Reference
PCIe1.0a	All	All GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI)	Reference
PCIe1.1	All	All GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI)	Reference
PCIe2.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	900	Base Spec 2.0, Table 4-9
			SSC	900	Base Spec 2.0, Table 4-9
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI)	Reference
PCIe3.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	900	Base Spec 3.0, Table 4-18
			SSC	900	Base Spec 3.0, Table 4-18
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI)	Reference

Table 93 Passing Limits Table for Tmin-Pulse Test (Parameter: $T_{MIN-PULSE}$)

PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI)	Reference
PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	Info Only	N/A (Information Only Test)
			SSC	Info Only	N/A (Information Only Test)
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 94 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	Not Applicable

Table 95 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	Not Applicable

Table 96 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision	
N/A	Not Applicable

Table 97 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.3.5	Transmitter Specification
Table 4-9	2.5 and 5.0 GT/s Transmitter Specifications

Table 98 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base and CEM Specification Revision	
N/A	Not Applicable

Table 99 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications

Table 100 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision	
N/A	Not Applicable

Table 101 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base and CEM Specification Revision	
N/A	Not Applicable

Table 102 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	Not Applicable

Table 103 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision	
N/A	Not Applicable

Table 104 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	Not Applicable

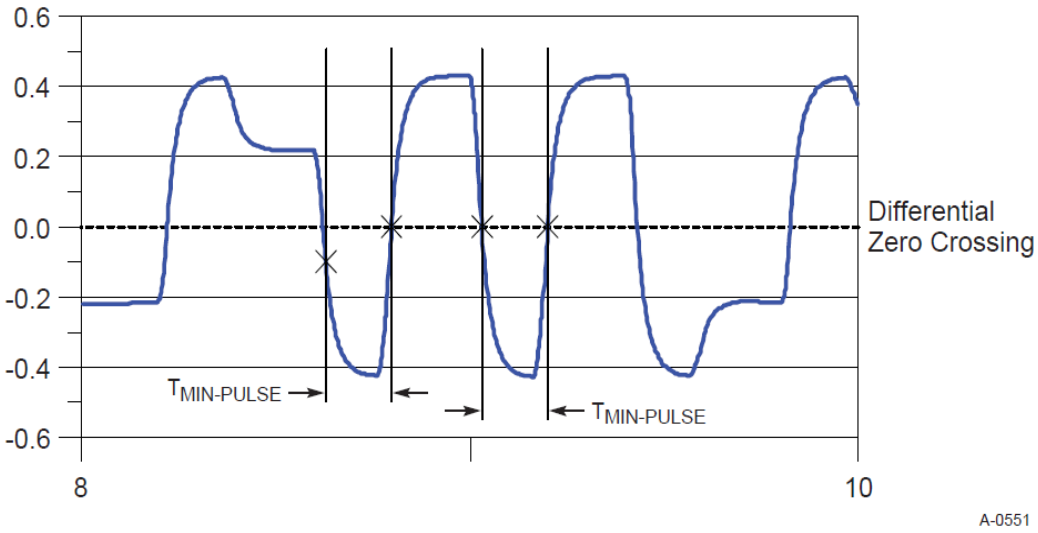


Figure 29 Minimum Pulse Width Definition

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:

   a Sets the value of **Clock Recovery Method** as **First Order PLL**.

   b Sets the value of **Nominal Data Rate** as **5.000000000Gb/s**.

   c Sets the value of **Loop Bandwidth** as **1.500 MHz**.

3 Enables **Real-Time Eye** using **De-emphasis** as **Real-Time Eye Bits**.

4 Measures the non - transition bits eye top and base.

5 Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.

6 Measures the transition bits eye top and base.

7 Configures **Thresholds** using **Measurement Analysis (EZJIT)** as follows:

   a Sets **Thresholds** as **20%,50%,80% of Top, Base**.

   b Defines **Top/Base** values using the previously measured eye top and base as **Histogram**.

8 If the **Transition Time Threshold** is configured as **Variable** using Automated Test Engine, then:
   a Configures the value for **Setup Horizontal** to 50 ps and **Center Reference** to 180 ps.
   b Configures **Real-Time Eye Setup** using Serial Data.
   c Selects **Real-Time Eye Bits** as **Pattern Qualify** and measures the fall time de-emphasis bits.
   d Selects **Real-Time Eye Bits** as **Pattern Qualify** and measures the rise time de-emphasis bits.
   e Selects **Real-Time Eye Bits** as **Pattern Qualify** and measures the fall time transition bits.
   f Selects **Real-Time Eye Bits** as **Pattern Qualify** and measures the rise time transition bits.
   g Reports the maximum and minimum value for rise and fall time.
   h Reports the worst value as actual result.
9 Finds the minimum value from the minimum rise time and the minimum fall time. Compares the obtained value with the value as per the conformance limits specified in the PCI Express Base Specification.
10 Reports the worst case measured rise/fall time value as the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deterministic Jitter Test > 1.5 MHz

The **Deterministic Jitter** test is a timing measurement in PCI Express 2.0 that requires separation of the high frequency jitter on the transmitter signal. The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

1 High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
2 Low frequency jitter (10 kHz - 1.5 MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
3 Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

This test requires the EZJIT-Plus option to be installed on the scope. The test is disabled if the option is unavailable.

Pass Limits

Table 105 Passing Limits Table for Deterministic Jitter Test > 1.5 MHz Test (Parameter: $T_{TX\text{-}HF\text{-}DJ\text{-}DD}$)

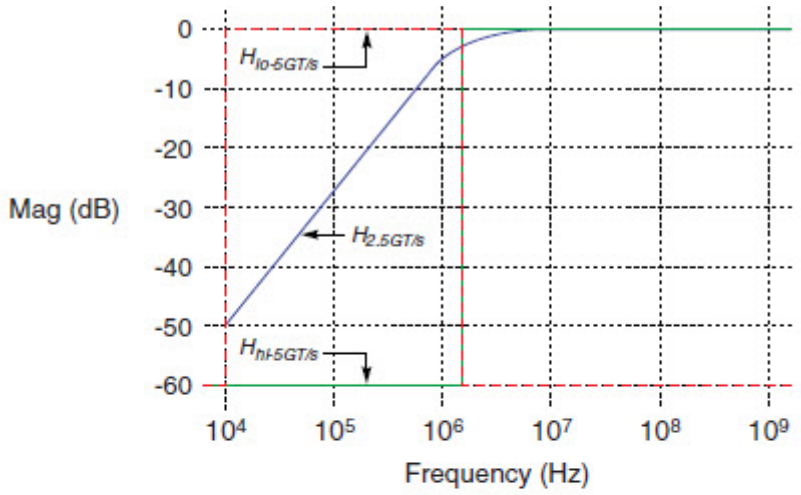
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI) (max)	Reference
PCIe1.0a	All	All GT/s	Clean Clock	N/A	Not Applicable
			SSC	N/A	Not Applicable
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI) (max)	Reference
PCIe1.1	All	All GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI) (max)	Reference
PCIe2.0	All	All GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI) (max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI) (max)	Reference
PCIe3.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	150	Base Spec 3.0, Table 4-18
			SSC	150	Base Spec 3.0, Table 4-18
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI) (max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 105 Passing Limits Table for Deterministic Jitter Test > 1.5 MHz Test (Parameter: $T_{TX-HF-DJ-DD}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mUI) (max)	Reference
PCIe4.0	All	All GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 106 PCI Express Gen 3.0 References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications



$$H_{2.5GT/s} = \frac{s}{s + w_c} \qquad w_c = 2\pi f_T$$

$$H_{hi\text{-}5GT/s} = if(f >= f_T)\ then\ 1.0\ else\ 10^{-3}$$

$$H_{lo\text{-}5GT/s} = if(f < f_{10kHz})\ then\ 10^{-3}$$

$$elseif\ (f < f_T)\ then\ 1.0$$

$$else\ 10^{-3}$$

$$f_T = 1.5\ MHz$$

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Figure 30 Plot of Transmitter HPF Filter Functions

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:

   a Sets the value of **Clock Recovery Method** as **Constant Frequency**, **Semi-Automatic** method and **Nominal Data Rate** to 5.000000000 Gb/s.

   b Turns on **TIE Filter** and configures the **Start Frequency** to **1.50000MHz** and **Stop Frequency** to **13GHz.**

3 Configures the following using the **Jitter / Noise Setup** as:

   a Configures **Measurement** as **TIE (Phase)**.

   b Configures **RJ Bandwidth** as **Narrow (Pink)**.

   c Configures **Units** as **Second**.

   d Checks **Auto** for **Pattern Length**.

   e Configures **BER Level** to **1E-12**.

4 Enables the jitter graph.

5 Configures the threshold for upper and lower level.

6 Reads the DJ value from the scope and divides by the unit interval.

7 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Random Jitter Test < 1.5 MHz

The **Random Jitter** test is a timing measurement in PCI Express 2.0 that requires separation of the low frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

- High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
- Low frequency jitter (10kHz – 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing. Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

Pass Limits

Table 107 Passing Limits Table for Random Jitter Test > 1.5 MHz Test (Parameter: $T_{TX-LF-RMS}$)

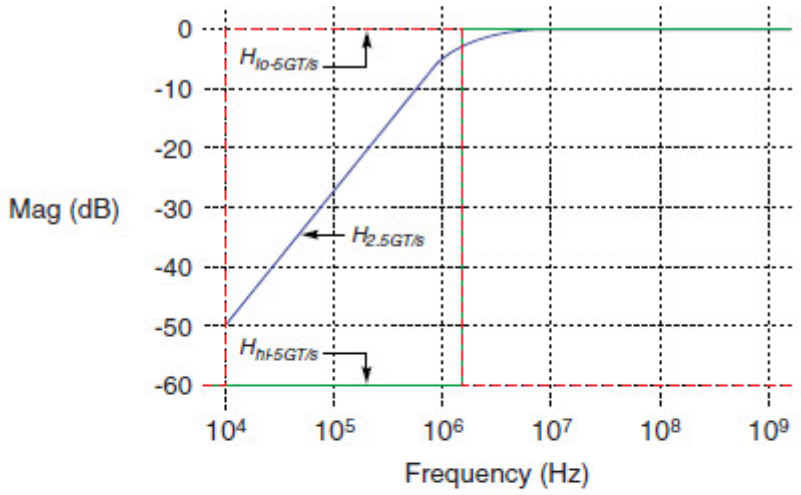
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (max)	Reference
PCIe1.0a	All	All GT/s	Clean Clock	N/A	Not Applicable
			SSC	N/A	Not Applicable
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (max)	Reference
PCIe1.1	All	All GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (max)	Reference
PCIe2.0	All	All GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (max)	Reference
PCIe3.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	3.00	Base Spec 3.0, Table 4-18
			SSC	3.00	Base Spec 3.0, Table 4-18
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 107 Passing Limits Table for Random Jitter Test > 1.5 MHz Test (Parameter: $T_{TX-LF-RMS}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (max)	Reference
PCIe4.0	All	All GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 108 PCI Express Gen 3.0 References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications



$$H_{2.5GT/s} = \frac{s}{s + w_c} \qquad w_c = 2\pi f_T$$

$$H_{hi\text{-}5GT/s} = if(f >= f_T)\ then\ 1.0\ else\ 10^{-3}$$

$$H_{lo\text{-}5GT/s} = if(f < f_{10kHz})\ then\ 10^{-3}$$

$$elseif\ (f < f_T)\ then\ 1.0$$

$$else\ 10^{-3}$$

$$f_T = 1.5\ MHz$$

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Figure 31 Plot of Transmitter HPF Filter Functions

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:
   a Sets the value of **Clock Recovery Method** as **Constant Frequency**, **Semi-Automatic** method and **Nominal Data Rate** to **5.000000000 Gb/s**.
   b Turns on **TIE Filter** and configures the **Start Frequency** to TIE filter frequency setting **of 10 kHz to 1.5 MHz .**
3 Configures the following using the **Jitter / Noise Setup** as:
   a Configures **Measurement** as **TIE (Phase)**.
   b Configures **RJ Bandwidth** as **Narrow (Pink)**.
   c Configures **Units** as **Second**.
   d Checks **Auto** for **Pattern Length**.
   e Configures **BER Level** to **1E-12**.
4 Enables the jitter graph.
5 Configures the threshold for upper and lower level.
6 Reads the TJ, RJ and DJ values from the scope and divides by the unit interval.
7 Reports the RJ measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Peak Common Mode Input Voltage Test

Receivers must reliably receive data when there is less than 150 mV of AC (>30 kHz) peak common mode input voltage. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in the PCI Express Base Specification.

$V_{RX\text{-}CM\text{-}AC} = |V_{RX\text{-}D+} + V_{RX\text{-}D-}|/2 - V_{RX\text{-}CM\text{-}DC}$

$V_{RX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{RX\text{-}D+} + V_{RX\text{-}D-}|/2$

NOTE This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel in put used), this test will be disabled. (see "Probing the Link for Rx Compliance" on page 34).

Pass Limits

Table 109 Passing Limits Table for AC Peak Common Mode Input Voltage Test (Parameter: $V_{RX\text{-}CM\text{-}AC}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe1.0a	Base - Receiver Tests	2.5 GT/s	Clean Clock	150.00	Base Spec 1.0a, Table 4-6
			SSC	150.00	Base Spec 1.0a, Table 4-6
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe1.1	Base - Receiver Tests	2.5 GT/s	Clean Clock	150.00	Base Spec 1.1, Table 4-6
			SSC	150.00	Base Spec 1.1, Table 4-6
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe2.0	Base - Receiver Tests	2.5 GT/s	Clean Clock	150.00	Base Spec 2.0, Table 4-12
			SSC	150.00	Base Spec 2.0, Table 4-12
	All Other	All	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe3.0	All	All	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 109 Passing Limits Table for AC Peak Common Mode Input Voltage Test (Parameter: $V_{RX-CM-AC}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	All	All	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 110 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
Section 4.3.4	Differential Receiver (RX) Input Specifications
Table 4-6	Differential Receiver (RX) Input Specifications

Table 111 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
Section 4.3.4	Differential Receiver (RX) Input Specifications
Table 4-6	Differential Receiver (RX) Input Specifications

Table 112 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.4.4	Receiver Specifications
Table 4-12	2.5 and 5.0 GT/s Receiver Specifications

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

The PCI Express test application performs the following automated steps for measuring the **AC Peak Common Mode Input Voltage** test based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3. Sets up DC common mode voltage using **Math (FFT and more...)** as follows:
   - *a* Configures **Operator** as **Common Mode** measurements.
   - *b* Loads common mode signal.
   - *c* Measures the average of common mode using V average measurement from scope.
   - *d* Measures compliance test limit boundaries (0V to 3.6V) using **Markers**.
4. Measures the average value of D+ and D- signal.
5. Computes DC common mode value by absolute the average of the total average value of the D+ signal and average value of D- signal.
6. Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the respective PCI Express Base Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

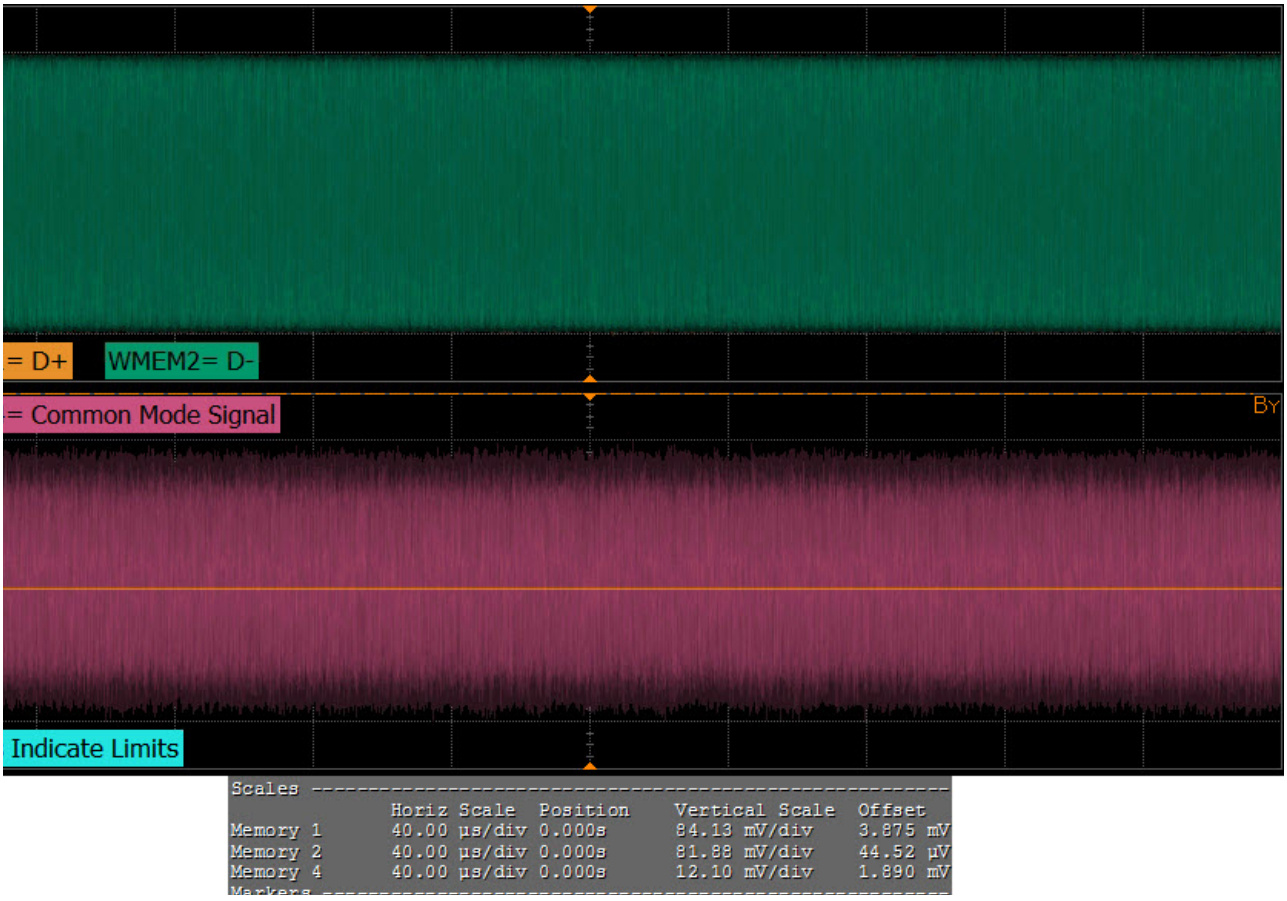


Figure 32 Reference Image for AC Peak Common Mode Input Voltage Test

RMS AC Peak Common Mode Output Voltage Test

The **RMS AC Peak Common Mode Output Voltage** is computed as:

$V_{TX\text{-}CM\text{-}AC\text{-}p} = RMS[(V_{D+} + V_{D-})/2 - DC_{AVG}(V_{D+} + V_{D-})/2]$

It is specified at the measurement point into a timing and voltage compliance test load and measured over any 250 consecutive T_X UIs.

NOTE This test is only available when the single-ended or SMA probing method has been used (see "Probing the Link for Tx Compliance" on page 28).

The AC common mode RMS voltage measurement calculates the RMS statistic of the common mode voltage waveform with the DC Value removed.

$v_{AC\text{-}RMS\text{-}CM}(i) = RMS\ (v_{AC\text{-}M}(i))$

where:

'i' is the index of all waveform values.

'$v_{AC\text{-}RMS\text{-}CM}$' is the RMS of the AC common mode voltage signal.

'$v_{AC\text{-}M}$' is the AC common mode voltage signal.

Pass Limits

Table 113 Passing Limits Table for RMS AC Peak Common Mode Output Voltage Test (Parameter: $V_{TX\text{-}CM\text{-}AC\text{-}p}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe1.0a	Base - Transmitter Tests	2.5 GT/s	Clean Clock	20.00	Base Spec 1.0a, Table 4-5
			SSC	20.00	Base Spec 1.0a, Table 4-5
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe1.1	Base - Transmitter Tests	2.5 GT/s	Clean Clock	20.00	Base Spec 1.1, Table 4-5
			SSC	20.00	Base Spec 1.1, Table 4-5
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe2.0	Base - Transmitter Tests	2.5. GT/s	Clean Clock	20.00	Base Spec 2.0, Table 4-9
			SSC	20.00	Base Spec 2.0, Table 4-9
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 113 Passing Limits Table for RMS AC Peak Common Mode Output Voltage Test (Parameter: $V_{TX-CM-AC-p}$)

	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe3.0	Base - Transmitter Tests	2.5. GT/s	Clean Clock	20.00	Base Spec 3.0, Table 4-18
			SSC	20.00	Base Spec 3.0, Table 4-18
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	All	All Other	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	2.5. GT/s	Clean Clock	20.00	Base Spec 1.1, Table 4-5
			SSC	20.00	Base Spec 1.1, Table 4-5
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	All	All Other	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 114 PCI Express Gen 1.0a, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications

Table 115 PCI Express Gen 1.1, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications

Table 116 PCI Express Gen 2.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.3.5	Transmitter Specifications
Table 4-9	2.5 and 5.0 GT/s Transmitter Specifications

Table 117 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

3 Sets up DC common mode voltage using **Math (FFT and more...)** as follows:

   a Configures **Operator** as **Common Mode** measurements.

   b Loads common mode signal.

   c Measures the average of common mode using **V average** measurement from scope.

   d Measures compliance test limit boundaries (0V to 3.6V) using **Markers**.

4 Measures **RMS Type** as **AC** and **Units** as **Volt** using **V rms Measurement**.

5 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the respective PCI Express Base Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

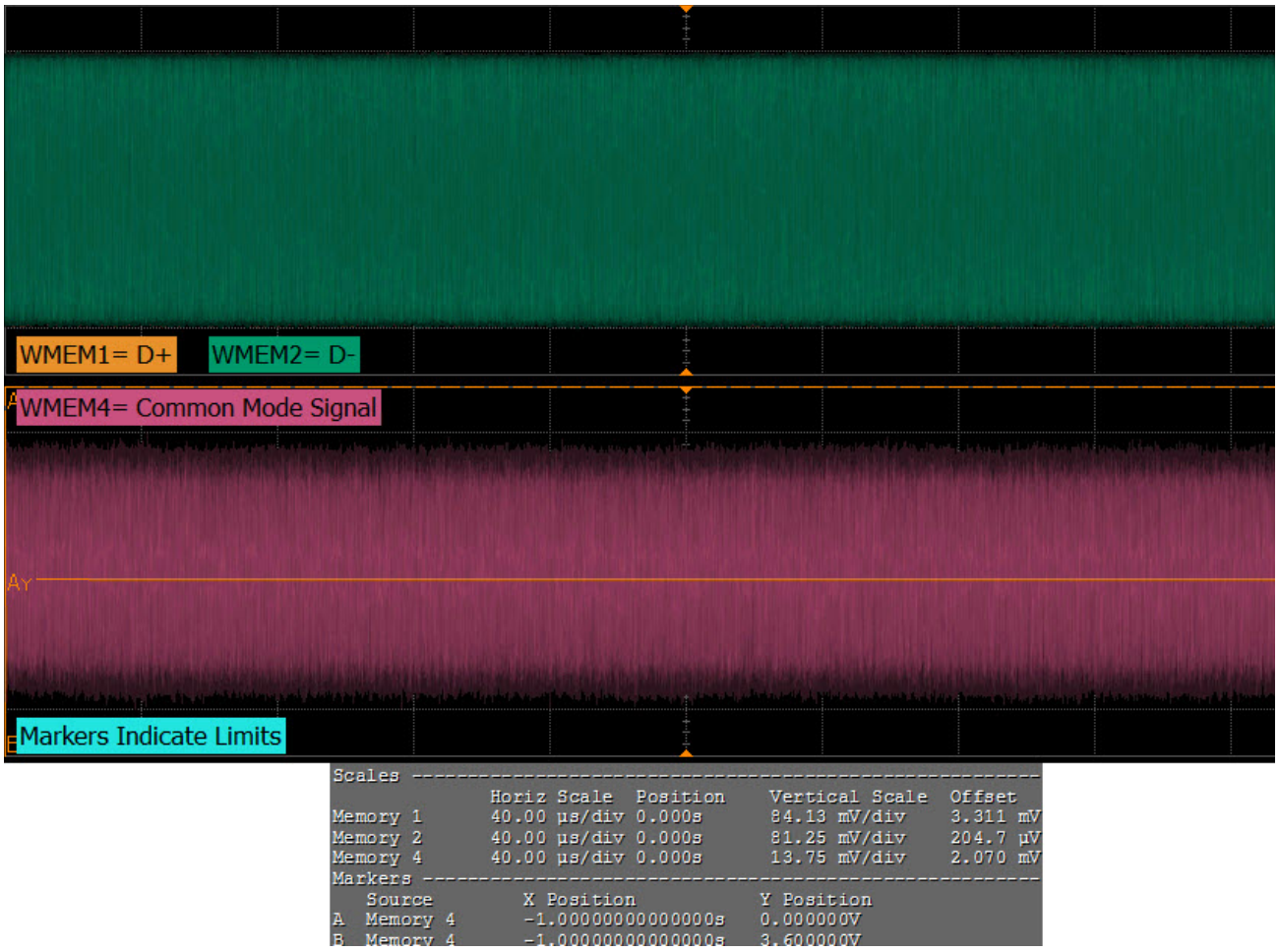


Figure 33 Reference Image for RMS AC Peak Common Mode Output Voltage Test

Avg DC Common Mode Output Voltage Test

The **Avg DC Common Mode Voltage** measurement computes the DC average of the common mode signal:

$V_{TX\text{-}DC\text{-}CM} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCI Express Base Specification, states that the transmitter DC common mode voltage ($V_{TX\text{-}DC\text{-}CM}$) must be held at the same value during all states.

Pass Limits

Table 118 Passing Limits Table for Avg DC Common Mode Output Voltage Test (Parameter: $V_{TX\text{-}DC\text{-}CM}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe1.0a	Base - Transmitter Tests	2.5 GT/s	Clean Clock	03.60	Base Spec 1.0a, Table 4-5
			SSC	03.60	Base Spec 1.0a, Table 4-5
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe1.1	Base - Transmitter Tests	2.5 GT/s	Clean Clock	03.60	Base Spec 1.1, Table 4-5
			SSC	03.60	Base Spec 1.1, Table 4-5
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe2.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	03.60	Base Spec 2.0, Table 4-9
			SSC	03.60	Base Spec 2.0, Table 4-9
	All other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe2.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	03.60	Base Spec 2.0, Table 4-9
			SSC	03.60	Base Spec 2.0, Table 4-9
	All other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference

Table 118 Passing Limits Table for Avg DC Common Mode Output Voltage Test (Parameter: $V_{TX\text{-}DC\text{-}CM}$)

PCIe3.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	3.60	Base Spec 3.0, Table 4-18
			SSC	3.60	Base Spec 3.0, Table 4-18
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe3.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	3.60	Base Spec 3.0, Table 4-18
			SSC	3.60	Base Spec 3.0, Table 4-18
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	3.60	Base Spec 4.0, Table 8-8
			SSC	3.60	Base Spec 4.0, Table 8-8
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	3.60	Base Spec 4.0, Table 8-8
			SSC	3.60	Base Spec 4.0, Table 8-8
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 119 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications

Table 120 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications

Table 121 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.3.5	Transmitter Specification
Table 4-9	2.5 and 5.0 GT/s Transmitter Specifications

Table 122 PCI Express Gen 3.0, 2.5 GT/s and 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications

Table 123 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 124 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.9	Data Rate Independent Tx Parameters
Table 8-8	Data Rate Independent Tx Parameters

Table 125 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.9	Data Rate Independent Tx Parameters
Table 8-8	Data Rate Independent Tx Parameters

Table 126 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 127 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

3 Sets up DC common mode voltage as follows:

   a Enables and displays common mode measurements.

   b Loads common mode signal to waveform memory.

   c Loads and enhance dynamic range D+ signal and D- signal.

   d Enables the average common mode measurement.

   e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).

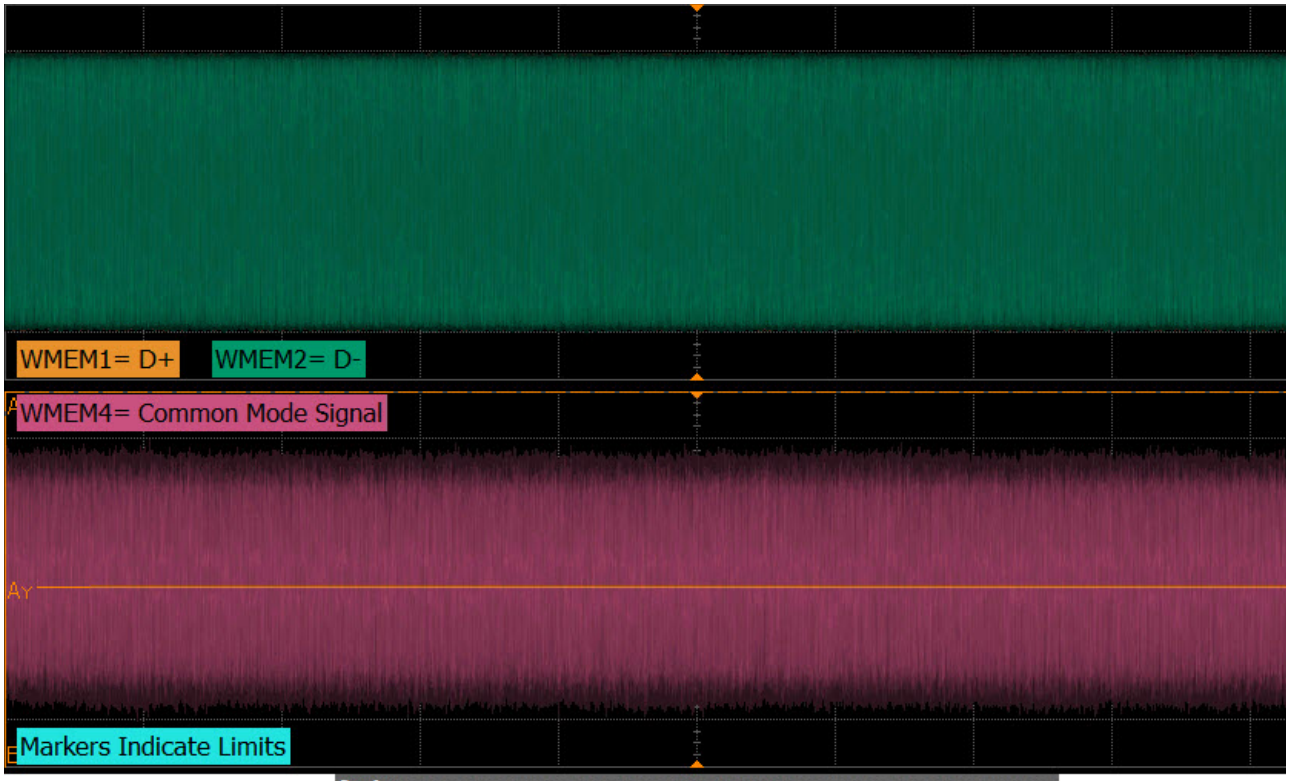
4 Measures the average value of D+ and D- signal.

5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.

6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the respective PCI Express Base Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Memory 1	40.00 µs/div	0.000s	84.13 mV/div	3.311 mV
Memory 2	40.00 µs/div	0.000s	81.25 mV/div	204.7 µV
Memory 4	40.00 µs/div	0.000s	13.75 mV/div	2.071 mV

Markers

	Source	X Position	Y Position
A	Memory 4	-1.00000000000000s	0.000000V
B	Memory 4	-1.00000000000000s	3.600000V

Figure 34 Avg DC Common Mode Output Voltage Test

DC Common Mode Output Voltage Variation Test

The **DC Common Mode Voltage** ($V_{TX\text{-}DC\text{-}CM}$) must be held at the same value during all states. The allowable range for $V_{TX\text{-}DC\text{-}CM}$ is 0 to 3.6 V (+/- 100mV).

The T_X DC Common Mode Output Voltage Variation measurement computes the worst case positive or negative excursion of the common mode signal from the average DC Common Mode Voltage $V_{TX\text{-}DC\text{-}CM}$.

$$V_{TX\text{-}DC\text{-}CM\text{-}VARIATION} = |Max\ (Max\ (V_{CM(i)}), Min\ (V_{CM(i)})) - V_{TX\text{-}DC\text{-}CM}\ |$$

Where:

'i' is the index of all waveform values.

'V_{CM}' is the common mode signal ($V_{TX\text{-}D+} + V_{TX\text{-}D-}$)/2.

Pass Limits

Table 128 Passing Limits Table for DC Common Mode Output Voltage Variation Test (Parameter: $V_{TX\text{-}DC\text{-}CM\text{-}VARIATION}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
All	Base - Transmitter Tests	2.5 GT/s	Clean Clock	100.00	PHY Electrical Test Consideration, Rev 1.0, Section 4.1.6
			SSC	100.00	PHY Electrical Test Consideration, Rev 1.0, Section 4.1.6
All	All Other	All Other	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 129 PCI Express Gen All, 2.5 GT/s References and Specification Notes

PCI Express™ PHY Electrical Test Consideration, Rev 1.0	
Section 4.1.6	Test 1.6 TX DC Common Mode Voltage

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Avg DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the average DC common mode output voltage test:

a Maximum common mode value

b Minimum common mode value

2 Finds the worst value between maximum common mode value and minimum common mode value.

3 Computes the DC common mode line delta by absolute the difference between average DC value of D+ and average DC value of D-.

4 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PHY Electrical Test Consideration.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Phase Jitter Test

Phase jitter is measured using the clock time interval error measurement with a bit error rate of 10^{-6}.

Pass Limits

Table 130 Passing Limits Table for Phase Jitter Test

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.1	Base - RefClk Tests	2.5 GT/s	Clean Clock	86.00	CEM Spec 1.1, Table 2-2
			SSC	86.00	CEM Spec 1.1, Table 2-2
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	86.00	CEM Spec 2.0, Table 2-2
			SSC	86.00	CEM Spec 2.0, Table 2-2
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	86.00	CEM Spec 3.0, Table 2-2
			SSC	86.00	CEM Spec 3.0, Table 2-2
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference

Table 130 Passing Limits Table for Phase Jitter Test

PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	86.00	CEM Spec 4.0, Section 2.1.5
			SSC	86.00	CEM Spec 4.0, Section 2.1.5
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 131 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 132 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ CEM Specification Revision 1.1	
Section 2.1.4	REFCLK Phase Jitter Specification
Table 2-2	Maximum Allowed Phase Jitter When Applied to Fixed Filter Characteristic

Table 133 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
Section 2.1.4	REFCLK Phase Jitter Specification For 2.5 GT/s Signaling Support
Table 2-2	Maximum Allowed Phase Jitter When Applied to Fixed Filter Characteristic

Table 134 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 135 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
Section 2.1.4	REFCLK Phase Jitter Specification For 2.5 GT/s Signaling Support
Table 2-2	Maximum Allowed Phase Jitter When Applied to Fixed Filter Characteristic

Table 136 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 137 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 138 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
Section 2.1.5	REFCLK Phase Jitter Specification for 2.5 GT/s, 5.0 306 GT/s, 8.0 GT/s and 16.0GT/s Signaling Support

Table 139 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 140 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 141 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.

2 Verifies that the signal period $\text{is} \sim 100MHz$.

3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

4 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

5 Configures **Memory Depth** to **20.0000Mpts** as **Manual** using **Acquisition Setup**.

6 Fits and displays all sample data on screen.

7 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.

8 Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 Gsa/s, clock rate 100 MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.

9 Stitches each acquired acquisition to make a continuous TIE data.

NOTE

You can use the **Stitch Method** configuration setting on scope to select the method used to stitch the waveform for the reference clock phase jitter test. The stitch method configuration setting applies only when the Spread Spectrum Clocking is enabled.

- Absolute - this method stitches the waveform based on absolute data.
- Dynamic - this method aligns waveform data to have common offset before stitching.

10 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:

a Converts time domain TIE data to frequency domain.

b Applies the PLL filter using parameters for common clocked architecture.

c Converts back the frequency domain TIE data to time domains.

d Computes the filtered peak-peak jitters.

11 Reports filtered peak-peak jitter as phase jitter and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

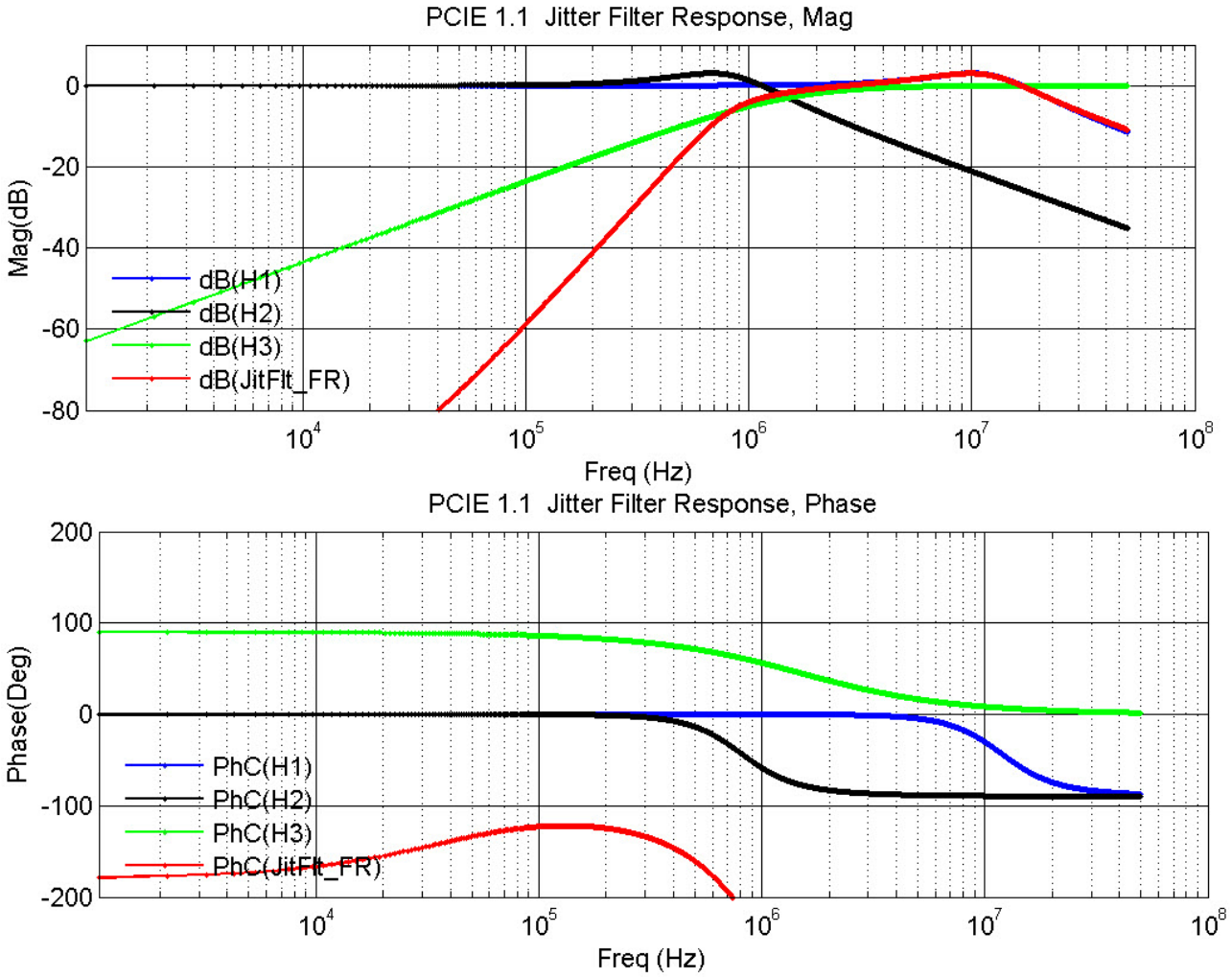


Figure 35 Reference Image for Jitter Filter Response

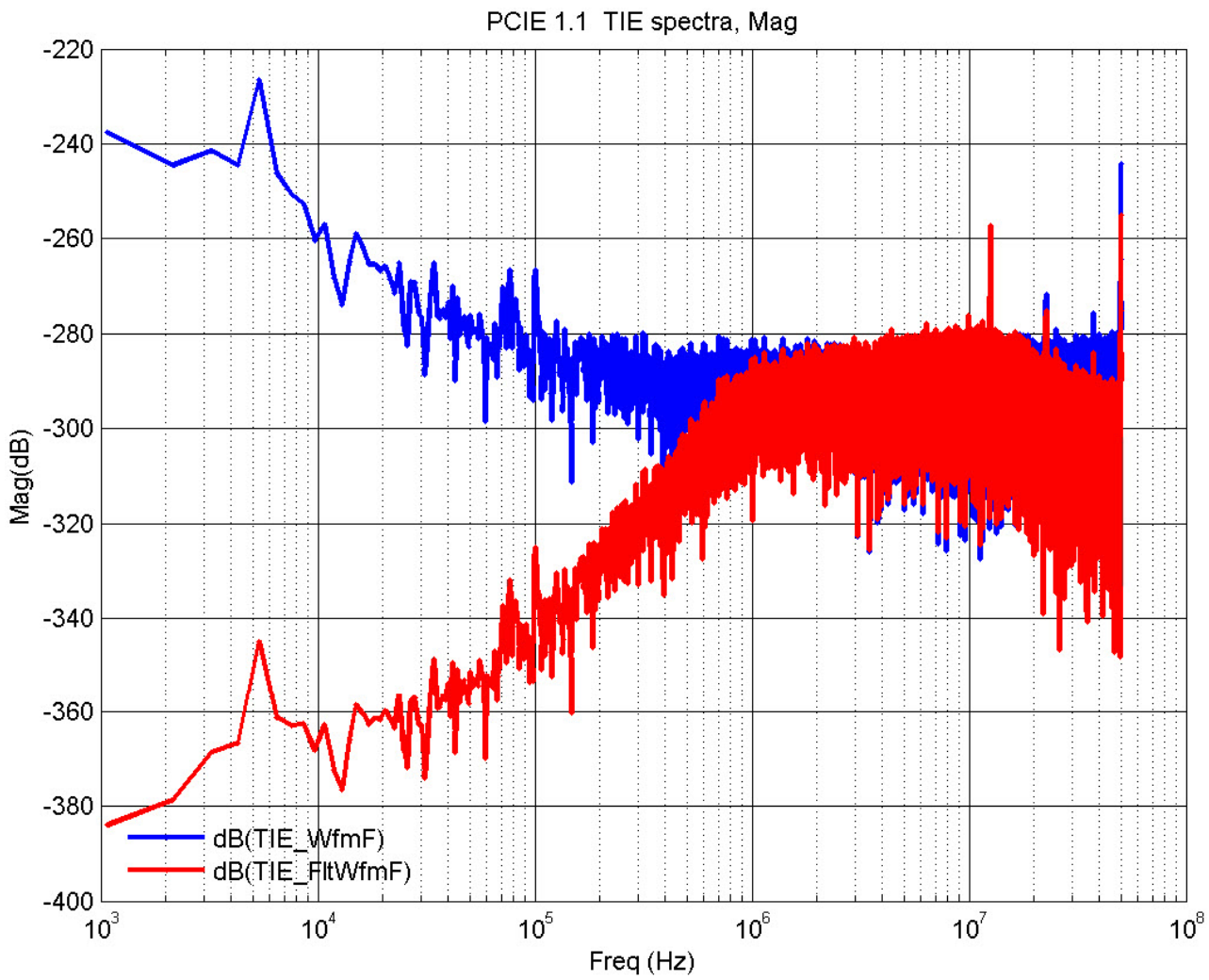


Figure 36 Reference Image for TIE Spectra, Mag

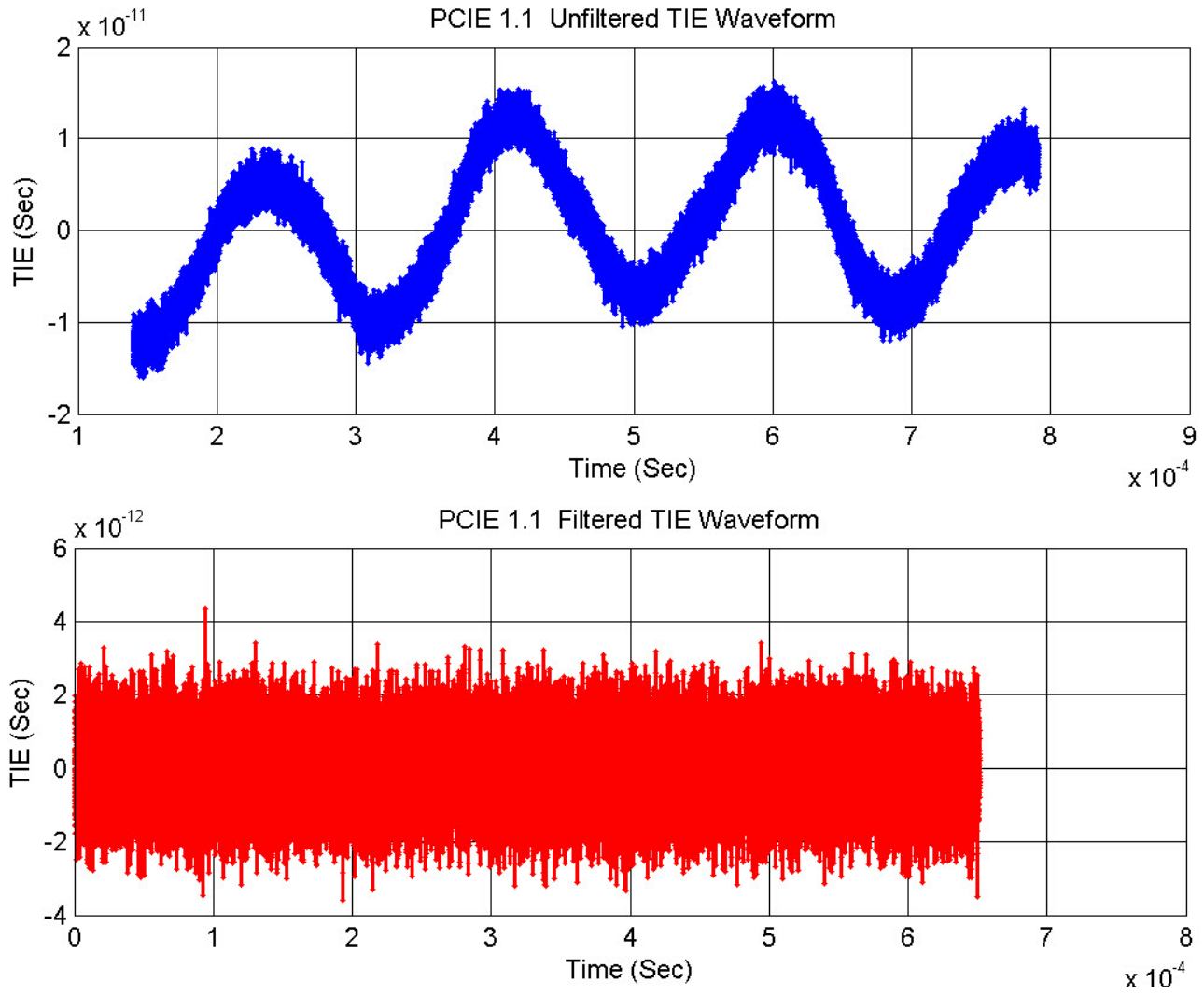


Figure 37 Reference Image for Unfiltered TIE Waveform

Rising Edge Rate Test

The rising edge rate test is measured from -150mV to +150mV on the differential waveform which is derived from RefClk+ minus RefClk-. The signal must be monotonic through the measurement region for rise time and 300mV measurement window is centered on the differential zero crossing.

Pass Limits

Table 142 Passing Limits Table for Rising Edge Rate Test (Parameter: Rising Edge Rate)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe1.1	Base - RefClk Tests	2.5 GT/s	Clean Clock	0.6 - 4.00	CEM Spec 1.1, Table 2-1
			SSC	0.6 - 4.00	CEM Spec 1.1, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe2.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	0.6 - 4.00	CEM Spec 2.0, Table 2-1
			SSC	0.6 - 4.00	CEM Spec 2.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe3.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	0.6 - 4.00	CEM Spec 3.0, Table 2-1
			SSC	0.6 - 4.00	CEM Spec 3.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference

Table 142 Passing Limits Table for Rising Edge Rate Test (Parameter: Rising Edge Rate)

PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe4.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	0.6 - 4.00	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
			SSC	0.6 - 4.00	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 143 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ CEM Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 144 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ CEM Specification Revision 1.1	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 145 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 146 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 147 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 148 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 149 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 150 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.2	REFCLK AC Specifications
Table 8-17	REFCLCK DC Specifications and AC Timing Requirements
PCI Express™ CEM Specification Revision 4.0	
Section 2.1.4	REFCLK AC Specifications

Table 151 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 152 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 153 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

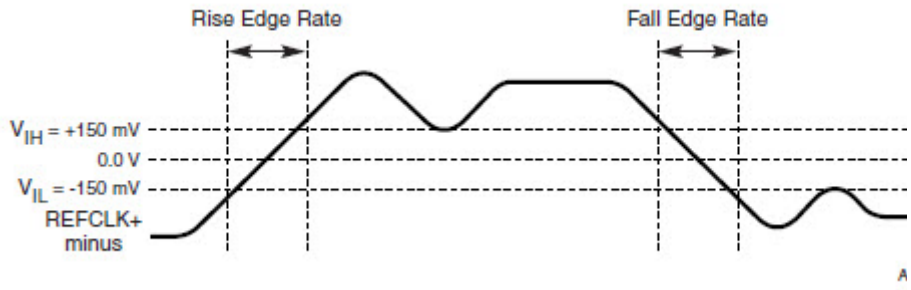


Figure 38 Differential Measurement Points for Rise and Fall Time

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.

2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

3 Fits and displays all sample data on screen.

4 Configures the **Top Level** threshold to 150mV and **Base Level** threshold to -150mV using **Threshold Setup**.

5 Measures the maximum rise time using **Rise time** measurement.

6 Zoom to maximum value of rise time.

7 Converts the maximum rise time to units of V/ns as given in the PCIE spec. [0.0000000003 / Maximum Rise Time value].

8 Reports the rising edge rate value and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

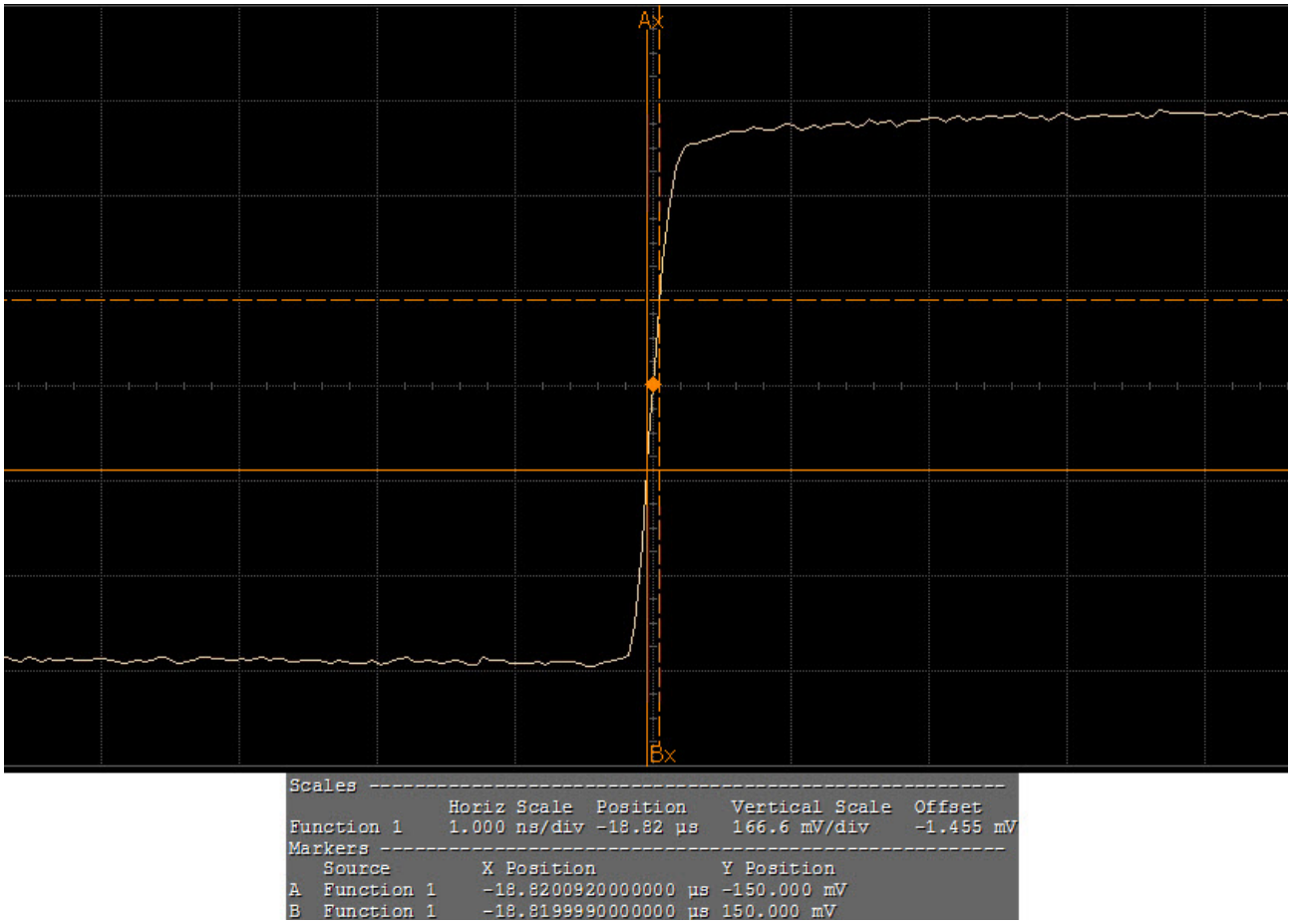


Figure 39 Reference Image for Rising Edge Rate

Falling Edge Rate Test

The falling edge rate test is measured from -150mV to +150mV on the differential waveform which is derived from RefClk+ minus RefClk-. The signal must be monotonic through the measurement region for fall time and 300mV measurement window is centered on the differential zero crossing.

Pass Limits

Table 154 Passing Limits Table for Falling Edge Rate Test (Parameter: Falling Edge Rate)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe1.1	Base - RefClk Tests	2.5 GT/s	Clean Clock	0.6 - 4.00	CEM Spec 1.1, Table 2-1
			SSC	0.6 - 4.00	CEM Spec 1.1, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe2.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	0.6 - 4.00	CEM Spec 2.0, Table 2-1
			SSC	0.6 - 4.00	CEM Spec 2.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe3.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	0.6 - 4.00	CEM Spec 3.0, Table 2-1
			SSC	0.6 - 4.00	CEM Spec 3.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference

Table 154 Passing Limits Table for Falling Edge Rate Test (Parameter: Falling Edge Rate)

PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe4.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	0.6 - 4.00	CEM Spec 1.1, Table 2-1
			SSC	0.6 - 4.00	CEM Spec 1.1, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V/ns) (Min) (Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 155 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ CEM Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 156 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ CEM Specification Revision 1.1	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 157 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 158 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 159 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 160 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 161 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 162 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.2	REFCLK AC Specifications
Table 8-17	REFCLCK DC Specifications and AC Timing Requirements
PCI Express™ CEM Specification Revision 4.0	
Section 2.1.4	REFCLK AC Specifications

Table 163 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 164 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 165 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

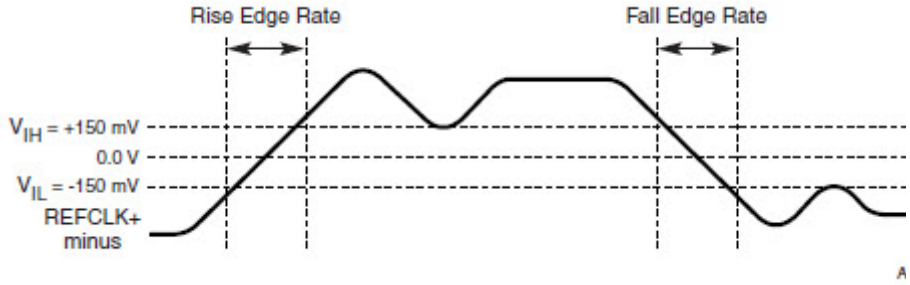


Figure 40 Differential Measurement Points for Rise and Fall Time

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.

2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

3 Fits and displays all sample data on screen.

4 Configures the **Top Level** threshold to 150mV and **Base Level** threshold to -150mV using **Threshold Setup**.

5 Measures the maximum fall time using **Fall time** measurement.

6 Zoom the resultant waveform to maximum value of fall time.

7 Converts the maximum fall time to units of V/ns as given in the PCIE specification [0.0000000003 / Maximum Fall Time value].

8 Reports the falling edge rate value and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

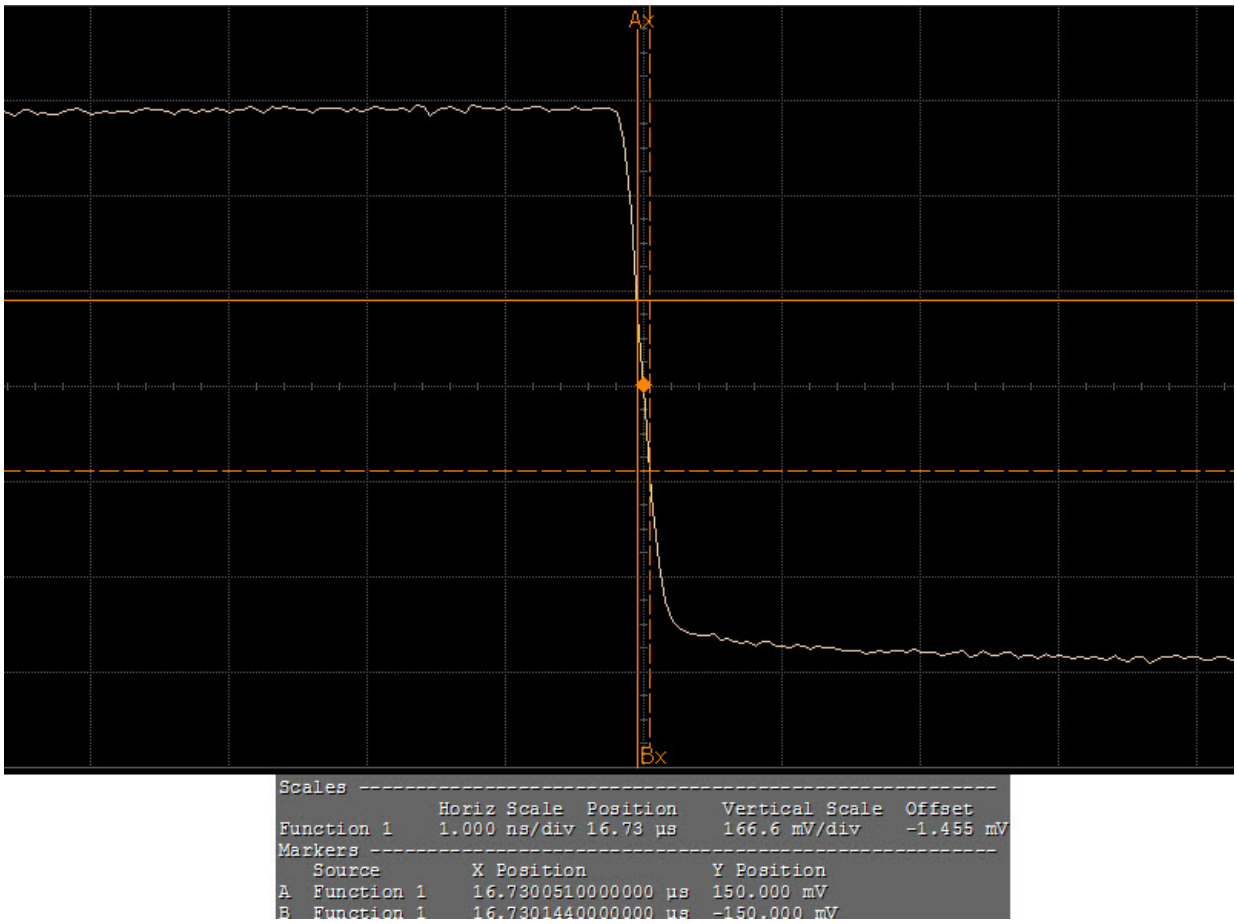


Figure 41 Reference Image for Falling Edge Rate

Differential Input High Voltage Test

The differential input high voltage test verifies that the reference clock differential input high voltage is within the conformance limits specified in Table 2-1 of the PCI Express CEM Specifications v1.1.

Pass Limits

Table 166 Passing Limits Table for Differential Input High Voltage Test (Parameter: V_{IH})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe1.1	Base - RefClk Tests	2.5 GT/s	Clean Clock	150.00	CEM Spec 1.1, Table 2-1
			SSC	150.00	CEM Spec 1.1, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe2.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	150.00	CEM Spec 2.0, Table 2-1
			SSC	150.00	CEM Spec 2.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe3.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	150.00	CEM Spec 3.0, Table 2-1
			SSC	150.00	CEM Spec 3.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference

Table 166 Passing Limits Table for Differential Input High Voltage Test (Parameter: V_{IH})

PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	150.00	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
			SSC	150.00	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 167 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ CEM Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 168 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ CEM Specification Revision 1.1	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 169 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 170 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 171 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 172 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 173 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 174 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.2	REFCLK AC Specifications
Table 8-17	REFCLCK DC Specifications and AC Timing Requirements
PCI Express™ CEM Specification Revision 4.0	
Section 2.1.4	REFCLK AC Specifications

Table 175 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 176 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 177 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.

2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

3 Fits and displays all sample data on screen.

4 Configures the **Top Level** threshold to 150mV and **Base Level** threshold to -150mV using **Threshold Setup**.

5 Measures the maximum voltage using **V max** measurement.

6 Reports the maximum voltage value as differential input high voltage and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

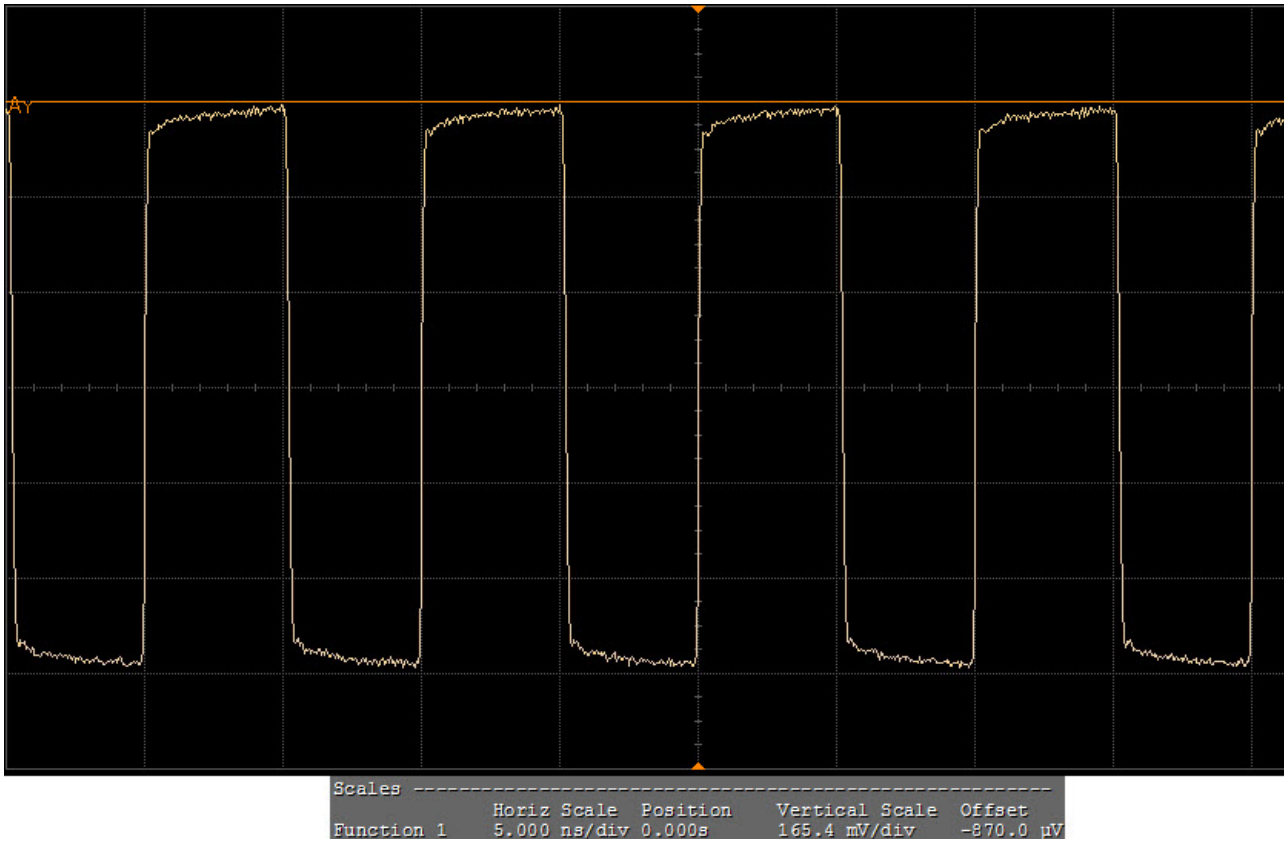


Figure 42 Reference Image for Differential Input High Voltage Test

Differential Input Low Voltage Test

The differential input low voltage test verifies that the reference clock differential input low voltage is within the conformance limits specified in the PCI Express Specifications.

Pass Limits

Table 178 Passing Limits Table for Differential Input Low Voltage Test (Parameter: V_{IL})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe1.1	Base - RefClk Tests	2.5 GT/s	Clean Clock	-150.00	CEM Spec 1.1, Table 2-1
			SSC	-150.00	CEM Spec 1.1, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe2.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	-150.00	CEM Spec 2.0, Table 2-1
			SSC	-150.00	CEM Spec 2.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe3.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	-150.00	CEM Spec 3.0, Table 2-1
			SSC	-150.00	CEM Spec 3.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference

Table 178 Passing Limits Table for Differential Input Low Voltage Test (Parameter: V_{IL})

PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	-150.00	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
			SSC	-150.00	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 179 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ CEM Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 180 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ CEM Specification Revision 1.1	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 181 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 182 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 183 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 184 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 185 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 186 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.2	REFCLK AC Specifications
Table 8-17	REFCLCK DC Specifications and AC Timing Requirements
PCI Express™ CEM Specification Revision 4.0	
Section 2.1.4	REFCLK AC Specifications

Table 187 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 188 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 189 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3. Fits and displays all sample data on screen.
4. Configures the **Top Level** threshold to 150mV and **Base Level** threshold to -150mV using **Threshold Setup**.
5. Measures the minimum voltage using **V min** measurement.
6. Reports the minimum voltage value as differential input low voltage and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

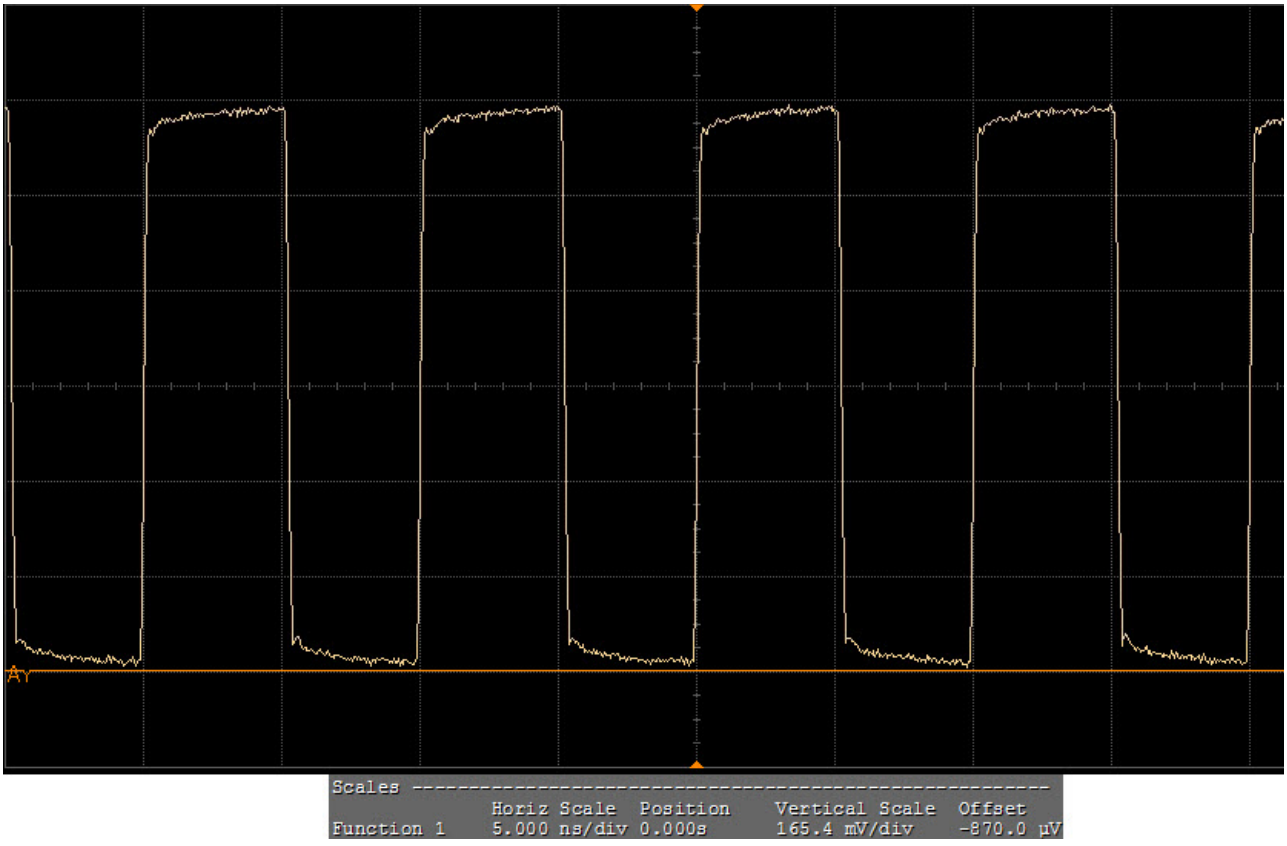


Figure 43 Reference Image for Differential Input Low Voltage Test

Average Clock Period Test

The average clock period accuracy of the differential waveform is measured in PPM (parts per million) where 1 PPM equals 100 Hz. A requirement of +/- 300 PPM applies to systems that do NOT employ SSC or that use a common clock source. For systems employing SSC there is an additional 2500 PPM nominal shift in the maximum period resulting in a maximum average period specification of +2800 PPM.

Pass Limits

Table 190 Passing Limits Table for Average Clock Period Test (Parameter: $T_{PERIOD\ AVG}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ppm) (Min/Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ppm) (Min/Max)	Reference
PCIe1.1	Base - RefClk Tests	2.5 GT/s	Clean Clock	-300/300	CEM Spec 1.1, Table 2-1
			SSC	-300/2800	CEM Spec 1.1, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ppm) (Min/Max)	Reference
PCIe2.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	-300/300	CEM Spec 2.0, Table 2-1
			SSC	-300/2800	CEM Spec 2.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ppm) (Min/Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ppm) (Min/Max)	Reference
PCIe3.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	-300/300	CEM Spec 3.0, Table 2-1
			SSC	-300/2800	CEM Spec 3.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 190 Passing Limits Table for Average Clock Period Test (Parameter: $T_{PERIOD\ AVG}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ppm) (Min/Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ppm) (Min/Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ppm) (Min/Max)	Reference
PCIe4.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	-300/300	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
			SSC	-300/2800	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ppm) (Min/Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ppm) (Min/Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ppm) (Min/Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 191 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ CEM Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 192 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ CEM Specification Revision 1.1	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 193 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 194 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 195 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 196 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 197 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 198 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.2	REFCLK AC Specifications
Table 8-17	REFCLCK DC Specifications and AC Timing Requirements
PCI Express™ CEM Specification Revision 4.0	
Section 2.1.4	REFCLK AC Specifications

Table 199 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 200 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 201 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.

2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

3 Configures **Memory Depth** to 10.0000Mpts as **Manual** using **Acquisition Setup**.

4 Fits and displays all sample data on screen.

5 Measures the average voltage using **V average** measurement.

6 Configures the **Top Level** threshold to +150mV and **Base Level** threshold to -150mV using **Threshold Setup**.

7 Measures the average frequency using **Frequency** measurement of **Clock**.

8 Measures the average period using **Period** measurement of **Clock**.

9 Computes the difference between ideal and actual frequency in terms of parts per million of 100MHz as follows:

$$\text{Difference between ideal and actual frequency} = [100MHz - AverageFrequency]/100$$

10 Reports the average clock period accuracy and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

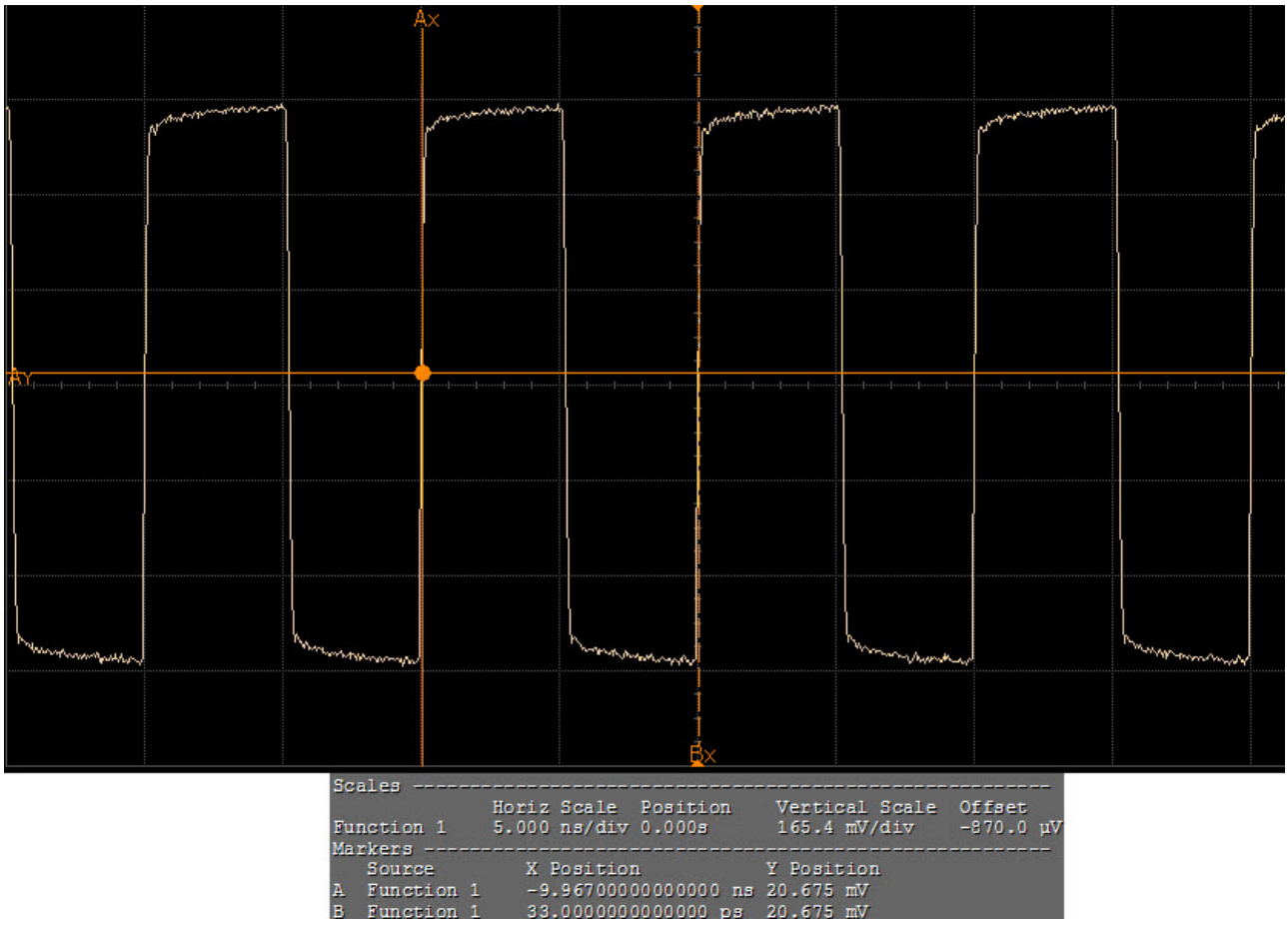


Figure 44 Reference Image for Average Clock Period

Duty Cycle Test

The duty cycle test verifies that the reference clock average clock period is within the conformance limits specified in Table 2-1 of the PCI Express CEM Specifications v1.1.

Pass Limits

Table 202 Passing Limits Table for Duty Cycle Test (Parameter: Duty Cycle)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe1.1	Base - RefClk Tests	2.5 GT/s	Clean Clock	40.0/60.0	CEM Spec 1.1, Table 2-1
			SSC	40.0/60.0	CEM Spec 1.1, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe2.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	40.0/60.0	CEM Spec 2.0, Table 2-1
			SSC	40.0/60.0	CEM Spec 2.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe3.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	40.0/60.0	CEM Spec 3.0, Table 2-1
			SSC	40.0/60.0	CEM Spec 3.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference

Table 202 Passing Limits Table for Duty Cycle Test (Parameter: Duty Cycle)

PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe4.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	40.0/60.0	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
			SSC	40.0/60.0	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 203 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ CEM Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 204 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ CEM Specification Revision 1.1	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 205 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 206 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 207 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 208 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 209 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 210 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.2	REFCLK AC Specifications
Table 8-17	REFCLCK DC Specifications and AC Timing Requirements
PCI Express™ CEM Specification Revision 4.0	
Section 2.1.4	REFCLK AC Specifications

Table 211 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 212 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 213 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.

2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

3 Configures **Memory Depth** to 10.0000 Mpts as **Manual** using **Acquisition Setup**.

4 Fits and displays all sample data on screen.

5 Measures the average voltage using **V average** measurement.

6 Configures the **Top Level** threshold to 150mV and **Base Level** threshold to -150mV using **Threshold Setup**.

7 Measures the duty cycle using the **Duty cycle** measurement.

8 Finds the margin for maximum duty cycle and minimum duty cycle.

9 Compares the margin and choose the largest margin to report the value (worst value) as duty cycle.

10 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

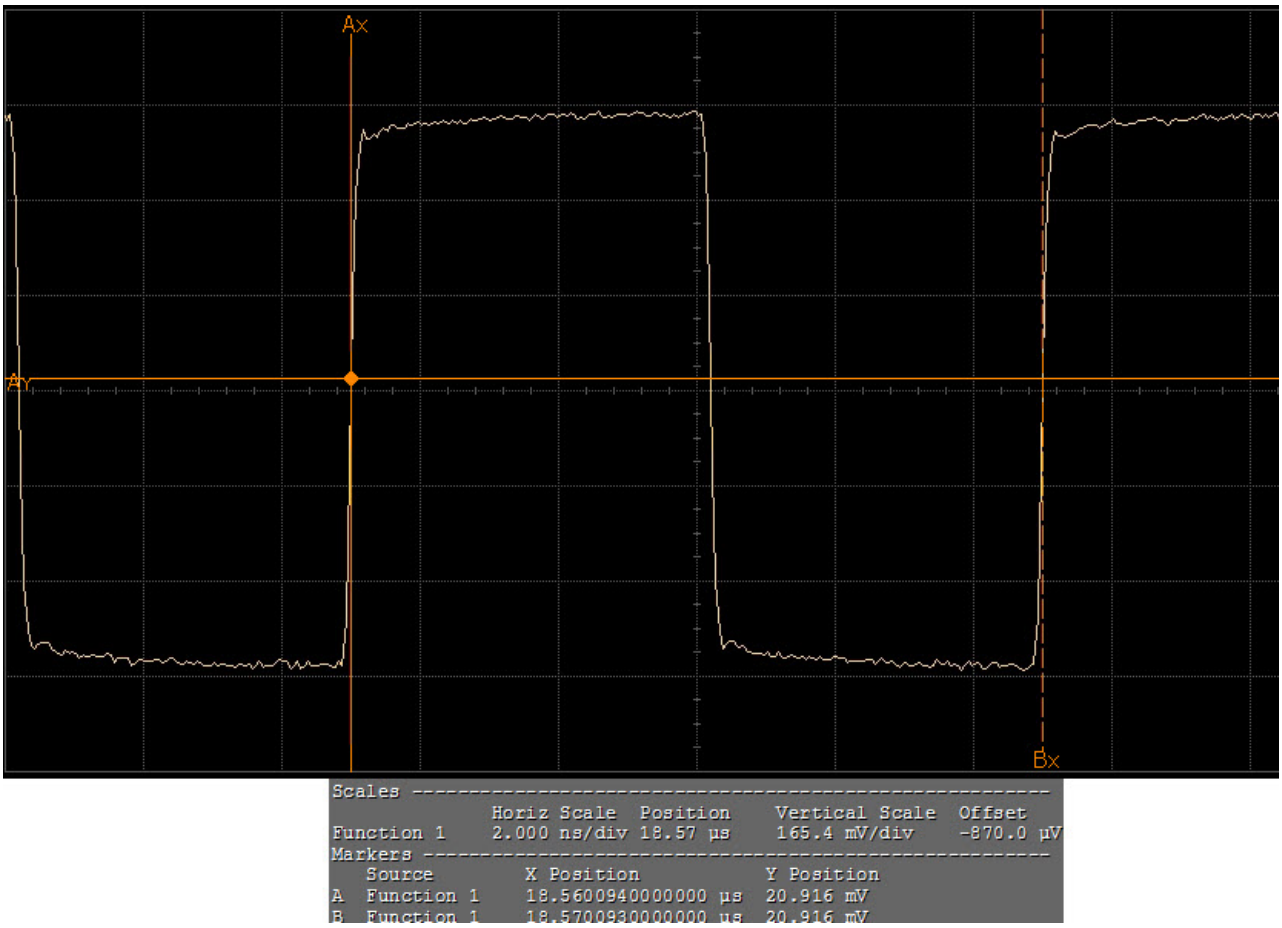


Figure 45 Reference Image for Duty Cycle

Absolute Crossing Point Voltage Test

The absolute crossing point voltage test is measured at crossing point where the instantaneous voltage value of the rising edge of RefClk+ equals the falling edge of RefClk-. It refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.

Pass Limits

Table 214 Passing Limits Table for Absolute Crossing Point Voltage Test (Parameter: V_{CROSS})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe1.1	Base - RefClk Tests	2.5 GT/s	Clean Clock	250/550	CEM Spec 1.1, Table 2-1
			SSC	250/550	CEM Spec 1.1, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe2.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	250/550	CEM Spec 2.0, Table 2-1
			SSC	250/550	CEM Spec 2.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe3.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	250/550	CEM Spec 3.0, Table 2-1
			SSC	250/550	CEM Spec 3.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference

Table 214 Passing Limits Table for Absolute Crossing Point Voltage Test (Parameter: V_{CROSS})

PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe4.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	250/550	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
			SSC	250/550	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 215 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ CEM Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 216 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ CEM Specification Revision 1.1	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 217 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 218 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 219 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 220 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 221 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 222 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.2	REFCLK AC Specifications
Table 8-17	REFCLCK DC Specifications and AC Timing Requirements
PCI Express™ CEM Specification Revision 4.0	
Section 2.1.4	REFCLK AC Specifications

Table 223 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 224 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 225 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

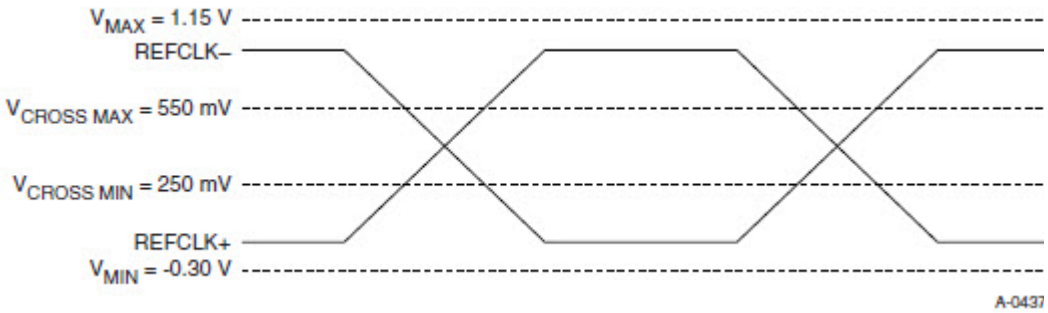


Figure 46 Single-Ended Measurement Points for Absolute Cross Point and Swing

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Uses MATLAB function to find the absolute crossing point voltage. The MATLAB function does the following:

   a Finds crossing edges for rising and falling edges.

   b Finds delta crossing for rising edge of RefClk+ and falling edge of RefClk-.

4 Computes the margin for minimum crossing point voltage and margin of maximum crossing point voltage.

5 Compares the margin and choose the smallest margin to report the value (worst value) as absolute crossing point voltage.

6 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Variation of V_{Cross} Test

The variation of V_{Cross} test is measured at crossing point where the instantaneous voltage value of the rising edge of Refclk+ equals the falling edge of Refclk-. It is defined as the total variation of all voltages of rising Refclk+ and falling Refclk-.

Pass Limits

Table 226 Passing Limits Table for Variation of V_{Cross} Test (Parameter: $V_{CROSS\ DELTA}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe1.1	Base - RefClk Tests	2.5 GT/s	Clean Clock	140.00	CEM Spec 1.1, Table 2-1
			SSC	140.00	CEM Spec 1.1, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe2.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	140.00	CEM Spec 2.0, Table 2-1
			SSC	140.00	CEM Spec 2.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe3.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	140.00	CEM Spec 3.0, Table 2-1
			SSC	140.00	CEM Spec 3.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference

Table 226 Passing Limits Table for Variation of V_{Cross} Test (Parameter: $V_{CROSS\ DELTA}$)

PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	140.00	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
			SSC	140.00	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 227 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ CEM Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 228 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ CEM Specification Revision 1.1	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 229 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 230 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 231 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 232 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 233 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 234 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.2	REFCLK AC Specifications
Table 8-17	REFCLCK DC Specifications and AC Timing Requirements
PCI Express™ CEM Specification Revision 4.0	
Section 2.1.4	REFCLK AC Specifications

Table 235 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 236 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 237 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

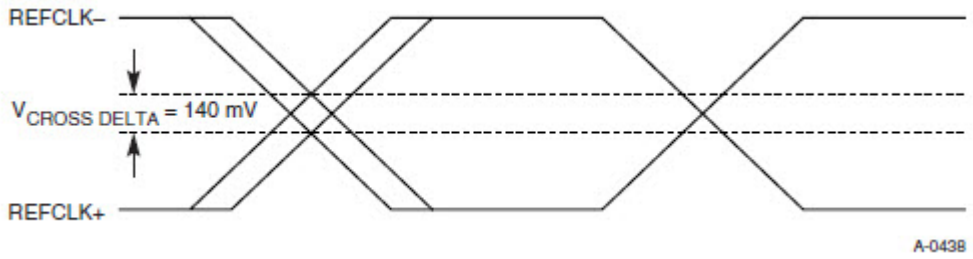


Figure 47 Single-Ended Measurement Points for Delta Cross Point

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the absolute crossing point voltage test.

1 Fits and displays all sample data on screen.
2 Uses MATLAB function to find the variation of V_{CROSS}. The MATLAB function does the following:
   a Finds crossing edges for rising and falling edges.
   b Finds delta crossing for rising edge of RefClk+ and falling edge of RefClk-.
3 Finds the differential value between maximum crossing rising edge and minimum crossing rising edge as variation of V_{Cross}.
4 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Max Input Voltage Test

The absolute max input voltage test verifies that the reference clock average clock period is within the conformance limits specified in Table 2-1 of the PCI Express CEM Specifications v1.1.

Pass Limits

Table 238 Passing Limits Table for Absolute Max Input Voltage Test (Parameter: V_{MAX})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe1.1	Base - RefClk Tests	2.5 GT/s	Clean Clock	1.150	CEM Spec 1.1, Table 2-1
			SSC	1.150	CEM Spec 1.1, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe2.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	1.150	CEM Spec 2.0, Table 2-1
			SSC	1.150	CEM Spec 2.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe3.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	1.150	CEM Spec 3.0, Table 2-1
			SSC	1.150	CEM Spec 3.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference

Table 238 Passing Limits Table for Absolute Max Input Voltage Test (Parameter: V_{MAX})

PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe4.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	1.150	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
			SSC	1.150	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 239 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ CEM Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 240 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ CEM Specification Revision 1.1	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 241 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 242 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 243 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 244 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 245 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 246 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.2	REFCLK AC Specifications
Table 8-17	REFCLCK DC Specifications and AC Timing Requirements
PCI Express™ CEM Specification Revision 4.0	
Section 2.1.4	REFCLK AC Specifications

Table 247 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 248 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 249 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

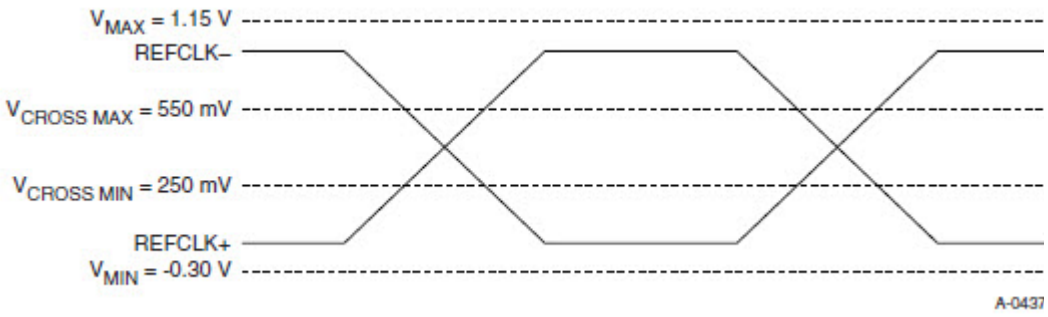


Figure 48 Single-Ended Measurement Points for Absolute Cross Point and Swing

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Configures the **Sample Rate** to 20GSa/s and **Memory Depth** to 10Mpts using **Acquisition Setup**.
3 Fits and displays all sample data on screen.
4 Turns on the **Measurement Analysis (EZJIT)** and checks **Measure All Edges**.
5 Measures the RefClk+ maximum voltage using **V max** measurement.
6 Measures the RefClk- maximum voltage using **V max** measurement.
7 Compares the RefClk+ maximum voltage and the RefClk- maximum voltage.
8 Reports the largest value (worst value) as the Absolute Max Input Voltage.
9 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

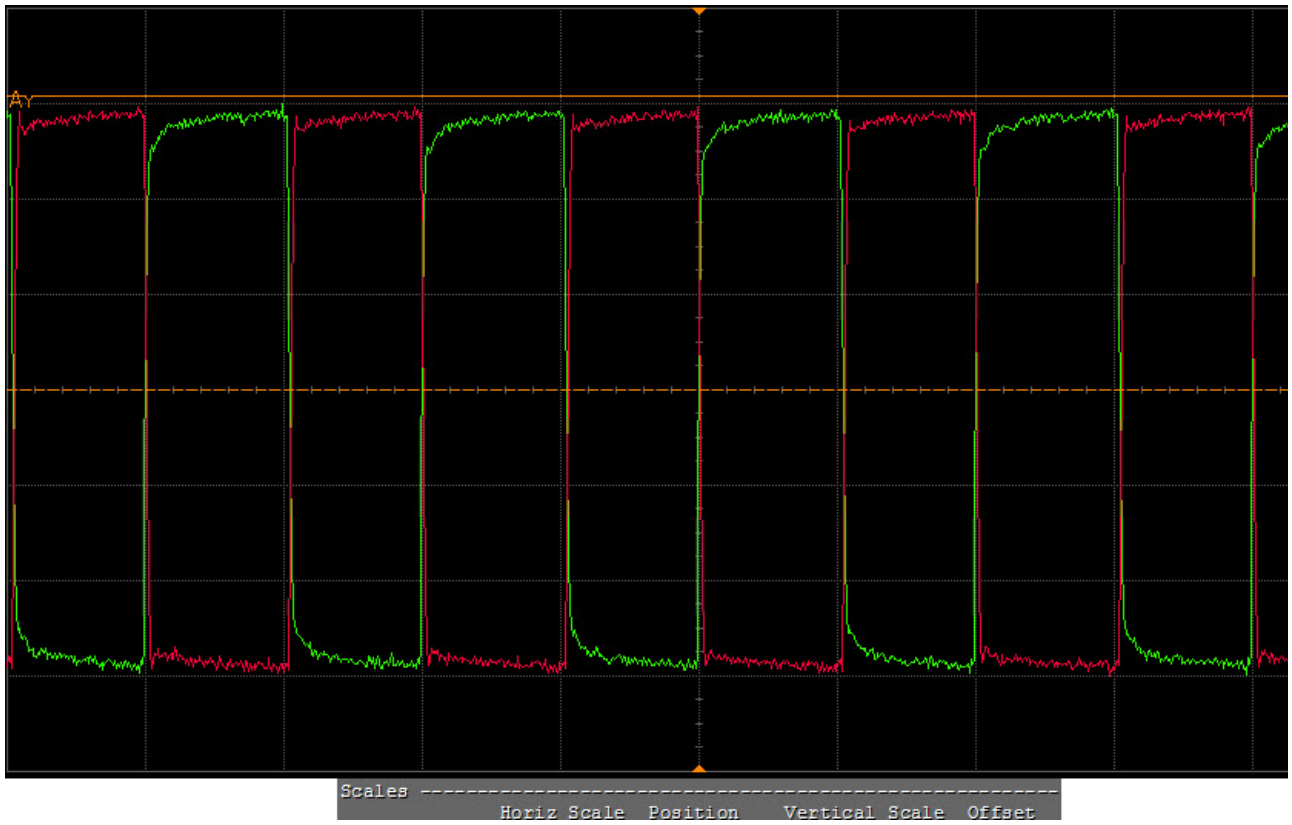


Figure 49 Reference Image for Absolute Max Input Voltage Test

Absolute Min Input Voltage Test

The absolute min input voltage test verifies that the reference clock average clock period is within the conformance limits specified in PCI Express CEM Specification.

Pass Limits

Table 250 Passing Limits Table for Absolute Min Input Voltage Test (Parameter: V_{MIN})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe1.1	Base - RefClk Tests	2.5 GT/s	Clean Clock	-300.00	CEM Spec 1.1, Table 2-1
			SSC	-300.00	CEM Spec 1.1, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe2.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	-300.00	CEM Spec 2.0, Table 2-1
			SSC	-300.00	CEM Spec 2.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe3.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	-300.00	CEM Spec 3.0, Table 2-1
			SSC	-300.00	CEM Spec 3.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference

Table 250 Passing Limits Table for Absolute Min Input Voltage Test (Parameter: V_{MIN})

PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe4.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	-300.00	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
			SSC	-300.00	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 251 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ CEM Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 252 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ CEM Specification Revision 1.1	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 253 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 254 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 255 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 256 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 257 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 258 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.2	REFCLK AC Specifications
Table 8-17	REFCLCK DC Specifications and AC Timing Requirements
PCI Express™ CEM Specification Revision 4.0	
Section 2.1.4	REFCLK AC Specifications

Table 259 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 260 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 261 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

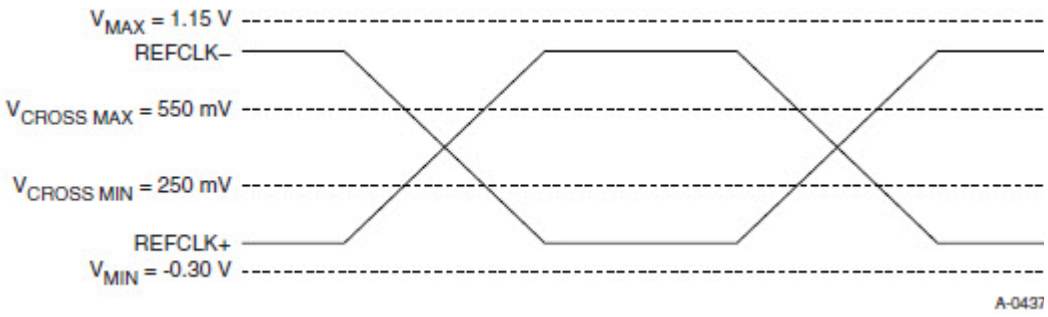


Figure 50 Single-Ended Measurement Points for Absolute Cross Point and Swing

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Configures the **Sample Rate** to 20 GSa/s and **Memory Depth** to 10 000 Mpts using **Acquisition Setup**.
3 Fits and displays all sample data on screen.
4 Turns on the **Measurement Analysis (EZJIT)** and checks **Measure All Edges**.
5 Measures the RefClk+ minimum voltage using **V min** measurement.
6 Measures the RefClk- minimum voltage using **V min** measurement.
7 Compares the RefClk+ minimum voltage and the RefClk- minimum voltage.
8 Reports the smallest value (worst value) as the Absolute Min Input Voltage.
9 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

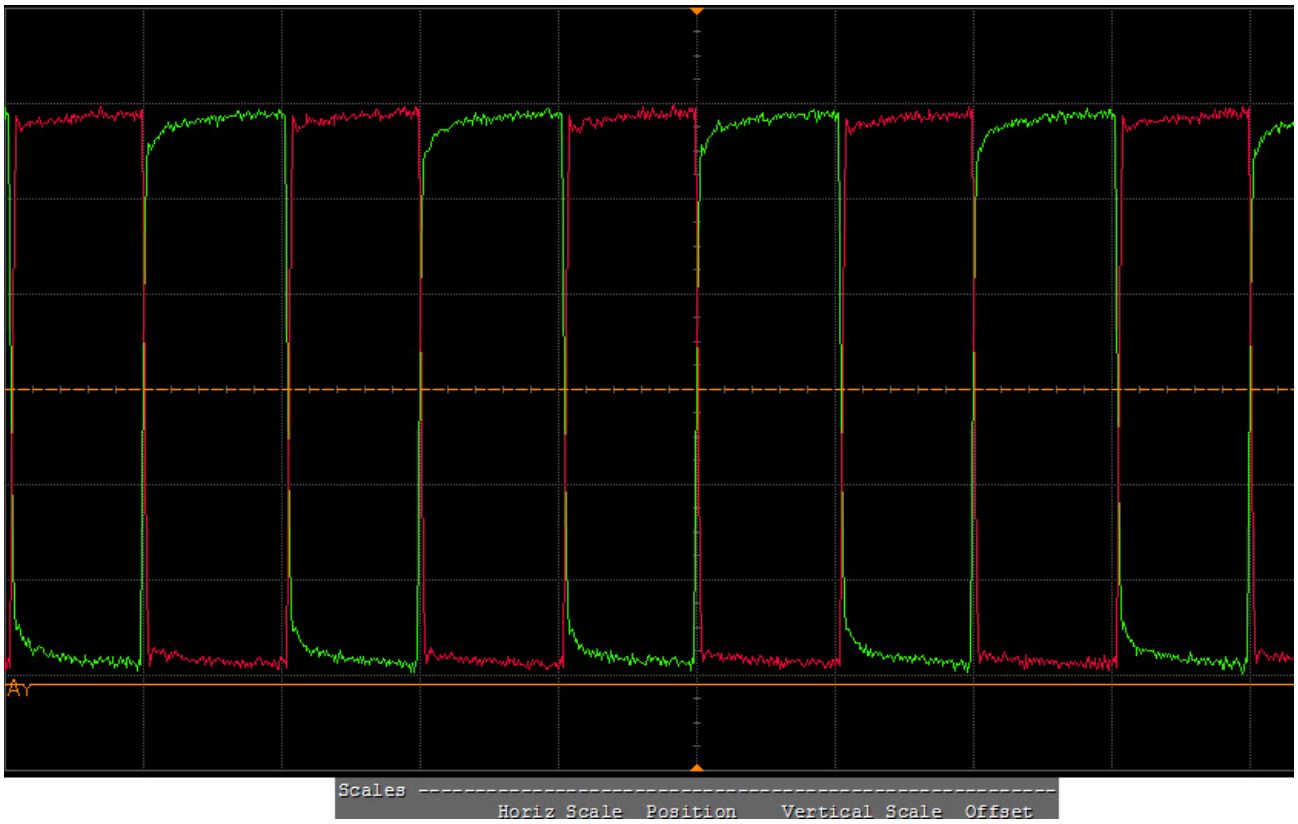


Figure 51 Reference Image for Absolute Min Input Voltage Test

Rise-Fall Matching Test

The rise-fall matching test matching applies to rising edge rate for RefClk+ and falling edge rate for RefClk-. It is measured using +/-75 mV window centered on the median cross point where RefClk+ rising meets RefClk- falling. The median cross point is used to calculate the voltage thresholds and oscilloscope is used to calculate the edge rate calculations. The rise edge rate of RefClk+ should be compared to the fall edge rate of RefClk-, the maximum allowed difference should not exceed 20% of the slowest edge rate.

Pass Limits

Table 262 Passing Limits Table for Rise-Fall Matching Test (Parameter: Rise-Fall Matching)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Max)	Reference
PCIe1.1	Base - RefClk Tests	2.5 GT/s	Clean Clock	20.00	CEM Spec 1.1, Table 2-1
			SSC	20.00	CEM Spec 1.1, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Max)	Reference
PCIe2.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	20.00	CEM Spec 2.0, Table 2-1
			SSC	20.00	CEM Spec 2.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Max)	Reference
PCIe3.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	20.00	CEM Spec 3.0, Table 2-1
			SSC	20.00	CEM Spec 3.0, Table 2-1
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 262 Passing Limits Table for Rise-Fall Matching Test (Parameter: Rise-Fall Matching)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Max)	Reference
PCIe4.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	20.00	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
			SSC	20.00	CEM Spec 4.0, Section 2.1.4 Base Spec 4.0, Table 8-17
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 263 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ CEM Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 264 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ CEM Specification Revision 1.1	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 265 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 266 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 267 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
Section 2.1.3	REFCLK AC Specifications
Table 2-1	REFCLCK DC Specifications and AC Timing Requirements

Table 268 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 269 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 270 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.2	REFCLK AC Specifications
Table 8-17	REFCLCK DC Specifications and AC Timing Requirements
PCI Express™ CEM Specification Revision 4.0	
Section 2.1.4	REFCLK AC Specifications

Table 271 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 272 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 273 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
N/A	N/A (Not Applicable)

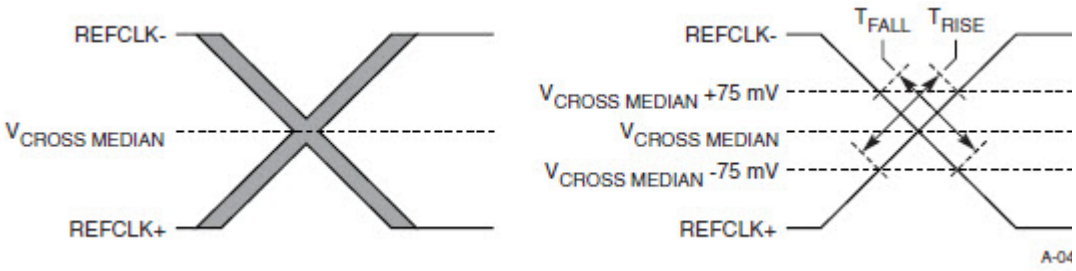


Figure 52 Single-Ended Measurement Points for Rise and Fall Time Matching

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the absolute crossing point voltage test.

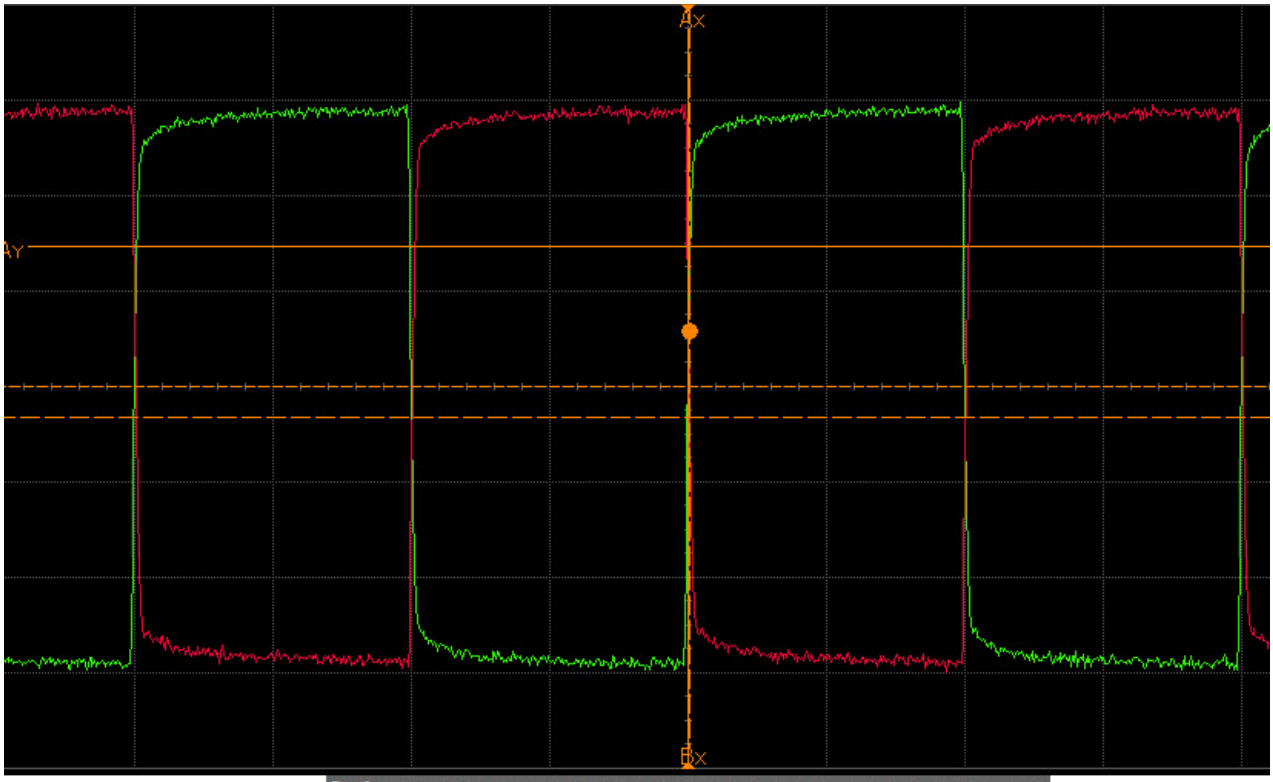
1 Configures the **Sample Rate** to 20 GSa/s and **Memory Depth** to 1 Mpts using **Acquisition Setup**.
2 Fits and displays all sample data on screen.
3 Sets the Middle Threshold by ([maximum crossing rising edge value +minimum crossing rising edge value] / 2).
4 Sets the **Upper Level** of **Custom Thresholds** as **Middle Level** of **Custom Thresholds** + 75 mV].
5 Sets the **Lower Level** of **Custom Thresholds** as **Middle Level** of **Custom Thresholds** - 75 mV].
6 Measures RefClk+ rise time using **Rise time** measurement.
7 Measures the RefClk- fall time using **Fall time** measurement.
8 Finds the slowest edge between RefClk+ rise time and RefClk- fall time.
9 Computes the Rise-Fall matching value as follows:

$$\text{.Rise-Fall Matching} = \frac{Abs|\text{RefClk+ rise time} - \text{RefClk- fall time}|}{\text{Slowest Edge Value} \times 100}$$

10 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Reference Image for Rise-Fall Matching

Peak to Peak Jitter (Common Clk) Test

This test verifies that the measured Peak to Peak jitter, TREFCLK-PP-CC, is less than the maximum allowed value.

Pass Limits

Table 274 Passing Limits Table for Peak to Peak Jitter (Common Clk) Test (Parameter: $T_{REFCLK-PP_CC}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - RefClk Tests	2.5 GT/s	Clean Clock	86.0	Base Spec 4.0, Table 8-22
			SSC	86.0	Base Spec 4.0, Table 8-22
	Base - RefClk Tests	All Other	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	All Other	All	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Max)	Reference
All Other	All	All	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 275 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 276 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 277 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 278 PCI Express Gen 3.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 279 PCI Express Gen 4.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.7	Jitter Limits for Refclk Architectures
Table 8-22	Jitter Limits for CC Architecture

Table 280 PCI Express Gen 4.0, All Other GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Verifies that the signal period is ~100 MHz.
3. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5. Configures **Memory Depth** to **50.0000 Mpts** as **Manual** using **Acquisition Setup**. If the desired option is not available, then it configures it to the highest available memory depth.
6. Fits and displays all sample data on the screen.
7. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8. Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 Gsa/s, clock rate 100 MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.
9. Stitches each acquired acquisition to make a continuous TIE data.
10. Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:
    - *a* Converts time domain TIE data to frequency domain.
    - *b* Applies the PLL filter using parameters for common clocked architecture.
    - *c* Converts back the frequency domain TIE data to time domains.
    - *d* Computes the filtered peak-peak jitters.
11. Reports filtered peak-peak jitter and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

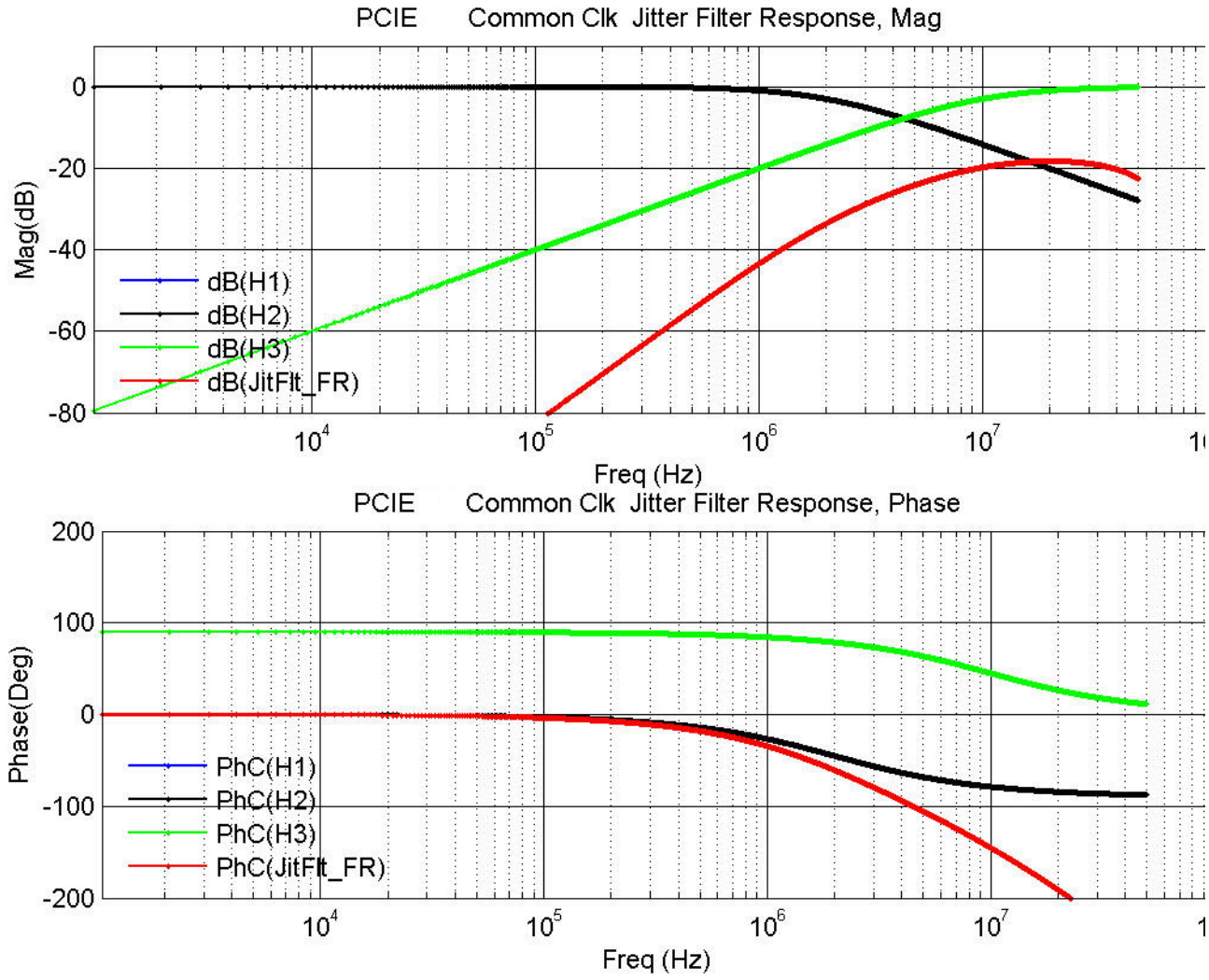


Figure 53 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

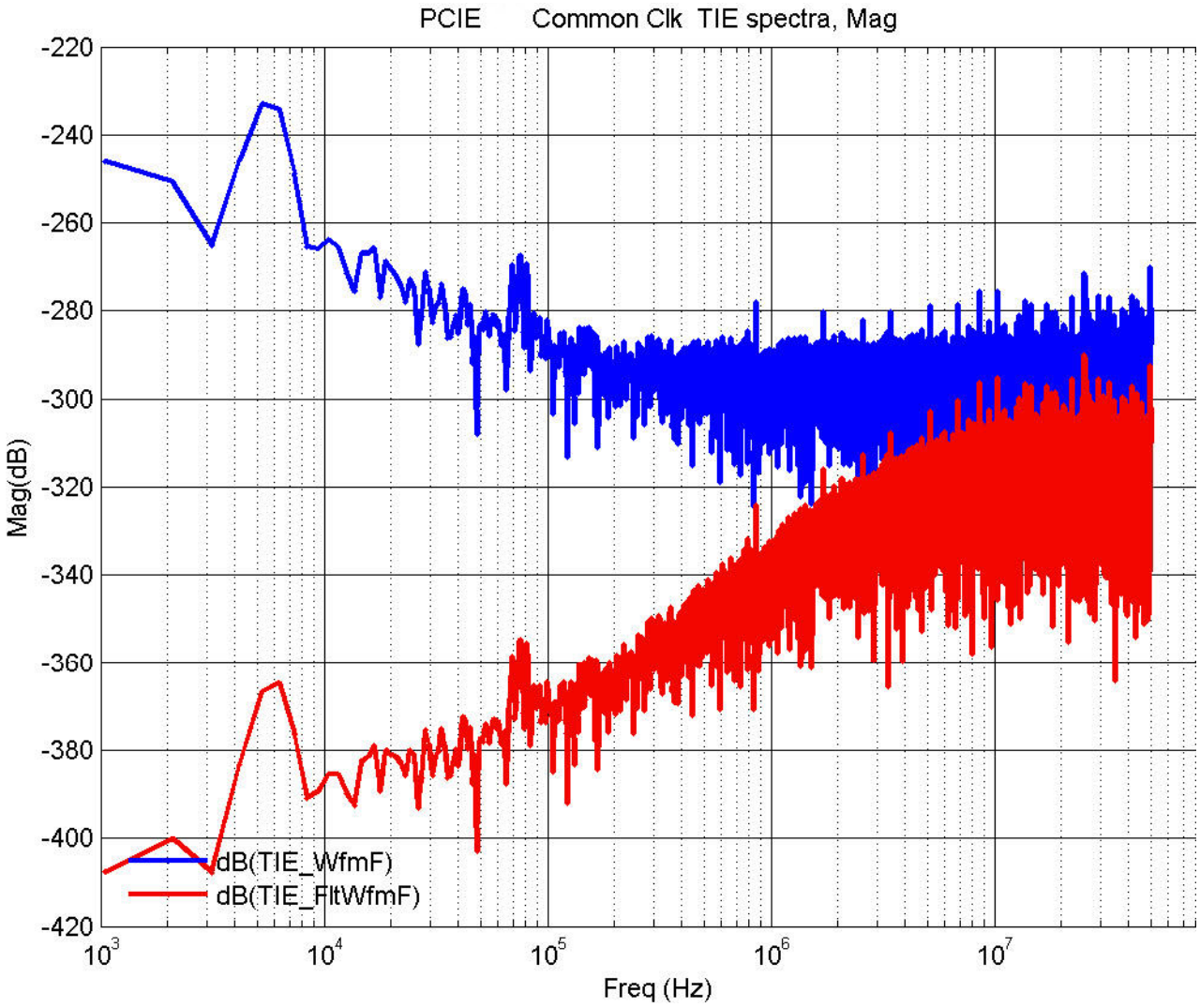


Figure 54 Reference Image for Common Clock TIE Spectra RMS Jitter Test

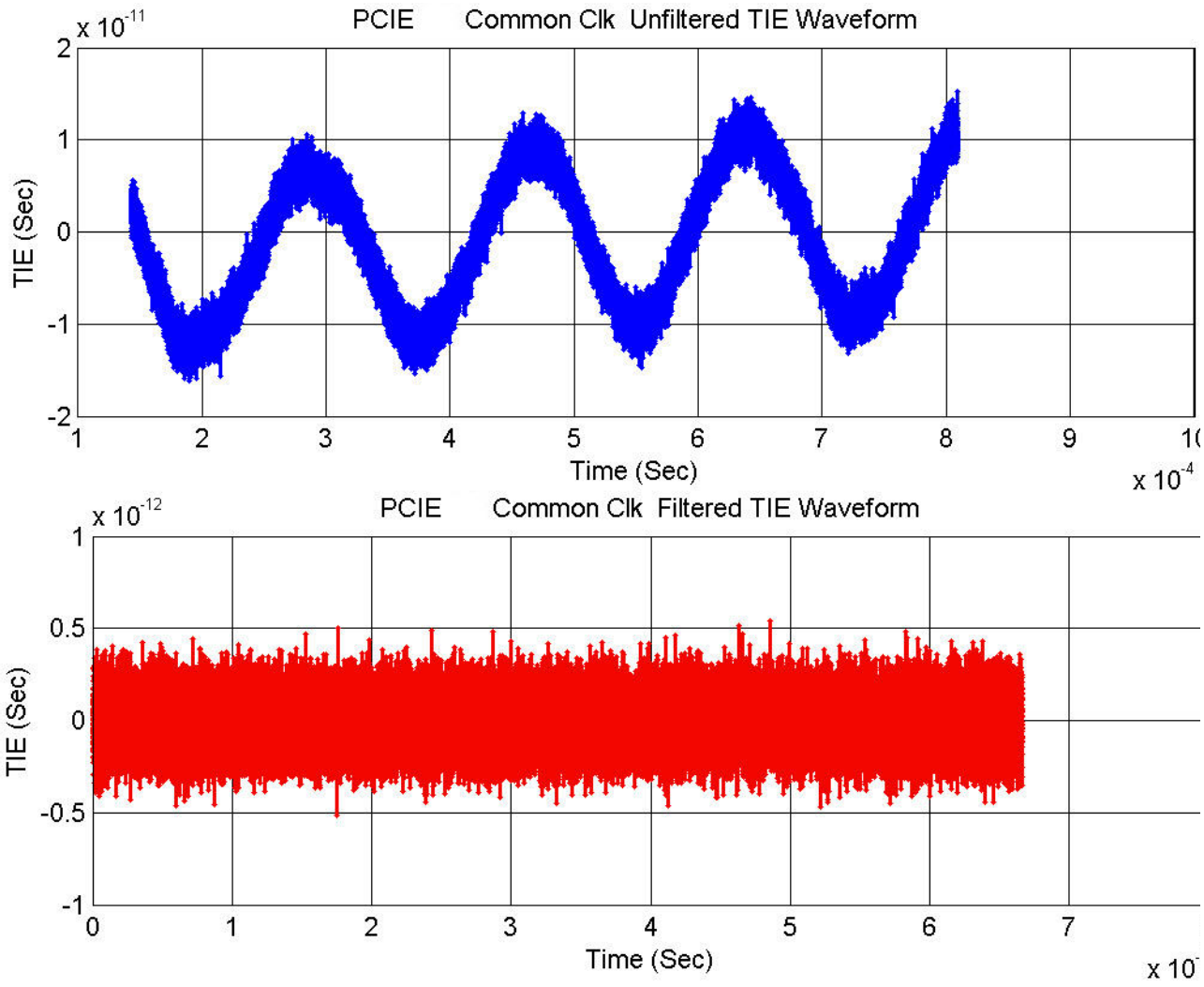


Figure 55 Reference Image for TIE Waveform RMS Jitter Test

AC Common Mode Voltage (1.25 GHz or 2.5 GHz LPF) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX\text{-}CM\text{-}AC\text{-}PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX\text{-}AC\text{-}CM\text{-}PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Pass Limits

Table 281 Passing Limits Table for AC Common Mode Voltage (1.25 or 2.5 GHz LPF) Test (Parameter: $V_{TX\text{-}CM\text{-}AC\text{-}PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe2.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	For 2.5 GHz: 100.00	Base Spec 2.0, Table 4-9
			SSC	For 2.5 GHz: 100.00	Base Spec 2.0, Table 4-9
	Base - Transmitter Tests	All Other	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	All Other	All	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe3.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	For 2.5 GHz: 150.00	Base Spec 3.0, Table 4-18
			SSC	For 2.5 GHz: 150.00	Base Spec 3.0, Table 4-18
	Base - Transmitter Tests	All Other	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	All Other	All	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 281 Passing Limits Table for AC Common Mode Voltage (1.25 or 2.5 GHz LPF) Test (Parameter: $V_{TX-CM-AC-PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits	Reference
PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	For 1.25 GHz: 150.00	Base Spec 4.0, Table 8-8
			SSC	For 1.25 GHz: 150.00	Base Spec 4.0, Table 8-8
	Base - Transmitter Tests	5.0 GT/s	Clean Clock	For 2.5 GHz: 150.00	Base Spec 4.0, Table 8-8
			SSC	For 2.5 GHz: 150.00	Base Spec 4.0, Table 8-8
	Base - Transmitter Tests	All Other	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	All Other	All	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 282 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 283 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 284 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 285 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.3.5	Transmitter Specifications
Table 4-9	2.5 and 5.0 GT/s Transmitter Specifications

Table 286 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 287 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications

Table 288 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 289 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 290 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.9	Data Rate Independent Tx Parameters
Table 8-8	Data Rate Independent Tx Parameters

Table 291 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 292 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Uses UDF LPF (Low Pass Filter) with cut off frequency of 1.25 or 2.5 GHz to the common mode signal.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

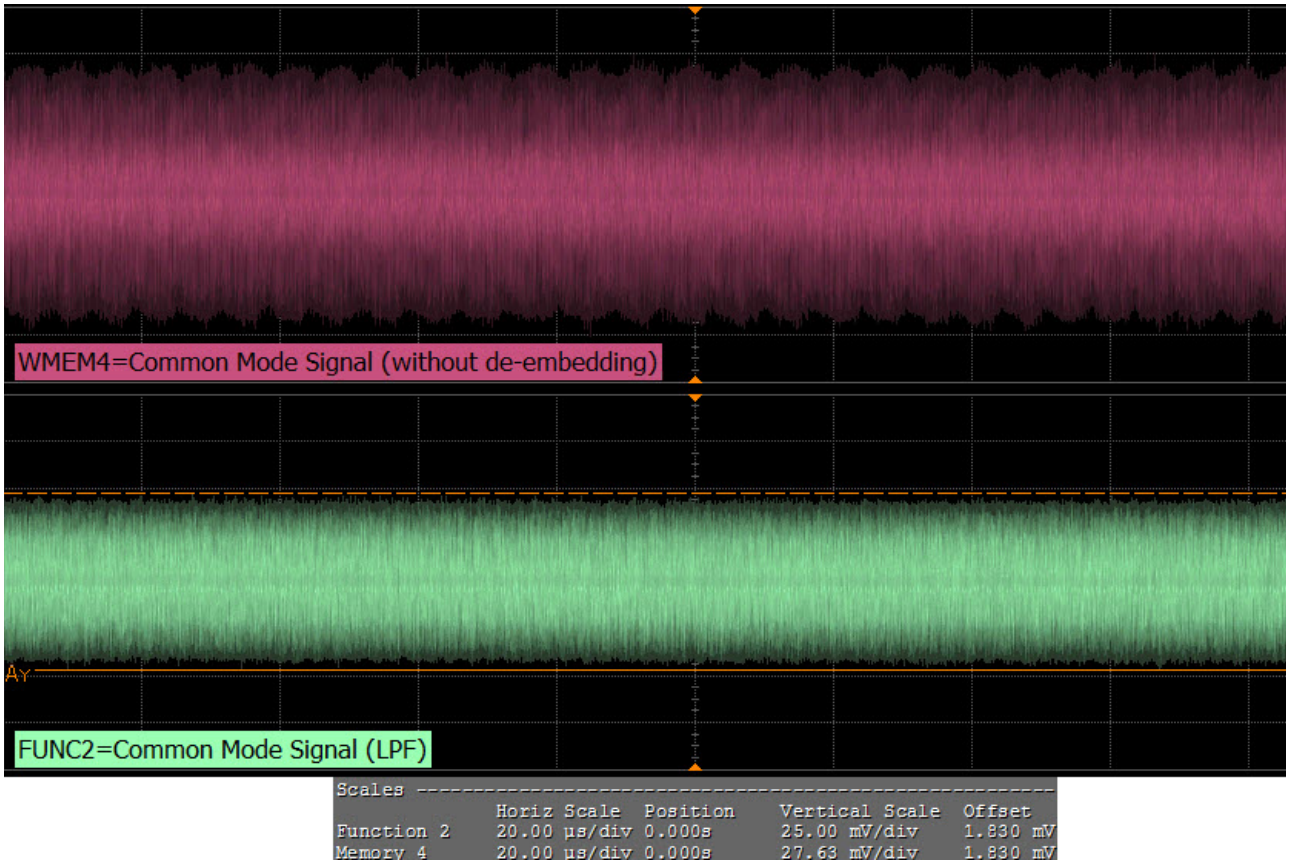


Figure 56 Reference Image for AC-CM voltage (4GHz LPF) Test

AC Common Mode Voltage (30 kHz to 500 MHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX\text{-}CM\text{-}AC\text{-}PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX\text{-}AC\text{-}CM\text{-}PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Pass Limits

Table 293 Passing Limits Table for AC Common Mode Voltage (30 kHz to 500 MHz) Test (Parameter: $V_{TX\text{-}CM\text{-}AC\text{-}PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe2.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	0.00/100.00	Base Spec 2.0, Table 4-9
			SSC	0.00/100.00	Base Spec 2.0, Table 4-9
	Base - Transmitter Tests	All Other	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	All Other	All	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe3.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	0.00/100.00	Base Spec 3.0, Table 4-18
			SSC	0.00/100.00	Base Spec 3.0, Table 4-18
	Base - Transmitter Tests	8.0 GT/s	Clean Clock	0.00/50.00	Base Spec 3.0, Table 4-18
			SSC	0.00/50.00	Base Spec 3.0, Table 4-18
	Base - Transmitter Tests	All Other	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	All Other	All	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 293 Passing Limits Table for AC Common Mode Voltage (30 kHz to 500 MHz) Test (Parameter: $V_{TX\text{-}CM\text{-}AC\text{-}PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	0.00/100.00	Base Spec 4.0, Table 8-8
			SSC	0.00/100.00	Base Spec 4.0, Table 8-8
	Base - Transmitter Tests	8.0 GT/s	Clean Clock	0.00/50.00	Base Spec 4.0, Table 8-8
			SSC	0.00/50.00	Base Spec 4.0, Table 8-8
	Base - Transmitter Tests	16.0 GT/s	Clean Clock	0.00/50.00	Base Spec 4.0, Table 8-8
			SSC	0.00/50.00	Base Spec 4.0, Table 8-8
	Base - Transmitter Tests	All Other	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	All Other	All	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 294 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 295 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 296 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 297 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.3.5	Transmitter Specifications
Table 4-9	2.5 and 5.0 GT/s Transmitter Specifications

Table 298 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 299 PCI Express Gen 3.0, 5.0 and 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications

Table 300 PCI Express Gen 4.0, Data Rate 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 301 PCI Express Gen 4.0, Data Rate 5.0, 8.0, and 16.0 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.9	Data Rate Independent Tx Parameters
Table 8-8	Data Rate Independent Tx Parameters

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the AC-CM Voltage (4GHz LPF) test.

1 Gets PCIE3 compliance signal.
2 Uses MATLAB function (BandPassFilter) to filter the signal with cutoff frequency of 30 KHz and 500 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}\ of\ |V_{TX\text{-}D+} + V_{TX\text{-}D\text{-}}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}\ of\ |V_{TX\text{-}D+} + V_{TX\text{-}D\text{-}}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Pass Limits

Table 302 Passing Limits Table for Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test (Parameter: $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE_IDLE\text{-}DELTA}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	**Test Point**	**Data Rate**	**Ref. Clock**	**Pass Limits (mV)**	**Reference**
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	**Test Point**	**Data Rate**	**Ref. Clock**	**Pass Limits (mV) (Max)**	**Reference**
PCIe2.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	0.00/100.00	Base Spec 2.0, Table 4-9
			SSC	0.00/100.00	Base Spec 2.0, Table 4-9
	Base - Transmitter Tests	5.0 GT/s	Clean Clock	0.00/100.00	Base Spec 2.0, Table 4-9
			SSC	0.00/100.00	Base Spec 2.0, Table 4-9
	Base - Transmitter Tests	All Other	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	All Other	All	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	**Test Point**	**Data Rate**	**Ref. Clock**	**Pass Limits (mV) (Max)**	**Reference**
PCIe3.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	0.00/100.00	Base Spec 3.0, Table 4-18
			SSC	0.00/100.00	Base Spec 3.0, Table 4-18
	Base - Transmitter Tests	5.0 GT/s	Clean Clock	0.00/100.00	Base Spec 3.0, Table 4-18
			SSC	0.00/100.00	Base Spec 3.0, Table 4-18

Table 302 Passing Limits Table for Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test (Parameter: $V_{TX-CM-DC-ACTIVE_IDLE-DELTA}$)

	Base - Transmitter Tests	8.0 GT/s	Clean Clock	0.00/100.00	Base Spec 3.0, Table 4-18
			SSC	0.00/100.00	Base Spec 3.0, Table 4-18
	Base - Transmitter Tests	All Other	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	All Other	All	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	0.00/100.00	Base Spec 4.0, Table 8-8
			SSC	0.00/100.00	Base Spec 4.0, Table 8-8
	Base - Transmitter Tests	5.0 GT/s	Clean Clock	0.00/100.00	Base Spec 4.0, Table 8-8
			SSC	0.00/100.00	Base Spec 4.0, Table 8-8
	Base - Transmitter Tests	8.0 GT/s	Clean Clock	0.00/100.00	Base Spec 4.0, Table 8-8
			SSC	0.00/100.00	Base Spec 4.0, Table 8-8
	Base - Transmitter Tests	16.0 GT/s	Clean Clock	0.00/100.00	Base Spec 4.0, Table 8-8
			SSC	0.00/100.00	Base Spec 4.0, Table 8-8
	Base - Transmitter Tests	All Other	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	All Other	All	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 303 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 304 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 305 PCI Express Gen 2.0, Data Rate 2.5 and 5.0 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.3.5	Transmitter Specifications
Table 4-9	2.5 and 5.0 GT/s Transmitter Specifications

Table 306 PCI Express Gen 3.0, Data Rate 2.5, 5.0, and 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications

Table 307 PCI Express Gen 4.0, Data Rate 2.5, 5.0, 8.0, and 16.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.9	Data Rate Independent Tx Parameters
Table 8-8	Data Rate Independent Tx Parameters

Understanding the Test Flow

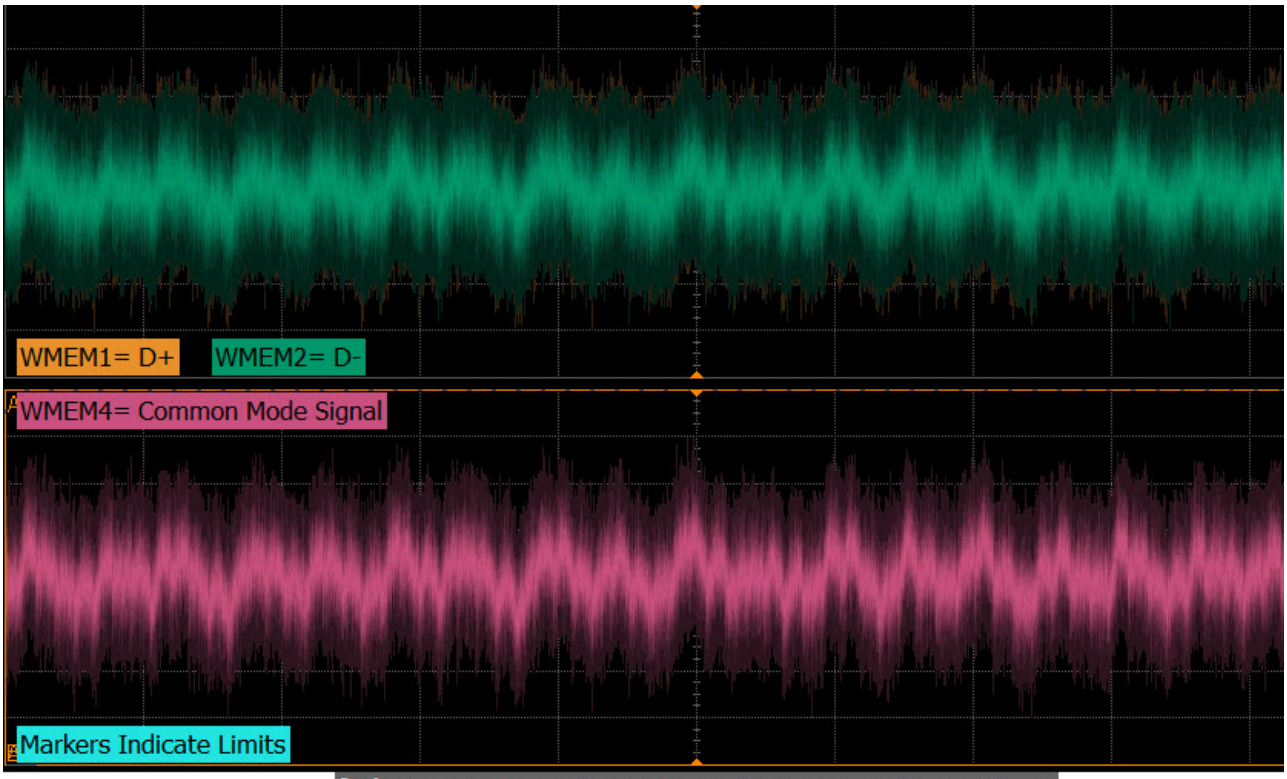
The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Memory 1	20.00 µs/div	0.000s	787.5 µV/div	2.755 mV
Memory 2	20.00 µs/div	0.000s	762.5 µV/div	8.203 mV
Memory 4	20.00 µs/div	0.000s	582.5 µV/div	5.479 mV

Markers

	Source	X Position	Y Position
A	Memory 4	-1.00000000000000s	0.000000V
B	Memory 4	-1.00000000000000s	3.600000V

Figure 57 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Pass Limits

Table 308 Passing Limits Table for DC Common-Mode Voltage Test (Parameter: $V_{TX\text{-}CM\text{-}DC}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe2.0	All	All	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	0.00/3.60	Base Spec 3.0, Table 4-18
			SSC	0.00/3.60	Base Spec 3.0, Table 4-18

Table 308 Passing Limits Table for DC Common-Mode Voltage Test (Parameter: $V_{TX-CM-DC}$)

	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	0.00/3.60	Base Spec 4.0, Table 8-8
			SSC	0.00/3.60	Base Spec 4.0, Table 8-8
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	0.00/3.60	Base Spec 4.0, Table 8-8
			SSC	0.00/3.60	Base Spec 4.0, Table 8-8
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 309 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 310 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 311 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 312 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 313 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 314 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 315 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications

Table 316 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 317 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 318 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.9	Data Rate Independent Tx Parameters
Table 8-8	Data Rate Independent Tx Parameters

Table 319 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.9	Data Rate Independent Tx Parameters
Table 8-8	Data Rate Independent Tx Parameters

Understanding the Test Flow

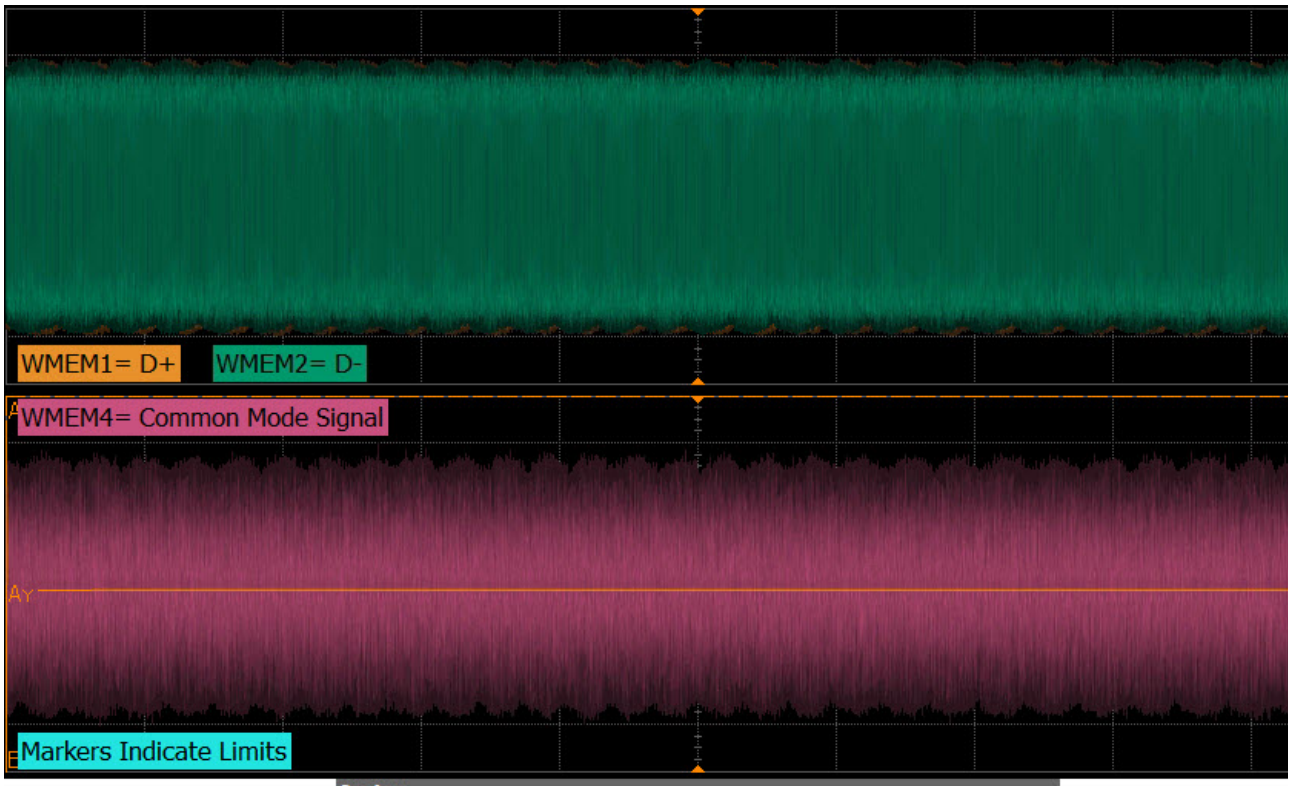
The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Sets up DC common mode voltage as follows:
   a Enables and displays common mode measurements.
   b Loads common mode signal to waveform memory.
   c Loads and enhance dynamic range D+ signal and D- signal.
   d Enables the average common mode measurement.
   e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).
4 Measures the average value of D+ and D- signal.
5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.
6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the respective PCI Express Base Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Memory 1	20.00 µs/div	0.000s	106.0 mV/div	8.610 mV
Memory 2	20.00 µs/div	0.000s	91.25 mV/div	1.475 mV
Memory 4	20.00 µs/div	0.000s	26.75 mV/div	3.600 mV

Markers

	Source	X Position	Y Position
A	Memory 4	-1.00000000000000s	0.000000V
B	Memory 4	-1.00000000000000s	3.600000V

Figure 58 Reference Image for DC Common Mode Voltage Test

AC Common-Mode Voltage (4 GHz or 8 GHz LPF) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX\text{-}CM\text{-}AC\text{-}PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX\text{-}AC\text{-}CM\text{-}PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Pass Limits

Table 320 Passing Limits Table for AC Common-Mode Voltage (4 or 8 GHz LPF) Test (Parameter: $V_{TX\text{-}CM\text{-}AC\text{-}PP}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe2.0	All	All	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference

Table 320 Passing Limits Table for AC Common-Mode Voltage (4 or 8 GHz LPF) Test (Parameter: $V_{TX-CM-AC-PP}$)

PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	For 4 GHz: 0.00/150 For 8 GHz: N/A	For 4 GHz: Base Spec 3.0, Table 4-18 For 8 GHz: N/A
			SSC	For 4 GHz: 0.00/150 For 8 GHz: N/A	For 4 GHz: Base Spec 3.0, Table 4-18 For 8 GHz: N/A
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	For 4 GHz: 0.00/150 For 8 GHz: N/A	For 4 GHz: Base Spec 4.0, Table 8-8 For 8 GHz: N/A
			SSC	For 4 GHz: 0.00/150 For 8 GHz: N/A	For 4 GHz: Base Spec 4.0, Table 8-8 For 8 GHz: N/A
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min/Max)	Reference

Table 320 Passing Limits Table for AC Common-Mode Voltage (4 or 8 GHz LPF) Test (Parameter: $V_{TX-CM-AC-PP}$)

PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	For 4 GHz: N/A	For 4 GHz: N/A (Not Applicable)
				For 8 GHz: 0.00/150	For 8 GHz: Base Spec 4.0, Table 8-8
			SSC	For 4 GHz: N/A	For 4 GHz: N/A (Not Applicable)
				For 8 GHz: 0.00/150	For 8 GHz: Base Spec 4.0, Table 8-8
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 321 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 322 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 323 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 324 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 325 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 326 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 327 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications

Table 328 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 329 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 330 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.9	Data Rate Independent Tx Parameters
Table 8-8	Data Rate Independent Tx Parameters

Table 331 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.9	Data Rate Independent Tx Parameters
Table 8-8	Data Rate Independent Tx Parameters

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3. Uses UDF LPF (Low Pass Filter) with cut off frequency of 4 GHz or 8 GHz to the common mode signal.
4. Measures the VPP of the filtered signal.
5. Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

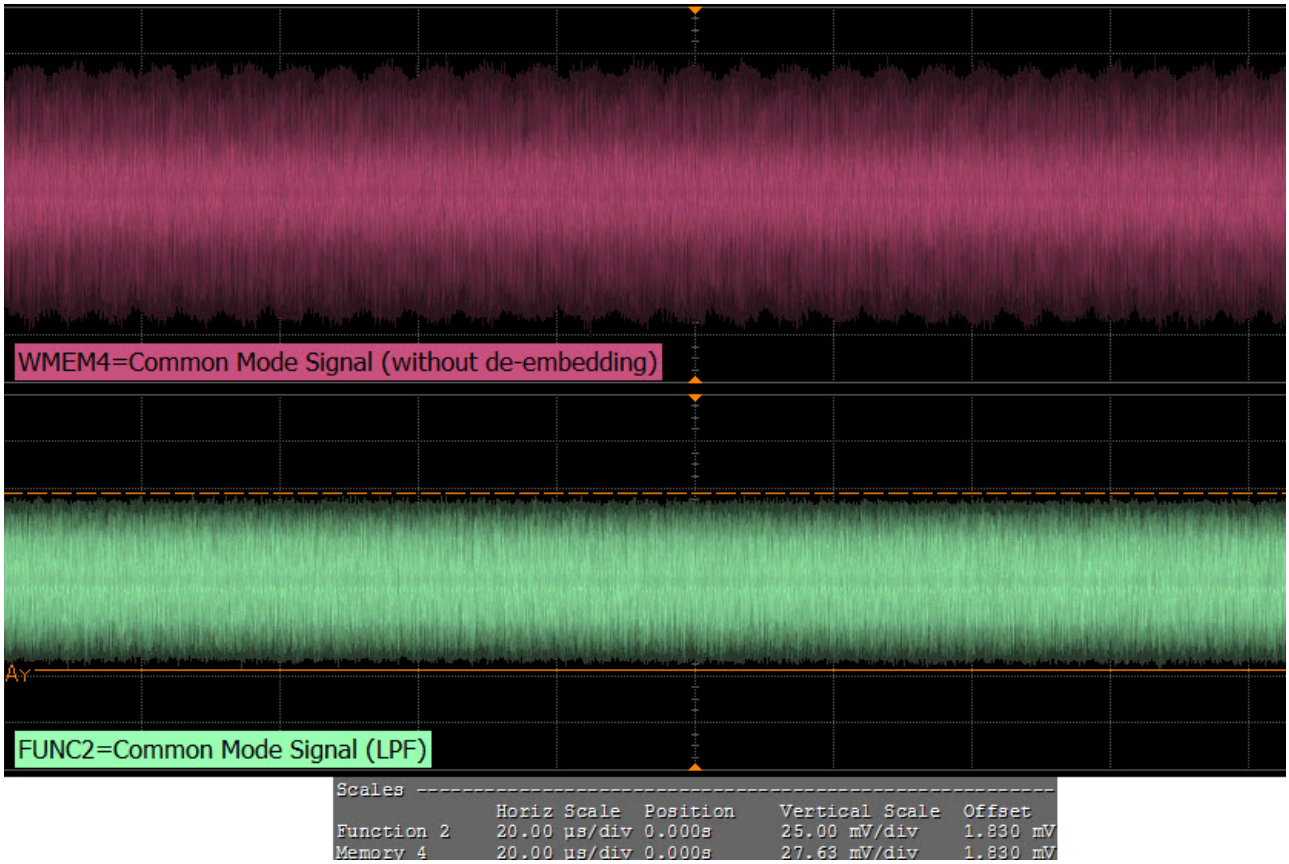


Figure 59 Reference Image for AC-CM voltage (4 GHz LPF) Test

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX\text{-}CM\text{-}DC\text{-}D+[during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D\text{-}[during\ L0]}| \leq 25\ mV$

$V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $|V_{TX\text{-}D+}|$ [during L0]

$V_{TX\text{-}CM\text{-}DC\text{-}D\text{-}} = DC_{(avg)}$ of $|V_{TX\text{-}D\text{-}}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Pass Limits

Table 332 Passing Limits Table for Absolute Delta of DC Common Mode Voltage Between D+ and D- Test (Parameter: $V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe1.0a	Base - Transmitter Tests	2.5 GT/s	Clean Clock	25.00	Base Spec 1.0a, Table 4-5
			SSC	25.00	Base Spec 1.0a, Table 4-5
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe1.1	Base - Transmitter Tests	2.5 GT/s	Clean Clock	25.00	Base Spec 1.1, Table 4-5
			SSC	25.00	Base Spec 1.1, Table 4-5
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe2.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	25.00	Base Spec 2.0, Table 4-9
			SSC	25.00	Base Spec 2.0, Table 4-9
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe2.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	25.00	Base Spec 2.0, Table 4-9
			SSC	25.00	Base Spec 2.0, Table 4-9
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 332 Passing Limits Table for Absolute Delta of DC Common Mode Voltage Between D+ and D- Test (Parameter: $V_{TX-CM-DC-LINE-DELTA}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe3.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	25.00	Base Spec 3.0, Table 4-18
			SSC	25.00	Base Spec 3.0, Table 4-18
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe3.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	25.00	Base Spec 3.0, Table 4-18
			SSC	25.00	Base Spec 3.0, Table 4-18
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	25.00	Base Spec 3.0, Table 4-18
			SSC	25.00	Base Spec 3.0, Table 4-18
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	25.00	Base Spec 4.0, Table 8-8
			SSC	25.00	Base Spec 4.0, Table 8-8
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	25.00	Base Spec 4.0, Table 8-8
			SSC	25.00	Base Spec 4.0, Table 8-8
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	25.00	Base Spec 4.0, Table 8-8
			SSC	25.00	Base Spec 4.0, Table 8-8
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 332 Passing Limits Table for Absolute Delta of DC Common Mode Voltage Between D+ and D- Test (Parameter: $V_{TX-CM-DC-LINE-DELTA}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	25.00	Base Spec 4.0, Table 8-8
			SSC	25.00	Base Spec 4.0, Table 8-8
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 333 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications

Table 334 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
Section 4.3.3	Differential Transmitter (TX) Output Specifications
Table 4-5	Differential Transmitter (TX) Output Specifications

Table 335 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.3.5	Transmitter Specifications
Table 4-9	2.5 and 5.0 GT/s Transmitter Specifications

Table 336 PCI Express Gen 3.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13	Common Transmitter Parameters
Table 4-18	Transmitter Specifications

Table 337 PCI Express Gen 4.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.9	Data Rate Independent Tx Parameters
Table 8-8	Data Rate Independent Tx Parameters

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
   - DC Common Mode Line Delta
   - Average DC value of D+
   - Average DC value of D-
2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.
3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

RMS Random Jitter

The **RMS Random Jitter** test is a timing measurement in PCI Express 2.0 that requires separation of the high frequency jitter on the transmitter signal.

The receiver margining leverages LF(low frequency) / HF(high frequency) jitter separation methodology employed for the transmitter.

There exists two different tests for this test with the same test procedure and exception of the template files as follows:

- Data clocked architecture RMS random jitter test
- Common reference clocked architecture RMS random jitter test

NOTE The RMS random jitter range for this test is not specified in the base specification (reference specs for all the transmitter and receiver tests). This test provides informative data only.

Pass Limits

Table 338 Passing Limits Table for RMS Random Jitter Test

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Li mits (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference

Table 338 Passing Limits Table for RMS Random Jitter Test

PCIe2.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	Base - Receiver Tests	5.0 GT/s	Clean Clock	100 mUI	For Data Clk: Informative Only For Common RefClk: Informative Only
			SSC	100 mUI	For Data Clk: Informative Only For Common RefClk: Informative Only
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	Cross Talk For -3.5 dB: N/A For -6.0 dB: N/A Without For -3.5 dB: N/A For -6.0 dB: N/A	Cross Talk For -3.5dB: Informative Only For -6.0dB: Informative Only Without For -3.5dB: Informative Only For -6.0dB: Informative Only
			SSC	Cross Talk For -3.5 dB: N/A For -6.0 dB: N/A Without For -3.5 dB: N/A For -6.0 dB: N/A	Cross Talk For -3.5dB: Informative Only For -6.0dB: Informative Only Without For -3.5dB: Informative Only For -6.0dB: Informative Only
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	Cross Talk: N/A Without: N/A	Cross Talk: Informative Only Without: Informative Only
			SSC	Cross Talk: N/A Without: N/A	Cross Talk: Informative Only Without: Informative Only
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference

Table 338 Passing Limits Table for RMS Random Jitter Test

PCIe3.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	Cross Talk For -3.5 dB: 1.400 ps For -6.0 dB: 1.400 ps Without For -3.5 dB: 1.400 ps For -6.0 dB: 1.400 ps	Cross Talk For -3.5 dB: CEM Spec 3.0, Table 4-8 For -6.0 dB: CEM Spec 3.0, Table 4-10 Without For -3.5 dB: CEM Spec 3.0, Table 4-8 For -6.0 dB: CEM Spec 3.0, Table 4-10
			SSC	Cross Talk For -3.5 dB: 1.400 ps For -6.0 dB: 1.400 ps Without For -3.5 dB: 1.400 ps For -6.0 dB: 1.400 ps	Cross Talk For -3.5 dB: CEM Spec 3.0, Table 4-8 For -6.0 dB: CEM Spec 3.0, Table 4-10 Without For -3.5 dB: CEM Spec 3.0, Table 4-8 For -6.0 dB: CEM Spec 3.0, Table 4-10
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	Cross Talk: 3.410 ps Without: 3.410 ps	Cross Talk: CEM Spec 3.0, Table 4-18 Without: CEM Spec 3.0, Table 4-18
			SSC	Cross Talk: 3.410 ps Without: 3.410 ps	Cross Talk: CEM Spec 3.0, Table 4-18 Without: CEM Spec 3.0, Table 4-18
	U.2 - EndPoint Tests	5.0 GT/s	Clean Clock	Cross Talk For -3.5 dB: 1.400 ps For -6.0 dB: 1.400 ps Without For -3.5 dB: 1.400 ps For -6.0 dB: 1.400 ps	Cross Talk For -3.5 dB: Informative only For -6.0 dB: Informative only Without For -3.5 dB: Informative only For -6.0 dB: Informative only
			SSC	Cross Talk For -3.5 dB: 1.400 ps For -6.0 dB: 1.400 ps Without For -3.5 dB: 1.400 ps For -6.0 dB: 1.400 ps	Cross Talk For -3.5 dB: Informative only For -6.0 dB: Informative only Without For -3.5 dB: Informative only For -6.0 dB: Informative only

Table 338 Passing Limits Table for RMS Random Jitter Test

	U.2 - RootComplex Tests	5.0 GT/s	Clean Clock	Cross Talk: 3.410 ps Without: 3.410 ps	Cross Talk: Informative only Without: Informative only
			SSC	Cross Talk: 3.410 ps Without: 3.410 ps	Cross Talk: Informative only Without: Informative only
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	Info Only	N/A (Informative only)
			SSC	Info Only	N/A (Informative only)
	CEM - EndPoint Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - RootComplex Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	Base - RefClk Tests	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference

Table 338 Passing Limits Table for RMS Random Jitter Test

PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	Info Only	N/A (Informative only)
			SSC	Info Only	N/A (Informative only)
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	Cross Talk For -3.5 dB: 1.400 ps For -6.0 dB: 1.400 ps Without For -3.5 dB: 1.400 ps For -6.0 dB: 1.400 ps	Cross Talk For -3.5 dB: CEM Spec 4.0, Table 13 For -6.0 dB: CEM Spec 4.0, Table 15 Without For -3.5 dB: CEM Spec 4.0, Table 13 For -6.0 dB: CEM Spec 4.0, Table 15
			SSC	Cross Talk For -3.5 dB: 1.400 ps For -6.0 dB: 1.400 ps Without For -3.5 dB: 1.400 ps For -6.0 dB: 1.400 ps	Cross Talk For -3.5 dB: CEM Spec 4.0, Table 13 For -6.0 dB: CEM Spec 4.0, Table 15 Without For -3.5 dB: CEM Spec 4.0, Table 13 For -6.0 dB: CEM Spec 4.0, Table 15
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	Cross Talk: 3.410 ps Without: 3.410 ps	Cross Talk: CEM Spec 4.0, Table 26 Without: CEM Spec 4.0, Table 26
			SSC	Cross Talk: 3.410 ps Without: 3.410 ps	Cross Talk: CEM Spec 4.0, Table 26 Without: CEM Spec 4.0, Table 26
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 339 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 340 PCI Express Gen 3.0, 5.0 GT/s References and Specification Notes

PCI Express™ CEM Specification Revision 3.0	
Section 4.8.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5.0 GT/s
Table 4-8	Add-in Card Jitter Requirements for 5.0 GT/s Signaling at 3.5 dB De-emphasis
Table 4-10	Add-in Card Jitter Requirements for 5.0 GT/s Signaling at 6.0 dB De-emphasis
PCI Express™ CEM Specification Revision 3.0	
Section 4.8.8	System Board Transmitter Path Compliance Eye Diagram at 5.0 GT/s
Table 4-18	System Board Jitter Requirements for 5.0 GT/s Signaling

Table 341 PCI Express Gen 4.0, 5.0 GT/s References and Specification Notes

PCI Express™ CEM Specification Revision 4.0	
Section 4.8.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5.0 GT/s
Table 13	Add-in Card Jitter Requirements for 5.0 GT/s Signaling at 3.5 dB De-emphasis
Table 15	Add-in Card Jitter Requirements for 5.0 GT/s Signaling at 6.0 dB De-emphasis
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.11	System Board Transmitter Path Compliance Eye Diagram at 5.0 GT/s
Table 26	System Board Jitter Requirements for 5.0 GT/s Signaling

Table 342 PCI Express Gen All, All GT/s References and Specification Notes

PCI Express™ Base Specification	
N/A	N/A (Not Applicable)
N/A	N/A (Not Applicable)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test.

Test Procedure

1 Gets RJ_rms test results from the SigTest tools.

2 Compares the measured RJ_rms value to the compliance test limits.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Maximum Deterministic Jitter Test

The **Maximum Deterministic Jitter** test is a timing measurement in PCI Express 2.0 that requires separation of the high frequency jitter on the transmitter signal.

The receiver margining leverages LF(low frequency) / HF(high frequency) jitter separation methodology employed for the transmitter.

There exists two different tests for this test with the same test procedure and exception of the template files as follows:

- Data clocked architecture maximum deterministic jitter test
- Common reference clocked architecture maximum deterministic jitter test

Pass Limits

Table 343 Passing Limits Table for Maximum Deterministic Jitter Test (Parameter: Dj_dd)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Li mits (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference

Table 343 Passing Limits Table for Maximum Deterministic Jitter Test (Parameter: Dj_dd)

PCIe2.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	Base - Receiver Tests	5.0 GT/s	Clean Clock	For DClk: 240 mUI For CRefClk: 300 mUI	For Data Clk: Base Spec 2.0, Table 4-12 For Common RefClk: Base Spec 2.0 Table 4-12
			SSC	For DClk: 240 mUI For CRefClk: 300 mUI	For Data Clk: Base Spec 2.0, Table 4-12 For Common RefClk: Base Spec 2.0 Table 4-12
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	Cross Talk For -3.5 dB: 57.000 ps For -6.0 dB: 57.000 ps Without For -3.5 dB: 54.000 ps For -6.0 dB: 54.000 ps	Cross Talk: For -3.5 dB: CEM Spec 2.0, Table 4-9 For -6.0 dB: CEM Spec 2.0, Table 4-11 Without For -3.5dB: CEM Spec 2.0, Table 4-9 For -6.0dB: CEM Spec 2.0, Table 4-11
			SSC	Cross Talk For -3.5 dB: 57.000 ps For -6.0 dB: 57.000 ps Without For -3.5 dB: 54.000 ps For -6.0 dB: 54.000 ps	Cross Talk: For -3.5 dB: CEM Spec 2.0, Table 4-9 For -6.0 dB: CEM Spec 2.0, Table 4-11 Without For -3.5dB: CEM Spec 2.0, Table 4-9 For -6.0dB: CEM Spec 2.0, Table 4-11
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	Cross Talk: 57.00 ps Without: 44.00 ps	Cross Talk: CEM Spec 2.0, Table 4-16 Without: CEM Spec 2.0, Table 4-16
			SSC	Cross Talk: 57.00 ps Without: 44.00 ps	Cross Talk: CEM Spec 2.0, Table 4-16 Without: CEM Spec 2.0, Table 4-16
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference

Table 343 Passing Limits Table for Maximum Deterministic Jitter Test (Parameter: Dj_dd)

PCIe3.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	Cross Talk For -3.5 dB: 57.000 ps For -6.0 dB: 57.000 ps Without For -3.5 dB: 54.000 ps For -6.0 dB: 54.000 ps	Cross Talk: For -3.5 dB: CEM Spec 3.0, Table 4-8 For -6.0 dB: CEM Spec 3.0, Table 4-10 Without For -3.5dB: CEM Spec 3.0, Table 4-8 For -6.0dB: CEM Spec 3.0, Table 4-10
			SSC	Cross Talk For -3.5 dB: 57.000 ps For -6.0 dB: 57.000 ps Without For -3.5 dB: 54.000 ps For -6.0 dB: 54.000 ps	Cross Talk: For -3.5 dB: CEM Spec 3.0, Table 4-8 For -6.0 dB: CEM Spec 3.0, Table 4-10 Without For -3.5dB: CEM Spec 3.0, Table 4-8 For -6.0dB: CEM Spec 3.0, Table 4-10
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	Cross Talk: 57.00 ps Without: 44.00 ps	Cross Talk: CEM Spec 3.0, Table 4-18 Without: CEM Spec 3.0, Table 4-18
			SSC	Cross Talk: 57.00 ps Without: 44.00 ps	Cross Talk: CEM Spec 3.0, Table 4-18 Without: CEM Spec 3.0, Table 4-18
	U.2 - EndPoint Tests	5.0 GT/s	Clean Clock	Cross Talk For -3.5 dB: 57.000 ps For -6.0 dB: 57.000 ps Without For -3.5 dB: 54.000 ps For -6.0 dB: 54.000 ps	Cross Talk: For -3.5 dB: U.2 Spec For -6.0 dB: U.2 Spec Without For -3.5 dB: U.2 Spec For -6.0 dB: U.2 Spec
			SSC	Cross Talk For -3.5 dB: 57.000 ps For -6.0 dB: 57.000 ps Without For -3.5 dB: 54.000 ps For -6.0 dB: 54.000 ps	Cross Talk: For -3.5 dB: U.2 Spec For -6.0 dB: U.2 Spec Without For -3.5 dB: U.2 Spec For -6.0 dB: U.2 Spec

Table 343 Passing Limits Table for Maximum Deterministic Jitter Test (Parameter: Dj_dd)

	U.2 - RootComplex Tests	5.0 GT/s	Clean Clock	Cross Talk: 57.00 ps Without: 44.00 ps	Cross Talk: U.2 Spec Without: U.2 Spec
			SSC	Cross Talk: 57.00 ps Without: 44.00 ps	Cross Talk: U.2 Spec Without: U.2 Spec
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference

Table 343 Passing Limits Table for Maximum Deterministic Jitter Test (Parameter: Dj_dd)

PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	Cross Talk For -3.5 dB: 57.000 ps For -6.0 dB: 57.000 ps Without For -3.5 dB: 54.000 ps For -6.0 dB: 54.000 ps	Cross Talk: For -3.5 dB: CEM Spec 4.0, Table 13 For -6.0 dB: CEM Spec 4.0, Table 15 Without For -3.5 dB: CEM Spec 4.0, Table 13 For -6.0 dB: CEM Spec 4.0, Table 15
			SSC	Cross Talk For -3.5 dB: 57.000 ps For -6.0 dB: 57.000 ps Without For -3.5 dB: 54.000 ps For -6.0 dB: 54.000 ps	Cross Talk: For -3.5 dB: CEM Spec 4.0, Table 13 For -6.0 dB: CEM Spec 4.0, Table 15 Without For -3.5 dB: CEM Spec 4.0, Table 13 For -6.0 dB: CEM Spec 4.0, Table 15
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	Cross Talk: 57.00 ps Without: 44.00 ps	Cross Talk: CEM Spec 4.0, Table 26 Without: CEM Spec 4.0, Table 26
			SSC	Cross Talk: 57.00 ps Without: 44.00 ps	Cross Talk: CEM Spec 4.0, Table 26 Without: CEM Spec 4.0, Table 26
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 344 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 345 PCI Express Gen 1.1, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification	
N/A	N/A (Not Applicable)

Table 346 PCI Express Gen 2.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification	
N/A	N/A (Not Applicable)

Table 347 PCI Express Gen 2.0, 5.0 GT/s References and Specification Notes

PCI Express™ Base Specification 2.0	
Section 4.3.4.4	Receiver Specifications
Table 4-12	2.5 and 5.0 GT/s Receiver Specifications
PCI Express™ CEM Specification 2.0	
Section 4.7.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5 GT/s
Table 4-9	Add-in Card Jitter Requirements For 5 GT/s Signaling at 3.5 dB De-emphasis
Table 4-11	Add-in Card Jitter Requirements For 5 GT/s Signaling at 6.0 dB De-emphasis
PCI Express™ CEM Specification 2.0	
Section 4.7.6	System Board Transmitter Path Compliance Eye Diagram at 5 GT/s
Table 4-16	System Board Jitter Requirements For 5 GT/s Signaling

Table 348 PCI Express Gen 3.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification	
N/A	N/A (Not Applicable)

Table 349 PCI Express Gen 3.0, 5.0 GT/s References and Specification Notes

PCI Express™ Base Specification	
Please refer to Table 347, “PCI Express Gen 2.0, 5.0 GT/s References and Specification Notes,”.	
PCI Express™ CEM Specification 3.0	
Section 4.8.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5 GT/s
Table 4-8	Add-in Card Jitter Requirements For 5 GT/s Signaling at 3.5 dB De-emphasis
Table 4-10	Add-in Card Jitter Requirements For 5 GT/s Signaling at 6.0 dB De-emphasis

Table 349 PCI Express Gen 3.0, 5.0 GT/s References and Specification Notes

PCI Express™ CEM Specification 3.0	
Section 4.8.8	System Board Transmitter Path Compliance Eye Diagram at 5.0 GT/s
Table 4-18	System Board Jitter Requirements For 5.0 GT/s Signaling

Table 350 PCI Express Gen 3.0, 8.0 GT/s References and Specification Notes

PCI Express™ Base Specification	
N/A	N/A (Not Applicable)

Table 351 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification	
N/A	N/A (Not Applicable)

Table 352 PCI Express Gen 4.0, 5.0 GT/s References and Specification Notes

PCI Express™ Base Specification	
Please refer to Table 347, "PCI Express Gen 2.0, 5.0 GT/s References and Specification Notes,".	
PCI Express™ CEM Specification 4.0	
Section 4.8.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5 GT/s
Table 13	Add-in Card Jitter Requirements For 5 GT/s Signaling at 3.5 dB De-emphasis
Table 15	Add-in Card Jitter Requirements For 5 GT/s Signaling at 6.0 dB De-emphasis
PCI Express™ CEM Specification 4.0	
Section 4.8.11	System Board Transmitter Path Compliance Eye Diagram at 5.0 GT/s
Table 26	System Board Jitter Requirements For 5.0 GT/s Signaling

Table 353 PCI Express Gen 4.0, 8.0 GT/s References and Specification Notes

PCI Express™ Base Specification	
N/A	N/A (Not Applicable)

Table 354 PCI Express Gen 4.0, 16.0 GT/s References and Specification Notes

PCI Express™ Base Specification	
N/A	N/A (Not Applicable)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test.

Test Procedure

1 Gets DJ_dd test results from the SigTest tools.

2 Compares the measured DJ_dd value to the compliance test limits.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Jitter at BER-12 Test

The **Total Jitter at BER-12** test is a timing measurement in PCI Express 2.0 that requires separation of the high frequency jitter on the transmitter signal.

The receiver margining leverages LF(low frequency) / HF(high frequency) jitter separation methodology employed for the transmitter.

There exists two different tests for this test with the same test procedure and exception of the template files as follows:

- Data clocked architecture total jitter at BER-12 test
- Common reference clocked architecture total jitter at BER-12 test

Pass Limits

Table 355 Passing Limits Table for Total Jitter at BER-12 Test (Parameter: $T_{RX-TJ-CC}$ or $T_{RX-TJ-DC}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Li mits (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference

Table 355 Passing Limits Table for Total Jitter at BER-12 Test (Parameter: $T_{RX-TJ-CC}$ or $T_{RX-TJ-DC}$)

PCIe2.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	Base - Receiver Tests	5.0 GT/s	Clean Clock	For DClk: 340 mUI For CRefClk: 400 mUI	For Data Clk: Base Spec 2.0, Table 4-12 For Common RefClk: Base Spec 2.0 Table 4-12
			SSC	For DClk: 340 mUI For CRefClk: 400 mUI	For Data Clk: Base Spec 2.0, Table 4-12 For Common RefClk: Base Spec 2.0 Table 4-12
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	Cross Talk For -3.5 dB: 77.000 ps For -6.0 dB: 77.000 ps Without For -3.5 dB: 74.000 ps For -6.0 dB: 74.000 ps	Cross Talk: For -3.5 dB: CEM Spec 2.0, Table 4-9 For -6.0 dB: CEM Spec 2.0, Table 4-11 Without: For -3.5dB: CEM Spec 2.0, Table 4-9 For -6.0dB: CEM Spec 2.0, Table 4-11
			SSC	Cross Talk For -3.5 dB: 77.000 ps For -6.0 dB: 77.000 ps Without For -3.5 dB: 74.000 ps For -6.0 dB: 74.000 ps	Cross Talk: For -3.5 dB: CEM Spec 2.0, Table 4-9 For -6.0 dB: CEM Spec 2.0, Table 4-11 Without For -3.5dB: CEM Spec 2.0, Table 4-9 For -6.0dB: CEM Spec 2.0, Table 4-11
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	Cross Talk: 105.00 ps Without: 92.00 ps	Cross Talk: CEM Spec 2.0, Table 4-16 Without: CEM Spec 2.0, Table 4-16
			SSC	Cross Talk: 105.00 ps Without: 92.00 ps	Cross Talk: CEM Spec 2.0, Table 4-16 Without: CEM Spec 2.0, Table 4-16
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference

Table 355 Passing Limits Table for Total Jitter at BER-12 Test (Parameter: $T_{RX-TJ-CC}$ or $T_{RX-TJ-DC}$)

PCIe3.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	Cross Talk For -3.5 dB: 77.000 ps For -6.0 dB: 77.000 ps Without For -3.5 dB: 74.000 ps For -6.0 dB: 74.000 ps	Cross Talk: For -3.5 dB: CEM Spec 3.0, Table 4-8 For -6.0 dB: CEM Spec 3.0, Table 4-10 Without: For -3.5 dB: CEM Spec 3.0, Table 4-8 For -6.0 dB: CEM Spec 3.0, Table 4-10
			SSC	Cross Talk For -3.5 dB: 77.000 ps For -6.0 dB: 77.000 ps Without For -3.5 dB: 74.000 ps For -6.0 dB: 74.000 ps	Cross Talk: For -3.5 dB: CEM Spec 3.0, Table 4-8 For -6.0 dB: CEM Spec 3.0, Table 4-10 Without: For -3.5 dB: CEM Spec 3.0, Table 4-8 For -6.0 dB: CEM Spec 3.0, Table 4-10
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	Cross Talk: 105.00 ps Without: 92.00 ps	Cross Talk: CEM Spec 3.0, Table 4-18 Without: CEM Spec 3.0, Table 4-18
			SSC	Cross Talk: 105.00 ps Without: 92.00 ps	Cross Talk: CEM Spec 3.0, Table 4-18 Without: CEM Spec 3.0, Table 4-18
	U.2 - EndPoint Tests	5.0 GT/s	Clean Clock	Cross Talk For -3.5 dB: 77.000 ps For -6.0 dB: 77.000 ps Without For -3.5 dB: 74.000 ps For -6.0 dB: 74.000 ps	Cross Talk: For -3.5 dB: U.2 Spec For -6.0 dB: U.2 Spec Without For -3.5 dB: U.2 Spec For -6.0 dB: U.2 Spec
			SSC	Cross Talk For -3.5 dB: 77.000 ps For -6.0 dB: 77.000 ps Without For -3.5 dB: 74.000 ps For -6.0 dB: 74.000 ps	Cross Talk: For -3.5 dB: U.2 Spec For -6.0 dB: U.2 Spec Without For -3.5 dB: U.2 Spec For -6.0 dB: U.2 Spec

Table 355 Passing Limits Table for Total Jitter at BER-12 Test (Parameter: $T_{RX-TJ-CC}$ or $T_{RX-TJ-DC}$)

	U.2 - RootComplex Tests	5.0 GT/s	Clean Clock	Cross Talk: 105.00 ps Without: 92.00 ps	Cross Talk: U.2 Spec Without: U.2 Spec
			SSC	Cross Talk: 105.00 ps Without: 92.00 ps	Cross Talk: U.2 Spec Without: U.2 Spec
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference

Table 355 Passing Limits Table for Total Jitter at BER-12 Test (Parameter: $T_{RX-TJ-CC}$ or $T_{RX-TJ-DC}$)

PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
	CEM - EndPoint Tests	5.0 GT/s	Clean Clock	Cross Talk For -3.5 dB: 77.000 ps For -6.0 dB: 77.000 ps Without For -3.5 dB: 74.000 ps For -6.0 dB: 74.000 ps	Cross Talk: For -3.5 dB: CEM Spec 4.0, Table 13 For -6.0 dB: CEM Spec 4.0, Table 15 Without For -3.5 dB: CEM Spec 4.0, Table 13 For -6.0 dB: CEM Spec 4.0, Table 15
			SSC	Cross Talk For -3.5 dB: 77.000 ps For -6.0 dB: 77.000 ps Without For -3.5 dB: 74.000 ps For -6.0 dB: 74.000 ps	Cross Talk: For -3.5 dB: CEM Spec 4.0, Table 13 For -6.0 dB: CEM Spec 4.0, Table 15 Without For -3.5 dB: CEM Spec 4.0, Table 13 For -6.0 dB: CEM Spec 4.0, Table 15
	CEM - RootComplex Tests	5.0 GT/s	Clean Clock	Cross Talk: 105.00 ps Without: 92.00 ps	Cross Talk: CEM Spec 4.0, Table 26 Without: CEM Spec 4.0, Table 26
			SSC	Cross Talk: 105.00 ps Without: 92.00 ps	Cross Talk: CEM Spec 4.0, Table 26 Without: CEM Spec 4.0, Table 26
	Base - RefClk Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 356 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 357 PCI Express Gen 1.1, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification	
N/A	N/A (Not Applicable)

Table 358 PCI Express Gen 2.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification	
N/A	N/A (Not Applicable)

Table 359 PCI Express Gen 2.0, 5.0 GT/s References and Specification Notes

PCI Express™ Base Specification 2.0	
Section 4.3.4.4	Receiver Specifications
Table 4-12	2.5 and 5.0 GT/s Receiver Specifications
PCI Express™ CEM Specification 2.0	
Section 4.7.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5 GT/s
Table 4-9	Add-in Card Jitter Requirements For 5 GT/s Signaling at 3.5 dB De-emphasis
Table 4-11	Add-in Card Jitter Requirements For 5 GT/s Signaling at 6.0 dB De-emphasis
PCI Express™ CEM Specification 2.0	
Section 4.7.6	System Board Transmitter Path Compliance Eye Diagram at 5 GT/s
Table 4-16	System Board Jitter Requirements For 5 GT/s Signaling

Table 360 PCI Express Gen 3.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification	
N/A	N/A (Not Applicable)

Table 361 PCI Express Gen 3.0, 5.0 GT/s References and Specification Notes

PCI Express™ Base Specification	
Please refer to Table 359, “PCI Express Gen 2.0, 5.0 GT/s References and Specification Notes,”.	
PCI Express™ CEM Specification 3.0	
Section 4.8.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5.0 GT/s
Table 4-8	Add-in Card Jitter Requirements For 5.0 GT/s Signaling at 3.5 dB De-emphasis
Table 4-10	Add-in Card Jitter Requirements For 5.0 GT/s Signaling at 6.0 dB De-emphasis

Table 361 PCI Express Gen 3.0, 5.0 GT/s References and Specification Notes

PCI Express™ CEM Specification 3.0	
Section 4.8.8	System Board Transmitter Path Compliance Eye Diagram at 5.0 GT/s
Table 4-18	System Board Jitter Requirements For 5.0 GT/s Signaling

Table 362 PCI Express Gen 3.0, 8.0 GT/s References and Specification Notes

PCI Express™ Base Specification	
N/A	N/A (Not Applicable)

Table 363 PCI Express Gen 4.0, 2.5 GT/s References and Specification Notes

PCI Express™ Base Specification	
N/A	N/A (Not Applicable)

Table 364 PCI Express Gen 4.0, 5.0 GT/s References and Specification Notes

PCI Express™ Base Specification	
Please refer to Table 359, “PCI Express Gen 2.0, 5.0 GT/s References and Specification Notes,”.	
PCI Express™ CEM Specification 4.0	
Section 4.8.2	Add-in Card Transmitter Path Compliance Eye Diagrams at 5.0 GT/s
Table 13	Add-in Card Jitter Requirements For 5.0 GT/s Signaling at 3.5 dB De-emphasis
Table 15	Add-in Card Jitter Requirements For 5.0 GT/s Signaling at 6.0 dB De-emphasis
PCI Express™ CEM Specification 4.0	
Section 4.8.11	System Board Transmitter Path Compliance Eye Diagram at 5.0 GT/s
Table 26	System Board Jitter Requirements For 5.0 GT/s Signaling

Table 365 PCI Express Gen 4.0, 8.0 GT/s References and Specification Notes

PCI Express™ Base Specification	
N/A	N/A (Not Applicable)

Table 366 PCI Express Gen 4.0, 16.0 GT/s References and Specification Notes

PCI Express™ Base Specification	
N/A	N/A (Not Applicable)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test.

Test Procedure

1 Gets total jitter at BER-12 test results from the SigTest tools and divides it by unit interval.
2 Compares the measured total jitter at BER-12 value to the compliance test limits.
3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Pass Limits

Table 367 Passing Limits Table for Uncorrelated Total Jitter Test (Parameter: T_{TX-UTJ})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	31.250	Base Spec 3.0, Table 4-19
			SSC	31.250	Base Spec 3.0, Table 4-19
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference

Table 367 Passing Limits Table for Uncorrelated Total Jitter Test (Parameter: T_{TX-UTJ})

PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	100.00	Base Spec 4.0, Table 8-7
			SSC	100.00	Base Spec 4.0, Table 8-7
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	50.00	Base Spec 4.0, Table 8-7
			SSC	50.00	Base Spec 4.0, Table 8-7
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	31.25	Base Spec 4.0, Table 8-7
			SSC	31.25	Base Spec 4.0, Table 8-7
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	12.50	Base Spec 4.0, Table 8-7
			SSC	12.50	Base Spec 4.0, Table 8-7
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 368 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 369 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 370 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 371 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 372 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 373 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13.1	8.0 GT/s Specific Tx Voltage and Jitter Parameter Table
Table 4-19	8.0 GT/s Specific Tx Voltage and Jitter Parameters

Table 374 PCI Express Gen 4.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 "Compliance Patterns in Various Encodings".**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs actual compliance testing using the SigTest tools.

   a Gets input test waveform data from scope.

   b Acquires scope sample waveform data (re-iterate to capture at least 1M UI).

   c Performs the transmitter compliance test function using the SigTest tools.

   d Gets compliance test results from SigTest tools.

   e Reports the RJ RMS jitter value.

   f Reports the peak total jitter value.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Pass Limits

Table 375 Passing Limits Table for Uncorrelated Deterministic Jitter Test (Parameter: $T_{TX-UDJDD}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	12.000	Base Spec 3.0, Table 4-19
			SSC	12.000	Base Spec 3.0, Table 4-19
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference

Table 375 Passing Limits Table for Uncorrelated Deterministic Jitter Test (Parameter: $T_{TX-UDJDD}$)

PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	100.00	Base Spec 4.0, Table 8-7
			SSC	100.00	Base Spec 4.0, Table 8-7
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	30.00	Base Spec 4.0, Table 8-7
			SSC	30.00	Base Spec 4.0, Table 8-7
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	12.00	Base Spec 4.0, Table 8-7
			SSC	12.00	Base Spec 4.0, Table 8-7
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	6.250	Base Spec 4.0, Table 8-7
			SSC	6.250	Base Spec 4.0, Table 8-7
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 376 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 377 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 378 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 379 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 380 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 381 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13.1	8.0 GT/s Specific Tx Voltage and Jitter Parameter Table
Table 4-19	8.0 GT/s Specific Tx Voltage and Jitter Parameters

Table 382 PCI Express Gen 4.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 "Compliance Patterns in Various Encodings".**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs actual compliance testing using the SigTest tools.

   a Gets input test waveform data from scope.

   b Acquires scope sample waveform data (re-iterate to capture at least 1M UI).

   c Performs the transmitter compliance test function using the SigTest tools.

   d Gets compliance test results from SigTest tools.

   e Reports the peak uncorrelated deterministic jitter value.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the maximum total uncorrelated PWJ $T_{TX-UPW-TJ}$ is within the allowed range.

Pass Limits

Table 383 Passing Limits Table for Total Uncorrelated PWJ (Pulse Width Jitter) Test (Parameter: $T_{TX-UPW-TJ}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	24.000	Base Spec 3.0, Table 4-19
			SSC	24.000	Base Spec 3.0, Table 4-19
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference

Table 383 Passing Limits Table for Total Uncorrelated PWJ (Pulse Width Jitter) Test (Parameter: $T_{TX-UPW-TJ}$)

PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	Info Only	N/A (Information Only)
			SSC	Info Only	N/A (Information Only)
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	40.00	Base Spec 4.0, Table 8-7
			SSC	40.00	Base Spec 4.0, Table 8-7
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	24.00	Base Spec 4.0, Table 8-7
			SSC	24.00	Base Spec 4.0, Table 8-7
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	12.500	Base Spec 4.0, Table 8-7
			SSC	12.500	Base Spec 4.0, Table 8-7
	CEM - EndPoint Tests	16.0 GT/s	Clean Clock	12.500	CEM Spec 4.0, Table 18
			SSC	12.500	CEM Spec 4.0, Table 18
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 384 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 385 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 386 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 387 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 388 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 389 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13.1	8.0 GT/s Specific Tx Voltage and Jitter Parameter Table
Table 4-19	8.0 GT/s Specific Tx Voltage and Jitter Parameters

Table 390 PCI Express Gen 4.0, 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters

Table 391 PCI Express Gen 4.0, 16 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.5	Add-in Card Transmitter Path Pulse Width Jitter at 16.0 GT/s
Table 18	Add-in Card Transmitter Path Uncorrelated Pulse Width Jitter Requirements at 16.0 GT/s

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 "Compliance Patterns in Various Encodings".**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs actual compliance testing using the SigTest tools.

   a Gets input test waveform data from scope.

   b Acquires scope sample waveform data (re-iterate to capture at least 1M UI).

   c Performs the transmitter compliance test function using the SigTest tools.

   d Gets compliance test results from SigTest tools.

   e Reports the random jitter value.

   f Reports the uncorrelated total pulse width jitter value.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX-UPW-DJDD}$ is within the allowed range.

Pass Limits

Table 392 Passing Limits Table for Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test (Parameter: $T_{TX-UPW-DJDD}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	10.000	Base Spec 3.0, Table 4-19
			SSC	10.000	Base Spec 3.0, Table 4-19
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference

Table 392 Passing Limits Table for Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test (Parameter: $T_{TX-UPW-DJDD}$)

PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	Info Only	N/A (Information Only)
			SSC	Info Only	N/A (Information Only)
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	40.00	Base Spec 4.0, Table 8-7
			SSC	40.00	Base Spec 4.0, Table 8-7
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	10.00	Base Spec 4.0, Table 8-7
			SSC	10.00	Base Spec 4.0, Table 8-7
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	5.000	Base Spec 4.0, Table 8-7
			SSC	5.000	Base Spec 4.0, Table 8-7
	CEM - EndPoint	16.0 GT/s	Clean Clock	5.000	CEM Spec 4.0, Table 18
			SSC	5.000	CEM Spec 4.0, Table 18
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 393 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 394 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 395 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 396 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 397 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 398 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13.1	8.0 GT/s Specific Tx Voltage and Jitter Parameter Table
Table 4-19	8.0 GT/s Specific Tx Voltage and Jitter Parameters

Table 399 PCI Express Gen 4.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters
PCI Express™ CEM Specification Revision 4.0	
Section 4.8.5	Add-in Card Transmitter Path Pulse Width Jitter at 16.0 GT/s
Table 18	Add-in Card Transmitter Path Uncorrelated Pulse Width Jitter Requirements at 16.0 GT/s

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 "Compliance Patterns in Various Encodings".**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs actual compliance testing using the SigTest tools.

   a Gets input test waveform data from scope.

   b Acquires scope sample waveform data (re-iterate to capture at least 1M UI).

   c Performs the transmitter compliance test function using the SigTest tools.

   d Gets compliance test results from SigTest tools.

   e Reports the peak deterministic DjDD uncorrelated PWJ value.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Data Dependent Jitter Test

This test verifies that the maximum data dependent jitter, T_{TX-DDJ} is within the allowed range.

Pass Limits

Table 400 Passing Limits Table for Data Dependent Jitter Test (Parameter: T_{TX-DDJ})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	18.000	Base Spec 3.0, Table 4-19
			SSC	18.000	Base Spec 3.0, Table 4-19
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference

Table 400 Passing Limits Table for Data Dependent Jitter Test (Parameter: T_{TX-DDJ})

PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	Info Only	N/A (Information Only)
			SSC	Info Only	N/A (Information Only)
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	Info Only	N/A (Information Only)
			SSC	Info Only	N/A (Information Only)
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	Info Only	N/A (Information Only)
			SSC	Info Only	N/A (Information Only)
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	Info Only	N/A (Information Only)
			SSC	Info Only	N/A (Information Only)
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 401 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 402 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 403 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 404 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 405 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 406 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13.1	8.0 GT/s Specific Tx Voltage and Jitter Parameter Table
Table 4-19	8.0 GT/s Specific Tx Voltage and Jitter Parameters

Table 407 PCI Express Gen 4.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters

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Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 "Compliance Patterns in Various Encodings".**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs actual compliance testing using the SigTest tools.

   a Gets input test waveform data from scope.

   b Acquires scope sample waveform data (re-iterate to capture at least 1M UI).

   c Performs the transmitter compliance test function using the SigTest tools.

   d Gets compliance test results from SigTest tools.

   e Reports the data dependent value.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Random Jitter Test

This test verifies that the random jitter, T_{TX-RJ} is within the allowed range.

Random jitter is uncorrelated with respect to data dependent jitter. T_{TX-RJ} may be obtained by subtracting $T_{TX-UDJ-DD}$ from T_{TX-UTJ}. and is included in the specification as an informative parameter only. It is typically used as a benchmark to characterize PLL performance.

Pass Limits

Table 408 Passing Limits Table for Random Jitter Test (Parameter: T_{TX-RJ})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference

Table 408 Passing Limits Table for Random Jitter Test (Parameter: T_{TX-RJ})

PCIe4.0	Base - Transmitter Tests	2.5 GT/s	Clean Clock	Info Only	N/A (Information Only)
			SSC	Info Only	N/A (Information Only)
	All Other	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	5.0 GT/s	Clean Clock	Info Only	N/A (Information Only)
			SSC	Info Only	N/A (Information Only)
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	Info Only	N/A (Information Only)
			SSC	Info Only	N/A (Information Only)
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	Info Only	N/A (Information Only)
			SSC	Info Only	N/A (Information Only)
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 409 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 410 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 411 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 412 PCI Express Gen 3.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 413 PCI Express Gen 4.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
   a Gets input test waveform data from scope.
   b Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
   c Performs the transmitter compliance test function using the SigTest tools.
   d Gets compliance test results from SigTest tools.
   e Reports the data dependent value.
3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Pseudo Package Loss, Non-Root Device Test

This test verifies that the maximum pseudo package loss, $ps21_{TX\text{-}NON\text{-}ROOT\text{-}DEVICE}$ is within the allowed range.

Separate $ps21_{TX}$ parameters are defined for packages containing Root Ports (Root Package) and for all other packages (Non-Root Package), based on the assumption that the former tend to be large and require socketing, while the latter are smaller and usually not socketed.

Package loss is measured by comparing the 64-zeroes/64-ones PP voltage (V_{111}) against a 1010 pattern (V_{101}). Tx package loss measurement is made with c_{-1} and c_{+1} both set to zero. A total of 10^6 measurements shall be made and averaged to obtain values for V_{101} and V_{111}. Multiple measurements shall be made and averaged to obtain stable values for V_{101} and V_{111}. Due to the HF content of V_{101}, $ps21_{TX}$ measurement requires that the breakout channel be de-embedded back to the Tx pin.

Measurement of V_{101} and V_{111} is made towards the end of each interval to minimize ISI and low frequency effects. V_{101} is defined as the peak-peak voltage between minima and maxima of the clock pattern. V_{111} is defined as the peak-peak voltage difference between the positive and negative levels of the two half cycles. The measurement should be averaged over multiple compliance patterns until the mean deviates by less than 2% between successive averages.

Pass Limits

Table 414 Passing Limits Table for Pseudo Package Loss, Non-Root Device Test (Parameter: $ps21_{TX}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference

Table 414 Passing Limits Table for Pseudo Package Loss, Non-Root Device Test (Parameter: $ps21_{TX}$)

PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	-3.000	Base Spec 3.0, Table 4-19
			SSC	-3.000	Base Spec 3.0, Table 4-19
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	-3.000	Base Spec 4.0, Table 8-7
			SSC	-3.000	Base Spec 4.0, Table 8-7
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	Cap. Ch: -3.000*	Captive Channel: Base Spec 4.0, Table 8-7, Table 8-4 *As per Base Spec 4.0, Figure 8-10: the value will be negative.
				N-Cap Ch: Info Only	Non Captive Channel: Base Spec 4.0, Table 8-7, Table 8-4
			SSC	Cap. Ch: -3.000*	Captive Channel: Base Spec 4.0, Table 8-7, Table 8-4 *As per Base Spec 4.0, Figure 8-10: the value will be negative.
				N-Cap Ch: Info Only	Non Captive Channel: Base Spec 4.0, Table 8-7, Table 8-4
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 415 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 416 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 417 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 418 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 419 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

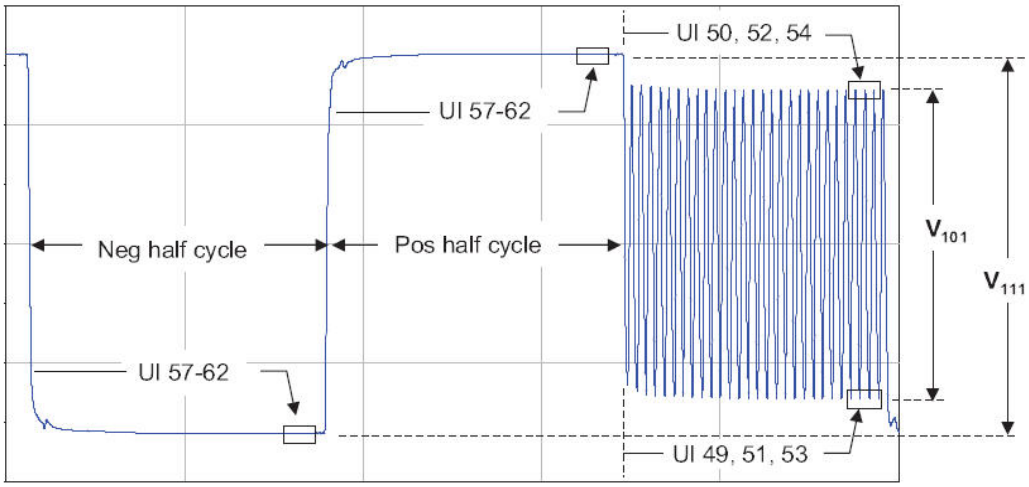
PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 420 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13.1	8.0 GT/s Specific Tx Voltage and Jitter Parameter Table
Table 4-19	8.0 GT/s Specific Tx Voltage and Jitter Parameters

Table 421 PCI Express Gen 4.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters



$$ps21_{TX} = 20\log_{10}(V_{101}/V_{111})$$

Figure 60 Compliance Pattern and Resulting Package Loss Test Waveform

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 "Compliance Patterns in Various Encodings".**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs actual compliance testing using the SigTest tools.

   a Gets input test waveform data from scope.

   b Acquires scope sample waveform data (re-iterate to capture at least 1M UI).

   c Performs the transmitter compliance test function using the SigTest tools.

   d Gets compliance test results from SigTest tools.

   e Reports the number of package loss measurements taken.

   f Reports the package loss ration value.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Pseudo Package Loss, Root Device Test

This test verifies that the maximum pseudo package loss, $ps21_{TX\text{-}ROOT\text{-}DEVICE}$ is within the allowed range.

Separate $ps21_{TX}$ parameters are defined for packages containing Root Ports (Root Package) and for all other packages (Non-Root Package), based on the assumption that the former tend to be large and require socketing, while the latter are smaller and usually not socketed.

Package loss is measured by comparing the 64-zeroes/64-ones PP voltage (V_{111}) against a 1010 pattern (V_{101}). Tx package loss measurement is made with c_{-1} and c_{+1} both set to zero. A total of 10^6 measurements shall be made and averaged to obtain values for V_{101} and V_{111}. Multiple measurements shall be made and averaged to obtain stable values for V_{101} and V_{111}. Due to the HF content of V_{101}, $ps21_{TX}$ measurement requires that the breakout channel be de-embedded back to the Tx pin.

Measurement of V_{101} and V_{111} is made towards the end of each interval to minimize ISI and low frequency effects. V_{101} is defined as the peak-peak voltage between minima and maxima of the clock pattern. V_{111} is defined as the peak-peak voltage difference between the positive and negative levels of the two half cycles. The measurement should be averaged over multiple compliance patterns until the mean deviates by less than 2% between successive averages.

Pass Limits

Table 422 Passing Limits Table for Pseudo Package Loss, Root Device Test (Parameter: $ps21_{TX}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference

Table 422 Passing Limits Table for Pseudo Package Loss, Root Device Test (Parameter: $ps21_{TX}$)

PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	-3.000	Base Spec 3.0, Table 4-19
			SSC	-3.000	Base Spec 3.0, Table 4-19
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	-3.000	Base Spec 4.0, Table 8-7
			SSC	-3.000	Base Spec 4.0, Table 8-7
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (dB) (Max)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	Info Only	Base Spec 4.0, Table 8-7, Table 8-4
			SSC	Info Only	Base Spec 4.0, Table 8-7, Table 8-4
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 423 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 424 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 425 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 426 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 427 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

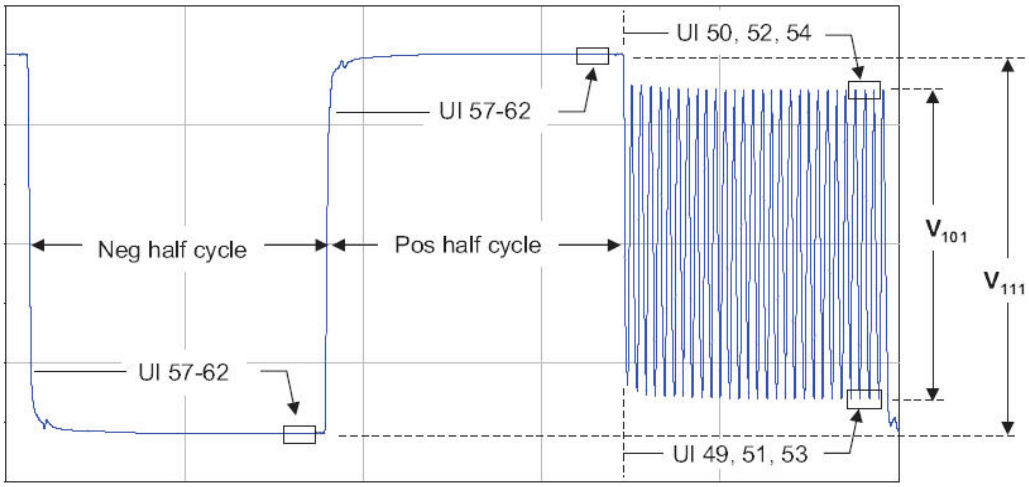
PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 428 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13.1	8.0 GT/s Specific Tx Voltage and Jitter Parameter Table
Table 4-19	8.0 GT/s Specific Tx Voltage and Jitter Parameters

Table 429 PCI Express Gen 4.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters



$$ps21_{TX} = 20\log_{10}(V_{101}/V_{111})$$

Figure 61 Compliance Pattern and Resulting Package Loss Test Waveform

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 "Compliance Patterns in Various Encodings".

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
   a Gets input test waveform data from scope.
   b Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
   c Performs the transmitter compliance test function using the SigTest tools.
   d Gets compliance test results from SigTest tools.
   e Reports the number of package loss measurements taken.
   f Reports the package loss ration value.
3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Max)

This test verifies that the SSC maximum deviation within the allowed range.

Pass Limits

Table 430 Passing Limits Table for SSC Peak Deviation (Max) Test (Parameter: $T_{SSC-FREQ-DEVIATION}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference

Table 430 Passing Limits Table for SSC Peak Deviation (Max) Test (Parameter: $T_{SSC-FREQ-DEVIATION}$)

PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	0.00%	Base Spec 4.0, Table 8-18
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	0.00%	Base Spec 4.0, Table 8-18
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 431 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 432 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 433 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 434 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 435 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 436 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 437 PCI Express Gen 4.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 438 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 439 PCI Express Gen 4.0, Data Rate 8.0 and 16 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.3	Data Rate Independent Refclk Parameters
Table 8-18	Data Rate Independent Refclk Parameters

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the data rate is 5.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures Period_max, Period_min and Period_average.
9 Computes SSC deviation Max(%) = ((1 / Data Rate) - SSC's Minimum UI) / (1 / Data Rate) * 100
10 Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Min)

This test verifies that the SSC minimum deviation within the allowed range.

Pass Limits

Table 440 Passing Limits Table for SSC Peak Deviation (Min) Test (Parameter: $T_{SSC-FREQ-DEVIATION}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference

Table 440 Passing Limits Table for SSC Peak Deviation (Min) Test (Parameter: $T_{SSC-FREQ-DEVIATION}$)

PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	-0.5%	Base Spec 4.0, Table 8-18
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	-0.5%	Base Spec 4.0, Table 8-18
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 441 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 442 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 443 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 444 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 445 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 446 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 447 PCI Express Gen 4.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 448 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 449 PCI Express Gen 4.0, 8.0 and 16.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.3	Data Rate Independent Refclk Parameters
Table 8-18	Data Rate Independent Refclk Parameters

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the data rate is 5.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures Period_max, Period_min and Period_average.
9 Computes SSC deviation Min(%) = ((1 / Data Rate) - SSC's Maximum UI) / (1 / Data Rate) * 100
10 Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Max df/dt (Slew Rate) Test

This test verifies that the SSC maximum slew rate is within the allowed range.

Pass Limits

Table 450 Passing Limits Table for SSC Max df/dt (Slew Rate) Test (Parameter: $T_{SSC-MAX-FREQ-SLEW}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference

Table 450 Passing Limits Table for SSC Max df/dt (Slew Rate) Test (Parameter: $T_{SSC-MAX-FREQ-SLEW}$)

PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	1.25 kppm/us	Base Spec 4.0, Table 8-18
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Max)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	1.25 kppm/us	Base Spec 4.0, Table 8-18
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 451 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 452 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 453 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 454 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 455 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 456 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 457 PCI Express Gen 4.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 458 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 459 PCI Express Gen 4.0, 8.0 and 16.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.3	Data Rate Independent Refclk Parameters
Table 8-18	Data Rate Independent Refclk Parameters

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures memory depth and sampling rate as per the data rate.
3. Fits and displays all sample data on screen.
4. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function.
6. The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:
   a Generates a differential plot ($x_n - x_{n-1}$).
   b The maximum slew rate corresponds to the peak of the differential plot.
7. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

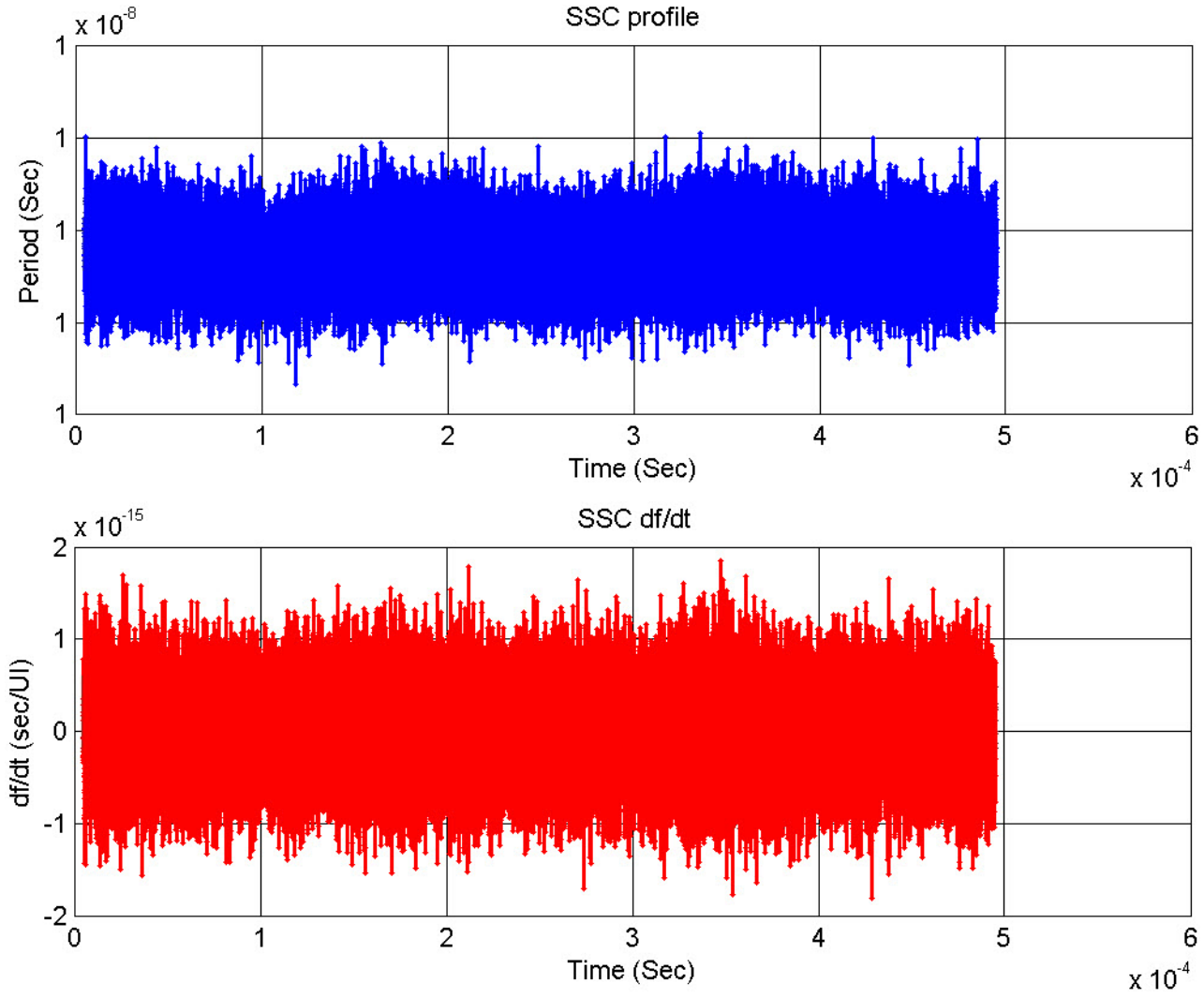


Figure 62 Maximum SSC Slew Rate

SSC Modulation Frequency

This test verifies that the SSC frequency range is in the allowable range.

Pass Limits

Table 460 Passing Limits Table for SSC Modulation Frequency Test (Parameter: F_{SSC})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference

Table 460 Passing Limits Table for SSC Modulation Frequency Test (Parameter: F_{SSC})

PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	30/33 kHz	Base Spec 4.0, Table 8-18
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (Min/Max)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	30/33 kHz	Base Spec 4.0, Table 8-18
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 461 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 462 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 463 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 464 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 465 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 466 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 467 PCI Express Gen 4.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 468 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 469 PCI Express Gen 4.0, 8.0 and 16.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.3	Data Rate Independent Refclk Parameters
Table 8-18	Data Rate Independent Refclk Parameters

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the data rate is 5.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Full Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during full swing signaling is within the conformance limits specified in Table 4-19 of the PCIE Base Specification, rev. 3.0.

The range for a transmitter's output voltage swing, (specified by V_d) with no equalization is defined by $V_{TH-FS-NO-EQ}$, and is obtained by setting c-1 and c+1 to zero and measuring the PP voltage on the 64-ones/64-zeros segment of the compliance pattern. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to last few UI of each half cycle (UI 57-62 of 64-ones/64-zeros). High frequency noise is mitigated by averaging over multiple reading until the PP noise over the area of interest is less than 2% of the magnitude of $V_{TH-FS-NO-EQ}$.

Pass Limits

Table 470 Passing Limits Table for Full Swing Tx Voltage with no TxEQ Test (Parameter: $V_{TX-FS-NO-EQ}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference

Table 470 Passing Limits Table for Full Swing Tx Voltage with no TxEQ Test (Parameter: $V_{TX-FS-NO-EQ}$)

PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	0.800/1.300	Base Spec 3.0, Table 4-19
			SSC	0.800/1.300	Base Spec 3.0, Table 4-19
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	0.800/1.300	Base Spec 4.0, Table 8-7
			SSC	0.800/1.300	Base Spec 4.0, Table 8-7
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	0.800/1.300	Base Spec 4.0, Table 8-7
			SSC	0.800/1.300	Base Spec 4.0, Table 8-7
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 471 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 472 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 473 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 474 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 475 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 476 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13.1	8.0 GT/s Specific Tx Voltage and Jitter Parameter Table
Table 4-19	8.0 GT/s Specific Tx Voltage and Jitter Parameters

Table 477 PCI Express Gen 4.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters

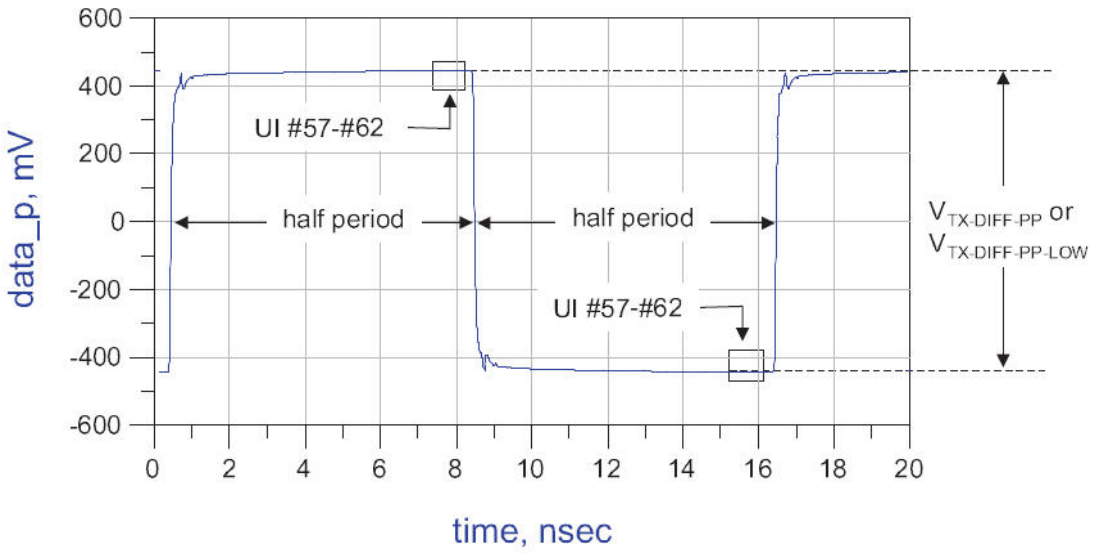


Figure 63 $V_{TX\text{-}FS\text{-}NO\text{-}EQ}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 "Compliance Patterns in Various Encodings".

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
4. Sets the **Horizontal Domain Scale** to 20.0µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Inputs the P4 saved waveform into SigTest tool.
8. Computes the measurement of Vb at preset value P4.
9. Reports the measurement of Vb during preset values P4.
10. Compares the de-emphasis value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Reduced Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during reduced swing signaling is within the conformance limits specified in Table 4-19 of the PCIE Base Specification, rev. 3.0, version.

The range for a transmitter's output voltage swing, (specified by V_d) with no equalization is defined by $V_{TH\text{-}RS\text{-}NO\text{-}EQ}$, and is obtained by setting c-1 and c+1 to zero and measuring the PP voltage on the 64-ones/64-zeros segment of the compliance pattern. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to last few UI of each half cycle (UI 57-62 of 64-ones/64-zeros). High frequency noise is mitigated by averaging over multiple reading until the PP noise over the area of interest is less than 2% of the magnitude of $V_{TH\text{-}RS\text{-}NO\text{-}EQ}$.

Pass Limits

Table 478 Passing Limits Table for Reduced Swing Tx Voltage with no TxEQ Test (Parameter: $V_{TX\text{-}RS\text{-}NO\text{-}EQ}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference

Table 478 Passing Limits Table for Reduced Swing Tx Voltage with no TxEQ Test (Parameter: $V_{TX\text{-}RS\text{-}NO\text{-}EQ}$)

PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	0.400/1.300	Base Spec 3.0, Table 4-19
			SSC	0.400/1.300	Base Spec 3.0, Table 4-19
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	0.400/1.300	Base Spec 4.0, Table 8-7
			SSC	0.400/1.300	Base Spec 4.0, Table 8-7
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (V) (Min/Max)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	0.400/1.300	Base Spec 4.0, Table 8-7
			SSC	0.400/1.300	Base Spec 4.0, Table 8-7
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 479 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 480 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 481 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 482 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 483 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 484 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13.1	8.0 GT/s Specific Tx Voltage and Jitter Parameter Table
Table 4-19	8.0 GT/s Specific Tx Voltage and Jitter Parameters

Table 485 PCI Express Gen 4.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters

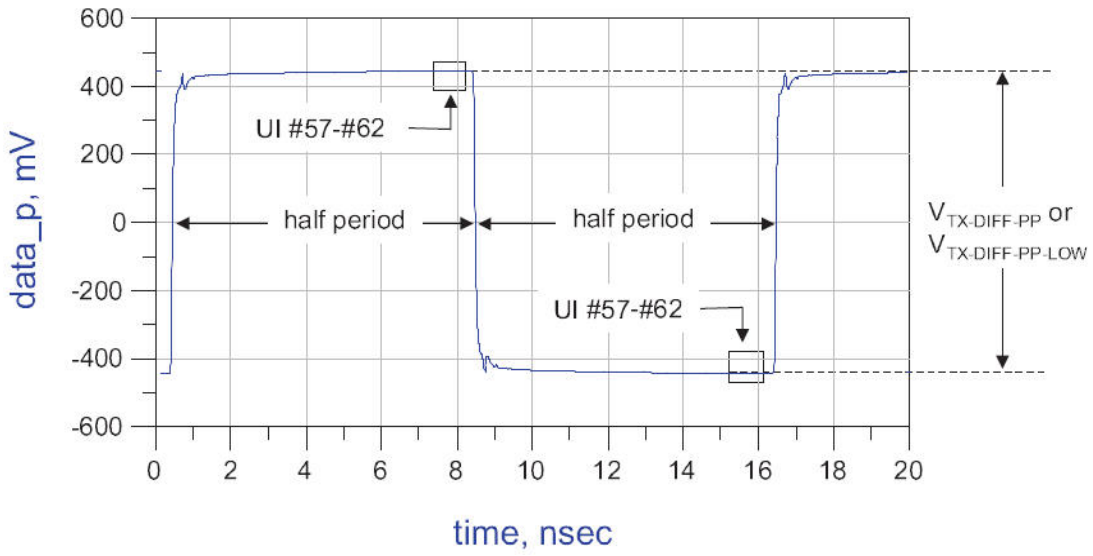


Figure 64 $V_{TX\text{-}FS\text{-}NO\text{-}EQ}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 "Compliance Patterns in Various Encodings".

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures **Memory Depth** to 8.00000 Mpts as **Manual** using **Acquisition Setup**.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Inputs the P4 saved waveform into SigTest tool.
8 Computes the measurement of Vb at preset value P4.
9 Reports the measurement of Vb during preset values P4.
10 Compares the de-emphasis value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Full Swing Test

This test verifies that the minimum swing during EIEOS for full swing $V_{TX\text{-}EIEOS\text{-}FS}$ is within the allowed range.

$V_{TX\text{-}EIEOS\text{-}FS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of eight consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX\text{-}EIEOS\text{-}FS}$ for full swing signaling and by $V_{TX\text{-}EIEOS\text{-}RS}$ for reduced swing signaling. $V_{TX\text{-}EIEOS\text{-}RS}$ is smaller than $V_{TX\text{-}EIEOS\text{-}FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $V_{TX\text{-}EIEOS\text{-}FS}$ is measured with a c+1 coefficient value of -0.33 and a c-1 coefficient of 0.00, corresponding to preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a boost tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 4-19. For reduced swing signaling $V_{TX\text{-}EIEOS\text{-}RS}$ is measured with a c+1 coefficient value of -0.167 and a c-1 coefficient of 0.00, corresponding to preset P1.

Both $V_{TX\text{-}EIEOS\text{-}FS}$ and $V_{TX\text{-}EIEOS\text{-}RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only the middle five UI. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX\text{-}EIEOS\text{-}FS}$ or $V_{TX\text{-}EIEOS\text{-}RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Pass Limits

Table 486 Passing Limits Table for Min Swing During EIEOS for Full Swing Test (Parameter: $V_{TX\text{-}EIEOS\text{-}FS}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference

Table 486 Passing Limits Table for Min Swing During EIEOS for Full Swing Test (Parameter: $V_{TX-EIEOS-FS}$)

PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	250.00	Base Spec 3.0, Table 4-19
			SSC	250.00	Base Spec 3.0, Table 4-19
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	250.00	Base Spec 4.0, Table 8-7
			SSC	250.00	Base Spec 4.0, Table 8-7
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	250.00	Base Spec 4.0, Table 8-7
			SSC	250.00	Base Spec 4.0, Table 8-7
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 487 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 488 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 489 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 490 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 491 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 492 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13.1	8.0 GT/s Specific Tx Voltage and Jitter Parameter Table
Table 4-19	8.0 GT/s Specific Tx Voltage and Jitter Parameters

Table 493 PCI Express Gen 4.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters

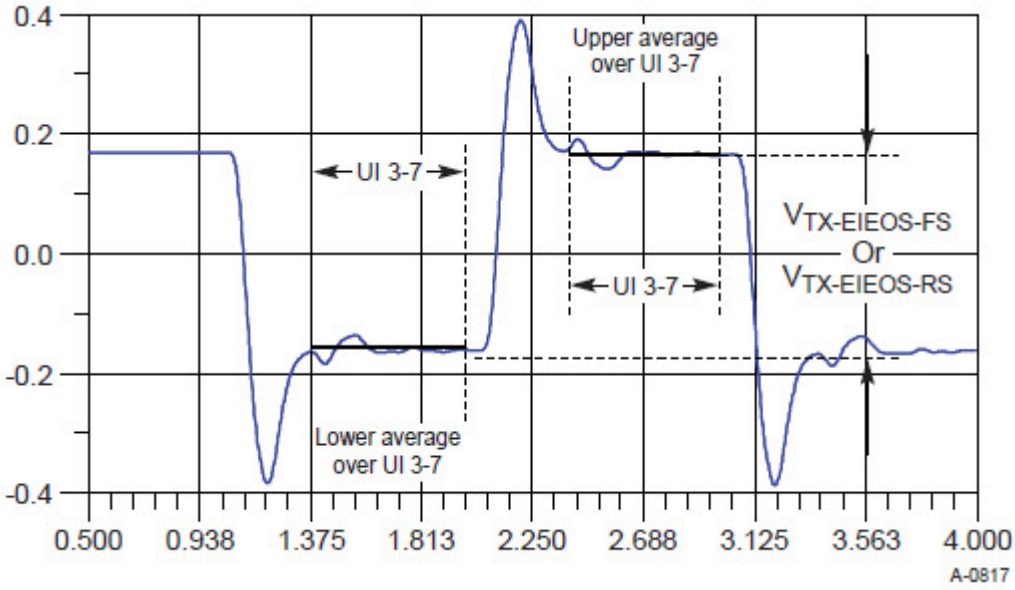


Figure 65 Measurement $V_{TX\text{-}EIEOS\text{-}FS}$ or $V_{TX\text{-}EIEOS\text{-}RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 "Compliance Patterns in Various Encodings".**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs actual compliance testing using the SigTest tools.

   a Gets input test waveform data from scope.

   b Acquires scope sample waveform data (re-iterate to capture at least 1M UI).

   c Performs the transmitter compliance test function using the SigTest tools.

   d Gets compliance test results from SigTest tools.

   e Finds and updates the worst case test result values.

   f Gets the average EIEOS high voltage.

   g Gets the average EIEOS low voltage.

   h Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Reduced Swing Test

This test verifies that the minimum swing during EIEOS for reduced swing $V_{TX-EIEOS-RS}$ is within the allowed range.

$V_{TX-EIEOS-FS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of eight consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX-EIEOS-FS}$ for full swing signaling and by $V_{TX-EIEOS-RS}$ for reduced swing signaling. $V_{TX-EIEOS-RS}$ is smaller than $V_{TX-EIEOS-FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $V_{TX-EIEOS-FS}$ is measured with a c+1 coefficient value of -0.33 and a c-1 coefficient of 0.00, corresponding to preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a boost tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 4-19. For reduced swing signaling $V_{TX-EIEOS-RS}$ is measured with a c+1 coefficient value of -0.167 and a c-1 coefficient of 0.00, corresponding to preset P1.

Both $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only the middle five UI. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Pass Limits

Table 494 Passing Limits Table for Min Swing During EIEOS for Reduced Swing Test (Parameter: $V_{TX-EIEOS-RS}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference

Table 494 Passing Limits Table for Min Swing During EIEOS for Reduced Swing Test (Parameter: $V_{TX-EIEOS-RS}$)

PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe3.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	232.00	Base Spec 3.0, Table 4-19
			SSC	232.00	Base Spec 3.0, Table 4-19
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe4.0	Base - Transmitter Tests	8.0 GT/s	Clean Clock	232.00	Base Spec 4.0, Table 8-7
			SSC	232.00	Base Spec 4.0, Table 8-7
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (mV) (Min)	Reference
PCIe4.0	Base - Transmitter Tests	16.0 GT/s	Clean Clock	232.00	Base Spec 4.0, Table 8-7
			SSC	232.00	Base Spec 4.0, Table 8-7
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 495 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 496 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 497 PCI Express Gen 2.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 498 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 499 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 500 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.3.13.1	8.0 GT/s Specific Tx Voltage and Jitter Parameter Table
Table 4-19	8.0 GT/s Specific Tx Voltage and Jitter Parameters

Table 501 PCI Express Gen 4.0, All GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.3.6	Data Rate Dependent Parameters
Table 8-7	Data Rate Dependent Transmitter Parameters

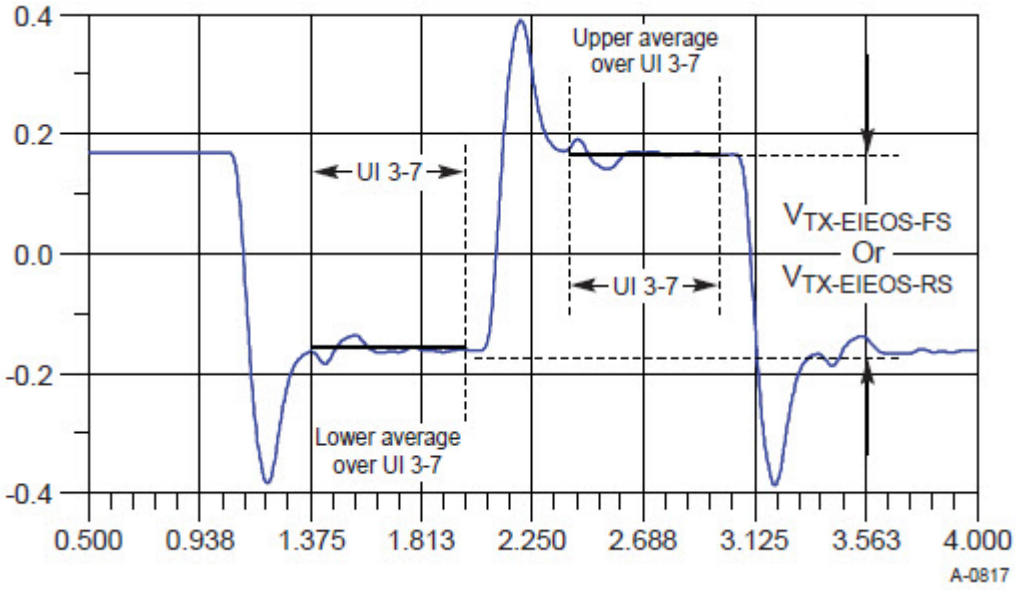


Figure 66 Measurement $V_{TX\text{-}EIEOS\text{-}FS}$ or $V_{TX\text{-}EIEOS\text{-}RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 "Compliance Patterns in Various Encodings".**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs actual compliance testing using the SigTest tools.

   a Gets input test waveform data from scope.

   b Acquires scope sample waveform data (re-iterate to capture at least 1M UI).

   c Performs the transmitter compliance test function using the SigTest tools.

   d Gets compliance test results from SigTest tools.

   e Finds and updates the worst case test result values.

   f Gets the average EIEOS high voltage.

   g Gets the average EIEOS low voltage.

   h Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

High Frequency >1.5 MHz RMS Jitter (Common Clk) (Data Clk) Test

This test verifies that the reference clock $T_{REFCLK-HF-RMS}$ is within the conformance limits specified in Table 4-31 of the PCIE Base Specification, rev. 3.0, version 0.71.

Pass Limits

Table 502 Passing Limits Table for High Frequency >1.5 MHz RMS Jitter (Common Clk) (Data Clk) Test (Parameter: $V_{REFCLK-HF-RMS}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	Reference Clock Tests	5.0 GT/s	Clean Clock	For CRefClk: 3.10 For DClk: 4.00	For Common RefClk: Base Spec 3.0, Table 4-31 For Data Clk: Base Spec 3.0, Table 4-33
			SSC	For CRefClk: 3.10 For DClk: 4.00	For Common RefClk: Base Spec 3.0, Table 4-31 or Data Clk: Base Spec 3.0, Table 4-33
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference

Table 502 Passing Limits Table for High Frequency >1.5 MHz RMS Jitter (Common Clk) (Data Clk) Test (Parameter: $V_{REFCLK-HF-RMS}$)

PCIe3.0	Reference Clock Tests	5.0 GT/s	Clean Clock	For CRefClk: 3.10 For DClk: 4.00	For Common RefClk: Base Spec 3.0, Table 4-31 For Data Clk: Base Spec 3.0, Table 4-33
			SSC	For CRefClk: 3.10 For DClk: 4.00	For Common RefClk: Base Spec 3.0, Table 4-31 or Data Clk: Base Spec 3.0, Table 4-33
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Reference Clock Tests	5.0 GT/s	Clean Clock	For CRefClk: 3.10	For Common RefClk: Base Spec 3.0, Table 4-31
			SSC	For CRefClk: 3.10	For Common RefClk: Base Spec 3.0, Table 4-31
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 503 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 504 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 505 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.7.3.3	Compliance Parameters for Common Refclk Rx Architecture
Table 4-31	Refclk Parameters for Common Refclk Rx Architecture at 5.0 GT/s
PCI Express™ Base Specification Revision 3.0	
Section 4.3.7.3.5	Compliance Parameters for Data Clocked Rx Architecture
Table 4-33	Refclk Parameters for Data Clocked Rx Architecture

Table 506 PCI Express Gen 2.0, All Other GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 507 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 508 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.7.3.3	Compliance Parameters for Common Refclk Rx Architecture
Table 4-31	Refclk Parameters for Common Refclk Rx Architecture at 5.0 GT/s
PCI Express™ Base Specification Revision 3.0	
Section 4.3.7.3.5	Compliance Parameters for Data Clocked Rx Architecture
Table 4-33	Refclk Parameters for Data Clocked Rx Architecture

Table 509 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 510 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.7.3.3	Compliance Parameters for Common Refclk Rx Architecture
Table 4-31	Refclk Parameters for Common Refclk Rx Architecture at 5.0 GT/s
PCI Express™ Base Specification Revision 3.0	
Section 4.3.7.3.5	Compliance Parameters for Data Clocked Rx Architecture
Table 4-33	Refclk Parameters for Data Clocked Rx Architecture

Table 511 PCI Express Gen 4.0, All Other GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Memory Depth** to 20.0000 Mpts as **Manual** using **Acquisition Setup**. If the desired option is not available, then it configures it to the highest available memory depth.
3. Fits and displays all sample data on screen.
4. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 Gsa/s, clock rate 100 MHz, each UI takes up 200 points. So for memory depth of 20M, each acquisition yields 100000 UIs. To achieve 1 million UIs, 10 acquisitions are required.
6. Stitches each acquired acquisition to make a continuous TIE data.
7. Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:
   - *a* Converts time domain TIE data to frequency domain.
   - *b* Applies a high pass filter to remove components which are <=1.5 MHz.
   - *c* Applies the PLL filter using parameters for common clocked architecture.
   - *d* Converts back the frequency domain TIE data to time domains.
   - *e* Computes the filtered peak-peak jitters and RMS jitter.
8. Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

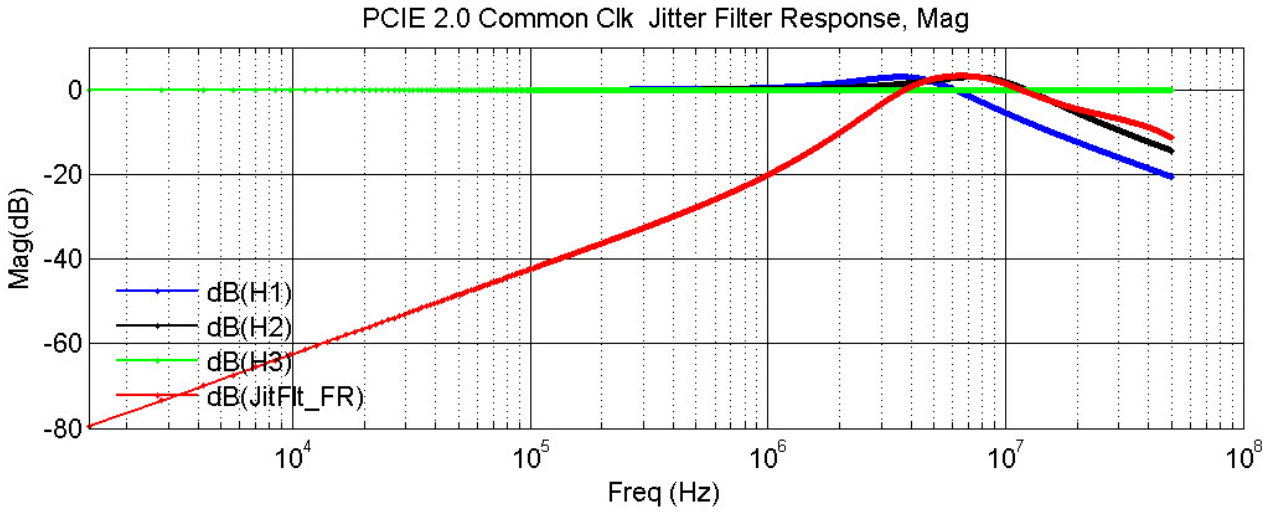


Figure 67 Common Clock Jitter Filter Response

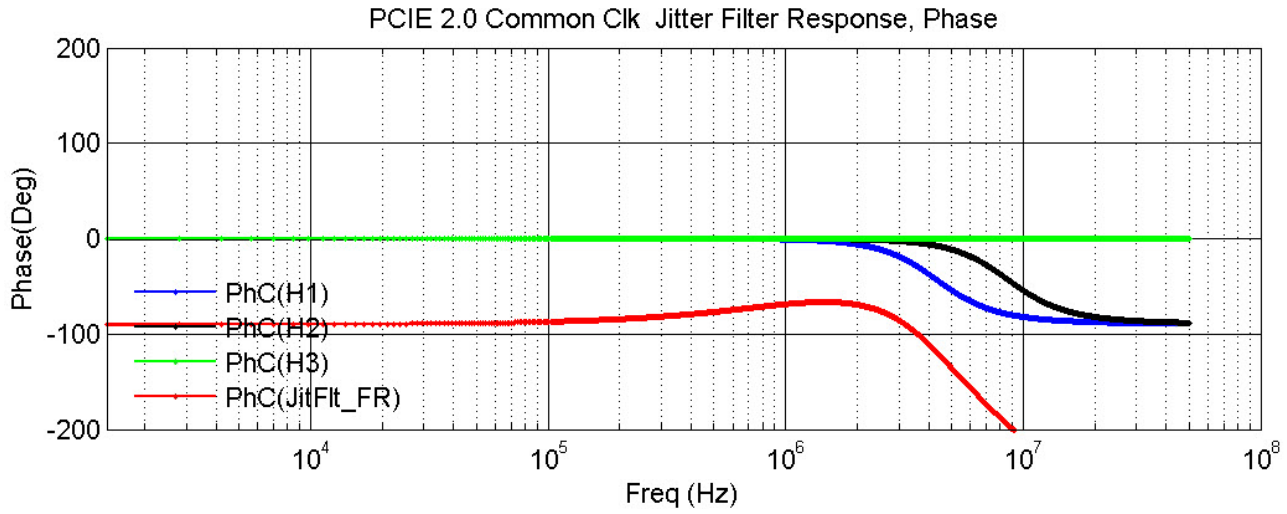


Figure 68 Common Clock Jitter Filter Response

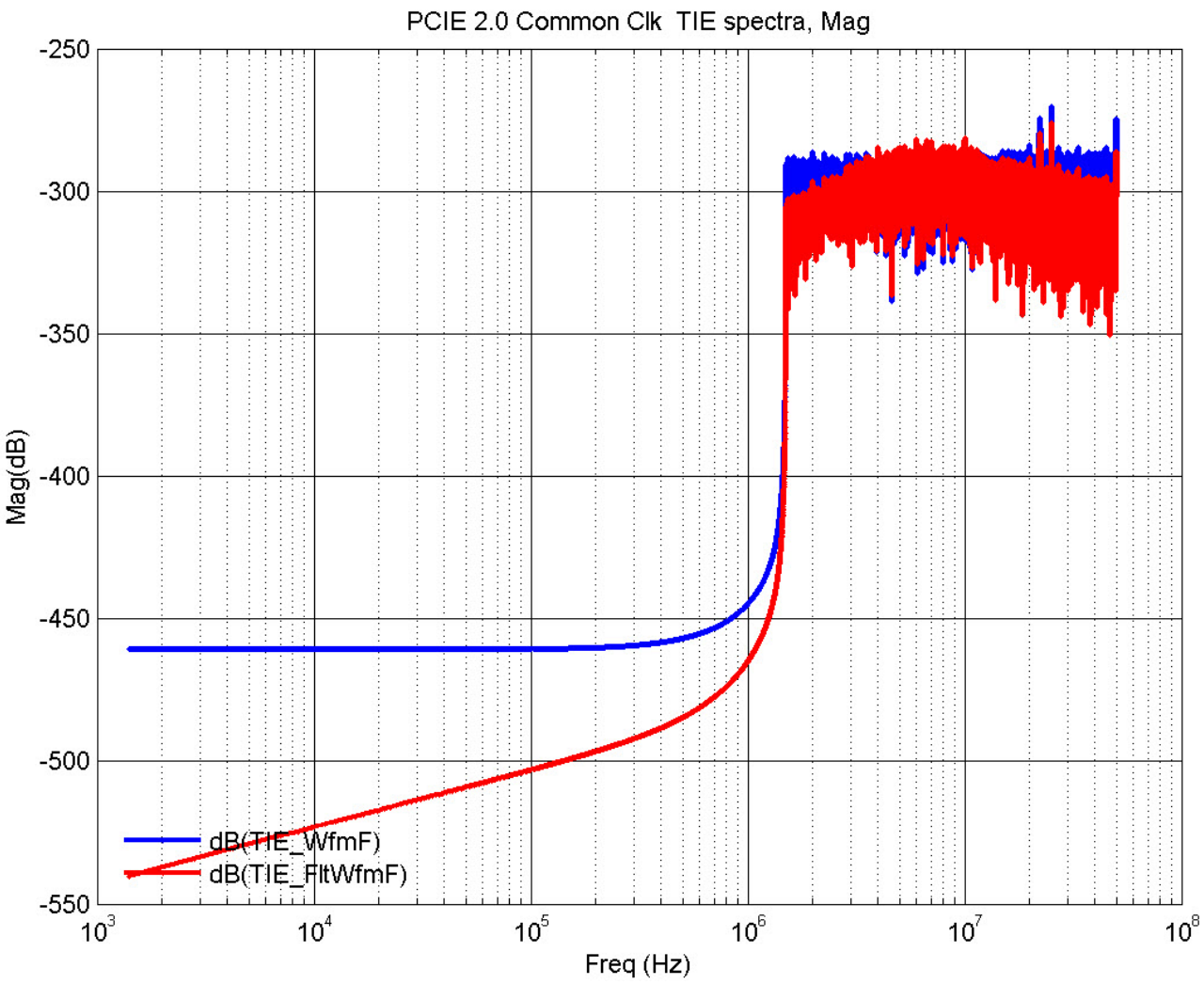


Figure 69 Common Clock TIE Spectra

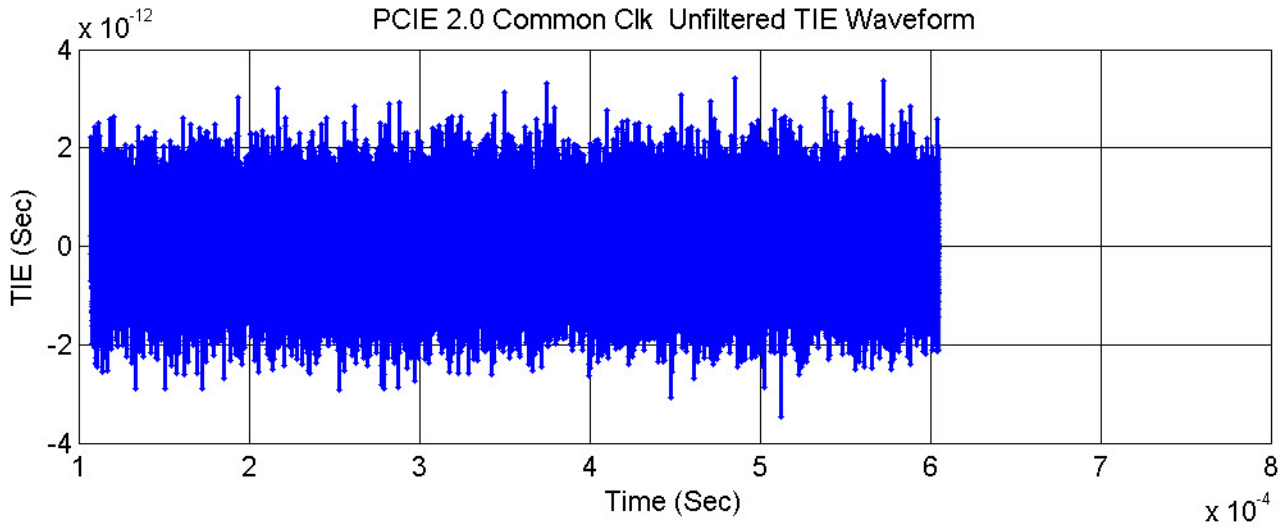


Figure 70 Common Clock Unfiltered TIE waveform

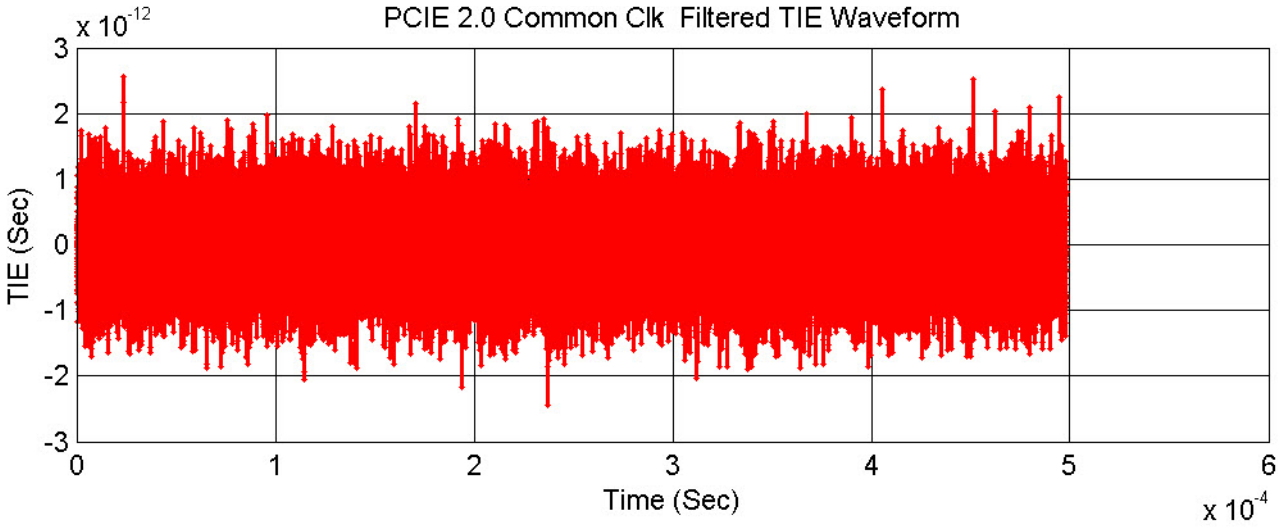


Figure 71 Common Clock Filtered TIE Waveform

SSC Residual (Common Clk) Test

This test verifies that the measured SSC residual is within the conformance limits specified in Table 4-31 of the PCIE Base Specification, rev. 3.0, version 0.71.

Pass Limits

Table 512 Passing Limits Table for SSC Residual (Common Clk) Test (Parameter: $T_{REFCLK-SSC-RES}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	Reference Clock Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	For CRefClk: 75.00	For Common RefClk: Base Spec 2.0, Table 4-16
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	Reference Clock Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	For CRefClk: 75.00	For Common RefClk: Base Spec 3.0, Table 4-31
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference

Table 512 Passing Limits Table for SSC Residual (Common Clk) Test (Parameter: $T_{REFCLK-SSC-RES}$)

PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Reference Clock Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	For CRefClk: 75.00	For Common RefClk: Base Spec 3.0, Table 4-31
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 513 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 514 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 515 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.7.2.3	Refclk Compliance Parameters for Common Refclk Rx Architecture
Table 4-16	Refclk Parameters for Common Refclk Rx Architecture at 5.0 GT/s

Table 516 PCI Express Gen 2.0, All Other GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 517 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 518 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.7.3.3	Compliance Parameters for Common Refclk Rx Architecture
Table 4-31	Refclk Parameters for Common Refclk Rx Architecture at 5.0 GT/s

Table 519 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 520 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.7.3.3	Compliance Parameters for Common Refclk Rx Architecture
Table 4-31	Refclk Parameters for Common Refclk Rx Architecture at 5.0 GT/s

Table 521 PCI Express Gen 4.0, All Other GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Memory Depth** to 20.0000Mpts as **Manual** using **Acquisition Setup**. If the desired option is not available, then it configures it to the highest available memory depth.
3. Fits and displays all sample data on screen.
4. Analyzes Time Interval Error (TIE) measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20Gsa/s, clock rate 100MHz, each UI takes up 200 points. So for memory depth of 20M, each acquisition yields 100000 UIs. To achieve 1 million UIs, 10 acquisitions are required.
6. Stitches each acquired acquisition to make a continuous TIE data.
7. Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:
   a Converts time domain TIE data to frequency domain.
   b Applies a high pass filter to remove components which are <=1.5MHz.
   c Applies the PLL filter using parameters for common clocked architecture.
   d Converts back the frequency domain TIE data to time domains.
   e Computes the filtered peak-peak jitters and RMS jitter.
8. Reports filtered peak-peak jitter as SSC residual and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Low Frequency 10 kHz to 1.5 MHz RMS Jitter (Common Clk) (Data Clk) Test

This test verifies that the reference clock $T_{REFCLK-LF-RMS}$ is within the conformance limits specified in, Table 4-31 of the PCIE Base Specification, rev. 3.0, version 0.71.

Pass Limits

Table 522 Passing Limits Table for Low Frequency 10 kHz to 1.5 MHz RMS Jitter (Common Clk) (Data Clk) Test (Parameter: $T_{REFCLK-LF-RMS}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	Reference Clock Tests	5.0 GT/s	Clean Clock	For CRefClk: 3.00 For DClk: 7.50	For Common RefClk: Base Spec 2.0, Table 4-16 F or Data Clk: Base Spec 2.0, Table 4-18
			SSC	For CRefClk: 3.00 For DClk: 7.50	For Common RefClk: Base Spec 2.0, Table 4-16 F or Data Clk: Base Spec 2.0, Table 4-18
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference

Table 522 Passing Limits Table for Low Frequency 10 kHz to 1.5 MHz RMS Jitter (Common Clk) (Data Clk) Test (Parameter: $T_{REFCLK-LF-RMS}$)

PCIe3.0	Reference Clock Tests	5.0 GT/s	Clean Clock	For CRefClk: 3.00 For DClk: 7.50	For Common RefClk: Base Spec 3.0, Table 4-31 For Data Clk: Base Spec 3.0, Table 4-33
			SSC	For CRefClk: 3.10 For DClk: 7.50	For Common RefClk: Base Spec 3.0, Table 4-31 F or Data Clk: Base Spec 3.0, Table 4-33
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Reference Clock Tests	5.0 GT/s	Clean Clock	For CRefClk: 3.00	For Common RefClk: Base Spec 3.0, Table 4-31
			SSC	For CRefClk: 3.00	For Common RefClk: Base Spec 3.0, Table 4-31
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 523 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 524 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 525 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.7.2.3	Refclk Compliance Parameters for Common Refclk Rx Architecture
Table 4-16	Refclk Parameters for Common Refclk Rx Architecture at 5.0 GT/s

Table 526 PCI Express Gen 2.0, All Other GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 527 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 528 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.7.3.3	Compliance Parameters for Common Refclk Rx Architecture
Table 4-31	Refclk Parameters for Common Refclk Rx Architecture at 5.0 GT/s
PCI Express™ Base Specification Revision 3.0	
Section 4.3.7.3.5	Compliance Parameters for Data Clocked Rx Architecture
Table 4-33	Refclk Parameters for Data Clocked Rx Architecture

Table 529 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 530 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.7.3.3	Compliance Parameters for Common Refclk Rx Architecture
Table 4-31	Refclk Parameters for Common Refclk Rx Architecture at 5.0 GT/s

Table 531 PCI Express Gen 4.0, All Other GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures **Memory Depth** to 20.0000Mpts as **Manual** using **Acquisition Setup**. If the desired option is not available, then it configures it to the highest available memory depth.

3 Fits and displays all sample data on screen.

4 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.

5 Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20Gsa/s, clock rate 100MHz, each UI takes up 200 points. So for memory depth of 20M, each acquisition yields 100000 UIs. To achieve 1 million UIs, 10 acquisitions are required.

6 Stitches each acquired acquisition to make a continuous TIE data.

7 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:

a Converts time domain TIE data to frequency domain.

b Applies a band pass filter to remove components which are <10KHz and >1.5MHz.

c Applies the PLL filter using parameters for common clocked architecture.

d Removes SSC components (fundamental and harmonics).

e Converts back the frequency domain TIE data to time domains.

f Computes the filtered peak-peak jitters and RMS jitter.

8 Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

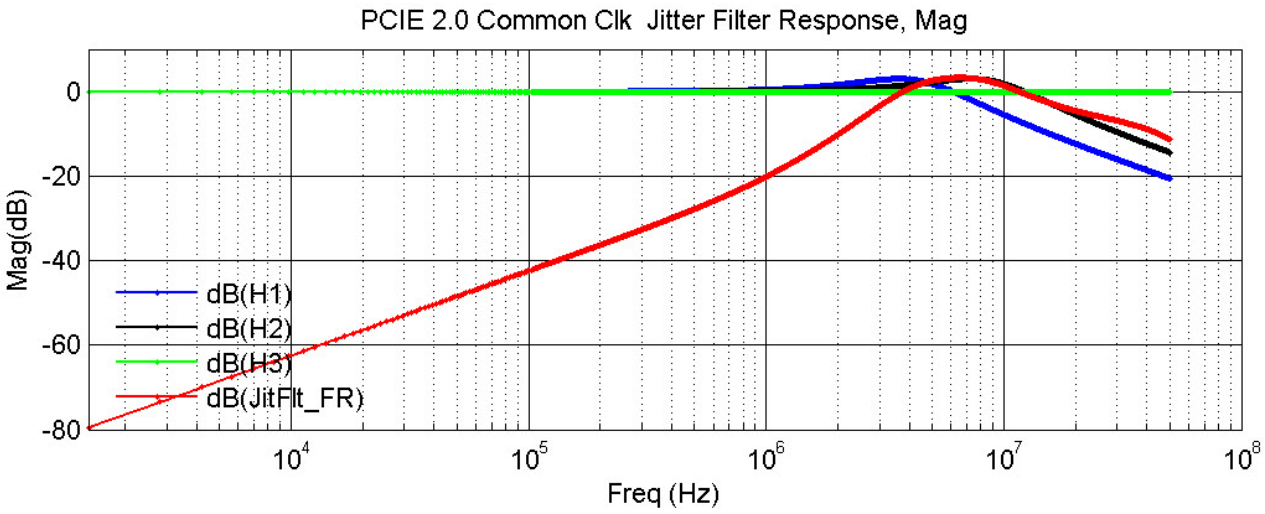


Figure 72 Common Clock Jitter Response

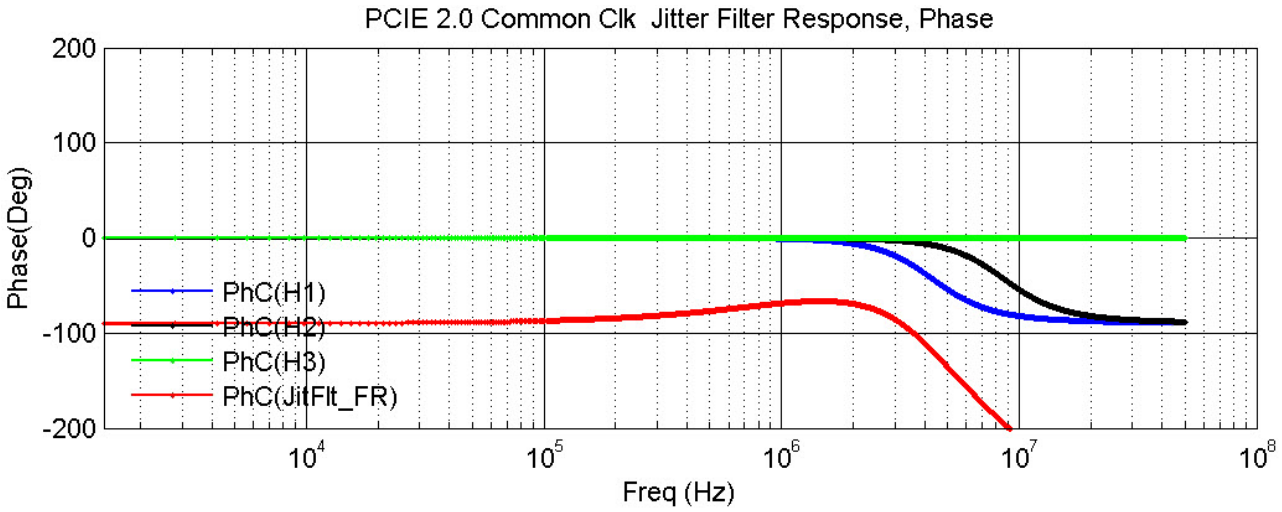


Figure 73 Common Clock Jitter Filter Response

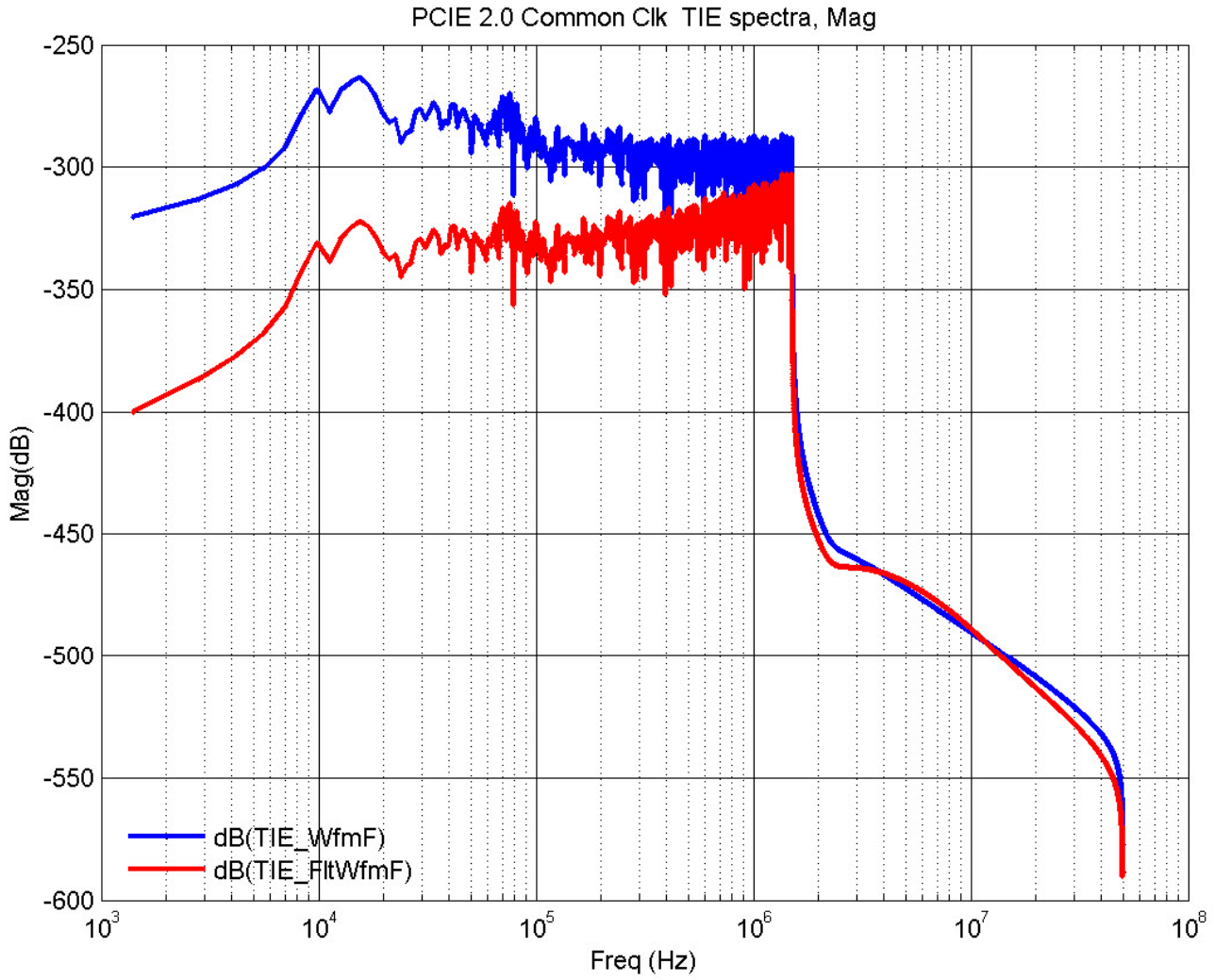


Figure 74 Common Clock TIE Spectra

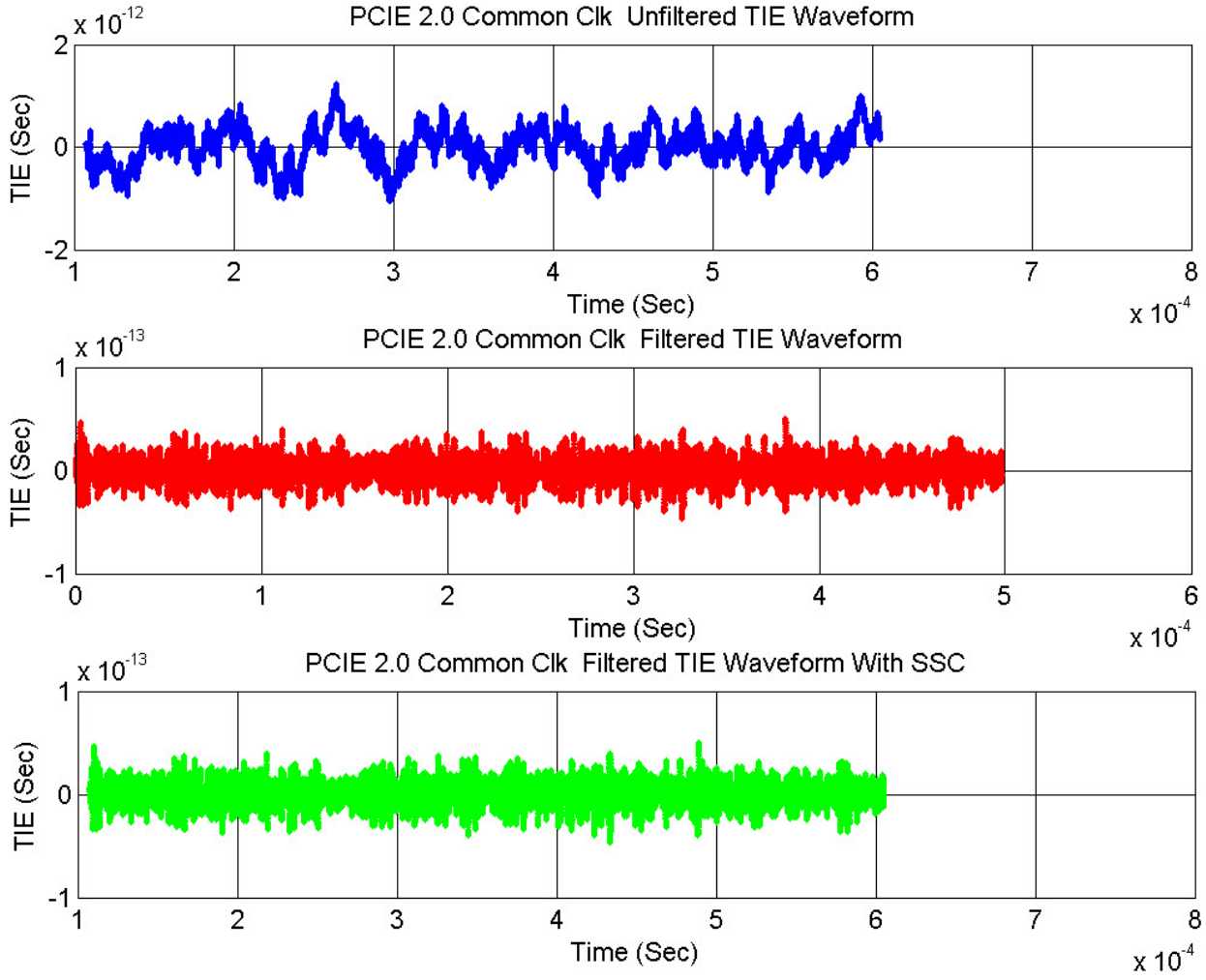


Figure 75 Common Clock TIE Waveform

SSC Deviation (Common Clk) (Data Clk) Test

This test verifies that the reference clock SSC deviation is within the conformance limits specified in Table 4-31 of the PCIE Base Specification, rev. 3.0, version 0.71.

Pass Limits

Table 532 Passing Limits Table for SSC Deviation (Common Clk) (Data Clk) Test (Parameter: $T_{SSC-FREQ-DEVIATION}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe2.0	Reference Clock Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	For CRefClk: -0.5/0.0 For DClk: -0.5/0.0	For Common RefClk: Base Spec 2.0, Table 4-16 For Data Clk: Base Spec 2.0, Table 4-16
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference

Table 532 Passing Limits Table for SSC Deviation (Common Clk) (Data Clk) Test (Parameter: $T_{SSC-FREQ-DEVIATION}$)

PCIe3.0	Reference Clock Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	For CRefClk: -0.53/0.03 For DClk: -0.53/0.03	For Common RefClk: Base Spec 3.0, Table 4-31 For Data Clk: Base Spec 3.0, Table 4-33
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe3.0	Reference Clock Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	For CRefClk: -0.53/0.03 For DClk: -0.53/0.03	For Common RefClk: Base Spec 3.0, Table 4-34 For Data Clk: Base Spec 3.0, Table 4-35
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe4.0	Reference Clock Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	For CRefClk: -0.5/0.0 For DClk: -0.5/0.0	For Common RefClk: Base Spec 4.0, Table 8-18 For Data Clk: Base Spec 4.0, Table 8-18
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe4.0	Reference Clock Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	For CRefClk: -0.5/0.0	For Common RefClk: Base Spec 4.0, Table 8-18
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 532 Passing Limits Table for SSC Deviation (Common Clk) (Data Clk) Test (Parameter: $T_{SSC-FREQ-DEVIATION}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (%) (Min/Max)	Reference
PCIe4.0	Reference Clock Tests	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	For CRefClk: -0.5/0.0	For Common RefClk: Base Spec 4.0, Table 8-18
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 533 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 534 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 535 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 536 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.7.2.3	Refclk Compliance Parameters for Common Refclk Rx Architecture
Table 4-16	Refclk Parameters for Common Refclk Rx Architecture at 5.0 GT/s

Table 537 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 538 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.7.3.3	Compliance Parameters for Common Refclk Rx Architecture
Table 4-31	Refclk Parameters for Common Refclk Rx Architecture at 5.0 GT/s

Table 538 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.7.3.5	Compliance Parameters for Data Clocked Rx Architecture
Table 4-33	Refclk Parameters for Data Clocked Rx Architecture

Table 539 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.8.2	Common Refclk Rx Architecture
Table 4-34	Parameters for Common Refclk Rx Architecture at 8.0 GT/s
PCI Express™ Base Specification Revision 3.0	
Section 4.3.8.3	Data Clocked Refclk Rx Architecture
Table 4-35	Parameters for Data Clocked Rx Architecture at 8.0 GT/s

Table 540 PCI Express Gen 4.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 541 PCI Express Gen 4.0, Data Rate 5.0, 8.0, and 16.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.3	Data Rate Independent Refclk Parameters
Table 8-18	Data Rate Independent Refclk Parameters

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
4 Uses markers to indicate upper and lower limit (trend data of periodic measurements).
5 Measures Period_max, Period_min and Period_average.
6 Reports the measurement results.
7 Calculates SSC deviation% = (MaxPeriod - MinPeriod)/MinPeriod * 100%

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Maximum SSC Slew Rate (Common Clk) (Data Clk) Test

This test verifies that the reference clock SSC slew rate is within the conformance limits specified in the PCIE Base Specification.

Pass Limits

Table 542 Passing Limits Table for Maximum SSC Slew Rate (Common Clk) (Data Clk) Test (Parameter: $T_{SSC-MAX-PERIOD-SLEW}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (fs/UI) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (fs/UI) (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (fs/UI) (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (fs/UI) (Max)	Reference
PCIe2.0	Reference Clock Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	For CRefClk: 750.00 For DClk: 750.00	For Common RefClk: Base Spec 2.0, Table 4-16 For Data Clk: Base Spec 2.0, Table 4-16
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (fs/UI) (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (fs/UI) (Max)	Reference
PCIe3.0	Reference Clock Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	For CRefClk: 750.00 For DClk: 750.00	For Common RefClk: Base Spec 3.0, Table 4-31 For Data Clk: Base Spec 3.0, Table 4-33
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 542 Passing Limits Table for Maximum SSC Slew Rate (Common Clk) (Data Clk) Test (Parameter: $T_{SSC-MAX-PERIOD-SLEW}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (fs/UI) (Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (fs/UI) (Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (fs/UI) (Max)	Reference
PCIe4.0	Reference Clock Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	For CRefClk: 750.00	For Common RefClk: Base Spec 3.0, Table 4-31
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (fs/UI) (Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (fs/UI) (Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 543 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 544 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 545 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 546 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.7.2.3	Refclk Compliance Parameters for Common Refclk Rx Architecture
Table 4-16	Refclk Parameters for Common Refclk Rx Architecture at 5.0 GT/s

Table 547 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 548 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.7.3.3	Compliance Parameters for Common Refclk Rx Architecture
Table 4-31	Refclk Parameters for Common Refclk Rx Architecture at 5.0 GT/s
PCI Express™ Base Specification Revision 3.0	
Section 4.3.7.3.5	Compliance Parameters for Data Clocked Rx Architecture
Table 4-33	Refclk Parameters for Data Clocked Rx Architecture

Table 549 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 550 PCI Express Gen 4.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 551 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.7.3.3	Compliance Parameters for Common Refclk Rx Architecture
Table 4-31	Refclk Parameters for Common Refclk Rx Architecture at 5.0 GT/s

Table 552 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 553 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

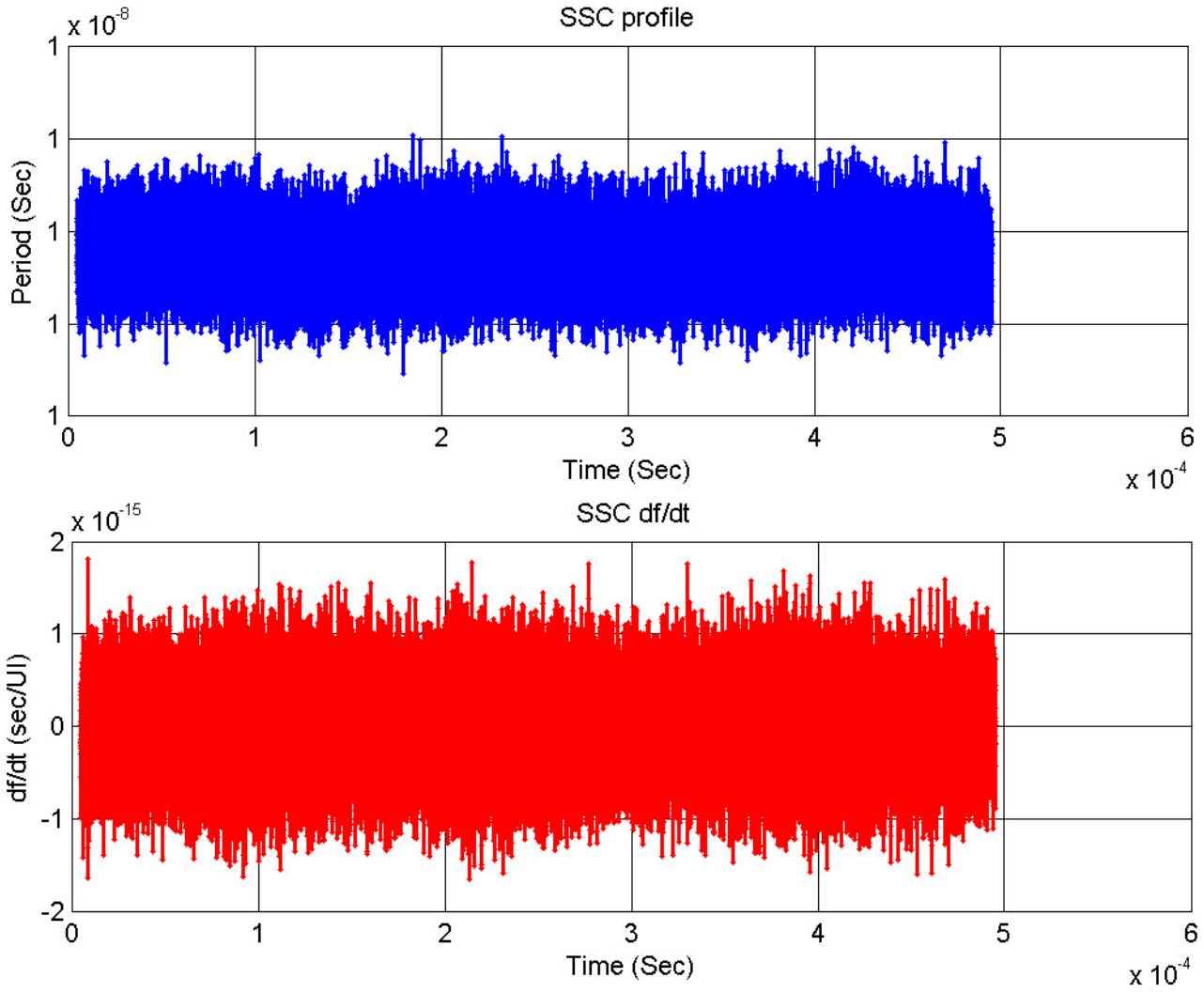
3 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.

4 The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function generates a differential plot ($x_n - x_{n-1}$). The maximum slew rate corresponds to the peak of the differential plot.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Full SSC Modulation (Data Clk) Test

This test verifies that the reference clock full SSC modulation is within the conformance limits specified in the PCIE Base Specification.

Pass Limits

Table 554 Passing Limits Table for Full SSC Modulation (Data Clk) Test (Parameter: $T_{REFCLK-SSC-FULL}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ns) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ns) (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ns) (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ns) (Max)	Reference
PCIe2.0	Reference Clock Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	For CRefClk: N/A For DClk: 20.00	For Common RefClk: N/A (Not Applicable) For Data Clk: Base Spec 2.0, Table 4-18
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ns) (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ns) (Max)	Reference
PCIe3.0	Reference Clock Tests	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	For CRefClk: N/A For DClk: 20.00	For Common RefClk: N/A (Not Applicable) For Data Clk: Base Spec 3.0, Table 4-33
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 554 Passing Limits Table for Full SSC Modulation (Data Clk) Test (Parameter: $T_{REFCLK-SSC-FULL}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ns) (Max)	Reference
PCIe3.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ns) (Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ns) (Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ns) (Max)	Reference
PCIe4.0	All	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ns) (Max)	Reference
PCIe4.0	All	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 555 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 556 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 557 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 558 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
Section 4.3.7.2.5	Refclk Compliance Parameters for Data Clocked Rx Architecture
Table 4-18	Refclk Parameters for Data Clocked Rx Architecture

Table 559 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 560 CI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.7.3.5	Compliance Parameters for Data Clocked Rx Architecture
Table 4-33	Refclk Parameters for Data Clocked Rx Architecture

Table 561 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 562 PCI Express Gen 4.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 563 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 564 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 565 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Memory Depth** to 20.0000 Mpts as **Manual** using **Acquisition Setup**. If the desired option is not available, then it configures it to the highest available memory depth.
3. Fits and displays all sample data on screen.
4. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20Gsa/s, clock rate 100MHz, each UI takes up 200 points. So for memory depth of 20M, each acquisition yields 100000 UIs. To achieve 1 million UIs, 10 acquisitions are required.
6. Stitches each acquired acquisition to make a continuous TIE data.
7. Analyzes the stitched TIE data using a MATLAB (PCIEMatlabFunction) function. The MATLAB function does the following:
   a Converts time domain TIE data to frequency domain.
   b Applies a band pass filter to remove components which are <=10KHz and components which are >=1.5MHz.
   c Applies the PLL filter using parameters for data clocked architecture.
   d Converts back the frequency domain TIE data to time domains.
   e Computes the peak-peak jitters. This value corresponds to the full SSC modulation since the SSC components were not removed.
8. Reports the peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Clock Frequency (Common Clk) (Data Clk) Test

This test verifies that the measured reference clock frequency is within the conformance limits specified in the PCIE Base Specification.

Pass Limits

Table 566 Passing Limits Table for Clock Frequency (Common Clk) (Data Clk) Test (Parameter: F_{REFCLK})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	Reference Clock Tests	8.0 GT/s	Clean Clock	For CRefClk: 99.97/100.03 For DClk: 99.97/100.03	For Common RefClk: Base Spec 3.0, Table 4-34 For Data Clk: Base Spec 3.0, Table 4-35
			SSC	N/A	N/A (Not Applicable)
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 566 Passing Limits Table for Clock Frequency (Common Clk) (Data Clk) Test (Parameter: F_{REFCLK})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Reference Clock Tests	8.0 GT/s	Clean Clock	For CRefClk: 99.97/100.03	For Common RefClk: Base Spec 4.0, Table 8-18
			SSC	N/A	N/A (Not Applicable)
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Reference Clock Tests	16.0 GT/s	Clean Clock	For CRefClk: 99.97/100.03	For Common RefClk: Base Spec 4.0, Table 8-18
			SSC	N/A	N/A (Not Applicable)
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 567 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 568 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 569 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 570 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 571 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 572 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 573 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.8.2	Common Refclk Rx Architecture
Table 4-34	Parameters for Common Refclk Rx Architecture at 8.0 GT/s
Section 4.3.8.3	Data Clocked Refclk Rx Architecture
Table 4-35	Parameters for Data Clocked Rx Architecture at 8.0 GT/s

Table 574 PCI Express Gen 4.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 575 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 576 PCI Express Gen 4.0, Data Rate 8.0 GT/s and 16.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.3	Data Rate Independent Refclk Parameters
Table 8-18	Data Rate Independent Refclk Parameters

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE To execute the test, follow the procedure in "Running Signal Quality Tests" on page 53 and select **Clock Frequency (Common Clk) (Data Clk).**

1 Gets the reference clock signal.
2 Verifies that the signal period is ~100 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Sets the time scale to 5 ns.
5 Fits and displays all sample data on the screen.
6 Enables jitter analysis so that measurements are made on all edges.
7 Measures the clock frequency.
8 Reports the mean frequency.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

RMS Jitter (Common Clk) (Data Clk) Test

This test verifies that the measured reference clock frequency is within the conformance limits specified in Table 4-34 of the PCIE Base Specification, rev. 3.0

Pass Limits

Table 577 Passing Limits Table for RMS Jitter (Common Clk) (Data Clk) Test (Parameter: $T_{REFCLK-RMS-CC}$)

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe3.0	Reference Clock Tests	8.0 GT/s	Clean Clock	For CRefClk: 1.00 For DClk: 1.00	For Common RefClk: Base Spec 3.0, Table 4-34 For Data Clk: Base Spec 3.0, Table 4-35
			SSC	For CRefClk: 1.00 For DClk: 1.00	For Common RefClk: Base Spec 3.0, Table 4-34 For Data Clk: Base Spec 3.0, Table 4-35

Table 577 Passing Limits Table for RMS Jitter (Common Clk) (Data Clk) Test (Parameter: $T_{REFCLK-RMS-CC}$)

	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Reference Clock Tests	5.0 GT/s	Clean Clock	For CRefClk: 3.10	For Common RefClk: Base Spec 4.0, Table 8-22
			SSC	For CRefClk: 3.10	For Common RefClk: Base Spec 4.0, Table 8-22
	All Other	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Reference Clock Tests	8.0 GT/s	Clean Clock	For CRefClk: 1.00	For Common RefClk: Base Spec 4.0, Table 8-22
			SSC	For CRefClk: 1.00	For Common RefClk: Base Spec 4.0, Table 8-22
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (ps) (Max)	Reference
PCIe4.0	Reference Clock Tests	16.0 GT/s	Clean Clock	For CRefClk: 0.5	For Common RefClk: Base Spec 4.0, Table 8-22
			SSC	For CRefClk: 0.5	For Common RefClk: Base Spec 4.0, Table 8-22
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 578 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 579 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 580 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 581 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 582 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 583 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 584 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.8.2	Common Refclk Rx Architecture
Table 4-34	Parameters for Common Refclk Rx Architecture at 8.0 GT/s
Section 4.3.8.3	Data Clocked Refclk Rx Architecture
Table 4-35	Parameters for Data Clocked Rx Architecture at 8.0 GT/s

Table 585 PCI Express Gen 4.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 586 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.7	Jitter Limits for Refclk Architectures
Table 8-22	Jitter Limits for CC Architecture

Table 587 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0
Please refer to Table 586, “PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes,”.

Table 588 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0
Please refer to Table 586, “PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes,”.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Verifies that the signal period is ~100MHz.
3. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5. Configures **Memory Depth** to **50.0000Mpts** as **Manual** using **Acquisition Setup**. If the desired option is not available, then it configures it to the highest available memory depth.
6. Fits and displays all sample data on the screen.
7. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8. Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 Gsa/s, clock rate 100 MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.
9. Stitches each acquired acquisition to make a continuous TIE data.
10. Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:
    a Converts time domain TIE data to frequency domain.
    b Applies the PLL filter using parameters for common clocked architecture.
    c Converts back the frequency domain TIE data to time domains.
    d Computes the filtered peak-peak jitters and RMS jitter.
11. Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

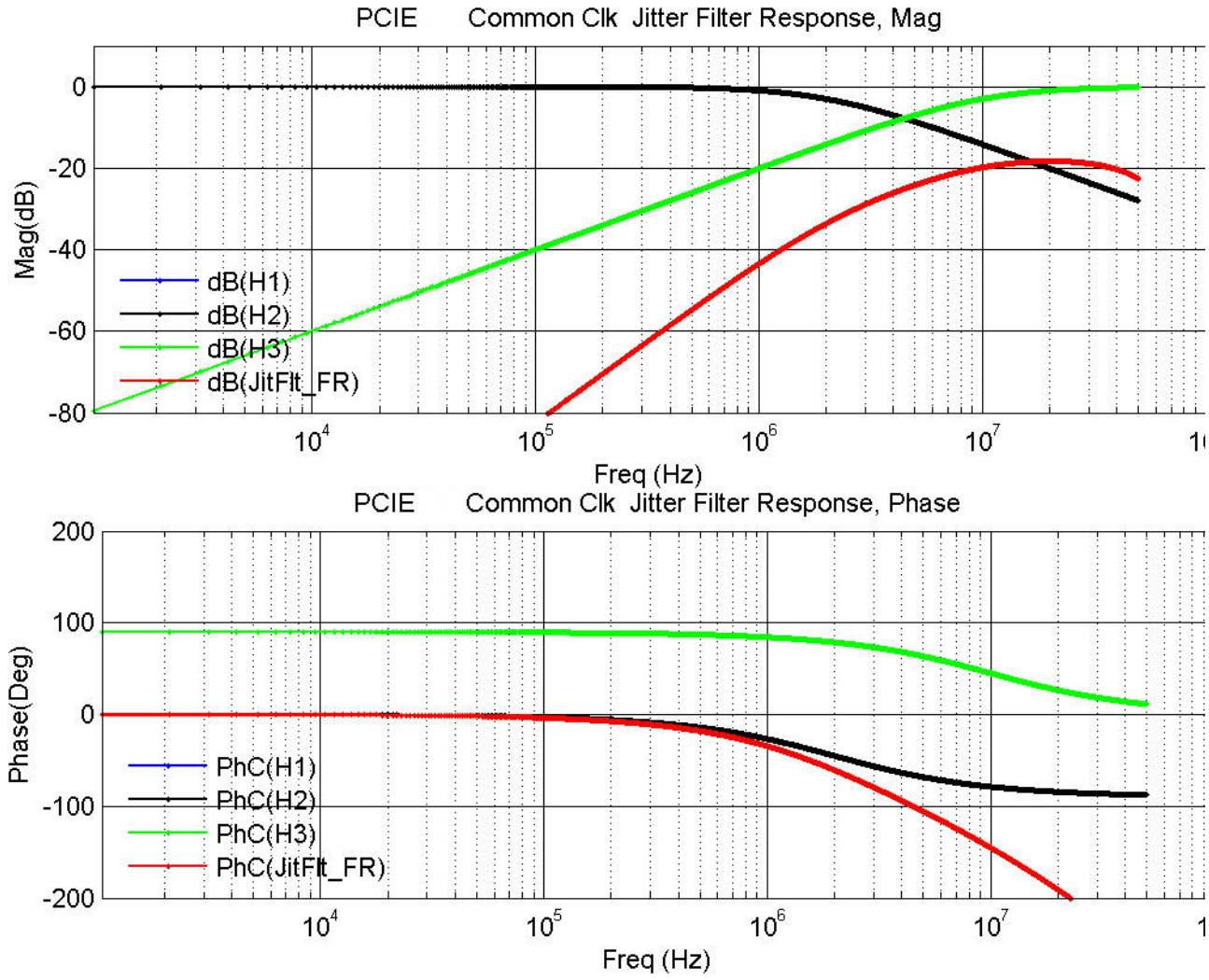


Figure 76 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

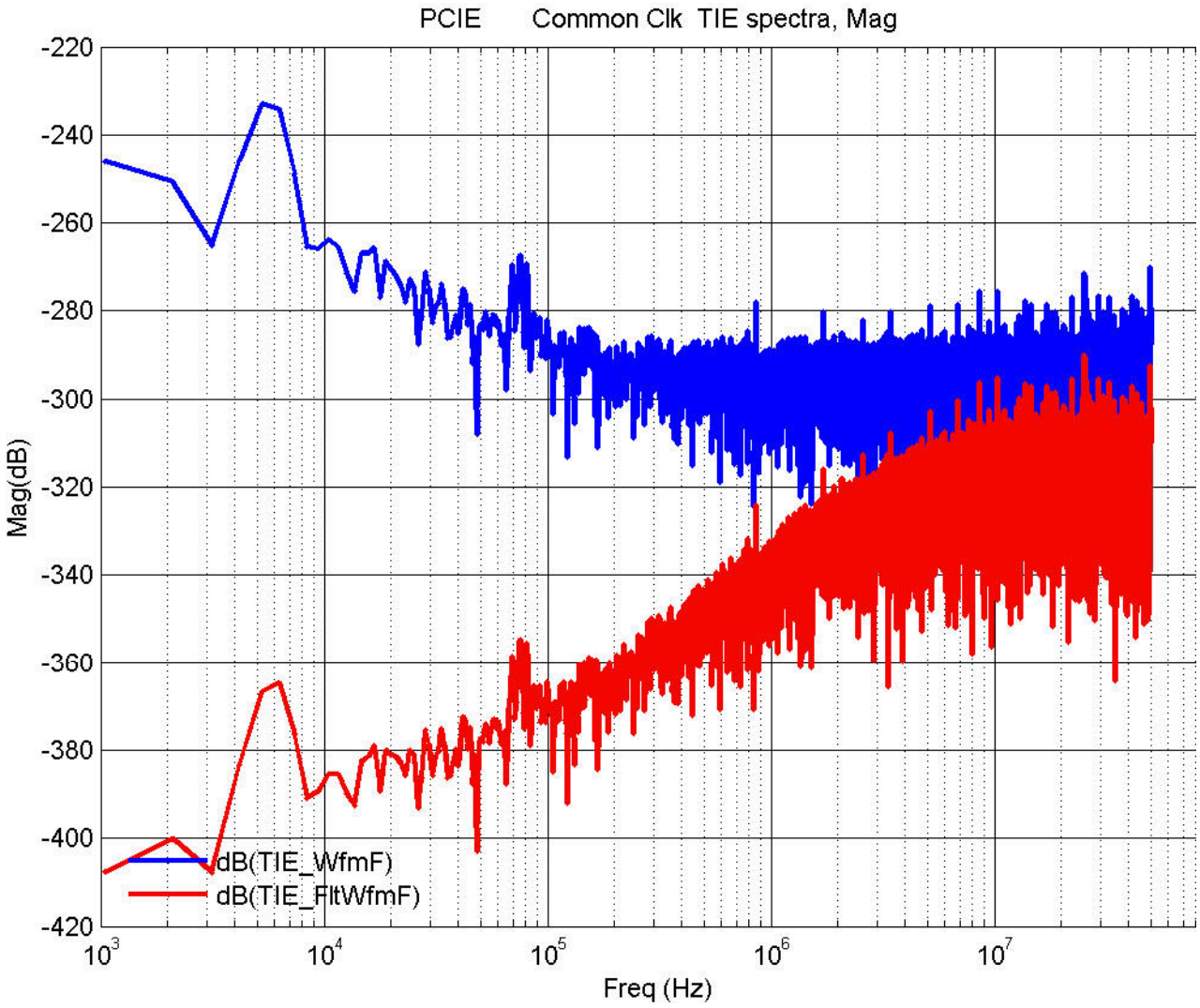


Figure 77 Reference Image for Common Clock TIE Spectra RMS Jitter Test

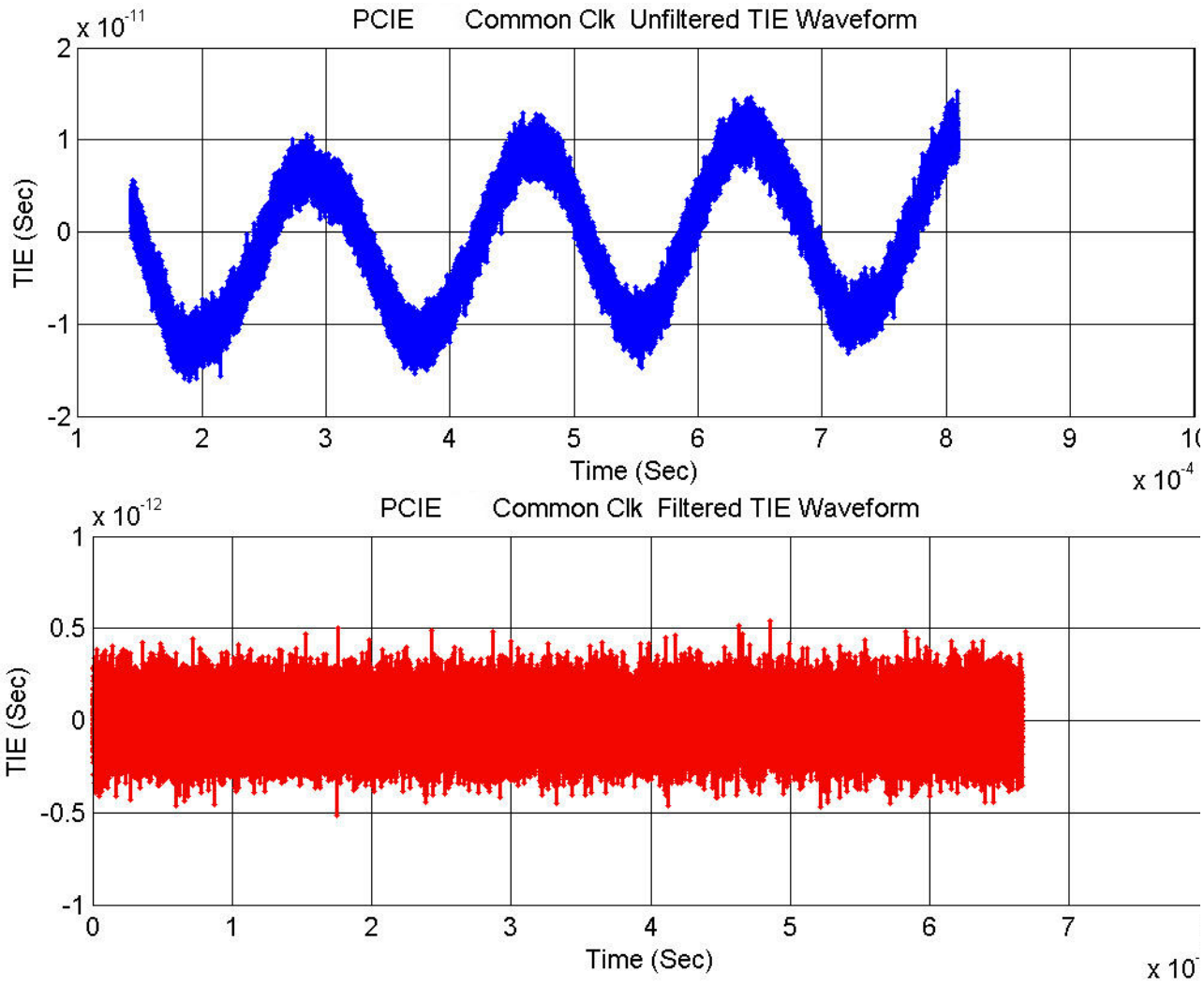


Figure 78 Reference Image for TIE Waveform RMS Jitter Test

SSC Frequency Range (Common Clk) (Data Clk)Test

This test verifies that the measured reference clock frequency is within the conformance limits specified in PCIE Base Specification.

Pass Limits

Table 589 Passing Limits Table for SSC Frequency Range (Common Clk) (Data Clk) Test (Parameter: F_{SSC})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (kHz) (Min/Max)	Reference
PCIe1.0a	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (kHz) (Min/Max)	Reference
PCIe1.1	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (kHz) (Min/Max)	Reference
PCIe2.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (kHz) (Min/Max)	Reference
PCIe2.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (kHz) (Min/Max)	Reference
PCIe3.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (kHz) (Min/Max)	Reference
PCIe3.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (kHz) (Min/Max)	Reference
PCIe3.0	Reference Clock Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	For CRefClk: 30.00/33.00 For DClk: 30.00/33.00	For Common RefClk: Base Spec 3.0, Table 4-34 For Data Clk: Base Spec 3.0, Table 4-35
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 589 Passing Limits Table for SSC Frequency Range (Common Clk) (Data Clk) Test (Parameter: F_{SSC})

Device	Test Point	Data Rate	Ref. Clock	Pass Limits (kHz) (Min/Max)	Reference
PCIe4.0	All	2.5 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (kHz) (Min/Max)	Reference
PCIe4.0	All	5.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (kHz) (Min/Max)	Reference
PCIe4.0	Reference Clock Tests	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	For CRefClk: 30.00/33.00	For Common RefClk: Base Spec 4.0, Table 8-18
	All Other	8.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)
Device	Test Point	Data Rate	Ref. Clock	Pass Limits (kHz) (Min/Max)	Reference
PCIe4.0	Reference Clock Tests	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	For CRefClk: 30.00/33.00	For Common RefClk: Base Spec 4.0, Table 8-18
	All Other	16.0 GT/s	Clean Clock	N/A	N/A (Not Applicable)
			SSC	N/A	N/A (Not Applicable)

Table 590 PCI Express Gen 1.0a References and Specification Notes

PCI Express™ Base Specification Revision 1.0a	
N/A	N/A (Not Applicable)

Table 591 PCI Express Gen 1.1 References and Specification Notes

PCI Express™ Base Specification Revision 1.1	
N/A	N/A (Not Applicable)

Table 592 PCI Express Gen 2.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 2.0	
N/A	N/A (Not Applicable)

Table 593 PCI Express Gen 2.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 594 PCI Express Gen 3.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 595 PCI Express Gen 3.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
N/A	N/A (Not Applicable)

Table 596 PCI Express Gen 3.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 3.0	
Section 4.3.8.2	Common Refclk Rx Architecture
Table 4-34	Parameters for Common Refclk Rx Architecture at 8.0 GT/s
Section 4.3.8.3	Data Clocked Refclk Rx Architecture
Table 4-35	Parameters for Data Clocked Rx Architecture at 8.0 GT/s

Table 597 PCI Express Gen 4.0, 2.5 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 598 PCI Express Gen 4.0, 5.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
N/A	N/A (Not Applicable)

Table 599 PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0	
Section 8.6.3	Data Rate Independent Refclk Parameters
Table 8-18	Data Rate Independent Refclk Parameters

Table 600 PCI Express Gen 4.0, 16.0 GT/s, References and Specification Notes

PCI Express™ Base Specification Revision 4.0
Please refer to Table 599, “PCI Express Gen 4.0, 8.0 GT/s, References and Specification Notes,”.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the signal period is ~ 100 MHz.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures the **Sample Rate** to 20 GSa/s and **Memory Depth** to 10 Mpts using **Acquisition Setup**.
6 Fits and displays all sample data on the screen.
7 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on FUNC3. This is the frequency of the SSC.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

5 Preset Equalization Tests at 8.0 GT/s and 16.0 GT/s for PCI-E 3.0 and PCI-E 4.0

Running Equalization Preset Tests / 428

This chapter provides the methods of implementation (MOIs) for equalization preset tests using a Keysight Q-Series, Z-Series, or UXR-Series (13 GHz – 33 GHz) Infiniium Oscilloscope, 1169A/B probes, and the PCI Express Compliance Test Application. These tests are only applicable to Gen 3.0 and Gen 4.0 at 8.0 GT/s and 16.0 GT/s data rates. **Equalization Preset Tests** are not available if the test point "**Base - RefClk Tests**" is selected in the **Set Up** tab.

Running Equalization Preset Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 23. In the **Select Tests** tab, navigate to "Equalization Preset Tests" heading, and select the required tests to run.

Equalization preset tests will only be available when **Equalization Preset Tests** check box is selected in the **Set Up** tab. These tests are only applicable to Gen 3.0 and Gen 4.0 for 8.0 GT/s and 16.0 GT/s data rates.

NOTE

Preset equalization tests must be run separately (not with other tests) in offline mode through following two distinct ways:

1) Run preset equalization tests only in offline mode - by selecting the **Equalization Preset Tests** check box and selecting the **Use saved waveform** check box .
OR

2) Run normal tests (Base, CEM, or Ref Clock) only in offline mode - by selecting only the **Use saved waveform** check box.

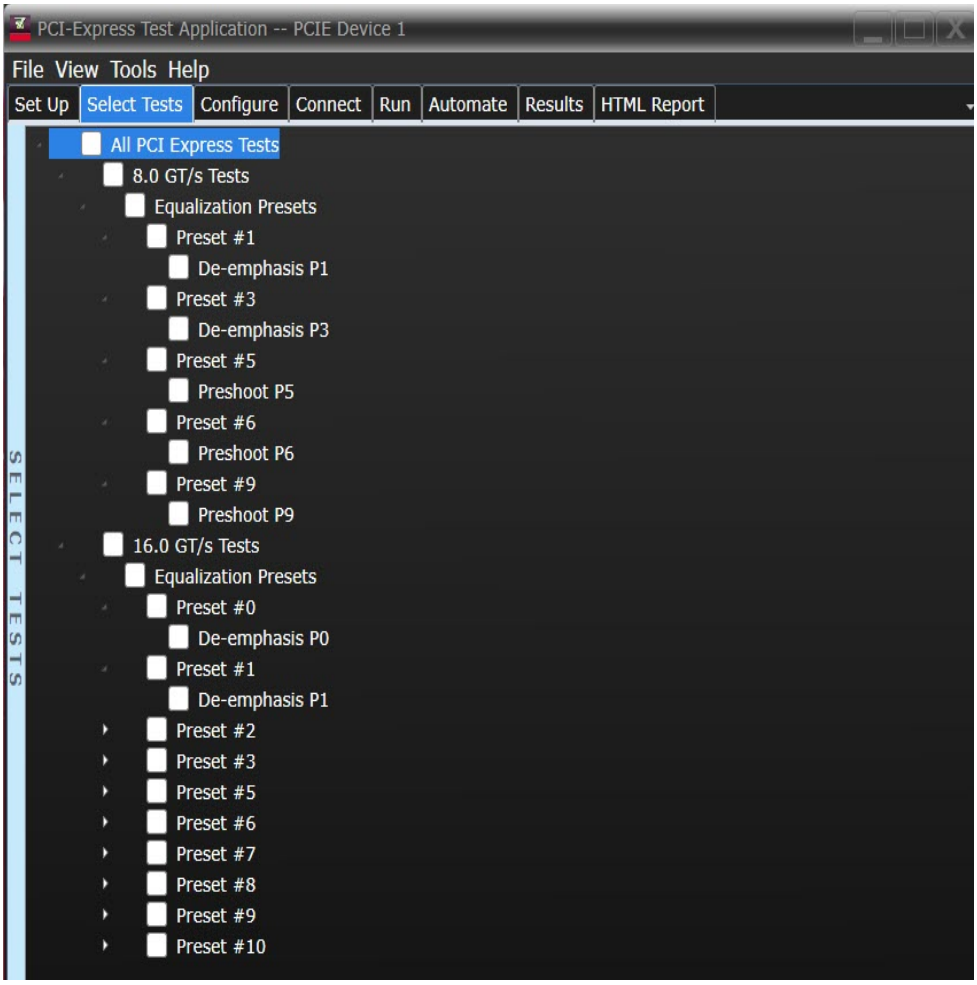


Figure 79 Equalization Presets Tests

Preset #1 Measurement (P1), De-emphasis Test

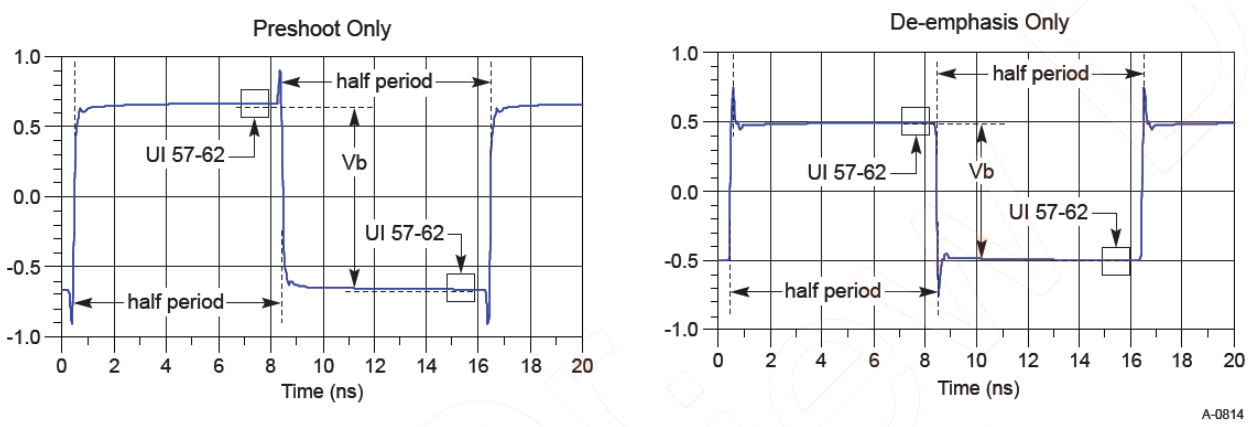
This test verifies that the de-emphasis of the preset number P1 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s /5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 601 **Preset Measurement Cross Reference Table**

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P1	P1/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 602 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P1	0.0	−3.5 ± 1 dB	0.000	−0.167	1.000	0.668	0.668

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
4 Sets the **Horizontal Domain Scale** to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P1.
8 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
9 Sets the **Horizontal Domain Scale** to 20.0µs.
10 Fits and displays all sample data on screen.
11 Saves the P1 signal in *.bin format.
12 Inputs the P4 and P1 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P1.
14 Reports the measurement of Vb during preset values P1 and P4.
15 Compares the de-emphasis value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #0 Measurement (P0), De-emphasis

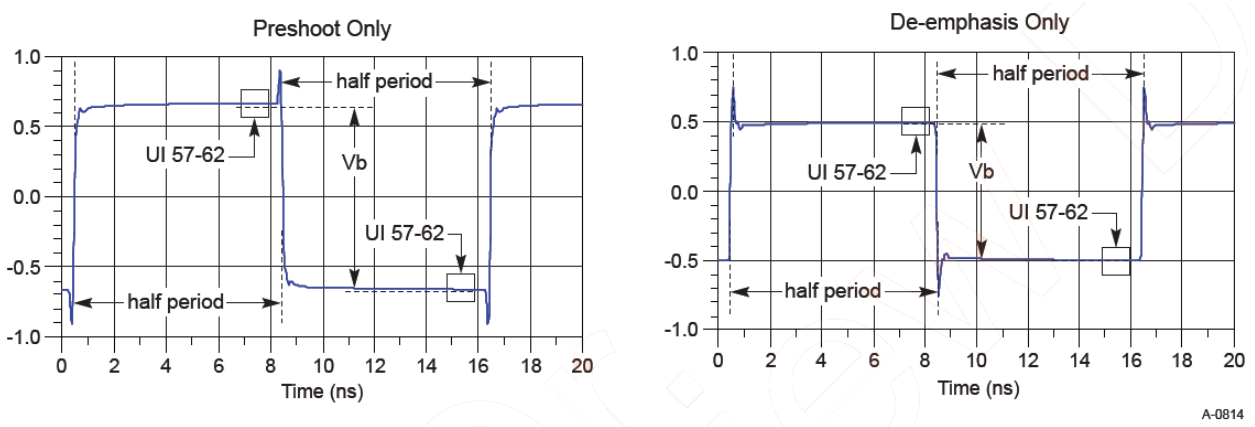
This test verifies that the de-emphasis of the preset number P0 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 603 **Preset Measurement Cross Reference Table**

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P0	P0/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 604 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P0	0.0	−6.0 ± 1.5 dB	0.000	−0.250	1.000	0.500	0.500

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
4 Sets the **Horizontal Domain Scale** to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P0.
8 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
9 Sets the **Horizontal Domain Scale** to 20.0µs.
10 Fits and displays all sample data on screen.
11 Saves the P0 signal in *.bin format.
12 Inputs the P4 and P0 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P0.
14 Reports the measurement of Vb during preset values P0 and P4.
15 Compares the de-emphasis value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #9 Measurement (P9), Preshoot

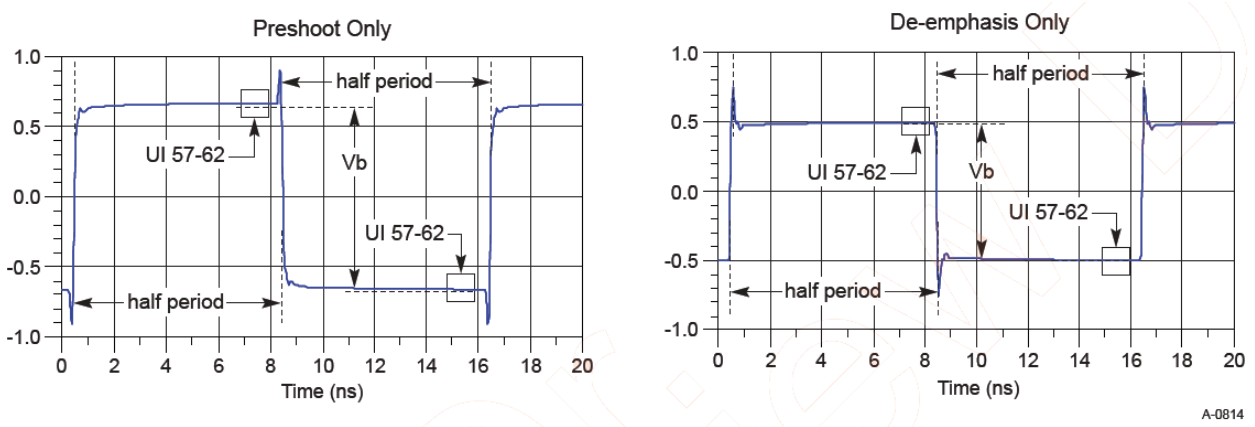
This test verifies that the preshoot of the preset number P9 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0, version 0.71.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 605 **Preset Measurement Cross Reference Table**

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P9	N/A	P4/P9

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 606 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P9	3.5 ± 1 dB	0.0	–0.166	0.000	0.668	0.668	1.000

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
4 Sets the **Horizontal Domain Scale** to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P9.
8 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
9 Sets the **Horizontal Domain Scale** to 20.0µs.
10 Fits and displays all sample data on screen.
11 Saves the P9 signal in *.bin format.
12 Inputs the P4 and P9 saved waveform into SigTest tool.
13 Computes the preshoot at preset value P9.
14 Reports the measurement of Vb during preset values P9 and P4.
15 Compares the preshoot value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #8 Measurement (P8), De-emphasis

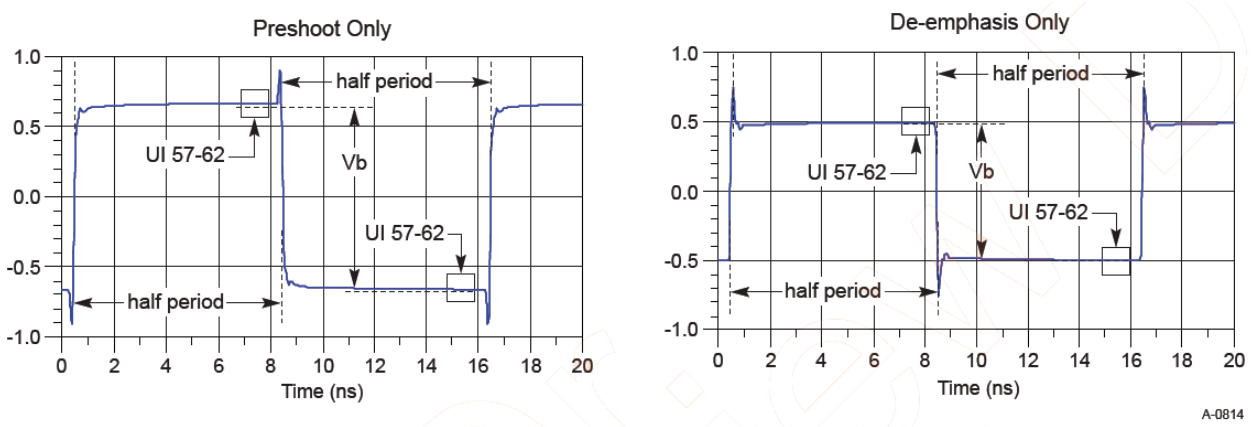
This test verifies that the de-emphasis of the preset number P8 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 607 **Preset Measurement Cross Reference Table**

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P8	P8/P6	P3/P8

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 608 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P8	3.5 ± 1 dB	–3.5 ± 1 dB	–0.125	–0.125	0.750	0.500	0.750

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P6.
3 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
4 Sets the **Horizontal Domain Scale** to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the P6 signal into *.bin format.
7 Configures the DUT to operate in preset value #P8.
8 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
9 Sets the **Horizontal Domain Scale** to 20.0µs.
10 Fits and displays all sample data on screen.
11 Saves the P8 signal in *.bin format.
12 Inputs the P6 and P8 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P8.
14 Reports the measurement of Vb during preset values P6 and P8.
15 Compares the de-emphasis value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #8 Measurement (P8), Preshoot

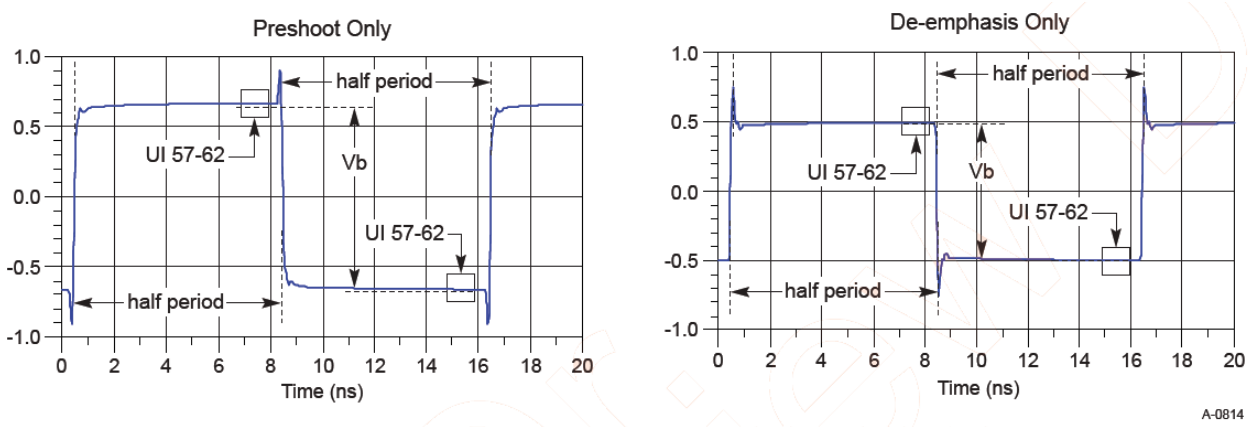
This test verifies that the preshoot of the preset number P8 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 609 **Preset Measurement Cross Reference Table**

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P8	P8/P6	P3/P8

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 610 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P8	3.5 ± 1 dB	–3.5 ± 1 dB	–0.125	–0.125	0.750	0.500	0.750

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P3.
3 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
4 Sets the **Horizontal Domain Scale** to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the P3 signal into *.bin format.
7 Configures the DUT to operate in preset value #P8.
8 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
9 Sets the **Horizontal Domain Scale** to 20.0µs.
10 Fits and displays all sample data on screen.
11 Saves the P8 signal in *.bin format.
12 Inputs the P3 and P8 saved waveform into SigTest tool.
13 Computes the preshoot at preset value P8.
14 Reports the measurement of Vb during preset values P3 and P8.
15 Compares the preshoot value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #7 Measurement (P7), De-emphasis

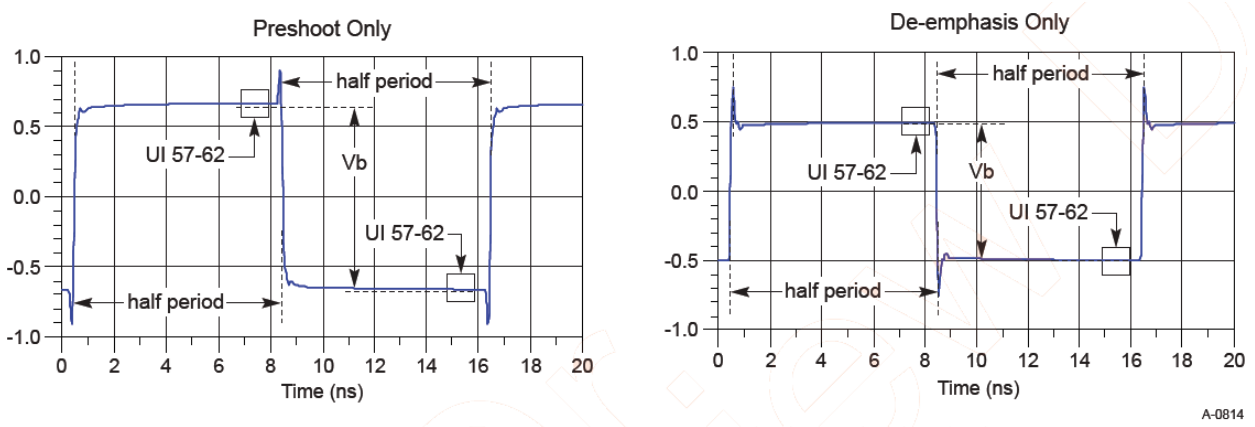
This test verifies that the de-emphasis of the preset number P7 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 611 **Preset Measurement Cross Reference Table**

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P7	P7/P5	P2/P7

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 612 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P5.
3 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
4 Sets the **Horizontal Domain Scale** to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the P5 signal into *.bin format.
7 Configures the DUT to operate in preset value #P7.
8 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
9 Sets the **Horizontal Domain Scale** to 20.0µs.
10 Fits and displays all sample data on screen.
11 Saves the P7 signal in *.bin format.
12 Inputs the P5 and P7 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P7.
14 Reports the measurement of Vb during preset values P5 and P7.
15 Compares the de-emphasis value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #7 Measurement (P7), Preshoot

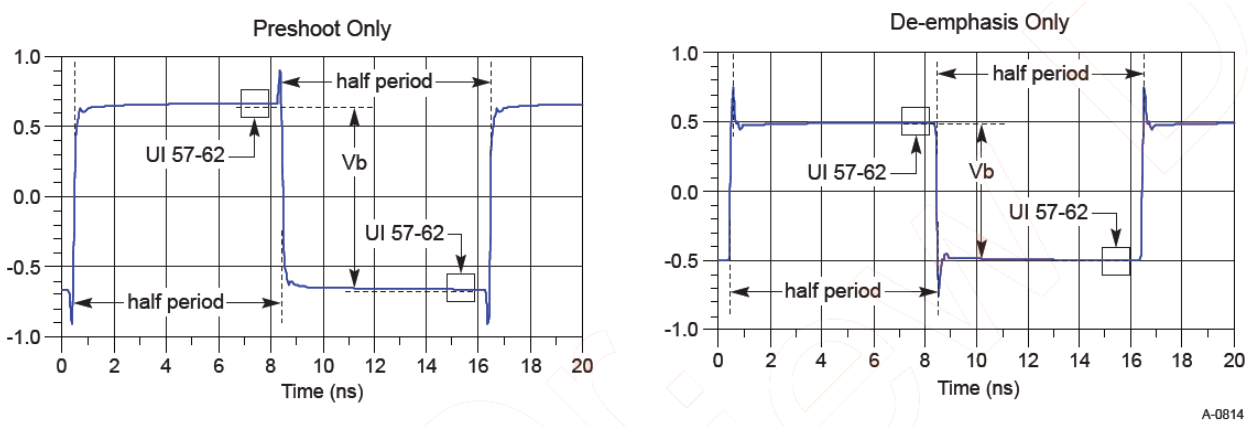
This test verifies that the preshoot of the preset number P7 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0, version 0.71.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 613 **Preset Measurement Cross Reference Table**

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P7	P7/P5	P2/P7

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 614 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P7	3.5 ± 1 dB	–6.0 ± 1.5 dB	–0.100	–0.200	0.800	0.400	0.600

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P2.
3. Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
4. Sets the **Horizontal Domain Scale** to 20.0µs.
5. Fits and displays all sample data on screen.
6. Saves the P2 signal into *.bin format.
7. Configures the DUT to operate in preset value #P7.
8. Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
9. Sets the **Horizontal Domain Scale** to 20.0µs.
10. Fits and displays all sample data on screen.
11. Saves the P7 signal in *.bin format.
12. Inputs the P2 and P7 saved waveform into SigTest tool.
13. Computes the preshoot at preset value P7.
14. Reports the measurement of Vb during preset values P2 and P7.
15. Compares the preshoot value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #5 Measurement (P5), Preshoot

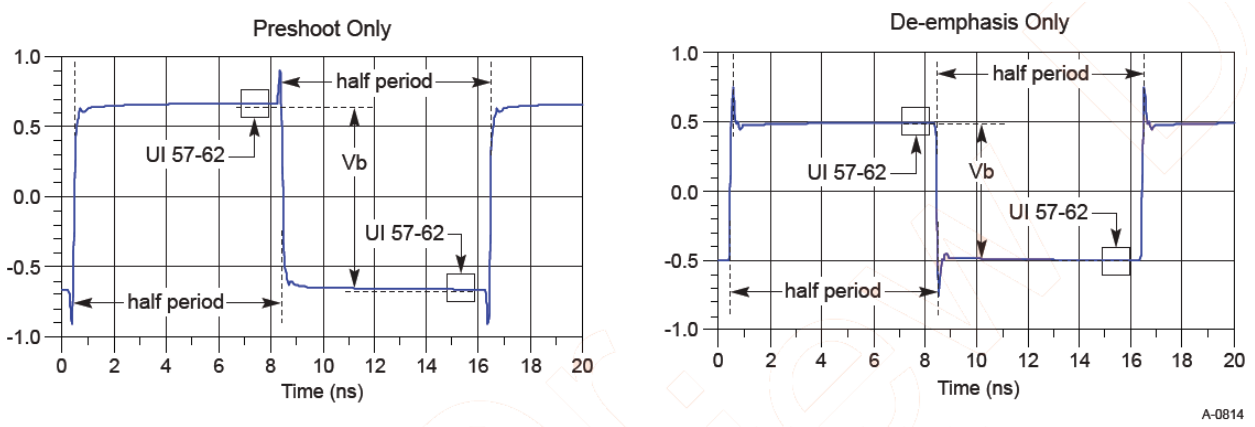
This test verifies that the preshoot of the preset number P5 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0, version 0.71

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 615 **Preset Measurement Cross Reference Table**

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P5	N/A	P4/P5

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 616 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P5	1.9 ± 1 dB	0.0	–0.100	0.000	0.800	0.800	1.000

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
4 Sets the **Horizontal Domain Scale** to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P5.
8 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
9 Sets the **Horizontal Domain Scale** to 20.0µs.
10 Fits and displays all sample data on screen.
11 Saves the P5 signal in *.bin format.
12 Inputs the P4 and P5 saved waveform into SigTest tool.
13 Computes the preshoot at preset value P5.
14 Reports the measurement of Vb during preset values P4 and P5.
15 Compares the preshoot value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #6 Measurement (P6), Preshoot

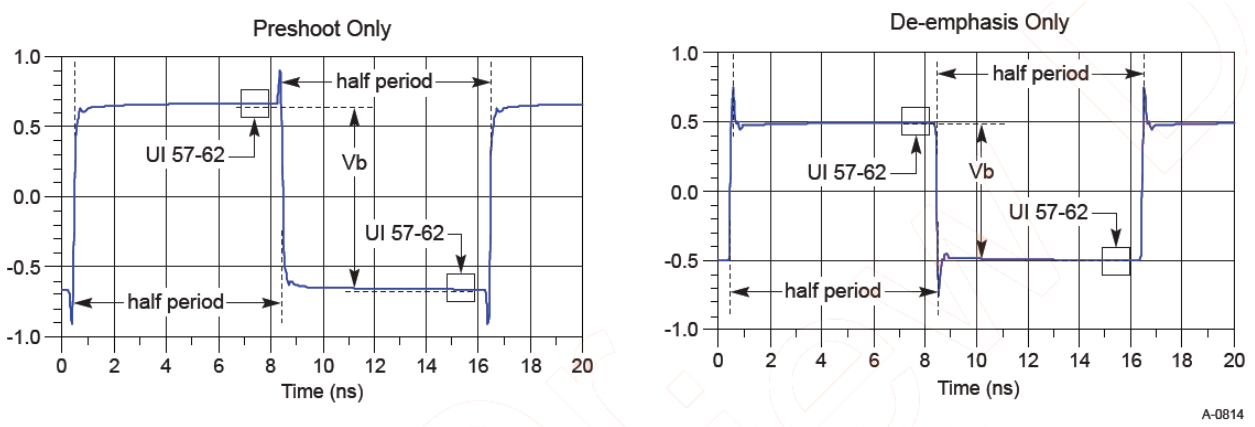
This test verifies that the preshoot of the preset number P6 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 617 **Preset Measurement Cross Reference Table**

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P6	N/A	P4/P6

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 618 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P6	2.5 ± 1 dB	0.0	–0.125	0.000	0.750	0.750	1.000

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
4 Sets the **Horizontal Domain Scale** to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P6.
8 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
9 Sets the **Horizontal Domain Scale** to 20.0µs.
10 Fits and displays all sample data on screen.
11 Saves the P6 signal in *.bin format.
12 Inputs the P4 and P6 saved waveform into SigTest tool.
13 Computes the preshoot at preset value P6.
14 Reports the measurement of Vb during preset values P6 and P4.
15 Compares the preshoot value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #3 Measurement (P3), De-emphasis

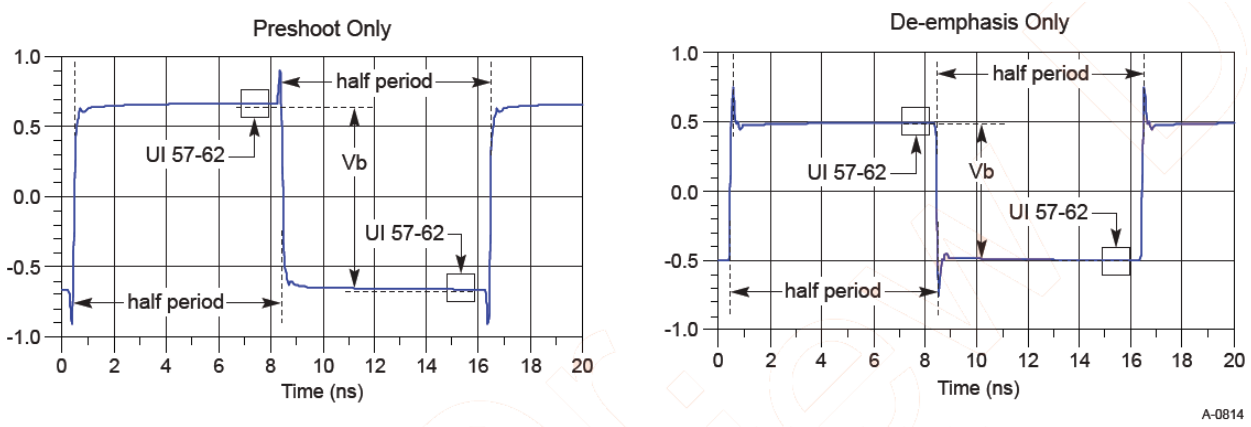
This test verifies that the de-emphasis of the preset number P3 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0, version 0.71.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 619 **Preset Measurement Cross Reference Table**

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P3	P3/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 620 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P3	0.0	−2.5 ± 1 dB	0.000	−0.125	1.000	0.750	0.750

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
4 Sets the **Horizontal Domain Scale** to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P3.
8 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
9 Sets the **Horizontal Domain Scale** to 20.0µs.
10 Fits and displays all sample data on screen.
11 Saves the P3 signal in *.bin format.
12 Inputs the P4 and P3 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P3.
14 Reports the measurement of Vb during preset values P1 and P3.
15 Compares the de-emphasis value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #2 Measurement (P2), De-emphasis

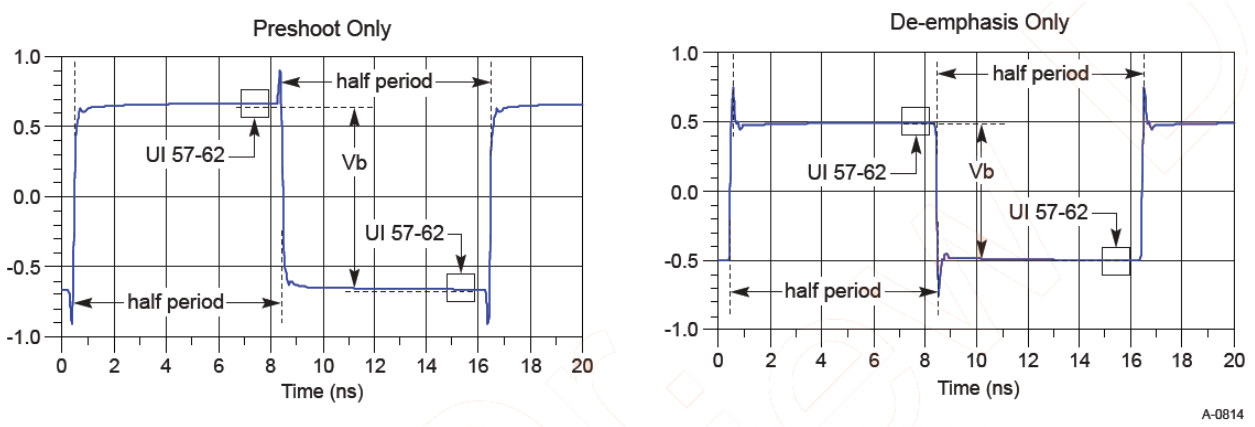
This test verifies that the de-emphasis of the preset number P0 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 621 **Preset Measurement Cross Reference Table**

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P2	P2/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 622 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P2	0.0	−4.4 ± 1.5 dB	0.000	−0.200	1.000	0.600	0.600

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
4 Sets the **Horizontal Domain** Scale to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P2.
8 Configures **Memory Depth** to 8.00000Mpts as **Manual** using **Acquisition Setup**.
9 Sets the **Horizontal Domain Scale** to 20.0µs.
10 Fits and displays all sample data on screen.
11 Saves the P2 signal in *.bin format.
12 Inputs the P4 and P2 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P2.
14 Reports the measurement of Vb during preset values P2 and P4.
15 Compares the de-emphasis value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #10 Measurement (P10), De-emphasis

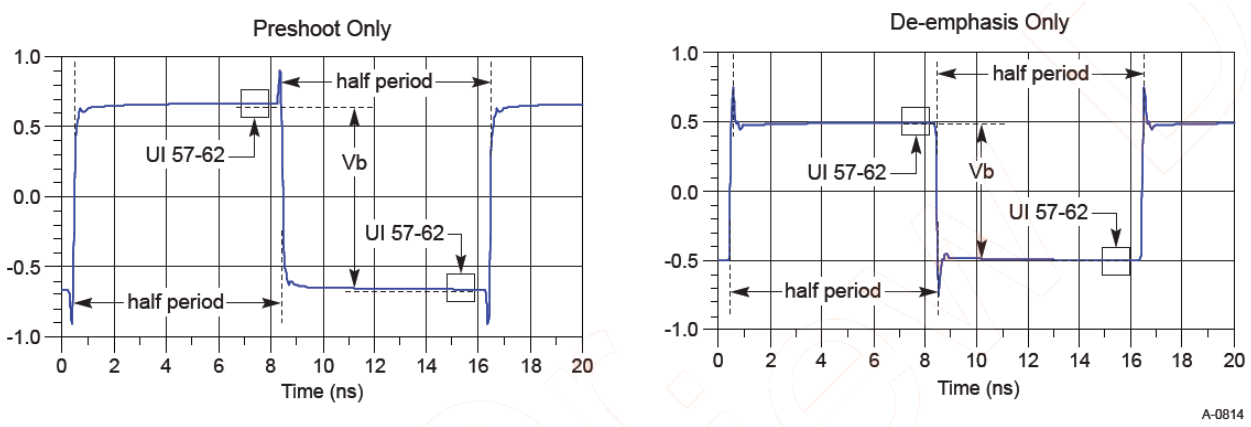
This test verifies that the de-emphasis of the preset number P10 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 623 **Preset Measurement Cross Reference Table**

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P10	P10/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 624 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P10	0.0	See below Note.	0.000	See below Note.	1.000	See below Note.	See below Note.

Test Definition Notes from the Specification

P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. The allowable P10 boost range is defined by the coefficient space lying between the two diagonal lines in Figure 4-50. This approach permits both full and reduced swing transmitters to use P10 for testing to their respective boost limits.

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Table 19 “Compliance Patterns in Various Encodings”.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures **Memory Depth** to 8.00000 Mpts as **Manual** using **Acquisition Setup**.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P10.
8 Configures **Memory Depth** to 8.00000 Mpts as **Manual** using **Acquisition Setup**.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P10 signal in *.bin format.
12 Inputs the P4 and P1 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P10.
14 Reports the measurement of Vb during preset values P10 and P4.
15 Compares the de-emphasis value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

6 Compliance Test List

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Gen 2.0, 2.5 GT/s, Tests / 468
Gen 2.0, 5.0 GT/s, Tests / 474
Gen 3.0, 2.5 GT/s, Tests / 481
Gen 3.0, 5.0 GT/s, Tests / 488
Gen 3.0, 8.0 GT/s, Tests / 498
Gen 4.0, 2.5 GT/s, Tests / 505
Gen 4.0, 5.0 GT/s, Tests / 510
Gen 4.0, 8.0 GT/s, Tests / 517
Gen 4.0, 16.0 GT/s, Tests / 522

This chapter provides a generation-wise organized list of all the compliance tests available in the D9040PCIC PCI Express Compliance Test Application. It links the tests with their respective Methods of Implementation (MOIs) available in the chapter "Compliance Tests" on page 51.

Gen 1.0a, 2.5 GT/s, Tests

Transmitter Tests

This section lists the Transmitter Tests for PCI Express Gen 1.0a at 2.5 GT/s:

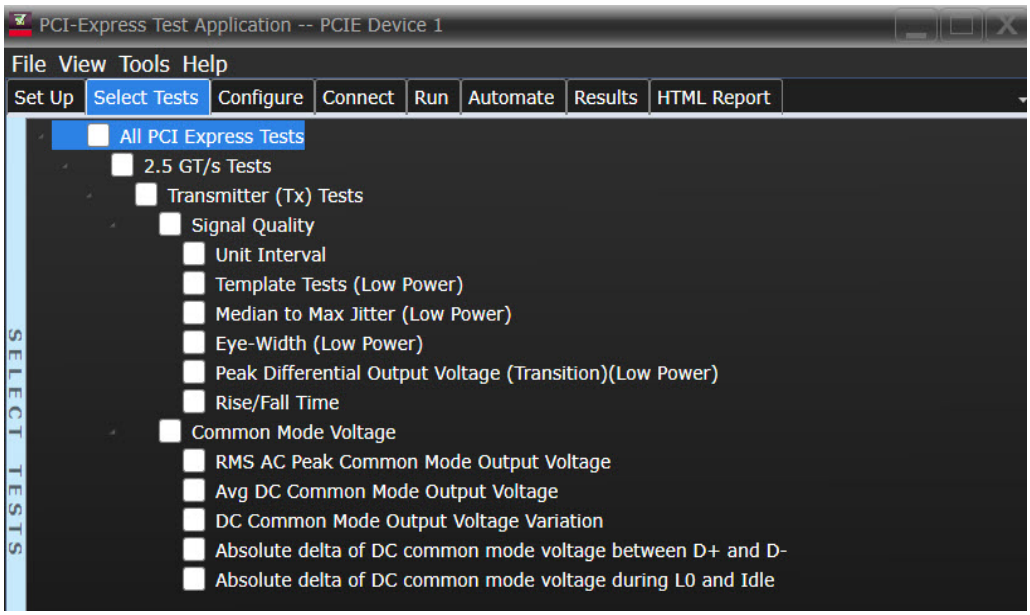


Figure 80 Gen 1.0a, 2.5 GT/s, Transmitter Tests

Transmitter (Tx) Tests - Signal Quality

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test (Low Power) (Full Power); see "Template Test" on page 63
- Median to Max Jitter Test (Low Power) (Full Power); see "Median to Max Jitter Test" on page 77
- Eye-Width (Low Power) (Full Power); see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Low Power) (Full Power); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Rise/Fall Time; see"Rise/Fall Time Test" on page 137
- Deemphasized Voltage Ratio; see"Deemphasized Voltage Ratio Test" on page 143

Transmitter (Tx) Tests - Common Mode Voltage

- RMS AC Peak Common Mode Output Voltage; see "RMS AC Peak Common Mode Output Voltage Test" on page 165
- Avg DC Common Mode Output Voltage; see "Avg DC Common Mode Output Voltage Test" on page 170
- DC Common Mode Output Voltage Variation; see "DC Common Mode Output Voltage Variation Test" on page 175
- Absolute delta of DC common mode voltage between D+ and D-; see "Absolute Delta of DC Common Mode Voltage Between D+ and D- Test" on page 272
- Absolute delta of DC common mode voltage between L0 and Idle; see "Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test" on page 256

Receiver Tests

This section lists the Receiver Tests for PCI Express Gen 1.0a at 2.5 GT/s:

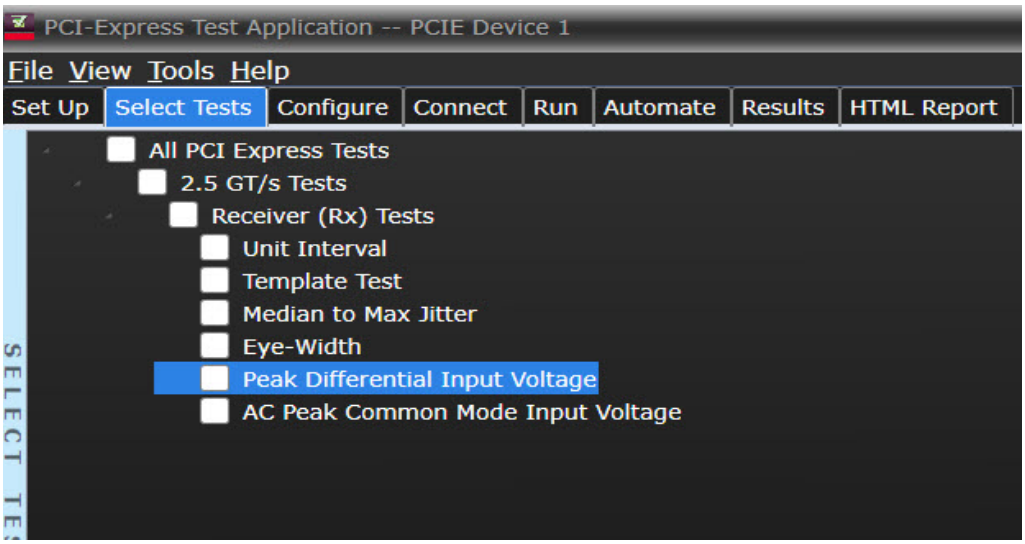


Figure 81 Gen 1.0a, 2.5 GT/s, Receiver Tests

Receiver (Rx) Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Median to Max Jitter; see "Median to Max Jitter Test" on page 77
- Eye-Width; see "Eye-Width Test" on page 85
- Peak Differential Input Voltage; see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- AC Peak Common Mode Input Voltage; see "AC Peak Common Mode Input Voltage Test" on page 161

CEM EndPoint Tests

This section lists the CEM EndPoint Tests for PCI Express Gen 1.0a at 2.5 GT/s:

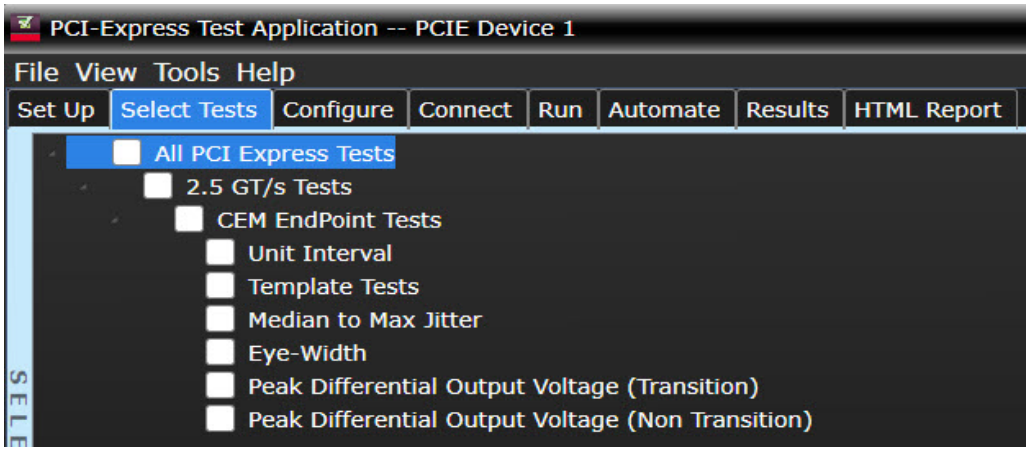


Figure 82 Gen 1.0a, 2.5 GT/s, CEM EndPoint Tests

CEM EndPoint Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Median to Max Jitter; see "Median to Max Jitter Test" on page 77
- Eye-Width; see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

CEM RootComplex Tests

This section lists the CEM RootComplex Tests for PCI Express Gen 1.0a at 2.5 GT/s:

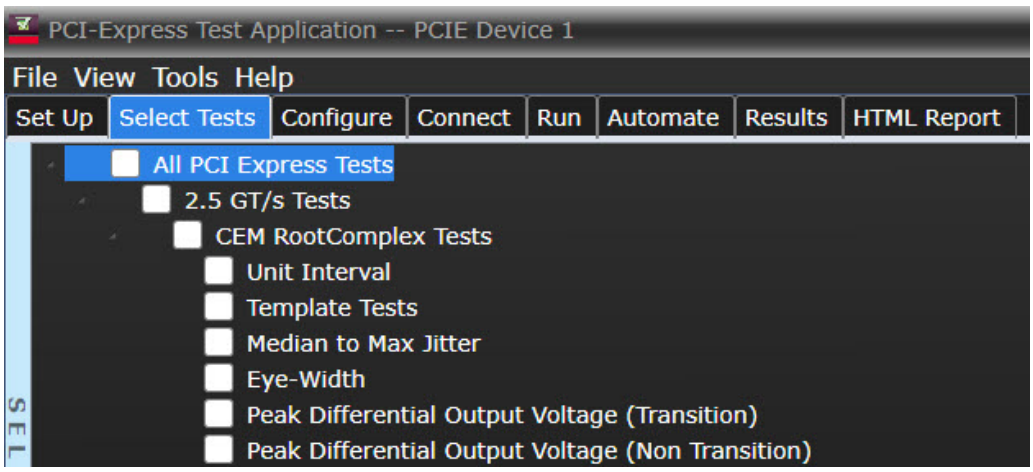


Figure 83 Gen 1.0a, 2.5 GT/s, CEM RootComplex Tests

CEM RootComplex Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Median to Max Jitter; see "Median to Max Jitter Test" on page 77
- Eye-Width; see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

Gen 1.1, 2.5 GT/s, Tests

Transmitter Tests

This section lists the Transmitter Tests for PCI Express Gen 1.1 at 2.5 GT/s:

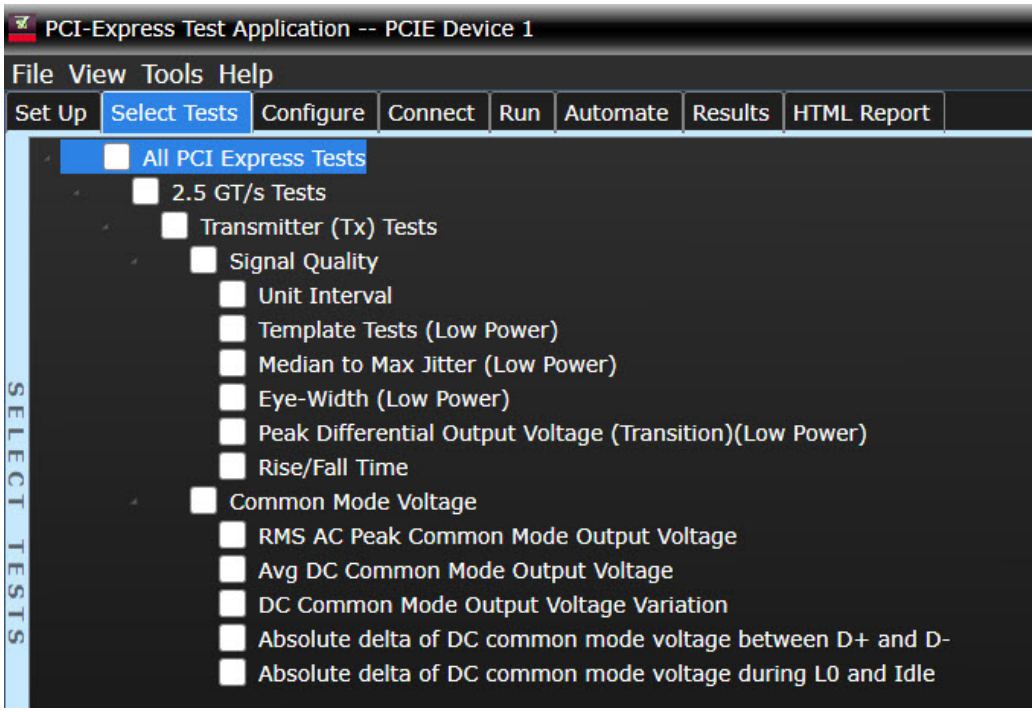


Figure 84 Gen 1.1, 2.5 GT/s, Transmitter Tests

Transmitter (Tx) Tests - Signal Quality

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test (Low Power) (Full Power); see "Template Test" on page 63
- Median to Max Jitter Test (Low Power) (Full Power); see "Median to Max Jitter Test" on page 77
- Eye-Width (Low Power) (Full Power); see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Transition) (Low Power) (Full Power); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Rise/Fall Time; see "Rise/Fall Time Test" on page 137
- Deemphasized Voltage Ratio; see "Deemphasized Voltage Ratio Test" on page 143

Transmitter (Tx) Tests - Common Mode Voltage

- RMS AC Peak Common Mode Output Voltage; see "RMS AC Peak Common Mode Output Voltage Test" on page 165
- Avg DC Common Mode Output Voltage; see "Avg DC Common Mode Output Voltage Test" on page 170
- DC Common Mode Output Voltage Variation; see "DC Common Mode Output Voltage Variation Test" on page 175

- Absolute delta of DC common mode voltage between D+ and D-; see “Absolute Delta of DC Common Mode Voltage Between D+ and D- Test" on page 272
- Absolute delta of DC common mode voltage between L0 and Idle; see “Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test" on page 256

Receiver Tests

This section lists the Receiver Tests for PCI Express Gen 1.1 at 2.5 GT/s:

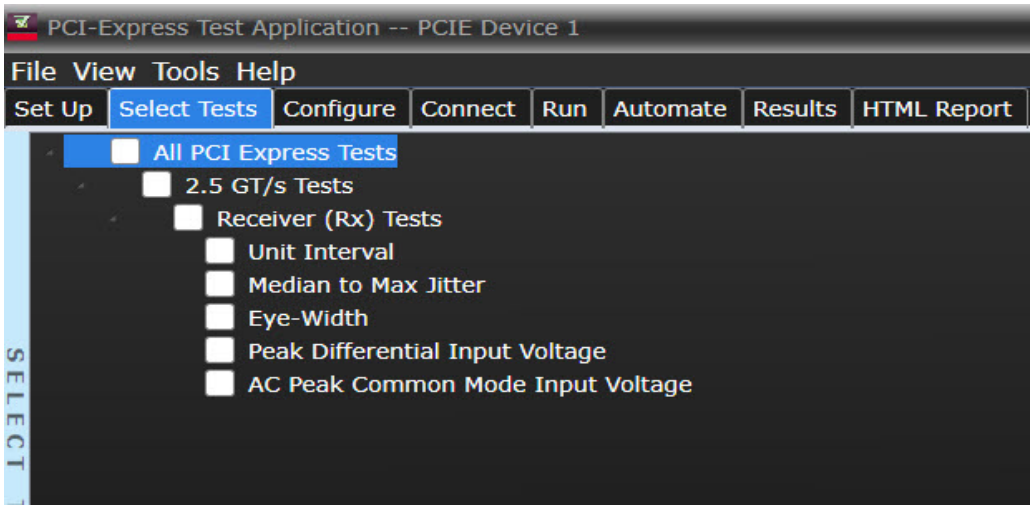


Figure 85 Gen 1.1, 2.5 GT/s, Receiver Tests

Receiver (Rx) Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Median to Max Jitter; see "Median to Max Jitter Test" on page 77
- Eye-Width; see "Eye-Width Test" on page 85
- Peak Differential Input Voltage; see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- AC Peak Common Mode Input Voltage; see "AC Peak Common Mode Input Voltage Test" on page 161

CEM EndPoint Tests

This section lists the CEM EndPoint Tests for PCI Express Gen 1.1 at 2.5 GT/s:

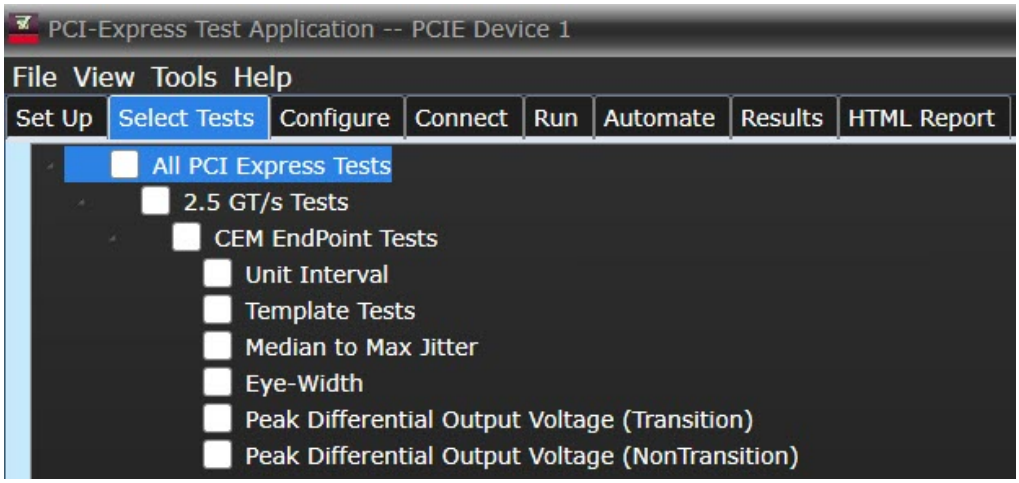


Figure 86 Gen 1.1, 2.5 GT/s, CEM EndPoint Tests

CEM EndPoint Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Median to Max Jitter; see "Median to Max Jitter Test" on page 77
- Eye-Width; see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

CEM RootComplex Tests

This section lists the CEM RootComplex Tests for PCI Express Gen 1.1 at 2.5 GT/s:

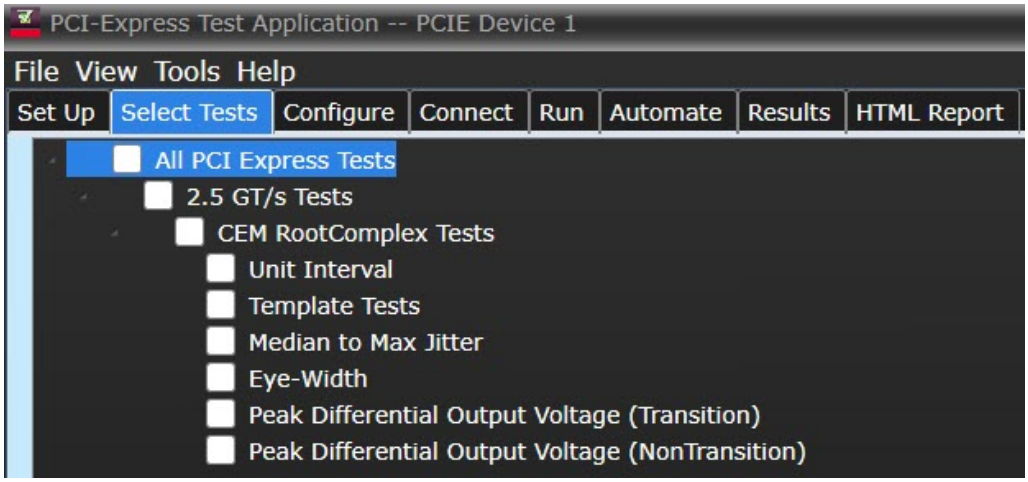


Figure 87 Gen 1.1, 2.5 GT/s, CEM RootComplex Tests

CEM RootComplex Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Median to Max Jitter; see "Median to Max Jitter Test" on page 77
- Eye-Width; see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

Reference Clock Tests

This section lists the Reference Clock Tests for PCI Express Gen 1.1 at 2.5 GT/s:

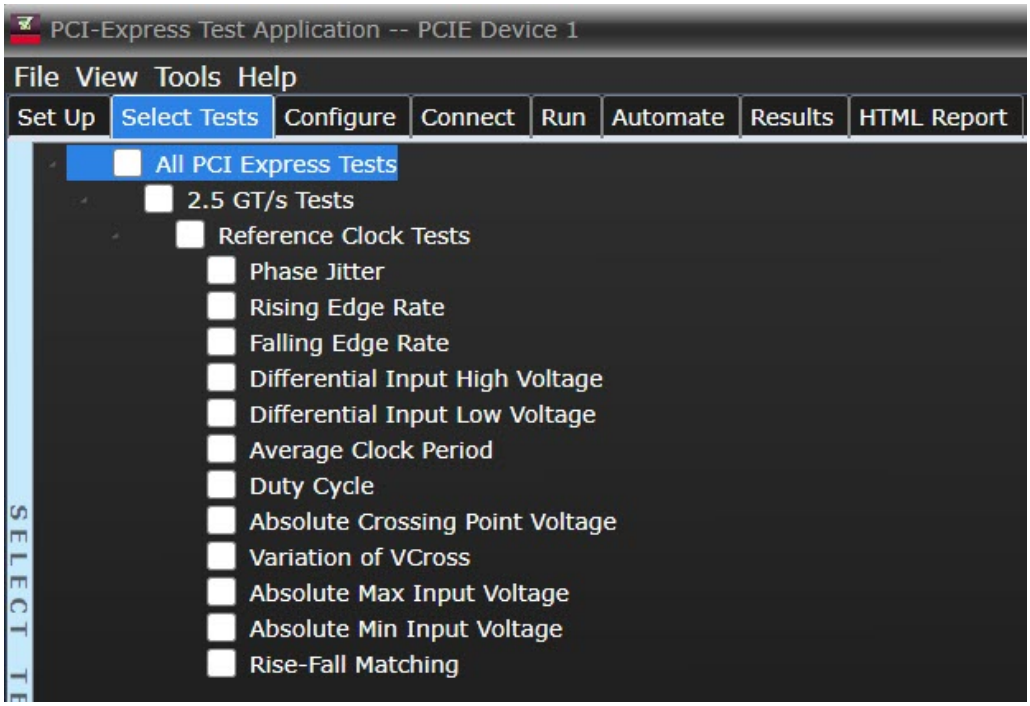


Figure 88 Gen 1.1, 2.5 GT/s, Reference Clock Tests

Reference Clock Tests

- Phase Jitter; see "Phase Jitter Test" on page 177
- Rising Edge Rate; see "Rising Edge Rate Test" on page 184
- Falling Edge Rate; see "Falling Edge Rate Test" on page 189
- Differential Input High Voltage; see "Differential Input High Voltage Test" on page 195
- Differential Input Low Voltage; see "Differential Input Low Voltage Test" on page 200
- Average Clock Period; see "Average Clock Period Test" on page 205
- Duty Cycle; see "Duty Cycle Test" on page 211
- Absolute Crossing Point Voltage; see "Absolute Crossing Point Voltage Test" on page 217
- Variation of VCross; see "Variation of V_{Cross} Test" on page 222
- Absolute Max Input Voltage; see "Absolute Max Input Voltage Test" on page 226
- Absolute Min Input Voltage; see "Absolute Min Input Voltage Test" on page 231
- Rise-Fall Matching; see "Rise-Fall Matching Test" on page 236

Gen 2.0, 2.5 GT/s, Tests

Transmitter Tests

This section lists the Transmitter Tests for PCI Express Gen 2.0 at 2.5 GT/s:

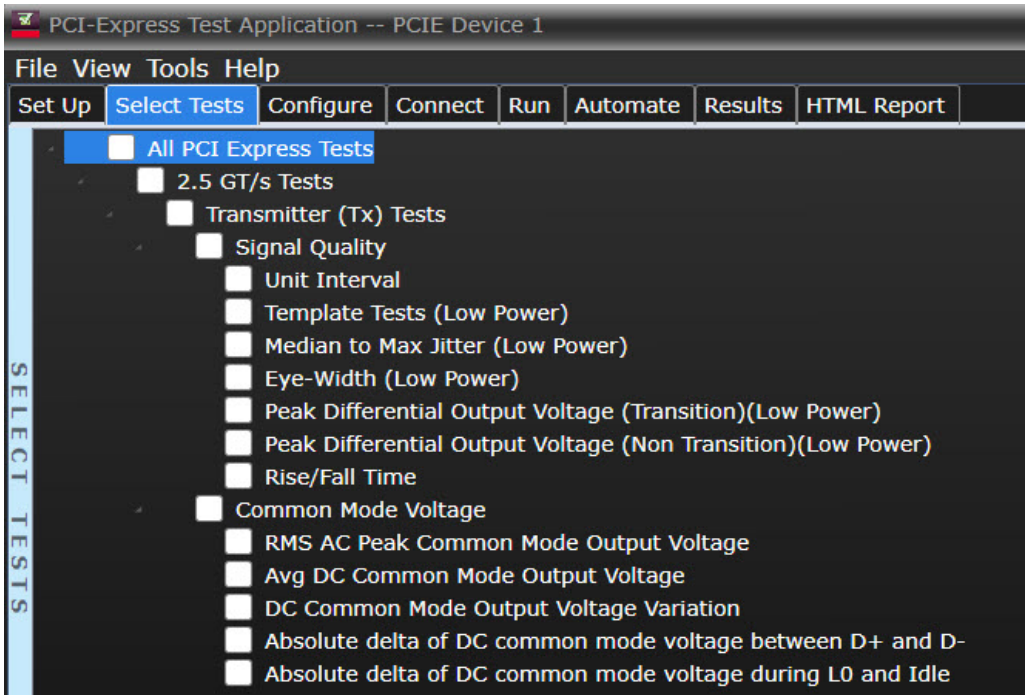


Figure 89 Gen 2.0, 2.5 GT/s, Transmitter Tests

Transmitter (Tx) Tests - Signal Quality

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test (Low Power) (Full Power); see "Template Test" on page 63
- Median to Max Jitter Test (Low Power) (Full Power); see "Median to Max Jitter Test" on page 77
- Eye-Width (Low Power) (Full Power); see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Transition) (Low Power) (Full Power); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition) (Low Power) (Full Power); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Rise/Fall Time; see "Rise/Fall Time Test" on page 137
- Deemphasized Voltage Ratio; see "Deemphasized Voltage Ratio Test" on page 143

Transmitter (Tx) Tests - Common Mode Voltage

- RMS AC Peak Common Mode Output Voltage; see "RMS AC Peak Common Mode Output Voltage Test" on page 165
- Avg DC Common Mode Output Voltage; see "Avg DC Common Mode Output Voltage Test" on page 170
- DC Common Mode Output Voltage Variation; see "DC Common Mode Output Voltage Variation Test" on page 175

- Absolute delta of DC common mode voltage between D+ and D-; see “Absolute Delta of DC Common Mode Voltage Between D+ and D- Test" on page 272
- Absolute delta of DC common mode voltage between L0 and Idle; see “Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test" on page 256

Receiver Tests

This section lists the Receiver Tests for PCI Express Gen 2.0 at 2.5 GT/s:

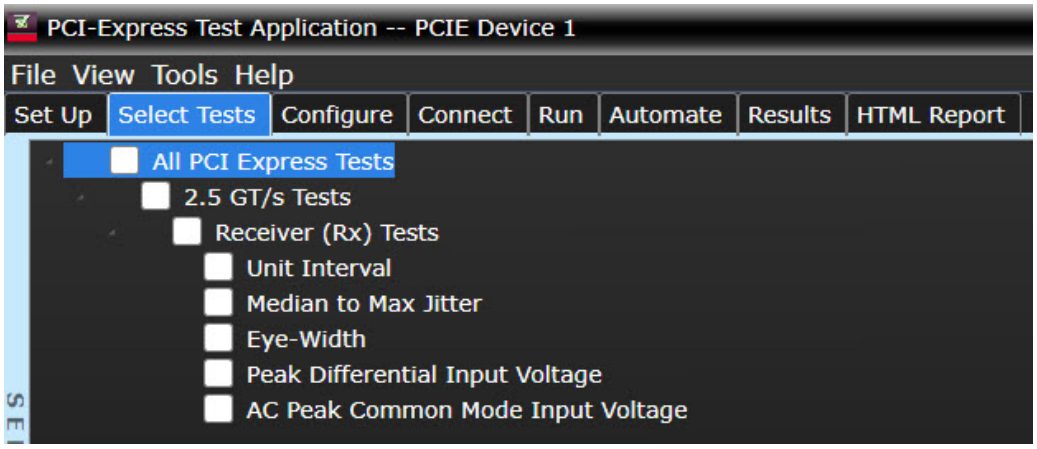


Figure 90 Gen 2.0, 2.5 GT/s, Receiver Tests

Receiver (Rx) Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Median to Max Jitter; see "Median to Max Jitter Test" on page 77
- Eye-Width; see "Eye-Width Test" on page 85
- Peak Differential Input Voltage; see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- AC Peak Common Mode Input Voltage; see "AC Peak Common Mode Input Voltage Test" on page 161

CEM EndPoint Tests

This section lists the CEM EndPoint Tests for PCI Express Gen 2.0 at 2.5 GT/s:

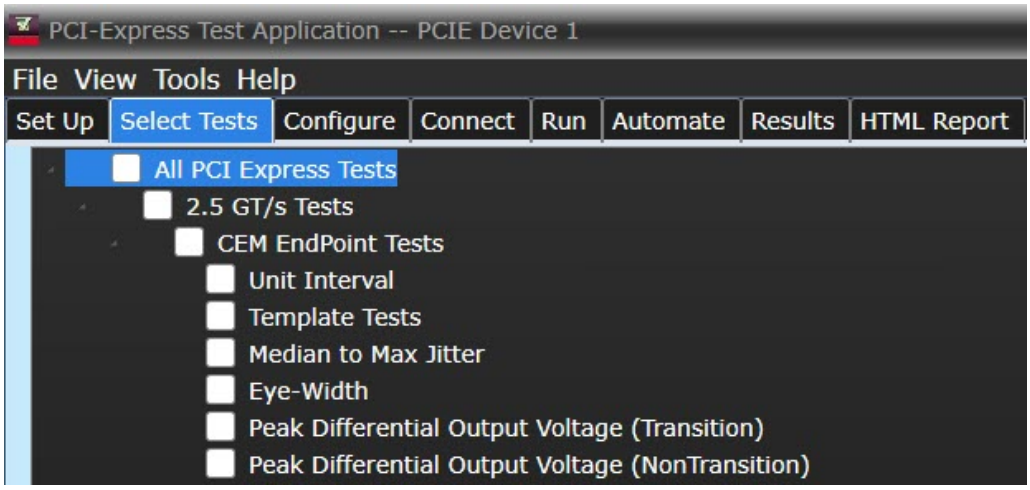


Figure 91 Gen 2.0, 2.5 GT/s, CEM EndPoint Tests

CEM EndPoint Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Median to Max Jitter; see "Median to Max Jitter Test" on page 77
- Eye-Width; see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

CEM RootComplex Tests

This section lists the CEM RootComplex Tests for PCI Express Gen 2.0 at 2.5 GT/s:

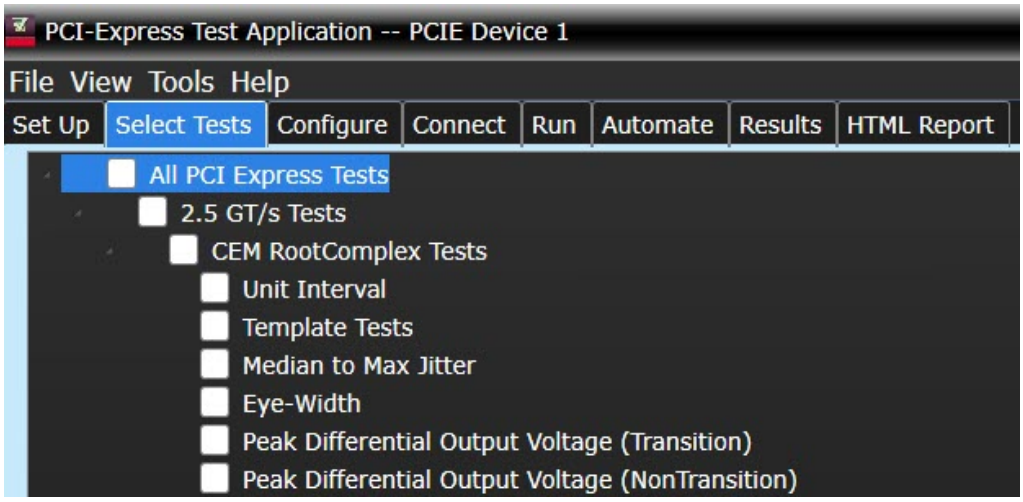


Figure 92 Gen 2.0, 2.5 GT/s, CEM RootComplex Tests

CEM RootComplex Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Median to Max Jitter; see "Median to Max Jitter Test" on page 77
- Eye-Width; see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

Reference Clock Tests

This section lists the Reference Clock Tests for PCI Express Gen 2.0 at 2.5 GT/s:

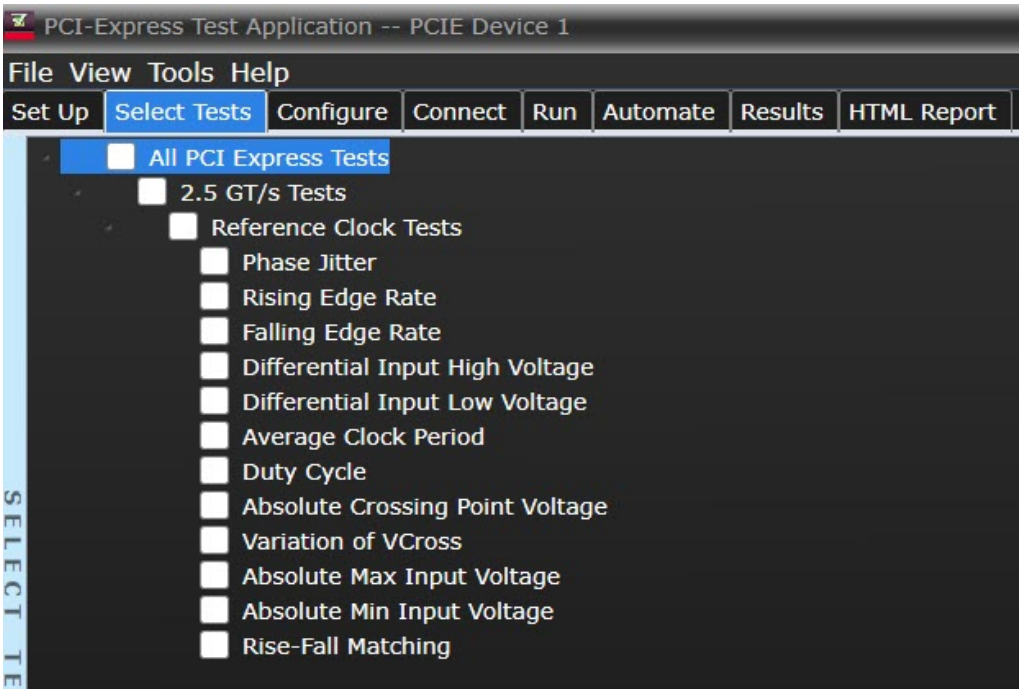


Figure 93 Gen 2.0, 2.5 GT/s, Reference Clock Tests

Reference Clock Tests

- Phase Jitter; see "Phase Jitter Test" on page 177
- Rising Edge Rate; see "Rising Edge Rate Test" on page 184
- Falling Edge Rate; see "Falling Edge Rate Test" on page 189
- Differential Input High Voltage; see "Differential Input High Voltage Test" on page 195
- Differential Input Low Voltage; see "Differential Input Low Voltage Test" on page 200
- Average Clock Period; see "Average Clock Period Test" on page 205
- Duty Cycle; see "Duty Cycle Test" on page 211
- Absolute Crossing Point Voltage; see "Absolute Crossing Point Voltage Test" on page 217
- Variation of VCross; see "Variation of V_{Cross} Test" on page 222
- Absolute Max Input Voltage; see "Absolute Max Input Voltage Test" on page 226
- Absolute Min Input Voltage; see "Absolute Min Input Voltage Test" on page 231
- Rise-Fall Matching; see "Rise-Fall Matching Test" on page 236

Gen 2.0, 5.0 GT/s, Tests

Transmitter Tests

This section lists the Transmitter Tests for PCI Express Gen 2.0 at 5.0 GT/s:

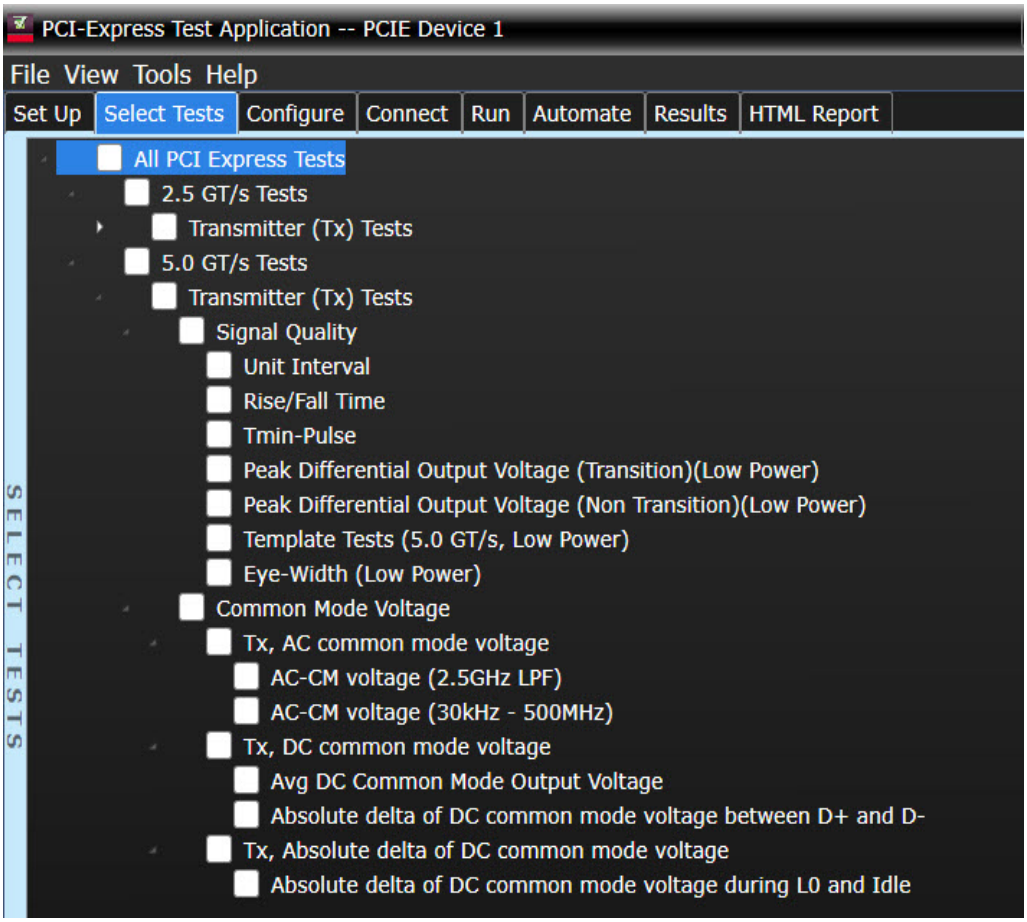


Figure 94 Gen 2.0, 5.0 GT/s, Transmitter Tests

Transmitter (Tx) Tests - Signal Quality

- Unit Interval; see "Unit Interval Test" on page 54
- Rise/Fall Time; see "Rise/Fall Time Test" on page 137
- Tmin-Pulse; see "Tmin-Pulse" on page 150
- Template Test (Low Power) (Full Power); see "Template Test" on page 63
- Eye-Width; see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Transition) (Low Power) (Full Power); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition) (Low Power) (Full Power); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Deemphasized Voltage Ratio; see "Deemphasized Voltage Ratio Test" on page 143

Transmitter (Tx) Tests - Common Mode Voltage

- AC Peak Common Mode Output Voltage (2.5GHz); see "The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal." on page 247
- AC-CM Voltage (30kHz - 500MHz); see "AC Common Mode Voltage (30 kHz to 500 MHz) Test" on page 252
- Avg DC Common Mode Output Voltage; see "Avg DC Common Mode Output Voltage Test" on page 170
- Absolute Delta of DC Common Mode Voltage During L0 and Idle; see "Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test" on page 256
- Absolute Delta of DC Common Mode Voltage During D+ and D-; see "Absolute Delta of DC Common Mode Voltage Between D+ and D- Test" on page 272

Receiver Tests

This section lists the Receiver Tests for PCI Express Gen 2.0 at 5.0 GT/s:

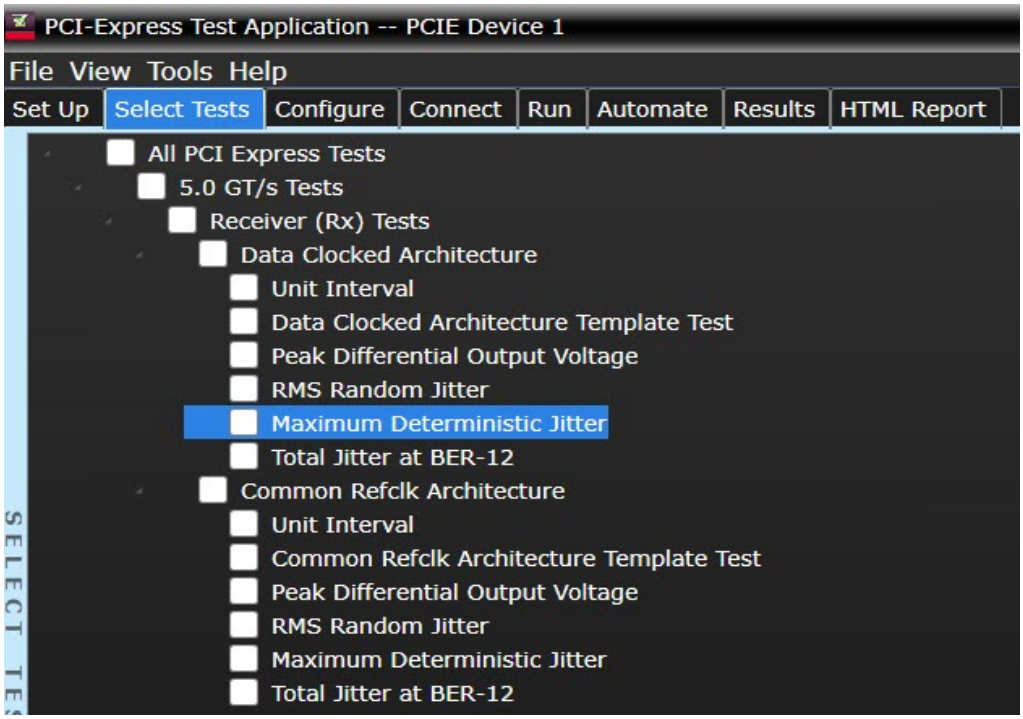


Figure 95 Gen 2.0, 5.0 GT/s, Receiver Tests

Receiver (Rx) Tests - Data Clocked Architecture

- Unit Interval; see "Unit Interval Test" on page 54
- Data Clocked Architecture Template Test; see "Template Test" on page 63
- Peak Differential Output Voltage; see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- RMS Random Jitter; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER-12; see "Total Jitter at BER-12 Test" on page 293

Receiver (Rx) Tests - Common Refclk Architecture

- Unit Interval; see "Unit Interval Test" on page 54
- Common Refclk Architecture Template Test; see "Template Test" on page 63
- Peak Differential Output Voltage; see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- RMS Random Jitter; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER-12; see "Total Jitter at BER-12 Test" on page 293

CEM EndPoint Tests

This section lists the CEM EndPoint Tests for PCI Express Gen 2.0 at 5.0 GT/s:

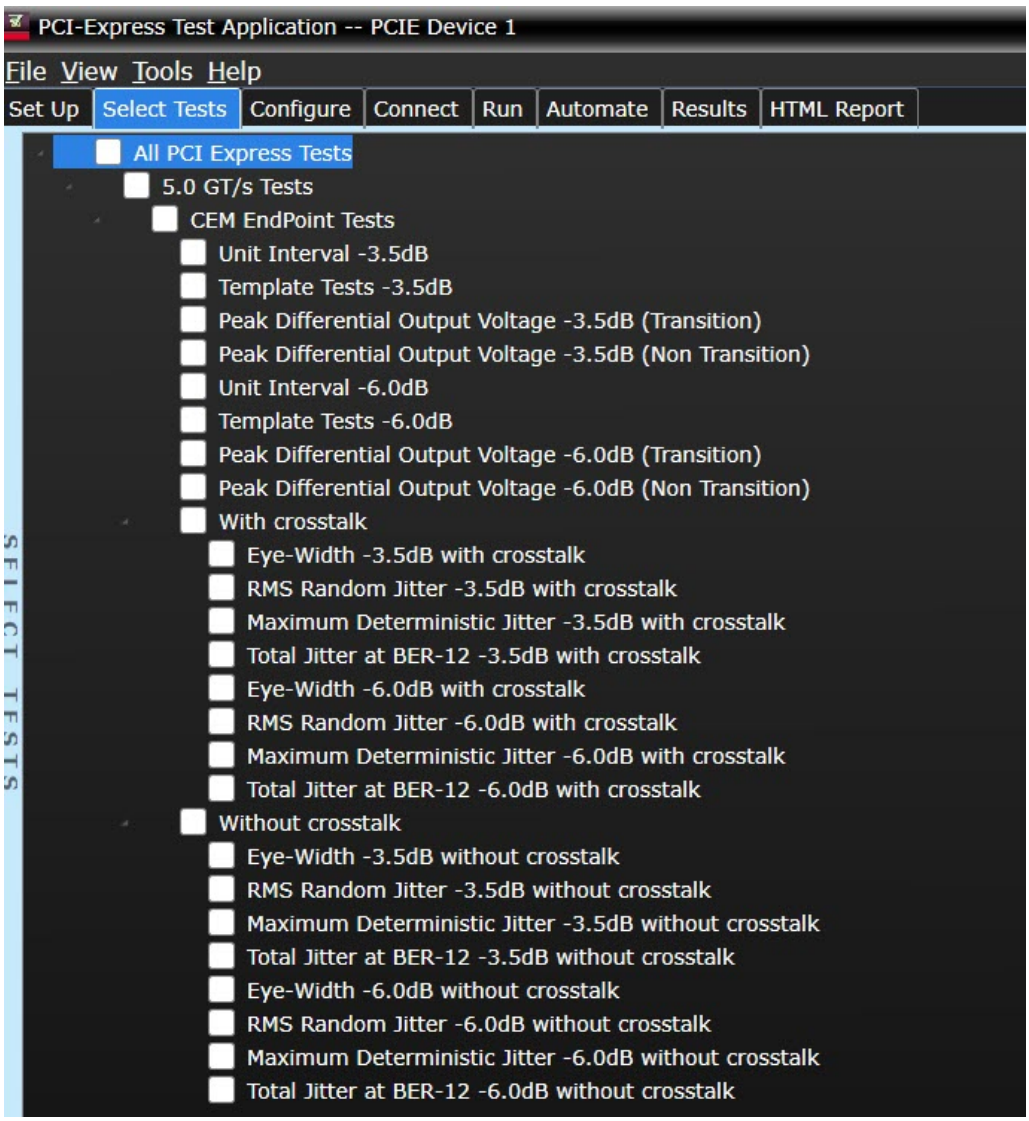


Figure 96 Gen 2.0, 5.0 GT/s, CEM EndPoint Tests

CEMEndPoint Tests

- Unit Interval -3.5 dB; see "Unit Interval Test" on page 54
- Template Test -3.5 dB; see "Template Test" on page 63
- Peak Differential Output Voltage -3.5 dB (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage -3.5 dB (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Unit Interval -6.0 dB; see "Unit Interval Test" on page 54
- Template Test -6.0 dB; see "Template Test" on page 63
- Peak Differential Output Voltage -6.0 dB (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage -6.0 dB (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

CEMEndPoint Tests - With crosstalk

- Eye-Width -3.5dB with crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter -3.5dB with crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter -3.5dB with crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER-12 -3.5dB with crosstalk; see "Total Jitter at BER-12 Test" on page 293
- Eye-Width -6.0dB with crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter -6.0dB with crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter -6.0dB with crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER-12 -6.0dB with crosstalk; see "Total Jitter at BER-12 Test" on page 293

CEMEndPoint Tests - Without crosstalk

- Eye-Width -3.5dB without crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter -3.5dB without crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter -3.5dB without crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER-12 -3.5dB without crosstalk; see "Total Jitter at BER-12 Test" on page 293
- Eye-Width -6.0dB without crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter -6.0dB without crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter -6.0dB without crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER-12 -6.0dB without crosstalk; see "Total Jitter at BER-12 Test" on page 293

CEM RootComplex Tests

This section lists the CEM RootComplex Tests for PCI Express Gen 2.0 at 5.0 GT/s:

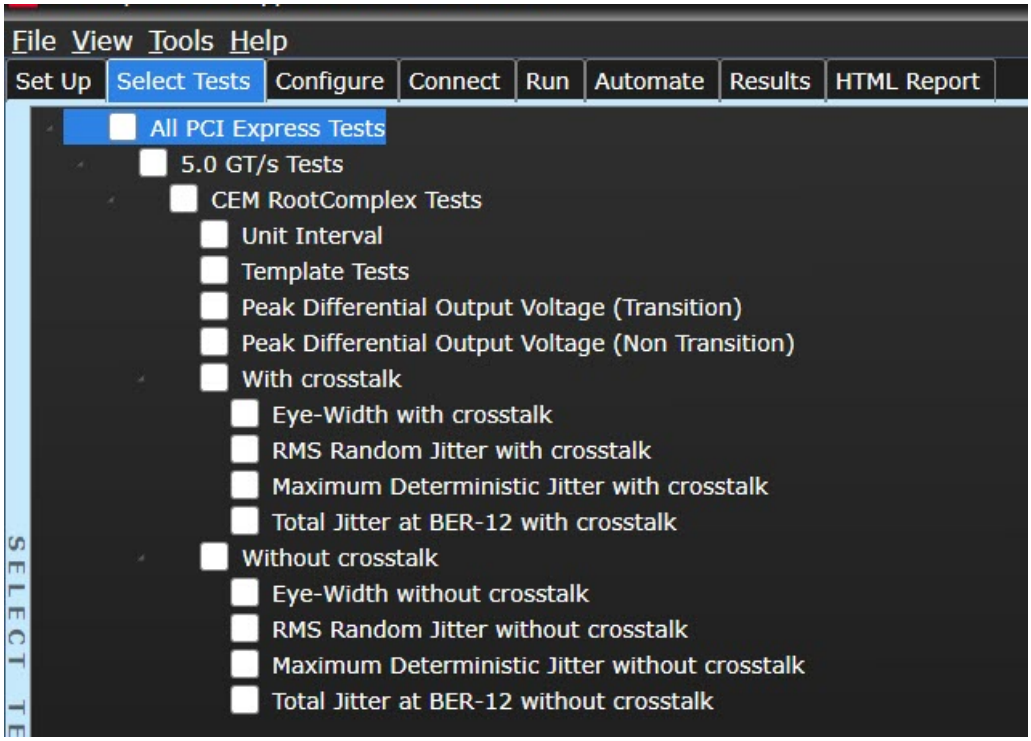


Figure 97 Gen 2.0, 5.0 GT/s, CEM RootComplex Tests

CEM RootComplex Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

CEM RootComplex Tests - With crosstalk

- Eye-Width with crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter with crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter with crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER-12 with crosstalk; see "Total Jitter at BER-12 Test" on page 293

CEM RootComplex Tests - Without crosstalk

- Eye-Width without crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter without crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter without crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER-12 without crosstalk; see "Total Jitter at BER-12 Test" on page 293

Reference Clock Tests

This section lists the Reference Clock Tests for PCI Express Gen 2.0 at 5.0 GT/s:

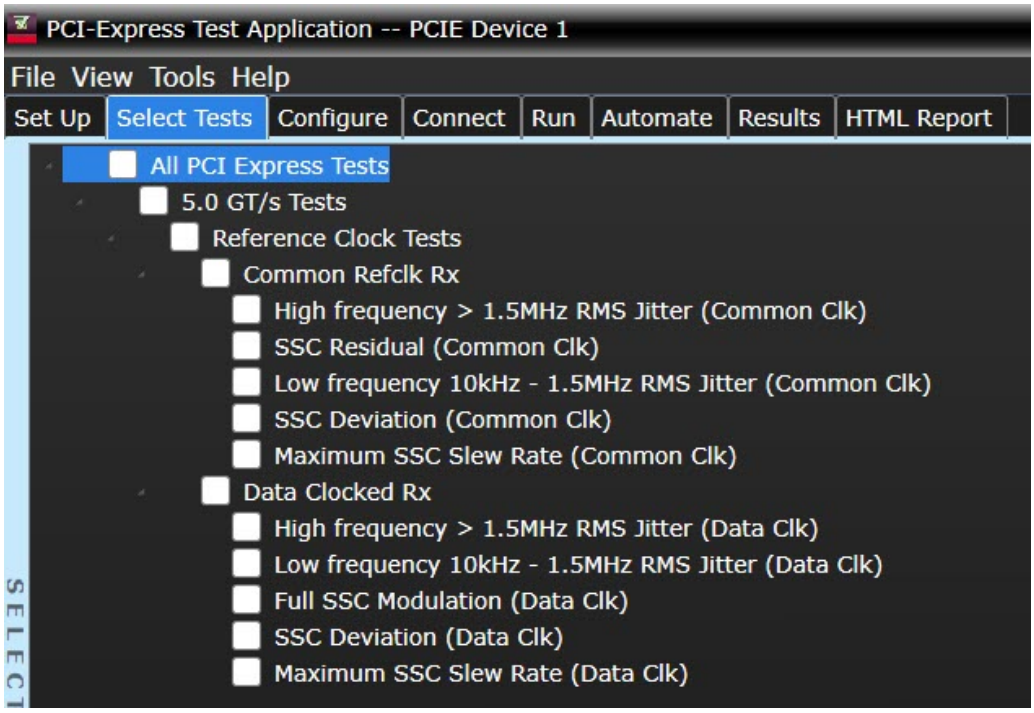


Figure 98 Gen 2.0, 5.0 GT/s, Reference Clock Tests

Reference Clock Tests - Common Refclk Rx

- High frequency > 1.5MHz RMS Jitter (Common Clk); see "High Frequency >1.5 MHz RMS Jitter (Common Clk) (Data Clk) Test" on page 375
- SSC Residual (Common Clk); see "SSC Residual (Common Clk) Test" on page 383
- Low frequency 10kHz - 1.5MHz RMS Jitter (Common Clk); see "Low Frequency 10 kHz to 1.5 MHz RMS Jitter (Common Clk) (Data Clk) Test" on page 387
- SSC Deviation (Common Clk); see "SSC Deviation (Common Clk) (Data Clk) Test" on page 395
- Maximum SSC Slew Rate (Common Clk); see "Maximum SSC Slew Rate (Common Clk) (Data Clk) Test" on page 400

Reference Clock Tests - Data Clocked Rx

- High frequency > 1.5MHz RMS Jitter (Data Clk); see "High Frequency >1.5 MHz RMS Jitter (Common Clk) (Data Clk) Test" on page 375
- Low frequency 10kHz - 1.5MHz RMS Jitter (Data Clk); see "Low Frequency 10 kHz to 1.5 MHz RMS Jitter (Common Clk) (Data Clk) Test" on page 387
- Full SSC Modulation (Data Clk); see "Full SSC Modulation (Data Clk) Test" on page 405
- SSC Deviation (Data Clk); see "SSC Deviation (Common Clk) (Data Clk) Test" on page 395
- Maximum SSC Slew Rate (Data Clk); see "Maximum SSC Slew Rate (Common Clk) (Data Clk) Test" on page 400

Gen 3.0, 2.5 GT/s, Tests

Transmitter Tests

This section lists the Transmitter Tests for PCI Express Gen 3.0 at 2.5 GT/s:

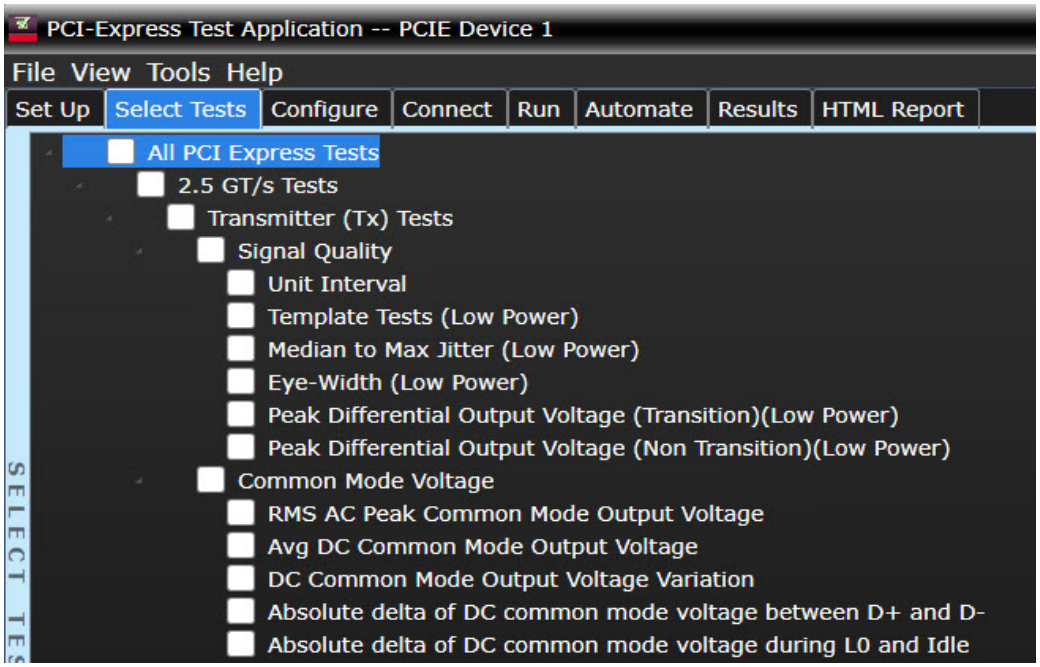


Figure 99 Gen 3.0, 2.5 GT/s, Transmitter Tests

Transmitter (Tx) Tests - Signal Quality

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test (Low Power) (Full Power); see "Template Test" on page 63
- Median to Max Jitter (Low Power) (Full Power); see "Median to Max Jitter Test" on page 77
- Eye-Width (Low Power) (Full Power); see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Transition) (Low Power) (Full Power); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition) (Low Power) (Full Power); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Deemphasized Voltage Ratio; see "Deemphasized Voltage Ratio Test" on page 143

Transmitter (Tx) Tests - Common Mode Voltage

- RMS AC Peak Common Mode Output Voltage; see "RMS AC Peak Common Mode Output Voltage Test" on page 165
- Avg DC Common Mode Output Voltage; see "Avg DC Common Mode Output Voltage Test" on page 170
- DC Common Mode Output Voltage Variation; see "DC Common Mode Output Voltage Variation Test" on page 175
- Absolute Delta of DC Common Mode Voltage between L0 and Idle; see "Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test" on page 256

- Absolute Delta of DC Common Mode Voltage between D+ and D–; see “Absolute Delta of DC Common Mode Voltage Between D+ and D- Test" on page 272

CEM EndPoint Tests

This section lists the CEM EndPoint Tests for PCI Express Gen 3.0 at 2.5 GT/s:

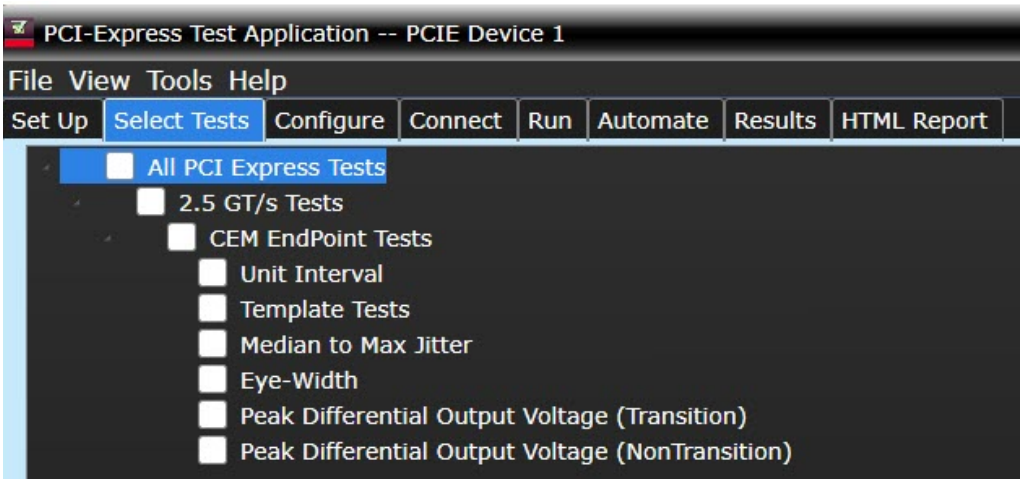


Figure 100 Gen 3.0, 2.5 GT/s, CEM EndPoint Tests

CEM EndPoint Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Median to Max Jitter; see "Median to Max Jitter Test" on page 77
- Eye-Width; see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

CEM RootComplex Tests

This section lists the CEM RootComplex Tests for PCI Express Gen 3.0 at 2.5 GT/s:

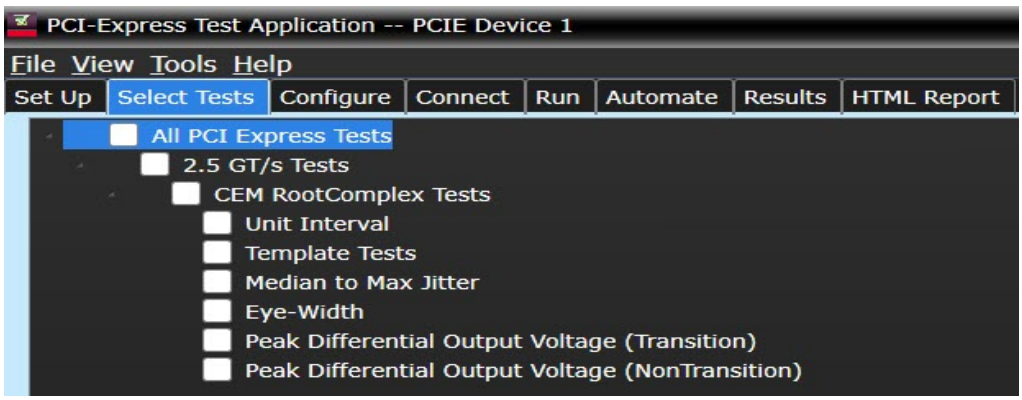


Figure 101 Gen 3.0, 2.5 GT/s, CEM RootComplex Tests

CEM RootComplex Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Median to Max Jitter; see "Median to Max Jitter Test" on page 77
- Eye-Width; see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition; see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

U.2 EndPoint Tests

This section lists the U.2 EndPoint Tests for PCI Express Gen 3.0 at 2.5 GT/s:

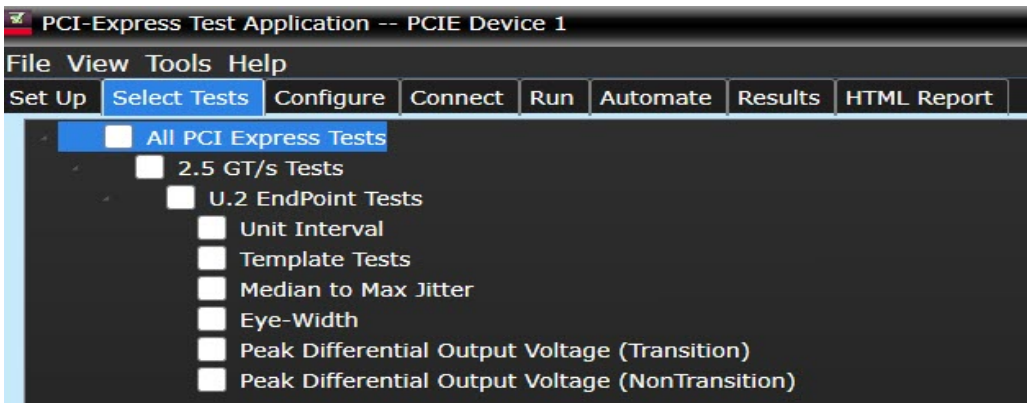


Figure 102 Gen 3.0, 2.5 GT/s, U.2 EndPoint Tests

U.2 EndPoint Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Median to Max Jitter; see "Median to Max Jitter Test" on page 77
- Eye-Width; see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

U.2 RootComplex Tests

This section lists the U.2 RootComplex Tests for PCI Express Gen 3.0 at 2.5 GT/s:

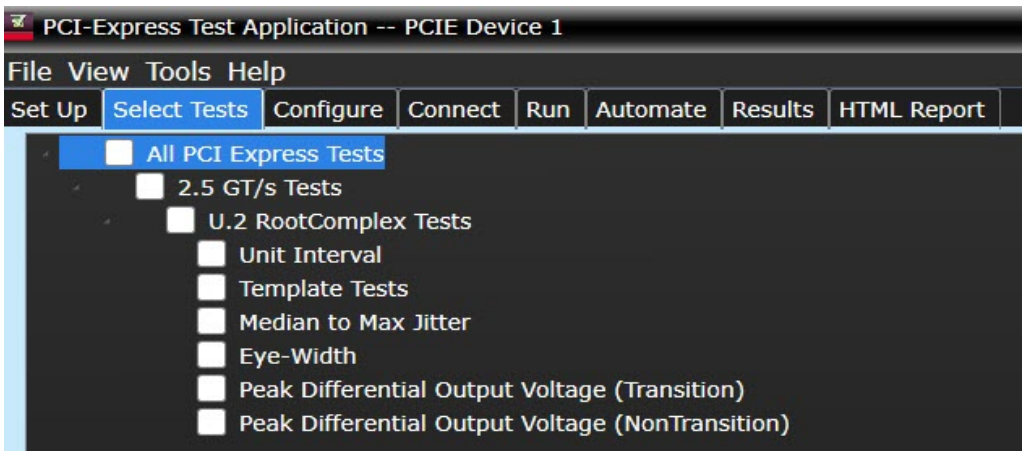


Figure 103 Gen 3.0, 2.5 GT/s, U.2 RootComplex Tests

U.2 RootComplex Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Median to Max Jitter; see "Median to Max Jitter Test" on page 77
- Eye-Width; see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

Reference Clock Tests

This section lists the Reference Clock Tests for PCI Express Gen 3.0 at 2.5 GT/s:

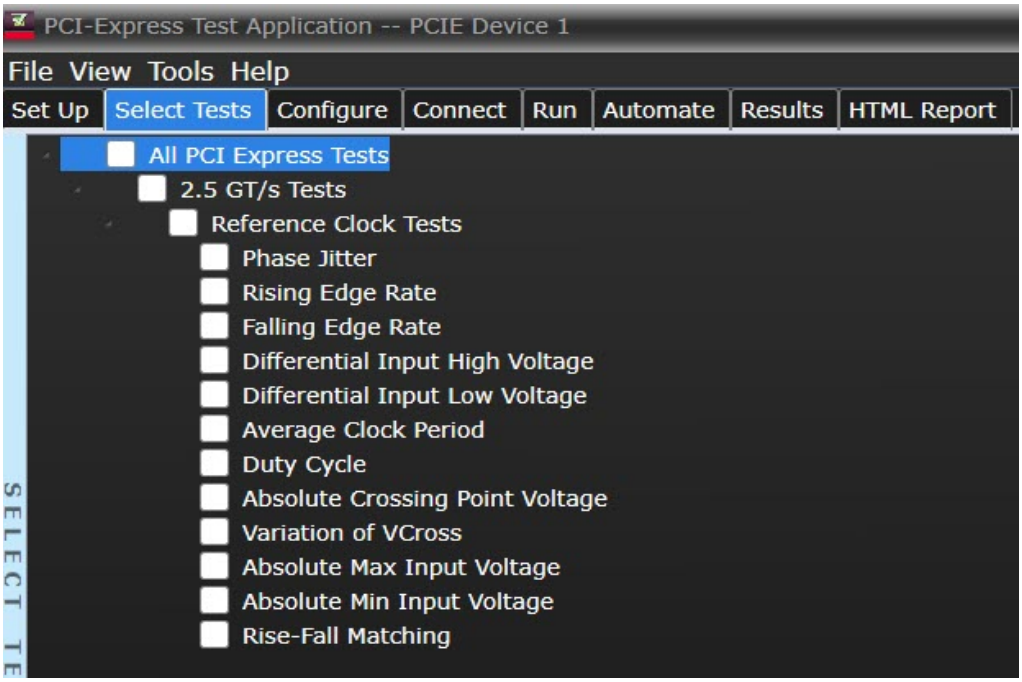


Figure 104 Gen 3.0, 2.5 GT/s, Reference Clock Tests

Reference Clock Tests

- Phase Jitter; see "Phase Jitter Test" on page 177
- Rising Edge Rate; see "Rising Edge Rate Test" on page 184
- Falling Edge Rate; see "Falling Edge Rate Test" on page 189
- Differential Input High Voltage; see "Differential Input High Voltage Test" on page 195
- Differential Input Low Voltage; see "Differential Input Low Voltage Test" on page 200
- Average Clock Period; see "Average Clock Period Test" on page 205
- Duty Cycle; see "Duty Cycle Test" on page 211
- Absolute Crossing Point Voltage; see "Absolute Crossing Point Voltage Test" on page 217
- Variation of VCross; see "Variation of V_{Cross} Test" on page 222
- Absolute Max Input Voltage; see "Absolute Max Input Voltage Test" on page 226
- Absolute Min Input Voltage; see "Absolute Min Input Voltage Test" on page 231
- Rise-Fall Matching; see "Rise-Fall Matching Test" on page 236

Gen 3.0, 5.0 GT/s, Tests

Transmitter Tests

This section lists the Transmitter Tests for PCI Express Gen 3.0 at 5.0 GT/s:

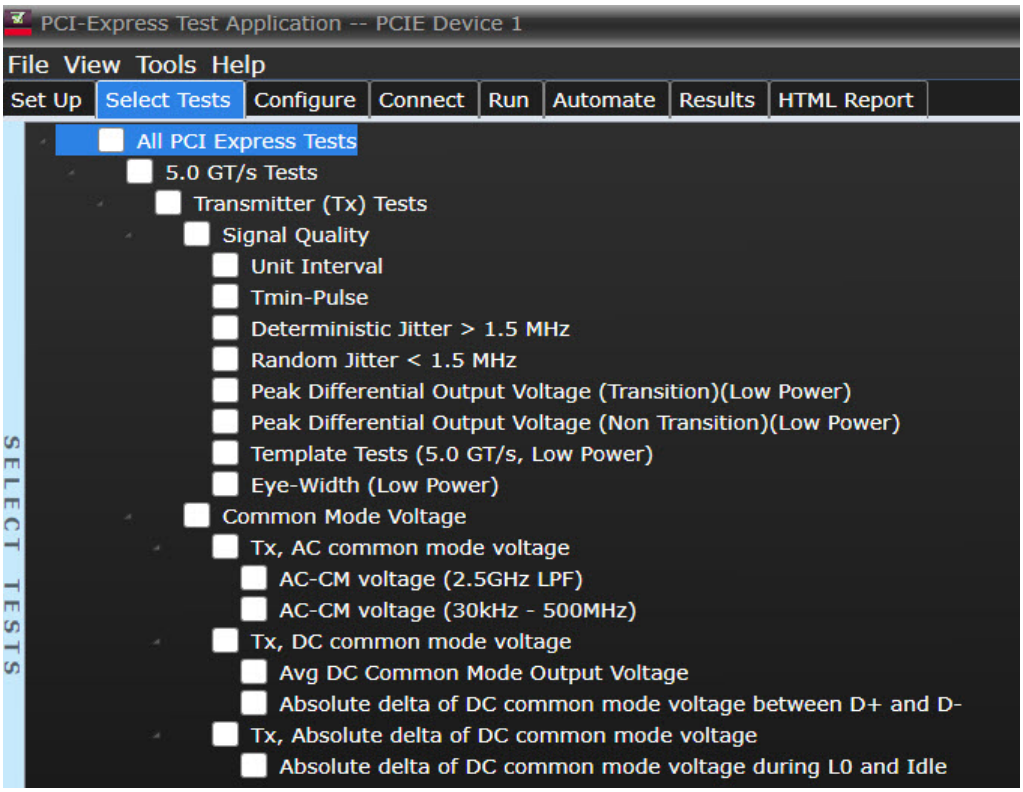


Figure 105 Gen 3.0, 5.0 GT/s, Transmitter Tests

Transmitter (Tx) Tests - Signal Quality

- Unit Interval; see "Unit Interval Test" on page 54
- Tmin-Pulse; see "Tmin-Pulse" on page 150
- Deterministic Jitter > 1.5 MHz; see "Deterministic Jitter Test > 1.5 MHz" on page 155
- Random Jitter < 1.5 MHz; see "Random Jitter Test < 1.5 MHz" on page 158
- Template Tests (Low Power) (Full Power); see "Template Test" on page 63
- Peak Differential Output Voltage (Transition) (Low Power) (Full Power); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition) (Low Power) (Full Power); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Deemphasized Voltage Ratio -3.5dB; see "Deemphasized Voltage Ratio Test" on page 143
- Deemphasized Voltage Ratio -6.0dB; see "Deemphasized Voltage Ratio Test" on page 143

Transmitter (Tx) Tests - Common Mode Voltage

- AC Peak Common Mode Output Voltage (2.5GHz); see "The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal." on page 247
- AC-CM Voltage (30kHz - 500MHz); see "AC Common Mode Voltage (30 kHz to 500 MHz) Test" on page 252
- Avg DC Common Mode Output Voltage; see "Avg DC Common Mode Output Voltage Test" on page 170
- Absolute Delta of DC Common Mode Voltage During D+ and D-; see "Absolute Delta of DC Common Mode Voltage Between D+ and D- Test" on page 272
- Absolute Delta of DC Common Mode Voltage During L0 and Idle; see "Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test" on page 256

CEM EndPoint Tests

This section lists the CEM EndPoint Tests for PCI Express Gen 3.0 at 5.0 GT/s:

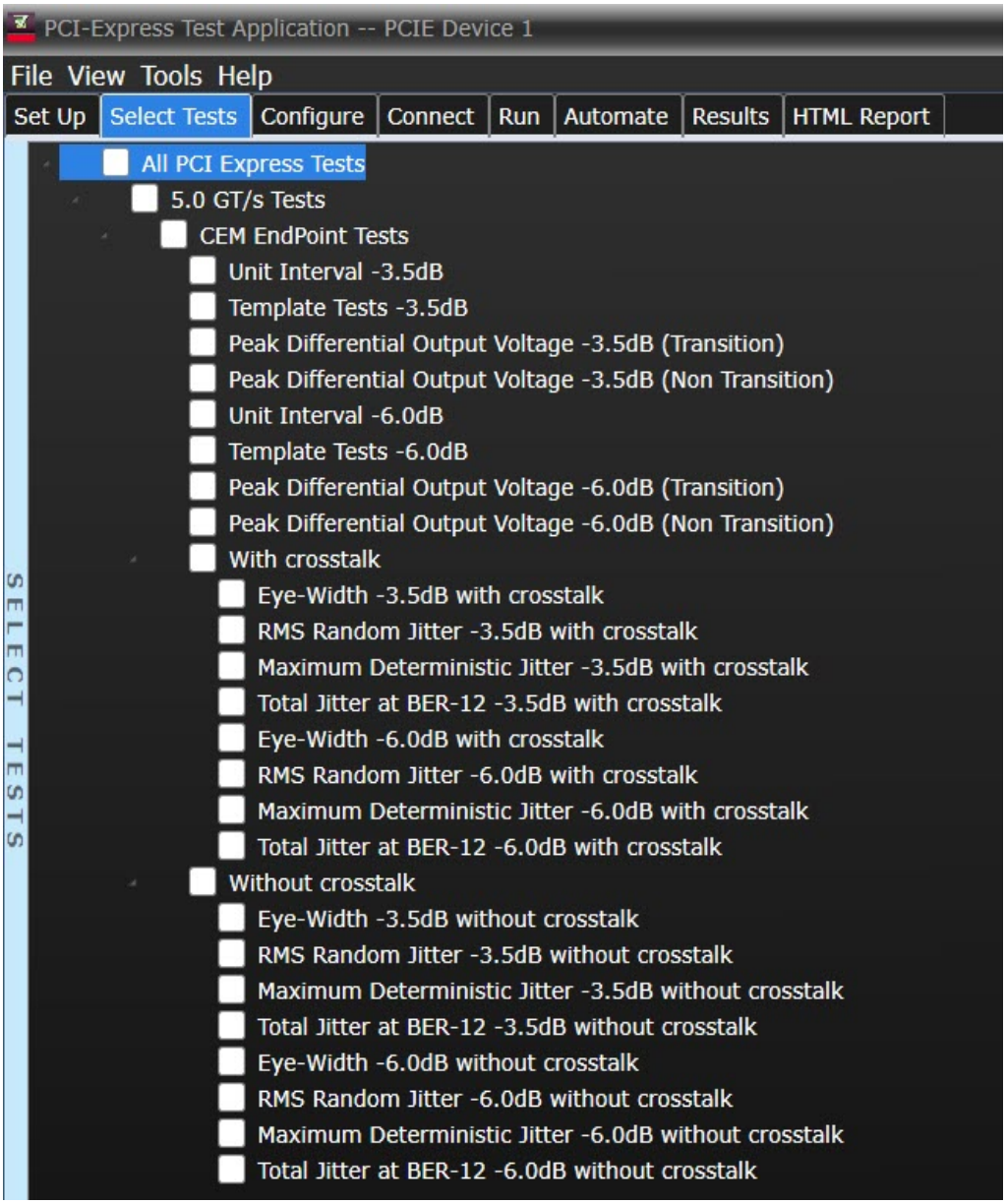


Figure 106 Gen 3.0, 5.0 GT/s, CEM EndPoint Tests

CEM EndPoint Tests

- Unit Interval -3.5dB; see "Unit Interval Test" on page 54
- Template Test -3.5dB; see "Template Test" on page 63
- Peak Differential Output Voltage -3.5dB (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage -3.5dB (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Unit Interval -6.0dB; see "Unit Interval Test" on page 54
- Template Test -6.0dB; see "Template Test" on page 63
- Peak Differential Output Voltage -6.0dB (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage -6.0dB (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

CEM EndPoint Tests - With Crosstalk

- Eye-Width -3.5dB with crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter -3.5dB with crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter -3.5dB with crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 -3.5dB with crosstalk; see "Total Jitter at BER-12 Test" on page 293
- Eye-Width -6.0dB with crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter -6.0dB with crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter -6.0dB with crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 -6.0dB with crosstalk; see "Total Jitter at BER-12 Test" on page 293

CEM EndPoint Tests - Without Crosstalk

- Eye-Width -3.5dB without crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter -3.5dB without crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter -3.5dB without crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 -3.5dB without crosstalk; see "Total Jitter at BER-12 Test" on page 293
- Eye-Width -6.0dB without crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter -6.0dB without crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter -6.0dB without crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 -6.0dB without crosstalk; see "Total Jitter at BER-12 Test" on page 293

CEM RootComplex Tests

This section lists the CEM RootComplex Tests for PCI Express Gen 3.0 at 5.0 GT/s:

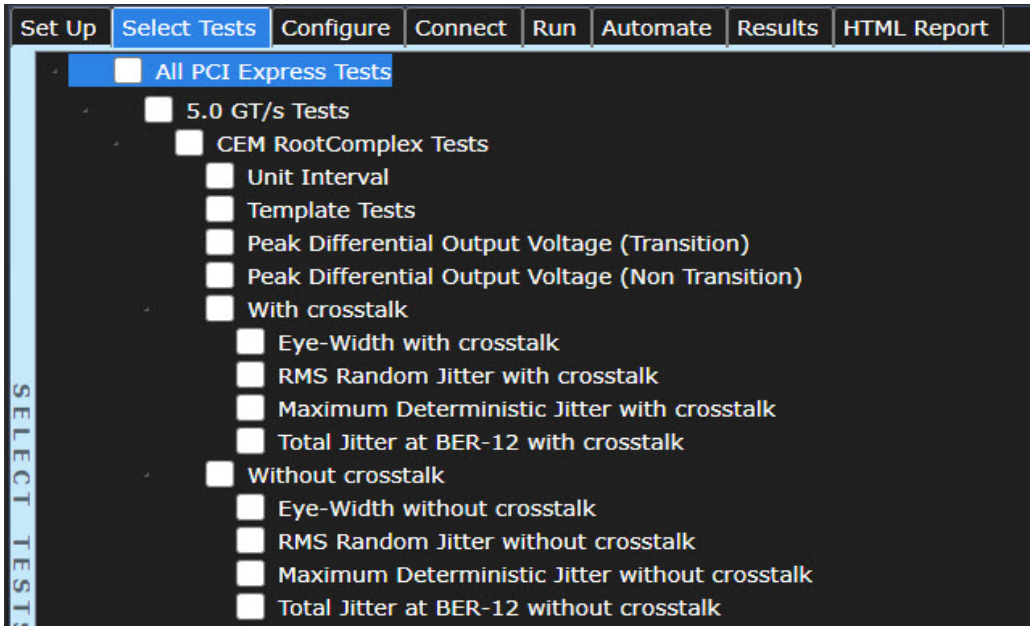


Figure 107 Gen 3.0, 5.0 GT/s, CEM RootComplex Tests

CEM RootComplex Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition; see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

CEM RootComplex Tests - With Crosstalk

- Eye-Width with crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter with crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter with crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 with crosstalk; see "Total Jitter at BER-12 Test" on page 293

CEM RootComplex Tests - Without Crosstalk

- Eye-Width without crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter with crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter without crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 without crosstalk; see "Total Jitter at BER-12 Test" on page 293

U.2 EndPoint Tests

This section lists the U.2 EndPoint Tests for PCI Express Gen 3.0 at 5.0 GT/s:

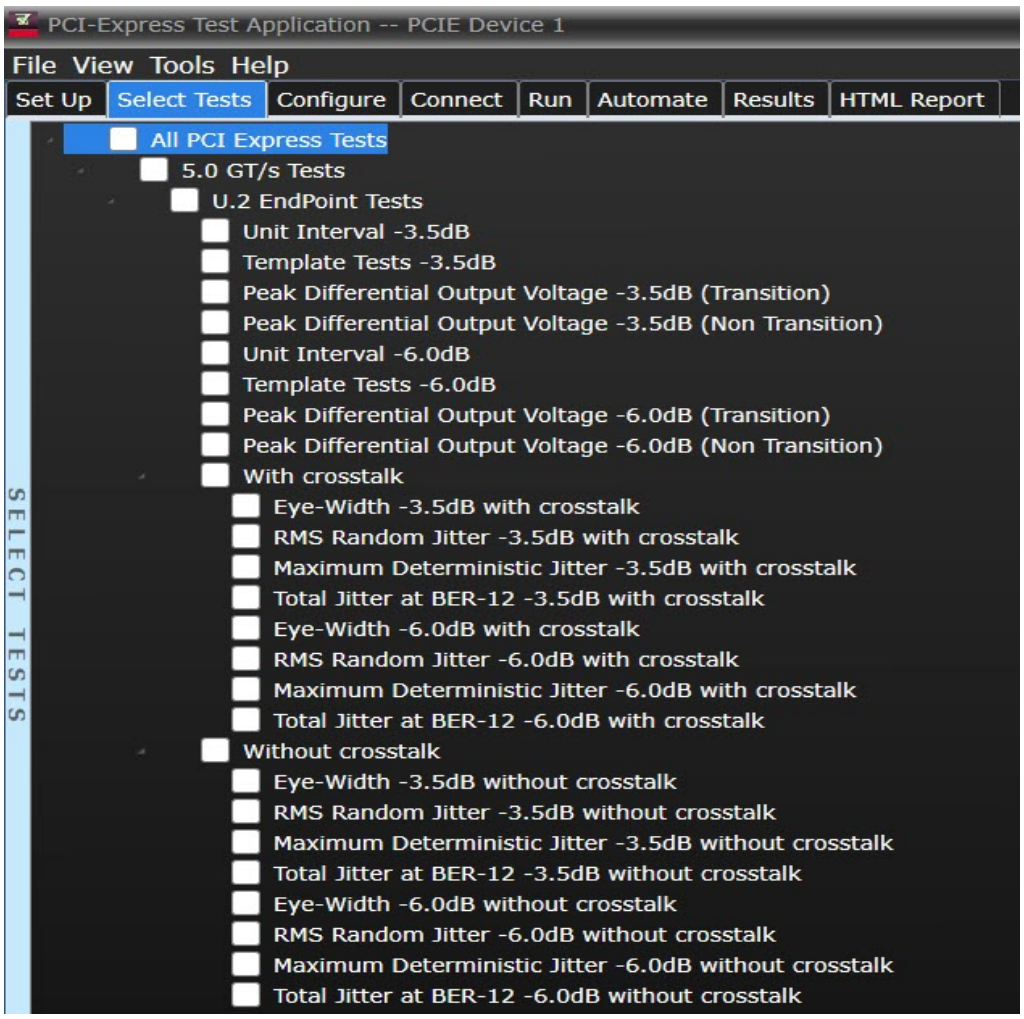


Figure 108 Gen 3.0, 5.0 GT/s, U.2 EndPoint Tests

U.2 EndPoint Tests

- Unit Interval -3.5dB; see "Unit Interval Test" on page 54
- Template Test -3.5dB; see "Template Test" on page 63
- Peak Differential Output Voltage -3.5dB (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage -3.5dB (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Unit Interval -6.0dB; see "Unit Interval Test" on page 54
- Template Test -6.0dB; see "Template Test" on page 63
- Peak Differential Output Voltage -6.0dB (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage -6.0dB (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

U.2 EndPoint Tests - With Crosstalk

- Eye-Width -3.5dB with crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter -3.5dB with crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter -3.5dB with crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 -3.5dB with crosstalk; see "Total Jitter at BER-12 Test" on page 293
- Eye-Width -6.0dB with crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter -6.0dB with crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter -6.0dB with crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 -6.0dB with crosstalk; see "Total Jitter at BER-12 Test" on page 293

U.2 EndPoint Tests - Without Crosstalk

- Eye-Width -3.5dB without crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter -3.5dB without crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter -3.5dB without crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 -3.5dB without crosstalk; see "Total Jitter at BER-12 Test" on page 293
- Eye-Width -6.0dB without crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter -6.0dB without crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter -6.0dB without crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 -6.0dB without crosstalk; see "Total Jitter at BER-12 Test" on page 293

U.2 RootComplex Tests

This section lists the U.2 RootComplex Tests for PCI Express Gen 3.0 at 5.0 GT/s:

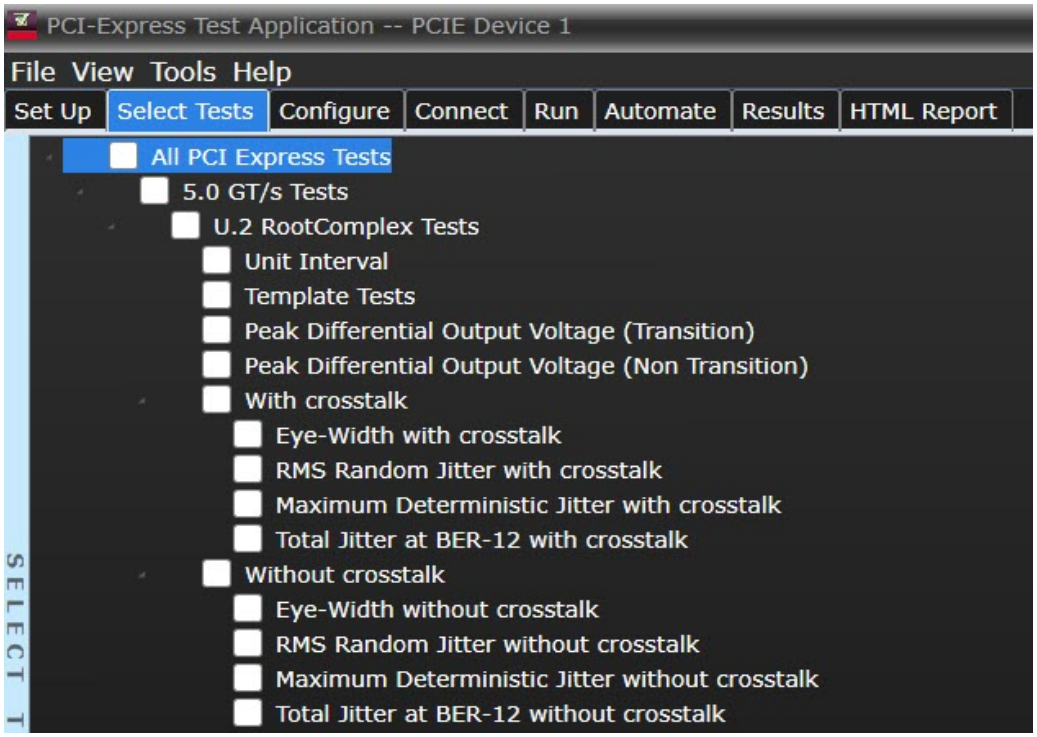


Figure 109 Gen 3.0, 5.0 GT/s, U.2 RootComplex Tests

U.2 RootComplex Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition; see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

U.2 RootComplex Tests - With Crosstalk

- Eye-Width with crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter with crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter with crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 with crosstalk; see "Total Jitter at BER-12 Test" on page 293

U.2 RootComplex Tests - Without Crosstalk

- Eye-Width without crosstalk; see “Eye-Width Test" on page 85
- RMS Random Jitter without crosstalk; see “RMS Random Jitter" on page 276
- Maximum Deterministic Jitter without crosstalk; see “Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 without crosstalk; see “Total Jitter at BER-12 Test" on page 293

Reference Clock Tests

This section lists the Reference Clock Tests for PCI Express Gen 3.0 at 5.0 GT/s:

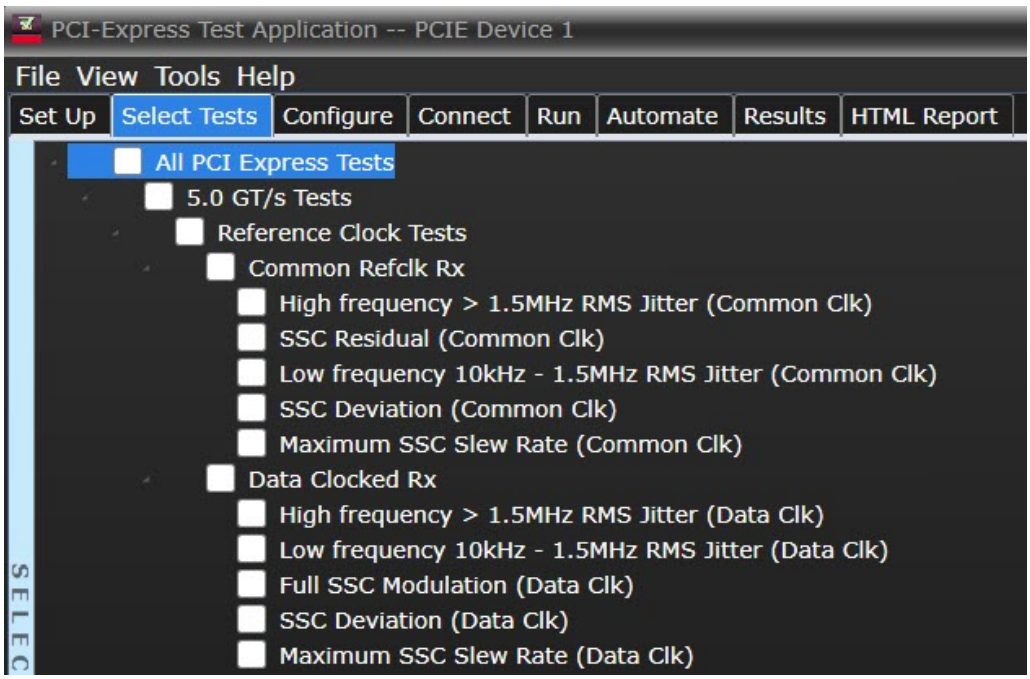


Figure 110 Gen 3.0, 5.0 GT/s, Reference Clock Tests

Reference Clock Tests - Common Refclk Rx

- High frequency > 1.5MHz RMS Jitter (Common Clk); see "High Frequency >1.5 MHz RMS Jitter (Common Clk) (Data Clk) Test" on page 375
- SSC Residual (Common Clk); see "SSC Residual (Common Clk) Test" on page 383
- Low frequency 10kHz - 1.5MHz RMS Jitter (Common Clk); see "Low Frequency 10 kHz to 1.5 MHz RMS Jitter (Common Clk) (Data Clk) Test" on page 387
- SSC Deviation (Common Clk); see "SSC Deviation (Common Clk) (Data Clk) Test" on page 395
- Maximum SSC Slew Rate (Common Clk); see "Maximum SSC Slew Rate (Common Clk) (Data Clk) Test" on page 400

Reference Clock Tests - Data Clocked Rx

- High frequency > 1.5MHz RMS Jitter (Data Clk); see "High Frequency >1.5 MHz RMS Jitter (Common Clk) (Data Clk) Test" on page 375
- Low frequency 10kHz - 1.5MHz RMS Jitter (Data Clk); see "Low Frequency 10 kHz to 1.5 MHz RMS Jitter (Common Clk) (Data Clk) Test" on page 387
- Full SSC Modulation (Data Clk); see "Full SSC Modulation (Data Clk) Test" on page 405
- SSC Deviation (Data Clk); see "SSC Deviation (Common Clk) (Data Clk) Test" on page 395
- Maximum SSC Slew Rate (Data Clk); see "Maximum SSC Slew Rate (Common Clk) (Data Clk) Test" on page 400

Gen 3.0, 8.0 GT/s, Tests

Transmitter Tests

This section lists the Transmitter Tests for PCI Express Gen 3.0 at 8.0 GT/s:

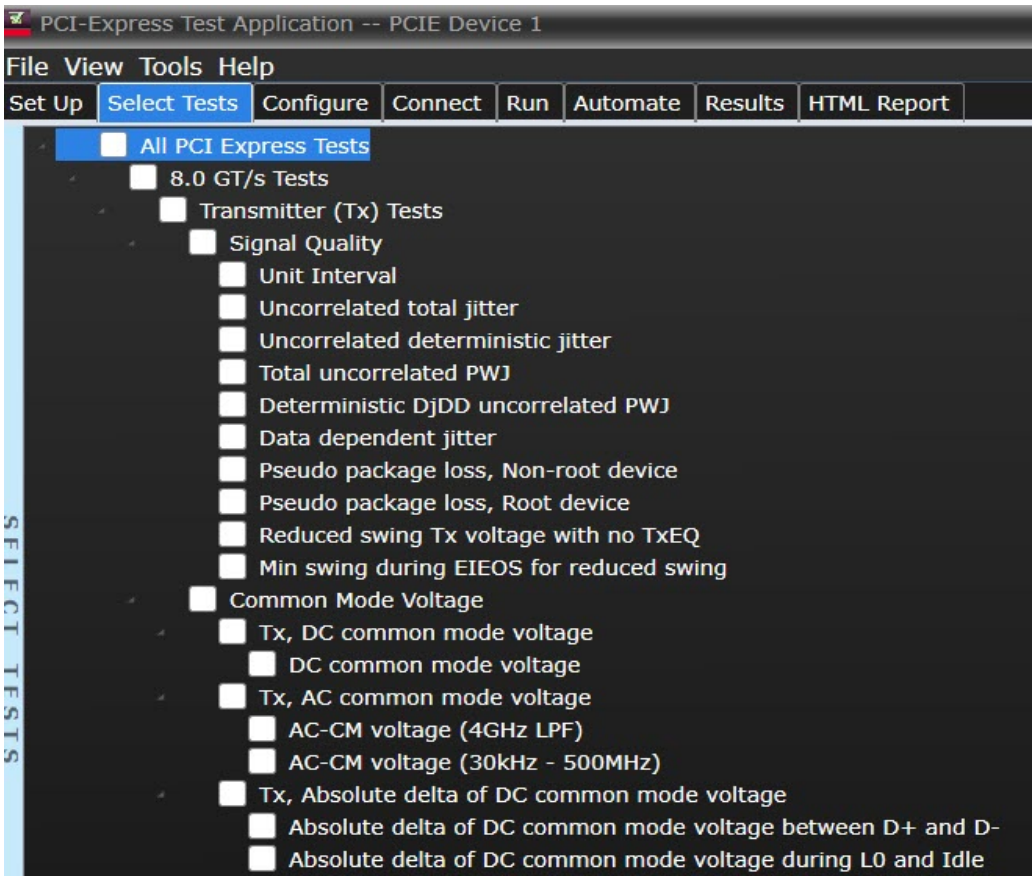


Figure 111 Gen 3.0, 8.0 GT/s, Transmitter Tests

Transmitter (Tx) Tests - Signal Quality

- Unit Interval; see "Unit Interval Test" on page 54
- Uncorrelated total jitter; see "Uncorrelated Total Jitter Test" on page 302
- Uncorrelated deterministic jitter; see "Uncorrelated Deterministic Jitter Test" on page 306
- Total uncorrelated PWJ; see "Total Uncorrelated PWJ (Pulse Width Jitter) Test" on page 310
- Deterministic DjDD uncorrelated PWJ; see "Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test" on page 314
- Data dependent jitter; see "Data Dependent Jitter Test" on page 318
- Pseudo package loss, Non-root device; see "Random Jitter Test" on page 322
- Pseudo package loss, Root device; see "Pseudo Package Loss, Root Device Test" on page 332
- Reduced swing Tx voltage with no TxEQ; see "Reduced Swing Tx Voltage with no TxEQ Test" on page 358
- Min swing during EIEOS for full swing; see "Min Swing During EIEOS for Full Swing Test" on page 362
- Min swing during EIEOS for reduced swing; see "Min Swing During EIEOS for Reduced Swing Test" on page 369

Transmitter (Tx) Tests - Common Mode Voltage

- DC Common Mode Voltage; see "DC Common-Mode Voltage Test" on page 261
- AC-CM Voltage (4GHz LPF); see "AC Common-Mode Voltage (4 GHz or 8 GHz LPF) Test" on page 266
- AC-CM Voltage (30kHz - 500MHz); see "AC Common Mode Voltage (30 kHz to 500 MHz) Test" on page 252
- Absolute Delta of DC Common Mode Voltage Between D+ and D-; see "Absolute Delta of DC Common Mode Voltage Between D+ and D- Test" on page 272
- Absolute Delta of DC Common Mode Voltage During L0 and Idle; see "Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test" on page 256

CEM EndPoint Tests

This section lists the CEM EndPoint Tests for PCI Express Gen 3.0 at 8.0 GT/s:

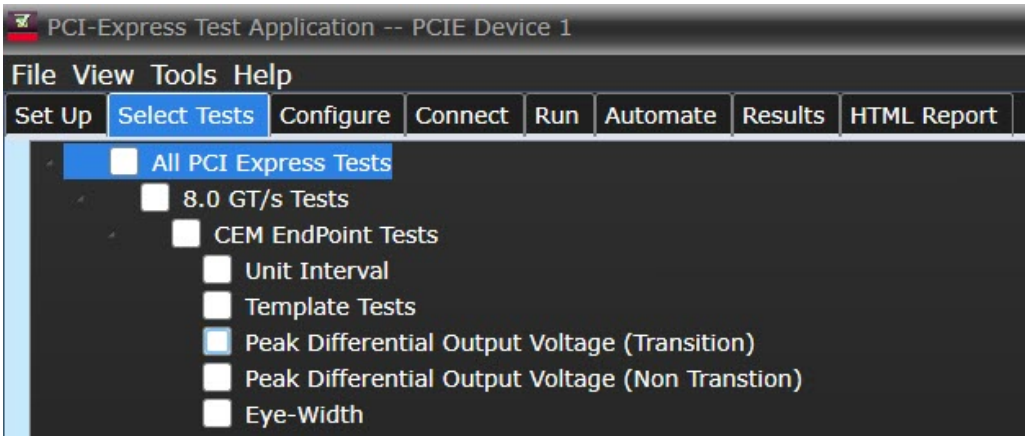


Figure 112 Gen 3.0, 8.0 GT/s, CEM EndPoint Tests

CEM EndPoint Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Eye-Width; see "Eye-Width Test" on page 85

CEM RootComplex Tests

This section lists the CEM RootComplex Tests for PCI Express Gen 3.0 at 8.0 GT/s:

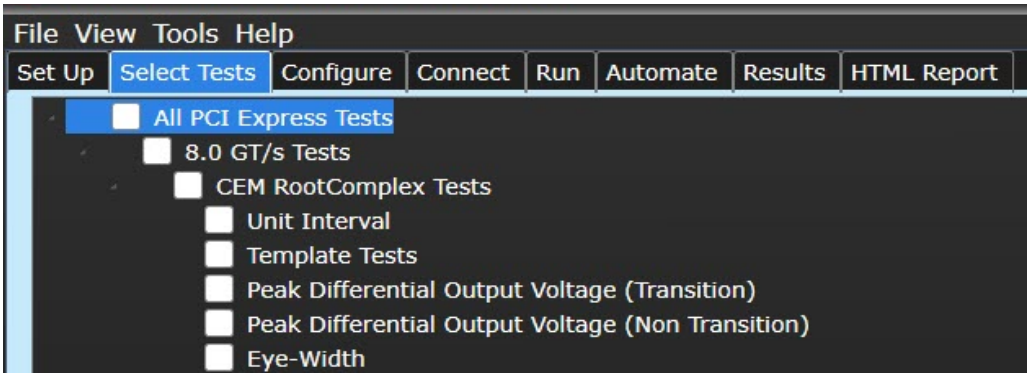


Figure 113 Gen 3.0, 8.0 GT/s, CEM RootComplex Tests

CEM Root Complex Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Tests; see "Template Test" on page 63
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Eye-Width; see "Eye-Width Test" on page 85

U.2 EndPoint Tests

This section lists the U.2 EndPoint Tests for PCI Express Gen 3.0 at 8.0 GT/s:

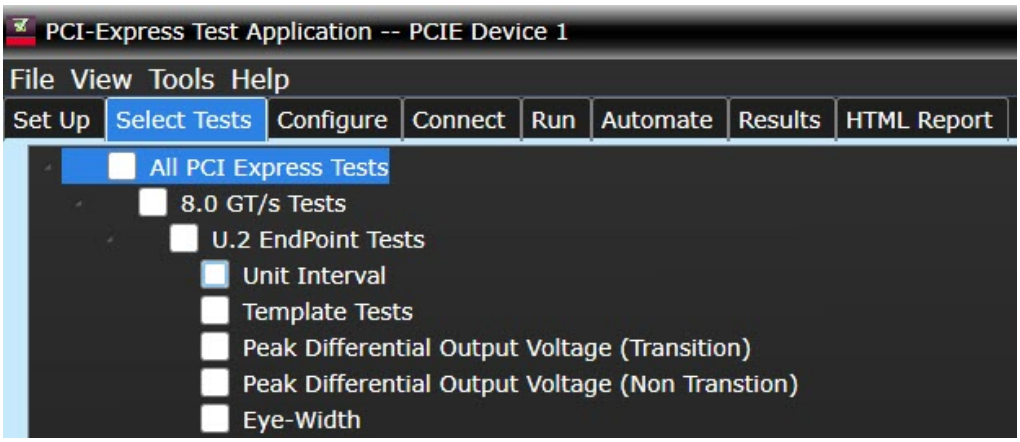


Figure 114 Gen 3.0, 8.0 GT/s, U.2 EndPoint Tests

U.2 EndPoint Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Eye-Width; see "Eye-Width Test" on page 85

U.2 RootComplex Tests

This section lists the U.2 RootComplex Tests for PCI Express Gen 3.0 at 8.0 GT/s:

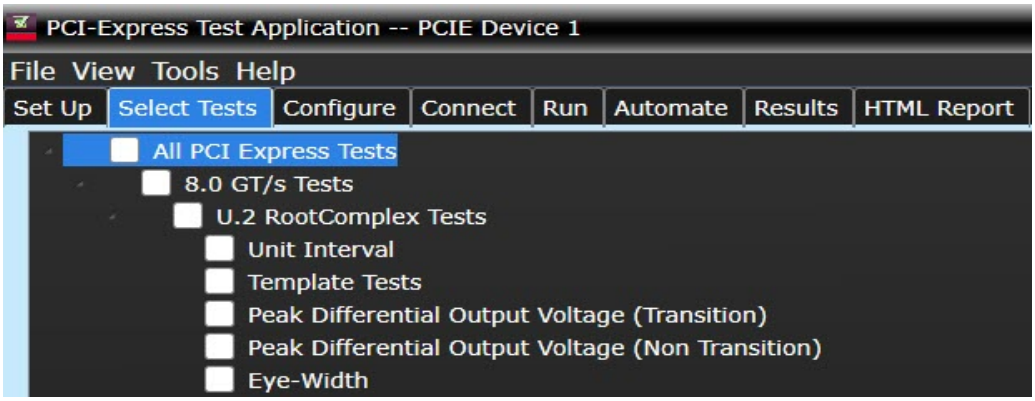


Figure 115 Gen 3.0, 8.0 GT/s, U.2 RootComplex Tests

U.2 RootComplex Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Eye-Width; see "Eye-Width Test" on page 85

Reference Clock Tests

This section lists the Reference Clock Tests for PCI Express Gen 3.0 at 8.0 GT/s:

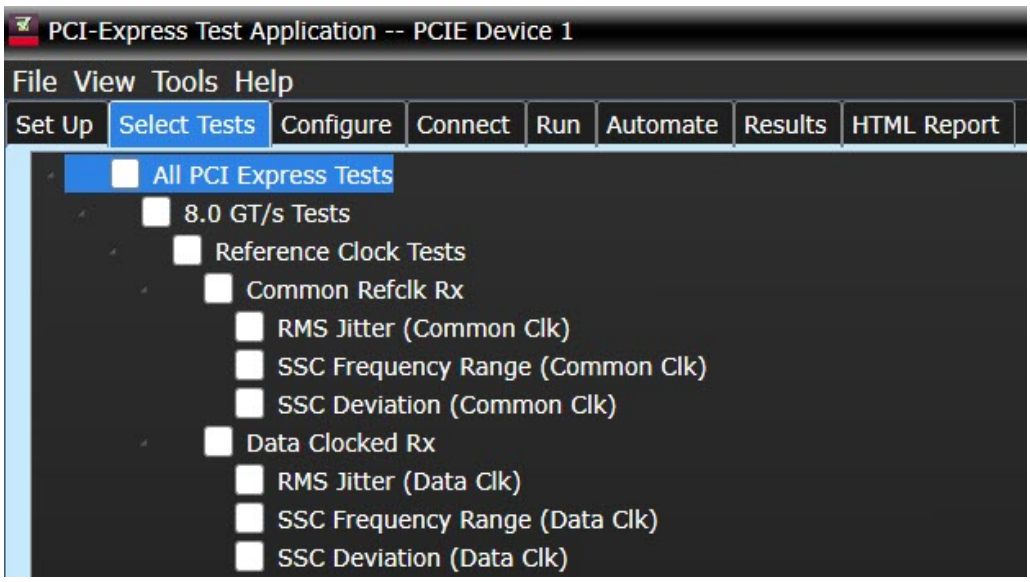


Figure 116 Gen 3.0, 8.0 GT/s, Reference Clock Tests

Reference Clock Tests - Common Refclk Rx

- RMS Jitter (Common Clk); see "Clock Frequency (Common Clk) (Data Clk) Test" on page 409
- SSC Frequency Range (Common Clk); see "SSC Frequency Range (Common Clk) (Data Clk)Test" on page 421
- SSC Deviation (Common Clk); see "SSC Deviation (Common Clk) (Data Clk) Test" on page 395
- Clock Frequency (Common Clk) (Data Clk): see "Clock Frequency (Common Clk) (Data Clk) Test" on page 409

Reference Clock Tests - Data Clocked Rx

- RMS Jitter (Data Clk); see "Clock Frequency (Common Clk) (Data Clk) Test" on page 409
- SSC Frequency Range (Data Clk); see "SSC Frequency Range (Common Clk) (Data Clk)Test" on page 421
- SSC Deviation (Data Clk); see "SSC Deviation (Common Clk) (Data Clk) Test" on page 395
- Clock Frequency (Common Clk) (Data Clk): see "Clock Frequency (Common Clk) (Data Clk) Test" on page 409

Gen 4.0, 2.5 GT/s, Tests

Transmitter Tests

This section lists the Transmitter Tests for PCI Express Gen 4.0 at 2.5 GT/s:

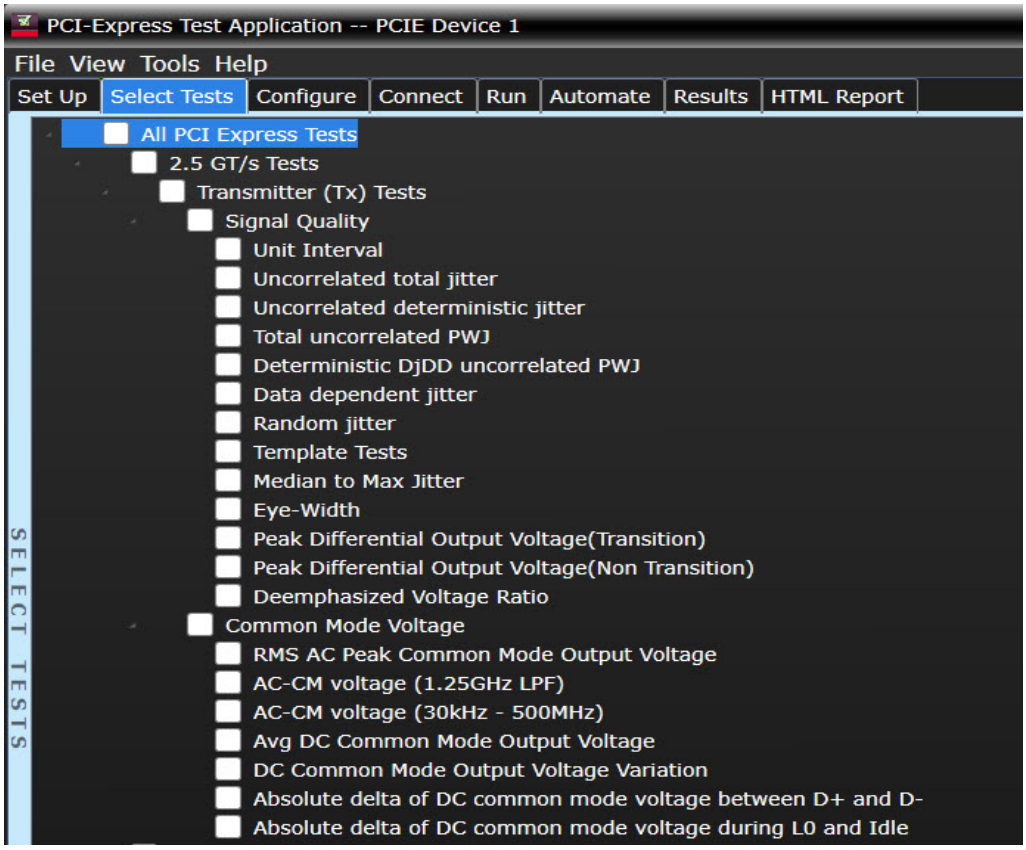


Figure 117 Gen 4.0, 2.5 GT/s, Transmitter Tests

Transmitter (Tx) Tests - Signal Quality

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test (Low Power) (Full Power); see "Template Test" on page 63
- Median to Max Jitter (Low Power) (Full Power); see "Median to Max Jitter Test" on page 77
- Eye-Width (Low Power) (Full Power); see "Eye-Width Test" on page 85
- Uncorrelated Total Jitter; see "Uncorrelated Total Jitter Test" on page 302
- Uncorrelated Deterministic Jitter; see "Uncorrelated Deterministic Jitter Test" on page 306
- Total Uncorrelated PWJ; see "Total Uncorrelated PWJ (Pulse Width Jitter) Test" on page 310
- Deterministic DjDD Uncorrelated PWJ; see "Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test" on page 314
- Data Dependent Jitter; see "Data Dependent Jitter Test" on page 318
- Random Jitter; see "Random Jitter Test" on page 322
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102

- Peak Differential Output Voltage (Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Deemphasized Voltage Ratio; see "Deemphasized Voltage Ratio Test" on page 143

Transmitter (Tx) Tests - Common Mode Voltage

- RMS AC Peak Common Mode Output Voltage; see "RMS AC Peak Common Mode Output Voltage Test" on page 165
- AC-CM Voltage (1.25 GHz or 2.5 GHz LPF); see "AC Common Mode Voltage (1.25 GHz or 2.5 GHz LPF) Test" on page 247
- AC-CM Voltage (30 kHz to 500 MHz); see "AC Common Mode Voltage (30 kHz to 500 MHz) Test" on page 252k
- Avg DC Common Mode Output Voltage; see "Avg DC Common Mode Output Voltage Test" on page 170
- DC Common Mode Output Voltage Variation; see "DC Common Mode Output Voltage Variation Test" on page 175
- Absolute Delta of DC Common Mode Voltage between D+ and D-; see "Absolute Delta of DC Common Mode Voltage Between D+ and D- Test" on page 272
- Absolute Delta of DC Common Mode Voltage between L0 and Idle; see "Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test" on page 256

CEM EndPoint Tests

This section lists the CEM EndPoint Tests for PCI Express Gen 4.0 at 2.5 GT/s:

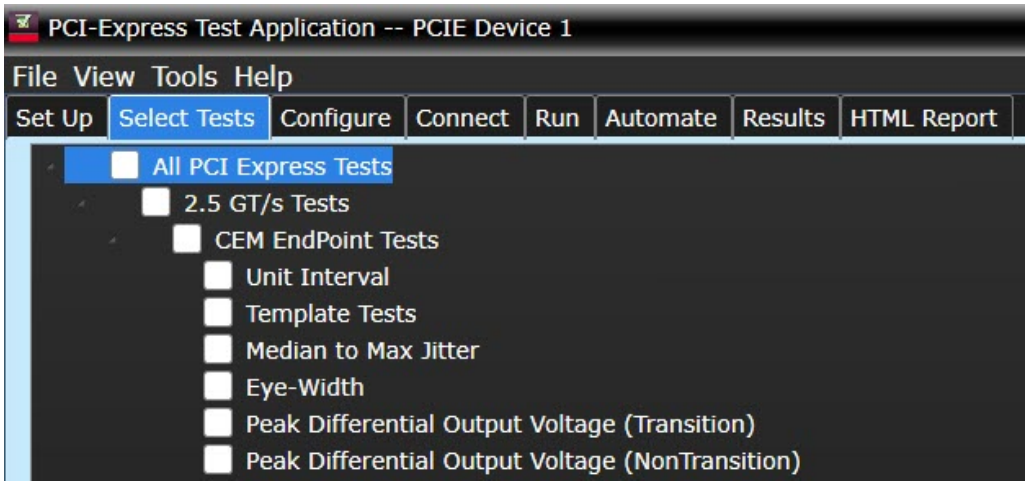


Figure 118 Gen 4.0, 2.5 GT/s, CEM EndPoint Tests

CEM EndPoint Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Median to Max Jitter; see "Median to Max Jitter Test" on page 77
- Eye-Width; see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

CEM RootComplex Tests

This section lists the CEM RootComplex Tests for PCI Express Gen 4.0 at 2.5 GT/s:

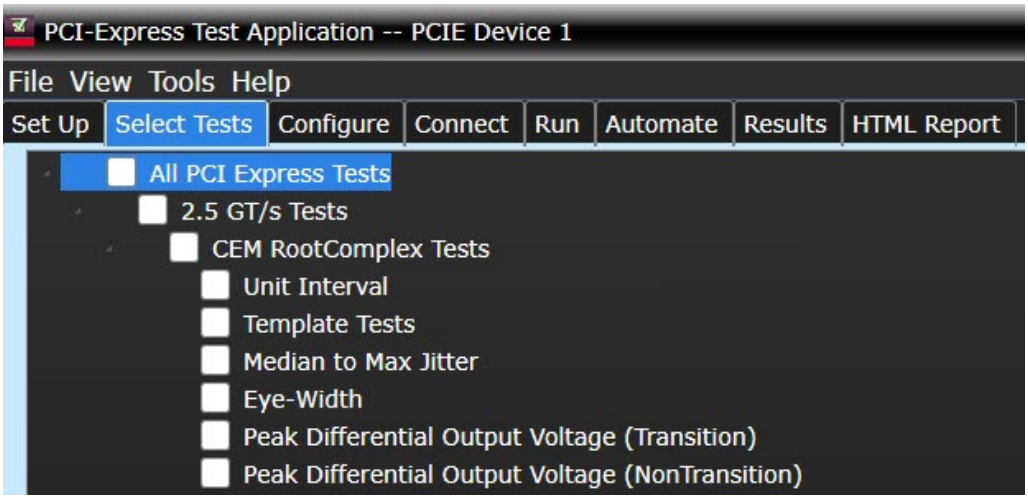


Figure 119 Gen 4.0, 2.5 GT/s, CEM RootComplex Tests

CEM RootComplex Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Median to Max Jitter; see "Median to Max Jitter Test" on page 77
- Eye-Width; see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

Reference Clock Tests

This section lists the Reference Clock Tests for PCI Express Gen 4.0 at 2.5 GT/s:

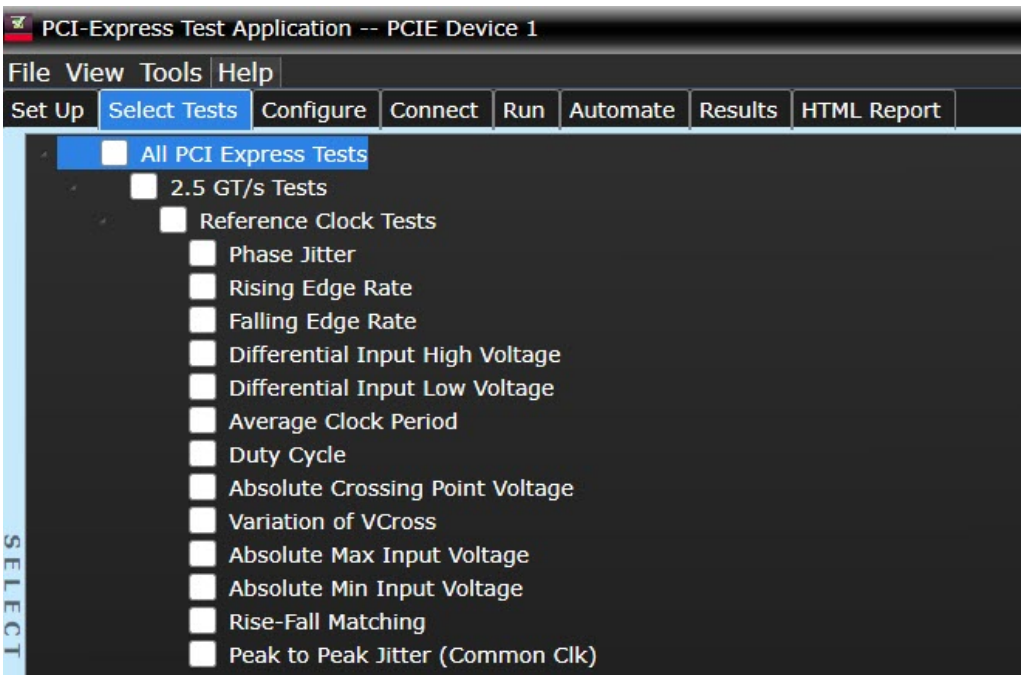


Figure 120 Gen 4.0, 2.5 GT/s, Reference Clock Tests

Reference Clock Tests

- Phase Jitter; see "Phase Jitter Test" on page 177
- Rising Edge Rate; see "Rising Edge Rate Test" on page 184
- Falling Edge Rate; see "Falling Edge Rate Test" on page 189
- Differential Input High Voltage; see "Differential Input High Voltage Test" on page 195
- Differential Input Low Voltage; see "Differential Input Low Voltage Test" on page 200
- Average Clock Period; see "Average Clock Period Test" on page 205
- Duty Cycle; see "Duty Cycle Test" on page 211
- Absolute Crossing Point Voltage; see "Absolute Crossing Point Voltage Test" on page 217
- Variation of VCross; see "Variation of V_{Cross} Test" on page 222
- Absolute Max Input Voltage; see "Absolute Max Input Voltage Test" on page 226
- Absolute Min Input Voltage; see "Absolute Min Input Voltage Test" on page 231
- Rise-Fall Matching; see "Rise-Fall Matching Test" on page 236
- Peak to Peak Jitter (Common Clk); see "Peak to Peak Jitter (Common Clk) Test" on page 241

Gen 4.0, 5.0 GT/s, Tests

Transmitter Tests

This section lists the Transmitter Tests for PCI Express Gen 4.0 at 5.0 GT/s:

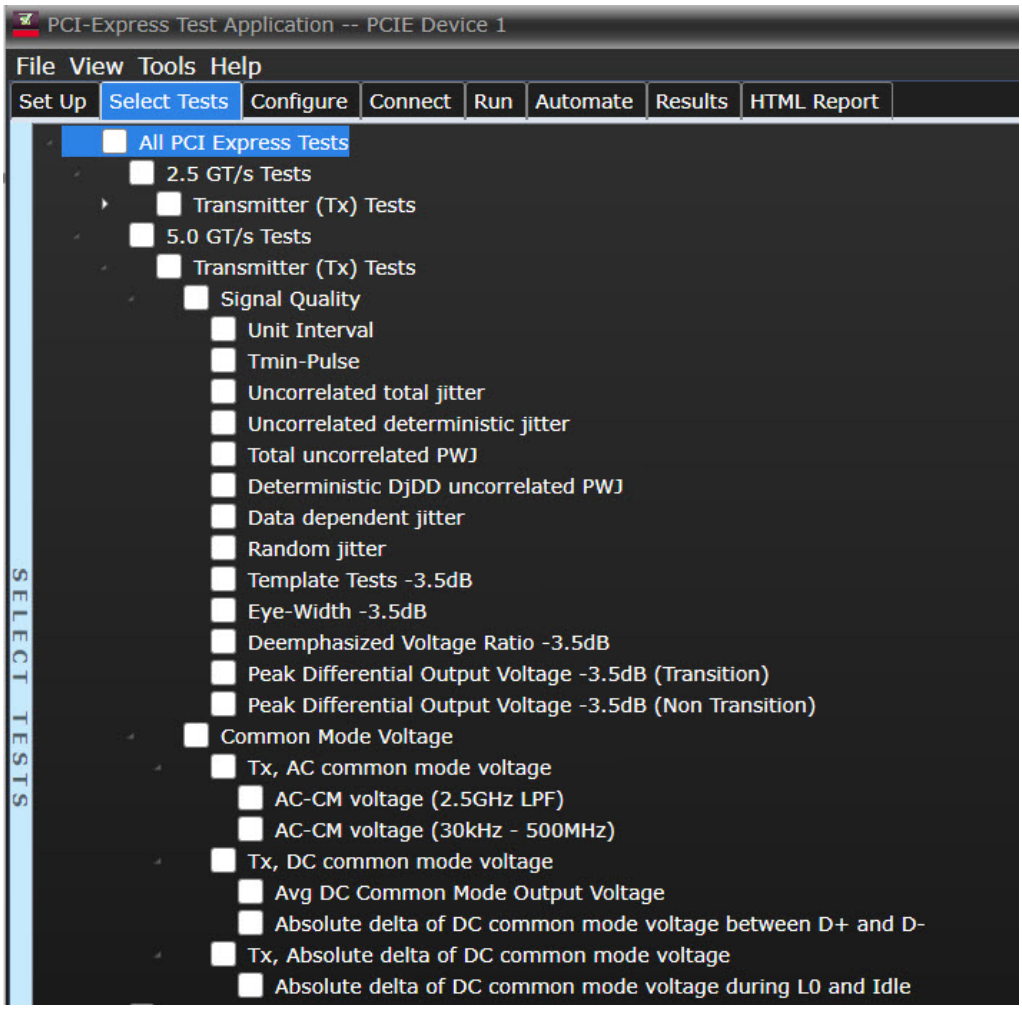


Figure 121 Gen 4.0, 5.0 GT/s, Transmitter Tests

Transmitter (Tx) Tests - Signal Quality

- Unit Interval; see "Unit Interval Test" on page 54
- Tmin-Pulse; see "Tmin-Pulse" on page 150
- Eye-Width; see "Eye-Width Test" on page 85
- Peak Differential Output Voltage (Transition) (Low Power) (Full Power); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition) (Low Power) (Full Power); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Uncorrelated Total Jitter; see "Uncorrelated Total Jitter Test" on page 302
- Uncorrelated Deterministic Jitter; see "Uncorrelated Deterministic Jitter Test" on page 306
- Total Uncorrelated PWJ; see "Total Uncorrelated PWJ (Pulse Width Jitter) Test" on page 310
- Deterministic DjDD Uncorrelated PWJ; see "Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test" on page 314
- Data Dependent Jitter; see "Data Dependent Jitter Test" on page 318
- Random Jitter; see "Random Jitter Test" on page 322
- Template Tests (Low Power) (Full Power); see "Template Test" on page 63
- Deemphasized Voltage Ratio. see "Deemphasized Voltage Ratio Test" on page 143

Transmitter (Tx) Tests - Common Mode Voltage

- AC Peak Common Mode Output Voltage (2.5 GHz); see "The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX\text{-}CM\text{-}AC\text{-}PP}$ is the value of difference between the maximum and minimum of the common mode signal." on page 247
- AC-CM Voltage (30kHz - 500MHz); see "AC Common Mode Voltage (30 kHz to 500 MHz) Test" on page 252
- Avg DC Common Mode Output Voltage; see "Avg DC Common Mode Output Voltage Test" on page 170
- Absolute Delta of DC Common Mode Voltage During D+and D-; see "Absolute Delta of DC Common Mode Voltage Between D+ and D- Test" on page 272
- Absolute Delta of DC Common Mode Voltage During L0 and Idle; see "Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test" on page 256

CEM EndPoint Tests

This section lists the CEM EndPoint Tests for PCI Express Gen 4.0 at 5.0 GT/s:

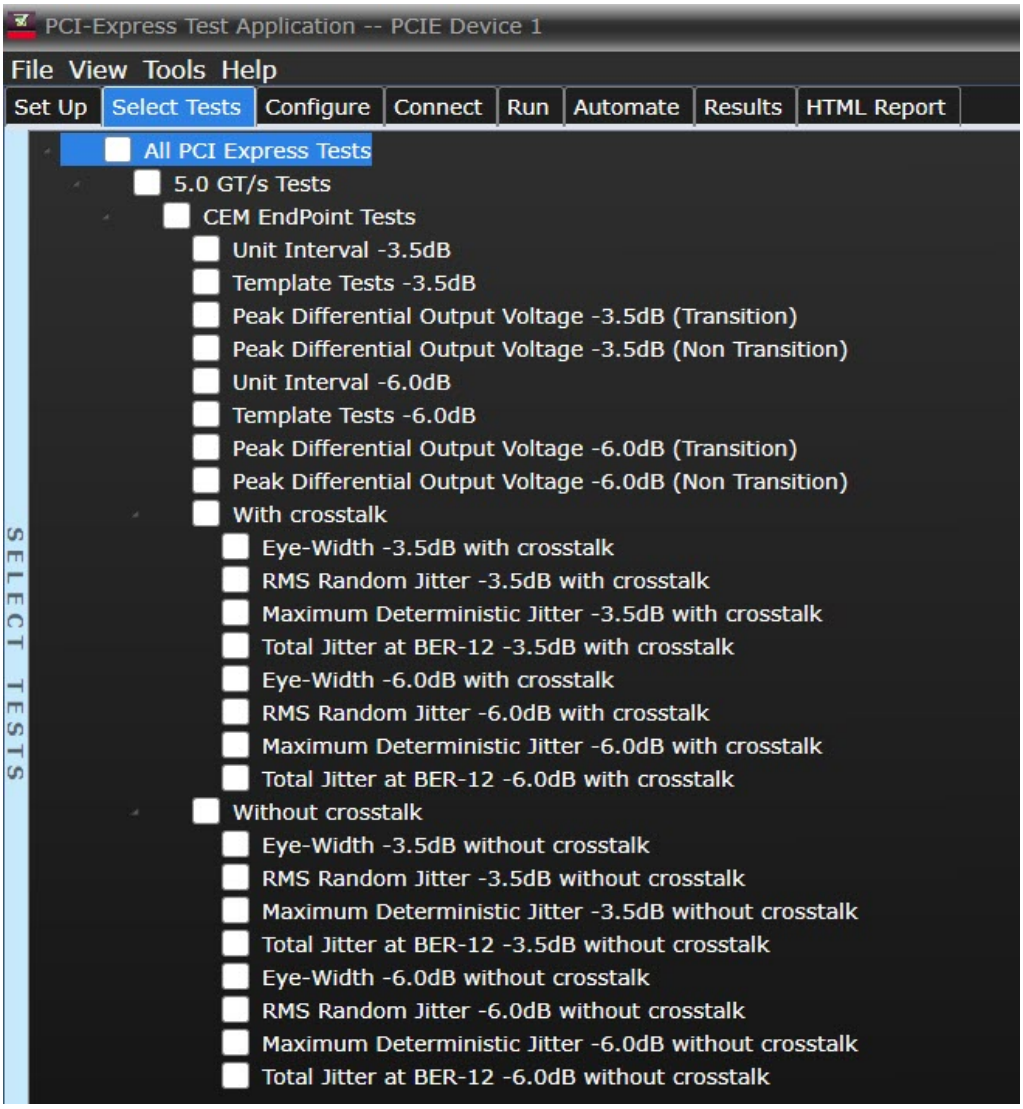


Figure 122 Gen 4.0, 5.0 GT/s, CEM EndPoint Tests

CEM EndPoint Tests

- Unit Interval -3.5dB; see "Unit Interval Test" on page 54
- Template Test -3.5dB; see "Template Test" on page 63
- Peak Differential Output Voltage -3.5dB (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage -3.5dB (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Unit Interval -6.0dB; see "Unit Interval Test" on page 54
- Template Test -6.0dB; see "Template Test" on page 63
- Peak Differential Output Voltage -6.0dB (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage -6.0dB (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

CEM EndPoint Tests - With Crosstalk

- Eye-Width -3.5dB with Crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter -3.5dB with Crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter -3.5dB with Crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 -3.5dB with Crosstalk; see "Total Jitter at BER-12 Test" on page 293
- Eye-Width -6.0dB with Crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter -6.0dB with Crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter -6.0dB with Crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 -6.0dB with Crosstalk; see "Total Jitter at BER-12 Test" on page 293

CEM EndPoint Tests - Without Crosstalk

- Eye-Width -3.5dB without Crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter -3.5dB without Crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter -3.5dB without Crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 -3.5dB without Crosstalk; see "Total Jitter at BER-12 Test" on page 293
- Eye-Width -6.0dB without Crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter -6.0dB without Crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter -6.0dB without Crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 -6.0dB without Crosstalk; see "Total Jitter at BER-12 Test" on page 293

CEM RootComplex Tests

This section lists the CEM RootComplex Tests for PCI Express Gen 4.0 at 5.0 GT/s:

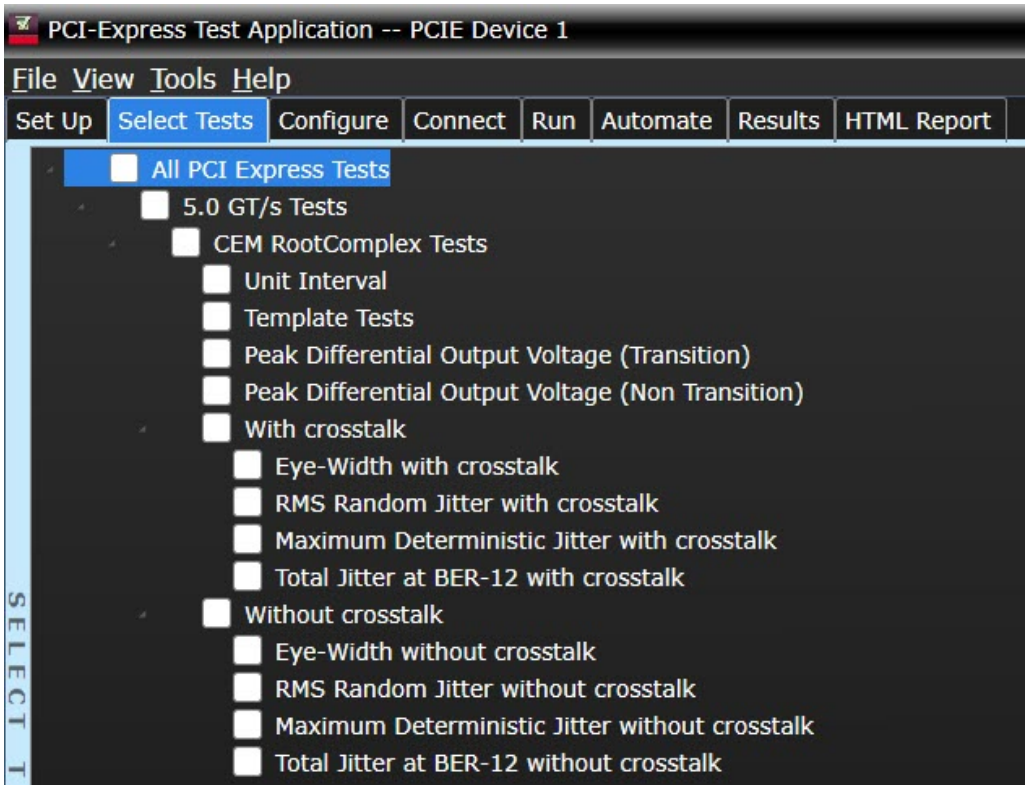


Figure 123 Gen 4.0, 5.0 GT/s, CEM RootComplex Tests

CEM RootComplex Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121

CEM RootComplex Tests - With Crosstalk

- Eye-Width with Crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter with Crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter with Crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 with Crosstalk; see "Total Jitter at BER-12 Test" on page 293

CEM RootComplex Tests - Without Crosstalk

- Eye-Width without Crosstalk; see "Eye-Width Test" on page 85
- RMS Random Jitter without Crosstalk; see "RMS Random Jitter" on page 276
- Maximum Deterministic Jitter without Crosstalk; see "Maximum Deterministic Jitter Test" on page 283
- Total Jitter at BER -12 without Crosstalk; see "Total Jitter at BER-12 Test" on page 293

Reference Clock Tests

This section lists the Reference Clock Tests for PCI Express Gen 4.0 at 5.0 GT/s:

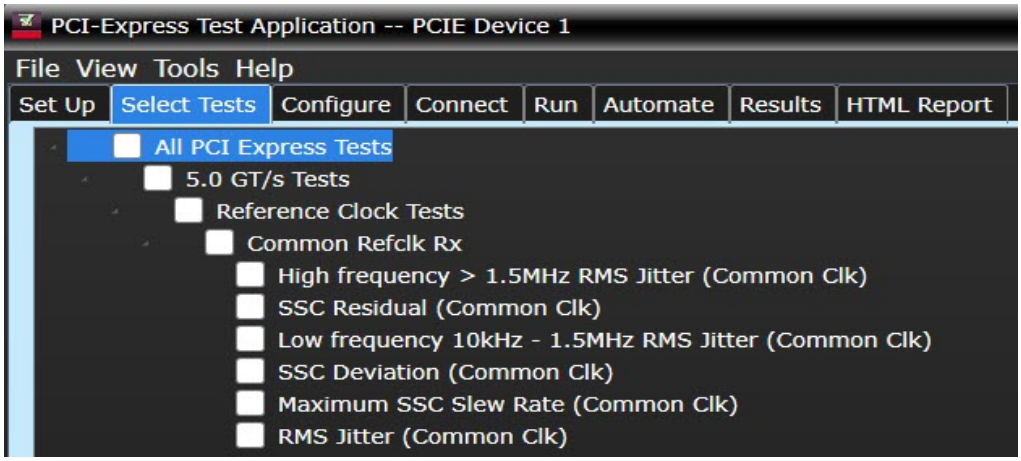


Figure 124 Gen 4.0, 5.0 GT/s, Reference Clock Tests

Reference Clock Tests - Common Refclk Rx

- High frequency > 1.5MHz RMS Jitter (Common Clk); see "High Frequency >1.5 MHz RMS Jitter (Common Clk) (Data Clk) Test" on page 375
- SSC Residual (Common Clk); see "SSC Residual (Common Clk) Test" on page 383
- Low frequency 10kHz - 1.5MHz RMS Jitter (Common Clk); see "Low Frequency 10 kHz to 1.5 MHz RMS Jitter (Common Clk) (Data Clk) Test" on page 387
- SSC Deviation (Common Clk); see "SSC Deviation (Common Clk) (Data Clk) Test" on page 395
- Maximum SSC Slew Rate (Common Clk); see "Maximum SSC Slew Rate (Common Clk) (Data Clk) Test" on page 400

Gen 4.0, 8.0 GT/s, Tests

Transmitter Tests

This section lists the Transmitter Tests for PCI Express Gen 4.0 at 8.0 GT/s:

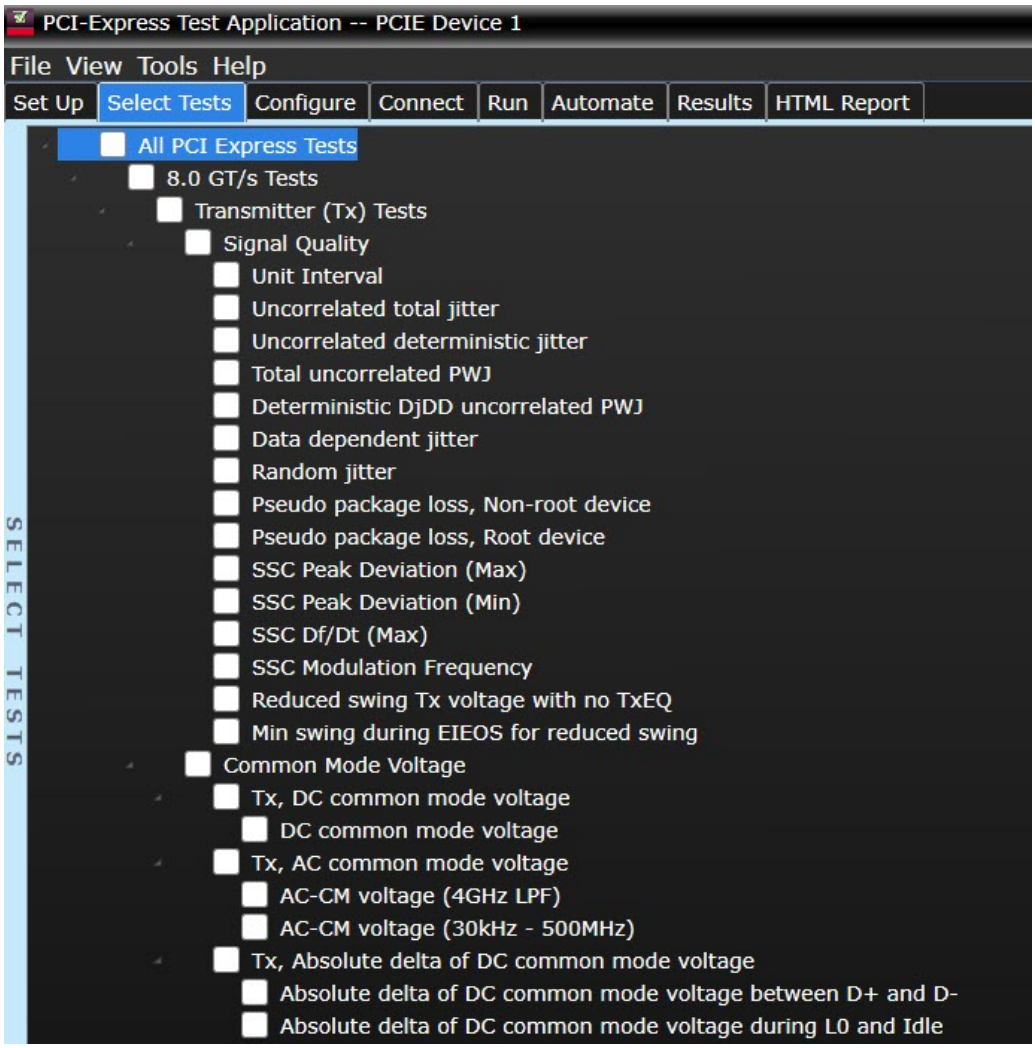


Figure 125 Gen 4.0, 8.0 GT/s, Transmitter Tests

Transmitter (Tx) Tests - Signal Quality

- Unit Interval; see "Unit Interval Test" on page 54
- Uncorrelated total jitter; see "Uncorrelated Total Jitter Test" on page 302
- Uncorrelated deterministic jitter; see "Uncorrelated Deterministic Jitter Test" on page 306
- Total uncorrelated PWJ; see "Total Uncorrelated PWJ (Pulse Width Jitter) Test" on page 310
- Deterministic DjDD uncorrelated PWJ; see "Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test" on page 314
- Data dependent jitter; see "Data Dependent Jitter Test" on page 318
- Random Jitter; see "Random Jitter Test" on page 322
- Pseudo package loss, Non-root device; see "Pseudo Package Loss, Non-Root Device Test" on page 326
- Pseudo package loss, Root device; see "Pseudo Package Loss, Root Device Test" on page 332
- SSC Peak Deviation (Max); see "SSC Peak Deviation (Max)" on page 337
- SSC Peak Deviation (Min); see "SSC Peak Deviation (Min)" on page 341
- SSC Df/Dt (Max); see "SSC Max df/dt (Slew Rate) Test" on page 345
- SSC Modulation Frequency; see "SSC Modulation Frequency" on page 350
- Full Swing Tx Voltage with no TxEQ; see "Full Swing Tx Voltage with no TxEQ Test" on page 354
- Reduced Swing Tx Voltage with no TxEQ; see "Reduced Swing Tx Voltage with no TxEQ Test" on page 358
- Min swing during EIEOS for full swing; see "Min Swing During EIEOS for Full Swing Test" on page 362
- Min swing during EIEOS for reduced swing; see "Min Swing During EIEOS for Reduced Swing Test" on page 369

Transmitter (Tx) Tests - Common Mode Voltage

- DC Common Mode Voltage; see "Unit Interval Test" on page 54
- AC-CM Voltage (4GHz LPF); see "AC Common-Mode Voltage (4 GHz or 8 GHz LPF) Test" on page 266
- AC-CM Voltage (30kHz - 500MHz); see "AC Common Mode Voltage (30 kHz to 500 MHz) Test" on page 252
- Absolute Delta of DC Common Mode Voltage Between D+ and D-; see "Absolute Delta of DC Common Mode Voltage Between D+ and D- Test" on page 272
- Absolute Delta of DC Common Mode Voltage During L0 and Idle; see "Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test" on page 256

CEM EndPoint Tests

This section lists the CEM EndPoint Tests for PCI Express Gen 4.0 at 8.0 GT/s:

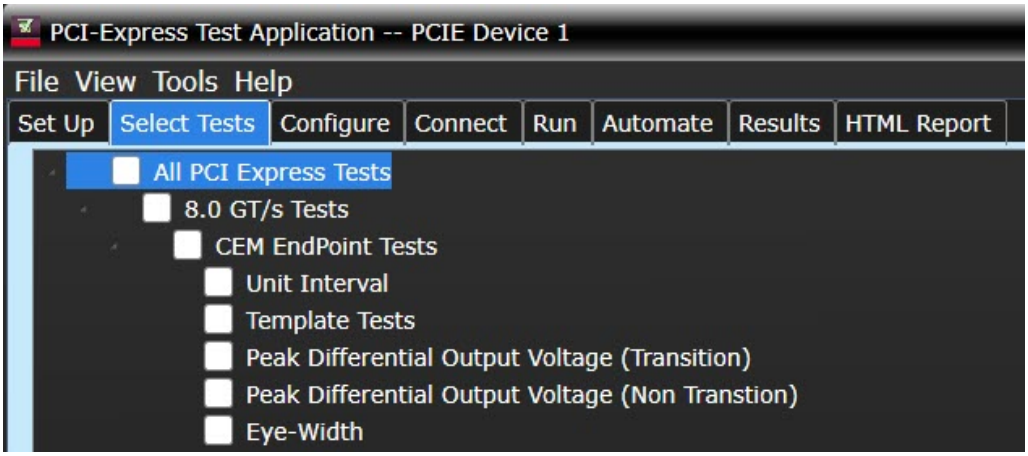


Figure 126 Gen 4.0, 8.0 GT/s, CEM EndPoint Tests

CEM EndPoint Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Test; see "Template Test" on page 63
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Eye-Width; see "Eye-Width Test" on page 85

CEM RootComplex Tests

This section lists the CEM RootComplex Tests for PCI Express Gen 4.0 at 8.0 GT/s:

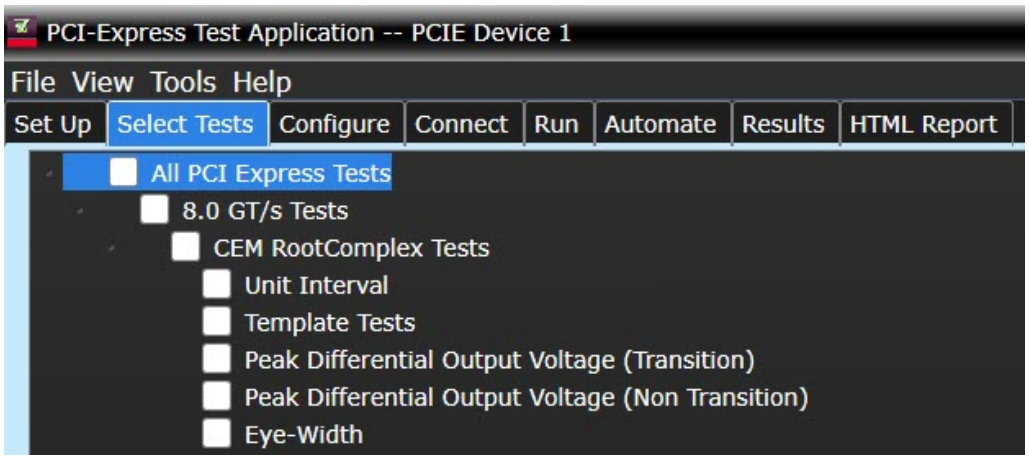


Figure 127 Gen 4.0, 8.0 GT/s, CEM RootComplex Tests

CEM RootComplex Tests

- Unit Interval; see "Unit Interval Test" on page 54
- Template Tests; see "Template Test" on page 63
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Eye-Width; see "Eye-Width Test" on page 85

Reference Clock Tests

This section lists the Reference Clock Tests for PCI Express Gen 4.0 at 8.0 GT/s:

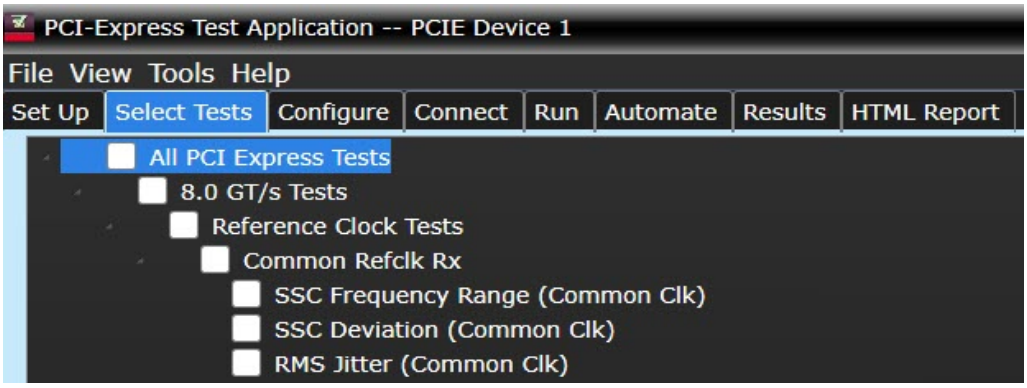


Figure 128 Gen 4.0, 8.0 GT/s, Reference Clock Tests

Reference Clock Tests - Common Refclk Rx

- SSC Frequency Range (Common Clk); see "SSC Frequency Range (Common Clk) (Data Clk)Test" on page 421
- SSC Deviation (Common Clk); see "SSC Deviation (Common Clk) (Data Clk) Test" on page 395
- RMS Jitter (Common Clk); see "Clock Frequency (Common Clk) (Data Clk) Test" on page 409
- Clock Frequency (Common Clk) (Data Clk): see "Clock Frequency (Common Clk) (Data Clk) Test" on page 409

Gen 4.0, 16.0 GT/s, Tests

Transmitter Tests

This section lists the Transmitter Tests for PCI Express Gen 4.0 at 16.0 GT/s:

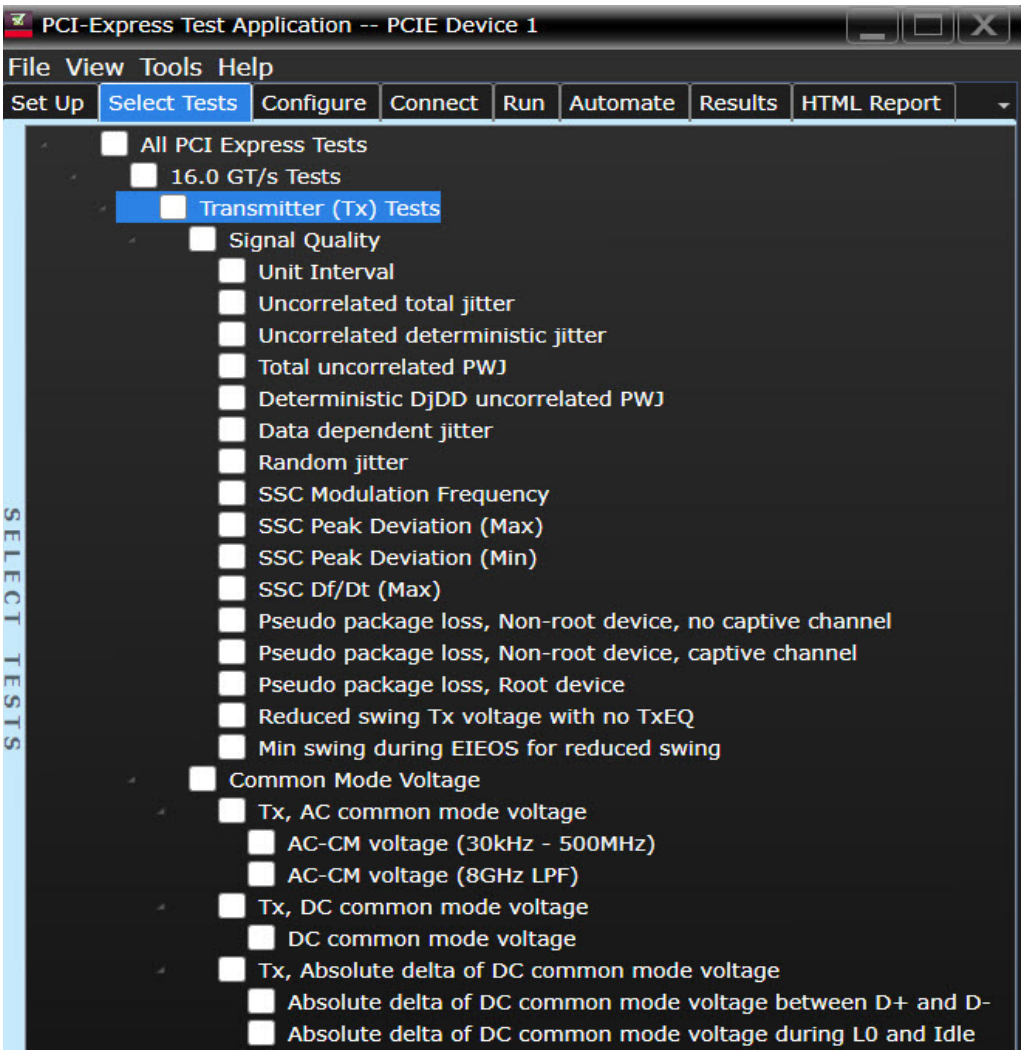


Figure 129 Gen 4.0, 16.0 GT/s, Transmitter Tests

Transmitter (Tx) Tests - Signal Quality

- Unit Interval; see "Unit Interval Test" on page 54
- Uncorrelated total jitter; see "Uncorrelated Total Jitter Test" on page 302
- Uncorrelated deterministic jitter; see "Uncorrelated Deterministic Jitter Test" on page 306
- Total uncorrelated PWJ; see "Total Uncorrelated PWJ (Pulse Width Jitter) Test" on page 310
- Deterministic DjDD uncorrelated PWJ; see "Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test" on page 314
- Data dependent jitter; see "Data Dependent Jitter Test" on page 318
- Random Jitter; see "Random Jitter Test" on page 322
- SSC Modulation Frequency; see "SSC Modulation Frequency" on page 350
- SSC Peak Deviation (Max); see "SSC Peak Deviation (Max)" on page 337
- SSC Peak Deviation (Min); see "SSC Peak Deviation (Min)" on page 341
- SSC Df/Dt (Max); see "SSC Max df/dt (Slew Rate) Test" on page 345
- Pseudo package loss, Non-root device, no captive channel; see "Pseudo Package Loss, Non-Root Device Test" on page 326
- Pseudo package loss, Non-root device, captive channel; see "Pseudo Package Loss, Non-Root Device Test" on page 326
- Pseudo package loss, Root device; see "Pseudo Package Loss, Root Device Test" on page 332
- Full Swing Tx Voltage with no TxEQ; see "Full Swing Tx Voltage with no TxEQ Test" on page 354
- Reduced Swing Tx Voltage with no TxEQ; see "Reduced Swing Tx Voltage with no TxEQ Test" on page 358
- Min swing during EIEOS for full swing; see "Min Swing During EIEOS for Full Swing Test" on page 362
- Min swing during EIEOS for reduced swing; see "Min Swing During EIEOS for Reduced Swing Test" on page 369

Transmitter (Tx) Tests - Common Mode Voltage

- AC-CM Voltage (30kHz - 500MHz); see "AC Common Mode Voltage (30 kHz to 500 MHz) Test" on page 252
- AC-CM Voltage (8GHz LPF); see "AC Common-Mode Voltage (4 GHz or 8 GHz LPF) Test" on page 266
- DC Common Mode Voltage; see "DC Common-Mode Voltage Test" on page 261
- Absolute Delta of DC Common Mode Voltage Between D+ and D-; see "Absolute Delta of DC Common Mode Voltage Between D+ and D- Test" on page 272
- Absolute Delta of DC Common Mode Voltage During L0 and Idle; see "Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test" on page 256

CEM EndPoint Tests

This section lists the CEM EndPoint Tests for PCI Express Gen 4.0 at 16.0 GT/s:

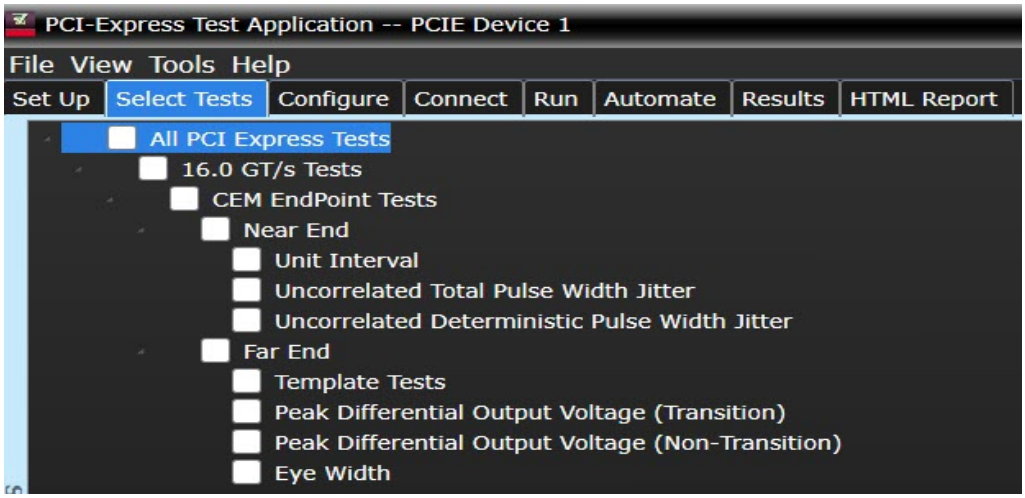


Figure 130 Gen 4.0, 16.0 GT/s, CEM EndPoint Tests

CEM EndPoint Tests - Near End

- Unit Interval; see "Unit Interval Test" on page 54
- Uncorrelated Total Pulse Width Jitter; see "Total Uncorrelated PWJ (Pulse Width Jitter) Test" on page 310
- Uncorrelated Deterministic Pulse Width Jitter; see "Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test" on page 314

CEM EndPoint Tests - Far End

- Template Test; see "Template Test" on page 63
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Eye-Width; see "Eye-Width Test" on page 85

CEM RootComplex Tests

This section lists the CEM RootComplex Tests for PCI Express Gen 4.0 at 16.0 GT/s:

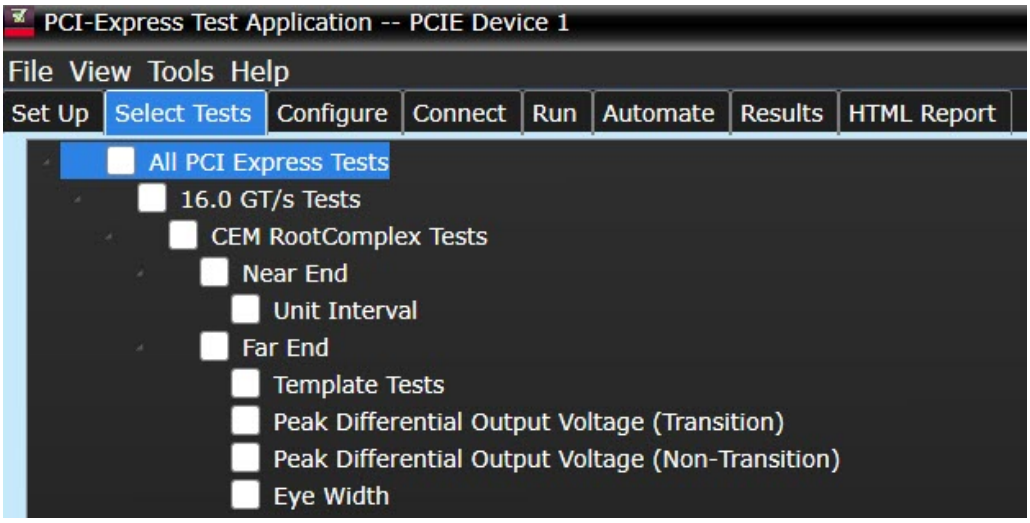


Figure 131 Gen 4.0, 16.0 GT/s, CEM RootComplex Tests

CEM RootComplex Tests - Near End

- Unit Interval; see "Unit Interval Test" on page 54

CEM RootComplex Tests - Far End

- Template Tests; see "Template Test" on page 63
- Peak Differential Output Voltage (Transition); see "Peak Differential Output/Input Voltage (Transition) Test" on page 102
- Peak Differential Output Voltage (Non Transition); see "Peak Differential Output Voltage (Non-Transition) Test" on page 121
- Eye-Width; see "Eye-Width Test" on page 85

Reference Clock Tests

This section lists the Reference Clock Tests for PCI Express Gen 4.0 at 16.0 GT/s:

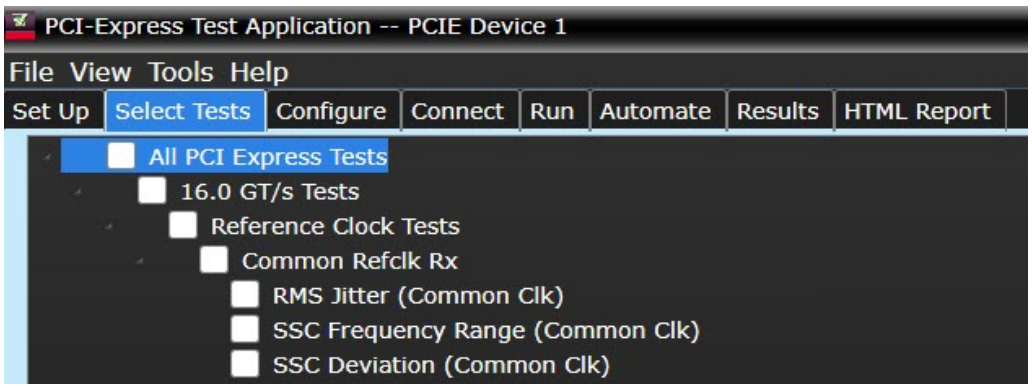


Figure 132 Gen 4.0, 16.0 GT/s, Reference Clock Tests

Reference Clock Tests - Common Refclk Rx

- RMS Jitter (Common Clk); see "Clock Frequency (Common Clk) (Data Clk) Test" on page 409
- SSC Frequency Range (Common Clk); see "SSC Frequency Range (Common Clk) (Data Clk)Test" on page 421
- SSC Deviation (Common Clk); see "SSC Deviation (Common Clk) (Data Clk) Test" on page 395
- Clock Frequency (Common Clk) (Data Clk): see "Clock Frequency (Common Clk) (Data Clk) Test" on page 409

7 Specification Notes

Gen 1.0a Spec Notes / 528
Gen 1.1 Spec Notes / 530
Gen 2.0 Spec Notes / 533
Gen 3.0 Spec Notes / 536
Gen 4.0 Spec Notes / 539

This chapter provides a generation-wise organized list of specification notes for all the tables that have been referenced for pass limits mentioned in the chapter "Compliance Tests" on page 51.

Gen 1.0a Spec Notes

Base Spec

This section lists specifications notes for all the relevant tables from PCI Express Base Specification Revision 1.0a.

Table 4-5: Differential Transmitter (TX) Output Specifications

1 No test load is necessarily associated with this value.

2 Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 and measured over any 250 consecutive TX UIs. (Also refer to the Transmitter compliance eye diagram shown in Figure 4-24.)

3 A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

4 The Transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 ohms to ground for both the D+ and D- line (i.e., as measured by a Vector Network Analyzer with 50 ohm probes - see Figure 4-25). Note that the series capacitors CTX is optional for the return loss measurement.

5 Measured between 20-80% at Transmitter package pins into a test load as shown in Figure 4-25 for both V_{TX-D+} and $V_{TX-D-.e}$

Table 4-6: Differential Receiver (RX) Input Specifications

6 No test load is necessarily associated with this value.

7 Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 4-25 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 4-26). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

8 A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total .6 UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

9 The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss 20 measurements for is 50 ohms to ground for both the D+ and D- line (i.e., as measured by a Vector Network Analyzer with 50 ohm probes - see Figure 4-25). Note: that the series capacitors CTX is optional for the return loss measurement.

10 Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.

11 The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

12 It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI 10 interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

CEM Spec

This section lists specifications notes for all the relevant tables from PCI Express CEM Specification Revision 1.0a.

Table 4-6: Add-in Card Transmitter Path Compliance Eye Requirements

The values in Table 4-6 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the add-in card. Exact conditions required for verifying compliance while generating this eye diagram are to be given in the compliance testing 15 document. The eye diagram is defined and centered with respect to the jitter median. The jitter median should be calculated across any 250 consecutive UIs. The maximum jitter outlier should be no greater than 118.5 ps away from the jitter median.

Table 4-8: System Board Transmitter Path Compliance Eye Requirements

The values in Table 4-8 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the isolated edge-finger boundary of an add-in card when mated with a connector. The eye diagram is defined and centered with respect to the jitter median. The jitter median should be calculated across any 250 consecutive UIs. The maximum jitter outlier should be no greater than 91.5 ps away from the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are to be given in the compliance testing document.

Gen 1.1 Spec Notes

Base Spec

This section lists specifications notes for all the relevant tables from PCI Express Base Specification Revision 1.1.

Table 4-5: Differential Transmitter (TX) Output Specifications

1 No test load is necessarily associated with this value.

2 Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 and measured using the clock recovery function specified in Section 4.3.3.2. (Also refer to the Transmitter compliance eye diagram shown in Figure 4-24.)

3 A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the Transmitter using the clock recovery function specified in Section 4.3.3.2. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget using the clock recovery function specified in Section 4.3.3.2. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. This parameter is measured with the equivalent of a zero jitter reference clock. The T_{TX-EYE} measurement is to be met at the target bit error rate.
The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ is to be met using the compliance pattern at a sample size of 1,000,000 UI.

4 The Transmitter input impedance shall result in a differential return loss greater than or equal to 10 dB with a differential test input signal no less than 200 mV (peak value, 400 mV differential peak to peak) swing around ground applied to D+ and D- lines and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (i.e., as measured by a Vector Network Analyzer with 50 Ω probes - see Figure 4-25). Note that the series capacitors CTX is optional for the return loss measurement.

5 Measured between 20-80% at Transmitter package pins into a test load as shown in Figure 4-25 for both V_{TX-D+} and $V_{TX-D-.e}$

6 $Z_{TX-DIFF-DC}$ is the small signal resistance of the transmitter measured at a DC operating point that is equivalent to that established by connecting a 100 Ω resistor from D+ and D- while the TX is driving a static logic one or logic zero. Equivalently, this parameter can be derived by measuring the RMS voltage of the TX while transmitting a test pattern into two different differential terminations that are near 100 Ω. Small signal resistance is measured by forcing a small change in differential voltage and dividing this by the corresponding change in current.

Table 4-6: Differential Receiver (RX) Input Specifications

7 No test load is necessarily associated with this value.

8 Specified at the measurement point and measured using the clock recovery function specified in Section 4.3.3.2. The test load in Figure 4-25 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 4-26). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as a reference for the eye diagram.

9 The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total 0.64. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time

value. The RX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as the reference for the eye diagram. This parameter is measured with the equivalent of a zero jitter reference clock. The T_{RX-EYE} measurement is to be met at the target bit error rate. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification is to be met using the compliance pattern at a sample size of 1,000,000 UI.

10 See the PCI Express Jitter and BER white paper for more details on the Rx-Eye measurement.

11 The Receiver input impedance shall result in a differential return loss greater than or equal to 10 dB with a differential test input signal of no less than 200 mV (peak value, 400 mV differential peak to peak) swing around ground applied to D+ and D- lines and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D- line (i.e., as measured by a Vector Network Analyzer with 50 Ω probes - see Figure 4-25). Note that the series capacitors CTX is optional for the return loss measurement.

12 Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.

13 The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 200 mV above the RX ground.

CEM Spec

This section lists specifications notes for all the relevant tables from PCI Express CEM Specification Revision 1.1.

Table 4-7: Add-in Card Transmitter Path Compliance Eye Requirements

1 An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.

2 Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 274 ps for simulation purpose at BER 10^{-12}.

4 $J_{TXA-MEDIAN-to-MAX-JITTER}$ is the maximum median-to-max jitter outlier as defined in the PCI Express Base Specification, Revision 1.1. The sample size for this measurement is 10^6 UI. This value can be increased to 63 ps for simulation purpose at BER 10^{-12}.

5 The values in Table 4-7 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the add-in card (see Figure 4-5). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

Table 4-9: System Board Transmitter Path Compliance Eye Requirements

1 An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.

2 Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.

3 T_{TXS} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 233 ps for simulation purpose at BER 10^{-12}.

4 $J_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-max jitter outlier as defined in the PCI Express Base Specification, Revision 1.1. The sample size for this measurement is 10^6 UI, This value can be increased to 83.5 ps for simulation purpose at BER 10^{-12}.

5 The values in Table 4-9 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the add-in card when mated with a connector (see Figure 4-5). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

Gen 2.0 Spec Notes

Base Spec

This section lists specifications notes for all the relevant tables from PCI Express Base Specification Revision 2.0.

Table 4-9: 2.5 and 5.0 GT/s Transmitter Specifications

1 SSC permits a +0, - 5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz.

2 Measurements at 5.0 GT/s require an oscilloscope with a bandwidth of .12.5 GHz, or equivalent, while measurements made at 2.5 GT/s require a scope with at least 6.2 GHz bandwidth. Measurement at 5.0 GT/s must deconvolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5 GT/s may be measured within 200 mils of Tx device's pins, although deconvolution is recommended. For measurement setup details, refer to Figure 4-23 and Figure 4-24. At least 10^6 UI of data must be acquired.

3 Transmitter jitter is measured by driving the Transmitter under test with a low jitter "idea" clock and connecting the DUT to a reference load.

4 Transmitter raw jitter data must be convolved with a filtering function that represents the worst case CDR tracking BW. 2.5 GT/s and 5.0 GT/s use different filter functions that are defined in Figure 4-21. After the convolution process has been applied, the center of the resulting eye must be determined and used as a reference point for obtaining eye voltage and margins.

5 $V_{TX\text{-}AC\text{-}CM\text{-}PP}$ and $V_{TX\text{-}AC\text{-}CM\text{-}P}$ are defined in Section 4.3.3.7. Measurement is made over at least 10^6 UI.

6 The Tx PLL Bandwidth must lie between the min and max ranges given in the above table. PLL peaking must lie below the value listed above. Note: the PLL B/W extends from zero up to the value(s) specified in the above table.

Table 4-12: 2.5 and 5.0 GT/s Receiver Specifications

1 Receiver eye margins are defined into a 2 x 50 Ω reference load. A Receiver is characterized by driving it with a signal whose characteristics are defined by the parameters specified in Table 4-10 and Table 4-11.

2 The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.

3 Two combinations of PLL BW and peaking are specified at 5.0 GT/s to permit designers to make trade-offs between the two parameters. If the PLL's min BW is .8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's min BW is relaxed to .5.0 MHz, then a tighter peaking value of 1.0 dB must be met. Note: a PLL BW extends from zero up to the value(s) defined as the min or max in the above table. For 2.5 GT/s a single PLL bandwidth and peaking value of 1.5-22 MHz and 3.0 dB are defined.

4 Measurements must be made for both common mode and differential return loss. In both cases the DUT must be powered up and DC isolated, and its D+/D- inputs must be in the low-Z state.

5 The Rx DC Common Mode Impedance must be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly. Compensation of this impedance can start immediately and the Rx Common Mode Impedance (constrained by $RL_{RX\text{-}CM}$ to 50 Ω + 20%) must be within the specified range by the time Detect is entered.

6 Common mode peak voltage is defined by the expression: max{|(Vd+ - Vd-) - V-CMDC|}.

7 $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}NEG}$ and $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ are defined respectively for negative and positive voltages at the input of the Receiver. Transmitter designers need to comprehend the large difference between >0 and <0 Rx impedances when designing Receiver detect circuits.

8 The $L_{RX-SKEW}$ parameter exists to handle repeaters that regenerate Refclk and introduce differing numbers of skips on different Lanes.

CEM Spec

This section lists specifications notes for all the relevant tables from PCI Express CEM Specification Revision 2.0.

Table 4-8: Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s and 3.5 dB De-emphasis

1 An ideal reference clock without jitter is assumed for this specification. All Links are assumed active 5 while generating this eye diagram. The eye diagram requires that CMM pattern (PCI Express Base Specification, Revision 2.0, Section 4.2.8) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.

3 T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 10^6 UI. This calculated eye width at BER 10^{-12} must not exceed T_{TXA}. If the add-in card board uses non-interleaved routing, then crosstalk will be present in the measured data. If the add-in card board uses interleaved routing, then crosstalk will not be present and an adjusted minimum eye width is used.

4 The values in Table 4-8 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

Table 4-10: Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s at 6.0 dB De-emphasis

1 An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern (PCI Express Base Specification, Revision 2.0, Section 4.2.8) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.

3 T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 10^6 UI. This calculated eye width at BER 10^{-12} must not exceed T_{TXA}. If the add-in card board uses non-interleaved routing, then crosstalk will be present in the measured data. If the add-in card board uses interleaved routing, then crosstalk will not be present and an adjusted minimum eye width is used.

4 The values in Table 4-10 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

Table 4-15: System Board Transmitter Path Compliance Eye Requirements at 5 GT/s

1 All Links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern (PCI Express Base Specification, Revision 2.0, Section 4.2.8) is being transmitted during the test using the de-emphasis level that the system board will use in normal operation.

2 Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.

3 T_{TXS} is the minimum eye width. The recommended sample size for the dual port measurement is at least 10^6 UI. The minimum eye opening at BER 10^{-12} is calculated based on the measured data

and must not exceed T_{TXS}. If the system board uses non-interleaved routing, then crosstalk will be present in the measured data. If the system uses interleaved routing, then crosstalk will not be present and an adjusted minimum eye width is used.

4 The values in Table 4-15 are referenced to an ideal 100 Ω differential load at the end of an isolated 2-inch 85 Ω differential trace behind a standard PCI express edge finger. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

Gen 3.0 Spec Notes

Base Spec

This section lists specifications notes for all the relevant tables from PCI Express Base Specification Revision 3.0.

Table 4-18: Transmitter Specifications

1 SSC permits a +0, - 5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz.

2 Measurements at 5.0 GT/s require an oscilloscope with a bandwidth of .12.5 GHz, or equivalent, while measurements made at 2.5 GT/s require a scope with at least 6.2 GHz bandwidth. Measurement at 5.0 GT/s must deconvolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5 GT/s may be measured within 200 mils of Tx device's pins, although deconvolution is recommended. For measurement setup details, refer Figure 4-32 to and Figure 4-33. At least 10^6 UI of data must be acquired.

3 Transmitter jitter is measured by driving the Transmitter under test with a low jitter "ideal" clock and connecting the DUT to a reference load.

4 Transmitter raw jitter data must be convolved with a filtering function that represents the worst case CDR tracking BW. 2.5 GT/s and 5.0 GT/s use different filter functions that are defined in Figure 4-49. After the convolution process has been applied, the center of the resulting eye must be determined and used as a reference point for obtaining eye voltage and margins.

5 $V_{TX-AC-CM-PP}$ and $V_{TX-AC-CM-P}$ are defined in Section 4.3.3.2. Measurement is made over at least 10^6 UI.

6 The Tx PLL Bandwidth must lie between the min and max ranges given in the above table. PLL peaking must lie below the value listed above. Note: the PLL B/W extends from zero up to the value(s) specified in the above table.

7 Measurements are made for both common mode and differential return loss. The DUT must be powered up and DC isolated, and its data+/data- outputs must be in the low-Z state at a static value.

8 A single combination of PLL BW and peaking is specified for 2.5 GT/s implementations. For 5.0 GT/s, two combinations of PLL BW and peaking are specified to permit designers to make a tradeoff between the two parameters. If the PLL's min BW is .8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's min BW is relaxed to .5.0 MHz, then a tighter peaking value of 1.0 dB must be met. In both cases, the max PLL BW is 16 MHz.

9 Reduced swing output, defined by $V_{TX-DIFF-PP-LOW}$ must be implemented as shown in Figure 4-37 with no deemphasis.

10 For 5.0 GT/s, de-emphasis timing jitter must be removed. An additional HPF function must be applied as shown in Figure 4-49. This parameter is measured by accumulating a record length of 10^6 UI while the DUT outputs a compliance pattern. $T_{MIN-PULSE}$ is defined to be nominally 1 UI wide and is bordered on both sides by pulses of the opposite polarity. Refer to Figure 4-38.

11 Root Complex Tx de-emphasis is configured from Upstream controller. Downstream Tx de-emphasis is set via a command, issued at 2.5 GT/s. For details, refer to the appropriate location in Section 4.2.

CEM Spec

This section lists specifications notes for all the relevant tables from PCI Express CEM Specification Revision 3.0.

Table 4-11: Add-in Card Transmitter Path Compliance Eye Requirements at 8.0 GT/s

1 A worst case reference clock with 1 ps RMS jitter is assumed for this revision of the specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (PCI Express Base Specification, Revision 3.0, Section 4.2.10) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). VTXA and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. For lab use, an informative voltage limit (V_{TXA} and V_{TXA_d}) at a BER of 10^{-6} is 46 mV.

3 T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 10^6 UI. This calculated eye width at BER 10^{-12} must not exceed T_{TXA}.

4 The values in Table 4-11 are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of approximately four inches of 85 Ω trace, followed by a second PCI Express connector, followed by approximately 10.8 inches of 85 Ω trace, followed by a reference receiver package all behind a standard PCI Express connector. This channel shall be referenced as the 8.0 GT/s Add-in Card Test Channel. S-parameters for the channel are provided with the specification. Note that additional loss from the measurement set-up must be removed. Note that the Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

Table 4-17: System Board Transmitter Path Compliance Eye Requirements at 5.0 GT/s

1 All Links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern (PCI Express Base Specification, Revision 3.0) is being transmitted during the test using the de-emphasis level that the system board will use in normal operation.

2 Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). VTXS and V_{TXS_d} are minimum differential peak-peak output voltages.

3 T_{TXS} is the minimum eye width. The recommended sample size for the dual port measurement is at least 10^6 UI. The minimum eye opening at BER 10^{-12} is calculated based on the measured data and must not exceed T_{TXS}. If the system board uses non-interleaved routing, then crosstalk will be present in the measured data. If the system uses interleaved routing, then crosstalk will not be present and an adjusted minimum eye width is used.

4 The values in Table 4-17 are referenced to an ideal 100 Ω differential load at the end of an isolated 2-inch 85 Ω differential trace behind a standard PCI express edge finger. This channel shall be referenced as the 5.0 GT/s System Board Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

Table 4-19: System Board Transmitter Path Compliance Eye Requirements at 8.0 GT/s with Ideal Adaptive TX Equalization

1 All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (PCI Express Base Specification, Revision 3.0, Section 4.2.10) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. For lab use, an informative voltage limit (V_{TXS} and $V_{TXS_d)}$ at a BER of 10^{-6} is 46 mV.

3 TTXA is the minimum eye width. The recommended sample size for this measurement is at least 10^6 UI. This calculated eye width at BER 10^{-12} must not exceed T_{TXA}.

4 The values in Table 4-19 are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 4.0 inches of 85 Ω trace, followed by a reference receiver package behind a standard PCI Express edge finger. This channel shall be referenced as the 8.0 GT/s System-Board Test Channel. The s-parameters for the channel are provided with this specification. Note that additional loss from the measurement set-up must be removed. Note that the System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant add-in card.

Gen 4.0 Spec Notes

Base Spec

This section lists specifications notes for all the relevant tables from PCI Express Base Specification Revision 4.0.

Table 8-7: Data Rate Dependent Transmitter Parameters

1 A single combination of PLL BW and peaking is specified for 2.5 GT/s implementations. For other data rates, two combinations of PLL BW and peaking are specified to permit designers to make a trade-off between the two parameters.

2 The Tx PLL Bandwidth must lie between the min and max ranges given in the above table. PLL peaking must lie below the value listed above. Note: the PLL B/W extends from zero up to the value(s) specified in the above table. The PLL BW is defined at the point where its transfer function crosses the -3dB point.

3 See Sections 8.3.3.4 and 0 for measurement details. For 8.0 GT/s and 16.0 GT/s no minimum voltage swing is specified because it is captured by $V_{TX-BOOST-FS}$ and $V_{TX-BOOST-RS}$ parameters.

4 $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0 and 16.0 GT/s that ensures that these parameters are met.

5 The numbers above take into account measurement error. For some Tx package/driver combinations $ps21_{TX}$ may be greater than 0 dB. The channel compliance methodology at 2.5 and 5.0 GT/s assumes the 8.0 GT/s package model.

6 The DUT must be powered up and DC isolated, and its data+/data- outputs must be in the low-Z state at a static value.

7 The reference plane for all parameters at 2.5 and 5.0 GT/s is the package pins.

CEM Spec

This section lists specifications notes for all the relevant tables from PCI Express CEM Specification Revision 4.0.

Table 18: Add-in Card Transmitter Path Pulse Width Jitter at 16.0 GT/s

N/A

Table 4-14: Add-in Card Transmitter Path Compliance Eye Requirements at 16.0 GT/s

1. A worst-case reference clock with 0.7 ps RMS jitter at the receiver of the Add-in Card is assumed for this revision of the specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification, Chapter 4) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-1104 emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}.
3. T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 2×10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}.
4. The values in Table 17 are referenced to an ideal 100 Ohm differential load at the end of an isolated (no crosstalk) test channel consisting of 85 Ohm FR4 trace with an insertion loss of 14 dB at Nyquist., followed by a root reference package all behind a standard PCI Express connector. This channel shall be referenced as the 16.0 GT/s Add-in Card Test Channel. S-parameters for the channel provided with the specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

Table 4-27: System Board Transmitter Path Compliance Eye Requirements at 16.0 GT/s with Ideal Adaptive TX Equalization

1. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification, Chapter 4) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. For lab use, an informative voltage limit (V_{TXS} and V_{TXS_d}) at a BER of 10^{-6} is 46 mV.
3. T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 10^6 UI. This calculated eye width at BER 10^{-12} must not exceed T_{TXA}.
4. The values in Table 4 25 are referenced to an ideal 100 Ohm differential load at the end of an isolated (no crosstalk) test channel consisting of 5 dB of 85 Ohm trace, followed by a reference receiver package behind a standard PCI Express edge-finger. This channel shall be referenced as the 16.0 GT/s System-Board Test Channel. The s-parameters for the channel are provided with this specification. Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant add-in card.

Appendices

KEYSIGHT TECHNOLOGIES

A Calibrating the Digital Storage Oscilloscope

Required Equipment for Calibration / 544
Internal Calibration / 545
Cable and Probe Calibration / 550
Channel-to-Channel De-skew / 559

This appendix describes the Keysight digital storage oscilloscope calibration procedures.

Required Equipment for Calibration

To calibrate the oscilloscope in preparation for running the PCI Express automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, qty = 2, (provided with the Keysight Infiniium oscilloscope).
- Calibration cable.
- BNC shorting cap.

Figure 1 below shows a drawing of the above connector items.

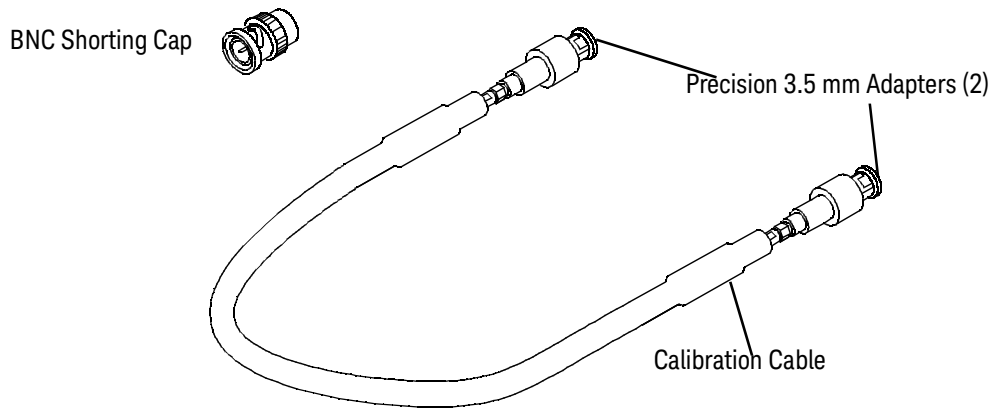


Figure 1 Accessories Provided with the Keysight Oscilloscope

- 50-ohm Coax Cable with SMA Male Connectors – 24-inch or less RG316/U or similar, qty = 2, matched length.
- SMA T-adapter.
- BNC to SMA male adapter, qty = 1.

Internal Calibration

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Keysight oscilloscope, this is referred to as Calibration. This Calibration will take about 20 minutes. Perform the following steps:

1 Set up the oscilloscope with the following steps:
   a Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.
   b If SigTest is being used on the oscilloscope, then connect a second monitor to the VGA connector located near the LAN port, on the rear of the oscilloscope.
   c Plug in the power cord.
   d Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.
   e Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 3 below.

2 Locate and prepare the accessories that will be required for the internal calibration:
   a Locate the BNC shorting cap.
   b Locate the calibration cable.
   c Locate the two Keysight precision SMA/BNC adapters.
   d Attach one SMA adapter to one end of the calibration cable - hand tighten snugly.
   e Attach the other SMA adapter to the other end of the calibration cable - hand tighten snugly.

3 Referring to Figure 2 below, perform the following steps:
   a Click on the Utilities>Calibration menu to open the Calibration window.

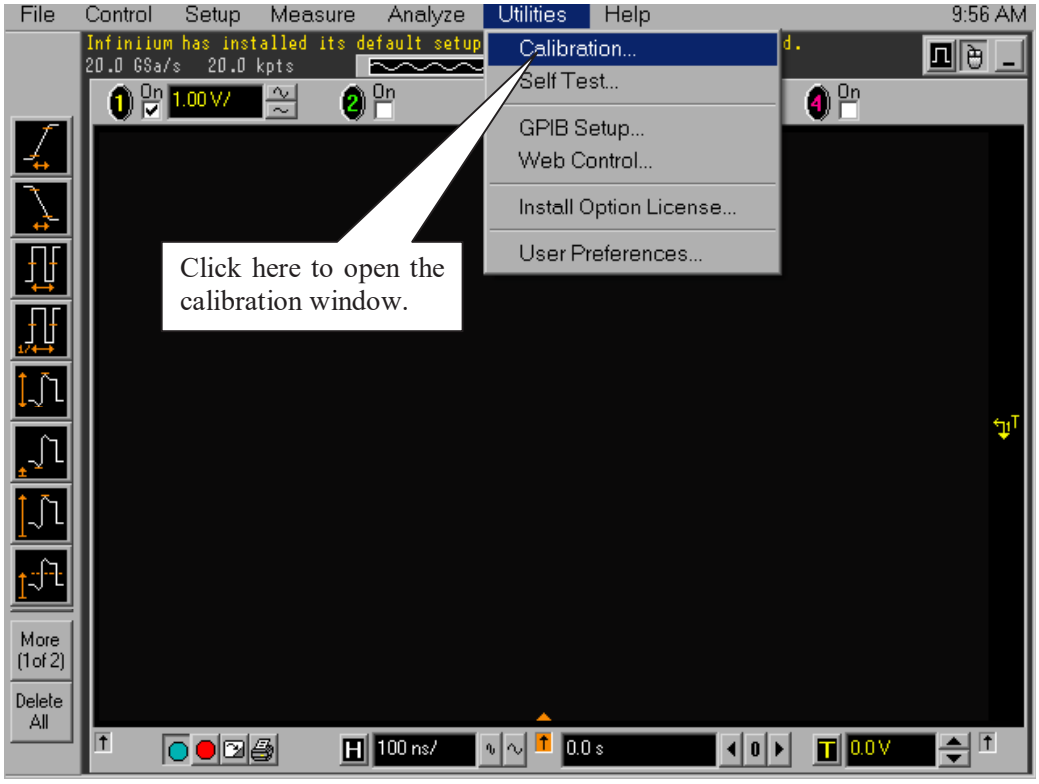


Figure 2 Accessing the Calibration Menu.

4 Referring to Figure 3 below, perform the following steps to start the calibration:

a Uncheck the Cal Memory Protect checkbox.

b Click the Start button to begin the calibration.

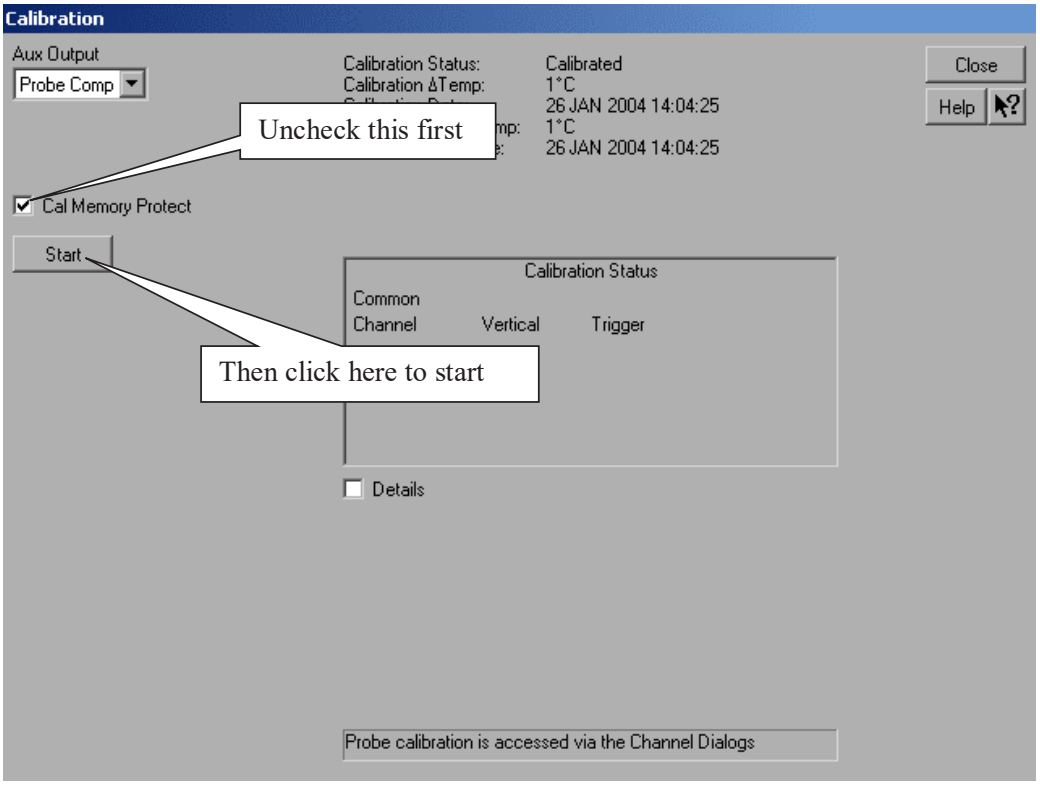


Figure 3 Oscilloscope Calibration Menu.

5 Follow the on-screen instructions:

a You will be prompted to disconnect everything from all the inputs, click the OK button.

b Then, you will be prompted to connect BNC shorting cap to a specified input. Install the BNC shorting cap by pressing it on the specified input BNC, and turning right. Click the OK button after moving the BNC cap to each specified channel.

c Then you will be prompted to connect the calibration cable with SMA adapters between the Aux Out and a specified input, as shown in the example in Figure 4 below. Install the SMA adapter by pressing it on input BNC, and hand tightening the outer ring turning right. Click the OK button after connecting the cable as prompted.

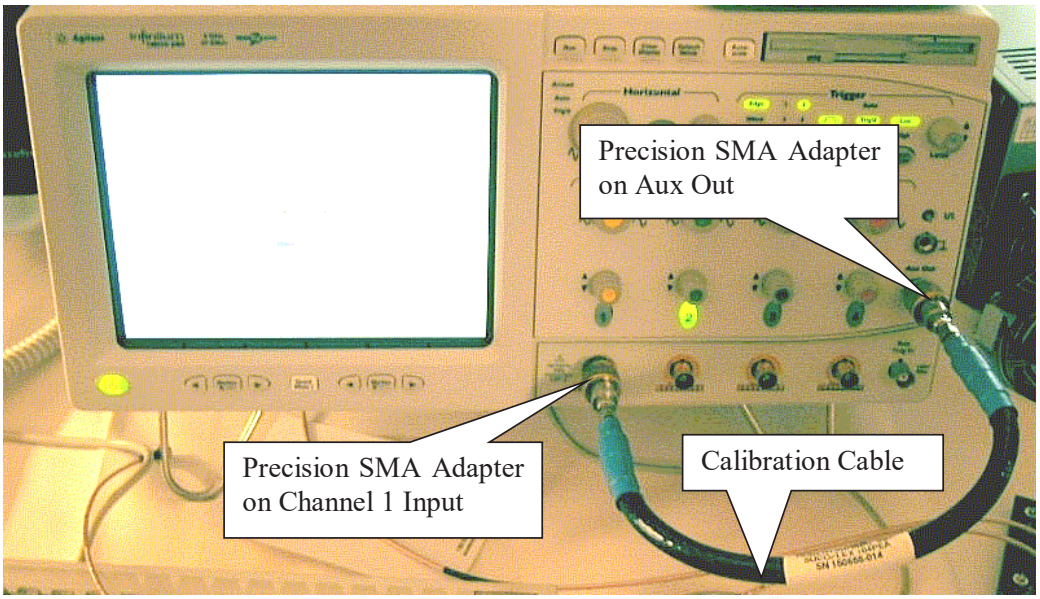


Figure 4 Calibration Cable Connection Example.

d Early during the calibration of channel 1, you will be prompted to perform a Time Scale Calibration, as shown in Figure 5 below.

e Click on the Default button to continue the calibration, using the Factory default calibration factors.

f When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the OK button to close this window.

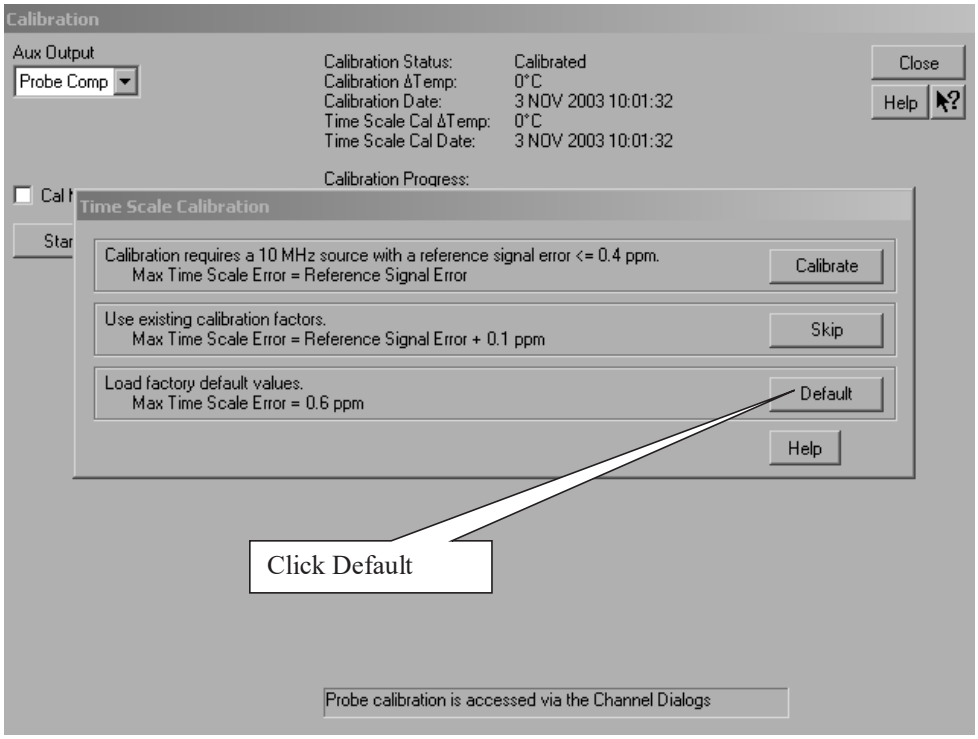


Figure 5 Time Scale Calibration Menu.

6 Referring to Figure 6 below, perform the following steps:

a Confirm that the Vertical and Trigger Calibration Status for all Channels passed.

b Click the Close button to close the calibration window.

c The internal calibration is completed.

d Read NOTE below.

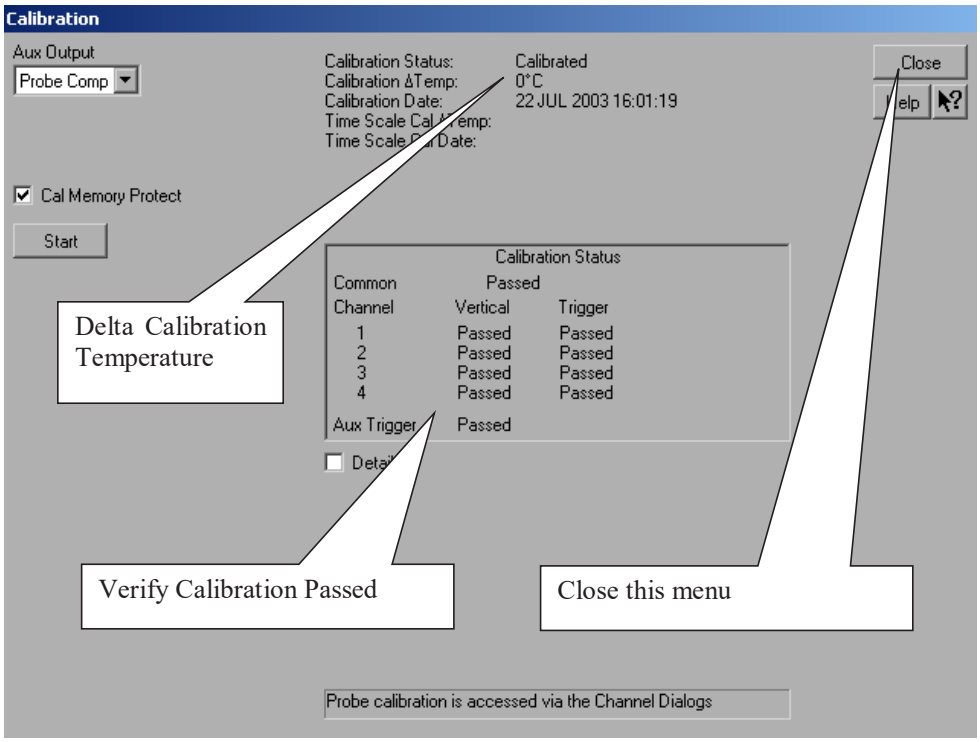


Figure 6 Calibration Status Screen.

NOTE

These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

Cable and Probe Calibration

Perform a 50-ohm direct-coupled input calibration for the SMA interface of channel 1 and channel 3. This calibration compensates for gain, offset, and skew errors in cables and probes. Perform the following steps.

1 Referring to the Figure 7 below, perform the following steps:

a Locate and connect one of the Keysight precision SMA adapters to the Channel 1 oscilloscope input.

b Locate and connect the other Keysight precision SMA adapter to the Channel 3 oscilloscope input.

c Locate and connect one end of one of the RG-316 cables to the SMA adapter on Channel 1.

d Locate and connect one end of the other RG-316 cable to the SMA adapter on Channel 3.

e Locate and connect the non-Keysight SMA/BNC adapter to the Aux Out BNC on the oscilloscope.

f Connect the other end of the cable attached to Channel 1 to the SMA adapter on the Aux Out.

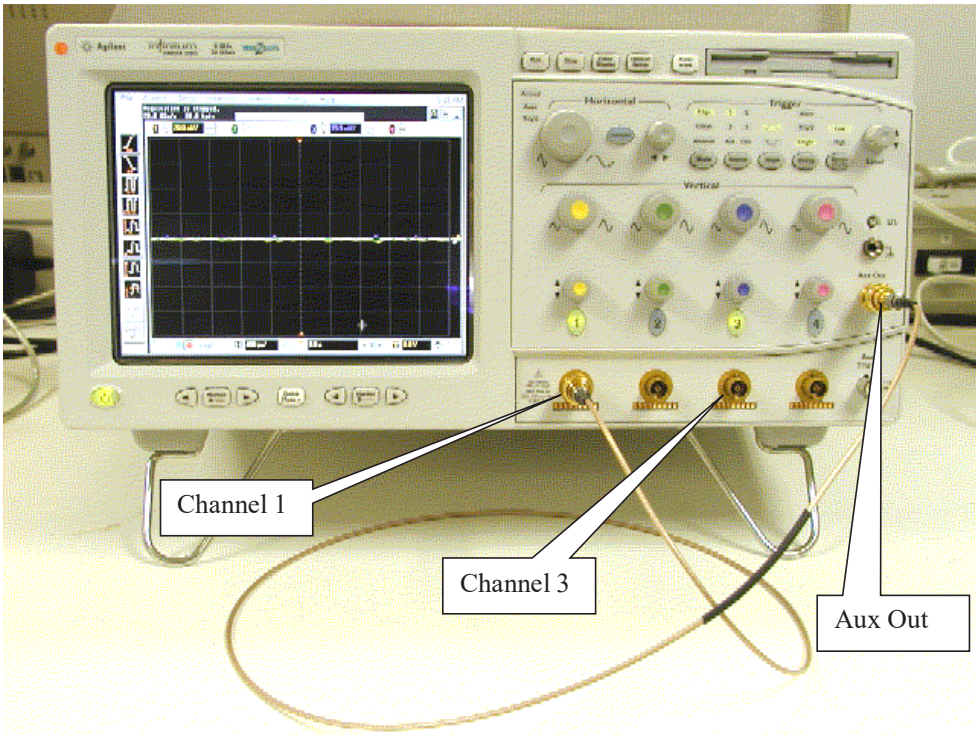


Figure 7 Vertical Input Calibration Connections (Cable on Channel 3 not shown).

2 Referring to Figure 8 below, perform the following steps:

a Click on the Setup>Channel 1 menu to open the Channel Setup window.

b Click the Probes button in the Channel Setup window, to open the Probe Setup window.

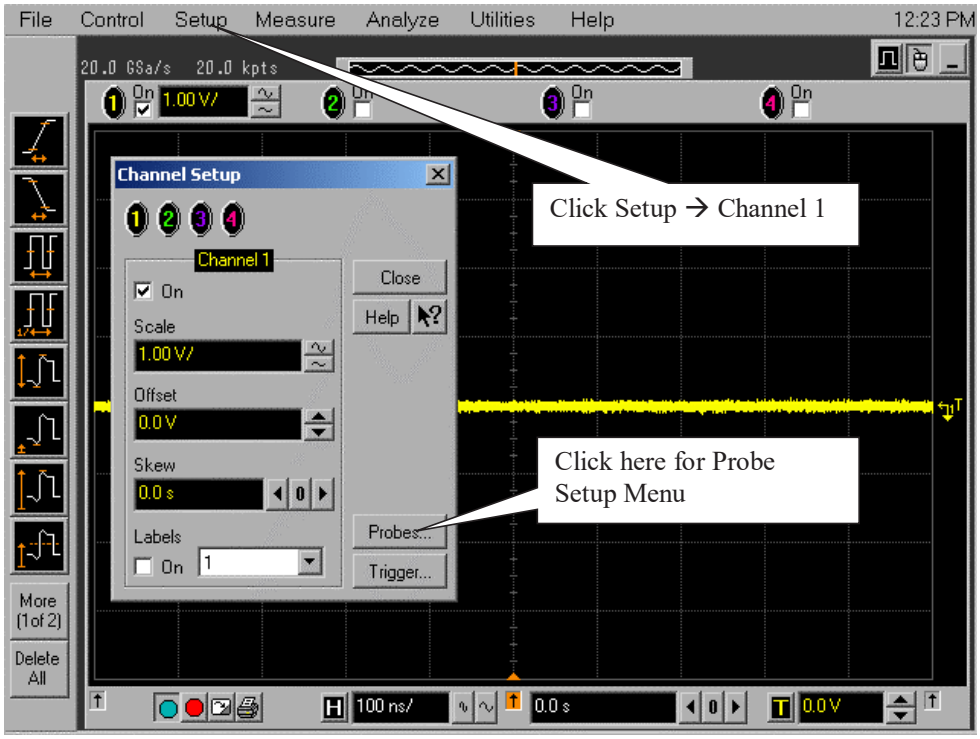


Figure 8 Channel Setup Window.

3 Referring to Figure 9 below, perform the following steps:

a Click the Configure Probing System button, and then click on User Defined Probes.

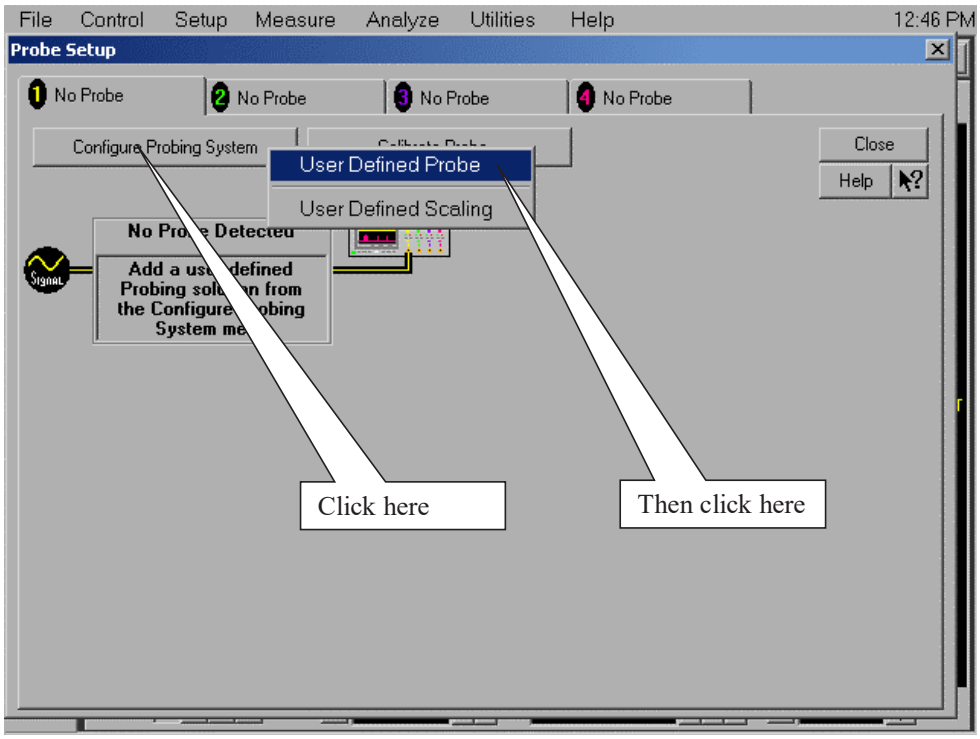


Figure 9 Probe Setup Window.

4 Referring to Figure 10 below, perform the following steps:

a Click on the Calibrate Probe button to open the Probe Calibration window.

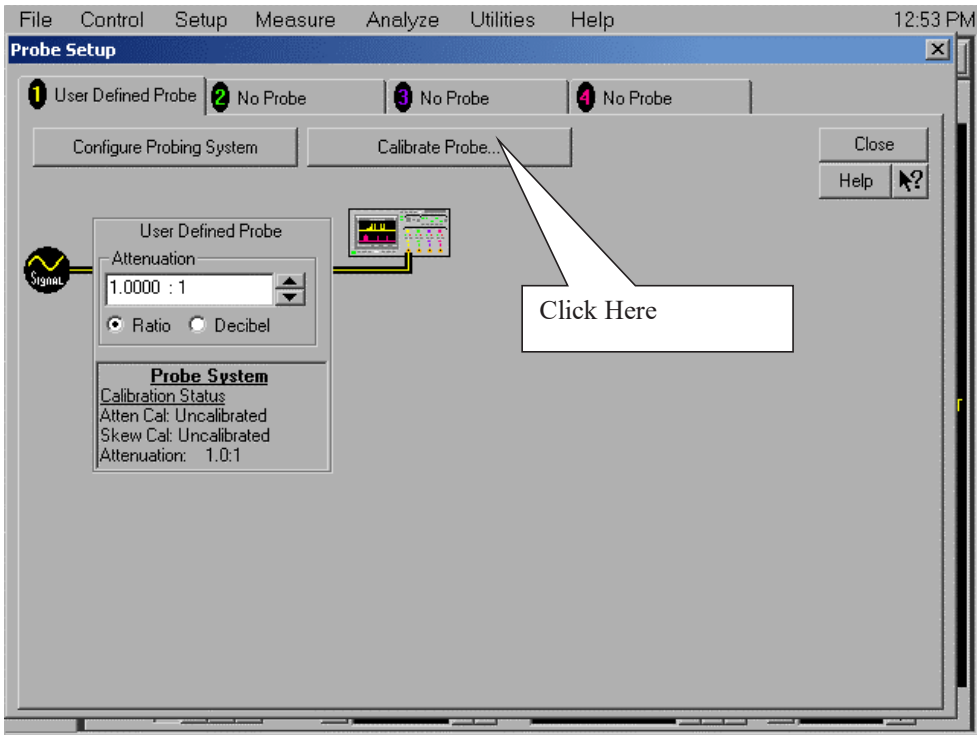


Figure 10 User Defined Probe Window.

5 Referring to Figure 11 below, perform the following steps:

a Select the Calibrated Atten/Offset Radio Button

b Click the Start Atten/Offset Calibration Button to open the Calibration window.

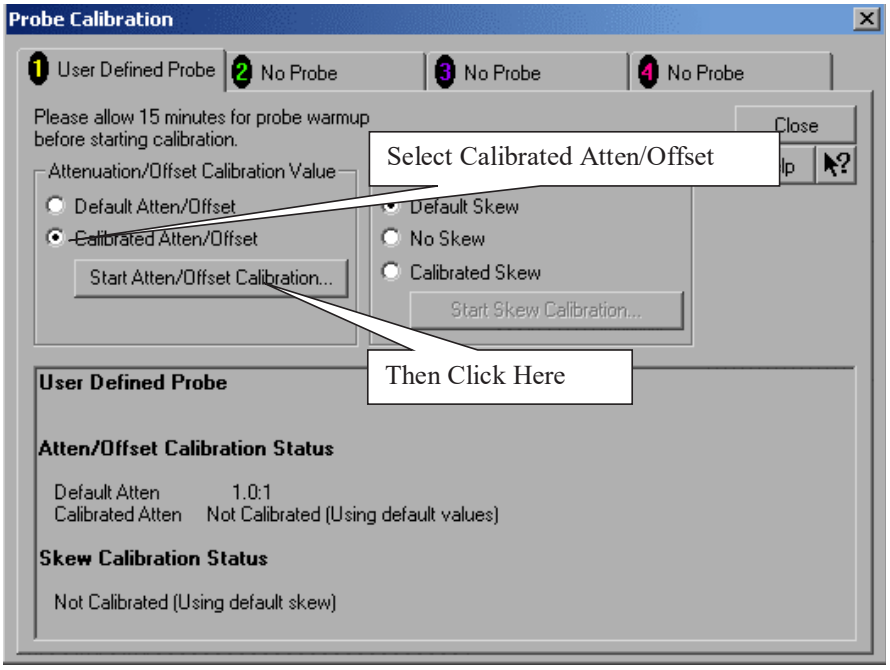


Figure 11 Probe Calibration Window.

6 Referring to Figure 12 shown below, perform the following steps:

a Ignore the instructions shown in the dialog box.

b Click the OK button on the Calibration window.

c The calibration should complete in about 10 seconds.

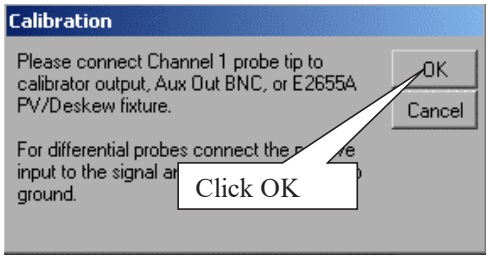


Figure 12 Calibration Window.

7 Referring to Figure 13 below, perform the following steps:

a Click OK to close the Probe Calibration Done window.

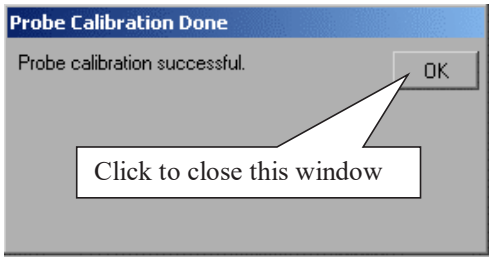


Figure 13 Probe Calibration Done Window.

8 Referring to Figure 14 below, perform the following steps:

a Select the Calibrated Skew Radio button in the Probe Calibration window

b Click the Start Skew Calibration button

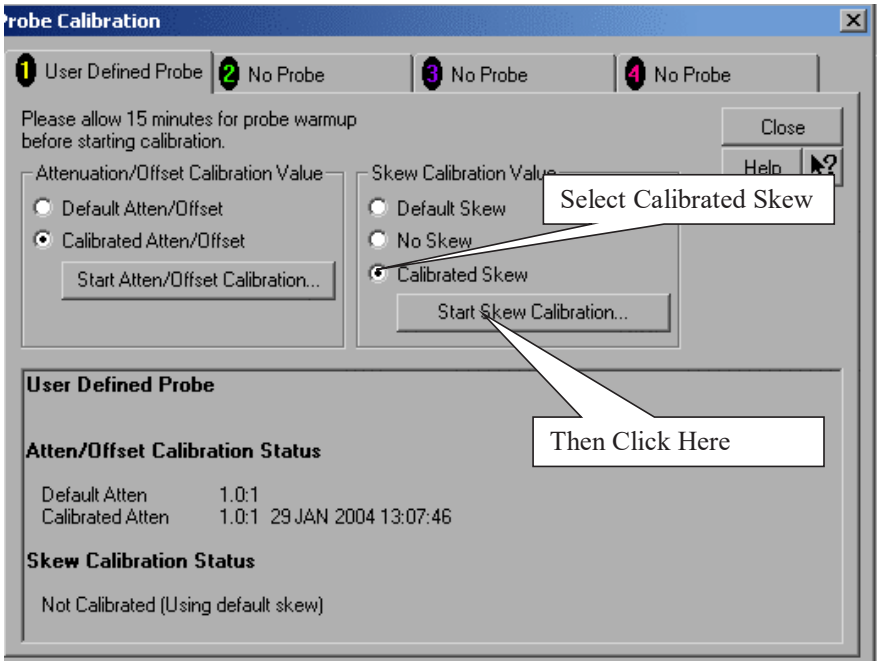


Figure 14 Probe Calibration Window.

9 Referring to Figure 15 shown below, perform the following steps:

a Ignore the instructions shown in the dialog box.

b Click the OK button on the Calibration window.

c The calibration should complete in about 10 seconds.

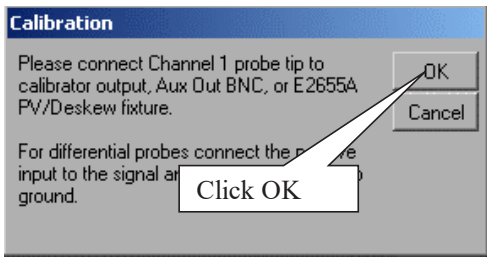


Figure 15 Calibration Window.

10 Referring to Figure 16 below, perform the following steps:

a Click OK to close the Probe Calibration Done window.

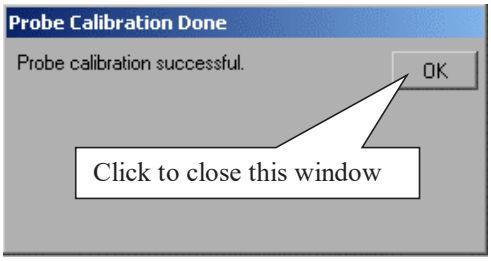


Figure 16 Calibration Window.

11 Referring to Figure 17 below, perform the following steps:

a Click the Close button to close this window.

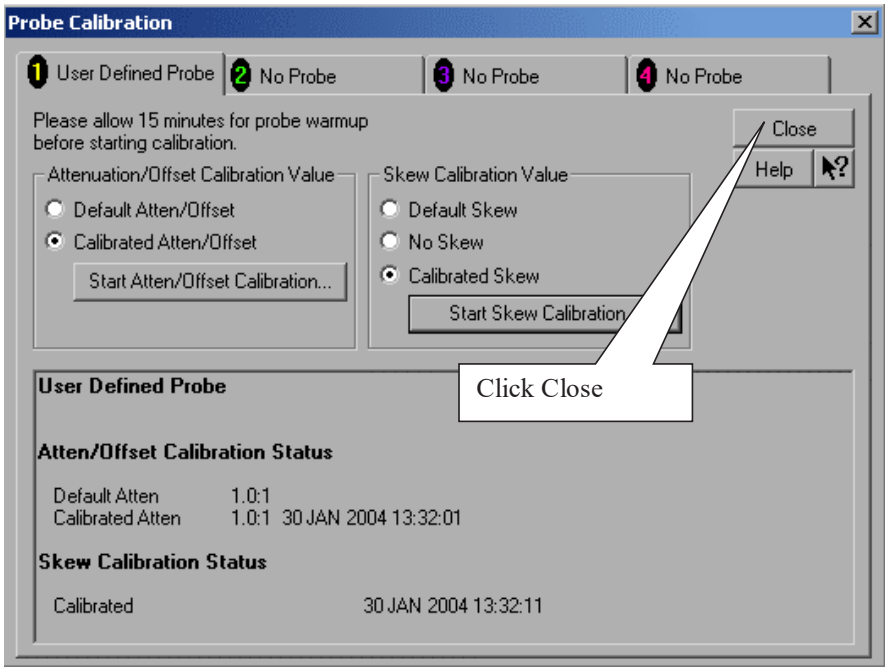


Figure 17 Calibration Window.

12 Referring to Figure 18 below, perform the following steps:

a Click on the Channel 3 tab.

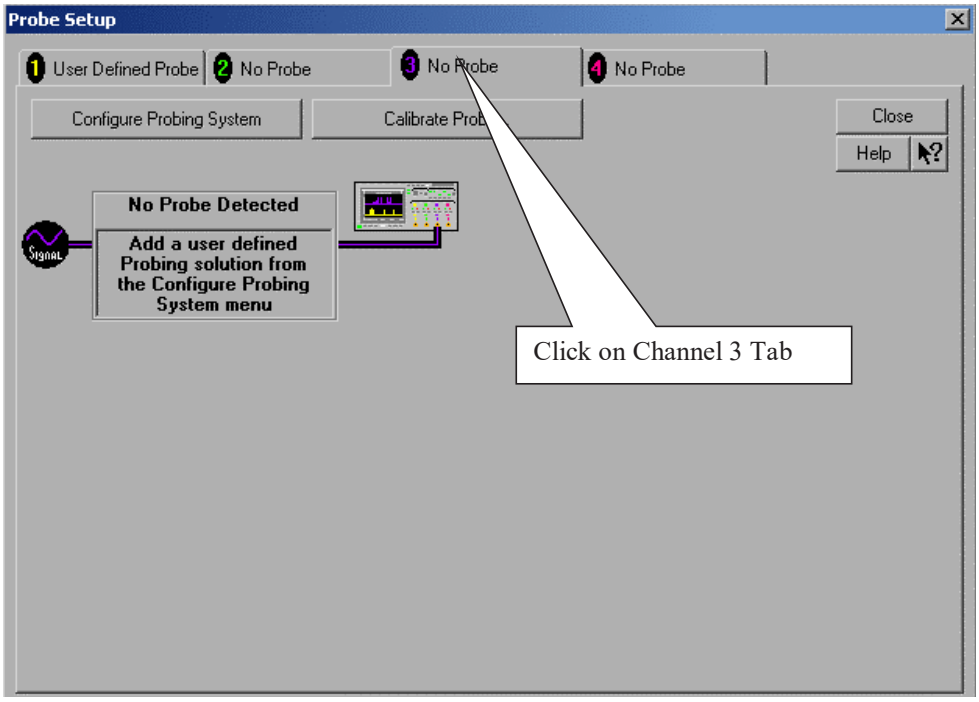


Figure 18 Calibration Window.

13 Referring to Figure 7 on page 550, perform the following steps:

a Disconnect the RG-316 cable connected to the SMA adapter on the Aux Out.

b Connect the other end of the RG-316 cable connected to the SMA adapter on Channel 3, to the SMA adapter on the Aux Out.

14 Repeat steps 3 through 11 of this section to calibrate the cable on Channel 3.

15 Click the Close button on the Probe Setup window (Figure 18) to close this window.

16 Click the Close button on the Channel Setup window (Figure 8 on page 551) to close this window.

17 The Cable and Probe calibration is complete.

18 Read the NOTE below.

NOTE

Each cable is now calibrated for the oscilloscope channel it is connected to. Do not switch cables between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the cables be labeled with the channel they were calibrated for.

Channel-to-Channel De-skew

This procedure ensures that the timing skew errors between channel 1 and channel 3 are minimized. Perform the following steps:

1 Referring to Figure 19 below, perform the following steps:

a Do not disconnect the RG-316 cables from either the Channel 1 or Channel 3 SMA adapters.

b If not already installed, install the non-Keysight SMA adapter on the oscilloscope Aux Out.

c Disconnect any cable connected to the SMA adapter on the Aux Out.

d Locate and connect the middle branch of the SMA Tee to the SMA adapter on the Aux Out BNC.

e Connect the far end of the cable from the Channel 1 SMA adapter, to one branch of the SMA Tee on the Aux Out.

f Connect the far end of the cable from the Channel 3 SMA adapter, to the other branch of the SMA Tee on the Aux Out.

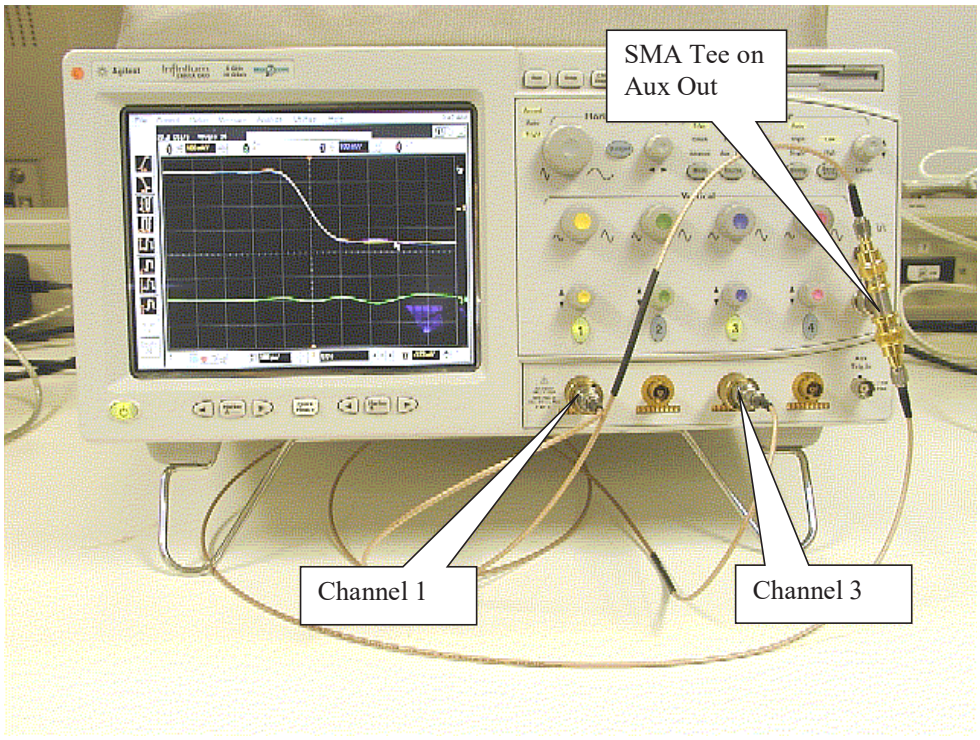


Figure 19 De-skew Connection.

2 Referring to Figure 20 below, perform the following steps:

a Select the File>Load>Setup menu to open the Load Setup window.

b Navigate to the directory location that contains the INF_SMA_Deskew.set setup file. If the setup file is not available, it can be created by following the instructions in Appendix C, “INF_SMA_Deskew.set Setup File Details.

c Select the INF_SMA_Deskew.set setup file by clicking on it.

d Click the Load button to configure the oscilloscope from this setup file.

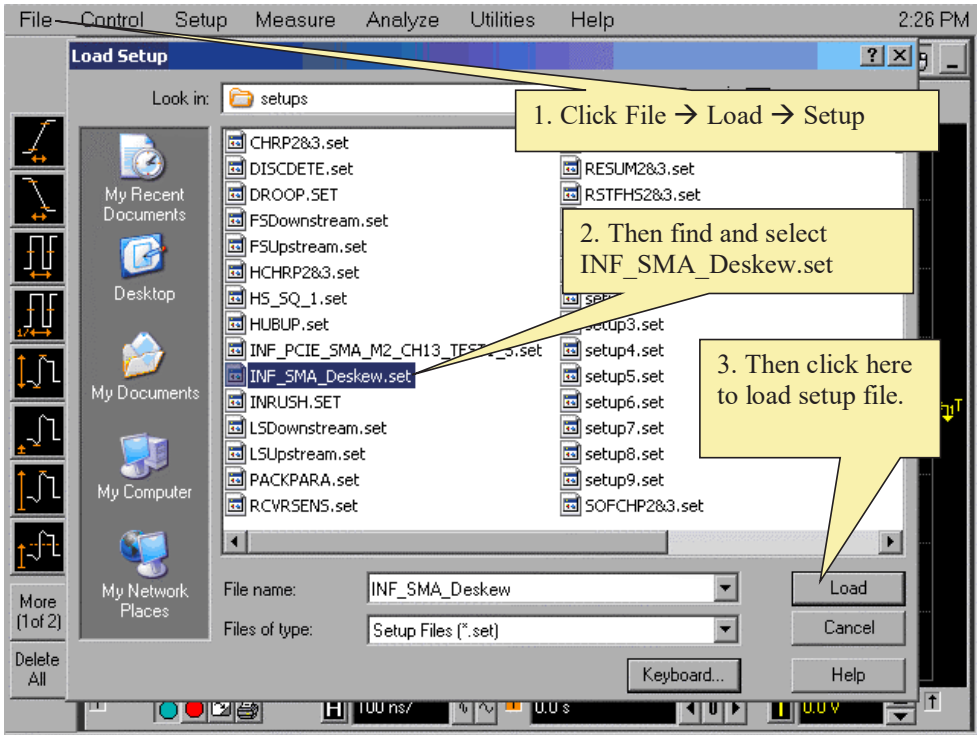


Figure 20 Load De-skew Setup.

The oscilloscope display should look similar to Figure 21 below. A falling edge of the square wave is shown in a 200 ps/div horizontal scale. The upper portion of the screen shows channel 1 (yellow trace) and channel 3 (purple trace) superimposed on one another. The lower portion of the screen is the differential signal (green trace) of channel 1 minus channel 3. The top two traces provide for visual inspection of relative time skew between the two channels. The bottom trace provides for visual presentation of unwanted differential mode signal resulted from relative channel skew (and to a much lesser extent from other inevitable channel mismatch parameters like gain and non-linearity). Figure 21 is an example of exaggerated skew between channel 1 and channel 3, measured to be about 50 ps with the cursor.

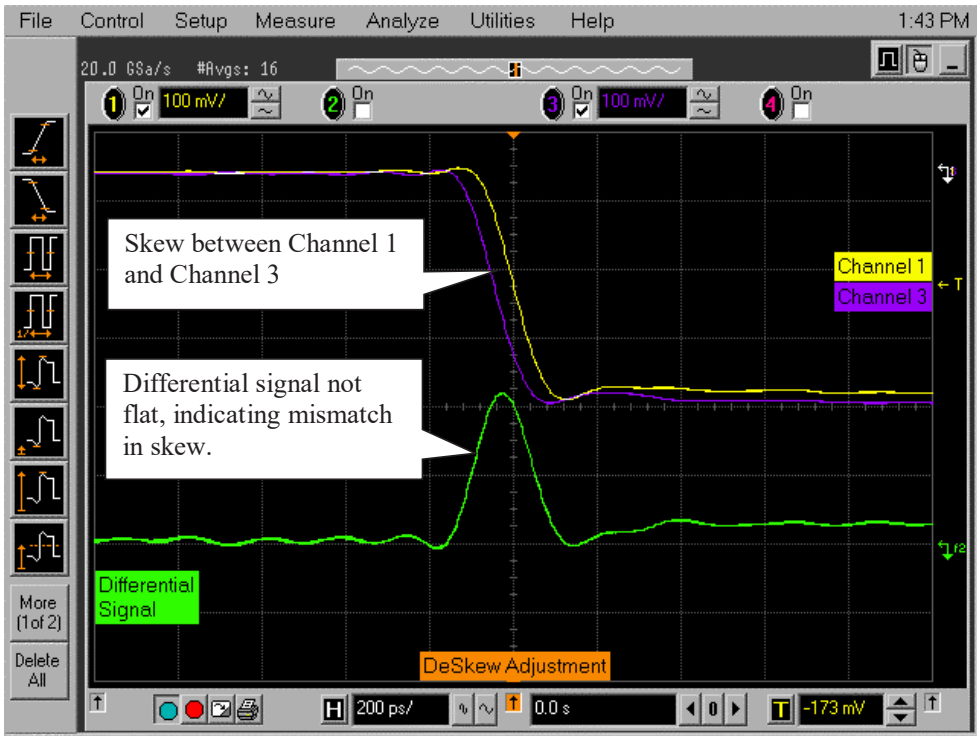


Figure 21 Channel Skew.

Figure 22 below shows the desired effect of no skew between the cables. Note that the channel 1 (yellow trace), channel 3 (purple trace) traces overlap, and the differential signal (green trace) is flat. If this is not the case, then perform the following steps to reduce the skew between channels 1 and 3.

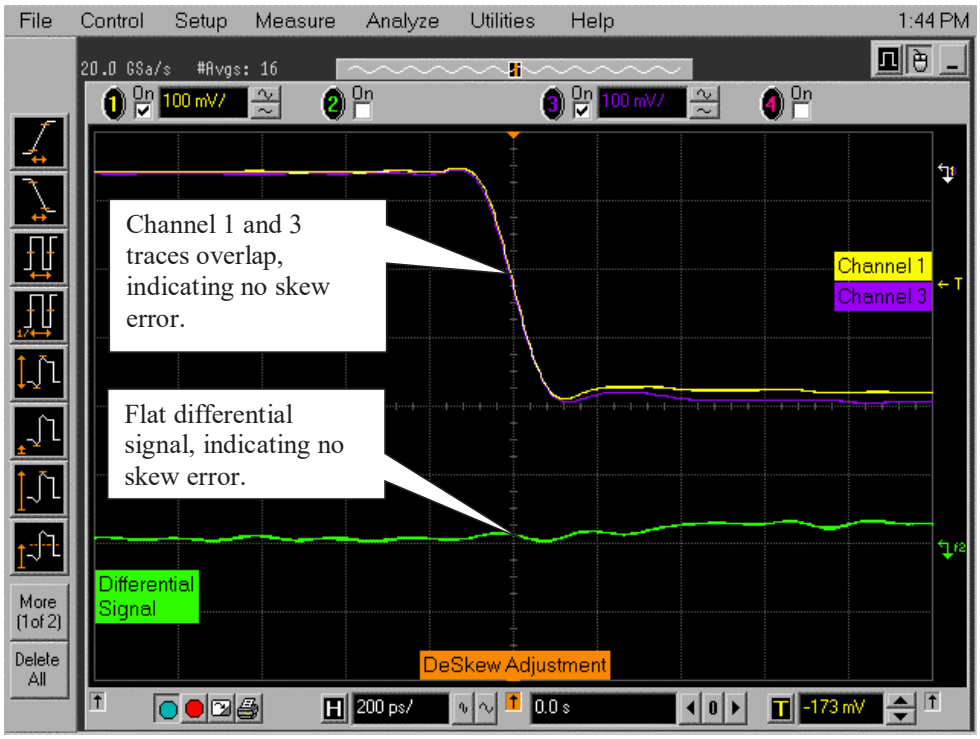


Figure 22 Skew Minimized.

3 Referring to Figure 23, perform the following steps to de-skew the channels:

a Click on the Setup>Channel 1 menu to open the Channel Setup window.

b Move the Channel Setup window to the left so you can see the traces.

c Adjust the Skew by clicking on the < or > arrows, to achieve the flattest response on the differential signal (green trace).

d Click the Close button on the Channel Setup window to close it.

e The de-skew operation is complete.

f Disconnect the cables from the Tee on the Aux Out BNC. Leave the cables connected to the Channel 1 and Channel 3 inputs.

g Read the NOTE below.

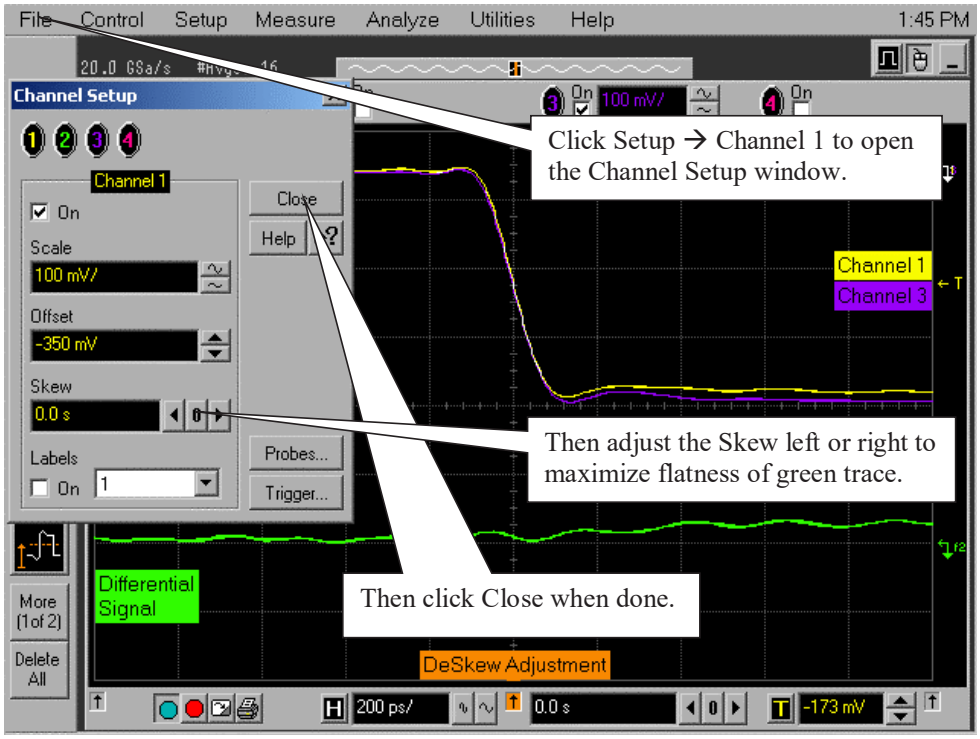


Figure 23 De-skewing Procedure.

NOTE

Each cable is now calibrated for the oscilloscope channel it is connected to. Do not switch cables between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the cables be labeled with the channel they were calibrated for.

B InfiniiMax Probing Options



Figure 24 1134A/B InfiniiMax Probe Amplifier



Figure 25 1134A/B Probe Amplifier and E2675A/B Differential Browser Probe Head

Keysight recommends 1169A/B or 1134A/B probe amplifiers. PCI Express 2.0 requires minimum of 1169A/B probe amplifiers. Keysight also recommends either the E2677A/B differential solder-in probe head or the E2675A/B differential browser probe head.

The differential solder-in probe head (E2677A/B) is recommended for highest signal fidelity while the differential browser probe head (E2675A/B) may be used for probing convenience.



Figure 26 Recommended Probe Heads for the PCI Express Testing

Table 1 Probe Head Characteristics

Probe Head	Model Number	Differential Measurement (BW, input C, input R)	Single-Ended Measurement (BW, input C, input R)
Differential browser	E2675A/B	6 GHz, 0.32 pF, 50 kOhm	6 GHz, 0.57 pF, 25 kOhm
Differential solder-in	E2677A/B	7 GHz / 12 GHz, 0.27 pF, 50 kOhm	7 GHz / 12GHz, 0.44 pF, 25 kOhm
Differential socket	E2678A/B	7 GHz / 12 GHz, 0.34 pF, 50 kOhm	7 GHz / 12 GHz, 0.56 pF, 25 kOhm

C INF_SMA_Deskew.set Setup File Details

If the INF_SMA_Deskew.set file is not available, you can create it by following these instructions. Start from a default setup by pressing the Default Setup key on the front panel. Then configure the following settings:

Acquisition	Averaging on number of averages 16 Interpolation on
Channel 1	Scale 100.0 mV/ Offset –350mV Coupling DC Impedance 50 Ohms
Channel 3	Turn Channel On; Scale 100.0 mV/ Offset –350m V Coupling DC Impedance 50 Ohms
Time base	Scale 200 ps/sec
Trigger	Trigger level –173mV Slope falling
Function 2	Turn on and configure for channel 1 subtract channel 3, Vertical scale 50 mV/ Offset 100.000 mV

NOTE INF_SMA_Deskew.set system location:
C:\Program Files\Keysight\Infiniium\Apps\PCIExpress\app\setups

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