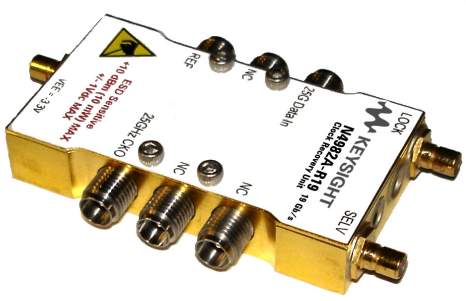
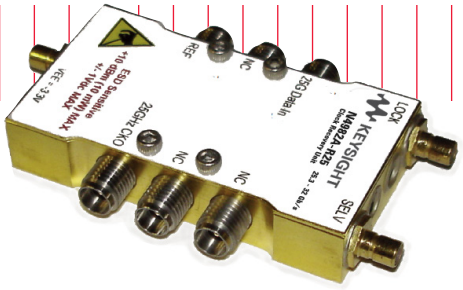
Keysight N4982A

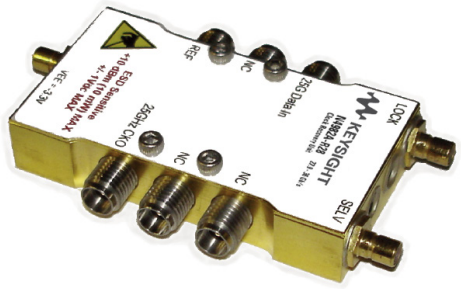
Clock Recovery Unit

For 100GbE, Fiberchannel, Infiniband, and 40G or SONET/SDH Applications

Data Sheet







KEYSIGHT TECHNOLOGIES

Unlocking Measurement Insights

N4982A Clock Recovery Units

- Low jitter output clock
- Low power dissipation
- Precision connectors
- Excellent signal quality
- Single low voltage DC supply

Compliant with RoHS WEE requirements

Description

The Keysight Technologies, Inc. N4982A series of clock recovery units (CRU) cover data rates from 19 to 36 Gb/s and 39.8 to 44 Gb/s with three different model options. The CRU modules utilize silicon germanium (SiGe) technology and offer both small size, and low power consumption.

Applications

The N4982A CRU modules can be used to extract a low jitter clock for 40G and 100G applications such as IEEE 802.3, OIF/CEI 25/28G, 32G Fiberchannel, 25G Infiniband, etc. The CRU's have sufficient bandwidth to operate both at common base rates, e.g. 25.78125 Gb/s, as well as in applications that require added bandwidth for forward error correction (FEC), e.g. 27.95, 30.9375 Gb/s. Broadband test systems will benefit from the low power dissipation, precision connectors and excellent signal quality.

Specifications at 33 °C case temperature

Parameter	Model-option number				Units
	N4982A-R19		N4982A-R25	N4982A-R28	
Data input					
Bit rate	19.0 to 26.0	39.8 to 44.0	25.3 to 32.0	27.9 to 36.0	Gb/s
Amplitude	100 to 1400	150 to 1400	50 to 1400	50 to 1400	mV p-p
Reference clock input					
Type	Half-rate	Quarter-rate	Quarter-rate	Quarter-rate	
Frequency	9.5 to 13.0	9.95 to 11.0	6.325 to 8.0	6.975 to 9.0	GHz
Amplitude	200 to 1400		50 to 1400	50 to 1400	mV p-p
Clock output					
Type	Full-rate	Half-rate	Half-rate	Half-rate	
Frequency	19.0 to 26.0	19.9 to 22.0	12.65 to 16.0	13.95 to 18.0	GHz
Amplitude (typical)	> 150		> 320	> 150	mV p-p
Jitter RMS (nominal)	0.5		0.5	0.5	ps
DC supply					
Voltage	–3.6 V dc		–3.3 V dc	–3.3 V dc	V
Current (nominal)	270		220	220	mA

Table 1.

Absolute maximum ratings

Parameter	Value
Supply voltage (VEE)	–3.8 V
Control voltage applied to SELV and LOCk	Max: +0.05 V Min: VEE - 0.05 V
Ref input power (REF)	+10 dBm
DC input voltage to DIN, REF and CKO	±1 V
Operating Temperature	0 to +70 °C
Storage Temperature	–50 to +125 °C

Table 2.

Performance Data N4982A-R19

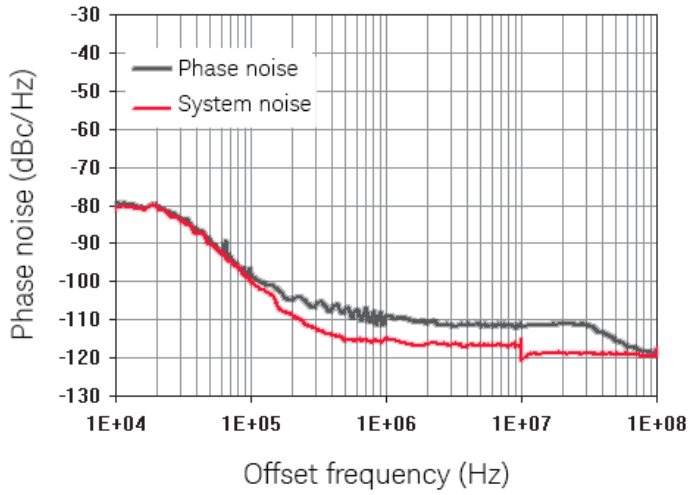


Figure 1. Phase noise of CKO at 25.78125 GHz locked to 2e31, 25.78125 Gb/s data

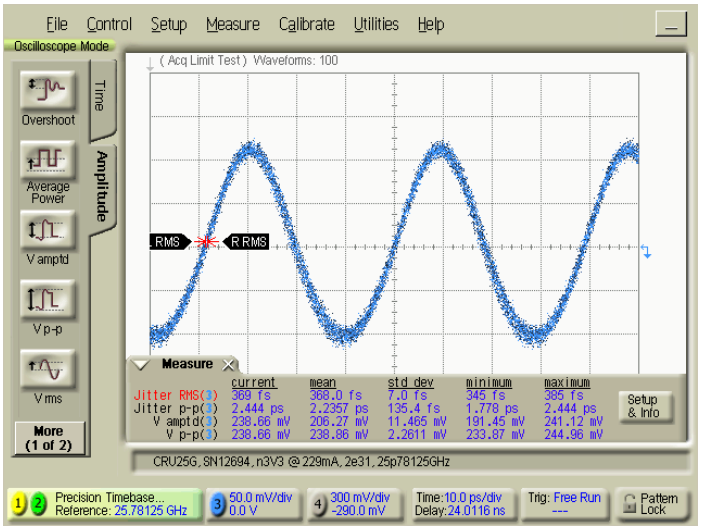


Figure 2. 25.78125 GHz clock output locked to 2e31, 25.78125 Gb/s data

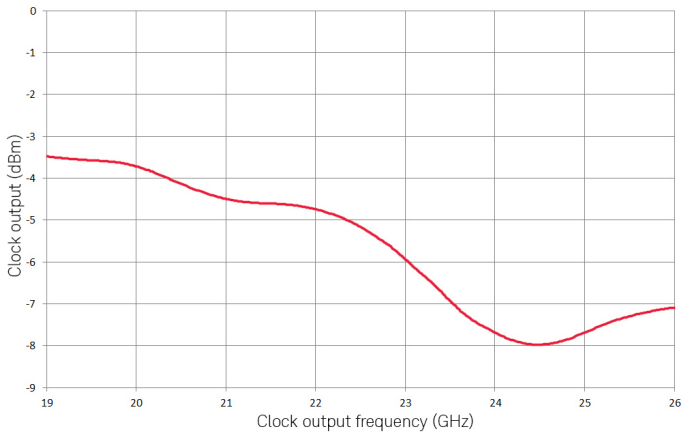


Figure 3. Output power vs frequency

Performance Data N4982A-R25

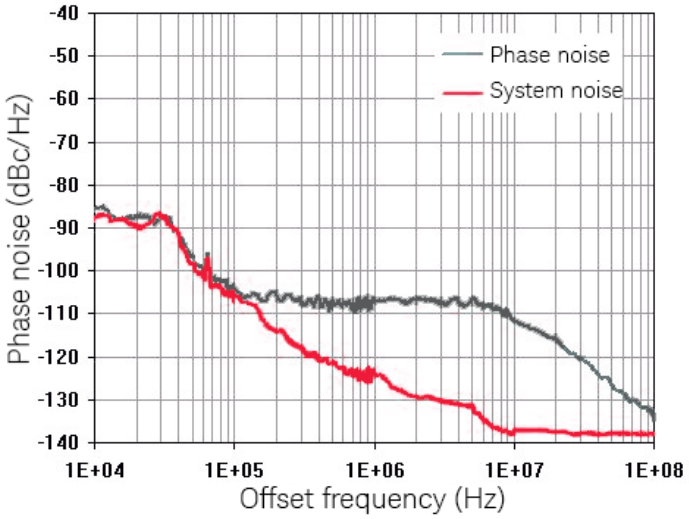


Figure 4. Phase noise of CKO at 13.975 GHz Locked to 2 e15, 27.95 Gb/s data

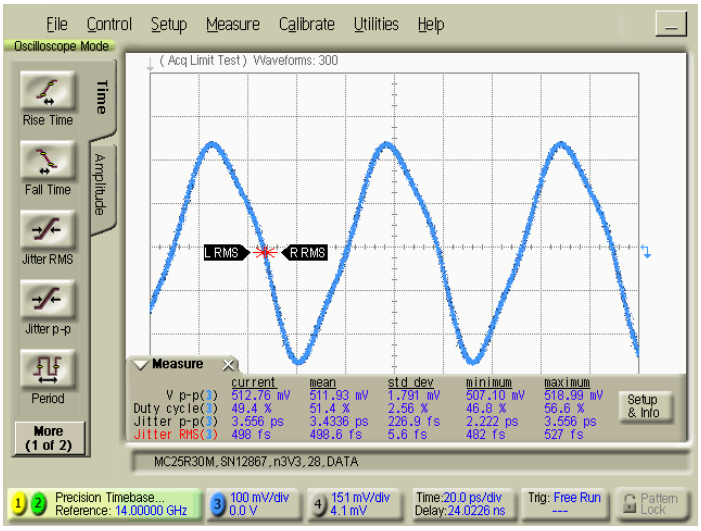


Figure 5. 13.975 GHz clock output locked to 2 e15, 27.95 Gb/s data

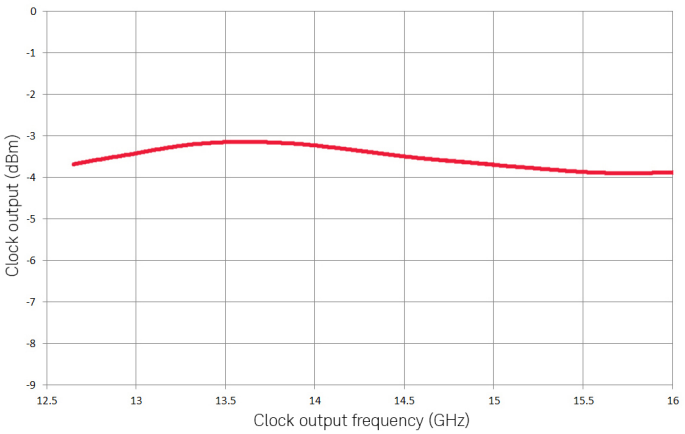


Figure 6. Output vs frequency

Performance Data N4982A-R28

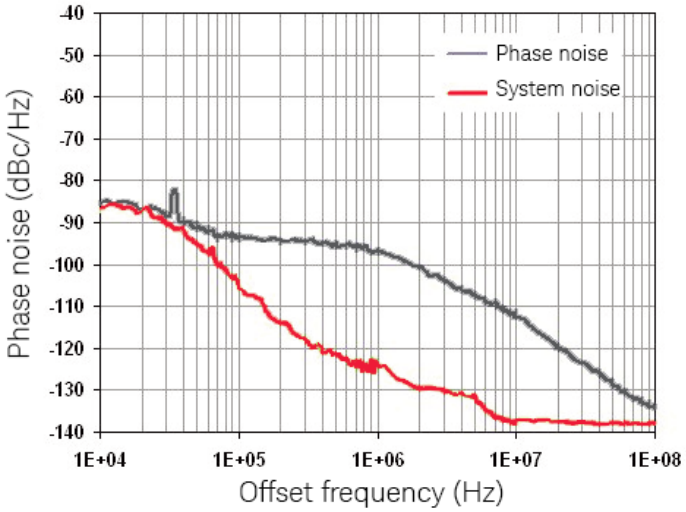


Figure 7. Phase noise of CKO at 14.0 GHz locked to 2e15, 28.0 Gb/s data

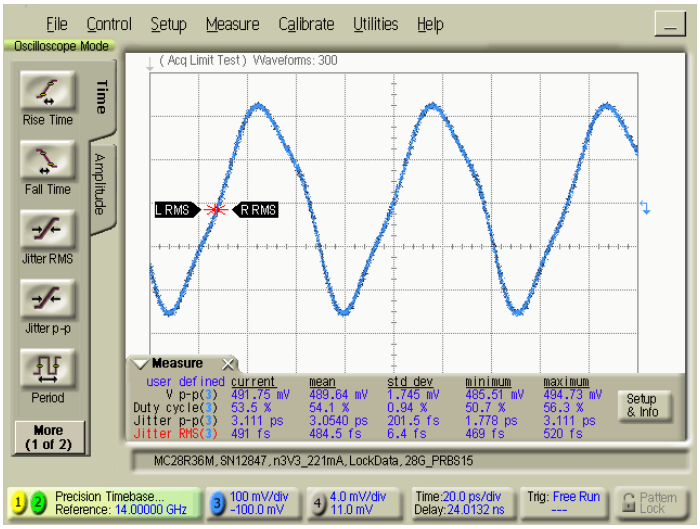


Figure 8. 14.0 GHz clock output locked to 2e15, 28.0 Gb/s data

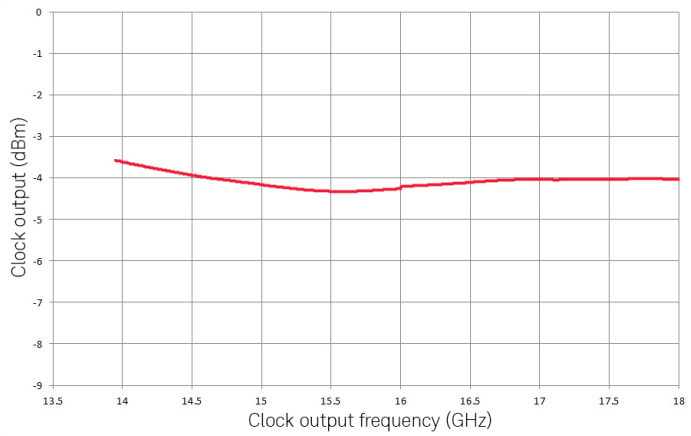


Figure 9. Output power vs frequency

N4982A Functional Block Diagram

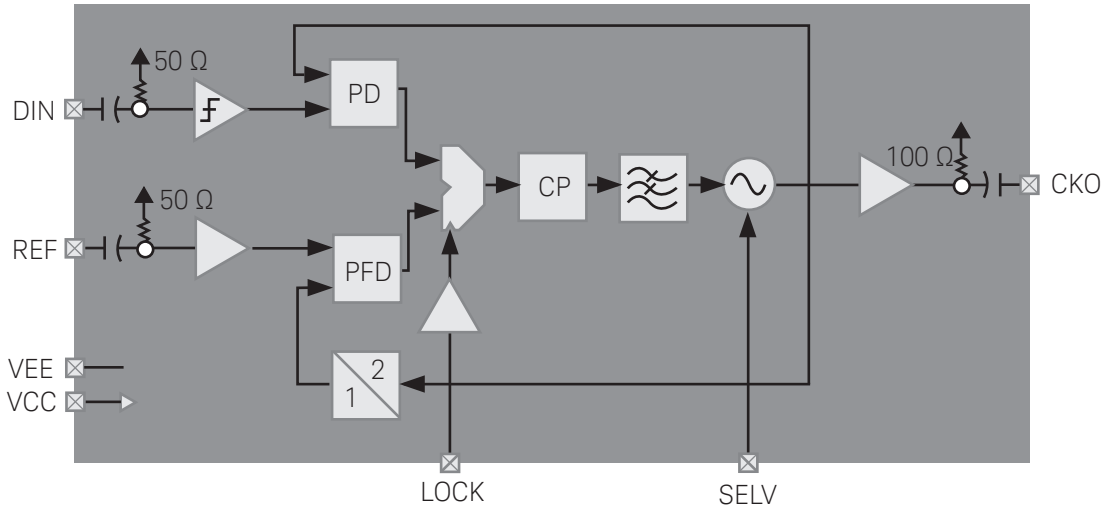


Figure 10. Functional block diagram

Pin description (see Figure 11 below)

Name	Pin	Description	Note	Connector
LOCK	1	Reference input selector	Internal PLL reference selector between input data and reference clock	SMB
SELV	2	Frequency range selector	Selects between two VCOs for lower/upper band	SMB
CKO	5	Clock output	AC-coupled, single ended output	2.92 mm
VEE	6	Negative supply voltage	Center pin –3.3 or –3.6 V, shield/case is ground	SMB
REF	7	Reference clock input	AC coupled input	2.92 mm
DIN	9	Data input	AC-coupled, single ended input	2.92 mm
NC	3, 4, 8	No connect		

Table 3.

LOCK logic

Parameters	State	Min	Typ	Max
Low (default)	Reference clock	–	–3.3 V	–
High	Data	–	0 V	–

Table 4.

SELV logic

Model-option number	Data rate range	SELV state	SELV voltage
N4982A-R19	19.0 to 22.2 Gb/s 39.8 to 44.0 Gb/s 22.2 to 26.0 Gb/	Low (default) Low (default) High	VEE (-3.6 V) VEE (-3.6 V) 0 V
N4982A-R25	25.3 to 29.0 Gb/s 27.5 to 32.0 Gb/s	High Low (default)	0 V VEE (-3.3 V)
N4982A-R28	27.9 to 32.0 Gb/s 32.0 to 36.0 Gb/s	Low (default) High	VEE (-3.3 V) 0 V

Table 5.

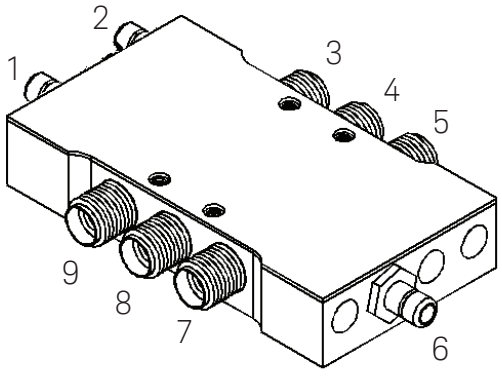


Figure 11. Module outline

N4982A Application Note

Clock recovery

The N4982A clock recovery unit has two phase locked loops with separate inputs—the REF input for training the loop to the right frequency, and the Data (DIN) input for phase locking the loop to the actual data. Refer to the block diagram. The CRU requires a 1/2 or 1/4 rate clock for training the PLL. Once the loop is trained, the input can be switched over to the data input by setting the LOCK pin (pin 1) High (0V).

Clock recovery setup procedure

1. Connect both data and reference inputs to the device. For example, with the N4982A-R19 if data rate is 25 Gb/s, then reference clock is 12.5 GHz (sine or square). Make sure that the LOCK pin (pin 1) is set to Low (VEE) or left open (it defaults to logic state Low).
2. Select the appropriate VCO frequency band by connecting SELV either VEE or 0V. For example, with the N4982A-R19 if the data rate is 25 Gb/s, then connect SELV to 0 V to enable the 22.2 to 26.0 GHz VCO band.
3. Monitor the output frequency to see if the loop has locked to the desired frequency. For this example, the loop is locked if CKO is 25 GHz.
4. Once the loop is locked (i.e. trained), switch the LOCK pin to High, or 0 V, to lock onto the data input.

Packaging Information

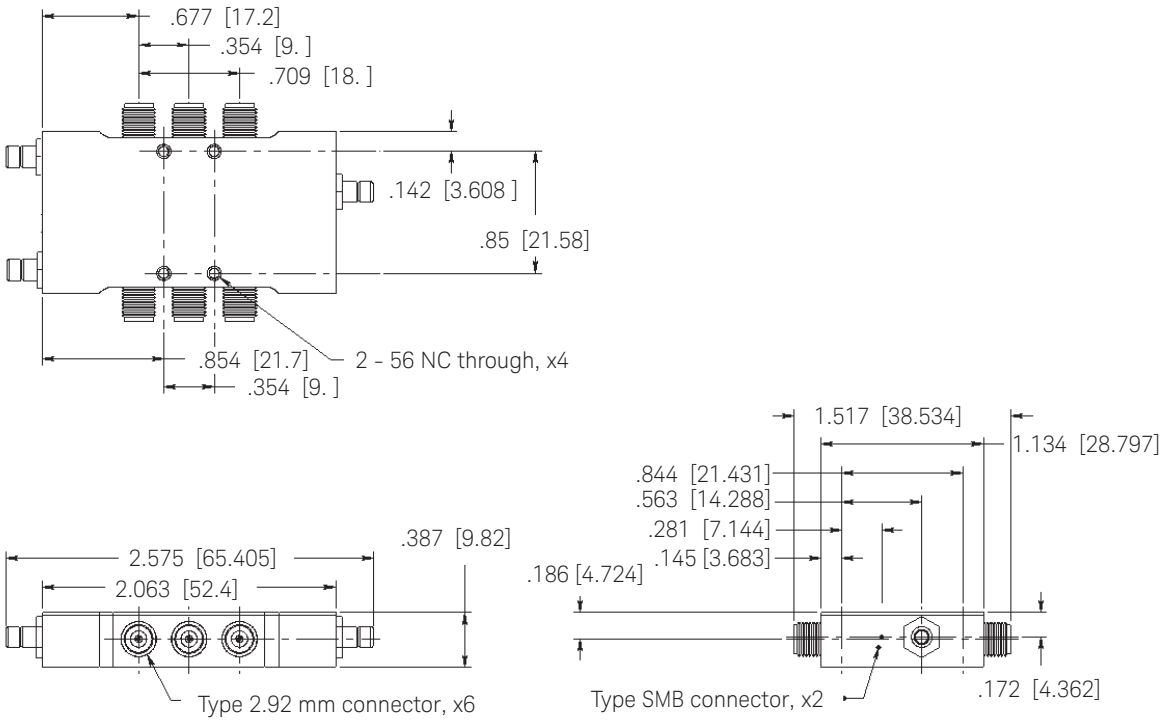


Figure 12. All measurements in inches (mm)

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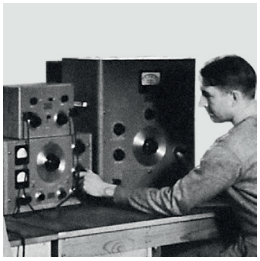
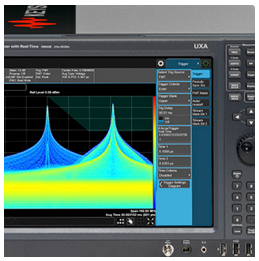


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Published in USA, December 1, 2017
5991-0701EN
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