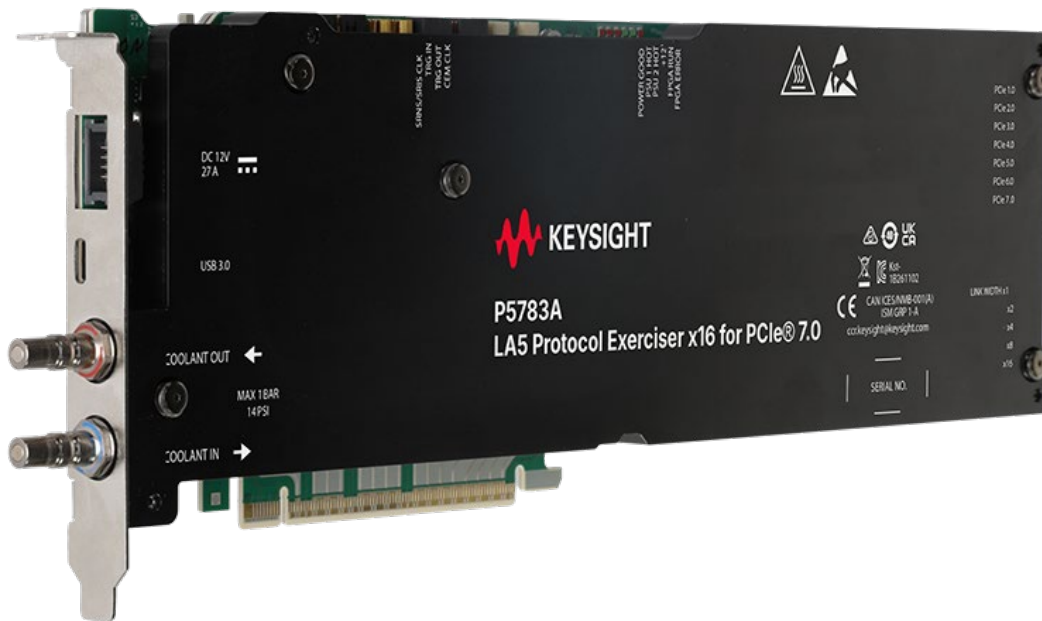


P5783A

Protocol Exerciser Module for PCIe® 7.0

Introduction

Keysight P5783A PCIe® 7.0 Protocol Exerciser allows test engineers to emulate both PCIe root complex and endpoint devices when validating PCIe designs. The exerciser supports traffic generation from 2.5 GT/s through 128 GT/s and lane widths from x1 to x16. The tool includes over 100 built-in LTSSM test cases, error insertion capabilities at the TLP and DLLP layers, and a protocol checker.



Product Overview

The Keysight P5783A PCIe® 7.0 Protocol Exerciser provides test and validation engineers a powerful tool for vetting and debugging their PCIe designs. The P5783A uses an integrated, single add-in card design that greatly simplifies the connection and setup while offering the signal integrity required for PCIe® 7.0 operation at data rates up to 128 GT/s. This enables test and validation engineers to focus their time and energy on designing and automating test cases for their products, rather than spending time dealing with an overly complex test setup.

The foundation of the P5783A is the improved signal integrity provided through the integrated design of the exerciser card. The card incorporates ASIC as the PCIe® 7.0 electrical interface and gearbox, providing a trustworthy test platform. This compact design allows Keysight engineers great versatility in ensuring that the P5783A offers signal integrity characteristics that can be tuned for many different test environments, while also providing quick link-up capability for test cases that focus on higher-layer protocol debugging. An integrated liquid-cooling system supports efficient heat dissipation during PCIe® 7.0 operation.

Key Capabilities Include:

The P5783A Exerciser supports PCIe data rates from 2.5 GT/s up to 128 GT/s and lane widths up to x16, along with the following features:

- Full-length PCIe® exerciser card featuring the ASIC with an integrated PCIe® 7.0 electrical interface and gear box
- Automated link training up to 128 GT/s
- Ability to initiate Higher and Lower Speed Changes between 2.5GT/s to max supported data rate
- Traffic generation directly from GUI or from automated user generated scripts
- Lane Reversal and polarity inversion detection
- Supports scalable flow control
- Link Training and Status State Machine (LTSSM) support with more than 100 built-in LTSSM test cases
- Lane and data rate negotiation from 2.5 GT/s to 128 GT/s
- Real-time equalization process
- Support for transaction layer features such as Memory Read/Write, I/O Read/Write, Config Read/Write, etc.
- Emulation as a Root Complex or an Endpoint
- Integrated liquid cooling system for efficient heat dissipation during PCIe® 7.0 operation at data rates up to 128 GT/s

Combined Exerciser and Analyzer Software

The Keysight P5783A PCIe® 7.0 Protocol Exerciser and P5762A PCIe® 7.0 Protocol Analyzer Module can be controlled through a common software interface, providing integrated configuration, traffic generation, capture, and analysis capabilities. The unified software environment enables users to configure exerciser and analyzer functions side by side through an intuitive tab-based interface, simplifying PCIe validation and debug workflows. Through this interface, users can configure key PCIe link characteristics, create and manage traffic generation scenarios, and efficiently exchange data between the exerciser and analyzer to accelerate protocol debugging and validation.

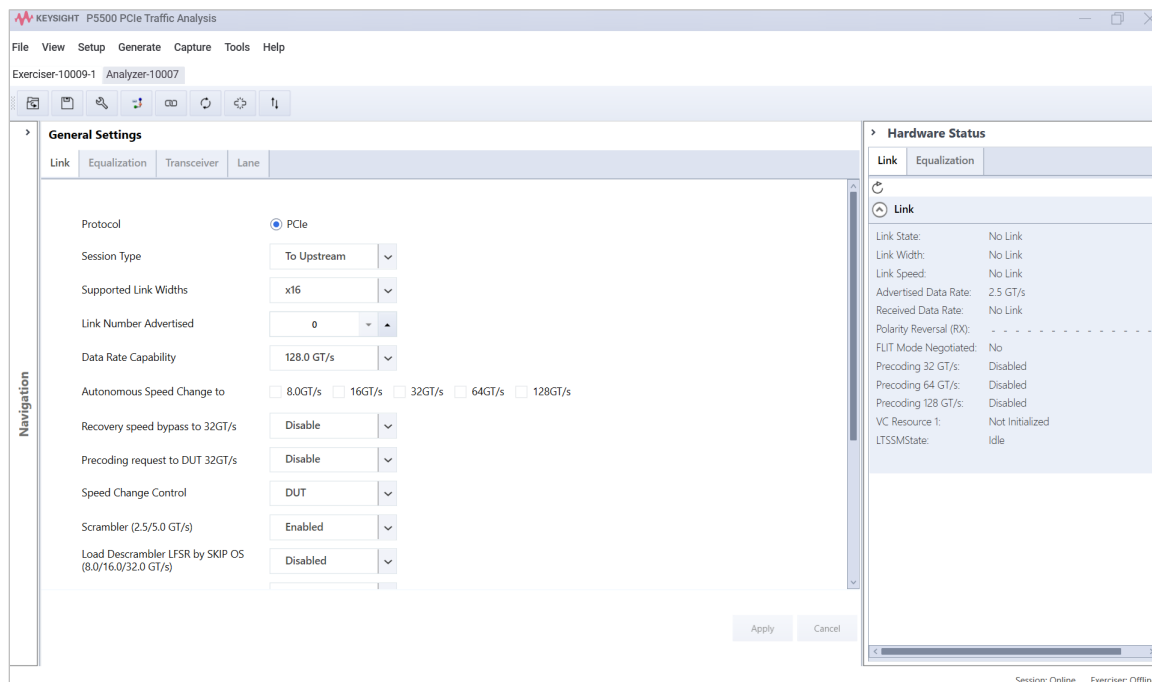


Figure 1. Keysight P5500 PCIe Traffic Analysis software for the P5783A Protocol Exerciser and P5762A Protocol Analyzer Module

Note: To enable protocol exerciser on the P5500 Traffic Analysis software, P5780PSWA license is required.

Ready to Go Protocol Test Features

The Keysight P5783A PCIe® 7.0 Protocol Exerciser is designed for rapid setup and configuration, enabling quick PCIe link bring-up and validation of LTSSM and protocol functionality. A comprehensive set of features supports efficient verification of fundamental PCIe capabilities.

Link Configuration

The P5783A PCIe® 7.0 Protocol Exerciser supports a wide range of PCIe link configuration options, providing engineers with a flexible platform for device validation, interoperability testing, and protocol debugging. Users can configure the following link parameters:

- Emulation as a Root Complex and an Endpoint
- Link widths from x1 to x16
- Data rate support for 2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s, 32.0 GT/s, 64.0 GT/s, and 128.0 GT/s
- Autonomous link speed changes between supported PCIe data rates
- Link training and link-speed negotiation
- Equalization configuration and control
- Lane reversal and polarity inversion support

General Settings			
Link	Equalization	Transceiver	Lane
Protocol	☒ PCIe		
Session Type	To Upstream		
Supported Link Widths	x16		
Link Number Advertised	0		
Data Rate Capability	128.0 GT/s		
Autonomous Speed Change to	☐ 8.0GT/s ☐ 16GT/s ☐ 32GT/s ☐ 64GT/s ☐ 128GT/s		
Recovery speed bypass to 32GT/s	Disable		
Precoding request to DUT 32GT/s	Disable		
Speed Change Control	DUT		
Scrambler (2.5/5.0 GT/s)	Enabled		
Load Descrambler LFSR by SKIP OS (8.0/16.0/32.0 GT/s)	Disabled		

Figure 2. PCIe Link configuration settings

LTSSM Test Tab

The LTSSM Test tab enables the execution of more than 100 LTSSM test cases based on the PCIe® 7.0 Base Specification, supporting a wide range of link training and state transition scenarios. It also provides configurable test criteria, including speed bypass and equalization bypass, to validate LTSSM flexibility under different operating conditions.

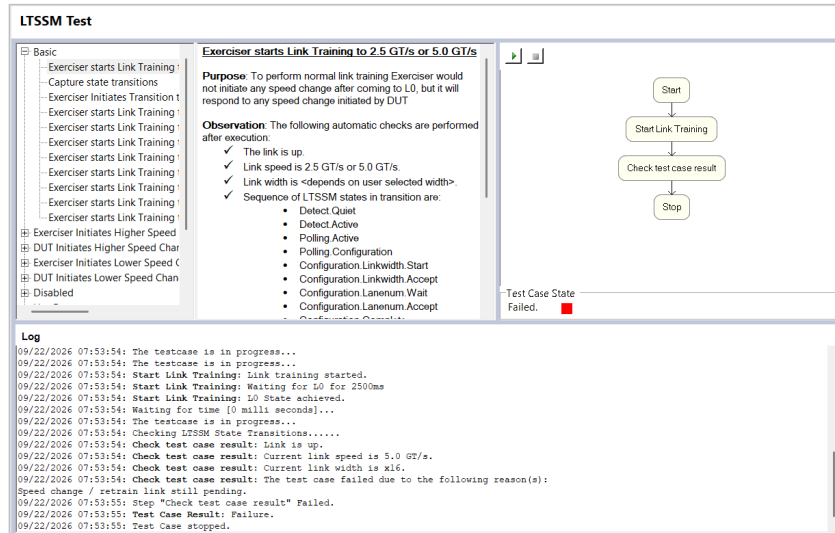


Figure 3. Over 100 LTSSM test cases are included

Lane Configuration

The P5783A PCIe® 7.0 Protocol Exerciser provides flexible lane configuration capabilities for PCIe link bring-up, validation, and debug. Users can enable or disable automatic lane reversal and independently invert transmitter lane polarity on selected lanes to emulate system configurations and verify device behavior under various lane-mapping scenarios.

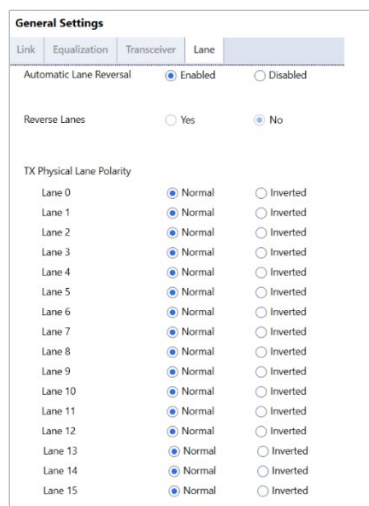


Figure 4. Lane configuration settings

Equalization and Transceiver Configuration Settings

The P5783A PCIe® 7.0 Protocol Exerciser provides extensive control over PCIe Link Equalization and transceiver parameters, enabling users to create targeted link training, interoperability, and compliance test scenarios across the respective PCIe specifications. Users can configure transmitter equalization settings and control equalization requests made during link training and link bring-up which includes typical requests such as presets and cursors.

General Settings

Link

Equalization

Transceiver

Lane

Equalization Settings (128.0 GT/s)

Automatic Coefficient Request To DUT

Autonomous Equalization

Request Preset In Phase 2/Phase 3

Perform Equalization In Recovery

Perform Equalization In Phase 2/Phase 3

Ignore Coefficient Rule A

Ignore Coefficient Rule B

Ignore Coefficient Rule C

Ignore Coefficient Rule D

☐

☒

☐

☐

☐

Presets

Cursors

Configure all lanes☐

Lane	DUT Start Preset	Exerciser Start Preset	DUT Target Preset
0	Q7	Q7	Q7
1	Q7	Q7	Q7
2	Q7	Q7	Q7
3	Q7	Q7	Q7
4	Q7	Q7	Q7
5	Q7	Q7	Q7

General Settings

Link

Equalization

Transceiver

Lane

Common Settings

Swing

1000 mV

Automatic Cursors (As Per DUT)

☒ 8.0 GT/s

☒ 16.0 GT/s

☒ 32.0 GT/s

☒ 64.0 GT/s

Figure 5. Equalization and Transceiver settings

Automation API

Custom test case development enables engineers to validate product-specific functionality and accelerate test coverage. To support automated testing workflows, the Keysight P5783A provides comprehensive scripting and automation capabilities through C# and Python APIs, enabling efficient execution of various test scenarios and increasing confidence in PCIe design reliability.

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Backplane Test Platform

The Keysight P5750A PCIe® 7.0 Backplane Test Platform features signal integrity enhancements designed to reduce crosstalk and improve signal fidelity. Utilizing low-loss materials and optimized signal paths, the platform supports reliable operation at data rates up to 128 GT/s, providing a stable environment for protocol analysis, interoperability testing, and device validation. Following are the features of the Test Backplane:

- Supports PCIe® 7.0 data rates from 2.5 GT/s to 128 GT/s.
- Includes CEM-to-CEM (up to x16) and CEM-to-EDSFF (up to x8) connector configurations.
- Supports Common Clock (CC), Separate Reference Clock with No Spread (SRNS), and Separate Reference Clock with Independent Spread (SRIS) architectures.
- Enhanced CEM and EDSFF signal integrity design help reduce crosstalk and improve measurement accuracy.
- Integrates a low-noise power supply with PCIe auxiliary power support for high-power endpoint devices.
- Robust mechanical design enables stable and reliable operation with test devices.

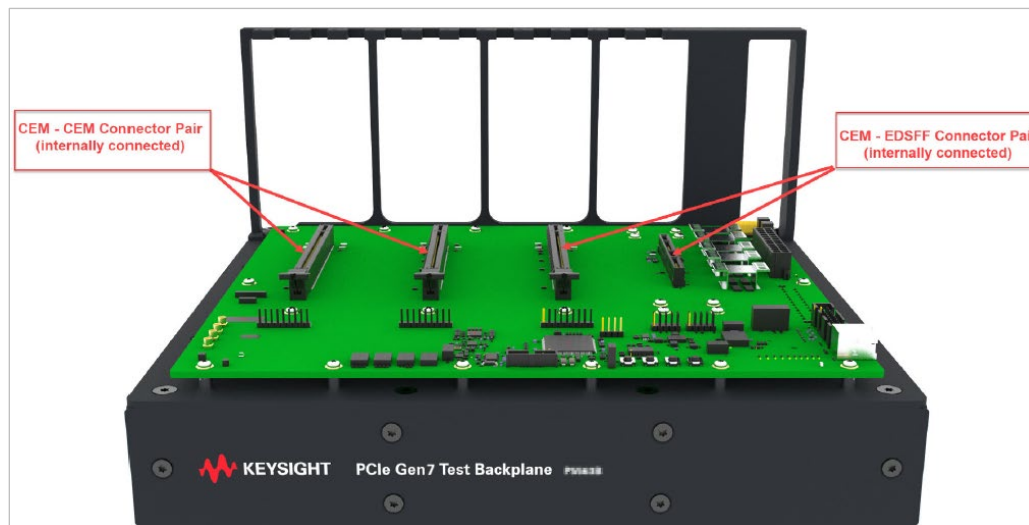


Figure 6. P5750A Backplane Test Platform

Use Case: Root Complex Emulation for Testing Endpoints

In this configuration, the P5783A PCIe® 7.0 Protocol Exerciser installed into a PCIe CEM slot on the test platform emulates a Root Complex and communicates with an endpoint device under test. The endpoint device is mounted on the P5773A PCIe® 7.0 x16 CEM Analyzer Interposer, enabling the exerciser to generate PCIe traffic and protocol events for endpoint validation and interoperability testing.

The P5783A provides control of key PCIe link parameters, including link training, equalization, and link-speed negotiation, allowing engineers to verify endpoint behavior under a variety of operating conditions. Engineers can validate link initialization and training sequences, investigate protocol interactions, and verify endpoint compliance with PCIe specifications including various error insertion scenarios for stress testing.

For enhanced debug and analysis capabilities, the P5773A Analyzer Interposer can be connected to one or more P5762A PCIe® 7.0 Protocol Analyzer Modules. In this configuration, traffic exchanged between the emulated Root Complex and the endpoint device is acquired by the interposer and transferred to the analyzer modules, where protocol capture, triggering, decode, and analysis are performed. Engineers can view and analyze protocol activity using the Keysight P5500 PCIe Traffic Analysis Software running on the controller PC.

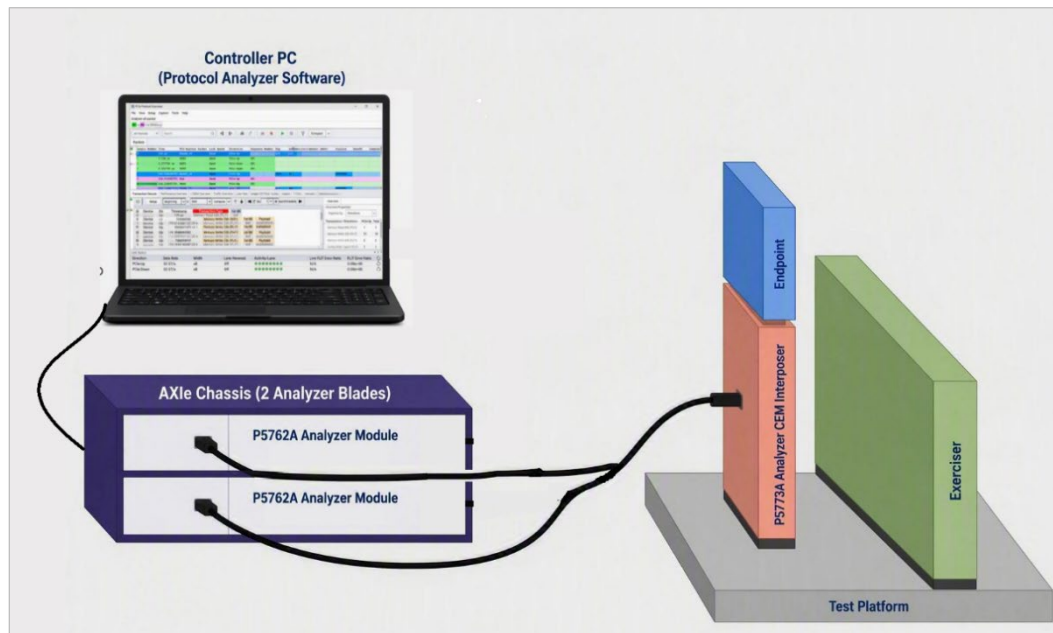


Figure 7. The P5783A PCIe 7.0 Protocol exerciser can be used to emulate a root complex

Use Case: End Point Emulation for Testing Root Complex

In this configuration, the P5783A PCIe® 7.0 Protocol Exerciser is mounted on the P5773A PCIe® 7.0 x16 CEM Analyzer Interposer, which is installed in a PCIe CEM slot on the host system. The P5783A emulates an endpoint device and communicates with the host system acting as a root complex.

Operating as an endpoint device, the P5783A generates and responds to PCIe traffic, enabling engineers to validate root complex behavior, verify link initialization and training sequences, and investigate protocol interactions during system development. This configuration provides a flexible platform for root complex validation, interoperability testing, and protocol debugging.

For enhanced protocol visibility and analysis, the P5773A Analyzer Interposer can be connected to one or more P5762A PCIe® 7.0 AXIe-based Protocol Analyzer Modules. In this configuration, traffic exchanged between the host system and the emulated endpoint device is acquired by the interposer and transferred to the analyzer modules, where protocol capture, triggering, decode, and analysis are performed. Engineers can view and analyze protocol activity using the Keysight P5500 PCIe Traffic Analysis Software running on the controller PC.

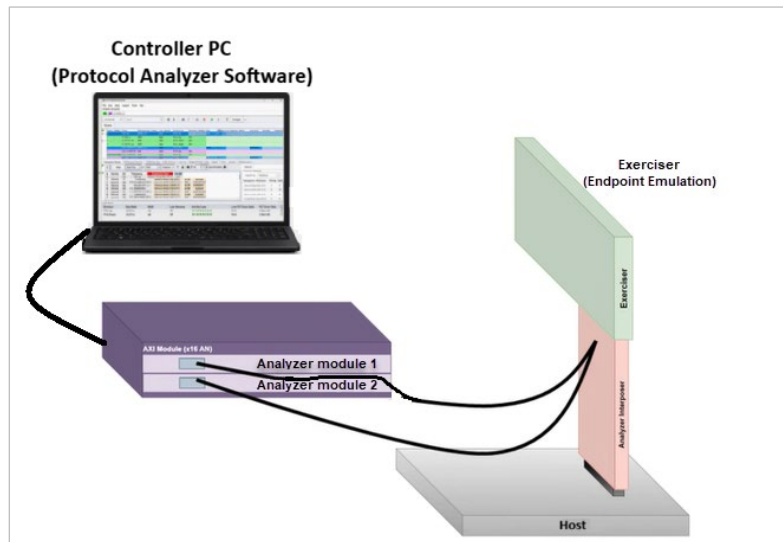


Figure 8. Endpoint emulation for testing a Root Complex using the P5783A PCIe® 7.0 Protocol Exerciser

Product Specifications

General Characteristics	Description	Comments
Link widths	x1, x2, x4, x8, x16	
Data rates	2.5 GT/s (Gen1), 5.0 GT/s (Gen2), 8.0 GT/s (Gen3), 16.0 GT/s, (Gen4), and 32 GT/s(Gen5), 64 GT/s(Gen6), and 128 GT/s (Gen7)	
Speed	Up to 64 GBaud PAM4 per lane	
Clocking architecture	Supports CC, SRNS, and SRIS clocking architectures	

Additional Recommended Hardware

While the Keysight P5783A PCIe® 7.0 Protocol Exerciser is quite versatile as a stand-alone test tool, more complicated test configurations can be supported when the P5783A is paired with additional Keysight hardware to improve analysis capability, robustness, and mechanical stability. Additional Keysight products that support the P5783A are shown below.

Keysight model number(s)	Description	Comments
P5762A	PCIe 7.0 Protocol Analyzer Module	Interfaces with the P5773A Analyzer Interposer to capture, decode, and analyze PCIe traffic acquired from the link under test.
M9506A	AXle High-Performance 5-Slot Chassis	Required for installation and operation of the P5762A PCIe 7.0 Protocol Analyzer Module
P5773A	PCIe 7.0 Analyzer CEM Interposer	Connects to the link under test and interfaces with the P5762A Analyzer Module
P5750A	PCIe 7.0 Backplane Test Platform	Supports CEM-to-CEM and CEM-to-EDSFF test configurations. Only needed for endpoint testing.
Controller PC	Microsoft Windows 11, 64-bit operating system (x64-based processor only)	Required for running P5500 PCIe Traffic Analysis software

Ordering Information

Model	Description	Comments
P5762A	PCIe 7.0 Analyzer AXIe Module x8	Two analyzer modules required to support x16 link width
P5773A	PCIe 7.0 Analyzer CEM Interposer x16	
P5783A	PCIe 7.0 Exerciser x16 CEM	
P5750A	PCIe 7.0 Test Backplane	
P5770PSWA	PCIe 7.0 Analyzer Software	License
P5780PSWA	PCIe 7.0 Exerciser Software	License

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