Keysight D9020DPHC MIPI® D-PHY℠ Compliance Test Application

KEYSIGHT

METHODS OF IMPLEMENTATION

Notices

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MIPI® D-PHY℠ Automated Testing—At a Glance

The Keysight D9020DPHC MIPI D-PHY Test Application allows the testing of all MIPI devices with the Keysight Infiniium Series Oscilloscopes based on the MIPI Alliance Standard for D-PHY specification. MIPI stands for Mobile Industry Processor Interface. The MIPI alliance is a collaboration of mobile industry leader with the objective to define and promote open standards for interfaces to mobile application processors.

The Keysight D9020DPHC MIPI D-PHY Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE

The tests performed by the Keysight D9020DPHC MIPI D-PHY Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.

Required Equipment and Software

In order to run the MIPI D-PHY automated tests, you need the following equipment and software:

Hardware

- Use one of the following oscilloscope models with a minimum bandwidth of 4 GHz or higher:
  - Keysight Infiniium Series Digital Storage Oscilloscopes (9000 Series, 90000 Series, 90000 X-Series, 90000 Q-Series, V-Series, or Z-Series)
  - Keysight UXR Oscilloscopes
  - Keysight Infiniium MXR Real-Time Oscilloscope; only channels 1-4 are supported and pairing of channels 1-3 and 2-4 is allowed. MXR supports up to 2.5 Gbps High-Speed Data Rate for D-PHY test signals.
  - For more info on supported oscilloscope models, please refer to the Keysight D9020DPHC MIPI D-PHY Test Application Release Notes on www.keysight.com.
- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Three InfiniiMax Probes (min. 5GHz bandwidth) - 1132A
- Probing connection:
  - Differential probe amplifier, with the minimum bandwidth of 5 GHz
  - One of the E2677A differential solder-in probe head, E2893A differential browser probe head, E2678B differential socket probe head, and E2669B differential kit, which includes E2675B, E2677B, and E2678B, are recommended
- Direct connect connection:
  - 15443A Matched cable pair
- Keysight also recommends using a second monitor to view the test application.

Software

- The minimum version of Infiniium Oscilloscope Software (see the Keysight D9020DPHC MIPI D-PHY Test Application Release Notes on www.keysight.com)
- Keysight D9020DPHC MIPI D-PHY Test Application software

Licensing information

Refer to the *Data Sheet* pertaining to MIPI D-PHY Test Application to know about the licenses you must install along with other optional licenses. Visit "http://www.keysight.com/find/D9020DPHC" and in the web page's **Document Library** tab, you may view the associated Data Sheet.

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

The licensing format for Keysight License Manager 6 differs from its predecessors. See "Installing the License Key" on page 41 to see the difference in installing a license key using either of the applications on your machine.

In This Book

This manual describes the tests that are performed by the Keysight D9020DPHC MIPI D-PHY Test Application in more detail; it contains information from (and refers to) various MIPI D-PHY specifications and it describes how the tests are performed.

- Chapter 2, “Installing the Test Application and Licenses” explains how to obtain the installer for the automated test application and install the associated licenses (if it was purchased separately).
- Chapter 3, “Preparing to Take Measurements” describes how to launch the Keysight D9020DPHC MIPI D-PHY Test Application and gives a brief overview of how it is used.
- Part A MIPI D-PHY 1.0 consists of tests pertaining to MIPI D-PHY v 1.0.
- Part B MIPI D-PHY 1.1 consists of tests pertaining to MIPI D-PHY v 1.1.
- Part C MIPI D-PHY 1.2 consists of tests pertaining to MIPI D-PHY v 1.2.
- Part D MIPI D-PHY 2.0 & 2.1 consists of tests pertaining to MIPI D-PHY v 2.0 & 2.1.
- Part I Electrical Characteristics emphasizes on HS Data, HS Clock, LP Data and LP Clock Transmitter tests. These tests are available for MIPI D-PHY 1.0, MIPI D-PHY 1.1, MIPI D-PHY 1.2, and MIPI D-PHY 2.0 and 2.1.
- Part II Global Operation covers Data and Clock Transmitter tests. These tests are available for MIPI D-PHY 1.0, MIPI D-PHY 1.1, MIPI D-PHY 1.2, and MIPI D-PHY 2.0 and 2.1.
- Part III HS Data-Clock Timing covers HS Data-Clock Timing Tests (available for MIPI D-PHY 1.0, MIPI D-PHY 1.1, MIPI D-PHY 1.2, and MIPI D-PHY 2.0 and 2.1) and HS Skew Calibration Burst Tests (available for MIPI D-PHY 1.2 and MIPI D-PHY 2.0 and 2.1).
- Part IV to Part VIII consists of the following sections, which are available only for MIPI D-PHY 2.0 and 2.1:
  - Part IV HS Spread Spectrum Clocking
  - Part V HS Jitter & Eye Diagram
  - Part VI Alt. Calibration Tests
  - Part VII Preamble Seq. Tests
  - Part VIII HS Idle Timing Tests
- Part IX Informative Tests consists of reference to FYI tests available for MIPI D-PHY 2.0 and 2.1.

See Also

The Keysight D9020DPHC MIPI D-PHY Test Application’s Online Help, which describes:

- Starting the MIPI D-PHY Test Application
- Creating or Opening a Test Project
- Setting Up the Test Environment
- Selecting Tests
- Configuring Tests
- Verifying Physical Connections
- Running Tests
- Configuring Automation in the Test Application
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
- Additional Settings in the Test App

2 Installing the Test Application and Licenses

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If you purchased the D9020DPHC MIPI D-PHY Test Application separate from your Infiniium oscilloscope, you must install the software and license key.

KEYSIGHT TECHNOLOGIES

Installing the Test Application

1. Make sure you have the minimum version of Infiniium Oscilloscope software (see the D9020DPHC release notes). To ensure that you have the minimum version, select **Help > About Infiniium...** from the main menu.
2. To obtain the MIPI D-PHY Test Application, go to Keysight website: "http://www.keysight.com/find/D9020DPHC".
3. In the web page's **Trials & Licenses** tab, click the **Details and Download** button to view instructions for downloading and installing the application software.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

1 Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.

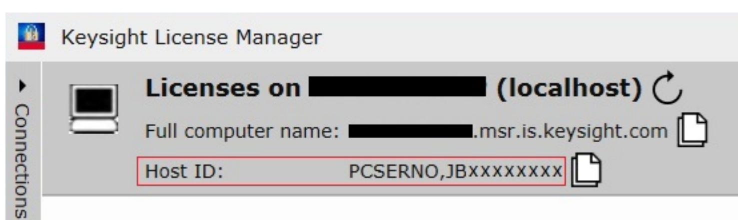

Figure 1 Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager.

3 From the configuration menu, use one of the options to install each license file.

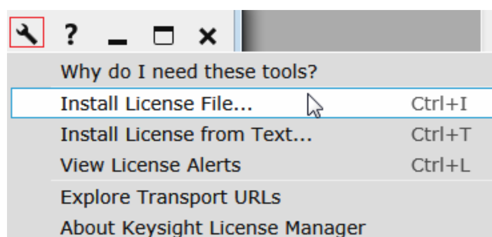

Figure 2 Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

1 Launch Keysight License Manager 6 on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID, which is the first set of alphanumeric value (as highlighted in Figure 3) that appears in the Environment tab of the application. Note that x indicates numeric values.

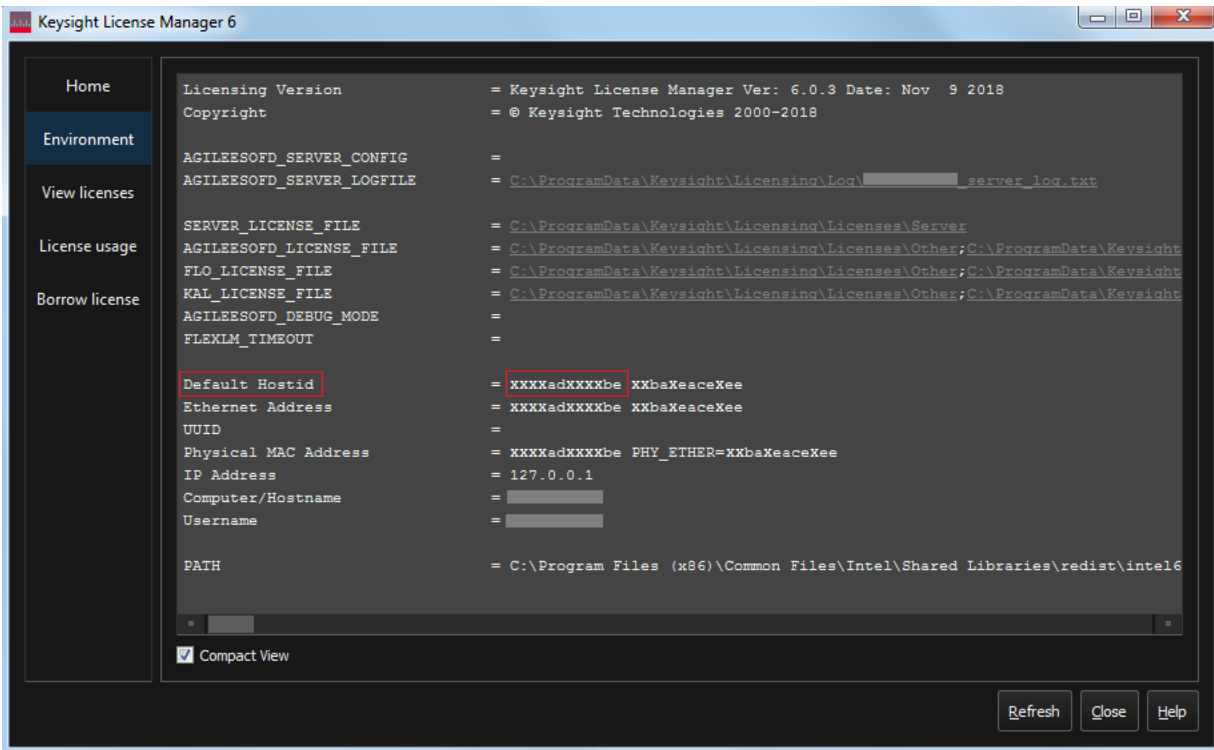

Figure 3 Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.
2 Launch Keysight License Manager 6.
3 From the Home tab, use one of the options to install each license file.

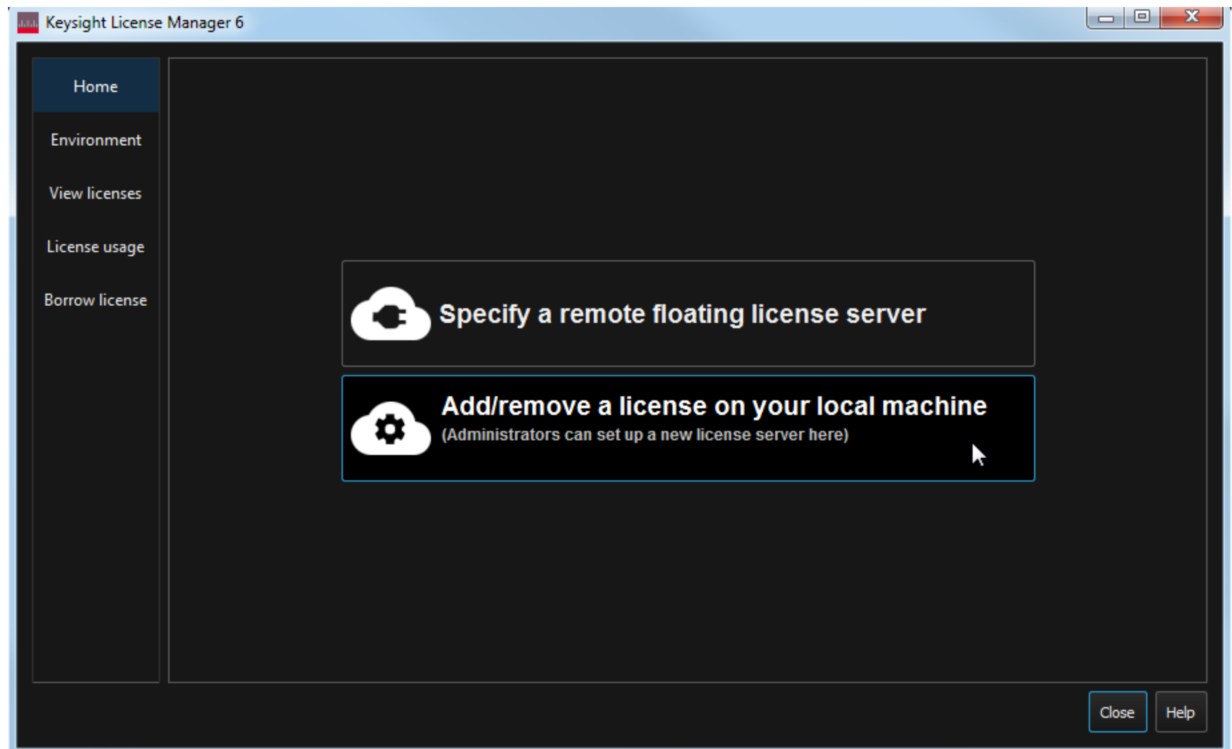

Figure 4 Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

3 Preparing to Take Measurements

Calibrating the Oscilloscope 46
Starting the MIPI D-PHY Test Application 47
Fixture Options 49

Before running the automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this application. After the oscilloscope and probe have been calibrated, you are ready to start the MIPI D-PHY Test Application and perform the measurements.

Calibrating the Oscilloscope

If you have not already calibrated the oscilloscope, refer to the *User Guide* for the respective Oscilloscope you are using.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.

NOTE If you switch cables between channels or other Oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the MIPI D-PHY Test Application

1 Ensure that the MIPI D-PHY Device Under Test (DUT) is operating and set to desired test modes. To start the MIPI D-PHY Test Application: From the Infiniium Oscilloscope's main menu, select **Analyze > Automated Test Apps > D9020DPHC MIPI D-PHY Test App**.

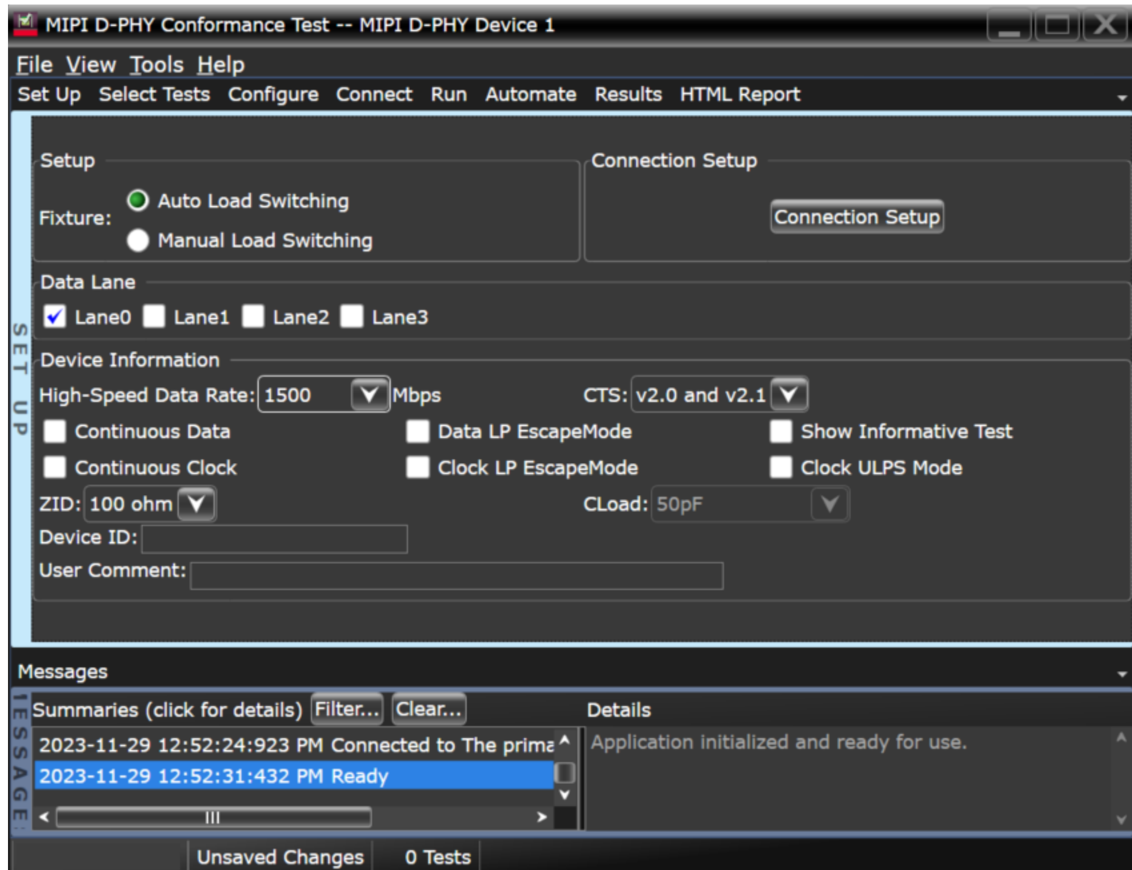

Figure 5 MIPI D-PHY Test Application Main Window

To understand the functionality of the various features in the user interface of the Test Application, refer to the *Keysight D9020DPHC MIPI D-PHY Test Application Online Help* available in the Help menu.

The task flow pane and the tabs in the main pane show the steps you take in running the automated tests:

Set Up	Lets you identify and set up the test environment, including information about the device under test. The Test App includes relevant information in the final HTML report.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (for example, channels used in test, voltage levels, etc.).
Connect	Shows you how to connect the oscilloscope to the device under test for the tests that are to be run.
Run	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automate	Lets you construct scripts of commands that drive execution of the application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE

In the **Configure** tab, the values for all such Configuration parameters that are Oscilloscope-dependent, will correspond to the Oscilloscope Model (DSOs or UXRs), where you are running the Test Application.

Fixture Options

In some high-speed serial technologies (such as, PCI Express, SATA and so on) that utilize a static, 100-ohm differential reference termination environment, it is typical to use the test equipment input ports as the reference termination load for measurements. However, it is not possible to use the test equipment (in this case, an oscilloscope) as the reference termination because the MIPI D-PHY technology utilizes a dynamic, switchable resistive termination at the receiver (to enable the power-saving feature). This switchable resistive termination, which is a 100-ohm differential reference termination, is enabled during the High-Speed (HS) mode of operation, and disabled (open termination environment) during the Low-Power (LP) mode.

The common approach to perform the MIPI D-PHY test measurements is to utilize some test measurement fixtures that have the capability to handle the required termination load of various forms for the selected tests (High-Speed mode or Low-Power mode tests). In general, there are two types of test fixtures where one type is able to handle the automatic switching of the required termination load and the other type supports only one termination load at a time.

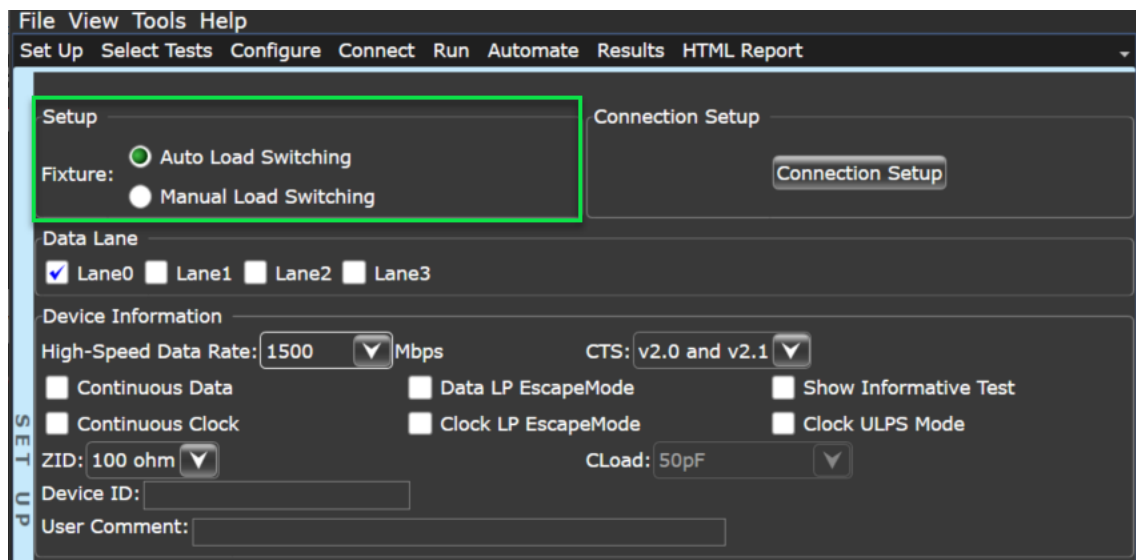

Figure 6 Fixture Options on the MIPI D-PHY Test App

Manual Load Switching

For test fixtures that may handle only static termination environment, either by providing a 100-ohm differential reference termination load or just an open load condition, you must select the **Manual Load Switching** option in the **Fixture** area of the **Set Up** tab of the test compliance application. In such scenarios, when you run tests after selecting some HS mode tests and some LP mode tests under the **Select Tests** tab, the application prompts a connection diagram, which allows you to change the physical set up and use the correct test fixture.

Auto Load Switching

For test fixtures that may handle the dynamic termination load switching criteria, you must select the **Auto Load Switching** option in the **Fixture** area of the **Set Up** tab of the test application. The most common test fixture that you may use is the MIPI D-PHY Reference Termination Board (RTB). You may obtain the MIP D-PHY RTB from the University of New Hampshire InterOperability Lab (UNH-IOL). The UNH-IOL works closely with the MIPI Alliance (standard body for MIPI) and has developed a testing program/fixtures/boards to meet the unique needs of the mobile industry (including the D-PHY RTB). In this scenario, you may use the same test fixture (for example, the RTB) setup to handle the dynamic termination environment required when testing all the HS mode tests.

Figure 7 Sample MIPI D-PHY Reference Termination board (RTB)

Part A
MIPI D-PHY 1.0

KEYSIGHT
TECHNOLOGIES

Part I
Electrical Characteristics

KEYSIGHT
TECHNOLOGIES

4 MIPI D-PHY 1.0 High Speed Data Transmitter (HS Data TX) Electrical Tests

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Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation / 58
Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($\Delta V_{CMTX(1,0)}$) Method of Implementation / 60
Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz (ΔV_{CMTX}(HF)) Method of Implementation / 62
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Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation / 71
Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation / 74
Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation / 75

This section provides the Methods of Implementation (MOIs) for the High Speed Data Transmitter (HS Data TX) Electrical tests using an Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

Probing for High Speed Data Transmitter Electrical Tests

When performing the HS Data TX tests, the MIPI D-PHY Test Application may prompt you to make changes to the physical setup. The connections for the HS Data TX tests may look similar to the following diagrams. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

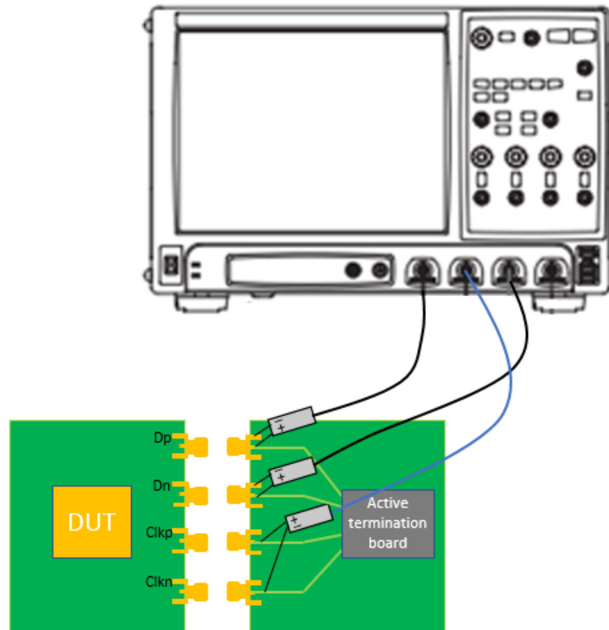

Figure 8 Probing for High Speed Data Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 8 are just for illustration).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, ZID (termination resistance), CLoad, Device ID and User Comments.
4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

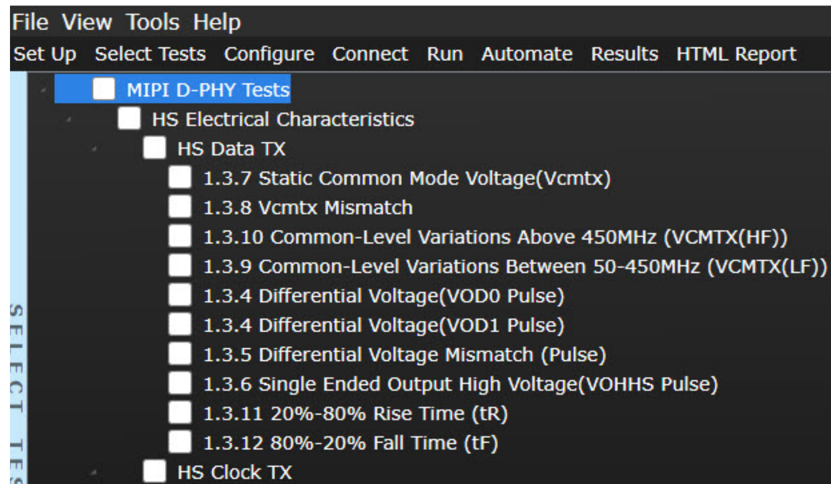

Figure 9 Selecting High Speed Data Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation

The High Speed Data Transmitter Static Common Mode Voltage, V_{CMTX} is defined as the arithmetic mean value of the voltages at the Dp and Dn pins. Because of various types of signal distortion that may occur, it is possible for V_{CMTX} to have different values when a Differential-1 vs. Differential-0 state is driven.

For this test, the values for V_{CMTX} is measured for both the Differential-1 and Differential-0 states and averaged over at least a HS burst.

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

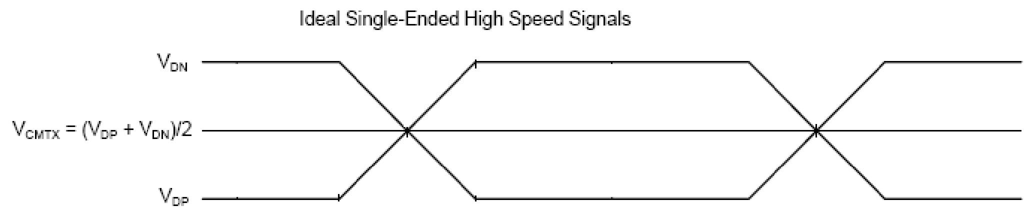

Figure 10 Ideal Single-Ended High Speed Signals

PASS Condition

The measured V_{CMTX} value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 1 Test Availability Condition for Test 1.3.7

Associated Test ID	HS Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Methods	
								Active Probe (Differential Probe)	Direct Connect (Active Termination Adapter)
811	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Available	Dependent on Continuous Clock and Continuous Data settings

Measurement Algorithm using Test ID 811

NOTE Use the Test ID# 811 to remotely access the test.

1 Trigger at SoT of HS Data burst (LP11 to LP01).
2 For the HS Data, common-mode waveform is required. The waveform can be constructed by using the following equation:

$$DataCommonMode = (D_p+D_n)/2$$

3 For the HS Clock, differential waveform is required. This can be achieved by directly probing the differential signal or by probing the single-ended clock signal and form a differential signal by using the singled-ended signals with the following equation:

$$ClockDiff = Clkp - Clkn$$

4 Sample the Common-Mode HS Data waveform by using all the edges of the differential HS Clock as sampler and denote it as V_{CMTX}.
5 Separate the V_{CMTX} into 2 arrays; V_{CMTX} for Differential-1 and V_{CMTX} for Differential-0.
6 Report the measurement results:
   - Mean V_{CMTX} for Differential-1 and Differential-0
   - V_{CMTX} worst value between Differential-1 and Differential-0
7 Compare the measured V_{CMTX} worst value to the compliance test limits.

Test References

See Test 1.3.7 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($\Delta V_{CMTX(1,0)}$) Method of Implementation

The common-mode voltage V_{CMTX} is defined as the arithmetic mean value of the voltages at the D_p and D_n pins. Because of various types of signal distortion that occurs, it is possible for V_{CMTX} to have different values when a Differential-1 vs. Differential-0 state is being driven.

For this test, the values for V_{CMTX} are measured for both the Differential-1 and differential-0 states and averaged over at least one HS Data burst. The difference between the V_{CMTX} values for Differential-1 and Differential-0 is computed.

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2} \quad , \quad \Delta V_{CMTX(1,0)} = \frac{V_{CMTX(1)} - V_{CMTX(0)}}{2}$$

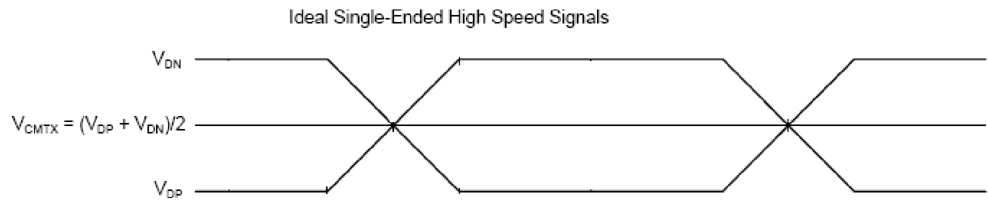

Figure 11 Ideal Single-Ended High Speed Signals

PASS Condition

The measured $\Delta V_{CMTX(1,0)}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 2 Test Availability Condition for Test 1.3.8

Associated Test ID	HS Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Methods	
								Active Probe (Differential Probe)	Direct Connect (Active Termination Adapter)
812	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Available	Dependent on Continuous Clock and Continuous Data settings

Measurement Algorithm using Test ID 812

NOTE **Use the Test ID# 812 to remotely access the test.**

1. This test requires the following prerequisite tests:
   - HS TX Static Common Mode Voltage (V_{CMTX}) (Test ID 811)
   - Actual V_{CMTX} for Differential-1 and Differential-0 measurements are performed and test results are stored.
2. Compute the V_{CMTX} mismatch using the following calculation:

   V_{CMTX} Mismatch = ([V_{CMTX} for Differential-1] - [V_{CMTX} for Differential-0]) / 2
3. Report the measurement results:
   - V_{CMTX} for Differential-1 and Differential-0
   - V_{CMTX} mismatch
4. Compare the measured ΔV_{CMTX} mismatch to the compliance test limit.

Test References

See Test 1.3.8 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz ($\Delta V_{CMTX(HF)}$) Method of Implementation

For this $\Delta V_{CMTX(HF)}$ test, the values for V_{CMTX} is obtained by using the following equation:

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

Ideally the common mode voltage should be as per the figure below.

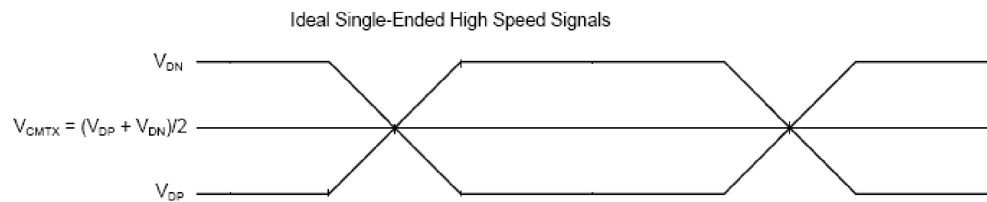

Figure 12 Ideal Single-Ended High Speed Signals

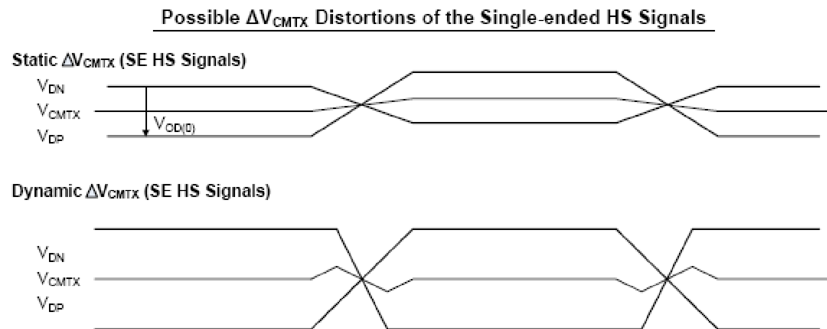

Figure 13 Possible Distortions of the ΔV_{CMTX} Single-Ended High Speed Signals

The objective of the test is to measure the distortion over the interested frequency band for a HS Data burst.

PASS Condition

The measured $\Delta V_{CMTX(HF)}$ value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 3 Test Availability Condition for Test 1.3.10

Associated Test ID	HS Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Methods	
									Active Probe (Differential Probe)	Direct Connect (Active Termination Adapter)
818	Not Applicable	100 ohms	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Available	Dependent on Continuous Clock and Continuous Data settings

Measurement Algorithm using Test ID 818

NOTE Use the Test ID# 818 to remotely access the test.

1 Trigger at SoT of HS Data burst (LP11 to LP01).
2 Find the HS Data bursts.
3 For the HS Data, common-mode waveform is required. The waveform can be constructed using the following equation:

$$DataCommonMode = (Dp+Dn)/2$$

4 A high pass filter with 3dB bandwidth frequency at 450MHz is applied to the common-mode waveform.
5 Measure the RMS voltage for the filtered waveform and record as $\Delta V_{CMTX(HF)}$.
6 Report the measurement results:
  - $\Delta V_{CMTX(HF)}$ value
7 Compare the measured $\Delta V_{CMTX(HF)}$ value to the compliance test limit.

Test References

See Test 1.3.10 in CTS v1.0 and Section 8.1.1 Table 17 in the D-PHY Specification v1.0.

Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz ($\Delta V_{CMTX(LF)}$) Method of Implementation

For this $\Delta V_{CMTX(LF)}$ test, the values for V_{CMTX} is obtained by using the following equation:

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

Ideally the common mode voltage should be as per the figure below:

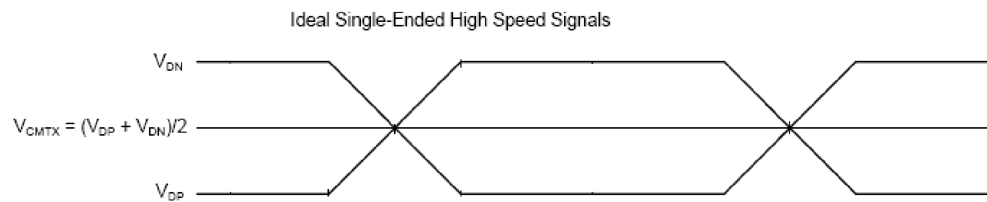

Figure 14 Ideal Single-Ended High Speed Signals

In reality, various type for distortion can happen as shown in figure below:

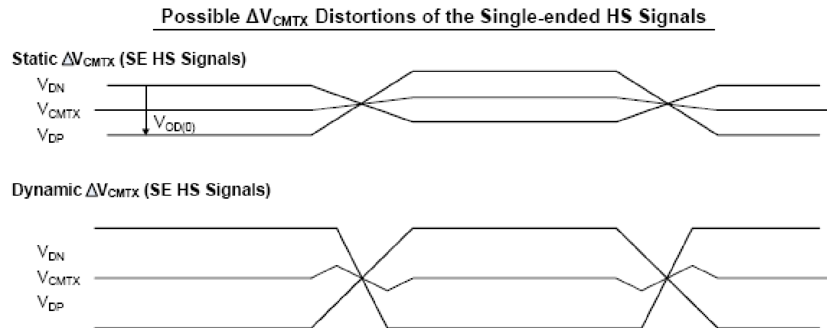

Figure 15 Possible Distortions of the ΔV_{CMTX} Single-Ended High Speed Signals

The objective of the test is to measure the distortion over the interested frequency band for a HS data burst.

PASS Condition

The measured $\Delta V_{CMTX(LF)}$ value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 4 Test Availability Condition for Test 1.3.9

Associated Test ID	HS Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Methods	
									Active Probe (Differential Probe)	Direct Connect (Active Termination Adapter)
819	Not Applicable	100 ohms	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Available	Dependent on Continuous Clock and Continuous Data settings

Measurement Algorithm using Test ID 819

NOTE Use the Test ID# 819 to remotely access the test.

1 Trigger at SoT of HS data burst (LP11 to LP01).
2 Find the HS data bursts.
3 For the HS data, common-mode waveform is required. The waveform can be constructed using the following equation:

DataCommonMode = (Dp+Dn)/2

4 A band pass filter with 3dB bandwidth frequency at 50MHz and 450MHz is applied to the common-mode waveform.
5 Measure the min and max voltage for the filtered waveform.
6 Select the worst absolute value for the min and max voltage and record it as $\Delta V_{CMTX(LF)}$.
7 Report the measurement results:
   - $\Delta V_{CMTX(LF)}$ value
8 Compare the measured $\Delta V_{CMTX(LF)}$ value to the compliance test limit.

Test References

See Test 1.3.9 in CTS v1.0 and Section 8.1.1 Table 17 in the D-PHY Specification v1.0.

Test 1.3.4 HS Data TX Differential Voltage (V_{OD}) Method of Implementation

The output differential voltage, V_{OD} is defined as the difference of voltages V_{DP} and V_{DN} at the Dp and Dn pins, respectively.

$$V_{OD} = V_{DP} - V_{DN}$$

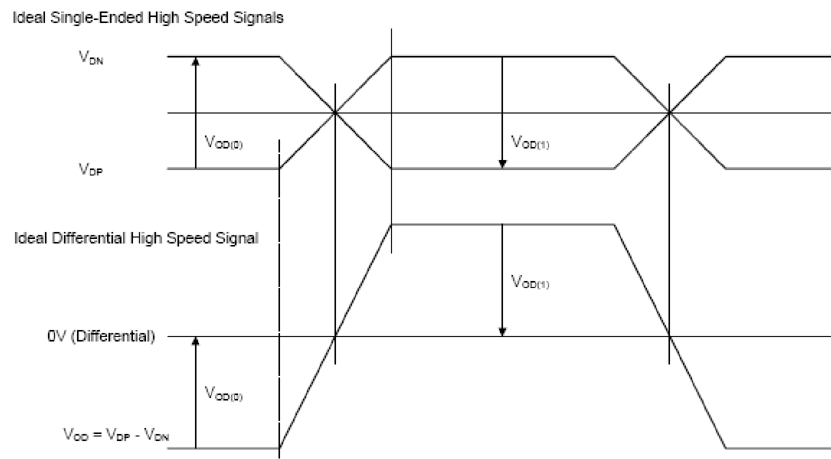

Figure 16 Ideal Single-Ended and Differential High Speed Signals

PASS Condition

The measured V_{OD} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 5 Test Availability Condition for Test 1.3.4

Associated Test IDs		8131	8132
Conditions			
HS Data Rate		Not applicable	Not applicable
Continuous Data		Not applicable	Not applicable
Continuous Clock		Not applicable	Not applicable
Data LP EscapeMode		Not applicable	Not applicable
Clock LP EscapeMode		Not applicable	Not applicable
Clock ULPS Mode		Not applicable	Not applicable
Informative Test		Not applicable	Not applicable
Probing Methods	**Active Probe (Differential Probe)**	Available	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock and Continuous Data settings	Availability dependent on Continuous Clock and Continuous Data settings
	Direct Connect	Availability dependent on Continuous Clock and Continuous Data settings	Availability dependent on Continuous Clock and Continuous Data settings

Measurement Algorithm using Test IDs 8131 and 8132

HS Data TX Differential Voltage (V_{OD0} Pulse)

NOTE Use the Test ID# 8131 to remotely access the test.

HS Data TX Differential Voltage (V_{OD1} Pulse)

NOTE Use the Test ID# 8132 to remotely access the test.

1. Trigger at SoT of HS data burst (LP11 to LP01).
2. Find the HS data bursts.
3. For HS data, differential waveform is required. The waveform can be constructed by using the following equation:

   DataDiff = Dp-Dn

4. For the HS Clock, differential waveform is required. The waveform can be constructed by using the following equation:

   ClkDiff = Clkp - Clkn

5. The acquired waveform is searched for the respective reference data pattern of “011111” for V_{OD1} and “100000” for V_{OD0} test.
6. Generates the averaged waveform that consists of all the reference data pattern found.

7 The mean value for the histogram window that fall between the centers of the fourth and fifth ‘1’ bits is measured as the mean V_{OD} value using the histogram function.

8 Report the measurement results:

- Mean V_{OD} for Differential-1 or Differential-0

9 Compare the mean V_{OD} value to the compliance test limit.

Test References

See Test 1.3.4 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Physical Specification v1.0.

Test 1.3.5 HS Data TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation

The Output Differential Voltage Mismatch, ΔV_{OD} is defined as the difference of the absolute values of the differential output voltage in the Differential-1 state $V_{OD(1)}$ and the differential output voltage in the Differential-0 state $V_{OD(0)}$.

$$\Delta V_{OD} = \left| V_{OD(1)} \right| - \left| V_{OD(0)} \right|$$

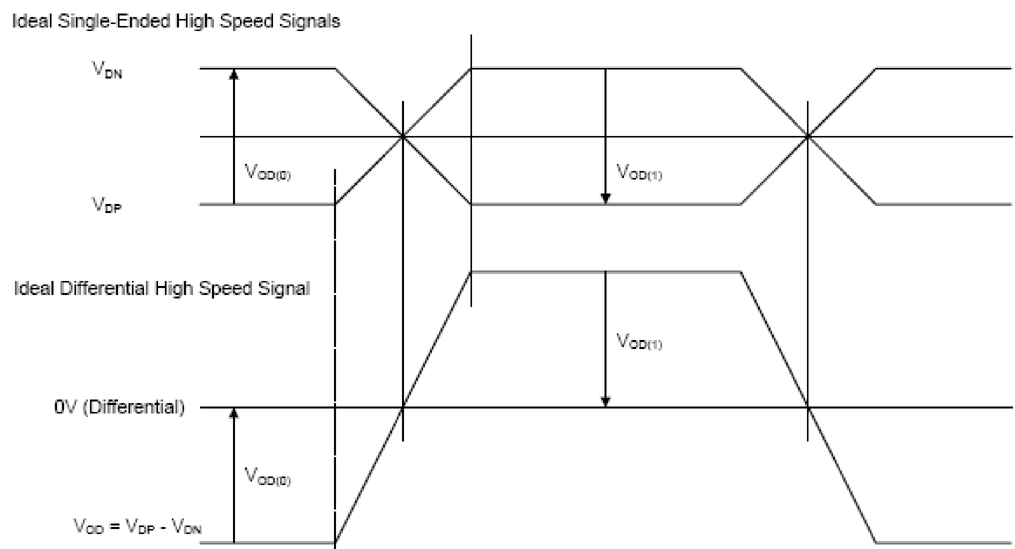

Figure 17 Ideal Single-Ended and Differential High Speed Signals

PASS Condition

The measured ΔV_{OD} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 6 Test Availability Condition for Test 1.3.5

Associated Test IDs		8141
Conditions		
HS Data Rate		Not applicable
Continuous Data		Not applicable
Continuous Clock		Not applicable
Data LP EscapeMode		Not applicable
Clock LP EscapeMode		Not applicable
Clock ULPS Mode		Not applicable
Informative Test		Not applicable
Probing Methods	**Active Probe (Differential Probe)**	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock and Continuous Data settings
	Direct Connect	Availability dependent on Continuous Clock and Continuous Data settings

Measurement Algorithm using Test ID 8141

HS Data TX Differential Voltage Mismatch (Pulse)

NOTE Use the Test ID# 8141 to remotely access the test.

1 This test requires the following prerequisite tests:
   - HS Data TX Differential Voltage (V_{OD0} Pulse) (Test ID: 8131)
   - HS Data TX Differential Voltage (V_{OD1} Pulse) (Test ID: 8132)
   - The actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.

2 Calculate the difference between V_{OD} for Differential-1 and Differential-0.

3 Report the measurement results:
   - V_{OD} for Differential-1 and Differential-0

4 Compare the measured ΔV_{OD} between Differential-1 and Differential-0 value to the compliance test limit.

Test References

See Test 1.3.5 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation

The output voltages V_{DP} and V_{DN} at the Dp and Dn pins should not exceed the High-Speed output high voltage, V_{OHHS}. V_{OLHS} is the High-Speed output, low voltage on Dp and Dn, and is determined by V_{OD} and V_{CMTX}. The High-Speed V_{OUT} is bounded by the minimum value of V_{OLHS} and the maximum value of V_{OHHS}.

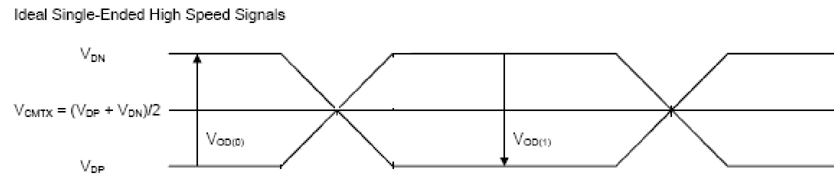

Figure 18 Ideal Single-Ended High Speed Signals

PASS Condition

The measured V_{OHHS} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 7 Test Availability Condition for Test 1.3.6

Associated Test IDs		8151	8152	8153
Conditions				
HS Data Rate		Not applicable	Not applicable	Not applicable
Continuous Data		Not applicable	Not applicable	Not applicable
Continuous Clock		Not applicable	Not applicable	Not applicable
Data LP EscapeMode		Not applicable	Not applicable	Not applicable
Clock LP EscapeMode		Not applicable	Not applicable	Not applicable
Clock ULPS Mode		Not applicable	Not applicable	Not applicable
Informative Test		Not applicable	Not applicable	Not applicable
Probing Methods	**Active Probe (Differential Probe)**	Available	Available	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock and Continuous Data settings	Availability dependent on Continuous Clock and Continuous Data settings	Availability dependent on Continuous Clock and Continuous Data settings
	Direct Connect	Not available	Not available	Not available
VOHHS Acquisition Method	**Single Acquisition**	Available	Not available	Not available
	Separated Acquisition	Not available	Available	Available

Measurement Algorithm using Test ID 8151

HS Data TX Single Ended Output High Voltage (V_{OHHS} Pulse)

NOTE Use the Test ID# 8151 to remotely access the test.

1 Trigger at SoT of HS Data burst (LP11 to LP01).
2 Find the HS Data Bursts.
3 The acquired single-ended Dp and Dn waveform is searched for the reference data pattern of “011111”.
4 The averaged waveform that consists of all the reference data patterns found is generated for Dp and Dn.
5 The mean value for the histogram window that falls between the centers of the fourth and fifth '1' bits is measured as the mean V_{OHHS} value for each single-ended HS Data signal and denotes each value as V_{OHHS} (Dp) and V_{OHHS} (Dn) using the **Histogram** function.
6 Report the measurement results:
   - V_{OHHS}(Dp)
   - V_{OHHS}(Dn)
   - Worst V_{OHHS} value
7 Compare the worst V_{OHHS} value to the compliance test limits.

Measurement Algorithm using Test ID 8152

HS Data TX Single Ended Output High Voltage ($V_{OHHS(Dp)}$ Pulse)

NOTE Use the Test ID# 8152 to remotely access the test.

1 Trigger at SoT of HS Data burst (LP11 to LP01).
2 Find the HS Data Bursts.
3 The acquired single-ended Dp is searched for the reference data pattern of “011111”.
4 The averaged waveform that consists of all the reference data patterns found is generated for Dp.
5 The mean value for the histogram window that falls between the centers of the fourth and fifth '1' bits is measured as the mean V_{OHHS} value for Dp signal and denotes each value as $V_{OHHS(Dp)}$ using the **Histogram** function.
6 Report the measurement results:
   - V_{OHHS}(Dp)
7 Compare the worst V_{OHHS} value to the compliance test limits.

Measurement Algorithm using Test ID 8153

HS Data TX Single Ended Output High Voltage ($V_{OHHS(Dn)}$ Pulse)

NOTE **Use the Test ID# 8153 to remotely access the test.**

1 Trigger at SoT of HS Data burst (LP11 to LP01).
2 Find the HS Data Bursts.
3 The acquired single-ended Dn is searched for the reference data pattern of “011111”.
4 The averaged waveform that consists of all the reference data patterns found is generated for Dn.
5 The mean value for the histogram window that falls between the centers of the fourth and fifth '1' bits is measured as the mean V_{OHHS} value for Dn signal and denotes each value as $V_{OHHS(Dn)}$ using the **Histogram** function.
6 Report the measurement results:
   - $V_{OHHS(Dn)}$
   - Worst V_{OHHS} value
7 Compare the worst V_{OHHS} value to the compliance test limits.

Test References

See Test 1.3.6 in CTS v1.0 (16Sept2010) and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation

The rise time, t_R is defined as the transition time between 20% and 80% of the full HS signal swing. The driver must meet the t_R specifications for all the allowable Z_{ID}.

PASS Condition

The measured t_R value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 8 Test Availability Condition for Test 1.3.11

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
8110	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 8110

NOTE Use the Test ID# 8110 to remotely access the test.

1 This test requires the following prerequisite tests:
   - *a* HS Clock Instantaneous (UI_{inst})[Max] (Test ID: 911): UI value measurements for test signal are performed and test results are stored.
   - *b* HS Data TX Differential Voltage (V_{OD}) (Test ID: 8131, 8132): Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
2 Trigger on SoT of HS Data burst (LP11->LP01).
3 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform using the following equation:

DataDiff = Dp-Dn

4 Define the measurement threshold as follows:

   Top Level: V_{OD1} (V_{OD} for Differential-1)

   Base Level: V_{OD0} (V_{OD} for Differential-0)

5 Use a MATLAB script to identify and extract all the “000111” pattern locations found in the differential signal.
6 Measure the 20%-80% rise time at all the rising edges of the “000111” pattern that is identified.
7 Compare the measured t_R (Mean) value with the maximum and minimum conformance test limits.

Test References

See Test 1.3.11 in CTS v1.0 and Section 9.1.1 Table 17 in the D-PHY Specification v1.0.

Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation

The fall time, t_F is defined as the transition time between 80% and 20% of the full HS signal swing. The driver must meet the t_F specifications for all the allowable Z_{ID}.

PASS Condition

The measured t_F value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 9 Test Availability Condition for Test 1.3.12

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
8111	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 8111

NOTE Use the Test ID# 81111 to remotely access the test.

1 This test requires the following prerequisite tests:
   a HS Clock Instantaneous (UI_{inst})[Max] (Test ID: 911)
   UI value measurements for test signal are performed and test results are stored.
   b HS Data TX Differential Voltage (V_{OD}) (Test ID: 8131, 8132)
   Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
2 Trigger on SoT of the HS Data burst (LP11->LP01).
3 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform using the following equation:

DataDiff = Dp-Dn

4 Define the measurement threshold as follows:

   Top Level: V_{OD1} (V_{OD} for Differential-1)

   Base Level: V_{OD0} (V_{OD} for Differential-0)
5 Use a MATLAB script to identify and extract all the “111000” pattern locations found in the differential signal.
6 Measure the 80%-20% fall time at all the falling edges of the “111000” pattern that is identified.
7 Compare the measured value of t_F (Mean) with the maximum and minimum conformance test limits.

Test References

See Test 1.3.12 in CTS v1.0 and Section 9.1.1 Table 17 in the D-PHY Specification v1.0.

5 MIPI D-PHY 1.0 High Speed Clock Transmitter (HS Clock TX) Electrical Tests

Probing for High Speed Clock Transmitter Electrical Tests / 78
Test 1.4.7 HS Clock TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation / 80
Test 1.4.8 HS Clock TX VCMTX Mismatch ($\Delta V_{CMTX}(_{1,0})$) Method of Implementation / 82
Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz (ΔV_{CMTX}(HF)) Method of Implementation / 84
Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz (ΔV_{CMTX}(LF)) Method of Implementation / 86
Test 1.4.4 HS Clock TX Differential Voltage (V_{OD}) Method of Implementation / 89
Test 1.4.5 HS Clock TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation / 92
Test 1.4.6 HS Clock TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation / 94
Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation / 96
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Test 1.4.17 HS Clock Instantaneous Method of Implementation / 98

This section provides the Methods of Implementation (MOIs) for the High Speed Clock Transmitter (HS Clock T_X) Electrical tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

KEYSIGHT TECHNOLOGIES

Probing for High Speed Clock Transmitter Electrical Tests

When performing the HS Clock T_X tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the HS Clock T_X tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

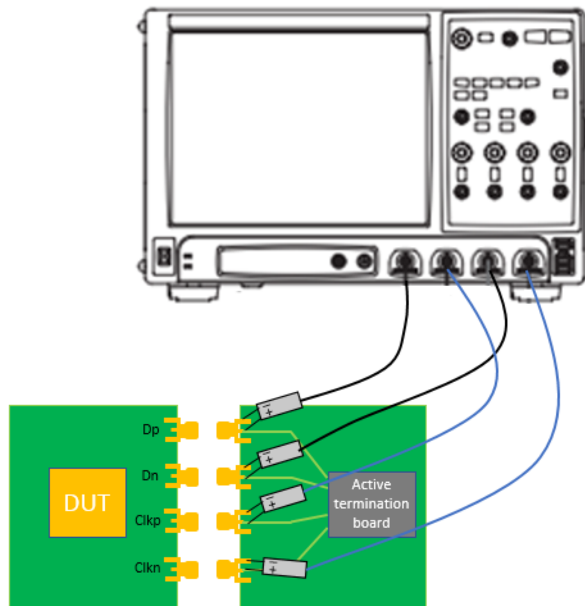

Figure 19 Probing for High Speed Clock Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 19 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, ZID (termination resistance), Cload, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

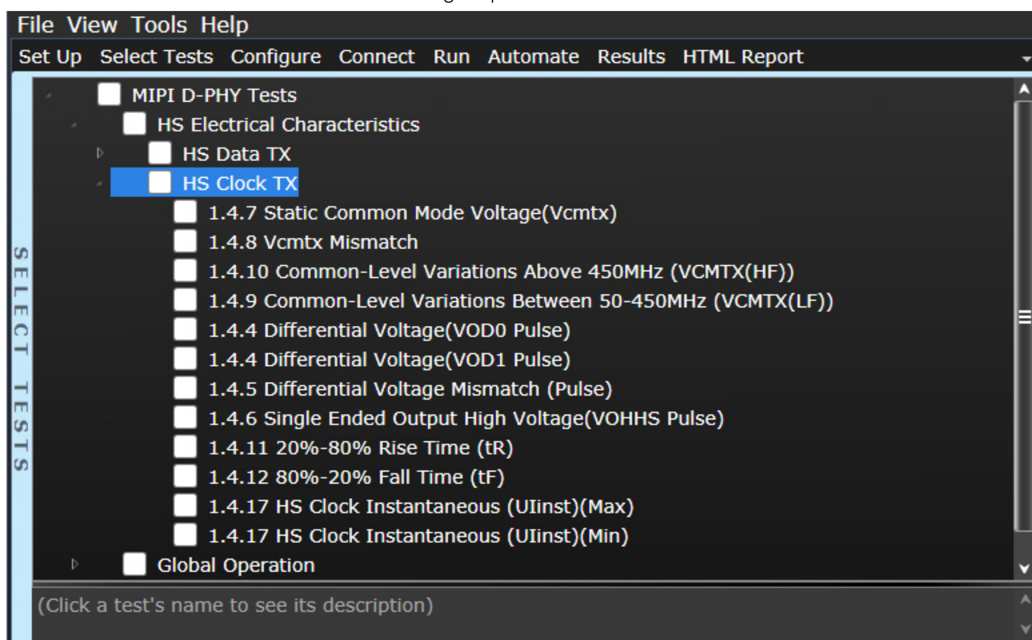

Figure 20 Selecting High Speed Clock Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.4.7 HS Clock TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation

The High Speed Clock Transmitter Common-Mode Voltage, V_{CMTX} is defined as the arithmetic mean value of the voltages at the Clkp and Clkn pins. Because of various types of signal distortion that may occur, it is possible for V_{CMTX} to have different values when a Differential-1 vs. Differential-0 state is driven.

For this test, the values for V_{CMTX} are measured for both the Differential-1 and Differential-0 states and averaged.

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

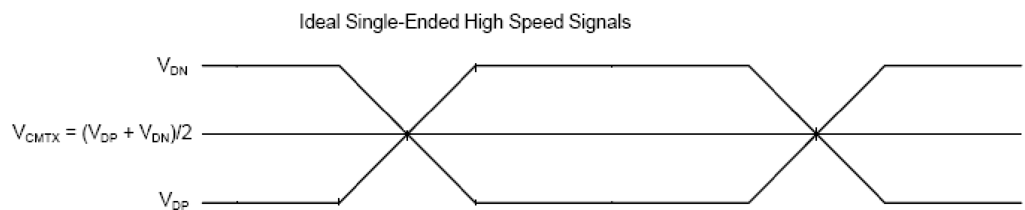

Figure 21 Ideal Single-Ended High Speed Signals

PASS Condition

The measured V_{CMTX} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 10 Test Availability Condition for Test 1.4.7

Associated Test IDs		1811
Conditions		
HS Data Rate		Not applicable
Continuous Data		Not applicable
Continuous Clock		Not applicable
Data LP EscapeMode		Not applicable
Clock LP EscapeMode		Not applicable
Clock ULPS Mode		Not applicable
Informative Test		Not applicable
Probing Methods	**Active Probe (Differential Probe)**	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock setting
	Direct Connect	Not available

Measurement Algorithm using Test ID 1811

NOTE

Use the Test ID# 1811 to remotely access the test.

1 Trigger the oscilloscope to acquire Clkp and Clkn.
2 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

3 Construct common-mode waveform by using the following equation:

ClkCommonMode = (Clkp+Clkn)/2

4 Sample the Common-Mode HS Clock waveform by using the center of the differential HS Clock's UI as sampler and denote as V_{CMTX}.
5 Separate the V_{CMTX} into 2 arrays; V_{CMTX} for Differential-1 and V_{CMTX} for Differential-0.
6 Report the measurement results:
   a Mean V_{CMTX} for Differential-1 and Differential-0
   b V_{CMTX} worst value between Differential-1 and Differential-0
7 Compare the measured V_{CMTX} worst value with the compliance test limits.

Test References

See Test 1.4.7 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1.4.8 HS Clock TX V_{CMTX} Mismatch ($\Delta V_{CMTX(1,0)}$) Method of Implementation

The common-mode voltage, V_{CMTX} is defined as the arithmetic mean value of the voltages at the Clkp and Clkn pins. Because of various types of signal distortion that may occur, it is possible for V_{CMTX} to have different values when a Differential-1 vs. Differential-0 state is driven.

For this $\Delta V_{CMTX(1,0)}$ test, the values for V_{CMTX} is measured for both the Differential-1 and Differential-0 states and averaged. The difference between the V_{CMTX} values for Differential-1 and Differential-0 is computed.

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2} \quad , \quad \Delta V_{CMTX(1,0)} = \frac{V_{CMTX(1)} - V_{CMTX(0)}}{2}$$

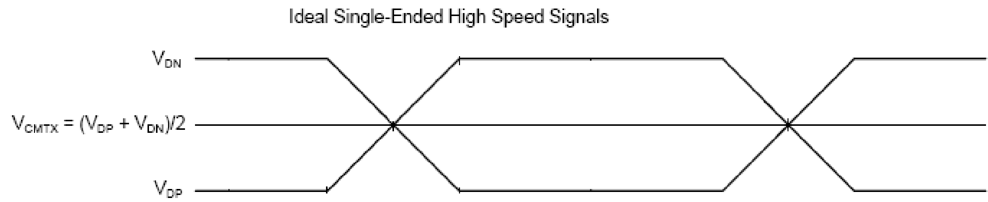

Figure 22 Ideal Single-Ended High Speed Signals.

PASS Condition

The measured $\Delta V_{CMTX(1,0)}$ value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 11 Test Availability Condition for Test 1.4.8

Associated Test IDs		1812
Conditions		
HS Data Rate		Not applicable
Continuous Data		Not applicable
Continuous Clock		Not applicable
Data LP EscapeMode		Not applicable
Clock LP EscapeMode		Not applicable
Clock ULPS Mode		Not applicable
Informative Test		Not applicable
Probing Methods	**Active Probe (Differential Probe)**	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock setting
	Direct Connect	Not available

Measurement Algorithm for Test ID 1812

NOTE Use the Test ID# 1812 to remotely access the test.

1 This test requires the following prerequisite tests.

   a HS Clock TX Static Common Mode Voltage (V_{CMTX}) (Test ID: 1811)

   The actual V_{CMTX} for Differential-1 and Differential-0 measurements are performed and test results are stored.

2 Calculate the V_{CMTX} mismatch using the following equation:

$$V_{CMTX} \text{ Mismatch} = ([V_{CMTX} \text{ for Differential-1}] - [V_{CMTX} \text{ for Differential-0}])/2$$

3 Report the measurement results.

   a V_{CMTX} for Differential-1 and Differential-0

   b V_{CMTX} Mismatch

4 Compare the measured ΔV_{CMTX} to the compliance test limit.

Test References

See Test 1.4.8 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz ($\Delta V_{CMTX(HF)}$) Method of Implementation

For this $\Delta V_{CMTX(HF)}$ test, the common mode voltage, V_{CMTX} is obtained by using the following equation:

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

Ideally, the common mode voltage should be as shown in Figure 23. In reality, various types of distortion could take place, as shown in Figure 24.

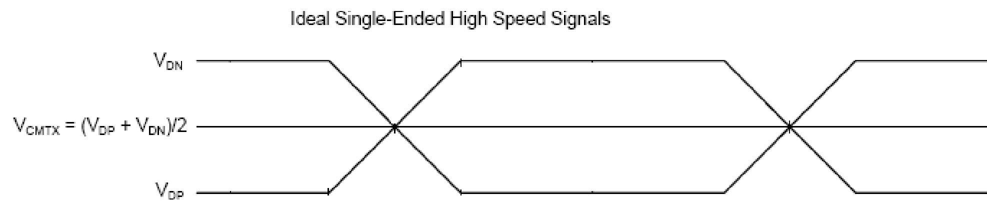

Figure 23 Ideal Single-Ended High Speed Signals

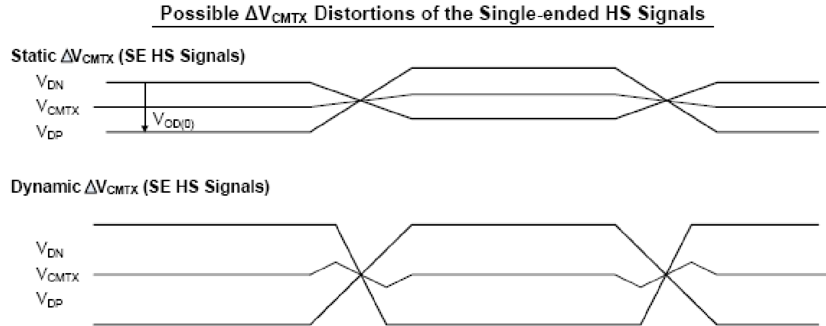

Figure 24 Possible Distortions of the ΔV_{CMTX} Single-Ended High Speed Signals

PASS Condition

The measured $\Delta V_{CMTX(HF)}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 12 Test Availability Condition for Test 1.4.10

Associated Test IDs		1818
Conditions		
HS Data Rate		Not applicable
ZID		100 ohms
Continuous Data		Not applicable
Continuous Clock		Not applicable
Data LP EscapeMode		Not applicable
Clock LP EscapeMode		Not applicable
Clock ULPS Mode		Not applicable
Informative Test		Not applicable
Probing Methods	**Active Probe (Differential Probe)**	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock setting
	Direct Connect	Not available

Measurement Algorithm using Test ID 1818

NOTE: Use the Test ID# 1818 to remotely access the test.

1 Trigger the oscilloscope to acquire Clkp and Clkn.
2 Construct common-mode waveform using the following equation:

   ClkCommonMode = (Clkp+Clkn)/2

3 Applies the single pole high pass filter with 3dB bandwidth frequency at 450MHz to the common-mode waveform.
4 Measure the RMS voltage for the filtered waveform and record as $\Delta V_{CMTX(HF)}$.
5 Report the measurement results:
   a $\Delta V_{CMTX(HF)}$ value
6 Compare the measured $\Delta V_{CMTX(HF)}$ value with the compliance test limit.

Test References

See Test 1.4.10 in CTS v1.0 and Section 8.1.1 Table 17 in the D-PHY Specification v1.0.

Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz ($\Delta V_{CMTX(LF)}$) Method of Implementation

For this $\Delta V_{CMTX(LF)}$ test, the common mode voltage V_{CMTX} is obtained by using the following equation:

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

Ideally, the common mode voltage should be as shown in Figure 25. In reality, various types of distortion could take place, as shown in Figure 26.

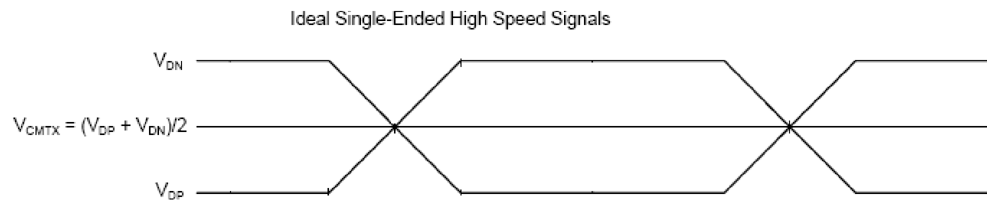

Figure 25 Ideal Single-Ended High Speed Signals

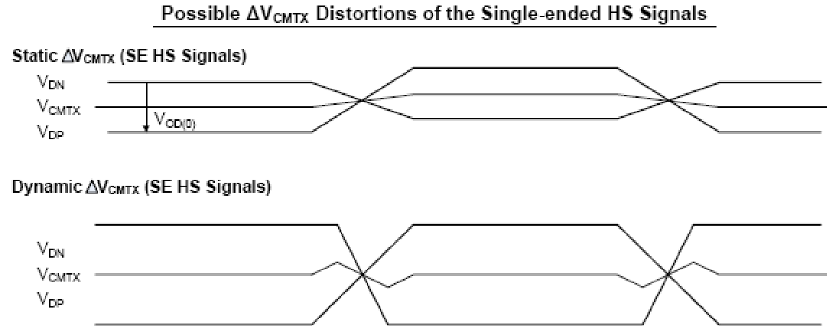

Figure 26 Possible Distortions of the ΔV_{CMTX} Single-Ended High Speed Signals

PASS Condition

The measured $\Delta V_{CMTX(LF)}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 13 Test Availability Condition for Test 1.4.9

Associated Test IDs		1819	1820
Conditions			
CTS		v1.0, v1.1	v1.2, v2.0, and v2.1
HS Data Rate		Not applicable	Not applicable
ZID		100 ohms	100 ohms
Continuous Data		Not applicable	Not applicable
Continuous Clock		Not applicable	Not applicable
Data LP EscapeMode		Not applicable	Not applicable
Clock LP EscapeMode		Not applicable	Not applicable
Clock ULPS Mode		Not applicable	Not applicable
Informative Test		Not applicable	Not applicable
Probing Methods	**Active Probe (Differential Probe)**	Available	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock setting	Availability dependent on Continuous Clock setting
	Direct Connect	Not available	Not available

Measurement Algorithm using Test ID 1819

NOTE Use the Test ID #1819 or #1820 to remotely access the test.

1 Trigger the oscilloscope to acquire Clkp and Clkn.

2 Construct common-mode waveform by using the following equation:

ClkCommonMode = (Clkp + Clkn)/2

3 A band pass filter with 3 dB bandwidth frequency at 50 MHz and 450 MHz will be applied to the common-mode waveform.

4 Measure the min and max voltage for the filtered waveform.

5 Select the worst absolute value for the min and max voltage and record it as $\Delta V_{CMTX(LF)}$.

6 Report the measurement results:

a $\Delta V_{CMTX(LF)}$ value

7 Compare the measured $\Delta V_{CMTX(LF)}$ value with the compliance test limit.

Test References

See D-PHY Specification v1.0, Section 8.1.1, Table 17, CTS v1.0(Test 1.4.9)

See D-PHY Specification v1.1, Section 9.1.1, Table 17, CTS v1.1(Test 1.4.9)

Measurement Algorithm using Test ID 1820

NOTE **Use the Test ID# 1820 to remotely access the test.**

1 Trigger the scope to acquire Datp. Datn, Clkp, and Clkn.

2 Construct common-mode waveform by using the following equation:

ClkCommonMode = (Clkp + Clkn)/2

3 Using post processing, find clock common-mode waveform location where Datp and Datn are operated in HS mode.

4 A band pass filter with 3 dB bandwidth frequency at 50 MHz and 450 MHz will be applied to the common-mode waveform.

5 Measure the min and max voltage for the filtered waveform.

6 Select the worst absolute value for the min and max voltage and record it as $\Delta V_{CMTX(LF)}$.

7 Report the measurement results:

a $\Delta V_{CMTX(LF)}$ value

8 Compare the measured $\Delta V_{CMTX(LF)}$ value with the compliance test limit.

Test References

See D-PHY Specification v1.2, Section 9.1.1, Table 20, CTS v1.2(Test 1.4.9)

See D-PHY Specification v2.1, Section 9.1.1, Table 26

Test 1.4.4 HS Clock TX Differential Voltage (V_{OD}) Method of Implementation

The Output Differential Voltage, V_{OD} is defined as the difference of voltages V_{DP} and V_{DN} at the Dp and Dn pins, respectively.

$$V_{OD} = V_{DP} - V_{DN}$$

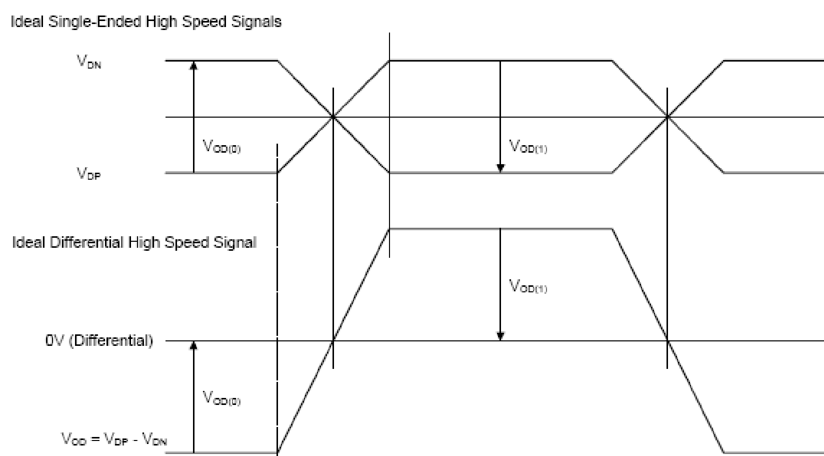

Figure 27 Ideal Single-Ended and Differential High Speed Signals

PASS Condition

The measured V_{OD} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 14 Test Availability Condition for Test 1.4.4

Associated Test IDs		18131	18132
Conditions			
HS Data Rate		Not applicable	Not applicable
Continuous Data		Not applicable	Not applicable
Continuous Clock		Not applicable	Not applicable
Data LP EscapeMode		Not applicable	Not applicable
Clock LP EscapeMode		Not applicable	Not applicable
Clock ULPS Mode		Not applicable	Not applicable
Informative Test		Not applicable	Not applicable
Probing Methods	**Active Probe (Differential Probe)**	Available	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock setting	Availability dependent on Continuous Clock setting
	Direct Connect	Availability dependent on Continuous Clock setting	Availability dependent on Continuous Clock setting

Measurement Algorithm using Test IDs 18131 and 18132

HS Clock TX Differential Voltage (V_{OD0} Pulse)

NOTE Use the Test ID# 18131 to remotely access the test.

HS Clock TX Differential Voltage (V_{OD1} Pulse)

NOTE Use the Test ID# 18132 to remotely access the test.

1 Trigger the oscilloscope to acquire Clkp and Clkn.
2 Construct the differential waveform using the following equation:

ClkDiff = Clkp-Clkn

3 Search the acquired waveform for the reference data pattern of “01” for V_{OD1} and “10” for V_{OD0} separately.
4 Generate the average waveform that consists of the reference data patterns.
5 Measure the mean value for the histogram window that falls between the centers of the ‘1’ bits as the Mean V_{OD1} value using the histogram function. For V_{OD0}, set the histogram window to measure the centers of the ‘0’ bits.
6 Report the measurement results
   - Mean V_{OD} for Differential-1 and Differential-0
7 Compare the mean V_{OD} value to the compliance test limits.

Test References

See Test 1.4.4 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1.4.5 HS Clock TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation

The output differential voltage mismatch, ΔV_{OD} is defined as the difference of the absolute values of the differential output voltage in the Differential-1 state $V_{OD(1)}$ and the differential output voltage in the Differential-0 state $V_{OD(0)}$.

$$\Delta V_{OD} = \left|V_{OD(1)}\right| - \left|V_{OD(0)}\right|$$

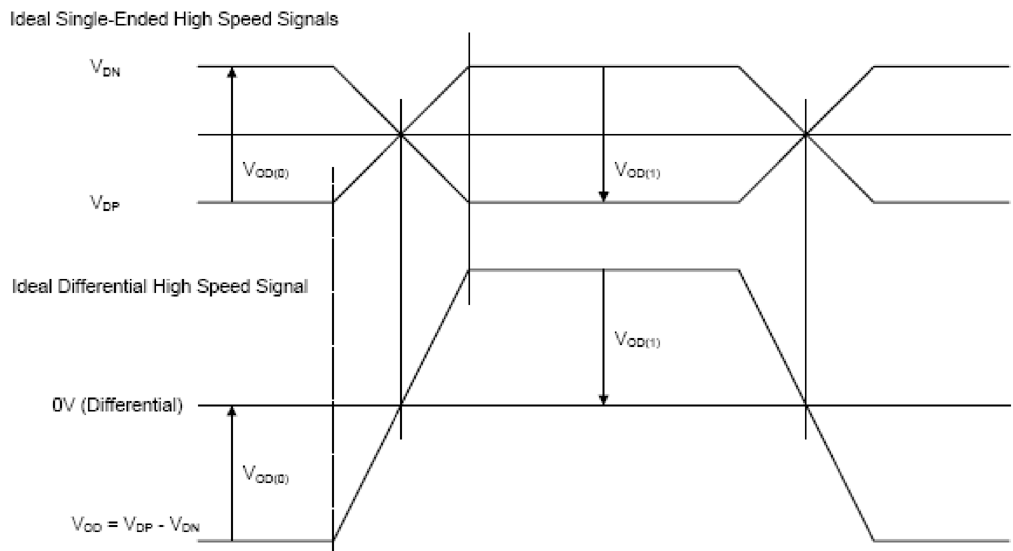

Figure 28 Ideal Single-Ended and Differential High Speed Signals.

PASS Condition

The measured ΔV_{OD} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 15 Test Availability Condition for Test 1.4.5

Associated Test IDs		18141
Conditions		
HS Data Rate		Not applicable
Continuous Data		Not applicable
Continuous Clock		Not applicable
Data LP EscapeMode		Not applicable
Clock LP EscapeMode		Not applicable
Clock ULPS Mode		Not applicable
Informative Test		Not applicable
Probing Methods	Active Probe (Differential Probe)	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock setting
	Direct Connect	Availability dependent on Continuous Clock setting

Measurement Algorithm using Test ID 18141

HS Clock TX Differential Voltage Mismatch (Pulse)

NOTE Use the Test ID# 18141 to remotely access the test.

1 This test requires the following prerequisite tests.

   a HS Clock TX Differential Voltage (V_{OD0} Pulse) (Test ID: 18131)

   b HS Clock TX Differential Voltage (V_{OD1} Pulse) (Test ID: 18132)

   The actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.

2 Calculate the difference between V_{OD} for Differential-1 and Differential-0.

3 Report the measurement results.

   a V_{OD} for Differential-1 and Differential-0

4 Compare the measured ΔV_{OD} between Differential-1 and Differential-0 value with the compliance test limit.

Test References

See Test 1.4.5 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1.4.6 HS Clock TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation

The output voltages V_{DP} and V_{DN} at the Clkp and Clkn pins should not exceed the High-Speed output high voltage, V_{OHHS}. V_{OLHS} is the High-Speed output, low voltage on Clkp and Clkn and is determined by V_{OD} and V_{CMTX}. The High-Speed V_{OUT} is bounded by the minimum value of V_{OLHS} and the maximum value of V_{OHHS}.

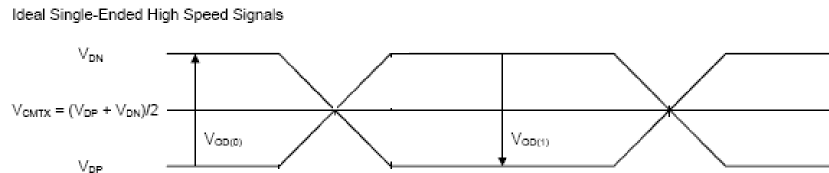

Figure 29 Ideal Single-Ended High Speed Signals

PASS Condition

The measured V_{OHHS} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 16 Test Availability Condition for Test 1.4.6

Associated Test IDs		18151
Conditions		
HS Data Rate		Not applicable
Continuous Data		Not applicable
Continuous Clock		Not applicable
Data LP EscapeMode		Not applicable
Clock LP EscapeMode		Not applicable
Clock ULPS Mode		Not applicable
Informative Test		Not applicable
Probing Methods	Active Probe (Differential Probe)	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock setting
	Direct Connect	Not available

Measurement Algorithm using Test ID 18151

HS Clock TX Single Ended Output High Voltage (V_{OHHS} Pulse)

NOTE Use the Test ID# 18151 to remotely access the test.

1. The acquired single-ended Clkp and Clkn waveform is searched for the reference data pattern of “01”.
2. The averaged waveform that consists of all the reference data patterns found are generated for Clkp and Clkn.
3. Measures the mean value for the histogram window that fall between the centers of the '1' bits as the Mean V_{OHHS} value for each single-ended HS Clock signal and denote each value as V_{OHHS} (Clkp) and V_{OHHS} (Clkn), using the **Histogram** function.
4. Report the measurement results.
   - V_{OHHS} (Clkp)
   - V_{OHHS} (Clkn)
   - Worst V_{OHHS} value
5. Compare the worst V_{OHHS} value to the compliance test limits.

Test References

See Test 1.4.6 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation

The rise time, t_R is defined as the transition time between 20% and 80% of the full HS signal swing. The driver must meet the t_R specifications for all allowable Z_{ID}.

PASS Condition

The measured t_R value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 17 Test Availability Condition for Test 1.4.11

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
18110	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 18110

NOTE Use the Test ID# 18110 to remotely access the test.

1 This test requires the following prerequisite tests:
   a HS Clock Instantaneous (UI_{inst})[Max] (Test ID: 911)
   UI value measurements for test signal are performed and test results are stored.
   b HS Clock T_X Differential Voltage (V_{OD}) (Test ID: 18131, 18132)
   Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
2 Trigger the oscilloscope to acquire Clkp and Clkn.
3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

   Top Level: V_{OD1} (V_{OD} for Differential-1)

   Base Level: V_{OD0} (V_{OD} for Differential-0)
5 Use a MATLAB script to identify and extract all “01” pattern locations found in the differential signal.
6 Measure the 20%-80% rise time at all rising edges of the “01” pattern that is identified.
7 Compare the value of the measured t_R (Mean) with the maximum and minimum compliance test limits.

Test References

See Test 1.4.11 in CTS v1.0 and Section 9.1.1 Table 17 in the D-PHY Specification v1.0.

Test 1.4.12 Clock Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation

The fall time, t_F is defined as the transition time between 80% and 20% of the full HS signal swing. The driver must meet the t_F specifications for all allowable Z_{ID}.

PASS Condition

The measured t_F value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 18 Test Availability Condition for Test 1.4.12

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
18111	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 18111

NOTE: Use the Test ID# 18111 to remotely access the test.

1 This test requires the following prerequisite tests:
   - *a* HS Clock Instantaneous (UI_{inst})[Max] (Test ID: 911)
     UI value measurements for test signal are performed and test results are stored.
   - *b* HS Clock T_X Differential Voltage (V_{OD}) (Test ID: 18131, 18132)
     Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.

2 Trigger the oscilloscope to acquire Clkp and Clkn.

3 Construct differential waveform by using the following equation:

   ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

   Top Level: V_{OD1} (V_{OD} for Differential-1)

   Base Level: V_{OD0} (V_{OD} for Differential-0)

5 Use a MATLAB script to identify and extract all “10” pattern locations found in the differential signal.

6 Measure the 80%-20% fall time at all falling edges of the “10” pattern that is identified.

7 Compare the value of the measured t_F (Mean) with the maximum and minimum compliance test limits.

Test References

See Test 1.4.12 in CTS v1.0 and Section 9.1.1 Table 17 in the D-PHY Specification v1.0.

Test 1.4.17 HS Clock Instantaneous Method of Implementation

The HS Clock instantaneous test verifies that the HS clock transmitted by clock TX during HS data burst does not exceed the required maximum value.

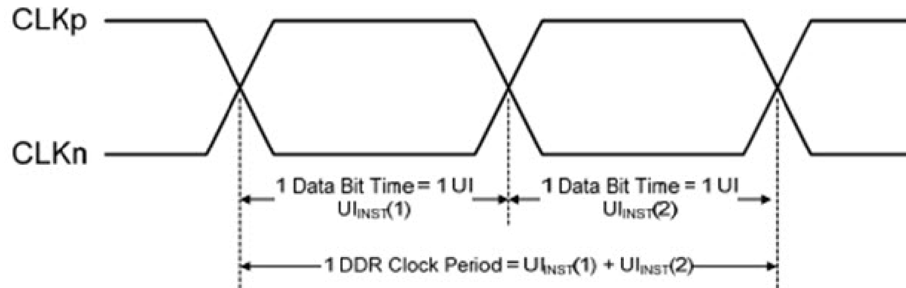

Figure 30 DDR Clock Definition

PASS Condition

The measured instantaneous UI must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 19 Test Availability Condition for Test 1.4.17

Associated Test IDs		911	914
Conditions			
HS Data Rate		Not applicable	Not applicable
ZID		100 ohms	100 ohms
Continuous Data		Not applicable	Not applicable
Continuous Clock		Not applicable	Not applicable
Data LP EscapeMode		Not applicable	Not applicable
Clock LP EscapeMode		Not applicable	Not applicable
Clock ULPS Mode		Not applicable	Not applicable
Informative Test		Not applicable	Not applicable
Probing Methods	**Active Probe (Differential Probe)**	Available	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock setting	Availability dependent on Continuous Clock setting
	Direct Connect	Availability dependent on Continuous Clock setting	Availability dependent on Continuous Clock setting

Measurement Algorithm using Test ID 911

HS Clock Instantaneous (UI_{inst}) [Max]

NOTE Use the Test ID# 911 to remotely access the test.

1 Capture the Clkp and Clkn waveform.
2 Construct the differential clock waveform using the following equation:

DiffClock = Clkp-Clkn

3 Measure the min, max and average Unit Interval of the differential clock waveform.
4 Store the min, max and average Unit Interval values.
5 Compare the max Unit Interval to the conformance limit.

Measurement Algorithm using Test ID 914

HS Clock Instantaneous (UI_{inst}) [Min]

NOTE Use the Test ID# 914 to remotely access the test.

1 Capture the Clkp and Clkn waveform.
2 Construct the differential clock waveform using the following equation:

DiffClock = Clkp-Clkn

3 Measure the min, max and average Unit Interval of the differential clock waveform.
4 Store the min, max and average Unit Interval values.
5 Compare the min Unit Interval to the conformance limit.

Test References

See Test 1.4.17 in CTS v1.0 and Section 9.1 Table 26 in the D-PHY Specification v1.0.

6 MIPI D-PHY 1.0 Low Power Data Transmitter (LP Data TX) Electrical Tests

Probing for Low Power Transmitter Electrical Tests / 102
Test 1.1.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation / 104
Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation / 106
Test 1.1.3 LP TX 15%-85% Rise Time Level (T_{RLP}) EscapeMode Method of Implementation / 108
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Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock ($T_{LP-PULSE-TX}$) Method of Implementation / 111
Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock ($T_{LP-PER-TX}$) Method of Implementation / 114
Test 1.1.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation / 116

This section provides the Methods of Implementation (MOIs) for the Low Power Data Transmitter (LP Data TX) Electrical tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

Probing for Low Power Transmitter Electrical Tests

When performing the LP TX tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the LP TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test Application for the exact number of probe connections.

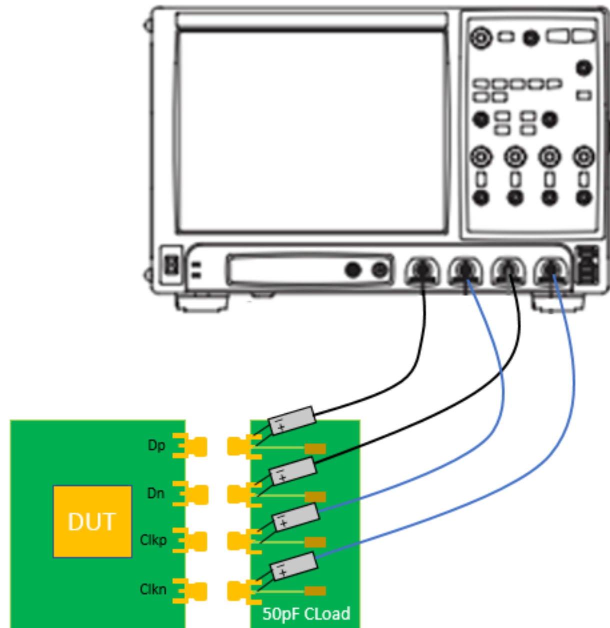

Figure 31 Probing for Low Power Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 31 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, ZID (termination resistance), Cload, Device ID and User Comments.
4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

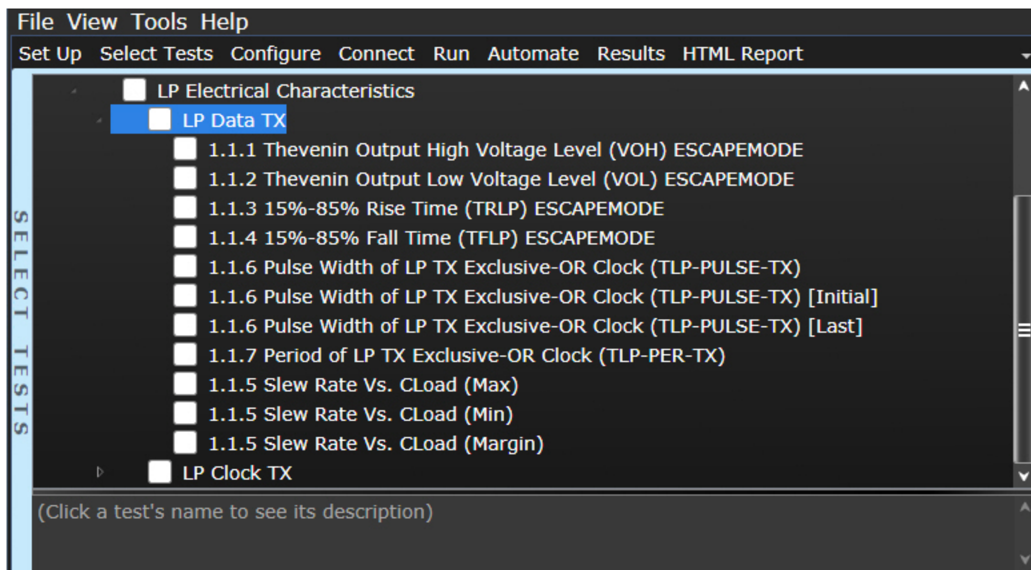

Figure 32 Selecting Low Power Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app’s task flow to set up the configuration options, run the tests and view the tests results.

Test 1.1.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation

V_{OH} is the Thevenin output high-level voltage in the high-level state, when the pad pin is not loaded.

PASS Condition

The measured V_{OH} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 20 Test Availability Conditions for Test 1.1.1

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
821	Not Applicable	Disabled	Not Applicable	Disabled	Not Applicable	Not Applicable	Enabled	Active Probe (Differential Probe)
8211	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 821

LP TX Thevenin Output High Voltage Level (V_{OH}) (Informative)

NOTE: Ensure that **Data LP EscapeMode** is disabled and **Informative Test** is enabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application. Use the Test ID# 821 to remotely access the test.

1 Trigger the Dp’s LP rising edge.
2 Position the trigger point at the center of the screen and make sure that the stable Dp LP high level voltage region is visible on the screen.
3 Accumulate the data using the persistent display mode.
4 Enable the **Histogram** feature and measure the entire display region after the trigger location.
5 Take the mode value from the **Histogram** and use this value as V_{OH} for Dp.
6 Repeat steps 1 to 6 for Dn.
7 Report the measurement results.
   a V_{OH} value for Dp channel
   b V_{OH} value for Dn channel
8 Compare the measured worst value of V_{OH} with the compliance test limits.

Measurement Algorithm using Test ID 8211

LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE

NOTE Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8211 to remotely access the test.

1 Trigger on LP Data EscapeMode pattern on the data signal. Without the presence of LP Escape mode, the trigger is unable to capture any valid signal for data processing.
2 Locate and use the Mark-1 state pattern to determine the end of the EscapeMode sequence.
3 Enable the **Histogram** feature and measure the entire LP Data EscapeMode sequence.
4 Take the mode value from the **Histogram** and use this value as V_{OH} for Dp.
5 Repeat steps 1 to 5 for Dn.
6 Report the measurement results.
   a V_{OH} value for Dp channel
   b V_{OH} value for Dn channel
7 Compare the measured worst value of V_{OH} with the conformance test limits.

Test References

See Test 1.1.1 in CTS v1.0 and Section 8.12 Table 18 in the D-PHY Specification v1.0.

Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation

V_{OL} is the Thevenin output low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low level state.

PASS Condition

The measured V_{OL} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 21 Test Availability Condition for Test 1.1.2

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
822	Not Applicable	Disabled	Not Applicable	Disabled	Not Applicable	Not Applicable	Enabled	Active Probe (Differential Probe)
8221	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 822

LP TX Thevenin Output Low Voltage Level (V_{OL}) (Informative)

NOTE Ensure that **Data LP EscapeMode** is disabled and **Informative Test is** enabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application. Use the Test ID# 822 to remotely access the test.

1 This test requires the following prerequisite test(s):
   a HS Entry: DATA TX $T_{HS-PREPARE}$ (Test ID: 557)
2 Trigger the Dp's LP falling edge.
3 Position the trigger point at the center of the screen and make sure that the stable Dp LP low level voltage region is visible on the screen.
4 Accumulate the data by using the persistent display mode.
5 Enable the **Histogram** feature and measure the entire display region after the trigger location.
6 Take the mode value from the **Histogram** and use this value as V_{OL} for Dp.
7 Repeat steps 1 to 7 for Dn.
8 Report the measurement results:
   a V_{OL} value for Dp channel
   b V_{OL} value for Dn channel
9 Compare the measured worst value of V_{OL} with the conformance test limits.

Measurement Algorithm using Test ID 8221

LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE

NOTE Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8221 to remotely access the test.

1 This test requires the following prerequisite tests:
   a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
2 Trigger on LP Data EscapeMode pattern on the data signal. Without the presence of the LP Escape mode, the trigger is unable to capture any valid signal for data processing.
3 Locate and use the Mark -1 state pattern to determine the end of the EscapeMode sequence.
4 Enable the **Histogram** feature and measure the entire LP data EscapeMode sequence.
5 Take the mode value from the **Histogram** and use this value as V_{OL} for Dp.
6 Repeat steps 1 to 6 for Dn.
7 Report the measurement results:
   a V_{OL} value for Dp channel
   b V_{OL} value for Dn channel
8 Compare the measured worst value of V_{OL} with the conformance test limits.

Test References

See Test 1.1.2 in CTS v1.0 and Section 8.1.2 Table 18 in the D-PHY Specification v1.0.

Test 1.1.3 LP TX 15%-85% Rise Time Level (T_{RLP}) EscapeMode Method of Implementation

The T_{RLP} is defined as 15%-85% rise time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD}. The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{RLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 22 Test Availability Condition for Test 1.1.3

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
8241	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 8241

NOTE Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8241 to remotely access the test.

1 This test requires the following prerequisite tests:
   a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
   b LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 8221)

   V_{OH} and V_{OL} values for Low Power signal measurements are performed and test results are stored.
2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3 All the rising edges in the EscapeMode sequence are processed in measuring the corresponding rise time.
4 The average 15%-85% rise time for Dp is recorded.
5 Repeat the steps for Dn.
6 Report the measurement results:
   a T_{RLP} average value for Dp channel
   b T_{RLP} average value for Dn channel
7 Compare the measured T_{RLP} worst value with the compliance test limit.

Test References

See Test 1.1.3 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

Test 1.1.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation

The T_{FLP} is defined as 15%-85% fall time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD}. The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{FLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 23 Test Availability Condition for Test 1.1.4

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
825	Not Applicable	Disabled	Not Applicable	Disabled	Not Applicable	Not Applicable	Enabled	Active Probe (Differential Probe)
8251	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 825

LP TX 15%-85% Fall Time (T_{FLP}) (Informative)

NOTE: Ensure that **Data LP EscapeMode** is disabled and **Informative Test** is enabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application. Use the Test ID# 825 to remotely access the test.

1 This test requires the following prerequisite tests:
   - *a* LP TX Thevenin Output High Voltage Level (V_{OH}) (Informative) (Test ID: 821)
   - *b* LP TX Thevenin Output Low Voltage Level (V_{OL}) (Informative) (Test ID: 822)

   Measure the V_{OH} and V_{OL} values for the low power signal and test results are stored.
2 All falling edges in LP are valid for this measurement.
3 Setup the trigger on LP falling edges.
4 Depending on the number of observation configuration, the oscilloscope is triggered accordingly.
5 The average 15%-85% fall time for Dp is recorded.
6 Repeat the same trigger steps for Dn.
7 Report the measurement results:
   - *a* T_{FLP} average value for Dp channel
   - *b* T_{FLP} average value for Dn channel
8 Compare the measured worst value of T_{FLP} with the compliance test limits.

Measurement Algorithm using Test ID 8251

LP TX 15%-85% Fall Time (T_{FLP}) ESCAPEMODE

NOTE Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8251 to remotely access the test.

1 This test requires the following prerequisite tests:
   a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
   b LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 8221)

   Measure the V_{OH} and V_{OL} values for the low power signal and test results are stored.
2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3 All falling edges in the filtered EscapeMode sequence are processed in measuring the corresponding fall time.
4 The average 15%-85% fall time for Dp is recorded.
5 Repeat steps 1 to 5 for Dn.
6 Report the measurement results:
   a T_{FLP} average value for Dp channel
   b T_{FLP} average value for Dn channel
7 Compare the measured worst value of T_{FLP} with the compliance test limits.

Test References

See Test 1.1.4 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock ($T_{LP-PULSE-TX}$) Method of Implementation

$T_{LP-PULSE-TX}$ is defined as the pulse width of the DUT Low-Power TX XOR clock. A graphical representation of the XOR operation that creates the LP clock is shown below. The D-PHY Standard actually separates the $T_{LP-PULSE-TX}$ specification into two parts:

a The first LP XOR clock pulse after a Stop state, or the last LP XOR clock pulse before a Stop state must be wider than 40ns.

b All other LP XOR clock pulses must be wider than 20ns.

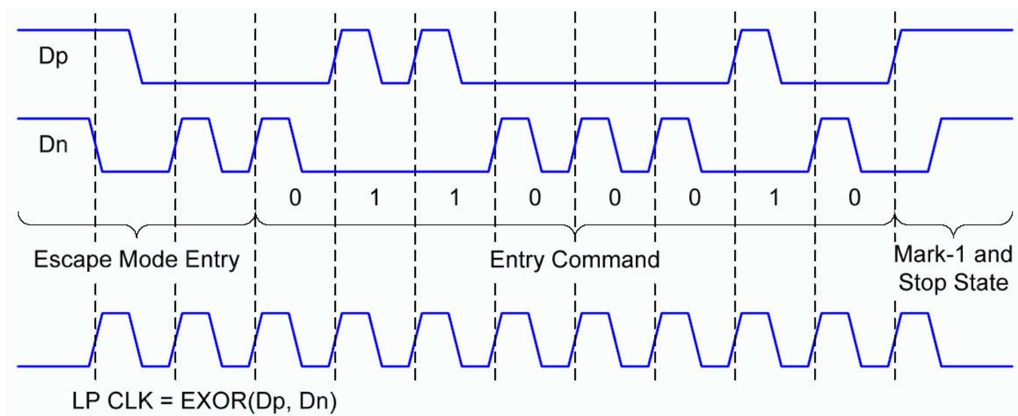

Figure 33 Graphical Representation of the XOR Operation

PASS Condition

The measured $T_{LP-PULSE-TX}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 24 Test Availability Condition for Test 1.1.6

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
827	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)
8271	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	
8272	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1827	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	Active Probe (Differential Probe)
18271	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	
18272	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	

Measurement Algorithm using Test IDs 827, 8271 and 8272

LP TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP\text{-}PULSE\text{-}TX}$)

NOTE Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 827 to remotely access the test.

LP TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP\text{-}PULSE\text{-}TX}$) [Initial]

NOTE Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8271 to remotely access the test.

LP TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP\text{-}PULSE\text{-}TX}$) [Last]

NOTE Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8272 to remotely access the test.

1 This test requires the following prerequisite tests:

   a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211).

   This is to trigger and capture an EscapeMode sequence data from the test signal.

2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.

3 Find all crossing points at the minimum trip level (500mV) and the maximum trip level (930mV) for Dp and Dn individually.

4 Find the initial pulse width, last pulse width and minimum width of all the other pulses at the specified minimum trip level and maximum trip level.

5 Find the rising-to-rising and falling-to-falling periods of the XOR clock at the mentioned minimum trip level and maximum trip level.

6 The worst case value for the pulse width found between the minimum trip level and maximum trip level will be used as the $T_{LP\text{-}PULSE\text{-}TX}$ value.

7 Compare the measured minimum $T_{LP\text{-}PULSE\text{-}TX}$ value with the compliance test limits.

Measurement Algorithm using Test IDs 1827, 18271 and 18272

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP\text{-}PULSE\text{-}TX}$)

NOTE Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 1827 to remotely access the test.

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP\text{-}PULSE\text{-}TX}$) [Initial]

NOTE Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 18271 to remotely access the test.

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP\text{-}PULSE\text{-}TX}$) [Last]

NOTE Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 18272 to remotely access the test.

1 This test requires the following prerequisite tests:
   a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
   This is to trigger and capture an EscapeMode sequence data from the test signal.
2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3 Find all crossing points at the minimum trip level (500mV) and the maximum trip level (930mV) for Clkp and Clkn individually.
4 Find the initial pulse width, last pulse width and minimum width of all the other pulses at the specified minimum trip level and maximum trip level.
5 Find the rising-to-rising and falling-to-falling periods of the XOR clock at the specified minimum trip level and maximum trip level.
6 The worst case value for the pulse width found between the minimum trip level and maximum trip level is used as the $T_{LP\text{-}PULSE\text{-}TX}$ value.
7 Compare the measured minimum $T_{LP\text{-}PULSE\text{-}TX}$ value with the compliance test limits.

Test References

See Test 1.1.6 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock ($T_{LP-PER-TX}$) Method of Implementation

$T_{LP-PER-TX}$ is defined as the period of the DUT Low-Power TX XOR clock. A graphical representation of the XOR operation that creates the LP clock is shown below. The D-PHY Standard separates the $T_{LP-PULSE-TX}$ specification into two parts:

a The first LP XOR clock pulse after a Stop state, or the last LP XOR clock pulse before a Stop state must be wider than 40ns.

b All other LP XOR clock pulses must be wider than 20ns.

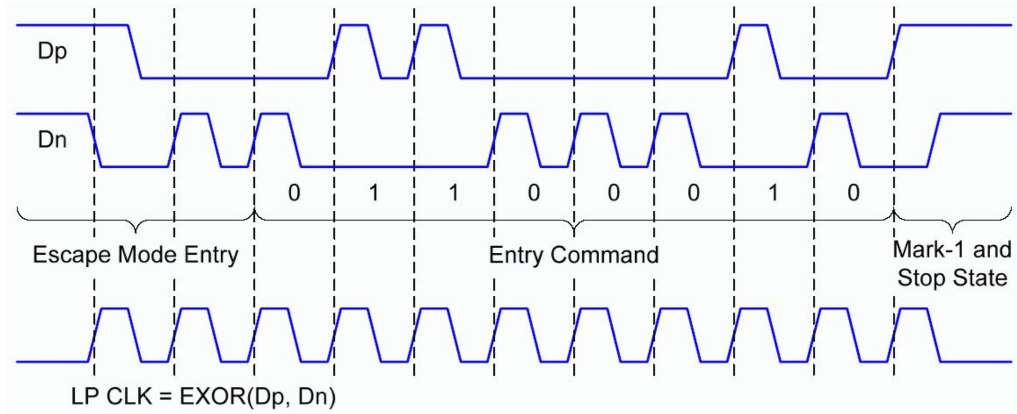

Figure 34 Graphical Representation of the XOR Operation

PASS Condition

The measured $T_{LP-PER-TX}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 25 Test Availability Condition for Test 1.1.7

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
828	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)
1828	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	

Measurement Algorithm using Test ID 828

LP TX Period of LP TX Exclusive-OR Clock ($T_{LP-PER-TX}$)

NOTE Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 828 to remotely access the test.

1 This test requires the following prerequisite test(s).
   a LP TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP-PULSE-TX}$) (Test ID: 827)

   The actual measurement algorithm of the $T_{LP-PER-TX}$ is performed in the mentioned prerequisite test.
2 The minimum value for all the rising-to-rising and falling-to-falling periods of the XOR clock at the minimum trip level (500mV) and the maximum trip level (930mV) is used as the $T_{LP-PER-TX}$ result.
3 Compare the measured minimum $T_{LP-PER-TX}$ value to the compliance test limits.

Measurement Algorithm using Test ID 1828

LP Clock TX Period of LP TX Exclusive-OR Clock ($T_{LP-PER-TX}$)

NOTE Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 1828 to remotely access the test.

1 This test requires the following prerequisite test(s).
   a LP Clock TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP-PULSE-TX}$) (Test ID: 1827)

   The actual measurement algorithm of the $T_{LP-PER-TX}$ is performed in the mentioned prerequisite test.
2 The minimum value for all the rising-to-rising and falling-to-falling periods of the XOR clock at the minimum trip level (500mV) and the maximum trip level (930mV) is used as the $T_{LP-PER-TX}$ result.
3 Compare the measured minimum $T_{LP-PER-TX}$ value with the compliance test limits.

Test References

See Test 1.1.7 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

Test 1.1.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation

The slew rate $\delta V/\delta t_{SR}$ is the derivative of the LP transmitter output signal voltage over time. The intention of specifying a maximum slew rate value in the specification is to limit EMI (Electro Magnetic Interference).

The specification also states that the Slew Rate must be measured as an average across any 50mV segment of the output signal transition.

PASS Condition

The measured slew rate $\delta V/\delta t_{SR}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 26 Test Availability Condition for Test 1.1.5

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
829	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)
8291	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	
8292	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	

Measurement Algorithm using Test IDs 829, 8291 and 8292

NOTE

Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test.

- To access the LP TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 829.
- To access the LP TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 8291.
- To access the LP TX Slew Rate Vs. C_{Load} (Margin) test remotely, use the Test ID# 8292.

1 This test requires the following prerequisite tests:
   a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
   b LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 8221)

   V_{OH} and V_{OL} values for low power signal measurements are performed and test results are stored.
2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3 Perform the slew rate measurement on the EscapeMode sequence for both Dp and Dn waveforms individually.
   For falling edge,
   a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
   b. Perform the slew rate measurement across the 400mV - 930mV region to determine the minimum slew rate result.
   For rising edge,
   a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.

b. Perform the slew rate measurement across the 400mV - 700mV region to determine the minimum slew rate result.
c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700mV - 930mV region.

4. Calculate the average value from all rising edges' maximum slew rate results. Calculate the average value from all falling edges' maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.
5. Calculate the average value from all rising edges' minimum slew rate results. Calculate the average value from all falling edges' minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
6. Calculate the average value from all rising edges' slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
7. The Slew Rate maximum, minimum and margin result values are stored.
8. Report the measurement results.
9. Compare the measured worst slew rate value with the conformance test limits.

Test References

See Test 1.1.5 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

7 MIPI D-PHY 1.0 Low Power Clock Transmitter (LP Clock TX) Electrical Tests

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Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation / 122
Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation / 124
Test 1.2.3 LP TX 15%-85% Rise Time Level (T_{RLP}) Method of Implementation / 126
Test 1.2.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation / 128
Test 1.2.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation / 131

This section provides the Methods of Implementation (MOIs) for the Low Power Clock Transmitter (LP Clock TX) Electrical tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

KEYSIGHT TECHNOLOGIES

Probing for Low Power Transmitter Electrical Tests

When performing the LP TX tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the LP TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test Application for the exact number of probe connections.

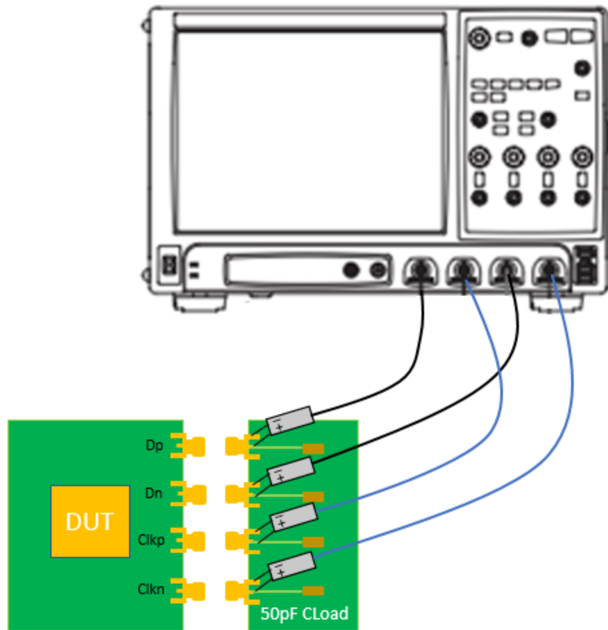

Figure 35 Probing for Low Power Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 35 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, ZID (termination resistance), Cload, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

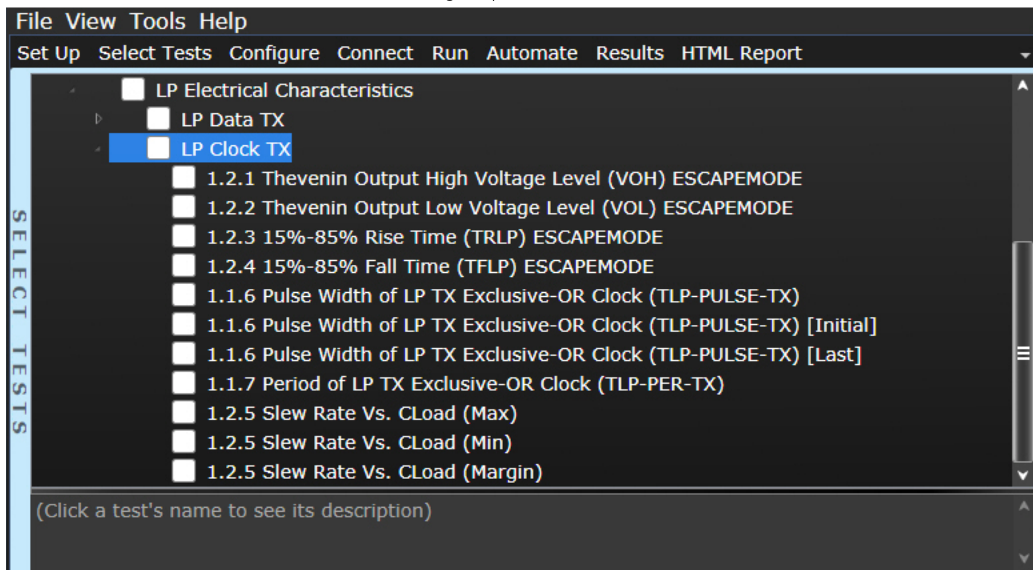

Figure 36 Selecting Low Power Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app’s task flow to set up the configuration options, run the tests and view the tests results.

Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation

V_{OH} is the Thevenin output high-level voltage in the high-level state, when the pad pin is not loaded.

PASS Condition

The measured V_{OH} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 27 Test Availability Condition for Test 1.2.1

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1821	Not Applicable	Not Applicable	Disabled	Not Applicable	Disabled	Disabled	Enabled	Active Probe (Differential Probe)
18211	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	
28211	Not Applicable	Not Applicable	Disabled	Not Applicable	Disabled	Enabled	Not Applicable	

Measurement Algorithm using Test ID 1821 and 28211

LP Clock TX Thevenin Output High Voltage Level (VOH) (Informative)

NOTE Ensure that the **Clock LP EscapeMode** and **Clock ULPS Mode** are disabled and **Informative Test** enabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application. Use the Test ID# 1821 to remotely access the test.

ULPS Clock TX Thevenin Output High Voltage Level (VOH) ULPSMODE

NOTE Select **Clock ULPS Mode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28211 to remotely access the test.

1 Trigger the Clkp's LP rising edge.
2 Position the trigger point at the center of the screen and make sure that the stable Clkp LP high level voltage region is visible on the screen.
3 Accumulate the data by using the persistent display mode.
4 Enable the **Histogram** feature and measure the entire display region after the trigger location.
5 Take the mode value from the **Histogram** and use this value as V_{OH} for Clkp.
6 Repeat steps 1 to 6 for Clkn.
7 Report the measurement results.
   a V_{OH} value for Clkp channel
   b V_{OH} value for Clkn channel
8 Compare the measured worst value of V_{OH} with the compliance test limits.

Measurement Algorithm using Test ID 18211

LP Clock TX Thevenin Output High Voltage Level (VOH) ESCAPEMODE

NOTE Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18211 to remotely access the test.

1. Trigger on an EscapeMode pattern on the data signal. Without the presence of the LP Escape mode, the trigger is unable to capture any valid signal for data processing.
2. Locate and use the Mark-1 state pattern to determine the end of the EscapeMode sequence.
3. Enable the **Histogram** feature and measure the entire LP EscapeMode sequence.
4. Take the mode value from the **Histogram** and use this value as V_{OH} for Clkp.
5. Repeat steps 1 to 4 for Clkn.
6. Report the measurement results.
   a V_{OH} value for Clkp channel
   b V_{OH} value for Clkn channel
7. Compare the measured worst value of V_{OH} with the compliance test limits.

Test References

See Test 1.2.1 in CTS v1.0 and Section 8.1.2 Table 18 in the D-PHY Specification v1.0.

Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation

V_{OL} is the Thevenin output low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low level state.

PASS Condition

The measured V_{OL} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 28 Test Availability Condition for Test 1.2.2

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1822	Not Applicable	Not Applicable	Disabled	Not Applicable	Disabled	Disabled	Enabled	Active Probe (Differential Probe)
18221	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	
28221	Not Applicable	Not Applicable	Disabled	Not Applicable	Disabled	Enabled	Not Applicable	

Measurement Algorithm using Test ID 1822

LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) (Informative)

NOTE: Ensure that the **Clock LP EscapeMode** and **Clock ULPS Mode** are disabled and **Informative Test** enabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application. Use the Test ID# 1822 to remotely access the test.

1 This test requires the following prerequisite tests:
   a HS Entry: CLK TX $T_{CLK-PREPARE}$ (Test ID: 552)
2 Trigger the Clkp's LP falling edge.
3 Position the trigger point at the center of the screen and make sure that the stable Clkp LP low level voltage region is visible on the screen.
4 Accumulate the data by using the persistent display mode.
5 Enable the **Histogram** feature and measure the entire display region after the trigger location.
6 Take the mode value from the **Histogram** and use this value as V_{OL} for Clkp.
7 Repeat steps 1 to 7 for Clkn.
8 Report the measurement results:
   a V_{OL} value for Clkp channel
   b V_{OL} value for Clkn channel
9 Compare the measured worst value of V_{OL} with the compliance test limits.

Measurement Algorithm using Test ID 18221

LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE

NOTE Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18221 to remotely access the test.

1 This test requires the following prerequisite tests:
   a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
2 Trigger on an EscapeMode pattern on the data signal. Without the presence of LP Escape mode, the trigger is unable to capture any valid signal for data processing.
3 Locate and use the Mark -1 state pattern to determine the end of the EscapeMode sequence.
4 Enable the **Histogram** feature and measure the entire LP EscapeMode sequence.
5 Take the mode value from the **Histogram** and use this value as V_{OL} for Clkp.
6 Repeat steps 1 to 6 for Clkn.
7 Report the measurement results:
   a V_{OL} value for Clkp channel
   b V_{OL} value for Clkn channel
8 Compare the measured worst value of V_{OL} with the compliance test limits.

Measurement Algorithm using Test ID 28221

ULPS Clock TX Thevenin Output Low Voltage Level (V_{OL}) ULPSMODE

NOTE Select **Clock ULPS Mode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28221 to remotely access the test.

1 This test requires the following prerequisite test(s):
   a ULPS Clock TX Thevenin Output High Voltage Level (VOH) ULPSMODE (Test ID: 28211)
2 Trigger the Clkp's LP falling edge.
3 Position the trigger point at the center of the screen and make sure that the stable Clkp LP low level voltage region is visible on the screen.
4 Accumulate the data by using the persistent display mode.
5 Enable the **Histogram** feature and measure the entire display region after the trigger location.
6 Take the mode value from the **Histogram** and use this value as V_{OL} for Clkp.
7 Repeat steps 1 to 7 for Clkn.
8 Report the measurement results:
   a V_{OL} value for Clkp channel
   b V_{OL} value for Clkn channel
9 Compare the measured worst value of V_{OL} with the conformance test limits.

Test References

See Test 1.2.2 in CTS v1.0 and Section 8.1.2 Table 18 in the D-PHY Specification v1.0.

Test 1.2.3 LP TX 15%-85% Rise Time Level (T_{RLP}) Method of Implementation

The T_{RLP} is defined as 15%-85% rise time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD}. The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{RLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 29 Test Availability Condition for Test 1.2.3

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
18241	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	Active Probe (Differential Probe)
28241	Not Applicable	Not Applicable	Disabled	Not Applicable	Disabled	Enabled	Not Applicable	

Measurement Algorithm using Test ID 18241

LP Clock TX 15%-85% Rise Time (T_{RLP}) ESCAPEMODE

NOTE Select **Clock LP Mode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18241 to remotely access the test.

1 This test requires the following prerequisite tests:
   a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
   b LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 18221)

   V_{OH} and V_{OL} values for Low Power signal measurements are performed and test results are stored.
2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3 Perform rise time measurement on the EscapeMode sequence for both Clkp and Clkn waveforms individually.
4 The max, mean and min result values are stored.
5 Report the measurement results:
   a T_{RLP} average value for Clkp channel
   b T_{RLP} average value for Clkn channel
6 Compare the measured T_{RLP} worst value derived from the T_{RLP} average value for Clkp and Clkn to the compliance test limit.

Measurement Algorithm using Test ID 28241

ULPS Clock TX 15%-85% Rise Time (TRLP) ULPSMODE

NOTE Select **Clock ULPS Mode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28241 to remotely access the test.

1. This test requires the following prerequisite tests:
   a. ULPS Clock TX Thevenin Output High Voltage Level (V_{OH}) ULPSMODE (Test ID: 28211)
   b. ULPS Clock TX Thevenin Output Low Voltage Level (V_{OL}) ULPSMODE (Test ID: 28221)

   V_{OH} and V_{OL} values for Low Power signal measurements are performed and test results are stored.
2. The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3. Perform rise time measurement on the EscapeMode sequence for both Clkp and Clkn waveforms individually.
4. The max, mean and min result values are stored.
5. Report the measurement results:
   a. T_{RLP} average value for Clkp channel
   b. T_{RLP} average value for Clkn channel
6. Compare the measured T_{RLP} worst value derived from the T_{RLP} average value for Clkp and Clkn to the compliance test limit.

Test References

See Test 1.2.3 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

Test 1.2.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation

The T_{FLP} is defined as 15%-85% fall time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD}. The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{FLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 30 Test Availability Condition for Test 1.2.4

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1825	Not Applicable	Not Applicable	Disabled	Not Applicable	Disabled	Disabled	Enabled	Active Probe (Differential Probe)
18251	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	
28251	Not Applicable	Not Applicable	Disabled	Not Applicable	Disabled	Enabled	Not Applicable	

Measurement Algorithm using Test ID 1825

LP Clock TX 15%-85% Fall Time (T_{FLP}) (Informative)

NOTE Ensure that the **Clock LP EscapeMode** and **Clock ULPS Mode** are disabled and **Informative Test** enabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application. Use the Test ID# 1825 to remotely access the test.

1 This test requires the following prerequisite tests:
   - *a* LP Clock TX Thevenin Output High Voltage Level (V_{OH}) (Informative) (Test ID: 1821)
   - *b* LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) (Informative) (Test ID: 1822)

   V_{OH} and V_{OL} values for Low Power signal measurements are performed and test results are stored.

2 Trigger is setup to trigger on LP falling edges.

3 The oscilloscope is triggered to capture the falling edges to be processed based on the “LP Observations” configuration in the **Configure** tab.

4 The average 15%-85% fall time for Clkp is recorded.

5 Repeat the same trigger steps for Clkn.

6 Report the measurement results:
   - *a* T_{FLP} average value for Clkp channel
   - *b* T_{FLP} average value for Clkn channel

7 Compare the measured worst value of T_{FLP} with the compliance test limits.

Measurement Algorithm using Test ID 18251

LP Clock TX 15%-85% Fall Time (T_{FLP}) ESCAPEMODE

NOTE Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18251 to remotely access the test.

1. This test requires the following prerequisite tests:
   a. LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
   b. LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 18221)

   V_{OH} and V_{OL} values for low power signal measurements are performed and test results are stored.
2. The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3. Perform fall time measurement on the EscapeMode sequence for both Clkp and Clkn waveforms individually.
4. The maximum, mean and minimum result values are stored.
5. Report the measurement results:
   a. T_{FLP} average value for Clkp channel
   b. T_{FLP} average value for Clkn channel
6. Compare the measured worst value of T_{FLP} derived from the average value of T_{FLP} for Clkp and Clkn to the compliance test limits.

Measurement Algorithm using Test ID 28251

ULPS Clock TX 15%-85% Fall Time (T_{FLP}) ULPSMODE

NOTE Select **Clock ULPS Mode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28251 to remotely access the test.

1. This test requires the following prerequisite tests:
   a. ULPS Clock TX Thevenin Output High Voltage Level (V_{OH}) ULPSMODE (Test ID: 28211)
   b. ULPS Clock TX Thevenin Output Low Voltage Level (V_{OL}) ULPSMODE (Test ID: 28221)

   V_{OH} and V_{OL} values for low power signal measurements are performed and test results are stored.
2. Trigger is setup to trigger on LP falling edges.
3. The oscilloscope is triggered to capture the falling edges to be processed based on the “LP Observations” configuration in the **Configure** tab.
4. The average 15%-85% fall time for Clkp is recorded.
5. Repeat the same trigger steps for Clkn.
6. Report the measurement results:
   a. T_{FLP} average value for Clkp channel
   b. T_{FLP} average value for Clkn channel
7. Compare the measured worst value of T_{FLP} to the compliance test limits.

Test References

See Test 1.2.4 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

Test 1.2.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation

The slew rate $\delta V / \delta t_{SR}$ is the derivative of the LP transmitter output signal voltage over time. The intention of specifying a maximum slew rate value in the specification is to limit EMI (Electro Magnetic Interference).

The specification also states that the Slew Rate must be measured as an average across any 50mV segment of the output signal transition.

PASS Condition

The measured slew rate $\delta V / \delta t_{SR}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 31 Test Availability Condition for Test 1.2.5

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1829	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	Active Probe (Differential Probe)
18291	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	
18292	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	
2829	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Enabled	Not Applicable	
28291	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Enabled	Not Applicable	
28292	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Enabled	Not Applicable	

Measurement Algorithm using Test ID 1829, 18291 and 18292

LP Clock TX Slew Rate Vs. C_{Load} (Max) /

LP Clock TX Slew Rate Vs. C_{Load} (Min) /

LP Clock TX Slew Rate Vs. C_{Load} (Margin)

NOTE

Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test.

- To access the LP Clk TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 1829.
- To access the LP Clk TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 18291.
- To access the LP Clk TX Slew Rate Vs. C_{Load} (Margin) test remotely, use the Test ID# 18292.

1 This test requires the following prerequisite tests:
   a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
   b LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 18221)

   V_{OH} and V_{OL} values for low power signal measurements are performed and test results are stored.
2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3 Perform the slew rate measurement on the EscapeMode sequence for both Clkp and Clkn waveforms individually.
   For falling edge,
   a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
   b. Perform the slew rate measurement across the 400mV - 930mV region to determine the minimum slew rate result.
   For rising edge,
   a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
   b. Perform the slew rate measurement across the 400mV - 700mV region to determine the minimum slew rate result.
   c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700mV - 930mV region.
4 Calculate the average value from all rising edges' maximum slew rate results. Calculate the average value from all falling edges' maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.
5 Calculate the average value from all rising edges' minimum slew rate results. Calculate the average value from all falling edges' minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
6 Calculate the average value from all rising edges' slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
7 The Slew Rate maximum, minimum and margin result values are stored.
8 Report the measurement results.
9 Compare the measured worst slew rate value for Clkp and Clkn to the compliance test limits.

ULPS Clock TX Slew Rate Vs. C_{Load} (Max) ULPSMODE/

ULPS Clock TX Slew Rate Vs. C_{Load} (Min) ULPSMODE/

ULPS Clock TX Slew Rate Vs. C_{Load} (Margin) ULPSMODE

Measurement Algorithm using Test ID 2829, 28291 and 28292

NOTE

Select **Clock ULPS Mode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test.

- To access the ULPS Clk TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 2829.
- To access the ULPS Clk TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 28291.
- To access the ULPS Clk TX Slew Rate Vs. C_{Load} (Margin) test remotely, use the Test ID# 28292.

1. This test requires the following prerequisite tests:
   a. ULPS Clock TX Thevenin Output High Voltage Level (V_{OH}) ULPSMODE (Test ID: 28211)
   b. ULPS Clock TX Thevenin Output Low Voltage Level (V_{OL}) ULPSMODE (Test ID: 28221)

   V_{OH} and V_{OL} values for low power signal measurements are performed and test results are stored.
2. The oscilloscope is triggered to capture rising and falling edges to be processed based on the “Number of ULPS Slew Edge” configuration in the **Configure** tab.
3. Perform the slew rate measurement on the mentioned triggered data for both Clkp and Clkn waveforms individually.
   For falling edge,
   a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
   b. Perform the slew rate measurement across the 400mV - 930mV region to determine the minimum slew rate result.
   For rising edge,
   a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
   b. Perform the slew rate measurement across the 400mV - 700mV region to determine the minimum slew rate result.
   c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700mV - 930mV region.
4. Calculate the average value from all rising edges’ maximum slew rate results. Calculate the average value from all falling edges’ maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.
5. Calculate the average value from all rising edges’ minimum slew rate results. Calculate the average value from all falling edges’ minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
6. Calculate the average value from all rising edges’ slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
7. The Slew Rate maximum, minimum and margin result values are stored.
8. Report the measurement results.
9. Compare the measured worst slew rate value for Clkp and Clkn to the compliance test limits.

Test References

See Test 1.2.5 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

Part II
Global Operation

KEYSIGHT
TECHNOLOGIES

8 MIPI D-PHY 1.0 Data Transmitter (Data TX) Global Operation Tests

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Test 1.3.13 HS Exit: Data TX $T_{HS-TRAIL}$ Method of Implementation / 146
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Test 1.3.15 HS Exit: Data TX T_{EOT} Method of Implementation / 150
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This section provides the Methods of Implementation (MOIs) for the Data Transmitter (Data TX) Global Operation tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

KEYSIGHT
TECHNOLOGIES

Probing for Data TX Global Operation Tests

When performing the Data TX tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the Data TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test Application for the exact number of probe connections.

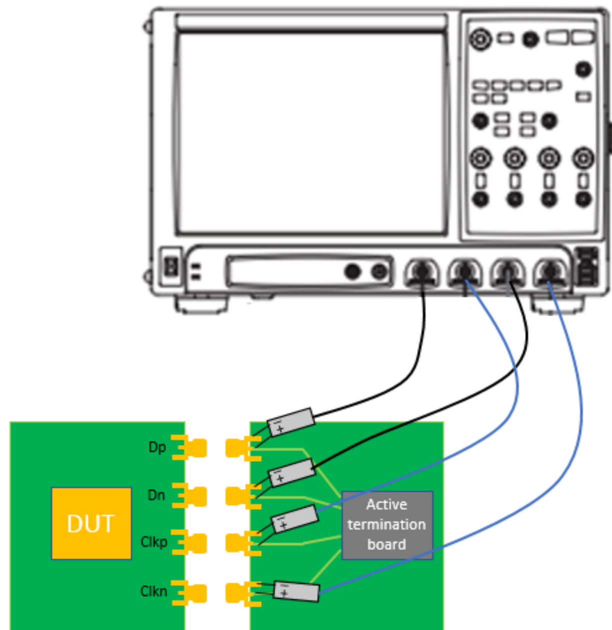

Figure 37 Probing for Data TX Global Operation Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 37 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, ZID (termination resistance), CLoad, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

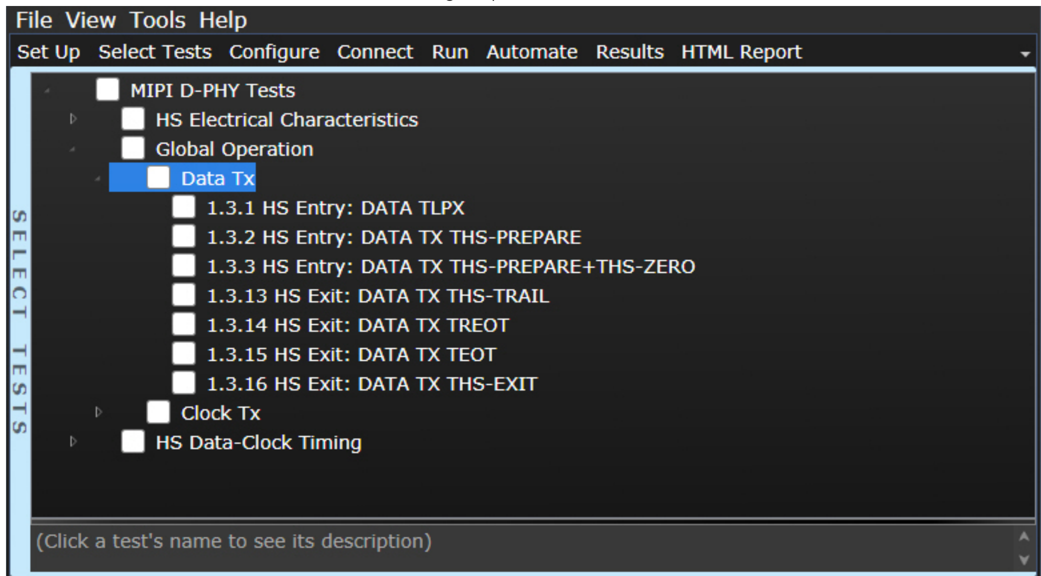

Figure 38 Selecting Data TX Global Operation Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.3.1 HS Entry: Data T_{LPX} Method of Implementation

This test verifies that the last LP-01's duration prior to HS Data burst is within the specification.

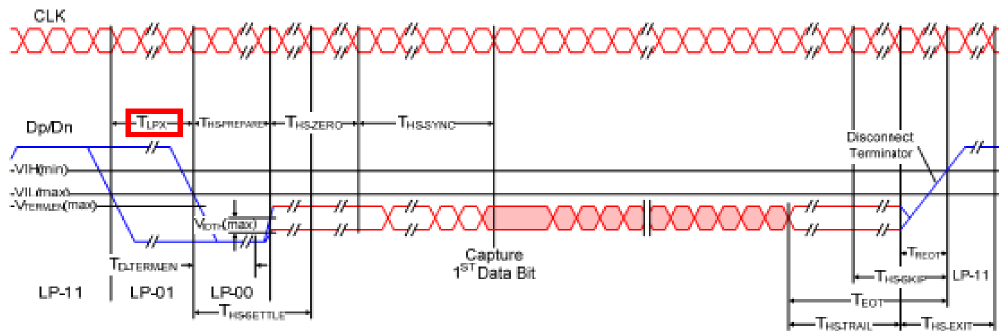

Figure 39 High-Speed Data Transmission in Bursts

PASS Condition

The T_{LPX} must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 32 Test Availability Condition for Test 1.3.1

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
511	Not Applicable	100 ohm	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 511

NOTE Use the Test ID# 511 to remotely access the test.

1. Trigger on the Dp's falling edge in LP-01 at the SoT.
2. Denote the time when the Dp falling edge first crosses V_{IL}(max), as T1.
3. Denote the time when the first Dn falling edge after T1 crosses VIL(max), as T2.
4. Calculate T_{LPX} by using the following equation:

$$T_{LPX} = T2-T1$$

5. Report the T_{LPX} measurement.
6. Compare the T_{LPX} to the conformance test limit.

Test References

See Test 1.3.1 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.3.2 HS Entry: Data TX $T_{HS-PREPARE}$ Method of Implementation

This test verifies that the last LP-00's duration prior to HS Data burst is within the specification.

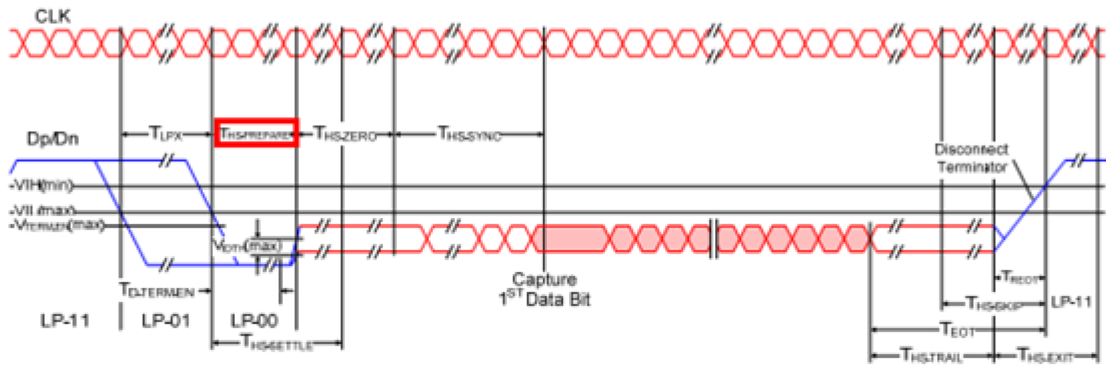

Figure 40 High-Speed Data Transmission in Bursts

PASS Condition

The $T_{HS-PREPARE}$ must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 33 Test Availability Condition for Test 1.3.2

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
557	Not Applicable	100 ohm	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 557

NOTE Use the Test ID# 557 to remotely access the test.

1 This test requires the following prerequisite tests:
- HS Clock Instantaneous: UI_{inst} [Max] (Test ID: 911)
- The minimum, maximum and average Unit Interval of the differential clock waveform is measured and test results are stored.

2 Trigger on the Dp's falling edge in LP-01 at the SoT.

3 Denote the time when the first Dn falling edge after LP-01 crosses V_{IL}(max), as T2.

4 Construct the differential waveform of Dp and Dn by using the following formula:

DataDiff = Dp-Dn

5 Find and denote the first falling edge of the differential waveform that crosses - V_{IDTH}(max) as T3. T3 must be greater than T2.
6 Calculate $T_{HS-PREPARE}$ by using the following equation:

$$T_{HS-PREPARE} = T3-T2$$

7 Report the $T_{HS-PREPARE}$.measured.
8 Compare the $T_{HS-PREPARE}$ value with the conformance test limit.

Test References

See Test 1.3.2 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.3.3 HS Entry: Data TX $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ Method of Implementation

This test verifies that the duration in time HS TX driving the line in HS0 prior to HS Sync sequence is within the specification. HS Sync-Sequence: 0001110101.

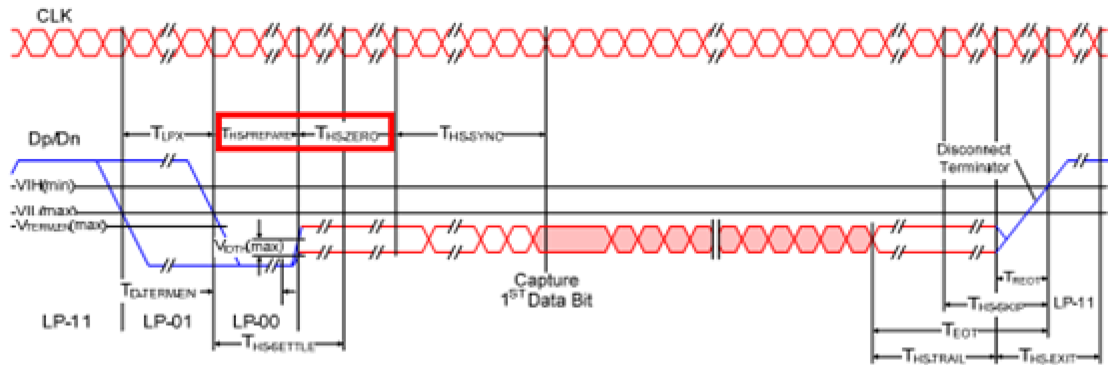

Figure 41 High-Speed Data Transmission in Bursts

PASS Condition

The average $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 34 Test Availability Condition for Test 1.3.3

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
558	Not Applicable	100 ohm	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 558

NOTE Use the Test ID# 558 to remotely access the test.

1 This test requires the following prerequisite tests:

   a HS Clock Instantaneous: UI_{inst} [Max] (Test ID: 911)

   The minimum, maximum and average Unit Interval of the differential clock waveform is measured and test results are stored.

2 Trigger on Dp's falling edge in LP-01 at the SoT.

3 Denote the time when the first Dn falling edge after Dp falling crosses VIL(max), as T2.

4 Construct the differential waveform of Dp and Dn by using the following formula:

$$DataDiff = Dp-Dn$$

5 Find and denote the first rising edge of the differential waveform that crosses $-V_{IDTH}$(max) as T4.

   where, T4 is where the bit pattern "000" occurs in HS Sync sequence ends.

6 Find and denote the next rising edge that crosses V_{IDTH}(max) after T4 as T5.

   where, T5 is where the bit pattern "111" occurs in HS Sync sequence ends.

7 The bit pattern "000" of HS Sync sequence should be the same length in time as the bit pattern "111", thus the time duration for the bit pattern "000" should be T5 - T4.

8 Calculate $T_{HS\text{-}PREPARE} + T_{HS\text{-}ZERO}$ by using the following equation:

$$T_{HS\text{-}PREPARE} + T_{HS\text{-}ZERO} = T4-(T5-T4)-T2$$

9 Report the measured $T_{HS\text{-}PREPARE} + T_{HS\text{-}ZERO}$.

10 Compare the average $T_{HS\text{-}PREPARE} + T_{HS\text{-}ZERO}$ with the conformance test limit.

Test References

See Test 1.3.3 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.3.13 HS Exit: Data TX $T_{HS-TRAIL}$ Method of Implementation

This test verifies that the duration in time of HS TX driving the line in inverted final differential state following the last payload data bit of a HS Data burst is equal or greater than the minimum required value.

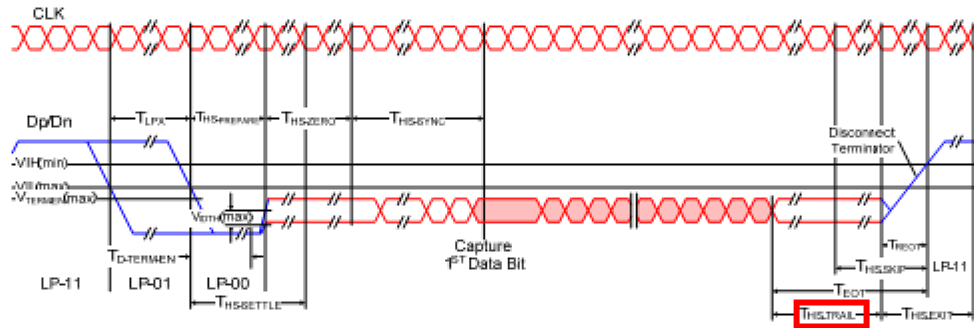

Figure 42 High-Speed Data Transmission in Bursts

PASS Condition

The average $T_{HS-TRAIL}$ must be equal or greater than the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 35 Test Availability Condition for Test 1.3.13

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
546	Not Applicable	100 ohm	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 546

NOTE Use the Test ID# 546 to remotely access the test.

1 Trigger on Dp's falling edge in LP-01 at the SoT.
2 Go to EoT of the same burst.
3 Find the time where the last payload data bit's differential edge crosses +/-V_{IDTH}(max), denoted as T6.
4 Find the time when the last TX differential edge crosses +/-V_{IDTH}(max), and denote it as T7. Note that T7 must be greater than T6.
5 Use the following calculation:

$$T_{HS-TRAIL} = T7-T6$$

6 Report the measured $T_{HS-TRAIL}$.

7 Compare the measured $T_{HS-TRAIL}$ with the conformance test limits.

Test References

See Test 1.3.13 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{REOT}) Method of Implementation

The rise-time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.

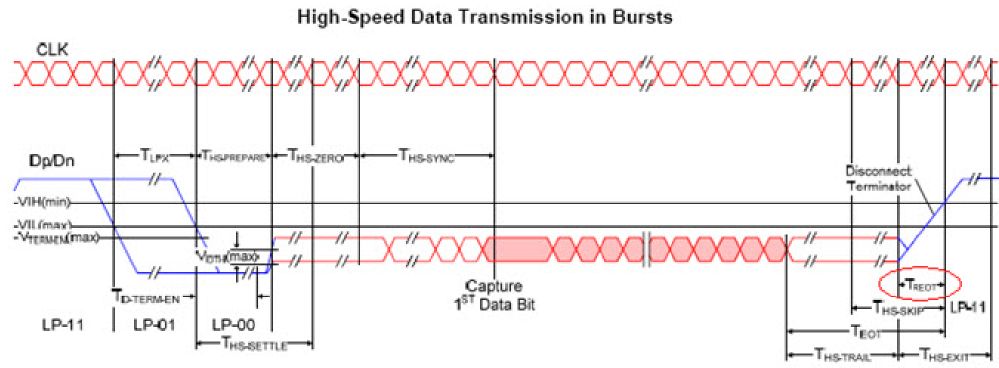

Figure 43 High-Speed Data Transmission in Bursts

PASS Condition

The measured T_{REOT} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 36 Test Availability Condition for Test 1.3.14

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
549	Not Applicable	100 ohm	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 549

NOTE Use the Test ID# 549 to remotely access the test.

1. Trigger on Dp's falling edge in LP-01 at the SoT.
2. Go to EoT.
3. Find the time where the last data TX differential edge crosses +/-V_{IDTH}(max), denoted as T1.
4. Find the time where Dp rising edge crosses V_{IH}(min)(880mV), and denote it as T2. Note that T2 must be greater than T1.
5. Use the following calculation:

$$T_{REOT} = T2 - T1$$

6. Report the measured T_{REOT}.

7 Compare the measured T_{REOT} with the conformance test limits.

Test References

See Test 1.3.14 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

Test 1.3.15 HS Exit: Data TX T_{EOT} Method of Implementation

This test verifies that the combined duration of the $T_{HS\text{-}TRAIL}$ and T_{REOT} intervals of the DUT Data TX is less than the maximum required value.

Figure 44 High-Speed Data Transmission in Bursts

PASS Condition

The average T_{EOT} value must be equal or less than the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 37 Test Availability Condition for Test 1.3.15

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
547	Not Applicable	100 ohm	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 547

NOTE Use the Test ID# 547 to remotely access the test.

1 This test requires the following prerequisite tests:
   - HS Clock Instantaneous: UI_{inst} [Max] (Test ID: 911)
   - The minimum, maximum and average Unit Interval of the differential clock waveform is measured and test results are stored.
2 Trigger on Dp's falling edge in LP-01 at the SoT.
3 Go to EoT.
4 Find the time when the last data differential edge crosses +/-V_{IDTH}(max), and denote it as T6.
5 Find the time where Dp rising edge crosses VIH(min)(880mV), and denote it as T8. Note that T8 must greater than T6.

6 Use the following calculation:

$$T_{EOT} = T8 - T6$$

7 Report the measured T_{EOT}.

8 Compare the measured T_{EOT} with the conformance test limits.

Test References

See Test 1.3.15 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.3.16 HS Exit: Data TX $T_{HS-EXIT}$ Method of Implementation

This test verifies that the Data TX remains in LP-11 state after exiting HS mode is greater than the minimum required value.

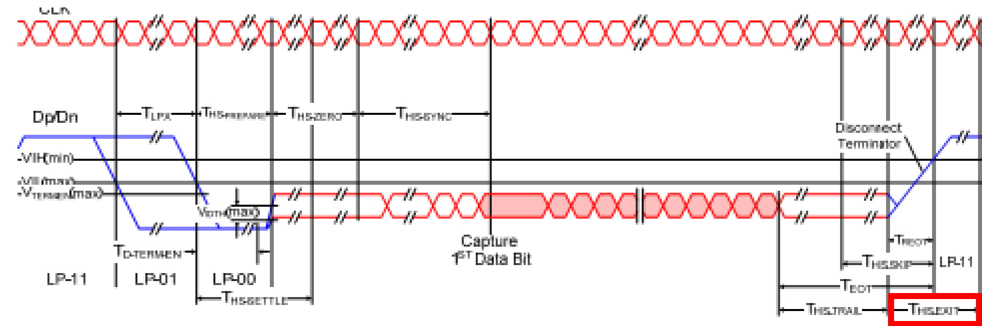

Figure 45 High-Speed Data Transmission in Bursts

PASS Condition

The average $T_{HS-EXIT}$ value must be equal or greater than the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 38 Test Availability Condition for Test 1.3.16

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
548	Not Applicable	100 ohm	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 548

NOTE Use the Test ID# 548 to remotely access the test.

1 Trigger on the Dp's falling edge in LP-01 at the SoT.
2 Go to EoT of the same burst.
3 Find the time when the last Data TX differential edge crosses +/-V_{IDTH}(max), and denote it as T7.
4 Find the time after T7 when Dp falling edge starts to cross VIL(min), and denote it as T9.
5 Use the following calculation:

$$T_{HS-EXIT} = T9-T7$$

6 Report the measured $T_{HS-EXIT}$.
7 Compare the measured $T_{HS-EXIT}$ with the conformance test limits.

Test References

See Test 1.3.16 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

9 MIPI D-PHY 1.0 Clock Transmitter (Clock TX) Global Operation Tests

Probing for Clock TX Global Operation Tests / 156
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Test 1.4.2 HS Entry: CLK TX $T_{CLK-PREPARE}$ Method of Implementation / 160
Test 1.4.3 HS Entry: CLK TX $T_{CLK-PREPARE}$+$T_{CLK-ZERO}$ Method of Implementation / 162
Test 1.5.1 HS Entry: CLK TX $T_{CLK-PRE}$ Method of Implementation / 164
Test 1.5.2 HS Exit: CLK TX $T_{CLK-POST}$ Method of Implementation / 166
Test 1.4.13 HS Exit: CLK TX $T_{CLK-TRAIL}$ Method of Implementation / 168
Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{REOT}) Method of Implementation / 170
Test 1.4.15 HS Exit: CLK TX T_{EOT} Method of Implementation / 172
Test 1.4.16 HS Exit: CLK TX $T_{HS-EXIT}$ Method of Implementation / 174

This section provides the Methods of Implementation (MOIs) for the Clock Transmitter (Clock TX) Global Operation tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

KEYSIGHT TECHNOLOGIES

Probing for Clock TX Global Operation Tests

When performing the Clock TX tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the Clock TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test Application for the exact number of probe connections.

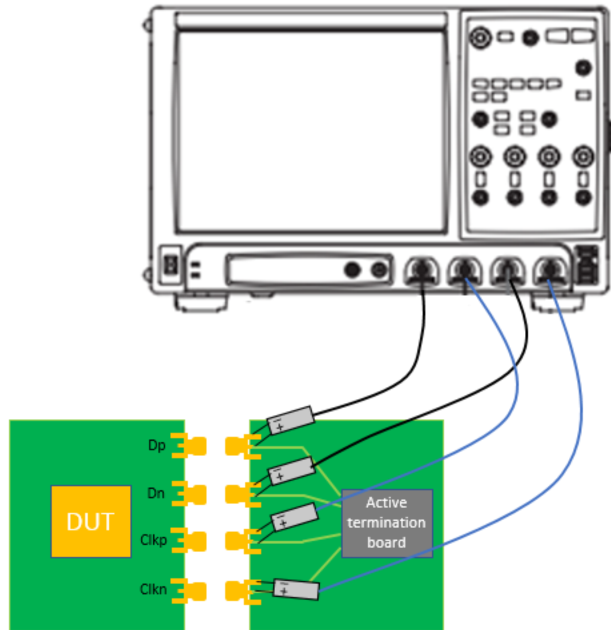

Figure 46 Probing for Clock TX Global Operation Tests

You can identify the channels used for each signal in the Configuration tab of the MIPI D-PHY Test Application. (The channels shown in Figure 46 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, ZID (termination resistance), Cload, Device ID and User Comments.
4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

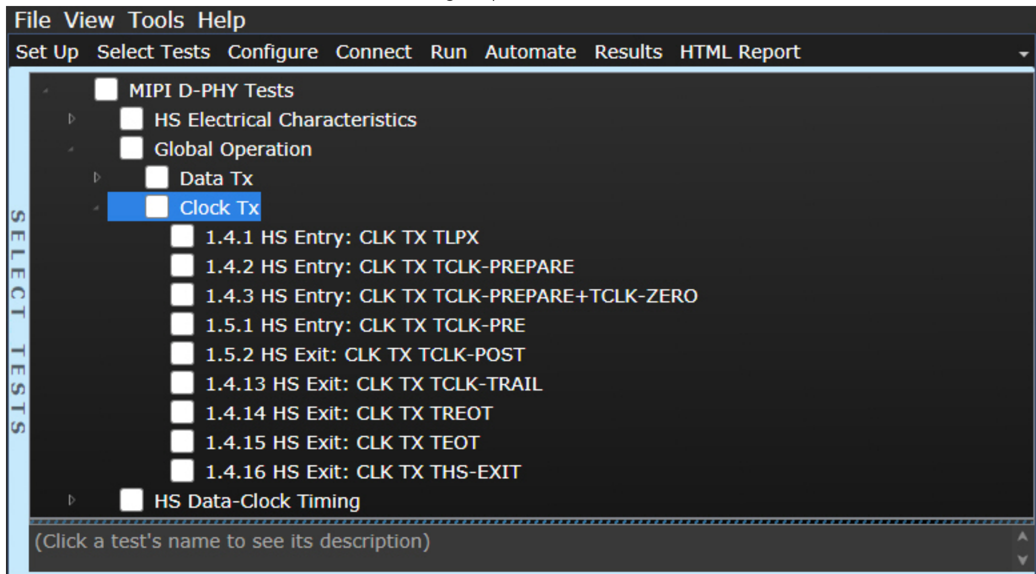

Figure 47 Selecting Clock TX Global Operation Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.4.1 HS Entry: CLK TX T_{LPX} Method of Implementation

This test verifies that the duration in time for the Clock TX to remain in LP-01 (Stop) state before entering the HS mode is greater than the minimum required value.

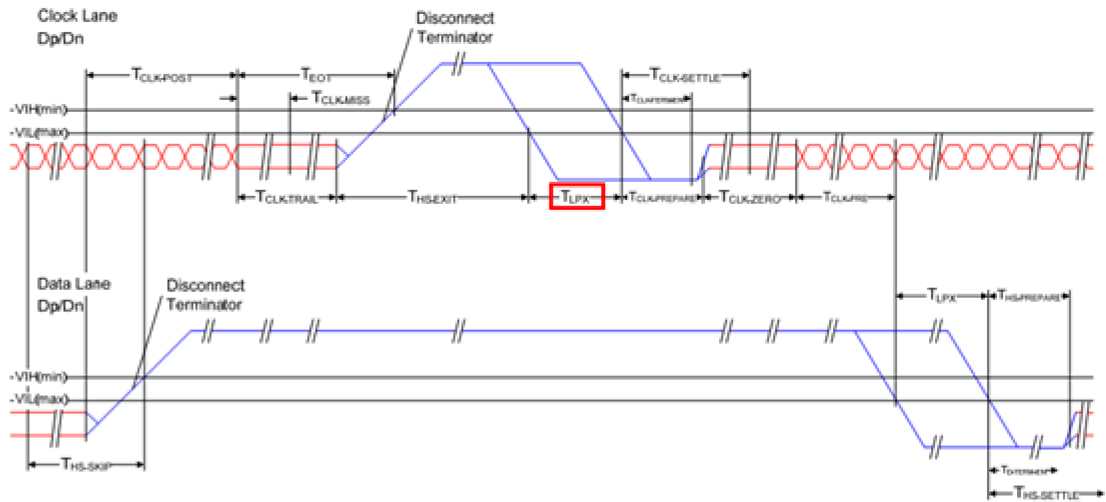

Figure 48 Switching the Clock Lane between Clock Transmission and Low-Power Mode

PASS Condition

The T_{LPX} must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 39 Test Availability Condition for Test 1.4.1

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
5510	Not Applicable	100 ohm	Not Applicable	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 5510

NOTE Use the Test ID# 5510 to remotely access the test.

1 Trigger on the Clkn's falling edge after LP-01.
2 Find the time of Clkp falling edge before the trigger position that crosses V_{IL}(max) and denote it as T1.
3 Find the time of Clkn falling edge after the T1 that crosses V_{IL}(max) and denote it as T2

4 Construct T_{LPX} using the following equation:

$$T_{LPX} = T2-T1$$

5 Report the T_{LPX} measurement.

6 Compare the measured T_{LPX} to the conformance limit.

Test References

See Test 1.4.1 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.4.2 HS Entry: CLK TX $T_{CLK-PREPARE}$ Method of Implementation

This test verifies that the duration in time for the Clock TX to remain in LP-00 state before entering HS mode is within the required value.

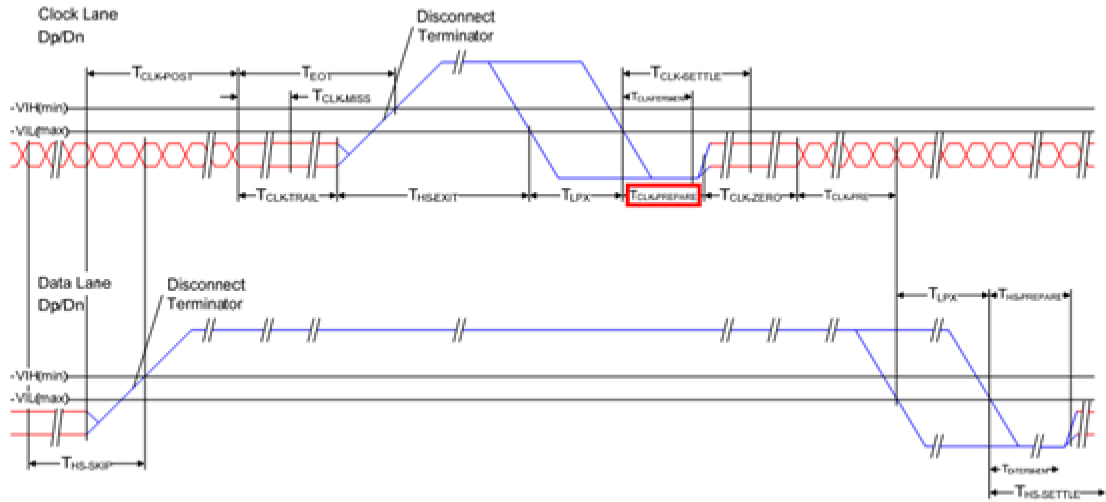

Figure 49 Switching the Clock Lane between Clock Transmission and Low-Power Mode

PASS Condition

The $T_{CLK-PREPARE}$ shall be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 40 Test Availability Condition for Test 1.4.2

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
552	Not Applicable	100 ohm	Not Applicable	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 552

NOTE Use the Test ID# 552 to remotely access the test.

1 Trigger on the Clkn falling edge after LP-01.
2 Find the time of Clkp falling edge before the trigger position that crosses V_{IL}(max). Mark the time as T1.
3 Find the time of Clkn falling edge after the T1 that crosses V_{IL}(max) and denote it as T2.
4 Construct the differential clock waveform using the following equation:

$$DiffClock = Clkp-Clkn$$

5. Find the time when DiffClock's falling edges first crosses $-V_{IDTH}$(MAX) after T2, and denote it as T3.
6. Calculate $T_{CLK-PREPARE}$ using the following equation:

$$T_{CLK-PREPARE} = T3-T2$$

7. Report the $T_{CLK-PREPARE}$.measurement.
8. Compare $T_{CLK-PREPARE}$ with the conformance test limit.

Test References

See Test 1.4.2 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.4.3 HS Entry: CLK TX $T_{CLK-PREPARE}+T_{CLK-ZERO}$ Method of Implementation

This test verifies that the duration in time for Clock TX to remain in LP-00 and HS0 state before starting clock transmission is greater than the minimum required value.

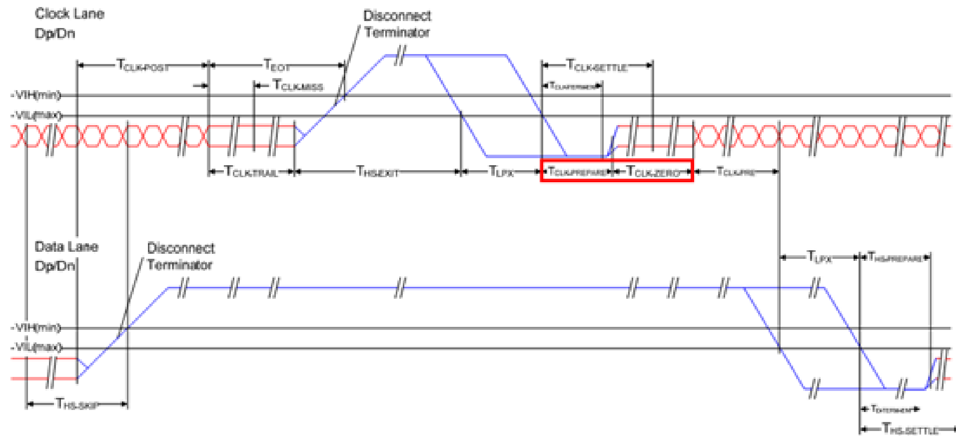

Figure 50 Switching the Clock Lane between Clock Transmission and Low Power Mode

PASS Condition

The $T_{CLK-PREPARE}+T_{CLK-ZERO}$ must be within the conformance limit as specified in the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 41 Test Availability Condition for Test 1.4.3

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
554	Not Applicable	100 ohm	Not Applicable	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 554

NOTE Use the Test ID# 554 to remotely access the test.

1 Trigger on the Clkn falling edge after LP-01.
2 Find the time of Clkp falling edge before the trigger position that crosses V_{IL}(max) and denote it as T1.
3 Find the time of Clkn falling edge after the T1 that crosses V_{IL}(max) and denote it as T2.
4 Construct the differential clock waveform by using the following equation:

DiffClock = Clkp-Clkn

5. Find the time when the DiffClock's falling edges first crosses -V_{IDTH}(max) after T2 and denote it as T3.
6. Find the time when the DiffClock's rising edges first crosses -V_{IDTH}(max) after T3 and denote it as T4.
7. Calculate $T_{CLK-PREPARE}+T_{CLK-ZERO}$ by using the following equation:

$$T_{CLK-PREPARE}+T_{CLK-ZERO} = T4-T2$$

8. Report the $T_{CLK-PREPARE}$.+$T_{CLK-ZERO}$ measurement.
9. Compare the $T_{CLK-PREPARE}+T_{CLK-ZERO}$ value with the conformance test limit.

Test References

See Test 1.4.3 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.5.1 HS Entry: CLK TX $T_{CLK-PRE}$ Method of Implementation

This test verifies that the duration in time for the Clock TX start to transmit clock until the Data TX is switch from LP11 (Stop) to LP01 state. The duration has to be greater than the required minimum value.

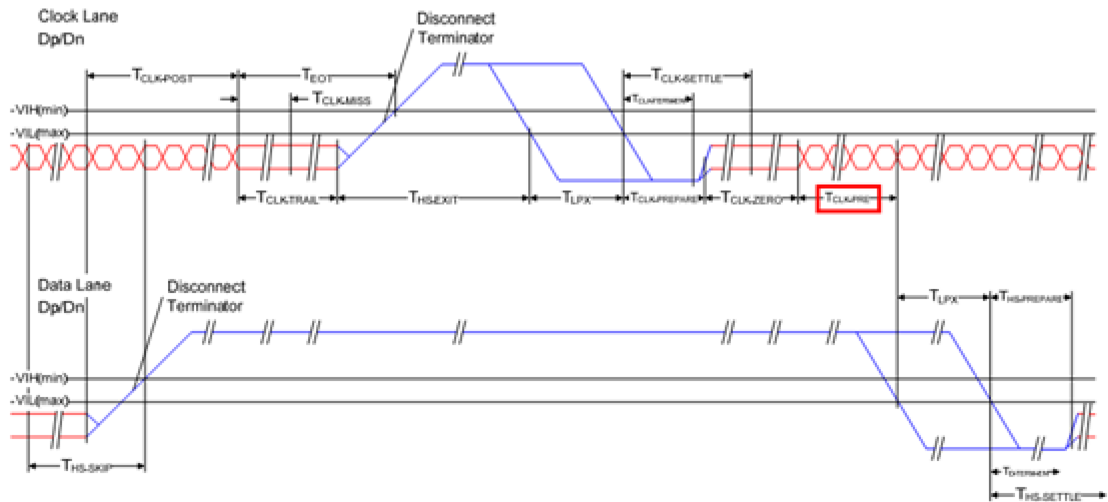

Figure 51 Switching the Clock Lane Between Clock Transmission and Low-Power Mode

PASS Condition

The $T_{CLK-PRE}$ value must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 42 Test Availability Condition for Test 1.5.1

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
551	Not Applicable	100 ohm	Not Applicable	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 551

NOTE Use the Test ID# 551 to remotely access the test.

1 This test requires the following prerequisite test:

a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)

Measure the minimum, maximum and average values of the Unit Interval for the differential clock waveform and the test results are stored.

2 Trigger on the Clkn's falling edge after LP-01.
3 Construct the differential clock waveform using the following equation:

DiffClock = Clkp-Clkn

4 Find the time when the DiffClock's rising edge first crosses $-V_{IDTH}$(max) after LP-00. Denote the time as T1.
5 Find the time when the Dp's LP falling edge from the same burst crosses V_{IL}(max). Mark the first edges found next to T1 as T2.
6 Calculate $T_{CLK-PRE}$ using the following equation:

$$T_{CLK-PRE} = T2-T1$$

7 Report the $T_{CLK-PRE}$ measurement.
8 Compare the $T_{CLK-PRE}$ value with the conformance test limit.

Test References

See Test 1.5.1 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.5.2 HS Exit: CLK TX $T_{CLK-POST}$ Method of Implementation

This test verifies that the DUT Clock Lane HS transmitter continues to transmit clock signaling for the minimum required duration after the last Data Lane switches to LP mode.

Figure 52 Switching the Clock Lane Between Clock Transmission and Low-Power Mode

PASS Condition

The average $T_{CLK-POST}$ must be equal or greater than the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 43 Test Availability Condition for Test 1.5.2

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
555	Not Applicable	100 ohm	Not Applicable	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 555

NOTE Use the Test ID# 555 to remotely access the test.

1 This test requires the following prerequisite tests:

   a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)

   Measure the minimum, maximum and average values of the Unit Interval for the differential clock waveform and the test results are stored.

2 Trigger on the Clkn's falling edge after LP-01.

3 Back trace to the previous EoT.

4 Construct the differential clock waveform using the following equation:

DiffClock = Clkp-Clkn

5 Find the time when the DiffClock crosses +/-V_{IDTH}(max) after last payload clock bit. Denote this time as T2.

6 Find the time when the last DiffData differential edge crosses +/-V_{IDTH}(max). Denote the time as T1. Note that T2 must be greater than T1.

7 Calculate $T_{CLK-POST}$ using the following equation:

$$T_{CLK-POST} = T2-T1$$

8 Report the $T_{CLK-POST}$ measured.

9 Compare the $T_{CLK-POST}$ value with the conformance test limit.

Test References

See Test 1.5.2 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.4.13 HS Exit: CLK TX $T_{CLK-TRAIL}$ Method of Implementation

This test verifies that the duration for Clock TX to drive the final HS-0 differential state following the last payload clock bit is equal or greater than the minimum required value.

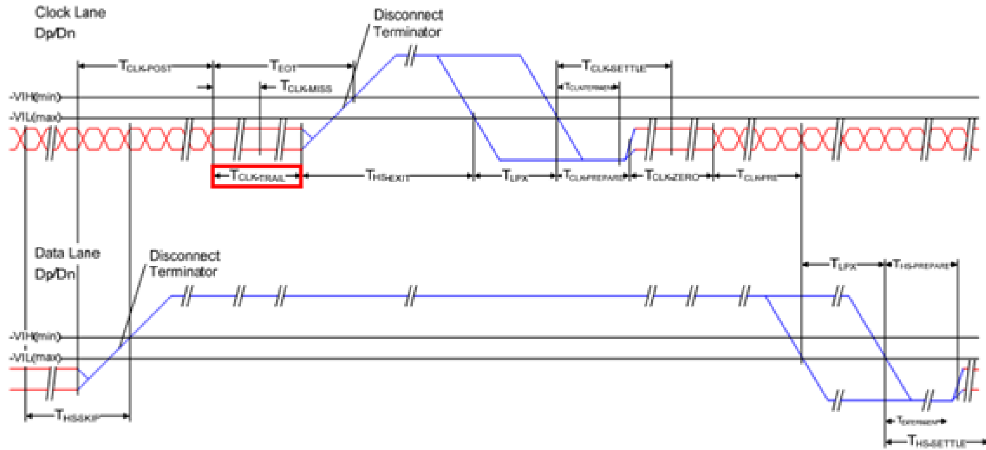

Figure 53 Switching the Clock Lane Between Clock Transmission and Low-Power Mode

PASS Condition

The average $T_{CLK-TRAIL}$ must be equal or greater than the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 44 Test Availability Condition for Test 1.4.13

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
543	Not Applicable	100 ohm	Not Applicable	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 543

NOTE Use the Test ID# 543 to remotely access the test.

1 Trigger on the Clkn's falling edge after LP-01.
2 Back trace to the previous EoT.
3 Construct the differential clock waveform by using the following equation:

$$DiffClock = Clkp-Clkn$$

4 Find the time when the DiffClock crosses +/-V_{IDTH}(max) after last payload clock bit and denote it as T1.

5 Find the time when the DiffClock crosses +/-V_{IDTH}(max) before switching to LP and denote the time as T2. Note that T2 must be greater than T1.
6 Calculate $T_{CLK-TRAIL}$ by using the following equation:

$$T_{CLK-TRAIL} = T2-T1$$

7 Report the $T_{CLK-TRAIL}$ measured.
8 Compare the $T_{CLK-TRAIL}$ value with the conformance test limit.

Test References

See Test 1.4.13 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{REOT}) Method of Implementation

This rise-time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.

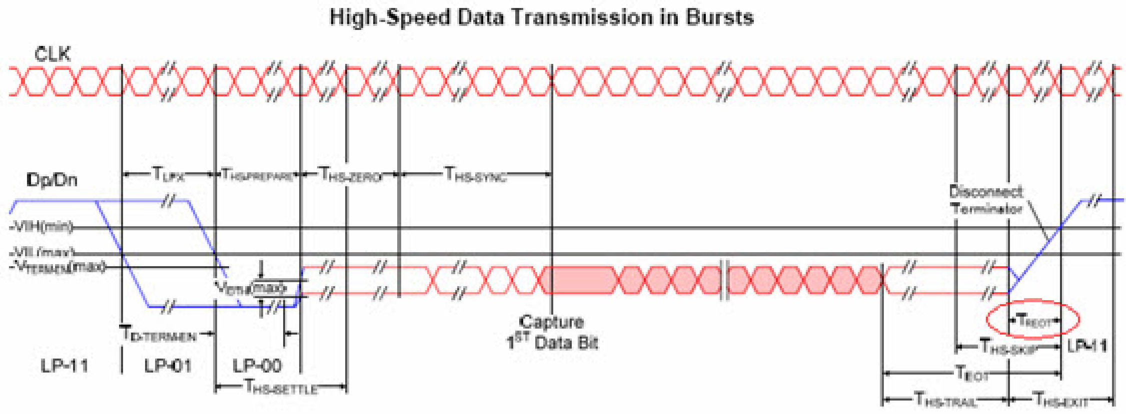

Figure 54 High Speed Data Transmission in Bursts

PASS Condition

The measured T_{EOT} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 45 Test Availability Condition for Test 1.4.14

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
559	Not Applicable	100 ohm	Not Applicable	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 559

NOTE Use the Test ID# 559 to remotely access the test.

1 Trigger on the Clkn's falling edge in LP-01 at the SoT.
2 Go to EoT.
3 Find the time where last Clock TX differential edge crosses +/-VIDTH(max), marked as T1.
4 Find the time where Clkp rising edge crosses VIH(min)(880mV), marked as T2. Note that T2 must be greater than T1.
5 Use the equation:

$$T_{REOT} = T2\text{-}T1$$

6 Report the measured T_{REOT}.

7 Compare the measured T_{REOT}value to the compliance test limits.

Test References

See Test 1.4.14 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

Test 1.4.15 HS Exit: CLK TX T_{EOT} Method of Implementation

This test verifies the time from start of $T_{CLK\text{-}TRAIL}$ period to start of LP-11 state is within the conformance limit.

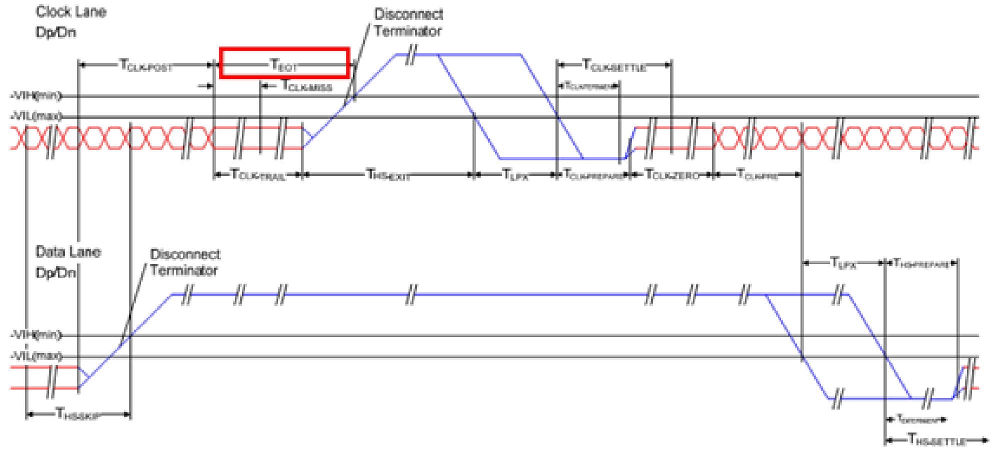

Figure 55 Switching the Clock Lane Between Clock Transmission and Low-Power Mode

PASS Condition

The average T_{EOT} value must be equal or less than the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 46 Test Availability Condition for Test 1.4.15

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
544	Not Applicable	100 ohm	Not Applicable	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 544

NOTE Use the Test ID# 544 to remotely access the test.

1 This test requires the following prerequisite tests:
   a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)

   Measure the minimum, maximum and average values of the Unit Interval for the differential clock waveform and the test results are stored.
2 Trigger on the Clkn's falling edge after LP-01.
3 Back trace to the previous EoT.

4 Construct the differential clock waveform by using the following equation:

DiffClock = Clkp-Clkn

5 Find the time when the DiffClock crosses +/-V_{IDTH}(max) after last payload clock bit. Denote the time as T1.

6 Find the time when the Clkp TX rising edge crosses V_{IH}(min)(880mV). Denote the time as T2. Note that T2 must be greater than T1.

7 Calculate T_{EOT} using the following equation:

$$T_{EOT} = T2-T1$$

8 Report the T_{EOT} measurement.

9 Compare the measured T_{EOT} value with the conformance test limit.

Test References

See Test 1.4.15 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.4.16 HS Exit: CLK TX $T_{HS-EXIT}$ Method of Implementation

This test verifies that the duration in time for the Clock TX to remain in LP-11 (Stop) state after exiting the HS mode is greater than the minimum required value.

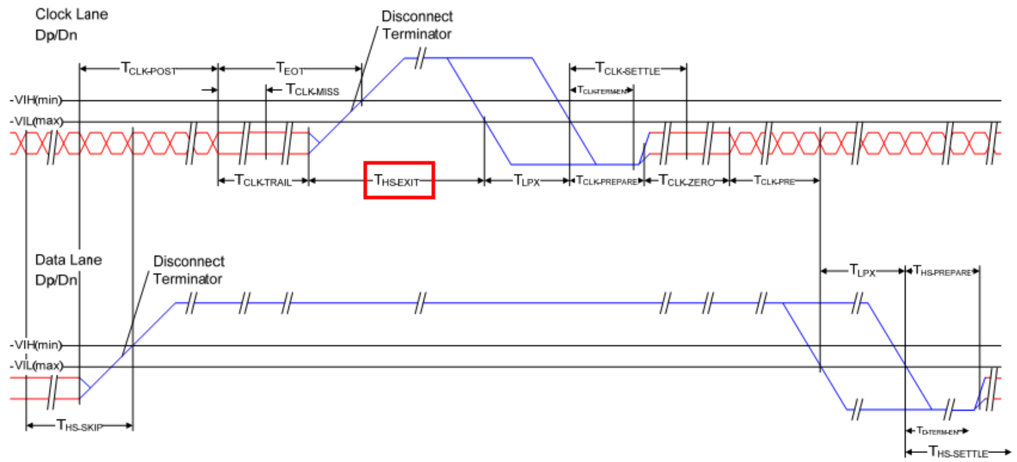

Figure 56 Switching the Clock Lane Between Clock Transmission and Low-Power Mode

PASS Condition

The average $T_{HS-EXIT}$ must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 47 Test Availability Condition for Test 1.4.16

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
556	Not Applicable	100 ohm	Not Applicable	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 556

NOTE Use the Test ID# 556 to remotely access the test.

1 Trigger on the Clkn's falling edge after LP-01.
2 Find and mark the time when the Clkp's falling edge before the trigger position that crosses V_{IL}(max) and denote it as T1.
3 Construct the differential clock waveform by using the following equation:

DiffClock = Clkp-Clkn

4. Find the time when the DiffClock last crosses $+V_{IDTH}$(max) or $-V_{IDTH}$(max) before T1, mark it as T0.
5. Calculate $T_{HS-EXIT}$ by using the following equation:

$$T_{HS-EXIT} = T1 - T0$$

6. Report the $T_{HS-EXIT}$ measurement.
7. Compare the measured $T_{HS-EXIT}$ to conformance limit.

Test References

See Test 1.4.16 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Part III HS Data-Clock Timing

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10 MIPI D-PHY 1.0 High Speed (HS) Data-Clock Timing Tests

Probing for High Speed Data-Clock Timing Tests / 180
Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation / 182
Test 1.5.4 Data-to-Clock Skew ($T_{SKEW(TX)}$) Method of Implementation / 183

This section provides the Methods of Implementation (MOIs) for the High Speed (HS) Data-Clock Timing tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

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Probing for High Speed Data-Clock Timing Tests

When performing the HS Data-Clock Timing tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the HS Data-Clock Timing tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

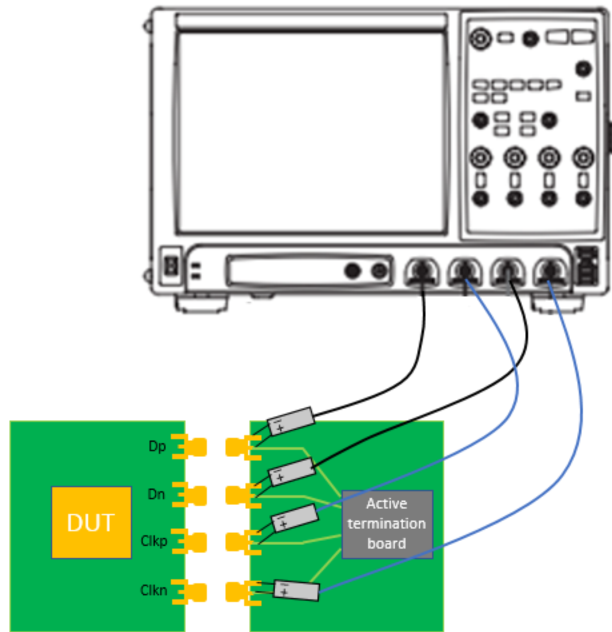

Figure 57 Probing for HS Data-Clock Timing Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 57 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in “Starting the MIPI D-PHY Test Application”.
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, ZID (Termination Resistance), CLoad, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

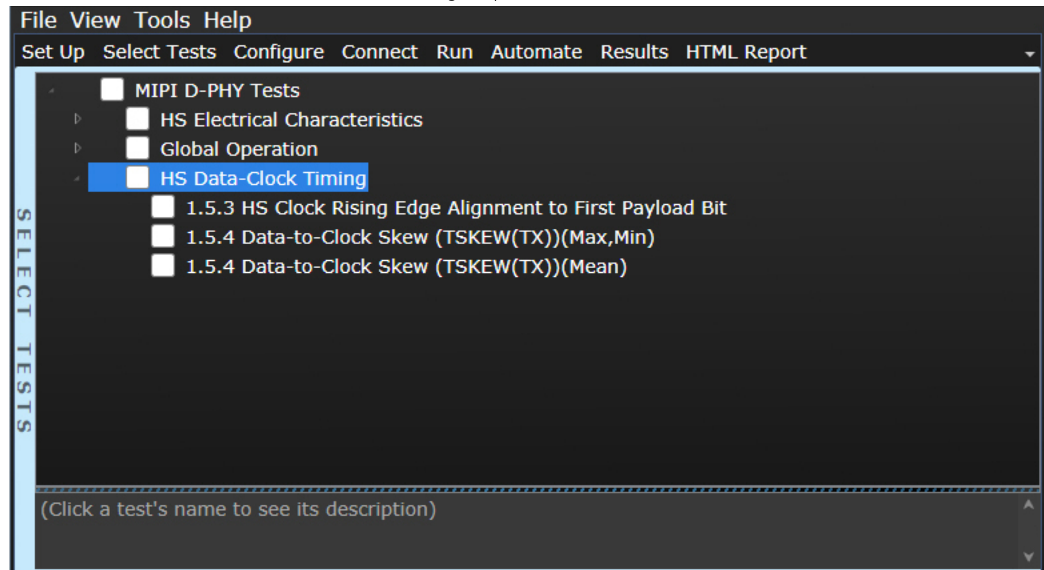

Figure 58 Selecting HS Data-Clock Timing Tests

5 Follow the MIPI D-PHY Test app’s task flow to set up the configuration options, run the tests and view the tests results.

Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation

This test verifies that the first payload bit of the HS transmission burst aligns with differential HS clock’s rising edge.

PASS Condition

A DiffClock rising edge must be found during the bit period of the first payload bit for the test to be considered as pass.

Test Availability Condition

Table 48 Test Availability Condition for Test 1.5.3

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
912	Not Applicable	100 ohm	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 912

NOTE: Use the Test ID# 912 to remotely access the test.

1 Trigger on Dn falling edge after LP-01.
2 Find the first payload bit which is the first bit that comes after HS sync sequence.
3 Construct the differential clock waveform by using the following equation:

DiffClock = Clkp-Clkn

4 Verify if there is a DiffClock rising edge found during the bit period of the first payload bit.
5 Report “Pass” as the final test result if there is a DiffClock rising edge found during the bit period of the first payload bit.
6 Report “Fail” as the final test result if no DiffClock rising edge is found during the bit period of the first payload bit.

Test References

See Test 1.5.3 in CTS v1.0 and Section 9.2 in the D-PHY Specification v1.0.

Test 1.5.4 Data-to-Clock Skew ($T_{SKEW(TX)}$) Method of Implementation

This test verifies that the Data to Clock Skew, measured at the transmitter is within the required specification. Based on the specifications, the mentioned T_{Skew} parameter is defined as the allowed deviation of the data launch time to the ideal 1/2UI displaced quadrature clock edge.

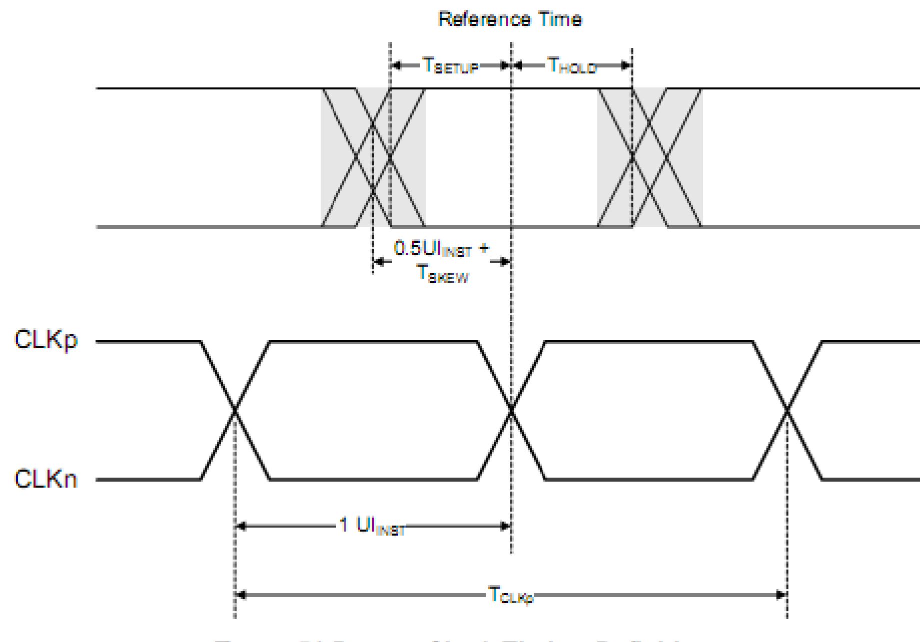

Figure 59 Data to Clock Timing Definitions

PASS Condition

The $T_{SKEW(TX)}$ in UI must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 49 Test Availability Condition for Test 1.5.4

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
913	Not Applicable	100 ohm	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)
9131	Not Applicable	100 ohm	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	

Measurement Algorithm using Test ID 913

NOTE Use the Test ID# 913 to remotely access the test.

1 This test requires the following prerequisite tests:
   a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)
   Measure the minimum, maximum and average values of the Unit Interval for the differential clock waveform and the test results are stored.
2 Dp, Dn, Clkp and Clkn waveforms are captured.
3 Construct the differential clock waveform using the following equation:

   DiffClock = Clkp-Clkn
4 Construct the differential data waveform by using the following equation:

   DiffData = Dp-Dn
5 Using the DiffClock's rising and falling edges, fold the DiffData to form a data eye.
6 Use the **Histogram** feature to find out the furthest edges on the left of the DiffData left crossing and use it to calculate the T_{Skew} (max).
7 Use the **Histogram** feature to find out the nearest edges on the left of the DiffData left crossing and use it to calculate the T_{Skew} (min).
8 Use the **Histogram** feature to find out the mean of the DiffData left crossing and use it to calculate the T_{Skew} (mean).
9 Calculate T_{Skew} values (max/min) in units of seconds and in units of UI using the following equation:

$$T_{Skew(TX)} \text{ (in seconds)} = (T_{Skew} - T_{Center}) - \text{MeanSkewRef}$$

$$T_{Skew(TX)} \text{ (in UI)} = T_{Skew}/\text{MeanUI}$$

NOTE MeanSkewRef = [0.5 * MeanUI obtained from the prerequisite test]

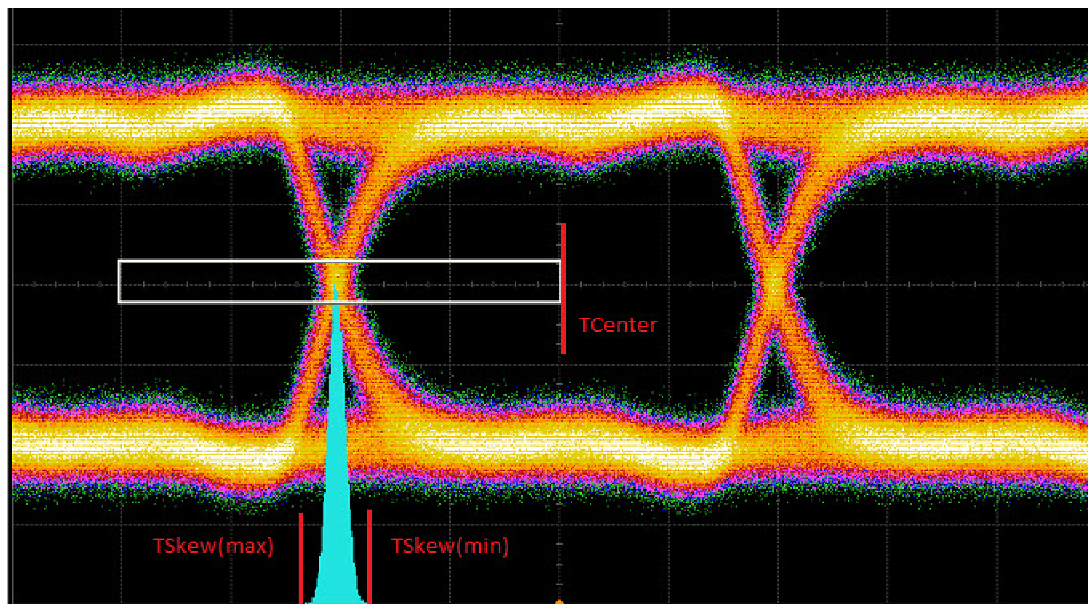

Figure 60 Data Eye

10 Calculate T_{Skew} (mean) in units of UI using the following equation:

$$T_{Skew(TX)} \text{ (in UI)} = T_{Skew}/\text{MeanUI}$$

11 The T_{Skew} (worst) is determined based on the T_{Skew} (max) and T_{Skew} (min) values with reference to the compliance test limit

12 Compare the T_{Skew} (worst) value with the conformance test limits.

Measurement Algorithm using Test ID 9131

NOTE Use the Test ID# 9131 to remotely access the test.

1 This test requires the following prerequisite tests:

   a Data-to-Clock Skew [$T_{Skew(TX)}$] (Max, Min) (Test ID: 913)

   Measure the value of T_{Skew} (mean) and the test results are stored.

2 Use the value of T_{Skew} (mean) measured in the prerequisite test as the final test result and compare the value to the conformance test limits.

Test References

See Test 1.5.4 in CTS v1.0 and Section 9.2.1 Table 27 in the D-PHY Specification v1.0.

Part IV
Informative Tests

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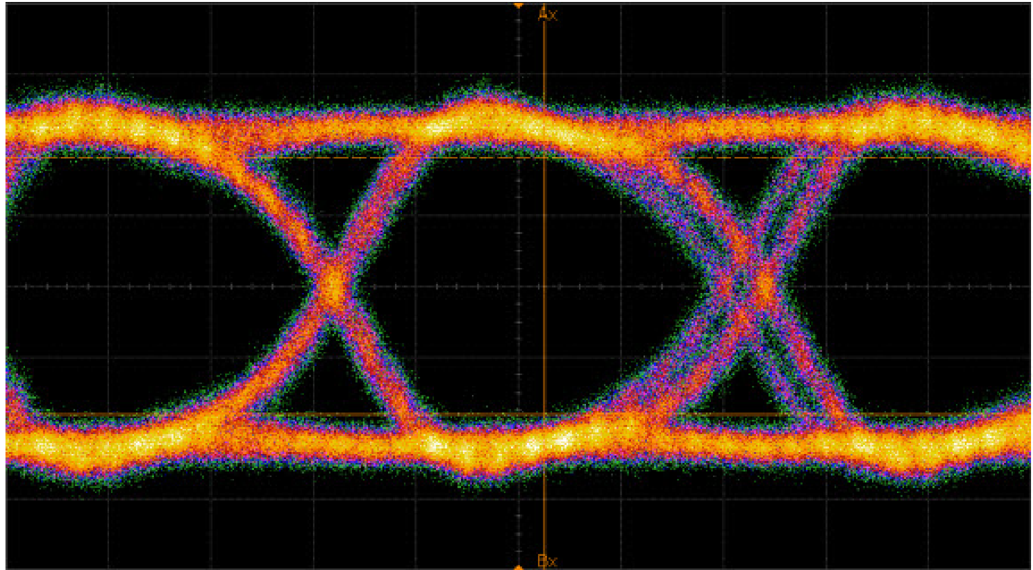
11 MIPI D-PHY 1.0 Informative Tests

HS Data Eye Height (Informative) Method of Implementation / 190
HS Data Eye Width (Informative) Method of Implementation / 192

This section provides the Methods of Implementation (MOIs) for the informative tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application. These tests are meant to provide additional test information on the DUT. The MIPI DPHY CTS specification do not explicitly specify these tests.

HS Data Eye Height (Informative) Method of Implementation

This test measures the eye height parameter of the test data signal by generating an Eye diagram based on the data and clock signal.



PASS Condition

The measured eye height must be within the limit as set by the user under the Configure tab of the application.

Test Availability Condition

Table 50 Test Availability Condition for HS Data Eye Height

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
915	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Enabled	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 915

NOTE Select **Informative Test** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 915 to remotely access the test.

1 Dp, Dn, Clkp and Clkn waveforms are captured.
2 Construct the differential clock waveform using the following equation:

DiffClock = Clkp-Clkn

3 Construct the differential data waveform using the following equation:

DiffData = Dp-Dn

4 Using DiffClock's rising and falling edges, fold the DiffData to form a data eye.

5 By utilizing histogram, the Eye Height and Eye Width parameters are measured.

   a The Eye Height measurement is made at 50% location of the eye diagram.

   b The Eye Width measurement is made at the 0V threshold level.

6 Report the measured Eye Height and Eye Width.

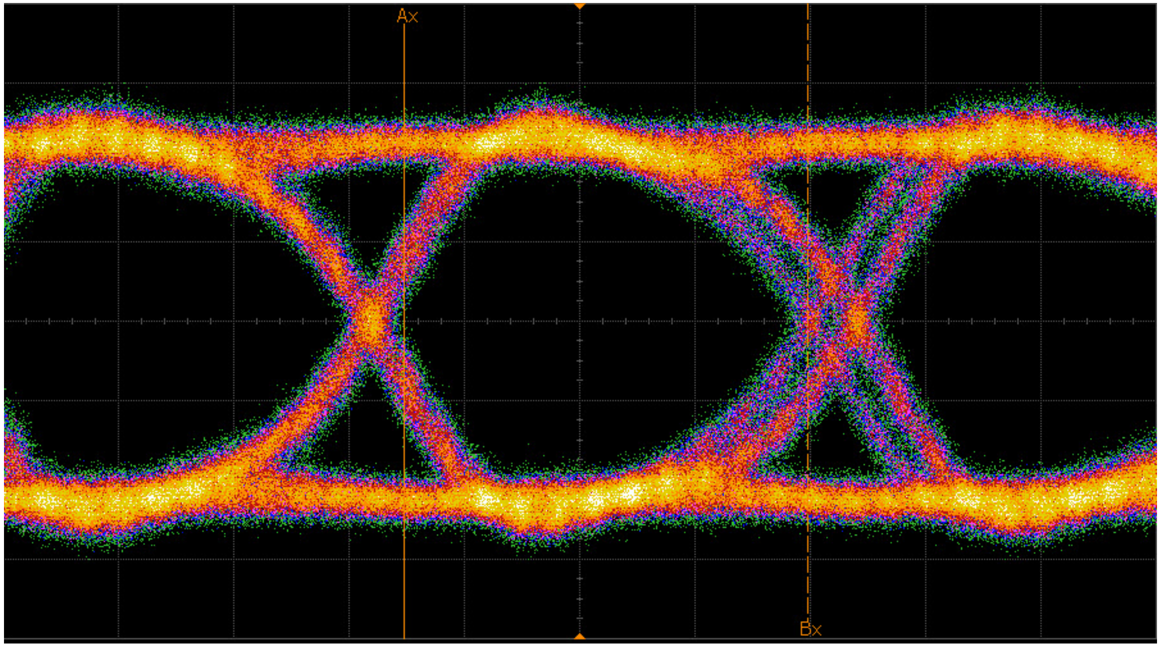
7 Compare measured Eye Height to the test limit. The test limit for this test is configurable under the **Configure** Tab of the application.

Test References

HS Data Eye Height Test is considered as Informative test.

HS Data Eye Width (Informative) Method of Implementation

This test measures the eye width parameter of the test data signal by generating an eye diagram based on the data and clock signal.



PASS Condition

The measured eye width must be within the limit as set by the user under the **Configure** tab of the application.

Test Availability Condition

Table 51 Test Availability Condition for HS Data Eye Width

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
916	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Enabled	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 916

NOTE Select **Informative Test** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 916 to remotely access the test.

1. This test requires the following pre-requisite test(s).
   a. HS Data Eye Height (Informative) (Test ID: 915)

   : Using DiffClock's rising and falling edges, fold the DiffData to form a data eye.

   : By utilizing histogram, the Eye Height and Eye Width parameters are measured.

   : The Eye Height measurement is made at 50% location of the eye diagram.

   : The Eye Width measurement is made at the 0V threshold level.
2. Report the measured Eye Height and Eye Width.
3. Compare measured Eye Width to the test limit. The test limit for this test is configurable under the **Configure** Tab of the application.

Test References

HS Data Eye Width Test is considered as Informative test.

Part B
MIPI D-PHY 1.1

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Part I
Electrical Characteristics

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12 MIPI D-PHY 1.1 High Speed Data Transmitter (HS Data TX) Electrical Tests

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Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($\Delta V_{CMTX}(_{1,0})$) Method of Implementation / 202
Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz (ΔV_{CMTX}(HF)) Method of Implementation / 202
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Test 1.3.4 HS Data TX Differential Voltage (V_{OD}) Method of Implementation / 202
Test 1.3.5 HS Data TX Differential Voltage Mismatch (? V_{OD}) Method of Implementation / 203
Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation / 203
Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation / 203
Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation / 203

This section provides the Methods of Implementation (MOIs) for the High Speed Data Transmitter (HS Data TX) Electrical tests using an Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 1.1 HS Data TX tests are the same as MIPI D-PHY 1.0 HS Data TX tests. Hence, they share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.0 High Speed Data Transmitter (HS Data TX) Electrical Tests".

The current chapter lists the references from the MIPI D-PHY 1.1 CTS.

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Probing for High Speed Data Transmitter Electrical Tests

When performing the HS Data TX tests, the MIPI D-PHY Test Application may prompt you to make changes to the physical setup. The connections for the HS Data TX tests may look similar to the following diagrams. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

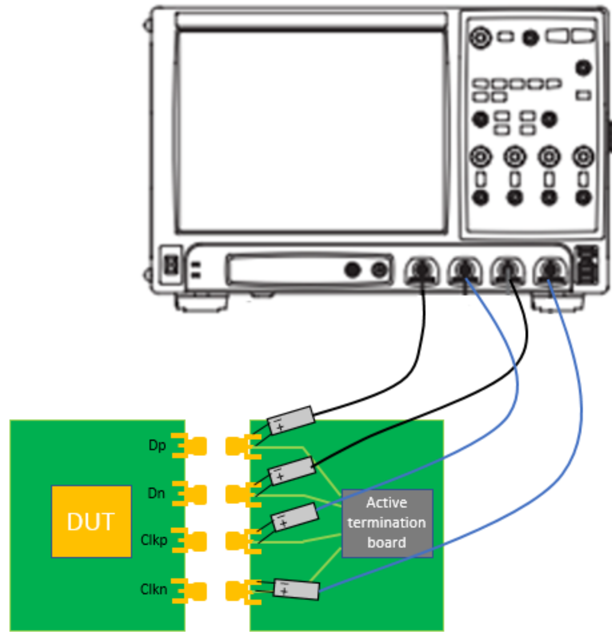

Figure 61 Probing for High Speed Data Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 61 are just for illustration).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in “Starting the MIPI D-PHY Test Application”.
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, ZID (termination resistance), Device ID and User Comments.
4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

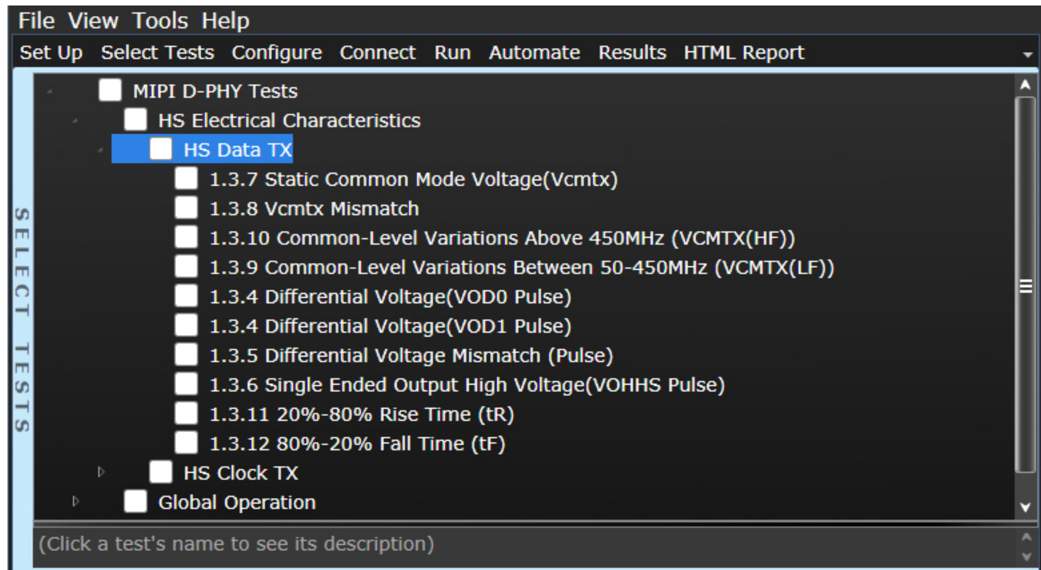

Figure 62 Selecting High Speed Data Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app’s task flow to set up the configuration options, run the tests and view the tests results.

Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation

For information about this test, refer to “Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation”.

Test References

See Test 1.3.7 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($\Delta V_{CMTX(1,0)}$) Method of Implementation

For information about this test, refer to “Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($\Delta V_{CMTX}(_{1,0})$) Method of Implementation”.

Test References

See Test 1.3.8 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz ($\Delta V_{CMTX(HF)}$) Method of Implementation

For information about this test, refer to “Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz (ΔV_{CMTX}(HF)) Method of Implementation”.

Test References

See Test 1.3.10 in CTS v1.1 and Section 9.1.1 Table 17 in the D-PHY Specification v1.1.

Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz ($\Delta V_{CMTX(LF)}$) Method of Implementation

For information about this test, refer to “Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz (ΔV_{CMTX}(LF)) Method of Implementation”.

Test References

See Test 1.3.9 in CTS v1.1 and Section 9.1.1 Table 17 in the D-PHY Specification v1.1.

Test 1.3.4 HS Data TX Differential Voltage (V_{OD}) Method of Implementation

For information about this test, refer to “Test 1.3.4 HS Data TX Differential Voltage (V_{OD}) Method of Implementation”.

Test References

See Test 1.3.4 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.3.5 HS Data TX Differential Voltage Mismatch (?V_{OD}) Method of Implementation

For information about this test, refer to "Test 1.3.5 HS Data TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation".

Test References

See Test 1.3.5 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation

For information about this test, refer to "Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation".

Test References

See Test 1.3.6 in CTS v1.1r03 (5June2013) and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation

For information about this test, refer to "Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation".

Test References

See Test 1.3.11 in CTS v1.1 and Section 9.1.1 Table 17 in the D-PHY Specification v1.1.

Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation

For information about this test, refer to "Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation".

Test References

See Test 1.3.12 in CTS v1.1 and Section 9.1.1 Table 17 in the D-PHY Specification v1.1.

13 MIPI D-PHY 1.1 High Speed Clock Transmitter (HS Clock TX) Electrical Tests

Probing for High Speed Clock Transmitter Electrical Tests / 206
Test 1.4.7 HS Clock TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation / 208
Test 1.4.8 HS Clock TX VCMTX Mismatch ($\Delta V_{CMTX}(_{1,0})$) Method of Implementation / 208
Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz (ΔV_{CMTX}(HF)) Method of Implementation / 208
Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz (ΔV_{CMTX}(LF)) Method of Implementation / 208
Test 1.4.4 HS Clock TX Differential Voltage (V_{OD}) Method of Implementation / 208
Test 1.4.5 HS Clock TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation / 209
Test 1.4.6 HS Clock TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation / 209
Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation / 209
Test 1.4.12 Clock Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation / 209
Test 1.4.17 HS Clock Instantaneous Method of Implementation / 209
Test 1.4.18 Clock Lane HS Clock Delta UI (UI variation) Method of Implementation / 210

This section provides the Methods of Implementation (MOIs) for the High Speed Clock Transmitter (HS Clock T_X) Electrical tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 1.1 HS Clock TX tests are the same as MIPI D-PHY 1.0 HS Clock TX tests. Hence, they share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. There is, however, an additional test that is supported by MIPI D-PHY 1.1 and not by MIPI D-PHY 1.0. The current chapter describes this test and lists the references from the MIPI D-PHY 1.1 CTS.

"Test 1.4.18 Clock Lane HS Clock Delta UI (UI variation) Method of Implementation"

For details of MIPI D-PHY 1.0 tests, refer to "MIPI D-PHY 1.0 High Speed Clock Transmitter (HS Clock TX) Electrical Tests".

KEYSIGHT TECHNOLOGIES

Probing for High Speed Clock Transmitter Electrical Tests

When performing the HS Clock T_X tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the HS Clock T_X tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

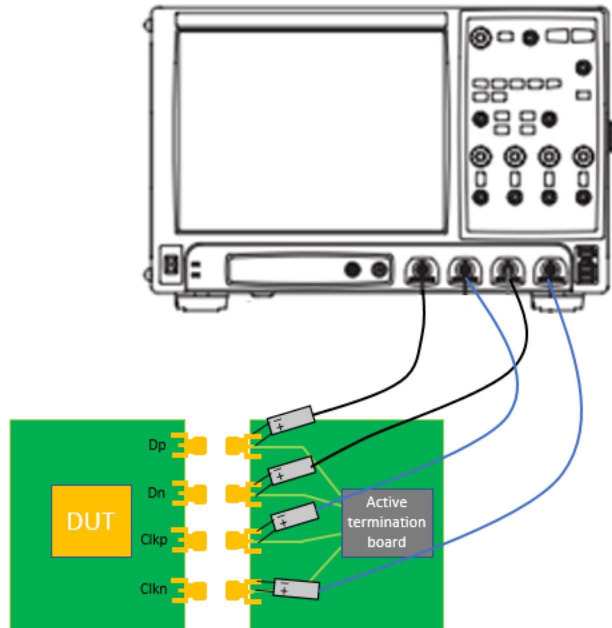

Figure 63 Probing for High Speed Clock Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 63 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, ZID (termination resistance), Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

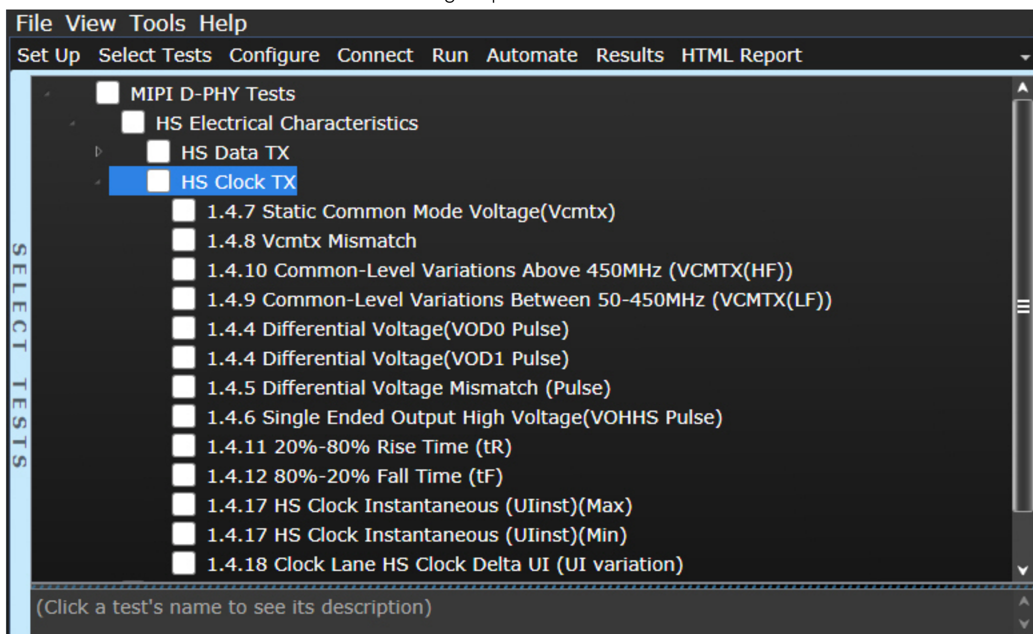

Figure 64 Selecting High Speed Clock Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.4.7 HS Clock TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation

For information about this test, refer to "Test 1.4.7 HS Clock TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation".

Test References

See Test 1.4.7 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.4.8 HS Clock TX V_{CMTX} Mismatch ($\Delta V_{CMTX(1,0)}$) Method of Implementation

For information about this test, refer to "Test 1.4.8 HS Clock TX VCMTX Mismatch ($\Delta V_{CMTX}(1,0)$) Method of Implementation".

Test References

See Test 1.4.8 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz ($\Delta V_{CMTX(HF)}$) Method of Implementation

For information about this test, refer to "Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz (ΔV_{CMTX}(HF)) Method of Implementation".

Test References

See Test 1.4.10 in CTS v1.1 and Section 9.1.1 Table 17 in the D-PHY Specification v1.1.

Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz ($\Delta V_{CMTX(LF)}$) Method of Implementation

For information about this test, refer to "Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz (ΔV_{CMTX}(LF)) Method of Implementation".

Test References

See Test 1.4.9 in CTS v1.1 and Section 9.1.1 Table 17 in the D-PHY Specification v1.1.

Test 1.4.4 HS Clock TX Differential Voltage (V_{OD}) Method of Implementation

For information about this test, refer to "Test 1.4.4 HS Clock TX Differential Voltage (V_{OD}) Method of Implementation".

Test References

See Test 1.4.4 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.4.5 HS Clock TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation

For information about this test, refer to "Test 1.4.5 HS Clock TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation".

Test References

See Test 1.4.5 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.4.6 HS Clock TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation

For information about this test, refer to "Test 1.4.6 HS Clock TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation".

Test References

See Test 1.4.6 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation

For information about this test, refer to "Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation".

Test References

See Test 1.4.11 in CTS v1.1 and Section 9.1.1 Table 17 in the D-PHY Specification v1.1.

Test 1.4.12 Clock Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation

For information about this test, refer to "Test 1.4.12 Clock Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation".

Test References

See Test 1.4.12 in CTS v1.1 and Section 9.1.1 Table 17 in the D-PHY Specification v1.1.

Test 1.4.17 HS Clock Instantaneous Method of Implementation

For information about this test, refer to "Test 1.4.17 HS Clock Instantaneous Method of Implementation".

Test References

See Test 1.4.17 in CTS v1.1 and Section 10.1 Table 26 in the D-PHY Specification v1.1.

Test 1.4.18 Clock Lane HS Clock Delta UI (UI variation) Method of Implementation

Clock Lane HS Clock Delta UI (UI variation) verifies that the frequency stability of the DUT HS Clock during a signal burst is within the conformance limits.

PASS Condition

The measured UI variation must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 52 Test Availability Condition for Test 1.4.18

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1911	Not Applicable	100 ohm	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 1911

NOTE Use the Test ID# 1911 to remotely access the test.

1. This test requires the following prerequisite test(s).
   a. HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)

   The minimum, maximum and average Unit Interval of the differential clock waveform is measured and stored.
2. Using MATLAB script, apply 1.98 MHz (33 kHz * 60 = 1.98 MHz) 2nd-order Butterworth low pass test filter to the measurement trend data.
3. Calculate the UI_Variant_min and UI_Variant_max according to the following equation:

   UI_Variant_min = ((UIinst_min - Uiinst_mean) / UIinst_mean) * 100%

   UI_Variant_max = ((UIinst_max - Uiinst_mean) / UIinst_mean) * 100%
4. Determine the UI_variant_worst based on the UI_Variant_min and UI_Variant_max calculated above.
5. Compare the worst measured value of UI_variant_worst with the conformance limit.

Test References

See Test 1.4.18 in CTS v1.1 and Section 10.1 Table 26 in the D-PHY Specification v1.1.

14 MIPI D-PHY 1.1 Low Power Data Transmitter (LP Data TX) Electrical Tests

Probing for Low Power Transmitter Electrical Tests / 212
Test 1.1.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation / 214
Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation / 216
Test 1.1.3 LP TX 15%-85% Rise Time Level (T_{RLP}) EscapeMode Method of Implementation / 218
Test 1.1.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation / 219
Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock ($T_{LP-PULSE-TX}$) Method of Implementation / 221
Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock ($T_{LP-PER-TX}$) Method of Implementation / 225
Test 1.1.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation / 227

This section provides the Methods of Implementation (MOIs) for the Low Power Data Transmitter (LP Data TX) Electrical tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

KEYSIGHT TECHNOLOGIES

Probing for Low Power Transmitter Electrical Tests

When performing the LP TX tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the LP TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test Application for the exact number of probe connections.

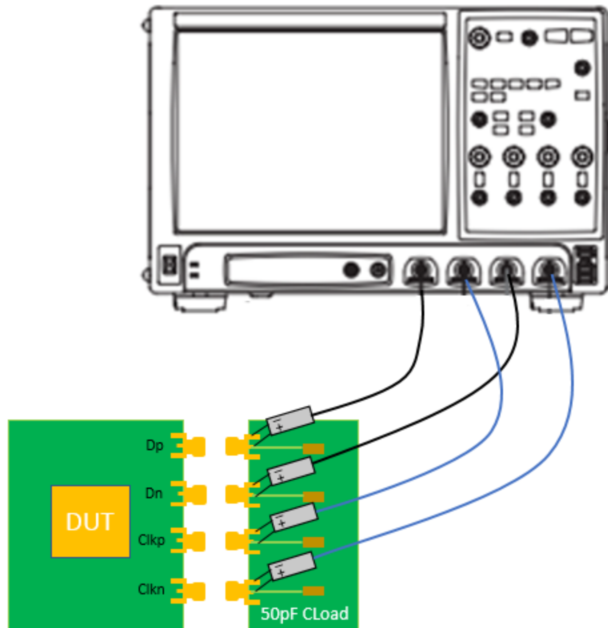

Figure 65 Probing for Low Power Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 65 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, ZID (termination resistance) Device ID and User Comments.
4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

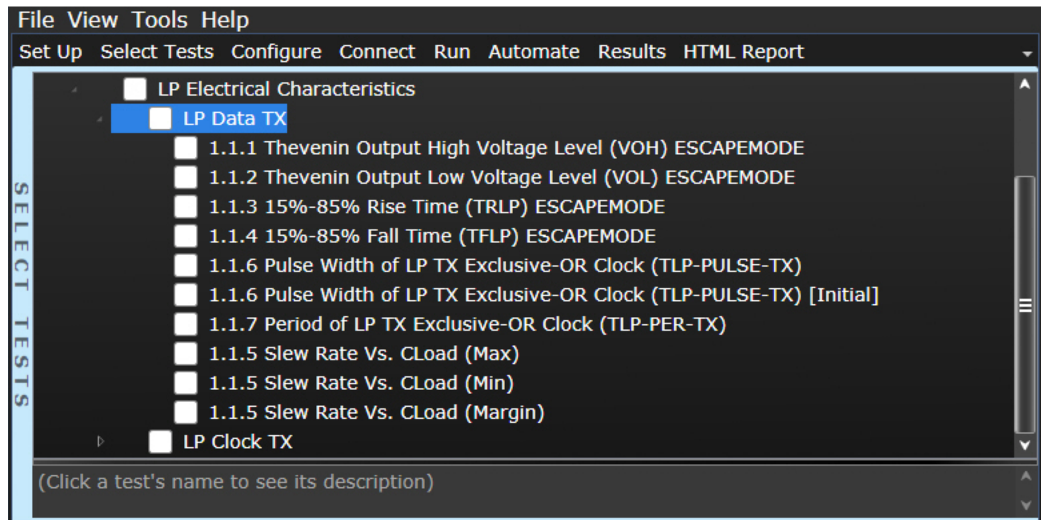

Figure 66 Selecting Low Power Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app’s task flow to set up the configuration options, run the tests and view the tests results.

Test 1.1.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation

V_{OH} is the Thevenin output high-level voltage in the high-level state, when the pad pin is not loaded.

PASS Condition

The measured V_{OH} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 53 Test Availability Conditions for Test 1.1.1

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
821	Not Applicable	Disabled	Not Applicable	Disabled	Not Applicable	Not Applicable	Enabled	Active Probe (Differential Probe)
8211	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	

Measurement Algorithm using Test ID 821

LP TX Thevenin Output High Voltage Level (V_{OH}) (Informative)

NOTE

Ensure that **Data LP EscapeMode** is disabled and **Informative Test** is enabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application. Use the Test ID# 821 to remotely access the test.

1 Trigger the Dp’s LP rising edge.
2 Position the trigger point at the center of the screen and make sure that the stable Dp LP high level voltage region is visible on the screen.
3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
4 Accumulate the data using the persistent display mode.
5 Enable the **Histogram** feature and measure the entire display region after the trigger location.
6 Take the mode value from the **Histogram** and use this value as V_{OH} for Dp.
7 Repeat steps 1 to 6 for Dn.
8 Report the measurement results.
  a V_{OH} value for Dp channel
  b V_{OH} value for Dn channel
9 Compare the measured worst value of V_{OH} with the compliance test limits.

Measurement Algorithm using Test ID 8211

LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE

NOTE

Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8211 to remotely access the test.

1. Trigger on LP Data EscapeMode pattern on the data signal. Without the presence of LP Escape mode, the trigger is unable to capture any valid signal for data processing.
2. Locate and use the Mark-1 state pattern to determine the end of the EscapeMode sequence.
3. Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired EscapeMode sequence waveform data.
4. Enable the **Histogram** feature and measure the entire LP Data EscapeMode sequence.
5. Take the mode value from the **Histogram** and use this value as V_{OH} for Dp.
6. Repeat steps 1 to 5 for Dn.
7. Report the measurement results.
   - *a* V_{OH} value for Dp channel
   - *b* V_{OH} value for Dn channel
8. Compare the measured worst value of V_{OH} with the conformance test limits.

Test References

See Test 1.1.1 in CTS v1.1 and Section 9.1.2 Table 18 in the D-PHY Specification v1.1.

Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation

V_{OL} is the Thevenin output low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low level state.

PASS Condition

The measured V_{OL} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 54 Test Availability Condition for Test 1.1.2

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
822	Not Applicable	Disabled	Not Applicable	Disabled	Not Applicable	Not Applicable	Enabled	Active Probe (Differential Probe)
8221	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	

Measurement Algorithm using Test ID 822

LP TX Thevenin Output Low Voltage Level (V_{OL}) (Informative)

NOTE Ensure that **Data LP EscapeMode** is disabled and **Informative Test** is enabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application. Use the Test ID# 822 to remotely access the test.

1. This test requires the following prerequisite test(s):
   a. HS Entry: DATA TX $T_{HS-PREPARE}$ (Test ID: 557)
2. Trigger the Dp's LP falling edge.
3. Position the trigger point at the center of the screen and make sure that the stable Dp LP low level voltage region is visible on the screen.
4. Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
5. Accumulate the data by using the persistent display mode.
6. Enable the **Histogram** feature and measure the entire display region after the trigger location.
7. Take the mode value from the **Histogram** and use this value as V_{OL} for Dp.
8. Repeat steps 1 to 7 for Dn.
9. Report the measurement results:
   a. V_{OL} value for Dp channel
   b. V_{OL} value for Dn channel
10. Compare the measured worst value of V_{OL} with the conformance test limits.

Measurement Algorithm using Test ID 8221

LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE

NOTE Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8221 to remotely access the test.

1. This test requires the following prerequisite tests:
   a. LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
2. Trigger on LP Data EscapeMode pattern on the data signal. Without the presence of the LP Escape mode, the trigger is unable to capture any valid signal for data processing.
3. Locate and use the Mark -1 state pattern to determine the end of the EscapeMode sequence.
4. Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired EscapeMode sequence waveform data.
5. Enable the **Histogram** feature and measure the entire LP data EscapeMode sequence.
6. Take the mode value from the **Histogram** and use this value as V_{OL} for Dp.
7. Repeat steps 1 to 6 for Dn.
8. Report the measurement results:
   a. V_{OL} value for Dp channel
   b. V_{OL} value for Dn channel
9. Compare the measured worst value of V_{OL} with the conformance test limits.

Test References

See Test 1.1.2 in CTS v1.1 and Section 9.1.2 Table 18 in the D-PHY Specification v1.1.

Test 1.1.3 LP TX 15%-85% Rise Time Level (T_{RLP}) EscapeMode Method of Implementation

The T_{RLP} is defined as 15%-85% rise time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD}. The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{RLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 55 Test Availability Condition for Test 1.1.3

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
8241	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 8241

NOTE Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8241 to remotely access the test.

1 This test requires the following prerequisite tests:
   a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
   b LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 8221)

   V_{OH} and V_{OL} values for Low Power signal measurements are performed and test results are stored.
2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3 A 400 MHz, 4th-order Butterworth low pass test filter is applied to the mentioned EscapeMode sequence data prior to performing the actual rise time measurement.
4 All the rising edges in the filtered EscapeMode sequence are processed in measuring the corresponding rise time.
5 The average 15%-85% rise time for Dp is recorded.
6 Repeat the steps for Dn.
7 Report the measurement results:
   a T_{RLP} average value for Dp channel
   b T_{RLP} average value for Dn channel
8 Compare the measured T_{RLP} worst value with the compliance test limit.

Test References

See Test 1.1.3 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Test 1.1.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation

The T_{FLP} is defined as 15%-85% fall time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD}. The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{FLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 56 Test Availability Condition for Test 1.1.4

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
825	Not Applicable	Disabled	Not Applicable	Disabled	Not Applicable	Not Applicable	Enabled	Active Probe (Differential Probe)
8251	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	

Measurement Algorithm using Test ID 825

LP TX 15%-85% Fall Time (T_{FLP}) (Informative)

NOTE Ensure that **Data LP EscapeMode** is disabled and **Informative Test** is enabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application. Use the Test ID# 825 to remotely access the test.

1. This test requires the following prerequisite tests:
   - *a* LP TX Thevenin Output High Voltage Level (V_{OH}) (Informative) (Test ID: 821)
   - *b* LP TX Thevenin Output Low Voltage Level (V_{OL}) (Informative) (Test ID: 822)

   Measure the V_{OH} and V_{OL} values for the low power signal and test results are stored.
2. All falling edges in LP are valid for this measurement.
3. Setup the trigger on LP falling edges.
4. Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
5. Depending on the number of observation configuration, the oscilloscope is triggered accordingly.
6. The average 15%-85% fall time for Dp is recorded.
7. Repeat the same trigger steps for Dn.
8. Report the measurement results:
   - *a* T_{FLP} average value for Dp channel
   - *b* T_{FLP} average value for Dn channel
9. Compare the measured worst value of T_{FLP} with the compliance test limits.

Measurement Algorithm using Test ID 8251

LP TX 15%-85% Fall Time (T_{FLP}) ESCAPEMODE

NOTE Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8251 to remotely access the test.

1 This test requires the following prerequisite tests:
   a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
   b LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 8221)

   Measure the V_{OH} and V_{OL} values for the low power signal and test results are stored.
2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to measuring the actual fall time.
4 All falling edges in the filtered EscapeMode sequence are processed in measuring the corresponding fall time.
5 The average 15%-85% fall time for Dp is recorded.
6 Repeat steps 1 to 5 for Dn.
7 Report the measurement results:
   a T_{FLP} average value for Dp channel
   b T_{FLP} average value for Dn channel
8 Compare the measured worst value of T_{FLP} with the compliance test limits.

Test References

See Test 1.1.4 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock ($T_{LP-PULSE-TX}$) Method of Implementation

$T_{LP-PULSE-TX}$ is defined as the pulse width of the DUT Low-Power TX XOR clock. A graphical representation of the XOR operation that creates the LP clock is shown below. The D-PHY Standard actually separates the $T_{LP-PULSE-TX}$ specification into two parts:

a The first LP XOR clock pulse after a Stop state, or the last LP XOR clock pulse before a Stop state must be wider than 40ns.

b All other LP XOR clock pulses must be wider than 20ns.

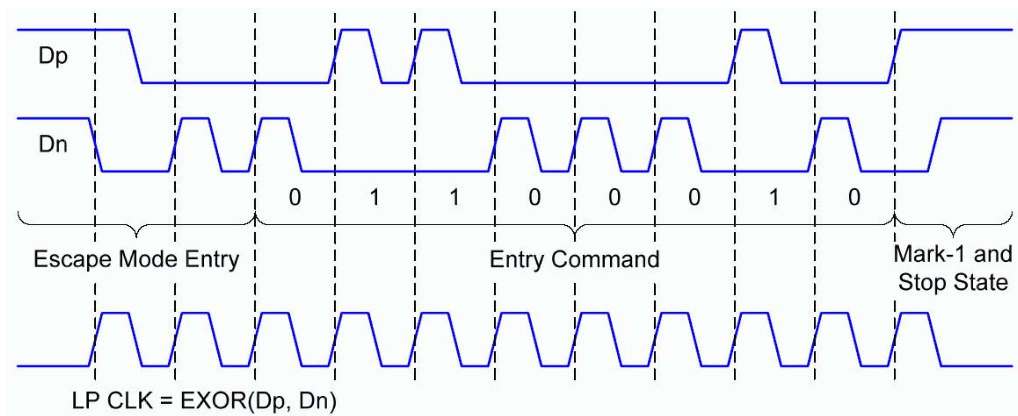

Figure 67 Graphical Representation of the XOR Operation

PASS Condition

The measured $T_{LP-PULSE-TX}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 57 Test Availability Condition for Test 1.1.6

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
827	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)
8271	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	
8272	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Enabled	

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1827	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	Active Probe (Differential Probe)
18271	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	
18272	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Enabled	

Measurement Algorithm using Test IDs 827, 8271 and 8272

LP TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP-PULSE-TX}$)

NOTE Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 827 to remotely access the test.

LP TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP-PULSE-TX}$) [Initial]

NOTE Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8271 to remotely access the test.

LP TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP-PULSE-TX}$) [Last]

NOTE Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8272 to remotely access the test.

1 This test requires the following prerequisite tests:
   a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211).
   This is to trigger and capture an EscapeMode sequence data from the test signal.
2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data.
4 Find all crossing points at the minimum trip level (500mV) and the maximum trip level (930mV) for Dp and Dn individually.
5 Find the initial pulse width, last pulse width and minimum width of all the other pulses at the specified minimum trip level and maximum trip level.
6 Find the rising-to-rising and falling-to-falling periods of the XOR clock at the mentioned minimum trip level and maximum trip level.
7 The worst case value for the pulse width found between the minimum trip level and maximum trip level will be used as the $T_{LP-PULSE-TX}$ value.
8 Compare the measured minimum $T_{LP-PULSE-TX}$ value with the compliance test limits.

Measurement Algorithm using Test IDs 1827, 18271 and 18272

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP-PULSE-TX}$)

NOTE Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 1827 to remotely access the test.

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP-PULSE-TX}$) [Initial]

NOTE Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 18271 to remotely access the test.

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP-PULSE-TX}$) [Last]

NOTE Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 18272 to remotely access the test.

1. This test requires the following prerequisite tests:
   a. LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)

   This is to trigger and capture an EscapeMode sequence data from the test signal.
2. The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3. Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data.
4. Find all crossing points at the minimum trip level (500mV) and the maximum trip level (930mV) for Clkp and Clkn individually.
5. Find the initial pulse width, last pulse width and minimum width of all the other pulses at the specified minimum trip level and maximum trip level.
6. Find the rising-to-rising and falling-to-falling periods of the XOR clock at the specified minimum trip level and maximum trip level.
7. The worst case value for the pulse width found between the minimum trip level and maximum trip level is used as the $T_{LP-PULSE-TX}$ value.
8. Compare the measured minimum $T_{LP-PULSE-TX}$ value with the compliance test limits.

Test References

See Test 1.1.6 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock ($T_{LP-PER-TX}$) Method of Implementation

$T_{LP-PER-TX}$ is defined as the period of the DUT Low-Power TX XOR clock. A graphical representation of the XOR operation that creates the LP clock is shown below. The D-PHY Standard separates the $T_{LP-PULSE-TX}$ specification into two parts:

a The first LP XOR clock pulse after a Stop state, or the last LP XOR clock pulse before a Stop state must be wider than 40ns.

b All other LP XOR clock pulses must be wider than 20ns.

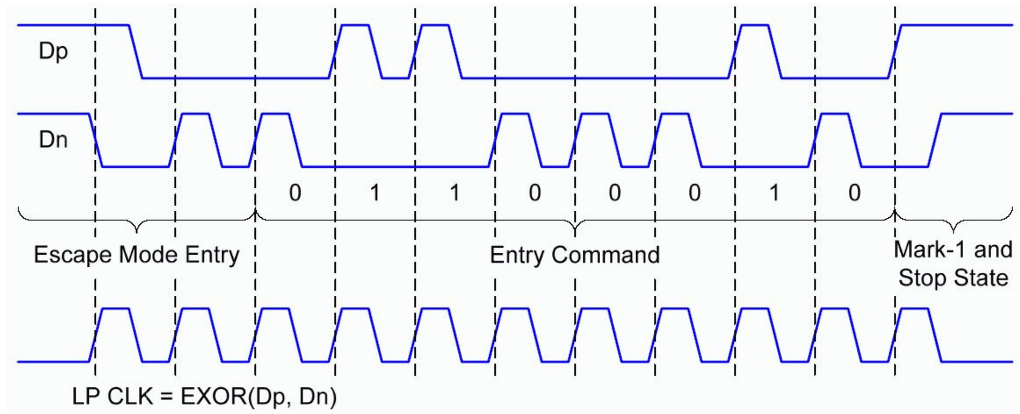

Figure 68 Graphical Representation of the XOR Operation

PASS Condition

The measured $T_{LP-PER-TX}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 58 Test Availability Condition for Test 1.1.7

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
828	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)
1828	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	

Measurement Algorithm using Test ID 828

LP TX Period of LP TX Exclusive-OR Clock ($T_{LP\text{-}PER\text{-}TX}$)

NOTE

Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 828 to remotely access the test.

1 This test requires the following prerequisite test(s).
   a LP TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP\text{-}PULSE\text{-}TX}$) (Test ID: 827)
   The actual measurement algorithm of the $T_{LP\text{-}PER\text{-}TX}$ is performed in the mentioned prerequisite test.
2 The minimum value for all the rising-to-rising and falling-to-falling periods of the XOR clock at the minimum trip level (500mV) and the maximum trip level (930mV) is used as the $T_{LP\text{-}PER\text{-}TX}$ result.
3 Compare the measured minimum $T_{LP\text{-}PER\text{-}TX}$ value to the compliance test limits.

Measurement Algorithm using Test ID 1828

LP Clock TX Period of LP TX Exclusive-OR Clock ($T_{LP\text{-}PER\text{-}TX}$)

NOTE

Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 1828 to remotely access the test.

1 This test requires the following prerequisite test(s).
   a LP Clock TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP\text{-}PULSE\text{-}TX}$) (Test ID: 1827)
   The actual measurement algorithm of the $T_{LP\text{-}PER\text{-}TX}$ is performed in the mentioned prerequisite test.
2 The minimum value for all the rising-to-rising and falling-to-falling periods of the XOR clock at the minimum trip level (500mV) and the maximum trip level (930mV) is used as the $T_{LP\text{-}PER\text{-}TX}$ result.
3 Compare the measured minimum $T_{LP\text{-}PER\text{-}TX}$ value with the compliance test limits.

Test References

See Test 1.1.7 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Test 1.1.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation

The slew rate $\delta V/\delta t_{SR}$ is the derivative of the LP transmitter output signal voltage over time. The intention of specifying a maximum slew rate value in the specification is to limit EMI (Electro Magnetic Interference).

The specification also states that the Slew Rate must be measured as an average across any 50mV segment of the output signal transition.

PASS Condition

The measured slew rate $\delta V/\delta t_{SR}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 59 Test Availability Condition for Test 1.1.5

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
829	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)
8291	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	
8292	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	

Measurement Algorithm using Test IDs 829, 8291 and 8292

NOTE

Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test.

- To access the LP TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 829.
- To access the LP TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 8291.
- To access the LP TX Slew Rate Vs. C_{Load} (Margin) test remotely, use the Test ID# 8292.

1 This test requires the following prerequisite tests:

   a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)

   b LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 8221)

   V_{OH} and V_{OL} values for low power signal measurements are performed and test results are stored.

2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.

3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to performing the actual slew rate measurement.

4 Perform the slew rate measurement on the filtered EscapeMode sequence for both Dp and Dn waveforms individually.
   For falling edge,
   a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
   b. Perform the slew rate measurement across the 400mV - 930mV region to determine the minimum slew rate result.

For rising edge,
a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
b. Perform the slew rate measurement across the 400mV - 700mV region to determine the minimum slew rate result.
c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700mV - 930mV region.

5. Calculate the average value from all rising edges' maximum slew rate results. Calculate the average value from all falling edges' maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.
6. Calculate the average value from all rising edges' minimum slew rate results. Calculate the average value from all falling edges' minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
7. Calculate the average value from all rising edges' slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
8. The Slew Rate maximum, minimum and margin result values are stored.
9. Report the measurement results.
10. Compare the measured worst slew rate value with the conformance test limits.

Test References

See Test 1.1.5 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

15 MIPI D-PHY 1.1 Low Power Clock Transmitter (LP Clock TX) Electrical Tests

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Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation / 232
Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation / 235
Test 1.2.3 LP TX 15%-85% Rise Time Level (T_{RLP}) Method of Implementation / 238
Test 1.2.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation / 240
Test 1.2.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation / 243

This section provides the Methods of Implementation (MOIs) for the Low Power Clock Transmitter (LP Clock TX) Electrical tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

KEYSIGHT TECHNOLOGIES

Probing for Low Power Transmitter Electrical Tests

When performing the LP TX tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the LP TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test Application for the exact number of probe connections.

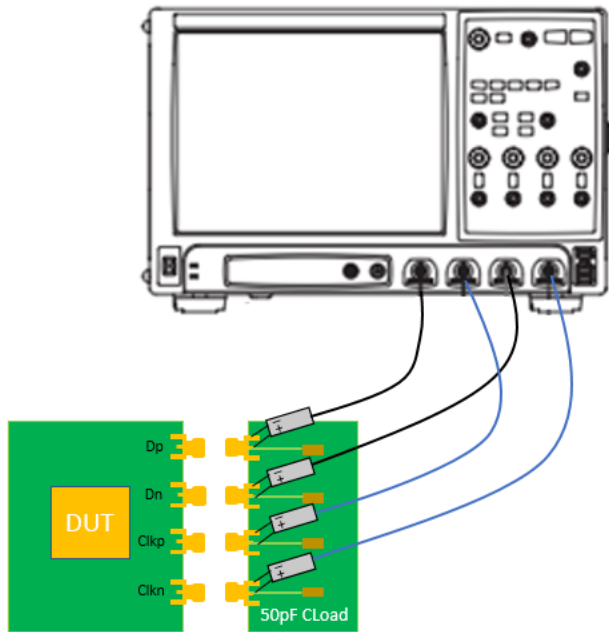

Figure 69 Probing for Low Power Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 69 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, ZID (termination resistance), Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

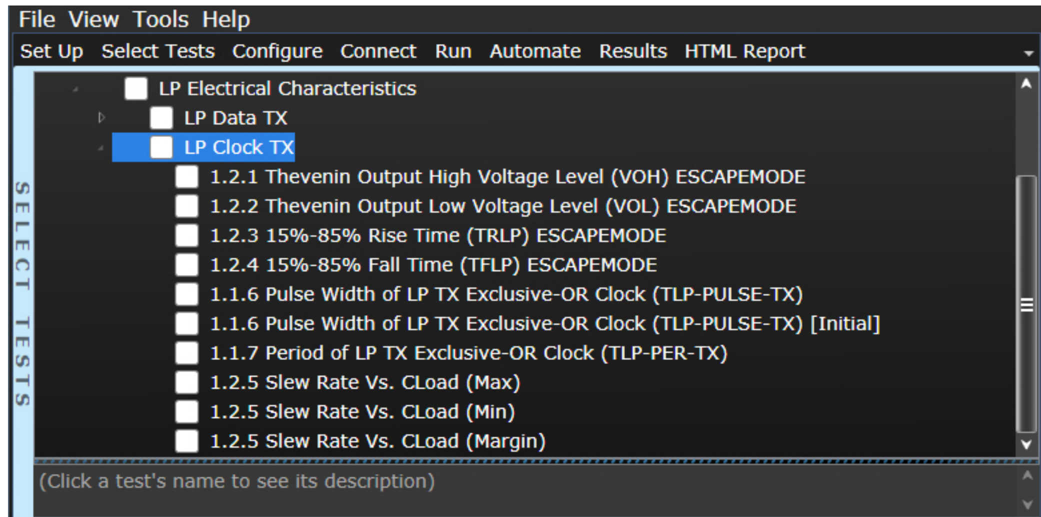

Figure 70 Selecting Low Power Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app’s task flow to set up the configuration options, run the tests and view the tests results.

Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation

V_{OH} is the Thevenin output high-level voltage in the high-level state, when the pad pin is not loaded.

PASS Condition

The measured V_{OH} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 60 Test Availability Condition for Test 1.2.1

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1821	Not Applicable	Not Applicable	Disabled	Not Applicable	Disabled	Disabled	Enabled	Active Probe (Differential Probe)
18211	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	
28211	Not Applicable	Not Applicable	Disabled	Not Applicable	Disabled	Enabled	Not Applicable	

Measurement Algorithm using Test ID 1821 and 28211

LP Clock TX Thevenin Output High Voltage Level (VOH) (Informative)

NOTE Ensure that the **Clock LP EscapeMode** and **Clock ULPS Mode** are disabled and **Informative Test** enabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application. Use the Test ID# 1821 to remotely access the test.

ULPS Clock TX Thevenin Output High Voltage Level (VOH) ULPSMODE

NOTE Select **Clock ULPS Mode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28211 to remotely access the test.

1 Trigger the Clkp's LP rising edge.
2 Position the trigger point at the center of the screen and make sure that the stable Clkp LP high level voltage region is visible on the screen.
3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
4 Accumulate the data by using the persistent display mode.
5 Enable the **Histogram** feature and measure the entire display region after the trigger location.
6 Take the mode value from the **Histogram** and use this value as V_{OH} for Clkp.
7 Repeat steps 1 to 6 for Clkn.

8 Report the measurement results.
   a V_{OH} value for Clkp channel
   b V_{OH} value for Clkn channel
9 Compare the measured worst value of V_{OH} with the compliance test limits.

Measurement Algorithm using Test ID 18211

LP Clock TX Thevenin Output High Voltage Level (VOH) ESCAPEMODE

NOTE Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18211 to remotely access the test.

1. Trigger on an EscapeMode pattern on the data signal. Without the presence of the LP Escape mode, the trigger is unable to capture any valid signal for data processing.
2. Locate and use the Mark-1 state pattern to determine the end of the EscapeMode sequence.
3. Apply a 400 MHz, 4th order Butterworth low pass test filter to the specified EscapeMode sequence data.
4. Enable the **Histogram** feature and measure the entire LP EscapeMode sequence.
5. Take the mode value from the **Histogram** and use this value as V_{OH} for Clkp.
6. Repeat steps 1 to 4 for Clkn.
7. Report the measurement results.
   a. V_{OH} value for Clkp channel
   b. V_{OH} value for Clkn channel
8. Compare the measured worst value of V_{OH} with the compliance test limits.

Test References

See Test 1.2.1 in CTS v1.1 and Section 9.1.2 Table 18 in the D-PHY Specification v1.1.

Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation

V_{OL} is the Thevenin output low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low level state.

PASS Condition

The measured V_{OL} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 61 Test Availability Condition for Test 1.2.2

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1822	Not Applicable	Not Applicable	Disabled	Not Applicable	Disabled	Disabled	Enabled	Active Probe (Differential Probe)
18221	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	
28221	Not Applicable	Not Applicable	Disabled	Not Applicable	Disabled	Enabled	Not Applicable	

Measurement Algorithm using Test ID 1822

LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) (Informative)

NOTE Ensure that the **Clock LP EscapeMode** and **Clock ULPS Mode** are disabled and **Informative Test** enabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application. Use the Test ID# 1822 to remotely access the test.

1 This test requires the following prerequisite tests:
   a HS Entry: CLK TX $T_{CLK-PREPARE}$ (Test ID: 552)
2 Trigger the Clkp's LP falling edge.
3 Position the trigger point at the center of the screen and make sure that the stable Clkp LP low level voltage region is visible on the screen.
4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
5 Accumulate the data by using the persistent display mode.
6 Enable the **Histogram** feature and measure the entire display region after the trigger location.
7 Take the mode value from the **Histogram** and use this value as V_{OL} for Clkp.
8 Repeat steps 1 to 7 for Clkn.
9 Report the measurement results:
   a V_{OL} value for Clkp channel
   b V_{OL} value for Clkn channel
10 Compare the measured worst value of V_{OL} with the compliance test limits.

Measurement Algorithm using Test ID 18221

LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE

NOTE Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18221 to remotely access the test.

1 This test requires the following prerequisite tests:
   a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
2 Trigger on an EscapeMode pattern on the data signal. Without the presence of LP Escape mode, the trigger is unable to capture any valid signal for data processing.
3 Locate and use the Mark -1 state pattern to determine the end of the EscapeMode sequence.
4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data.
5 Enable the **Histogram** feature and measure the entire LP EscapeMode sequence.
6 Take the mode value from the **Histogram** and use this value as V_{OL} for Clkp.
7 Repeat steps 1 to 6 for Clkn.
8 Report the measurement results:
   a V_{OL} value for Clkp channel
   b V_{OL} value for Clkn channel
9 Compare the measured worst value of V_{OL} with the compliance test limits.

Measurement Algorithm using Test ID 28221

ULPS Clock TX Thevenin Output Low Voltage Level (V_{OL}) ULPSMODE

NOTE Select **Clock ULPS Mode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28221 to remotely access the test.

1 This test requires the following prerequisite test(s):
   a ULPS Clock TX Thevenin Output High Voltage Level (VOH) ULPSMODE (Test ID: 28211)
2 Trigger the Clkp's LP falling edge.
3 Position the trigger point at the center of the screen and make sure that the stable Clkp LP low level voltage region is visible on the screen.
4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
5 Accumulate the data by using the persistent display mode.
6 Enable the **Histogram** feature and measure the entire display region after the trigger location.
7 Take the mode value from the **Histogram** and use this value as V_{OL} for Clkp.
8 Repeat steps 1 to 7 for Clkn.
9 Report the measurement results:
   a V_{OL} value for Clkp channel
   b V_{OL} value for Clkn channel
10 Compare the measured worst value of V_{OL} with the conformance test limits.

Test References

See Test 1.2.2 in CTS v1.1 and Section 9.1.2 Table 18 in the D-PHY Specification v1.1.

Test 1.2.3 LP TX 15%-85% Rise Time Level (T_{RLP}) Method of Implementation

The T_{RLP} is defined as 15%-85% rise time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD}. The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{RLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 62 Test Availability Condition for Test 1.2.3

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
18241	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	Active Probe (Differential Probe)
28241	Not Applicable	Not Applicable	Disabled	Not Applicable	Disabled	Enabled	Not Applicable	

Measurement Algorithm using Test ID 18241

LP Clock TX 15%-85% Rise Time (T_{RLP}) ESCAPEMODE

NOTE Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18241 to remotely access the test.

1 This test requires the following prerequisite tests:
   a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
   b LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 18221)

   V_{OH} and V_{OL} values for Low Power signal measurements are performed and test results are stored.
2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to performing the actual rise time measurement.
4 Perform rise time measurement on the filtered EscapeMode sequence for both Clkp and Clkn waveforms individually.
5 The max, mean and min result values are stored.
6 Report the measurement results:
   a T_{RLP} average value for Clkp channel
   b T_{RLP} average value for Clkn channel
7 Compare the measured T_{RLP} worst value derived from the T_{RLP} average value for Clkp and Clkn to the compliance test limit.

Measurement Algorithm using Test ID 28241

ULPS Clock TX 15%-85% Rise Time (TRLP) ULPSMODE

NOTE Select **Clock ULPS Mode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28241 to remotely access the test.

1. This test requires the following prerequisite tests:
   a. ULPS Clock TX Thevenin Output High Voltage Level (V_{OH}) ULPSMODE (Test ID: 28211)
   b. ULPS Clock TX Thevenin Output Low Voltage Level (V_{OL}) ULPSMODE (Test ID: 28221)

   V_{OH} and V_{OL} values for Low Power signal measurements are performed and test results are stored.
2. The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3. Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to performing the actual rise time measurement.
4. Perform rise time measurement on the filtered EscapeMode sequence for both Clkp and Clkn waveforms individually.
5. The max, mean and min result values are stored.
6. Report the measurement results:
   a. T_{RLP} average value for Clkp channel
   b. T_{RLP} average value for Clkn channel
7. Compare the measured T_{RLP} worst value derived from the T_{RLP} average value for Clkp and Clkn to the compliance test limit.

Test References

See Test 1.2.3 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Test 1.2.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation

The T_{FLP} is defined as 15%-85% fall time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD}. The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{FLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 63 Test Availability Condition for Test 1.2.4

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1825	Not Applicable	Not Applicable	Disabled	Not Applicable	Disabled	Disabled	Enabled	Active Probe (Differential Probe)
18251	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	
28251	Not Applicable	Not Applicable	Disabled	Not Applicable	Disabled	Enabled	Not Applicable	

Measurement Algorithm using Test ID 1825

LP Clock TX 15%-85% Fall Time (T_{FLP}) (Informative)

NOTE Ensure that the **Clock LP EscapeMode** and **Clock ULPS Mode** are disabled and **Informative Test** enabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application. Use the Test ID# 1825 to remotely access the test.

1 This test requires the following prerequisite tests:
   a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) (Informative) (Test ID: 1821)
   b LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) (Informative) (Test ID: 1822)

   V_{OH} and V_{OL} values for Low Power signal measurements are performed and test results are stored.
2 Trigger is setup to trigger on LP falling edges.
3 The oscilloscope is triggered to capture the falling edges to be processed based on the “LP Observations” configuration in the **Configure** tab.
4 Apply a 400 MHz, 4th-order Butterworth low pass test filter to the specified triggered data prior to performing the actual fall time measurement.
5 The average 15%-85% fall time for Clkp is recorded.
6 Repeat the same trigger steps for Clkn.
7 Report the measurement results:
   a T_{FLP} average value for Clkp channel
   b T_{FLP} average value for Clkn channel

8 Compare the measured worst value of T_{FLP} with the compliance test limits.

Measurement Algorithm using Test ID 18251

LP Clock TX 15%-85% Fall Time (T_{FLP}) ESCAPEMODE

NOTE Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18251 to remotely access the test.

1 This test requires the following prerequisite tests:
   a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
   b LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 18221)

   V_{OH} and V_{OL} values for low power signal measurements are performed and test results are stored.
2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to performing the actual fall time measurement.
4 Perform fall time measurement on the filtered EscapeMode sequence for both Clkp and Clkn waveforms individually.
5 The maximum, mean and minimum result values are stored.
6 Report the measurement results:
   a T_{FLP} average value for Clkp channel
   b T_{FLP} average value for Clkn channel
7 Compare the measured worst value of T_{FLP} derived from the average value of T_{FLP} for Clkp and Clkn to the compliance test limits.

Measurement Algorithm using Test ID 28251

ULPS Clock TX 15%-85% Fall Time (T_{FLP}) ULPSMODE

NOTE Select **Clock ULPS Mode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28251 to remotely access the test.

1 This test requires the following prerequisite tests:
   a ULPS Clock TX Thevenin Output High Voltage Level (V_{OH}) ULPSMODE (Test ID: 28211)
   b ULPS Clock TX Thevenin Output Low Voltage Level (V_{OL}) ULPSMODE (Test ID: 28221)

   V_{OH} and V_{OL} values for low power signal measurements are performed and test results are stored.
2 Trigger is setup to trigger on LP falling edges.
3 The oscilloscope is triggered to capture the falling edges to be processed based on the “LP Observations” configuration in the **Configure** tab.
4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned trigger data prior to measuring the actual fall time.
5 The average 15%-85% fall time for Clkp is recorded.
6 Repeat the same trigger steps for Clkn.

7 Report the measurement results:
   a T_{FLP} average value for Clkp channel
   b T_{FLP} average value for Clkn channel
8 Compare the measured worst value of T_{FLP} to the compliance test limits.

Test References

See Test 1.2.4 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Test 1.2.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation

The slew rate $\delta V/\delta t_{SR}$ is the derivative of the LP transmitter output signal voltage over time. The intention of specifying a maximum slew rate value in the specification is to limit EMI (Electro Magnetic Interference).

The specification also states that the Slew Rate must be measured as an average across any 50mV segment of the output signal transition.

PASS Condition

The measured slew rate $\delta V/\delta t_{SR}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 64 Test Availability Condition for Test 1.2.5

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1829	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	Active Probe (Differential Probe)
18291	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	
18292	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	
2829	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Enabled	Not Applicable	
28291	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Enabled	Not Applicable	
28292	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Enabled	Not Applicable	

Measurement Algorithm using Test ID 1829, 18291 and 18292

LP Clock TX Slew Rate Vs. C_{Load} (Max) /

LP Clock TX Slew Rate Vs. C_{Load} (Min) /

LP Clock TX Slew Rate Vs. C_{Load} (Margin)

NOTE

Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test.

- To access the LP Clk TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 1829.
- To access the LP Clk TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 18291.
- To access the LP Clk TX Slew Rate Vs. C_{Load} (Margin) test remotely, use the Test ID# 18292.

1 This test requires the following prerequisite tests:
   a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
   b LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 18221)

   V_{OH} and V_{OL} values for low power signal measurements are performed and test results are stored.
2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to performing the actual slew rate measurement.
4 Perform the slew rate measurement on the filtered EscapeMode sequence for both Clkp and Clkn waveforms individually.
   For falling edge,
   a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
   b. Perform the slew rate measurement across the 400mV - 930mV region to determine the minimum slew rate result.
   For rising edge,
   a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
   b. Perform the slew rate measurement across the 400mV - 700mV region to determine the minimum slew rate result.
   c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700mV - 930mV region.
5 Calculate the average value from all rising edges' maximum slew rate results. Calculate the average value from all falling edges' maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.
6 Calculate the average value from all rising edges' minimum slew rate results. Calculate the average value from all falling edges' minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
7 Calculate the average value from all rising edges' slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
8 The Slew Rate maximum, minimum and margin result values are stored.
9 Report the measurement results.
10 Compare the measured worst slew rate value for Clkp and Clkn to the compliance test limits.

ULPS Clock TX Slew Rate Vs. C_{Load} (Max) ULPSMODE/

ULPS Clock TX Slew Rate Vs. C_{Load} (Min) ULPSMODE/

ULPS Clock TX Slew Rate Vs. C_{Load} (Margin) ULPSMODE

Measurement Algorithm using Test ID 2829, 28291 and 28292

NOTE

Select **Clock ULPS Mode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test.

- To access the ULPS Clk TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 2829.
- To access the ULPS Clk TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 28291.
- To access the ULPS Clk TX Slew Rate Vs. C_{Load} (Margin) test remotely, use the Test ID# 28292.

1 This test requires the following prerequisite tests:
   a ULPS Clock TX Thevenin Output High Voltage Level (V_{OH}) ULPSMODE (Test ID: 28211)
   b ULPS Clock TX Thevenin Output Low Voltage Level (V_{OL}) ULPSMODE (Test ID: 28221)

   V_{OH} and V_{OL} values for low power signal measurements are performed and test results are stored.
2 The oscilloscope is triggered to capture rising and falling edges to be processed based on the “Number of ULPS Slew Edge” configuration in the **Configure** tab.
3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired waveform data prior to performing the actual slew rate measurement.
4 Perform the slew rate measurement on the mentioned triggered data for both Clkp and Clkn waveforms individually.
   For falling edge,
   a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
   b. Perform the slew rate measurement across the 400mV - 930mV region to determine the minimum slew rate result.
   For rising edge,
   a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
   b. Perform the slew rate measurement across the 400mV - 700mV region to determine the minimum slew rate result.
   c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700mV - 930mV region.
5 Calculate the average value from all rising edges’ maximum slew rate results. Calculate the average value from all falling edges’ maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.
6 Calculate the average value from all rising edges’ minimum slew rate results. Calculate the average value from all falling edges’ minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
7 Calculate the average value from all rising edges’ slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
8 The Slew Rate maximum, minimum and margin result values are stored.
9 Report the measurement results.

10 Compare the measured worst slew rate value for Clkp and Clkn to the compliance test limits.

Test References

See Test 1.2.5 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Part II
Global Operation

KEYSIGHT
TECHNOLOGIES

16 MIPI D-PHY 1.1 Data Transmitter (Data TX) Global Operation Tests

Probing for Data TX Global Operation Tests / 250
Test 1.3.1 HS Entry: Data T_{LPX} Method of Implementation / 252
Test 1.3.2 HS Entry: Data TX $T_{HS\text{-}PREPARE}$ Method of Implementation / 252
Test 1.3.3 HS Entry: Data TX $T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$ Method of Implementation / 252
Test 1.3.13 HS Exit: Data TX $T_{HS\text{-}TRAIL}$ Method of Implementation / 252
Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{REOT}) Method of Implementation / 252
Test 1.3.15 HS Exit: Data TX T_{EOT} Method of Implementation / 252
Test 1.3.16 HS Exit: Data TX $T_{HS\text{-}EXIT}$ Method of Implementation / 253

This section provides the Methods of Implementation (MOIs) for the Data Transmitter (Data TX) Global Operation tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 1.1 Data TX Global Operation tests are the same as MIPI D-PHY 1.0 Data TX Global Operation tests. Hence, they share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.0 Data Transmitter (Data TX) Global Operation Tests".

The current chapter lists the references from the MIPI D-PHY 1.1 CTS.

KEYSIGHT TECHNOLOGIES

Probing for Data TX Global Operation Tests

When performing the Data TX tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the Data TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test Application for the exact number of probe connections.

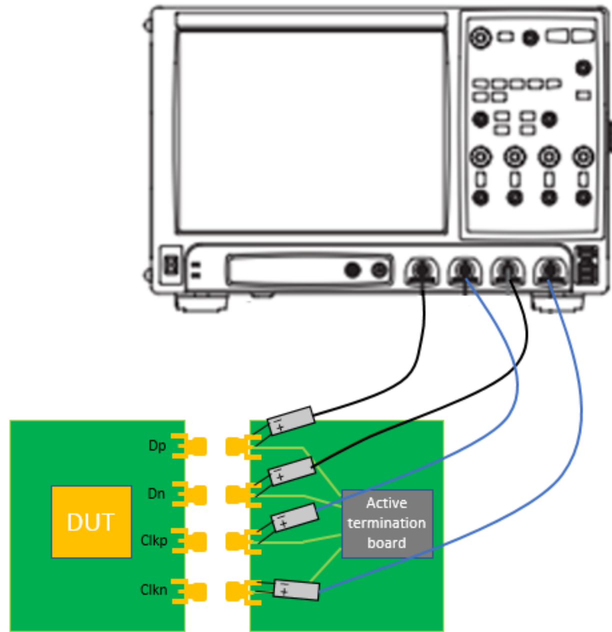

Figure 71 Probing for Data TX Global Operation Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 71 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, ZID (termination resistance) Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

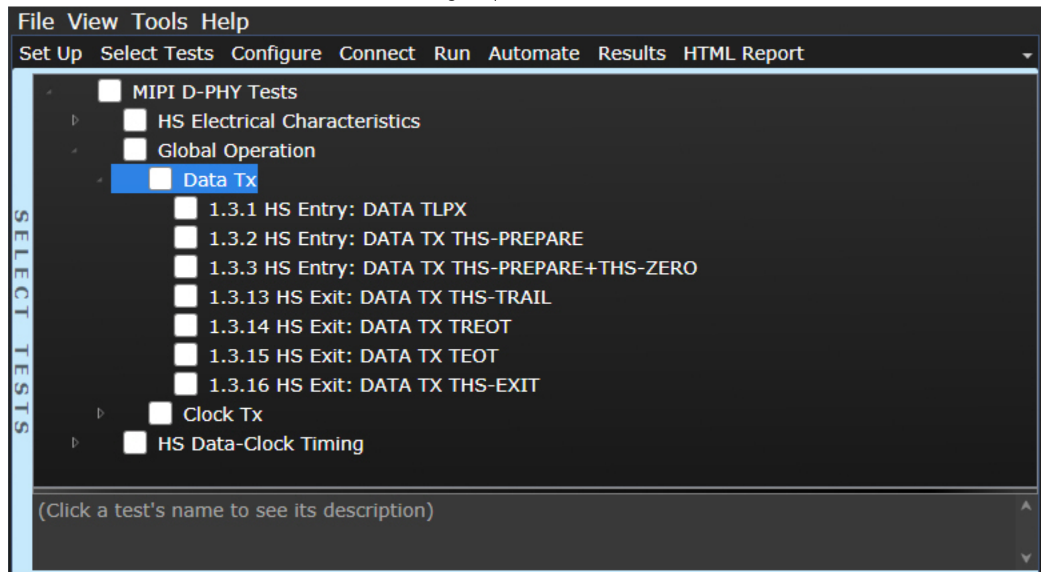

Figure 72 Selecting Data TX Global Operation Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.3.1 HS Entry: Data T_{LPX} Method of Implementation

For information about this test, refer to "Test 1.3.1 HS Entry: Data T_{LPX} Method of Implementation".

Test References

See Test 1.3.1 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.3.2 HS Entry: Data TX $T_{HS\text{-}PREPARE}$ Method of Implementation

For information about this test, refer to "Test 1.3.2 HS Entry: Data TX $T_{HS\text{-}PREPARE}$ Method of Implementation".

Test References

See Test 1.3.2 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.3.3 HS Entry: Data TX $T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$ Method of Implementation

For information about this test, refer to "Test 1.3.3 HS Entry: Data TX $T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$ Method of Implementation".

Test References

See Test 1.3.3 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.3.13 HS Exit: Data TX $T_{HS\text{-}TRAIL}$ Method of Implementation

For information about this test, refer to "Test 1.3.13 HS Exit: Data TX $T_{HS\text{-}TRAIL}$ Method of Implementation".

Test References

See Test 1.3.13 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{REOT}) Method of Implementation

For information about this test, refer to "Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{REOT}) Method of Implementation".

Test References

See Test 1.3.14 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Test 1.3.15 HS Exit: Data TX T_{EOT} Method of Implementation

For information about this test, refer to "Test 1.3.15 HS Exit: Data TX T_{EOT} Method of Implementation".

Test References

See Test 1.3.15 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.3.16 HS Exit: Data TX $T_{HS-EXIT}$ Method of Implementation

For information about this test, refer to "Test 1.3.16 HS Exit: Data TX $T_{HS-EXIT}$ Method of Implementation".

Test References

See Test 1.3.16 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

17 MIPI D-PHY 1.1 Clock Transmitter (Clock TX) Global Operation Tests

Probing for Clock TX Global Operation Tests / 256
Test 1.4.1 HS Entry: CLK TX T_{LPX} Method of Implementation / 258
Test 1.4.2 HS Entry: CLK TX $T_{CLK-PREPARE}$ Method of Implementation / 258
Test 1.4.3 HS Entry: CLK TX $T_{CLK-PREPARE}$+$T_{CLK-ZERO}$ Method of Implementation / 258
Test 1.5.1 HS Entry: CLK TX $T_{CLK-PRE}$ Method of Implementation / 258
Test 1.5.2 HS Exit: CLK TX $T_{CLK-POST}$ Method of Implementation / 258
Test 1.4.13 HS Exit: CLK TX $T_{CLK-TRAIL}$ Method of Implementation / 258
Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{REOT}) Method of Implementation / 259
Test 1.4.15 HS Exit: CLK TX T_{EOT} Method of Implementation / 259
Test 1.4.16 HS Exit: CLK TX $T_{HS-EXIT}$ Method of Implementation / 259

This section provides the Methods of Implementation (MOIs) for the Clock Transmitter (Clock TX) Global Operation tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 1.1 Clock TX Global Operation tests are the same as MIPI D-PHY 1.0 Clock TX Global Operation tests. Hence, they share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.0 Clock Transmitter (Clock TX) Global Operation Tests".

The current chapter lists the references from the MIPI D-PHY 1.1 CTS.

KEYSIGHT TECHNOLOGIES

Probing for Clock TX Global Operation Tests

When performing the Clock TX tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the Clock TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test Application for the exact number of probe connections.

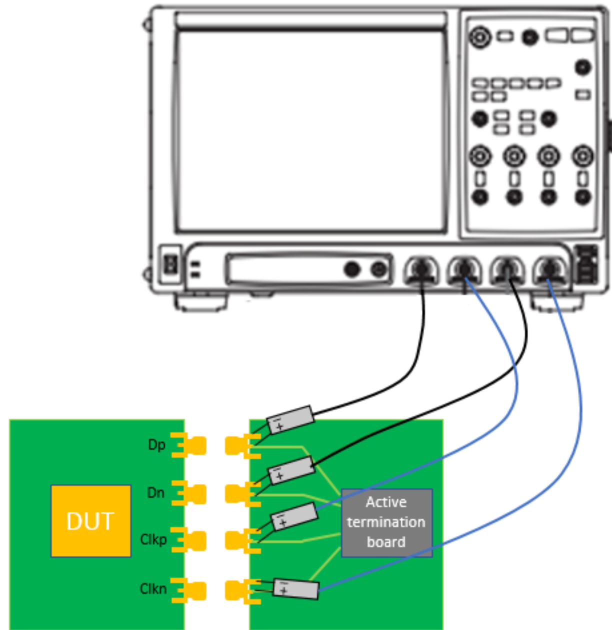

Figure 73 Probing for Clock TX Global Operation Tests

You can identify the channels used for each signal in the Configuration tab of the MIPI D-PHY Test Application. (The channels shown in Figure 73 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, ZID (termination resistance), Device ID and User Comments.
4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

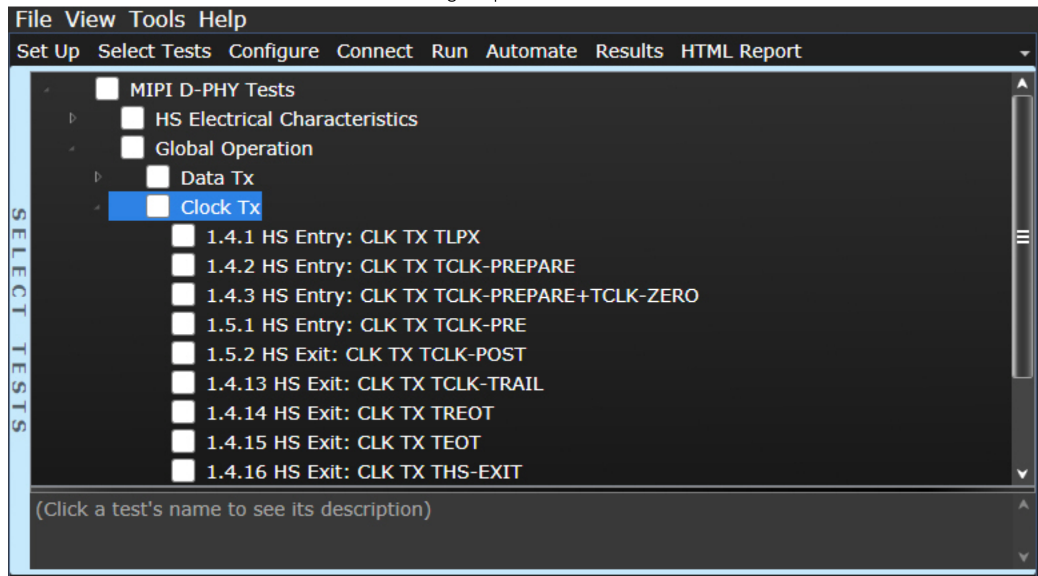

Figure 74 Selecting Clock TX Global Operation Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.4.1 HS Entry: CLK TX T_{LPX} Method of Implementation

For information about this test, refer to "Test 1.4.1 HS Entry: CLK TX T_{LPX} Method of Implementation".

Test References

See Test 1.4.1 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.4.2 HS Entry: CLK TX $T_{CLK-PREPARE}$ Method of Implementation

For information about this test, refer to "Test 1.4.2 HS Entry: CLK TX $T_{CLK-PREPARE}$ Method of Implementation".

Test References

See Test 1.4.2 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.4.3 HS Entry: CLK TX $T_{CLK-PREPARE}+T_{CLK-ZERO}$ Method of Implementation

For information about this test, refer to "Test 1.4.3 HS Entry: CLK TX $T_{CLK-PREPARE}+T_{CLK-ZERO}$ Method of Implementation".

Test References

See Test 1.4.3 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.5.1 HS Entry: CLK TX $T_{CLK-PRE}$ Method of Implementation

For information about this test, refer to "Test 1.5.1 HS Entry: CLK TX $T_{CLK-PRE}$ Method of Implementation".

Test References

See Test 1.5.1 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.5.2 HS Exit: CLK TX $T_{CLK-POST}$ Method of Implementation

For information about this test, refer to "Test 1.5.2 HS Exit: CLK TX $T_{CLK-POST}$ Method of Implementation".

Test References

See Test 1.5.2 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.4.13 HS Exit: CLK TX $T_{CLK-TRAIL}$ Method of Implementation

For information about this test, refer to "Test 1.4.13 HS Exit: CLK TX $T_{CLK-TRAIL}$ Method of Implementation".

Test References

See Test 1.4.13 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{REOT}) Method of Implementation

For information about this test, refer to "Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{REOT}) Method of Implementation".

Test References

See Test 1.4.14 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Test 1.4.15 HS Exit: CLK TX T_{EOT} Method of Implementation

For information about this test, refer to "Test 1.4.15 HS Exit: CLK TX T_{EOT} Method of Implementation".

Test References

See Test 1.4.15 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.4.16 HS Exit: CLK TX $T_{HS-EXIT}$ Method of Implementation

For information about this test, refer to "Test 1.4.16 HS Exit: CLK TX $T_{HS-EXIT}$ Method of Implementation".

Test References

See Test 1.4.16 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Part III HS Data-Clock Timing

KEYSIGHT
TECHNOLOGIES

18 MIPI D-PHY 1.1 High Speed (HS) Data-Clock Timing Tests

Probing for High Speed Data-Clock Timing Tests / 264
Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation / 266
Test 1.5.4 Data-to-Clock Skew ($T_{SKEW(TX)}$) Method of Implementation / 266

This section provides the Methods of Implementation (MOIs) for the High Speed (HS) Data-Clock Timing tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 1.1 High Speed (HS) Data-Clock Timing tests are the same as MIPI D-PHY 1.0 High Speed (HS) Data-Clock Timing tests. Hence, they share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.0 High Speed (HS) Data-Clock Timing Tests"

The current chapter lists the references from the MIPI D-PHY 1.1 CTS.

Probing for High Speed Data-Clock Timing Tests

When performing the HS Data-Clock Timing tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the HS Data-Clock Timing tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

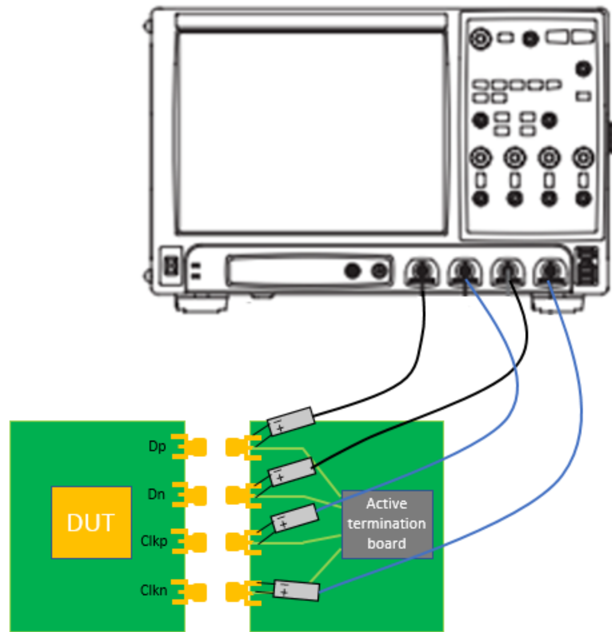

Figure 75 Probing for HS Data-Clock Timing Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 75 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, ZID (termination resistance), Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

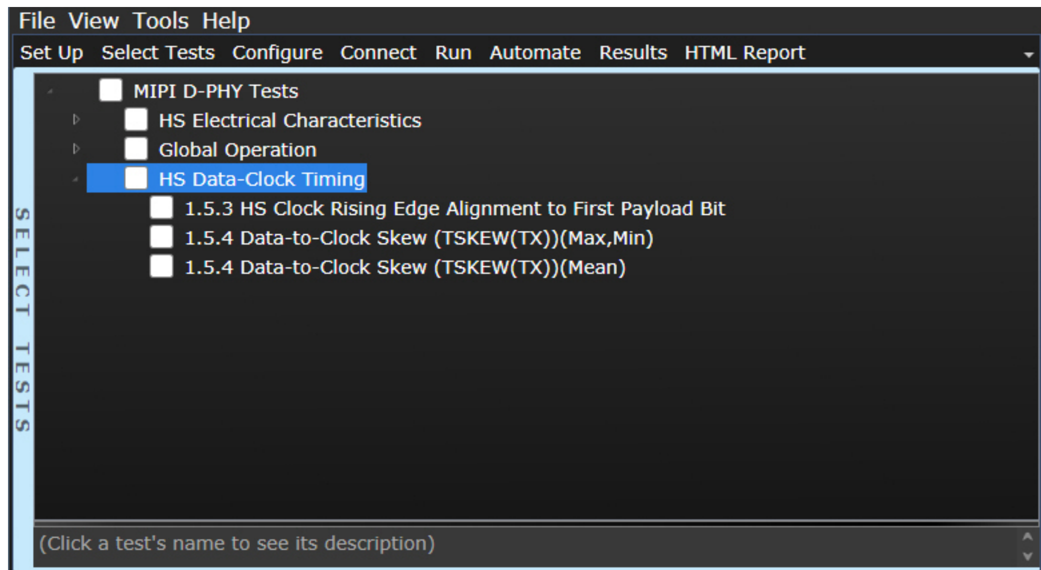

Figure 76 Selecting HS Data-Clock Timing Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation

For information about this test, refer to "Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation".

Test References

See Test 1.5.3 in CTS v1.1 and Section 10.2 in the D-PHY Specification v1.1.

Test 1.5.4 Data-to-Clock Skew ($T_{SKEW(TX)}$) Method of Implementation

For information about this test, refer to "Test 1.5.4 Data-to-Clock Skew ($T_{SKEW(TX)}$) Method of Implementation".

Test References

See Test 1.5.4 in CTS v1.1 and Section 10.2.1 Table 27 in the D-PHY Specification v1.1.

Part IV
Informative Tests

KEYSIGHT TECHNOLOGIES

19 MIPI D-PHY 1.1 Informative Tests

MIPI D-PHY 1.1 Informative tests are the same as MIPI D-PHY 1.0 Informative tests. Hence, they share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to “MIPI D-PHY 1.0 Informative Tests”.

Part C
MIPI D-PHY 1.2

KEYSIGHT
TECHNOLOGIES

Part I
Electrical Characteristics

KEYSIGHT
TECHNOLOGIES

20 MIPI D-PHY 1.2 High Speed Data Transmitter (HS Data TX) Electrical Tests

Probing for High Speed Data Transmitter Electrical Tests / 276
Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation / 278
Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($\Delta V_{CMTX(1,0)}$) Method of Implementation / 278
Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz (ΔV_{CMTX}(HF)) Method of Implementation / 278
Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz (ΔV_{CMTX}(LF)) Method of Implementation / 278
Test 1.3.4 HS Data TX Differential Voltage (V_{OD}) Method of Implementation / 278
Test 1.3.5 HS Data TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation / 279
Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation / 279
Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation / 280
Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation / 283
Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz (ΔV_{CMTX}(LF)) Method of Implementation / 286

This section provides the Methods of Implementation (MOIs) for the High Speed Data Transmitter (HS Data TX) Electrical tests using an Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 1.2 HS Data TX tests are similar to the MIPI D-PHY 1.0 HS Data TX tests. Hence, most of the tests share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.0 High Speed Data Transmitter (HS Data TX) Electrical Tests".

The current chapter lists the references from the MIPI D-PHY 1.2 CTS and describes the difference in the Method of Implementation from the corresponding MIPI D-PHY 1.0 test for the following tests:

"Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation"

"Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation"

Probing for High Speed Data Transmitter Electrical Tests

When performing the HS Data TX tests, the MIPI D-PHY Test Application may prompt you to make changes to the physical setup. The connections for the HS Data TX tests may look similar to the following diagrams. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

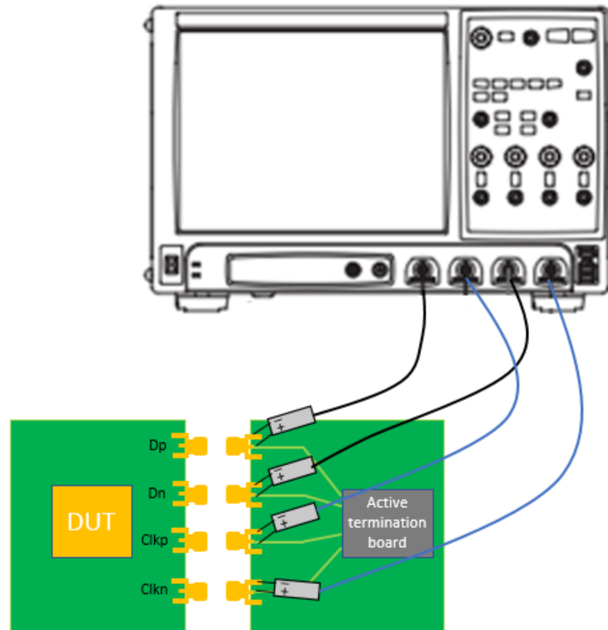

Figure 77 Probing for High Speed Data Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 77 are just for illustration).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, Device ID and User Comments.
4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

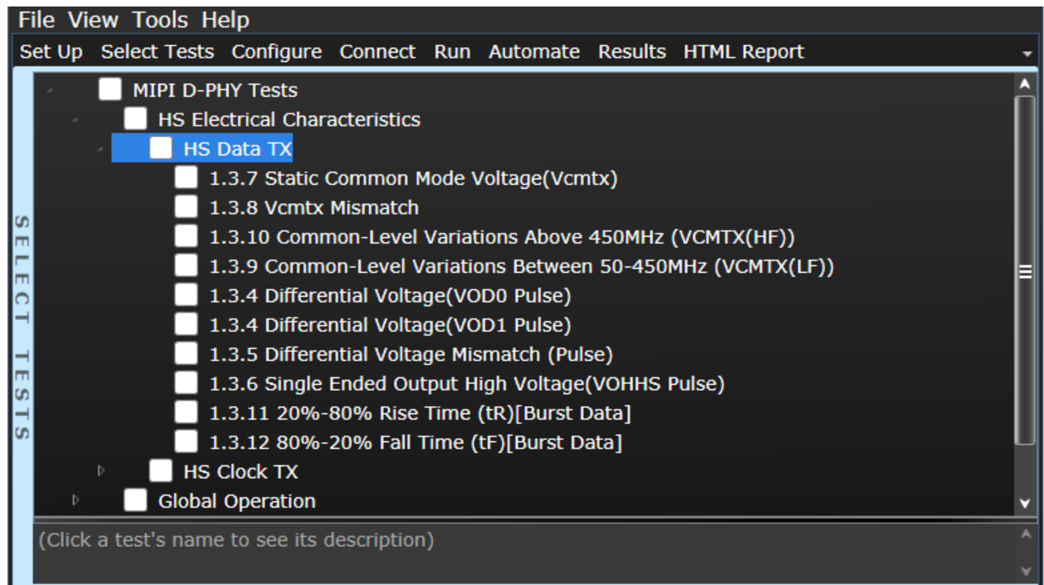

Figure 78 Selecting High Speed Data Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation

For information about this test, refer to "Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation".

Test References

See Test 1.3.7 in CTS v1.2 and Section 9.1.1 Table 19 in the D-PHY Specification v1.2.

Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($\Delta V_{CMTX(1,0)}$) Method of Implementation

For information about this test, refer to "Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($\Delta V_{CMTX}(1,0)$) Method of Implementation".

Test References

See Test 1.3.8 in CTS v1.2 and Section 9.1.1 Table 19 in the D-PHY Specification v1.2.

Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz ($\Delta V_{CMTX(HF)}$) Method of Implementation

For information about this test, refer to "Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz (ΔV_{CMTX}(HF)) Method of Implementation".

Test References

See Test 1.3.10 in CTS v1.2 and Section 9.1.1 Table 20 in the D-PHY Specification v1.2.

Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz ($\Delta V_{CMTX(LF)}$) Method of Implementation

For information about this test, refer to "Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz (ΔV_{CMTX}(LF)) Method of Implementation".

Test References

See Test 1.3.9 in CTS v1.2 and Section 9.1.1 Table 20 in the D-PHY Specification v1.2.

Test 1.3.4 HS Data TX Differential Voltage (V_{OD}) Method of Implementation

For information about this test, refer to "Test 1.3.4 HS Data TX Differential Voltage (V_{OD}) Method of Implementation".

Test References

See Test 1.3.4 in CTS v1.2 and Section 9.1.1 Table 19 in the D-PHY Specification v1.2.

Test 1.3.5 HS Data TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation

For information about this test, refer to "Test 1.3.5 HS Data TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation".

Test References

See Test 1.3.5 in CTS v1.2 and Section 9.1.1 Table 19 in the D-PHY Specification v1.2.

Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation

For information about this test, refer to "Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation".

Test References

See Test 1.3.6 in CTS v1.2r09 (29Sep2014) and Section 9.1.1 Table 19 in the D-PHY Specification v1.2.

Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation

The rise time, t_R is defined as the transition time between 20% and 80% of the full HS signal swing. The driver must meet the t_R specifications for all the allowable Z_{ID}.

PASS Condition

The measured t_R value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 65 Test Availability Condition for Test 1.3.11

Associated Test IDs		81101	81102	81104	81105
Conditions					
HS Data Rate		Not applicable	Not applicable	Not applicable	Not applicable
Continuous Data		Disabled	Enabled	Disabled	Enabled
Continuous Clock		Not applicable	Not applicable	Not applicable	Not applicable
Data LP EscapeMode		Not applicable	Not applicable	Not applicable	Not applicable
Clock LP EscapeMode		Not applicable	Not applicable	Not applicable	Not applicable
Clock ULPS Mode		Not applicable	Not applicable	Not applicable	Not applicable
Informative Test		Not applicable	Not applicable	Enabled	Enabled
Probing Methods	**Active Probe (Differential Probe)**	Available	Available	Available	Available
	Direct Connect (Active Termination Adapter)	Not available	Availability dependent on Continuous Clock and Continuous Data settings	Not available	Availability dependent on Continuous Clock and Continuous Data settings
	Direct Connect	Not available	Availability dependent on Continuous Clock and Continuous Data settings	Not available	Availability dependent on Continuous Clock and Continuous Data settings

Measurement Algorithm using Test ID 81101

NOTE Use the Test ID# 81101 to remotely access the test.

1 This test requires the following prerequisite tests:

   a HS Entry: Data TX $T_{HS\text{-}PREPARE} + T_{HS\text{-}ZERO}$ (Test ID: 558 for Test ID: 81101)

   Actual value for V_{HS_ZERO} is measured and test results are stored.

2 Trigger on SoT of HS Data burst (LP11->LP01).

3 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform using the following equation:

DataDiff = Dp-Dn

4 Define the measurement threshold as follows:

   Top Level: Inverse of V_{HS_ZERO}

   Base Level: V_{HS_ZERO}

5 Use a MATLAB script to identify and extract all the “000111” pattern locations found in the differential signal.
6 Measure the 20%-80% rise time at all the rising edges of the “000111” pattern that is identified.
7 Compare the measured t_R (Mean) value with the maximum conformance test limit.

Measurement Algorithm using Test ID 81102

NOTE Use the Test ID# 81102 to remotely access the test.

---

1 This test requires the following prerequisite tests:
   a HS Clock Instantaneous (UI_{inst})[Max] (Test ID: 911)
   UI value measurements for test signal are performed and test results are stored.
   b HS Data TX Differential Voltage (V_{OD}) (Test ID: 8131, 8132)
   Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
2 Trigger on SoT of HS Continuous Data.
3 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform using the following equation:

$$DataDiff = Dp-Dn$$

4 Define the measurement threshold as follows:

   Top Level: V_{OD1} (V_{OD} for Differential-1)

   Base Level: V_{OD0} (V_{OD} for Differential-0)

5 Use a MATLAB script to identify and extract all the “000111” pattern locations found in the differential signal.
6 Measure the 20%-80% rise time at all the rising edges of the “000111” pattern that is identified.
7 Compare the measured t_R (Mean) value with the maximum conformance test limit.

Measurement Algorithm using Test ID 81104

NOTE Use the Test ID# 81104 to remotely access the test.
This test is an informative test.

---

1 This test requires the following prerequisite test:
   a Data Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 81101)
   Rise time measurements are performed and t_R (Mean) test result is stored.
2 Compare the measured t_R (Mean) value with the minimum conformance test limits.

Measurement Algorithm using Test ID 81105

NOTE

Use the Test ID# 81105 to remotely access the test.

This test is an informative test.

1. This test requires the following prerequisite test:
   a. Data Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 81102)
      Rise time measurements are performed and t_R (Mean) test result is stored.
2. Compare the measured t_R (Mean) value with the minimum conformance test limits.

Test References

See Test 1.3.11 in CTS v1.2 and Section 9.1.1 Table 20 in the D-PHY Specification v1.2.

Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation

The fall time, t_F is defined as the transition time between 80% and 20% of the full HS signal swing. The driver must meet the t_F specifications for all the allowable Z_{ID}.

PASS Condition

The measured t_F value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 66 Test Availability Condition for Test 1.3.12

Associated Test IDs		81111	81112	81114	81115
Conditions					
HS Data Rate		Not applicable	Not applicable	Not applicable	Not applicable
Continuous Data		Disabled	Enabled	Disabled	Enabled
Continuous Clock		Not applicable	Not applicable	Not applicable	Not applicable
Data LP EscapeMode		Not applicable	Not applicable	Not applicable	Not applicable
Clock LP EscapeMode		Not applicable	Not applicable	Not applicable	Not applicable
Clock ULPS Mode		Not applicable	Not applicable	Not applicable	Not applicable
Informative Test		Not applicable	Not applicable	Enabled	Enabled
Probing Methods	**Active Probe (Differential Probe)**	Available	Available	Available	Available
	Direct Connect (Active Termination Adapter)	Not available	Availability dependent on Continuous Clock and Continuous Data settings	Not available	Availability dependent on Continuous Clock and Continuous Data settings
	Direct Connect	Not available	Availability dependent on Continuous Clock and Continuous Data settings	Not available	Availability dependent on Continuous Clock and Continuous Data settings

Measurement Algorithm using Test ID 81111

NOTE Use the Test ID# 81111 to remotely access the test.

1 This test requires the following prerequisite tests:

   a HS Entry: Data TX $T_{HS\text{-}PREPARE} + T_{HS\text{-}ZERO}$ (Test ID: 558 for Test ID: 81111)

   Actual value for V_{HS_ZERO} is measured and test results are stored.

2 Trigger on SoT of the HS Data burst (LP11->LP01).

3 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform using the following equation:

$$DataDiff = Dp\text{-}Dn$$

4 Define the measurement threshold as follows:

Top Level: Inverse of V_{HS_ZERO}

Base Level: V_{HS_ZERO}

5 Use a MATLAB script to identify and extract all the “111000” pattern locations found in the differential signal.

6 Measure the 80%-20% fall time at all the falling edges of the “111000” pattern that is identified.

7 Compare the measured value of t_F (Mean) with the maximum conformance test limit.

Measurement Algorithm using Test ID 81112

NOTE **Use the Test ID# 81112 to remotely access the test.**

---

1 This test requires the following prerequisite tests:

a HS Clock Instantaneous (UI_{inst})[Max] (Test ID: 911)
UI value measurements for test signal are performed and test results are stored.

b HS Data TX Differential Voltage (V_{OD}) (Test ID: 8131, 8132)
Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.

2 Trigger on SoT of HS Continuous Data.

3 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform using the following equation:

$$Data_{Diff} = Dp\text{-}Dn$$

4 Define the measurement threshold as follows:

Top Level: V_{OD1} (V_{OD} for Differential-1)

Base Level: V_{OD0} (V_{OD} for Differential-0)

5 Use a MATLAB script to identify and extract all the “111000” pattern locations found in the differential signal.

6 Measure the 80%-20% fall time at all the falling edges of the “111000” pattern that is identified.

7 Compare the measured t_F (Mean) value with the maximum conformance test limit.

Measurement Algorithm using Test ID 81114

NOTE **Use the Test ID# 81114 to remotely access the test.**
This test is an informative test.

---

1 This test requires the following prerequisite test:

a Data Lane HS-TX 80%-20% Fall Time (t_F) (Test ID: 81111)
Fall time measurements are performed and t_F (Mean) test result is stored.

2 Compare the measured t_F (Mean) value with the minimum conformance test limits.

Measurement Algorithm using Test ID 81115

NOTE

Use the Test ID# 81115 to remotely access the test.

This test is an informative test.

1 This test requires the following prerequisite test:

  a Data Lane HS-TX 80%-20% Fall Time (t_F) (Test ID: 81112)
  Fall time measurements are performed and t_F (Mean) test result is stored.

2 Compare the measured t_F (Mean) value with the minimum conformance test limits.

Test References

See Test 1.3.12 in CTS v1.2 and Section 9.1.1 Table 20 in the D-PHY Specification v1.2.

Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz ($\Delta V_{CMTX(LF)}$) Method of Implementation

For information about this test, refer to "Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz (ΔV_{CMTX}(LF)) Method of Implementation".

Test References

See Test 1.4.9 in CTS v1.2 and Section 9.1.1 Table 20 in the D-PHY Specification v1.2.

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Test 1.4.7 HS Clock TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation / 290
Test 1.4.8 HS Clock TX VCMTX Mismatch ($\Delta V_{CMTX}(_{1,0})$) Method of Implementation / 290
Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz (ΔV_{CMTX}(HF)) Method of Implementation / 290
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Test 1.4.17 HS Clock Instantaneous Method of Implementation / 299
Test 1.4.18 Clock Lane HS Clock Delta UI (UI variation) Method of Implementation / 300

This section provides the Methods of Implementation (MOIs) for the High Speed Clock Transmitter (HS Clock T_X) Electrical tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 1.2 HS Clock TX tests are similar to the MIPI D-PHY 1.0 HS Clock TX tests. Hence, they share the same Method of Implementation (MOI) as many of the corresponding MIPI D-PHY 1.0 tests. There is, however, an additional test that is supported by MIPI D-PHY 1.2 and not by MIPI D-PHY 1.0. Also, two tests have different methods of implementation from the corresponding MIPI D-PHY 1.0 tests. The current chapter describes these tests and lists the references from the MIPI D-PHY 1.2 CTS.

"Test 1.4.18 Clock Lane HS Clock Delta UI (UI variation) Method of Implementation" (Not in MIPI D-PHY 1.0).
"Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation" (Different from MIPI D-PHY 1.0).
"Test 1.4.12 Clock Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation" (Different from MIPI D-PHY 1.0).

For details of MIPI D-PHY 1.0 tests, refer to "MIPI D-PHY 1.0 High Speed Clock Transmitter (HS Clock TX) Electrical Tests".

KEYSIGHT TECHNOLOGIES

Probing for High Speed Clock Transmitter Electrical Tests

When performing the HS Clock T_X tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the HS Clock T_X tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

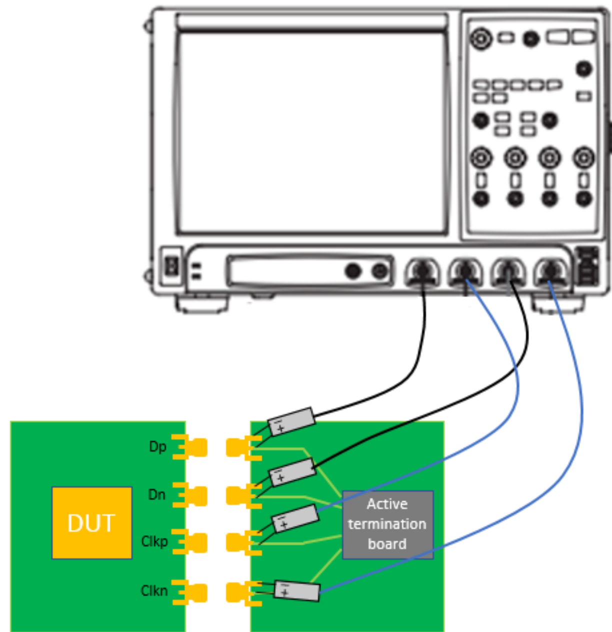

Figure 79 Probing for High Speed Clock Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 79 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

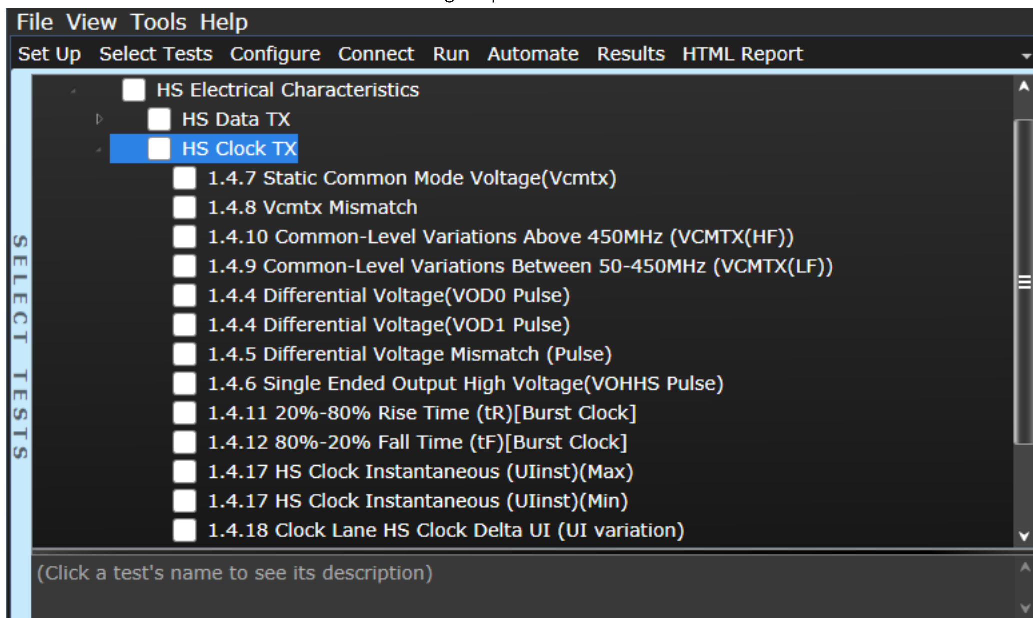

Figure 80 Selecting High Speed Clock Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.4.7 HS Clock TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation

For information about this test, refer to "Test 1.4.7 HS Clock TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation".

Test References

See Test 1.4.7 in CTS v1.2 and Section 9.1.1 Table 19 in the D-PHY Specification v1.2.

Test 1.4.8 HS Clock TX V_{CMTX} Mismatch ($\Delta V_{CMTX(1,0)}$) Method of Implementation

For information about this test, refer to "Test 1.4.8 HS Clock TX VCMTX Mismatch ($\Delta V_{CMTX}(1,0)$) Method of Implementation".

Test References

See Test 1.4.8 in CTS v1.2 and Section 9.1.1 Table 19 in the D-PHY Specification v1.2.

Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz ($\Delta V_{CMTX(HF)}$) Method of Implementation

For information about this test, refer to "Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz (ΔV_{CMTX}(HF)) Method of Implementation".

Test References

See Test 1.4.10 in CTS v1.2 and Section 9.1.1 Table 20 in the D-PHY Specification v1.2.

Test 1.4.4 HS Clock TX Differential Voltage (V_{OD}) Method of Implementation

For information about this test, refer to "Test 1.4.4 HS Clock TX Differential Voltage (V_{OD}) Method of Implementation".

Test References

See Test 1.4.4 in CTS v1.2 and Section 9.1.1 Table 19 in the D-PHY Specification v1.2.

Test 1.4.5 HS Clock TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation

For information about this test, refer to "Test 1.4.5 HS Clock TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation".

Test References

See Test 1.4.5 in CTS v1.2 and Section 9.1.1 Table 19 in the D-PHY Specification v1.2.

Test 1.4.6 HS Clock TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation

For information about this test, refer to "Test 1.4.6 HS Clock TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation".

Test References

See Test 1.4.6 in CTS v1.2 and Section 9.1.1 Table 19 in the D-PHY Specification v1.2.

Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation

The rise time, t_R is defined as the transition time between 20% and 80% of the full HS signal swing. The driver must meet the t_R specifications for all allowable Z_{ID}.

PASS Condition

The measured t_R value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 67 Test Availability Condition for Test 1.4.11

Associated Test IDs		181101	181102	181103	181104	181105	181106
Conditions							
HS Data Rate		Not applicable	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
Continuous Data		Not applicable	Disabled	Dependent on Continuous Clock setting	Not applicable	Disabled	Dependent on Continuous Clock setting
Continuous Clock		Disabled	Dependent on Continuous Data setting	Enabled	Disabled	Dependent on Continuous Data setting	Enabled
Data LP EscapeMode		Not applicable	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
Clock LP EscapeMode		Not applicable	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
Clock ULPS Mode		Not applicable	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
Informative Test		Not applicable	Not applicable	Not applicable	Enabled	Enabled	Enabled
Probing Methods	**Active Probe (Differential Probe)**	Available	Available	Available	Available	Available	Available
	Direct Connect (Active Termination Adapter)	Not Available	Not Available	Availability dependent on Continuous Clock setting	Not Available	Not Available	Availability dependent on Continuous Clock setting
	Direct Connect	Not Available	Not Available	Availability dependent on Continuous Clock setting	Not Available	Not Available	Availability dependent on Continuous Clock setting

Measurement Algorithm using Test ID 181101

NOTE Use the Test ID# 181101 to remotely access the test.

1 This test requires the following prerequisite tests:

a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)

Measure the UI value for the test signal and test results are stored.

b HS Entry: CLK TX $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ (Test ID: 554)

Measure the actual value of V_{HS_ZERO} and the test results are stored.

2 Trigger the oscilloscope to acquire Clkp and Clkn.

3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

Top Level: Inverse of V_{HS_ZERO}

Base Level: V_{HS_ZERO}

5 Use a MATLAB script to identify and extract all “01” pattern locations found in the differential signal.

6 Measure the 20%-80% rise time at all rising edges of the “01” pattern that is identified.

7 Compare the value of the measured t_R (Mean) with the maximum compliance test limit.

Measurement Algorithm using Test ID 181102

NOTE **Use the Test ID# 181102 to remotely access the test.**

1 This test requires the following prerequisite test:

a Data Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 81101)

Measure the actual value of V_{HS_ZERO} and the test results are stored.

2 Trigger the oscilloscope to acquire Clkp and Clkn.

3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

Top Level: Inverse of V_{HS_ZERO}

Base Level: V_{HS_ZERO}

5 Use a MATLAB script to identify and extract all “01” pattern locations found in the differential signal.

6 Measure the 20%-80% rise time at all rising edges of the “01” pattern that is identified.

7 Compare the value of the measured t_R (Mean) with the maximum compliance test limit.

Measurement Algorithm using Test ID 181103

NOTE **Use the Test ID# 181103 to remotely access the test.**

1 This test requires the following prerequisite tests:

a HS Clock Instantaneous (UI_{inst})[Max] (Test ID: 911)
UI value measurements for test signal are performed and test results are stored.

b HS Clock T_X Differential Voltage (V_{OD}) (Test ID: 18131, 18132)
Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.

2 Trigger the oscilloscope to acquire Clkp and Clkn.

3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

Top Level: V_{OD1} (V_{OD} for Differential-1)

Base Level: V_{OD0} (V_{OD} for Differential-0)

5 Use a MATLAB script to identify and extract all “01” pattern locations found in the differential signal.

6 Measure the 20%-80% rise time at all rising edges of the “01” pattern that is identified.

7 Compare the value of the measured t_R (Mean) with the maximum compliance test limit.

Measurement Algorithm using Test ID 181104

NOTE Use the Test ID# 181104 to remotely access the test.

This test is an informative test.

1 This test requires the following prerequisite test:
   a Clock Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 181101)
   Rise time measurements are performed and t_R (Mean) test result is stored.

2 Compare the value of the measured t_R (Mean) with the minimum compliance test limits.

Measurement Algorithm using Test ID 181105

NOTE Use the Test ID# 181105 to remotely access the test.

This test is an informative test.

1 This test requires the following prerequisite test:
   a Clock Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 181102)
   Rise time measurements are performed and t_R (Mean) test result is stored.

2 Compare the value of the measured t_R (Mean) with the minimum compliance test limits.

Measurement Algorithm using Test ID 181106

NOTE Use the Test ID# 181106 to remotely access the test.

This test is an informative test.

1 This test requires the following prerequisite test:
   a Clock Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 181103)
   Rise time measurements are performed and t_R (Mean) test result is stored.

2 Compare the value of the measured t_R (Mean) with the minimum compliance test limits.

Test References

See Test 1.4.11 in CTS v1.2 and Section 9.1.1 Table 20 in the D-PHY Specification v1.2.

Test 1.4.12 Clock Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation

The fall time, t_F is defined as the transition time between 80% and 20% of the full HS signal swing. The driver must meet the t_F specifications for all allowable Z_{ID}.

PASS Condition

The measured t_F value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 68 Test Availability Condition for Test 1.4.12

Associated Test IDs		181111	181112	181113	181114	181115	181116
Conditions							
HS Data Rate		Not applicable	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
Continuous Data		Not applicable	Disabled	Dependent on Continuous Clock setting	Not applicable	Disabled	Dependent on Continuous Clock setting
Continuous Clock		Disabled	Dependent on Continuous Data setting	Enabled	Disabled	Dependent on Continuous Data setting	Enabled
Data LP EscapeMode		Not applicable	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
Clock LP EscapeMode		Not applicable	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
Clock ULPS Mode		Not applicable	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
Informative Test		Not applicable	Not applicable	Not applicable	Enabled	Enabled	Enabled
Probing Methods	**Active Probe (Differential Probe)**	Available	Available	Available	Available	Available	Available
	Direct Connect (Active Termination Adapter)	Not Available	Not Available	Availability dependent on Continuous Clock setting	Not Available	Not Available	Availability dependent on Continuous Clock setting
	Direct Connect	Not Available	Not Available	Availability dependent on Continuous Clock setting	Not Available	Not Available	Availability dependent on Continuous Clock setting

Measurement Algorithm using Test ID 181111

NOTE Use the Test ID# 181111 to remotely access the test.

1 This test requires the following prerequisite tests:
   a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)
   Measure the minimum, maximum and average values of the Unit Interval for the differential clock waveform and the test results are stored.
   b HS Entry: CLK TX $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ (Test ID: 554)
   Measure the actual value of V_{HS_ZERO} and the test results are stored.
2 Trigger the oscilloscope to acquire Clkp and Clkn.
3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

Top Level: Inverse of V_{HS_ZERO}

Base Level: V_{HS_ZERO}

5 Use a MATLAB script to identify and extract all “10” pattern locations found in the differential signal.
6 Measure the 80%-20% fall time at all falling edges of the “10” pattern that is identified.
7 Compare the value of the measured t_F (Mean) with the maximum compliance test limit.

Measurement Algorithm using Test ID 181112

NOTE Use the Test ID# 181112 to remotely access the test.

1 This test requires the following prerequisite tests:
   a Data Lane HS-TX 80%-20% Fall Time (t_F) (Test ID: 81111)
   Measure the actual value of V_{HS_ZERO} and the test results are stored.
2 Trigger the oscilloscope to acquire Clkp and Clkn.
3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

Top Level: Inverse of V_{HS_ZERO}

Base Level: V_{HS_ZERO}

5 Use a MATLAB script to identify and extract all “10” pattern locations found in the differential signal.
6 Measure the 80%-20% fall time at all falling edges of the “10” pattern that is identified.
7 Compare the value of the measured t_F (Mean) with the maximum compliance test limit.

Measurement Algorithm using Test ID 181113

NOTE Use the Test ID# 181113 to remotely access the test.

1 This test requires the following prerequisite tests:
   a HS Clock Instantaneous (UI_{inst})[Max] (Test ID: 911)
   UI value measurements for test signal are performed and test results are stored.
   b HS Clock T_X Differential Voltage (V_{OD}) (Test ID: 18131, 18132)
   Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
2 Trigger the oscilloscope to acquire Clkp and Clkn.
3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

Top Level: V_{OD1} (V_{OD} for Differential-1)

Base Level: V_{OD0} (V_{OD} for Differential-0)

5 Use a MATLAB script to identify and extract all “10” pattern locations found in the differential signal.
6 Measure the 80%-20% fall time at all falling edges of the “10” pattern that is identified.
7 Compare the value of the measured t_F (Mean) with the maximum compliance test limits.

Measurement Algorithm using Test ID 181114

NOTE Use the Test ID# 181114 to remotely access the test.
This test is an informative test.

1 This test requires the following prerequisite test:
   a Clock Lane HS-TX 80%-20% Fall Time (t_F) (Test ID: 181111)
   Fall time measurements are performed and t_F (Mean) test result is stored.
2 Compare the value of the measured t_F (Mean) with the minimum compliance test limits.

Measurement Algorithm using Test ID 181115

NOTE Use the Test ID# 181115 to remotely access the test.
This test is an informative test.

1 This test requires the following prerequisite test:
   a Clock Lane HS-TX 80%-20% Fall Time (t_F) (Test ID: 181112)
   Fall time measurements are performed and t_F (Mean) test result is stored.
2 Compare the value of the measured t_F (Mean) with the minimum compliance test limits.

Measurement Algorithm using Test ID 181116

NOTE

Use the Test ID# 181116 to remotely access the test.

This test is an informative test.

1. This test requires the following prerequisite test:
   a. Clock Lane HS-TX 80%-20% Fall Time (t_F) (Test ID: 181113)
      Fall time measurements are performed and t_F (Mean) test result is stored.
2. Compare the value of the measured t_F (Mean) with the minimum compliance test limits.

Test References

See Test 1.4.12 in CTS v1.2 and Section 9.1.1 Table 20 in the D-PHY Specification v1.2.

Test 1.4.17 HS Clock Instantaneous Method of Implementation

For information about this test, refer to "Test 1.4.17 HS Clock Instantaneous Method of Implementation".

Test References

See Test 1.4.17 in CTS v1.2 and Section 10.1 Table 29 in the D-PHY Specification v1.2.

Test 1.4.18 Clock Lane HS Clock Delta UI (UI variation) Method of Implementation

Clock Lane HS Clock Delta UI (UI variation) verifies that the frequency stability of the DUT HS Clock during a signal burst is within the conformance limits.

PASS Condition

The measured UI variation must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 69 Test Availability Condition for Test 1.4.18

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1911	<=1.5Gbps	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)

Measurement Algorithm using Test ID 1911

NOTE Use the Test ID# 1911 to remotely access the test.

1 This test requires the following prerequisite test(s).

   a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)

   The minimum, maximum and average Unit Interval of the differential clock waveform is measured and stored.

2 Using MATLAB script, apply 1.98MHz (33 kHz * 60 = 1.98 MHz) 2nd-order Butterworth low pass test filter to the measurement trend data.

3 Calculate the UI_Variant_min and UI_Variant_max according to the following equation:

UI_Variant_min = ((UIinst_min - Uiinst_mean) / UIinst_mean) * 100%

UI_Variant_max = ((UIinst_max - Uiinst_mean) / UIinst_mean) * 100%

4 Determine the UI_variant_worst based on the UI_Variant_min and UI_Variant_max calculated above.

5 Compare the worst measured value of UI_variant_worst with the conformance limit.

Test References

See Test 1.4.18 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

22 MIPI D-PHY 1.2 Low Power Data Transmitter (LP Data TX) Electrical Tests

Probing for Low Power Transmitter Electrical Tests / 302
Test 1.1.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation / 304
Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation / 304
Test 1.1.3 LP TX 15%-85% Rise Time Level (T_{RLP}) EscapeMode Method of Implementation / 304
Test 1.1.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation / 304
Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock ($T_{LP-PULSE-TX}$) Method of Implementation / 305
Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock ($T_{LP-PER-TX}$) Method of Implementation / 308
Test 1.1.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation / 310

This section provides the Methods of Implementation (MOIs) for the Low Power Data Transmitter (LP Data TX) Electrical tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 1.2 LP Data TX Electrical tests are similar to the MIPI D-PHY 1.1 LP Data TX Electrical tests. Hence, most of the tests share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.1 Low Power Data Transmitter (LP Data TX) Electrical Tests".

The current chapter lists the references from the MIPI D-PHY 1.2 CTS and describes the difference in the Method of Implementation from the corresponding MIPI D-PHY 1.1 test for the following tests:

"Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock ($T_{LP-PULSE-TX}$) Method of Implementation"

"Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock ($T_{LP-PER-TX}$) Method of Implementation"

"Test 1.1.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation"

KEYSIGHT TECHNOLOGIES

Probing for Low Power Transmitter Electrical Tests

When performing the LP TX tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the LP TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test Application for the exact number of probe connections.

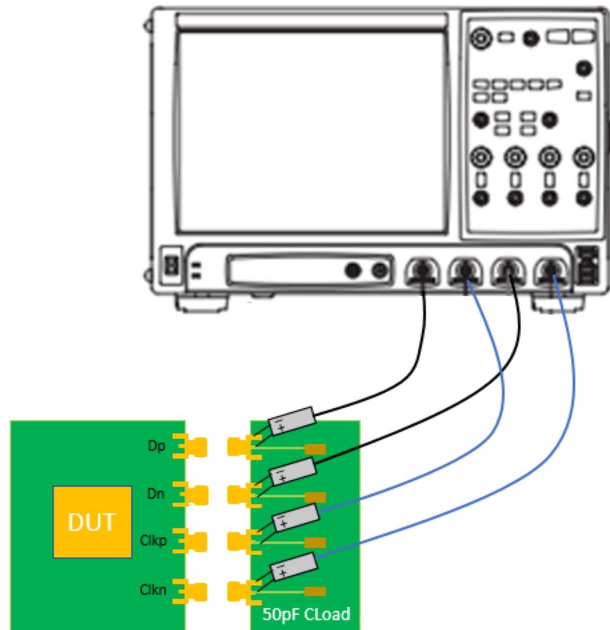

Figure 81 Probing for Low Power Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 81 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, Device ID and User Comments.
4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

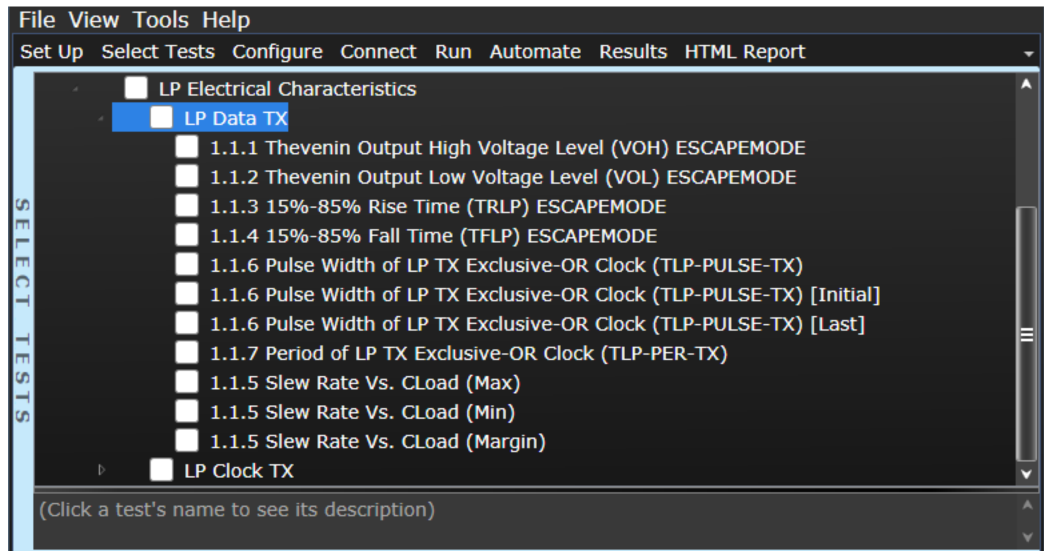

Figure 82 Selecting Low Power Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app’s task flow to set up the configuration options, run the tests and view the tests results.

Test 1.1.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation

For information about this test, refer to "Test 1.1.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation".

Test References

See Test 1.1.1 in CTS v1.2 and Section 9.1.2 Table 21 in the D-PHY Specification v1.2.

Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation

For information about this test, refer to "Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation".

Test References

See Test 1.1.2 in CTS v1.2 and Section 9.1.2 Table 21 in the D-PHY Specification v1.2.

Test 1.1.3 LP TX 15%-85% Rise Time Level (T_{RLP}) EscapeMode Method of Implementation

For information about this test, refer to "Test 1.1.3 LP TX 15%-85% Rise Time Level (T_{RLP}) EscapeMode Method of Implementation".

Test References

See Test 1.1.3 in CTS v1.2 and Section 9.1.2 Table 22 in the D-PHY Specification v1.2.

Test 1.1.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation

For information about this test, refer to "Test 1.1.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation".

Test References

See Test 1.1.4 in CTS v1.2 and Section 9.1.2 Table 22 in the D-PHY Specification v1.2.

Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock ($T_{LP\text{-}PULSE\text{-}TX}$) Method of Implementation

$T_{LP\text{-}PULSE\text{-}TX}$ is defined as the pulse width of the DUT Low-Power TX XOR clock. A graphical representation of the XOR operation that creates the LP clock is shown below. The D-PHY Standard actually separates the $T_{LP\text{-}PULSE\text{-}TX}$ specification into two parts:

a The first LP XOR clock pulse after a Stop state, or the last LP XOR clock pulse before a Stop state must be wider than 40ns.

b All other LP XOR clock pulses must be wider than 20ns.

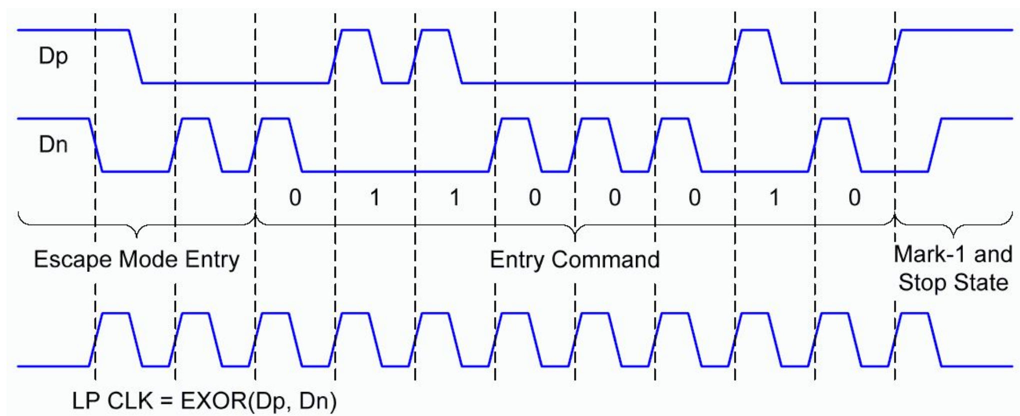

Figure 83 Graphical Representation of the XOR Operation

PASS Condition

The measured $T_{LP\text{-}PULSE\text{-}TX}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 70 Test Availability Condition for Test 1.1.6

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
827	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)
8271	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	
8272	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Enabled	

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1827	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	
18271	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	
18272	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Enabled	

Measurement Algorithm using Test IDs 827, 8271 and 8272

LP TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP\text{-}PULSE\text{-}TX}$)

NOTE Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 827 to remotely access the test.

LP TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP\text{-}PULSE\text{-}TX}$) [Initial]

NOTE Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8271 to remotely access the test.

LP TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP\text{-}PULSE\text{-}TX}$) [Last]

NOTE Select **Data LP EscapeMode** and **Informative Test** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8272 to remotely access the test.

1 This test requires the following prerequisite tests:

   a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211).

   This is to trigger and capture an EscapeMode sequence data from the test signal.

2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.

3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data.

4 Find all crossing points at the minimum trip level (500mV) and the maximum trip level (930mV for data rates that are less than or equal to 1.5 Gbps or 790mV for data rates greater than 1.5 Gbps) for Dp and Dn individually.

5 Find the initial pulse width, last pulse width and minimum width of all the other pulses at the specified minimum trip level and maximum trip level.

6 Find the rising-to-rising and falling-to-falling periods of the XOR clock at the mentioned minimum trip level and maximum trip level.

7 The worst case value for the pulse width found between the minimum trip level and maximum trip level will be used as the $T_{LP\text{-}PULSE\text{-}TX}$ value.

8 Compare the measured minimum $T_{LP\text{-}PULSE\text{-}TX}$ value with the compliance test limits.

Measurement Algorithm using Test IDs 1827, 18271 and 18272

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP\text{-}PULSE\text{-}TX}$)

NOTE Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 1827 to remotely access the test.

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP\text{-}PULSE\text{-}TX}$) [Initial]

NOTE Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 18271 to remotely access the test.

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP\text{-}PULSE\text{-}TX}$) [Last]

NOTE Select **Clock LP EscapeMode** and **Informative Test** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 18272 to remotely access the test.

1 This test requires the following prerequisite tests:
   a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
   This is to trigger and capture an EscapeMode sequence data from the test signal.
2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data.
4 Find all crossing points at the minimum trip level (500mV) and the maximum trip level (930mV for data rates that are less than or equal to 1.5 Gbps or 790mV for data rates greater than 1.5 Gbps) for Clkp and Clkn individually.
5 Find the initial pulse width, last pulse width and minimum width of all the other pulses at the specified minimum trip level and maximum trip level.
6 Find the rising-to-rising and falling-to-falling periods of the XOR clock at the specified minimum trip level and maximum trip level.
7 The worst case value for the pulse width found between the minimum trip level and maximum trip level is used as the $T_{LP\text{-}PULSE\text{-}TX}$ value.
8 Compare the measured minimum $T_{LP\text{-}PULSE\text{-}TX}$ value with the compliance test limits.

Test References

See Test 1.1.6 in CTS v1.2 and Section 9.1.2 Table 22 in the D-PHY Specification v1.2.

Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock ($T_{LP\text{-}PER\text{-}TX}$) Method of Implementation

$T_{LP\text{-}PER\text{-}TX}$ is defined as the period of the DUT Low-Power TX XOR clock. A graphical representation of the XOR operation that creates the LP clock is shown below. The D-PHY Standard separates the $T_{LP\text{-}PULSE\text{-}TX}$ specification into two parts:

a The first LP XOR clock pulse after a Stop state, or the last LP XOR clock pulse before a Stop state must be wider than 40ns.

b All other LP XOR clock pulses must be wider than 20ns.

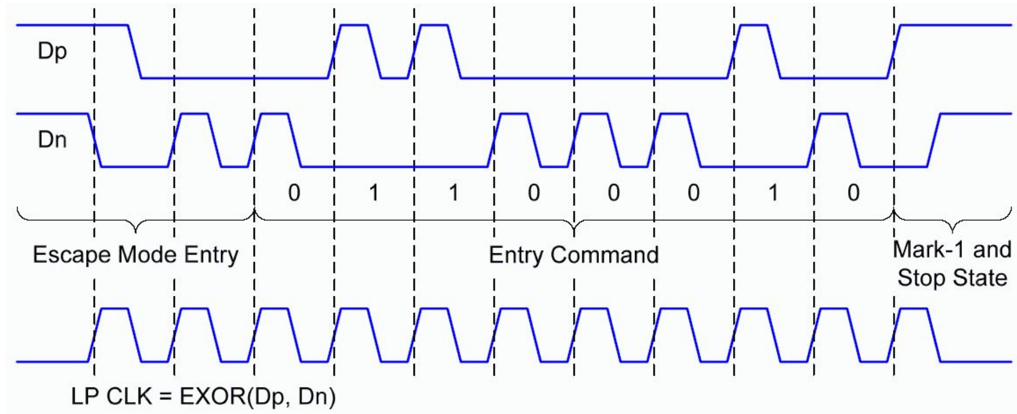

Figure 84 Graphical Representation of the XOR Operation

PASS Condition

The measured $T_{LP\text{-}PER\text{-}TX}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 71 Test Availability Condition for Test 1.1.7

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
828	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)
1828	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	

Measurement Algorithm using Test ID 828

LP TX Period of LP TX Exclusive-OR Clock ($T_{LP-PER-TX}$)

NOTE Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 828 to remotely access the test.

1. This test requires the following prerequisite test(s).
   a. LP TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP-PULSE-TX}$) (Test ID: 827)

   The actual measurement algorithm of the $T_{LP-PER-TX}$ is performed in the mentioned prerequisite test.
2. The minimum value for all the rising-to-rising and falling-to-falling periods of the XOR clock at the minimum trip level (500mV) and the maximum trip level (930mV for data rates that are less than or equal to 1.5 Gbps or 790mV for data rates greater than 1.5 Gbps) is used as the $T_{LP-PER-TX}$ result.
3. Compare the measured minimum $T_{LP-PER-TX}$ value to the compliance test limits.

Measurement Algorithm using Test ID 1828

LP Clock TX Period of LP TX Exclusive-OR Clock ($T_{LP-PER-TX}$)

NOTE Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 1828 to remotely access the test.

1. This test requires the following prerequisite test(s).
   a. LP Clock TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP-PULSE-TX}$) (Test ID: 1827)

   The actual measurement algorithm of the $T_{LP-PER-TX}$ is performed in the mentioned prerequisite test.
2. The minimum value for all the rising-to-rising and falling-to-falling periods of the XOR clock at the minimum trip level (500mV) and the maximum trip level (930mV for data rates that are less than or equal to 1.5 Gbps or 790mV for data rates greater than 1.5 Gbps) is used as the $T_{LP-PER-TX}$ result.
3. Compare the measured minimum $T_{LP-PER-TX}$ value with the compliance test limits.

Test References

See Test 1.1.7 in CTS v1.2 and Section 9.1.2 Table 22 in the D-PHY Specification v1.2.

Test 1.1.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation

The slew rate $\delta V/\delta t_{SR}$ is the derivative of the LP transmitter output signal voltage over time. The intention of specifying a maximum slew rate value in the specification is to limit EMI (Electro Magnetic Interference).

The specification also states that the Slew Rate must be measured as an average across any 50mV segment of the output signal transition.

PASS Condition

The measured slew rate $\delta V/\delta t_{SR}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 72 Test Availability Condition for Test 1.1.5

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
829	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)
8291	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	
8292	Not Applicable	Disabled	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	

Measurement Algorithm using Test IDs 829, 8291 and 8292

NOTE

Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test.

- To access the LP TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 829.
- To access the LP TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 8291.
- To access the LP TX Slew Rate Vs. C_{Load} (Margin) test remotely, use the Test ID# 8292.

1 This test requires the following prerequisite tests:

   a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)

   b LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 8221)

   V_{OH} and V_{OL} values for low power signal measurements are performed and test results are stored.

2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.

3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to performing the actual slew rate measurement.

4 Perform the slew rate measurement on the filtered EscapeMode sequence for both Dp and Dn waveforms individually.
   For falling edge,
   a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
   b. Perform the slew rate measurement across the 400mV - 930mV region for data rate <= 1.5 Gbps OR 400mV - 790mV region for data rate > 1.5 Gbps to determine the minimum slew rate

result.
For rising edge,
a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
b. Perform the slew rate measurement across the 400mV - 700mV region for data rate <= 1.5 Gbps OR 400mV - 550mV region for data rate > 1.5 Gbps to determine the minimum slew rate result.
c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700mV - 930mV region for data rate <= 1.5 Gbps OR 550mV-790mV region for data rate > 1.5 Gbps.

5. Calculate the average value from all rising edges' maximum slew rate results. Calculate the average value from all falling edges' maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.
6. Calculate the average value from all rising edges' minimum slew rate results. Calculate the average value from all falling edges' minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
7. Calculate the average value from all rising edges' slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
8. The Slew Rate maximum, minimum and margin result values are stored.
9. Report the measurement results.
10. Compare the measured slew rate results with the conformance test limits.

Test References

See Test 1.1.5 in CTS v1.2 and Section 9.1.2 Table 22 in the D-PHY Specification v1.2.

23 MIPI D-PHY 1.2 Low Power Clock Transmitter (LP Clock TX) Electrical Tests

Probing for Low Power Transmitter Electrical Tests / 314
Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation / 316
Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation / 316
Test 1.2.3 LP TX 15%-85% Rise Time Level (T_{RLP}) Method of Implementation / 316
Test 1.2.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation / 316
Test 1.2.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation / 317

This section provides the Methods of Implementation (MOIs) for the Low Power Clock Transmitter (LP Clock TX) Electrical tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 1.2 HS Data TX tests are similar to the MIPI D-PHY 1.1 LP Clock TX Electrical tests. Hence, most of the tests share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.1 tests. For details, refer to "MIPI D-PHY 1.1 Low Power Clock Transmitter (LP Clock TX) Electrical Tests".

The current chapter lists the references from the MIPI D-PHY 1.2 CTS and describes the difference in the Method of Implementation from the corresponding MIPI D-PHY 1.1 test for the following test:

"Test 1.2.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation"

KEYSIGHT TECHNOLOGIES

Probing for Low Power Transmitter Electrical Tests

When performing the LP TX tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the LP TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test Application for the exact number of probe connections.

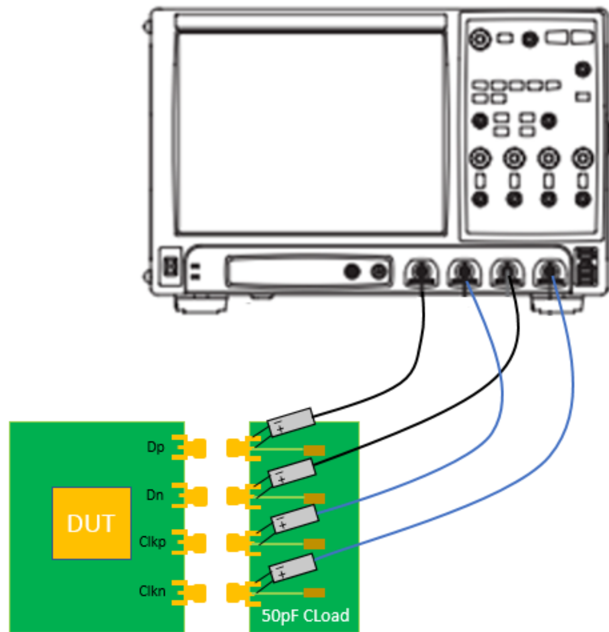

Figure 85 Probing for Low Power Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 85 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

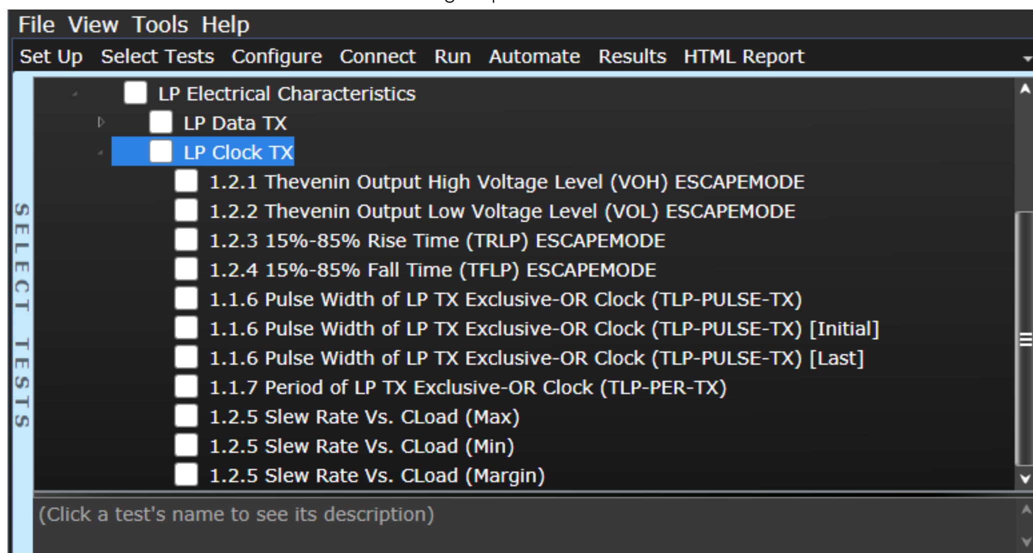

Figure 86 Selecting Low Power Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation

For information about this test, refer to "Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation".

Test References

See Test 1.2.1 in CTS v1.2 and Section 9.1.2 Table 21 in the D-PHY Specification v1.2.

Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation

For information about this test, refer to "Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation".

Test References

See Test 1.2.2 in CTS v1.2 and Section 9.1.2 Table 21 in the D-PHY Specification v1.2.

Test 1.2.3 LP TX 15%-85% Rise Time Level (T_{RLP}) Method of Implementation

For information about this test, refer to "Test 1.2.3 LP TX 15%-85% Rise Time Level (T_{RLP}) Method of Implementation".

Test References

See Test 1.2.3 in CTS v1.2 and Section 9.1.2 Table 22 in the D-PHY Specification v1.2.

Test 1.2.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation

For information about this test, refer to "Test 1.2.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation".

Test References

See Test 1.2.4 in CTS v1.2 and Section 9.1.2 Table 22 in the D-PHY Specification v1.2.

Test 1.2.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation

The slew rate $\delta V/ \delta t_{SR}$ is the derivative of the LP transmitter output signal voltage over time. The intention of specifying a maximum slew rate value in the specification is to limit EMI (Electro Magnetic Interference).

The specification also states that the Slew Rate must be measured as an average across any 50mV segment of the output signal transition.

PASS Condition

The measured slew rate $\delta V/ \delta t_{SR}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 73 Test Availability Condition for Test 1.2.5

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1829	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	Active Probe (Differential Probe)
18291	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	
18292	Not Applicable	Not Applicable	Disabled	Not Applicable	Enabled	Disabled	Not Applicable	
2829	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Enabled	Not Applicable	
28291	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Enabled	Not Applicable	
28292	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Enabled	Not Applicable	

Measurement Algorithm using Test ID 1829, 18291 and 18292

LP Clock TX Slew Rate Vs. C_{Load} (Max) /

LP Clock TX Slew Rate Vs. C_{Load} (Min) /

LP Clock TX Slew Rate Vs. C_{Load} (Margin)

NOTE

Select **Clock LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test.

- To access the LP Clk TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 1829.
- To access the LP Clk TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 18291.
- To access the LP Clk TX Slew Rate Vs. C_{Load} (Margin) test remotely, use the Test ID# 18292.

1 This test requires the following prerequisite tests:
   a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
   b LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 18221)

   V_{OH} and V_{OL} values for low power signal measurements are performed and test results are stored.
2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to performing the actual slew rate measurement.
4 Perform the slew rate measurement on the filtered EscapeMode sequence for both Clkp and Clkn waveforms individually.
   For falling edge,
   a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
   b. Perform the slew rate measurement across the 400mV - 930mV region for data rate <= 1.5 Gbps or 400mV - 790mV region for data rate > 1.5 Gbps to determine the minimum slew rate result.
   For rising edge,
   a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
   b. Perform the slew rate measurement across the 400mV - 700mV region for data rate <= 1.5 Gbps or 400mV-550mV region for data rate > 1.5 Gbps to determine the minimum slew rate result.
   c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700mV - 930mV region for data rate <= 1.5 Gbps or 550mV - 790mV region for data rate > 1.5 Gbps.
5 Calculate the average value from all rising edges’ maximum slew rate results. Calculate the average value from all falling edges’ maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.
6 Calculate the average value from all rising edges’ minimum slew rate results. Calculate the average value from all falling edges’ minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
7 Calculate the average value from all rising edges’ slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
8 The Slew Rate maximum, minimum and margin result values are stored.

9 Report the measurement results.

10 Compare the measured worst slew rate value for Clkp and Clkn to the compliance test limits.

ULPS Clock TX Slew Rate Vs. C_{Load} (Max) ULPSMODE/

ULPS Clock TX Slew Rate Vs. C_{Load} (Min) ULPSMODE/

ULPS Clock TX Slew Rate Vs. C_{Load} (Margin) ULPSMODE

Measurement Algorithm using Test ID 2829, 28291 and 28292

NOTE

Select **Clock ULPS Mode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test.

- To access the ULPS Clk TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 2829.
- To access the ULPS Clk TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 28291.
- To access the ULPS Clk TX Slew Rate Vs. C_{Load} (Margin) test remotely, use the Test ID# 28292.

1 This test requires the following prerequisite tests:

   a ULPS Clock TX Thevenin Output High Voltage Level (V_{OH}) ULPSMODE (Test ID: 28211)

   b ULPS Clock TX Thevenin Output Low Voltage Level (V_{OL}) ULPSMODE (Test ID: 28221)

   V_{OH} and V_{OL} values for low power signal measurements are performed and test results are stored.

2 The oscilloscope is triggered to capture rising and falling edges to be processed based on the “Number of ULPS Slew Edge” configuration in the **Configure** tab.

3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired waveform data prior to performing the actual slew rate measurement.

4 Perform the slew rate measurement on the mentioned triggered data for both Clkp and Clkn waveforms individually.
   For falling edge,
   a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
   b. Perform the slew rate measurement across the 400mV - 930mV region for data rate <= 1.5 Gbps or 400mV - 790mV region for data rate > 1.5 Gbps to determine the minimum slew rate result.
   For rising edge,
   a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
   b. Perform the slew rate measurement across the 400mV - 700mV region for data rate <= 1.5 Gbps or 400mV-550mV region for data rate > 1.5 Gbps to determine the minimum slew rate result.
   c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700mV - 930mV region for data rate <= 1.5 Gbps or 550mV - 790mV region for data rate > 1.5 Gbps.

5 Calculate the average value from all rising edges’ maximum slew rate results. Calculate the average value from all falling edges’ maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.

6. Calculate the average value from all rising edges' minimum slew rate results. Calculate the average value from all falling edges' minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
7. Calculate the average value from all rising edges' slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
8. The Slew Rate maximum, minimum and margin result values are stored.
9. Report the measurement results.
10. Compare the measured worst slew rate value for Clkp and Clkn to the compliance test limits.

Test References

See Test 1.2.5 in CTS v1.2 and Section 9.1.2 Table 22 in the D-PHY Specification v1.2.

Part II
Global Operation

KEYSIGHT
TECHNOLOGIES

24 MIPI D-PHY 1.2 Data Transmitter (Data TX) Global Operation Tests

Probing for Data TX Global Operation Tests / 324
Test 1.3.1 HS Entry: Data T_{LPX} Method of Implementation / 326
Test 1.3.2 HS Entry: Data TX $T_{HS-PREPARE}$ Method of Implementation / 326
Test 1.3.3 HS Entry: Data TX $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ Method of Implementation / 326
Test 1.3.13 HS Exit: Data TX $T_{HS-TRAIL}$ Method of Implementation / 326
Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{REOT}) Method of Implementation / 326
Test 1.3.15 HS Exit: Data TX T_{EOT} Method of Implementation / 328
Test 1.3.16 HS Exit: Data TX $T_{HS-EXIT}$ Method of Implementation / 328

This section provides the Methods of Implementation (MOIs) for the Data Transmitter (Data TX) Global Operation tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 1.2 Data TX Global Operation tests are similar to the MIPI D-PHY 1.0 Data TX Global Operation tests. Hence, most of the tests share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.0 Data Transmitter (Data TX) Global Operation Tests".

The current chapter lists the references from the MIPI D-PHY 1.2 CTS and describes the difference in the Method of Implementation from the corresponding MIPI D-PHY 1.0 test for the following test:

"Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{REOT}) Method of Implementation".

"Test 1.3.15 HS Exit: Data TX T_{EOT} Method of Implementation".

KEYSIGHT TECHNOLOGIES

Probing for Data TX Global Operation Tests

When performing the Data TX tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the Data TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test Application for the exact number of probe connections.

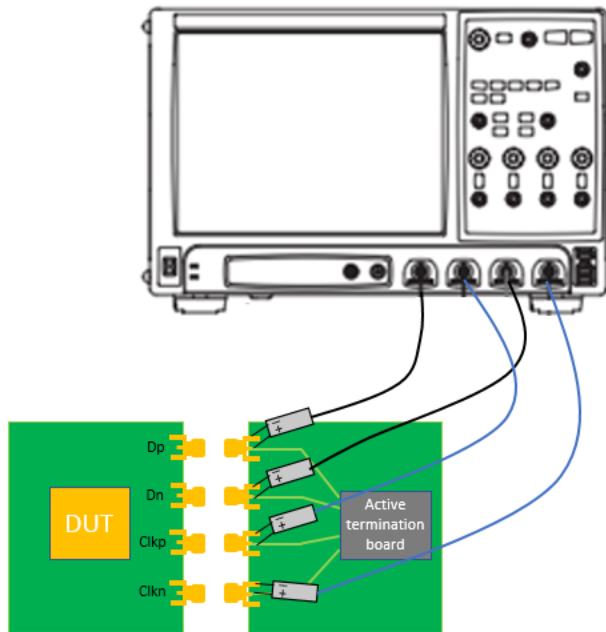

Figure 87 Probing for Data TX Global Operation Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 87 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

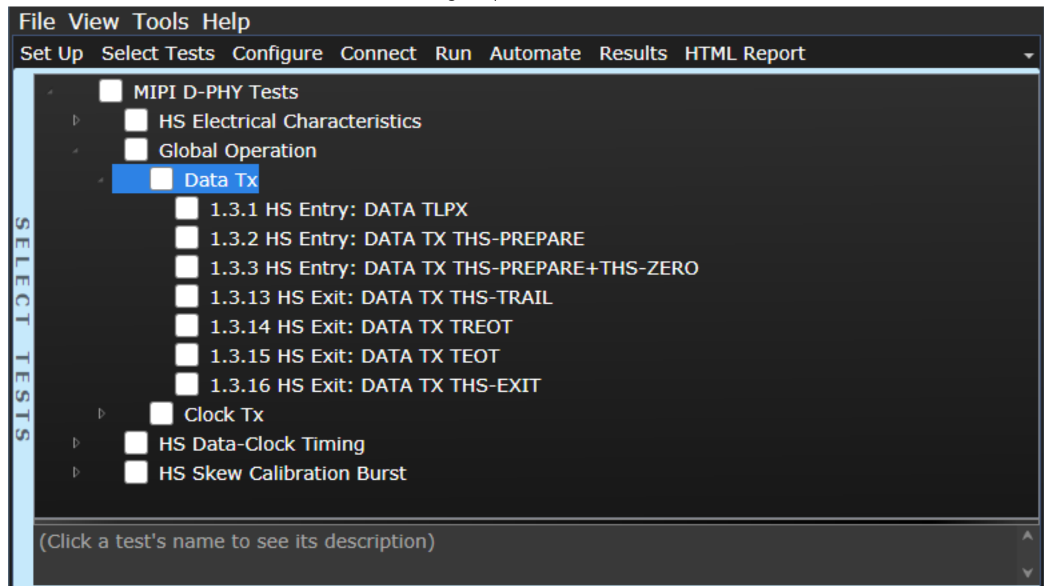

Figure 88 Selecting Data TX Global Operation Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.3.1 HS Entry: Data T_{LPX} Method of Implementation

For information about this test, refer to "Test 1.3.1 HS Entry: Data T_{LPX} Method of Implementation".

Test References

See Test 1.3.1 in CTS v1.2 and Section 6.9 Table 14 in the D-PHY Specification v1.2.

Test 1.3.2 HS Entry: Data TX $T_{HS-PREPARE}$ Method of Implementation

For information about this test, refer to "Test 1.3.2 HS Entry: Data TX $T_{HS-PREPARE}$ Method of Implementation".

Test References

See Test 1.3.2 in CTS v1.2 and Section 6.9 Table 14 in the D-PHY Specification v1.2.

Test 1.3.3 HS Entry: Data TX $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ Method of Implementation

For information about this test, refer to "Test 1.3.3 HS Entry: Data TX $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ Method of Implementation".

Test References

See Test 1.3.3 in CTS v1.2 and Section 6.9 Table 14 in the D-PHY Specification v1.2.

Test 1.3.13 HS Exit: Data TX $T_{HS-TRAIL}$ Method of Implementation

For information about this test, refer to "Test 1.3.13 HS Exit: Data TX $T_{HS-TRAIL}$ Method of Implementation".

Test References

See Test 1.3.13 in CTS v1.2 and Section 6.9 Table 14 in the D-PHY Specification v1.2.

Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{REOT}) Method of Implementation

This test is similar to the corresponding MIPI D-PHY 1.0 test. This section describes only the changes from the MIPI D-PHY 1.0 test. For details of the corresponding MIPI D-PHY 1.0 test, refer to "Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{REOT}) Method of Implementation".

Measurement Algorithm using Test ID 549

NOTE **Use the Test ID# 549 to remotely access the test.**

1 Trigger on Dp's falling edge in LP-01 at the SoT.
2 Go to EoT.
3 Find the time where the last data TX differential edge crosses +/-V_{IDTH}(max), denoted as T1.
4 Find the time where Dp rising edge crosses V_{IH}(min) (880mV for data rate <= 1.5 Gbps OR 740mV for data rate > 1.5 Gbps), and denote it as T2. Note that T2 must be greater than T1.

5 Use the following calculation:

$$T_{REOT} = T2\text{-}T1$$

6 Report the measured T_{REOT}.

7 Compare the measured T_{REOT} with the conformance test limits.

Test References

See Test 1.3.14 in CTS v1.2 and Section 9.1.2 Table 22 in the D-PHY Specification v1.2.

Test 1.3.15 HS Exit: Data TX T_{EOT} Method of Implementation

This test is similar to the corresponding MIPI D-PHY 1.0 test. This section describes only the changes from the MIPI D-PHY 1.0 test. For details of the corresponding MIPI D-PHY 1.0 test, refer to "Test 1.3.15 HS Exit: Data TX T_{EOT} Method of Implementation".

Measurement Algorithm using Test ID 547

NOTE Use the Test ID# 547 to remotely access the test.

1. This test requires the following prerequisite tests:
   - HS Clock Instantaneous: UI_{inst} [Max] (Test ID: 911)
   - The minimum, maximum and average Unit Interval of the differential clock waveform is measured and test results are stored.
2. Trigger on Dp's falling edge in LP-01 at the SoT.
3. Go to EoT.
4. Find the time when the last data differential edge crosses +/-V_{IDTH}(max), and denote it as T6.
5. Find the time where Dp rising edge crosses VIH(min)(880mV for data rate <= 1.5 Gbps OR 740mV for data rate > 1.5 Gbps), and denote it as T8. Note that T8 must greater than T6.
6. Use the following calculation:

$$T_{EOT} = T8-T6$$

7. Report the measured T_{EOT}.
8. Compare the measured T_{EOT} with the conformance test limits.

Test References

See Test 1.3.15 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.3.16 HS Exit: Data TX $T_{HS-EXIT}$ Method of Implementation

For information about this test, refer to "Test 1.3.16 HS Exit: Data TX $T_{HS-EXIT}$ Method of Implementation".

Test References

See Test 1.3.16 in CTS v1.2 and Section 6.9 Table 14 in the D-PHY Specification v1.2.

25 MIPI D-PHY 1.2 Clock Transmitter (Clock TX) Global Operation Tests

Probing for Clock TX Global Operation Tests / 330
Test 1.4.1 HS Entry: CLK TX T_{LPX} Method of Implementation / 332
Test 1.4.2 HS Entry: CLK TX $T_{CLK-PREPARE}$ Method of Implementation / 332
Test 1.4.3 HS Entry: CLK TX $T_{CLK-PREPARE}+T_{CLK-ZERO}$ Method of Implementation / 332
Test 1.5.1 HS Entry: CLK TX $T_{CLK-PRE}$ Method of Implementation / 332
Test 1.5.2 HS Exit: CLK TX $T_{CLK-POST}$ Method of Implementation / 332
Test 1.4.13 HS Exit: CLK TX $T_{CLK-TRAIL}$ Method of Implementation / 332
Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{REOT}) Method of Implementation / 333
Test 1.4.15 HS Exit: CLK TX T_{EOT} Method of Implementation / 333
Test 1.4.16 HS Exit: CLK TX $T_{HS-EXIT}$ Method of Implementation / 334

This section provides the Methods of Implementation (MOIs) for the Clock Transmitter (Clock TX) Global Operation tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 1.2 Clock TX Global Operation tests are similar to the MIPI D-PHY 1.0 Clock TX Global Operation tests. Hence, most of the tests share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.0 Clock Transmitter (Clock TX) Global Operation Tests".

The current chapter lists the references from the MIPI D-PHY 1.2 CTS and describes the difference in the Method of Implementation from the corresponding MIPI D-PHY 1.0 test for the following test:

"Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{REOT}) Method of Implementation".

"Test 1.4.15 HS Exit: CLK TX T_{EOT} Method of Implementation".

KEYSIGHT TECHNOLOGIES

Probing for Clock TX Global Operation Tests

When performing the Clock TX tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the Clock TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test Application for the exact number of probe connections.

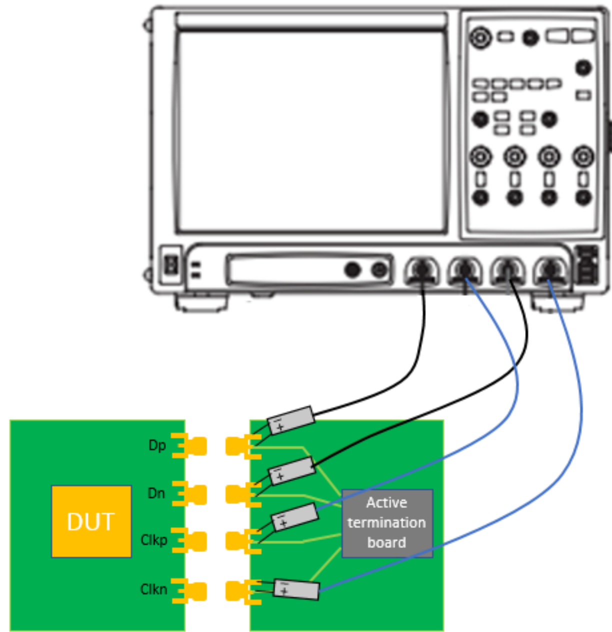

Figure 89 Probing for Clock TX Global Operation Tests

You can identify the channels used for each signal in the Configuration tab of the MIPI D-PHY Test Application. (The channels shown in Figure 89 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, Device ID and User Comments.
4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

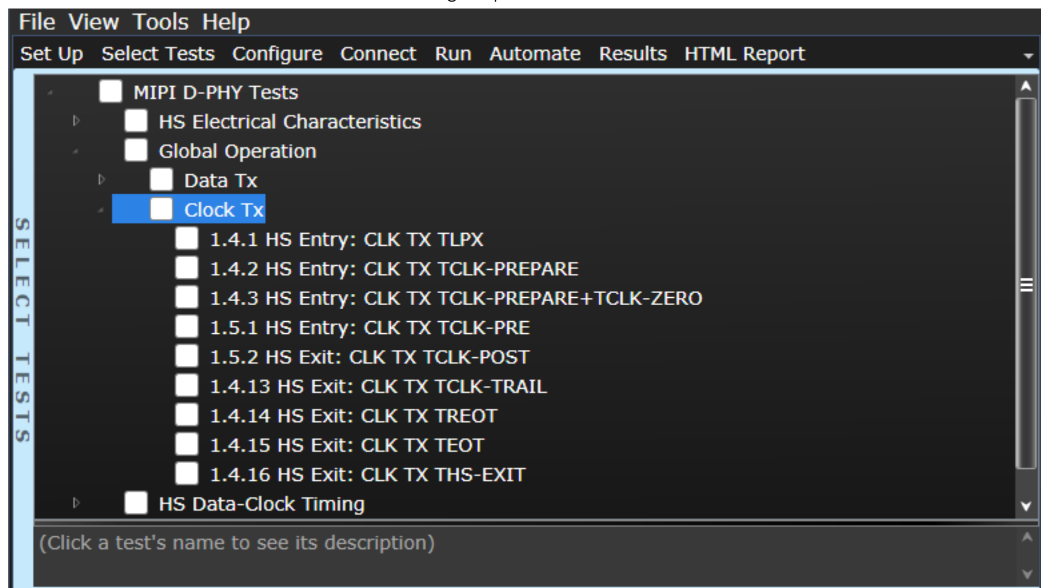

Figure 90 Selecting Clock TX Global Operation Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.4.1 HS Entry: CLK TX T_{LPX} Method of Implementation

For information about this test, refer to "Test 1.4.1 HS Entry: CLK TX T_{LPX} Method of Implementation".

Test References

See Test 1.4.1 in CTS v1.2 and Section 6.9 Table 14 in the D-PHY Specification v1.2.

Test 1.4.2 HS Entry: CLK TX $T_{CLK-PREPARE}$ Method of Implementation

For information about this test, refer to "Test 1.4.2 HS Entry: CLK TX $T_{CLK-PREPARE}$ Method of Implementation".

Test References

See Test 1.4.2 in CTS v1.2 and Section 6.9 Table 14 in the D-PHY Specification v1.2.

Test 1.4.3 HS Entry: CLK TX $T_{CLK-PREPARE}$+$T_{CLK-ZERO}$ Method of Implementation

For information about this test, refer to "Test 1.4.3 HS Entry: CLK TX $T_{CLK-PREPARE}$+$T_{CLK-ZERO}$ Method of Implementation".

Test References

See Test 1.4.3 in CTS v1.2 and Section 6.9 Table 14 in the D-PHY Specification v1.2.

Test 1.5.1 HS Entry: CLK TX $T_{CLK-PRE}$ Method of Implementation

For information about this test, refer to "Test 1.5.1 HS Entry: CLK TX $T_{CLK-PRE}$ Method of Implementation".

Test References

See Test 1.5.1 in CTS v1.2 and Section 6.9 Table 14 in the D-PHY Specification v1.2.

Test 1.5.2 HS Exit: CLK TX $T_{CLK-POST}$ Method of Implementation

For information about this test, refer to "Test 1.5.2 HS Exit: CLK TX $T_{CLK-POST}$ Method of Implementation".

Test References

See Test 1.5.2 in CTS v1.2 and Section 6.9 Table 14 in the D-PHY Specification v1.2.

Test 1.4.13 HS Exit: CLK TX $T_{CLK-TRAIL}$ Method of Implementation

For information about this test, refer to "Test 1.4.13 HS Exit: CLK TX $T_{CLK-TRAIL}$ Method of Implementation".

Test References

See Test 1.4.13 in CTS v1.2 and Section 6.9 Table 14 in the D-PHY Specification v1.2.

Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{REOT}) Method of Implementation

This test is similar to the corresponding MIPI D-PHY 1.0 test. This section describes only the changes from the MIPI D-PHY 1.0 test. For details of the corresponding MIPI D-PHY 1.0 test, refer to "Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{REOT}) Method of Implementation".

Measurement Algorithm using Test ID 559

NOTE **Use the Test ID# 559 to remotely access the test.**

1 Trigger on the Clkn's falling edge in LP-01 at the SoT.
2 Go to EoT.
3 Find the time where last Clock TX differential edge crosses +/-VIDTH(max), marked as T1.
4 Find the time where Clkp rising edge crosses VIH(min) (880mV for data rate <= 1.5 Gbps or 740mV for data rate > 1.5 Gbps), marked as T2. Note that T2 must be greater than T1.
5 Use the equation:

$$T_{REOT} = T2-T1$$

6 Report the measured T_{REOT}.
7 Compare the measured T_{REOT}value to the compliance test limits.

Test References

See Test 1.4.14 in CTS v1.2 and Section 9.1.2 Table 22 in the D-PHY Specification v1.2.

Test 1.4.15 HS Exit: CLK TX T_{EOT} Method of Implementation

This test is similar to the corresponding MIPI D-PHY 1.0 test. This section describes only the changes from the MIPI D-PHY 1.0 test. For details of the corresponding MIPI D-PHY 1.0 test, refer to "Test 1.4.15 HS Exit: CLK TX T_{EOT} Method of Implementation".

Measurement Algorithm using Test ID 544

NOTE **Use the Test ID# 544 to remotely access the test.**

1 This test requires the following prerequisite tests:
   a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)
   Measure the minimum, maximum and average values of the Unit Interval for the differential clock waveform and the test results are stored.
2 Trigger on the Clkn's falling edge after LP-01.
3 Back trace to the previous EoT.
4 Construct the differential clock waveform by using the following equation:

$$DiffClock = Clkp-Clkn$$

5 Find the time when the DiffClock crosses +/-V_{IDTH}(max) after last payload clock bit. Denote the time as T1.

6 Find the time when the Clkp TX rising edge crosses V_{IH}(min)(880mV for data rate <= 1.5 Gbps OR 740mV for data rate > 1.5 Gbps). Denote the time as T2. Note that T2 must be greater than T1.
7 Calculate T_{EOT} using the following equation:

$$T_{EOT} = T2-T1$$

8 Report the T_{EOT} measurement.
9 Compare the measured T_{EOT} value with the conformance test limit.

Test References

See Test 1.4.15 in CTS v1.2 and Section 6.9 Table 14 in the D-PHY Specification v1.2.

Test 1.4.16 HS Exit: CLK TX $T_{HS-EXIT}$ Method of Implementation

For information about this test, refer to "Test 1.4.16 HS Exit: CLK TX $T_{HS-EXIT}$ Method of Implementation".

Test References

See Test 1.4.16 in CTS v1.2 and Section 6.9 Table 14 in the D-PHY Specification v1.2.

Part III HS Data-Clock Timing & HS Skew Calibration Burst

KEYSIGHT TECHNOLOGIES

26 MIPI D-PHY 1.2 High Speed (HS) Data-Clock Timing Tests

Probing for High Speed Data-Clock Timing Tests / 338
Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation / 340
Test 1.5.4 Data-to-Clock Skew ($T_{SKEW(TX)}$) Method of Implementation / 340

This section provides the Methods of Implementation (MOIs) for the High Speed (HS) Data-Clock Timing tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

Probing for High Speed Data-Clock Timing Tests

When performing the HS Data-Clock Timing tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the HS Data-Clock Timing tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

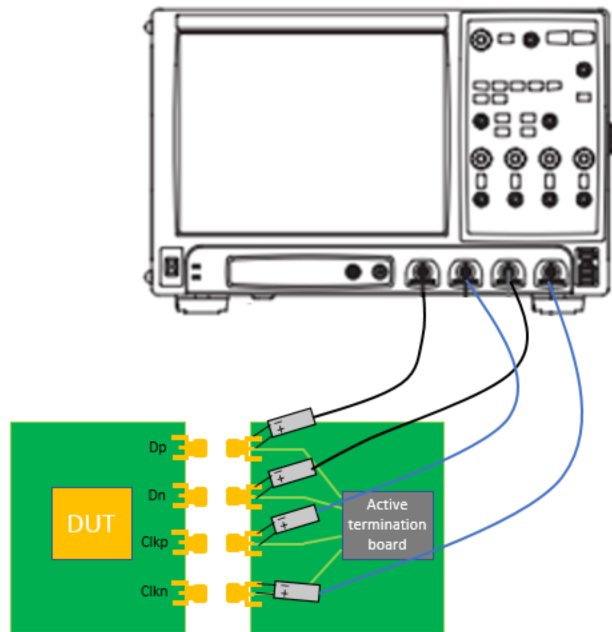

Figure 91 Probing for HS Data-Clock Timing Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 91 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

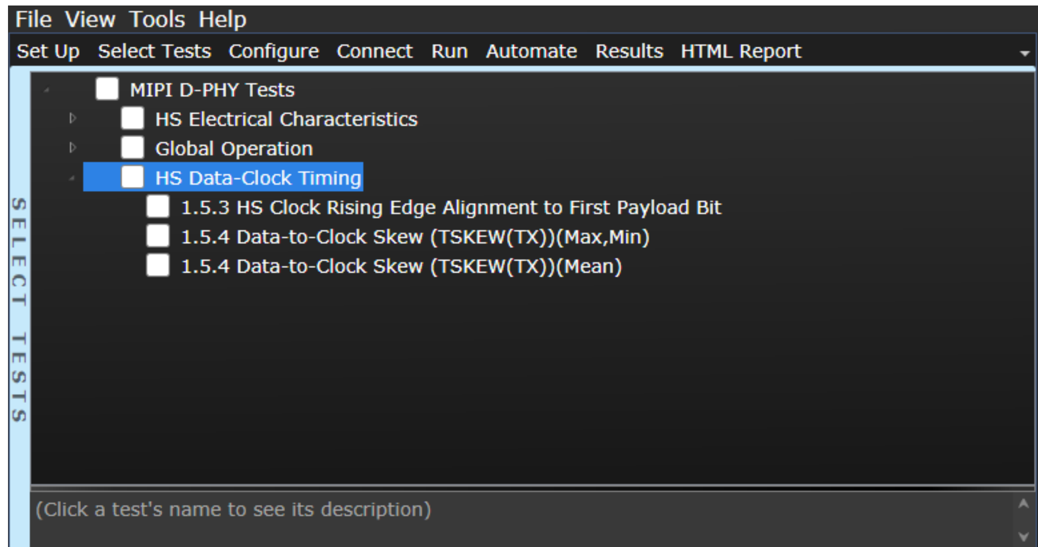

Figure 92 Selecting HS Data-Clock Timing Tests

5 Follow the MIPI D-PHY Test app’s task flow to set up the configuration options, run the tests and view the tests results.

Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation

This test has the same method of implementation as the corresponding MIPI D-PHY 1.0 test. For details, refer to "Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation".

Test References

See Test 1.5.3 in CTS v1.2 and Section 10.2 in the D-PHY Specification v1.2.

Test 1.5.4 Data-to-Clock Skew ($T_{SKEW(TX)}$) Method of Implementation

This test is similar to the corresponding MIPI D-PHY 1.0 test. This section describes only the changes from the MIPI D-PHY 1.0 test. For details of the corresponding MIPI D-PHY 1.0 test, refer to "Test 1.5.4 Data-to-Clock Skew ($T_{SKEW(TX)}$) Method of Implementation".

Measurement Algorithm using Test ID 913

NOTE Use the Test ID# 913 to remotely access the test.

1 This test requires the following prerequisite tests:

   a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)

   Measure the minimum, maximum and average values of the Unit Interval for the differential clock waveform and the test results are stored.

2 Dp, Dn, Clkp and Clkn waveforms are captured.

3 Construct the differential clock waveform using the following equation:

   DiffClock = Clkp-Clkn

4 Construct the differential data waveform by using the following equation:

   DiffData = Dp-Dn

5 Using the DiffClock's rising and falling edges, fold the DiffData to form a data eye.

6 Use the **Histogram** feature to find out the furthest edges on the left of the DiffData left crossing and use it to calculate the T_{Skew} (max).

7 Use the **Histogram** feature to find out the nearest edges on the left of the DiffData left crossing and use it to calculate the T_{Skew} (min).

8 Use the **Histogram** feature to find out the mean of the DiffData left crossing and use it to calculate the T_{Skew} (mean).

9 Calculate T_{Skew} values (max/min) in units of seconds and in units of UI using the following equation:

$$T_{Skew(TX)} \text{ (in seconds)} = (T_{Skew} - T_{Center}) - \text{MeanSkewRef}$$

$$T_{Skew(TX)} \text{ (in UI)} = T_{Skew}/\text{MeanUI}$$

NOTE

For HS rates <= 1.5 Gbps, the MeanSkewRef is calculated as:

MeanSkewRef = [0.5 * MeanUI obtained from the prerequisite test]

For HS rates > 1.5 Gbps, the MeanSkewRef is calculated as:

MeanSkewRef = [Measured T_{Skew} (mean) – T_{Center}]

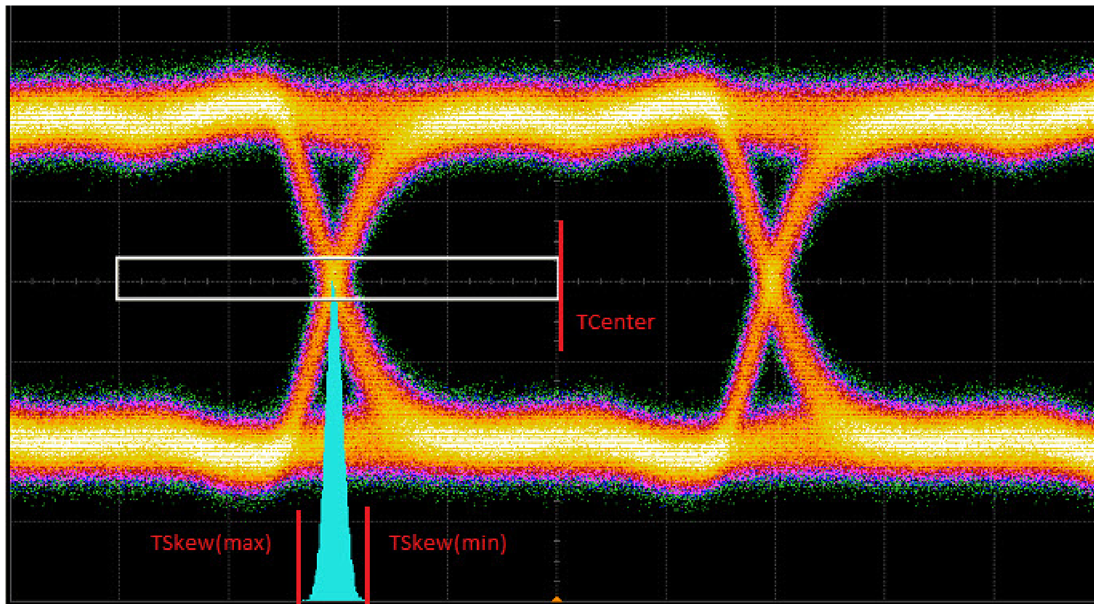

Figure 93 Data Eye

10 Calculate T_{Skew} (mean) in units of UI using the following equation:

$$T_{Skew(TX)} \text{ (in UI)} = T_{Skew}/\text{MeanUI}$$

11 The T_{Skew} (worst) is determined based on the T_{Skew} (max) and T_{Skew} (min) values with reference to the compliance test limit.

12 Compare the T_{Skew} (worst) value with the conformance test limits.

Test References

See Test 1.5.4 in CTS v1.2 and Section 10.2.1 Table 30 in the D-PHY Specification v1.2.

27 MIPI D-PHY 1.2 High Speed (HS) Skew Calibration Burst Tests

Probing for High Speed Skew Calibration Burst Tests / 344
Test 1.5.5 Initial HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL) Method of Implementation / 346
Test 1.5.6 Periodic HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL) Method of Implementation / 348

This section provides the Methods of Implementation (MOIs) for the High Speed (HS) Skew Calibration Burst tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

KEYSIGHT TECHNOLOGIES

Probing for High Speed Skew Calibration Burst Tests

When performing the HS Skew Calibration Burst tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the HS Skew Calibration Burst tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

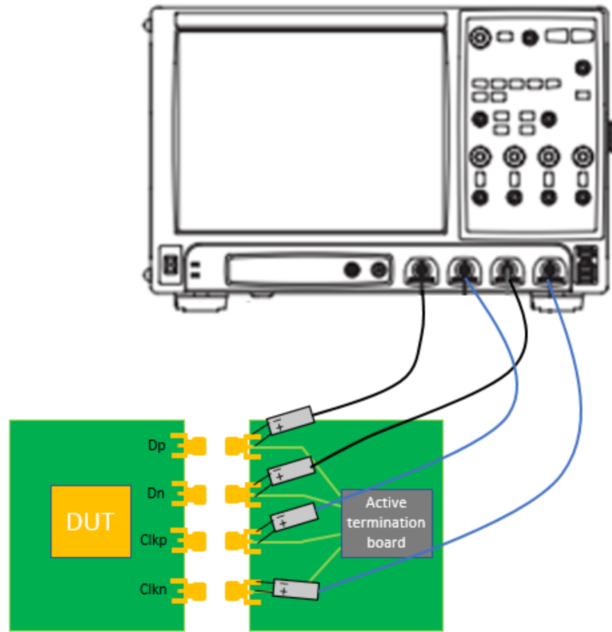

Figure 94 Probing for HS Skew Calibration Burst Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 94 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

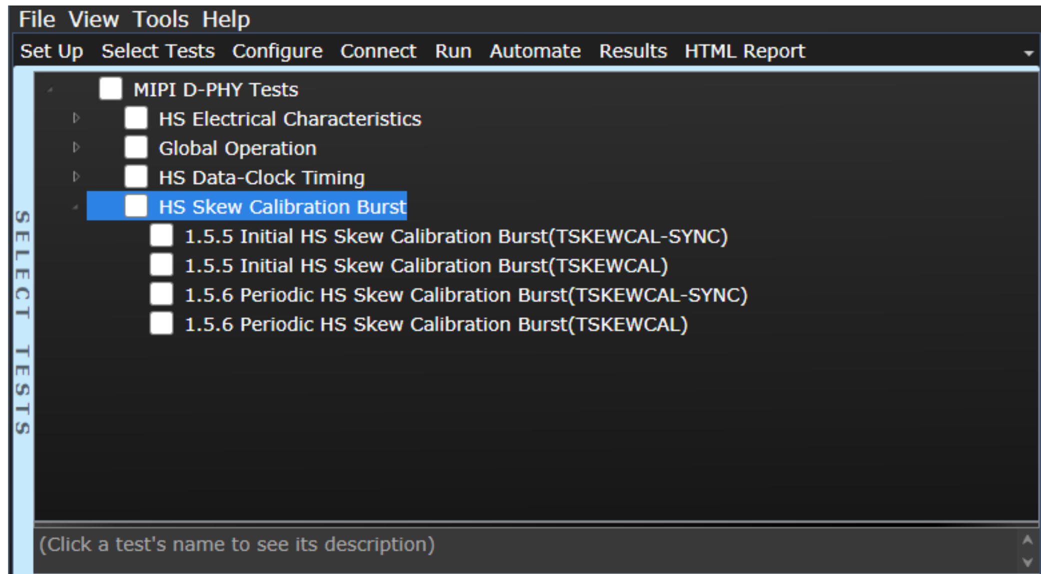

Figure 95 Selecting HS Skew Calibration Burst Tests

5 Follow the MIPI D-PHY Test app’s task flow to set up the configuration options, run the tests and view the tests results.

Test 1.5.5 Initial HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL) Method of Implementation

This test verifies that TSKEWCAL-SYNC and TSKEWCAL are within the specification.

6

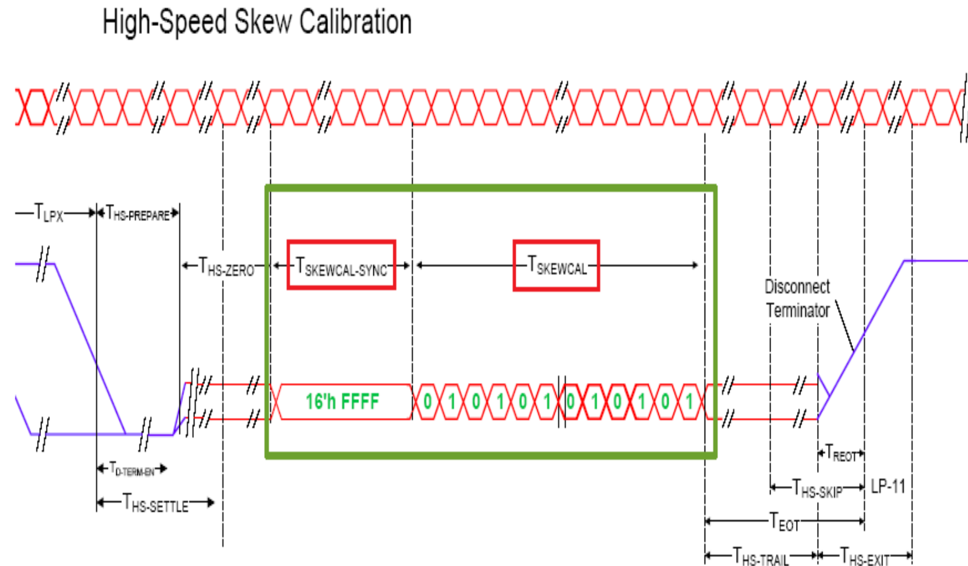

Figure 96 Normal Mode versus Skew Calibration

PASS Condition

The TSKEWCAL-SYNC and TSKEWCAL values must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 74 Test Availability Condition for Test 1.5.5

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
917	>1.5 Gbps	100 ohm	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)
918	> 1.5 Gbps	100 ohm	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	

Measurement Algorithm using Test ID 917

NOTE Use the Test ID# 917 to remotely access the test.

1 Trigger on Dp's falling edge in LP-01 on Initial HS Skew calibration burst.
2 Construct the differential waveform of Dp and Dn by using the following equation:

$$Data_{Diff} = Dp - Dn$$

3 Measure the average Unit Interval value of the differential data waveform.
4 Find the first rising edge of the differential waveform that crosses 0V after the LP-00 state. Mark the time as T_1.
5 Find and mark the next falling edge that crosses 0V. Mark the time as T_2.
6 Calculate TSKEWCAL-SYNC using the following equation:

TSKEWCAL-SYNC = T_2-T_1

7 From the T_2 position, find the final edge position where the bit pattern "01010101..." ends. Mark the position as T_3.
8 Calculate TSKEWCAL using the following equation:

TSKEWCAL = T_3-T_2

9 Report the measurement result:

TSKEWCAL-SYNC

10 Compare the TSKEWCAL-SYNC value with the compliance test limits.

Measurement Algorithm using Test ID 918

NOTE Use the Test ID# 918 to remotely access the test.

1 This test requires the following prerequisite test:
   a Initial HS Skew Calibration Burst (TSKEWCAL-SYNC) (Test ID: 917)
   Actual TSKEWCAL value is measured and test result is stored.
2 Report the measurement result:

TSKEWCAL

3 Compare the TSKEWCAL value with the compliance test limit.

Test References

See Test 1.5.5 in CTS v1.2 and Section 6.1.2 Table 18 in the D-PHY Specification v1.2.

Test 1.5.6 Periodic HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL) Method of Implementation

This test verifies that TSKEWCAL-SYNC and TSKEWCAL are within the specification.

PASS Condition

The TSKEWCAL-SYNC and TSKEWCAL values must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 75 Test Availability Condition for Test 1.5.6

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
919	> 1.5 Gbps	100 ohm	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe)
920	> 1.5 Gbps	100 ohm	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Not Applicable	

Measurement Algorithm using Test ID 919

NOTE Use the Test ID# 919 to remotely access the test.

1 Trigger on Dp's falling edge in LP-01 on Periodic HS Skew calibration burst.

2 Construct the differential waveform of Dp and Dn by using the following equation:

$$Data_{Diff} = Dp - Dn$$

3 Measure the average Unit Interval value of the differential data waveform.

4 Find the first rising edge of the differential waveform that crosses 0V after the LP-00 state. Mark the time as T_1.

5 Find and mark the next falling edge that crosses 0V. Mark the time as T_2.

6 Calculate TSKEWCAL-SYNC using the following equation:

TSKEWCAL-SYNC = T_2-T_1

7 From the T_2 position, find the final edge position where the bit pattern "01010101..." ends. Mark the position as T_3.

8 Calculate TSKEWCAL using the following equation:

TSKEWCAL = T_3-T_2

9 Report the measurement result:

TSKEWCAL-SYNC

10 Compare the TSKEWCAL-SYNC value with the compliance test limits.

Measurement Algorithm using Test ID 920

NOTE Use the Test ID# 920 to remotely access the test.

1 This test requires the following prerequisite test:
   a Periodic HS Skew Calibration Burst (TSKEWCAL-SYNC) (Test ID: 919)
   Actual TSKEWCAL value is measured and test result is stored.
2 Report the measurement result:

   TSKEWCAL
3 Compare the TSKEWCAL value with the compliance test limit.

Test References

See Test 1.5.6 in CTS v1.2 and Section 6.1.2 Table 18 in the D-PHY Specification v1.2.

Part IV
Informative Tests

KEYSIGHT
TECHNOLOGIES

28 MIPI D-PHY 1.2 Informative Tests

MIPI D-PHY 1.2 Informative tests are the same as MIPI D-PHY 1.0 Informative tests. Hence, they share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.0 Informative Tests".

KEYSIGHT TECHNOLOGIES

Part D
MIPI D-PHY 2.0 & 2.1

KEYSIGHT
TECHNOLOGIES

Part I
Electrical Characteristics

KEYSIGHT
TECHNOLOGIES

29 MIPI D-PHY 2.0 & 2.1 High Speed Data Transmitter (HS Data TX) Electrical Tests

Probing for High Speed Data Transmitter Electrical Tests / 360
Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation / 362
Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($\Delta V_{CMTX}(_{1,0})$) Method of Implementation / 362
Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz (ΔV_{CMTX}(HF)) Method of Implementation / 362
Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz (ΔV_{CMTX}(LF)) Method of Implementation / 362
Test 1.3.4 HS Data TX Differential Voltage (V_{OD} Pulse) Method of Implementation / 363
Test 1.3.5 HS Data TX Differential Voltage Mismatch (Pulse) (ΔV_{OD}) Method of Implementation / 366
Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation / 369
Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation / 370
Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation / 373
Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz (ΔV_{CMTX}(LF)) Method of Implementation / 376

This section provides the Methods of Implementation (MOIs) for the High Speed Data Transmitter (HS Data TX) Electrical tests using an Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 2.0 and 2.1 HS Data TX tests are similar to the MIPI D-PHY 1.2 HS Data TX tests. Hence, all the tests share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.2 tests. For details, refer to "MIPI D-PHY 1.2 High Speed Data Transmitter (HS Data TX) Electrical Tests".

The current chapter lists the references from the MIPI D-PHY 2.0 specification.

KEYSIGHT TECHNOLOGIES

Probing for High Speed Data Transmitter Electrical Tests

When performing the HS Data TX tests, the MIPI D-PHY Test Application may prompt you to make changes to the physical setup. The connections for the HS Data TX tests may look similar to the following diagrams. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

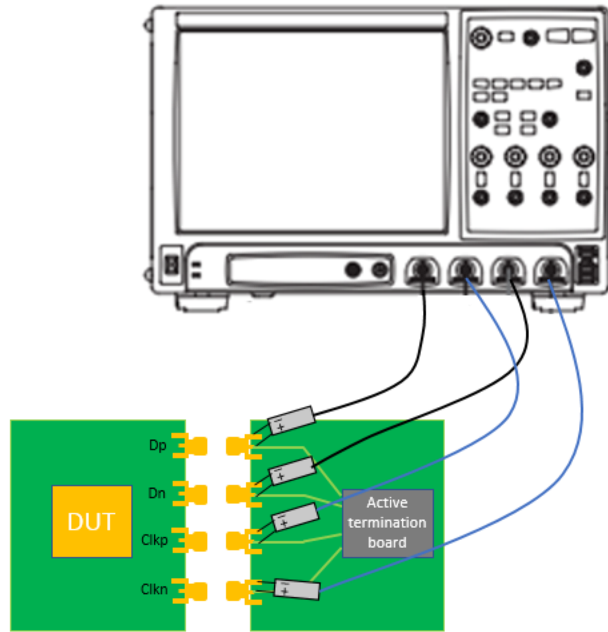

Figure 97 Probing for High Speed Data Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 97 are just for illustration).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1. Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2. In the MIPI D-PHY Test app, click the **Set Up** tab.
3. Enter the High-Speed Data Rate, Device ID and User Comments.
4. Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

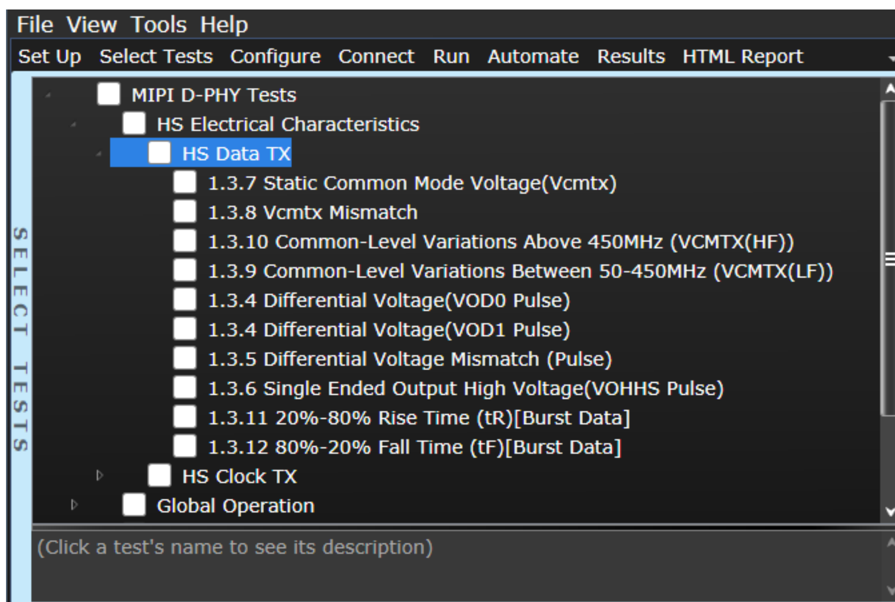

Figure 98 Selecting High Speed Data Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app’s task flow to set up the configuration options, run the tests and view the tests results.

Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation

For information about this test, refer to "Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation".

Test References

See Section 9.1.1 Table 20 in the D-PHY Specification v2.0.

Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($\Delta V_{CMTX(1,0)}$) Method of Implementation

For information about this test, refer to "Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($\Delta V_{CMTX}(_{1,0})$) Method of Implementation".

Test References

See Section 9.1.1 Table 20 in the D-PHY Specification v2.0.

Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz ($\Delta V_{CMTX(HF)}$) Method of Implementation

For information about this test, refer to "Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz (ΔV_{CMTX}(HF)) Method of Implementation".

Test References

See Section 9.1.1 Table 21 in the D-PHY Specification v2.0.

Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz ($\Delta V_{CMTX(LF)}$) Method of Implementation

For information about this test, refer to "Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz (ΔV_{CMTX}(LF)) Method of Implementation".

Test References

See Section 9.1.1 Table 21 in the D-PHY Specification v2.0.

Test 1.3.4 HS Data TX Differential Voltage (V_{OD} Pulse) Method of Implementation

The output differential voltage, V_{OD} is defined as the difference of voltages V_{DP} and V_{DN} at the Dp and Dn pins, respectively.

$$V_{OD} = V_{DP} - V_{DN}$$

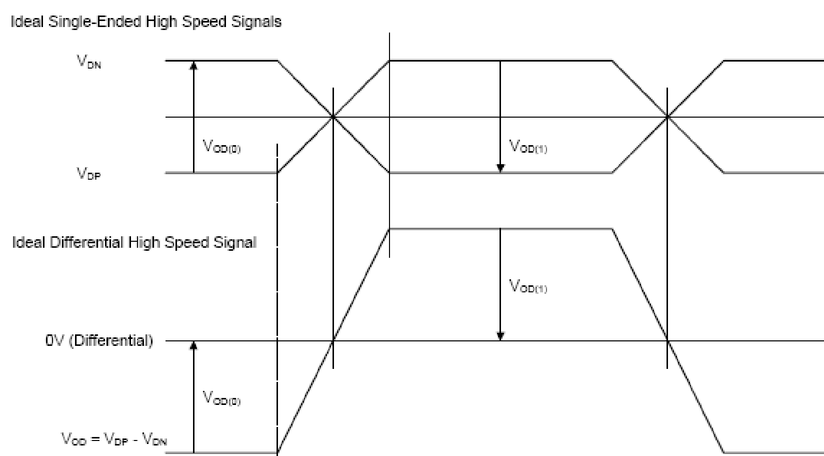

Figure 99 Ideal Single-Ended and Differential High Speed Signals

PASS Condition

The measured V_{OD} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 76 Test Availability Condition for Test 1.3.4 (when HS Data Rate is higher than 1500 Mbps)

Associated Test IDs		8133	8134
Conditions			
HS Data Rate		Not applicable	Not applicable
Continuous Data		Not applicable	Not applicable
Continuous Clock		Not applicable	Not applicable
Data LP EscapeMode		Not applicable	Not applicable
Clock LP EscapeMode		Not applicable	Not applicable
Clock ULPS Mode		Not applicable	Not applicable
Informative Test		Applicable	Applicable
Probing Methods	**Active Probe (Differential Probe)**	Available	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock and Continuous Data settings	Availability dependent on Continuous Clock and Continuous Data settings
	Direct Connect	Availability dependent on Continuous Clock and Continuous Data settings	Availability dependent on Continuous Clock and Continuous Data settings

Table 77 Test Availability Condition for Test 1.3.4 (when HS Data Rate is lower than or equal to 1500 Mbps)

Associated Test IDs		8131	8132
Conditions			
HS Data Rate		Not applicable	Not applicable
Continuous Data		Not applicable	Not applicable
Continuous Clock		Not applicable	Not applicable
Data LP EscapeMode		Not applicable	Not applicable
Clock LP EscapeMode		Not applicable	Not applicable
Clock ULPS Mode		Not applicable	Not applicable
Informative Test		Not applicable	Not applicable
Probing Methods	**Active Probe (Differential Probe)**	Available	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock and Continuous Data settings	Availability dependent on Continuous Clock and Continuous Data settings
	Direct Connect	Availability dependent on Continuous Clock and Continuous Data settings	Availability dependent on Continuous Clock and Continuous Data settings

Measurement Algorithm using Test IDs 8131, 8133, 8132, and 8134

HS Data TX Differential Voltage (V_{OD0} Pulse)

NOTE **Use the Test ID# 8131 and 8133 to remotely access the test.**

HS Data TX Differential Voltage (V_{OD1} Pulse)

NOTE **Use the Test ID# 8132 and 8134 to remotely access the test.**

1 Trigger at SoT of HS data burst (LP11 to LP01).
2 Find the HS data bursts.
3 For HS data, differential waveform is required. The waveform can be constructed by using the following equation:

DataDiff = Dp-Dn

4 For the HS Clock, differential waveform is required. The waveform can be constructed by using the following equation:

ClkDiff = Clkp - Clkn

5 The acquired waveform is searched for the respective reference data pattern of “011111” for V_{OD1} and “100000” for V_{OD0} test.
6 Generates the averaged waveform that consists of all the reference data pattern found.
7 The mean value for the histogram window that fall between the centers of the fourth and fifth ‘1’ bits is measured as the mean V_{OD} value using the histogram function.
8 Report the measurement results:
   - Mean V_{OD} for Differential-1 or Differential-0
9 Compare the mean V_{OD} value to the compliance test limit.

Test References

See Section 9.1.1 Table 25 in the D-PHY Specification v2.1.

Test 1.3.5 HS Data TX Differential Voltage Mismatch (Pulse) (ΔV_{OD}) Method of Implementation

The Output Differential Voltage Mismatch, ΔV_{OD} is defined as the difference of the absolute values of the differential output voltage in the Differential-1 state $V_{OD(1)}$ and the differential output voltage in the Differential-0 state $V_{OD(0)}$.

$$\Delta V_{OD} = \left|V_{OD(1)}\right| - \left|V_{OD(0)}\right|$$

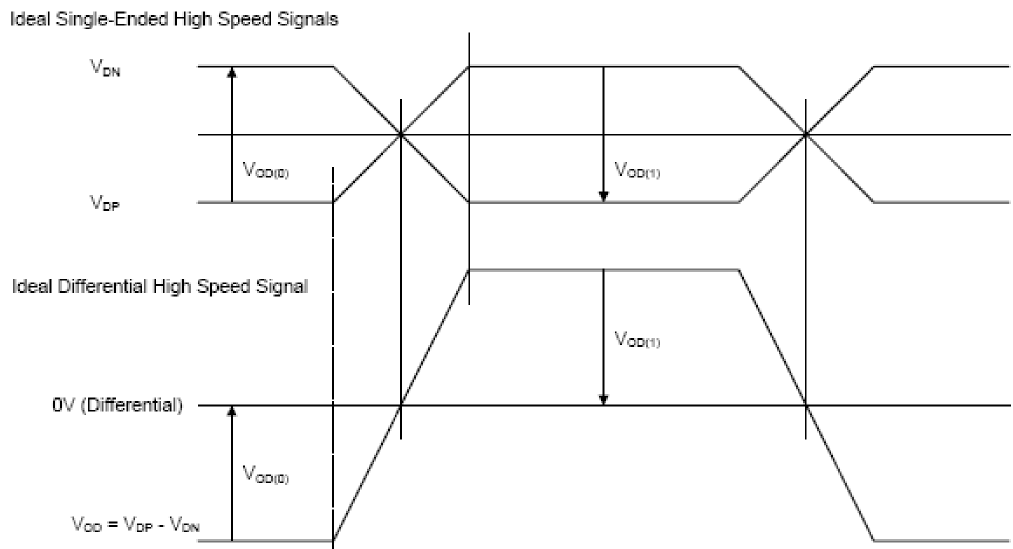

Figure 100 Ideal Single-Ended and Differential High Speed Signals.

PASS Condition

The measured ΔV_{OD} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 78 Test Availability Condition for Test 1.3.5 (when HS Data Rate is higher than 1500 Mbps)

Associated Test IDs		8142
Conditions		
HS Data Rate		Not applicable
Continuous Data		Not applicable
Continuous Clock		Not applicable
Data LP EscapeMode		Not applicable
Clock LP EscapeMode		Not applicable
Clock ULPS Mode		Not applicable
Informative Test		Applicable
Probing Methods	Active Probe (Differential Probe)	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock and Continuous Data settings
	Direct Connect	Availability dependent on Continuous Clock and Continuous Data settings

Table 79 Test Availability Condition for Test 1.3.5 (when HS Data Rate is lower than or equal to 1500 Mbps)

Associated Test IDs		8141
Conditions		
HS Data Rate		Not applicable
Continuous Data		Not applicable
Continuous Clock		Not applicable
Data LP EscapeMode		Not applicable
Clock LP EscapeMode		Not applicable
Clock ULPS Mode		Not applicable
Informative Test		Not applicable
Probing Methods	Active Probe (Differential Probe)	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock and Continuous Data settings
	Direct Connect	Availability dependent on Continuous Clock and Continuous Data settings

Measurement Algorithm using Test ID 8141 and 8142

HS Data TX Differential Voltage Mismatch (Pulse)

NOTE Use the Test ID# 8141 and 8142 to remotely access the test.

1 This test requires the following prerequisite tests:
   - HS Data TX Differential Voltage (V_{OD0} Pulse) (Test ID: 8131)
   - HS Data TX Differential Voltage (V_{OD1} Pulse) (Test ID: 8132)
   - The actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
2 Calculate the difference between V_{OD} for Differential-1 and Differential-0.
3 Report the measurement results:
   - V_{OD} for Differential-1 and Differential-0
4 Compare the measured ΔV_{OD} between Differential-1 and Differential-0 value to the compliance test limit.

Test References

See Section 9.1.1 Table 25 in the D-PHY Specification v2.1.

Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation

For information about this test, refer to "Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation".

Test References

See Section 9.1.1 Table 20 in the D-PHY Specification v2.0 (23Nov2015).

Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation

The rise time, t_R is defined as the transition time between 20% and 80% of the full HS signal swing. The driver must meet the t_R specifications for all the allowable Z_{ID}.

PASS Condition

The measured t_R value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 80 Test Availability Condition for Test 1.3.11

Associated Test IDs		81101	81102	81104	81105
Conditions					
HS Data Rate		Applicable	Applicable	Applicable	Applicable
Continuous Data		Disabled	Enabled	Disabled	Enabled
Continuous Clock		Not applicable	Not applicable	Not applicable	Not applicable
Data LP EscapeMode		Not applicable	Not applicable	Not applicable	Not applicable
Clock LP EscapeMode		Not applicable	Not applicable	Not applicable	Not applicable
Clock ULPS Mode		Not applicable	Not applicable	Not applicable	Not applicable
Informative Test		Not applicable	Not applicable	Enabled	Enabled
Probing Methods	**Active Probe (Differential Probe)**	Available	Available	Available	Available
	Direct Connect (Active Termination Adapter)	Not available	Availability dependent on Continuous Clock and Continuous Data settings	Not available	Availability dependent on Continuous Clock and Continuous Data settings
	Direct Connect	Not available	Availability dependent on Continuous Clock and Continuous Data settings	Not available	Availability dependent on Continuous Clock and Continuous Data settings

Measurement Algorithm using Test ID 81101

NOTE Use the Test ID# 81101 to remotely access the test. This test is applicable up to 1500 Mbps data rate.

1 This test requires the following prerequisite tests:
   a HS Entry: Data TX $T_{HS\text{-}PREPARE} + T_{HS\text{-}ZERO}$ (Test ID: 558 for Test ID: 81101)
   Actual value for V_{HS_ZERO} is measured and test results are stored.
2 Trigger on SoT of HS Data burst (LP11->LP01).
3 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform using the following equation:

DataDiff = Dp-Dn

4 Define the measurement threshold as follows:

   Top Level: Inverse of V_{HS_ZERO}

   Base Level: V_{HS_ZERO}

5 Use a MATLAB script to identify and extract all the “000111” pattern locations found in the differential signal.
6 Measure the 20%-80% rise time at all the rising edges of the “000111” pattern that is identified.
7 Compare the measured t_R (Mean) value with the maximum conformance test limit.

Measurement Algorithm using Test ID 81102

NOTE **Use the Test ID# 81102 to remotely access the test. This test is applicable up to 1500 Mbps data rate.**

1 This test requires the following prerequisite tests:
   a HS Clock Instantaneous (UI_{inst})[Max] (Test ID: 911)
   UI value measurements for test signal are performed and test results are stored.
   b HS Data TX Differential Voltage (V_{OD}) (Test ID: 8131, 8132)
   Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
2 Trigger on SoT of HS Continuous Data.
3 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform using the following equation:

DataDiff = Dp-Dn

4 Define the measurement threshold as follows:

   Top Level: V_{OD1} (V_{OD} for Differential-1)

   Base Level: V_{OD0} (V_{OD} for Differential-0)

5 Use a MATLAB script to identify and extract all the “000111” pattern locations found in the differential signal.
6 Measure the 20%-80% rise time at all the rising edges of the “000111” pattern that is identified.
7 Compare the measured t_R (Mean) value with the maximum conformance test limit.

Measurement Algorithm using Test ID 81104

NOTE **Use the Test ID# 81104 to remotely access the test. This test is applicable up to 1500 Mbps data rate. This test is an informative test.**

1 This test requires the following prerequisite test:
   a Data Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 81101)
   Rise time measurements are performed and t_R (Mean) test result is stored.
2 Compare the measured t_R (Mean) value with the minimum conformance test limits.

Measurement Algorithm using Test ID 81105

NOTE Use the Test ID# 81105 to remotely access the test. This test is applicable up to 1500 Mbps data rate. This test is an informative test.

1 This test requires the following prerequisite test:
   a Data Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 81102)
   Rise time measurements are performed and t_R (Mean) test result is stored.
2 Compare the measured t_R (Mean) value with the minimum conformance test limits.

Test References

See Test 1.3.11 in CTS v1.2 and Section 9.1.1 Table 20 in the D-PHY Specification v1.2.

Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation

The fall time, t_F is defined as the transition time between 80% and 20% of the full HS signal swing. The driver must meet the t_F specifications for all the allowable Z_{ID}.

PASS Condition

The measured t_F value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 81 Test Availability Condition for Test 1.3.12

Associated Test IDs		81111	81112	81114	81115
Conditions					
HS Data Rate		Applicable	Applicable	Applicable	Applicable
Continuous Data		Disabled	Enabled	Disabled	Enabled
Continuous Clock		Not applicable	Not applicable	Not applicable	Not applicable
Data LP EscapeMode		Not applicable	Not applicable	Not applicable	Not applicable
Clock LP EscapeMode		Not applicable	Not applicable	Not applicable	Not applicable
Clock ULPS Mode		Not applicable	Not applicable	Not applicable	Not applicable
Informative Test		Not applicable	Not applicable	Enabled	Enabled
Probing Methods	**Active Probe (Differential Probe)**	Available	Available	Available	Available
	Direct Connect (Active Termination Adapter)	Not available	Availability dependent on Continuous Clock and Continuous Data settings	Not available	Availability dependent on Continuous Clock and Continuous Data settings
	Direct Connect	Not available	Availability dependent on Continuous Clock and Continuous Data settings	Not available	Availability dependent on Continuous Clock and Continuous Data settings

Measurement Algorithm using Test ID 81111

NOTE Use the Test ID# 81111 to remotely access the test. This test is applicable up to 1500 Mbps data rate.

1 This test requires the following prerequisite tests:

   a HS Entry: Data TX $T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$ (Test ID: 558 for Test ID: 81111)

   Actual value for V_{HS_ZERO} is measured and test results are stored.

2 Trigger on SoT of the HS Data burst (LP11->LP01).

3 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform using the following equation:

$$DataDiff = Dp-Dn$$

4 Define the measurement threshold as follows:

Top Level: Inverse of V_{HS_ZERO}

Base Level: V_{HS_ZERO}

5 Use a MATLAB script to identify and extract all the “111000” pattern locations found in the differential signal.
6 Measure the 80%-20% fall time at all the falling edges of the “111000” pattern that is identified.
7 Compare the measured value of t_F (Mean) with the maximum conformance test limit.

Measurement Algorithm using Test ID 81112

NOTE **Use the Test ID# 81112 to remotely access the test. This test is applicable up to 1500 Mbps data rate.**

1 This test requires the following prerequisite tests:
   a HS Clock Instantaneous (UI_{inst})[Max] (Test ID: 911)
   UI value measurements for test signal are performed and test results are stored.
   b HS Data TX Differential Voltage (V_{OD}) (Test ID: 8131, 8132)
   Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
2 Trigger on SoT of HS Continuous Data.
3 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform using the following equation:

$$Data_{Diff} = Dp\text{-}Dn$$

4 Define the measurement threshold as follows:

Top Level: V_{OD1} (V_{OD} for Differential-1)

Base Level: V_{OD0} (V_{OD} for Differential-0)

5 Use a MATLAB script to identify and extract all the “111000” pattern locations found in the differential signal.
6 Measure the 80%-20% fall time at all the falling edges of the “111000” pattern that is identified.
7 Compare the measured t_F (Mean) value with the maximum conformance test limit.

Measurement Algorithm using Test ID 81114

NOTE **Use the Test ID# 81114 to remotely access the test. This test is applicable up to 1500 Mbps data rate. This test is an informative test.**

1 This test requires the following prerequisite test:
   a Data Lane HS-TX 80%-20% Fall Time (t_F) (Test ID: 81111)
   Fall time measurements are performed and t_F (Mean) test result is stored.
2 Compare the measured t_F (Mean) value with the minimum conformance test limits.

Measurement Algorithm using Test ID 81115

NOTE **Use the Test ID# 81115 to remotely access the test. This test is applicable up to 1500 Mbps data rate. This test is an informative test.**

1 This test requires the following prerequisite test:
   a Data Lane HS-TX 80%-20% Fall Time (t_F) (Test ID: 81112)
      Fall time measurements are performed and t_F (Mean) test result is stored.
2 Compare the measured t_F (Mean) value with the minimum conformance test limits.

Test References

See Test 1.3.12 in CTS v1.2 and Section 9.1.1 Table 20 in the D-PHY Specification v1.2.

Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz ($\Delta V_{CMTX(LF)}$) Method of Implementation

For information about this test, refer to "Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz (ΔV_{CMTX}(LF)) Method of Implementation".

Test References

See Section 9.1.1 Table 21 in the D-PHY Specification v2.0.

See D-PHY Specification v2.1, Section 9.1.1, Table 26

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Test 1.4.7 HS Clock TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation / 380
Test 1.4.8 HS Clock TX VCMTX Mismatch ($\Delta V_{CMTX}(_{1,0})$) Method of Implementation / 380
Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz (ΔV_{CMTX}(HF)) Method of Implementation / 380
Test 1.4.4 HS Clock TX Differential Voltage (V_{OD} Pulse) Method of Implementation / 381
Test 1.4.5 HS Clock TX Differential Voltage Mismatch (Pulse) (ΔV_{OD}) Method of Implementation / 384
Test 1.4.6 HS Clock TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation / 387
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Test 1.4.17 HS Clock Instantaneous Method of Implementation / 394
Test 1.4.18 Clock Lane HS Clock Delta UI (UI variation) Method of Implementation / 395
Test 1.4.20 Clock Lane HS Clock Period Jitter Method of Implementation / 396

This section provides the Methods of Implementation (MOIs) for the High Speed Clock Transmitter (HS Clock T_X) Electrical tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 2.0 and 2.1 HS Clock TX tests are similar to the MIPI D-PHY 1.2 HS Clock TX tests. Hence, they share the same Method of Implementation (MOI) as all the corresponding MIPI D-PHY 1.2 tests. For details of MIPI D-PHY 1.2 tests, refer to "MIPI D-PHY 1.2 High Speed Clock Transmitter (HS Clock TX) Electrical Tests".

The current chapter lists the references from the MIPI D-PHY 2.0 specification.

Probing for High Speed Clock Transmitter Electrical Tests

When performing the HS Clock T_X tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the HS Clock T_X tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

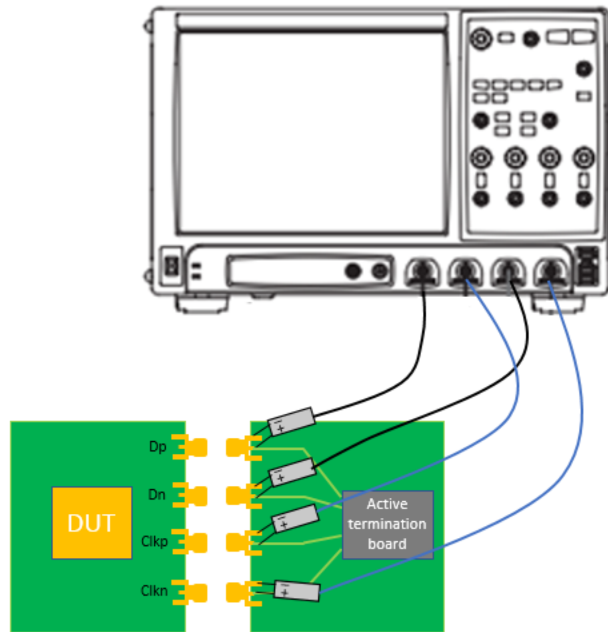


Figure 101 Probing for High Speed Clock Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 101 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

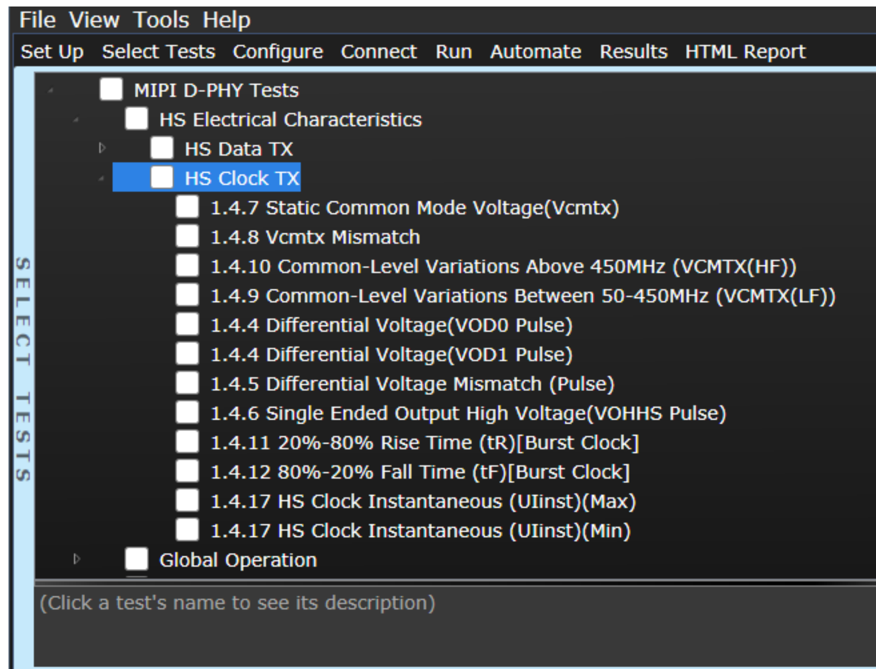


Figure 102 Selecting High Speed Clock Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app’s task flow to set up the configuration options, run the tests and view the tests results.

Test 1.4.7 HS Clock TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation

For information about this test, refer to "Test 1.4.7 HS Clock TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation".

Test References

See Section 9.1.1 Table 20 in the D-PHY Specification v2.0.

Test 1.4.8 HS Clock TX V_{CMTX} Mismatch ($\Delta V_{CMTX(1,0)}$) Method of Implementation

For information about this test, refer to "Test 1.4.8 HS Clock TX VCMTX Mismatch ($\Delta V_{CMTX}(_{1,0})$) Method of Implementation".

Test References

See Section 9.1.1 Table 20 in the D-PHY Specification v2.0.

Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz ($\Delta V_{CMTX(HF)}$) Method of Implementation

For information about this test, refer to "Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz (ΔV_{CMTX}(HF)) Method of Implementation".

Test References

See Section 9.1.1 Table 21 in the D-PHY Specification v2.0.

Test 1.4.4 HS Clock TX Differential Voltage (V_{OD} Pulse) Method of Implementation

The Output Differential Voltage, V_{OD} is defined as the difference of voltages V_{DP} and V_{DN} at the Dp and Dn pins, respectively.

$$V_{OD} = V_{DP} - V_{DN}$$

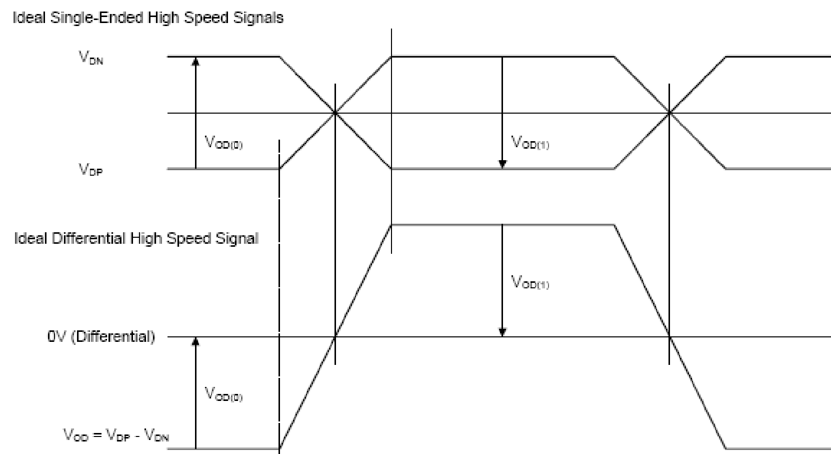


Figure 103 Ideal Single-Ended and Differential High Speed Signals

PASS Condition

The measured V_{OD} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 82 Test Availability Condition for Test 1.4.4 (when HS Data Rate is higher than 1500 Mbps)

Associated Test IDs		18133	18134
Conditions			
HS Data Rate		Not applicable	Not applicable
Continuous Data		Not applicable	Not applicable
Continuous Clock		Not applicable	Not applicable
Data LP EscapeMode		Not applicable	Not applicable
Clock LP EscapeMode		Not applicable	Not applicable
Clock ULPS Mode		Not applicable	Not applicable
Informative Test		Applicable	Applicable
Probing Methods	Active Probe (Differential Probe)	Available	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock setting	Availability dependent on Continuous Clock setting
	Direct Connect	Availability dependent on Continuous Clock setting	Availability dependent on Continuous Clock setting

Table 83 Test Availability Condition for Test 1.4.4 (when HS Data Rate is lower than or equal to 1500 Mbps)

Associated Test IDs		18131	18132
Conditions			
HS Data Rate		Not applicable	Not applicable
Continuous Data		Not applicable	Not applicable
Continuous Clock		Not applicable	Not applicable
Data LP EscapeMode		Not applicable	Not applicable
Clock LP EscapeMode		Not applicable	Not applicable
Clock ULPS Mode		Not applicable	Not applicable
Informative Test		Not applicable	Not applicable
Probing Methods	Active Probe (Differential Probe)	Available	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock setting	Availability dependent on Continuous Clock setting
	Direct Connect	Availability dependent on Continuous Clock setting	Availability dependent on Continuous Clock setting

Measurement Algorithm using Test IDs 18131, 18132, 18133, and 18134

HS Clock TX Differential Voltage (V_{OD0} Pulse)

NOTE Use the Test ID# 18131 and 18133 to remotely access the test.

HS Clock TX Differential Voltage (V_{OD1} Pulse)

NOTE Use the Test ID# 18132 and 18134 to remotely access the test.

1 Trigger the oscilloscope to acquire Clkp and Clkn.
2 Construct the differential waveform using the following equation:

ClkDiff = Clkp-Clkn

3 Search the acquired waveform for the reference data pattern of “01” for V_{OD1} and “10” for V_{OD0} separately.
4 Generate the average waveform that consists of the reference data patterns.
5 Measure the mean value for the histogram window that falls between the centers of the ‘1’ bits as the Mean V_{OD1} value using the histogram function. For V_{OD0}, set the histogram window to measure the centers of the ‘0’ bits.
6 Report the measurement results
   - Mean V_{OD} for Differential-1 and Differential-0
7 Compare the mean V_{OD} value to the compliance test limits.

Test References

See Section 9.1.1, Table 25 in the D-PHY Specification v2.1.

Test 1.4.5 HS Clock TX Differential Voltage Mismatch (Pulse) (ΔV_{OD}) Method of Implementation

The output differential voltage mismatch, ΔV_{OD} is defined as the difference of the absolute values of the differential output voltage in the Differential-1 state $V_{OD(1)}$ and the differential output voltage in the Differential-0 state $V_{OD(0)}$.

$$\Delta V_{OD} = \left|V_{OD(1)}\right| - \left|V_{OD(0)}\right|$$

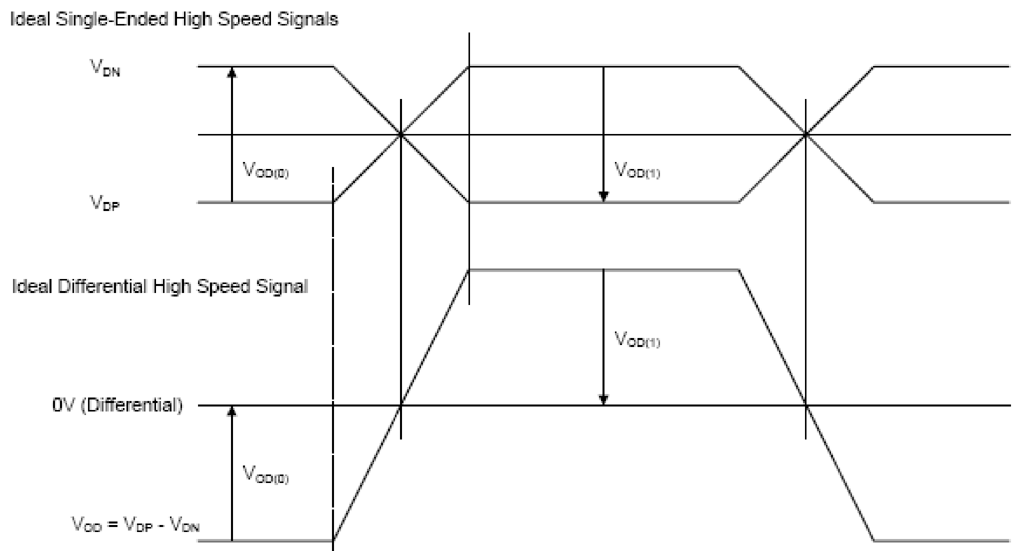


Figure 104 Ideal Single-Ended and Differential High Speed Signals.

PASS Condition

The measured ΔV_{OD} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 84 Test Availability Condition for Test 1.4.5 (when HS Data Rate is higher than 1500 Mbps)

Associated Test IDs		18142
Conditions		
HS Data Rate		Not applicable
Continuous Data		Not applicable
Continuous Clock		Not applicable
Data LP EscapeMode		Not applicable
Clock LP EscapeMode		Not applicable
Clock ULPS Mode		Not applicable
Informative Test		Applicable
Probing Methods	**Active Probe (Differential Probe)**	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock setting
	Direct Connect	Availability dependent on Continuous Clock setting

Table 85 Test Availability Condition for Test 1.4.5 (when HS Data Rate is lower than or equal to 1500 Mbps)

Associated Test IDs		18141
Conditions		
HS Data Rate		Not applicable
Continuous Data		Not applicable
Continuous Clock		Not applicable
Data LP EscapeMode		Not applicable
Clock LP EscapeMode		Not applicable
Clock ULPS Mode		Not applicable
Informative Test		Not applicable
Probing Methods	**Active Probe (Differential Probe)**	Available
	Direct Connect (Active Termination Adapter)	Availability dependent on Continuous Clock setting
	Direct Connect	Availability dependent on Continuous Clock setting

Measurement Algorithm using Test ID 18141 and 18142

HS Clock TX Differential Voltage Mismatch (Pulse)

NOTE Use the Test ID# 18141 and 18142 to remotely access the test.

1 This test requires the following prerequisite tests.
   a HS Clock TX Differential Voltage (V_{OD0} Pulse) (Test ID: 18131)
   b HS Clock TX Differential Voltage (V_{OD1} Pulse) (Test ID: 18132)

   The actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
2 Calculate the difference between V_{OD} for Differential-1 and Differential-0.
3 Report the measurement results.
   a V_{OD} for Differential-1 and Differential-0
4 Compare the measured ΔV_{OD} between Differential-1 and Differential-0 value with the compliance test limit.

Test References

See Section 9.1.1, Table 25 in the D-PHY Specification v2.1.

Test 1.4.6 HS Clock TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation

For information about this test, refer to "Test 1.4.6 HS Clock TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation".

Test References

See Section 9.1.1 Table 20 in the D-PHY Specification v2.0.

Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation

The rise time, t_R is defined as the transition time between 20% and 80% of the full HS signal swing. The driver must meet the t_R specifications for all allowable Z_{ID}.

PASS Condition

The measured t_R value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 86 Test Availability Condition for Test 1.4.11

Associated Test IDs		181101	181102	181103	181104	181105	181106
Conditions							
HS Data Rate		Applicable	Applicable	Applicable	Applicable	Applicable	Applicable
Continuous Data		Not applicable	Disabled	Dependent on Continuous Clock setting	Not applicable	Disabled	Dependent on Continuous Clock setting
Continuous Clock		Disabled	Dependent on Continuous Data setting	Enabled	Disabled	Dependent on Continuous Data setting	Enabled
Data LP EscapeMode		Not applicable	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
Clock LP EscapeMode		Not applicable	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
Clock ULPS Mode		Not applicable	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
Informative Test		Not applicable	Not applicable	Not applicable	Enabled	Enabled	Enabled
Probing Methods	Active Probe (Differential Probe)	Available	Available	Available	Available	Available	Available
	Direct Connect (Active Termination Adapter)	Not Available	Not Available	Availability dependent on Continuous Clock setting	Not Available	Not Available	Availability dependent on Continuous Clock setting
	Direct Connect	Not Available	Not Available	Availability dependent on Continuous Clock setting	Not Available	Not Available	Availability dependent on Continuous Clock setting

Measurement Algorithm using Test ID 181101

> **NOTE** Use the Test ID# 181101 to remotely access the test. This test is only available up to 1500 Mbps data rate.

1 This test requires the following prerequisite tests:

a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)

Measure the UI value for the test signal and test results are stored.

b HS Entry: CLK TX $T_{CLK-PREPARE} + T_{CLK-ZERO}$ (Test ID: 554)

Measure the actual value of V_{HS_ZERO} and the test results are stored.

2 Trigger the oscilloscope to acquire Clkp and Clkn.
3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

Top Level: Inverse of V_{HS_ZERO}

Base Level: V_{HS_ZERO}

5 Use a MATLAB script to identify and extract all “01” pattern locations found in the differential signal.
6 Measure the 20%-80% rise time at all rising edges of the “01” pattern that is identified.
7 Compare the value of the measured t_R (Mean) with the maximum compliance test limit.

Measurement Algorithm using Test ID 181102

NOTE **Use the Test ID# 181102 to remotely access the test. This test is only available up to 1500 Mbps data rate.**

1 This test requires the following prerequisite test:
   a Data Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 81101)
   Measure the actual value of V_{HS_ZERO} and the test results are stored.
2 Trigger the oscilloscope to acquire Clkp and Clkn.
3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

Top Level: Inverse of V_{HS_ZERO}

Base Level: V_{HS_ZERO}

5 Use a MATLAB script to identify and extract all “01” pattern locations found in the differential signal.
6 Measure the 20%-80% rise time at all rising edges of the “01” pattern that is identified.
7 Compare the value of the measured t_R (Mean) with the maximum compliance test limit.

Measurement Algorithm using Test ID 181103

NOTE **Use the Test ID# 181103 to remotely access the test. This test is only available up to 1500 Mbps data rate.**

1 This test requires the following prerequisite tests:
   a HS Clock Instantaneous (UI_{inst})[Max] (Test ID: 911)
   UI value measurements for test signal are performed and test results are stored.
   b HS Clock T_X Differential Voltage (V_{OD}) (Test ID: 18131, 18132)
   Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
2 Trigger the oscilloscope to acquire Clkp and Clkn.

3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

Top Level: V_{OD1} (V_{OD} for Differential-1)

Base Level: V_{OD0} (V_{OD} for Differential-0)

5 Use a MATLAB script to identify and extract all “01” pattern locations found in the differential signal.
6 Measure the 20%-80% rise time at all rising edges of the “01” pattern that is identified.
7 Compare the value of the measured t_R (Mean) with the maximum compliance test limit.

Measurement Algorithm using Test ID 181104

NOTE **Use the Test ID# 181104 to remotely access the test. This test is only available up to 1500 Mbps data rate. This test is an informative test.**

1 This test requires the following prerequisite test:
   a Clock Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 181101)
   Rise time measurements are performed and t_R (Mean) test result is stored.
2 Compare the value of the measured t_R (Mean) with the minimum compliance test limits.

Measurement Algorithm using Test ID 181105

NOTE **Use the Test ID# 181105 to remotely access the test. This test is only available up to 1500 Mbps data rate. This test is an informative test.**

1 This test requires the following prerequisite test:
   a Clock Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 181102)
   Rise time measurements are performed and t_R (Mean) test result is stored.
2 Compare the value of the measured t_R (Mean) with the minimum compliance test limits.

Measurement Algorithm using Test ID 181106

NOTE **Use the Test ID# 181106 to remotely access the test. This test is only available up to 1500 Mbps data rate. This test is an informative test.**

1 This test requires the following prerequisite test:
   a Clock Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 181103)
   Rise time measurements are performed and t_R (Mean) test result is stored.
2 Compare the value of the measured t_R (Mean) with the minimum compliance test limits.

Test References

See Test 1.4.11 in CTS v1.2 and Section 9.1.1 Table 20 in the D-PHY Specification v1.2.

Test 1.4.12 Clock Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation

The fall time, t_F is defined as the transition time between 80% and 20% of the full HS signal swing. The driver must meet the t_F specifications for all allowable Z_{ID}.

PASS Condition

The measured t_F value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 87 Test Availability Condition for Test 1.4.12

Associated Test IDs		181111	181112	181113	181114	181115	181116
Conditions							
HS Data Rate		Applicable	Applicable	Applicable	Applicable	Applicable	Applicable
Continuous Data		Not applicable	Disabled	Dependent on Continuous Clock setting	Not applicable	Disabled	Dependent on Continuous Clock setting
Continuous Clock		Disabled	Dependent on Continuous Data setting	Enabled	Disabled	Dependent on Continuous Data setting	Enabled
Data LP EscapeMode		Not applicable	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
Clock LP EscapeMode		Not applicable	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
Clock ULPS Mode		Not applicable	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
Informative Test		Not applicable	Not applicable	Not applicable	Enabled	Enabled	Enabled
Probing Methods	**Active Probe (Differential Probe)**	Available	Available	Available	Available	Available	Available
	Direct Connect (Active Termination Adapter)	Not Available	Not Available	Availability dependent on Continuous Clock setting	Not Available	Not Available	Availability dependent on Continuous Clock setting
	Direct Connect	Not Available	Not Available	Availability dependent on Continuous Clock setting	Not Available	Not Available	Availability dependent on Continuous Clock setting

Measurement Algorithm using Test ID 181111

NOTE **Use the Test ID# 181111 to remotely access the test. This test is only available up to 1500 Mbps data rate.**

1 This test requires the following prerequisite tests:

   a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)

   Measure the minimum, maximum and average values of the Unit Interval for the differential clock waveform and the test results are stored.

   b HS Entry: CLK TX $T_{CLK-PREPARE} + T_{CLK-ZERO}$ (Test ID: 554)

   Measure the actual value of V_{HS_ZERO} and the test results are stored.

2 Trigger the oscilloscope to acquire Clkp and Clkn.

3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

   Top Level: Inverse of V_{HS_ZERO}

   Base Level: V_{HS_ZERO}

5 Use a MATLAB script to identify and extract all “10” pattern locations found in the differential signal.

6 Measure the 80%-20% fall time at all falling edges of the “10” pattern that is identified.

7 Compare the value of the measured t_F (Mean) with the maximum compliance test limit.

Measurement Algorithm using Test ID 181112

NOTE **Use the Test ID# 181112 to remotely access the test. This test is only available up to 1500 Mbps data rate.**

1 This test requires the following prerequisite tests:

   a Data Lane HS-TX 80%-20% Fall Time (t_F) (Test ID: 81111)

   Measure the actual value of V_{HS_ZERO} and the test results are stored.

2 Trigger the oscilloscope to acquire Clkp and Clkn.

3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

   Top Level: Inverse of V_{HS_ZERO}

   Base Level: V_{HS_ZERO}

5 Use a MATLAB script to identify and extract all “10” pattern locations found in the differential signal.

6 Measure the 80%-20% fall time at all falling edges of the “10” pattern that is identified.

7 Compare the value of the measured t_F (Mean) with the maximum compliance test limit.

Measurement Algorithm using Test ID 181113

NOTE Use the Test ID# 181113 to remotely access the test. This test is only available up to 1500 Mbps data rate.

1. This test requires the following prerequisite tests:
   - *a* HS Clock Instantaneous (UI_{inst})[Max] (Test ID: 911)
     UI value measurements for test signal are performed and test results are stored.
   - *b* HS Clock T_X Differential Voltage (V_{OD}) (Test ID: 18131, 18132)
     Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
2. Trigger the oscilloscope to acquire Clkp and Clkn.
3. Construct differential waveform by using the following equation:

   ClkDiff = Clkp-Clkn

4. Define the measurement threshold as:

   Top Level: V_{OD1} (V_{OD} for Differential-1)

   Base Level: V_{OD0} (V_{OD} for Differential-0)

5. Use a MATLAB script to identify and extract all “10” pattern locations found in the differential signal.
6. Measure the 80%-20% fall time at all falling edges of the “10” pattern that is identified.
7. Compare the value of the measured t_F (Mean) with the maximum compliance test limits.

Measurement Algorithm using Test ID 181114

NOTE Use the Test ID# 181114 to remotely access the test. This test is only available up to 1500 Mbps data rate. This test is an informative test.

1. This test requires the following prerequisite test:
   - *a* Clock Lane HS-TX 80%-20% Fall Time (t_F) (Test ID: 181111)
     Fall time measurements are performed and t_F (Mean) test result is stored.
2. Compare the value of the measured t_F (Mean) with the minimum compliance test limits.

Measurement Algorithm using Test ID 181115

NOTE Use the Test ID# 181115 to remotely access the test. This test is only available up to 1500 Mbps data rate. This test is an informative test.

1. This test requires the following prerequisite test:
   - *a* Clock Lane HS-TX 80%-20% Fall Time (t_F) (Test ID: 181112)
     Fall time measurements are performed and t_F (Mean) test result is stored.
2. Compare the value of the measured t_F (Mean) with the minimum compliance test limits.

Measurement Algorithm using Test ID 181116

NOTE Use the Test ID# 181116 to remotely access the test. This test is only available up to 1500 Mbps data rate. This test is an informative test.

1 This test requires the following prerequisite test:
   a Clock Lane HS-TX 80%-20% Fall Time (t_F) (Test ID: 181113)
      Fall time measurements are performed and t_F (Mean) test result is stored.
2 Compare the value of the measured t_F (Mean) with the minimum compliance test limits.

Test References

See Test 1.4.12 in CTS v1.2 and Section 9.1.1 Table 20 in the D-PHY Specification v1.2.

Test 1.4.17 HS Clock Instantaneous Method of Implementation

For information about this test, refer to "Test 1.4.17 HS Clock Instantaneous Method of Implementation".

Test References

See Section 10.1 Table 30 in the D-PHY Specification v2.0.

Test 1.4.18 Clock Lane HS Clock Delta UI (UI variation) Method of Implementation

Clock Lane HS Clock Delta UI (UI variation) verifies that the frequency stability of the DUT HS Clock during a signal burst is within the conformance limits.

Test References

See Section 10.1, Table 35 in the D-PHY Specification v2.1.

Test Availability Condition

Table 88 Test Availability Condition for Test 1.4.18

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1200300	Not Applicable	100 ohm	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Direct Connect

Measurement Algorithm using Test ID 1200300

NOTE Use the Test ID# 1200300 to remotely access the test.

1 Trigger the oscilloscope to acquire Clkp and Clkn.

2 Construct the differential clock waveform using the following equation:

DiffClock = Clkp-Clkn

3 Setup the Clock Recovery to use the Explicit Clock method where the rising and falling edges of ClockDiff are used to fold clock signal to form a Clock Eye.

4 Using the histogram feature in the oscilloscope, measure the left eye crossing position and store the peak-to-peak value as LeftJitterPeaktoPeak.

5 Calculate the UI_variant based using the following equation:

UI_Variant = (LeftJitterPeaktoPeak / UIinst_mean) * 100%

6 Report the UI_variant as the final measurement result and compare this value against the conformance limits.

Test References

See Test 1.4.18 in CTS v2.1 and Section 10.1, Table 35 in the D-PHY Specification v2.1.

Test 1.4.20 Clock Lane HS Clock Period Jitter Method of Implementation

This test verifies the period jitter of the DUT HS Clock is within the conformance limits.

PASS Condition

The measured period jitter shall be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 89 Test Availability Condition for Test 1.4.20

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1200310	> 2.5 Gbps	100 ohm	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Direct Connect
1200311	> 2.5 Gbps	100 ohm	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Direct Connect

NOTE This test is not applicable for D-PHY Physical Layer Conformance Test Suite version 1.0, 1.1 and 1.2.

Measurement Algorithm using Test IDs 1200310, 1200311

NOTE This test is applicable for HS data rate >2.5 Gbps only.

NOTE Use the Test ID# 1200310 and 1200311 to remotely access the test.

1. Trigger the oscilloscope to acquire Clkp and Clkn.
2. Construct the differential clock waveform using the following equation:

   DiffClock = Clkp-Clkn
3. Setup the Clock Recovery to use the Explicit Clock method where the rising edges of ClockDiff are used to fold clock signal to form a Clock Eye.
4. Using the histogram feature in the oscilloscope, measure the left eye crossing position and store the peak-to-peak value as LeftJitterPeaktoPeak.
5. Calculate the Period_Jitter based using the following equation:

   Period_Jitter = (LeftJitterPeaktoPeak / UIinst_mean) * 100%
6. Report the Period_Jitter as the final measurement result and compare this value against the conformance limits.

Test References

See Test 1.4.20 in CTS v2.1 and Section 10.1, Table 35 in the D-PHY Specification v2.1.

31 MIPI D-PHY 2.0 & 2.1 Low Power Data Transmitter (LP Data TX) Electrical Tests

Probing for Low Power Transmitter Electrical Tests / 400
Test 1.1.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation / 402
Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation / 402
Test 1.1.3 LP TX 15%-85% Rise Time Level (T_{RLP}) EscapeMode Method of Implementation / 402
Test 1.1.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation / 402
Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock ($T_{LP-PULSE-TX}$) Method of Implementation / 403
Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock ($T_{LP-PER-TX}$) Method of Implementation / 403
Test 1.1.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation / 403

This section provides the Methods of Implementation (MOIs) for the Low Power Data Transmitter (LP Data TX) Electrical tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 2.0 and 2.1 LP Data TX tests are similar to the MIPI D-PHY 1.2 LP Data TX tests. Hence, all the tests share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.2 tests. For details, refer to "MIPI D-PHY 1.2 Low Power Data Transmitter (LP Data TX) Electrical Tests".

The current chapter lists the references from the MIPI D-PHY 2.0 specification.

KEYSIGHT TECHNOLOGIES

Probing for Low Power Transmitter Electrical Tests

When performing the LP TX tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the LP TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test Application for the exact number of probe connections.

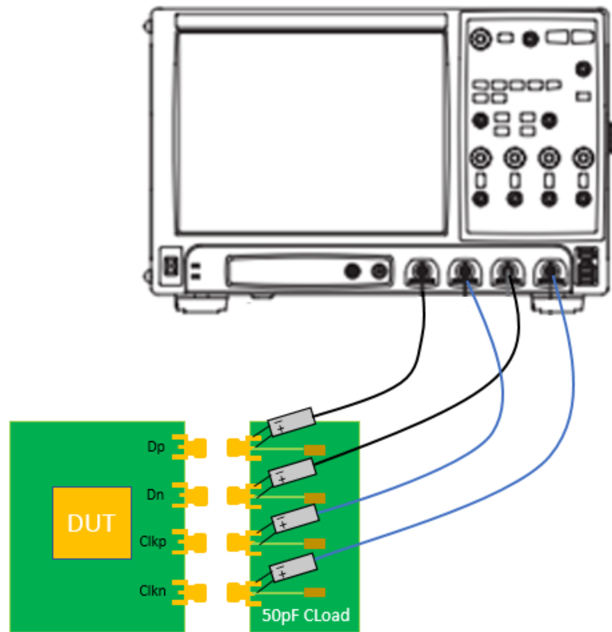


Figure 105 Probing for Low Power Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 105 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, Device ID and User Comments.
4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

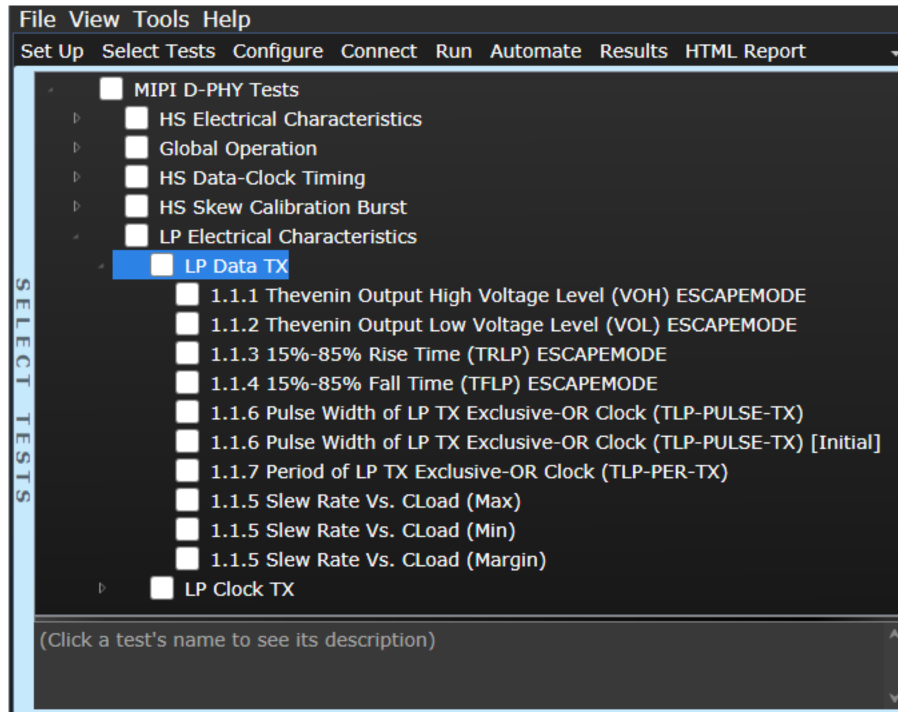


Figure 106 Selecting Low Power Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app’s task flow to set up the configuration options, run the tests and view the tests results.

Test 1.1.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation

For information about this test, refer to "Test 1.1.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation".

Test References

See Section 9.1.2 Table 22 in the D-PHY Specification v2.0.

Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation

For information about this test, refer to "Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation".

Test References

See Section 9.1.2 Table 22 in the D-PHY Specification v2.0.

Test 1.1.3 LP TX 15%-85% Rise Time Level (T_{RLP}) EscapeMode Method of Implementation

For information about this test, refer to "Test 1.1.3 LP TX 15%-85% Rise Time Level (T_{RLP}) EscapeMode Method of Implementation".

Test References

See Section 9.1.2 Table 23 in the D-PHY Specification v2.0.

Test 1.1.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation

For information about this test, refer to "Test 1.1.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation".

Test References

See Section 9.1.2 Table 23 in the D-PHY Specification v2.0.

Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock ($T_{LP-PULSE-TX}$) Method of Implementation

For information about this test, refer to "Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock ($T_{LP-PULSE-TX}$) Method of Implementation".

Test References

See Section 9.1.2 Table 23 in the D-PHY Specification v2.0.

Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock ($T_{LP-PER-TX}$) Method of Implementation

For information about this test, refer to "Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock ($T_{LP-PER-TX}$) Method of Implementation".

Test References

See Section 9.1.2 Table 23 in the D-PHY Specification v2.0.

Test 1.1.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation

For information about this test, refer to "Test 1.1.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation".

Test References

See Section 9.1.2 Table 23 in the D-PHY Specification v2.0.

32 MIPI D-PHY 2.0 & 2.1 Low Power Clock Transmitter (LP Clock TX) Electrical Tests

Probing for Low Power Transmitter Electrical Tests / 406
Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation / 408
Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation / 408
Test 1.2.3 LP TX 15%-85% Rise Time Level (T_{RLP}) Method of Implementation / 408
Test 1.2.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation / 408
Test 1.2.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation / 408

This section provides the Methods of Implementation (MOIs) for the Low Power Clock Transmitter (LP Clock TX) Electrical tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 2.0 and 2.1 LP Clock TX tests are similar to the MIPI D-PHY 1.2 LP Clock TX tests. Hence, all the tests share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.2 tests. For details, refer to "MIPI D-PHY 1.2 Low Power Clock Transmitter (LP Clock TX) Electrical Tests".

The current chapter lists the references from the MIPI D-PHY 2.0 specification.

KEYSIGHT TECHNOLOGIES

Probing for Low Power Transmitter Electrical Tests

When performing the LP TX tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the LP TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test Application for the exact number of probe connections.

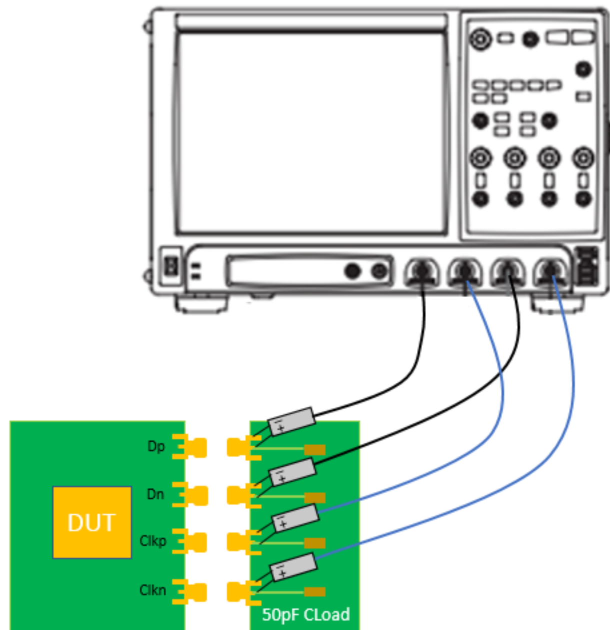


Figure 107 Probing for Low Power Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 107 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

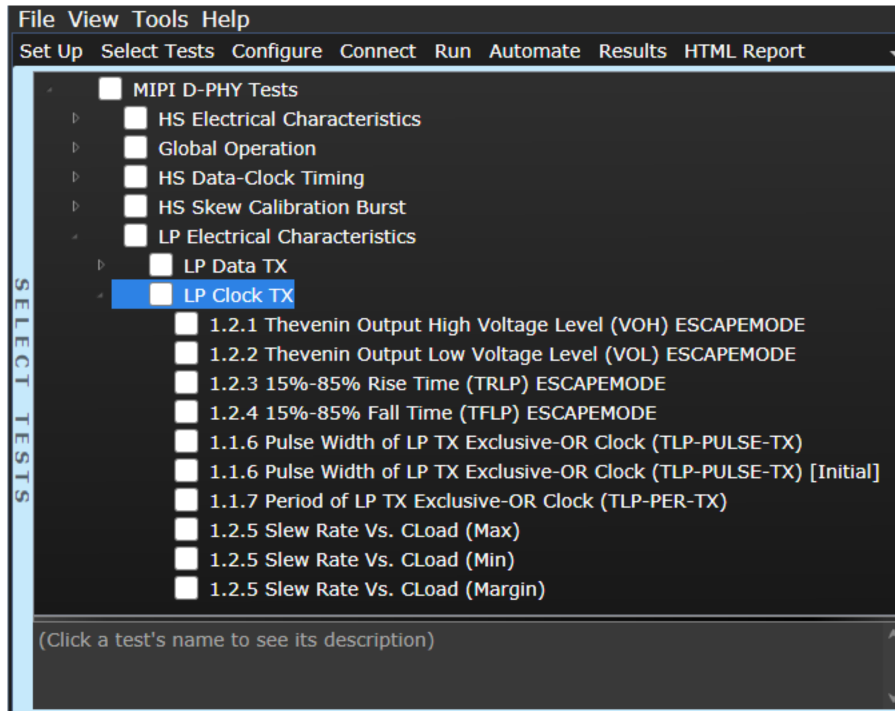


Figure 108 Selecting Low Power Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app’s task flow to set up the configuration options, run the tests and view the tests results.

Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation

For information about this test, refer to "Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation".

Test References

See Section 9.1.2 Table 22 in the D-PHY Specification v2.0.

Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation

For information about this test, refer to "Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation".

Test References

See Section 9.1.2 Table 22 in the D-PHY Specification v2.0.

Test 1.2.3 LP TX 15%-85% Rise Time Level (T_{RLP}) Method of Implementation

For information about this test, refer to "Test 1.2.3 LP TX 15%-85% Rise Time Level (T_{RLP}) Method of Implementation".

Test References

See Section 9.1.2 Table 23 in the D-PHY Specification v2.0.

Test 1.2.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation

For information about this test, refer to "Test 1.2.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation".

Test References

See Section 9.1.2 Table 23 in the D-PHY Specification v2.0.

Test 1.2.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation

For information about this test, refer to "Test 1.2.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation".

Test References

See Section 9.1.2 Table 23 in the D-PHY Specification v2.0.

Part II
Global Operation

KEYSIGHT
TECHNOLOGIES

33 MIPI D-PHY 2.0 & 2.1 Data Transmitter (Data TX) Global Operation Tests

Probing for Data TX Global Operation Tests / 412
Test 1.3.1 HS Entry: Data T_{LPX} Method of Implementation / 414
Test 1.3.2 HS Entry: Data TX $T_{HS-PREPARE}$ Method of Implementation / 414
Test 1.3.3 HS Entry: Data TX $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ Method of Implementation / 414
Test 1.3.13 HS Exit: Data TX $T_{HS-TRAIL}$ Method of Implementation / 414
Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{REOT}) Method of Implementation / 414
Test 1.3.15 HS Exit: Data TX T_{EOT} Method of Implementation / 415
Test 1.3.16 HS Exit: Data TX $T_{HS-EXIT}$ Method of Implementation / 415

This section provides the Methods of Implementation (MOIs) for the Data Transmitter (Data TX) Global Operation tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 2.0 and 2.1 Data TX Global Operation tests are similar to the MIPI D-PHY 1.2 Data TX Global Operation tests. Hence, all the tests share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.2 tests. For details, refer to “MIPI D-PHY 1.2 Data Transmitter (Data TX) Global Operation Tests”.

The current chapter lists the references from the MIPI D-PHY 2.0 specification.

KEYSIGHT
TECHNOLOGIES

Probing for Data TX Global Operation Tests

When performing the Data TX tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the Data TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test Application for the exact number of probe connections.

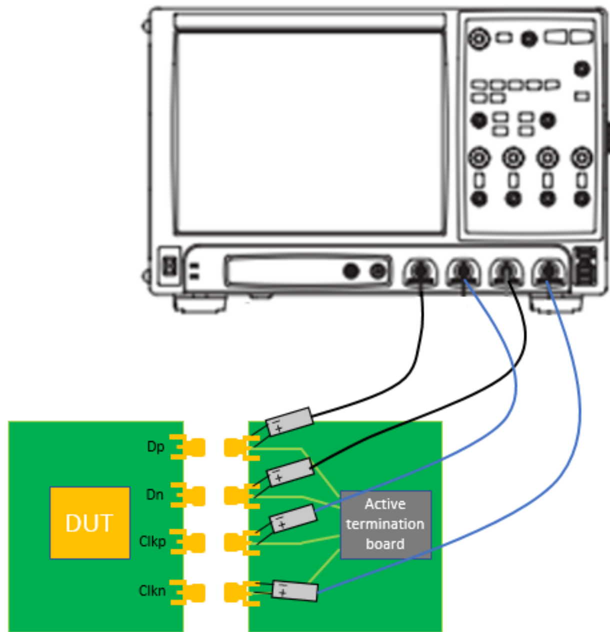


Figure 109 Probing for Data TX Global Operation Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 109 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

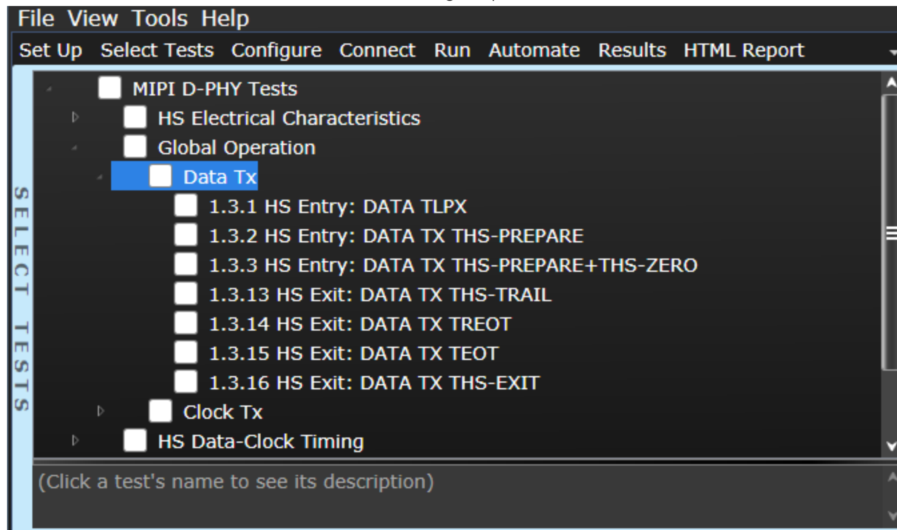


Figure 110 Selecting Data TX Global Operation Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.3.1 HS Entry: Data T_{LPX} Method of Implementation

For information about this test, refer to "Test 1.3.1 HS Entry: Data T_{LPX} Method of Implementation".

Test References

See Section 6.9 Table 14 in the D-PHY Specification v2.0.

Test 1.3.2 HS Entry: Data TX $T_{HS-PREPARE}$ Method of Implementation

For information about this test, refer to "Test 1.3.2 HS Entry: Data TX $T_{HS-PREPARE}$ Method of Implementation".

Test References

See Section 6.9 Table 14 in the D-PHY Specification v2.0.

Test 1.3.3 HS Entry: Data TX $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ Method of Implementation

For information about this test, refer to "Test 1.3.3 HS Entry: Data TX $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ Method of Implementation".

Test References

See Section 6.9 Table 14 in the D-PHY Specification v2.0.

Test 1.3.13 HS Exit: Data TX $T_{HS-TRAIL}$ Method of Implementation

For information about this test, refer to "Test 1.3.13 HS Exit: Data TX $T_{HS-TRAIL}$ Method of Implementation".

Test References

See Section 6.9 Table 14 in the D-PHY Specification v2.0.

Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{REOT}) Method of Implementation

For information about this test, refer to "Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{REOT}) Method of Implementation".

Test References

See Section 9.1.2 Table 23 in the D-PHY Specification v2.0.

Test 1.3.15 HS Exit: Data TX T_{EOT} Method of Implementation

For information about this test, refer to “Test 1.3.15 HS Exit: Data TX T_{EOT} Method of Implementation”.

Test References

See Section 6.9 Table 14 in the D-PHY Specification v2.0.

Test 1.3.16 HS Exit: Data TX $T_{HS-EXIT}$ Method of Implementation

For information about this test, refer to “Test 1.3.16 HS Exit: Data TX $T_{HS-EXIT}$ Method of Implementation”.

Test References

See Section 6.9 Table 14 in the D-PHY Specification v2.0.

34 MIPI D-PHY 2.0 & 2.1 Clock Transmitter (Clock TX) Global Operation Tests

Probing for Clock TX Global Operation Tests / 418
Test 1.4.1 HS Entry: CLK TX T_{LPX} Method of Implementation / 420
Test 1.4.2 HS Entry: CLK TX $T_{CLK-PREPARE}$ Method of Implementation / 420
Test 1.4.3 HS Entry: CLK TX $T_{CLK-PREPARE}$+$T_{CLK-ZERO}$ Method of Implementation / 420
Test 1.5.1 HS Entry: CLK TX $T_{CLK-PRE}$ Method of Implementation / 420
Test 1.5.2 HS Exit: CLK TX $T_{CLK-POST}$ Method of Implementation / 420
Test 1.4.13 HS Exit: CLK TX $T_{CLK-TRAIL}$ Method of Implementation / 420
Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{REOT}) Method of Implementation / 421
Test 1.4.15 HS Exit: CLK TX T_{EOT} Method of Implementation / 421
Test 1.4.16 HS Exit: CLK TX $T_{HS-EXIT}$ Method of Implementation / 421

This section provides the Methods of Implementation (MOIs) for the Clock Transmitter (Clock TX) Global Operation tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 2.0 and 2.1 Clock TX Global Operation tests are similar to the MIPI D-PHY 1.2 Clock TX Global Operation tests. Hence, all the tests share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.2 tests. For details, refer to "MIPI D-PHY 1.2 Clock Transmitter (Clock TX) Global Operation Tests".

The current chapter lists the references from the MIPI D-PHY 2.0 specification.

KEYSIGHT TECHNOLOGIES

Probing for Clock TX Global Operation Tests

When performing the Clock TX tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the Clock TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test Application for the exact number of probe connections.

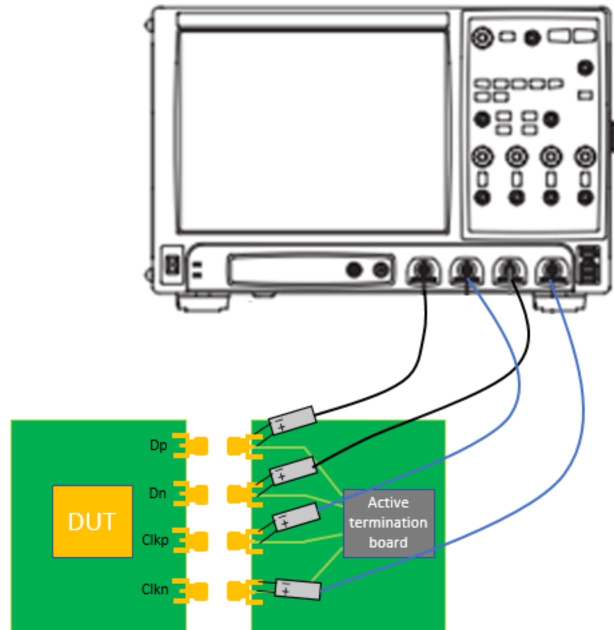


Figure 111 Probing for Clock TX Global Operation Tests

You can identify the channels used for each signal in the Configuration tab of the MIPI D-PHY Test Application. (The channels shown in Figure 111 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, Device ID and User Comments.
4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

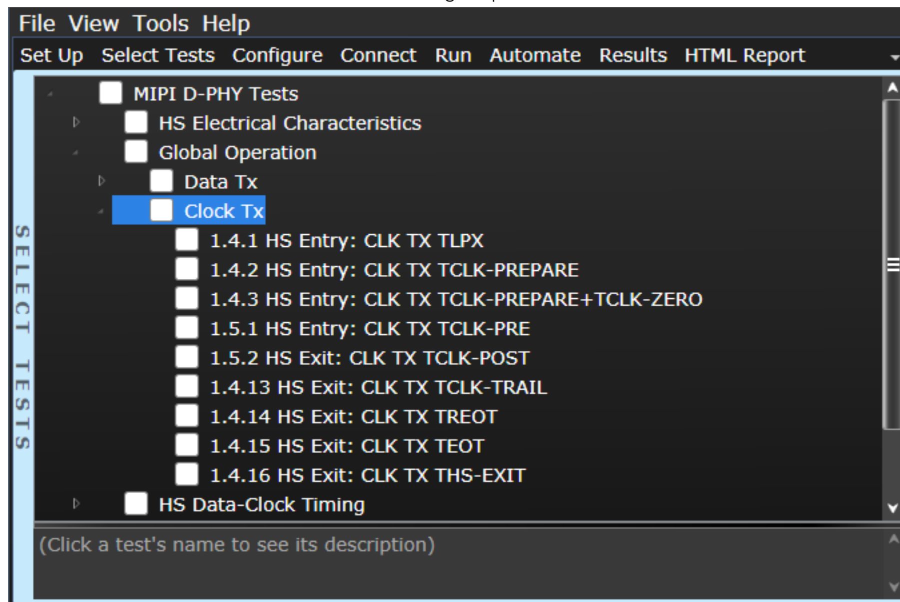


Figure 112 Selecting Clock TX Global Operation Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.4.1 HS Entry: CLK TX T_{LPX} Method of Implementation

For information about this test, refer to "Test 1.4.1 HS Entry: CLK TX T_{LPX} Method of Implementation".

Test References

See Section 6.9 Table 14 in the D-PHY Specification v2.0.

Test 1.4.2 HS Entry: CLK TX $T_{CLK-PREPARE}$ Method of Implementation

For information about this test, refer to "Test 1.4.2 HS Entry: CLK TX $T_{CLK-PREPARE}$ Method of Implementation".

Test References

See Section 6.9 Table 14 in the D-PHY Specification v2.0.

Test 1.4.3 HS Entry: CLK TX $T_{CLK-PREPARE}$+$T_{CLK-ZERO}$ Method of Implementation

For information about this test, refer to "Test 1.4.3 HS Entry: CLK TX $T_{CLK-PREPARE}$+$T_{CLK-ZERO}$ Method of Implementation".

Test References

See Section 6.9 Table 14 in the D-PHY Specification v2.0.

Test 1.5.1 HS Entry: CLK TX $T_{CLK-PRE}$ Method of Implementation

For information about this test, refer to "Test 1.5.1 HS Entry: CLK TX $T_{CLK-PRE}$ Method of Implementation".

Test References

See Section 6.9 Table 14 in the D-PHY Specification v2.0.

Test 1.5.2 HS Exit: CLK TX $T_{CLK-POST}$ Method of Implementation

For information about this test, refer to "Test 1.5.2 HS Exit: CLK TX $T_{CLK-POST}$ Method of Implementation".

Test References

See Section 6.9 Table 14 in the D-PHY Specification v2.0.

Test 1.4.13 HS Exit: CLK TX $T_{CLK-TRAIL}$ Method of Implementation

For information about this test, refer to "Test 1.4.13 HS Exit: CLK TX $T_{CLK-TRAIL}$ Method of Implementation".

Test References

See Section 6.9 Table 14 in the D-PHY Specification v2.0.

Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{REOT}) Method of Implementation

For information about this test, refer to "Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{REOT}) Method of Implementation".

Test References

See Section 9.1.2 Table 23 in the D-PHY Specification v2.0.

Test 1.4.15 HS Exit: CLK TX T_{EOT} Method of Implementation

For information about this test, refer to "Test 1.4.15 HS Exit: CLK TX T_{EOT} Method of Implementation".

Test References

See Section 6.9 Table 14 in the D-PHY Specification v2.0.

Test 1.4.16 HS Exit: CLK TX $T_{HS-EXIT}$ Method of Implementation

For information about this test, refer to "Test 1.4.16 HS Exit: CLK TX $T_{HS-EXIT}$ Method of Implementation".

Test References

See Section 6.9 Table 14 in the D-PHY Specification v2.0.

Part III HS Data-Clock Timing & HS Skew Calibration Burst

KEYSIGHT TECHNOLOGIES

35 MIPI D-PHY 2.0 & 2.1 High Speed (HS) Data-Clock Timing Tests

Probing for High Speed Data-Clock Timing Tests / 426
Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation / 428
Test 1.5.4 Data-to-Clock Skew ($T_{SKEW(TX)}$) Method of Implementation / 428

This section provides the Methods of Implementation (MOIs) for the High Speed (HS) Data-Clock Timing tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 2.0 and 2.1 HS Data Clock Timing tests are similar to the MIPI D-PHY 1.2 HS Data Clock Timing tests. Hence, all the tests share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.2 tests. For details, refer to "MIPI D-PHY 1.2 High Speed (HS) Data-Clock Timing Tests".

The current chapter lists the references from the MIPI D-PHY 2.0 specification.

KEYSIGHT TECHNOLOGIES

Probing for High Speed Data-Clock Timing Tests

When performing the HS Data-Clock Timing tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the HS Data-Clock Timing tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

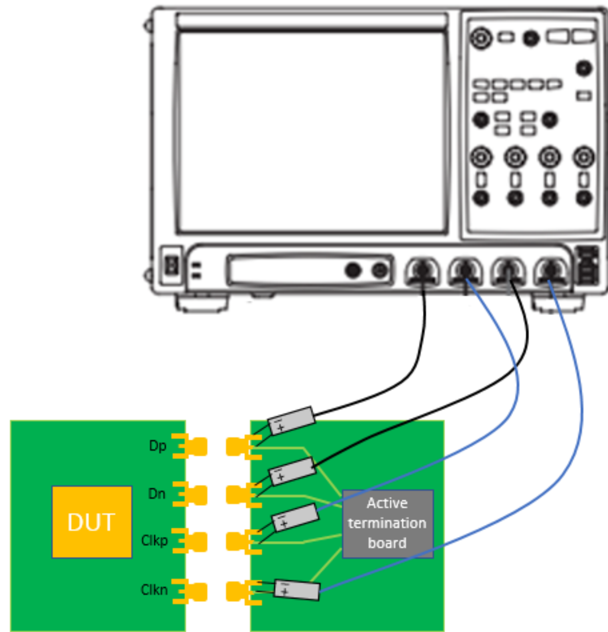


Figure 113 Probing for HS Data-Clock Timing Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 113 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

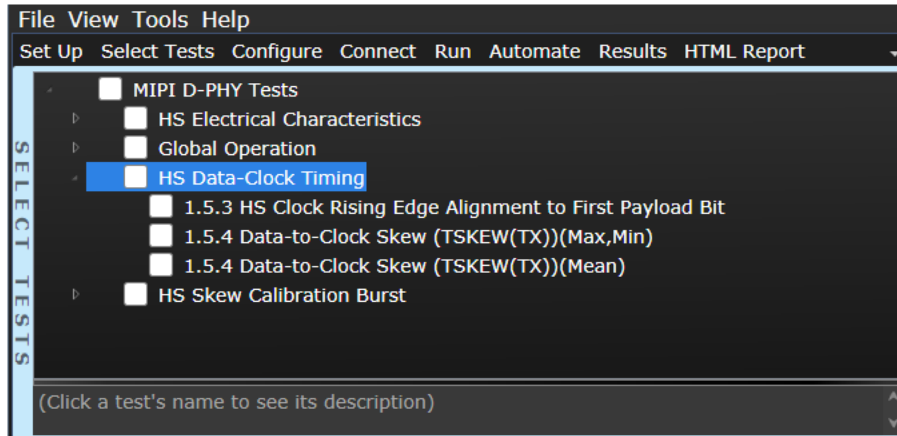


Figure 114 Selecting HS Data-Clock Timing Tests

5 Follow the MIPI D-PHY Test app’s task flow to set up the configuration options, run the tests and view the tests results.

Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation

For information about this test, refer to "Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation".

Test References

See Section 10.2 in the D-PHY Specification v2.0.

Test 1.5.4 Data-to-Clock Skew ($T_{SKEW(TX)}$) Method of Implementation

This test is similar to the corresponding MIPI D-PHY 1.0 and 1.2 tests. This section describes the procedure applicable to MIPI D-PHY 2.0 & 2.1 only. For details of the corresponding MIPI D-PHY 1.0 test, refer to "Test 1.5.4 Data-to-Clock Skew ($T_{SKEW(TX)}$) Method of Implementation" and for the MIPI D-PHY 1.2 test, refer to "Test 1.5.4 Data-to-Clock Skew ($T_{SKEW(TX)}$) Method of Implementation". The procedure for Test ID#9131 is the same for all MIPI D-PHY specifications.

Measurement Algorithm using Test ID 913

NOTE Use the Test ID# 913 to remotely access the test.

1 This test requires the following prerequisite tests:

   a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)

   Measure the minimum, maximum and average values of the Unit Interval for the differential clock waveform and the test results are stored.

2 Dp, Dn, Clkp and Clkn waveforms are captured.

3 Construct the differential clock waveform using the following equation:

$$DiffClock = Clkp-Clkn$$

4 Construct the differential data waveform by using the following equation:

$$DiffData = Dp-Dn$$

5 Using the DiffClock's rising and falling edges, fold the DiffData to form a data eye.

6 Use the **Histogram** feature to find out the furthest edges on the left of the DiffData left crossing and use it to calculate the T_{Skew} (max).

7 Use the **Histogram** feature to find out the nearest edges on the left of the DiffData left crossing and use it to calculate the T_{Skew} (min).

8 Use the **Histogram** feature to find out the mean of the DiffData left crossing and use it to calculate the T_{Skew} (mean).

9 Calculate T_{Skew} values (max/min) in units of seconds and in units of UI using the following equation:

$$T_{Skew(TX)} \text{ (in seconds)} = (T_{Skew} - T_{Center}) - MeanSkewRef$$

$$T_{Skew(TX)} \text{ (in UI)} = T_{Skew}/MeanUI$$

NOTE MeanSkewRef = [0.5 * MeanUI obtained from the prerequisite test]

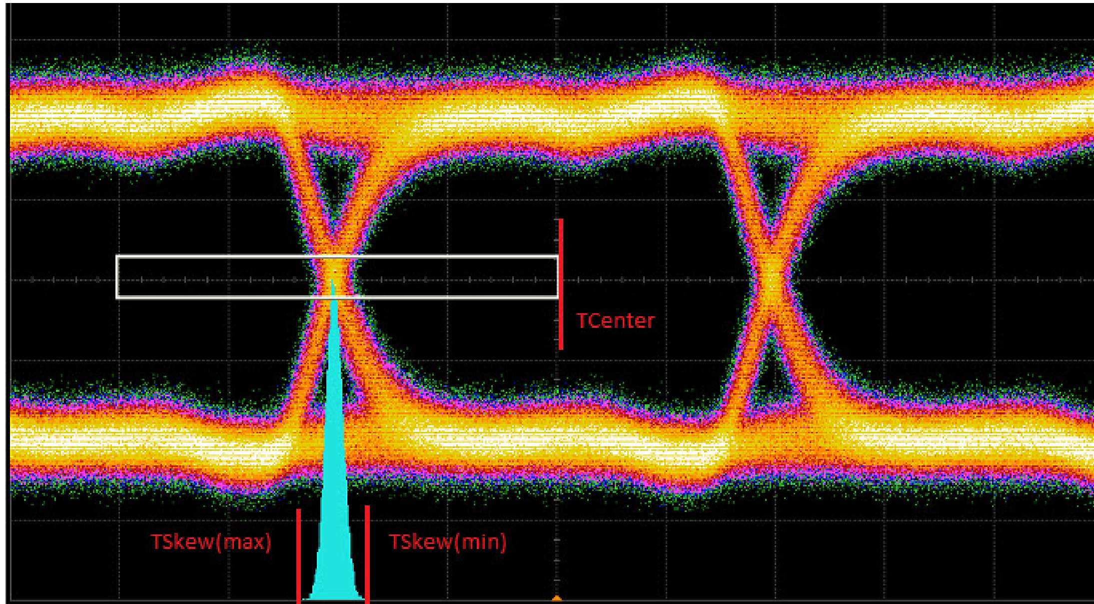


Figure 115 Data Eye

10 Calculate T_{Skew} (mean) in units of UI using the following equation:

$$T_{Skew(TX)} \text{ (in UI)} = T_{Skew}/\text{MeanUI}$$

11 The T_{Skew} (worst) is determined based on the T_{Skew} (max) and T_{Skew} (min) values with reference to the compliance test limit.

12 Compare the T_{Skew} (worst) value with the conformance test limits.

Test References

See Section 10.2.1.2 Table 31 in the D-PHY Specification v2.0.

36 MIPI D-PHY 2.0 & 2.1 High Speed (HS) Skew Calibration Burst Tests

Probing for High Speed Skew Calibration Burst Tests / 432
Test 1.5.5 Initial HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL) Method of Implementation / 434
Test 1.5.6 Periodic HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL) Method of Implementation / 434

This section provides the Methods of Implementation (MOIs) for the High Speed (HS) Skew Calibration Burst tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

MIPI D-PHY 2.0 and 2.1 HS Skew Calibration Burst tests are similar to the MIPI D-PHY 1.2 HS Skew Calibration Burst tests. Hence, all the tests share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.2 tests. For details, refer to "MIPI D-PHY 1.2 High Speed (HS) Skew Calibration Burst Tests".

The current chapter lists the references from the MIPI D-PHY 2.0 specification.

KEYSIGHT TECHNOLOGIES

Probing for High Speed Skew Calibration Burst Tests

When performing the HS Skew Calibration Burst tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the HS Skew Calibration Burst tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

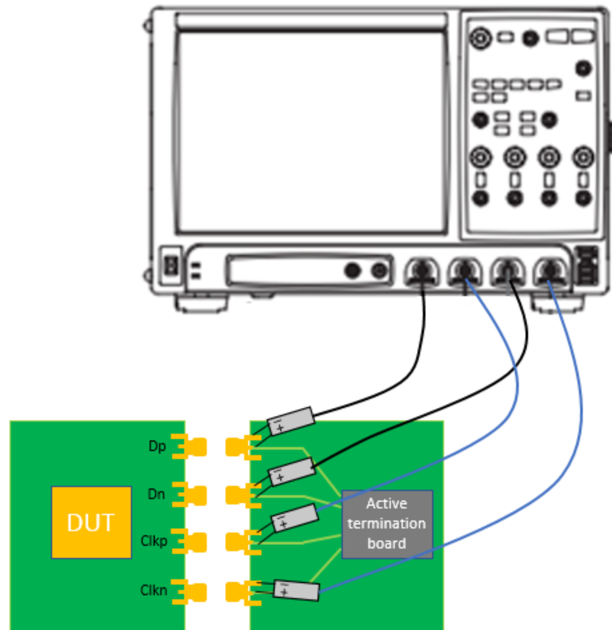


Figure 116 Probing for HS Skew Calibration Burst Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 116 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

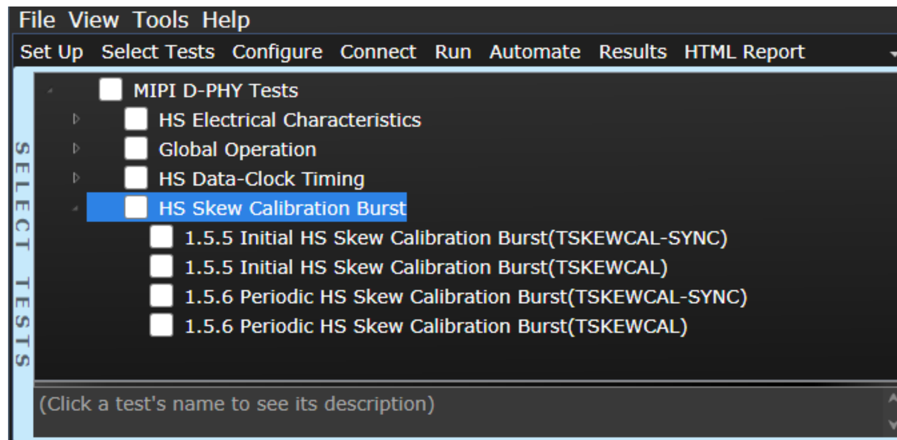


Figure 117 Selecting HS Skew Calibration Burst Tests

5 Follow the MIPI D-PHY Test app’s task flow to set up the configuration options, run the tests and view the tests results.

Test 1.5.5 Initial HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL) Method of Implementation

For information about this test, refer to "Test 1.5.5 Initial HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL) Method of Implementation".

Test References

See Section 6.12 Table 18 in the D-PHY Specification v2.0.

Test 1.5.6 Periodic HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL) Method of Implementation

For information about this test, refer to "Test 1.5.6 Periodic HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL) Method of Implementation".

Test References

See Section 6.12 Table 18 in the D-PHY Specification v2.0.

Part IV
HS Spread Spectrum Clocking

KEYSIGHT
TECHNOLOGIES

37 MIPI D-PHY 2.0 & 2.1High Speed (HS) Data Spread Spectrum Clocking Tests

Probing for High Speed Data Spread Spectrum Clocking Tests / 438
Test HS Data SSC Modulation Rate [Continuous Data] (Informative) Method of Implementation / 440
Test HS Data SSC Deviation [Continuous Data] (Informative) Method of Implementation / 442
Test HS Data SSC df/dt [Continuous Data] (Informative) Method of Implementation / 443

This section provides the Methods of Implementation (MOIs) for the High Speed (HS) Data Spread Spectrum Clocking tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

Probing for High Speed Data Spread Spectrum Clocking Tests

When performing the HS Data Spread Spectrum Clocking tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the HS Data Spread Spectrum Clocking tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

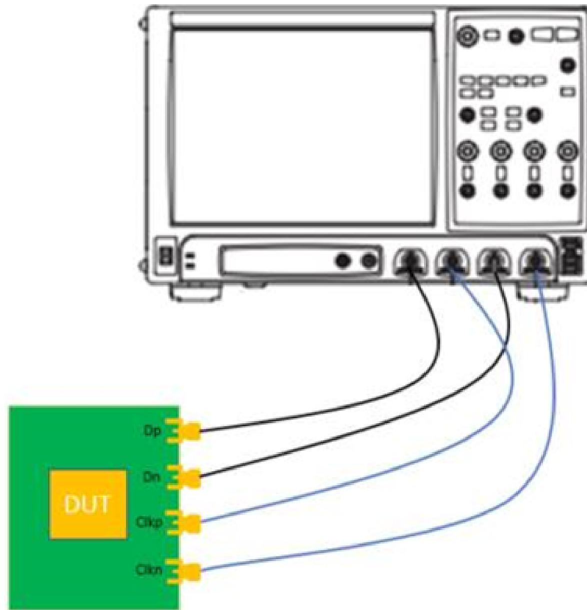


Figure 118 Probing for HS Data Spread Spectrum Clocking Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 118 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

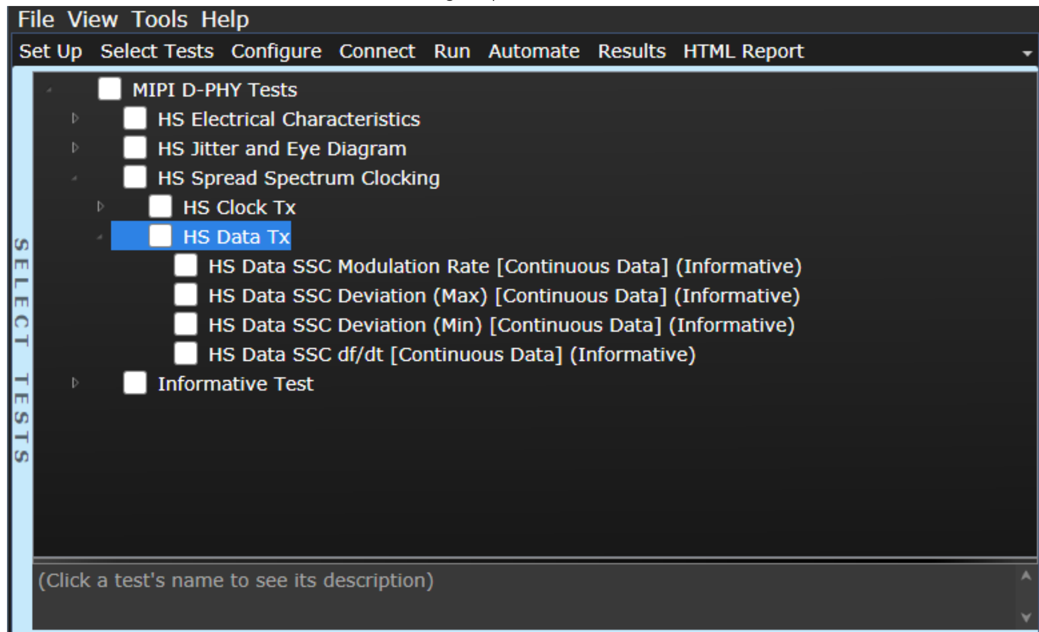


Figure 119 Selecting HS Data Spread Spectrum Clocking Tests

5 Follow the MIPI D-PHY Test app’s task flow to set up the configuration options, run the tests and view the tests results.

Test HS Data SSC Modulation Rate [Continuous Data] (Informative) Method of Implementation

This test verifies that the SSC Modulation Rate is within the specification.

PASS Condition

The measured SSC Modulation Rate value must be within the conformance limit as specified in the specification mentioned under the References section.

Test Availability Condition

Table 90 Test Availability Condition for HS Data SSC Modulation Rate Test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
200200	>2.5 Gbps	100 ohm	Enabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Enabled	Direct Connect

Measurement Algorithm using Test ID 200200

NOTE Use the Test ID# 200200 to remotely access the test.

1 Trigger the scope to acquire Dp and Dn.
2 Construct differential data of Dp and Dn using the following equation:

DataDiff = Dp - Dn

3 Set Unit Interval measurement on DataDiff to ON.
4 Enable the measurement trend for the unit interval measurement. The measurement trend will be used for processing.
5 Using the MATLAB script, apply a 1.98MHz (33 kHz * 60 = 1.98 MHz), 2nd-order Butterworth low pass test filter to the measurement trend data and inverse the filtered data to generate the SSC profile.
6 Calculate the frequency from all SSC profiles and store the mean value as SSC Modulation Rate value.
7 Measure the maximum-profile peak value and minimum-profile peak value for all SSC profiles and store the values as Bit_Rate_Max and Bit_Rate_Min, respectively.
8 Calculate the SSC modulation deviation using the following equations:

SSC Deviation(Min) = (Bit_Rate_Max – Bit_Rate_Nominal)/ (Bit_Rate_Nominal) * 1E6

SSC Deviation(Max) = (Bit_Rate_Min – Bit_Rate_Nominal)/ (Bit_Rate_Nominal) * 1E6

9 Using the Matlab script, post-process the measurement trend data to create the DFDT profile with a timing interval of 0.5µs.
10 Measure the maximum and minimum df/dt values and store df/dt values as SSC df/dt values.
11 Report the measurement results for SSC Modulation Rate.
12 Compare the measured SSC modulation rate value to the compliance test limits.

Test References

See Section 10.2.2, Table 39 in the D-PHY Specification v2.0 & v2.1.

Test HS Data SSC Deviation [Continuous Data] (Informative) Method of Implementation

This test verifies that the SSC Deviation is within the specification.

PASS Condition

The measured SSC Deviation values must be within the conformance limit as specified in the specification mentioned under the References section.

Test Availability Condition

Table 91 Test Availability Condition for HS Data SSC Deviation Test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
200201	> 2.5 Gbps	100 ohm	Enabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Enabled	Direct Connect
200202	> 2.5 Gbps	100 ohm	Enabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Enabled	Direct Connect

Measurement Algorithm using Test IDs 200201 and 200202

NOTE Use the Test IDs# 200201 and 200202 to remotely access the test.

1. This test requires the following pre-requisite test.
   HS Data SSC Modulation Rate [Continuous Data] (Informative) (Test ID: 200200): Actual SSC Deviation(Max) and SSC Deviation(Min) measurements are performed and test results are stored.
2. Report the measurement results:
   SSC Deviation(Max)
   SSC Deviation(Min)
3. Compare the measured SSC Deviation(Max) and SSC Deviation(Min) values with the compliance test limit.

Test References

See Section 10.2.2, Table 39 in the D-PHY Specification v2.0 & v2.1.

Test HS Data SSC df/dt [Continuous Data] (Informative) Method of Implementation

This test verifies that the SSC df/dt is within the specification.

PASS Condition

The measured SSC df/dt value must be within the conformance limit as specified in the specification mentioned under the References section.

Test Availability Condition

Table 92 Test Availability Condition for HS Data SSC df/dt Test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
200203	> 2.5 Gbps	100 ohm	Enabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Enabled	Direct Connect

Measurement Algorithm using Test ID 200203

NOTE Use the Test ID# 200203 to remotely access the test.

1 This test requires the following pre-requisite test.
HS Data SSC Modulation Rate [Continuous Data] (Informative) (Test ID: 200200): Actual SSC df/dt measurement is performed and test result is stored.
2 Report the measurement results:
SSC df/dt
3 Compare the measured SSC df/dt value with the compliance test limit.

Test References

See Section 10.2.2, Table 39 in the D-PHY Specification v2.0 & v2.1.

38 MIPI D-PHY 2.0 & 2.1 High Speed (HS) Clock Spread Spectrum Clocking Tests

Probing for High Speed Clock Spread Spectrum Clocking Tests / 446
Test 1.4.19 HS Clock SSC Modulation Rate [Continuous Clock] Method of Implementation / 448
Test 1.4.19 HS Clock SSC Deviation [Continuous Clock] Method of Implementation / 449
Test 1.4.19 HS Clock SSC df/dt [Continuous Clock] Method of Implementation / 450

This section provides the Methods of Implementation (MOIs) for the High Speed (HS) Clock Spread Spectrum Clocking tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

KEYSIGHT TECHNOLOGIES

Probing for High Speed Clock Spread Spectrum Clocking Tests

When performing the HS Clock Spread Spectrum Clocking tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the HS Clock Spread Spectrum Clocking tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

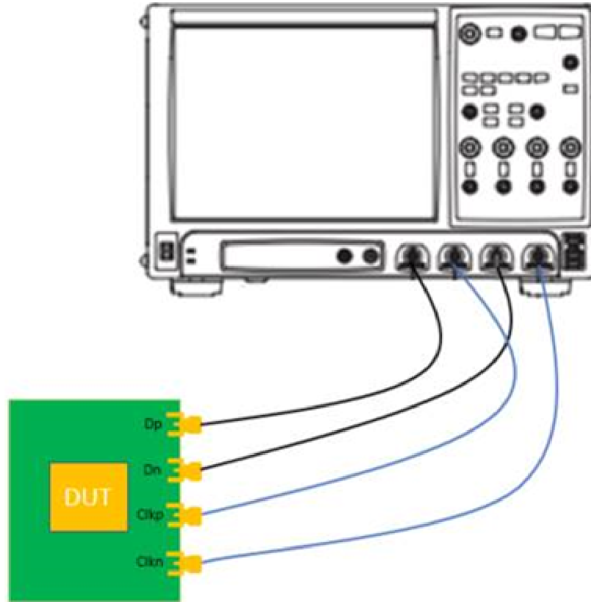


Figure 120 Probing for HS Clock Spread Spectrum Clocking Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 120 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test app, click the **Set Up** tab.
3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

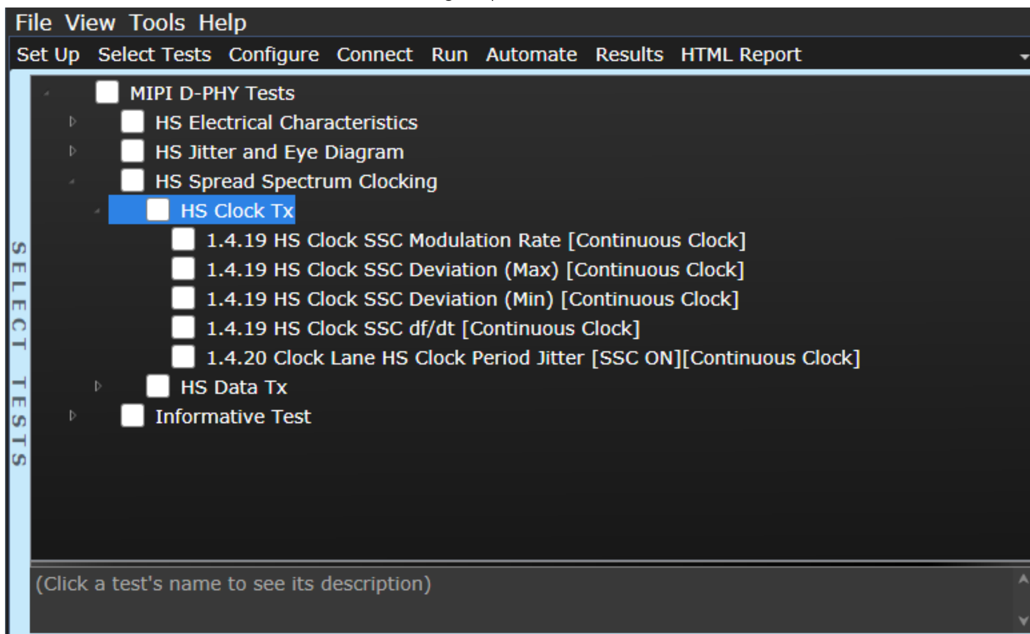


Figure 121 Selecting HS Clock Spread Spectrum Clocking Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.4.19 HS Clock SSC Modulation Rate [Continuous Clock] Method of Implementation

This test verifies that the SSC Modulation Rate is within the specification.

PASS Condition

The measured SSC Modulation Rate value must be within the conformance limit as specified in the specification mentioned under the Test References section.

Test Availability Condition

Table 93 Test Availability Condition for HS Clock SSC Modulation Rate Test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1200200	>2.5 Gbps	100 ohm	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Direct Connect

Measurement Algorithm using Test ID 1200200

NOTE Use the Test ID# 1200200 to remotely access the test.

1 Trigger the scope to acquire Clkp and Clkn.
2 Construct differential data of Clkp and Clkn using the following equation:

ClockDiff = Clkp - Clkn

3 Set Unit Interval measurement on ClockDiff to ON.
4 Enable the measurement trend for the unit interval measurement. The measurement trend will be used for processing.
5 Using the MATLAB script, apply a 1.98MHz (33 kHz * 60 = 1.98 MHz), 2nd-order Butterworth low pass test filter to the measurement trend data and inverse the filtered data to generate the SSC profile.
6 Calculate the mean frequency from all SSC profiles and store the mean value as SSC Modulation Rate value.
7 Measure the maximum-profile peak value and minimum-profile peak value for all SSC profiles and store the values as Bit_Rate_Max and Bit_Rate_Min, respectively.
8 Calculate the SSC modulation deviation using the following equations:

SSC Deviation(Min) = (Bit_Rate_Max – Bit_Rate_Nominal)/ (Bit_Rate_Nominal) * 1E6

SSC Deviation(Max) = (Bit_Rate_Min – Bit_Rate_Nominal)/ (Bit_Rate_Nominal) * 1E6

9 Using the Matlab script, post-process the measurement trend data to create the DFDT profile with a timing interval of 0.5µs.
10 Measure the maximum and minimum df/dt values and store df/dt values as SSC df/dt values.
11 Report the measurement results for SSC Modulation Rate.
12 Compare the measured SSC modulation rate value to the compliance test limits.

Test References

See Section 10.2.2, Table 39 in the D-PHY Specification v2.0 & v2.1.

Test 1.4.19 HS Clock SSC Deviation [Continuous Clock] Method of Implementation

This test verifies that the SSC Deviation is within the specification.

PASS Condition

The measured SSC Deviation values shall be within the conformance limit as specified in the specification mentioned under the Test References section.

Test Availability Condition

Table 94 Test Availability Condition for HS Clock SSC Deviation Test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1200201	> 2.5 Gbps	100 ohm	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Direct Connect
1200202	> 2.5 Gbps	100 ohm	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Direct Connect

Measurement Algorithm using Test IDs 1200201 and 1200202

NOTE Use the Test IDs# 1200201 and 1200202 to remotely access the test.

1 This test requires the following pre-requisite test.
HS Clock SSC Modulation Rate [Continuous Clock] (Test ID: 1200200): Actual SSC Deviation(Max) and SSC Deviation(Min) measurements are performed and test results are stored.
2 Report the measurement results for SSC Deviation(Max) and SSC Deviation(Min).
3 Compare the measured SSC Deviation(Max) and SSC Deviation(Min) values with the compliance test limit.

Test References

See Section 10.2.2, Table 39 in the D-PHY Specification v2.0 & v2.1.

Test 1.4.19 HS Clock SSC df/dt [Continuous Clock] Method of Implementation

This test verifies that the SSC df/dt is within the specification.

PASS Condition

The measured SSC df/dt value must be within the conformance limit as specified in the specification mentioned under the Test References section.

Test Availability Condition

Table 95 Test Availability Condition for HS Clock SSC df/dt Test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
1200203	> 2.5 Gbps	100 ohm	Not Applicable	Enabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Direct Connect

Measurement Algorithm using Test ID 1200203

NOTE Use the Test ID# 1200203 to remotely access the test.

1. This test requires the following pre-requisite test.
   HS Clock SSC Modulation Rate [Continuous Clock] (Test ID: 1200200): Actual SSC df/dt measurement is performed and test result is stored.
2. Report the measurement results for SSC df/dt.
3. Compare the measured SSC df/dt value with the compliance test limit.

Test References

See Section 10.2.2, Table 39 in the D-PHY Specification v2.0 & v2.1.

Part V
HS Jitter & Eye

KEYSIGHT TECHNOLOGIES

39 MIPI D-PHY 2.0 & 2.1High Speed (HS) Jitter and Eye Diagram Tests

Probing for High Speed Jitter and Eye Diagram Tests / 454
Test HS Data to Clock Total Jitter [Continuous Data] Method of Implementation / 456
Test HS Data to Clock Deterministic Jitter [Continuous Data] Method of Implementation / 457
Test HS Data to Clock Random Jitter [Continuous Data] Method of Implementation / 458
Test 1.5.7 HS Clock Eye Diagram [Continuous Clock] Method of Implementation / 459
Test 1.5.7 HS Data Eye Diagram [Continuous Data] Method of Implementation / 460

This section provides the Methods of Implementation (MOIs) for the High Speed (HS) Jitter and Eye Diagram tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

KEYSIGHT TECHNOLOGIES

Probing for High Speed Jitter and Eye Diagram Tests

When performing the HS Jitter and Eye Diagram tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the HS Jitter and Eye Diagram tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

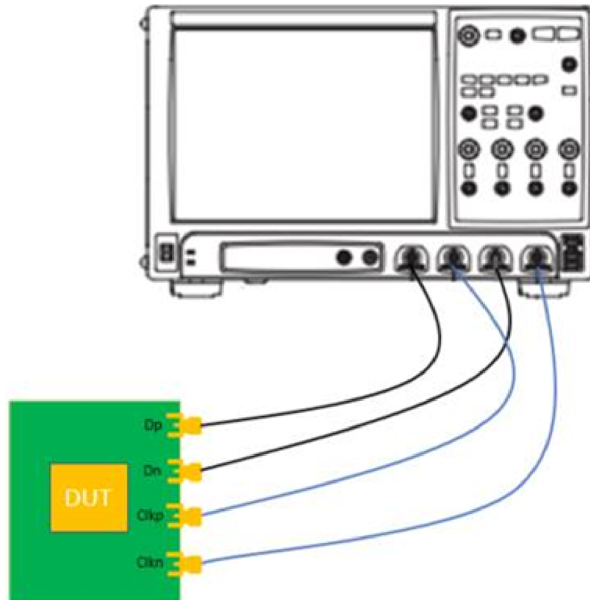


Figure 122 Probing for HS Jitter and Eye Diagram Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 122 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the MIPI D-PHY Test App, click the **Set Up** tab.
3 In the **Set Up** tab **> Device Information** section, enter the **High-Speed Data Rate** greater then 1.5 Gbps, for example, 1600 Mbps, and press **Enter**.
4 Select the **CTS** version as **v2.0 and v2.1**
5 Select the two check boxes: **Continuous Data** and **Continuous Clock**.
6 As jitter tests are informative, please select the **Show Informative Tests** check box to view them.

7 Click the **Select Tests** tab and select the **HS Jitter and Eye Diagram** tests that you want to run.

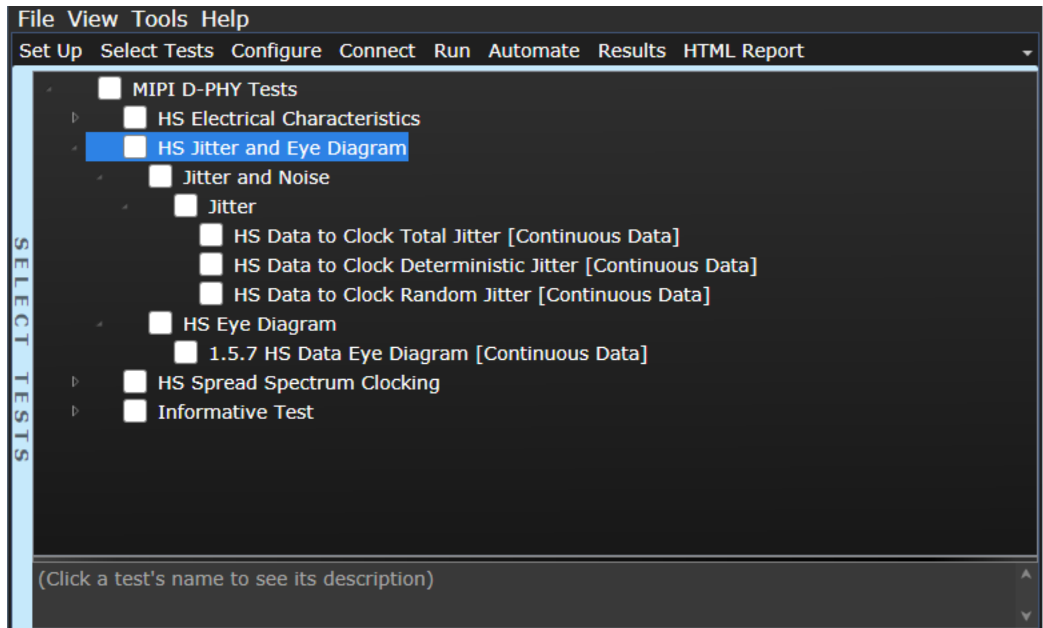


Figure 123 Selecting HS Jitter and Eye Diagram Tests

8 Set up the configuration options, run the tests, and view the tests results. You may see the online help for more elaborated steps on how to configure, run, and view the test results.

Test HS Data to Clock Total Jitter [Continuous Data] Method of Implementation

This test verifies that the HS Data to Clock Total Jitter is within the specification.

PASS Condition

The measured HS Data to Clock Total Jitter value must be within the conformance limit as specified in the specification mentioned under the References section.

Test Availability Condition

Table 96 Test Availability Condition for HS Data to Clock Total Jitter Test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
200110	>1.5 Gbps	100 ohm	Dependency on Continuous Clock setting	Enabled	Not Applicable	Not Applicable	Not Applicable	Applicable	Direct Connect

Measurement Algorithm using Test ID 200110

NOTE Use the Test ID# 200110 to remotely access the test. This test is applicable above 1.5 Gbps data rate, and it is an informative test.

1. Trigger the scope to acquire Dp, Dn, Clkp and Clkn.
2. Construct differential clock of Clkp and Clkn using the following equation:
   ClockDiff = Clkp-Clkn
3. Construct differential data of Dp and Dn using the following equation:
   DataDiff = Dp - Dn
4. Set up the clock recovery to use explicit clock method where the ClockDiff's rising and falling edges will be used to fold the DataDiff to form a data eye.
5. Measure the following measurement using the “EZJIT Complete” feature of the scope:
   Total Jitter (TJ)
   Deterministic Jitter (DJ)
   Random Jitter (RJ)
6. Report measurement result:
   Total Jitter
7. Compare the measured Total Jitter value with the compliance test limit.

Test References

See Section 10.2.1.3 Table 33 in the D-PHY Specification v2.0.

Test HS Data to Clock Deterministic Jitter [Continuous Data] Method of Implementation

This test verifies that the HS Data to Clock Deterministic Jitter is within the specification.

PASS Condition

The measured HS Data to Clock Deterministic Jitter value must be within the conformance limit as specified in the specification mentioned under the References section.

Test Availability Condition

Table 97 Test Availability Condition for HS Data to Clock Deterministic Jitter Test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
200111	> 1.5 Gbps	100 ohm	Dependency on Continuous Clock setting	Enabled	Not Applicable	Not Applicable	Not Applicable	Applicable	Direct Connect

Measurement Algorithm using Test ID 200111

NOTE Use the Test ID# 200111 to remotely access the test. This test is applicable above 1.5 Gbps data rate, and it is an informative test.

1. This test requires the following pre-requisite test(s).
   HS Data to Clock Total Jitter [Continuous Data]: Actual Deterministic Jitter measurement is performed and test result is stored.
2. Report the measurement result:
   Deterministic Jitter
3. Compare the measured Deterministic Jitter value with the compliance test limit.

Test References

See Section 10.2.1.3 Table 33 in the D-PHY Specification v2.0.

Test HS Data to Clock Random Jitter [Continuous Data] Method of Implementation

This test verifies that the HS Data to Clock Random Jitter is within the specification.

PASS Condition

The measured HS Data to Clock Random Jitter value must be within the conformance limit as specified in the specification mentioned under the References section.

Test Availability Condition

Table 98 Test Availability Condition for HS Data to Clock Random Jitter Test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
200112	> 1.5 Gbps	100 ohm	Dependency on Continuous Clock setting	Enabled	Not Applicable	Not Applicable	Not Applicable	Applicable	Direct Connect

Measurement Algorithm using Test ID 200112

NOTE Use the Test ID# 200112 to remotely access the test. This test is applicable above 1.5 Gbps data rate, and it is an informative test.

1 This test requires the following pre-requisite test(s).
HS Data to Clock Total Jitter [Continuous Data]: Actual Random Jitter measurement is performed and test result is stored.
2 Report the measurement result:
Random Jitter
3 Compare the measured Random Jitter value with the compliance test limit.

Test References

See Section 10.2.1.3 Table 33 in the D-PHY Specification v2.0.

Test 1.5.7 HS Clock Eye Diagram [Continuous Clock] Method of Implementation

This test verifies that the HS Clock Eye Diagram is within the specification.

PASS Condition

The generated eye diagram must not violate the mask specified in the specification mentioned under the Test References section.

Test Availability Condition

Table 99 Test Availability Condition for HS Clock Eye Diagram Test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
200100	> 1.5 Gbps	100 ohm	Dependency on Continuous Clock setting	Enabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Direct Connect

Measurement Algorithm using Test ID 1200100

NOTE Use the Test ID# 1200100 to remotely access the test. This test is applicable above 1.5 Gbps data rate.

1 Trigger the scope to acquire Clkp and Clkn.
2 Construct differential clock of Clkp and Clkn using the following equation:

ClockDiff = Clkp-Clkn

3 Embed the “Standard Channel” reference channel using the “InfiniiSim” function in the Oscilloscope for ClockDiff signal.
4 Set up the clock recovery to use explicit clock method where the ClockDiff’s rising and falling edges will be used to fold the clock signal to form a clock eye.
5 Using the histogram feature in the Oscilloscope, measure the right eye crossing position and left eye crossing position to determine the center of the eye diagram. Place mask on the center of eye diagram.
6 Acquire 3M UIs and run the mask testing feature in the Oscilloscope.
7 Check the mask violation result.
8 The mask violation result is used as the final test result for this test.

Test References

See Section 10.2.3, Table 40 in the D-PHY Specification v2.0 & v2.1.

Test 1.5.7 HS Data Eye Diagram [Continuous Data] Method of Implementation

This test verifies that the HS Data Eye Diagram is within the specification.

PASS Condition

The generated eye diagram must not violate the mask specified in the specification mentioned under the References section.

Test Availability Condition

Table 100 Test Availability Condition for HS Data Eye Diagram Test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
200100	> 1.5 Gbps	100 ohm	Dependency on Continuous Clock setting	Enabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Direct Connect

Measurement Algorithm using Test ID 200100

NOTE Use the Test ID# 200100 to remotely access the test. This test is applicable above 1.5 Gbps data rate.

1 Trigger the Oscilloscope to acquire Dp, Dn, Clkp and Clkn.

2 Construct differential clock of Clkp and Clkn using the following equation:

ClockDiff = Clkp-Clkn

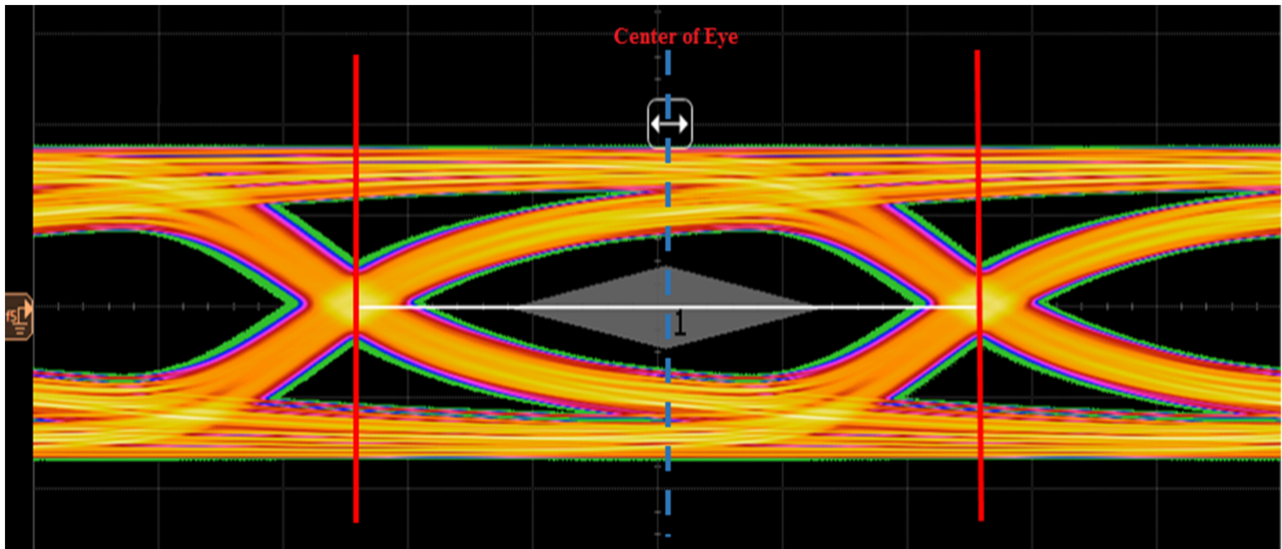
3 Construct differential data of Dp and Dn using the following equation:

DataDiff = Dp - Dn

4 Embed the “Standard Channel” reference channel using the “InfiniiSim” function in the Oscilloscope for ClockDiff and DataDiff signals.

5 Set up the clock recovery to use the Explicit Clock method where the ClockDiff’s rising and falling edges are used to fold the DataDiff to form a data eye.

6 Using the histogram feature in the Oscilloscope, measure the right eye crossing position and left eye crossing position to determine the center of the eye diagram. Place mask on the center of eye diagram.

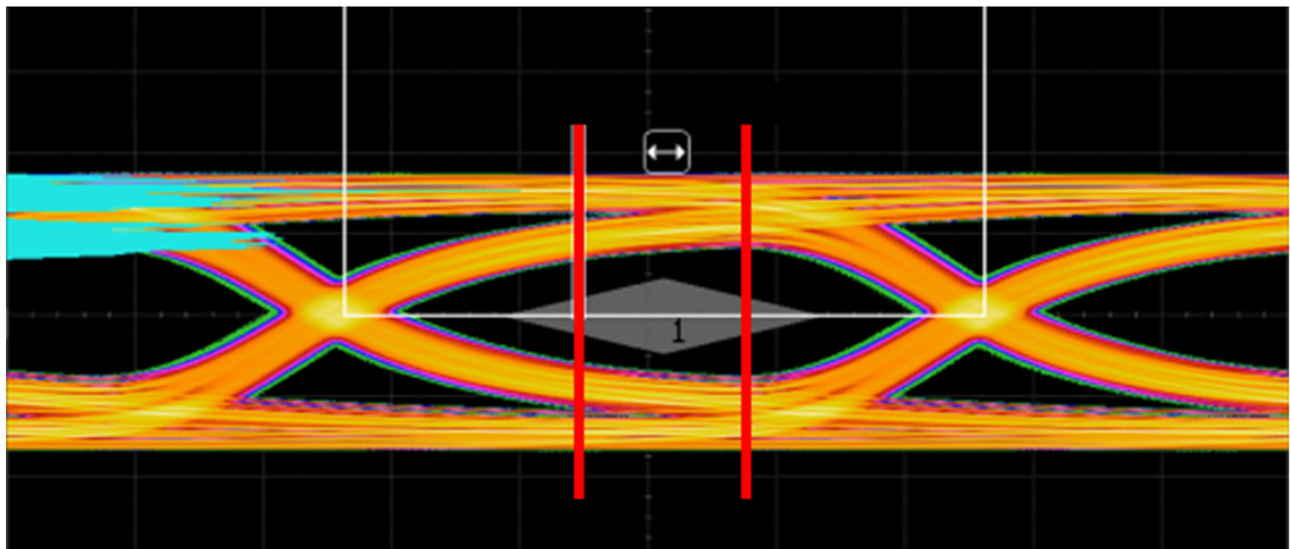


7 Acquire 3M UIs and run the mask testing feature in the Oscilloscope.

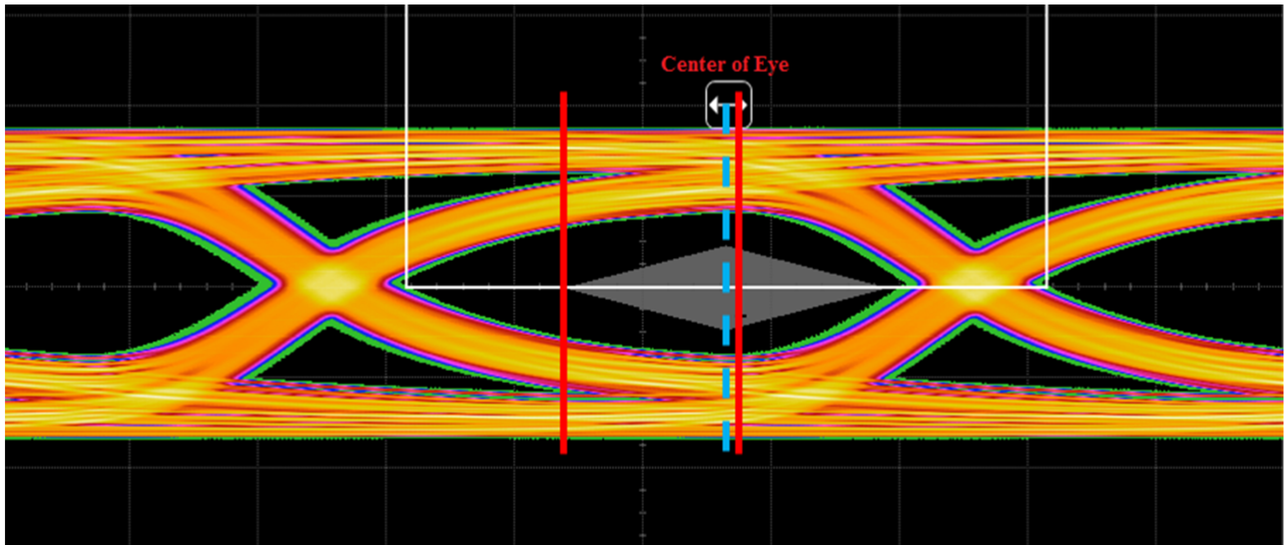
8 Check the mask violation result.

9 If mask violation occurs:

   a Use the histogram feature in the Oscilloscope to find the highest eye height location within the range value from “Mask Shift Horizontal Range (UI) [Eye Diagram]” configurable option. Use it as the center of eye diagram.



b Place mask on the center of eye diagram.



c Acquire 3M UIs and run the mask testing feature in the scope.

d Check the mask violation result.

10 The mask violation result is used as the final test result for this test.

Test References

See Section 10.2.3, Table 40 in the D-PHY Specification v2.0 & v2.1.

Part VI
Alt. Calibration Tests

KEYSIGHT
TECHNOLOGIES

40 MIPI D-PHY 2.0 & 2.1 Alternate Calibration Sequence Tests

Probing for Alternate Calibration Sequence Tests / 466
Test 1.5.8 Alternate Calibration Sequence [TALTCAL-SYNC] Method of Implementation / 468
Test 1.5.8 Alternate Calibration Sequence [TALTCAL] Method of Implementation / 470

This section provides the Methods of Implementation (MOIs) for the Alternate Calibration Sequence tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

Probing for Alternate Calibration Sequence Tests

When performing the Alternate Calibration Sequence tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the these tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

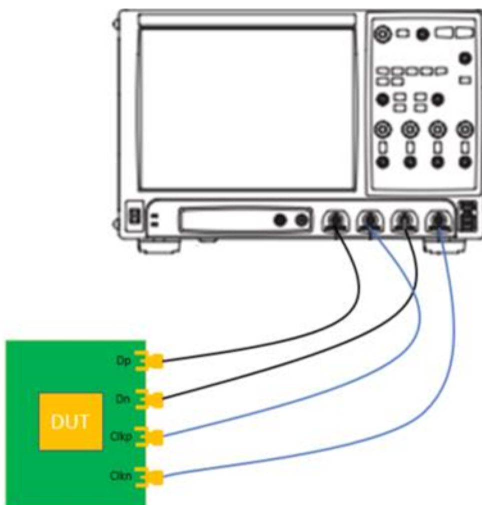


Figure 124 Probing for Alternate Calibration Sequence Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 124 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".

2 In the **Set Up** tab, select or configure the options that define the connected DUT's characteristics.

3 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

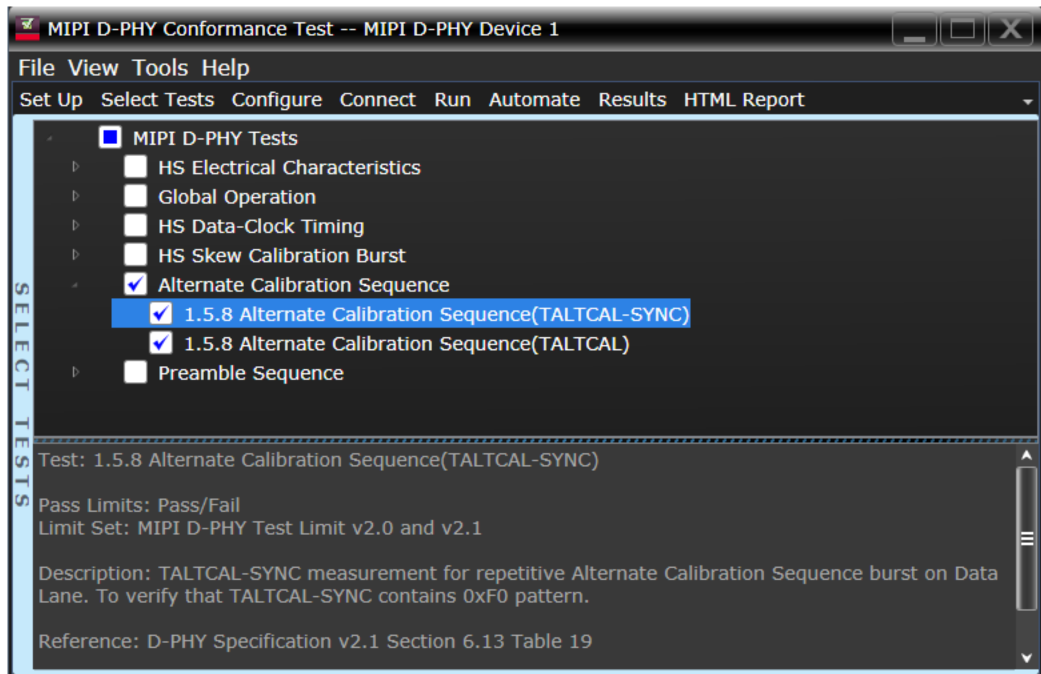


Figure 125 Selecting Alternate Calibration Sequence tests

4 Optionally, in the **Configure** tab, modify the configuration options that are needed for compliance.

5 Run the selected tests. Once tests are completed, the **Results** tab displays the test results.

Test 1.5.8 Alternate Calibration Sequence [TALTCAL-SYNC] Method of Implementation

This test verifies the TALTCAL-SYNC of the DUT is within the conformance limits.

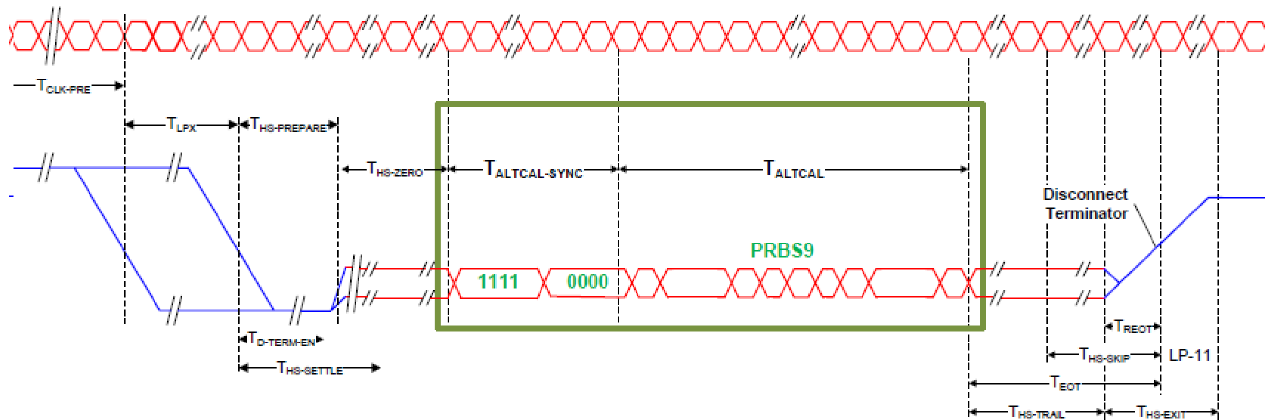


Figure 126 Alternate Calibration Sequence

PASS Condition

The measured TALTCAL-SYNC shall be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 101 Test Availability Condition for Alternate Calibration Sequence test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
200400	>2.5 Gbps	100 ohm	Dependency on Continuous Clock setting	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe) or Direct Connect

Measurement Algorithm using Test ID 200400

NOTE Use the Test ID# 200400 to remotely access the test.

This test supports Burst Clock & Burst Data signals and requires Repetitive Alternate Calibration Sequence.

1 Run the following test as a pre-requisite:

   a HS Clock Instantaneous (UIinst)(Max) (Test ID: 911)

   : The minimum, maximum and average Unit Interval of the differential clock waveform is measured and stored.

2 Trigger on Dp's falling edge in LP-01 at the SoT.

3 Construct differential data of Dp and Dn using the following equation:

DataDiff = Dp - Dn

4. Find the time when the first rising edge of the differential waveform crosses 0V after the LP-00 state. Mark this time as T1.
5. From the position marked as T1, find the time when the next falling edge crosses 0V. Mark this time as T2.
6. From the position marked as T2, find the time when the next rising edge crosses 0V. Mark this time as T3. Verify that the bit pattern from T1 to T3 is “11110000”.
7. From the position marked as T3, find the time when the last differential Data signal’s edge crosses 0V. Mark this time as T4.
8. Calculate TALTCAL-SYNC using the following equation:

   TALTCAL-SYNC = T3 - T1

9. Compare the measured TALTCAL-SYNC value with the compliance test limits.

Test References

See Section 6.13, Table 19 in the D-PHY Specification v2.1.

Test 1.5.8 Alternate Calibration Sequence [TALTCAL] Method of Implementation

This test verifies the TALTCAL of the DUT is within the conformance limits.

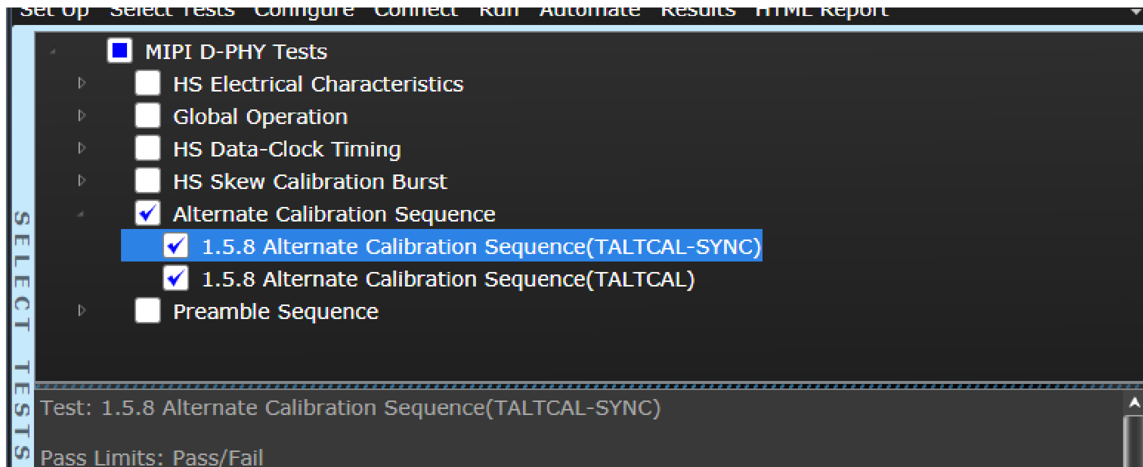


Figure 127 Alternate Calibration Sequence

PASS Condition

The measured TALTCAL shall be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 102 Test Availability Condition for Alternate Calibration Sequence test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
200401	>2.5 Gbps	100 ohm	Dependency on Continuous Clock setting	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe) or Direct Connect

Measurement Algorithm using Test ID 200401

NOTE

Use the Test ID# 200401 to remotely access the test.

This test supports Burst Clock & Burst Data signals and requires Repetitive Alternate Calibration Sequence.

1 The following test is run as a pre-requisite:

   a Alternate Calibration Sequence [TALTCAL-SYNC] (Test ID: 200400)

   : The positions T3 and T4 are measured.

2 Calculate TALTCAL using the following equation:

TALTCAL = T4 - T3

3 Compare the measured TALTCAL value with the compliance test limits.

Test References

See Section 6.13, Table 19 in the D-PHY Specification v2.1.

Part VII
Preamble Seq. Tests

KEYSIGHT
TECHNOLOGIES

41 MIPI D-PHY 2.0 & 2.1 Preamble Sequence Tests

Probing for Preamble Sequence Tests / 476
Test 1.5.9 Preamble Sequence [TPREAMBLE] Method of Implementation / 478
Test 1.5.9 Preamble Sequence [TEXTSYNC] Method of Implementation / 480

This section provides the Methods of Implementation (MOIs) for the Preamble Sequence tests using a Keysight Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

KEYSIGHT TECHNOLOGIES

Probing for Preamble Sequence Tests

When performing the Preamble Sequence tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the these tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

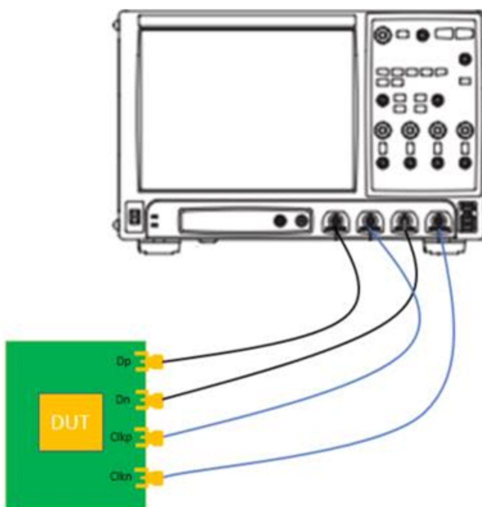


Figure 128 Probing for Alternate Calibration Sequence Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 128 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the **Set Up** tab, select or configure the options that define the connected DUT's characteristics.
3 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

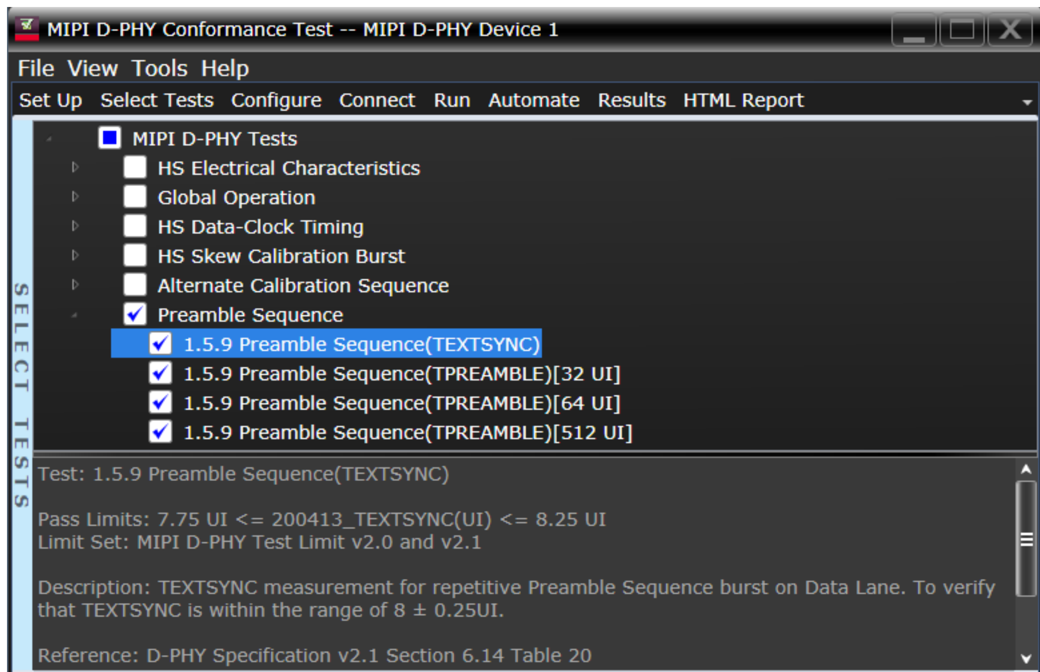


Figure 129 Selecting Preamble Sequence tests

4 Optionally, in the **Configure** tab, modify the configuration options that are needed for compliance.
5 Run the selected tests. Once tests are completed, the **Results** tab displays the test results.

Test 1.5.9 Preamble Sequence [TPREAMBLE] Method of Implementation

This test verifies the TPREAMBLE of the DUT is within the conformance limits.

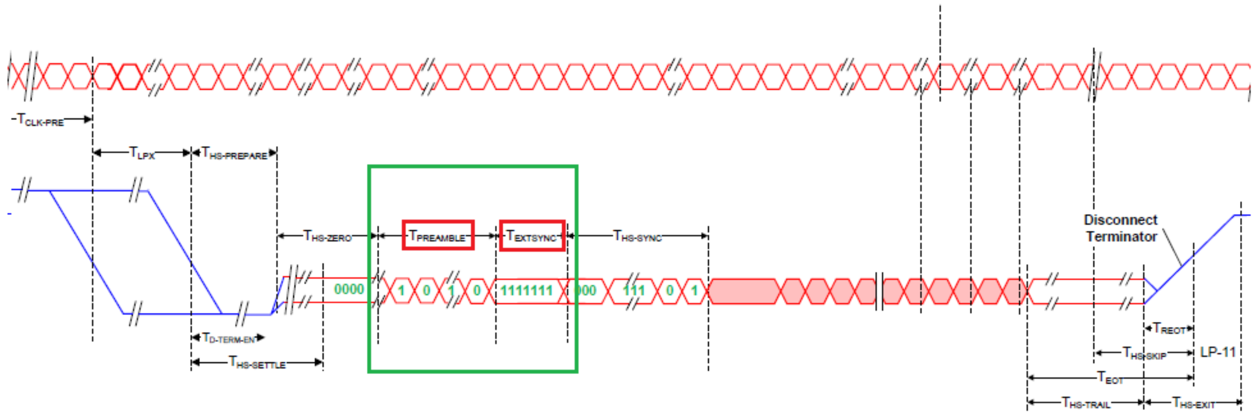


Figure 130 Preamble Sequence Timing

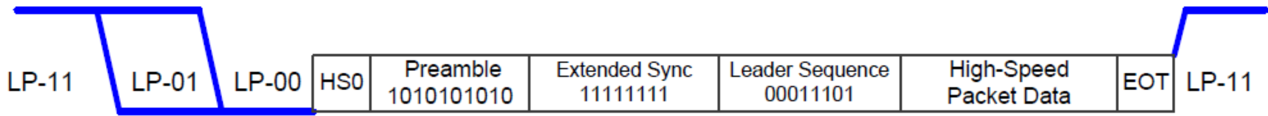


Figure 131 Preamble Sequence Requirements

PASS Condition

The measured TPREAMBLE shall be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 103 Test Availability Condition for Preamble Sequence test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
200410 200411 200412	>2.5 Gbps	100 ohm	Dependency on Continuous Clock setting	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe) or Direct Connect

Measurement Algorithm using Test ID 200410, 200411 and 200412

> **NOTE**
>
> **Use the Test ID# 200410, 200411 and 200412 to remotely access the test.**
>
> **This test supports Burst Clock & Burst Data signals and requires Repetitive Preamble Sequence.**

1. Trigger on Dp's falling edge in LP-01 at the SoT.
2. Construct differential data waveform of Dp and Dn using the following equation:

   DataDiff = Dp - Dn
3. Measure the average Unit Interval value of the differential data waveform.
4. Find the time when the first rising edge of the differential waveform crosses 0V after the LP-00 state. Mark this time as T1.
5. From the position marked as T1, find the final rising edge where the bit pattern "1010101010..." ends. Mark this time as T2.
6. From the position marked as T2, find the time when the next falling edge crosses 0V. Mark this time as T3.
7. Calculate TPREAMBLE using the following equation:

   TPREAMBLE = T2 - T1
8. Compare the measured TPREAMBLE value with the compliance test limits.

Test References

See Section 6.14, Table 20 in the D-PHY Specification v2.1.

Test 1.5.9 Preamble Sequence [TEXTSYNC] Method of Implementation

This test verifies the TEXTSYNC of the DUT is within the conformance limits.

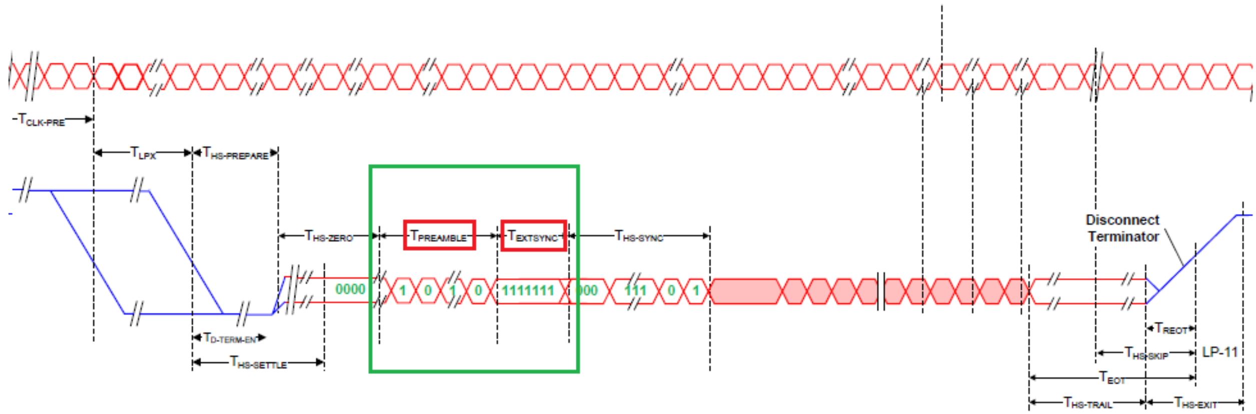


Figure 132 Preamble Sequence Timing

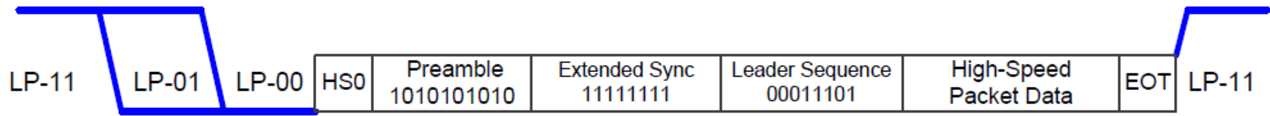


Figure 133 Preamble Sequence Requirements

PASS Condition

The measured TEXTSYNC shall be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 104 Test Availability Condition for Preamble Sequence test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
200413	>2.5 Gbps	100 ohm	Dependency on Continuous Clock setting	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Active Probe (Differential Probe) or Direct Connect

Measurement Algorithm using Test ID 200413

> **NOTE**
>
> **Use the Test ID# 200413 to remotely access the test.**
>
> **This test supports Burst Clock & Burst Data signals and requires Repetitive Preamble Sequence.**

1 The following test is run as a pre-requisite:
   a Preamble Sequence [TPREAMBLE (32UI)] (Test ID: 200413)
   : The positions T2 and T3 are measured.
2 Calculate TEXTSYNC using the following equation:

   TEXTSYNC = T3 - T2

3 Compare the measured TEXTSYNC value with the compliance test limits.

Test References

See Section 6.14, Table 20 in the D-PHY Specification v2.1.

Part VIII
HS Idle Timing Tests

KEYSIGHT
TECHNOLOGIES

42 MIPI D-PHY 2.0 & 2.1HS Idle Timing Tests

Probing for HS Idle Timing Tests / 486
Test 1.5.10 HS Idle [THS-IDLE-POST] Method of Implementation / 488
Test 1.5.10 HS Idle [THS-IDLE-CLKHS0] Method of Implementation / 490
Test 1.5.10 HS Idle [THS-IDLE-PRE + THS-ZERO] Method of Implementation / 491

This section provides the Methods of Implementation (MOIs) for the HS Idle Timing tests using a Keysight Infiniium Series oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test Application.

Probing for HS Idle Timing Tests

When performing the Alternate Calibration Sequence tests, the MIPI D-PHY Test Application will prompt you to make the proper connections. The connections for the these tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

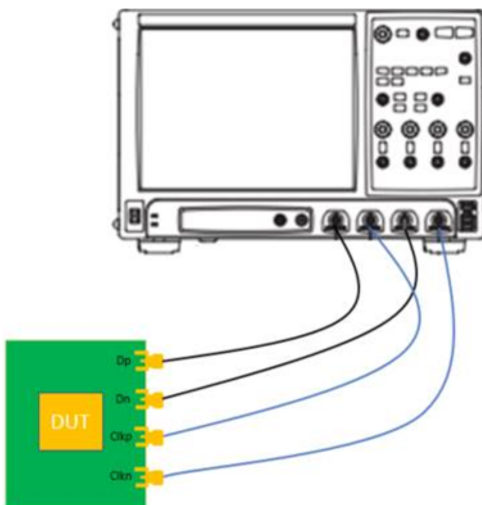


Figure 134 Probing for Alternate Calibration Sequence Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test Application. (The channels shown in Figure 134 are just examples).

For more information on the probe amplifiers and probe heads, refer to the help manuals for Infiniimax Probes.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Test Application".
2 In the **Set Up** tab, select or configure the options that define the connected DUT's characteristics.
3 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

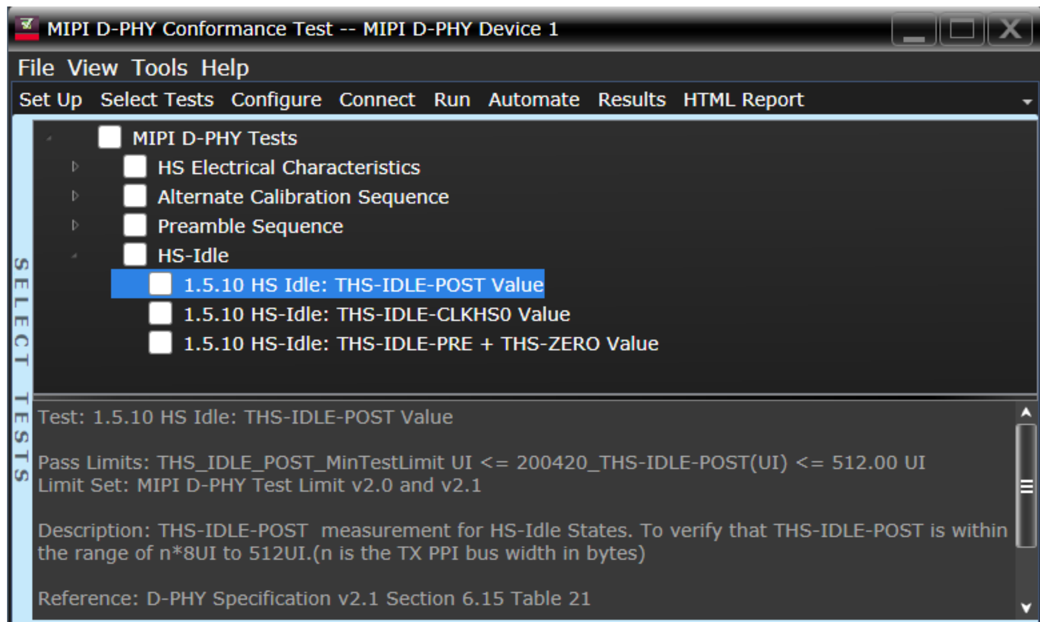


Figure 135 Selecting HS Idle Timing tests

4 Optionally, in the **Configure** tab, modify the configuration options that are needed for compliance.
5 Run the selected tests. Once tests are completed, the **Results** tab displays the test results.

Test 1.5.10 HS Idle [THS-IDLE-POST] Method of Implementation

This test verifies the THS-IDLE-POST of the DUT is within the conformance limits.

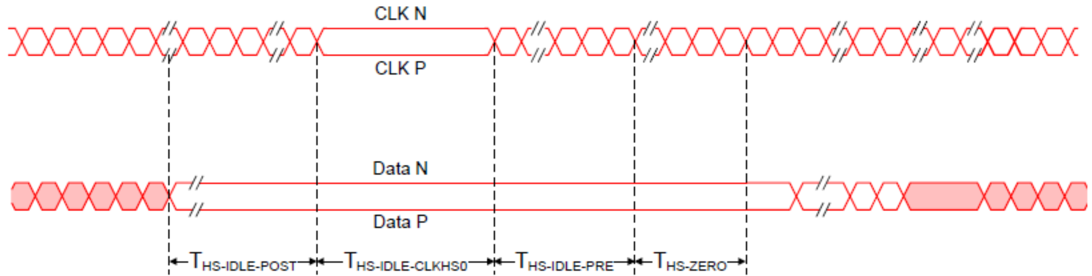


Figure 136 HS Idle Timing Diagram

PASS Condition

The measured THS-IDLE-POST shall be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 105 Test Availability Condition for HS Idle Timing test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
200420	Not Applicable	100 ohm	Dependency on Continuous Clock setting	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Direct Connect

Measurement Algorithm using Test ID 200420

NOTE Use the Test ID# 200420 to remotely access the test.

This test supports Burst Clock & Burst Data signals and requires Repetitive HS-Idle States.

1 Run the following test as a pre-requisite:

   a HS Clock Instantaneous (UIinst)(Max) (Test ID: 911)

   : The minimum, maximum and average Unit Interval of the differential clock waveform is measured and stored.

2 Trigger on the HS Idle State of the Data signal using a pulse width trigger.

3 Construct differential clock of Clkp and Clkn using the following equation:

$$ClockDiff = Clkp - Clkn$$

4 Construct differential data of Dp and Dn using the following equation:

$$DataDiff = Dp - Dn$$

5. To identify the HS-Idle position, find the start position of the first negative pulse width, which is greater than "Minimum Valid HS Idle State Length" value on the DataDiff waveform. You may configure the "Minimum Valid HS Idle State Length" value in the Configure tab. Mark this time as T1.
6. From the position marked as T1, find the start and end positions of the consecutive 0-bits pattern on ClockDiff. Mark the start position as T2 and end position as T3.
7. From the position marked at T3, find the next rising edge that crosses 0V on the DataDiff waveform. Mark this time as T4.

   Note that T4 is the time where the bit pattern '000' occurs in the end of HS Sync-Sequence. The bit pattern '000' of the HS Sync-Sequence must have the same duration as 3UI, where the Unit Interval value is measured in the pre-requisite test.

   Therefore, the end position of THS-ZERO must be (T4 - 3UI).
8. Calculate THS-IDLE-POST using the following equation:

   THS-IDLE-POST = T2 - T1
9. Compare the measured THS-IDLE-POST value with the compliance test limits.

Test References

See Section 6.15, Table 21 in the D-PHY Specification v2.1.

Test 1.5.10 HS Idle [THS-IDLE-CLKHS0] Method of Implementation

This test verifies the THS-IDLE-CLKHS0 of the DUT is within the conformance limits.

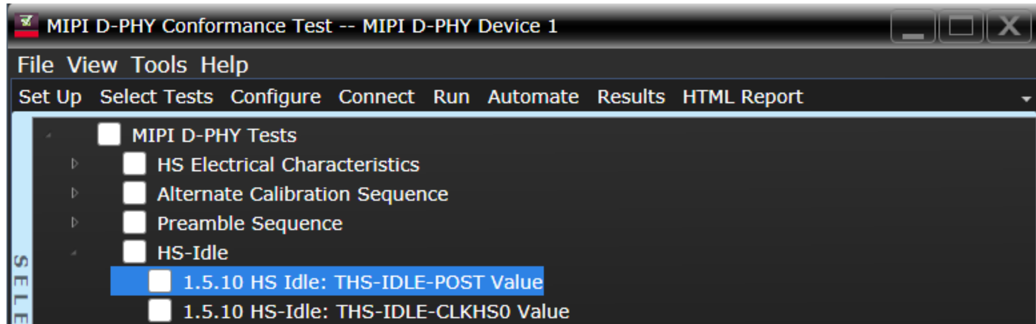


Figure 137 HS Idle Timing Diagram

PASS Condition

The measured THS-IDLE-CLKHS0 shall be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 106 Test Availability Condition for HS Idle Timing test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
200421	Not Applicable	100 ohm	Dependency on Continuous Clock setting	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Direct Connect

Measurement Algorithm using Test ID 200421

NOTE

Use the Test ID# 200421 to remotely access the test.

This test supports Burst Clock & Burst Data signals and requires Repetitive HS-Idle States.

1 The following test is run as a pre-requisite:

  a HS Idle: [THS-IDLE-POST] (Test ID: 200420)

  : The positions T2 and T3 are measured.

2 Calculate THS-IDLE-CLKHS0 using the following equation:

$$THS\text{-}IDLE\text{-}CLKHS0 = T3 - T2$$

3 Compare the measured THS-IDLE-CLKHS0 value with the compliance test limits.

Test References

See Section 6.15, Table 21 in the D-PHY Specification v2.1.

Test 1.5.10 HS Idle [THS-IDLE-PRE + THS-ZERO] Method of Implementation

This test verifies the THS-IDLE-PRE + THS-ZERO of the DUT is within the conformance limits.

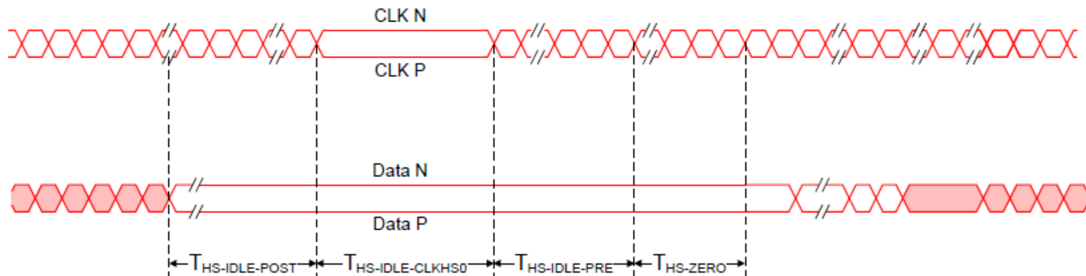


Figure 138 HS Idle Timing Diagram

PASS Condition

The measured THS-IDLE-PRE + THS-ZERO shall be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 107 Test Availability Condition for HS Idle Timing test

Associated Test ID	High-Speed Data Rate	ZID	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
200422	Not Applicable	100 ohm	Dependency on Continuous Clock setting	Disabled	Not Applicable	Not Applicable	Not Applicable	Not Applicable	Direct Connect

Measurement Algorithm using Test ID 200422

NOTE

Use the Test ID# 200422 to remotely access the test.

This test supports Burst Clock & Burst Data signals and requires Repetitive HS-Idle States.

1 The following test is run as a pre-requisite:
   a HS Idle: [THS-IDLE-POST] (Test ID: 200420)
   : The positions T3 and (T4 - 3UI) are measured.
2 Calculate THS-IDLE-PRE + THS-ZERO using the following equation:

   THS-IDLE-PRE + THS-ZERO = (T4 - 3UI) - T3

3 Compare the measured THS-IDLE-PRE + THS-ZERO value with the compliance test limits.

Test References

See Section 6.15, Table 21 in the D-PHY Specification v2.1.

Part IX
Informative Tests

KEYSIGHT
TECHNOLOGIES

43 MIPI D-PHY 2.0 & 2.1 Informative Tests

Test 1.3.I HS Data TX De-emphasis Level / 496

Other than the HS Data TX De-emphasis Level tests described below, the MIPI D-PHY 2.0 and 2.1 Informative tests are the same as MIPI D-PHY 1.0 Informative tests. Hence, they share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details regarding the rest of the tests, refer to "MIPI D-PHY 1.0 Informative Tests".

Test 1.3.I HS Data TX De-emphasis Level

This test verifies the De-emphasis level of the DUT is within the conformance limits.

PASS Condition

The measured De-emphasis level shall be within the conformance limit as specified in the D-PHY specification mentioned under the Test References section.

Test Availability Condition

Table 108 Test Availability Condition for HS Data TX De-emphasis Level

Associated Test ID	High-Speed Data Rate	Continuous Data	Continuous Clock	Data LP EscapeMode	Clock LP EscapeMode	Clock ULPS Mode	Informative Test	Probing Method
200300	> 2.5 Gbps	Enabled	Enabled	Not Applicable	Not Applicable	Not Applicable	Enabled	Direct Connect

Measurement Algorithm using Test ID 200300

NOTE Select **Informative Test** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 200300 to remotely access the test.

1. Trigger the Oscilloscope to acquire Dp, Dn, Clkp and Clkn waveforms.
2. Construct the differential clock of Clkp and Clkn using the following equation:

   DiffClock = Clkp-Clkn
3. Construct the differential data of Dp and Dn using the following equation:

   DiffData = Dp-Dn
4. For De-emphasis Level(Bit0) measurement, the Application searches the acquired for the respective reference data pattern of “1000”. An averaged waveform is generated, which consists of all reference data patterns found.
5. Using the Histogram function, the mean value for the histogram window that falls on the first ‘0’ bits will be measured as the Mean V_{OD0} value.
6. Using the Histogram function, the mean value for the histogram window that falls on the third ‘0’ bits will be measured as the Mean V_{OD0_EQ} value.
7. For De-emphasis Level(Bit1) measurement, the Application searches the acquired for the respective reference data pattern of “0111”. An averaged waveform is generated, which consists of all reference data patterns found.
8. Using the Histogram function, the mean value for the histogram window that falls on the first ‘1’ bits will be measured as the Mean V_{OD1} value.
9. Using the Histogram function, the mean value for the histogram window that falls on the third ‘1’ bits will be measured as the Mean V_{OD1_EQ} value.
10. Calculate De-emphasis Level(Bit0) using the equation:

$$EQ_{TX}(Bit0) = -20 \log (V_{OD0_EQ} / V_{OD0})$$

11 Calculate De-emphasis Level(Bit1) using the equation:

$$EQ_{TX}(Bit1) = -20 \log (V_{OD1_EQ} / V_{OD1})$$

12 Report measurement results for EQ_{TX}(Bit0) and EQ_{TX}(Bit1).

13 Compare the De-Emphasis Level values to the compliance test limits.

Test References

See Section 9.1.1.7, Table 25 in the D-PHY Specification v2.1.

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