RELEASE NOTES

D9040PCIC PCI Express Compliance Test Application

Keysight D9040PCIC Software Version 4.81.3.0

Release Date:	February, 2026
Operating System:	• Microsoft Windows 10 /11 (UXR/UXR-B-Series Oscilloscope) • Microsoft Windows 10 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series, or V-Series Oscilloscope)
Instrument Software Version:	• 11.71.00021 (UXR/UXR-B-Series Oscilloscope) • 11.71.00021 (MXR/MXR-B-Series Oscilloscope) • 6.74.01101 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series, or V-Series Oscilloscope)
File Name:	SetupInfPCIExpress04810003.exe
Licenses:	Please see the product data sheet on Keysight.com.

Issue Fixed

- Fixed an issue where the **Tx, Pseudo Package Loss** tests would report incorrect result values when executed alongside other tests with non-Preset 4 configurations.
  Please refer to **Appendix E – Tests Affected by the Pseudo Package Loss Preset Handling Issue** for the list of affected tests.

Keysight D9040PCIC Software Version 4.81.2.0

Release Date:	December, 2025
Operating System:	• Microsoft Windows 10 /11 (UXR/UXR-B-Series Oscilloscope) • Microsoft Windows 10 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series, or V-Series Oscilloscope)
Instrument Software Version:	• 11.71.00021 (UXR/UXR-B-Series Oscilloscope) • 11.71.00021 (MXR/MXR-B-Series Oscilloscope) • 6.74.01101 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series, or V-Series Oscilloscope)
File Name:	SetupInfPCIExpress04810002.exe
Licenses:	Please see the product data sheet on Keysight.com.

Issue Fixed

- Fixed an issue where certain tests in Base - Transmitter Test Point were incorrectly using the non-SRIS template file with SSC enabled.
  Please refer to **Appendix E – Base Test SSC Enabled Template File Changes** for the list of affected tests.

- Fixed incorrect measurement procedure for the following Reference Clock test, now it will use median cross point and edge rate as per the specification.

    - Clock Rise-Fall Matching Test

Keysight D9040PCIC Software Version 4.81.1.0

Release Date:	May, 2025
Operating System:	Microsoft Windows 10 /11 (UXR/UXR-B-Series Oscilloscope) Microsoft Windows 10 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series, or V-Series Oscilloscope)
Instrument Software Version:	11.70.00015 (UXR/UXR-B-Series Oscilloscope) 11.70.00015 (MXR/MXR-B-Series Oscilloscope) 6.74.01101 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series, or V-Series Oscilloscope)
File Name:	SetupInfPCIExpress04810001.exe
Licenses:	Please see the product data sheet on Keysight.com.

Issues Fixed

- Fixed an issue with the InfiniiSim bandwidth setting that impacted EndPoint and Root Complex tests.
- Corrected the limits for Tx Boost Ratio Full Swing and Tx Boost Ratio Reduced Swing tests.

Keysight D9040PCIC Software Version 4.81.0.0

Release Date:	September, 2023
Requirements Category (e.g., operating system):	Microsoft Windows 10
Requirements Category (e.g., instrument software version):	6.74.01101 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series, V-Series Oscilloscope) 11.60.00115 (UXR/UXR-B-Series Oscilloscope) 11.60.00115 (MXR/MXR-B-Series Oscilloscope)
File Name:	SetupInfPCIExpress04810000.exe
Licenses:	Please see the product data sheet on Keysight.com.

New Features / Additions

- Added **DUT Automation Toggle Count** setting in **Configure** tab for all tests except the reference clock tests.
- Added **RefClk Settings Precedence** setting in **Configure** tab for reference clock tests.
- Added following ten new tests:
    1. **Deterministic Jitter > 1.5 MHz** (Tx Tests, PCIe 2.0, 5.0 GT/s) (Test ID: 2192)
    2. **Random Jitter < 1.5 MHz** (Tx Tests, PCIe 2.0, 5.0 GT/s) (Test ID: 2194)
    3. **Ring-back Voltage** (RefClk Tests, PCIe 1.1/2.0/3.0/4.0, 2.5 GT/s) (Test ID: 930)
    4. **TStable** (RefClk Tests, PCIe 1.1/2.0/3.0/4.0, 2.5 GT/s) (Test ID: 940)
    5. **Absolute Period** (RefClk Tests, PCIe 1.1/2.0/3.0/4.0, 2.5 GT/s) (Test ID: 950)
    6. **Cycle to Cycle Jitter** (RefClk Tests, PCIe 1.1/2.0/3.0/4.0, 2.5 GT/s) (Test ID: 960)
    7. **Tx Boost Ratio Reduced Swing** (Tx Tests, PCIe 3.0/4.0, 8.0 GT/s) (Test ID 3190)
    8. **Tx Boost Ratio Full Swing** (Tx Tests, PCIe 3.0/4.0, 8.0 GT/s) (Test ID 3200)
    9. **Tx Boost Ratio Reduced Swing** (Tx Tests, PCIe 3.0/4.0, 16.0 GT/s) (Test ID 4190)
    10. **Tx Boost Ratio Full Swing** (Tx Tests, PCIe 3.0/4.0, 16.0 GT/s) (Test ID 4200)

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Modifications / Changes

- 8.0 GT/s and 16.0 GT/s Equalization Preset Tests enhanced to run multiple lanes with switch matrix.
- Modified connection diagram for Reference Clock tests for single ended and differential connections.
- Increased the maximum value for Reference Clock Tests > **Number of Clock UI Cycles** in **Configure** tab to 200k.
- Modified the default value for Reference Clock Tests > Sample Rate, GSa/s in **Configure** tab to Maximum.

Issues Fixed

- Fixed an issue wherein **SigTest Report Path Setup GUI** didn't have a **Done** button.
- Fixed an issue wherein tests aborted intermittently during run under certain conditions.
- Fixed an issue wherein Reference Clock tests were aborting during run under certain conditions with InfiniiSim enabled.
- Fixed an issue wherein running Reference Clock tests with UXR had a default value of 16 GSa/s.
- Fixed an issue of incorrect report header details in HTML report under certain conditions.
- Fixed an issue wherein MXR scope displayed incorrect test lists under certain conditions.
- Fixed an issue wherein application was not prompting for the signal required when user ran test using Switch Matrix
- Fixed an issue wherein DUT automation was unable to find the initial state of DUT under certain conditions.

Keysight D9040PCIC Software Version 4.80.1.0

Release Date:	April 7, 2023
Requirements Category (e.g., operating system):	Microsoft Windows 10
Requirements Category (e.g., instrument software version):	6.73.00102 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series, V-Series Oscilloscope) 11.50.00401 (UXR/UXR-B-Series Oscilloscope) 11.50.00601 (MXR/MXR-B-Series Oscilloscope)
File Name:	SetupInfPCIExpress04800001.exe
Licenses:	Please see the product data sheet on Keysight.com.

Modifications / Changes

- Updated Keysight License Manager 5.
- Supports UXR-B Series and MXR-B Series Oscilloscope.

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Keysight D9040PCIC Software Version 4.80.0.0

Release Date:	March 3, 2023
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.73.00102 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series, V-Series Oscilloscope) 11.40.00105 (UXR-Series Oscilloscope) 11.40.00105 (MXR-Series Oscilloscope)
File Name:	SetupInfPCIExpress04800000.exe
Licenses:	Please see the product data sheet on Keysight.com.

New Features / Additions

- Made measurement method (**SigTest** (default) or **Infiniium**) user selectable for below tests.
    - Deemphasized Voltage Ratio test
    - Peak Differential Output Voltage test

  Please see **Appendix E** for more info.
    - **Appendix E - Deemphasized Voltage Ratio Tests Change**
    - **Appendix E - Peak Differential Output Voltage Tests Change**
- Added the option to select multiple **Signal Quality Preset**s from P0 to P10.
  Please see **Appendix E – Signal Quality Preset Permutations** for the supported tests.
- EZJ (EZJIT) and EZP (EZJIT Plus) license have been set as mandatory for certain tests.
  Please see **Appendix E – License Required for Tests** for the test list.

Modifications / Changes

- In **Configure** tab, changed the naming and description of **Number of Clock UI** and **Reference Clock Tests** parameters to reflect the default settings.
- PCIE Gen 3.0, **Pseudo package loss** (8.0 GT/s) test name and limits changed.
  Please see **Appendix E - PCIE Gen 3.0 Pseudo Package Loss (8.0 GT/s)** for the change list.
- PCIE Gen 4.0 > **CEM – End Point Tests > Uncorrelated Deterministic Pulse Width Jitter** (16.0 GT/s) test (Test ID 4460) has been changed to informative.

- Changed the reporting format for test pass limits.
  Please see **Appendix E - Pass Limits Reporting Change** for the change list.

- Updated the template tests below with extrapolated eye height information:

  - **CEM - RootComplex Tests > Template Test** (16.0 GT/s) (Test ID 4510)
  - **CEM - EndPoint Tests > Template Test** (16.0 GT/s) (Test ID 4410)

- If jitter test value is calculated negative, it will be reported as zero.
  Please see **Appendix E - Jitter Tests Value Reporting Change** for the change list.

Issues Fixed

- Fixed the bug wherein **5.0 GT/s De-emphasis** selection was not visible after switching from **Half** to **Full** power level.

- Fixed parameters reported as no value in **Peak Differential Output Voltage** test.
  Please see **Appendix E – Peak Differential Output Voltage Reporting** for the test list.

- Modified SigTest template file to properly handle SSC tests.
  Please see the impacted test list in **Appendix E – Updated 2.5 GT/s and 5.0 GT/s SSC Enabled Template File for Base Tests**.

- Fixed parameters reported as no value in certain CEM - RootComplex tests.
  Please see **Appendix E – Fixed Reporting as No Value** for the test list.

- Fixed bug to ensure 5.0 GT/s tests should not be visible when the data rate is not supported in MXR scope.

- Fixed bug to ensure eye diagram image should not be reported in tests other than template tests.

- Fixed bug to ensure that the CAL OUT option should not be available for MXR oscilloscope.

- Fixed bug related to missing name info in test results and report in case for 5.0 GT/s de-emphasis.
  Please see, **Appendix E – 5.0 GT/s De-emphasis Missing Test Name Information** for the test list.

Known Issues

- Limitation: Infiniium Offline only supports VXI-11 protocol address TCPIP0::localhost::inst0::INSTR to successfully run certain tests.
  Please see **Appendix E – Limitation When Using Infiniium Offline** for the test list.

KEYSIGHT

Keysight D9040PCIC Software Version 4.71.9.0

Release Date:	August 30, 2022
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.73.00102 (90000 Series, 90000 X-Series, 90000 Q-Series, or Z-Series Oscilloscope) 11.30.00406 (UXR-Series Oscilloscope) 11.30.00406 (MXR-Series Oscilloscope)
File Name:	SetupInfPCIExpress04710009.exe
Licenses:	Please see the product data sheet on Keysight.com.

Issues Fixed

- Increased the number of maximum attempts allowed to reset the DUT during the DUT Automation operation.
- Fixed DUT Automation functionality to allow toggling to the correct preset required for Base – Transmitter Tests.
- Fixed the issue related to incompatible SCPI command related to AUX OUT port of Keysight Infiniium 90000 Series oscilloscopes.

Keysight D9040PCIC Software Version 4.71.4.0

Release Date:	April 12, 2022
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.71.00001 (90000 Series, 90000 X-Series, 90000 Q-Series, or 90000 Z-Series Oscilloscope) 11.25.00202 (UXR-Series Oscilloscope) 11.25.00202 (MXR-Series Oscilloscope)
File Name:	SetupInfPCIExpress04710004.exe
Licenses:	Please see the product data sheet on Keysight.com.

Modifications / Changes

- Peak Differential Output Voltage tests in CEM Test Point will no longer display an eye diagram.

Issues Fixed

- Fixed the automation script run error which occurred after loading saved project.
- Fixed PWJ tests error which occurred when the SRIS option was enabled.
- Fixed the manual toggle windows. Now, correct preset number is displayed while running Equalization Preset Tests.

Known Issues

- 5.0 GT/s De-emphasis option in Device Under Test Setup windows might not be visible properly after switching Power Level option.

  Workaround: Start a new project or switch to another Test Point to restore the 5GT/s De-emphasis option.

KEYSIGHT

Keysight D9040PCIC Software Version 4.71.0.0

Release Date:	October 26, 2021
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.60.00403 (90000 Series, 90000 X-Series, 90000 Q-Series, or Z-Series Oscilloscope) 11.10.00105 (UXR-Series Oscilloscope) 11.40.00105 (MXR-Series Oscilloscope)
File Name:	SetupInfPCIExpress04710000.exe
Licenses:	Please see the product data sheet on Keysight.com.

New Features / Additions

- Supports the Keysight Infiniium applications' bundle license for PCIe. The PCI Express bundle license provides access to the following applications:
    - Keysight D9040PCIC PCI Express Compliance Test Application
    - Keysight D9050PCIC PCI Express Gen 5 Compliance Test Application

Keysight D9040PCIC Software Version 4.70.10.0

Release Date:	May 28, 2021
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.55.00504 (90000 Series, 90000 X-Series, 90000 Q-Series, or 90000 Z-Series Oscilloscope) 10.25.01302 (UXR-Series Oscilloscope) 11.10.00202 (MXR-Series Oscilloscope)
File Name:	SetupInfPCIExpress04700010.exe
Licenses:	Please see the product data sheet on Keysight.com.

New Features / Additions

- The application now supports the MXR Oscilloscope. Following tests are supported:
    - All tests at 2.5 GT/s data rate
    - Only reference clock tests at all data rates

Modifications / Changes

- The following PCIe 4.0, Base -Transmitter Tests at 16.0 GT/s data rate, now require a PWJ clock pattern:
    - Total Uncorrelated PWJ
    - Deterministic DjDD Uncorrelated PWJ
- PCIe 4.0, Base -Transmitter Tests at 16.0 GT/s data rate have been reordered to optimize the test flow
- Negative measurement result produced by the following PCIe 4.0, Base – Transmitter Test at 8.0 GT/s data rate will be reported as an invalid result:
    - Uncorrelated Deterministic Jitter Test
- Standardized Eye-Width test naming and the test result description; please see Appendix D for the change list.

Issues Fixed

- Fixed timeout issue in **Unit Interval Test** (**PCIe4.0**, **Root – Complex Test**,) which occurred with following configuration:
    - UXR Oscilloscope
    - InfiniiSim enabled
- Removed eye width checking in the following **PCIe 2.0**, **Base – Receiver Test,** at **5.0 GT/s** data rate:
    - Common Refclk Architecture Template Test
- Removed invalid eye diagram in the following **PCIe 4.0**, **CEM - RootComplex Test**, at **16.0 GT/s** data rate:
    - Eye-Width Test
- Fixed invalid result description for the following **PCIe 4.0**, **Base – RefClk Test**, at **2.5 GT/s** data rate:
    - Peak to Peak Jitter (Common Clk)
- Fixed general GUI bugs

Keysight D9040PCIC Software Version 4.70.0.0

Release Date:	March 10, 2021
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.55.00504 (90000 Series, 90000 X-Series, 90000 Q-Series, or Z-Series Oscilloscope) 10.25.01302 (UXR-Series Oscilloscope)
File Name:	SetupInfPCIExpress04700000.exe
Licenses:	Please see the product data sheet on Keysight.com.

Additions / New Features

- Added remote command to setup M81150/60A in DUT Automation.

Modifications / Changes

- The application has been updated to FW0624 and SL0624.
- Performed correction on “Non Transtion” test name; please see Appendix B for the change list.
- Updated PCIE Generation 3, Base Tx Template Test to informative test; please see Appendix C for the change list
- Applied -12dB CTLE template file for 16.0 GT/s CEM End Point Pulse Width Jitter tests
- Interpolation option (if selected) will now apply to the entire tests from all data rates and PCIE Generation during signal acquisition. It was not applying to all tests from PCIE Generation 3 previously.
- Interpolation will not apply to waveform while loading the waveform. Previously, the application was applying 16 pts interpolation while loading waveform for Rise/Fall time Test.
- Corrected the “Connection Type” reporting in Saved Waveform Mode
- Included tolerance in test limits for PCIE Generation 4, Base Transmitter SSC Peak Deviation (Min and Max) tests
- Ensured that the IP and SICL address of M81150/60A is not empty prior to establishing a connection

- Removed SigTest version 3.2.0.3 option in 16GT/s tests
- Removed sample rates option that is no longer valid

Issues Fixed

- Fixed Peak Differential Output Voltage (Non Transition) test reporting invalid test result
- Fixed Rise/Fall Time test error when interpolation option is enabled
- Fixed Connection Type reporting bugs in Test Report
- Fixed missing preset information during manual toggle
- Fixed Workshop Mode test did not use SSC template file when SSC is enabled
- Fixed missing remote hints in Test Point selection
- Fixed DUT Automation bugs
- Fixed GUI bugs after load project
- Fixed general GUI bugs
- Fixed test filtering bugs

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Keysight D9040PCIC Software Version 4.60.0.0

Release Date:	November 20, 2020
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.55.00504 (90000 Series, 90000 X-Series, 90000 Q-Series, or Z-Series Oscilloscope) 10.25.00902 (UXR-Series Oscilloscope)
File Name:	SetupInfPCIExpress04600000.exe
Licenses:	Please see the product data sheet on Keysight.com.

Additions / New Features

- Added user tips in “DUT Automation Setup” dialog box
- Enabled 128 GSa/s Sample Rates option for 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s tests
- Added 2.5G/s Template Test in Base – Receiver Tests for PCIE Generation 1.1 and 2.0

Modifications / Changes

- The application has been updated to FW0621 and SL0621
- Major update on test pass limits, spec references, test descriptions, and test IDs across the application; please see Appendix A for complete change list
- The entire set of Base – Receiver Tests has been updated to use SigTest executable
- At 8.0 GT/s, embedding has been switched from SigTest to InfiniiSim for below mentioned test points as SigTest does not support data rates higher than 40 GSa/s
    - CEM – End Point Tests
    - CEM – Root Complex Tests
    - U.2 – End Point Tests
    - U.2 – Root Complex Tests
- Only Single Ended connection option is available for Switch Matrix
- Only Full Power Level option is available for CEM – End Point / Root Complex and U.2 – End Point / Root Complex test points
- Peak Differential Output Voltage test in Base – Receiver Tests has been changed to Peak Differential Input Voltage test

- DUT Automation feature will not save preset waveforms that are not needed for Low Power Equalization Preset Tests
- Unit Interval Tests have been enhanced to report test results up to the precision level of 5 decimal points
- 8.0 GT/s and 16 GT/s Min swing during EIEOS for reduced swing test have been updated to request for Preset 1 waveform
- Sample rates and bandwidth setting changed message moved to Summaries panel, no longer a message box prompted
- Removed User Defined Limit selection

Issues Fixed

- Fixed low power tests use wrong template file when running tests in batch
- Fixed common mode test failed to run using Saved Waveform mode
- Fixed common mode test failed on second run when using remote command
- Fixed Equalization Preset Test reported test result with invalid unit
- Fixed Unit Interval Test using SRIS limit in PCIE Generations that do not support SRIS option
- Fixed 8.0 GT/s and 16 GT/s SSC Df/Dt measurement graph plotting issue
- Fixed tests do not use SRIS template file when SRIS option is enabled
- Fixed Manual Toggle not working after user re-setup toggle source / close and re-launch the Manual Toggle GUI
- Fixed Reference Clock – RMS Jitter test did not remove of non-SSC content
- Fixed test filtering bugs

KEYSIGHT

Keysight D9040PCIC Software Version 4.50.2.0

Release Date:	July 30, 2020
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.55.00504 (90000 Series, 90000 X-Series, 90000 Q-Series, or Z-Series Oscilloscope) 10.25.00607 (UXR-Series Oscilloscope)
File Name:	SetupInfPCIExpress04500002.exe
Licenses:	Please see the product data sheet on Keysight.com.

Issues Fixed

- Fixed DUT Automation does not toggle to correct preset when running Preset Equalization Test.
- Fixed DUT Automation goes wrong when Collective Data Acquisition option is enabled.

Keysight D9040PCIC Software Version 4.50.0.0

Release Date:	June 30, 2020
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.55.00504 (90000 Series, 90000 X-Series, 90000 Q-Series, or Z-Series Oscilloscope) 10.25.00607 (UXR-Series Oscilloscope)
File Name:	SetupInfPCIExpress04500000.exe
Licenses:	Please see the product data sheet on Keysight.com.

Additions / New Features

- Supports 2 channel scope
- Supports 16 lanes switch matrix for Base Transmitter Tests & CEM End Point Tests with Single Ended Connections
- DUT Automation is now available in Base – Transmitter Tests
- SigTest version configuration option (Debug Mode) is now user editable
- SigTest version configuration option (Debug Mode) for 8 GT/s & 16 GT/s Equalization Preset Tests is now available
- Added SigTest version 4.0.52
- Reports SigTest version used in 8 GT/s Equalization Preset Tests
- Reports “NA” for test result in case SigTest tool doesn’t provide any result.
- Added notes to highlight that SigTest tool version 4.0.x does not support 2.5, 5.0, and 8.0 GT/s CEM tests
- Supports N5444A Probe Head
- Added support for binary waveform (.bin) file for saved waveform option.

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Modifications / Changes

- Uses FW0610 and SL0610
- Updated Method of Implementation (MOI) and Online Help
- Provided M81150A/60A and CAL OUT (100 MHz) as toggle source option for UXR
- Provided M81150A/60A, CAL OUT (100 MHz), CAL OUT (HF Osc), and AUX OUT (HF Osc) as toggle source option for non-UXR
- Improved compliance pattern signal check for 16 GT/s signal
- Added Peak Differential Output Voltage (Transition and Non-Transition) in all PCIE generations
- Added Deemphasized Voltage Ratio Test in all PCIE generations
- Updated and enhanced the content of Connection Diagram
- Format changed for Connection Type in test report (to support 2 channel scope)
- Enhanced change signal message content
- Unit Interval Test is now showing exact value for its test limit
- Changed 2.5 GT/s Unit Interval Test to use mean UI as final result
- Updated the number of presets required by 16 GT/s Pulse Width Jitter test;
  DUT Automation will perform the same number of toggles according to updated number of presets.
- Updated Sample Rate to show accurate value
- Test apps will stop and prompt user to re-enable DUT after the test using idle signal is completed if DUT Automation features is enabled.
- Disabled Preset Equalization Test option when Reference Clock Test is selected
- Allowed use of FUNC3 for clock signal display for Root Complex test
- Changed Receiver Test naming – Peak Differential Output Voltage to Peak Differential Input Voltage for 2.5 GT/s data rate in PCIe 1.0a. PCIe 1.1, and PCIe 2.0.
- Migrated U.2 Root Complex Tests to use SigTest executables for more accurate result
- Cleaned up distributed SigTest template file folder
- Cleaned up connection diagram file that is no longer needed

- Renamed "Differential Probe" to "Differential" in Connection Setup windows
- Removed "Timeout.txt" and its dependencies, and replaced with common time out amount
- Removed "Use Power Switch Reset DUT" feature
- Removed “Silent Mode” option for SigTest
- Removed unnecessary "Sample Rate" field from report section
- Removed S-Parameter option that is no longer applicable
- Removed "Docs" folder; merged its content into *C:\Program Files\Keysight\Infiniium\Apps\PCIExpress\help*
- Removed *C:\Program Files\Keysight\Infiniium\Apps\PCIExpress\deembed* folder; merged its content into *C:\Users\Public\Documents\Infiniium\Apps\PCIExpress\S-Params*
- Moved INF_SMA_Deskew.set to *C:\ProgramFiles\Keysight\Infiniium\Apps\PCIExpress\app\setups*

Issues Fixed

- Resolved the issue: Invalid template file used for 16 GT/s Root Complex test when SSC option is enabled
- Pass limits corrected for Peak Differential Output Voltage Tests (both Transition and Non-Transition)
- Fixed Pseudo package loss, Root device test limit (both Gen3 and Gen4)
- Fixed invalid Random Jitter Test result
- Fixed differential connection not working for “Collective Data Acquisition” option
- Fixed missing required signal change message prompt for Crosstalk and Without Crosstalk test
- Fixed invalid test result in “Workshop Compliance Mode” due to no embedding applied
- Fixed 16 lanes switch matrix issue
- Removed Base Transmitter Template Test with deemphasis for low power
- Added Template Test with deemphasis in PCIE Gen4
- Fixed wrapper memory issue for Rx Tests
- Fixed tests not running with default setting after test application is launched
- Fixed the tests that were not running in Offline mode
- Fixed false fail results in Base Rx Tests
- Fixed Reference Clock Test error that appeared when the test was run with different parameters and the test results were appended to the existing results.
- Fixed no connection change message / duplicate connection change prompt issue
- Fixed the issue related to limiting the bandwidth settings based on scope capability.
- Fixed scaling issue in UXR Senior
- Fixed Template Test as it was using invalid template for -3.5 dB and -6.0 dB deemphasis
- Fixed the defect related to license validation while loading a saved project
- Fixed issue to enable Single Ended connection option for Saved Waveform mode and Automation script
- Fixed AC-CM invalid limit issue

- Fixed differential connection not switching clock channel correctly for Root Complex tests
- Fixed SSC Mod Deviation formula
- Removed extra signal scaling steps in DUT automation which was causing error when running in UXR Senior
- Fixed the defect: Equalization preset tests throw error when run using DUT Automation feature with Collective Acquisition on.
- Resolved intermittent timeout issue when Measure All Edges option is turned on
- Removed redundant configuration variables in Remote Programming variables
- Resolved error found in Workshop Mode test and reduced its test time
- Fixed the issue that Test Point GUI did not refresh correctly as per user's last selected option
- Fixed general Switch Matrix test routine issue
- Fixed general CEM and U.2 - Root Complex Tests routine issue
- Fixed general 2 channels scope issue
- Fixed general test result calculation (result unit and test limit issue)
- Fixed general GUI issue

Known Issues

- Tests do not run correctly in case of multiple trials while using Saved Waveform Mode through remote command.
- 5GT/s Base Receiver Test – Peak Differential Output Voltage should be Peak Differential Input Voltage.
- SigTest is generating eye diagrams having inaccurate upper limit for Gen4 CEM 8.0 GT/s and 16.0 GT/s Tests
- Some tests have inaccurate test description and references
- SigTest tools (version 3.2.0.3) doesn't provide test results for the following Base Transmitter tests:
    - Total uncorrelated PWJ (2.5 GT/s, 5.0 GT/s, and 8.0 GT/s)
    - Deterministic DjDD uncorrelated PWJ (2.5 GT/s, 5.0 GT/s, and 8.0 GT/s)
    - Data dependent jitter (2.5 GT/s, 5.0 GT/s, and 8.0 GT/s)

  - Pseudo package loss, Root or Non-root device (8.0 GT/s)
  - Full swing Tx voltage with no TxEQ (8.0 GT/s)
  - Min swing during EIEOS for full swing (8.0 GT/s)

- SigTest tools (version 4.0.46) doesn't provide test results for the following Base Transmitter Tests:

  - Uncorrelated total jitter (2.5 GT/s, 5.0 GT/s, and 8.0 GT/s)
  - Uncorrelated deterministic jitter (2.5 GT/s, 5.0 GT/s, and 8.0 GT/s)
  - Random jitter (2.5 GT/s, 5.0 GT/s, and 8.0 GT/s)

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Keysight D9040PCIC Software Version 4.31.0004

Release Date:	December 12, 2019
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.50.00906 (90000 Series, 90000 X-Series, 90000 Q-Series, or Z-Series Oscilloscope) 10.12.05115 (UXR-Series Oscilloscope)
File Name:	SetupInfPCIExpress04310004.exe
Licenses:	Please see the product data sheet on Keysight.com.

Additions / New Features

- Added SigTest version 4.0.51 and default version for the entire 16 GT/s tests

Modification / Changes

- Updated SigTest version 3.2.0.3 as default version for 8 GT/s CEM End Point tests
- Updated non-transition eye limit for SigTest version 4.0.46 & 4.0.51 template file

Issues Fixed

- Fixed Reference Clock RMS Jitter test report false failed issue

KEYSIGHT

Keysight D9040PCIC Software Version 4.31.0003

Release Date:	November 11, 2019
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.50.01201 (90000 Series, 90000 X-Series, 90000 Q-Series, or Z-Series Oscilloscope) 10.11.05004 (UXR-Series Oscilloscope)
File Name:	SetupInfPCIExpress04310003.exe
Licenses:	Please see the product data sheet on Keysight.com.

Additions / New Features

- Report selected Preset on each test run
- Reported additional Jitter measurement result output by SigTest executables

Modification / Changes

- Removed “Non-transition failures” & “Transition failures” result field in Template Tests
- Updated Bandwidth, Number of UI and Sampling Rates option
- Fixed SigTest executables generated text file result to Project folder
- Handle SigTest executables version 3.2.0.3 that output **"Composit Eye Height"**

Issues Fixed

- Fixed wrong labelling in eye diagram
- Fixed upload result to repository error due to long test name
- Fixed Template Test reported false failed result
- Fixed SSC tests that are not working due to missing reference assembly
- Fixed switch matrix error when user chooses Keysight U3020A S26
- Fixed Low Power Template Test not reporting eye diagram issue
- Fixed no proper channel setup issue when running test using multiple lane

Known Issues

- Unable to run Equalization Preset Tests with “Collective Data Acquisition” features together with Signal Quality Tests at the same time.

KEYSIGHT

Keysight D9040PCIC Software Version 4.31.0001

Release Date:	September 20, 2019
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.40.01101 (90000 Series, 90000 X-Series, 90000 Q-Series, or Z-Series Oscilloscope) 10.11.04711 (UXR-Series Oscilloscope)
File Name:	SetupInfPCIExpress04310001.exe
Licenses:	Please see the product data sheet on Keysight.com.

Additions / New Features

- Added informative Pseudo Package Loss test for Non-Root Package Device that does not support captive channel

Modification / Changes

- Removed Switch Matrix license checking as it is no longer needed

Issues Fixed

- Fixed 2.5 GT/s Average Clock Period test result screenshot in full windows
- Fixed 2.5 GT/s Rise/Fall Time test invalid test limit
- Fixed 2.5 GT/s Template Test not showing transition eyes diagram
- Fixed 5 GT/s informative Template Test appears as “Fail” in test report
- Fixed DUT Automation did not re-toggle to correct signal for 5 GT/s crosstalk and without crosstalk tests

Keysight D9040PCIC Software Version 4.31.0000

Release Date:	July 26, 2019
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.40.00801 (90000 Series, 90000 X-Series, 90000 Q-Series, or Z-Series Oscilloscope) 10.10.04601 (UXR-Series Oscilloscope)
File Name:	SetupInfPCIExpress04310000.exe
Licenses:	Please see the product data sheet on Keysight.com.

Additions / New Features

- Supports PPKS license
- Added CEM – End Point PWJ tests which required “Preset 10 + extra 2 toggles” signal
- Replaced Pseudo package loss test with 2 separate tests as listed below:
    - Pseudo package loss, Non-root device
    - Pseudo package loss, Root device
- It is applicable to PCIe Gen 3 and PCIe Gen 4, according to specification
- Added InfiniiSim license checking at the beginning of test. Notify user and abort test if license is not available.
- Prompt user with extra information of signal required to run test

Modification / Changes

- Updated default bandwidth limit and sampling rates value according to data rates
- Removed “SigTest Embedding” button which is no longer applicable
- 5GT/s Template test in Base Transmitter Tests is using fixed template file. No deemphasis level template file being used anymore
- Equalization Preset tests are no longer able to run with different Test Point at one time, while using saved waveform (offline mode) to run test

- Replaced Gen 4 2.5 GT/s RMS Jitter (Common Clk) test with Peak to Peak Jitter (Common Clk) test according to specification
- Corrected the required signal information
- Workshop Mode no longer saves signal in WFM format
- Improved Workshop Mode & Equalization Preset test time by removing saving of signal in BIN format redundantly
- Removed checking for signal trigger during signal pattern checking

Issues Fixed

- Fixed Root Complex test error and missing connection diagram issue if user changed the channel configuration to use Channel 2 and 4
- Fixed missing required signal change notification to user
- Fixed test did not re-acquire waveform with correct Preset
- Fixed Jitter measurement trend timeout issue in SSC test
- Fixed inaccurate test filtering & test list availability issue
- Fixed inaccurate test result issue
- Fixed SigTest reported result string changed issue in newer version
- Fixed invalid GUI option available for user
- Fixed DUT Automation AUX out issue
- Fixed general license checking issue

Known Issues

- Refer Version 04.30 “Known Issue” section for details

SigTest version configuration overview

- PCIE Gen 1.0a & SigTest

Gen	Data Speed (GT/s)	Test Point	SigTest Configuration
1.0a	2.5	Base	4.0.46
		CEM – End Point	3.2.0.3
		CEM – Root Complex	3.2.0.3

- PCIE Gen 2.0 & SigTest

Gen	Data Speed (GT/s)	Test Point	SigTest Configuration
1.1	2.5	Base	4.0.46
		CEM – End Point	3.2.0.3
		CEM – Root Complex	3.2.0.3
		Reference Clock	3.2.0 (Not configurable)

- PCIE Gen 2.0 & SigTest

Gen	Data Speed (GT/s)	Test Point	SigTest Configuration
2.0	2.5	Base	4.0.46
		CEM – End Point	3.2.0.3
		CEM – Root Complex	3.2.0.3
		Reference Clock	3.2.0 (Not configurable)
	5	Base	4.0.46
		CEM – End Point	3.2.0.3
		CEM – Root Complex	3.2.0.3
		Reference Clock	3.2.0 (Not configurable)

- PCIE Gen 3.0 & SigTest

Gen	Data Speed (GT/s)	Test Point	SigTest Configuration
3.0	2.5	Base	4.0.46
		CEM – End Point	3.2.0.3
		CEM – Root Complex	3.2.0.3
		U.2 – End Point	3.2.0.3
		U.2 – Root Complex	3.2.0.3
		Reference Clock	3.2.0 (Not configurable)
	5	Base	4.0.46
		CEM – End Point	3.2.0.3
		CEM – Root Complex	3.2.0.3
		U.2 – End Point	3.2.0.3
		U.2 – Root Complex	3.2.0.3
		Reference Clock	3.2.0 (Not configurable)
	8	Base	4.0.46
		CEM – End Point	3.2.0.3
		CEM – Root Complex	3.2.0.3
		U.2 – End Point	3.2.0.3
		U.2 – Root Complex	3.2.0.3
		Reference Clock	3.2.0 (Not configurable)
		Preset	4.0.46 (Not configurable)

- PCIE Gen 4.0 & SigTest

Gen	Data Speed (GT/s)	Test Point	SigTest Configuration
4.0	2.5	Base	4.0.46
		CEM – End Point	3.2.0.3
		CEM – Root Complex	3.2.0.3
		Reference Clock	3.2.0 (Not configurable)
	5	Base	4.0.46
		CEM – End Point	3.2.0.3
		CEM – Root Complex	3.2.0.3
		Reference Clock	3.2.0 (Not configurable)
	8	Base	4.0.46
		CEM – End Point	3.2.0.3
		CEM – Root Complex	3.2.0.3
		Reference Clock	3.2.0 (Not configurable)
		Preset	4.0.46 (Not configurable)
	16	Base	4.0.46
		CEM – End Point	4.0.46
		CEM – Root Complex	4.0.46
		Reference Clock	3.2.0 (Not configurable)
		Preset	4.0.46 (Not configurable)

Keysight N5393F/N5393G Software Version 4.30.0001

Release Date:	October 30, 2018
Requirements Category (e.g., operating system):	Microsoft Windows 7
Requirements Category (e.g., instrument software version):	6.30.00609 (90000 Series, 90000 X-Series, 90000 Q-Series, or Z-Series Oscilloscope) 10.00.03708 (UXR-Series Oscilloscope)
File Name:	SetupInfPCIExpress04300001.exe
Licenses:	Please see the product data sheet on Keysight.com.

Modification / Changes

- Fixed 16GT/s Equalization Preset Tests SigTest error when Collective Data Acquisition option enabled
- Improve signal scaling to handle inconsistent Idle state for Absolute delta of DC common mode voltage during L0 and Idle tests

Known Issues

- Refer Version 04.30 “Known Issue” section for details

SigTest version configuration overview

- PCIE Gen 1.0a & SigTest

Gen	Data Speed (GT/s)	Test Point	SigTest Configuration
1.0a	2.5	Base	4.0.39
		CEM – End Point	4.0.39
		CEM – Root Complex	3.2.0.1

- PCIE Gen 2.0 & SigTest

Gen	Data Speed (GT/s)	Test Point	SigTest Configuration
1.1	2.5	Base	3.2.0 (Not configurable)
		CEM – End Point	4.0.39
		CEM – Root Complex	3.2.0.1
		Reference Clock	3.2.0 (Not configurable)

- PCIE Gen 2.0 & SigTest

Gen	Data Speed (GT/s)	Test Point	SigTest Configuration
2.0	2.5	Base	3.2.0 (Not configurable)
		CEM – End Point	4.0.39
		CEM – Root Complex	3.2.0.1
		Reference Clock	3.2.0 (Not configurable)
	5	Base	3.2.0 (Not configurable)
		CEM – End Point	4.0.37
		CEM – Root Complex	3.2.0.1
		Reference Clock	3.2.0 (Not configurable)

- PCIE Gen 3.0 & SigTest

Gen	Data Speed (GT/s)	Test Point	SigTest Configuration
3.0	2.5	Base	3.2.0 (Not configurable)
		CEM – End Point	4.0.39
		CEM – Root Complex	3.2.0.1
		U.2 – End Point	4.0.39
		U.2 – Root Complex	3.2.0.1
		Reference Clock	3.2.0 (Not configurable)
	5	Base	3.2.0 (Not configurable)
		CEM – End Point	4.0.37
		CEM – Root Complex	3.2.0.1
		U.2 – End Point	4.0.37
		U.2 – Root Complex	3.2.0.1
		Reference Clock	3.2.0 (Not configurable)
	8	Base	3.2.0 (Not configurable)
		CEM – End Point	4.0.39
		CEM – Root Complex	3.2.0.1
		U.2 – End Point	4.0.39
		U.2 – Root Complex	3.2.0 (Not configurable)
		Reference Clock	3.2.0 (Not configurable)
		Preset	4.0.37 (Not configurable)

- PCIE Gen 4.0 & SigTest

Gen	Data Speed (GT/s)	Test Point	SigTest Configuration
4.0	2.5	Base	3.2.0 (Not configurable)
		CEM – End Point	4.0.39
		CEM – Root Complex	3.2.0.1
		Reference Clock	3.2.0 (Not configurable)
	5	Base	4.0.37
		CEM – End Point	4.0.37
		CEM – Root Complex	3.2.0.1
		Reference Clock	3.2.0 (Not configurable)

	8	Base	4.0.39
		CEM – End Point	4.0.39
		CEM – Root Complex	3.2.0.1
		Reference Clock	3.2.0 (Not configurable)
		Preset	4.0.37 (Not configurable)
	16	Base	4.0.39
		CEM – End Point	4.0.39
		CEM – Root Complex	3.2.0.1
		Reference Clock	3.2.0 (Not configurable)
		Preset	4.0.37 (Not configurable)

KEYSIGHT

Keysight N5393F/N5393G Software Version 04.30

Released Date:	10th October 2018
Requirements category (e.g., operating system):	Microsoft Windows 7
Requirements category (e.g., instrument software version):	6.30.00609 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series), 10.00.03708 (UXR-Series) Oscilloscope
File Name:	SetupInfPCIExpress0430.exe

Addition

- Support UXR-Series
- Added AC-CM voltage tests for 16GT/s Base Transmitter Tests in Common Mode Voltage tests
- Integrated SigTest version 4.0.39 * refer to Notes 1 & 2
- SigTest version selection (Debug Mode) in each Data Speed
- Re-categories tests as Near End and Far End

Modification

- De-emphasis option for 5GT/s test no longer available in Workshop Compliance Mode. Both -3.5dB and -6.0dB de-emphasis tests will appear in test list together
- Fixed de-embedded package file issue for CEM End Point and Root Complex tests
- Fixed incorrect Non-Transition Eye image and label in 16GT/s test reports
- Fixed test limit for 5GT/s Non-Transition voltage measurement
- Fixed tests missing issue in Use saved waveform and Debug mode
- Fixed missing lower limit issue when Half Power option being chosen
- Prompt user for bandwidth changed due to sampling rates requirements
- Fixed test report missing Preset Type issue
- Fixed and improved general GUI issue
- Fixed general issue for Use saved waveform mode

- Fixed general test sequence, measurement and SigTest template files issue

Known Issues

- SigTest version 4.0.39 did not work for 5GT/s tests. Version 4.0.37 will be used for 5GT/s tests
- SigTest version 3.2.0.1 did not work for Base Transmitter and End Point Template Test
- Temporary hide Uncorrelated Total Pulse Width Jitter and Uncorrelated Deterministic Pulse Width Jitter tests due to no workable SigTest version available
- This application only able to process differential waveform when it is Saved Waveform mode of Equalization Preset Test. The differential waveform file directory / path MUST NOT contain any empty space because it will cause SigTest crashed.

Notes 1 – 5GT/s tests still using SigTest version 4.0.37. Root Complex tests still using SigTest version 3.2.0.1

Notes 2 – PCIE 3.0 and PCIE 4.0 Equalization Preset Tests using SigTest version 4.0.37

KEYSIGHT

Keysight N5393F/N5393G Software Version 04.20

Released Date:	6 July 2018
Requirements category (e.g., operating system):	Microsoft Windows 7
Requirements category (e.g., instrument software version):	6.20.00701 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series), 6.00.00625 (S-Series) Oscilloscope
File Name:	SetupInfPCIExpress0420.exe

Addition

- Added Gen4 CEM EndPoint Tests
- Added CEM Rootcomplex Tests

Modification

- Fixed Preset test for Gen3.
- Fixed Gen3 8GT/s RefClk RMS Jitter test in offline test
- Revised 81150A setup.
- Added Setup for 81150A using remote command.
- Fixed Tx, Full swing Tx voltage with no TxEQ (16.0 GT/s) not running due to no waveform loaded
- For Gen3 add in card and system board, added additional check on template path because it can be change from setup tab and configure tab
- Fixed the conflict setting on CEM-End point and CEM system on Gen 3 (S-parameter path)
- Default lane0 as checked
- Added back offline capability for preset test.
- When run Preset test in offline, allow to browse to the dedicate file directory instead of file selection.
- Changed 5G test Non transition test to Informative Only. (Both Full Power and half power)
- Fixed error (input string not in correct format) in Median to Max Jitter (2.5 GT/s).

- Extend the timeout for waveform saving process as the default timeout will not enough for large waveform file.
- Increase the looping number (Dut toggle) due to additional preset pattern in Gen4 DUT.
- Fixed U2.endpoint test for 5G not being hide when uncheck the 5G checkbox
- Revised the result reporting format for eye width test.
- Exposed SRIS option if Gen4 being selected, it should be visible on all speed.
- EndPoint Eye Width test (-6dB) reported with an actual limit instead of Pass/Fail
- Fixed connection Diagram not being display on PCIe1 root complex test
- Removed rise/Fall time measurement on Gen3 and Gen4.

KEYSIGHT

Keysight N5393F/N5393G Software Version 04.11

Released Date:	20 April 2018
Requirements category (e.g., operating system):	Microsoft Windows 7
Requirements category (e.g., instrument software version):	6.00.00625 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series), 6.00.00625 (S-Series) Oscilloscope
File Name:	SetupInfPCIExpress0411.exe

Additions

- Added different limits for reference clock tests with SSC and without SSC.
- Added configuration to allow SigTest to run in silent mode.
- Added AC Common Mode Voltage – 30kHz to 500MHz (5.0GT/s) as per PCIE 3 Base Specification.
- Enabled DUT automation for U.2 tests.
- Reported Preset# for 8GT/s and 16GT/s signal quality tests respectively in HTML report.
- Added instruction for user to use DC Blocks when toggling DUT test mode using 81150A/60A.

Modifications

- Renamed AC Common Mode Voltage (5.0GT/s) to AC Common Mode Voltage – 2.5GHz LPF (5.0GT/s). New limit applied.
- Changed Tx Full Swing with no TxEQ test to use only Preset#4.
- Waveform (*.bin) files will be saved in PlugfestWfm folder.
- Updated label for 8.0GT/s and 16GT/s ref clock tests result table.
- Changed all PCIE 2.0 and PCIE 1.1 EndPoint and RootComplex end point tests to use same connection diagram as PCIE 3.0.
- Changed clock recovery to 2nd Order PLL when measuring rise fall time in Gen 2 5GT/s.
- Deployed SigTest 4.0.37.

Keysight N5393F/N5393G Software Version 04.10

Released Date:	29 Mar 2017
Requirements category (e.g., operating system):	Microsoft Windows 7
Requirements category (e.g., instrument software version):	6.00.00625 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series), 6.00.00625 (S-Series) Oscilloscope
File Name:	SetupInfPCIExpress0410.exe

Additions

- Add support for Infiniium Oscilloscope Software version 6.0.
- Cut in updated template and s-parameter files for U2 tests.
- Added new test limit for Peak Differential Output Voltage (Transition and Non Transition) Root End Point for PCIE 3.0.

KEYSIGHT

Keysight N5393F/N5393G Software Version 04.00

Released Date:	10 Mar 2017
Requirements category (e.g., operating system):	Microsoft Windows 7
Requirements category (e.g., instrument software version):	5.75.00402 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series), 5.75.00402 (S-Series) Oscilloscope
File Name:	SetupInfPCIExpress0400.exe

Additions

- Added Transmitter tests for PCIE G4 Base Specification 0.7.
    - Speed supported: 16GT/s, 8.0GT/s, 5.0GT/s and 2.5GT/s
- Added Reference Clock tests for PCIE G4 Base Specification 0.7.
- Added PCIE G3 U.2 Connector Transmitter tests
    - Speed supported: 8.0GT/s, 5.0GT/s and 2.5GT/s
- Added DUT Automation.
- Added Workshop Compliance Mode.

Keysight N5393D/N5393E Software Version 03.45

Released Date:	13 January 2017
Requirements category (e.g., operating system):	Microsoft Windows 7
Requirements category (e.g., instrument software version):	5.70.00802 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series), 5.00 (9000 Series) Oscilloscope
File Name:	SetupInfPCIExpress0345.exe

Modifications

- Fixed the following test issues
    - ExpressCard eye mask test folding issue.
    - Equalization Preset test units.
    - Missing test when offline feature is turn on.

KEYSIGHT

Keysight N5393D/N5393E Software Version 03.44

Released Date:	8 April 2016
Requirements category (e.g., operating system):	Microsoft Windows 7
Requirements category (e.g., instrument software version):	5.00 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series), 5.00 (9000 Series) Oscilloscope
File Name:	SetupInfPCIExpress0344.exe

Additions

- Added differential probe support for PCIE Gen2 Receiver Common Clk tests.

Modifications

- Fixed the following test issues
    - Updated P10 limit.
    - Updated minimum Eye Height in PCIE Gen 2 System Board, Peak Differential Output Voltage test.
    - Added connection type in PCIE Gen 2 Transmitter test.
    - Updated the acquisition depth for PCIE Gen 1 Reference Clock, Average Clock Period test to 10Mpts.

Keysight N5393D/N5393E Software Version 03.43

Released Date:	17 August 2015
Requirements category (e.g., operating system):	Microsoft Windows 7
Requirements category (e.g., instrument software version):	4.60 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series), 4.60 (9000 Series) Oscilloscope
File Name:	SetupInfPCIExpress0343.exe

Additions

- Added new test for PCIE 2.0 (5.0 G/Ts).
    - Tmin-Pulse
    - AC Peak Common Mode Output Voltage
    - Absolute delta of DC common mode voltage during L0 and Idle

Modifications

- Fixed the following test issues
    - Add-in Card and System Board RMS RJ pass fail limit
    - PCIE Gen 1 Unit Interval test report actual value using worst case value.
    - Uninstall others Valiframe application issue.
    - Does not allow offset signal for AVG Common Mode Output Voltage test.

KEYSIGHT

Agilent N5393D/N5393E Software Version 03.42

Released Date:	24 November 2014
Requirements category (e.g., operating system):	Microsoft Windows 7
Requirements category (e.g., instrument software version):	4.60 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series), 4.60 (9000 Series) Oscilloscope
File Name:	SetupInfPCIExpress0342.exe

Additions

- Enabled PCIE Gen 1 supports for S-Series scope.
- Added additional info report for Template Test.
- (Max Voltage, Min Voltage, Eye Top Margin, Eye Bottom Margin, Eye Height, Eye Height Margin)

Modifications

- Fixed the following test issues
    - Add-in Card and System Board RMS RJ pass fail limit
    - Wrong Transmitter PCIE2.0 (5GT/s) Eye-width value reported
    - SigTestWrapper crash when input not compliance signal
    - System Board 5GT/s template test limit

Agilent N5393D/N5393E Software Version 03.41

Released Date:	8 August 2014
Requirements category (e.g., operating system):	Microsoft Windows 7
Requirements category (e.g., instrument software version):	4.60 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series), 4.60 (9000 Series) Oscilloscope
File Name:	SetupInfPCIExpress0341.exe

Additions

- Supports HDF5 format.

Modifications

- Fixed the following test issues
    - Exception throw from Switch matrix
    - Reference Clock Number of UI processed cycles
    - De embed fixture is System Board
    - Unclean eye diagram

KEYSIGHT

Agilent N5393D/N5393E Software Version 03.40

Released Date:	2 June 2014
Requirements category (e.g., operating system):	Microsoft Windows 7
Requirements category (e.g., instrument software version):	4.60 (90000 Series, 90000 X-Series, 90000 Q-Series, Z-Series), 4.60 (9000 Series) Oscilloscope
File Name:	SetupInfPCIExpress0340.exe

Modifications

- Supports for Infiniium Oscilloscope Software version 5.00.

Agilent N5393C Software Version 03.35

Released Date:	1 June 2014
Requirements category (e.g., operating system):	Microsoft Windows XP, Microsoft Windows 7
Requirements category (e.g., instrument software version):	3.60 (90000 Series, 90000 X-Series) Oscilloscope
File Name:	SetupInfPCIExpress0335.exe

Modifications

- Fixed bug that unable to turn on Switch Matrix

Note

- This will be the last version to support Infiniium Oscilloscope Baseline Version 4.20.

KEYSIGHT

Agilent N5393C Software Version 03.34

Released Date:	19 May 2014
Requirements category (e.g., operating system):	Microsoft Windows XP, Microsoft Windows 7
Requirements category (e.g., instrument software version):	3.60 (90000 Series, 90000 X-Series) Oscilloscope
File Name:	SetupInfPCIExpress0334.exe

Modifications

- Improved algorithm and updated the limit for SSC deviation test in PCIE 2 and PCIE 3
- Improved algorithm for Peak Differential Output Voltage (Transition and Non-Transition) in PCIE 1, PCIE 2 and PCIE 3.
- Fixed the following test issue
    - Absolute Crossing Point Voltage test in PCIE 1.1
    - Receiver calibration setup in PCIE 3
    - De-emphasis ratio test in PCIE 1 and PCIE 2
    - Common clock filter in PCIE 2

Note

- This will be the last version to support Infiniium Oscilloscope Baseline Version 4.20.

Agilent N5393C Software Version 03.33

Released Date:	13 December 2013
Requirements category (e.g., operating system):	Microsoft Windows XP, Microsoft Windows 7
Requirements category (e.g., instrument software version):	3.60 (90000 Series, 90000 X-Series) Oscilloscope
File Name:	SetupInfPCIExpress0333.exe

Modifications

- Separate the Peak Differential Output Voltage to Peak Differential Output Voltage Transition and Peak Differential Output Voltage Non Transition
- Changed the Template test limit format
- Improve algorithm for PCIE 1 Template test

KEYSIGHT

Agilent N5393C Software Version 03.32

Released Date:	16 July 2013
Requirements category (e.g., operating system):	Microsoft Windows XP, Microsoft Windows 7
Requirements category (e.g., instrument software version):	3.60 (90000 Series, 90000 X-Series) Oscilloscope
File Name:	SetupInfPCIExpress0332.exe

Modifications

- Support MSOX90000 Series Oscilloscopes
- Added Interpolation configuration for PCIE1 and PCIE2.

Agilent N5393C Software Version 03.31

Released Date:	7 June 2013
Requirements category (e.g., operating system):	Microsoft Windows XP, Microsoft Windows 7
Requirements category (e.g., instrument software version):	3.60 (90000 Series, 90000 X-Series) Oscilloscope
File Name:	SetupInfPCIExpress0331.exe

Modifications

- Fixed bug that caused the application to crash when no switch matrix license is installed.

KEYSIGHT

Agilent N5393C Software Version 03.30

Released Date:	20 May 2013
Requirements category (e.g., operating system):	Microsoft Windows XP, Microsoft Windows 7
Requirements category (e.g., instrument software version):	3.60 (90000 Series, 90000 X-Series) Oscilloscope
File Name:	SetupInfPCIExpress0330.exe

Modifications

- Enabled switch matrix capability.
- Enabled precision probe capability.

Agilent N5393C Software Version 03.21

Released Date:	26 February 2013
Requirements category (e.g., operating system):	Microsoft Windows XP, Microsoft Windows 7
Requirements category (e.g., instrument software version):	3.60 (90000 Series, 90000 X-Series) Oscilloscope
File Name:	SetupInfPCIExpress0321.exe

Modifications

- Set default sampling rate to 40Gsa/s during startup so that bandwidth limit is at 16GHz instead of 8GHz.
- Implement correct limits for Peak Differential Output Voltage for PCIE 3.0 Add-in Card.

KEYSIGHT

Agilent N5393C Software Version 03.20

Released Date:	22 November 2012
Requirements category (e.g., operating system):	Microsoft Windows XP, Microsoft Windows 7
Requirements category (e.g., instrument software version):	3.50 (90000 Series) Oscilloscope
File Name:	SetupInfPCIExpress0320.exe

Additions

- PCIE 3.0 Receiver Calibration.
- PCIE 3.0 Receiver Test Setup.

Modifications

- Changed de-emphasis ratio measurement to use eye-diagram and histogram
- Implement correct mask limits for eye measurement for signals with 3.5dB and 6.5dB ratios.
- Improved rise/fall time measurements for variable transition time threshold to get better accuracy.

Agilent N5393C Software Version 03.10

Released Date:	19 April 2012
Requirements category (e.g., operating system):	Microsoft Windows XP, Microsoft Windows 7
Requirements category (e.g., instrument software version):	3.22.0004 (90000 Series) Oscilloscope
File Name:	SetupInfPCIExpress0310.exe

Additions

- PCIE 3.0 Add-in Card tests.
- PCIE 3.0 System Board tests.

Modifications

- Fixed bug that caused Template test to hang.
- Fixed bug that caused Reference Clock test to crash.

KEYSIGHT

Agilent N5393C Software Version 03.02

Released Date:	5 July 2011
Requirements category (e.g., operating system):	Microsoft Windows XP, Microsoft Windows 7
Requirements category (e.g., instrument software version):	3.00.900 (90000 Series) Oscilloscope
File Name:	SetupInfPCIExpress0302.exe

Modifications

- Fixed bug that caused Template test to crash for PCIE 2.0.
- Fixed bug that caused connection diagrams to be blank.
- Improved algorithm for PCIE 2.0 Reference clock tests.

Agilent N5393C Software Version 03.00

Released Date:	24 December 2010
Requirements category (e.g., operating system):	Microsoft Windows XP, Microsoft Windows 7
Requirements category (e.g., instrument software version):	3.00.900 (90000 Series) Oscilloscope
File Name:	SetupInfPCIExpress0300.exe

Additions

- PCIE 3.0 Transmitter tests.
- PCIE 3.0 Reference clock tests.
- PCIE 2.0 Reference clock tests.

KEYSIGHT

Agilent N5393B Software Version 02.12

Released Date:	27 March 2009
Requirements category (e.g., operating system):	Microsoft Windows XP
Requirements category (e.g., instrument software version):	1.40.04 (90000 Series) Oscilloscope 5.60.00 (80000 Series) Oscilloscope
File Name:	SetupInfPCIExpress0212.exe

Additions

- Added support for PCIE half swing power tests.

Modifications:

- Fixed issue in PCIE clock recovery method.
- Fixed bug where certain tests pass with infinity value.

Agilent N5393B Software Version 02.10

Released Date:	03 March 2008
Requirements category (e.g., operating system):	Microsoft Windows XP
Requirements category (e.g., instrument software version):	1.00.00 (90000 Series) Oscilloscope 5.40.00 (80000 Series) Oscilloscope
File Name:	SetupInfPCIExpress0210.exe

Additions

- Added support for DSO90000 Series Oscilloscopes.

Agilent N5393B Software Version 02.00

Released Date:	17 January 2009
Requirements category (e.g., operating system):	Microsoft Windows XP
Requirements category (e.g., instrument software version):	5.40.00 (80000 Series) Oscilloscope
File Name:	SetupInfPCIExpress0200.exe

- Additions
- Added tests for PCIE 2.0.

Modifications:

- Modified the Unit Interval test to calculate and report the mean unit interval value for the entire sample waveform.
- Updated the System board tests for PCIE 2.0 to support the new 2-port testing as specified in the PCIE CEM specification document version 2.0.

Agilent N5393A Software Version 01.12

Released Date:	28 September 2007
Requirements category (e.g., operating system):	Microsoft Windows XP
Requirements category (e.g., instrument software version):	5.20.00 (80000 Series) Oscilloscope
File Name:	SetupInfPCIExpress0112.exe

Bug Fixed

- Fixed bug in Peak Differential Output Voltage test which caused occasional wrong results.
- Fixed bug in DC Common Mode Line Delta test which caused Line Delta to be computed incorrectly and displayed “VTX-CM-DC-D+” or “VTX-CM-DC-D-” as signed values instead of absolute values.
- Fixed incorrect specification limit from 25V to 25mV in the 2.0 version of DC Common Mode Line Delta test.

KEYSIGHT

Agilent N5393A Software Version 01.11

Released Date:	22 May 2007
Requirements category (e.g., operating system):	Microsoft Windows XP
Requirements category (e.g., instrument software version):	5.20.00 (80000 Series) Oscilloscope
File Name:	SetupInfPCIExpress0111.exe

Modifications:

- Changed default sample rate to 40GSa/s for PCIE 2.0 and 20GSa/s for PCIE 1.0a, 1.1, & Express Card.

Bug fixed:

- Fixed Set Up page selection of Express Card test where previously the Module tests and Host tests were swapped in the test tree display.
- Fixed defect that caused an error dialog "Error Setting Sample Rate Valid Range" to appear on scopes that did not have the EBW option.

Agilent N5393A Software Version 01.10

Released Date:	9 February 2007
Requirements category (e.g., operating system):	Microsoft Windows XP
Requirements category (e.g., instrument software version):	5.20.00 (80000 Series) Oscilloscope
File Name:	SetupInfPCIExpress0110.exe

Additions

- Added tests for PCIE 1.1.
- Added some preliminary "teaser" tests for PCIE 2.0.

KEYSIGHT

Agilent N5393A Software Version 01.03

Released Date:	N/A
Requirements category (e.g., operating system):	Microsoft Windows XP
Requirements category (e.g., instrument software version):	A.03.90
File Name:	N/A

Modifications

- Improved signal detection routines to handle signals with large common mode voltage.

Bug Fixed

- Fixed an issue introduced in 1.02 that broke the Tx DC Common Mode Measurements by producing very large common mode voltage values.
- Fixed the issue that was causing AVG DC common mode voltage to measure infinity value when the common mode voltage was larger than 400mV.

Agilent N5393A Software Version 01.02

Released Date:	30 January 2006
Requirements category (e.g., operating system):	Microsoft Windows XP
Requirements category (e.g., instrument software version):	A.03.90
File Name:	SetupInfPCIExpress0102.exe

Additions

- Added user control to disable signal checks.

Modifications

- Enhanced dynamic range for some tests to accommodate marginal signals.
- Modified Peak Voltage Test method in order to correctly compute Vpeak over the entire waveform (instead of just mid-ui).

Bug Fixed

- Corrected typo in SSC UI limits (minor precision error).

KEYSIGHT

Agilent N5393A Software Version 01.01

Released Date:	17 February 2006
Requirements category (e.g., operating system):	Microsoft Windows XP
Requirements category (e.g., instrument software version):	A.03.90
File Name:	SetupInfPCIExpress0101.exe

Additions

- Added support for Spread Spectrum Clocking (SSC).
- Added support for DS080000 Series Oscilloscopes.
- Added support for changing the sample rate option.
- Added the Enhanced Bandwidth option for DSO80000 series scopes (used for Noise Reduction at 6GHz).

Modifications

- Modified the Unit Interval algorithm to improve performance on low amplitude signals.

Bug Fixed

- Fixed the issue in html output report where clicking the hyperlinks at the top of the report would not navigate to the details for that test.
- Provided a workaround for a known bug in WindowsXP Compressed folders to allow the viewer to see image files.

Agilent N5393A Software Version 01.00

Released Date:	14 June 2006
Requirements category (e.g., operating system):	Microsoft Windows XP
Requirements category (e.g., instrument software version):	A.03.50
File Name:	SetupInfPCIExpress0100.exe

Initial Release

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Appendix A

Tests no longer consist of prerequisite test

PCIE Gen	Data Rates	Test Name & ID
1.0a	2.5GT/s	Tx, Median to Max Jitter 2
1.0a	2.5GT/s	Tx, Median to Max Jitter (Low Power) 10002
1.0a	2.5GT/s	Tx, Eye Width 3
1.0a	2.5GT/s	Tx, Eye Width (Low Power) 10003
1.0a	2.5GT/s	Tx, Deemphasized Voltage Ratio 5
1.0a	2.5GT/s	Tx, Peak Differential Output Voltage (Transition) 7
1.0a	2.5GT/s	Tx, Peak Differential Output Voltage (Transition) (Low Power) 10007
1.0a	2.5GT/s	RootComplex Tests, Median to Max Jitter 402
1.0a	2.5GT/s	RootComplex Tests, Eye-Width 403
1.0a	2.5GT/s	EndPoint Tests, Median to Max Jitter 202
1.0a	2.5GT/s	EndPoint Tests, Eye-Width 203
1.0a	2.5GT/s	Rx, Median to Max Jitter 102
1.0a	2.5GT/s	Rx, Eye-Width 103
1.1, 2.0	2.5GT/s	Rx, Median to Max Jitter 1220
1.1, 2.0	2.5GT/s	Rx, Eye-Width 1230
1.1, 2.0, 3.0, 4.0	2.5GT/s	EndPoint Tests, Median to Max Jitter 1320

1.1, 2.0, 3.0, 4.0	2.5GT/s	EndPoint Tests, Eye-Width 1330
1.1, 2.0, 3.0, 4.0	2.5GT/s	RootComplex Tests, Median to Max Jitter 1420
1.1, 2.0, 3.0, 4.0	2.5GT/s	RootComplex Tests, Eye-Width 1430
2.0	5.0GT/s	Rx, Data Clocked Architecture Peak Differential Input Voltage 2241
2.0	5.0GT/s	Rx, Common Refclk Architecture Peak Differential Input Voltage 2243

KEYSIGHT

Test ID & Name changes

Base - Transmitter Test (2.5 GT/s)

PCIE Gen	Data Rates	Test Name & ID in 4.50.0.0	Test Name & ID in 4.60.0.0
1.0a	2.5GT/s	DC Common Mode Line Delta 9	Absolute delta of DC common mode voltage between D+ and D- 9
1.0a	2.5GT/s	N/A	Tx, Absolute delta of DC common mode voltage during L0 and Idle 60
1.1, 2.0	2.5GT/s	Peak Differential Output Voltage (Non Transition) 11400	Peak Differential Output Voltage (Non Transition) 21400
1.1	2.5GT/s	Peak Differential Output Voltage (Non Transition) (Low Power) 11140	Peak Differential Output Voltage (Non Transition) (Low Power) 11141
1.1, 2.0, 3.0, 4.0	2.5GT/s	DC Common Mode Line Delta 1184	Absolute delta of DC common mode voltage between D+ and D- 1184
1.1, 2.0, 3.0, 4.0	2.5GT/s	N/A	Tx, Absolute delta of DC common mode voltage during L0 and Idle 1040
2.0, 3.0, 4.0	2.5GT/s	Peak Differential Output Voltage (Low Power) 11140	Peak Differential Output Voltage (Transition) (Low Power) 11140
2.0, 3.0, 4.0	2.5GT/s	N/A	Peak Differential Output Voltage (Non Transition) (Low Power) 11401
4.0	2.5GT/s	Median to Max Jitter 1120	Median to Max Jitter 41120
4.0	2.5GT/s	Median to Max Jitter (Low Power) 11120	Median to Max Jitter (Low Power) 411120
4.0	2.5GT/s	RMS AC Peak Common Mode Output Voltage 1170	RMS AC Peak Common Mode Output Voltage 41170
4.0	2.5GT/s	N/A	Tx, AC Peak Common Mode Output Voltage - 1.25GHz LPF 41171
4.0	2.5GT/s	N/A	Tx, AC common mode voltage - 30kHz to 500MHz

			41172

Base - Transmitter Test (5.0 GT/s)

PCIE Gen	Data Rates	Test Name & ID in 4.50.0.0	Test Name & ID in 4.60.0.0
2.0, 3.0, 4.0	5GT/s	Peak Differential Output Voltage (Transition) 2144	Peak Differential Output Voltage -3.5dB (Transition) 2144
2.0	5GT/s	Peak Differential Output Voltage (Non Transition) 2154	Peak Differential Output Voltage -3.5dB (Non Transition) 2159
2.0	5GT/s	Eye Width 2134	Eye Width -3.5dB 2134
2.0, 3.0, 4.0	5GT/s	NA	Peak Differential Output Voltage -6.0dB (Transition) 2145
2.0	5GT/s	NA	Peak Differential Output Voltage -6.0dB (Non Transition) 2158
2.0, 3.0	5GT/s	NA	Eye Width -6.0dB 2135
2.0, 3.0	5GT/s	NA	Eye Width (Low Power) 2234
2.0, 3.0, 4.0	5GT/s	DC Common Mode Line Delta 2184	Absolute delta of DC common mode voltage between D+ and D- 2184
2.0	5GT/s	AC common mode voltage - 2.5GHz LPF 3170	AC common mode voltage 3171
2.0	5GT/s	AC common mode voltage - 30kHz to 500MHz 3175	NA
2.0, 3.0, 4.0	5GT/s	Short Name: AC Peak Common Mode Output Voltage (2.5GHz) 3170	Short Name: AC-CM voltage (2.5GHz LPF) 3170
3.0, 4.0	5GT/s	Peak Differential Output Voltage (Non Transition) 2154	Peak Differential Output Voltage -3.5dB (Non Transition) 2154
3.0	5GT/s	NA	Eye Width -3.5dB 2134

3.0, 4.0	5GT/s	NA	Peak Differential Output Voltage -6.0dB (Non Transition) 2155
4.0	5GT/s	Tmin-pulse 2152	Tmin-pulse 42152
4.0	5GT/s	Eye Width 42134	Eye Width -3.5dB 42134
4.0	5GT/s	NA	Eye Width -6.0dB 42135

Base - Transmitter Test (8.0 GT/s)

PCIE Gen	Data Rates	Test Name & ID in 4.50.0.0	Test Name & ID in 4.60.0.0
3.0	8GT/s	Reduced swing Tx voltage with no TxEQ 13060	Reduced swing Tx voltage with no TxEQ 13061

Base – Receiver Test (All Data Rates)

PCIE Gen	Data Rates	Test Name & ID in 4.50.0.0	Test Name & ID in 4.60.0.0
1.1 & 2.0	2.5GT/s	NA	Template Test 1210

CEM – End Point Test (All Data Rates)

PCIE Gen	Data Rates	Test Name & ID in 4.50.0.0	Test Name & ID in 4.60.0.0
1.0a	2.5GT/s	Peak Differential Output Voltage 207	Peak Differential Output Voltage (Non Transition) 207
1.0a	2.5GT/s	N/A	Peak Differential Output Voltage (Transition) 297
1.1	2.5GT/s	Peak Differential Output Voltage (Transition) 1340	Peak Differential Output Voltage (Transition) 1297
1.1	2.5GT/s	Peak Differential Output Voltage (Non Transition) 1350	Peak Differential Output Voltage (Non Transition) 1207

3.0 & 4.0	5GT/s	RJ RMS (with crosstalk) (ps) (-3.5dB) 2382	RJ RMS (with crosstalk) (ps) (-3.5dB) 238200
3.0 & 4.0	5GT/s	RJ RMS (without crosstalk) (ps) (-3.5dB) 2383	RJ RMS (without crosstalk) (ps) (-3.5dB) 238300
3.0 & 4.0	5GT/s	RJ RMS (with crosstalk) (ps) (-6.0dB) 2384	RJ RMS (with crosstalk) (ps) (-6.0dB) 238400
3.0 & 4.0	5GT/s	RJ RMS (without crosstalk) (ps) (-6.0dB) 2385	RJ RMS (without crosstalk) (ps) (-6.0dB) 238500
4.0	8GT/s	Peak Differential Output Voltage (Transition) 4320	Peak Differential Output Voltage (Transition) 44200
4.0	8GT/s	Peak Differential Output Voltage (Non Transition) 4321	Peak Differential Output Voltage (Non Transition) 44201
4.0	8GT/s	Template Test 3410	Template Test 43410

CEM – Root Complex Test (All Data Rates)

PCIE Gen	Data Rates	Test Name & ID in 4.50.0.0	Test Name & ID in 4.60.0.0
1.0a	2.5GT/s	Peak Differential Output Voltage 407	Peak Differential Output Voltage (Non Transition) 407
1.0a	2.5GT/s	N/A	Peak Differential Output Voltage (Transition) 497
1.1	2.5GT/s	Peak Differential Output Voltage (Transition) 1440	Peak Differential Output Voltage (Transition) 1497
1.1	2.5GT/s	Peak Differential Output Voltage (Non Transition) 1450	Peak Differential Output Voltage (Non Transition) 1407
3.0, 4.0	5GT/s	Random Jitter (with crosstalk) 2482	Random Jitter (with crosstalk) 248200
3.0, 4.0	5GT/s	Random Jitter (without crosstalk) 2483	Random Jitter (without crosstalk) 248300

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Appendix B

“Non Transtion” Test Name correction

PCIE Gen	Data Rates	Test Name & ID in 4.60.0.0	Test Name & ID in 4.70.0.0
4.0	8.0GT/s	Peak Differential Output Voltage (Non Transtion) 44201	Peak Differential Output Voltage (Non Transition) 44201
3.0	8.0GT/s	Peak Differential Output Voltage (Non Transtion) 3421	Peak Differential Output Voltage (Non Transition) 3421
3.0	8.0GT/s	Peak Differential Output Voltage (Non Transtion) 38003	Peak Differential Output Voltage (Non Transition) 38003

Appendix C

Update on Informative Test

PCIE Gen	Data Rates	Test Name & ID in 4.60.0.0	Test Name & ID in 4.70.0.0
3.0	5.0GT/s	Tx, Template Tests (5.0 GT/s, Low Power) 21140	Tx, Template Tests (5.0 GT/s, Low Power) 321140

Appendix D

Eye Width Test Name & Test Result Descriptor Standardization

PCIE Gen	Data Rates	Test Name & ID in 4.70.0.0	Test Name & ID in 4.70.9.0
4.0	16.0GT/s	RootComplex Tests, Eye Width (16.0 GT/s) 4540	RootComplex Tests, Eye-Width (16.0 GT/s) 4540
PCIE Gen	**Data Rates**	**Test ID & Test Result Descriptor in 4.70.0.0**	**Test ID & Test Result Descriptor in 4.70.9.0**
4.0	16.0GT/s	4540 Eye Width (G4, RootComplex, 16GT/s)	4540 Eye-Width (G4, RootComplex, 16GT/s)
4.0	16.0GT/s	4440 Eye Width (G4, EndPoint, 16GT/s)	4440 Eye-Width (G4, EndPoint, 16GT/s)
3.0, 4.0	8.0GT/s	3430 Eye Width (G3, EndPoint, 8GT/s)	3430 Eye-Width (G3, EndPoint, 8GT/s)

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Appendix E

PCIE Gen 3.0 Pseudo Package Loss 8.0 GT/s

PCIE Gen	Data Rate	Test Name & ID in 4.71.9.0	Test Name & ID in 4.80.0.0
3.0	8.0 GT/s	Pseudo package loss (8.0 GT/s Root device) 3140 Informative test	Pseudo package loss (8.0 GT/s) 3140 Limits added per specification
3.0	8.0 GT/s	Pseudo package loss (8.0 GT/s Non-root device) 314000 Informative test	Test Removed

Pass Limits Reporting Change

Changes in 4.80.0.0: Pass Limits as manual margin Pass / Fail.

PCIE Gen	Data Rate	Test ID	Test Name
2.0	5GT/s	110	Rx, Template Test (2.5 GT/s)
1.0a	2.5GT/s	210	EndPoint Tests, Template Tests (2.5 GT/s)
1.1	2.5GT/s	1210	Rx, Template Test (2.5 GT/s)
1.1	2.5GT/s	1310	EndPoint Tests, Template Tests (2.5 GT/s)
2.0	5GT/s	2316	EndPoint Tests, Template Tests -3.5dB (5.0 GT/s)
2.0	5GT/s	2318	EndPoint Tests, Template Tests -6.0dB (5.0 GT/s)
4.0	16.0GT/s	4410	EndPoint Tests, Template Tests (16.0 GT/s)
4.0	16.0GT/s	4510	RootComplex Tests, Template Tests (16.0 GT/s)

4.0	16.0GT/s	5029	RootComplex Tests - SigTest (16.0 GT/s) - Far End
3.0	2.5GT/s	12110	Tx, Template Tests (2.5 GT/s, Low Power)
1.1	2.5GT/s	18001	U.2 EndPoint Tests, Template Tests (2.5 GT/s)
2.0	5GT/s	21140	Tx, Template Tests (5.0 GT/s, Low Power)
2.0	5GT/s	21141	Tx, Template Tests -3.5dB (5.0 GT/s)
2.0	5GT/s	21142	Tx, Template Tests -6.0dB (5.0 GT/s)
2.0	5GT/s	28001	U.2 EndPoint Tests, Template Tests -3.5dB (5.0 GT/s)
2.0	5GT/s	28005	U.2 EndPoint Tests, Template Tests -6.0dB (5.0 GT/s)

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Jitter Tests Value Reporting Change

Changes in 4.80.0.0: Below jitter tests will be reported as zero if the value is calculated as negative.

PCIE Gen	Data Rate	Test ID	Test Name
1.0a	2.5 GT/s	2	Tx, Median to Max Jitter (2.5 GT/s)
1.0a	2.5 GT/s	102	Rx, Median to Max Jitter (2.5 GT/s)
1.0a	2.5 GT/s	202	EndPoint Tests, Median to Max Jitter (2.5 GT/s)
1.0a	2.5 GT/s	402	RootComplex Tests, Median to Max Jitter (2.5 GT/s)
1.1	2.5 GT/s	1090	Tx, Uncorrelated total jitter (2.5 GT/s)
1.1	2.5 GT/s	1101	Tx, Uncorrelated deterministic jitter (2.5 GT/s)
1.1	2.5 GT/s	1102	Tx, Total uncorrelated PWJ (2.5 GT/s)
1.1	2.5 GT/s	1103	Tx, Deterministic DjDD uncorrelated PWJ (2.5 GT/s)
1.1	2.5 GT/s	1104	Tx, Data dependent jitter (2.5 GT/s)
1.1	2.5 GT/s	1106	Tx, Random jitter RMS (2.5 GT/s)
1.1	2.5 GT/s	1120	Tx, Median to Max Jitter (2.5 GT/s)
1.1	2.5 GT/s	1220	Rx, Median to Max Jitter (2.5 GT/s)
1.1	2.5 GT/s	1320	EndPoint Tests, Median to Max Jitter (2.5 GT/s)
1.1	2.5 GT/s	1420	RootComplex Tests, Median to Max Jitter (2.5 GT/s)
2.0	5.0 GT/s	2000	Tx, Uncorrelated deterministic jitter (5.0 GT/s)
2.0	5.0 GT/s	2090	Tx, Uncorrelated total jitter (5.0 GT/s)
2.0	5.0 GT/s	2102	Tx, Total uncorrelated PWJ (5.0 GT/s)
2.0	5.0 GT/s	2103	Tx, Deterministic DjDD uncorrelated PWJ (5.0 GT/s)
2.0	5.0 GT/s	2104	Tx, Data dependent jitter (5.0 GT/s)
2.0	5.0 GT/s	2106	Tx, Random jitter RMS (5.0 GT/s)
2.0	5.0 GT/s	2120	Tx, Median to Max Jitter (2.5 GT/s)
2.0	5.0 GT/s	2192	Tx, Deterministic Jitter > 1.5 MHz (5.0 GT/s)
2.0	5.0 GT/s	2282	Rx, Data Clocked Architecture RMS Random Jitter (5.0 GT/s)
2.0	5.0 GT/s	2284	Rx, Common Refclk Architecture RMS Random Jitter (5.0 GT/s)
2.0	5.0 GT/s	2292	Rx, Data Clocked Architecture Maximum Deterministic Jitter (5.0 GT/s)
2.0	5.0 GT/s	2294	Rx, Common Refclk Architecture Maximum Deterministic Jitter (5.0 GT/s)
2.0	5.0 GT/s	2296	Rx, Data Clocked Architecture Total Jitter at BER-12 (5.0 GT/s)
2.0	5.0 GT/s	2298	Rx, Common Refclk Architecture Total Jitter at BER-12 (5.0 GT/s)
2.0	5.0 GT/s	2320	EndPoint Tests, Median to Max Jitter (2.5 GT/s)
2.0	5.0 GT/s	2382	EndPoint Tests, RMS Random Jitter -3.5dB with crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2383	EndPoint Tests, RMS Random Jitter -3.5dB without crosstalk (5.0 GT/s)

2.0	5.0 GT/s	2384	EndPoint Tests, RMS Random Jitter -6.0dB with crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2385	EndPoint Tests, RMS Random Jitter -6.0dB without crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2392	EndPoint Tests, Maximum Deterministic Jitter -3.5dB with crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2393	EndPoint Tests, Maximum Deterministic Jitter -3.5dB without crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2394	EndPoint Tests, Maximum Deterministic Jitter -6.0dB with crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2395	EndPoint Tests, Maximum Deterministic Jitter -6.0dB without crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2396	EndPoint Tests, Total Jitter at BER-12 -3.5dB with crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2397	EndPoint Tests, Total Jitter at BER-12 -3.5dB without crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2398	EndPoint Tests, Total Jitter at BER-12 -6.0dB with crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2399	EndPoint Tests, Total Jitter at BER-12 -6.0dB without crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2482	RootComplex Tests, RMS Random Jitter with crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2483	RootComplex Tests, RMS Random Jitter without crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2492	RootComplex Tests, Maximum Deterministic Jitter with crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2493	RootComplex Tests, Maximum Deterministic Jitter without crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2496	RootComplex Tests, Total Jitter at BER-12 with crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2497	RootComplex Tests, Total Jitter at BER-12 without crosstalk (5.0 GT/s)
3.0	8.0 GT/s	3090	Tx, Uncorrelated total jitter (8.0 GT/s)
3.0	8.0 GT/s	3100	Tx, Uncorrelated deterministic jitter (8.0 GT/s)
3.0	8.0 GT/s	3110	Tx, Total uncorrelated PWJ (8.0 GT/s)
3.0	8.0 GT/s	3120	Tx, Deterministic DjDD uncorrelated PWJ (8.0 GT/s)
3.0	8.0 GT/s	3130	Tx, Data dependent jitter (8.0 GT/s)
4.0	16.0 GT/s	4090	Tx, Uncorrelated total jitter (16.0 GT/s)
4.0	16.0 GT/s	4100	Tx, Uncorrelated deterministic jitter (16.0 GT/s)
4.0	16.0 GT/s	4110	Tx, Total uncorrelated PWJ (16.0 GT/s)
4.0	16.0 GT/s	4120	Tx, Deterministic DjDD uncorrelated PWJ (16.0 GT/s)
4.0	16.0 GT/s	4130	Tx, Data dependent jitter (16.0 GT/s)
4.0	16.0 GT/s	4160	Tx, Random jitter RMS (16.0 GT/s)
4.0	16.0 GT/s	4450	EndPoint Tests, Uncorrelated Total Pulse Width Jitter (16.0 GT/s)
4.0	16.0 GT/s	4460	EndPoint Tests, Uncorrelated Deterministic Pulse Width Jitter (16.0 GT/s)
1.0a	2.5 GT/s	10002	Tx, Median to Max Jitter (2.5 GT/s, Low Power)
1.0a	2.5 GT/s	11120	Tx, Median to Max Jitter (2.5 GT/s, Low Power)
1.0a	2.5 GT/s	12120	Tx, Median to Max Jitter (2.5 GT/s, Low Power)

3.0	2.5 GT/s	17002	U.2 RootComplex Tests, Median to Max Jitter (2.5 GT/s)
3.0	2.5 GT/s	18002	U.2 EndPoint Tests, Median to Max Jitter (2.5 GT/s)
3.0	5.0 GT/s	27005	U.2 RootComplex Tests, RMS Random Jitter with crosstalk (5.0 GT/s)
3.0	5.0 GT/s	27006	U.2 RootComplex Tests, Maximum Deterministic Jitter with crosstalk (5.0 GT/s)
3.0	5.0 GT/s	27007	U.2 RootComplex Tests, Total Jitter at BER-12 with crosstalk (5.0 GT/s)
3.0	5.0 GT/s	27009	U.2 RootComplex Tests, RMS Random Jitter without crosstalk (5.0 GT/s)
3.0	5.0 GT/s	27010	U.2 RootComplex Tests, Maximum Deterministic Jitter without crosstalk (5.0 GT/s)
3.0	5.0 GT/s	27011	U.2 RootComplex Tests, Total Jitter at BER-12 without crosstalk (5.0 GT/s)
3.0	5.0 GT/s	28009	U.2 EndPoint Tests, RMS Random Jitter -3.5dB with crosstalk (5.0 GT/s)
3.0	5.0 GT/s	28010	U.2 EndPoint Tests, Maximum Deterministic Jitter -3.5dB with crosstalk (5.0 GT/s)
3.0	5.0 GT/s	28011	U.2 EndPoint Tests, Total Jitter at BER-12 -3.5dB with crosstalk (5.0 GT/s)
3.0	5.0 GT/s	28013	U.2 EndPoint Tests, RMS Random Jitter -6.0dB with crosstalk (5.0 GT/s)
3.0	5.0 GT/s	28014	U.2 EndPoint Tests, Maximum Deterministic Jitter -6.0dB with crosstalk (5.0 GT/s)
3.0	5.0 GT/s	28015	U.2 EndPoint Tests, Total Jitter at BER-12 -6.0dB with crosstalk (5.0 GT/s)
3.0	5.0 GT/s	28017	U.2 EndPoint Tests, RMS Random Jitter -3.5dB without crosstalk (5.0 GT/s)
3.0	5.0 GT/s	28018	U.2 EndPoint Tests, Maximum Deterministic Jitter -3.5dB without crosstalk (5.0 GT/s)
3.0	5.0 GT/s	28019	U.2 EndPoint Tests, Total Jitter at BER-12 -3.5dB without crosstalk (5.0 GT/s)
3.0	5.0 GT/s	28021	U.2 EndPoint Tests, RMS Random Jitter -6.0dB without crosstalk (5.0 GT/s)
3.0	5.0 GT/s	28022	U.2 EndPoint Tests, Maximum Deterministic Jitter -6.0dB without crosstalk (5.0 GT/s)
3.0	5.0 GT/s	28023	U.2 EndPoint Tests, Total Jitter at BER-12 -6.0dB without crosstalk (5.0 GT/s)
4.0	2.5 GT/s	41120	Tx, Median to Max Jitter (2.5 GT/s)
4.0	8.0 GT/s	43090	Tx, Uncorrelated total jitter (8.0 GT/s)
4.0	8.0 GT/s	43100	Tx, Uncorrelated deterministic jitter (8.0 GT/s)
4.0	8.0 GT/s	43110	Tx, Total uncorrelated PWJ (8.0 GT/s)
4.0	8.0 GT/s	43120	Tx, Deterministic DjDD uncorrelated PWJ (8.0 GT/s)
4.0	8.0 GT/s	43130	Tx, Data dependent jitter (8.0 GT/s)
4.0	8.0 GT/s	43160	Tx, Random jitter RMS (8.0 GT/s)
3.0	5.0 GT/s	238200	EndPoint Tests, RMS Random Jitter -3.5dB with crosstalk (5.0 GT/s)
3.0	5.0 GT/s	238300	EndPoint Tests, RMS Random Jitter -3.5dB without crosstalk (5.0 GT/s)
3.0	5.0 GT/s	238400	EndPoint Tests, RMS Random Jitter -6.0dB with crosstalk (5.0 GT/s)

3.0	5.0 GT/s	238500	EndPoint Tests, RMS Random Jitter -6.0dB without crosstalk (5.0 GT/s)
3.0	5.0 GT/s	248200	RootComplex Tests, RMS Random Jitter with crosstalk (5.0 GT/s)
3.0	5.0 GT/s	248300	RootComplex Tests, RMS Random Jitter without crosstalk (5.0 GT/s)
4.0	2.5 GT/s	411120	Tx, Median to Max Jitter (2.5 GT/s, Low Power)

Deemphasized Voltage Ratio Tests Change

Changes in 4.80.0.0: Option to select SigTest (Default) or Infiniium measurement method.

PCIE Gen	Data Rate	Test ID	Test Name
1.0a	2.5 GT/s	5	Tx, Deemphasized Voltage Ratio (2.5 GT/s)
1.1	5.0 GT/s	2000	Tx, Uncorrelated deterministic jitter (5.0 GT/s)
3.0	2.5 GT/s	2160	Tx, Deemphasized Voltage Ratio (2.5 GT/s)
3.0	5.0 GT/s	2162	Tx, Deemphasized Voltage Ratio -3.5dB (5.0 GT/s)
3.0	5.0 GT/s	2164	Tx, Deemphasized Voltage Ratio -6.0dB (5.0 GT/s)
2.0	5.0 GT/s	216200	Tx, Deemphasized Voltage Ratio -3.5dB (5.0 GT/s)
4.0	5.0 GT/s	216201	Tx, Deemphasized Voltage Ratio -3.5dB (5.0 GT/s)
2.0	5.0 GT/s	216400	Tx, Deemphasized Voltage Ratio -6.0dB (5.0 GT/s)
3.0	5.0 GT/s	216401	Tx, Deemphasized Voltage Ratio -6.0dB (5.0 GT/s)

Peak Differential Output Voltage Tests Change

Changes in 4.80.0.0: Option to select SigTest (Default) or Infiniium measurement method.

PCIE Gen	Data Rate	Test ID	Test Name
1.0a	2.5GT/s	5	Tx, Peak Differential Output Voltage (Transition) (2.5 GT/s)
1.0a	2.5GT/s	70	Tx, Peak Differential Output Voltage (Non Transition) (2.5 GT/s)
1.0a	2.5GT/s	207	EndPoint Tests, Peak Differential Output Voltage (Non Transition) (2.5 GT/s)
1.0a	2.5GT/s	297	EndPoint Tests, Peak Differential Output Voltage (Transition) (2.5 GT/s)
1.0a	2.5GT/s	407	RootComplex Tests, Peak Differential Output Voltage (Non Transition) (2.5 GT/s)
1.0a	2.5GT/s	497	RootComplex Tests, Peak Differential Output Voltage (Transition) (2.5 GT/s)
1.1, 2.0, 3.0, 4.0	2.5GT/s	1140	Tx, Peak Differential Output Voltage (Transition) (2.5 GT/s)
1.1	2.5GT/s	1207	EndPoint Tests, Peak Differential Output Voltage (Non Transition) (2.5 GT/s)
1.1	2.5GT/s	1297	EndPoint Tests, Peak Differential Output Voltage (Transition) (2.5 GT/s)
2.0, 3.0, 4.0	2.5GT/s	1340	EndPoint Tests, Peak Differential Output Voltage (Transition) (2.5 GT/s)
2.0, 3.0, 4.0	2.5GT/s	1350	EndPoint Tests, Peak Differential Output Voltage (Non Transition) (2.5 GT/s)
1.1	2.5GT/s	1407	RootComplex Tests, Peak Differential Output Voltage (Non Transition) (2.5 GT/s)
2.0, 3.0, 4.0	2.5GT/s	1440	RootComplex Tests, Peak Differential Output Voltage (Transition) (2.5 GT/s)
2.0, 3.0, 4.0	2.5GT/s	1450	RootComplex Tests, Peak Differential Output Voltage (Non Transition) (2.5 GT/s)

1.1	2.5GT/s	1497	RootComplex Tests, Peak Differential Output Voltage (Transition) (2.5 GT/s)
2.0, 3.0, 4.0	5.0GT/s	2144	Tx, Peak Differential Output Voltage -3.5dB (Transition) (5.0 GT/s)
2.0, 3.0, 4.0	5.0GT/s	2145	Tx, Peak Differential Output Voltage -6.0dB (Transition) (5.0 GT/s)
3.0, 4.0	5.0GT/s	2154	Tx, Peak Differential Output Voltage -3.5dB (Non Transition) (5.0 GT/s)
3.0, 4.0	5.0GT/s	2155	Tx, Peak Differential Output Voltage -6.0dB (Non Transition) (5.0 GT/s)
2.0	5.0GT/s	2158	Tx, Peak Differential Output Voltage -6.0dB (Non Transition) (5.0 GT/s)
2.0	5.0GT/s	2159	Tx, Peak Differential Output Voltage -3.5dB (Non Transition) (5.0 GT/s)
2.0, 3.0, 4.0	5.0GT/s	2346	EndPoint Tests, Peak Differential Output Voltage -3.5dB (Transition) (5 GT/s)
2.0, 3.0, 4.0	5.0GT/s	2348	EndPoint Tests, Peak Differential Output Voltage -6.0dB (Transition) (5 GT/s)
2.0, 3.0, 4.0	5.0GT/s	2356	EndPoint Tests, Peak Differential Output Voltage -3.5dB (Non Transition) (5 GT/s)
2.0, 3.0, 4.0	5.0GT/s	2358	EndPoint Tests, Peak Differential Output Voltage -6.0dB (Non Transition) (5 GT/s)
2.0	5.0GT/s	2440	RootComplex Tests, Peak Differential Output Voltage (Transition) (5.0 GT/s)
2.0	5.0GT/s	2450	RootComplex Tests, Peak Differential Output Voltage (Non Transition) (5.0 GT/s)
1.0a	2.5GT/s	10007	Tx, Peak Differential Output Voltage (Transition) (2.5 GT/s, Low Power)
2.0, 3.0, 4.0	2.5GT/s	11140	Tx, Peak Differential Output Voltage (Transition) (2.5 GT/s, Low Power)
1.1	2.5GT/s	11141	Tx, Peak Differential Output Voltage (Transition) (2.5 GT/s, Low Power)

3.0, 4.0	2.5GT/s	11400	Tx, Peak Differential Output Voltage (Non Transition) (2.5 GT/s)
2.0, 3.0, 4.0	2.5GT/s	11401	Tx, Peak Differential Output Voltage (Non Transition) (2.5 GT/s, Low Power)
3.0	2.5GT/s	17003	U.2 RootComplex Tests, Peak Differential Output Voltage (Transition) (2.5 GT/s)
3.0	2.5GT/s	17004	U.2 RootComplex Tests, Peak Differential Output Voltage (Non Transition) (2.5 GT/s)
3.0	2.5GT/s	18003	U.2 EndPoint Tests, Peak Differential Output Voltage (Transition) (2.5 GT/s)
3.0	2.5GT/s	18004	U.2 EndPoint Tests, Peak Differential Output Voltage (Non Transition) (2.5 GT/s)
2.0, 3.0, 4.0	5.0GT/s	21140	Tx, Peak Differential Output Voltage (Transition) (5.0 GT/s, Low Power)
1.1, 2.0	2.5GT/s	21400	Tx, Peak Differential Output Voltage (Non Transition) (2.5 GT/s)
2.0, 3.0, 4.0	5.0GT/s	21540	Tx, Peak Differential Output Voltage (Non Transition) (5.0 GT/s, Low Power)
3.0	5.0GT/s	24400	RootComplex Tests, Peak Differential Output Voltage (Transition) (5.0 GT/s)
3.0	5.0GT/s	24500	RootComplex Tests, Peak Differential Output Voltage (Non Transition) (5.0 GT/s)
3.0	5.0GT/s	27002	U.2 RootComplex Tests, Peak Differential Output Voltage (Transition) (5.0 GT/s)
3.0	5.0GT/s	27003	U.2 RootComplex Tests, Peak Differential Output Voltage (Non Transition) (5.0 GT/s)
3.0	5.0GT/s	28002	U.2 EndPoint Tests, Peak Differential Output Voltage - 3.5dB (Transition) (5 GT/s)
3.0	5.0GT/s	28003	U.2 EndPoint Tests, Peak Differential Output Voltage - 3.5dB (Non Transition) (5 GT/s)
3.0	5.0GT/s	28006	U.2 EndPoint Tests, Peak Differential Output Voltage - 6.0dB (Transition) (5 GT/s)
3.0	5.0GT/s	28007	U.2 EndPoint Tests, Peak Differential Output Voltage - 6.0dB (Non Transition) (5 GT/s)
4.0	5.0GT/s	44400	RootComplex Tests, Peak Differential Output Voltage (Transition) (5.0 GT/s)

4.0	5.0GT/s	44500	RootComplex Tests, Peak Differential Output Voltage (Non Transition) (5.0 GT/s)

Signal Quality Preset Permutations

Changes in 4.80.0.0: Below tests support signal quality preset permutations.

PCIE Gen	Data Rate	Test ID	Test Name
3.0, 4.0	8.0 GT/s	3000	Tx, Unit interval (8.0 GT/s)
3.0, 4.0	8.0 GT/s	3010	Tx, DC common mode voltage (8.0 GT/s)
3.0, 4.0	8.0 GT/s	3021	Tx, AC common mode voltage - 4GHz LPF (8.0 GT/s)
3.0, 4.0	8.0 GT/s	3022	Tx, AC common mode voltage - 30kHz to 500MHz (8.0 GT/s)
3.0, 4.0	8.0 GT/s	3030	Tx, Absolute delta of DC common mode voltage between D+ and D- (8.0 GT/s)
3.0, 4.0	8.0 GT/s	3040	Tx, Absolute delta of DC common mode voltage during L0 and Idle (8.0 GT/s)
3.0	8.0 GT/s	3090	Tx, Uncorrelated total jitter (8.0 GT/s)
3.0	8.0 GT/s	3100	Tx, Uncorrelated deterministic jitter (8.0 GT/s)
3.0	8.0 GT/s	3110	Tx, Total uncorrelated PWJ (8.0 GT/s)
3.0	8.0 GT/s	3120	Tx, Deterministic DjDD uncorrelated PWJ (8.0 GT/s)
3.0	8.0 GT/s	3130	Tx, Data dependent jitter (8.0 GT/s)
3.0, 4.0	8.0 GT/s	3400	EndPoint Tests, Unit Interval (8.0 GT/s)
3.0	8.0 GT/s	3410	EndPoint Tests, Template Tests (8.0 GT/s)
3.0	8.0 GT/s	3420	EndPoint Tests, Peak Differential Output Voltage (Transition) (8.0 GT/s)
3.0	8.0 GT/s	3421	EndPoint Tests, Peak Differential Output Voltage (Non Transition) (8.0 GT/s)
3.0, 4.0	8.0 GT/s	3430	EndPoint Tests, Eye-Width (8.0 GT/s)

3.0, 4.0	8.0 GT/s	3500	RootComplex Tests, Unit Interval (8.0 GT/s)
3.0, 4.0	8.0 GT/s	3510	RootComplex Tests, Template Tests (8.0 GT/s)
3.0, 4.0	8.0 GT/s	3520	RootComplex Tests, Peak Differential Output Voltage (Transition) (8.0 GT/s)
3.0, 4.0	8.0 GT/s	3521	RootComplex Tests, Peak Differential Output Voltage (Non Transition) (8.0 GT/s)
3.0, 4.0	8.0 GT/s	3530	RootComplex Tests, Eye-Width (8.0 GT/s)
4.0	16.0 GT/s	4000	Tx, Unit interval (16.0 GT/s)
4.0	16.0 GT/s	4010	Tx, DC common mode voltage (16.0 GT/s)
4.0	16.0 GT/s	4030	Tx, Absolute delta of DC common mode voltage between D+ and D- (16.0 GT/s)
4.0	16.0 GT/s	4040	Tx, Absolute delta of DC common mode voltage during L0 and Idle (16.0 GT/s)
4.0	16.0 GT/s	4090	Tx, Uncorrelated total jitter (16.0 GT/s)
4.0	16.0 GT/s	4100	Tx, Uncorrelated deterministic jitter (16.0 GT/s)
4.0	16.0 GT/s	4130	Tx, Data dependent jitter (16.0 GT/s)
4.0	16.0 GT/s	4160	Tx, Random jitter RMS (16.0 GT/s)
4.0	16.0 GT/s	4170	Tx, AC common mode voltage - 30kHz to 500MHz (16.0 GT/s)
4.0	16.0 GT/s	4171	Tx, AC common mode voltage - 8GHz LPF (16.0 GT/s)
4.0	16.0 GT/s	4370	Tx, SSC Modulation Frequency (PCIE 4.0 16.0GT/s)
4.0	16.0 GT/s	4380	Tx, SSC Peak Deviation (Max) (PCIE 4.0 16.0GT/s)
4.0	16.0 GT/s	4385	Tx, SSC Peak Deviation (Min) (PCIE 4.0 16.0GT/s)
4.0	16.0 GT/s	4390	Tx, SSC Df/Dt (Max) (PCIE 4.0 16.0GT/s)

4.0	16.0 GT/s	4400	EndPoint Tests, Unit Interval (16.0 GT/s)
4.0	16.0 GT/s	4410	EndPoint Tests, Template Tests (16.0 GT/s)
4.0	16.0 GT/s	4420	EndPoint Tests, Peak Differential Output Voltage (Transition) (16.0 GT/s)
4.0	16.0 GT/s	4430	EndPoint Tests, Peak Differential Output Voltage (Non Transition) (16.0 GT/s)
4.0	16.0 GT/s	4440	EndPoint Tests, Eye-Width (16.0 GT/s)
4.0	16.0 GT/s	4500	RootComplex Tests, Unit Interval (16.0 GT/s)
4.0	16.0 GT/s	4510	RootComplex Tests, Template Tests (16.0 GT/s)
4.0	16.0 GT/s	4520	RootComplex Tests, Peak Differential Output Voltage (Transition) (16.0 GT/s)
4.0	16.0 GT/s	4530	RootComplex Tests, Peak Differential Output Voltage (Non Transition) (16.0 GT/s)
4.0	16.0 GT/s	4540	RootComplex Tests, Eye-Width (16.0 GT/s)
4.0	8.0 GT/s	5005	EndPoint Tests - SigTest (8.0 GT/s)
3.0	8.0 GT/s	5009	RootComplex Tests - SigTest (8.0 GT/s)
3.0	8.0 GT/s	5016	U.2 EndPoint Tests - SigTest (8.0 GT/s)
3.0	8.0 GT/s	5024	U.2 System Board Tx SigTest (PCIE 3.0, 8.0 GT/s)
4.0	16.0 GT/s	5027	RootComplex Tests - SigTest (16.0 GT/s) - Near End
4.0	16.0 GT/s	5028	EndPoint Tests - SigTest (16.0 GT/s) - Far End
4.0	16.0 GT/s	5029	RootComplex Tests - SigTest (16.0 GT/s) - Far End
3.0	8.0 GT/s	37000	U.2 System Board Tx, Unit Interval (PCIE 3.0, 8.0 GT/s)
3.0	8.0 GT/s	37001	U.2 System Board Tx, Template Tests (PCIE 3.0, 8.0 GT/s)

3.0	8.0 GT/s	37002	U.2 System Board Tx, Peak Differential Output Voltage (Non Transition) (PCIE 3.0, 8.0 GT/s)
3.0	8.0 GT/s	37003	U.2 System Board Tx, Peak Differential Output Voltage (Transition) (PCIE 3.0, 8.0 GT/s)
3.0	8.0 GT/s	37004	U.2 System Board Tx, Eye-Width (PCIE 3.0, 8.0 GT/s)
3.0	8.0 GT/s	38000	U.2 EndPoint Tests, Unit Interval (8.0 GT/s)
3.0	8.0 GT/s	38001	U.2 EndPoint Tests, Unit Interval (8.0 GT/s)
3.0	8.0 GT/s	38002	U.2 EndPoint Tests, Peak Differential Output Voltage (Transition) (8.0 GT/s)
3.0	8.0 GT/s	38003	U.2 EndPoint Tests, Peak Differential Output Voltage (Non Transition) (8.0 GT/s)
3.0	8.0 GT/s	38004	U.2 EndPoint Tests, Eye-Width (8.0 GT/s)
4.0	8.0 GT/s	43090	Tx, Uncorrelated total jitter (8.0 GT/s)
4.0	8.0 GT/s	43100	Tx, Uncorrelated deterministic jitter (8.0 GT/s)
4.0	8.0 GT/s	43110	Tx, Total uncorrelated PWJ (8.0 GT/s)
4.0	8.0 GT/s	43120	Tx, Deterministic DjDD uncorrelated PWJ (8.0 GT/s)
4.0	8.0 GT/s	43130	Tx, Data dependent jitter (8.0 GT/s)
4.0	8.0 GT/s	43160	Tx, Random jitter RMS (8.0 GT/s)
4.0	8.0 GT/s	43170	Tx, SSC Modulation Frequency (PCIE 4.0 8.0GT/s)
4.0	8.0 GT/s	43180	Tx, SSC Peak Deviation (Max) (PCIE 4.0 8.0GT/s)
4.0	8.0 GT/s	43185	Tx, SSC Peak Deviation (Max) (PCIE 4.0 8.0GT/s)
4.0	8.0 GT/s	43190	Tx, SSC Df/Dt (Max) (PCIE 4.0 8.0GT/s)
4.0	8.0 GT/s	43410	EndPoint Tests, Template Tests (8.0 GT/s)

4.0	8.0 GT/s	44200	EndPoint Tests, Peak Differential Output Voltage (Transition) (8.0 GT/s)
4.0	8.0 GT/s	44201	EndPoint Tests, Peak Differential Output Voltage (Non Transition) (8.0 GT/s)

License Required for Tests

Changes in 4.80.0.0: Below tests require EZJ (EZJIT) license.

PCIE Gen	Data Rate	Test ID	Test Name
1.0a	2.5 GT/s	1	Tx, Unit Interval (2.5 GT/s)
1.0a	2.5 GT/s	100	Rx, Unit Interval (2.5 GT/s)
2.0	2.5 GT/s	200	EndPoint Tests, Unit Interval (2.5 GT/s)
1.0a	2.5 GT/s	400	RootComplex Tests, Unit Interval (2.5 GT/s)
3.0	2.5 GT/s	810	Reference Clock, Phase Jitter (2.5 GT/s)
1.1	2.5 GT/s	1100	Tx, Unit Interval (2.5 GT/s)
1.1	2.5 GT/s	1200	Rx, Unit Interval (2.5 GT/s)
1.1, 2.0, 3.0, 4.0	2.5 GT/s	1300	EndPoint Tests, Unit Interval (2.5 GT/s)
1.1, 2.0, 3.0, 4.0	2.5 GT/s	1400	RootComplex Tests, Unit Interval (2.5 GT/s)
4.0	2.5 GT/s	1900	Reference Clock, Peak to Peak (Common Clk) (2.5 GT/s)
4.0	2.5 GT/s	1901	Reference Clock, RMS Jitter (Data Clk) (2.5 GT/s)
3.0	5.0 GT/s	2100	Tx, Unit Interval (5.0 GT/s)
3.0	2.5 GT/s	2101	Tx, Unit Interval (2.5 GT/s)
2.0	5.0 GT/s	2200	Rx, Data Clocked Architecture Unit Interval (5.0 GT/s)
2.0	2.5 GT/s	2201	Rx, Unit Interval (2.5 GT/s)
2.0	5.0 GT/s	2202	Rx, Common RefClk Architecture Unit Interval (5.0 GT/s)
2.0	2.5 GT/s	2300	EndPoint Tests, Unit Interval -3.5dB (5.0 GT/s)
2.0	2.5 GT/s	2301	EndPoint Tests, Unit Interval (2.5 GT/s)
2.0	5.0 GT/s	2302	EndPoint Tests, Unit Interval -6.0dB (5.0 GT/s)
2.0	5.0 GT/s	2400	RootComplex Tests, Unit Interval (5.0 GT/s)
2.0	2.5 GT/s	2401	RootComplex Tests, Unit Interval (2.5 GT/s)
3.0	5.0 GT/s	2810	Reference Clock, High frequency > 1.5MHz RMS Jitter (Common Clk) (5.0 GT/s)
4.0	5.0 GT/s	2820	Reference Clock, SSC Residual (Common Clk) (5.0 GT/s)
3.0	5.0 GT/s	2830	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Common Clk) (5.0 GT/s)

3.0	5.0 GT/s	2840	Reference Clock, SSC Deviation (Common Clk) (5.0GT/s)
3.0	5.0 GT/s	2850	Reference Clock, Maximum SSC Slew Rate (Data Clk) (5.0 GT/s)
3.0	5.0 GT/s	2860	Reference Clock, High frequency > 1.5MHz RMS Jitter (Data Clk) (5.0 GT/s
3.0	5.0 GT/s	2870	Reference Clock, Full SSC Modulation (Data Clk) (5.0 GT/s)
3.0	5.0 GT/s	2880	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Data Clk) (5.0 GT/s)
3.0	5.0 GT/s	2890	Reference Clock, SSC Deviation (Data Clk) (5.0 GT/s)
3.0	5.0 GT/s	2895	Reference Clock, Maximum SSC Slew Rate (Data Clk) (5.0 GT/s)
4.0	5.0 GT/s	2900	Reference Clock, RMS Jitter (Common Clk) (5.0 GT/s)
4.0	5.0 GT/s	2901	Reference Clock, RMS Jitter (Data Clk) (5.0 GT/s)
3.0	8.0 GT/s	3000	Tx, Unit interval (8.0 GT/s)
3.0	8.0 GT/s	3400	EndPoint Tests, Unit Interval (8.0 GT/s)
3.0	8.0 GT/s	3500	RootComplex Tests, Unit Interval (8.0 GT/s)
3.0	8.0 GT/s	3820	Reference Clock, RMS Jitter (Common Clk) (8.0 GT/s)
4.0	8.0 GT/s	3830	Reference Clock, SSC Frequency Range (Common Clk) (8.0 GT/s)
4.0	8.0 GT/s	3840	Reference Clock, SSC Deviation (Common Clk) (8.0GT/s)
4.0	8.0 GT/s	3840	Reference Clock, SSC Deviation (Common Clk) (8.0GT/s)
3.0	8.0 GT/s	3870	Reference Clock, RMS Jitter (Data Clk) (8.0 GT/s)
3.0	8.0 GT/s	3880	Reference Clock, SSC Frequency Range (Data Clk) (8.0 GT/s)
3.0	8.0 GT/s	3890	Reference Clock, SSC Deviation (Data Clk)(8.0GT/s)
3.0	8.0 GT/s	3900	Reference Clock, RMS Jitter (Common Clk) (8.0 GT/s)
4.0	8.0 GT/s	3900	Reference Clock, RMS Jitter (Common Clk) (8.0 GT/s)
4.0	8.0 GT/s	3901	Reference Clock, RMS Jitter (Data Clk) (8.0 GT/s)
4.0	16.0 GT/s	4000	Tx, Unit interval (16.0 GT/s)
4.0	16.0 GT/s	4370	Tx, SSC Modulation Frequency (PCIE 4.0 16.0GT/s)
4.0	16.0 GT/s	4380	Tx, SSC Peak Deviation (Max) (PCIE 4.0 16.0GT/s)
4.0	16.0 GT/s	4385	Tx, SSC Peak Deviation (Min) (PCIE 4.0 16.0GT/s)

4.0	16.0 GT/s	4390	Tx, SSC Df/Dt (Max)(PCIE 4.0 16.0GT/s)
4.0	16.0 GT/s	4400	EndPoint Tests, Unit Interval (16.0 GT/s)
4.0	16.0 GT/s	4500	RootComplex Tests, Unit Interval (16.0 GT/s)
4.0	16.0 GT/s	4830	Reference Clock, SSC Frequency Range (Common Clk) (16.0 GT/s)
4.0	16.0 GT/s	4840	Reference Clock, SSC Deviation (Common Clk) (16.0GT/s)
4.0	16.0 GT/s	4840	Reference Clock, SSC Deviation (Common Clk) (16.0GT/s)
4.0	16.0 GT/s	4900	Reference Clock, RMS Jitter (Common Clk) (16.0 GT/s)
4.0	16.0 GT/s	4901	Reference Clock, RMS Jitter (Data Clk) (16.0 GT/s)
3.0	2.5 GT/s	17000	U.2 RootComplex Tests, Unit Interval (2.5 GT/s)
3.0	2.5 GT/s	18000	U.2 EndPoint Tests, Unit Interval (2.5 GT/s)
3.0	5.0 GT/s	27000	U.2 RootComplex Tests, Unit Interval (5.0 GT/s)
3.0	5.0 GT/s	28000	U.2 EndPoint Tests, Unit Interval -3.5dB (5.0 GT/s)
3.0	5.0 GT/s	28004	U.2 EndPoint Tests, Unit Interval -6.0dB (5.0 GT/s)
3.0	8.0GT/s	37000	U.2 RootComplex Tests, Unit Interval (8.0 GT/s)
3.0	8.0GT/s	38000	U.2 EndPoint Tests, Unit Interval (8.0 GT/s)
4.0	8.0GT/s	43170	Tx, SSC Modulation Frequency (PCIE 4.0 8.0GT/s)
4.0	8.0GT/s	43180	Tx, SSC Peak Deviation (Max) (PCIE 4.0 8.0GT/s)
4.0	8.0GT/s	43185	Tx, SSC Peak Deviation (Min) (PCIE 4.0 8.0GT/s)
4.0	8.0GT/s	43190	Tx, SSC Df/Dt (Max)(PCIE 4.0 8.0GT/s)

Changes in 4.80.0.0: Below test requires EZP (EZJIT Plus) license.

PCIE Gen	Data Rate	Test ID	Test Name
3.0	5.0 GT/s	2194	Tx, Random Jitter < 1.5 MHz (5.0 GT/s)

Peak Differential Output Voltage Reporting

Changes in 4.80.0.0: Below tests have no value issue fixed in test result and report.

PCIE Gen	Data Rate	Test ID	Test Name
2.0	2.5 GT/s	1450	RootComplex Tests, Peak Differential Output Voltage (Non Transition)(2.5 GT/s)
2.0	5.0 GT/s	2450	RootComplex Tests, Peak Differential Output Voltage (Non Transition) (5.0 GT/s)
3.0	8.0 GT/s	3520	RootComplex Tests, Peak Differential Output Voltage (Transition)(8.0 GT/s)
3.0	8.0 GT/s	3521	RootComplex Tests, Peak Differential Output Voltage (Non Transition)(8.0 GT/s)
3.0	2.5 GT/s	17004	U.2 RootComplex Tests, Peak Differential Output Voltage (Non Transition)(2.5 GT/s)
3.0	2.5 GT/s	21400	Tx, Peak Differential Output Voltage (Non Transition)(2.5 GT/s)
3.0	5.0 GT/s	24500	RootComplex Tests, Peak Differential Output Voltage (Non Transition)(5.0 GT/s)
3.0	5.0 GT/s	27003	U.2 RootComplex Tests, Peak Differential Output Voltage (Non Transition)(5.0 GT/s)
3.0	8.0 GT/s	37002	U.2 RootComplex Tests, Peak Differential Output Voltage (Transition)(8.0 GT/s)
3.0	8.0 GT/s	37003	U.2 RootComplex Tests, Peak Differential Output Voltage (Non Transition) (8.0 GT/s)
4.0	5.0 GT/s	44500	RootComplex Tests, Peak Differential Output Voltage (Non Transition) (5.0 GT/s)

Updated 2.5 GT/s and 5.0 GT/s SSC Enabled Template File for Base Tests

Changes in 4.80.0.0: Modified template file for SSC enabled handling.

PCIE Gen	Data Rate	Test ID	Test Name
4.0	2.5 GT/s	1090	Tx, Uncorrelated total jitter (2.5 GT/s)
4.0	2.5 GT/s	1101	Tx, Uncorrelated deterministic jitter (2.5 GT/s)
4.0	2.5 GT/s	1102	Tx, Total uncorrelated PWJ (2.5 GT/s)
4.0	2.5 GT/s	1103	Tx, Deterministic DjDD uncorrelated PWJ (2.5 GT/s)
4.0	2.5 GT/s	1104	Tx, Data dependent jitter (2.5 GT/s)
4.0	2.5 GT/s	1106	Tx, Random jitter RMS (2.5 GT/s)
4.0	5.0 GT/s	2000	Tx, Uncorrelated deterministic jitter (5.0 GT/s)
4.0	5.0 GT/s	2090	Tx, Uncorrelated total jitter (5.0 GT/s)
4.0	5.0 GT/s	2102	Tx, Total uncorrelated PWJ (5.0 GT/s)
4.0	5.0 GT/s	2103	Tx, Deterministic DjDD uncorrelated PWJ (5.0 GT/s)
4.0	5.0 GT/s	2104	Tx, Data dependent jitter (5.0 GT/s)
4.0	5.0 GT/s	2106	Tx, Random jitter RMS (5.0 GT/s)

Fixed Reporting as No Value

Changes in 4.80.0.0: Removed unused no value parameters in below tests

PCIE Gen	Data Rate	Test ID	Test Name
2.0	5.0 GT/s	2430	RootComplex Tests, Eye-Width with crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2431	RootComplex Tests, Eye-Width without crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2482	RootComplex Tests, RMS Random Jitter with crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2483	RootComplex Tests, RMS Random Jitter without crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2496	RootComplex Tests, Total Jitter at BER-12 with crosstalk (5.0 GT/s)
2.0	5.0 GT/s	2497	RootComplex Tests, Total Jitter at BER-12 without crosstalk (5.0 GT/s)
3.0	8.0 GT/s	3510	RootComplex Tests, Template Tests (8.0 GT/s)
3.0	8.0 GT/s	3530	RootComplex Tests, Eye-Width (8.0 GT/s)
3.0	5.0 GT/s	27004	U.2 RootComplex Tests, Eye-Width with crosstalk (5.0 GT/s)
3.0	5.0 GT/s	27005	U.2 RootComplex Tests, RMS Random Jitter with crosstalk (5.0 GT/s)
3.0	5.0 GT/s	27007	U.2 RootComplex Tests, Total Jitter at BER-12 with crosstalk (5.0 GT/s)
3.0	5.0 GT/s	27008	U.2 RootComplex Tests, Eye-Width without crosstalk (5.0 GT/s)
3.0	5.0 GT/s	27009	U.2 RootComplex Tests, RMS Random Jitter without crosstalk (5.0 GT/s)
3.0	5.0 GT/s	27011	U.2 RootComplex Tests, Total Jitter at BER-12 without crosstalk (5.0 GT/s)
3.0	8.0 GT/s	37001	U.2 RootComplex Tests, Template Tests (8.0 GT/s)
3.0	8.0 GT/s	37004	U.2 RootComplex Tests, Eye-Width (8.0 GT/s)
3.0	5.0 GT/s	248200	RootComplex Tests, RMS Random Jitter with crosstalk (5.0 GT/s)
3.0	5.0 GT/s	248300	RootComplex Tests, RMS Random Jitter without crosstalk (5.0 GT/s)

5GT/s De-emphasis Missing Test Name Information

Changes in 4.80.0.0: Added missing 5.0 GT/s de-emphasis value information in test result and test report.

PCIE Gen	Data Rate	Test ID	Test Name
3.0	5.0 GT/s	2144	Tx, Peak Differential Output Voltage -3.5dB (Transition) (5.0 GT/s)
3.0	5.0 GT/s	2145	Tx, Peak Differential Output Voltage -6.0dB (Transition) (5.0 GT/s)
2.0	5.0 GT/s	2154	Tx, Peak Differential Output Voltage -3.5dB (Non Transition) (5.0 GT/s)
2.0	5.0 GT/s	2155	Tx, Peak Differential Output Voltage -6.0dB (Non Transition) (5.0 GT/s)
2.0	5.0 GT/s	2155	Tx, Peak Differential Output Voltage -6.0dB (Non Transition) (5.0 GT/s)
2.0	5.0 GT/s	2158	Tx, Peak Differential Output Voltage -6.0dB (Non Transition) (5.0 GT/s)
2.0	5.0 GT/s	2159	Tx, Peak Differential Output Voltage -3.5dB (Non Transition) (5.0 GT/s)
2.0	5.0 GT/s	2162	Tx, Deemphasized Voltage Ratio -3.5dB (5.0 GT/s)
2.0	5.0 GT/s	2164	Tx, Deemphasized Voltage Ratio -6.0dB (5.0 GT/s)
2.0	5.0 GT/s	2346	EndPoint Tests, Peak Differential Output Voltage -3.5dB (Transition) (5.0 GT/s)
2.0	5.0 GT/s	2348	EndPoint Tests, Peak Differential Output Voltage -6.0dB (Transition) (5.0 GT/s)
2.0	5.0 GT/s	2356	EndPoint Tests, Peak Differential Output Voltage -3.5dB (Non Transition) (5.0 GT/s)
2.0	5.0 GT/s	2358	EndPoint Tests, Peak Differential Output Voltage -6.0dB (Non Transition) (5.0 GT/s)
2.0	5.0 GT/s	2430	RootComplex Tests, Eye-Width with crosstalk (5.0 GT/s)
3.0	5.0 GT/s	28002	U.2 EndPoint Tests, Peak Differential Output Voltage -3.5dB (Transition) (5.0 GT/s)
3.0	5.0 GT/s	28003	U.2 EndPoint Tests, Peak Differential Output Voltage -3.5dB (Non Transition) (5.0 GT/s)
3.0	5.0 GT/s	28006	U.2 EndPoint Tests, Peak Differential Output Voltage -6.0dB (Transition) (5.0 GT/s)
3.0	5.0 GT/s	28007	U.2 EndPoint Tests, Peak Differential Output Voltage -6.0dB (Non Transition) (5.0 GT/s)
2.0	5.0 GT/s	216200	Tx, Deemphasized Voltage Ratio -3.5dB (5.0 GT/s)
2.0	5.0 GT/s	216201	Tx, Deemphasized Voltage Ratio -3.5dB (5.0 GT/s)
2.0	5.0 GT/s	216400	Tx, Deemphasized Voltage Ratio -6.0dB (5.0 GT/s)
2.0	5.0 GT/s	216401	Tx, Deemphasized Voltage Ratio -6.0dB (5.0 GT/s)

Limitation When Using Infiniium Offline

PCIE Gen	Data Rate	Test ID	Test Name
1.1	2.5 GT/s	810	Reference Clock, Phase Jitter (2.5 GT/s)
1.1	2.5 GT/s	880	Reference Clock, Absolute Crossing Point Voltage (2.5 GT/s)
4.0	2.5 GT/s	1900	Reference Clock, Peak to Peak (Common Clk) (2.5 GT/s)
4.0	2.5 GT/s	1901	Reference Clock, RMS Jitter (Data Clk) (2.5 GT/s)
2.0	5.0 GT/s	2152	Tx, Tmin-Pulse (5.0 GT/s)
3.0	8.0 GT/s	2810	Reference Clock, High frequency > 1.5MHz RMS Jitter (Common Clk) (5.0 GT/s)
3.0	5.0 GT/s	2830	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Common Clk) (5.0 GT/s)
3.0	5.0 GT/s	2860	Reference Clock, High frequency > 1.5MHz RMS Jitter (Data Clk) (5.0 GT/s)
3.0	5.0 GT/s	2880	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Data Clk) (5.0 GT/s)
4.0	5.0 GT/s	2900	Reference Clock, RMS Jitter (Common Clk) (5.0 GT/s)
4.0	5.0 GT/s	2901	Reference Clock, RMS Jitter (Data Clk) (5.0 GT/s)
3.0	8.0 GT/s	3820	Reference Clock, RMS Jitter (Common Clk) (8.0 GT/s)
3.0	8.0 GT/s	3870	Reference Clock, RMS Jitter (Data Clk) (8.0 GT/s)
4.0	8.0 GT/s	3900	Reference Clock, RMS Jitter (Common Clk) (8.0 GT/s)
4.0	8.0 GT/s	3901	Reference Clock, RMS Jitter (Data Clk) (8.0 GT/s)
4.0	16.0 GT/s	4900	Reference Clock, RMS Jitter (Common Clk) (16.0 GT/s)
4.0	16.0 GT/s	4901	Reference Clock, RMS Jitter (Data Clk) (16.0 GT/s)
4.0	5.0 GT/s	42152	Tx, Tmin-Pulse (5.0 GT/s)

Base Test SSC Enabled Template File Changes

Changes in 4.81.2.0: Corrected the handling of SRIS template for the base tests below.

PCIE Gen	Data Rate	Test ID	Test Name
1.1	2.5 GT/s	1110	Tx, Template Tests (2.5 GT/s)
1.1	2.5 GT/s	1120	Tx, Median to Max Jitter (2.5 GT/s)
1.1	2.5 GT/s	1130	Tx, Eye-Width (2.5 GT/s)

1.1	2.5 GT/s	1140	Tx, Peak Differential Output Voltage (Transition) (2.5 GT/s)
1.1	2.5 GT/s	21400	Tx, Peak Differential Output Voltage (Non Transition) (2.5 GT/s)
1.1	2.5 GT/s	1160	Tx, Deemphasized Voltage Ratio (2.5 GT/s)
1.1	2.5 GT/s	11110	Tx, Template Tests (2.5 GT/s, Low Power)
1.1	2.5 GT/s	11120	Tx, Median to Max Jitter (2.5 GT/s, Low Power)
1.1	2.5 GT/s	11130	Tx, Eye-Width (2.5 GT/s, Low Power)
1.1	2.5 GT/s	11141	Tx, Peak Differential Output Voltage (Transition) (2.5 GT/s, Low Power)
2.0	5.0 GT/s	2192	Tx, Deterministic Jitter > 1.5 MHz (5.0 GT/s)
2.0	5.0 GT/s	2194	Tx, Random Jitter < 1.5 MHz (5.0 GT/s)
2.0	5.0 GT/s	21142	Tx, Template Tests -6.0dB (5.0 GT/s)
2.0	5.0 GT/s	2135	Tx, Eye-Width -6.0dB (5.0 GT/s)
2.0	5.0 GT/s	216400	Tx, Deemphasized Voltage Ratio -6.0dB (5.0 GT/s)
2.0	5.0 GT/s	2145	Tx, Peak Differential Output Voltage -6.0dB (Transition) (5.0 GT/s)
2.0	5.0 GT/s	2158	Tx, Peak Differential Output Voltage -6.0dB (Non Transition) (5.0 GT/s)
2.0	5.0 GT/s	21141	Tx, Template Tests -3.5dB (5.0 GT/s)
2.0	5.0 GT/s	216200	Tx, Deemphasized Voltage Ratio -3.5dB (5.0 GT/s)
2.0	5.0 GT/s	2159	Tx, Peak Differential Output Voltage -3.5dB (Non Transition) (5.0 GT/s)
2.0	5.0 GT/s	21140	Tx, Template Tests (5.0 GT/s, Low Power)
2.0	5.0 GT/s	21440	Tx, Peak Differential Output Voltage (Transition) (5.0 GT/s, Low Power)
2.0	5.0 GT/s	21540	Tx, Peak Differential Output Voltage (Non Transition) (5.0 GT/s, Low Power)
2.0	5.0 GT/s	2234	Tx, Eye-Width (5.0 GT/s, Low Power)
3.0	2.5 GT/s	11400	Tx, Peak Differential Output Voltage (Non Transition) (2.5 GT/s)
3.0	2.5 GT/s	2160	Tx, Deemphasized Voltage Ratio (2.5 GT/s)
3.0	2.5 GT/s	11140	Tx, Peak Differential Output Voltage (Transition) (2.5 GT/s, Low Power)
3.0	2.5 GT/s	11401	Tx, Peak Differential Output Voltage (Non Transition) (2.5 GT/s, Low Power)
3.0	5.0 GT/s	2114	Tx, Template Tests -3.5 dB (5.0 GT/s)
3.0	5.0 GT/s	2134	Tx, Eye-Width -3.5 dB (5.0 GT/s)
3.0	5.0 GT/s	2144	Tx, Peak Differential Output Voltage -3.5dB (Transition) (5.0 GT/s)
3.0	5.0 GT/s	2154	Tx, Peak Differential Output Voltage -3.5dB (Non Transition) (5.0 GT/s)

3.0	5.0 GT/s	2162	Tx, Deemphasized Voltage Ratio -3.5dB (5.0 GT/s)
3.0	5.0 GT/s	2174	Tx, Template Tests -6.0dB (5.0 GT/s)
3.0	5.0 GT/s	2135	Tx, Eye-Width -6.0dB (5.0 GT/s)
3.0	5.0 GT/s	2164	Tx, Deemphasized Voltage Ratio -6.0dB (5.0 GT/s)
3.0	5.0 GT/s	2145	Tx, Peak Differential Output Voltage -6.0dB (Transition) (5.0 GT/s)
3.0	5.0 GT/s	2155	Tx, Peak Differential Output Voltage -6.0dB (Non Transition) (5.0 GT/s)
3.0	5.0 GT/s	321140	Tx, Template Tests (5.0 GT/s, Low Power)
3.0	8.0 GT/s	3140	Tx, Pseudo Package Loss (8.0 GT/s)
3.0	8.0 GT/s	314000	Tx, Pseudo Package Loss (8.0 GT/s, Root Device)
3.0	8.0 GT/s	3130	Tx, Data Dependent Jitter (8.0 GT/s)
3.0	8.0 GT/s	3120	Tx, Deterministic DjDD Uncorrelated PWJ (8.0 GT/s)
3.0	8.0 GT/s	3110	Tx, Total Uncorrelated PWJ (8.0 GT/s)
3.0	8.0 GT/s	3100	Tx, Uncorrelated Deterministic Jitter (8.0 GT/s)
3.0	8.0 GT/s	3090	Tx, Uncorrelated Total Jitter (8.0 GT/s)
3.0	8.0 GT/s	3050	Tx, Full Swing Tx Voltage with No TxEQ (8.0 GT/s)
3.0	8.0 GT/s	13061	Tx, Reduced swing Tx voltage with no TxEQ (8.0 GT/s, Low Power)
3.0	8.0 GT/s	3070	Tx, Min Swing during EIEOS for Full Swing (8.0 GT/s)
3.0	8.0 GT/s	13080	Tx, Min Swing during EIEOS for Reduced Swing (8.0 GT/s, Low Power)
4.0	5.0 GT/s	42114	Tx, Template Tests -3.5dB (5.0 GT/s)
4.0	5.0 GT/s	42134	Tx, Eye-Width -3.5dB (5.0 GT/s)
4.0	5.0 GT/s	216201	Tx, Deemphasized Voltage Ratio -3.5dB (5.0 GT/s)
4.0	16.0 GT/s	4140	Tx, Pseudo Package Loss (16.0 GT/s, Non-Root Device Not Support Captive Channel)
4.0	16.0 GT/s	414001	Tx, Pseudo Package Loss (16.0 GT/s, Non-Root Device Support Captive Channel)
4.0	16.0 GT/s	414000	Tx, Pseudo Package Loss (16.0 GT/s, Root Device)
4.0	8.0 GT/s	43140	Tx, Pseudo Package Loss (8.0 GT/s, Non-Root Device)
4.0	8.0 GT/s	4314000	Tx, Pseudo Package Loss (8.0 GT/s, Root Device)
4.0	16.0 GT/s	4130	Tx, Data Dependent Jitter (16.0 GT/s)
4.0	8.0 GT/s	43130	Tx, Data Dependent Jitter (8.0 GT/s)

4.0	5.0 GT/s	2104	Tx, Data Dependent Jitter (5.0 GT/s)
4.0	2.5 GT/s	1104	Tx, Data Dependent Jitter (2.5 GT/s)
4.0	16.0 GT/s	4160	Tx, Random Jitter RMS (16.0 GT/s)
4.0	8.0 GT/s	43160	Tx, Random Jitter RMS (8.0 GT/s)
4.0	5.0 GT/s	2106	Tx, Random Jitter RMS (5.0 GT/s)
4.0	2.5 GT/s	1106	Tx, Random Jitter RMS (2.5 GT/s)
4.0	16.0 GT/s	4120	Tx, Deterministic DjDD Uncorrelated PWJ (16.0 GT/s)
4.0	2.5 GT/s	1103	Tx, Deterministic DjDD Uncorrelated PWJ (2.5 GT/s)
4.0	5.0 GT/s	2103	Tx, Deterministic DjDD Uncorrelated PWJ (5.0 GT/s)
4.0	8.0 GT/s	43120	Tx, Deterministic DjDD Uncorrelated PWJ (8.0 GT/s)
4.0	16.0 GT/s	4110	Tx, Total Uncorrelated PWJ (16.0 GT/s)
4.0	2.5 GT/s	1102	Tx, Total Uncorrelated PWJ (2.5 GT/s)
4.0	5.0 GT/s	2102	Tx, Total Uncorrelated PWJ (5.0 GT/s)
4.0	8.0 GT/s	43110	Tx, Total Uncorrelated PWJ (8.0 GT/s)
4.0	16.0 GT/s	4100	Tx, Uncorrelated Deterministic Jitter (16.0 GT/s)
4.0	2.5 GT/s	1101	Tx, Uncorrelated Deterministic Jitter (2.5 GT/s)
4.0	5.0 GT/s	2000	Tx, Uncorrelated Deterministic Jitter (5.0 GT/s)
4.0	8.0 GT/s	43100	Tx, Uncorrelated Deterministic Jitter (8.0 GT/s)
4.0	16.0 GT/s	4090	Tx, Uncorrelated Total Jitter (16.0 GT/s)
4.0	2.5 GT/s	1090	Tx, Uncorrelated Total Jitter (2.5 GT/s)
4.0	5.0 GT/s	2090	Tx, Uncorrelated Total Jitter (5.0 GT/s)
4.0	8.0 GT/s	43090	Tx, Uncorrelated Total Jitter (8.0 GT/s)
4.0	16.0 GT/s	4050	Tx, Full Swing Tx Voltage with No TxEQ (16.0 GT/s)
4.0	16.0 GT/s	14050	Tx, Reduced Swing Tx Voltage with No TxEQ (16.0 GT/s, Low Power)
4.0	8.0 GT/s	13060	Tx, Reduced Swing Tx Voltage with No TxEQ (8.0 GT/s, Low Power)
4.0	16.0 GT/s	4070	Tx, Min Swing during EIEOS for Full Swing (16.0 GT/s)
4.0	16.0 GT/s	14070	Tx, Min Swing during EIEOS for Reduced Swing (16.0 GT/s, Low Power)
4.0	2.5 GT/s	41110	Tx, Template Tests (2.5 GT/s)
4.0	2.5 GT/s	41120	Tx, Median to Max Jitter (2.5 GT/s)

4.0	2.5 GT/s	41130	Tx, Eye-Width (2.5 GT/s)
4.0	5.0 GT/s	216401	Tx, Deemphasized Voltage Ratio -6.0dB (5.0 GT/s)
4.0	5.0 GT/s	42135	Tx, Eye-Width -6.0dB (5.0 GT/s)
4.0	5.0 GT/s	42214	Tx, Template Tests -6.0dB (5.0 GT/s)

Tests Affected by the Pseudo Package Loss Preset Handling Issue

Changes in 4.81.3.0: Corrected the preset handling issue for the base tests below.

PCIE Gen	Data Rate	Test ID	Test Name
3.0	8.0 GT/s	3140	Tx, Pseudo package loss (8.0 GT/s)
3.0	8.0 GT/s	314000	Tx, Pseudo package loss (8.0 GT/s Root device)
4.0	8.0 GT/s	4314000	Tx, Pseudo package loss (8.0 GT/s Root device)
4.0	8.0 GT/s	43140	Tx, Pseudo package loss (8.0 GT/s Non-root device)
4.0	16.0 GT/s	414000	Tx, Pseudo package loss (16.0 GT/s Root device)
4.0	16.0 GT/s	414001	Tx, Pseudo package loss (16.0 GT/s Non-root device support captive channel)
4.0	16.0 GT/s	4140	Tx, Pseudo package loss (16.0 GT/s Non-root device not support captive channel)