Keysight D9030TBTC Thunderbolt 3 Test Application

KEYSIGHT TECHNOLOGIES

Methods of Implementation

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7 Transmitter Tests for 20.625 GB/s Systems

1 Overview

Thunderbolt 3 Automated Testing—At a Glance

The Keysight D9030TBTC Thunderbolt 3 Test Application allows the testing of all 3rd Generation Thunderbolt devices with the Keysight Infiniium Oscilloscope. These tests are based on the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.

The USB Type-C connector in conjunction with a Thunderbolt Controller is capable of providing two dual-simplex lanes (or channels). Each lane provides bi-directional 10.3125, 20.625 GB/s, 10 GB/s or 20 GB/s of bandwidth. The USB Type-C connector is capable of connecting Thunderbolt products when using either a USB Type-C Full Featured cable, a Thunderbolt Passive cable, a Thunderbolt Active Electrical or Optical Cable, or Thunderbolt legacy Cable or Dongle.

The current version of the Thunderbolt 3 Test Application also extends support for bit rates of 10 Gb/s and 20Gb/s based on the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9* specification document.

The Thunderbolt 3 Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run, and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE The tests performed by the Thunderbolt 3 Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.

Required Equipment and Software

In order to run the Thunderbolt 3 automated tests, you need the following equipment and software:

Hardware

- Use one of the Oscilloscope models given in Table 1.
- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Keysight also recommends using a second monitor to view the test application.

Table 1 lists the recommended test equipments for running the Thunderbolt 3 tests. Note that all test equipments require calibration to ensure accurate and repeatable results. The test equipments must be calibrated prior to, and if necessary, during the test procedure.

Table 1 Test Equipments and Accessories for Thunderbolt 3 Tests

Required Equipment	Test Equipment Capabilities/Description	Recommended Test Equipment
Test Point Access Boards	TPA Boards provide test point for the pins on the Thunderbolt connector and an easy way to control the DUT	▪ Thunderbolt Plug Test Fixture or equivalent ▪ Wilder TBT-TPA-UHG2 Thunderbolt Micro-Controller Test Module with USB Cable or equivalent
Real Time Scopes (choose from one of the available options)	▪ DC to 21±1GHz -3dB bandwidth or greater ▪ 80G sample/sec Sampling rate or greater, sampling 2 channels simultaneously ▪ Sample memory: 2 channels at 50M samples per channel or greater ▪ 1st and 2nd order CDR capability ▪ Equalization for USB 3.1 model capability	▪ Keysight Z-Series Oscilloscope (25GHz and above)
	▪ DC to 21±1GHz -3dB bandwidth or greater ▪ 128G sample/sec Sampling rate or greater, sampling 2 channels simultaneously ▪ Sample memory: 2 channels at 50M samples per channel or greater ▪ 1st and 2nd order CDR capability ▪ Equalization for USB 3.1 model capability	▪ Keysight UXR Series Oscilloscope (25GHz and above)
Accessories		
Low insertion loss phase matched cables	▪ Phase matched ±2° @ 40GHz ▪ Max IL in 10GHz < 1.2dB	▪ Rosenberger UK Micro Coax FC142A0-014-MTIE 2.92m (x2) L-1m (40GHz) ▪ Rosenberger Adaptor: RPC-2.92 female – SMP female - 02K119-K00E3

Software

- The minimum version of Infiniium Oscilloscope Software (see the Keysight D9030TBTC Thunderbolt 3 Test Application Release Notes)
- Keysight D9030TBTC Thunderbolt 3 Test Application software

Licensing information

Refer to the *Data Sheet* pertaining to Thunderbolt 3 Test Application to know about the licenses you must install along with other optional licenses. Visit "http://www.keysight.com/find/D9030TBTC" and in the web page's **Document Library** tab, you may view the associated Data Sheet.

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

The licensing format for Keysight License Manager 6 differs from its predecessors. See “Installing the License Key" on page 31 to see the difference in installing a license key using either of the applications on your machine.

In This Book

This manual describes the tests that are performed by the Thunderbolt 3 Test Application in more detail.

- Chapter 2, “Installing the Test Application and Licenses” describes how to install the software and licenses for the Thunderbolt 3 Test Application software (if it was purchased separately).
- Chapter 3, “Preparing to Take Measurements” describes how to start the Thunderbolt 3 Test Application and gives a brief overview of its features.
- Chapter 4, “Host / Device Thunderbolt 3 Transmitter Testing” contains an overview on the Thunderbolt system components and requirements for Transmitter testing.
- Chapter 5, “Transmitter Tests for 10.3125 GB/s Systems” describes procedures to run electrical tests on a Thunderbolt DUT operating at a bit rate of 10.3125 GB/s.
- Chapter 6, “Transmitter Tests for 10 GB/s Systems” describes procedures to run electrical tests on a Thunderbolt DUT operating at a rounded-off bit rate of 10 GB/s.
- Chapter 7, “Transmitter Tests for 20.625 GB/s Systems” describes procedures to run electrical tests on a Thunderbolt DUT operating at a bit rate of 20.625 GB/s.
- Chapter 8, “Transmitter Tests for 20 GB/s Systems” describes procedures to run electrical tests on a Thunderbolt DUT operating at a rounded-off bit rate of 20 GB/s.

See Also

The Keysight D9030TBTC Thunderbolt 3 Test Application Methods of Implementation’s Online Help, which describes:

- Starting the Thunderbolt 3 Test Application
- Creating or Opening a Test Project
- Setting Up the Test Environment
- Selecting Tests
- Configuring Tests
- Verifying Physical Connections
- Running Tests
- Configuring Automation in the Test Application
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
- Additional Settings in the Test App

References

- The Thunderbolt standard specifications are available in *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9* and *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

2 Installing the Test Application and Licenses

If you purchased the Keysight D9030TBTC Thunderbolt 3 Test Application separate from your Infiniium oscilloscope, you must install the software and license key.

Installing the Test Application

1. Make sure you have the minimum version of Infiniium Oscilloscope software (see the D9030TBTC Thunderbolt 3 Test Application release notes). To ensure that you have the minimum version, select **Help > About Infiniium...** from the main menu.
2. To obtain the Thunderbolt 3 Test Application, go to Keysight website: "http://www.keysight.com/find/D9030TBTC".
3. In the web page's **Trials & Licenses** tab, click the **Details and Download** button to view instructions for downloading and installing the application software.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

1 Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.

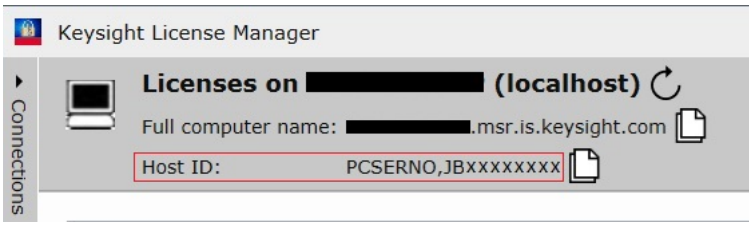


Figure 1 Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager.

3 From the configuration menu, use one of the options to install each license file.

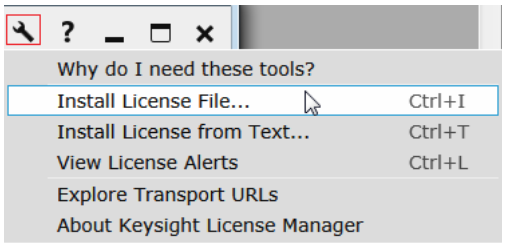


Figure 2 Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

1. Launch Keysight License Manager 6 on your machine, where you wish to run the Test Application and its features.
2. Copy the Host ID, which is the first set of alphanumeric value (as highlighted in Figure 3) that appears in the Environment tab of the application. Note that x indicates numeric values.

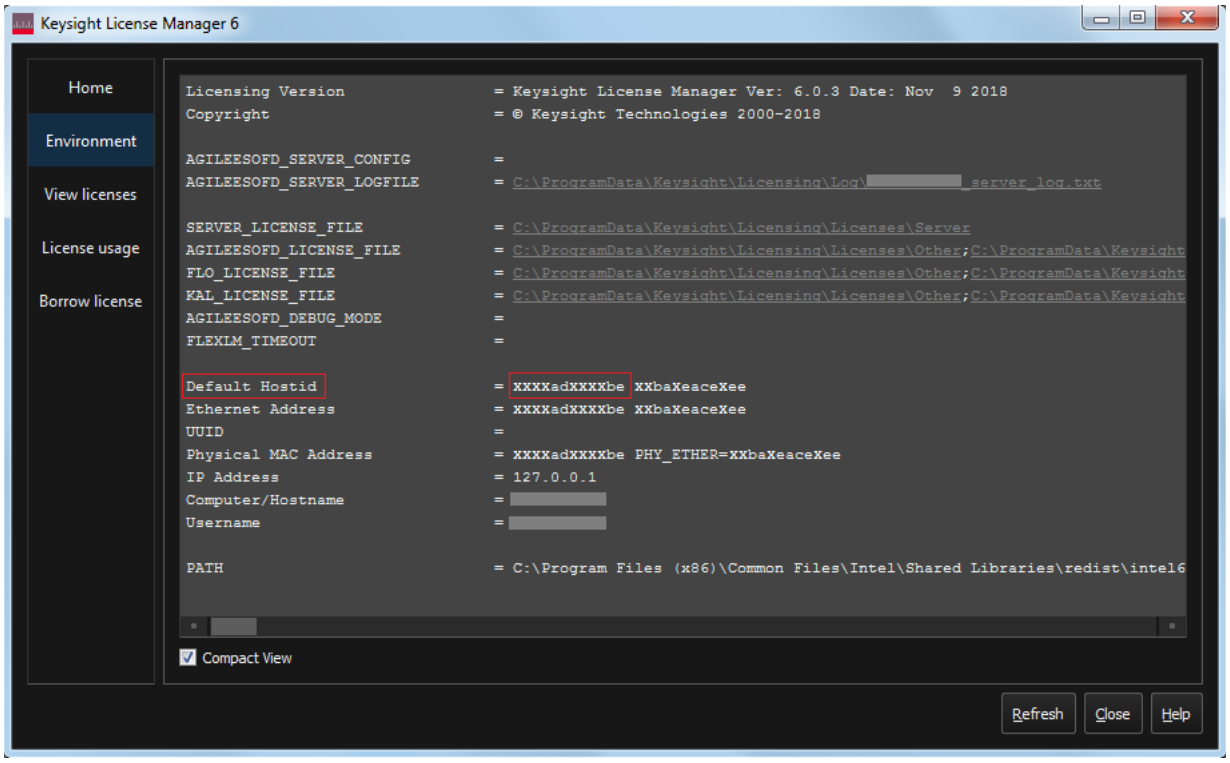


Figure 3 Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager 6.

3 From the Home tab, use one of the options to install each license file.

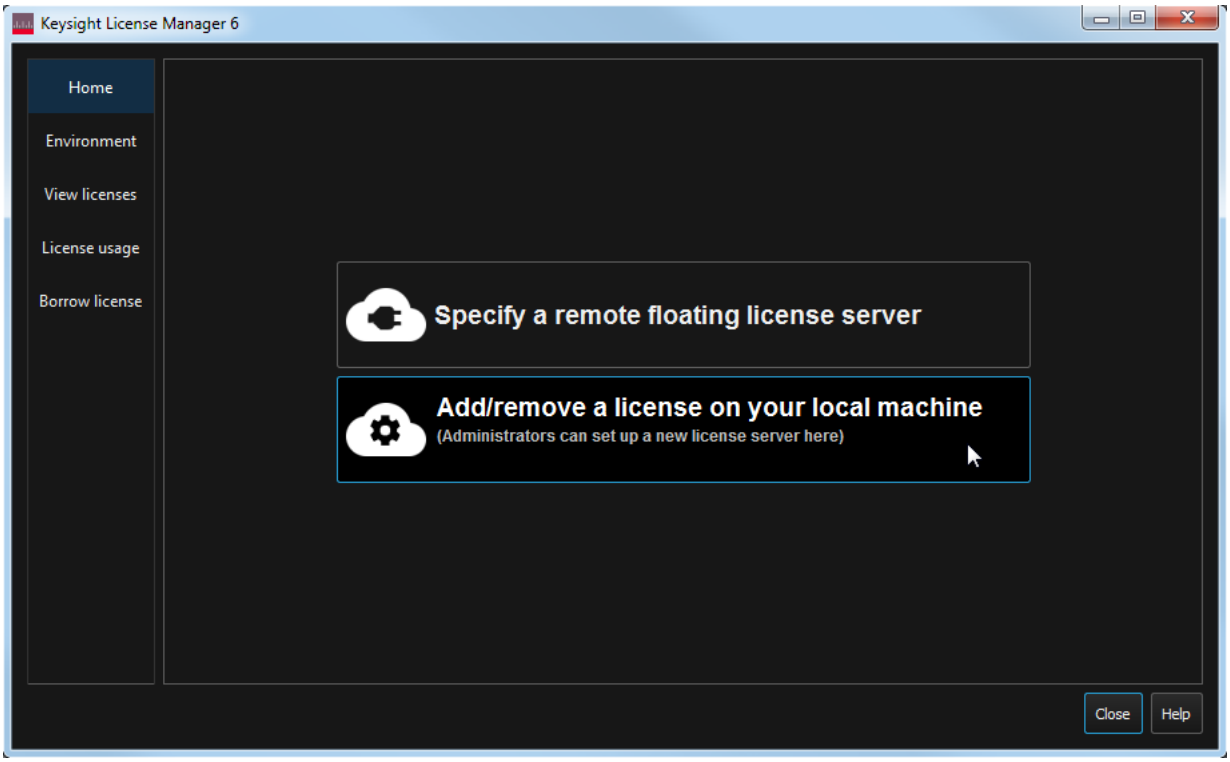


Figure 4 Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

3 Preparing to Take Measurements

Before running the automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this application. After the oscilloscope and probe have been calibrated, you are ready to start the Thunderbolt 3 Test Application and perform the measurements.

Calibrating the Oscilloscope

If you have not already calibrated the oscilloscope, refer to the *User Guide* for the respective Oscilloscope you are using.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.

NOTE If you switch cables between channels or other Oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the Thunderbolt 3 Test Application

1 Ensure that the Thunderbolt 3 Device Under Test (DUT) is operating and set to desired test modes. To start the Thunderbolt 3 Test Application: From the Infiniium Oscilloscope's main menu, select **Analyze > Automated Test Apps > D9030TBTC Thunderbolt 3 Test App**.

NOTE The **Test Lane** drop-down options in the **Set Up** tab, when the Test App is launched on a 4-Channel Oscilloscope, are different from that on a 2-Channel Oscilloscope.

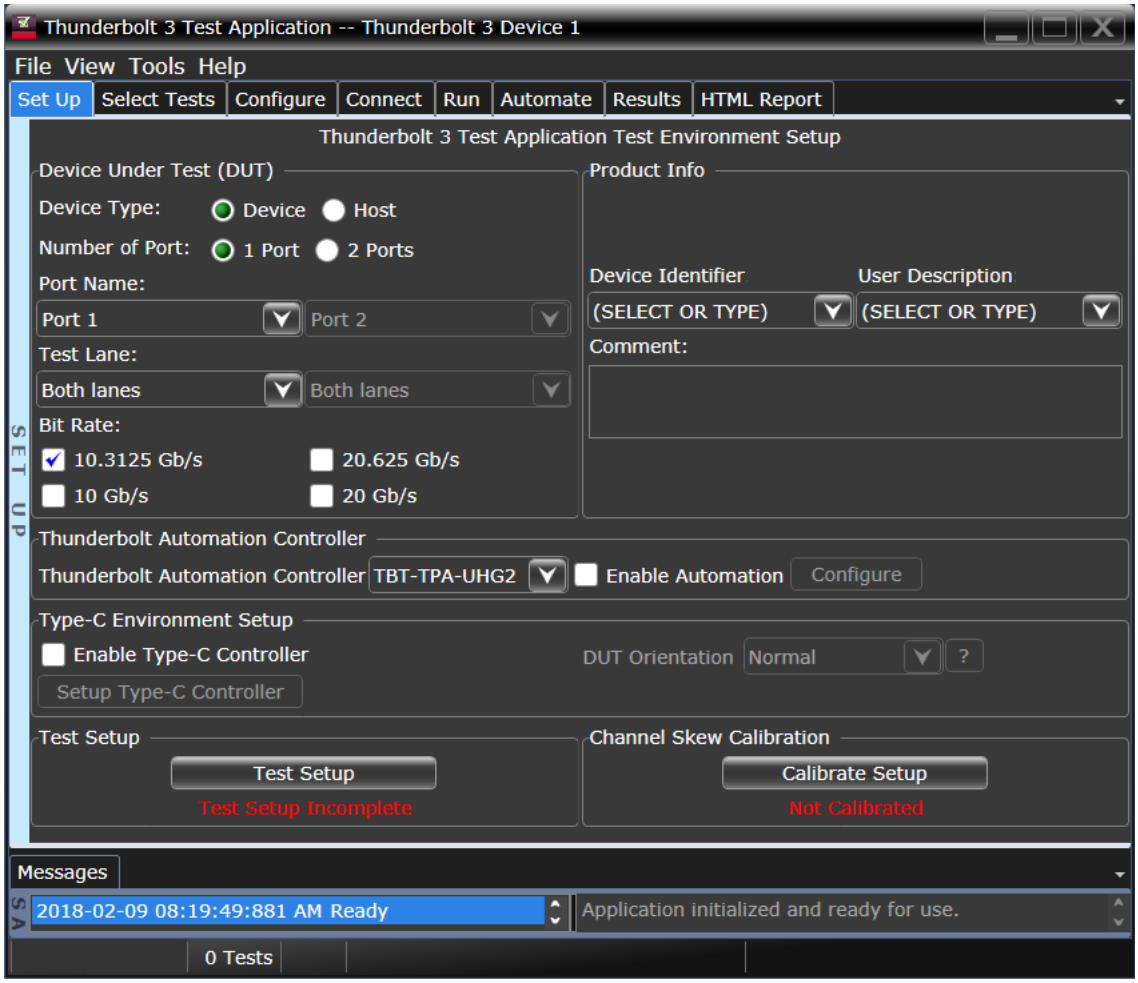


Figure 5 Thunderbolt 3 Test Application default window on 4-Ch Oscilloscope

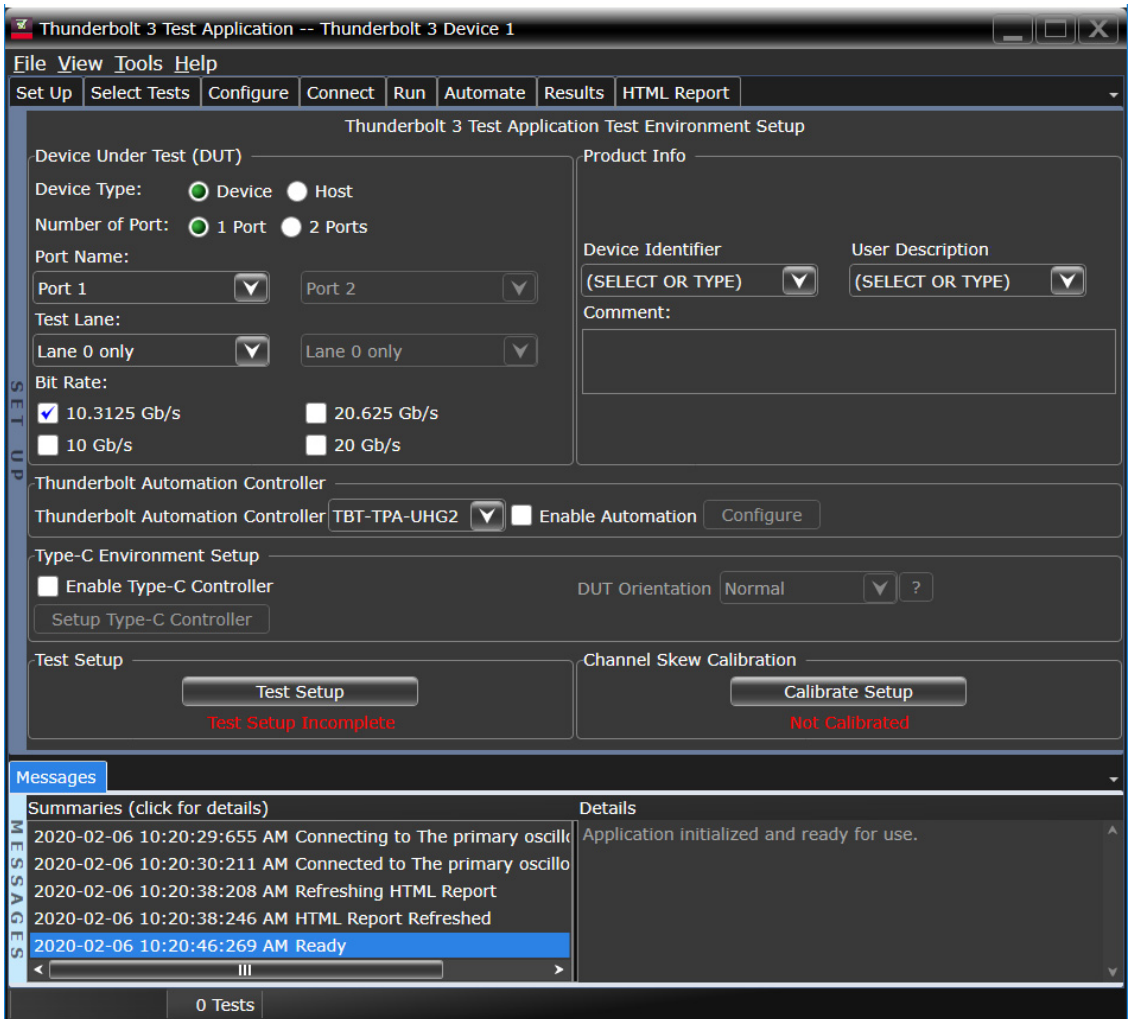


Figure 6 Thunderbolt 3 Test Application default window on 2-Ch Oscilloscope

To understand the functionality of the various features in the user interface of the Test Application, refer to the *Keysight D9030TBTC Thunderbolt 3 Test Application Online Help* available in the Help menu.

The task flow pane and the tabs in the main pane show the steps you take in running the automated tests:

Set Up	Lets you identify and set up the test environment, including information about the device under test. The Test App includes relevant information in the final HTML report.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (for example, channels used in test, voltage levels, etc.).
Connect	Shows you how to connect the oscilloscope to the device under test for the tests that are to be run.
Run	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automate	Lets you construct scripts of commands that drive execution of the application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE

In the **Configure** tab, the values for all such Configuration parameters that are Oscilloscope-dependent, will correspond to the Oscilloscope Model (DSOs or UXRs), where you are running the Test Application.

Setting up the Thunderbolt 3 Test Application

In order to run the electrical compliance tests on a Thunderbolt DUT operating at a bit rate of either 10.3125 GB/s, 20.625 GB/s, 10 GB/s. 20 GB/s or all, you must set up the Thunderbolt 3 Test Application to be able to view and select the required tests.

1 Start the Thunderbolt 3 Test Application. See "Starting the Thunderbolt 3 Test Application" on page 37.

2 Under the **Set Up** tab, select the following options, as shown in Figure 7.

a **Device Type:** – Select DUT Type as either **Device** (default) or **Host**.

b **Number of Port:** – Select **1 Port** (default) or **2 Ports**.

c **Port Name:** –This drop-down field allows you to select a port name or even type a custom name for the ports being used for testing. Default values are **Port 1** and **Port 2**.

d **Test Lane:** – The drop-down options, when the Test App is launched on a 4-Channel Oscilloscope, are different from that on a 2-Channel Oscilloscope.

- On a 4-Channel Oscilloscope–From the drop-down options, select either **Both Lanes** (default), **Lane 0 only** or **Lane 1 only**; depending on the number of lanes being used for testing.
- On a 2-Channel Oscilloscope–From the drop-down options, select either **Lane 0 only** or **Lane 1 only**; depending on the number of lanes being used for testing.

e **Bit Rate** – Select either one or more bit-rates to indicate the signal speed on the DUT.

f **Product Info** – Helps you in proper identification of the DUT on HTML reports. This option is particularly useful when running compliance tests on multiple DUTs.

- **Device Identifier:** – Type an appropriate name/identifier for the DUT, which is being tested. The entries are saved such that you may select the values again later, if required.
- **User Description:** – Type an appropriate description for the DUT, which is being tested. The entries are saved such that you may select the values again later, if required.
- **Comment:** – Type appropriate comments, if required.

g **Thunderbolt Automation Controller** – Select **Enable Automation** to enable the automation controller. Use this feature for remote configuration and controlling of a Thunderbolt Host or Device, which is a usually a remote PC or a Thunderbolt Micro-Controller.

h **USB Type-C Test Controller** – Select **Enable Type-C Controller** to set up the Type-C controller. Use this feature to connect to the Type-C controller device along with defining the Type-C capability of the Thunderbolt DUT with Type-C implementation.

For more information about using the **Thunderbolt Automation Controller** and **USB Type-C Test Controller** features, refer to the *Keysight D9030TBTC Thunderbolt 3 Test Application Online Help*.

i **Test Setup**– Click the **Test Setup** button to set up the following calibration prerequisites:

- **Preset Calibration** – Required to run the Transmitter Preset Calibration tests.
- **CTLE Calibration** – Required to run the Transmitter CTLE Calibration tests.
- **Power Profile** – Appears only when the **Enable Type-C Controller** is selected. Defines the power supply and demand requirements of a Thunderbolt DUT with Type-C implementation, which may be connected either as a provider or a consumer.

j **Channel Skew Calibration** – Click the **Calibrate Setup** button to perform **Channel Skew Calibration** before running the tests. Required to calibrate Channel Skew on the Oscilloscope Channels where the DUT is connected.

See "Calibration Setup for Compliance Tests" on page 47 for more information on these calibration options.

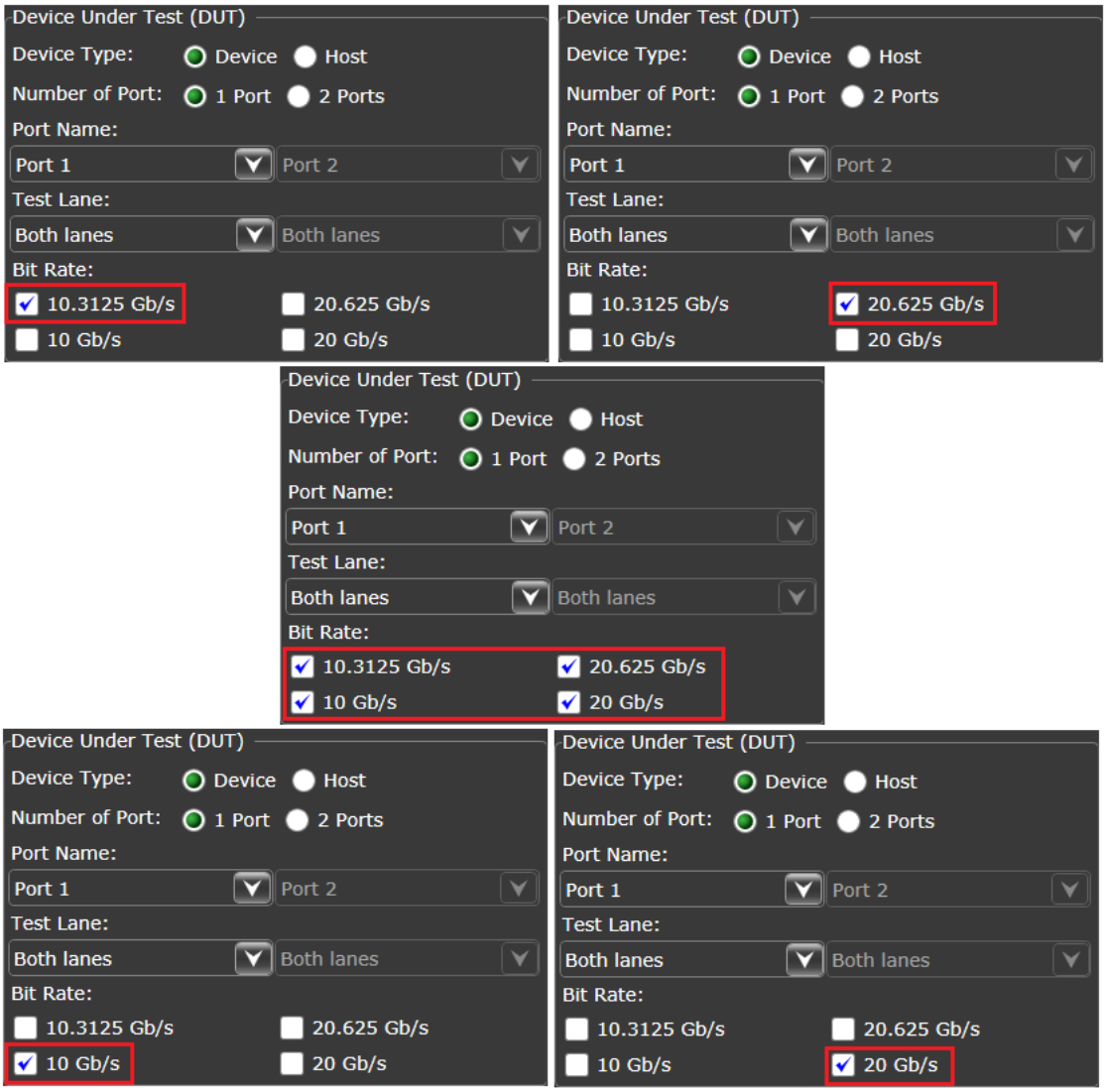


Figure 7 Set Up options for DUT Type "Device" on a 4-Channel Oscilloscope

3 Based on your choices under the **Set Up** tab, the **Select Tests** tab filters tests into test groups corresponding to one or more selected bit-rates and the selected option for device type, port and lane.

For example, Figure 8 shows how test groups are filtered when you select **Device Type:** as **Device**, **Number of Port** as **2 Ports** and **Test Lane:** as **Both lanes** along with selecting all bit rates. Similarly, Figure 9 shows how test groups are filtered when only one bit-rate is selected along with setting **Device Type:** as **Host**, **Number of Port** as **1 Port** and **Test Lane:** as **Lane 0 only**. Select the tests that you want to run using the Thunderbolt 3 Test Application. Refer to the *Keysight D9030TBTC Thunderbolt 3 Test Application Online Help* to know more about how to select tests.

NOTE The **Test Lane** drop-down options in the **Set Up** tab, when the Test App is launched on a 4-Channel Oscilloscope, are different from that on a 2-Channel Oscilloscope. Therefore, on the latter instrument, only **Lane 0 only** or **Lane 1 only** options appear, as otherwise shown in Figure 8.

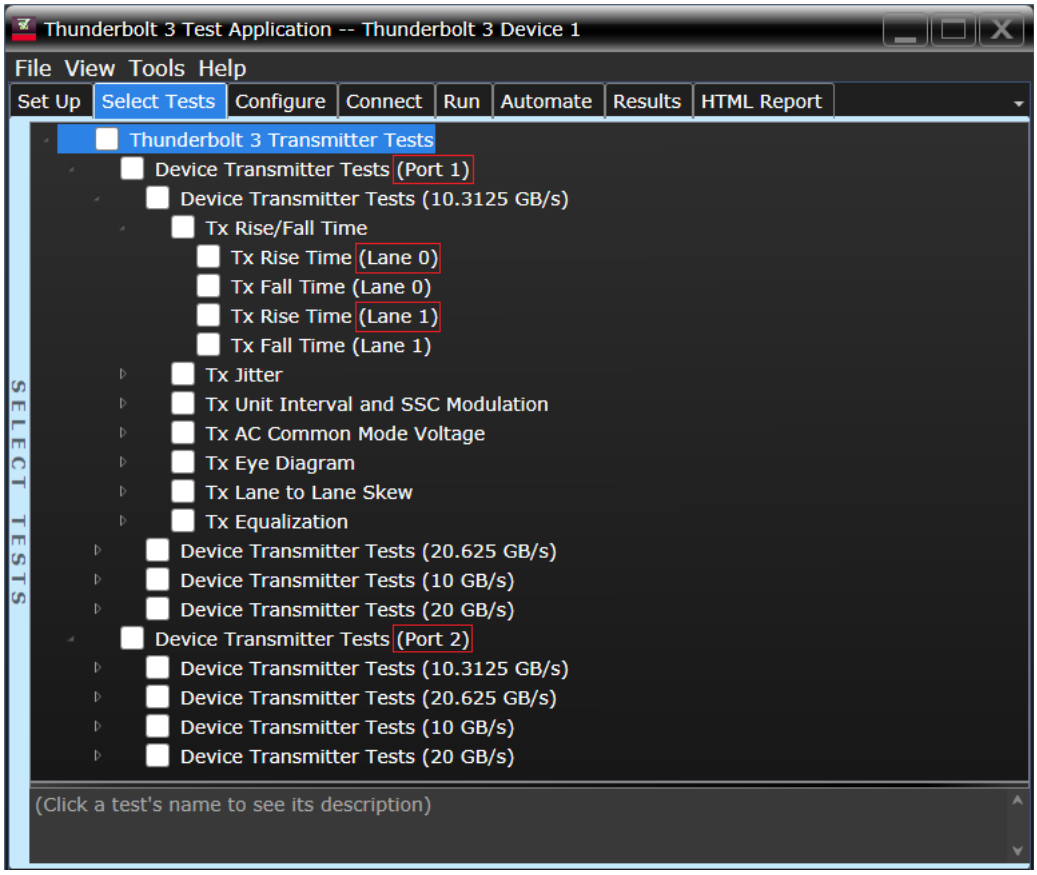


Figure 8 Selecting Transmitter Tests for all bit rates

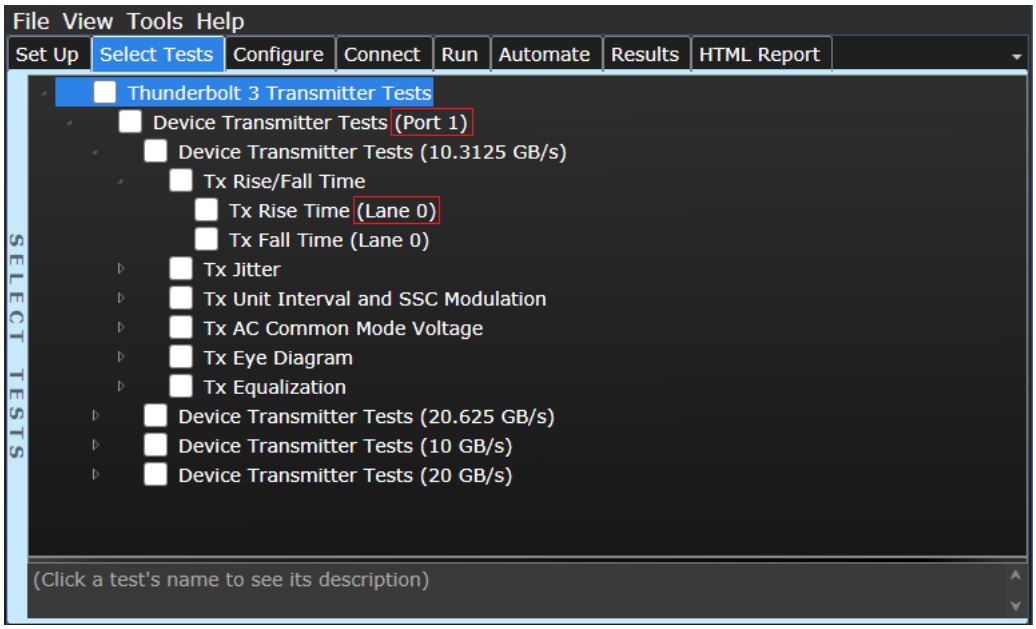


Figure 9 Select Transmitter Tests for a single bit rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only.**

4 Under the **Configure** tab, you may modify the values for various configurable options associated with the compliance tests. By default, the Thunderbolt 3 Test Application sets the values of these options to the optimum value according to the standard specifications.

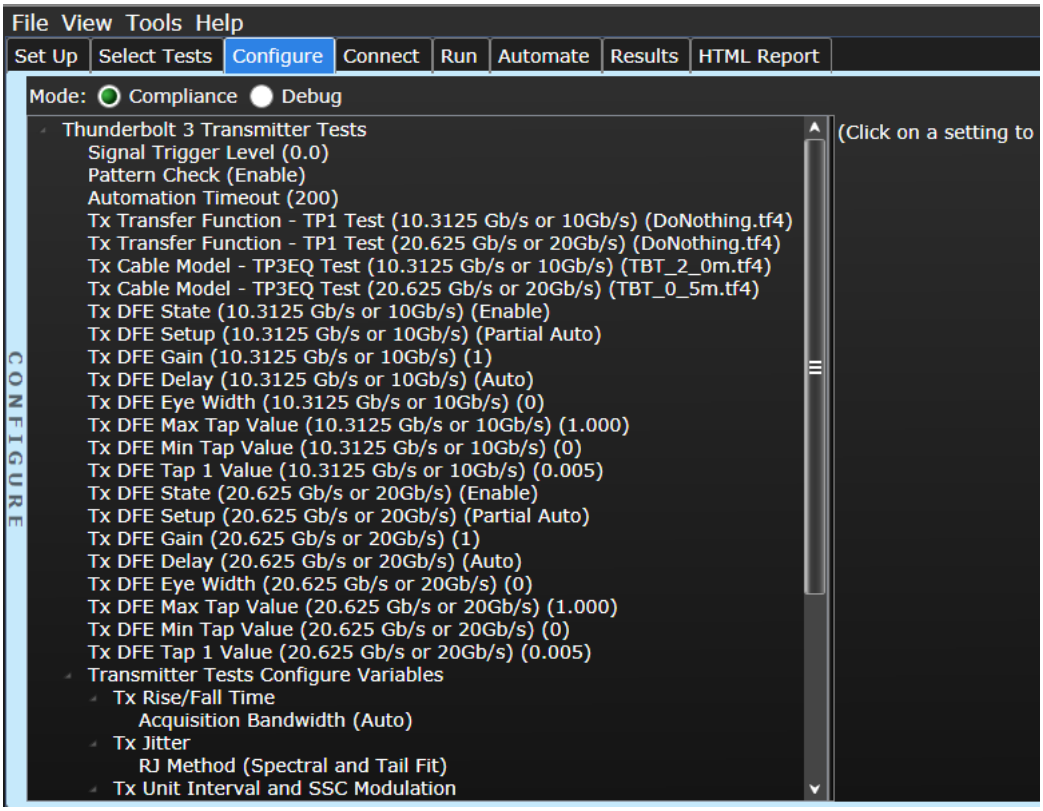


Figure 10 Configure options for Thunderbolt 3 Tests

5 Under the **Connect** tab, the TThunderbolt 3 Test Application displays a Connection Diagram along with a list of instructions. Figure 11 and Figure 12 show the connection diagrams for a 2-Lane set up and for a 1-Lane set up, respectively, on a 4-Channel Oscilloscope, whereas Figure 13 shows the connection diagram for the “Lane 0 Only” set up on a 2-Channel Oscilloscope. If you have already set up a physical connection, you may verify else connect the DUT with the Oscilloscope as shown under this tab. Note that during some test runs, the application may prompt you for a change in physical connection/setup.

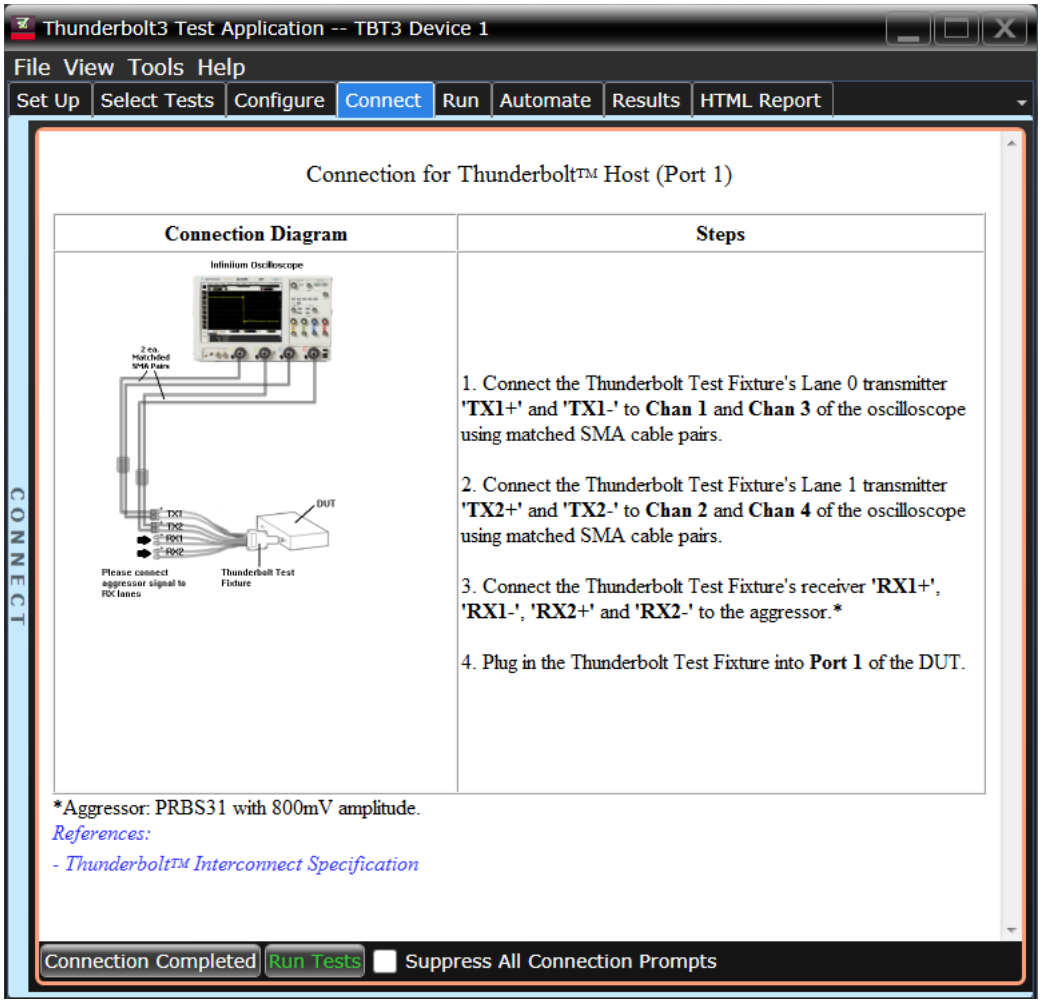


Figure 11 Connection Diagram and Instructions for a 2-Lane test set up on a 4-Ch Oscilloscope

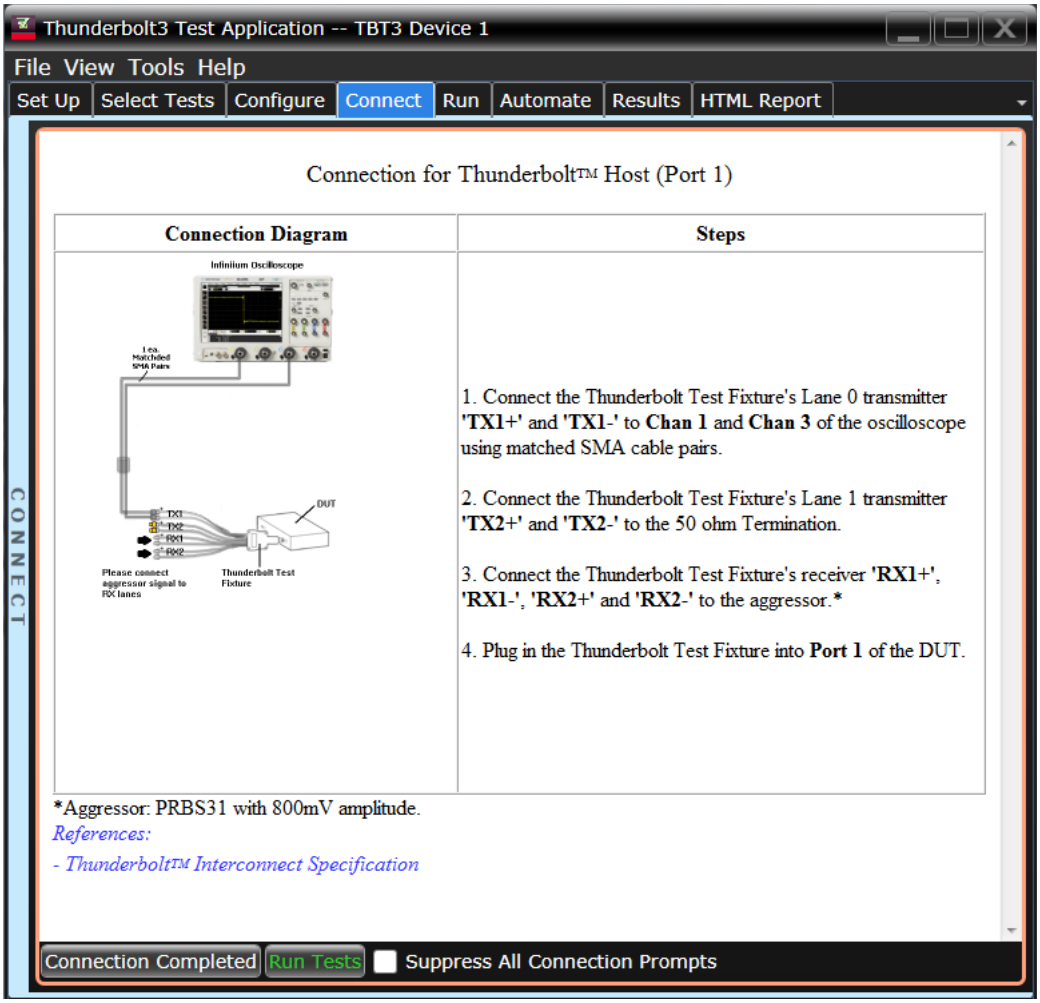


Figure 12 Connection Diagram and Instructions for a 1-Lane test set up on a 4-Ch Oscilloscope

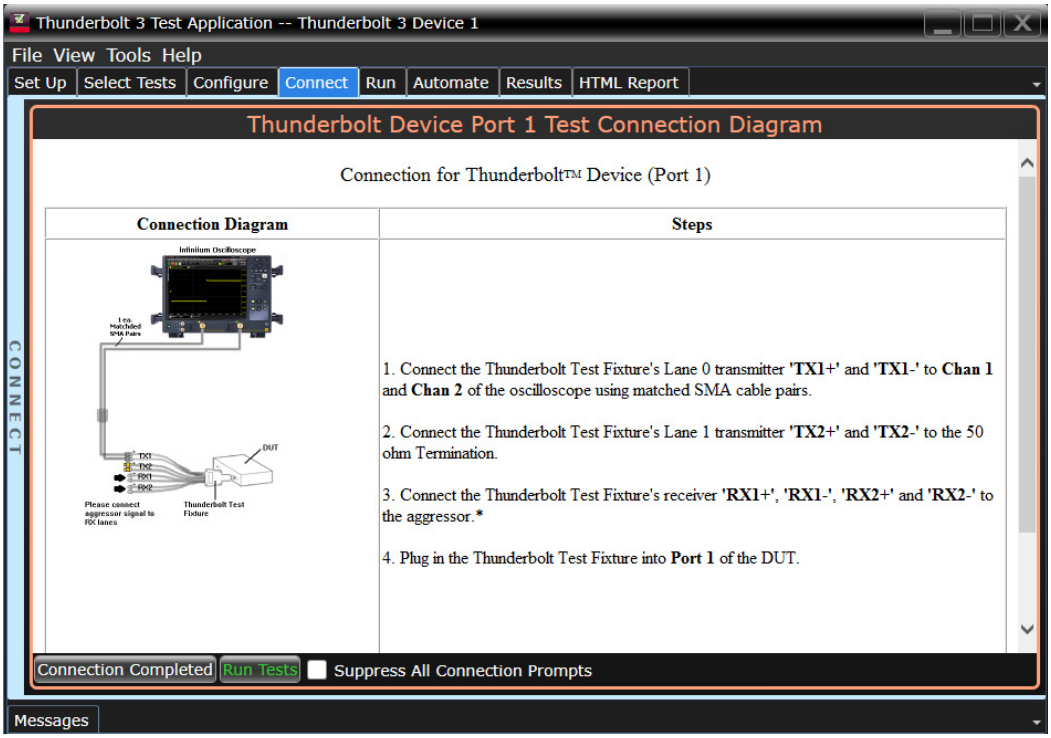


Figure 13 Connection Diagram and Instructions for “Lane 0 Only” on 2-Channel Oscilloscope

6 Once you have performed steps 1 to 5, you are ready to run compliance tests on the Thunderbolt DUT. Additionally, you may configure/modify the run settings, automate options in the Test Application, view, export and print the test results and the HTML reports generated by the Test Application. Refer to the *Keysight D9030TBTC Thunderbolt 3 Test Application Online Help* to know more about how to use the Test Application.

Calibration Setup for Compliance Tests

Before running compliance tests on a Thunderbolt DUT, it is imperative that the testing equipment and its accessories be calibrated. The Thunderbolt 3 Test Application provides the options to run Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration.

Channel Skew Calibration

In order to achieve accurate test results and to verify that the Device under test is compliant to the standards, it is necessary to calibrate the Oscilloscope channels that are connected via cables to the Thunderbolt DUT.

Perform the following:

1 In the **Channel Skew Calibration** area of the **Set Up** tab of the Thunderbolt 3 Test Application, click the **Calibrate Setup** button.

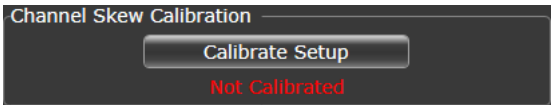


Figure 14 Channel Skew Calibration area under the **Set Up** tab

2 The **Calibration** window appears, where the **Channel Skew Calibration** tab is displayed by default, as shown in Figure 15 for a 4-Channel Oscilloscope and in Figure 16 for a 2-Channel Oscilloscope.

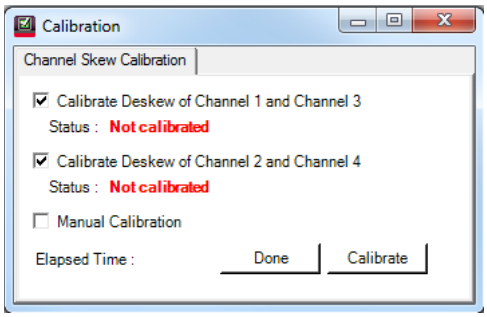


Figure 15 Options for Channel Skew Calibration on a 4-Channel Oscilloscope

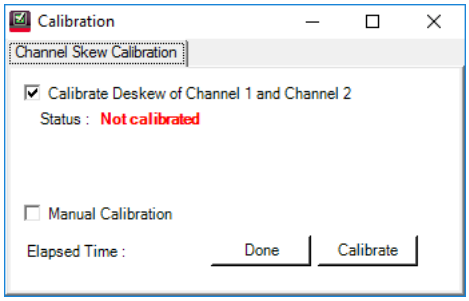


Figure 16 Options for Channel Skew Calibration on a 2-Channel Oscilloscope

Under the **Channel Skew Calibration** tab, the Thunderbolt 3 Test Application displays the status of the Oscilloscope Channels that have been calibrated for de-skew. As shown in the images above, the options are checked by default and the status of each of these options is **Not Calibrated**. You may also select the **Manual Calibration** check box to perform Channel Skew Calibration later.

To start calibration of the selected Oscilloscope channel pairs, click the **Calibrate** button. The **Test Instruction for Thunderbolt 3 Compliance** window appears.

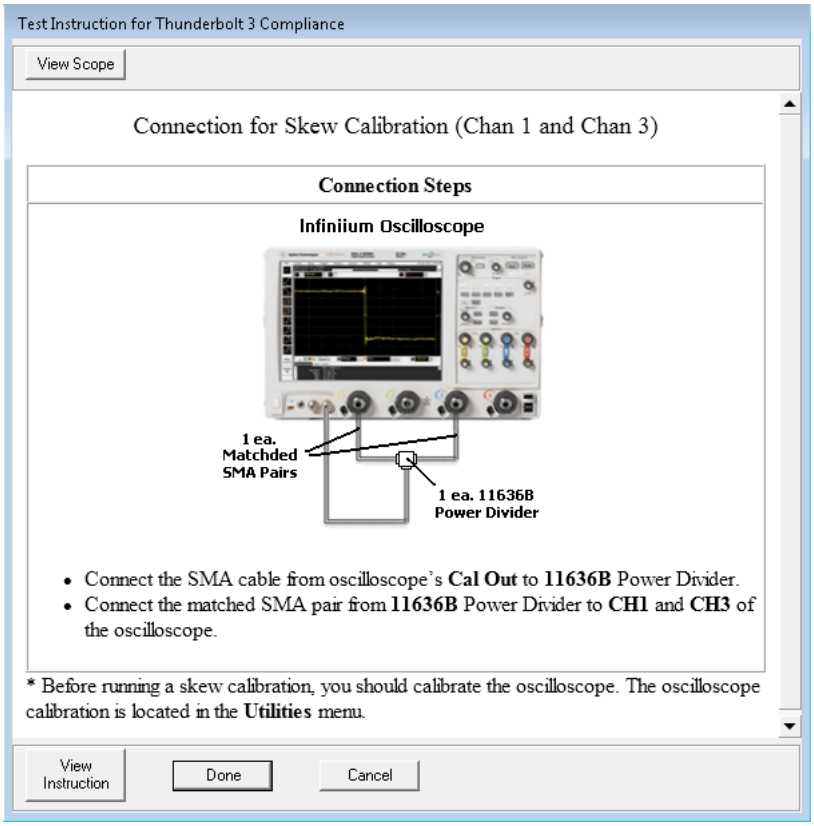


Figure 17 Instructions for Channel Skew Calibration for the selected Channels on a 4-Ch Oscilloscope

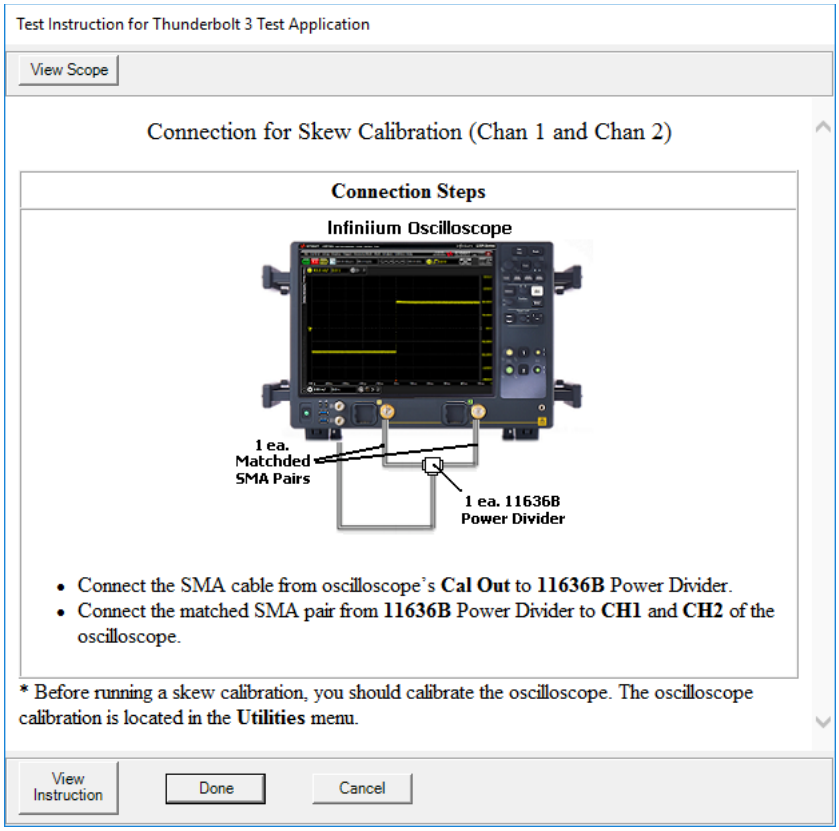


Figure 18 Instructions for Channel Skew Calibration for the selected Channels on a 2-Ch Oscilloscope

The **Test Instruction for Thunderbolt 3 Compliance** window provides instructions and connection diagram required to be set up to perform Channel Skew Calibration. Note that before you start performing Channel Skew Calibration, the Oscilloscope must have been calibrated.

On the **Test Instruction for Thunderbolt 3 Compliance** window,

1 Click the **View Scope** button to minimize this window and to see the Oscilloscope screen for the waveform and to use the Infiniium controls to perform Oscilloscope Calibration (if it has not been done yet).

2 Click the **View Instruction** button to maximize the window to view the instructions and the connection diagram again.

3 Once you have set up the physical connection for Channel Skew Calibration for the respective channels, click **Done** to begin Calibration. You may click **Cancel** at any point to simply return to the **Calibration** window.

When you click **Done**, the **Calibration** window displays again with the updated Status along with the time elapsed during this process, as shown in Figure 19 and :

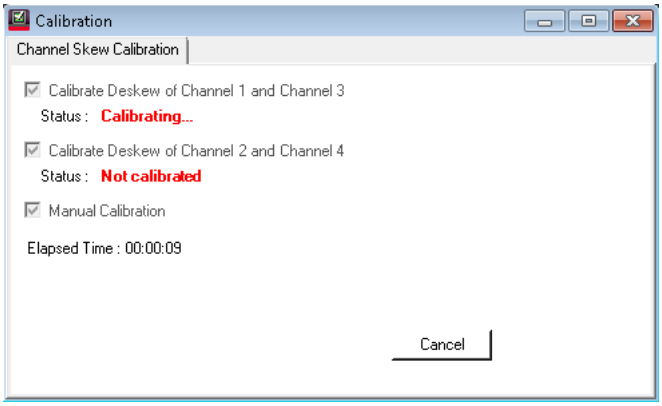


Figure 19 Changes in Calibration status on a 4-Channel Oscilloscope

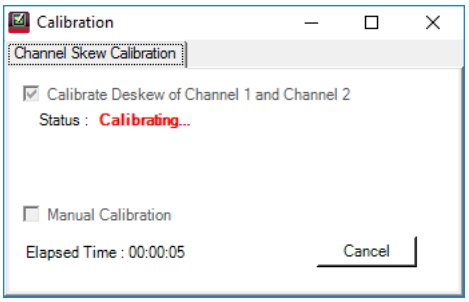


Figure 20 Changes in Calibration status on a 2-Channel Oscilloscope

Once the Calibration process is successfully done, the status changes to **Calibrated**. You may click **Cancel** to stop the process of Channel Skew Calibration at any time.

4 After the Channel Skew Calibration is complete, click the **Done** button to return to the Thunderbolt 3 Test Application Test Environment Setup.

Preset Calibration

The **Preset Calibration** tab allows you to select the preset number, which has been set on the Thunderbolt DUT, to be used in the Thunderbolt 3 Test Application. You may also perform the preset sweep to find the optimum preset.

Perform the following:

1 In the **Test Setup** area of the **Set Up** tab of the Thunderbolt 3 Test Application, click the **Test Setup** button.

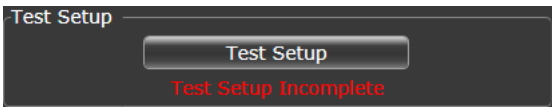


Figure 21 Test Setup area under the **Set Up** tab

2 The **Test Setup** window appears, where the **Preset Calibration** tab is displayed by default, as shown in Figure 22 for a 4-Channel Oscilloscope and Figure 23 for a 2-Channel Oscilloscope.

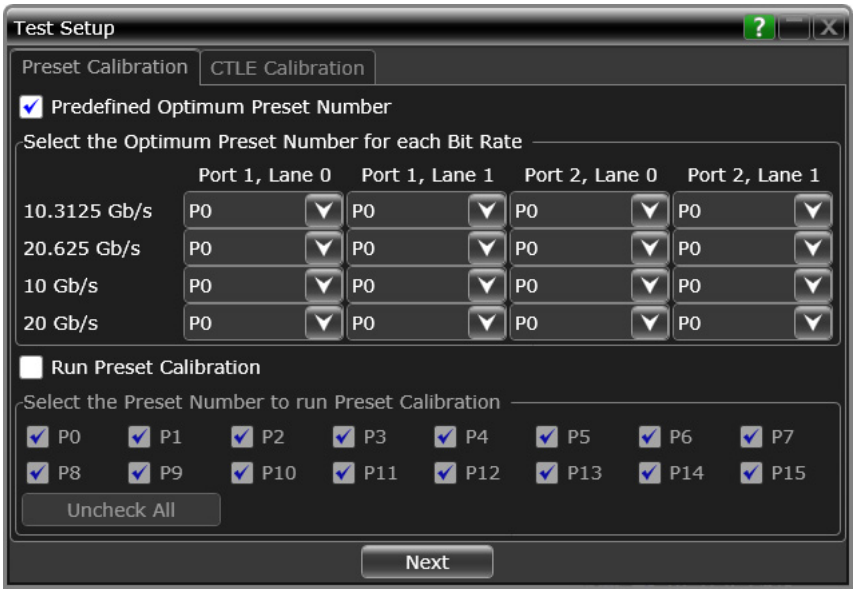


Figure 22 Default view of the Preset Calibration tab on a 4-Channel Oscilloscope

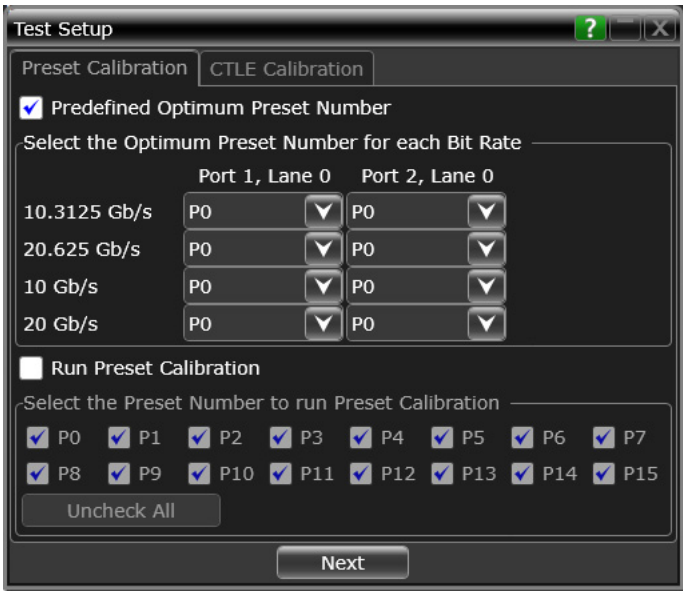


Figure 23 Default view of the Preset Calibration tab on a 2-Channel Oscilloscope

Under the **Preset Calibration** tab,

1 By default, the **Predefined Optimum Preset Number** check-box is selected and the default Preset Number for the selected bit rates is set to **P0**.

2 From the **Select the Optimum Preset Number for each Bit Rate** area, select a preset number from the drop-down options corresponding to each bit-rate and port-lane combination.

3 Select the **Run Preset Calibration** check-box only if you wish to run Preset Calibration to find the optimum preset value for the DUT. By default, all preset values are selected.

4 In the **Run Preset Calibration**, you may de-select any of the preset numbers to exclude them from preset calibration. You may use the **Uncheck All** or **Check All** radio buttons to perform this action as well.

NOTE By default, the test group for **Preset Calibration** for each selected bit-rate is hidden in the **Select Tests** tab when **Predefined Optimum Preset Number** is selected for the respective bit-rates. To view and select the **Preset Calibration** tests in the **Select Tests** tab, select the **Run Preset Calibration** option in the **Test Setup** window of the **Set Up** tab.

5 Click **Next** to move to the next tab.

CTLE Calibration

The **CTLE Calibration** tab allows you to select the Continues-Time Linear Equalizer (CTLE) used for the TP3EQ tests in the Thunderbolt 3 Test Application. You may also perform the CTLE DC gain sweep to find the optimum CTLE DC gain.

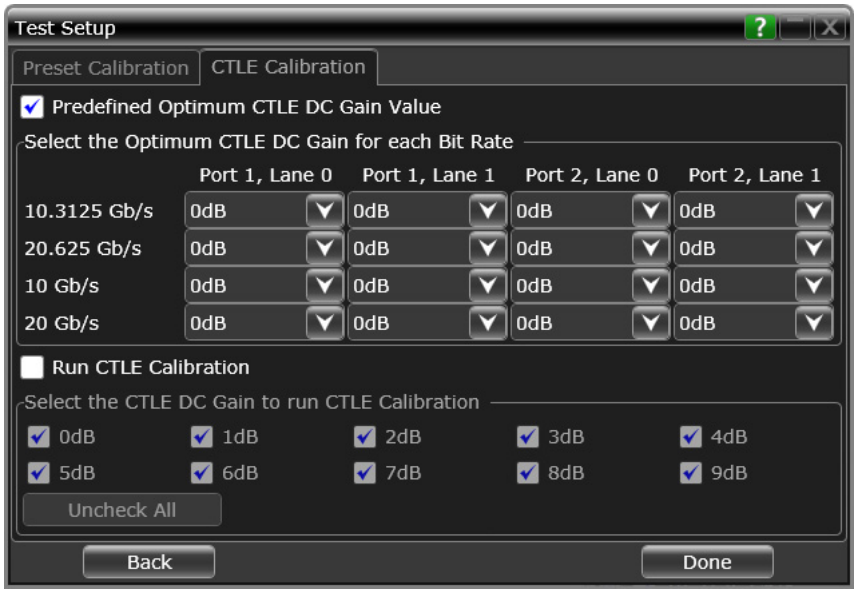


Figure 24 Default view of the CTLE Calibration tab on a 4-Channel Oscilloscope

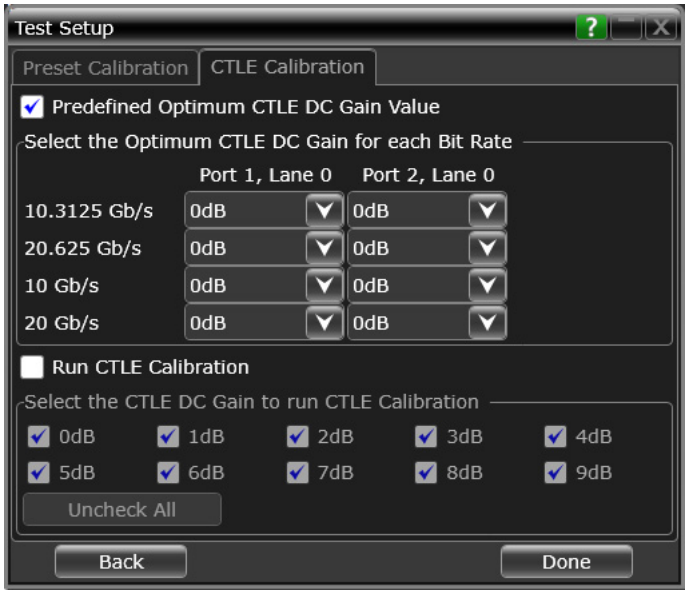


Figure 25 Default view of the CTLE Calibration tab on a 2-Channel Oscilloscope

Under the **CTLE Calibration** tab,

1 By default, the **Predefined Optimum CTLE DC Gain Value** check-box is selected and the default DC Gain value for the selected bit rates is set to **0dB**.

2 From the **Select the Optimum CTLE DC Gain for each Bit Rate** area, select a DC Gain value from the drop-down options corresponding to each bit-rate and port-lane combination.

3 Select the **Run CTLE Calibration** check-box only if you wish to run CTLE Calibration to find the optimum DC Gain value for the DUT. By default, all DC Gain values are selected.

4 In the **Run CTLE Calibration** area, you may de-select any of the DC Gain values to exclude them from CTLE calibration. You may use the **Uncheck All** or **Check All** radio buttons to perform this action as well.

NOTE

By default, the test group for **CTLE Calibration** for each selected bit-rate is hidden in the **Select Tests** tab when **Predefined Optimum CTLE DC Gain Value** is selected for the respective bit-rates. To view and select the **CTLE Calibration** tests in the **Select Tests** tab, select the **Run CTLE Calibration** option in the **Test Setup** window of the **Set Up** tab.

5 Click **Done** to save any modifications done to the **Test Setup** window and to return to the Thunderbolt Test Environment Setup.

6 If you have enabled Type-C Controller in the **Set Up** tab, the **Power Profile** tab is also displayed in the **Test Setup** window. Click the **Next** button, which appears instead of **Done**.

Power Profile

The **Power Profile** tab allows you to select the voltage and current requirements when the Thunderbolt DUT with the Type-C implementation is connected for testing.

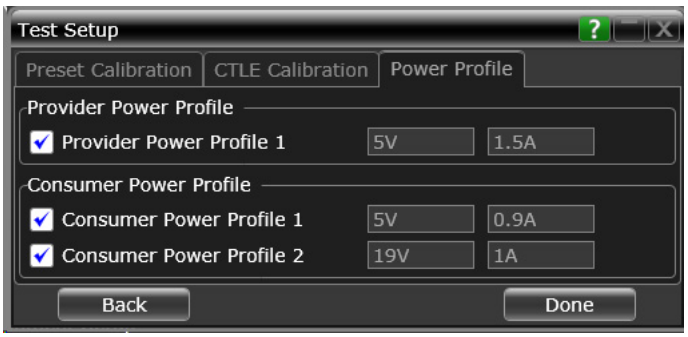


Figure 26 Default view of the Power Profile tab

Under the **Power Profile** tab,

1 Use the check-box to select or de-select one of listed **Provider Power Profile** or **Consumer Power Profile** options.

   If the connected Thunderbolt3 DUT with Type-C behaves as the source of power supply, it is identified and denoted as Provider Power Profile. If the DUT consumes power, it is identified and denoted as Consumer Power Profile.

2 The number of power profiles displayed varies based on the power profile supported by the DUT, which in turn, is obtained during the DUT Capability Query.

3 Click **Done** to save any modifications done to the **Power Profile** tab and to return to the Thunderbolt 3 Test Application Test Environment Setup.

4 Host / Device Thunderbolt 3 Transmitter Testing

The Keysight D9030TBTC Thunderbolt 3 Test Application enables compliance testing of the Host and Device Transmitter systems operating at bit rates of either 10.3125 GB/s, 20.625 GB/s, 10 GB/s or 20 GB/s; based on *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.

System Components in Thunderbolt Technology

The following section help you understand an overview of the system components associated with Transmitter testing in the Thunderbolt Technology.

Overview

You may construct a range of system Devices using the networking architecture of the Thunderbolt Technology. The Thunderbolt Technology connector ports, which function either as “Upstream” (pointing towards a Host) or “Downstream” (pointing towards an Endpoint), characterize the Thunderbolt Technology link. A network of Thunderbolt Technology links, after they are connected and configured, form a tree topology, such that the upstream ports lead to a Thunderbolt Host at the root of the tree. For example, a Thunderbolt Device may exchange information with the Thunderbolt Host on its upstream Thunderbolt Technology connector, thereby behaving as an information channel between the Host and Devices to its downstream port(s), which may be connected directly or indirectly. See Figure 27.

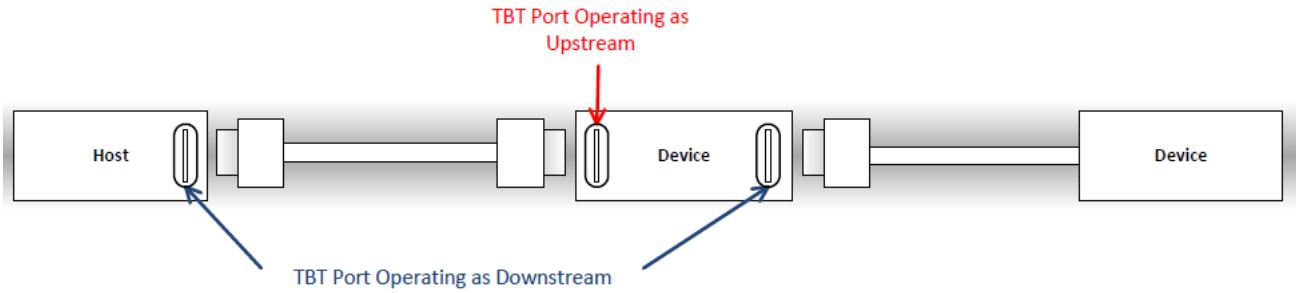


Figure 27 Thunderbolt Technology Link Connection Block Diagram

An inter-domain connection is established when two Thunderbolt Host systems are connected directly. An inter-domain connection is also referred to as a peer-to-peer connection and is also formed when two downstream ports, originating from two different Host trees, are connected.

You shall find that in the inter-domain connections, memory to memory transactions occur for communication between the Host systems and the system software configures the connections for the Thunderbolt network in their respective tree, such as DisplayPort connections and PCIe transactions to Devices are carried out with the Host in their respective tree. See Figure 28.

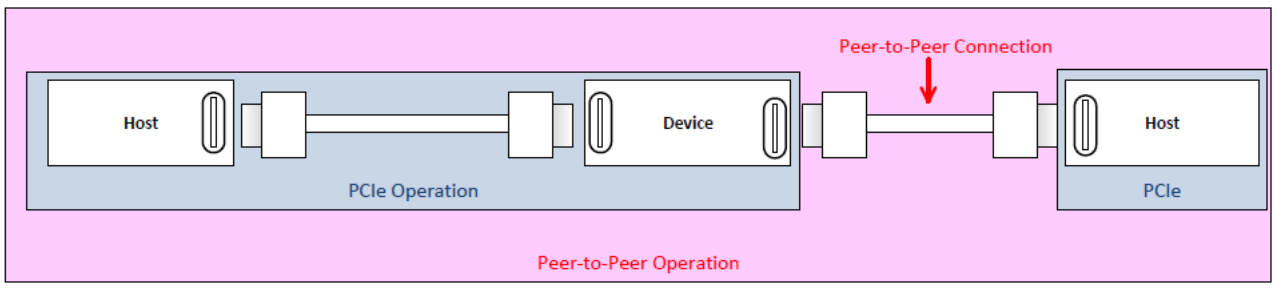


Figure 28 Thunderbolt Technology Peer-to-Peer Connection Block Diagram

The Thunderbolt Technology link consists of a Thunderbolt Host, a Thunderbolt Display, a Thunderbolt Adapter and a Thunderbolt Application Device. A Thunderbolt Display, a Thunderbolt Adapter or a Thunderbolt Application Device are generically referred to as Thunderbolt Devices.

Thunderbolt Host

This component is a usually a computer. A Thunderbolt Host has one or more “Downstream” Thunderbolt Technology connector ports, but no “Upstream” Thunderbolt Technology connector ports. However, Thunderbolt Hosts can be connected peer-to-peer. A Thunderbolt Host provides the role of Thunderbolt network discovery and configuration. There shall be at least one Thunderbolt Host in a Thunderbolt network. A Thunderbolt network with more than one Thunderbolt Host can provide peer-to-peer communications between the Thunderbolt Hosts present on the network. A Thunderbolt Host Type-C includes the following:

- A Thunderbolt Controller, which contains one or more DisplayPort input interfaces, a PCI Express interface, and one or more Thunderbolt Technology interfaces.
- A multiplexer, which selects either Thunderbolt, DP v1.2, or USB r3.1 data. The multiplexer is integrated into the 3rd Generation Thunderbolt Controller.
- A Link Controller with a UART interface for managing operation and power states of the Thunderbolt link when in the Thunderbolt Alternate Mode. The Link Controller is integrated into the 3rd Generation Thunderbolt Controller.
- A USB PD Port Controller implemented as a DRP with the ability to support the Thunderbolt and DisplayPort Alternate Modes.
- At least one USB Type-C connector.

Table 2 lists the Thunderbolt Host rules in conjunction with the USB Type-C connector.

Table 2 Thunderbolt Host Rules with USB Type-C connector

Technology	Thunderbolt Host Rules
USB	▪ Hosts shall support USB r3.1 gen1 and gen2. Hosts shall support USB r2.0. ▪ Hosts shall support USB PD and Biphase Mark Coding. ▪ Hosts shall provision power as defined in Section 7.3 of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
Thunderbolt	▪ Hosts shall support 3rd Generation Thunderbolt with the USB Type-C connector. ▪ Hosts shall support the pin mapping as defined in Section 7.5.1 of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
PCIe	▪ Hosts shall connect PCIe to the Thunderbolt Controller. ▪ One port Hosts are recommended to connect 4-lanes of PCIe Gen3 to the Thunderbolt Controller. ▪ One port Hosts shall connect at least 2-lanes of PCIe Gen3 to the Thunderbolt Controller. ▪ Two port Hosts shall connect 4-lanes of PCIe Gen3 to the Thunderbolt Controller. ▪ Hosts shall support PCIe hot plug.
DisplayPort	▪ Hosts shall redrive DisplayPort from the Thunderbolt Controller to the USB Type-C connector. ▪ One port Thunderbolt Hosts are recommended to connect two DP v1.2 streams (4-lanes each) to the Thunderbolt Controller. ▪ One port Thunderbolt Hosts shall connect at least one DP v1.2 stream (4-lanes) to the Thunderbolt Controller. ▪ Two port Thunderbolt Hosts shall connect at least two DP v1.2 streams (4-lanes each) to the Thunderbolt Controller. ▪ Hosts shall support the pin mapping as defined in Section 7.5.2 of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.

Thunderbolt Device

A Thunderbolt Device has at least one port that is capable of operating as an “Upstream” port and contains a Thunderbolt Controller and optionally a PCIe to I/O Bridge to another interface such as FireWire, Ethernet, or eSATA. The Thunderbolt Device may present the other interface connector or may include internal functionality that is appropriate to a device. Thunderbolt Controllers contain some PCIe to I/O bridging capabilities and additional I/O Bridge chips may not be needed. You may refer to the appropriate Thunderbolt Controller datasheet for more information.

When the Thunderbolt Device is connected to the Thunderbolt Host, the bridge chip functions as if it were connected directly to the Host's PCIe bus. A Thunderbolt Device with a downstream port, shall provide DP v1.2 support or USB r3.1 support in the case where a USB Type-C cable and a USB or DP Device are connected. Examples of Thunderbolt Devices include a PCIe expansion chassis or a RAID array controller, a Thunderbolt to FireWire adapter, a Thunderbolt to Ethernet adapter, a Thunderbolt Display and so on.

A Thunderbolt Device may have one or more ports, which can operate as "Downstream" port(s). A Thunderbolt Device may or may not have a Thunderbolt cable permanently attached. A Thunderbolt Device with a Thunderbolt cable permanently attached is called a Tethered Device.

Thunderbolt Display—A Thunderbolt Display is a specific type of Thunderbolt Device. A Thunderbolt Display has at least one port, which is capable of operating as an Upstream Thunderbolt Technology connector port and an integrated display which shall display DisplayPort format information tunneled through the Thunderbolt Technology link. A Thunderbolt Display may also have a second port operating as a "Downstream" port. Downstream ports operate as the Thunderbolt Technology connector ports and optionally support USB r3.1 when a USB device is connected or DP on Type-C when a DisplayPort adapter is connected. A Thunderbolt Display may also contain PCIe subsystems connected to the Thunderbolt Controller's PCIe interface, for example a Gigabit Ethernet controller.

Thunderbolt Links and Lanes

A link is defined as one or more dual-simplex communication paths between two Thunderbolt Controllers. A link may be composed of multiple lanes or channels. A link is symmetric in that each direction of the link shall support the same number of lanes and each lane shall operate at the same signaling rate.

A lane is composed of two differential signal pairs, one transmitting and one receiving. Each differential pair operates at a signaling rate which defines the speed of communication for that lane. Multiple lanes may be aggregated (bonded) to scale bandwidth. The Thunderbolt Technology connector can be connected to 1 or 2 Thunderbolt Lanes, depending on the implementation or Thunderbolt rules.

3rd Generation Thunderbolt Compliance Methodology

System Compliance Test Point Definitions

The 3rd Generation Thunderbolt defines the following reference points for compliance testing of Host/Device Thunderbolt Transmitter Systems:

1 TP1—Reference measurement point located at the plug side of the Host/Device Transmitter output. Used as a reference point for defining the Host/Device Transmitter and the Active Cable/Adapter Receiver specifications.

2 TP2—Reference measurement point located at the plug side of the Host/Device Receiver input. Used as a reference point for defining the Active Cable/Adapter Transmitter and the Host/Device Receiver specifications.

3 TP3EQ—Reference measurement point located at the far-end side of a passive cable or at the output of a tethered device. Used as a reference point for passive installations and tethered devices. All the measurements at this point are done after applying reference equalization.

For Host / Device Transmitter testing, all measurements shall be referenced to the TP1/TP3EQ compliance points defined above and as shown in Figure 29. Calibration shall be applied in cases where direct measurement at TP1 is not feasible.

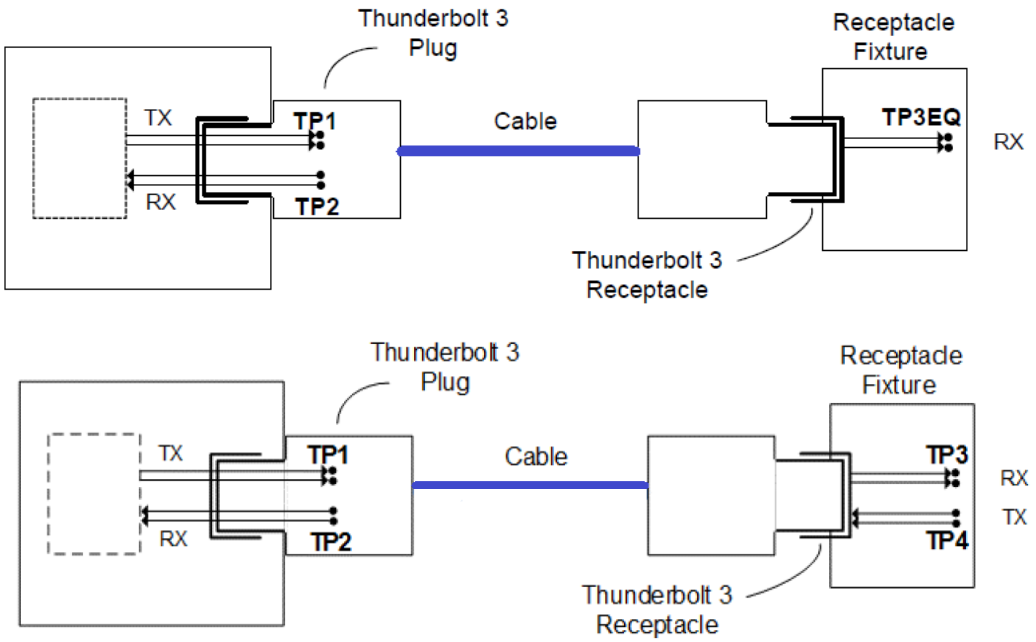


Figure 29 Thunderbolt Compliance Points Definition

AC Coupling Capacitors

The high speed electrical interfaces shall be AC-coupled. The Host/Device transmit paths shall include AC-coupling capacitance between 165nF and 265nF. In addition, the plugs of the Active Cable and the Tethered Device should include AC-coupling capacitance between 165nF and 265nF placed at their output transmit path. Capacitors shall not be placed on the high-speed receiver paths of the different 3rd Generation Thunderbolt components.

Jitter and Eye Measurement Methodology

The Thunderbolt jitter and eye diagram specifications are all referenced to a golden clock-and-data recovery (CDR) function, meaning that all measurements shall be performed after applying appropriate tracking on the signal's phase. The reference CDR is modeled by a 2nd order PLL response (type II), which derives the following jitter rejection mask, described in Laplace domain, as described in Figure 30:

$$H_{jitter}(s) = \frac{s^2}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + {\omega_n}^2}$$

Where:

$s = j \cdot 2 \cdot \pi \cdot f$, ζ *is the damping factor,*

ω_n *is the natural frequency of the system*

Figure 30 Jitter Rejection Mask described in Laplace domain

Table 3 defines the 3rd Generation Thunderbolt Reference CDR Parameters:

Table 3 3rd Generation Thunderbolt Reference CDR Parameters

Speed	Damping Factor	Cutoff Frequency [Hz]
Gen2 (10.3125 GB/s or 10 GB/s)	0.94	5MHz
Gen3 (20.625 GB/s or 20 GB/s)	0.94	5MHz

Reference Equalization Function

All the measurements done at the output of the cable assembly, denoted as TP3EQ, should be referenced to a golden receiver equalization function, that is, all measurements shall be performed after applying appropriate equalization on the measured signals. The reference receiver applied at TP3EQ comprises of parametric Continuous-Time-Linear-Equalizer (CTLE) and Decision-Feedback-Equalizer (DFE), as described in Figure 31. For each measurement referenced to TP3EQ, make sure to set the best equalization parameters such that the calculated eye-diagram is optimized.

Reference CTLE

The equation, shown in Figure 31, describes the frequency response for the Converged IO reference continuous time linear equalizer (CTLE) that must be used for compliance testing:

$$H(s) = 1.41 \cdot w_{p2} \cdot \frac{s + \frac{A_{DC}}{1.41} \cdot w_{p1}}{(s + w_{p1}) \cdot (s + w_{p2})}$$

Where:

A_{DC} *is the DC gain*

$$w_{p1} = \begin{cases} 2 \cdot \pi \cdot 1.5e9 \ \frac{rad}{Sec} & Speed = 10.3125\ Gb/s \\ 2 \cdot \pi \cdot 5e9 \ \frac{rad}{Sec} & Speed = 20.625\ Gb/s \end{cases}$$

$$w_{p2} = \begin{cases} 2 \cdot \pi \cdot 5e9 \ \frac{rad}{Sec} & Speed = 10.3125\ Gb/s \\ 2 \cdot \pi \cdot 10e9 \ \frac{rad}{Sec} & Speed = 20.625\ Gb/s \end{cases}$$

$s = j \cdot 2 \cdot \pi \cdot f$ *is the frequency in Laplace domain*

Figure 31 Frequency Response Equation for 3rd Generation Thunderbolt CTLE

Apply ten different CTLE configurations such that the value of A_{DC} is one of $\{10^{-x/20} : x = 0, 1, 2, \ldots, 9\ [dB]\}$.

Figure 32 and Figure 33 show the Frequency Response of the 3rd Generation Thunderbolt Reference CTLE for Gen2 devices and for Gen3 devices, respectively.

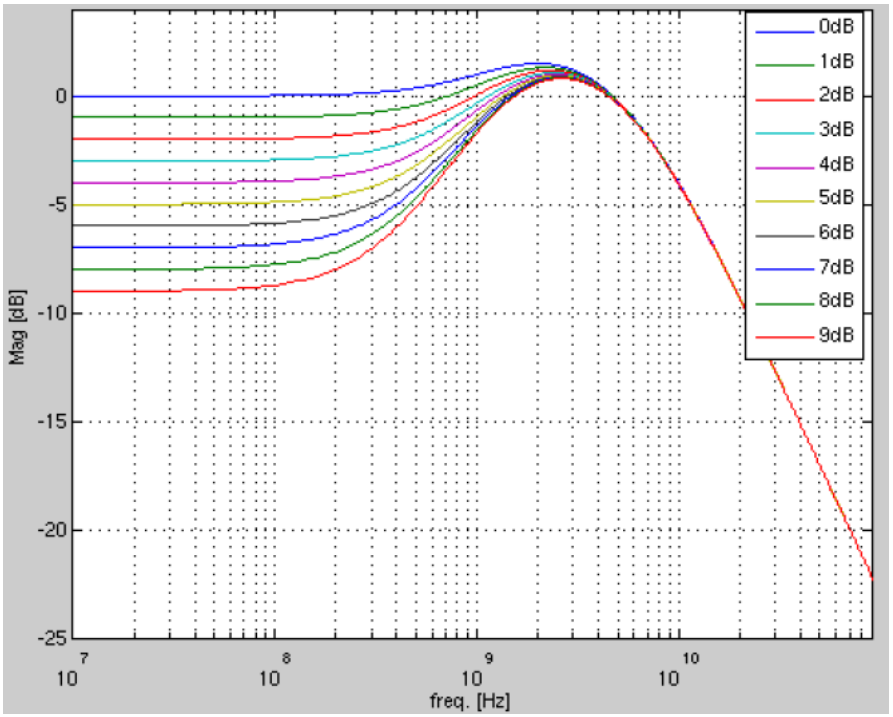


Figure 32 Thunderbolt 3 Reference CTLE for Gen2 devices

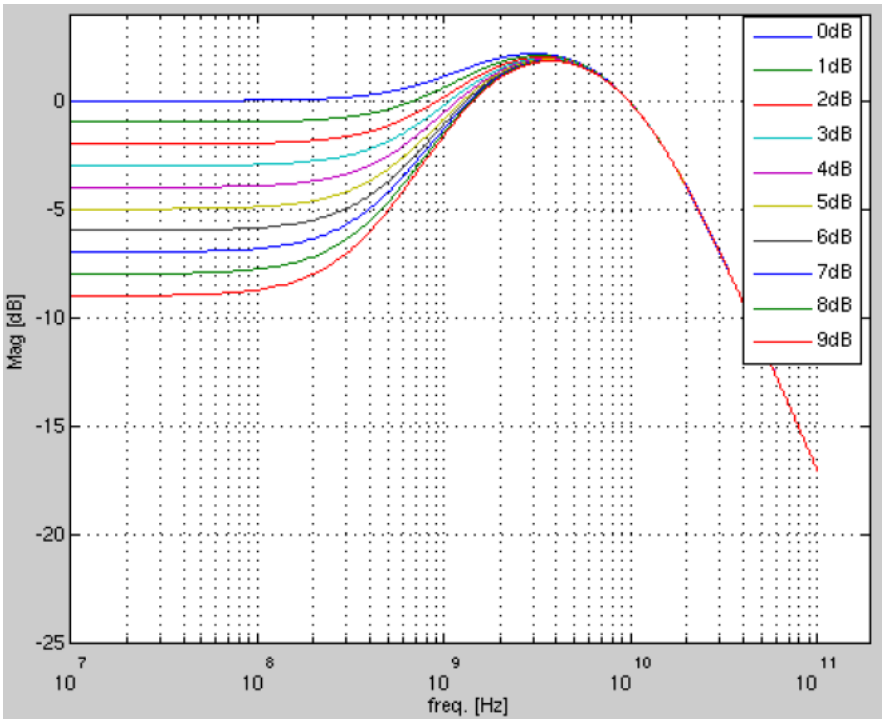


Figure 33 Thunderbolt 3 Reference CTLE for Gen3 devices

Reference DFE

A 1-tap reference feedback filter is defined as part of the reference receiver equalizer used in the compliance testing. The DFE formula is described in the equation, shown in Figure 34.

$$y_n = x_n - c_1 \cdot sign(y_{n-1})$$

Where:

y_n *is the DFE output at time instant* n

x_n *is the DFE input (incoming signal after applying the CTLE)*

c_1 *is the DFE coefficient, which may get values between* 0 *to* 50mV.

Figure 34 3rd Generation Thunderbolt Decision-Feedback-Equalizer (DFE) Formula

Figure 35 shows the flowchart representation of the Reference Receiver Equalization.

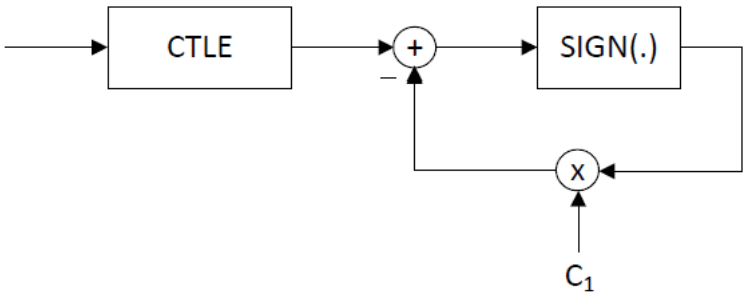


Figure 35 3rd Generation Thunderbolt Reference Receiver Equalization

Requirements for Host / Device Transmitter Compliance

The 3rd Generation Thunderbolt Host/Device transmitter compliance test is defined at the output of a “golden” plug fixture (Thunderbolt3-P) at point TP1 and at the output of a “golden” receptacle fixture (Thunderbolt3-R) at point TP3EQ. For more information about the reference test boards Thunderbolt3-P and Thunderbolt3-R, refer to Section 5.6.4 and Section 5.7.4 of *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9 specification*.

The Host/Device Transmitter shall transmit a PRBS31 pattern during the compliance testing, except when testing specific parameters that require dedicated patterns that are explicitly defined in the specific context. The test shall be performed while the Spread-Spectrum-Clocking (SSC) is enabled, and while the neighbor interfaces are active.

Host / Device Transmitter Specifications for both Gen2 and Gen3 devices (all bit-rates)

Table 4 defines parameters for the 3rd Generation Thunderbolt Host/Device Transmitters, which apply for both Gen2 and Gen3 devices.

Table 4 Common Host / Device Transmitter Specifications at TP1

Symbol	Description	Min	Max	Units	Comments
TX_EQ	Transmitter Equalization	See “Transmit Equalization” on page 65	–	–	–
SSC_DOWN_SPREAD_RANGE	SSC down-spreading deviation	0.4	0.5	%	–
SSC_DOWN_SPREAD_RATE	SSC down-spreading modulation rate	SSC_DSR_MIN	SSC_DSR_MAX	KHz	See Note 0
SSC_PHASE_DEVIATION	Phase jitter associated with the SSC modulation	2.5	SSC_PD_MAX	ns pp	See Note 0 and Note 1
SSC_SLEW_RATE	SSC df/dt during data mode	–	1000	ppm/µs	See Note 2
LANE_TO_LANE_SKEW	Skew between dual transmit signals	–	26	ns	–
RISE_FALL_TIME	TX Rise/Fall time measured between 20-80% levels	10	–	ps	Test Pattern shall be alternating square pattern of sixteen 0’s and sixteen 1’s

Note:

0. Refer to Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

1. The SSC phase deviation shall be extracted from the transmitted signal. During this test, the transmitter shall be configured to send PRBS31 pattern. The SSC phase deviation is the signal phase jitter after applying a 2nd order low-pass filter with 3dB point at 2MHz.

2. The SSC slew rate shall be extracted from the transmitted signal over measurement intervals of 0.5us. The SSC slew-rate shall be extracted from the phase information after applying a 2nd order low-pass filter with 3dB point at 2MHz.SSC_SLEW_RATE_DATA is the SSC frequency deviation over time while valid data is being transmitted in which 1E-12 bit error rate is required without assuming forward error correction.

Transmit Equalization

The 3rd Generation Thunderbolt Host/Device implements coefficient based equalization at its transmitter. The transmit equalization should support 16 specified preset covering different de-emphasis and pre-shoot configurations. The equalizer's structure is based on UI-spaced 3 tap finite-impulse-response (FIR) filter as shown in Figure 37. The transmitted level corresponding to the nth symbol is calculated using the equation shown in Figure 36:

$$tx\_out_n = \sum_{k=-1}^{1} data\_in_{n-k} \cdot C_k$$

where:

tx_out_n is the transmitted level at time instant n

$data\_in_{n-k}$ is the data symbol at time instant n-k

C_k is the k^{th} coefficient of the FIR filter

Figure 36 Transmit Equalization equation for transmitted levels corresponding to the nth symbol

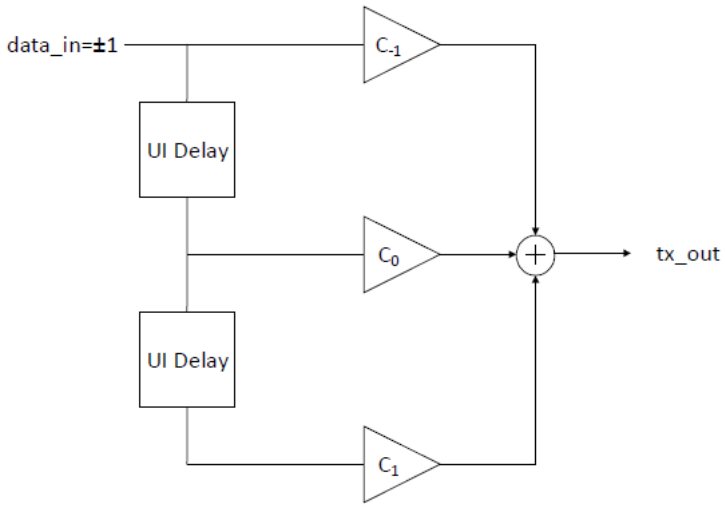


Figure 37 Transmitter Equalizer Structure

Table 5 indicates the normative Pre-shoot and De-emphasis requirements of the transmitter equalization presets and the corresponding informative coefficients values.

Preset configurations 0 to 14 represent operation mode with full-swing transmitter output while configuration 15 represents the low-swing mode. When you select configuration 15, the transmitter's output swing should be attenuated by 3.5±1dB compared to its full-swing operation. The required tolerance of the Pre-shoot and De-emphasis is ±1dB.

Table 5 Transmit Equalization Presets

Preset Number	Pre-Shoot [dB]	De-Emphasis
0	0	0
1	0	-1.9
2	0	-3.6
3	0	-5.0
4	0	-8.4
5	0.9	0
6	1.1	-1.9
7	1.4	-3.8
8	1.7	-5.8
9	2.1	-8.0
10	1.7	0
11	2.2	-2.2
12	2.5	-3.6
13	3.4	-6.7
14	4.3	-9.3
15	1.7	-1.7

Note:

1. Pre-Shoot and De-Emphasis are calculated using the equations shown in Figure 38:

$$Preshoot = 20 \cdot log_{10}\left(\frac{-C_{-1} + C_0 + C_1}{C_{-1} + C_0 + C_1}\right)$$

$$De - emphasis = 20 \cdot log_{10}\left(\frac{C_{-1} + C_0 + C_1}{C_{-1} + C_0 - C_1}\right)$$

Figure 38 Equations to calculate Pre-Shoot and De-Emphasis

Figure 39 depicts the corresponding frequency responses of the different transmit equalization presets for Gen2 systems:

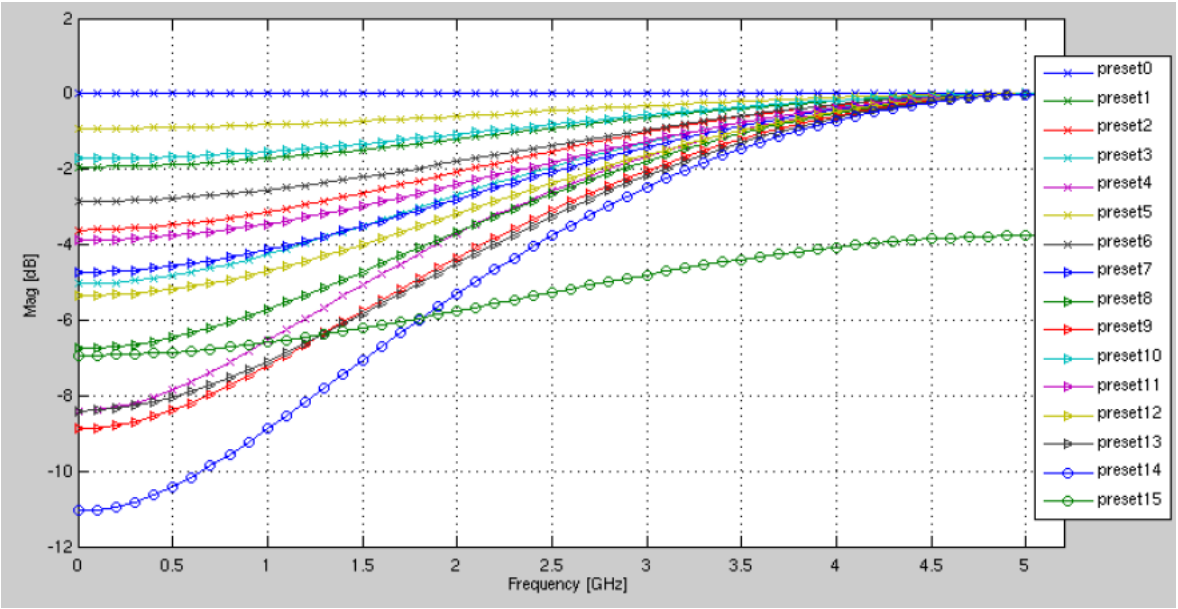


Figure 39 Transmitter Equalizer Frequency Response for Gen2 systems

Figure 40 depicts the corresponding frequency responses of the different transmit equalization presets for Gen3 systems:

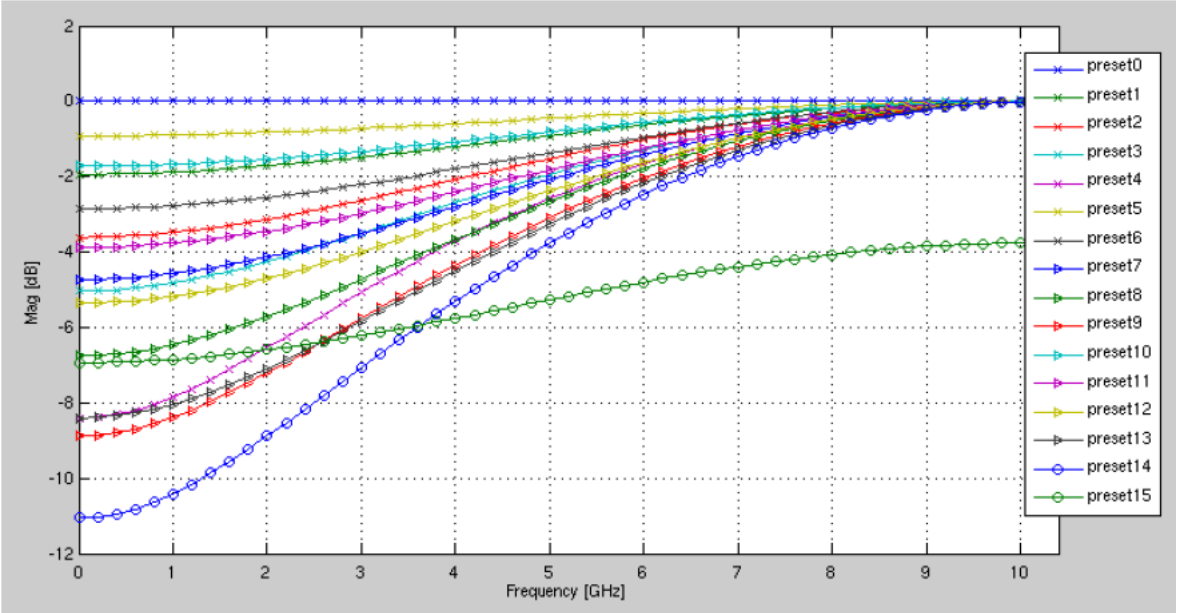


Figure 40 Transmitter Equalizer Frequency Response for Gen3 systems

Host / Device Transmitter Compliance Specifications for Gen2 Connections

Table 6 and Table 7 define the required specifications for Gen2 Host/Device transmitter. These tables describe specification limits, which are in addition to Table 4, which covers specification limits common to both Gen2 and Gen3 devices. Table 7 should be measured after applying the reference receiver equalization function defined in "Reference Equalization Function" on page 61.

Table 6 Gen2 Host / Device Transmitter Specifications at TP1

Symbol	Description	Min	Max	Units	Comments
UI	Unit Interval	G2_UI_MIN	G2_UI_MAX	ps	Frequency high limit = 0 ppm Frequency low limit = -5000 ppm See Notes 0, 4
UI_MEAN	Average Unit Interval	G2_UI_MEAN_MIN	G2_UI_MEAN_MAX	ps	See Notes 0, 5
AC_CM	TX AC Common Mode Voltage	–	100	mV pp	See Note 2
TJ	Total Jitter	–	0.38	UI pp	See Notes 2, 3
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	–	0.31	UI pp	See Notes 2, 3
UDJ	Deterministic Jitter that is uncorrelated to the transmitted data	–	0.17	UI pp	–
UDJ_LF	Low Frequency Uncorrelated Deterministic Jitter	–	0.04	UI pp	See Note 8
DUT_CYCLE_DISTORTION	DJ associated by DCD Jitter	–	0.03	UIp-p	–
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	180	–	mV	Measured for 1E6 UI. See Notes 1, 2 and Figure 41
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	–	700	mV	Measured for 1E6 UI. See Notes 1, 2 and Figure 41

Note:

0. Refer to Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.
1. TX voltage is differential.
2. Measured while applying the reference CDR described in "Jitter and Eye Measurement Methodology" on page 60.
3. TJ is defined as the sum of all "deterministic" components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top).
4. UI shall be calculated dynamically using a uniform moving average filter with window size of 3000 symbols.
5. The average UI shall be measured over windows at the size of one SSC cycle.
6. The test shall be performed while the SSC is enabled, and while all other interfaces are active with uncorrelated data.
7. The transmit equalization preset shall be set such that the eye opening is optimized at TP1.
8. UDJ_LF is the uncorrelated deterministic jitter measured after applying 2nd order Low-Pass-Filter with 3dB cut-off at 2MHz on the measured jitter. This filter needs to be applied on top of the reference CDR rejection function.

Table 7 Gen2 Host / Device Transmitter Specifications at TP3EQ

Symbol	Description	Min	Max	Units	Comments
TJ	Total Jitter	–	0.60	UI pp	See Notes 2, 3
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	–	0.31	UI pp	See Notes 2, 3
UDJ	Uncorrelated Deterministic Jitter	–	0.17	UI pp	–
X1	TX eye horizontal opening	–	0.22	UI	Measured for 1E6 UI. See Notes 2, 5 and Figure 41
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	52	–	mV	Measured for 1E6 UI. See Notes 1, 2 and Figure 41
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	–	1000	mV	Measured for 1e-6 UI. See Notes 1, 2 and Figure 41

Note:

1. TX voltage is differential.
2. Measured while applying the reference CDR described in “Jitter and Eye Measurement Methodology” on page 60 and the reference equalizer defined in “Reference Equalization Function” on page 61.
3. TJ is defined as the sum of all “deterministic” components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top).
4. The test shall be performed while the SSC is enabled, and while all other interfaces are active with uncorrelated data.
5. X1 specification is informative but should be assumed as a valid reference if direct TJ measurement cannot be done at TP3EQ reliably due to equipment limitations.

Figure 41 shows the Host / Device Transmitter Eye Mask Notations, defined in the tables above.

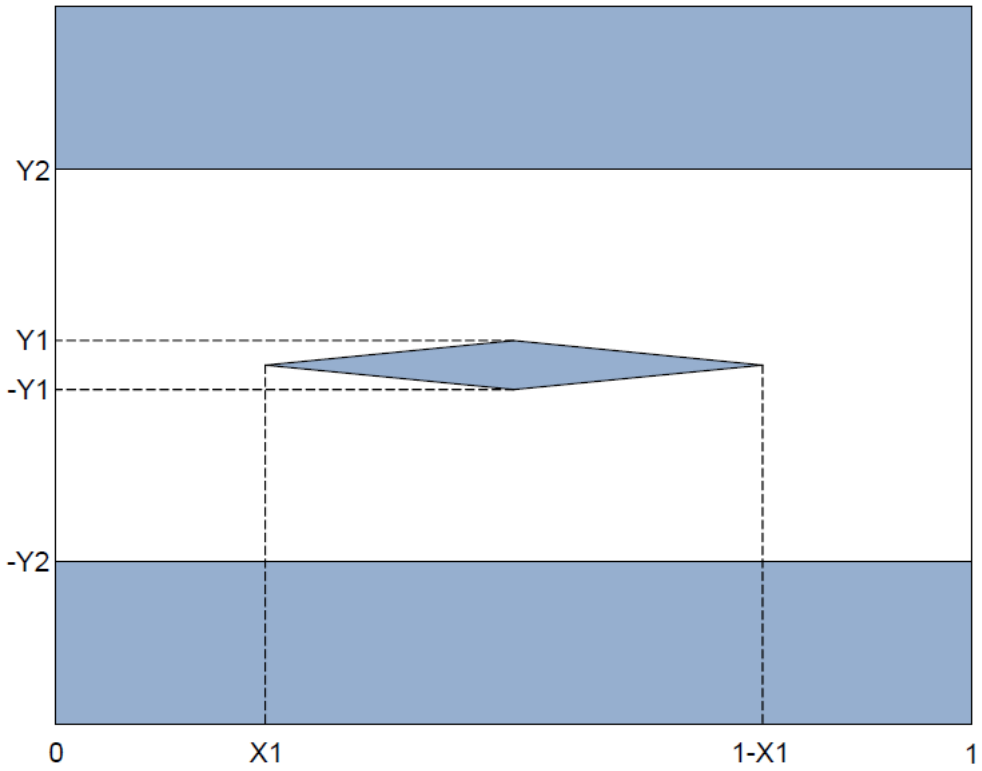


Figure 41 Host / Device TX Mask Notations

Host / Device Transmitter Compliance Specifications for Gen3 Connections

Table 8 and Table 9 define the required specifications for Gen3 Host/Device transmitter. These tables describe specification limits, which are in addition to Table 4, which covers specification limits common to both Gen2 and Gen3 devices. Table 9 should be measured after applying the reference receiver equalization function defined in "Reference Equalization Function" on page 61.

Table 8 Gen3 Host / Device Transmitter Specifications at TP1

Symbol	Description	Min	Max	Units	Comments
UI	Unit Interval	G3_UI_MIN	G3_UI_MAX	ps	Frequency high limit = 0 ppm Frequency low limit = -5000 ppm See Notes 0, 4
UI_MEAN	Average Unit Interval	G3_UI_MEAN_MIN	G3_UI_MEAN_MAX	ps	See Notes 0, 5
AC_CM	TX AC Common Mode Voltage	–	100	mV pp	Maximum allowed ACCM voltage
TJ	Total Jitter	–	0.46	UI pp	See Notes 2, 3
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	–	0.31	UI pp	See Notes 2, 3
UDJ	Deterministic Jitter that is uncorrelated to the transmitted data	–	0.17	UI pp	–
UDJ_LF	Low Frequency Uncorrelated Deterministic Jitter	–	0.07	UI pp	See Note 8
DUT_CYCLE_DISTORTION	DJ associated by DCD Jitter	–	0.03	UIp-p	–
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	120	–	mV	Measured for 1E6 UI. See Notes 1, 2 and Figure 41
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	–	700	mV	Measured for 1E6 UI. See Notes 1, 2 and Figure 41

Note:

0. Refer to Table 5-8 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.
1. TX voltage is differential.
2. Measured while applying the reference CDR described in "Jitter and Eye Measurement Methodology" on page 60.
3. TJ is defined as the sum of all "deterministic" components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top).
4. UI shall be calculated dynamically using a uniform moving average filter with window size of 6000 symbols.
5. The average UI shall be measured over windows at the size of one SSC cycle.
6. The test shall be performed while the SSC is enabled, and while all other interfaces are active with uncorrelated data.
7. The transmit equalization preset shall be set such that the eye opening is optimized at TP1.
8. UDJ_LF is the uncorrelated deterministic jitter measured after applying 2nd order Low-Pass-Filter with 3dB cut-off at 2MHz on the measured jitter. This filter needs to be applied on top of the reference CDR rejection function.

Table 9 Gen3 Host / Device Transmitter Specifications at TP3EQ

Symbol	Description	Min	Max	Units	Comments
TJ	Total Jitter	–	0.60	UI pp	See Notes 2, 3
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	–	0.31	UI pp	See Notes 2, 3
UDJ	Uncorrelated Deterministic Jitter	–	0.17	UI pp	–
X1	TX eye horizontal opening	–	0.22	UI	Measured for 1E6 UI. See Notes 2, 5 and Figure 41
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	46	–	mV	Measured for 1E6 UI. See Notes 1, 2 and Figure 41
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	–	1000	mV	Measured for 1E6 UI. See Notes 1, 2 and Figure 41

Note:

1. TX voltage is differential.
2. Measured while applying the reference CDR described in “Jitter and Eye Measurement Methodology” on page 60 and the reference equalizer defined in “Reference Equalization Function” on page 61.
3. TJ is defined as the sum of all “deterministic” components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top).
4. The test shall be performed while the SSC is enabled, and while all other interfaces are active with uncorrelated data.
5. X1 specification is informative but should be assumed as a valid reference if direct TJ measurement cannot be done at TP3EQ reliably due to equipment limitations.

Table 10 displays the Parameter Limits for certain tests, as defined in *Table 5-24* of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Table 10 Parameter Limits for certain Thunderbolt 3 Transmitter Gen2 and Gen3 Tests

Parameter	Legacy values	Rounded values	Units
SSC_DSR_MIN	35	30	KHz
SSC_DSR_MAX	37	33	KHz
SSC_PD_MAX	18.5	22	ns
G2_UI_MIN	96.9697	100.0	ps
G2_UI_MAX	97.457	100.5025	ps
G2_UI_MEAN_MIN	97.1835	100.2205	ps
G2_UI_MEAN_MAX	97.2419	100.2808	ps
G3_UI_MIN	48.4848	50.0	ps
G3_UI_MAX	48.7285	50.2513	ps
G3_UI_MEAN_MIN	48.5918	50.1102	ps
G3_UI_MEAN_MAX	48.6210	50.1404	ps

Transmitter Test Setup

Figure 42 shows the typical connections to the DUT and the control PC (if any) used for Host / Device Transmitter testing for both Gen2 and Gen3 Systems. During the test runs, if required, the Thunderbolt 3 Test Application prompts for changes in connection setup.

NOTE **Before you begin any tests or data acquisition, ensure that the Oscilloscope is warmed, calibrated and the cables de-skewed. See** "Calibrating the Infiniium Oscilloscope" on page 159.

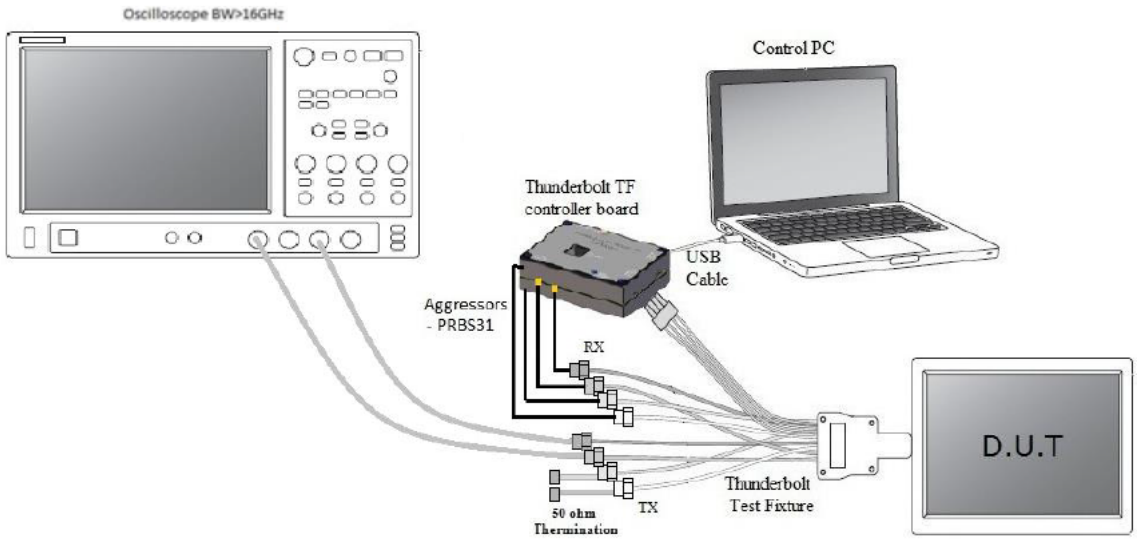


Figure 42 Thunderbolt 3 Host / Device Transmitter Common Test Setup

Connecting to the DUT

1. Connect the Lane under test TX_P, TX_N to the Oscilloscope.
2. Connect termination to the TX Lane, which is not under test.
3. Connect the RX Lanes to Thunderbolt Micro-Controller SMA Lanes, 800mV amplitude to inject crosstalk.

5 Transmitter Tests for 10.3125 GB/s Systems

This section provides the Methods of Implementation (MOIs) to run electrical tests on a Thunderbolt DUT operating at a bit rate of 10.3125 GB/s using an Keysight Infiniium Oscilloscope and other accessories, along with the Thunderbolt 3 Test Application.

NOTE All Thunderbolt 3 devices that support a bit rate of 10.3125 Gb/s are classified as Gen2 devices.

Tx Preset Calibration

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Preset Calibration Test is to find the optimized preset for the platform.

NOTE Prior to running the compliance tests, the Host / Device must go through Preset Calibration.

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Preset Calibration* are checked.

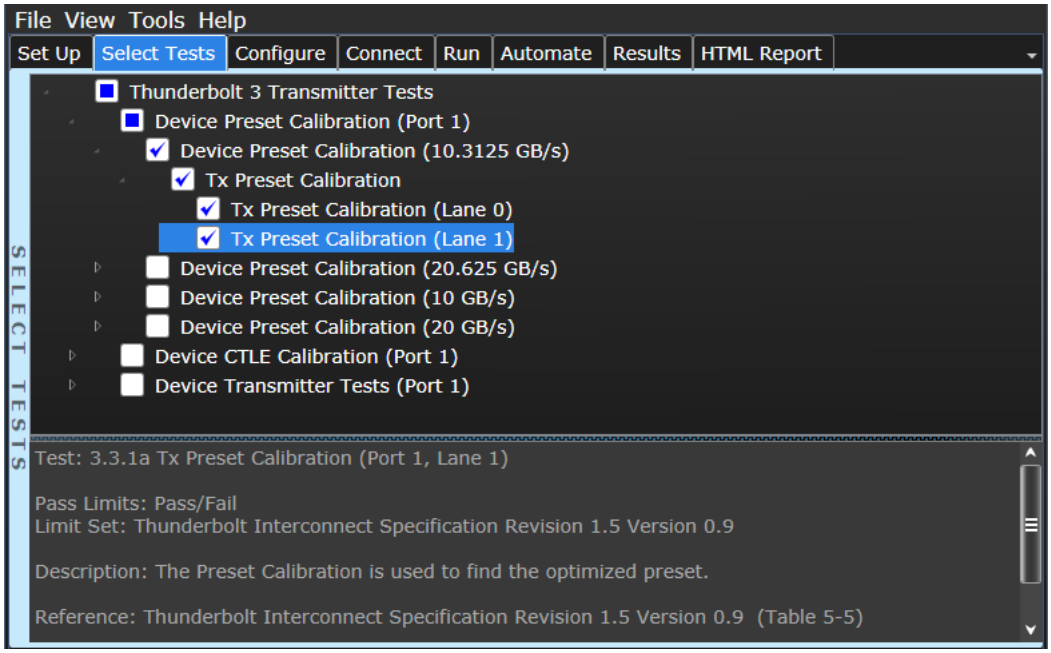


Figure 43 Selecting the Tx Preset Calibration tests

NOTE By default, the test group for **Preset Calibration** for each selected bit-rate is hidden in the **Select Tests** tab when **Predefined Optimum Preset Number** is selected for the respective bit-rates. To view and select the **Preset Calibration** tests in the **Select Tests** tab, select the **Run Preset Calibration** option in the **Test Setup** window of the **Set Up** tab.

Test Procedure

1 Connect the DUT to the Oscilloscope.
2 Configure the DUT transmitter to output PRBS31, preset 0 on all lanes with SSC enabled.
3 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used.
   b Oscilloscope with a minimum bandwidth of 16GHz.
4 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Adjust vertical and horizontal scales such that the signal fits within the Oscilloscope's display
   c Measured at 1E6 UI
5 Capture eye height and eye width for lane 0.
6 Register mean eye height and mean eye width values.
7 Repeat the test for all remaining Thunderbolt transmit presets (till preset 15 as shown in Table 5).
8 Repeat the test for the remaining Thunderbolt lanes.
9 For each lane, choose the preset that provides maximum eye width. If there are two presets with the same eye width, select the one with the greater eye height.

Expected / Observable Results

For each lane, the preset that provides the maximum eye width is the optimized preset for the platform. If two presets have the same eye width, the preset with a greater eye height is the optimized preset.

Test References

See

- "Section 3.3.1 Preset Calibration" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-5 of the *Thunderbolt™ Interconnect Specification Revision 1.5 Version 0.9.*

Tx CTLE Calibration

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx CTLE Calibration Test is to find the optimized CTLE (Continuous-Time-Linear-Equalizer) for the platform.

See "Reference CTLE" on page 61 to know more about CTLE.

NOTE Apply equalization on the Oscilloscope, when testing at TP3EQ.

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx CTLE Calibration* are checked.

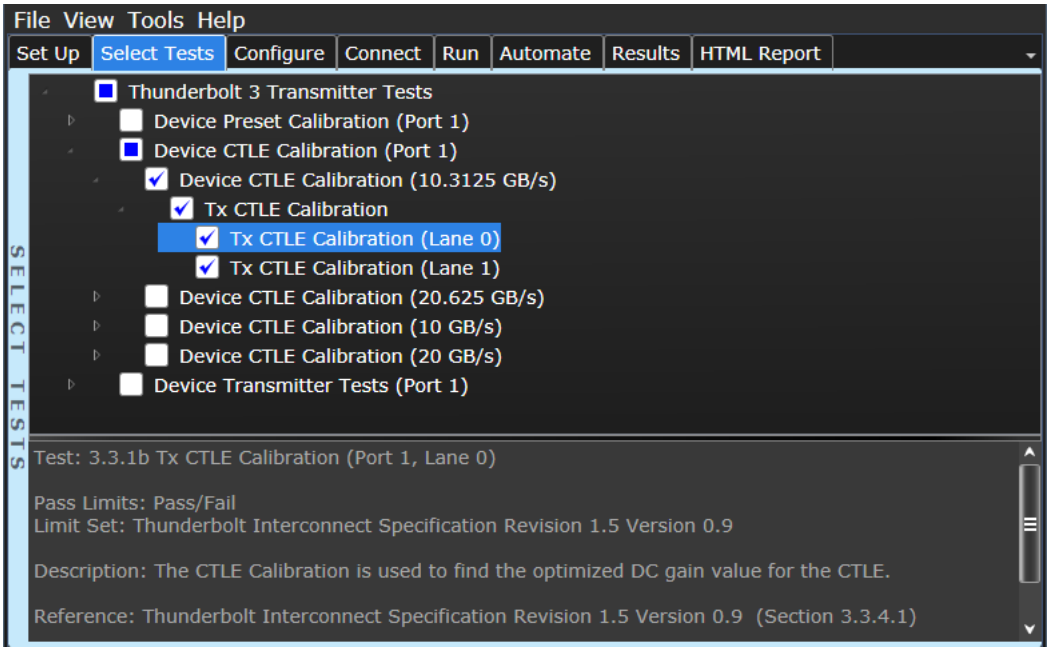


Figure 44 Selecting the Tx CTLE Calibration tests

NOTE By default, the test group for **CTLE Calibration** for each selected bit-rate is hidden in the **Select Tests** tab when **Predefined Optimum CTLE DC Gain Value** is selected for the respective bit-rates. To view and select the **CTLE Calibration** tests in the **Select Tests** tab, select the **Run CTLE Calibration** option in the **Test Setup** window of the **Set Up** tab.

Test Procedure

1 Follow the CTLE model as described in "Reference CTLE" on page 61, with the following parameters:

a AC Gain = 1.41

b Wp1 = 2 * π * 1.5G rad/sec

c Wp2 = 2 * π * 5G rad/sec

2 Apply ten different CTLE configurations such that A_{DC}, which is the DC Gain, is a value that lies within the following equation:

$$\{10^{-x/20} : x = 0 - 9\ [dB]\}$$

3 Calibrate A_{DC} using the following procedure:

a Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

b Select A_{DC} for x = 0.

c Perform measurement with reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.

d Capture the waveform and process it with the Digital Oscilloscope:

- Sampling Rate $\geq$ 80 GSa/s
- Adjust vertical & horizontal scale such that the signal fits within the Oscilloscope's display
- Measured at 1E6 UI

e Eye height should be positioned at the "0" of the real time eye horizontal position.

f Apply a Histogram to the lower and upper sections of the eye, with ±1% deviation in time axis in order to calculate the eye height. Eye height is the delta between the minimum value from the upper histogram result (see Figure 45) and the maximum value from the lower histogram result (see Figure 46).

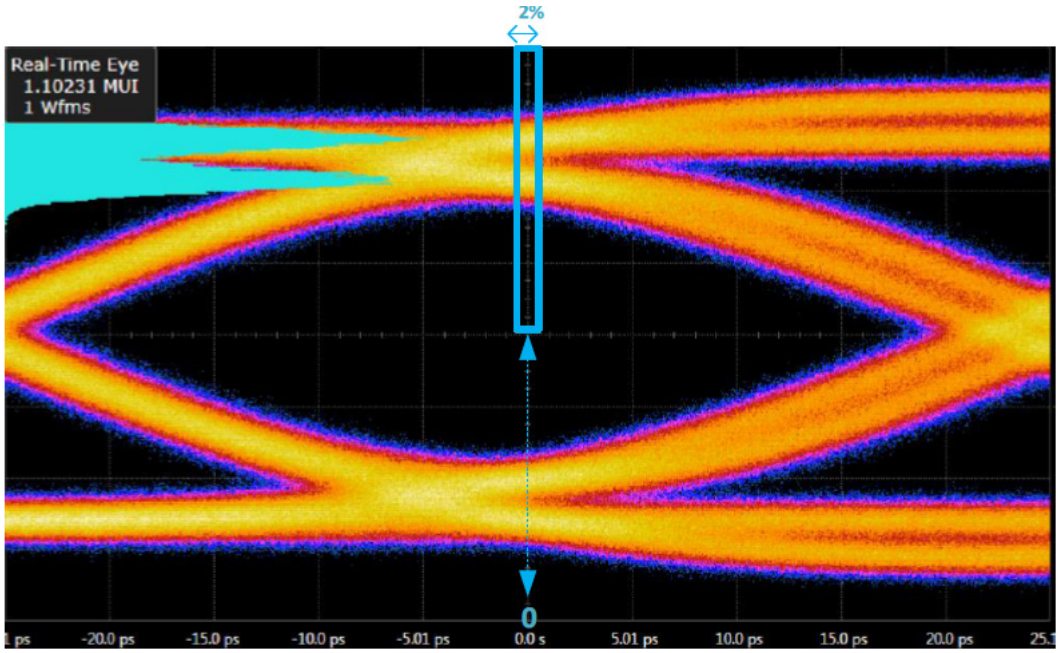


Figure 45 Thunderbolt RX TP3EQ Eye Height upper location measurement

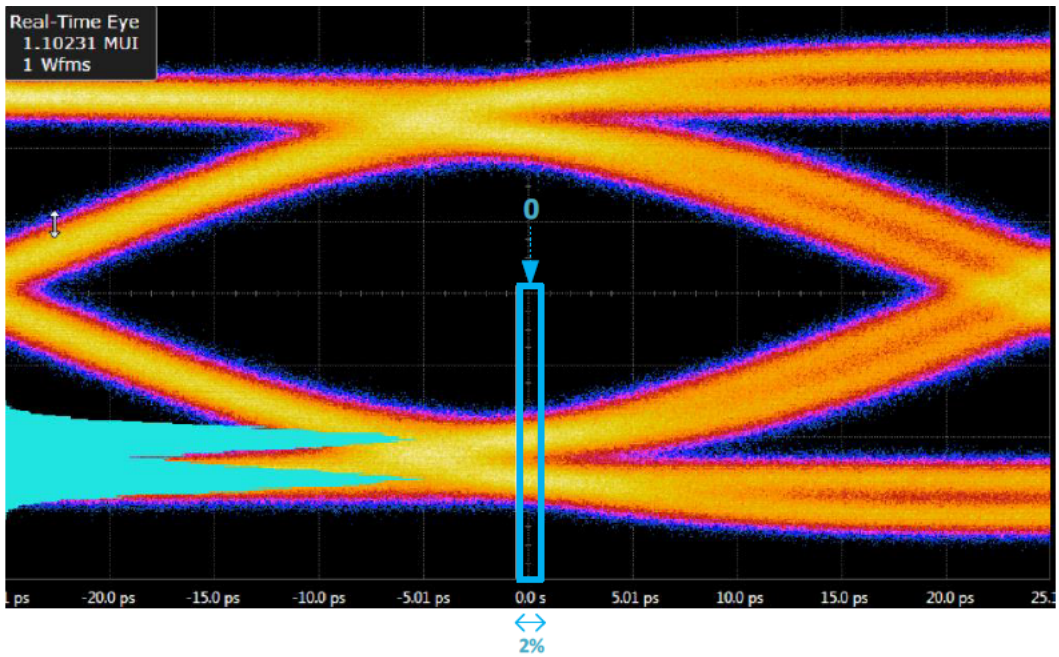


Figure 46 Thunderbolt RX TP3EQ Eye Height lower location measurement

g Capture five times (each time over new 1MUI record length) the minimum value of both eye height and eye width.

h Average the five captured values, that is, average of (5 times minimum eye height) and average of (5 times minimum eye width).

i Repeat this procedure from step 3b to 3i with x = x + 1 upto x = 9.

j Measure that value of A_{DC} (including DFE tap value), which yields the maximum eye height. If there are two values of A_{DC} (including DFE tap value), which have the same eye height, select the one that has the greater eye width.

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

For each lane, the DC Gain value that provides the maximum eye height is the optimized CTLE for the platform. If two DC Gain values have the same eye height, the one with a greater eye width is the optimized CTLE.

Test References

See

- "Section 8.1 Appendix C – Equalization Calibration" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9.*
- Section 3.3.4.1 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Rise/Fall Time

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Rise/Fall Time Test is to confirm that the rise times and fall times on the Thunderbolt differential signals are within the limits of the specification.

Test Pass Requirement

Rise Time and Fall Time ≥ 10ps (Refer to Table 4 on page 64).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Rise/Fall Time* are checked.

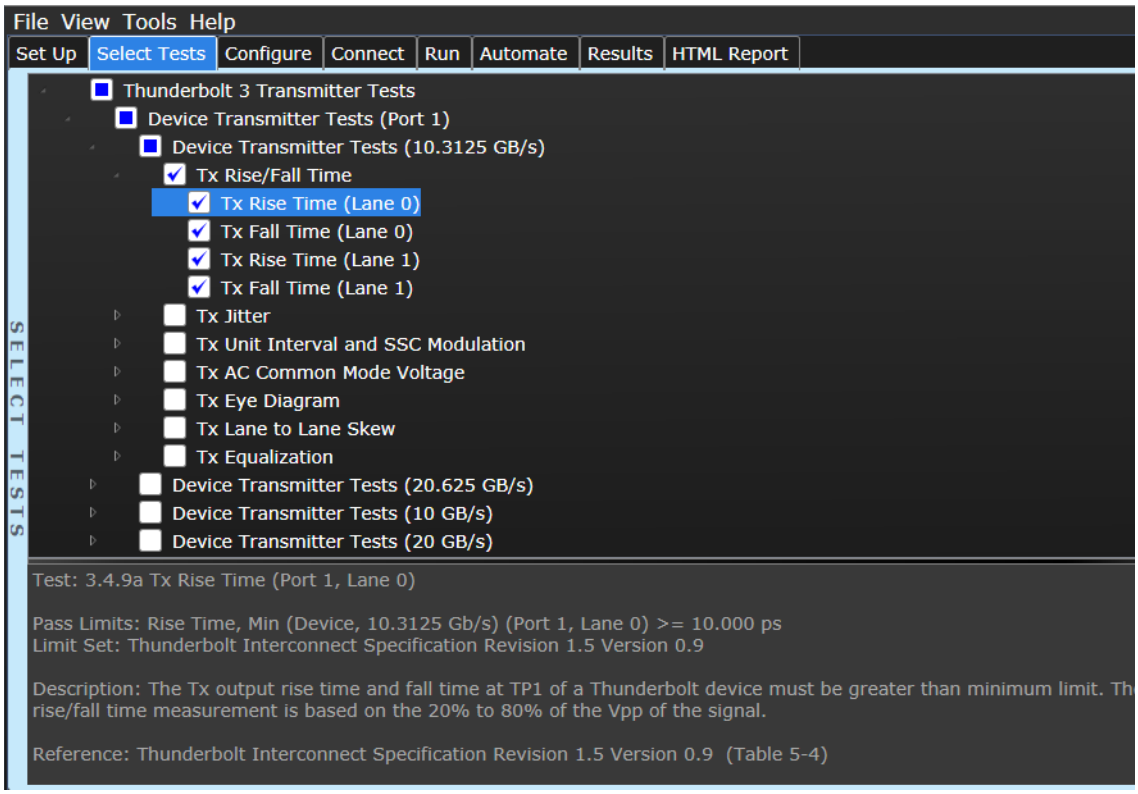


Figure 47 Selecting the Tx Rise/Fall Time tests

Test Procedure

1 Configure the DUT transmitter to output alternating square pattern of 16 0's and 16 1's on all lanes with SSC enabled.

2 Evaluate at least 4Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 4Mpts. Use the maximum analog bandwidth of the Oscilloscope.

No CDR, no average and no interpolation to be used.

Adjust vertical scale such that the signal fits within the Oscilloscope's display.

3 Measure T_{RISE} as the mode of the sampled edge times from 20% to 80% of the differential swing voltage rising edge.

4 Measure T_{FALL} as the mode of the sampled edge times from 80% to 20% of the differential swing voltage falling edge.

5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If T_{RISE} < 10ps, the status of test is FAIL.

If T_{FALL} < 10ps, the status of test is FAIL.

Test References

See

- "Section 3.4.9 Gen2 Rise/Fall Time Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-4 of the *Thunderbolt™ Interconnect Specification Revision 1.5 Version 0.9*.

Tx Total Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Total Jitter Test is to confirm that the Total Jitter of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of 1E-13.

Test Pass Requirement

Total Jitter (TJ) $\leq$ 0.38 UI_{p-p} (Refer to Table 6 on page 68).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Total Jitter* are checked.

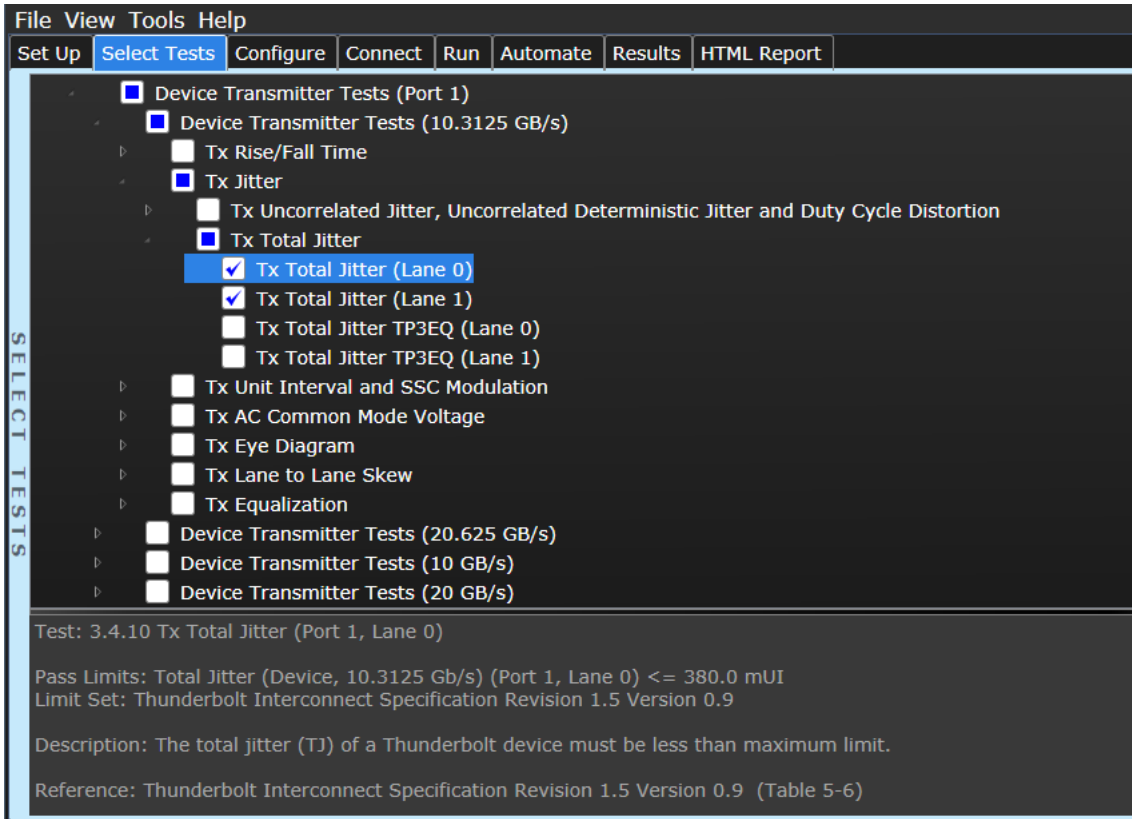


Figure 48 Selecting the Tx Total Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   b Oscilloscope with a minimum bandwidth of 16GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display.
   f Referenced to 1E-13 statistics.
4 Capture the values of Total Jitter (TJ) and Deterministic Jitter (DJ).
5 If TJ > 0.38 UI_{p-p}, perform the following steps:
   a Configure the DUT transmitter to output alternating square pattern of one 0's and one 1's on all lanes with SSC enabled. (The pattern is SQ2 instead of PRBS15).
   b Perform measurements with:

- Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
- Oscilloscope with a minimum bandwidth of 16GHz

c Capture the waveform and process it with the Digital Oscilloscope:

- Sampling Rate $\geq$ 80 GSa/s
- Pattern length – Periodic
- Jitter Separation method must be suitable for cross-talk on the signal
- Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
- Adjust vertical scale such that the signal fits within the Oscilloscope's display.
- Referenced to 1E-13 statistics.

d Capture the Random Jitter (RJ) result.

e Calculate TJ using the equation:

TJ = DJ + 14.7 * RJ (DJ from #4; PRBS15 and RJ from #5d; SQ2)

6 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If TJ > 0.38 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.4.10 Gen2 Total Jitter" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Uncorrelated Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Jitter Test is to confirm that the Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Jitter (UJ) $\leq$ 0.31 UI_{p-p} (Refer to Table 6 on page 68).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

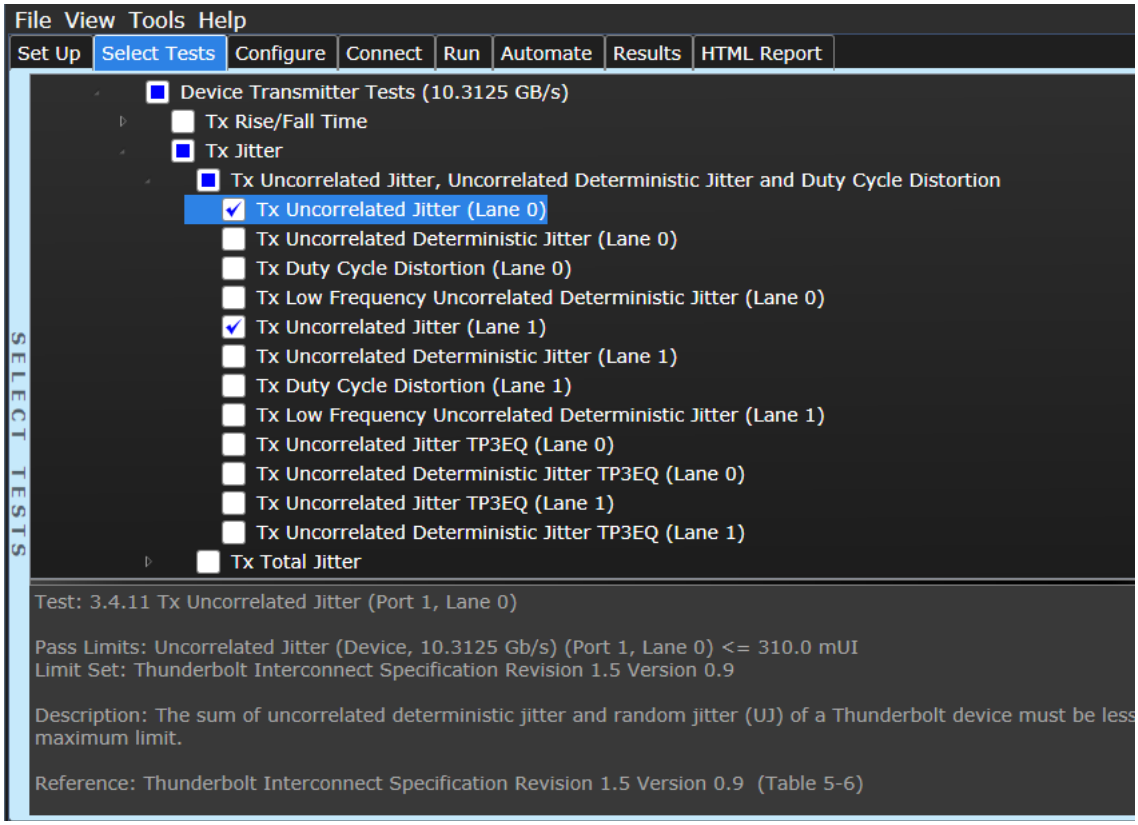


Figure 49 Selecting the Tx Uncorrelated Jitter tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Perform measurements with:
   - *a* Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   - *b* Oscilloscope with a minimum bandwidth of 16GHz
3. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Pattern length – Periodic
   - *c* Jitter Separation method must be suitable for cross-talk on the signal
   - *d* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *e* Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   - *f* Referenced to 1E-13 statistics
4. Capture the Total Jitter (TJ) and Data Dependent Jitter (DDJ) results.
5. Calculate UJ using the equation:

$$UJ = TJ - DDJ$$

6. Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UJ > 0.31 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.4.11 Gen2 UJ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Uncorrelated Deterministic Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Deterministic Jitter Test is to confirm that the Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Deterministic Jitter that is uncorrelated to the transmitted data (UDJ) $\leq$ 0.17 UI_{p-p} (Refer to Table 6 on page 68).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

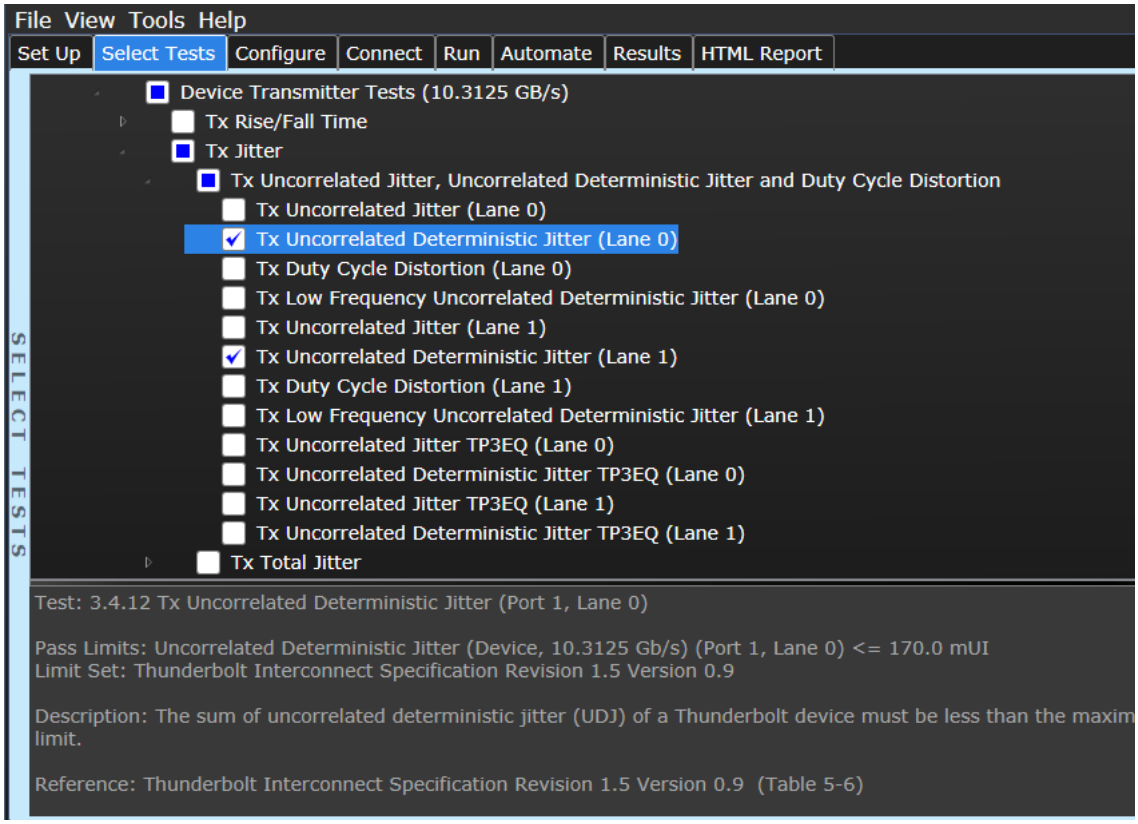


Figure 50 Selecting the Tx Uncorrelated Deterministic Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 16GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   f Referenced to 1E-13 statistics
4 Capture the UDJ result (same as BUJ over the Oscilloscope).
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UDJ > 0.17 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.4.12 Gen2 UDJ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Low Frequency Uncorrelated Deterministic Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Low Frequency Uncorrelated Deterministic Jitter Test is to confirm that the Low Frequency Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Low Frequency Uncorrelated Deterministic Jitter (UDJ_LF) $\leq$ 0.04 UI_{p-p} (Refer to Table 6 on page 68).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

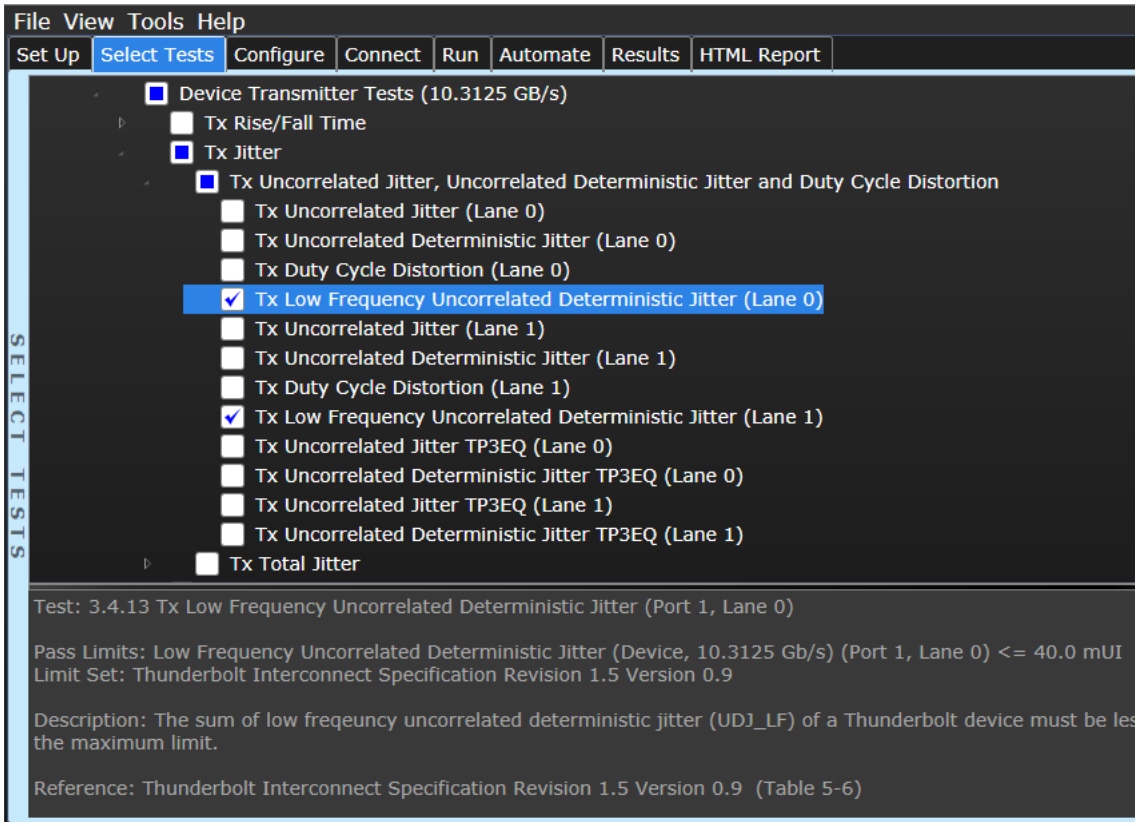


Figure 51 Selecting the Tx Low Frequency Uncorrelated Deterministic Jitter tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Perform measurements with:
   - *a* Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   - *b* Apply 2nd order Low-Pass-Filter with 3 dB cut-off at 2MHz; no average and no interpolation to be used
   - *c* Oscilloscope with a minimum bandwidth of 16GHz
3. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Pattern length – Periodic
   - *c* Jitter Separation method must be suitable for cross-talk on the signal
   - *d* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *e* Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
4. Capture the UDJ_LF result.
5. Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UDJ_LF > 0.04 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.4.13 Gen2 Low Frequency UDJ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Duty Cycle Distortion

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Duty Cycle Distortion Test is to confirm that the transmitter Deterministic Jitter Associated by Duty-Cycle-Distortion Jitter falls within the limits of the specification.

Test Pass Requirement

Duty-Cycle-Distortion (DCD) ≤ 0.03UIp-p (Refer to Table 6 on page 68).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

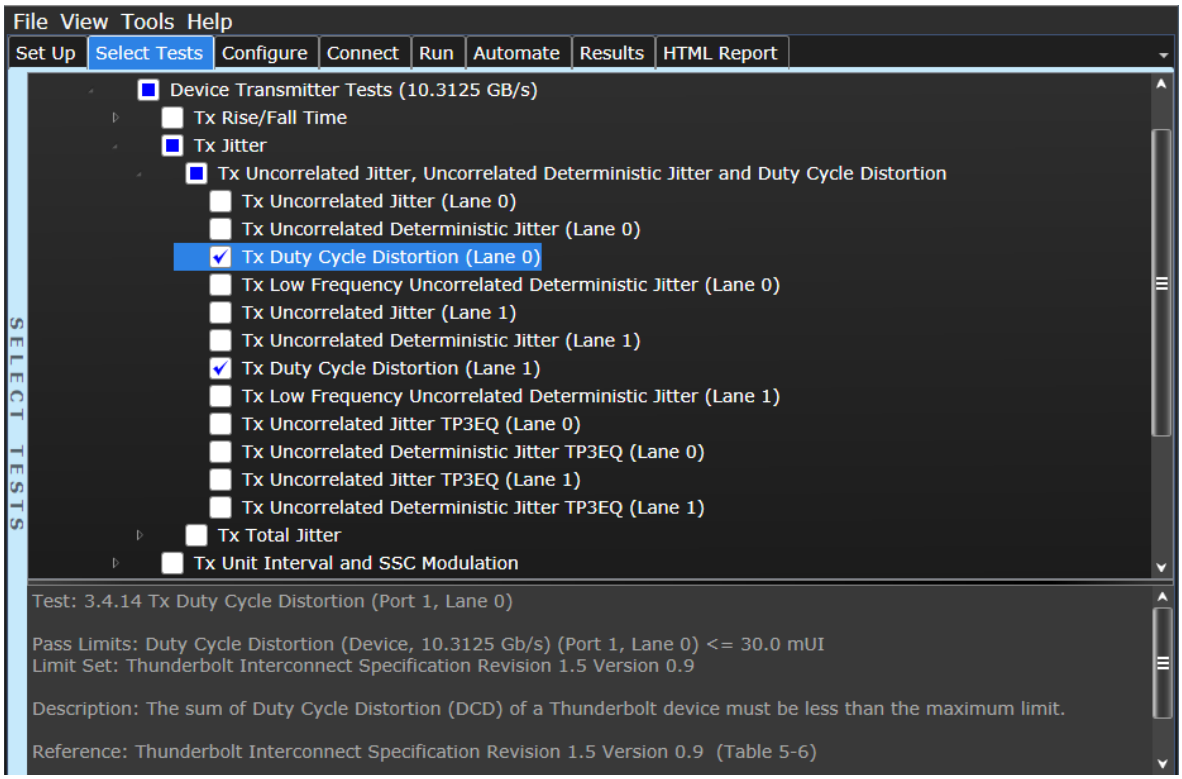


Figure 52 Selecting the Tx Duty Cycle Distortion tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 16GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts.
4 Capture the DCD result.
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If DCD > 0.03UIp-p, the status of test is FAIL.

Test References

See

- "Section 3.4.14 Gen2 DCD Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Unit Interval

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Unit Interval Test is to confirm that the data rate, under all conditions, does not exceed the minimum or maximum limits of the specification.

Test Pass Requirement

G2_UI_MIN ≤ Unit Interval ≤ G2_UI_MAX (Refer to Table 6 on page 68 and Table 10 on page 72).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

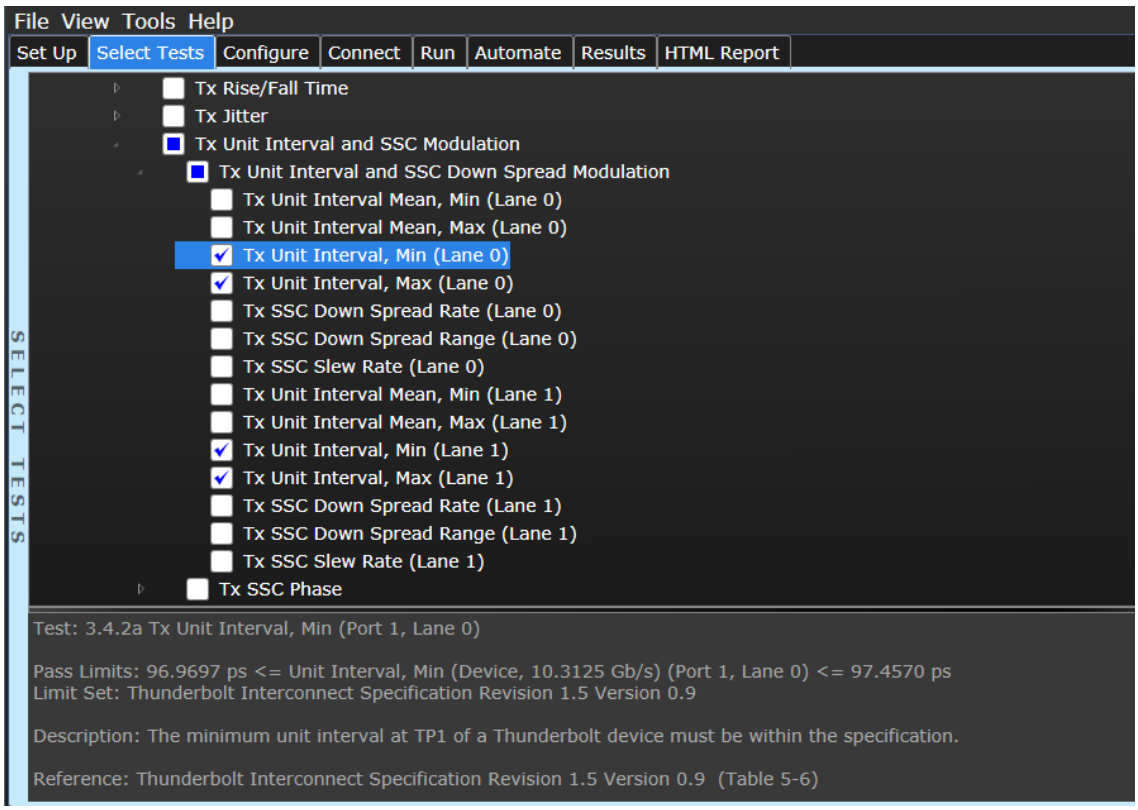


Figure 53 Selecting the Tx Unit Interval tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 16GHz
3 Calculate UI dynamically using a uniform moving average filter procedure with a window size of 3000 symbols.
4 Measure the values of both UI_{MAX} and UI_{MIN}.
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UI_{MAX} > G2_UI_MAX, the status of test is FAIL.

If UI_{MIN} < G2_UI_MIN, the status of test is FAIL.

Test References

See

- "Section 3.4.2 Gen2 Unit Interval Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Unit Interval Mean

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Unit Interval Mean Test is to confirm that the average data rate, under all conditions, does not exceed the minimum or maximum limits of the specification.

Test Pass Requirement

G2_UI_MEAN_MIN ≤ Average Unit Interval ≤ G2_UI_MEAN_MAX (Refer to Table 6 on page 68 and Table 10 on page 72).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

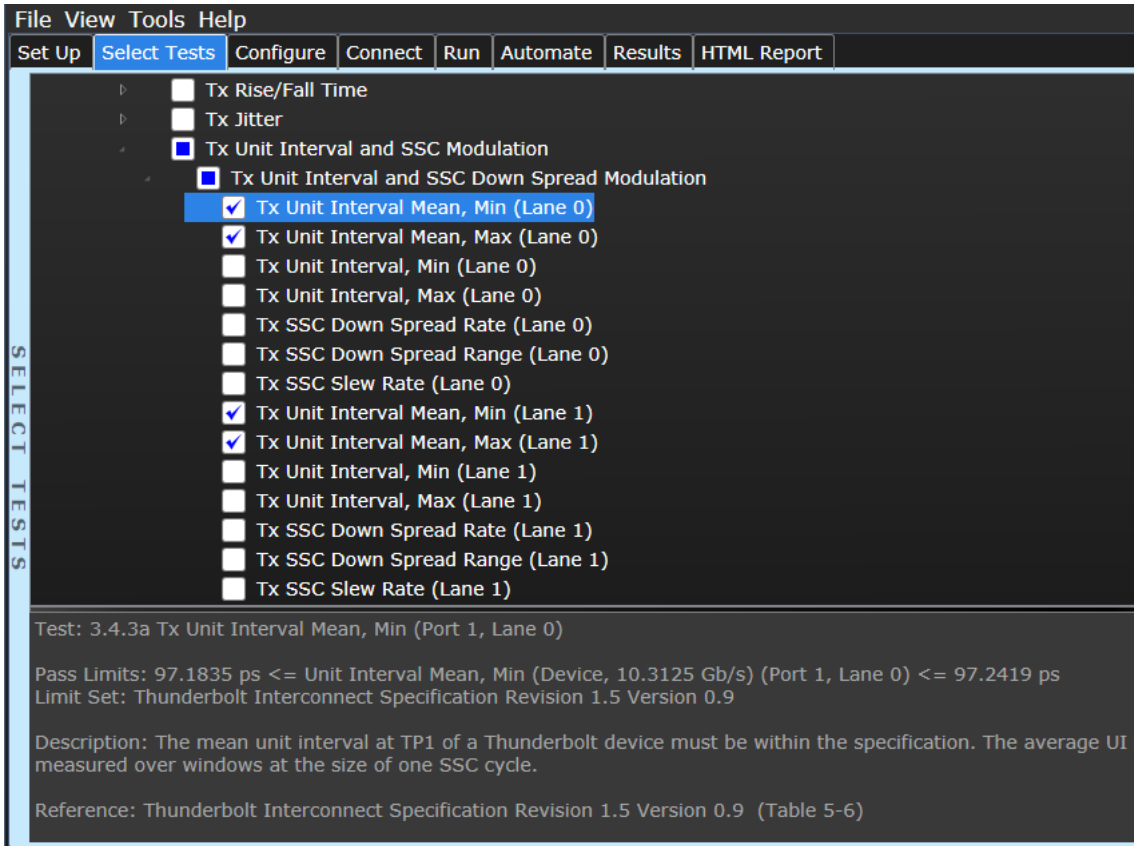


Figure 54 Selecting the Tx Unit Interval Mean tests

Test Procedure

1. Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   - *c* No CDR, no average and no interpolation to be used
   - *d* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *e* Oscilloscope must have a minimum bandwidth of 16GHz
3. Use mathematical analysis to measure the average unit interval over a window of the size of one SSC cycle, determined by the SSC_Down_Spread_Rate.
4. Measure UI_MEAN over different windows that uniformly cover the Oscilloscope capture for at least 300ms (more than 10 SSC Cycles) with 10000 UI window jumps. See Figure 55.

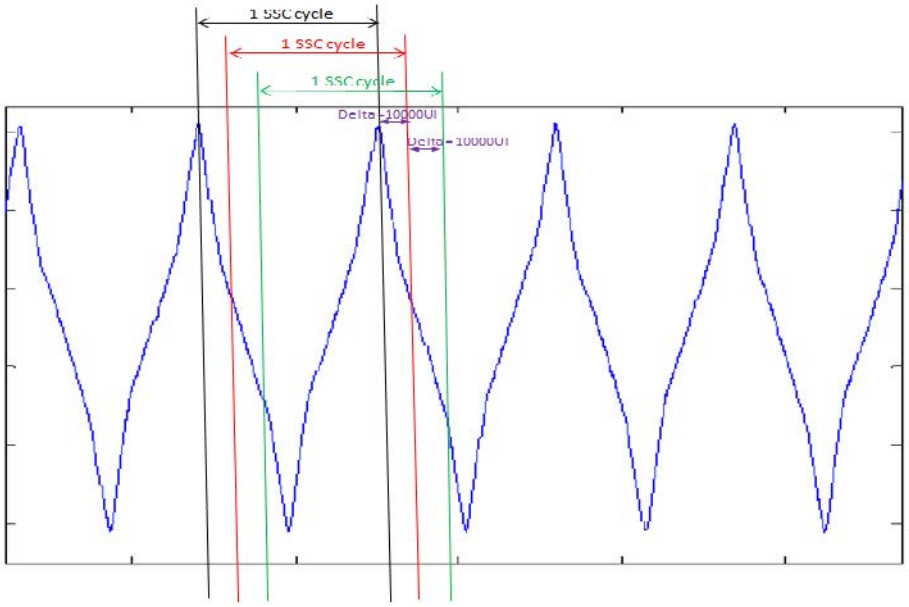


Figure 55 Measurement of UI_MEAN over at least 10 SSC Cycles

5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If the maximum UI_MEAN measured > G2_UI_MEAN_MAX, the status of test is FAIL.

If the minimum UI_MEAN measured < G2_UI_MEAN_MIN, the status of test is FAIL.

Test References

See

- "Section 3.4.3 Gen2 Unit Interval Mean Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9.*
- Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx SSC Down Spread Range

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Down Spread Range Test is to confirm that the data down spreading is within the limits of the specification.

Test Pass Requirement

0.4% ≤ SSC_Down_Spread_Range ≤ 0.5% (Refer to Table 4 on page 64).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

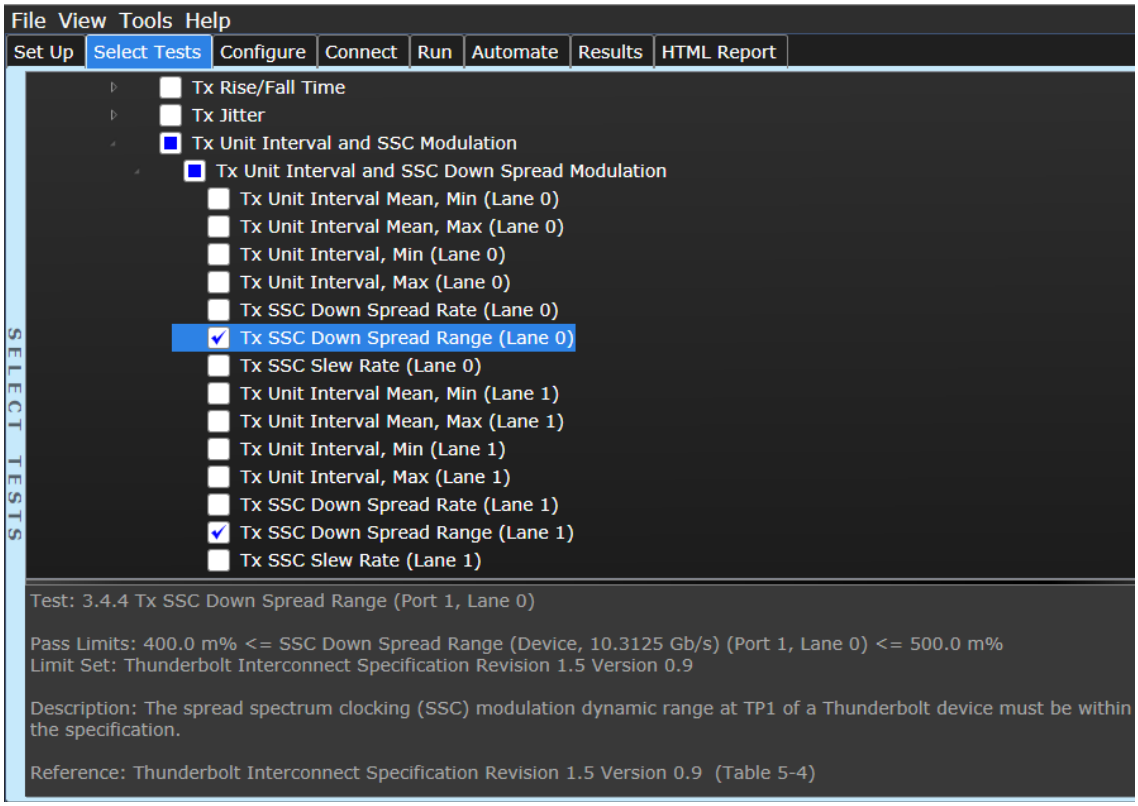


Figure 56 Selecting the Tx SSC Down Spread Range tests

Test Procedure

1. Run the "Tx Unit Interval" Test as a prerequisite to obtain UI_{MAX} and UI_{MIN}.
2. Use the obtained value of UI_{MAX} and UI_{MIN} to calculate the Range percentage:

$$\text{Maximum Deviation} = 100*\{[10.3125G - (1 / UI_{MAX})] / 10.3125G\}$$

$$\text{Minimum Deviation} = 100*\{[10.3125G - (1 / UI_{MIN})] / 10.3125G\}$$

3. Calculate SSC Down Spread Range using the equation:

$$\text{Maximum Deviation - Minimum Deviation}$$

4. Repeat the test for all remaining Thunderbolt lanes.

Expected / Observable Results

If SSC_Down_Spread_Range > 0.5% or SSC_Down_Spread_Range < 0.4%, the status of test is FAIL.

Test References

See

- "Section 3.4.4 Gen2 SSC Down Spread Deviation Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx SSC Down Spread Rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Down Spread Rate Test is to confirm that the Link clock down-spreading modulation rate is within the limits of the specification.

Test Pass Requirement

SSC_DSR_MIN ≤ SSC_Down_Spread_Rate ≤ SSC_DSR_MAX (Refer to Table 4 on page 64 and Table 10 on page 72).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

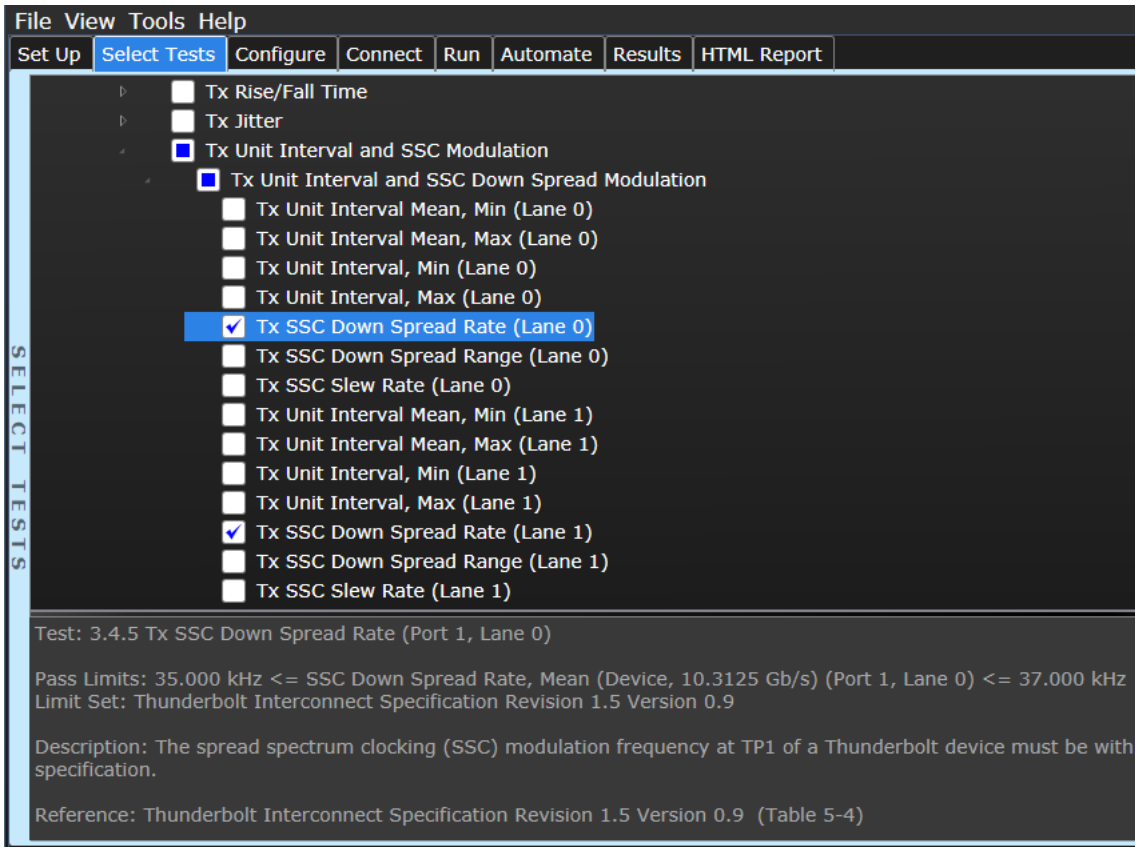


Figure 57 Selecting the Tx SSC Down Spread Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 16GHz
3 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If SSC_DSR_MIN > SSC_Down_Spread_Rate > SSC_DSR_MAX, the status of test is FAIL.

Test References

See

- "Section 3.4.5 Gen2 SSC Down Spread Rate Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx SSC Phase Deviation

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Phase Deviation Test is to confirm that the SSC Phase Deviation is within the limits of the specification.

Test Pass Requirement

2.5ns p-p ≤ SSC_Phase_Deviation ≤ SSC_PD_MAX (Refer to Table 4 on page 64 and Table 10 on page 72).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx SSC Phase* are checked.

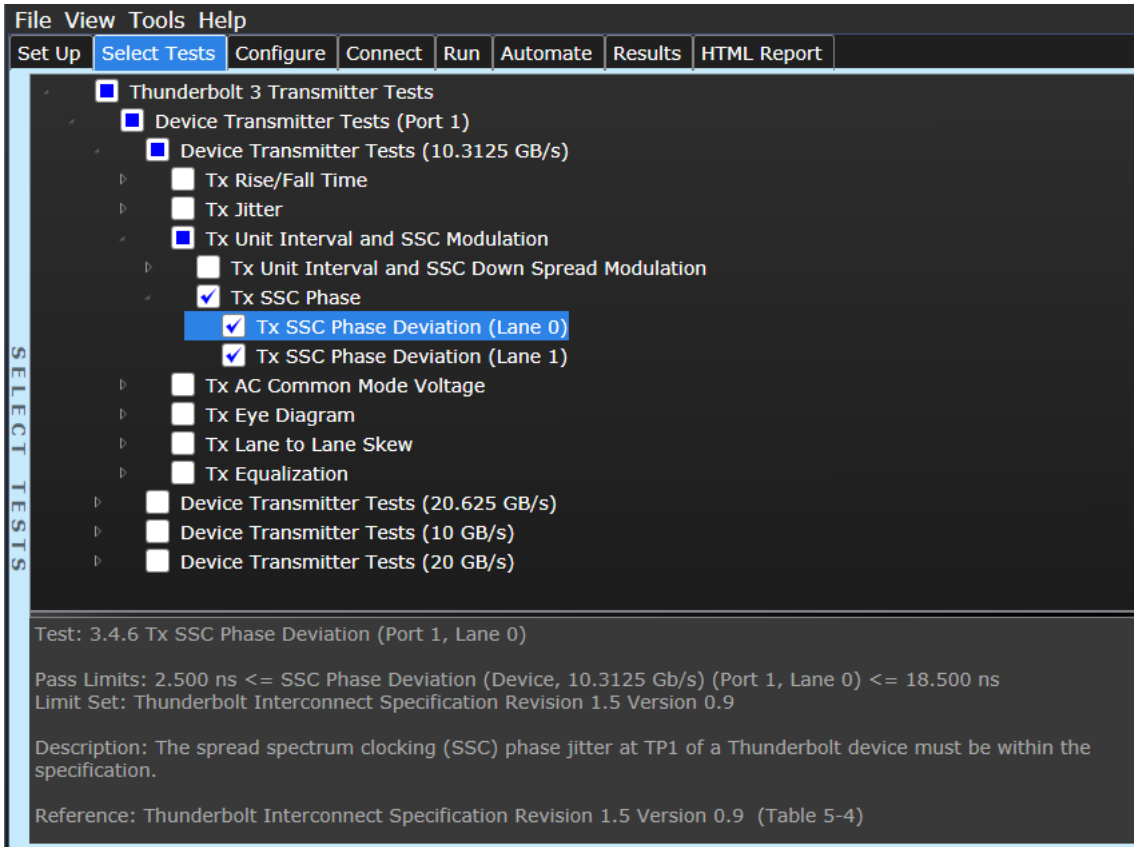


Figure 58 Selecting the Tx SSC Phase Deviation tests

Test Procedure

1. Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2. Capture the waveform and process it with the Digital Oscilloscope's software:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   - *c* No CDR, no average and no interpolation to be used
   - *d* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *e* Oscilloscope must have a minimum bandwidth of 16GHz
3. Extract the SSC Phase Deviation from the transmitted signal.
4. Extract the SSC Phase Deviation from the phase jitter after applying a 2^{nd} order low-pass filter with 3dB point at 2 MHz.
5. Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If 2.5ns p-p > SSC_Phase_Deviation > SSC_PD_MAX the status of test is FAIL.

Test References

See

- "Section 3.4.6 Gen2 SSC Phase Deviation Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx SSC Slew Rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Slew Rate Test is to confirm that the SSC Slew Rate is within the limits of the specification.

Test Pass Requirement

SSC_Slew_Rate ≤ 1000 ppm/µs (Refer to Table 4 on page 64).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

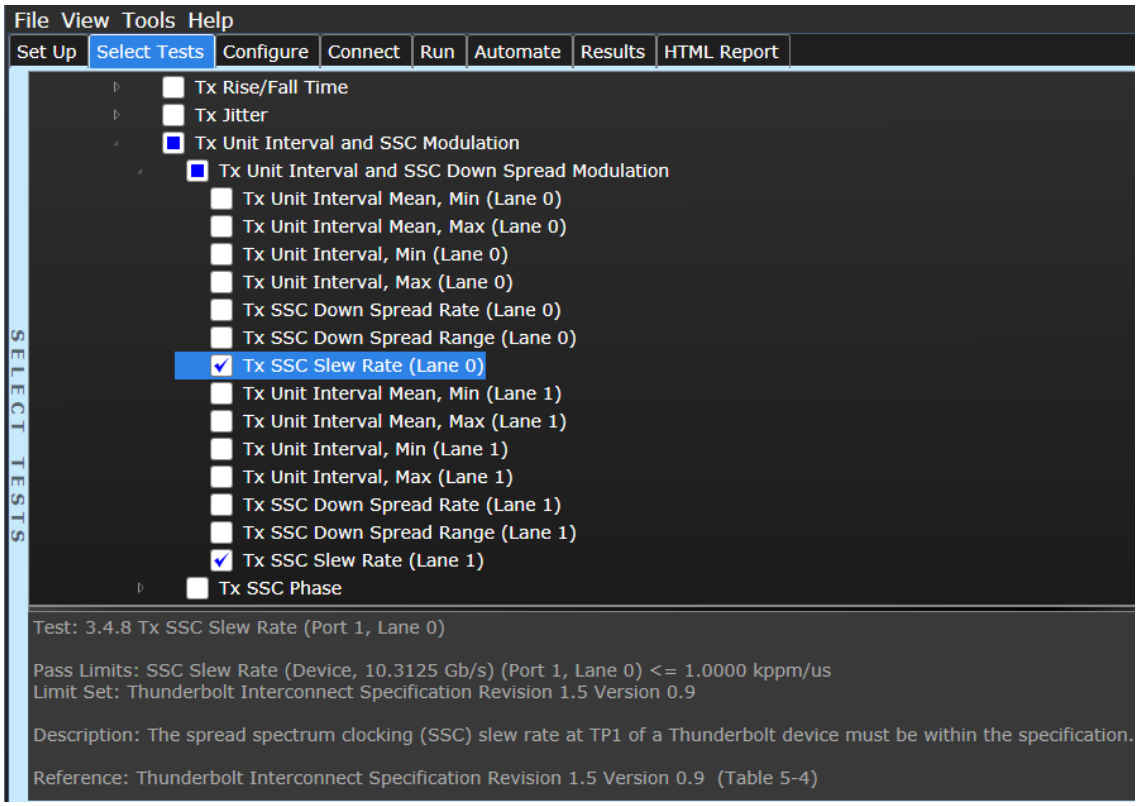


Figure 59 Selecting the Tx SSC Slew Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and post process it with an appropriate software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Extract SSC slew rate from the transmitted signal over measurement intervals of 0.5µs
   f Extract SSC slew rate from the phase information after applying a 2nd order Low-Pass-Filter with 3 dB cut-off at 2MHz.
   g Oscilloscope must have a minimum bandwidth of 16GHz
3 SSC_Slew_Rate is measured as the SSC frequency deviation over time while valid data is being transmitted in which 1E-12 bit error rate is required without assuming forward error correction.
4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If SSC_Slew_Rate > 1000 ppm/µs, the status of test is FAIL.

Test References

See

- "Section 3.4.7 Gen2 SSC Slew Rate Data Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Lane to Lane Skew

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Lane to Lane Skew Test is to confirm that the Skew between dual transmit signals of the same port group falls within the limits of the specification.

Test Pass Requirement

Lane_to_Lane_Skew ≤ 26nS (Refer to Table 4 on page 64).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Lane to Lane Skew* are checked.

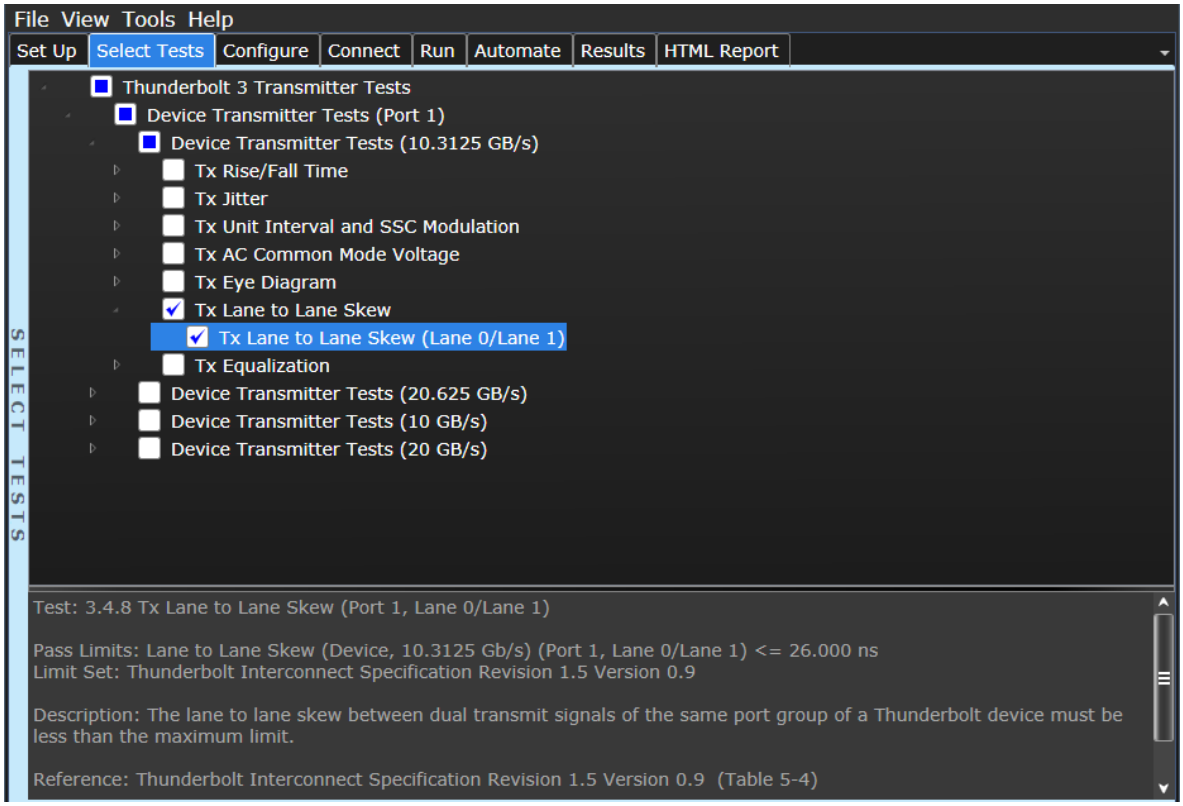


Figure 60 Selecting the Tx Lane to Lane Skew tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveforms from 2 lanes from the same port together and post process it with an appropriate software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 10Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 10Mpts.
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Measurement must be performed between consecutive rising edges
   f Oscilloscope must have a minimum bandwidth of 16GHz
3 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If Lane_to_Lane_Skew > 26nS, the status of test is FAIL.

Test References

See

- "Section 3.4.8 Gen2 Lane to Lane Skew Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Eye Diagram

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Eye Diagram Test is to confirm that the differential signal on each Thunderbolt differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram should meet the conditions depicted in Figure 61.

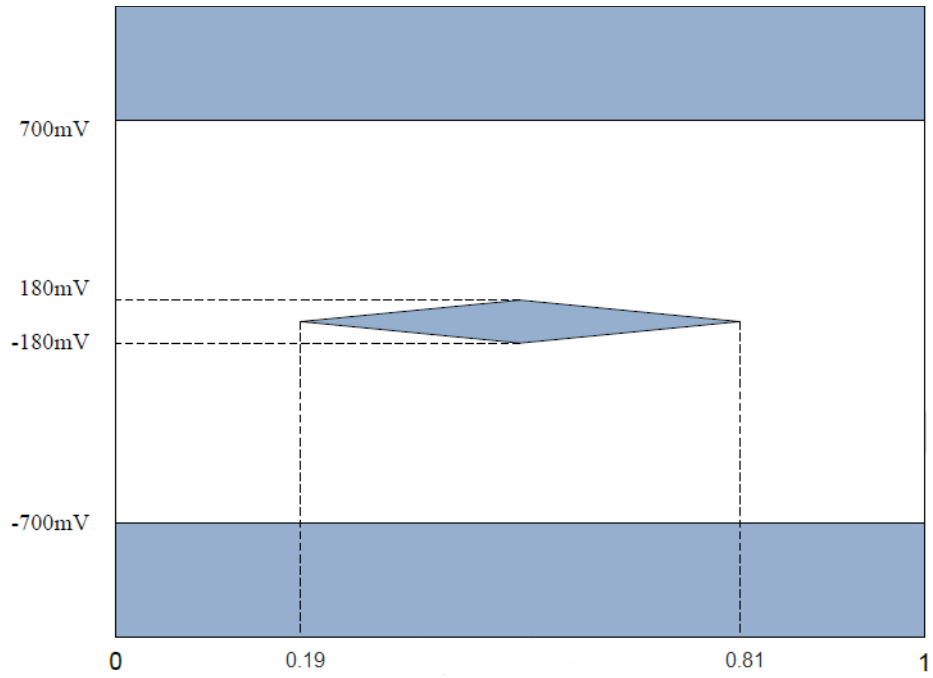


Figure 61 Pass Condition for Tx Eye Diagram Tests

(Refer to Table 6 on page 68 and Figure 41 on page 70).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Eye Diagram* are checked.

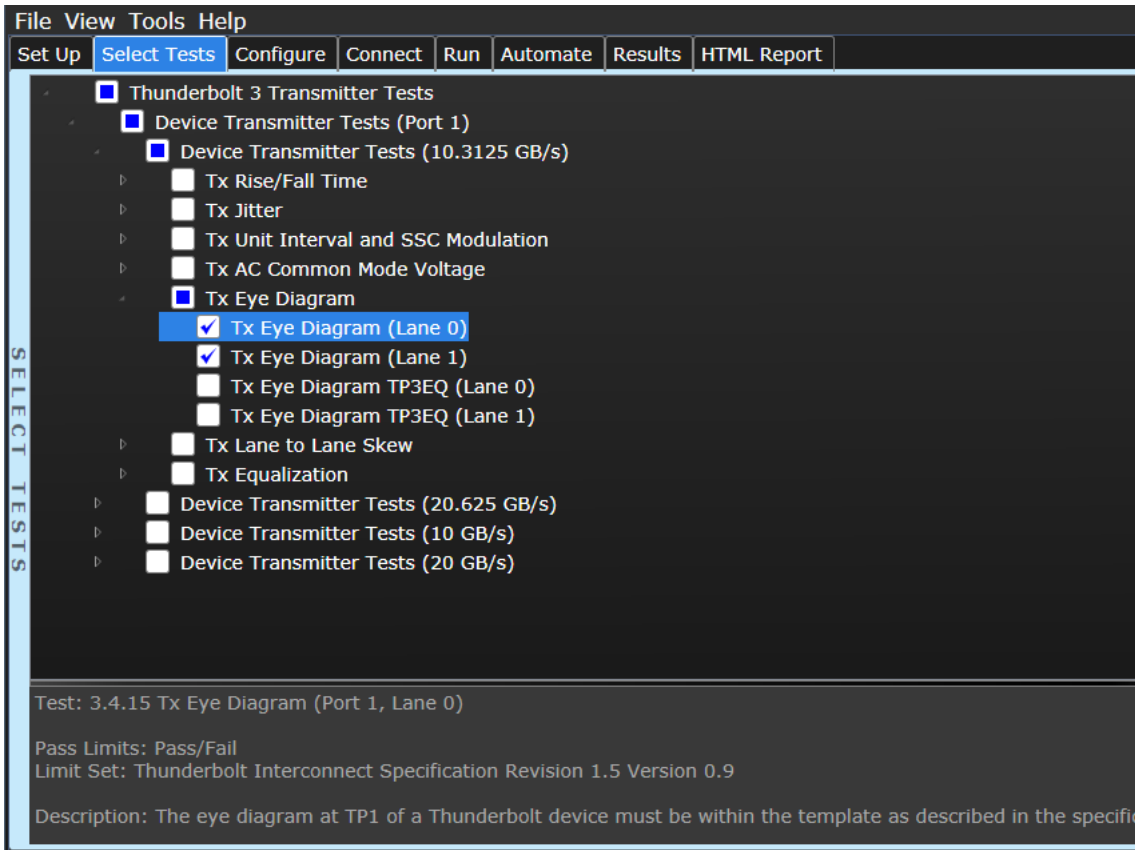


Figure 62 Selecting the Tx Eye Diagram tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 16GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Adjust vertical scale such that the signal fits within the Oscilloscope's display
   c Measured at 1E6 UI
4 Compare the data eye to the TP1 eye diagram mask. Check for conditions described in the section "Expected / Observable Results".
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the inner or outer height voltage (+/- 700mV), the status of the test is FAIL.

ii If any part of the waveform hits the mask, the status of the test is FAIL.

Test References

See

- "Section 3.4.16 Gen2 Eye Diagram Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-6 and Figure 5-15 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx AC Common Mode Voltage

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx AC Common Mode Voltage Test is to confirm that the transmitter common mode on the Thunderbolt differential signals is within the limits of the specification.

Test Pass Requirement

TX AC Common Mode Voltage $\leq 100mV_{p-p}$ (Refer to Table 6 on page 68).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx AC Common Mode Voltage* are checked.

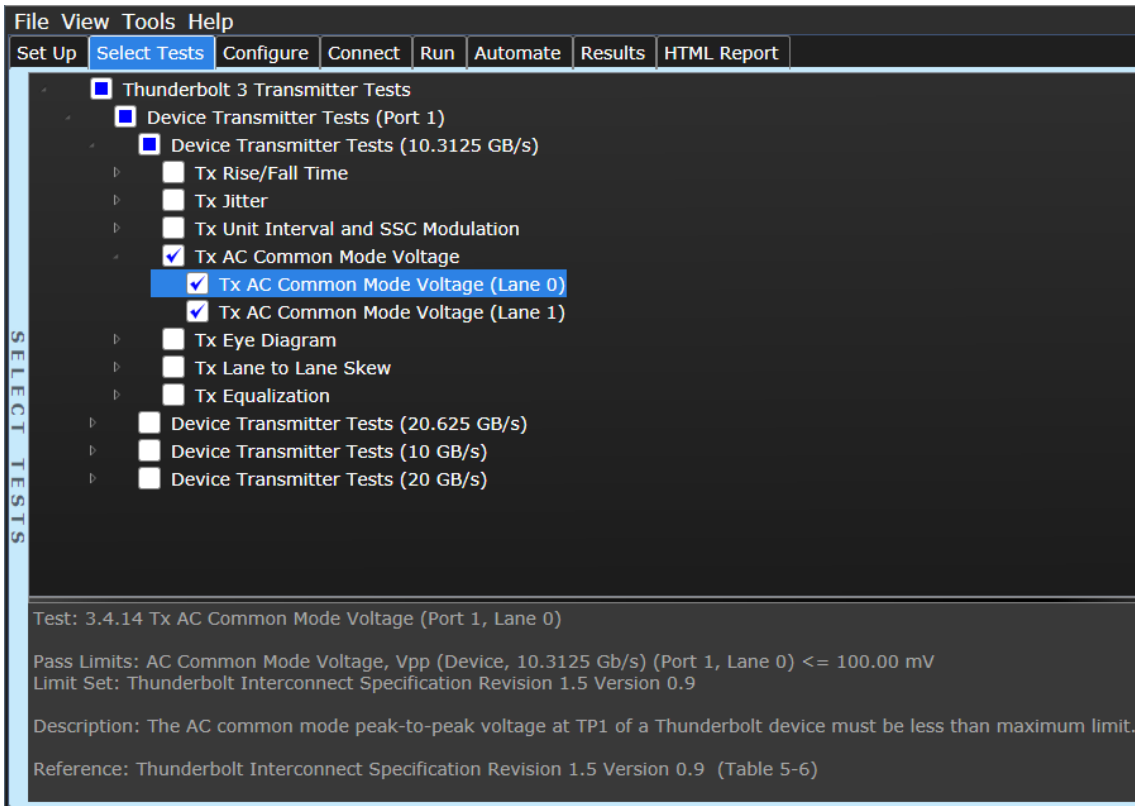


Figure 63 Selecting the Tx AC Common Mode Voltage tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Oscilloscope must have a minimum bandwidth of 16GHz
3 Calculate the AC Common Mode Voltage (V_{AC-CM}) using the equation:

$$V_{AC-CM} = (V_{TX-P} + V_{TX-N}) / 2$$

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $V_{AC-CM} > 100mV_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.4.15 Gen2 AC Common Mode Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Total Jitter TP3EQ

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Total Jitter TP3EQ Test is to confirm that the Total Jitter at point TP3EQ of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of 1E-13.

Test Pass Requirement

Total Jitter (TJ_{TP3EQ}) $\leq$ 0.60 UI_{p-p} (Refer to Table 7 on page 69).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Total Jitter* are checked.

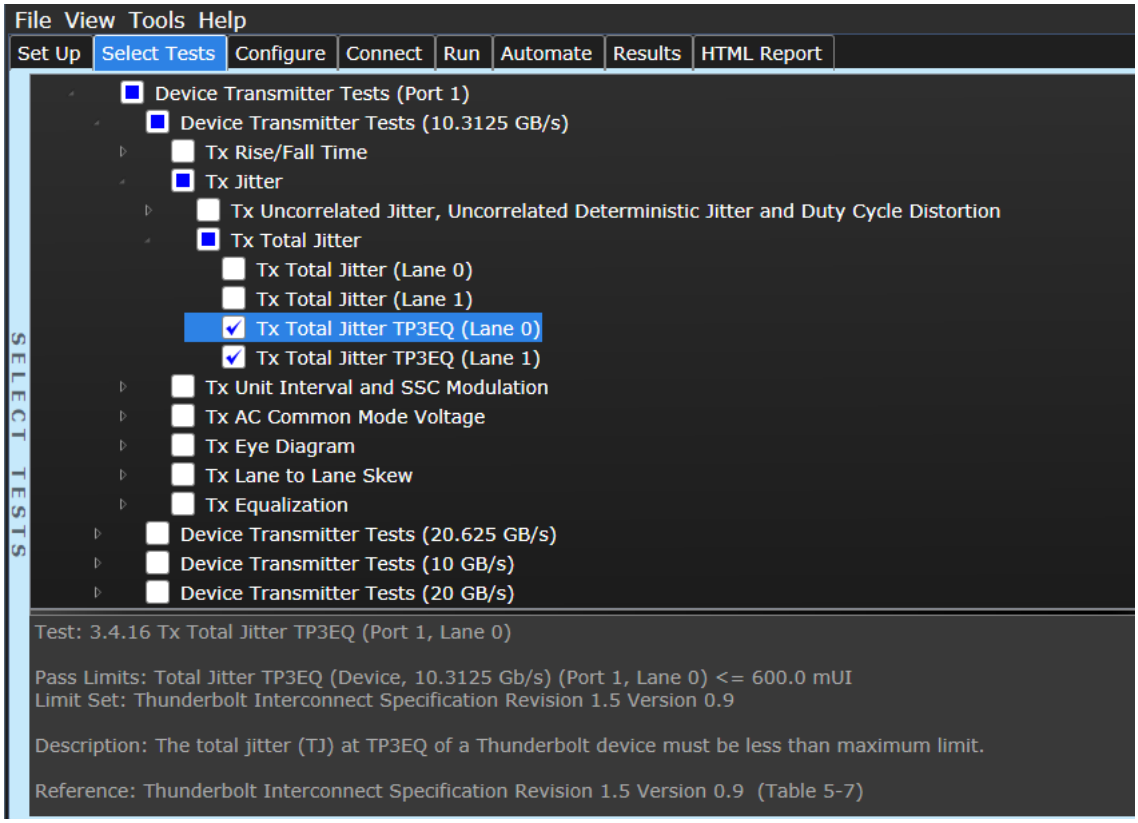


Figure 64 Selecting the Tx Total Jitter TP3EQ tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Embed the Type-C cable in the Oscilloscope. For Gen 2 systems, use TP3_EQ embedding file *TBT_2m.s4p*.
3. De-embed the cables from the test fixture to the Oscilloscope.
4. Ensure that measurements are done with a calibrated reference equalizer (CTLE only). See "Tx CTLE Calibration" on page 78.
5. Perform measurements with:
   - *a* Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   - *b* Oscilloscope with a minimum bandwidth of 16GHz
6. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Pattern length – Periodic
   - *c* Jitter Separation method must be suitable for cross-talk on the signal
   - *d* Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   - *e* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *f* Referenced to 1E-13 statistics
7. Capture the values of Total Jitter (TJ_{TP3EQ}) and Deterministic Jitter (DJ_{TP3EQ}).

8 If $TJ_{TP3EQ} > 0.60\ UI_{p-p}$, perform the following steps:

a Configure the DUT transmitter to output alternating square pattern of one 0's and one 1's on all lanes with SSC enabled. (The pattern is SQ2 instead of PRBS15).

b Perform measurements with:

- Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
- Oscilloscope with a minimum bandwidth of 16GHz

c Capture the waveform and process it with the Digital Oscilloscope:

- Sampling Rate $\geq$ 80 GSa/s
- Pattern length – Periodic
- Jitter Separation method must be suitable for cross-talk on the signal
- Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
- Adjust vertical scale such that the signal fits within the Oscilloscope's display.
- Referenced to 1E-13 statistics.

d Capture the Random Jitter (RJ_{TP3EQ}) result.

e Calculate TJ_{TP3EQ} using the equation:

$TJ_{TP3EQ} = DJ_{TP3EQ} + 14.7 * RJ_{TP3EQ}$ (DJ_{TP3EQ} from #7; PRBS15 and RJ_{TP3EQ} from #8d; SQ2)

9 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $TJ_{TP3EQ} > 0.60\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.4.17 Gen2 Total Jitter TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-7 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Uncorrelated Jitter TP3EQ

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Jitter TP3EQ Test is to confirm that the Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] at point TP3EQ of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Jitter (UJ_{TP3EQ}) $\leq$ 0.31 UI_{p-p} (Refer to Table 7 on page 69).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

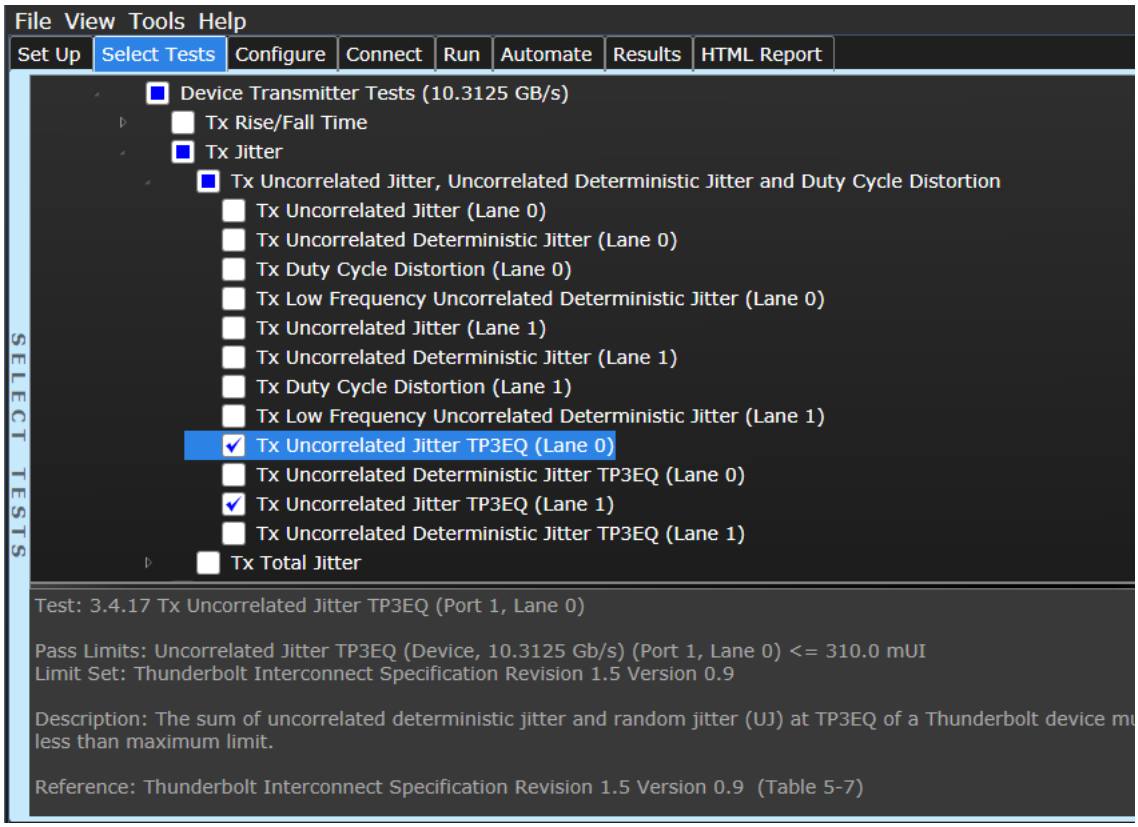


Figure 65 Selecting the Tx Uncorrelated Jitter TP3EQ tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Embed the Type-C cable in the Oscilloscope. For Gen 2 systems, use TP3_EQ embedding file *TBT_2m.s4p*.
3. De-embed the cables from the test fixture to the Oscilloscope.
4. Ensure that measurements are done with a calibrated reference equalizer (CTLE only). See "Tx CTLE Calibration" on page 78.
5. Perform measurements with:
   a. Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b. Oscilloscope with a minimum bandwidth of 16GHz
6. Capture the waveform and process it with the Digital Oscilloscope:
   a. Sampling Rate $\geq$ 80 GSa/s
   b. Pattern length – Periodic
   c. Jitter Separation method must be suitable for cross-talk on the signal
   d. Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   e. Adjust vertical scale such that the signal fits within the Oscilloscope's display
   f. Referenced to 1E-13 statistics
7. Capture the values of Total Jitter (TJ_{TP3EQ}) and Data Deterministic Jitter (DDJ_{TP3EQ}).

8 Calculate UJ_{TP3EQ} using the equation:

$$UJ_{TP3EQ} = TJ_{TP3EQ} - DDJ_{TP3EQ}$$

9 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $UJ_{TP3EQ} > 0.31\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.4.18 Gen2 UJ TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-7 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Uncorrelated Deterministic Jitter TP3EQ

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Deterministic Jitter TP3EQ Test is to confirm that the Uncorrelated Deterministic Jitter at point TP3EQ of the transmitter is within the limits of the specification.

Test Pass Requirement

Deterministic Jitter that is uncorrelated to the transmitted data (UDJ_{TP3EQ}) $\leq$ 0.17 UI_{p-p} (Refer to Table 7 on page 69).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

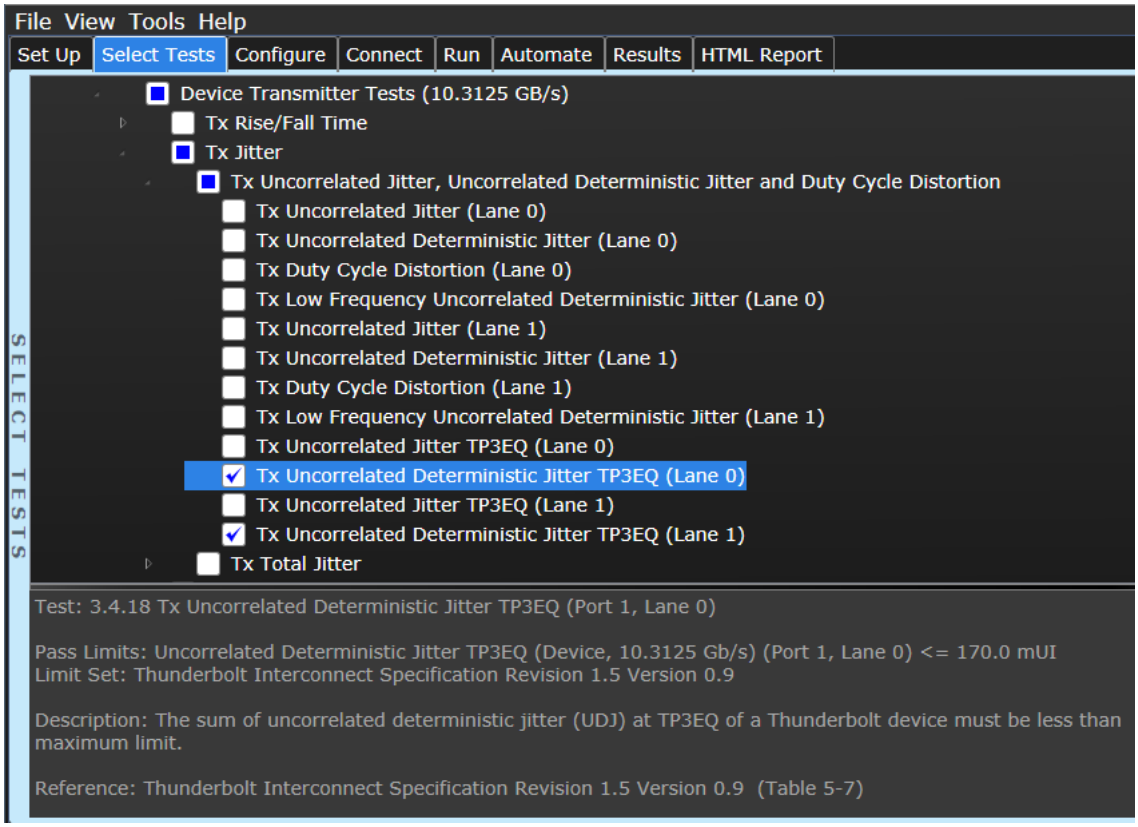


Figure 66 Selecting the Tx Uncorrelated Deterministic Jitter TP3EQ tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Embed the Type-C cable in the Oscilloscope. For Gen 2 systems, use TP3_EQ embedding file *TBT_2m.s4p*.
3. De-embed the cables from the test fixture to the Oscilloscope.
4. Ensure that measurements are done with a calibrated reference equalizer (CTLE only). See "Tx CTLE Calibration" on page 78.
5. Perform measurements with:
   a. Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b. Oscilloscope with a minimum bandwidth of 16GHz
6. Capture the waveform and process it with the Digital Oscilloscope:
   a. Sampling Rate $\geq$ 80 GSa/s
   b. Pattern length – Periodic
   c. Jitter Separation method must be suitable for cross-talk on the signal
   d. Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   e. Adjust vertical scale such that the signal fits within the Oscilloscope's display
7. Capture the values of Total Jitter (TJ_{TP3EQ}) and Data Deterministic Jitter (DDJ_{TP3EQ}).

8 Capture the UDJ_{TP3EQ} result (same as BUJ over the Oscilloscope).

9 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $UDJ_{TP3EQ} > 0.17\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.4.19 Gen2 UDJ TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-7 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Eye Diagram TP3EQ

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Eye Diagram TP3EQ Test is to confirm that the differential signal on each Thunderbolt differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram at TP3EQ should meet the conditions depicted in Figure 67.

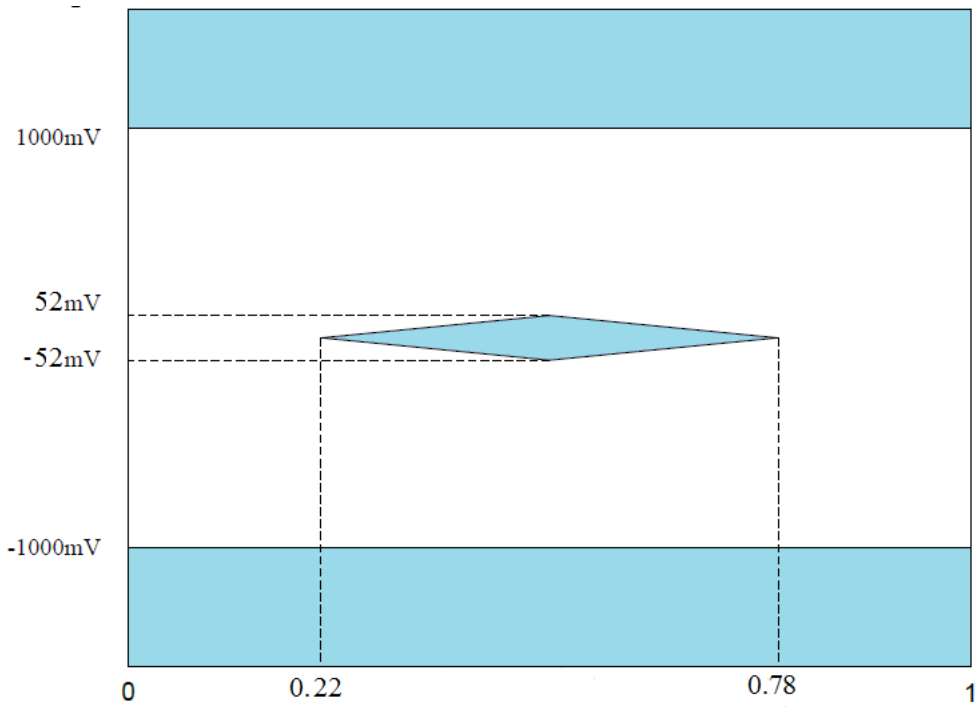


Figure 67 Pass Condition for Tx Eye Diagram TP3EQ Tests

(Refer to Table 7 on page 69 and Figure 41 on page 70).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Eye Diagram* are checked.

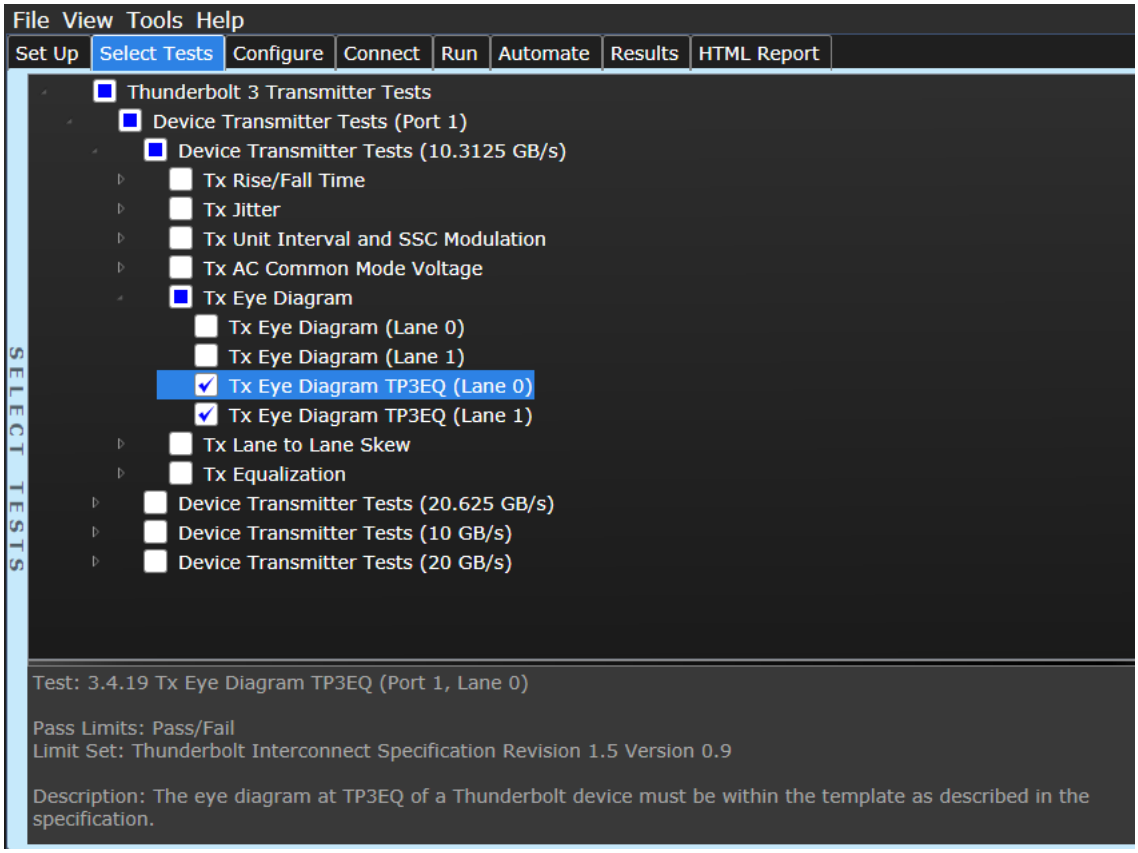


Figure 68 Selecting the Tx Eye Diagram TP3EQ tests

Test Procedure

1. Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2. Embed the Type-C cable in the Oscilloscope. For Gen 2 systems, use TP3_EQ embedding file *TBT_2m.s4p*.
3. De-embed the cables from the test fixture to the Oscilloscope.
4. Ensure that measurements are done with a calibrated reference equalizer (CTLE and DFE). See "Tx CTLE Calibration" on page 78.
5. Perform measurements with:
   - *a* Reference CDR based on the 2^{nd} order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   - *b* Oscilloscope with a minimum bandwidth of 16GHz
6. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Adjust vertical and horizontal scale such that the signal fits within the Oscilloscope's display
   - *c* Accumulate at 1E6 UI
7. Compare the data eye to the TP3EQ eye diagram mask. Check for conditions described in the section "Expected / Observable Results".
8. Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the inner or outer eye height voltage (+/-1000mV), the status of the test is FAIL.

ii If any part of the waveform hits the mask, the status of the test is FAIL.

Test References

See

- "Section 3.4.20 Gen2 Eye Diagram Measurement TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-7 and Figure 5-15 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Equalization Tests

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Equalization Tests is to confirm that the transmitter equalization is within the limits of the specification. The Tx Equalization Tests are further divided into three tests, namely:

- Tx Equalization Pre-shoot
- Tx Equalization Deemphasis
- Tx Swing Preset 15

Test Pass Requirement

Transmitter Swing: 3.5 ± 1dB (for preset 15 only)

Pre-shoot, De-Emphasis: ± 1dB for the following presets:

Table 11 Transmitter Equalization Presets

Preset Number	Pre-Shoot	De-Emphasis
0	0	0
1	0	-1.9
2	0	-3.6
3	0	-5.0
4	0	-8.4
5	0.9	0
6	1.1	-1.9
7	1.4	-3.8
8	1.7	-5.8
9	2.1	-8.0
10	1.7	0
11	2.2	-2.2
12	2.5	-3.6
13	3.4	-6.7
14	4.3	-9.3
15	1.7	-1.7

(Refer to Table 5 on page 66).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Equalization* are checked.

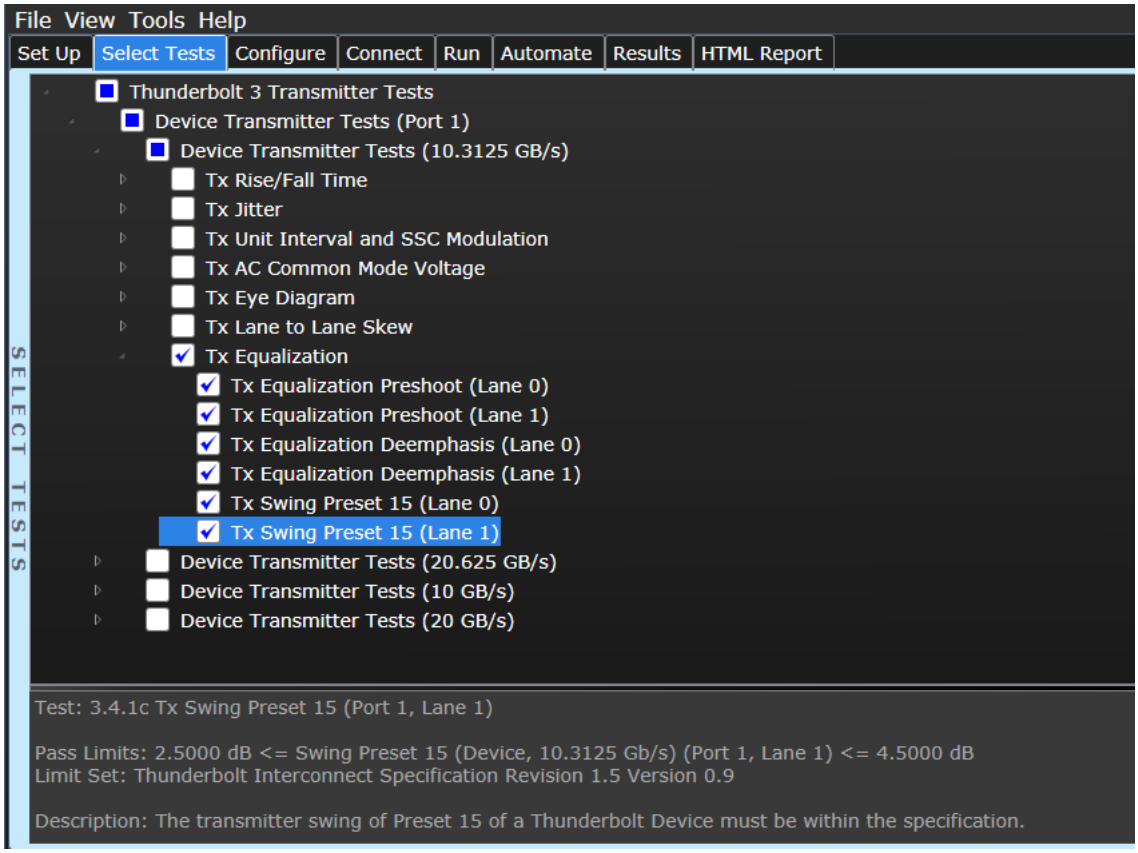


Figure 69 Selecting the Tx Equalization tests

4 Under the **Configure** tab of the Test Application, select **ALL** for the Configuration Variable “Tx Equalization” to run the tests for preset numbers P0 to P15.

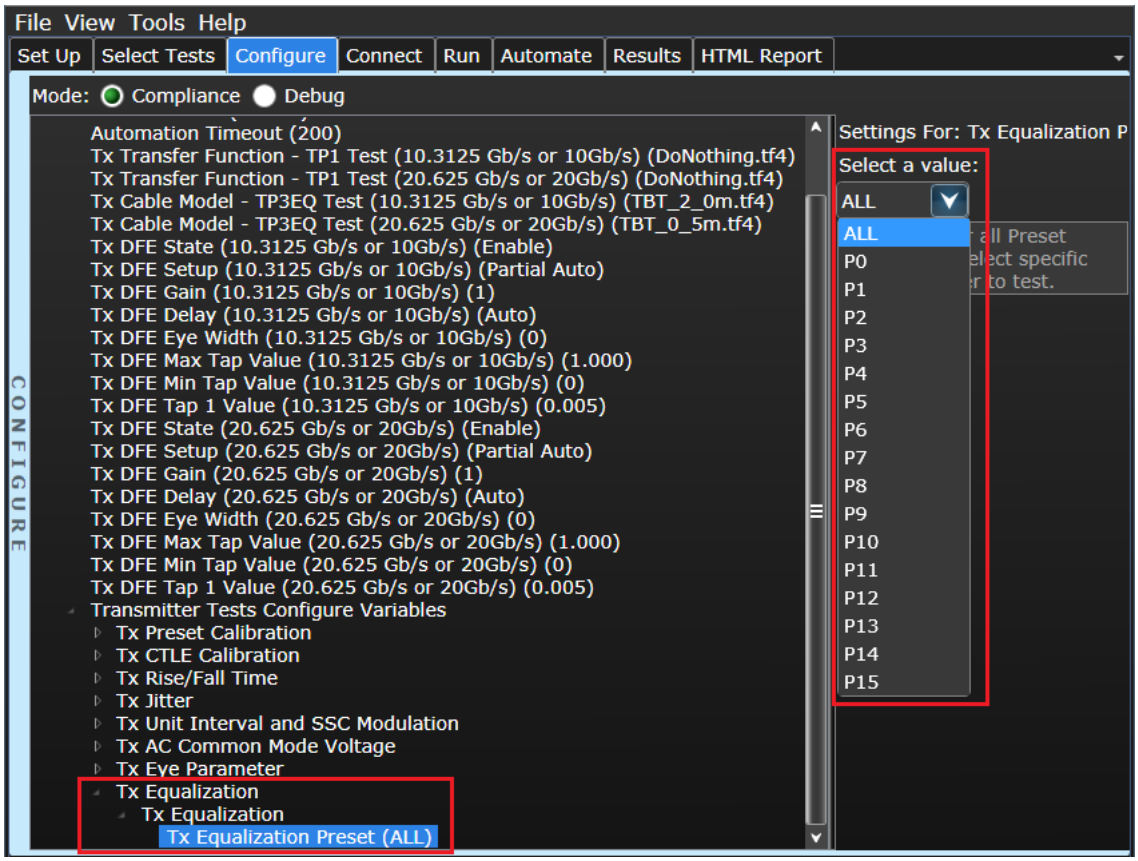


Figure 70 Configuring Tx Equalization Preset Variable

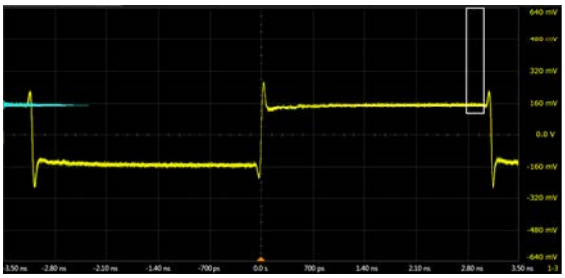
Test Procedure

1 Set Preset 0 (P0).

2 Configure the DUT transmitter to output alternating square pattern of 64 0’s and 64 1’s on all lanes with SSC enabled along with both pre-shoot and de-emphasis enabled.

3 Adjust vertical scale such that the signal fits within the Oscilloscope’s display.

4 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



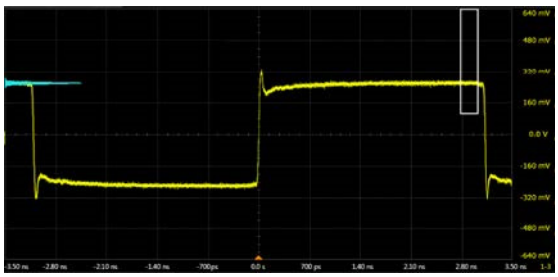
5 Measure differential amplitude voltage (V_1) for bits 57 to 62 using the equation:

$$V_1 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

6 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with de-emphasis enabled but no pre-shoot.

7 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

8 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



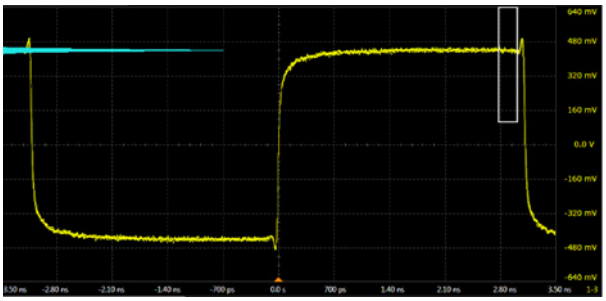
9 Measure differential amplitude voltage (V_2) for bits 57 to 62 using the equation:

$$V_2 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

10 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with pre-shoot enabled but no de-emphasis.

11 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

12 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



13 Measure differential amplitude voltage (V_3) for bits 57 to 62 using the equation:

$$V_3 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

$$\text{Set Pre-Shoot to be } 20 * \log_{10} [V_2/V_1]$$

$$\text{Set De-Emphasis to be } 20 * \log_{10} [V_1/V_3]$$

14 Repeat steps 2 to 10 for all Presets defined in Table 11.

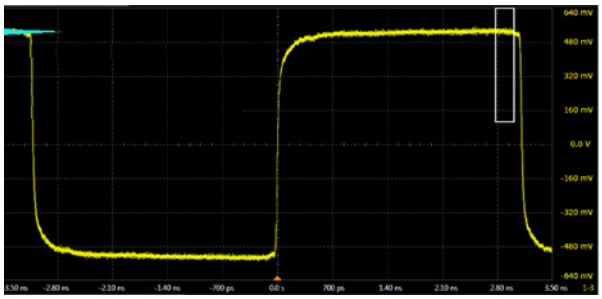
15 Check for PASS/FAIL conditions for both Pre-shoot and De-emphasis.

16 Set the DUT to Preset 0 (P0).

17 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

18 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

19 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



20 Measure differential amplitude voltage (V_0) for bits 57 to 62 using the equation:

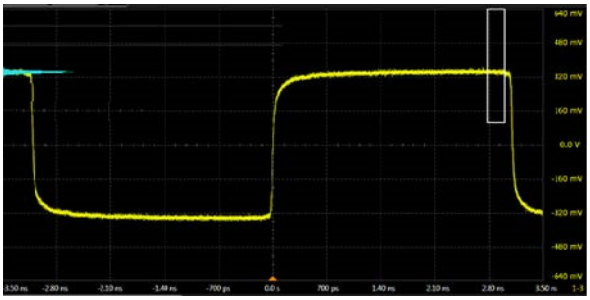
$$V_0 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

21 Set the DUT to Preset 15 (P15).

22 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

23 Adjust vertical scale such that the signal fits within the Oscilloscope's display

24 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



25 Measure differential amplitude voltage (V_{15}) for bits 57 to 62 using the equation:

$$V_{15} = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

$$\text{Set Swing to be } 20 * \log_{10} [V_0/V_{15}]$$

26 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If the Pre-Shoot for a particular Preset number is not within ± 1dB of the matching value in Table 11, the status of test is FAIL.

If the De-Emphasis for a particular Preset number is not within ± 1dB of the matching value in Table 11, the status of test is FAIL.

If Swing < 2.5 dB or Swing > 4.5 dB, the status of test is FAIL.

Test References

See

- "Section 3.4.1 Gen2 Transmitter Equalization" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-5 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

6 Transmitter Tests for 10 GB/s Systems

This section provides the Methods of Implementation (MOIs) to run electrical tests on a Thunderbolt DUT operating at a bit rate of 10 GB/s using an Keysight Infiniium Oscilloscope and other accessories, along with the Thunderbolt 3 Test Application.

NOTE All Thunderbolt 3 devices that support a bit rate of 10 Gb/s are classified as Gen2 devices.

Tx Preset Calibration

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Preset Calibration Test is to find the optimized preset for the platform.

NOTE Prior to running the compliance tests, the Host / Device must go through Preset Calibration.

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Preset Calibration* are checked.

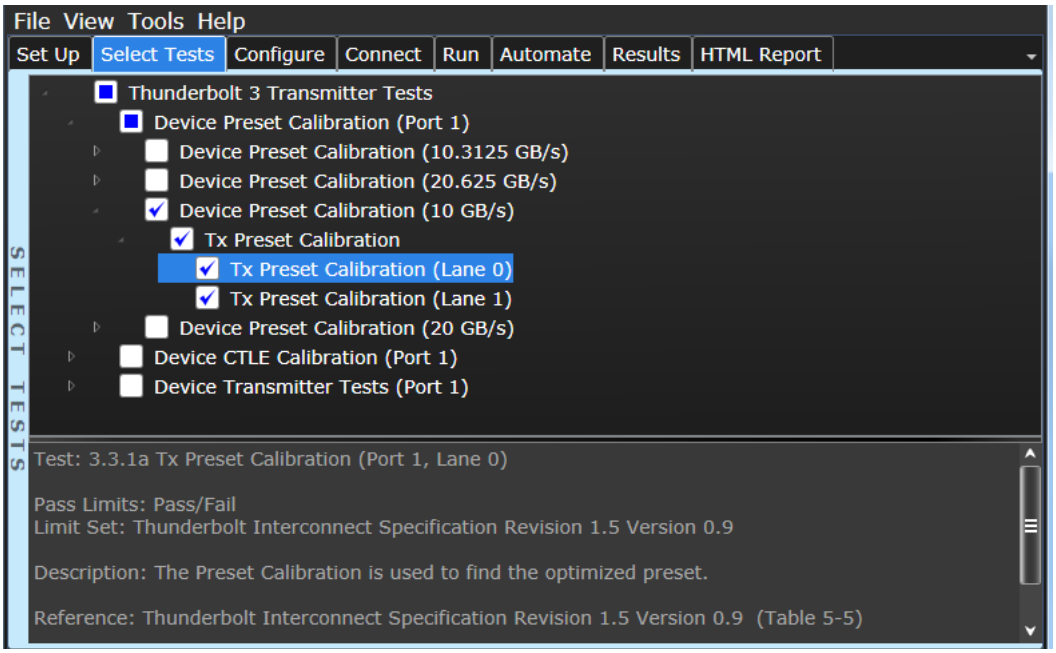


Figure 71 Selecting the Tx Preset Calibration tests

NOTE By default, the test group for **Preset Calibration** for each selected bit-rate is hidden in the **Select Tests** tab when **Predefined Optimum Preset Number** is selected for the respective bit-rates. To view and select the **Preset Calibration** tests in the **Select Tests** tab, select the **Run Preset Calibration** option in the **Test Setup** window of the **Set Up** tab.

Test Procedure

1 Connect the DUT to the Oscilloscope.
2 Configure the DUT transmitter to output PRBS31, preset 0 on all lanes with SSC enabled.
3 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used.
   b Oscilloscope with a minimum bandwidth of 16GHz.
4 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Adjust vertical and horizontal scales such that the signal fits within the Oscilloscope's display
   c Measured at 1E6 UI
5 Capture eye height and eye width for lane 0.
6 Register mean eye height and mean eye width values.
7 Repeat the test for all remaining Thunderbolt transmit presets (till preset 15 as shown in Table 5).
8 Repeat the test for the remaining Thunderbolt lanes.
9 For each lane, choose the preset that provides maximum eye width. If there are two presets with the same eye width, select the one with the greater eye height.

Expected / Observable Results

For each lane, the preset that provides the maximum eye width is the optimized preset for the platform. If two presets have the same eye width, the preset with a greater eye height is the optimized preset.

Test References

See

- "Section 3.3.1 Preset Calibration" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-5 of the *Thunderbolt™ Interconnect Specification Revision 1.5 Version 0.9.*

Tx CTLE Calibration

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx CTLE Calibration Test is to find the optimized CTLE (Continuous-Time-Linear-Equalizer) for the platform.

See "Reference CTLE" on page 61 to know more about CTLE.

NOTE Apply equalization on the Oscilloscope, when testing at TP3EQ.

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx CTLE Calibration* are checked.

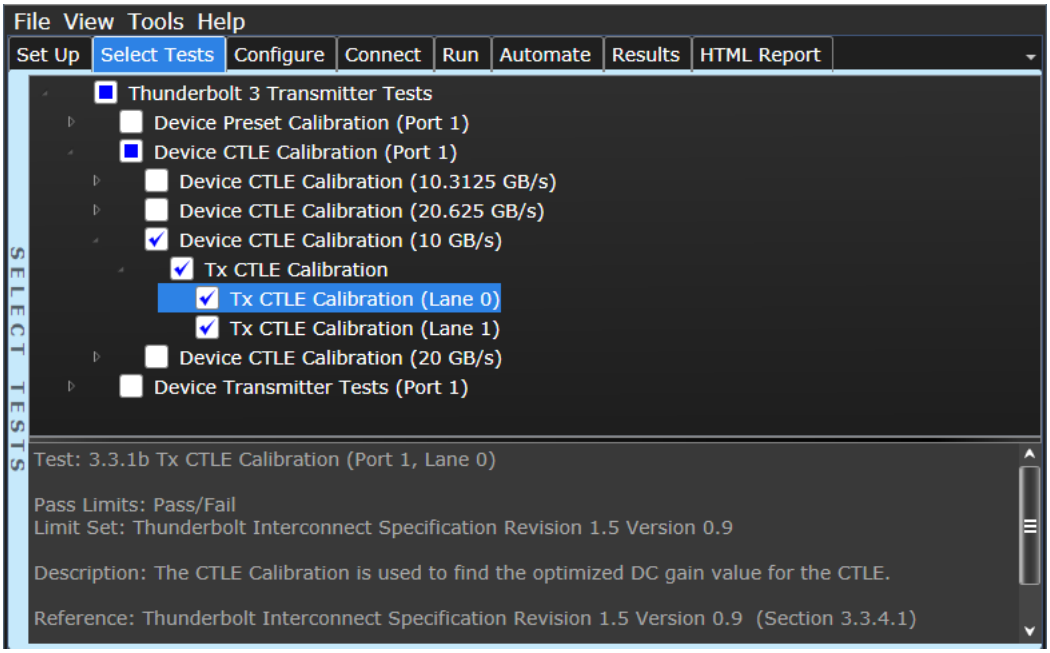


Figure 72 Selecting the Tx CTLE Calibration tests

NOTE By default, the test group for **CTLE Calibration** for each selected bit-rate is hidden in the **Select Tests** tab when **Predefined Optimum CTLE DC Gain Value** is selected for the respective bit-rates. To view and select the **CTLE Calibration** tests in the **Select Tests** tab, select the **Run CTLE Calibration** option in the **Test Setup** window of the **Set Up** tab.

Test Procedure

1 Follow the CTLE model as described in "Reference CTLE" on page 61, with the following parameters:

a AC Gain = 1.41

b Wp1 = 2 * π * 1.5G rad/sec

c Wp2 = 2 * π * 5G rad/sec

2 Apply ten different CTLE configurations such that A_{DC}, which is the DC Gain, is a value that lies within the following equation:

$$\{10^{-x/20} : x = 0 – 9\ [dB]\}$$

3 Calibrate A_{DC} using the following procedure:

a Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

b Select A_{DC} for x = 0.

c Perform measurement with reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.

d Capture the waveform and process it with the Digital Oscilloscope:

- Sampling Rate $\geq$ 80 GSa/s
- Adjust vertical & horizontal scale such that the signal fits within the Oscilloscope's display
- Measured at 1E6 UI

e Eye height should be positioned at the "0" of the real time eye horizontal position.

f Apply a Histogram to the lower and upper sections of the eye, with ±1% deviation in time axis in order to calculate the eye height. Eye height is the delta between the minimum value from the upper histogram result (see Figure 73) and the maximum value from the lower histogram result (see Figure 75).

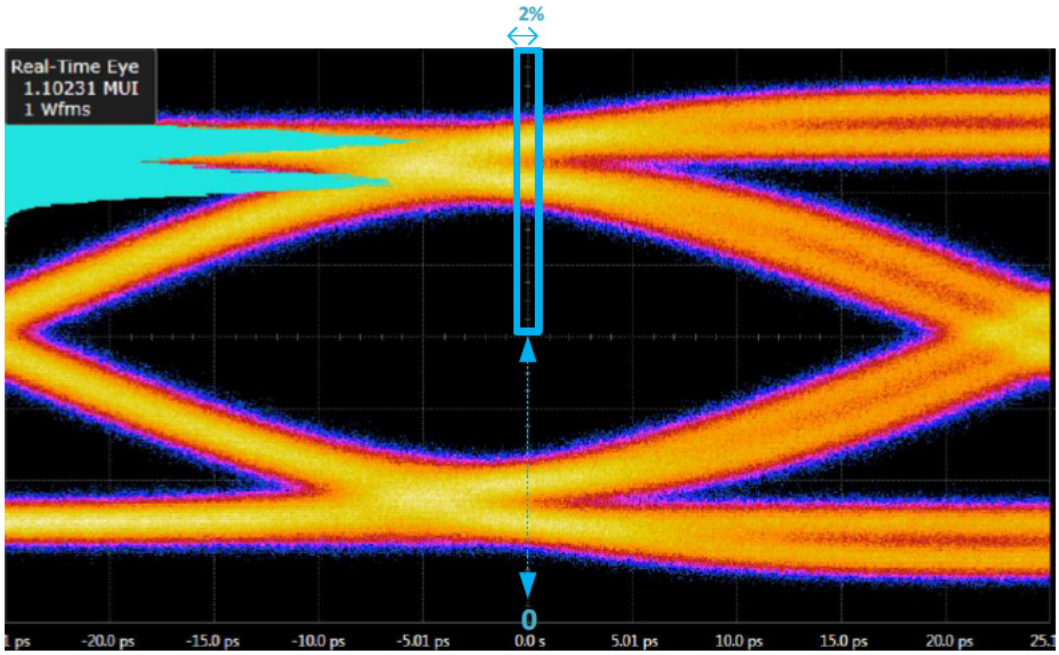


Figure 73 Thunderbolt RX TP3EQ Eye Height upper location measurement

Figure 74

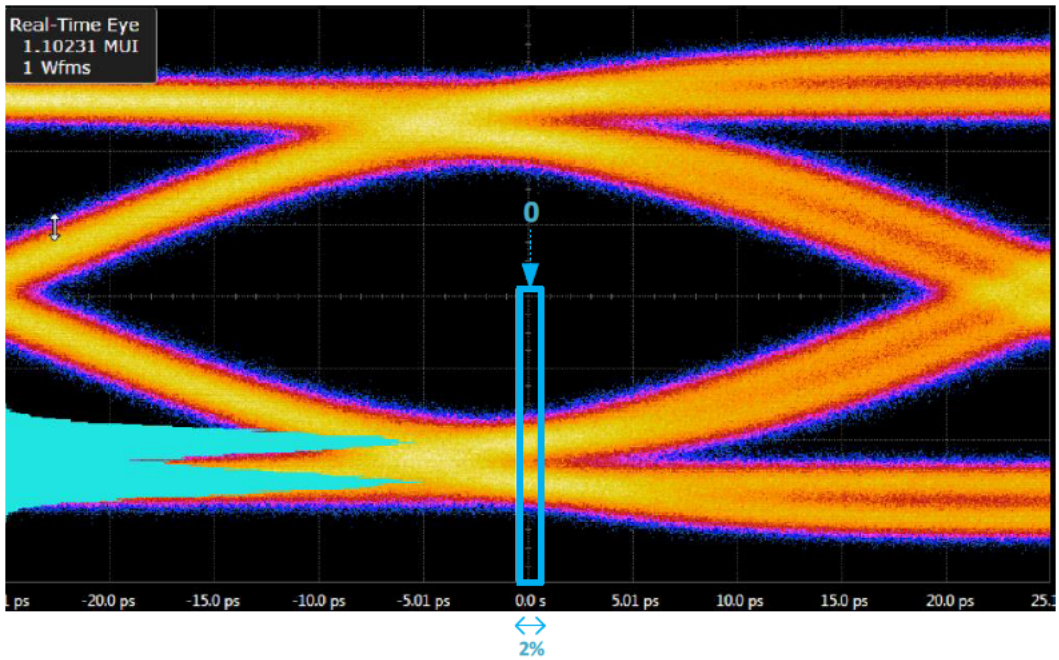


Figure 75 Thunderbolt RX TP3EQ Eye Height lower location measurement

g Capture five times (each time over new 1MUI record length) the minimum value of both eye height and eye width.

h Average the five captured values, that is, average of (5 times minimum eye height) and average of (5 times minimum eye width).

i Repeat this procedure from step 3b to 3i with x = x + 1 upto x = 9.

j Measure that value of A_{DC} (including DFE tap value), which yields the maximum eye height. If there are two values of A_{DC} (including DFE tap value), which have the same eye height, select the one that has the greater eye width.

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

For each lane, the DC Gain value that provides the maximum eye height is the optimized CTLE for the platform. If two DC Gain values have the same eye height, the one with a greater eye width is the optimized CTLE.

Test References

See

- "Section 8.1 Appendix C – Equalization Calibration" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9.*
- Section 3.3.4.1 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Rise/Fall Time

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Rise/Fall Time Test is to confirm that the rise times and fall times on the Thunderbolt differential signals are within the limits of the specification.

Test Pass Requirement

Rise Time and Fall Time ≥ 10ps (Refer to Table 4 on page 64).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Rise/Fall Time* are checked.

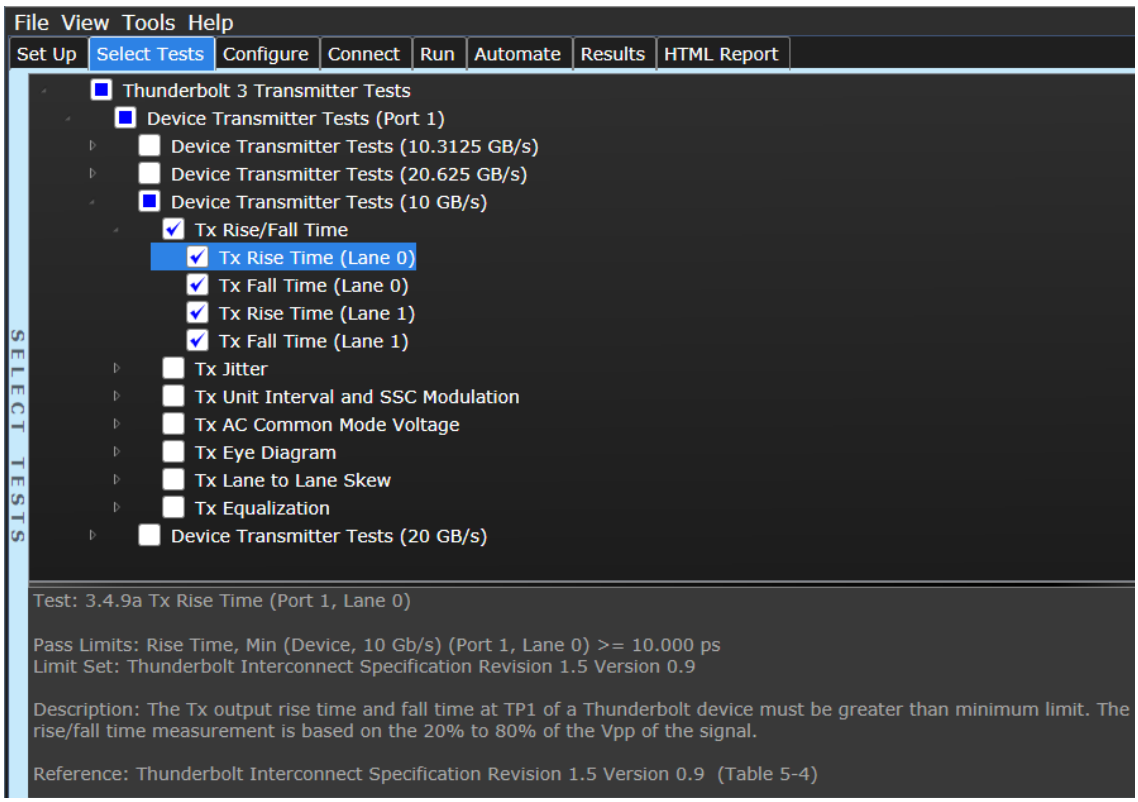


Figure 76 Selecting the Tx Rise/Fall Time tests

Test Procedure

1 Configure the DUT transmitter to output alternating square pattern of 16 0's and 16 1's on all lanes with SSC enabled.
2 Evaluate at least 4Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 4Mpts. Use the maximum analog bandwidth of the Oscilloscope.

   No CDR, no average and no interpolation to be used.

   Adjust vertical scale such that the signal fits within the Oscilloscope's display.
3 Measure T_{RISE} as the mode of the sampled edge times from 20% to 80% of the differential swing voltage rising edge.
4 Measure T_{FALL} as the mode of the sampled edge times from 80% to 20% of the differential swing voltage falling edge.
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If T_{RISE} < 10ps, the status of test is FAIL.

If T_{FALL} < 10ps, the status of test is FAIL.

Test References

See

- "Section 3.4.9 Gen2 Rise/Fall Time Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Total Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Total Jitter Test is to confirm that the Total Jitter of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of $1x10^{-13}$.

Test Pass Requirement

Total Jitter (TJ) $\leq$ 0.38 UI_{p-p} (Refer to Table 6 on page 68).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Total Jitter* are checked.

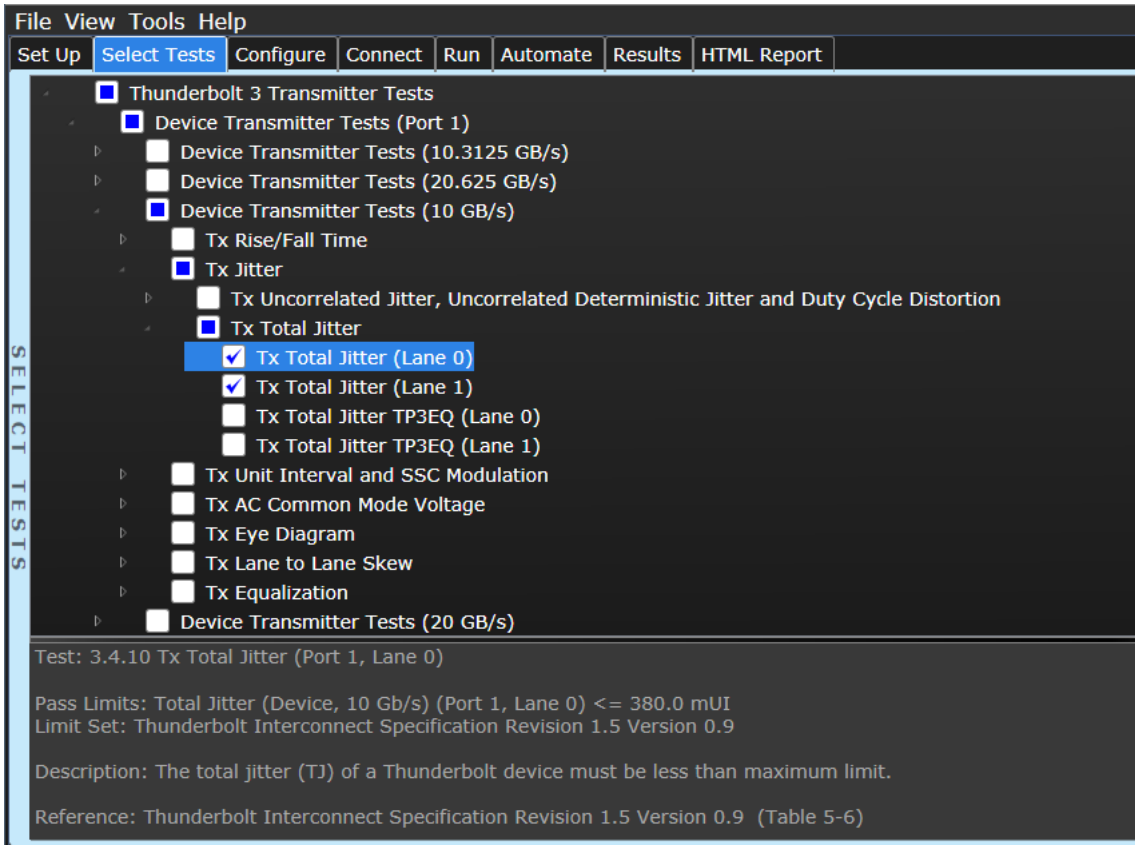


Figure 77 Selecting the Tx Total Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   b Oscilloscope with a minimum bandwidth of 16GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display.
   f Referenced to 1E-13 statistics.
4 Capture the values of Total Jitter (TJ) and Deterministic Jitter (DJ).
5 If TJ > 0.38 UI_{p-p}, perform the following steps:
   a Configure the DUT transmitter to output alternating square pattern of one 0's and one 1's on all lanes with SSC enabled. (The pattern is SQ2 instead of PRBS15).
   b Perform measurements with:

- Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
- Oscilloscope with a minimum bandwidth of 16GHz

c Capture the waveform and process it with the Digital Oscilloscope:

- Sampling Rate $\geq$ 80 GSa/s
- Pattern length – Periodic
- Jitter Separation method must be suitable for cross-talk on the signal
- Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
- Adjust vertical scale such that the signal fits within the Oscilloscope's display.
- Referenced to 1E-13 statistics.

d Capture the Random Jitter (RJ) result.

e Calculate TJ using the equation:

TJ = DJ + 14.7 * RJ (DJ from #4; PRBS15 and RJ from #5d; SQ2)

6 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If TJ > 0.38 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.4.10 Gen2 Total Jitter" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Uncorrelated Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Jitter Test is to confirm that the Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Jitter (UJ) $\leq$ 0.31 UI_{p-p} (Refer to Table 6 on page 68).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

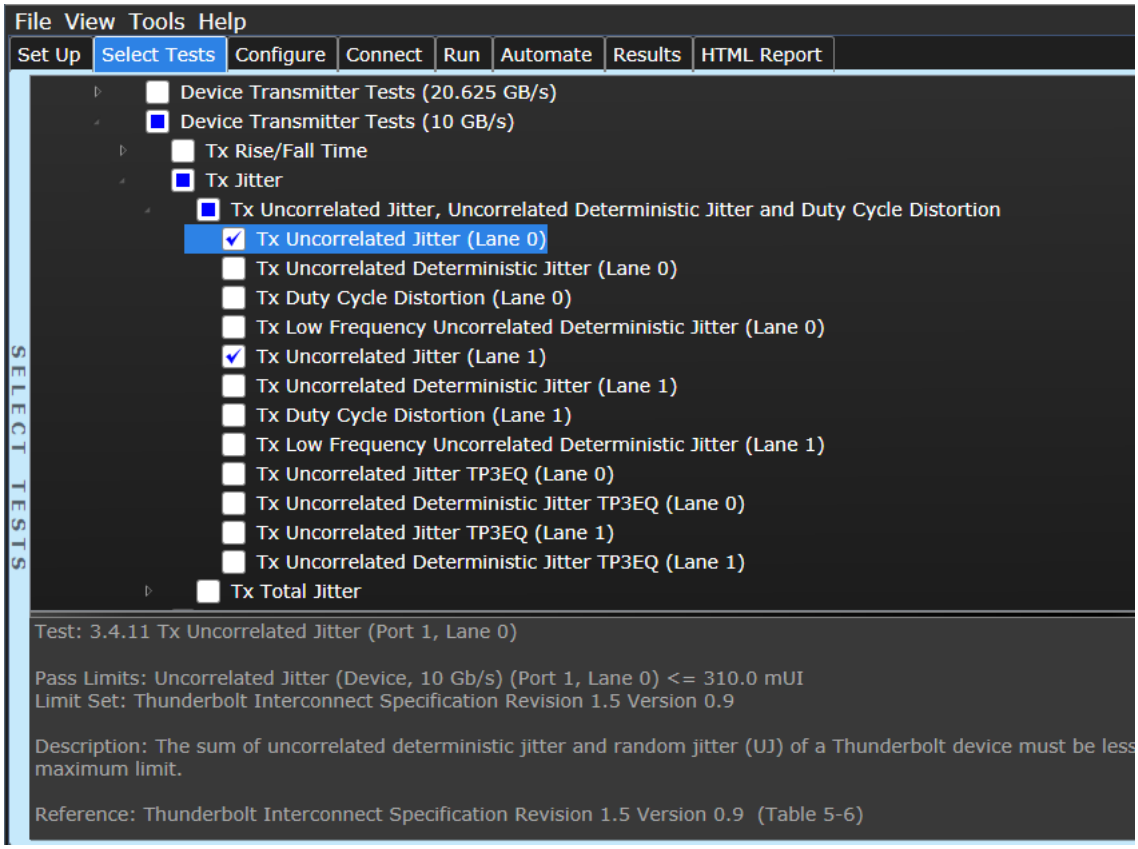


Figure 78 Selecting the Tx Sum of Uncorrelated Jitter tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Perform measurements with:
   - *a* Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   - *b* Oscilloscope with a minimum bandwidth of 16GHz
3. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Pattern length – Periodic
   - *c* Jitter Separation method must be suitable for cross-talk on the signal
   - *d* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *e* Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   - *f* Referenced to 1E-13 statistics
4. Capture the Total Jitter (TJ) and Data Dependent Jitter (DDJ) results.
5. Calculate UJ using the equation:

$$UJ = TJ - DDJ$$

6. Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UJ > 0.31 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.4.11 Gen2 UJ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Uncorrelated Deterministic Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Deterministic Jitter Test is to confirm that the Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Deterministic Jitter (UDJ) $\leq$ 0.17 UI_{p-p} (Refer to Table 6 on page 68).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

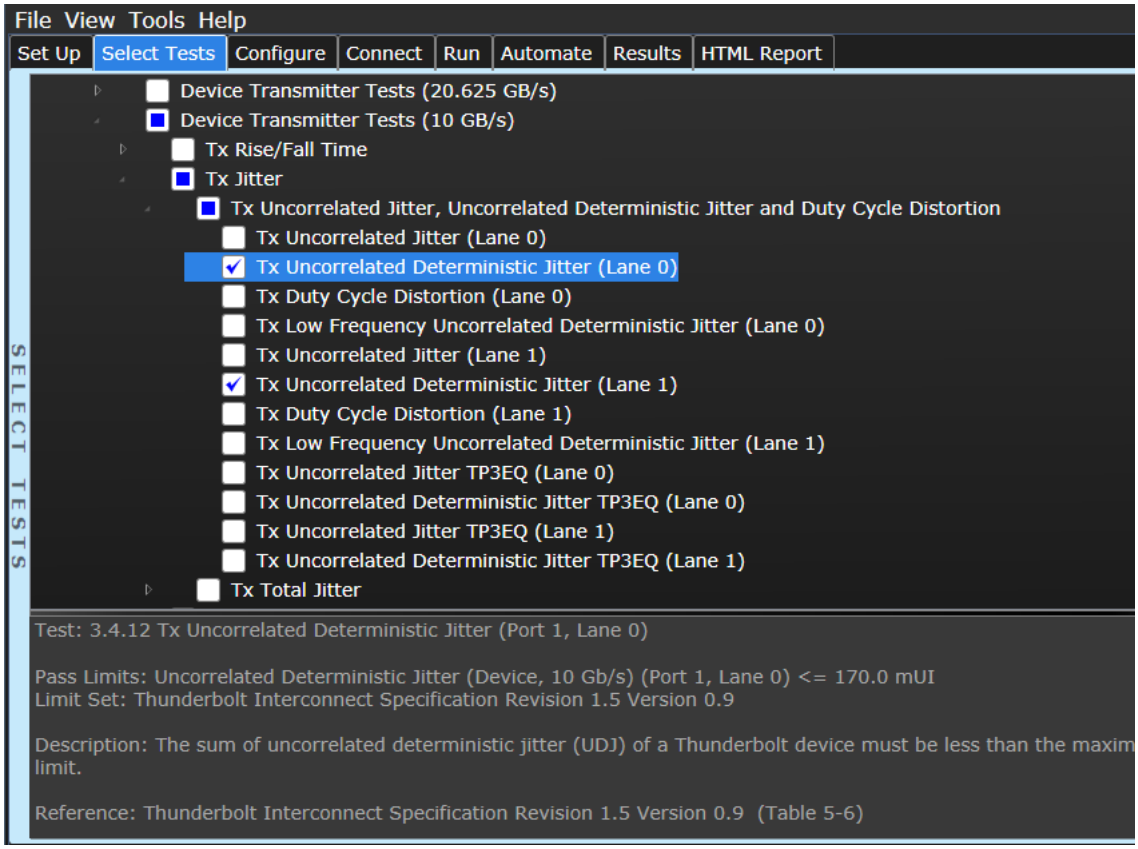


Figure 79 Selecting the Tx Uncorrelated Deterministic Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 16GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   f Referenced to 1E-13 statistics
4 Capture the UDJ result (same as BUJ over the Oscilloscope).
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UDJ > 0.17 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.4.12 Gen2 UDJ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Low Frequency Uncorrelated Deterministic Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Low Frequency Uncorrelated Deterministic Jitter Test is to confirm that the Low Frequency Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Low Frequency Uncorrelated Deterministic Jitter (UDJ_LF) $\leq$ 0.04 UI_{p-p} (Refer to Table 6 on page 68).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

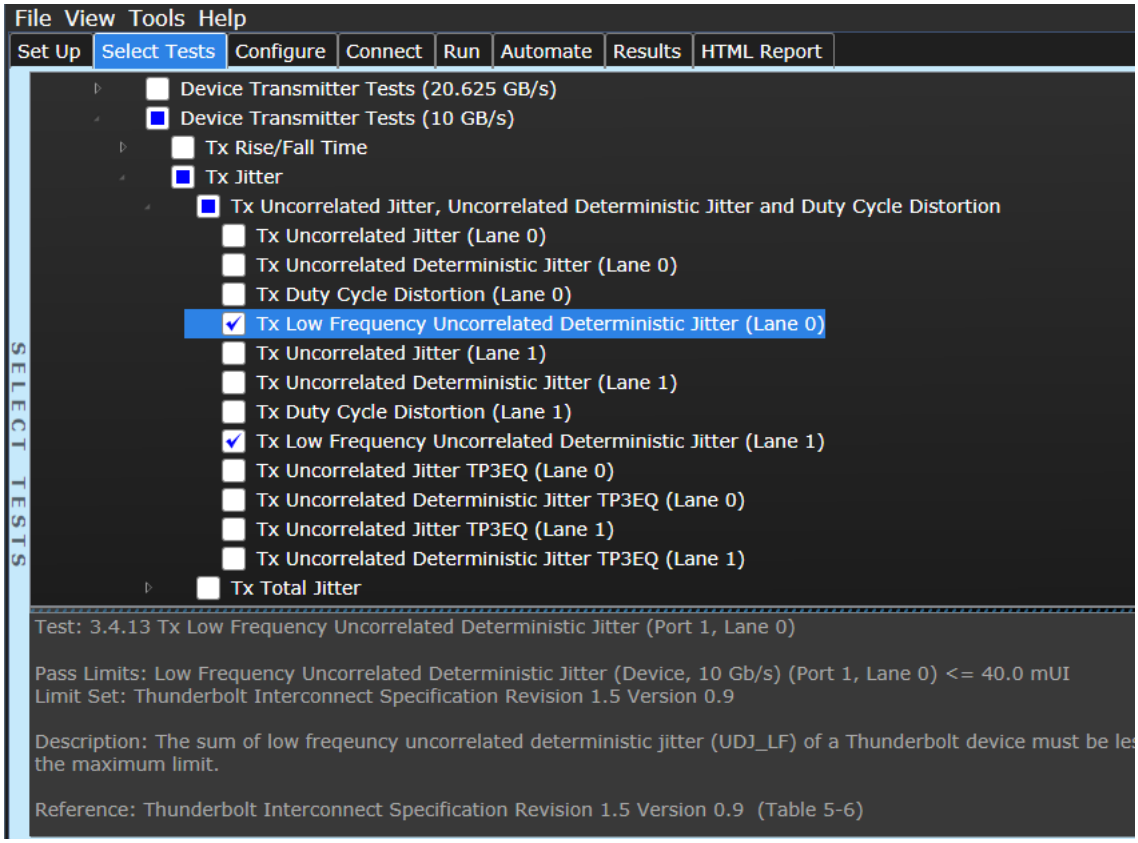


Figure 80 Selecting the Tx Low Frequency Uncorrelated Deterministic Jitter tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Perform measurements with:
   - *a* Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   - *b* Apply 2nd order Low-Pass-Filter with 3 dB cut-off at 2MHz; no average and no interpolation to be used
   - *c* Oscilloscope with a minimum bandwidth of 16GHz
3. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Pattern length – Periodic
   - *c* Jitter Separation method must be suitable for cross-talk on the signal
   - *d* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *e* Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
4. Capture the UDJ_LF result.
5. Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UDJ_LF > 0.04 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.4.13 Gen2 Low Frequency UDJ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Duty Cycle Distortion

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Duty Cycle Distortion Test is to confirm that the transmitter Deterministic Jitter Associated by Duty-Cycle-Distortion Jitter falls within the limits of the specification.

Test Pass Requirement

Duty-Cycle-Distortion (DCD) ≤ 0.03UIp-p (Refer to Table 6 on page 68).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

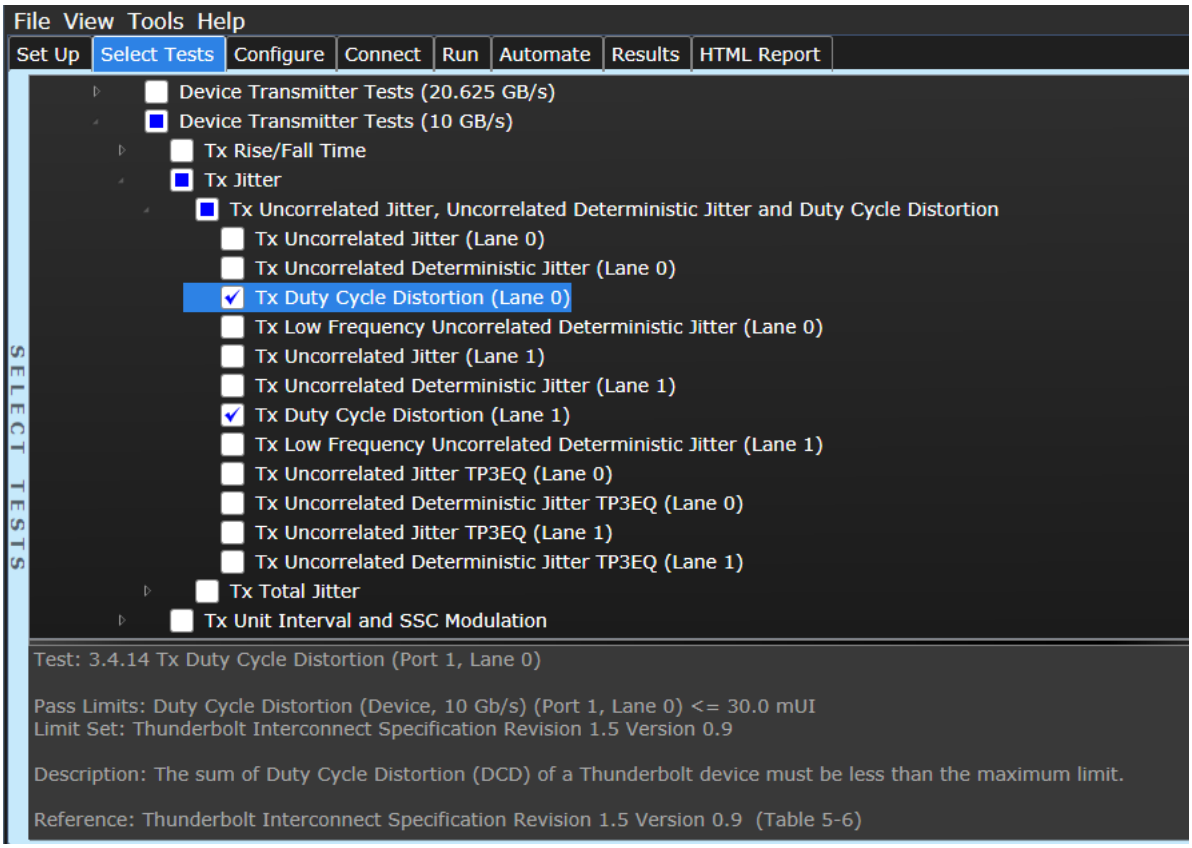


Figure 81 Selecting the Tx Duty Cycle Distortion tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Perform measurements with:
   - *a* Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   - *b* Oscilloscope with a minimum bandwidth of 16GHz
3. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Pattern length – Periodic
   - *c* Jitter Separation method must be suitable for cross-talk on the signal
   - *d* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *e* Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts.
4. Capture the DCD result.
5. Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If DCD > 0.03UIp-p, the status of test is FAIL.

Test References

See

- "Section 3.4.14 Gen2 DCD Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Unit Interval

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Unit Interval Test is to confirm that the data rate, under all conditions, does not exceed the minimum or maximum limits of the specification.

Test Pass Requirement

G2_UI_MIN ≤ Unit Interval ≤ G2_UI_MAX (Refer to Table 6 on page 68).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

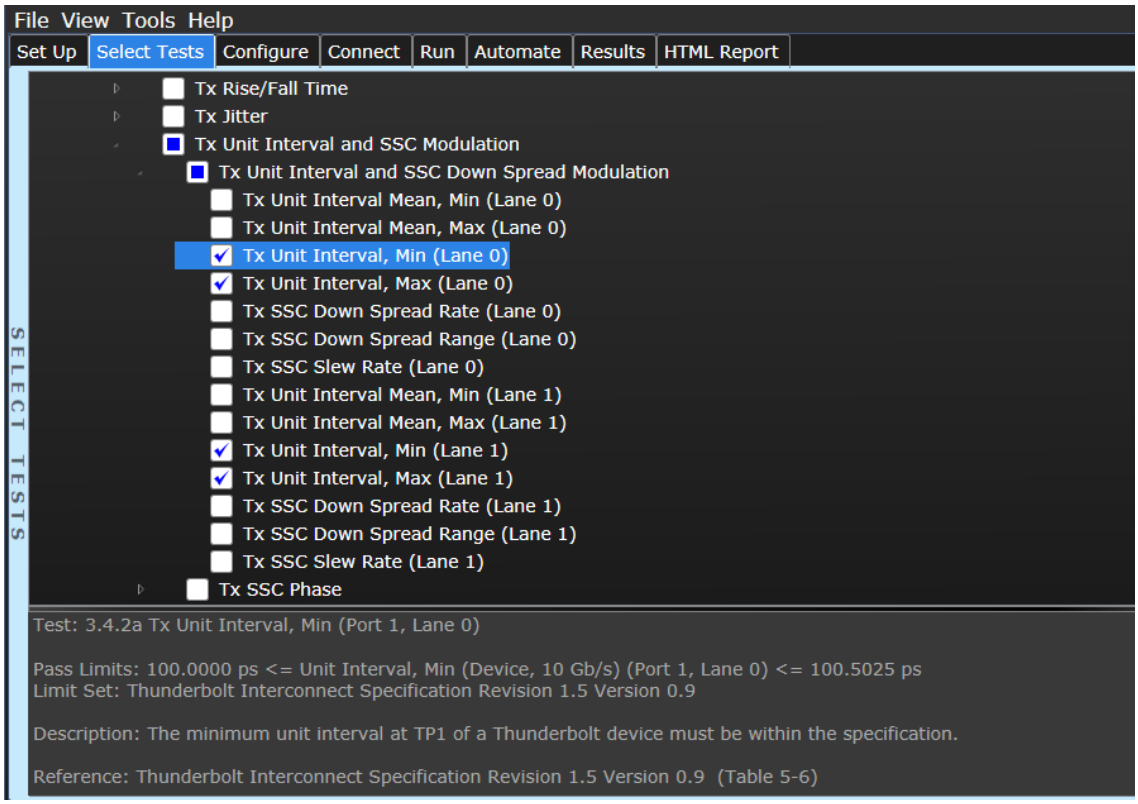


Figure 82 Selecting the Tx Unit Interval tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 16GHz
3 Calculate UI dynamically using a uniform moving average filter procedure with a window size of 3000 symbols.
4 Measure the values of both UI_{MAX} and UI_{MIN}.
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UI_{MAX} > G2_UI_MAX, the status of test is FAIL.

If UI_{MIN} < G2_UI_MIN, the status of test is FAIL.

Test References

See

- "Section 3.4.2 Gen2 Unit Interval Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Unit Interval Mean

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Unit Interval Mean Test is to confirm that the average data rate, under all conditions, does not exceed the minimum or maximum limits of the specification.

Test Pass Requirement

G2_UI_MEAN_MIN ≤ Average Unit Interval ≤ G2_UI_MEAN_MAX (Refer to Table 6 on page 68).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

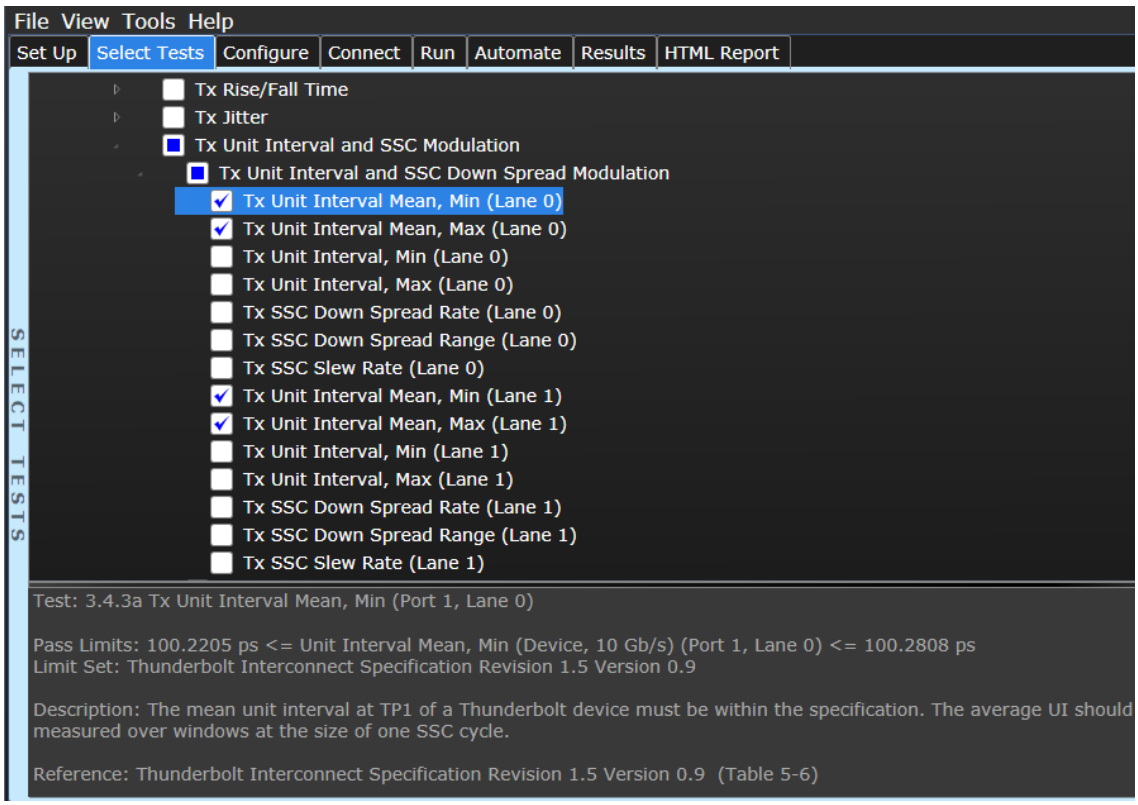


Figure 83 Selecting the Tx Unit Interval Mean tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate ≥ 80 GSa/s

b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts

c No CDR, no average and no interpolation to be used

d Adjust vertical scale such that the signal fits within the Oscilloscope's display

e Oscilloscope must have a minimum bandwidth of 16GHz

3 Use mathematical analysis to measure the average unit interval over a window of the size of one SSC cycle, determined by the SSC_Down_Spread_Rate.

4 Measure UI_MEAN over different windows that uniformly cover the Oscilloscope capture for at least 300ms (more than 10 SSC Cycles) with 10000 UI window jumps. See Figure 84.

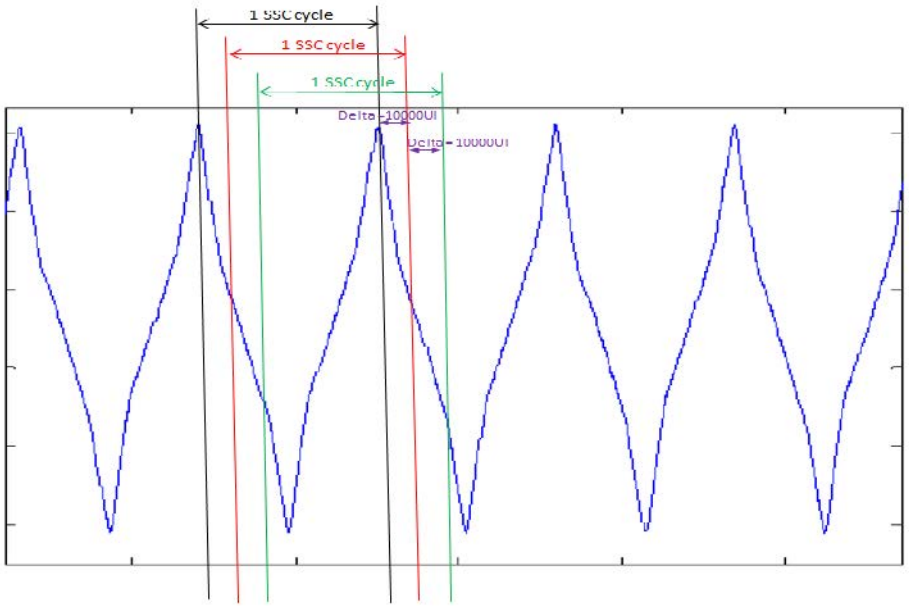


Figure 84 Measurement of UI_MEAN over at least 10 SSC Cycles

5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If the maximum UI_MEAN measured > G2_UI_MEAN_MAX, the status of test is FAIL.

If the minimum UI_MEAN measured < G2_UI_MEAN_MIN, the status of test is FAIL.

Test References

See

- "Section 3.4.3 Gen2 Unit Interval Mean Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx SSC Down Spread Range

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Down Spread Range Test is to confirm that the data down spreading is within the limits of the specification.

Test Pass Requirement

0.4% ≤ SSC_Down_Spread_Range ≤ 0.5% (Refer to Table 4 on page 64).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

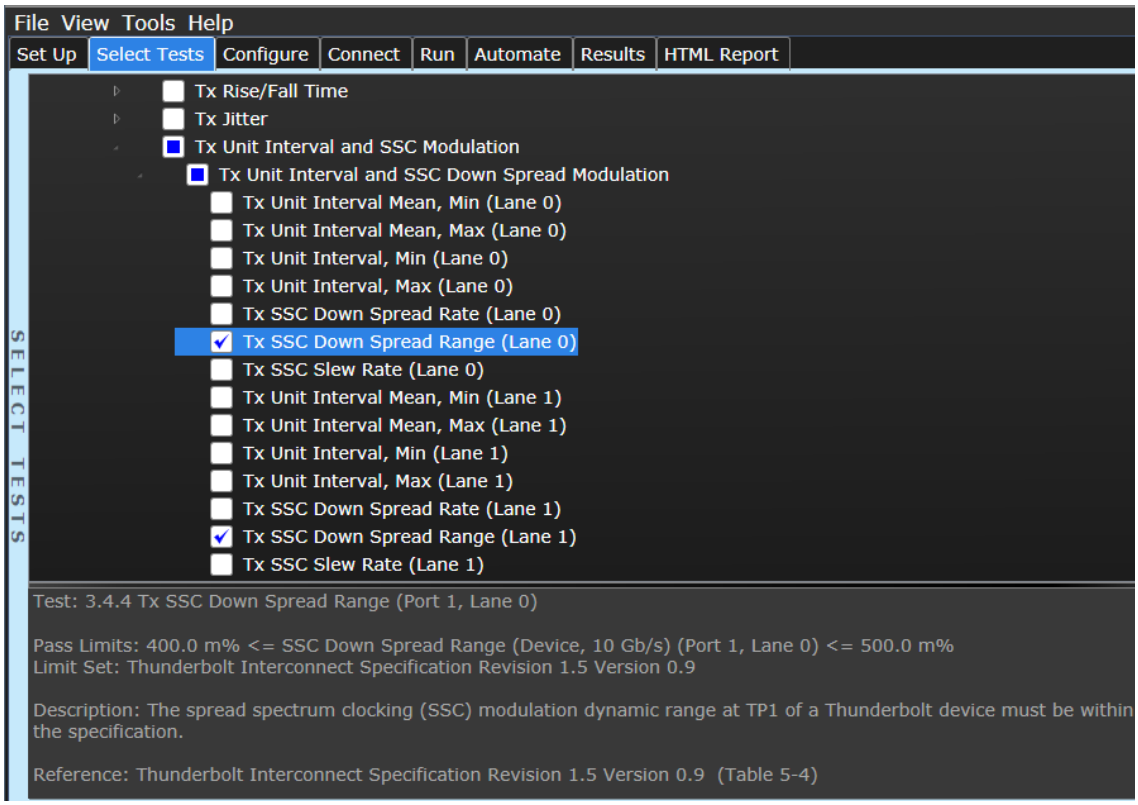


Figure 85 Selecting the Tx SSC Down Spread Range tests

Test Procedure

1 Run the "Tx Unit Interval" Test as a prerequisite to obtain UI_{MAX} and UI_{MIN}.
2 Use the obtained value of UI_{MAX} and UI_{MIN} to calculate the Range percentage:

$$\text{Maximum Deviation} = 100*\{[10G - (1 / UI_{MAX})] / 10G\}$$

$$\text{Minimum Deviation} = 100*\{[10G - (1 / UI_{MIN})] / 10G\}$$

3 Calculate SSC Down Spread Range using the equation:

$$\text{Maximum Deviation - Minimum Deviation}$$

4 Repeat the test for all remaining Thunderbolt lanes.

Expected / Observable Results

If SSC_Down_Spread_Range > 0.5% or SSC_Down_Spread_Range < 0.4%, the status of test is FAIL.

Test References

See

- "Section 3.4.4 Gen2 SSC Down Spread Deviation Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx SSC Down Spread Rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Down Spread Rate Test is to confirm that the Link clock down-spreading modulation rate is within the limits of the specification.

Test Pass Requirement

SSC_DSR_MIN ≤ SSC_Down_Spread_Rate ≤ SSC_DSR_MAX (Refer to Table 4 on page 64).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

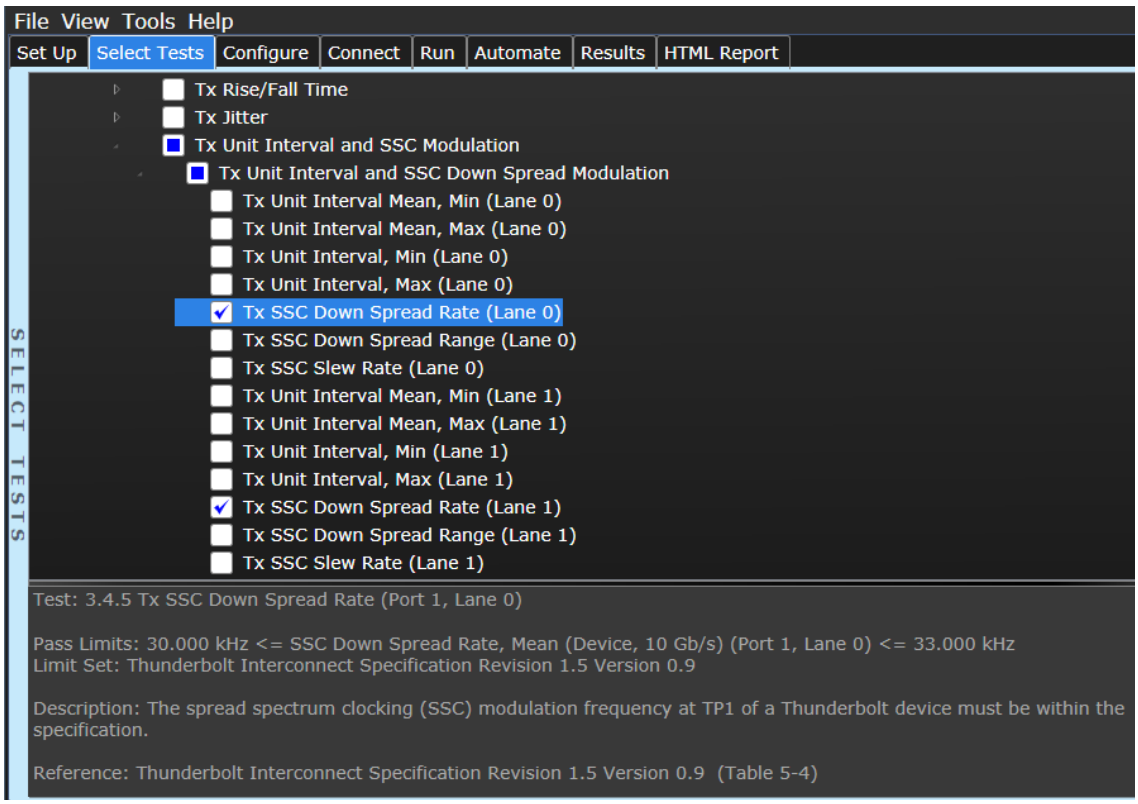


Figure 86 Selecting the Tx SSC Down Spread Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 16GHz
3 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If SSC_DSR_MIN > SSC_Down_Spread_Rate > SSC_DSR_MAX, the status of test is FAIL.

Test References

See

- "Section 3.4.5 Gen2 SSC Down Spread Rate Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx SSC Phase Deviation

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Phase Deviation Test is to confirm that the SSC Phase Deviation is within the limits of the specification.

Test Pass Requirement

2.5ns p-p ≤ SSC_Phase_Deviation ≤ SSC_PD_MAX (Refer to Table 4 on page 64).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx SSC Phase* are checked.

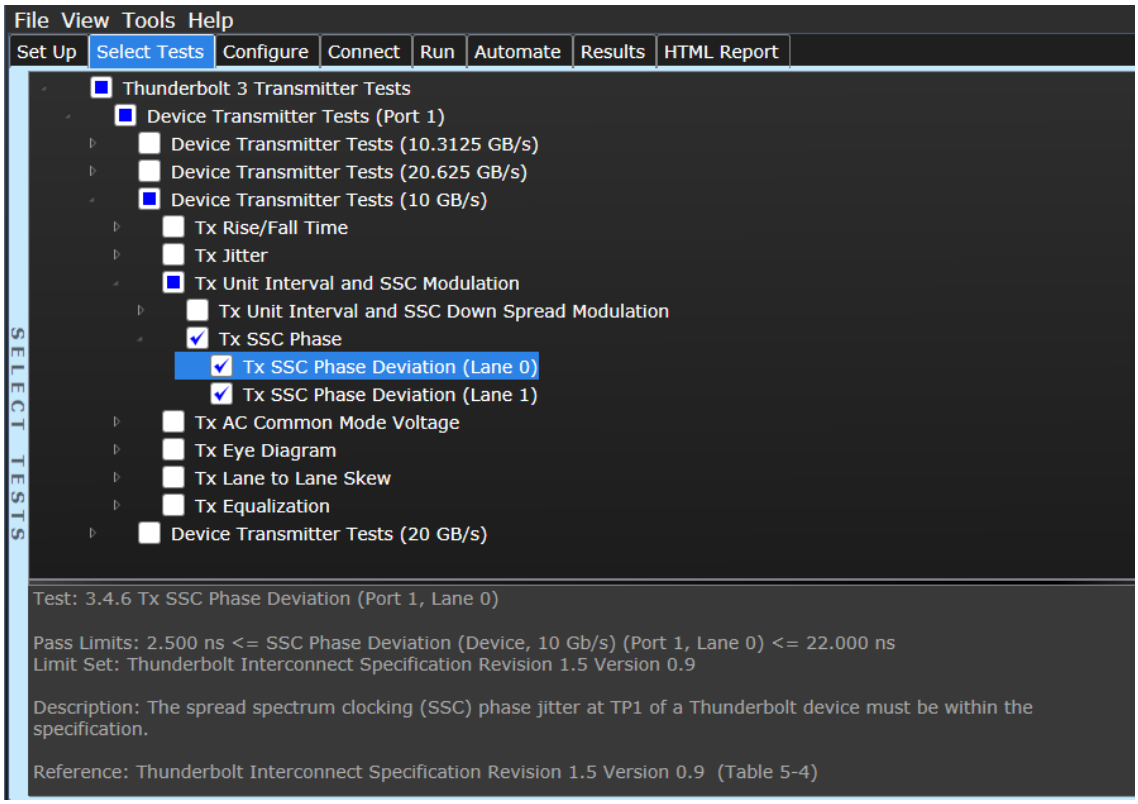


Figure 87 Selecting the Tx SSC Phase Deviation tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope's software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 16GHz
3 Extract the SSC Phase Deviation from the transmitted signal.
4 Extract the SSC Phase Deviation from the phase jitter after applying a 2^{nd} order low-pass filter with 3dB point at 2 MHz.
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If 2.5ns p-p > SSC_Phase_Deviation > SSC_PD_MAX the status of test is FAIL.

Test References

See

- "Section 3.4.6 Gen2 SSC Phase Deviation Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx SSC Slew Rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Slew Rate Test is to confirm that the SSC Slew Rate is within the limits of the specification.

Test Pass Requirement

SSC_Slew_Rate ≤ 1000 ppm/µs (Refer to Table 4 on page 64).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

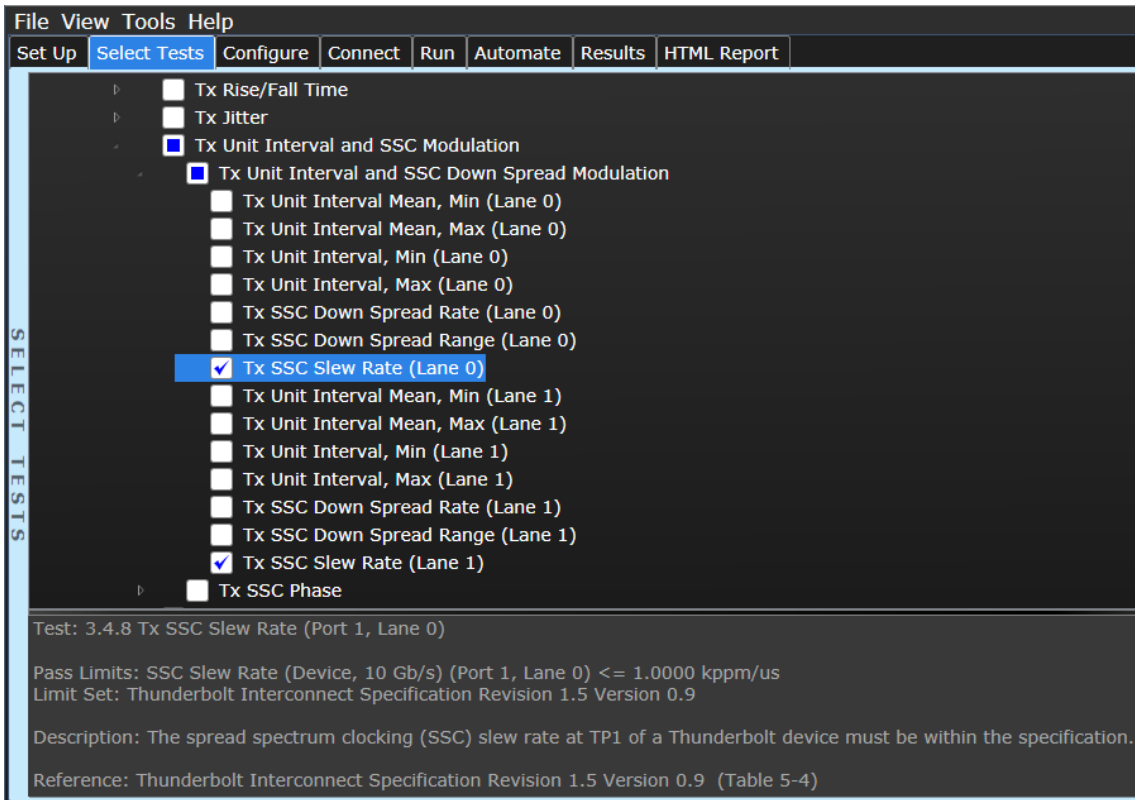


Figure 88 Selecting the Tx SSC Slew Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and post process it with an appropriate software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Extract SSC slew rate from the transmitted signal over measurement intervals of 0.5µs
   f Extract SSC slew rate from the phase information after applying a 2nd order Low-Pass-Filter with 3 dB cut-off at 2MHz.
   g Oscilloscope must have a minimum bandwidth of 16GHz
3 SSC_Slew_Rate is measured as the SSC frequency deviation over time while valid data is being transmitted in which 1E-12 bit error rate is required without assuming forward error correction.
4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If SSC_Slew_Rate > 1000 ppm/µs, the status of test is FAIL.

Test References

See

- "Section 3.4.7 Gen2 SSC Slew Rate Data Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Lane to Lane Skew

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Lane to Lane Skew Test is to confirm that the Skew between dual transmit signals of the same port group falls within the limits of the specification.

Test Pass Requirement

Lane_to_Lane_Skew ≤ 26nS (Refer to Table 4 on page 64).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Lane to Lane Skew* are checked.

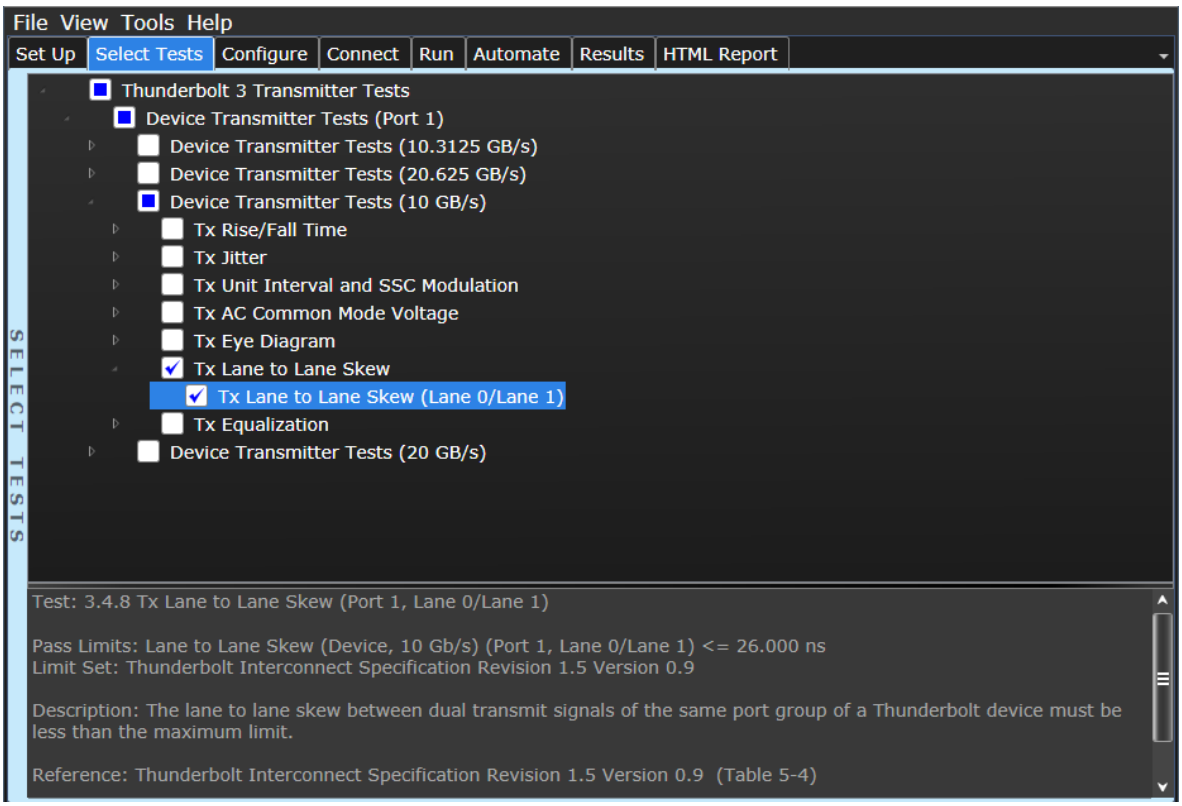


Figure 89 Selecting the Tx Lane to Lane Skew tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveforms from 2 lanes from the same port together and post process it with an appropriate software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 10Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 10Mpts.
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Measurement must be performed between consecutive rising edges
   f Oscilloscope must have a minimum bandwidth of 16GHz
3 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If Lane_to_Lane_Skew > 26nS, the status of test is FAIL.

Test References

See

- "Section 3.4.8 Gen2 Lane to Lane Skew Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Eye Diagram

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Eye Diagram Test is to confirm that the differential signal on each Thunderbolt differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram should meet the conditions depicted in Figure 90.

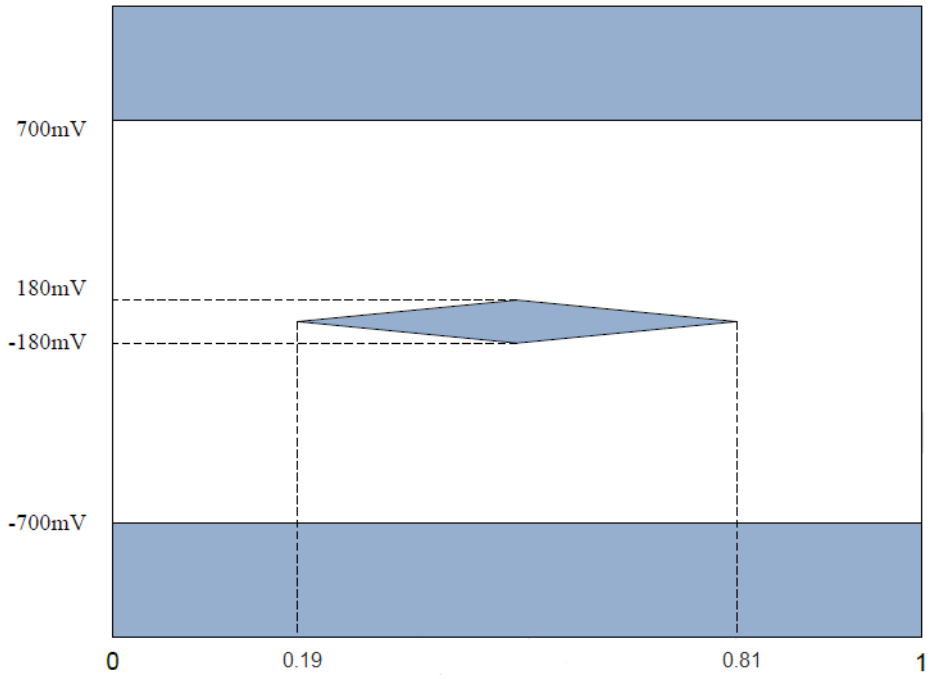


Figure 90 Pass Condition for Tx Eye Diagram Tests

(Refer to Table 6 on page 68 and Figure 41 on page 70).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Eye Diagram* are checked.

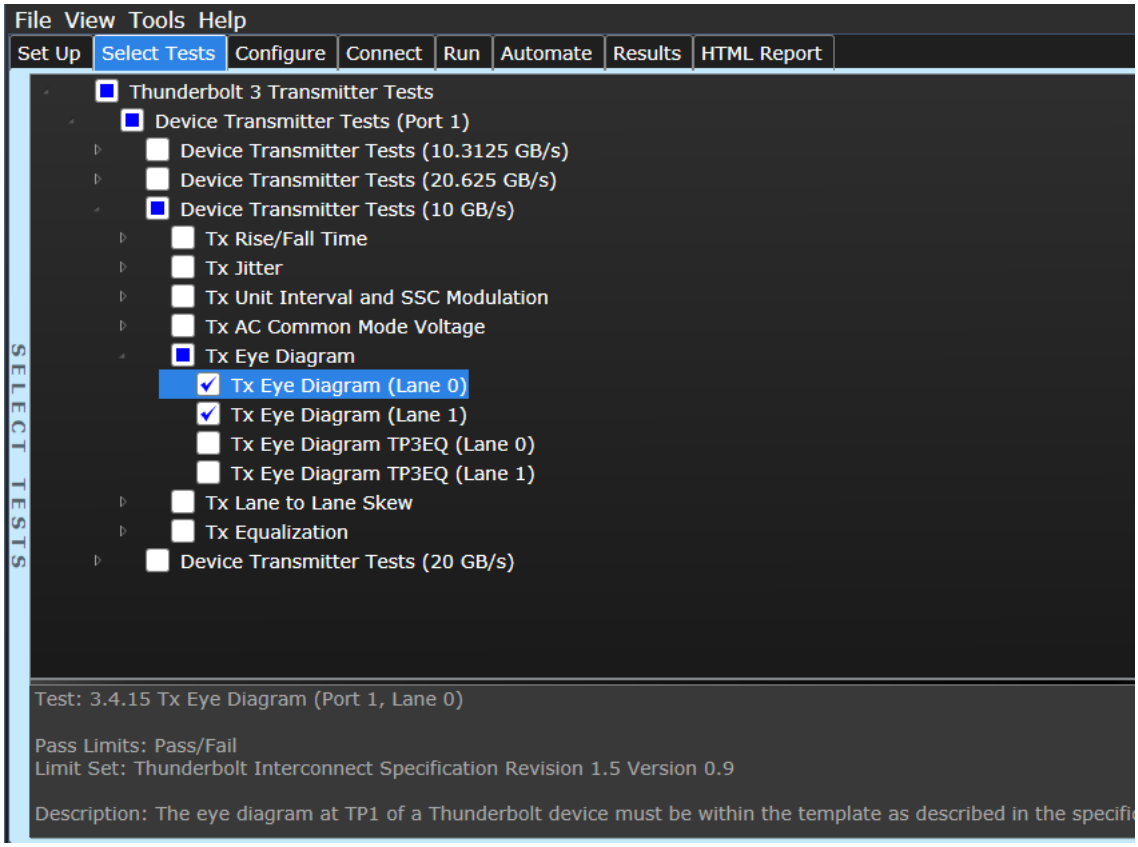


Figure 91 Selecting the Tx Eye Diagram tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Perform measurements with:

a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used

b Oscilloscope with a minimum bandwidth of 16GHz

3 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate $\geq$ 80 GSa/s

b Adjust vertical scale such that the signal fits within the Oscilloscope's display

c Measured at 1E6 UI

4 Compare the data eye to the TP1 eye diagram mask. Check for conditions described in the section "Expected / Observable Results".

5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the inner or outer height voltage (+/- 700mV), the status of the test is FAIL.

ii If any part of the waveform hits the mask, the status of the test is FAIL.

Test References

See

- "Section 3.4.16 Gen2 Eye Diagram Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-6 and Figure 5-15 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx AC Common Mode Voltage

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx AC Common Mode Voltage Test is to confirm that the transmitter common mode on the Thunderbolt differential signals is within the limits of the specification.

Test Pass Requirement

TX AC Common Mode Voltage $\leq 100mV_{p-p}$ (Refer to Table 6 on page 68).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx AC Common Mode Voltage* are checked.

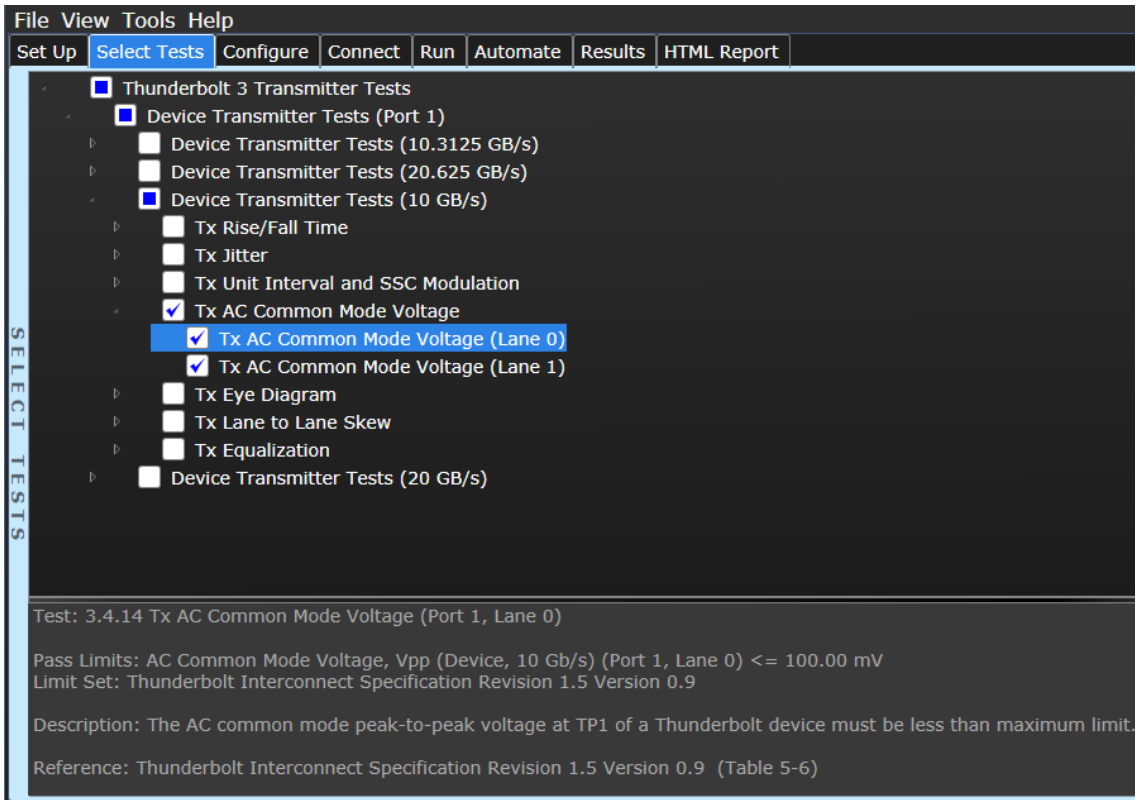


Figure 92 Selecting the Tx AC Common Mode Voltage tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Oscilloscope must have a minimum bandwidth of 16GHz
3 Calculate the AC Common Mode Voltage (V_{AC-CM}) using the equation:

$$V_{AC-CM} = (V_{TX-P} + V_{TX-N}) / 2$$

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $V_{AC-CM} > 100mV_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.4.15 Gen2 AC Common Mode Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Total Jitter TP3EQ

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Total Jitter TP3EQ Test is to confirm that the Total Jitter at point TP3EQ of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of $1x10^{-13}$.

Test Pass Requirement

Total Jitter (TJ_{TP3EQ}) $\leq$ 0.60 UI_{p-p} (Refer to Table 7 on page 69).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Total Jitter* are checked.

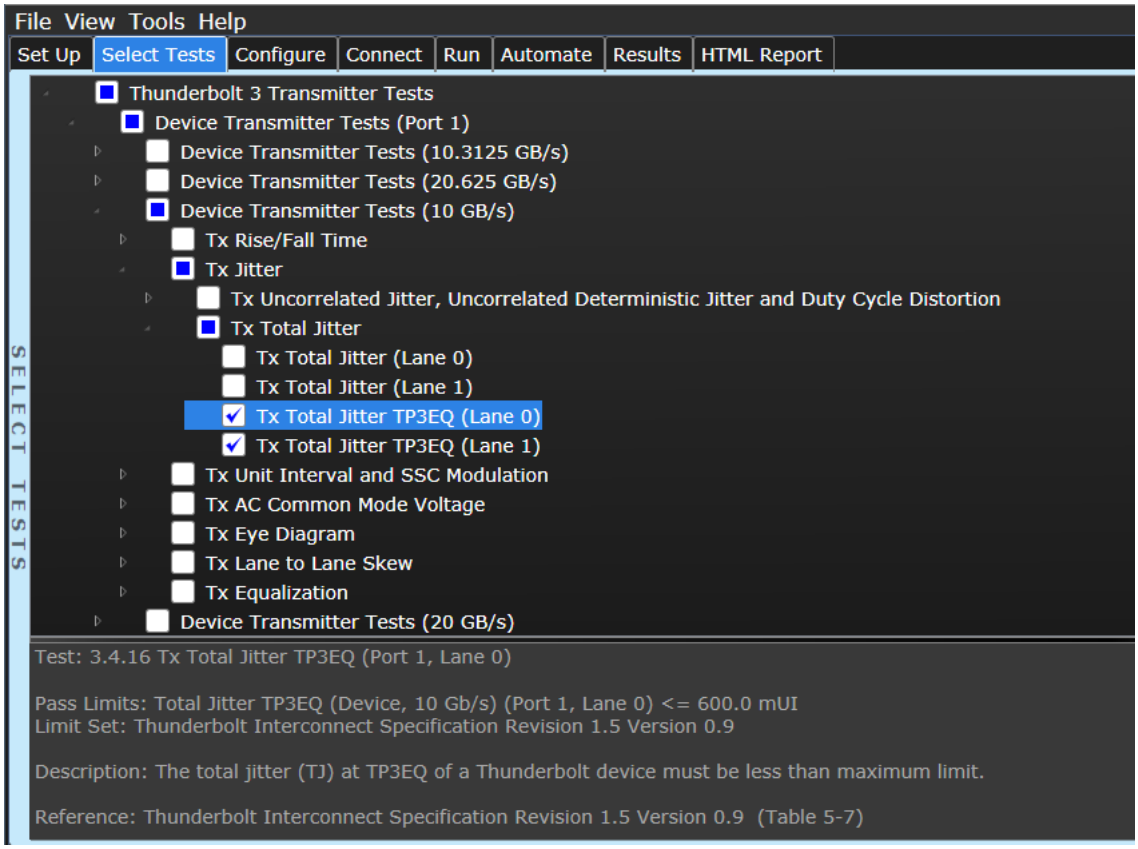


Figure 93 Selecting the Tx Total Jitter TP3EQ tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.

2 Embed the Type-C cable in the Oscilloscope. For Gen 2 systems, use TP3_EQ embedding file *TBT_2m.s4p*.

3 De-embed the cables from the test fixture to the Oscilloscope.

4 Ensure that measurements are done with a calibrated reference equalizer (CTLE only). See "Tx CTLE Calibration" on page 140.

5 Perform measurements with:

a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used

b Oscilloscope with a minimum bandwidth of 16GHz

6 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate $\geq$ 80 GSa/s

b Pattern length – Periodic

c Jitter Separation method must be suitable for cross-talk on the signal

d Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts

e Adjust vertical scale such that the signal fits within the Oscilloscope's display

f Referenced to 1E-13 statistics

7 Capture the values of Total Jitter (TJ_{TP3EQ}) and Deterministic Jitter (DJ_{TP3EQ}).

8 If $TJ_{TP3EQ} > 0.60\ UI_{p-p}$, perform the following steps:

a Configure the DUT transmitter to output alternating square pattern of one 0's and one 1's on all lanes with SSC enabled. (The pattern is SQ2 instead of PRBS15).

b Perform measurements with:

- Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
- Oscilloscope with a minimum bandwidth of 16GHz

c Capture the waveform and process it with the Digital Oscilloscope:

- Sampling Rate $\geq$ 80 GSa/s
- Pattern length – Periodic
- Jitter Separation method must be suitable for cross-talk on the signal
- Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
- Adjust vertical scale such that the signal fits within the Oscilloscope's display.
- Referenced to 1E-13 statistics.

d Capture the Random Jitter (RJ_{TP3EQ}) result.

e Calculate TJ_{TP3EQ} using the equation:

$TJ_{TP3EQ} = DJ_{TP3EQ} + 14.7 * RJ_{TP3EQ}$ (DJ_{TP3EQ} from #7; PRBS15 and RJ_{TP3EQ} from #8d; SQ2)

9 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $TJ_{TP3EQ} > 0.60\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.4.17 Gen2 Total Jitter TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-7 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Uncorrelated Jitter TP3EQ

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Jitter TP3EQ Test is to confirm that the Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] at point TP3EQ of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Jitter (UJ_{TP3EQ}) $\leq$ 0.31 UI_{p-p} (Refer to Table 7 on page 69).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

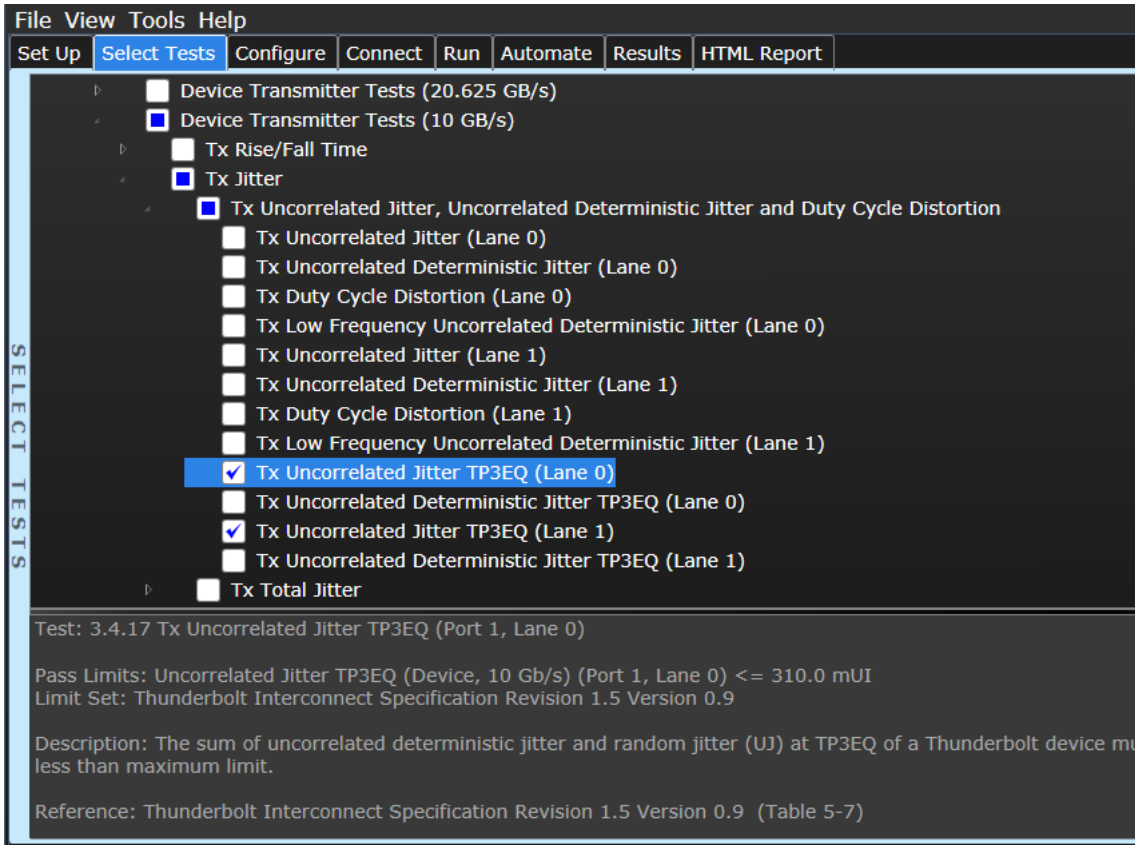


Figure 94 Selecting the Tx Uncorrelated Jitter TP3EQ tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Embed the Type-C cable in the Oscilloscope. For Gen 2 systems, use TP3_EQ embedding file *TBT_2m.s4p*.
3. De-embed the cables from the test fixture to the Oscilloscope.
4. Ensure that measurements are done with a calibrated reference equalizer (CTLE only). See "Tx CTLE Calibration" on page 140.
5. Perform measurements with:
   - *a* Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   - *b* Oscilloscope with a minimum bandwidth of 16GHz
6. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Pattern length – Periodic
   - *c* Jitter Separation method must be suitable for cross-talk on the signal
   - *d* Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   - *e* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *f* Referenced to 1E-13 statistics

7 Capture the values of Total Jitter (TJ_{TP3EQ}) and Data Deterministic Jitter (DDJ_{TP3EQ}).

8 Calculate UJ_{TP3EQ} using the equation:

$$UJ_{TP3EQ} = TJ_{TP3EQ} - DDJ_{TP3EQ}$$

9 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $UJ_{TP3EQ} > 0.31\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.4.18 Gen2 UJ TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-7 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Uncorrelated Deterministic Jitter TP3EQ

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Deterministic Jitter TP3EQ Test is to confirm that the Uncorrelated Deterministic Jitter at point TP3EQ of the transmitter is within the limits of the specification.

Test Pass Requirement

Deterministic Jitter that is uncorrelated to the transmitted data (UDJ_{TP3EQ}) ≤ 0.17 UI_{p-p} (Refer to Table 7 on page 69).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

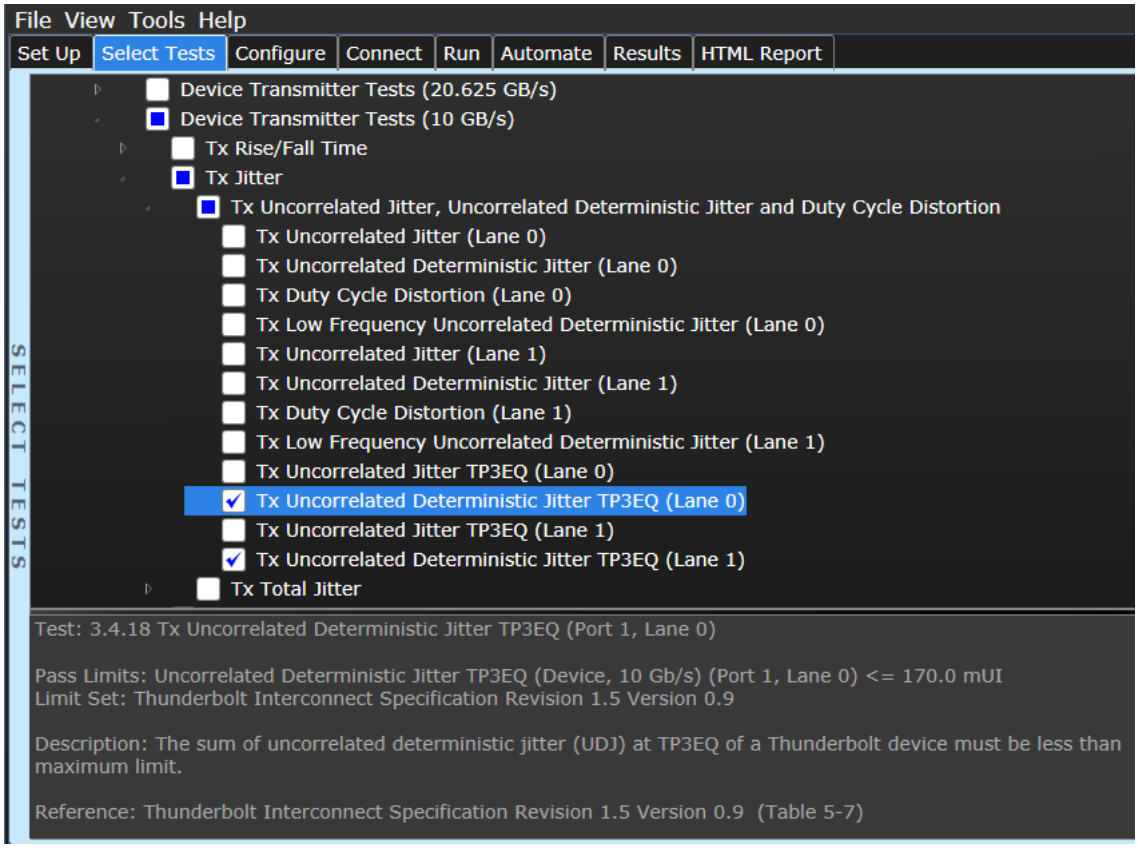


Figure 95 Selecting the Tx Uncorrelated Deterministic Jitter TP3EQ tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Embed the Type-C cable in the Oscilloscope. For Gen 2 systems, use TP3_EQ embedding file *TBT_2m.s4p*.
3 De-embed the cables from the test fixture to the Oscilloscope.
4 Ensure that measurements are done with a calibrated reference equalizer (CTLE only). See "Tx CTLE Calibration" on page 140.
5 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 16GHz
6 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display
7 Capture the values of Total Jitter (TJ_{TP3EQ}) and Data Deterministic Jitter (DDJ_{TP3EQ}).

8 Capture the UDJ_{TP3EQ} result (same as BUJ over the Oscilloscope).

9 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $UDJ_{TP3EQ} > 0.17\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.4.19 Gen2 UDJ TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-7 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Eye Diagram TP3EQ

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Eye Diagram TP3EQ Test is to confirm that the differential signal on each Thunderbolt differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram at TP3EQ should meet the conditions depicted in Figure 96.

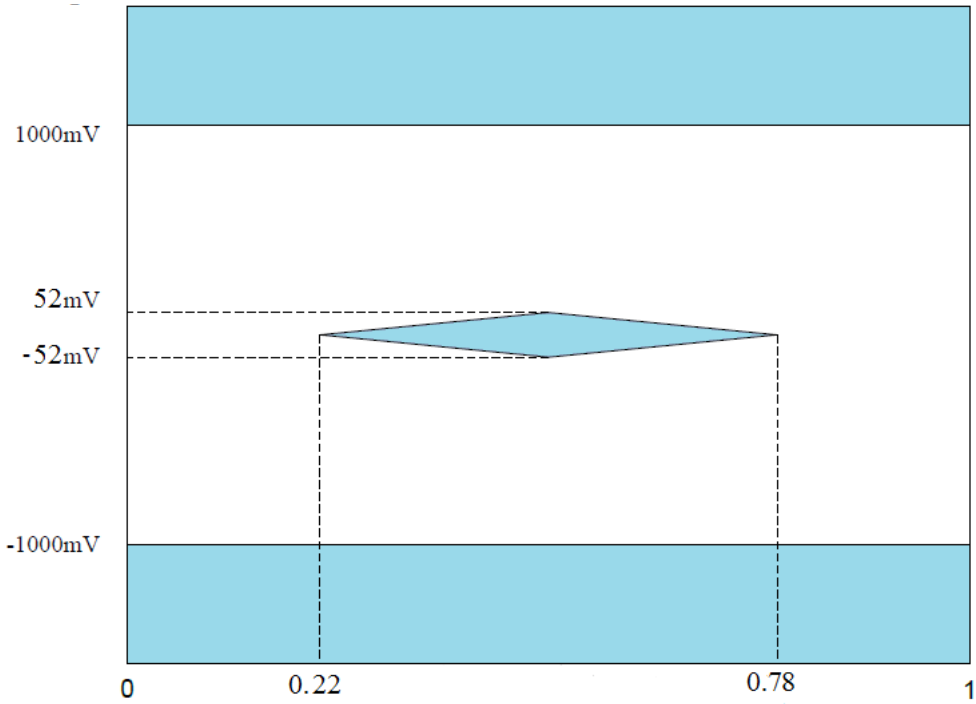


Figure 96 Pass Condition for Tx Eye Diagram TP3EQ Tests

(Refer to Table 7 on page 69 and Figure 41 on page 70).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Eye Diagram* are checked.

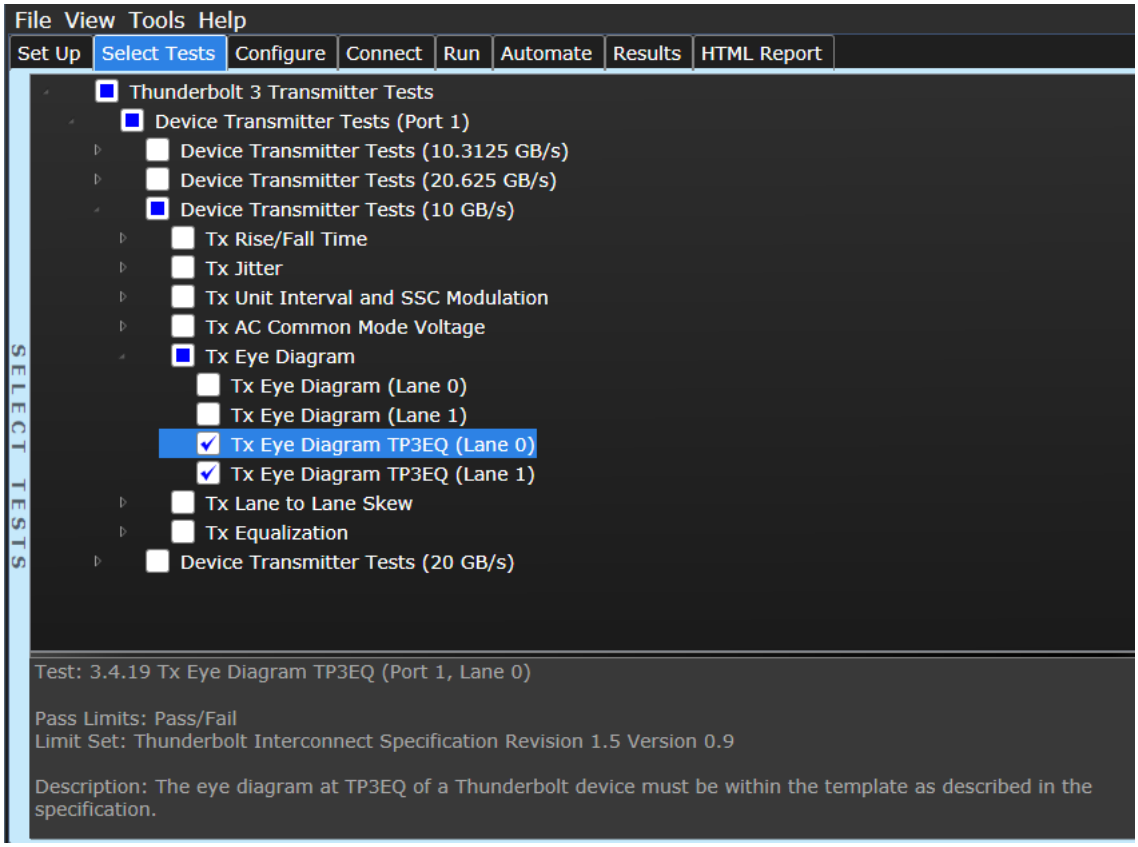


Figure 97 Selecting the Tx Eye Diagram TP3EQ tests

Test Procedure

1. Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2. Embed the Type-C cable in the Oscilloscope. For Gen 2 systems, use TP3_EQ embedding file *TBT_2m.s4p*.
3. De-embed the cables from the test fixture to the Oscilloscope.
4. Ensure that measurements are done with a calibrated reference equalizer (CTLE and DFE). See "Tx CTLE Calibration" on page 140.
5. Perform measurements with:
   - *a* Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   - *b* Oscilloscope with a minimum bandwidth of 16GHz
6. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Adjust vertical and horizontal scale such that the signal fits within the Oscilloscope's display
   - *c* Accumulate at 1E6 UI
7. Compare the data eye to the TP3EQ eye diagram mask. Check for conditions described in the section "Expected / Observable Results".
8. Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the high or low maximum voltage (+/-1000mV), the status of the test is FAIL.

ii If any part of the waveform hits the mask, the status of the test is FAIL.

Test References

See

- "Section 3.4.20 Gen2 Eye Diagram Measurement TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-7 and Figure 5-15 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Equalization Tests

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Equalization Tests is to confirm that the transmitter equalization is within the limits of the specification. The Tx Equalization Tests are further divided into three tests, namely:

- Tx Equalization Pre-shoot
- Tx Equalization Deemphasis
- Tx Swing Preset 15

Test Pass Requirement

Transmitter Swing: 3.5 ± 1dB (for preset 15 only)

Pre-shoot, De-Emphasis: ± 1dB for the following presets:

Table 12 Transmitter Equalization Presets

Preset Number	Pre-Shoot	De-Emphasis
0	0	0
1	0	-1.9
2	0	-3.6
3	0	-5.0
4	0	-8.4
5	0.9	0
6	1.1	-1.9
7	1.4	-3.8
8	1.7	-5.8
9	2.1	-8.0
10	1.7	0
11	2.2	-2.2
12	2.5	-3.6
13	3.4	-6.7
14	4.3	-9.3
15	1.7	-1.7

(Refer to Table 5 on page 66).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Equalization* are checked.

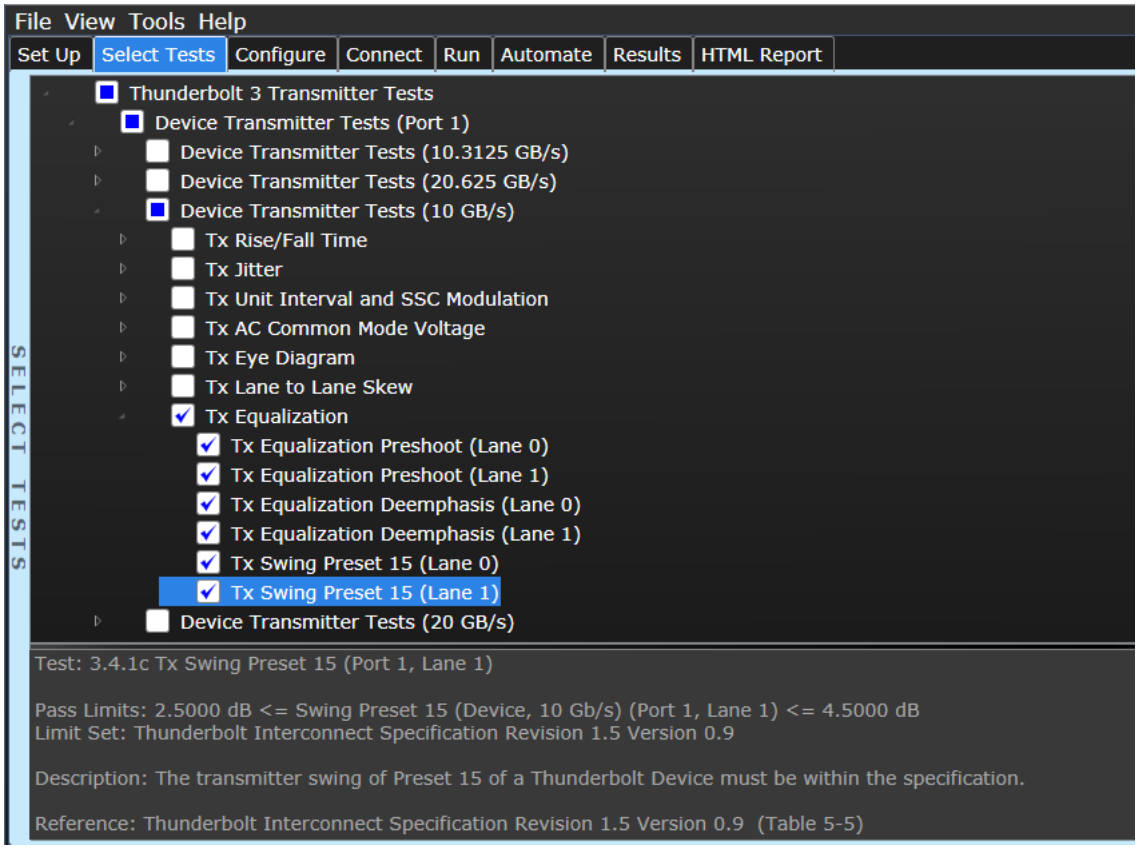


Figure 98 Selecting the Tx Equalization tests

4 Under the **Configure** tab of the Test Application, select **ALL** for the Configuration Variable “Tx Equalization” to run the tests for preset numbers P0 to P15.

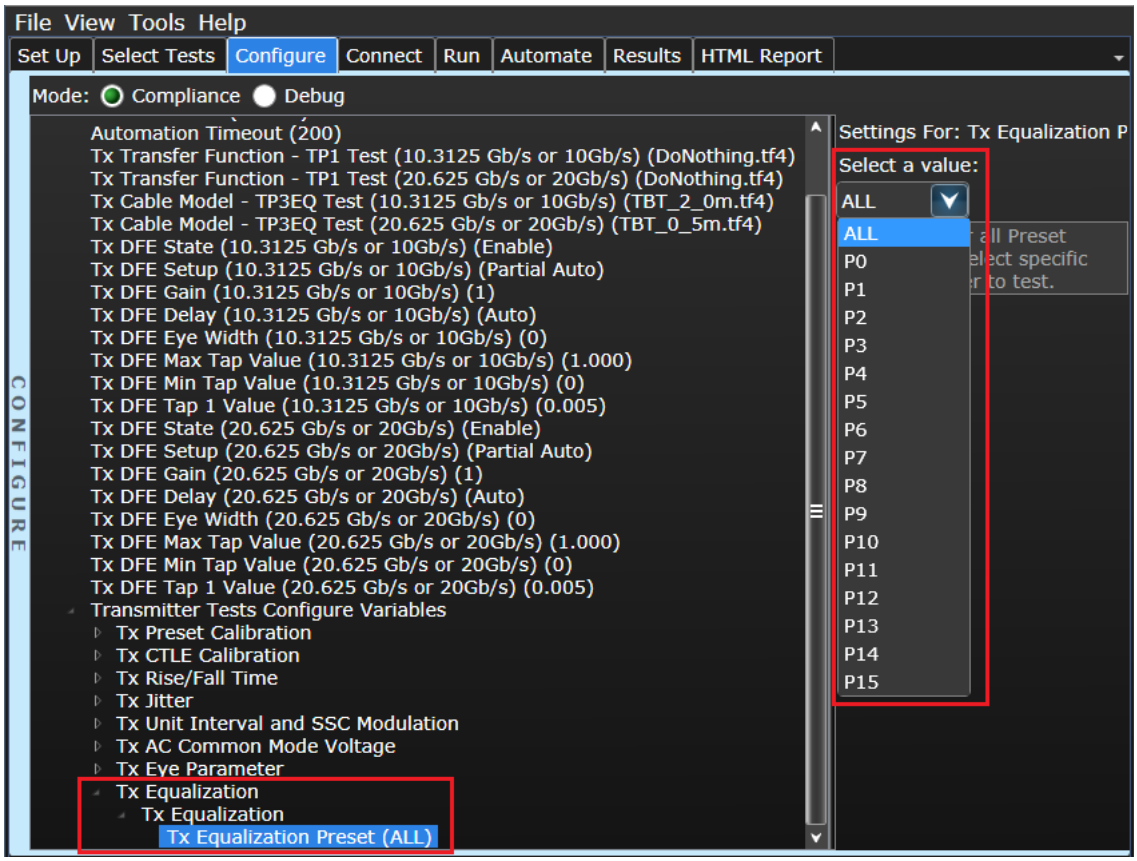


Figure 99 Configuring Tx Equalization Preset Variable

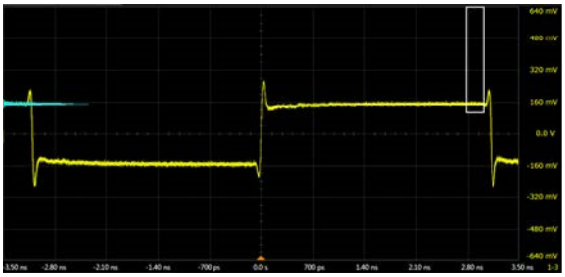
Test Procedure

1 Set Preset 0 (P0).

2 Configure the DUT transmitter to output alternating square pattern of 64 0’s and 64 1’s on all lanes with SSC enabled along with both pre-shoot and de-emphasis enabled.

3 Adjust vertical scale such that the signal fits within the Oscilloscope’s display.

4 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



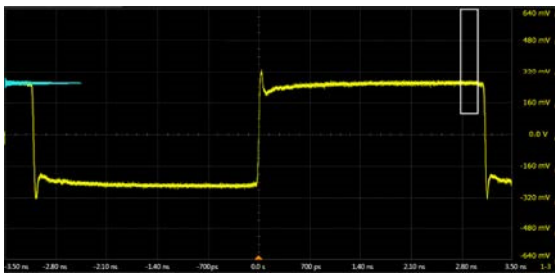
5 Measure differential amplitude voltage (V_1) for bits 57 to 62 using the equation:

$$V_1 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

6 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with de-emphasis enabled but no pre-shoot.

7 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

8 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



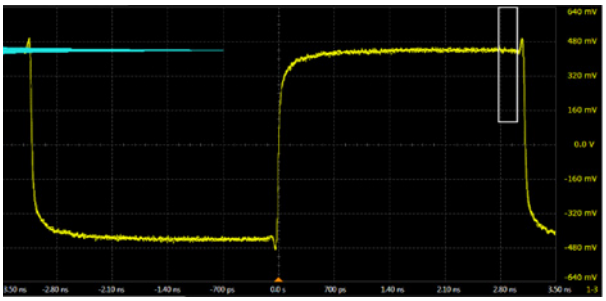
9 Measure differential amplitude voltage (V_2) for bits 57 to 62 using the equation:

$$V_2 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

10 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with pre-shoot enabled but no de-emphasis.

11 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

12 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



13 Measure differential amplitude voltage (V_3) for bits 57 to 62 using the equation:

$$V_3 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

$$\text{Set Pre-Shoot to be } 20 * \log_{10} [V_2/V_1]$$

$$\text{Set De-Emphasis to be } 20 * \log_{10} [V_1/V_3]$$

14 Repeat steps 2 to 10 for all Presets defined in Table 12.

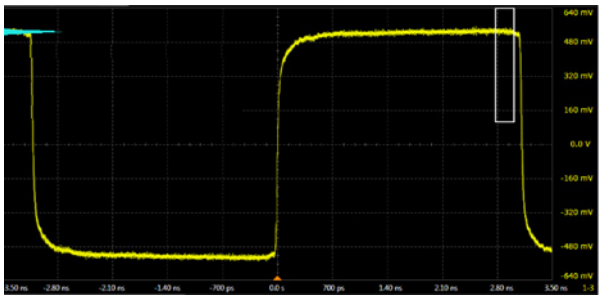
15 Check for PASS/FAIL conditions for both Pre-shoot and De-emphasis.

16 Set the DUT to Preset 0 (P0).

17 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

18 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

19 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



20 Measure differential amplitude voltage (V_0) for bits 57 to 62 using the equation:

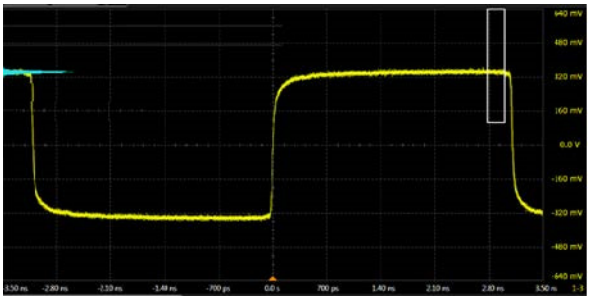
$$V_0 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

21 Set the DUT to Preset 15 (P15).

22 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

23 Adjust vertical scale such that the signal fits within the Oscilloscope's display

24 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



25 Measure differential amplitude voltage (V_{15}) for bits 57 to 62 using the equation:

$$V_{15} = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

Set Swing to be $20 * \log_{10} [V_0/V_{15}]$

26 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If the Pre-Shoot for a particular Preset number is not within ± 1dB of the matching value in Table 12, the status of test is FAIL.

If the De-Emphasis for a particular Preset number is not within ± 1dB of the matching value in Table 12, the status of test is FAIL.

If Swing < 2.5 dB or Swing > 4.5 dB, the status of test is FAIL.

Test References

See

- "Section 3.4.1 Gen2 Transmitter Equalization" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-5 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

7 Transmitter Tests for 20.625 GB/s Systems

This section provides the Methods of Implementation (MOIs) to run electrical tests on a Thunderbolt DUT operating at a bit rate of 20.625 GB/s using an Keysight Infiniium Oscilloscope and other accessories, along with the Keysight D9030TBTC Thunderbolt 3 Test Application.

NOTE **All Thunderbolt 3 devices that support a bit rate of 20.625 Gb/s are classified as Gen3 devices.**

Tx Preset Calibration

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Preset Calibration Test is to find the optimized preset for the platform.

NOTE Prior to running the compliance tests, the Host / Device must go through Preset Calibration.

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Preset Calibration* are checked.

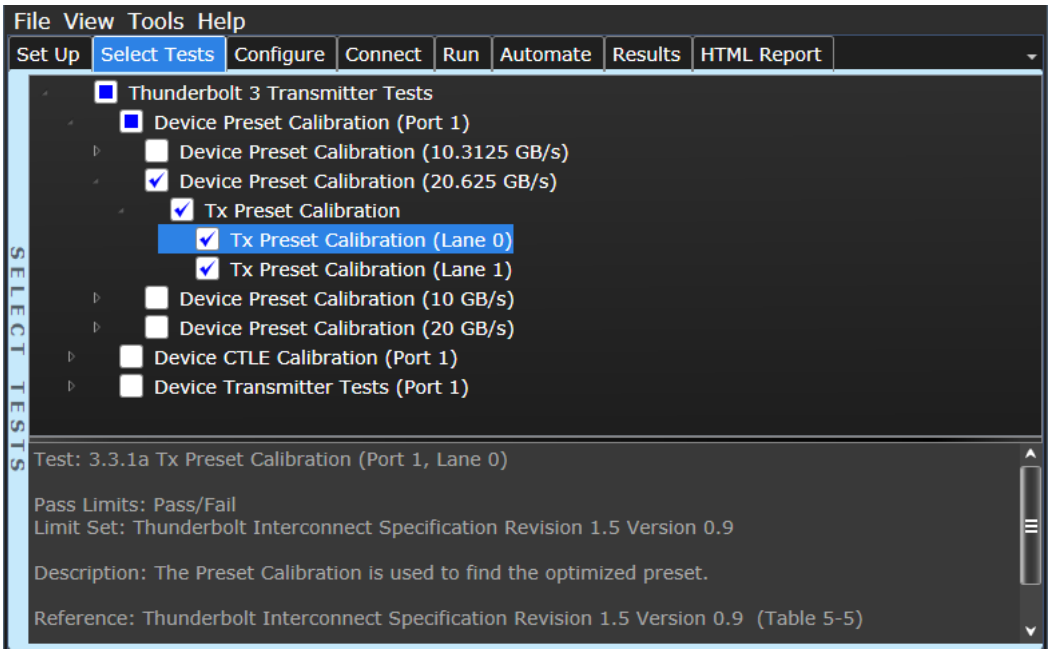


Figure 100 Selecting the Tx Preset Calibration tests

NOTE By default, the test group for **Preset Calibration** for each selected bit-rate is hidden in the **Select Tests** tab when **Predefined Optimum Preset Number** is selected for the respective bit-rates. To view and select the **Preset Calibration** tests in the **Select Tests** tab, select the **Run Preset Calibration** option in the **Test Setup** window of the **Set Up** tab.

Test Procedure

1 Connect the DUT to the Oscilloscope.
2 Configure the DUT transmitter to output PRBS31, preset 0 on all lanes with SSC enabled.
3 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used.
   b Oscilloscope with a minimum bandwidth of 21GHz.
4 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Adjust vertical scale such that the signal fits within the Oscilloscope's display
   c Measured at 1E6 UI
5 Capture eye height and eye width for lane 0.
6 Register mean eye height and mean eye width values.
7 Repeat the test for the remaining Thunderbolt lanes.
8 Repeat the test for all remaining Thunderbolt transmit presets (till preset 15 as shown in Table 5).
9 For each lane, choose the preset that provides maximum eye width. If there are two presets with the same eye width, select the one with the greater eye height.

Expected / Observable Results

For each lane, the preset that provides the maximum eye width is the optimized preset for the platform. If two presets have the same eye width, the preset with a greater eye height is the optimized preset.

Test References

See

- "Section 3.3.1 Preset Calibration" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-5 of the *Thunderbolt™ Interconnect Specification Revision 1.5 Draft 0.8.*

Tx CTLE Calibration

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx CTLE Calibration Test is to find the optimized CTLE (Continuous-Time-Linear-Equalizer) for the platform.

See "Reference CTLE" on page 61 to know more about CTLE.

NOTE Apply equalization on the Oscilloscope, when testing at TP3EQ.

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx CTLE Calibration* are checked.

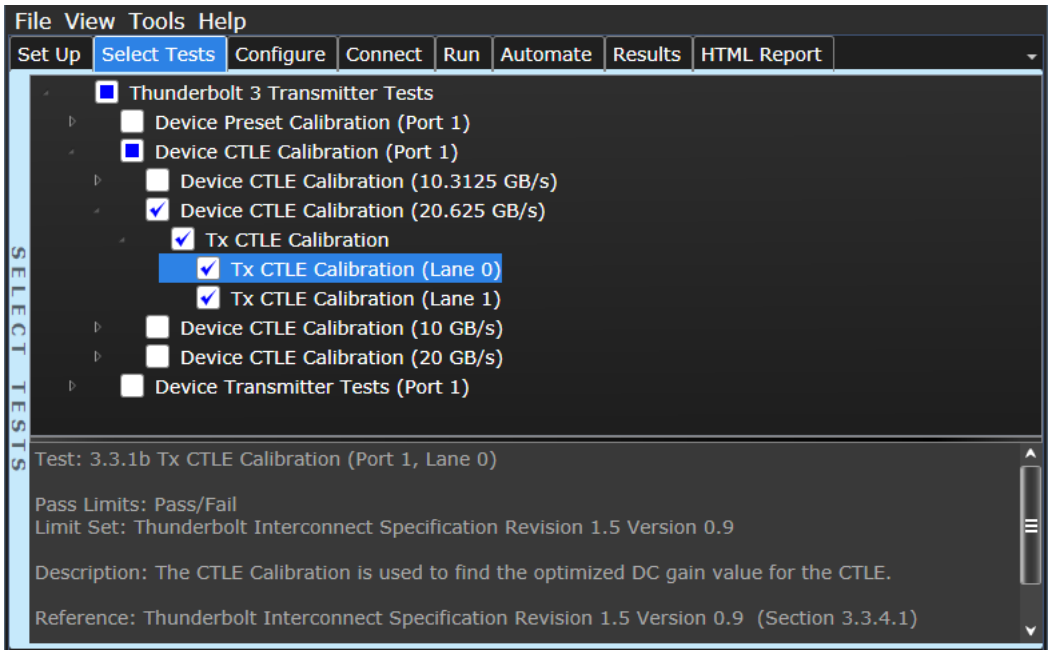


Figure 101 Selecting the Tx CTLE Calibration tests

NOTE By default, the test group for **CTLE Calibration** for each selected bit-rate is hidden in the **Select Tests** tab when **Predefined Optimum CTLE DC Gain Value** is selected for the respective bit-rates. To view and select the **CTLE Calibration** tests in the **Select Tests** tab, select the **Run CTLE Calibration** option in the **Test Setup** window of the **Set Up** tab.

Test Procedure

1 Follow the CTLE model as described in "Reference CTLE" on page 61, with the following parameters:

a AC Gain = 1.41

b Wp1 = 2 * π * 5G rad/sec

c Wp2 = 2 * π * 10G rad/sec

2 Apply ten different CTLE configurations such that A_{DC}, which is the DC Gain, is a value that lies within the following equation:

$$\{10^{-x/20} : x = 0 – 9\ [dB]\}$$

3 Calibrate A_{DC} using the following procedure:

a Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

b Select A_{DC} for x = 0.

c Perform measurement with reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used. Oscilloscope with a minimum bandwidth of 21GHz.

d Capture the waveform and process it with the Digital Oscilloscope:

- Sampling Rate ≥ 80 GSa/s
- Adjust vertical & horizontal scale such that the signal fits within the Oscilloscope's display
- Measured at 1E6 UI

e Eye height should be positioned at the "0" of the real time eye horizontal position.

f Apply a Histogram to the lower and upper sections of the eye, with ±1% deviation in time axis in order to calculate the eye height. Eye height is the delta between the minimum value from the upper histogram result (see Figure 102) and the maximum value from the lower histogram result (see Figure 103).

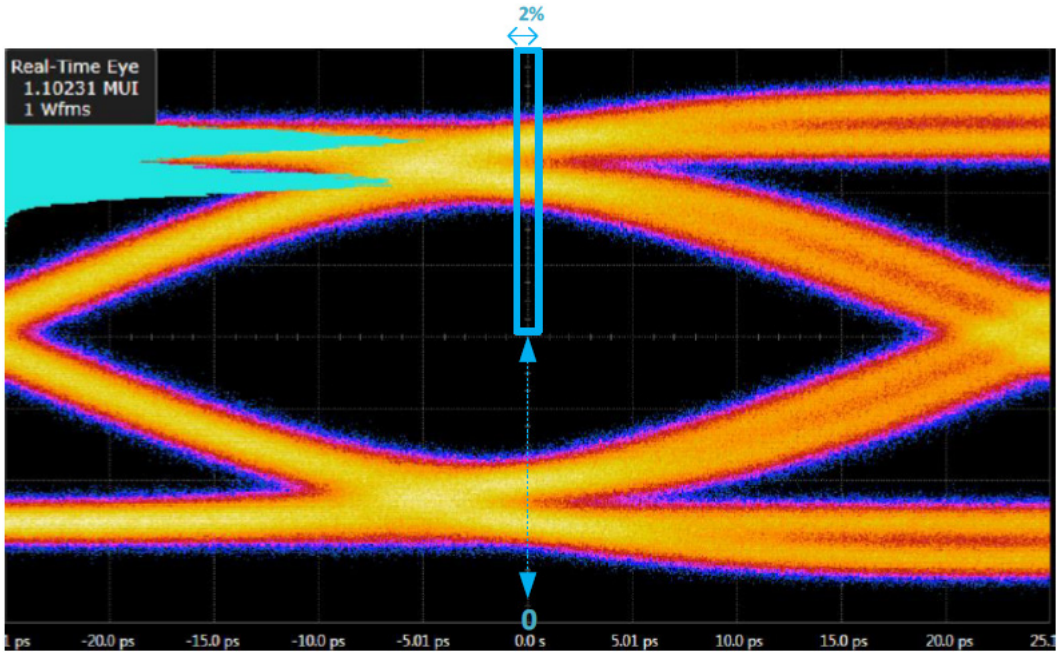


Figure 102 Thunderbolt RX TP3EQ Eye Height upper location measurement

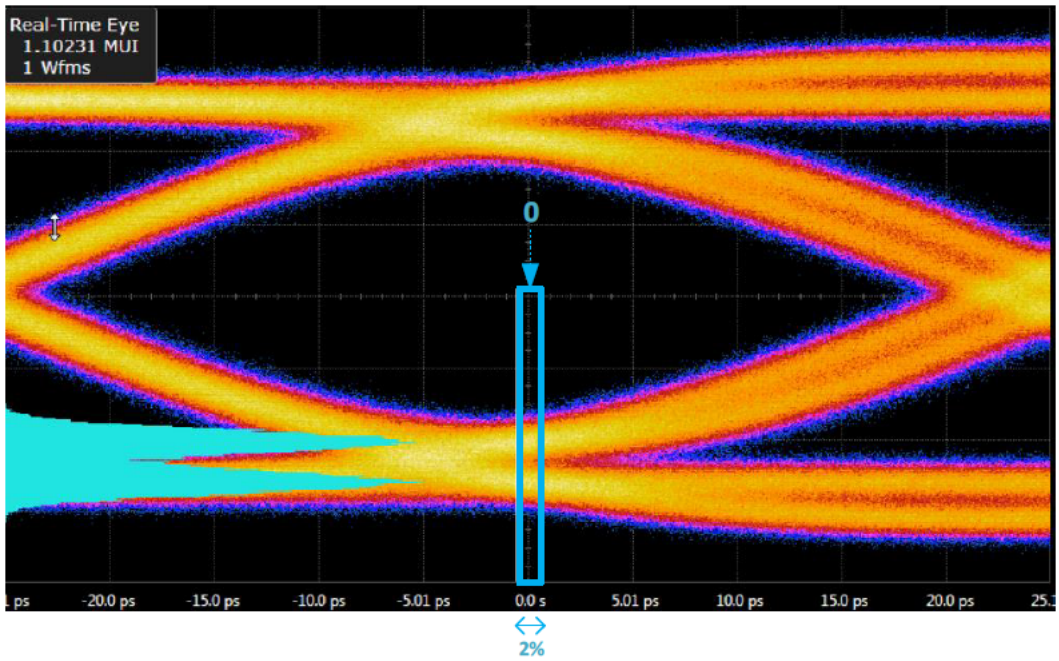


Figure 103 Thunderbolt RX TP3EQ Eye Height lower location measurement

g Capture five times (each time over new 1MUI record length) the minimum value of both eye height and eye width.

h Average the five captured values, that is, average of (5 times minimum eye height) and average of (5 times minimum eye width).

i Repeat this procedure from step 3b to 3i with x = x + 1 upto x = 9.

j Measure that value of A_{DC} (including DFE tap value), which yields the maximum eye height. If there are two values of A_{DC} (including DFE tap value), which have the same eye height, select the one that has the greater eye width.

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

For each lane, the DC Gain value that provides the maximum eye height is the optimized CTLE for the platform. If two DC Gain values have the same eye height, the one with a greater eye width is the optimized CTLE.

Test References

See

- "Section 8.2 Appendix C – Equalization Calibration" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9.*
- Section 3.3.4.1 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Rise/Fall Time

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Rise/Fall Time Test is to confirm that the rise times and fall times on the Thunderbolt differential signals are within the limits of the specification.

Test Pass Requirement

Rise Time and Fall Time ≥ 10ps (Refer to Table 4 on page 64).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Rise/Fall Time* are checked.

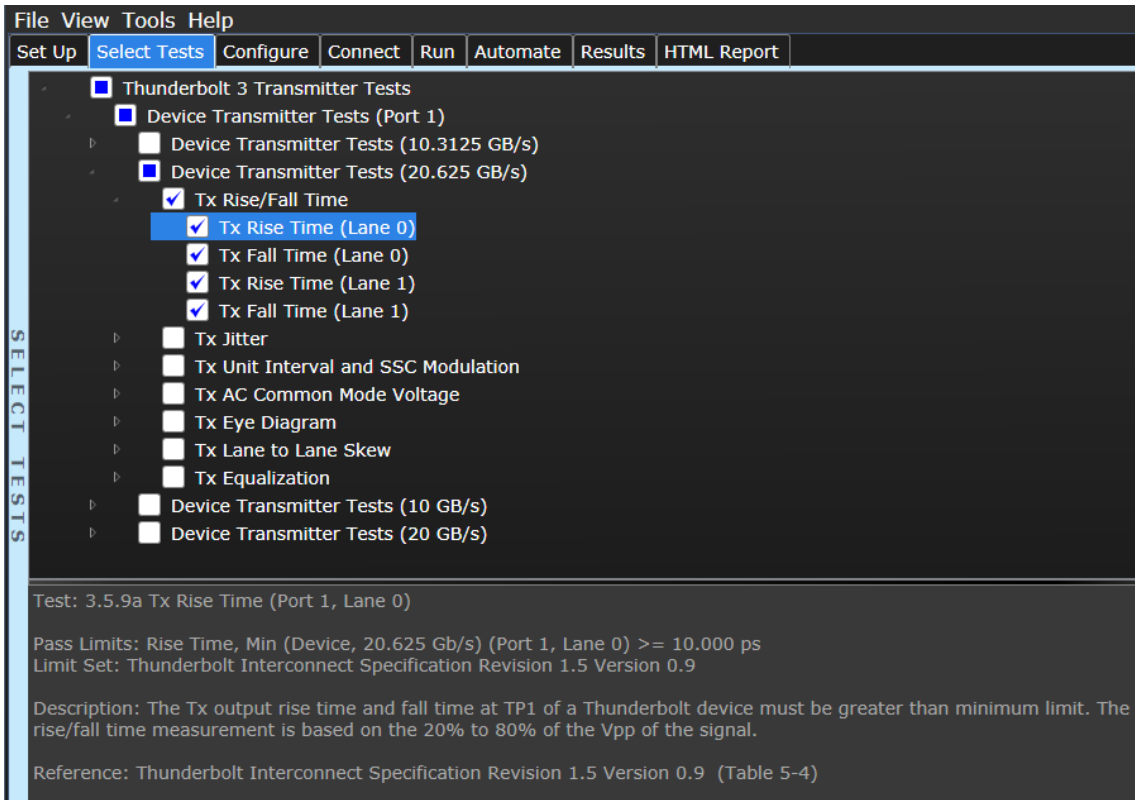


Figure 104 Selecting the Tx Rise/Fall Time tests

Test Procedure

1 Configure the DUT transmitter to output alternating square pattern of 16 0's and 16 1's on all lanes with SSC enabled.

2 Evaluate at least 4Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 4Mpts. Use the maximum analog bandwidth of the Oscilloscope.

   No CDR, no average and no interpolation to be used.

   Adjust vertical scale such that the signal fits within the Oscilloscope's display.

3 Measure T_{RISE} as the mode of the sampled edge times from 20% to 80% of the differential swing voltage rising edge.

4 Measure T_{FALL} as the mode of the sampled edge times from 80% to 20% of the differential swing voltage falling edge.

5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If T_{RISE} < 10ps, the status of test is FAIL.

If T_{FALL} < 10ps, the status of test is FAIL.

Test References

See

- "Section 3.5.9 Gen3 Rise/Fall Time Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Total Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Total Jitter Test is to confirm that the Total Jitter of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of 1×10^{-13}.

Test Pass Requirement

Total Jitter (TJ) $\leq 0.46\ UI_{p\text{-}p}$ (Refer to Table 8 on page 71).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Total Jitter* are checked.

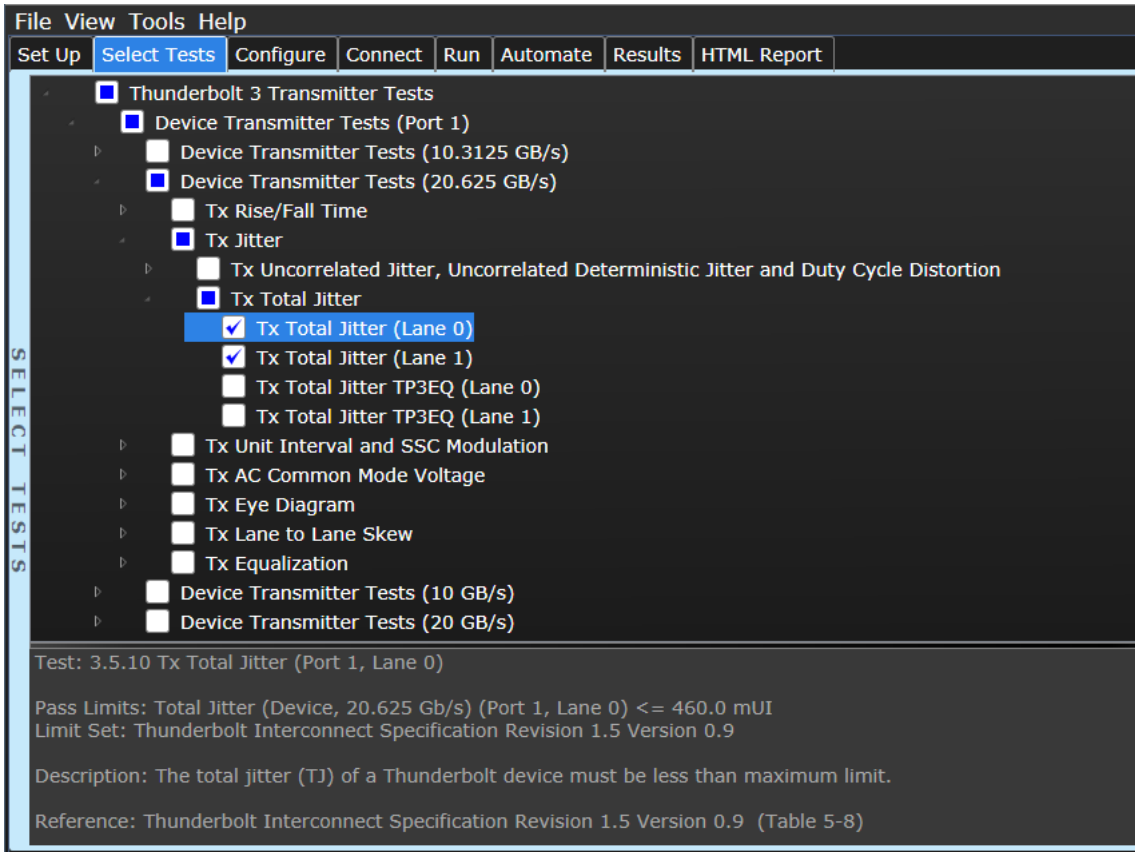


Figure 105 Selecting the Tx Total Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   b Oscilloscope with a minimum bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display.
   f Referenced to 1E-13 statistics.
4 Capture the values of Total Jitter (TJ) and Deterministic Jitter (DJ).

5 If TJ > 0.46 UI_{p-p}, perform the following steps:

a Configure the DUT transmitter to output alternating square pattern of one 0's and one 1's on all lanes with SSC enabled. (The pattern is SQ2 instead of PRBS15).

b Perform measurements with:

- Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
- Oscilloscope with a minimum bandwidth of 21GHz

c Capture the waveform and process it with the Digital Oscilloscope:

- Sampling Rate $\geq$ 80 GSa/s
- Pattern length – Periodic
- Jitter Separation method must be suitable for cross-talk on the signal
- Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
- Adjust vertical scale such that the signal fits within the Oscilloscope's display.
- Referenced to 1E-13 statistics.

d Capture the Random Jitter (RJ) result.

e Calculate TJ using the equation:

TJ = DJ + 14.7 * RJ (DJ from #4; PRBS15 and RJ from #5d; SQ2)

6 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If TJ > 0.46 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.5.10 Gen3 Total Jitter" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Uncorrelated Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Jitter Test is to confirm that the Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Jitter (UJ) $\leq$ 0.31 UI_{p-p} (Refer to Table 8 on page 71).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

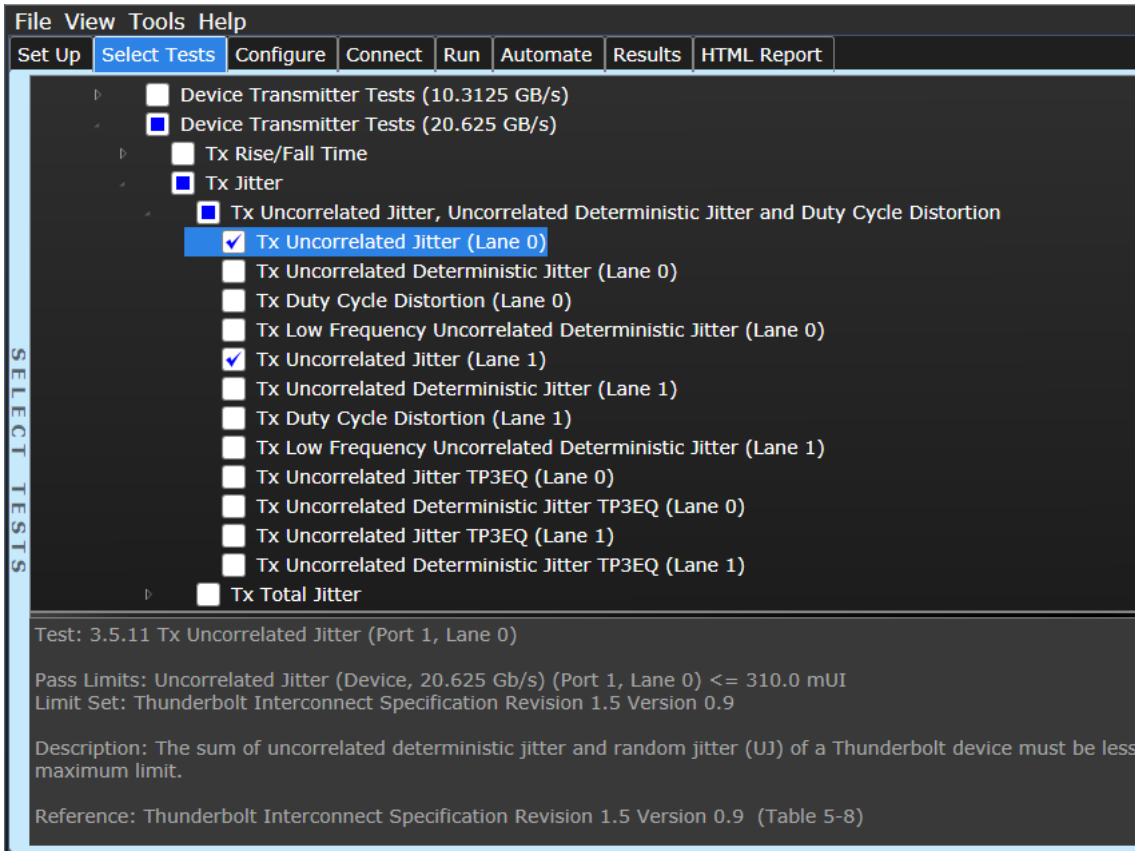


Figure 106 Selecting the Tx Uncorrelated Jitter tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Perform measurements with:
   - *a* Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   - *b* Oscilloscope with a minimum bandwidth of 21GHz
3. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Pattern length – Periodic
   - *c* Jitter Separation method must be suitable for cross-talk on the signal
   - *d* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *e* Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   - *f* Referenced to 1E-13 statistics
4. Capture the Total Jitter (TJ) and Data Dependent Jitter (DDJ) results.
5. Calculate UJ using the equation:

$$UJ = TJ - DDJ$$

6. Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UJ > 0.31 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.5.11 Gen3 UJ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Uncorrelated Deterministic Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Deterministic Jitter Test is to confirm that the Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Deterministic Jitter (UDJ) $\leq$ 0.17 UI_{p-p} (Refer to Table 8 on page 71).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

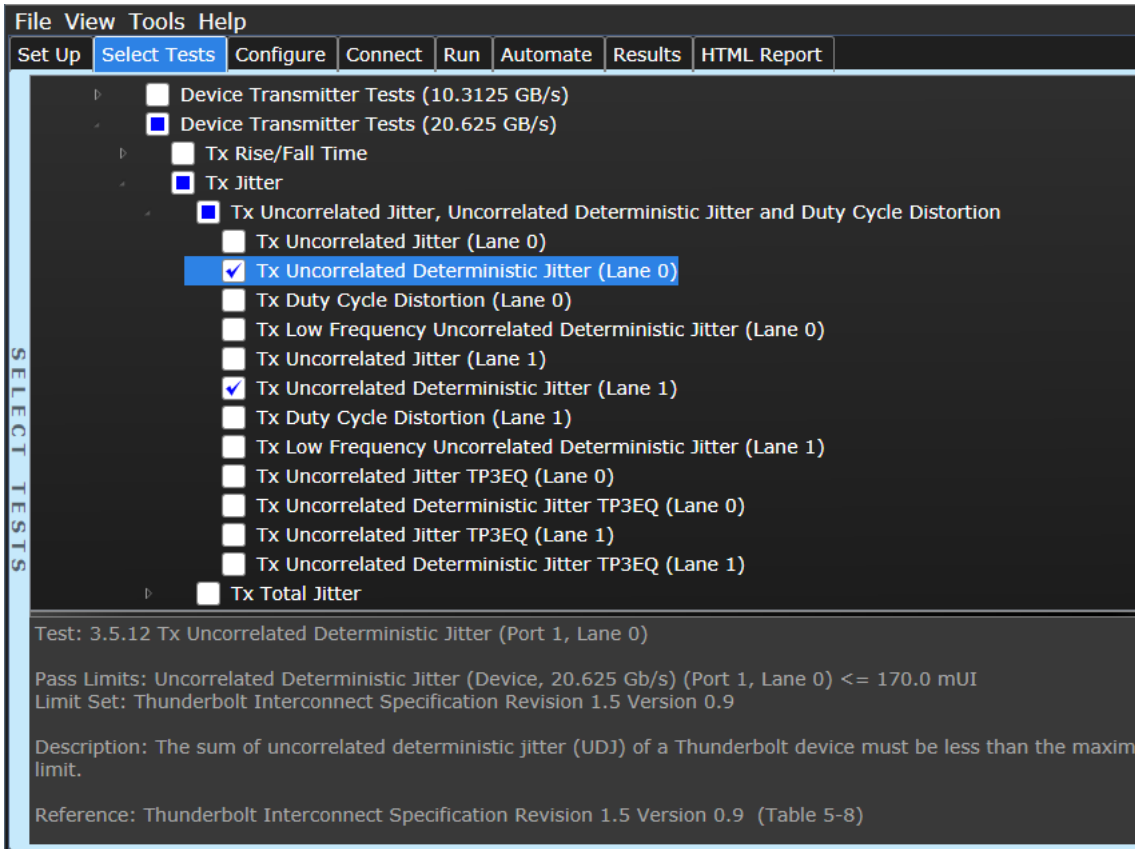


Figure 107 Selecting the Tx Uncorrelated Deterministic Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   f Referenced to 1E-13 statistics
4 Capture the UDJ result (same as BUJ over the Oscilloscope).
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UDJ > 0.17 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.5.12 Gen3 UDJ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Low Frequency Uncorrelated Deterministic Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Low Frequency Uncorrelated Deterministic Jitter Test is to confirm that the Low Frequency Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Low Frequency Uncorrelated Deterministic Jitter (UDJ_LF) $\leq$ 0.07 UI_{p-p} (Refer to Table 8 on page 71).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

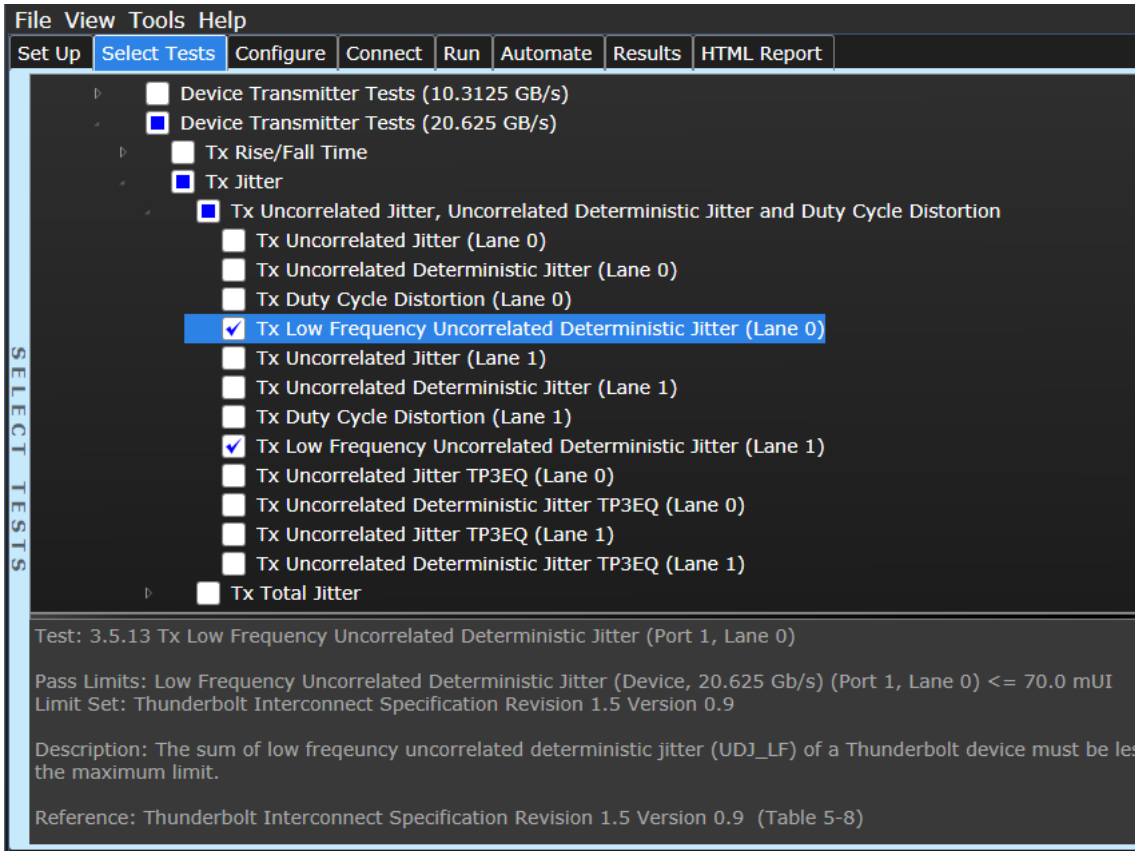


Figure 108 Selecting the Tx Low Frequency Uncorrelated Deterministic Jitter tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Perform measurements with:
   - *a* Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   - *b* Apply 2nd order Low-Pass-Filter with 3 dB cut-off at 2MHz; no average and no interpolation to be used
   - *c* Oscilloscope with a minimum bandwidth of 21GHz
3. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Pattern length – Periodic
   - *c* Jitter Separation method must be suitable for cross-talk on the signal
   - *d* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *e* Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
4. Capture the UDJ_LF result.
5. Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UDJ_LF > 0.07 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.5.13 Gen3 Low Frequency UDJ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Duty Cycle Distortion

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Duty Cycle Distortion Test is to confirm that the transmitter Deterministic Jitter Associated by Duty-Cycle-Distortion Jitter falls within the limits of the specification.

Test Pass Requirement

Duty-Cycle-Distortion (DCD) ≤ 0.03UIp-p (Refer to Table 6 on page 68).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

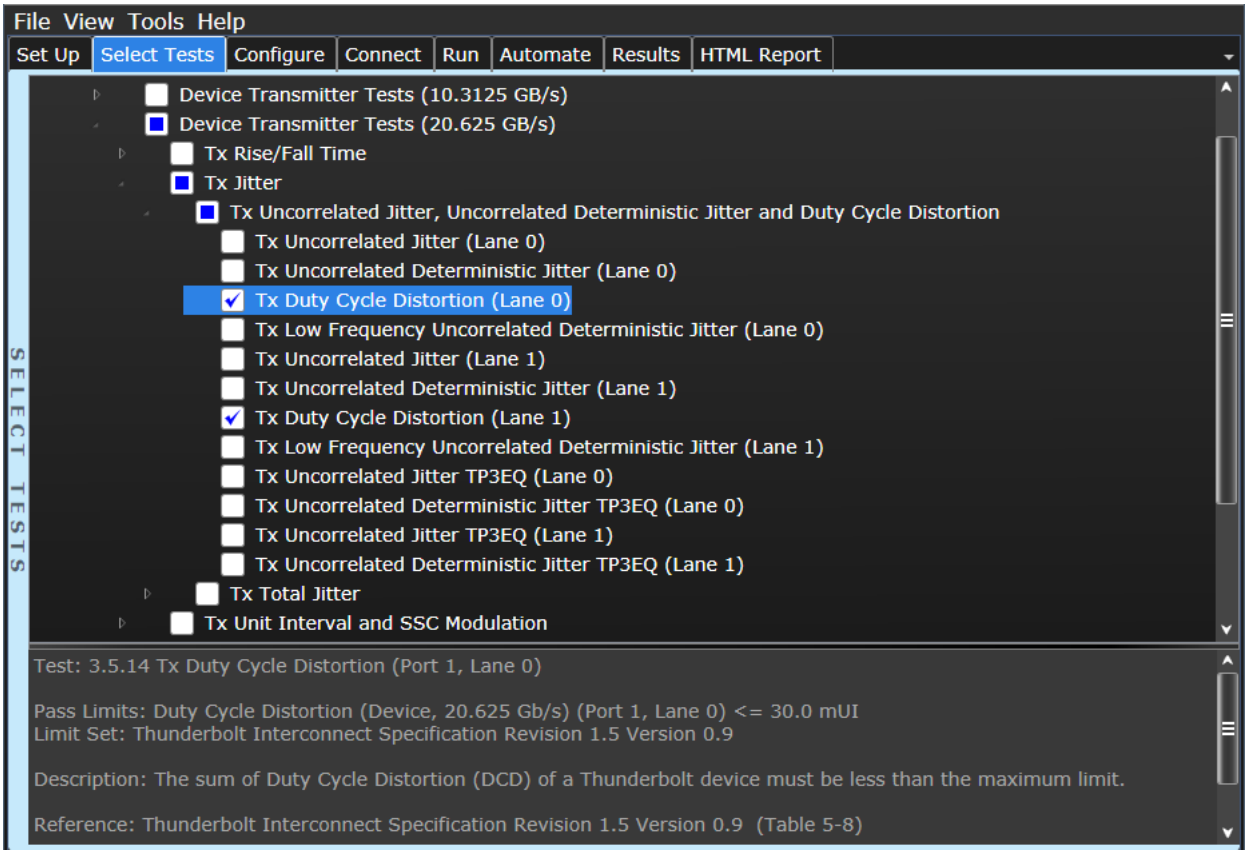


Figure 109 Selecting the Tx Duty Cycle Distortion tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts.
4 Capture the DCD result.
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If DCD > 0.03UIp-p, the status of test is FAIL.

Test References

See

- "Section 3.5.14 Gen3 DCD Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Unit Interval

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Unit Interval Test is to confirm that the data rate, under all conditions, does not exceed the minimum or maximum limits of the specification.

Test Pass Requirement

G3_UI_MIN ≤ Unit Interval ≤ G3_UI_MAX (Refer to Table 8 on page 71).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

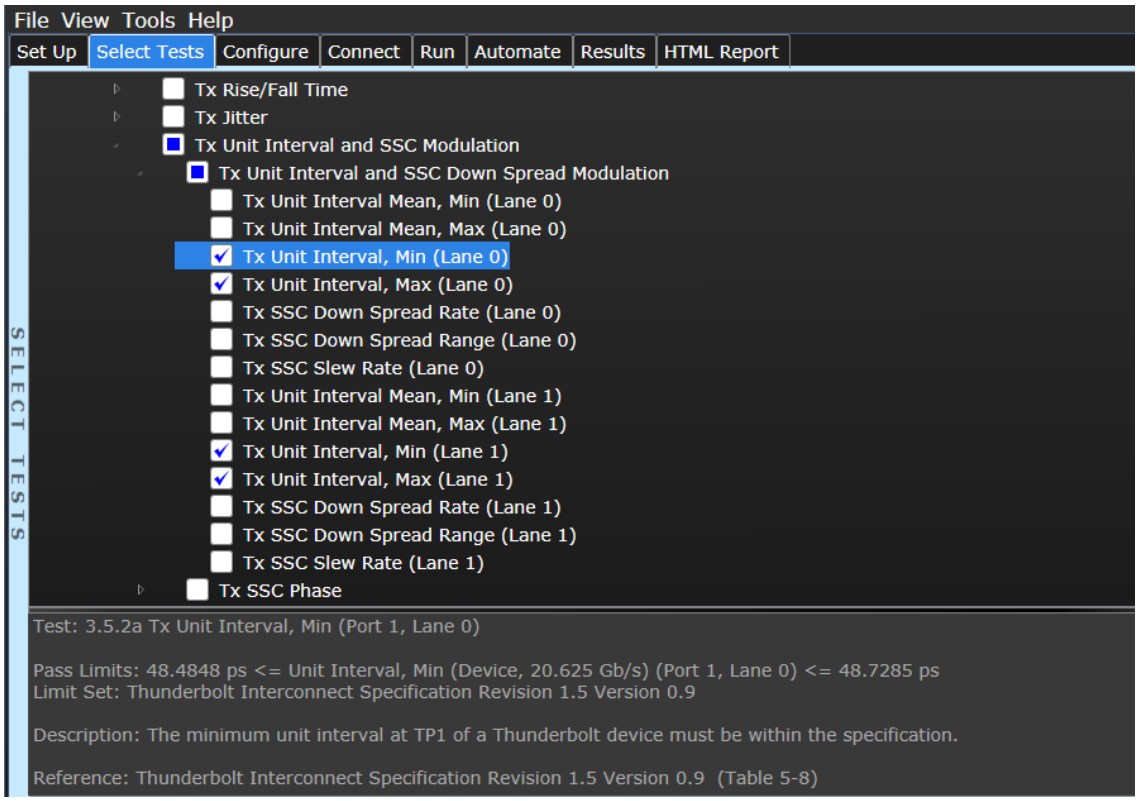


Figure 110 Selecting the Tx Unit Interval tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 21GHz
3 Calculate UI dynamically using a uniform moving average filter procedure with a window size of 6000 symbols.
4 Measure the values of both UI_{MAX} and UI_{MIN}.
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UI_{MAX} > G3_UI_MAX, the status of test is FAIL.

If UI_{MIN} < G3_UI_MIN, the status of test is FAIL.

Test References

See

- "Section 3.5.2 Gen3 Unit Interval Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Unit Interval Mean

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Unit Interval Mean Test is to confirm that the average data rate, under all conditions, does not exceed the minimum or maximum limits of the specification.

Test Pass Requirement

G3_UI_MEAN_MIN ≤ Average Unit Interval ≤ G3_UI_MEAN_MAX (Refer to Table 8 on page 71).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

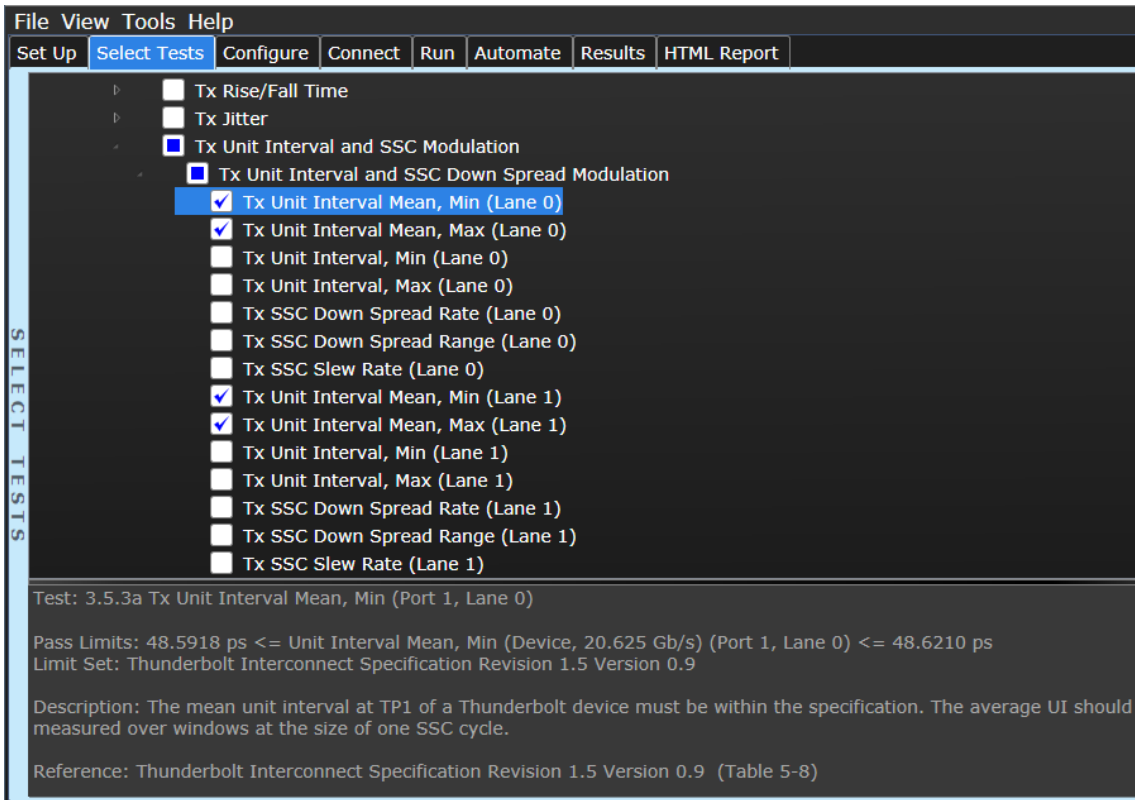


Figure 111 Selecting the Tx Unit Interval Mean tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate ≥ 80 GSa/s

b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts

c No CDR, no average and no interpolation to be used

d Adjust vertical scale such that the signal fits within the Oscilloscope's display

e Oscilloscope must have a minimum bandwidth of 21GHz

3 Use mathematical analysis to measure the average unit interval over a window of the size of one SSC cycle, determined by the SSC_Down_Spread_Rate.

4 Measure UI_MEAN over different windows that uniformly cover the Oscilloscope capture for at least 300ms (more than 10 SSC Cycles) with 10000 UI window jumps. See Figure 112.

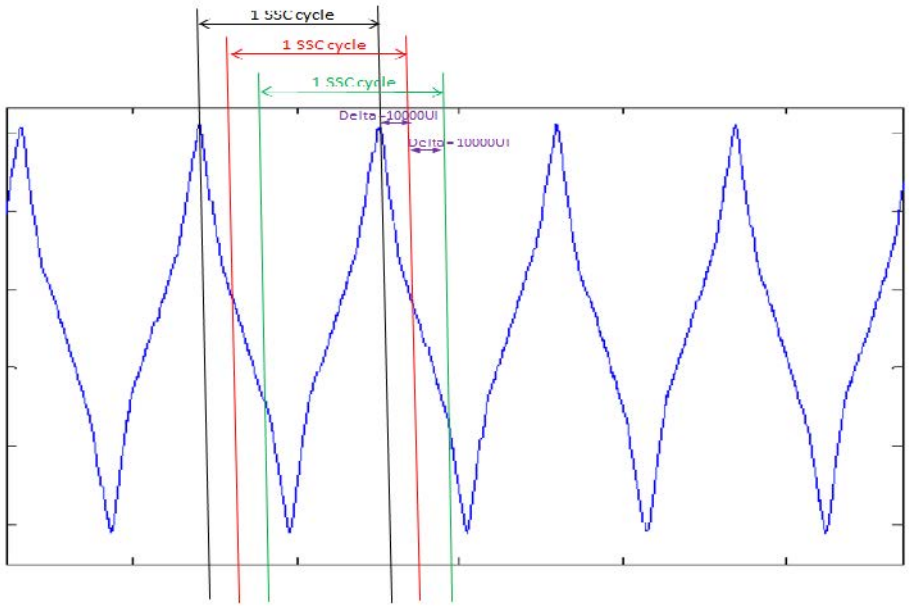


Figure 112 Measurement of UI_MEAN over at least 10 SSC Cycles

5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If the maximum UI_MEAN measured > G3_UI_MEAN_MAX, the status of test is FAIL.

If the minimum UI_MEAN measured < G3_UI_MEAN_MIN, the status of test is FAIL.

Test References

See

- "Section 3.5.3 Gen3 Unit Interval Mean Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx SSC Down Spread Range

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Down Spread Range Test is to confirm that the data down spreading is within the limits of the specification.

Test Pass Requirement

0.4% ≤ SSC_Down_Spread_Range ≤ 0.5% (Refer to Table 4 on page 64).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

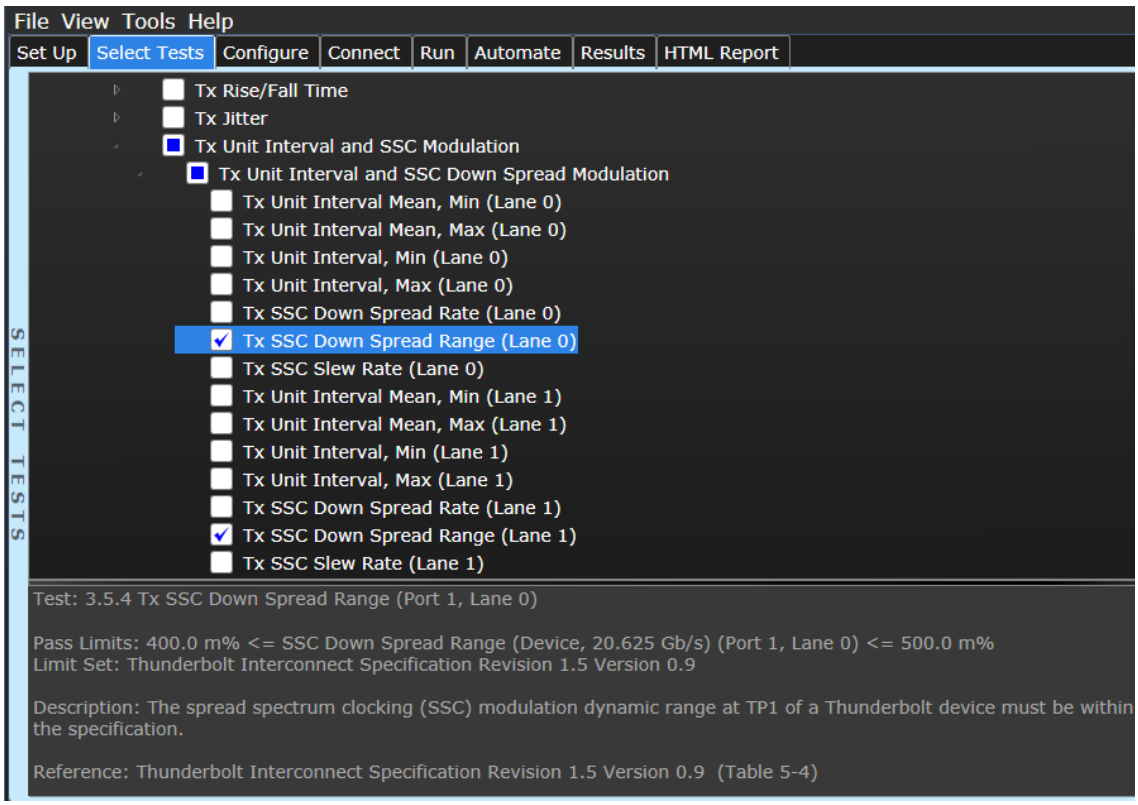


Figure 113 Selecting the Tx SSC Down Spread Range tests

Test Procedure

1. Run the "Tx Unit Interval" Test as a prerequisite to obtain UI_{MAX} and UI_{MIN}.
2. Use the obtained value of UI_{MAX} and UI_{MIN} to calculate the Deviation percentage:

   $$\text{Maximum Deviation} = 100*\{[20.625G - (1 / UI_{MAX})] / 20.625G\}$$

   $$\text{Minimum Deviation} = 100*\{[20.625G - (1 / UI_{MIN})] / 20.625G\}$$
3. Calculate SSC Down Spread Range using the equation:

   $$\text{Maximum Deviation} - \text{Minimum Deviation}$$
4. Repeat the test for all remaining Thunderbolt lanes.

Expected / Observable Results

If SSC_Down_Spread_Range > 0.5% or SSC_Down_Spread_Range < 0.4%, the status of test is FAIL.

Test References

See

- "Section 3.5.4 Gen3 SSC Down Spread Deviation Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx SSC Down Spread Rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Down Spread Rate Test is to confirm that the Link clock down-spreading modulation rate is within the limits of the specification.

Test Pass Requirement

SSC_DSR_MIN ≤ SSC_Down_Spread_Rate ≤ SSC_DSR_MAX (Refer to Table 4 on page 64).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

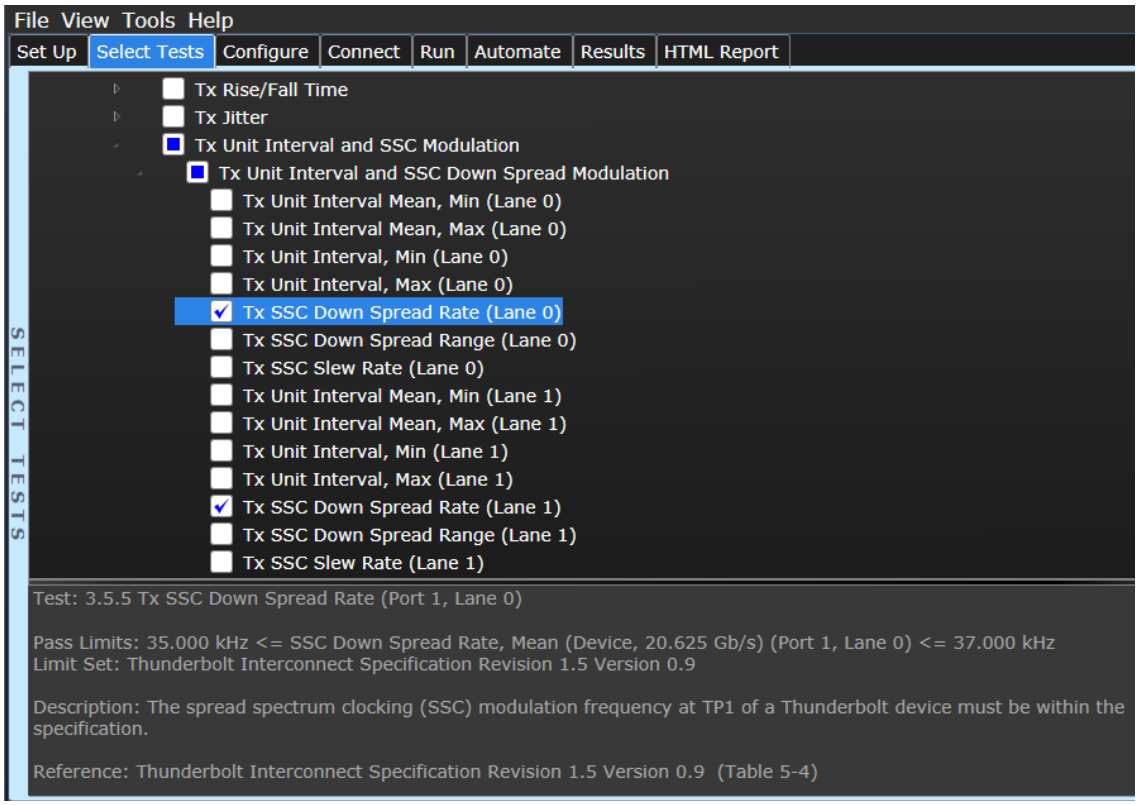


Figure 114 Selecting the Tx SSC Down Spread Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 21GHz
3 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If SSC_DSR_MIN > SSC_Down_Spread_Rate > SSC_DSR_MAX, the status of test is FAIL.

Test References

See

- "Section 3.5.5 Gen3 SSC Down Spread Rate Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx SSC Phase Deviation

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Phase Deviation Test is to confirm that the SSC Phase Deviation is within the limits of the specification.

Test Pass Requirement

2.5ns p-p ≤ SSC_Phase_Deviation ≤ SSC_PD_MAX (Refer to Table 4 on page 64).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx SSC Phase* are checked.

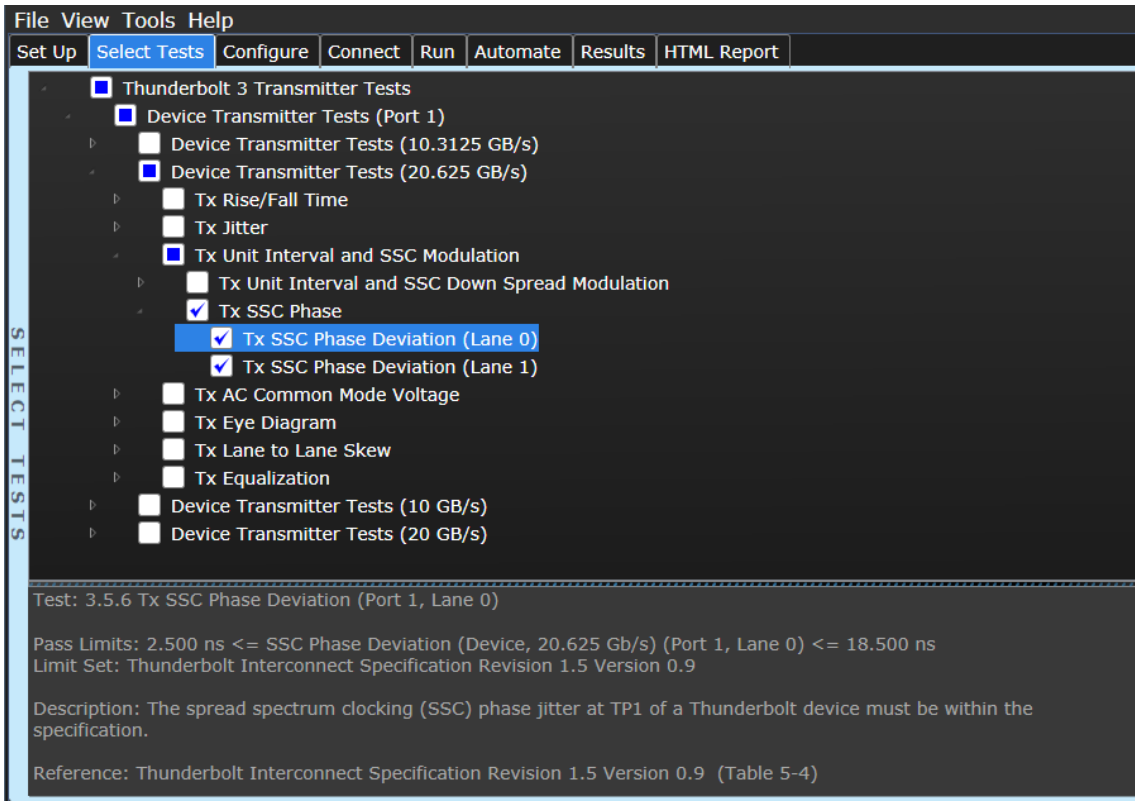


Figure 115 Selecting the Tx SSC Phase Deviation tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope's software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 21GHz
3 Extract the SSC Phase Deviation from the transmitted signal.
4 Extract the SSC Phase Deviation from the phase jitter after applying a 2^{nd} order low-pass filter with 3dB point at 2 MHz.
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If 2.5ns p-p > SSC_Phase_Deviation > SSC_PD_MAX the status of test is FAIL.

Test References

See

- "Section 3.5.6 Gen3 SSC Phase Deviation Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx SSC Slew Rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Slew Rate Test is to confirm that the SSC Slew Rate is within the limits of the specification.

Test Pass Requirement

SSC_Slew_Rate ≤ 1000 ppm/µs (Refer to Table 4 on page 64).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

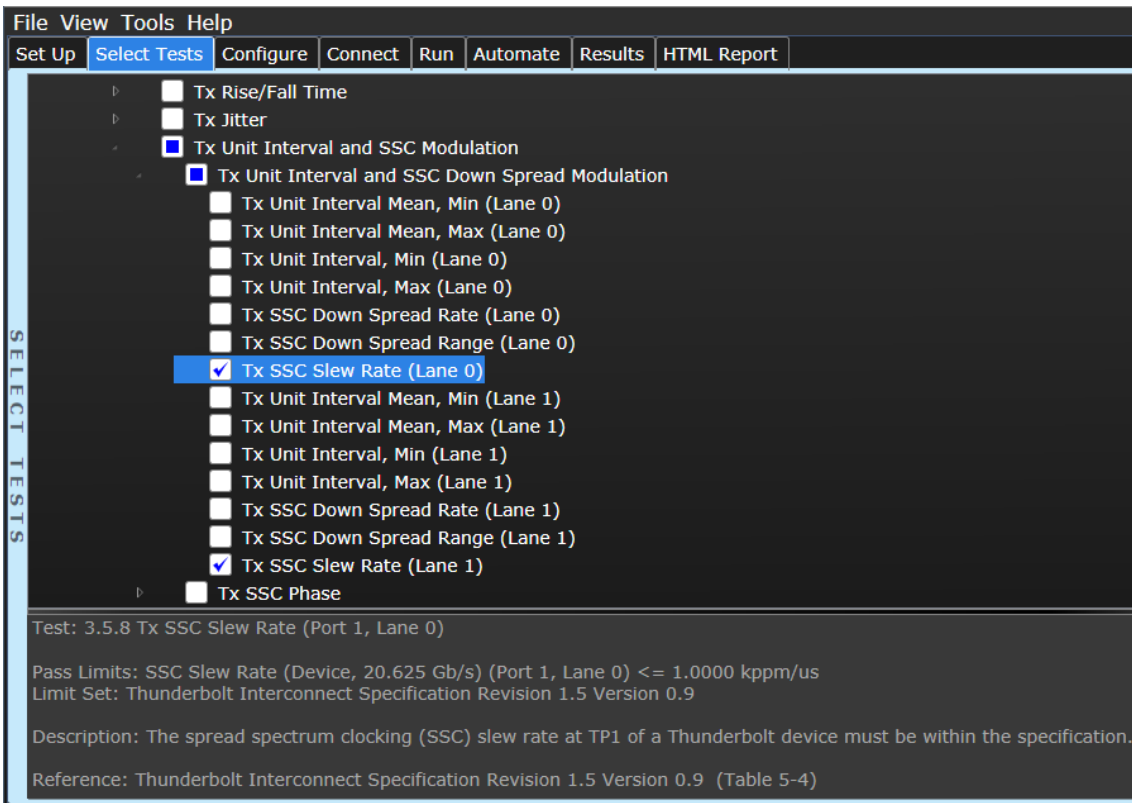


Figure 116 Selecting the Tx SSC Slew Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and post process it with an appropriate software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Extract SSC slew rate from the transmitted signal over measurement intervals of 0.5µs
   f Extract SSC slew rate from the phase information after applying a 2nd order Low-Pass-Filter with 3 dB cut-off at 2MHz.
   g Oscilloscope must have a minimum bandwidth of 21GHz
3 SSC_Slew_Rate is measured as the SSC frequency deviation over time while valid data is being transmitted in which 1E-12 bit error rate is required without assuming forward error correction.
4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If SSC_Slew_Rate_Data > 1000 ppm/µs, the status of test is FAIL.

Test References

See

- "Section 3.5.7 Gen3 SSC Slew Rate Data Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Lane to Lane Skew

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Lane to Lane Skew Test is to confirm that the Skew between dual transmit signals of the same port group falls within the limits of the specification.

Test Pass Requirement

Lane_to_Lane_Skew ≤ 26nS (Refer to Table 4 on page 64).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Lane to Lane Skew* are checked.

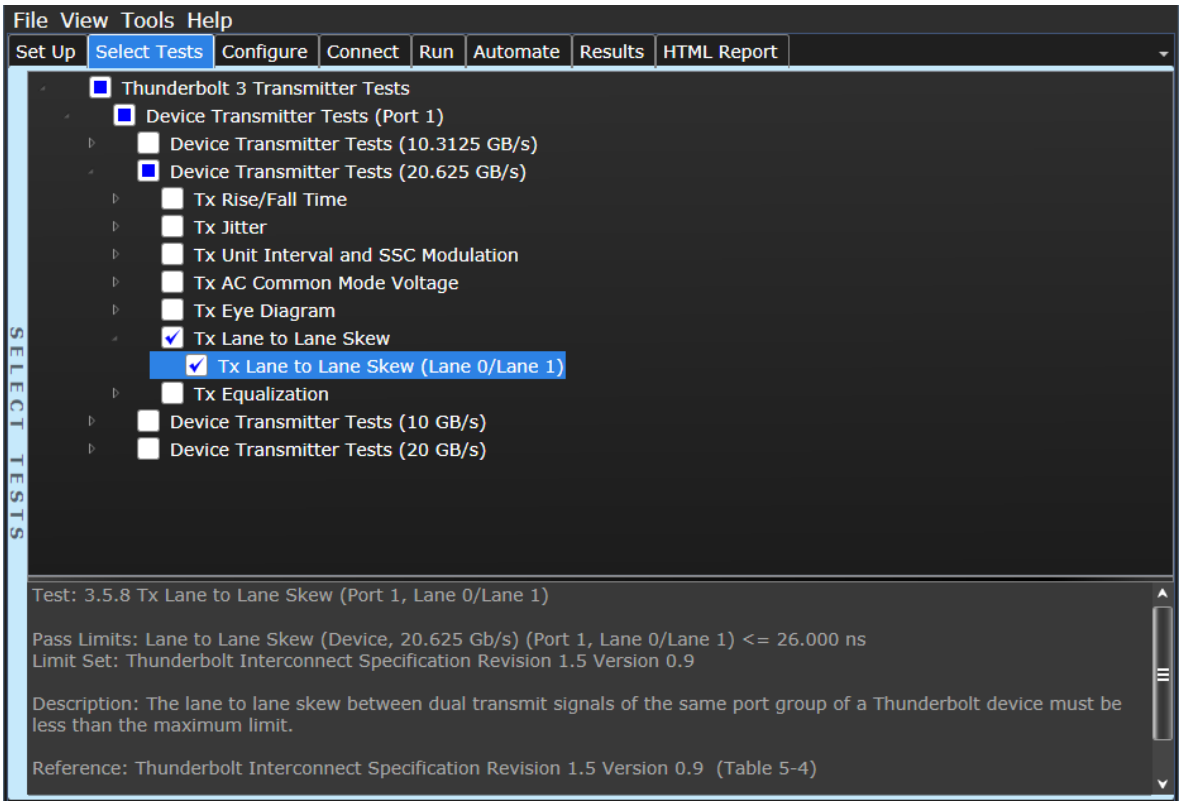


Figure 117 Selecting the Tx Lane to Lane Skew tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveforms from 2 lanes from the same port together and post process it with an appropriate software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 10Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 10Mpts.
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Measurement must be performed between consecutive rising edges
   f Oscilloscope must have a minimum bandwidth of 21GHz
3 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If Lane_to_Lane_Skew > 26nS, the status of test is FAIL.

Test References

See

- "Section 3.5.8 Gen3 Lane to Lane Skew Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Eye Diagram

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Eye Diagram Test is to confirm that the differential signal on each Thunderbolt differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram should meet the conditions depicted in Figure 118.

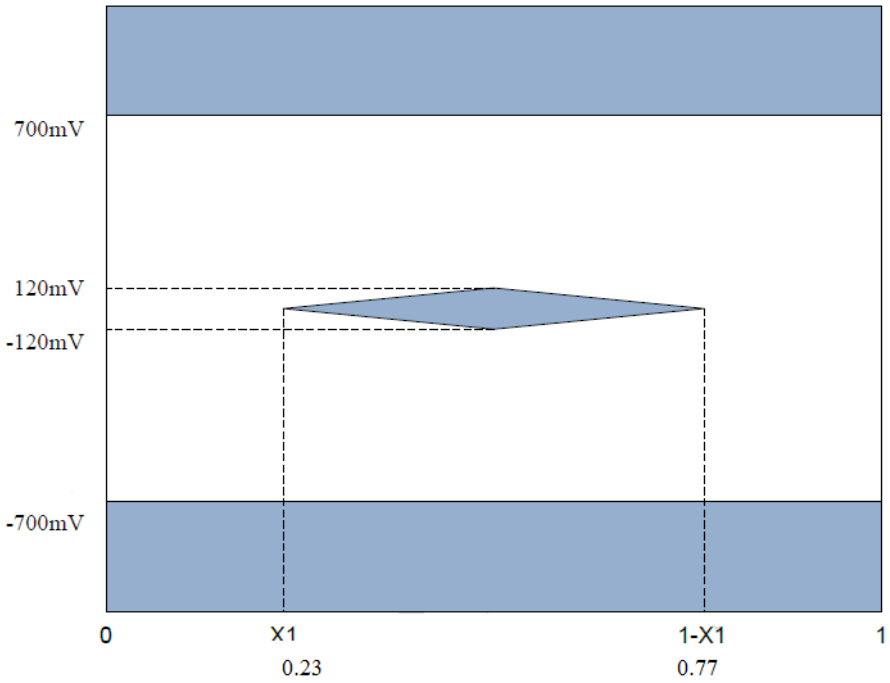


Figure 118 Pass Condition for Tx Eye Diagram Tests

(Refer to Table 8 on page 71 and Figure 41 on page 70).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Eye Diagram* are checked.

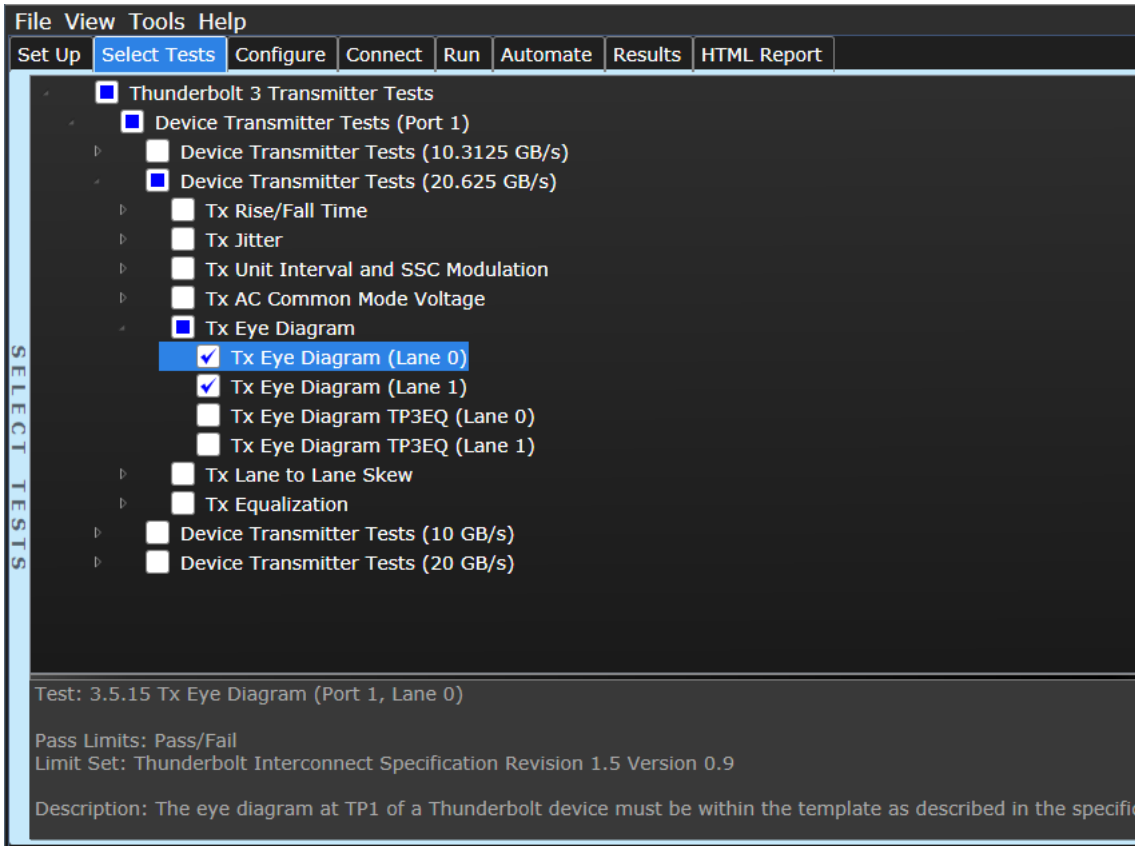


Figure 119 Selecting the Tx Eye Diagram tests

Test Procedure

1. Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2. Perform measurements with:
   - *a* Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   - *b* Oscilloscope with a minimum bandwidth of 21GHz
3. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *c* Measured at 1E6 UI
4. Compare the data eye to the TP1 eye diagram mask. Check for conditions described in the section "Expected / Observable Results".
5. Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the inner or outer height voltage (+/- 700mV), the status of the test is FAIL.

ii If any part of the waveform hits the mask, the status of the test is FAIL.

Test References

See

- "Section 3.5.16 Gen3 Eye Diagram Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-8 and Figure 5-15 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx AC Common Mode Voltage

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx AC Common Mode Voltage Test is to confirm that the transmitter common mode on the Thunderbolt differential signals is within the limits of the specification.

Test Pass Requirement

TX AC Common Mode Voltage $\leq 100mV_{p-p}$ (Refer to Table 8 on page 71).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx AC Common Mode Voltage* are checked.

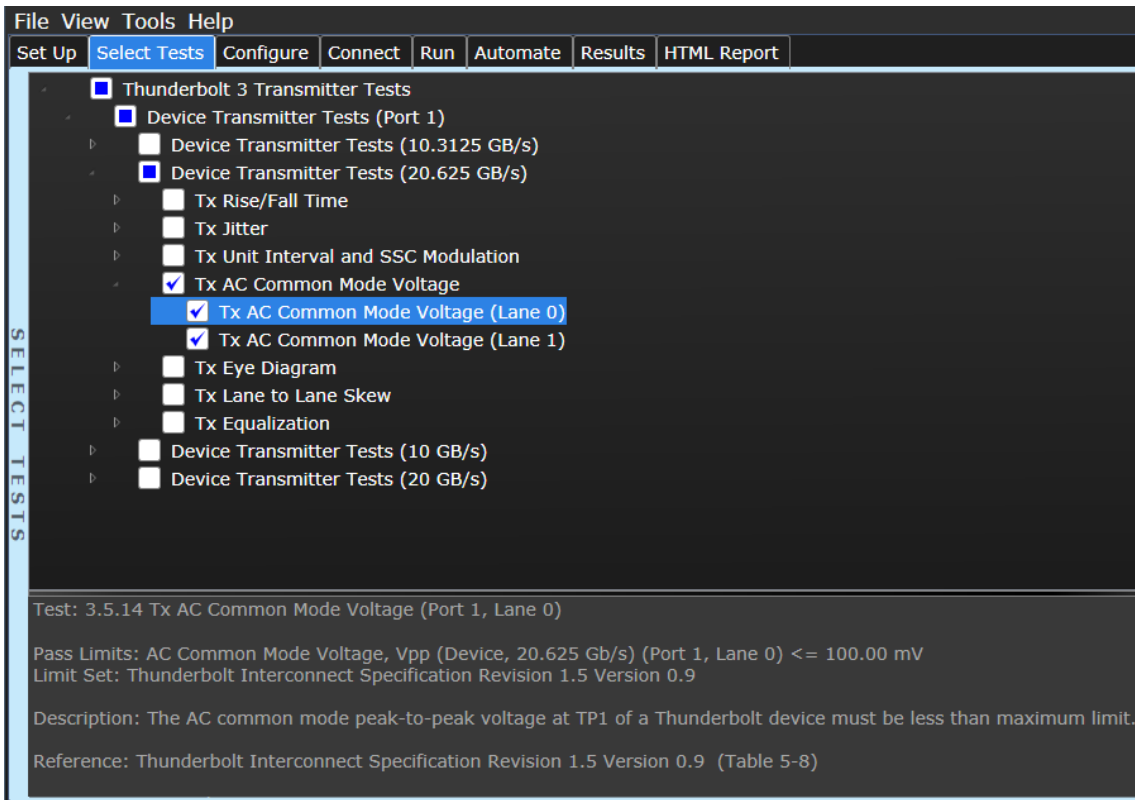


Figure 120 Selecting the Tx AC Common Mode Voltage tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Oscilloscope must have a minimum bandwidth of 21GHz
3 Calculate the AC Common Mode Voltage (V_{AC-CM}) using the equation:

$$V_{AC-CM} = (V_{TX-P} + V_{TX-N}) / 2$$

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $V_{AC-CM} > 100mV_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.5.15 Gen3 AC Common Mode Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Total Jitter TP3EQ

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Total Jitter TP3EQ Test is to confirm that the Total Jitter at point TP3EQ of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of $1x10^{-13}$.

Test Pass Requirement

Total Jitter (TJ_{TP3EQ}) $\leq$ 0.60 UI_{p-p} (Refer to Table 9 on page 72).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Total Jitter* are checked.

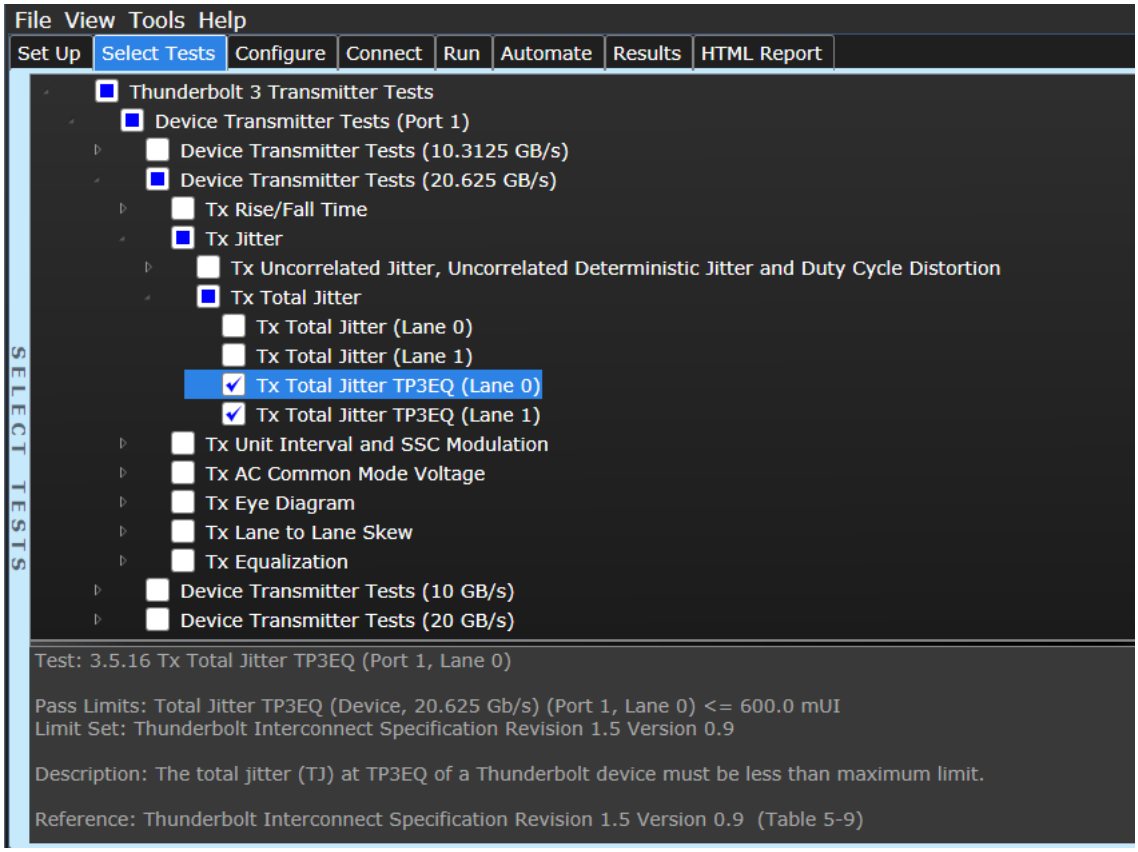


Figure 121 Selecting the Tx Total Jitter TP3EQ tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Embed the Type-C cable in the Oscilloscope. For Gen 3 systems, use TP3_EQ embedding file *TBT_0p8m.s4p*.
3 De-embed the cables from the test fixture to the Oscilloscope.
4 Ensure that measurements are done with a calibrated reference equalizer (CTLE only). See "Tx CTLE Calibration" on page 200.
5 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 21GHz
6 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display
   f Referenced to 1E-13 statistics

7 Capture the values of Total Jitter (TJ_{TP3EQ}) and Deterministic Jitter (DJ_{TP3EQ}).

8 If $TJ_{TP3EQ} > 0.60\ UI_{p-p}$, perform the following steps:

a Configure the DUT transmitter to output alternating square pattern of one 0's and one 1's on all lanes with SSC enabled. (The pattern is SQ2 instead of PRBS15).

b Perform measurements with:

- Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
- Oscilloscope with a minimum bandwidth of 21GHz

c Capture the waveform and process it with the Digital Oscilloscope:

- Sampling Rate $\geq$ 80 GSa/s
- Pattern length – Periodic
- Jitter Separation method must be suitable for cross-talk on the signal
- Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
- Adjust vertical scale such that the signal fits within the Oscilloscope's display.
- Referenced to 1E-13 statistics.

d Capture the Random Jitter (RJ_{TP3EQ}) result.

e Calculate TJ_{TP3EQ} using the equation:

$TJ_{TP3EQ} = DJ_{TP3EQ} + 14.7 * RJ_{TP3EQ}$ (DJ_{TP3EQ} from #7; PRBS15 and RJ_{TP3EQ} from #8d; SQ2)

9 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $TJ_{TP3EQ} > 0.60\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.5.17 Gen3 Total Jitter TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-9 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Uncorrelated Jitter TP3EQ

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Jitter TP3EQ Test is to confirm that the Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] at point TP3EQ of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Jitter (UJ_{TP3EQ}) $\leq$ 0.31 UI_{p-p} (Refer to Table 9 on page 72).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

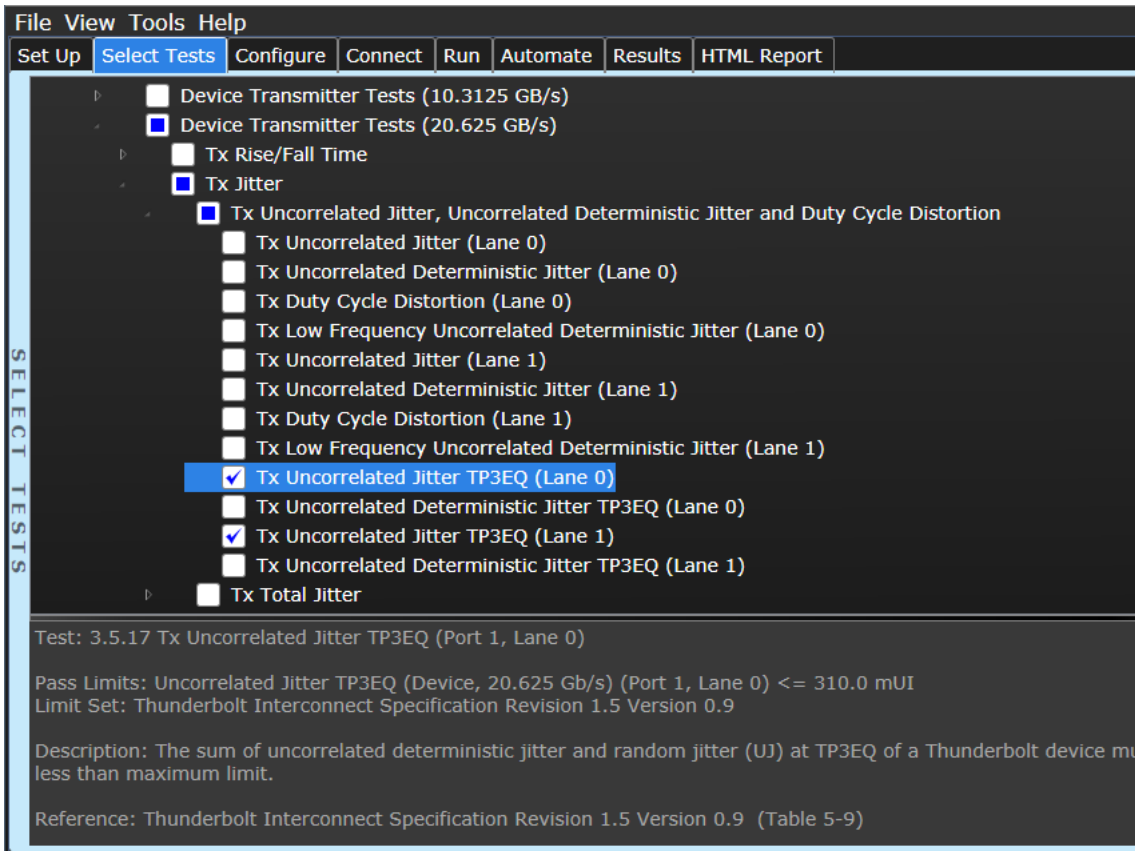


Figure 122 Selecting the Tx Uncorrelated Jitter TP3EQ tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Embed the Type-C cable in the Oscilloscope. For Gen 3 systems, use TP3_EQ embedding file *TBT_0p8m.s4p*.
3. De-embed the cables from the test fixture to the Oscilloscope.
4. Ensure that measurements are done with a calibrated reference equalizer (CTLE only). See "Tx CTLE Calibration" on page 200.
5. Perform measurements with:
   - *a* Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   - *b* Oscilloscope with a minimum bandwidth of 21GHz
6. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Pattern length – Periodic
   - *c* Jitter Separation method must be suitable for cross-talk on the signal
   - *d* Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   - *e* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *f* Referenced to 1E-13 statistics

7 Capture the values of Total Jitter (TJ_{TP3EQ}) and Data Deterministic Jitter (DDJ_{TP3EQ}).

8 Calculate UJ_{TP3EQ} using the equation:

$$UJ_{TP3EQ} = TJ_{TP3EQ} - DDJ_{TP3EQ}$$

9 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $UJ_{TP3EQ} > 0.31\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.5.18 Gen3 UJ TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-9 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Uncorrelated Deterministic Jitter TP3EQ

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Sum of Uncorrelated Deterministic Jitter TP3EQ Test is to confirm that the sum of Uncorrelated Deterministic Jitter at point TP3EQ of the transmitter is within the limits of the specification.

Test Pass Requirement

Deterministic Jitter that is uncorrelated to the transmitted data (UDJ_{TP3EQ}) ≤ 0.17 UI_{p-p} (Refer to Table 9 on page 72).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

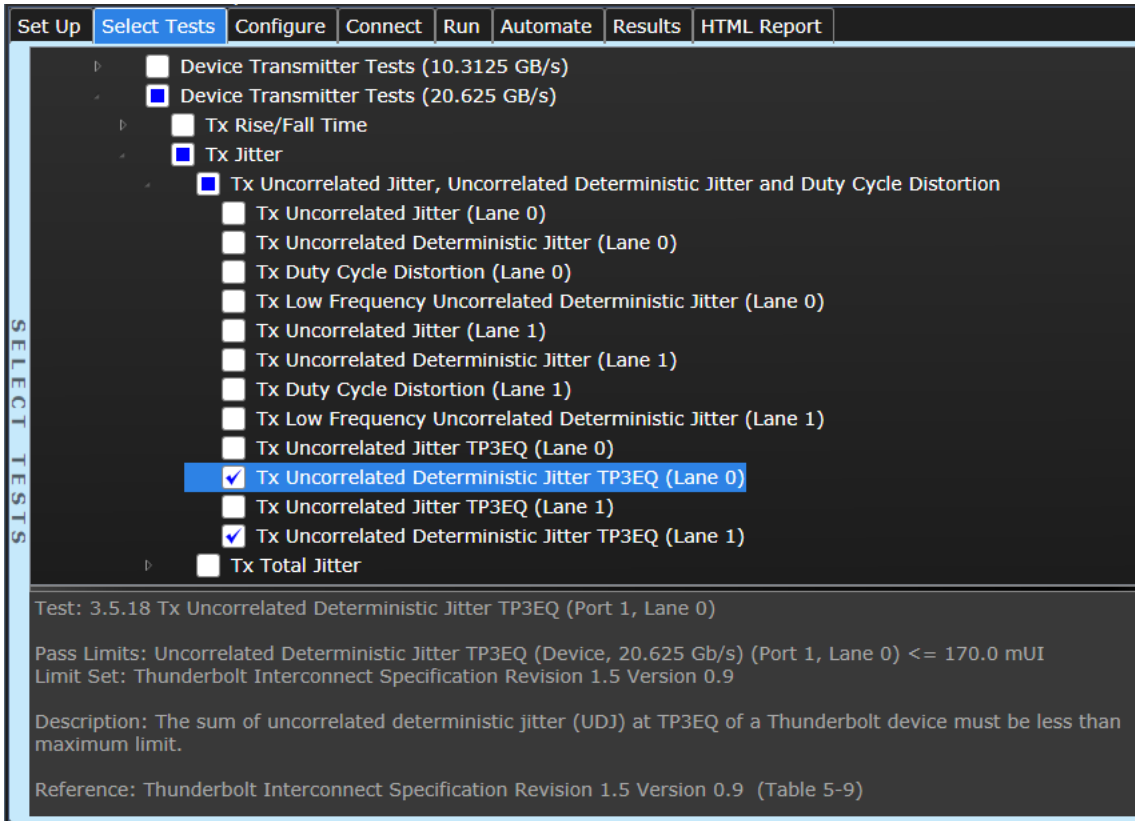


Figure 123 Selecting the Tx Uncorrelated Deterministic Jitter TP3EQ tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Embed the Type-C cable in the Oscilloscope. For Gen 3 systems, use TP3_EQ embedding file *TBT_0p8m.s4p*.
3 De-embed the cables from the test fixture to the Oscilloscope.
4 Ensure that measurements are done with a calibrated reference equalizer (CTLE only). See "Tx CTLE Calibration" on page 200.
5 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 21GHz
6 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display
7 Capture the values of Total Jitter (TJ_{TP3EQ}) and Data Deterministic Jitter (DDJ_{TP3EQ}).
8 Capture the UDJ_{TP3EQ} result (same as BUJ over the Oscilloscope).

9 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $UDJ_{TP3EQ} > 0.17\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.5.19 Gen3 UDJ TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-9 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Eye Diagram TP3EQ

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Eye Diagram TP3EQ Test is to confirm that the differential signal on each Thunderbolt differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram at TP3EQ should meet the conditions depicted in Figure 124.

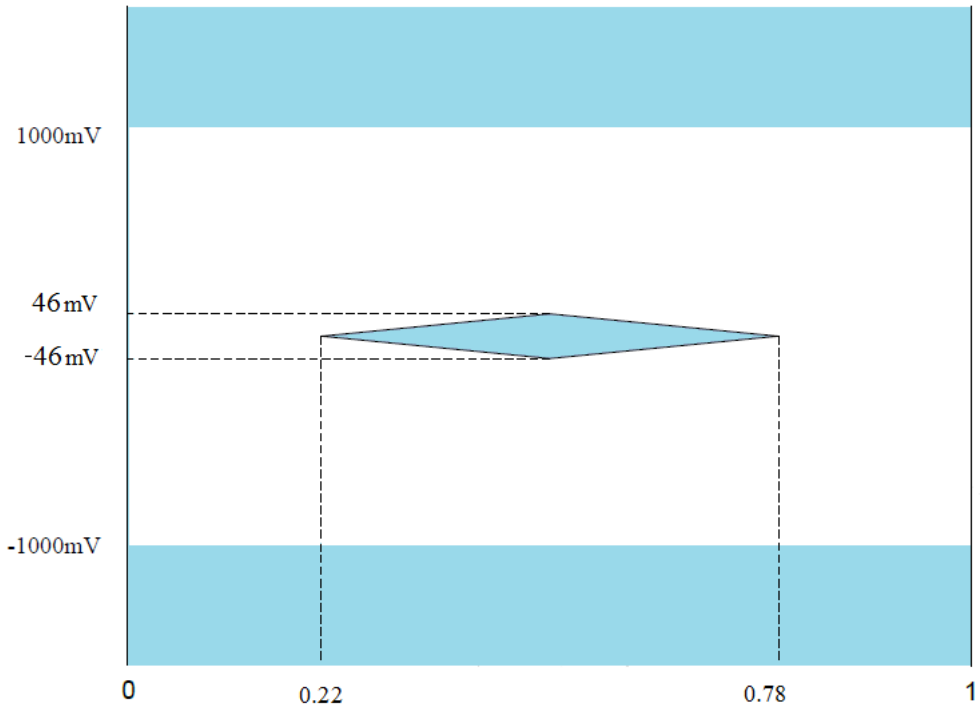


Figure 124 Pass Condition for Tx Eye Diagram TP3EQ Tests

(Refer to Table 9 on page 72 and Figure 41 on page 70).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Eye Diagram* are checked.

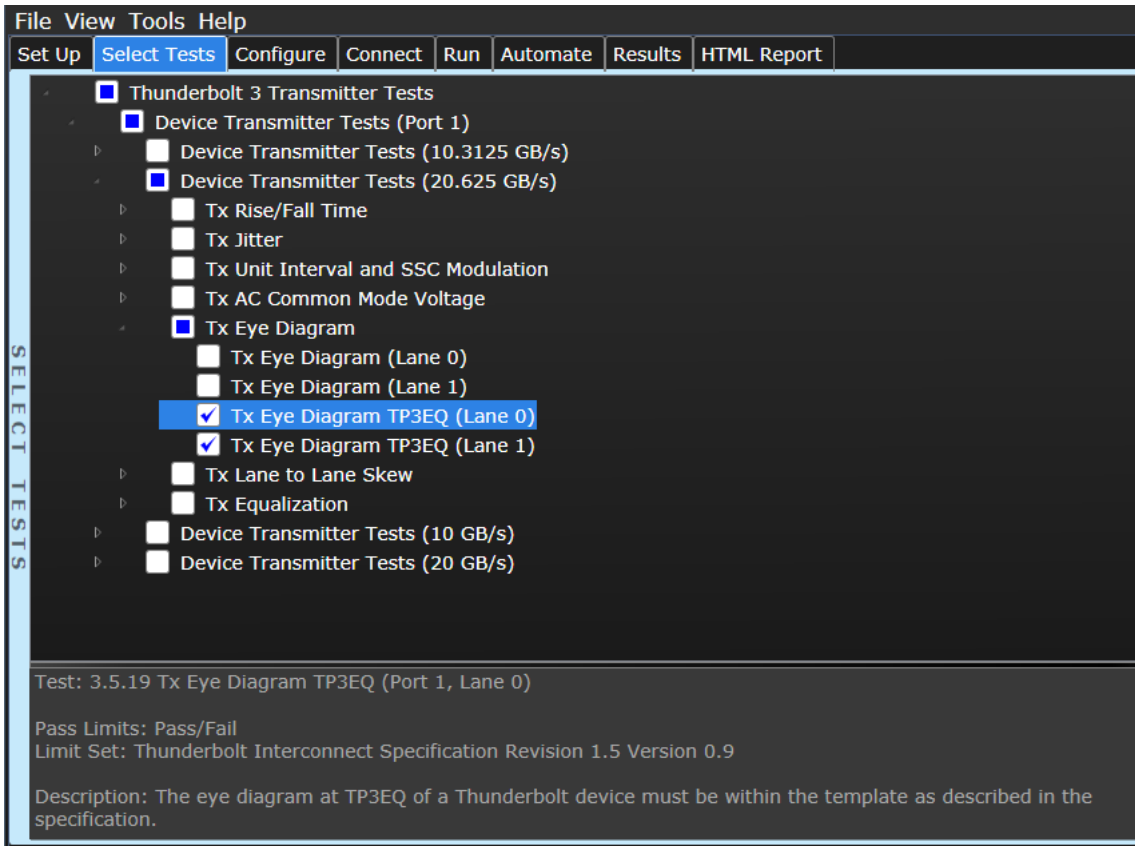


Figure 125 Selecting the Tx Eye Diagram TP3EQ tests

Test Procedure

1. Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2. Embed the Type-C cable in the Oscilloscope. For Gen 3 systems, use TP3_EQ embedding file *TBT_0p8m.s4p*.
3. De-embed the cables from the test fixture to the Oscilloscope.
4. Ensure that measurements are done with a calibrated reference equalizer (CTLE and DFE). See "Tx CTLE Calibration" on page 200.
5. Perform measurements with:
   a. Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b. Oscilloscope with a minimum bandwidth of 21GHz
6. Capture the waveform and process it with the Digital Oscilloscope:
   a. Sampling Rate $\geq$ 80 GSa/s
   b. Adjust vertical and horizontal scale such that the signal fits within the Oscilloscope's display
   c. Accumulate at 1E6 UI
7. Compare the data eye to the TP3EQ eye diagram mask. Check for conditions described in the section "Expected / Observable Results".
8. Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the high or low maximum voltage (+/-1000mV), the status of the test is FAIL.

ii If any part of the waveform hits the mask, the status of the test is FAIL.

Test References

See

- "Section 3.5.20 Gen3 Eye Diagram Measurement TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-9 and Figure 5-15 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Equalization Tests

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Equalization Tests is to confirm that the transmitter equalization is within the limits of the specification. The Tx Equalization Tests are further divided into three tests, namely:

- Tx Equalization Pre-shoot
- Tx Equalization Deemphasis
- Tx Swing Preset 15

Test Pass Requirement

Transmitter Swing: 3.5 ± 1dB (for preset 15 only)

Pre-shoot, De-Emphasis: ± 1dB for the following presets:

Table 13 Transmitter Equalization Presets

Preset Number	Pre-Shoot	De-Emphasis
0	0	0
1	0	-1.9
2	0	-3.6
3	0	-5.0
4	0	-8.4
5	0.9	0
6	1.1	-1.9
7	1.4	-3.8
8	1.7	-5.8
9	2.1	-8.0
10	1.7	0
11	2.2	-2.2
12	2.5	-3.6
13	3.4	-6.7
14	4.3	-9.3
15	1.7	-1.7

(Refer to Table 5 on page 66).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Equalization* are checked.

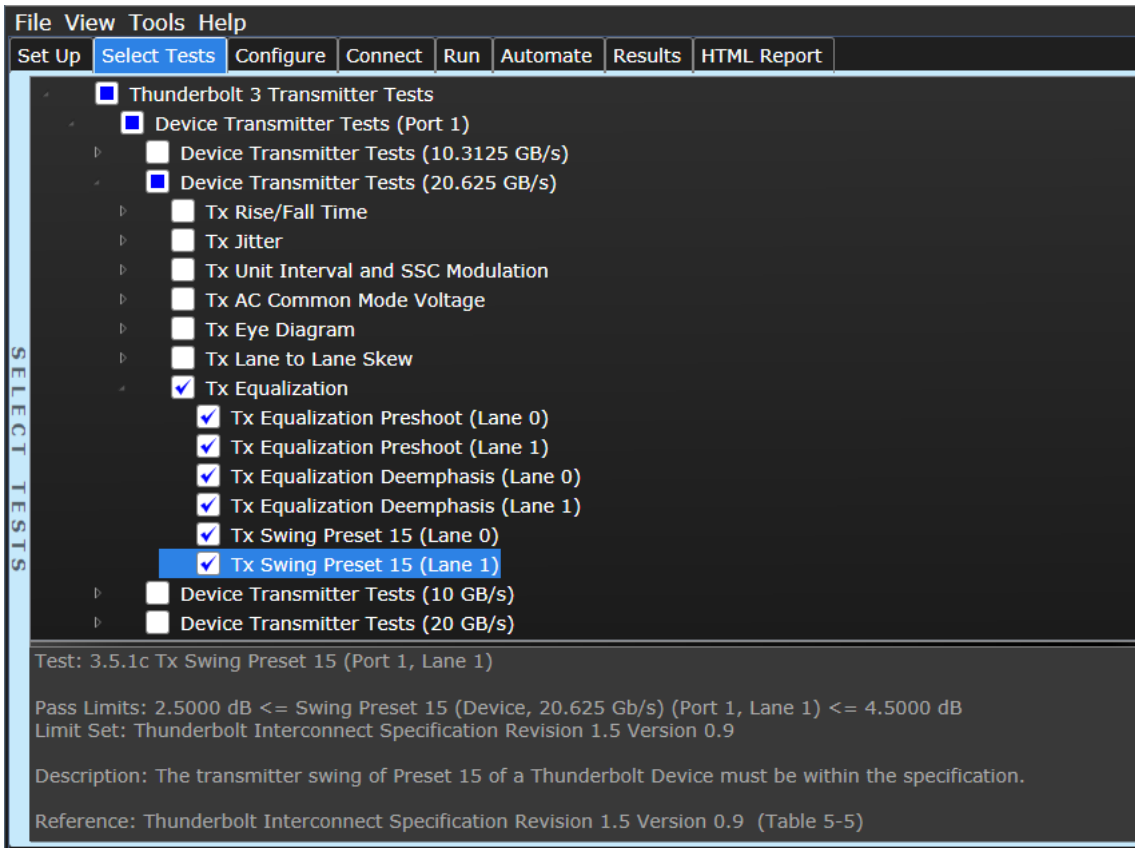


Figure 126 Selecting the Tx Equalization tests

4 Under the **Configure** tab of the Test Application, select **ALL** for the Configuration Variable “Tx Equalization” to run the tests for preset numbers P0 to P15.

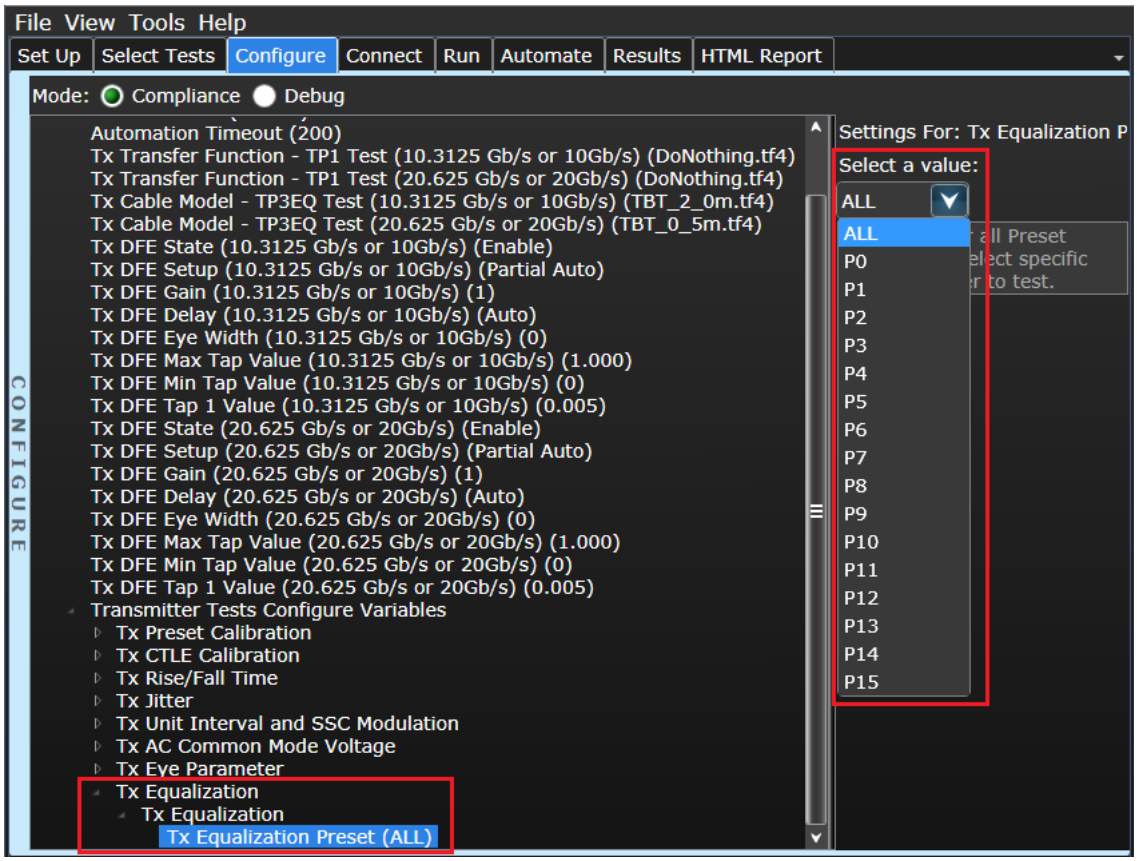


Figure 127 Configuring Tx Equalization Preset Variable

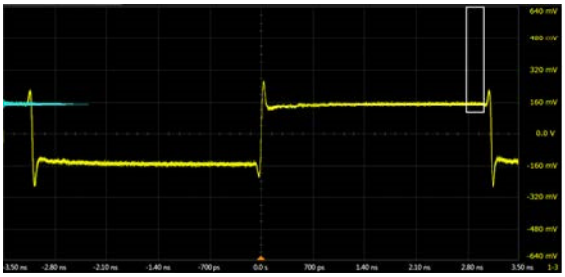
Test Procedure

1 Set Preset 0 (P0).

2 Configure the DUT transmitter to output alternating square pattern of 64 0’s and 64 1’s on all lanes with SSC enabled along with both pre-shoot and de-emphasis enabled.

3 Adjust vertical scale such that the signal fits within the Oscilloscope’s display.

4 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



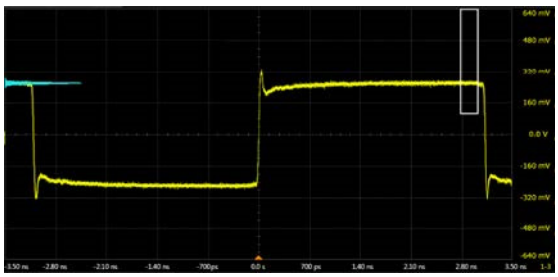
5 Measure differential amplitude voltage (V_1) for bits 57 to 62 using the equation:

$$V_1 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

6 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with de-emphasis enabled but no pre-shoot.

7 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

8 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



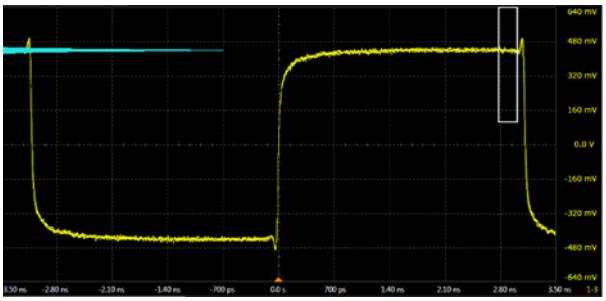
9 Measure differential amplitude voltage (V_2) for bits 57 to 62 using the equation:

$$V_2 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

10 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with pre-shoot enabled but no de-emphasis.

11 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

12 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



13 Measure differential amplitude voltage (V_3) for bits 57 to 62 using the equation:

$$V_3 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

$$\text{Set Pre-Shoot to be } 20 * \log_{10} [V_2/V_1]$$

$$\text{Set De-Emphasis to be } 20 * \log_{10} [V_1/V_3]$$

14 Repeat steps 2 to 10 for all Presets defined in Table 13.

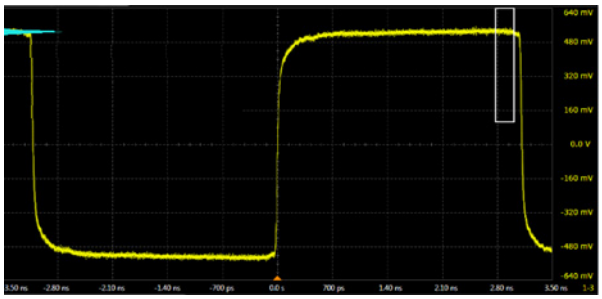
15 Check for PASS/FAIL conditions for both Pre-shoot and De-emphasis.

16 Set the DUT to Preset 0 (P0).

17 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

18 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

19 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



20 Measure differential amplitude voltage (V_0) for bits 57 to 62 using the equation:

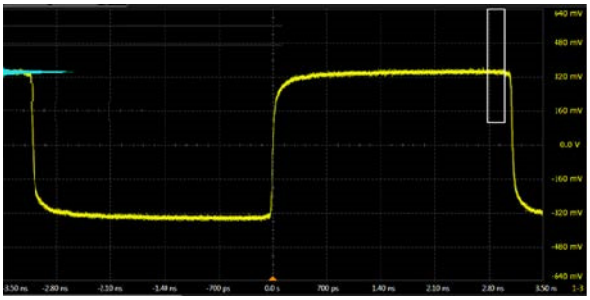
$$V_0 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

21 Set the DUT to Preset 15 (P15).

22 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

23 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

24 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



25 Measure differential amplitude voltage (V_{15}) for bits 57 to 62 using the equation:

$$V_{15} = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

Set Swing to be $20 * \log_{10} [V_0/V_{15}]$

26 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If the Pre-Shoot for a particular Preset number is not within ± 1dB of the matching value in Table 13, the status of test is FAIL.

If the De-Emphasis for a particular Preset number is not within ± 1dB of the matching value in Table 13, the status of test is FAIL.

If Swing < 2.5 dB or Swing > 4.5 dB, the status of test is FAIL.

Test References

See

- "Section 3.5.1 Transmitter Equalization" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-5 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

8 Transmitter Tests for 20 GB/s Systems

This section provides the Methods of Implementation (MOIs) to run electrical tests on a Thunderbolt DUT operating at a bit rate of 20 GB/s using an Keysight Infiniium Oscilloscope and other accessories, along with the Keysight D9030TBTC Thunderbolt 3 Test Application Methods of Implementation.

NOTE All Thunderbolt 3 devices that support a bit rate of 20 Gb/s are classified as Gen3 devices.

Tx Preset Calibration

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Preset Calibration Test is to find the optimized preset for the platform.

NOTE Prior to running the compliance tests, the Host / Device must go through Preset Calibration.

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Preset Calibration* are checked.

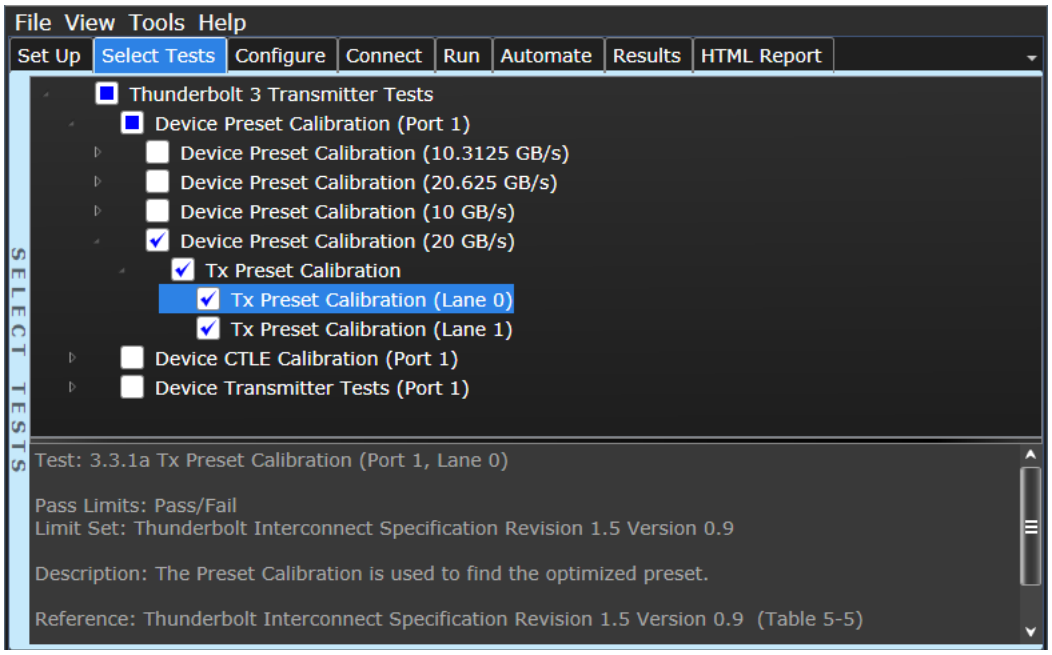


Figure 128 Selecting the Tx Preset Calibration tests

NOTE By default, the test group for **Preset Calibration** for each selected bit-rate is hidden in the **Select Tests** tab when **Predefined Optimum Preset Number** is selected for the respective bit-rates. To view and select the **Preset Calibration** tests in the **Select Tests** tab, select the **Run Preset Calibration** option in the **Test Setup** window of the **Set Up** tab.

Test Procedure

1 Connect the DUT to the Oscilloscope.
2 Configure the DUT transmitter to output PRBS31, preset 0 with SSC enabled.
3 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used.
   b Oscilloscope with a minimum bandwidth of 21GHz.
4 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Adjust vertical scale such that the signal fits within the Oscilloscope's display
   c Measured at 1E6 UI
5 Capture eye height and eye width for lane 0.
6 Register mean eye height and mean eye width values.
7 Repeat the test for the remaining Thunderbolt lanes.
8 Repeat the test for all remaining Thunderbolt transmit presets (till preset 15 as shown in Table 5).
9 For each lane, choose the preset that provides maximum eye width. If there are two presets with the same eye width, select the one with the greater eye height.

Expected / Observable Results

For each lane, the preset that provides the maximum eye width is the optimized preset for the platform. If two presets have the same eye width, the preset with a greater eye height is the optimized preset.

Test References

See

- "Section 3.3.1 Preset Calibration" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-5 of the *Thunderbolt™ Interconnect Specification Revision 1.5 Draft 0.8.*

Tx CTLE Calibration

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx CTLE Calibration Test is to find the optimized CTLE (Continuous-Time-Linear-Equalizer) for the platform.

See "Reference CTLE" on page 61 to know more about CTLE.

NOTE Apply equalization on the Oscilloscope, when testing at TP3EQ.

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx CTLE Calibration* are checked.

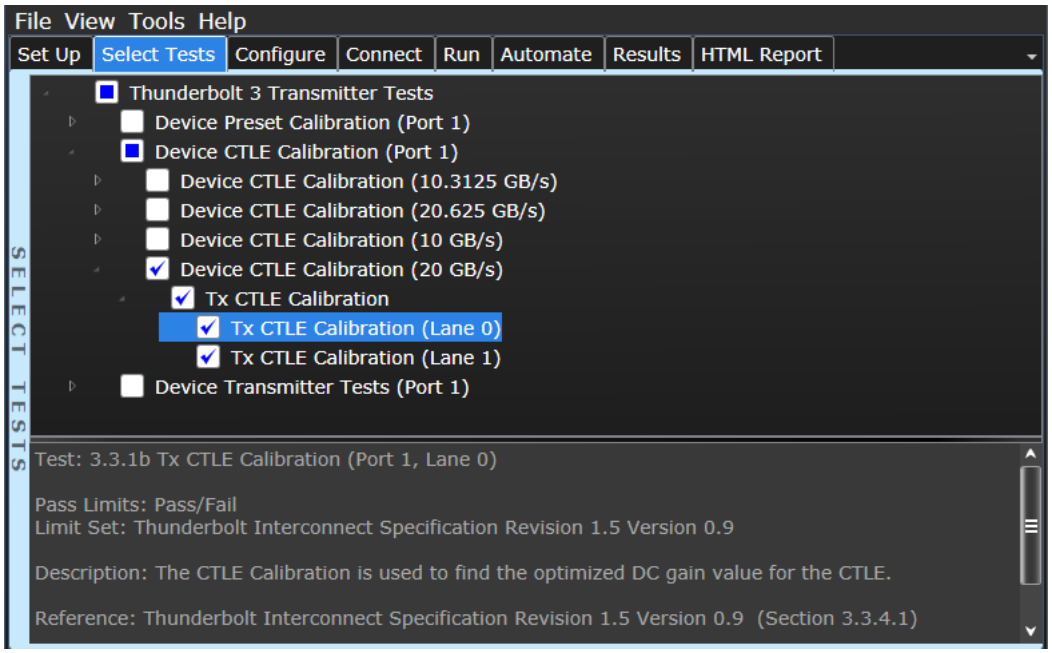


Figure 129 Selecting the Tx CTLE Calibration tests

NOTE By default, the test group for **CTLE Calibration** for each selected bit-rate is hidden in the **Select Tests** tab when **Predefined Optimum CTLE DC Gain Value** is selected for the respective bit-rates. To view and select the **CTLE Calibration** tests in the **Select Tests** tab, select the **Run CTLE Calibration** option in the **Test Setup** window of the **Set Up** tab.

Test Procedure

1 Follow the CTLE model as described in "Reference CTLE" on page 61, with the following parameters:

a AC Gain = 1.41

b Wp1 = 2 * π * 5G rad/sec

c Wp2 = 2 * π * 10G rad/sec

2 Apply ten different CTLE configurations such that A_{DC}, which is the DC Gain, is a value that lies within the following equation:

$$\{10^{-x/20} : x = 0 – 9\ [dB]\}$$

3 Calibrate A_{DC} using the following procedure:

a Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

b Select A_{DC} for x = 0.

c Perform measurement with Reference CDR based on the 2^{nd} order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used. Oscilloscope with a minimum bandwidth of 21GHz.

d Capture the waveform and process it with the Digital Oscilloscope:

- Sampling Rate $\geq$ 80 GSa/s
- Adjust vertical & horizontal scale such that the signal fits within the Oscilloscope's display
- Measured at 1E6 UI

e Eye height should be positioned at the "0" of the real time eye horizontal position.

f Apply a Histogram to the lower and upper sections of the eye, with ±1% deviation in time axis in order to calculate the eye height. Eye height is the delta between the minimum value from the upper histogram result (see Figure 130) and the maximum value from the lower histogram result (see Figure 131).

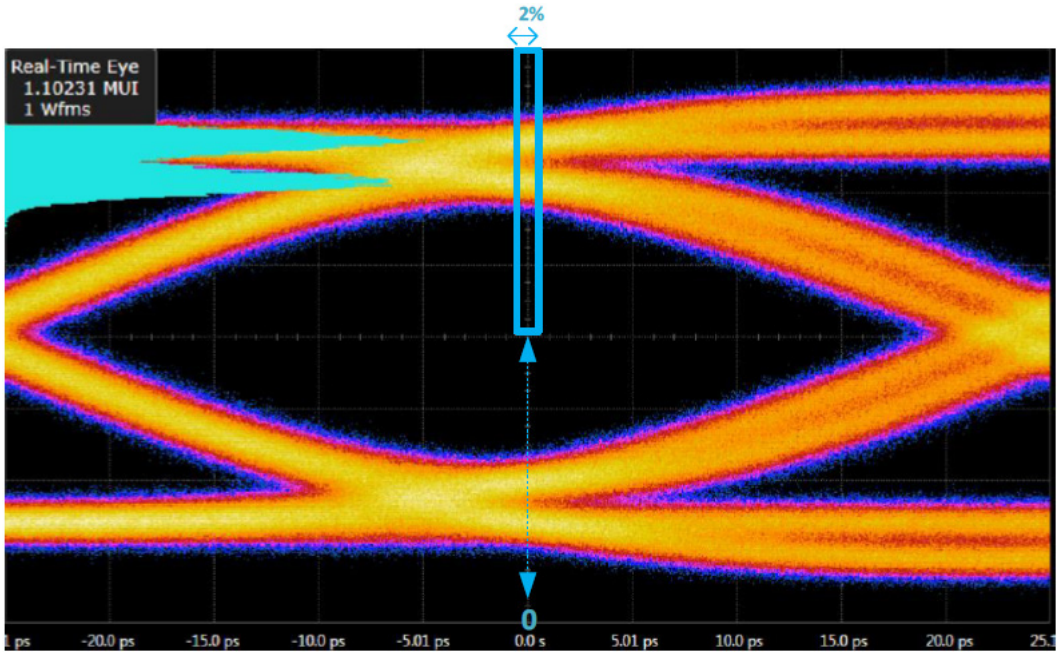


Figure 130 Thunderbolt RX TP3EQ Eye Height upper location measurement

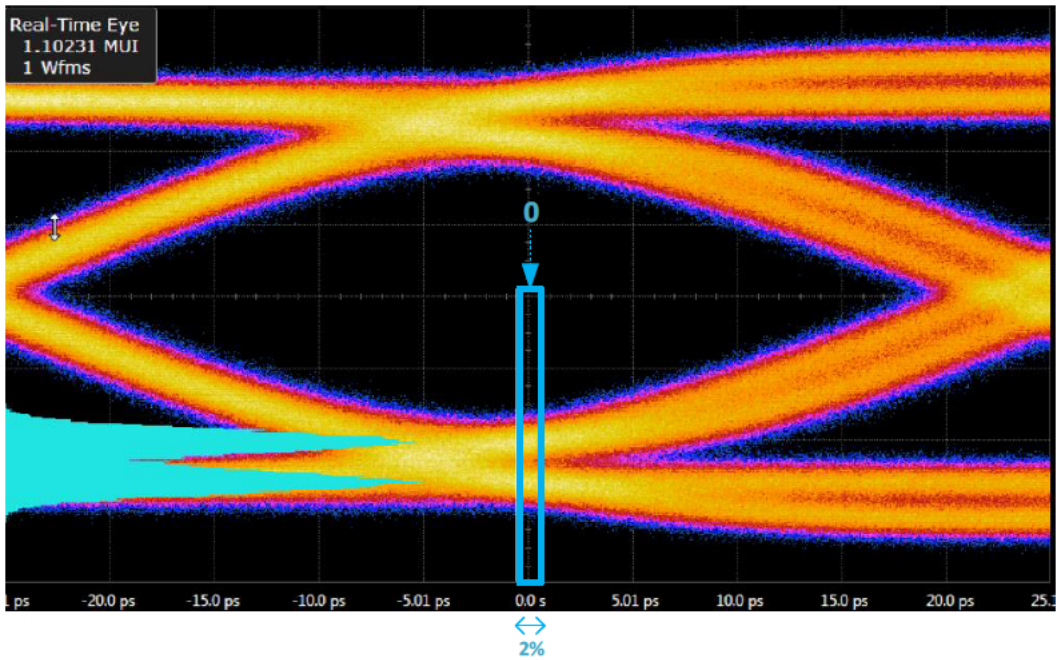


Figure 131 Thunderbolt RX TP3EQ Eye Height lower location measurement

g Capture five times (each time over new 1MUI record length) the minimum value of both eye height and eye width.

h Average the five captured values, that is, average of (5 times minimum eye height) and average of (5 times minimum eye width).

i Repeat this procedure from step 3b to 3i with x = x + 1 upto x = 9.

j Measure that value of A_{DC} (including DFE tap value), which yields the maximum eye height. If there are two values of A_{DC} (including DFE tap value), which have the same eye height, select the one that has the greater eye width.

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

For each lane, the DC Gain value that provides the maximum eye height is the optimized CTLE for the platform. If two DC Gain values have the same eye height, the one with a greater eye width is the optimized CTLE.

Test References

See

- "Section 8.2 Appendix C – Equalization Calibration" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9.*
- Section 3.3.4.1 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Rise/Fall Time

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Rise/Fall Time Test is to confirm that the rise times and fall times on the Thunderbolt differential signals are within the limits of the specification.

Test Pass Requirement

Rise Time and Fall Time ≥ 10ps (Refer to Table 4 on page 64).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Rise/Fall Time* are checked.

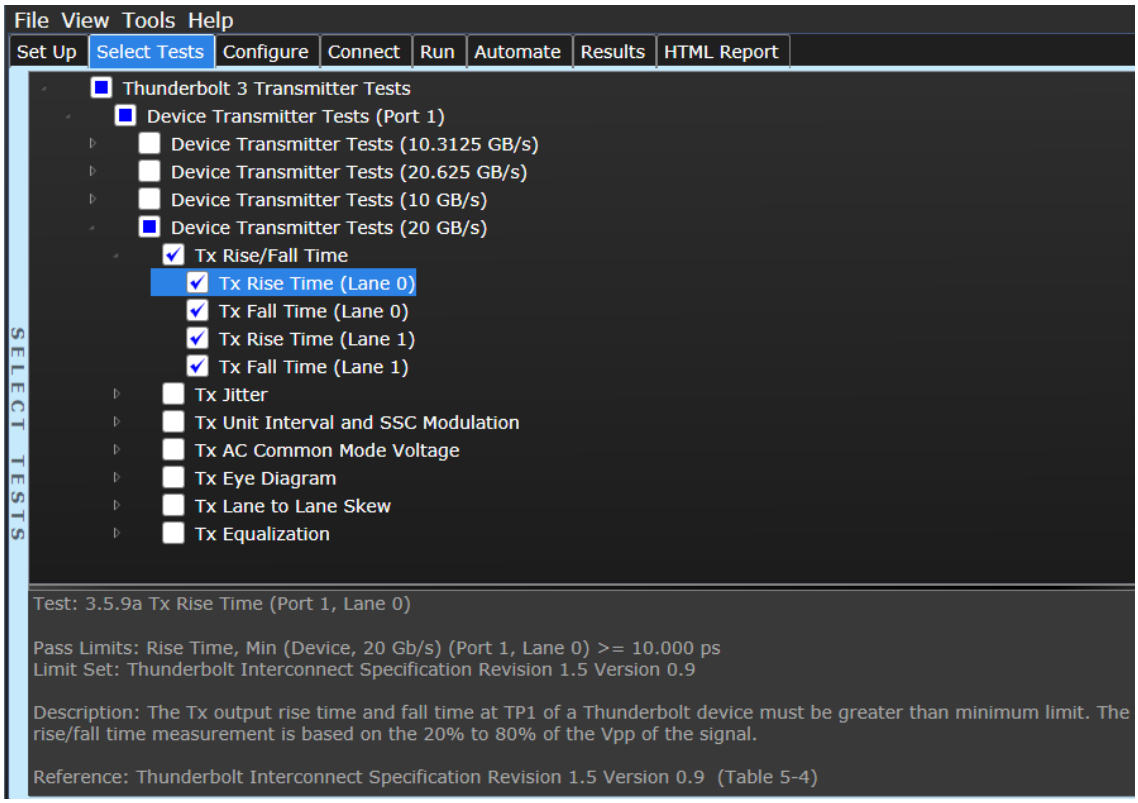


Figure 132 Selecting the Tx Rise/Fall Time tests

Test Procedure

1 Configure the DUT transmitter to output alternating square pattern of 16 0's and 16 1's on all lanes with SSC enabled.
2 Evaluate at least 4Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 4Mpts. Use the maximum analog bandwidth of the Oscilloscope.

   No CDR, no average and no interpolation to be used.

   Adjust vertical scale such that the signal fits within the Oscilloscope's display.
3 Measure T_{RISE} as the mode of the sampled edge times from 20% to 80% of the differential swing voltage rising edge.
4 Measure T_{FALL} as the mode of the sampled edge times from 80% to 20% of the differential swing voltage falling edge.
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If T_{RISE} < 10ps, the status of test is FAIL.

If T_{FALL} < 10ps, the status of test is FAIL.

Test References

See

- "Section 3.5.9 Gen3 Rise/Fall Time Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Total Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Total Jitter Test is to confirm that the Total Jitter of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of 1×10^{-13}.

Test Pass Requirement

Total Jitter (TJ) $\leq$ 0.46 UI_{p-p} (Refer to Table 8 on page 71).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Total Jitter* are checked.

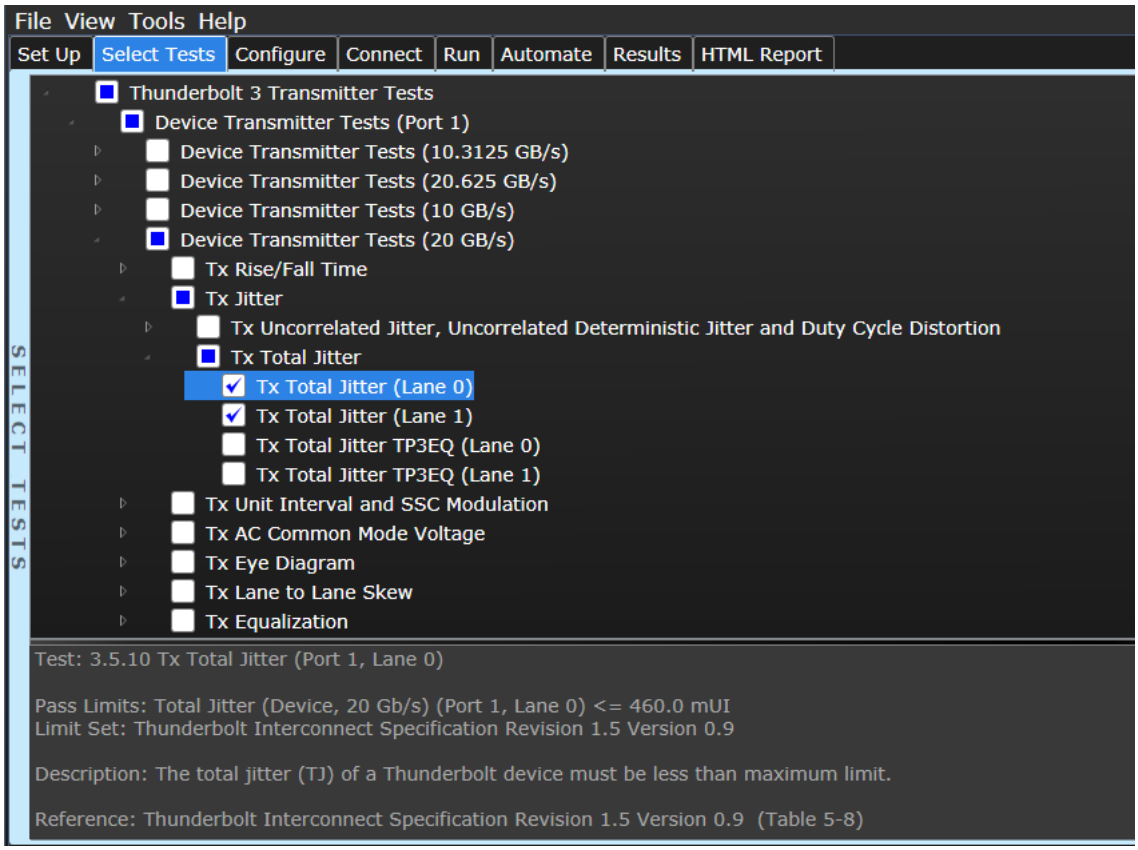


Figure 133 Selecting the Tx Total Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   b Oscilloscope with a minimum bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display.
   f Referenced to 1E-13 statistics.
4 Capture the values of Total Jitter (TJ) and Deterministic Jitter (DJ).
5 If TJ > 0.46 UI_{p-p}, perform the following steps:
   a Configure the DUT transmitter to output alternating square pattern of one 0's and one 1's on all lanes with SSC enabled. (The pattern is SQ2 instead of PRBS15).
   b Perform measurements with:

- Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
- Oscilloscope with a minimum bandwidth of 21GHz

c Capture the waveform and process it with the Digital Oscilloscope:

- Sampling Rate $\geq$ 80 GSa/s
- Pattern length – Periodic
- Jitter Separation method must be suitable for cross-talk on the signal
- Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
- Adjust vertical scale such that the signal fits within the Oscilloscope's display.
- Referenced to 1E-13 statistics.

d Capture the Random Jitter (RJ) result.

e Calculate TJ using the equation:

TJ = DJ + 14.7 * RJ (DJ from #4; PRBS15 and RJ from #5d; SQ2)

6 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If TJ > 0.46 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.5.10 Gen3 Total Jitter" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Uncorrelated Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Jitter Test is to confirm that the Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Jitter (UJ) $\leq$ 0.31 UI_{p-p} (Refer to Table 8 on page 71).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

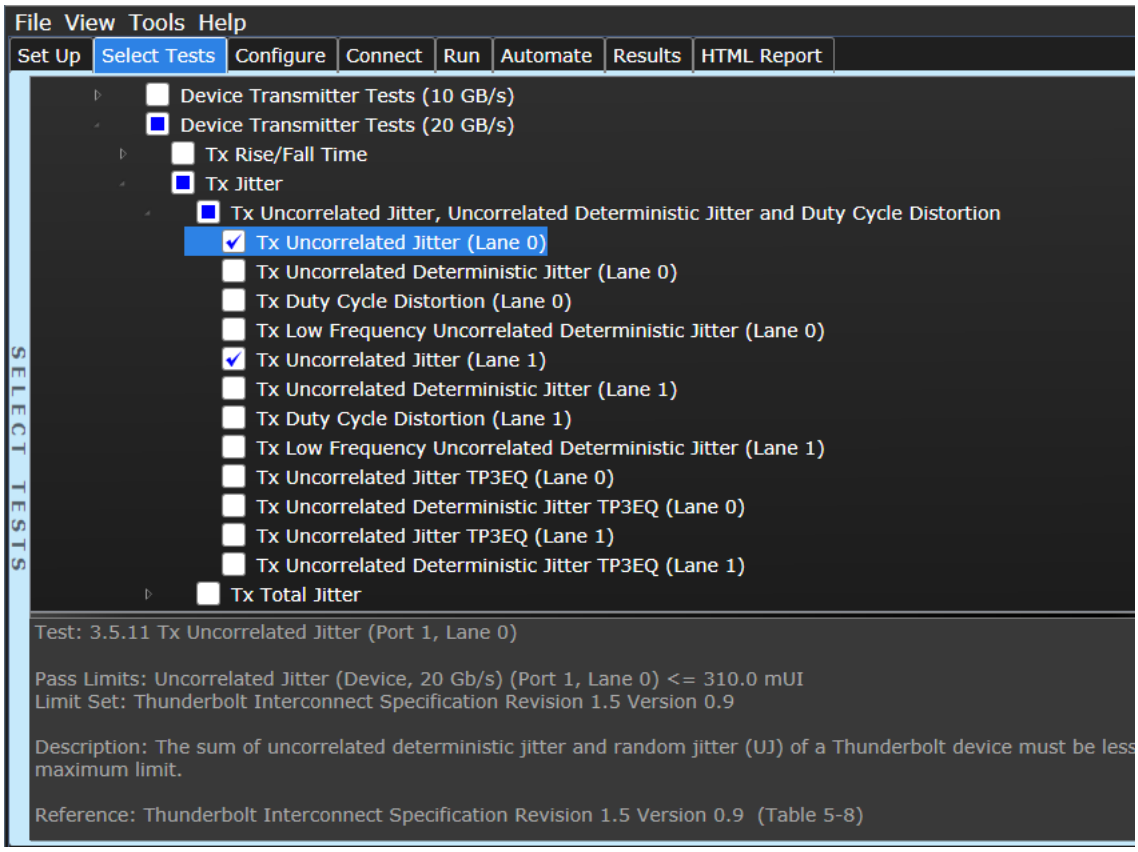


Figure 134 Selecting the Tx Uncorrelated Jitter tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Perform measurements with:
   - *a* Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   - *b* Oscilloscope with a bandwidth of 21GHz
3. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Pattern length – Periodic
   - *c* Jitter Separation method must be suitable for cross-talk on the signal
   - *d* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *e* Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   - *f* Referenced to 1E-13 statistics
4. Capture the Total Jitter (TJ) and Data Dependent Jitter (DDJ) results.
5. Calculate UJ using the equation:

$$UJ = TJ - DDJ$$

6. Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UJ > 0.31 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.5.11 Gen3 UJ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Uncorrelated Deterministic Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Deterministic Jitter Test is to confirm that the Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Deterministic Jitter (UDJ) $\leq$ 0.17 UI_{p-p} (Refer to Table 8 on page 71).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

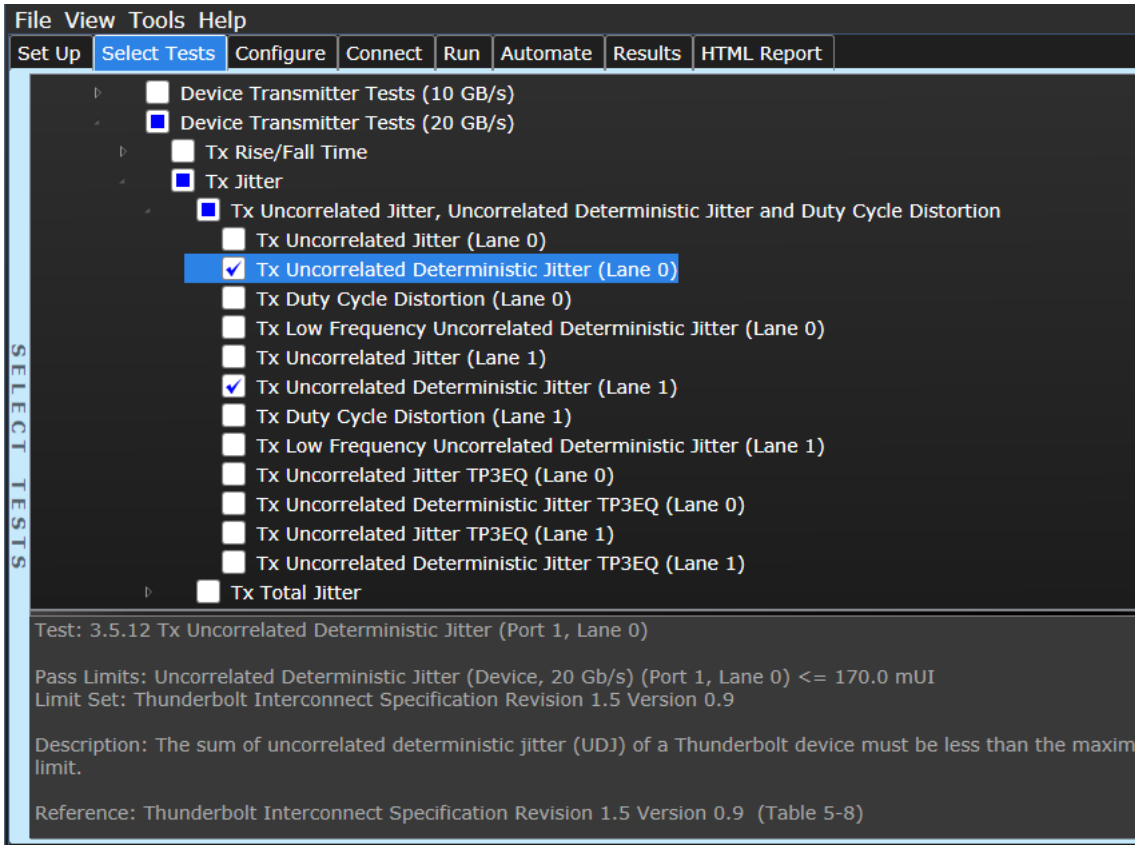


Figure 135 Selecting the Tx Uncorrelated Deterministic Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   f Referenced to 1E-13 statistics
4 Capture the UDJ result (same as BUJ over the Oscilloscope).
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UDJ > 0.17 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.5.12 Gen3 UDJ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Low Frequency Uncorrelated Deterministic Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Low Frequency Uncorrelated Deterministic Jitter Test is to confirm that the Low Frequency Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Low Frequency Uncorrelated Deterministic Jitter (UDJ_LF) $\leq$ 0.07 UI_{p-p} (Refer to Table 8 on page 71).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

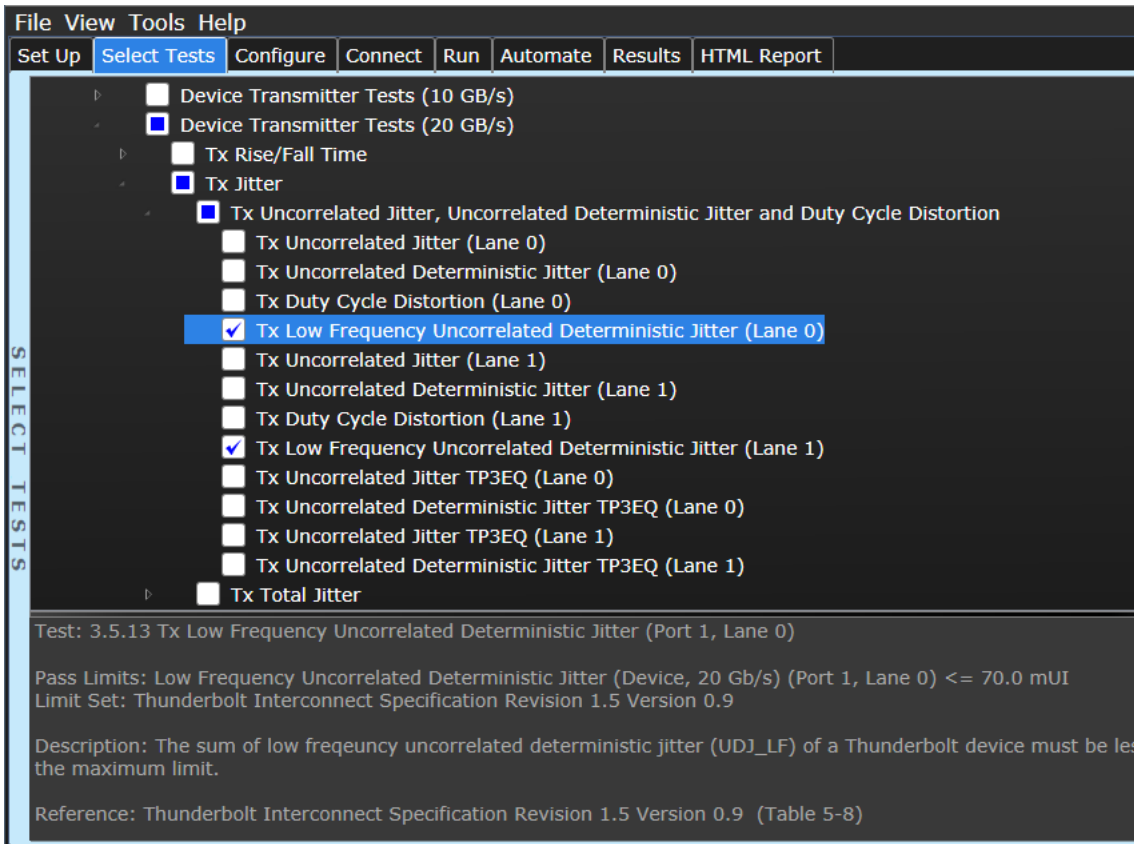


Figure 136 Selecting the Tx Low Frequency Uncorrelated Deterministic Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   b Apply 2nd order Low-Pass-Filter with 3 dB cut-off at 2MHz; no average and no interpolation to be used
   c Oscilloscope with a bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate ≥ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
4 Capture the UDJ_LF result.
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UDJ_LF > 0.07 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.5.13 Gen3 Low Frequency UDJ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Duty Cycle Distortion

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Duty Cycle Distortion Test is to confirm that the transmitter Deterministic Jitter Associated by Duty-Cycle-Distortion Jitter falls within the limits of the specification.

Test Pass Requirement

Duty-Cycle-Distortion (DCD) ≤ 0.03UIp-p (Refer to Table 6 on page 68).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

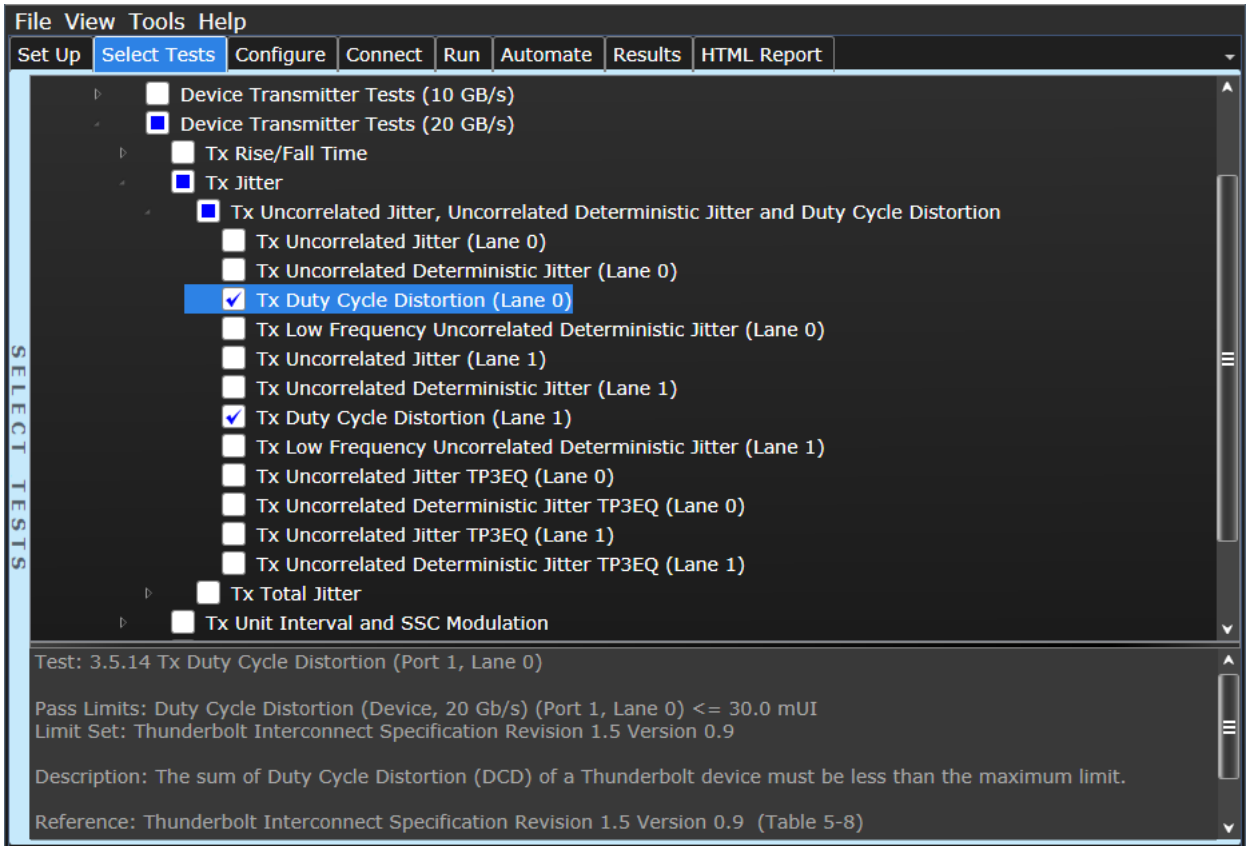


Figure 137 Selecting the Tx Duty Cycle Distortion tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.

2 Perform measurements with:

a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used

b Oscilloscope with a minimum bandwidth of 21GHz

3 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate $\geq$ 80 GSa/s

b Pattern length – Periodic

c Jitter Separation method must be suitable for cross-talk on the signal

d Adjust vertical scale such that the signal fits within the Oscilloscope's display

e Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts.

4 Capture the DCD result.

5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If DCD > 0.03UIp-p, the status of test is FAIL.

Test References

See

- "Section 3.5.14 Gen3 DCD Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Unit Interval

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Unit Interval Test is to confirm that the data rate, under all conditions, does not exceed the minimum or maximum limits of the specification.

Test Pass Requirement

G3_UI_MIN ≤ Unit Interval ≤ G3_UI_MAX (Refer to Table 8 on page 71).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

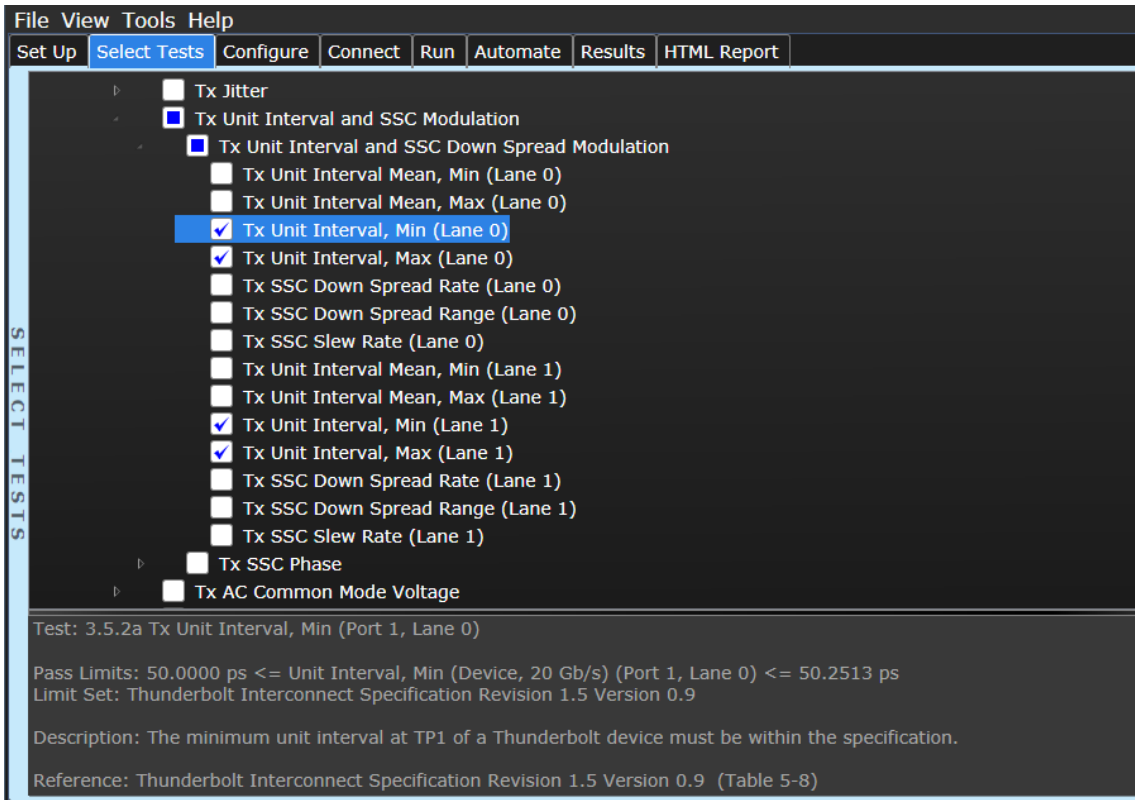


Figure 138 Selecting the Tx Unit Interval tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 21GHz
3 Calculate UI dynamically using a uniform moving average filter procedure with a window size of 6000 symbols.
4 Measure the values of both UI_{MAX} and UI_{MIN}.
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UI_{MAX} > G3_UI_MAX, the status of test is FAIL.

If UI_{MIN} < G3_UI_MIN, the status of test is FAIL.

Test References

See

- "Section 3.5.2 Unit Interval Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Unit Interval Mean

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Unit Interval Mean Test is to confirm that the average data rate, under all conditions, does not exceed the minimum or maximum limits of the specification.

Test Pass Requirement

G3_UI_MEAN_MIN ≤ Average Unit Interval ≤ G3_UI_MEAN_MAX (Refer to Table 8 on page 71).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

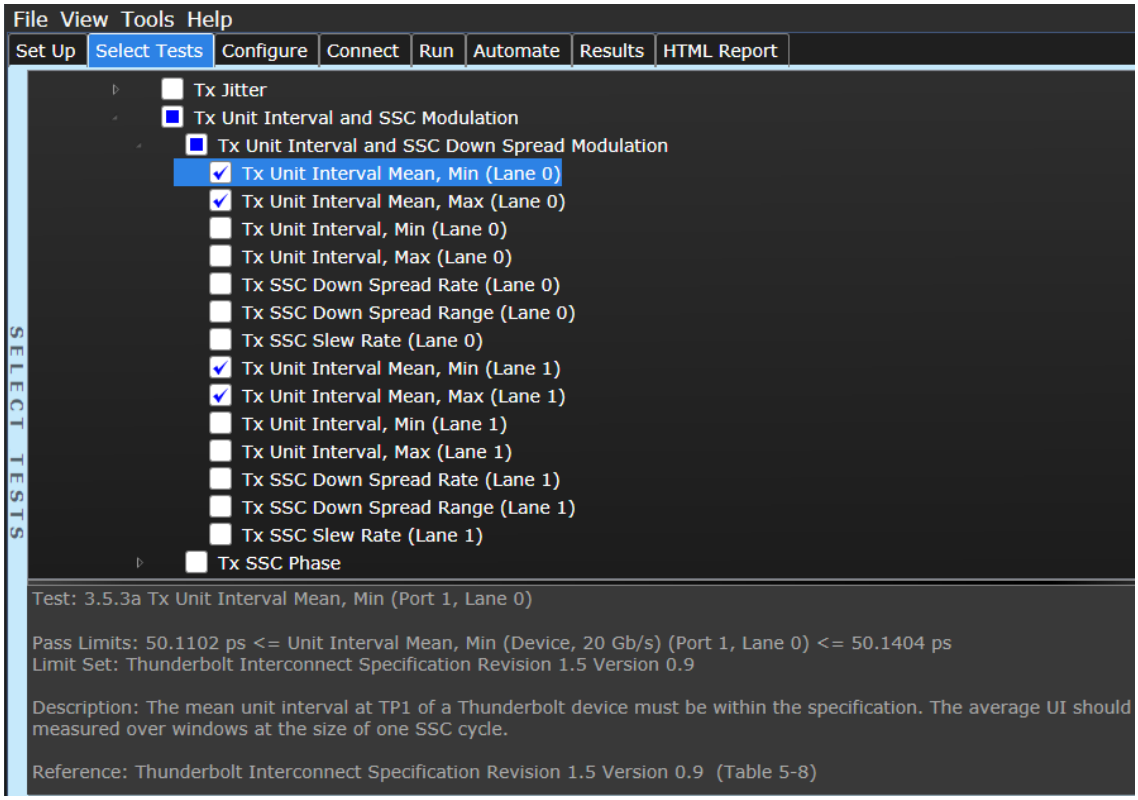


Figure 139 Selecting the Tx Unit Interval Mean tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate ≥ 80 GSa/s

b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts

c No CDR, no average and no interpolation to be used

d Adjust vertical scale such that the signal fits within the Oscilloscope's display

e Oscilloscope must have a minimum bandwidth of 21GHz

3 Use mathematical analysis to measure the average unit interval over a window of the size of one SSC cycle, determined by the SSC_Down_Spread_Rate.

4 Measure UI_MEAN over different windows that uniformly cover the Oscilloscope capture for at least 300ms (more than 10 SSC Cycles) with 10000 UI window jumps. See Figure 140.

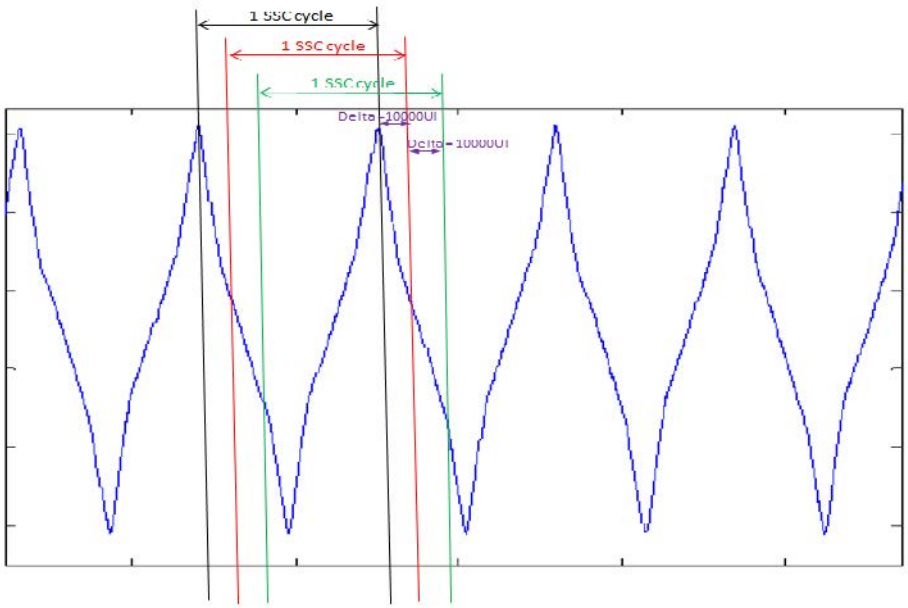


Figure 140 Measurement of UI_MEAN over at least 10 SSC Cycles

5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If the maximum UI_MEAN measured > G3_UI_MEAN_MAX, the status of test is FAIL.

If the minimum UI_MEAN measured < G3_UI_MEAN_MIN, the status of test is FAIL.

Test References

See

- "Section 3.5.3 Gen3 Unit Interval Mean Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx SSC Down Spread Range

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Down Spread Range Test is to confirm that the data down spreading is within the limits of the specification.

Test Pass Requirement

0.4% ≤ SSC_Down_Spread_Range ≤ 0.5% (Refer to Table 4 on page 64).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

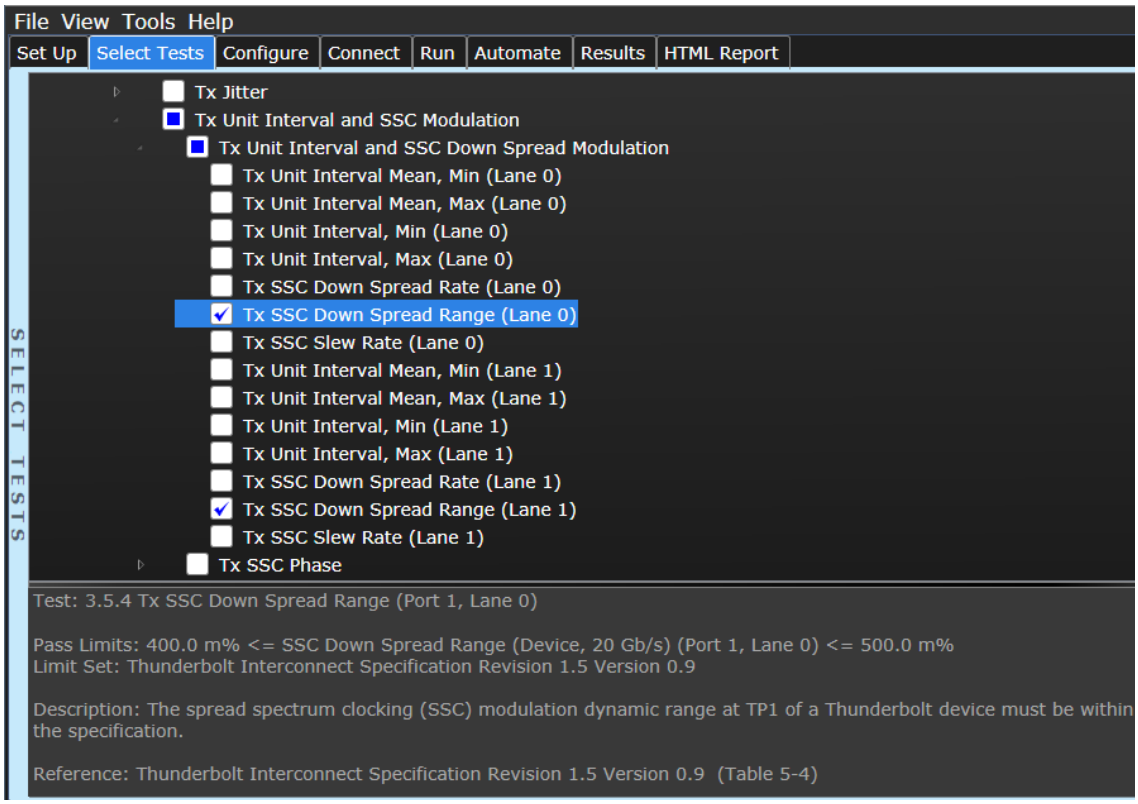


Figure 141 Selecting the Tx SSC Down Spread Range tests

Test Procedure

1. Run the "Tx Unit Interval" Test as a prerequisite to obtain UI_{MAX} and UI_{MIN}.
2. Use the obtained value of UI_{MAX} and UI_{MIN} to calculate the Deviation percentage:

$$\text{Maximum Deviation} = 100*\{[20G - (1 / UI_{MAX})] / 20G\}$$

$$\text{Minimum Deviation} = 100*\{[20G - (1 / UI_{MIN})] / 20G\}$$

3. Calculate SSC Down Spread Range using the equation:

$$\text{Maximum Deviation - Minimum Deviation}$$

4. Repeat the test for all remaining Thunderbolt lanes.

Expected / Observable Results

If SSC_Down_Spread_Range > 0.5% or SSC_Down_Spread_Range < 0.4%, the status of test is FAIL.

Test References

See

- "Section 3.5.4 SSC Down Spread Deviation Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx SSC Down Spread Rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Down Spread Rate Test is to confirm that the Link clock down-spreading modulation rate is within the limits of the specification.

Test Pass Requirement

SSC_DSR_MIN ≤ SSC_Down_Spread_Rate ≤ SSC_DSR_MAX (Refer to Table 4 on page 64).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

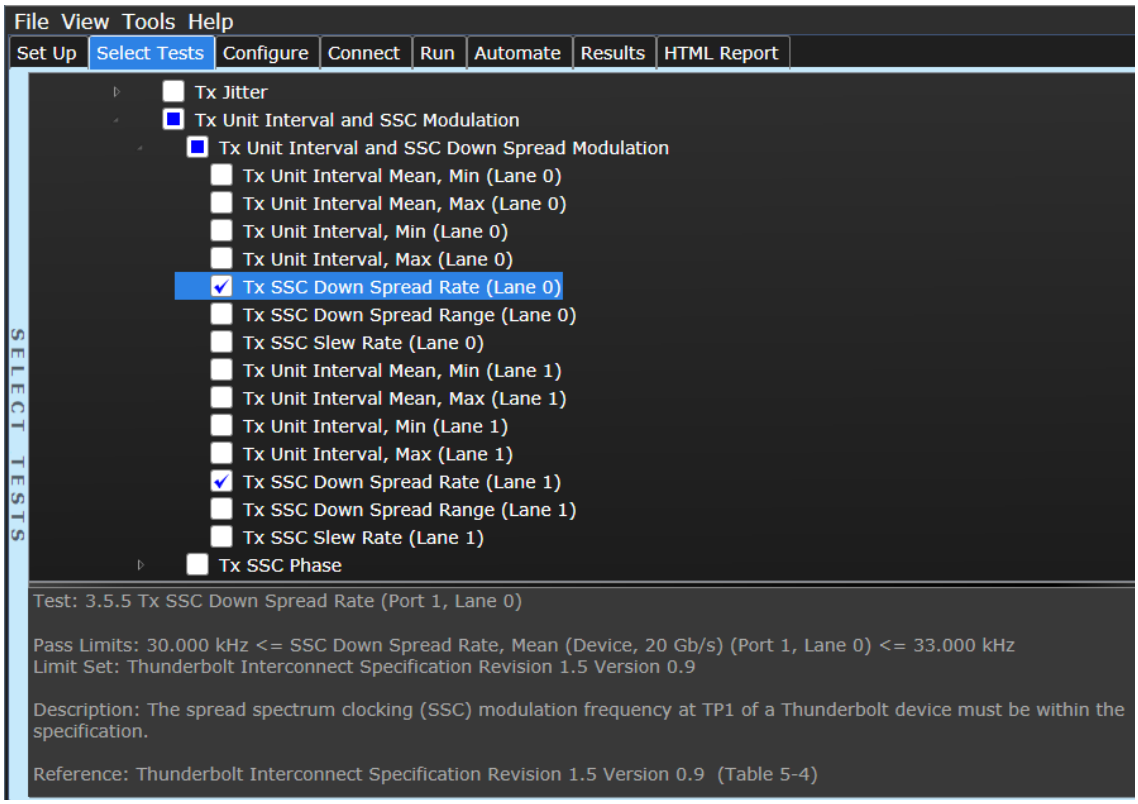


Figure 142 Selecting the Tx SSC Down Spread Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 21GHz
3 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If SSC_DSR_MIN > SSC_Down_Spread_Rate > SSC_DSR_MAX, the status of test is FAIL.

Test References

See

- "Section 3.5.5 Gen3 SSC Down Spread Rate Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx SSC Phase Deviation

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Phase Deviation Test is to confirm that the SSC Phase Deviation is within the limits of the specification.

Test Pass Requirement

2.5ns p-p ≤ SSC_Phase_Deviation ≤ SSC_PD_MAX (Refer to Table 4 on page 64).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx SSC Phase* are checked.

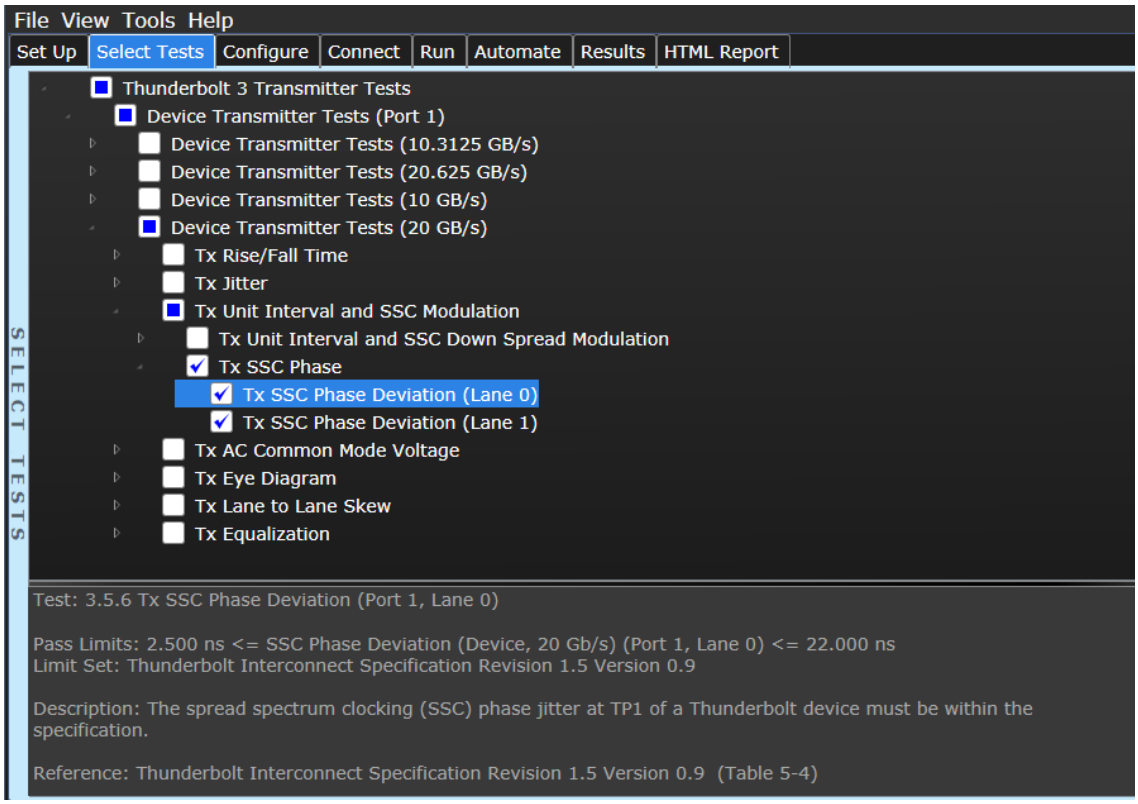


Figure 143 Selecting the Tx SSC Phase Deviation tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope's software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 21GHz
3 Extract the SSC Phase Deviation from the transmitted signal.
4 Extract the SSC Phase Deviation from the phase jitter after applying a 2^{nd} order low-pass filter with 3dB point at 2 MHz.
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If 2.5ns p-p > SSC_Phase_Deviation > SSC_PD_MAX the status of test is FAIL.

Test References

See

- "Section 3.5.6 Gen3 SSC Phase Deviation Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx SSC Slew Rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Slew Rate Test is to confirm that the SSC Slew Rate is within the limits of the specification.

Test Pass Requirement

SSC_Slew_Rate ≤ 1000 ppm/µs (Refer to Table 4 on page 64).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

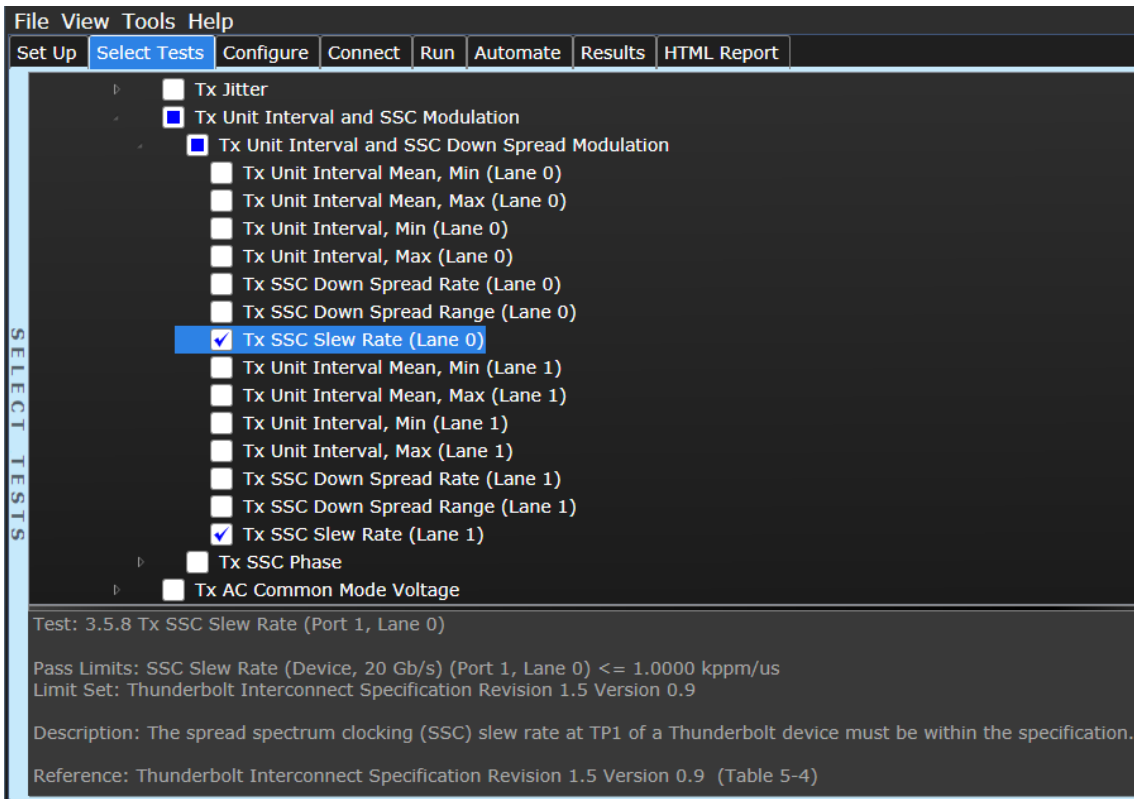


Figure 144 Selecting the Tx SSC Slew Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and post process it with an appropriate software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Extract SSC slew rate from the transmitted signal over measurement intervals of 0.5µs
   f Extract SSC slew rate from the phase information after applying a 2nd order Low-Pass-Filter with 3 dB cut-off at 2MHz.
   g Oscilloscope must have a minimum bandwidth of 21GHz
3 SSC_Slew_Rate is measured as the SSC frequency deviation over time while valid data is being transmitted in which 1E-12 bit error rate is required without assuming forward error correction.
4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If SSC_Slew_Rate > 1000 ppm/µs, the status of test is FAIL.

Test References

See

- "Section 3.5.7 Gen3 SSC Slew Rate Data Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Lane to Lane Skew

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Lane to Lane Skew Test is to confirm that the Skew between dual transmit signals of the same port group falls within the limits of the specification.

Test Pass Requirement

Lane_to_Lane_Skew ≤ 26nS (Refer to Table 4 on page 64).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Lane to Lane Skew* are checked.

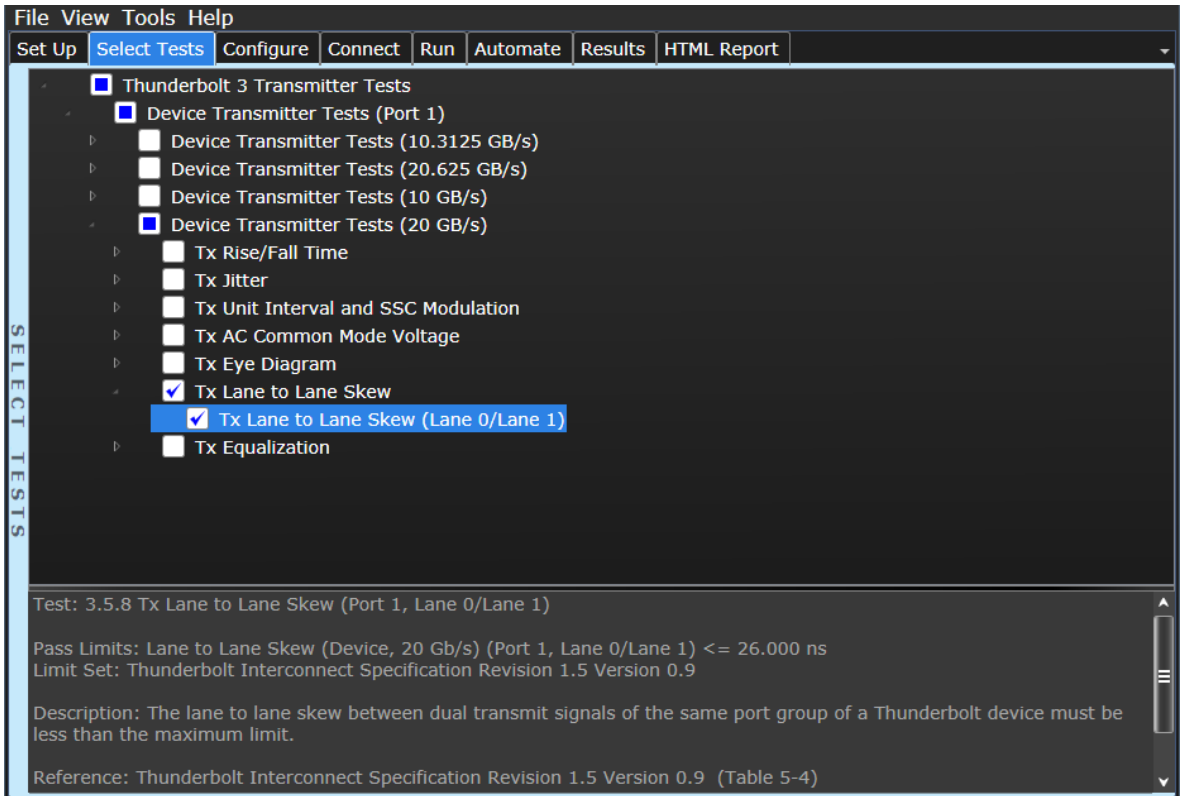


Figure 145 Selecting the Tx Lane to Lane Skew tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveforms from 2 lanes from the same port together and post process it with an appropriate software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 10Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 10Mpts.
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Measurement must be performed between consecutive rising edges
   f Oscilloscope must have a minimum bandwidth of 21GHz
3 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If Lane_to_Lane_Skew > 26nS, the status of test is FAIL.

Test References

See

- "Section 3.5.8 Gen3 Lane to Lane Skew Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5, Version 0.9*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9.*

Tx Eye Diagram

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Eye Diagram Test is to confirm that the differential signal on each Thunderbolt differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram should meet the conditions depicted in Figure 146.

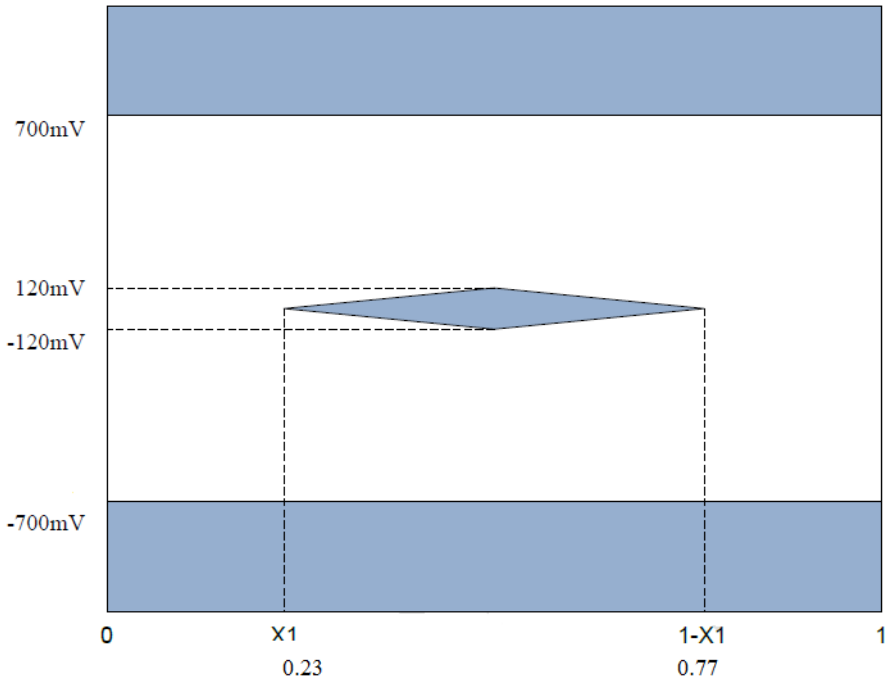


Figure 146 Pass Condition for Tx Eye Diagram Tests

(Refer to Table 8 on page 71 and Figure 41 on page 70).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Eye Diagram* are checked.

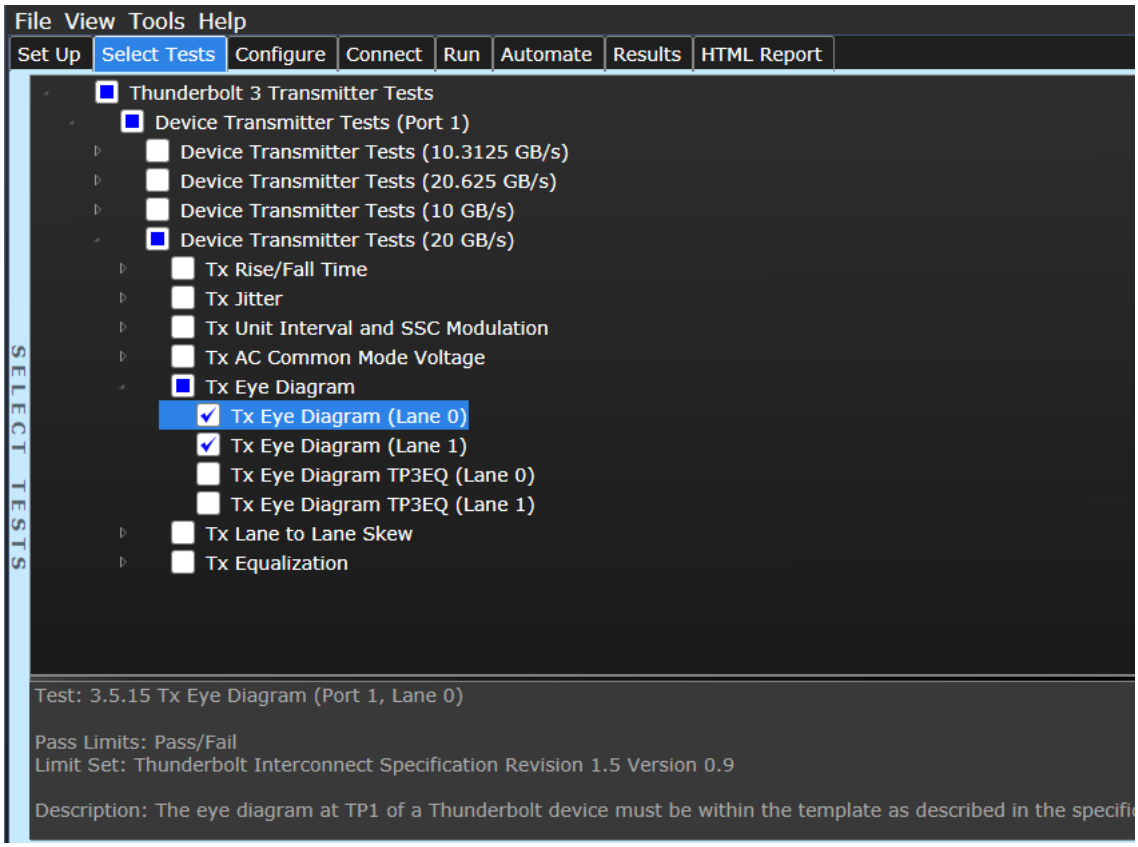


Figure 147 Selecting the Tx Eye Diagram tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Perform measurements with:

a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used

b Oscilloscope with a minimum bandwidth of 21GHz

3 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate $\geq$ 80 GSa/s

b Adjust vertical scale such that the signal fits within the Oscilloscope's display

c Measured at 1E6 UI

4 Compare the data eye to the TP1 eye diagram mask. Check for conditions described in the section "Expected / Observable Results".

5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the inner or outer height voltage (+/- 700mV), the status of the test is FAIL.

ii If any part of the waveform hits the mask, the status of the test is FAIL.

Test References

See

- “Section 3.5.16 Gen3 Eye Diagram Measurement” of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-8 and Figure 5-15 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx AC Common Mode Voltage

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx AC Common Mode Voltage Test is to confirm that the transmitter common mode on the Thunderbolt differential signals is within the limits of the specification.

Test Pass Requirement

TX AC Common Mode Voltage $\leq 100mV_{p-p}$ (Refer to Table 8 on page 71).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx AC Common Mode Voltage* are checked.

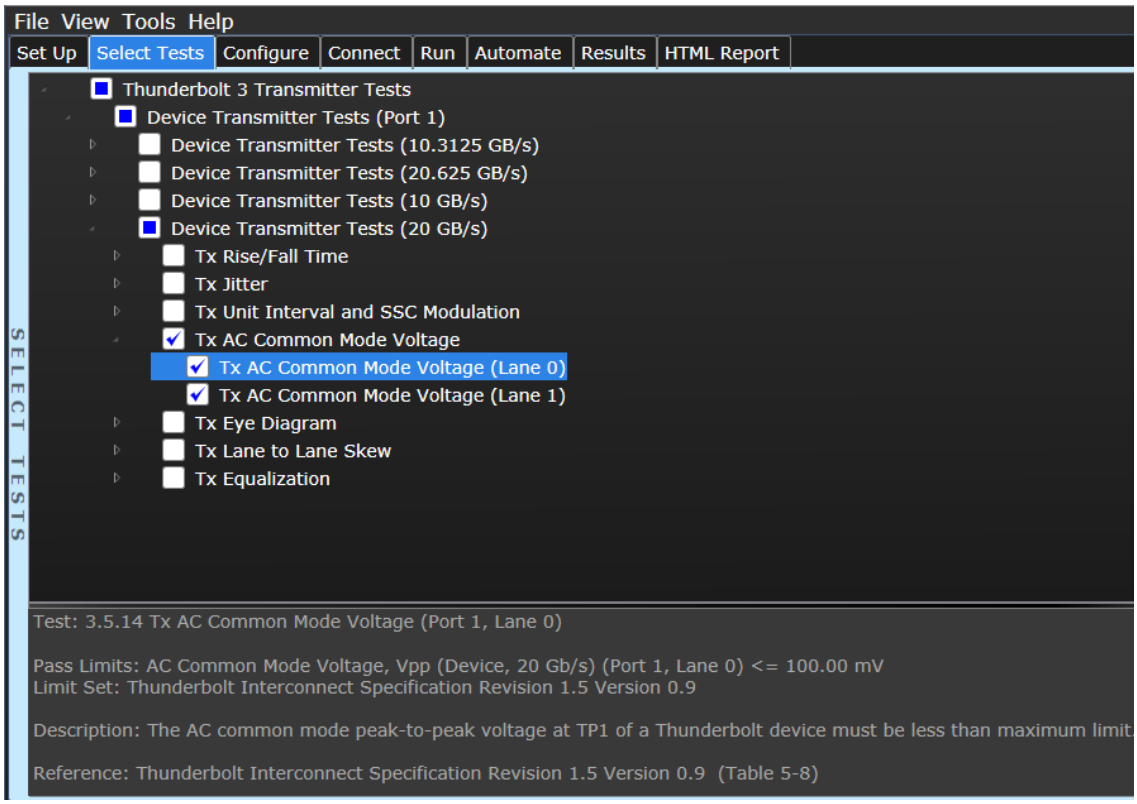


Figure 148 Selecting the Tx AC Common Mode Voltage tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Oscilloscope must have a bandwidth of 21±1GHz
3 Calculate the AC Common Mode Voltage (V_{AC-CM}) using the equation:

$$V_{AC-CM} = (V_{TX-P} + V_{TX-N}) / 2$$

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $V_{AC-CM} > 100mV_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.5.15 Gen3 AC Common Mode Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Total Jitter TP3EQ

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Total Jitter TP3EQ Test is to confirm that the Total Jitter at point TP3EQ of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of $1x10^{-13}$.

Test Pass Requirement

Total Jitter (TJ_{TP3EQ}) $\leq$ 0.60 UI_{p-p} (Refer to Table 9 on page 72).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Total Jitter* are checked.

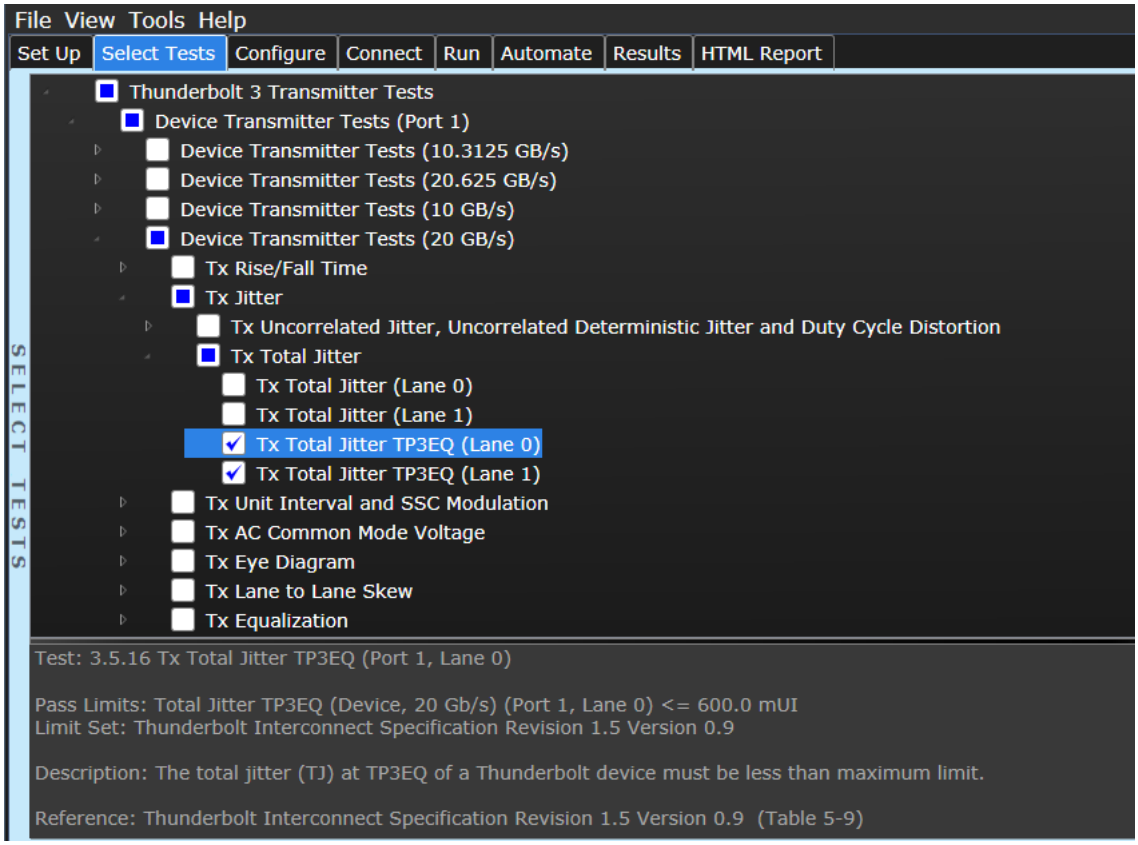


Figure 149 Selecting the Tx Total Jitter TP3EQ tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Embed the Type-C cable in the Oscilloscope. For Gen 3 systems, use TP3_EQ embedding file *TBT_0p8m.s4p*.
3 De-embed the cables from the test fixture to the Oscilloscope.
4 Ensure that measurements are done with a calibrated reference equalizer (CTLE only). See "Tx CTLE Calibration" on page 260.
5 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a bandwidth of 21GHz
6 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate ≥ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display
   f Referenced to 1E-13 statistics

7 Capture the values of Total Jitter (TJ_{TP3EQ}) and Deterministic Jitter (DJ_{TP3EQ}).

8 If $TJ_{TP3EQ} > 0.60\ UI_{p-p}$, perform the following steps:

a Configure the DUT transmitter to output alternating square pattern of one 0's and one 1's on all lanes with SSC enabled. (The pattern is SQ2 instead of PRBS15).

b Perform measurements with:

- Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
- Oscilloscope with a minimum bandwidth of 21GHz

c Capture the waveform and process it with the Digital Oscilloscope:

- Sampling Rate $\geq$ 80 GSa/s
- Pattern length – Periodic
- Jitter Separation method must be suitable for cross-talk on the signal
- Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
- Adjust vertical scale such that the signal fits within the Oscilloscope's display.
- Referenced to 1E-13 statistics.

d Capture the Random Jitter (RJ_{TP3EQ}) result.

e Calculate TJ_{TP3EQ} using the equation:

$TJ_{TP3EQ} = DJ_{TP3EQ} + 14.7 * RJ_{TP3EQ}$ (DJ_{TP3EQ} from #7; PRBS15 and RJ_{TP3EQ} from #8d; SQ2)

9 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $TJ_{TP3EQ} > 0.60\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.5.17 Gen3 Total Jitter TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-9 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Uncorrelated Jitter TP3EQ

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Jitter TP3EQ Test is to confirm that the Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] at point TP3EQ of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Jitter (UJ_{TP3EQ}) $\leq$ 0.31 UI_{p-p} (Refer to Table 9 on page 72).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

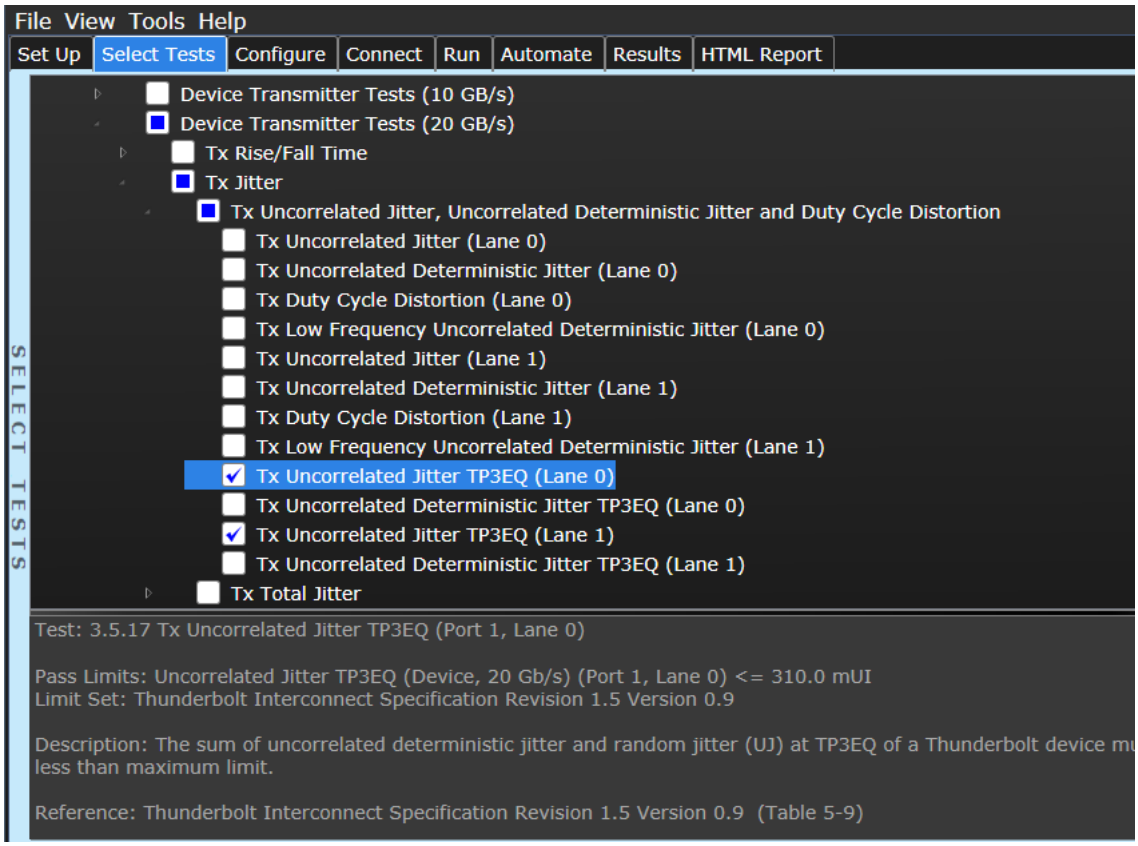


Figure 150 Selecting the Tx Uncorrelated Jitter TP3EQ tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Embed the Type-C cable in the Oscilloscope. For Gen 3 systems, use TP3_EQ embedding file *TBT_0p8m.s4p*.
3. De-embed the cables from the test fixture to the Oscilloscope.
4. Ensure that measurements are done with a calibrated reference equalizer (CTLE only). See "Tx CTLE Calibration" on page 260.
5. Perform measurements with:
   - *a* Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   - *b* Oscilloscope with a minimum bandwidth of 21GHz
6. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Pattern length – Periodic
   - *c* Jitter Separation method must be suitable for cross-talk on the signal
   - *d* Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   - *e* Adjust vertical scale such that the signal fits within the Oscilloscope's display

7 Capture the values of Total Jitter (TJ_{TP3EQ}) and Data Deterministic Jitter (DDJ_{TP3EQ}).

8 Capture the UDJ_{TP3EQ} result (same as BUJ over the Oscilloscope).

9 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $UDJ_{TP3EQ} > 0.17\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.5.18 Gen3 UJ TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-9 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Uncorrelated Deterministic Jitter TP3EQ

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Deterministic Jitter TP3EQ Test is to confirm that the Uncorrelated Deterministic Jitter at point TP3EQ of the transmitter is within the limits of the specification.

Test Pass Requirement

Deterministic Jitter that is uncorrelated to the transmitted data (UDJ_{TP3EQ}) $\leq$ 0.17 UI_{p-p} (Refer to Table 9 on page 72).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.
3. Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

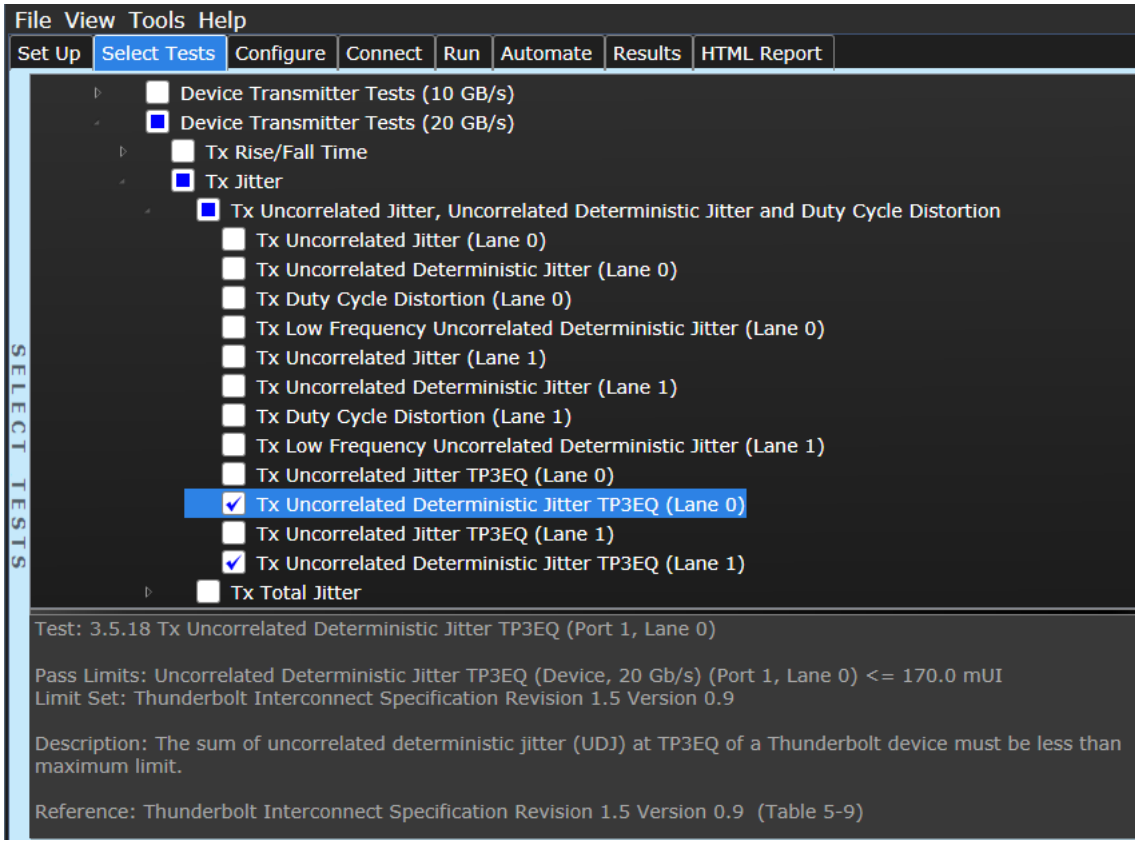


Figure 151 Selecting the Tx Uncorrelated Deterministic Jitter TP3EQ tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Embed the Type-C cable in the Oscilloscope. For Gen 3 systems, use TP3_EQ embedding file *TBT_0p8m.s4p*.
3 De-embed the cables from the test fixture to the Oscilloscope.
4 Ensure that measurements are done with a calibrated reference equalizer (CTLE only). See "Tx CTLE Calibration" on page 260.
5 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 21GHz
6 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ration to 27Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display
7 Capture the values of Total Jitter (TJ_{TP3EQ}) and Data Deterministic Jitter (DDJ_{TP3EQ}).

8 Capture the UDJ_{TP3EQ} result (same as BUJ over the Oscilloscope).

9 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $UDJ_{TP3EQ} > 0.17\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.5.19 Gen3 UDJ TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-9 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Eye Diagram TP3EQ

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Eye Diagram TP3EQ Test is to confirm that the differential signal on each Thunderbolt differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram at TP3EQ should meet the conditions depicted in Figure 152.

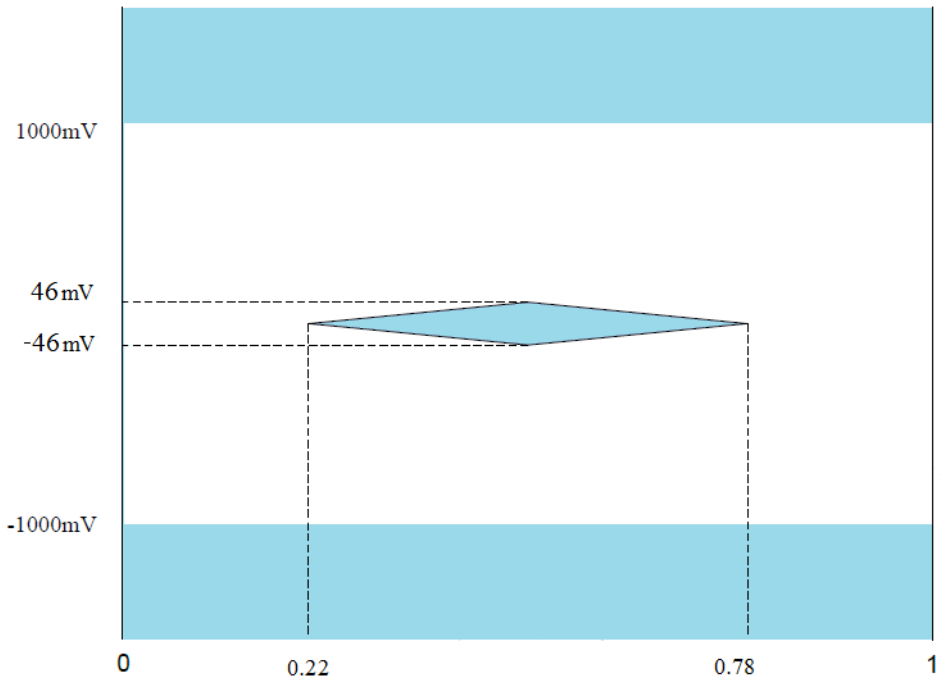


Figure 152 Pass Condition for Tx Eye Diagram TP3EQ Tests

(Refer to Table 9 on page 72 and Figure 41 on page 70).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see "Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Eye Diagram* are checked.

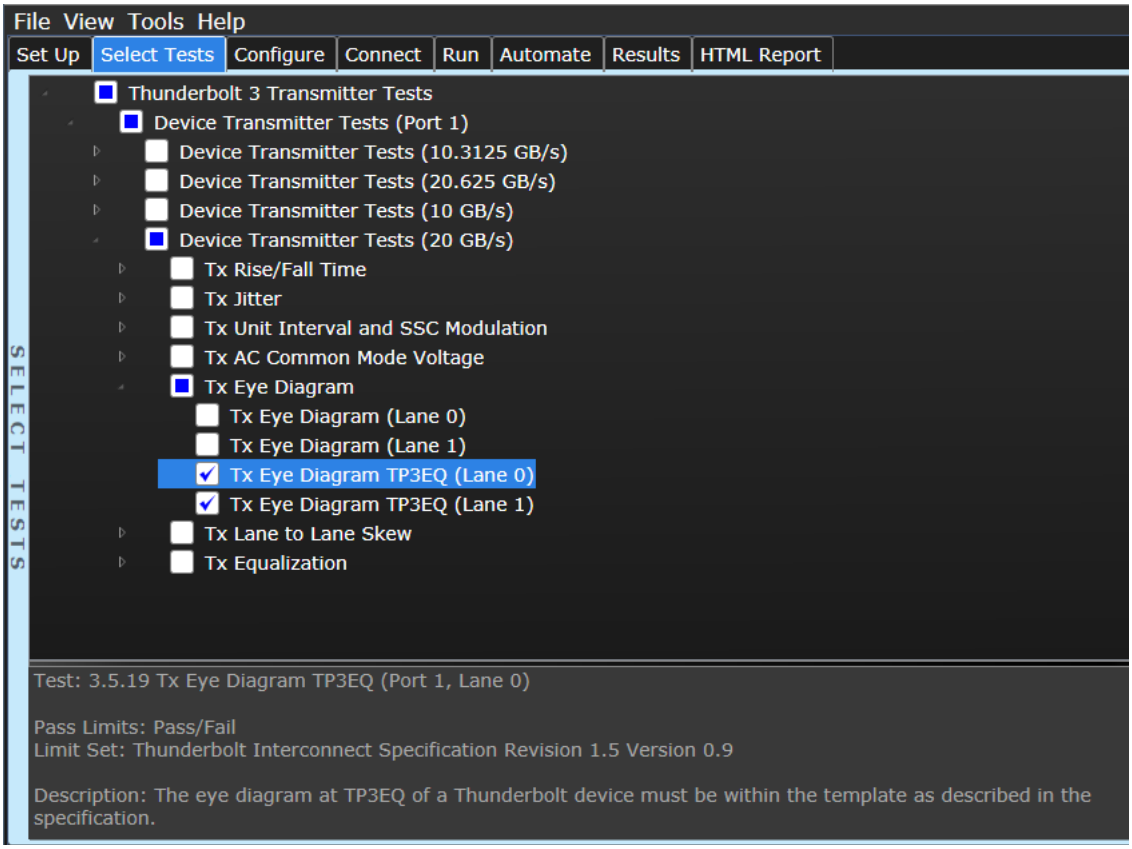


Figure 153 Selecting the Tx Eye Diagram TP3EQ tests

Test Procedure

1. Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2. Embed the Type-C cable in the Oscilloscope. For Gen 3 systems, use TP3_EQ embedding file *TBT_0p8m.s4p*.
3. De-embed the cables from the test fixture to the Oscilloscope.
4. Ensure that measurements are done with a calibrated reference equalizer (CTLE and DFE). See "Tx CTLE Calibration" on page 260.
5. Perform measurements with:
   - *a* Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   - *b* Oscilloscope with a minimum bandwidth of 21GHz
6. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Adjust vertical and horizontal scale such that the signal fits within the Oscilloscope's display
   - *c* Accumulate at 1E6 UI
7. Compare the data eye to the TP3EQ eye diagram mask. Check for conditions described in the section "Expected / Observable Results".
8. Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the high or low maximum voltage (+/-1000mV), the status of the test is FAIL.

ii If any part of the waveform hits the mask, the status of the test is FAIL.

Test References

See

- "Section 3.5.20 Gen3 Eye Diagram Measurement TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-9 and Figure 5-15 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

Tx Equalization Tests

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Equalization Tests is to confirm that the transmitter equalization is within the limits of the specification. The Tx Equalization Tests are further divided into three tests, namely:

- Tx Equalization Pre-shoot
- Tx Equalization Deemphasis
- Tx Swing Preset 15

Test Pass Requirement

Transmitter Swing: 3.5 ± 1dB (for preset 15 only)

Pre-shoot, De-Emphasis: ± 1dB for the following presets:

Table 14 Transmitter Equalization Presets

Preset Number	Pre-Shoot	De-Emphasis
0	0	0
1	0	-1.9
2	0	-3.6
3	0	-5.0
4	0	-8.4
5	0.9	0
6	1.1	-1.9
7	1.4	-3.8
8	1.7	-5.8
9	2.1	-8.0
10	1.7	0
11	2.2	-2.2
12	2.5	-3.6
13	3.4	-6.7
14	4.3	-9.3
15	1.7	-1.7

(Refer to Table 5 on page 66).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 73 and for configuring the Thunderbolt 3 Test Application, see “Setting up the Thunderbolt 3 Test Application" on page 40.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 47.

3 Under the **Select Tests** tab of the Thunderbolt 3 Test Application, ensure that the tests under the test group *Tx Equalization* are checked.

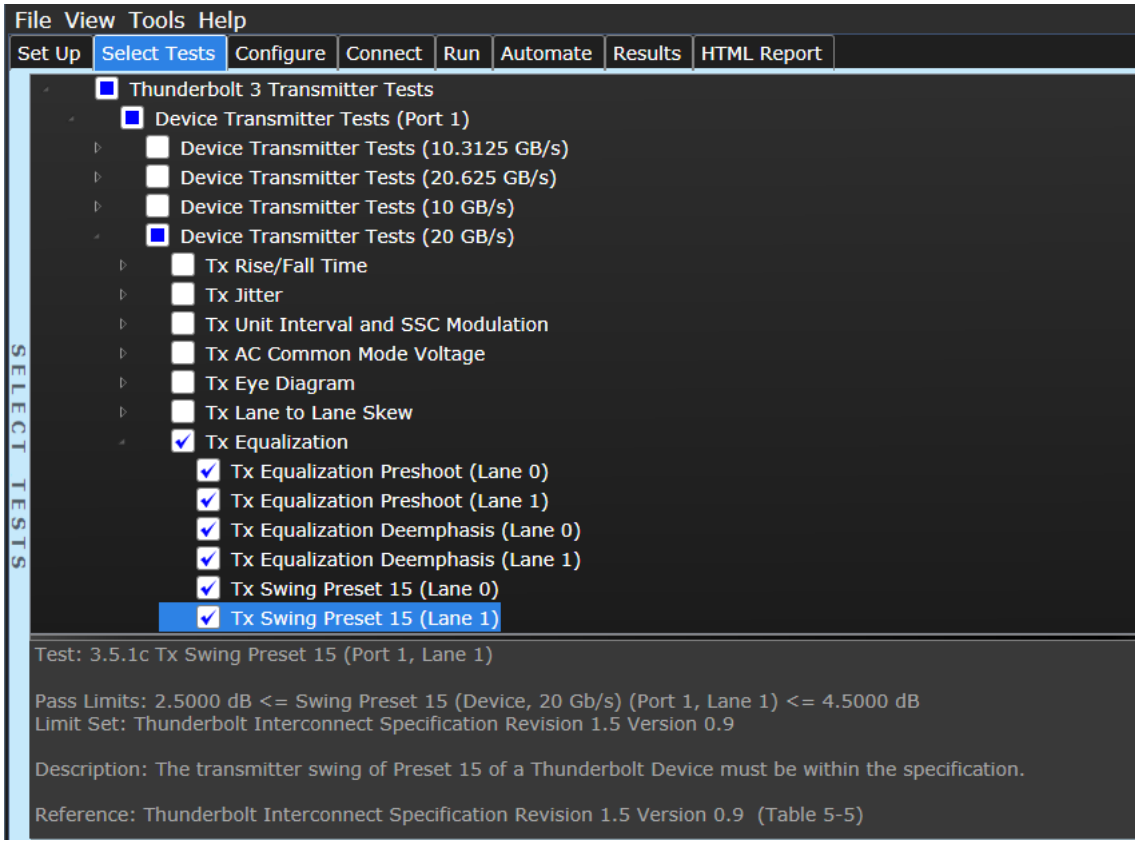


Figure 154 Selecting the Tx Equalization tests

4 Under the **Configure** tab of the Test Application, select **ALL** for the Configuration Variable “Tx Equalization” to run the tests for preset numbers P0 to P15.

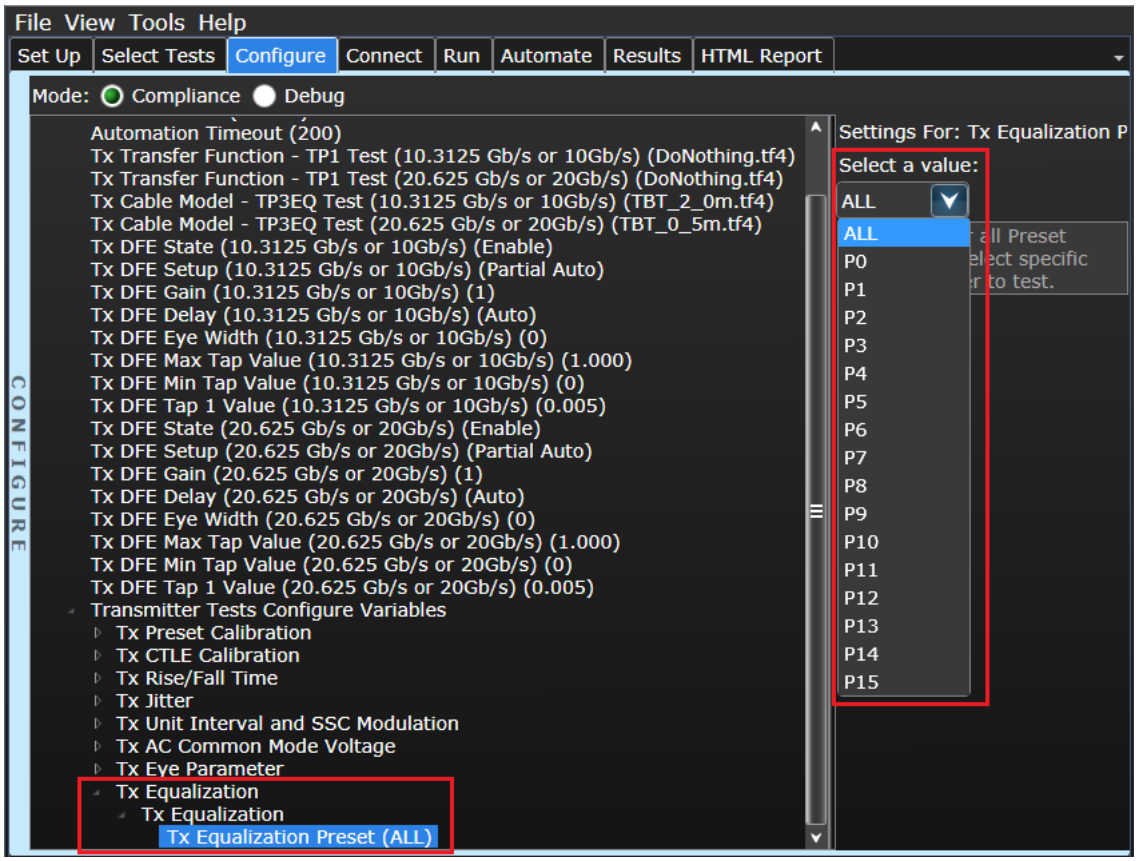


Figure 155 Configuring Tx Equalization Preset Variable

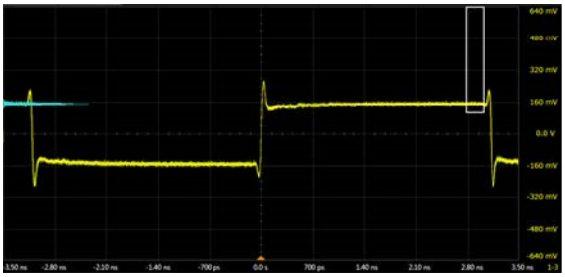
Test Procedure

1 Set Preset 0 (P0).

2 Configure the DUT transmitter to output alternating square pattern of 64 0’s and 64 1’s on all lanes with SSC enabled along with both pre-shoot and de-emphasis enabled.

3 Adjust vertical scale such that the signal fits within the Oscilloscope’s display.

4 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



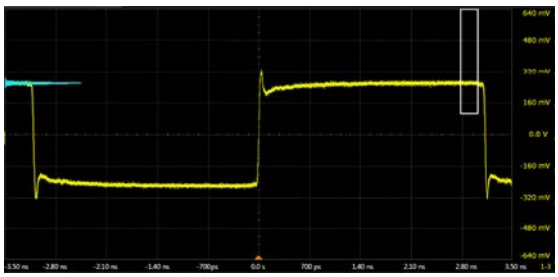
5 Measure differential amplitude voltage (V_1) for bits 57 to 62 using the equation:

$$V_1 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

6 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with de-emphasis enabled but no pre-shoot.

7 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

8 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



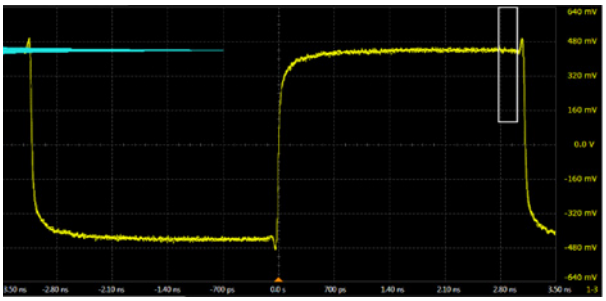
9 Measure differential amplitude voltage (V_2) for bits 57 to 62 using the equation:

$$V_2 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

10 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with pre-shoot enabled but no de-emphasis.

11 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

12 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



13 Measure differential amplitude voltage (V_3) for bits 57 to 62 using the equation:

$$V_3 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

$$\text{Set Pre-Shoot to be } 20 * \log_{10} [V_2/V_1]$$

$$\text{Set De-Emphasis to be } 20 * \log_{10} [V_1/V_3]$$

14 Repeat steps 2 to 10 for all Presets defined in Table 14.

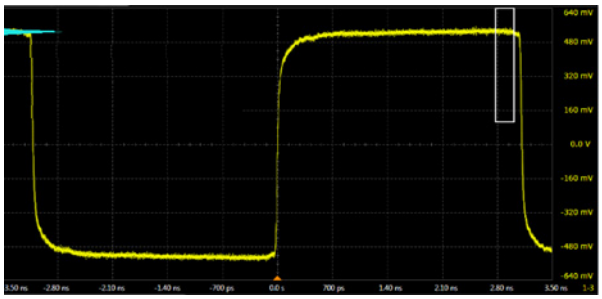
15 Check for PASS/FAIL conditions for both Pre-shoot and De-emphasis.

16 Set the DUT to Preset 0 (P0).

17 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

18 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

19 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



20 Measure differential amplitude voltage (V_0) for bits 57 to 62 using the equation:

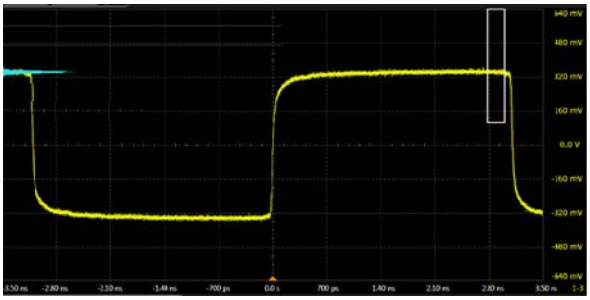
$$V_0 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

21 Set the DUT to Preset 15 (P15).

22 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

23 Adjust vertical scale such that the signal fits within the Oscilloscope's display

24 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



25 Measure differential amplitude voltage (V_{15}) for bits 57 to 62 using the equation:

$$V_{15} = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

Set Swing to be $20 * \log_{10} [V_0/V_{15}]$

26 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If the Pre-Shoot for a particular Preset number is not within ± 1dB of the matching value in Table 14, the status of test is FAIL.

If the De-Emphasis for a particular Preset number is not within ± 1dB of the matching value in Table 14, the status of test is FAIL.

If Swing < 2.5 dB or Swing > 4.5 dB, the status of test is FAIL.

Test References

See

- "Section 3.5.1 Transmitter Equalization" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Revision 1.5 Version 0.9*.
- Table 5-5 of the *Thunderbolt Interconnect Specification Revision 1.5 Version 0.9*.

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