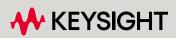
D9050LDDC LPDDR5 Test Application - Methods of Implementation



METHODS OF IMPLEMENTATION

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Keysight D9050LDDC LPDDR5 Test Application Methods of Implementation

1 Overview

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LPDDR5 Automated Testing-At a Glance

The Keysight D9050LDDC LPDDR5 Test Application helps you verify compliance of the SDRAM type (LPDDR5) to the respective JEDEC specifications using a supported Keysight Infiniium Oscilloscope. The Keysight D9050LDDC LPDDR5 Test Application:

- · Lets you select individual or multiple tests to run.
- · Lets you identify the device being tested and its configuration.
- · Shows you how to make oscilloscope connections to the device under test.
- · Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- · Creates a printable HTML report of the tests that have been run.

NOTE

The tests performed by the Keysight D9050LDDC LPDDR5 Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.

For each SDRAM type being tested, you may refer to the following specification documents for compliance testing measurements. For more information, see the JEDEC website: https://www.jedec.org/.

SDRAM Type	Reference Documents
LPDDR5	JEDEC Standard, LPDDR5, JESD209-5C, June 2023

Required Equipment and Software

In order to run the LPDDR5 automated tests, you need the following equipment and software:

Hardware

- Use one of the following Oscilloscope models. Refer to www.keysight.com for the respective bandwidth ranges.
 - Keysight DSO9000A-Series, DSO90000A-Series and DSOX90000A/Q/Z/V-Series Oscilloscopes with a minimum bandwidth of 8GHz (recommended) for accurate measurements. For faster speed grade devices, a minimum bandwidth of 16GHz is recommended for data rates of up to 6.4 GT/s and 25GHz is recommended for data rate of 8.5GT/s.
 - Keysight UXR Oscilloscopes
- Target Device Under Test (DUT)
- · InfiniiMax probe amplifiers:
 - N1169A 12GHz InfiniiMax II probe amplifier
 - MX0020A 10GHz InfiniiMax Ultra Probe Amplifier
 - MX0021A 13GHz InfiniiMax Ultra Probe Amplifier
 - MX0022A 16GHz InfiniiMax Ultra Probe Amplifier
 - MX0023A 25GHz InfiniiMax RC Probe Amplifier
 - MX0024A 20GHz InfiniiMax Ultra Probe Amplifier
 - MX0025A 25GHz InfiniiMax Ultra Probe Amplifier
- InfiniiMax probe heads InfiniiMax II probe heads and accessories (compatible with 9000 Series and 90000 Series, use N5442A precision BNC adapter with 90000X/Q Series):
 - N5381A InfiniiMax II 12GHz differential solder-in probe head and accessories
 - N5382A InfiniiMax II 12GHz differential browser
 - · E2677A InfiniiMax II 12GHz differential solder-in probe head and accessories
 - N5425A InfiniiMax II 12GHz ZIF probe head
 - N5426A InfiniiMax II ZIF tips (×10)
- InfiniiMax Ultra/RC Probe Amplifiers probe heads and accessories:
 - · MX0100A InfiniiMax Micro Probe Head
 - MX0103A Bullet Adapter
- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Precision 3.5 mm BNC to SMA male adapter, Keysight p/n 54855-67604, qty = 2 (provided with the Keysight 54855A and 80000B series oscilloscopes)
- 50-ohm Coax Cable with SMA Male Connectors 24-inch or less RG-316/U or similar, qty = 2, matched length
- Keysight also recommends using a second monitor to view the test application.

Software

- The minimum version of Infiniium Oscilloscope Software (see the Keysight D9050LDDC LPDDR5 Test Application Release Notes)
- Keysight D9050LDDC LPDDR5 Test Application software
- · Keysight E2688A Serial Data Analysis and Clock Recovery software (for clock recovery)

Licensing information

Refer to the *Data Sheet* pertaining to LPDDR5 Test Application to know about the licenses you must install along with other optional licenses. Visit "http://www.keysight.com/find/D9050LDDC" and in the web page's **Document Library** tab, you may view the associated Data Sheet.

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

The licensing format for Keysight License Manager 6 differs from its predecessors. See "Installing the License Key" on page 19 to see the difference in installing a license key using either of the applications on your machine.

NOTE

Keysight D9050LDDC LPDDR5 Compliance Test Application supports Keysight D9010AGGC Compliance Test Software Measurement Server for using multiple machines/PCs over a network as acquisition engines and processing engines in order to significantly enhance the test execution speed. To know more, please see the D9010AGGC product page on keysight.com (http://www.keysight.com/find/d9010aggc).

In This Book

This manual describes the tests that are performed by the Keysight D9050LDDC LPDDR5 Test Application in more detail; it contains information from (and refers to) the LPDDR5 specification and it describes how the tests are performed.

- Chapter 1, "Overview" gives an overview of the automated test application and the required equipment and software.
- Chapter 2, "Installing the Test Application and Licenses" explains how to obtain the installer for
 the automated test application and install the associated licenses (if it was purchased separately).
- Chapter 3, "Preparing to Take Measurements" describes how to launch the Keysight D9050LDDC LPDDR5 Test Application and gives a brief overview of how it is used.
- Chapter 4, "Electrical Tests" describes the methods of implementation for WRITE and READ cycle electrical tests performed on LPDDR5 devices.
- Chapter 5, "Timing Tests" describes the methods of implementation for timing tests performed on LPDDR5 devices.
- Chapter 6, "Eye Diagram Tests" describes the methods of implementation for eye diagram tests
 performed on LPDDR5 devices.

See Also

The Keysight D9050LDDC LPDDR5 Test Application's Online Help, which describes:

- Starting the LPDDR5 Test Application
- · Creating or Opening a Test Project
- Setting Up the Test Environment
- Selecting Tests
- Configuring Tests
- Verifying Physical Connections
- Running Tests
- Configuring Automation in the Test Application
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
- · Additional Settings in the Test App

1 Overview

Keysight D9050LDDC LPDDR5 Test Application Methods of Implementation

2 Installing the Test Application and Licenses

Installing the Test Application 18 Installing the License Key 19

If you purchased the D9050LDDC LPDDR5 Test Application separate from your Infiniium oscilloscope, you must install the software and license key.



Installing the Test Application

- 1 Make sure you have the minimum version of Infiniium oscilloscope software (see the D9050LDDC release notes). To ensure that you have the minimum version, select Help > About Infiniium... from the main menu.
- 2 To obtain the LPDDR5 Test Application, go to Keysight website: "http://www.keysight.com/find/D9050LDDC".
- 3 In the web page's **Free Trials** tab, click the **Details and Download** button to view instructions for downloading and installing the application software.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

- 1 Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.
- 2 Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.

-	Keysig	nt License <mark>Manage</mark> r	
		Licenses on	(localhost) 🔿
		Full computer name:	.msr.is.keysight.com
ectio		Host ID:	PCSERNO, JBXXXXXXX
ns			

Figure 1 Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

- 1 Save the license files on the machine, where you wish to run the Test Application and its features.
- 2 Launch Keysight License Manager.
- 3 From the configuration menu, use one of the options to install each license file.

3 2 - □ ×	
Why do I need these tools?	
Install License File	Ctrl+I
Install License from Text	Ctrl+T
View License Alerts	Ctrl+L
Explore Transport URLs	
About Keysight License Manager	

Figure 2 Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

- 1 Launch Keysight License Manager 6 on your machine, where you wish to run the Test Application and its features.
- 2 Copy the Host ID, which is the first set of alphanumeric value (as highlighted in Figure 3) that appears in the Environment tab of the application. Note that x indicates numeric values.

aaa Keysight License	Manager 6	
Home	Licensing Version	= Keysight License Manager Ver: 6.0.3 Date: Nov 9 2018
Environment	Copyright AGILEESOFD SERVER CONFIG	= © Keysight Technologies 2000-2018
View licenses	AGILEESOFD_SERVER_LOGFILE	<u>C:\ProgramData\Keysight\Licensing\Log\server_log.txt</u>
License usage	SERVER_LICENSE_FILE AGILEESOFD_LICENSE_FILE FLO LICENSE FILE	<pre>= C:\ProgramData\Keysight\Licensing\Licenses\Server = C:\ProgramData\Keysight\Licensing\Licenses\OtherfC:\ProgramData\Keysight = C:\ProgramData\Keysight\Licensing\Licenses\OtherfC:\ProgramData\Keysight</pre>
Borrow license	KAL_LICENSE_FILE AGILEESOFD_DEBUG_MODE FLEXIM_TIMEOUT	<pre>= C:\ProgramData\Keysight\Licensing\Licenses\Other;C:\ProgramData\Keysight = =</pre>
	Default Hostid Ethernet Address	= XXXXadXXXXbe XXbaXeaceXee = XXXXadXXXXbe XXbaXeaceXee
	UUID Physical MAC Address IP Address	= = xxxxadxxxxbe PHY_ETHER=xxbaxeacexee = 127.0.0.1
	Computer/Hostname Username	
	PATH	= C:\Program Files (x86)\Common Files\Intel\Shared Libraries\redist\intel6
	Compact View	
		Refresh Close Help

Figure 3 Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

- 1 Save the license files on the machine, where you wish to run the Test Application and its features.
- 2 Launch Keysight License Manager 6.
- 3 From the **Home** tab, use one of the options to install each license file.

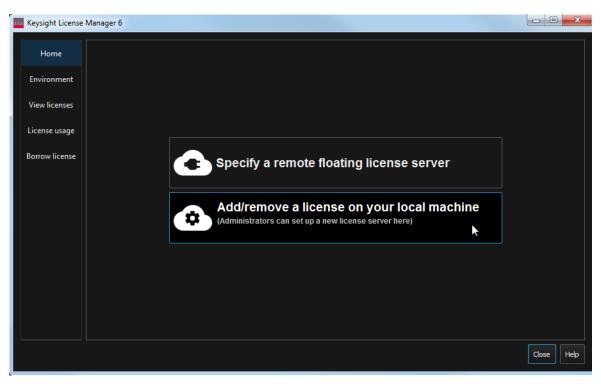


Figure 4 Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

2 Installing the Test Application and Licenses

Keysight D9050LDDC LPDDR5 Test Application Methods of Implementation

3

Preparing to Take Measurements

Calibrating the Oscilloscope 24 Starting the LPDDR5 Test Application 25

Before running the automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this application. After the oscilloscope and probe have been calibrated, you are ready to start the LPDDR5 Test Application and perform the measurements.



Calibrating the Oscilloscope

If you have not already calibrated the oscilloscope, refer to the *User Guide* for the respective Oscilloscope you are using.



If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.



If you switch cables between channels or other Oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the LPDDR5 Test Application

1 Ensure that the LPDDR5 Device Under Test (DUT) is operating and set to desired test modes. To start the LPDDR5 Test Application: From the Infiniium Oscilloscope's main menu, select Analyze > Automated Test Apps > D9050LDDC LPDDR5 Test App.



To launch the application on worker PCs in measurement server mode: From the Infiniium Oscilloscope's main menu, select **Analyze** > **Automated Test Apps** > **Measurement Server** > **D9050LDDC LPDDR5 Measurer**.

ਵ	LPDD	R5 Test LPI	DDR5 Devic	e 1	-		-					
Fi	le Vie	ew Tools He	elp				_					
P		(Y	Connect	Run	Autor	nate	Results	HTML Report			-
	LPDDR5 Test Environment Setup									Â		
	Gene	eral Settings -					Sign	al Source	Settings ——			II
		Mode					СК ([Diff) (Live))			II
	Liv	e Signal					Ch	annel1				II
	Dat	a Rate [MT/s]	wc	K Frequency	[MHz]		WC	< (Diff) (Liv	re)			II
	32	00	16	00			Ch	annel 2				II
	WCI	K:CK Ratio	Clo	ck Frequency	[MHz]		DQ	(Live)				II
	2:1		80	0			Ch	annel 3				II
SE	Ava	ilable Signal Sou	irce				CA ((Live)				
Ξ	СК	(Diff), WCK (Di	ff), DQ, CA				Channel4				П	
												- 11
Р												- 11
				_					_			- 11
				Se	ttings.	.			Sourc	e Thresh	olds	- 11
	Test	Report Comm	onto (Onti	unal)								- 11
		Report Comm		,								II
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		07-19 09:01:										
—							V					۷
	0 Test	S										

Figure 5 LPDDR5 Test Application Main Window

To understand the functionality of the various features in the user interface of the Test Application, refer to the *Keysight D9050LDDC LPDDR5 Test Application Online Help* available in the **Help** menu.

The task flow pane and the tabs in the main pane show the steps you take in running the automated tests:

Tab	Description
Set Up	Lets you identify and set up the test environment, including information about the device under test. The Test App includes relevant information in the final HTML report.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select al tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (for example, channels used in test, voltage levels, etc.).
Connect	Shows you how to connect the oscilloscope to the device under test for the tests that are to be run
Run	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing. Also, allows users to create tags for calibrations and tests.
Automate	Lets you construct scripts of commands that drive execution of the application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE

In the **Configure** tab, the values for all such Configuration parameters that are Oscilloscope-dependent, will correspond to the Oscilloscope Model (DSOs or UXRs), where you are running the Test Application.

Configuring Set Up tab for availability of specific tests

The **Set Up** tab consists of configuration options that correspond to the LPDDR5 device under test (DUT). Select the appropriate options for the relevant tests to appear.

The configuration options specified in the previous table can be set in specific areas of the LPDDR5 Test Application:

• LPDDR5 General Setup—Configure parameters specific to the DUT. To access this window, click Settings... under the Set Up tab.

LPDDR5 Gen	eral Setup				?	
Test Mode						
O Live S	ignal 🔵 (Offline				
Data Rate						
3200	🔽 МТ/	s JEDEC	standard value	es		
wcк : ск	Ratio 2:1		WCK Frequen Clock Frequen			
Signal Sou	rce ——					
CK (Diff),	WCK (Diff)	, DQ, CA				
Single	e-Ended Mo	ode				
Signal Ope	ration Mod	e ———				
CK (Diff)	Continuou	s	$\mathbf{\Sigma}$			
WCK (Diff)	Burst			Burst WCK	options	
RDQS Prea	mble/Posta	amble Leng	th			
RDQS Pream	nble	Static: 4 t	WCK, Toggle: 0	tWCK		
RDQS Postar	mble	0.5 tWCK				
RDQS Posta	mble Mode	Toggle				
WCK Postamble Length						
WCK Postam	ıble	2.5 tWCK				
Show H	lints				OK Close	

Figure 6 General Settings under Set Up tab

- **Test Mode**—select whether to run tests on a live signal (with DUT connected) or on offline signal (saved waveforms).
- Data Rate-select the speed grade for test signal transmission.
- WCK:CK Ratio select the Frequency ratio for Write Clock (WCK) and Clock (CK) signal. Please refer to the Table 1.

WCK:CK Ratio Data Rate Range [Mbps] Clock Frequency Range [MHz] Unit Lower Limit (>) Upper Limit (<u>></u>) Lower Limit (>) Upper Limit (<u>></u>) 2:1 40 533 10 133 nCK 2:1 533 1067 133 267 nCK 2:1 1067 1600 267 400 nCK 2:1 1600 2133 400 533 nCK 2:1 2133 2750 533 688 nCK 2750 3200 2:1 688 800 nCK 4:1 40 533 5 67 nCK 4:1 533 1067 67 133 nCK 4:1 1067 1600 133 200 nCK 4:1 1600 2133 200 267 nCK 2133 2750 267 nCK 4:1 344 4:1 2750 3200 344 400 nCK 4:1 3200 3733 400 467 nCK 4:1 3733 4267 467 533 nCK 4:1 4267 4800 533 600 nCK 4:1 4800 600 688 nCK 5500 5500 6000 688 nCK 4:1 750 6000 6400 750 800 4:1 nCK 6400 7500 800 937.5 4:1 nCK 4:1 7500 8533 937.5 1066.5 nCK

Table 1 WCK:CK Ratio

- **Signal Source**—select the combination of signals for the corresponding LPDDR5 tests to appear in the Select Tests tab.
- **Signal Operation Mode**—select whether the differential clock and differential write clock signals will be transmitted in either continuous or burst modes. For WCK bursts, you may select the read/write separation technique.
- **RDQS Preamble/Postamble Length**—Select the length of RDQS preamble and postamble when RDQS (Diff) is selected as one of the test signals.
- WCK Postamble Length—Select the length of WCK postamble when WCK (Diff) is selected as one of the test signals.
- Signal Source Setup-To access this window, click Source... under the Set Up tab.
 - For Live Signal Test Mode, assign Oscilloscope Channels to each signal selected under Signal Source.



Figure 7 Signal Source Settings under Set Up tab

• For **Offline** Test Mode, click **Browse...** against each signal type and select the offline waveform file in *wfm* format.

Signal Source	Setup		?
Available O	ffline Signal(s)		
CK (Diff)	NA	Browse	
WCK (Diff)	NA	Browse	
DQ	NA	Browse	
СА	NA	Browse	1
Show H	ints		OK Close

Figure 8

Signal Source Settings under Set Up tab

- Threshold Setup-To access this window, click Thresholds... under the Set Up tab.
 - Under **Signal Thresholds** tab, verify or modify the upper, middle and lower threshold values for each selected **Signal Source** type.

Threshold Setup		? 🗖
Signal Thresholds	Measurement Thresholds	
CK (Diff) CK (Diff) CA CA CA CA CA CA CA CA	dance Him Con	Read Barat High Impediance Wins Barat Mode Unset
Show Hints		

- Figure 9 Signal threshold settings
 - Under **Measurement Thresholds** tab, verify or modify the corresponding threshold values required for measurements to be performed on each selected **Signal Source** type.

Threshold Setu	P		?					
Signal Thresh	Signal Thresholds Measurement Thresholds							
	VDD VH (AC) VH (DC) VREF VIL (DC) VIL (AC)	VDDQ VIHdiff V0H (AC) VOH(IFF V0H (DC) VOH(IFF V0H (DC) VIHdiff V0L (AC) VIHdiff						
General CK (Diff) WCK (Diff) DQ CA	VDD2H (V) 1.05 VDDQ (V) 0.5 VDD	VrefDQ (V) 0.15 V VrefCA (V) 0.15 V						
Show Hin	ts	OK C	Close					

Figure 10 Measurement threshold settings

• Click **OK** to apply and save any changes made to each window for the settings to take effect.

NOTE	Starting from application version 2.0.2.0 onwards, it is recommended for the WCK threshold to use the measurement threshold's upper/middle/lower threshold level that crosses all the valid transitions, which exclude the preamble region, and the middle threshold has to be within the middle level of the transition. Please refer to Figure 11.
NOTE	There is a special case where the WCK negative pulse within the preamble region is narrower than the negative pulse after the preamble region. To cater this waveform, it is recommended to use the signal threshold's upper/middle/lower threshold level that crosses all the valid transitions in the preamble region. Please refer to Figure 11.
NOTE	The prerequisite Test IDs indicate all such tests that must be run prior to the corresponding tests. It is possible that one or more of the prerequisite tests may not have been selected prior to running the related test. However, the LPDDR5 Test Application automatically runs such tests and displays the resulting values.

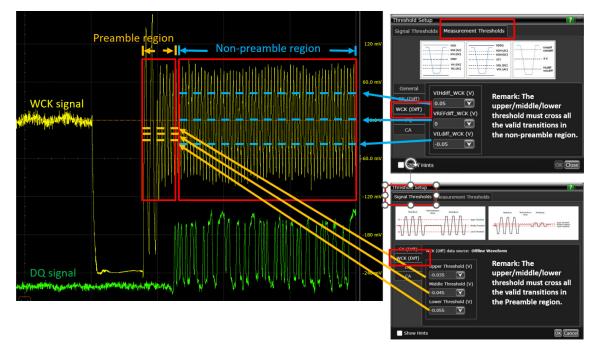


Figure 11 Configuring WCK (Diff) Signal Thresholds and Measurement Thresholds

Using Keysight D9010AGGC Compliance Test Software Measurement Server

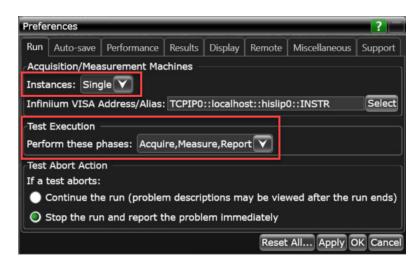
Keep the following points in mind when using Keysight D9010AGGC Compliance Test Software Measurement Server:

- When the **Acquire, Measure, Report** is selected as the test execution phase, then **Offline** Test mode cannot be selected.
- When the **Measure, Report** is selected as the test execution phase, then **Live Test** mode cannot be selected.
- When the **Acquire (only)** is selected as the test execution phase, then test execution can be performed and projects can be saved.
- Before loading a project for performing offline processing, ensure that under the **Run** tab of the Preferences dialog:
 - Single is selected from the Instances drop-down list.
 - Under the Test Execution section, Measure, Report option is selected.

-										
Prefe	rences						?			
Run	Auto-save	Performance	Results	Display	Remote	Miscellaneous	Support			
Acqu	isition/Mea	surement Ma	chines –							
Insta	Instances: Single									
Infin	iium VISA A	Address/Alias:	TCPIP0	::localho	st::hislip	0::INSTR	Select			
Test	Execution									
Perfo	orm these p	hases: Meas	ure,Repo	ort 🔽						
Test	Abort Actio	n ———			-					
If a t	test aborts:									
Continue the run (problem descriptions may be viewed after the run ends)										
0 9	O Stop the run and report the problem immediately									
	Reset All Apply OK Cance									

The test execution phase can be switched either via GUI or by using the remote command.

- Before loading a project for performing run using live signal, ensure that under the **Run** tab of the Preferences dialog:
 - Single is selected from the Instances drop-down list.
 - Under the Test Execution section, Acquire, Measure, Report option is selected.



The test execution phase can be switched either via GUI or by using the remote command.



If the correct test execution phase is not set in a manner described above, you might see no tests under the Select Tests tab.



It is recommended to name your projects in a manner, e.g., by using the "offline" or "live" suffixes to the names of the project files.

• There are certain tests called "acquisition dominant tests" that require multiple waveforms for the test execution cycle. These tests are executed on the oscilloscope itself as transferring the waveforms to the worker PCs or computation PCs will lead to increased test time. The following table lists the acquisition dominant tests in the D9050LDDC LPDDR5 compliance application.

Test ID	Test Name
102020	tCK(avg)
102022	tCH(avg)
102023	tCL(avg)
102024	tCH(abs)
102025	tCL(abs)
102027	tjit(per)
102000	tWCK(avg)
102001	tWCK(abs)
102002	tWCKH(avg)
102003	tWCKL(avg)
102004	tWCKH(abs)

Test ID	Test Name
102005	tWCKL(abs)
102006	tjit(CC)
102007	tjit(per)
102008	tERR(2per) Write Clock Cumulative error across 2 cycles
102009	tERR(3per) Write Clock Cumulative error across 3 cycles
102010	tERR(4per) Write Clock Cumulative error across 4 cycles
102021	tCK(abs)
102026	tjit(CC)
141000	tDIVW1 Margin
141001	tDIVW2 Margin
141002	vDIVW Margin
141003	tDIPW
141004	tDIHL
141005	VDIHL_AC
141007	tWCK2DQI_HF
130003	tQSH
130004	tQSL
140007	tWCK2DQ0_HF
251107	tWCKHL
251110	tWCKH
251111	tWCKL
251007	tCKHL
251010	tCKH
251011	tCKL
142020	tCSIVW1 Margin
142021	tCSIVW2 Margin
142022	vCSIVW Margin
142023	tCSIPW
142024	vCSIHL_AC
142001	tCIVW1 Margin
142002	tCIVW2 Margin
142003	vCIVW Margin
142004	tCIPW
142005	vCIHL_AC

Test ID	Test Name
142006	tCA2CA_share
142000	tCA2CA
140000	tQW

For more information about the Keysight D9010AGGC Measurement Server, refer to the following documents:

- Keysight D9010AGGC Compliance Test Software Measurement Server User Guide https://www.keysight.com/in/en/assets/9921-01769/user-manuals/D9010AGGC-User-Guide.pd f
- Keysight Digital Test Apps Measurement Server Feature Application Note https://www.keysight.com/in/en/assets/3121-1027/application-notes/Keysight-Digital-Test-Ap ps-Measurement-Server-Feature.pdf

3 Preparing to Take Measurements

Keysight D9050LDDC LPDDR5 Test Application Methods of Implementation

4 Electrical Tests

RDQS Detect Method for Read Write Separation 38 Data tests 41 Command/Address tests 54 Chip Select tests 61 Clock (Diff) Tests 68 Write Clock (Diff) Tests 77 Clock (SE Mode) Tests 87 Write Clock (SE Mode) Tests 92 Clock (SE) CK_t (Clock Plus) tests 97 Clock (SE) CK_c (Clock Minus) tests 106 Clock (SE) CK_t & CK_c (Clock Plus & Minus) tests 115 Write Clock (SE) WCK_t (Write Clock Plus) tests 117 Write Clock (SE) WCK_c (Write Clock Minus) tests 125 Write Clock (SE) WCK_t & WCK_c (Write Clock Plus & Minus) tests 134 Read Data Strobe (Diff) tests 136 Read Data Strobe (SE) RDQS_t (Read Data Strobe Plus) tests 138 Read Data Strobe (SE) RDQS_c (Read Data Strobe Minus) tests 145 Read Data Strobe (SE) RDQS_t & RDQS_C (Read Data Strobe Plus & Minus) tests 152



RDQS Detect Method for Read Write Separation

RDQS Detect is a read write separation method. This method works when the signal source contains at least an RDQS signal and a WCK signal. In this method, the Read/Write burst data is identified based on the presence of RDQS burst. If WCK burst contains an RDQS burst, then it is a Read burst. If the WCK burst does not contain an RDQS burst, then it is a Write burst.

If you select the RDQS Detect mode as the burst identification method, you must select the length of the WCK Postamble in the WCK Postamble Length section of the LPDDR5 General Setup dialog box.

LPDDR5 General Setup)			_	?
Set the data rate of the	tect cignal h	w entering a custor	n value or cel	act fr	om the
JEDEC standard data ra		y entering a custor			
3200 🔽 МТ	7/s JEDE	C standard value	es		
WCK : CK Ratio 2:	1	WCK Frequen Clock Frequer			
Signal Source					
WCK_t (SE), WCK_	c (SE), RDO	QS_t (SE), RDQS	5_c (SE)		
Single-Ended M	1ode				
Signal Operation Mod	de				
CK (Diff) Continuo	us				
WCK (Diff) Burst			Burst WCK	opti	ons
RDQS Preamble/Post	amble Len	ath			
Identify the length of R					
RDQS Preamble	Static: 4	tWCK, Toggle: 0	tWCK		
RDQS Postamble	0.5 tWCk	ζ			
RDQS Postamble Mode	Toggle				
WCK Postamble Leng	jth				
	CK Postamb	le.			
WCK Postamble	2.5 tWCk	<		$\mathbf{\vee}$	
	2.5 tWC	К			
🖌 Show Hints	4.5 tWC				OK Cance

Figure 12 LPDDR5 General Setup Dialog



Figure 13 WCK Burst Options Setup Dialog

Tests that support the RDQS Detect Burst Identification Method

The following Electrical tests support the RDQS Burst Identification method:

WRITE Tests

- Vindiff_WCK
- Vindiff_WCK/2HighPulse
- Vindiff_WCK/2LowPulse
- Vinse_WCK (Positive Pulse)
- Vinse_WCK (Negative Pulse)
- Vinse_WCK_High (WCK_t)
- Vinse_WCK_High (WCK_c)
- Vinse_WCK_Low (WCK_t)
- Vinse_WCK_Low (WCK_c)
- vDIHP1
- vDILP1
- · vDIHP2
- vDILP2
- VIHdiff_WCK
- VILdiff_WCK
- SRIdiffR_WCK
- SRIdiffF_WCK
- Vix_WCK_Ratio
- Vinse_WCK
- Vinse_WCK_SE
- Vinse_WCK_SE_High
- Vinse_WCK_SE_Low
- SRIseR_WCKSE
- SRIseF_WCKSE

READ Tests

- SRQseR_DQ
- SRQseF_DQ
- SRQdiffR_RDQS
- SRQdiffF_RDQS

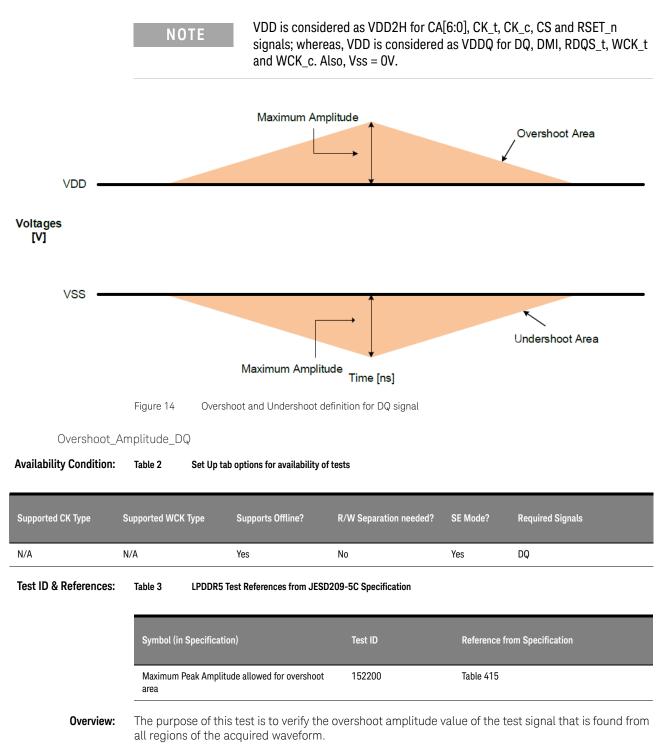
Method of Implementation for the RDQS Detect Burst Identification Method

The following are the steps for the method of implementation for the RDQS Detect burst identification method:

- 1 Populate the burst from WCK signal.
- 2 Locate FirstWCKRising for the burst.
- 3 Compute TimeA = FirstWCKRising + tWCKPRE_Toggle_RD * ClockCycleWidth.
- 4 Compute TimeB = Start of WCK postamble. For example, if tWCKPST=2.5nWCK then TimeB = time of second last rising edge of WCK burst. If tWCKPST=4.5nWCK then TimeB = time of fourth last rising edge of WCK burst.
- 5 Compute TimeC = 0.5*(TimeA+TimeB)
- 6 Compute VmaxTimeCWithinUI = Vmax range from (TimeC 1*UI) to (TimeC + 1*UI)
- 7 Compute VminTimeCWithinUI = Vmin range from (TimeC 1*UI) to (TimeC + 1*UI)
- 8 If [(VmaxTimeCWithinUI > VOHDiff_RDQS) AND (VminTimeCWithinUI < VOLDiff_RDQS)] then the burst will be recognized as a READ burst. Otherwise, the burst will be recognized as a WRITE burst.
- 9 Repeat steps 2 to 8 for the rest of burst.

Data tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 14.



In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

- **Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},$ V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

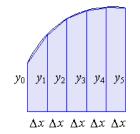
Overshoot Amplitude = $V_{MAX} - V_{DDQ}$

b Evaluate Area_below_ V_{DDQ} using the equation:

Area_below_V_{DDQ} = (OvershootRegion_End - OvershootRegion_Start) x V_{DDQ}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$\mathrm{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_n}{2}\Big)$$

Figure 15 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_OV - Area_below_V_{DDQ}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DDQ}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JESD209-5C specification.

Undershoot_Amplitude_DQ

Availability Condition:	Table 4	Set Up tab options for availability of tests
-------------------------	---------	--

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	DQ

Test ID & References: Table 5 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for undershoot area	152201	Table 415

Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

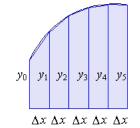
Procedure: 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

- 2 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.
- 3 Within UndershootRegion # 1:
 - a Evaluate Undershoot Amplitude by:
 - i Using $T_{\text{MIN}}, V_{\text{MIN}}$ to obtain the time-stamp of the minimum voltage on the UndershootRegion.
 - ii Calculating Undershoot Amplitude using the equation:

Undershoot Amplitude = Vss - V_{MIN}

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

The Trapezoidal Rule



$$\operatorname{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

${f Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+h$	$\left(\frac{y_n}{2}\right)$
--	------------------------------

Figure 16 Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/ The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JESD209-5C specification.

_ 、	p tab options for availability	of tests		
Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Yes	No	Yes	DQ
			Deference	from Constituation
		152202	Table 415	from Specification
	Supported WCK Type N/A Table 7 LPDD Symbol (in Specifi	Table 6 Set Up tab options for availability Supported WCK Type Supports Offline? N/A Yes	Table 6 Set Up tab options for availability of tests Supported WCK Type Supports Offline? R/W Separation needed? N/A Yes No Table 7 LPDDR5 Test References from JESD209-5C Specification Symbol (in Specification) Test ID	Table 6 Set Up tab options for availability of tests Supported WCK Type Supports Offline? R/W Separation needed? SE Mode? N/A Yes No Yes Table 7 LPDDR5 Test References from JESD209-5C Specification Reference Symbol (in Specification) Test ID Reference

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

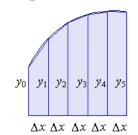
- **Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}}, V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

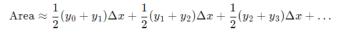
Overshoot Amplitude = $V_{MAX} - V_{DDQ}$

b Evaluate Area_below_V_{DDQ} using the equation:

Area_below_V_{DDQ} = (OvershootRegion_End - OvershootRegion_Start) x V_{DDQ}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:





We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$\mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

- Figure 17 Equation for Total_Area_Above_OV
 - *d* Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_OV - Area_below_V_{DDQ}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DDQ}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JESD209-5C specification.

Undershoot_Area_DQ

Availability Condition:	Table 8	Set Up tab options for availability of tests
-------------------------	---------	--

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	N/A	Yes	No	Yes	DQ		
Test ID & References:	Table 9 LPDDR	5 Test References from JE	SD209-5C Specification				
	Symbol (in Specifica	tion)	Test ID	Reference f	rom Specification		
	Maximum undershoo	t area above VSS	152203	Table 415			
Overview:	from all regions of	of the acquired wav	he undershoot amplitud eform. In case of an unc width and undershoot a	lershoot, the	e test signal that is found undershoot area is		
Procedure:	(vertical scale	e adjustment).	perform signal conditio	Ū	mize screen resolution		
		potRegion" starts at	ross the acquired wavef t the falling edge of Vss		and ends at the rising edge		
		3 Within UndershootRegion # 1:					
	 a Evaluate Undershoot Amplitude by: i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion. 						
		0	Amplitude using the equ	lation:			
		Und	dershoot Amplitude = Vs	s - V _{MIN}			
	<i>b</i> Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:						
		The Trapezo	oidal Rule				

Δχ Δχ Δχ Δχ Δχ

*y*₀ *y*₁ *y*₂ *y*₃ *y*₄

$$ext{Area}pprox rac{1}{2}(y_0+y_1)\Delta x+rac{1}{2}(y_1+y_2)\Delta x+rac{1}{2}(y_2+y_3)\Delta x+\dots$$

We can simplify this to give us the $\ensuremath{\mathbf{Trapezoidal\ Rule}}$, for n trapezoids:

$$egin{aligned} \operatorname{Area} &pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big) \end{aligned}$$

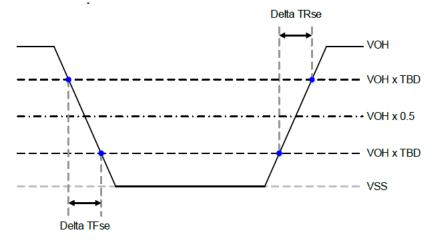
y5

Figure 18

Equation for Total_Area_Below_Vss

- *c* To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JESD209-5C specification.



Output slew rate for single-ended signals are measured as shown in Figure 19.

Figure 19 Single-ended output slew rate definition for DQ signal

SRQseR_DQ

Availability Condition:	Table 10	Set Up tab options for availability of tests
-------------------------	----------	--

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	Yes	DQ, RDQS(Diff)

Test ID & References: Table 11

LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
SRQse	150000	Table 429

Overview:

iew: The purpose of this test is to verify the rising slew rate value of the test signal within the read burst.

- **Procedure:** 1 Acquire and split the read and write burst of the acquired signal.
 - 2 Take the first valid READ burst found.
 - 3 Find all the valid rising edges in the specified burst. A valid rising edge starts at $V_{\rm OL}$ crossing and ends at the following $V_{\rm OH}$ crossing.
 - $\begin{array}{ll} 4 & \mbox{For all the valid rising edges, find the transition time, T_R.} \\ & \mbox{T_R}$ is the time starting at V_{OL} crossing and ending at the following V_{OH} crossing.} \end{array}$
 - 5 Calculate SRQseR_DQ using the equation:

 $SRQseR_DQ = [V_{OH} - V_{OL}] / T_R$

6 Determine the worst result from the set of SRQseR_DQ measured.

Expected/ The calculated Rising Slew (SRQseR_DQ) value for the test signal shall be within the conformance limits as per the JESD209-5C specification.

SRQseF_DQ

Availability Condition: Table 12 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	N/A	Yes	Yes	Yes	DQ, RDQS(Diff)		
Test ID & References:	Table 13 LPDDR	5 Test References from JE	SD209-5C Specification				
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification		
	SRQse		150001	Table 429			
Overview:	The purpose of th	nis test is to verify t	he falling slew rate valu	e of the test	signal within the read burst.		
Procedure:	 Take the first Find all the v. A valid falling For all the va T_R is the time 	 Find all the valid falling edges in the specified burst. A valid falling edge starts at V_{OH} crossing and ends at the following V_{OL} crossing. For all the valid falling edges, find the transition time, T_F. T_R is the time starting at V_{OH} crossing and ending at the following V_{OL} crossing. Calculate SRQseF_DQ using the equation: SRQseF_DQ = [V_{OH} - V_{OL}] / T_F 					
Expected/ Observable Results:	The calculated F		F_DQ) value for the test		be within the conformance		

vDIHP1

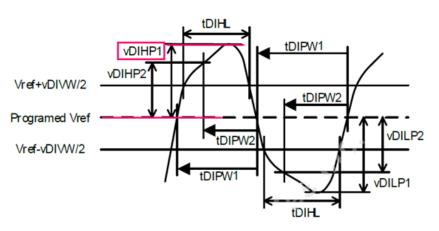


Figure 20 DQ Rx pulse amplitude from prog. Vref DQ of the test signal

Availability Condition: Table 14 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode? Required Signals	Required Signals
N/A	Burst & Continuous	YES	Yes	Yes	WCK (Diff), DQ
Test ID & References:	Table 15 LPDDR5	Test References from JE	SD209-5C Specification		
	Symbol (in Specificat	ion)	Test ID	Reference f	from Specification
	vDIHP1		153000		Table 468
Overview:		The purpose of this test is to verify DQ Rx pulse amplitude from prog. Vref DQ of the test signal that is found from all region of the acquired waveform.			
Procedure:		1 Find all valid positive pulses in the specified burst. A valid positive pulse starts at the valid risin edge and ends at the following valid falling edge.			
	2 Zoom into the				
	3 If the pulse is a single pulse (<1.5UI), then measure the VMax, and then calculate the value of vDIHP1 using the equation:				nen calculate the value of
	vDIHP1 = V _{max} - V _{ref}				
	4 Continue the previous step with the rest of the positive pulses found in the specified burst.			in the specified burst.	
	5 Determine the				
/Expected Observable Results:		lue of vDIHP1 shal	l be within the conforma	ince limits as	s per the JESD209-5C

vDILP1

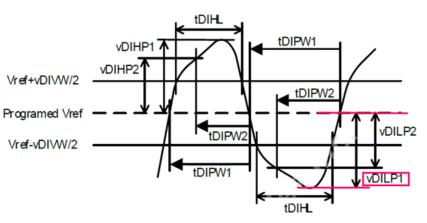


Figure 21 DQ Rx pulse amplitude from prog. Vref DQ of the test signal

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	Yes	Yes	WCK (Diff), DQ

Availability Condition: Table 16 Set Up tab options for availability of tests

Test ID & References: Table 17 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
vDILP1	153001	Table 468

Overview: The purpose of this test is to verify DQ Rx pulse amplitude from prog. Vref DQ of the test signal that is found from all region of the acquired waveform.

Procedure: 1 Find all valid negative pulses in the specified burst. A valid negative pulse starts at the valid falling edge and ends at the following valid rising edge.

- 2 Zoom into the first pulse.
- 3 If the pulse is a single pulse (<1.5UI), then measure the Vmin, and then calculate the value of vDILP1 using the equation:

 $vDILP1 = V_{min} - V_{ref}$

- 4 Continue the previous step with the rest of the negative pulses found in the specified burst.
- 5 Determine the worst result from the set of vDILP1 measured.

Expected/ The measured value of vDILP1 shall be within the conformance limits as per the JESD209-5C **Observable Results:** specification.

vDIHP2

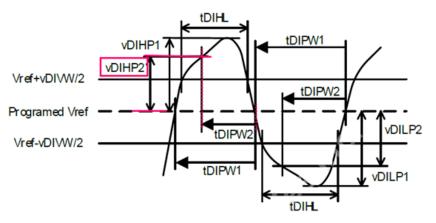


Figure 22 DQ Rx early pulse amplitude from prog. Vref DQ of the test signal

Availability Condition: Table 18 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	Yes	Yes	WCK (Diff), DQ

Test ID & References: Ta

Table 19 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
vDIHP2	153002	Table 468

Overview: The purpose of this test is to verify DQ Rx early pulse amplitude from prog. Vref DQ of the test signal that is found from all region of the acquired waveform.

Procedure:

- 1 Find all valid falling DQ crossings at VREFDQ level in the specified burst.
- 2 For each falling DQ crossing found,
 - a Get the timestamp of crossing. Then, calculate tA=tCross-tDIPW2(Compliance). *Compliance value of tDIPW2 is 0.26UI.
 - *b* If the pulse is a single pulse (pulse width < 1.5UI), then proceed to measure DQ voltage at tA. Measured value is vDIHP2 result.

Note that if the pulse is not a single pulse, then do not proceed to measure the DQ voltage.

3 Determine the worst result from the set of vDIHP2 measured.

Expected/ The measured value of vDIHP2 shall be within the conformance limits as per the JESD209-5C **Observable Results:** specification.

vDILP2

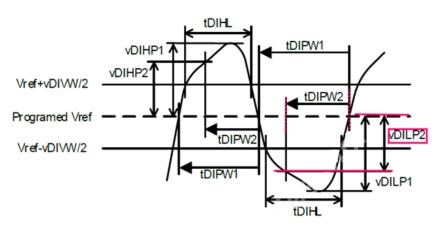


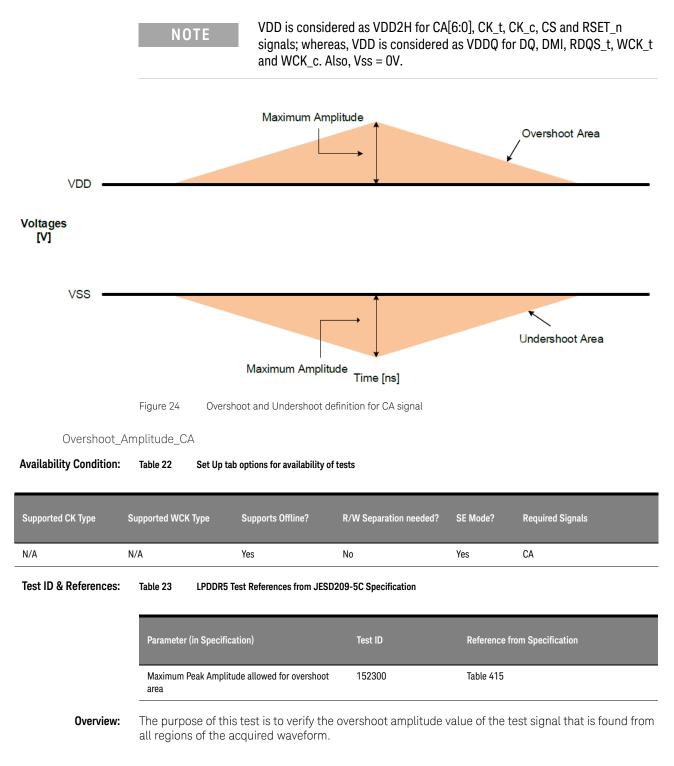
Figure 23 DQ Rx early pulse amplitude from prog. Vref DQ of the test signal

Supported CK Type	Supported WCK Type	upported WCK Type Supports Offline? R/W Separation needed? SE Mode? Required Signals					
Burst & Continuous	Burst & Continuous	Yes	Yes	Yes	WCK (Diff), DQ		
Test ID & References:	Table 21 LPDDR	5 Test References from JE	SD209-5C Specification				
	Symbol (in Specifica	tion)	Test ID	Reference f	from Specification		
	vDILP2		153003		Table 468		
Overview:		-	DQ Rx early pulse amplit acquired waveform.	ude from pro	og. Vref DQ of the test signal		
Procedure:	 2 For each risir a Get the tin *Complian b If the pulse Measured Note that 	 a Get the timestamp of crossing. Then, calculate tA=tCross-tDIPW2(Compliance). *Compliance value of tDIPW2 is 0.26UI. b If the pulse is a single pulse (pulse width < 1.5UI), then proceed to measure DQ voltage at tA Measured value is vDILP2 result. Note that if the pulse is not a single pulse, then do not proceed to measure the DQ voltage. 					
Expected/ Observable Results:		3 Determine the worst result from the set of vDILP2 measured. The measured value of vDILP2 shall be within the conformance limits as per the JESD209-5C specification.					

Availability Condition: Table 20 Set Up tab options for availability of tests

Command/Address tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 24.



When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

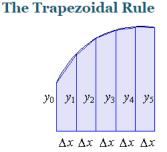
- **Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},\,V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DD2H}$

b Evaluate Area_below_V_{DD2H} using the equation:

Area_below_V_{DD2H} = (OvershootRegion_End - OvershootRegion_Start) x V_{DD2H}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$ext{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 25 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_OV - Area_below_V_{DD2H}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DD2H}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

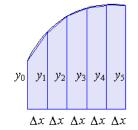
Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JESD209-5C specification.

Undershoot_Amplitude_CA

Availability Condition: Table 24 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed	? SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	CA
Test ID & References:	Table 25 LPDDR	5 Test References from .	JESD209-5C Specification		
	Parameter (in Speci	fication)	Test ID	Reference	from Specification
	Maximum Peak Amp area	litude allowed for unders	shoot 152301	Table 415	
Overview:	from all regions	of the acquired wa	r the undershoot ampliti aveform. In case of an u lal Method Area Calcula	ndershoot, the	ne test signal that is found e undershoot area is
Procedure:		uire signal data an e adjustment).	d perform signal condit	ioning to max	imize screen resolution
	An "Undersh	An "UndershootRegion" starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.			
	3 Within UndershootRegion # 1:				
	 a Evaluate Undershoot Amplitude by: i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion. 				
					oltage on the
	ii Calcu	ulating Undershoo	t Amplitude using the e	quation:	
		U	ndershoot Amplitude =	Vss - V _{MIN}	
	b Evaluate 1	otal Area Below	Vss by using Trapezoida	Mathod Ara	a Calculation:

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + h \Big)$	$\left(\frac{y_n}{2}\right)$		
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Figure 26 Equation for Total_Area_Below_Vss

- *c* To find the worst case, save the following calculated results for later use:
 - · Overshoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/ The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JESD209-5C specification.

	Overs	hoot	Area	СА
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Availability Condition: Table 26 Set Up tab options for availability of tests

Supported CK Type	Supported WCK	Type Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	CA
Test ID & References:	Table 27	le 27 LPDDR5 Test References from JESD209-5C Specification			

Parameter (in Specification)	Test ID	Reference from Specification
Maximum overshoot area above V_{DD2H}/V_{DDQ}	152302	Table 415

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

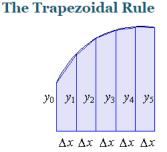
- **Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}}, V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DD2H}$

b Evaluate Area_below_V_{DD2H} using the equation:

Area_below_V_{DD2H} = (OvershootRegion_End - OvershootRegion_Start) x V_{DD2H}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



$$\mathrm{Area}pprox rac{1}{2}(y_0+y_1)\Delta x+rac{1}{2}(y_1+y_2)\Delta x+rac{1}{2}(y_2+y_3)\Delta x+\dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$ext{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

- Figure 27 Equation for Total_Area_Above_OV
 - d Calculate Area_Above_ V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_OV - Area_below_V_{DD2H}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - · Area_Above_V_{DD2H}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

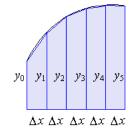
Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JESD209-5C specification.

Undershoot_Area_CA

Availability Condition:	Table 28	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
N/A	N/A	Yes	No	Yes	CA	
Test ID & References:	Table 29 LPC	DR5 Test References from J	ESD209-5C Specification			
	Parameter (in Sp	ecification)	Test ID	Reference from Specification		
	Maximum unders	hoot area above VSS	152303	Table 415		
Overview:		of this test is to verify as of the acquired wa		e value of th	e test signal that is found	
	In case of an u undershoot ar		rshoot area is calculated	based on th	e undershoot width and	
Procedure:	1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).					
	2 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.					
	3 Within UndershootRegion # 1:					
	a Evaluate Undershoot Amplitude by:					
)			
		ing T _{MIN} , V _{MIN} to obta dershootRegion.	ain the time-stamp of the	e minimum v	oltage on the	
	Un	dershootRegion.	2		oltage on the	
	Un	dershootRegion. Iculating Undershoot	ain the time-stamp of the	lation:	oltage on the	

The Trapezoidal Rule



$$\mathrm{Area}pprox rac{1}{2}(y_0+y_1)\Delta x+rac{1}{2}(y_1+y_2)\Delta x+rac{1}{2}(y_2+y_3)\Delta x+\dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$igg| \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

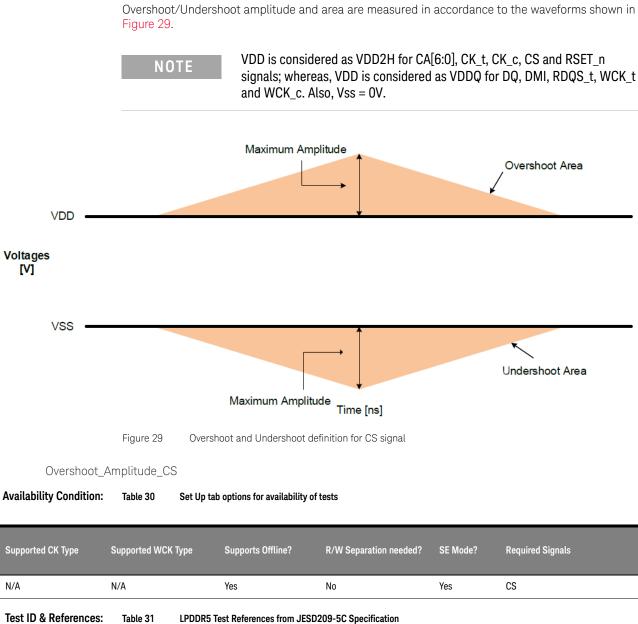
Figure 28 Equation for Total_Area_Below_Vss

- *c* To find the worst case, save the following calculated results for later use:
 - · Overshoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/ Observable Results:

The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JESD209-5C specification.

Chip Select tests



Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in

Parameter (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for overshoot area	152400	Table 415
The nurnose of this test is to verify the o	wershoot ampl	itude value of the test signal that is found from

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

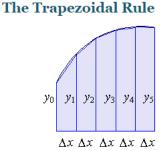
- **Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},\,V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DD2H}$

b Evaluate Area_below_V_{DD2H} using the equation:

Area_below_V_{DD2H} = (OvershootRegion_End - OvershootRegion_Start) x V_{DD2H}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



$$\operatorname{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$\mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 30 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_OV - Area_below_V_{DD2H}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DD2H}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

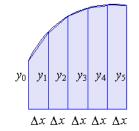
Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JESD209-5C specification.

Undershoot_Amplitude_CS

Availability Condition: Table 32 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	CS
Test ID & References:	Table 33 LPDDR	Test References from J	ESD209-5C Specification		
	Parameter (in Specif	ication)	Test ID	Reference	from Specification
	Maximum Peak Ampl area	itude allowed for unders	noot 152401	Table 415	
Overview:	from all regions of	of the acquired wa	the undershoot amplitud veform. In case of an un al Method Area Calculati	dershoot, the	ne test signal that is found e undershoot area is
Procedure:		iire signal data and e adjustment).	l perform signal conditic	ning to maxi	mize screen resolution
		ootRegion" starts a	cross the acquired wave at the falling edge of Vss		g and ends at the rising edge
	3 Within Under	shootRegion # 1:			
	a Evaluate L	ndershoot Amplitu	ıde by:		
		T _{MIN} , V _{MIN} to obta rshootRegion.	ain the time-stamp of th	e minimum v	oltage on the
	ii Calcu	lating Undershoot	Amplitude using the eq	uation:	
		Ur	dershoot Amplitude = V	ss - V _{MIN}	
	b Evaluate T	otal Area Below \	/ss by using Trapezoidal	Method Area	Calculation:

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + y_n \Big)$	$-\frac{y_n}{2}\Big)$
---	-----------------------

Figure 31 Equation for Total_Area_Below_Vss

- *c* To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/ The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JESD209-5C specification.

Overshoot	Area_CS
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Availability Condition: Table 34 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	CS

Test ID & References: Table 35 LPDDR5 Test References from JESD209-5C Specification

Parameter (in Specification)	Test ID	Reference from Specification
Maximum overshoot area above V_{DD2H}/V_{DDQ}	152402	Table 415

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

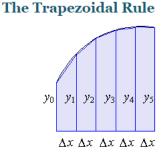
- **Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},\,V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DD2H}$

b Evaluate Area_below_V_{DD2H} using the equation:

Area_below_V_{DD2H} = (OvershootRegion_End - OvershootRegion_Start) x V_{DD2H}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$ext{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

- Figure 32 Equation for Total_Area_Above_OV
 - *d* Calculate Area_Above_ V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_OV - Area_below_V_{DD2H}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - · Area_Above_V_{DD2H}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

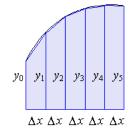
Expected/The Overshoot Amplitude and Area measurement value shall be within the conformance limits as perObservable Results:the JESD209-5C specification.

Undershoot_Area_CS

Availability Condition: Table 36 Set Up tab options for availability of tests

Supported CK Type	Supported WC	CK Type Supports Offline	e? R/W Separation need	led? SE Mode?	Required Signals				
N/A	N/A	Yes	No	Yes	CS				
Test ID & References:	Table 37	LPDDR5 Test References fro	om JESD209-5C Specification						
	Paramete	er (in Specification)	Test ID	Reference	e from Specification				
	Maximum	n undershoot area above VSS	152403	Table 415					
Overview:	from all	The purpose of this test is to verify the undershoot amplitude value of the test signal that is for from all regions of the acquired waveform.							
		of an undershoot, the ur oot amplitude.	ndershoot area is calcul	ated based on t	he undershoot width and				
Procedure:		1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).							
	An "l	2 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.							
	3 With								
	a Ev	valuate Undershoot Amp	plitude by:						
	i	Using T _{MIN} , V _{MIN} to a UndershootRegion.	obtain the time-stamp o	of the minimum	voltage on the				
	ii	i Calculating Undersh	oot Amplitude using the	e equation:					
		Undershoot Amplitude = Vss - V _{MIN}							
				<i>b</i> Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:					

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

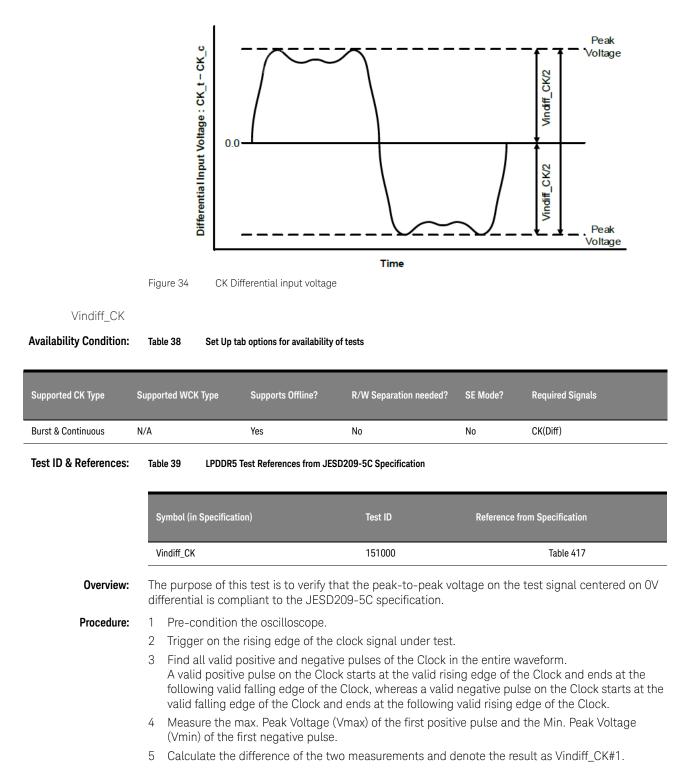
$$igg| \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 33 Equation for Total_Area_Below_Vss

- *c* To find the worst case, save the following calculated results for later use:
 - · Overshoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JESD209-5C specification.

Clock (Diff) Tests



Consider Figure 34 to understand how the minimum input differential voltage is measured at the input receiver.

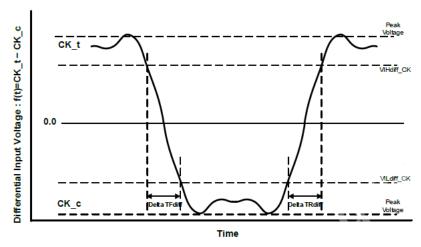
	Vindiff_CK#1 = Vmax - Vmin
	6 Then, measure Vmin of first negative pulse and Vmax of the second positive pulse.
	7 Calculate the difference of the two measurements and denote the result as Vindiff_CK#2.
	8 Continue steps 4 to 7 for measurements on the remaining pulse that was obtained.
	9 Determine the worst result from the set of Vindiff_CK values measured.
Expected/ Observable Results:	The measured value of Vindiff_CK for the test signal shall be within the conformance limits as per the JESD209-5C specification.

Vindiff_CK/2HighPulse

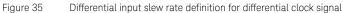
Availability Condition:	Table 40 Set Up	tab options for availability	of tests					
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
Burst & Continuous	N/A	Yes	No	No	CK(Diff)			
Test ID & References:	Test ID & References: Table 41 LPDDR5 Test References from JESD209-5C Specification							
	Symbol (in Specifica	ation)	Test ID	Reference f	from Specification			
			151001		T-11- (17			
	Vindiff_CK		151001		Table 417			
Overview:		his test is to verify t JESD209-5C speci	nat the peak voltage of t fication.	the high puls	se of the test signal is			
Procedure:	1 Pre-conditio	n the oscilloscope.						
	2 Trigger on th	e rising edge of the	clock signal under test.					
	3 Find all valid positive pulses of the Clock in the entire waveform. A valid positive pulse on the Clock starts at the valid rising edge of the Clock and ends at the following valid falling edge of the Clock.							
	4 Zoom into the first pulse and measure the max. Peak Voltage (Vmax). Consider Vmax as the value of Vindiff_CK/2.							
	5 Continue the	previous step with	the rest of the positive p	oulses found	in the specified waveform.			
	6 Determine th	ne worst result from	the set of Vindiff_CK/2	alues that a	re measured.			
/Expected Observable Results:	The measured va the JESD209-50		for the test signal shall	be within the	e conformance limits as per			

Vindiff_CK/2LowPulse

Availability Condition:	Condition: Table 42 Set Up tab options for availability of tests						
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	No	No	CK(Diff)		
Test ID & References:	ICES: Table 43 LPDDR5 Test References from JESD209-5C Specification						
	Symbol (in Specifica	ation)	Test ID	Reference f	rom Specification		
	Vindiff_CK		151002		Table 417		
Overview:		his test is to verify t JESD209-5C speci	hat the peak voltage of t fication.	the low pulse	e of the test signal is		
Procedure:	1 Pre-conditio	n the oscilloscope.					
	2 Trigger on th	e falling edge of the	e clock signal under test				
	A valid nega				the Clock and ends at the		
	4 Zoom into th of Vindiff_CK		easure the min. Peak Vol	tage (Vmin).	Consider Vmin as the value		
	5 Continue the	previous step with	the rest of the negative	pulses found	I in the specified waveform.		
	6 Determine th	ne worst result from	the set of Vindiff_CK/2	values that a	re measured.		
/Expected Observable Results:	The measured va the JESD209-50		for the test signal shall	be within the	e conformance limits as per		



Input slew rate for differential signals are measured as shown in Figure 35.



VIHdiff_CK

Availability Condition: Table 44 Set Up tab options for availability of tests

Table 45

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK(Diff)

Test ID & References:

LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
VIHdiff_CK	151006	Table 420

Overview: The purpose of this test is to verify that the high level differential input voltage value of the test signal is compliant to the JESD209-5C specification.

Procedure:

- 1 Pre-condition the oscilloscope.
- 2 Trigger on the rising edge of the clock signal under test.
- 3 Find all valid Clock positive pulse in the triggered waveform. A valid Clock positive pulse starts at the OV crossing at valid Clock rising edge and ends at the OV crossing at the following valid Clock falling edge.
- 4 Zoom into the first pulse and measure the top voltage V_{TOP} . Here, V_{TOP} is the voltage value on the rising edge after which the signal loses the monotonicity of the slope. Consider the value of V_{TOP} as VIHdiff_CK.
- 5 Continue the previous step for all positive pulses found in the specified waveform.
- 6 Determine the worst result from the set of VIHdiff_CK values that are measured.

Expected/ The worst measured VIHdiff_CK for the test signal shall be within the conformance limits as per the JESD209-5C specification.

VILdiff_CK

Availability Condition: Table 46 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	No	No	CK(Diff)		
Test ID & References:							
Test ID & References: Table 47 LPDDR5 Test References from JESD209-5C Specification							
	Symbol (in Specifica	Symbol (in Specification) Test ID Reference		from Specification			
	VILdiff_CK		151007		Table 420		
Overview:	The purpose of this test is to verify the low level differential input voltage value of the test signal is compliant to the JESD209-5C specification.						
Procedure: Expected/ Observable Results:	 Pre-condition the oscilloscope. Trigger on the rising edge of the clock signal under test. Find all valid Clock negative pulse in the triggered waveform. A valid Clock negative pulse starts at the 0V crossing at valid Clock falling edge and ends at the 0V crossing at the following valid Clock rising edge. Zoom into the first pulse and measure the base voltage V_{BASE}. Here, V_{BASE} is the voltage value on the falling edge after which the signal loses the monotonicity of the slope. Consider the value of V_{BASE} as VILdiff_CK. Continue the previous step for all negative pulses found in the specified waveform. Determine the worst result from the set of VILdiff_CK values that are measured. The worst measured VILdiff_CK for the test signal shall be within the conformance limits as per the JESD209-5C specification. 						
SRIdiffR_CK		tab options for availability	of tests				
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	No	No	CK(Diff)		
Test ID & References: Table 49 LPDDR5 Test References from JESD209-5C Specification							
Symbol (in Specification) Test ID Reference from Specification							
SRIdiffR_CK			151008		Table 421		

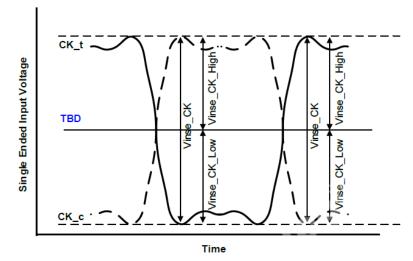
Overview:	The purpose of this test is to verify that the differential input slew rate for rising edge of the Clock signal is compliant to the JESD209-5C specification.
Procedure:	 Pre-condition the oscilloscope. Trigger on the rising edge of the clock signal under test. Find all the valid Clock rising edges in the entire waveform. A valid clock rising edge starts at VILdiff_CK crossing and ends at the following VIHdiff_CK
	 crossing. For all the valid Clock rising edges, measure the transition time, DeltaTRdiff. DeltaTRdiff is the time starting at VILdiff_CK crossing and ending at the following VIHdiff_CK crossing. 5 Calculate SRIdiffR_CK using the equation:
	SRIdiffR_CK = [VIHdiff_CK - VILdiff_CK] / DeltaTRdiff 6 Determine the worst result from the set of SRIdiffR_CK measured.
Expected/ Observable Results:	The measured value of SRIdiffR_CK for the Clock signal shall be within the conformance limits as per the JESD209-5C specification.

SRIdiffF_CK

Availability Condition: Table 50 Set Up tab options for availability of tests

Supported CK Type	Suppo	orted WCK Type	Supports Offline?	R/W Separation needed	SE Mode?	Required Signals
Burst & Continuous	N/A		Yes	No	No	CK(Diff)
Test ID & References:	Tab	ole 51 LPDDR5	i Test References from JI	ESD209-5C Specification		
	s	Symbol (in Specifica	tion)	Test ID	Reference	from Specification
	S	RIdiffF_CK		151009		Table 421
Overview:			nis test is to verify nt to the JESD209	-	ut slew rate fo	or falling edge of the Clock
Procedure:	1	Pre-condition	the oscilloscope.			
	2	Trigger on the	e falling edge of th	e clock signal under te	st.	
	3	Find all the va	alid Clock falling e	dges in the entire wave	form.	
		A valid clock crossing.	falling edge starts	at VIHdiff_CK crossing	and ends at t	he following VILdiff_CK
	4 For all the valid Clock falling edges, measure the transition time, DeltaTFdiff. DeltaTFdiff is the time starting at VIHdiff_CK crossing and ending at the following VILdiff_CK crossing.					
	5	Calculate SRI	diffF_CK using the	equation:		
			SRIdiffF_CI	K = [VILdiff_CK - VIHdif	f_CK] / Delta	ſFdiff
	6	Determine th	e worst result from	n the set of SRIdiffF_CK	measured.	

Expected/ The measured value of SRIdiffF_CK for the Clock signal shall be within the conformance limits as per the JESD209-5C specification.



The minimum input single-ended voltage is measured as shown in Figure 36.

Figure 36 Clock Single-ended Input Voltage definition

Vinse_CK (Positive Pulse)

Availability Condition:	Table 52	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK(Diff)

Test ID & References: Table 53 LPDDR5 Test References from JESD209-5C Specification

s	symbol (in Specification)	Test ID	Reference from Specification
۷	/inse_CK	151010	Table 418

Overview: The purpose of this test is to verify the peak voltage of high pulse.

Procedure: 1 Pre-condition the oscilloscope.

- 2 Trigger on the rising edge of the clock signal under test.
- 3 Find all valid positive pulses of the Clock in the entire waveform. A valid positive pulse on the Clock starts at the valid rising edge of the Clock and ends at the following valid falling edge of the Clock.
- 4 Zoom into the first pulse and measure V_{MAX} .
- 5 Calculate the value of Vinse_CK (Positive Pulse) using the equation:

Vinse_CK (Positive Pulse) = $V_{MAX} - V_{REF}$



For this test, the Test App considers Vref to be ($V_{REFdiff_CK}$), which in turn, is typically set to 0V.

- 6 Continue the previous step with the rest of the positive pulses found in the specified waveform.
- 7 Determine the worst result from the set of Vinse_CK (Positive Pulse) measured.

Expected/The measured value of Vinse_CK (Positive Pulse) for the test signal shall be within the conformanceObservable Results:limits as per the JESD209-5C specification.

- Vinse_CK (Negative Pulse)
- Availability Condition: Table 54 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK(Diff)

Test ID & References:

Table 55 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification	
Vinse_CK	151011	Table 418	

Overview: The purpose of this test is to verify the peak voltage of low pulse.

- **Procedure:** 1 Pre-condition the oscilloscope.
 - 2 Trigger on the falling edge of the clock signal under test.
 - 3 Find all valid negative pulses of the Clock in the entire waveform. A valid negative pulse on the Clock starts at the valid falling edge of the Clock and ends at the following valid rising edge of the Clock.
 - 4 Zoom into the first pulse and measure V_{MIN} .
 - 5 Calculate the value of Vinse_CK (Negative Pulse) using the equation:

Vinse_CK (Negative Pulse) = $V_{REF} - V_{MIN}$



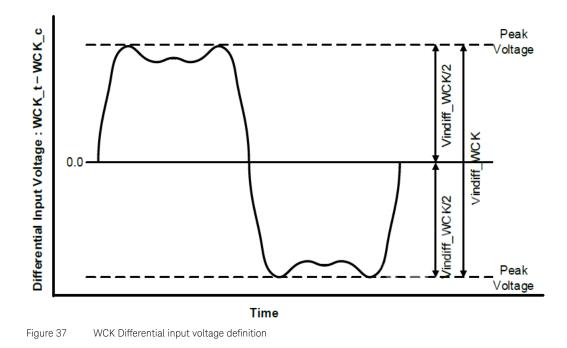
For this test, the Test App considers Vref to be $(V_{REFdiff_CK})$, which in turn, is typically set to OV.

6 Continue the previous step with the rest of the negative pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_CK (Negative Pulse) measured.

Expected/ The measured value of Vinse_CK (Negative Pulse) for the test signal shall be within the conformance limits as per the JESD209-5C specification.

Write Clock (Diff) Tests



Consider Figure 37 to understand how the minimum input differential voltage is measured at the input receiver.

Vindiff_WCK

Availability Condition:	Table 56	Set Up tab options for availability of tests
-------------------------	----------	--

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ

Test ID & References: Table 57 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
Vindiff_WCK	151100	Table 423

Overview: The purpose of this test is to verify that the peak-to-peak voltage on the test signal centered on OV differential is compliant to the JESD209-5C specification.

Procedure:

- 1 Pre-condition the oscilloscope.
- 2 Trigger on the rising edge of the Write Clock signal under test.
- 3 Find all valid positive and negative pulses of the Write Clock in the entire waveform. A valid positive pulse on the Write Clock starts at the valid rising edge of the Write Clock and ends at the following valid falling edge of the Write Clock, whereas a valid negative pulse on the

Write Clock starts at the valid falling edge of the Write Clock and ends at the following valid rising edge of the Write Clock.

- 4 Measure the max. Peak Voltage (Vmax) of the first positive pulse and the Min. Peak Voltage (Vmin) of the first negative pulse.
- 5 Calculate the difference of the two measurements and denote the result as Vindiff_WCK#1.

Vindiff_WCK#1 = Vmax - Vmin

- 6 Then, measure Vmin of first negative pulse and Vmax of the second positive pulse.
- 7 Calculate the difference of the two measurements and denote the result as Vindiff_WCK#2.
- 8 Continue steps 4 to 7 for measurements on the remaining pulse that was obtained.
- 9 Determine the worst result from the set of Vindiff_WCK values measured.

Expected/ The measured value of Vindiff_WCK for the test signal shall be within the conformance limits as per the JESD209-5C specification.

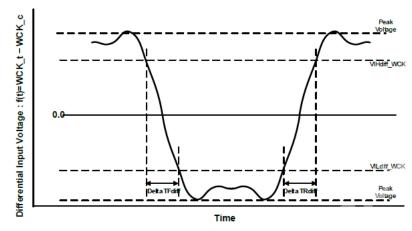
Vindiff_WCK/2HighPulse

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ	
Test ID & References:	es: Table 59 LPDDR5 Test References from JESD209-5C Specification					
	Symbol (in Specifica	ation)	Test ID	Reference	from Specification	
	Vindiff_WCK		151101	Table 423		
Overview:	 The purpose of t	his test is to verify t JESD209-5C speci	hat the peak voltage of		se of the test signal is	
Overview: Procedure:	The purpose of t compliant to the	,	hat the peak voltage of		se of the test signal is	
	The purpose of t compliant to the 1 Pre-condition	JESD209-5C speci n the oscilloscope.	hat the peak voltage of	the high puls	se of the test signal is	
	The purpose of t compliant to the Pre-condition Trigger on th Find all valid A valid positi	JESD209-5C speci n the oscilloscope. e rising edge of the positive pulses of the ve pulse on the Wri	hat the peak voltage of fication. Write Clock signal unde he Write Clock in the en te Clock starts at the va	the high puls er test. tire waveforr lid rising edg	Ĵ	
	The purpose of t compliant to the Pre-condition Trigger on th Find all valid A valid positi ends at the fi Zoom into th	JESD209-5C speci n the oscilloscope. e rising edge of the positive pulses of the ve pulse on the Wri ollowing valid falling	hat the peak voltage of fication. Write Clock signal unde he Write Clock in the en te Clock starts at the va g edge of the Write Cloc	the high puls er test. tire waveforr lid rising edg k.	n.	
	The purpose of t compliant to the Pre-condition Trigger on th Find all valid A valid positi ends at the fi Zoom into th of Vindiff_W0	JESD209-5C speci n the oscilloscope. e rising edge of the positive pulses of th ve pulse on the Wri ollowing valid falling e first pulse and me CK/2HighPulse.	hat the peak voltage of fication. Write Clock signal unde he Write Clock in the en te Clock starts at the va g edge of the Write Cloc asure the max. Peak Vol	the high puls er test. tire waveforr lid rising edg k. tage (Vmax).	m. ge of the Write Clock and	

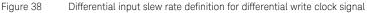
Vindiff_WCK/2LowPulse

Availability Condition:	Table 60	Set Up tab options for availability of tests
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Supported CK Type	Supported	WCK Туре	Supports Offline?	R/W Separation	needed? SE Mode?	Required Signals
Burst & Continuous	Burst		Yes	No	No	CK(Diff), WCK(Diff), DQ
Test ID & References:	Table 61	LPDDR	5 Test References from J	IESD209-5C Specificat	ion	
	Symbo	ol (in Specifica	ation)	Test ID	Referen	ce from Specification
	Vindiff	_WCK		151102	Table 42	23
Overview:			his test is to verify JESD209-5C spe		tage of the low p	ulse of the test signal is
Procedure:	1 Pre	e-conditio	n the oscilloscope.			
	2 Tri	gger on th	e falling edge of th	ne Write Clock sig	gnal under test.	
	3 Find all valid negative pulses of the Write Clock in the entire waveform. A valid negative pulse on the Write Clock starts at the valid falling edge of the Wri ends at the following valid rising edge of the Write Clock.					
			e first pulse and m CK/2LowPulse.	neasure the min. I	Peak Voltage (Vmi	n). Consider Vmin as the value
	5 Cc	ntinue the	previous step with	h the rest of the r	egative pulses for	und in the specified waveform.
	6 De	termine th	ne worst result fror	n the set of Vindi	f_WCK/2LowPuls	e values that are measured.
/Expected Observable Results:			alue of Vindiff_WC JESD209-5C spec		the test signal sha	all be within the conformance



Input slew rate for differential WCK signals are measured as shown in Figure 38.



VIHdiff_WCK

Availability Condition:	Table 62	Set Up tab options for availability of tests
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Table 63

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ

Test ID & References:

LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
VIHdiff_WCK	151106	Table 426

Overview: The purpose of this test is to verify that the high level differential input voltage value of the test signal is compliant to the JESD209-5C specification.

Procedure: 1 Pre-condition the oscilloscope.

- 2 Trigger on the rising edge of the Write Clock signal under test.
- 3 Find all valid Write Clock positive pulse in the triggered waveform. A valid Write Clock positive pulse starts at the 0V crossing at valid Write Clock rising edge and ends at the 0V crossing at the following valid Clock falling edge.
- 4 Zoom into the first pulse and measure the top voltage V_{TOP} . Here, V_{TOP} is the voltage value on the rising edge after which the signal loses the monotonicity of the slope. Consider the value of V_{TOP} as VIHdiff_WCK.
- 5 Continue the previous step for all positive pulses found in the specified waveform.
- 6 Determine the worst result from the set of VIHdiff_WCK values that are measured.

Expected/ The worst measured VIHdiff_WCK for the test signal shall be within the conformance limits as per the JESD209-5C specification.

VILdiff_WCK

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ
Test ID & References:	Table 65 LPDD	PR5 Test References from JE	SD209-5C Specification		
	Symbol (in Specifi	cation)	Test ID	Reference	from Specification
	VILdiff_WCK		151107	Table 426	
Overview:		this test is to verify t this JESD209-5C spec		input voltag	e value of the test signal is
Procedure:		on the oscilloscope.			
	3 Find all vali A valid Writ	d Write Clock negati e Clock negative pul	Write Clock signal under ve pulse in the triggered se starts at the OV cross ollowing valid Write Cloc	waveform. ing at valid ^v	Write Clock falling edge and e.
	4 Zoom into t on the fallir	the first pulse and me	easure the base voltage he signal loses the mon	V _{BASE} . Here	, V_{BASE} is the voltage value
			ll negative pulses found		
Expected/ Observable Results:		sured VILdiff_WCK fo	the set of VILdiff_WCK v		are measured. onformance limits as per th
SRIdiffR_W(СК				
Availability Condition:	Table 66 Set L	Ip tab options for availability	of tests		

Test ID & References: Table 67 LPDDR5 Test References from JESD209-5C Specification

Yes

Symbol (in Specification)	Test ID	Reference from Specification
SRIdiff_WCK	151108	Table 427

No

No

CK(Diff), WCK(Diff), DQ

Burst

Burst & Continuous

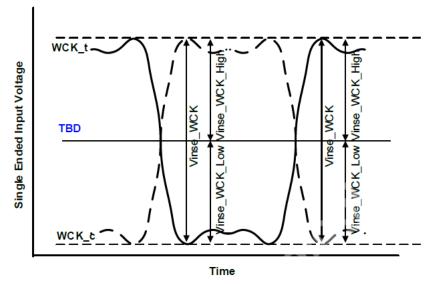
Overview:	The purpose of this test is to verify that the differential input slew rate for rising edge of the Write Clock signal is compliant to the JESD209-5C specification.
Procedure:	1 Pre-condition the oscilloscope.
	2 Trigger on the rising edge of the Write Clock signal under test.
	3 Find all the valid Write Clock rising edges in the entire waveform.
	A valid Write Clock rising edge starts at VILdiff_WCK crossing and ends at the following VIHdiff_WCK crossing.
	4 For all the valid Write Clock rising edges, measure the transition time, DeltaTRdiff. DeltaTRdiff is the time starting at VILdiff_WCK crossing and ending at the following VIHdiff_WCK crossing.
	5 Calculate SRIdiffR_WCK using the equation:
	SRIdiffR_WCK = [VIHdiff_WCK - VILdiff_WCK] / DeltaTRdiff
	6 Determine the worst result from the set of SRIdiffR_WCK measured.
Expected/ Observable Results:	The measured value of SRIdiffR_WCK for the Write Clock signal shall be within the conformance limits as per the JESD209-5C specification.

SRIdiffF_WCK

Availability Condition: Table 68 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ	
Test ID & References:	Table 69 LPDDF	5 Test References from JE	SD209-5C Specification			
	Symbol (in Specific	ation)	Test ID	Reference f	rom Specification	
	SRIdiff_WCK		151109	Table 427		
Overview:		,	1	t slew rate fo	r falling edge of the Write	
Procedure:	 Clock signal is compliant to the JESD209-5C specification. Pre-condition the oscilloscope. Trigger on the falling edge of the Write Clock signal under test. Find all the valid Write Clock falling edges in the entire waveform. A valid Write Clock falling edge starts at VIHdiff_WCK crossing and ends at the following VILdiff_WCK crossing. For all the valid Write Clock falling edges, measure the transition time, DeltaTFdiff. DeltaTFdiff is the time starting at VIHdiff_WCK crossing and ending at the following VILdiff_WCK crossing. Calculate SRIdiffF_WCK using the equation: SRIdiffF_WCK = [VILdiff_WCK - VIHdiff_WCK] / DeltaTFdiff 					
	6 Determine t	_	the set of SRIdiffF_WCk		ται ΓοιΠ	

Expected/The measured value of SRIdiffF_WCK for the Write Clock signal shall be within the conformanceObservable Results:limits as per the JESD209-5C specification.



Input slew rate for differential WCK signals are measured as shown in Figure 38.

Figure 39 Differential input slew rate definition for differential write clock signal

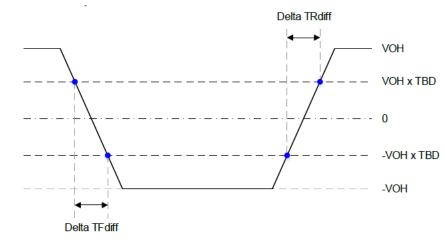
Vinse_WCK (Positive Pulse)

Availability Condition: Table 70 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ
Test ID & References:	Table 71 LPDI	OR5 Test References from JE	SD209-5C Specification		
	Symbol (in Specif	ication)	Test ID	Reference	from Specification
	Vinse_WCK		151110	Table 424	
Overview:	The purpose o	f this test is to verify t	he peak voltage of high	pulse.	
Overview: Procedure:		f this test is to verify t ion the oscilloscope.	he peak voltage of high	pulse.	
	1 Pre-condit	ion the oscilloscope.	he peak voltage of high Write Clock signal unde		
	 Pre-condition Trigger on Find all valing A valid position 	ion the oscilloscope. the rising edge of the id positive pulses of th itive pulse on the Wri	Write Clock signal unde ne Write Clock in the en	er test. tire wavefori lid rising edg	m. ge of the Write Clock and
	 Pre-condition Trigger on Find all valid position A valid position A the 	ion the oscilloscope. the rising edge of the id positive pulses of th itive pulse on the Wri	Write Clock signal unden ne Write Clock in the en te Clock starts at the val g edge of the Write Cloc	er test. tire wavefori lid rising edg	

Vinse_WCK (Positive Pulse) = $V_{MAX} - V_{REF}$

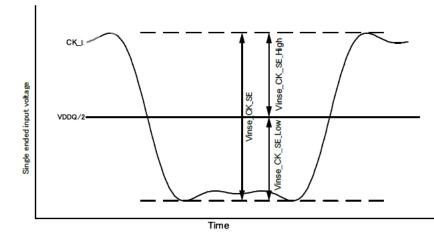
	NOTE	For this test, is typically s		s Vref to be	(V _{REFdiff_WCK}), which in turn,
Expected/ Observable Results:	7 Determine the The measured val	e worst result from	the set of Vinse_WCK (Positive Pulse) for the te	Positive Puls	l in the specified waveform. e) measured. all be within the conformance
Vinse_WCK Availability Condition:	(Negative Pulse) Table 72 Set Up ta	ab options for availability	of tests		
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ
Test ID & References:	Table 73 LPDDR5 Symbol (in Specificat	Test References from JE	SD209-5C Specification Test ID	Reference	from Specification
	Vinse_WCK		151111	Table 424	
Test Overview:	The purpose of th	is test is to verify t	he peak voltage of low p	oulse.	
Test Procedure:	 2 Trigger on the 3 Find all valid r A valid negati ends at the fo 4 Zoom into the 	negative pulses of ve pulse on the Wr llowing valid rising first pulse and me value of Vinse_WC	edge of the Write Cloc	ntire wavefo alid falling e k. g the equati	dge of the Write Clock and on:
	NOTE	For this test, typically set		s Vref to be (V _{REFdiff_CK}), which in turn, is
Expected/ Observable Results:	7 Determine the The measured val	e worst result from ue of Vinse_WCK (the rest of the negative the set of Vinse_WCK (Negative Pulse) for the 209-5C specification.	Negative Pu	



Output slew rate for differential signals are measured as shown in Figure 40.

Figure 40 Differential output slew rate definition for WCK signal

Clock (SE Mode) Tests



The minimum single-ended CK input voltage is measured as shown in Figure 41.

Figure 41 Single-ended mode CK input Voltage definition

Vinse_CK_SE

Availability Condition:	Table 74	Set Up tab options for availability of tests
-------------------------	----------	--

Supported CK Type	Suppo	orted WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A		Yes	No	Yes	CK(Diff)
Test ID & References:	Tal	ble 75 LPDDR	5 Test References from JE	SD209-5C Specification		
	ę	Symbol (in Specifica	tion)	Test ID	Reference	from Specification
	١	Vinse_CK_SE		251000		Table 432
Overview:				hat the peak-to-peak 99-5C specification.	voltage on the	e test signal centered on
Procedure:	1	Pre-condition	n the oscilloscope.			
	2	Trigger on th	e rising edge of the	clock signal under tes	t.	
	3 Find all valid positive and negative pulses of the Clock in the entire waveform. A valid positive pulse on the Clock starts at the valid rising edge and ends at the following falling edge, whereas a valid negative pulse on the Clock starts at the valid falling edge and at the following valid rising edge.					d ends at the following valid
	4		max. Peak Voltage first negative pulse		tive pulse and	d the Min. Peak Voltage
	5	Calculate the	e difference of the t	wo measurements and	denote the re	esult as Vinse_CK_SE#1.
			١	/inse_CK_SE#1 = Vma>	- Vmin	

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	6 Then, measure Vmin of first negative pulse and Vmax of the second positive pulse.
	7 Calculate the difference of the two measurements and denote the result as Vinse_CK_SE#2.
	8 Continue steps 4 to 7 for measurements on the remaining pulse that was obtained.
	9 Determine the worst result from the set of Vinse_CK_SE values measured.
Expected/ Observable Results:	The measured value of Vinse_CK_SE for the test signal shall be within the conformance limits as per the JESD209-5C specification.

Vinse_CK_SE_High

Availability Condition:	Table 76	Set Up tab options for availability of tests
-------------------------	----------	--

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

Test ID & References: Table 77 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_CK_SE_High	251012	Table 432

Test Overview: The purpose of this test is to verify the peak voltage of high pulse.

Test Procedure:

1 Pre-condition the oscilloscope.

- 2 Trigger on the rising edge of the clock signal under test.
- 3 Find all valid positive pulses of the Clock in the entire waveform. A valid positive pulse on the Clock starts at the valid rising edge and ends at the following valid falling edge.
- 4~ Zoom into the first pulse and measure $V_{\text{MAX}}.$
- 5 Calculate the value of Vinse_CK_SE_High using the equation:

 $Vinse_CK_SE_High = V_{MAX} - V_{REF}$

NOTE

For this test, the Test App considers Vref to be $(V_{DDQ}/2)$.

- 6 Continue the previous step with the rest of the positive pulses found in the specified waveform.
- 7 Determine the worst result from the set of Vinse_CK_SE_High measured.

Expected/ The measured value of Vinse_CK_SE_High for the test signal shall be within the conformance limits **Observable Results:** as per the JESD209-5C specification.

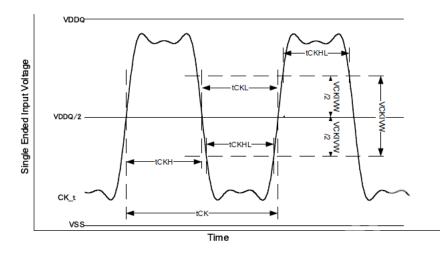
Vinse_CK_SE_Low

Availability Condition:	Table 78	Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)	
Test ID & References:	Table 79 LPDDR5	Test References from JE	SD209-5C Specification			
	Symbol (in Specification	on)	Test ID	Reference f	from Specification	
	Vinse_CK_Low		251014	Table 432		
Overview:	The purpose of thi	s test is to verify t	he peak voltage of low p	oulse.		
Procedure:	1 Pre-condition	the oscilloscope.				
	2 Trigger on the	falling edge of the	e clock signal under test			
	A valid negativ	3 Find all valid negative pulses of the Clock in the entire waveform. A valid negative pulse on the Clock starts at the valid falling edge of the Clock and ends at the following valid rising edge of the Clock.				
	4 Zoom into the	first pulse and me	easure V _{MIN} .			
	5 Calculate the	value of Vinse_CK	_SE_Low using the equa	tion:		
	$Vinse_CK_SE_Low = V_{REF} - V_{MIN}$					
	NOTE For this test, the Test App considers Vref to be (V _{DDQ} /2).					
	6 Continue the p	previous step with	the rest of the negative	pulses found	d in the specified waveform.	

7 Determine the worst result from the set of Vinse_CK_SE_Low measured.

Expected/ The measured value of Vinse_CK_SE_Low for the test signal shall be within the conformance limits as per the JESD209-5C specification.



The single-ended clock input slew rate can be measured as shown in Figure 42.

Figure 42 Single-ended mode CK pulse definitions

SRIseR_CKSE

Availability Condition:	Table 80	Set Up tab options for availability of tests
-------------------------	----------	--

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)
Test ID & References:	Table 81 LPDD)R5 Test References from JE	SD209-5C Specification		
	Symbol (in Specif	ication)	Test ID	Reference	from Specification
	SRICKSE		251008		Table 432
Overview:		this test is to verify t iant to the JESD209-	0	out slew rate	e for rising edge of the Clock
Procedure:	1 Pre-conditi	on the oscilloscope.			
	2 Trigger on	the rising edge of the	Clock (CK) signal under	r test.	
		0 0	s in the entire waveform e following VIH_CK cross		ck rising edge starts at
	4 For all the	valid CK rising edges	, measure the transition	time, DeltaT	Rdiff.
	DeltaTRdiff	is the time starting a	at VIL_CK crossing and e	nding at the	e following VIH_CK crossing.
	5 Calculate S	RIseR_CKSE using th	ne equation:		
		SRIseR_C	CKSE = [VIH_CK - VIL_C	K] / DeltaTR	diff
		where,	VIH_CK = ([VDDQ/2] + [VCKIVW/2]))
		VIL	CK = ([VDDQ/2] - [VCk	(IVW/2])	
	6 Determine	the worst result from	the set of SRIseR_CKSE	E measured.	

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Expected/ The measured value of SRIseR_CKSE for the Clock signal shall be within the conformance limits as per the JESD209-5C specification.

SRIseF_CKSE

Availability Condition:	Table 82	Set Up tab options for availability of tests	
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

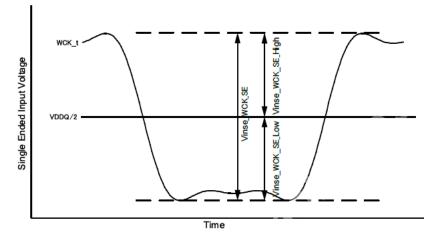
Test ID & References: Table 83 LPDDR5 Test References from JESD209-5C Specification

	Symbol (in Specification)	Test ID	Reference from Specification
	SRICKSE	251009	Table 432
Overview:	The purpose of this test is to signal is compliant to the JE	, , , , , , , , , , , , , , , , , , , ,	out slew rate for falling edge of the Clock
Procedure:	 Find all the valid CK falli VIH_CK crossing and en For all the valid CK fallir 	ge of the Clock (CK) signal under ing edges in the entire waveform ds at the following VIL_CK cross ng edges, measure the transition tarting at VIH_CK crossing and e	n. A valid Clock falling edge starts at sing.
		RIseF_CKSE = [VIL_CK - VIH_CH where, VIH_CK = ([VDDQ/2] + VIL_CK = ([VDDQ/2] - [VCH ult from the set of SRIseF_CKSE	[VCKIVW/2]) (IVW/2])

Expected/ The measured value of SRIseF_CKSE for the Clock signal shall be within the conformance limits as per the JESD209-5C specification.

4 Electrical Tests

Write Clock (SE Mode) Tests



The minimum single-ended WCK input voltage is measured as shown in Figure 41.

Figure 43 Single-ended mode WCK input Voltage definition

Vinse_WCK_SE

Availability Condition: Table 84 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	Burst	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ		
Test ID & References:	Table 85 LPD	Table 85 LPDDR5 Test References from JESD209-5C Specification					
	Symbol (in Spec	fication)	Test ID	Reference	from Specification		
	Vinse_WCK_SE		251100	Table 431			
Overview:		of this test is to verify t mpliant to the JESD2(oltage on the	e test signal centered on		
Procedure:	1 Pre-condi	ion the oscilloscope.					
	2 Trigger on	the rising edge of the	write clock signal unde	r test.			
	3 Find all valid positive and negative pulses of the Write Clock in the entire waveform. A valid positive pulse on the Write Clock starts at the valid rising edge and ends at the followin valid falling edge, whereas a valid negative pulse on the Write Clock starts at the valid falling edge and ends at the following valid rising edge.						
	 4 Measure the max. Peak Voltage (Vmax) of the first positive pulse and the Min. Peak Voltage (Vmin) of the first negative pulse. 						
	5 Calculate	the difference of the t	wo measurements and c	lenote the re	esult as Vinse_WCK_SE#1.		
		Vi	neo WCK SE#1 - Vmay	Vmin			

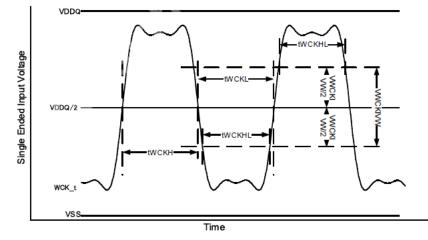
Vinse_WCK_SE#1 = Vmax - Vmin

Expected/ Observable Results: Vinse_WCK	 7 Calculate the 8 Continue stee 9 Determine the The measured value per the JESD205 	e difference of the tw ps 4 to 7 for measu ne worst result from	rements on the remainir the set of Vinse_WCK_S	enote the re ng pulse tha SE values m	esult as Vinse_WCK_SE#2. t was obtained.
Availability Condition:	-	tab options for availability	r of tests		
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ
Test ID & References:	Table 87 LPDDR Symbol (in Specifica	5 Test References from JE ation)	SD209-5C Specification Test ID	Reference	from Specification
	Vinse_WCK_SE_Hig	h	251112	Table 431	
Overview:		his test is to verify t JESD209-5C speci	hat the peak voltage of the first the peak voltage of the first term of	the high pul	lse of the test signal is
Procedure:	 Pre-condition the oscilloscope. Trigger on the rising edge of the write clock signal under test. Find all valid positive pulses of the Write Clock in the entire waveform. A valid positive pulse on the Write Clock starts at the valid rising edge and ends at the following valid falling edge. Zoom into the first pulse and measure V_{MAX}. Calculate the value of Vinse_WCK_SE_High using the equation: Vinse_WCK_SE_High = V_{MAX} - V_{REF} NOTE For this test, the Test App considers Vref to be (V_{refDQ}/2). Continue the previous step with the rest of the positive pulses found in the specified waveform. 				
Expected/ Observable Results:	The measured va			-	asured. within the conformance limits

Vinse_WCK_SE_Low

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ
est ID & References:	Table 89 LPDDR5	Test References from JES	SD209-5C Specification		
	Symbol (in Specificat	ion)	Test ID	Reference	from Specification
	Vinse_WCK_SE_Low		251114	Table 431	
Overview:		nis test is to verify t JESD209-5C speci	hat the peak voltage of fication.	the low puls	e of the test signal is
Procedure:	1 Pre-condition	1 Pre-condition the oscilloscope.			
	2 Trigger on the	e falling edge of the	e write clock signal unde	er test.	
	3 Find all valid negative pulses of the Write Clock in the entire waveform. A valid negative pulse on the Write Clock starts at the valid falling edge of the Clock and ends the following valid rising edge of the Write Clock.				
	-	e first pulse and me			
	5 Calculate the	value of Vinse_WC	K_SE_Low using the eq	uation:	
	Vinse_WCK_SE_Low = $V_{REF} - V_{MIN}$				
	NOTE	For this test,	the Test App considers	s Vref to be (V _{refDQ} /2).

Expected/The measured value of Vinse_WCK_SE_Low for the test signal shall be within the conformance limitsObservable Results:as per the JESD209-5C specification.



The single-ended write clock input slew rate can be measured as shown in Figure 44.

Figure 44 Single-ended mode WCK pulse definitions

SRIseR_WCKSE

Availability Condition:	Table 90	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK	Type Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ
Test ID & References:	Table 91	LPDDR5 Test References from	n JESD209-5C Specification		
	Symbol (in	Specification)	Test ID	Reference	from Specification
	SRIWCKSE		251108	Table 431	
Overview:			fy that the single-ended in IESD209-5C specification.	put slew rat	e for rising edge of the Writ
Procedure:	 Trigge Find a at VIL For all Delta crossi 	 2 Trigger on the rising edge of the Write Clock (WCK) signal under test. 3 Find all the valid WCK rising edges in the entire waveform. A valid Write Clock rising edge at VIL_WCK crossing and ends at the following VIH_WCK crossing. 4 For all the valid WCK rising edges, measure the transition time, DeltaTRdiff. DeltaTRdiff is the time starting at VIL_WCK crossing and ending at the following VIH_WCK crossing. 5 Calculate SRIseR_WCKSE using the equation: SRIseR_WCKSE = [VIH_WCK - VIL_WCK] / DeltaTRdiff 			
			, VIH_WCK = ([VDDQ/2] + WCK = ([VDDQ/2] - [VW	-	[2])
	C Deter				-I

6 Determine the worst result from the set of SRIseR_WCKSE measured.

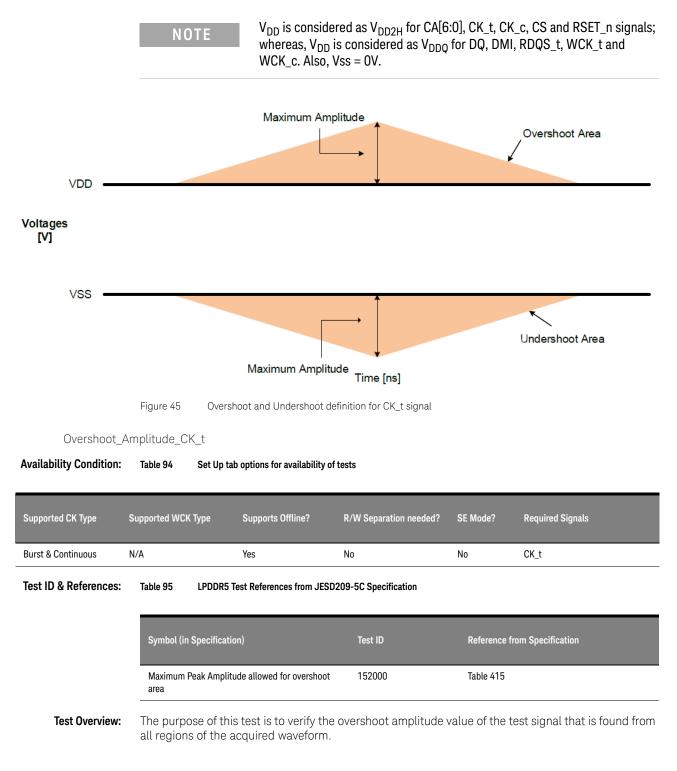
Expected/ The measured value of SRIseR_WCKSE for the Write Clock signal shall be within the conformance limits as per the JESD209-5C specification.

SRIseF_WCKSE

Availability Condition:	Table 92 Set Up t	ab options for availability	of tests		
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ
Test ID & References:	Table 93 LPDDR5	Test References from JES	D209-5C Specification		
	Symbol (in Specificat	ion)	Test ID	Reference f	rom Specification
	SRIWCKSE		251109	Table 431	
Overview:			nat the single-ended inp D209-5C specification.	out slew rate	for falling edge of the Write
Procedure:	1 Pre-condition	the oscilloscope.			
	00	0 0	Write Clock (WCK) sign		
		3 Find all the valid WCK falling edges in the entire waveform. A valid Write Clock falling edge start at VIH_WCK crossing and ends at the following VIL_WCK crossing.			
	4 For all the val				
	DeltaTFdiff is the time starting at VIH_WCK crossing and ending at the following VIL_WCK crossing.				he following VIL_WCK
	5 Calculate SRI	seF_WCKSE using	the equation:		
		SRIseF_WCK	SE = [VIL_WCK - VIH_V	VCK] / Delta	TFdiff
		where, VII	H_WCK = ([VDDQ/2] + [VWCKIVW/2	2])
		_	/CK = ([VDDQ/2] - [VW		
	6 Determine the	e worst result from	the set of SRIseF_WCKS	SE measured	l.
Expected/ Observable Results:		lue of SRIseF_WCK JESD209-5C specif		signal shall b	e within the conformance

Clock (SE) CK_t (Clock Plus) tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 45.



When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

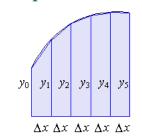
- **Test Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},\,V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DD2H}$

b Evaluate Area_below_V_{DD2H} using the equation:

Area_below_V_{DD2H} = (OvershootRegion_End - OvershootRegion_Start) x V_{DD2H}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



The Trapezoidal Rule

$$\mathrm{Area}pprox rac{1}{2}(y_0+y_1)\Delta x+rac{1}{2}(y_1+y_2)\Delta x+rac{1}{2}(y_2+y_3)\Delta x+\dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$\mathrm{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_n}{2}\Big)$$

Figure 46 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_OV - Area_below_V_{DD2H}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DD2H}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

ed/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as perthe JESD209-5C specification.

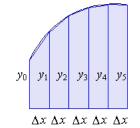
Expected/ Observable Results:

Undershoot_Amplitude_CK_t

Availability Condition: Table 96 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK_t
Test ID & References:	Table 97 LPDDR	5 Test References from JE	SD209-5C Specification		
	Symbol (in Specifica	ation)	Test ID	Reference	from Specification
	Maximum Peak Amp area	litude allowed for undersh	oot 152001	Table 415	
Test Overview:	The purpose of this test is to verify the undershoot amplitude value of the test signal that is foun from all regions of the acquired waveform.				
	In case of an uno Calculation.	In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method A Calculation.			
Test Procedure:		uire signal data and e adjustment).	perform signal conditio	ning to max	imize screen resolution
	2 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (0V) crossing and ends at the risin of Vss (0V) crossing.				g and ends at the rising edge
	3 Within Unde	rshootRegion # 1:			
	a Evaluate l	Jndershoot Amplitu	de by:		
		g T _{MIN} , V _{MIN} to obta ershootRegion.	in the time-stamp of the	e minimum v	voltage on the
	ii Calcu	ulating Undershoot	Amplitude using the equ	uation:	
		Un	dershoot Amplitude = V	ss – V _{MIN}	
	b Evaluate T	otal_Area_Below_V	ss by using Trapezoidal	Method Area	a Calculation:

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg[\operatorname{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_0}{2}\Big)$	$\left(\frac{l_n}{2}\right)$
---	------------------------------

Figure 47 Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JESD209-5C specification.

Availability Condition:	Table 98	Set Up tab options for availabilit	ty of tests		
Supported CK Type	Supported WCK	Type Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK_t
Test ID & References:	Table 99	LPDDR5 Test References from J	ESD209-5C Specification		
	Symbol (in S	Specification)	Test ID	Reference	from Specification
	Maximum ov	vershoot area above V _{DD2H} /V _{DDQ}	152002	Table 415	

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

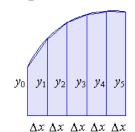
- **Test Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},\,V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

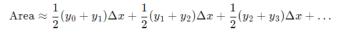
Overshoot Amplitude = $V_{MAX} - V_{DD2H}$

b Evaluate Area_below_V_{DD2H} using the equation:

Area_below_V_{DD2H} = (OvershootRegion_End - OvershootRegion_Start) x V_{DD2H}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:





We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$\mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

- Figure 48 Equation for Total_Area_Above_OV
 - *d* Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_OV - Area_below_V_{DD2H}

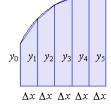
- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DD2H}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JESD209-5C specification.

Undershoot_Area_CK_t

Availability Condition: Table 100 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	N/A	Yes	No	No	CK_t	
Test ID & References:	Table 101 LPDDR5	Test References from JE	SD209-5C Specification			
	Symbol (in Specificat	ion)	Test ID	Reference	from Specification	
	Maximum undershoot	t area above VSS	152003	Table 415		
Test Overview:	from all regions o	The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.				
Test Procedure:	1 Sample/acqu (vertical scale		perform signal conditio	ning to maxi	mize screen resolution	
	2 Find the "Und An "Undersho	 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (0V) crossing and ends at the rising edg of Vss (0V) crossing. 				
	3 Within Under					
		a Evaluate Undershoot Amplitude by:				
		 Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion. 				
	ii Calcul	ating Undershoot	Amplitude using the equ	lation:		
		Und	dershoot Amplitude = Vs	ss - V _{MIN}		
	b Evaluate To	otal_Area_Below_V	ss by using Trapezoidal	Method Area	a Calculation:	
		The Trapez	oidal Rule			
		K				



 $\operatorname{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$

We can simplify this to give us the $\ensuremath{\mathbf{Trapezoidal\ Rule}}$, for n trapezoids:

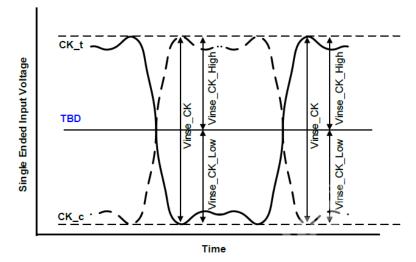
$$\mathrm{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_n}{2}\Big)$$

Figure 49

Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JESD209-5C specification.



The minimum input single-ended voltage is measured as shown in Figure 50.

Figure 50 Clock Single-ended Input Voltage definition

Vinse_CK_High (CK_t)

Availability Condition:	Table 102	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK_t

Test ID & References: Table 103 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_CK_High	151012	Table 418

Test Overview: The purpose of this test is to verify the peak voltage of high pulse.

Test Procedure:

1 Pre-condition the oscilloscope.

- 2 Trigger on the rising edge of the clock signal under test.
- 3 Find all valid positive pulses of the Clock in the entire waveform. A valid positive pulse on the Clock starts at the valid rising edge and ends at the following valid falling edge.
- 4~ Zoom into the first pulse and measure $V_{\text{MAX}}.$
- 5 Calculate the value of Vinse_CK_High (CK_t) using the equation:

Vinse_CK_High (CK_t) = $V_{MAX} - V_{REF}$

NOTE

For this test, the Test App considers Vref to be VrefCA configuration value (set under Measurement Thresholds).

- 6 Continue the previous step with the rest of the positive pulses found in the specified waveform.
- 7 Determine the worst result from the set of Vinse_CK_High (CK_t) measured.

Expected/ The measured value of Vinse_CK_High (CK_t) for the test signal shall be within the conformance limits as per the JESD209-5C specification.

Vinse_CK_Low (CK_t)

Availability Condition: Table 104 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK_t

Test ID & References:

Table 105 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification	
Vinse_CK_Low	151014	Table 418	

Overview: Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the falling edge of the clock signal under test.

The purpose of this test is to verify the peak voltage of low pulse.

- 3 Find all valid negative pulses of the Clock in the entire waveform. A valid negative pulse on the Clock starts at the valid falling edge and ends at the following valid rising edge of the Clock.
- 4 Zoom into the first pulse and measure V_{MIN} .
- 5 Calculate the value of Vinse_CK_Low (CK_t) using the equation:

Vinse_CK_Low (CK_t) = $V_{REF} - V_{MIN}$



For this test, the Test App considers Vref to be VrefCA configuration value (set under Measurement Thresholds).

6 Continue the previous step with the rest of the negative pulses found in the specified waveform.

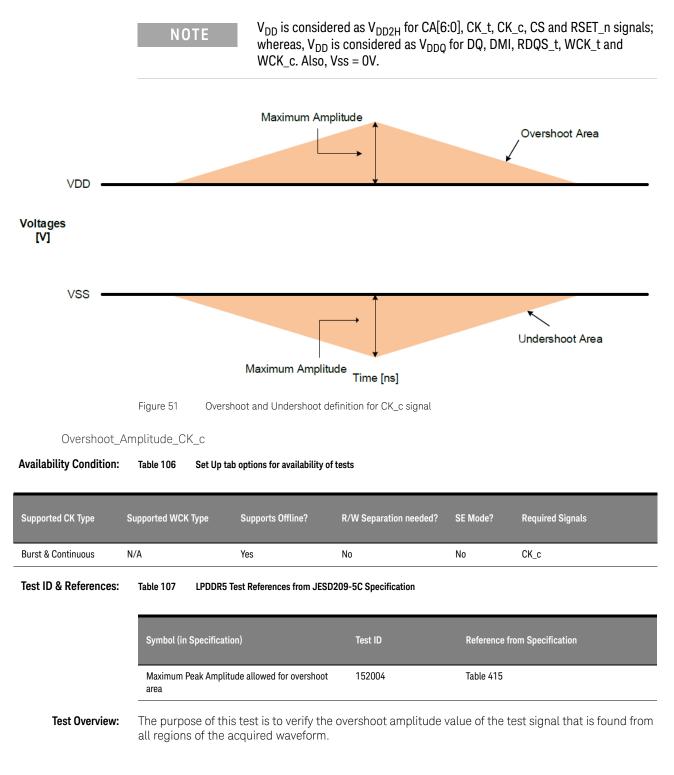
7 Determine the worst result from the set of Vinse_CK_Low (CK_t) measured.

Expected/ The mean **Observable Results:** as per the mean **observable**

The measured value of Vinse_CK_Low (CK_t) for the test signal shall be within the conformance limits
 as per the JESD209-5C specification.

Clock (SE) CK_c (Clock Minus) tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 51.



When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

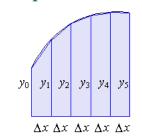
- **Test Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},\,V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DD2H}$

b Evaluate Area_below_V_{DD2H} using the equation:

Area_below_V_{DD2H} = (OvershootRegion_End - OvershootRegion_Start) x V_{DD2H}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



The Trapezoidal Rule

$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$\mathrm{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_n}{2}\Big)$$

Figure 52 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_OV - Area_below_V_{DD2H}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DD2H}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

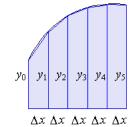
Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JESD209-5C specification.

Undershoot_Amplitude_CK_c

Availability Condition: Table 108 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
Burst & Continuous	N/A	Yes	No	No	CK_c			
Test ID & References:	Table 109 LPDDR5 Test References from JESD209-5C Specification							
	Symbol (in Specification) Test ID Reference from Specifi				from Specification			
	Maximum Peak Amplitude allowed for undershoot area		oot 152005	Table 415				
Test Overview:	The purpose of this test is to verify the undershoot amplitude value of the test signal that is for from all regions of the acquired waveform.							
	In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.							
Test Procedure:	1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).							
	g and ends at the rising edge							
	of Vss (0V) crossing. 3 Within UndershootRegion # 1:							
	oltage on the							
	ii Calculating Undershoot Amplitude using the equation:							
	Undershoot Amplitude = Vss - V _{MIN}							
	<i>b</i> Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:							

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + 2 \Big)$	$\left(\frac{y_n}{2}\right)$
---	------------------------------

Figure 53 Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JESD209-5C specification.

Overshoot_/	Area_CK_c
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Availability Condition: Table 110 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK_c

Test ID & References: Table 111 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
Maximum overshoot area above $V_{\text{DD2H}}/V_{\text{DDQ}}$	152006	Table 415

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

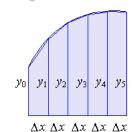
- **Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},\,V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

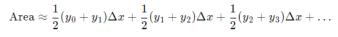
Overshoot Amplitude = $V_{MAX} - V_{DD2H}$

b Evaluate Area_below_V_{DD2H} using the equation:

Area_below_V_{DD2H} = (OvershootRegion_End - OvershootRegion_Start) x V_{DD2H}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:





We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$\mathrm{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_n}{2}\Big)$$

- Figure 54 Equation for Total_Area_Above_OV
 - *d* Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_OV - Area_below_V_{DD2H}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DD2H}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JESD209-5C specification.

Undershoot_Area_CK_c

Availability Condition: Table 112 Set Up tab options for availability of tests

Durat & Cantinuaus	N/A	Vec	Ne	Ne	
Burst & Continuous	N/A	Yes	No	No	CK_c
Test ID & References:	Table 113 LP	DDR5 Test References from J	IESD209-5C Specification		
	Symbol (in Spe	cification)	Test ID	Reference	from Specification
	Maximum under	rshoot area above VSS	152007	Table 415	
Overview:	from all regio	ons of the acquired wa	the undershoot amplitud aveform. In case of an unc ot width and undershoot a	dershoot, the	ne test signal that is found e undershoot area is
Procedure:	(vertical s) 2 Find the ' An "Unde	scale adjustment). 'UndershootRegion" a	d perform signal condition across the acquired wavef at the falling edge of Vss (orm.	mize screen resolution g and ends at the rising edg
		ndershootRegion # 1:			
		te Undershoot Amplit	2		
		sing I _{MIN} , V _{MIN} to obt ndershootRegion.	ain the time-stamp of the	e minimum v	oltage on the
	ii Ca	alculating Undershoot	t Amplitude using the equ	lation:	
		Ur	ndershoot Amplitude = Vs	ss - V _{MIN}	
	b Evalua	te Total_Area_Below_\	Vss by using Trapezoidal	Method Area	a Calculation:
		The Trane	zoidal Rule		

$\Delta x \Delta x \Delta x \Delta x \Delta x \Delta x$

yo y1 y2 y3 y4 y5

$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the $\ensuremath{\mathbf{Trapezoidal\ Rule}}$, for n trapezoids:

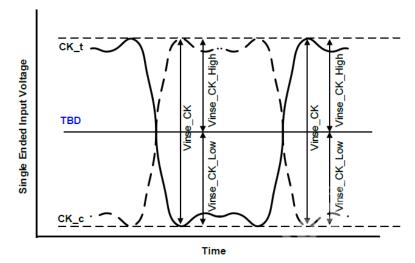
$$egin{array}{l} \operatorname{Area}pprox\Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big) \end{array}$$

Figure 55

Equation for Total_Area_Below_Vss

- *c* To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JESD209-5C specification.



The minimum input single-ended voltage is measured as shown in Figure 36.

Figure 56 Clock Single-ended Input Voltage definition

Vinse_CK_High (CK_c)

Availability Condition:	Table 114	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK_c

Test ID & References: Table 115 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_CK_High	151013	Table 418

Overview: The purpose of this test is to verify the peak voltage of high pulse.

Procedure:

1 Pre-condition the oscilloscope.

- 2 Trigger on the rising edge of the clock signal under test.
- 3 Find all valid positive pulses of the Clock in the entire waveform. A valid positive pulse on the Clock starts at the valid rising edge and ends at the following valid falling edge.
- 4~ Zoom into the first pulse and measure $V_{\text{MAX}}.$
- 5 Calculate the value of Vinse_CK_High (CK_c) using the equation:

Vinse_CK_High (CK_c) = $V_{MAX} - V_{REF}$



For this test, the Test App considers Vref to be VrefCA configuration value (set under Measurement Thresholds).

- 6 Continue the previous step with the rest of the positive pulses found in the specified waveform.
- 7 Determine the worst result from the set of Vinse_CK_High (CK_c) measured.

Expected/The measured value of Vinse_CK_High (CK_c) for the test signal shall be within the conformanceObservable Results:limits as per the JESD209-5C specification.

```
Vinse_CK_Low (CK_c)
```

Availability Condition: Table 116 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK_c

Test ID & References:

Table 117 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_CK_Low	151015	Table 418

Overview: Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the falling edge of the clock signal under test.

The purpose of this test is to verify the peak voltage of low pulse.

- 3 Find all valid negative pulses of the Clock in the entire waveform. A valid negative pulse on the Clock starts at the valid falling edge and ends at the following valid rising edge.
- 4 Zoom into the first pulse and measure V_{MIN} .
- 5 Calculate the value of Vinse_CK_Low (CK_c) using the equation:

Vinse_CK_Low (CK_c) = $V_{REF} - V_{MIN}$

NOTE

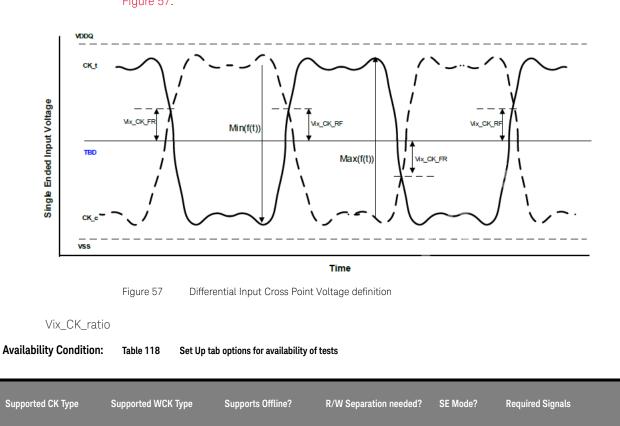
For this test, the Test App considers Vref to be VrefCA configuration value (set under Measurement Thresholds).

6 Continue the previous step with the rest of the negative pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_CK_Low (CK_c) measured.

Expected/ The measured value of Vinse_CK_Low (CK_c) for the test signal shall be within the conformance limits as per the JESD209-5C specification.

Clock (SE) CK t & CK c (Clock Plus & Minus) tests



No

The cross-point voltage of the differential input signals (CK_t, CK_c) is measured as shown in Figure 57.

Yes

Test ID & References: Table 119 LPDDR5 Test References from JESD209-5C Specification

N/A

Symbol (in Specification)	Test ID	Reference from Specification
Vix_CK_ratio	151016	Table 422

Overview:

Burst & Continuous

The purpose of this test is to verify the ratio of the calculated crossing point voltage from the value of the measured crossing point voltage on the input differential pair test signals.



For Clock (CK) signal, the Test App considers Vref to be the VrefCA configuration value (set under Measurement Thresholds).

No

CK_t, CK_c

Procedure:

- 1 Sample/Acquire data waveforms.
- 2 Use Subtract FUNC to generate the differential waveform from the 2-source input.
- 3 Find the Vmax and Vmin of the differential signal denoted as Max(f(t)) and Min(f(t)) respectively.

4 Find the time-stamp of all differential CK crossing that crosses 0V.
5 Use V _{Time} to get the actual crossing point voltage value using the time-stamp obtained in the previous step.
6 At each crosspoint (rising and falling) found, find the voltage differential between the crosspoint and V _{Ref} . The rising and falling crosspoint voltage differential is denoted as Vix_CK_RF and Vix_CK_FR respectively.
7 For each cross point voltage, calculate the final result using the equation (for Rising):
V _{IX} _CK_ratio = 100% x [Vix_CK_RF/Max(f(t))]
8 For each cross point voltage, calculate the final result using the equation (for Falling):
V _{IX} _CK_ratio = 100% x [Vix_CK_FR/Min(f(t))]
9 Determine the worst result from the set of V _{IX} _CK_ratio measured.
The calculated value of the crossing point voltage ratio for the differential test signal pair shall be within the conformance limits as per the JESD209-5C specification in the References section.

Vinse_CK

Availability Condition: Table 120 Set Up tab options for availability of tests

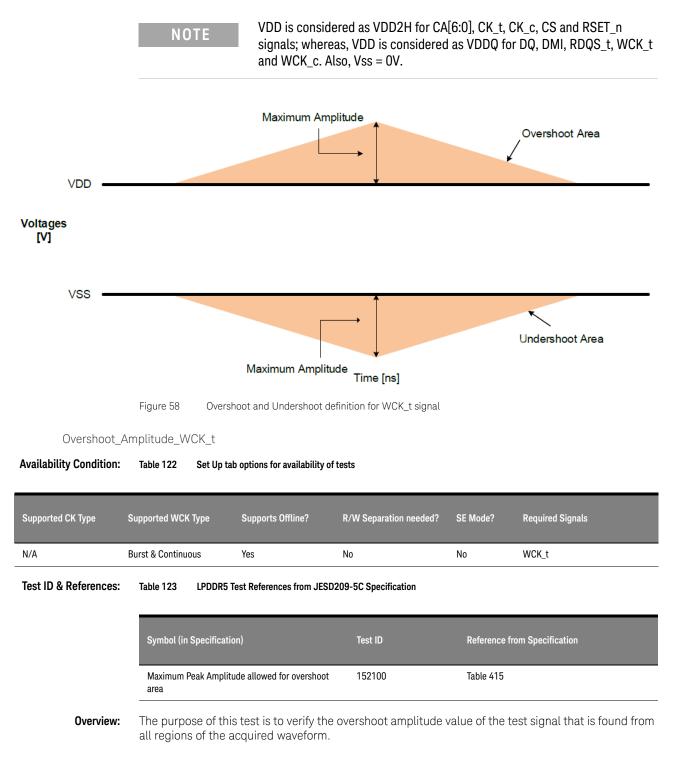
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK_t, CK_c

Test ID & References: Table 121 LPDDR5 Test References from JESD209-5C Specification

	Symbol (in Specification)	Test ID	Reference from Specification
	Vinse_CK	151017	Table 418
Overview:	The purpose of this test is to veri	fy the maximum voltag	e difference between the test signals.
Procedure:	 Find all valid positive and neg Zoom into the first pulse and CK_t and CK_c. Repeat previous step for all p Determine the worst result from 	measure Vmax, where ^v ulses.	Vmax is the point to point difference between pulses.
Expected/ Observable Results:	The measured value of the Vinse the JESD209-5C specification in		shall be within the conformance limits as per n.

Write Clock (SE) WCK_t (Write Clock Plus) tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 58.



When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

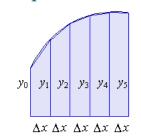
- **Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}}, V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DDQ}$

b Evaluate Area_below_V_{DDQ} using the equation:

Area_below_V_{DDQ} = (OvershootRegion_End - OvershootRegion_Start) x V_{DDQ}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



The Trapezoidal Rule

$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$\mathrm{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_n}{2}\Big)$$

Figure 59 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_OV - Area_below_V_{DDQ}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DDQ}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

the Overshoot Amplitude and Area measurement value shall be within the conformance limits as per sults:the JESD209-5C specification.

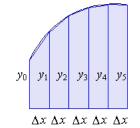
Expected/ Observable Results:

Undershoot_Amplitude_WCK_t

Availability Condition: Table 124 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	Burst & Continuous	Yes	No	No	WCK_t		
Test ID & References	Table 125 LPDDR	5 Test References from JE	SD209-5C Specification				
	Symbol (in Specifica	ation)	Test ID	Reference	from Specification		
	Maximum Peak Amp area	litude allowed for undersh	oot 152101	Table 415			
Test Overview:		The purpose of this test is to verify the undershoot amplitude value of the test signal that is foun- from all regions of the acquired waveform.					
	In case of an und Calculation.	dershoot, the under	shoot area is calculated	based on th	e Trapezoidal Method Area		
Test Procedure:		1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).					
 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (0V) crossing and of Vss (0V) crossing. 				g and ends at the rising edge			
	3 Within Unde	5					
	a Evaluate l	Jndershoot Amplitu	de by:				
		g T _{MIN} , V _{MIN} to obta rshootRegion.	in the time-stamp of the	e minimum v	oltage on the		
	ii Calcu	llating Undershoot ,	Amplitude using the equ	uation:			
		Und	dershoot Amplitude = V	ss - V _{MIN}			
	b Evaluate T	otal_Area_Below_V	ss by using Trapezoidal	Method Area	a Calculation:		

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg[\operatorname{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_0}{2}\Big)$	$\left(\frac{n}{2}\right)$
---	----------------------------

Figure 60 Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/ The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JESD209-5C specification.

Overshoot	Area	W	Cł	<	t
-----------	------	---	----	---	---

Availability Condition: Table 126 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	No	WCK_t
Test ID & References:	Table 127 LPDDR5	Test References from JES	D209-5C Specification		

Symbol (in Specification)	Test ID	Reference from Specification
Maximum overshoot area above V_{DD2H}/V_{DDQ}	152102	Table 415

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

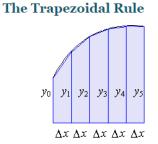
- **Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},\,V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DDQ}$

b Evaluate Area_below_V_{DDQ} using the equation:

Area_below_V_{DDQ} = (OvershootRegion_End - OvershootRegion_Start) x V_{DDQ}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



$$\operatorname{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the **Trapezoidal Rule**, for *n* trapezoids:

$$egin{array}{l} \operatorname{Area}pprox\Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big) \end{array}$$

Figure 61 Equation for Total_Area_Above_OV

d Calculate Area_Above_ V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_OV - Area_below_V_{DDQ}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DDQ}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JESD209-5C specification.

Undershoot_Area_WCK_t

Availability Condition: Table 128 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	Burst & Continuous	Yes	No	No	WCK_t		
Test ID & References:	Table 129 LPDDR5 Te	est References from JE	SD209-5C Specification				
	Symbol (in Specification	n)	Test ID	Reference f	rom Specification		
	Maximum undershoot a	rea above VSS	152103	Table 415			
Overview:	from all regions of	the acquired way	the undershoot amplitud /eform. In case of an und t width and undershoot a	lershoot, the	e test signal that is found undershoot area is		
Procedure:			perform signal condition	ning to maxii	mize screen resolution		
	2 Find the "Unde	An "UndershootRegion" starts at the falling edge of Vss (0V) crossing and ends at the rising edge					
	3 Within Undersh						
	a Evaluate Uno	•	2				
		_{MIN} , V _{MIN} to obta 100tRegion.	in the time-stamp of the	e minimum v	oltage on the		
	ii Calculat	ing Undershoot	Amplitude using the equ	ation:			
		Un	dershoot Amplitude = Vs	s - V _{MIN}			
	b Evaluate Tota	al_Area_Below_V	ss by using Trapezoidal 1	Method Area	Calculation:		
		The Trapez	zoidal Rule				

Δx Δx Δx Δx Δx

yo y1 y2 y3 y4 y5

$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the $\ensuremath{\mathbf{Trapezoidal\ Rule}}$, for n trapezoids:

$$\mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big) igg|$$

Figure 62

Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Set Up tab options for availability of tests

Expected/ The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JESD209-5C specification.

Vinse_WCK_High (WCK_t)

Table 130

Availability Condition:

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	Burst & Continuous	Yes	No	No	WCK_t		
Test ID & References:	Table 131 LPDDR	5 Test References from JE	SD209-5C Specification				
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification		
	Vinse_WCK_High		151112	Table 424			
Overview:	The purpose of the	nis test is to verify t	he peak voltage of high	pulse.			
Procedure:	 Pre-condition the oscilloscope. Trigger on the rising edge of the write clock signal under test. Find all valid positive pulses of the Write Clock in the entire waveform. A valid positive pulse on the Write Clock starts at the valid rising edge and ends at t valid falling edge. Zoom into the first pulse and measure V_{MAX}. Calculate the value of Vinse_WCK_High (WCK_t) using the equation: 						
	Vinse_WCK_High (WCK_t) = $V_{MAX} - V_{REF}$						
	NOTE		ock (WCK) signal, the To n value (set under Meas		siders Vref to be the VrefD resholds).		
			the rest of the positive p the set of Vinse_WCK_H		l in the specified waveform t) measured.		
Expected/ Observable Results:	The measured va		High (WCK_t) for the te	0	ll be within the conforman		

Vinse_WCK_Low (WCK_t)

Availability Condition: Table 132 Set Up tab options for availability of tests

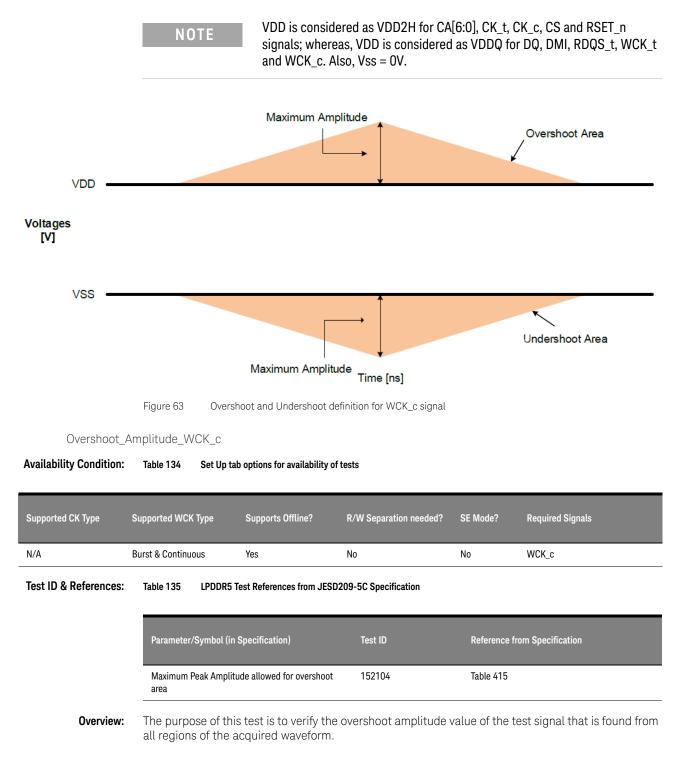
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals				
N/A	Burst & Continuous	Yes	No	No	WCK_t				
Test ID & References	Table 133 LPDDR	85 Test References from JE	SD209-5C Specification						
	Symbol (in Specific	ation)	Test ID	Reference	from Specification				
	Vinse_WCK_Low		151114	Table 424					
Overview	The purpose of t	this test is to verify t	he peak voltage of low p	oulse.					
Procedure	: 1 Pre-conditio	1 Pre-condition the oscilloscope.							
	2 Trigger on th	2 Trigger on the falling edge of the write clock signal under test.							
	A valid nega	3 Find all valid negative pulses of the Write Clock in the entire waveform. A valid negative pulse on the Write Clock starts at the valid falling edge and ends at the following valid rising edge.							
	0	ne first pulse and me	easure V _{MIN} .						
	5 Calculate the value of Vinse_WCK_Low (WCK_t) using the equation:								
	Vinse_WCK_Low (WCK_t) = $V_{REF} - V_{MIN}$								
	NOTE	NOTE For Write Clock (WCK) signal, the Test App considers Vref to be the VrefDQ configuration value (set under Measurement Thresholds).							
	6 Continue the	e previous step with	the rest of the negative	pulses foun	d in the specified waveform				
	7 Determine th	he worst result from	the set of Vinse_WCK_l	_ow (WCK_t) measured.				

Expected/ Observable Results:

The measured value of Vinse_WCK_Low (WCK_t) for the test signal shall be within the conformance limits as per the JESD209-5C specification.

Write Clock (SE) WCK_c (Write Clock Minus) tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 63.



When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

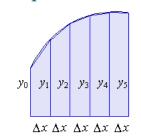
- **Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}}, V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DDQ}$

b Evaluate Area_below_V_{DDQ} using the equation:

Area_below_V_{DDQ} = (OvershootRegion_End - OvershootRegion_Start) x V_{DDQ}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



The Trapezoidal Rule

$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$\mathrm{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_n}{2}\Big)$$

Figure 64 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_OV - Area_below_V_{DDQ}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DDQ}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

ted/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per ults: the JESD209-5C specification.

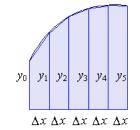
Expected/ Observable Results:

Undershoot_Amplitude_WCK_c

Availability Condition: Table 136 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
N/A	Burst & Continuous	Yes	No	No	WCK_c			
Test ID & References:	Table 137 LPDDR5	Test References from J	ESD209-5C Specification					
	Symbol (in Specificat	Symbol (in Specification) Test ID Reference from Specification						
	Maximum Peak Ampli area	itude allowed for unders	noot 152105	Table 415				
Overview:		The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.						
	In case of an und Calculation.	ershoot, the unde	rshoot area is calculate	d based on th	ne Trapezoidal Method Area			
Procedure:	1 Sample/acqu (vertical scale		l perform signal conditi	oning to max	imize screen resolution			
	2 Find the "Unc	dershootRegion" a ootRegion" starts a	cross the acquired wave t the falling edge of Vs		g and ends at the rising edge			
		shootRegion # 1:						
	a Evaluate U	ndershoot Amplitu	ide by:					
		T _{MIN} , V _{MIN} to obta shootRegion.	ain the time-stamp of t	ne minimum v	oltage on the			
	ii Calcu	lating Undershoot	Amplitude using the ed	quation:				
		Ur	dershoot Amplitude = `	/ss - V _{MIN}				
	b Evaluate To	otal_Area_Below_\	/ss by using Trapezoida	l Method Area	a Calculation:			

The Trapezoidal Rule



$$\operatorname{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg { m Area}pprox \Delta x \Big({y_0\over 2} + y_1 + y_2 + y_3 + \ldots +$	$\left(\frac{y_n}{2} \right)$
--	--------------------------------

Figure 65 Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JESD209-5C specification.

Overshoot Area WCK

Availability Condition: Table 138 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	No	WCK_c
Test ID & References:	Table 139 LPDDR5	Test References from JE	SD209-5C Specification		
	Symbol (in Specificat	tion)	Test ID	Reference	from Specification

Maximum overshoot area above V _{DD2H} /V _{DDQ} 152	Table 4	15

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

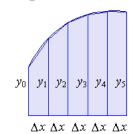
When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

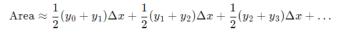
- **Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}}, V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

b Evaluate Area_below_V_{DDQ} using the equation:

Area_below_V_{DDQ} = (OvershootRegion_End - OvershootRegion_Start) x V_{DDQ}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:





We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$\mathrm{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_n}{2}\Big)$$

- Figure 66 Equation for Total_Area_Above_OV
 - *d* Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_0V - Area_below_V_{DDQ}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DDQ}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JESD209-5C specification.

Undershoot_Area_WCK_c

Availability Condition: Table 140 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type Support	s Offline? R/W Separation neede	ed? SE Mode? Required Signals				
N/A	Burst & Continuous Yes	No	No WCK_c				
Test ID & References:	Table 141 LPDDR5 Test Refere	nces from JESD209-5C Specification					
	Symbol (in Specification)	Test ID	Reference from Specification				
	Maximum undershoot area above	VSS 152107	Table 415				
Overview:	from all regions of the acq		litude value of the test signal that is found undershoot, the undershoot area is oot amplitude.				
Procedure:	1 Sample/acquire signal (vertical scale adjustm		ditioning to maximize screen resolution				
	2 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.						
	3 Within UndershootReg						
	a Evaluate Undershoo						
	i Using T _{MIN} , V _M UndershootReg	_{IIN} to obtain the time-stamp of gion.	f the minimum voltage on the				
	ii Calculating Un	dershoot Amplitude using the	equation:				
	Undershoot Amplitude = Vss - V _{MIN}						
	b Evaluate Total_Area	_Below_Vss by using Trapezoi	dal Method Area Calculation:				
	The	e Trapezoidal Rule					
		y ₀ y ₁ y ₂ y ₃ y ₄ y ₅					

$$\Delta x \Delta x \Delta x \Delta x \Delta x$$

 $\operatorname{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$

We can simplify this to give us the $\ensuremath{\mathbf{Trapezoidal\ Rule}}$, for n trapezoids:

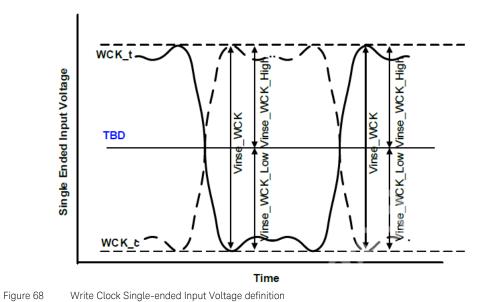
$$\mathrm{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_n}{2}\Big)$$

Figure 67

Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JESD209-5C specification.



The minimum input single-ended voltage is measured as shown in Figure 68.

0

Vinse_WCK_High (WCK_c)

Availability Condition: Table 142 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
N/A	Burst & Continuous	Yes	No	No	WCK_c	
Test ID & References:	Table 143 LPDDR	5 Test References from JE	SD209-5C Specification			
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification	
	Vinse_WCK_High		151113	Table 424		
Overview:	The purpose of t	his test is to verify t	he peak voltage of high	pulse.		
Procedure:	1 Pre-condition	n the oscilloscope.				
	2 Trigger on th	e rising edge of the	write clock signal unde	r test.		
	A valid positi	3 Find all valid positive pulses of the write clock in the entire waveform. A valid positive pulse on the Write Clock starts at the valid rising edge and ends at the following valid falling edge.				
	4 Zoom into th	e first pulse and me	easure V _{MAX} .			
	5 Calculate the	e value of Vinse_WC	K_High (WCK_c) using	the equatior	1:	

Vinse_WCK_High (WCK_c) = $V_{MAX} - V_{REF}$

NOTE

For Write Clock (WCK) signal, the Test App considers Vref to be the VrefDQ configuration value (set under Measurement Thresholds).

6 Continue the previous step with the rest of the positive pulses found in the specified waveform.

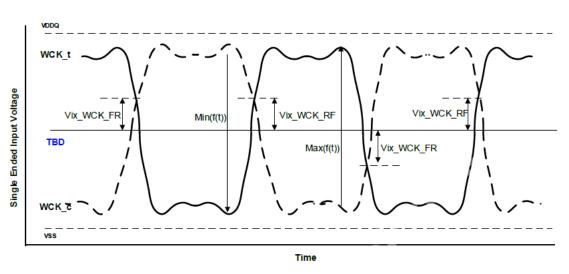
7 Determine the worst result from the set of Vinse_WCK_High (WCK_c) measured.

Expected/ The measured value of Vinse_WCK_High (WCK_c) for the test signal shall be within the conformance limits as per the JESD209-5C specification.

Vinse_WCK_Low (WCK_c)

Availability Condition:	Table 144 Set Up ta	b options for availability	of tests		
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	No	WCK_c
Test ID & References:	Table 145 LPDDR5	Test References from JE	SD209-5C Specification		
	Symbol (in Specificati	on)	Test ID	Reference	from Specification
	Vinse_WCK_Low		151115	Table 424	
Overview:	The purpose of th	is test is to verify t	he peak voltage of low p	oulse.	
Procedure:	 Pre-condition the oscilloscope. Trigger on the falling edge of the write clock signal under test. Find all valid negative pulses of the Write Clock in the entire waveform. A valid negative pulse on the Write Clock starts at the valid falling edge and ends at the valid rising edge. Zoom into the first pulse and measure V_{MIN}. Calculate the value of Vinse_WCK_Low (WCK_c) using the equation: Vinse_WCK_Low (WCK_c) = V_{REF} - V_{MIN} 				ge and ends at the following
	NOTE 6 Continue the	configuration	n value (set under Meas	surement Th	siders Vref to be the VrefDQ resholds). d in the specified waveform.
Expected/ Observable Results:	The measured val) measured. Il be within the conformance

Write Clock (SE) WCK_t & WCK_c (Write Clock Plus & Minus) tests



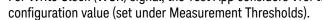
The cross-point voltage of the differential input signals (WCK_t, WCK_c) is measured as shown in Figure 69.



```
Vix_WCK_ratio
```

Availability Condition:	Table 146	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
N/A	Burst & Continuous	Yes	Yes	No	WCK_t, WCK_c	
Test ID & References	: Table 147 LPDDF	25 Test References from JE	SD209-5C Specification			
	Symbol (in Specific	ation)	Test ID	Reference	from Specification	
	Vix_WCK_ratio		151116	Table 428		
Overview		The purpose of this test is to verify the ratio of the calculated crossing point voltage from the val the measured crossing point voltage on the input differential pair test signals.				
	NOTE		ock (WCK) signal, the Te		siders Vref to be the VrefDQ	



Procedure: 1 S

- 1 Sample/Acquire data waveforms.
- 2 Use Subtract FUNC to generate the differential waveform from the 2-source input.
- 3 Find the Vmax and VMin of the differential signal denoted as Max(f(t)) and Min(f(t)) respectively.

	4 Find the time-stamp of all differential WCK crossing that crosses 0V.
	5 Use V _{Time} to get the actual crossing point voltage value using the time-stamp obtained in the previous step.
	6 At each crosspoint (rising and falling) found, find the voltage differential between the crosspoint and V _{Ref} . The rising and falling crosspoint voltage differential is denoted as Vix_WCK_RF and Vix_WCK_FR respectively.
	7 For each cross point voltage, calculate the final result using the equation (for Rising):
	V _{IX} _WCK_ratio = 100% x [Vix_WCK_RF/Max(f(t))]
	8 For each cross point voltage, calculate the final result using the equation (for Falling):
	V _{IX} _WCK_ratio = 100% x [Vix_WCK_FR/Min(f(t))]
	9 Determine the worst result from the set of V_{IX} -WCK_ratio measured.
Expected/ Observable Results:	The calculated value of the crossing point voltage ratio for the differential test signal pair shall be within the conformance limits as per the JESD209-5C specification in the References section.

Vinse_WCK

Availability Condition: Table 148 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	No	WCK_t, WCK_c

Test ID & References: Table 149 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_WCK	151117	Table 424

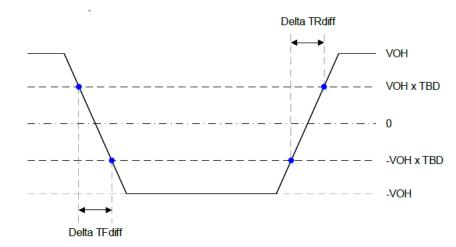
Overview: The purpose of this test is to verify the maximum voltage difference between the test signals.

Procedure: 1 Find all valid positive and negative pulses for WCK_t.

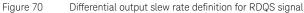
- 2 Zoom into the first pulse and measure Vmax, where Vmax is the point to point difference between WCK_t and WCK_c.
- 3 Repeat previous step for all pulses.
- 4 Determine the worst result from the set of Vinse WCK pulses.

Expected/The measured value of the Vinse_WCK shall be within the conformance limits as per theObservable Results:JESD209-5C specification in the References section.

Read Data Strobe (Diff) tests



Output slew rate for differential signals are measured as shown in Figure 70.s



SRQdiffR_RDQS

Availability Condition: Table 150 Set U	p tab options for availability of tests
---	---

N/A Yes Yes No DQ, RDQS(Diff)	Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
	N/A	N/A	Yes	Yes	No	DQ, RDQS(Diff)

Test ID & References: Table 151 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
SRQdiff	150002	Table 430

Overview: The purpose of this test is to verify the differential output slew rate for rising edge of the test signal within the read burst.

Procedure: 1 Acquire and split the read and write burst of the acquired signal.

- 2 Take the first valid READ burst found.
- 3 Find all the valid Strobe rising edges in the specified burst. A valid Strobe rising edge starts at V_{OL} crossing and ends at the following V_{OH} crossing.
- $\begin{array}{ll} \mbox{4} & \mbox{For all the valid Strobe rising edges, find the transition time, T_R.} \\ & \mbox{T_R}$ is the time starting at V_{OL} crossing and ending at the following V_{OH} crossing.} \end{array}$
- 5 Calculate SRQdiffR using the equation:

SRQdiffR =
$$[V_{OH} - V_{OI}] / T_R$$

6 Determine the worst result from the set of SRQdiffR measured.

Expected/ The measured value of SRQdiffR for the test signal shall be within the conformance limits as per the JESD209-5C specification.

SRQdiffF_RDQS

Availability Condition: Table 152 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	No	DQ, RDQS(Diff)

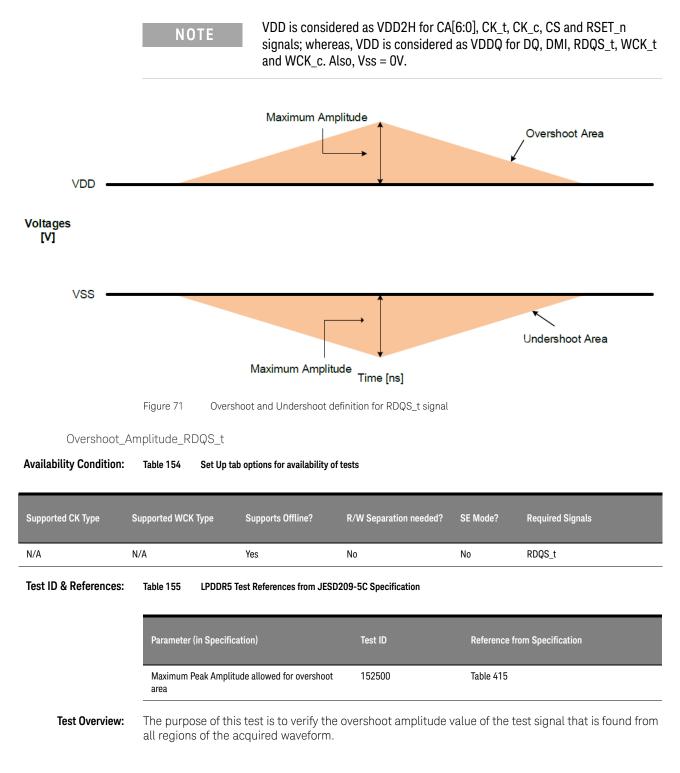
Test ID & References: Table 153 LPDDR5 Test References from JESD209-5C Specification

	9	ymbol (in Specification)	Test ID	Reference from Specification				
	S	RQdiff	150003	Table 430				
Overview:	The purpose of this test is to verify the differential output slew rate for falling edge of the test sign within the read burst.							
Procedure:	1	Acquire and split the read and write burst of the acquired signal.						
	2	Take the first valid READ burst found.						
	3	Find all the valid Strobe falling edges in the specified burst. A valid Strobe falling edge starts at V_{OH} crossing and ends at the following V_{OL} crossing.						
	4	For all the valid Strobe falling edges, find the transition time, T_F . T_F is the time starting at V_{OH} crossing and ending at the following V_{OI} crossing.						
	5	Calculate SRQdiffF using the						
			SRQdiffF = [V _{OH} - V	_{ol}] / T _F				
	6	Determine the worst result fro	om the set of SRQdiffF r	neasured.				

Expected/ The measured value of SRQdiffF for the test signal shall be within the conformance limits as per the JESD209-5C specification.

Read Data Strobe (SE) RDQS_t (Read Data Strobe Plus) tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 71.



When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

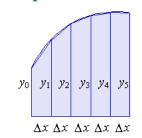
- **Test Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},\,V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DDQ}$

b Evaluate Area_below_V_{DDQ} using the equation:

Area_below_V_{DDQ} = (OvershootRegion_End - OvershootRegion_Start) x V_{DDQ}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



The Trapezoidal Rule

$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$\mathrm{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_n}{2}\Big)$$

Figure 72 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_OV - Area_below_V_{DDQ}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DDQ}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

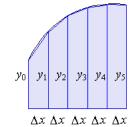
Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JESD209-5C specification.

Undershoot_Amplitude_RDQS_t

Availability Condition: Table 156 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
N/A	N/A	Yes	No	No	RDQS_t	
Test ID & References	Table 157 LPDDR	5 Test References from JE	SD209-5C Specification			
	Parameter (in Specif	ication)	Test ID	Reference	from Specification	
	Maximum Peak Amp area	itude allowed for undersh	oot 152501	Table 415		
Test Overview:	The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.					
	In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Me Calculation.					
Test Procedure	1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).					
	 2 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (OV) crossing and ends at the rising edg of Vss (OV) crossing. 3 Within UndershootRegion # 1: 					
	a Evaluate Undershoot Amplitude by:					
	 Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion. 					
	ii Calcu	lating Undershoot .	Amplitude using the equ	uation:		
		Un	dershoot Amplitude = V	ss – V _{MIN}		
	<i>b</i> Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:					

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_0}{2} \Big)$	$\left(\frac{n}{2}\right)$
--	----------------------------

Figure 73 Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/ The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JESD209-5C specification.

Overshoot_Area_RDQS_t

Availability Condition: Table 158 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
N/A	N/A	Yes	No	No	RDQS_t	
Test ID & References: Table 159 LPDDR5 Test References from JESD209-5C Specification						

Symbol (in Specification)	Test ID	Reference from Specification
Maximum overshoot area above V_{DD2H}/V_{DDQ}	152502	Table 415

Test Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

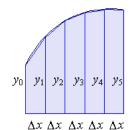
- **Test Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},\,V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DDQ}$

b Evaluate Area_below_V_{DDQ} using the equation:

Area_below_V_{DDQ} = (OvershootRegion_End - OvershootRegion_Start) x V_{DDQ}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



Area
$$\approx rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$\mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

- Figure 74 Equation for Total_Area_Above_OV
 - *d* Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_OV - Area_below_V_{DDQ}

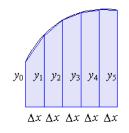
- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DDQ}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JESD209-5C specification.

Undershoot_Area_RDQS_t

Availability Condition: Table 160 Set Up tab options for availability of tests

Supported CK Type	Suppo	rted WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	N/A		Yes	No	No	RDQS_t		
Test ID & References:	Tab	Table 161 LPDDR5 Test References from JESD209-5C Specification						
	S	ymbol (in Specifica	tion)	Test ID	Reference	Reference from Specification		
	M	aximum undershoo	ot area above VSS	152503	Table 415			
Test Overview:	The purpose of this test is to verify the undershoot amplitude value of the test signal that is four from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.							
Test Procedure:	1	1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).						
	2	2 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.						
	3 Within UndershootRegion # 1:							
		a Evaluate Undershoot Amplitude by:						
	i Using T _{MIN} , V _{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.					voltage on the		
	ii Calculating Undershoot Amplitude using the equation:							
		Undershoot Amplitude = Vss - V _{MIN}						
		<i>b</i> Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:						
			The Trapez	oidal Rule				



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the **Trapezoidal Rule**, for n trapezoids:

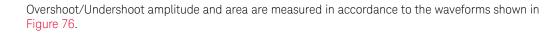
$$egin{aligned} \operatorname{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big) \end{aligned}$$

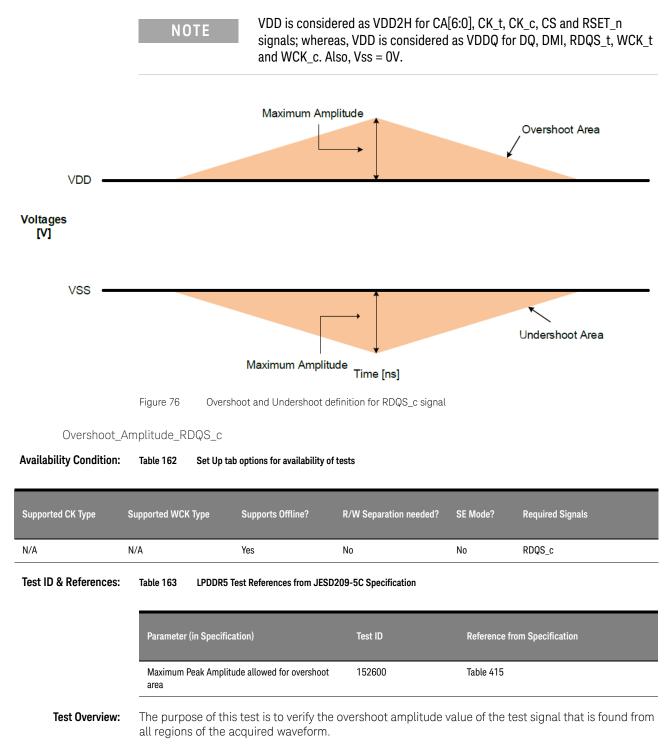
Figure 75 Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JESD209-5C specification.

Read Data Strobe (SE) RDQS_c (Read Data Strobe Minus) tests





When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

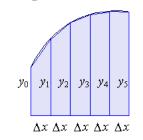
- **Test Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DDQ} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}}, V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude =
$$V_{MAX} - V_{DD}$$

b Evaluate Area_below_V_{DD} using the equation:

Area_below_V_{DD} = (OvershootRegion_End - OvershootRegion_Start) x V_{DD}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



The Trapezoidal Rule

Area
$$\approx \frac{1}{2}(y_0 + y_1)\Delta x + \frac{1}{2}(y_1 + y_2)\Delta x + \frac{1}{2}(y_2 + y_3)\Delta x + \dots$$

We can simplify this to give us the **Trapezoidal Rule**, for n trapezoids:

$$ext{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 77 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DD} using the equation:

Area_Above_V_{DD} = Total_Area_Above_OV - Area_below_V_{DD}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DD}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

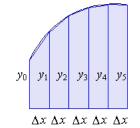
Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JESD209-5C specification.

Undershoot_Amplitude_RDQS_c

Availability Condition: Table 164 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	N/A	Yes	No	No	RDQS_c		
Test ID & References	: Table 165 LPDDR	5 Test References from JE	SD209-5C Specification				
	Parameter (in Speci	fication)	Test ID	Reference	from Specification		
	Maximum Peak Amp area	litude allowed for undersho	pot 152601	Table 415			
Test Overview	The purpose of this test is to verify the undershoot amplitude value of the test signal that is fo from all regions of the acquired waveform.						
	In case of an und Calculation.	dershoot, the under	shoot area is calculated	based on th	ne Trapezoidal Method Area		
Test Procedure		1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).					
	An "Undersh						
	3 Within Unde						
	a Evaluate l	Indershoot Amplitu	de by:				
		i Using T _{MIN} , V _{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.					
	ii Calcu	ii Calculating Undershoot Amplitude using the equation:					
		Undershoot Amplitude = Vss - V _{MIN}					
	b Evaluate T	otal_Area_Below_V	ss by using Trapezoidal	Method Area	a Calculation:		

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + 2 \Big)$	$\left(\frac{y_n}{2}\right)$
---	------------------------------

Figure 78 Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/ The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JESD209-5C specification.

Overshoot_Area_RDQS_c

Availability Condition: Table 166 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	No	RDQS_c

Test ID & References: Table 167 LPDDR5 Test References from JESD209-5C Specification

Parameter (in Specification)	Test ID	Reference from Specification
Maximum overshoot area above $V_{\text{DD2H}}/V_{\text{DDQ}}$	152602	Table 415

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

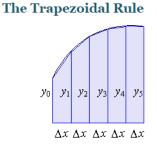
- **Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DD} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}}, V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude =
$$V_{MAX} - V_{DD}$$

b Evaluate Area_below_V_{DD} using the equation:

Area_below_V_{DD} = (OvershootRegion_End - OvershootRegion_Start) x V_{DD}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$egin{aligned} \operatorname{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big) \end{bmatrix}$$

Figure 79 Equation for Total_Area_Above_OV

d Calculate Area_Above_ V_{DD} using the equation:

Area_Above_V_{DD} = Total_Area_Above_OV - Area_below_V_{DD}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DD}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JESD209-5C specification.

Undershoot_Area_RDQS_c

Availability Condition: Table 168 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
N/A	N/A	Yes	No	No	RDQS_c	
Test ID & References:	Table 169 LPDDR	5 Test References from JE	SD209-5C Specification			
	Parameter (in Speci	fication)	Test ID	Reference	from Specification	
	Maximum undersho	ot area above VSS	152603	Table 415		
Overview:	from all regions	of the acquired wav	he undershoot amplitud eform. In case of an unc width and undershoot a	lershoot, the	ne test signal that is found e undershoot area is	
Procedure:		1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).				
	2 Find the "Un An "Undersh	 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing. 				
	3 Within Unde	rshootRegion # 1:				
		Jndershoot Amplitu	5			
	i Using Unde	g T _{MIN} , V _{MIN} to obta ershootRegion.	in the time-stamp of the	e minimum v	oltage on the	
	ii Calcu	ulating Undershoot ,	Amplitude using the equ	lation:		
		Und	dershoot Amplitude = Vs	s - V _{MIN}		
	b Evaluate 7	Fotal_Area_Below_V	ss by using Trapezoidal	Method Area	a Calculation:	
		The Trapez	oidal Rule			
		<i>y</i> 0 <i>y</i> 1	y ₂ y ₃ y ₄ y ₅			

$$\Delta x \Delta x \Delta x \Delta x \Delta x \Delta x$$

 $\operatorname{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$

We can simplify this to give us the $\ensuremath{\mathbf{Trapezoidal\ Rule}}$, for n trapezoids:

$$\mathrm{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_n}{2}\Big)$$

Figure 80

Equation for Total_Area_Above_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JESD209-5C specification.

Read Data Strobe (SE) RDQS_t & RDQS_C (Read Data Strobe Plus & Minus) tests

tRPRE (Read Data Strobe Plus & Minus)

Availability Condition: Table 170 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	N/A	Yes	No	No	RDQS_t (SE), RDQS_c (SE)		
Test ID & References:	Table 171 LPDDR5	Test References from JE	SD209-5C Specification				
	Symbol (in Specificat	tion)	Test ID	Reference	from Specification		
	tRPRE		152700	Table 222			
Test Overview:		The purpose of this test is to verify the time when RDQS_c start driving high (*preamble behavior) to RDQS edge that associate with the first DQ signal crossing for the read cycle.					
Test Procedure:					ined RDQS preamble length, ke this edge as tRPRE_end.		
	Note that cro	ssing must be betw	veen RDQS Plus rising a	nd RDQS Mi	inus falling.		
	toggling prea	2 If RDQS Preamble = "Static:0tWCK, Toggle: 4tWCK", then find the first crossing (before the toggling preamble). Take this edge as tRPRE_start. *Note:crossing must be between RDQS Plus rising and RDQS Minus falling.					
		mble is other optio e as tRPRE_start fo		lated Low-Z	point at RDQS Minus signal.		
	4 Measure the t	time difference bet	ween these two edges (†	tRPRE_start	and tRPRE_end).		
	5 Report the m	easurement as tRP	RE.				
Expected/ Observable Results:	The measured va	lue of tRPRE for th	e test signal is considere	ed for 'Inforr	nation-Only' purpose.		

Keysight D9050LDDC LPDDR5 Test Application Methods of Implementation

5 Timing Tests

RDQS Detect Method for Read Write Separation 154 Data Tests 156 Clock (Diff) Tests 160 Clock (SE Mode) Tests 167 Write Clock (Diff) tests 170 Write Clock (SE Mode) Tests 180 RDQS (Diff) Tests 183 Other timing tests 189



RDQS Detect Method for Read Write Separation

RDQS Detect is a read write separation method. This method works when the signal source contains at least an RDQS signal and a WCK signal. In this method, the Read/Write burst data is identified based on the presence of RDQS burst. If WCK burst contains an RDQS burst, then it is a Read burst. If the WCK burst does not contain an RDQS burst, then it is a Write burst.

If you select the RDQS Detect mode as the burst identification method, you must select the length of the WCK Postamble in the WCK Postamble Length section of the LPDDR5 General Setup dialog box.

LPDDR5 General	Setup			?		
			1			
JEDEC standard				om the		
3200	🗸 мт,	's JEDEC standard values				
		WCK Frequency : 160	0 MHz			
WCK : CK Ratio 2:1 Clock Frequency : 800 MHz						
Signal Source						
affect the availal all the signal sou						
WCK_t (SE),	WCK_c	(SE), RDQS_t (SE), RDQS_c (SE)	$\mathbf{\nabla}$			
	ndad M					
Single-Er	naea M	ode				
Signal Operatio	on Mod	e				
CK (Diff) Co	ntinuou	is 💙				
WCK (Diff) Bu	rst	Burst W	CK opti	ons		
RDQS Preambl	le/Posta	amble Length				
RDQS Preamble		Static: 4 tWCK, Toggle: 0 tWCK				
RDQS Postamble		0.5 tWCK				
RDQS Postamble	e Mode	Toggle	V			
WCK Postamble Length						
	Identify the length of WCK Postamble.					
WCK Postamble		2.5 tWCK				
		2.5 tWCK				
🖌 Show Hints	5	4.5 tWCK		OK Cancel		
		6.5 tWCK				

Figure 81 LPDDR5 General Setup Dialog



Figure 82 WCK Burst Options Setup Dialog

Tests that support the RDQS Detect Burst Identification Method

The following Timing tests support the RDQS Burst Identification method:

WRITE Tests

- tWCK2CK
- tWCKHL
- tWCKH
- tWCKL
- tDIPW1
- tDIPW2
- tDIHL

READ Tests

- tRPRE
- tRPST
- tDQSQ
- tQSH
- tQSL
- tjitRDQS_1UI(avg)
- tjitRDQS_1UI(abs)
- tjitRDQS_2UI(abs)
- tjitRDQS_3UI(abs)
- tjitRDQS_4UI(abs)
- tjitRDQS_1UI
- tjitRDQS_3UI

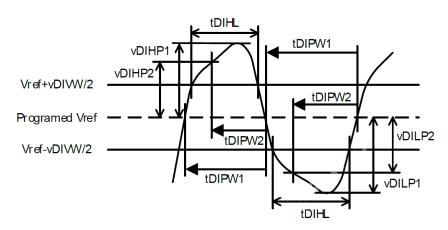
Method of Implementation for the RDQS Detect Burst Identification Method

The following are the steps for the method of implementation for the RDQS Detect burst identification method:

- 1 Populate the burst from WCK signal.
- 2 Locate FirstWCKRising for the burst.
- 3 Compute TimeA = FirstWCKRising + tWCKPRE_Toggle_RD * ClockCycleWidth.
- 4 Compute TimeB = Start of WCK postamble. For example, if tWCKPST=2.5nWCK then TimeB = time of second last rising edge of WCK burst. If tWCKPST=4.5nWCK then TimeB = time of fourth last rising edge of WCK burst.
- 5 Compute TimeC = 0.5*(TimeA+TimeB)
- 6 Compute VmaxTimeCWithinUI = Vmax range from (TimeC 1*UI) to (TimeC + 1*UI)
- 7 Compute VminTimeCWithinUI = Vmin range from (TimeC 1*UI) to (TimeC + 1*UI)
- 8 If [(VmaxTimeCWithinUI > VOHDiff_RDQS) AND (VminTimeCWithinUI < VOLDiff_RDQS)] then the burst will be recognized as a READ burst. Otherwise, the burst will be recognized as a WRITE burst.
- 9 Repeat steps 2 to 8 for the rest of burst.

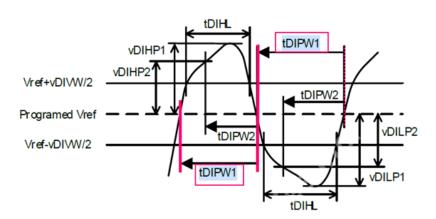
Data Tests

The DQ Rx pulse width and amplitude are measured in accordance to the waveforms shown in Figure 83.





tDIPW1





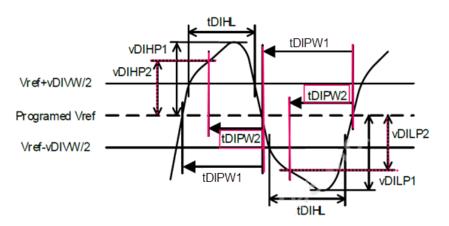
Availability Condition: Table 172 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	Yes	Yes	WCK (Diff), DQ

Test ID & References: Table 173 LPDDR5 Test References from JESD209-5C Specification

	Symbol (in Specification)	Test ID	Reference from Specification			
	tDIPW1	160000	Table 468			
Overview:	The purpose of this test is to ver all region of the acquired wavef		VrefDQ of the test signal that is found from			
Procedure:	 For all rising DQ crossing, fir then calculate the time diffe For all falling DQ crossing, fi then calculate the time diffe 	 then calculate the time different as tDIPW1 result. For all falling DQ crossing, find the next rising DQ crossing. If the pulse is a single pulse (<1.5UI), then calculate the time different as tDIPW1 result. 				
Expected/ Observable Results:	The measured value of tDIPW1 specification.	shall be within the confo	prmance limits as per the JESD209-5C			

tDIPW2





Availability Condition: Table 174 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	Yes	Yes	WCK (Diff), DQ

Test ID & References:	Table 175 LPDDR5 Test References	s from JESD209-5C Specification	
	Symbol (in Specification)	Test ID	Reference from Specification
	tDIPW2	160001	Table 468
Overview:	The purpose of this test is to region of the acquired wavefo		of the test signal that is found from all
Procedure:	6	Illing DQ crossings at VREFDQ g at [Vref+vDIHP2(Compliance of vDIHP2 is 55mV.	
	3 Find all falling DQ crossin Note: Compliance value c	g at [Vref+vDILP2(Compliance of vDILP2 is -55mV.	e)].
			xt falling DQ crossing at VREFDQ level. If culate the time different as tDIPW2 result.
			xt rising DQ crossing at VREFDQ level. If culate the time different as tDIPW2 result.
	6 Determine the worst resu	lt from the set of tDIPW2 mea	sured.
Expected/ Observable Results:	The measured value of tDIPW specification.	/2 shall be within the conform	ance limits as per the JESD209-5C

tDIHL

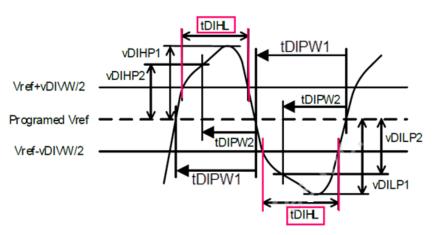


Figure 86 DQ Rx pulse width @ Vref DQ +/- vDIVW/2 of the test signal

Availability Condition: Set Up tab options for availability of tests Table 176

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	Yes	Yes	WCK (Diff), DQ

	Symbol (in Specification)	Test ID	Reference from Specification				
	tDIHL	160002	Table 468				
Overview:	The purpose of this test is to verify DQ Rx pulse width @ Vref DQ +/- vDIVW/2 of the test signal that is found from all region of the acquired waveform.						
Procedure:	 Find all valid rising and falling DQ crossings at [Vref+vDIVW/2] level in the specified burst. For all rising DQ crossing at [Vref+vDIVW/2], find falling DQ crossing at same level. If the associated pulse is a single pulse (< 1.5UI), then calculate the time different as tDIHL result. Find all valid rising and falling DQ crossings at [Vref-vDIVW/2] level in the specified burst. For all falling DQ crossing at [Vref-vDIVW/2], find rising DQ crossing at same level. If the associated pulse is a single pulse (< 1.5UI), then calculate the time different as tDIHL result. For all falling DQ crossing at [Vref-vDIVW/2], find rising DQ crossing at same level. If the associated pulse is a single pulse (< 1.5UI), then calculate the time different as tDIHL result. Determine the worst result from the set of tDIHL measured. 						
Expected/ Observable Results:	The measured value of tDIHL shall be within the conformance limits as per the JESD209-5C specification.						

Test ID & References: Table 177 LPDDR5 Test References from JESD209-5C Specification

Clock (Diff) Tests

The equations for the measurement of various parameters pertaining to Clock differential tests are given below:

$$tCK(avg) = \left(\sum_{j=1}^{N} tCKj\right)/N$$

where
$$N = 200$$

Figure 87 Calculation for tCK(avg)

$$tCH(avg) = \left(\sum_{j=1}^{N} tCHj\right) / (N \times tCK(avg))$$

where N = 200

Figure 88 Calculation for tCH(avg)

$$tCL(avg) = \left(\sum_{j=1}^{N} tCLj\right) / (N \times tCK(avg))$$

where N = 200

Figure 89 Calculation for tCL(avg)

tjit(per) = Min./Max. of {tCKi - tCK(avg), where i = 1 to 200}

Figure 90 Calculation for tjit(per)

Figure 91 Calculation for tjit(CC)



tCK(abs), tCH(abs) and tCL(abs) are measured directly on the Differential Clock signal and are considered as informative tests.

tCK(avg) Average Clock Period

Availability Condition: Table 178 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)			
Test ID & References:	Table 179 LPDDR5	i Test References from JI	SD209-5C Specification					
	Symbol (in Specificat	tion)	Test ID	Reference	from Specification			
	tCK(avg)		102020		Table 453-457			
Overview:		tCK(avg) is the average clock period across a consecutive 200-cycle window. This test measures the period from the rising edge of a cycle to the next rising edge within the waveform window.						
Procedure:	 Acquire 202 cycles from the test signal. Measure a sliding "window" of 200 cycles. Calculate the average period value for periods 1-200. Calculate the average period value for periods 2-201. Calculate the average period value for periods 3-202. Three measurement results are generated after step 4 is complete. Check the three measured results for the smallest and largest values, which are recorded as the worst case values. Compare the worst case values to the compliance test limits. 							
Expected/ Observable Results:	The measured value of tCK(avg) shall be within the conformance limits as per the JESD209-5C specification.							

tCK(abs) Absolute Clock Period

Availability Condition:	Table 180	Set Up tab options for availabil	ity of tests					
Supported CK Type	Supported WCK	Type Supports Offline?	R/W Separation needed	? SE Mode?	Required Signals			
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)			
Test ID & References:	Test ID & References: Table 181 LPDDR5 Test References from JESD209-5C Specification							
	Symbol (in	Specification)	Test ID	Reference f	rom Specification			
	tCK(abs)		102021		Table 453-457			

Availability Condition:

Overview:	tCK(abs) is the absolute clock period within a waveform window. This test measures the period from the rising edge of a cycle to the next consecutive rising edge within the waveform window.
Procedure:	1 Acquire 202 cycles from the test signal.
	2 Find the maximum period value for period 1-202.
	3 Find the minimum period value for period 1-202.
	4 Check the two results for the worst case values.
	5 Compare the worst case values to the compliance test limits.
Expected/ Observable Results:	The measured value of tCK(abs) for the test signal shall be within the conformance limits as per the JESD209-5C specification.

Set Up tab options for availability of tests

tCH(avg) Average High pulse width Table 182

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)		
Test ID & References:	Table 183 LPDD	R5 Test References from JE	SD209-5C Specification				
	Symbol (in Specifi	cation)	Test ID	Reference	from Specification		
	tCH(avg)		102022		Table 453-457		
Overview:	window. This te	tCH(avg) is the average pulse width across any consecutive 200 high pulses within a waveform window. This test measures the average duty cycle of all positive pulse widths within a window of 200 consecutive cycles.					
Procedure:	1 Acquire 202	cycles from the test	signal.				
	2 Measure a sliding "window" of 200 cycles.						
			ulses from cycle #1 to cy rates one measurement		nd determine the average		
	4 Measure the width of the high pulses from cycle #2 to cycle #201 and determine the average value for this window. This generates one more measurement result and two measurement values, overall.						
	5 Measure the width of the high pulses from cycle #3 to cycle #202 and determines the aver value for this window. This generates one more measurement result and three measuremer results, overall.						
		6 Check the three measured values for the smallest and largest values, which are recorded as the worst case values.					
	7 Compare th	e worst case values †	to the compliance test li	mits.			
/Expected Observable Results:	The measured value of tCH(avg) shall be within the conformance limits as per the JESD209-5C specification.						

tCL(avg) Average Low pulse width

Availability Condition: Table 184 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)			
Test ID & References:	Table 185 LPDDR5	i Test References from J	ESD209-5C Specification					
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification			
	tCL(avg)		102023		Table 453-457			
Overview:	window. This test	tCL(avg) is the average pulse width across any consecutive 200 low pulses within a waveform window. This test measures the average duty cycle of all negative pulse widths within a window of 200 consecutive cycles.						
Procedure:		cycles from the tes ding "window" of 2	0					
	3 Measure the	width of the low p	2		determine the average valu			
	 4 Measure the width of the low pulses from cycle#2 to cycle#201 and determine the average for this window. This generates one more measurement result and two measurement value overall. 5 Measure the width of the low pulses from cycle#3 to cycle#202 and determines the average for this window. This generates one more measurement result and three measurement result and three measurement result. 							
	6 Check the the worst case va		es for the smallest and la	rgest values	s, which are recorded as the			
	7 Compare the	worst case values	to the compliance test li	mits.				
Expected/ Observable Results:	The measured va specification.	The measured value of tCL(avg) shall be within the conformance limits as per the JESD209-5C						

tCH(abs) Absolute HIGH Clock pulse width

Availability Condition: Table 186

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

Set Up tab options for availability of tests

lest ID & References:	S: Table 187 LPDDR5 Test References from JESD209-5C specification							
	Symbol (in Specification)	Test ID	Reference from Specification					
	tCH(abs)	102024	Table 453-457					
Overview:	the following falling edge. This t	tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge. This test measures the absolute duty cycle of all positive pulse widths within a window of consecutive 200 cycles.						
Procedure:	 Acquire 202 cycles from the test signal. Find the maximum high pulses width value for positive pulses #1 to #202. Find the minimum high pulses width value for positive pulses #1 to #202. Check these two results for the worst case values. Compare the worst case values to the compliance test limits. 							
Expected/ Observable Results:	The measured value of tCH(abs) JESD209-5C specification.	for the test signal shall	be within the conformance limits as per the					

Test ID & References: Table 187 LPDDR5 Test References from JESD209-5C specification

tCL(abs) Absolute LOW Clock pulse width

Availability Condition:	Table 188	Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)			
Test ID & References:	Table 189 LPDDR5	Test References from JE	SD209-5C Specification					
	Symbol (in Specificat	Test ID	Reference	from Specification				
	Symbol (in Opconical			Reference				
	tCL(abs)		102025		Table 453-457			
Overview:	the following risin	tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge. This test measures the absolute duty cycle of all negative pulse widths within a window of 200 consecutive cycles.						
Procedure:	1 Acquire 202 c	ycles from the test	signal.					
	2 Find the maxi	mum low pulses w	idth value for negative p	oulses #1 to a	#202.			
			dth value for negative p	ulses #1 to #	ŧ202.			
	4 Check these t	wo results for the v	worst case values.					
	5 Compare the	worst case values t	to the compliance test li	mits.				
/Expected Observable Results:		The measured value of tCL(abs) for the test signal shall be within the conformance limits as per the JESD209-5C specification.						

tjit(CC) Maximum Clock Jitter between consecutive cycles

Availability Condition: Table 190 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)		
Test ID & References:	Table 191 LPDDR5	Test References from JE	SD209-5C Specification				
	Symbol (in Specification)		Test ID	Reference	from Specification		
	tjit(CC)		102026		Table 453-457		
Overview:		tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles. This test measures the clock period from the rising edge of a clock cycle to the next rising edge.					
Procedure:	 Acquire 202 cycles from the test signal. Measure the difference between every adjacent pair of periods. Generate a total of 201 measurement results. Check the results for the smallest and largest values, which are recorded as the worst case values. Compare the worst case values to the compliance test limits. 						
/Expected Observable Results:	The measured value of tJIT(cc) for the test signal shall be within the conformance limits as per the JESD209-5C specification.						

tjit(per) Clock period jitter

Availability Condition: Table 192 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

Test ID & References: Table 193 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
tjit(per)	102027	Table 453-457

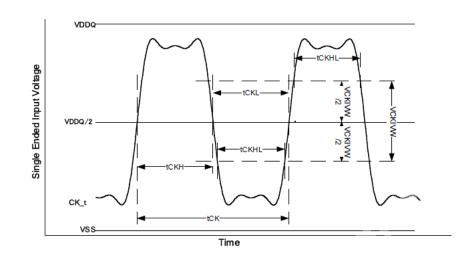
Overview: tJIT(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg). This test measures the difference between a measured clock period and the average clock period across multiple cycles of the clock.

Procedure: 1 Acquire 202 cycles from the test signal.

- 2 Measure the difference between every period inside a 200 cycle window with the average of the whole window.
- 3 Calculate the average for periods 1 to 200.
- 4 Measure the difference between period #1, period #2 and so on up to period #200; with the average and save the resulting value as a measurement result. A total of 200 measurement results are generated.
- 5 For the next set of measurement values, slide the window by one period and measure the average of period #2 up to period #201.
- 6 Compare period #2 with the new average.
 Continue the comparison for period #3, #4 and so on up to period #201.
 A total of 200 additional measurement results are generated such that there are 400 measured values overall.
- 7 For the next set of measurement values, slide the window by one more period and measure the average of period #3 up to period #202.
- Compare period #3 with the new average.
 Continue the comparison for period #4, #5 and so on up to period #202.
 A total of 200 additional measurement results are generated such that there are 600 measured values overall.
- 9 Check the 600 results for the smallest and largest values, which are recorded as the worst case values.
- 10 Compare the worst case values to the compliance test limits.

Expected/ The measured value of tJIT(per) for the test signal shall be within the conformance limits as per the **Observable Results:** JESD209-5C specification.

Clock (SE Mode) Tests



The single-ended mode clock timing parameters can be measured as shown in Figure 92.

Figure 92 Single-ended mode CK pulse definitions

```
tCKHL
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Availability Condition:	Table 194	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

Test ID & References: Table 195 LPDDR5 Test References from JESD209-5C Specification

	Symbol (in Specification)	Test ID	Reference from Specification
	tCKHL	251007	Table 432
Overview:	The purpose of this test is to ver signal.	rify the pulse width of all '	the high pulses and the low pulses in the test
Procedure:	2 Perform steps for tCKL to m	neasure the worst low pu	ulse width in the test signal. lse width in the test signal. pulse width and worst low pulse width
Expected/ Observable Results:	The measured value of tCKHL s specification.	hall be within the confor	mance limits as per the JESD209-5C

tCKH

Availability Condition: Table 196 Set Up tab options for availability of tests

Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)
Test ID & References: Table 197 LPDDR5 Test Refere		R5 Test References from J	ESD209-5C Specification		
	Symbol (in Specific	cation)	Test ID	Reference	from Specification
	tCKH		251010		Figure 312
Overview:	The purpose of	purpose of this test is to verify the pulse width of all the high pulse in the test signal.			
Procedure:	 Find all valid Clock starts the Clock. Find the ma Find the min 	at the valid rising e ximum high pulse v himum high pulse w he worst high pulse	edge of the Clock and end vidth value for all the pos vidth value for all the pos	ds at the foll itive pulses itive pulses i	
Expected/ Observable Results:	The measured value of tCKH shall be considered for "Information Only" purposes (as there are no conformance limits specified in JESD209-5C specification).			purposes (as there are no	
tCKL					
Availability Condition:	Table 198 Set U	o tab options for availabilit	ty of tests		

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

Test ID & References: Table 199 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
tCKL	251011	Figure 312

Overview: The purpose of this test is to verify the pulse width of all the low pulses in the test signal.

Procedure: 1 Pre-condition the oscilloscope.

- 2 Find all valid negative pulses of the Clock in the entire waveform. A valid negative pulse on the Clock starts at the valid falling edge of the Clock and ends at the following valid rising edge of the Clock.
- 3 Find the maximum low pulse width value for all the negative pulses identified.
- 4 Find the minimum low pulse width value for all the negative pulses identified.
- 5 Determine the worst low pulse width (tCKL) in the test signal from the maximum and minimum pulse width measured.

Expected/ The measured value of tCKL shall be considered for "Information Only" purposes (as there are no conformance limits specified in JESD209-5C specification).

Write Clock (Diff) tests

An LPDDR5 SDRAM utilizes two types of clock with different frequencies. The frequency of WCK is four times or twice higher than the command clock. LPDDR5 uses a DDR data interface. The data interface uses two differential forwarded clocks (WCK t/WCK c) that are source synchronous to the DQs. DDR means that the data is registered at every rising edge of WCK_t and rising edge of WCK_c. WCK_t and WCK_c operate at twice the frequency of the command/address clock (CK_t/CK_c). WCK t/WCK c is used to sample DQ data for write operation and toggle DQ data for read operation. WCK_t/WCK_c must start toggle before starting write or read DQ data burst. All data bits (DQ[7:0] for WCK t[0]/WCK c[0], and DQ[15:8] for WCK t[1]/WCK c[1]) carry the training feedback to the controller. WCK is required to be trained to arrive at the DQ latch center-aligned with the Data eye training is accomplished by delaying the DQ signals relative to WCK such that the Data eye arrives at the receiver latch centered on the WCK transition. The latency control unit inside the SDRAM performs clock domain change of WRITE or READ commands from CK domain to WCK domain. An LPDDR5 SDRAM supports WCK free running mode. The DRAM controller must keep WCK toggling at its full rate after WCK2CK synchronization regardless of DQ operation. An LPDDR5 SDRAM requires being in WCK2CK synchronization state before the internal write operation starts. For WRITE operations, WCK must be driven at least tWCKPRE Static+tWCKPRE Toggle WR before the write DQ burst. LPDDR5 will have a WCK post-amble of 0.5*tCK or TBD*tCK, after completing all write DQ burst.

The equations for the measurement of various parameters pertaining to Write Clock differential tests are given below:

$$tWCK(avg) = \left(\sum_{j=1}^{N} tWCKj\right)/N$$

where N = 200

Figure 93 Calculation for tWCK(avg)

$$tWCH(avg) = \left(\sum_{j=1}^{N} tWCHj\right) / (N \times tWCK(avg))$$

Figure 94 Calculati

Calculation for tWCH(avg)

$$tWCL(avg) = \left(\sum_{j=1}^{N} tWCLj\right) / (N \times tWCK(avg))$$

where
$$N = 200$$

Figure 95 Calculation for tWCL(avg)

tjit(per) = Min./Max. of {tWCKi - tWCK(avg), where i = 1 to 200}

Figure 96 Calculation for tjit(per) for WCK (Diff)

tjit(CC) = Max. of |{tWCK(i + 1) - tWCK(i)}|

Figure 97

Calculation for tjit(CC) for WCK (Diff)



tWCK(abs), tWCH(abs) and tWCL(abs) are measured directly on the Differential Write Clock signal and are considered as informative tests.

tWCK(avg) Average Write Clock period

Availability Condition: Table 200 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)
Test ID & References:	Table 201 LPDDF	85 Test References from JE	SD209-5C Specification		
	Symbol (in Specific	ation)	Test ID	Reference	from Specification
	tWCK(avg)		102000		Table 459
Overview:	iew: tWCK(avg) is the average write clock period across a consecutive 200-cycle window. This test measures the period from the rising edge of a cycle to the next rising edge within the wavefor window.				
Procedure:	 2 Measure a s 3 Calculate th 4 Calculate th 5 Calculate th 5 Calculate th 6 Check the th worst case v 	 Calculate the average period value for periods 1-200. Calculate the average period value for periods 2-201. Calculate the average period value for periods 3-202. Three measurement results are generated after step 4 is complete. Check the three measured results for the smallest and largest values, which are recorded as worst case values. 			
/Expected Observable Results:					s as per the JESD209-5C

tWCK(abs) Absolute Write Clock period

Availability Condition: Table 202 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)	
Test ID & References:	References: Table 203 LPDDR5 Test References fr		SD209-5C Specification			
Symbol (in Specification)			Test ID	Reference f	from Specification	
	tWCK(abs)		102001		Table 459	
Overview:	tWCK(abs) is the absolute write clock period within a waveform window. This test measures the period from the rising edge of a cycle to the next consecutive rising edge within the waveform window.					
Procedure:	 Acquire 202 cycles from the test signal. Find the maximum period value for period 1-202. Find the minimum period value for period 1-202. Check the two results for the worst case values. Compare the worst case values to the compliance test limits. 					
/Expected Observable Results:		The measured value of tWCK(abs) shall be within the conformance limits as per the JESD209-5C				

tWCKH(avg) Average High pulse width

Availability Condition: Table 204 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)

Test ID & References: Table 205 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
tWCKH(avg)	102002	Table 459

Overview: tWCKH(avg) is the average pulse width across any consecutive 200 high pulses within a waveform window. This test measures the average duty cycle of all positive pulse widths within a window of 200 consecutive cycles.

Procedure: 1	Acquire 202	2 cycles from the	test signal.
--------------	-------------	-------------------	--------------

- 2 Measure a sliding "window" of 200 cycles.
- 3 Measure the width of the high pulses from cycle #1 to cycle #200 and determine the average value for this window. This generates one measurement result.
- 4 Measure the width of the high pulses from cycle #2 to cycle #201 and determine the average value for this window. This generates one more measurement result and two measurement values, overall.
- 5 Measure the width of the high pulses from cycle #3 to cycle #202 and determines the average value for this window. This generates one more measurement result and three measurement results, overall.
- 6 Check the three measured values for the smallest and largest values, which are recorded as the worst case values.
- 7 Compare the worst case values to the compliance test limits.

Expected/ The measured value of tWCKH(avg) shall be within the conformance limits as per the JESD209-5C **Observable Results:** specification.

tWCKL(avg) Average Low pulse width

Availability Condition: Table 206 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)

Test ID & References: Table 207 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
tWCKL(avg)	102003	Table 459

Overview: tWCKL(avg) is the average pulse width across any consecutive 200 low pulses within a waveform window. This test measures the average duty cycle of all negative pulse widths within a window of 200 consecutive cycles.

Procedure:

- 1 Acquire 202 cycles from the test signal.
 - 2 Measure a sliding "window" of 200 cycles.
 - 3 Measure the width of the low pulses from cycle#1 to cycle#200 and determine the average value for this window. This generates one measurement result.
 - 4 Measure the width of the low pulses from cycle#2 to cycle#201 and determine the average value for this window. This generates one more measurement result and two measurement values overall.
 - 5 Measure the width of the low pulses from cycle#3 to cycle#202 and determine the average value for this window. This generates one more measurement result and three measurement results overall.
 - 6 Check the three measured values for the smallest and largest values, which are recorded as the worst case values.
 - 7 Compare the worst case values to the compliance test limits.

Expected/ The measured value of tWCKL(avg) shall be within the conformance limits as per the JESD209-5C **Observable Results:** specification.

tWCKH(abs) Absolute HIGH Write Clock pulse width

Availability Condition: Table 208 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)

Test ID & References: Table 209 LPDDR5 Test References from JESD209-5C Specification

	Symbol (in Specification)	Test ID	Reference from Specification	
	tWCKH(abs)	102004	Table 459	
Overview:	tWCKH(abs) is the absolute instantaneous write clock high pulse width, as measured from one ri edge to the following falling edge. This test measures the absolute duty cycle of all positive puls widths within a window of consecutive 200 cycles.			
Procedure:	 Acquire 202 cycles from the test signal. Find the maximum high pulses width value for positive pulses #1 to #202. Find the minimum high pulses width value for positive pulses #1 to #202. Check these two results for the worst case values. Compare the worst case values to the compliance test limits. 			
Expected/ Observable Results:	The measured value of tWCKH(abs) shall be within the conformance limits as per the JESD209-50 specification.			

tWCKL(abs) Absolute LOW Write Clock pulse width

Availability Condition:	Table 210 Set Up 1	ab options for availability	of tests		
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)
Test ID & References:	Table 211 LPDDR5	Test References from JE	SD209-5C Specification		
	Symbol (in Specifica	ion)	Test ID	Reference f	rom Specification
	tWCKL(abs)		102005		Table 459

Overview:	tWCKL(abs) is the absolute instantaneous write clock low pulse width, as measured from one falling edge to the following rising edge. This test measures the absolute duty cycle of all negative pulse widths within a window of 200 consecutive cycles.
Procedure:	1 Acquire 202 cycles from the test signal.
	2 Find the maximum low pulses width value for negative pulses #1 to #202.
	3 Find the minimum low pulses width value for negative pulses #1 to #202.
	4 Check these two results for the worst case values.
	5 Compare the worst case values to the compliance test limits.
Expected/ Observable Results:	The measured value of tWCKL(abs) shall be within the conformance limits as per the JESD209-5C specification.

tjit(CC) Maximum Write Clock Jitter between consecutive cycles

Availability Condition: Table 212 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)
Test ID & References:	Table 213 LPDDR	5 Test References from JE	SD209-5C Specification		
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification
	tjit(CC)		102006		Table 459
Overview:		s test measures the			een two consecutive write dge of a write clock cycle to
Procedure:	1 Acquire 202 d	cycles from the test	signal.		
	2 Measure the	difference between	every adjacent pair of p	eriods.	
	3 Generate a total of 201 measurement results.				
	4 Check the results for the smallest and largest values, which are recorded as the worst case values.			orded as the worst case	
	5 Compare the	worst case values ⁻	to the compliance test li	mits.	
/Expected Observable Results:		lue of tJIT(cc) shall	be within the conforma	nce limits a	s per the JESD209-5C

tjit(per) Write Clock period jitter

Availability Condition: Table 214 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)	
Test ID & References:	Table 215 LPDDR	5 Test References from JE	SD209-5C Specification			
	Symbol (in Specifica	ition)	Test ID	Reference	from Specification	
	tjit(per)		102007		Table 459	
Overview:	tWCK(avg). This	test measures the	efined as the largest dev difference between a me nultiple cycles of the writ	easured write	e clock period and the	
Procedure:	2 Measure the	 Acquire 202 cycles from the test signal. Measure the difference between every period inside a 200 cycle window with the average of the whole window. 				
	4 Measure the average and	 4 Measure the difference between period #1, period #2 and so on up to period #200; with the average and save the resulting value as a measurement result. A total of 200 measurement results are generated. 				
	5 For the next set of measurement values, slide the window by one period and measure the average of period #2 up to period #201.					
	Continue the A total of 200					
		 For the next set of measurement values, slide the window by one more period and measure th average of period #3 up to period #202. 				
	 8 Compare period #3 with the new average. Continue the comparison for period #4, #5 and so on up to period #202. A total of 200 additional measurement results are generated such that there are 600 measure values overall. 					
	9 Check the 60 values.	0 results for the sm	nallest and largest value	s, which are	recorded as the worst case	
	10 Compare the	worst case values	to the compliance test li	imits.		
Expected/ Observable Results:	The measured va specification.	alue of tJIT(per) sha	ll be within the conform	ance limits a	as per the JESD209-5C	

tERR(2per) Write Clock Cumulative error across 2 cycles

Availability Condition: Table 216 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)		
Test ID & References:	Table 217 LPDDR	Table 217 LPDDR5 Test References from JESD209-5C Specification					
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification		
	tERR(2per)		102008	Table 459			
Overview:	average clock pe		e cycles of the clock. Su		ed clock period and the easurements include multiple		
Procedure:	Example input te	st signal:					
	Frequency: 1 kH:	z, Number of cycle	s acquired: 202				
	 tERR(2per) is very similar to tJIT(per), except that a small 2-cycle window is formed inside a lar 200-cycle window. The width of the total consecutive cycles for the small window (denoted as compared against equivalent number of consecutive average cycles (denoted as C) obtained fr the large 200-cycle window (n x C), where C is the average value of the 200 cycle large window n is the number of cycles. In the case of tERR(2per), n = 2. The steps described in the following procedure cover for all cycles, when n is replaced by the respective number of cycles. 1 Calculate the average period inside the first large 200-cycle window, denote as C₁. 2 Calculate the small window width, W (total width of 2 consecutive cycles). The first small wi would cover period #1 and period #2. 				enoted as C) obtained from 200 cycle large window and escribed in the following mber of cycles. v, denote as C ₁ . ycles). The first small window		
	n=2 for tERR		alue from C_1 and W four	nd above usi	ng the equation below, where		
			n is the number of conse	-			
			by one period and find to over period #2 and period		the next 2 consecutive cycles		
		3 with the new valu					
		rocess described ir o period#200) is cc	n steps 1 to 5 until the la overed.	ast small win	dow within C_1 (from		
			and denote it as CumE				
	8 Repeat steps 1 to 7 to derive CumErr2 (for the second large 200-cycle window of period to #201) and CumErr3 (for the third large 200-cycle window of period cycle #3 to #202).						
		e worst error Cuml			the worst value as the result		
		e same as tERR(2pe indow size of 4-cyc		window size	e is 3-cycle wide. tERR(4per)		
/Expected Observable Results:	All measured val JESD209-5C spe		or the test signal shall be	e within the o	conformance limits as per the		

tERR(3per) Write Clock Cumulative error across 3 cycles

Availability Condition: Table 218 Set Up tab options for availability of tests

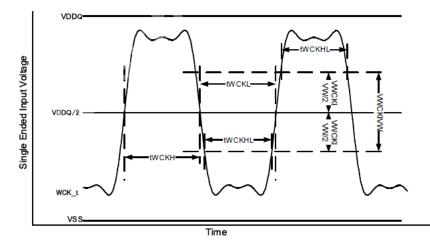
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	Puret & Captinuous	Vac	No	Yes	WCK(Diff)		
N/A	Burst & Continuous	Yes	No	Yes			
Test ID & References:	Table 219 LPDDR	5 Test References from JE	SD209-5C Specification				
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification		
	tERR(3per)		102009	Table 459			
Overview:	average clock pe	The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock. Supported measurements include multiple cycle windows with values of "n" (for "n" cycles).					
Procedure:	Example input te	st signal:					
	Frequency: 1 kHz	z, Number of cycles	s acquired: 202				
	 200-cycle window. The width of the total consecutive cycles for the small window (denoted as W) i compared against equivalent number of consecutive average cycles (denoted as C) obtained from the large 200-cycle window (n x C), where C is the average value of the 200 cycle large window an n is the number of cycles. In the case of tERR(3per), n = 3. The steps described in the following procedure cover for all cycles, when n is replaced by the respective number of cycles. 1 Calculate the average period inside the first large 200-cycle window, denote as C₁. 2 Calculate the small window width, W (total width of 2 consecutive cycles). The first small window would cover period #1 and period #2. 3 Calculate the cumulative error value from C₁ and W found above using the equation below, when n=3 for tERR(3per). 				enoted as C) obtained from 200 cycle large window and escribed in the following nber of cycles. <i>y</i> , denote as C ₁ . ycles). The first small window		
	tERR(nper) =	W - n x C ₁ , where r	n is the number of conse	ecutive cycle	S		
			by one period and find to over period #2 and perio		the next 2 consecutive cycles		
		3 with the new valu					
		rocess described ir o period#200) is co	i steps 1 to 5 until the la vered.	ist small win	dow within C_1 (from		
			and denote it as CumE				
			mErr2 (for the second la hird large 200-cycle win		cle window of period cycle #2 od cycle #3 to #202).		
	9 Determine th for tERR(3pe		Err1, CumErr2 and Cum	Err3. Report	the worst value as the result		
		e same as tERR(2pe indow size of 4-cyc		window size	e is 3-cycle wide. tERR(4per)		
Expected/ Observable Results:	All measured val JESD209-5C spe		or the test signal shall be	e within the c	conformance limits as per the		

tERR(4per) Write Clock Cumulative error across 4 cycles

Availability Condition: Table 220 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Supported on Type	Supported work type	Supports Ontine:	N/W Separation needed:	SL MOUE:	Required Signals		
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)		
Test ID & References:	Table 221 LPDDR	Table 221 LPDDR5 Test References from JESD209-5C Specification					
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification		
	tERR(4per)		102010	Table 459			
Overview:	average clock pe	The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock. Supported measurements include multiple cycle windows with values of "n" (for "n" cycles).					
Procedure:	Example input te	st signal:					
	Frequency: 1 kH	z, Number of cycles	s acquired: 202				
	 tERR(4per) is very similar to tJIT(per), except that a small 4-cycle window is formed inside a lar 200-cycle window. The width of the total consecutive cycles for the small window (denoted as compared against equivalent number of consecutive average cycles (denoted as C) obtained fr the large 200-cycle window (n x C), where C is the average value of the 200 cycle large window n is the number of cycles. In the case of tERR(4per), n = 4. The steps described in the following procedure cover for all cycles, when n is replaced by the respective number of cycles. 1 Calculate the average period inside the first large 200-cycle window, denote as C₁. 2 Calculate the small window width, W (total width of 2 consecutive cycles). The first small window using the equation below, we calculate the cumulative error value from C₁ and W found above using the equation below, we can also the compared approximation. 				enoted as C) obtained from 200 cycle large window and escribed in the following nber of cycles. v, denote as C ₁ . ycles). The first small window		
	n=4 for tERR tERR(nner) =	•	n is the number of conse	ecutive cycle			
	4 Sweep the sr	nall window across		the width of	the next 2 consecutive cycles		
		3 with the new valu					
	period#199 t	6 Repeat the process described in steps 1 to 5 until the last small window within C ₁ (from period#199 to period#200) is covered.					
			and denote it as CumE				
			mErr2 (for the second la hird large 200-cycle wir		cle window of period cycle #2 od cycle #3 to #202).		
	9 Determine th for tERR(2pe		Err1, CumErr2 and Cum	Err3. Report	the worst value as the result		
		e same as tERR(2pe indow size of 4-cyc		window size	e is 3-cycle wide. tERR(4per)		
/Expected Observable Results:	All measured val JESD209-5C spe		or the test signal shall be	e within the o	conformance limits as per the		

Write Clock (SE Mode) Tests



The single-ended mode write clock timing parameters can be measured as shown in Figure 92.

Figure 98 Single-ended mode WCK pulse definitions

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tWCKHL
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Availability Condition:	Table 222	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	Yes	Yes	WCK(Diff)
Test ID & References:	Table 223 LPDDR5 Test References from JESD209-5C Specification				
	Symbol (in Specification)		Test ID	Reference from Specification	
	tWCKHL		251107	Table 431	
Overview:	The purpose of this test is to verify the pulse width of all the high pulses and the low pulses in the test signal.				
Procedure:	 Perform steps for tWCKH to measure the worst high pulse width in the test signal. Perform steps for tWCKL to measure the worst low pulse width in the test signal. Determine the final worst result from the worst high pulse width and worst low pulse width measured. 				
/Expected Observable Results:	The measured value of tWCKHL shall be within the conformance limits as per the JESD209-5C specification.				

tWCKH

Availability Condition: Table 224 Set Up tab options for availability of tests

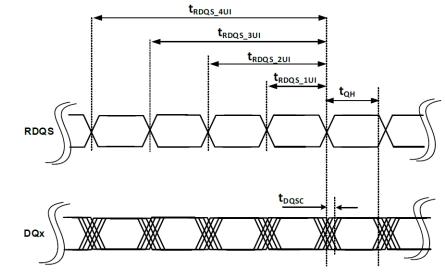
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	Yes	Yes	WCK(Diff)
Test ID & References:	Table 225 LPDDR	5 Test References from JES	SD209-5C Specification		
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification
	tWCKH		251110		Figure 310
Overview:	The purpose of t	his test is to verify t	he pulse width of all the	high pulses	in the test signal.
Procedure: Expected/ Observable Results:	 Consider the Find all valid Write Clock s falling edge of Find the max Find the mini Determine th minimum pui The measured value 	first valid WRITE or positive pulses of th starts at the valid ris of the Write Clock. imum high pulse wi mum high pulse wi e worst high pulse se width measured.	he Write Clock in the spe sing edge of the Write C dth value for all the pos dth value for all the pos width (tWCKH) in the te be considered for "Info	ecified burst. lock and end sitive pulses itive pulses i est signal from	A valid positive pulse on the ds at the following valid identified. dentified.
tWCKL Availability Condition: Supported CK Type		tab options for availability Supports Offline?	D209-5C specification). of tests R/W Separation needed?	SE Mode?	Required Signals
Supported CK Type	Supported work type	Supports offiline?	K/W Separation needed?	SE Mode?	Requireu Signais
N/A	Burst & Continuous	Yes	Yes	Yes	WCK(Diff)
Test ID & References:	Table 227 LPDDR	5 Test References from JES	SD209-5C Specification		
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification
	tWCKL		251111		Figure 310
• •					

Overview: The purpose of this test is to verify the pulse width of all the low pulses in the test signal.

- **Procedure:** 1 Acquire and identify the WRITE or READ burst data of the test signal.
 - 2 Consider the first valid WRITE or READ burst found.
 - 3 Find all valid negative pulses of the Write Clock in the specified burst. A valid negative pulse on the Write Clock starts at the valid falling edge of the Write Clock and ends at the following valid rising edge of the Write Clock.
 - 4 Find the maximum low pulse width value for all the negative pulses identified.
 - 5 Find the minimum low pulse width value for all the negative pulses identified.
 - 6 Determine the worst low pulse width (tWCKL) in the test signal from the maximum and minimum pulse width measured.

Expected/ The measured value of tWCKL shall be considered for "Information Only" purposes (as there are no conformance limits specified in JESD209-5C specification).

RDQS (Diff) Tests



The RDQS jitter parameters can be measured as shown in Figure 99.

Figure 99

N-UI DQ to RDQS output timing definitions



The NUI Jitter performs on a read burst and does not require read/write separation.

tjitRDQS_1UI(avg)

Availability Condition: Table 228 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	RDQS(Diff)

Test ID & References: Table 229 LPDDR5 Test Referen

29 LPDDR5 Test References from JESD209-5C Specification

	Symbol (in Specification)	Test ID	Reference from Specification
	tjitRDQS_1UI(avg)	102028	Table 464
Overview:	The purpose of this test is to m	neasure average 1UI jitter	of RDQS.
Procedure:	1 Acquire the RDQS signal.		
	2 Detect all the bursts in the	RDQS signal by analyzin	g the start and end of the bursts.
	3 For each burst:		
	• Measure all the positive and	d negative pulse widths w	vithin a burst.

	Store all measured values in the Measured List.
	4 AvgPulseWidth = The average of all pulse widths in the Measured List.
	5 Test result = AvgPulseWidth - UnitInterval. Note:UnitInterval=1/Datarate
Expected/ Observable Results:	The measured value of tjitRDQS_1UI(avg) shall be within the conformance limits as per the JESD209-5C specification.

tjitRDQS_1UI(abs)

Availability Conditi	on: Table 230	Set Up tab o	ptions for availability of test	s
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	RDQS(Diff)

Test ID & References: Table 231 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
tjitRDQS_1UI(abs)	102029	Table 464

Overview: The purpose of this test is to measure absolute 1UI jitter of RDQS.

- Procedure: 1
 - 1 Acquire the RDQS signal.
 - 2 Detect all the bursts in the RDQS signal by analyzing the start and end of the bursts.
 - 3 For each burst:
 - Measure the distance between n edge and (n+1) edge, where n>1, n+1<=the number of edges in a burst. For example, in the first iteration, measure the distance between the first edge and the second edge.
 - Store the measured value in the Measured List.
 - 4 In the Measured List, take the MaxValue, then calculate MaxEndResult=MaxValue-1.0*UnitInterval. Note:UnitInterval=1/Datarate
 - 5 In the Measured List, take the MinValue, then calculate MinEndResult=MinValue-1.0*UnitInterval. Note:UnitInterval=1/Datarate
 - 6 Compare MaxEndResult and MinEndResult with the test limit and pick the one that is worst as the test result.

Expected/ The measured value of tjitRDQS_1UI(abs) shall be within the conformance limits as per the JESD209-5C specification.

tjitRDQS_2UI(abs)

Availability Condition: Table 232 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	RDQS(Diff)
Test ID & References:	Table 233 LPDDR5	Test References from JE	SD209-5C Specification		
	Symbol (in Specificat	ion)	Test ID	Reference	from Specification
	tjitRDQS_2UI(abs)		102030		Table 464
Overview:	The purpose of th	is test is to measu	re absolute 2UI jitter of	RDQS.	
Procedure:	 2 Detect all the 2 For each burst Measure the d burst. For exar edge. Store the mea 4 In the Measur MaxEndResult Note:UnitInte 5 In the Measur MinEndResult Note:UnitInte 	bursts in the RDQ t: istance between n nple, in the first ite sured value in the ed List, take the M t=MaxValue-2.0*U rval=1/Datarate ed List, take the M :=MinValue-2.0*Ur rval=1/Datarate :EndResult and Min	ration, measure the dista Measured List. axValue, then calculate nitInterval. inValue, then calculate iitInterval.	here n>1, n+ ance betwee	nd of the bursts. 2<=the number of edges in a n the first edge and the thirc ck the one that is worst as
/Expected Observable Results:	The measured val JESD209-5C spe		I(abs) shall be within the	e conforman	ce limits as per the

tjitRDQS_3UI(abs)

Availability Condition:	Table 234	Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	RDQS(Diff)

	Symbol (in Specification)	Test ID	Reference from Specification
	tjitRDQS_3UI(abs)	102031	Table 464
Overview:	The purpose of this test is to me	easure absolute 3UI jitter	of RDQS.
Procedure:	1 Acquire the RDQS signal.		
		RDQS signal by analyzing	g the start and end of the bursts.
	3 For each burst:		
			e, where n>1, n+3<=the number of edges distance between the first edge and the
	• Store the measured value in	the Measured List.	
	4 In the Measured List, take th MaxEndResult=MaxValue-3. Note:UnitInterval=1/Datarat	0*UnitInterval.	ate
	5 In the Measured List, take th MinEndResult=MinValue-3.0 Note:UnitInterval=1/Datarat)*UnitInterval.	ate
	6 Compare MaxEndResult and the test result.	I MinEndResult with the	test limit and pick the one that is worst a

tjitRDQS_4UI(abs)

Availability Condition: Table 236 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	RDQS(Diff)
Test ID & References:	Table 237 LPDDR	5 Test References from JE	SD209-5C Specification		
	Symbol (in Specifica	ation)	Test ID	Reference f	rom Specification
	tjitRDQS_4UI(abs)		102032		Table 464
Overview:		his test is to measu	102032 re absolute 4UI jitter of I	RDQS.	Table 464

	 Measure the distance between n edge and (n+4) edge, where n>1, n+4<=the number of edges in a burst. For example, in the first iteration, measure the distance between the first edge and the fifth edge. Store the measured value in the Measured List.
	 In the Measured List, take the MaxValue, then calculate MaxEndResult=MaxValue-4.0*UnitInterval. Note:UnitInterval=1/Datarate
	5 In the Measured List, take the MinValue, then calculate MinEndResult=MinValue-4.0*UnitInterval. Note:UnitInterval=1/Datarate
	6 Compare MaxEndResult and MinEndResult with the test limit and pick the one that is worst as the test result.
Expected/ Observable Results:	The measured value of tjitRDQS_4UI(abs) shall be within the conformance limits as per the JESD209-5C specification.

tjitRDQS_1UI

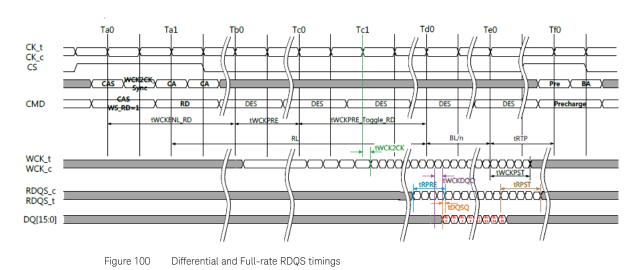
Availability Condition:	Table 238 Set Up ta	b options for availability o	ftests		
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	RDQS(Diff)
Test ID & References:	Table 239 LPDDR5	Test References from JESD	209-5C Specification		
	Symbol (in Specificati	on)	Test ID	Reference fr	om Specification
	tjitRDQS_1UI		102033		Table 464
Overview:	The tjitRDQS_1UI	is a remainder of at	osolute 1UI jitter of RD	QS with avera	age 1UI jitter removed.
Procedure:		QS_1UI(abs) and tji RDQS_1UI(abs) - tji	tRDQS_1UI(avg) test. tRDQS_1UI(avg).		
Expected/ Observable Results:				formance lim	its as per the JESD209-5C
tjitRDQS_3U	I				
Availability Condition:	Table 240 Set Up ta	b options for availability o	ftests		

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	RDQS(Diff)

Test ID & References: Table 241 LPDDR5 Test References from JESD209-5C Specification

	Symbol (in Specification)	Test ID	Reference from Specification			
	tjitRDQS_3UI	102034	Table 464			
Overview:	The tjitRDQS_3UI is a remainde	r of absolute 3UI jitter of R	DQS with average 1UI jitter removed			
Procedure:	 Perform tjitRDQS_3UI(abs) and tjitRDQS_1UI(avg) test. Test result=tjitRDQS_3UI(abs) - tjitRDQS_1UI(avg). 					
Expected/ Observable Results:	The measured value of tjitRDQS specification.	S_3UI shall be within the co	nformance limits as per the JESD209-5C			

Other timing tests



To check for various timing parameters, consider the timing diagram shown in Figure 100.



Availability Condition: Table 242 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	Burst only	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ	
Test ID & References:	Table 243 LPDDR5	Test References from JES	SD209-5C Specification			
	Symbol (in Specificat	ion)	Test ID	Reference f	rom Specification	
	tWCK2CK		131000	Table 32		
Overview:	The purpose of th (WCK) signal.	iis test is to verify t	he phase offset betweer	n the Clock (I	CK) signal and Write Clock	
Procedure:	 Acquire and split read and write burst of the acquired signal. Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded. Take the first valid READ or WRITE burst found. Find the first valid rising WCK edge (excluding the preamble pattern) of the specified burst. Find the nearest CK edge. Measure tWCK2CK as the time difference between these two edges of WCK and CK. 					
/Expected Observable Results:	The measured va specification.	The measured value of tWCK2CK shall be within the conformance limits as per the JESD209-5C				

tRPRE

Availability Condition: Table 244 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	Yes	DQ, RDQS(Diff)
Test ID & References:	Table 245 LPDDR5	Test References from JE	SD209-5C Specification		
	Symbol (in Specificat	ion)	Test ID	Reference	from Specification
	tRPRE		130000		Table 222
Overview:			he time when RDQS dif ate with the first DQ sig		t driving low (*preamble for the read cycle.
Procedure:		valid RDQS burst [.] reshold (0V) of the		g edge (befc	ore the toggling preamble) at
		2 Find the edge after the defined RDQS preamble length, which is configured in the General Setu window of the Set Up tab. Take this edge as tRPRE_end.			
		3 If RDQS Preamble = "Static:OtWCK, Toggle: 4tWCK", then tRPRE_start is at the found edge in step 1. If RDQS Preamble is other option, then tRPRE_start is at the extrapolated Low-Z point.			
	4 Measure the t	ime difference bet	ween these two edges(t	RPRE_start a	and tRPRE_end).
	5 Report the m	easurement as tRP	RE.		
/Expected Observable Results:		lue of tRPRE shall	be within the conformar	nce limits as	per the JESD209-5C
	·				

tRPST

Availability Condition: Table 246 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	Yes	DQ, RDQS(Diff)
Test ID & References: Table 247 LPDDR5 Test References from JESD209-5C Specification					
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification
	tRPST		130001		Table 222
Overview	v: The purpose of the table of table	nis test is to verify t	he time when RDQS is r	no longer dri	ving from high/low state to

rview: The purpose of this test is to verify the time when RDQS is no longer driving from high/low state to Hi-impedance from the last DQ signal crossing (last bit of the Read Data burst).

Procedure:	1 Find the last edge of the RDQS burst found.
	2 Find the edge pertaining to RDQS postamble length prior to the edge found in the previous step
	3 Measure the time difference between these two edges.
	4 Report the measurement as tRPST.
Expected/ Observable Results:	The measured value of tRPST shall be within the conformance limits as per the JESD209-5C specification.

tDQSQ

Availability Condition: Table 248 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	Yes	DQ, RDQS(Diff)

Test ID & References: Table 249 LPDDR5 Test References from JESD209-5C Specification

	Symbol (in Specification)	Test ID	Reference from Specification	
	tDQSQ	130002	Table 222	
Overview:	The purpose of this test is to ve access time to the associated o		n the RDQS (RDQS rising and falling edges) J) signal.	
Procedure:	 Find all valid rising and falling DQ crossings at VREFDQ level in the specified burst. For all DQ crossings found, locate the nearest RDQS edges. Measure the time difference between these two edges. Report the measurement as tDQSQ. 			
Expected/ Observable Results:	The measured value of tDQSQ specification.	shall be within the confor	mance limits as per the JESD209-5C	

tQSH

Availability Condition: Table 250 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?		Required Signals
N/A	N/A	Yes	Yes	Yes	WCK(Diff), DQ, RDQS(Diff)

Test ID & References:	Table 251 LPDDR5 Test References from JESD205	9-5C Specification			
	Symbol (in Specification)	Test ID	Reference from Specification		
	tQSH	130003	Table 335		
Overview:	The purpose of this test is to verify the w	idth of the positive	pulse of the RDQS signal.		
Procedure:	 Measure tQSH as the time starting from a rising edge of the RDQS positive pulse and ending at the following falling edge. Capture all values of tQSH. Determine the worst result from the set of tQSH measured. 				
Expected/ Observable Results:	The measured value of tQSH shall be wit specification.	hin the conformanc	e limits as per the JESD209-5C		

tQSL

Availability Condition: Table 252 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	Yes	WCK(Diff), DQ, RDQS(Diff)

Test ID & References: Table 253 LPDDR5 Test References from JESD209-5C Specification

	Symbol (in Specification)	Test ID	Reference from Specification
	tQSL	130004	Table 335
Overview:	The purpose of this test is to v	erify the width of the negati	ve pulse of the RDQS signal.
Procedure:	1 Measure tQSL as the time the following rising edge.	starting from a falling edge	of the RDQS negative pulse and ending at
	2 Capture all values of tQSL		
	3 Determine the worst result	t from the set of tQSL measu	ured.
Expected/	The measured value of tQSL s	hall be within the conforma	nce limits as per the JESD209-5C

Observable Results: specification. Keysight D9050LDDC LPDDR5 Test Application Methods of Implementation

6 Eye Diagram Tests

RDQS Detect Method for Read Write Separation194DQ Rx Voltage and Timing (WRITE) tests198DQ Rx Voltage and Timing (READ) tests211CA Rx Voltage and Timing tests216CS Rx Voltage and Timing tests229



RDQS Detect Method for Read Write Separation

RDQS Detect is a read write separation method. This method works when the signal source contains at least an RDQS signal and a WCK signal. In this method, the Read/Write burst data is identified based on the presence of RDQS burst. If WCK burst contains an RDQS burst, then it is a Read burst. If the WCK burst does not contain an RDQS burst, then it is a Write burst.

If you select the RDQS Detect mode as the burst identification method, you must select the length of the WCK Postamble in the WCK Postamble Length section of the LPDDR5 General Setup dialog box.

LPDDR5 General Setup		? [
JEDEC standard data rat	Set the data rate of the test signal by entering a custom value or select from the JEDEC standard data rate values.					
WCK : CK Ratio 2:1	WCK : CK Ratio 2:1 VCK Frequency : 1600 MHz Clock Frequency : 800 MHz					
Signal Source ——						
WCK_t (SE), WCK_c	(SE), RDQS_t (SE), RDQS_c (SE)					
Single-Ended M	ode					
Signal Operation Mod	e					
CK (Diff) Continuou	is 💙					
WCK (Diff) Burst	WCK (Diff) Burst WCK options					
RDQS Preamble/Posta	amble Length					
RDQS Preamble	Static: 4 tWCK, Toggle: 0 tWCK					
RDQS Postamble	0.5 tWCK					
RDQS Postamble Mode	Toggle					
WCK Postamble Length						
Identify the length of WCK Postamble.						
WCK Postamble	2.5 tWCK					
	2.5 tWCK					
🖌 Show Hints	4.5 tWCK 6.5 tWCK	OK Cancel				

Figure 101 LPDDR5 General Setup Dialog



Figure 102 WCK Burst Options Setup Dialog

Tests that support the RDQS Detect Burst Identification Method

The following Eye Diagram tests support the RDQS Burst Identification method:

WRITE Tests

- tDIVW1 Margin
- tDIVW2 Margin
- vDIVW Margin
- tDIPW
- tDIHL
- · VDIHL_AC
- tWCK2DQI_HF
- tDQ2DQ

READ Tests

- tQW
- tWCK2DQO_HF

Method of Implementation for the RDQS Detect Burst Identification Method

The following are the steps for the method of implementation for the RDQS Detect burst identification method:

- 1 Populate the burst from WCK signal.
- 2 Locate FirstWCKRising for the burst.
- 3 Compute TimeA = FirstWCKRising + tWCKPRE_Toggle_RD * ClockCycleWidth.
- 4 Compute TimeB = Start of WCK postamble. For example, if tWCKPST=2.5nWCK then TimeB = time of second last rising edge of WCK burst. If tWCKPST=4.5nWCK then TimeB = time of fourth last rising edge of WCK burst.
- 5 Compute TimeC = 0.5*(TimeA+TimeB)
- 6 Compute VmaxTimeCWithinUI = Vmax range from (TimeC 1*UI) to (TimeC + 1*UI)
- 7 Compute VminTimeCWithinUI = Vmin range from (TimeC 1*UI) to (TimeC + 1*UI)
- 8 If [(VmaxTimeCWithinUI > VOHDiff_RDQS) AND (VminTimeCWithinUI < VOLDiff_RDQS)] then the burst will be recognized as a READ burst. Otherwise, the burst will be recognized as a WRITE burst.
- 9 Repeat steps 2 to 8 for the rest of burst.

References for DQ Rx Voltage and Timing tests

LPDDR5 DQ, DMI, Parity and DBI Rx mask is defined as hexagonal mask as shown in Figure 103. The mask (vDIVW, tDIVW1, tDIVW2) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal.

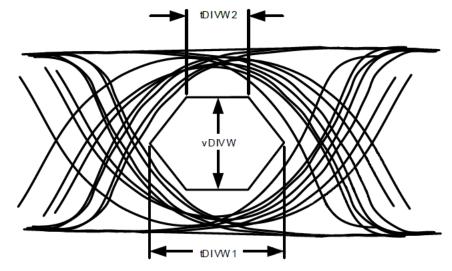


Figure 103 DQ Rx Mask definition

Rx mask voltage vDIVW has to be centered around VrefDQ as shown in Figure 104. DQ single input pulse amplitude into the receiver has to meet or exceed vDIHL_AC at any point over the total UI. vDIHL_AC is the peak to peak voltage centered around VrefDQ such that vDIHL_AC/2 min has to be met both above and below VrefDQ.

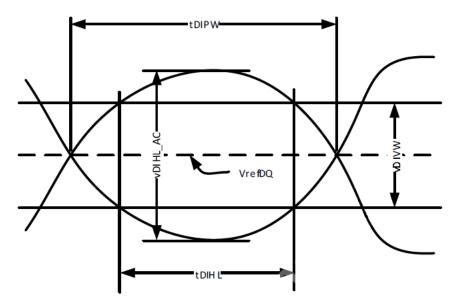


Figure 104 Identifying DQ Rx Mask parameters with respect to VrefDQ

tWCK2DQI is measured at the center (midpoint) of the tDIVW window, as shown in Figure 105. The LPDDR5-SDRAM uses an un-matched WCK-DQ path for lower power, so the WCK must arrive at the SDRAM ball prior to the DQ signal by the amount of tWCKDQI. The WCK must be trained to arrive at the DQ pad center-aligned with the DQ-data.

DQ, WCK data-in at DRAM Pin

Non Minimum Data Eye / Maximum Rx Mask

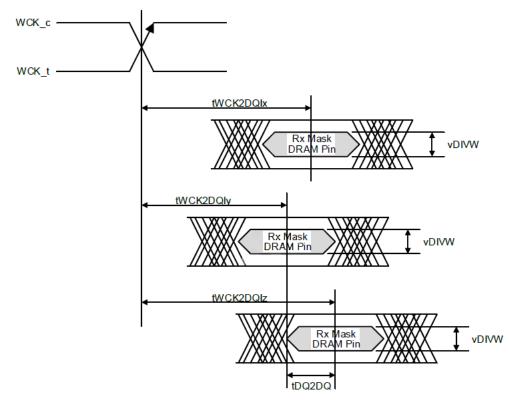


Figure 105 Identifying DQ Rx Mask parameters with respect to WCK

DQ Rx Voltage and Timing (WRITE) tests

tDIVW1 Margin

Availability Condition: Table 254 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst & Continuous	No	Yes	Yes	CK(Diff), WCK(Diff), DQ
Test ID & References:	Table 255 LPDDF	25 Test References from JE	SD209-5C Specification		
	Symbol (in Specific	ation)	Test ID	Reference	from Specification
	tDIVW1		141000		Table 467
Overview:	The purpose of t generated.	his test is to measu	re the minimum tDIVW1	Margin of t	he WRITE eye diagram
Procedure:	1 Calculate th Application.	e initial time scale v	alue based on selected s	speed grade	e options in the Test
	2 Check for va	lid WCK input test s	signals by verifying its fre	equency and	l amplitude values.
	3 Set up the o	scilloscope:			
			arate Write burst and re ed for eye folding later.	turn the filte	ered WCK signals as
	b Set up me	easurement threshol	d values for the DQx cha	annel and th	ne WCKx channel input.
			ues for DQx channel and	WCKx char	nnel input.
		olor Grade Display c	ption to ON.		
	e Set up Ma				
		ock Recovery on SD.			
			ed WCK, Rise/Fall Edge		
	-	eal Time Eye on SDA			
		zontal offset for the	eye diagram: st Application, under eye	o diagram +	poto povigoto to DO Dy
		nd Timing Tests:	si Application, under ey	e ulayraill te	בסוס, המעוצמופ נט שע אג

- Select 'UserDefined' to self define the eye horizontal offset
- Specify the user defined horizontal offset
- *b* The horizontal offset value is used to reposition the eye diagram horizontally.
- 5 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - *b* Load the mask file and start the Mask Test.
- 6 Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

- 7 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.
 - Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 8 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
- 9 Use the Histogram feature in the Infiniium Application to measure the tDIVW1 Margin value for both corners of the Test Mask.
 - The tDIVW1 Margin for each Test Mask corner is denoted by tDIVW1_m1 and tDIVW1_m2.
- 10 Find the minimum value between tDIVW1_m1 and tDIVW1_m2. Use the minimum value as the worst time gap.
- 11 Calculate the margin (in percentage) using the equation:

Margin (%) = [(Worst_time_gap) / (Half of mask width)] x 100%

where, Worst_time_gap is the time gap between the mask and the eye at corners m1 and m2.

12 Report the worst time gap and margin percentage as test results.

Expected/ The measured tDIVW1 Margin value for the test signal indicates if there is a violation in the mask region.

tDIVW2 Margin

Availability Condition: Table 256 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst & Continuous	No	Yes	Yes	CK(Diff), WCK(Diff), DQ
Test ID & References:	Table 257 LPDDR5	Test References from JES	SD209-5C Specification		
	Symbol (in Specificat	ion)	Test ID	Reference f	rom Specification
	tDIVW2		141001		Table 467
Overview:	The purpose of th generated.	nis test is to measur	re the minimum tDIVW2	Margin of tl	ne WRITE eye diagram

- **Procedure:** 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.
 - 2 Check for valid WCK input test signals by verifying its frequency and amplitude values.
 - 3 Set up the oscilloscope:
 - a Using UDF methodology, separate Write burst and return the filtered WCK signals as Recovered Clock, which is used for eye folding later.
 - *b* Set up measurement threshold values for the DQx channel and the WCKx channel input.
 - c Set up fixed vertical scale values for DQx channel and WCKx channel input.
 - *d* Set the Color Grade Display option to ON.
 - e Set up Mask Test.
 - f Set up Clock Recovery on SDA.
 - : Explicit clock, Source = filtered WCK, Rise/Fall Edge
 - g Set the Real Time Eye on SDA to ON.
 - 4 Perform horizontal offset for the eye diagram:
 - a In the Configure Tab of the Test Application, under eye diagram tests, navigate to DQ Rx Voltage and Timing Tests:
 - · Select 'UserDefined' to self define the eye horizontal offset
 - · Specify the user defined horizontal offset
 - b The horizontal offset value is used to reposition the eye diagram horizontally.
 - 5 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - b Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
 - 6 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - b Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.
 - · Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 7 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
- Use the Histogram feature in the Infiniium Application to measure the tDIVW2 Margin value for all the four corners of the Test Mask.
 The tDIVW2 Margin for each Test Mask corner is denoted by tDIVW2_m1, tDIVW2_m2, tDIVW2_m3 and tDIVW2_m4.
- 9 Find the minimum value between tDIVW2_m1, tDIVW2_m2, tDIVW2_m3 and tDIVW2_m4. Use the minimum value as the worst time gap.
- 10 Calculate the margin (in percentage) using the equation:

Margin (%) = [(Worst_time_gap) / (Half of mask width)] x 100%

where, Worst_time_gap is the time gap between the mask and the eye at four corners m1, m2, m3, m4.

11 Report the worst time gap and margin percentage as test results.

Expected/ The measured tDIVW2 Margin value for the test signal indicates if there is a violation in the mask region.

vDIVW Margin

Availability Condition: Table 258 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst & Continuous	No	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: Table 259 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
vDIVW	141002	Table 467

- **Overview:** The purpose of this test is to measure the minimum vDIVW Margin of the WRITE eye diagram generated.
- **Procedure:** 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.
 - 2 Check for valid WCK input test signals by verifying its frequency and amplitude values.
 - 3 Set up the oscilloscope:
 - a Using UDF methodology, separate Write burst and return the filtered WCK signals as Recovered Clock, which is used for eye folding later.
 - b Set up measurement threshold values for the DQx channel and the WCKx channel input.
 - c Set up fixed vertical scale values for DQx channel and WCKx channel input.
 - *d* Set the Color Grade Display option to ON.
 - e Set up Mask Test.
 - f Set up Clock Recovery on SDA.
 - : Explicit clock, Source = filtered WCK, Rise/Fall Edge
 - g Set the Real Time Eye on SDA to ON.
 - 4 Perform horizontal offset for the eye diagram:
 - a In the Configure Tab of the Test Application, under eye diagram tests, navigate to DQ Rx Voltage and Timing Tests:
 - · Select 'UserDefined' to self define the eye horizontal offset
 - · Specify the user defined horizontal offset
 - b The horizontal offset value is used to reposition the eye diagram horizontally.

- 5 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - *b* Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 6 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.
 - · Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 7 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
- 8 Use the Histogram feature in the Infiniium Application to measure the vDIVW Margin value for the top and the bottom area of the Test Mask. The measured vDIVW margin is denoted as vDIVW Margin upper and vDIVW Margin lower.
- 9 Find the minimum value between vDIVW Margin Upper and vDIVW Margin lower. Use this value as the worst voltage gap.
- 10 Calculate the worst margin (in percentage) using the equation:

Margin (%) = [(Worst_voltage_gap) / (Half of mask height)] x 100%

where, Worst_voltage_gap is the voltage gap between the mask and the eye at the top and bottom.

11 Report the worst voltage gap and the margin percentage as test results.

Expected/ The measured value of vDIVW Margin for the test signal indicates if there is a violation in the mask region.

tDIPW

Availability Condition: Table 260 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst & Continuous	No	Yes	Yes	CK(Diff), WCK(Diff), DQ

	Symbol (in Specification)	Test ID	Reference from Specification
	tDIPW	141003	Table 467
Overview:	The purpose of this test is to ve	erify the minimum input D	Q Rx pulse width defined at the Vcent_DQ
Procedure:	 This test requires the follow tDIVW1 Margin (Test ID: 14 Location for Vcent is determined) 	1000)	ed.
	2 Acquire and identify the RE	AD and WRITE burst data	of the acquired signal.
	3 Use all valid WRITE bursts		
	4 Find all valid rising and falli WRITE data burst.	ing DQ edges, which are d	lefined as the crossings at Vcent in the
	5 Measure tDIPW as the time following falling/rising edge		ng edge of the DQ to the time ending at t
	6 Process all valid edges in th	ne WRITE data burst.	
	7 Collect all tDIPW.		
	8 Determine the worst result result.	from the set of tDIPW valu	ues measured and report it as the final te
Expected/ servable Results:	The measured value of tDIPW f JESD209-5C specification.	for the test signal shall be	within the conformance limit as per the

Test ID & References: Table 261 LPDDR5 Test References from JESD209-5C Specification

tDIHL

Availability Condition: Table 262 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst & Continuous	No	Yes	Yes	CK(Diff), WCK(Diff), DQ
Test ID & References:	Table 263 LPDD	R5 Test References from JE	SD209-5C Specification		
	Symbol (in Specific	cation)	Test ID	Reference	from Specification
	tDIHL		141004		Table 467
Overview:	The purpose of defined at the V	,	he minimum input DQ R	x pulse widt	th above and below vDIVW
Procedure:	1 Calculate th Application.		alue based on selected s	speed grade	options in the Test
	2 Check for va	alid WCK input test s	ignals by verifying its fre	equency and	amplitude values.

- 3 Set up the oscilloscope:
 - a Using UDF methodology, separate Write burst and return the filtered WCK signals as Recovered Clock, which is used for eye folding later.
 - b Set up measurement threshold values for the DQx channel and the WCKx channel input.
 - c Set up fixed vertical scale values for DQx channel and WCKx channel input.
 - *d* Set the Color Grade Display option to ON.
 - e Set up Mask Test.
 - f Set up Clock Recovery on SDA.
 - : Explicit clock, Source = filtered WCK, Rise/Fall Edge
 - g Set the Real Time Eye on SDA to ON.
- 4 Perform horizontal offset for the eye diagram:
 - a In the Configure Tab of the Test Application, under eye diagram tests, navigate to DQ Rx Voltage and Timing Tests:
 - · Select 'UserDefined' to self define the eye horizontal offset
 - · Specify the user defined horizontal offset
 - b The horizontal offset value is used to reposition the eye diagram horizontally.
- 5 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - b Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 6 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - b Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.
 - Select a positive value greater than 0 to specify vCENT.
 - To obtain the vCENT value with 'WidestOpening' selected:
 - i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
 - ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
 - iii Use the voltage level at the widest eye opening as the value for Vcent.
- 7 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
- Use the Histogram feature to measure the width of the eye opening at the top and bottom of the 8 mask.
- The worst value of the width obtained between the top and bottom is reported as tDIHL. 9

Expected/ **Observable Results:**

The measured value of tDIHL for the test signal shall be within the conformance limit as per the JESD209-5C specification.

vDIHL_AC

Availability Condition: Table 264 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst & Continuous	No	Yes	Yes	CK(Diff), WCK(Diff), DQ
Test ID & References:	Table 265 LPDDR5	Test References from JE	SD209-5C Specification		
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification
	VDIHL_AC		141005		Table 467
Overview:		nis test is to measu ceed at any point o		oulse ampliti	ude vDIHL_AC that the pulse
Procedure:	 Application. Check for val Set up the os a Using UDF Recovered b Set up mean c Set up fixe d Set the Conent e Set up Cloneter f Set up Cloneter g Set the Reference Perform horizing a In the Connent Voltage and Select 'Use Specify the best of the horizone Ferform Massing a Set the Massing b Coad the mesting c Stop the Nent a In the Connent b Coad the mesting c Stop the Nent <lic li="" nent<="" stop="" the=""> c Stop the Nent c Stop the Nen</lic>	id WCK input test a cilloscope: I methodology, sep Clock, which is us asurement thresho d vertical scale val lor Grade Display of sk Test. ck Recovery on SD cock, Source = filter al Time Eye on SD contal offset for the figure Tab of the Te d Timing Tests: erDefined' to self d a user defined horiz ntal offset value is c Testing: ask Test Run Until s hask file and start t fask Test when the a specified in the co d store the Vcent of figure tab of the Te Diagram Tests, na This is the level, wh	ues for DQx channel an option to ON. A. red WCK, Rise/Fall Edge A to ON. e eye diagram: est Application, under ey efine the eye horizontal zontal offset used to reposition the e setting to 'Forever'. the Mask Test. counter for 'Total Wave onfiguration option 'Tota value. To determine the st Application, choose N	requency and eturn the filte hannel and th d WCKx cha e ye diagram t offset eye diagram forms' excee al Waveform' value of Vce Mode as Deb and Timing of the Eye M	d amplitude values. ered WCK signals as he WCKx channel input. nnel input. ests, navigate to DQ Rx horizontally. eds the number of required

	 Select a positive value greater than 0 to specify vCENT.
	To obtain the vCENT value with 'WidestOpening' selected:
	i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
	ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
	iii Use the voltage level at the widest eye opening as the value for Vcent.
	7 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
	8 Use the Histogram feature in the Infiniium Application to measure the vDIHL_AC/2 values for the top and the bottom area of the Test Mask. The measured vDIHL_AC/2 values is denoted as vDIHL_AC/2_top and vDIHL_AC/2_bottom.
	9 Calculate vDIHL_AC using the equation:
	vDIHL_AC = [vDIHL_AC/2_top] - [vDIHL_AC/2_bottom]
	10 Report the measured vDIHL_AC as test result.
Expected/ Observable Results:	The measured value of vDIHL_AC for the test signal shall be within the conformance limit as per the JESD209-5C specification.

tWCK2DQI_HF

Availability Condition:	Table 266	Set Up tab	options for availability of	tests		
Supported CK Type	Supported WCK	Туре	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst only		No	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: Table 267 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
tWCK2DQI_HF	141007	Table 462

Overview: The purpose of this test is to verify the offset between the WCK signal and the start of DQ input pulse / DQ input Rx mask.

Procedure: 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid WCK input test signals by verifying its frequency and amplitude values.

- 3 Set up the oscilloscope:
 - a Using UDF methodology, separate Write burst and return the filtered WCK signals as Recovered Clock, which is used for eye folding later.
 - *b* Set up measurement threshold values for the DQx channel and the WCKx channel input.
 - c Set up fixed vertical scale values for DQx channel and WCKx channel input.
 - d Set the Color Grade Display option to ON.
 - e Set up Mask Test.
 - f Set up Clock Recovery on SDA.
 - : Explicit clock, Source = filtered WCK, Rise/Fall Edge
 - g Set the Real Time Eye on SDA to ON.
- 4 Realign the eye opening of the first transition DQ bit to the center of the screen:
 - *a* Increase the search range on the screen to the range specified in the 'First DQ Transition Search Range (ps)' configuration option in the Configure tab, so that the crossing point of the eye is visible on the screen.
 - *b* Use the Histogram feature to find the first crossing point at 'VRefDQ' level horizontally across the screen.
 - c Realign the center of the eye to the middle time position.

NOTE

If the Test Application is unable to find any cross point within the search range, it prompts an error and this test run is aborted.

- 5 Perform horizontal offset for the eye diagram:
 - a In the Configure Tab of the Test Application, under eye diagram tests, navigate to DQ Rx Voltage and Timing Tests:
 - · Select 'UserDefined' to self define the eye horizontal offset
 - · Specify the user defined horizontal offset
 - b The horizontal offset value is used to reposition the eye diagram horizontally.
- 6 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - *b* Load the mask file and start the Mask Test.
 - *c* Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 7 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.
 - Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 8 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.

Expected/ Observable Results:	 10 Determine the locatio as FilteredWCKLoc. 11 Compute the final tes tWCK2DQI_HF = EyeC 12 Determine the worst r final test result. 	time at the Vcent level of th on of the filtered WCK rising e st result using the equation: CenterLoc - FilteredWCKLoc result from the set of tWCK2 VCK2DQI_HF for the test sig ration.	edges used in the rea	covered clock and denote it sured and report it as the
Write Eye Di	agram			
Availability Condition:	Table 268 Set Up tab options	for availability of tests		
Supported CK Type	Supported WCK Type Suppor	rts Offline? R/W Separation no	eeded? SE Mode?	Required Signals
Burst & Continuous	Burst only Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ
Test ID & References:	Symbol (in Specification)	rences from JESD209-5C Specification Test ID	Reference fro	om Specification
	NA (Information_Only test)		N	A (Information-Only test)
Overview:	generate an eye diagram	141009 s to automate all the require for the data WRITE cycle. having a mask test is that it agram created.	d setup procedures	

- · Save equalization output as BIN file.
- 9 If DFE mode is Auto/Manual
 - Load BIN file(post DFE DQ) into WMemory2.
 - If DFE is OFF
 - Load acquired DQ signal into WMemory2.
- 10 Load "WCKEyeFilt.bin" into WMemory4. Then use Function2 as "Magnify/Duplicate" of Loaded Waveform Memory.
- 11 Setup Clock Recovery settings on SDA.
 - Explicit clock, Source = Function2(WCKEyeFilt), Rise/Fall Edge
- 12 Setup measurement threshold values for the Function3(Data) and the Function2(WCKEyeFilt).
- 13 Setup fix time scale and time position values for Function3(Data) and Function2(WCKEyeFilt).
- 14 Turn ON Color Grade Display option.
- 15 Identify the X1 value for re-adjustment of selected test mask.
- 16 Setup Mask Test settings.
- 17 Turn ON Real Time Eye on SDA.
- 18 Start mask test until eye diagram folded.
- 19 Return total failed UnitInterval as a test result.

Expected/ The measured value of Write Eye Diagram for the test signal is considered for 'Information-Only' **Observable Results:** purpose.

```
tDQ2DQ
```

Availability Condition:	Table 270 Set Up	tab options for availability	of tests			
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
N/A	Burst only	No	Yes	Yes	WCK(Diff), DQ[x], DQ[Y]	
Test ID & References:	Test ID & References: Table 271 LPDDR5 Test References from JESD209-5C Specification					
	Symbol (in Specifica	ition)	Test ID	Reference	from Specification	

Symbol (in Specification)	Test ID	Reference from Specification
tDQ2DQ	141008	Table 467

Overview:

: The purpose of this test is to measure the DQ to DQ offset.

Procedure:

1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid WCK, DQ[x], DQ[y] input test signals by verifying its frequency and amplitude values.

- 3 Set up the oscilloscope:
 - a Using UDF methodology, separate Write burst and return the filtered WCK signals as Recovered Clock, which is used for eye folding later.
 - b Set up measurement threshold values for the DQx channel and the WCKx channel input.
 - c Set up fixed vertical scale values for DQx channel and WCKx channel input.
 - d Set the Color Grade Display option to ON.
 - e Set up Mask Test.
 - f Set up Clock Recovery on SDA.
 - : Explicit clock, Source = filtered WCK, Rise/Fall Edge
 - g Set the Real Time Eye on SDA to ON.
- 4 Perform horizontal offset for the eye diagram:
 - *a* In the Configure Tab of the Test Application, under eye diagram tests, navigate to DQ Rx Voltage and Timing Tests:
 - · Select 'UserDefined' to self define the eye horizontal offset
 - · Specify the user defined horizontal offset
 - b The horizontal offset value is used to reposition the eye diagram horizontally.
- 5 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - b Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 6 Determine and store the Vcent value of DQ[x] and DQ[y]. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.
 - Select a positive value greater than 0 to specify vCENT.
 - To obtain the vCENT value with 'WidestOpening' selected:
 - i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
 - ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
 - iii Use the voltage level at the widest eye opening as the value for Vcent.
- 7 Use Histogram measurements to determine the center location of the eye diagram at Vcent level and denote it as EyeCenterLoc1 (for Data Source 1) and EyeCenterLoc2 (for Data Source 2).
- 8 Position the scope marker (M1) at EyeCenterLoc1. Note the value as tM1.
- 9 Position the another marker (M2) at EyeCenterLoc2. Note the value as tM2
- 10 Measure tDQ2DQ as the difference of the two marker positions:

tDQ2DQ = tM1 - tM2

where, Worst_time_gap is the time gap between the mask and the eye at corners m1 and m2.

11 Report the difference as the final value of tDQ2DQ.

Expected/ The measured value of tDQ2DQ for the test signal shall be within the conformance limit as per the JESD209-5C specification.

DQ Rx Voltage and Timing (READ) tests

tQW

Availability Condition: Table 272 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	Yes	Yes	CK(Diff), DQ, RDQS(Diff)
Test ID & References: Table 273 LPDDR5 Test Re		Test References from JESD	209-5C Specification		

Symbol (in Specification)	Test ID	Reference from Specification
tQW	140000	Table 464

Overview: The purpose of this test is to verify the tQW parameter by measuring the DQ Read Eye.

Procedure:

- Calculate initial time scale value based on selected LPDDR5 speed grade options.
 Check for valid RDQS input test signals by verifying its frequency and amplitude values.
- 3 Set up the oscilloscope:
 - a Using UDF methodology, separate Write burst and return the filtered RDQS signals as recovered clock for eye folding later.
 - b Set up measurement threshold values for the DQ channel and the RDQS channel input.
 - c Set up vertical scale values for DQ channel and RDQS channel input.
 - d Set Color Grade Display option to ON.
 - e Set up Mask Test settings.
 - f Set up Clock Recovery settings on SDA.
 - : Explicit clock, Source = filtered RDQS, Rise/Fall Edge
 - g Set Real Time Eye on SDA to ON.
- 4 Perform horizontal offset for the eye diagram:
 - a In the Configure Tab of the Test Application, under eye diagram tests, navigate to DQ Rx Voltage and Timing Tests:
 - · Select 'UserDefined' to self define the eye horizontal offset
 - · Specify the user defined horizontal offset
 - *b* The horizontal offset value is used to reposition the eye diagram horizontally.
- 5 Perform Mask Testing:
 - a Set the Mask Test Run setting to 'Forever'.
 - *b* Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 6 Measure the Eye Height and Eye Width.
- 7 Report the measured Eye Height and Eye Width.

Expected/ The measured tQW value for the test signal shall be within the conformance limit as per the JESD209-5C specification.

tWCK2DQO_HF

Availability Condition: Table 274 Set Up tab options for availability of tests

Burst & Continuous	Burst only	No	Yes	Yes	CK(Diff), WCK(Diff), DQ		
Test ID & References:	Table 275 LPD	Table 275 LPDDR5 Test References from JESD209-5C Specification					
	Symbol (in Speci	ication)	Test ID	Reference	e from Specification		
	tWCK2DQ0_HF		140007		Table 462		
Overview:		The purpose of this test is to verify the offset between the WCK signal and the start of DQ output pulse / DQ output Rx mask.					
Procedure:	Application 2 Check for v 3 Set up the a Using U Recover b Set up r c Set up r c Set up r c Set up r c Set up N f Set up C : Explicit g Set the 4 Realign the a Increase Search R eye is via b Use the the scre	n. valid WCK input test oscilloscope: DF methodology, sej ed Clock, which is us neasurement thresho xed vertical scale va Color Grade Display Mask Test. Clock Recovery on SI clock, Source = filte Real Time Eye on SD e eye opening of the the search range or Range (ps)' configura sible on the screen. Histogram feature to en.	me scale value based on selected speed grade options in the Test nput test signals by verifying its frequency and amplitude values. be: ology, separate Read burst and return the filtered WCK signals as which is used for eye folding later. Int threshold values for the DQx channel and the WCKx channel input. I scale values for DQx channel and WCKx channel input. I scale values for DQx channel and WCKx channel input. e Display option to ON. very on SDA. rece = filtered WCK, Rise/Fall Edge Eye on SDA to ON. ng of the first transition DQ bit to the center of the screen: or range on the screen to the range specified in the 'First DQ Transition configuration option in the Configure tab, so that the crossing point of				

- 5 Perform horizontal offset for the eye diagram:
 - a In the Configure Tab of the Test Application, under eye diagram tests, navigate to DQ Rx Voltage and Timing Tests:
 - Select 'UserDefined' to self define the eye horizontal offset

- Specify the user defined horizontal offset
- *b* The horizontal offset value is used to reposition the eye diagram horizontally.
- 6 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - *b* Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 7 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - b Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.
 - Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 8 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
- 9 Find the mid-point in time at the Vcent level of the eye diagram and denote it as EyeCenterLoc.
- 10 Determine the location of the filtered WCK rising edges used in the recovered clock and denote it as FilteredWCKLoc.
- 11 Compute the final test result using the equation:

tWCK2DQO_HF = EyeCenterLoc - FilteredWCKLoc

12 Determine the worst result from the set of tWCK2DQO_HF values measured and report it as the final test result.

Expected/ The measured value of tWCK2DQO_HF for the test signal shall be within the conformance limit as per the JESD209-5C specification.

References for CA Rx Voltage and Timing tests

LPDDR5 command and address interface operates from a differential clock (CK_t and CK_c). Commands and addresses are registered single data rate (SDR) at every rising edge of CK. Chip Select (CS) is part of the command code, and is sampled on the rising(falling) edge of CK_t (CK_c). The Read/Write command behavior depends on the bank architecture. The READ and WRITE commands are each initiated with CS, and CA[6:0] asserted to the proper state at the rising and falling edges of CK, as defined by the Command Truth Table (refer to *Table 154* of the *JESD209-5* specification). Command/Address ODT (On-Die Termination) is a feature of the LPDDR5 SDRAM that allows the SDRAM to turn on/off termination resistance for CK_t, CK_c, and CA[6:0] signals.

LPDDR5 CA Rx mask is defined as hexagonal mask shape as shown in Figure 106. All CA signals apply the same compliance mask and operate in double data rate mode. The receiver mask (Rx Mask vCIVW, tCIVW1, tCIVW2) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal. CA Rx mask window center is around CK_t/CK_c cross point (differential mode). Rx mask voltage vCIVWI(max) has to be centered around VrefCA. CA single input pulse signal amplitude into the receiver has to meet or exceed vCIHL_AC at any point over the total UI. vCIHL_AC is the peak to peak voltage centered around VrefCA such that vCIHL_AC/2 min has to be met both above and below VrefCA. vCIHL_AC does not have to be met when no transitions are occurring. tCA2CA is defined fastest CA[x] mask center to slowest CA[y] mask center.

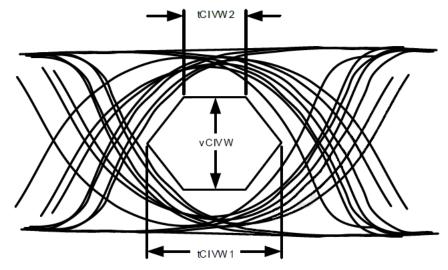
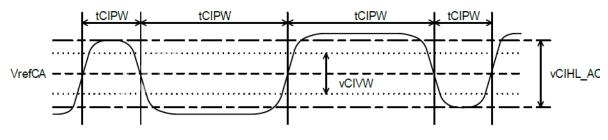
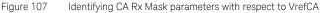


Figure 106 CA Rx Mask Defintion





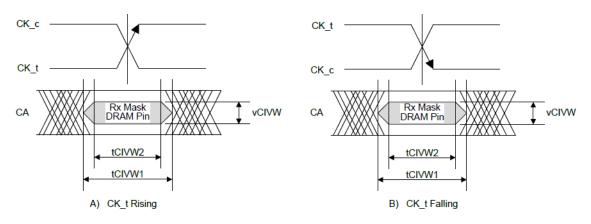


Figure 108 Identifying CA Rx Mask parameters with respect to CK

CA Rx Voltage and Timing tests

tCIVW1 Margin

Availability Condition: Table 276 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CA
Test ID & References:	Table 277 LPDDR5	Test References from JESD	209-5C Specification		

Symbol (in Specification)	Test ID	Reference from Specification
tCIVW1	142001	Table 466

Overview: The purpose of this test is to measure the minimum tCIVW1 Margin of the CA eye diagram generated.

Procedure: 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

- 2 Check for valid Clock (CK) and CA input test signals by verifying its frequency and amplitude values.
- 3 On the Oscilloscope:
 - a Set the Trigger to 'Auto-Sweep'.
 - b Set the Sampling Rate of the Oscilloscope to the maximum value.
 - *c* Set the Sampling Points to the user defined value configured for the 'Sampling Points (Pts) for Eye Diagram Tests Only' configuration option in the Configure tab of the Test Application.
 - d Set Function 1 to duplicate the CK signal.
 - e Set the Color Grade Display option to ON.
 - f Set up Mask Test settings.
 - g Set up Clock Recovery on SDA.
 - : Explicit clock, Source = Function 1, Rising Edge
 - h Set the Real Time Eye on SDA to ON.
 - *i* Set up measurement threshold values for Function 1 and CA input signals.
 - *j* Change Trigger Source to 'CA input signal' on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CA bus.
- 4 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - b Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 5 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to CA Rx Voltage and Timing tests > vCENT CA mode (V). This is the level, where the vertical center of the Eye Mask is placed.

- · Select 'WidestOpening' to use the widest eye opening as vCENT.
- · Select a positive value greater than 0 to specify vCENT.

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
- 7 Use the Histogram feature in the Infiniium Application to measure the tCIVW1 Margin value for both corners of the Test Mask.

The tCIVW1 Margin for each Test Mask corner is denoted by tCIVW1_m1 and tCIVW1_m2.

- 8 Find the minimum value between tCIVW1_m1 and tCIVW1_m2. Use the minimum value as the worst time gap.
- 9 Calculate the margin (in percentage) using the equation:

Margin (%) = [(Worst_time_gap) / (Half of mask width)] x 100%

where, Worst_time_gap is the time gap between the mask and the eye at corners m1 and m2. 10 Report the worst time gap and margin percentage as test results.

Expected/ The measured tCIVW1 Margin value for the test signal indicates if there is a violation in the mask region.

tCIVW2 Margin

Availability Condition: Table 278 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CA

Test ID & References: Table 279 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
tCIVW2	142002	Table 466

Overview: The purpose of this test is to measure the minimum tCIVW2 Margin of the CA eye diagram generated.

Procedure: 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid Clock (CK) and CA input test signals by verifying its frequency and amplitude values.

- 3 On the Oscilloscope:
 - a Set the Trigger to 'Auto-Sweep'.
 - b Set the Sampling Rate of the Oscilloscope to the maximum value.
 - c Set the Sampling Points to the user defined value configured for the 'Sampling Points (Pts) for Eye Diagram Tests Only' configuration option in the Configure tab of the Test Application.
 - *d* Set Function 1 to duplicate the CK signal.
 - e Set the Color Grade Display option to ON.
 - f Set up Mask Test settings.
 - g Set up Clock Recovery on SDA.
 - : Explicit clock, Source = Function 1, Rising Edge
 - h Set the Real Time Eye on SDA to ON.
 - *i* Set up measurement threshold values for Function 1 and CA input signals.
 - *j* Change Trigger Source to 'CA input signal' on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CA bus.
- 4 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - *b* Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 5 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to CA Rx Voltage and Timing tests > vCENT CA mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.
 - · Select a positive value greater than 0 to specify vCENT.

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.

7 Use the Histogram feature in the Infinitum Application to measure the tCIVW2 Margin value for all the four corners of the Test Mask. The tCIVW2 Margin for each Test Mask corner is denoted by tCIVW2_m1, tCIVW2_m2, tCIVW2_m3 and tCIVW2_m4.

- 8 Find the minimum value between tCIVW2_m1, tCIVW2_m2, tCIVW2_m3 and tCIVW2_m4. Use the minimum value as the worst time gap.
- 9 Calculate the margin (in percentage) using the equation:

Margin (%) = [(Worst_time_gap) / (Half of mask width)] x 100%

where, Worst_time_gap is the time gap between the mask and the eye at four corners m1, m2, m3, m4.

10 Report the worst time gap and margin percentage as test results.

Expected/ Observable Results:

f/ The measured tCIVW2 Margin value for the test signal indicates if there is a violation in the maskregion.

vCIVW Margin

Availability Condition: Table 280 Set Up tab options for availability of tests

Burst & Continuous	N/A	No	No	Yes	CK(Diff), CA			
est ID & References:		R5 Test References from JE		100				
	Symbol (in Specific	ation)	Test ID	Reference	from Specification			
	vCIVW		142003		Table 466			
Overview:	The purpose of	this test is to measu	re the minimum vCIVW I	Margin of th	e CA eye diagram generat			
Procedure:			alue based on selected s	speed grade	options in the Test			
	Application. 2 Check for va		CA input test signals by v	erifying its f	requency and amplitude			
	values.		, , ,	, ,				
		3 On the Oscilloscope:						
	a Set the Trigger to 'Auto-Sweep'.							
	 b Set the Sampling Rate of the Oscilloscope to the maximum value. c Set the Sampling Points to the user defined value configured for the 'Sampling Points (Pts) for 							
	c Set the Sampling Points to the user defined value configured for the 'Sampling Points Eye Diagram Tests Only' configuration option in the Configure tab of the Test Applica							
	, ,	ion 1 to duplicate th	0	0				
	e Set the C	olor Grade Display c	ption to ON.					
	f Set up Mask Test settings.							
	g Set up Cl	ock Recovery on SD.	Α.					
	: Explicit	clock, Source = Fund	ction 1, Rising Edge					
	h Set the R	eal Time Eye on SDA	A to ON.					
	i Set up m	easurement threshol	ld values for Function 1 a	and CA inpu	t signals.			
	, 0	00	input signal' on both Ris s activity on CA bus.	sing/Falling	Edges to prevent timeout			
	4 Perform Ma	sk Testing:						
	a Set the M	lask Test Run Until s	etting to 'Forever'.					
	b Load the	mask file and start t	he Mask Test.					
			counter for 'Total Wavef onfiguration option 'Total		ds the number of required			
	5 Determine a	and store the Vcent v	value. To determine the v	alue of Vcer	nt:			
	a In the Co	nfigure tab of the Te	st Application, choose N	lode as Deb	ug.			
			vigate to CA Rx Voltage : rtical center of the Eye N		tests > vCENT CA mode (\ ed.			
	 Select 'W 							

	То	obtain the vCENT value with 'WidestOpening' selected:
		i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
		ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
		iii Use the voltage level at the widest eye opening as the value for Vcent.
		position the Test Mask so that it is centered on the Vcent value with the Test Mask width and ght set in the Configure tab.
	top	e the Histogram feature in the Infiniium Application to measure the vCIVW Margin value for the and the bottom area of the Test Mask. e measured vCIVW margin is denoted as vCIVW Margin upper and vCIVW Margin lower.
		d the minimum value between vCIVW Margin Upper and vCIVW Margin lower. Use this value the worst voltage gap.
	9 Cal	culate the worst margin (in percentage) using the equation:
		Margin (%) = [(Worst_voltage_gap) / (Half of mask height)] x 100%
		ere, Worst_voltage_gap is the voltage gap between the mask and the eye at the top and tom.
	10 Rej	port the worst voltage gap and the margin percentage as test results.
Expected/ Observable Results:	The me region.	easured value of vCIVW Margin for the test signal indicates if there is a violation in the mask

tCIPW

Procedure:

Availability Condition:	Table 282	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CA

Test ID & References: Table 283 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
tCIPW	142004	Table 466

Overview: The purpose of this test is to verify the minimum input CA Rx pulse width defined at the Vcent_CA.

1 This test requires the following pre-requisite test:

• tCIVW1 Margin (Test ID: 142001) Location for Vcent is determined and its value is stored.

2	Perform the pulse width on the CA signal:
	a Set to ON the positive pulse width measurement and jitter statistics to measure all the edges.
	<i>b</i> Set the measurement threshold to a hysteresis of ± CA mask height at the threshold level of Vcent_CA.
	c Obtain the minimum result from the measurements as the worst positive pulse width.
	<i>d</i> Repeat steps a to c for negative pulse width and store the minimum result from the measurement as the worst negative pulse width.
3	Compare the minimum values from the positive and negative pulse width results.
4	Measure tDIPW as the time starting from a rising/falling edge of the CA signal to the time ending at the following falling/rising edge.
5	Capture all values of tCIPW.
6	Convert the unit for the values from seconds to UI.
7	Determine the worst result from the set of tCIPW values measured and report it as the final test result.

Expected/ The measured value of tCIPW for the test signal shall be within the conformance limit as per the JESD209-5C specification.

vCIHL_AC

Availability Condition: Table 284 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CA

Test ID & References: Table 285 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
vCIHL_AC	142005	Table 466

- **Overview:** The purpose of this test is to measure the CA single input pulse amplitude vCIHL_AC that the pulse must meet or exceed at any point over the total UI.
- **Procedure:** 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.
 - 2 Check for valid Clock (CK) and CA input test signals by verifying its frequency and amplitude values.
 - 3 Set up the oscilloscope:
 - a Set the Trigger to 'Auto-Sweep'.
 - b Set up measurement threshold values for the CAx channel and the CKx channel input.
 - c Set up fixed vertical scale values for CAx channel and CKx channel input.
 - *d* Set the Color Grade Display option to ON.
 - e Set up Mask Test.
 - f Set up Clock Recovery on SDA.

g Set the Real Time Eye on SDA to ON. 4 Perform Mask Testing: a Set the Mask Test Run Until setting to 'Forever'. b Load the mask file and start the Mask Test. c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'. 5 Determine and store the Vcent value. To determine the value of Vcent: a In the Configure tab of the Test Application, choose Mode as Debug. b Under Eye Diagram Tests, navigate to CA Rx Voltage and Timing tests > vCENT CA mode (V). This is the level, where the vertical center of the Eye Mask is placed. · Select 'WidestOpening' to use the widest eye opening as vCENT. Select a positive value greater than 0 to specify vCENT. To obtain the vCENT value with 'WidestOpening' selected: The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye i height measured at the center of the eye diagram). Scan for the widest eye opening at the mentioned search range with a scan resolution of ii 5mV. iii Use the voltage level at the widest eye opening as the value for Vcent. 6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab. 7 Use the Histogram feature in the Infiniium Application to measure the vCIHL_AC/2 values for the top and the bottom area of the Test Mask. The measured vCIHL_AC/2 values is denoted as vCIHL_AC/2_top and vCIHL_AC/2_bottom. 8 Calculate vCIHL_AC using the equation: vCIHL_AC = [vCIHL_AC/2_top] - [vCIHL_AC/2_bottom] 9 Report the measured vCIHL_AC as test result. Expected/ The measured value of vCIHL AC for the test signal shall be within the conformance limit as per the **Observable Results:** JESD209-5C specification. tCA2CA Availability Condition: Table 286 Set Up tab options for availability of tests Supported CK Type Supported WCK Type Supports Offline? **R/W Separation needed?** SE Mode? **Required Signals**

: Explicit clock, Source = filtered CK, Rise/Fall Edge

Test ID & References: Table 287 LPDDR5 Test References from JESD209-5C Specification

No

Symbol (in Specification)	Test ID	Reference from Specification
tCA2CA	142000	Table 466

No

Yes

CK(Diff), CA[x], CA[y]

Burst & Continuous

N/A

- **Overview:** The purpose of this test is to verify the mask offset between the fastest CA[x] mask center to the slowest CA[y] mask center.
- **Procedure:** 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.
 - 2 Check for valid Clock (CK), CA[x] and CA[y] input test signals by verifying its frequency and amplitude values.
 - 3 On the Oscilloscope:
 - a Set the Trigger to 'Auto-Sweep'.
 - *b* Set the Sampling Rate of the Oscilloscope to the maximum value.
 - c Set the Sampling Points to the user defined value configured for the 'Sampling Points (Pts) for Eye Diagram Tests Only' configuration option in the Configure tab of the Test Application.
 - *d* Enable CK, CA[x] and CA[y] source channels.
 - e Set the Color Grade Display option to ON.
 - f Set up Mask Test settings.
 - g Set up Clock Recovery on SDA.
 - : Explicit clock, Source = CK source channel, Rising Edge
 - h Set the Real Time Eye on SDA to ON.
 - i Set up measurement threshold values for CK, CA[x] & CA[y] input signals.
 - *j* Change Trigger Source to 'CA[x] input signal' and 'CA[y] input signal', respectively on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CA bus.
 - 4 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - b Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
 - 5 Determine and store the Vcent values for CA[x] and CA[y]. To determine the value of Vcent, perform the following steps for each CA[x] and CA[y] input signals:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to CA Rx Voltage and Timing tests > vCENT CA mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - Select 'WidestOpening' to use the widest eye opening as vCENT.
 - Select a positive value greater than 0 to specify vCENT.

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 6 From the 'WidestOpening' or 'user-defined' Vcent determined for CA[x] eye, find its midpoint. Denote this value as CA[x]_mid.
- 7 From the 'WidestOpening' or 'user-defined' Vcent determined for CA[y] eye, find its midpoint. Denote this value as CA[y]_mid.
- 8 Calculate tCA2CA using the equation:

 $tCA2CA = CA[x]_mid - CA[y]_mid$

9 Report this difference as tCA2CA.

Expected/ Observable Results: The measured value of tCA2CA shall be within the conformance limits as per the JESD209-5C specification.

tCA2CA_share

Availability Condition: Table 288 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	No	No	Yes	CK(Diff), CA[x], CA[y]

Test ID & References: Table 289 LPDDR5 Test References from JESD209-5C Specification

Overview: The purpose of this test is to verify the mask offset between dies which are in the same PKG and share same power supplies.

CA2CA_share_R

Procedure:	1	Calculate the initial time scale value based on selected speed grade options in the Test Application.
	2	Check for valid Clock (CK), CA[x] and CA[y] input test signals by verifying its frequency and amplitude values.
	3	On the Oscilloscope:
		a Set the Trigger to 'Auto-Sweep'.
		b Set the Sampling Rate of the Oscilloscope to the maximum value.
		c Set the Sampling Points to the user defined value configured for the 'Sampling Points (Pts) for

- Eye Diagram Tests Only' configuration option in the Configure tab of the Test Application.
- d Enable CK, CA[x] and CA[y] source channels.
- e Set the Color Grade Display option to ON.
- f Set up Mask Test settings.
- g Set up Clock Recovery on SDA.
- : Explicit clock, Source = CK source channel, Rising Edge
- h Set the Real Time Eye on SDA to ON.
- i Set up measurement threshold values for CK, CA[x] & CA[y] input signals.
- *j* Change Trigger Source to 'CA[x] input signal' and 'CA[y] input signal', respectively on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CA bus.
- 4 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - b Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

Prerequisite: The CA2CA_share_R and CA2CA_share_F measurements must be performed before determining the final value of tCA2CA_share.

- 5 Determine and store the Vcent values for CA[x] and CA[y]. To determine the value of Vcent, perform the following steps for each CA[x] and CA[y] input signals:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to CA Rx Voltage and Timing tests > vCENT CA mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.
 - Select a positive value greater than 0 to specify vCENT.
 - To obtain the vCENT value with 'WidestOpening' selected:
 - i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
 - ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
 - iii Use the voltage level at the widest eye opening as the value for Vcent.
- 6 From the 'WidestOpening' or 'user-defined' Vcent determined for CA[x] eye, find its midpoint. Denote this value as CA[x]_mid.
- 7 From the 'WidestOpening' or 'user-defined' Vcent determined for CA[y] eye, find its midpoint. Denote this value as CA[y]_mid.
- 8 Calculate CA2CA_share_R using the equation:

Sub-equation to apply	Condition
CA2CA_share_R = max(CA[x]_mid, CA[y]_mid)	if min(CA[x]_mid, CA[y]_mid) >= 0
CA2CA_share_R = Abs[max(CA[x]_mid, CA[y]_mid) - min(CA[x]_mid, CA[y]_mid)]	if max(CA[x]_mid, CA[y]_mid) >=0 and min(CA[x]_mid, CA[y]_mid) < 0
CA2CA_share_R = Abs[min(CA[x]_mid, CA[y]_mid)]	if max(CA[x]_mid, CA[y]_mid) < 0

CA2CA_share_F

- **Procedure:** 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.
 - 2 Check for valid Clock (CK), CA[x] and CA[y] input test signals by verifying its frequency and amplitude values.
 - 3 On the Oscilloscope:
 - a Set the Trigger to 'Auto-Sweep'.
 - *b* Set the Sampling Rate of the Oscilloscope to the maximum value.
 - *c* Set the Sampling Points to the user defined value configured for the 'Sampling Points (Pts) for Eye Diagram Tests Only' configuration option in the Configure tab of the Test Application.
 - *d* Enable CK, CA[x] and CA[y] source channels.
 - e Set the Color Grade Display option to ON.
 - f Set up Mask Test settings.
 - g Set up Clock Recovery on SDA.
 - : Explicit clock, Source = CK source channel, Falling Edge

- *h* Set the Real Time Eye on SDA to ON.
- *i* Set up measurement threshold values for CK, CA[x] & CA[y] input signals.
- *j* Change Trigger Source to 'CA[x] input signal' and 'CA[y] input signal', respectively on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CA bus.
- 4 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - b Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 5 Determine and store the Vcent values for CA[x] and CA[y]. To determine the value of Vcent, perform the following steps for each CA[x] and CA[y] input signals:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to CA Rx Voltage and Timing tests > vCENT CA mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.
 - · Select a positive value greater than 0 to specify vCENT.

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 6 From the 'WidestOpening' or 'user-defined' Vcent determined for CA[x] eye, find its midpoint. Denote this value as CA[x]_mid.
- 7 From the 'WidestOpening' or 'user-defined' Vcent determined for CA[y] eye, find its midpoint. Denote this value as CA[y]_mid.
- 8 Calculate CA2CA_share_F using the equation:

Sub-equation to apply	Condition
CA2CA_share_F = max(CA[x]_mid, CA[y]_mid)	if min(CA[x]_mid, CA[y]_mid) >= 0
CA2CA_share_F = Abs[max(CA[x]_mid, CA[y]_mid) - min(CA[x]_mid, CA[y]_mid)]	if max(CA[x]_mid, CA[y]_mid) >=0 and min(CA[x]_mid, CA[y]_mid) < 0
CA2CA_share_F = Abs[min(CA[x]_mid, CA[y]_mid)]	if max(CA[x]_mid, CA[y]_mid) < 0

tCA2CA_share

Procedure: The tCA2CA_share is defined by the below equation.

tCA2CA_share= max(CA2CA_share_R , CA2CA_share_F)

This means that the higher of the two values, CA2CA_share_R or CA2CA_share_F, will be the value of the tCA2CA_share test result.

Expected/ The measured value of tCA2CA_share shall be within the conformance limits as per the JESD209-5C **Observable Results:** specification.

References for CS Rx Voltage and Timing tests

LPDDR5 CS Rx mask for Synchronous mode is defined as hexagonal mask shape as shown in Figure 109. CS signals apply the same compliance mask and operate in single data rate mode. The receiver mask (Rx Mask vCSIVW, tCSIVW1, tCSIVW2) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal.

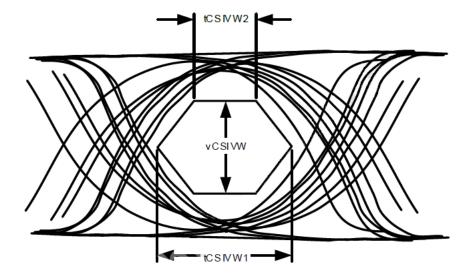


Figure 109 CS Rx Mask definition

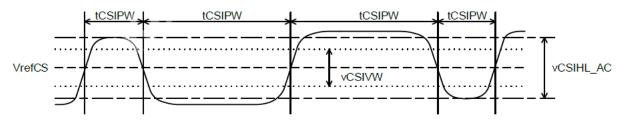


Figure 110 Identifying CS Rx Mask parameters with respect to VrefCS

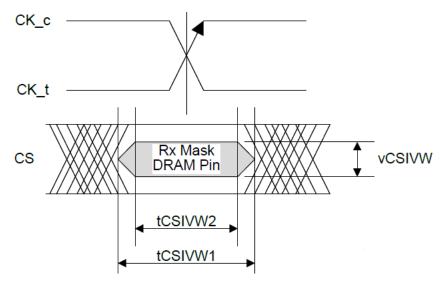


Figure 111 Identifying CS Rx Mask parameters with respect to CK

CS Rx Voltage and Timing tests

tCSIVW1 Margin

Availability Condition: Table 290 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CS
Test ID & References:	Table 291 LPDDR	5 Test References from JI	SD209-5C Specification		
	Symbol (in Specific	ation)	Test ID	Reference	from Specification
	tCSIVW1		142020		Table 465
Overview:	The purpose of t generated.	his test is to measu	ire the minimum tCSIVW	/1 Margin of	the CS eye diagram
Procedure:	 Application. Check for vavalues. On the Oscila Set the Tribic Set the Sacconstruction Set the Sacconstruction Set the Sacconstruction Set the Construction Set up Margon Set up Classing Set up Classing Explicit on 	lid Clock (CK) and (oscope: igger to 'Auto-Swea ampling Rate of the ampling Points to the am Tests Only' conf ion 1 to duplicate the olor Grade Display of usk Test settings.	ep'. Oscilloscope to the max ne user defined value con iguration option in the C ne CK signal. option to ON. MA. ction 1, Rising Edge	verifying its f imum value. ifigured for t	requency and amplitude he 'Sampling Points (Pts) for
	 j Change Tisuch case 4 Perform Mas a Set the M b Load the c Stop the N waveform 5 Determine a 	igger Source to 'CS s, when there is les k Testing: ask Test Run Until s nask file and start to Mask Test when the s specified in the co nd store the Vcent	s activity on CS bus. setting to 'Forever'. the Mask Test.	sing/Falling forms' excee Waveform'. value of Vcer	Edges to prevent timeout for ds the number of required nt:
			vigate to CS Rx Voltage a ertical center of the Eye N		tests > vCENT CS mode (V). ed.

- · Select 'WidestOpening' to use the widest eye opening as vCENT.
- · Select a positive value greater than 0 to specify vCENT.

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
- 7 Use the Histogram feature in the Infiniium Application to measure the tCSIVW1 Margin value for both corners of the Test Mask.

The tCSIVW1 Margin for each Test Mask corner is denoted by tCSIVW1_m1 and tCSIVW1_m2.

- 8 Find the minimum value between tCSIVW1_m1 and tCSIVW1_m2. Use the minimum value as the worst time gap.
- 9 Calculate the margin (in percentage) using the equation:

Margin (%) = [(Worst_time_gap) / (Half of mask width)] x 100%

- where, Worst_time_gap is the time gap between the mask and the eye at corners m1 and m2.
- 10 Report the worst time gap and margin percentage as test results.

Expected/ The measured tCSIVW1 Margin value for the test signal indicates if there is a violation in the mask region.

tCSIVW2 Margin

Availability Condition: Table 292 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CS

Test ID & References: Table 293 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
tCSIVW2	142021	Table 465

Overview: The purpose of this test is to measure the minimum tCSIVW2 Margin of the CS eye diagram generated.

Procedure: 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid Clock (CK) and CS input test signals by verifying its frequency and amplitude values.

- 3 On the Oscilloscope:
 - a Set the Trigger to 'Auto-Sweep'.
 - *b* Set the Sampling Rate of the Oscilloscope to the maximum value.
 - c Set the Sampling Points to the user defined value configured for the 'Sampling Points (Pts) for Eye Diagram Tests Only' configuration option in the Configure tab of the Test Application.
 - *d* Set Function 1 to duplicate the CK signal.
 - e Set the Color Grade Display option to ON.
 - f Set up Mask Test settings.
 - g Set up Clock Recovery on SDA.
 - : Explicit clock, Source = Function 1, Rising Edge
 - h Set the Real Time Eye on SDA to ON.
 - i Set up measurement threshold values for Function 1 and CS input signals.
 - *j* Change Trigger Source to 'CS input signal' on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CS bus.
- 4 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - *b* Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 5 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to CS Rx Voltage and Timing tests > vCENT CS mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.
 - Select a positive value greater than 0 to specify vCENT.

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.

7 Use the Histogram feature in the Infiniium Application to measure the tCSIVW2 Margin value for all the four corners of the Test Mask. The tCSIVW2 Margin for each Test Mask corner is denoted by tCSIVW2_m1, tCSIVW2_m2, tCSIVW2_m3 and tCSIVW2_m4.

- 8 Find the minimum value between tCSIVW2_m1, tCSIVW2_m2, tCSIVW2_m3 and tCSIVW2_m4. Use the minimum value as the worst time gap.
- 9 Calculate the margin (in percentage) using the equation:

Margin (%) = [(Worst_time_gap) / (Half of mask width)] x 100%

where, Worst_time_gap is the time gap between the mask and the eye at four corners m1, m2, m3, m4.

10 Report the worst time gap and margin percentage as test results.

Expected/ The measured tCSIVW2 Margin value for the test signal indicates if there is a violation in the mask region.

vCSIVW Margin

Availability Condition: Table 294 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type S	upports Offline? R/W Separation	n needed? SE Mode? Required Signals
Burst & Continuous	N/A N	o No	Yes CK(Diff), CS
Test ID & References:	Table 295 LPDDR5 Test	References from JESD209-5C Specificati	tion
	Symbol (in Specification)	Test ID	Reference from Specification
	vCSIVW	142022	Table 465
Overview:	The purpose of this te generated.	est is to measure the minimum	n vCSIVW Margin of the CS eye diagram
Procedure:	 Application. Check for valid Clivalues. On the Oscillosco a Set the Trigger b Set the Sampli c Set the Sampli Eye Diagram Te d Set Function 1 e Set the Color Of f Set up Mask Te g Set up Clock R Explicit clock, h Set the Real Ti i Set up measure j Change Trigger such cases, wh 4 Perform Mask Tes a Set the Mask T b Load the mask c Stop the Mask waveforms spe Determine and st a In the Configur b Under Eye Diag This is the leve Select 'Widestte 	ock (CK) and CS input test sign pe: to 'Auto-Sweep'. ng Rate of the Oscilloscope to ng Points to the user defined vi- ests Only' configuration option to duplicate the CK signal. Grade Display option to ON. est settings. ecovery on SDA. Source = Function 1, Rising Ed me Eye on SDA to ON. ement threshold values for Fun r Source to 'CS input signal' on the there is less activity on CS I sting: test Run Until setting to 'Forever file and start the Mask Test. Test when the counter for 'Tota cified in the configuration optio ore the Vcent value. To determ te tab of the Test Application, c	value configured for the 'Sampling Points (Pts) for in the Configure tab of the Test Application. Edge inction 1 and CS input signals. In both Rising/Falling Edges to prevent timeout for bus. er'. er'. al Waveforms' exceeds the number of required ion 'Total Waveform'. nine the value of Vcent: choose Mode as Debug. Voltage and Timing tests > vCENT CS mode (V). the Eye Mask is placed. e opening as vCENT.

	To obtain the vCENT value with 'WidestOpening' selected:
	i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
	ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
	iii Use the voltage level at the widest eye opening as the value for Vcent.
	6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
	7 Use the Histogram feature in the Infiniium Application to measure the vCSIVW Margin value for the top and the bottom area of the Test Mask. The measured vCIVW margin is denoted as vCSIVW Margin upper and vCSIVW Margin lower.
	8 Find the minimum value between vCSIVW Margin Upper and vCSIVW Margin lower. Use this value as the worst voltage gap.
	9 Calculate the worst margin (in percentage) using the equation:
	Margin (%) = [(Worst_voltage_gap) / (Half of mask height)] x 100%
	where, Worst_voltage_gap is the voltage gap between the mask and the eye at the top and bottom.
	10 Report the worst voltage gap and the margin percentage as test results.
Expected/ Observable Results:	The measured value of vCSIVW Margin for the test signal indicates if there is a violation in the mask region.

tCSIPW

Availability Condition:	Table 296	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CS

Test ID & References: Table 297 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
tCSIPW	142023	Table 465

Overview: The purpose of this test is to verify the minimum input CS Rx pulse width defined at the Vcent_CS.

Procedure:

- 1 This test requires the following pre-requisite test:
- tCIVW1 Margin (Test ID: 142020) Location for Vcent is determined and its value is stored.

	 2 Perform the pulse width on the CS signal: a Set to ON the positive pulse width measurement and jitter statistics to measure all the edges. b Set the measurement threshold to a hysteresis of ±CS mask height at the threshold level of Vcent_CS. c Obtain the minimum result from the measurements as the worst positive pulse width.
	d Repeat steps a to c for negative pulse width and store the minimum result from the measurement as the worst negative pulse width.
	3 Compare the minimum values from the positive and negative pulse width results.
	4 Measure tDIPW as the time starting from a rising/falling edge of the CS signal to the time ending at the following falling/rising edge.
	5 Capture all values of tCSIPW.
	6 Convert the unit for the values from seconds to UI.
	7 Determine the worst result from the set of tCSIPW values measured and report it as the final test result.
Expected/ Observable Results:	The measured value of tCSIPW for the test signal shall be within the conformance limit as per the JESD209-5C specification.

vCSIHL_AC

Availability Condition: Table 298 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CS

Test ID & References: Table 299 LPDDR5 Test References from JESD209-5C Specification

Symbol (in Specification)	Test ID	Reference from Specification
vCSIHL_AC	142024	Table 465

Overview: The purpose of this test is to measure the CS single input pulse amplitude vCSIHL_AC that the pulse must meet or exceed at any point over the total UI.

- **Procedure:** 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.
 - 2 Check for valid Clock (CK) and CS input test signals by verifying its frequency and amplitude values.
 - 3 Set up the oscilloscope:
 - a Set the Trigger to 'Auto-Sweep'.
 - b Set up measurement threshold values for the CSx channel and the CKx channel input.
 - c Set up fixed vertical scale values for CSx channel and CKx channel input.
 - *d* Set the Color Grade Display option to ON.
 - e Set up Mask Test.
 - f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered CK, Rise/Fall Edge

- g Set the Real Time Eye on SDA to ON.
- 4 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - *b* Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 5 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to CS Rx Voltage and Timing tests > vCENT CS mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.
 - Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
- 7 Use the Histogram feature in the Infinitum Application to measure the vCSIHL_AC/2 values for the top and the bottom area of the Test Mask.

The measured vCSIHL_AC/2 values is denoted as vCSIHL_AC/2_top and vCSIHL_AC/2_bottom.

8 Calculate vCSIHL_AC using the equation:

vCSIHL_AC = [vCSIHL_AC/2_top] - [vCSIHL_AC/2_bottom]

9 Report the measured vCSIHL_AC as test result.

Expected/ The measured value of vCSIHL_AC for the test signal shall be within the conformance limit as per the JESD209-5C specification.

Eye Diagram for CA

Availability Condition:	Table 300 Set Up	tab options for availability	of tests		
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst & Continuous	Yes	No	Yes	DQ, CA
Test ID & References:	st ID & References: Table 301 LPDDR5 Test References from JESD209-5C Specification				
	Symbol (in Specifica	Symbol (in Specification)		Reference from Specification	
	NA (Information-Only	r test)	142007	1	NA (Information-Only test)

Overview:	ge Th	e purpose of this test is to automate all the required setup procedures required in order to enerate an eye diagram for the Command Address signal. In additional feature of having a mask test is that it allows users to perform evaluations and obugging on the eye diagram created.
Procedure:	1	Acquire the Clock and CommandAddress signal.
	2	Load acquired CommandAddress signal into WMemory4. Then use Function4 as "Magnify/Duplicate" of Loaded Waveform Memory.
	3	Load Clock signal into WMemory1. Then use Function1 as "Magnify/Duplicate" of Loaded Waveform Memory.
	4	Setup Clock Recovery settings on SDA.
		 Explicit clock, Source = Clock, Rise/Fall Edge
	5	Setup measurement threshold values for the Function4(CommandAddress) and the Function1(Clock).
	6	Setup fix time scale and time position values for Function4(CommandAddress) and Function1(Clock).
	7	Turn ON Color Grade Display option.
	8	Identify the X1 value for re-adjustment of selected test mask.
	9	Setup Mask Test settings.
	10) Turn ON Real Time Eye on SDA.
	11	Start mask test until eye diagram folded.
	12	Return total failed UnitInterval as a test result.
Expected/	Th	e measured value of Eye Diagram for CA for the test signal is considered for 'Information-On

Expected/The measured value of Eye Diagram for CA for the test signal is considered for 'Information-Only'Observable Results:purpose.



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