

Agilent M9252A DigRF host adapter

SW Version 1.05.0017

Oct 2, 2014

- Software Version 1.05.0017
- Internal Build 1.05.0017.0149
- V6 FPGA Version 04.23
- K7 FPGA Versions 06.32, 100.18 (Frame Capture) , 200.3 (Enhanced IQ Capture)
- Package GUID 4FE4E4C5-2F79-48F4-93EB-F7E37AE2E24F

Overview

The M9252A DigRF Host Adapter module belongs to the Agilent RDX family. The module provides the serial stimulus capabilities required for DigRF v4 based RFIC evaluation and characterization. A single module combines stimulus and Rx side capture capabilities to generate configurable control and data traffic and observe the response from the device under test (DUT). It allows engineers to work in the domain (digital or RF) of their choice to quickly characterize the DUT's digital and wireless behavior.

For more information on M9252A, please visit www.agilent.com/find/M9252A.

Current OSes supported

Windows XP 32, Windows 7 32/64

Installation Steps

- Please remove any previous installed version of M9252A from control panel before installing current version.
- Install “Agilent M9252A DigRFHostAdapter 1.05.xxxx Build xx-xxx-xx.exe”

Important usage notes.

- SUS license must be installed to use this software build.
- User needs to install Advanced Feature License to use the enhanced IQ capture & Frame Capture mode
- Programming of V6 image
 - Run application “C:\Program Files (x86)\Agilent\M9252A\Bin\ AcqEepromProg.exe”
 - Select FPGA “C:\Program Files (x86)\Agilent \M9252A\FPGA\ M9252A_v6.vme”
 - Restart Chassis then Host Controller PC

Known Limitations / Issues

- Cannot upload & configure IQ data while Tx or Rx is running.
- Bi-Link mode
 - Clock and Line Rate should be same for both links
 - Cannot upload & configure IQ data when Tx or Rx is running on any link
- Speed of VSA data push when working with 2 link might be very slow(VSA performance issue)
- Send Immediate Configuration
 - Jump should always be preceded and followed by Control Frames. Jump cannot be first instruction. If you have nothing add Dummy frame as many as you like.
 - The timing of Jump should be a non-zero value.(Due to unpredictable nature of the FIFO , it's advisable to give a delay of 100,000 SI and the Maximum worst condition is 300,000 SI)
- There have some issues observed at some PC's during the upload of the Iq/DigRF frames. To overcome the upload issues the PCIe burst size needs to be reduced. To do so the user needs to set some additional settings in the registry located at either [HKEY_LOCAL_MACHINE\SOFTWARE\Wow6432Node\Agilent\M9252A] or [HKEY_LOCAL_MACHINE\SOFTWARE\Agilent\M9252A]
 - "DebugDDRReadSize"=dword:00004000
 - "DebugConfig"=dword:4DebugDDRReadSize ranges from 0x1000 to 0x100000, default is 0x100000
- Frame Capture Mode
 - Tx should be in stopped state during Rx Stop & Captured frames upload

Software Revision History

SW Version 1.05.0017

- VSA Data Push support using M9252A.exe (VSA License issue fixed)
- SUS & Advanced Features Licensing support added
 - User needs to install SUS License to use this build
- Enhanced Single Link IQ Capture mode & Frame Capture mode added
 - New type added EDIGRFModuleType:: AGT_DIGRF_MODULETYPE_LINK1_EX_IQ
 - InitModuleEx API added for selecting module type for 3 modes of operation
 - User needs to install Advanced Feature License to use the modes
- Variable length IQ payload support (CUSTOM waveform type)
- Capability to capture frames
- Capability to store Timestamps of each captured frame
- Time correlation of TX and RX DigRF frames
- Support for programming DigRF frames with Timestamps
- CLC Looping of DigRF frames
- DLC Looping of DigRF frames
- Discontinuous transmission support

- Bug Fixes
 - WIT# 346151: Enhanced IQ mode and single IQ mode do not capture reliably for incoming frames with link error
 - WIT# 336325: Capture issue with sys-burst mode
 - WIT# 347414: LTE 15 unstability in phoenix release 1.01.0011
 - WIT# 340810: Software build information mismatch between GUI and TCL window
 - WIT# 338962: Sample frequency list are not greyed out in GUI for GSM/EDGE_RX
 - WIT# 350218: AddDLCInstructionloop API issue
 - WIT# 344904: gear 1 and gear 2 speed only 1 lane shows in GUI in enhanced IQ capture mode
 - WIT# 329498: EI do not update while exporting captured frames to file
 - WIT# 336325: Capture issue with sys-burst mode
 - WIT # 328520 : Connection issue with VSA production license
 - WIT # 328862 : Phoenix doesn't work with signal studio MEU waveforms
 - WIT # 322869 : PHX crash during IQ file upload for long duration in loop
 - WIT # 323330 : Unusual behavior for burst size 0/1
 - WIT # 323333 : SOF Disparity reset after every burst
 - WIT # 326433 : With customized customer CLC payload Tx status remain running even after transmitting all frames
 - WIT # 199253 : Tx issue while playing using .wfm file
 - WIT #201387 : M9252A doesn't enter STALL mode in case of gap in transmission
 - WIT #200537 : Transmission in continuous mode not working
 - WIT # 200103 : Wrong Spectrum displayed in VSA while using "Push to VSA
 - WIT # 196510 : Tcl shell crashed on using Getframe API
 - WIT # 196510 : Tcl shell crashed on using Getframe API
 - WIT # 201731 : IQ data gets corrupted during multiple capture
 - WIT # 213081: PHX 1.0 DLC frame distance issue
 - WIT # 214259 : Issue in CLC Tx configuration for BiLink
 - WIT # 209798: Unreliable/No capture in case of error in incoming frames
 - WIT # 214964: M9252A support with Ericsson Ruby script Environment(tcl85 support)
 - WIT # 215444: Tcl crash issue related to loading wfm IQ file
 - WIT # 214962: Performance issue while pushing to VSA
 - WIT # 199253 : Tx issue while playing using .wfm file
 - WIT # 201387 : M9252A doesn't enter STALL mode in case of gap in transmission

- New APIs (Refer API Help M9252A_API_HELP.CHM)
 - InitModuleEx API added for selecting module type for 3 modes of operation
 - FrameUpload: GetCapturedFrames, ExportCapturedFramesToFile
 - IQConfiguration: AddDLCInstructionLoop

- CLCConfiguration : AddWaitFrame
- PLL Locked status 'AGT_DIGRF_STAT_PLL_LOCKED' added in the 'GetStatus' API.