Keysight N5990A-366/367 MIPI M-PHY Frame Generator Software

Getting Started Guide

KEYSIGHT TECHNOLOGIES

Notices

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1 Overview

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Document History

First Edition (June, 2017)

The first edition of this user guide describes functionality of software version 2.50

Second Edition (August, 2020)

The second edition of this user guide describes functionality of software version 4.20.

MIPI M-PHY Frame Generator Overview

The MIPI (Mobile Industry Processor Interface) M-PHY Frame Generator software (for short “Frame Generator” or “software”) is a stand-alone software utility. It provides semi-automatic control of Keysight Technologies M8020A J-BERT (Jitter Bit Error Ratio Tester) based MIPI M-PHY generator hardware for physical layer tests. For UniPro and UFS testing the BERT equipment can be combined with the BIT-3000 DSGA to put the DUT into UniPro Test Mode and retrieve the Frame and Error Counters.

The Frame Generator is a flexible tool for trouble-shooting and debugging. It complements the full Test Automation Software, which provides automated physical layer compliance tests and device characterization. It generates the data sequences and allows pattern changes as well as the control of signal levels, data rate, and timing parameters.

The software runs on a standard Windows PC and controls the hardware test resources through appropriate interfaces such as LAN (Local Area Network).

2 Software Installation and Update

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If the software is already installed on the PC and does not require any updates, proceed to the next chapter Starting and Registering the Software.

Software Installation

The MIPI M-PHY Frame Generator software runs on a standard PC, which is used to control the test instruments. The supported operating systems and required software that has to be installed before installation of the MIPI M-PHY Frame Generator are given in the following subsections.

Supported Operating Systems

The MIPI M-PHY Frame Generator software is supported by the following operating systems:

- OS Windows® 10, 64-Bits, English version

Software Requirements

Install the following software in the order given:

- Current Keysight IO libraries
- Microsoft .NET Framework version 4.7.1 or higher

Once the software requirements are met, the MIPI M-PHY Frame Generator software installer file can be executed, see Figure 1.

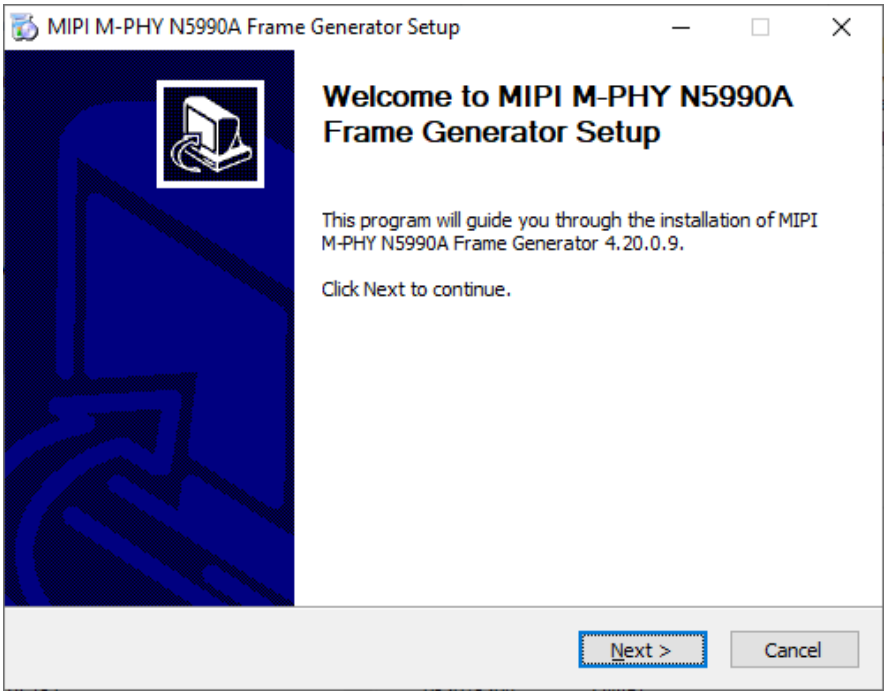

Figure 1 Installer Wizard

The second page of the installer wizard will show the software license agreement (see Figure 2). Read it carefully and select "**I accept the terms of the License Agreement**" option. Then, after the "**Next**" button has been pressed, the install location window is displayed as shown in Figure 3. Click the "**Browse...**" button to select the destination folder, in which the software is to be installed. Next, click the "**Install**" button to install the software.

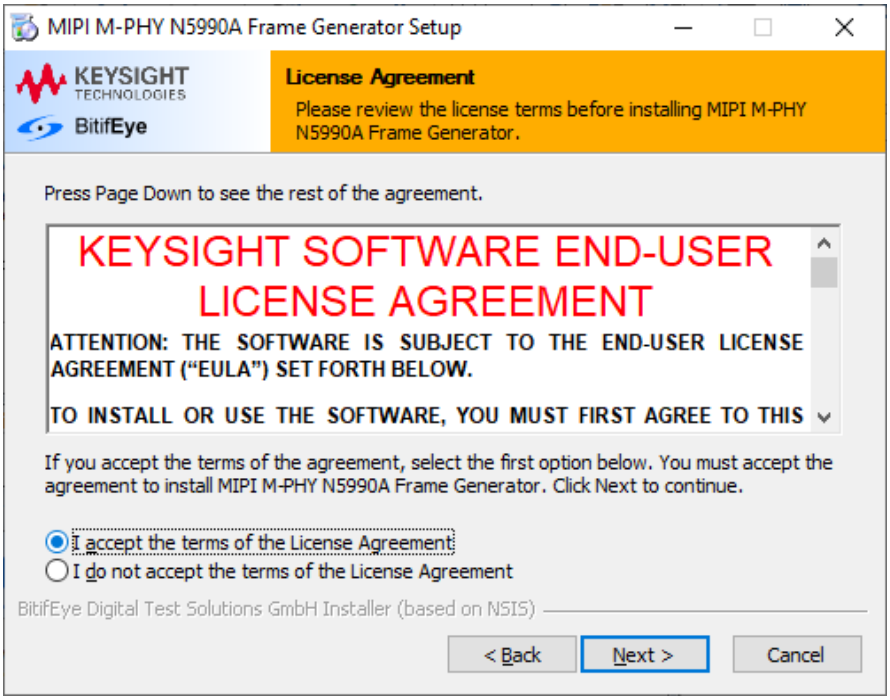

Figure 2 License Agreement Window

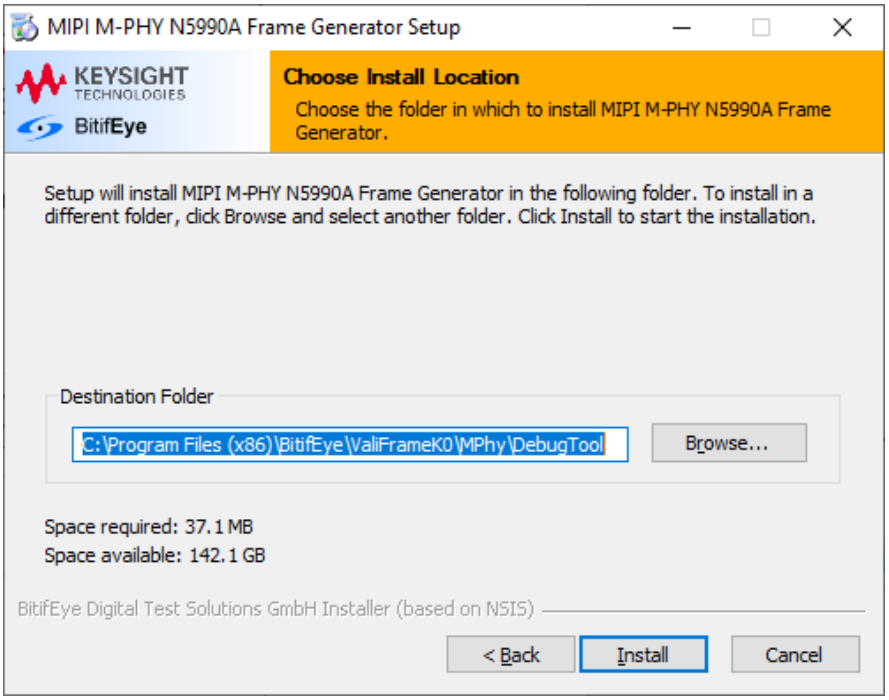

Figure 3 Install Location Window

After the installation the computer does not need to be rebooted. An icon named "**MIPI M-PHY Frame Generator**" will be added to the desktop as shown in Figure 4.

Figure 4 MIPI M-PHY Frame Generator Icon

Software Update

If the MIPI M-PHY Frame Generator software needs to be upgraded, first uninstall the existing version from the PC. The software can be uninstalled from the **Star Menu > All Programs > Bitifeye M-PHY N5990A > M-PHY Frame Generator (N5990A)**. Once the software uninstall is completed, reinstall the software, for installation steps, please see the section Software Installation.

3 Starting and Registering the Software

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After the software has been installed, an icon is added to the desktop as shown in Figure 4. Start the software with a double-click of the left mouse button. Alternatively, start the application from "**All Programs** > **BitifEye** > **M-PHY Frame Generator**".

Starting Unregistered Software

Starting the software without a valid license key opens a dialog box as shown in Figure 5.

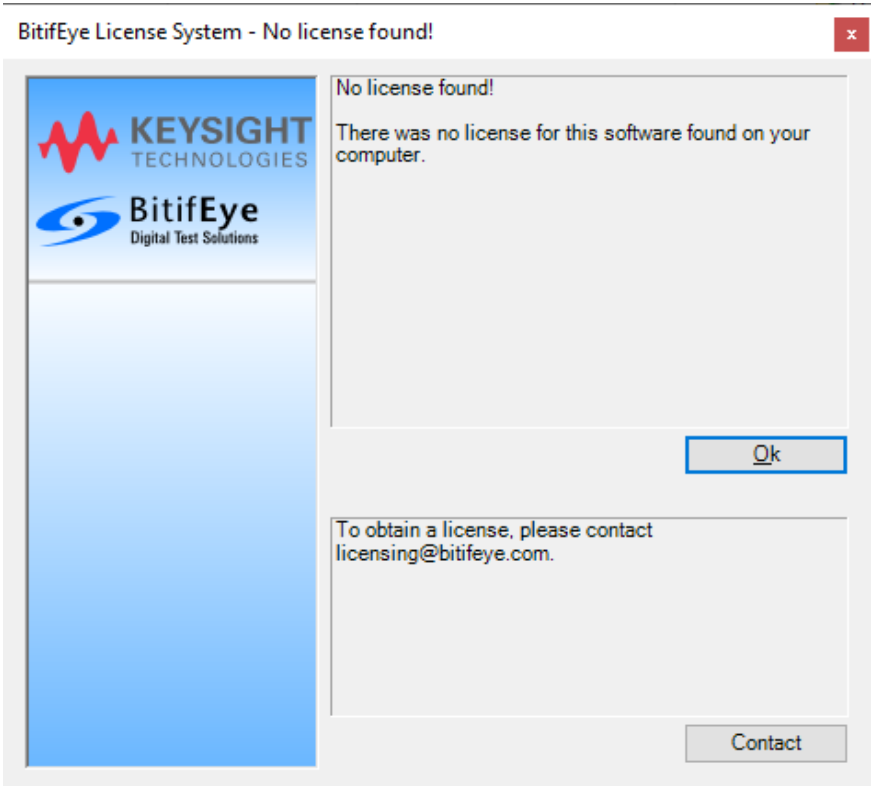

Figure 5 License Start-up Dialog Window

To get a valid license, use the BitifEye License Manage (BLM) portal: https://licensing.bitifeye.com/. With the certification number you can add the license to your PC and activate it.

For detailed instructions on how to use the BLM, please refer to the manual “BitifEye License Manager User Guide”.

Starting Registered Software

If the software is already registered, it starts automatically. Proceed to the chapter Test Instrument Setup, and then to the chapter Using the Software.

4 Test Instrument Setup

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J-BERT M8020A MIPI M-PHY Generator

To use this setup, select “M8020A” configuration (see Figure 6) and leave the “**Separate Low Speed Generator (DSGA)**” option unchecked in the **Instrument Connection** dialog (see Connecting to the Instruments).

This system configuration only requires the M8020A. The instrument works as generator and as Error Detector if necessary.

It supports the Loopback and Unipro operation modes. For UniPro Test Mode, the M8020A Error Detector requires that the DUT responses are sent in HS Continuous Mode, meaning with FILLER symbols in between the counter values.

Furthermore, for the training pattern generation memory restrictions apply, as described below under “**M8020A + DSGA**”.

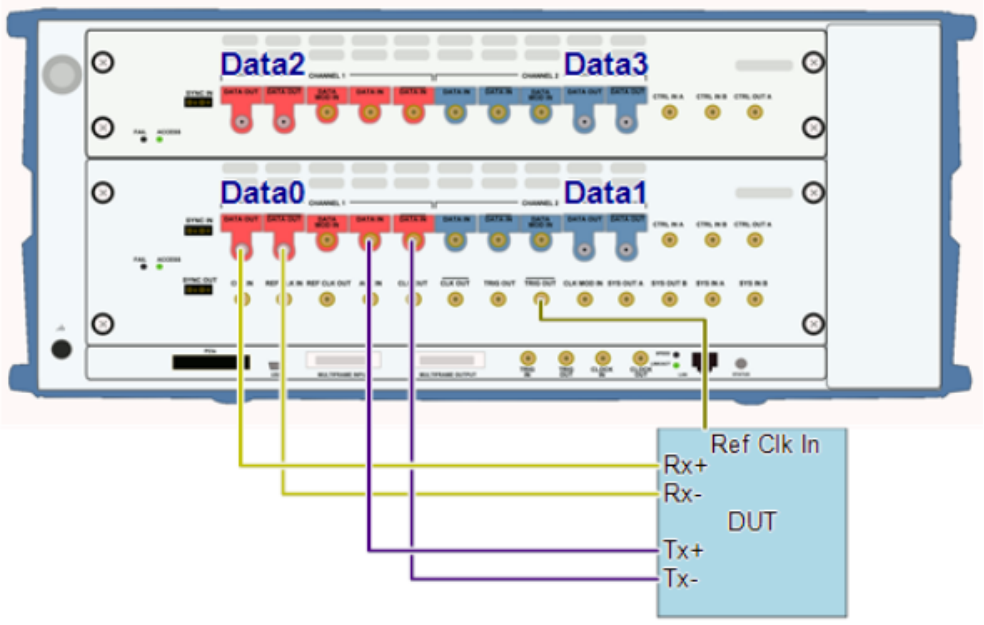

Figure 6 MIPI-PHY Frame Generator Hardware Setup for J-BERT M8020A

For all system configurations, the setup can include optionally TTCs (Transition Time Converters). The value of the TTC depends on the Gear used:

- 250 ps for Gear 1
- 120 ps for Gear 2
- 33 ps for Gear 3

J-BERT M8020A + DSGA MIPI M-PHY Generator

To use this setup, select “M8020A” configuration (see Figure 7) and check the “**Separate Low Speed Generator (DSGA)**” option in the **Instrument Connection** dialog (see Connecting to the Instruments).

This system configuration is recommended for the UniPro test mode. In this case the DSGA is used for the DUT configuration and to receive the frame and error counters, while the M8020A is used to generate the test pattern as well as the frame and error counter requests. If DUT configuration must happen in the same lane that will be tested, it is mandatory to use two switches to alternate the DUT inputs between the two generators.

The advantage of M8020A + DSGA setup with respect to the standalone M8020A comes from the much lower DSGA data rate. Since PWM data with M8020A is generated by bit multiplication, and depending on the test conditions the M8020A can be running at 9,984 Gbps, the generation of the training sequence will take much longer than with the DSGA, and the pattern may not even fit into the M8020A instrument's memory.

The DSGA Error Detector requires that the DUT responses come in PWM Mode, either Bursted or Continuous.

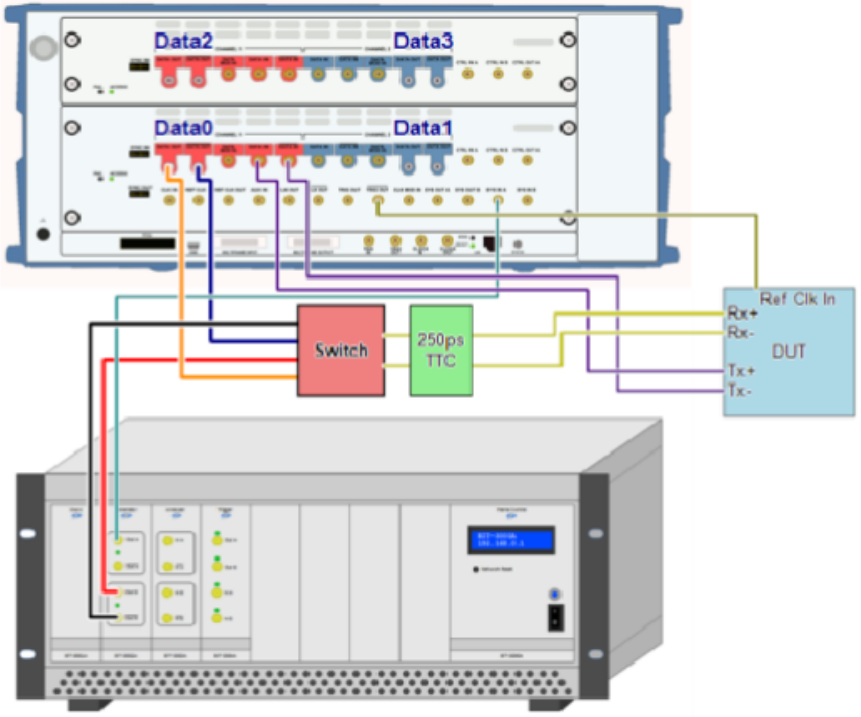

Figure 7 MIPI-PHY Frame Generator Hardware Setup for J-BERT M8020A + DSGA

DSGA MIPI M-PHY Generator

To use this setup, select "**BitifEye DSGA**" configuration (see Figure 8) option in the **Instrument Connection** dialog (see Connecting to the Instruments).

The DSGA (Bit3000) can be used standalone to generate the PWM and SYS signal.

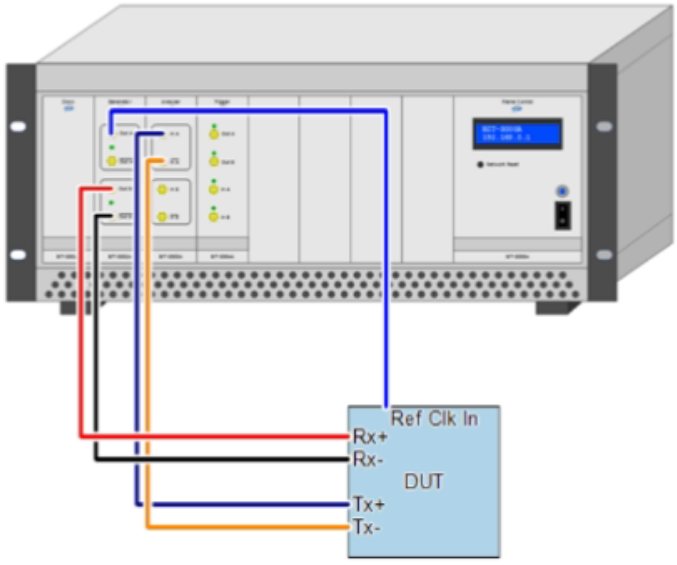

Figure 8 MIPI-PHY Frame Generator Hardware Setup for DSGA

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Connecting to the Instruments

Once the test instrument setup is finished, start the MIPI M-PHY Frame Generator software. The **Frame Generator** main window appears as shown in Figure 9.

Press the "**Connect...**" button to connect to the instruments the Connection dialog window appears as shown in Figure 10.

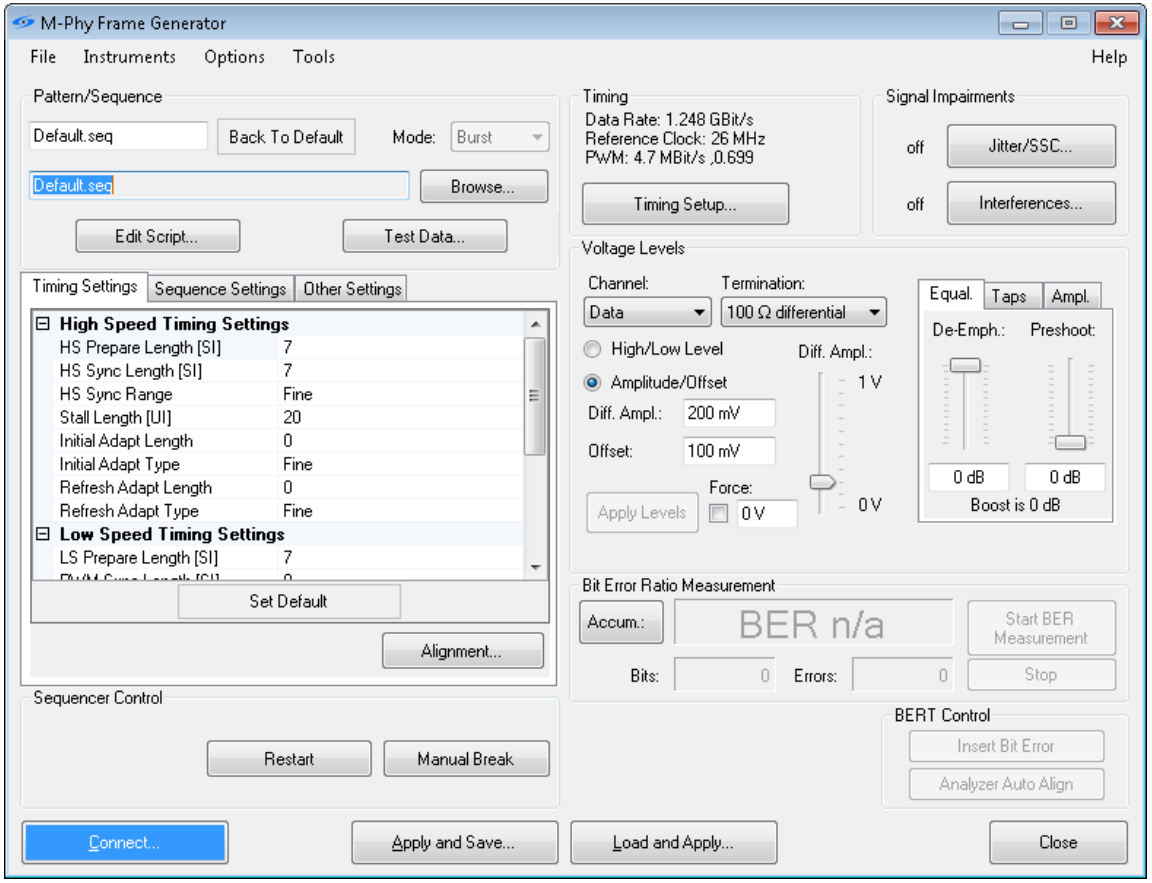

Figure 9 Frame Generator Main Window (instruments disconnected)

In the **Instrument Connection** dialog window:

1 Select the BERT configuration such as:

a J-BERT M8020A

b BitifEye DSGA

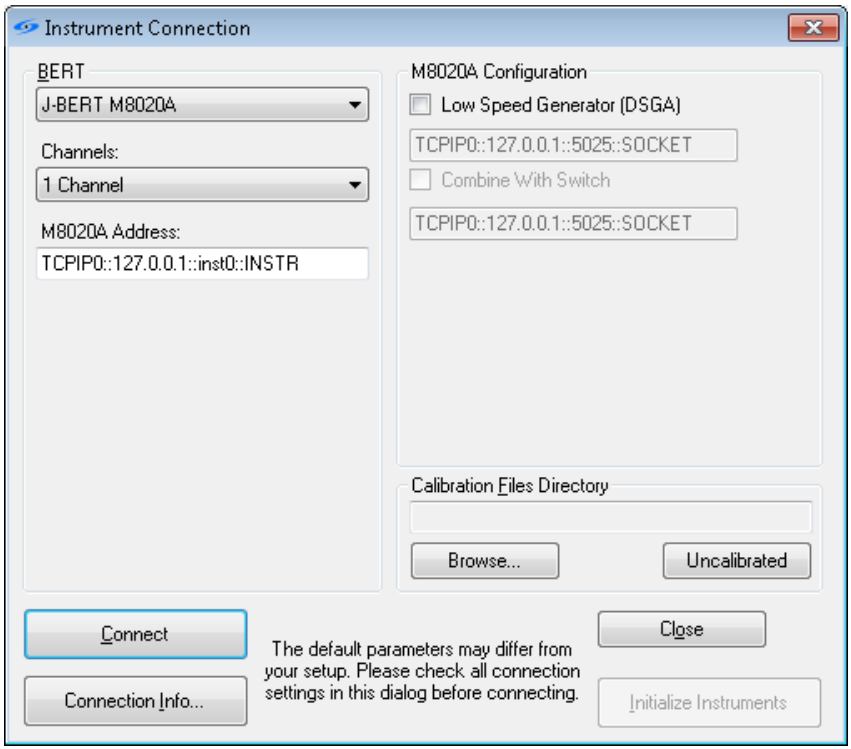

Figure 10 Instrument Connection Window (BERT selection)

Then select the BERT configuration details, (see Figure 10):

- Select the number of data channels.
- Specify the connection string, which is shown by the Keysight VISA IO Connection Expert Software.

2 The "**Auxiliary Instruments**" vary depending on the selected BERT configuration system (see Figure 11):

If M8020A BERT is selected as BERT configuration:

- The M8020A J-BERT instrument can be used either stand-alone or in combination with the DSGA. Select the "**Use Separate Low Speed Generator**" option to add the DSGA to the system configuration. Refer to J-BERT M8020A + DSGA MIPI M-PHY Generator in the previous section for more details about this setup.

  If this option is selected, introduce the DSGA address.

- This setup can be combined with a Matrix Switch that allows to connect several lanes at the same time. That will reduce the number of connection setup changes. If selected, the Switch address must be specified.

The Bitifeye DSGA configuration does not require additional instruments.

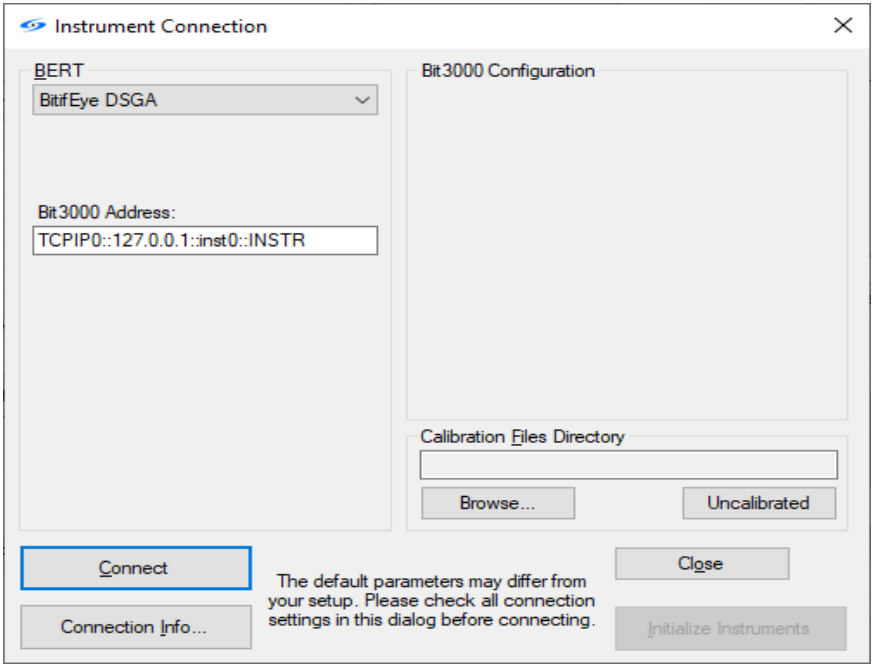

Figure 11 Instrument Connection Dialog (BitifEye DSGA selection)

3 Pressing on the "**Connection Info**" button, enables the connection set-up for the selected BERT configuration.

4 If the calibration files are available, load the files using the "**Browse...**" button from the directory where the calibration files exist.

5 Press the "**Connect**" button to connect the Instrument (M8020A or DSGA).

6 Once the instruments are connected successfully, the "**Initialize Instruments**" button is then enabled. Pressing the "**Initialize Instruments**" button applies the default configuration to the instrument(s).

7 The "**Close**" button closes the "**Instrument Connection**" dialog window without applying any settings.

8 8. Clicking on the "**Initialize Instruments**" button displays the Frame Generator main window as shown in Figure 12.

Frame Generator Main Window

It comprises seven sections for selecting HS and LP MIPI M-PHY signal parameters (see Figure 12):

1 Pattern/Sequence
2 Timing/Sequence/Other Settings
3 Timing
4 Signal Impairment
5 Voltage Levels
6 Bit Error Rate Measurement
7 BERT Control
8 Sequencer Control

Configure the MIPI M-PHY Frame Generator software by selecting the data sequence file, the desired pattern, HS data rate and pulse width modulation (PWM) parameters (for MIPI Type I modules, which use the PWM mode as the low speed mode) and HS gear speed in the Frame Generator main window.

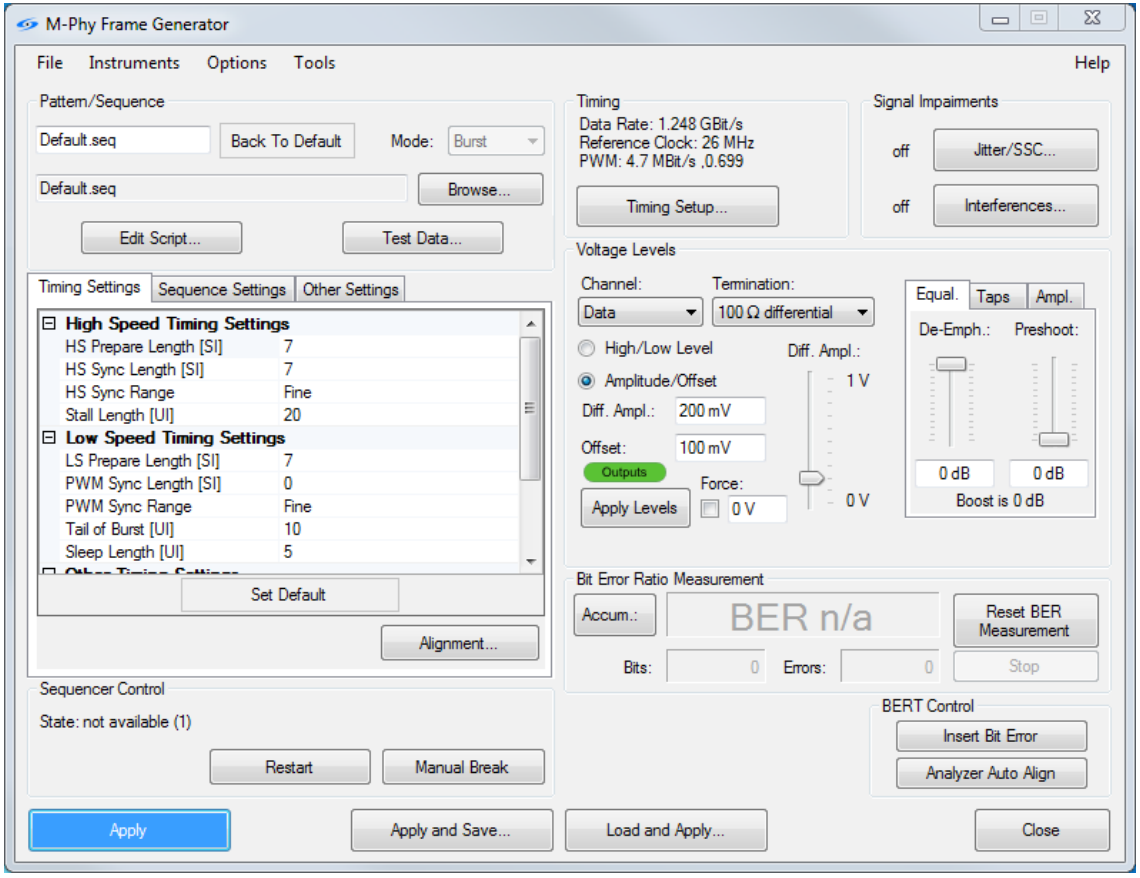

Figure 12 Frame Generator Main Window (after the instruments are connected)

After the desired parameters have been selected, the following steps (see Figure 12) can be done.

- Pressing on "**Apply Setting**" button sends the setup information to the instrument(s). Once this information is received by the instrument(s), the transmission of the M-PHY signal is started. The signal is transmitted continuously until a new setting is applied.
- Click on "**Apply and Save...**" to save the settings with the selected or specified values for the Pattern, Sequence, Levels, Signal Impairments, BER Measurement and Timing parameters.

- "**Load and Apply...**" button is used to load the setting that has been stored.
- "**Close**" button closes the Frame Generator software.

For MIPI M-PHY Frame Generator, some wildcards are available for the sequence file names and those can be used as explained in the section Wildcards.

Wildcards

This section refers to the wildcards availability in the M-PHY Frame Generator for the sequence file names selected in the "**Pattern/Sequence Selection Section**" (Figure 13). If a wildcard sequence name is provided, the sequence name is replaced with different names during run time depending on the test specifics. It is the user responsibility to provide such sequence files in the M-PHY pattern directory, which are not provided by BitifEye.

All the supported wildcards are listed in the table 1 (none are mandatory).

Table 1 Supported Wildcards

Wildcard	Values
[Type]	Rx and Tx
[LsGear]	PWM1, PWM2, PWM3,..PWM7
[HsGear]	Gear1A,..Gear3B
[Mode]	Cont and Burst
[Channel]	Data0, Data1, Data2, and Data3
[Terminated]	RT and NT
[Amplitude]	Large, Small

Example

If the file name is provided as "**Default[Mode].seq**", the sequence file is automatically connected to the default path, "C:\ProgramData\BitifEye\M-Phy Frame Generator\Pattern\Default[Mode].seq" and the drop down menu for "**Mode**" is also enabled.

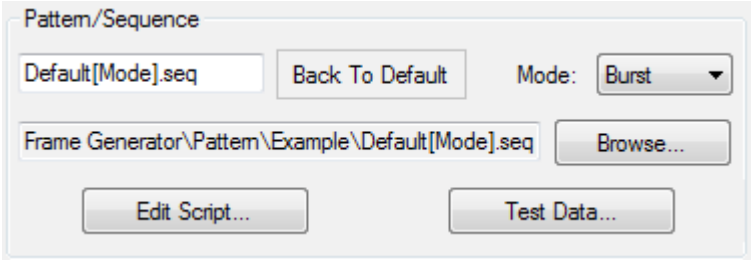

Figure 13 Example of a Wildcard for Sequence Name

NOTE For the GearX-A tests, the sequence file name appears as "MphyComplianceGearXA.seq". If the GearX-A appears with "-" (dash), the ValiFrame does not recognize the sequence file and fails.

Pattern/Sequence Selection

In the Pattern/Sequence section (see Figure 14), either a selected Sequence file (with or without a wildcard) or a Test Data can be specified and personalized. All the parameters are described bellow:

Back to Default

A click on the "**Back To Default**" button sets the default sequence file, "**Default.seq**".

Mode

It is enabled only when the sequence name, "**Mode**" is provided as a wildcard for the sequence file. It can be selected two such options as:

- Burst
- Continuous

Browse

The "**Browse...**" button allows the sequence file to be selected. This file contains the data blocks. By pressing the "**Browse...**" button, the sequence files can be selected. The default location of the sequence files is "C:\ ProgramData\BitifEye\MIPI M-PHY Frame Generator\Pattern".

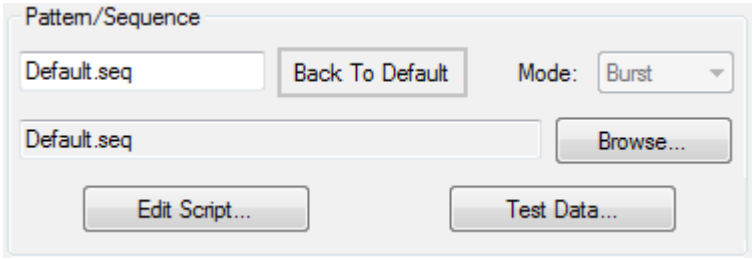

Figure 14 Pattern/Sequence Section

Edit Script

Clicking on the button "**Edit Script**" will open the M-PHY Script Editor Window as shown in Figure 15.

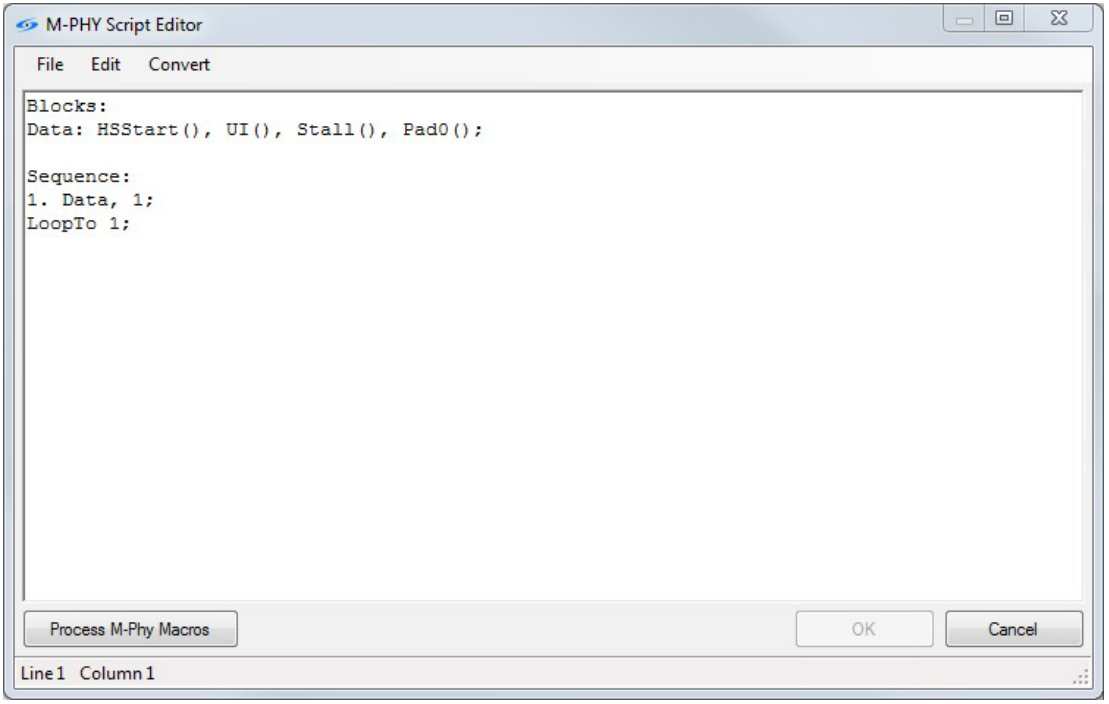

Figure 15 Script Editor Window

The **Script Editor** allows to edit the training sequence and pattern using a unified syntax. For details about this language syntax refer to the "*MIPI M-PHY Frame Generator Language Guide*" document.

By default the **Script Editor** contains the script corresponding to the selected sequence. Every time the sequence is changed, by using the "**Browse**" or "**Back to Default**" button, the edited script is overwritten.

The **File** menu allows to Save or Load the script and Apply or Discard the changes. The **Convert** menu can be used to convert pattern data between different representations (binary, hexadecimal, 8b/10b).

Click the button "**Process M-PHY Macros**" or the same option in the Edit menu to start a script translation, where the macros and symbol names are converted into their binary or 8b/10b representation.

If two generators are used simultaneously, one of them must be selected as shown in Figure 16. When clicking on the button "**Process M-PHY Macros**" only will be processed the sequence steps executed in the selected generator.

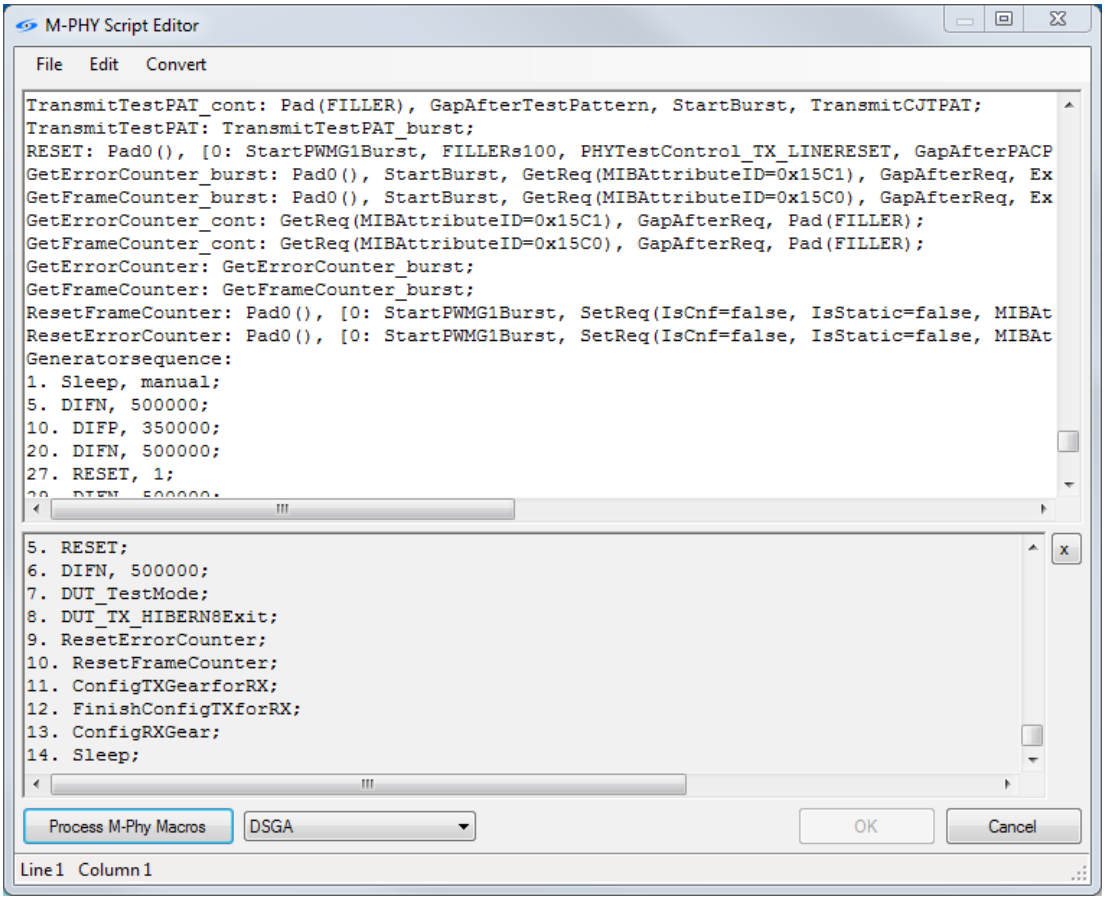

Figure 16 Script Editor Window (for two instruments)

Test Data

If "**Test Data**" button is pressed the **Data Dialog** window will appear as shown in Figure 17.

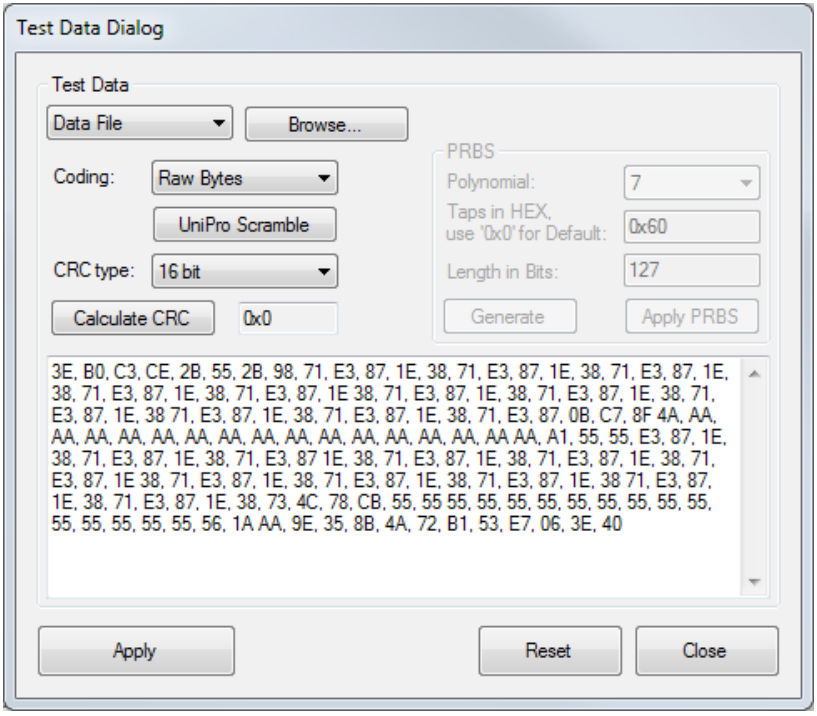

Figure 17 Test Data Dialog Window

The content of the pattern can be specified in this dialog. Select the data type from the drop-down list:

1 Data File

2 Generate PRBS.

When **Data File** is selected, the following properties are available:

Browse

The "**Browse...**" button allows test patterns such as CJTPAT and CRPAT, which are frequently required, to be selected. By pressing on the "**Browse**" button a file load dialog is opened to allow to load a pattern (data) file. The format of these files are described in the "*MIPI M-PHY Frame Generator*

Language Guide" document. Some example pattern are installed at the default path "(C:\ProgramData\BitifEye\MIPI M-PHY Frame Generator\Pattern").

Coding

Select the conversion type from the drop-down list.

1 Bits
2 Raw Bytes
3 8Bit Words
4 10Bit coded

The panel on the bottom of the window displays the coding result as shown in Figure 18 to Figure 21.

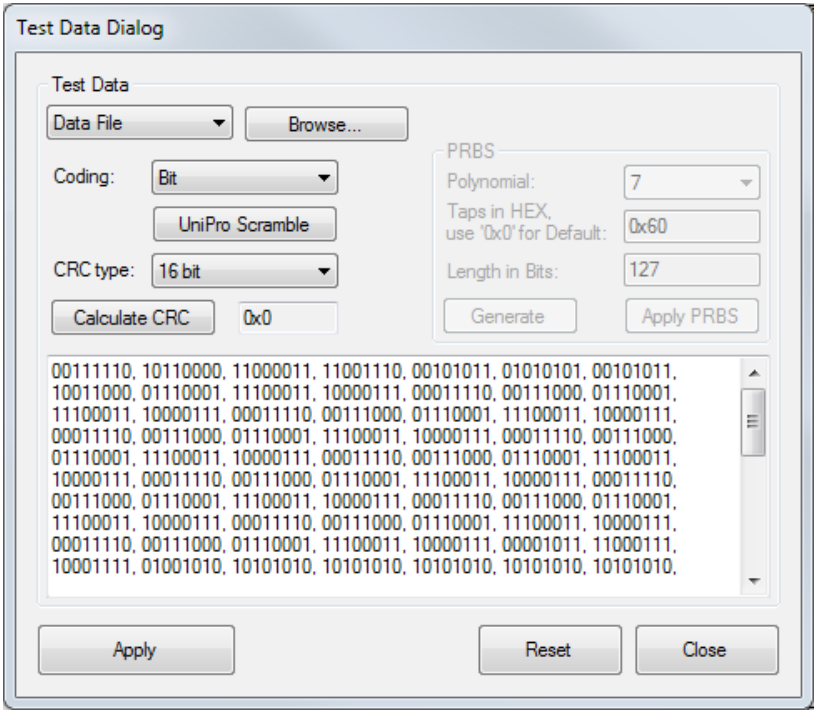

Figure 18 Test Data for Bit Coding

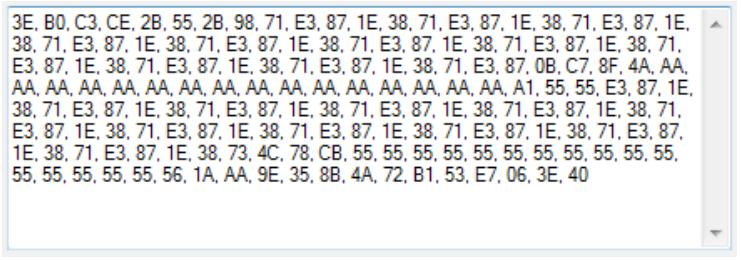

Figure 19 Test Data for Raw Bytes Coding

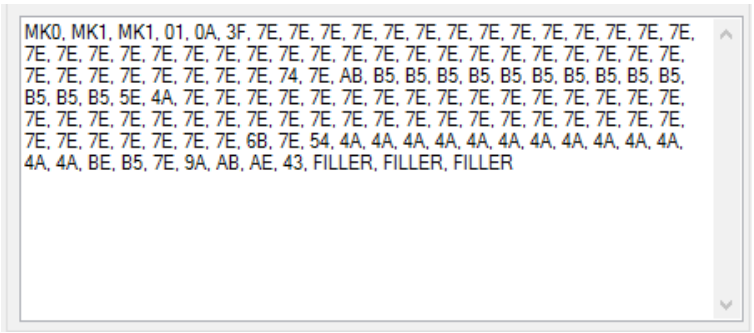

Figure 20 Test Data for 8Bit Words Coding

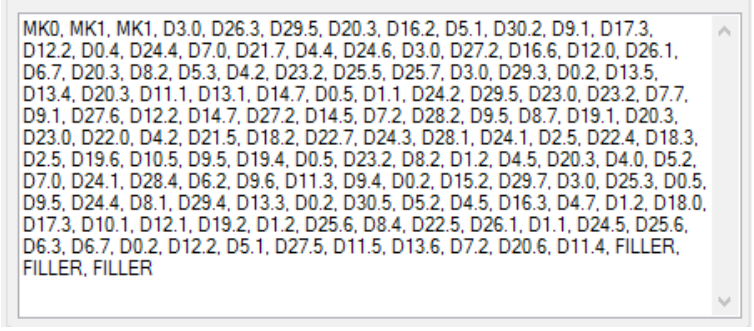

Figure 21 Test Data for 10Bit coded Coding

UniPro Scramble

Pressing on "**UniPro Scramble**" button, a window pops-up as shown in Figure 22 and it allows to generate a scrambled pattern as defined in the UniPro 1.6 specification. It includes the possibility of distributing the "**Input**" data to each lane, apply the alignment, scramble the data, and finally merge it back to the "**Output**" block. The Output data can be saved as a pattern (.seq or .dat) file by coping the data to a text file and loaded for the Frame Generator as GUI pattern.

The procedure to scramble a pattern according to the UniPro 1.6 specification is the following:

1 In Figure 22, the pattern is loaded directly from the **Data Dialog** (Figure 18 to Figure 21) and converted into 8-Bit words such as MK0, MK1, 84, FE, and FILLER and displayed in the "**Input" field**.

2 The pattern includes hex numbers (without 0x), M-PHY marker and filler symbols and these symbols must be formatted to "MK<number>" and "FILLER". This pattern can also be edited but should be assured that it contains only one burst of data with UniPro data packets.

3 The number of lanes can be chosen from the drop-down menu and each selected lane will be scrambled individually with a specific seed for the scrambler.

4 When the check box "**Align Lanes**" is selected, two MK2 symbols are aligned lane-wise and replaces series of FILLER symbols before the scrambling.

5 If the option, "**Add Sync (MK0, MK1)**" is checked, the sync pattern (MK0, MK1) can be added automatically for each data lane at the beginning of the pattern. If the Input pattern already contains a sync pattern, it must be removed manually and select "**Add Sync (MK0, MK1)**" option as each lane requires one sync pattern.

6 By pressing on the "**Apply**" button, the Input pattern is separated over the selected number of lanes, the sync pattern is added and the data is scrambled at each lane independently. Finally the processed input pattern of all data lanes is merged and displayed in the "**Output**" field.

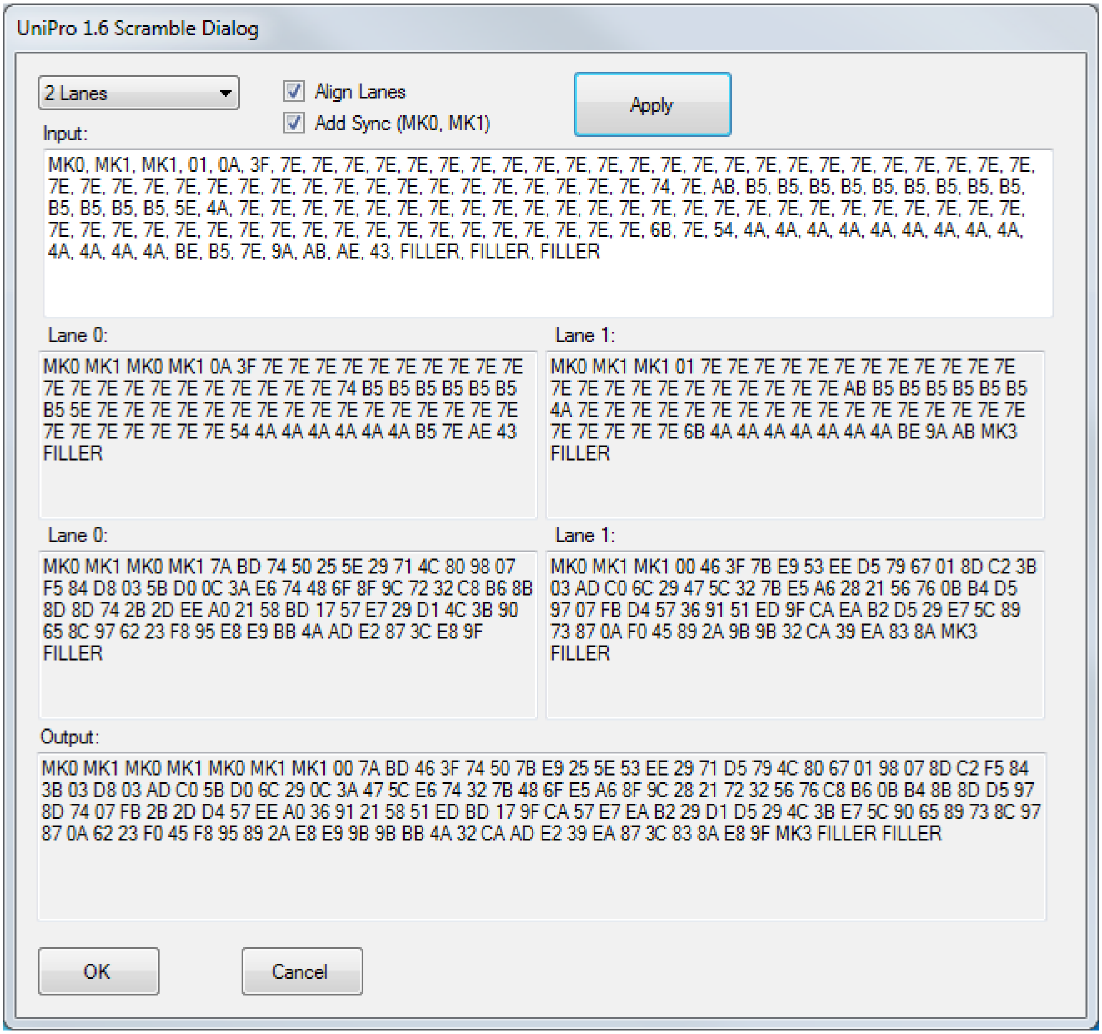

Figure 22 UniPro 1.6 Scramble Dialog

7 The series of three consecutive FILLER symbols are replaced by MK3, 67, FILLER (the number of 67 increases according to the number of FILLER symbols, for example if 5 consecutive FILLER symbols exist, the result will be MK3, 67, 67, 67, FILLER). This result is displayed in the first row of lane dependent text fields.

8 The second row of lane dependent text fields display the scrambled data for each lane. The scrambling of MPHY data signals is started once the sync sequence has been received on each lane. The marker and FILLER symbols shall never be scrambled.

9 The data is scrambled with a PRBS which is generated using a LFSR (Linear Feedback Shift Register), implementing the generator polynomial: G(x) = x16 + x5 +x4 +x3 + 1. The LFSR generates an eight bit sequence at G(x) for every M-PHY symbol. The LFSR polynomial generation also advances for eight bit cycles, when symbols that must not be scrambled are presented to the scrambler.

10 The **Output** field shows the final and merged scrambled pattern. If "**s**" is kept at the beginning of the pattern, the data is converted from 8b10 b coded to binary data stream.

11 Pressing on "**OK**" button closes the UniPro 1.6 Scramble Dialog (Figure 22). The pattern from the Output field is copied to Data Dialog (Figure 17 to Figure 21) and converted to 8 Bit Words coding.

12 After the word size has been set to 20 bit (this is important for the proper distribution to each lane), press "**Apply**" to send this scrambled pattern to the instruments.

CRC Type

CRC (Cyclic Redundancy Check) is used to check the accidental changes to the raw data. The CRC type can be selected as:

- 16 bit
- 16 bit UniPro
- 8 bit

Calculate CRC

This button is used to calculate the CRC for the selected CRC type.

The option "**Generate PRBS...**" is used to generate the data code for the short repeating patterns of 10 bit code words (see Figure 23).

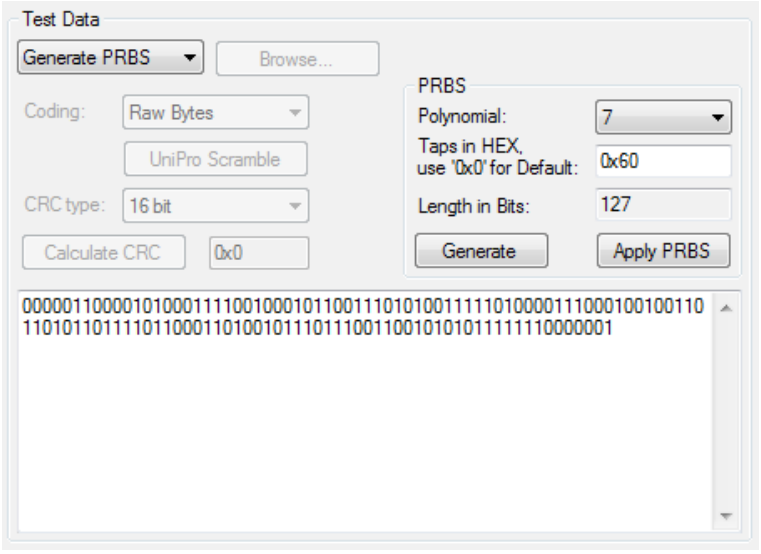

Figure 23 Test Data for Generate PRBS

Polynomial

The PRBS can be generated using a LFSR. The order of the polynomial can be selected from 3 to 16.

Taps in HEX

Set here the polynomial taps with a hexadecimal number. When '0x0' is set and then "**Generate**" button is pressed, the taps value is re-calculated to get the maximum bit length according the polynomial order selected.

Generate

If the "**Generate**" button is pressed, the bottom panel shows the pattern bits. The length is indicated in the property "**Length in bits**".

Apply PRBS

Press the "**Apply PRBS**" button to generate the corresponding PRBS code.

NOTE

The pattern defined in the "**Test Data**" dialog will only be used when the sequence file contains the "**UI**" key word in the block definition section (see sequence file format in the "*MIPI M-PHY Frame Generator Language Guide*" document). The default sequence contains the UI statement, "**Test Data**" hence is used with the default sequence. To return to the default sequence quickly, press the "**Back To Default**" button.

Timing/Sequence/Other Settings

Timing Settings

In the **Timing Settings** section some timing parameters related with the sequence can be modified as shown in Figure 24.

The value of the parameter can be changed by entering the desired values manually. These timing parameters are defined in the Table 6/7 “PREPARE and SYNC Attribute and Dependent Parameter Values” of the M-PHY Specification document.

If the selected timing parameters are not changed, their default values are applied, if “**HSStart**” or “**LSStart**” is part of the sequence file (see sequence syntax definition in the “*MIPI M-PHY Frame Generator Language Guide” document*).

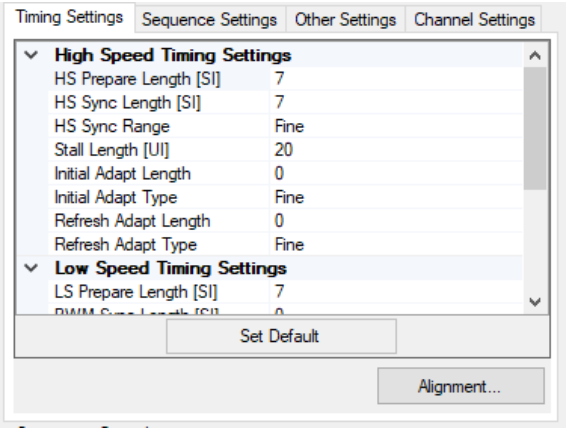

Figure 24 Timing Settings parameters

High Speed Timing Settings

- **HS Prepare Length**
  The prepare length is the initial sub-state before the HS-burst starts and it defines the number of DIFP (Differential Positive Voltage) states before the bit stream is started. An example of HS prepare length is shown in Figure 25. The actual HS prepare length can be calculated with the formulas given in the Table 6/7 “PREPARE and SYNC Attribute and Dependent Parameter Values” of the M-PHY Specification document.

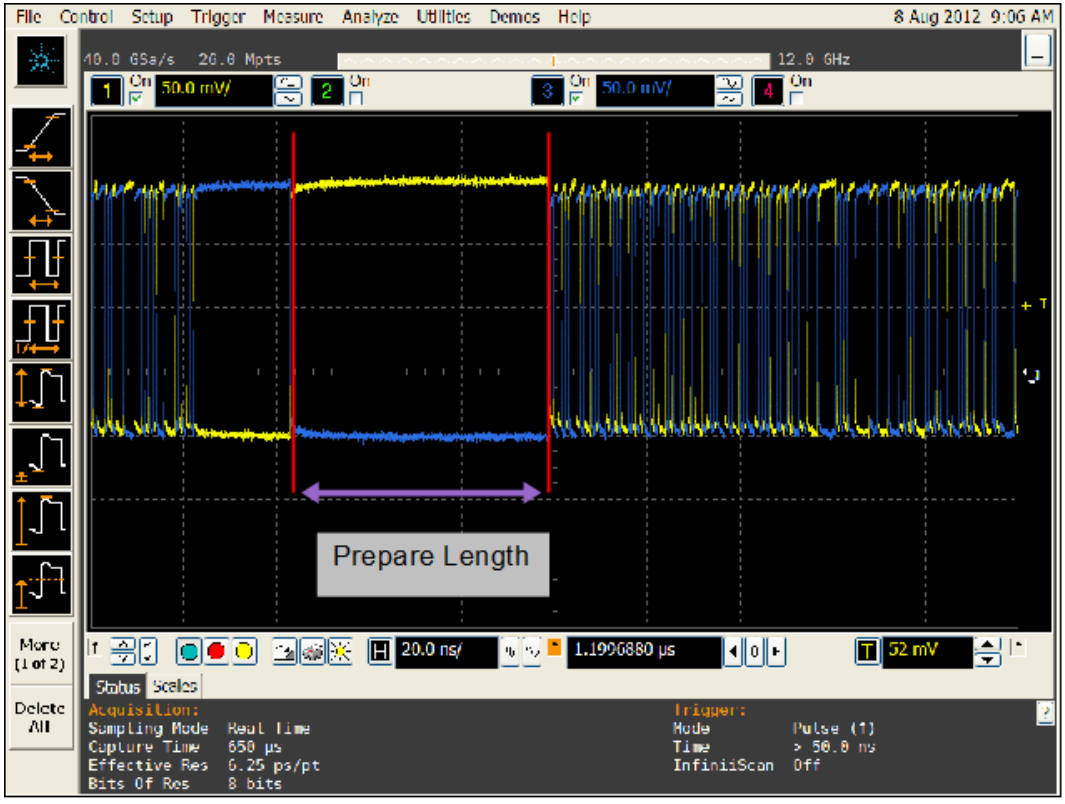

Figure 25 HS Prepare Length Example

- **HS SYNC Length**
  This defines the number of SYNC pattern symbols before the burst starts. For HS mode, the prepare length will be followed by the SYNC sequence (D10.5, D26.5). In HS burst and PWM burst (for PWM-G6, PWM-G7), the SYNC sequence is followed by the payload. The payload starts with MARKER0 (MK0). An example of the SYNC sequence (D10.5, D26.5) followed by MK0 symbol in the case of HS burst is as shown in Figure 26.

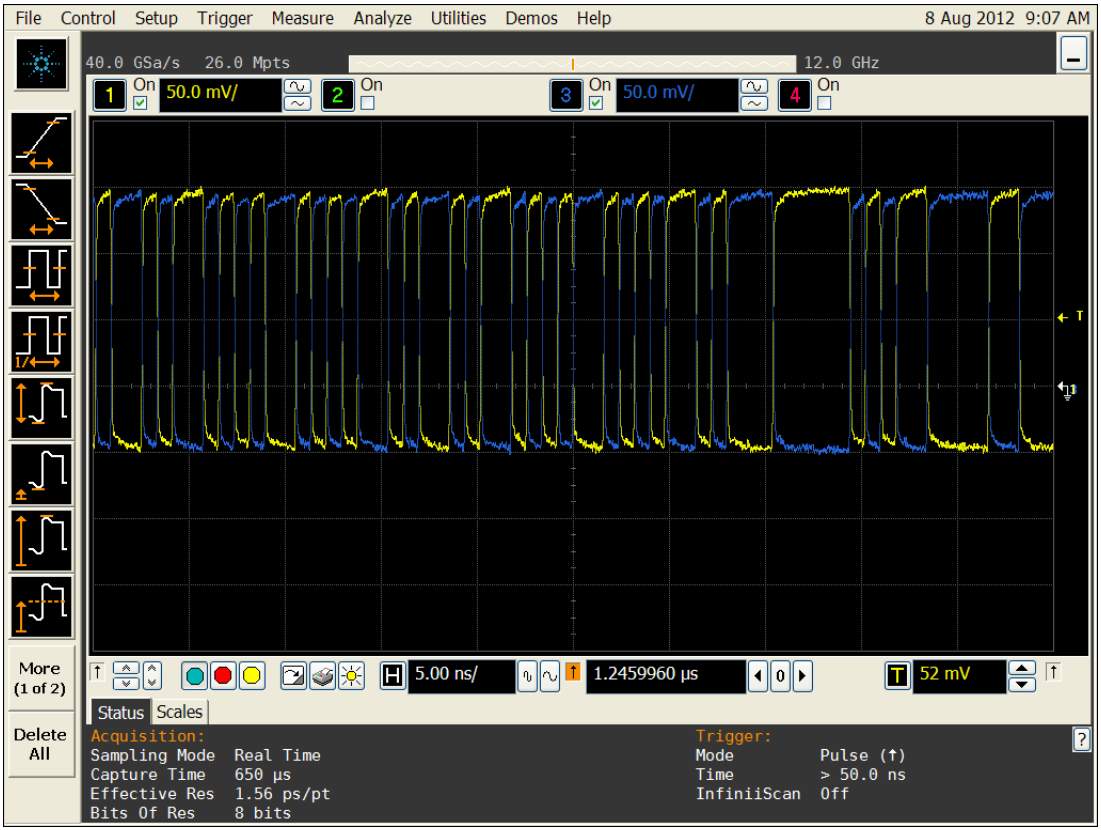

Figure 26 Sync Sequence is followed by MK0 in HS burst

- **HS SYNC Range**
  It sets the sync range to “FINE” (0) or “COARSE”. If “COARSE” is selected, the sync time duration T_sync is equal to Min (2^sync_length, 2^14).
- **Stall Length**
  It defines the number of DIFN states after a data burst. This parameter only affects the data output when the sequence file (seeFigure) contains a “STALL” entry in the data block definition. Figure 29 shows an example of PWM stall.

- **Initial Adapt Length**
  The ADAPT sub-state is intended for the DUT equalizer training to adapt to the channel characteristic, when receiving an HS data stream. The ADAPT sequence shall start with an MK0 followed by an 8b10b encoded PRBS9 pattern completed by one b0 bit. The Initial Adapt Length parameter defines the duration of the Initial ADAPT sequence after power-up.
- **Initial Adapt Type**
  It can be set as fine or coarse.
  When it is set to fine the Initial ADAPT sequence is calculated as:
  T = 650 * (Adapt_length + 1).
  When it is set to coarse the Initial ADAPT sequence is calculated as:
  T = 650 * 2Adapt_length
- **Refresh Adapt Length**
  It defines the duration of the refresh ADAPT sequence during link operation.
- **Refresh Adapt Type**
  It can be set as fine or coarse.
  When it is set to fine the refresh ADAPT sequence is calculated as:
  T = 650 * (Adapt_length + 1).
  When it is set to coarse the refresh ADAPT sequence is calculated as:
  T = 650 * 2Adapt_length

Low Speed Timing Settings

- **LS Prepare Length**
  This defines the number of DIFP states before the LS burst starts. LS burst depends on the type of DUT modules as given below:

  1 PWM Burst for the DUT Type I modules

  2 SYS Burst for the DUT Type II modules

  An example of SYS prepare length is shown in Figure 27. The actual "**SYS prepare length**" can be calculated with the formulas given in the Table 6/7 "PREPARE and SYNC Attribute and Dependent Parameter Values" of the M-PHY Specification document.

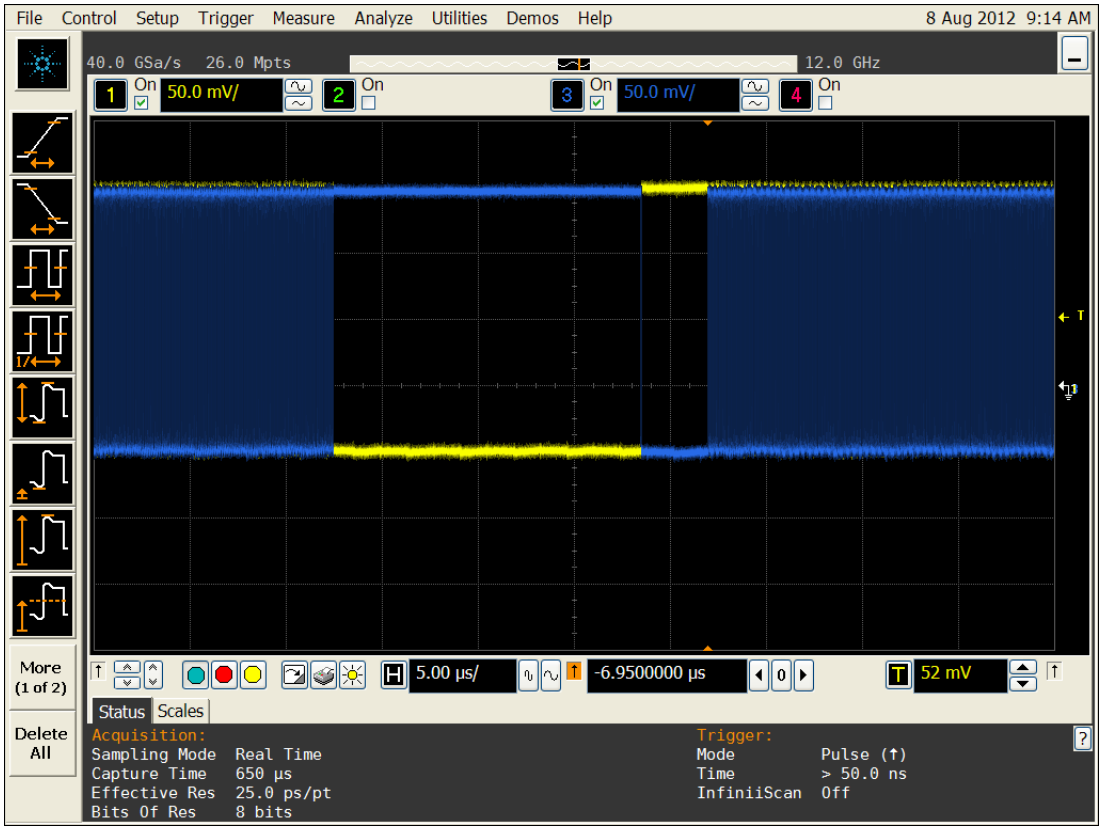

Figure 27 SYS Prepare Length Example

- **PWM Sync Length**
  This defines the number of SYNC pattern symbols before the burst starts in LS mode. It can be selected from 0 to 15. It only applies to PWM-G6 and PWM-G7, where the prepare length may be followed by the SYNC sequence. For SYS burst and the other PWM gears, the SYNC sequence is not added.

  The SYNC length can be calculated using the method given in the Table 6/7 “PREPARE and SYNC Attribute and Dependent Parameter Values” of the M-PHY Specification document. Figure 28 shows an example of MK0 (K28.5) symbol in the case of PWM burst.

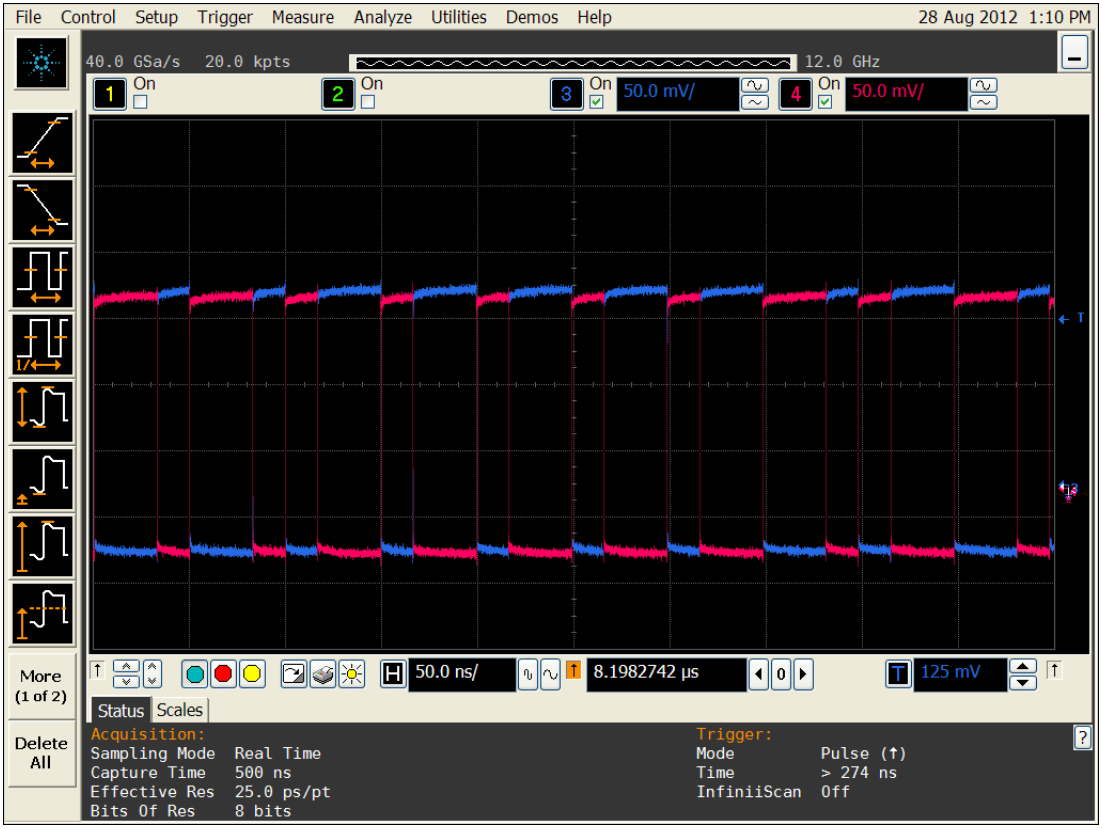

Figure 28 PWM MK0

- **PWM SYNC Range**
  This sets the sync range to “FINE” (0) or “COARSE”. If “COARSE” is selected, the sync time duration T_sync is equal to Min (2^sync_length, 2^14).
- **Tail of Burst**
  It is defined as either a series of 0 bits or 1 bits transmission after the last 8b10b symbol of the burst.
- **Sleep Length**
  It is the power saving state in LS-mode. It will add as many DIFN (0) states as given by the Sleep length in the user interface. The LS Stall for SYS burst also adds DIFN (0) states but for PWM burst, the stall adds all PWM zeros and one PWM one. For example: LS STALL id PWM (10), stall will be nine PWM zeros and one PWM one.

Other Timing Settings

- **Squelch Pulses**
  This defines the number of pulses in the squelch data block. This parameter only affects the data output when the sequence file contains a “SQUELCH” entry in the data block definition (in Pattern/Sequence selection section Figure 14).
- **Squelch Pulse Width**
  Squelch pulse width is the width of the DIFN pulse in the squelch data block.

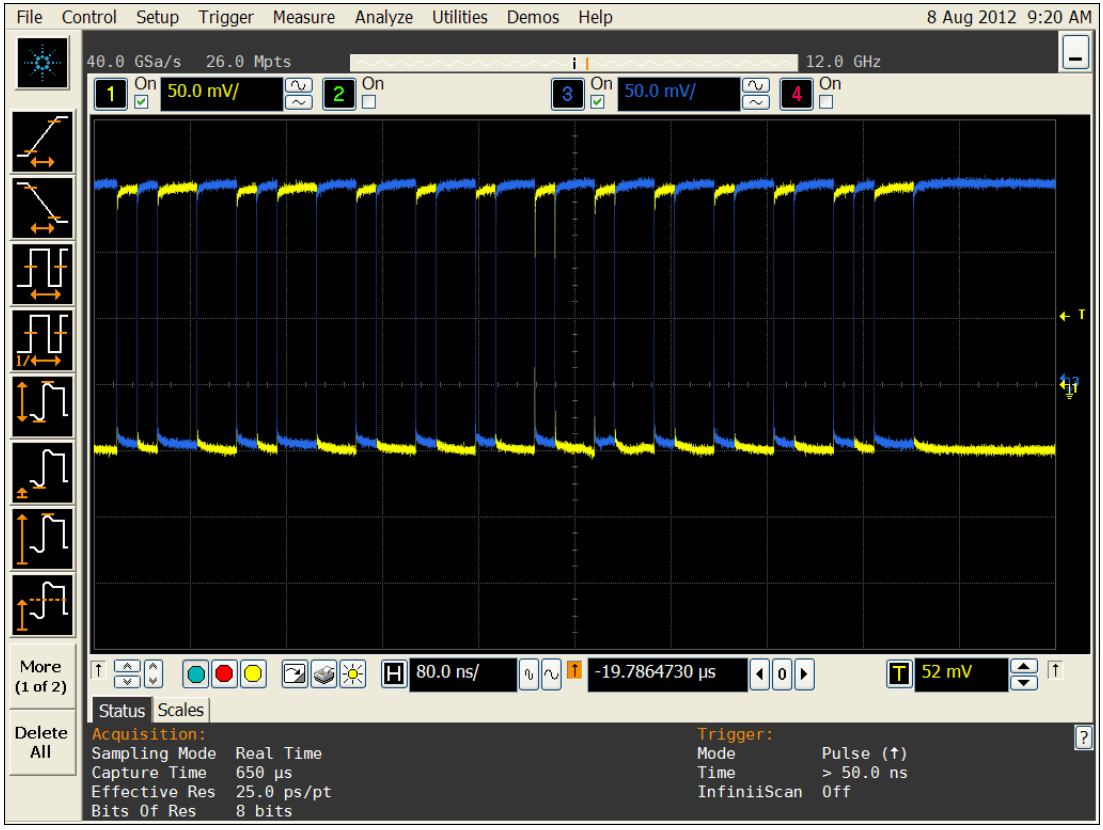

Figure 29 PWM Stall Example (PWM Exit with 9 zeros and 1 one)

- **Squelch Pulse Distance**
  This is the distance between DIFN pulses in the squelch data block.
- **Example of Squelch Pulse and Squelch Pulse Distance**
  When the values of the squelch pulses, squelch pulse width, and squelch pulse distance are changed in the Timing parameter selection section as in Figure 31, the waveform is as shown in Figure 30.

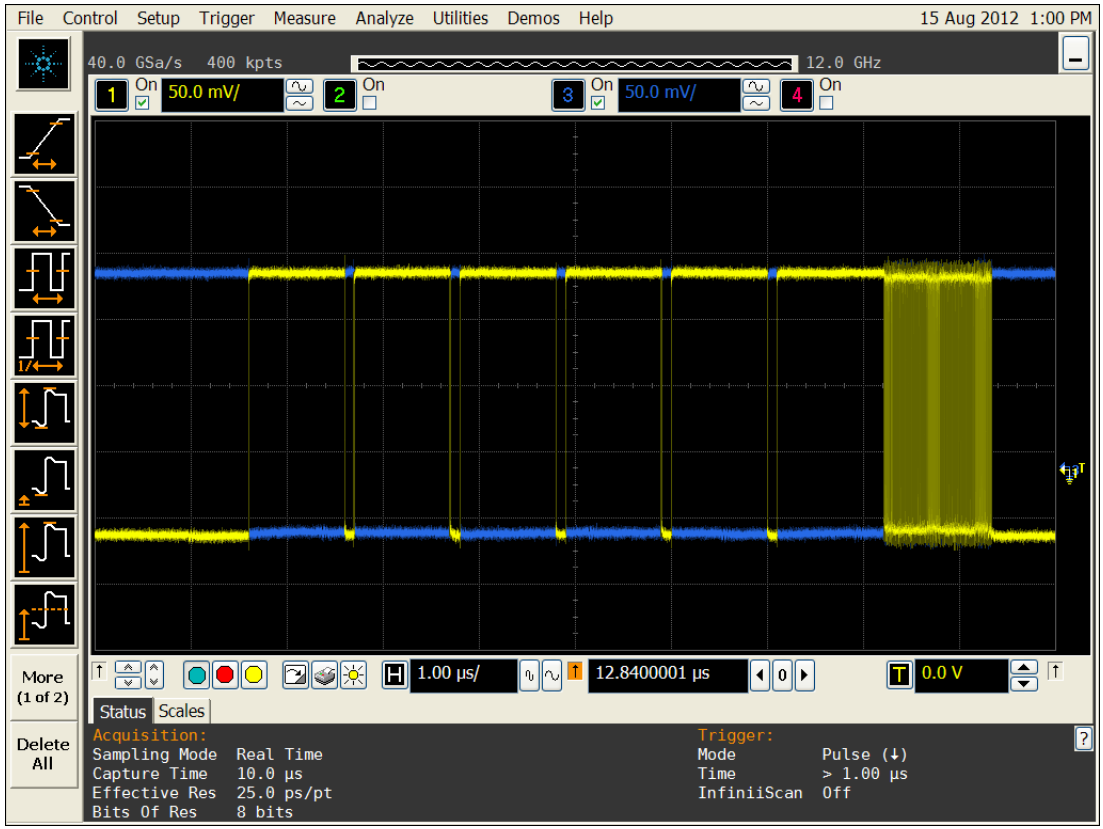

Figure 30 Squelch Pulse Width and Distance

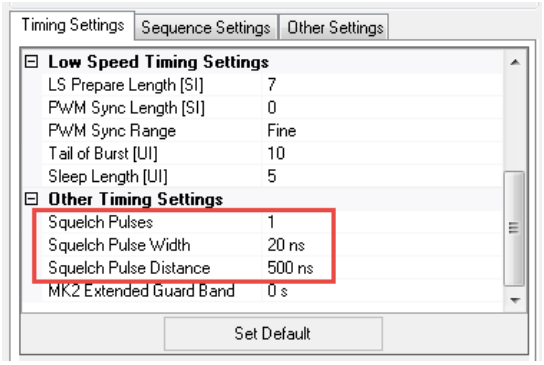

Figure 31 Squelch Pulse Timing Example

- **MK2 Extended Guard Band**
  According to the UniPro 1.6 specification, for HS Burst, the prepare length remains as in a normal sequence but the sync length can be increased with the MK2 Extended Guard Band value. For PWM with Gear 1 to 5, the prepare length increases by adding the value of MK2 Extended Guard Band and in case of PWM with Gear 6 and 7, the prepare length does not change but the sync length increases by the MK2 Extended Guard Band value. The MK2 Extended Guard Band value can be set in Timing Parameter Selection (see Timing/Sequence/Other Settings). The Frame Generator supports a new macro called “GuardBand”, it should be used alone in one block and placed in between HS/LSStart and the payload.

  The resulting Sequence file looks like the following example:

Table 2 Sequence Examples using "GuardBand"

HS Burst	LS Burst
Blocks: Start: PAD,HSStart; ExtendedGuard: GuardBand; Data: B"MPhyCJPatData0.dat",Stall,PAD; Sequence: 1. Start,1; 2. ExtendedGuard,1; 3. Data,1;	Blocks: Start: PAD,LSStart; ExtendedGuard: GuardBand; Data: LB"MPhyCJPatData0.dat",LSStall,PAD; Sequence: 1. Start,1; 2. ExtendedGuard,1; 3. Data,1;

- **Alignment**
  By pressing the "**Alignment**" button (on the bottom of the Timing Setting panel), the alignment dialog window is started as shown in Figure 32.

  For M8020A generator, the skew is applied instantaneously to the channels without stopping the data transmission.

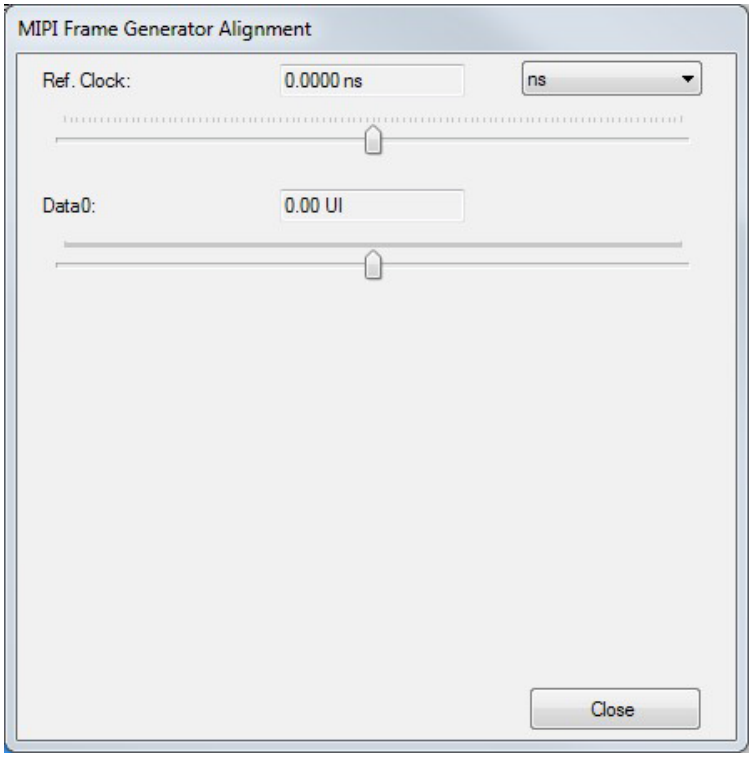

Figure 32 Alignment Dialog

Sequence Settings

Some sequence settings can be configured by selecting the Sequence Settings tab as shown in Figure 33:

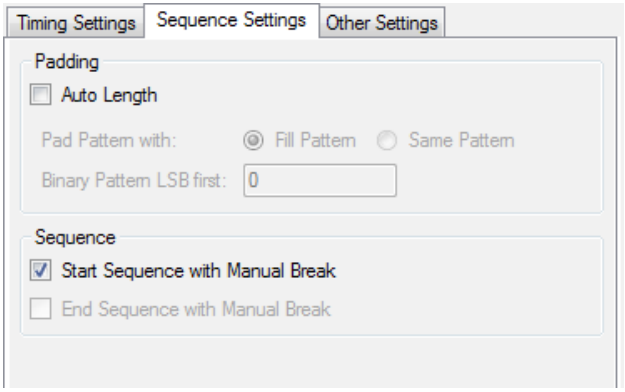

Figure 33 Sequence Setting parameters

Auto Length

If this box is checked, zeros (0) are added to the test data to meet the data generator's memory segmentation requirements (refer to the "*MIPI M-PHY Frame Generator Language Guide*" document for more details about granularity restrictions).

Two choices are available for padding the block size to the instrument pattern granularity:

- Fill Pattern

  Selecting "Fill Pattern", extends the block by a pattern specified in binary format in the "Binary Pattern LSB (Least Significant Bit) first" text box. The default is to extend the DIFN (Differential Negative Voltage) (0) states

- Same Pattern

  If "same Pattern" option is used, the same pattern is used to extend the block.

Start Sequence with Manual break

If selected, the sequence will start with a manual break.

End Sequence with Manual break

If selected, the sequence will end with a manual break.

NOTE When using the automatically generated Unipro sequence files this option must be disabled.

Other Settings

In the **Other Settings** tab (see Figure 34), the following parameters can be modified:

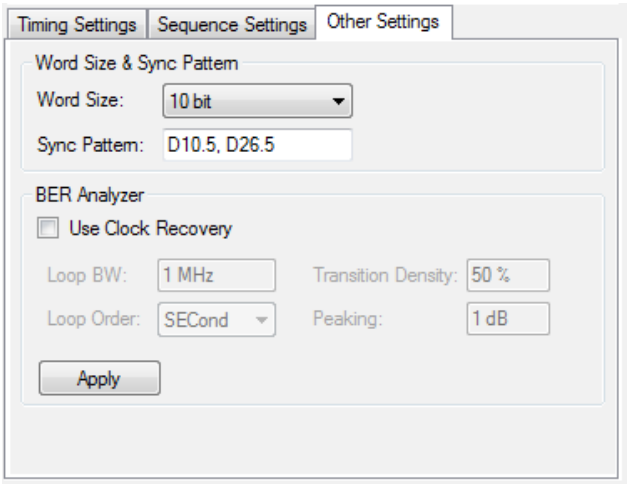

Figure 34 Other Settings parameters

Word Size

The word size can be selected as 8 bits, 10bits, 16 bits and 20 bits.

Sync Pattern

D10.5 and D26.5 are the default sync symbols used for the sync pattern. The symbols with at least seven transitions inside the symbol (out of nine possible transitions) are used for the sync sequence.

DSGA & Switch Options

Type: It can be as

- Relay

- Solid State
- Both: Both types can be in the same DSGA chassis

Order: Only available for relay type. With relay switches you can control the way normal and complement switch: “simultaneously”, “N before P” or “P before N”.

Delay: Only available for relay type. If the switching order is not simultaneous, you can set approximately the delay for the operation.

Set Amplitude to 0 before switching: Check this option to force that the generators amplitude is set to 0 before switching. This is to reduce the effects that the relay switch bouncing has on some DUTs; it can make them come out of test mode

Use Clock Recovery

Check this option for using the CDR in the Analyzer.

Loop BW

Introduce here the Bandwidth value of the analyzer CDR.

Loop Order

It can be selected as First or Second order.

Peaking

The CDR peaking can be selected as Low, Medium or High.

Transition Density

The transition density of the CDR can be set from 0% to 100%

Channel Settings

Lane Test Mode

Select the option “Simultaneously” to test all the lanes at the same time. In this case, make sure that the sequence file is adapted accordingly.

Lane Under Test

The lane that will be tested with when the Lane Test Mode is selected as “Individually”

Timing

The timing section shows the current data rate and reference clock frequency selected. To change these and others parameters related with the burst in HS mode and LS mode click on the button "**Timing Setup...**". A window as shown in Figure 35 will appear.

Mphy Type

Type

Select here the low speed type as Type I (PWM) or Type II (SYS). Data transmission occurs during the bursts. In general, a Type I module uses PWM self-clocked LS signaling and a Type II module uses SYS LS signaling. Type II modules require a shared reference clock between the two ends of each lane, where as Type I modules need to be able to operate with independent local clock references on each side of the lane.

Ref Clock Frequency

The frequencies 19.2 MHz, 26 MHz, 38.4 MHz, and 52 MHz can be selected as reference clock frequency from the drop-down list.

Applied Freq

It is the reference clock frequency that will be configured on the instrument.

High Speed

Nominal Data Rate

It sets the reference clock frequency to achieve the nominal Gear x-B data rate value as given in the specification. In case of custom data rates, the reference clock is adjusted to achieve the HS data rate that the user provided.

Nominal Ref. Clock

For the selected reference clock frequency, the generated data rate is calculated as a multiple of the reference clock.

HS Gear

HS gears, GEAR 1-A, 1-B, 2-A, 2-B, 3-A, 3-B, 4-A and 4-B can be selected from a drop-down list. The data rates are displayed automatically in the adjacent box. The available data rates depend on the capabilities of the data generator hardware.

Applied DR

It is the Data Rate value that is set to the instrument.

Deviation

This is the deviation from the nominal value. Deviations of 0%, +0.1%, and –0.1% can be selected. This deviation will be applied to all data rates (HS and LS) and also to the reference clock frequency.

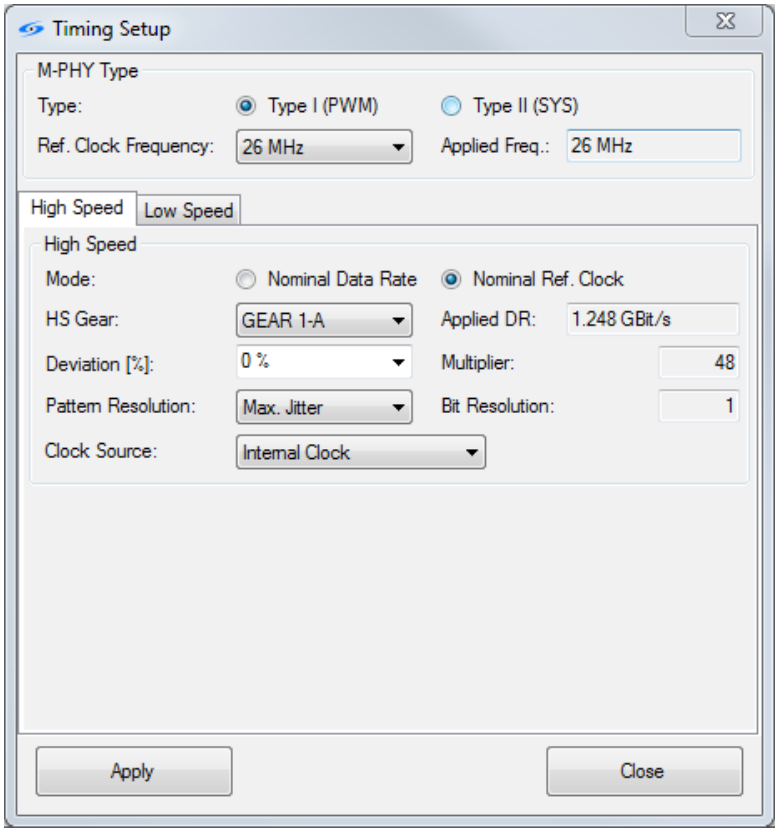

Figure 35 Timing Setup Window (High Frequency)

Multiplier factor

It is the multiple value of the reference clock frequency to the applied data rate value.

Pattern Resolution

The HS data rate is the master data rate. All other frequency and timing parameters are derived from it. To gain higher granularity for skew and PWM generation, the instrument can be run at a multiple of the HS data rate. In this case, even the HS data stream uses bit doubling. This can be continued by selecting the max. resolution mode instead of the max. jitter mode.

Bit Resolution (read only)

The bit resolution depends on the Pattern Resolution selected. It shows how many times the HS bit will be multiplied to archive the selected HS Gear.

Low Speed

If the option “Type I (PWM)” from the Type drop-down menu is selected, the PWM parameters can be modified in the Low Speed section as shown in Figure 36.

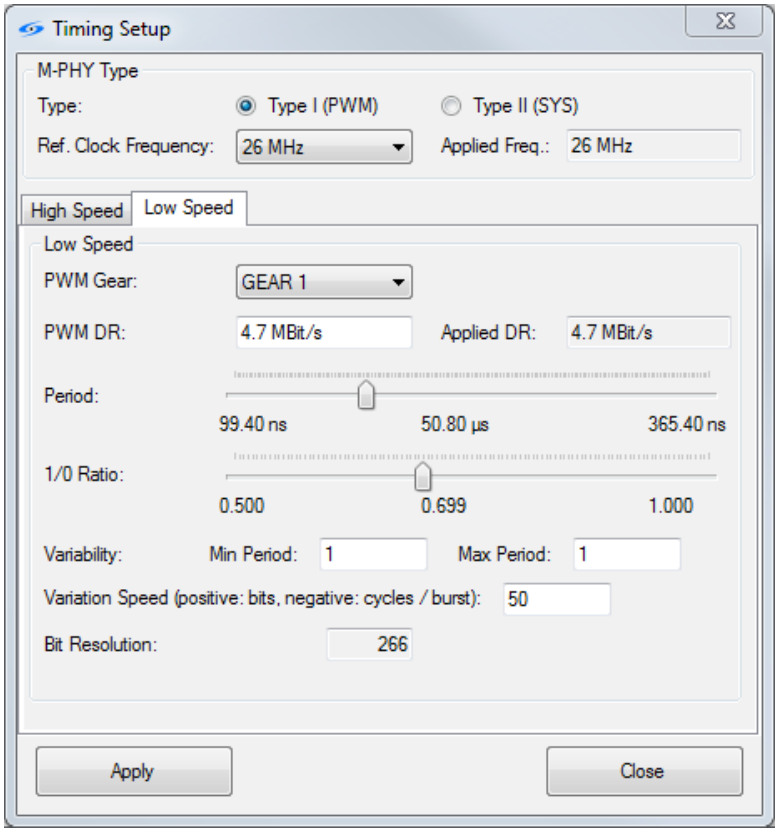

Figure 36 Timing Setup Window (Low Speed)

PWM Gear

Select the PWM gear range (Gear 1 to 7) using the drop-down list. PWM Gear1 is the default at start-up and after reset.

PWM DR

It is the nominal frequency for the Gear selected.

Applied DR

It is the Data Rate value that is set to the instrument.

Period

Select the period for one bit by moving the slider. Since PWM is generated by bit multiplying, the choice of available data rates is limited.

1/0 Ratio

This sets the PWM ratio for the long state. Since PWM is generated by bit multiplying, the number of ratios is limited.

Variability

M-PHY allows a variation of the bit length in PWM mode. The two values for “min. Period” and “max. Period” define the maximum deviation for the generated bit length.

Variation Speed (positive: bits, negative: cycles / burst)

The bit variability is a sinusoidal function. The variation speed allows the frequency or period of the variation to be set. If the variation speed value is positive, then the period is given in PWM bits.

Example: If the value is 10, then the sinusoidal function has a period of 10 PWM bits.

If the variation speed value is negative, then the period value is given as number of cycles per burst.

Example: For a burst with 250 PWM bits and a '–10' (negative) speed, the variation period is 25 PWM bits.

Bits Resolution (read only)

Number of bits per PWM period.

Low Speed Gen.

If the DSGA is used to generate low speed signal, the **Timing Setup** dialog will include a panel for configuring the PWM signal created with the DSGA (see Figure 37). For more detail about the PWM parameters refer to previous section.

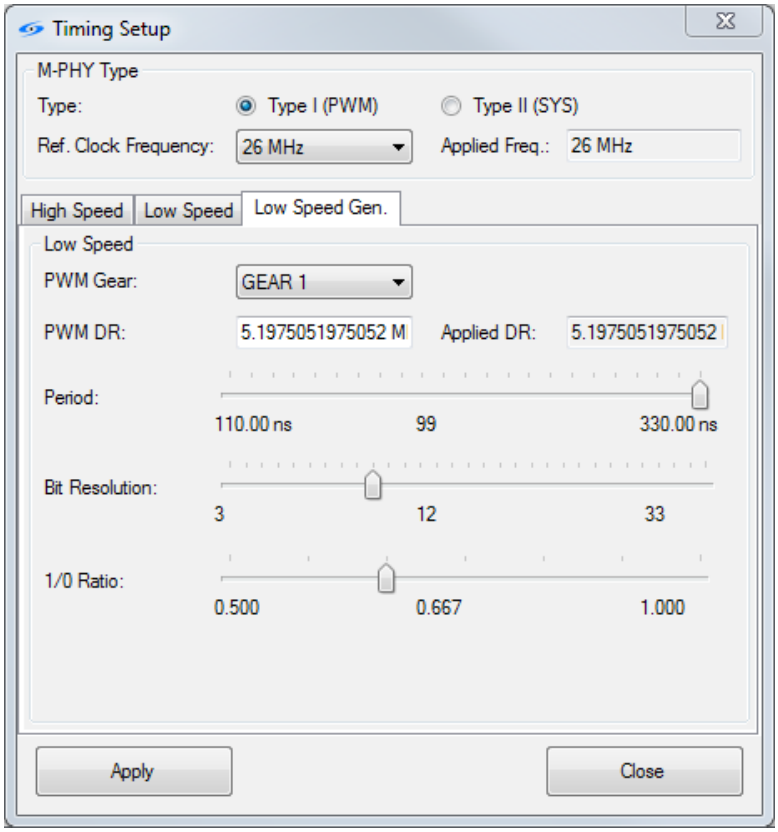

Figure 37 Timing Setup Window (Low Frequency for DSGA)

Signal Impairments

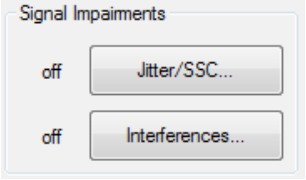

Figure 38 Signal Impairments Section

Jitter Setup

Pressing the "**Jitter/SSC**" button in the Signal Impairments Selection section (see Figure 38), starts the **Jitter Setup** dialog as shown in Figure 39. If hardware jitter sources are available, the jitter amplitude and frequency can be selected for sinusoidal, random, and periodic jitter. The parameter values can be entered either by selecting the parameter field with a left mouse-button click and using the slider or manually.

Only the LF Sinusoidal Jitter via Clock is generated via clock modulation. The LF Random Jitter, LF Sinusoidal Jitter and ST Sinusoidal and Random Jitter components are generated via delay lines.

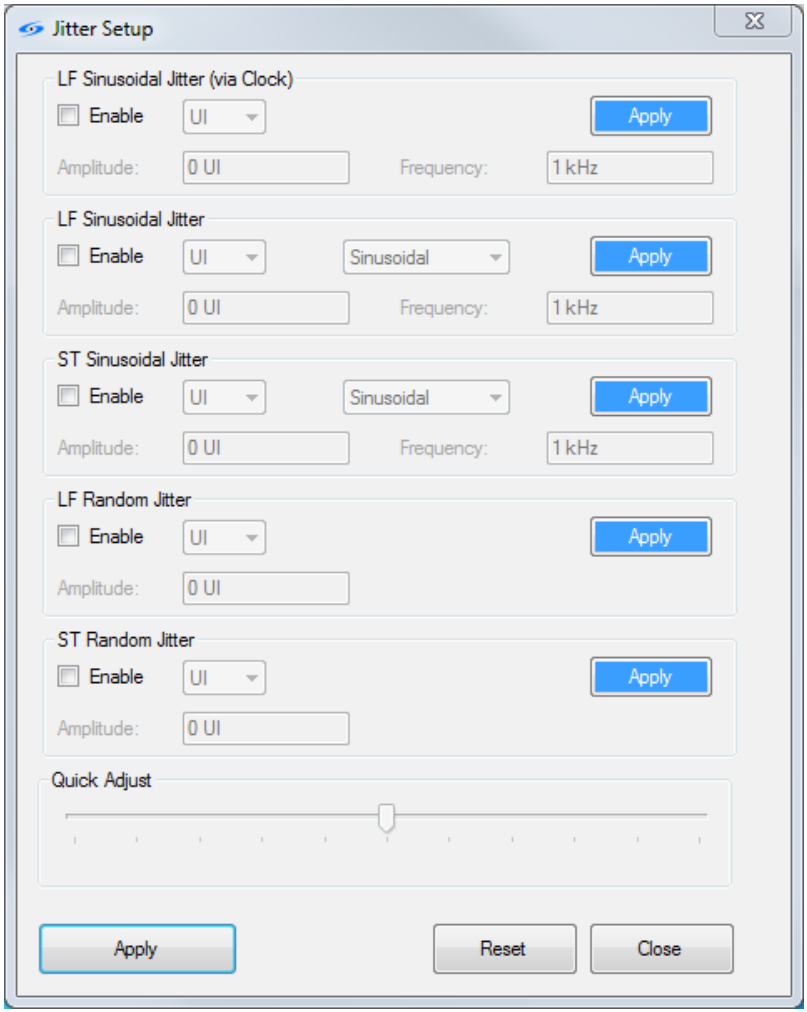

Figure 39 Jitter Setup Window

Apply

When any slider is moved, the corresponding parameter will be written to the hardware immediately. Values changed in the text boxes need to be applied by pressing the "**Apply**" button to effectively set on the instrument.

Reset

It restores all the jitter settings to the default value.

Close

It closes the "**Jitter Setup**" dialog box.

Sinusoidal Interference Setup

By pressing the button "**Interferences...**" in the Signal Impairments section, the Sinusoidal Interference Setup window appears as shown in Figure 40.

This dialog allows to add Common Mode and/or Differential Mode Sinusoidal Interference to the output signal. The amplitude peak to peak and the frequency can be selected for both impairments.

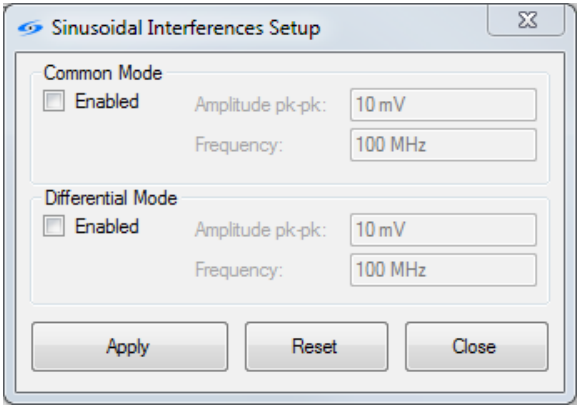

Figure 40 Sinusoidal Interference Setup Window

Voltage Levels

The reference clock and data channel levels can be modified in the Voltage Levels Panel (Figure 41). The parameter values can be entered numerically or by using the slider. If the parameter values are entered numerically, the "**Apply Levels**" button needs to be pressed to apply the values. If instead a slider is moved to change a voltage value, the value is automatically applied on the instrument. The levels can be set for each data channel individually, as well as, for the reference clock.

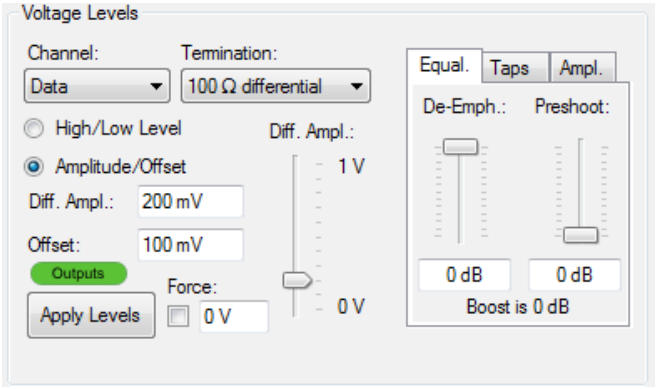

Figure 41 Voltage Levels Selection Section

Channel

"Channel" allows the "Data" channel and "Reference clock" channel to be selected from a drop-down menu.

High/Low Level – Amplitude/Offset

The levels can be set as High and Low level values or as Amplitude and Offset voltage.

Outputs

The "Outputs" button is only available for the M8020A generator. Clicking on the button will turn on/off the M8020A outputs.

If the button is in green color means that the outputs of the M8020A are turn on and if is in red color means that the outputs are turn off.

Apply Levels

This button applies the values, which are selected manually for “High/Low level” and “Amplitude/Offset” for the channel selected above (Data or Reference clock).

Force 0V

A click on “Force” check box sets the data output amplitudes to the defined value (0 by default) without using the slider.

De-Emphasis

The de-emphasis and pre-shoot levels can be selected. The tabs let you select between three different views:

- de-emphasis and pre-shoot in dB
- FIR(Finite Impulse Response) tap coefficients
- emphasized and de-emphasized voltage levels

Note that when any slider is moved, the corresponding parameter will be written to the hardware immediately.

If two instrument are used simultaneously the Voltage section will show two panels. One for the Main Generator (the M8020A) and other one for the LS Generator (the DSGA). See Figure 42.

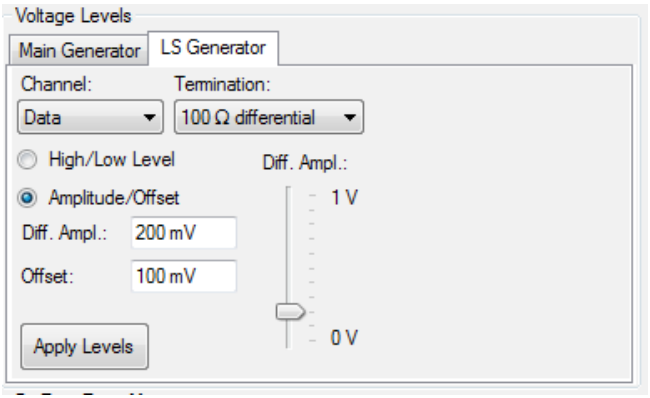

Figure 42 Voltage Levels Selection Section (for two instruments)

BER Measurement

Figure 43 shows the BER Measurement Panel.

This panel allow to measure the Bit Error Rate when the DUT is working in loopback mode. In loopback mode the DUT will loop back the received test pattern. Then the Error Detector (ED) compares the pattern returned by the DUT with the generated pattern to detect bit errors and compute the BER.

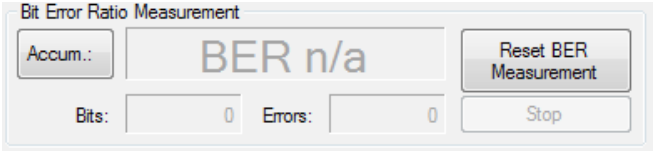

Figure 43 BER Measurement Section

BER (Bit Error Rate)

Bit error rate is the ratio of the number of false or error bits to the total number of transmitted bits, that is; errors/bits.

Accumulated - Current

When the button on the left site of the BER panel is set to "**Accum...**", the displayed BER is calculated from the total number of bit and total number of errors. Click in that button to toggle to "**Current**". In that case, the displayed BER is calculated with the last error counter reading.

Errors

This shows the number of errors detected by the BERT analyzer.

Bits

This shows the total number of transmitted bits.

Start BER Measurement

Pressing the "Start BER Measurement" button in the BER Measurement panel (Figure 43) will reset the bit and error counters and start the BER measurement. Once the "**Start**" button is pressed, the button "**Stop**" is enabled.

Stop

By clicking on the "**Stop**" button, the BER measurement is ended.

BERT Control

Insert Bit Error

The “Insert Bit Error” option of the BERT Control section (see Figure 44) allows to add a bit error in the data pattern.

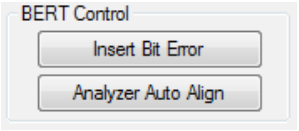

Figure 44 BERT Control

Analyzer Auto Align

The “**Analyzer Auto Align**” button is used for conducting a bit alignment of the BERT analyzer. For a comparison of the incoming pattern with the pattern in the analyzer, the clock of the TX (Transmitter) side of the DUT and the analyzer clock must be in phase. This is ensured by a common reference clock. When the received bits are not synchronized with the pattern of the analyzer, the computed BER will be very high. In this case, clicking on the “**Analyzer Auto Align**” button restarts the synchronization algorithm in the analyzer.

Sequencer

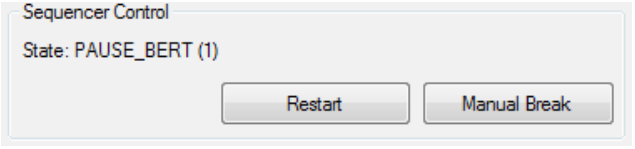

Figure 45 Sequencer Section

Stop/Start

With a click on “**Stop**” button, the running process is terminated and then the button is renamed to “Start”. Pressing “**Start**” will start again the sequence from the beginning. This functionality is only available when the Bitifeye DSGA is selected as BERT in the “Instrument Connection” dialog.

Restart

Pressing on the "**Restart**" button triggers a sequence restart on the instrument.

Manual Break

The "**Manual Break**" button allows to send manual break events to the instrument. When a sequence contains blocks that are conditionally looped (blocks that contain a manual break condition), sending a manual break results in a break from the loop in the instrument.

Unipro Test Mode

Unipro Script Generation

To operate in UniPro Test Mode it is necessary to replace the default scripts by UniPro scripts. These are generated in the "**UniPro Script Generator**" dialog.

From the "**Tools**",option in the menu click on **Unipro Script Generator...**" and the "**UniPro Script Generator**" dialog will open.

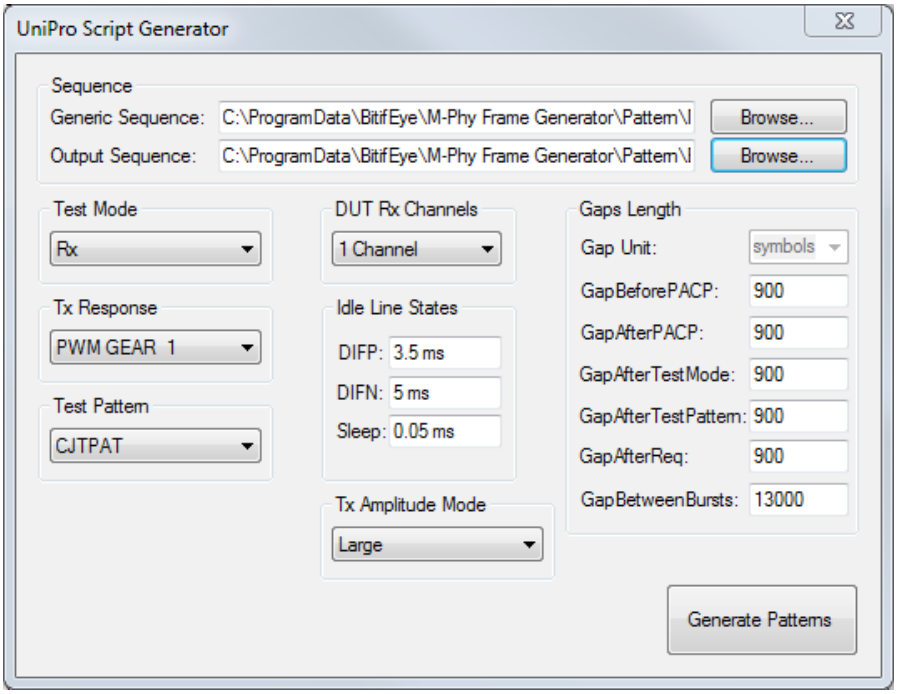

Figure 46 Unipro Script Generator Dialog

Here several properties can be selected:

Test Mode

Select the test type as:

- Rx or
- Tx

Tx Response

In Receiver tests, the DUT can be configured to transmit the response in high or low speed:

- PWM Gear 1: The DUT will transmit the signal in low speed PWM. This option must be selected for the setups that include the DSGA instrument as Error Detector (M8020A + DSGA).
- HS Gear 1-A, 1-B, ...,4-B: The DUT will transmit the signal in high speed. This option must be selected for the stand-alone M8020A setup.

Rx Configuration

In Transmitter tests, the DUT can be configured to receive the PACP packets in high or low speed.

- PWM Gear 1: The DUT will expect to receive the signal in low speed PWM. This option must be selected for the DSGA setup.
- HS Gear 1-A, 1-B, ...,4-B: The DUT will expect to receive the signal in high speed. This option must be selected for the M8020A setup.

Test Pattern

Chose between the two test patterns supported by the UniPro Adapter Layer:

- CJTPAT
- CRPAT

Tx Gear

Chose the transmitted gear for Tx mode

For Rx mode, the gear is selected in the **Timing Setup** dialog.

DUT Rx/Tx Channels

Select the number of channels to be tested from 1 to 4

Tx Amplitude Mode

The DUT can be configured to transmit with two different amplitude modes:

- Large
- Small

Select the desired amplitude mode. If both are selected different scripts will be generated for each mode.

Idle Line States

Specify the time of the different Idle signals

Gaps Length

Specify the length of the different GAPs that are used in the training sequence.

After pressing the “Generate Patterns” button all the scripts will be created.

When the dialog is closed, the default sequence is replaced in the Pattern/Sequence section of the main window. Now the sequence namesmake use of Wildcards.

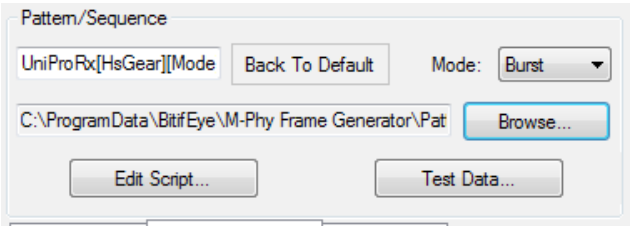

Figure 47 Unipro sequence name

Example: When running a receiver test for:

- HS Gear 1A
- in burst transmission mode
- large amplitude
- channel 1

The Unipro[Type][HsGear][Mode][Amplitude][Channel].seq sequence name will be replaced by:

- UniproRxGear1ABurstLargeData0.seq

Pattern Coding

In Unipro mode, the DUT is configured to Test Mode and Frame and Error counters requests are interleaved with the test pattern. Then the Frame Generator decodes the responses captured with the test equipment and calculates the BER.

This functionality is controlled through the "**Data Coding Converter**" dialog. From the "**Tools**" option in the menu click on "**Pattern Coding...**" and the "**Data Coding Converter**" dialog will open (see Figure 48).

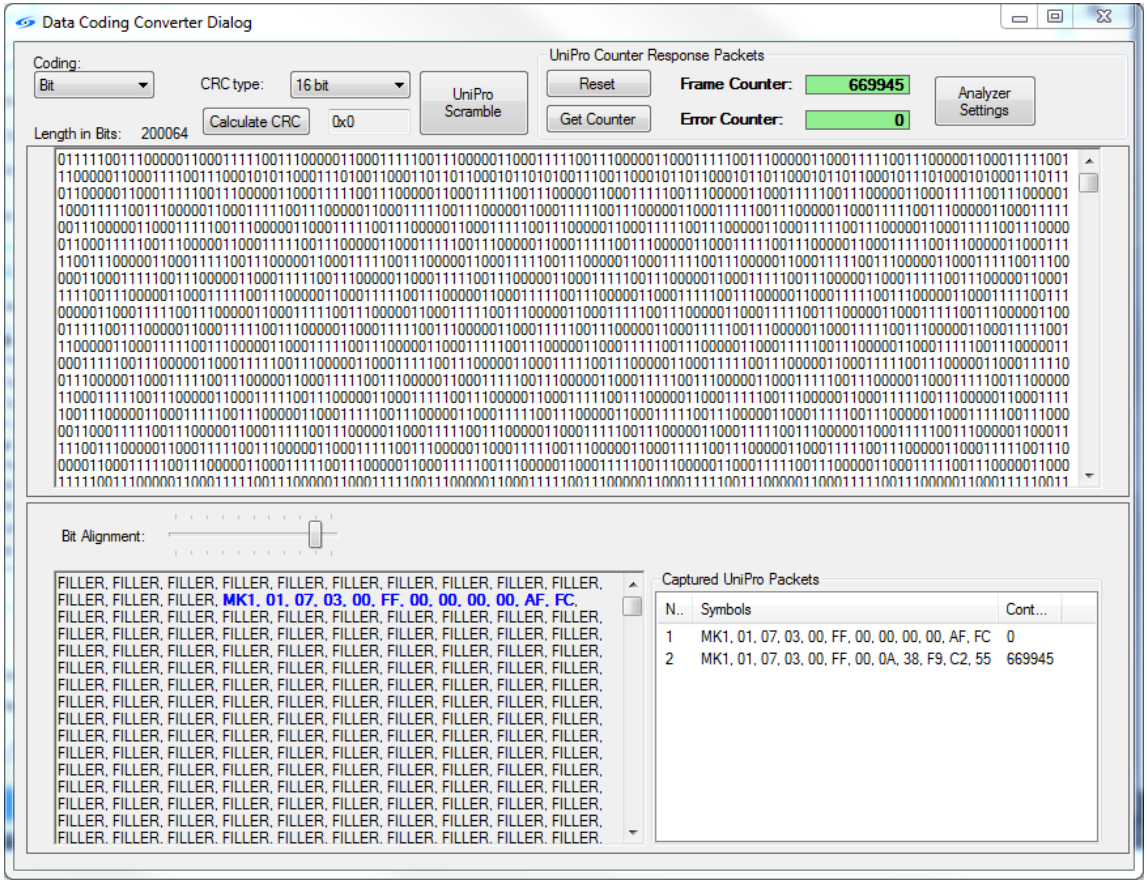

Figure 48 Data Coding Converter dialog

Analyzer Settings

First step, prior to start the measurement, is necessary to set the analyzer instrument by clicking on the “Analyzer Settings” button (see Figure 49).

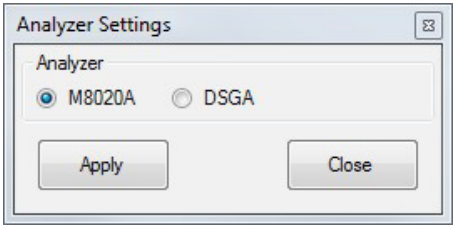

Figure 49 Analyzer Settings dialog

In Unipro Test Mode either the M8020A or the DSGA can be used as analyzer. The M8020A analyzer needs that t he DUT transmit the responses in HS Continuous mode. The DSGA can receive the DUT responses in PWM mode (Continuous or Burst).

For DSGA case, is necessary to specify a rough estimate of the data rate the DUT is responding with. The DSGA analyzer allows to select the compare mode as Differential or Single-Ended. The Single-Ended mode allows the user to connect the Tx- to the DSGA and Tx+ to the scope, to verify that the DUT is working by using the scope decoder.

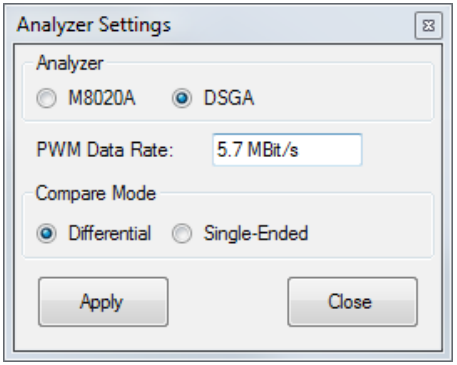

Figure 50 Analyzer Settings dialog for DSGA

Reset

A click on the "**Reset**" button will reset the DUT counters.

Get Counters

When clicking on the "**Get Counters**" button, the data captured by the analyzer will be shown in the output panel (the one on the top), and the Frame Counter and Error Counter values will be updated.

The panel on the bottom shows the decoded data. To see the correct symbols is necessary to adjust the alignment by using the Bit Alignment slide. Once the bit alignment is set properly, the Unipro Packets will be highlighted in blue (see Figure 48)

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