Keysight Logic and Protocol Analyzer Software (64-bit Application)

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Version 7.00.0206 (April 27, 2026)

Modifications

- Fix incorrect decode of some newer DDR5 RCD registers.
- Fix issues in DDR/LPDDR Setup Assistant and DDR/LPDDR Configuration Creator with handling of LPDDR5 2-bus-per-card setups.
- Fix defect in DDR/LPDDR Setup Assistant with code that figures out the middle of the signal swing. In some cases, the code was throwing a silent exception.
- Fix defect in DDR/LPDDR Post Process Compliance Tool that appeared with the handling of the Futureplus FS2675 interposer.
- Fix issue with eyescan setup for LPDDR6 in DDR/LPDDR Configuration Creator.

Additions

- Release initial version of ONFi SCA Viewer for decode and analysis of ONFi SCA (Separate Command Address) protocol.

Version 7.00.0194 (March 10, 2026)

Modifications

- Fix issue with DDR Setup Assistant when used with DDR5 system running UDIMM/DRAM 2N mode.
- Fix potential false positive with DDR Post-process Compliance Tool when analyzing DDR5 2-rank system running ODT commands to non-target rank.

Additions

- None

Version 7.00.0189 (January 25, 2026)

Modifications

- None

Additions

- Add support for LPDDR5 4-CS 315-ball BGA interposer.
- Add support for acquiring and processing 2 LPDDR5 busses on same LA card when the two busses share a common clock.

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Version 7.00.0184 (December 6, 2025)

Modifications

- Update references for LPDDR5 in DDR/LPDDR Post-Process Compliance Tool to be current with latest JEDEC released spec (version JESD209-5C).
- Fix issue in DDR/LPDDR Post-Process Compliance Tool where values set in “Set Limits From System Parameters” dialog would be lost when subsequently manually editing a limit value.
- Fix issue with custom .NET DLL physical address handling for LPDDR5 memory viewer. The Bank Group value was not being correctly passed on to the custom DLL.

Additions

- Add support for Futureplus FS2675 interposer.

Version 7.00.0180 (October 13, 2025)

Modifications

- Fix issue with how LPDDR6 listing decoder handles row address.
- Add symbols for CA and COMMAND0/1 labels for LPDDR6 configurations.

Additions

- Add support for LPDDR6 in DDR/LPDDR Memory Viewer.

Version 7.00.0172 (July 30, 2025)

Modifications

- Fix issue with DDR Setup Assistant handling of Futureplus FS2612 interposer.

Version 7.00.0170 (July 22, 2025)

Modifications

- Update export feature in Transaction Decode in DDR/LPDDR Memory Viewer to allow user to select to export either raw (RD/WR) data or computed data.
- Fix issue with LPDDR5 Listing Decoder with handling more than 2 CS pins in setup.

Additions

- Add support for Futureplus FS2612 interposer.
- Update all DDR tools to include initial support for DDR5 MRDIMM.
- New LPDDR6 Listing Decoder.
- Add LPDDR6 support in DDR/LPDDR Configuration Creator.

Version 7.00.0158 (June 11, 2025)

Modifications

- None

Additions

- Added support in all tools for capturing LPDDR5/5X at higher speeds (data rate >= 10GT/s).

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Version 7.00.0154 (May 5, 2025)

Modifications

- Update DDR Post Process Compliance Tool for DDR5:
    - Add additional tests for RD/WR timings needed to correctly handle upper speed bins (6800 and greater) for 3DS configurations.
    - Fix handling of some tests that were still using very small time values instead of clocks as a measurement basis.
- Fix issue with matching ACT/RD/WR/PRE commands for LPDDR4 in DDR/LPDDR Memory Viewer.
- Update DDR Setup Assistant for LPDDR5 to select better default sample positions for CS and CA.

Additions

- Added feature to DDR/LPDDR Memory Viewer to allow export of statistics in Performance tab.
- Added support for up to 19 row bits for LPDDR4 in both LPDDR listing decoder and DDR/LPDDR Memory Viewer.

Version 7.00.0147 (March 12, 2025)

Modifications

- Update DDR Post Process Compliance Tool for DDR5:
    - Add handling of RCRC and WCRC into calculations of parameters that are dependent on burst length.
    - Add additional tests for RD/WR timings needed to correctly handle upper speed bins (6800 and greater).
- Update LPDDR5 configuration files to include more trigger favorites.
- Add the “Validate CK/CS/CA sample positions” step into DDR Setup Assistant for LPDDR5. (This was previously only available for DDR5).

Additions

- None

Version 7.00.0142 (February 3, 2025)

Modifications

- Improve handling of selection of RDIMM 2N mode in both memory viewer and compliance tool when FP-FS2670 is used for probing. In this case, the Logic Analyzer capture follows UDIMM/DRAM 2N timing protocols.

Additions

- Add support in Viewscope for MXR B series models.
- Add support for 2N timings in DDR5 Trigger Utility.

Version 7.00.0139 (November 7, 2024)

Modifications

- Add handling of DDR5 2N timings to DDR Eyescan. This fixes a workaround that required using a different latency number in DDR Eyescan vs. the DDR Memory Viewer when the system was in a 2N mode.
- Fix an issue with DDR Setup Assistant in the initial threshold setup step when the probing solution was a probe with a clock divider.

Additions

- Support for LPDDR5 496-ball BGA interposer. Includes:
    - State configurations
    - DDR Setup Assistant support

Version 7.00.0136 (October 21, 2024)

Modifications

- Update install process to include missing prerequisite – fixes potential situation where install succeeds, but main LA app fails on startup.

Additions

- None

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Version 7.00.0132 (October 10, 2024)

Modifications

- In DDR/LPDDR Memory Viewer, show the only field in DDR5 mode registers 46 and 47 as a hex (not decimal) value.
- Fix defect with handling of BG in calls to user-defined physical address translation DLL.

Additions

- New DDR5 Trigger Utility to improve ease of use in setting up logic analyzer trigger specifications with DDR5, especially when probing with interposers that have a clock divider.
- Support for FP-FS2910A LPDDR5 LPCAMM interposer. Includes:
    - State configurations
    - DDR Setup Assistant support
    - LPDDR5 F-FS2910A Timing Config Creator to create custom configuration designed for timing mode

Version 7.00.0110 (July 26, 2024)

Modifications

- Fix defect with configuration files for DDR5 RDIMM interposers FP-FS2600 and FP-FS2603. There was only one PAR label, and there need to be two – PAR_R for capture of the rising edge and PAR_F for capture of the falling edge.

Additions

- New LPDDR5 features:
    - Several new compliance tests in the DDR/LPDDR Post Process Compliance Tool.
    - Add support for RFM single-bank commands in the DDR/LPDDR Memory Viewer.

Version 7.00.0104 (June 17, 2024)

Modifications

- Fix defect where incorrect states would be referenced in DDR/LPDDR Post Process Compliance Tool results with pass/fail tests and a DDR5 clock divided interposer.

Additions

- Update DDR5 tools to be current with JESD79-5C_v1.30.
    - Add compliance parameter information for speeds 6800 to 8800.
    - Update parameter definitions that change with enabling of PRAC.
    - Add additional compliance test, run when PRAC is enabled, for tRP when 9 or more banks are open.
    - Update other parameters as needed.
    - Update mode register decoding in DDR/LPDDR Memory Viewer.

Version 7.00.0097 (May 11, 2024)

Modifications

- Improve measurement of clock frequency in DDR/LPDDR Memory Viewer.
- Enhance measurement accuracy of many parameters in DDR5 and LPDDR5 where small time values may be involved. In these cases, convert the time value to the equivalent number of clocks to make the measurement.
- Fix defect recently introduced into Post-process compliance tool with handling LPDDR4 traces.

Version 7.00.0091 (April 20, 2024)

Modifications

- Fix issue in DDR/LPDDR Post Process Compliance Tool with tpbr2pbr parameter in LPDDR5. The measurement would not work correctly if the system clock paused in the middle of the measurement.
- Update DDR Setup Assistant to reflect that the new “Validate Command/Address Setup” step is no longer in a beta state.

Additions

- Add support in DDR/LPDDR Post Process Compliance Tool for Enhanced WCK Always On Mode in LPDDR5.

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Version 7.00.0086 (March 20, 2024)

Modifications

- In DDR/LPDDR Post process Compliance Tool, improve display of limit value in the results tab when the limit varies by clock speed.
- Fix issue with display of refresh per bank for LPDDR4 in memory viewer. (TTS-72661)
- Remove DDR5 and LPDDR5 tests from Real-time Compliance Tool. They are no longer supported.

Additions

- Support in all tools for protocol and measurement changes for LPDDR5X.
- Many new and updated LPDDR5/5X compliance measurements.
- Support in all tools for DRFM for LPDDR5/5X.
- Two new features in the Transaction Decode tab in the DDR/LPDDR Memory Viewer:
    - Allow exporting a range of transactions (rather than the entire trace).
    - Allow exporting the read/write data along with the transactions.

Version 7.00.0050 (October 6, 2023)

Modifications

- Many new and updated DDR5 compliance measurements.
- Fix issue with DDR Setup Assistant and the FP-FS2600. The selections available on the initial DDR Setup Assistant page were not working correctly.
- Fix bug with 16861A and transitional timing mode. Storage qualification options were not available in the trigger dialog.

Additions

- Add support for LPDDR4 123-ball interposer.

Version 7.00.0040 (June 16, 2023)

Modifications

- Fix crash when saving a configuration file with a DDR/LPDDR Memory Viewer on the workspace, and particular data in the viewer. (TTS-54399)
- Removed the Logic Update Tool from the install process. It is obsolete.
- Fix problem with DDR/LPDDR Memory Viewer when computing GDDR6 data.
- Add new test to DDR/LPDDR Post-process Compliance Tool, measuring precharge to refresh (tRP).
- Fix defect in DDR/LPDDR Post-process Compliance Tool – exception when trying to load a saved project containing test results. (CSG-106044)

Version 7.00.0031 (April 19, 2023)

Modifications

- Fix issue with DDR/LPDDR memory viewer not correctly detecting clock speed changes in all cases.
- Fix for DDR5 in DDR/LPDDR memory viewer and DDR/LPDDR post-process compliance tool – correctly handle non-target ODT commands issued to a rank that is currently in powerdown mode.
- Add support in all tools for DDR5 solution consisting of FP-FS2600 DDR5 RDIMM interposer combined with FP-FS2605 DDR5 RDIMM satellite interposer.

Version 7.00.0028 (March 28, 2023)

Modifications

- Update to final version of licensing code.

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Version 7.00.0026 (March 16, 2023)

Modifications

- Fix several LPDDR4 measurements in DDR/LPDDR Post Process Compliance Tool. (CSG-106044)
- Enhancements to DDR Setup Assistant:
    - Recognize and handle 2N timing in DDR5 for probes that do *not* have a clock divider and set 2N mode in all tools and viewers that require this setting.
    - Improve default values for prepend text for DDR5 configuration file load step.
    - Modify wording in the configuration load step to improve clarity.
    - New feature (beta at this time) to allow user running DDR Setup Assistant to automatically launch the DDR/LPDDR Post Process Compliance Tool to run the steps needed to validate CK/CS/CA tuning. This feature is available only for DDR5 setup at this time, but it will be added for other DDR/LPDDR types when the feature moves out of the beta phase.
- When the module name provides a hint, pre-select the DDR/LPDDR type selection when starting the DDR/LPDDR Post Process Configuration Tool.
- Update to latest version of licensing code.

Additions

- Add beta feature in DDR Configuration Creator that allows users to create configurations for the ONFi memory viewer.

Version 7.00.0022 (January 27, 2023)

Modifications

- Add support for decode of MRR response for LPDDR5 even when DUT is changing system clock speeds.
- Updates and fixes to DDR5 configuration files for FP-FS2601, FP-FS2670, and BGA probes.
- Add configuration files and DDR Setup Assistant support for FP-FS2611.
- Fix defect in DDR Memory Viewer with handling of MRS commands when user has selected that there is only one active BG bit.
- Fix potential crash in DDR and ONFi Memory Viewers.
- Several corrections to DDR5 protocol compliance: 1) WR->RDA test updated to measure only when BG and bank match. 2) Update calculation of tRRD_L parameter value to be a clock (not time) value. This increases the accuracy of the measurement. 3) Fix WRToRD type tests to exclude measuring when the WR is a WR w/AP.
- Updates/fixes for DDR Setup Assistant's handling of DDR5 probes that are designed for use above 5GT/s (i.e., those with active clock divider circuitry). DDR Setup Assistant now correctly handles setting of CK/CS/CA sample positions when target is running in 1N or 2N modes.
- Fix to handling of "empty" bits – signals that are not probed but are expected by various tools to be assigned to different labels – in DDR Configuration Creator.

Additions

- Add configuration files and DDR Setup Assistant support for FP-FS2611.

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Version 7.00.0013 (September 19, 2022)

Modifications

- Add configuration files and support in DDR Setup Assistant for FP-FS2660 and FP-FS2670 DDR5 RDIMM interposers.
- Fix problems with “Reconstructed Signals” window in DDR5 setups with probing solution that has a clock divider (FP-FS2670 and BGA 78-ball w/ clock divider).

Version 7.00.0008 (August 22, 2022)

Modifications

- Update all DDR/LPDDR tools to be current with latest LPDDR4 spec – JESD209-4D. This includes handling decode of new Refresh Management commands.
- Fix problems with handling of DDR5 MRR command in the DDR/LPDDR memory viewer. (CSG95192)

Version 7.00.0007 (July 19, 2022)

Modifications

- Fix issue with DDR5 4000 limits file that resulted in error when trying to edit limit values.
- Fix WRToRDASameBankGroup test. It should be to the same *bank*, not the same *bank group*. Updated it to work on bank, not bank group. (CSG-90176)
- Add configs and setup assistant support for Blossom x16 102-ball DDR5 probe.
- Add configs for FP-FS2603 DDR5 RDIMM CA-only probe.
- Fix tRFC1 and tRFC2 tests for DDR5 to exclude PDX from measurements, as per recent spec change.
- Update algorithm in DDR Setup Assistant for LPDDR5 eye placements for CK/CS/CA signals.
- Add new symbols for LPDDR5 configurations that represent either a MWR or Write.
- Simplify LPDDR5 real-time compliance trigger specs that measure to MWR or Write.
- For LPDDR5 compliance, change references to CAS latency and CAS write latency to read latency and write latency, respectively.
- Change default for bank group organization for LPDDR5 “Set Limits from System Parameters” dialog. It had been 8B mode, and now defaults to Bank Group.
- Update DDR5 parameters for lower speed bins (3200 to 4800), in both post-process compliance and real-time compliance tools, to match latest draft spec.

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FLEE (Fast Light Expression Evaluator): https://github.com/mparlak/Flee

Grammatica: https://grammatica.percederberg.net/index.html

VXPLib: https://vxplib.sourceforge.net/index.html