M8000 Series of BER Test Solutions

M8020A High-Performance BERT

M8040A High-Performance BERT 64 GBd

M8050A High-Performance BERT 120 GBd

KEYSIGHT

USER GUIDE

Notices

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User Documentation

User documentation includes comprehensive information on features that may impact the secure deployment, use, and decommissioning of our products. This includes details on exposed network ports, the use of cryptography and authentication, and firmware security settings, if necessary.

Obtaining Source Code

This product uses open source packages. To the extent required by the applicable open source license(s), Keysight makes source code available upon request. To request source code, contact Keysight Support at www.keysight.com/main/support.jspx.

Safety Summary

The following general safety precautions must be observed during all phases of operation of this instrument. Failure to comply with these precautions or with specific warnings or operating instructions in the product manuals violates safety standards of design, manufacture, and intended use of the instrument. Keysight Technologies assumes no liability for the customer's failure to comply with these requirements. Product manuals are provided with your instrument on CD-ROM and/or in printed form. Printed manuals are an option for many products. Manuals may also be available on the Web. Go to www.keysight.com and type in your product number in the Search field at the top of the page.

General

This product is a Safety Class 1 instrument (provided with a protective earth terminal). The protective features of this product may be impaired if it is used in a manner not specified in the operation instructions.

All Light Emitting Diodes (LEDs) used in this product are Class 1 LEDs as per IEC 60825-1.

Environment Conditions

This instrument is intended for indoor use in an overvoltage category II, pollution degree 2 environment. It is designed to operate at a maximum relative humidity of 95% and at altitudes of up to 2000 meters.

Refer to the specifications tables for the ac mains voltage requirements and ambient operating temperature range.

Before Applying Power

Verify that all safety precautions are taken. The power cable inlet of the instrument serves as a device to disconnect from the mains in case of hazard. The instrument must be positioned so that the operator can easily access the power cable inlet. When the instrument is rack mounted the rack must be provided with an easily accessible mains switch.

Ground the Instrument

To minimize shock hazard, the instrument chassis and cover must be connected to an electrical protective earth ground. The instrument must be connected to the ac power mains through a grounded power cable, with the ground wire firmly connected to an electrical ground (safety ground) at the power outlet. Any interruption of the protective (grounding) conductor or disconnection of the protective earth terminal will cause a potential shock hazard that could result in personal injury.

Do Not Operate in an Explosive Atmosphere

Do not operate the instrument in the presence of flammable gases or fumes.

Do Not Remove the Instrument Cover

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made only by qualified personnel.

Instruments that appear damaged or defective should be made inoperative and secured against unintended operation until they can be repaired by qualified service personnel.

External Connections

Any other instruments connected to this instrument shall be approved to a suitable safety standard and must include reinforced insulation from hazardous voltages, in particular mains.

Safety Symbols

Table 1 Safety Symbols

Symbol	Description
	Indicates warning or caution. If you see this symbol on a product, you must refer to the manuals for specific Warning or Caution information to avoid personal injury or damage to the product.
	Frame or chassis ground terminal. Typically connects to the equipment's metal frame.
	KC is the Korean certification mark to demonstrate that the equipment is Class A suitable for professional use and is for use in electromagnetic environments outside of the home.
	Contains parts or assemblies susceptible to damage by electrostatic discharge (ESD). Use electrostatic discharge protective handling procedures to avoid malfunctions or potential damage to the instruments.
40	Indicates the time period during which no hazardous or toxic substance elements are expected to leak or deteriorate during normal use. Forty years is the expected useful life of the product.
	The RCM Mark is a compliance mark to the ACMA (Australian Spectrum Management Agency). This indicates compliance with all Australian EMC regulatory information.
C US	Indicates that the product was tested and has met the certification requirements for electrical, plumbing and/or mechanical products.

Symbol	Description
CE CAN ICES/NMB-001(A) ISM GRP 1-A	The CE mark is a registered trademark of the European Community. This CE mark shows that the product complies with all the relevant European Legal Directives. CAN ICES/NMB-001(A) - This ISM device complies with the Canadian ICES-001(A). Cet appareil ISM est conforme a la norme NMB-001(A) du Canada. ISM GRP 1-A - This is an Industrial Scientific and Medical (ISM) Group 1 Class A product.
	This symbol on all primary and secondary packaging indicates compliance to China standard GB 18455-2001.

Compliance and Environmental Information

Table 2 Compliance and Environmental Information

Safety Symbol	Description
	The crossed out wheeled bin symbol indicates that separate collection for waste electric and electronic equipment (WEEE) is required, as obligated by DIRECTIVE 2012/19/EU and other National legislation. See http://about.keysight.com/en/companyinfo/environment/takeback.shtml to understand your Trade in options with Keysight in addition to product takeback instructions.

About This Guide

Here is how the information in this document is organized.

Introduction

This chapter provides an overview of this manual.

Know Your Hardware

This chapter provides an information on the various modules of M8020A/M8040A/M8050A, their setup and the provided accessories.

Exploring M8070B User Interface

This chapter describes the M8070B user interface and the functionality provided by its common GUI elements.

Configuring Your System

This chapter describes how to configure the M8020A/M8040A/M8050A system using the Module View, Group View and System View.

Setting up Generator

This chapter provides information on settings provided by the M8020A/M8040A/M8050A Generator.

Setting up Analyzer

This chapter provides information on settings provided by the M8020A/M8040A/M8050A Analyzer.

Setting up Patterns

This chapter describes the functionality provided by the M8070B Pattern Editor and Sequence Editor.

Working with Measurements

This chapter describes the setup, execution, monitoring and results of the measurements supported by M8070B system software.

Utilities

This chapter describes the utilities provided by the M8070B system software.

Licenses

This chapter provides information on the M8020A/M8040A/M8050A and M8070B licenses and their installation procedure.

Appendix

This chapter provides information about basic troubleshooting and factory patterns.

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KEYSIGHT TECHNOLOGIES

Overview

M8020A High-Performance BERT

The Keysight J-BERT M8020A high-performance BERT enables fast, accurate receiver characterization of single-and multi-lane devices running up to 16 or 32 Gb/s.

With today's highest level of integration, the M8020A streamlines your test setup. In addition, automated in situ calibration of signal conditions ensures accurate and repeatable measurements.

Figure 1 Typical base M8020A instrument configuration

Key Features

- Data rates up to 8.5 and 16 Gb/s expandable to 32 Gb/s
- 1 to 4 BERT channels in a 5-slot AXIe chassis
- Integrated and calibrated jitter injection: RJ, PJ1, PJ2, SJ, BUJ, sinusoidal level interference (common-mode and differential-mode), SSC (triangular and arbitrary, residual) and Clock/2
- 8 tap deemphasis, positive and negative
- Integrated and adjustable Intersymbol Interference
- Interactive link training for PCI Express
- Built-in clock recovery and equalization
- All options and modules are upgradeable

M8020A Applications

The J-BERT M8020A is designed for R&D and test engineers who characterize and verify compliance of chips, devices, boards and systems with serial I/O ports up to 16 Gb/s and 32 Gb/s in the consumer, computer, mobile computing, data center and communications industry.

The J-BERT M8020A can be used to test popular serial bus standards, such as PCI Express®, SATA/SAS, DisplayPort, USB Super Speed, MIPI M-PHY, SD UHS-II, Fibre Channel, QPI, memory buses , backplanes, repeaters, active optical cables, Thunderbolt, 10/40 GbE/SFP+/QSFP, 100 GbE/CFP2.

M8040A High-Performance BERT

The Keysight Technologies M8040A is a highly integrated BERT for physical layer characterization and compliance testing.

With support for pulse amplitude modulation 4-level (PAM4) and non-return-to-zero (NRZ) signals, and symbol rates up to 64 GBd (corresponds to 112 Gbit/s) it covers all flavors of the emerging 400 GbE and CEI-56G standards.

The M8040A BERT´ s true error analysis provides repeatable and accurate results, optimizing the performance margins of your devices.

Figure 2 Typical M8040A instrument configuration

Key Features

The M8040A provides the following features:

- Data rates from 2 to 32 and 64 Gbaud
- PAM4, PAM3 and NRZ selectable from user interface
- Built-in 5 tap transmitter FFE with multiple presets to compensate loss
- Integrated and calibrated jitter injection: RJ, LF and HF PJ (multi-tone, sinusoidal), BUJ, clk/2 jitter, sRJ, rSSC, and SSC (spread spectrum clocking)
- Forward Error Correction (FEC) encoding and error insertion for testing DUTs with FEC decoder
- Two pattern generator channels per module to emulate aggressor lane
- Linearity tests with adjustable PAM4 and PAM3 levels
- Interactive link training 2.5/5/8/16/ 32/64 GT/s PCI Express®
- Interactive link training for USB 3.2, 5 Gb/s and 10 Gb/s, x1 and x2
- New SSC clock switch profile supported according to CTS V1.02
- SKP OS filtering for 2.5/ 5/ 8/ 16/ 32 64 GT/s PCI Express® and SKP OS filtering for USB 3.2
- PCIe pre-coder support
- USB4 Version 2.0 pre-coder and scrambler support
- ALIGN filtering for SATA 3G / 6G and SAS 3G / 6G/ 12G
- Short connections to the DUT with remote heads for the pattern generator
- True PAM4 error detection in real-time for low BER levels
- Built-in and adjustable equalization to re-open closed eyes
- Integrated clock recovery and control of external clock recovery units N1076A/B, N1077A, N1078A
- RI and SI level interference injection via M8054A interference source for M8194A/95A/96A AWG
- Graphical user interface and remote control via M8000 system software
- Error distribution analysis to debug burst error conditions, real-time
- Reference clock multiplier support with SSC extended to 64 Gbaud

M8040A Applications

The M8040A is designed for R&D and test engineers who characterize chips, devices, transceiver modules and sub-components, boards and systems with serial I/O ports operating with data rates up to 32 GBd and 64 GBd in the data center and communications industries.

The M8040A can be used for receiver (input) testing for many popular interconnect standards, such as:

- IEEE 802.3bs 400 and 200 Gigabit Ethernet (200GAUI, 200GBASE, 400GAUI, 400GBASE)
- IEEE 802.3bj 100 Gigabit Ethernet
- IEEE 802.3cd 50, 100 and 200 Gigabit Ethernet
- IEEE 802.3ck 400 Gigabit Ethernet
- OIF CEI - 56G and -112G (NRZ and PAM4 versions)
- 25G and 50G PON
- PCI Express 64/32/16/8/5/2.5 GT/s
- CCIX
- SAS
- USB 3.2, USB4 and USB4 Version 2.0
- Thunderbolt 3/4
- DisplayPort 2.1
- MIPI M-PHY Gear 5
- 64G/112G Fiber Channel
- InfiniBand-HDR and NDR
- Proprietary interfaces for chip-to-chip, chip-to-module, backplanes, repeaters, and active optical cables, operating up to 64 Gbaud.

M8050A High-Performance BERT 120 GBd

The Keysight M8050A high-performance bit error ratio tester (BERT) enables accurate characterization of receivers used in next-generation data center networks and server interfaces. With uncompromised signal integrity, support for NRZ, PAM4, PAM6, and PAM8 signals, and data rates up to 120 GBd, the flexible architecture of the M8050A supports 1.6T path finding as well as other leading-edge technologies.

The M8050A high-performance BERT is one part of the Keysight M8000 Series of BER test solutions. It can be combined with other hardware and software of the M8000 Series.

The M8050A is a modular instrument which supports the following modules:

- M8042A Pattern Generator Module
- M8043A Error Analyzer Module
- M8009A Clock Module
- M8058A/M8059A Remote Head for M8042A Pattern Generator
- M8052A Remote Head for M8043A Error Analyzer

M8050A being a modular product includes different sets of modules which are hosted in an AXI chassis. Each module and its features have their own license. You need to install these options in your instrument in order to use the modules or features. For details, refer to the chapter Licenses on page 823. However, if you have ordered M8050A-BU2/BU3/BU4/BU5, no license is required.

For details on the features and hardware components of each of the above mentioned modules, refer to *M8050A Getting Started Guide*.

Figure 3 Typical M8050A instrument configuration

Key Features

- M8042A Pattern Generator:
  - Symbol rates from 2 to 120 GBd
  - Line coding: NRZ, PAM3, PAM4, PAM6, and PAM8
  - Built-in seven tap de-emphasis for improved channel loss compensation
  - Transition time at < 5 ps and < 100 fs root mean square (RMS) intrinsic random jitter
  - Jitter injection integrated and calibrated for receiver tolerance testing RJ, PJ1, PJ2, BUJ, sRJ, and clk / 2
- M8043A Error Analyzer Module:
  - Symbol rates from 2 to 64.4 GBd
  - Line coding: NRZ, and PAM4
  - Built-in 16-tap FFE for improved channel loss compensation
  - Built-in CTLE and 256-tap FIR filter improved channel loss compensation
  - Flexible solution with software license upgradeable functionality

M8050A Applications

The M8050A helps engineers design and characterize chips, devices, transceiver modules, sub-components, boards, and systems. Quickly test serial I/O ports operating at data rates up to 120 GBd across the server, computing, data center, and communication industries. Combining the M8050A BERT with a Keysight UXR-Series 80 GHz oscilloscope gives you a full 1.6T receiver and transmitter test solution to assess your Ethernet systems.

Document History

Table 3 Document History

Edition	Description
Edition 1.0, Dec 2018	Edition 1.0 of the M8000 Series User Guide is in accordance to the M8070B version 6.0.
Edition 2.0, May 2019	Edition 2.0 of the M8000 Series User Guide is in accordance to the M8070B version 6.5.
Edition 3.0, Oct 2019	Edition 3.0 of the M8000 Series User Guide is in accordance to the M8070B version 6.7.
Edition 3.3, April 2020	Edition 3.3 of the M8000 Series User Guide is in accordance to the M8070B version 7.0.
Edition 3.6, June 2020	Edition 3.6 of the M8000 Series User Guide is in accordance to the M8070B version 7.1.
Edition 3.7, July 2020	Edition 3.7 of the M8000 Series User Guide is in accordance to the M8070B version 7.2.
Edition 4.1, Feb 2021	Edition 4.1 of the M8000 Series User Guide is in accordance to the M8070B version 7.5.
Edition 5.0, April 2021	Edition 5.0 of the M8000 Series User Guide is in accordance to the M8070B version 8.0.
Edition 6.0, Nov 2021	Edition 6.0 of the M8000 Series User Guide is in accordance to the M8070B version 8.5.
Edition 7.0, April 2022	Edition 7.0 of the M8000 Series User Guide is in accordance to the M8070B version 9.0 and M8042A initial release.
Edition 8.0, July 2022	Edition 8.0 of the M8000 Series User Guide is in accordance to the M8070B version 9.1.
Edition 9.0, Oct 2022	Edition 9.0 of the M8000 Series User Guide is in accordance to the M8070B version 9.5.
Edition 10.0, Dec 2022	Edition 10.0 of the M8000 Series User Guide is in accordance to the M8070B version 9.5.1.
Edition 11.0, April 2023	Edition 11.0 of the M8000 Series User Guide is in accordance to the M8070B version 10.0.
Edition 12.0, July 2023	Edition 12.0 of the M8000 Series User Guide is in accordance to the M8070B version 10.1 and M8043A initial release.
Edition 13.0, Nov 2023	Edition 13.0 of the M8000 Series User Guide is in accordance to the M8070B version 10.5, M8042A 3.5 and M8043A 3.5 release.

Edition	Description
Edition 14.0, April 2024	Edition 14.0 of the M8000 Series User Guide is in accordance to the M8070B version 11.0.
Edition 15.0, May 2024	Edition 15.0 of the M8000 Series User Guide is in accordance to the M8070B version 11.0 Patch2 and M8042A V4.0.
Edition 16.0, Sept 2024	Edition 16.0 of the M8000 Series User Guide is in accordance to the M8070B version 11.5 and M8047C PCI Express Re-driver.
Edition 17.0, Dec 2024	Edition 17.0 of the M8000 Series User Guide is in accordance to the M8070B version 11.6, M8042A V4.5 and M8043A 4.5.
Edition 18.0, Mar 2025	Edition 18.0 of the M8000 Series User Guide is in accordance to the M8070B version 12.0, M8042A V5.0 and M8009A V5.0.
Edition 18.1, June 2025	Edition 18.1 of the M8000 Series User Guide is in accordance to the M8070B version 12.0.150.6.
Edition 18.2, July 2025	Edition 18.2 of the M8000 Series User Guide is in accordance to the M8043A V5.5.
Edition 19.0, Sept 2025	Edition 19.0 of the M8000 Series User Guide is in accordance to the M8070B 12.5 and M8042A V5.5.
Edition 20.0, Mar 2026	Edition 20.0 of the M8000 Series User Guide is in accordance to the M8070B 13.0 and M8042A V6.0.
Edition 20.1, June 2026	Edition 20.1 of the M8000 Series User Guide is in accordance to the M8070B 13.1.

Related Documents

Table 4 Related Documents

Document Part No.	Document Title
M8000-91B01	M8020A Start Here
M8000-91B03	M8040A Start Here
M8000-91B20	M8050A Start Here
M8000-91B04	M8000 Series Tips for Preventing Damage
M8000-91B05	M8000 Series Installation Guide
M8000-91B06	M8020A Getting Started Guide
M8000-91B07	M8040A Getting Started Guide

Document Part No.	Document Title
M8000-91B21	M8050A Getting Started Guide
M8000-91B08	M8000 Series BER Test Solutions User Guide
M8000-91B09	M8000 Series BER Test Solutions Programming Guide
M8000-91B14	M8000 Series Plugins Getting Started Guide
M8000-91B10	M8000 Series Advance Measurement Package User Guide
M8000-91B11	M8000 Series Error Distribution Analysis Package User Guide
M8000-91B15	M8070ISIB Adjustable ISI Package for M8000 Series User Guide
M8000-91B16	M8070OBLT Out-of-Band Link Training Package User Guide

Additional Documents

- http://www.keysight.com/find/M9506A for 5-slot chassis related documentation.
- http://www.keysight.com/find/M9502A for 2-slot chassis related documentation.
- http://www.keysight.com/find/M8195A for M8195A Arbitrary Waveform Generator related documentation.
- http://www.keysight.com/find/M8196A for M8196A Arbitrary Waveform Generator related documentation.
- http://www.keysight.com/find/M8194A for M8194A Arbitrary Waveform Generator related documentation.
- http://www.keysight.com/find/M8100 for M8100 Series Arbitrary Waveform Generator related documentation.

Abbreviations used in this Document

Table 5 Abbreviations

Abbreviation	Extended Form
AXIe	AdvancedTCA Extensions for Instrumentation and Test
AWG	Arbitrary Waveform Generator
BER	Bit Error Ratio
CDR	Clock Data Recovery

Abbreviation	Extended Form
CTLE	Continuous-Time Linear Equalizer
DUT	Device Under Test
ESD	Electrostatic Discharge
ESM	Embedded System Module
GB	Gigabyte
GUI	Graphical User Interface
J-BERT	Jitter-Bit Error Ratio Tester
LED	Light-Emitting Diode
MB	Megabyte
MIPI	Mobile Industry Processor Interface
PC	Personal Computer
PCIe	Peripheral Component Interconnect Express
PLL	Phase Locked Loop
PRBS	Pseudorandom Binary Sequence
PXI	PCI eXtensions for Instrumentation
R & D	Research & Development
SAS	Serial Attached SCSI
SATA	Serial Advanced Technology Attachment
SCPI	Standard Commands for Programmable Instruments
SMA	SubMiniature Version A
SSC	Spread Spectrum Clock
TCP	Transmission Control Protocol
USB	Universal Serial Bus
VCO	Voltage Controlled Oscillator

M8000 Series of BER Test Solutions
User Guide

2 Know Your Hardware

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KEYSIGHT TECHNOLOGIES

M8020A Overview

The Keysight's J-BERT M8020A High-Performance BERT is a modular instrument which supports the following modules:

- M8041A high-performance BERT generator-analyzer-clock 8/16 Gb/s
- M8051A high-performance BERT generator-analyzer 8/16 Gb/s.
- M8062A 32Gb/s Front-end for J-BERT M8020A High-Performance BERT
- In addition to above J-BERT modules, it also supports M8194A, M8195A, and M8196A Arbitrary Waveform Generator modules. Details of these modules can be found at
  - www.keysight.com/find/M8194A
  - www.keysight.com/find/M8195A
  - www.keysight.com/find/M8196A

M8020A being a modular product includes different sets of modules which are hosted in an AXI chassis. Each module and its features have their own license. You need to install these options in your instrument in order to use the modules or features. For details, refer to the chapter Licenses on page 823. However, if you have ordered M8020A-BU1, no license is required.

The M8041A module must be installed in slots 1 through 3 in the AXIe chassis unless the M9536A AXIe Embedded Controller is installed. The following configurations are possible in an M9505A 5-slot chassis:

- **1 or 2-channel, 16 Gb/s -** (1) M8041A
- **3 or 4-channel, 16 Gb/s -** (1) M8041A + (1) M8051A
- **1-channel, 32 Gb/s (Pattern Generator only or full BERT) -** (1) M8041A + (1) M8062A
- M8194A/M8195A/M8196A module can be added into the 5 slot module

Additionally, the M8062A and M8194A/M8195A/M8196A modules can be installed and operated in a 2 slot frame.

NOTE

In case an AWG module (M8194A/M8195A/M8196A) and/or an IFS module (M8053A/M8054A) is used in a combined system with M8020A modules, ensure that the AWG and IFS modules are mounted in a slot number higher than clock generating M8020A module (M8041A) in the AXIe chassis. In other words, the AWG and IFS module always has to be mounted above the M8041A module in the chassis.

Also note that the M8050A clock generation modules (M8009A + M8042A) are not supported with M8100 series AWG modules (M8008A + M8198A/M8199A/M8199B) in an M8070B hardware setup, as only one set of clock modules can be used in a chassis. However, the interference source module (M8053A/M8054A) can be used together with the M8050A clock generation modules. In this configuration, the interference source module must be mounted above the M8050A clock generation module in the chassis.

For details on the features and hardware components of each of the above-mentioned modules, refer to M8020A Modules on page 50.

M9505A AXIe Chassis

The M9505A AXIe Chassis is a modular instrument chassis that supports complex and high density testing. The chassis provides slots for installing multiple AXIe based instrument modules such as the M8041A, M8042A, M8043A, M8045A, M8046A, M8051A, M8062A and M8009A modules. Besides providing a frame for the installation of these instrument modules, the M9505A AXIe Chassis also provides power, a cooling system, a PCIe Gen2 local data bus, a Gigabit LAN interconnect, and a cabled USB (USB option required) and PCIe connection for external host computer connectivity.

The following model of the M9505A AXIe Chassis supports the M8020A modules:

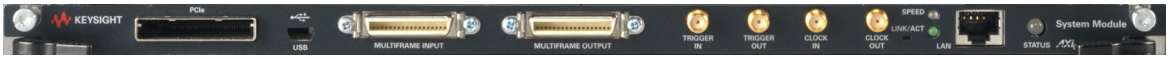
- M9505A - a 5-Slot AXIe chassis

NOTE The USB connection is recommended when using a laptop or desktop PC as an external controller. The PCIe connection is recommended for use with a desktop PC as an external controller only.

Refer to the *Keysight M9505A AXIe Chassis Startup Guide* to get detailed information about the AXIe chassis.

AXIe Embedded System Module (USB ESM)

The bottom slot of the AXIe chassis is reserved for the Embedded System Module (ESM) which is factory-installed. The ESM has a USB 2.0 interface as well as a PCIe x8, Gen1 and Gen2 compliant interface to connect an external host computer to the chassis. The following figure shows the PCIe Port and USB Port in ESM.



The ESM:

- runs the chassis embedded operating system which manages all internal tasks and communications.
- tracks inserted modules and manages power requirements.
- monitors chassis temperature and controls variable-speed chassis fans.
- monitors module sensors and reports component failures to a system log.
- acts as a Gigabit Ethernet switch; forwards frames along the backplane.
- connects an external host computer to the chassis.
- synchronizes timing across all modules through the Keysight Trigger Bus, using an internal or external clock source.
- LAN connector on AXIe ESM is not used. Only use LAN connection on the host computer.
- Either the PCIe (desktop only) or USB (desktop or laptop) port can be used in this ESM but not both simultaneously. When you use the PCIe port, the USB port is automatically disabled until the PCIe port is no longer in use.

M9506A AXIe Chassis

The Keysight M9506A AXIe chassis is a modular instrument chassis fully compatible with the AXIe Wide PCIe specification. It allows multiple application-specific instrument modules to share a common chassis frame, power supply, cooling system, PCI Express (PCIe) x16 Generation (Gen) 3 backplane, Gigabit LAN hub, local bus for module-to-module signaling, and host PC connections. The full rack chassis provides five general purpose peripheral slots that accept 1U AXIe instrument modules.

Additional features include:

- Up to 300 W per slot power
- Five AXIe Wide compliant slots
- PCIe x16 Gen 3 Backplane allows module to module communication
- Default PCIe configuration merges both cable ports to one Gen 3 x16 PCIe Cable Port.
- Open AXIe Zone 3 for custom use (cable access, analog backplane, etc.)
- Thunderbolt™ 3 Connection Port[1]
- Cascaded PCIe for multiple chassis systems
- Parallel and Star Triggering
- Push-pull fan system for quieter operation

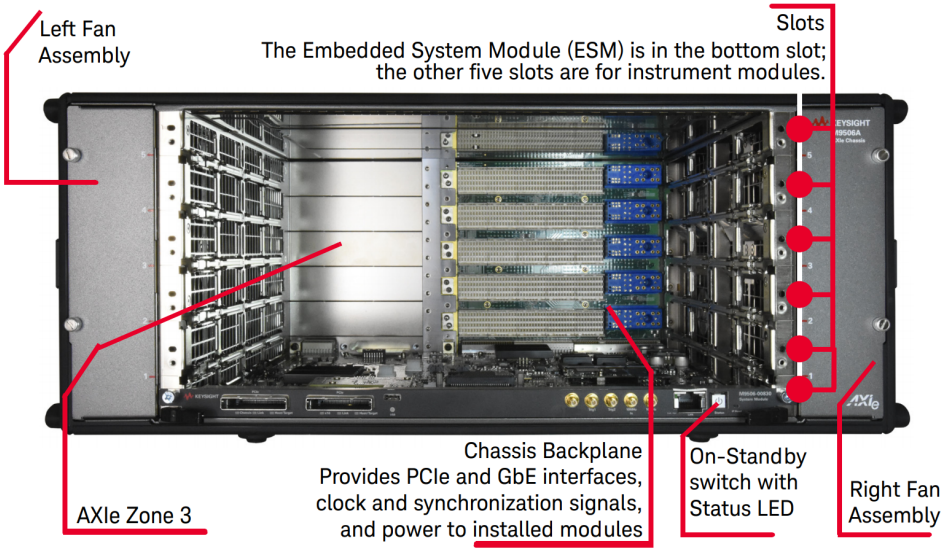
The chassis includes a half-height Embedded System Module (ESM) that manages chassis functions. The ESM provides all ATCA (Advanced Telecommunications Computing Architecture) shelf manager functions, plus these AXIe extensions:

- Host PC connectivity (Gen 3 PCIe x8/x16, Thunderbolt 3, Ethernet)
- Sources timing signals (CLK100, SYNC, and FCLK)
- Routes STRIG (Star Trigger) to instruments through the backplane
- Two bi-directional trigger access ports route trigger signals through to the backplane parallel trigger bus and star triggers (STRIG) to each slot
- Provides backplane PCIe and Ethernet communication between modules

1 Thunderbolt™ is the brand name of an interface standard developed by Intel (in conjunction with Apple) that allows connection of external peripherals to a computer. Thunderbolt 3 specification provides Gen 3 PCI Express (PCIe), DisplayPort, and DC power in one USB-C compatible cable; only PCIe is supported on the M9506A. Charging devices such as laptop computers over Thunderbolt 3 is not supported on the M9506A.

Other than a power button/status light (on the ESM), all monitoring, control, and communication with the chassis requires a host PC. This can be an embedded PC specifically designed for use in an AXIe chassis (such as the Keysight M9537A) or remote (a rackmount, desktop, or laptop) PC.

The Gen 3 PCIe Cable Interface ports provides up to a 8GB/s (theoretical) for Gen 3 x8 and 16 GB/s (theoretical) for Gen 3 x16. The Thunderbolt 3 port provides a Gen 3 x4 link with up to 4 GB/s (theoretical) bandwidth.



Refer to the *Keysight M9506A 5-Slot AXIe Chassis Startup Guide* to get detailed information about the AXIe chassis.

Host Computer

A host computer is used to:

- host all the software components of the instrument modules needed to control, configure, and use the modules.
- communicate with the ESM of the M9505A AXIe Chassis to allow you to monitor and control the chassis.

A host computer can be:

- the M9537A AXIe Embedded Controller module.
- a laptop with a USB port or with PCIe port.
- a desktop PC with a USB port or x8 or wider PCIe slot for the cabled PCIe adapter card.

Keysight M9537A AXIe Embedded Controller Module

The M9537A AXIe Embedded Controller is a one slot module that you can install in the M9505A AXIe Chassis like any other instrument module. This module acts as a host computer when installed in the M9505A AXIe Chassis. It is always installed in slot 1 of the M9505A AXIe Chassis.

The following figure displays this module.

Keysight M9537A AXIe Embedded Controller Module

The M9537A AXIe Embedded Controller is a one slot module that you can install in the M9505A AXIe Chassis like any other instrument module. This module acts as a host computer when installed in the M9505A AXIe Chassis. It is always installed in slot 1 of the M9505A AXIe Chassis. It may be installed in any slot of the M9514A AXIe chassis except for Slot 7 which is reserved for the ASM. However, to eliminate interference with the local

bus used for E-Keying (if your AXIe modules use E-Keying), you should install the controller in one of the outside slots; e.g., 1 or 14 first, then 2 or 13, etc.

The following figure displays this module:

The ESM:

- runs the chassis embedded operating system which manages all internal tasks and communications.
- tracks inserted modules and manages power requirements.
- monitors chassis temperature and controls variable- speed chassis fans.
- monitors module sensors and reports component failures to a system log.
- acts as a Gigabit Ethernet switch; forwards frames along the backplane.
- connects an external host computer to the chassis.
- synchronizes timing across all modules through the Keysight Trigger Bus, using an internal or external clock source.

LAN connector on AXIe ESM is not used. Only use LAN connection on the host computer.

Either the PCIe (desktop only) or USB (desktop or laptop) port can be used in this ESM but not both simultaneously. When you use the PCIe port, the USB port is automatically disabled until the PCIe port is no longer in use.

M8020A Modules

The M8020A modules are recognized by the model number and name located on their front panel.

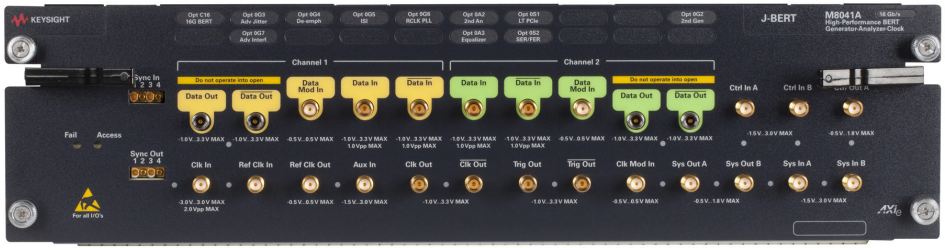
Each BERT module can be configured for 8 Gb/s or 16 Gb/s operation, as generator-only or as full BERT. Some upgraded features/components of a module are licensed and are only available when you purchase a license for that option. The M8062A module supports 32 Gb/s and the M8195A as a BERT module can support higher speeds than 16 Gb/s. The M8195A cannot be used as a full BERT. It has no analyzer.

The following sections describe each of the M8020A instrument modules in detail.

J-BERT M8041A Generator-Analyzer-Clock Module

The J-BERT M8041A is a BERT module that can be installed into an Keysight M9505A 5-slot AXIe chassis. This module occupies three slots.

The M8041A is a two channel bit error ratio tester with built-in clock and data generator for performing compliance and characterization measurements. The second channel requires a license.



M8041A Features

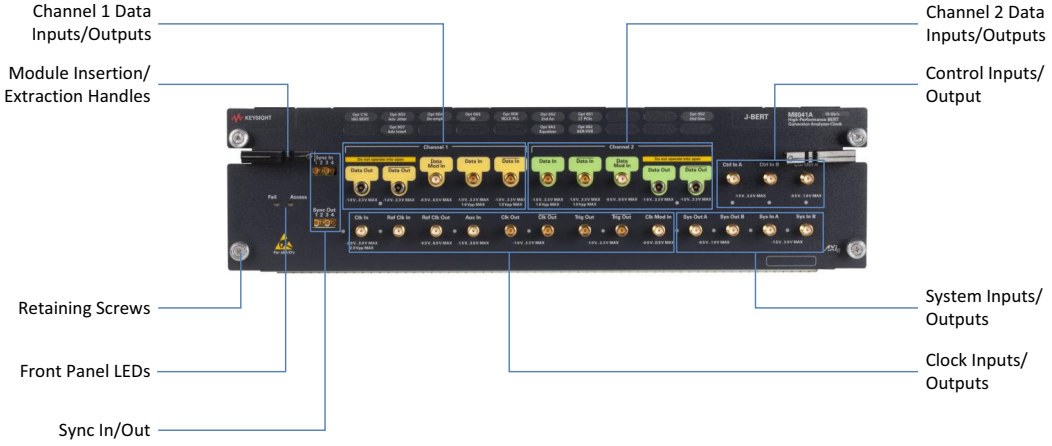
The M8041A module provides the following features:

- Two channel pattern generator (option 0G2) and two channel error detector (option 0A2)
- Data rate from 256 Mb/s to 16.2 Gb/s (option G16 or C16) for pattern generation and error detection
- Built in jitter injection (option 0G3)

- Adjustable ISI offered for M8041A and M8051A (option 0G5), software 2.0 and serial number >= DE55300500
- Built in 8 tap deemphasis (option 0G4)
- Built in receiver equalization (CTLE, option 0A3)
- Built in reference clock multiplier for pattern generator (option 0G6)
- Simultaneous common mode and differential mode level interference (option 0G7)
- Interactive link training (option 0S1, Software 1.5)
- Four universal control inputs with adjustable threshold
- Three universal control outputs with adjustable levels
- 2 Gb pattern memory per channel (requires software 1.5)

M8041A Module Components

The following figure displays the front panel of the M8041A module with its various components labeled.



The M8041A module has the following components.

Table 6 Insertion/Extraction and Retaining

Component	Description
Retaining screws	The screws on both ends of the module are used to retain the module tightly inside the M9505A AXIe Chassis slot once you have fully placed it inside the chassis. To remove the module, you first need to loosen these screws ensuring that these screws disengage completely.
Module Insertion/Extraction Handles	The handles on both sides of the module to insert or eject the module from the slot of the M9505A AXIe Chassis.

Table 7 Front Panel LEDs

Connector Name	Active when...	Color
Fail	power-up fault condition	red
Access	power-up ready state	green
Data In x	input is overloaded	red
Data Out x	output is overloaded	red
Data Mod In x	input is active	green
Ctrl In A/Ctrl In B	logic level is detected	green
Ctrl Out A	output is active	green
Clk In	signal is detected	green
Ref Clk In	signal is detected	green
Ref Clk Out	output is active	green
Aux In	not used	n/a
Clk Out	output is active	green
Trig Out	output is active	green
Clk Mod In	input is active	green
Sys Out A/Sys Out B	output is active	green
Sys Ctrl In A/Sys Ctrl In B	logic level is detected	green

M8041A Front Panel Connector Inputs/Outputs

CAUTION The inputs of the M8041A module are sensitive to static electricity. Therefore, take necessary anti-static precautions, such as wearing a grounded wrist strap, to minimize the possibility of electrostatic damage.

Table 8 Channel x Data Inputs/Outputs

Component	Description
Data Out and /Data Out	Differential data outputs (3.5 mm, female).
Data In and /Data In	Differential data inputs (3.5 mm, female).
Data Mod In	Accepts an external source for data out delay modulation (SMA, female).

Table 9 Clock Inputs/Outputs

Component	Description
Clk In	External clock input in the range of 8.1 to 16.2 GHz. This input is used as a direct clock for all channels in forwarded clock applications (SMA, female).
Ref Clk In	Reference clock input for applications that provide a host reference clock in the range of 10 MHz to 16 GHz. The clock signal may be SSC modulated and is used as the reference for the system clock of all Tx and Rx channels. A SSC tolerant PLL is used to multiply the reference clock to the system clock (SMA, female).
Ref Clk Out	The reference clock output is used to provide a 10 MHz or 100 MHz reference clock to the DUT or other test equipment (SMA, female).
Clk Out and /Clk Out	Differential clock output (3.5 mm, female).
Trig Out and /Trig Out	This output is used to send a trigger signal to another connected device, such as an oscilloscope (3.5 mm, female). It can also be used as a sub rate clock.
Clk Mod In	Input for delay modulation of the Trig Out and Clk Out channel. Both outputs are always affected (SMA, female).

Table 10 Sync In/Sync Out

Component	Description
Sync In	This input is used to synchronize two or more modules to a common system clock. It is connected to the Sync Out of the other module.
Sync Out	This output is used to synchronize two or more modules to a common system clock. It is connected to the Sync In of the other module.

Table 11 System Inputs/Outputs

Component	Description
Sys Out A/Sys Out B	System level control outputs used to signal events to the DUT or external instruments (SMA, female).
Sys In A/Sys In B	System level control inputs used to generate sequencer events (SMA, female).

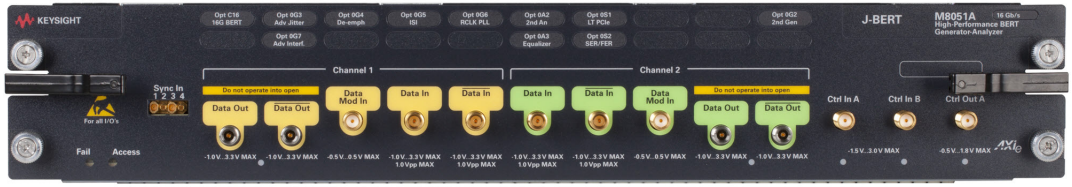
Table 12 Control Inputs/Output

Component	Description
Ctrl In A/Ctrl In B	The module has two control inputs at the font panel each. Functionality of each input can be selected as: sequence trigger, error add, and pattern capture event.
Ctrl Out A	The module has one control output at the front panel with the following functionality (SMA, female): **Error Output** This signal can be used to trigger an external instrument to help in error analysis. If an error occurs, a single RZ pulse is generated. Continuous errors will result in a clock signal.

J-BERT M8051A Generator-Analyzer

The J-BERT M8051A is an instrument module that can be installed into the M9505A 5-slot AXIe Chassis. This module occupies two slots and requires the M8041A module for proper operation.

The M8051A is a two channel Generator and two channel Analyzer for performing compliance and characterization measurements.

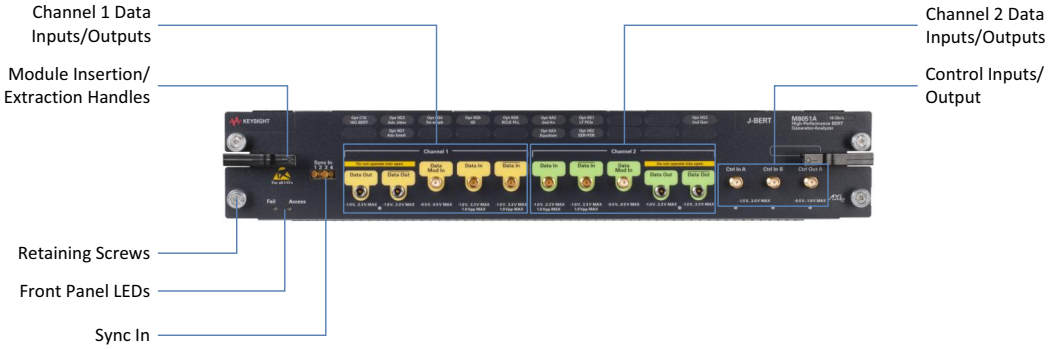


M8051A Features

The main M8051A features are the same as the M8041A features. For details, refer to J-BERT M8041A Generator-Analyzer-Clock Module on page 50.

M8051A Module Components

The following figure displays the front panel of the M8051A module with its various components labeled.



The M8051A module has the following components.

Table 13 Insertion/Extraction and Retaining

Component	Description
Retaining screws	The screws on both ends of the module are used to retain the module tightly inside the M9505A AXIe Chassis slot once you have fully placed it inside the chassis. To remove the module, you first need to loosen these screws ensuring that these screws disengage completely.
Module Insertion/Extraction Handles	The handles on both sides of the module to insert or eject the module from the slot of the M9505A AXIe Chassis.

Table 14 Front Panel LEDs

Connector Name	Active when...	Color
Fail	power-up fault condition	red
Access	power-up ready state	green
Data In x	input is overloaded	red
Data Out x	output is overloaded	red
Data Mod In x	input is active	green
Ctrl In A/Ctrl In B	logic level is detected	green

M8051A Front Panel Connector Inputs/Outputs

CAUTION The inputs of the M8051A module are sensitive to static electricity. Therefore, take necessary anti-static precautions, such as wearing a grounded wrist strap, to minimize the possibility of electrostatic damage.

Table 15 Channel x Data Inputs/Outputs

Component	Description
Data Out and /Data Out	Differential data outputs (3.5 mm, female).
Data In and /Data In	Differential data inputs (3.5 mm, female).
Data Mod In	Accepts an external source for data out delay modulation (SMA, female).

Table 16 Sync In

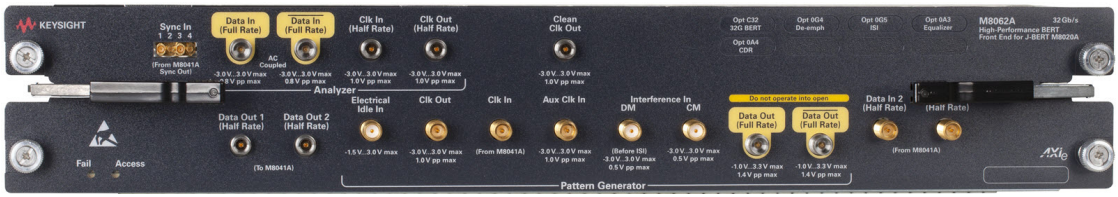
Component	Description
Sync In	This input is used to synchronize two or more modules to a common system clock. It is connected to the Sync Out of the other module or to the clock distribution module if more than two modules are installed. The sync cable is required if M8051A is connected with M8041A module.

Table 17 Control Inputs/Output

Component	Description
Ctrl In A/Ctrl In B	The module has two control inputs at the font panel each. Functionality of each input can be selected as: sequence trigger, error add, and pattern capture event.
Ctrl Out A	The module has one control output at the front panel with the following functionality (SMA, female): **Error Output** This signal can be used to trigger an external instrument to help in error analysis. If an error occurs, a single RZ pulse is generated with the width of half a vector length. Continuous errors will result in a clock signal.

M8062A 32Gb/s Front-end for J-BERT M8020A High-Performance BERT

The M8062A extends the data rate of the J-BERT M8020A Bit Error Ratio Tester to the speeds required for testing devices with lane rates in the 25-28 Gb/s range. When combined with a two channel M8041A, the system provides data pattern generation and full-rate error analysis for users and systems with lane rates up to 32.4 Gb/s.



M8062A Features

- Extends maximum data rate of J-BERT M8020A up to 32.4 Gb/s
- Seamless control of pattern generator and error analyzer
- Integrated 8-tap deemphasis
- Built in ISI generator for channel emulation
- Analyzer equalization eliminates errors resulting from closed eyes in loop back path
- Built in CDR for data rates up to 32 Gb/s

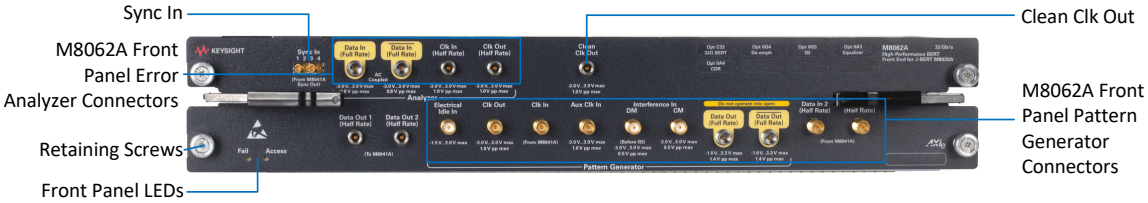
NOTE **The CDR license (M8062A-0A4) is required to enable the CDR feature. M8062A modules with serial numbers < MY55400300 may also require a hardware upgrade in order to enable this feature.**

Refer to the *Online Help* installed and integrated into the M8070B software to learn about how to use this module.

NOTE **Phase-matched cables must be used when connecting the M8041A data and clock outputs to the M8062A data and clock inputs. The provided cable set, Keysight M8062-61643, meets this requirement.**

M8062A Module Components

The following figure displays the front panel of the M8062A module with its various components labeled.



The M8062A module has the following components.

Table 18 Insertion/Extraction and Retaining

Component	Description
Retaining screws	The screws on both ends of the module are used to retain the module tightly inside the M9505A AXIe Chassis slot once you have fully placed it inside the chassis. To remove the module, you first need to loosen these screws ensuring that these screws disengage completely.
Module Insertion/Extraction Handles	The handles on both sides of the module to insert or eject the module from the slot of the M9505A AXIe Chassis.

Table 19 Front Panel LEDs

Connector Name	Active when...	Color
Fail	power-up fault condition	red
Access	power-up ready state	green

CAUTION The inputs and outputs of the M8062A module are sensitive to static electricity. Therefore, take necessary anti-static precautions, such as wearing a grounded wrist strap, to minimize the possibility of electrostatic damage.

Table 20 Sync In/Clean Clk Out

Connector Name	Description
Sync In	This input is used to synchronize two or more modules to a common system clock. It is connected to the Sync Out of the other module. The sync cable is required if M8062A is connected with M8041A module.
Clean Clk Out	Half-rate, or divided, clock output with no applied jitter.

M8062A Front Panel Pattern Generator Connectors

Table 21 Electrical Idle Input

Component	Description
Electrical Idle In	This input is used to enable/disable the output signal by an external control signal. If the input level is above the threshold level the module enters electrical idle. Normal operation resumes when the input level is below the threshold (SMA, female).

Table 22 Pattern Generator Clock Inputs/Output

Component	Description
Clk Out	Half-rate Pattern Generator clock output. Carries the same jitter as the full-rate data output.
Clk In	Pattern Generator clock input (half-rate). Connect to clock output of M8041A.
Aux Clk In	Alternate Pattern Generator clock input (half-rate). Typically unused.

Table 23 DMI/CMI Inputs

Component	Description
DMI In	Differential Mode Interference input. Applies a single-ended, external interference source differentially to the data output (SMA, female).
CMI In	Common Mode Interference input. Applies a single-ended, external interference source to both the normal and complement data output signals (SMA, female).

Table 24 Pattern Generator Data Inputs/Outputs

Component	Description
Data Out and /Data Out	Differential or single-ended, full-rate data output to the device under test. Unused outputs must be terminated into 50 Ω. (2.4 mm, female).
Data In 1 and Data In 2	Single-ended, half-rate data inputs from the M8041A module (3.5 mm, female).

M8062A Front Panel Analyzer Connectors

Table 25 Error Analyzer Data Inputs/Outputs

Component	Description
Data In and /Data In	Differential or single-ended, full-rate data input from the device under test. Unused input should be terminated into 50 Ω. (2.4 mm, female). These ports are AC coupled.
Data Out 1 and Data Out 2	Single-ended, half-rate data outputs to the M8041A module (3.5 mm, female).

Table 26 Error Analyzer Clock Inputs/Output

Component	Description
Clk Out	Half-rate Error Analyzer clock output, synchronous with analyzer sampling.
Clk In	Half-rate, Error Analyzer clock input. Allows external clocking of the Error Analyzer.

M8020A Module Setup

M8020A being a modular product includes different sets of modules which are hosted in an AXI chassis. It comprises of exactly one M8041A generator-analyzer-clock module and optionally one additional M8051A generator-analyzer module. The M8041A generator-analyzer-clock module is a true superset of the M8051A generator-analyzer module.

Setting up a Single Channel System

The single channel system is the smallest configuration consisting of one M8041A generator-analyzer-clock module within a 5-slot frame. You can upgrade it to a 2 channel system by adding the two channel options (second channel generator and second channel analyzer).

Setting up a Multi-Channel System

The multi-channel system is comprised of exactly one clock / data module and one or more data channels mounted in an AXIe frame.

The multi-channel system can be:

2-Channel System

A two-channel system consists of one clock/data module.

The following figure illustrates a two-channel system.

4-Channel System

A four-channel system consists of one clock module and one data modules.

The following figure illustrates a four-channel system.

For more details on how to establish connections between the M8020A modules, refer to the *M8020A Installation Guide*.

M8040A Overview

The M8040A is a modular instrument which supports the following modules:

- M8045A High-Performance BERT Pattern Generator-Clock
- M8046A High-Performance BERT Analyzer
- M8057A/B Pattern Generator Remote Head

M8040A being a modular product includes different sets of modules which are hosted in an AXI chassis. Each module and its features have their own license. You need to install these options in your instrument in order to use the modules or features. For details, refer to the chapter Licenses on page 823. However, if you have ordered M8040A-BU1, no license is required.

For details on the features and hardware components of each of the above mentioned modules, refer to *M8040A Getting Started Guide*.

NOTE

In case an AWG module (M8194A/M8195A/M8196A) and/or an IFS module (M8053A/M8054A) is used in a combined system with M8040A modules, ensure that the AWG and IFS modules are mounted in a slot number higher than clock generating M8040A module (M8045A) in the AXIe chassis. In other words, the AWG and IFS module always has to be mounted above the M8045A module in the chassis.

Also note that the M8050A clock generation modules (M8009A + M8042A) are not supported with M8100 series AWG modules (M8008A + M8198A/M8199A/M8199B) in the same setup, as only one set of clock modules can be used in a chassis. However, the interference source module (M8053A/M8054A) can be used together with the M8050A clock generation modules. In this configuration, the interference source module must be mounted above the M8050A clock generation module in the chassis.

M8040A Modules

M8045A High-Performance BERT Pattern Generator-Clock Module

The M8045A module can be a one or two data channel system (a second channel can be added with license). A one channel instrument has to be returned to the factory for installing the second channel (hardware) and license. It occupies three slots of the 5-slot M9505A AXIe chassis.

M8045A Features

- Up to two Pattern Generator channels per 3-slot-module
- Symbol rate 2 to 64 GBd
- NRZ and PAM4 format is software-selectable
- PAM4 up to 64 GBd
- Built in deemphasis
- Built in and calibrated jitter generation
- External jitter modulation per channel
- Remote head to get close to the DUT
- Pattern memory, PRBS, pattern sequencing
- Sequencing control by external control signals

Refer to the *Online Help* installed and integrated into the M8070B software to learn about how to use this module.

M8045A Module Components

The following figure displays the front panel of the M8045A module (2 data channel system):

The M8045A module has the following components.

Table 27 Insertion/Extraction and Retaining

Component	Description
Retaining screws	The screws on both ends of the module are used to retain the module tightly inside the M9505A AXIe Chassis slot once you have fully placed it inside the chassis. To remove the module, you first need to loosen these screws ensuring that these screws disengage completely.
Module Insertion/Extraction Handles	The handles on both sides of the module to insert or eject the module from the slot of the M9505A AXIe Chassis.

Table 28 Front Panel LEDs

Connector Name	Active when...	Color
Fail	power-up fault condition	red
Access	power-up ready state	green
Data Mod In 1/2	signal is detected	green
Clk Out 1/2	output is active	green
Ctrl Out 1/2	output is active	green
Ctrl In 1/2	logic level is detected	green
P & N 1/2	output is active	green
Clk In	signal is detected	green
Ref Clk In	signal is detected	green
Ref Clk Out	Outputs a 10 and 100 MHz clock, 1 Vpp single ended into 50 Ohm	green
Aux In	not used	n/a
Clk Out	output is active	green
Trig Out	output is active	green
Clk Mod In	input is active	green
Sys Out A/Sys Out B	output is active	green
Sys In A/Sys In B	logic state is detected	green

M8045A Front Panel Input/Output Ports

CAUTION The inputs/outputs of the M8045A module are sensitive to static electricity. Therefore, take necessary anti-static precautions, such as wearing a grounded wrist strap, to minimize the possibility of electrostatic damage.

Table 29 M8045A Front Panel Input/Output Ports

Connector Name	Description
Clk Out 1, 2	▪ Low Jitter (~150fs) Clk out. Baud-rate / 1,2,4,8,16 ▪ Same Jitter as Data out or clean clk ▪ Typ 1.5 V pp ▪ Used for Analyzer as external clock
P and N	P and N must be connected to M8057A/B remote head.
Remote Head 1, 2	Remote Head Control. This output provides power and control signals for the remote head amplifier
Data Mod In 1, 2	This input is used for data out delay modulation by an external source.
Ctrl In A, B	The data module has 2 control inputs at the front panel. Functionality of each input can be selected as: sequence trigger, error addition.
Ctrl Out A, B	The data module has 2 control output at the front panel. ▪ Ctrl Out A is the control output of channel 1. ▪ Ctrl Out B is the control output of channel 2. ▪ A pattern sequence that is using CTRL OUT A or CTRL OUT B will always drive all the control outputs of the channels that execute the pattern sequence. For independent control of Ctrl Out A and B, use independent sequences for channel 1 and 2.
Sync Out A, B	This output is used to synchronize two or more modules to a common system clock. It is connected to the SYNC IN of the other module.
Clk In	Clock not used for M8045A.
Ref Clk In	Reference clock input for applications that provide a host reference clock in the range of 10 MHz ... 16 GHz. It may be SSC modulated and is used as the reference for the system clock of all TX and RX channels. A SSC tolerant PLL is used to multiply the reference clock to the system clock.
Ref Clk Out	The reference clock output is used to provide a 10 MHz or 100 MHz reference clock to the DUT or other test equipment.

Connector Name	Description
Aux In	Port not in use.
Clk Out	Differential clock output.
Trig Out	This output is used to send a trigger signal to another connected device, such as an oscilloscope.
Clk Mod In	Input for delay modulation of TRIG OUT and CLK OUT channel, always affects both outputs.
Sys In A, Sys In B	These are control inputs at system level and can be used to generate events for the sequencer. The granularity is the vector size.
Sys Out A, Sys Out B	These are control outputs at system level and can be used to signal events to the DUT or external instruments. The granularity is the vector size.

M8046A High-Performance BERT Analyzer Module

The M8046A is an instrument module that can be installed into the M9505A 5- slot AXIe chassis. This module occupies one slot.

The M8046A supports symbol rates up to 32.4 GBd, the default is NRZ format.

The analyzer module can be used for error analysis in conjunction with the M8045A pattern generator, the M8194A/M8195A/M8196A Arbitrary Waveform generators or as stand-alone.

With M8070B, the M8046A can also be used in conjunction with M8041A + M8062A.

NOTE

The three or four channel configuration requires a cable (provided with the M8046A) that connects the M8045A Sync Out to the M8046A Sync In to synchronize the two modules to a common system clock. The M8046A Analyzer module can also be used with an external clock coming from CR (e.g. N1076A) or Generator output (M8045A channel 1/2 Clock Output or M8194A/M8195A/M8196A Data Output).

M8046A Features

- Symbol rates 2.50 GBd to 58 GBd
- One channel per 1-slot module
- Supports NRZ and PAM4
- 70 mV input sensitivity for NRZ and 40mV + 12% of input range per eye for PAM4
- Built-in equalization
- Real-time bit error and symbol error analysis
- PCIe link training for Gen3, Gen4, Gen5 and Gen6
- Built-in Clock Recovery
- SKP OS filtering for PCIe, USB 3.x and SATA/SAS
- Supports USB4v2 inverse pre-coder

M8046A Module Components

The following figure displays the front panel of the M8046A module with its various components:

The M8046A module has the following components.

Table 30 Insertion/Extraction and Retaining

Component	Description
Retaining screws	The screws on both ends of the module are used to retain the module tightly inside the M9505A AXIe Chassis slot once you have fully placed it inside the chassis. To remove the module, you first need to loosen these screws ensuring that these screws disengage completely.
Module Insertion/Extraction Handles	The handles on both sides of the module to insert or eject the module from the slot of the M9505A AXIe Chassis.

Table 31 Front Panel LEDs

Connector Name	Active when...	Color
Fail	power-up fault condition	red
Access	power-up ready state	green
Clk In	on when output active and CLK detected	green
Ctrl Out	on when output active	green
Ctrl In	logic state is detected	green
Data In	data received	green

M8046A Front Panel Inputs/Outputs Ports

CAUTION The inputs of the M8046A module are sensitive to static electricity. Therefore, take necessary anti-static precautions, such as wearing a grounded wrist strap, to minimize the possibility of electrostatic damage.

Table 32 M8046A Front Panel Inputs/Outputs Ports

Connector Name	Description
Data In and /Data In	Differential data inputs (3.5 mm, female)
Clk In	Clock input to sample the incoming data. Full/half and quarter-rate clock. Single ended.
Sync In	This input is used to synchronize two or more modules to a common system clock. It is connected to the Sync Out of the other module or to the clock distribution module if more than two modules are installed. The sync cable is required if M8046A is connected with M8045A Pattern Generator module. Not needed if external clock is used.
Ctrl Out A	Outputs a pulse in case of an error. Generates a pulse or static high/low if used from sequencer. **NOTE**: On the M8046A module, if error event condition occurs at the Analyzer, only then a single RZ pulse is generated. Continuous errors will result in a clock signal.
Ctrl In A	This input can be used as sequence trigger or pattern capture event.

M8057A/B Pattern Generator Remote Head

The M8057A/B remote head is an external box which must be connected to each channel of M8045A module. The three cables are fixed on the back side of M8057A/B which need to be connected to M8045A remote head, P and N connectors. It helps in minimizing signal degradations caused by lossy channels.

NOTE

Please note that it is mandatory to connect the M8057A/B remote head with each channel of the M8045A module. Operation without an M8057A/B remote head is unsupported and will not result in the configured output settings, potentially leading to damage of a connected device under test.

M8057A/B Remote Head Components

The following figure displays the front panel of the M8057A remote head with its various components. The similar front panel components are also available on the M8057B remote head.

Connect the cable (Part No. M8045A-801) to the front panel of the remote head. Specifications of the M8040A data sheet are valid at the output of the matched cable pair M8045A-801 that is attached to the M8057A/B remote head.

The M8057A/B remote head has the following components.

Table 33 Front Panel LEDs

Connector Name	Active when...	Color
Ready	remote head is operation	green

Table 34 M8057A/B Front Panel Inputs/Outputs Ports

Connector Name	Description
Data Out and /Data Out	Connected to DUT

The following figure displays the back panel of the M8057A/B remote head with its various components:

The back panel of M8057A/B remote head has cables which connect with each channel of M8045A remote head controls (P and N). The length of these cables are 85 cm.

Ensure that the chassis is NOT powered up or connected to a power source while making connections to M8057A/B.

Also, make sure NOT to remove the M8057A/B connections when it is powered on. However, if you wish to remove the M8057A/B connections, ensure that the instrument is powered off.

M8040A Module Setup

The M8040A 64GBd BERT is based on individual modules that are controlled by the M8070B software. The modules must be hosted in the 5-slot AXI chassis as described below:

- The M8045A module occupies three slots of the 5-slot M9505A AXIe chassis. It must be installed in slots 1 through 3 in the AXIe chassis unless the M9537A AXIe Embedded Controller is installed. The M9537A AXIe Embedded Controller must be installed in slot 1.
- The M8046A module occupies a single slot of the 5-slot M9505A AXIe chassis.
- The M8057A/B remote head is an external box which must be connected to each channel of M8045A module. Three cables are fixed on the back side of M8057A/B which need to be connected to M8045A remote head, P and N connectors.

The following figure shows a typical setup of M8045A, M8046A and M8057A/B.

M8050A Overview

The Keysight M8050A high-performance bit error ratio tester (BERT) enables accurate characterization of receivers used in next-generation data center networks and server interfaces. With uncompromised signal integrity, support for NRZ, PAM4, PAM6, and PAM8 signals, and data rates up to 120 GBd, the flexible architecture of the M8050A supports 1.6T pathfinding as well as other leading-edge technologies.

The M8050A high-performance BERT is one part of the Keysight M8000 Series of BER test solutions. It can be combined with other hardware and software of the M8000 Series.

The M8050A is a modular instrument which supports the following modules:

- M8042A Pattern Generator Module
- M8043A Error Analyzer Module
- M8009A Clock Module
- M8058A/M8059A/M8068A/M8069A Remote Head for M8042A Pattern Generator
- M8052A Remote Head for M8043A Error Analyzer

All the M8050A modules are controlled by the M8070B system software.

M8050A being a modular product includes different sets of modules which are hosted in an AXI chassis. Each module and its features have their own license. You need to install these options in your instrument in order to use the modules or features. For details, refer to the chapter Licenses on page 823. However, if you have ordered M8050A-BU2/BU3/BU4/BU5, no license is required.

For details on the features and hardware components of each of the above mentioned modules, refer to *M8050A Getting Started Guide*.

M8050A Modules

M8042A Pattern Generator

The M8042A pattern generator module operates from 2 to 120 GBd. It is available as one channel or two channel version. You can select three symbol rate ranges.The M8042A is an instrument module that can be installed into the M9505A 5- slot AXIe chassis. The one channel version occupies two slots while the two channel version occupies three slots in he M9505A 5- slot AXIe chassis. The M8042A requires the clock module with jitter modulation M8009A, and one remote head for each data output channel. For operation above 64 GBd the 120 GBd pattern generator remote head M8059A is required.

For the following generator functions a module option is required:

- Pattern generation up to 32 GBd for NRZ and PAM4 (M8042A-G32)
- Pattern generation up to 64 GBd for NRZ and PAM4 (M8042A-G642)
- Pattern generation up to 120 GBd for NRZ and PAM4 (M8042A-G12)
- De-emphasis, module-wide license (M8042A-0G4)

M8042A Module Components

The following figure displays the front panel of the M8042A module:

Figure 4 M8042A module front panel

As displayed in Figure 4 on page -76, the M8042A module has the following components.

Table 35 Front Panel LEDs

Front Panel LED	Active when...	Color
Fail	power-up fault condition	red
Access	power-up ready state	green

Table 36 Insertion/Extraction and Retaining

Component	Description
Retaining screws	The screws on both ends of the module are used to retain the module tightly inside the M9505A AXIe Chassis slot once you have fully placed it inside the chassis. To remove the module, you first need to loosen these screws ensuring that these screws disengage completely.
Module Insertion/Extraction Handles	The handles on both sides of the module to insert or eject the module from the slot of the M9505A AXIe Chassis.

M8042A Front Panel Connectors

CAUTION The inputs of the M8042A module are sensitive to static electricity. Therefore, take necessary anti-static precautions, such as wearing a grounded wrist strap, to minimize the possibility of electrostatic damage.

The M8042A pattern generator module provides many supplementary inputs and outputs. Shown here is the overview of all inputs and outputs for a two-channel version of M8042A.

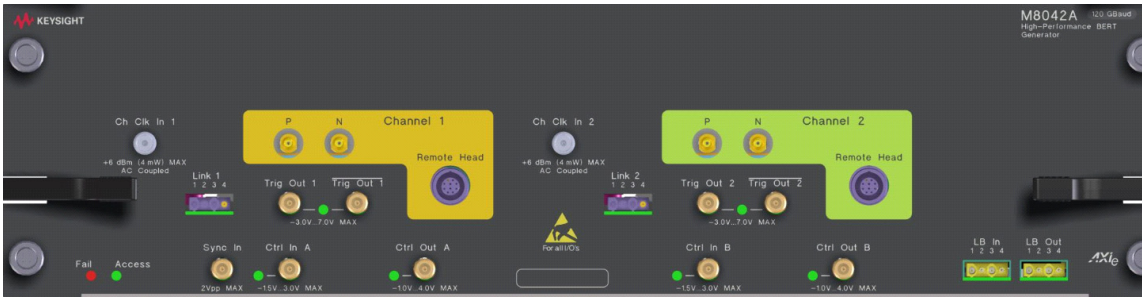


Figure 5 M8042A two channel version

Table 37 M8042A Front Panel Connectors

Connector	Description
P, N, Remote head channel 1/2	For connection to remote head
Ch Clk In 1/2	Clock from M8009A
Link 1/2	For link training and synchronization with other modules
Sync In	Sync from M8009A
Trig Out 1/2	Trigger output 3.5 mm (f)
Crtl In A/B	Trigger sequencer and error insertion 3.5 mm (f)
Crtl Out A/B	Generates a pulse or static high/low if used from sequencer 3.5 mm (f)
LB In/Out	Local bus connection to next chassis

M8009A Clock Generator

Keysight's M8009A clock generator is designed as sample clock source for the M8042A pattern generator. The M8009A clock module with integrated jitter modulation operates from 2 to 60 GHz. It can be locked to external reference clocks.

For the following functions a module option is required:

- Advanced jitter modulation for up to two channels, license (M8009A-0G3)
- Reference clock multiplier, license (M8009A-0G6)
- Clock Generator two channel 60 GHz, 1 slot AXIe (M8009A-062). This option is only available only for the new hardware i.e. M8009A-062.

The M8009A is an instrument module that can be installed into the M9505A 5-slot AXIe chassis. It comes as a 1-slot AXIe module, which allows the M8009A plus up to two M8042A pattern generator modules to be plugged into a single 5-slot AXIe chassis.

M8009A Module Components

The following figure provides an overview of all inputs and outputs of the M8009A clock module with jitter modulation:

The following figure shows the front panel of the M8009A clock module:

Figure 6 M8009A-061 module front panel

The following figure shows the front panel of the M8009A-062 clock module with the new "Clk Out 32G" port:

Figure 7 M8009A-062 module front panel

As displayed in Figure 7 on page -79, the M8009A module has the following components.

Table 38 Front Panel LEDs

Front Panel LED	Active when...	Color
Fail	power-up fault condition	red
Access	power-up ready state	green

Table 39 Insertion/Extraction and Retaining

Component	Description
Retaining screws	The screws on both ends of the module are used to retain the module tightly inside the M9505A AXIe Chassis slot once you have fully placed it inside the chassis. To remove the module, you first need to loosen these screws ensuring that these screws disengage completely.
Module Insertion/Extraction Handles	The handles on both sides of the module to insert or eject the module from the slot of the M9505A AXIe Chassis.

M8009A Front Panel Connectors

CAUTION The inputs of the M8009A module are sensitive to static electricity. Therefore, take necessary anti-static precautions, such as wearing a grounded wrist strap, to minimize the possibility of electrostatic damage.

Table 40 M8009A Front Panel Connectors

Connector	Description
Clk Out 32G	This signal is intended to be used to drive a DUT that requires a sub-rate clock. It can contain identical jitter as channel clock output 1. The clock signal is aligned to the data pattern. M8009A-062 is a license that is available for the new hardware of M8009A i.e. M8009A-062. This port is only available on M8009A modules with M8009A-062 option. However, Clk Out 32G is also accessible to user even without this license installed in the system. It provides the signal with the frequency range from 1 to 32.4 GHz.
Clk Out 16G	This signal provides a reference clock for a DUT. It can be operated with jitter and without jitter. It provides a differential clock with adjustable amplitude, offset and termination. No phase alignment to data output. It provides the signal with the frequency range from 31.25 MHz to 16.2499 GHz.
Ch Clk Out 1	This signal provides the clock signal for the pattern generator M8042A and AWG modules. Ch Clk Out 1 has to be connected to Ch Clk In 1 of the M8042A module.
Ch Clk Out 2	This output can be switched between two modes: ▪ Channel clock mode This signal provides the clock signal for the second channel of the pattern generator M8042A. Ch Clk Out 2 has to be connected to Ch Clk In 2 of the M8042A module. Independent jitter profile for Ch Clk Out 2 compared to Ch Clk Out 1 ▪ Forwarded clock mode This signal is intended to be used to drive a DUT that requires a data rate divide by a second clock. It can contain identical jitter as the Ch Clk 1 Output 1. This clock signal is synchronous to the data pattern, phase relation will change when divider settings are modified.
Sync In	This input is reserved for future use.
Sync Out A/B/C	This output is used to sync with M8042A module only.
Sys Trig In A/B	This signal is reserved for future use.

Connector	Description
Ref Clk In	This input allows locking the system clock to an external reference clock of 10 or 100 MHz instead of the internal oscillator.
Ref Clk Out	This signal provides a reference clock to lock with other instruments in the test setup. It provides clock frequency 10 MHz or 100 MHz.
Ref Clk Out 16G	This signal provides a clock between 8 and 16 GHz, relative to symbol rate. It can be used as clock input or as trigger input for a precision time base of a DCA. Clean clock only.

M8058A/M8059A/M8068A/M8069A Remote Head for M8042A Pattern Generator

The M8058A/M8059A/M8068A/M8069A remote head includes an external amplifier that is used in combination with the M8042A Pattern Generator. It helps in minimizing signal degradations caused by lossy channels. Four remote heads are available for the pattern generator module M8042A.

The M8068A and M8069A offer significantly higher output amplitude than the M8058A and M8059A.

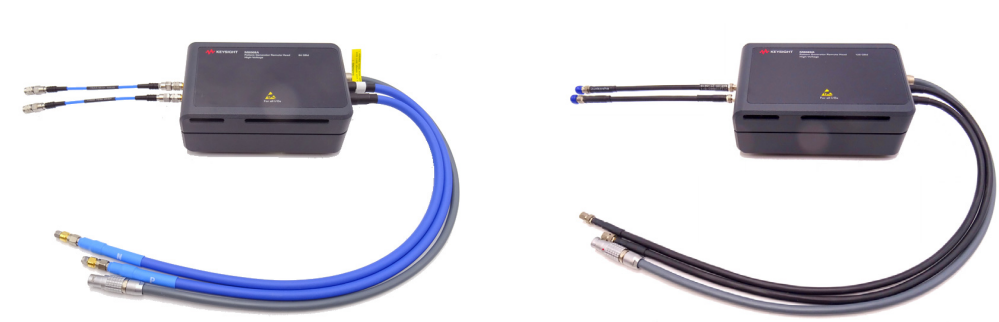
The following figure shows the M8058A and M8059A remote heads:

M8058A - Pattern Generator Remote Head up to 64.8 GBd

M8059A - Pattern Generator Remote Head up to 120 GBd

Figure 8 M8058A and M8059A remote heads

The following figure shows the M8068A and M8069A remote heads:



M8068A - Pattern Generator Remote Head up to 64.8 GBd

M8069A - Pattern Generator Remote Head up to 120 GBd

Figure 9 M8068A and M8069A remote heads

The 64 GBd M8058A/M8068A remote head is shown at the left side and this provides 1.85 mm connectors. It is used to accommodate close connection to the device under test for symbol rates up to 64.8 GBd.

The 120 GBd M8059A/M8069A remote head is shown on the right side and provides 1.0 mm connectors and is used to accommodate close connection to the device under test for symbol rates up to 120 GBd.

The three cables on the back side of the remote heads are used to connect with the M8042A pattern generator module and are not removable.

Please refer "*Tips for Preventing Damage*" document for mounting remote head cables.

M8058A/M8059A/M8068A/M8069A Remote Head Components

The following figure displays the front panel of the M8058A/M5059A/M8068A/M8069A remote head with its various components.

Figure 10 M8058A/M8059A/M8068A/M8069A remote head

As displayed in Figure 10 on page -84, the M8058A/M8059A/M8068A/M8069A remote head has the following components.

Table 41 Front Panel LED

Front Panel LED	Active when...	Color
Ready	Remote head is operational	Green
Data Out, $\overline{\text{Data Out}}$	On when data output is active	Green

Table 42 M8058A/M8059A/M8068A/M8069A Front Panel Connector

Connector	Description
Data Out, $\overline{\text{Data Out}}$	Connected to DUT

The back panel of M8058A/M8059A/M8068A/M8069A remote head has cables which connects with each channel of M8042A remote head ports. The length of the remote head including cables is ~830 mm.

Ensure that the chassis is NOT powered up or connected to a power source while making connections to M8058A/M8059A/M8068A/M8069A.

Also, make sure NOT to remove the M8058A/M8059A/M8068A/M8069A connections when it is powered on. However, if you wish to remove the M8058A/M8059A/M8068A/M8069A connections, ensure that the instrument is powered off.

M8043A Error Analyzer

The M8043A error analyzer module operates from 2.0 to 64.4 GBd. It requires the remote head M8052A. The M8043A is an instrument module that can be installed into the M9505A 5-slot AXIe chassis. This module occupies two slots in the M9505A 5-slot AXIe chassis and is always recommended to install on the slots above the M8042A and M8009A modules. The M8043A comes always with a built-in clock recovery. Integrated equalization with FIR, FFE and CTLE is optional. For error analysis above 64.4 GBd we recommend using the UXR0802A/04A with control from M8070B. See below for more details.

Using the remote input of the M8043A module without the M8052A remote head is prohibited.

The following analyzer options are provided:

- Error analysis up to 32.4 GBd for NRZ and PAM4 (M8043A-A32)
- Error analysis up to 64.4 GBd for NRZ and PAM4 (M8043A-A64)
- Equalization and de-embedding capability (M8043A-0A3)
- SKP OS Filtering for PCIe 128GT/s (M8043A-0S2)

M8043A Module Components

The following figure displays the front panel of the M8043A module:

Figure 11 M8043A module front panel

As displayed in Figure 4 on page -76, the M8043A module has the following components.

Table 43 Front Panel LEDs

Front Panel LED	Active when...	Color
Fail	power-up fault condition	red
Access	power-up ready state	green
Ctrl Out	ON when output active	green
Ctrl In	logic state is detected	green

Table 44 Insertion/Extraction and Retaining

Component	Description
Retaining screws	The screws on both ends of the module are used to retain the module tightly inside the M9505A AXIe Chassis slot once you have fully placed it inside the chassis. To remove the module, you first need to loosen these screws ensuring that these screws disengage completely.
Module Insertion/Extraction Handles	The handles on both sides of the module to insert or eject the module from the slot of the M9505A AXIe Chassis.

M8043A Front Panel Input/Output Ports

CAUTION The inputs of the M8043A module are sensitive to static electricity. Therefore, take necessary anti-static precautions, such as wearing a grounded wrist strap, to minimize the possibility of electrostatic damage.

The M8043A error analyzer module provides many supplementary inputs and outputs. Shown here is the overview of all inputs and outputs provided by M8043A.

Figure 12 M8043A front panel input/output ports

Table 45 M8043A Front Panel Input/Output Ports

Connector	Description
Remote Head	This port provides data input and control signals for M8052A remote head.
Cal	This calibration output is used for factory calibration at Keysight facilities.
Link	This communication link is for future use.
Clk In	This port enables source-synchronous operation, allowing effective analysis of data with Spread Spectrum Clocking (SSC). Clock Input operation requires M8043A serial number above MY64A01000.
Ctrl In	This port provides functionality that can be selected as: sequence trigger, pattern capture event.
Ctrl Out	This port outputs a pulse in case of an error. It generates a pulse or static high/low if used from sequencer.

M8052A Remote Head for M8043A Error Analyzer

The M8052A remote head is an external amplifier that must be used with the M8043A Error Analyzer. It helps in minimizing signal degradations caused by lossy channels.

The following figure shows the M8052A remote head:

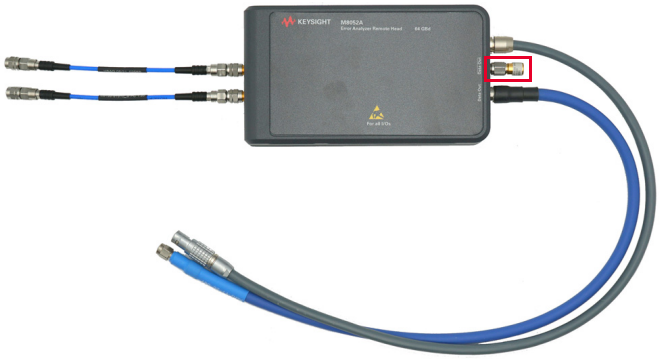


Figure 13 M8052A remote head

Two cables on the back side of the remote head are used to connect with the M8043A error analyzer and are not removable.

Please refer "*Tips for Preventing Damage*" document for mounting remote head cables.

Terminate the $\overline{\text{Data Out}}$ connector (highlighted in red) with 50 Ohm (as is shipping condition).

M8052A Remote Head Components

The following figure displays the front panel of the M8052A remote head with its various components.

Figure 14 M8052A remote head components

As displayed in Figure 14 on page -89, the M8052A remote head has the following components.

Table 46 Front Panel LED

Front Panel LED	Active when...	Color
Ready	Remote head is operational	green

Table 47 M8052 Front Panel Connector

Connector	Description
Data In and /Data In	Connected to DUT

The back panel of M8052A remote head has two cables which connects with the remote head ports of the M8043A. The length of the remote head including cables is about 835 mm.

Ensure that the chassis is NOT powered up or connected to a power source while making connections to M8052A.

Also, make sure NOT to remove the M8052A connections when it is powered on. However, if you wish to remove the M8052A connections, ensure that the instrument is powered off.

M8050A Module Setup

This section describe how to connect M8042A pattern generator and M8009A clock module in order to prepare a single-channel, two-channel and four-channel systems.

The following table shows the cables required for preparing a single-channel, two-channel and four-channel systems:

Clk Module Connections	Part No.	Option	Description
DAT Clk Cable	M8199-61624		Clock Cable, 2 Channel systems with 2x M8199-61624
DAT Clk Cable channel 1	M8042-61621	M8042A-801	Clock Cable Semi-rigid for Pattern Generator M8042A, Channel 1
DAT Clk Cable channel 2	M8042-61622	M8042A-802	Clock Cable Semi-rigid for Pattern Generator M8042A, Channel 2
Sync Cable 3.5 mm	M8042-61623	M8042A-803	Synchronization Cable, Semi-rigid for Pattern Generator M8042A and M8009A

Preparing Single-Channel System

For a single channel system, you would need a M8042A pattern generator (one channel) and M8009A clock module.

Follow the given steps to make the single-channel system:

1 Connect M8009A Channel Clock Out 1 port with the M8042A Channel Clock In 1 port using a semi-rigid cable.

2 Connect M8009A Sync Out A port with the M8042A Sync In port using a 3.5 mm sync cable.

Figure 15 Single-channel system

Preparing Two-Channel System

CASE – 1: Preparing two-channel system using one M8042A pattern generator (two channels) and one M8009A clock module.

Follow the given steps to prepare the two-channel system:

1 Connect M8009A Channel Clock Out 1 port with the M8042A Channel Clock In 1 port using M8199-61624 cable or a semi-rigid (M8042A-801) cable.

2 Connect M8009A Channel Clock Out 2 port with the M8042A Channel Clock In 2 port using M8199-61624 cable or a semi-rigid (M8042A-802) cable.

3 Connect M8009A Sync Out A port with the M8042A Sync In port using a 3.5 mm sync (M8042-61623) cable.

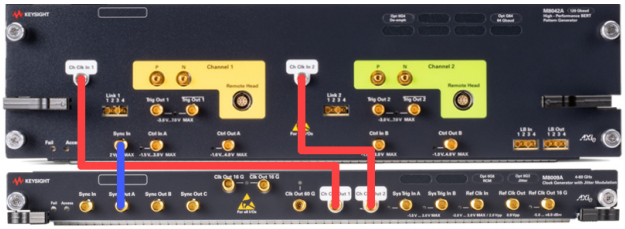


Figure 16 Two-channel system using one M8042A pattern generator (two channels) and one M8009A clock module

NOTE **Both channels must be properly clocked in order to arm the system. To ensure proper arming, connect both channels Clock In to the respective Clock Out on the clock module.**

CASE – 2: Preparing two-channel system using two M8042A pattern generators (one channel) and one M8009A clock module.

Follow the given steps to prepare the two-channel system:

1 Connect M8009A Channel Clock Out 1 port with the primary M8042A Channel Clock In 1 port using M8199-61624 cable or a semi-rigid (M8042A-801) cable.

2 Connect M8009A Channel Clock Out 2 port with the secondary M8042A Channel Clock In 1 port using M8199-61624 cable or a semi-rigid (M8042A-802) cable.

3 Connect M8009A Sync Out A port with the primary M8042A Sync In port using a 3.5 mm sync (M8042-61623) cable.

4 Connect M8009A Sync Out B port with the secondary M8042A Sync In port using a 3.5 mm sync (M8042-61623) cable.

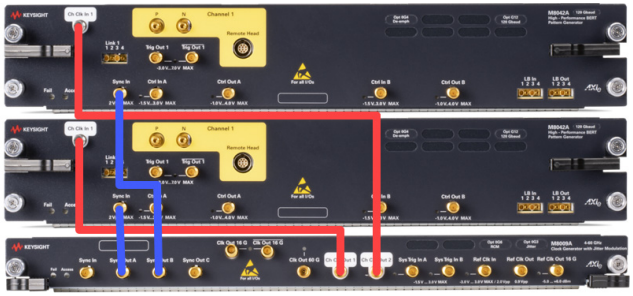


Figure 17 Two-channel system using two M8042A pattern generator (one channel) and one M8009A clock module

NOTE **When preparing a two-channel system, mixing one-channel and two-channel M8042A modules in a combined M8009A/M8042A instrument is not supported.**

Preparing Four-Channel System

For a four-channel system, you will require two M8042A two-channel pattern generators, two M8009A clock modules, two 5-slot chassis, and the necessary connecting cables. Install one M8009A and M8042A in each of the chassis. Make sure the M8009A is in a lower slot number than M8042A.

Select one of the two chassis as primary and the other as secondary. This is important as the following cabling instructions rely on this setup.

Follow the steps outlined below to set up the four-channel system:

1 Connect M8009A Sync Out A port with the M8042A Sync In port using a 3.5 mm sync cable.

2 Connect M8009A Channel Clock Out 1 port with the M8042A Channel Clock In 1 port using either an M8199-61624 cable or a semi-rigid (M8042A-801) cable.

3 Connect M8009A Channel Clock Out 2 port with the M8042A Channel Clock In 2 port using either an M8199-61624 cable or a semi-rigid (M8042A-802) cable.

4 Connect the M8009A Ref Clk Out 16 G port to the M8009A Ref Clk In port using either an M8199-61624 cable or a semi-rigid M8042A-802 cable. Additionally, connect the M8009A Sync Out B port to the M8009A Sync In port. Finally, connect the Clock Out port of the chassis defined as primary to the Clock In port of the System Module defined as secondary chassis.

5 Use a local bus (LB) cable (M8041-61601) to connect the M8042A LB Out port to the M8042A LB In port on the second chassis.

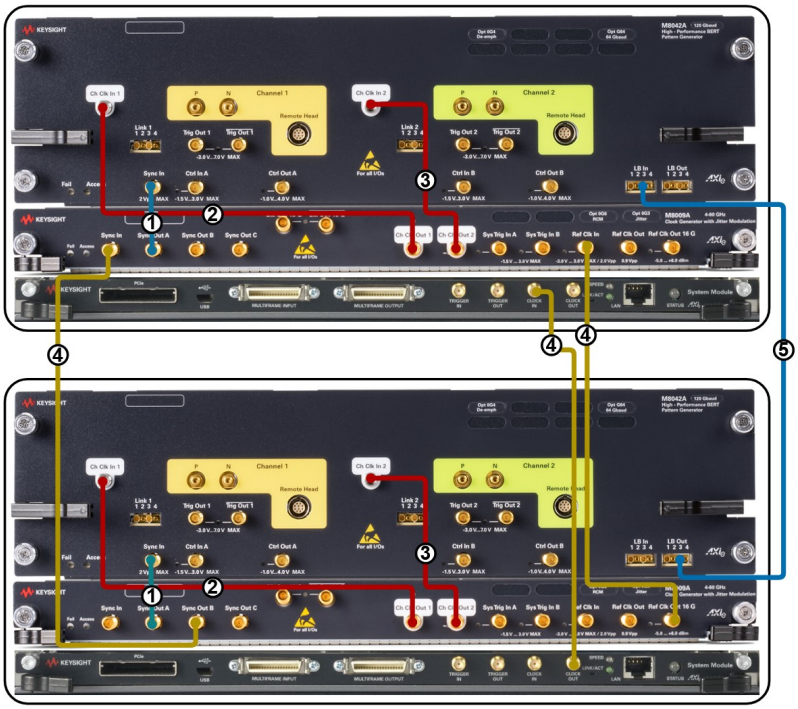


Figure 18 Four-channel system using two M8042A pattern generators (two channels) and two M8009A clock modules

M8070B Supported Plugins

The M8070B system software supports the following plugins:

- **Advanced Measurement Package** - The Advanced Measurement Package provides the following measurements:
  - Output Timing
  - Output Level
  - Jitter Tolerance
  - Eye Diagram
  - Parameter Sweep
  - BER Based Deemphasis

  For details on the measurements provided by **Advanced Measurement Package**, please refer to *M8000 Series Advanced Measurement Package User Guide*.
- **Error Distribution Analysis Package** - The Error Distribution Analysis Package provides the following measurement:
  - Error Distribution Analysis

  For details on the measurement provided by **Error Distribution Analysis Package**, please refer to *M8000 Series Error Distribution Analysis Package User Guide*.
- **M8070ISIB** - Adjustable ISI for M8000 Series of BER Test Solutions. For details on M8070ISIB, please refer to *M8070ISIB Adjustable ISI Package for M8000 Series User Guide*.
- **M8070OBLT Out-of-Band Link Training** - For details, please refer to *M8070OBLT Package User Guide*.

These plugin files (*.M8KP) which can be downloaded from Keysight web page.

NOTE

The M8070B supported plugins requires a valid license for activation. For details on the required license, refer to the *User Guide* or *Online Help* of the respective plugin.

The M8070B software comes with a Plugin Manager to simplify all the tasks related to plugin management. The Plugin Manager can help you to install the plugins. For further details on how to install, update or uninstall plugins, please refer to the Manage Plug-ins on page 805. Additionally, you can also refer to the *M8000 Series Plugins Getting Started Guide*.

M8100 Series Arbitrary Waveform Generators

The Keysight M8100 series arbitrary waveform generators (AWGs) offer a level of versatility that enables you to set up complex real-world signals – whether you need precise signals to characterize the performance of a design or need to stress a device to its limits. From low-observable radar to high-density communications, testing is more realistic with Keysight's precision arbitrary waveform generators.

The M8100 series modules are recognized by the model number and name located on their front panel. Each of the supported modules has some standard hardware and software features that are available with a standard license for that module. Some upgraded features/components of a module are licensed and are only available when you purchase and install a license for that option.

The M8100 series modules are controlled by the M8070B systems application software. In addition, a MATLAB based free utility named IQTools is included with the instrument software that provides a large number of waveform generation utilities as well as an option to download user-defined waveforms. The IQtools also supports "in-system calibration" to measure and compensate the frequency and phase response of the AWG and any external circuitry. It can compensate skew between all channels. When using the ILV-option in case of M8199A, IQtools additionally provides an automated skew calibration to optimize system performance.

Details of M8100 modules can be found at:
www.keysight.com/find/M8100

The following M8100 series modules are supported by the M8070B system software:

- M8199A 128/256 GSa/s Arbitrary Waveform Generator
  - M8158A AWG Remote Head for M8199A
  - M8008A Clock Generator
- M8199B 256 GSa/s Arbitrary Waveform Generator
  - M8008A Clock Generator
- M8198A Arbitrary Waveform Generator
  - M8157A AWG Remote Head for M8198A
- M8194A 120 GSa/s Arbitrary Waveform Generator
- M8195A 65 GSa/s Arbitrary Waveform Generator
- M8196A 92 GSa/s Arbitrary Waveform Generator

Ensure that you have the latest version of M8070B software installed on your system. Also, ensure that you have installed the M8199A/B and M8198A module driver in the M8070B software. The M8070B software and M8199A/B and M8198A module driver file can be downloaded from Keysight web page www.keysight.com.

For complete details on how to control M8199A/B and M8198A AWGs through the M8070B software system, refer to the *M8100 Series User Guide*.

For information on M8199A/B remote programming, refer to the *M8100 Series Programming Guide*.

NOTE

Note that the M8050A clock generation modules (M8009A + M8042A) are not supported with M8100 series AWG modules (M8008A + M8198A/M8199A/M8199B) in an M8070B hardware setup, as only one set of clock modules can be used in a chassis.

However, the interference source module (M8053A/M8054A) can be used together with the M8050A clock generation modules. In this configuration, the interference source module must be installed in slots with higher numbers than the M8050A clock generation modules. In other words, the interference source module must be mounted above the M8050A clock generation module in the chassis.

M8199A 128/256 GSa/s Arbitrary Waveform Generator

Keysight's M8199A 128/256 GSa/s Arbitrary Waveform Generator delivers twice the sampling rate, coupled with 50 percent more analog bandwidth and increased ENOB compared to legacy AWG products. This combination of industry-leading specifications enables research engineers to quickly and accurately develop advanced components for terabit transmission systems.

The M8199A is a powerful arbitrary waveform generator, which enables signal generation of up to 140 GBd with outstanding signal quality in a 2-slot AXIe module. Whether testing the discrete components of optical coherent systems or path-finding for terabit transmission in the next-generation data center, the M8199A is ideal for addressing the need for high sample rates and high analog bandwidth.

For complete details on M8199A Arbitrary Waveform Generator, visit www.keysight.com/find/M8199A.

M8199B 256 GSa/s Arbitrary Waveform Generator

Keysight's M8199B 256 GSa/s Arbitrary Waveform Generator (AWG) is a high-performance signal source for arbitrary signals, with the highest sample rate and the widest bandwidth in its class. The M8199B enables generation of high-quality signals of up to 160 GBd in a 2-slot AXIe module.

For applications beyond 128 GBd, the M8199B AWG is the ideal solution where it provides high-speed and precise testing of various optical systems, and it provides stress signals to test next generator digital signal processor ASICs and new algorithm concepts. The flexibility of the waveform generator with high speeds, combined with excellent intrinsic jitter performances makes the M8199B a truly unique and versatile instrument for Intensity-Modulation/Direct-Detect (IM/DD) optical applications.

The M8199B AWG also allows you to generate any arbitrary waveform that can be mathematically described and can be used for physics, chemistry, and general-purpose electronics research.

For complete details on M8199B Arbitrary Waveform Generator, visit www.keysight.com/find/M8199B.

M8008A Clock Generator

Keysight's M8008A clock generator is designed as sample clock source for the M8199A and M8199B Arbitrary Waveform Generators. It can also be used as a standalone low-jitter clock source for other applications. It has four outputs that provides an output frequency of 32 GHz to 64 GHz. It has two system trigger inputs that allow system control from external hardware. It also allows synchronous trigger distribution over local bus on the AXIe chassis backplane to adjacent PG/AWG modules.

The M8008A is an instrument module that can be installed into the M9505A 5-slot AXIe chassis. It comes as a 1-slot AXIe module, which allows the M8008A plus up to two M8199A / M8199B modules to be plugged into a single 5-slot AXIe chassis.

For complete details on M8008A Clock module, visit www.keysight.com/find/M8008A.

M8198A 256 GSa/s Arbitrary Waveform Generator

Keysight's M8198A 128 GSa/s Arbitrary Waveform Generator is the highest flexible arbitrary waveform generator that offers a unique combination of high sample rate, high-bandwidth, deep memory, and advanced functionalities. Whether performing breakthrough 6G research, testing the discrete components of an optical system, addressing deep memory or wide bandwidth application in aerospace/defense, or experimenting with high-speed transmission, you need precision and flexibility to deliver your next generation technology needs.

With sample rates of 128 GSa/s, the M8198A has enough oversampling gain to generate extremely broad bandwidth, yet high fidelity RF signals. The flexibility of the waveform generation with high speeds digital to analog converter and deep memory, combined with excellent intrinsic jitter performance makes the M8198A a truly unique and versatile instrument.

The M8198A enables advanced research allowing for customization of modulation formats and data patterns to boost transmission rates to the next level. In addition, the M8198A incorporates digital correction techniques for frequency and phase-response compensation of the AWG output and any external circuit such as cables, board traces, connectors etc. This allows the AWG to generate the desired signal at the device under test input. Any channels can be embedded/de-embedded if the S-parameters of the respective circuits are provided.

The M8198A AWG also allows you to generate any arbitrary waveform that can be mathematically described and can be used for physics, chemistry, and general-purpose electronics research.

For complete details on M8198A Arbitrary Waveform Generator, visit www.keysight.com/find/M8198A.

M8194A 120 GSa/s Arbitrary Waveform Generator

The Keysight Technologies, Inc. M8194A arbitrary waveform generator (AWG) has the highest sample rate and the widest bandwidth in its class with up to four synchronized channels operating simultaneously in one module.

- Sample rate up to 120 GSa/s (on all 4 channels simultaneously)
- Analog bandwidth: 45 GHz (typical), generate signals with frequency components up to 50 GHz
- 8 bits vertical resolution
- 512 kSa of waveform memory per channel

- 1, 2, or 4 differential channels per 1-slot AXIe module (number of channels is software upgradeable)
- Amplitude up to 0.8 Vpp(se) / 1.6 Vpp(diff.), voltage window -1.0 to +2.5 V
- Transition time (20%/80%): 11 ps without corrections / 6 ps with corrections applied (typical)
- Built-in frequency and phase response calibration for clean output signals
- Up to 4 modules (= 16 channels) can be synchronized

The M8194A AWG gives you the versatility to generate any mathematically defined arbitrary waveform, ultra-short yet precise pulses and extremely wideband chirps.

The basic functionality of the M8194A is controlled from a soft front panel application running on the AXIe embedded controller or external PC or laptop. However, the M8194A can also be integrated into the M8070B system software for M8000 Series of BER test solutions.

NOTE **For Real-Time Oscilloscopes as an error detector, M8194A AWG can be used with UXR1104A sampling oscilloscopes.**

NOTE **Launching the M8194A module may take a longer time than the other AWGs.**

Details of M8194A module can be found at www.keysight.com/find/M8194A.

M8195A 65 GSa/s Arbitrary Waveform Generator

The M8195A AWG gives you the versatility to create the signals you need for digital applications, optical and electrical communication and advanced research.

The Keysight M8195A is a 65 GSa/s Arbitrary Waveform Generator with highest bandwidth and channel density. Flexible signal generation at up to 32 GBd. Clean and distorted signal to stress the device to the limits. High speed AWG with up to 65 GSa/s sample rate and 20 GHz bandwidth

on up to four channels per module. The M8195A arbitrary waveform generator offers an output amplitude of up to 2 Vpp (diff.) and adjustable DC offset.

The M8195A module has four channels and up to five modules can be inserted in a 5-slot AXIe chassis to provide a maximum of 20 channels. This is valid for channels which are not synchronized across module boundaries. To synchronize these modules, a sync module is added in the frame. Since the sync module occupies a single slot, only four AWG modules can now be added thereby providing a maximum of 16 channels in a frame.

The basic functionality of the M8195A is controlled from a soft front panel application running on the AXIe embedded controller or external PC or laptop. However, the M8195A can also be integrated into the M8070B system software for M8000 Series of BER test solutions.

Details of M8195A module can be found at www.keysight.com/find/M8195A.

M8196A 92 GSa/s Arbitrary Waveform Generator

The Keysight M8196A is a 92 GSa/s Arbitrary Waveform Generator with highest bandwidth and channel density. It offers up to 4 x 512 kSa waveform memory. It is a high speed AWG with up to 96 GSa/s sample rate and 32 GHz bandwidth on up to 4 channels per module. The M8196A arbitrary waveform generator offers an output amplitude of up to 2 Vpp (diff.) and adjustable DC offset.

The M8196A provides high speed, precision, and flexibility which is ideally suited for digital applications, optical, aerospace/defense, and electrical communication.

The basic functionality of the M8196A is controlled from a soft front panel application running on the AXIe embedded controller or external PC or laptop. However, the M8196A can also be integrated into the M8070B system software for M8000 Series of BER test solutions.

Details of M8196A module can be found at www.keysight.com/find/M8196A.

M8053A Interference Source Module

The Keysight M8053A interference source module allows you to generate repeatable and accurate level impairments for testing of high-speed digital receivers that support symbol rates up to 120 GBd. The M8053A interference source module is controlled through the M8070B system software. The M8053A interference source module occupies 2 slots in an AXIe chassis and should be used in combination with the M8050A modules.

Key Features & Specifications

- Random level interference with crest factor > 5
- Sinusoidal level interference
- Common mode and differential mode
- Bandwidth adjustable up to 64 GHz
- 2 output channels with differential signals avoiding baluns
- Adjustable amplitude up to 1 Vpp (se), 2 Vpp (diff.)
- 2-slot AXIe module for combined configurations with M8050A high-performance BERT
- Matched coupler pair for interference injection before and after the ISI channel (NEXT, FEXT)
- Graphical user interface and remote control via M8070B system software for M8000 series of BER test solution

For more information on controlling the M8053A from M8070B, refer to Controlling M8053A from M8070B System Software on page 306.

Details of M8053A module can be found at:
www.keysight.com/find/M8053A

Installing M8053A Module in AXIe Chassis

The M8053A interference source can be configured with a M8050A high-performance BERT in a single 5-slot M9505A/M9506A AXIe chassis. The M8053A Interference Source module occupies two slots of the AXIe chassis. The M8053A module should be installed in the upper slot. The following figure illustrates an M8053A module with M8042A module (one channel) and M8009A clock module installed in a 5-slot AXIe chassis.

M8042A (1-channel), M8009A, M8053A in single chassis

It is also possible to configure the M8053A in a second AXIe chassis (M9502A/M9505A/M9506A). In case of installing an M8042A module (two channels) and an M8009A clock module in a 5-slot AXIe chassis, the M8053A module must be installed in separate 5-slot AXIe chassis.

M8042A (2-Channels), M8009A in chassis - 1

M8043A, M8053A in chassis - 2

The whole BERT system including the M8053A is controlled by the M8070B system software.

NOTE

It is recommended to connect two or multiple chassis via USB to two (multiple) USB ports of the controller. Thereafter, no further MultiFrame cable connections are required.

M8054A Interference Source Module

The Keysight M8054A interference source module allows you to generate repeatable and accurate level impairments for testing of high-speed digital receivers that support symbol rates up to 64 GBd. The M8054A interference source module is controlled through the M8070B system software.

Key Features & Specifications

- Random level interference with crest factor > 5
- Sinusoidal level interference
- Common mode and differential mode
- Bandwidth adjustable up to 32 GHz
- 4 differential output channels to avoid baluns
- Adjustable amplitude up to 1 Vpp (se), 2 Vpp (diff.)
- 1-slot AXIe module for combined configurations with M8040A high-performance BERT
- Graphical user interface and remote control via M8070B system software for M8000 series of BER test solution

For more information on controlling the M8054A from M8070B, refer to Controlling M8054A from M8070B System Software on page 320.

Details of M8054A module can be found at www.keysight.com/find/M8054A.

M8047B PCI Express Re-driver

The M8047B PCI Express Re-driver is a remote head for M8020A and M8040A error detectors, which enables testing of the system under tests with longer back channels. It reconditions signals through CTLE stages and linear amplification stages. The M8047B PCI Express Re-driver is controlled and powered via USB. It is controllable and remote programmable through M8070B system software (version 9.1 and above). For more information on controlling the M8047B PCI Express Re-driver from M8070B, refer to Controlling M8047B PCI Express Re-driver from M8070B User Interface on page 346.

Key Features

- Extends back channel each up to 17 dB
- Two-stage CTLE and linear output driver
- Controlled and powered through USB
- Graphical user interface and remote control via M8070B system software for M8000 series of BER test solution.

Details of M8047B PCI Express Re-driver module can be found at www.keysight.com/find/M8047B.

M8047C PCI Express Re-driver

The M8047C PCI Express Re-driver is a remote head for the M8046A error detector which enables testing of the system under tests with longer back channels. It reconditions signals through CTLE stages and linear amplification stages. The M8047C PCI Express Re-driver is controlled and powered via USB. It is controllable and remote programmable through M8070B system software (version 11.0 and above). For more information on controlling the M8047C PCI Express Re-driver from M8070B, refer to Controlling M8047C PCI Express Re-driver from M8070B User Interface on page 349.

Key Features

- Extends back channel each up to 37 dB
- Two-stage CTLE and linear output driver
- Controlled and powered through USB
- Graphical user interface and remote control via M8070B system software for M8000 series of BER test solution.

Details of M8047C PCI Express Re-driver module can be found at www.keysight.com/find/M8047C.

Other Supported Hardware(s)

Keysight N1076A/N1076B/N1077A DCA-M Clock Recovery

The N1076A/N1076B electrical clock recovery and N1077A electrical/optical clock recovery provide necessary clock signals to trigger an 86100D, N109x-series DCA-M oscilloscopes, or the error detector in a M8070B.

Figure 19 N1076A Electrical Clock Recovery

Figure 20 N1076B Electrical Clock Recovery

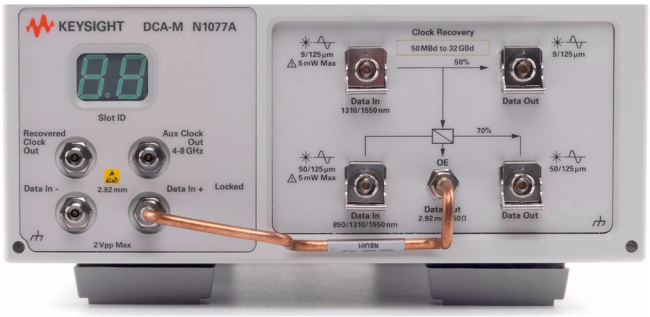


Figure 21 N1077A Optical/Electrical Clock Recovery

You can use an N1076A/N1076B/N1077A when:

- Access to appropriate clock signals from the Device Under Test (DUT) is not possible. The clock is recovered from the data stream.
- The existing clock has excessive intrinsic jitter that prevents accurate measurements. The N1076/7A can act as clean-up PLL for the clock.
- Input data is between 50 MBd and 16 GBd (32 GBd with option 232).
- Input range for N1076B is:
  - Option 264 - 125 MBd to 64 GBd
  - Option 232 - 125 MBd to 32 GBd
  - Option 216 - 125 MBd to 16 GBd

Detailed description of N1076A/N1076B/N1077A can be found at:

www.keysight.com/find/N1076A

www.keysight.com/find/N1076B

www.keysight.com/find/N1077A

Keysight Real Time Oscilloscopes

The M8070B system software supports certain real-time oscilloscopes to measure BER of NRZ signals and BER as well as SER of PAM4 signals. The real-time oscilloscope is completely controlled from M8070B to capture a signal and convert into a pattern stream that is then uploaded into the M8070B for comparison with an expected pattern and provide BER/SER measurements.

Nevertheless, it is possible to stop measuring BER on the integrated oscilloscope and therefore allow interactive tweaking of oscilloscope settings before continuing the BER measurements.

Currently, the following oscilloscopes models are supported:

- DSOZ634A Infiniium Z-Series Digital Storage Oscilloscope 63GHz / 160Gsa/s
- DSAZ634A Infiniium Z-Series Digital Signal Analyzer 63GHz / 160Gsa/s
- DSOZ594A Infiniium Z-Series Digital Storage Oscilloscope 59GHz / 160Gsa/s
- DSAZ594A Infiniium Z-Series Digital Signal Analyzer 59GHz / 160Gsa/s
- DSOZ504A Infiniium Z-Series Digital Storage Oscilloscope 50GHz / 160Gsa/s
- DSAZ504A Infiniium Z-Series Digital Signal Analyzer 50GHz / 160Gsa/s
- DSOX96204Q Infiniium Q-Series Digital Storage Oscilloscope 63GHz / 160Gsa/s
- DSAX96204Q Infiniium Q-Series Digital Signal Analyzer 63GHz / 160Gsa/s
- UXR0334A/B 33GHz / 128GSa/s
- URX0402A/B 40GHz / 256GSa/s
- UXR0404A/B 40GHz / 256GSa/s
- UXR0502A/B 50GHz / 256GSa/s
- UXR0504A/B 50GHz / 256GSa/s
- UXR0592A/B 59GHz / 256GSa/s
- UXR0594A/B 59GHz / 256GSa/s
- UXR0592A/BP 59GHz / 256GSa/s
- UXR0594A/BP 59GHz / 256GSa/s
- UXR0702A/B 70GHz / 256GSa/s
- UXR0704A/B 70GHz / 256GSa/s
- UXR0702A/BP 70GHz / 256GSa/s
- UXR0704A/BP 70GHz / 256GSa/s

- UXR0802A/B 80GHz / 256GSa/s
- UXR0804A/B 80GHz / 256GSa/s
- UXR0902B 90GHz / 256GSa/s
- UXR0904B 90GHz / 256GSa/s
- UXR1002A/B 100GHz / 256GSa/s
- UXR1004A/B 100GHz / 256GSa/s
- UXR1102A/B 110GHz / 256GSa/s
- UXR1104A/B 110GHz / 256GSa/s

Detailed description of the above oscilloscopes can be found at:
http://www.keysight.com/find/oscilloscopes

The following licenses are required on the oscilloscope:

- N5384A Serial Data Analysis (SDA)
- N8827A PAM4 Measurement (PM4)
- N5461A Equalization (DEQ)

NOTE

The minimum supported Infiniium version is 06.10.00616.

The minimum supported Infiniium UXR-Series version is 10.10.

For details on how to control a real-time scope from M8070B, refer to the *M8000 Series Advance Measurement Package User Guide*.

N7005A Optical-to-Electrical Converters

The M8070B software supports N7005A optical-to-electrical converter connected with real-time scope as an error detector.

This optical-to-electrical converter directly converts optical signals into electrical signals for convenient analysis on a compatible Infiniium real-time oscilloscope.

NOTE

In case of M8070B, this probe is supported for UXR series only.

The minimum supported Infiniium version for this feature is 10.20.XX.

N7005A Components

The details of N7005A Optical-to-Electrical Converter can be found at:

https://www.keysight.com/in/en/assets/9018-70016/user-manuals/9018-70016.pdf

For more information on using the N7005A Optical-to-Electrical Converter from M8070B, refer to the *M8000 Series Advance Measurement Package User Guide*.

DCA models supported for deemphasis optimization tool

The following instruments support the auto deemphasis feature to optimize the deemphasis settings. For more information on auto deemphasis feature, refer to M8040A Automatic Pattern Generator Deemphasis on page 388.

Figure 22 86108B Precision Waveform Analyzer

Figure 23 N1060A Precision Waveform Analyzer

Figure 24 N1094A DCA-M Sampling Oscilloscope (Two Electrical Channels)

Figure 25 N1094B DCA-M Sampling Oscilloscope (Four Electrical Channels)

Figure 26 N1092C DCA-M Sampling Oscilloscope (One Optical and Two Electrical Channels)

Figure 27 N1092E DCA-M Sampling Oscilloscope (Two Optical and Two Electrical Channels)

Figure 28 N1030A 65 GHz Single Channel Optical Module

Detailed description of 86108B/N1030A/N1060A/N1094A/N1094B/N1092C/N1092E can be found at:

www.keysight.com/find/86108B

www.keysight.com/find/N1030A

www.keysight.com/find/N1060A

www.keysight.com/find/N1094A

www.keysight.com/find/N1094B

www.keysight.com/find/N1092C

www.keysight.com/find/N1092E

Hardware Setup for M8046A and M8062A Modules

The M8046A module and the M8062A module can be used in the same setup. The following are the supported configurations:

1 Two M9505A 5-slot AXIe chassis controlled via USB

Chassis 1:

- Slot 1: M8041A
- Slot 4: M8062A

Chassis 2:

- Slot 1: M8046A

USB control ports of both chassis connected to the controlling PC

2 Two M9505A 5-slot AXIe chassis using an embedded controller

Chassis 1:

- Slot 1: M8041A
- Slot 4: M8062A

Chassis 2:

- Slot 1: Embedded Controller (M9536A or M9537A)
- Slot 2: M8046A

USB control port of chassis 1 is connected to a USB 2.0 port of the embedded controller

3 M9514A 14-slot chassis controlled from external computer

- Slot 1: M8041A
- Slot 4: M8062A
- Slot 6: M8046A
- Slot 7: M9521A AXIe System Module

4 M9514A 14-slot chassis controlled from embedded controller

- Slot 1: Embedded Controller (M9536A or M9537A)
- Slot 2: M8041A
- Slot 5: M8062A
- Slot 7: M9521A AXIe System ModuleSlot 8: M8046A

The M8046A may be used with a N1076A external clock recovery.

Limitations

The following are the limitations while using the M8046A and M8062A modules in the same setup:

- The M8046A does not support all sequencer word width settings of a M8041A/M8062A combination.
- Even though M8041A/M8062A and M8046A support a common sequencer word width of 1, they internally work with a different granularity and therefore cannot be used in the same sequence. Instead individual sequences need to be defined for M8062A Data Out, Data In and M8046A.
- In order to run the M8062A Data Out and M8046A Data In at the same symbol rate, the CLK IN frequency of M8046A needs to be specified manually. To do this, disable 'Follow SYS CLK' under Clock and specify CLK IN frequency and multiplier as required for the setup.

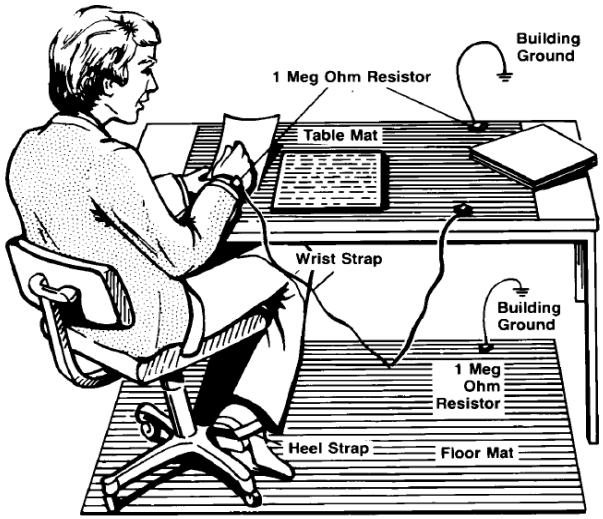
ESD Protection

CAUTION

Electrostatic discharge (ESD) can damage the circuits of the components on M8020A/M8040A/M8050A modules (M8041A, M8042A, M8051A, M8062A, M8043A, M8045A, M8046A, M8057A/B, M8058A, M8059A, M8068A, M8069A and M8052A). Avoid applying static discharges to the front-panel connectors. Before connecting any coaxial cable to the connectors, momentarily short the center and outer conductors of the cable together. Avoid touching the front-panel connectors without first touching the frame of the instrument. Be sure the instrument and all connected devices (DUT, etc.) are properly earth-grounded (to a common ground) to prevent buildup of static charge and electrical over-stress. Take necessary anti-static precautions, such as wearing a grounded wrist strap, to minimize the possibility of electrostatic damage.

Electrostatic discharge (ESD) can damage or destroy electronic components. All work on electronic assemblies should be performed at a static-safe work station. The following list and figure shows an example of a static-safe work station using two types of ESD protection. Purchase acceptable ESD accessories from your local supplier.

- Conductive table-mat and wrist-strap combination.
- Conductive floor-mat and heel-strap combination.



Both types, when used together, provide a significant level of ESD protection. Of the two, only the table-mat and wrist-strap combination provides adequate ESD protection when used alone. To ensure user safety, the static-safe accessories must provide at least 1 MW of isolation from ground.

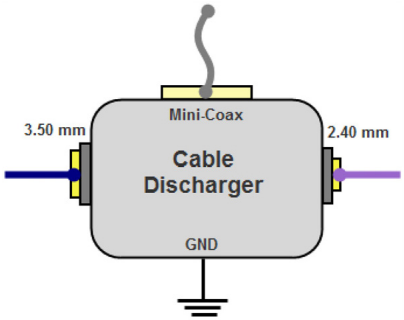
WARNING These techniques for a static-safe work station should not be used when working on circuitry with a voltage potential greater than 500 volts.

Discharging Cables

Loose cables are like a capacitor and can hold electrostatic charges. The free end of a cable touching surfaces that have voltage levels will cause product damage. Before connecting any cable to product connector, short the center and outer conductors of the cable together to ground momentarily.

You should use the cable discharger provided with the initial product shipment and shown in the following figures.

While discharging a cable, make sure to ground the box appropriately, via the “GND” connector of the box, to the ground connector of the AXIe chassis as shown in the figure.



That is either directly using the accessories provided with the discharger like the grounding cable, or via an ESD mat, which is connected to the ground connector of the AXIe chassis.

Discharge your cables using the matching connector e.g. 2.40 mm (also for 1.85 mm), 3.50 mm (also for 2.92 mm) and Mini-Coax. You may stick the cable discharger box to your instrument/AXIe chassis e.g. using the fastener tape provided.

Fixture made of plastic can store charges, and probing powered devices can subject inputs to damaging voltage and power levels. Poor AC power supply connected to product or DUT may create AC transients, insufficient grounding, floating neutral lines which cause damaging currents to flow into or out of the instrument.

For more information about electrostatic discharge, contact the Electrostatic Discharge Association www.esda.org.

M8000 Series of BER Test Solutions

User Guide

3 Quick Tour with M8070B User Interface

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KEYSIGHT TECHNOLOGIES

Overview

The M8070B system software for the M8000 Series of BER Test Solutions is required to control M8020A/M8040A/M8050A modules (M8041A, M8042A, M8051A, M8062A, M8043A, M8045A, M8046A and M8057A/B, M8058A, M8059A, M8068A, M8069A and M8052A) and other modules from M8100 AWG family (M8199A, M8199B, M8194A, M8195A and M8196A). It provides a user-friendly experience that can be used with standard or touchscreen enabled computers. It is fully supported by the Microsoft Windows 11 and Windows 10 IoT Enterprise operating systems. The M8070B software also supports an off-line version, that does not require any license to operate.

The M8070B user interface provides an interactive graphical display in multiple windows containing controls, that enable you to perform the tasks. The GUI components include menus, tool bars, dialog boxes, toggle buttons, standard windows buttons, drop-down lists, sliders, and many more which are further discussed in this manual.

NOTE

Depending upon the M8020A/M8040A/M8050A bundle with of chassis/controller pre-installation, you may have to install the M8070B software. Refer to *M8000 Series Installation Guide* and follow the given instructions to install the M8070B system software.

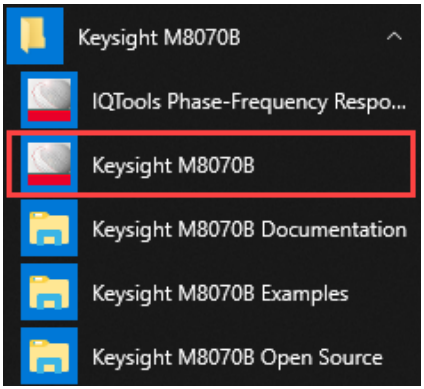
NOTE

Verify your account permissions. Ensure that you have full administrative privileges (run as Administrator) before you install or upgrade the M8070B system software on a PC running Windows 11 or Windows 10 IoT Enterprise. Not doing so may result in the installation failure. Please contact your system administrator to provide you the administrative rights.

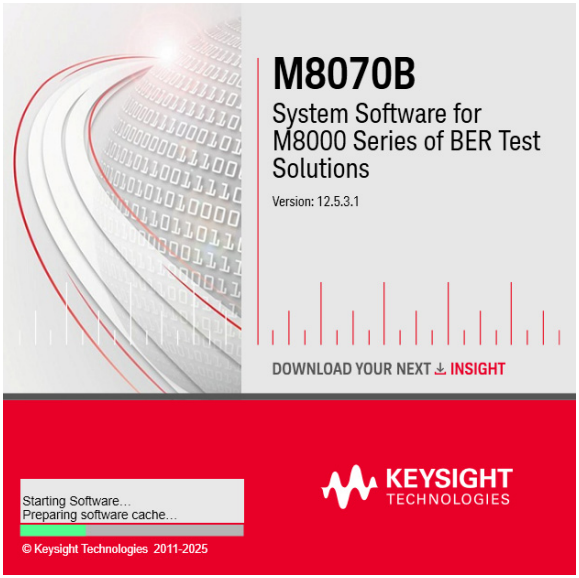
Launching M8070B User Interface

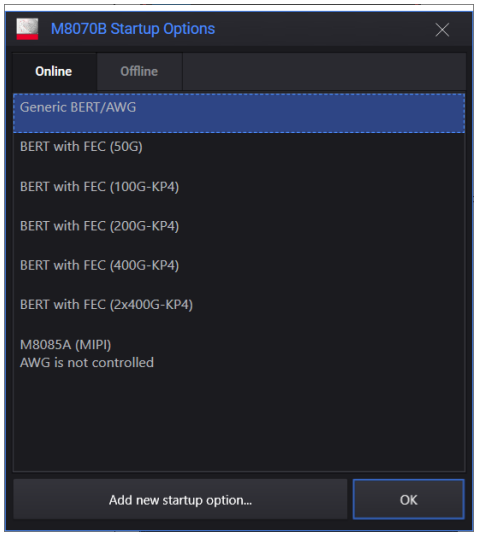
To launch the M8070B user interface, do the following:

1 Go to **Start** menu and then click **All Programs** > **Keysight M8070B** > **Keysight M8070B.**



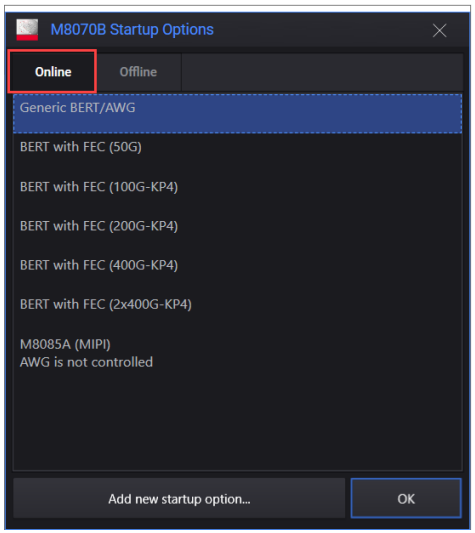
The M8070B splash screen will appear. Wait until the **M8070B Startup Options** dialog box opens.

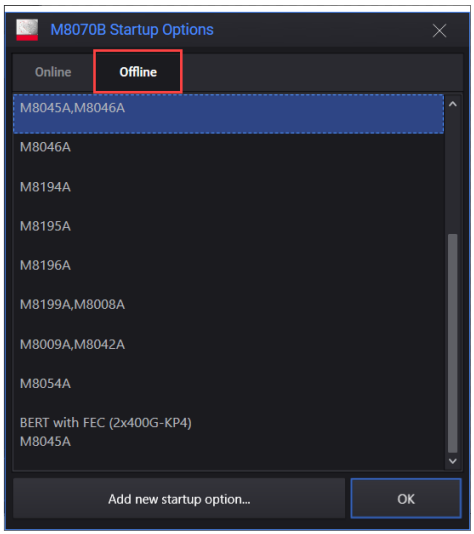




2 On the **M8070B Startup Options** dialog box, select one of the following tabs:

- **Online**: Select this tab, if you are using the M8070B in online mode.
- **Offline**: Select this tab, if you are using the M8070B in offline mode.





3 To launch the M8070B in online mode, select one of the following launch options:

- **Generic BERT/AWG**: The general purpose BERT operation with full support of all computer standard specific functionalities, like PCIe LTSSM, or SKP-OS removal.
- **BERT with FEC (50G)**: In this mode, the M8045A module works in 50G KP4 mode. All other modules operate exactly like in the Generic BERT mode.

  The factory patterns IEEE_802_3cd_RS_544_514_Remote_Fault and IEEE_802_3cd_RS_544_514_Scrambled_Idle uses an FEC as specified for 50G KP4 applications. A dedicated FEC error insertion logic allows inserting a customizable number of errors per FEC frame as well as inserting single Bit Interleaved Parity (BIP) errors.
- **BERT with FEC (100G KP4)**: In this mode, the M8045A module works in 100G KP4 mode. All other modules operate exactly like in the Generic BERT mode. The factory patterns IEEE_802_3cd_RS_544_514_Remote_Fault and IEEE_802_3cd_RS_544_514_Scrambled_Idle uses an FEC as specified for 100G KP4 applications. The Computer Standard specific functionalities, like dedicated PHY-Protocols or LTSSM support, is not available when the M8045A module works in 100G KP4 mode. The M8045A module is restricted to the symbol rates ranges from 16.208 GBd to 26.6 GBd and 32.416 GBd to 53.2 GBd. Symbol rate outside these two ranges are not available.
- **BERT with FEC (200G KP4)**: In this mode, the M8045A module works in 200G KP4 mode. All other modules operate exactly like in the Generic BERT mode. The factory patterns IEEE_802_3cd_RS_544_514_Remote_Fault and IEEE_802_3cd_RS_544_514_Scrambled_Idle uses an FEC as specified for 200G KP4 applications. The Computer Standard specific functionalities, like dedicated PHY-Protocols or LTSSM support, is not available when the M8045A module works in 200G KP4 mode. The M8045A module is restricted to the symbol rates ranges from 16.208 GBd to 26.6 GBd and 32.416 GBd to 53.2 GBd. Symbol rate outside these two ranges are not available.

- **BERT with FEC (400G KP4)**: In this mode, the M8045A module works in 400G KP4 mode. All other modules operate exactly like in the Generic BERT mode. The factory patterns IEEE_802_3cd_RS_544_514_Remote_Fault and IEEE_802_3cd_RS_544_514_Scrambled_Idle uses an FEC as specified for 400G KP4 applications. The Computer Standard specific functionalities, like dedicated PHY-Protocols or LTSSM support, is not available when the M8045A module works in 400G KP4 mode. The M8045A module is restricted to the symbol rates ranges from 16.208 GBd to 26.6 GBd and 32.416 GBd to 53.2 GBd. Symbol rate outside these two ranges are not available.
- **BERT with FEC (2x400G KP4)**: In this mode, the M8045A module works in 2x400G KP4 mode. All other modules operate exactly like in the Generic BERT mode. The factory patterns IEEE_802_3cd_RS_544_514_Remote_Fault and IEEE_802_3cd_RS_544_514_Scrambled_Idle uses an FEC as specified for 2x400G KP4 applications. The Computer Standard specific functionalities, like dedicated PHY-Protocols or LTSSM support, is not available when the M8045A module works in 2x400G KP4 mode. The M8045A module is restricted to the symbol rates ranges from 32.416 GBd to 53.2 GBd. Symbol rate outside these range is not available.
- **M8085A (MIPI) AWG is not controlled**: M8085A (MIPI) Test Solution.

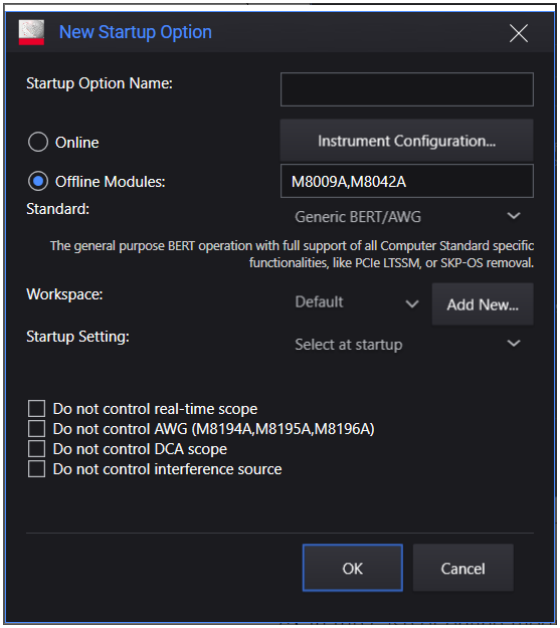
For more information, refer to FEC Encoding on page 419.

4 To launch the M8070B in offline mode, select one of the following launch options:
- **M8045A, M8046A, M8054A**: Launches the M8070B with M8045A, M8046A, and M8054A modules.
- **M8041A, M8051A**: Launches the M8070B with M8041A and M8051A modules.
- **M8041A, M8062A**: Launches the M8070B with M8041A and M8062A modules.
- **M8045A, M8046A**: Launches the M8070B with M8045A and M8046A modules.
- **M8008A, M8199A**: Launches the M8070B with M8008A and M8199A modules.
- **M8008A, M8199B**: Launches the M8070B with M8008A and M8199B modules.
- **M8009A, M8042A, M8043A**: Launches the M8070B with M8009A, M8042A and M8043A modules. Note that M8009A module must be in front of M8042A module in offline startup options.

- **M8046A**: Launches the M8070B with M8046A module.
- **M8094A**: Launches the M8070B with M8094A module.
- **M8095A**: Launches the M8070B with M8095A module.
- **M8096A**: Launches the M8070B with M8096A module.

5 To add a new startup option, click **Add new startup options...** button on the **M8070B Startup Options** dialog box. For each new startup option, this dialog automatically checks all previously saved configurations and selects the one that matches the most recent change, rather than creating a new entry in the configuration list.

The **New Startup Option** dialog box appears. Enter the required information.

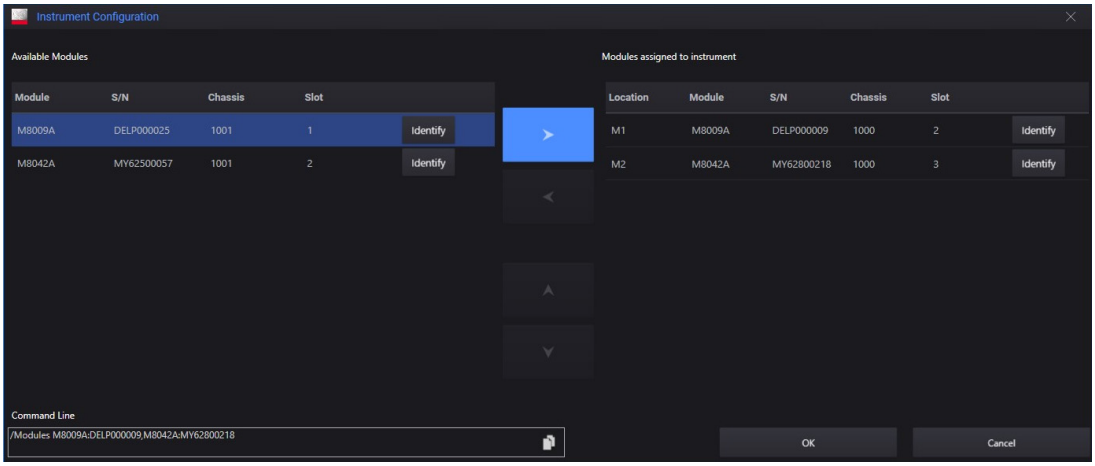


a Type the name of the startup option in the **Startup Option Name** text box.

b Select an option **Online** or **Offline Modules**.

c In the case of online modules and a 4-channel system with two M8009A and two M8042A modules in two AXIe frames, first make sure that the cable connections as described in the M8050A Getting Started Guide under Preparing Four-Channel System are correct.

Then click the **Instrument Configuration** button. The **Instrument Configuration** window displays all connected modules. See the following figure:



The list of **Available Modules** shows the M8009A and M8042A modules detected by the M8070B and currently not assigned to the instrument. The list of **Modules assigned to instrument** shows the M8009A and M8042A modules currently assigned to the instrument. For each module product number, serial number, chassis identifier and chassis slot number are shown. For the modules assigned to the instrument their location identifier is shown additionally. The M8009A, which is connected via its Sync Out B to the Sync In of the other M8009A is the primary M8009A and location identifier M1 must be assigned to it. Its Sync signal is transmitted to the secondary M8009A in the other chassis.

The **Identify** toggle button allows to flash the **Access** LED on the corresponding module front panel.

Use the left/right arrows to move modules from one list to the other. Moving modules from the left to the right list moves all modules from the corresponding chassis. Moving modules from the right to the left list moves the individually selected module. Use the up/down arrows (only possible on the right in the list under **Modules assigned to the instrument**) to move the chassis along with their associated modules one line up or down.

Other connected modules like M8043A Error Detector or M8053A Interference Source are not displayed in the Instrument Configuration window. They are appended at the end of the list and assigned the next free location identifier.

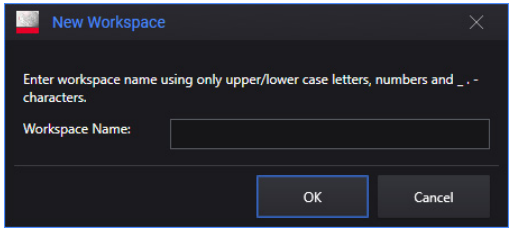
During manual configuration a command line is created and displayed on the left at the bottom of the dialog. This command line can be used to recreate this configuration. This allows to skip the **New Startup Option** dialog on subsequent restarts of the M8070B.

d In case of Offline Modules, type the module name(s) that you want to launch with M8070B. Please note that if you are opting for starting M8009A & M8042A modules, the M8009A module must be in front of M8042A module in offline startup options.

e Select an option from the **Standard** drop-down list. The following options are available:

- Generic BERT
- BERT with FEC (50G)
- BERT with FEC (100G KP4)
- BERT with FEC (200G KP4)
- BERT with FEC (400G KP4)
- BERT with FEC (2x400G KP4)
- M8085A (MIPI)

f Select a workspace from the **Workspace** drop-down list. Initially only the default workspace is available. You can create a new workspace by clicking **Add New...** button.



g Select an option from the **Startup** Setting drop-down list. The following options are available:

- **Select at startup**: Opens the **Recall Instrument State** dialog which allows you to load the M8070B user interface with the stored settings. For details, refer to Recall Instrument State on page 169.

- **Factory Preset**: Launches the M8070B user interface with factory default settings.
- **Last Used**: Launches the M8070B user interface with the last used settings.

h Select or unselect "**Do not control real-time scope"** checkbox for the respective setting. This will allow M8070B software to ignore real-time scope when launched.

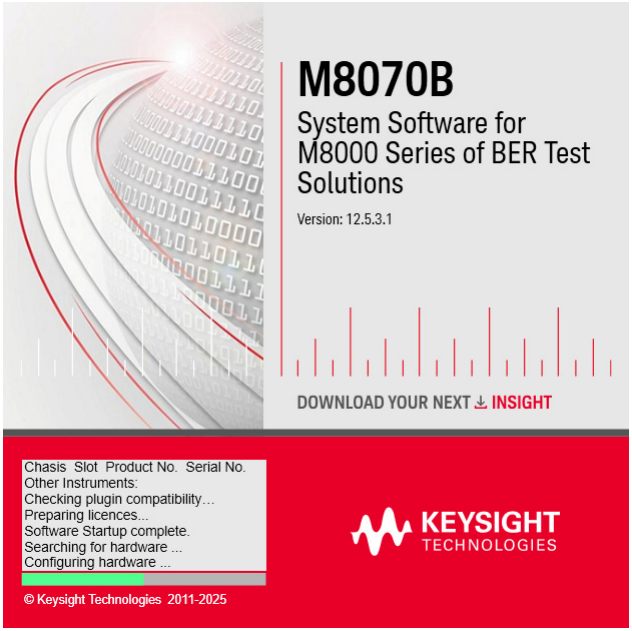
i Select or unselect "**Do not control AWG (M8194A,M8195A,M8196A)"** checkbox for the respective setting. This will allow M8070B software to ignore M8194A, M8195A and M8196A AWGs when launched.

j Select or unselect "**Do not control DCA scope"** checkbox for the respective setting. This will allow M8070B software to ignore DCA scope when launched.

k Select or unselect "**Do not control interference source"** checkbox for the respective setting. This will allow M8070B software to ignore interference source when launched.

6 Click **OK**.

The M8070B splash screen appears again:



Starting M8070B on the command line

- When no additional command line arguments are given, M8070B starts in Generic BERT/AWG mode.
- To launch M8070B in 50G KP4 mode, use the following command line argument: `/set:M8045A-50G-KP4`

  Example: Start M8070B in 50G-KP4 mode using the workspace named 50G-KP4 to separate settings from the Computer Standard specific settings:

  ```
  C:\Program Files\Keysight\M8070B\
  bin>Keysight.M8070B.exe /set:M8045A-50G-KP4
  /workspace 50G-KP4
  ```
- To launch M8070B in 100G KP4 mode, use the following command line argument: `/set:M8045A-100G-KP4`

  Example: Start M8070B in 100G-KP4 mode using the workspace named 100G-KP4 to separate settings from the Computer Standard specific settings:

  ```
  C:\Program Files\Keysight\M8070B\
  bin>Keysight.M8070B.exe /set:M8045A-100G-KP4
  /workspace 100G-KP4
  ```
- To launch M8070B in 200G KP4 mode, use the following command line argument: `/set:M8045A-200G-KP4`

  Example: Start M8070B in 200G-KP4 mode using the workspace named 200G-KP4 to separate settings from the Computer Standard specific settings:

  ```
  C:\Program Files\Keysight\M8070B\
  bin>Keysight.M8070B.exe /set:M8045A-200G-KP4
  /workspace 200G-KP4
  ```
- To launch M8070B in 400G KP4 mode, use the following command line argument: `/set:M8045A-400G-KP4`

  Example: Start M8070B in 400G-KP4 mode using the workspace named 400G-KP4 to separate settings from the Computer Standard specific settings:

  ```
  C:\Program Files\Keysight\M8070B\
  bin>Keysight.M8070B.exe /set:M8045A-400G-KP4
  /workspace 400G-KP4
  ```

- To launch M8070B in 2x400G KP4 mode, use the following command line argument: `/set:M8045A-2x400G-KP4`

  Example: Start M8070B in 2x400G-KP4 mode using the workspace named 2x400G-KP4 to separate settings from the Computer Standard specific settings:

  ```
  C:\Program Files\Keysight\M8070B\
  bin>Keysight.M8070B.exe /set:M8045A-2x400G-KP4
  /workspace 2x400G-KP4
  ```

- To launch M8070B using a user-defined configuration file, use the following command line argument: `/config`

  Example:

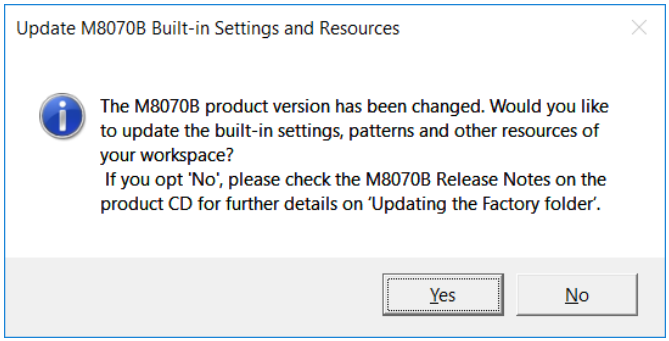
  Assuming you have a configuration file named "Offline_M8045A_M8046A.m8kc" stored in the folder `C:\ConfigurationFilesExamples`. This file is used to launch M8070B with the M8045A and M8046A modules in offline mode.

  In that case, the command will be:

  ```
  C:\Program Files\Keysight\M8070B\bin>
  Keysight.M8070B.exe /config "C:\
  ConfigurationFilesExamples\
  Offline_M8045A_M8046A.m8kc" -offline "M8045A,
  M8046A"
  ```

Messages while launching M8070B GUI

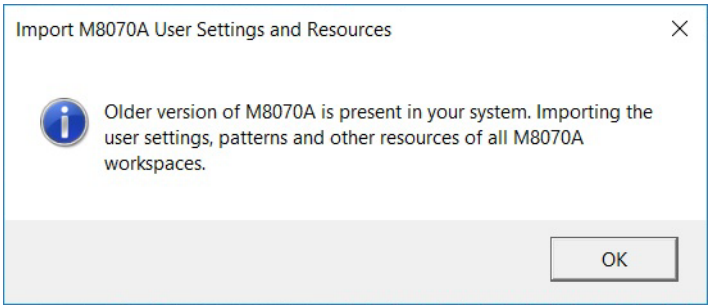
Whenever there is a change in the M8070B software version, the following message appears:



This message box prompts the user to update the workspace as there is an update in the software version.

- Clicking on “Yes” will update the workspace.
- Clicking on “No” will do nothing and you will have to manually update the workspace. For details on how to update the workspace, refer the “M8070B Release Notes”.

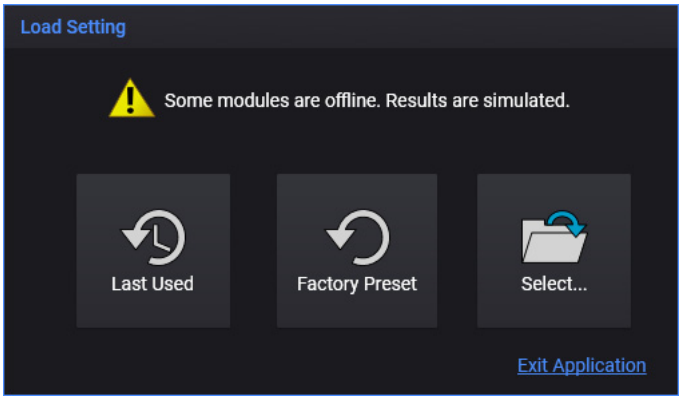
Whenever, an old workspace data (M8070A) is detected, the following message will appear:



- Clicking on “OK” will import the user settings, patterns and other resources of M8070A workspace to M8070B workspace.

Load Setting

Before the M8070B software is launched, a **Load Setting** dialog will appear which allows you to load settings.



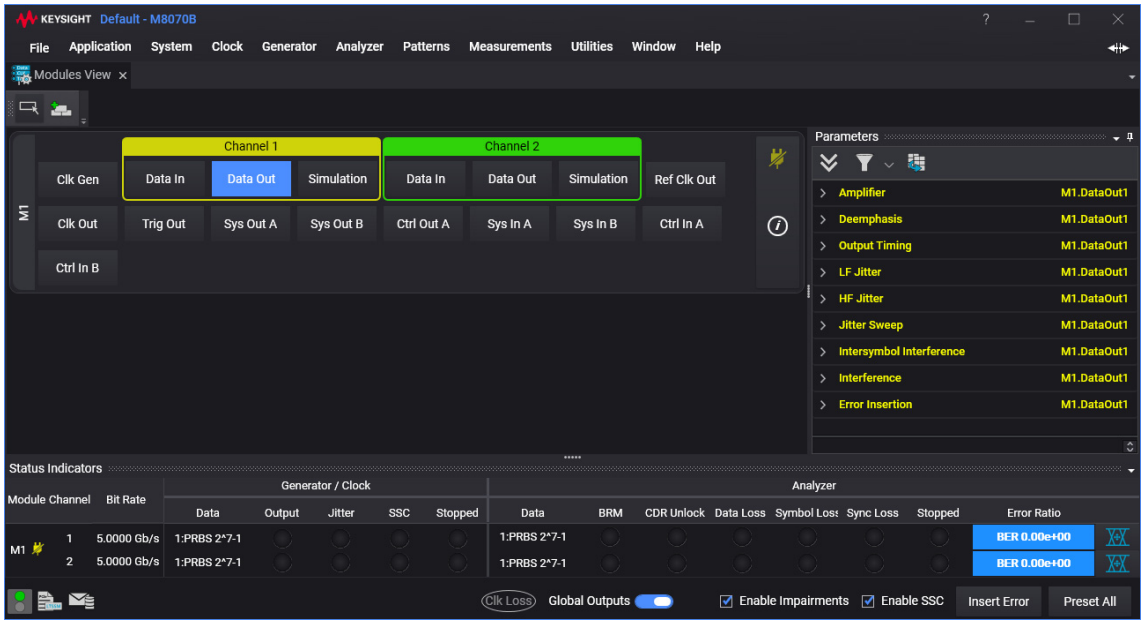
The **Load Setting** dialog provides the following settings:

- **Last Used**: Launches the M8070B user interface with the last used settings.
- **Factory Preset**: Launches the M8070B user interface with factory default settings.
- **Select...**: Opens the **Recall Instrument State** dialog which allows you to load the M8070B user interface with the stored settings. For details, refer to Recall Instrument State on page 169.
- **Exit Application**: Terminates the M8070B application.

NOTE The **Load Setting** dialog will appear each time the M8070B software is launched.

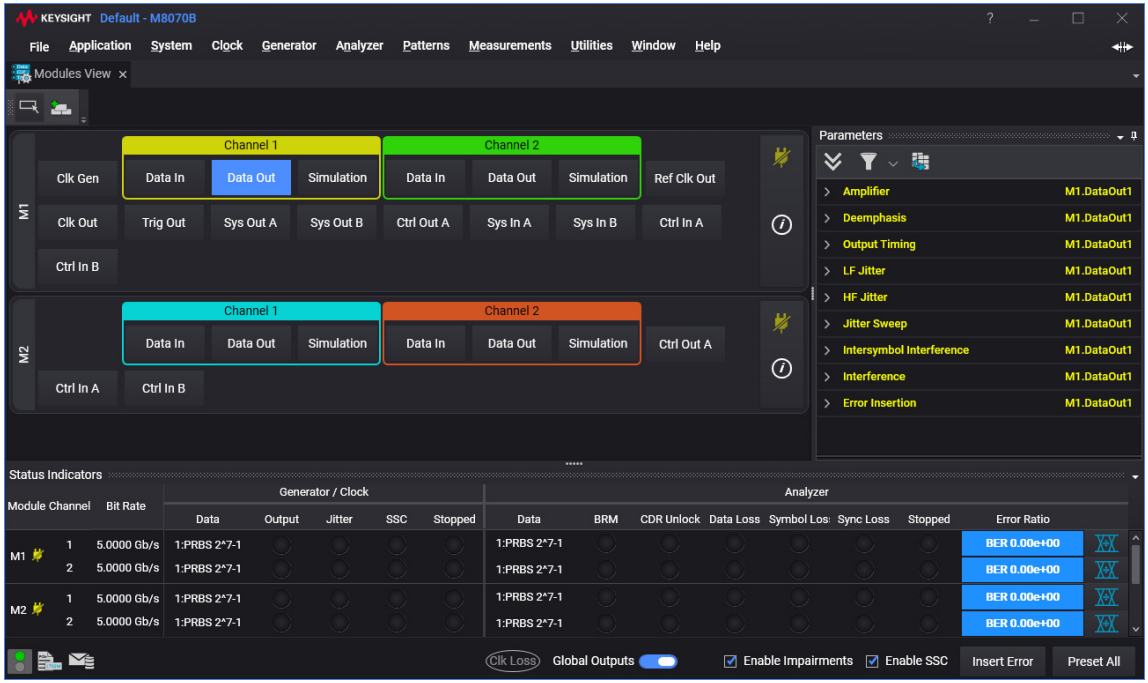
NOTE A warning message will appear on the top of **Load Setting** dialog if the modules are offline. In this case, the results are simulated.

Once the settings are loaded, the M8070B software launches. The following figure shows the an example of M8070B user interface when there is only one module connected to the M8020A system.



In the similar way, modules are also shown they are connected to the M8040A/M8050A system. Details on the **Module View** is further described in the section Module View on page 179.

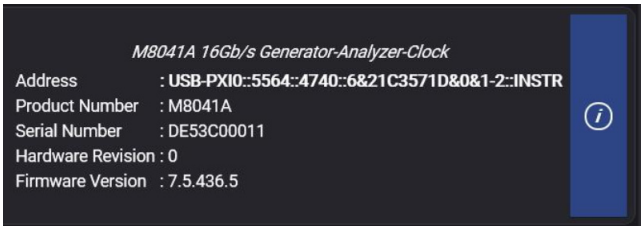
The following figure shows an example when two modules connected to the M8020A system:



In the similar way, modules are also shown they are connected to the M8040A/M8050A system. Details on the **Module View** is further described in the section Module View on page 179.

Get Module Information

You can get the module information that is connected to the M8020A/M8040A/M8050A by clicking the icon present at the right side of each module. If properly connected, the module information will be shown as depicted in the following figure:



It provides the following information about the module:

- **Address** - Address of module, e.g. USB-PXIO::11::0::INSTR
- **Product Number** - Product no. of the module, e.g. M8041A
- **Serial Number** - Serial no. of the module, e.g. DE53C00061
- **Hardware Revision** - Hardware revision of module, e.g. 0

However, if you unable to get the module information, we suggest you to restart the M8070B software.

In the off-line mode, the icon will appear in the M8070B GUI.

Exploring M8070B User Interface

The M8070B user interface consists of the following GUI elements:

- Title Bar
- Menu Bar
- Main Window
- Status Bar

The detailed information on these GUI elements are described in the following sections.

Title Bar

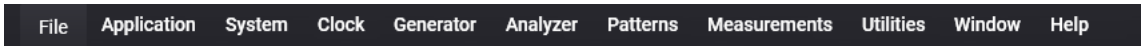
The title bar contains an application icon, title, a context-sensitive help icon and standard buttons to minimize, maximize or to close the window.

The ? context-sensitive help icon provides information about the M8070B user interface relative to the task a user performs.

The title bar is shown in the following figure.

Menu Bar

The menu bar consists of various drop-down menus which provide access to different functions, and launch interactive GUI controls.



The menu bar includes the following drop-down menus:

- File
- Application
- System
- Clock
- Generator
- Analyzer
- Patterns

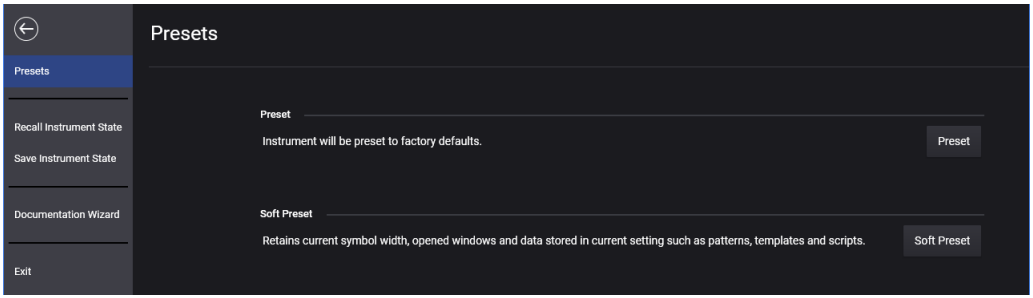
- Measurements
- Utilities
- Window
- Help
- Increase/Decrease Splitter Size

Each drop-down menu and their options are described in the following sections.

File Menu

The **File** menu provides the following selection:

- **Presets** - Opens the **Presets** dialog.



This dialog allows you to:

- **Preset** - Resets the parameters to their default values.
  You can also perform a soft preset/preset to the instrument by sending *RST command in the SCPI panel. For details on *RST command, refer to *M8000 Series Programming Guide*
- **Soft Preset** - This option resets the instrument state to factory default settings. However, it retains current symbol width, opened windows and data stored in current setting such as patterns, templates and scripts.

- **Recall Instrument State...** - Opens the **Recall Instrument State** dialog which allows you to retrieve the user-defined settings or the factory settings.
  For more details, refer to Recall Instrument State on page 169.
- **Save Instrument State...** - Opens the **Save Instrument State** dialog which allows you to save the current instrument state.
  For more details, refer to Save Instrument State on page 171.

- **Documentation Wizard** - Opens the **Documentation Wizard** dialog which allows you to save data to a compressed (.zip) folder. For more details, refer to Documentation Wizard on page 172.
- **Exit** - Closes the M8070B user interface.

Application Menu

The **Application** menu allows you to select application specific features for the following:

- PCI Express
- USB
- SATA
- MIPI C-PHY/D-PHY (Included in separately available MIPI plug-in)
- 10 GBASE KR Link Training (For details, refer to the *10 GBASE KR Link Training User Guide*)
- M8070OBLT Out-of-Band Link Training Package (For details, see *M8070OBLT Package User Guide*).

On selecting any of these standards from the **Application** menu, a standard specific dialog or plug-in interface will appear.

System Menu

The **System** menu allows you to launch the various display views provided by M8020A/M8040A/M8050A. It provides the following selections:

- **Module View** - The **Module View** is a graphical representation of the input/output ports that are present on the front panel of the modules, connected to the M8020A. You can use the Module View to configure the properties of a single port or a group (combination of multiple ports). For details, refer to Module View on page 179.
- **System View** - The **System View** displays the block representation of the currently selected channel of the M8020A/M8040A/M8050A. In addition, it also allows you to interactively modify the configuration settings for each channel. For details, refer to System View on page 209.
- **Groups View** - The **Group View** allows you to create a group of ports and re-program their properties. For details, refer to Group View on page 234.

- **Impairment Setup View** - The **Impairment Setup View** provides a tabular representation of the Impairment Sources and their corresponding parameters for each Data Out channel of the connected modules. This tabular visualization helps you to view, compare and configure the Impairment Source parameters for each channel in the same window. For details, refer to Impairment Setup View on page 222.
- **Setup View** - The **Setup View** shows the block diagram of the pattern generator and error detector to provide a simple overview of the most important instrument settings at a glance. For details, refer to Setup View on page 240.
- **Custom View** - The **Custom View** allows you to simplify the configuration process by consolidating all the necessary parameters into a single, easy-to-use interface. Instead of navigating through multiple views, you can configure everything at one place, significantly improving efficiency and usability. For details, refer to Custom View on page 247.
- **Ctrl In/ Ctrl Out** - Opens the **Module View** with the Ctrl In/Ctrl Out ports selected and the corresponding parameters are reflected in the **Properties** window.
- **Sys In/Out A/B** - Opens the **Module View** with the Sys In/Out ports selected and the corresponding parameters are reflected in the properties window.

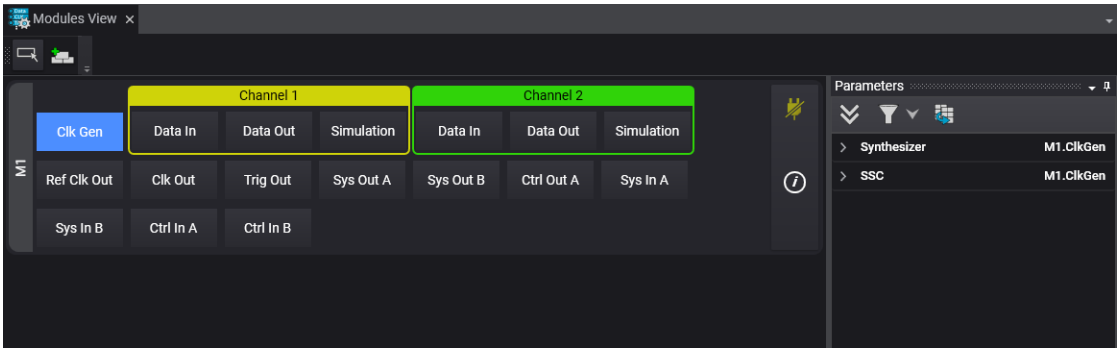
Clock Menu

The **Clock** menu provides the following selections:

- **Clock Generator** - Allows you to configure **Clk Gen** port.
- **Clock Output** - Allows you to configure **Clk Out** port.

Once you make a selection, the **Module View** appears with the **Clk Gen/Clk Out** ports selected and the corresponding parameters are reflected in the **Properties** window.

The following figure shows the **Module View** with the **Clk Gen** port selected:



The generator's output ports are used to supply a clock signal and trigger for another device (for example, analyzer), and an arbitrary data signal for testing your device. For details, refer to Setting up Generator on page 357.

To change bit rate, go to the **Properties** window and then click on the **Synthesizer** function block.

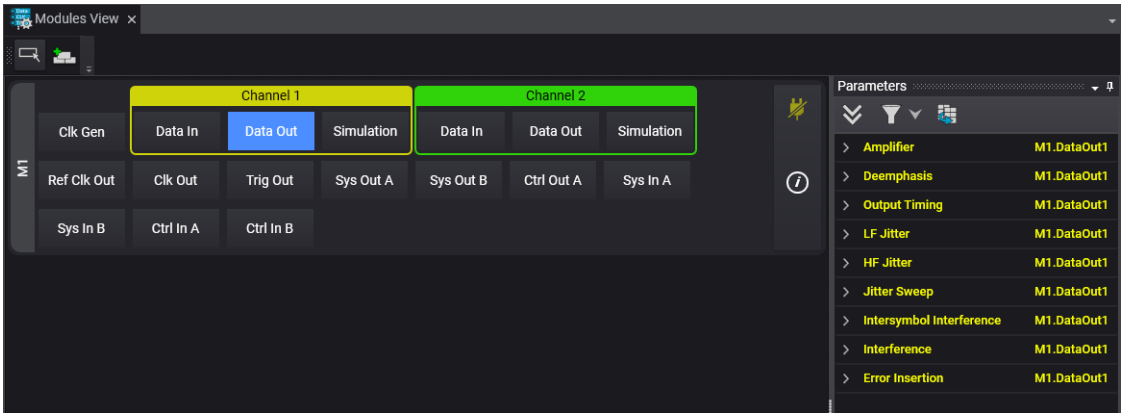
Generator Menu

The **Generator** menu provides the following selections:

- **Data Output** - Allows you to configure **Data Out** port.
- **Trigger Out** - Allows you to configure **Trig Out** port.

Once you make a selection, the **Module View** shows the **Data Out/Trig Out** ports selected and the corresponding parameters are reflected in the **Properties** window.

The following figure shows the **Module View** with the **Data Out** port selected:



The generator's ports are used to set the clock frequency and the output signal with respect to jitter, error insertion and signal output. For details, refer to Setting up Generator on page 357.

To change amplitude/offset, go to **Properties** window and then click the **Amplifier** function block.

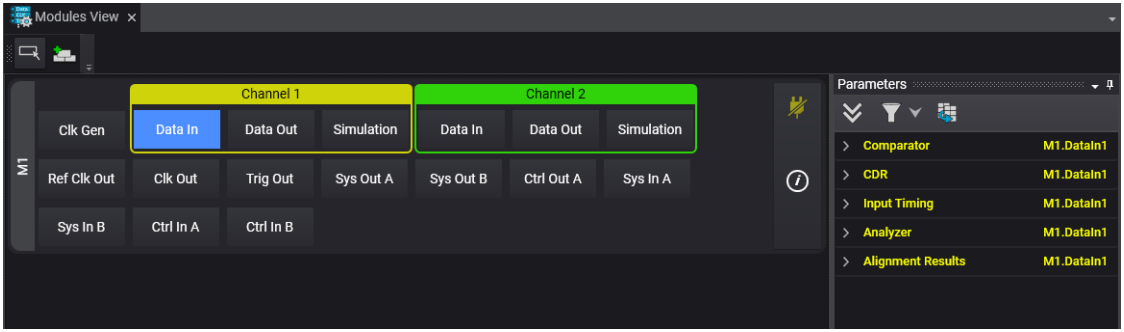
Analyzer Menu

The **Analyzer** menu provides the following selections:

- **Data Input** - Allows you to configure **Data In** port.

Once you make a selection, the **Module View** shows the **Data In** ports selected and the corresponding parameters are reflected in the **Properties** window.

The following figure shows the **Module View** with the **Data In** port selected:

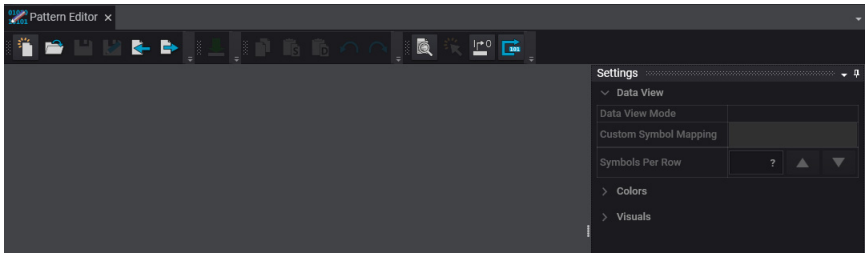


The analyzer's ports are used for running tests and for connecting external equipment. For details, refer to Setting up Analyzer on page 509.

Patterns Menu

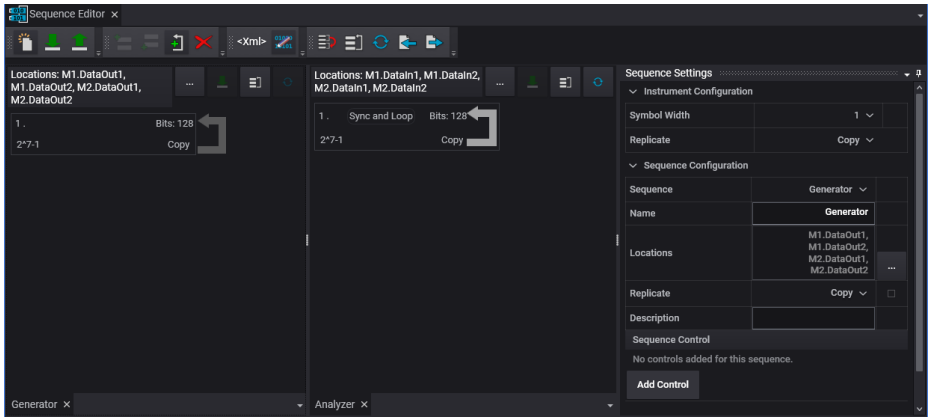
The **Patterns** menu provides the following selections:

- **Select Pattern...** - Opens the **Select Sequence Pattern** dialog. It allows you to override all sequences with a single block loop. For details refer to Pattern Editor on page 655.
- **Pattern Editor** - Opens the **Pattern Editor** user interface as shown in the following figure:



The pattern editor provides an interactive user-interface for creating, editing and importing patterns. For details, refer to Pattern Editor on page 655.

- **Sequence Editor** - Opens the **Sequence Editor** user interface as shown in the following figure:



The **Sequence Editor** allows you to create and maintain sequences. In addition to this, it also allows you to edit the memory patterns. For details, refer to Sequence Editor on page 613.

Measurements Menu

The M8070B system software provides the following types of measurements:

- **Error Ratio** – The error ratio measurement allows you to collect measurement data over a specific period. This can be used to create test scenarios that are reproducible and comparable. Also, you can let tests run over long times and then evaluate the results afterwards. For details, refer to Error Ratio Measurement on page 774.

In addition, the M8070B system software also provides the following measurements will be only available on installing the following plugins:

- **Advanced Measurement Package**

  The **Advanced Measurement Package** provides the following measurements:

  - Output Timing
  - Output Level
  - Jitter Tolerance
  - Eye Diagram
  - Parameter Sweep
  - BER Based Deemphasis

  For details on the measurements provided by **Advanced Measurement Package**, refer to *M8000 Series Advanced Measurement Package User Guide*.

- **Error Distribution Analysis Package**

  The **Error Distribution Analysis Package** provides the following measurement:

  - Error Distribution Analysis

  For details on the measurement provided by **Error Distribution Analysis Package**, refer to *M8000 Series Error Distribution Analysis Package User Guide*.

Utilities Menu

The **Utilities** menu provides the following selections:

- **Logger** - The Logger window displays errors, warnings and information messages along with their respective descriptions, applications from where they are generated and their time stamps. For details, refer to Logger Window on page 803.
- **Script Editor** - The Script Editor provides flexibility to the programmers to automate their plug-ins thus allowing them to do everything they want in the measurements. Launches the Script Editor which enables the programmers to automate their plug-ins. For details, refer to *M8070ADVB Advanced Measurement Package User Guide*.

NOTE Please note that the Script Editor is supported by the Advanced Measurement Package which requires a license for its activation. For details, refer to *M8070ADVB Advanced Measurement Package User Guide*.

- **DUT Control Interface** - The DUT Control Interface allows you to control a device under test at well defined positions within the measurements of the M8070B software. For details, refer to *M8070ADVB Advanced Measurement Package User Guide*.

NOTE Please note that the DUT Control Interface is supported by the Advanced Measurement Package which requires a license for its activation. For details, refer to *M8070ADVB Advanced Measurement Package User Guide*.

- **SCPI Editor** - The SCPI Editor lists all SCPI that can be used to program M8020A/M8040A/M8050A and also provides a platform to execute them. For details, refer to *M8070ADVB Advanced Measurement Package User Guide*.

NOTE Please note that the SCPI Editor is supported by the Advanced Measurement Package which requires a license for its activation. For details, refer to *M8070ADVB Advanced Measurement Package User Guide*.

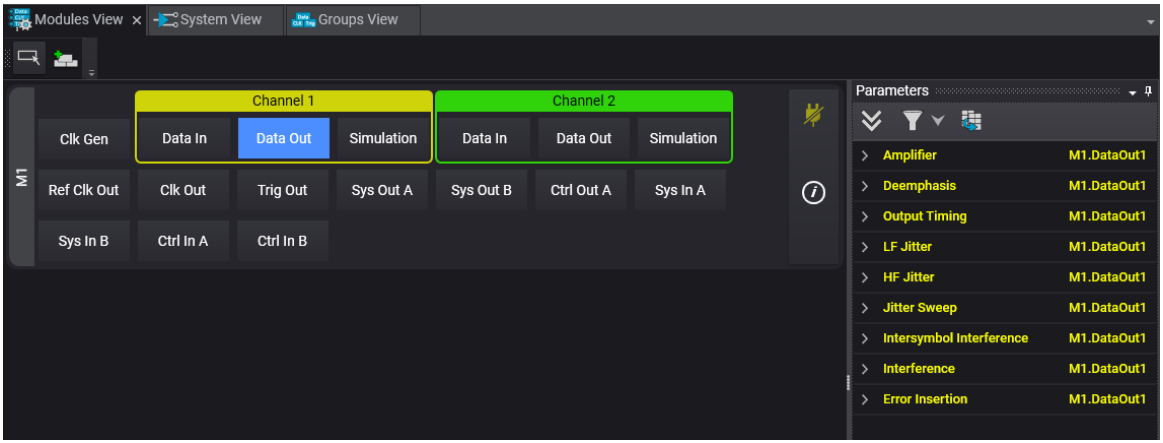
- **SCPI Recorder** - The SCPI recorder enables you to quickly discover, record, and learn about the commands needed to perform almost any task remotely. For details, refer to SCPI Recorder on page 791.
- **SCPI Server Information** - This dialog lists the VISA resource and remote access strings to connect instruments. or details, refer to SCPI Server Information on page 804.
- **Licenses...** - Opens the **Licenses** window that displays the license information currently installed in the modules or host. For details, refer to Licenses Window on page 799.
- **Manage Plug-ins...** - The **Manage Plug-ins...** option simplifies all the tasks related to plug-in management. It displays list of plug-ins that are installed in the software. In addition, the **Manage Plug-ins...** also allows you to install, uninstall and update the plug-ins. For details, refer to Manage Plug-ins on page 805.
- **Manage Instrument Drivers** - The **Manage Instrument Drivers** utility simplifies all the tasks related to instrument driver management. It displays a list of instrument drivers that are installed in the M8070B software. For each instrument driver, it displays information such as Name, Version, Vendor, Description, State, and Build Date. In addition, the **Manage Instrument Drivers** also allows you to install, uninstall, and upgrade the instrument drivers. For details, refer to Manage Instrument Drivers on page 813
- **Services > Self Test** - The **Self Test** utility checks the specific system information of the hardware components for basic functionality. For details, refer to Self Test Utility on page 794.
- **Preferences...** - Opens the **Preferences** window which allows you to set the display and channel settings in the user interface. For details, refer to Preferences Window on page 800.

Window Menu

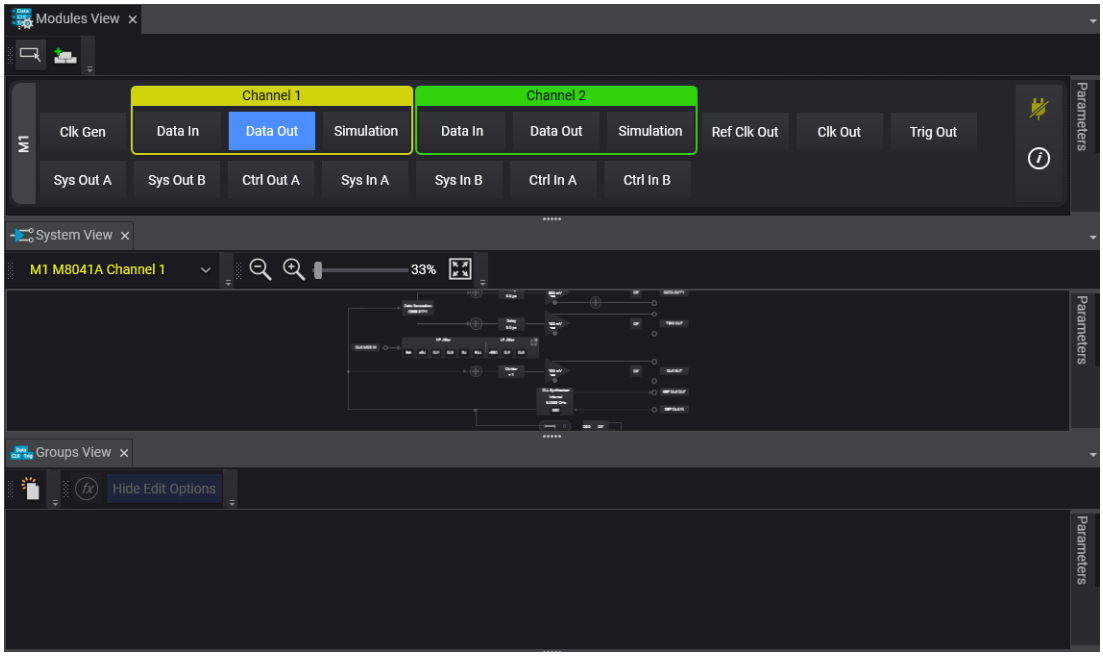
The **Window** menu allows you to change the layout/arrangement of various open windows. It includes the following selections:

- **Floats** - Allows you to float the selected window.
- **Dock** - Docks the selected window.
- **Grid Layout** - The Grid Layout option contains the following:
  - **Cascade** - Arranges the multiple opened windows in a docked view so that you can see all or part of each window; consisting of individual tabs for each window.

The following figure shows the docked/tabbed view of three different windows.



- **Tile Horizontally** - Aligns the multiple opened windows in a horizontal sequence. The following figure shows the horizontal sequence of three different windows.



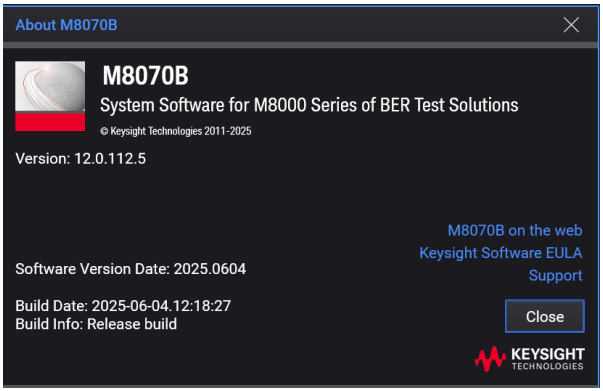
- **Tile Vertically** - Aligns open windows in a vertical sequence. The following figure shows the vertical sequence of three different windows.

- **Focus Center Content** - Minimizes or hides additional dialog boxes or property sheets of the multiple open windows to focus on the center content.
- **Close All** - Closes all the open windows.

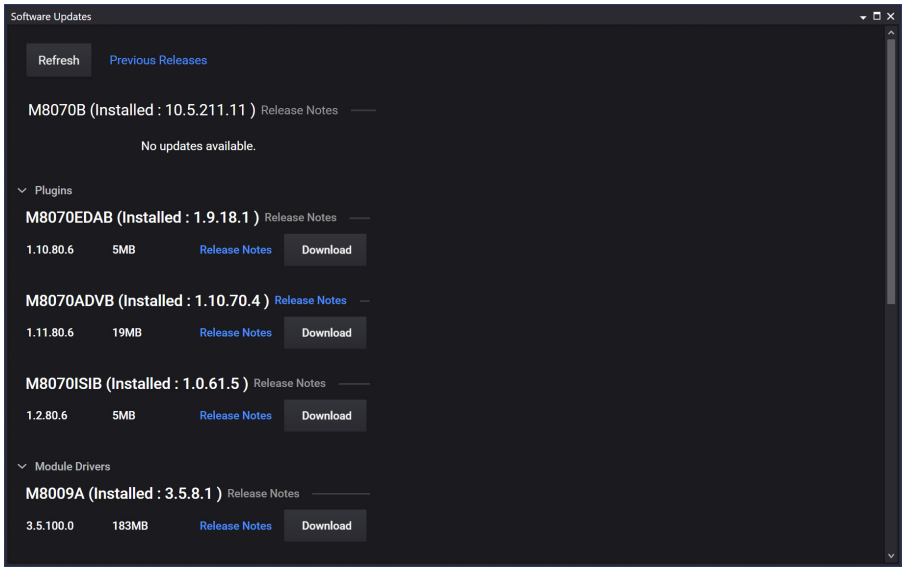
Help Menu

The **Help** menu includes the following selections:

- **Help Contents (F1)** - Opens the online help that provides the information about the Keysight M8070B.
- **Technical Support >** - It provides the following selections:
  - **Keysight Community** - Opens the **Keysight Community Help** page in the web browser.
  - **My Support ID** - Opens **My Support ID** window that displays the information on the installed licenses, their description and Host ID.
  - **My Support Subscription** - Opens the **My Support Subscription** window that displays information on the installed licenses, their description, software version on which they are installed, software version date and support subscription.
- **Keysight Software Manager Utility** - Opens the **Keysight Software Manager Utility** window, which allows you to manage all types of Keysight licenses for a wide variety of software products and instruments. For more information, refer to Keysight Software Manager Utility on page 843.
- **PathWave Calibration Advisor** - Opens the **PathWave Calibration Advisor** window which allows you to set the calibration interval, configure calibration due reminders, check the calibration status, view calibration certificates and test reports, and contact Keysight for a calibration service. For details, see PathWave Calibration Advisor on page 173.
- **About M8070B** - Provides detailed product information for M8070B, including version number, build date, build details, and web links for M8070B information, Keysight software EULA, and support.



- **Check for Updates** - Opens the **Software Updates** window, which displays the currently installed versions of the M8070B software, plugins, and module drivers and also provide option to download and install their latest software versions.



You can perform the following actions in the **Software Updates** window:

- Click the **Refresh** button to update the software information in the **Software Updates** window.
- Click **Release Notes** to check the release information of the respective version.
- Click **Download** to download the respective version of the software, supported plugin, or module driver. If the **Download** button is not displayed, this indicates that you have the latest version installed on your system. Once the software is downloaded, the **Install** button appears.
- Click **Install** to install the respective version of the software or plugin. Ensure that you accept the Keysight software license agreement to continue installation.
- Click **Previous Releases** to download the previous version of the M8070B software, plugin, or module driver from the M8070B software download page.

Increase/Decrease Splitter Size

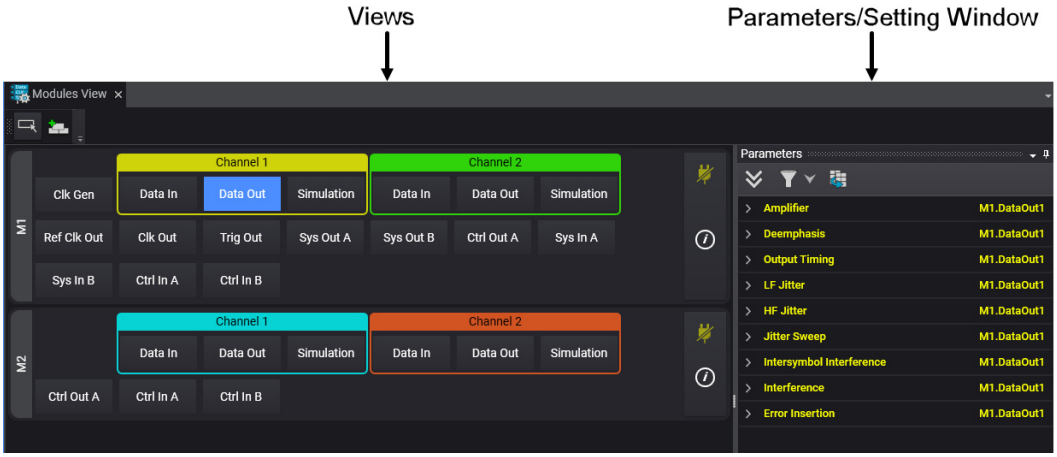
The **Splitter** option allows you to either increase or decrease the divided space between the windows forms used in the user interface. This icon is located on the right side of the menu bar. The splitter functionality provides an easy navigation to the users who are using a touchscreen interface.

Main Window

The main window refers to the middle area of the M8070B user interface that allows you to launch different display views (e.g. **Module View**, **Group View**, **System View**, etc.). You can use the menu bar to launch these views on the main window. Each view can be configured through the **Parameters** window. The detailed description of different views, their parameter settings, controls and dialogs are described in the subsequent sections in this manual.

When you launch the M8070B software, by default, it shows the **Module View** on the main window.

The following figure shows how the main window appears:



Status Bar

The status bar is located at the bottom of the M8070B user interface. The status bar is shown in the following figure:

It provides the following functions:

- Button to show/hide the **Status Indicator** window. For details, refer to Status Indicators Window on page 158.
- Button to show/hide the **Logger** window that displays errors, warnings and information messages which are generated from the M8020A/M8040A/M8050A system. For details, refer to Logger Window on page 159.
- Button to show/hide the **Show Link Training Log** window. For details, refer to Link Training Log Window on page 160.
- Error indicator for the clock loss. When there is any clock loss, the respective indicator turns red.
- Toggle button to enable/disable the **Global Outputs** and check-boxes to enable/disable the **Impairments** and **SSC** state.
- **Progress Indicator** to visualize the progression of multiple GUI operations and/or background operations in a single bar. However, if the process takes too long to complete, you have an option to terminate that process by clicking on the **Abort** button which appears on the **Status Bar**.

NOTE

The behavior of progress indicator depends upon the number of process involved in any operation. It displays progress of each individual process in a single bar. Time for each operation may vary and sometimes may be very quick. Therefore, at some instance, it may display a progress to be complete (100%) and then suddenly switch to incomplete (50%).

WARNING

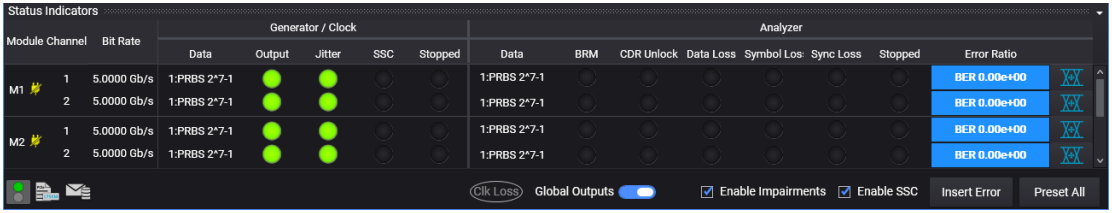
You will see a warning sign on the status bar if the “Global Output State” is off. In this case, all data outputs will be disabled until the “Global Output State” is turned on. Click the “Output” button present on the status bar to turn on the “Global Output State”.

- **Insert Error** button to insert a single bit error on each Data Out location of the connected modules.
- **Preset All** button opens the **Preset Instrument** dialog that allows to reset the instrument state to factory default settings.

Status Indicators Window

The **Status Indicators** window displays the status indicators for the generator and analyzer ports of each channel of the connected modules. This includes:

- Setup information such as **Bit Rate** for each channel of the connected module.
- Generator port information such as:
  - Data information that shows the name/type of the pattern downloaded to that data block and its indicator shows which data block is currently transmitting the sequence.
  - State information of generator such as **Output**, **Jitter** and **SSC** (indicated by green LED).
  - Error indicator for the current GUI state. When the current GUI is stopped, the respective indicator turns red.
- Analyzer port information such as:
  - Data information that shows the name/type of the pattern downloaded to that data block and its indicator shows which data block is currently transmitted the sequence.
  - State information of analyzer such as **BRM** (indicated by green LED).
  - Error indicators of analyzer such as CDR Unlock, Data Loss, Symbol Loss and Sync Loss (indicated by red LED).
  - Error indicator for the current GUI state. When the current GUI is stopped, the respective indicator turns red.
  - Calculated BER
  - **Alignment BER Threshold** button to start BER threshold auto alignment.

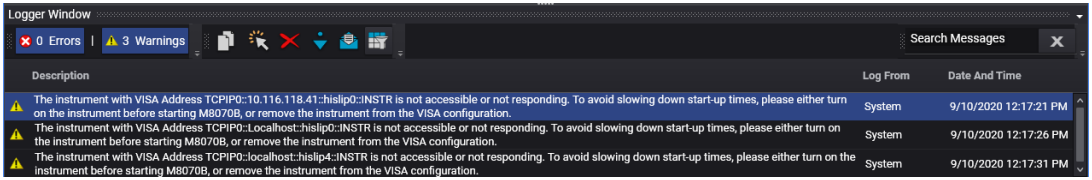


The **Status Indicator** window always appears whenever you launch the M8070B user interface. However, you can open/close this window by clicking on the **Status Indicator** button, present on the status bar.

Logger Window

The **Logger** window displays errors and warnings messages along with their respective descriptions, applications from where they are generated and their time stamps.

The **Logger** window always appears whenever you launch the M8070B user interface. However, you can open/close this window by clicking on the **Logger** button, present on the status bar.



The **Logger** window allows you to:

- **Message Selection** - Use this option to choose whether you want to view errors, warnings or information message.
- **Copy** - Use this option to copy a message. You need to select a message in order to enable copy feature.
- **Select All** - Use this option to select all messages. It also enables copying all messages.
- **Clear Messages** - Use this option to delete all messages.
- **Auto Scroll** - Use this option to enable/disable auto scroll option. When the **Auto Scroll** option is enabled, it will automatically scroll you to the new message without using the scroll bar.

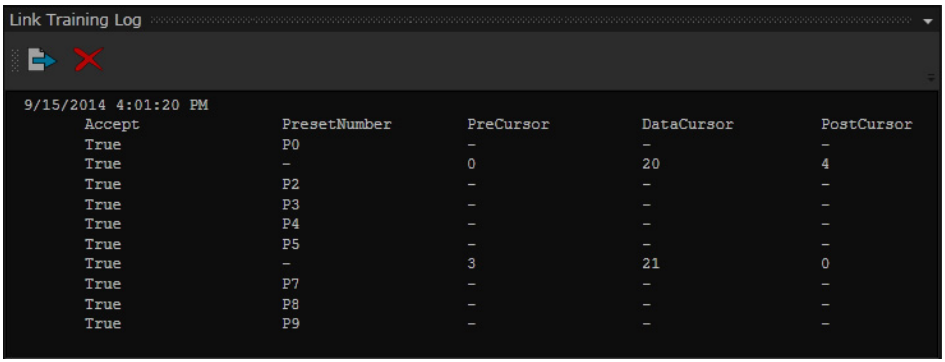
- **Open On Message** - Turn this button OFF if you don't want the Logger window to automatically pop-up whenever a message is received.
- **Column Option** - Use this button to filter the messages either from **Log From** column or **Date and Time** column.
- **Search Messages** - Use this option to search messages by providing an input in the **Search Messages** search box.

Link Training Log Window

The **Link Training Log** window displays the logs for link training PCIe 3.0.

You can open/close the **Link Training Log** window by clicking on the **Link Training Log** button present in the status bar. The **Link Training Log** button with orange background indicates an update or new entry in the link training log.

The following figure shows the **Link Training Log** window:



The **Link Training Log** window provides the following options:

- **Export Log** - Click the **Export Log** button to save the link training log.
- **Clear Logs** - Click the **Clear Logs** button to delete all link training logs.

For more details on link training, refer to Interactive Link Training on page 698.

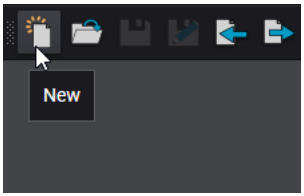
Other GUI Features

Following are the GUI elements that make the M8070B user interface interactive.

Tooltip

The tooltip is a small pop-up window that concisely describes the object being pointed to, such as descriptions of toolbar controls, icons, graphics, links, menu items and taskbar buttons.

The following example shows the tooltip providing a description of toolbar buttons.



Here is another example where the tooltip provides information to the user on the minimum and maximum values the parameter can hold.

Toggle Button

The toggle button allows you to toggle between the two features. For example, in the following figure, we are using the toggle button to either expand or collapse the parameter list.

ON/OFF Switch

The ON/OFF switch enables or disables a given feature.

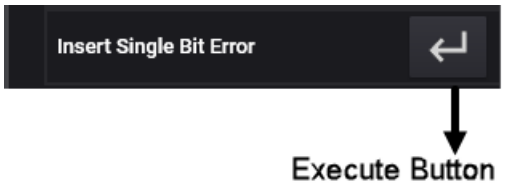
The following figure shows how a ON/OFF switch is used to turn the state feature ON.

However, at some instances in the GUI, the ON/OFF switch will be enabled when you select the corresponding check box.

Execute Button

The **Execute** button allows you to perform an activity, once you click on it.

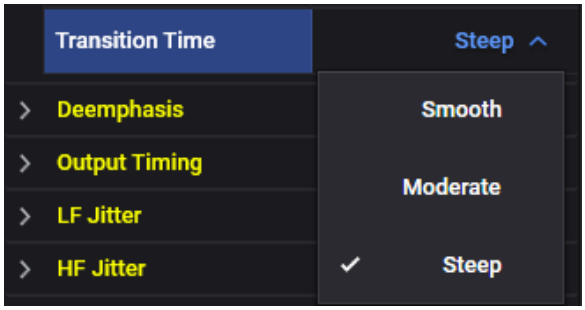
The following figure shows an **Execute** button that is used to perform pattern synchronization.



Drop-Down List

The drop-down list allows you to choose either one or sometimes multiple selections from the provided list.

The following shows the drop-down list to choose the **Transition Time**.

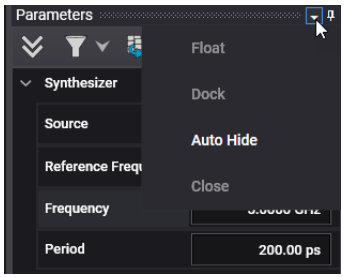


Numeric Entries

Most numeric entries have a pre-defined maximum, minimum, and default value displayed in their corresponding pop-up menu.

Numeric values in numeric entries can be changed using the on-screen numeric keypad. For details, refer On-Screen Numeric Keypad on page 166.

Window Option



The window options allow you to float or dock anywhere in the application window. It provides quick access to logically grouped features from one location. For example, you can select and generate various layouts from the single window.

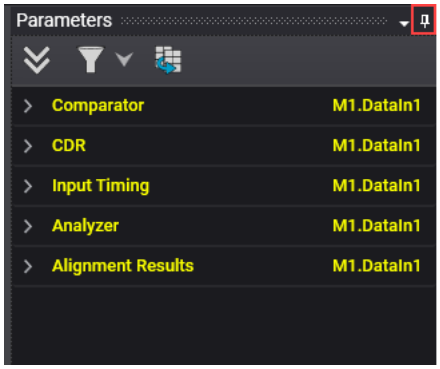
You can move a window anywhere on the screen or to a different monitor. You can also use the auto-hide feature of the windows to show or hide them on the desktop. You can also close the floating windows.

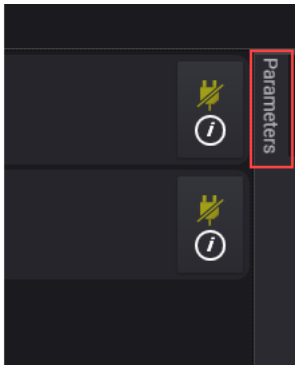
Auto Hide Feature

The automatic hiding functionality gives you the ability to imitate the behavior of the dock windows in the M8070B user interface. When it's enabled for a dock panel, this panel is automatically hidden when the mouse pointer leaves its area. Dock panels are hidden at the nearest form's edge. For example, if a panel is docked to the right edge of the form, it will be hidden at the right edge.

End-users can enable the automatic hiding functionality by clicking the auto hide button displayed within the panel's caption.

The image below illustrates how the automatic hiding functionality can be enabled and how to show the hidden dock panel.

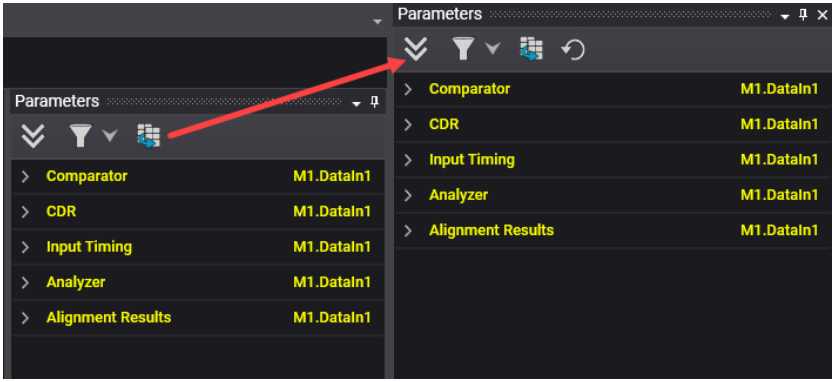




Copying Parameter Window

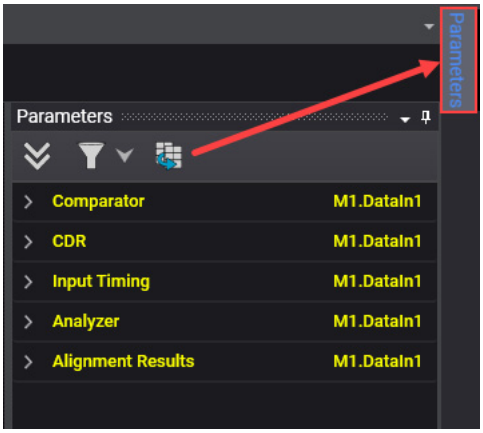
The copying feature creates a replica of parameters window to enhance the usability. It allows you to work on two different instances of the application. The changes you make in one window display immediately in the other window.

The following figure shows the copied parameters window.



Once copied and then enabling the auto hide feature, the cloned parameters window is docked to the right edge of the main user interface. The copied parameters window pops up once you click on it.

The following figure shows the copied parameters window docked to the right edge of the main user interface.



On-Screen Numeric Keypad

The on-screen numeric keypad makes it easier to enter the numbers, units, etc., specially if you are using a touchscreen monitor. The on-screen numeric keypad pops up whenever you tap mouse pointer or touch (in case of touchscreen) in a text field or other area where user inputs are required.

NOTE Remember to unselect the **Disable** Keypad option in the **Settings** window in order to enable the on-screen numeric keypad. For details, refer to Preferences Window on page 800.

The on-screen numeric keypad contains the following buttons:

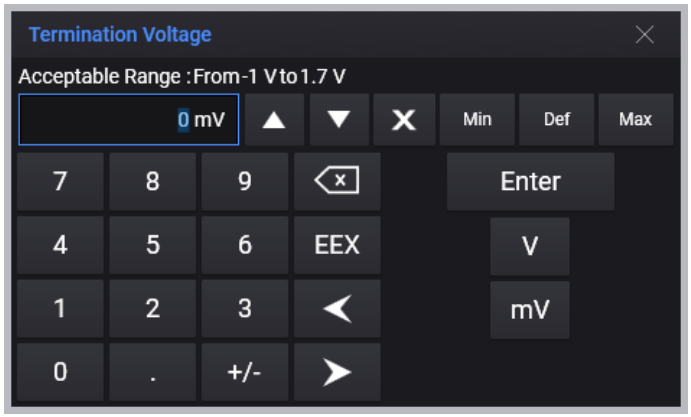
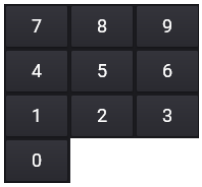


Table 48 On-screen numeric keypad

Button	Name	Description
	Number Buttons	Press these buttons to enter a numeric value. The acceptable range of a parameter is shown at the top of the keypad.
	Decimal Button	Press this button to enter a decimal numeric value.
	Function Button	Press this button to toggle between the addition (+) and subtraction (-) function.
	UP/DOWN Button	Press these buttons to increase or decrease the numeric values, respectively.
	Backspace Button	Press this button to delete any character before the current position of the pointer.
	LEFT/RIGHT Button	Press these buttons to move the pointer one position left or right, respectively.
	Exponent Button	Press this button to enter exponents.
	Enter Button	Press this button to apply the value.

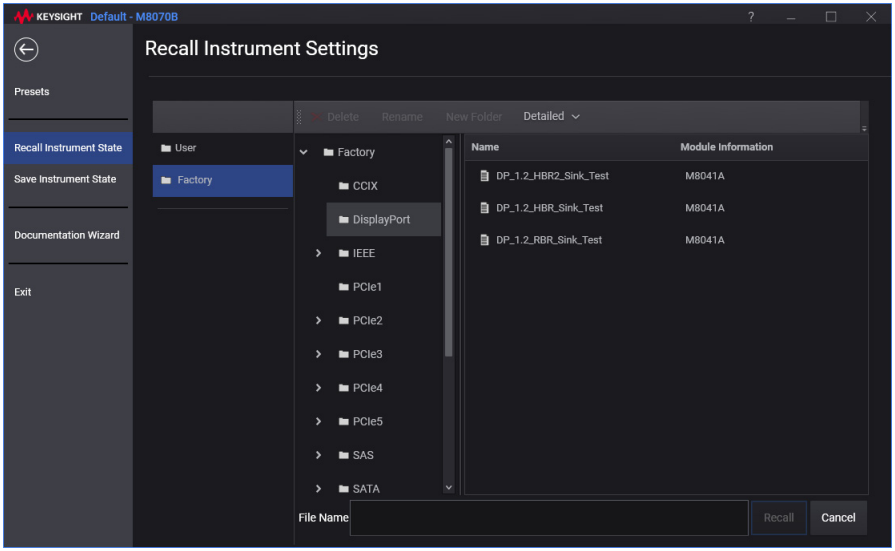
Button	Name	Description
mV	Units Button	Press this button to assign units to the numeric value. Please note that the units may change depending on the parameter.
✕	Clear Field Button	Press this button to clear the text field.
Min Def Max	Minimum/ Default/ Maximum Button	Press this button to insert either minimum, or default, or maximum numeric value of the parameter.

Recall/Save Instrument State

Recall Instrument State

To recall an instrument state, do the following:

1 Go to **File** menu and then click **Recall Instrument State...**. The **Recall Instrument Settings** dialog will appear as shown in the following figure.



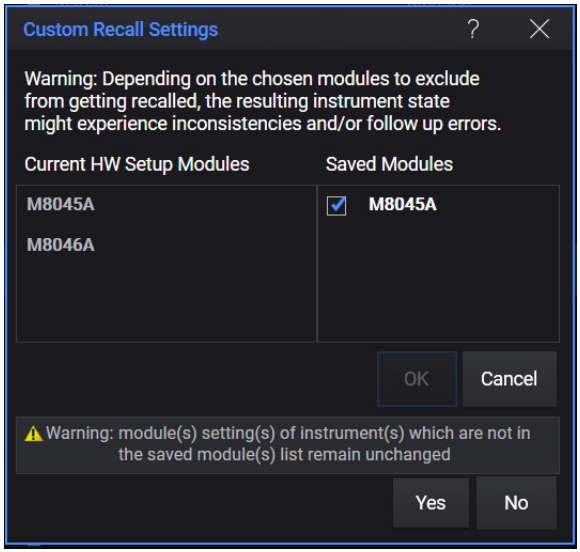
2 Select the folder (User or Factory) to view the files.

3 (Optional) You can select the **Tiles** view or **Details** view from the drop-down list. The **Details** view displays the name of the module.

4 Select the file which is to be recalled.

5 Click **Recall**.

For the recall operation to be successful, ensure that the set of hardware modules on which the recall is being done should be exactly same as the set of hardware modules on which the settings was saved. However, if there is any hardware modules mismatch, the following "**Custom Recall Settings**" dialog will appear:



This dialog displays and provides option to include/exclude the hardware modules from getting recalled. Ensure that the set of modules on which the recall is being done should match with the set of hardware modules on which the settings was saved. Once, the modules selection is done on the "**Custom Recall Settings**" dialog, click **OK**. In case of hardware mismatch, a warning message will be displayed. For example, if you have saved the settings using the hardware set which includes M8045A only, and now attempt to recall in the hardware set which includes both the M8045A and M8046A, a warning message will appear in the "**Custom Recall Settings**" dialog.
In this case, when you click **Yes**, only the settings for the M8045A module will be recalled to the current M8045A module.

NOTE The custom recall operation creates a copy of the setting, with the suffix '_modified' added to the name.

6 To rename a file, select the file and click Rename. The filename will become editable.

7 To delete a file, select the file and click **Delete**.

8 To add new folder, select location you want to create your folder and then click **New Folder**.

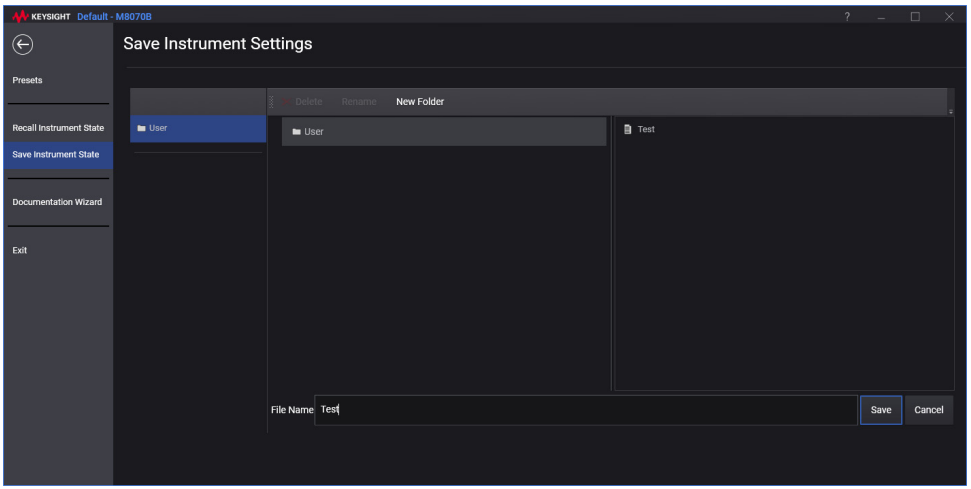
9 To rename a folder, select the folder and click **Rename**. The folder name will become editable.

10 To delete a folder, select the folder and click **Delete**.

Save Instrument State

To save an instrument state, do the following:

1 Go to **File** menu and then click **Save Instrument State...**. The **Save Instrument Settings** dialog will appear as shown in the following figure.



2 Enter a file name and click **Save**. The current settings will be saved under the filename.

3 To rename a file, select the file and click **Rename**. The filename will become editable.

4 To delete a file, select the file and click **Delete**.

5 To add new folder, select location you want to create your folder and then click **New Folder**.

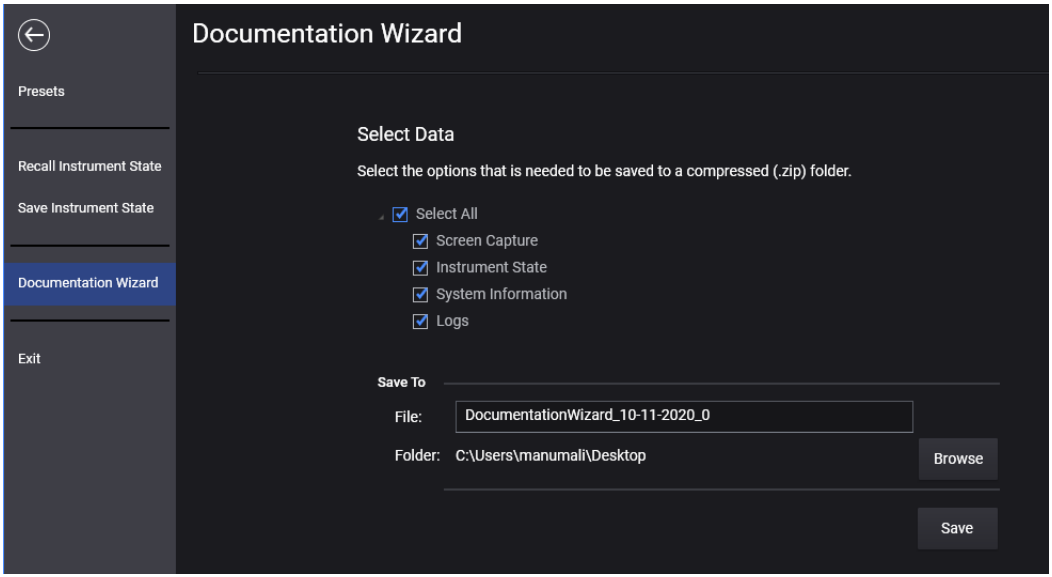
6 To rename a folder, select the folder and click **Rename**. The folder name will become editable.

7 To delete a folder, select the folder and click **Delete**.

Documentation Wizard

To save the data to a compressed (.zip) folder, do the following:

1 Go to **File** menu and then click **Documentation Wizard**. The **Save Documentation Wizard** dialog will appear as shown in the following figure.



2 Select the options that is needed to be saved to a compressed (.zip) folder. The following options are available:
   - Select All
     - Screen Capture
     - Instrument State
     - System Information
     - Logs
3 Type an appropriate name for the file in the **File** text box.
4 Browse to the location where you want to save the file.
5 Click **Save**.

A compressed file with the same name is saved at the location.

PathWave Calibration Advisor

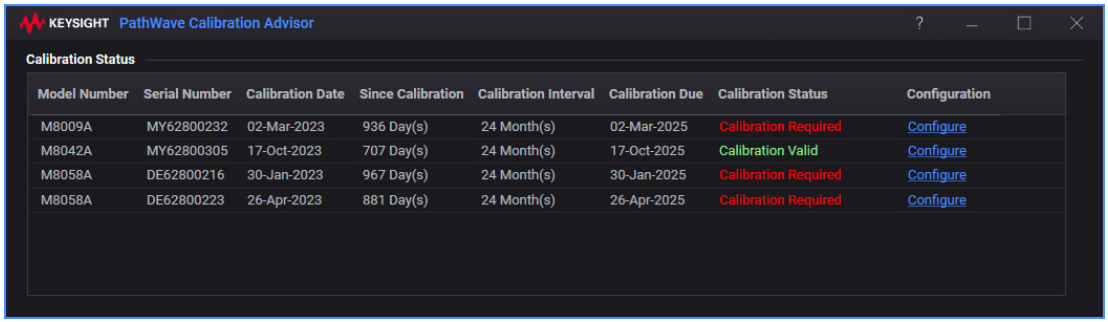
Overview

PathWave Calibration Advisor helps maintain your instrument at peak performance. You can set the calibration interval, configure calibration due reminders, check the calibration status, view calibration certificates and test reports, and contact Keysight for a calibration service.

This option is available under the **Help** menu of the M8070B user interface.

NOTE **Currently, the PathWave Calibration Advisor is only supported by M8050A modules (M8042A & M8043A).**

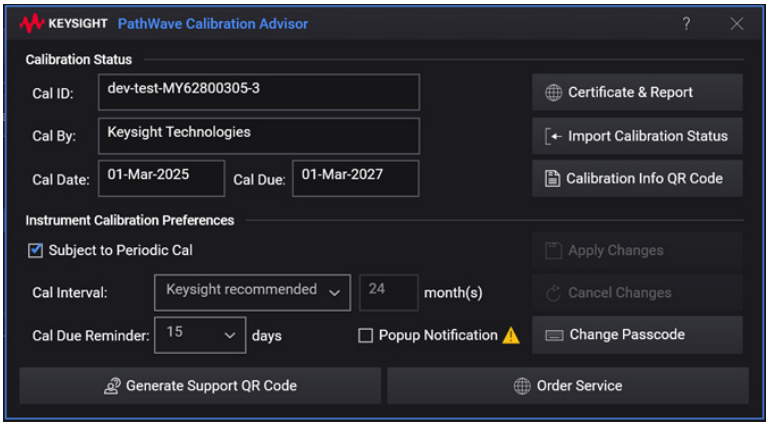
Exploring User Interface



Model Number	Serial Number	Calibration Date	Since Calibration	Calibration Interval	Calibration Due	Calibration Status	Configuration
M8009A	MY62800232	02-Mar-2023	936 Day(s)	24 Month(s)	02-Mar-2025	Calibration Required	Configure
M8042A	MY62800305	17-Oct-2023	707 Day(s)	24 Month(s)	17-Oct-2025	Calibration Valid	Configure
M8058A	DE62800216	30-Jan-2023	967 Day(s)	24 Month(s)	30-Jan-2025	Calibration Required	Configure
M8058A	DE62800223	26-Apr-2023	881 Day(s)	24 Month(s)	26-Apr-2025	Calibration Required	Configure

This window includes calibration information, calibration status, and configuration buttons for each running module.

- **Configuration**: Click **Configure** to display the calibration information details and change preferences.



Calibration Status

Feature	Description
Cal ID	Calibration ID number. It can be the same as the calibration certificate number when the instrument is calibrated by Keysight.
Cal By	The service provider that provided the calibration service.
Cal Date	Date of the calibration.
Cal Due	Calibration due date. It is calculated as Cal Date + Cal Interval (click here for exceptions).
Certificate & Report	Get a link to view the instrument's calibration certificate and measurement report online.
Import Calibration Status	Import the calibration status (download and/or import file).
Calibration Info QR Code	Generate and display a QR code that contains the instrument's calibration status and settings.

Instrument Calibration Preferences

Feature	Description
Subject to Periodic Cal	Check this box if the instrument is planned to be calibrated periodically (recommended). If unchecked, Cal Interval, Cal Due, Cal Due Reminder, and Popup Notification are not applicable.
Cal Interval	Set the interval between calibrations. Options are: ▪ Keysight recommended: Use the product-specific Keysight recommended calibration interval. ▪ User defined: You can set the interval to be 1 to 120 months.
Cal Due Reminder	Select how many days before the Cal Due date to start displaying the calibration due popup reminder at 12:00 AM every day. Options are 30 days, 15 days, or 7 days.
Popup Notification	Enable or disable the Calibration Status reminder popup. If disabled, the notification will pop up only at power on. If enabled, the notification will also pop up at 12:00 AM every day when the current date is ≤ the Cal Due Reminder days.
Apply Changes	Saves any changes you made to the Instrument Calibration Preferences. **NOTE:** A passcode is required to save changes.
Cancel Changes	Cancels any changes and restores them to the last saved state.
Change Passcode	Allows you to establish a new passcode or reset the passcode to the factory default ("Key4Cal"). **NOTE:** The passcode is case-sensitive.

Generate Support QR Code

Clicking this button generates and displays a QR code that contains the current instrument configuration data. Take a photo of the QR code and include it in your communication with the Keysight support center.

In addition to displaying the QR code, the pop-up dialog also displays the QR code content if you select "Display the QR code content." at the bottom of the dialog. This is a helpful way to view and capture all important configurations.

NOTE Be sure to hide the QR code content before taking a photo of the QR code.

Order Service

If your instrument is connected to the Internet, click this button to access the Keysight Support Portal, where you can order service for your instrument.

Help

If you have any queries about **PathWave Calibration Advisor**, contact Keysight at keysight.com/find/contactus.

Remote Programming

These calibration settings can also be executed using the remote programming. For details of these commands, refer to the *M8000 Series Programming Guide*.

M8000 Series of BER Test Solutions
User Guide

4 User Interface - M8070B Display Views

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KEYSIGHT TECHNOLOGIES

Overview

The M8070B system software provides the following types of views:

- Module View
- System View
- Impairment Setup View
- Group View
- Setup View

In addition, on installing the **Advanced Measurement Package**, the following instruments can be controlled from M8070B System Software:

- N1076A/77A
- N1076B/78A
- Real-Time Oscilloscope

Description on the **Advanced Measurement Package** and steps to control the above instruments are explained in the *M8000 Series Advanced Measurement Package User Guide*.

NOTE Please note that the Advanced Measurement Package requires license for its activation. For details on license, see M8070B Plugin Licenses on page 839.

NOTE Verify your account permissions. Ensure that you have full administrative privileges (run as Administrator) before you install or upgrade the M8070B system software on a PC running Windows 11 or Windows 10 IoT Enterprise. Not doing so may result in installation failure. Please contact your system administrator to provide you the administrative rights.

Module View

The **Module View** is a graphical representation of the input/output ports that are present on the front panel of the modules, configured into the M8020A/M8040A/M8050A. The M8020A supports the M8041A (Generator, Analyzer, Clock Module), M8051A (Generator-Analyzer) and M8062A modules that are installed into an Keysight M9505A 5-slot AXIe chassis. The M8040A supports the M8045A (Generator) and M8046A (Analyzer) modules that are installed into an Keysight M9505A 5-slot AXIe chassis. The M8050A supports the M8009A (Clock), M8042A (Generator) and M8043A (Analyzer) modules that are installed into an Keysight M9505A 5-slot AXIe chassis. These modules have a different set of input/output ports depending upon their functionality e.g. generator, analyzer or clock. Each module consists of two channels (channel 1 and channel 2) depending upon the licenses, you have ordered. Each channel contains Data Out (Generator) and Data In (Analyzer) ports.

The modules are identified as M1, M2, M3 and so on in the GUI.

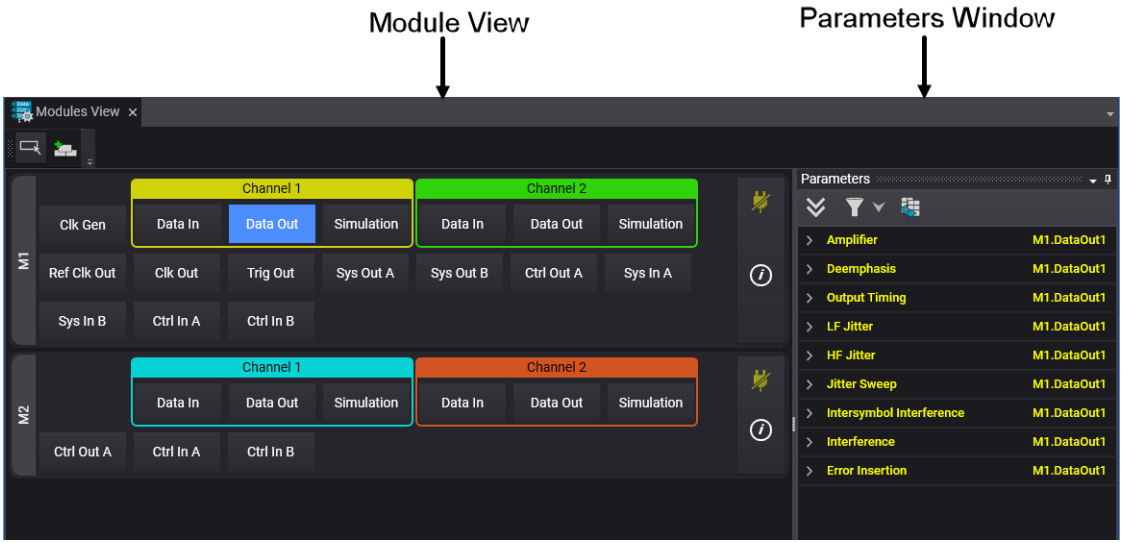
You can use the **Module View** to configure the properties of a single port or a group (combination of multiple ports). For details, refer to Group View on page 234.

How to Launch Module View

The **Module View** is launched by-default whenever you launch the M8070B user interface. However, if it is not available or is closed, you still can launch it.
To do so:

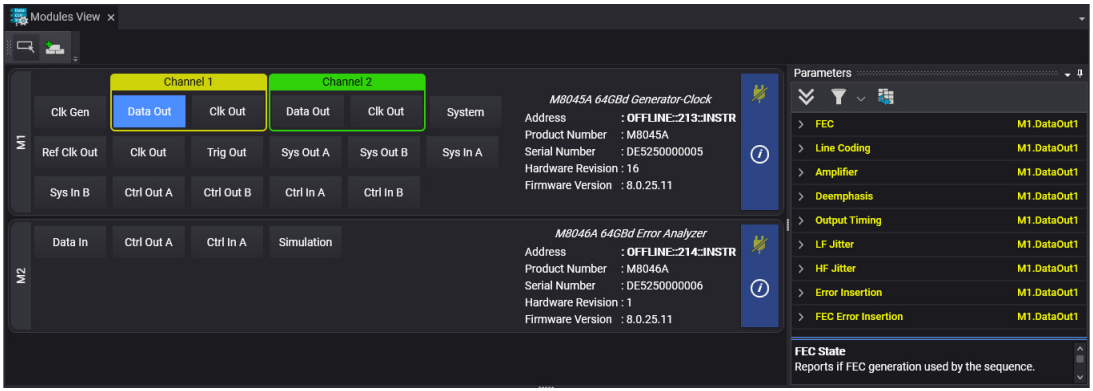
- Go to the **Menu Bar** > **System** and then select **Module View**.

The following figure shows an example of **Module View** when M8041A (M1) and M8051A (M2) modules are connected:

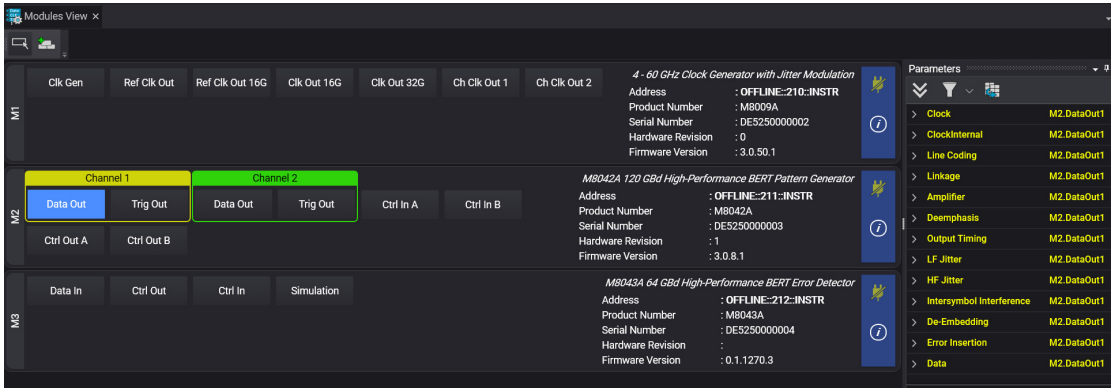


The left side shows the connected modules and the right side shows the **Parameters** window. Each module has input and output ports which can be configured through the **Parameters** window. For details on inputs and output ports, refer to Input and Output Ports on page 182. When you click on the port, the respective configurable parameters are displayed in the **Parameters** window. For details, refer to Parameters Window on page 189.

The following figure shows an example of **Module View** when M8045A (M1) and M8046A (M2) modules are connected:



The following figure shows an example of **Module View** when M8009A (M1), M8042A (M2) and M8043A (M3) modules are connected:



Input and Output Ports

M8041A and M8051A Modules

The M8041A (8.5/16G Generator, Analyzer, Clock Module) and M8051A (Generator-Analyzer) modules can have the following input and output ports:

- **Clock Gen**: Clock can be generated from the internal oscillator or an external source.
- **Data Out**: Data Out acts as the output port for the Generator which may be connected to the DUT. The data outputs serve as device stimuli and can be set up so that they are compatible with a variety of logic families.
- **Data In**: Data In acts as the input port for the Analyzer. This port is connected to the data signal which is the output of the DUT. Here the signal received and the signal generated internally is compared for calculating the bit error ratio.
- **Ref Clk Out**: The reference clock output is used to provide a 10 MHz or 100 MHz reference clock to the DUT or other test equipment (SMA, female).
- **Clock Out**: The clock out port serves as frequency (bit rate) references. If we want to operate the external device at the system clock frequency then the device operating frequency can be set up using the clock out.
- **Trig Out**: Trig Out serves as an output port of the Generator. It allows you to connect a trigger for another device which can be used to provide a 10 MHz or
100 MHz reference clock to the DUT or other test equipment.
- **Sys Out A/Sys Out B**: System level control outputs used to signal events to the DUT or external instruments.
- **Ctrl Out A:** The module has one control output at the front panel with the following selectable functionality of Error Output.
- **Sys In A/Sys In B**: System level control inputs used to generate sequencer events.
- **Ctrl In A/Ctrl In B**: The M8041A and M8051A modules has two control inputs at the front panel each with the following selectable functionality of Error Add Input, Output Blanking, Electrical Idle and Gating Input.

M8062A Module

The M8062A (32Gb/s Front-end for J-BERT M8020A High-Performance BERT) module has the following ports on its front panel:

On Pattern Generator Side

- **Data In 1 and Data In 2 (Half Rate) -** Single-ended, half-rate data inputs from the M8041A module (3.5 mm, female).
- **Data Out and /Data Out -** Differential or single-ended, full-rate data output to the device under test. Unused outputs must be terminated into 50 Ω. (2.4 mm, female).
- **DMI In -** Differential Mode Interference input. Applies a single-ended, external interference source differentially to the data output (SMA, female).
- **CMI In -** Common Mode Interference input. Applies a single-ended, external interference source to both the normal and complement data output signals (SMA, female).
- **Clk Out -** Half-rate Pattern Generator clock output. Carries the same jitter as the full-rate data output.
- **Clk In -** Pattern Generator clock input (half-rate). Connect to clock output of M8041A.
- **Aux Clk In -** Alternate Pattern Generator clock input (half-rate). Typically unused.
- **Electrical Idle In -** This input is used to enable/disable the output signal by an external control signal. If the input level is above the threshold level the module enters electrical idle. Normal operation resumes when the input level is below the threshold (SMA, female).

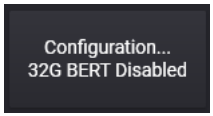
On Analyzer Side

- **Data In and /Data In -** Differential or single-ended, full-rate data input from the device under test. Unused input should be terminated into 50 Ω. (2.4 mm, female). These ports are AC coupled.
- **Data Out 1 and Data Out 2 -** Single-ended, half-rate data outputs to the M8041A module (3.5 mm, female).
- **Clk Out -** Half-rate Error Analyzer clock output, synchronous with analyzer sampling.
- **Clk In -** Half-rate, Error Analyzer clock input. Allows external clocking of the Error Analyzer.

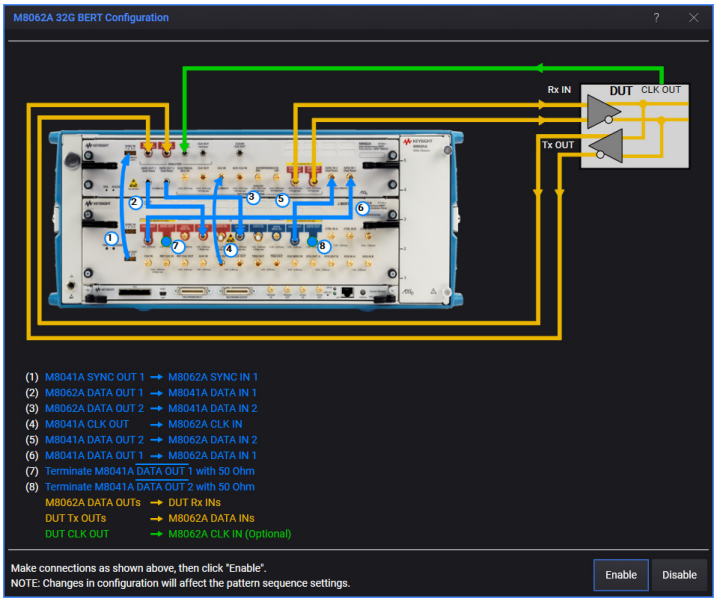
M8062A Configuration

The **M8062A Configuration** dialog provides configuration settings for M8062A. To open the **M8062A Configuration** dialog:

- Go to **Menu Bar** > **System** and then click **Module View**.
- Locate the **M8062A** module.
- Click **Configuration...** button.



The **M8062A Configuration** dialog will appear as shown in the following figure:



This dialog displays the connection diagram and connection instructions.

- Click **Enable**. In the 32G mode, access to some M8041A user controls are disabled to facilitate software control of this configuration. For the block diagram representation and to interactively modify the settings of the currently 32G mode, switch to **System View**. For details, refer System View with M8062A Integration on page 215.

M8045A Module

The M8045A module has the following ports on its front panel:

- **Remote Head - P and N Ports** - The P and N ports of each channel must be connected to the M8057A/B.
- **Clk Out1 and Clk Out 2** - These are the Clk Out ports of channel 1 and 2, respectively. It can generate either a Clean Clk or all timing impairments like Data Out.
- **Ref Clock In** - The Ref Clk In input can be used as reference frequency or as external system frequency directly for the instrument. An external provided signal can be measured at that input. This input is tightly involved in the system frequency generation.
- **Ref Clock Out** - The Ref Clk Out is used to provide a 10 MHz or 100 MHz reference clock to the DUT or other test equipment.
- **Clock Out and Clock Out** - The differential clock output serve as frequency (bit rate) reference and can be set up so that they are compatible with a variety of logic families. With respect to Clock Out, Clock Out\ has inverted logic.
- **Trigger Out and Trigger Out** - This port allows you to trigger another device (for example, an oscilloscope) and can be set up so that they are compatible with a variety of logic families. Trigger Out has more modes, e.g. sub rate clock to be used as ref clock for a DUT. With respect to Trigger Out, Trigger Out \has inverted logic.
- **Sys Out A/B** - The system level control outputs used to trigger events to the DUT or external instruments.
- **Ctrl Out A** - The control output port provides the Error Output functionality.

M8042A Module

The M8042A module has the following ports on its front panel:

- **Data Out 1, Data Out 2** - This port characteristics for M8042A with M8058A/M8059A/M8068A/M8069A. Values apply at the end of the reference cable at the outputs of the remote heads M8058A, M8059A, M8068A or M8069A.
- **Ctrl In A, Ctrl In B** - This port can be selected as: sequence trigger, error insertion.
- **Ctrl Out A, Ctrl Out B** - This port provides a pulse or static high/low if used from sequencer.
- **Trig Out 1, Trig Out 2** - This port can be used in different modes:
  - Divided clock with dividers
  - Sequence block trigger
  - Pulse mode triggered by sequencer (only if memory pattern is used)
  - “Pulse on PRBS” mode NRZ only. Matched pattern without ignoring defined bits (only if algorithmic pattern is used)

  The trigger output 2 is only available for the two-channel version of M8042A.
- **Link1, Link 2** - This port enables interactive link training with low latency between a pattern generator channel and a M8046A analyzer module. Requires cable M8051A-801. LINK 2 is only available for the two-channel version of M8042A.
- **Ch Clk In 1/2** - This port is used to connect with the M8009A clock module. The channel clock input 2 is only available for the two-channel version of M8042A.
- **Sync In** - This port is used to connect with M8009A clock module.
- **LB In, LB Out** - This port is needed for communication connected to the previous AXIe chassis. The local bus output is needed for communication connected to the next AXIe chassis.

M8009A Module

The M8009A module has the following ports on its front panel:

- **Clk Out 32G** - This port is intended to be used to drive a DUT that requires a sub-rate clock. It can contain identical jitter as channel clock output 1. The clock signal is aligned to the data pattern. Its only available on M8009A modules with option -062. It provides the signal with the frequency range from1 to 32.4 GHz.

- **Clk Out 16G** - This port provides a reference clock for a DUT. It can be operated with jitter and without jitter. It provides a differential clock with adjustable amplitude, offset and termination. No phase alignment to data output. It provides the signal with the frequency range from 31.25 MHz to 16.2499 GHz.
- **Ch Clk Out 1** - This port provides the clock signal for the pattern generator M8042A and AWG modules. Ch Clk Out 1 has to be connected to Ch Clk In 1 of the M8042A module.
- **Ch Clk Out 2** - This port can be switched between the Channel clock mode or Forwarded clock mode.
- **Sync In** - This port is reserved for future use.
- **Sync Out A/B/C** - This port is used to sync with M8042A module only.
- **Sys Trig In A/B** - This port is reserved for future use.
- **Ref Clk In** - This port allows locking the system clock to an external reference clock of 10 or 100 MHz instead of the internal oscillator.
- **Ref Clk Out** - This port provides a reference clock to lock with other instruments in the test setup. It provides clock frequency 10 MHz or 100 MHz.
- **Ref Clk Out 16G** - This port provides a clock between 8 and 16 GHz, relative to symbol rate. It can be used as clock input or as trigger input for a precision time base of a DCA. Clean clock only.

M8043A Module

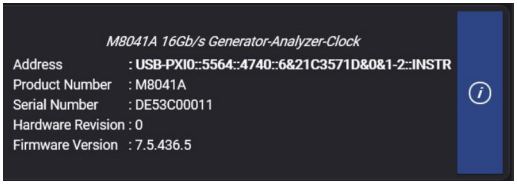
The M8043A module has the following ports on its front panel:

- **Remote Head** - This port provides data input and control signals for M8052A remote head.
- **Cal** - This calibration output is used for factory calibration at Keysight facilities.
- **Link** - This communication link is for future use.
- **Clk In** - This port enables source-synchronous operation, allowing effective analysis of data with Spread Spectrum Clocking (SSC).
- **Ctrl In** - This port provide functionality that can be selected as: sequence trigger, pattern capture event.
- **Ctrl Out** - This port outputs a pulse in case of an error. It generates a pulse or static high/low if used from sequencer.

Show Module Information

You can get the module information that is connected to

the M8020A/M8040A/M8050A by clicking the icon present at the right side of each module. The module information will be shown as depicted in the following figure:



It provides the following information about the module:

- **Address** - Address of module, e.g. USB-PXIO::11::0::INSTR
- **Product Number** - Product no. of the module, e.g. M8041A
- **Serial Number** - Serial no. of module, e.g. DE53C00061
- **Hardware Revision** - Hardware revision of module, e.g. 0

Selecting Single/Multiple Ports

You can select either single or multiple ports by pressing the toggle button, available on the top of the main window. It provides the following modes selection:

Single Selection Mode - allows you to select only one port at a time from the connected modules.

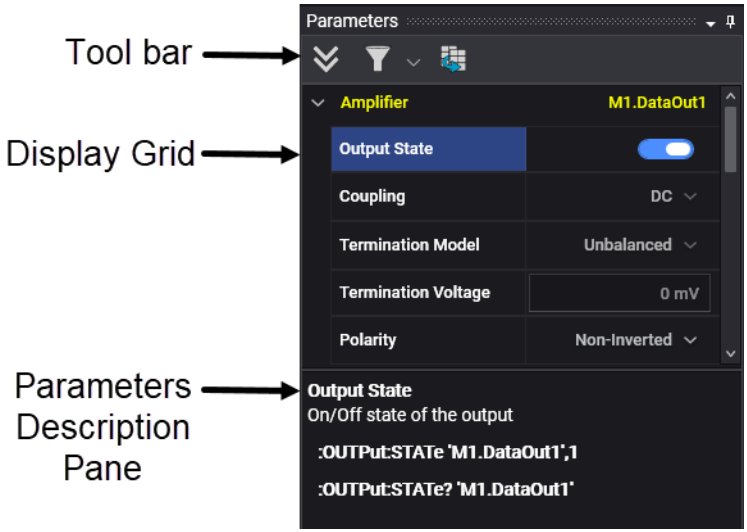
Multiple Selection Mode - allows you to select multiple ports from the connected modules.

Parameters Window

The **Parameters** window displays the functional blocks of the selected port/port groups. Each functional block has a set of parameters. The **Parameters** window also allows you to set the parameters of the selected port/port groups.

If you try to set a parameter which conflicts with other parameter or in other words is dependent on other parameter, a **Auto Correct Confirmation** dialog appears. For details, see Auto Correction Confirmation Dialog on page 193.

The **Parameters** window is shown in the following figure:



The **Parameters** window has the following sections:

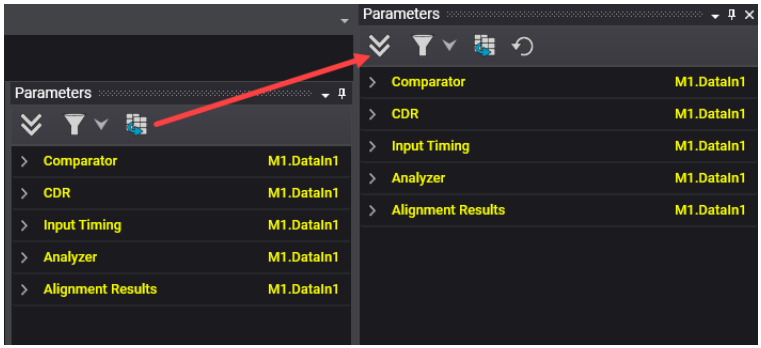
- Tool bar
- Display Grid
- Parameters Description Pane

The **Parameters** window tool bar includes the following icons:

- Expand/Collapse All Group: Click this icon to expand or collapse the functional blocks.

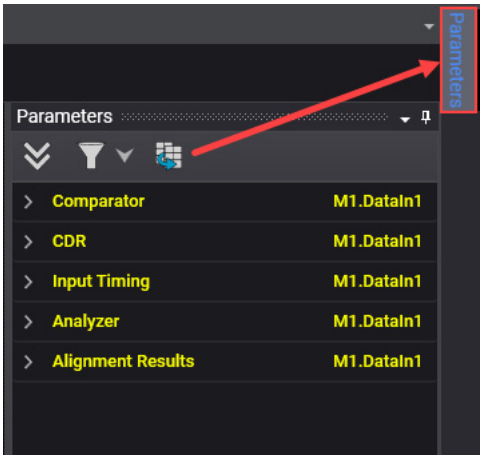
- Show Search Option: Allows you to filter and customize your results by using the following options:
  - By Location
  - By Functional Block
  - By Property

- Copying Parameter Window: Creates a replica of **Parameters** window to enhance the usability. It allows you to work on two different instances of the application. The changes you make in one window display immediately in the other window. The icon present on the copied parameter window loads all properties of the module. The following figure shows the copied **Parameters** window.



Once copied and then enabling the auto hide feature, the copied parameters window is docked to the right edge of the main user interface. The copied parameters window pops up once you click on it.

The following figure shows the copied parameters window docked to the right edge of the main user interface.



- **Display Grid**: Displays the parameters of the selected port/port groups within a grid. The left column contains the parameter names; the right column contains the parameter values.

  In addition, it also allows you to set the parameters of the selected port/port groups.

  The naming convention used for the port/port group is explained with the help of following example:

  M1.DataIn1

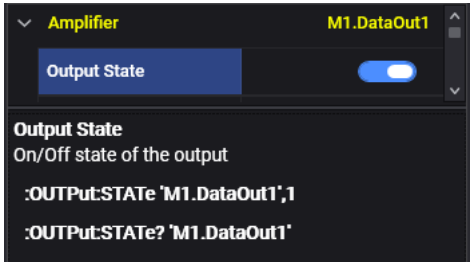
  Where,

  - M1 stands for Module1
  - DataIn stands for DataIn port
  - 1 for channel 1

  The functional blocks use the different color schemes to represent different channels. You can set the color schemes of each channel from the Setting window. For details, refer to Preferences Window on page 800.

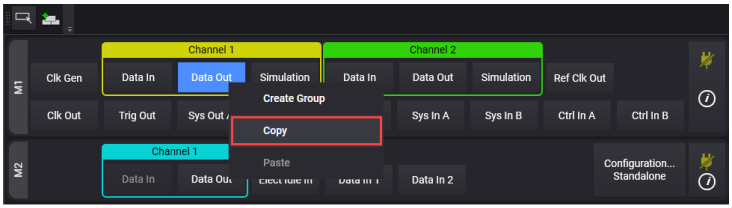
- **Parameter Description Pane**: Provides the description and related SCPI of the currently selected parameter.

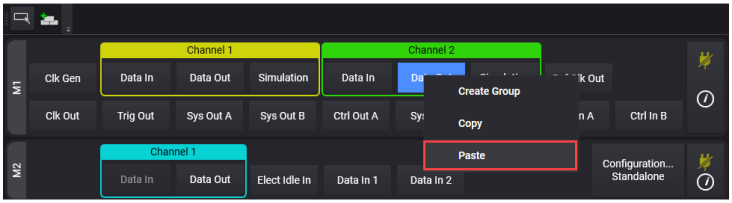
  The following figure shows the **Parameter Description Pane** providing the description and the related SCPI when the line coding parameter is selected.



- **Copy-Paste Parameters Settings**: The **Parameter Window** allows you to copy all parameter's settings of one location to the another similar location within the same module. This helps to keeps the similar parameter settings for same locations across different channels.
  For example, if you want to the copy the parameter's setting of DataOut of channel 1 to DataOut of channel 2, just right-click on DataOut of channel 1 and select **Copy** and then right-click on DataOut of channel 2 and select **Paste**.

  The following figure illustrates how copy-paste of one location to another similar location within a module is done:

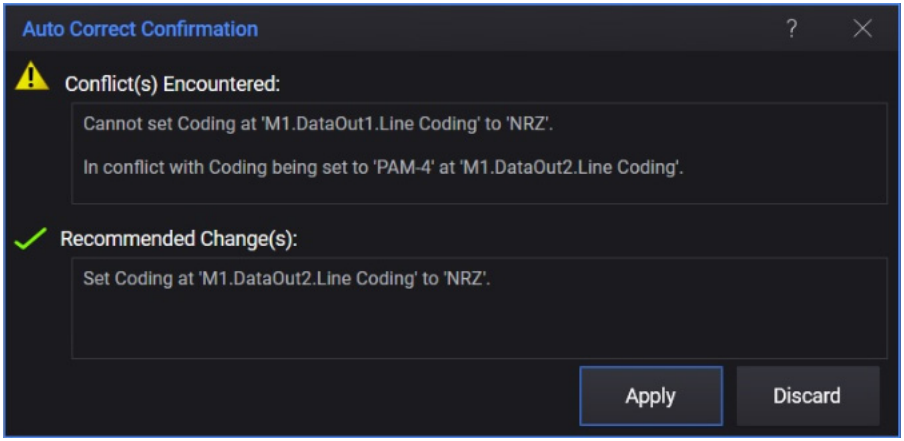




Auto Correction Confirmation Dialog

There are several parameters in the M8070B GUI which are interdependent on the settings of other parameters. For details of these parameters, refer to Table 49 on page -194 and Table 50 on page -201.

An **Auto Correct Confirmation** dialog appears if you try to set a parameter which conflicts with other parameter or in other words is dependent on the settings of other parameter. This dialog display the conflicts encountered and also provides the recommended setting to overcome those conflicts. If you click **Apply** button, the recommended settings will be applied on the M8070B GUI. However, if you click **Discard** button, the previous settings will be applied. The following figure shows an **Auto Correct Confirmation** dialog which is displayed when a user tries to set a ClkGen frequency and it conflicts with ClkOut Output Timing Divider.



Dependent Parameters

There are several parameters in the M8070B GUI which are interdependent on the settings of other parameters. Refer to Table 49 on page -194 and Table 50 on page -201 for details of these parameters. For details on the related/dependent SCPIs of these parameters, please refer to *M8000 Series Programing Guide*.

Table 49 M8020A Dependent Parameters

Functional block / Parameter	Identifier Location	Dependent Parameters	Description	Related /Dependent SCPI
Amplifier	M1.DataOut1	Amplitude	Depends on termination voltage, CMI and DMI amplitudes	":SOURce:VOLTage:AMPLitude :OUTPut:TVOLtage :SOURce:INTerference:LEVel:CMODe:AMPLitude :SOURce:INTerference:LEVel:DMODe:AMPLitude"
		High	Depends on amplitude and offset value	":SOURce:VOLTage:HIGH :SOURce:VOLTage:AMPLitude :SOURce:VOLTage:OFFSet"
		Low	Depends on amplitude and offset value	":SOURce:VOLTage:LOW :SOURce:VOLTage:AMPLitude :SOURce:VOLTage:OFFSet"
		Offset	Depends on termination voltage	":SOURce:VOLTage:OFFSet :OUTPut:TVOLtage "
		Amplitude Range (if Auto-range enabled)	DataOut maximum amplitude will become limited to the selected amplitude range value	":SOURce:VOLTage:AMPLitude :SOURce:VOLTage:RANGe:AUTO :SOURce:VOLTage:RANGe:SELect :OUTPut:STATe"
		Coupling	Selecting incorrect coupling enables output protection, and as a result DataOut state could not be enabled	":OUTPut:STATe :OUTPut:COUPling"
		Termination Model	Only available when coupling is selected as DC	":OUTPut:COUPling :OUTPut:TCONfig"
		Termination Voltage	Available only if coupling is selected as DC and termination model is selected as unbalanced	":OUTPut:COUPling :OUTPut:TCONfig :OUTPut:TVOLtage"
		CMI State	CMI value depends only if CMI state is enabled	":SOURce:INTerference:LEVel:CMODe:STATe :SOURce:INTerference:LEVel:CMODe:AMPLitude"
		CMI Amplitude	DataOut maximum amplitude will b limited to 900mV if CMI state is enabled	":SOURce:VOLTage:AMPLitude :SOURce:INTerference:LEVel:CMODe:STATe :SOURce:INTerference:LEVel:CMODe:AMPLitude :OUTPut:STATe"
		DMI State	Depends on DataOut Amplitude maximum value	":SOURce:INTerference:LEVel:DMODe:STATe :SOURce:INTerference:LEVel:DMODe:AMPLitude"

Functional block / Parameter	Identifier Location	Dependent Parameters	Description	Related /Dependent SCPI
		DMI Amplitude	On applying DMI amplitude as max (360mV) then maximum value of DataOut1 Amplitude will become 840mV	":SOURce:VOLTage:AMPLitude :SOURce:INTerference:LEVel:DMODe:STATe :SOURce:INTerference:LEVel:DMODe:AMPLitude :OUTPut:STATe"
LF Jitter	M1.DataOut1	PJ State	Value doesn't applicable if state is Off	:SOURce:JITTer:LFRequency:PERiodic:STATe
		PJ Amplitude	PJ amplitude depends on PJ frequency, rSSC amplitude, rSSC state and rSSC frequency	":SOURce:JITTer:LFRequency:PERiodic:STATe :SOURce:JITTer:LFRequency:PERiodic:AMPLitude :SOURce:JITTer:LFRequency:PERiodic:FREQuency :SOURce:JITTer:LFRequency:RSSClocking:STATe :SOURce:JITTer:LFRequency:RSSClocking:AMPLitud e: SOURce:JITTer:LFRequency:RSSClocking:FREQuenc y"
		PJ Frequency	PJ frequency depends on PJ amplitude, rSSC amplitude, rSSC state and rSSC frequency	":SOURce:JITTer:LFRequency:PERiodic:STATe :SOURce:JITTer:LFRequency:PERiodic:AMPLitude :SOURce:JITTer:LFRequency:PERiodic:FREQuency :SOURce:JITTer:LFRequency:RSSClocking:STATe :SOURce:JITTer:LFRequency:RSSClocking:AMPLitud e :SOURce:JITTer:LFRequency:RSSClocking:FREQuen cy"
		rSSC State	Value doesn't applicable if state is Off	:SOURce:JITTer:LFRequency:RSSClocking:STATe
		rSSC Amplitude	rSSC amplitude depends on rSSC frequency, PJ amplitude, PJ state and PJ frequency	":SOURce:JITTer:LFRequency:PERiodic:STATe :SOURce:JITTer:LFRequency:PERiodic:AMPLitude :SOURce:JITTer:LFRequency:PERiodic:FREQuency :SOURce:JITTer:LFRequency:RSSClocking:STATe :SOURce:JITTer:LFRequency:RSSClocking:AMPLitud e :SOURce:JITTer:LFRequency:RSSClocking:FREQuen cy"
		rSSC Frequency	rSSC frequency depends on rSSC amplitude, PJ amplitude, PJ state and PJ frequency	":SOURce:JITTer:LFRequency:PERiodic:STATe :SOURce:JITTer:LFRequency:PERiodic:AMPLitude :SOURce:JITTer:LFRequency:PERiodic:FREQuency :SOURce:JITTer:LFRequency:RSSClocking:STATe :SOURce:JITTer:LFRequency:RSSClocking:AMPLitud e :SOURce:JITTer:LFRequency:RSSClocking:FREQuen cy"

Functional block / Parameter	Identifier Location	Dependent Parameters	Description	Related /Dependent SCPI
		Unit	If unit is selected as 'sec', the jitter amplitude min/max values also depends on Data rate (synthesizer frequency)	":SOURce:JITTer:LFRequency:UNIT :SOURce:FREQuency"
		Data rate (Synthesizer frequency)	If unit is selected as 'sec', the jitter amplitude min/ max values also depends on Data rate (synthesizer frequency)	":SOURce:JITTer:LFRequency:UNIT :SOURce:FREQuency"
HF Jitter	M1.DataOut1	PJ1 State	Value doesn't applicable if state is Off	:SOURce:JITTer:HFRequency:PERiodic1:STATe
		PJ1 Amplitude	"Depends on PJ2 amplitude, BUJ amplitude, RJ amplitude, sRJ amp1 and sRJ amp2 (User can choose either sRJ Or combination of BUJ and RJ)"	":SOURce:JITTer:HFRequency:PERiodic2:AMPLitude :SOURce:JITTer:HFRequency:BUNCorrelate:AMPLitude :SOURce:JITTer:HFRequency:RANDom:AMPLitude :SOURce:JITTer:HFRequency:SPECtrally:AMPLitude1 :SOURce:JITTer:HFRequency:SPECtrally:AMPLitude2 "
		PJ2 State	Value doesn't applicable if state is Off	:SOURce:JITTer:HFRequency:PERiodic2:STATe
		PJ2 Amplitude	"Depends on PJ1 amplitude, BUJ amplitude, RJ amplitude, sRJ amp1 and sRJ amp2 (User can choose either sRJ Or combination of BUJ and RJ)"	":SOURce:JITTer:HFRequency:PERiodic1:AMPLitude :SOURce:JITTer:HFRequency:BUNCorrelate:AMPLitude :SOURce:JITTer:HFRequency:RANDom:AMPLitude :SOURce:JITTer:HFRequency:SPECtrally:AMPLitude1 :SOURce:JITTer:HFRequency:SPECtrally:AMPLitude2 "
		BUJ State	"Value doesn't applicable if state is Off Also depends on sRJ state"	":SOURce:JITTer:HFRequency:BUNCorrelate:STATe :SOURce:JITTer:HFRequency:SPECtrally:STATe"
		BUJ Amplitude	Depends on PJ1 amplitude, PJ2 amplitude, RJ amplitude, sRJ amp1 and sRJ amp2	":SOURce:JITTer:HFRequency:PERiodic1:AMPLitude :SOURce:JITTer:HFRequency:PERiodic2:AMPLitude :SOURce:JITTer:HFRequency:RANDom:AMPLitude :SOURce:JITTer:HFRequency:SPECtrally:AMPLitude1 :SOURce:JITTer:HFRequency:SPECtrally:AMPLitude2 "
		RJ State	"Value doesn't applicable if state is Off Also depends on sRJ state"	":SOURce:JITTer:HFRequency:RANDom:STATe :SOURce:JITTer:HFRequency:SPECtrally:STATe"

Functional block / Parameter	Identifier Location	Dependent Parameters	Description	Related /Dependent SCPI
		RJ Amplitude	Depends on PJ1 amplitude, PJ2 amplitude, BUJ amplitude, sRJ amp1 and sRJ amp2	":SOURce:JITTer:HFRequency:PERiodic1:AMPLitude :SOURce:JITTer:HFRequency:PERiodic2:AMPLitude :SOURce:JITTer:HFRequency:BUNCorrelate:AMPLitude :SOURce:JITTer:HFRequency:SPECtrally:AMPLitude1 :SOURce:JITTer:HFRequency:SPECtrally:AMPLitude2 "
		sRJ State	"Value doesn't applicable if state is Off Also depends on RJ and BUJ state"	":SOURce:JITTer:HFRequency:SPECtrally:STATe :SOURce:JITTer:HFRequency:RANDom:STATe :SOURce:JITTer:HFRequency:BUNCorrelate:STATe"
		sRJ Amplitude 1(RMS) LF	Depends on PJ1 amplitude, PJ2 amplitude, BUJ amplitude, RJ amp and sRJ amp2	":SOURce:JITTer:HFRequency:PERiodic1:AMPLitude :SOURce:JITTer:HFRequency:PERiodic2:AMPLitude :SOURce:JITTer:HFRequency:BUNCorrelate:AMPLitude :SOURce:JITTer:HFRequency:RANDom:AMPLitude :SOURce:JITTer:HFRequency:SPECtrally:AMPLitude2 "
		sRJ Amplitude 2(RMS) HF	Depends on PJ1 amplitude, PJ2 amplitude, BUJ amplitude, RJ amp and sRJ amp1	":SOURce:JITTer:HFRequency:PERiodic1:AMPLitude :SOURce:JITTer:HFRequency:PERiodic2:AMPLitude :SOURce:JITTer:HFRequency:BUNCorrelate:AMPLitude :SOURce:JITTer:HFRequency:RANDom:AMPLitude :SOURce:JITTer:HFRequency:SPECtrally:AMPLitude1 "
sRJ State	M1.DataOut1	BUJ State (Data Out)	If sRJ is ON, then BUJ state cannot be enabled	":SOURce:JITTer:HFRequency:SPECtrally:STATe :SOURce:JITTer:HFRequency:BUNCorrelate:STATe"
		RJ State (Data Out)	If sRJ is ON, then RJ state cannot be enabled	":SOURce:JITTer:HFRequency:SPECtrally:STATe :SOURce:JITTer:HFRequency:RANDom:STATe"
		BUJ State (Clock Out)	If sRJ is ON, then BUJ state cannot be enabled	":SOURce:JITTer:HFRequency:SPECtrally:STATe :SOURce:JITTer:HFRequency:BUNCorrelate:STATe"
		RJ State (Clock Out)	If sRJ is ON, then RJ state cannot be enabled	":SOURce:JITTer:HFRequency:SPECtrally:STATe :SOURce:JITTer:HFRequency:RANDom:STATe"
BUJ State	M1.DataOut1	sRJ State (Data Out)	If BUJ state is ON, then DataOut sRJ cannot be enabled	":SOURce:JITTer:HFRequency:SPECtrally:STATe :SOURce:JITTer:HFRequency:BUNCorrelate:STATe"
		sRJ State (Clock Out)	If BUJ state is ON, then ClockOut sRJ cannot be enabled	":SOURce:JITTer:HFRequency:SPECtrally:STATe :SOURce:JITTer:HFRequency:BUNCorrelate:STATe"
RJ State	M1.DataOut1	sRJ State (Data Out)	If RJ state is ON, then DataOut sRJ cannot be enabled	":SOURce:JITTer:HFRequency:RANDom:STATe :SOURce:JITTer:HFRequency:SPECtrally:STATe"

Functional block / Parameter	Identifier Location	Dependent Parameters	Description	Related /Dependent SCPI
		sRJ State (Data Out)	If RJ state is ON, then ClockOut sRJ cannot be enabled	":SOURce:JITTer:HFRequency:RANDom:STATe :SOURce:JITTer:HFRequency:SPECtrally:STATe"
sRJ State	M1.DataOut1	RJ State (Data Out)	If sRJ state is ON, then DataOut RJ cannot be enabled	":SOURce:JITTer:HFRequency:SPECtrally:STATe :SOURce:JITTer:HFRequency:RANDom:STATe"
		BUJ State (Data Out)	If sRJ state is ON, then DataOut BUJ cannot be enabled	":SOURce:JITTer:HFRequency:SPECtrally:STATe :SOURce:JITTer:HFRequency:BUNCorrelate:STATe"
		RJ State (Clock Out)	If sRJ state is ON, then ClockOut RJ cannot be enabled	":SOURce:JITTer:HFRequency:SPECtrally:STATe :SOURce:JITTer:HFRequency:RANDom:STATe"
		BUJ State (Clock Out)	If sRJ state is ON, then ClockOut BUJ cannot be enabled	":SOURce:JITTer:HFRequency:SPECtrally:STATe :SOURce:JITTer:HFRequency:BUNCorrelate:STATe"
RJ Low Pass Filter as 1000 MHz	M1.DataOut1	Depends on Data Rate (Synthesizer frequency)	Can only be selected is Data Rate is above 7.5 GHz	":SOURce:JITTer:HFRequency:RANDom:STATe :SOURce:FREQuency :SOURce:JITTer:HFRequency:RANDom:FILTer:LPASs"
Jitter Sweep State	M1.DataOut1	RJ State (Data Out)	If Jitter Sweep state is ON, then DataOut RJ cannot be enabled	":SOURce:JITTer:SWEep:STATe :SOURce:JITTer:HFRequency:RANDom:STATe"
		PJ2 State (Data Out)	If Jitter Sweep state is ON, then DataOut PJ2 cannot be enabled	":SOURce:JITTer:SWEep:STATe :SOURce:JITTer:HFRequency:PERiodic2:STATe"
		PJ2 State (Clock Out)	If Jitter Sweep state is ON, then ClockOut PJ2 cannot be enabled	":SOURce:JITTer:SWEep:STATe :SOURce:JITTer:HFRequency:PERiodic2:STATe"
Jitter Sweep Amplitude, start and stop frequency	M1.DataOut1	Jitter sweep mode	User programmable only If Mode is selected as Constant amplitude	":SOURce:JITTer:SWEep:STATe :SOURce:JITTer:SWEep:AMPLitude:MODE :SOURce:JITTer:SWEep:AMPLitude:VALue :SOURce:JITTer:SWEep:FREQuency:STARt :SOURce:JITTer:SWEep:FREQuency:STOP"
Jitter Sweep profile, Step distance	M1.DataOut1	Jitter sweep mode	User programmable only If Mode is selected as Variable amplitude	":SOURce:JITTer:SWEep:STATe :SOURce:JITTer:SWEep:AMPLitude:MODE :SOURce:JITTer:SWEep:STEP:DISTance :SOURce:JITTer:SWEep:DATA:FILE"
Jitter Sweep Step Distance	M1.DataOut1	Jitter sweep mode	Jitter sweep step distance parameter is re-programmable only if Mode is selected as Variable amplitude	":SOURce:JITTer:SWEep:STATe :SOURce:JITTer:SWEep:AMPLitude:MODE :SOURce:JITTer:SWEep:STEP:DISTance"

Functional block / Parameter	Identifier Location	Dependent Parameters	Description	Related /Dependent SCPI
CMI Amplitude	M1.DataOut1	CMI State	Value doesn't applicable if state is Off	":SOURce:VOLTage:AMPLitude :SOURce:INTerference:LEVel:CMODe:STATe :SOURce:INTerference:LEVel:CMODe:AMPLitude"
		Amplifier Amplitude	The max value of CMI amplitude depends on amplifier amplitude	":SOURce:VOLTage:AMPLitude :SOURce:INTerference:LEVel:CMODe:STATe :SOURce:INTerference:LEVel:CMODe:AMPLitude"
		Amplifier Offset	Depends on DataOut amplifier offset, high and low values	":SOURce:VOLTage:AMPLitude :SOURce:INTerference:LEVel:CMODe:STATe :SOURce:INTerference:LEVel:CMODe:AMPLitude :SOURce:VOLTage:LOW :SOURce:VOLTage:HIGH :SOURce:VOLTage:OFFSet"
DMI Amplitude	M1.DataOut1	DMI State	Value doesn't applicable if state is Off	":SOURce:VOLTage:AMPLitude :SOURce:INTerference:LEVel:DMODe:STATe :SOURce:INTerference:LEVel:DMODe:AMPLitude"
		Amplifier Amplitude	The max value of DMI amplitude depends on amplifier amplitude	":SOURce:VOLTage:AMPLitude :SOURce:INTerference:LEVel:DMODe:STATe :SOURce:INTerference:LEVel:DMODe:AMPLitude"
		Amplifier Offset	Depends on DataOut amplifier offset, high and low values	":SOURce:VOLTage:AMPLitude :SOURce:INTerference:LEVel:DMODe:STATe :SOURce:INTerference:LEVel:DMODe:AMPLitude :SOURce:VOLTage:LOW :SOURce:VOLTage:HIGH :SOURce:VOLTage:OFFSet"
Error Insertion Ratio	M1.DataOut1	Error Insertion Mode	Error ratio of 1E-1 or 1E-2 are selectable only if error insertion mode is selected as Variable spacing	":OUTPut:EINSertion:MODE :OUTPut:EINSertion:RATio"
Inter-Symbol Interference Mode	M1.DataOut1	Depends on selected Preset value	ISI mode as Two-Point only available when Preset is selected as Custom	":SOURce:INTerference:ISYMbol:MODE :SOURce:INTerference:ISYMbol:PRESet"
Deemphasis Preset Register Number	M1.DataOut1	State of Preset Enable button	Re-programmable only if state of Preset Enable button is ON	":OUTPut:DEEMphasis:PRESet:ENABle :OUTPut:DEEMphasis:PRESet"
Bit Recovery Mode State	M1.DataIn1	Depends on CDR State	BRM mode can only be enabled if CDR state is ON	":INPut:CDR:JTF:STATe :INPut:DATA:BRMode"

Functional block / Parameter	Identifier Location	Dependent Parameters	Description	Related /Dependent SCPI
CDR State	M1.DataIn1	Depends on CDR Control type	If CDR control type is Sequence controlled, then CDR state will be controlled by Analyzer sequence block settings	:INPut:CDR:CTRL
CDR Loop Bandwidth	M1.DataIn1	Depends on Data Rate	Maximum value of CDR loop bandwidth depends on Data rate (Synthesizer frequency)	":INPut:CDR:JTF:STATe :SOURce:FREQuency"
		Depends on Loop Order	Depends on type of the selected loop order	":INPut:CDR:JTF:STATe :INPut:CDR:JTF:LORDer"
		Depends on Peaking	Peaking and Loop bandwidth are interdependent	":INPut:CDR:JTF:LORDer :INPut:CDR:JTF:SECond:PEAKing"
Comparator Compare Mode	M1.DataIn1	Depends on Termination Configuration	Available only if Termination configuration is selected as Unbalanced	:INPut:TCONfig
Termination Voltage	M1.DataIn1	Depends on Termination Configuration	Available only if Termination configuration is selected as Unbalanced	":INPut:TCONfig :INPut:TVOLtage :INPut:CMODe"
SSC Profile Shape	M1.ClkGen	Depends on SSC Profile	Available only if SSC profile is selected as Arbitrary	":SOURce:SSCLocking:STATe :SOURce:SSCLocking:PROFile :SOURce:SSCLocking:SHAPe"

Table 50 M8040A Dependent Parameters

Functional block / Parameter	Identifier Location	Dependent Parameters	Description	Related /Dependent SCP
Clock Gen Frequency	M1.ClkGen	M8046A Clock source	Depends on termination voltage, CMI and DMI amplitudes	":SOURce:VOLTage:AMPLitude :OUTPut:TVOLtage :SOURce:INTerference:LEVel:CMODe:AMPLitude :SOURce:INTerference:LEVel:DMODe:AMPLitude"
		M8046A Follow Sys Clock Option	Depends on amplitude and offset value	":SOURce:VOLTage:HIGH :SOURce:VOLTage:AMPLitude :SOURce:VOLTage:OFFSet"
		M1.ClkOut State	Depends on amplitude and offset value	":SOURce:VOLTage:LOW :SOURce:VOLTage:AMPLitude :SOURce:VOLTage:OFFSet"
		M1.ClkOut Divider	Depends on termination voltage	":SOURce:VOLTage:OFFSet :OUTPut:TVOLtage "
Amplifier	M1.DataOut1	Amplitude	Depends on termination voltage and synthesizer frequency	":SOURce:VOLTage:AMPLitude :OUTPut:TVOLtage :SOURce:FREQuency"
		High	Depends on amplitude and offset	":SOURce:VOLTage:HIGH :SOURce:VOLTage:AMPLitude :SOURce:VOLTage:OFFSet"
		Low	Depends on amplitude and offset	":SOURce:VOLTage:LOW :SOURce:VOLTage:AMPLitude :SOURce:VOLTage:OFFSet"
		Offset	Depends on termination voltage	":SOURce:VOLTage:OFFSet :OUTPut:TVOLtage"
		Coupling	Selecting incorrect coupling enables output protection, and as a result DataOut state could not be enabled	":OUTPut:STATe :OUTPut:COUPling"
		Termination Model	Only available when coupling is selected as DC	":OUTPut:COUPling :OUTPut:TCONfig"
		Termination Voltage	Available only if coupling is selected as DC to termination model is selected as unbalanced	":OUTPut:COUPling :OUTPut:TCONfig :OUTPut:TVOLtage"

Functional block / Parameter	Identifier Location	Dependent Parameters	Description	Related /Dependent SCP
		Clock Gen Frequency	Maximum amplitude will be 900mV if synthesizer frequency is below 32.414GHz, but if synthesizer frequency is above 32.414GHz, then maximum amplitude will be 600mV	":SOURce:VOLTage:AMPLitude :SOURce:FREQuency"
Deemphasis Co-efficient 2	M1.DataOut1	Automatic main cursor state	Re-programmable only if Automatic main cursor state is disabled	":OUTPut:DEEMphasis:CURSor:MAIN:AUTO :OUTPut:DEEMphasis:CURSor:MAGNitude2"
Deemphasis Co-efficients	M1.DataOut1	Depends on Coefficient 0, 1 and 3 state	Deemphasis coefficient values are interdependent and sum of all the cursors cannot be more than 1.0	":OUTPut:DEEMphasis:CURSor:MAIN:AUTO :OUTPut:DEEMphasis:CURSor:MAGNitude0 :OUTPut:DEEMphasis:CURSor:MAGNitude1 :OUTPut:DEEMphasis:CURSor:MAGNitude2 :OUTPut:DEEMphasis:CURSor:MAGNitude3"
LF Jitter	M1.DataOut1	PJ State	Value doesn't applicable if state is Off	:SOURce:JITTer:LFRequency:PERiodic:STATe
		PJ Amplitude	PJ Amplitude depends on PJ frequency	":SOURce:JITTer:LFRequency:PERiodic:STATe :SOURce:JITTer:LFRequency:PERiodic:AMPLitude :SOURce:JITTer:LFRequency:PERiodic:FREQuency"
		PJ Frequency	PJ frequency depends on PJ amplitude	":SOURce:JITTer:LFRequency:PERiodic:STATe :SOURce:JITTer:LFRequency:PERiodic:AMPLitude :SOURce:JITTer:LFRequency:PERiodic:FREQuency"
		Unit	If unit is selected as sec, then amplitude min/max values will be expressed in sec	":SOURce:JITTer:LFRequency:UNIT :SOURce:FREQuency"
HF Jitter	M1.DataOut1	PJ1 State	Value doesn't applicable if state is Off	:SOURce:JITTer:HFRequency:PERiodic1:STATe
		PJ1 Amplitude	Depends on PJ2 amplitude, BUJ amplitude and RJ amplitude	":SOURce:JITTer:HFRequency:PERiodic2:AMPLitude :SOURce:JITTer:HFRequency:BUNCorrelate:AMPLitude :SOURce:JITTer:HFRequency:RANDom:AMPLitude"
		PJ2 State	Value doesn't applicable if state is Off	:SOURce:JITTer:HFRequency:PERiodic2:STATe
		PJ2 Amplitude	Depends on PJ1 amplitude, BUJ amplitude and RJ amplitude	":SOURce:JITTer:HFRequency:PERiodic1:AMPLitude :SOURce:JITTer:HFRequency:BUNCorrelate:AMPLitude :SOURce:JITTer:HFRequency:RANDom:AMPLitude"

Functional block / Parameter	Identifier Location	Dependent Parameters	Description	Related /Dependent SCP
		BUJ State	Value doesn't applicable if state is Off	:SOURce:JITTer:HFRequency:BUNCorrelate:STATe
		BUJ Amplitude	Depends on PJ1 amplitude, PJ2 amplitude and RJ amplitude	":SOURce:JITTer:HFRequency:PERiodic1:AMPLitude :SOURce:JITTer:HFRequency:PERiodic2:AMPLitude :SOURce:JITTer:HFRequency:RANDom:AMPLitude"
		RJ State	Value doesn't applicable if state is Off	:SOURce:JITTer:HFRequency:RANDom:STATe
		RJ Amplitude	Depends on PJ1 amplitude, PJ2 amplitude and BUJ amplitude	":SOURce:JITTer:HFRequency:PERiodic1:AMPLitude :SOURce:JITTer:HFRequency:PERiodic2:AMPLitude :SOURce:JITTer:HFRequency:BUNCorrelate:AMPLitude"
Error Insertion Ratio	M1.DataOut1	Error Insertion Mode	Error ratio of 1E-1 or 1E-2 are selectable only if error insertion mode is selected as Variable spacing	":OUTPut:EINSertion:MODE :OUTPut:EINSertion:RATio"
N8046A Clock	M2.DataIn	Clock Source	Some parameters only available if clock source is selected as CLK IN	:CLOCk:SOURce
		Follow Sys Clock	Follow Sys Clk option only available if clock source is selected as CLK IN	":CLOCk:SOURce :CLOCk:TRACk:STATe"
		Clk In Multiplier	Clk In multiplier value depends on Data rate and available only if clock source is selected as CLK IN	":CLOCk:SOURce :CLOCk:FREQuency:MULTiplier"
Clock Source as External Clock Recovery	M2.DataIn	Clock Source	Available only if FlexDCA is configured for M8070B and N1076A module is connected with the system running M8070B	:CLOCk:SOURce
Symbol Mapping as Grey, Custom and Uncoded	M2.DataIn/ M1.DataOut1	Line Coding	Available only if Line coding is selected as PAM4	":DATA:LINecoding:VALue :DATA:LINecoding:PAM4:MAPPing :DATA:LINecoding:PAM4:SYMBol:LEVel1 :DATA:LINecoding:PAM4:SYMBol:LEVel2"
Custom Symbol Mapping	M2.DataIn/ M1.DataOut1	Line Coding	Available only if Line coding is selected as PAM4 and Symbol mapping is selected as Custom	":DATA:LINecoding:VALue :DATA:LINecoding:PAM4:MAPPing:CUSTom :DATA:LINecoding:PAM4:SYMBol:LEVel1 :DATA:LINecoding:PAM4:SYMBol:LEVel2"

Functional block / Parameter	Identifier Location	Dependent Parameters	Description	Related /Dependent SCP
Upper, Middle and Lower Thresholds	M2.DataIn	Depends on Line Coding	Available only if Line coding is selected as PAM4	":DATA:LINecoding:VALue :DATA:LINecoding:PAM4:MAPPing :INPut:VOLTage:PAM4:SYMBol:THReshold1|THReshold :INPut:VOLTage:PAM4:SYMBol:THReshold2 :INPut:VOLTage:PAM4:SYMBol:THReshold3"
Alignment results for Upper, Middle and Lower Eye Height	M2.DataIn	Depends on Line Coding	Available only if Line coding is selected as PAM4 (Only Query Command)	":DATA:LINecoding:VALue :INPut:ALIGnment:EYE:RESult:PAM4:HEIGht1|HEIGht? :INPut:ALIGnment:EYE:RESult:PAM4:HEIGht2? :INPut:ALIGnment:EYE:RESult:PAM4:HEIGht3?"
Alignment results for Upper, Middle and Lower Thresholds	M2.DataIn	Depends on Line Coding	Available only if Line coding is selected as PAM4	":DATA:LINecoding:VALue :INPut:ALIGnment:EYE:RESult:PAM4:THReshold1|THReshold? :INPut:ALIGnment:EYE:RESult:PAM4:THReshold2? :INPut:ALIGnment:EYE:RESult:PAM4:THReshold3?"
PRBS Polynomial as 2^7-1	Sequence Editor	Depends on Analyzer sequence	Not downloadable for Analyzer sequence for M8046A module	:DATA:SEQuence:VALue
Symbol Width other than 1 for M8045A and M8046A	Sequence Editor	M8045A and M8046A only support Symbol Width as 1	Symbol width other that 1 are not supported on M8040A modules	:DATA:SEQuence:VALue
Branch condition as Break for M8046A	Sequence Editor	Branch condition as Break is not supported for Analyzer sequence	Branch condition as Break is not supported for Analyzer sequence	:DATA:SEQuence:VALue
RJ Low Pass Filter as 1000 MHz	M1.DataOut1	Depends on Data Rate (Synthesizer frequency)	Can only be selected is Data Rate is above 7.5 GHz	":SOURce:JITTer:HFRequency:RANDom:STATe :SOURce:FREQuency :SOURce:JITTer:HFRequency:RANDom:FILTer:LPASs"

Non-Configurable Parameters

The Table 51 on page -205 lists the M8040A parameters which are non-configurable (read-only/gray out/disabled) by default or become non-configurable while configuring other dependent parameters.

Table 51 M8040A Non-Configurable Parameters

Functional block name	Parameters	Disabled parameters	Parameters that are non-configurable by default	Parameters that are non-configurable due to settings of other parameters
Clk Gen	Synthesizer (Select Source as Direct)	▪ Frequency ▪ Period	▪ In the Direct source mode, Frequency and Period will be in disabled state.	
	Synthesizer (Select Source as Clock Multiplier)	▪ Frequency ▪ Period	▪ In the Clock Multiplier mode, Frequency and Period will be in disabled state.	
	SSC	▪ Shape	▪ The SSC Shape parameters (Open, Import, Export and Reset to Default) are disabled by default. These parameters are enabled when SSC Profile is selected as Arbitrary.	
Data Out	Line Coding (Select PAM)	▪ Symbol 0 Level ▪ Symbol 3 Level	▪ In the PAM4 Line Coding, Symbol 0 Level and Symbol 3 Level are in disabled state by default.	
	Amplifier	▪ Termination Voltage ▪ Coupling ▪ Termination Model		▪ In the DC Unbalanced mode, all these three parameters become disabled on turning ON the output state.
	Amplifier	▪ Termination Voltage ▪ Coupling ▪ Termination Model		▪ In the DC Balanced mode, on turning ON the output state, Coupling and Termination Model are disabled and Termination Voltage is not available for user.
	Amplifier	▪ High ▪ Low ▪ Offset ▪ Termination Voltage ▪ Termination Model		▪ On selecting Coupling as AC==> High, Low and offset parameters are disabled. Also, Termination Voltage and Termination Model are unavailable in AC coupling.

Functional block name	Parameters	Disabled parameters	Parameters that are non-configurable by default	Parameters that are non-configurable due to settings of other parameters
	Deemphasis	▪ Coefficient 2 (Main) ▪ Output Swing ▪ Pre-cursor2 ▪ Pre-cursor1 ▪ Post-cursor1	▪ In the Deemphasis block, Coefficient 2 (Main), Output Swing, Pre-cursor2, Pre-cursor1, Post-Cursor1 are in disabled state by default. ▪ However, Coefficient 2 (Main) is enabled when the Automatic main cursor is turned off.	
	Output Timing	▪ Data Rate	▪ Data Rate in Output Timing is always in disabled state.	
	Error Insertion	▪ Insert Single Bit Error		▪ In Error Insertion block, when Mode is selected as Error Ratio (Fixed spacing) or Error Ratio (Variable Spacing), on Turning ON error ratio insertion state, "Insert Single Bit Error" will be unavailable.
	Error Insertion	▪ Error Ratio		▪ On selecting, Mode as Ctrl In A, Ctrl In B, Break, Sys In A, Sys In B Error Ratio will be disabled.
Clk Out of Channels	Output Timing	▪ Frequency	▪ Frequency is always in disabled state by default.	
Clock Out of M8045A	Amplifier	▪ Termination Voltage		▪ On selecting, Termination model as Balanced, Termination Voltage will be unavailable.
	Output Timing	▪ Frequency	▪ Frequency is always in disabled state by default.	
Trigger Out	Amplifier	▪ Termination Voltage		▪ On selecting, Termination model as Balanced, Termination Voltage will be unavailable.
	Configuration	▪ Subrate Frequency	▪ Whenever the Operating mode is Subrate clock, Subrate Frequency is in disabled state by default	
	Configuration	▪ Divider ▪ Subrate Frequency		▪ On selecting operating mode as Sequencer Controlled, Divider and Subrate frequency will be unavailable.

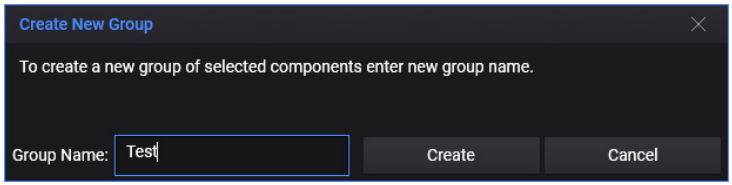
Functional block name	Parameters	Disabled parameters	Parameters that are non-configurable by default	Parameters that are non-configurable due to settings of other parameters
Data In	Clock (Select Source as Clk In and Follow Sys clk is Enabled)	▪ Symbol Rate ▪ Clk In Frequency	▪ Symbol Rate and Clock In Frequency are disabled.	
	Clock (Select Source as Clk In and Follow Sys clk is Disabled)	▪ Clk In Frequency		▪ On Turning Off the 'Follow Sys Clock', Clk In Frequency will become re-programmable.
	Clock (Select Source as Sys Clk)	▪ Follow Sys Clock ▪ Clk In Multiplier ▪ Clk In Frequency ▪ Symbol Rate	▪ Symbol Rate is in disabled state.	▪ On selecting source as "Sys Clk", Follow Sys Clk and Clk In Multiplier, Clk In Frequency will be unavailable.
	Line Coding - PAM4 (Select PAM4-Uncoded OR Gray Coded)	▪ Custom Symbol Mapping		▪ Custom Symbol Mapping is not available in PAM4 Uncoded and PAM4 Gray coded.
	Comparator	▪ Upper Threshold ▪ Middle Threshold ▪ Lower Threshold	▪ Upper Threshold, Middle Threshold and Lower Threshold will be available under comparator block in case of PAM4 coding only.	
	Input Timing	▪ Data Rate	▪ Data rate is always is disabled state.	
	Alignment Results	▪ All Parameters	▪ All Alignment results will be in disabled state. irrespective of the line coding (NRZ or PAM4).	

Creating Groups in the Module View

The **Module View** allows you to create a group of available ports and simultaneously allows you to configure their parameters.

To create a group:

- Switch to **Multiple Selection Mode** by pressing **Single Selection Mode** icon.
- From your keyboard, hold the Ctrl key and select the ports from the modules. You need to select at least two ports in order to create a group.
- Right-click on the selected ports and click **Create Group** option or alternatively you can select the ports and click **Create Group of Selection** icon. A **Create New Group** dialog will appear as shown in the following figure:



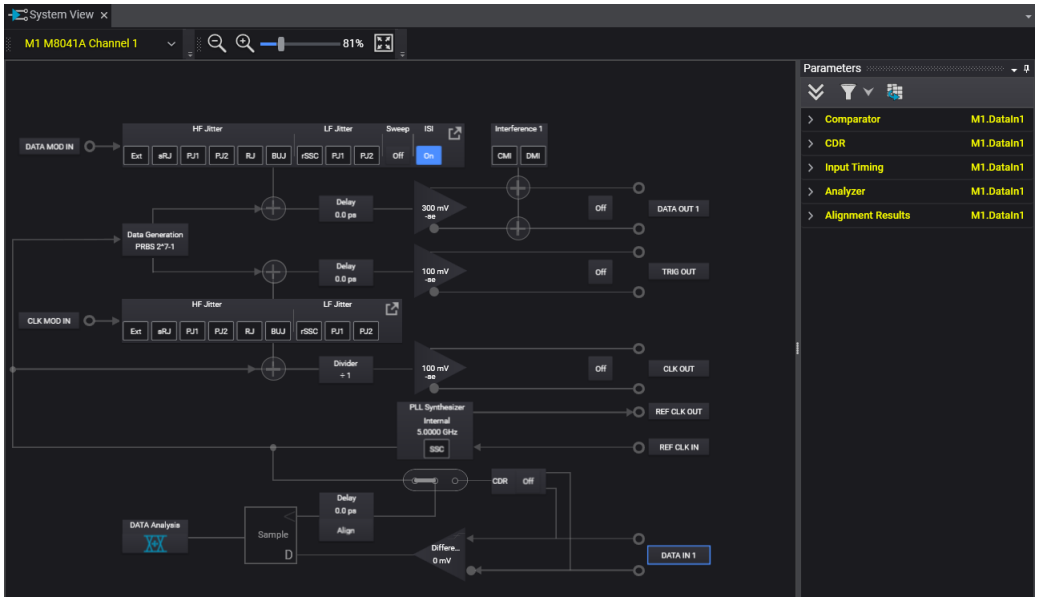
- Provide a group name and press **Create**.

A new group will be created in the **Group View**.

System View

The **System View** displays the block diagram representation of the currently selected channel of the M8020A/M8040A/M8050A.
In addition, it also allows you to interactively modify the settings for each channel.

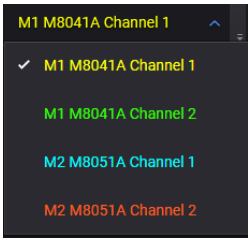
The **System View** user interface is shown in the following figure.



The principal parts are represented by blocks which are connected by lines/arrows to show the relationship of the blocks. These blocks are highlighted by the blue lines around block on mouse focus and the corresponding parameters are displayed in the **Parameters** window. The block may contain feature elements (for example, LF Jitter contain PJ and rSSC). You can click on the respective button to enable the feature elements. Once enabled, the feature elements are highlighted in blue color.

Channels

Displays the channels that are connected to the module. You can select the channel on which you want to configure channel settings. You can assign a different color to each channel so that they are easily identified. For details, refer to Preferences Window on page 800.



Using the Zoom Tool

The following figure shows the options provided by the zoom tool.

The zoom tools provide the following functionality:

- The **Zoom In** button allows you to enlarge the block diagram to view more details.
- The **Zoom Out** button allows you to reduce the block diagram.
- The **Zoom Slider** allows you to zoom in or zoom out the block diagram.

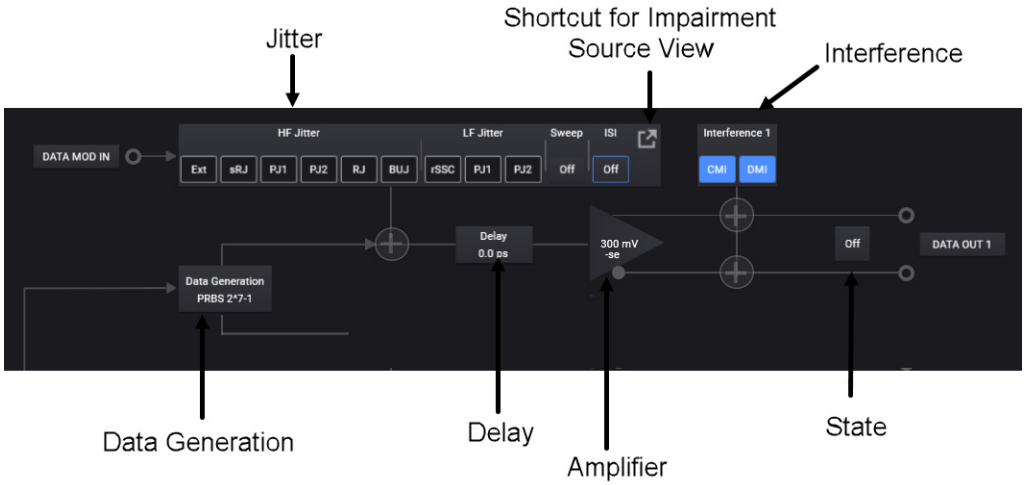
  The mouse wheel also provides a quick alternative to the zoom control. To zoom in and out using the mouse, hold down the [Ctrl] key while you turn the mouse wheel. Each click, up or down, increases or decreases the zoom factor by 25%.
- The **Fit to View** button fits the width of the block diagram so that the user does not have to scroll the block diagram to the right or to the left.

Understanding the System View

To understand the **System View**, let's divide it into the following sections:

Generator

The following section of the System View represents the generator function:



It allows you to apply settings on the Data Out port or location (data generator).

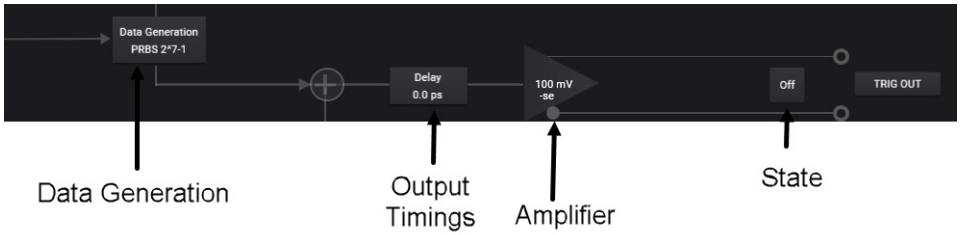
It includes the following blocks:

- State - Click on the Off button to enable the outputs of Data Out for the selected channel. Once the outputs are enabled, the button changes to “ON” On. If you press the button again, it will turn the state “OFF”.
- Jitter - Use this block to enable the jitter source of High Frequency Jitter, Low Frequency and Sweep. For more details on jitter, refer to Jitter Setup on page 428.
- Intersymbol Interference - Use this option to enable/disable ISI feature.
- Shortcut for Impairment Setup View - Use this shortcut to access the Impairment Setup View. For more details, refer to Impairment Setup View on page 222.

- Interference - Use this block to enable the interference (CMI or DMI). For details refer to Interference .
- Amplifier - This block represents the current value of Data Out's amplitude parameter. You can change the value by clicking on this block and modify the respective parameter in the Parameters window.
- Delay - Set the delay of the active edge of the data output.
- Data Generation - Acts as the output port for the generator which may be connected to the DUT.

Trigger

The following section of the System View represents the trigger function:



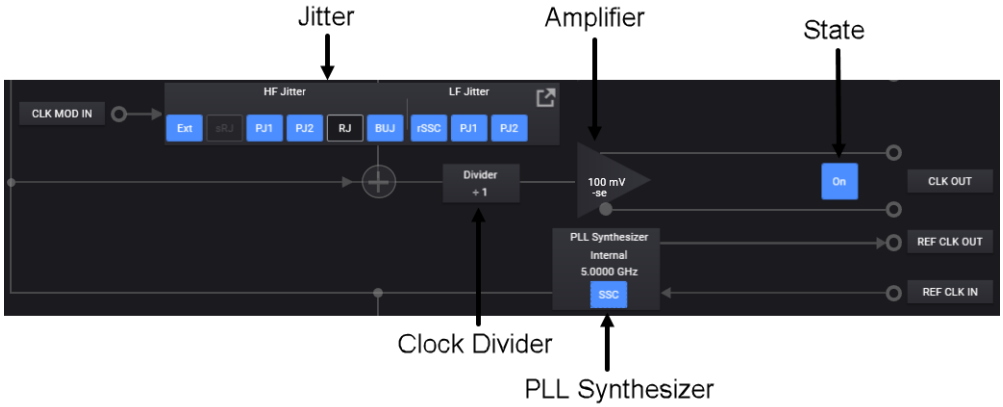
It allows you to apply settings on the Trigger Out port or location.

It includes the following blocks:

- State - Click on the Off button to enable the output of Trigger Output for the channel. Once the output is enabled, the button changes to “ON” On . If you press the button again, it will turn the state “OFF”.
- Amplifier - Use this block to set the parameters related to amplifier of the trigger output.
- Output Timing - Use this block to set the delay of the active edge of the trigger output.

Clock

The following section of the System View represents the clock function:

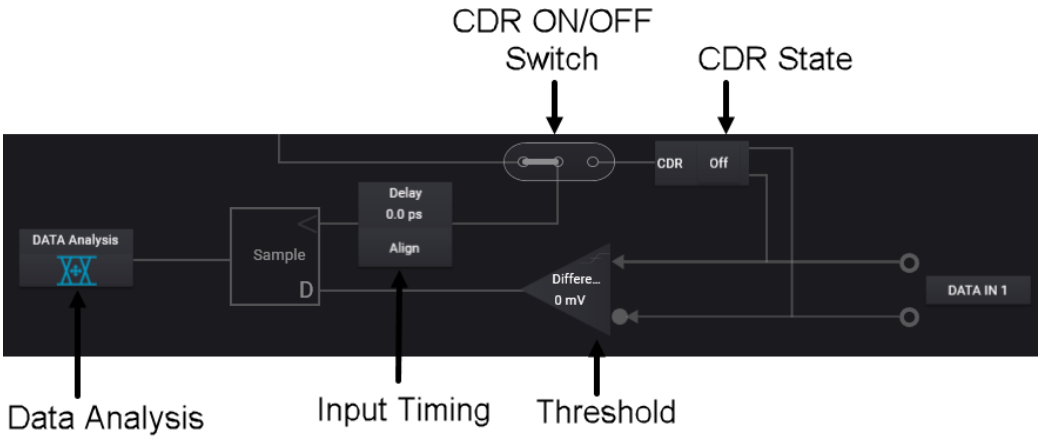


The clock function allows you to apply settings on the Clock Out port or location. It includes the following blocks:

- State - Click on the Off button to enable the output of Clock Source. Once the output is enabled, the button changes to “ON” On. If you press the button again, it will turn the state “OFF”.
- Jitter - Use this block to enable the elements of High Frequency Jitter, Low Frequency. For more details on jitter, refer to Jitter Setup on page 428.
- Amplifier - Use this block to set the parameters related to amplifier of the clock output.
- Clock Divider - Use this block to set a factor on which the output signal will be divided.
- PLL Synthesizer - This block represents the currently selected clock source. You can change the clock source by clicking on this block and the modify the respective parameter in Parameters pane. To enable the SSC state jitter source, click on the SSC button. Once the SSC state is enabled, the button changes to “ON” SSC. This is how the bit rate is set. For example, 5 GHz sets the bit rate to 5 Gb/s. If you press the button again, it will turn the state “OFF”.

Analyzer

The following section of the System View represents the analyzer function:



The Analyzer function allows you to apply settings on the Data In port or location (analyzer). It includes the following blocks:

- State - Click on the Off button to enable the CDR state. Once the CDR state is enabled, the button changes to “ON” On. For more details, refer to CDR Setup for M8020A on page 524. If you press the button again, it will turn the state “OFF”.
- Threshold - Use this block to set the threshold of the input comparator.
- Input Timing - Use this block to set input timing delay.
- Data Analysis - Use this block to set input threshold and sampling point delay.

System View with M8062A Integration

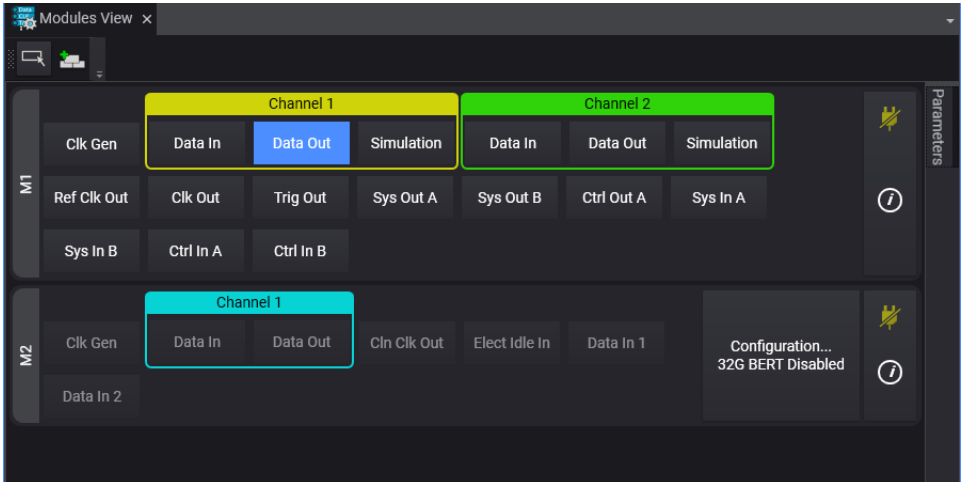
This section describes the block diagrams provided by the **System View** when M8062A is integrated with other modules of M8020A.

M8062A Configuration

The following steps describe the procedure for M8062A configuration:

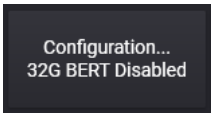
- Launch the M8070B software.
- If the **Modules View** is not already opened, go to **Menu Bar** > **System** and then click **Module View**.
- Locate the **M8062A** module. The following figure shows an example of

Module View when an M8062A (M2) and an M8041A (M1) are installed in the M8020A system:

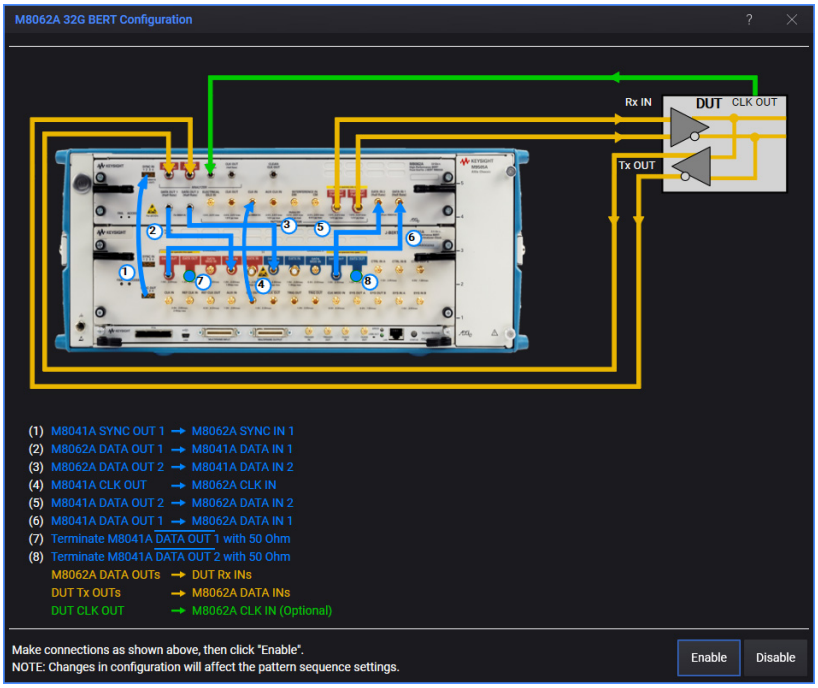


NOTE The M8062A module cannot be used standalone. It must be used in combination with an M8041A module.

- Click the **Configuration...** button present on the M8062A module.



The **M8062A Configuration** dialog will appear as shown in the following figure:

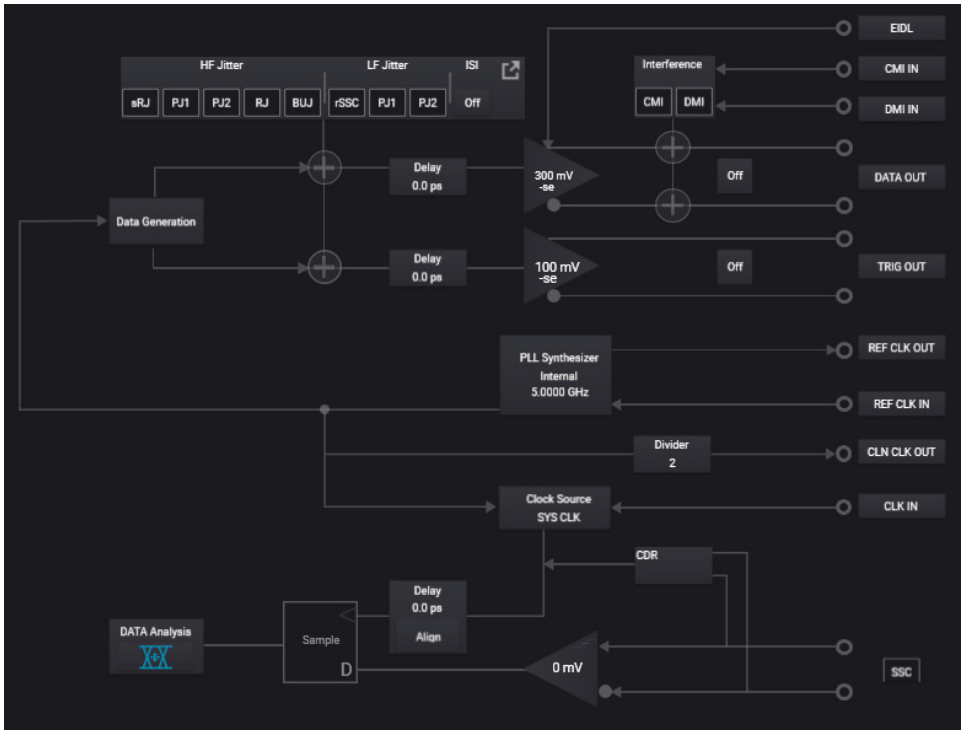


- Make the connections as described in the above figure.
- Click **Enable**.
- For the block diagram representation and interactively modify the settings of the currently mode, switch to **System View**. To do so, go to **Menu Bar** > **System** and then click **System View**.

NOTE System view for M8062A is available only when 32G mode is enabled.

NOTE In 32G mode, access to some M8041A user controls are disabled to facilitate software control of this configuration.

The following figure shows the **System View** of the M8062A module:



In the M8062A **System View**, the principal parts are represented by blocks which are connected by lines/arrows to show the relationship of the blocks. These blocks are highlighted by blue lines around the block on mouse focus. Parameters corresponding to the selected block are displayed in the **Parameters** window, on the right. The block may contain feature elements (for example, LF Jitter contains PJ and rSSC). You can click on the respective button to enable the feature elements. Once enabled, the feature elements are highlighted in blue color. For more details, refer to System View on page 209.

In addition to the blocks that are described in the section System View on page 209, the M8062A **System View** has the following new blocks:

- **Clean Clk Out** - Half-rate, or divided, clock output with no applied jitter.
- **Clk In** - Pattern Generator clock input (half-rate). Connect to clock output of M8041A.
- **Clock Source** - Selects the clock source (CDR, System Clock or Clock In) for the M8062A DataIn port (Analyzer).
- **CDR** - Selecting "CDR" as the M8062A DataIn clock source enables the Analyzer CDR, so that incoming data is sampled using the recovered clock.
- **Auto Re-Lock** - When this feature is enabled (the default setting) the CDR will automatically re-lock when there is a loss of lock. When it is disabled, the CDR will only attempt to re-lock when manually initiated by clicking on the arrow next to the Auto Re-Lock On/Off button. It may be necessary to perform a manual re-lock after a pattern change.
- **High Transition Density** - For data patterns with high transition density, such as 1010 pattern, the CDR may have trouble gaining lock. Enabling the High Transition Density setting reduces the CDR's internal gain to allow it to better lock on patterns with high transition densities. It may be necessary to perform a manual CDR re-lock after a change in the High Transition Density setting.
- **Optimize** - After the CDR has gained lock, certain condition changes, such as increasing applied jitter levels, can cause the analyzer to begin to measure errors. Executing the Optimize function causes the CDR to perform a finer alignment adjustment, which may result in a return to an error-free measurement.

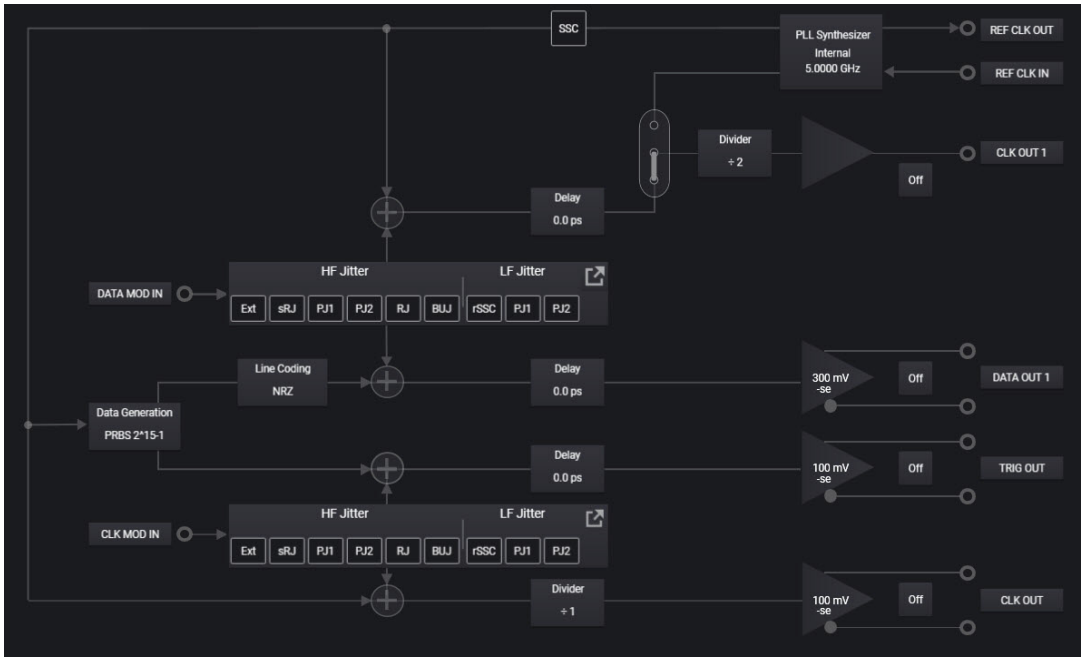
NOTE

When using the Analyzer CDR, it may take a longer time to lock and achieve BER=0 after a frequency change than with the other clock sources.

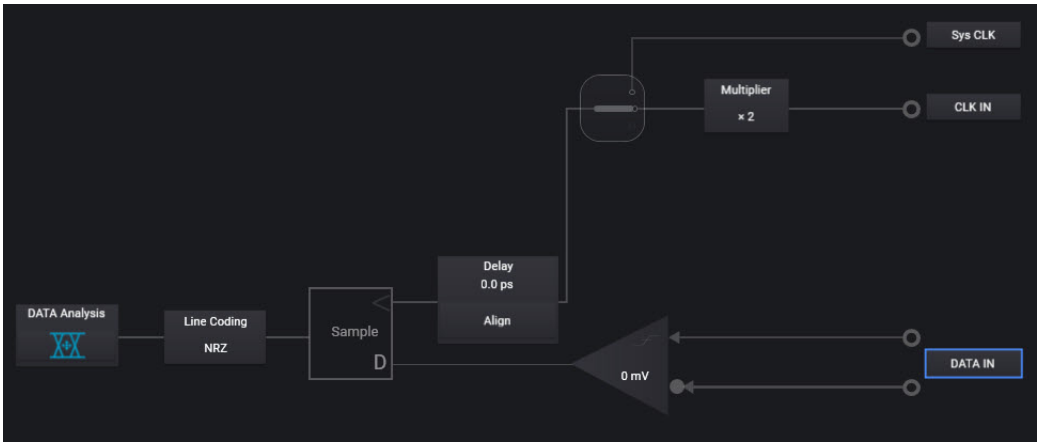
M8040A System View

The **System View** displays the block diagram representation of the currently selected channel of the M8040A modules (M8045A and M8046A). In addition, it also allows you to interactively modify the settings for each channel.

The following figure shows the **System View** of channel 1 of the M8045A module (M1):



The following figure shows the **System View** of the M8046A module (M2):



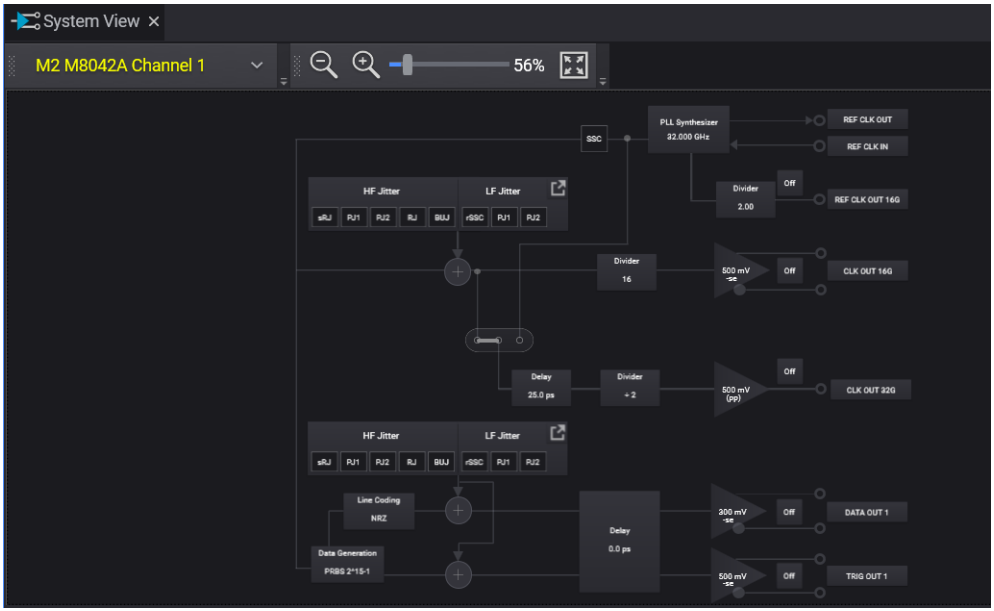
The principal parts of the M8045A and M8046A **System View** are represented by blocks which are connected by lines/arrows to show the relationship of the blocks. These blocks are highlighted by blue lines around the block on mouse focus. On clicking these blocks, the mostly used parameters are available which can be configured using the on-screen numeric keypad.

However, parameters corresponding to the selected block are displayed in the Parameters window, on the right. The block may contain feature elements (for example, HF Jitter contains PJ1, PJ2 and RJ). You can click on the respective button to enable the feature elements. Once enabled, the feature elements are highlighted in blue color. For more details, refer to System View on page 209.

M8050A System View

The **System View** displays the block diagram representation of the currently selected channel of the M8050A modules (M8009A, M8042A and M8043A). In addition, it also allows you to interactively modify the settings for each channel.

The following figure shows the **System View** of the of channel 1 of the M8042A generator module (M2):



The principal parts of the **System View** are represented by blocks which are connected by lines/arrows to show the relationship of the blocks. These blocks are highlighted by blue lines around the block on mouse focus. On clicking these blocks, the mostly used parameters are available which can be configured using the on-screen numeric keypad.

However, parameters corresponding to the selected block are displayed in the Parameters window, on the right. The block may contain feature elements (for example, HF Jitter contains PJ1, PJ2 and RJ). You can click on the respective button to enable the feature elements. Once enabled, the feature elements are highlighted in blue color. For more details, refer to System View on page 209.

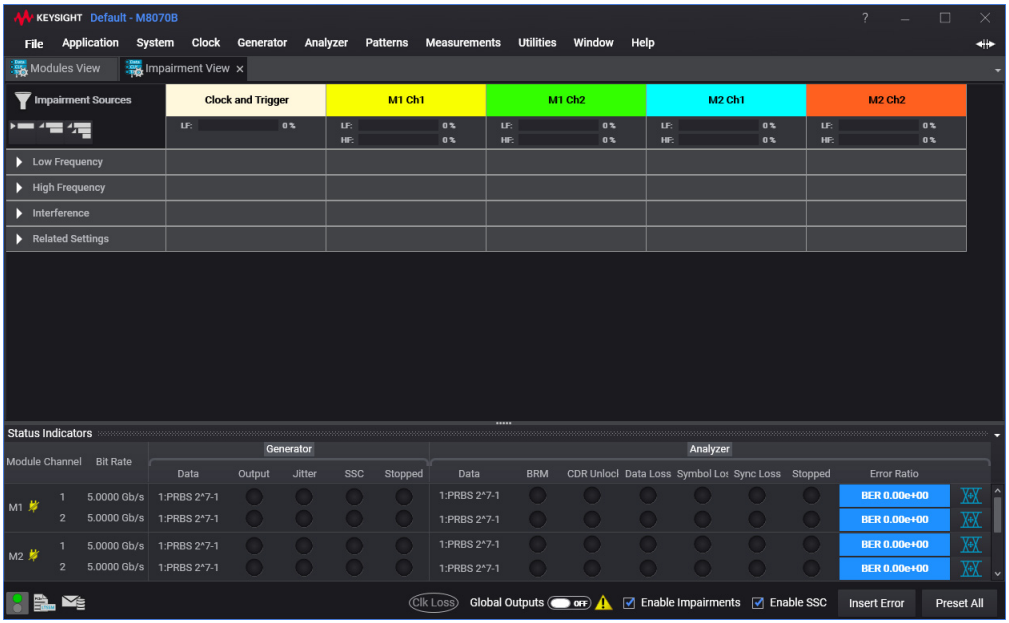
Impairment Setup View

The **Impairment Setup View** provides a tabular representation of the Impairment Sources and their corresponding parameters for each Data Out channel of the connected modules. This tabular visualization helps you to view, compare and configure the Impairment Source parameters for each channel in the same window.

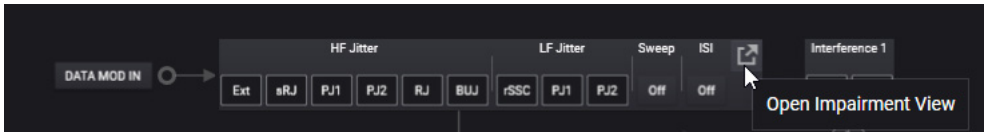
How to Access the Impairment Setup View

The following are the two ways to access **Impairment Setup View**:

1 Through **Menu Bar** - Go to **Menu Bar** and then click **System** > **Impairment Setup View**. The **Impairment Setup View** will appear as shown in the following figure:



2 Through **System View** - The **Impairment Setup View** can also be accessed through the **System View** by clicking on the **Open Impairment View** shortcut as shown in the following figure:



Features of the Impairment Setup View

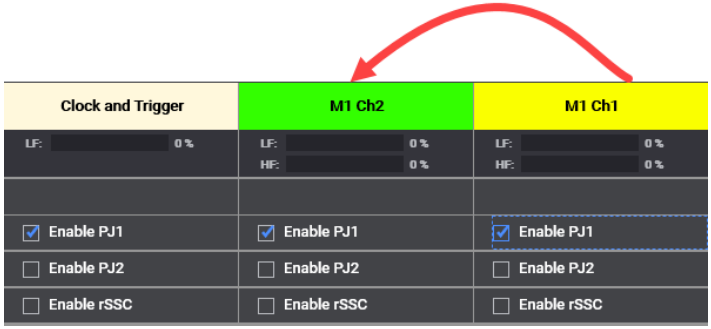
In this tabular matrix of the **Impairment Setup View**, the rows consist of the Impairment Sources, their corresponding options and their related parameters. The columns represents channels Data Out, Clock and Trigger parameters for each channel.

Columns

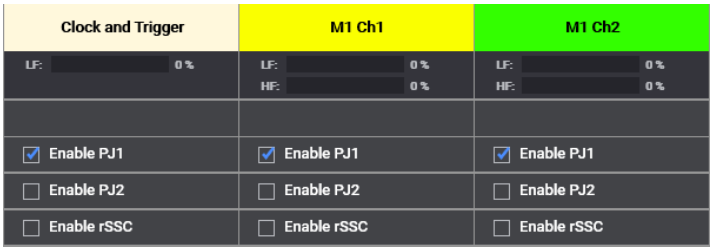
Each channel of a module is represented using a particular color code, which form the column header and they correspond to the color-coding used for that channel in the **Modules View**. See Module View on page 179.

You may rearrange the column headers by clicking and dragging a header to the desired position.

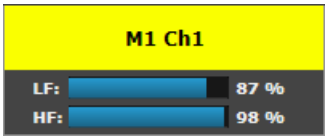
For example, if you want to view the settings of M1Ch2 first, then click and hold the cursor on M1 Ch2, drag it to the right and release the cursor at the desired position.



The **Impairment Setup View** will now show the channel position as shown in the following figure:



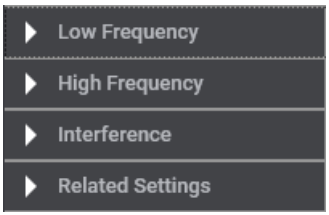
Under each column's header, there are Low Frequency (LF) and High Frequency (HF) usage indicator. The Clock and Trigger has a Low Frequency indicator only. The following figure shows LF and HF indicator for channel 1 of module 1 (M1 Ch1):



These indicators display how much low frequency and/or high frequency is applied on each channel in percentage.

Rows

The Impairment Sources form the rows in the tabular matrix and have a hierarchical structure. To expand and view the options, click ▶ to the left of each Impairment Source.



The following list shows the Impairment Sources and their respective options that are available in the **Impairment Setup View**.

1 Low Frequency (Jitter)

   a PJ

   b rSSC

2 High Frequency (Jitter)
   a PJ1
   b PJ2
   c BUJ
   d RJ
   e sRJ
   f Sweep
3 Interference
   a ISI
   b CMI
   c DMI
4 Related Settings
   a SSC
   b Clk/2 Jitter

You can view, compare and even to configure the values of Impairments Source parameters for each channel. For more details on these Impairment Sources and their respective parameters, please refer to the chapter Setting up Generator on page 357.

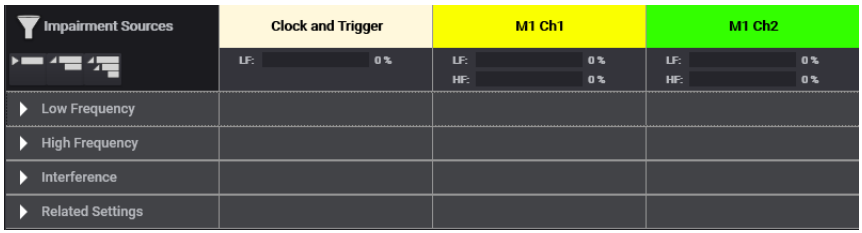
Viewing Options in the Impairment Setup View

The **Impairment Setup View** provides the following viewing options:

- Collapse All

  This is the default viewing option of the tabular view.

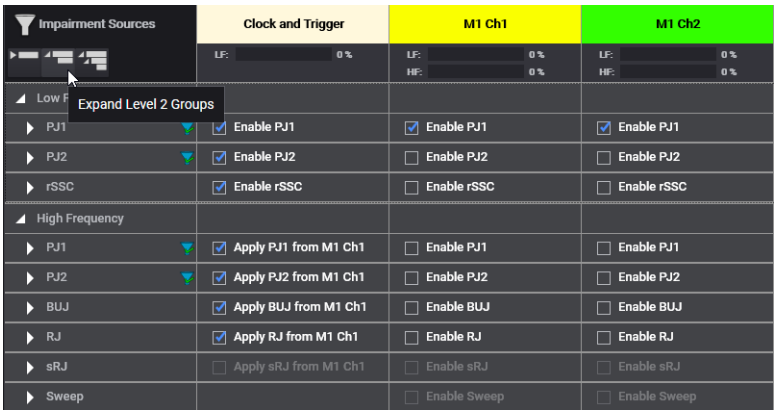
  Click on the button to collapse the Impairment Sources rows, such that only the top-level hierarchy is displayed. In other words, in this view option, the options under each Impairment Source for the corresponding Data Out, Clock and Trigger of a channel are hidden.



- Expand Level 2 Groups

  This is one-level expansion of the tabular view.

  Click on the button to view options available under Impairment Sources. This view allows you to enable/disable the Impairment Sources options for corresponding channel.



- Expand All

  This is two-level expansion of the tabular view.

  Click on the button to view the parameters and the corresponding values for each option under the Impairment Sources. This view provides a full view of impairment setup view. Using this view, you can either enable or disable the Impairment Source options and also modify the parameter's value for each channel.

Impairment Sources	Clock and Trigger	M1 Ch1	M1 Ch2
	LF: 0 %	LF: 0 % HF: 0 %	LF: 0 % HF: 0 %
Low Frequen			
PJ1	Enable PJ1	Enable PJ1	Enable PJ1
Frequency	1.0000 kHz	1.0000 kHz	1.0000 kHz
Amplitude	0.0 mUI	0.0 mUI	0.0 mUI
PJ2	Enable PJ2	Enable PJ2	Enable PJ2
Frequency	1.0000 kHz	1.0000 kHz	1.0000 kHz
Amplitude	0.0 mUI	0.0 mUI	0.0 mUI
rSSC	Enable rSSC	Enable rSSC	Enable rSSC
Frequency	33.000 kHz	33.000 kHz	33.000 kHz
Amplitude	0.0 mUI	0.0 mUI	0.0 mUI
High Frequency			
PJ1	Apply PJ1 from M1 Ch1	Enable PJ1	Enable PJ1
Frequency	10.000 MHz	10.000 MHz	10.000 MHz
Amplitude	0.0 mUI	0.0 mUI	0.0 mUI

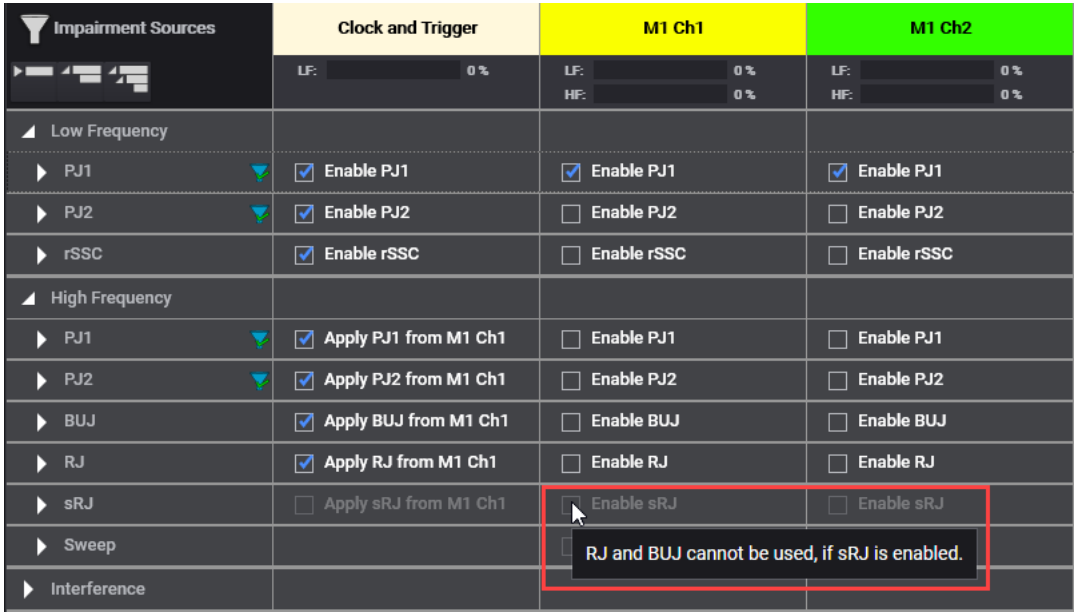
Expand All

How to set parameters in Impairment Setup View

To enable an option for an Impairment Source corresponding to a Channel or Clock and Trigger, select the check-box for the corresponding setting. To disable the option, unselect the check-box. The following shows an example how to enable the PJ option:

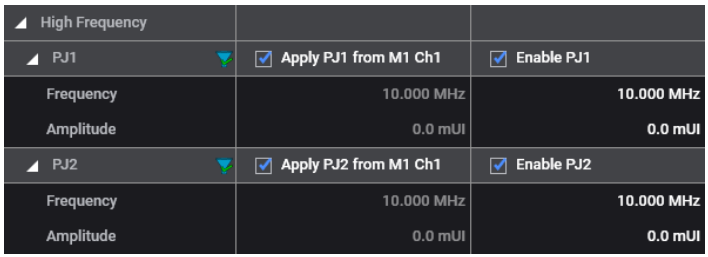
rSSC	Enable rSSC

Some options available under the impairment sources are dependent on each other, such that enabling one or more option disables other options. Hover the mouse cursor on the tabular cells to understand the relational impact of such options, as shown in the example below.

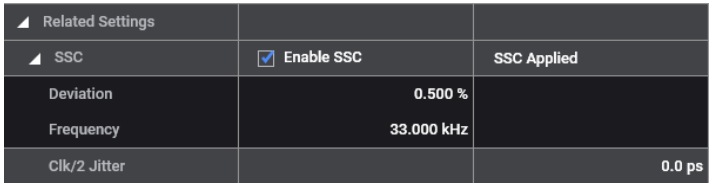


The following are the dependencies which should be followed while configuring parameters:

- Sweep cannot be enabled if PJ is enabled.
- sRJ cannot be used if BUJ is enabled.
- RJ and BUJ cannot be used if sRJ is enabled.
- PJ and PJ2 cannot be used if Sweep is enabled.
- High Frequency Jitter profile of Clock and Trigger Out are controlled by Data Out of channel 1 as shown in the following figure:



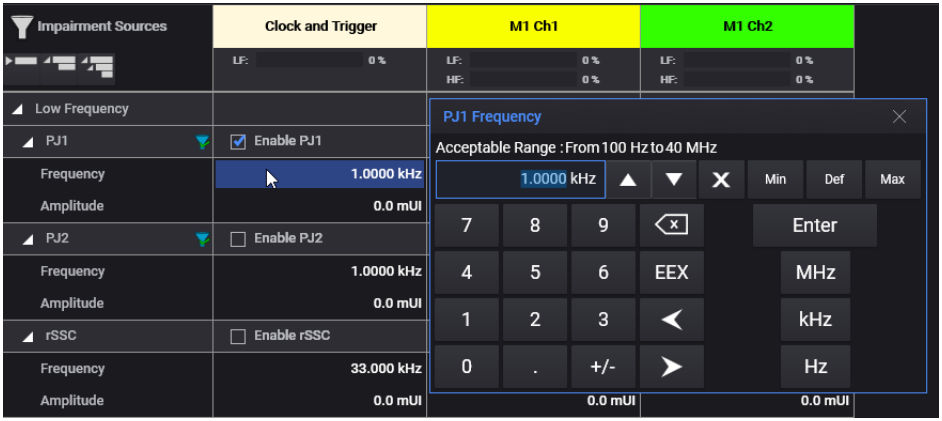
- The SSC can be enabled/disabled for all Data Out channels by a single option as shown in the following figure:



The option to either enable or disable SSC feature is available under Clock and Trigger column.

The **Impairment Setup View** also allows you to modify the parameter values. Depending upon whether the keypad option is enabled or disabled, the parameter values can be modified in the following ways:

- **When the keypad is enabled:** In this case when you click on the values which you want to modify, an on-screen numeric keypad appears as shown in the following figure:



Either type-in the values using the keyboard or use the on-screen numeric keypad to modify these values.

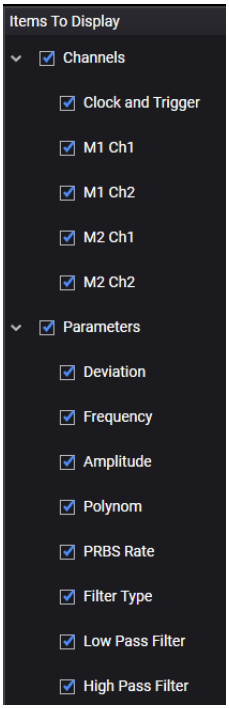
For more details on how to use the on-screen numeric keypad, refer to On-Screen Numeric Keypad on page 166.

- **When the keypad is disabled:** In this case, you are directly allowed to type-in the values using the keyboard.

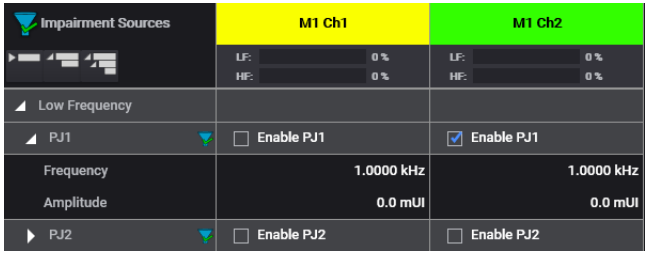
How to Use Filters

Filters can be used to select the items to be displayed in the **Impairment Setup View**. In other word, it helps you to hide the items which are not required in the **Impairment Setup View**.

To apply filters, click on the icon. This opens **Items To Display** window as shown in the following figure:



By default, all items (Channels and Parameters) in the **Items To Display** window are selected. However, you can select/unselect the check-box to show/hide the items. The changes are immediately reflected in the **Impairment Setup View**. For example, upon selecting M1 Ch1, M1 Ch2 under the Channels list and PJ under Jitter Types, the **Impairment Setup View** appears as shown below:

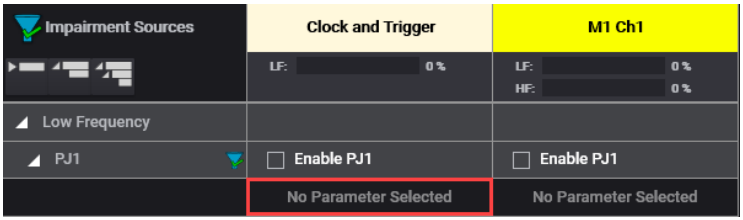


NOTE

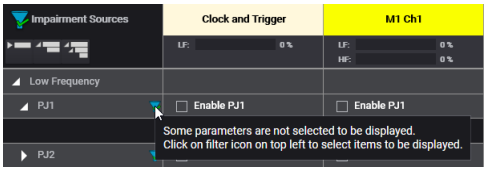
It is mandate to select at-least one channel. Failing this will display a message on the **Impairment Setup View** window that no channels are selected.

Notice that the icon appears on the top right of the **Impairment Setup View** which indicates that the filter has been applied.

If the channels are selected but their corresponding parameters are not selected, a message that no parameters are selected will be displayed.



The icon also appears in front of each item whose corresponding parameters are not selected. If you move the mouse pointer on this icon, a tool-tip message is displayed as shown in the following figure:



Impairment Setup View Support by the M8050A System

The **Impairment Setup View** provides a tabular representation of the **Impairment Sources** and their corresponding parameters for each **Data Out** channel of the connected module. This tabular visualization helps you to view, compare and configure the Impairment Source parameters for each channel in the same window.

The M8050A system includes the M8009A clock and M8042A pattern generator modules. This section describes the behavior of **Impairment Setup View** when the **Configuration Mode** of the Ch Clk Out 2 of the M8009A module is selected as either **Module Clock** or **Forwarded Clock**.

Here is the **Impairment Setup View** when the **Configuration Mode** is selected as **Module Clock**:

Impairment Sources	Clock	M2 Ch1	M2 Ch2
	LF: 0 %	LF: 0 % HF: 0 %	LF: 0 % HF: 0 %
Low Frequency			
High Frequency			
Interference			
Related Settings			

In this mode, the **Impairment Setup View** will display a tabular representation of the **Data Out** channels (M2 Ch1 & M2 Ch2) along with their corresponding parameters.

Here is the **Impairment Setup View** when the **Configuration Mode** is selected as **Forwarded Clock**:

Impairment Sources	Clock	M1 ChClkOut2	M2 Ch1
	LF: 0 %	LF: 0 % HF: 0 %	LF: 0 % HF: 0 %
Low Frequency			
High Frequency			
Interference			
Related Settings			

In this mode, the **Impairment Setup View** will display a tabular representation of the **Forwarded Clock Out** (M1.ChCLKOut2) of the M8009A module and **Data Out** (M2 Ch1) channel of the M8042A module and their corresponding parameters.

For details on how to configure parameters, refer to the section Impairment Setup View on page 222.

Group View

The **Group View** allows you to:

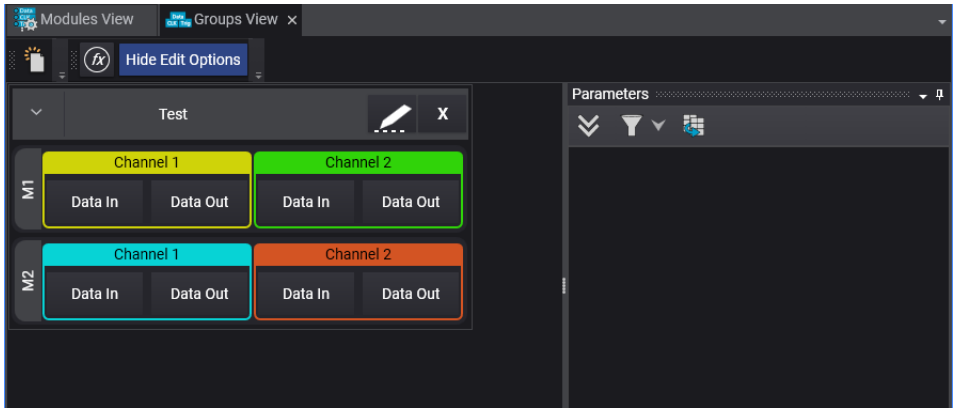
- Add/remove ports of a group.
- Set the properties of functional block of a group.

How to Launch Group View

The **Group View** is automatically launched when you create a group from the **Module View**. For details, refer to Creating Groups in the Module View on page 208.
However, you also launch the **Group View** from the main GUI. To do so:

- Go to the **Menu Bar** > **System** and then select **Group View**.

The **Group View** will appear as shown in the following figure:



The **Group View** includes the following elements:

- Tool bar
- Group View

Tool bar

The tool bar includes the following elements to perform specific functions:

Table 52

Elements	Name	Description
	Create New Group	Opens the **System Group Editor** which allows you to create a new group. For more details, refer to Create New Groups in Group View on page 236.
	Show Functional Block in Group	Use this toggle button to show functional blocks or locations in a group.
Show Edit Options	Show Edit Options	Use this toggle button to show/hide the group edit options.
	Edit Existing Group	Opens the **System Group Editor** which allows you to edit the group. For details, refer to Edit Existing Group on page 238. This icon is only visible when the group is in the edit mode.
X	Delete Group	Deletes the group.

Group View

The **Group View** allows you to create, edit and delete a group. In addition, it also allows you to set the properties of functional block of the group. These features are further described in the upcoming sections of this chapter.

Create New Groups in Group View

To create a group in **Group View**:

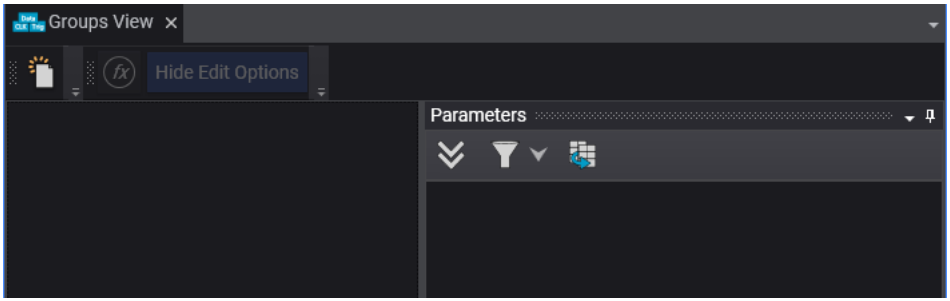
- Click **New Group** icon available on the tool bar. This will open the **System Group Editor**.
- Select the ports or locations from the left side the **System Group Editor** and the preview of selected ports or locations will appear on right side. See the following figure:

- Type a group name in the provided field and click **Create**. A new group will be created under that name.

Show Function Block/Location in Groups

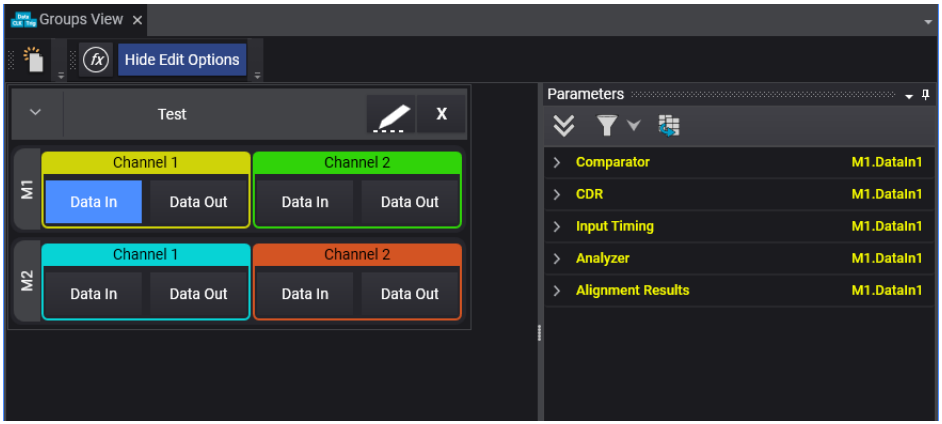
The **Group View** allows you to set the group properties either through functional blocks or through locations in the group.

You can click icon to switch to show functional blocks in the group. See the following figure:



The group is represented in the form of functional blocks available in the group. Once you click on the function block, the respective properties of the functional block are visible in the **Parameters** window. You can now set the properties of each functional block.

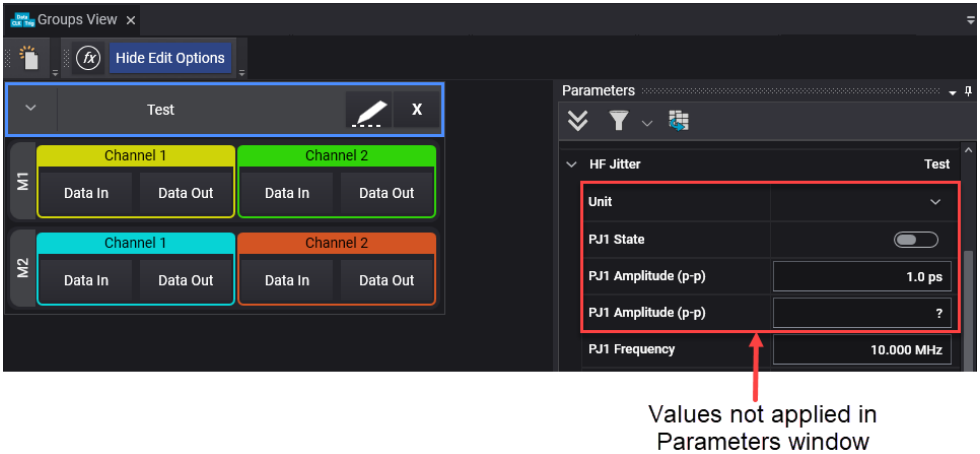
You can click icon to switch to show locations in the group. See the following figure:



The group is represented in the form of ports or locations available in the group. Once you click on the port or location, the respective properties of the port or location block are visible in the Parameters window.

The main advantage of the **Group View** is that it allows you to set the properties patterns/sequence of similar ports at once.

However, if you set the properties of the similar ports or locations that exists in different channels of a group, the properties of the ports or locations will not be applied. If you try to group the properties by clicking on the header of **Group View**, the corresponding value in the Parameters window will either be blank or show “?”.
See the following figure:

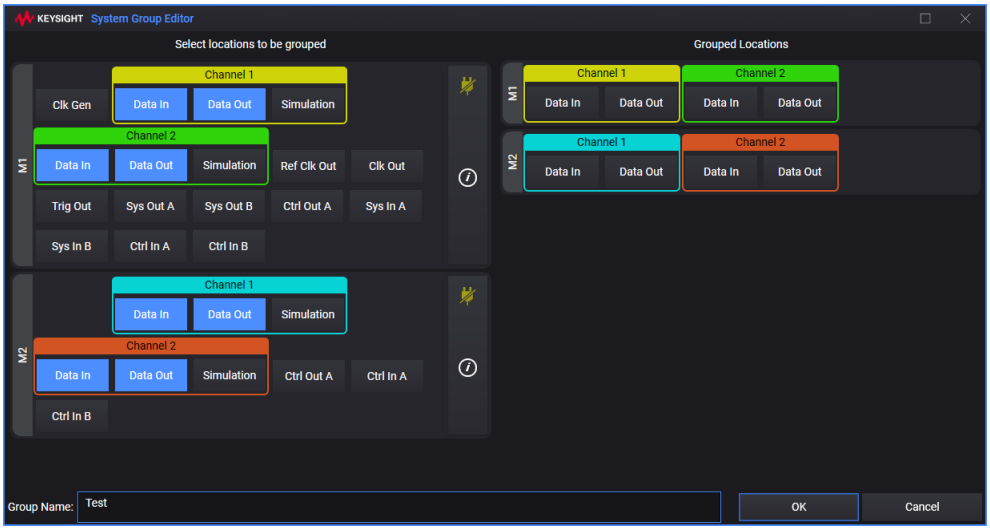


In this situation, you have to specify the property’s value which will be later applied to both ports or locations.

Edit Existing Group

To edit an existing group;

- Click on the **Edit Existing Group** icon. This will open the **System Group Editor** window.
- Select the ports or locations from the left side of the **System Group Editor** and the preview of selected ports or locations will appear on right side. See the figure below:



- Click **OK**. The group will be edited. However, if you provide a new group name in the provided field and click **OK**, a new group will be created under that name.

Delete a Group

You can also delete a group. To do so:

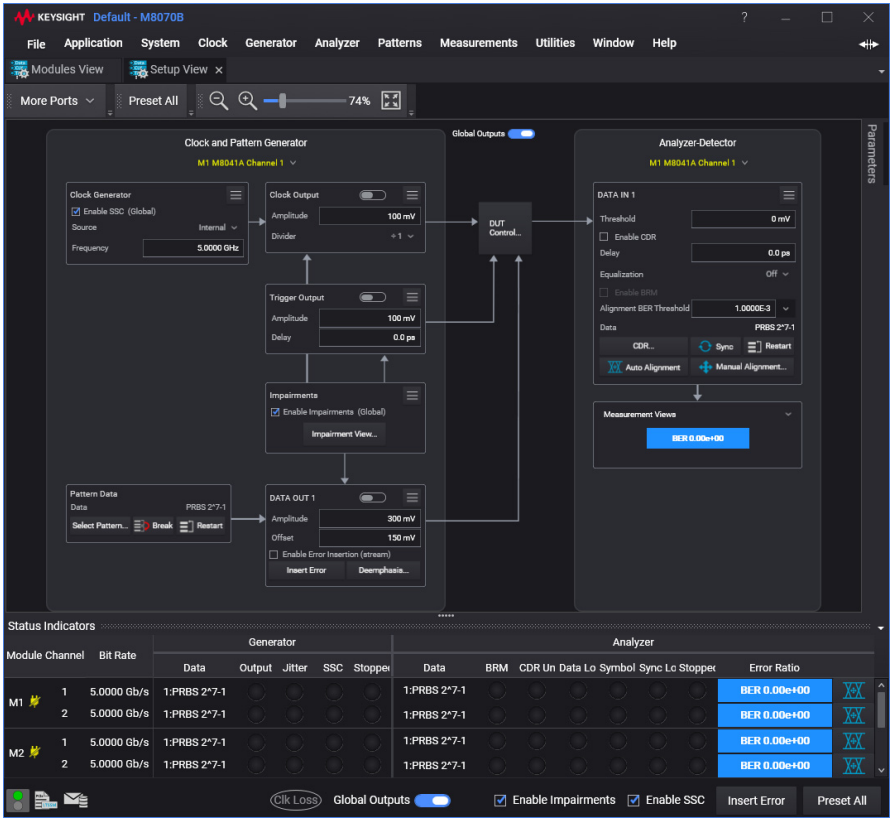
- Click on the **Delete Group** icon. It will open a **Delete Group** message box.
- Click **Delete**. The group will be removed from the view.

Setup View

The **Setup View** shows the block diagram of the pattern generator and error detector to provide a simple overview of the most important instrument settings at a glance.

How to Access the Setup View

The **Setup View** can be accessed on clicking the **Setup View** tab, once the M8070B software is launched. It can also be accessed through Menu Bar. Go to **Menu Bar** and then click **System** > **Setup View**. Please note that the **Setup View** user interface is different for each system, depending upon the connected modules. The following figure shows an example of the **Setup View** for M8020A system (M8041A and M8051A):



Similarly, you can access the **Setup View** for M8020A/M8040A/M8050A system which can include M8041A, M8042A, M8009A, M8051A, M8062A, M8043A, M8045A, M8046A, M8199A, M8199B, M8194A, M8195A, M8196A, clock recovery and real-time oscilloscope that can be controlled by M8070B.

Understanding Setup View

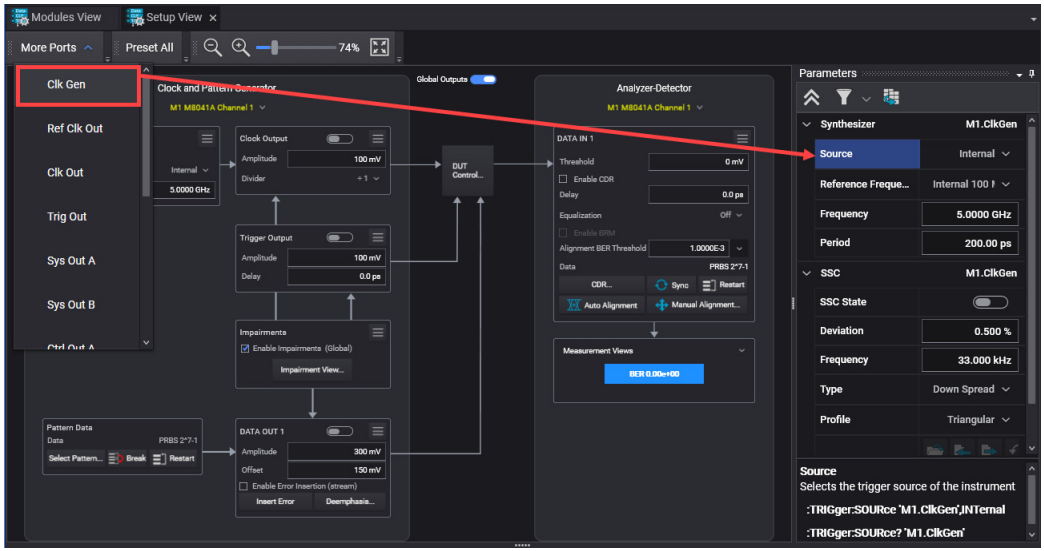
The **Setup View** interface includes a toolbar, a block diagram and a parameter window. All these GUI elements are described in the following section.

NOTE The information about the GUI elements such as buttons and text fields, where the user inputs are required, are provided in the form of tooltip.

Toolbar

- **More Ports**

  The drop-down option allows you to configure the ports which are not available in the Generator or Analyzer blocks. On selecting a port, the respective parameters are displayed in the **Parameters** window.



- **Preset All**

  This option opens the “Preset Instrument State” dialog which resets the instrument state to factory default settings. For details, see section “Preset Instrument State” in the File Menu on page 141.

- **Zoom Tool**

  The following figure shows the options provided by the zoom tool.

  The zoom tools provide the following functionality:

  - The **Zoom In** button allows you to enlarge the block diagram to view more details.
  - The **Zoom Out** button allows you to reduce the block diagram.
  - The **Zoom Slider** allows you to zoom in or zoom out the block diagram.
  - The mouse wheel also provides a quick alternative to the zoom control. To zoom in and out using the mouse, hold down the [Ctrl] key while you turn the mouse wheel. Each click, up or down, increases or decreases the zoom factor by 25%.
  - The **Fit to View** button fits the width of the window so that the user does not have to scroll the block diagram to the right or to the left.

Block Diagram

This section shows the block diagram of the “Clock and Pattern Generator” pane and the “Analyzer-Detector” pane which is connected via a DUT Control.... Each pane displays the functional blocks and their frequently used parameters. You can configure these basic parameters to perform a measurement.

The user interface provided by the block diagram provides the following features:

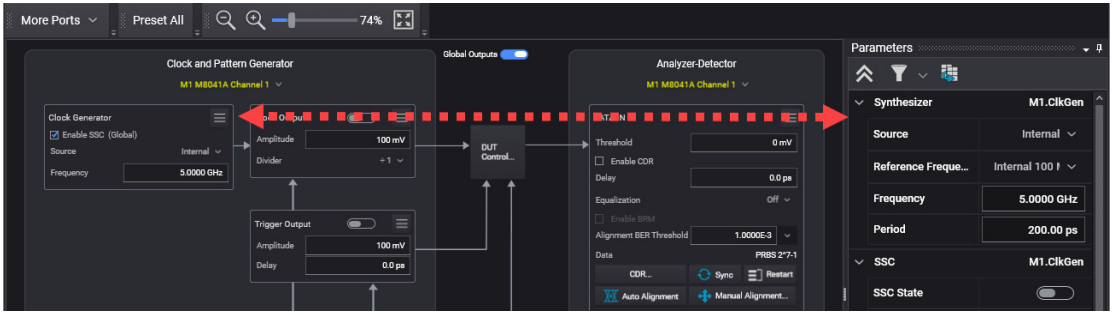
- **Channel Selection** - The channel selection for the Generator or Analyzer can be made using the drop-down list. Depending upon the selected channel, its corresponding block diagram will be displayed.

  Please ensure to enable the outputs by clicking on the **Global Outputs**

button. The same can be done by clicking on the

Global Output button present on the status bar.

- **Parameters Window** - Once, the channel section is made, you can configure the basic parameters of each functional block. However, you can also view and configure the detailed parameters on clicking the ≡ button, available at the top right of the block. All the parameters related to that functional block will be displayed in the **Parameter** window.



- **Clock and Pattern Generator pane**

  The “Clock and Pattern Generator” pane display the functional blocks which are related to clock generation and pattern generator. It may include Clock Generator, Clock Output, Trigger Output, Impairments, Pattern Data and Data Out 1 for a given channel. However, these functional blocks may vary, depending upon the type of module. In case of M8046A, the Data Out functional will show an additional **Coding** parameter. Similarly for other modules such as M8062A or AWG modules (M8194A/M8195A/M8196A), the functional blocks may vary depending upon the channel selection.

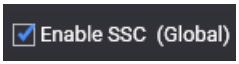
- **Analyzer-Detector pane**

  The “Analyzer-Detector” pane display the functional blocks like DATA In which are related to error detection. It may include, Threshold, Equalization, CDR, depending upon the connected modules. For example, the CDR option will not be available for M8046A analyzer. This pane also provides access to various measurements which are supported by the selected analyzer channel. For example, the eye diagram and output level measurements will not be available for M8046A analyzer.

GUI Elements Description

The various GUI elements which are available in the block diagram are described below:

- **Check-Box** - You can use the check-box feature to enable/disable the feature such as **Enable SSC**, **Enable CDR**, etc. The following is an example of **Enable SSC** check-box:

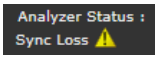


- **Toggle Button** - You can use to the toggle button to the enable the outputs such as clock output, trigger output, etc. The following is an example of **Global Output** button.

- **Command Button** - You can also use the command buttons such as **Break**, **Restart** and **Sync** to perform some actions. The following is an example of **Restart** button:

- **Buttons that opens another window** - There are some buttons which takes you to another window such as **Deemphasis...**, **CDR....**, **DUT Control...**. When you click on these buttons, they open with the respective window/parameters. The following is an example of button which take you to **Impairment View** window:

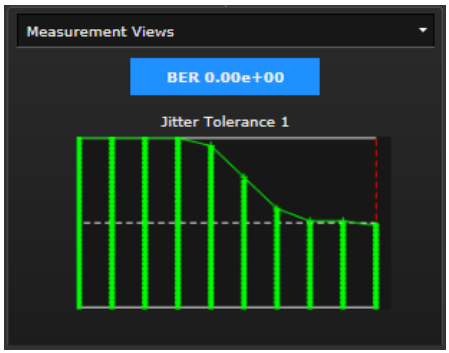
- **Status Information** – Depending upon the analyzer's performance, this option provides the current status of the analyzer such as stopped CDR unlocked, sync loss, etc. The following is an example of analyzer status when there is a sync loss:



- **Measurement Selection** – Use this drop-down list to select the measurement. The measurement will be provided depending upon the selected analyzer channel.

- **Status Indicator for Calculated BER/SER** – Indicates the status of the calculated BER/SER.

- **Measurement Preview** - Display the measurement preview of the currently run measurement. If you have already run the measurement once, it will show the status of last run measurement. You can double-click on the measurement preview to open the measurement window, provided the instance of that measurement is not closed. The following figure shows an example of measurement preview when the Jitter Tolerance measurement is executed.



How to perform a basic measurement

Follow the given steps to perform a basic measurement using a **Setup View**:

1. Open the **Setup View** window.
2. From the block diagram, select the channel for the “Clock and Pattern Generator” and “Analyzer-Detector” pane.
3. Use the available functional blocks to configure the required parameters for the “Clock and Pattern Generator” and “Analyzer-Detector” pane.
4. Click **Auto Align** button to start the BER threshold auto alignment. Click **Manual Alignment...** button, in case the manually aligning of the sampling point is required.
5. Select the measurement. It will take you to the respective measurement window.
6. Run the measurement. You will see the measurement preview on the “Analyzer-Detector” pane.

Custom View

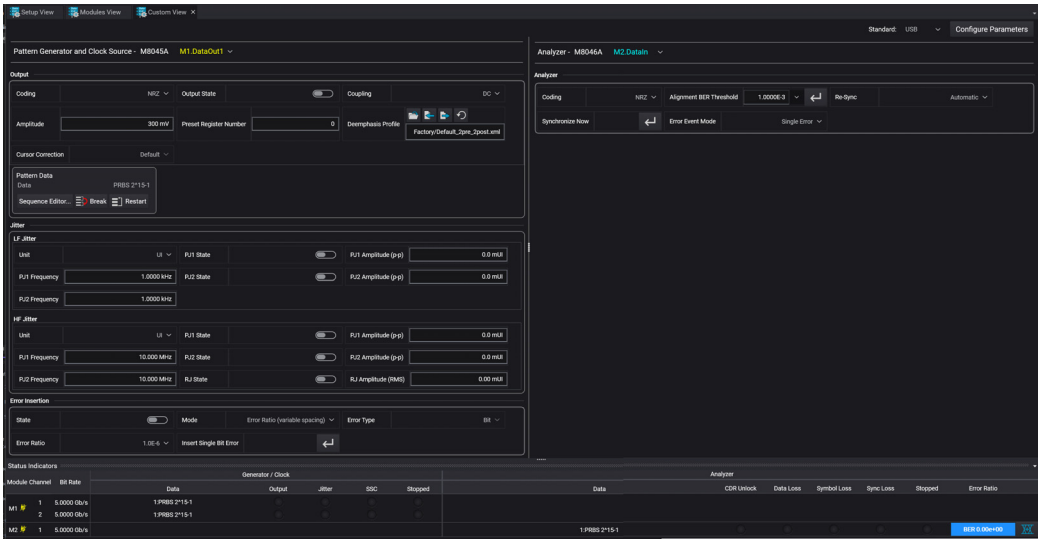
The **Custom View** allows you to simplify the configuration process by providing all the required parameters in a single, easy-to-use interface. Instead of switching between multiple views, you can configure the complete setup from one location, which improves efficiency and usability.

This feature is especially useful when performing USB or PCIe link training operations, as it provides quick access to configure all default parameters from a single window.

The **Custom View** is available under the **System** menu in the M8070B user interface. Selecting this option opens a **Custom View** window, which displays default configuration parameters for the following modules:

- Pattern Generator Modules (M8042A, M8041A, M8051A, M8045A)
- Analyzer Modules (M8041A, M8051A, M8046A)
- Clock Module (M8009A)
- Interference Source Modules (M8054A)
- BERT Front End Module (M8062A)
- AWG Modules (M8194A, M8195A, M8196A)

The following figure shows an example of a **Custom View** window showing the default configuration parameters for the M8040A modules (M8045A & M8046A):



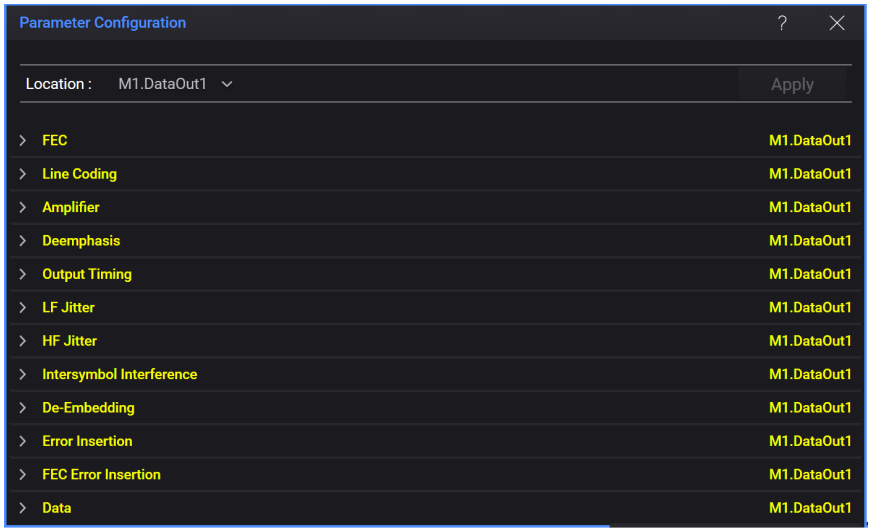
Use the intuitive drop-down lists to select module channels and quickly target specific configurations.

By default, the **Custom View** display displays the default parameters required for USB link training operations. To load the default parameters for PCIe link training operations, use the **Standard** drop-down list available at the top-right corner of the **Custom View** and select **PCIe**.

Configuring Parameters in the Custom View

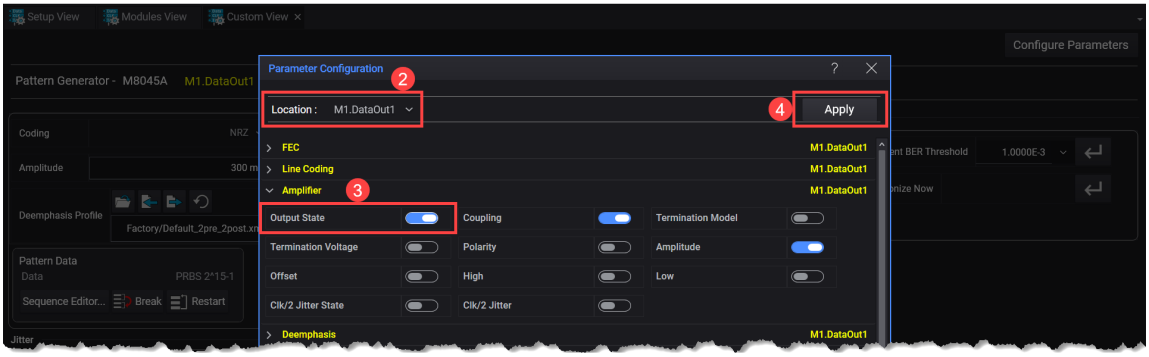
The **Custom View** provides a **Parameter Configuration** tool that allows you to show or hide parameters for selected channels. To access this tool, click **Configure Parameters** in the main M8070B interface.

Here is an example of a **Parameter Configuration** tool that displays all available functional blocks and their parameters for the selected module.



Use this tool to make and review changes. When ready, click the **Apply** button in the upper-right corner of the tool to confirm the changes. The **Custom View** layout updates dynamically to reflect all modifications. The **Apply** button remains disabled until you make at least one change, ensuring that updates are applied intentionally.

Here is an example to demonstrate how to show the **Output State** parameter in the **Custom View**:



1. In the **Custom View** window, click the **Configuration Parameters**. This opens the **Parameter Configuration** tool.
2. In the **Parameter Configuration** tool, select the desired location (for example, M1.DataOut1).
3. Under the **Amplifier** function block, enable the **Output State** parameters.
4. Click **Apply**. The **Custom View** now displays the **Output State** parameter.
5. Follow the similar steps to hide parameters in **Custom View**.

Key Features

Here are the key features of using the **Custom View** window:

- Access configuration parameters for all connected modules in a single view.
- Switch quickly between Pattern Generator, Analyzer, Clock, Interference Source, and AWG settings.
- Launch the **Sequence Editor** directly within **Custom View** without opening separate windows.
- Save the current **Custom View** settings and recall them later without reconfiguring the instrument each time. For details on how to save and recall an instrument setting, refer to "Recall/Save Instrument State on page 169".

Module Specific Configuration

The **Custom View** provides access to configuration parameters for all connected modules. However, some configurations are module-specific, as listed below:

- M8050A Modules

  For M8050A modules (M8042A and M8009A), an additional section is available for configuring the M8009A module, apart from the M8042A Pattern Generator settings.
- BERT Front End Module

  For M8062A, a dedicated **Configuration** button is available for setting the integration mode.
- AWG Module

  For M8195A AWG, the **M8195A Configuration** dialog option is available to allow tailored settings for interference channels.

PCIe LTSSM View

The PCIe LTSSM View allows you to simplify the link training workflow which reduces the number of configuration steps required to perform Link Training and Status State Machine (LTSSM) operations, making the process faster and more intuitive for users.

Although LTSSM functionality already exists in M8070B (See Interactive Link Training on page 698), the earlier configuration required multiple manual steps and detailed sequence editing. The PCIe LTSSM View now addresses these limitations by consolidating all the necessary parameters into a single, easy-to-use interface.

For details on the PCIe LTSSM View user interface, see PCIe LTSSM View User Interface on page 252.

NOTE

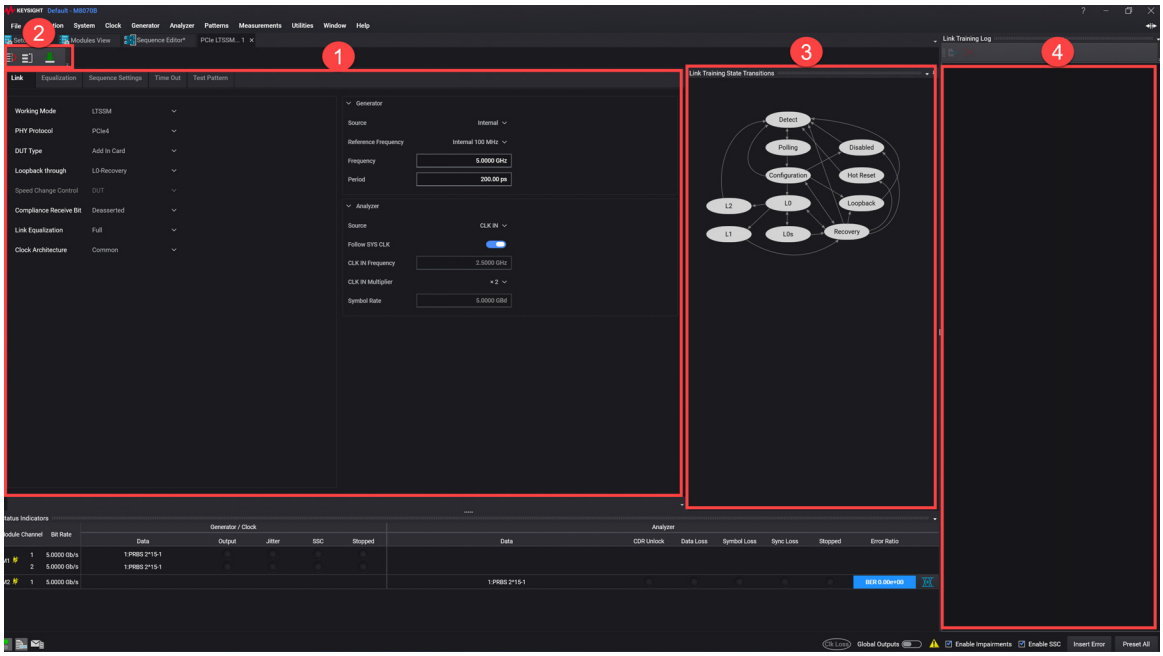
The PCIe LTSSM View is currently supported by M8040A modules only.

PCIe LTSSM View User Interface

The PCIe LTSSM View is available under the **Application** menu in the M8070B user interface.

NOTE **The PCIe LTSSM View is only available when the PCIe LTSSM license is enabled.**

Selecting this option opens a PCIe LTSSM View user interface as shown in the following figure.



The PCIe LTSSM View consists of the following GUI elements:

1 LTSSM Configuration Panel
2 Toolbar
3 Link Training State Transitions
4 Link Training Log

LTSSM Configuration Panel

This panel provides the required settings to initiate and control the LTSSM process. Only mandatory parameters are provided, reducing complexity while maintaining functional completeness.

This panel provides only the essential LTSSM configuration options, eliminating the need to manually manage multiple sequence blocks in the sequence editor.

This approach replaces the earlier workflow where users had to create and manage several sequence elements to perform link training.

This panel provides the following tabs:

1. **Link Tab** – This tab contains two sections. The first section displays key link training properties from the Sequence Editor, including PHY Protocol, DUT Type, Loopback Through, and Compliance Receive Bit. The second section provides important Generator and Analyzer module settings from the Modules View, such as Frequency, Source, CLK IN Multiplier, and other parameters required for link training.
2. **Equalization Tab** – This tab contains two sections. The first section provides preset equalization settings for different PCIe generations available in the Sequence Editor. The second section includes the PCIe RX EQ Matrix Editor for advanced equalization configuration.
3. **Sequence Settings Tab** – This tab contains settings related to link training sequence execution, including Trigger State, Lane, Link, and State Timeout File configuration.
4. **Time Out Tab** – This tab provides a dedicated timeout editor that displays all LTSSM state timeout values in a table format. Using this tab, you can directly edit and save timeout values. This enhanced functionality simplifies and speeds up the debugging workflow. When you click an LTSSM state in the bubble diagram, the corresponding state is automatically highlighted in the Time Out tab. You can then use the drop-down option to modify the timeout values for the sub-states of the selected state.
5. **Test Pattern Tab** - This tab contains test pattern configuration options for both Generator and Analyzer modules, allowing users to apply test patterns directly within the sequence block. In addition, when the PHY Protocol is set to PCIe 6, analyzer-side options such as Inverse Precoding and FEC Decoding options are also available in this tab.

For detailed information about the parameters available in the LTSSM Configuration Panel tabs, see Interactive Link Training on page 698.

Toolbar

The toolbar includes **Break**, **Restart**, and **Download** buttons for quick LTSSM control and configuration management.

1 **Break** - Starts the link training process when clicked. Its functionality is equivalent to the Break operation available in the Sequence Editor.

2 **Restart** - Breaks the current link and restarts the link training process. This behavior is also consistent with the Restart functionality in the Sequence Editor.

3 **Download** - Allows users to download and apply the configured settings directly to the Sequencer without switching back to the Sequence Editor, providing a faster and more seamless workflow.

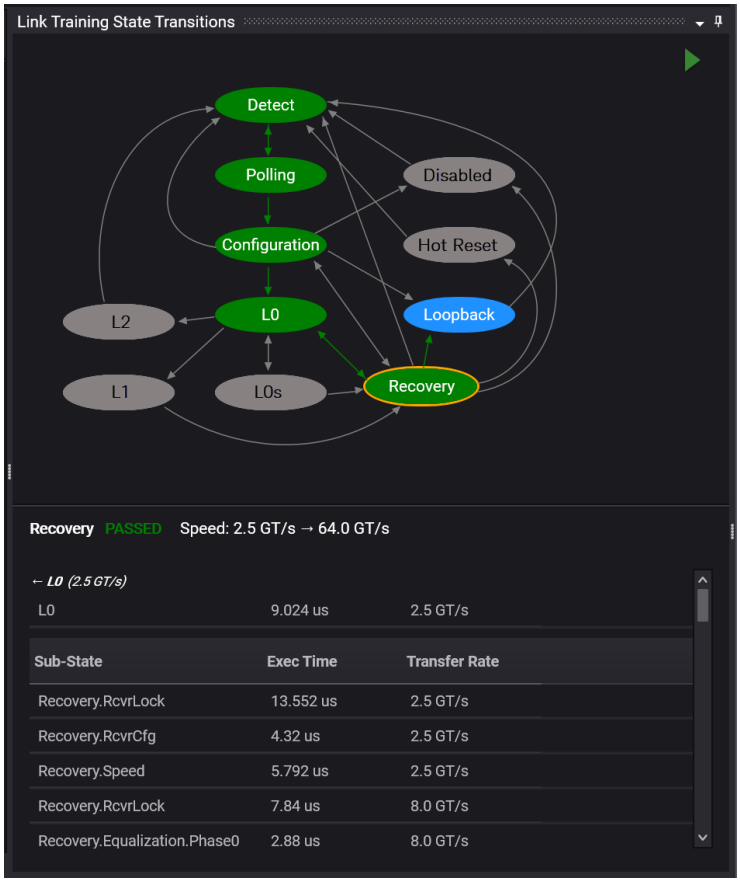
Link Training State Transitions

Link Training State Transitions window displays a bubble diagram representing the PCIe LTSSM flow. This diagram provides a graphical visualization of LTSSM logs, allowing you to quickly verify whether link training was successful or failed without manually analyzing lengthy log files.

Each LTSSM state in the bubble diagram is color-coded based on its execution status. Typically, the green indicates the passed tests, while the red indicates the failed one. The blue indicates the last active LTSSM state. You can click on a particular state to view detailed information in a tabular format, including its sub-states, timeout values, and execution time at a specific data rate.

NOTE

The PCIe LTSSM View in the M8000 Series BERT does not support the following states: L0s, L1, L2, Hot Reset, and Disabled. These unsupported states are displayed in gray in the bubble diagram



The Link Training State Transitions window also provides a **Replay** button, which allows users to replay the complete link training flow step-by-step. Since LTSSM transitions occur very quickly, typically within milliseconds, the replay feature helps you to better understand how link training progressed and identify where the failures or retries occurred during the process.

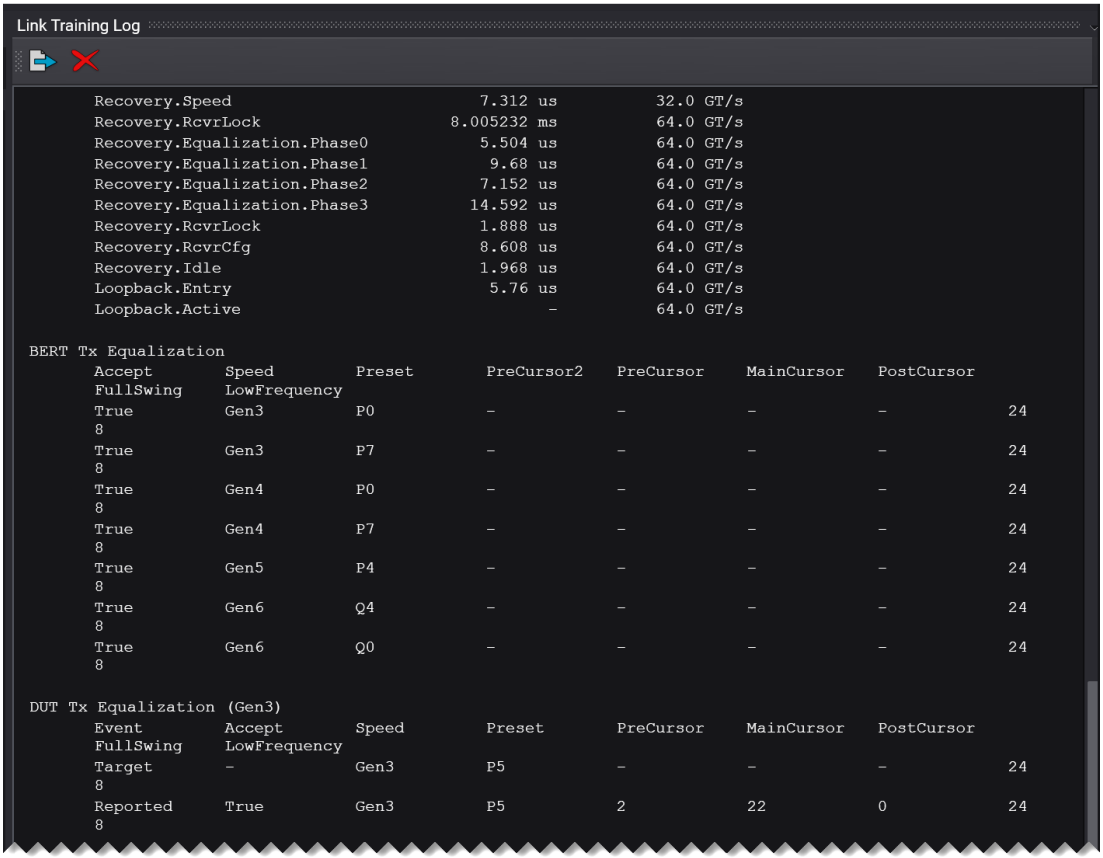
For detailed information on the Link Training States, see Interactive Link Training on page 698.

Link Training Log

The Link Training Log window displays the log generated while initiating the link training test. All information regarding the executed tests and their status is displayed with the date and time stamp. This helps to identify the root cause of a problem. For instance, the Link Training Log shows test failure due to an unexpected LTSSM state change.

The Link Training Log window provides the following options:

- **Export Log** - Click **Export Log** button to save the link training log to a desired location.
- **Clear Logs** - Click **Clear Logs** button to delete link training log.



Performing LTSSM using PCIe LTSSM View

This section describes the steps to perform Link Training and Status State Machine (LTSSM) using the PCIe LTSSM View. As explained earlier, the link training can also be performed using the M8070B (See Interactive Link Training on page 698), however, using PCIe LTSSM View reduces the configuration steps and makes the process faster.

NOTE The PCIe LTSSM View is currently supported for PCIe protocol only.

Steps:

1. Launch the M8070B software.
2. Connect to the required hardware modules and verify that all instruments are detected.
3. Open the **PCIe LTSSM View** from the M8070B application.
4. Configure the basic link settings:
   - PHY Protocol
   - DUT Type
   - Loopback Through
   - Compliance Receive Bit
5. Configure the **Generator** and **Analyzer** settings:
   - Frequency
   - Clock settings
   - Preset values
   - Equalization settings (if required)
6. Select the required LTSSM test scenario or state sequence.
7. Apply or save the configuration.
8. Click **Break** in the **PCIe LTSSM View** toolbar to initiate the link training process.
9. Monitor:
   - LTSSM state transitions
   - Link status
   - Pass/Fail results
   - Error counters and logs
10. After the LTSSM is completed, review the results and save the report if needed.

Controlling M8194A, M8195A, and M8196A AWG(s) from M8070B User Interface

The M8070B system software allows you to control AWGs (M8194A, M8195A, and M8196A) along with the M8020A/M8040A modules. Once the M8194A/M8195A/M8196A AWG module is installed into an AXIe chassis, it can be accessed via the M8070B software. Ensure that you have latest version of M8070B software installed in your system.

To access M8194A, you should have the latest version of M8070B (7.0 or above) and M8194A (Rev 1.2.5.0 or above)

To access M8196A, you should have the specific version of M8070B (3.4 or above) and M8196A SFP (Rev 2.0.2.0 or above).

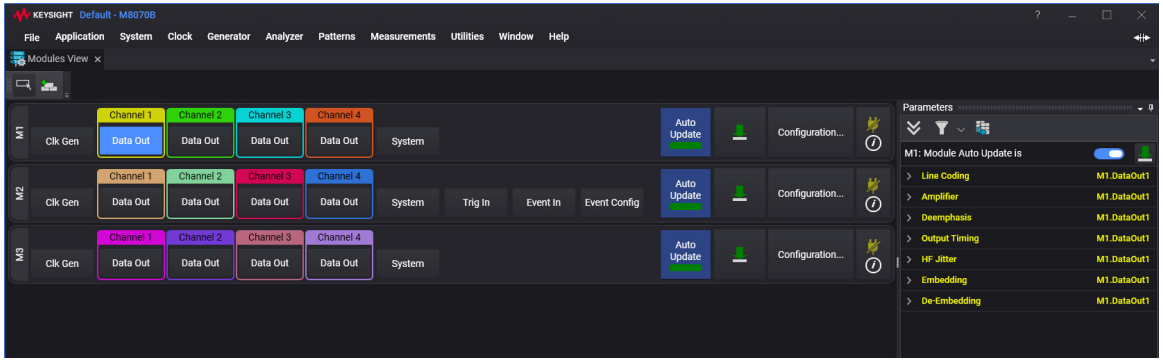
For complete details on M8194A Arbitrary Waveform Generator, visit www.keysight.com/find/m8194A.

For complete details on M8195A Arbitrary Waveform Generator, visit www.keysight.com/find/m8195A.

For complete details on M8196A Arbitrary Waveform Generator, visit www.keysight.com/find/m8196A.

AWG(s) in Module View

Once the AWG integration is done, you will see an AWG module entry in the **Module View**. The following figure shows the **Module View** of M8194A/M8195A/M8196A AWG:

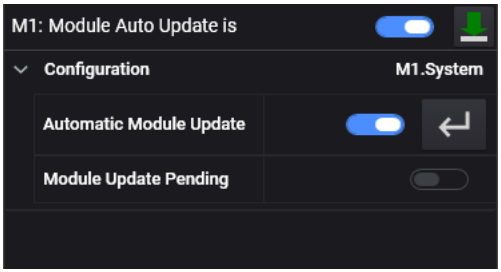


Automatic Module Update in AWG(s)

The **Automatic Module Update** feature enables you to turn the automatic module updates ON or OFF. This feature is available on the right-side of the module or under the **System** parameters.

The following parameters are available for **System**:

- **Configuration**: The Configuration function has the following components:



  - **Automatic Module Update**: Enables or disables the automatic module updates. The same can be done by clicking the **Auto Update** button present on the Module View of AWG module.

    When the **Automatic Module Update** parameter is enabled, the modules state updates automatically, whenever a property is changed.

    When the **Automatic Module Update** parameter is disabled, the time intensive operation's execution defers for parameter changes. Depending on the module type, this may disable some or all the property updates. Additionally, it can also disable the dynamic parameter limit calculations, which can trigger the **Auto Correct Confirmation** dialog when the module updates.
  - **Module Update Pending**: Applies the currently configured software state into module. This can also be done using the **Apply** button next to the Automatic Module Update ON/OFF toggle button. The same can be done by clicking the **Apply** button present on the Module View of AWG module. The orange **Apply** button indicates that the module update is pending.

NOTE

This parameter cannot be changed directly. When the Automatic Module Update parameter is enabled, the Module Update Pending parameter changes to OFF automatically.

NOTE

The module update pending indication will not detect the changes done to (externally) referenced files or when bypassing the user interface. An example of this effect is a pattern file which is edited while being referenced by a sequence bound to the concerned module. Another example is a selected S-Parameter file which is modified directly on the file system.

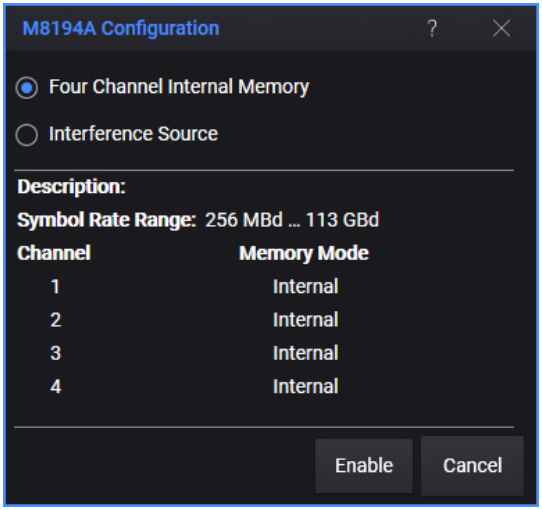
To update the module in these cases, it is necessary to perform a full module update by triggering the module update command.

M819xA Configuration

This section describes the steps to configure M8194A, M8195A, and M8196A AWGs.

M8194A Configuration

1 Click the **Configuration...** button. Depending upon the available channels in M8194A, the **M8194A Configuration** dialog will appear. The following figure shows the **M8194A Configuration** dialog when four channels in M8194A are available:



2 Click on the radio button to select the memory mode. The following modes are available:

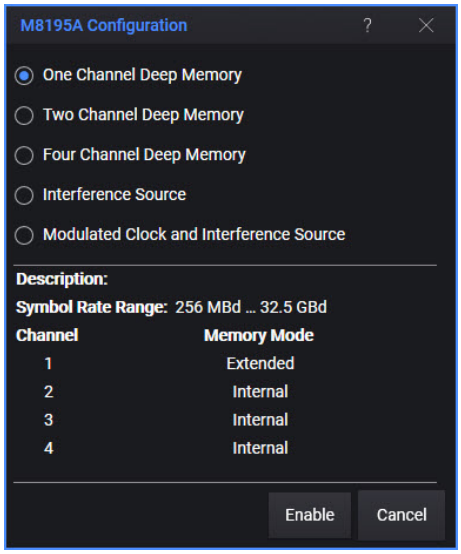
- **Four Channels Deep Memory**: The Data Out locations of all four channels will be sourced from extended memory. The data range in this mode is 256 MBd ... 113 GBd.
- **Interference Source**: The Data Out locations of all channels are used to generate interference (Sinusoidal Interference and/or Random Interference).

3 Click **Enable**.

M8195A Configuration

NOTE M8195A Configuration option is not available for M8195A (Rev 1).

1 Click the **Configuration...** button. Depending upon the available channels in M8195A, the **M8195A Configuration** dialog will appear. The following figure shows the **M8195A Configuration** dialog when four channels in M8195A are available:



2 Click on the radio button to select the memory mode. The following modes are available:

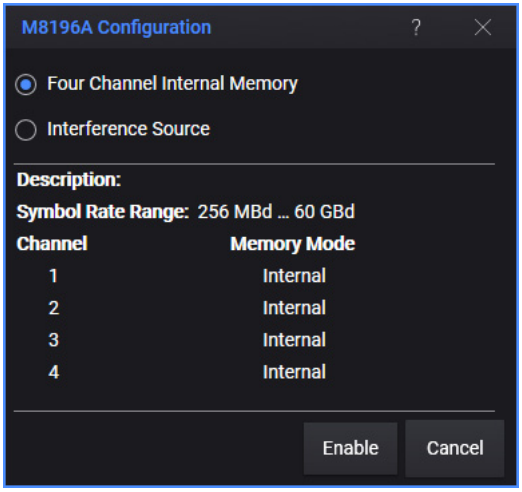
- **One Channel Deep Memory**: The Data Out location of one channel will be sourced from extended memory and the other channels will be sourced from module internal memory. The data range in this mode is 256 Mb/s ... 65 Gb/s.
- **Two Channels Deep Memory**: The Data Out locations of two channels will be sourced from extended memory and the other channels will be sourced from module internal memory. The data range in this mode is 256 Mb/s ... 32.5 Gb/s.

- **Four Channels Deep Memory**: The Data Out locations of all four channels will be sourced from extended memory. The data range in this mode is 256 Mb/s ... 16.250 Gb/s.
- **Interference Source**: The Data Out locations of all channels are used to generate interference (Sinusoidal Interference and/or Random Interference).
- **Modulated Clock and Interference Source**: Channels are used to generate modulated clock and interference source.

3 Click **Enable**.

M8196A Configuration

1 Click the **Configuration...** button. Depending upon the available channels in M8196A, the **M8196A Configuration** dialog will appear. The following figure shows the **M8196A Configuration** dialog when four channels in M8196A are available:



2 Click on the radio button to select the memory mode. The following modes are available:

- **Four Channels Deep Memory**: The Data Out locations of all four channels will be sourced from extended memory. The data range in this mode is 256 Mb/s ... 60 Gb/s.
- **Interference Source**: The Data Out locations of all channels are used to generate interference (Sinusoidal Interference and/or Random Interference).

3 Click **Enable**.

Configuring AWG(s) Parameters

The M8194A/M8195A/M8196A AWG has the **Data Out** and **Clk Gen** ports. You can use the **Parameters** window to configure these ports.

- **Line Coding** - Sets the line coding as NRZ or PAM4.
- **Amplifier** - The **Amplifier** function has the following components:
  - **Output State** - Enables or disables the state of the output.
  - **Termination Voltage** - Sets the external termination voltage.
  - **Amplitude** - Sets the amplitude of the output signal.
  - **Offset** - Sets the offset voltage of output signal.
  - **High** - Sets the high voltage of output signal.
  - **Low** - Sets the low voltage of output signal.
  - **Pulse Shaping Filter** - Sets the filter type used on the waveform.

    For M8194A, the filter type choices are Gaussian, Raised Cosine, and Root Raised Cosine.

    For M8195A, this parameter is not available.

    For M8196A, the filter type choices are Gaussian and Raised Cosine.

    Depending upon the specific filter used, the waveform gets properties like transition time or roll-off factor.
  - **Roll-Off Factor** - Sets the roll-off factor for the raised cosine pulse shaping filter. This parameter is only available in M8194A and M8196A.
  - **Transition Time** - Sets the transition time (20%/80%) of data output signal. This parameter is only available when the option **Gaussian** is selected under the **Pule Shaping Filter**.
  - **Crossover** - Sets the data's crossover percentage.
  - **Fast Amplitude Change** – Enables or disables the amplitude change without waveform recalculation and download. This option can be enabled for new optimization and can be disabled to have existing programs behave exactly as now. You can use the download waveform option to download the waveform at any time.

    This option is applicable when:
    - Amplitude is above 80mV
    - If only one of the interference sources (RI, SI1 or SI2) is enabled

If more than one interference sources (RI, SI1 and SI2) are enabled, the waveform re-calculation is necessary and waveform needs to be re-downloaded on changing the amplitude. Because of this 'Fast Amplitude Change' is not used if more than one sources are enabled.

This option is available only when the '**Interference Source**' or '**Modulated Clock and Interference Source**' options are selected in the **Configuration** dialog box. For more information, refer to M819xA Configuration on page 261.

- **Deemphasis** - Sets the deemphasis values in terms of coefficient values. The number of pre and post cursor depends on the BERT model. For details, see Deemphasis Signal Generator on page 380.
- **Output Timing** - Sets the delay of the output data signal.
- **HF Jitter**- Enables and sets the high frequency jitter.
- **Embedding** - Sets the S-Parameter for embedding.
- **De embedding** - The **De embedding** function has the following components:
  - **Channel Specific** - Applies channel specific correction of the amplitude and phase using an internal calibration.
  - **Standard Cable** - Defines whether the signal should be pre-distorted considering the properties of the standard cable set.
  - **S-Parameter State** - Enables/Disables S-Parameter compensation.
  - **S-Parameter Profile** - Selects the S-Parameter profile. It also allows you to import and export a S-Parameter profile.
  - **S-Parameter Output Port** - Selects the output port in S-Parameter profile.
  - **S-Parameter Input Port** - Selects the input port in S-Parameter profile.
- **Clk Gen -** The **Clk Gen** port has the following components:
  - **Synthesizer** - Used to set data rate frequency and period.
  - **SSC** - Controls the state of the SSC jitter source.
- **Channel Configuration** - The **Channel Configuration** function has the following components:
  - **Channel Coupling** – The channel coupling provides the flexibility to couple the two channels. Depending upon the availability of channels in a module, the channels can be coupled in the following ways:
    - **Four channel Module**: Channels 1/2 and Channels 3/4
    - **Two Channel Module**: Channels 1/4

Use the drop-down option to select the channels. For example, selecting “1/2” will couple channels 1 and 2. Once the channels are coupled, the parameters values will be identical across both channels.

Select “**None**”, if channel coupling is not required.

Physical connection changes are required for the channels to be coupled. Ensure to terminate the unused output ports with 50 Ohms.

- **Random Interference**: The **Random Interference** function has the following components:
  - **RI State**: Enables or disables Random Interference.
  - **RI Mode**: Sets the mode of the output signal. The available options are:
    - **Common Mode** – In this case, Common Mode Random Interference will be generated using non-inverted port of coupled channels.
    - **Differential Mode** – In this case, Differential Mode Random Interference will be generated using non-inverted port of coupled channels.
  - **RI Amplitude (RMS)**: Sets the amplitude of the output signal for random interference in Vrms.

    Note that the value of RI Amplitude will also reflect in the Amplitude parameter of the Amplifier functional block. The total amplitude across all enabled states [RI (p-p), SI1 (p-p), SI2 (p-p)] must be between 0 to 995 mV.

    The RI Amplitude V (p-p) will change when changing RI amplitude (Vrms) or the crest factor change (Vpp = CF(linear)*Vrms).
  - **Crest Factor unit**: Used to set the random interference crest factor unit type. Following unit types are allowed:
    - **Linear**: This is the default setting. Select this unit to specify the crest factor as voltage ratio.
    - **Logarithmic**: Select this unit to specify the crest factor in dB.
  - **RI Crest Factor**: Used to set the random interference crest factor value in dB or as voltage ratio depending on the currently selected crest factor unit type. This is defined as peak value.
  - **RI Highest Frequency**: Used to set the random interference high frequency in Hz.
  - **RI Lowest Frequency**: Used to set the random interference low frequency in Hz.

- **Sinusoidal Interference**: The Sinusoidal Interference function has the following components:
  - **SI State (1/2)**: Enables or disables Sinusoidal Interference. The available options are:
  - **SI Mode (1/2)**: Sets the tone mode of the output signal. The available options are:
    - **Common Mode** – In this case, Common Mode Sinusoidal Interference will be generated using non-inverted port of coupled channels.
    - **Differential Mode** – In this case, Differential Mode Sinusoidal Interference will be generated using non-inverted port of coupled channels.
  - **SI Frequency (1/2)**: Sets the frequency of the output signal for tone mode.

NOTE

The Frequency option is obsolete now. The SI1 Frequency acts as Frequency (old) when SI2 state is disabled.

When the SI1 State option is enabled, and the SI2 State option is disabled, then the following frequency ranges are applicable for SI1 Frequency:

- For M8194A - 160KHz to 45GHz
- For M8195A - 320KHz to 25 GHz
- For M8196A - 160KHz to 32 GHz

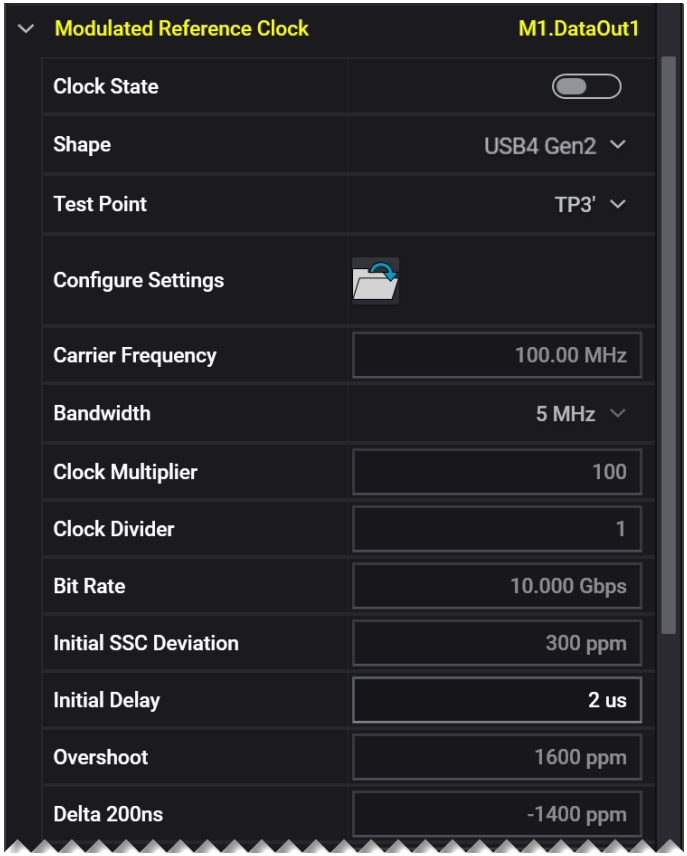
When both the SI1 Frequency and SI2 Frequency options are enabled, then the frequency range for the AWGs (M8194A, M8195A, and M8196A) is 1MHz to 12GHz. This is multi-tone behavior.

  - **SI Amplitude (1/2) (p-p)**: Sets the amplitude of the output signal for tone mode.
  - **SI Phase (1/2)**: Sets the phase of the output signal for tone mode.

Modulated Clock and Interference Clock for M8195A

For M8195A, channels are used to generate modulated clock and interference sources. When the Modulated Clock and Interference Clock mode is selected, AWG channel 1 and channel 2 will be used for the modulated reference clock. Channel 1 is used for the clock signal and channel 2 is used for pulse signal. The pulse signal is can be used for triggering the scope while advancing from one segment to another. Channel 3 and channel 4 will be used for RI and SI.

Channel 1 has the following components:



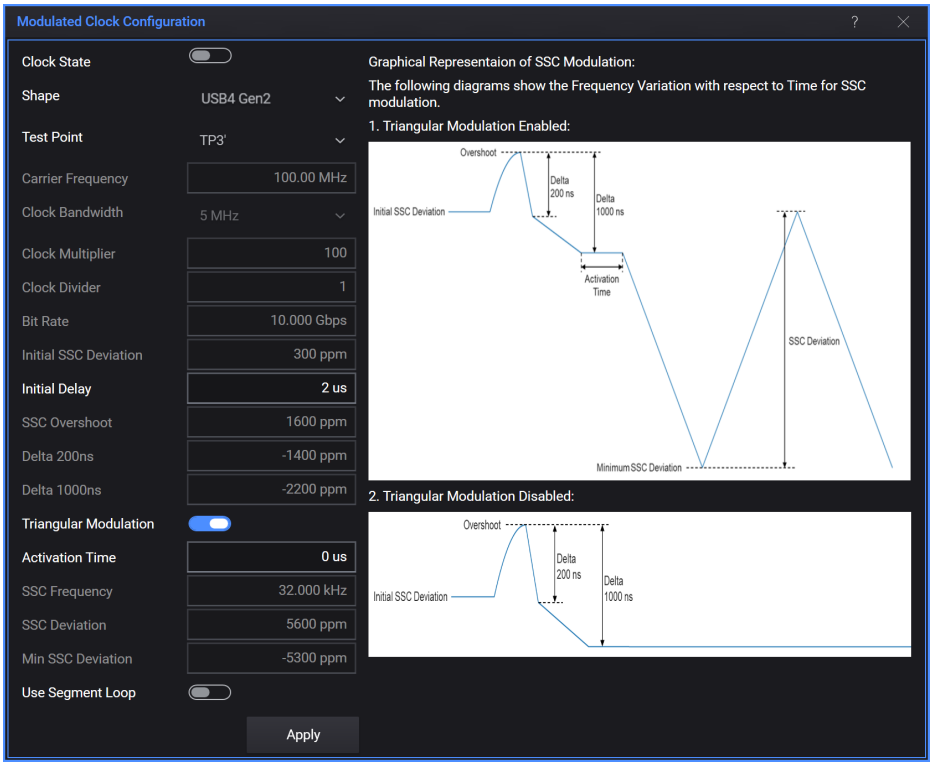
- **Channel Configuration**: Refer to Configuring AWG(s) Parameters Channel Configuration section.
- **Amplifier**: Refer to Configuring AWG(s) Parameters Amplifier section.

- **Modulated Reference Clock**: The **Modulated Reference Clock** function has the following parameters:
  - **Clock State**: Enables or disables the Modulated Reference Clock generation. Once the clock state is enabled, the first waveform segment will be played repeatedly.
  - **Shape**: Select the deviation shape to be used for the reference clock. The following options are available:
    - **USB4 Gen2, USB4 Gen3, USB4 Gen4, DP RBR, DP HBR, DP HBR2, DP HBR3, DP UHBR10, DP UHBR13.5 and DP UHBR20**: Select the shape to be used for modulated reference clock. USB4 Gen2 is the default option.
    - **User Defined**: This option allows editing the clock parameters. Use this option to specify user-defined values for the clock parameters.
    - **Custom**: This option allows using custom deviation files for each waveform segment. The maximum allowed segment count is 4.
  - **Test Point**: Select the test point at the receiver. The option is available for USB4 Gen2, USB4 Gen3, USB4 Gen4, DP UHBR10, DP UHBR13.5, DP UHBR20 and TBT3 shapes only. This affects the Overshoot value only, as shown below, and all other parameters remain the same.

Test Point	Overshoot
TP3’	1600 ppm
TP3	1400 ppm

  - **Configure Settings**: This option opens the **Modulated Clock Configuration** dialog which allows to configure all the modulated clock parameters.

    The following figure show the **Modulated Clock Configuration** dialog for 'User Defined' shape:



In 'User Defined' mode it is possible to configure all the modulated clock parameters and the synthesizer parameters. For USB4 Gen2, USB4 Gen3, USB4 Gen4, DP RBR, DP HBR, DP HBR2, DP HBR3, DP UHBR10, DP UHBR13.5 and DP UHBR20 shapes specifications the synthesizer and modulated clock the parameters are not configurable except for “Triangular Modulation”, “Activation Time” and “Use Segment Loop” parameters. The clock multiplier and clock divider values for the synthesizer are automatically adjusted based on the bit rate. User can configure all the parameters without downloading the waveform. Once the settings are adjusted, user can click ‘**Apply**’ button on the **Modulated Clock Configuration** dialog to download the waveform.

- **Carrier Frequency**: Carrier frequency of the modulated reference
  SSC Frequency: SSC frequency of the modulated reference clock in Hz
- **SSC Deviation**: SSC frequency deviation in ppm.

- **Minimum SSC Deviation**: The minimum SSC frequency deviation in ppm.
- **Initial SSC Deviation**: Initial non-modulated SSC frequency deviation in ppm.
- **Initial Delay** - Initial delay for the clock switch segment. This parameter is available for DP/USB and 'User Defined' shapes. It is not be available for 'Custom' shape specification.
- **Overshoot**: The maximum frequency deviation offset in ppm.
- **Delta 200ns**: Frequency deviation over 200 ns measurement window. This corresponds to the first straight slope after the overshoot. Delta is measured from the overshoot peak.
- **Delta 1000ns**: Frequency deviation over 1000 ns measurement window. This corresponds to the second straight slope after the overshoot. Delta is measured from the overshoot peak.
- **Triangular Modulation**: Enables or disables the triangular SSC modulation after the clock switch.
- **Activation Time**: Option for adjusting time before enabling the triangular SSC modulation.
- **Segment Loop**: Enable or disable the segment loop.
- **Segment No.** - Display the segment number of the current modulated clock.
- **Force Event**: Force event to advance from first segment to the next segment or to reset the sequence.
- **Restart** - Restarts the modulated clock sequence and start playing the first segment.

For USB4 Gen2, USB4 Gen2, USB4 Gen2, DP RBR, DP HBR, DP HBR2, DP HBR3, DP UHBR10, DP UHBR13.5 and DPUHBR 20, TBT3, and User Defined shapes, the waveform sequence contains 3 entries corresponding to 3 segments. The waveforms for different segments are as follows:

- **Segment 1**: Flat at the transient start. It plays a fixed sample. This segment is played continuously until 'Force Event' is clicked.
- **Segment 2**: The deviated spread spectrum signal interpolated to AWG sample rate. This is the transient segment and played only once.
- **Segment 3**: The triangular waveform. This segment is played continuously until 'Force Event' is clicked.

When the Clock State is enabled, the first segment will be played continuously until the Force Event button is clicked. The second segment is played once. The last segment is played continuously until reset with 'Force Event'.

The following table shows the waveforms for different segments for channel 1 and 2:

Waveform Segment	1	2	3
CH1 (modulated ref clk)	Constant frequency	Steep clock transient (segment starts flat)	Periodic triangles
CH2 (helper signal)	Off (0V)	On (High)	Off (0V)
Loop condition	Infinite Break with Force Event	Once	Infinite Break with Force Event

The parameter values for USB4 Gen2, USB4 Gen3, USB4 Gen4, DP RBR, DP HBR, DP HBR2, DP HBR3, DP UHBR10, DP UHBR13.5 and DP UHBR20 shapes are shown in the table below:

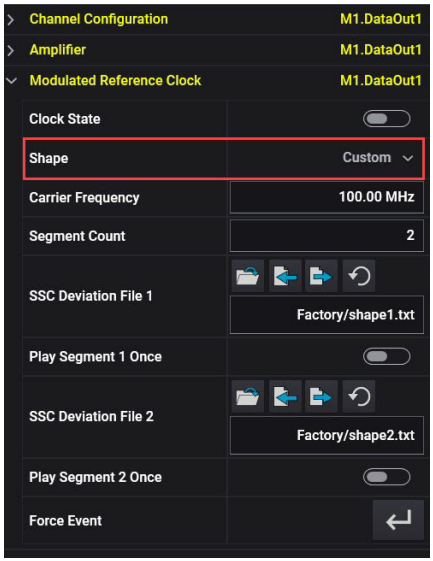
Specification	USB4 Gen2	USB4 Gen3	USB4 Gen4	DP RBR	DP HBR	DP HBR2	DP HBR3	DP UHBR10	DP UHBR13.5	DP UHBR20
Carrier frequency [MHz}	100	100	100	101.25	90	100	101.25	100	100	100
Bitrate [Gbps]	10	20	20	1.62	2.7	5.4	8.1	10	13.5	20
SSC Frequency [kHz]	32	32	32	32	32	32	32	32	32	32
SSC Deviation [ppm]	5600	5600	5600	5600	5600	5600	5600	5600	5600	5600
Minimum SSC Deviation [ppm]	-5300	-5300	-5300	-5300	-5300	-5300	-5300	-5300	-5300	-5300k
Initial SSC Deviation [ppm]	300	300	300	300	300	300	300	300	300	300
Overshoot [ppm]	1600 (TP3') 1400 (TP3)	1600 (TP3') 1400 (TP3)	1600 (TP3') 1400 (TP3)	1804	2452	1836	2250	1600 (TP3') 1400 (TP3)	1600 (TP3') 1400 (TP3)	1600 (TP3') 1400 (TP3)
Delta 200ns [ppm]	-1400	-1400	-1400	-2360	-3592	-2022	-2422	-1400	-1400	-1400
Delta 1000ns [ppm]	-2200	-2200	-2200	-3450	-4745	-3513	-4341	-2200	-2200	-2200

The parameters for 'Custom' shape are as follows:

- **Carrier Frequency**: Carrier frequency of the modulated reference clock.
- **Segment Count**: Set the number of segments. You can set a maximum of four segments.

- **SSC Deviation File1..4**: Select the deviation file for the segment. Each segment is defined in a text file with deviation in ppm, (e.g., shape1.txt, shape2.txt, shape3.txt, and shape4.txt) stored under "\Documents\Keysight\M8070B\Workspaces\Default\Factory\SharedResources\ModulatedClockDeviations" directory.

  You can select the deviation files for each segment and import, export, and reset the deviation file.
- **Play Segment (1..4) Once**: This parameter is available for each segment. It is used to select if the segment should be played only once. By default, the segments are played continuously until 'Force Event button is clicked to advance to the next segment.



Channel 2 has the following components:

- **Channel Configuration**: Refer to Configuring AWG(s) Parameters Channel Configuration section.
- **Amplifier**: Refer to Configuring AWG(s) Parameters Amplifier section.

Channel 3 and channel 4 has the following components:

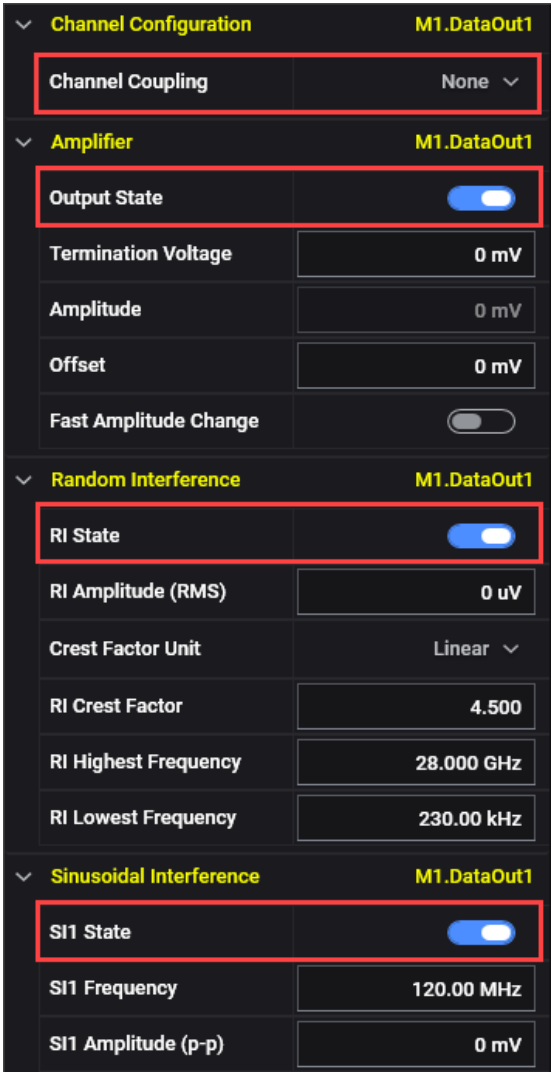
- Channel Configuration
- Amplifier
- Random Interference
- Sinusoidal Interference
- De-embedding

This is similar to RI/SI for memory configuration mode “Interference Source”. Refer to Configuring AWG(s) Parameters for more information.

Simultaneous Injection of RI and SI Using M819xA AWGs on Same Channel

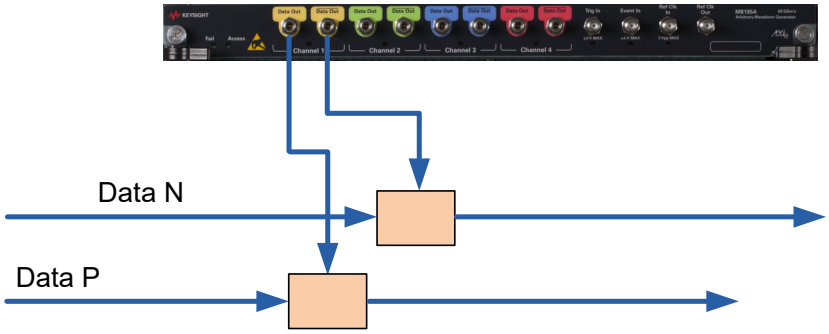
The M819xA AWG enables you to generate random interference (RI) and sinusoidal interference (SI) on the same channel. To select the Interference Source, refer to M819xA Configuration on page 261.

M819xA AWG RI and SI Parameters (Same Channel)



The following functional blocks are available in the **Parameter** Window to generate RI and SI.

- **Channel Configuration**: For generating RI and SI on same channel, select **None** from the **Channel Coupling** drop-down list.



For more information, refer to Configuring AWG(s) Parameters Channel Configuration section.

- **Amplifier** – This functional block has the following parameters:
  - **Output State** – For generating RI and SI on same channel, the **Output State** option must be enabled.
  - **Termination Voltage** – Sets the external termination voltage.
  - **Amplitude** – This option is disabled. The value of the Amplitude option depends on the enabled states. The amplitude value can be calculated as the sum of RI Amplitude Vpp (RI Amplitude Vrms, CrestFactor), SI1 Amplitude, and SI2 Amplitude based on the states enabled.
  - **Offset** – Sets the offset of the output signal.
  - **Fast Amplitude Change** – Enables or disables the amplitude change without waveform recalculation and download. This option can be enabled for new optimization and can be disabled to have existing programs behave exactly as now. You can use the download waveform option to download the waveform at any time.

    This option is applicable when:

    - Amplitude is above 80mV.
    - If only one of the interference sources (RI, SI1 or SI2) is enabled.

- **Random Interference**: For generating RI and SI on the same channel, the following option must be configured under the Random Interference block:
  - **RI State**: The RI State option must be enabled.
  - **RI Amplitude (RMS)**: Sets the amplitude of the output signal for random interference in Vrms.

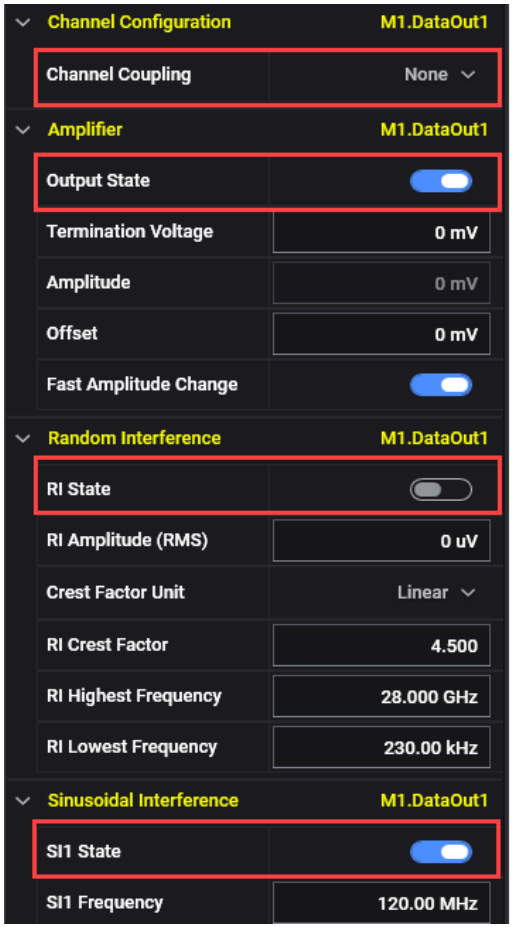
    Note that the value of RI Amplitude will also reflect in the Amplitude parameter of the Amplifier functional block. The total amplitude across all enabled states [RI (p-p), SI1 (p-p), SI2 (p-p)] must be between 0 to 995 mV.

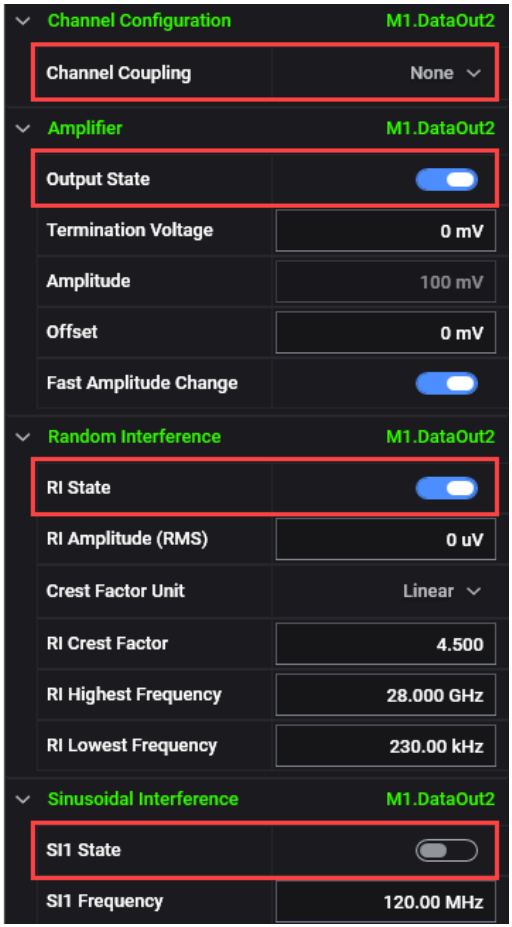
    The RI Amplitude V (p-p) will change when changing RI amplitude (Vrms) or the crest factor change (Vpp = CF(linear)*Vrms).
  - **Crest Factor unit**: Used to set the random interference crest factor unit type. Following unit types are allowed:
    - **Linear**: This is the default setting. Select this unit to specify the crest factor as voltage ratio.
    - **Logarithmic**: Select this unit to specify the crest factor in dB.
  - **RI Crest Factor**: Used to set the random interference crest factor value in dB or as voltage ratio depending on the currently selected crest factor unit type. This is defined as peak value.
  - **RI Highest Frequency**: Used to set the random interference high frequency in Hz.
  - **RI Lowest Frequency**: Used to set the random interference low frequency in Hz.
- **Sinusoidal Interference**: For generating RI and SI on the same channel, the following option must be configured under the Sinusoidal Interference block:
  - **SI State (1/2)**: The SI State (1/2) option must be enabled.
  - **SI Frequency (1/2)**: Sets the frequency of the output signal for tone mode.
  - **SI Amplitude (1/2) (p-p)**: Sets the amplitude of the output signal for tone mode.
  - **SI Phase (1/2)**: Sets the phase of the output signal for tone mode.
- **De-embedding** - Refer to Configuring AWG(s) Parameters De-embedding section.

Simultaneous Injection of RI and SI Using M819xA AWGs on Different Channels

The M819xA AWG enables you to generate random interference (RI) and sinusoidal interference (SI) on different channels simultaneously. To select the Interference Source, refer to M819xA Configuration on page 261.

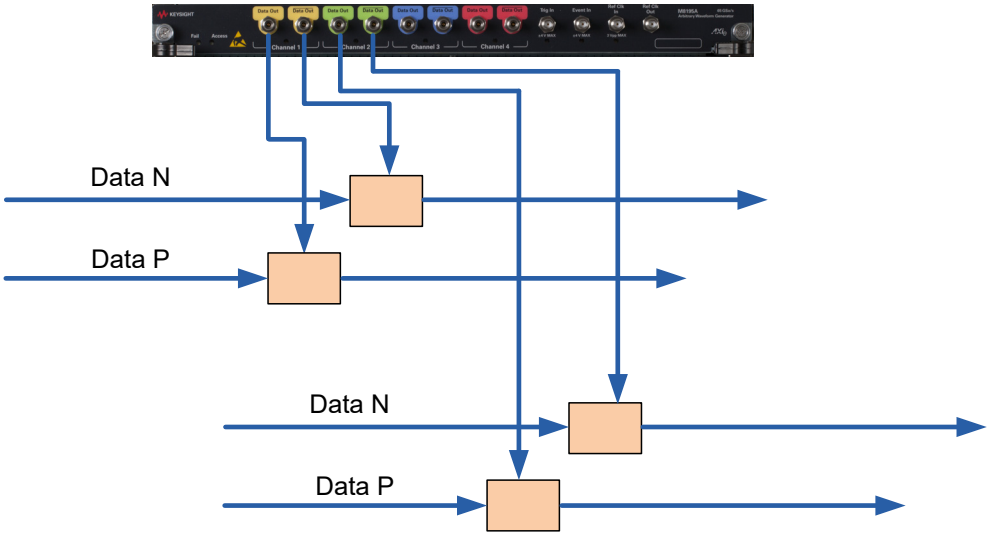
M819xA AWG RI and SI Parameters (Different Channels)





The following functional blocks are available in the **Parameter** Window to generate RI and SI.

- **Channel Configuration**: For generating RI and SI on different channels, select **None** from the **Channel Coupling** drop-down list.



For more information, refer to Configuring AWG(s) Parameters Channel Configuration section.

- **Amplifier**: For generating RI and SI on different channels, the **Output State** option must be enabled on both the channels. For more information, refer to M819xA AWG RI and SI Parameters (Same Channel) Amplifier section.
- **Random Interference**: For generating RI and SI on different channels, the following option must be configured under the Random Interference block of Channel1:
  - **RI State**: The RI State option must be enabled.

  For configuring the rest of the random interference options, refer to M819xA AWG RI and SI Parameters (Same Channel) Random Interference section.
- **Sinusoidal Interference**: For generating RI and SI on different channels, the following option must be configured under the Sinusoidal Interference block of Channel2:
  - **SI State (1/2)**: The SI State (1/2) option must be enabled.

For configuring the rest of the sinusoidal interference options, refer to M819xA AWG RI and SI Parameters (Same Channel) Sinusoidal Interference section.

NOTE **For generating RI and SI on different channels, the RI state of one channel and the SI state of another channel must be enabled.**

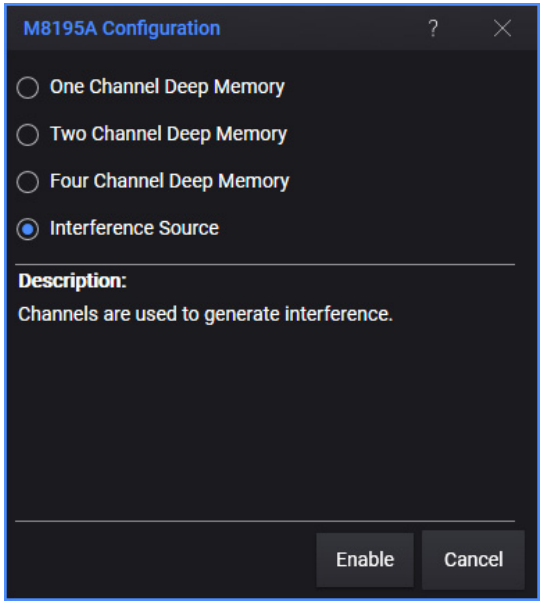
- **De-Embedding** - Refer to Configuring AWG(s) Parameters De-Embedding section.

Simultaneous Injection of CMSI and DMSI Using M819xA AWGs

The channels of M819xA AWG can be coupled to generate common mode sinusoidal interference (CMSI) and differential mode sinusoidal interference (DMSI) on an output signal. CMSI/DMSI is an extension of existing interference source.

Follow the given steps to generate multi-tone CMSI/DMSI on the output signals:

1 In the M819xA **Configuration** dialog, select **Interference Source** and then click **Enable**.



For more information on **Configuration** dialog, see M819xA Configuration on page 261.

2 Set the parameters to generate multi-tone CMSI/DMSI. For details on parameters, see M819xA AWG CMSI and DMSI Parameters on page 281.

M819xA AWG CMSI and DMSI Parameters

The following functional blocks are available in the **Parameter Window** to generate CMSI and DMSI.

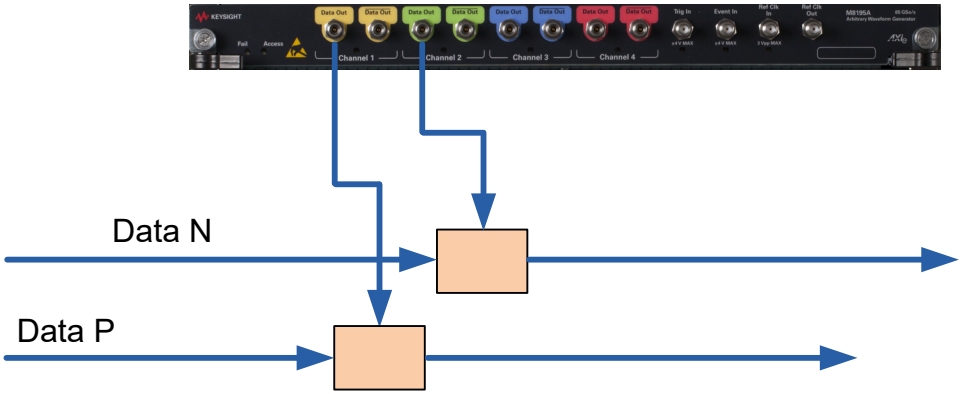
- **Channel Configuration**
  - **Channel Coupling** – The channel coupling provides the flexibility to couple the two channels. Depending upon the availability of channels in a module, the channels can be coupled in the following ways:
    - **Four channel Module**: Channels 1/2 and Channels 3/4

- **Two Channel Module**: Channels 1/4

Use the drop-down option to select the channels. For example, selecting “1/2” will couple channels 1 and 2. Once the channels are coupled, the parameters values will be identical across both channels.

Physical connection changes are required for the channels to be coupled. If two channels (Channel 1 and Channel 2) are coupled, then the differential pair cable must be connected to the non-inverted ports of channel 1 and channel 2. Ensure to terminate the unused output ports with 50 Ohms.

The following block digram provides an example how to cable the normal/complement outputs of AWG to couple channels 1 and 2:



Select “**None**”, if channel coupling is not required.

- **Amplifier** – This functional block has the following parameters:
  - **Output State** – Turns on/off the state of the output.
  - **Termination Voltage** – Sets the external termination voltage.
  - **Amplitude** – This option is disabled. The value of the Amplitude option depends on the enabled states. The amplitude value can be calculated as the sum of RI Amplitude Vpp (RI Amplitude Vrms, CrestFactor), SI1 Amplitude, and SI2 Amplitude based on the states enabled.
  - **Offset** – Sets the offset of the output signal.

- **Amplitude Correction Factor** – Sets the amplitude correction factor. The **Amplitude Correction Factor** parameter is not included in the coupling and so it can be set independently on each coupled channels.

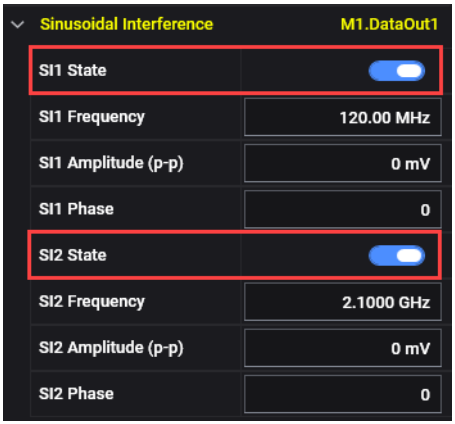
  The **Amplitude Correction Facto**r parameter enables you to correct the amplitude loss when channels are already coupled. The purpose of this parameter to increase/decrease the gain without changing the Amplitude parameter value. The amplitude correction factor follows the maximum limit of amplitude parameter.

  The amplitude correction factor parameter of a channel is not synced with the coupled channel. If two channels (Channel 1 and Channel 2) are coupled, and the amplitude correction factor is changed for channel 1, then it does not affect the value of channel 2.
- **Fast Amplitude Change** – Enables or disables the amplitude change without waveform recalculation and download. This option can be enabled for new optimization and can be disabled to have existing programs behave exactly as now. You can use the download waveform option to download the waveform at any time.

  This option is applicable when:
  - Amplitude is above 80mV.
  - If only one of the interference sources (RI, SI1 or SI2) is enabled.

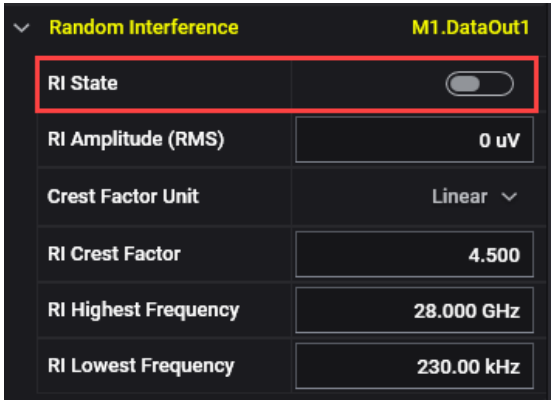
- **Sinusoidal Interference** – This functional block allows you to set State, Mode, Frequency, Amplitude and Phase for individual signal (1/2). It has the following parameters:
  - **SI State (1/2)**: Enables or disables Sinusoidal Interference.

NOTE The SI State (1/2) option must be enabled to generate CMSI and DMSI.



- **SI Mode (1/2)**: Sets the tone mode of the output signal. The available options are:
  - **Common Mode** – In this case, Common Mode Sinusoidal Interference will be generated using non-inverted port of coupled channels.
  - **Differential Mode** – In this case, Differential Mode Sinusoidal Interference will be generated using non-inverted port of coupled channels.
- **Amplitude (p-p) (1/2)**: Sets the amplitude of selected tone (1/2). Note that the value of **Amplitude 1** will also reflect in the **Amplitude** parameter of the **Amplifier** functional block. The total amplitude across both tones must be between 0 to 995 mV.
- **Frequency (1/2)**: Sets the frequency of the selected tone (1/2).
- **Phase (1/2)**: Sets the phase of the selected tone (1/2).

- **Random Interference**: To generate CMSI and DMSI only, disable the **RI State** option under the Random Interference block.



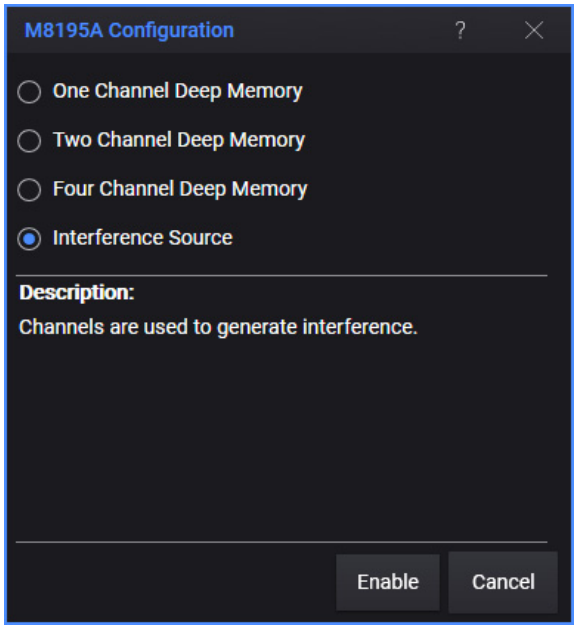
- **De-Embedding** - Refer to Configuring AWG(s) Parameters De-Embedding section.

Simultaneous Injection of CMRI or DMRI Using M819xA AWGs

The channels of M819xA AWG can be coupled to generate common mode random interference (CMRI) or differential mode random interference (DMRI) on an output signal. CMRI/DMRI is an extension of existing interference source.

Follow the given steps to generate CMRI/DMRI on the output signals:

1 On the right-side of the module, click **Configuration**.



2 In the M819xA **Configuration** dialog box, select **Interference Source**, and then click **Enable**.

3 Set the parameters to generate CMRI/DMRI. For details on parameters, see M819xA AWG CMRI/DMRI Parameters on page 287.

M819xA AWG CMRI/DMRI Parameters

The following functional blocks are available in the **Parameter Window** to generate CMRI or DMRI.

- **Channel Configuration**
  - **Channel Coupling** – The channel coupling provides the flexibility to couple the two channels. Depending upon the availability of channels in a module, the channels can be coupled in the following ways:
    - **Four channel Module**: Channels 1/2 and Channels 3/4
    - **Two Channel Module**: Channels 1/4

    Use the drop-down option to select the channels. For example, selecting “1/2” will couple channels 1 and 2. Once the channels are coupled, the parameters values will be identical across both channels.

    Select “**None**”, if channel coupling is not required.

    Physical connection changes are required for the channels to be coupled. Ensure to terminate the unused output ports with 50 Ohms.
- **Amplifier** – This functional block has the following parameters:
  - **Output State** – Enables or disables the state of the output.
  - **Termination Voltage** – Sets the termination voltage of the output signal.
  - **Amplitude** – This option is disabled. The value of the Amplitude option depends on the enabled states. The amplitude value can be calculated as the sum of RI Amplitude Vpp (RI Amplitude Vrms, CrestFactor), SI1 Amplitude, and SI2 Amplitude based on the states enabled.
  - **Offset** – Sets the offset voltage of the output signal.
  - **Amplitude Correction Factor** – Sets the amplitude correction factor. The **Amplitude Correction Factor** parameter is not included in the coupling and so it can be set independently on each coupled channels.

    The **Amplitude Correction Facto**r parameter enables you to correct the amplitude loss when channels are already coupled. The purpose of this parameter to increase/decrease the gain without changing the Amplitude parameter value. The amplitude correction factor follows the maximum limit of amplitude parameter.

The amplitude correction factor parameter of a channel is not synced with the coupled channel. If two channels (Channel 1 and Channel 2) are coupled, and the amplitude correction factor is changed for channel 1, then it does not affect the value of channel 2.

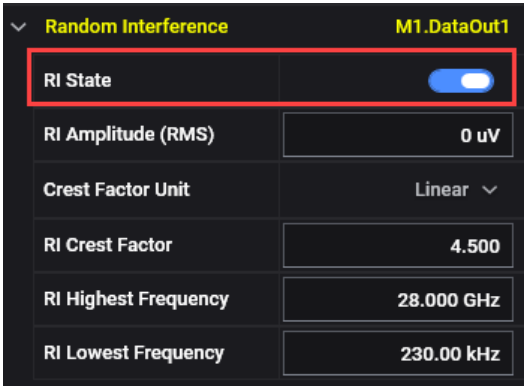
- **Fast Amplitude Change** – Enables or disables the amplitude change without waveform recalculation and download. This option can be enabled for new optimization and can be disabled to have existing programs behave exactly as now. You can use the download waveform option to download the waveform at any time.

  This option is applicable when:

  - Amplitude is above 80mV.
  - If only one of the interference sources (RI, SI1 or SI2) is enabled.

- **Random Interference -** The **Random Interference** function has the following components:
  - **RI State**: Enables or disables Random Interference.

NOTE The RI State option must be enabled to generate CMRI and DMRI.

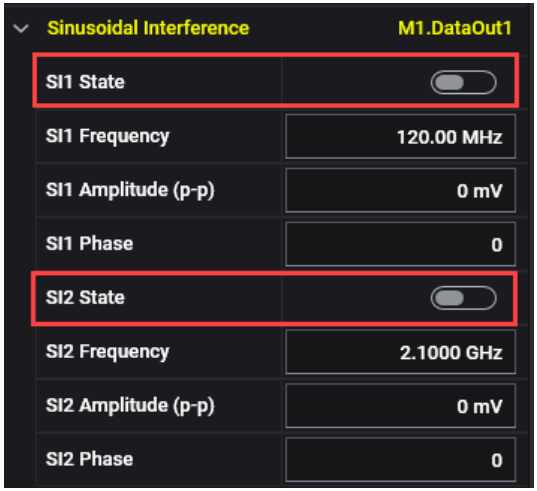


- **RI Mode**: Sets the mode of the output signal. The available options are:
  - **Common Mode** – In this case, Common Mode Random Interference will be generated using non-inverted port of coupled channels.
  - **Differential Mode** – In this case, Differential Mode Random Interference will be generated using non-inverted port of coupled channels.
- **RI Amplitude (RMS)**: Sets the amplitude of the output signal for random interference in Vrms.

  Note that the value of RI Amplitude will also reflect in the Amplitude parameter of the Amplifier functional block. The total amplitude across all enabled states [RI (p-p), SI1 (p-p), SI2 (p-p)] must be between 0 to 995 mV.

  The RI Amplitude V (p-p) will change when changing RI amplitude (Vrms) or the crest factor change (Vpp = CF(linear)*Vrms).
- **Crest Factor Unit** - Used to set the random interference crest factor unit type. Following unit types are allowed:
  - **Linear** - This is the default setting. Select this unit to specify the crest factor as voltage ratio.
  - **Logarithmic** - Select this unit to specify the crest factor in dB.
- **RI Crest Factor** - Used to set the random interference crest factor value in dB or as voltage ratio depending on the currently selected crest factor unit type. This is defined as peak value.
- **RI Highest Frequency** - Used to set the random interference high frequency in Hz.
- **RI Lowest Frequency** - Used to set the random interference low frequency in Hz.

- **Sinusoidal Interference**: To generate CMRI/DMRI only, disable the **SI State (1/2)** option under the Sinusoidal Interference block.



- **De-Embedding** - Refer to Configuring AWG(s) Parameters De-Embedding section.

Simultaneous Injection of CMRI with CMSI Using M819xA AWGs

The channels of M819xA AWG can be coupled to generate common mode random interference (CMRI) with common mode sinusoidal interference (CMSI) on an output signal. To select the Interference Source, refer to M819xA Configuration on page 261.

M819xA AWG CMRI with CMSI Parameters

The following functional blocks are available in the **Parameter Window** to generate CMRI with CMSI.

- **Channel Configuration**: For generating CMRI with CMSI, do not select "**None**" from the **Channel Coupling** drop-down list.

  For more information, refer to Configuring AWG(s) Parameters Channel Configuration section.
- **Amplifier**: Refer to M819xA AWG CMSI and DMSI Parameters Amplifier section.
- **Random Interference**: For generating CMRI with CMSI, the following options must be configured under the Random Interference block:
  - **RI State**: Enable the RI state option.
  - **RI Mode**: From the **RI Mode** drop-down list, select **Common Mode**.

  For configuring the rest of the random interference options, refer to M819xA AWG CMRI/DMRI Parameters Random Interference section.
- **Sinusoidal Interference**: For generating CMRI with CMSI, the following options must be configured under the Sinusoidal Interference block:
  - **SI State (1/2)**: Enable the SI state (1/2) option.
  - **SI Mode (1/2)**: From the **SI Mode (1/2)** drop-down list, select **Common Mode**.

  For configuring the rest of the sinusoidal interference options, refer to M819xA AWG CMSI and DMSI Parameters Sinusoidal Interference section.
- **De-Embedding** - Refer to Configuring AWG(s) Parameters De-Embedding section.

Simultaneous Injection of CMRI with DMSI Using M819xA AWGs

The channels of M819xA AWG can be coupled to generate common mode random interference (CMRI) with differential mode sinusoidal interference (DMSI) on an output signal. To select the Interference Source, refer to M819xA Configuration on page 261.

M819xA AWG CMRI with DMSI Parameters

The following functional blocks are available in the **Parameter Window** to generate CMRI with DMSI.

- **Channel Configuration**: For generating CMRI with DMSI, do not select "**None**" from the **Channel Coupling** drop-down list.

  For more information, refer to Configuring AWG(s) Parameters Channel Configuration section.
- **Amplifier**: Refer to M819xA AWG CMSI and DMSI Parameters Amplifier section.
- **Random Interference**: For generating CMRI with DMSI, the following options must be configured under the Random Interference block:
  - **RI State**: Enable the RI state option.
  - **RI Mode**: From the **RI Mode** drop-down list, select **Common Mode**.

  For configuring the rest of the random interference options, refer to M819xA AWG CMRI/DMRI Parameters Random Interference section.
- **Sinusoidal Interference**: For generating CMRI with DMSI, the following options must be configured under the Sinusoidal Interference block:
  - **SI State (1/2)**: Enable the SI state (1/2) option.
  - **SI Mode (1/2)**: From the **SI Mode (1/2)** drop-down list, select **Differential Mode**.

  For configuring the rest of the sinusoidal interference options, refer to M819xA AWG CMSI and DMSI Parameters Sinusoidal Interference section.
- **De-Embedding** - Refer to Configuring AWG(s) Parameters De-Embedding section.

Simultaneous Injection of DMRI with CMSI Using M819xA AWGs

The channels of M819xA AWG can be coupled to generate differential mode random interference (DMRI) with common mode sinusoidal interference (CMSI) on an output signal. To select the Interference Source, refer to M819xA Configuration on page 261.

M819xA AWG DMRI with CMSI Parameters

The following functional blocks are available in the **Parameter Window** to generate DMRI with CMSI.

- **Channel Configuration**: For generating DMRI with CMSI, do not select "**None**" from the **Channel Coupling** drop-down list.

  For more information, refer to Configuring AWG(s) Parameters Channel Configuration section.
- **Amplifier**: Refer to M819xA AWG CMSI and DMSI Parameters Amplifier section.
- **Random Interference**: For generating DMRI with CMSI, the following options must be configured under the Random Interference block:
  - **RI State**: Enable the RI state option.
  - **RI Mode**: From the **RI Mode** drop-down list, select **Differential Mode**.

  For configuring the rest of the random interference options, refer to M819xA AWG CMRI/DMRI Parameters Random Interference section.
- **Sinusoidal Interference**: For generating DMRI with CMSI, the following options must be configured under the Sinusoidal Interference block:
  - **SI State (1/2)**: Enable the SI state (1/2) option.
  - **SI Mode (1/2)**: From the **SI Mode (1/2)** drop-down list, select **Common Mode**.

  For configuring the rest of the sinusoidal interference options, refer to M819xA AWG CMSI and DMSI Parameters Sinusoidal Interference section.
- **De-Embedding** - Refer to Configuring AWG(s) Parameters De-Embedding section.

Simultaneous Injection of DMRI with DMSI Using M819xA AWGs

The channels of M819xA AWG can be coupled to generate differential mode random interference (DMRI) with differential mode sinusoidal interference (DMSI) on an output signal. To select the Interference Source, refer to M819xA Configuration on page 261.

M819xA AWG DMRI with DMSI Parameters

The following functional blocks are available in the **Parameter Window** to generate DMRI with DMSI.

- **Channel Configuration**: For generating DMRI with DMSI, do not select "**None**" from the **Channel Coupling** drop-down list.

  For more information, refer to Configuring AWG(s) Parameters Channel Configuration section.
- **Amplifier**: Refer to M819xA AWG CMSI and DMSI Parameters Amplifier section.
- **Random Interference**: For generating DMRI with DMSI, the following options must be configured under the Random Interference block:
  - **RI State**: Enable the RI state option.
  - **RI Mode**: From the **RI Mode** drop-down list, select **Differential Mode**.

  For configuring the rest of the random interference options, refer to M819xA AWG CMRI/DMRI Parameters Random Interference section.
- **Sinusoidal Interference**: For generating DMRI with DMSI, the following options must be configured under the Sinusoidal Interference block:
  - **SI State (1/2)**: Enable the SI state (1/2) option.
  - **SI Mode (1/2)**: From the **SI Mode (1/2)** drop-down list, select **Differential Mode**.

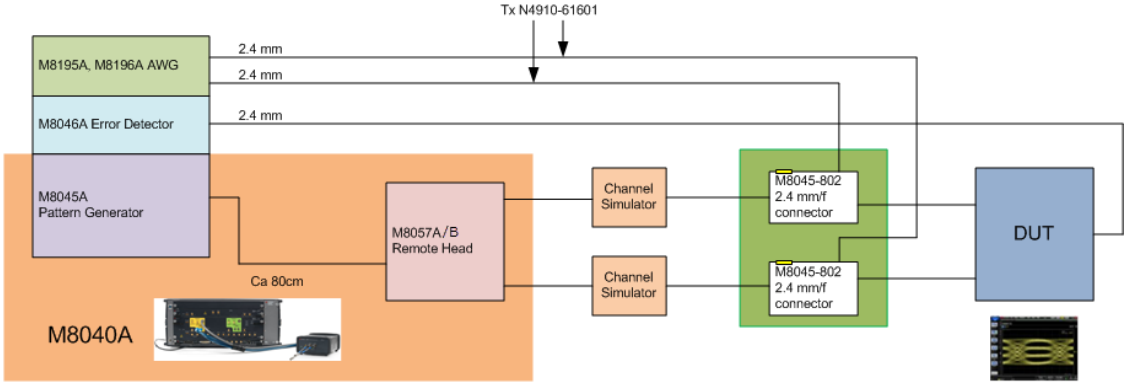
  For configuring the rest of the sinusoidal interference options, refer to M819xA AWG CMSI and DMSI Parameters Sinusoidal Interference section.
- **De-Embedding** - Refer to Configuring AWG(s) Parameters De-Embedding section.

AWG as External Level Interference (RI/SI) Source

The Keysight M8194A, M8195A, and M8196A AWG can be used as external level interference source with sinusoidal and random modulation. For this you need to select '**Interference Source**' from the M8194A, M8195A, and M8196A configuration dialog. For more details on the M8194A, M8195A, and M8196A configuration dialog, refer to M8194A Configuration on page 261, M8195A Configuration on page 262, and M8196A Configuration on page 263. The M8070B system software allows controlling interference parameters such as amplitude, highest frequency, lowest frequency and crest factor. Keysight provides a matched directional coupler pair (orderable option M8045-802) for injecting the RI or SI signal before or after the channel. Specifications for external level interference sources RI/SI with M8194A, M8195A, and M8196A can be found in M8040A data sheet.

The following block diagram shows the recommended RX test setup with Interference Source (M8194A/M8195A/M8196A):

Block Diagram for RX Test Setup with RI/SI Source



System View with AWG(s) Integration

This section describes the block diagram provided by the **System View** when AWG module is integrated in M8070B. The **System View** for AWG varies on the number of channels available on M8194A, M8195A, or M8196A.

The following figure shows **System View** of M8194A/M8195A/M8196A when all four channels are available.

The **System View** of AWG shows four Data Out channels in the same window. The principal parts of the **System View** are represented by blocks which are connected by lines/arrows to show the relationship of the blocks. These blocks are highlighted by blue lines around the block on mouse focus. On clicking these blocks, the mostly used parameters are available which can be configured using the on-screen numeric keypad. However, parameters corresponding to the selected block are displayed in

the **Parameters** window, on the right. The block may contain feature elements (for example, HF Jitter contains PJ1, PJ2 and RJ). You can click on the respective button to enable the feature elements. Once enabled, the feature elements are highlighted in blue color. For more details, refer to System View on page 209.

Signal Generation in AWG

For detailed information about signal generation on arbitrary waveform generators of the M81XX class can be found in the document named "Fundamentals of Arbitrary Waveform Generation" which can be downloaded from here: www.keysight.com/find/awg-apps

Using AWG Frequency Response Calibration for Improved Signal Performance

Keysight recommends performing signal calibration within the AWG system (M8194A/M8195A/M8196A) for DUT testing.

In other words, the specific channel of the AWG must be calibrated with specific cables and connectors that are used between the AWGs DATA OUT and the DUTs RX port.

To perform the phase/frequency response calibration, you require a DCA-X and DCA-M sampling scope with a receiver module above 30 GHz. Alternatively, you may use a DSA-Z series real-time scope, which is capable of signal analysis above 30 GHz. Generally, a better signal quality is achieved when this calibration is performed using a sampling scope as compared to the calibration performed using a real-time scope.

A S-Parameter file is generated as a result of performing this calibration using IQTools, which can be imported as a De-Embedding filter into the M8070B software. For details on how to perform these steps, refer to *IQToolsPhaseFrequencyResponseCalibration.pdf*, which is available within the M8070B documentation folder.

M8194A amplitude behavior using (de-)embedding

When using M8194A with (de-)embedding, the effective amplitude of the output signal depends strongly on the frequency contents of the generated signal. The amplifier amplitude accessible in M8070B represents the value of the amplifier chip inside the module. The cables and connectors inside and outside of the module are ignored.

For the M8195A and M8196A integration, this frequency dependency is largely compensated by software algorithms. The amplifier amplitude in M8070B represents the value measurable at the calibration plane (when using (de-)embedding) after the cables and connectors inside and outside of the module.

This compensation is currently not done for M8194A and will, therefore, lead to the effective amplitude that can be measured and the amplifier amplitude set in M8070B to deviate. In extreme cases, the effective amplitude can be less than half of the specified amplitude.

For example, when using a raised cosine edge filter with a roll-off factor of 1.0, the slope of the edges in the serial data signal is very steep. Using some kind of de-embedding (e.g., using S-Parameter), the waveform is pre-distorted to look optimal at the measurement plane used for determining these de-embedding parameters.

When using IQTools with an oscilloscope to generate an S-Parameter calibration file, it includes the cables and connectors between the amplifier in the module and the oscilloscope's front panel.

The required pre-distortion leads to high-frequency content having to be present in the generated waveform at the generator side (the output amplifier of an M8194A channel). These high-frequency spectral parts will mostly not be visible at the receiving end because they are removed by a cable or connector, which is behaving as a low pass filter.

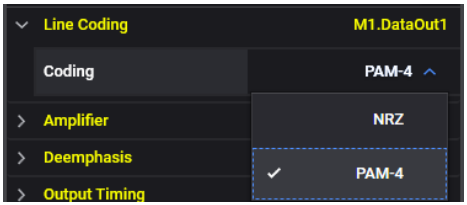
But these still (factors above the data rate) need to be present on the generator's amplifier to improve signal quality at the receiver side, so the effectively measurable amplitude differs from the amplitude required at the generator.

Now when reducing the roll-off factor of the raised cosine edge filter to 0.3, on the other hand, the signal bandwidth (high-frequency content) is reduced, and less pre-distortion is required. Therefore the effective amplitude at the receiver will deviate less strongly from the amplitude required at the amplifier inside the M8194A module.

In general, the more pre-distortion is necessary. Higher the required correction frequencies are, the more strongly the effectively measurable amplitude is reduced from the amplifier amplitude specified in M8070.

Selecting Line Coding

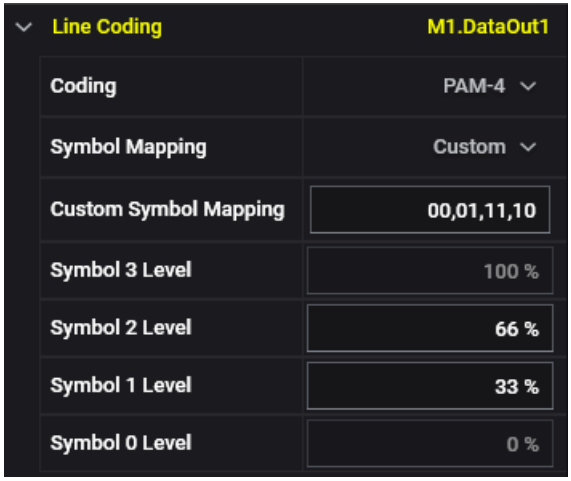
You can define the line coding for a M8194A/M8195A/M8196A **Data Out** port through the **Parameters** window. The M8194A/M8195A/M8196A **Data Out** port supports NRZ and PAM4 line coding.



NOTE

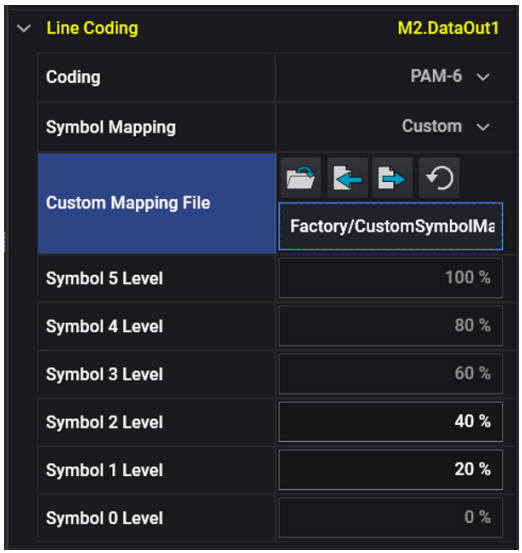
Make sure to use the similar line coding of all Data Out ports assigned to the same sequence of M8194A/M8195A/M8196A. An "Auto Correction" window will appear if you select different line coding. Clicking on the "Allow" button present on this window, applies the same line coding on all Data Out ports.

The **PAM4** line coding provides the symbol mapping options as shown in the following figure:



- **Uncoded** - In this mapping, the bit sequence 00 maps to symbol 0, 01 maps to symbol 1, 10 maps to symbol 2 and 11 maps to symbol 3.
- **Gray Coded** - In this mapping, the bit sequence 00 maps to symbol 0, 00 maps to symbol 0, 01 maps to symbol 1, 11 maps to symbol 2 and 10 maps to symbol 3.
- **Custom** - In this mapping the consecutive data bits are mapped to symbols. The mapping is defined as a comma separated list of bit sequences (e.g. 00, 01, 11, 10). The position within this list corresponds to the symbol level. First value is for Symbol 0 an the last value is for Symbol 3.
- **Symbol Level** - It controls the PAM4 level mappings. It can be used to adjust the actual output level that is being generated by a data output for a specific PAM4 symbol. The levels of PAM4 symbol 0 and 3 cannot be adjusted and are always kept at the value of 0% and 100% of the actual output voltage swing.

The **PAM6** and **PAM8** line coding provides the symbol mapping options as shown in the following figure:



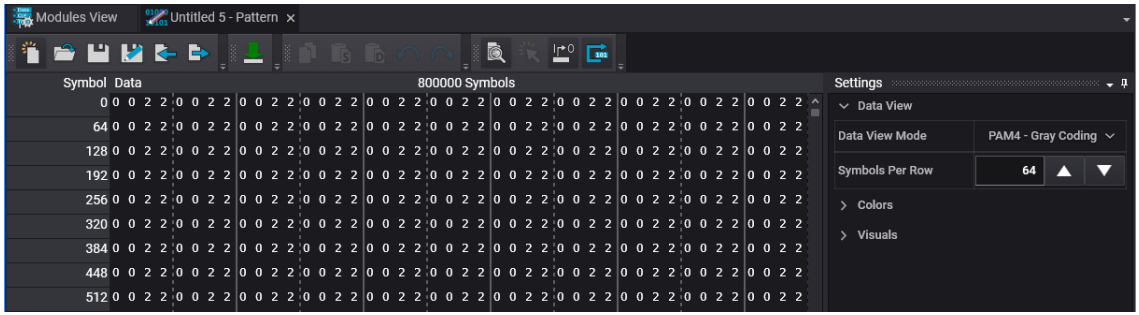
- **Coding -** Select the line coding as PAM6 or PAM8.
- **Uncoded** - In this mapping, the bit sequence 000 maps to Symbol 0, 001 to Symbol 1, 010 to Symbol 2, 011 to Symbol 3, 100 to Symbol 4 and 101 to Symbol 5 for PAM6. The bit sequence 000 maps to Symbol 0, 001 to Symbol 1, 010 to Symbol 2, 011 to Symbol 3, 100 to Symbol 4 and 101 to Symbol 5, 110 to Symbol 6 and 111 to Symbol 7 for PAM8.
- **Custom** - If the **Symbol Mapping** mode **Custom** is selected you have to specify the **Custom Mapping File**.
- **Symbol Level** - It controls the PAM6 or PAM8 level mappings. It can be used to adjust the actual output level that is being generated by a data output for a specific PAM6 or PAM8 symbol. For PAM6, Symbol Level 0 to 5 are available and for PAM8 Symbol Level 0 to 7 are visible. The levels of PAM6 symbol 0 and 5 cannot be adjusted and are always kept at the value of 0% and 100% of the actual output voltage swing. The levels of PAM8 symbol 0 and 7 cannot be adjusted and are always kept at the value of 0% and 100% of the actual output voltage swing.

Creating Patterns for AWG(s)

The M8070B software provides **Pattern Editor** for M8194A/M8195A/M8196A module as well. The functionality of the **Pattern Editor** is same as for other modules. You can create, edit, load patterns and perform the pattern settings in the same way as done for other modules. For more details, refer to Pattern Editor on page 655.

However for bit coded patterns, the **Pattern Editor** allows you to view the symbols in the **PAM4 No Coding** and **PAM4 Gray Coding**. These options are available in the **Settings** > **Data View Mode**.

The following figure shows an example of bit symbol, viewed in the **PAM4 Gray Coding.**



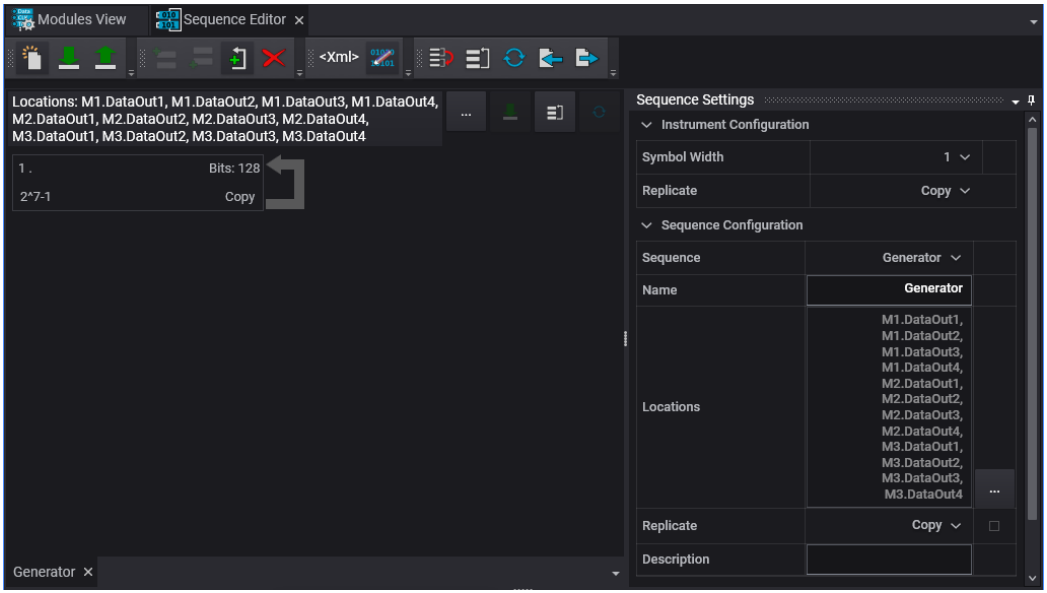
In the **PAM4 No Coding** mode, the bit sequence 00 maps to symbol 0, 10 maps to symbol 2 and 11 maps to symbol 3.

In the **PAM4 Gray Coding** mode, the bit sequence 00 maps to symbol 0, 00 maps to symbol 0, 01 maps to symbol 1, 11 maps to symbol 2 and 10 maps to symbol 3.

Sequence Settings for AWG(s)

The M8070B software provides **Sequence Editor** which can be used with most of the devices supported by M8070B. The functionality of the **Sequence Editor** is the same as for other modules. You can create, edit, load patterns and perform sequence settings in the same way as done in the M8070B sequence editor. You can change pattern type as static, clock, PRBS, memory pattern, in single block with infinite loop. For more details, refer to Sequence Editor on page 613.

The M819xA modules can be also be configured from the M8070B **Sequence Editor**. The following figure shows the AWG(s) **Sequence Editor**:



You can use the **Sequence Settings** window to reprogram the values of AWG parameters.

Parameters which are not applicable for AWG modules will be either hidden, disabled or checked when performing a sequence download.

The **Sequence Editor** when used with an AWG module, has the following capabilities:

- A single block can be looped infinitely
- Supports the following block types:
  - PRBS (all polynomials that fit into AWG memory)
  - Memory
  - Static 0 or 1
  - Single pulse per block
  - Clock

Jitter Setting in AWG(s)

The AWG integration into the M8070B software supports sinusoidal jitter, random jitter and spread spectrum clocking (SSC).

Sinusoidal jitter and random jitter can be turned on and off per channel while SSC can only be activated per module.

Periodic Jitter (Valid for PJ1, PJ2 and SSC)

When defining a sequence referencing a specific pattern it will automatically be generated containing the specified jitter. For example in case the given pattern has a duration of 1 µs for the selected baud rate and the jitter period is 2 µs it would not be possible for this jitter to correctly appear inside the pattern. To handle this a second iteration of the pattern is appended giving the memory segment a total duration of 2 µs. With this it is possible for the resulting waveform to contain the selected jitter.

A side effect of this procedure is that the required sample memory for a selected pattern changes depending on the selected jitter components.

In case the jitter cannot be mapped to the available memory while adhering to the jitter accuracy defined in the data sheet a warning message will be displayed to make the user aware of this shortcoming.

Measuring Periodic Jitter

When measuring periodic jitter on an oscilloscope it is important to note that the jitter period will always be rounded in a way that the effective pattern length (which may contain multiple iterations of the user defined pattern) is a multiple of this jitter period.

Another thing to note is that for short pattern, high jitter frequency and the case where the data rate is an integer multiple of the jitter frequency the effective pattern can become maximally short. This will be observable by a relatively fast start of waveform playback but can have an impact on the measured jitter histogram.

For the above mentioned cases the number of distinct edge deviations from their non-jittered positions can be limited which leads to a histogram containing only a low number of lines.

To tweak the quality of the jitter histogram it is possible to use a larger pattern e.g. by repeating the shorter pattern multiple times in the pattern file or using an odd number for the jitter frequency.

Random Jitter (RJ)

The given pattern will be generated with the selected random jitter parameters. Definable are thereby a low pass and high pass frequency which limits the contained jitter components.

Measuring Random Jitter

As the waveform is completely pre-calculated it is not possible to generate truly random jitter with this approach.

Similar to the periodic jitter case it is also true for random jitter that short patterns will not lead to a realistic looking jitter histogram. If a better jitter quality is desired it is therefore necessary to use a longer pattern. In case the actual pattern needs to be short it is possible to have it repeat multiple times in the pattern file and thereby obtain different edge deviations on a single symbol.

Controlling M8053A from M8070B System Software

The M8070B system software allows you to control the M8053A interference source module along with the M8050A modules. Once the M8053A interference source module is installed into an AXIe chassis, it can be accessed via the M8070B software.

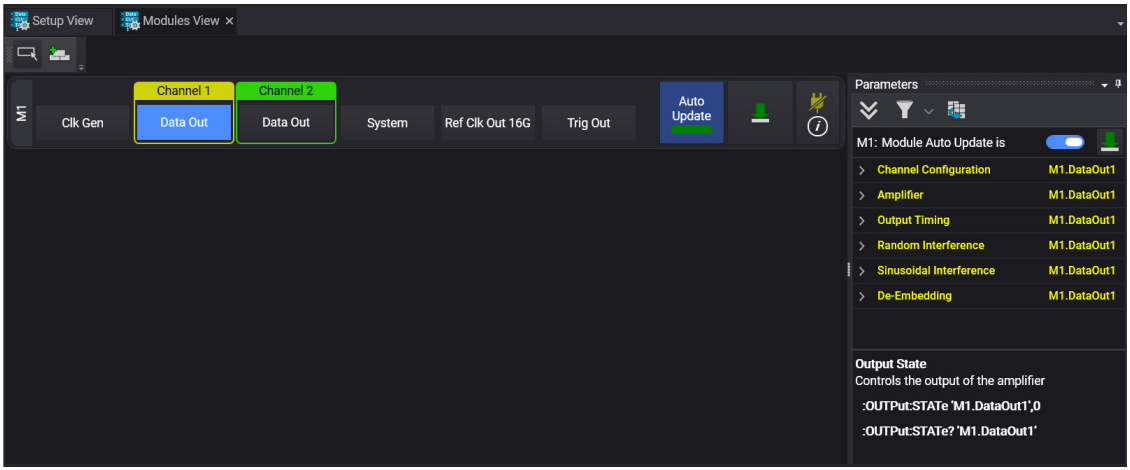
Ensure that you have the latest version of M8070B (version 10.5.200.8 or later) and M8053A module driver installed in your system.

You can control the following interference parameters for the M8053A interference source through M8070B system software.

- Channel Coupling
- Amplifier
- Output Timing
- Random Interference
- Sinusoidal Interference
- De-Embedding

M8053A in Module View

The following figure shows the **Module View** of M8053A.



M8053A Parameters Configuration

The M8053A interference source has the **Clk Gen**, **Data Out**, **System**, **Ref Clk Out 16G**, and **Trigger Out** ports. You can use the **Parameters** window to configure these ports.

The following parameters are available for **Data Out**:

- **Channel Configuration** – The Channel Configuration function has the following components:
  - **Channel Coupling** – Provides the flexibility to couple two channels for using them as a differential pair. With channel coupling enabled, sinusoidal and random interference can be injected either as common-mode or differential-mode interference. To couple channels 1 and 2, select “Ch1 and Ch2”. Once the channels are coupled, the parameters values will be identical across both channels.

    Select "None", if channel coupling is not required.

    Physical connection changes are required for the channels to be coupled. If two channels (Channel 1 and Channel 2) are coupled, then the differential pair cable must be connected to the non-inverted ports of channel 1 and channel 2. Ensure to terminate the unused output ports with 50 Ohms.
- **Amplifier** – The Amplifier function has the following components:
  - **Output State** – Enables or disables the state of the output.
  - **Amplitude** – This is a read-only parameter. The value of the amplifier amplitude is automatically calculated based on the enabled sources.
  - **External Attenuation** – Sets the external frequency-independent attenuation in dB. This option scales the source amplitude such that they are calibrated after the attenuator rather at the output of the instrument. Click the button to copy the de-embedding’s “Estimated DC Loss” value.
  - **Amplitude Correction Factor** – Sets the amplitude correction factor. The Amplitude Correction Factor parameter is not included in the coupling and so it can be set independently on each coupled channels.

    The Amplitude Correction Factor parameter enables you to correct the amplitude loss when channels are already coupled. The purpose of this parameter to increase/decrease the gain without changing the Amplitude parameter value. The amplitude correction factor follows the maximum limit of amplitude parameter.

The amplitude correction factor parameter of a channel is not synced with the coupled channel. If two channels (Channel 1 and Channel 2) are coupled, and the amplitude correction factor is changed for channel 1, then it does not affect the value of channel 2.

- **Output Timing** – Sets the data delay of the output channel.
- **Random Interference** – The **Random Interference** generates band-limited gaussian noise signals. It has the following components:
  - **RI State** – Enables or disables Random Interference.
  - **RI Amplitude (RMS)** – Sets the amplitude of the output signal for random interference in Vrms.
  - **RI Highest Frequency** – Used to set the random interference high frequency in Hz.
  - **RI Lowest Frequency** – Used to set the random interference low frequency in Hz.
- **Sinusoidal Interference** – The Sinusoidal Interference function has the following components:
  - **SI State (1/2)** – Enables or disables Sinusoidal Interference.
  - **SI Frequency (1/2)** – Sets the frequency of the output signal.
  - **SI Amplitude (1/2) (p-p)** – Sets the amplitude of the output signal.
  - **SI Phase (1/2)** – Sets the phase of the output signal.
- **De-Embedding** – The De-Embedding function has the following components:
  - **Channel Specific** – Applies channel specific correction of the amplitude and phase using an internal calibration.
  - **S-Parameter State** – Enables/Disables S-Parameter compensation.
  - **S-Parameter Profile** – Selects the S-Parameter profile for de-embedding. It also allows you to import and export a S-Parameter profile.
  - **S-Parameter Output Port** – Selects the output port in S-Parameter profile.
  - **S-Parameter Input Port** – Selects the input port in S-Parameter profile.
  - **Estimated DC Loss** – Displays the DC loss that is estimated from the loaded S-Parameters

The following parameters are available for **Clk Gen**:

- **Source** – Selects the trigger source of the instrument. It has the following options:

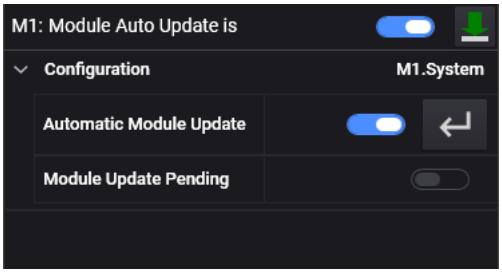
  - **Internal** – The sample rate is derived from and internal reference clock. See the datasheet for its accuracy.
  - **Reference** – The sample rate is derived from a 10/100 MHz reference clock applied to the “Ref Clk In” connector.
- **Sample Rate** – The sample rate is calculated automatically based on the configured interference source parameters.

The following parameters are available for **Ref Clk Out 16G**:

- **Output State** – Controls the output of the Ref Clk Out 16G. This output is not affected when the Global Output is enabled.
- **Frequency** – The frequency at the Ref Clk Out 16G is always 1/16th of the sample rate.

The following parameters are available for **System**:

- **Configuration** – The Configuration function has the following components:



  - **Automatic Module Update** – Enables or disables the automatic module updates. The same can be done by clicking the **Auto Update** button present on the Module View of module.

When the **Automatic Module Update** parameter is enabled, the modules state updates automatically, whenever a property is changed.

When the **Automatic Module Update** parameter is disabled, the time intensive operation's execution defers for parameter changes. Depending on the module type, this may disable some or all the

property updates. Additionally, it can also disable the dynamic parameter limit calculations, which can trigger the **Auto Correct Confirmation** dialog when the module updates.

- **Module Update Pending** – Applies the currently configured software state into module. This can also be done using the **Apply** button next to the Automatic Module Update ON/OFF toggle button. The same can be done by clicking the **Apply** button present on the Module View of module. The orange **Apply** button indicates that the module update is pending.

NOTE

This parameter cannot be changed directly. When the Automatic Module Update parameter is enabled, the Module Update Pending parameter changes to OFF automatically.

NOTE

The module update pending indication will not detect the changes done to (externally) referenced files or when bypassing the user interface. An example of this effect is a pattern file which is edited while being referenced by a sequence bound to the concerned module. Another example is a selected S-Parameter file which is modified directly on the file system.

To update the module in these cases, it is necessary to perform a full module update by triggering the module update command.

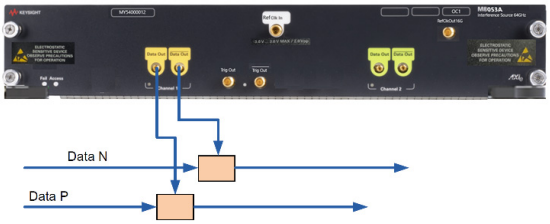
The following parameters are available for **Trig Out**:

- **Amplifier** – It provides the following options:
  - **Output State** – Enables or disables the state of the output.
  - **Amplitude** – Single-ended peak-to-peak amplitude of the Trig out signal, not adjustable.
  - **Offset** – Sets the offset voltage of output signal, not adjustable.
- **Output Timing**
  - **Divider** – Sets the Trig Out clock divider relative to the sample rate. Only even dividers are supported.
  - **Frequency** – Output frequency, calculated as sample rate divided by divider.

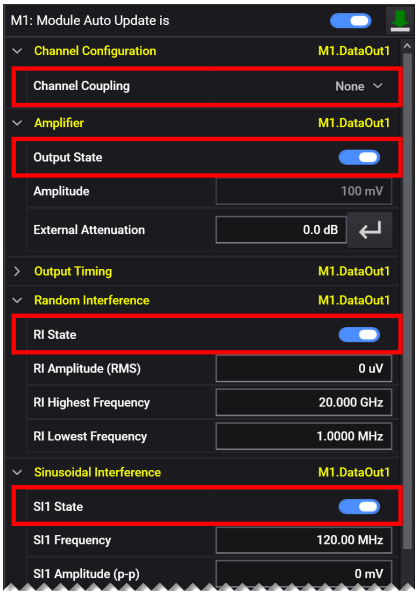
Simultaneous Injection of RI and SI Using M8053A on Same Channel

The M8053A enables you to generate random interference (RI) and sinusoidal interference (SI) on the same channel.

The following figure illustrates simultaneous injection of RI and SI using M8053A on the same channel.



The following functional blocks are available in the **Parameter Window** to generate RI and SI.

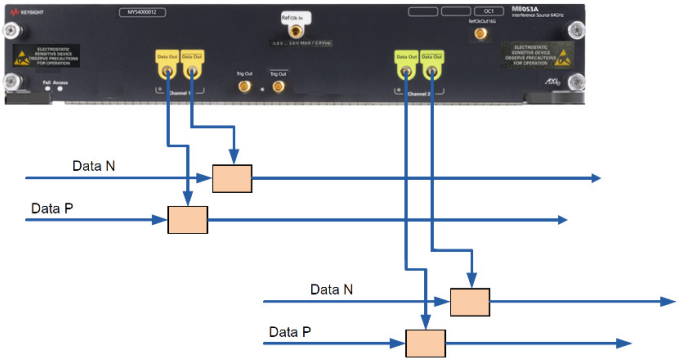


For more information on these functional blocks and corresponding parameters, refer to M8053A Parameters Configuration on page 307.

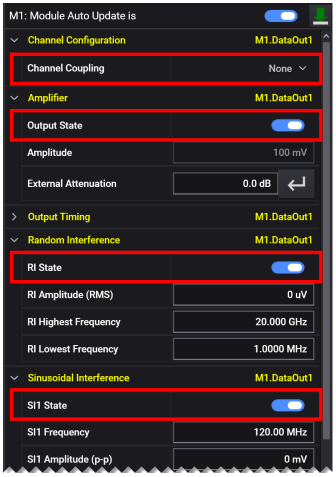
Simultaneous Injection of RI and SI Using M8053A on Different Channels

The M8053A enables you to generate random interference (RI) and sinusoidal interference (SI) on different channels simultaneously.

The following figure illustrates simultaneous injection of RI and SI using M8053A on the same channel.



The following functional blocks are available in the **Parameter Window** to generate RI and SI.



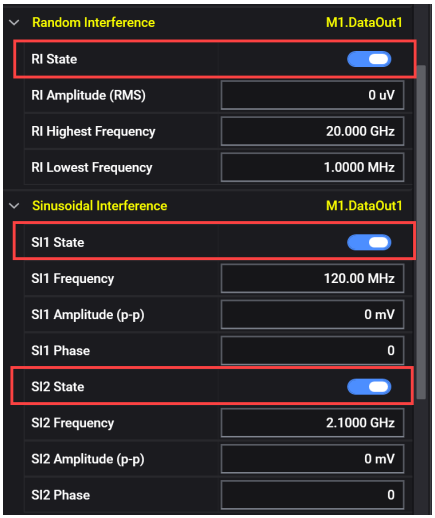
For more information on these functional blocks and corresponding parameters, refer to M8053A Parameters Configuration on page 307.

Simultaneous Injection of CMSI and DMSI Using M8053A

With channel coupling enabled, the M8053A can generate common-mode or differential mode interference signals. The mode is selectable for each source (SI1, SI2, RI) individually, allowing arbitrary combinations of random and sinusoidal interference sources with different modes.

Set the parameters to generate multi-tone CMSI/DMSI. For details on parameters, see M8053A Parameters Configuration on page 307.

NOTE The RI State and SI State (1/2) option must be enabled to generate CMSI and DMSI.

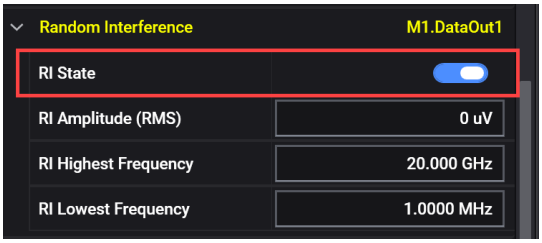


Simultaneous Injection of CMRI or DMRI using M8053A

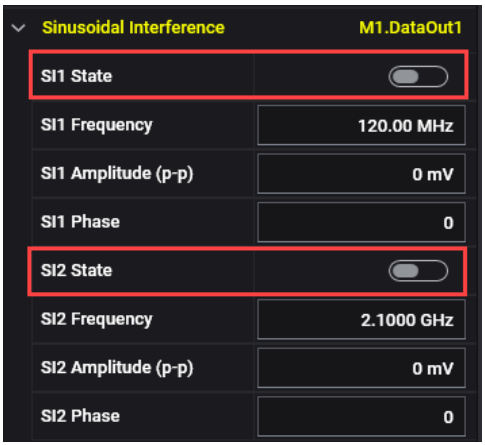
With channel coupling enabled, the M8053A can generate common mode random interference (CMRI) or differential mode random interference (DMRI) on an output signal. The mode is selectable for each source (SI1, SI2, RI) individually, allowing arbitrary combinations of random and sinusoidal interference sources with different modes.

Set the parameters to generate CMRI/DMRI. For details on parameters, see M8053A Parameters Configuration on page 307.

The RI State option must be enabled to generate CMRI and DMRI.



To generate CMRI and DMRI only, disable the **SI State (1/2)** option under the Sinusoidal Interference block.



Simultaneous Injection of CMRI with CMSI Using M8053A

The channels of M8053A can be coupled to generate common mode random interference (CMRI) with common mode sinusoidal interference (CMSI) on an output signal.

The following functional blocks are available in the **Parameter Window** to generate CMRI with CMSI.

- **Channel Configuration**: For generating CMRI with CMSI, do not select "**None**" from the **Channel Coupling** drop-down list.

  For more information, refer to M8053A Parameters Configuration Channel Configuration section.
- **Amplifier**: Refer to M8053A Parameters Configuration Amplifier section.
- **Random Interference**: For generating CMRI with CMSI, the following options must be configured under the Random Interference block:
  - **RI State**: Enable the RI state option.
  - **RI Mode**: From the **RI Mode** drop-down list, select **Common Mode**.

  For configuring the rest of the random interference options, refer to M8053A Parameters Configuration Random Interference section.
- **Sinusoidal Interference**: For generating CMRI with CMSI, the following options must be configured under the Sinusoidal Interference block:
  - **SI State (1/2)**: Enable the SI state (1/2) option.
  - **SI Mode (1/2)**: From the **SI Mode (1/2)** drop-down list, select **Common Mode**.

  For configuring the rest of the sinusoidal interference options, refer to M8053A Parameters Configuration Sinusoidal Interference section.
- **De-Embedding** - Refer to M8053A Parameters Configuration De-Embedding section.

Simultaneous Injection of CMRI with DMSI Using M8053A

The channels of M8053A can be coupled to generate common mode random interference (CMRI) with differential mode sinusoidal interference (DMSI) on an output signal.

The following functional blocks are available in the **Parameter Window** to generate CMRI with DMSI.

- **Channel Configuration**: For generating CMRI with DMSI, do not select "**None**" from the **Channel Coupling** drop-down list.

  For more information, refer to M8053A Parameters Configuration Channel Configuration section.
- **Amplifier**: Refer to M8053A Parameters Configuration Amplifier section.
- **Random Interference**: For generating CMRI with DMSI, the following options must be configured under the Random Interference block:
  - **RI State**: Enable the RI state option.
  - **RI Mode**: From the **RI Mode** drop-down list, select **Common Mode**.

  For configuring the rest of the random interference options, refer to M8053A Parameters Configuration Random Interference section.
- **Sinusoidal Interference**: For generating CMRI with DMSI, the following options must be configured under the Sinusoidal Interference block:
  - **SI State (1/2)**: Enable the SI state (1/2) option.
  - **SI Mode (1/2)**: From the **SI Mode (1/2)** drop-down list, select **Differential Mode**.

  For configuring the rest of the sinusoidal interference options, refer to M8053A Parameters Configuration Sinusoidal Interference section.
- **De-Embedding** - Refer to M8053A Parameters Configuration De-Embedding section.

Simultaneous Injection of DMRI with CMSI Using M8053A

The channels of M8053A can be coupled to generate differential mode random interference (DMRI) with common mode sinusoidal interference (CMSI) on an output signal.

The following functional blocks are available in the **Parameter Window** to generate DMRI with CMSI.

- **Channel Configuration**: For generating DMRI with CMSI, do not select "**None**" from the **Channel Coupling** drop-down list.

  For more information, refer to M8053A Parameters Configuration Channel Configuration section.
- **Amplifier**: Refer to M8053A Parameters Configuration Amplifier section.
- **Random Interference**: For generating DMRI with CMSI, the following options must be configured under the Random Interference block:
  - **RI State**: Enable the RI state option.
  - **RI Mode**: From the **RI Mode** drop-down list, select **Differential Mode**.

  For configuring the rest of the random interference options, refer to M8053A Parameters Configuration Random Interference section.
- **Sinusoidal Interference**: For generating DMRI with CMSI, the following options must be configured under the Sinusoidal Interference block:
  - **SI State (1/2)**: Enable the SI state (1/2) option.
  - **SI Mode (1/2)**: From the **SI Mode (1/2)** drop-down list, select **Common Mode**.

  For configuring the rest of the sinusoidal interference options, refer to M8053A Parameters Configuration Sinusoidal Interference section.
- **De-Embedding** - Refer to M8053A Parameters Configuration De-Embedding section.

Simultaneous Injection of DMRI with DMSI Using M8053A

The channels of M8053A can be coupled to generate differential mode random interference (DMRI) with differential mode sinusoidal interference (DMSI) on an output signal.

The following functional blocks are available in the **Parameter Window** to generate DMRI with DMSI.

- **Channel Configuration**: For generating DMRI with DMSI, do not select "**None**" from the **Channel Coupling** drop-down list.

  For more information, refer to M8053A Parameters Configuration Channel Configuration section.
- **Amplifier**: Refer to M8053A Parameters Configuration Amplifier section.
- **Random Interference**: For generating DMRI with DMSI, the following options must be configured under the Random Interference block:
  - **RI State**: Enable the RI state option.
  - **RI Mode**: From the **RI Mode** drop-down list, select **Differential Mode**.

  For configuring the rest of the random interference options, refer to M8053A Parameters Configuration Random Interference section.
- **Sinusoidal Interference**: For generating DMRI with DMSI, the following options must be configured under the Sinusoidal Interference block:
  - **SI State (1/2)**: Enable the SI state (1/2) option.
  - **SI Mode (1/2)**: From the **SI Mode (1/2)** drop-down list, select **Differential Mode**.

  For configuring the rest of the sinusoidal interference options, refer to M8053A Parameters Configuration Sinusoidal Interference section.
- **De-Embedding** - Refer to M8053A Parameters Configuration De-Embedding section.

M8053A as External Level Interference (RI/SI) Source

The M8053A is an external level interference source with Random and Sinusoidal modulation. For more details on the M8053A configuration, refer to M8053A Parameters Configuration . The M8070B system software allows controlling interference parameters such as amplitude, highest frequency, lowest frequency, crest factor and so on.

Keysight provides a matched coupler pair (M8053A-803) for injecting the RI or SI signal before or after the channel. Specifications for external level interference sources RI/SI with M8053A can be found in M8053A data sheet (see, www.keysight.com/find/M8053A).

Controlling M8054A from M8070B System Software

The M8070B system software allows you to control the M8054A interference source module along with the M8020A/M8040A modules. Once the M8054A interference source module is installed into an AXIe chassis, it can be accessed via the M8070B software.

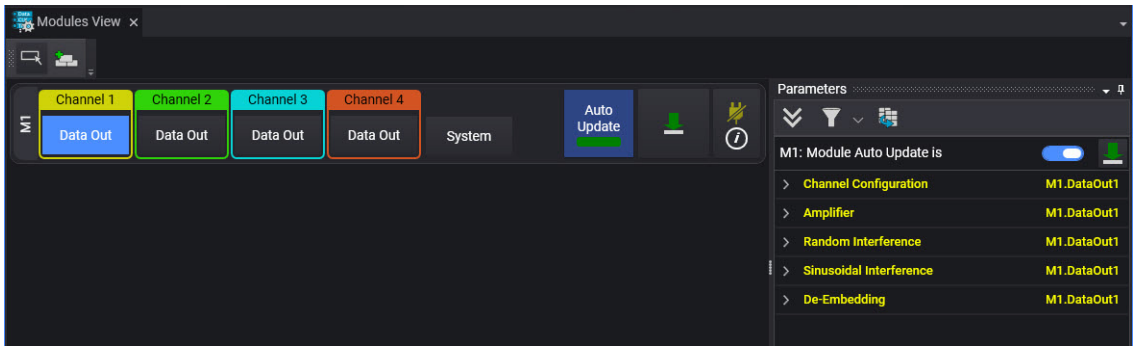
Ensure that you have the latest version of M8070B (version 6.5 or later) and M8054A software installed in your system.

You can control the following interference parameters for the M8054A interference source through M8070B system software.

- Channel Coupling
- Amplifier
- Random Interference
- Sinusoidal Interference
- De-Embedding

M8054A in Module View

The following figure shows the **Module View** of M8054A.



M8054A Configuration

By default, the Interference Source option is enabled.

M8054A Parameters configuration

The M8054A interference source has the **Data Out** and **System** ports. You can use the **Parameters** window to configure these ports.

The following parameters are available for **Data Out**:

- **Channel Configuration**: The Channel Configuration function has the following components:
  - **Channel Coupling**: Provides the flexibility to couple two channels. Depending upon the availability of the channels in a module, the channels can be coupled in the following ways:
    - **Four channel Mode**: Channels 1/2 and Channels 3/4
    - **Two Channel Module**: Channels 1/2

    Use the drop-down option to select the channels. For example, selecting "1/2" will couple channels 1 and 2. Once the channels are coupled, the parameters values will be identical across both channels.

    Select "None", if channel coupling is not required.

    Physical connection changes are required for the channels to be coupled. If two channels (Channel 1 and Channel 2) are coupled, then the differential pair cable must be connected to the non-inverted ports of channel 1 and channel 2. Ensure to terminate the unused output ports with 50 Ohms.

- **Amplifier**: The Amplifier function has the following components:
  - **Output State**: Enables or disables the state of the output.
  - **Termination Voltage**: Sets the termination voltage of the output signal.
  - **Amplitude** – This option is disabled. The value of the Amplitude option depends on the enabled states. The amplitude value can be calculated as the sum of RI Amplitude Vpp (RI Amplitude Vrms, CrestFactor), SI1 Amplitude, and SI2 Amplitude based on the states enabled.
  - **Offset**: Sets the offset voltage of the output signal.

- **Amplitude Correction Factor** – Sets the amplitude correction factor. The **Amplitude Correction Factor** parameter is not included in the coupling and so it can be set independently on each coupled channels.

  The **Amplitude Correction Facto**r parameter enables you to correct the amplitude loss when channels are already coupled. The purpose of this parameter to increase/decrease the gain without changing the Amplitude parameter value. The amplitude correction factor follows the maximum limit of amplitude parameter.
- The amplitude correction factor parameter of a channel is not synced with the coupled channel. If two channels (Channel 1 and Channel 2) are coupled, and the amplitude correction factor is changed for channel 1, then it does not affect the value of channel 2.
- **Fast Amplitude Change** – Enables or disables the amplitude change without waveform recalculation and download. This option can be enabled for new optimization and can be disabled to have existing programs behave exactly as now. You can use the download waveform option to download the waveform at any time.

  This option is applicable when:
  - Amplitude is above 80mV
  - If only one of the interference sources (RI, SI1 or SI2) is enabled

  If more than one interference sources (RI, SI1 and SI2) are enabled, the waveform re-calculation is necessary and waveform needs to be re-downloaded on changing the amplitude. Because of this 'Fast Amplitude Change' is not used if more than one sources are enabled.

  This option is available only when the '**Interference Source**' or '**Modulated Clock and Interference Source**' options are selected in the **Configuration** dialog box. For more information, refer to M819xA Configuration on page 261.

- **Random Interference**: The **Random Interference** function has the following components:
  - **RI State**: Enables or disables Random Interference.
  - **RI Mode**: Sets the mode of the output signal. The available options are:
    - **Common Mode**: In this case, Common Mode Random Interference will be generated using non-inverted port of coupled channels.

        - **Differential Mode**: In this case, Differential Mode Random Interference will be generated using non-inverted port of coupled channels.
    - **RI Amplitude (RMS)**: Sets the amplitude of the output signal for random interference in Vrms.

      Note that the value of RI Amplitude will also reflect in the Amplitude parameter of the Amplifier functional block. The total amplitude across all enabled states [RI (p-p), SI1 (p-p), SI2 (p-p)] must be between 0 to 995 mV.

      The RI Amplitude V (p-p) will change when changing RI amplitude (Vrms) or the crest factor change (Vpp = CF(linear)*Vrms).
    - **Crest Factor unit**: Used to set the random interference crest factor unit type. Following unit types are allowed:
        - **Linear**: This is the default setting. Select this unit to specify the crest factor as voltage ratio.
        - **Logarithmic**: Select this unit to specify the crest factor in dB.
    - **RI Crest Factor**: Used to set the random interference crest factor value in dB or as voltage ratio depending on the currently selected crest factor unit type. This is defined as peak value.
    - **RI Highest Frequency**: Used to set the random interference high frequency in Hz.
    - **RI Lowest Frequency**: Used to set the random interference low frequency in Hz.
- **Sinusoidal Interference**: The Sinusoidal Interference function has the following components:
    - **SI State (1/2)**: Enables or disables Sinusoidal Interference.
    - **SI Mode (1/2)**: Sets the tone mode of the output signal. The available options are:
        - **Common Mode**: In this case, Common Mode Sinusoidal Interference will be generated using non-inverted port of coupled channels.
        - **Differential Mode**: In this case, Differential Mode Sinusoidal Interference will be generated using non-inverted port of coupled channels.

- **SI Frequency (1/2)**: Sets the frequency of the output signal for tone mode.

NOTE

The Frequency option is obsolete now. The SI1 Frequency acts as Frequency (old) when SI2 state is disabled.

When the SI1 State option is enabled, and the SI2 State option is disabled, then the following frequency range is applicable for SI1 Frequency: 160KHz to 32 GHz.

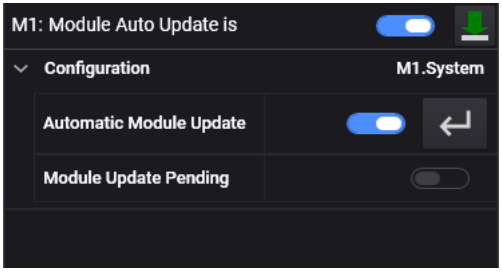
When both the SI1 Frequency and SI2 Frequency options are enabled, then the frequency range is 1MHz to 12GHz. This is multi-tone behavior.

- **SI Amplitude (1/2) (p-p)**: Sets the amplitude of the output signal for tone mode.
- **SI Phase (1/2)**: Sets the phase of the output signal for tone mode.

- **De-Embedding** - The De-Embedding function has the following components:
  - **Channel Specific** - Applies channel specific correction of the amplitude and phase using an internal calibration.
  - **Standard Cable** - Defines whether the signal should be pre-distorted considering the properties of the standard cable set.

The following parameters are available for **System**:

- **Configuration**: The Configuration function has the following components:



  - **Automatic Module Update**: Enables or disables the automatic module updates. The same can be done by clicking the **Auto Update** button present on the Module View of module.

When the **Automatic Module Update** parameter is enabled, the modules state updates automatically, whenever a property is changed.

When the **Automatic Module Update** parameter is disabled, the time intensive operation's execution defers for parameter changes. Depending on the module type, this may disable some or all the property updates. Additionally, it can also disable the dynamic parameter limit calculations, which can trigger the **Auto Correct Confirmation** dialog when the module updates.

- **Module Update Pending**: Applies the currently configured software state into module. This can also be done using the **Apply** button next to the Automatic Module Update ON/OFF toggle button. The same can be done by clicking the **Apply** button present on the Module View of module. The orange **Apply** button indicates that the module update is pending.

NOTE This parameter cannot be changed directly. When the Automatic Module Update parameter is enabled, the Module Update Pending parameter changes to OFF automatically.

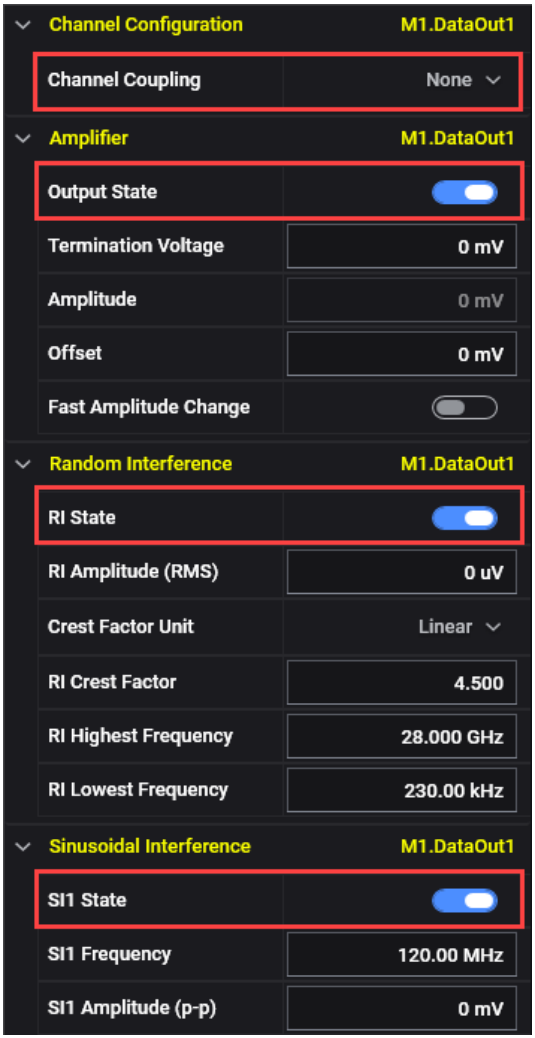
NOTE The module update pending indication will not detect the changes done to (externally) referenced files or when bypassing the user interface. An example of this effect is a pattern file which is edited while being referenced by a sequence bound to the concerned module. Another example is a selected S-Parameter file which is modified directly on the file system.

To update the module in these cases, it is necessary to perform a full module update by triggering the module update command.

Simultaneous Injection of RI and SI Using M8054A on Same Channel

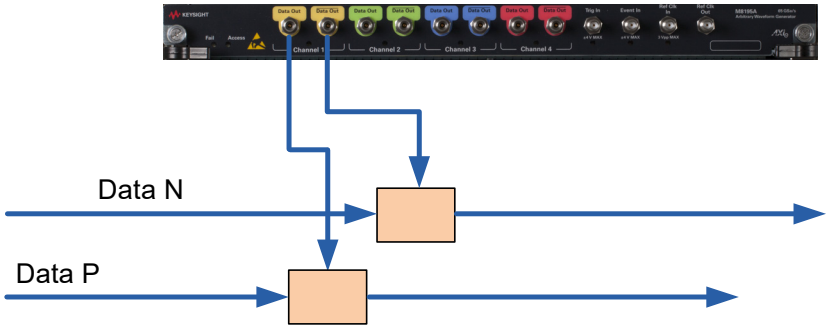
The M8054A enables you to generate random interference (RI) and sinusoidal interference (SI) on the same channel.

M8054A RI and SI Parameters (Same Channel)



The following functional blocks are available in the **Parameter Window** to generate RI and SI.

- **Channel Configuration**: For generating RI and SI, select **None** from the **Channel Coupling** drop-down list.



For more information, refer to M8054A Parameters configuration Channel Configuration section.

- **Amplifier** – This functional block has the following parameters:
  - **Output State** – For generating RI and SI on same channel, the **Output State** option must be enabled.
  - **Termination Voltage** – Sets the external termination voltage.
  - **Amplitude** – This option is disabled. The value of the Amplitude option depends on the enabled states. The amplitude value can be calculated as the sum of RI Amplitude Vpp (RI Amplitude Vrms, CrestFactor), SI1 Amplitude, and SI2 Amplitude based on the states enabled.
  - **Offset** – Sets the offset of the output signal.
  - **Fast Amplitude Change** – Enables or disables the amplitude change without waveform recalculation and download. This option can be enabled for new optimization and can be disabled to have existing programs behave exactly as now. You can use the download waveform option to download the waveform at any time.

    This option is applicable when:

    - Amplitude is above 80mV
    - If only one of the interference sources (RI, SI1 or SI2) is enabled

- **Random Interference**: For generating RI and SI on the same channel, the following option must be configured under the Random Interference block:
  - **RI State**: The RI State option must be enabled.
  - **RI Amplitude (RMS)**: Sets the amplitude of the output signal for random interference in Vrms.

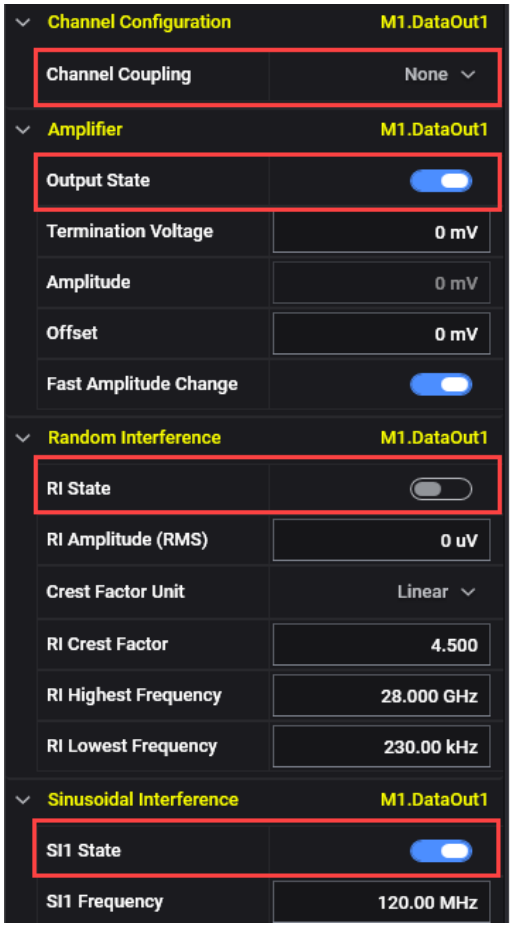
    Note that the value of RI Amplitude will also reflect in the Amplitude parameter of the Amplifier functional block. The total amplitude across all enabled states [RI (p-p), SI1 (p-p), SI2 (p-p)] must be between 0 to 995 mV.

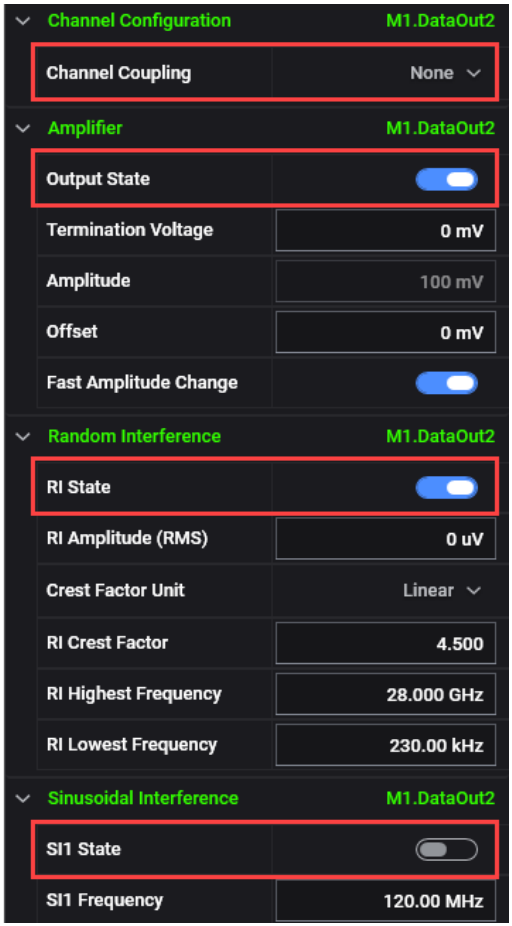
    The RI Amplitude V (p-p) will change when changing RI amplitude (Vrms) or the crest factor change (Vpp = CF(linear)*Vrms).
  - **Crest Factor unit**: Used to set the random interference crest factor unit type. Following unit types are allowed:
    - **Linear**: This is the default setting. Select this unit to specify the crest factor as voltage ratio.
    - **Logarithmic**: Select this unit to specify the crest factor in dB.
  - **RI Crest Factor**: Used to set the random interference crest factor value in dB or as voltage ratio depending on the currently selected crest factor unit type. This is defined as peak value.
  - **RI Highest Frequency**: Used to set the random interference high frequency in Hz.
  - **RI Lowest Frequency**: Used to set the random interference low frequency in Hz.
- **Sinusoidal Interference**: For generating RI and SI on the same channel, the following option must be configured under the Sinusoidal Interference block:
  - **SI State (1/2)**: The SI State (1/2) option must be enabled.
  - **SI Frequency (1/2)**: Sets the frequency of the output signal for tone mode.
  - **SI Amplitude (1/2) (p-p)**: Sets the amplitude of the output signal for tone mode.
  - **SI Phase (1/2)**: Sets the phase of the output signal for tone mode.
- **De-Embedding** - Refer to M8054A Parameters configuration De-Embedding section.

Simultaneous Injection of RI and SI Using M8054A on Different Channels

The M8054A enables you to generate random interference (RI) and sinusoidal interference (SI) on different channels simultaneously.

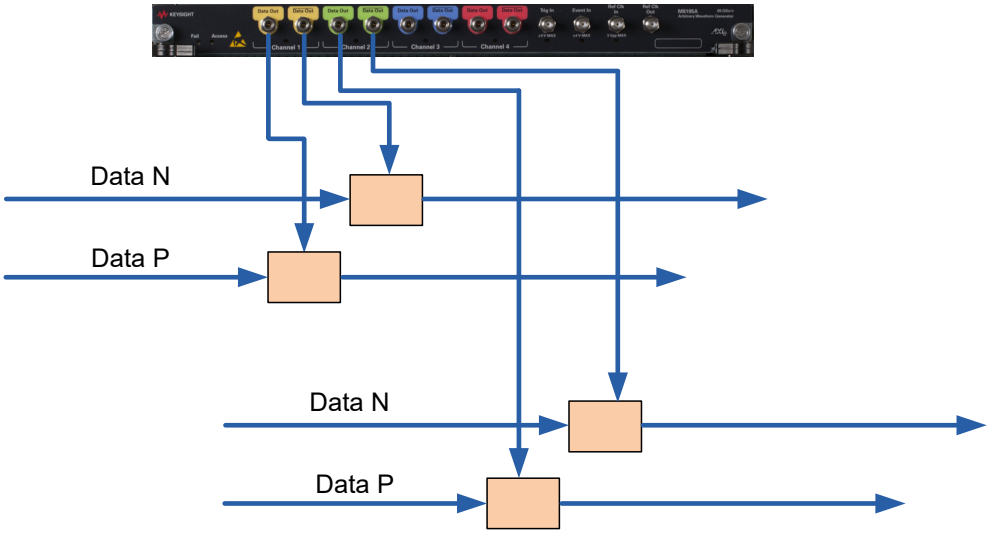
M8054A RI and SI Parameters (Different Channels)





The following functional blocks are available in the **Parameter Window** to generate RI and SI.

- **Channel Configuration**: For generating RI and SI, select **None** from the **Channel Coupling** drop-down list on two different channels.



For more information, refer to M8054A Parameters configuration Channel Configuration section.

- **Amplifier**: For generating RI and SI on different Channels, the **Output State** option must be enabled on both the channels. Refer to M8054A RI and SI Parameters (Same Channel) Amplifier section.
- **Random Interference**: For generating RI and SI on different channels, the following option must be configured under the Random Interference block of Channel1:
  - **RI State**: The RI State option must be enabled.

  For configuring the rest of the random interference options, refer to M8054A RI and SI Parameters (Same Channel) Random Interference section.
- **Sinusoidal Interference**: For generating RI and SI on different channels, the following option must be configured under the Sinusoidal Interference block of Channel2:
  - **SI State (1/2)**: The SI State (1/2) option must be enabled.

For configuring the rest of the sinusoidal interference options, refer to M8054A RI and SI Parameters (Same Channel) Sinusoidal Interference section.

NOTE For generating RI and SI on different channels, the RI state of one channel and the SI state of another channel must be enabled.

- **De-Embedding** - Refer to M8054A Parameters configuration De-Embedding section.

Simultaneous Injection of CMSI and DMSI Using M8054A

The channels of M8054A can be coupled to generate common mode sinusoidal interference (CMSI) and differential mode sinusoidal interference (DMSI) on an output signal. CMSI/DMSI is an extension of existing sinusoidal interference.

Set the parameters to generate multi-tone CMSI/DMSI. For details on parameters, see M8054A CMSI and DMSI Parameters .

M8054A CMSI and DMSI Parameters

The following functional blocks are available in the **Parameters** Window to generate multi-tone CMSI/DMSI.

- **Channel Configuration**: The Channel Configuration function has the following components:
  - **Channel Coupling**: Provides the flexibility to couple two channels. Depending upon the availability of the channels in a module, the channels can be coupled in the following ways:
    - **Four Channel Module**: Channels 1/2 and Channels 3/4
    - **Two Channel Module**: Channels 1/2

    Use the drop-down option to select the channels. For example, selecting "1/2" will couple channels 1 and 2. Once the channels are coupled, the parameters values will be identical across both channels.

    Select "None", if channel coupling is not required.

    When the channel coupling is enabled, the parameters of both the coupled channels are synced automatically. Physical connection changes are required for the channels to be coupled. If two channels (Channel 1 and Channel 2) are coupled, then the differential pair cable must be connected to the non-inverted ports of channel 1 and channel 2. Ensure to terminate the unused output ports with 50 Ohms.
- **Amplifier**: The Amplifier function has the following components:
  - **Output State**: Enables or disables the state of the output.
  - **Termination Voltage**: Sets the termination voltage of the output signal.
  - **Amplitude** – This option is disabled. The value of the Amplitude option depends on the enabled states. The amplitude value can be calculated as the sum of RI Amplitude Vpp (RI Amplitude Vrms, CrestFactor), SI1 Amplitude, and SI2 Amplitude based on the states enabled.

- **Offset**: Sets the offset voltage of the output signal.
- **Amplitude Correction**: Sets the amplitude correction factor.

  The **Amplitude Correction Factor** parameter is not included in the coupling and so it can be set independently on each coupled channel.

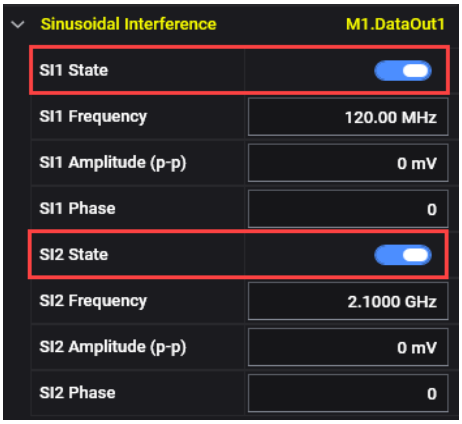
  The **Amplitude Correction Factor** parameter enables you to correct the amplitude loss when channels are already coupled. The purpose of this parameter to increase/decrease the gain without changing the Amplitude parameter value. The amplitude correction factor follows the maximum limit of amplitude parameter.

  The amplitude correction factor parameter of a channel is not synced with the coupled channel. If two channels (Channel 1 and Channel 2) are coupled, and the amplitude correction factor is changed for channel 1, then it does not affect the value of channel 2.
- **Fast Amplitude Change** – Enables or disables the amplitude change without waveform recalculation and download. This option can be enabled for new optimization and can be disabled to have existing programs behave exactly as now. You can use the download waveform option to download the waveform at any time.

  This option is applicable when:
  - Amplitude is above 80mV
  - If only one of the interference sources (RI, SI1 or SI2) is enabled

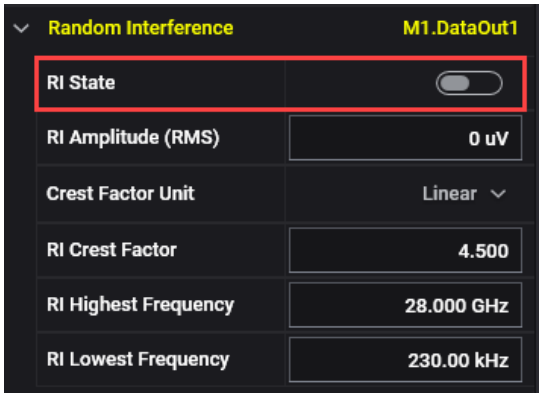
- **Sinusoidal Interference**: This functional block allows you to set State, Mode, Frequency, Amplitude and Phase for individual signal (1/2). It has the following parameters:
  - **SI State (1/2)**: Enables or disables Sinusoidal Interference.

NOTE The SI State (1/2) option must be enabled to generate CMSI and DMSI.



- **SI Mode (1/2)**: Sets the tone mode of the output signal. The available options are:
  - **Common Mode**: In this case, Common Mode Sinusoidal Interference will be generated using non-inverted port of coupled channels.
  - **Differential Mode**: In this case, Differential Mode Sinusoidal Interference will be generated using non-inverted port of coupled channels.
- **SI Frequency (1/2)**: Sets the frequency of the selected tone (1/2).
- **SI Amplitude (p-p) (1/2)**: Sets the amplitude of selected tone (1/2). Please note that the value of Amplitude 1 will also reflect in the Amplitude parameter of the Amplifier functional block. The total amplitude across both tones must be between 0 to 995 mV.
- **SI Phase (1/2)**: Sets the phase of the selected tone (1/2).

- **Random Interference**: To generate CMSI and DMSI only, disable the **RI State** option under the Random Interference block.



- **De-Embedding** - Refer to M8054A Parameters configuration De-Embedding section.

Simultaneous Injection of CMRI or DMRI using M8054A

The channels of M8054A can be coupled to generate common mode random interference (CMRI) or differential mode random interference (DMRI) on an output signal. CMRI/DMRI is an extension of existing interference source.

Set the parameters to generate CMRI/DMRI. For details on parameters, see M8054A CMRI/DMRI Parameters .

M8054A CMRI/DMRI Parameters

The following functional blocks are available in the **Parameters** Window to generate CMRI or DMRI.

- **Channel Configuration**: The Channel Configuration function has the following components:
  - **Channel Coupling**: Provides the flexibility to couple two channels. Depending upon the availability of the channels in a module, the channels can be coupled in the following ways:
    - **Four channel Mode**: Channels 1/2 and Channels 3/4
    - **Two Channel Module**: Channels 1/2

    Use the drop-down option to select the channels. For example, selecting "1/2" will couple channels 1 and 2. Once the channels are coupled, the parameters values will be identical across both channels.

    Select "None", if you don't want to generate CMRI.

    Physical connection changes are required for the channels to be coupled. Ensure to terminate the unused output ports with 50 Ohms.
- **Amplifier**: The Amplifier function has the following components:
  - **Output State**: Enables or disables the state of the output.
  - **Termination Voltage**: Sets the termination voltage of the output signal.
  - **Amplitude** – This option is disabled. The value of the Amplitude option depends on the enabled states. The amplitude value can be calculated as the sum of RI Amplitude Vpp (RI Amplitude Vrms, CrestFactor), SI1 Amplitude, and SI2 Amplitude based on the states enabled.
  - **Offset**: Sets the offset voltage of the output signal.

- **Amplitude Correction Factor** – Sets the amplitude correction factor. The **Amplitude Correction Factor** parameter is not included in the coupling and so it can be set independently on each coupled channels.

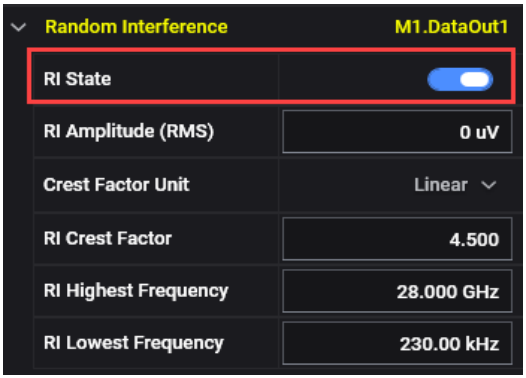
  The **Amplitude Correction Facto**r parameter enables you to correct the amplitude loss when channels are already coupled. The purpose of this parameter to increase/decrease the gain without changing the Amplitude parameter value. The amplitude correction factor follows the maximum limit of amplitude parameter.

  The amplitude correction factor parameter of a channel is not synced with the coupled channel. If two channels (Channel 1 and Channel 2) are coupled, and the amplitude correction factor is changed for channel 1, then it does not affect the value of channel 2.
- **Fast Amplitude Change** – Enables or disables the amplitude change without waveform recalculation and download. This option can be enabled for new optimization and can be disabled to have existing programs behave exactly as now. You can use the download waveform option to download the waveform at any time.

  This option is applicable when:
  - Amplitude is above 80mV
  - If only one of the interference sources (RI, SI1 or SI2) is enabled

- **Random interference**: The Random interference function has the following components:
  - **RI State**: Enables or disables Random Interference.

NOTE The RI State option must be enabled to generate CMRI and DMRI.



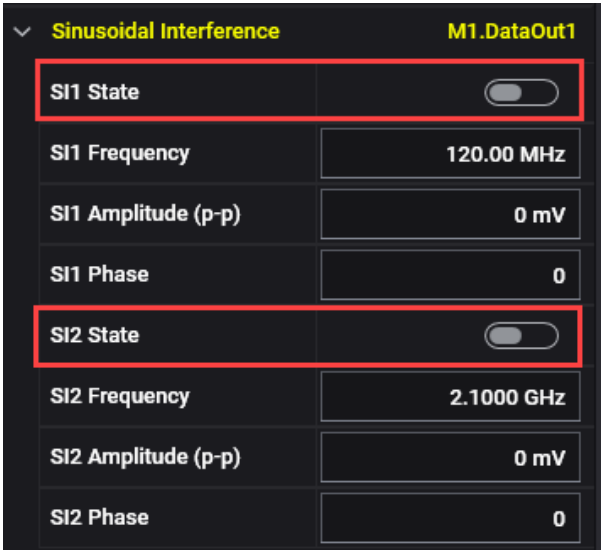
- **RI Mode**: Sets the mode of the output signal. The available options are:
  - **Common Mode**: In this case, Common Mode Random Interference will be generated using non-inverted port of coupled channels.
  - **Differential Mode**: In this case, Differential Mode Random Interference will be generated using non-inverted port of coupled channels.
- **RI Amplitude (RMS)**: Sets the amplitude of the output signal for random interference in Vrms.

  Note that the value of RI Amplitude will also reflect in the Amplitude parameter of the Amplifier functional block. The total amplitude across all enabled states [RI (p-p), SI1 (p-p), SI2 (p-p)] must be between 0 to 995 mV.

  The RI Amplitude V (p-p) will change when changing RI amplitude (Vrms) or the crest factor change (Vpp = CF(linear)*Vrms).
- **Crest Factor unit**: Used to set the random interference crest factor unit type. Following unit types are allowed:
  - **Linear**: This is the default setting. Select this unit to specify the crest factor as voltage ratio.
  - **Logarithmic**: Select this unit to specify the crest factor in dB.

- **RI Crest Factor**: Used to set the random interference crest factor value in dB or as voltage ratio depending on the currently selected crest factor unit type. This is defined as peak value.
- **RI Highest Frequency**: Used to set the random interference high frequency in Hz.
- **RI Lowest Frequency**: Used to set the random interference low frequency in Hz.

- **Sinusoidal Interference**: To generate CMRI and DMRI only, disable the **SI State (1/2)** option under the Sinusoidal Interference block.



- **De-Embedding** - Refer to M8054A Parameters configuration De-Embedding section.

Simultaneous Injection of CMRI with CMSI Using M8054A

The channels of M8054A can be coupled to generate common mode random interference (CMRI) with common mode sinusoidal interference (CMSI) on an output signal.

M8054A CMRI with CMSI Parameters

The following functional blocks are available in the **Parameter Window** to generate CMRI with CMSI.

- **Channel Configuration**: For generating CMRI with CMSI, do not select "**None**" from the **Channel Coupling** drop-down list.

  For more information, refer to M8054A Parameters configuration Channel Configuration section.
- **Amplifier**: Refer to M8054A CMSI and DMSI Parameters Amplifier section.
- **Random Interference**: For generating CMRI with CMSI, the following options must be configured under the Random Interference block:
  - **RI State**: Enable the RI state option.
  - **RI Mode**: From the **RI Mode** drop-down list, select **Common Mode**.

  For configuring the rest of the random interference options, refer to M8054A CMRI/DMRI Parameters Random Interference section.
- **Sinusoidal Interference**: For generating CMRI with CMSI, the following options must be configured under the Sinusoidal Interference block:
  - **SI State (1/2)**: Enable the SI state (1/2) option.
  - **SI Mode (1/2)**: From the **SI Mode (1/2)** drop-down list, select **Common Mode**.

  For configuring the rest of the sinusoidal interference options, refer to M8054A CMSI and DMSI Parameters Sinusoidal Interference section.
- **De-Embedding** - Refer to M8054A Parameters configuration De-Embedding section.

Simultaneous Injection of CMRI with DMSI Using M8054A

The channels of M8054A can be coupled to generate common mode random interference (CMRI) with differential mode sinusoidal interference (DMSI) on an output signal.

M8054A CMRI with DMSI Parameters

The following functional blocks are available in the **Parameter Window** to generate CMRI with DMSI.

- **Channel Configuration**: For generating CMRI with DMSI, do not select "**None**" from the **Channel Coupling** drop-down list.

  For more information, refer to M8054A Parameters configuration Channel Configuration section.
- **Amplifier**: Refer to M8054A CMSI and DMSI Parameters Amplifier section.
- **Random Interference**: For generating CMRI with DMSI, the following options must be configured under the Random Interference block:
  - **RI State**: Enable the RI state option.
  - **RI Mode**: From the **RI Mode** drop-down list, select **Common Mode**.

  For configuring the rest of the random interference options, refer to M8054A CMRI/DMRI Parameters Random Interference section.
- **Sinusoidal Interference**: For generating CMRI with DMSI, the following options must be configured under the Sinusoidal Interference block:
  - **SI State (1/2)**: Enable the SI state (1/2) option.
  - **SI Mode (1/2)**: From the **SI Mode (1/2)** drop-down list, select **Differential Mode**.

  For configuring the rest of the sinusoidal interference options, refer to M8054A CMSI and DMSI Parameters Sinusoidal Interference section.
- **De-Embedding** - Refer to M8054A Parameters configuration De-Embedding section.

Simultaneous Injection of DMRI with CMSI Using M8054A

The channels of M8054A can be coupled to generate differential mode random interference (DMRI) with common mode sinusoidal interference (CMSI) on an output signal.

M8054A DMRI with CMSI Parameters

The following functional blocks are available in the **Parameter Window** to generate DMRI with CMSI.

- **Channel Configuration**: For generating DMRI with CMSI, do not select "**None**" from the **Channel Coupling** drop-down list.

  For more information, refer to M8054A Parameters configuration Channel Configuration section.
- **Amplifier**: Refer to M8054A CMSI and DMSI Parameters Amplifier section.
- **Random Interference**: For generating DMRI with CMSI, the following options must be configured under the Random Interference block:
  - **RI State**: Enable the RI state option.
  - **RI Mode**: From the **RI Mode** drop-down list, select **Differential Mode**.

  For configuring the rest of the random interference options, refer to M8054A CMRI/DMRI Parameters Random Interference section.
- **Sinusoidal Interference**: For generating DMRI with CMSI, the following options must be configured under the Sinusoidal Interference block:
  - **SI State (1/2)**: Enable the SI state (1/2) option.
  - **SI Mode (1/2)**: From the **SI Mode (1/2)** drop-down list, select **Common Mode**.

  For configuring the rest of the sinusoidal interference options, refer to M8054A CMSI and DMSI Parameters Sinusoidal Interference section.
- **De-Embedding** - Refer to M8054A Parameters configuration De-Embedding section.

Simultaneous Injection of DMRI with DMSI Using M8054A

The channels of M8054A can be coupled to generate differential mode random interference (DMRI) with differential mode sinusoidal interference (DMSI) on an output signal.

M8054A DMRI with DMSI Parameters

The following functional blocks are available in the **Parameter Window** to generate DMRI with DMSI.

- **Channel Configuration**: For generating DMRI with DMSI, do not select "**None**" from the **Channel Coupling** drop-down list.

  For more information, refer to M8054A Parameters configuration Channel Configuration section.
- **Amplifier**: Refer to M8054A CMSI and DMSI Parameters Amplifier section.
- **Random Interference**: For generating DMRI with DMSI, the following options must be configured under the Random Interference block:
  - **RI State**: Enable the RI state option.
  - **RI Mode**: From the **RI Mode** drop-down list, select **Differential Mode**.

  For configuring the rest of the random interference options, refer to M8054A CMRI/DMRI Parameters Random Interference section.
- **Sinusoidal Interference**: For generating DMRI with DMSI, the following options must be configured under the Sinusoidal Interference block:
  - **SI State (1/2)**: Enable the SI state (1/2) option.
  - **SI Mode (1/2)**: From the **SI Mode (1/2)** drop-down list, select **Differential Mode**.

  For configuring the rest of the sinusoidal interference options, refer to M8054A CMSI and DMSI Parameters Sinusoidal Interference section.
- **De-Embedding** - Refer to M8054A Parameters configuration De-Embedding section.

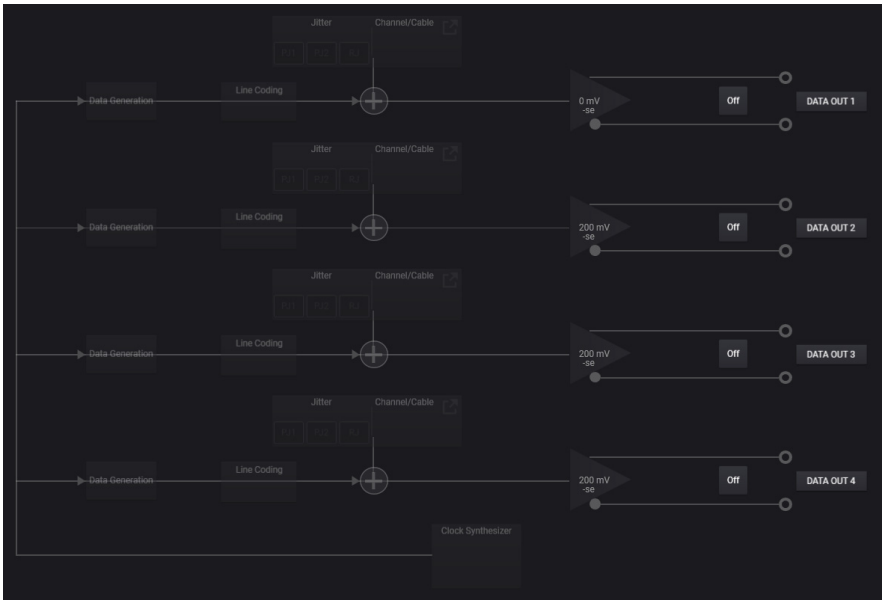
M8054A as External Level Interference (RI/SI) Source

The M8054A is an external level interference source with Random and Sinusoidal modulation. For more details on the M8054A configuration, refer to M8054A Configuration . The M8070B system software allows controlling interference parameters such as amplitude, highest frequency, lowest frequency, crest factor and so on.

Keysight provides a matched directional coupler pair (M8045A-802) and a matched coupler pair (M8045A-803) for injecting the RI or SI signal before or after the channel. Specifications for external level interference sources RI/SI with M8054A can be found in M8040A data sheet.

System View of M8054A

This section describes the block diagram provided by the System View when M8054A module is integrated in M8070B. The System View for M8054A varies on the number of channels available.



The principal parts of the System View are represented by blocks, and these blocks are connected by lines/arrows.

When a block is selected, the corresponding parameter values are displayed under the Parameters pane. The selected block is highlighted by blue borders. For more details, refer to System View .

Controlling M8047B PCI Express Re-driver from M8070B User Interface

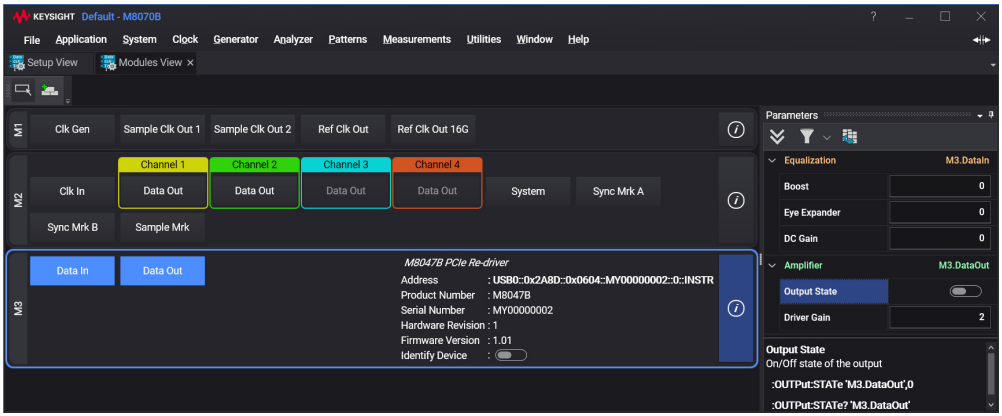
The M8070B system software (version 9.1 or above) allows you to control M8047B PCI express re-driver along with the M8040A modules. In order to control M8047B module, the M8047B module driver must be installed in the M8070B software. The module driver file can be downloaded from Keysight web page www.keysight.com. For details on how to install the M8047B module driver in the M8070B software, refer to the section Manage Instrument Drivers on page 813. Once the M8047B module driver is installed and it is connected to the host computer with USB, it can be accessed via the M8070B software. The Data In ports of the M8047B should be connected to the back channel of your device under test and the Data Out port of M8047B should be connected with the Data In ports of an error detector.

NOTE **The M8047B PCI Express Re-driver requires the presence of additional modules. For more information, refer to *M8047B Data Sheet.***

For complete details on the M8047B PCI Express Re-driver, visit www.keysight.com/find/M8047B.

M8047B in Module View

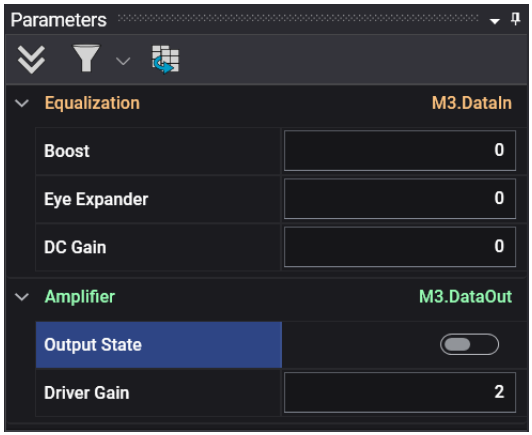
Once the M8047B integration is done, you will see an M8047B PCI Express Re-driver entry in the **Module View**. The following figure shows the **Module View** of M8047B:



The **Identify Device** toggle button enables you to identify which M8047B PCI Express Re-driver on bench corresponds to this particular software module by blinking the status LED on M8047B. When the **Identify Device** toggle button is ON, the M8047B LED will blink. The default setting is OFF.

M8047B Parameters configuration

The M8047B PCI Express Re-driver has the **Data Out** and **Data In** ports. You can use the **Parameters** window to configure these ports.



The following parameters are available to program the M8047B PCI Express Re-driver:

- **Equalization**: The following parameters are available for **Data In**.
  - **Boost**: Sets the equalizer boost. The range for this parameter is 0 - 33.
  - **Eye Expander**: Sets the value of the PAM4 eye expander. The range for this parameter is 0 - 3.
  - **DC Gain**: Sets the equalizer DC Gain value. The range for this parameter is 0 - 3.
- **Amplifier**: The following parameters are available for **Data Out**.
  - **Output State**: Enables or disables the state of the output.
  - **Driver Gain**: Sets the output VOD. The range for this parameter is 0 - 3.

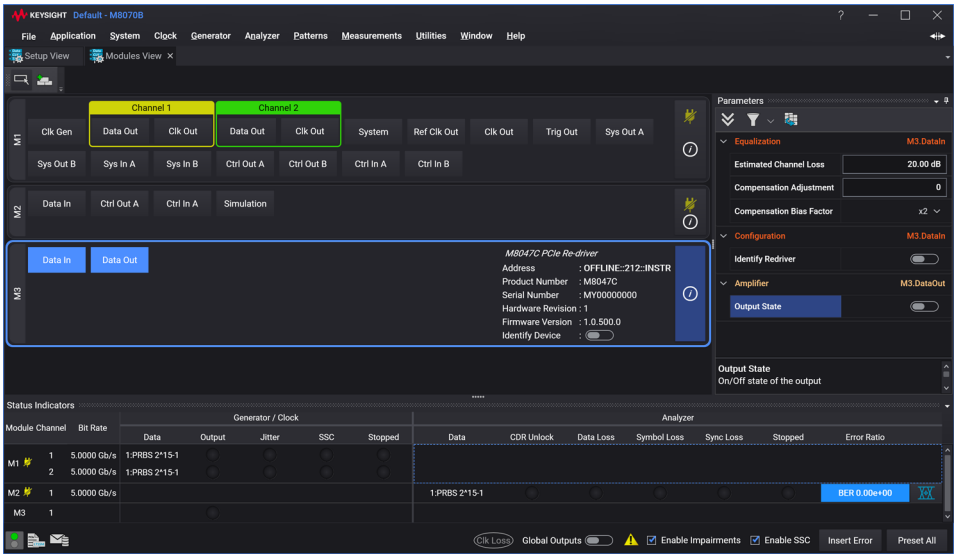
Controlling M8047C PCI Express Re-driver from M8070B User Interface

The M8070B system software (version 11.0 or above) allows you to control M8047C PCI express re-driver along with the M8046A error detector module. In order to control M8047C module, the M8047C module driver must be installed in the M8070B software. The module driver file can be downloaded from Keysight web page www.keysight.com. For details on how to install the M8047C module driver in the M8070B software, refer to the section Manage Instrument Drivers on page 813. Once the M8047C module driver is installed and it is connected to the host computer with USB, it can be accessed via the M8070B software. The Data In ports of the M8047C should be connected to the back channel of your device under test and the Data Out port of M8047C should be connected with the Data In ports of an error detector.

For complete details on the M8047C PCI Express Re-driver, visit www.keysight.com/find/M8047C.

M8047C in Module View

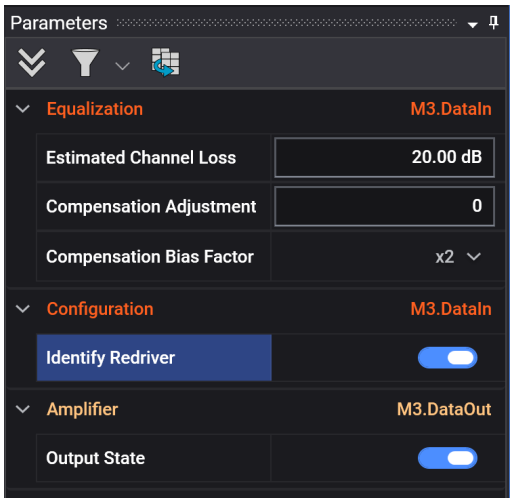
Once the M8047C integration is done, you will see an M8047C PCI Express Re-driver entry in the **Module View**. The following figure shows the **Module View** of M8047C:



The **Identify Device** toggle button enables you to identify which M8047C PCI Express Re-driver on bench corresponds to this particular software module by blinking the status LED on M8047C. When the **Identify Device** toggle button is ON, the M8047C LED will blink. The default setting is OFF.

M8047C Parameters Configuration

The M8047C PCI Express Re-driver has the **Data Out** and **Data In** ports. You can use the **Parameters** window to configure these ports.



The following parameters are available to program the M8047C PCI Express Re-driver:

- **Equalization**:
  - **Estimated Channel Loss**: Sets a nominal estimated loss on the back channel in dB that the user expects to compensate.
  - **Compensation Adjustment**: Allows the user to fine-tune the compensation with respect to the given estimated channel loss.
  - **Compensation Bias Factor**: Defines the factor of the bias current for the equalization.
- **Configuration**:
  - **Identify Redriver**: Identifies redriver by enabling the blinking.
- **Amplifier**:
  - **Output State**: Enables or disables the state of the output.

Extended Sequencing Capabilities in AWGs

Basic Sequencing

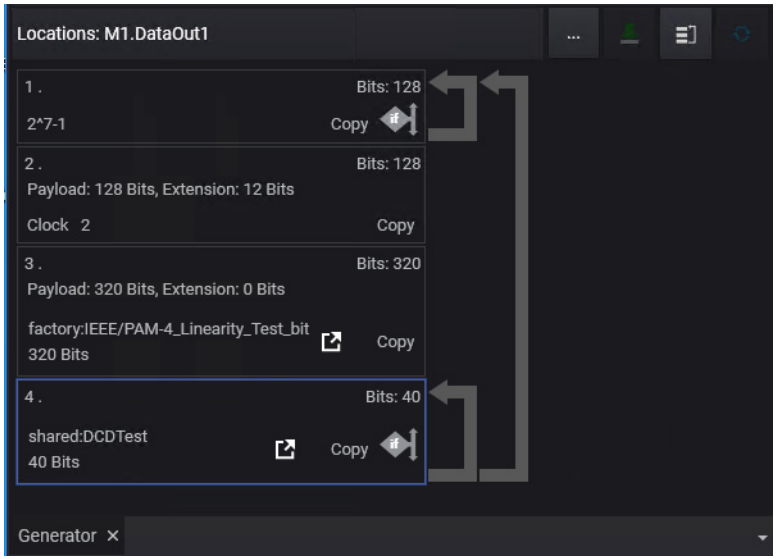
This section describes how patterns are generated in case only a single infinitely looped sequence block is defined. This basic sequencing description is valid for M8194A, M8195A, and M8196A modules.

- PRBS, Static, and Clock sequence block types are repeated with their minimum possible granularity ignoring the number of symbols specified in the sequence block length.
- Memory Patterns and Pulses are created with the chosen pattern length using the sequence block length as the minimum repetition rate.

Extended Sequencing

Pattern Generation

This section describes how the distinct sequence block types are generated when using the enhanced AWG sequencing capabilities in M8070B. Presently, these capabilities are only available with M8195A modules which are configured with the 'SEQ' option meant for sequencing.



- PRBS

  In a looping sequence block, a PRBS pattern is generated using the specified sequence block length as a minimum number of bits and increased to a full repetition of the base PRBS. As an example, a PRBS7-1 with original length of 127 bits and a sequence block length of 200 bits is given. This will generate a PRBS pattern with a length of 254 bits, meaning two PRBS7-1 iterations. These 254 bits are then used as a base pattern for the generated waveform and multiplied as required to fit into an AWG memory segment.

  Non-looping patterns contain the number of sequence bits defined in the sequence block and do not consider the natural PRBS repetition length.

- Memory Pattern

  For memory patterns, only the number of bits that are specified as sequence block length, occur in the resulting pattern. In case the memory pattern has a length of 200 bits while the sequence block length is specified as 100 bits, only the first 100 bit of the memory pattern will be used for generating the data stream.

- Static

  Static segments use the number of bits in the sequence block, either as a minimum repetition length for roll-out in looped sequence blocks or for defining a minimum pattern length in non-looped sequence blocks.

- Clock

  The minimum number of clock symbols are defined by the least common multiple of the clock divider setting and the number of bits specified as sequence block length. In case the line coding is, for example defined as PAM4, the number of bits of a clock sequence block additionally needs to be divisible by the number of bits per symbol which is 2 bit/symbol.

- Pulse

  The pulse pattern considers the number of bits specified as sequence block length as the minimum pattern length. The length of the pulse's high duration is thereby specified by the width property configurable in the sequence block's data properties. In case of a line coding containing more than one bit per symbol, the pulse pattern width and length must be a multiple of the bits per symbol value (For PAM4, this value is 2 bit/symbol).

Block Settings

Sequence Block

A sequence block can contain an arbitrary user defined pattern, but the effective length of such a sequence block is enlarged internally to fit all the granularity requirements. This leads an effectively sent waveform to be separated into two distinct parts. One part is dubbed as payload (containing the desired pattern) while the other part is called extension (required to meet hardware limitations).

It is ensured that the sequence block length always contains an integral number of symbols. Additionally, the number of sequence block symbols is divisible by two, which allows to stay in sync with a half rate clock signal across multiple sequence blocks.

Sequence Block

Payload	Extension

Traditionally, a sequence block contains only the desired pattern but for M8195A modules, a non-looped sequence block contains a payload and extension pattern part.

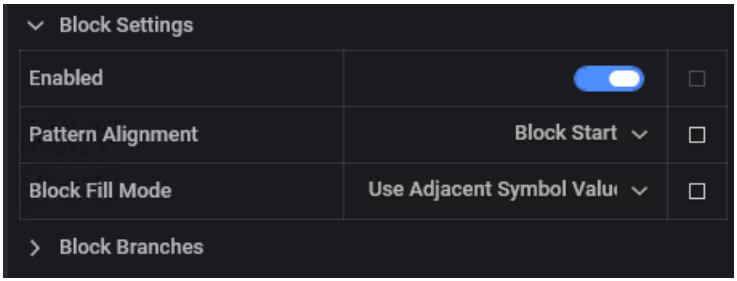
- Payload

  It consists of the user-defined pattern. The data sent during the payload duration is provided from a memory pattern location, PRBS selection, etc.

  The location of the payload inside a sequence block is selectable. Following are the available choices for pattern alignment:

  - Align payload to sequence block start
  - Align payload to sequence block end
- Extension

  The extension part is necessary because of limitations such as sequencer linkage across multiple channels, AWG sample memory granularities, module-wide sample rate and so forth. It extends the waveform sent during playback of a non-looped sequence block to match all preconditions.



The data content of the extension pattern is selectable. Following are the selectable block fill modes:

- Use Adjacent Symbol Value

  Depending on payload alignment, this setting uses the first or the last symbol value of the payload pattern for filling up the sequence block.

  Using this option will generally produces the shortest sequence block duration with the smallest extension pattern.

- Repeat Pattern

  This setting repeats the payload inside the extension block. Using this setting, the entire sequence block containing an integral number of payload repeats. This setting produces the same output, independent of the selected payload alignment mode.

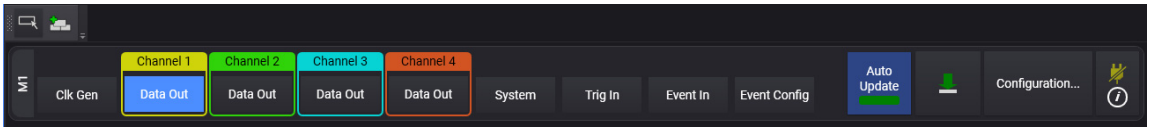
  This option generally causes the extension pattern length to increase as it needs to allow for accommodating multiples of the payload pattern length.

- Fill Extension with Clock Signal

  This option fills the extension pattern with a half rate clock.

Event Configuration

The M8070B software system supports some of the hardware triggering capabilities of M8195A. These features can be configured via the modules view when accessing the 'Trig In', 'Event In', or 'Event Config' functional blocks.



Trig In and Event In

These blocks allow configuration of the input comparator state of the AWG module by defining a decision threshold voltage and an input detection polarity. An event is asserted from the respective input in case the detected voltage transitions above the defined threshold voltage for positive polarity or below the threshold voltage for negative polarity.

Event Config

In this functional block, it is possible to configure whether "Trig In" or "Event In" is connected to trigger a conditional break event in a multi-block sequence. Using M8195A SFP (Soft Front Panel), the advance event corresponds to the conditional break event in M8070B.

By using the break command from the sequence editor it is possible to fire the "Force (Advance) Event" in the SFP. Additionally, it is possible to enable or disable the hardware advance event by using the "Advance Event State" switch.

SCPI Commands

The advance sequencing can also be executed using the remote programming. For details of these commands, refer to *M8000 Series Programming Guide*.

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User Guide

5 Setting up Generator

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KEYSIGHT TECHNOLOGIES

Overview

The M8020A/M8040A/M8050A generator generates an output signal based on a data pattern. It has the following possibilities for generating an output signal:

- Providing a wide range of clock frequencies

  You can use the generator's internal clock or an external clock for defining the frequency of the outgoing stream.

- Distorting the signal by adding jitter

  You can connect an external delay control device (for example a function generator) to add jitter to the generated signal.

- Adding errors to the output stream

  The M8020A/M8040A/M8050A can be set up to insert errors into the outgoing stream either internally, according to an external signal, or manually (from the operator).

- Run-time switching between two patterns

  You can set up two patterns and switch between them during runtime either automatically, according to an external signal, or manually.

- Suppressing the output stream

  The output signal can be suppressed according to an external signal.

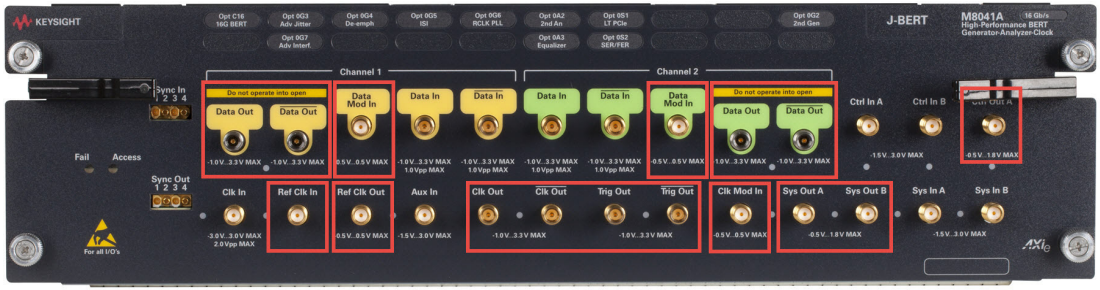
The M8020A/M8040A/M8050A generator also provides output ports that let you connect an external instrument, such as an oscilloscope.

M8020A Generator Ports

The M8020A generator ports are used to set the generator's clock frequency and to define the output signal with respect to jitter, error insertion and signal output. In addition, the generator's output ports are also used to supply a clock signal and trigger (for example, analyzer), and an arbitrary data signal for testing your device.

The M8020A provides a high level of integration with built-in clock synthesizer, deemphasis, jitter and level interference. It allows you to set the parameters for the built-in generator parameters such as amplifier, deemphasis, HF and LF jitter, common mode interference and differential mode interference.

The following figure shows the M8020A generator's ports.



The M8020A generator's ports include the following:

- Ref Clock In

  The Ref Clk In input can be used as reference frequency or as external system frequency directly for the instrument. An external provided signal can be measured at that input. This input is tightly involved in the system frequency generation.

- Data Out and $\overline{\text{Data Out}}$

  The differential data output serve as device stimuli and can be set up so that they are compatible with a variety of logic families. With respect to $\overline{\text{Data Out}}$, Data Out has inverted logic.

- Clock Out and $\overline{\text{Clock Out}}$

  The differential clock output serve as frequency (bit rate) reference and can be set up so that they are compatible with a variety of logic families. With respect to Clock Out, $\overline{\text{Clock Out}}$ has inverted logic.

- Trigger Out and $\overline{\text{Trigger Out}}$

  This port allows you to trigger another device (for example, an oscilloscope) and can be set up so that they are compatible with a variety of logic families. Trigger Out has more modes, e.g. sub rate clock to be used as ref clock for a DUT. With respect to Trigger Out, $\overline{\text{Trigger Out}}$ has inverted logic.
- Sys Out A/B

  The system level control outputs used to trigger events to the DUT or external instruments.
- Ctrl Out A

  The control output port provides the Error Output functionality.

The complementary outputs can be used when:

- additional output capability is needed for an instrument such as an oscilloscope or digital communication analyzer.
- your device requires differential inputs.

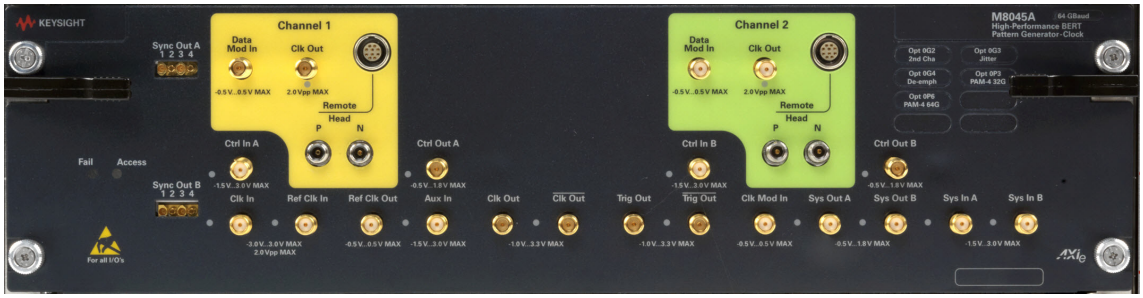
NOTE **The Generator's Data Out, Clock Out, Trigger Out and ports must be terminated with 50 Ω if they are not connected.**

M8040A Generator Ports

The M8040A generator ports are used to set the generator's clock frequency and to define the output signal with respect to jitter, error insertion and signal output. In addition, the generator's output ports are also used to supply a clock signal and trigger (for example, analyzer), and an arbitrary data signal for testing your device.

The M8040A provides a high level of integration with built-in clock synthesizer, deemphasis, jitter and level interference. It allows you to set the parameters for the built-in generator parameters such as amplifier, deemphasis, HF and LF jitter, common mode interference and differential mode interference.

The following figure shows the M8040A generator's ports.



The M8040A generator's ports include the following:

- Remote Head - P and N Ports

  The P and N ports of each channel must be connected to the M8057A/B.

- Clk Out1 and Clk Out 2

  These are the Clk Out ports of channel 1 and 2, respectively. It can generate either a Clean Clk or all timing impairments like Data Out.

- Ref Clock In

  The Ref Clk In input can be used as reference frequency or as external system frequency directly for the instrument. An external provided signal can be measured at that input. This input is tightly involved in the system frequency generation.

- Ref Clock Out

  The Ref Clk Out is used to provide a 10 MHz or 100 MHz reference clock to the DUT or other test equipment.

- Clock Out and $\overline{\text{Clock Out}}$

  The differential clock output serve as frequency (bit rate) reference and can be set up so that they are compatible with a variety of logic families. With respect to Clock Out, $\overline{\text{Clock Out}}$ has inverted logic.
- Trigger Out and $\overline{\text{Trigger Out}}$

  This port allows you to trigger another device (for example, an oscilloscope) and can be set up so that they are compatible with a variety of logic families. Trigger Out has more modes, e.g. sub rate clock to be used as ref clock for a DUT. With respect to Trigger Out, $\overline{\text{Trigger Out}}$ has inverted logic.
- Sys Out A/B

  The system level control outputs used to trigger events to the DUT or external instruments.
- Ctrl Out A

  The control output port provides the Error Output functionality.

The complementary outputs can be used when:

- additional output capability is needed for an instrument such as an oscilloscope or digital communication analyzer.
- your device requires differential inputs.

NOTE **The Generator's Data Out, Clock Out, Trigger Out and ports must be terminated with 50 Ω if they are not connected.**

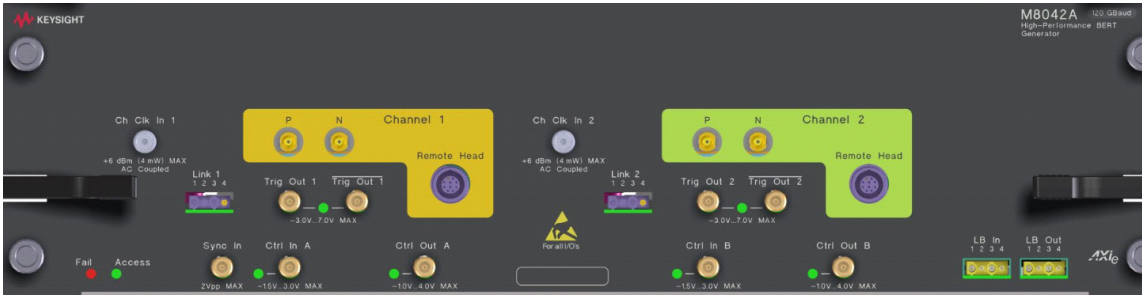
M8050A Generator Ports

The M8050A generator ports are used to set the generator's clock frequency and to define the output signal with respect to jitter, error insertion and signal output.

In addition, the generator's output ports are also used to supply a clock signal and trigger (for example, analyzer), and an arbitrary data signal for testing your device.

The M8050A provides a high level of integration with built-in clock synthesizer, deemphasis, jitter and level interference. It allows you to set the parameters for the built-in generator parameters such as amplifier, deemphasis, HF and LF jitter, common mode interference and differential mode interference.

The following figure shows the M8050A generator's ports.



The M8050A generator's ports include the following:

- **Data Out 1, Data Out 2** - This port characteristics for M8042A with M8058A/M8059A/M8068A/M8069A. Values apply at the end of the reference cable at the outputs of the remote heads M8058A, M8059A, M8068A or M8069A.
- **Ctrl In A, Ctrl In B** - This port can be selected as: sequence trigger, error insertion.
- **Ctrl Out A, Ctrl Out B** - This port provides a pulse or static high/low if used from sequencer.
- **Trig Out 1, Trig Out 2** - This port can be used in different modes:
  - Divided clock with dividers
  - Sequence block trigger
  - Pulse mode triggered by sequencer (only if memory pattern is used)

- "Pulse on PRBS" mode NRZ only. Matched pattern without ignoring defined bits (only if algorithmic pattern is used)

The trigger output 2 is only available for the two-channel version of M8042A.

- **Link1, Link 2** - This port enables interactive link training with low latency between a pattern generator channel and a M8046A analyzer module. Requires cable M8051A-801. LINK 2 is only available for the two-channel version of M8042A.
- **Ch Clk In 1/2** - This port is used to connect with the M8009A clock module. The channel clock input 2 is only available for the two-channel version of M8042A.
- **Sync In** - This port is used to connect with M8009A clock module.
- **LB In, LB Out** - This port is needed for communication connected to the previous AXIe chassis. The local bus output is needed for communication connected to the next AXIe chassis.

Understanding Pattern Generator Features

The following sections describe the pattern generator features.

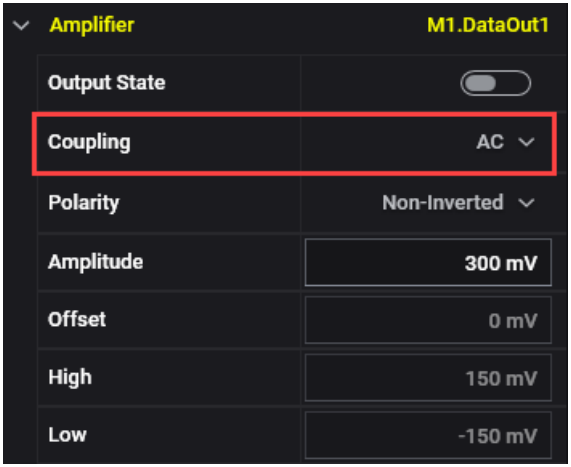
Output Termination Modes of M8045A with M8057A/B

The following modes are available:

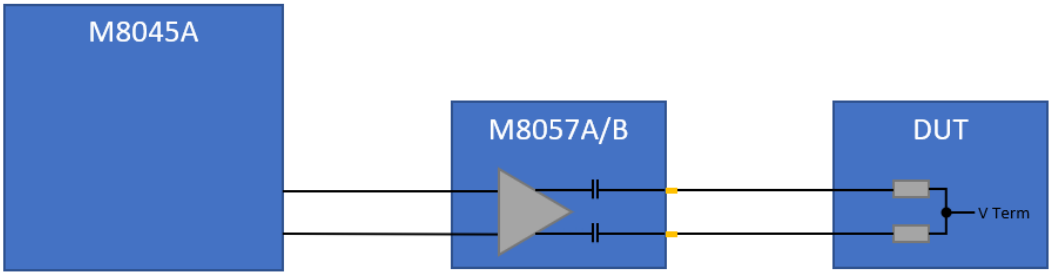
- AC Coupled
- DC Coupled, Unbalanced
- DC Coupled, Balanced

AC Coupled

- In the M8045A module, go to **Parameters > Amplifier > Coupling > AC**.



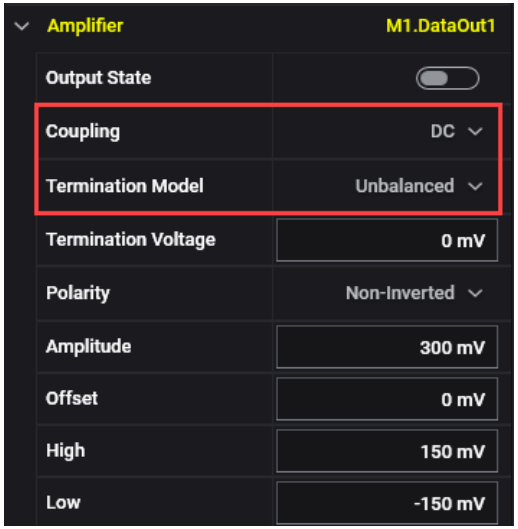
The following block diagram displays the AC coupling:



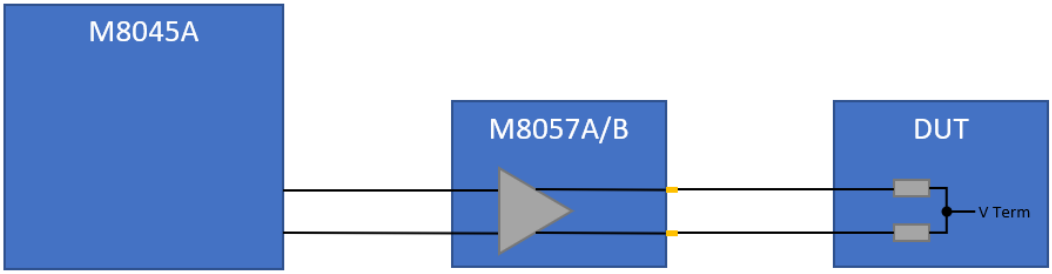
The main difference to M8020A is that the AC coupling is in the instrument. External AC coupling is still possible but not necessary.

DC Coupled, Unbalanced

- In the M8045A module, do the following:
  - *a* Go to **Parameters > Amplifier > Coupling > DC**.
  - *b* Go to **Parameters > Amplifier > Termination Model > Unbalanced**.



The following block diagram displays the DC coupling with unbalanced termination model:

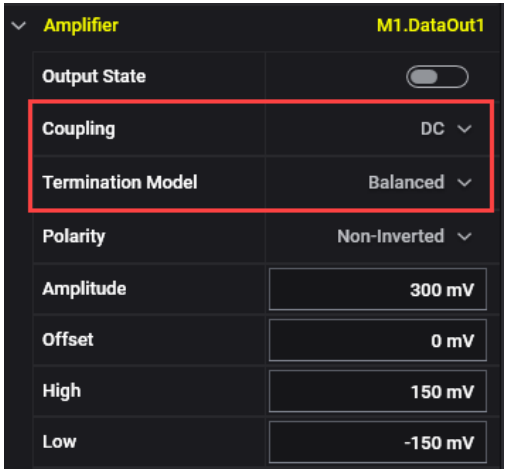


Limits for Termination Impedance:

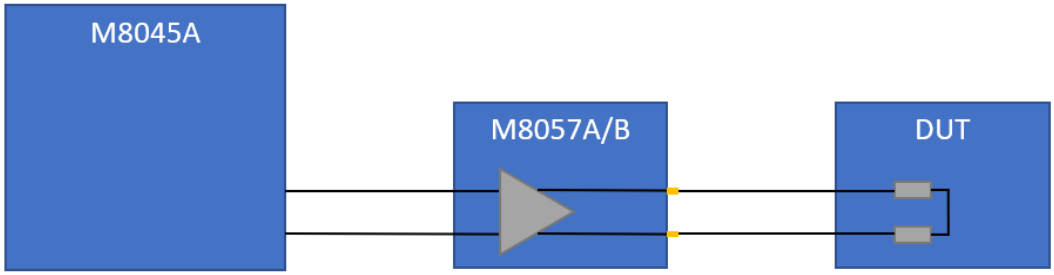
40 Ohm – 65 Ohm

DC Coupled, Balanced

- In the M8045A module, do the following:
  - *a* Go to **Parameters > Amplifier > Coupling > DC**.
  - *b* Go to **Parameters > Amplifier > Termination Model > Balanced**.



The following block diagram displays the DC coupling with balanced termination model:



Limits for Termination Impedance:

70Ohm – 130 Ohm

Operation into open is possible for these ranges:

- Output amplitude max. 450 mV
- Offset 0 – 370 mV

Understanding the Output Protection Circuit

The M8041A, M8045A, M8042A and M8051A J-BERT modules offers a huge flexibility for external termination schemes and external termination voltages to address common technologies. For details, please refer to the respective M8020A, M8040A and M8050A Data Sheet.

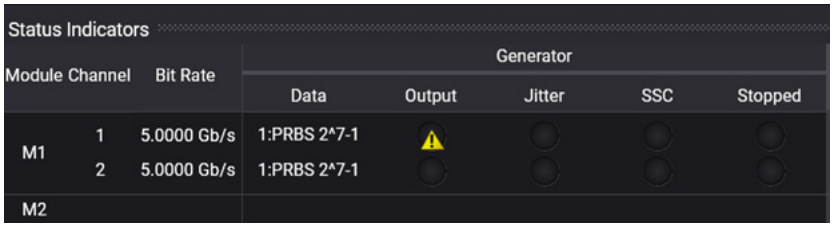
An internal protection circuit continuously monitors the voltages of clock, data and trigger output. It becomes active and turns off the output(s) if the externally applied termination voltage does not match the respective setting (any longer).

NOTE

The M8020A/M8040A/M8050A output port groups (Data, Clock and Trigger Out) have their own protection circuit. As a consequence, if an output voltage violation occurs at any of the output port(s), then the respective output port group gets disabled or stops working. The output(s) needs to be actively (via GUI or remotely) re-enabled after the fault condition has been removed.

If an output voltage violation occurs, the output(s) is switched off, which means to a "high impedance" condition. When it gets switched on again (manually by the user) it again follows the standard enabling procedure with termination voltage(s) & impedance checks.

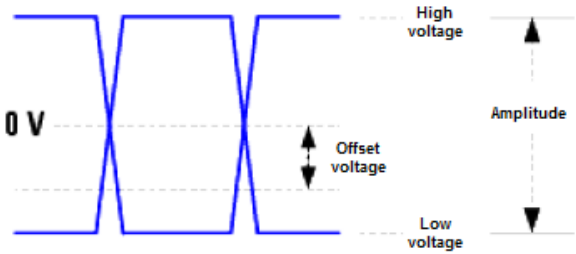
A warning icon appears in the **Status Window** as shown in the following figure:



Understanding the Output Level Parameters

The following figure shows the parameters of a Data, Clock, or Trigger output signal.

As shown in this figure, the signal output levels have the following components:



- High voltage is the upper voltage level of the signal.
- Low voltage is the lower voltage level of the signal.
- Offset voltage is the offset of the average voltage level from 0 V.
- Amplitude of the signal.

When adjusting the output levels, it is important to understand the concept of how the M8020A/M8040A/M8050A handles voltages.

Changing the Amplitude

Typically, during tests, when you adjust the amplitude, you want to keep the offset constant. This keeps the ideal sampling point within the eye. The M8020A/M8040A/M8050A handles this by keeping offset voltage constant when amplitude is changed.

Changing the Output Levels

On the other hand, you may want to adjust the output voltage level without changing the amplitude. The M8020A/M8040A/M8050A handles this by keeping amplitude constant when offset voltage is changed and high/low voltage are accordingly adjusted.

Voltage Level Restrictions

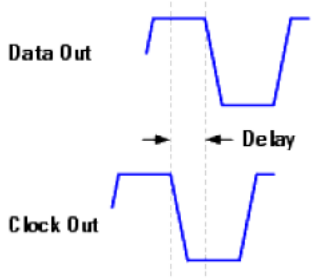
The M8020A/M8040A/M8050A cannot generate a signal that has voltage levels out of range. If you try to enter a value for one parameter that would put another parameter out of limits, the M8020A/M8040A/M8050A rejects the change. This could happen, for example, if low voltage is already at the minimum, and you try to lower either of high voltage or low voltage, or increase amplitude.

Understanding Delay and Crossover

The Delay feature is supported by M8020A/M8040A/M8050A and the crossover feature is supported by M8020A only. It provides the possibility of modifying the output data signal by varying the signal's delay to the clock signal, and the signal's crossover.

Delay

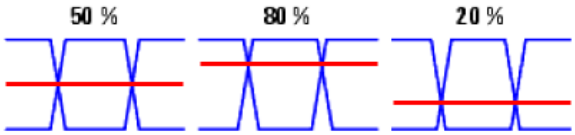
The exact time delay through a test setup can vary. The delay function allows you to compensate for this by adjusting the active edge of the trigger output relative to the clock/data outputs. This varies the phase relationship of the data and clock outputs (causes the data to have a certain time delay after the clock pulse). The higher the delay, the greater the time difference between the clock signal and the data signal. The delay can be adjusted by the generator’s Data Out 1 and Data Out 2 ports.



Crossover

Crossover is the voltage level where the overlapped rising and falling edges of the logic levels intersect. This adjustment varies the widths of the logic highs and lows.

The following figure shows examples of crossover at 50 %, 80 %, and 20 %:



Note that the crossover feature is not supported by M8040A.

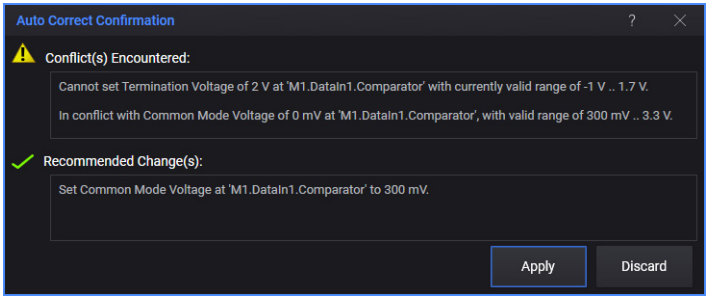
Why Incorrect Terminations Could Damage Your Device

Choosing wrong terminations may cause your device to output voltage levels that are not as expected. It may also cause excessive current or current flow in the wrong direction, which can damage your device.

Note that an internal protection circuit becomes active if the termination voltage is wrongly adjusted. The protection circuit sets the output voltages to safe levels, typically:

Vhi = Vlo = Vterm = externally measured termination voltage.

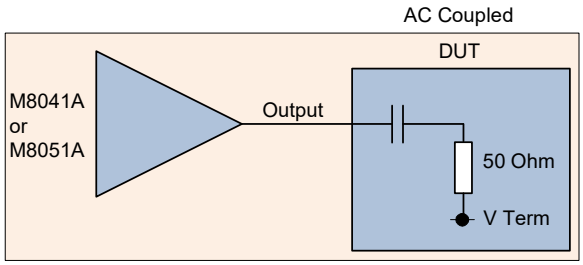
If you adjust the termination voltage, and try to enter value(s) which are outside of the currently allowed window, the **Auto Correction Confirmation** message box will pop up with respective apply and discard options as shown in the following figure:



M8020A AC Coupling and Bias Tees

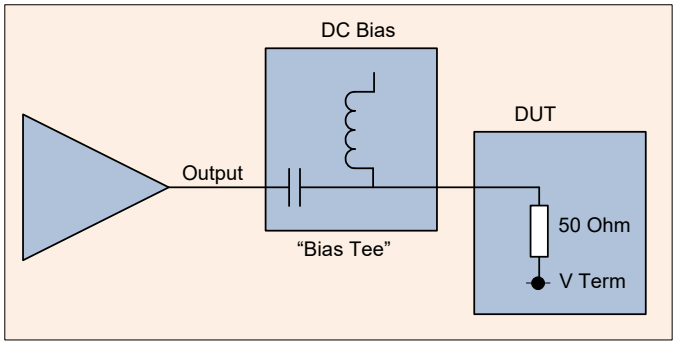
The generator's outputs are always internally DC-coupled; even when AC termination is selected. For this reason, caution must be taken when connecting your instrument to a device or test setup.

The diagram below shows a device that is AC coupled. Note that the capacitor is part of the test setup.



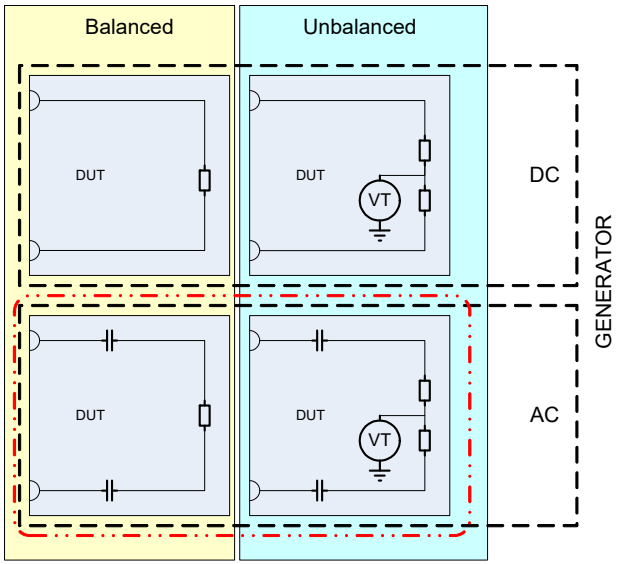
You can use an external bias to power your device. You must ensure, however, that the network is oriented correctly. If it is not, your device or instrument may get damaged.

The following diagram shows a bias tee that is positioned correctly. Notice that the generator's outputs are protected by the blocking capacitor.



M8020A/M8040/M8050A Coupling Modes

The following drawing is an example of the external DUT connected to the generator output for the different possible settings.



VT = Termination Voltage

This figure shows what the generator expects to be externally connected as DUT, with respect to the different selectable termination models.

For AC-coupled mode (see red box above), the instrument actually cannot and does not need to distinguish between these two termination schemes. Therefore the drop-down box **Termination Model** is not shown and active within the GUI when the AC coupled mode is selected.

There are certain impedance/voltage limits you need to keep in order to be able to turn on (enable) the output(s).

Whenever an output amplifier is turned on, the external DC resistance as well as the external termination voltage is measured and calculated.

These are the impedance/voltage limits for various modes / configurations:

- **DC Coupling Unbalanced:** The measured externally connected resistance should be within the allowed range which is between 40 to 65 Ω here. Also, if an external termination voltage is detected that is not within the allowed ±100 mV tolerance window, the output(s) will not turn on.
- **DC Coupling Balanced:** The measured externally connected resistance should be within the allowed range which is between 70 to 130 Ω here. In this DC Coupling Balanced mode there is an exception implemented, that allows the output(s) to drive high impedance ('into open'). For this, the set maximum amplitude should be below 450 mV, and the offset setting should be between 0-370 mV.
- **AC Coupling:** When using the AC coupled mode, you must apply an external DC blocking capacitor. When AC coupling is selected, internal coupling capacitors are present in the remote head; however, external DC blocking capacitors may still be required depending on the measurement setup or application. Here the external DC resistance must be greater than or equal to 300 Ω, with the HF resistance being ~50 Ω (single - ended) or ~100 Ω (differential). For M8040A and M8050A, the internal AC coupling capacitance is 100 nF.

Setting up Terminations

Before you can start sending signals to your device, you have to choose the proper termination mode. To do so:

1 Go to the **Menu Bar** > **Generator** and then select **Data Out**.

2 Select **Amplifier** functional block from the **Parameters** window.

3 Provide the DUT's termination settings.

4 Provide termination voltage.

CAUTION Selecting the wrong termination may damage your device.

5 Connect the DUT's input ports to the M8020A/M8040A/M8050A's output ports.

CAUTION Do not apply external voltages to the generator outputs.

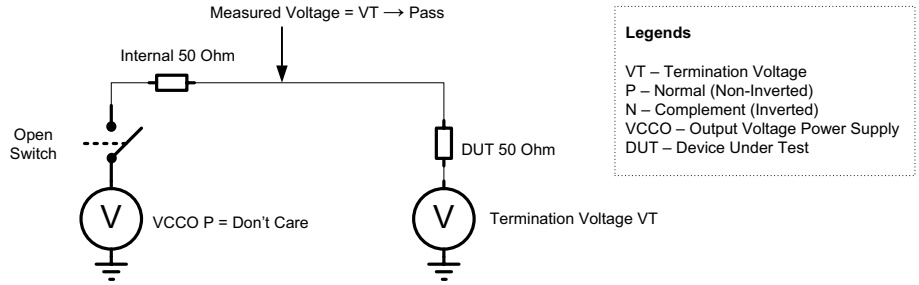
Output ports of the generator that are not connected to another device must be terminated with 50 Ω to prevent the M8020A/M8040A/M8050A from damage. If outputs are disconnected they are usually not turned on because the output enable check detects the misconfiguration. If outputs are disconnected after they have been turned on the protection circuit might get triggered depending on the specific configuration. In this case the output will be switched off. This is an emergency scenario and should never be a normal habit. It can be switched on again (manually by the user) after removing the fault condition, it again follows the standard enabling procedure with termination voltage(s) & impedance checks.

NOTE When the Data Out and Data In ports are not connected and are terminated with 50 Ω resistor, the Data Loss and Sync Loss indicators may appear red or blink. This is normal behavior and does not indicate a hardware fault.

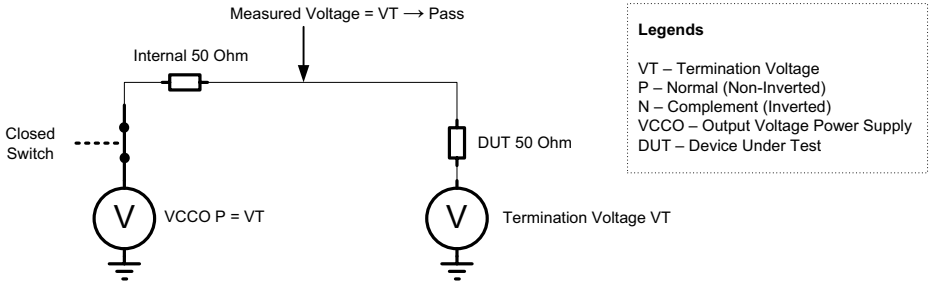
DC Check (Unbalanced/Balanced Termination) for M8020A/M8040A/M8050A

DC Check for Unbalanced Termination

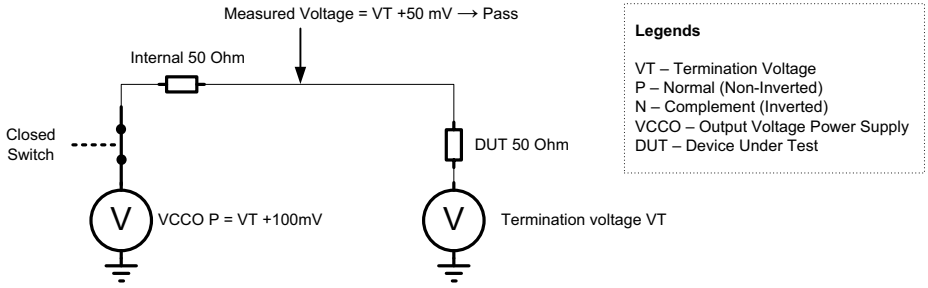
Step 1 If the Measured Voltage = VT –> Pass, go to Step 2.



Step 2 If the Measured Voltage = VT –> Pass, go to Step 3.



Step 3 If the Measured Voltage = VT + 50 mV –> Pass, turn on the output driver.



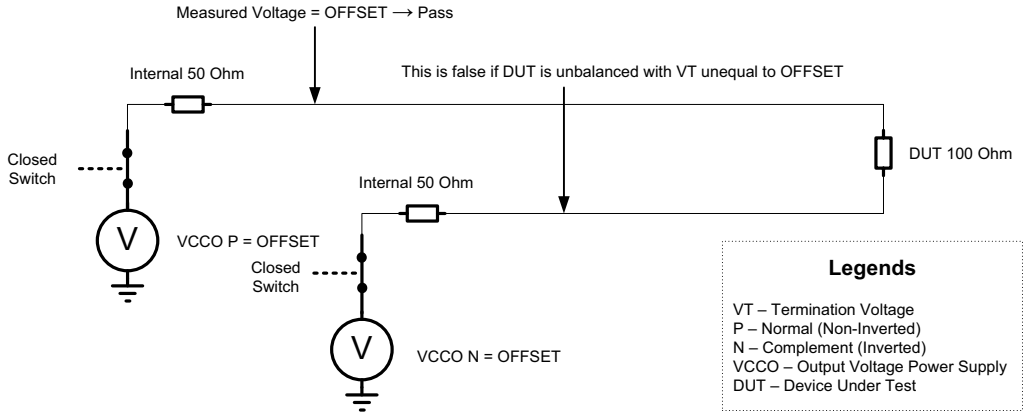
NOTE

In the above diagrams, only normal output is shown. However, the DC check however is done for normal and complement output. In general, the both outputs (P/N) need to be terminated the same way.

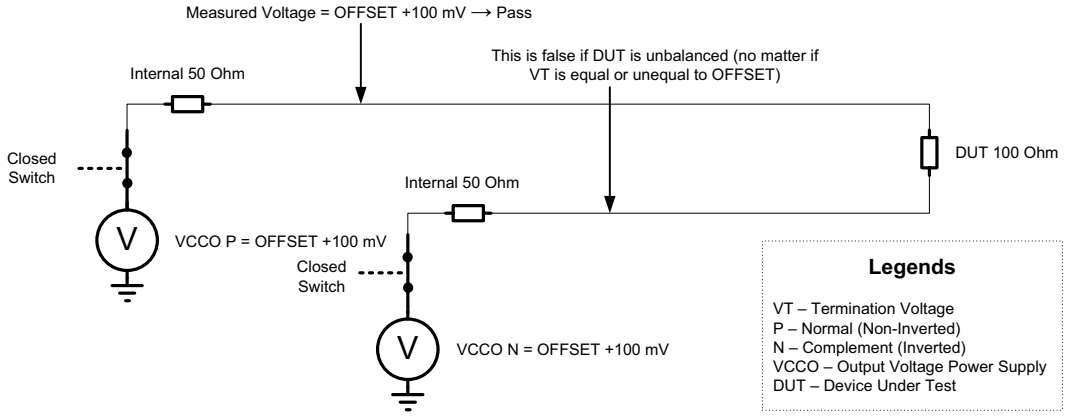
In single ended use case for better convenience the unused output can be terminated with 50 Ohm into GND although termination voltage of used output might not be zero. This is only true as long as the offset voltage is between +1V and -1V. The mismatch is detected during the test and is compensated internally. This is implemented in order to make the termination of unused outputs easier.

DC Check for Balanced Termination

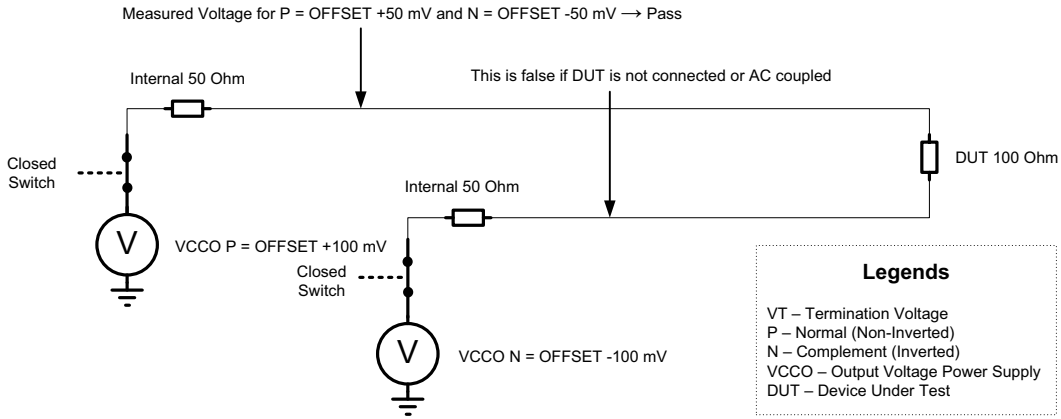
Step 1 If the Measured Voltage = OFFSET -> Pass, go to Step 2. However, this is false if DUT is unbalanced with VT unequal to OFFSET.



Step 2 If the Measured Voltage = OFFSET + 100 mV -> Pass, go to Step 3. However, this is false if DUT is unbalanced (no matter if VT is equal or unequal to OFFSET).



Step 3 If the Measured Voltage for P is OFFSET +50 mV and for N is OFFSET -50 mV -> Pass. Turn on the output driver. However, this is false if DUT is not connected or AC coupled.



Adjust Output Levels (optional)

Data, Clock and Trigger Out offset and voltage levels can be adjusted. This is typically done when you want to tune your BER measurement or stress the device.

You can adjust the related parameters of the data and clock amplitudes and offsets on the GUI.

To enter specific values for the outputs from the keyboard:

1 Go to the **Menu Bar** > **Generator** and then select **Data Out** and **Trigger Out** ports. Once more, go to the **Menu Bar** > **Generator** and then select **Clock Out** port.

2 Select **Amplifier** functional block from the **Parameters** window.

3 Select coupling as **DC.**

4 Select termination model as **Unbalanced**.

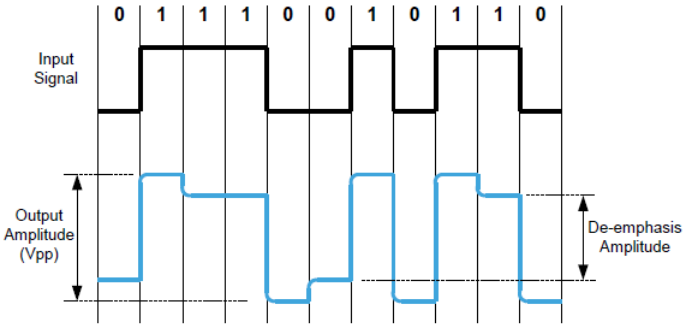
5 Enter the desired termination voltage.

NOTE If the standard enabling procedure with termination voltage(s) and impedance checks fails the output(s) will stay off. In this state the output resistance is "high impedance". It can be switched on again (manually by the user) after removing the fault condition, it again follows the standard enabling procedure with termination voltage(s) and impedance checks.

Deemphasis Signal Generator

The M8020A/M8040A/M8050A has a built-in deemphasis signal generator that can be connected between the Data Out port of the generator and the DUT.

Deemphasis is a method that reduces the voltage of a digital signal if the generated level is high or low for more than one clock period. The principle is illustrated in the following figure.



The deemphasis amplitude is specified as a fraction of the output amplitude (in percent or dB).

Post-cursor deemphasis

The figure above refers to a so-called post-cursor deemphasis. You may wish to know how that is generated.

- One branch has a programmable amplifier to produce the desired output voltage (Peak to Peak Voltage).

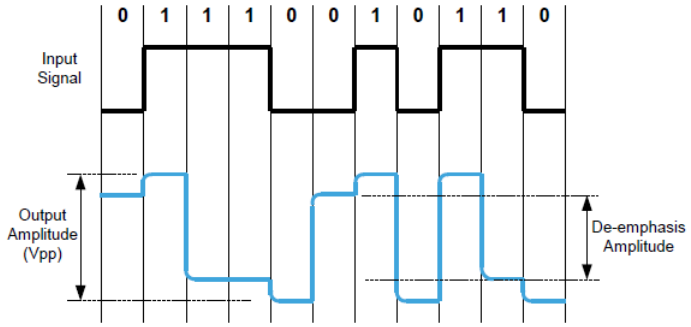
- The other one has an adjustable delay (automatically set to one signal clock period) and a programmable inverting attenuator/amplifier to produce the delayed signal with a lower voltage swing.

Finally, the signals of both branches are added. This means, the delayed signal voltage is subtracted from the specified peak-to-peak amplitude.

Pre-cursor deemphasis

It is also possible to convert the input signal to a pre-cursor deemphasized signal.

This can be done by setting the output voltage swing to the desired deemphasis amplitude and specifying a negative amplitude ratio (an amplification). This inverts the roles of the two branches. The delayed signal has now a larger amplitude than the direct signal. A waveform example is illustrated in the following figure.



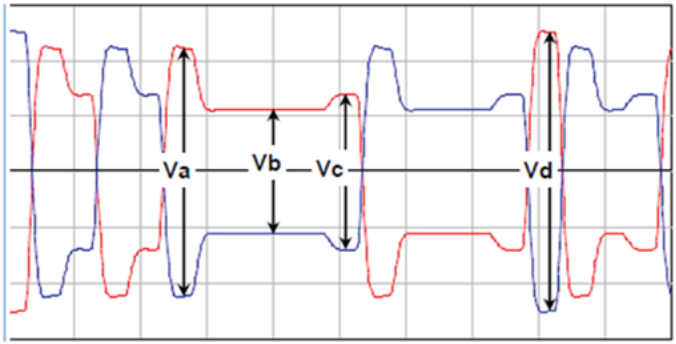
When pre-cursor deemphasis is generated this way, the complementary Output of the Deemphasis Signal Converter becomes the normal output and vice versa.

CAUTION

Be very careful if you set the deemphasis ratio to amplification! In this case, there is no indication of the peak-to-peak voltage applied to the DUT. You need to calculate or measure the output signal voltage precisely. Otherwise you might damage your device.

Deemphasis on 1 pre-cursor and 1 post-cursor

The following example illustrates the output of the differential signal with variable deemphasis on 1 pre-cursor and 1 post-cursor generated by M8020A Deemphasis.



Controlling the Deemphasis

To control the deemphasis function:

1 Go to the **Menu Bar** > **Generator** and then select **Data Out**.

2 Select **Deemphasis** function block from the **Parameters** window.

M8070B Factory Deemphasis Profiles

Table 53 on page -383 lists the deemphasis profile files which are available at the following location (Factory folder) when the M8070B software is installed:

Location: C:\Users\<username>\Documents\Keysight\M8070B\Workspaces\Default\Factory\SharedResources\TxFFEDeemphasisPresets

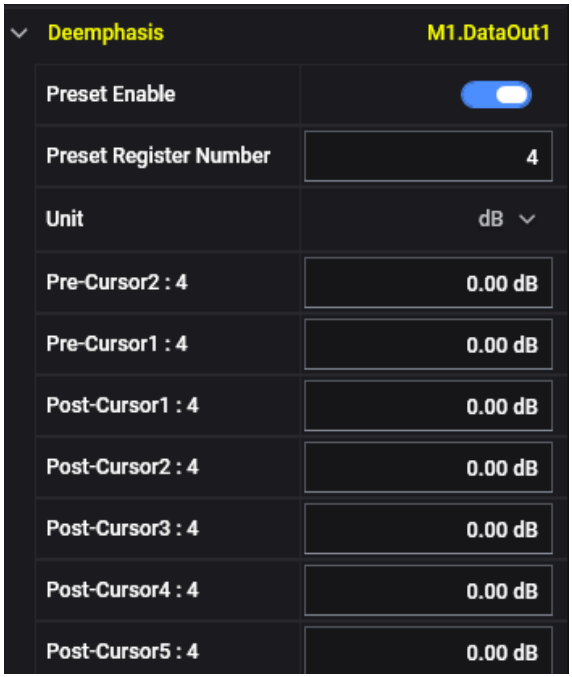
Table 53 Deemphasis profile files

Deemphasis Profile File	Description	Instrument Assembly
DeemphasisPresetProfile_7Cursors.xml	50 Presets with the Main Cursor at 3.	M8050A
Default_2pre_2post.xml	Dummy Tx FFE profile with 2 pre-cursors and 2 post-cursors.	M8040A
Default_3pre_3post.xml	Dummy Tx FFE profile with 3 pre-cursors and 3 post-cursors.	M8040A
USB4.xml	USB4 Gen2/Gen3 TX FFE preset table as per the USB4 Version 2.0 specification.	M8040A
USB4_7Cursors.xml	USB4 Gen2/Gen3 TX FFE preset table as per the USB4 Version 2.0 specification.	M8050A
USB4_80G.xml	USB4 Gen4 TX FFE preset table as per the USB4 Version 2.0 specification.	M8040A
USB4_80G_7Cursors.xml	USB4 Gen4 TX FFE preset table as per the USB4 Version 2.0 specification.	M8050A

M8020A Deemphasis

You can use the **Preset Enable** button to enable/disable changing the deemphasis preset register number. Once the **Preset Enable** option is enabled, you can set the preset register number. There are 31 preset registers available addressed by a register index of 0 up to 30. The tap values of the ‘current’ preset register are shown at the output. Preset register 0 is the default register. Supported preset values for M8041A, M8051A and M8062A are 0 - 30.

You can toggle between dB (decibel) and % (percent). Toggling does not change the value. The **Deemphasis** function block also allows you to set the “Positive” or “Negative” polarity for deemphasis.



M8045A Deemphasis

The M8045A provides built-in 5 taps deemphasis with positive and negative cursors based on a finite impulse response (FIR) filter. You are allowed to enter the deemphasis values in terms of coefficient values.

Table 54 Specifications for multi-tap deemphasis

	NRZ	PAM4
Deemphasis taps	5 taps, can be adjusted for each channel independently	
Coefficient 0	0.0 to ± 0.45	0.0 to ± 0.45
Coefficient 1	0.0 to ± 0.45	0.0 to ± 0.45
Coefficient 2	0.3 to 1	0.3 to 1
Coefficient 3	0.0 to ± 0.45	0.0 to ± 0.45
Coefficient 4	0.0 to ± 0.45	0.0 to ± 0.45
Cursor coefficient resolution	0.01	0.01

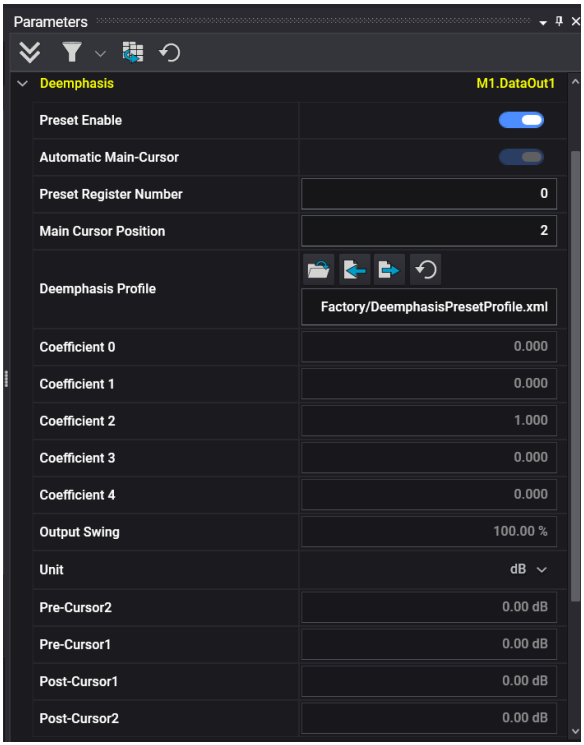
You can use the **Preset Enable** button to enable/disable changing the deemphasis preset register number. Once the **Preset Enable** option is enabled, you can set the preset register number. There are 50 preset registers available addressed by a register index of 0 up to 49. The tap values of the ‘current’ preset register are shown at the output. Preset register 0 is the default register. Supported preset values for M8045A and M8046A are 0 - 49. The presets 48 and 49 represent low-swing configurations and are the exception to the rule that the sum of the absolute value of all coefficients must be equal to 1.

Controlling the M8045A Deemphasis

To control the M8045A deemphasis function:

1 Go to the **Menu Bar** > **Generator** and then select **Data Out**.

2 Select **Deemphasis** function block from the **Parameters** window. The following **Deemphasis** parameters will be shown:



M8045A supports five deemphasis cursors, with an adjustable main-cursor position between cursor 1 and cursor 3. This allows selecting the following configuration:

Main Cursor Position	Number of Pre-Cursors	Number of Post-Cursors
1	1	3
2	2	2
3	3	1

You can enter the deemphasis values in terms of coefficient values. Once you enter the coefficient values, the pre-cursor and post-cursor values are automatically reflected in the corresponding fields. Once the **Automatic Main-Cursor** button is enabled, you are not allowed to adjust the main cursor as it is automatically calculated. However, to change the values for main cursor, you need to disable the **Automatic Main-Cursor** button. You are allowed to toggle between dB (decibel) and % (percent). Toggling does not change the value.

Set the values as following:

- **Automatic Main-Cursor**: Enables automatic calculation of the main cursor.
- **Preset Register Number** - Selects a deemphasis preset register. Supported preset value for M8045A is 0 - 49.
- **Main Cursor Position**: Sets the main cursor position. This can be changed from 1 to 3. The default is value 2.
- **Deemphasis Profile** - Selects the deemphasis preset file from the M8070B workspace (Factory, Current or Shared folder). You are allowed to modify the deemphasis preset values when the deemphasis preset file when loaded from the “Current” or “Shared” folder. All modification made are directly saved to the file. However, when the deemphasis preset file when loaded from the “Factory” folder, you are not allowed to modify the deemphasis preset values (read only state).
- **Coefficient 0**: Controls the filter coefficient 0.
- **Coefficient 1**: Controls the filter coefficient 1.
- **Coefficient 2**: Controls the filter coefficient 2.
- **Coefficient 3**: Controls the filter coefficient 3.
- **Coefficient 4**: Controls the filter coefficient 4.
- **Output Swing:** Resulting peak to peak output swing as percentage of the configured output amplitude.
- **Unit**: You can toggle between dB (decibel) and % (percent).

NOTE

The Deemphasis parameter displays the TxEQ Matrix Editor settings when the PCIe option is selected under the PHY Protocol drop-down list in the Sequence Configuration parameter.

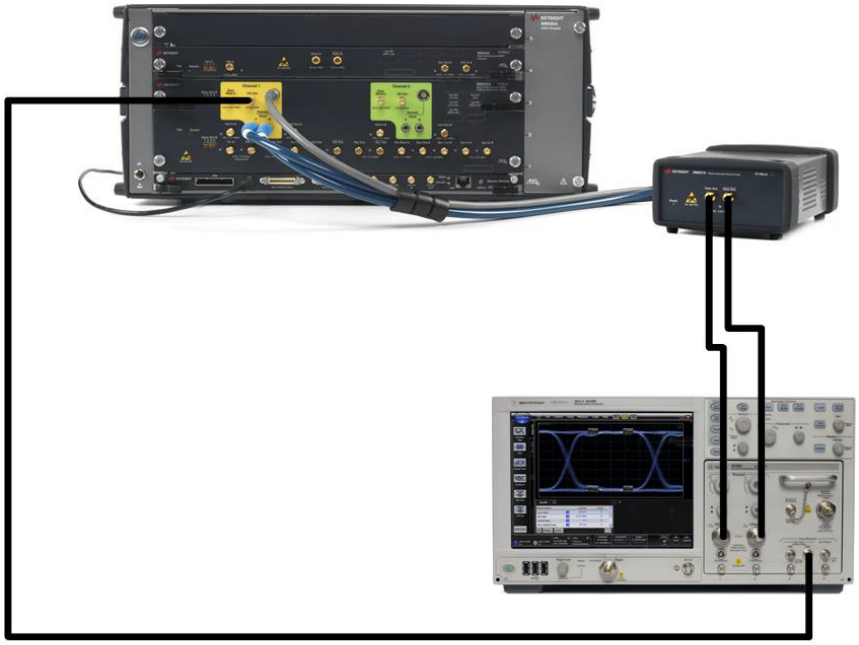
M8040A Automatic Pattern Generator Deemphasis

The Auto Deemphasis feature optimizes the deemphasis settings at the end of the cable to get the best eye performance from the instrument. Additionally, this feature allows you to deembed/embed cable or fixture using an s-parameter file.[

Connection Diagrams

Connection Diagram 1

The following figure shows how to establish a connection among M8045A, M8057A/B and 86100D with 86108B:



Connection among M8045A, M8057A/B and 86100D with 86108B

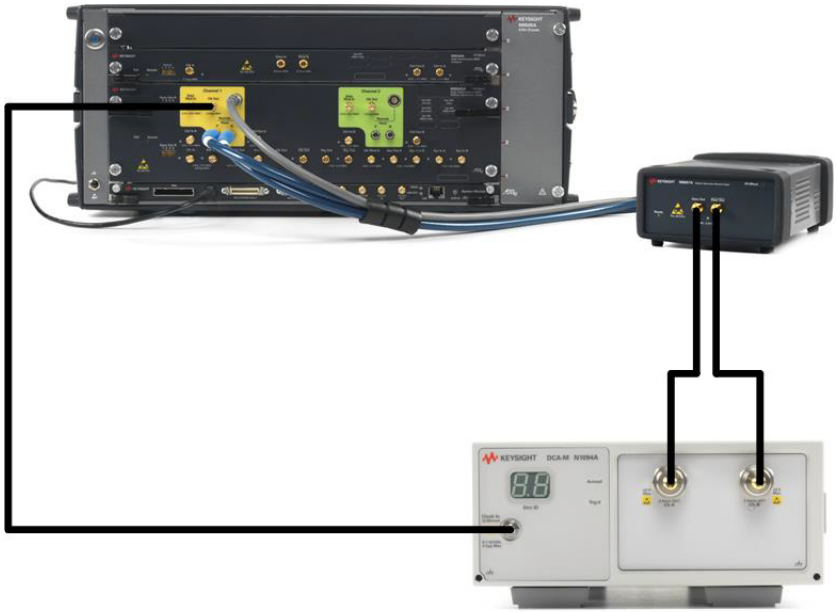
Connection Diagram 2

The following figure shows how to establish a connection among M8045A, M8057A/B and N1000A with N1060A:

Connection among M8045A, M8057A/B and N1000A with N1060A

Connection Diagram 3

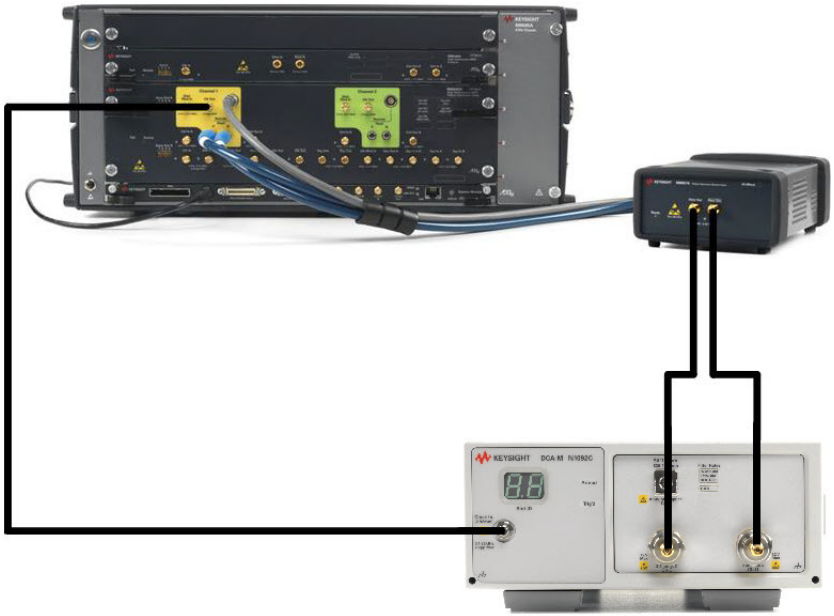
The following figure shows how to establish a connection among M8045A, M8057A/B and N1094A:



Connection among M8045A, M8057A/B and N1094A

Connection Diagram 4

The following figure shows how to establish a connection among M8045A, M8057A/B and N1092C:



Connection among M8045A, M8057A/B and N1092C

Connection Diagram 5

The following figure shows how to establish a connection among M8045A, M8057A/B, and Infiniium UXR-series oscilloscope:

Connection among M8045A, M8057A/B and UXR-series oscilloscope

Using FlexDCA/UXR series oscilloscope from within M8070B

For details on controlling FlexDCA (86108B/N1060A/N1094A/N1094B) and UXR series oscilloscope from M8070B, refer to *M8070ADVB Advanced Measurement Package User Guide* or *Online Help*.

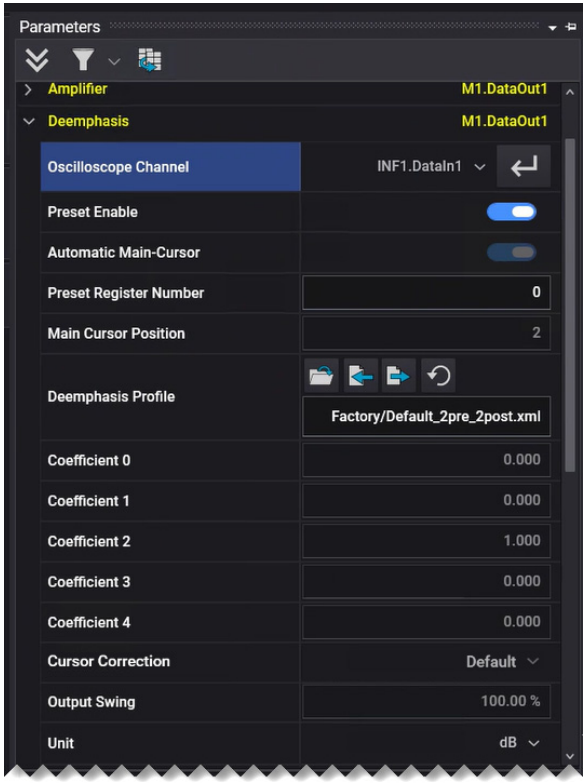
Controlling M8040A Automatic Pattern Generator Deemphasis

1 To control the M8045A auto-deemphasis function, do the following:

a Go to the **Menu Bar** > **Generator** and then select **Data Out**.

b Select **Deemphasis** function block from the **Parameters** window.

The following **Deemphasis** parameters will be shown:



You can enter the deemphasis values in terms of coefficient values. Once you enter the coefficient values, the pre-cursor and post-cursor values are automatically reflected in the corresponding fields. Once the Automatic Main-Cursor button is enabled, you are not allowed to adjust the main cursor as it is automatically calculated. However, to change the values for main cursor, you need to disable the Automatic Main-Cursor button. You are allowed to toggle between dB (decibel) and % (percent). Toggling does not change the value.

c Set the **Deemphasis** values as following:

- **Oscilloscope Channel**: Select an instrument to perform the auto deemphasis. If both DCA & UXR are available as modules, then we can select any of the modules from the drop-down list of available channels. By default, the DCA module will be selected.
- **Preset Enable**: Enables or disables changing the deemphasis preset register number. Once the **Preset Enable** option is enabled, you can set the preset register number.
- **Automatic Main-Cursor** toggle button: Enables automatic calculation of the main cursor.
- **Preset Register Number** - Selects a deemphasis preset register. The supported preset value for M8045A is 0 - 49.
- **Main Cursor Position**: Sets the main cursor position. This can be changed from 1 to 3. The default value is 2.
- **Deemphasis Profile** - Selects the deemphasis preset file from the M8070B workspace (Factory, Current or Shared folder). You are allowed to modify the deemphasis preset values when the deemphasis preset file when loaded from the “Current” or “Shared” folder. All modifications made are directly saved to the file. However, when the deemphasis preset file when loaded from the “Factory” folder, you are not allowed to modify the deemphasis preset values (read-only state).
- **Coefficient 0**: Controls the filter coefficient 0.
- **Coefficient 1**: Controls the filter coefficient 1.
- **Coefficient 2 (Main)**: Controls the filter coefficient 2 (main cursor).
- **Coefficient 3**: Controls the filter coefficient 3.
- **Coefficient 4**: Controls the filter coefficient 4.
- **Cursor Correction**: Selects the cursor correction mode. The available cursor correction modes are “Default” and “None”. If the cursor correction mode is selected as “Default” then it uses the factory calibration table, however, if “None” is selected, it will turn off the calibration table.This parameter is only available for PAM3 line coding and when the deemphasis profile is selected as “Factory/USB4_80G.xml”.
- **Output Swing**: Resulting peak to peak output swing as percentage of the configured output amplitude.

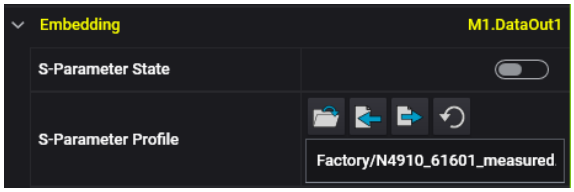
- **Unit**: You can toggle between dB (decibel) and % (percent).

NOTE The auto deemphasis adjustment is supported only for NRZ and PAM4 line coding.

2 The embedding process enables to add the S21 loss to the deemphasis tap settings within the given deemphasis tap resolution/range. To control the **Embedding** function, do the following:

a Select **Embedding** function block from the **Parameters** window.

The following **Embedding** parameters will be shown:



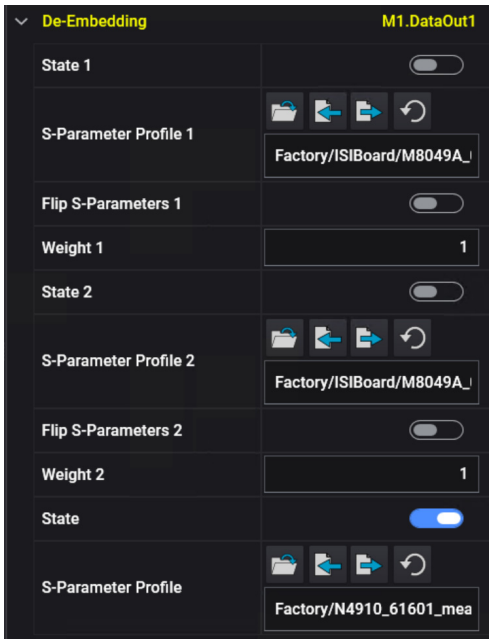
b Set the **Embedding** values as following:

- **State**: Enables/Disables S-Parameter compensation.
- **S-Parameter Profile**: Selects the S-Parameter profile. It also allows you to import and export a S-Parameter profile. It supports S2P file format for embedding.

3 The de-embedding process enables to compensate the loss of cable or channel using the generators deemphasis capability with the given resolution/range. To control the **De-Embedding** function, do the following:

a Select **De-Embedding** function block from the **Parameters** window.

The following **De-Embedding** parameters will be shown:



b Set the **De-Embedding** values as following:

- **State**: Enables/Disables S-Parameter compensation.
- **S-Parameter Profile**: Selects the S-Parameter profile. It also allows you to import and export a S-Parameter profile.

4 Once the above settings are done, click the ↵ **Execute** button. In the case of the UXR series oscilloscope, the **Data In** and **Common** parameters in the **Properties** window will be not be available until the deemphasis coefficients are calculated automatically.

M8050A Automatic Pattern Generator Deemphasis

The Auto Deemphasis feature optimizes the deemphasis settings at the end of the cable to get the best eye performance from the instrument. Currently, this feature supports N1060A and N1046A DCAs.

Connection Diagrams

Diagram 1

The following figure shows how to establish a connection among M8009A, M8042A, M8058A and N1060A DCA.

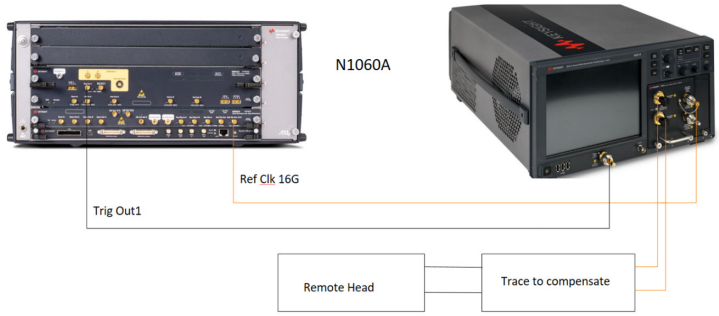


Diagram 2

The following figure shows how to establish a connection among M8009A, M8042A and N1046A DCA.

NOTE Ensure that you have turn on Ref Clk 16G, Trig Out, Data Out Amplifier and the global Output before applying auto-deemphasis.

NOTE Setting a high voltage value on the DataOut amplitude will result in an error and stop auto deemphasis. In this case, try again with a smaller amplitude value.

NOTE Remember not to use N1046A DCA together with N1060A in one chassis. In this case, there is no PTB (precision timebase) support for N1046A.

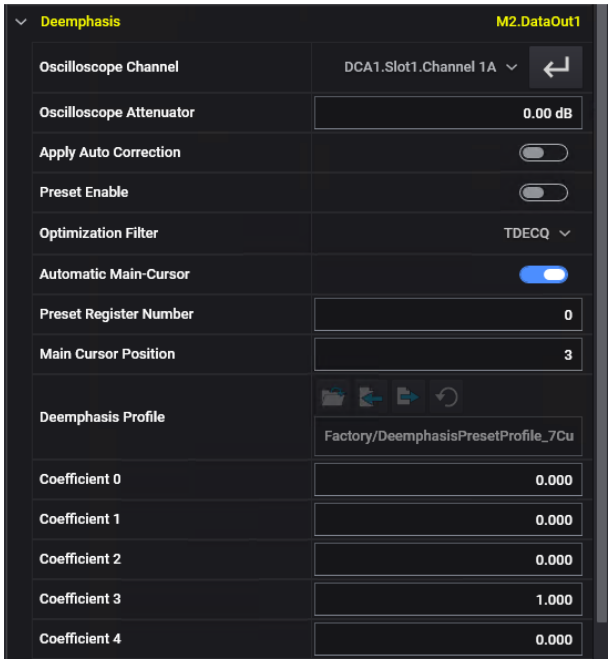
Controlling M8050A Automatic Pattern Generator Deemphasis

To control the M8042A auto-deemphasis function, do the following:

1 Go to the **Menu Bar** > **Generator** and then select **Data Out**.

2 Select **Deemphasis** function block from the **Data Out** > **Parameters** window.

The following **Deemphasis** parameters will be shown:



3 Configure the automatic deemphasis function using the following parameters:
   - **Oscilloscope Channel**: Select a channel to perform the auto deemphasis, and then click **Execute** button.
   - **Oscilloscope Attenuator**: Set attenuation if an external attenuator is connected.
4 Once the deemphasis adjustment is done using the above parameters, click **Apply Auto Correction** to enable or disable the correction data.

Controlling M8050A Pattern Generator Deemphasis

You can enter the deemphasis values in terms of coefficient values. Once you enter the coefficient values, the pre-cursor and post-cursor values are automatically reflected in the corresponding fields. Once the **Automatic Main-Cursor** button is enabled, you are not allowed to adjust the main cursor as it is automatically calculated. However, to change the values for main cursor, you need to disable the **Automatic Main-Cursor** button. You are allowed to toggle between dB (decibel) and % (percent). Toggling does not change the value.

1 Set the Deemphasis values using the following parameters:
   - **Oscilloscope Channel**: Select a channel to perform the auto deemphasis, and then click Execute button.
   - **Automatic Main-Cursor**: Enables automatic calculation of the main cursor.
   - **Preset Enable**: Enables or disables changing the deemphasis preset register number. Once the Preset Enable option is enabled, you can set the preset register number.
   - **Optimization Filter**: Selects the optimization filter, either through a linear equalizer or TDECQ equalizer.

NOTE The M8042A auto-deemphasis function with TDECQ equalizer is only supported by FlexDCA version A.07.81.6 and higher.

   - **Automatic Main-Cursor**: Enables automatic calculation of the main cursor.
   - **Preset Register Number**: Selects a deemphasis preset register.
   - **Main Cursor Position**: Sets the main cursor position. This can be changed from 2 to 4. The default value is 2.
   - **Deemphasis Profile** - Selects the deemphasis preset file from the M8070B workspace (Factory, Current or Shared folder).

- **Coefficient 0**: Controls the filter coefficient 0.
- **Coefficient 1**: Controls the filter coefficient 1.
- **Coefficient 2 (Main)**: Controls the filter coefficient 2 (main cursor).
- **Coefficient 3**: Controls the filter coefficient 3.
- **Coefficient 4**: Controls the filter coefficient 4.
- **Coefficient 5**: Controls the filter coefficient 5.
- **Coefficient 6**: Controls the filter coefficient 6.
- **Output Swing**: Resulting peak to peak output swing as percentage of the configured output amplitude.
- **Unit**: You can toggle between dB (decibel) and % (percent).

2 Once the deemphasis adjustment is done using the above parameters, click **Apply Auto Correction** to enable the correction data.

Setting Up Data Out Port Parameters

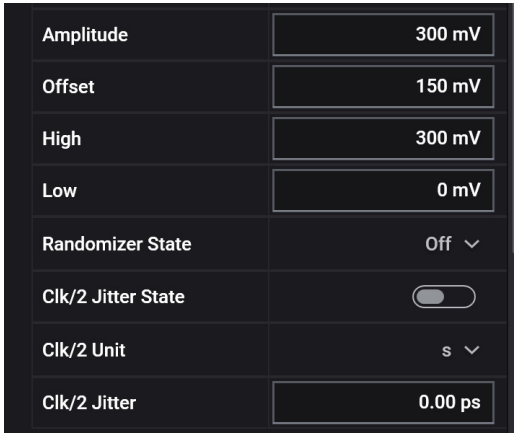
The generator produces clock and data outputs that serve as frequency reference and device stimulus for the device under test.

To set the **Data Out** parameters:

1 Go to the **Menu Bar** > **Generator** and then select **Data Out** port.

2 Select **Amplifier** functional block from the **Parameters** window.

3 Set the parameters as described in this section. Depending on whether you are using the M8020A, M8040A, or M8050A, the “Data Out” parameters under the “Amplifier” functional block may vary. The following screenshot is from the M8050A:



Amplitude

This text field allows manual entry of the voltage amplitude and displays the current value.

To modify the value, click inside the text field and enter the desired value.

NOTE

The M8020A/M8040A/M8050A will not allow you to adjust a voltage beyond its limits. The limit is determined by the M8020A/M8040A/M8050A's internal hardware. If a limit is encountered, the M8020A/M8040A/M8050A sends a message to the System Error. For more information about voltage limits, see the M8020A, M8040A & M8050A Data Sheets.

NOTE

If you may want to adjust the output voltage level without changing the Amplitude, the M8020A/M8040A/M8050A handles this by keeping Amplitude constant when Offset voltage is changed and High and Low voltages are accordingly adjusted.

Similarly, if you want to adjust the output voltage level without changing the Offset, the M8020A/M8040A/M8050A handles this by keeping Offset constant when Amplitude is changed and High and Low voltages are accordingly adjusted.

You can even click **Auto Range** option which will automatically select the amplitude range according to amplitude. This option is only available with M8020A.

High Voltage

This text field allows manual entry of the logic high voltage level and displays the current value.

To modify the value, click inside the text field and enter the desired value.

Offset Voltage

This text field allows manual entry of the voltage level halfway between logic high and logic low (the offset) and displays the current value.

To modify the value, click inside the text field and enter the desired value.

Low Voltage

This text field allows manual entry of the logic low voltage level and displays the current value.

To modify the value, click inside the text field and enter the desired value.

Crossover

This text field allows manual entry of the data's crossover percentage, and displays the current value.

Note that the crossover feature is not supported by M8040A and M8050A.

Clk/2 State

This option allows to enable the Clk/2 Jitter on the output signal.

Clk/2 Jitter

This text field allows manual entry of the Clk/2 Jitter at the Data Out port in units of seconds. It provides half rate clocking; the clock at the clock output runs at half the bit rate.

The Clk/2 Jitter is defined as the absolute delay between odd and even symbols, representing the full timing difference between consecutive edges. It is not measured relative to the ideal transition time and therefore corresponds to a peak-to-peak (not half-amplitude) value.

Data Polarity Inverted

Use this option to invert the logic of the data outputs (Data Out, Trigger Out and Clock Out).

Transition Time

Use this option to control the transition time of the output signal. The choices are smooth, moderate and steep.

Note that the transition time is only supported by M8020A.

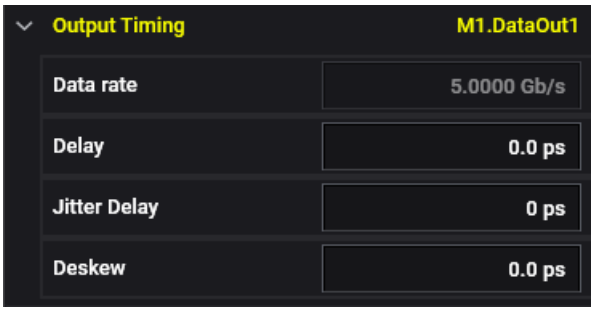
Randomizer State

Use this option to switch the randomizer on or off. If the randomizer is on, non-linear distortions of the signal are minimized, but a higher noise floor is introduced. Switch the randomizer on when the non-linear distortions are dominating SNDR and off when the noise is dominating SNDR. By default, the randomizer is off.

Note that the Randomizer State is only supported by M8050A.

Setting up Output Timing

The **Output Timing** functional block provides following parameters:



- **Data Rate** - Sets the channel data rate in b/s. To set up the data rate, go to Clock Generator and set the Frequency.
- **Delay** - Controls the data delay of the output signal. This also affects the channel's Clock Out signal when the clock source is configured as Data Clock.
- **Jitter Delay** - Controls the delay of jitter profile. Use this option to adjust the jitter phase between multiple outputs (e.g. clock and data) on the receiving side to ensure error free sampling for the jitter frequencies and amplitudes used in the setup.
- **Deskew** - This feature is used to match or adjust the timing delay between the Data Out channels. It is a delay offset that is intended to deskew the output in respect to other outputs. This value is an offset to the data delay as well as jitter delay.

Bit Rate

Bit rate is defined as bits per second. The Generator's clock rate sets the bit rate and serves as the frequency reference for the Data, Clock and Trigger outputs, your device, and the Analyzer (if it receives its clock from the Generator). It can be generated internally or supplied from an external source.

When to Use an External Clock Source?

The M8020A/M8040A/M8050A's internal clock can be used for most testing purposes.

There are some circumstances, however, when an external clock source is required:

- Synchronization with an external clock

  The M8020A/M8040A/M8050A can be connected to an external clock to allow it to run as part of a larger external system.
- Use of a modulated clock

  A frequency- or delay-modulated clock can be used to provide a small amount of jitter to the clock signal.
- Use of a precision clock

  A precision clock with very low phase noise can be used to enhance the instrument's performance. This is especially interesting for longterm measurements.

Bit Rate Range

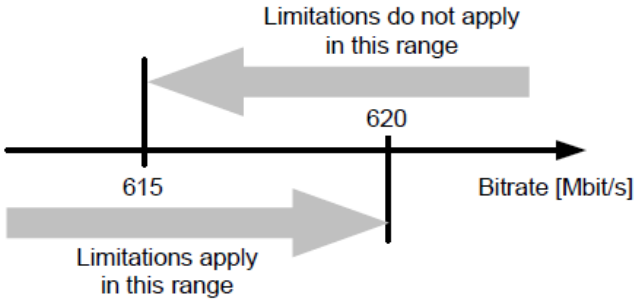
The M8040A provides symbol rate from 2.0 to 32.4 GBd for M8045A Option -G32 and 2.0 to 58.0 GBd (all specifications are valid up to 58 GBd with over-programming up to 64.8 GBd) for M8045A
Option -G64.

The M8020A provides bit rates from 256 Mbit/s up to 16.2 Gbit/s, depending on the instrument's options.

However, several specific properties and limitations need to be taken into account when working at low bit rates. The limitations apply to the instrument according to the following hysteresis curve:

- If the bit rate falls below 615 Mbit/s, the limitations apply.
- If the bit rate exceeds 620 Mbit/s, the limitations no longer apply.

The following figure clarifies the behavior in the range between 615 Mbit/s and 620 Mbit/s:



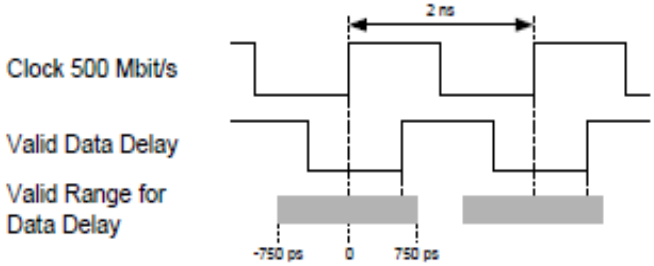
For the generator the following rules apply:

- Below 620 Mbit/s, the Generator can only be operated with an external clock source, because the internal clock source can only produce signals higher than 620 Mbit/s.
- The trigger output cannot be set up to trigger on certain pattern positions or pattern sequences. If this option is enabled (for example in the user interface), the trigger is sent once for each pattern, but the bit position cannot be specified.

  The option to trigger on the divided clock signal is supported as usual.
- There are restrictions to the available clock to data delay values.

  The Generator can vary the clock to data delay only within a range of 10 ns (relative to the clock signal). For frequencies above 666 Mbit/s, this range is sufficient to cover the complete clock cycle (= 1 unit interval).

  For lower frequencies, the valid data delay range is smaller than the clock cycle. The Generator cannot generate signals with a delay outside this range. Therefore, the data delay cannot be set to all values within the clock cycle.

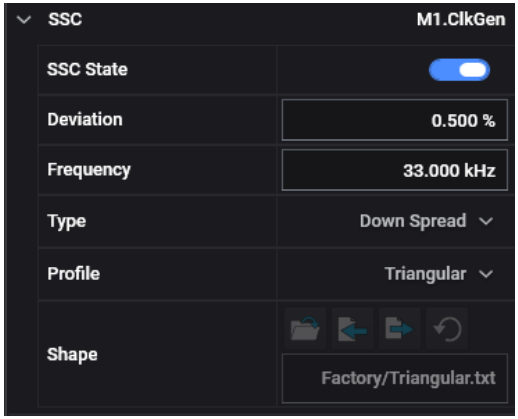


Spread Spectrum Clocking

A **Spread Spectrum Clock** (SSC) is widely used for reducing the peak electromagnetic radiation at the nominal clock frequency. With SSC, the clock pulse is modulated with a relatively low-frequency triangle waveform. This broadens the clock signal spectrum and reduces the peak energy. The M8020A/M8040A/M8050A allows to emulate such SSC on the data, trigger and clock output signals.

The M8020A/M8040A/M8050A has a built-in SSC generator.

For the **SSC** settings, go to **Menu Bar** > **Clock** > **Clock Generator** and then select **SSC** function block from the **Parameter** window.



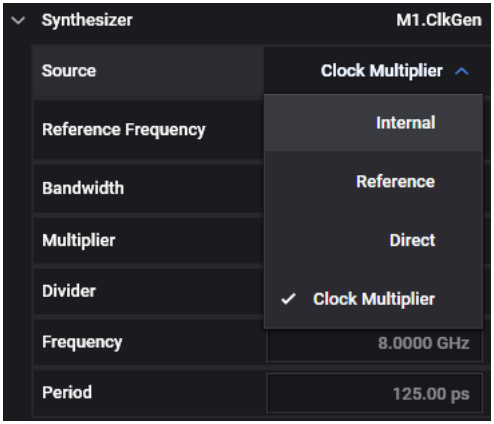
Setting the Bit Rate

You can use an external clock source or the M8020A/M8040A/M8050A's internal clock to control the bit rate.

To set the bit rate:

1 Go to **Menu Bar** > **Clock** and then **Clock Generator**.

2 Select **Synthesizer** function block from the **Parameter** window.



3 Select the appropriate clock source from the following options:

- **Internal** - When clock source is selected as Internal, an internal clock oscillator is used. For the internal clock source, different reference clock sources are available for the internal oscillator. When the Reference frequency is selected as Internal 100 MHz, then 100 MHz Reference clock of M8041A/ M8045A module is used and when Reference frequency is selected as AXIe 100 MHz, then 100 MHz reference clock of M950XA AXIe chassis is used.
- **Reference** - To use clock source as Reference, we need to connect external reference clock source to Ref Clk In port of M8041A/ M8045A module. Depending upon the connected clock source, you have to choose between either 100 MHz reference frequency or 10 MHz reference frequency.
- **Direct** - To use Clock source as Direct, you need to connect external clock source to Ref Clk In port of M8041A/ M8045A port. Enter the frequency of the clock source as the Reference frequency. Also, you can use the **Execute** button to measure the frequency of the connected clock source. This connects the external clock directly to the clock generator at 8.1 GHz to 16.20 GHz.

- **Clock Multiplier** - To use the clock source as Clock Multiplier, you need to connect external clock source to the Ref Clk In port of the M8041A/ M8045A module and then specify the reference frequency. You can generate the specific frequency by choosing multiplier and divider value. Also, you can use the **Execute** button to measure the frequency of the connected clock source.

  The Clock Multiplier option is also supported by M8045A. This option can be enabled by using the M8045A-0G6 license. For more details on licensing, refer to M8040A Licenses on page 833. This option is applicable for PCIe 2.5G, 5G, 8G, and 16G. To use the clock multiplier feature in M8040A, the serial number of M8045A module must be greater than or equivalent to 1000. The range of the multiplier is 21 - 648.

4 For Direct clock source, click **Execute** button to measure the incoming clock's clock rate.

5 Select a clock rate:

- For Internal Clock Source, you can enter a clock rate in the Value and Units field.
- For 10/100 MHz Ref Clock Source, the clock connected to the 10/100 MHz Ref In port must be 10/100 MHz.

The selected clock rate applies to the generator. This is also the clock rate generated at the generator's Clock Out port. The analyzer internally receives its clock from the generator, it runs at the same clock rate.

External Clock Divider

The internal clock (i.e. the bitrate) is the external clock divided by the value specified in the clock divider field. The external clock divider field is available if you have close an external clock source.

External PLL Clock Divider and Multiplier

The internal clock (i.e. the bitrate) is the external PLL divided by the value specified in the divider field and multiplied with the value specified in the multiplier field. The external PLL clock divider and multiplier field are available if you have chosen a clock source.

Clock Rate Indicators

The Bit Rate indicators are shown in the **Status Indicators** display their current bit rate.

The analyzer bit rate is measured from the incoming clock signal or derived from the data signal.

Trigger Output

The generator's **Trigger Out** port can be used to send a trigger to external devices like an oscilloscope or digital communication analyzer.

In pattern mode, the generator sends a trigger signal that is at least 32 bits long.

In sequence mode, the generator can send a trigger signal whenever a block of the sequence starts or restarts.

Several options are available for the trigger signal. As an example, you can send the trigger as a divided clock signal or as an indicator when the data pattern starts.

Setting Up Trigger Output

To set up the generator's **Trigger Output** port:

1 Connect the external instrument to the **Trigger Out** port.

2 Go to **Menu Bar** > **Generator** > and then select **Trigger Out**.

3 Provide the necessary configuration.

The delay option in the **Trigger Out** functional block sets the delay of the trigger output. When it is set to 0 ps, this means there is no delay or the trigger output and data output are in sync. When it is set as 10 ps, this means the signal which will be received at trigger output port will have a delay of 10 ps.

You can always generate a divided clock signal at the **Trigger Out** port.

The alternate trigger signals refer to patterns and are not generated in sequence mode.

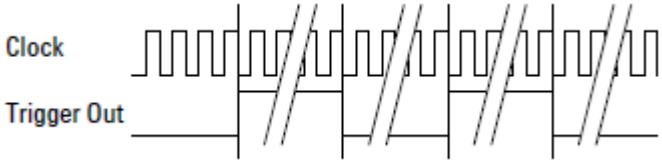
If SSC is enabled, then it also have impact on trigger output signal.

To support the generation of a trigger spike at the beginning of a sequence block, the **Trigger Output** can be put into **Sequence** mode.

NOTE The jitter at **Trigger Out** is always the same as jitter at **Clock Out**. Since, there are no parameters available in the M8070B GUI to set jitter at **Trigger Out**, it can be set using **Clock Out** parameters.

Clock Divided by n

Select this option to send a trigger signal from the **Trigger/Ref Clock Out** port at every nth clock pulse. Note that the trigger signal itself consists of n/2 bits high followed by n/2 bits low. For example, Clock divided by 8 works as shown below.



NOTE If the Divider Factor n is uneven (For example 3), the clock's duty cycle will not be 50%, but the signal will stay high for (n+1)/2 and low for (n-1)/2. This results in a Duty Cycle Distortion (DCD) of 0.5 UI.

Sequence Trigger

This function becomes available after a user-defined sequence has been downloaded to the generator.

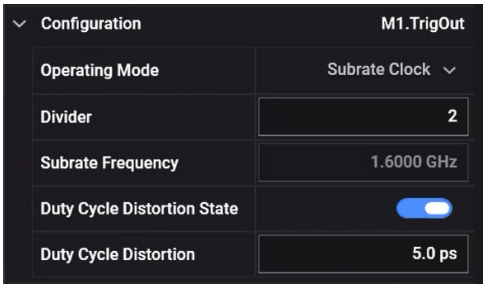
Click this function to switch the **Trigger Out** port to **Sequence** mode.

In Sequence mode, the **Trigger Out** can generate a spike whenever the execution of a block starts or restarts. Whether that happens for a particular block or not is defined for each block individually in the sequence expression.

Duty Cycle Distortion

Duty cycle distortion is a type of deterministic jitter in which the signal has the width of the positive pulses that are not equal to that of negative pulses. The Duty Cycle Distortion parameter can be used for adjusting the Duty Cycle Distortion of the subrate clock that is generated at Trigger Out. The signal's duty cycle is shifted towards right or left edge of the signal depending on the adjustment made in the delay parameter.

This function becomes available when the operating mode is selected as Subrate Clock.



The following two parameters are available to set the Duty Cycle Distortion:

- **Duty Cycle Distortion State** - Enables or disables the effect of Duty Cycle Distortion on the Trigger Out.
- **Duty Cycle Distortion** - Adjust the duty cycle distortion in seconds. Any adjustment done with this parameter is in addition to the anyways existent duty cycle error caused by an odd subrate divider value. This parameter is not available, and the effect on the hardware is disabled when the operating mode is set to Sequencer Control.

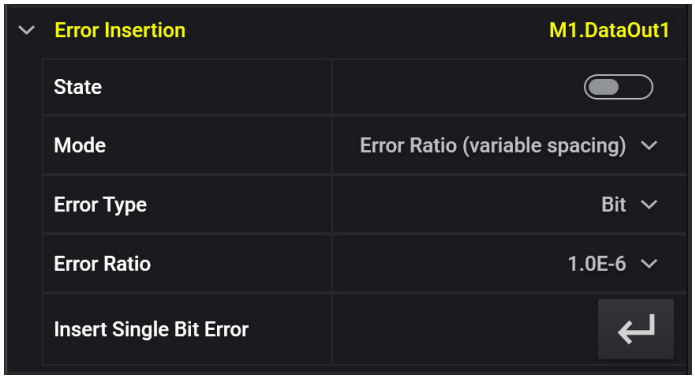
Below is the recommended settings which you must use on the scope in order to get accurate measurements for the DCD values.

Recommended Settings: Perform Auto Scale to adjust the amplitude scale and offset value as per the input signal. Ensure that Trigger settings are set as Trigger Mode set to Edge, Trigger source to Channel1 or channel at which input signal is connected, Trigger Level to 0.0V and Trigger Sweep must be set to Triggered.

Error Insertion

To test error correction algorithms, alarms and other functions that are embedded in the data pattern, you can insert logic errors (flipped bits) into the pattern.

For the error insertion, go to **Menu Bar** > **Data Out** and select **Error Insertion** function block from the **Parameters** window.



Mode

An error can be inserted through different operating modes which can be selected through this drop-down option. The following options are available; Error Ratio (Fixed Spacing), Error Ratio (Variable Spacing), Ctrl In A, Ctrl In B, Break, etc. You are only allowed to set the values for Error Ratio (Fixed Spacing), Error Ratio (Variable Spacing). For Ctrl In A/B, Sys In A/B modes, the errors are then inserted instead driven by the signal applied to the respective port or by the Break button available in the Sequence Editor.

Error Type

The error type can be selected using the drop-down menu. The default error insertion type is 'Bit.' To inject symbol errors based on the specified 'Error Ratio,' the error insertion type 'Symbol' must be selected. Currently, the 'Symbol' error type is available only for PAM3 and PAM4 line coding.

Inserting Error Bits

The instrument provides several options for inserting error bits manually or automatically. You have the following options for inserting errors into the output data stream:

Insert Single Bit Stream

To insert single bit stream:

- Click the slide switch to turn on the **Error Insertion** state.
- Select the supported mode from the drop-down list.
- Select the error ratio from the drop-down list.

Insert Single Bit Error

To manually insert a single bit error into the output stream:

- Click the **Data Out** port.
- Select **Error Insertion** functional block and select **Error Type** as **Bit** to enable the **Insert Single Bit Error** state.
- Click the 'Insert Single Bit' **Execute** button.

Insert Single Symbol Error

To manually insert a single symbol error into the output stream:

- Click the **Data Out** port.
- Select **Error Insertion** functional block and select **Error Type** as **Symbol** to enable the **Insert Single Symbol Error** state. Note that this option is only applicable when the M8042A pattern generator module operates in the PAM3, PAM4, PAM6, or PAM8 line coding and the M8045A pattern generator module operates in the PAM3 or PAM4 line coding.
- Click the 'Insert Single Symbol Error' **Execute** button.

Insert Disparity Error

To manually insert a single disparity error into the output steam:

- Click **Data Out** port.
- Select **Error Insertion** functional block and enable the **Insert Disparity Error** state. Please note that this option is only applicable valid for 8b/10b operating mode on the specified output of M8041A generator ports.

NOTE

TIP - To find out how your DUT reacts on very small bit error rates, set up the pattern generator to enter errors once every 10^{-12} bits and run a longer accumulative test.

You can then find the DUT's true error rate by calculating the difference between the bit error rate set up in the Generator and the accumulated bit error rate found by the Analyzer.

NOTE

If you set up too high an error rate, the Analyzer will not be able to synchronize to the incoming pattern. When setting up an error rate, always make sure that the synchronization threshold is higher than the bit error rate.

FEC Error Insertion

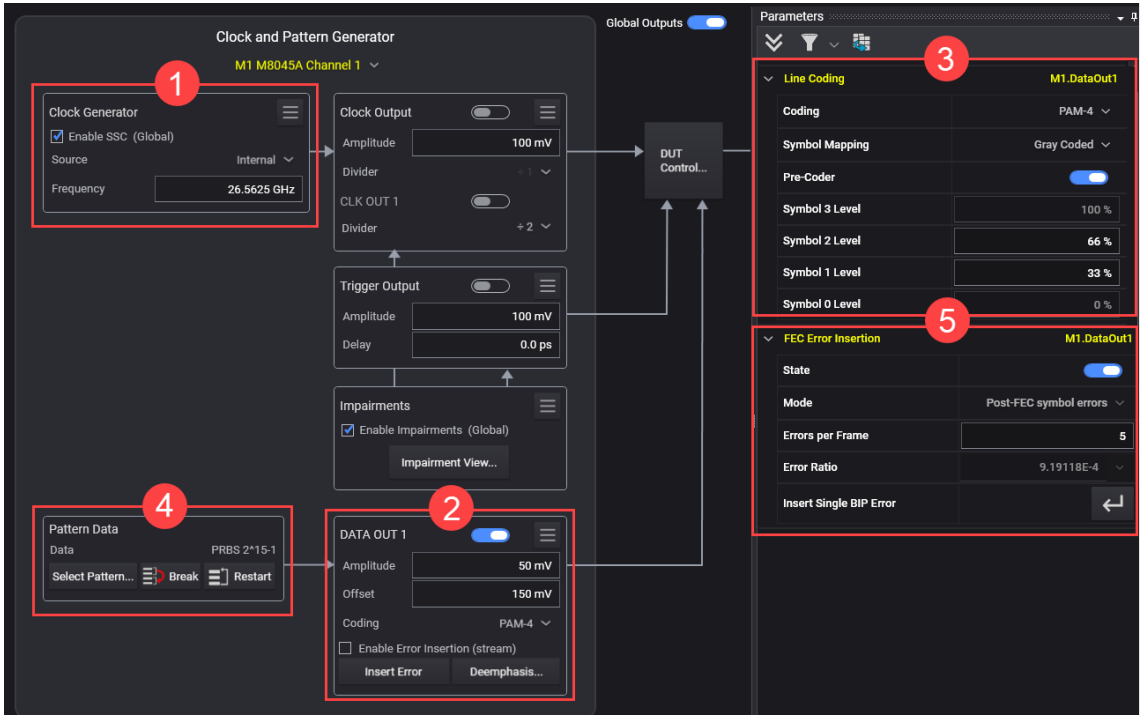
The FEC error insertion is independent from the error insertion controlled with the **FEC Error Insertion** functional block available in the **Parameters** window. Both error insertions can be used at the same time.

The FEC error insertion is a license feature and is support by M8070B software by installing a module specific FEC license. For details on FEC license, please refer to the Licenses on page 823.

FEC is enabled by selecting one of the FEC factory patterns.

- IEEE_802_3cd_RS_544_514_Scrambled_Idle
- IEEE_802_3cd_RS_544_514_Remote_Fault

To generate FEC for PAM4 on M8042A/M8045A, follow the given steps using M8070B **Setup View** as illustrated in the following figure:

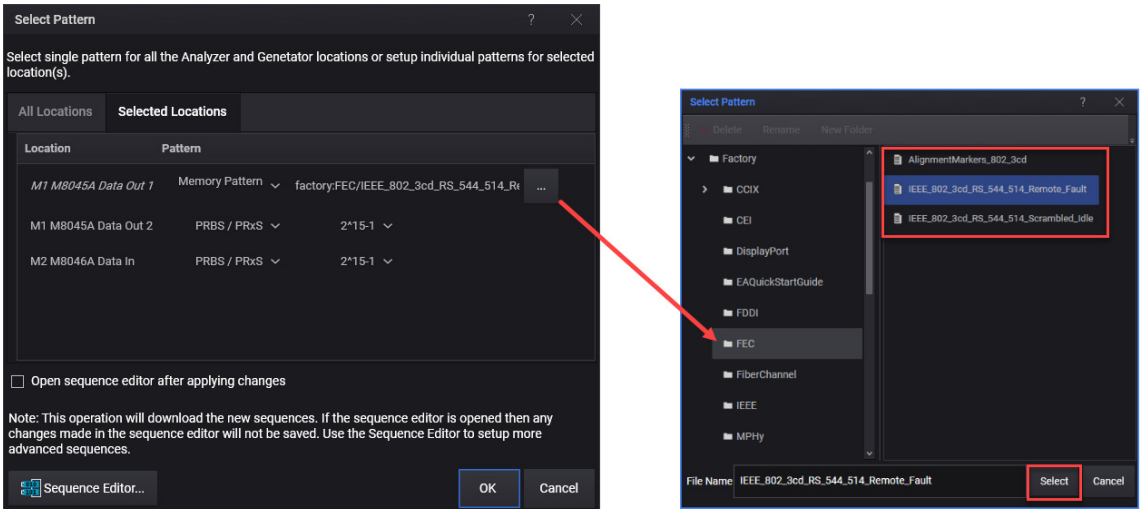


1 On the **Clock Generator** functional block, set the symbol rate between 16.208 GBd to 26.563 GBd. Please note that the FEC engine only supports 26.5625 GBd PAM4 signals.

2 On the **Data Out** functional block, set output levels. Make sure to turn **ON** the output levels.

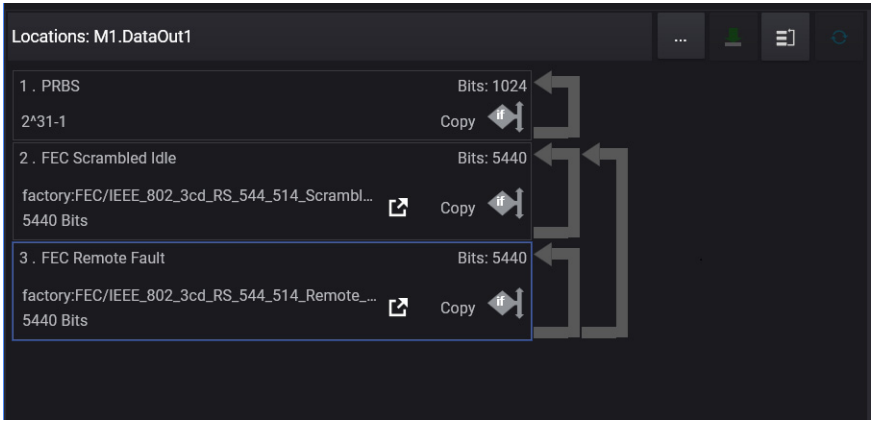
3 On the **Line Coding** functional block select **PAM4**. Enable the PAM4 **Pre-Coder**. Enabling the pre-coder is optional and is only required if the DUT also have the pre-coder enabled.

4 Next step involves selecting the FEC pattern. To do this, click **Select Pattern** dialog. For more information on this dialog, refer to Select Pattern Dialog on page 649. Use this dialog to download FEC pattern on the **Data Out** locations as shown in the following figure:



Both channels of the M8045A generate the FEC encoded signal independently. When setting up the same sequence for both channels, both channels will generate the exactly same bit sequence.

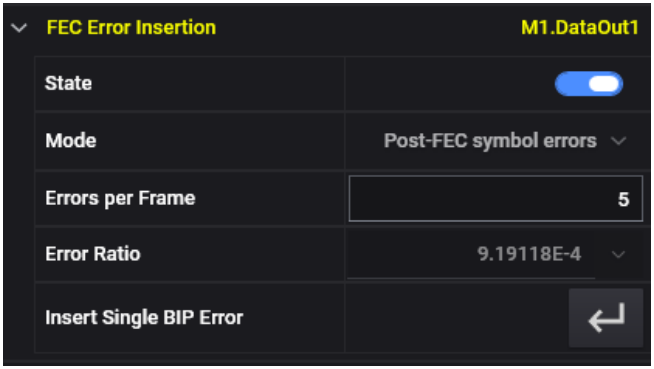
5 The FEC pattern will be now available in the **Sequence Editor**. Infinitely loop the PRBS, FEC encoded scrambled idle and FEC remote fault patterns. Press the Break button to move the sequence to the next block. Refer to Sequence Editor on page 613 for details on how to create, loop and break sequences.



FEC patterns require a block length of 5440 and use either an infinite loop or counted loop. The loop count must be a multiple of 8.

Due to the differences between FEC frame length and sequencer word width, there will be phases of invalid FEC data when transitioning from a FEC encoded sequence lock into a non-FEC sequence block and vice versa.

6 You can now insert the FEC error into the output data. It can be either pre-FEC error or post FEC error. Select **FEC Error Insertion** function block from the **Parameters** window.



You have the following options for inserting FEC errors into the output data stream:

- **State** - Enables/disables the continuous FEC error insertion. The inserted errors are after the FEC encoding.
- **Errors per Frame** - Specifies the number of symbols to be corrupted within a single FEC frame. The inserted errors are at random symbol positions. Each corrupted symbol will contain exactly one bit error at a random bit position.
- **Insert Single BIP Error** - Insert a single Bit Interleaved Parirty (BIP) error. This is a pre-FEC error and can be inserted at any time, even if the FEF error insertion is disabled.

FEC Remote Programming

The following SCPI commands can be used for FEC error insertion remote programming:

1 Commands for selecting FEC patterns:

:DATA:SEQuence:SET 'M1.DataOut1',Memory,'factory:FEC/IEEE_802_3cd_RS_544_514_Scrambled_Idle‘

:DATA:SEQuence:SET 'M1.DataOut1',Memory,'factory:FEC/IEEE_802_3cd_RS_544_514_Remote_Fault'

2 Commands for FEC error insertion:

a Enable/disable symbol error insertion

```
:DATA:FEC:EINSertion:STATe 'M1.DataOut1',<0|1|OFF|ON>
```

b Set the number of symbol errors per FEC frame

```
:DATA:FEC:EINSertion:ERRors 'M1.DataOut1',<NR1>
```

c Insert a single BIP error

```
:DATA:FEC:EINSertion:BIP:ONCE 'M1.DataOut1';*OPC?
```

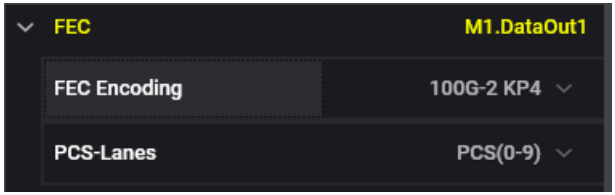
For further details on these SCPI commands, please refer to the *M8000 Series Programming Guide*.

FEC Encoding

FEC Encoding for M8045A

The M8045A module works in 50G, 100G KP4, 200G KP4, 400G KP4 and 2x400G KP4 modes. The FEC Encoding and PCS-Lanes are two additional parameters under FEC functional block when one of the following startup options is selected while launching the M8070B application:

- BERT with FEC (50G)
- BERT with FEC (100G KP4)
- BERT with FEC (200G KP4)
- BERT with FEC (400G KP4)
- BERT with FEC (2x400G KP4)



- **FEC Encoding** - This is a non-editable field. The generated FEC is according to the given standard. It depends on the startup option selected (50G, 100G KP4, 200G KP4, 400G KP4, 2x400G KP4).
- **PCS-Lanes** - This is a non-editable field. It selects the PCS-Lanes generated on the channel. This does not affect the patterns that are not FEC encoded.

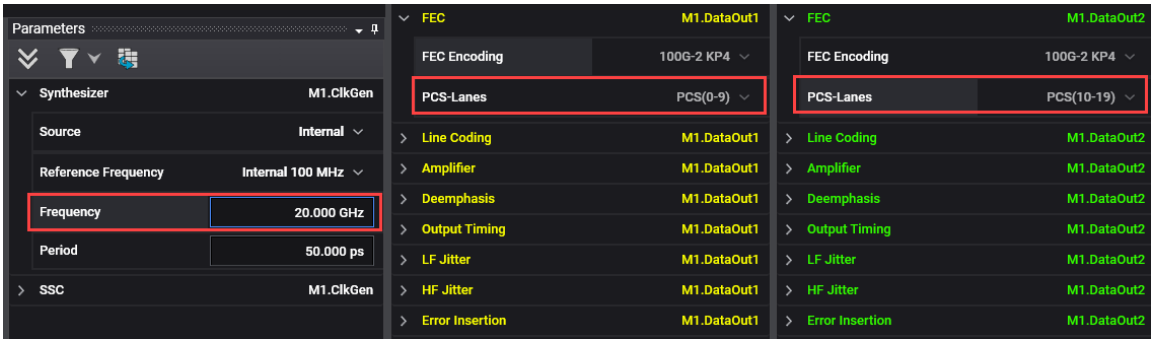
The M8045A module is restricted to the symbol rates which ranges from 16.208 GBd to 26.6 GBd and 32.416 GBd to 53.2 GBd. The following table summarizes the supported symbol-rate ranges for different KP4 modes of the M8045A module:

	16.208 GBd - 26.6 GBd	32.416 GBd - 53.2 GBd
50G KP4	Yes	No
100G KP4	Yes	Yes

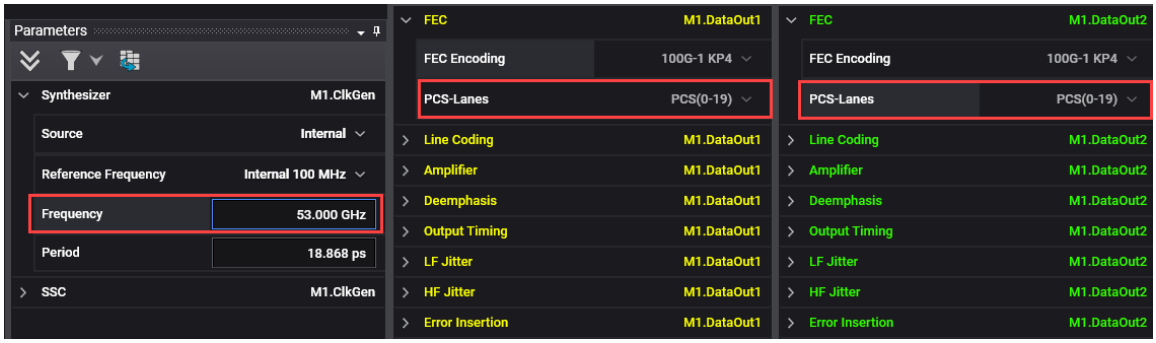
	16.208 GBd - 26.6 GBd	32.416 GBd - 53.2 GBd
200G KP4	Yes	No
400G KP4	Yes	No
2x400G KP4	No	Yes

Examples showing the symbol rate range option for FEC (100G KP4) and FEC (2x400G KP4) are shown later in this section.

In case of BERT with FEC (100G KP4), the PCS-Lanes value depends on the symbol rate range. For 16.208 GBd to 26.6 GBd, the PCS lanes are split between both the channels. For example, channel one uses (0-9) and channel two uses (10-19).



For 32.416 GBd to 53.2 GBd, both the channels use the same number of lanes (0-19).



In case of BERT with FEC (2x400G KP4), the PCS-Lanes value depends on the symbol rate range. For 32.416 GBd to 53.2 GBd, the PCS lanes are split between both the channels. For example, channel one uses (0-3) and channel two uses (4-7).

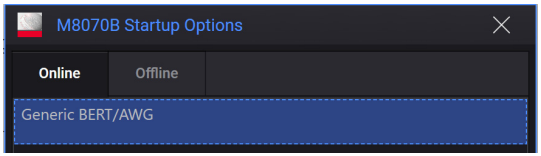
FEC Encoding for M8042A

The M8042A pattern generator module supports forward error correction (FEC) and precoding encoding according to IEEE802.3cd. The M8042A module operates in 100G-1 KP4, 200G-2 KP4 and 2x400G-4 KP4 modes for PAM4 line coding. All other modules operate exactly as in the Generic BERT mode. The factory patterns IEEE_802_3cd_RS_544_514_Remote_Fault and IEEE_802_3cd_RS_544_514_Scrambled_Idle use FEC as specified for 100G KP4, 200G KP4 and 2x400G KP4 applications. Computer standard-specific functionalities, such as dedicated PHY-Protocols or LTSSM support, are not available when the M8042A module operates in 100G KP4, 200G KP4 and 2x400G KP4 modes.

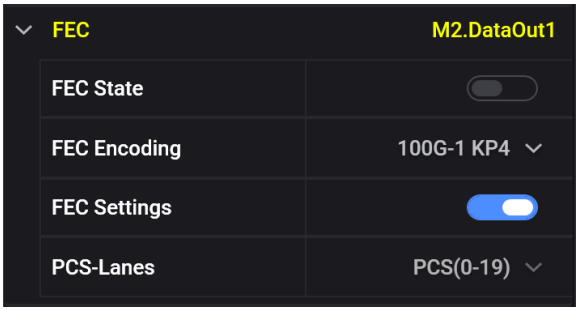
The M8042A module has a symbol rate range from 32.416 GBd to 53.2 GBd.

To enable FEC Encoding in M8042A, follow the given instructions:

1 Start the M8070B with the Generic BERT/AWG option.

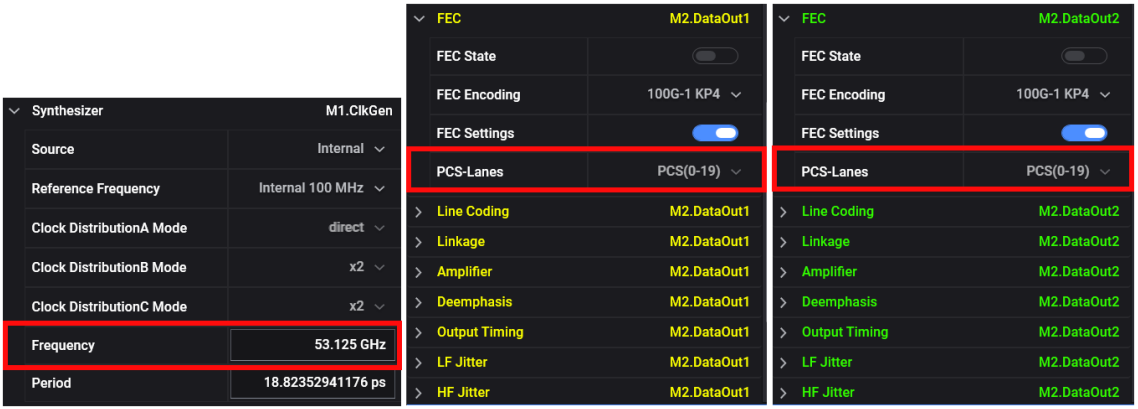


2 In the M8042A Data Out parameter, select FEC functional block. The following FEC parameters will be available:



- **FEC State** - This is a read-only option which indicates whether FEC is enabled or disabled. FEC is enabled when FEC supported patterns with PAM4 line coding and within the supported data rate range are selected.
- **FEC Encoding** - This option allows to select the FEC encoding according to the given standard. The following FEC encodings are supported:
  - 100G-1 KP4
  - 200G-2 KP4
  - 2x400G-4 KP4
  - 200GE 1.6T KP4
- **FEC Settings** – This option applies the FEC settings in the M8042A Pattern Generator module, setting the line coding to PAM4 and the data rate to 53.125 Gbd.
- **PCS-Lanes** - This is a non-editable field. It selects the PCS-Lanes generated on the channel. This does not affect the patterns that are not FEC encoded.

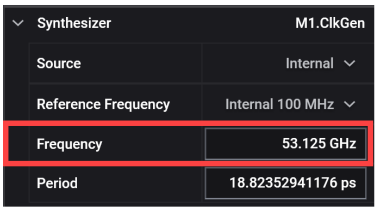
Example showing the symbol rate range option for FEC (100G-1 KP4) is shown in this section.

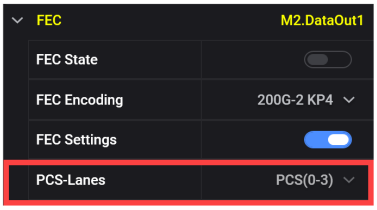


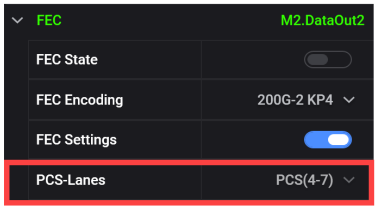
For 32.416 GBd to 53.2 GBd, both the channels use the same number of lanes (0-19).

In case of BERT with FEC (200G-2 KP4) and FEC (2x400G-4 KP4), the PCS-Lanes value depends on the symbol rate range. For 32.416 GBd to 53.125 GBd, the PCS lanes are split between both the channels. For example, channel one uses (0-3) and channel two uses (4-7).

Example showing the symbol rate range option for FEC (200G-2 KP4) is shown in this section.







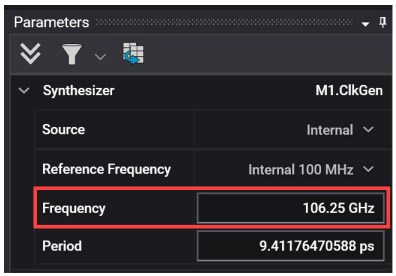
In case of BERT with FEC (200GE 1.6T KP4), the both channel uses the same PCS-Lanes value (0-7) for the symbol rate range between 64.8 GBd to 106.4 GBd. Any value beyond this symbol rate range is not supported.

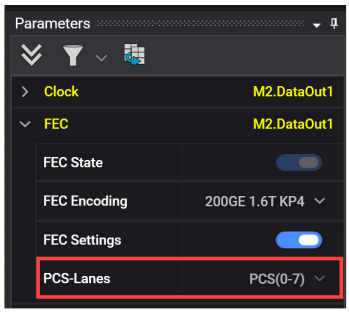
NOTE

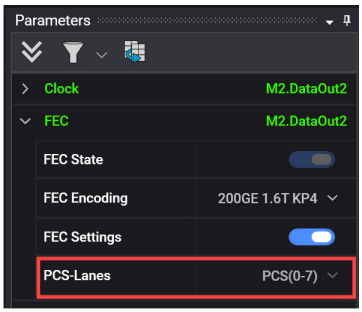
Note that the FEC settings are automatically disabled if the symbol rate falls outside the recommended range or if an invalid line coding is selected.

The M8070B software verifies whether the required FEC pattern is already loaded. If not, the software automatically opens the **Select Pattern** dialog (see Select Pattern Dialog on page 649) to load the pattern.

Example showing the symbol rate range option for FEC (200GE 1.6T KP4) is shown in this section.



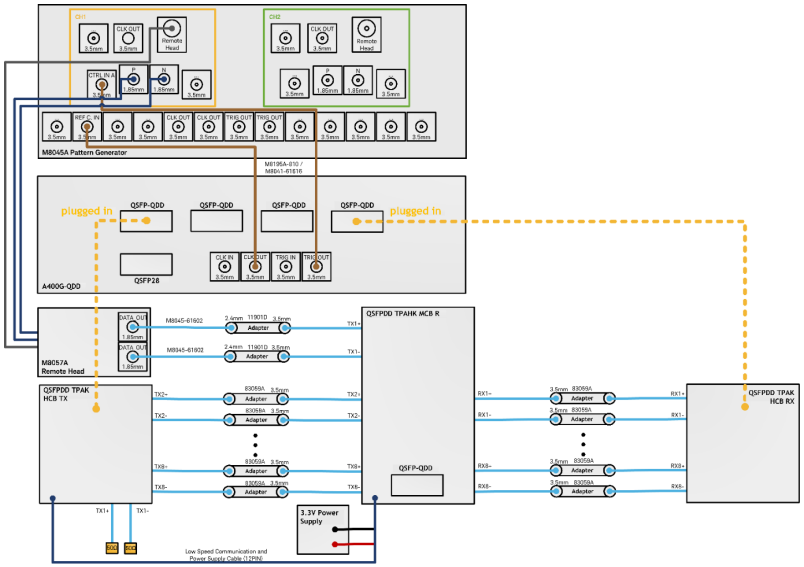




NOTE

For the 200G-2 and 400G-4 KP4 FEC modes , a A400GE-QDD or a G800GE is required to generate the electrical lanes carrying the residual PCS lanes. An external clock as well as a trigger is used to sync the PCS generated by the BERT with those from the A400GE-QDD/G800GE.

The following figure illustrates a loop-back test setup for evaluating the electrical Rx performance of a 400GAUI-8 optical transceiver. Test signals from the pattern generator are routed through the remote head to the QSFP-DD HCB, looped back via the HCB-Rx adapter, and captured by the error detector for BER measurement. Clock, trigger, power, and control connections ensure proper synchronization and operation during testing.

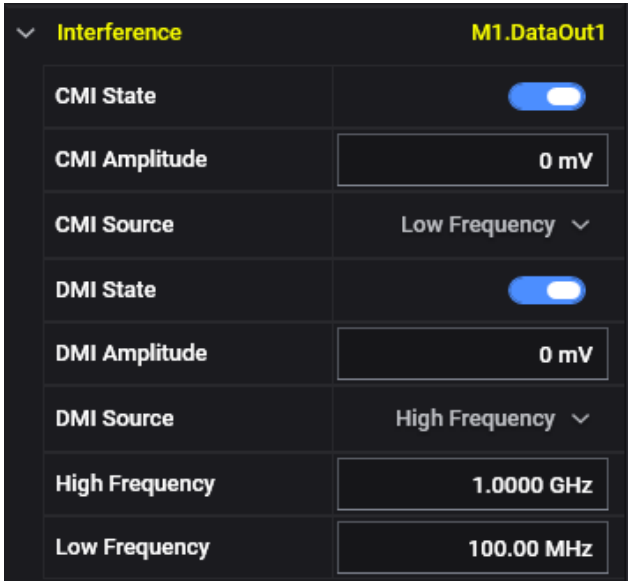


The following figure illustrates a high-speed test setup with an M8040A BERT connected to a G800GE platform and Wilder OSFP MCB. Two OSFP transceivers are linked via optical fibers for loop-back testing, with RF connections for signal transmission, a cooling fan for thermal management, and a PC for control and monitoring.

Interference

The M8020A supports the following two types of interference:

- Common Mode Interference (CMI)
- Differential Mode Interference (DMI)



Common Mode Interference (CMI)

Common Mode Interference (asymmetrical mode) relates to ground (CMI). It has the following characteristics:

- **State**: Enables / disables common mode interference (CMI).
- **Amplitude**: Specifies the amplitude of the common mode interference (CMI).
- **Frequency Source**: Specifies the frequency source for common mode interference (CMI). It can be high frequency source or low frequency source.

Differential Mode Interference (DMI)

Differential Mode Interference (DMI) - Differential Mode Interference (symmetrical mode) is independent of ground (DMI). It has the following characteristics:

- **State**: Enables / disables differential mode interference (DMI).
- **Amplitude**: Specifies the amplitude of the differential mode interference (DMI).
- **Frequency Source**: Specifies the frequency source for differential mode interference (DMI). It can be high frequency source or low frequency source.
- **High Frequency**: Specifies the frequency of the high frequency source.
- **Low Frequency**: Specifies the frequency of the low frequency source.

Jitter Setup

The **Jitter Setup** function is used for composing the total jitter in a defined and calibrated way.

The M8020A/M8040A/M8050A supports the following types of jitters:

- High Frequency Jitter (HF Jitter)
- Low Frequency Jitter (LF Jitter)

High Frequency Jitter (HF Jitter)

The **High Frequency Jitter** is a composition of the following types of jitters:

- Periodic Jitter 1
- Periodic Jitter 2
- Bounded Uncorrelated Jitter
- Random Jitter
- Spectrally Distributed Random Jitter
- External Jitter Source (Connected to the Delay Ctrl input)

NOTE For HF Jitter, the Periodic Jitter 1 and Periodic Jitter 2 values are entered as p-p values, and Random Jitter is entered in RMS.

Low Frequency Jitter (LF Jitter)

The **Low Frequency Jitter** is a composition of the following types of jitters:

- Periodic Jitter 1
- Periodic Jitter 2
- Residual Spread Spectrum Clock

NOTE For LF Jitter, the Periodic Jitter 1, Periodic Jitter 2 and Residual Spread Spectrum Clock Amplitude values are entered as p-p values.

How to Enable Global Jitter State

You can enable the global jitter state by selecting the **Enable Impairments** check box, present on the status bar of the GUI.

Set Jitter Configuration

In this section, an example of **Periodic Jitter 1** is shown to specify the jitter components.

To specify the jitter components:

- **Set Unit**: Defines the unit of jitter amplitude value in either seconds or UI.
- **Enable Jitter**: Enable the jitter source (press the corresponding button).
- **Set Parameters**: Set the most commonly used parameter (typically Amplitude and Frequency) directly.

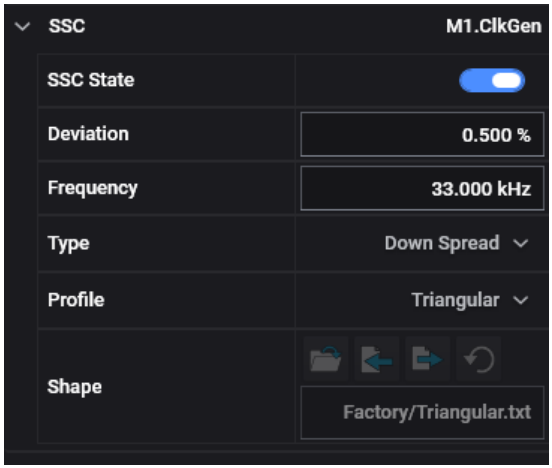
Spread Spectrum Clock

The **Spread Spectrum Clocking** setting controls the generator's spread spectrum (SSC) clocking feature. When the SSC is enabled, it impacts the Data Out, Clock Out, and Trigger Out ports.

The spread spectrum clock is characterized by:

- Deviation
- Frequency
- Type

- Profile
- Shape



- **Deviation**

  If the deviation type **Center Spread** is selected, the deviation can be changed in two different ways:

  - **Change the Center Spread value**: the bit rate remains unchanged, while the upper and lower frequency changes according to the selected deviation. The deviation value specifies ½ p-p value.
  - **Change the Down Spread value**: the upper frequency remains unchanged, while the bit rate is adjusted. The deviation value specifies the p-p value.

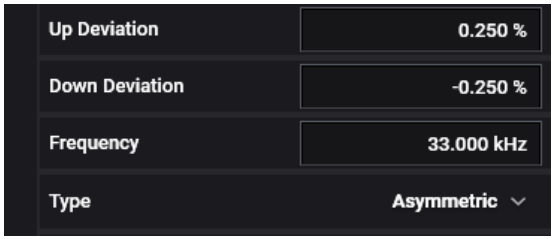
  For some setups, the I/Q modulator's range limitations require to use Center Spread instead of Down Spread and adjust the bit rate (and deviation) accordingly.

  If the upper or lower frequency is change, the bit rate will be adjusted according to the selected deviation. The center frequency corresponds to the configured bit rate.

  Please note that both the upper and lower frequency and the frequency adjustment of all three frequencies are not reflected in the firmware. The GUI just calculates the resulting bit rate and writes it to the firmware.

The **Deviation** of the clock rate. The ranges of SSC deviation are given below. For the maximum SSC range, refer to the *M8040A Data Sheet*.

- Down Spread with deviation of 0 ... 1 PPM
- Up Spread with deviation of 0 ... 1 PPM
- Center Spread with deviation of 0 ... 1 PPM
- Asymmetric allows to independently specify up and down deviation. When this is selected, the deviation is no longer specified in terms of peak-peak deviation, but independently for up and down deviation. The value ranges for the up deviation are 0 PPM to 1 PPM and for down deviation are -1 PPM to 0 PPM. The Asymmetric deviation type is only available in M8041A and M8046A modules.



NOTE The deviation in Upspread and Downspread is the p-p value while in Centerspread it is 1/2 p-p.

- **Frequency**: The deviation Frequency. The SCC provides the frequency range of 100 Hz – 200 kHz.
- **Type**: You can click the drop-down list to choose among Down Spread, Up Spread, Center Spread and Asymmetric deviation type.
- **Profile**: Controls the profile of the spread spectrum clocking. You can use the drop-down list to choose between the Triangular and Arbitrary profile.
- **Shape**: For Arbitrary profile, you need to specify the Arbitary Waveform file. It is a simple text file that contains the data points which define the arbitrary waveform of the SSC profile.

NOTE

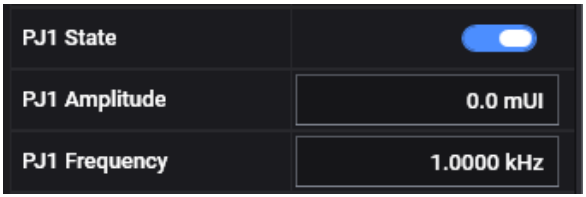
The Spread Spectrum Clocking setting follows the following:

- Available on M8041A, M8042A and M8045A
- (Only for Center-Spread SSC) No signal clock/signal disruption when changing
  - **SSC state**
  - **SSC deviation**
  - **SSC frequency**
- When using up-spread or down-spread, changing one of the above parameters causes a clock-loss and therefore signal disruption.
- In center-spread mode, the SSC parameters get applied to the next period of the SSC waveform.

Periodic Jitter 1

The **Periodic Jitter 1** is characterized by:

- Amplitude
- Frequency

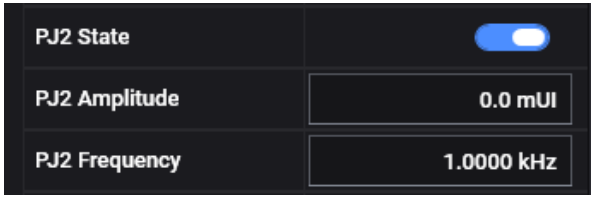


- **Amplitude**: Controls the amplitude of periodic jitter 1.
- **Frequency**: Controls the frequency of the periodic jitter 1.

Periodic Jitter 2

The **Periodic Jitter 2** is characterized by:

- Amplitude
- Frequency



- **Amplitude**: Controls the amplitude of periodic jitter 2.
- **Frequency**: Controls the frequency of the periodic jitter 2.

Specify the Components for Jitter Sweep

The **Periodic Jitter 2** has the following modes:

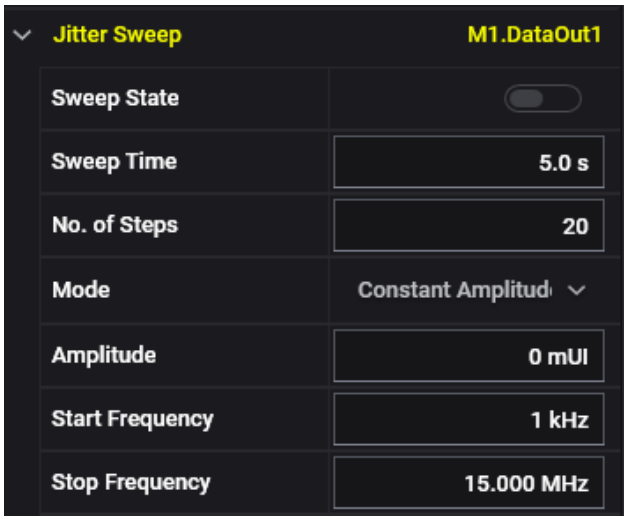
- Constant Amplitude Sweep
- Variable Amplitude Sweep

To specify the components of jitter sweep select **Jitter Sweep** functional block from the **Parameter** window and then select the **Mode** from the drop-down list to specify components the jitter sweep.

Periodic Jitter 2 – Constant Amplitude Sweep Parameters

The **Periodic Jitter 2 – Constant Amplitude Sweep** is characterized by:

- Amplitude
- Frequency Range
- Sweep Time
- No. of Steps

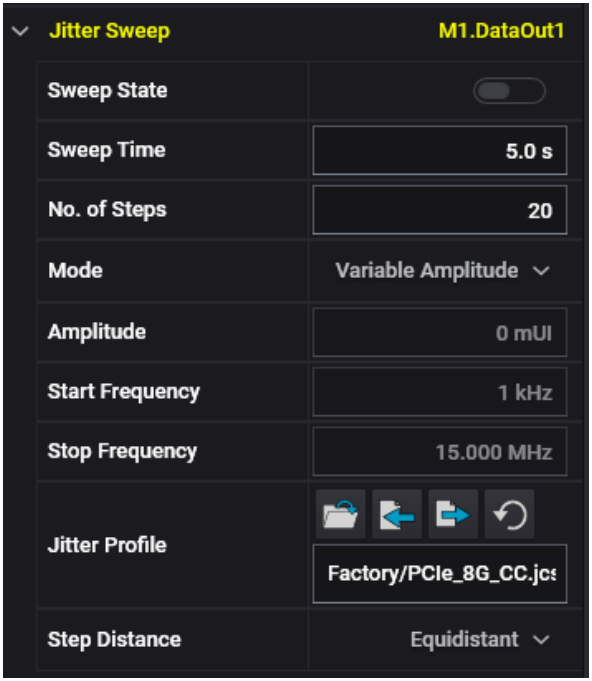


- **Amplitude**: The maximum peak-to-peak Amplitude is limited by the free capacity of the chosen delay line.
- **Frequency Range**: The stop frequency has to be higher than start frequency and the range should be in accordance with the selected waveform.
- **Sweep Time**: You can specify the duration for sweeping the specified frequency range once.
- **No. of Steps**: You can specify the number of steps to fulfill a complete sweep. The start and stop values are included. The valid range is between 2 to 100.

Periodic Jitter 2 – Variable Amplitude Sweep Parameters

The **Periodic Jitter 2 – Variable Amplitude Sweep** is characterized by:

- Standard
- Sweep Time
- No. of Steps
- Step Distance



- **Standard**: You can use this drop-down list to specify whether you want to select a pre-defined standard or a user-defined standard. All the available predefined standards will be shown in this list. However, if you select the user-defined standard, press **Jitter Profile** button to locate the **Jitter Tolerance** standard. The user-defined standard uses the same file format like the **Jitter Tolerance Compliance** measurement.

NOTE Selecting the Standard does allocate the required amount of jitter modulation on the delay line being used. To avoid errors when changing the selection, it is recommended to either select the corresponding bit rate first, or enable the PJ2 source after setting the correct bit rate.

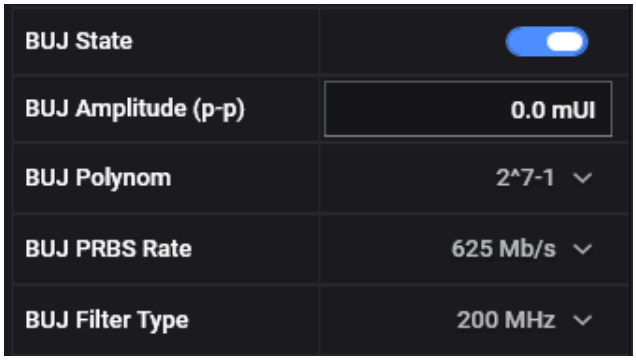
- **Sweep Time**: You can specify the duration for sweeping the selected jitter profile/standard once.

- **No. of Steps**: You can specify the number of steps to fulfill a complete sweep. The start and stop values are included. The valid range is between 2 to 100.
- **Step Distance**: You can use this drop-down list to specify whether the frequency steps are log equidistant (EQUidistant) along the periodic jitter curve or a frequency step matches a corner frequency on the periodic jitter curve.

Bounded Uncorrelated Jitter

Bounded Uncorrelated Jitter is characterized by

- Amplitude
- PRBS polynomial
- Data rate
- Filter type

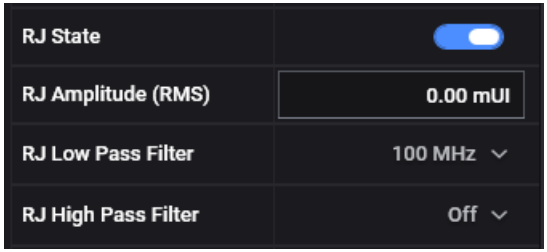


- **Amplitude**: Controls the amplitude of the BUJ jitter source.
- **PRBS polynomial**: The PRBS polynomial can be chosen from a list. Available are eight polynomials, from 2^7-1 up to 2^31-1.
- **Data Rate**: Enter an appropriate **Data Rate**.
- **Filter Type**: The bounded uncorrelated jitter source is equipped with three low-pass filters with cut-off frequencies at 50, 100, and 200 MHz. One of these filters is always active.

Random Jitter

Random Jitter is characterized by:

- Amplitude
- Filter Settings



- **RJ State**: Click this switch to enable the random jitter.
- **RJ Amplitude**: The random jitter amplitude must be entered as an rms (root mean square) value.
- **RJ Low Pass Filter**: Controls the low pass filter of the random jitter source. The random jitter source is equipped with a 100 MHz, 500 MHz and 1 GHz low pass filter to limit the spectral range. For M8020A and M8040A, it is also possible to set the low pass filter of the random jitter 500 MHz at or below 3.75 Gb/s.
- **RJ High Pass Filter**: Controls the high pass filter of the random jitter source. The random jitter source is equipped with a 10 MHz high pass to limit the spectral range.

NOTE Please note that the minimum data rate must be set 8 GHz in order to set the RJ low pass filter to 1 GHz.

Spectrally Distributed Random Jitter

Spectrally Distributed Random Jitter is composed of two jitter sources: low frequency jitter and high frequency jitter. It is characterized by the amplitudes of the low and the high frequency jitter.

NOTE The sRJ on M8045A requires M8045A-0G3 license.

Spectral Distributed Random Jitter is characterized by

- Amplitude LF
- Amplitude HF

It has the following parameters:

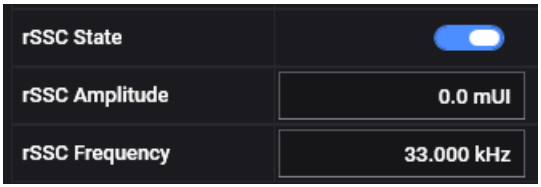
- **sRJ State**: Click this switch to enable the spectrally distributed random jitter.
- **SRJ Amplitude 1 (RMS) LF**: This is the low frequency jitter amplitude as rms value.
- **SRJ Amplitude 2 (RMS) HF**: This is the high frequency jitter amplitude as rms value.
- **sRJ Low Pass Filter**: The spectrally distributed random jitter is equipped with a 100 MHz low pass filter to limit the spectral range, which can be enabled by pressing the corresponding switch.

Residual Spread Spectrum Clock

The **Residual Spread Spectrum Clock** (rSSC) is generated by modulating the clock that is used for data generation.

The Residual Spread Spectrum Clock is characterized by:

- rSSC Amplitude
- rSSC Frequency



It has the following parameters:

- **rSSC State**: Click this button to enable/disable the Residual Spread Spectrum Clock.
- **rSSC Amplitude**: This is the amplitude of the rSSC jitter source.
- **rSSC Frequency**: This is the frequency of the rSSC jitter source.

External Jitter Source

To enable the external jitter source:

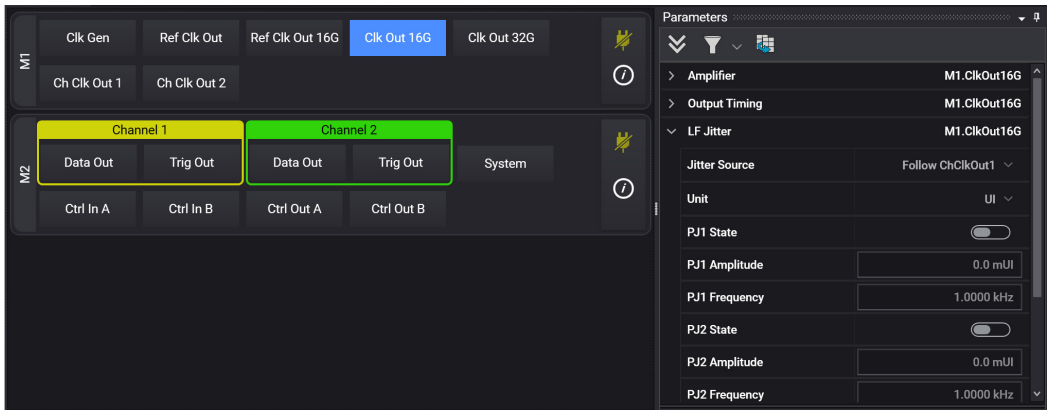
- From the **Data Out** port select **HF Jitter** functional block in the **Parameters** window.
- Click the **External** switch to enable external jitter.

NOTE Even if the external jitter source is enabled, you can still add or change internal jitter components.

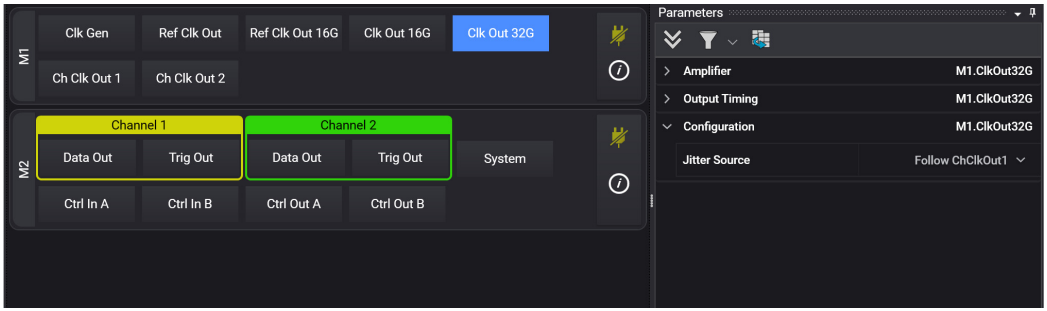
Automatic Jitter Parameter Synchronization in M8009A Clock Module

To support PCIe test configurations with Jitter Tolerance measurements, the Jitter parameters can be automatically copied from ChClkOut1 to ClkOut16G/32G of the M8009A Clock Module. A Jitter Source parameter is available for both ClkOut16G LF Jitter and ClkOut32G.

- **ClkOut16G LF Jitter**: This parameter is read-only and is automatically copied from the Jitter Source parameter in ClkOut32G. If ChClkOut1 is selected, the Jitter Source parameters (Amplitude and Frequency) are copied from ChClkOut1. The Jitter Source state can be toggled on or off independently.



- **ClkOut32G**: If Follow ChClkOut1 is selected, the Jitter Source parameters (Frequency, Amplitude, and State) are copied from ChClkOut1. Similarly, if Follow ClkOut16G is selected, the Jitter Source parameters (Frequency, Amplitude, and State) are copied from ClkOut16G.



Idle Pattern

Idle pattern is used during the time when the sequence is downloading. At this time, the pattern generator sequence patterns are not ready for frame generation.

Follow the given steps to apply the idle pattern:

1 From the Data Out port select Data functional block in the Parameters window.

2 Select Idle Pattern as PRBS or Static 0.

TxEQ Matrix Editor

The **TxEQ Matrix Editor** enables you to either create a new TxEQ coefficient matrix or modify an existing matrix to support PCIe deemphasis values.

Launching the TxEQ Matrix Editor

To launch the **TxEQ Matrix Editor** from the M8070B application, follow one of the following procedures:

- Launching the TxEQ Matrix Editor through M8070B Menu Bar
- Launching the TxEQ Matrix Editor through M8070B Module View Parameters Window

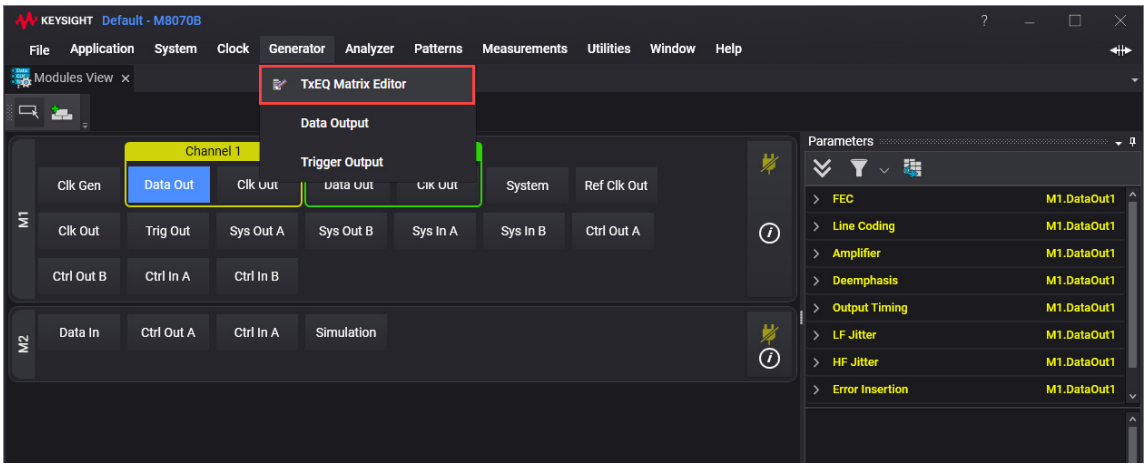
Launching the TxEQ Matrix Editor through M8070B Menu Bar

Prerequisites

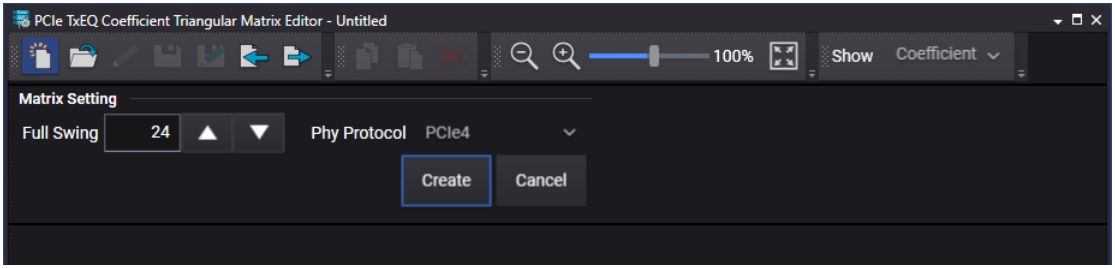
- The PG module must be connected
- The PCIe LTSSM licenses must be installed

To launch the TxEQ Matrix Editor through M8070B Menu Bar, perform the following steps:

- Go to **Menu Bar > Generator > TxEQ Matrix Editor**.



The **PCIe TxEQ Coefficient Triangular Matrix Editor - Untitled** window appears.



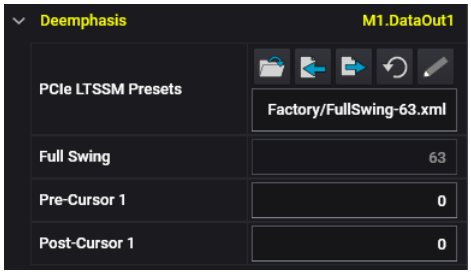
Launching the TxEQ Matrix Editor through M8070B Module View Parameters Window

Prerequisites

- The PCIe option must be selected under the PHY Protocol drop-down list in the Sequence Configuration parameter. For more information, refer to M8046A PHY Protocol Selection (SKP OS Filtering) .

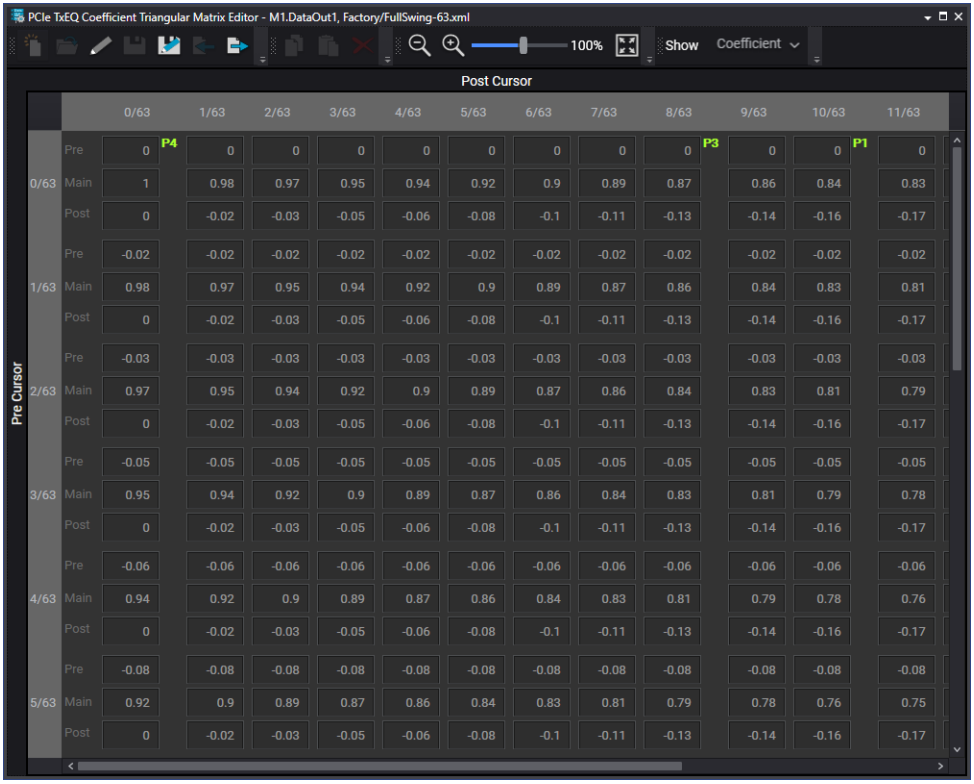
To launch the **TxEQ Matrix Editor** through M8070B Module View Parameters window, perform the following steps:

1 Go to M8070B Module View > **Data Out > Parameters > Deemphasis > PCIe LTSSM Presets.**



2 Click the **Edit TxEQ Matrix** icon.

The **PCIe TxEQ Matrix Editor** appears for the selected file. The PCIe TxEQ Matrix Editor title bar displays the module number and the factory file selected.

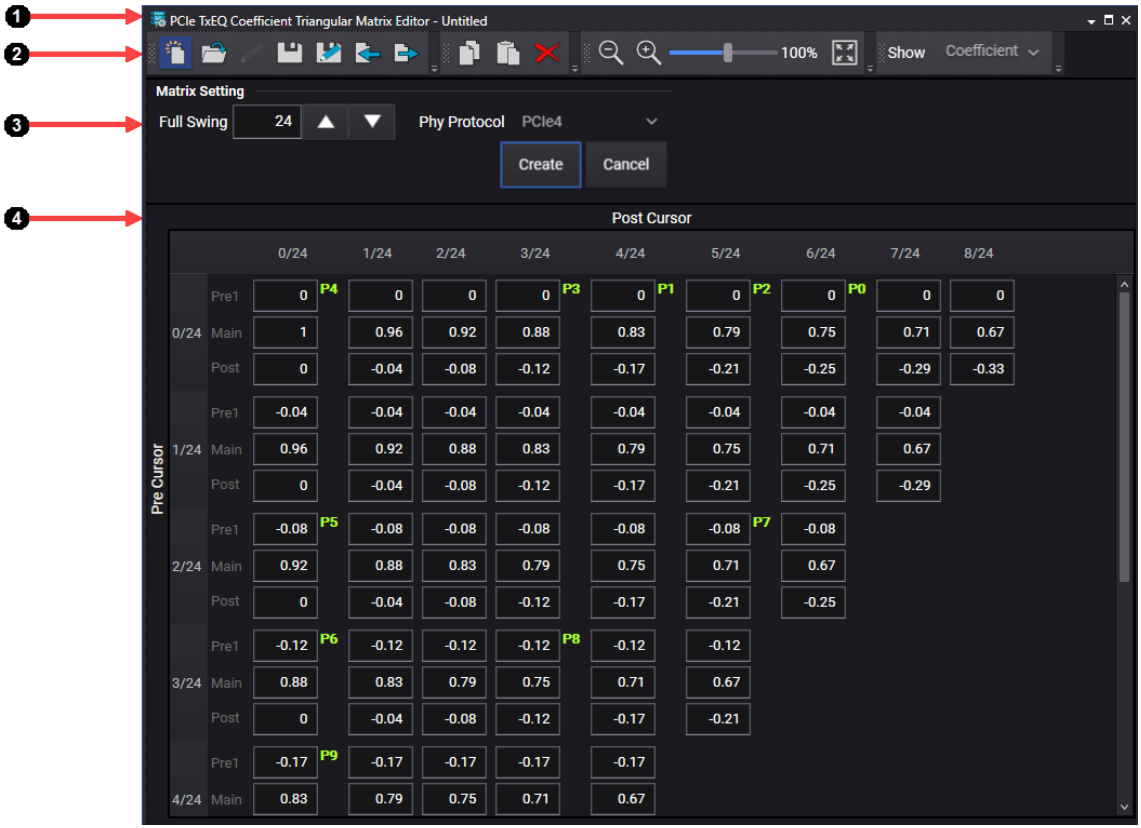


Pre Cursor		0/63	1/63	2/63	3/63	4/63	5/63	6/63	7/63	8/63	9/63	10/63	11/63
0/63	Pre	0 (P4)	0	0	0	0	0	0	0	0 (P3)	0	0 (P1)	0
	Main	1	0.98	0.97	0.95	0.94	0.92	0.9	0.89	0.87	0.86	0.84	0.83
	Post	0	-0.02	-0.03	-0.05	-0.06	-0.08	-0.1	-0.11	-0.13	-0.14	-0.16	-0.17
1/63	Pre	-0.02	-0.02	-0.02	-0.02	-0.02	-0.02	-0.02	-0.02	-0.02	-0.02	-0.02	-0.02
	Main	0.98	0.97	0.95	0.94	0.92	0.9	0.89	0.87	0.86	0.84	0.83	0.81
	Post	0	-0.02	-0.03	-0.05	-0.06	-0.08	-0.1	-0.11	-0.13	-0.14	-0.16	-0.17
2/63	Pre	-0.03	-0.03	-0.03	-0.03	-0.03	-0.03	-0.03	-0.03	-0.03	-0.03	-0.03	-0.03
	Main	0.97	0.95	0.94	0.92	0.9	0.89	0.87	0.86	0.84	0.83	0.81	0.79
	Post	0	-0.02	-0.03	-0.05	-0.06	-0.08	-0.1	-0.11	-0.13	-0.14	-0.16	-0.17
3/63	Pre	-0.05	-0.05	-0.05	-0.05	-0.05	-0.05	-0.05	-0.05	-0.05	-0.05	-0.05	-0.05
	Main	0.95	0.94	0.92	0.9	0.89	0.87	0.86	0.84	0.83	0.81	0.79	0.78
	Post	0	-0.02	-0.03	-0.05	-0.06	-0.08	-0.1	-0.11	-0.13	-0.14	-0.16	-0.17
4/63	Pre	-0.06	-0.06	-0.06	-0.06	-0.06	-0.06	-0.06	-0.06	-0.06	-0.06	-0.06	-0.06
	Main	0.94	0.92	0.9	0.89	0.87	0.86	0.84	0.83	0.81	0.79	0.78	0.76
	Post	0	-0.02	-0.03	-0.05	-0.06	-0.08	-0.1	-0.11	-0.13	-0.14	-0.16	-0.17
5/63	Pre	-0.08	-0.08	-0.08	-0.08	-0.08	-0.08	-0.08	-0.08	-0.08	-0.08	-0.08	-0.08
	Main	0.92	0.9	0.89	0.87	0.86	0.84	0.83	0.81	0.79	0.78	0.76	0.75
	Post	0	-0.02	-0.03	-0.05	-0.06	-0.08	-0.1	-0.11	-0.13	-0.14	-0.16	-0.17

Exploring the TxEQ Matrix Editor User Interface

The **TxEQ Matrix Editor** user interface includes the following elements:

1. Title Bar
2. Menu Bar
3. Matrix Setting pane
4. Matrix Editor Pane



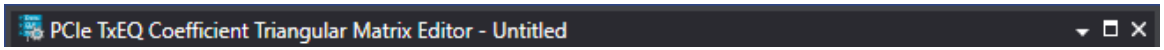
Title Bar

The title bar displays the application icon, title of the file, Options drop-down arrow, and the standard buttons to maximize or to close the window.

The **Options** drop-down arrow includes the following:

- **Close** - Closes the TxEQ Matrix Editor window.
- **Dock** - Docks the TxEQ Matrix Editor window with the other open tabs.

The title bar is shown in the following figure.



Menu Bar

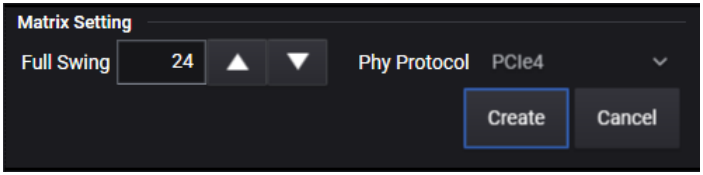
The menu bar includes the following elements:

Elements	Name	Description
	New (CTRL + N)	Allows you to create a new matrix. For more information, refer to Creating a new matrix . **NOTE**: This option is enabled only when you launch the TxEQ Matrix Editor through M8070B Menu Bar.
	Open (CTRL + O)	Allows you to open an existing file to modify/edit. On click of **Open** icon, the Open PCIe LTSSM deemphasis presets dialog box appears. For more information, refer to Opening an existing matrix . **NOTE**: This option is enabled only when you launch the TxEQ Matrix Editor through M8070B Menu Bar.
	Edit	Allows you to make changes to an existing file. For more information, refer to Editing an existing matrix .
	Save (CTRL + S)	Allows you to save the file on your local system. On click of **Save** icon, the Save PCIe LTSSM deemphasis presets dialog box appears. **NOTE**: The Factory files cannot be saved using the **Save** option. Use **Save as** option to save any changes at different location.
	Save as (F12)	Allows you to save a copy of opened matrix to a new location. On click of **Save as** icon, the Save PCIe LTSSM deemphasis presets dialog box appears.

Elements	Name	Description
	Import (CTRL + I)	Allows you to import any existing matrix file from any location to M8070B workspace to edit. On click of **Import** icon, the Select PCIe LTSSM deemphasis presets To Import dialog box appears, which enables you to import the file. For more information, refer to Importing a matrix file . **NOTE**: This option is enabled only when you launch the TxEQ Matrix Editor through M8070B Menu Bar.
	Export (CTRL + E)	Allows you to export the current matrix to a file to any location. On click of **Export** icon, the Open PCIe LTSSM deemphasis presets dialog box appears, which enables you to export the file. For more information, refer to Exporting a matrix file .
	Copy	Allows you to copy any cell from the matrix editor. This option is enabled only when any cell/value is selected in matrix editor.
	Paste	Allows you to paste any valid value from clipboard to matrix value. This option is enabled only when there is any valid data to paste in the matrix editor.
	Delete	Allows you to delete any cell value from the matrix editor. This option is enabled only when any cell/value is selected in matrix editor.
100%	Zoom-In/Zoom-Out	Allows you to zoom-in and zoom-out the value of each cell of the matrix. By default, the matrix editor pane appears in Fit to Display mode.
	Fit to Display	Allows you to display the Matrix Editor pane in the current view without any scroll bars.
Show Coefficient Coefficient dB	Show drop-down list	Allows you to select an option from the **Show** drop-down list. The following options are available: • Coefficient : Enables you to edit the cell values in the Matrix Editor pane. • dB : Displays the matrix cell value in decibels. It displays the data in read-only mode, that is, the cell values cannot be edited in this mode.

Matrix Setting pane

The Matrix Setting pane enables you to change the settings of the matrix editor. This pane is accessible only when you launch the TxEQ Matrix Editor through the M8070B Menu Bar. For more information on launching, refer to Launching the TxEQ Matrix Editor through M8070B Menu Bar . The matrix settings pane enables you to set the Full Swing value, Phy Protocol, and create the matrix. The acceptable range for Full Swing value is 24 - 63.

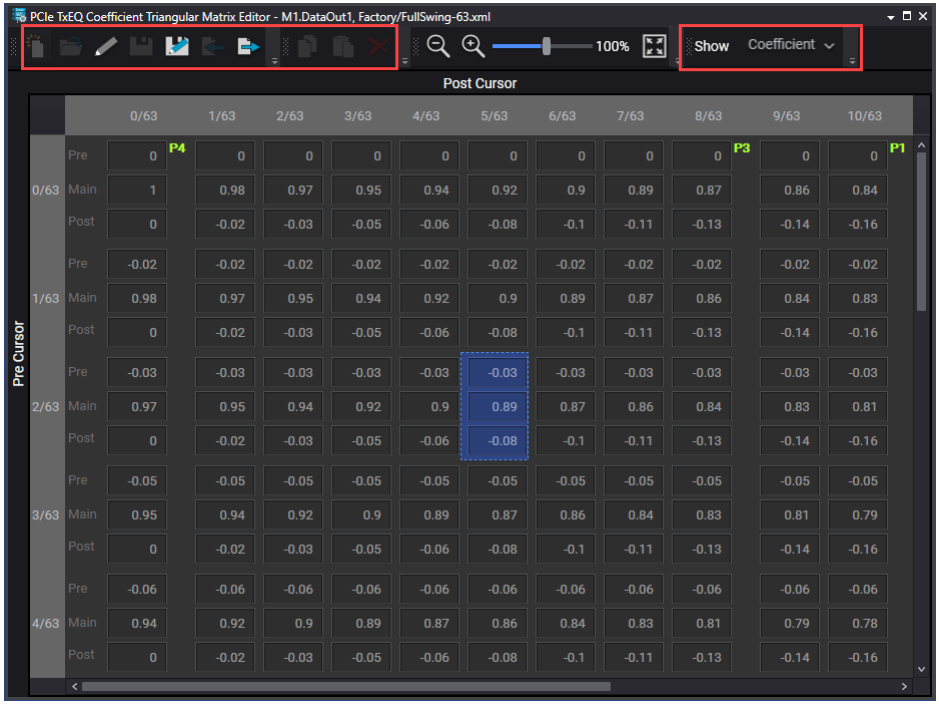


Matrix Editor Pane

The Matrix Editor pane enables you to edit any value of the opened matrix file. You can edit the value of the matrix cells when **Show** mode from the Matrix Setting is selected as **Coefficient**.

The Matrix Editor pane displays the following values in each cell:

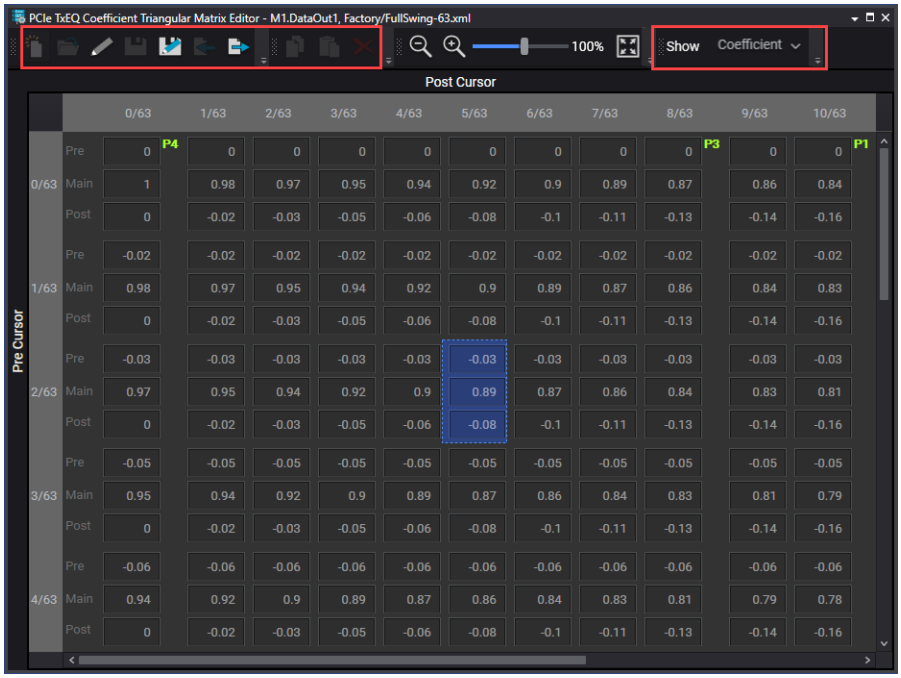
- Pre-Cursor
- Main
- Post-Cursor



The Matrix Editor pane includes the following features:

- The horizontal pane displays the Post-Cursor value and the vertical pane displays the Pre-Cursor value.
- You can use the arrow keys, ENTER, TAB, or single click to navigate to the required matrix cell. The currently selected cell is highlighted by blue borders.

- If you launch the TxEQ Matrix Editor through the M8070B Module View parameters window, you can press CTRL + ENTER or double-click the desired cell to apply the currently selected value to the respective channel. This feature is applicable only when you are in non-editing mode and data is displayed as coefficient.

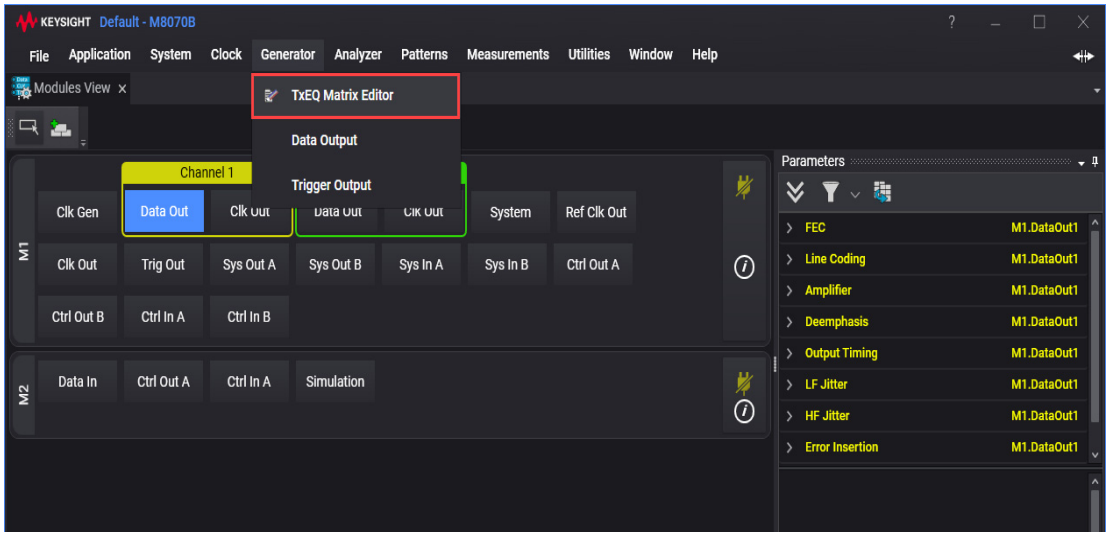


Creating a new matrix

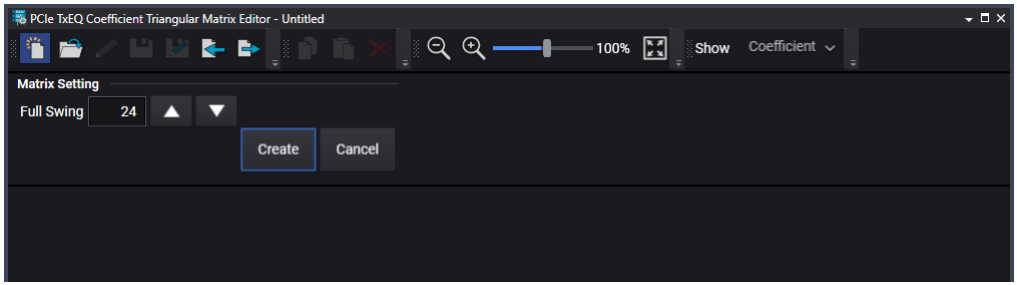
To create a new matrix, perform the following steps:

1 Go to **Menu Bar > Generator > TxEQ Matrix Editor**.

NOTE This option is available only when you launch the TxEQ Matrix Editor through M8070B Menu Bar.



The **PCIe TxEQ Matrix Editor - Untitled Matrix** window appears.



2 On the Tool Bar, click **New** icon. By default, this option is displayed.

3 Under the **Matrix Setting** pane, do the following:

a Enter the appropriate value in the **Full Swing** text box.

You can use the Up/Down icons to increase or decrease the Full Swing value.

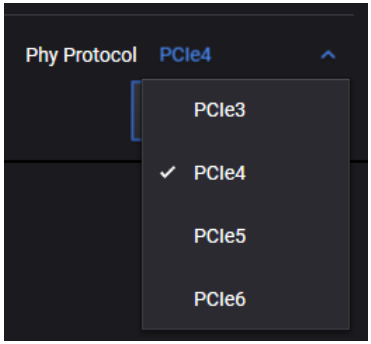
The acceptable range for Full Swing value is 24 - 63.

b Select an appropriate option from the Phy Protocol drop-down list.

The following options are available:

- PCIe3
- PCIe4
- PCIe5
- PCIe6

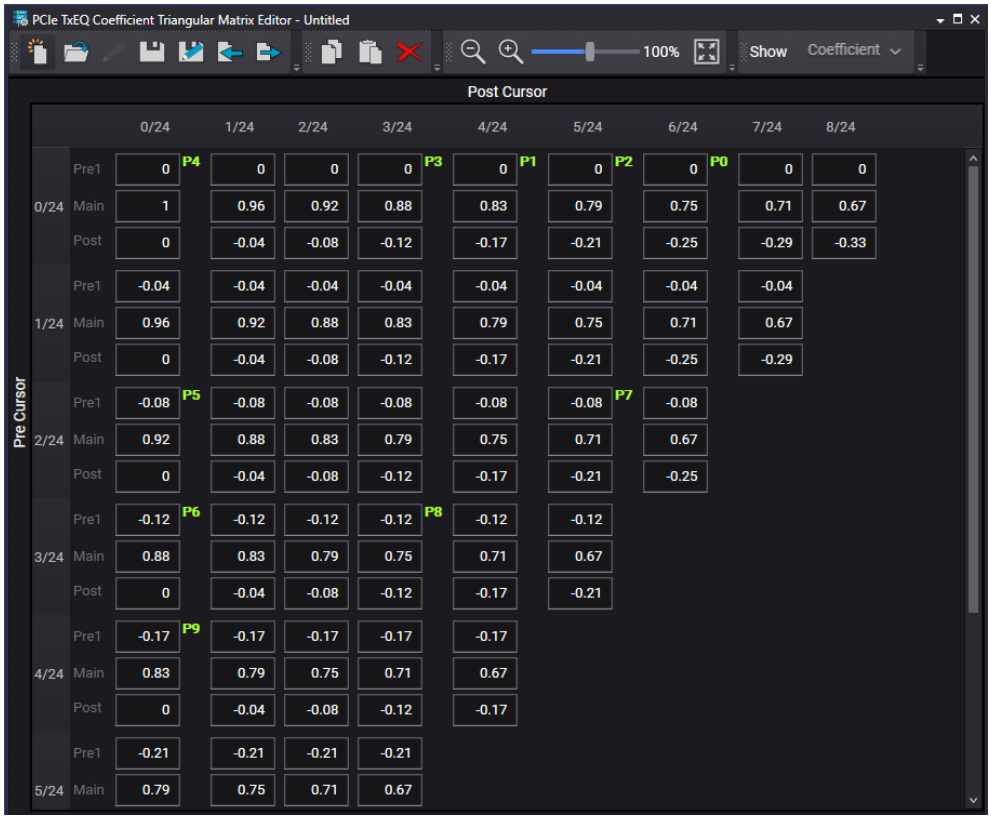
By default, PCIe4 is selected.



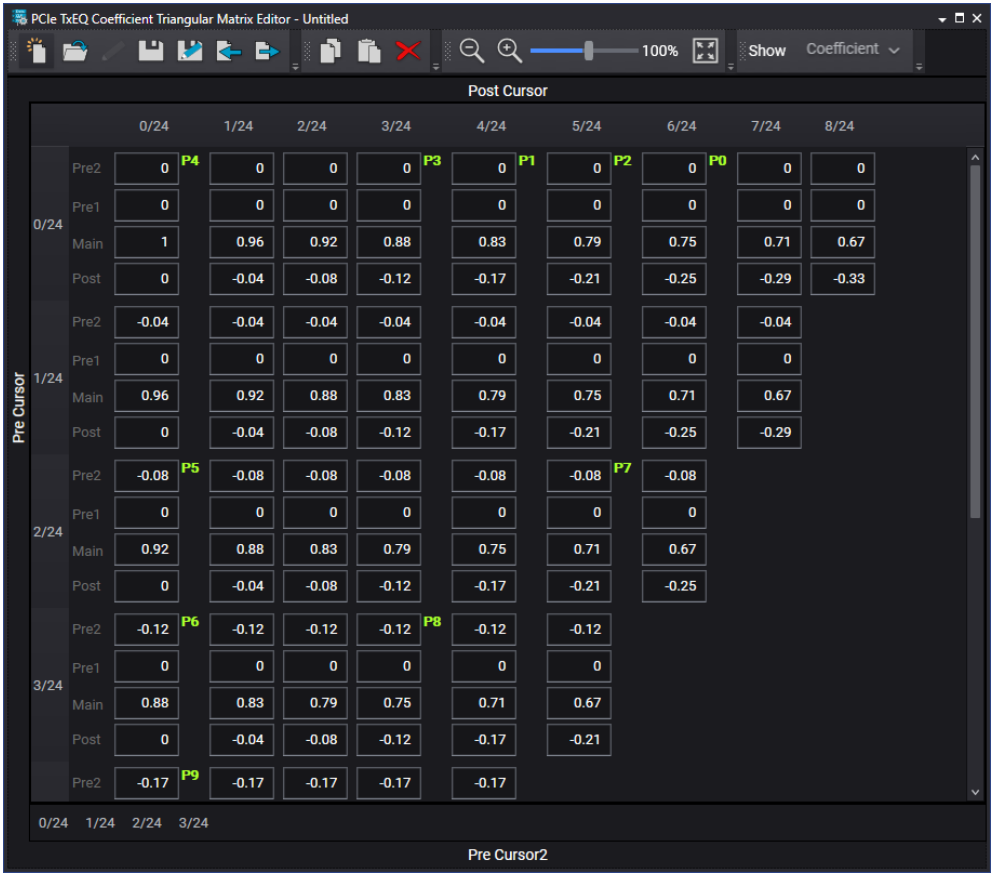
c Click **Create**.

The **PCIe TxEQ Matrix Editor** pane displays the matrix as per the value entered.

- When you select any of the PCIe3, 4, 5 protocols, the old matrix (NRZ) will be created/opened.

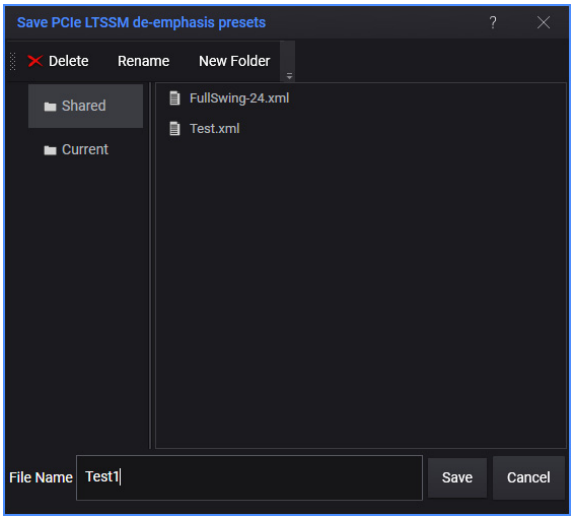


- When you select the PCIe6 protocol, the old matrix (PAM4) will be created/opened.



NOTE When you launch the TxEQ Matrix Editor through the module view parameters window, the type of matrix editor depends on the selected Phy protocol in sequence editor.

4 Click **Save** icon to save the matrix.
The **Save PCIe LTSSM deemphasis presets** dialog box appears.



5 On the **Save PCIe LTSSM deemphasis presets** dialog box, do the following:

a Select a folder where you want to save the file.

By default, two folders; **Shared** and **Current** are available. Click **New Folder** to create a new folder.

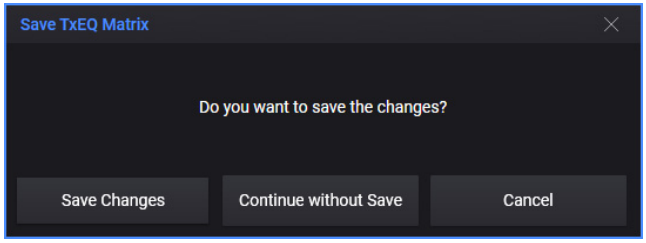
b Type an appropriate name for the file in the **File Name** text box.

c Click **Save**.

The file is saved at the location. The PCIe TxEQ Matrix Editor title bar displays the name of the selected file.

NOTE

If you start a new process (Open, Import, Export, or Close) without saving the current matrix, the **Save TxEQ Matrix** dialog box appears.



The following options are available:

- **Save Changes**: Saves the changes to the file. The **Save PCIe LTSSM deemphasis presets** dialog box appears.
- **Continue without Save**: Continues with the new process without saving the current file to the system.
- **Cancel**: Cancels the new process and the user remains in the editor window.

Opening an existing matrix

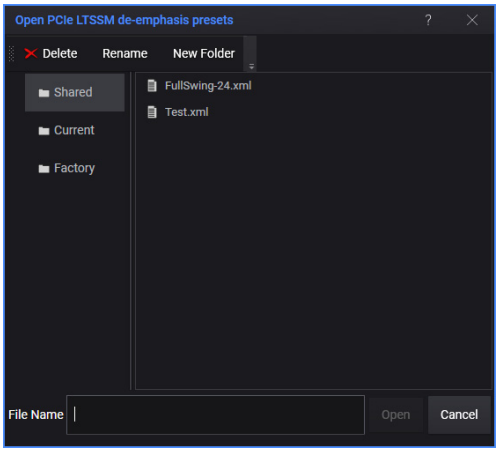
To open an existing matrix, perform the following steps:

1 Launch the TxEQ Matrix Editor through M8070B Menu Bar.

For more information, refer to Launching the TxEQ Matrix Editor through M8070B Menu Bar on page 442.

2 Click Open icon.

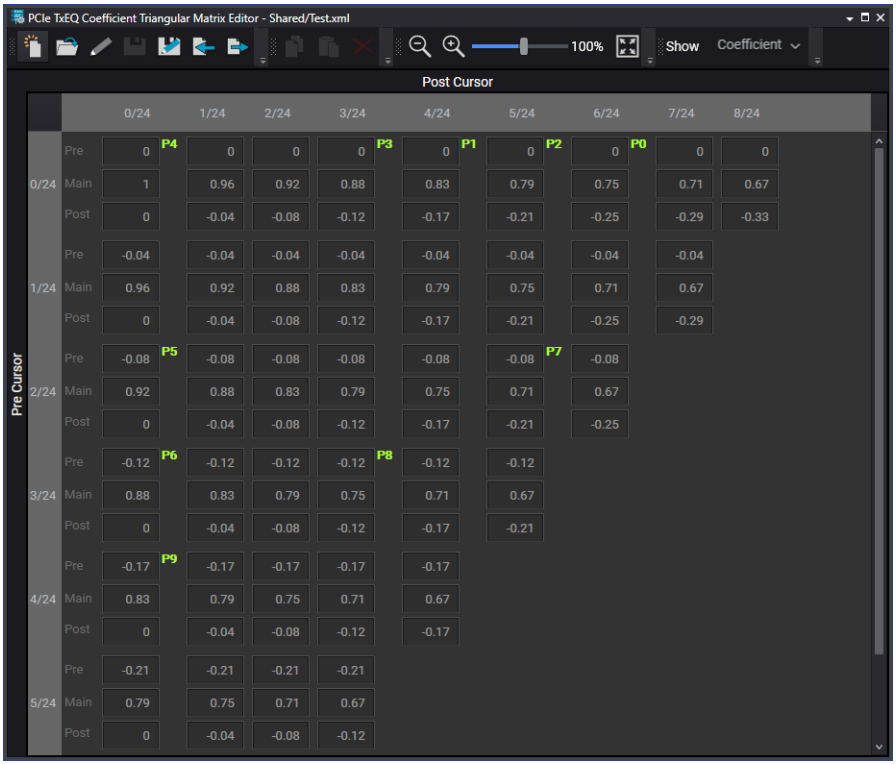
The **Open PCIe LTSSM deemphasis presets** dialog box appears.



3 On the **Open PCIe LTSSM deemphasis presets** dialog box, select the appropriate file.

4 Click **Open**.

The TxEQ Matrix Editor displays the selected file. The PCIe TxEQ Matrix Editor title bar displays the name of the selected file.



Pre Cursor		0/24	1/24	2/24	3/24	4/24	5/24	6/24	7/24	8/24
0/24	Pre	0 P4	0	0	0 P3	0 P1	0 P2	0 P0	0	0
	Main	1	0.96	0.92	0.88	0.83	0.79	0.75	0.71	0.67
	Post	0	-0.04	-0.08	-0.12	-0.17	-0.21	-0.25	-0.29	-0.33
1/24	Pre	-0.04	-0.04	-0.04	-0.04	-0.04	-0.04	-0.04	-0.04	
	Main	0.96	0.92	0.88	0.83	0.79	0.75	0.71	0.67	
	Post	0	-0.04	-0.08	-0.12	-0.17	-0.21	-0.25	-0.29	
2/24	Pre	-0.08 P5	-0.08	-0.08	-0.08	-0.08	-0.08 P7	-0.08		
	Main	0.92	0.88	0.83	0.79	0.75	0.71	0.67		
	Post	0	-0.04	-0.08	-0.12	-0.17	-0.21	-0.25		
3/24	Pre	-0.12 P6	-0.12	-0.12	-0.12 P8	-0.12	-0.12			
	Main	0.88	0.83	0.79	0.75	0.71	0.67			
	Post	0	-0.04	-0.08	-0.12	-0.17	-0.21			
4/24	Pre	-0.17 P9	-0.17	-0.17	-0.17	-0.17				
	Main	0.83	0.79	0.75	0.71	0.67				
	Post	0	-0.04	-0.08	-0.12	-0.17				
5/24	Pre	-0.21	-0.21	-0.21	-0.21					
	Main	0.79	0.75	0.71	0.67					
	Post	0	-0.04	-0.08	-0.12					

Editing an existing matrix

To edit an existing file, perform one of the following:

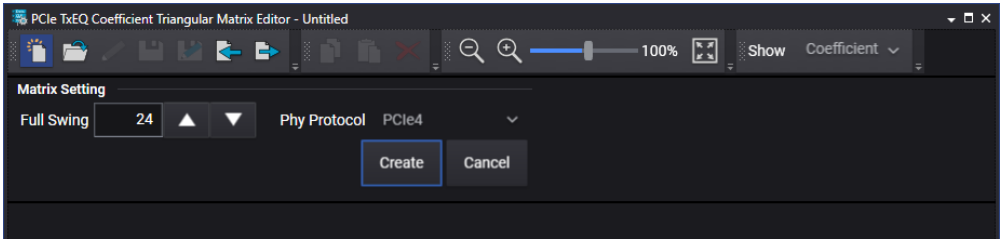
- Editing an existing file (TxEQ Matrix Editor through M8070B Menu Bar)
- Editing an existing file (TxEQ Matrix Editor through M8070B Module View Parameters Window)

Editing an existing file (TxEQ Matrix Editor through M8070B Menu Bar)

When you launch the TxEQ Matrix Editor through M8070B menu bar, perform the following steps to edit an existing matrix.

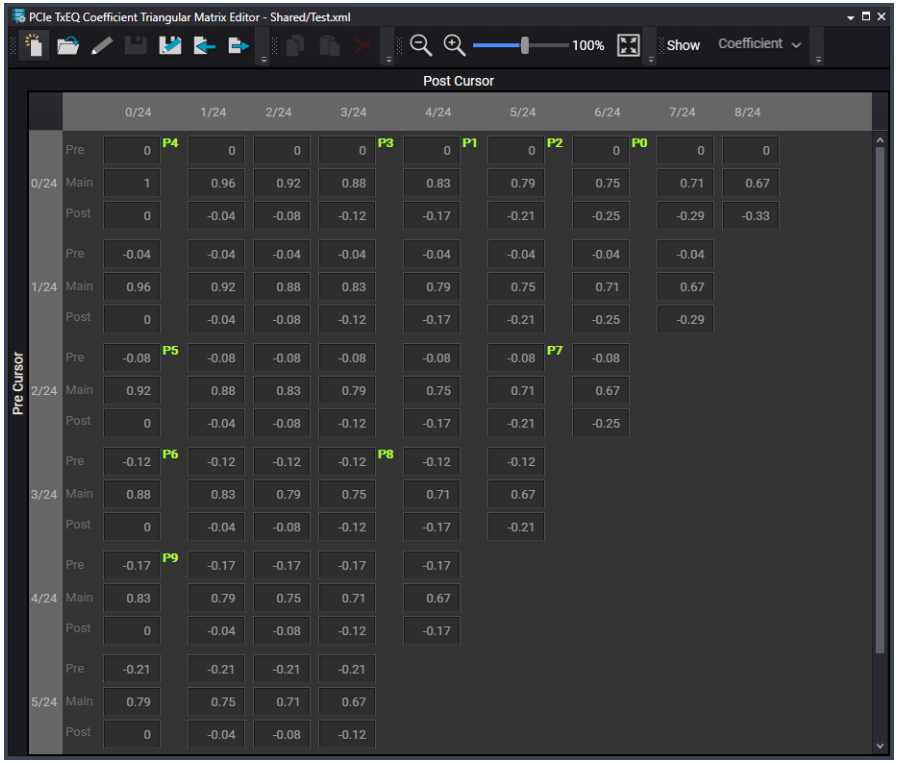
1 Go to Menu Bar > **Generator > TxEQ Matrix Editor**.

The **PCIe TxEQ Matrix Editor - Untitled Matrix** window appears.

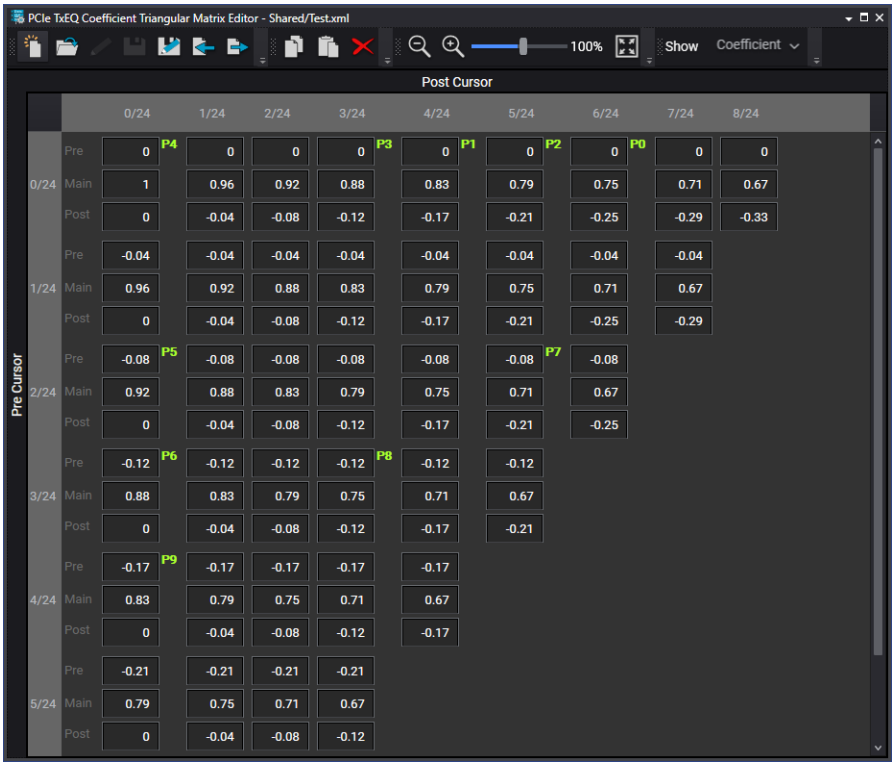


2 Click **Open** icon to open an existing file for editing. Refer to Opening an existing matrix on page 458, for more information.

The TxEQ Matrix Editor displays the selected file.



3 On the **PCIe TxEQ Matrix Editor**, click **Edit** icon.
The PCIe Matrix Editor enables you to edit the cell values.

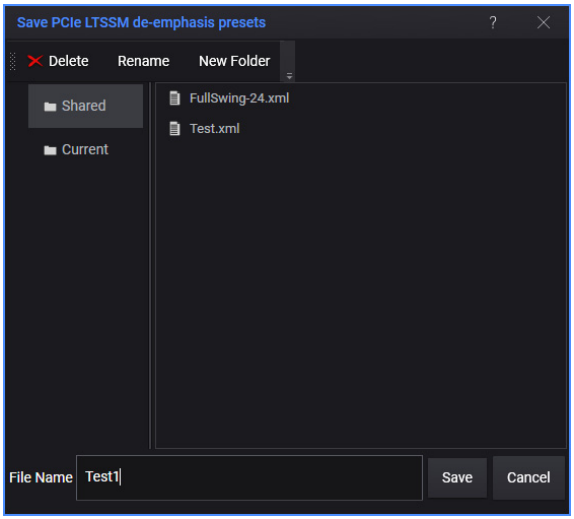


The Save, Save as, Copy, Paste, and Delete icons are enabled in Edit mode. The Save option is enabled when you modify any of the cell value.

4 After all the modifications are done, do one of the following:
   - Click **Save** icon to save the file.
   - Click **Save as** icon to save the copy of the file to a new location.

NOTE The Factory files cannot be saved using the **Save** option. Use **Save as** option to save any changes at different location.

When the **Save as** option is clicked, the **Save LTSSM deemphasis presets** dialog box appears.



5 (Optional) On the **Save PCIe LTSSM deemphasis presets** dialog box, do the following:

a Select a folder where you want to save the file.

By default, two folders; Shared and Current are available. Click **New Folder** to create a new folder.

b Type an appropriate name for the file.

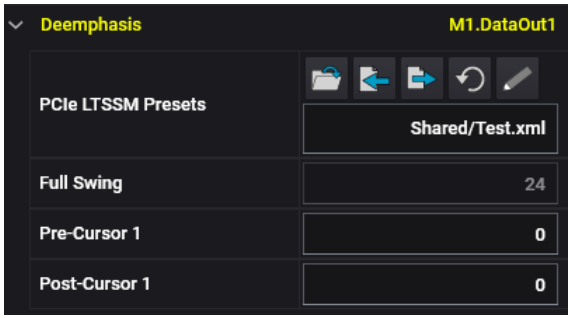
c Click **Save**.

The file is saved at the location. The PCIe TxEQ Matrix Editor title bar displays the name of the selected file.

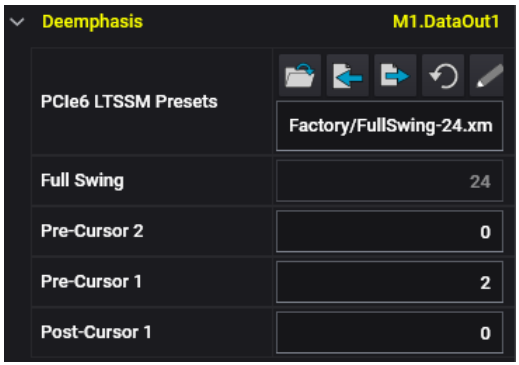
Editing an existing file (TxEQ Matrix Editor through M8070B Module View Parameters Window)

When you launch the TxEQ Matrix Editor through M8070B module view parameters window, perform the following steps to edit an existing matrix.

1 Go to M8070B Module View > **Data Out > Parameters > Deemphasis > PCIe LTSSM Presets**.



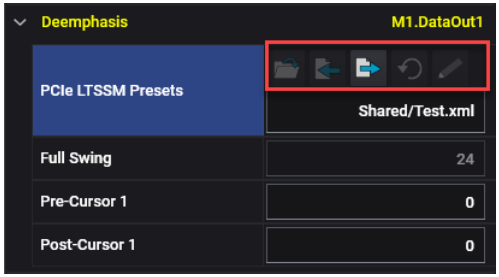
In the case of PCIe6, the Pre-Cursor 2 text box is available to set the current pre-cursor 2 value.



2 Click the **Edit TxEQ Matrix** icon.

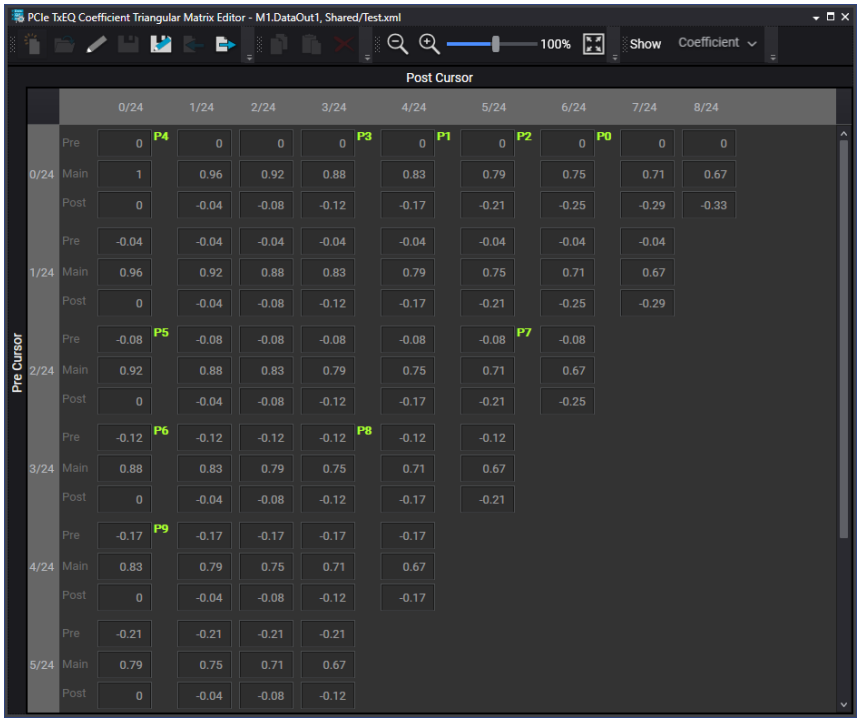
NOTE

When the **Edit TxEQ Matrix** icon is clicked, the **Open**, **Import**, **Reset**, and **Edit TxEQ Matrix** options are disabled under the **PCIe LTSSM Presets** parameter.



When the Matrix Editor window is closed, these options are enabled again.

The TxEQ Matrix Editor appears for the selected file. The **New**, **Open**, **Save**, **Save as**, **Import**, **Copy**, **Paste**, and **Delete** options are disabled.



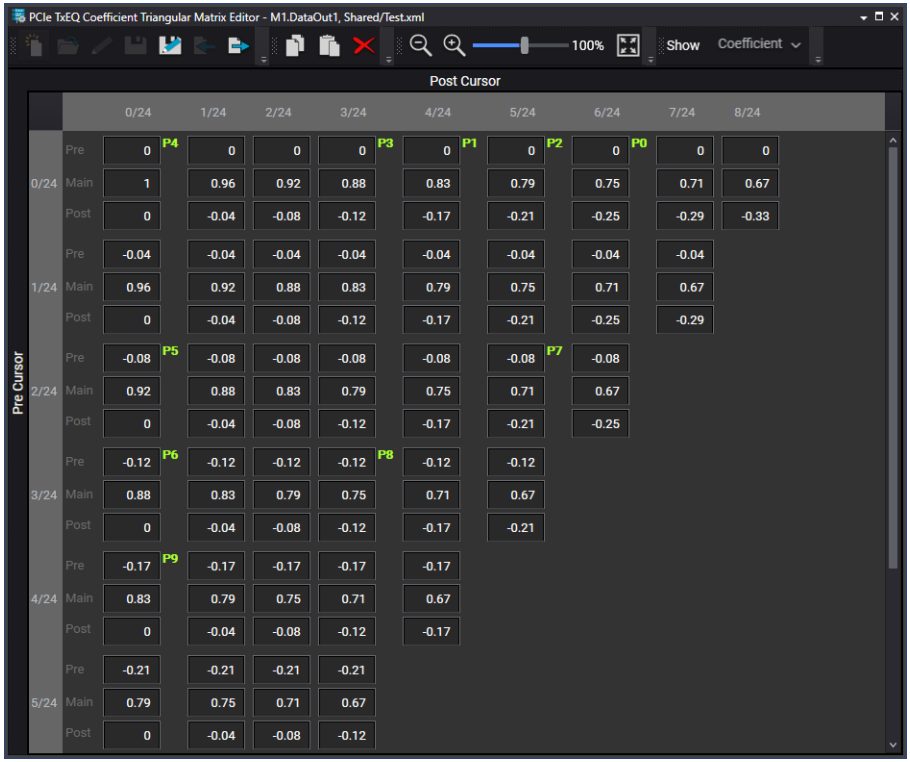
NOTE

You can select another channel through the M8070B main window, even when the TxEQ Matrix Editor is already opened for a particular channel. When selected, all the buttons are enabled for this channel.

When you click the **Edit TxEQ Matrix Editor** icon for the new channel, the TxEQ Matrix Editor displays the selected file, and the PCIe TxEQ Matrix Editor title bar displays the name of the selected file.

3 On the PCIe TxEQ Matrix Editor, click **Edit** icon.

The PCIe Matrix Editor enables you to edit the cell values.

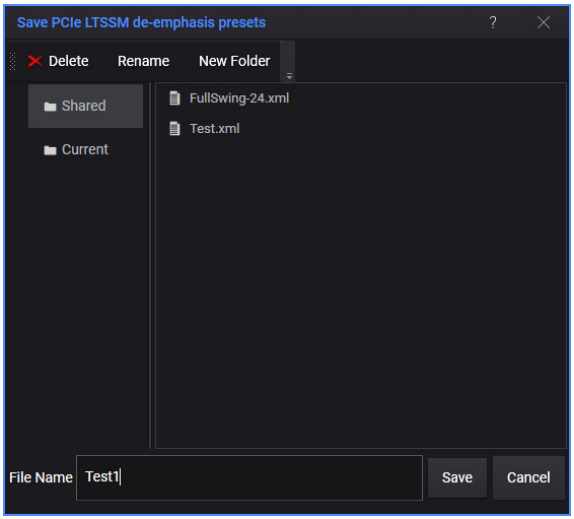


The Save, Save as, Copy, Paste, and Delete icons are enabled in Edit mode. The Save option is enabled when you modify any of the cell value.

4 After all the modifications are done, do one of the following:
   - Click **Save** icon to save the file.
   - Click **Save as** icon to save the copy of the file to a new location.

NOTE The Factory files cannot be saved using the **Save** option. Use **Save as** option to save any changes at different location.

When the **Save as** option is clicked, the **Save LTSSM deemphasis presets** dialog box appears.



5 (Optional) On the **Save PCIe LTSSM deemphasis presets** dialog box, do the following:

a Select a folder where you want to save the file.

By default, two folders; Shared and Current are available. Click **New Folder** to create a new folder.

b Type an appropriate name for the file.

c Click **Save**.

The file is saved at the location.

Importing a matrix file

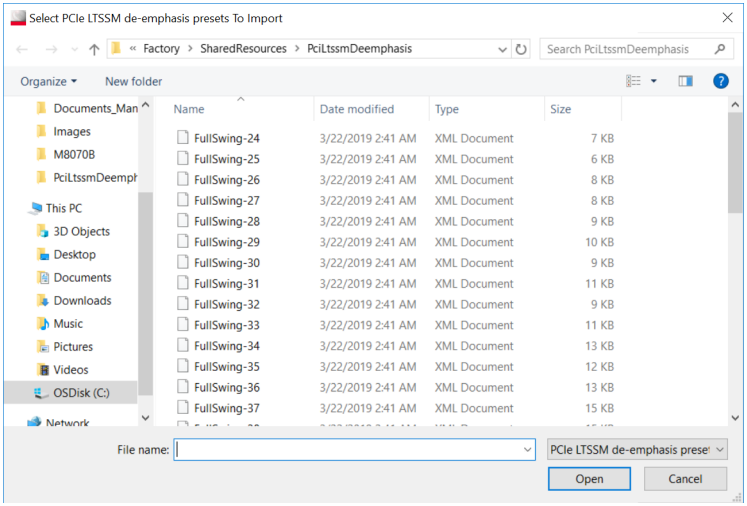
To import an existing matrix file from any location to M8070B workspace, perform the following steps:

1 Launch the TxEQ Matrix Editor through M8070B Menu Bar.

For more information, refer to Launching the TxEQ Matrix Editor through M8070B Menu Bar .

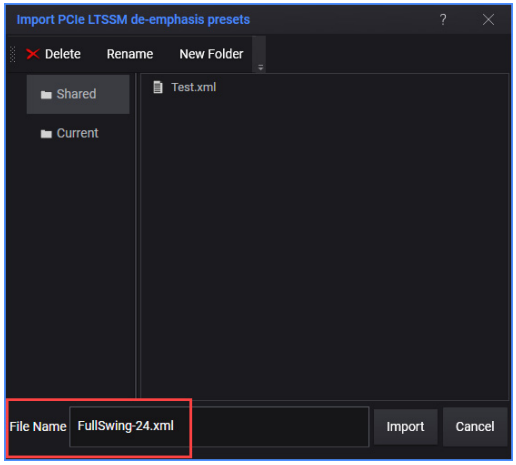
2 Click **Import** icon.

The **Select PCIe LTSSM deemphasis presets To Import** dialog box appears.



3 Browse the required matrix file, and then click **Open**.

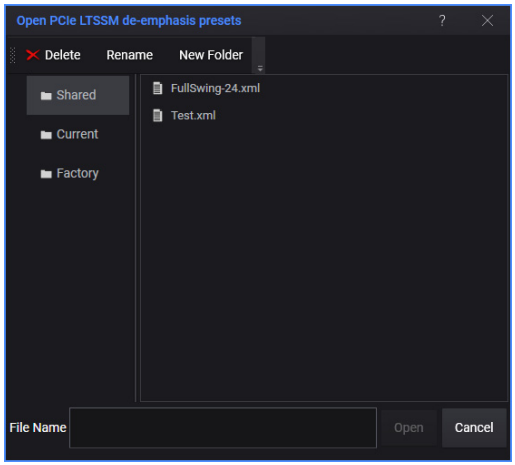
4 In the **Save PCIe LTSSM deemphasis presets** dialog box, type an appropriate name in the **File Name** text box.



5 Click **Import**.

The selected file is imported successfully. The PCIe TxEQ Matrix Editor title bar displays the name of the selected file.

6 (Optional) Click **Open** icon to check the imported file.



The imported file is opened in Matrix Editor.

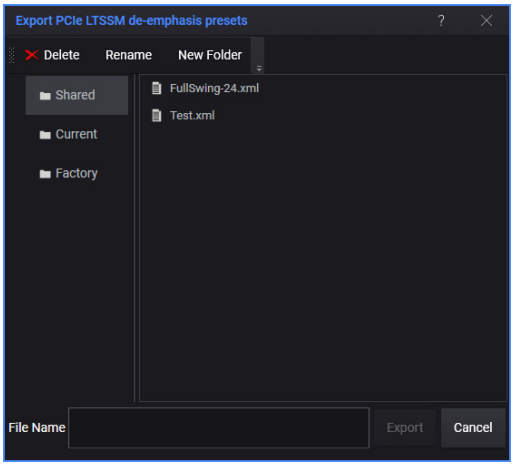
Exporting a matrix file

To export the current matrix to a file to any location, perform the following steps:

1 Launch the TxEQ Matrix Editor. For more information, refer to Launching the TxEQ Matrix Editor .

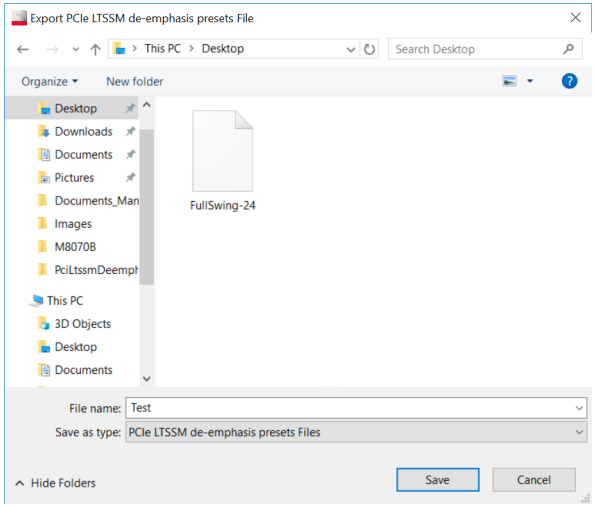
2 Click **Export** icon.

The **Open PCIe LTSSM deemphasis presets** dialog box appears.



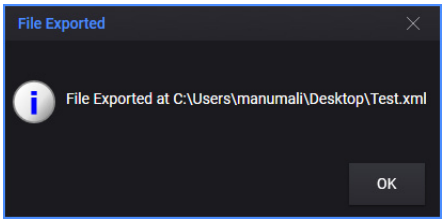
3 Select a file, and then click **Open**.

The **Export PCIe deemphasis presets File** dialog box appears.



4 Type the name of the file in the **File name** text box, and then click **Save**.

The File Exported at [Location name] message appears.



5 Click **OK**.

Adjustable Intersymbol Interference

The M8070B system software provides integrated and adjustable Intersymbol Interference (ISI) capability to test next-generation high-speed digital designs.

The adjustable and programmable ISI function allows emulating channel loss for characterizing and compliance testing of high-speed digital receivers. This function is integrated in each pattern generator channel of the M8020A which streamlines test setup by eliminating the need for external cabling and switching of external ISI traces.

As data rates continuously increase, channel loss between transmitter and receiver becomes more important. Channel loss is caused by printed circuit board traces, connectors, and cables in the signal path; resulting in ISI which depends on the channel material and dimensions, the data rate, and bit pattern. All high-speed digital receivers are specified to tolerate a certain amount of total jitter, which typically includes some ISI caused by channel loss. During receiver characterization and compliance test, this loss needs to be emulated.

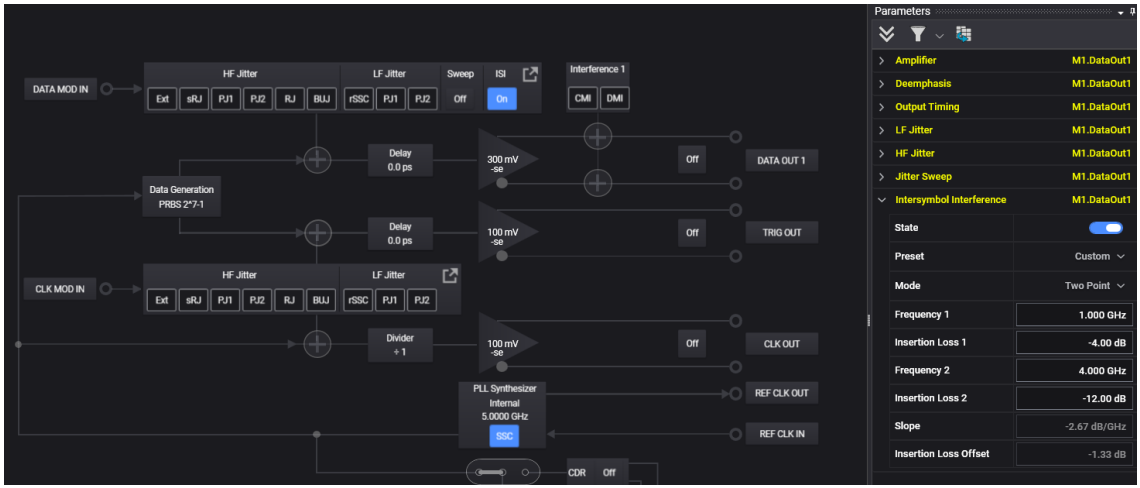
The built-in ISI functionality is programmable for each pattern generator channel. It simplifies receiver test automation for data rates up to 16 Gb/s.

The new adjustable ISI option offers the following advantages:

- Streamlines receiver test setup by providing the highest level of integration.
- Provides accurate and repeatable results for receiver characterization and compliance test by supporting a wide range of loss up to 25 dB and 16 GHz with linear loss curves and fine step resolution.
- Fits into the fully scalable and upgradeable receiver test solution with an upgrade option.

Using System View for ISI Configuration

You can use the **System View** to configure the ISI parameters for a selected '**Data Out**' location. When you select ISI in the **Jitter** block of the **System View**, the corresponding parameters are loaded on the **Parameters** window. You can create your own preset or manipulate frequency and insertion loss for the selected preset.



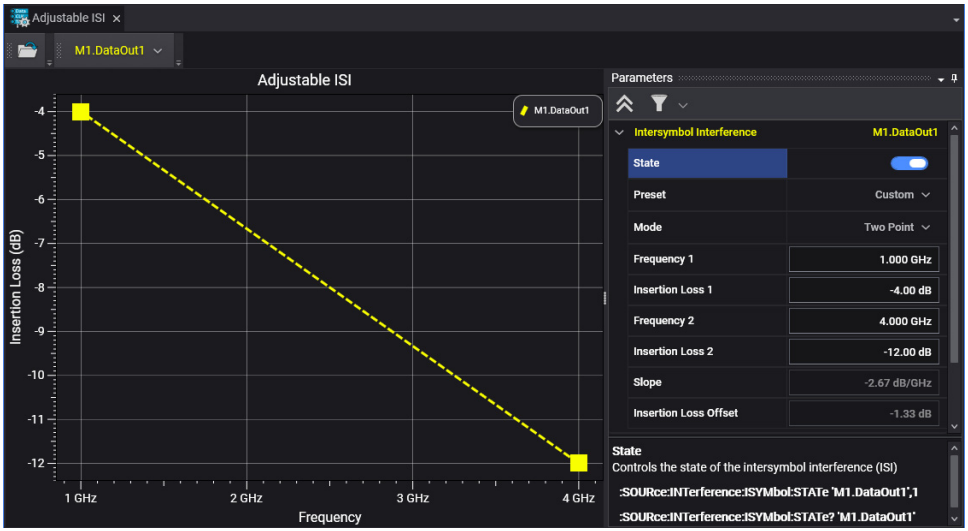
However, the **System View** does not provide flexibility to graphically manipulate the ISI parameters. This can be achieved using the **Adjustable ISI** window.

How to Launch Adjustable ISI Window:

To launch the **Adjustable ISI** window

- Go to the **Menu Bar** > **Generator** and then select **Adjustable ISI**.

The **Adjustable ISI** window will appear as shown in the following figure:



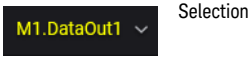
It includes the following elements:

- Toolbar
- Adjustable ISI Graph
- ISI Parameters

Toolbar

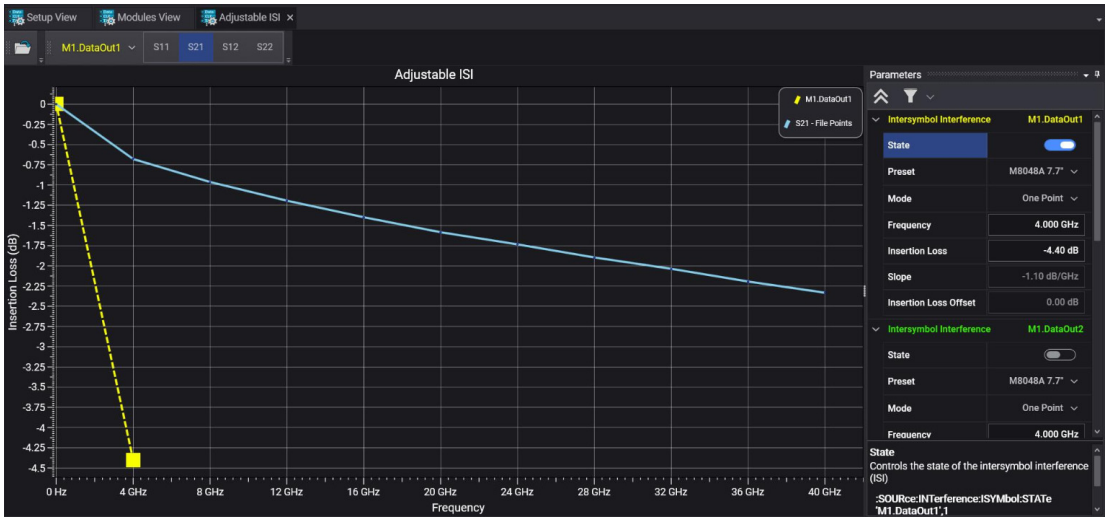
The toolbar provides the following convenient adjustable ISI functions:

Table 55

Elements	Name	Description
	Open SnP File	Click this button to open an s-parameters file (S2P). Currently, the M8070B GUI supports two port (S2P) and four port (S4P) s-parameters files. The s-parameters (also known as scattered parameters) are displayed when the scattered pattern file is loaded. S-parameters are complex matrix that show insertion loss at certain frequency. The two-port device displays four data points while the four-port device displays sixteen data points.
	Channel Selection	Use this drop-down list for channel section for which the graph is plotted for the corresponding values.

Adjustable ISI Graph

The following figure illustrates an ISI graph for 4-port system:



The ISI graph shows the insertion loss for a 2-port or 4-port system. The values on the graph represents insertion loss with respect to frequency. You can select the data points according to which you want to generate the loss and then manipulate points graphically (mouse drag) or by parameter window to draw the data point graph. Please note that if you manipulate the points of the linear graph to the values which are not in the defined limits of Slope and Offset, the pointer will change to ⊘ icon. In this case, the linear graph will switch to last set values. However, if you manipulate the points of the linear graph to the values which are not in the defined limits of Slope and Offset, the pointer will change to ! icon. In this case, a message will appear at the bottom of the graph along with the undo option to revert the graph changes.

ISI Parameters

The ISI parameters are summarized in the following list:

- **State** - Enables/disables the ISI state.
- **Preset** - Allows you to select preset for specific applications representing a typical loss characteristic.
- **Mode** - Controls the ISI as one point or two points. For each point you can specify frequency and insertion loss at that frequency. The calculated values are displayed in the **Parameters** window.
  - **One Point**: In this mode, one point of the linear graph is fixed while the another point can be moved graphically to manipulate insertion loss/frequency values.
  - **Two Points**: In this mode, both points of the linear graph can be moved graphically to manipulate insertion loss/frequency values.
- **Slope** - Shows the calculated slope value (Insertion Loss/frequency, dB/GHz).
- **Insertion Loss Offset** - Shows the Insertion Loss Offset (at frequency= 0 Hz).

Intersymbol Interference (ISI) Setup

The following steps describe the procedure for ISI setup:

1. Connect the DUT in loopback mode. For connection details, refer to *M8020A Getting Started Guide*.
2. From the M8070B software, launch **Adjustable ISI** window.
3. Select **M1.DataOut1** channel from drop-down list.
4. From the **Parameters** window, select the **Preset** from the provided list. It will show the linear graph.

5 Select the mode as '**Two Points**'.
6 Manipulate insertion loss/frequency values either graphically or by **Parameters** window.
7 Alternatively, you can also open a S2P or S4P file and graphically manipulate loss and frequency parameters according to data points.
8 Click the toggle button to enable the ISI state.

De-Embedding

The M8042A and M8045A generator modules provides de-embedding capabilities to compensate for losses in the loop-back path. In high-speed digital communications testing, the signal at the device under test (DUT) is not the same as the signal leaving the BERT's output, because cables, connectors, fixtures, and probes all introduce frequency-dependent losses and distortions. De-Embedding in the M8042A and M8045A is a digital signal processing feature that allows the BERT to remove the effects of test fixtures and interconnects, ensuring the DUT sees the correct signal conditions for compliance and margin testing.

To perform the De-Embedding:

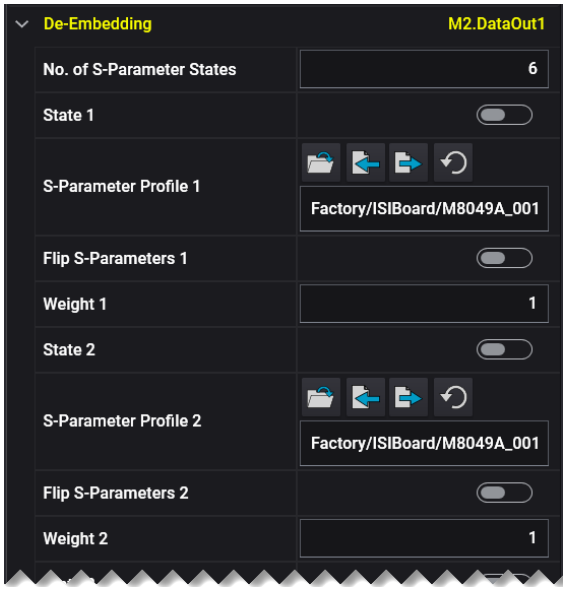
1 Go to the **Menu Bar** > **Generator** and then select **Data Out**.

2 In the **Parameters** window, select **De-Embedding** function block.

3 Specify **De-Embedding** configuration using the provided parameters.

The **De-Embedding** parameters are identical for both the M8042A and M8045A generator modules. The only difference is that the M8042A allows you to create and configure up to six S-Parameter profiles, whereas the M8045A supports only two S-Parameter profiles.

The following image shows the **De-Embedding** parameter for the M8042A generator module.



The **De-Embedding** parameters for M8042A and M8045A generator modules are summarized in the following list:

- **No of S-Parameter States** - Allows you to create and configure up to six S-Parameter profiles. This option is only available for the M8042A pattern generator module.
- **State 1|2|3|4|5|6** - Enables/disables the S-Parameter profiles. The M8042A supports up to six S-Parameter profiles while M8045A supports only two S-Parameter profiles.
- **S-Parameter Profile 1|2|3|4|5|6** - Allows you to select the S-Parameter file (S2P, S4P) to de-embedding effect of the cable. The S-Parameter files (standard cables, ISI Boards and couplers) are available in the “Factory” folder. You can also import or export the user-defined S-Parameter file.
- **Flip S-Parameters 1|2|3|4|5|6** - Allows you to flip the S-Parameter ports for embedding instead of de-embedding a cable.
- **Weight 1|2|3|4|5|6** - Sets the weight for the selected de-embedding S-Parameter profile.
- **Operator Output 1|2|3|4|5|6** - Selects operator output for S-Parameter profile for selected de-embedding profile. Note that this parameter will only be available when an S4P file is loaded in the “S-Parameter Profile”.
- **Port 1|2|3|4|5|6** - Selects the port for the S-Parameter profile when using an external ISI board. Note that this parameter will only be available when an S4P file is loaded in the “S-Parameter Profile”.

Line Coding

You can define the line coding for a **Data Out** port of the M8042A, M8045A, M8194A, M8195A, and M8196A modules through the **Parameters** window.

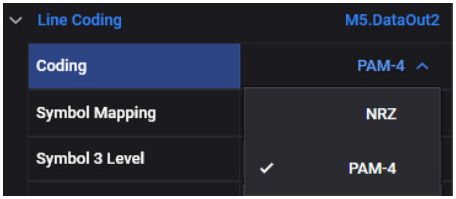
To set the line coding:

1 Go to the **Menu Bar** > **Generator** and then select **Data Out**.

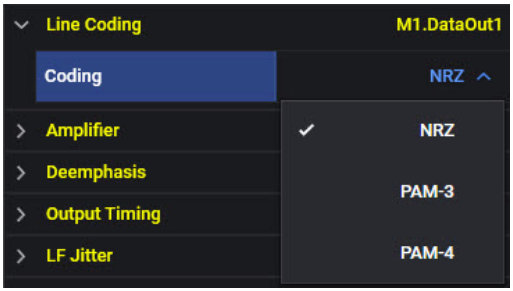
2 Select **Line Coding** functional block from the **Parameters** pane.

3 Select the line coding.

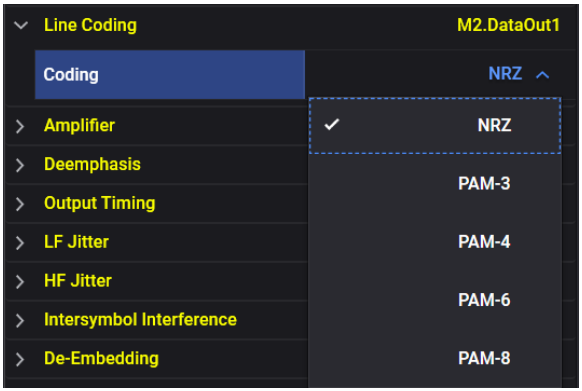
For M8194A, M8195A, and M8196A modules, the **Data Out** port supports **NRZ** and **PAM4** line coding which defines how consecutive data bits are mapped to symbols.



For M8045A module, the **Data Out** port supports **NRZ, PAM3,** and **PAM4** line coding.

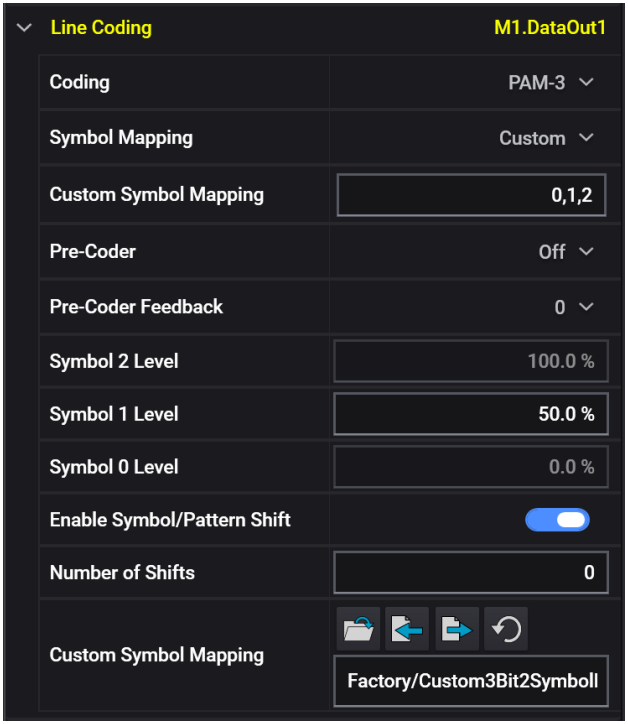


For M8042A module, the **Data Out** port supports **NRZ, PAM3**, **PAM4**, **PAM6** and **PAM8** line coding.



PAM3 Line Coding

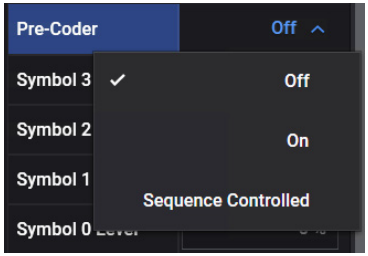
The **PAM3** line coding provides the following symbol mapping options as shown in the following figure:



- **Symbol Mapping** – The following options are available:
  - **Uncoded** – In this mapping, the low voltage maps to symbol 0, the middle voltage maps to symbol 1, and upper voltage maps to symbol 3.
  - **Custom** – In this mapping the voltage levels are mapped to symbols. The mapping is defined as a comma separated list of symbols (e.g. 0, 1, 2). The position within this list corresponds to the voltage level. The first value is for lower voltage, second value is for middle voltage, and last value is for upper voltage.

    This parameter accepts the symbol level values in decimal format (for example, 50.1, 60.2).

- **Pre-Coder** - The Pre-Coder option enables/disables the PAM3 pre-coder or can be sequence controlled.



- **Pre-Coder Feedback** - The pre-coder feedback option allows you to select the initial feedback value (0, 1, or 2), which determines how the output of the precoded signal is generated.
- **Symbol Level** - The PAM3 line coding provides the Symbol Level options which controls the PAM3 level mappings. It can be used to adjust the actual output level that is being generated by a data output for a specific PAM3 symbol. The levels of PAM3 symbol 0 and 2 cannot be adjusted and are always kept at the value of 0% and 100% of the actual output voltage swing.
- **Enable Symbol/Pattern Shift** - Click this button to enable or disable the pattern shift and symbol mapper functionality in the hardware.
- **Number of Shifts** - Use this option to specify the number of symbols by which the pattern needs to be rotated. This option becomes available when Enable Symbol/Pattern Shift is turned on.
- **Custom Symbol Mapping** - Use this option to select the mapping file to be used for symbol mapping in the hardware. This option becomes available when "**Enable Symbol/Pattern Shift**" is turned on.

PRTS Support by PAM3

The M8042A and M8045A modules support the generation of the following PRTS values when the line coding is set to PAM3.

- 3^17-1
- 3^19-1
- 3^23-1

These PRTS values are algorithmically generated, like other PRBS patterns. Therefore, it is advancing while in a sequence block that is configured to generate the PRTS, and stops while the sequencer is generating other non-PRTS blocks.

These sequences will simply continue when re-entering another sequence block that is configured for the respective PRTS (3^17, 3^19, 3^23).

The given seed value is applied when the sequence is starting for the first time, but not when advancing or jumping from one sequence block to another one.

It is possible to specify the seed value of the PRTS generator. The format is the same as for a PRBS in NRZ mode. Therefore, the seed value is a hexadecimal number that is built by 2 bits for each PAM3 symbol.

The symbol mapping is:

Symbol	Bit Sequence
0	00
1	10
2	01

The seed value, bit sequence, and the hexadecimal values for the different PRTS values are given below:

- 3^17

  The default seed value for PRTS-17 is the PAM3 symbol sequence 10000000000000000 ('16 zeros + 1 one')

  Using the symbol mapping above this results in the bit sequence 0010 0000 0000 0000 0000 0000 0000 0000 0000

  The above bit sequence gives the hexadecimal value 200000000

- 3^19

  The default seed value for PRTS-19 is the PAM3 symbol sequence 111111111111111111 ('all ones')

  Using the symbol mapping above this results in the bit sequence

  10 1010 1010 1010 1010 1010 1010 1010 1010 1010

  The above bit sequence gives the hexadecimal value 2AAAAAAAAA

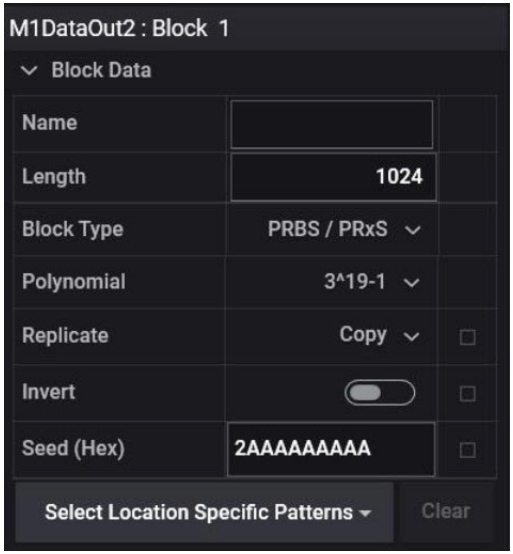
- 3^23

  The default seed value for PRTS-23 is the PAM3 symbol sequence 1000000000000000000000 ('22 zeros + 1 one')

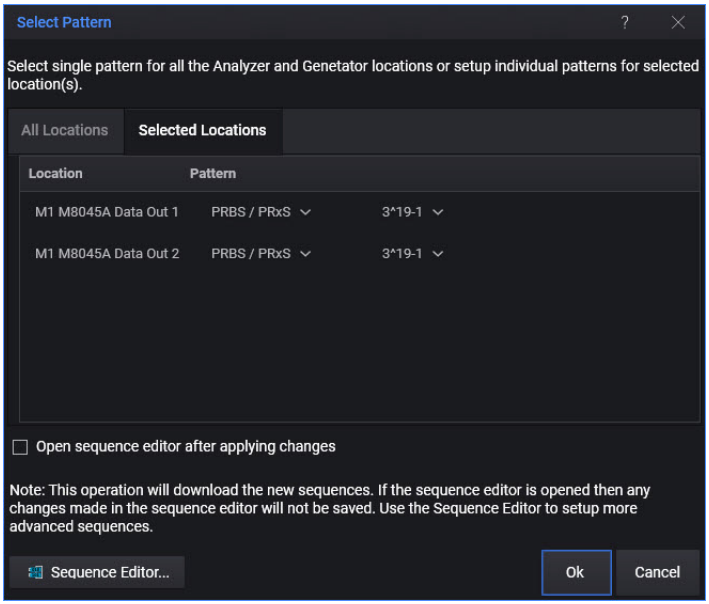
  Using the symbol mapping above this results in the bit sequence 10 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000

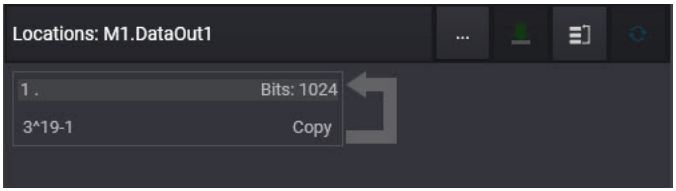
  The above bit sequence gives the hexadecimal value 200000000000

The following figure displays the 3^19-1 PRTS selected on sequence block. The 3^17-1 and 3^23-1 PRTS values can also be selected in the similar way.



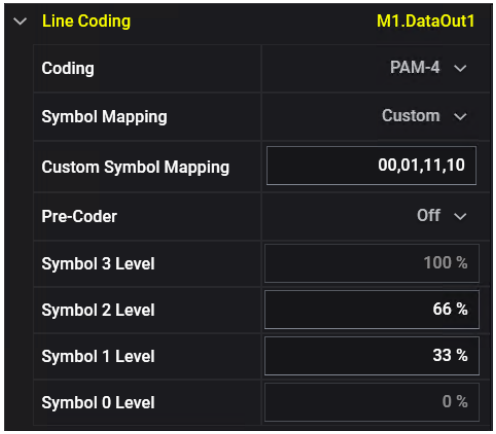
The following figure displays the 3^19-1 PRTS selected on Generator. The 3^17-1 and 3^23-1 PRTS values can also be selected in the similar way.





PAM4 Line Coding

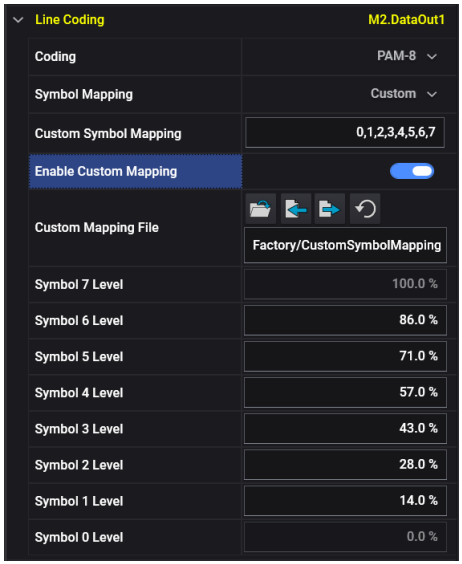
The **PAM4** line coding provides the following symbol mapping options as shown in the following figure:



- **Symbol Mapping** - The following options are available.
  - **Uncoded** - In this mapping, the bit sequence 00 maps to symbol 0, 10 maps to symbol 2 and 11 maps to symbol 3.
  - **Gray Coded** - In this mapping, the bit sequence 00 maps to symbol 0, 00 maps to symbol 0, 01 maps to symbol 1, 11 maps to symbol 2 and 10 maps to symbol 3.
  - **Custom** - In this mapping the consecutive data bits are mapped to symbols. The mapping is defined as a comma separated list of bit sequences (e.g. 00, 01, 11, 10). The position within this list corresponds to the symbol level. First value is for Symbol 0 an the last value is for Symbol 3.
- **Pre-Coder** - The Pre-Coder option enables/disables the PAM4 pre-coder or can be sequence controlled.
- **Symbol Level**: It controls the PAM4 level mappings. It can be used to adjust the actual output level that is being generated by a data output for a specific PAM4 symbol. The levels of PAM4 symbol 0 and 3 cannot be adjusted and are always kept at the value of 0% and 100% of the actual output voltage swing.

PAM6/PAM8 Line Coding

The **PAM6** and **PAM8** line coding provides the symbol mapping options as shown in the following figure:



- **Coding -** Select the line coding as PAM6 or PAM8. Please note that a memory pattern must be selected before switching as the algorithmic PRBS memory blocks are not supported for PAM6/8.
- **Symbol Mapping** - The following options are available.
  - **Uncoded** - In this mapping, the bit sequence 00 maps to symbol 0, 10 maps to symbol 2 and 11 maps to symbol 3.
  - **Custom** - In this mapping, the consecutive data bits are mapped to symbols. The mapping is defined as a comma-separated list of bit sequences (e.g., 0,1,2,3,4,5,6,7). The position within this list corresponds to the symbol level. The first value is for Symbol 0 and the last value is for Symbol 7.
- **Enable Custom Symbol Mapping** - Click this toggle button to enable the custom symbol mapping. Once this option is selected, the **Custom Mapping File** option appears. Using this option, to use the custom mapping file. Currently, this option is only supported by PAM6/PAM8 line coding. For details, refer to Understanding PAM6/PAM8 Custom Symbol Mapping on page 490.

- **Symbol Level** – It controls the PAM6 or PAM8 level mappings. It can be used to adjust the actual output level that is being generated by a data output for a specific PAM6 or PAM8 symbol. For PAM6, Symbol Level 0 to 5 are available and for PAM8 Symbol Level 0 to 7 are available. The levels of PAM6 symbol 0 and 5 cannot be adjusted and are always kept at the value of 0% and 100% of the actual output voltage swing. The levels of PAM8 symbol 0 and 7 cannot be adjusted and are always kept at the value of 0% and 100% of the actual output voltage swing.

NOTE

Make sure to use the similar line coding for all Data Out ports of M8042A/M8045A/M8194A/M8195A/M8196A. An "Auto Correction" window will appear if you select different line coding for Data Out ports. Clicking on the "Apply" button, present on this window applies same line coding on all Data Out ports.

Understanding PAM6/PAM8 Custom Symbol Mapping

The Custom Symbol Mapping functionality converts the bit sequences into symbol sequences while it is downloaded into the hardware. This feature is enabled by toggling the “Enable Custom Symbol Mapping” button. Once this option is enabled, you can select the custom mapping file. Currently, only 3 bit to 1 symbol (3b1s) or 5 bit to 2 symbol (5b2s) mappings are supported by PAM6 and PAM8 line coding.

3 Bit to 1 Symbol mapping for PAM6:

For 3 bit mapping there will 6 unique 3 bit sequences corresponding 6 symbols. The custom mapping XML file for 3b1s mapping contains 'SymbolMapping' blocks corresponding to each symbol. The attribute ‘symbols’ is used to specify the symbols and the attribute ‘bits’ is used to specify the corresponding 3 bit sequence. Since the maximum possible 3 bit combination is 6 mapping for only 6 symbols can be defined. This is doing something like regular symbol mapping with the difference that it takes effect during pattern download while the regular symbol mapping has an immediate effect (not requires pattern download).

The format of XML file for 3b1s mapping will be as follows:

```
▼<PamCustomSymbolMappings xmlns:xsd="http://www.w3.org/2001/XMLSchema" xmlns:xsi="http://www.w3.org/2001/XMLSchema-instance">
   <Version>1.0</Version>
   <Description>Custom Symbol Mapping for PAM line coding</Description>
   <NoOfLevels>6</NoOfLevels>
   <NoOfBits>3</NoOfBits>
   <NoOfSymbols>1</NoOfSymbols>
  ▼<SymbolMappings>
     <SymbolMapping symbols="0" bits="000"/>
     <SymbolMapping symbols="1" bits="001"/>
     <SymbolMapping symbols="2" bits="010"/>
     <SymbolMapping symbols="3" bits="011"/>
     <SymbolMapping symbols="4" bits="100"/>
     <SymbolMapping symbols="5" bits="101"/>
   </SymbolMappings>
 </PamCustomSymbolMappings>
```

3 Bit to 1 Symbol mapping for PAM8:

```
▼<PamCustomSymbolMappings xmlns:xsd="http://www.w3.org/2001/XMLSchema" xmlns:xsi="http://www.w3.org/2001/XMLSchema-instance">
   <Version>1.0</Version>
   <Description>Custom Symbol Mapping for PAM line coding</Description>
   <NoOfLevels>8</NoOfLevels>
   <NoOfBits>3</NoOfBits>
   <NoOfSymbols>1</NoOfSymbols>
  ▼<SymbolMappings>
     <SymbolMapping symbols="0" bits="000"/>
     <SymbolMapping symbols="1" bits="001"/>
     <SymbolMapping symbols="2" bits="010"/>
     <SymbolMapping symbols="3" bits="011"/>
     <SymbolMapping symbols="4" bits="100"/>
     <SymbolMapping symbols="5" bits="101"/>
     <SymbolMapping symbols="6" bits="110"/>
     <SymbolMapping symbols="7" bits="111"/>
   </SymbolMappings>
 </PamCustomSymbolMappings>
```

5 Bit to 2 Symbol mapping for PAM6:

For 5 bit mapping there will 32 unique 5 bit sequences corresponding 32 symbol pairs. The custom mapping XML file for 5b2s mapping contains 'SymbolMapping' blocks corresponding to each pair. The attribute ‘symbols’ is used to specify the symbol pair and the attribute ‘bits’ is used to specify the corresponding 5 bit sequence. Since the maximum possible 5 bit combination is 32 mapping for only 32 symbol pairs can be defined.

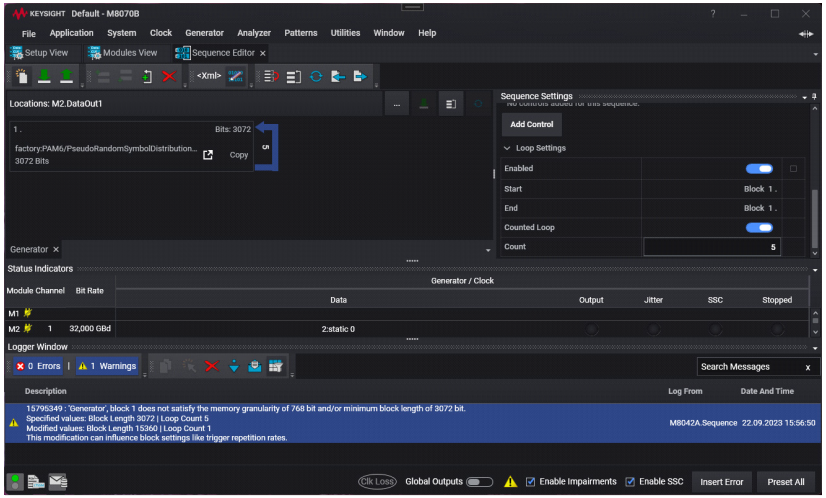
The format of XML file for 5b2s mapping will be as follows:


```xml
<PamCustomSymbolMappings xmlns:xsd="http://www.w3.org/2001/XMLSchema" xmlns:xsi="http://www.w3.org/2001/XMLSchema-instance">
  <Version>1.0</Version>
  <Description>Custom Symbol Mapping for PAM line coding</Description>
  <NoOfLevels>6</NoOfLevels>
  <NoOfBits>5</NoOfBits>
  <NoOfSymbols>2</NoOfSymbols>
  <SymbolMappings>
    <SymbolMapping symbols="01" bits="00000"/>
    <SymbolMapping symbols="02" bits="00001"/>
    <SymbolMapping symbols="03" bits="00011"/>
    <SymbolMapping symbols="04" bits="00010"/>
    <SymbolMapping symbols="10" bits="00100"/>
    <SymbolMapping symbols="11" bits="00101"/>
    <SymbolMapping symbols="12" bits="01000"/>
    <SymbolMapping symbols="13" bits="01001"/>
    <SymbolMapping symbols="14" bits="01011"/>
    <SymbolMapping symbols="15" bits="01010"/>
    <SymbolMapping symbols="20" bits="01100"/>
    <SymbolMapping symbols="21" bits="01101"/>
    <SymbolMapping symbols="22" bits="10000"/>
    <SymbolMapping symbols="23" bits="10001"/>
    <SymbolMapping symbols="24" bits="10011"/>
    <SymbolMapping symbols="25" bits="10010"/>
    <SymbolMapping symbols="30" bits="10100"/>
    <SymbolMapping symbols="31" bits="10110"/>
    <SymbolMapping symbols="32" bits="11000"/>
    <SymbolMapping symbols="33" bits="11001"/>
    <SymbolMapping symbols="34" bits="11011"/>
    <SymbolMapping symbols="35" bits="11010"/>
    <SymbolMapping symbols="40" bits="11100"/>
    <SymbolMapping symbols="41" bits="11101"/>
    <SymbolMapping symbols="42" bits="00110"/>
    <SymbolMapping symbols="43" bits="00111"/>
    <SymbolMapping symbols="44" bits="01110"/>
    <SymbolMapping symbols="45" bits="01111"/>
    <SymbolMapping symbols="51" bits="10101"/>
    <SymbolMapping symbols="52" bits="10111"/>
    <SymbolMapping symbols="53" bits="11110"/>
    <SymbolMapping symbols="54" bits="11111"/>
  </SymbolMappings>
</PamCustomSymbolMappings>
```


The custom mapping file can be modified by editing it and then importing it as desired, but for every possible bit sequence, a corresponding unique symbol sequence must be defined.

When the Custom Symbol Mapping feature is enabled, the M8070B system software remaps the memory patterns during download.

Because the bit-sequence must meet the hardware requirements after the mapping procedure, the pattern length must be a multiple of 640 bit (in the case of 5b2s, 256 symbols per vector * 5 bit/2 symbols = 640 bit). This is due to the mapping procedure increasing the length of the pattern. If the pattern is infinite, it is unrolled to fit the requirements.



A memory pattern with a counted loop that does not fulfill the granularity requirements may get converted into a longer pattern with a lower loop count, without possibly changing the effective length of the pattern. In this case, a warning message is displayed.

The Custom Symbol Mapping and Symbol Mapping are independently applied onto the generated signal. The Custom Symbol Mapping is applied (first) during pattern download via the M8070B software where the pattern memory content is modified. The Symbol Mapping is applied (second) in real time from the FPGA the pattern memory content is not affected.

The following example illustrates how the symbol mapping inverts the symbol pattern:

1 Binary user input "payload" data
2 Natively mapped symbols
3 Custom Symbol Mapping file remaps the pattern in the hardware as specified in the XML file
4 Symbol Mapping inverts the symbol pattern
   - (000b) 0 -> 0 -> 5
   - (001b) 1 -> 1 -> 4
   - (010b) 2 -> 2 -> 3
   - (011b) 3 -> 5 -> 0
   - (100b) 4 -> 3 -> 2
   - (101b) 5 -> 4 -> 1

5 Just for verification, both of these operations used the other way around yield a different result, therefore they are not commutative:
   - (000b) 0 -> 5 -> 4
   - (001b) 1 -> 4 -> 3
   - (010b) 2 -> 3 -> 5
   - (011b) 3 -> 2 -> 2
   - (100b) 4 -> 1 -> 1
   - (101b) 5 -> 0 -> 0

Segmented SSC Profile using M8009A Clock Module

Segmented SSC turns the M8009A Clock Module into an advanced system clock source, supporting complex SSC modulations with up to four arbitrary shapes that can be played in a sequence and/or in a loop. A new profile “Segmented Arbitrary” is added to enable it. In addition, a trigger capability is added to do test setup calibration for compliance testing. Triggering capability is included to capture the generated signal at precise instants relative to the SSC modulation. Application-specific presets for the USB4 and DP2.1 technologies are provided in order to address the Receiver Clock Switch compliance test requirement.

The M8009A clock module sends a trigger signal to the system module on the STRIG line. See the system module’s User Guide (*Keysight M9502A 2-Slot and M9505A 5-Slot AXIe Chassis User Guide*) for routing STRIG to the trigger output on the front panel.

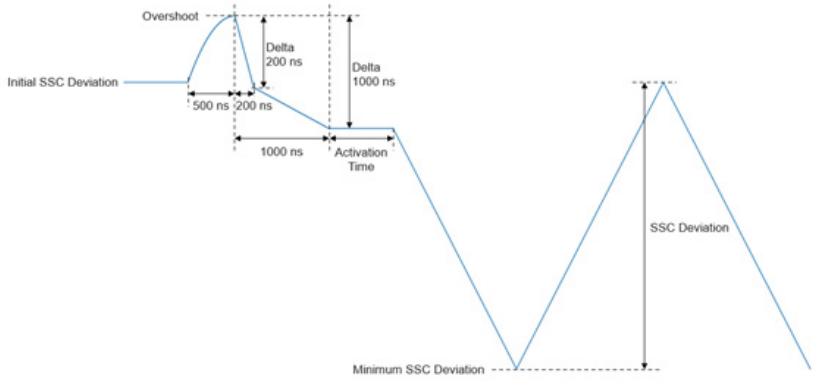
The following image displays the Trigger Out port on the front panel of the System Module.

Trigger Out

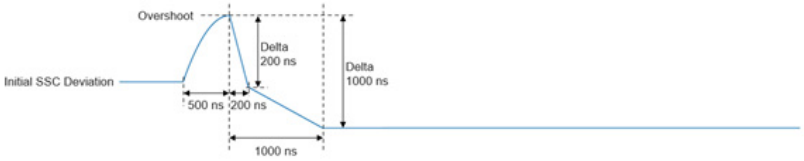
In the standard or user-defined shapes, the trigger output is high during the clock switch segment. For custom shapes, the trigger output is high for segments that have the trigger property set.

The following figures show the Frequency variation with respect to Time for Segmented SSC with and without Triangular Modulation:

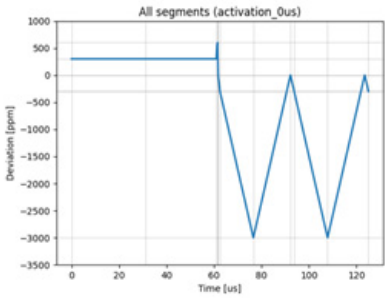
1 With Triangular Modulation

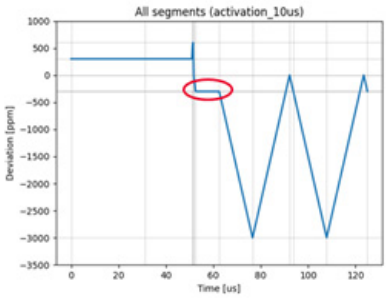


2 Without Triangular Modulation



The following figure shows the effect of applying activation time on a segment:





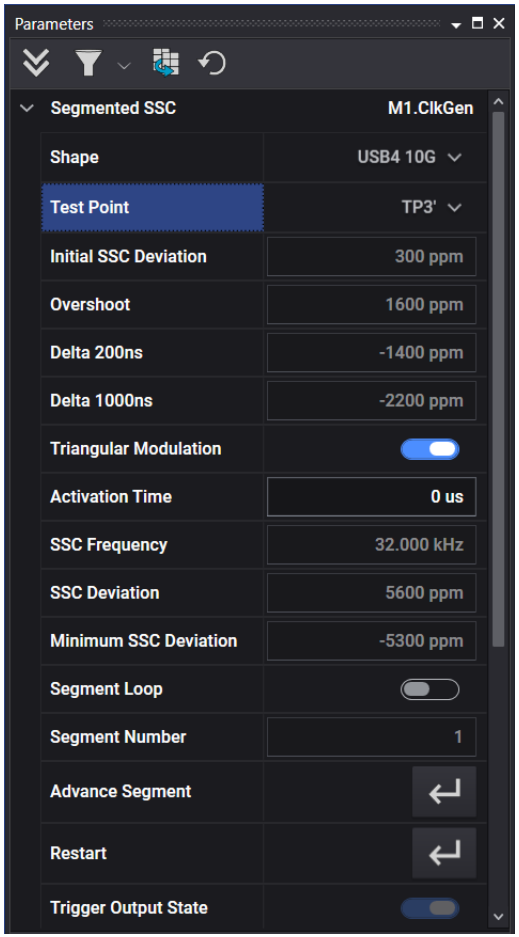
Segmented SSC Configuration

This section describes the steps to configure **Segmented SSC** in the M8009A clock module.

1. To enable the **Segmented SSC** configuration, you need to select **ClkGen** and then go to **SSC** functional block in the **Properties** window.
2. Select the **SSC Profile** as “Segmented Arbitrary” from the drop-down list.
3. A new **Segmented SSC** functional block will appear in the **Properties** window.
4. Use the parameters provided in the **Segmented SSC** functional block to configure the segmented SSC. For details on **Segmented SSC** parameters, refer to Segmented SSC Parameters on page 498.

Segmented SSC Parameters

The **Segmented SSC** functional block provides the following parameters:



- **Shape**: This option provides the following functionalities:
  - select a preset in conjunction with the test point
  - select **User Defined** mode where the user can edit the parameters
  - select **Custom** mode where the user can load a deviation waveform
    - **Segment Count** – Specifies how many segments define the segmented SSC profile. Acceptable range is from 1 to 4.

- **SSC Deviation File** – Sets the deviation waveform file to be loaded into this segment. The file must contain one decimal number per line that specifies deviation in ppm. The maximum deviation range is ±10000 ppm. The deviation points defined by the file will be re-sampled to fill the 32768 samples long segment. Use numeric suffix 1 to 4 to select the segment for which the file name needs to be set.
- **Trigger on Segment** – Enables or disables trigger on segment. If enabled, the trigger output is high while this segment is being played back, else the trigger output is low during play back.
- **Play segment Once** – Enables or disables the 'Play Once' option for a segment for Custom shape. Use numeric suffix 1 to 4 to select the segment for which the option needs to be set. When this option is enabled, the segment is played only once and the segmented SSC automatically advances to the next one. If disabled, this segment will be played in a loop until clicking the "Advance Segment" button. Only then, the segmented SSC will advance to the next one.

- **Test Point** – Selects the test point at the receiver. Affects the overshoot for applicable shapes.
- **Initial SSC Deviation** – Sets the initial non-modulated deviation in ppm. This parameter can only be modified if the shape is selected as "User Defined" or "Custom".
- **Overshoot** – Sets the absolute peak deviation of the overshoot in ppm. This parameter can only be modified if the shape is selected as "User Defined" or "Custom".
- **Delta 200ns** – Sets the relative deviation over 200 ns in ppm after the overshoot. This corresponds to the first straight slope after the overshoot. Delta is measured from the overshoot peak. This parameter can only be modified if the shape is selected as "User Defined" or "Custom".
- **Delta 1000ns** – Sets the relative deviation over 1000 ns in ppm after the overshoot. This corresponds to the second straight slope after the overshoot. Delta is measured from the overshoot peak. This parameter can only be modified if the shape is selected as "User Defined" or "Custom".
- **Triangular Modulation** – Enables or disables the triangular SSC modulation after the clock switch.
- **Activation Time** – Sets the activation time before enabling the triangular modulation. The activation time range is 0 to 20 us. This allows delaying the SSC profile activation by specified amount of time.

- **SSC Frequency** – Sets the frequency of the triangular modulation. In custom shape mode, it specifies the inverse of the duration of each segment. This parameter can only be modified if the shape is selected as “User Defined” or “Custom”.
- **SSC Deviation** – Sets the peak-to-peak deviation of the triangular modulation in ppm. This parameter can only be modified if the shape is selected as “User Defined” or “Custom”.
- **Minimum SSC Deviation** – Sets the minimum deviation of the triangular modulation in ppm. This parameter can only be modified if the shape is selected as “User Defined” or “Custom”.
- **Segment Loop** – Enables or disables the segment loop.

  If enabled, all the three segments (initial deviation, clock switch, triangular modulation) will be played back continuously one after the other. The initial deviation and triangular modulation segments are repeated 10 times.

  If disabled, the initial segment will be played repeatedly. Clicking the “Advance Segment” button plays the clock segment once and then repeats the triangular modulation segment. Clicking the “Advance Segment” button a second time switches back to the initial deviation segment.
- **Segment Number** – Displays the segment that is currently being played by the segmented SSC.
- **Advance Segment** – Advances to the next segment in the sequence.
- **Restart** – Stops the segmented SSC sequence and restarts it at the first segment.
- **Trigger Output State** – Drives the trigger signal to the system module on the STRIG line. This parameter is ‘read-only’ and cannot be modified.

Configuring Trigger Output on System Module (ESM)

To configure the Trigger Out of the system module,

1 Navigate to http://169.254.1.0 to access the chassis’ web interface.

NOTE **To access the URL, the chassis must be online with the instrument module connected.**

2 Under the Trigger tab:

   i Select the output enable for SMA Trigger ‘Out’.

   ii Set its input signal to STRIG.

   Slot number must be the same as where the clock module resides.

   iii Click “Save Trigger Routing as Default State” as shown in Figure 29 to apply these settings and make them persistent across power cycles.

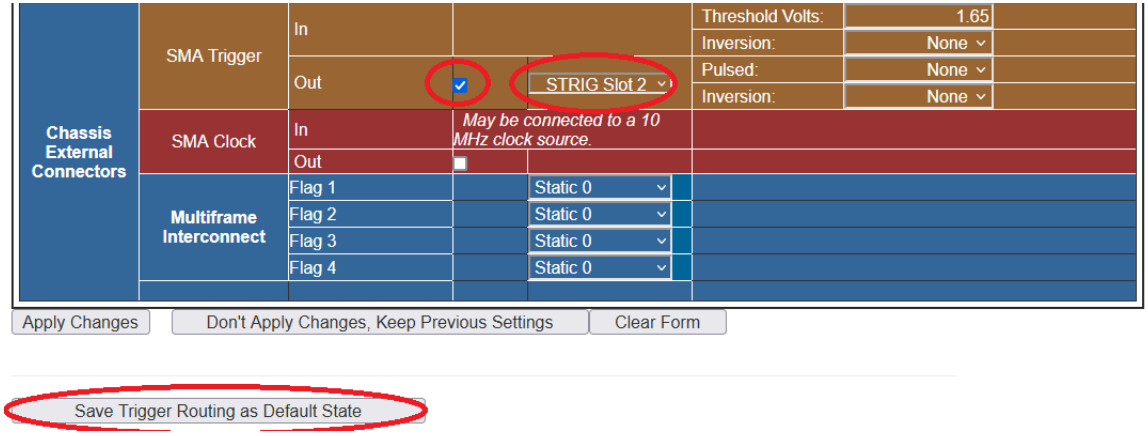


Figure 29 Configuring Trigger Out in the System Module

LFPS Generator

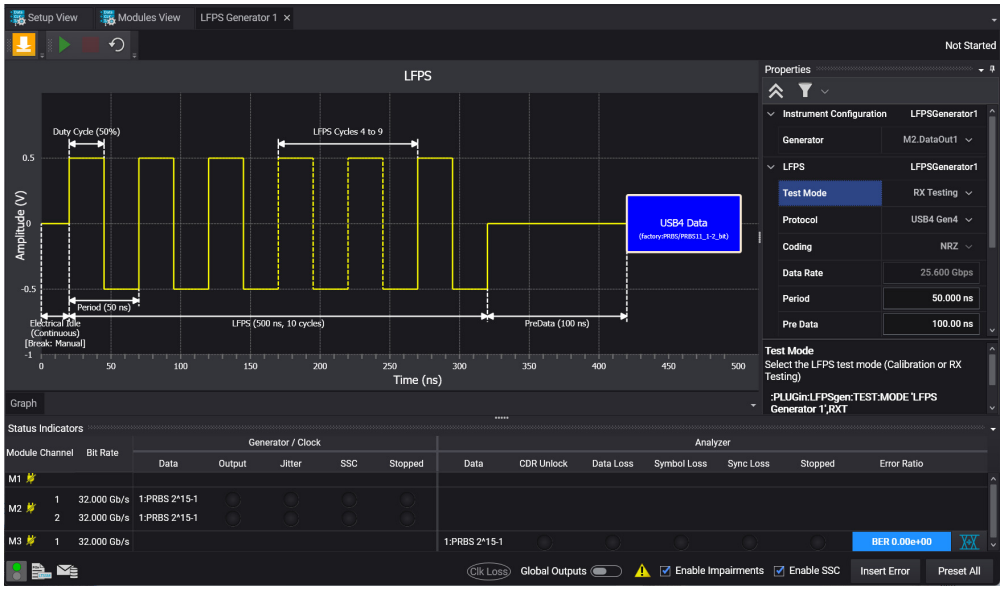
The LFPS Generator utility is used to generate LFPS patterns and sequences using the M8070B system software. It allows for the configuration of LFPS cycles, period, duty cycle, pre-data duration, and electrical idle duration. This utility is supported by the M8042A and M8045A pattern generator modules. The LFPS Generator supports USB4v2 Gen 2 (10 Gbps), Gen 3 (20 Gbps), and Gen 4 (25.6 Gbps) data rates. For USB4v2 Gen 2 and Gen 3, NRZ line coding is used, while for USB4v2 Gen 4, PAM3 line coding is used.

Launching the LFPS Generator

To launch the **LFPS Generator**:

- Go to the **Menu Bar** > **Generator** and then select **LFPS Generator**.

The **LFPS Generator** interface will appear as shown in the following figure:



The **LFPS Generator** interface consists of the following GUI elements:

- Toolbar
- Properties Window
- LFPS Graphical View

The listed GUI elements are described in the section that follows.

Toolbar

The **LFPS Generator** toolbar provides the following convenient functions:

Table 56

Icon	Name	Description
	Download	Click this button to download the pattern and sequence to the selected location. An orange button indicates that the pattern is modified and is not yet downloaded to any location.
	Start	Click this button to start the LFPS generation.
	Stop	Click this button to stop the LFPS generation.
	Reset	Click this button to reset the LFPS parameters to default values.

Properties Window

The **Properties** window allows you to set the properties of the LFPS parameters for the selected location. For each location, it contains two types of parameters:

- Instrument Configuration - It has the following property:
  - Generator - Use this drop-down option to select the generator location.
- LFPS - It has the following properties:

Properties	Description	Range
Test Mode	Allows the user to select between 'Rx Testing' and 'Calibration' mode. The default mode is 'Rx Testing'.	Rx Testing, Calibration
Protocol	The USB4v2 protocol to be used for LFPS Generation. Based on the selected protocol the data rate for the LFPS is set.	USB4 Gen2 (10 Gbps), USB4 Gen3 (20 Gbps) and USB4 Gen4 (25.6 Gbps)
Coding	Show the currently used line coding as per the selected protocol. This is a read only property.	-
Data Rate	It shows the data rate for the selected protocol. This is a read only property.	-
Period	The period of LFPS cycle.	20 to 80 ns
Pre Data	Period of time in which electrical idle will be set after the LFPS sequence.	80 to 120 ns
Pre-Data (Adjusted)	LFPS pre-data duration after the pattern block granularity adjustment in ns.	-
Cycles	Number of LFPS cycles.	1 to 100
Duty Cycle	The Duty Cycle of the LFPS signal.	45 to 55 %
EI Duration	The duration of electrical idle.	20 to 80 ns
Test Pattern	Displays the test pattern of the selected protocol. This is a read-only property.	-

LFPS Graphical View

The **LFPS Graphical View** provides a visual representation of the LFPS sequence blocks based on the selected test mode. It displays waveform data used for LFPS generation as a function of time, with the X-axis representing duration in nanoseconds (ns) and the Y-axis representing waveform amplitude in volts (V). The graph also highlights key LFPS parameters and their corresponding durations.

Rx Testing Mode

The following figure shows the visual representation of the LFPS sequence blocks in **Rx Testing** mode:

In this mode, the waveform graph displays the following sequence blocks:

- EI Idle Block

  Represents the Electrical Idle (EI) portion of the LFPS sequence. The graph shows the EI signal pattern.
- LFPS Burst and Pre-Data Block
  - For an LFPS burst, the graph shows up to 6 cycles:
    - If the burst has ≤ 6 cycles, all cycles are shown with their actual duration.
    - If the burst has > 6 cycles, the graph shows the first 3 and the last cycle as solid lines, while the 4th and 5th cycles are shown as dotted lines to represent the middle portion.

- The Pre-Data portion is shown immediately after the LFPS burst. This corresponds to the Electrical Idle data after the LFPS burst in the ‘LFPS Burst and Pre-Data’ sequence block pattern. The Pre-Data length is adjusted to meet the sequence block granularity requirement.

- USB4 Test Pattern Block

  The USB4 test pattern block will be displayed as a rectangle with the label 'USB4 Data' and the test pattern name for the currently selected PHY Protocol.

Calibration Mode

The following figure shows the visual representation of the LFPS sequence blocks in **Calibration** mode:

In this mode, the graph displays the following LFPS sequence blocks:

- EI Idle Block

  Represents the Electrical Idle (EI) portion of the LFPS sequence. The graph shows the EI signal pattern.

- LFPS Continuous Block

  Represents a continuous LFPS cycle repetition. The same LFPS cycle repeats until the sequence is stopped by clicking Break.

  - The graph will always show fixed number of LFPS cycle repetitions (8 cycles), regardless of the actual duration.

Generating LFPS Pattern and Sequence

Follow the given steps to generate the LFPS pattern and sequence:

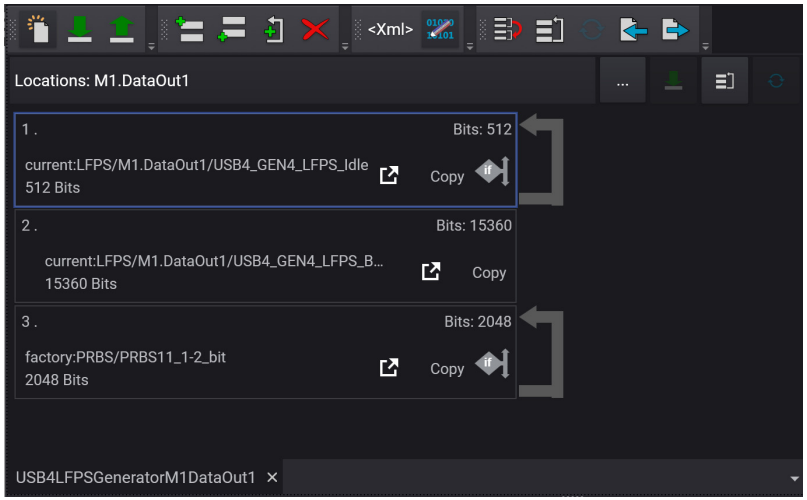
1 Set the LFPS generator properties. For details, see Properties Window on page 504.

2 Click the '**Download**' button. When this button is clicked, it creates the LFPS sequence combining the LFPS patterns in separate sequence blocks in the sequence editor.
In 'Rx Testing' mode the LFPS sequence contains the following blocks:
   - EI Idle block
   - LFPS Burst and Pre-Data block
   - USB4 Test Pattern block

   The following table shows the memory pattern used for different protocols:

Protocol	Test Pattern
USB4 Gen 2	factory:USB_4.0/USB4_GEN2_SLOS1
USB4 Gen 3	factory:USB_4.0/USB4_GEN3_SLOS1
USB4 Gen 4	PRBS 2^11 -1

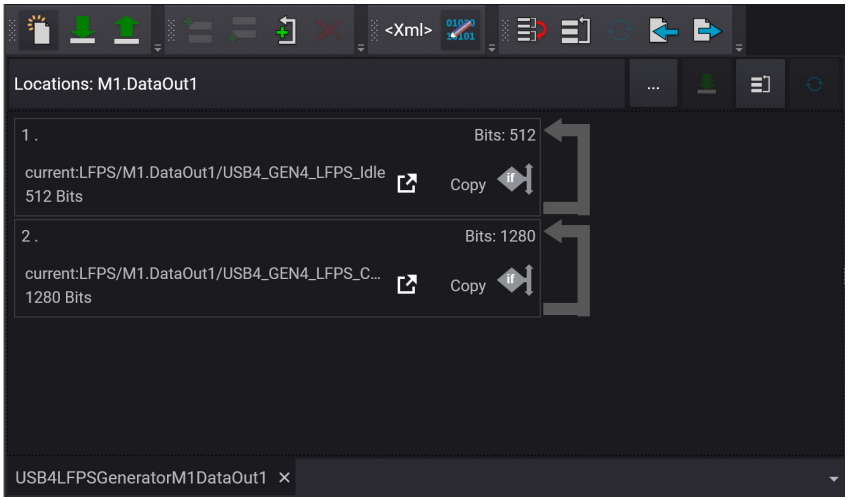
The following image shows the LFPS sequence for 'Rx Testing' test mode:



In 'Calibration' mode the LFPS sequence contains the following blocks:

- EI Idle block
- LFPS Continuous

The following image shows the LFPS sequence for 'Calibration' test mode:



3 To start LFPS generation, the user needs to click the 'Run' button. This will move the sequence from the 'EI Idle' block to the next one.

If the Test Mode is 'Rx Testing', clicking 'Run' button will execute the 'LFPS Burst and Pre-Data' block once, then move to the 'Test Pattern' block, which will play continuously.

If the Test Mode is 'Calibration', clicking 'Run' button will move the sequence from 'EI Idle' to the 'LFPS Continuous' block, which will play continuously.

Clicking the 'Stop' button will restart the sequence and return to the 'EI Idle' block, which will play until the 'Run' button is clicked again.

M8000 Series of BER Test Solutions
User Guide

6 Setting up Analyzer

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KEYSIGHT TECHNOLOGIES

Overview

The M8020A/M8040A/M8050A Analyzer examines an incoming bit stream, compares it to the expected pattern, and locates any inconsistencies. The Analyzer requires the following settings to work correctly:

- The expected pattern

  The Analyzer needs to "know" which data to expect so that it can detect bit errors. No expected patterns are required in BRM mode.
- Correct clock frequency

  Required to recognize the bit rate in the data stream.
- Appropriate sampling point

  The sampling point defines where the Analyzer tries to differentiate between 0s and 1s in the data stream. This is necessary so that the Analyzer recognizes the data bits correctly.
- Synchronization to the incoming pattern

  The expected pattern must be synchronized to the incoming pattern so that the Analyzer can find any discrepancies.

The Analyzer provides the following functions to enable you to perform tests:

- Automatic pattern synchronization

  The Analyzer shifts the incoming data stream bitwise to match it to the expected data pattern. A correct BER can only be measured with matching patterns.
- Error accumulation

  You can specify whether a test runs for a specified time or until a specific number of errors has occurred. This lets you carry out longer tests while logging the results to a file.
- BER location mode

  You can specify whether all errors are counted or only the errors that occurred on a particular bit position or range of positions.
- Trigger output for external measurement instruments

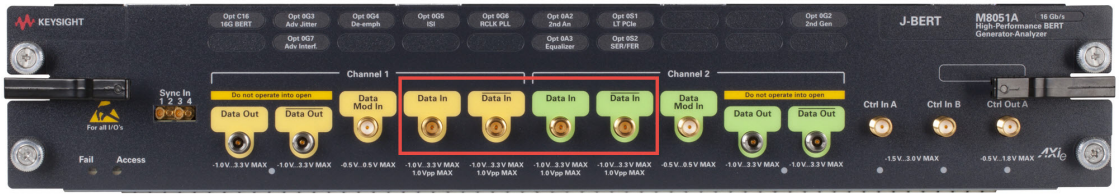
  This allows you to connect other devices for further error analysis.
- Data format

  The M8040A (M8046A) and M8050A (M8043A) analyzer has an enhanced capability over M8020A analyzer to analyze PAM4 data in addition to NRZ.

M8020A/M8040A/M8050A Analyzer Ports

The M8020A/M8040A/M8050A analyzer's ports are used for running tests and for connecting external equipment.

The following figure shows the J-BERT M8041A analyzer's ports.



The M8041A analyzer's ports include the following:

- Data In and $\overline{\text{Data In}}$

  This port is connected to the data signal and the inverted data signal.

The following figure shows the M8040A analyzer's (M8046A) ports.

The M8046A analyzer's ports include the following:

- Data In and $\overline{\text{Data In}}$

  This port is connected to the data signal and the inverted data signal.
- Clk In

  This is a clock input port to sample the incoming data. Supports full/half and quarter-rate clock. Single ended.
- Ctrl In A

  This port can be used as sequence trigger or pattern capture event.
- Ctrl Out A

  This port outputs a pulse in case of an error. It generates a pulse or static high/low if used from sequencer.

The following figure shows the M8050A analyzer's (M8043A) ports.

The M8043A analyzer's ports include the following:

- Remote Head

  This port provides data input and control signals for M8052A remote head.
- Clk In

  This port enables source-synchronous operation, allowing effective analysis of data with Spread Spectrum Clocking (SSC). Clock Input operation requires M8043A serial number above MY64A01000.
- Ctrl In

  This port provide functionality that can be selected as: sequence trigger, pattern capture event.
- Ctrl Out

  This port outputs a pulse in case of an error. It generates a pulse or static high/low if used from sequencer.

Data In Port Termination

To ensure a valid setup and to protect the devices from damage, proper termination must be specified for both **Data In** connections. You can specify the termination by entering the termination voltage in the respective field.

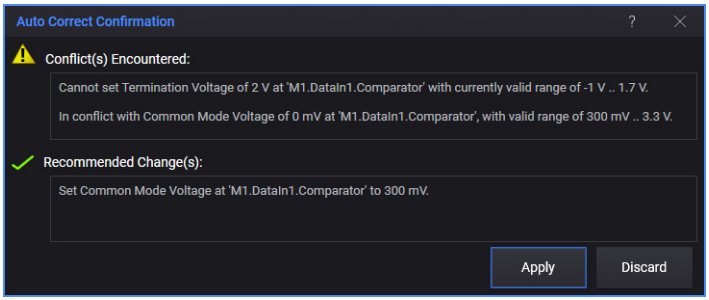
CAUTION **Selecting the wrong termination may damage your device.**

NOTE When the Data Out and Data In ports are not connected and are terminated with 50 Ω resistor, the Data Loss and Sync Loss indicators may appear red or blink. This is normal behavior and does not indicate a hardware fault.

Why Can Wrong Terminations Damage Your Device?

Choosing wrong terminations may cause your device to output voltage levels that are not as expected. It may also cause excessive current or current flow in the wrong direction, which can damage your device.

If you adjust the termination voltage, and try to enter value(s) which are outside of the currently allowed window, the Auto Correction Confirmation message box will pop up with respective apply and discard options as shown in the following figure:



Setting Up Termination

To select the termination for the Analyzer:

NOTE You must know the termination voltage of the data signal that your DUT sends to the Analyzer.

1. Go to the **Menu Bar** > **Analyzer** and then select **Data In**.
2. Select **Comparator** functional block from the **Parameters** window.
3. In the **Termination Voltage** field, enter the termination voltage that is appropriate for the incoming data signal.

CAUTION Selecting the wrong termination may damage your device.

4. In the **Polarity** field, select **Inverted** if your device inverts data.

You can now physically connect the DUT to the Analyzer.

Compare Mode

The selection in this list defines how the signals arriving at the **Data In** and **/Data In** connectors are interpreted. The following options are available:

- Differential

  If differential mode is selected, both input ports need to receive a signal. The actual data signal is measured as the voltage difference between the two incoming signals.
- SE-Normal (Single Ended - Normal)

  In normal mode, only the **Data In** port receives the data signal, the **/Data In** port is inactive.
- SE-Complement (Single Ended - Complement)

  In complement mode, only the **Data In** port receives the data signal, the **/Data In** port is inactive.
- Single-Ended

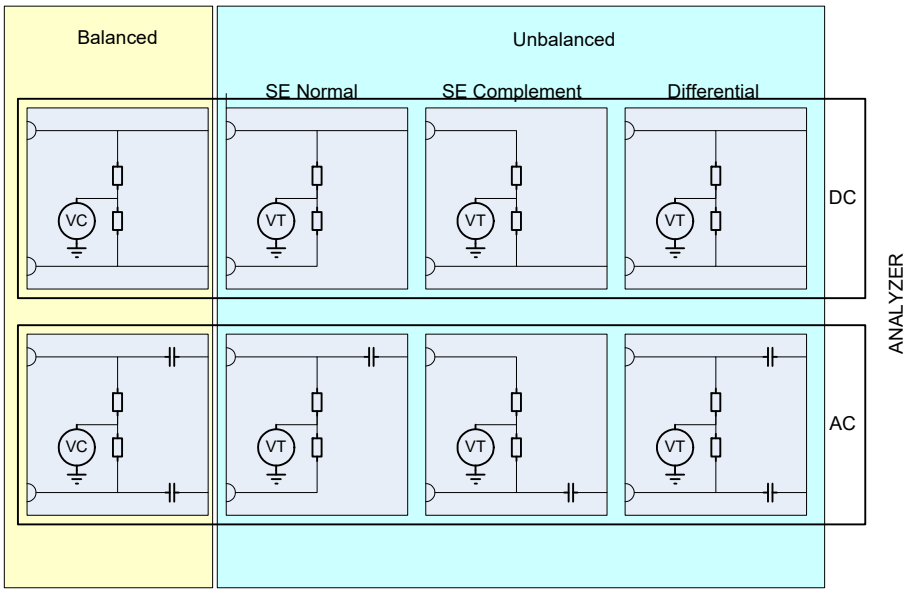
  In the Single-Ended mode, the data stream is provided at either Normal input or Complement input. The other input is either left open or terminated with 50 Ohm.

NOTE When compare mode is set to Differential, the amplitude value is split in half to give a peak to peak value equal to amplitude set. In Single-Ended mode, the value is similar to the value set in the Amplitude parameter.

NOTE The availability of the particular compare mode selection depends on the currently used hardware.

The following drawing is an example how the instrument internal circuitry looks like for different settings.

This figure is only true for M8041A and M8051A modules with serial numbers < DE55300500.



VT = Termination Voltage

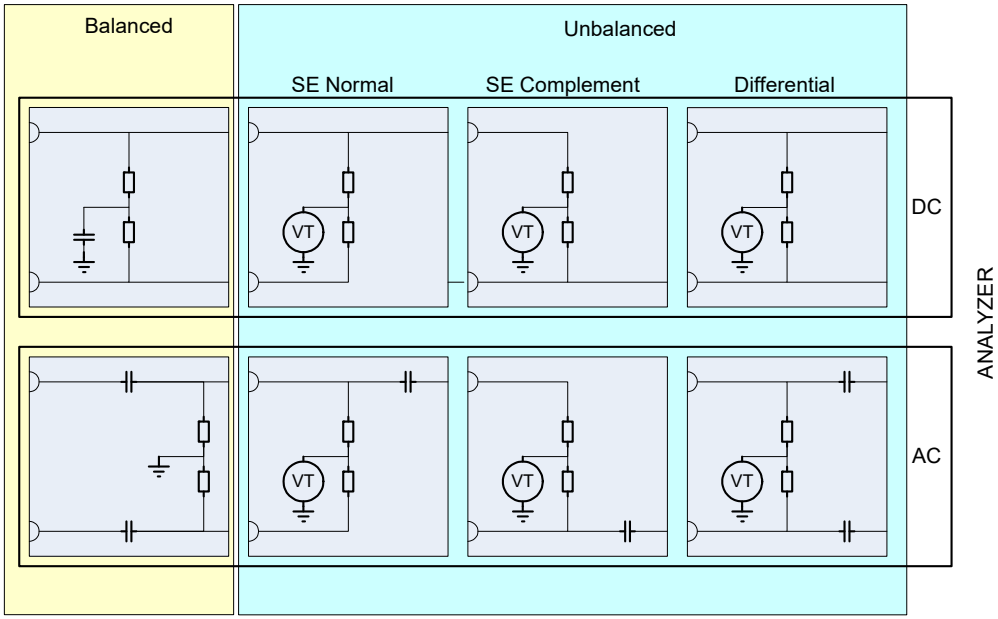
VC = Common Mode Voltage

This figure shows what the analyzer represents as termination scheme to the DUT. The DUT would be connected to the connectors shown on the left part of the respective schemes above.

For the balanced settings the internal termination voltage of the analyzer is set to equal the Common Mode Voltage, which must be given by the user in the GUI.

The following figure shows a slightly modified figure for the analyzer part:

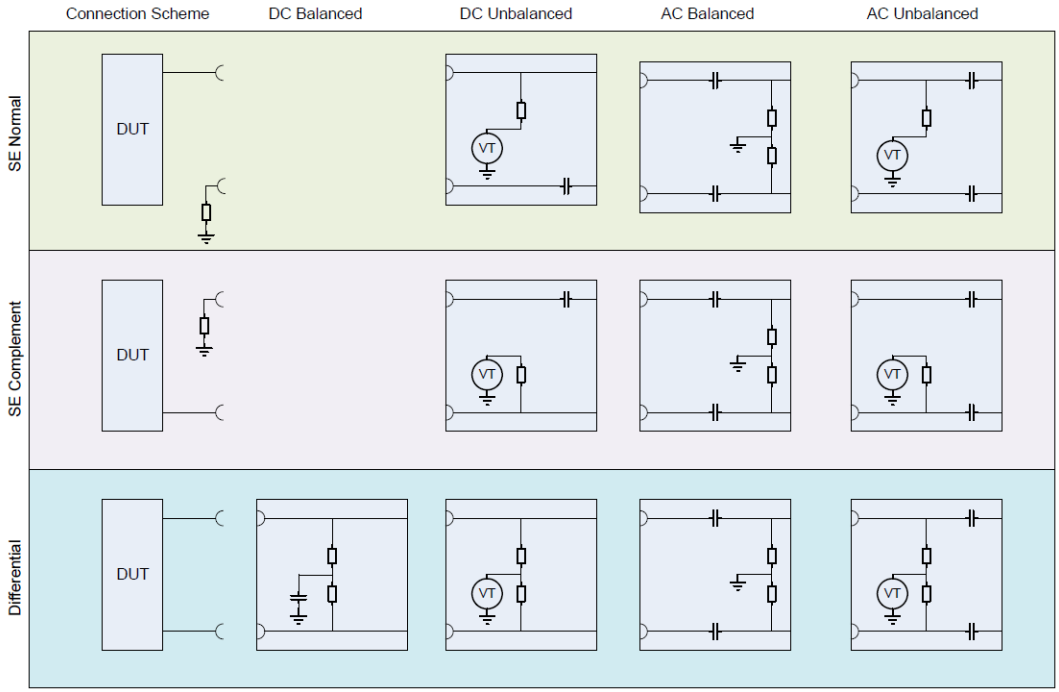
This figure is true for M8041A and M8051A modules with serial numbers >= DE55300500.



VT = Termination Voltage

This above figure shows what the analyzer represents as termination scheme to the DUT. The DUT would be connected to the connectors shown on the left part of the respective schemes above.

The following figure is true for M8046A modules.



Data Inverted

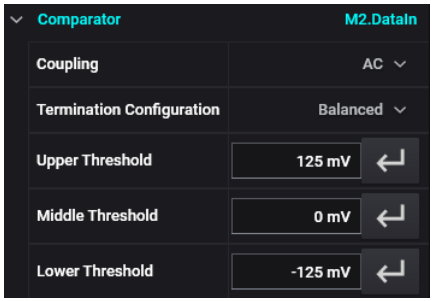
To activate data inverted function, select the **Polarity** as **Inverted** in the **Comparator** functional block of the **Analyzer**. This function is required if your device inverts data.

Threshold

Enter a **Threshold** value for applications that do not provide a continuous data stream at the input (for example, any application using bursts), because the averaged threshold voltage will drift from the correct level when there is no input.

PAM4 Decision Threshold

It is only available for PAM4 line coding. It controls the decision threshold of the PAM4 decoder within the data input's input window. The setting of the PAM4 decision thresholds always refers to the actual input voltage range.



The following 3 decision thresholds are applied:

Threshold	Symbol
Lower	Decides between symbol 0 and symbol 1.
Middle	Decides between symbol 1 and symbol 2.
Upper	Decides between symbol 2 and symbol 3.

Termination Voltage

In this field, enter the termination voltage that is appropriate for the incoming data signal. This selection should be made before the device is connected to the analyzer.

CAUTION Selecting the wrong termination may damage your device.

The **Data In** port is connected to a 50 Ω load impedance (or termination) within the **Analyzer**. Data termination refers to the voltage level at the end of this load. The logic output from a device requires any connected equipment, including the **Analyzer**, to have a specific termination voltage.

Input Range

Before you can synchronize the **Analyzer** to the incoming data stream, you need to define the voltage range within which the eye is located.

Both the high and low level of the data signal must be within this range to find the eye.

NOTE The input voltage range for M8020A, M8040A is 2V and 500 mV, respectively. The input voltage range for M8050A is 50 mV and 600 mV, respectively. When you modify either the high or low voltage, the other voltage is automatically adjusted.

Squelch Threshold

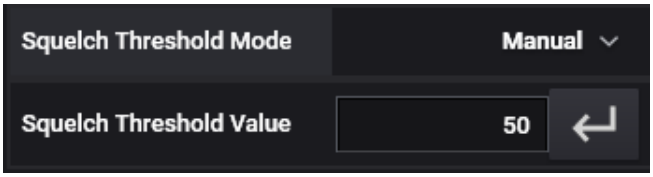
The **Squelch Threshold** feature allows you to adjust the squelch threshold values in link training applications (e.g. USB link training).

NOTE This feature is only available with M8020A modules (M8041A and M8051A).

It has the following parameters:

- **Squelch Threshold Mode** - Use this parameter to select either **Auto** or **Manual** mode. In the **Auto** mode, the instrument works with factory calibrated values. In the **Manual** mode, user is allowed to adjust the current squelch threshold value.

  The following figure shows the available parameters in the **Manual** mode:



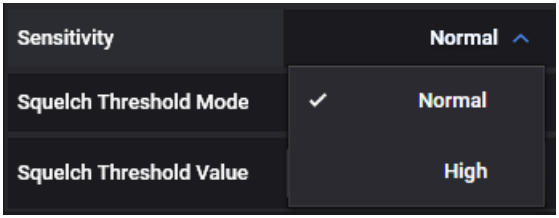
- **Squelch Threshold Value** - Use this parameter to set the squelch threshold value in range from 0 ... 255.
- **Preset Button** - Use this button to set the default squelch threshold value.

Input Sensitivity

The Sensitivity parameter enables you to set the error detector input sensitivity to normal or high.

NOTE This feature is only available with M8020A modules (M8041A and M8051A).

1 Go to **Menu Bar** > **Analyzer** and then select **Data In**.
2 Select **Comparator** functional block from the **Parameters** window.
3 From the **Sensitivity** drop-down list, select an option.
The following options are available:
- Normal
- High



Input sensitivity*	50 mV typical @ normal sensitivity mode†
	40 mV typical @ high sensitivity mode[2]

* *Measured with PRBS 2^{31} - 1 at 16 Gb/s, AC coupling mode, BER of 10-12, CTLE disabled.*

† *Eye height measured at input of reference cable M8041A-801 with DCA-X module 86117A. Applies for single ended and differential input signals.*

Clock Setup

To measure the **Bit Error Rate** with the **Analyzer**, the bit rate of the data stream must be known. Depending on the options the instrument is delivered with, you could use either an external clock source for the Analyzer (for example, the clock from the generator), or extract the clock signal from the incoming data (CDR mode).

CDR mode does not work for all kinds of data patterns. For example, if the device under test sends only blocks of ones and zeros, there are no transitions in the data stream and the M8020A cannot recover the clock.

Also, if you are testing bursts, there are some special considerations for setting up CDR.

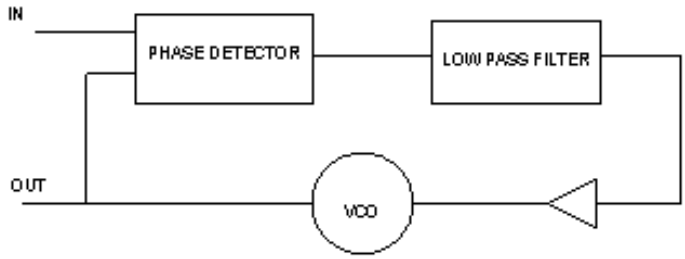
How does Clock Data Recovery Work?

In CDR mode, the CDR has to recover the clock from the incoming data. To do this, the hardware has to decide whether the voltage at the input connector is a logical '1' or '0' and then recover the clock from the detected transitions.

Clock Data Recovery (CDR) is a special kind of Phase Locked Loop (PLL), which recovers clock signal of a data stream. It is a regulatory loop, which synchronizes the local oscillator with an external reference, in this case the incoming data stream.

Phase Locked Loop

A PLL has three parts: a phase detector, a loop filter, and a Voltage Controlled Oscillator (VCO). The phase detector has two inputs, and one output, which is proportional to the phase difference of the inputs. The loop filter is a low pass filter which attenuates the higher frequencies from the output of the phase detector. The VCO is an adjustable oscillator which changes the output frequency depending on its input voltage. The diagram below shows a simple PLL.



One of the most important characteristics of a PLL is its loop transfer function.The loop bandwidth is defined as the integrated magnitude of the PLL's frequency transfer function over the entire frequency spectrum. The loop bandwidth describes how the regulatory loop tracks the VCO to a sine wave FM modulated input signal. Above the bandwidth the loop cannot track such a modulation completely, and thus, the response to the modulation is attenuated.

The other loop parameter is peaking. This describes how much a modulation is exaggerated (mostly close to the loop bandwidth).

Transition Density

The transition density is defined by the number of transitions in the incoming data divided by the total number of bits transmitted. In this field enter the transition density in (%).

This parameter affects the loop bandwidth, and thus must be entered correctly. Some standards specify the loop bandwidth for a given transition density. In such a case enter the value given in the specification, so that the CDR behaves according to the standard. If a standard from the preset list is selected, this field is also preset.

Loop Bandwidth

This is the range of the CDR loop bandwidth. In this field the user should enter the loop bandwidth value; the range is within 313 kHz to 20 MHz.

When the M8020A/M8040A/M8050A Analyzer is used to characterize a data stream instead of a receiver, the loop parameters should be set according to the used standard.

If the CDR is used to recover the bit stream from a receiver to be characterized due to a lack of a clock output, choose the loop bandwidth significantly higher than the receiver's bandwidth. To characterize a DUT's

CDR it is the best practice to use its recovered clock output instead of the M8020A's built in CDR. Choose a low loop bandwidth to measure the jitter on an incoming data stream as the CDR will track the incoming jitter up to the loop bandwidth and thus make it invisible to the Analyzer.

CDR Spread Spectrum Clocking

This control is used to adapt the CDR to an input bit stream with SSC.

Enabling SSC state widens the loss of lock detection window, and sets the peaking to optimum SSC performance. Enter the **Expected Deviation** and the type of deviation (**Up-Spread**, **Down-Spread** or **Center-Spread**) to set the locking window to an optimum.

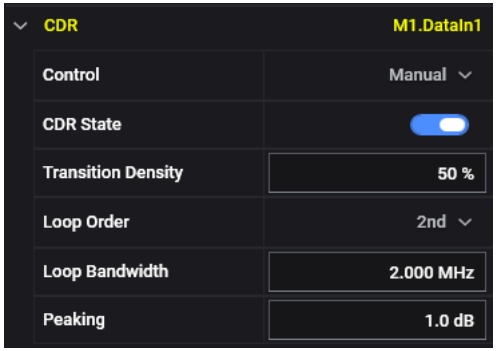
SSC is mostly used **Down-Spread** which means, the clock signal is modulated to a lower frequency and back. Thus the average frequency is lowered by half of the maximum deviation. The CDR is adapted to that value. Enter the maximum deviation as specified in the standard.

CDR Setup for M8020A

The M8020A has an internal CDR. Follow the given steps to perform a **CDR Setup**:

1 Go to the **Menu Bar** > **Analyzer** and then select **Data In**.

2 Select **CDR** functional block from the **Parameters** window. The following parameters will appear:



3 Click **CDR State** switch to turn on the CDR state.

4 Specify the CDR parameters setting. For details on CDR parameters, refer to .M8020A CDR Parameters on page 525.

M8020A CDR Parameters

The M8020A has the following parameters:

- **Control**: You can specify whether the CDR is controlled by the pattern sequence or if it is manually enabled or disabled.
- **CDR State** - It enables or disables the CDR state.
- **Transition Density**: It affects the loop parameters, and it must be either entered, or measured. Some standards define a loop bandwidth for a specific transition density.
- **Loop Order** - The data stream contains multiple frequencies, and the CDR needs to know the expected data rate. You can choose between 2 types of CDR; 1st order and 2nd order.
- **Loop Bandwidth**: It is the input parameter to set the characteristics of the loop.
- **Peaking**: Additionally, you can set the value for peaking in the provided field. It defines the second order CDR characteristics by defining a peaking value which is valid for jitter transfer function. The peaking parameter is only available for the second Loop Order.

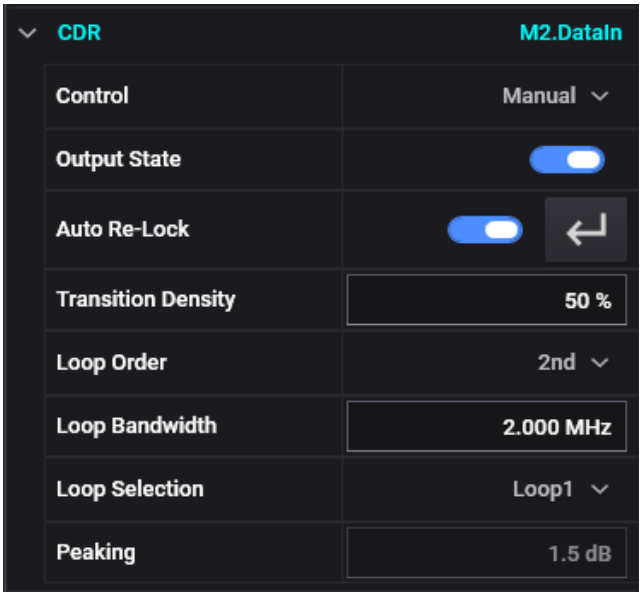
CDR Setup for M8040A

The M8040A system supports internal as well as external CDR.

Internal CDR Setup

The M8040A system has an internal CDR. Follow the given steps to perform a **CDR Setup**:

1. Go to the **Menu Bar** > **Analyzer** and then select **Data In**.
2. From the **Parameters** window, select the clock source as “CDR”. The following parameters will appear:



3 Click **CDR State** switch to turn on the CDR state.

4 Specify the CDR parameters setting.

- **Control**: You can specify whether the CDR is controlled by the pattern sequence or if it is manually enabled or disabled.
- **Output State** - It enables or disables recovered clock signals at the Rec Clk Out.
- **Auto Re-Lock** - It enables or disables the automatic clock recovery locking.
- **Transition Density**: It affects the loop parameters, and it must be either entered, or measured. Some standards define a loop bandwidth for a specific transition density.
- **Loop Order** - The data stream contains multiple frequencies, and the CDR needs to know the expected data rate. You can choose between 2 types of CDR; 1st order and 2nd order.
- **Loop Bandwidth** - It is the input parameter to set the characteristics of the loop.
- **Loop Selection** - It specifies type 2 loop transition frequency and thereby the JTF peaking. The choices are Loop1, Loop2, Loop3 and Loop4.

- **Peaking**: Additionally, you can set the value for peaking in the provided field. It defines the second order CDR characteristics by defining a peaking value which is valid for jitter transfer function. The peaking parameter is only available for the second Loop Order.

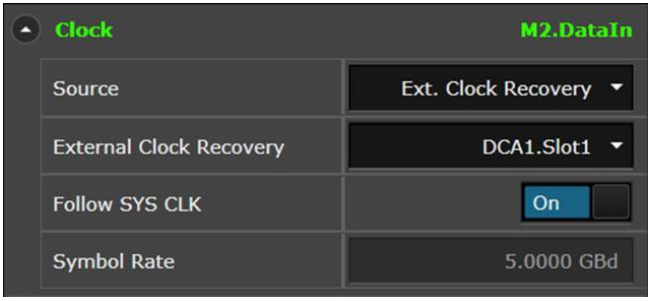
External CDR Setup

The N1076A/77A can be assigned to an M8046A error detector to be used as an external clock recovery. In this case, M8046A will ensure that certain critical parameters are automatically kept in sync between M8046A and N1076A/77A. To use the N1076A/77A from within M8070B, the FlexDCA N1000-Series System Software has to be started and fully running before starting M8070B. Once all these instruments are connected, start the M8070B software. For details on connections and how to access N1076A/77A from within M8070B, refer to *M8070B Advance Measurement Package User Guide*.

Follow the given steps to perform a **CDR Setup**:

1 Go to the **Menu Bar** > **Analyzer** and then select **Data In**.

2 Select **Clock** functional block from the **Parameters** window. The following parameters will appear:



3 Select 'Ext. Clock Recovery' as Clock Source of M8046A.

4 Choose one of the available external clock recoveries under "External Clock Recovery".

For further details, refer to *M8070B Advance Measurement Package User Guide*.

CDR Setup for M8050A

The M8050A system supports both internal as well as external clock.

The Clock Input of the M8043A enables source-synchronous operation, allowing effective analysis of data with Spread Spectrum Clocking (SSC). During this operation, the M8043A's Clock Data Recovery (CDR) helps reduce clock-data skew and jitter. For optimal SSC tracking, the clock and data signals must be aligned to minimize residual jitter. The M8043A can receive clock and data inputs from various devices, including the M8009A for source-synchronous operation.

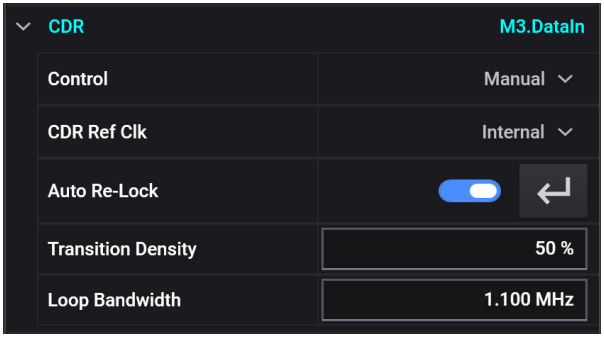
The M8043A requires a serial number above MY64A01000 for Clock Input functionality.

CDR Setup

Follow the given steps to perform a **CDR Setup** in M8050A system:

1 Go to the **Menu Bar** > **Analyzer** and then select **Data In**.

2 From the **Parameters** window, select the **CDR** functional block. The following parameters will appear:

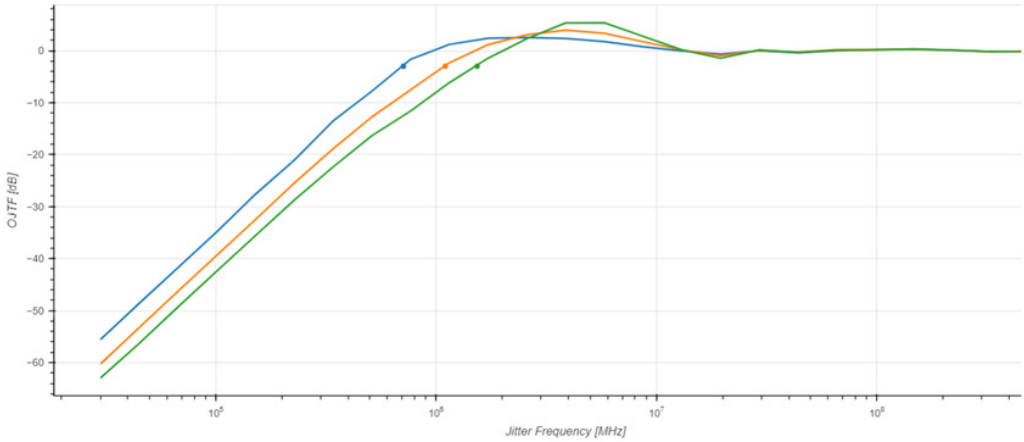


3 Specify the CDR parameters setting.

- **Control**: You can specify whether the CDR is controlled by the pattern sequence or if it is manually enabled or disabled. In case of Manual, there is no option to disable the CDR.
- **CDR Ref Clk** - This option selects the CDR reference clock that enables the source-synchronous operation which can be used for SSC tracking. The reference clock that can be selected is 4, 8 or 16 GHz.
- **Auto Re-Lock** - It enables or disables the automatic clock recovery locking.

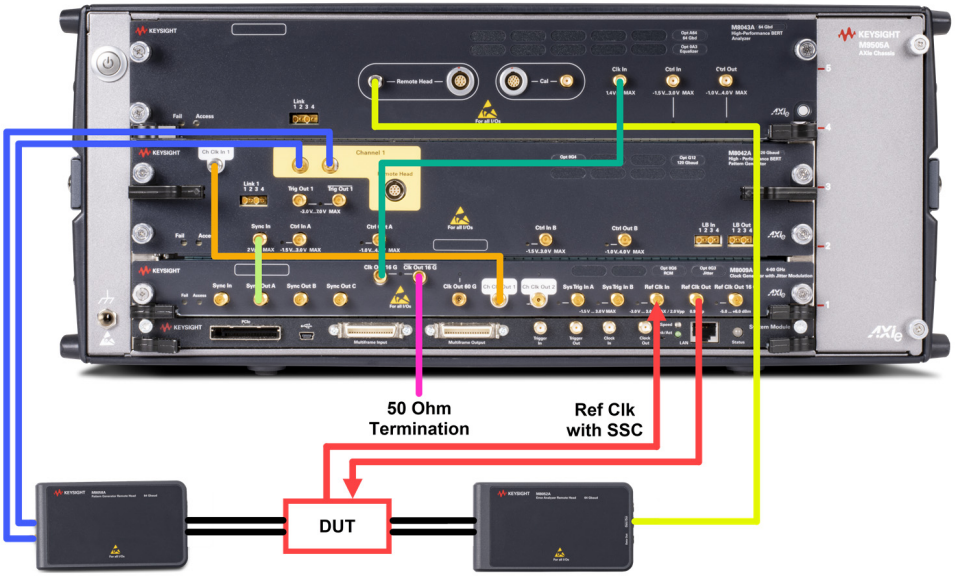
- **Transition Density**: It affects the loop parameters and it must be entered. Some standards define a loop bandwidth for a specific transition density.
- **Loop Bandwidth** - It is the -3 dB corner frequency of the CDR's observed jitter transfer function (OJTF).

  Example: The following image shows CDR with 0.7, 1.1 and 1.5 MHz OJTF loop bandwidth:



Setting up Source-Synchronous Operation

The following diagram demonstrates the process of setting up the source -synchronous operation using the M8042A, M8009A and M8043A modules.



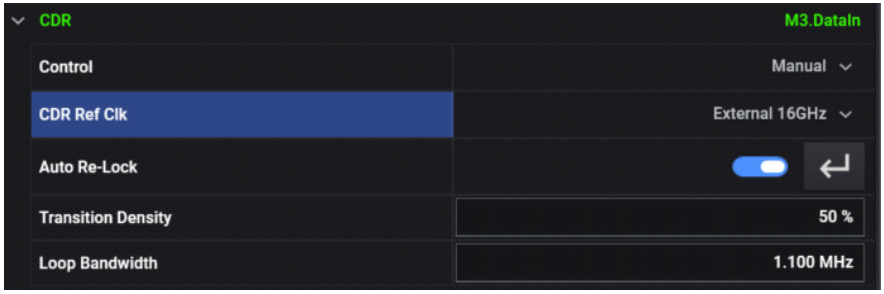
1 Connect the M8009A Channel Clock Out 1 port to the M8042A Channel Clock In 1 port using a semi-rigid cable.
2 Connect the M8009A Sync Out A port to the M8042A Sync In port using a 3.5 mm sync cable.
3 Terminate the M8009A Clk Out 16 G complement port with 50-ohm.
4 Connect the M8009A Clk Out 16 G port to the M8043A Clk In port.
5 Connect the M8042A to the M8058A remote head, which is then connected to the DUT (Device Under Test).
6 Connect the M8043A to the M8052A remote head, which is then connected to the DUT.
7 The connection of the Ref Clk depends on the mode of operation. If the DUT provides the reference clock with SSC, the connection is made from the DUT to the Ref Clk In of the M8009A. However, if the M8009A is used as the reference, the Ref Clk Out of the M8009A is connected to the DUT.

Setting the Optimal Jitter Delay in Source-Synchronous Operation

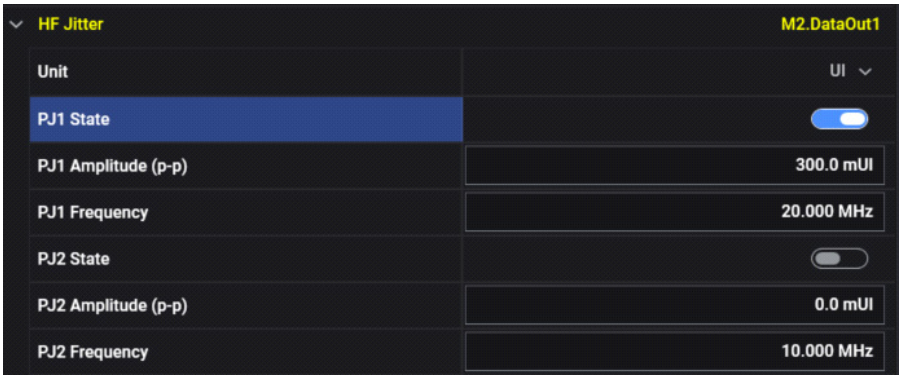
For a M8050A setup with M8042A, M8043A and M8009A, the optimal Jitter Delay can be determined as explained in the following steps. If the DUT is not forwarding the PJ sent by the M8042A to the M8043A, the Jitter Delay does not need to be optimized. In source-synchronous operation, SSC can be compensated without setting the optimal jitter delay.

For this setup, the Clk Out 16G of the M8009A is used as the reference clock for the Clk In of the M8043A.

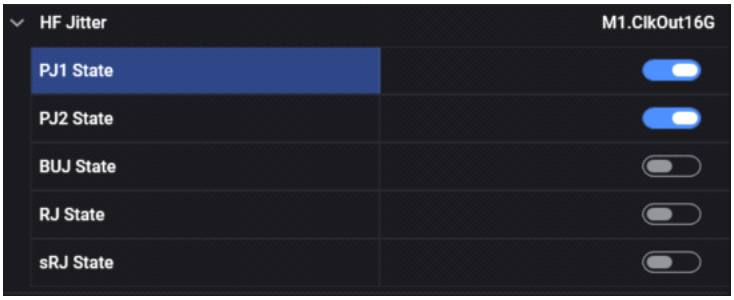
1 Go to the **Menu Bar** > **Analyzer** and then select **Data In**. From the **Parameters** window select the **CDR** functional block. The parameter **CDR Ref Clk** should be set to external to enable source-synchronous operation.



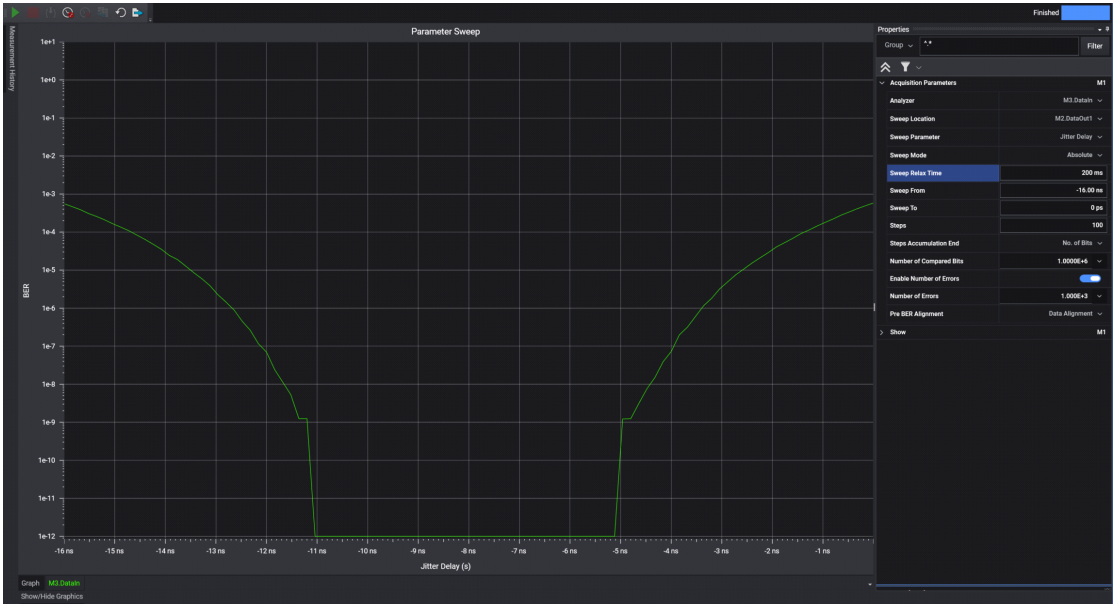
2 Go to the **Menu Bar** > **Generator** and then select **Data Out**. From the **Parameters** window, select the **HF Jitter** functional block. Set **HF Jitter** for M8042A to 0.3 UI PJ with a PJ frequency of 20 MHz.



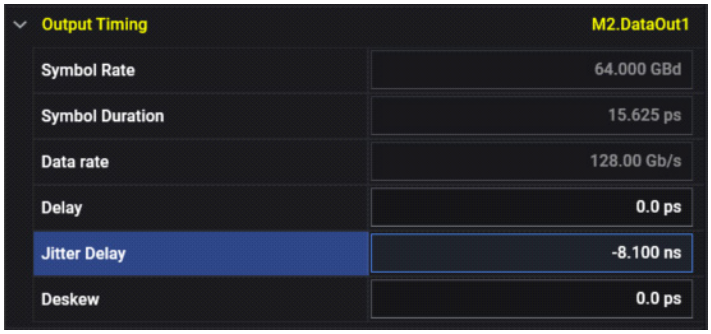
3 The Jitter also needs to be enabled for the Clk Out 16G. Therefore, go to the **Clk Out 16G** tab and then select the **HF Jitter** functional block. Enable the **HF Jitter** as shown in the following figure:



4 Go to the **Menu Bar** > **Measurements** > **Parameter Sweep** and run a sweep over the Jitter delay like shown in the measurement below. A Sweep Relax Time of 200 ns should be set, and for Pre-BER alignment, "Data Alignment" should be selected.



5 The optimal Jitter Delay can be determined from the Parameter Sweep. It is the center of the range in which the BER was smaller than 1e-12. Go to the **Menu Bar** > **Generator** and then select **Data Out**. From the **Parameters** window, select the **Output Timing** functional block. In this case the optimal **Jitter Delay** is set to -8.1 ns.



Pattern Synchronization

The M8020A/M8040A/M8050A calculates bit error rates by comparing the received data with the expected data patterns. To do this, it needs to know where the start of the pattern is located in the data stream.

Introduction to Pattern Synchronization

Pattern synchronization (sync) refers to aligning the incoming data pattern with the internal reference pattern.

Hardware-Generated Patterns

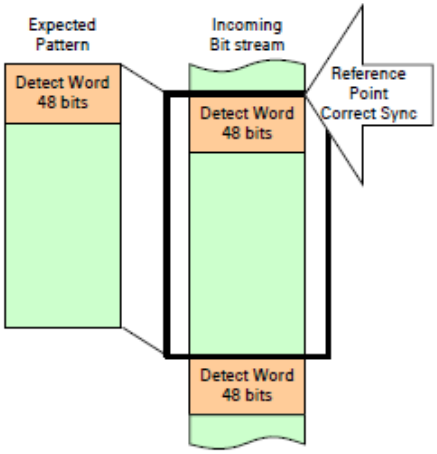
For 2^n-1 PRBS patterns, bits from the incoming data pattern "seed" the Analyzer's Generator, causing it to generate a precisely aligned internal reference pattern.

Memory-Based Patterns

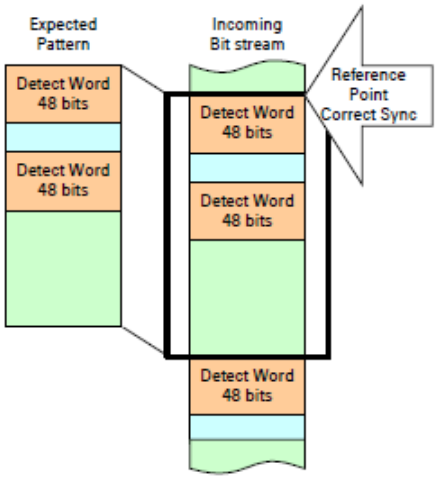
For software-generated and user patterns, a 48-bit pattern from the pattern is used as a detect word. Optimally, this detect word should be unique within the entire pattern. The Analyzer searches for this detect word within the incoming data stream, and uses the point in the data stream as a reference, and compares all following bits with the pattern. If the measured BER is better than the synchronization BER, the Analyzer will be synchronized.

There are thus three possible outcomes for a synchronization:

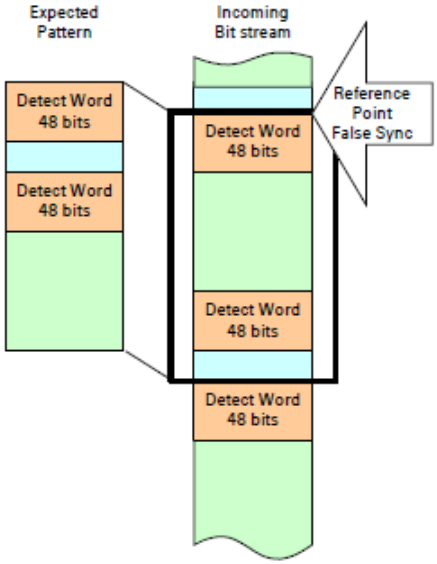
- Single instance of the detect word in the data stream



- Multiple instances of the detect word with correct synchronization.



- Multiple instances of the detect word with false synchronization.



If the **Analyzer** attempts to synchronize on the incorrect detect word, the BER will be unacceptably high, and, if automatic synchronization is selected, the **Analyzer** attempts another re-sync.

The detect word on which the **Analyzer** attempts to re-sync is chosen strictly by chance. So if there are two instances of the detect word in the pattern, the Analyzer has a 50% chance of selecting the correct one.

The more instances of the detect word exist in the pattern, the higher are the chances for incorrect synchronization. The software attempts in any case to identify a 48-bit pattern that occurs as seldom as possible in the pattern. For very large patterns, this can unfortunately take a very long time, and the software ends the search if it expects that it would take longer to find an adequate detect word than it would to attempt to synchronize. If the search for a detect word is ended, the most unique detect word identified is used.

Patterns must always be synchronized in order to do accurate BER testing. If patterns are out of alignment by just one bit, errors can be as high as 50% (5E-1) for PRBS patterns, and 100% (1E+0) for custom patterns.

By default, the **Analyzer** is in automatic sync mode with a sync threshold of 1E-3. This setting is recommended for most applications, and usually allows the synchronization function to be "transparent", requiring no attention. However, for special applications, changes can be made to the sync mode and sync threshold.

What Type of Synchronization Should You Use?

The type of synchronization you use affects how errors are measured and displayed. A **Sync Loss** is recognized when the BER is greater than the sync threshold. This can be caused by a high error rate, pattern misalignment, or clock loss. Choose the sync mode setting that is appropriate for the type of errors you anticipate.

- Automatic Sync with a sync threshold BER of 1E-3 is recommended for most applications.

  With this mode selected, the synchronization algorithm starts whenever the BER exceeds the threshold. However, it is not possible to make accurate BER measurements higher than the sync threshold.
- Manual sync can be used for synchronizing once, confirming proper pattern alignment, and then measuring BERs higher than the sync threshold. This is useful for the following applications:
  - To monitor the integrity of clock signals. You may wish to measure BERs that exceed the sync threshold to confirm clock slip.
  - To collect data for constructing eye contour information. You may wish to move the sampling point to locations in the data eye that have BERs exceeding the sync threshold.

  This mode doesn't allow the analyzer to automatically synchronize if the BER becomes greater than the sync threshold. For example, the analyzer will not re-synchronize after momentary clock loss.

NOTE **Adjusting the data input delay may cause momentary clock loss. If you select Manual Sync mode, this may also result in sync loss.**

- Burst sync mode is a special operating mode for measuring data in bursts of bits, rather than one continuous stream of bits.

NOTE If the Analyzer is in Manual Sync mode, it is recommended that you keep an eye on the **Sync Loss** indicator, present on the **Status Indicator**. There are various actions that can lead to loss of synchronization. Check the sync loss every time you make changes to the instrument.

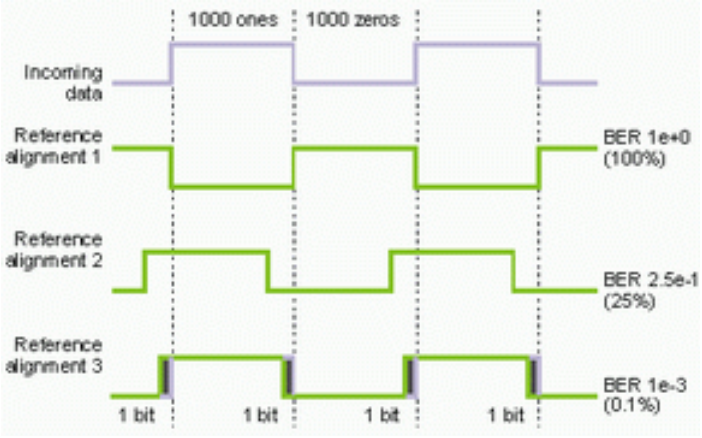
What is False Synchronization?

For patterns other than PRBS, the **Analyzer** may gain sync at a point in the pattern that meets the sync threshold, but is not the correct point where the internal reference pattern and the received data pattern match. This is called false synchronization.

NOTE False synchronization cannot occur with PRBS patterns because a 1 bit misalignment would cause a measurement of 50% or more errors. Thus, the BER during a misalignment would always be greater than the sync threshold BER.

For example, consider a pattern of 1000 ones and 1000 zeros as shown in the following figure. With reference alignment 1 the patterns are totally out of phase and the Analyzer is measuring 100% errors.

But as the reference moves closer to optimum alignment, the percentage of errors gradually approaches zero (reference alignment 2 and 3). For exact alignment, the sync threshold must be set lower than the BER caused by a 1 bit misalignment, in this case 1E-3.

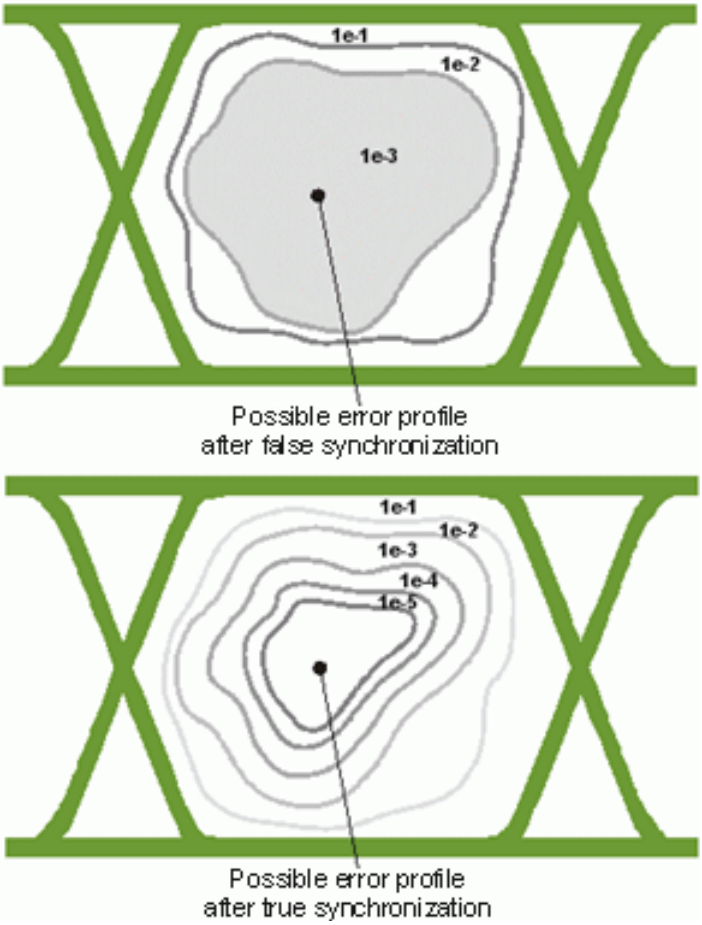


How Can You Tell if Your Synchronization is False?

You may suspect false synchronization under the following conditions:

- You are using a pattern other than PRBS and the Analyzer gains sync, but it measures a constant, fixed error ratio.
- You are using a pattern other than PRBS and the Analyzer gains sync, but auto-search functions (Auto Align, Clock/Data Center, Threshold Center) repeatedly fail.

  In a false sync, the sync threshold BER of 1E-3 may be met, but eye edges at BER 1E-3 (required by an auto-search function) may not be found. This is because BERs less than 1E-3 do not exist within the data eye.



If you suspect a false sync, try re-synchronizing at a sync threshold BER lower than the fixed error ratio. If sync is acquired without the problems listed above, then your previous sync was false. Your current sync should be on an exact pattern alignment.

NOTE While auto-search functions are in progress, the sync threshold BER is changed to the same value as the alignment BER threshold. If you are using these functions and want to consistently re-synchronize at a lower sync threshold, you must set the alignment BER threshold to the same value as the sync threshold BER.

How to Synchronize an Incoming Pattern

To synchronize the incoming pattern to the expected pattern:

1 Go to the **Menu Bar** > **Analyzer** and then select **Data In**.

2 Select the **Analyzer** function block from the **Parameters** window.

3 Select **Re-Sync**. The choices are **Automatic** or **Manual**.

- Automatic Sync

  When this option is selected, the **Analyzer** constantly tries to synchronize the patterns when the BER threshold is exceeded.

- Manual

  Manual synchronization can be selected, for example, if the signal delay is very unstable, and you want to avoid that, the resynchronization process affects the measurement results.

Bit Recovery Mode

Understanding Bit Recovery Mode (BRM)

NOTE **The M8040A analyzer (M8046A) and the M8050A analyzer (M8043A) does not support bit recovery mode.**

Traditionally, bit error rate testing compares the bits from a Device Under Test (DUT) against a reference data set, called the expected data. The user of Bit Error Ratio Tester (BERT) has to provide this expected data and load it into the M8020A.

The M8020A system then samples the incoming data signal with a sampling point that can be varied over time and voltage, to measure the BER. The M8070B system software is capable of creating graphics, such as the eye opening, from the information gathered during sampling. A compare circuit counts the differences between the bits of the incoming data stream and the expected data.

Now there is a mode that removes the need for the user to provide expected data, while still allowing one and two-dimensional measurements, such as the eye opening.

This is the Bit Recovery Mode (BRM).

This has two benefits:

- the user does not need to worry about the expected bits, which makes a setup easier and faster.
- the M8020A system can measure non-deterministic data streams. This means it is no longer necessary to force a device into a specific test mode.

Bit recovery mode uses a second sampling circuit in the M8020A analyzer to always sample at the sweet spot of the eye (typically at 50% of eye opening in time and voltage). The sampled data from this second sampling circuit acts as a reference and is passed to the compare circuitry, instead of the expected data.

This means the BER is now a relative figure. Taking the bit from the sweet spot of the eye cannot verify if this bit is correct in itself, it can just use it as a reference for any bit sampled in the border area of the eye. Bit recovery

mode makes one and two-dimensional sweeps possible to sample in the border area of the eye and find out how the BER value increases. From this we can derive the random and deterministic (Rj and Dj) characteristics.

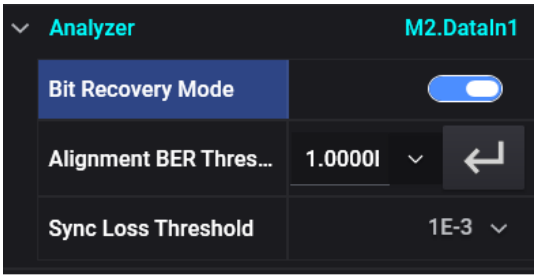
We can also take the eye opening with a known, deterministic test pattern and compare it with operational data, where a device idles or provides scrambled data, or there are asynchronous events like hand-shake signals.

The Bit Recovery mode also has a limitation that it requires a minimum eye opening: an eye that is too narrow cannot be processed. Care also needs to be taken if there is a good eye opening but there is a finite BER inside the eye.

Setting up Bit Recovery Mode

To set up the **Bit Recovery Mode** mode:

1. Go to the **Menu Bar** > **Analyzer** and then select **Data Input** or if you are in **Module View**, then click on **Data In** location.
2. Select **Analyzer** functional block from the **Parameters** window.
3. Click **Bit Recovery Mode** switch to turn on the **Bit Recovery Mode**.



NOTE The bit recovery mode can be enabled only when CDR state is on.

Once the **Bit Recovery Mode** is enabled, the BRM indicator on the **Status Indicator** turns green. See Status Indicators Window on page 158.

BRM can be used with all measurements supported by M8070B system software.

Sampling Point Setup

This section provides basic information on the sampling point setup.

How Does the Sampling Point Setup Work?

The sampling point of a data signal is defined by two values: a point in time and a voltage level. Each bit of the data signal is sampled at this point in time and in reference to this voltage level. The point in time (in reference to the clock signal) is referred to as the data input delay, and the voltage level is referred to as the threshold.

The location of the sampling point is the decision factor as to whether the incoming bits are identified as logic 0's or 1's. To measure the accurate bit error ratio at the input port, false readings of logic 0's or 1's must be avoided. Therefore, the sampling point must be set to the optimum location within the data eye.

The functions within the **Sampling Point Setup** window allow you to:

- Prepare the Analyzer for the incoming data signal regarding the connector termination.
- Adjust the location of the sampling point.

For details on **Sampling Point Setup** window, see Sampling Point Setup Window on page 547.

Auto Alignment

Use this option to automatically set the optimum sampling point.

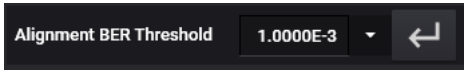
To perform the **Auto Alignment**:

1 Go to the **Menu Bar** > **Analyzer** and then select **Data In**.

2 Select **Analyzer** function block from the **Parameters** window.

3 Specify **Alignment BER Threshold** form the provided list.

4 Click **Execute** button for the align sample delay and decision threshold voltage to the received data.



5 Alternatively, you can click on **Alignment BER Threshold** button present on the Status Indicator to start BER threshold auto alignment.

This routine will not stop if the optimum sampling point cannot be found. If no optimum sampling point is found after a reasonable time, you can click **Abort**.

The following settings may affect the result of the auto align function:

- Polarity (Data Inverted)
- Threshold (BER Threshold)

NOTE When the line coding “PAM4” is selected for the loopback mode, it is recommended to adjust the pattern generator data output deemphasis for the post cursor for error free operation (e.g. +0.05 at 25 GBd).

Threshold Center Alignment

To perform the **Threshold Center Alignment**:

1 Go to the **Menu Bar** > **Analyzer** and then select **Data In**.

2 Select **Comparator** function block from the **Parameters** window.

3 Specify the **Threshold** and then click **Execute** button for the threshold center alignment.

The threshold center alignment starts an auto-search function that sets the threshold to the optimum point of the incoming data eye on the vertical voltage axis without changing the data input delay. This function can be used for determining the optimum threshold for asymmetric data eyes, or for patterns with an unequal mark density.

NOTE This function uses the alignment BER Threshold to determine the top and bottom eye edges.

Delay Center Alignment

To perform the **Delay Center Alignment**:

1. Go to the **Menu Bar** > **Analyzer** and then select **Data In**.
2. Select **Input Timings** function block from the **Parameters** window.
3. Specify the **Delay** and then click the **Execute** button to align the sample delay to the received data.

This button starts an auto-search function that aligns the data signal with the clock signal so that the **Analyzer** samples at the optimum point of the data eye in the time axis. This automatically compensates for delays in the clock/data paths, preventing unnecessary errors. The decision threshold is not changed.

NOTE Ensure that the received clock frequency is stable before using Data Center.

NOTE The clock/data alignment process time is pattern dependent, and with some large user patterns the alignment can take several minutes. If you encounter such a long time with a user pattern, it may be possible to first perform clock/data alignment on a pure PRBS pattern. This generally does not affect alignment accuracy, and can minimize measurement time.

This tip does not apply in cases of severe pattern dependent jitter or with devices that do not work with PRBS patterns.

NOTE This function uses the alignment BER threshold to determine the left and right eye edges.

Canceling Auto Align

Click this button to cancel the **Auto Align**, **Threshold Center**, or **Data Center** functions while they are in progress. The following parameters will be returned to their previous value or status:

- Auto Align Canceled
  - Data Delay and Threshold values returned to previous.
- Threshold Center Canceled
  - Threshold value returned to previous.
- Data Center Canceled
  - Data Delay value returned to previous.

Alignment BER Threshold

In this list, select an alignment BER threshold that is appropriate for your application.

The alignment BER threshold is the pre-defined threshold used by the **Auto Align**, **Threshold Center**, and **Data Center** functions to define the edges of the data input eye in the time and voltage axes. You may wish to change the threshold for the following reasons:

- Choosing smaller alignment BER thresholds will cause the auto-search functions to set more accurate sampling points. However, if the BER threshold is set lower than the residual BER of the measurement, the auto-search functions will fail. 1E-9 is the smallest BER threshold available.

Sampling Point Setup Window

The **Sampling Point Setup** window allows you view and then manually adjust the location of the sampling point.

It can be access though the **Menu Bar**. Go to **Menu Bar** and then click **Analyzer** > **Sampling Point Setup**. However, if you are in the **Setup View** window, you can click on the **Manual Alignment...** button to open the **Sampling Point Setup** window.

The following figure shows the sampling point setup window for M8020A system (M8041A and M8051A):

The vertical axis represents the threshold voltage value and the horizontal axis represents delay which can be used to manually adjusted the location of sampling point.

NOTE

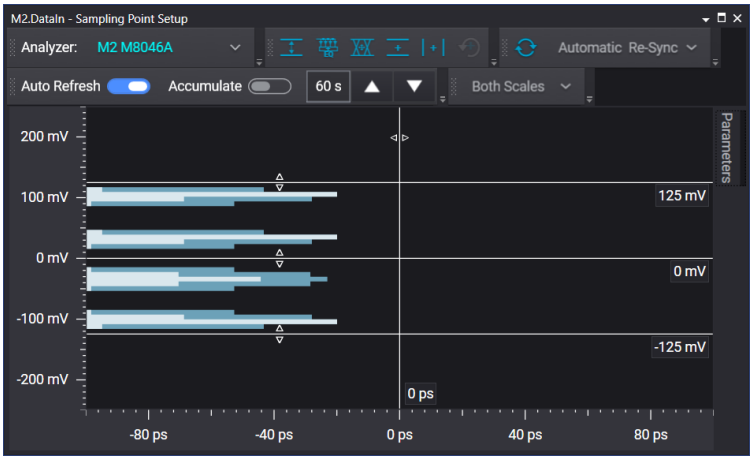
The threshold value is displayed in volts for electrical signals. In the case of an optical signal, when the probe is connected with real-time scope as ED, the graph will show the threshold value in watt.

For more information on using the N7005A Optical-to-Electrical Converter from M8070B, refer to the *M8000 Series Advance Measurement Package User Guide*.

For M8040A and M8050A systems, the **Sampling Point Setup** window display histograms which represents number of times a signal has achieved a particular threshold.

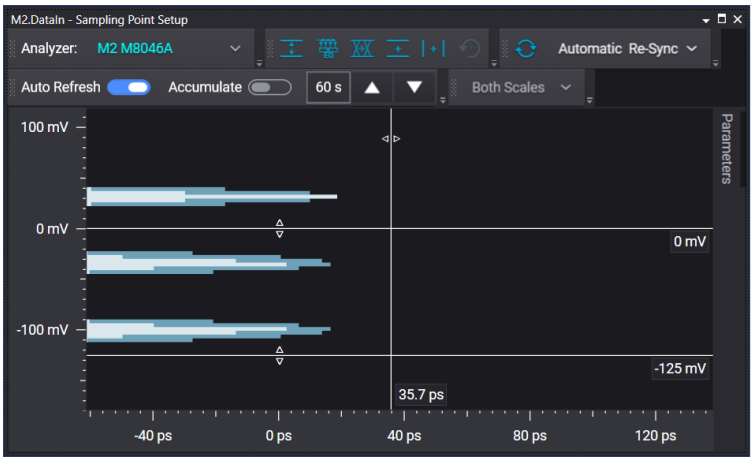
For PAM4 line coding, the **Sampling Point Setup** window shows three vertical voltage axis which represents Upper, Middle and Lower threshold value which can be used to manually adjusted the location of sampling point.

The following figure shows the **Sampling Point Setup** window displaying histograms and vertical voltage axis for PAM4 line coding:



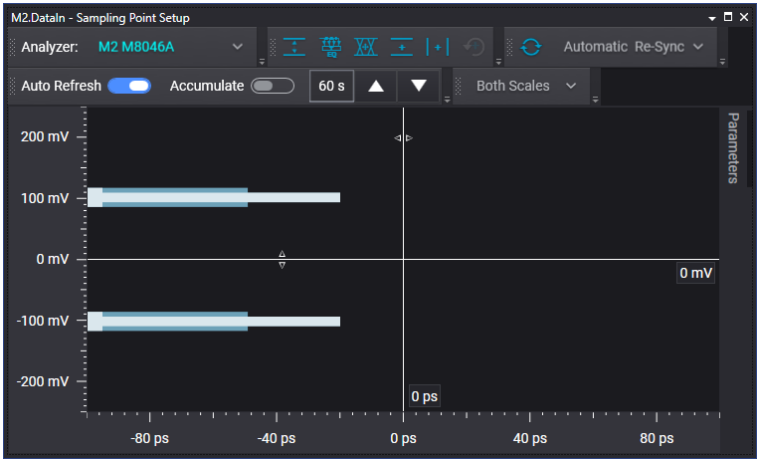
For PAM3 line coding, the **Sampling Point Setup** window shows two vertical voltage axis which represents Upper and Lower threshold value which can be used to manually adjusted the location of sampling point.

The following figure shows the **Sampling Point Setup** window displaying histograms and vertical voltage axis for PAM3 line coding:



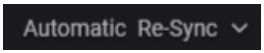
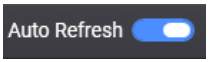
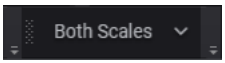
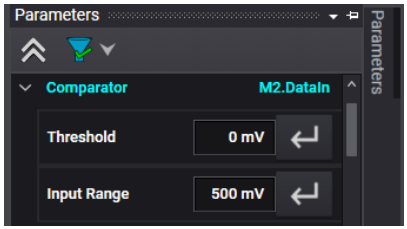
For NRZ line coding, the **Sampling Point Setup** window shows one vertical voltage axis which represents threshold value which can be used to manually adjusted the location of sampling point.

The following figure shows the **Sampling Point Setup** window displaying histograms and vertical voltage axis for NRZ line coding:



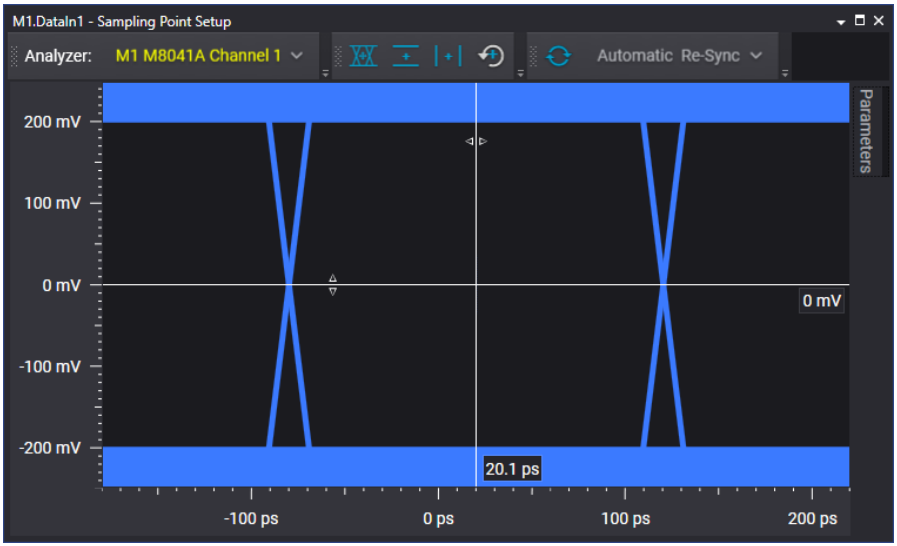
The GUI elements provided in the **Sampling Point Setup** window user interface depends on the type of selected analyzer channel. The following table describes the elements provided by the **Sampling Point Setup** window:

GUI Elements	Name	Description
Analyzer: M1 M8041A Channel 1	Select Channel	Use this drop-down list to specify the Analyzer's channel on which sampling should be done.
	Optimize Input Range	Click this button to adjust the input voltage window to match the received signal at the Data In connectors. This button is available when the sampling is done using the M8046A analyzer module.
	Optimize Equalizer Coefficients	Click this button to optimize the equalizer settings, using the current coefficient setting as a starting point. This button is available when the sampling is done using the M8046A analyzer module.
	Auto Align	Click this button to automatically set the optimum sampling point. This routine will not stop if the optimum sampling point is not found.
	Align Threshold	Click this button to start an auto-search function that sets the threshold to the optimum point of the incoming data eye on the vertical voltage axis without changing the data input delay.
	Align Data	Click this button to start an auto-search function that aligns the data signal with the clock signal so that the error detector samples at the optimum point of the data eye in the time axis. This automatically compensates for delays in the clock/data paths, preventing unnecessary errors.
	Reset Sampling Point	Click this button to return the **Threshold** and **Data Delay** to the values measured during the last auto alignment.
	Pattern Sync	Click this button to manually initiate the pattern synchronization. This is recommended whenever you did changes to the pattern setup, the voltage levels or the hardware connections (for example, altered cable lengths). Pattern synchronization is not required if it is selected as "Automatic" in the Analyzer functional block.

GUI Elements	Name	Description
	Automatic Re-Sync / Manual Re-Sync	Use this drop-down list to choose whether you want and automatic or manual synchronization. ▪ **Automatic Re-Sync** - With this option selected, the error detector constantly tries to synchronize the patterns when the BER threshold is exceeded. ▪ **Manual Re-Sync** - Manual synchronization can be selected, for example, if the signal delay is very unstable, and you want to avoid that the re-synchronization process affects the measurement results. In Manual synchronization mode use the **Pattern Sync** button to start the pattern synchronization.
	Auto Refresh	Use this toggle button to automatically refresh the histogram. This option is available when the sampling is done using the M8046A analyzer module.
	Accumulate	Use this toggle button to accumulate histogram for the specified time (in seconds). Use the up and down arrows to specify the time. This option is available when the sampling is done using the M8046A analyzer module.
	Scale	Use this drop-down list to view measured histogram of the received signal on various scales (linear, logarithmic or both). This option is available when the sampling is done using the M8046A analyzer module.
	Parameters Window	While you can manually adjust the voltage, delay values by moving the sampling point, the same can also be done through the Parameters window and vice versa. Similarly, you can also use the Parameters window to execute functions such as selecting the Equalization Mode, specifying Coefficients, Auto Align, Align Threshold, Align Data and Pattern Sync.

How to Set the Sampling Point Automatically

In most cases, you will set up the sampling point automatically. Even if you wish to make some manual adjustments, it is recommended to start with automatically aligning the sampling point. For automatically aligning, press the **Auto Align** button. It will automatically set the optimum sampling point as shown in the following figure:



For the PAM4 line coding in M8046A analyzer, it will automatically set the optimum sampling point as shown in the following figure:

How to Adjust the Sampling Point Manually

For manual adjustments, select the vertical voltage axis and move the sampling point vertically towards other location at the selected delay. The same can also be done by changing the **Threshold** value in the **Parameter** window. The **Sample Point** on the sampling diagram moves vertically as you change the value.

In case of PAM4 line coding in M8046A analyzer, there are three vertical voltage axis which represents **Upper**, **Middle** and **Lower** threshold value. You can move the sampling point vertically towards the other location at the selected delay.

The same can also be done by changing the **Upper**, **Middle** and **Lower** threshold value in the **Parameter** window.

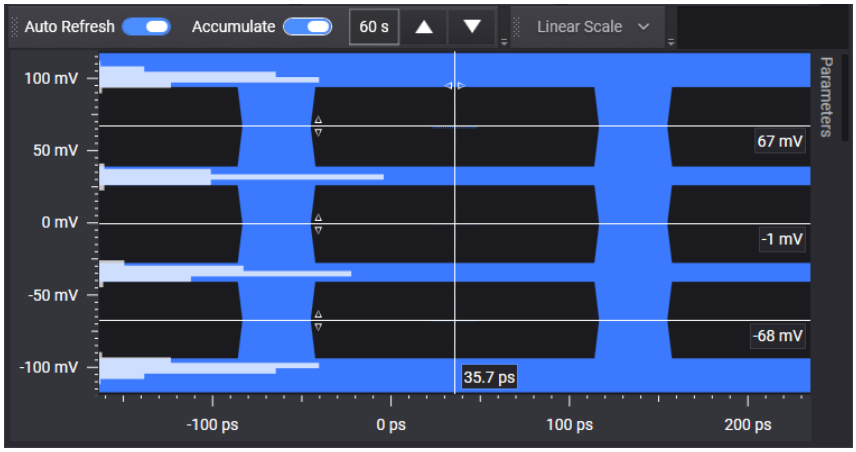
Similarly, select the horizontal axis and move the sampling point horizontally towards the other location at the selected voltage. The same can also be done by changing the **Delay** value in the **Parameter** window. The **Sample Point** in the sampling diagram moves horizontally as you change the value.

How to View Measured Histogram on Different Scales

The Sampling Point Setup allows to view the measured histogram of the received signal on different scales.

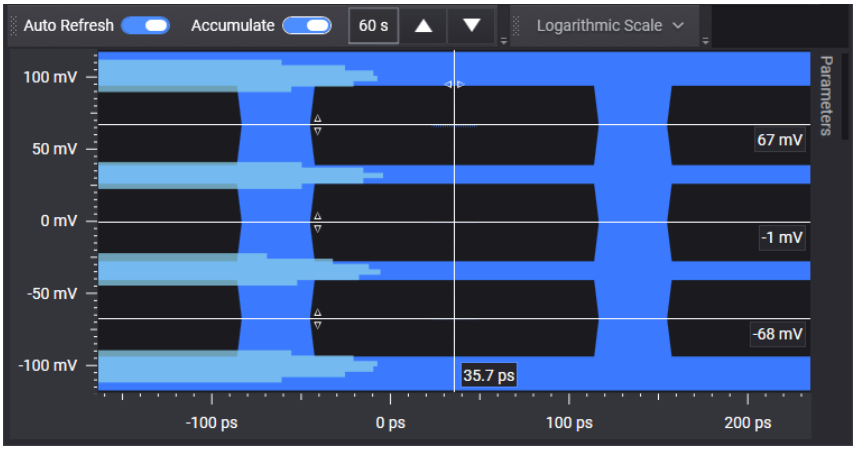
- Linear Scale

  Draws the histogram using a linear scale for the hit count.

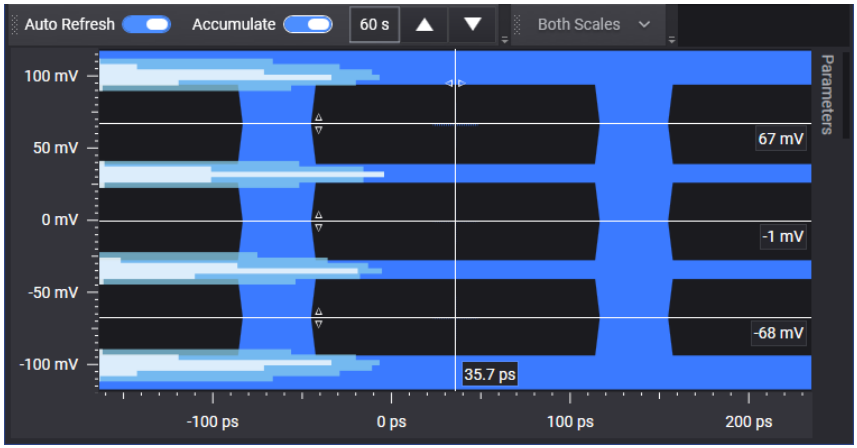


- Logarithmic Scale

  Draws the histogram using a logarithmic scale for the hit count.

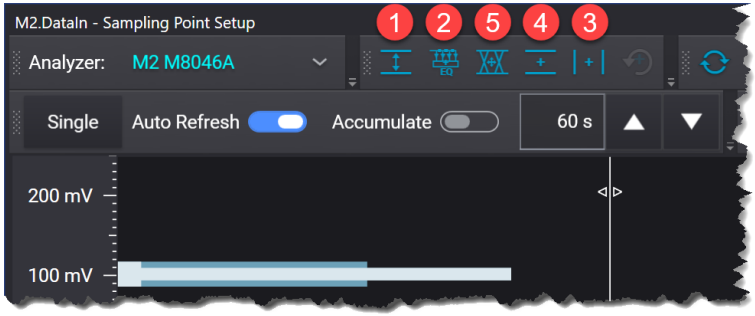


- Both Scales
  Draws the histogram twice, using both scales (linear and logarithmic).



How to Optimize BER using a Sampling Point Setup

To achieve an optimal Bit Error Ratio (BER) using the error detector modules, particularly when measuring high data rates, the below steps should be followed:



1 Input Voltage Optimization - Adjust the input voltage to accurately match the received signal at the Data In connectors.

2 Auto Equalization - Fine tune the equalizer settings, using the current coefficient values as the baseline for optimization.

3 Delay Alignment - Ensure precise alignment of delays in the clock and data paths to minimize timing-related errors.

4 Threshold Adjustment - Initiate the auto-search function to automatically set the threshold at the optimal vertical voltage point within the data eye, without altering the data input delay.

5 Auto-Alignment - Execute the auto-alignment routine to determine the best sampling point. Note that this process will continue even if the optimal point is not immediately found.

M8070ADVB Plugin support with M8043A Analyzer

Using the Advance Measurement software package, you can enable the M8043A Analyzer to generate an eye diagram of the input signal. The histogram-based approach allows:

- More frequent updates
- Display NRZ as well as PAM4 encoded signals

The eye diagram is measured using the data after the 16-tap FFE and before the slicer according to following block diagram:

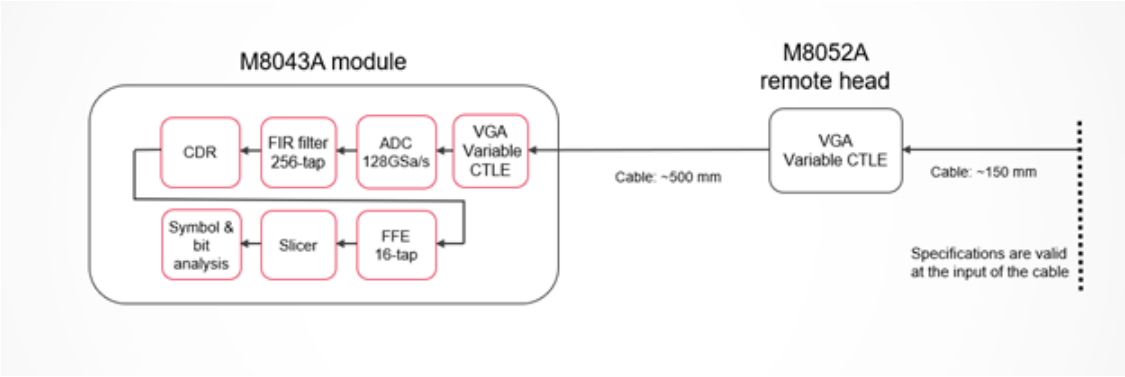
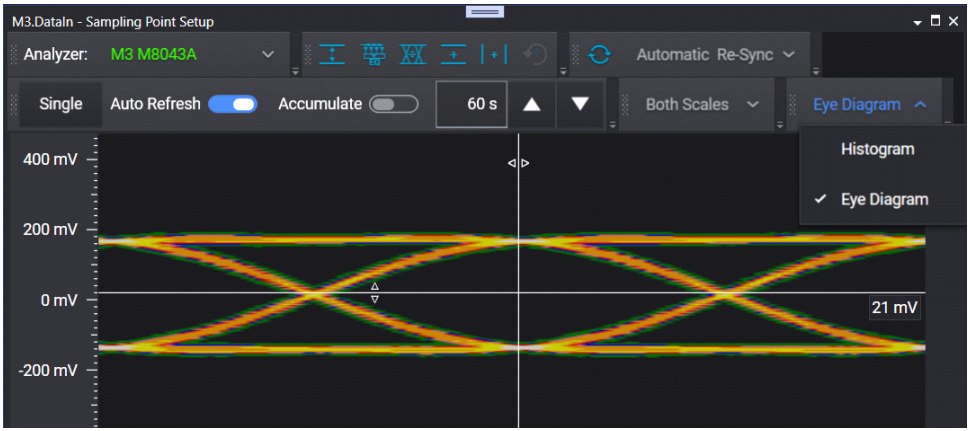


Figure 30 Block diagram of error analyzer module M8043A with M8052A remote head

NOTE Ensure that the M8070ADVB license installed in the M8070B system software to generate the Eye Diagram on the corresponding Sampling Point Setup window.

After installing the M8070ADVB license, open the **Sampling Point Setup** window in the M8043A Analyzer. A new drop-down menu is available to switch between the **Eye Diagram** and the **Histogram** features. While the Eye Diagram measurement is running, the Bit Error Counters are disabled.

The following image shows the **Sampling Point Setup** window with the menu option to toggle between the **Eye Diagram** and **Histogram** options:



For details on **Sampling Point Setup** window, refer to Sampling Point Setup Window on page 547.

Line Coding

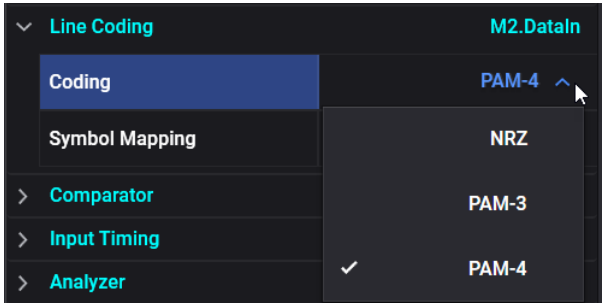
You can define the line coding for a **Data In** port of the M8043A and M8046A error analyzer modules through the **Parameters** window. The M8043A module supports NRZ and PAM4 line coding while the M8046A module supports NRZ, PAM3 and PAM4 line coding.

To set the line coding:

1 Go to the **Menu Bar** > **Generator** and then select **Data In**.

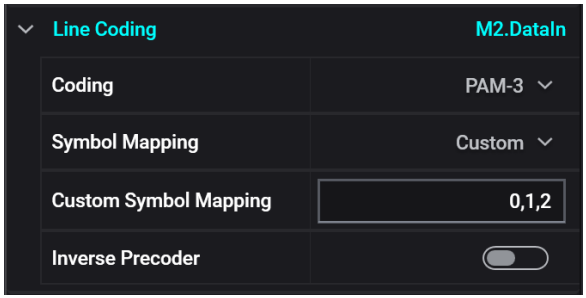
2 Select **Line Coding** functional block from the **Parameters** pane.

3 Select the line coding. The **Data In** port supports **NRZ**, **PAM3** and **PAM4** line coding.



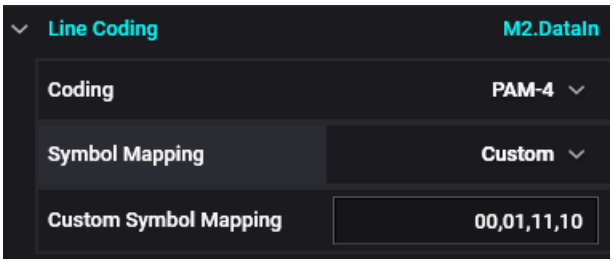
The **PAM3** line coding provides the following symbol mapping options:

- **Uncoded** - In this mapping, the bit sequence 00 maps to symbol 0, 01 maps to symbol 1 and 10 maps to symbol 2.
- **Custom** - In this mapping the consecutive data bits are mapped to symbols. The mapping is defined as a comma separated list of symbols (e.g. 0, 1, 2). The position within this list corresponds to the symbol level. First value is for Symbol 0 and the last value is for Symbol 2.
- **Inverse Precoder** - This option allows you to enable or disable the inverse precoder for PAM3 line coding.



The **PAM4** line coding provides the following symbol mapping options:

- **Uncoded** - In this mapping, the bit sequence 00 maps to symbol 0, 01 maps to symbol 1, 10 maps to symbol 2 and 11 maps to symbol 3.
- **Gray Coded** - In this mapping, the bit sequence 00 maps to symbol 0, 01 maps to symbol 1, 11 maps to symbol 2 and 10 maps to symbol 3.
- **Custom** - In this mapping the consecutive data bits are mapped to symbols. The mapping is defined as a comma separated list of bit sequences (e.g. 00, 01, 11, 10). The position within this list corresponds to the symbol level. First value is for Symbol 0 an the last value is for Symbol 3.



Error Event Mode

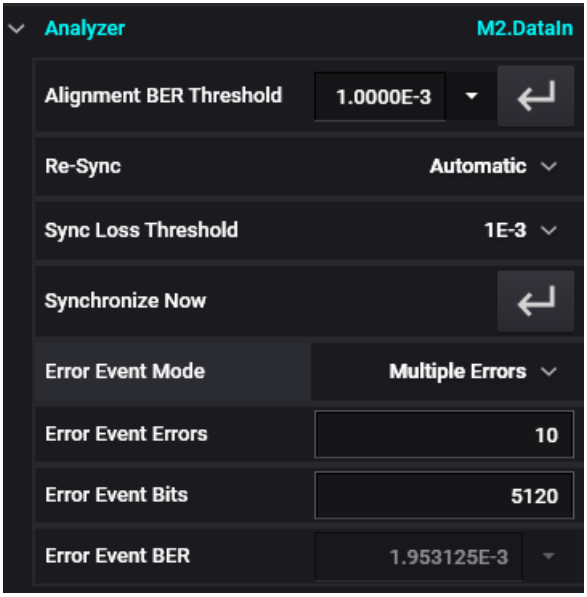
The Error Event Mode controls how detected errors are reported. Errors are detected within the sequence granularity of the error detector. For M8043A and M8046A, this granularity is 512 bits.

The error detector is capable of reporting the first detected error immediately, or of reporting the nth error with an adjustable number of observed bits.

This feature is supported by M8046A and M8043A analyzers.

The error event can be used to do the following:

- Control the branching within the pattern sequence.
- Provide an error trigger at Ctrl Out A.
- Trigger the pattern capture on either the first error or if the error rate exceeds the defined condition.



The following parameters are available:

- **Error Event Mode** - Controls how the detected errors are reported. The following options are available:

- **Single Error** - Selecting this option enables the triggering of data capture after a single error is found.
- **Multiple Error** - Selecting this option enables the triggering of data capture after it fulfills the below requirements.
  - **Error Event Errors** - Defines the number of errors that causes the generation of the error event.
  - **Error Event Bits** - Defines the number of bits that defines the reporting interval. The error event will be generated at the end of the interval. The length of the reporting interval must be a multiple of the sequence granularity (512 bits for M8043A and M8046A).
  - **Error Event BER** - Reports the Bit Error Ratio that corresponds configured number of errored bits for the error event generation. This field is not editable.

Alignment Results

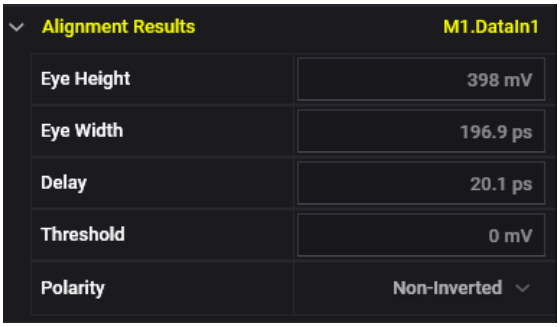
Alignment Results for M8020A/M8040A

The alignment results are the output of auto alignment. These results are displayed on pressing the auto-alignment button.

The following alignment results are available for NRZ coding:

- **Eye Height** - Height of the eye opening
- **Eye Width** - Width of the eye opening
- **Delay** - Optimum sample delay
- **Threshold** - Optimum threshold voltage
- **Polarity** - Data polarity used for pattern synchronization

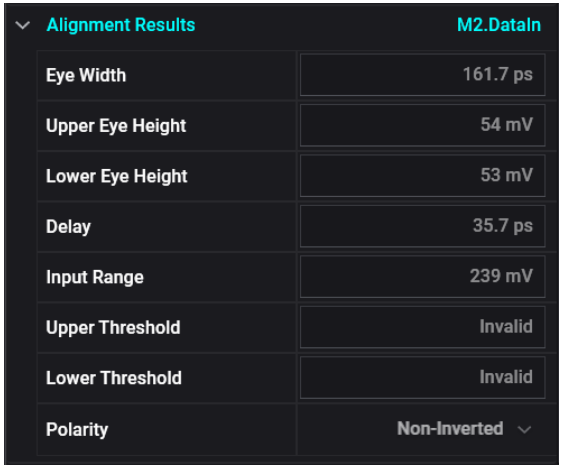
The following figure illustrates alignment results for NRZ coding:



The following alignment results are available for PAM3 coding:

- **Eye Width** - Width of the eye opening
- **Upper Eye Height** – Height of the upper eye opening
- **Lower Eye Height** - Width of the lower eye opening
- **Delay** - Optimum sample delay
- **Input Range** - Input voltage range
- **Upper Threshold** - Upper PAM3 decision threshold
- **Lower Threshold** - Lower PAM3 decision threshold
- **Polarity** - Data polarity used for pattern synchronization

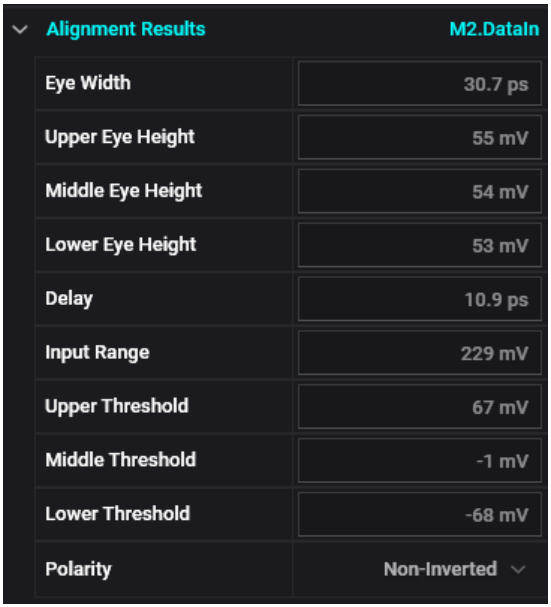
The following figure illustrates alignment results for PAM3 coding:



The following alignment results are available for PAM4 coding:

- **Eye Width** - Width of the eye opening
- **Upper Threshold** - Upper PAM4 decision threshold
- **Middle Threshold** - Middle PAM4 decision threshold
- **Lower Threshold** - Lower PAM4 decision threshold
- **Delay** - Optimum sample delay
- **Polarity** - Data polarity used for pattern synchronization

The following figure illustrates alignment results for PAM4 coding:



Alignment Results for M8050A

The following M8043A analyzer alignment results are available for NRZ line coding:

- **Eye Width** - Width of the eye opening
- **Delay** - Optimum sample delay
- **Input Range** - Input voltage range
- **Threshold** - Optimum threshold voltage
- **Polarity** - Data polarity used for pattern synchronization
- **Input Range** - Input voltage range

The following figure illustrates M8043A analyzer alignment results for NRZ line coding:

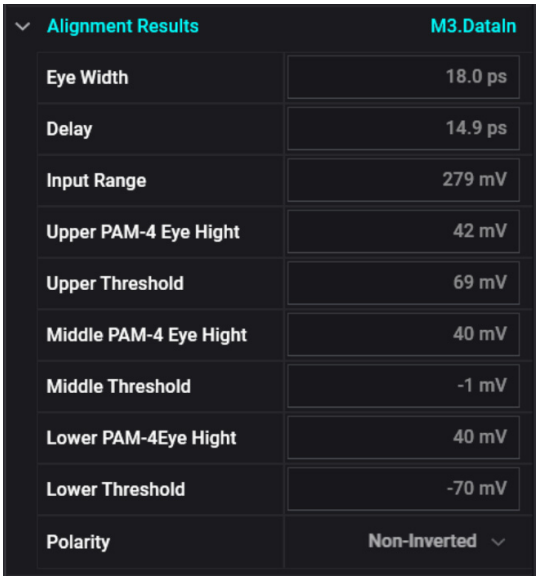
The following M8043A analyzer alignment results are available for PAM4 line coding:

The following alignment results are available for PAM4 line coding:

- **Eye Width** - Width of the eye opening
- **Delay** - Optimum sample delay
- **Input Range** - Input voltage range
- **Upper PAM4 Eye Height** - Upper height of the PAM4 eye opening
- **Upper Threshold** - Upper PAM4 decision threshold
- **Middle PAM4 Eye Height** - Middle height of the PAM4 eye opening
- **Middle Threshold** - Middle PAM4 decision threshold
- **Lower PAM4 Eye Height** - Lower height of the PAM4 eye opening

- **Lower Threshold** - Lower PAM4 decision threshold
- **Polarity** - Data polarity used for pattern synchronization
- **Input Range** - Input voltage range

The following figure illustrates M8043A analyzer alignment results for PAM4 line coding:



Alignment Results	M3.DataIn
Eye Width	18.0 ps
Delay	14.9 ps
Input Range	279 mV
Upper PAM-4 Eye Hight	42 mV
Upper Threshold	69 mV
Middle PAM-4 Eye Hight	40 mV
Middle Threshold	-1 mV
Lower PAM-4Eye Hight	40 mV
Lower Threshold	-70 mV
Polarity	Non-Inverted

Equalization

Equalization is used to correct for the problems caused by the transmission channel. Equalization techniques provide a way to discern the original signal (the signal coming out of the transmitter) given a distorted signal at the receiver.

In other words, equalization corrects for the high-frequency component voltage levels and, in the process, corrects the trajectories of these components in the corresponding eye diagram (that is, opens up the eye).

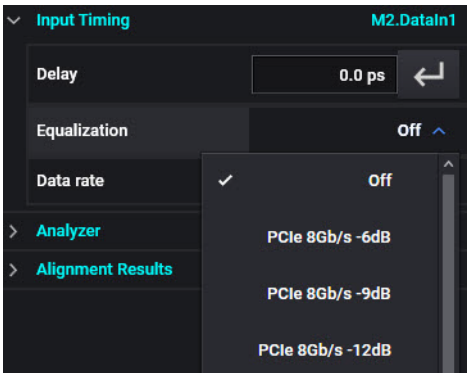
The M8070B software provides integrated and adjustable equalization capabilities to compensate the loss characteristic in an incoming signal.

Equalization in M8041A/M8051A Data In

The M8041A/M8051A Data In provides pre-defined equalization presets on incoming signals for specific applications e.g. PCIe, USB. The calibration of the equalization is only valid for these specific applications.

Follow the given steps to perform equalization in the M8041A/M8051A Data In:

1 Go to **Menu Bar** > **Analyzer** and then select **Data In**.
2 Select **Input Timing** functional block from the **Parameters** window.
3 Select the **Equalization** presets form the provided drop-down list.



NOTE The M8041A-0A3 or M8051A-0A3 license is required to enable the equalization feature in M8041A Data In or M8051A Data In, respectively.

Equalization in M8062A Data In

The M8062A Data In provides pre-defined equalization presets on incoming signals for the data rates above 20 Gb/s.

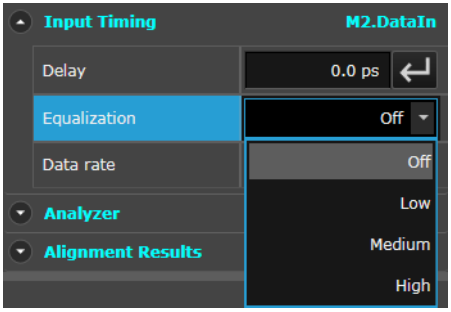
NOTE The **Equalization** option in the M8062A user interface will be enabled for the data rates above 20 Gb/s.

Follow the given steps to perform equalization in the M8062A Data In:

1 Go to **Menu Bar** > **Analyzer** and then select **Data In**.

2 Select **Input Timing** functional block from the **Parameters** window.

3 Select the **Equalization** preset form the provided drop-down list. The available equalization presets are Low, Medium or High.



NOTE The M8062A-0A3 license is required to enable the equalization feature in M8062A Data In.

Equalization in M8046A Data In

The M8046A analyzer allows you to either enter the equalizer coefficients manually or use the preset levels. The direct input of the equalizer coefficients allows fine tuning the equalizer to a degree which is not possible with the preset levels.

The following modes are available:

- Preset defined by the Equalizer Level

  This includes automatic compensation of the standard cables for either the error detector alone, or the error detector plus the additional required data cables and pick-offs in case of external clock recovery usage.
- Manual entry with cable compensation

  This mode allows the user to configure the filter coefficients manually, while still having the same automatic standard cable compensation in place that is being done in the Preset mode.
- Manual entry without cable compensation

  This mode allows the user to configure the filter coefficients manually. No cable compensation is being done. Therefore this mode can be used if the measurement setup is not using the standard cables. E.g. when using shorter cables, where the automatic cable compensation will result in overcompensating the cables even on the lowest equalization setting.

User Parameters

- Selection of equalization-mode
  - Equalizer Presets with cable compensation

    The equalizer gain is controlled as Equalizer Level, and the losses of the standard cabling is automatically included in the equalizer setting.
  - Manual coefficient entry with cable compensation

    The coefficients of the Feed Forward Equalizer can be entered manually. Additionally the losses of the standard cabling is automatically included in the equalizer setting.
  - Manual coefficient entry

    The coefficients of the Feed Forward Equalizer can be entered manually. No cable losses are automatically compensated. Use this mode when using non-standard cabling.

- FIR filter coefficients

  There are 16 filter coefficients, numbered from 0 to 15. Coefficient 2 is the main-cursor and cannot be changed.

  The available value range depends on the coefficient and is defined as follows:

  Coefficient 0: -0.25 .. + 0.25

  Coefficient 1: -0.5 .. + 0.5

  Coefficient 2: 1.0

  Coefficient 3: -0.5 .. +0.5

  Coefficient 4: -0.25 .. + 0.25

  Coefficient 5: -0.125 .. +0.125

  Coefficient 6 to 15: -0.0625 .. +0.0625

Additionally the sum of all 16 coefficients may not be 0.

User Interface for Equalization in M8046A

Preset Mode

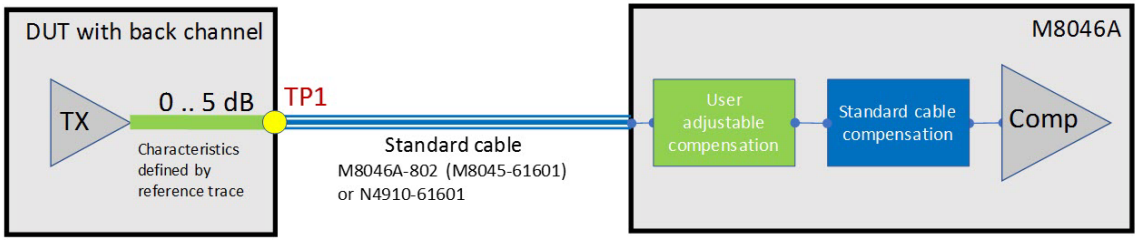
In this mode, the equalizer gain is controlled by the Equalizer Level.

This mode can be used for quick pre-configuration of the filter coefficients before starting with manual fine tuning of individual filter coefficients.

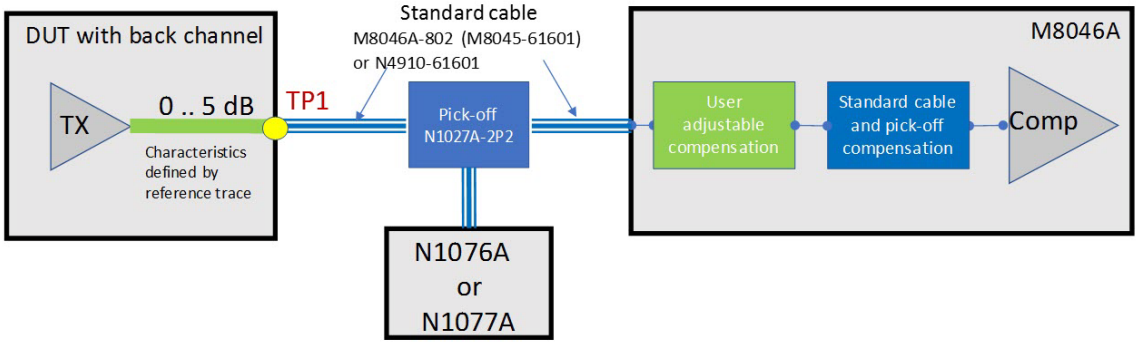
The M8046A provides integrated and adjustable equalization capabilities on the data input to compensate for the loss characteristic of the back channel. Equalization can be adjusted from no equalization (0) to maximum equalization (120) in equidistant steps. This feature is available for NRZ and PAM4 signals and requires M8070B software 4.0 or higher.

The equalization is always automatically compensating the required reference cables (M8046A-802 or N4910A). This applies also when an external clock recovery N1076A/N1076B/N1077A/N1078A is used for the recommended pick-off and reference cables. It is mandatory to use the specified cables and pickoffs. Keysight recommends to use the reference cables (refer to M8040A data sheet) because other cables will lead to over/or under-compensation of the input signal.

Setup without external clock recovery



Setup with external clock recovery



NOTE After changing the equalization level, it is required to re-adjust the threshold voltages again, or use the auto-alignment to re-optimize the sample point setting.

The M8046A Error Detector provides 120 pre-defined equalization levels for NRZ signals and 55 equalization levels for PAM4 signals. These equalization levels can be adjusted on the data input to compensate for the loss characteristic of the back channel. Specifications on these equalization levels can also be found in M8040A data sheet.

Manual Mode with Cable Compensation

This mode allows configuring the filter coefficients directly. It still adds the standard cable compensation that is done in Preset mode.

NOTE Note, that the coefficients will be set to default when switching from Preset mode to Manual mode with cable compensation.

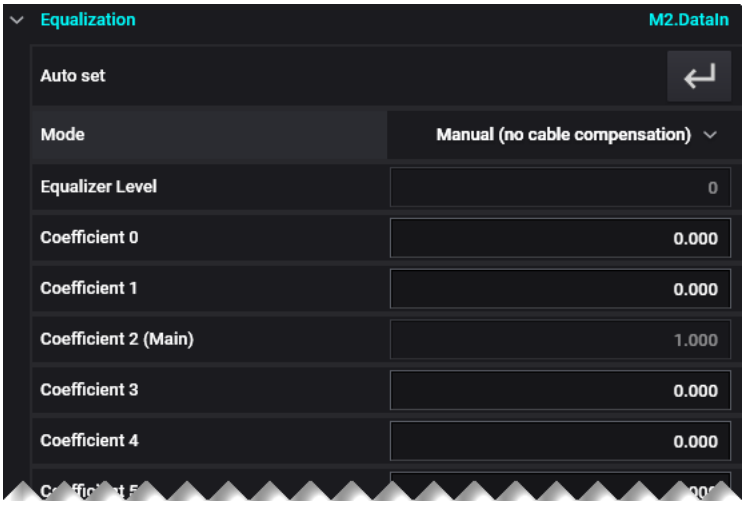
In this case the filter coefficients will include the standard cable compensation.

Manual Mode without Cable Compensation

This mode allows configuring the filter coefficients directly. No additional cable compensation is being done.

NOTE

Note that when switching from Preset mode to Manual mode without cable compensation, the filter coefficients are not cleared to default. This way, the setting of the Preset mode can be taken over and fine-tuned manually.



Automatic Equalizer Coefficient Optimization

The M8046A provides an automatic optimization of the equalizer coefficients.

The automatic optimization can only be used when the individual cursor coefficients are controllable. If the equalizer is operated in preset mode, it will automatically switch to manual mode without cable correction before starting optimizing the equalizer setting.

Precondition:

- The received signal must contain all symbol levels according to the line coding being used.
- The optimization will fail, if a PAM4 signal is only containing 2 or 3 out of the possible 4 symbol levels.
- The received signal must produce distinguishable peaks for the signal levels and at least some 'valley' between the peaks.
- The equalizer auto set function includes finding the corresponding sample delay setting. But the sample delay will be re-programmed to the initial value after the equalizer setting has been determined.
- The input range needs to be configured correctly.

  Use the Input Range auto-set function to configure the Input Range to the correct value.

When the pre-conditions are met, the equalizer auto-set can be executed. Performing the full auto-alignment after the equalizer optimization, will set the sample delay and thresholds to the best possible delay setting.

Using the equalizer auto-set

- Open the **Sample Point Setup** window.

  The individual steps can also be done from the **Parameters** window, but the **Sampling Point Setup** provides the response on the progress and display quality results of the settings.

- Press to optimize the Input Range

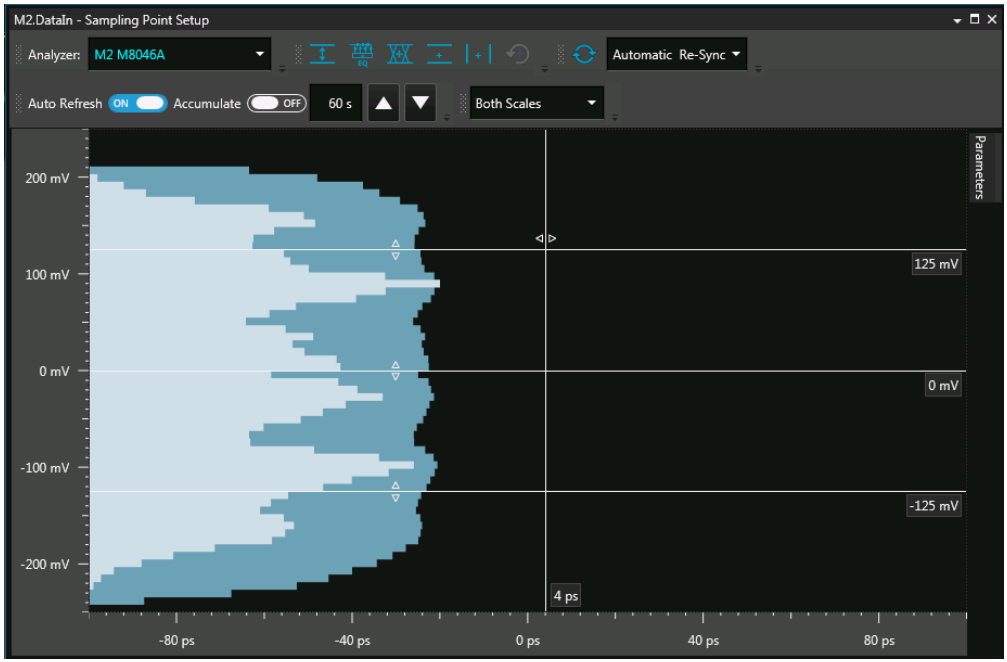
- Press to optimize the equalizer coefficients

- Press to determine the optimum sample delay and threshold settings

Manual Optimization of the Equalization Level in Preset Mode

The sampling point setup is showing histogram data of the received signal for an M8046A error detector. This can be used to determine the required equalization level.

1 Go to **Menu Bar** > **Analyzer** and then select **Sampling Point Setup**.

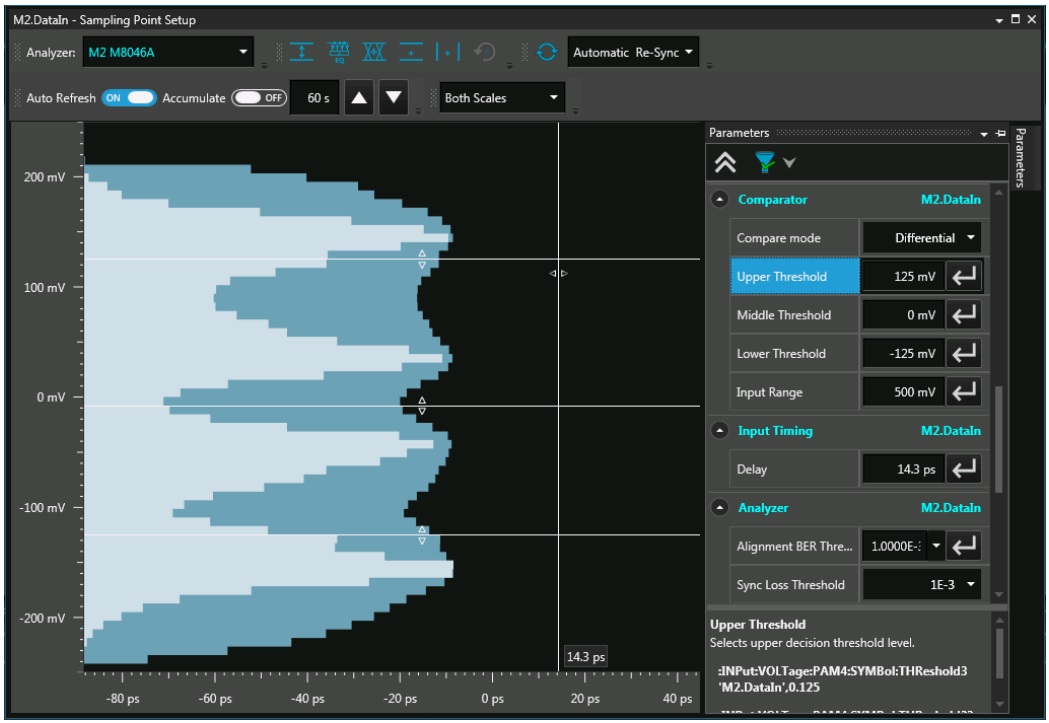


2 Click on the **Parameters** tab on the right side of the graph. Ensure that the parameters remain visible by clicking the pin at the top right corner.

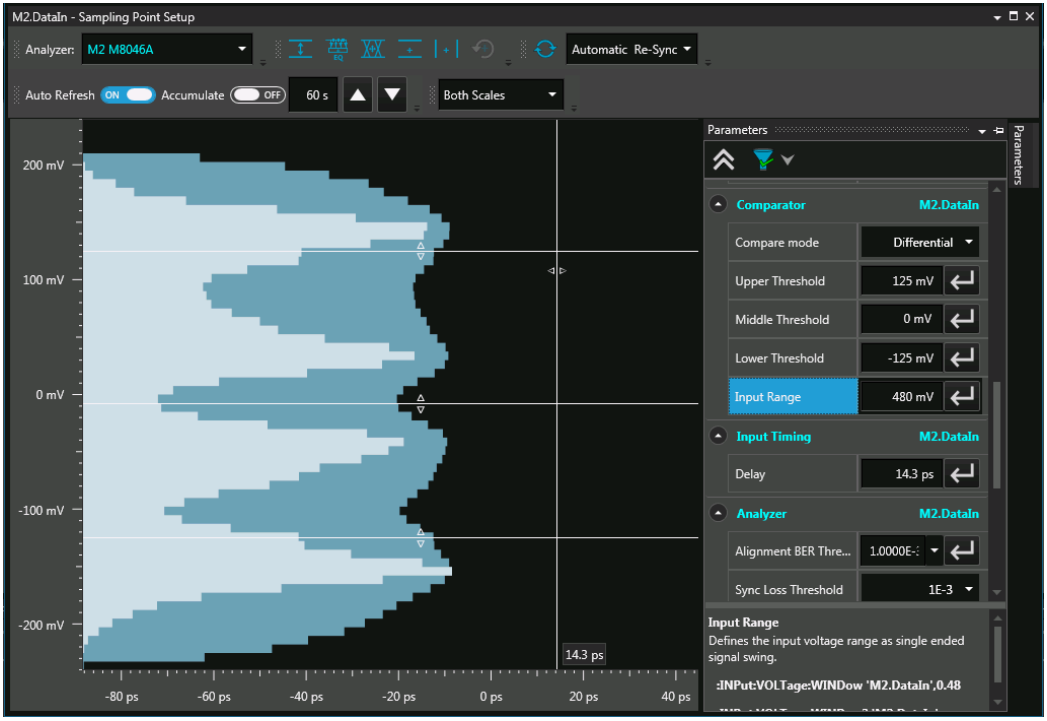
3 Start with the maximum Input range of 500 mV. This ensures that the received signal will not get clipped in the input stage.

4 Click the sample delay marker, and keep the left mouse button held down, while dragging the marker to a position that is supposed to be between the transitions of the signal. Alternatively change the sample delay setting in the parameter editor.

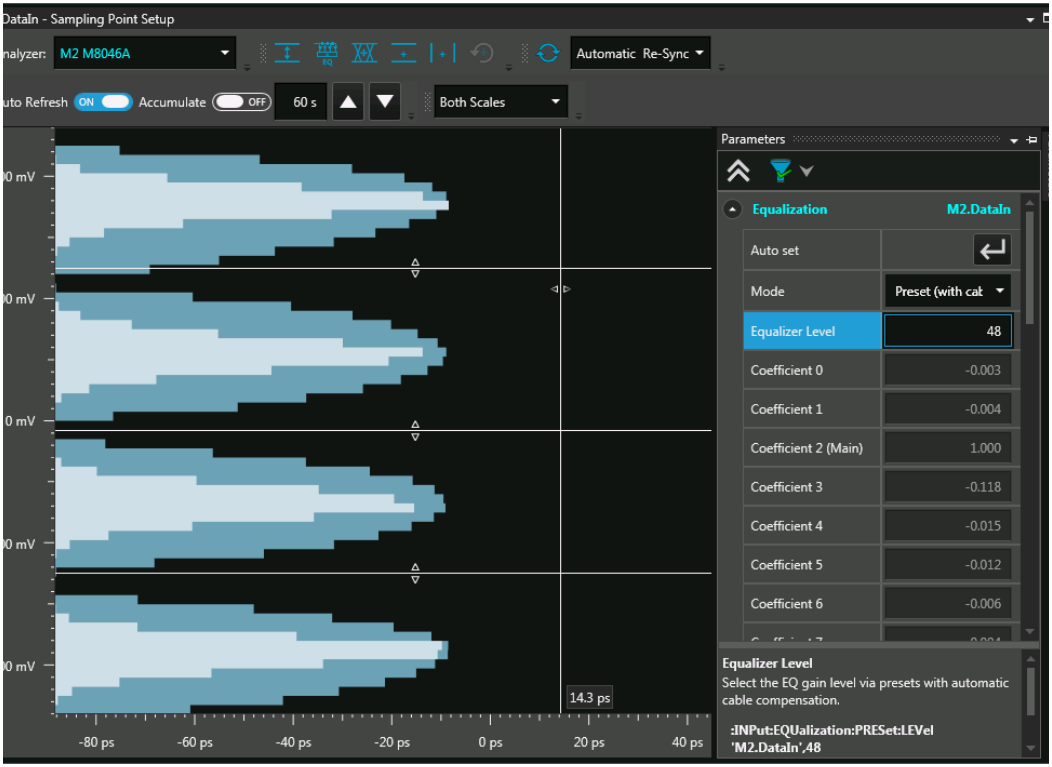
This does not have to be perfect, the goal is just not to sample at the signal transitions.



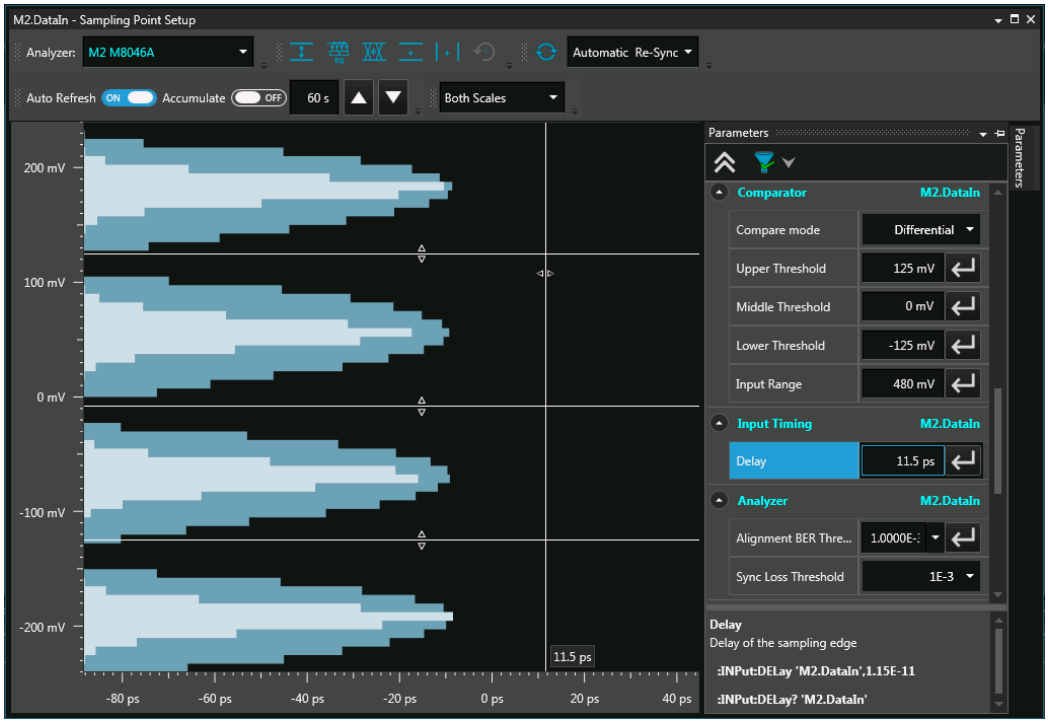
5 Adjust the input range so that the signal is using around 90 to 95 percent of the input voltage window.



6 Increase the equalization level while observing the histogram. Find the equalization level that opens the eye. This may require re-adjusting the sample delay marker.

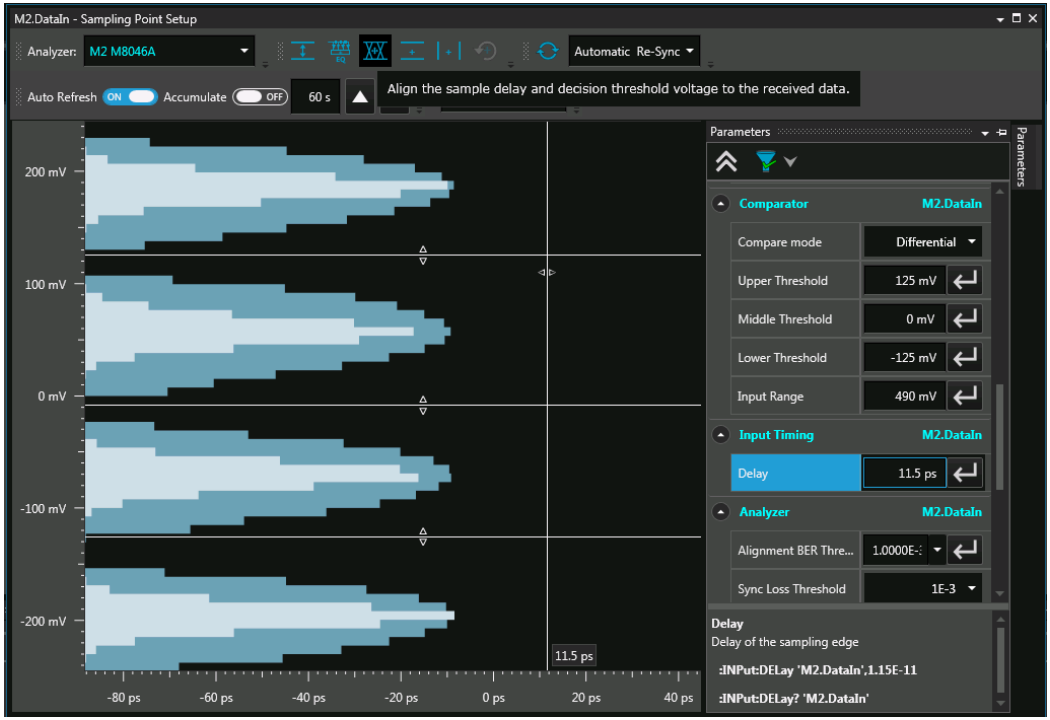


7 After manually optimizing the sample delay.

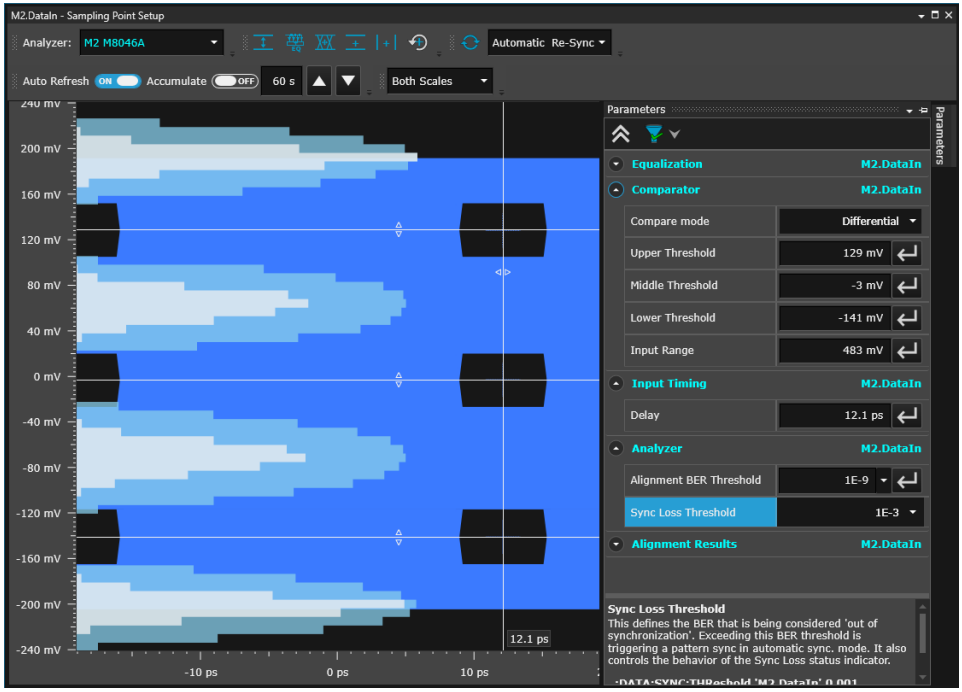


8 It may be required to iterate steps 6 and 7.

9 Finally, click the auto-alignment button.



10 In this example the received signal is a PAM4 signal with a peak amplitude of 150 mV and completely closed eyes. The auto alignment reports eye heights of 10 mV, 9 mV and 13 mV in the logger (**Utilities** > **Logger**) for an alignment BER threshold of 1e-9. At the end of the auto alignment, the sampling point setup will draw a schematic eye diagram that gives an indication of the eye opening at the configured alignment BER threshold.



The above figure shows the calculated threshold values and the black area at the sampling point shows the total eye opening achieved after applying equalization.

NOTE

The alignment BER threshold defines the BER level that is used by the auto-alignments to determine the inner eye opening as shown in the sampling point setup. The inner eye opening at the alignment BER threshold is used to calculate the optimum sample delay and threshold voltages. The lower BER alignment threshold values result in a more precise sampling point, especially when the eye opening is small. It also increases the measurement execution time.

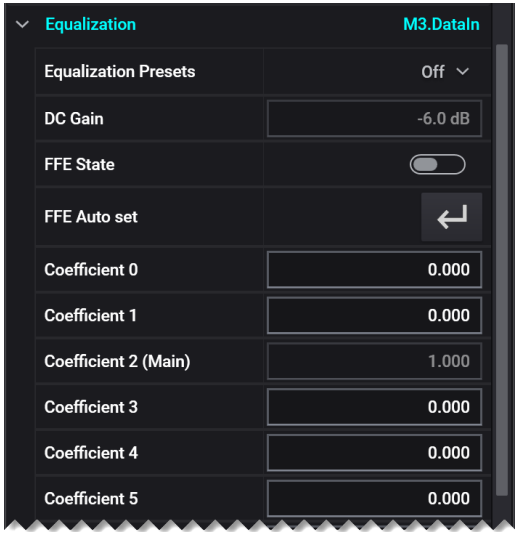
Equalization in M8043A Data In

The M8043A analyzer provides an adjustable equalization capabilities to compensate the loss characteristic in an incoming signal. To enable the equalization capability of the M8043A, the option -0A3 has to be installed. For equalization of the back channel from the DUT to the M8043A uses a combination of CTLE, a 256-tap FIR filter running at 128 GSa/s, and a 16-tap FFE (feed forward equalizer) running at the recovered symbol rate.

The following modes are available:

- Manual coefficient setting of the FFE.
- Automatic coefficient optimization of the FFE - Requires an input signal with random-like pattern. It's an iterative procedure to minimize BER.
- Presets. Affects combination of CTLE and FIR filter. The following pre-configured settings are available:
  - PCIe 8Gb/s (-12 dB to -6 dB)
  - PCIe 16Gb/s (-12 dB to -6 dB)
  - PCIe 32Gb/s (-15 dB to -5 dB)
  - PCIe 64Gb/s (-15 dB to -5 dB)
  - PCIe 128Gb/s (-15 dB to -5 dB)
  - CEI-112G (-12 dB to -2 dB)
  - IEEE 802.3 200Gaui-4 (-9 dB to -1 dB)

The following figure display the parameters required to set the equalization in M8043A analyzer:



User Parameters

- **Equalization Presets** - Use this option to select the input signal equalization for specific applications. The calibration of this parameter is only valid for the specific application.
- **DC Gain** - Specifies the gain for the selected preset. You can set a gain with an accuracy of 0.1 dB. The minimum and maximum gain is defined in the standard for each preset type. This parameter is only enabled if the equalization preset type is not set to OFF, that is, an equalizer preset type is selected before.
- **FFE State** - Enables or disables the FFE equalization.
- **FFE Auto Set** - When clicked, automatically determines the correct FFE coefficients for the current input signal.
- **FIR filter coefficients** - There are 16 filter coefficients, numbered from 0 to 15. Coefficient 2 is the main-cursor and cannot be changed.

  The available value range depends on the coefficient and is defined as follows:

  Coefficient 0: -0.25 .. + 0.25

  Coefficient 1: -0.5 .. + 0.5

  Coefficient 2: 1.0

  Coefficient 3: -0.5 .. +0.5

  Coefficient 4: -0.25 .. + 0.25

  Coefficient 5: -0.125 .. +0.125

  Coefficient 6 to 15: -0.0625 .. +0.0625

Additionally the sum of all 16 coefficients may not be 0.

De-Embedding

The M8043A analyzer provides de-embedding capabilities to compensate for losses in the loop-back path. To enable the de-embedding capability of the M8043A, the option -0A3 has to be installed. This section describes the functionality that is available when option -0A3 is installed.

For de-embedding the back channel from the DUT to the M8043A the M8043A uses a combination of CTLE (Continuous Time Linear Equalization) and a 256-tap FIR filter running at 128 GSa/s. The digital FIR filter offers very powerful and accurate de-embedding capability, Accuracy of FIR filter based de-embedding is limited by filter length, and resolution.

To perform the De-Embedding:

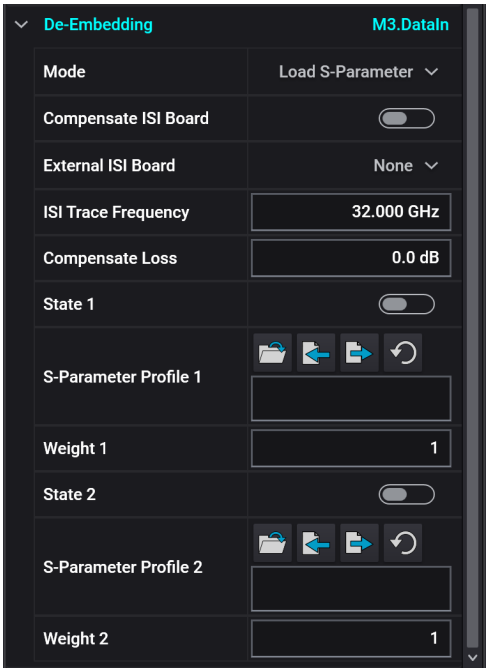
1 Go to the **Menu Bar** > **Analyzer** and then select **Data In**.

2 Select **De-Embedding** function block from the **Parameters** window.

3 Select the de-embedding mode. The available options are summarized in the following list:

- **Load S-Parameter** – Use that mode to de-embed a known channel or an ideal ISI-Trace.
- **Measure Channel Response** – Use that mode to de-embed an unknown channel by measuring the channel response of a short and known pattern signal.

4 If you select the de-embedding mode as **Load S-Parameter**, the following parameters are available:



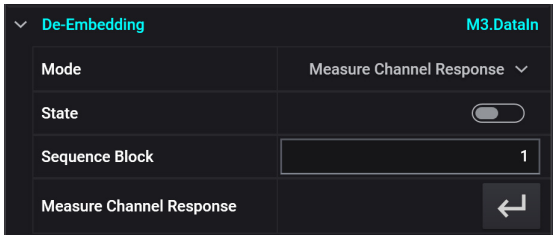
5 Specify **De-Embedding** using the provided parameters.

The required parameters are summarized in the following list:

- **Compensate ISI Board** - Use this option to enable/disable the compensation of an ISI board. You can choose one ISI Board from a drop down list or manipulate frequency and compensate loss for the selected preset or you can also use both at the same time.
- **External ISI Board** - Allows you to select the external ISI board from the drop-down list. Ensure that the external ISI board selected from this drop-down list should be connected to the hardware. If you select “None” from the drop-down list, no external ISI board will selected and the compensation of an ISI board will depend upon the specified frequency and compensation loss.
- **ISI Trace Frequency** - Defines the frequency, where the ISI board has the specified loss.
- **Compensation Loss** - Defines the attenuation of the ISI board at the specified frequency in dB.
- **State 1/2** - Enables/disables the de-embedding 1 or 2 configuration to the hardware module.

- **S-Parameter Profile 1/2** - Allows you to select the S-Parameter file (S2P, S4P) to de-embedding effect of the cable. The S-Parameter files (standard cables, ISI Boards and couplers) are available in the “Factory” folder. You can also import or export the user-defined S-Parameter file.
- **Weight 1/2** - Sets the weight for de-embedding 1 or 2.
- **Operator Output 1/2** - Selects operator output for S-Parameter profile for de-embedding 1 or 2. Note that this parameter will only be available when an S4P file is loaded in the “S-Parameter Profile 1/2”.
- **Port 1/2** - Selects port for S-Parameter profile for external ISI board for de-embedding 1 or 2. Note that this parameter will only be available when an S4P file is loaded in the “S-Parameter Profile 1/2”.

6 However, if you select the de-embedding mode as **Measure Channel Response**, the following parameters are available:



7 Specify **De-Embedding** using the provided parameters.

The required parameters are summarized in the following list:

- **State** - Enables/disables current auto-correction results.
- **Sequence Block** - Defines the block number in a sequence that includes the specified training pattern.
- **Measure Channel Response** - Automatically determines the best de-embedding setting by measuring the current channel response.

8 The sequence block with the specified training pattern must meet the following requirements:

- Min and max pattern length, which is defined in the data sheet.
- Must be a pattern signal (e.g. PRBS)
- The trainings pattern (Symbols, Line Coding, Coding) must correspond to the pattern signal, which was generated on the generator side.

RxEQ Matrix Editor

The **RxEQ Matrix Editor** enables you to either create a new RxEQ coefficient matrix or modify an existing matrix to support PCIe equalization coefficients and threshold values. It supports the PCIe speed grades from 2.5 GT/s to 64 GT/s. The **RxEQ Matrix Editor** uses the JSON file for its operation.

Launching the RxEQ Matrix Editor

To launch the **RxEQ Matrix Editor** from the M8070B application, follow one of the following procedures:

- Launching the RxEQ Matrix Editor through M8070B Menu Bar
- Launching the RxEQ Matrix Editor through M8070B Module View Parameters Window

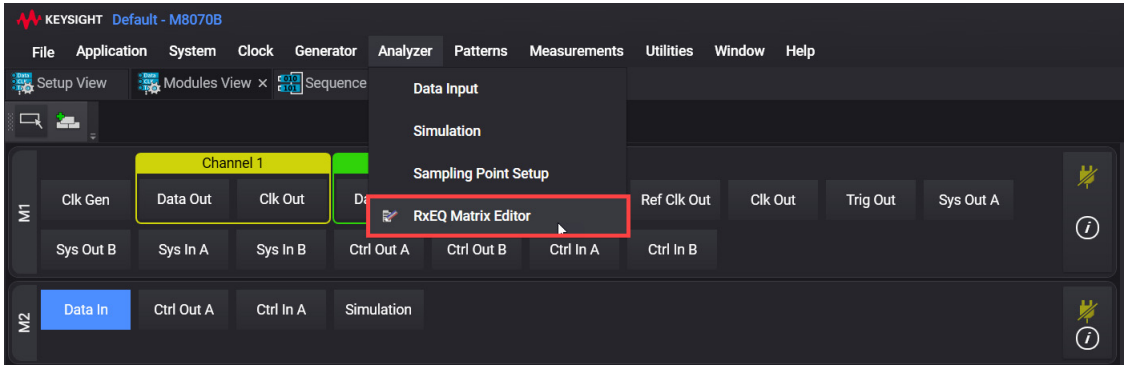
Launching the RxEQ Matrix Editor through M8070B Menu Bar

Prerequisites

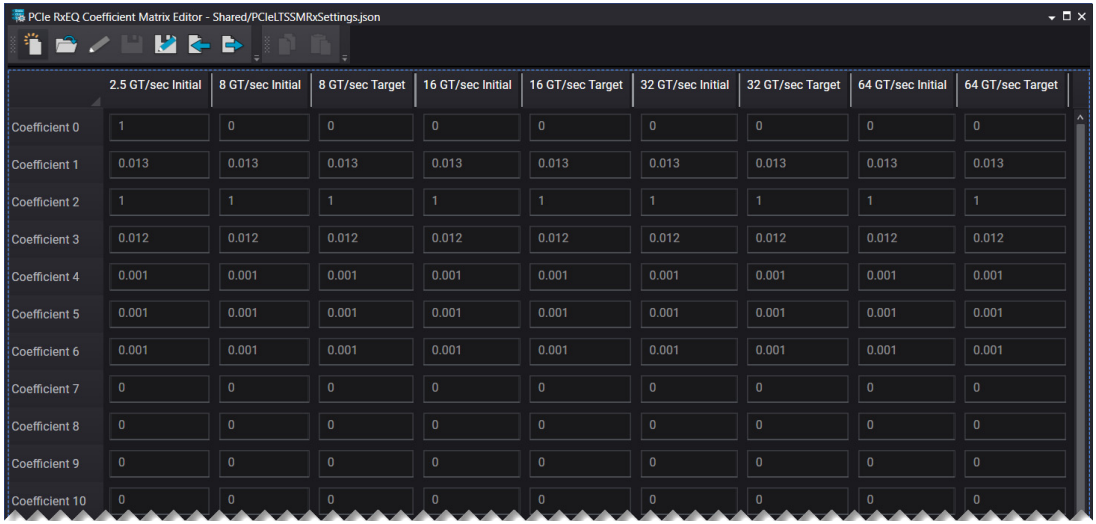
- The PG module must be connected
- The PCIe LTSSM licenses must be installed

To launch the RxEQ Matrix Editor through M8070B Menu Bar, perform the following steps:

- Go to **Menu Bar > Analyzer > RxEQ Matrix Editor**.



The **RxEQ Coefficient Matrix Editor** window appears. The PCIe RxEQ Matrix Editor title bar displays the module number and the factory file selected.



	2.5 GT/sec Initial	8 GT/sec Initial	8 GT/sec Target	16 GT/sec Initial	16 GT/sec Target	32 GT/sec Initial	32 GT/sec Target	64 GT/sec Initial	64 GT/sec Target
Coefficient 0	1	0	0	0	0	0	0	0	0
Coefficient 1	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
Coefficient 2	1	1	1	1	1	1	1	1	1
Coefficient 3	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012
Coefficient 4	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 5	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 6	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 7	0	0	0	0	0	0	0	0	0
Coefficient 8	0	0	0	0	0	0	0	0	0
Coefficient 9	0	0	0	0	0	0	0	0	0
Coefficient 10	0	0	0	0	0	0	0	0	0

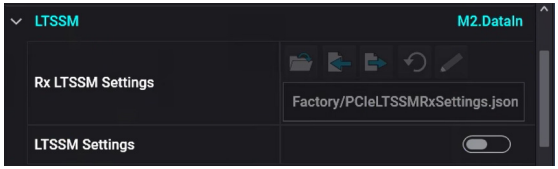
Launching the RxEQ Matrix Editor through M8070B Module View Parameters Window

Prerequisites

- The PCIe option must be selected under the PHY Protocol drop-down list in the **Sequence Configuration** parameter. For more information, refer to M8046A PHY Protocol Selection (SKP OS Filtering) on page 746

To launch the **RxEQ Matrix Editor** through M8070B Module View Parameters window, perform the following steps:

1. Load the memory using the **Select Pattern** dialog. For details, see User-Defined Sequences on page 648.
2. Open the **Sequence Editor**.
3. Download the memory pattern in the **Data In** location.
4. From the **Sequence Settings**, go to **Sequence Configuration** functional block.
5. Select the **PCIe** option under the **PHY Protocol** drop-down list.
6. Go to M8070B Module View > **Data In** > **Parameters** > **LTSSM** > **Rx LTSSM Settings**.

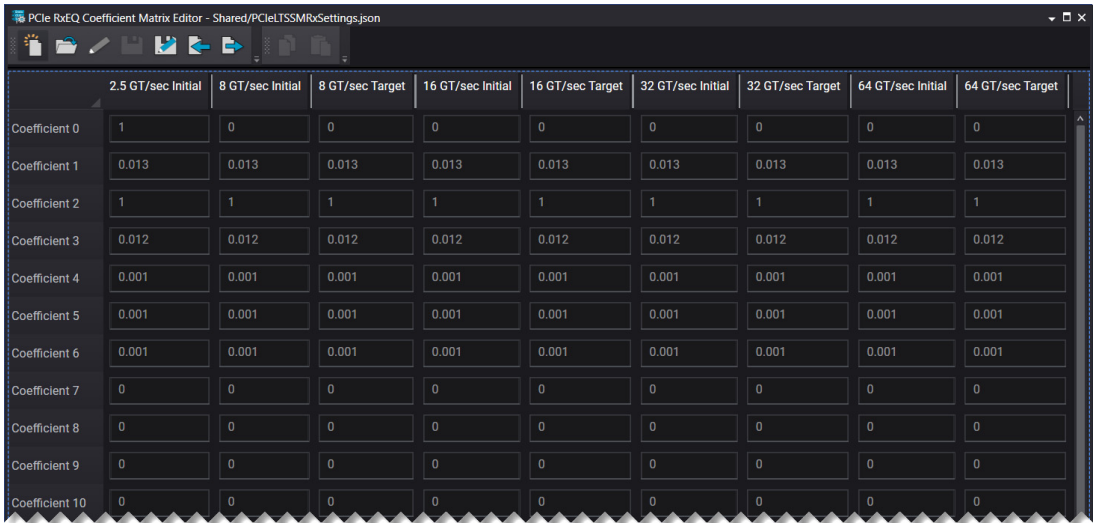


7 Click **LTSSM Settings** button to enable or disable the Rx LTSSM settings. When this option is disable, user have a user preset setting which is define under “Equalization” and “Comparator”. However, when this option is enabled, user can define 16 deferent preset setting and user can edit up to 64 GT/s.

Note that when enabling the LTSSM settings using the JSON file, you may encounter an error indicating a conflict between the threshold values and the input range. To resolve this, you can modify the input range, which will allow you to activate the **LTSSM Settings** toggle button. This error typically occurs when the threshold values specified in the JSON file exceed the input range.

8 Click the **Edit RxEQ Matrix** button.

The **PCIe RxEQ Matrix Editor** appears for the selected file. The PCIe RxEQ Matrix Editor title bar displays the module number and the factory file selected.



	2.5 GT/sec Initial	8 GT/sec Initial	8 GT/sec Target	16 GT/sec Initial	16 GT/sec Target	32 GT/sec Initial	32 GT/sec Target	64 GT/sec Initial	64 GT/sec Target
Coefficient 0	1	0	0	0	0	0	0	0	0
Coefficient 1	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
Coefficient 2	1	1	1	1	1	1	1	1	1
Coefficient 3	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012
Coefficient 4	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 5	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 6	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 7	0	0	0	0	0	0	0	0	0
Coefficient 8	0	0	0	0	0	0	0	0	0
Coefficient 9	0	0	0	0	0	0	0	0	0
Coefficient 10	0	0	0	0	0	0	0	0	0

Note that till 32 GT/s, only middle threshold will be considered, however, when PHY protocol is selected to PCIe 6 or PAM-4, all threshold 64 GT/s will be considered for link training.

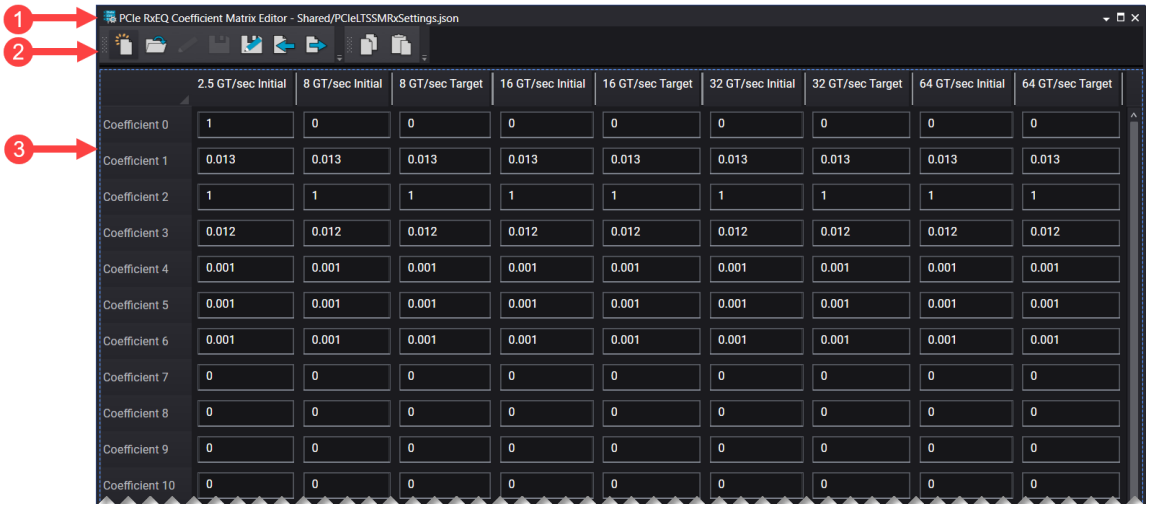
Exploring the RxEQ Matrix Editor User Interface

The **RxEQ Matrix Editor** user interface includes the following elements:

1 Title Bar

2 Menu Bar

3 Matrix Editor Pane



	2.5 GT/sec Initial	8 GT/sec Initial	8 GT/sec Target	16 GT/sec Initial	16 GT/sec Target	32 GT/sec Initial	32 GT/sec Target	64 GT/sec Initial	64 GT/sec Target
Coefficient 0	1	0	0	0	0	0	0	0	0
Coefficient 1	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
Coefficient 2	1	1	1	1	1	1	1	1	1
Coefficient 3	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012
Coefficient 4	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 5	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 6	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 7	0	0	0	0	0	0	0	0	0
Coefficient 8	0	0	0	0	0	0	0	0	0
Coefficient 9	0	0	0	0	0	0	0	0	0
Coefficient 10	0	0	0	0	0	0	0	0	0

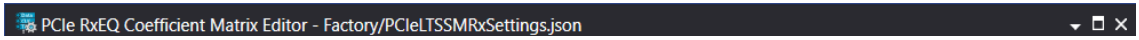
Title Bar

The title bar displays the application icon, title of the file, Options drop-down arrow, and the standard buttons to maximize or to close the window.

The **Options** drop-down arrow includes the following:

- **Close** - Closes the **RxEQ Matrix Editor** window.
- **Dock** - Docks the **RxEQ Matrix Editor** window with the other open tabs.

The title bar is shown in the following figure.



Menu Bar

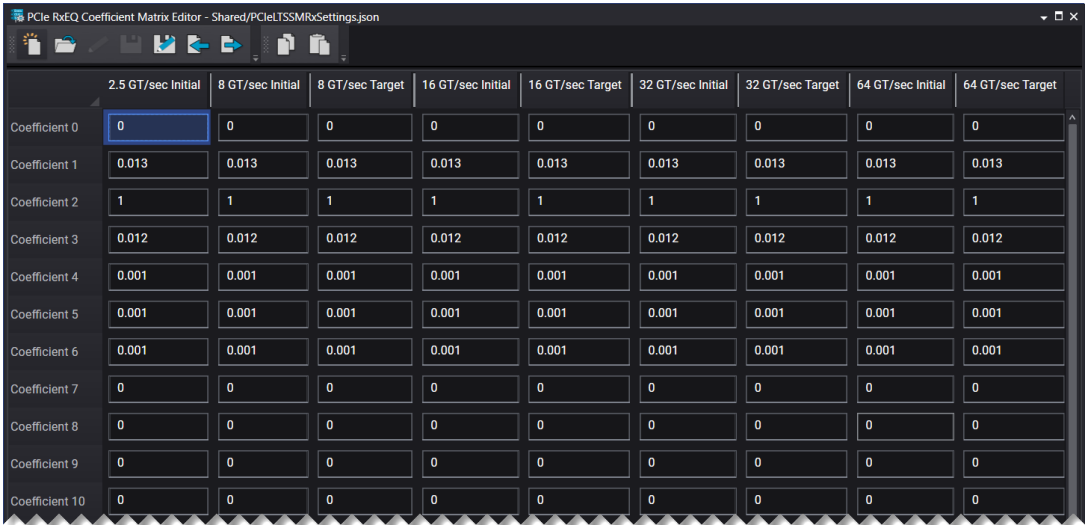
The menu bar includes the following elements:

Elements	Name	Description
	New (CTRL + N)	Allows you to create a new matrix. For more information, refer to Creating a new matrix . **NOTE**: This option is enabled only when you launch the RxEQ Matrix Editor through M8070B Menu Bar.
	Open (CTRL + O)	Allows you to open an existing file to modify/edit. On click of **Open** button, the **Open LTSSM Rx Settings** dialog box appears. For more information, refer to Opening an existing matrix . **NOTE**: This option is enabled only when you launch the RxEQ Matrix Editor through M8070B Menu Bar.
	Edit	Allows you to make changes to an existing file. For more information, refer to Editing an existing matrix .
	Save (CTRL + S)	Allows you to save the file on your local system. On click of **Save** icon, the **Save LTSSM Rx Settings** dialog box appears. **NOTE**: The Factory files cannot be saved using the **Save** option. Use **Save as** option to save any changes at different location.
	Save as (F12)	Allows you to save a copy of opened matrix to a new location. On click of **Save as** icon, the **Save LTSSM Rx Settings** dialog box appears.
	Import (CTRL + I)	Allows you to import any existing matrix file from any location to M8070B workspace to edit. On click of **Import** icon, the **Select LTSSM Rx Settings To Import** dialog box appears, which enables you to import the file. For more information, refer to Importing a matrix file . **NOTE**: This option is enabled only when you launch the RxEQ Matrix Editor through M8070B Menu Bar.
	Export (CTRL + E)	Allows you to export the current matrix to a file to any location. On click of **Export** icon, the **Export LTSSM Rx Settings File** box appears, which enables you to export the file. For more information, refer to Exporting a matrix file .
	Copy	Allows you to copy any cell from the matrix editor. This option is enabled only when any cell/value is selected in matrix editor.
	Paste	Allows you to paste any valid value from clipboard to matrix value. This option is enabled only when there is any valid data to paste in the matrix editor.

Matrix Editor Pane

The Matrix Editor pane enables you to edit any value of the opened matrix file.

The Matrix Editor pane displays the coefficient and threshold values of the PCIe speed grades from 2.5 GT/s to 64 GT/s. To edit the value of the matrix cells for the previously saved files (JSON), you need to click the **Edit RxEQ Matrix** button present on the toolbar. Once, the matrix is modified, you can save/export it. For details see Exporting a matrix file on page 609.



	2.5 GT/sec Initial	8 GT/sec Initial	8 GT/sec Target	16 GT/sec Initial	16 GT/sec Target	32 GT/sec Initial	32 GT/sec Target	64 GT/sec Initial	64 GT/sec Target
Coefficient 0	0	0	0	0	0	0	0	0	0
Coefficient 1	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
Coefficient 2	1	1	1	1	1	1	1	1	1
Coefficient 3	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012
Coefficient 4	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 5	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 6	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 7	0	0	0	0	0	0	0	0	0
Coefficient 8	0	0	0	0	0	0	0	0	0
Coefficient 9	0	0	0	0	0	0	0	0	0
Coefficient 10	0	0	0	0	0	0	0	0	0

The Matrix Editor pane includes the following features:

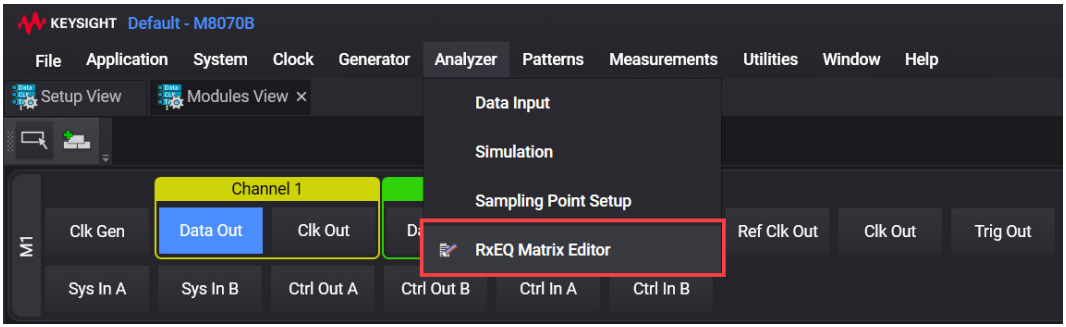
- The horizontal pane displays the coefficient and threshold values for each PCIe speed grades.
- You can use the arrow keys, ENTER, TAB, or single click to navigate to the required matrix cell. The currently selected cell is highlighted by blue borders.
- If you launch the **RxEQ Matrix Editor** through the M8070B Module View **Parameters** window, you can press CTRL + ENTER or double-click the desired cell to apply the currently selected value to the respective channel. This feature is applicable only when you are in non-editing mode and data is displayed as coefficient.

Creating a new matrix

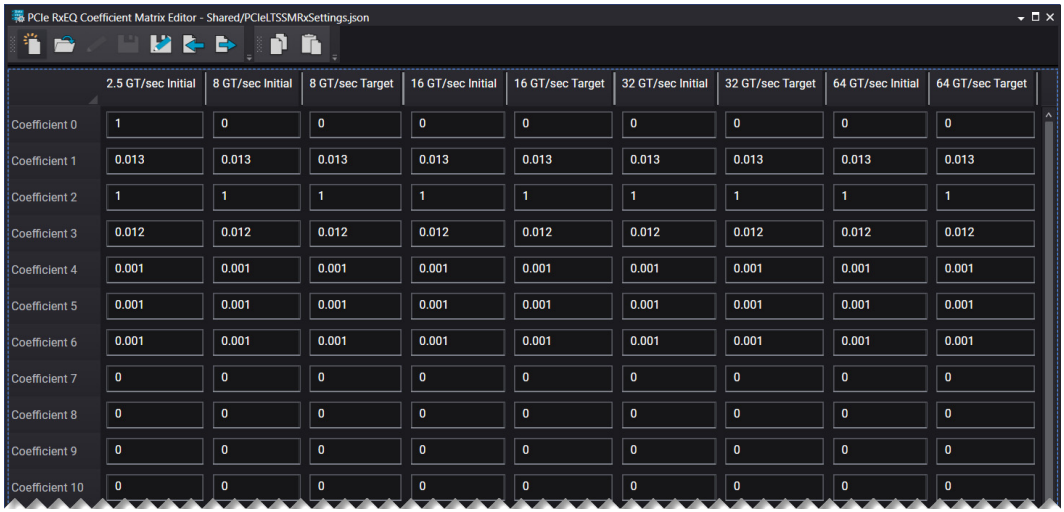
To create a new matrix, perform the following steps:

1 Go to **Menu Bar > Analyzer > RxEQ Matrix Editor**.

NOTE This option is available only when you launch the RxEQ Matrix Editor through M8070B Menu Bar.



The **PCIe RxEQ Matrix Editor** window appears.

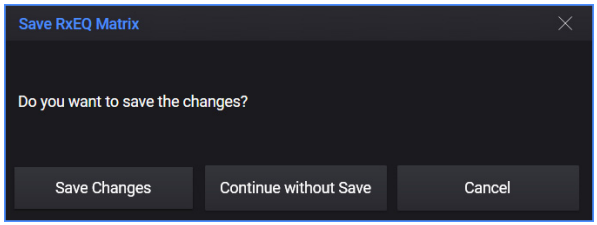


	2.5 GT/sec Initial	8 GT/sec Initial	8 GT/sec Target	16 GT/sec Initial	16 GT/sec Target	32 GT/sec Initial	32 GT/sec Target	64 GT/sec Initial	64 GT/sec Target
Coefficient 0	1	0	0	0	0	0	0	0	0
Coefficient 1	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
Coefficient 2	1	1	1	1	1	1	1	1	1
Coefficient 3	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012
Coefficient 4	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 5	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 6	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 7	0	0	0	0	0	0	0	0	0
Coefficient 8	0	0	0	0	0	0	0	0	0
Coefficient 9	0	0	0	0	0	0	0	0	0
Coefficient 10	0	0	0	0	0	0	0	0	0

It loads a default factory file showing some coefficient and threshold values of the PCIe speed grades from 2.5 GT/s to 64 GT/s. You can edit these values and later save/export this file. For details, see Editing an existing matrix on page 600 and Exporting a matrix file on page 609.

Once you modify the file, you can save the changes to a new file. To do so.

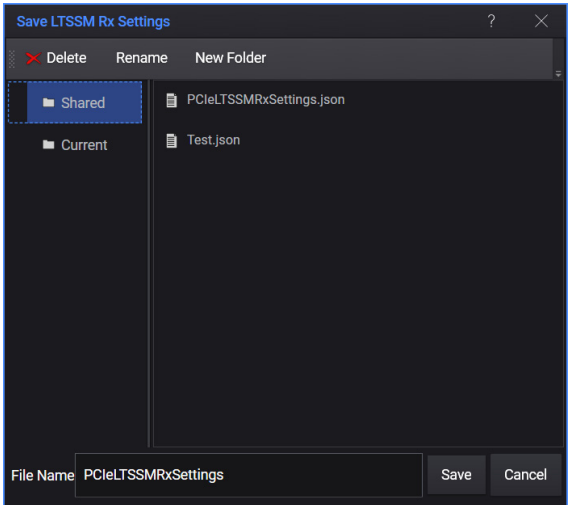
1 Click **New** button. The **Save RxEQ Matrix** dialog box appears.



The following options are available:

- **Save Changes**: Saves the changes to the file. The **Save LTSSM Rx Settings** dialog box appears.
- **Continue without Save**: Continues with the new process without saving the current file to the system.
- **Cancel**: Cancels the new process and the user remains in the editor window.

2 Click **Save Changes** option to save the matrix. The **Save LTSSM Rx Settings** dialog box appears.



3 On the **Save LTSSM Rx Settings** dialog box, do the following:

a Select a folder where you want to save the file.

By default, two folders; **Shared** and **Current** are available. Click **New Folder** to create a new folder.

b Type an appropriate name for the file in the **File Name** text box.

c Click **Save**.

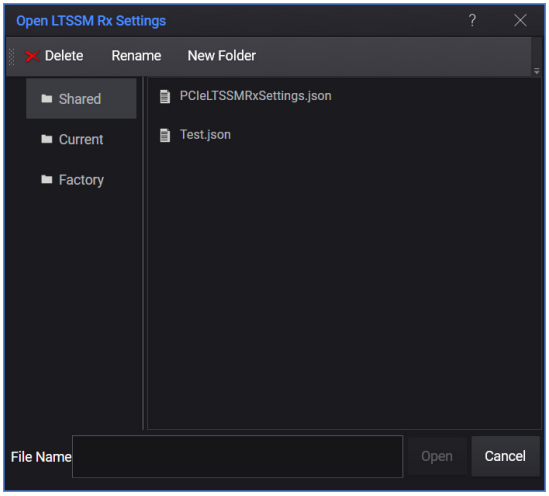
The file is saved in *JSON* format at the provided location. The PCIe RxEQ Matrix Editor title bar displays the name of the selected file.

Opening an existing matrix

To open an existing matrix, perform the following steps:

1 Launch the RxEQ Matrix Editor. For more information, refer to Launching the RxEQ Matrix Editor on page 590.

2 On the RxEQ Matrix Editor, click **Open** button present on the toolbar. The **Open LTSSM Rx Settings** dialog box appears.



3 On the **Open LTSSM Rx Settings** dialog box, select the appropriate file.

4 Click **Open**. The RxEQ Matrix Editor displays the selected file. The PCIe RxEQ Matrix Editor title bar displays the name of the selected file.

Editing an existing matrix

To edit an existing file, perform one of the following:

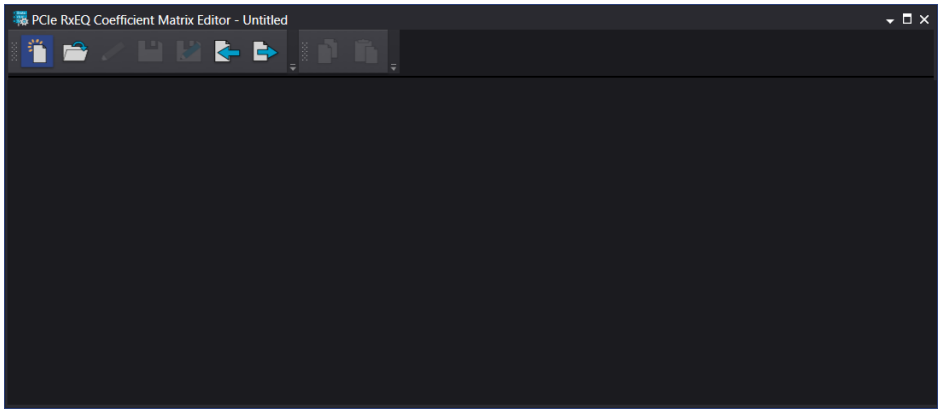
- Editing an existing file (RxEQ Matrix Editor through M8070B Menu Bar)
- Editing an existing file (RxEQ Matrix Editor through M8070B Parameters Window)

Editing an existing file (RxEQ Matrix Editor through M8070B Menu Bar)

When you launch the RxEQ Matrix Editor through M8070B menu bar, perform the following steps to edit an existing matrix.

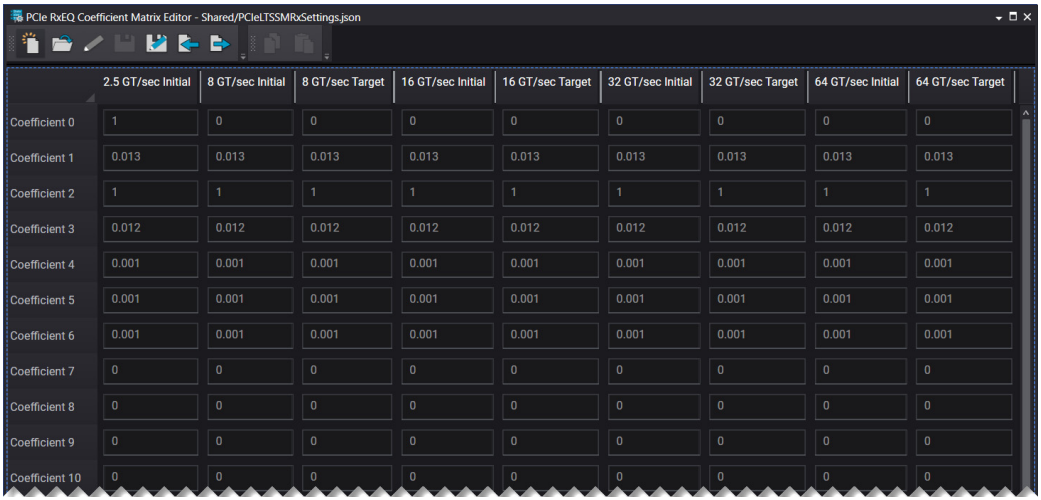
1 Go to **Menu Bar** > **Analyzer** > **RxEQ Matrix Editor**.

The **PCIe RxEQ Coefficient Matrix Editor** window appears.



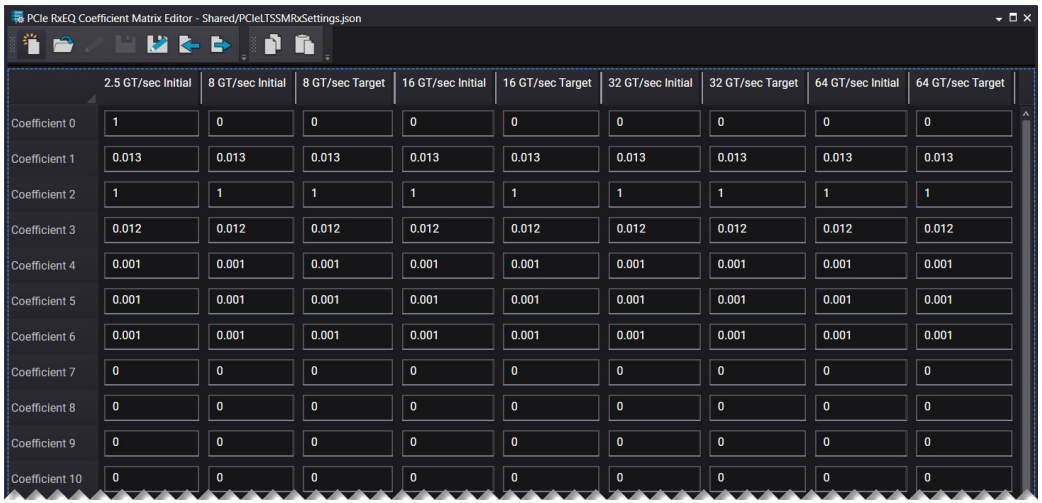
2 Click **Open** icon to open an existing file for editing. Refer to Opening an existing matrix on page 598, for more information.

The **RxEQ Matrix Editor** displays the selected file.



	2.5 GT/sec Initial	8 GT/sec Initial	8 GT/sec Target	16 GT/sec Initial	16 GT/sec Target	32 GT/sec Initial	32 GT/sec Target	64 GT/sec Initial	64 GT/sec Target
Coefficient 0	1	0	0	0	0	0	0	0	0
Coefficient 1	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
Coefficient 2	1	1	1	1	1	1	1	1	1
Coefficient 3	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012
Coefficient 4	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 5	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 6	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 7	0	0	0	0	0	0	0	0	0
Coefficient 8	0	0	0	0	0	0	0	0	0
Coefficient 9	0	0	0	0	0	0	0	0	0
Coefficient 10	0	0	0	0	0	0	0	0	0

3 On the **PCIe RxEQ Matrix Editor**, click **Edit** button.
The **PCIe Matrix Editor** enables you to edit the cell values.



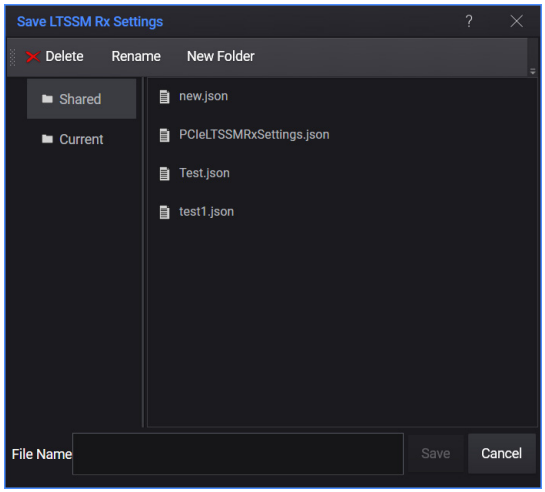
	2.5 GT/sec Initial	8 GT/sec Initial	8 GT/sec Target	16 GT/sec Initial	16 GT/sec Target	32 GT/sec Initial	32 GT/sec Target	64 GT/sec Initial	64 GT/sec Target
Coefficient 0	1	0	0	0	0	0	0	0	0
Coefficient 1	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
Coefficient 2	1	1	1	1	1	1	1	1	1
Coefficient 3	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012
Coefficient 4	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 5	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 6	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 7	0	0	0	0	0	0	0	0	0
Coefficient 8	0	0	0	0	0	0	0	0	0
Coefficient 9	0	0	0	0	0	0	0	0	0
Coefficient 10	0	0	0	0	0	0	0	0	0

The Save, Save as, Copy, Paste, and Delete icons are enabled in Edit mode. The Save option is enabled when you modify any of the cell value.

4 After all the modifications are done, do one of the following:
   - Click **Save** icon to save the file.
   - Click **Save as** icon to save the copy of the file to a new location.

NOTE The Factory files cannot be saved using the **Save** option. Use **Save as** option to save any changes at different location.

When the **Save as** option is clicked, the **Save LTSSM Rx Settings** dialog box appears.



5 (Optional) On the **Save LTSSM Rx Settings** dialog box, do the following:
   a Select a folder where you want to save the file.

   By default, two folders; Shared and Current are available. Click **New Folder** to create a new folder.
   b Type an appropriate name for the file.
   c Click **Save**.

   The file is saved at the location. The PCIe RxEQ Matrix Editor title bar displays the name of the selected file.

Editing an existing file (RxEQ Matrix Editor through M8070B Parameters Window)

To launch the RxEQ Matrix Editor through M8070B Parameters Window, perform the following steps:

1 Load the memory using the **Select Pattern** dialog. For details, see User-Defined Sequences on page 648.

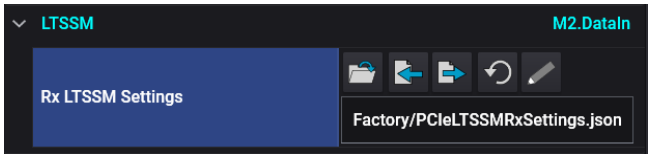
2 Open the **Sequence Editor**.

3 Download the memory pattern in the **Data In** location.

4 From the **Sequence Settings**, go to **Sequence Configuration** functional block.

5 Select the **PCIe** option under the **PHY Protocol** drop-down list.

6 Go to M8070B Module View > **Data In** > **Parameters** > **LTSSM** > **Rx LTSSM Settings**.



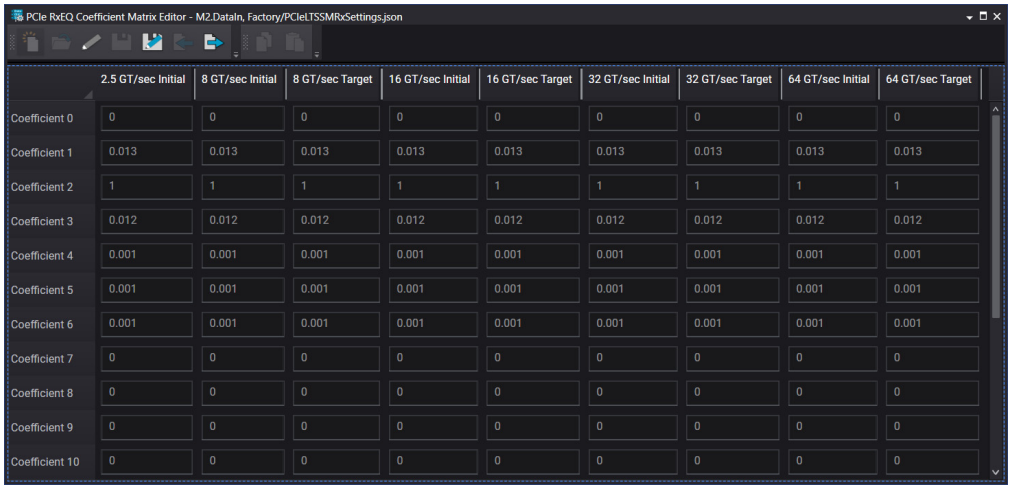
7 Click the **Edit RxEQ Matrix** button.

NOTE

When the **Edit RxEQ Matrix** button is clicked, the **Open, Import, Reset,** and **Edit RxEQ Matrix** options are disabled under the **Rx LTSSM Settings** parameter.

When the **Matrix Editor** window is closed, these options are enabled again.

The RxEQ Matrix Editor appears for the selected file. The **New**, **Open**, **Save**, **Save as**, **Import**, **Copy**, and **Paste** options are disabled.



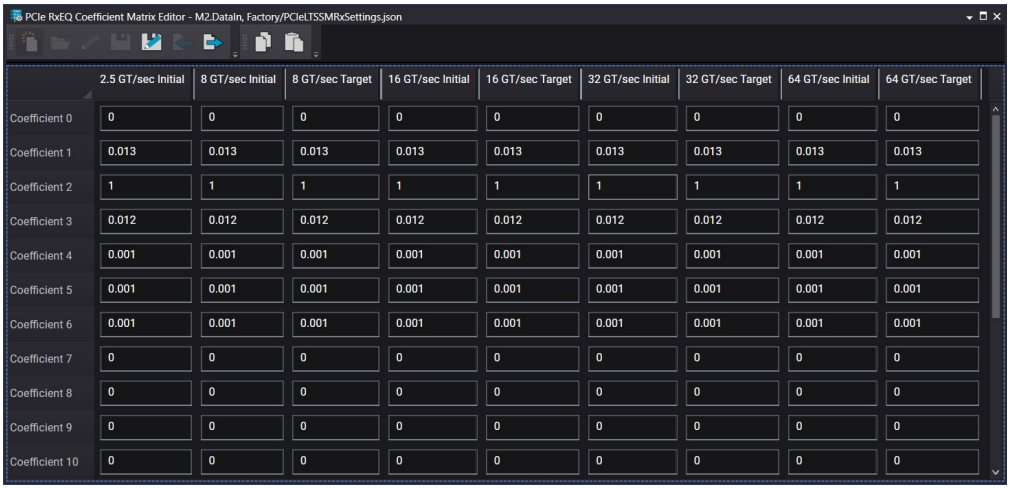
	2.5 GT/sec Initial	8 GT/sec Initial	8 GT/sec Target	16 GT/sec Initial	16 GT/sec Target	32 GT/sec Initial	32 GT/sec Target	64 GT/sec Initial	64 GT/sec Target
Coefficient 0	0	0	0	0	0	0	0	0	0
Coefficient 1	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
Coefficient 2	1	1	1	1	1	1	1	1	1
Coefficient 3	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012
Coefficient 4	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 5	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 6	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 7	0	0	0	0	0	0	0	0	0
Coefficient 8	0	0	0	0	0	0	0	0	0
Coefficient 9	0	0	0	0	0	0	0	0	0
Coefficient 10	0	0	0	0	0	0	0	0	0

NOTE

You can select another channel through the M8070B main window, even when the RxEQ Matrix Editor is already opened for a particular channel. When selected, all the buttons are enabled for this channel.

When you click the **Edit RxEQ Matrix Editor** icon for the new channel, the RxEQ Matrix Editor displays the selected file, and the PCIe RxEQ Matrix Editor title bar displays the name of the selected file.

8 On the PCIe RxEQ Matrix Editor, click **Edit** button.
The PCIe Matrix Editor enables you to edit the cell values.



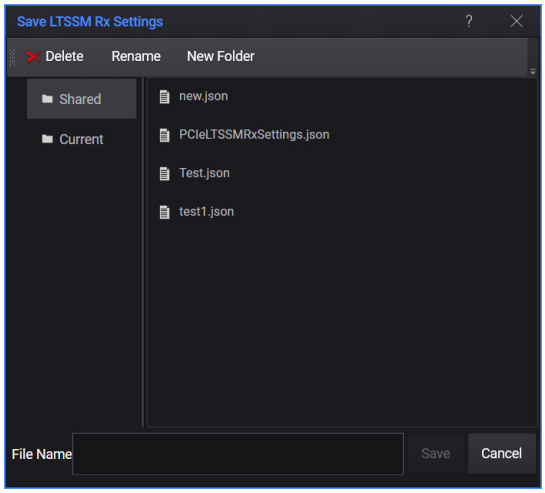
	2.5 GT/sec Initial	8 GT/sec Initial	8 GT/sec Target	16 GT/sec Initial	16 GT/sec Target	32 GT/sec Initial	32 GT/sec Target	64 GT/sec Initial	64 GT/sec Target
Coefficient 0	0	0	0	0	0	0	0	0	0
Coefficient 1	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
Coefficient 2	1	1	1	1	1	1	1	1	1
Coefficient 3	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012	0.012
Coefficient 4	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 5	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 6	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Coefficient 7	0	0	0	0	0	0	0	0	0
Coefficient 8	0	0	0	0	0	0	0	0	0
Coefficient 9	0	0	0	0	0	0	0	0	0
Coefficient 10	0	0	0	0	0	0	0	0	0

The Save, Save as, Copy, Paste, and Delete buttons are enabled in Edit mode. The Save option is enabled when you modify any of the cell value.

9 After all the modifications are done, do one of the following:
   - Click **Save** button to save the file.
   - Click **Save as** button to save the copy of the file to a new location.

NOTE The Factory files cannot be saved using the **Save** option. Use **Save as** option to save any changes at different location.

When the **Save as** option is clicked, the **Save LTSSM Rx Settings** dialog box appears.



10 (Optional) On the **Save LTSSM Rx Settings** dialog box, do the following:

a Select a folder where you want to save the file.

By default, two folders; Shared and Current are available. Click **New Folder** to create a new folder.

b Type an appropriate name for the file.

c Click **Save**.

The file is saved at the location. The **PCIe RxEQ Matrix Editor** title bar displays the name of the selected file.

Importing a matrix file

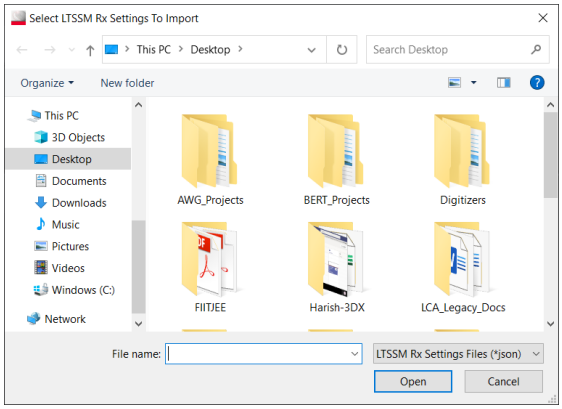
To import an existing matrix file from any location to M8070B workspace, perform the following steps:

1 Launch the RxEQ Matrix Editor through M8070B Menu Bar.

For more information, refer to Launching the RxEQ Matrix Editor through M8070B Menu Bar .

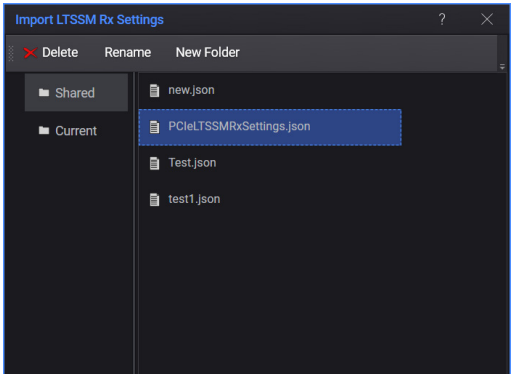
2 Click **Import** button.

The **Select LTSSM Rx Settings To Import** dialog box appears.



3 Browse the required matrix file, and then click **Open**.

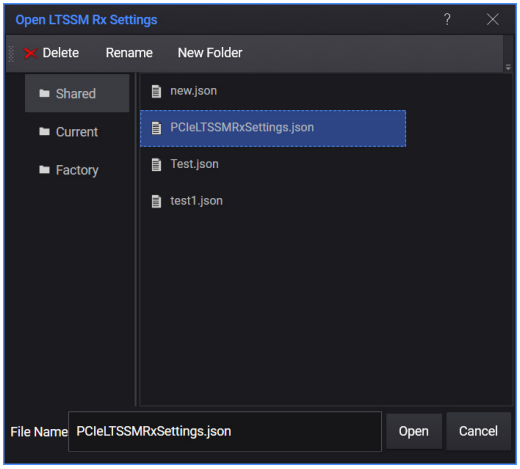
4 In the **Import LTSSM Rx Setting** dialog box, type an appropriate name in the **File Name** text box.



5 Click **Import**.

The selected file is imported successfully. The PCIe RxEQ Matrix Editor title bar displays the name of the selected file.

6 (Optional) Click **Open** button to check the imported file.



The imported file is opened in Matrix Editor.

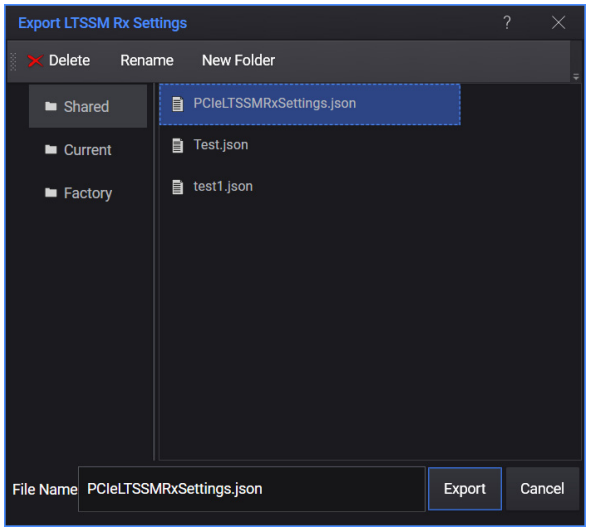
Exporting a matrix file

To export the current matrix to a file to any location, perform the following steps:

1 Launch the RxEQ Matrix Editor. For more information, refer to Launching the RxEQ Matrix Editor .

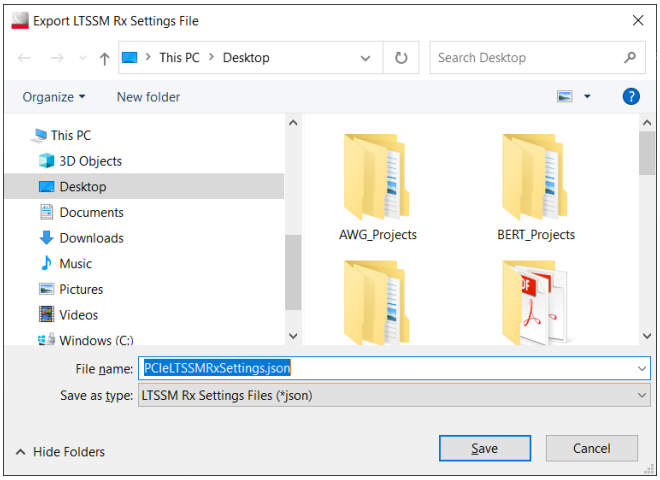
2 Click **Export** button.

The **Export LTSSM Rx Settings** dialog box appears.



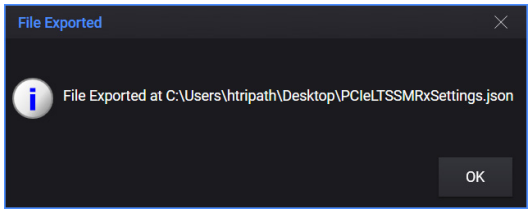
3 Select a file, and then click **Export**.

The **Export LTSSM Rx Setting File** dialog box appears.



4 Type the name of the file in the **File name** text box, and then click **Save**.

The File Exported at [Location name] message appears.



5 Click **OK**.

M8000 Series of BER Test Solutions
User Guide

7 Setting up Patterns

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Using Pattern Shift and 3b2s Mapping in M8070B / 760

KEYSIGHT TECHNOLOGIES

Pattern Overview

The purpose of data patterns is to simulate the type of data that your device might receive in the real world. Different patterns present different data loads to your instrument, which can cause variations in the bit error ratio. A bit pattern is sent from the generator to your device. At the same time, the expected output pattern of your device is internally generated in the analyzer (to provide a reference).

The M8041A and M8051A modules supports 2 Gb pattern memory per channel (requires M8070B).

The M8045A and M8046A modules support 2 Gb pattern memory per channel (requires M8070B)

Selecting a pattern is the first step in setting up a BER measurement. The M8020A provides various patterns to fulfill most standard testing needs. The M8020A modules support the following types of patterns:

- PRBS
- Pulse
- Clock
- Static
- Memory Patterns
- Squelch (Electrical Idle)

The M8040A modules support the following types of patterns:

- PRBS (supports all except for 2^7-1 on analyzer)
- Pulse (supports for NRZ, doesn't support for PAM4)
- Clock (supports for NRZ, doesn't support for PAM4)
- Static
- Memory Patterns
- Squelch (Electrical Idle)

Patterns consist of a sequence of symbols. A symbol can have the following type of coding:

- Binary (Bit)
- 8B/10B
- 128B/130B
- 128B/132B

Sequence Editor

Overview

The sequence editor allows you to create and maintain sequences. In addition to this, it also allows you to edit the memory patterns.

A sequence consists of up to 500 blocks that can be looped. Single or multiple blocks can be looped. The sum of the blocks and the counted loops must not exceed 500. An overall loop restarts the sequence after it has come to its end.

You can also upload predefined sequences for PCIe, USB and SATA using the **Recall Setting** dialog. For details, refer to Recall/Save Instrument State on page 169.

When to Use a Sequence

You may wish to test a device that uses a certain protocol for processing data.

For example, the device might expect synchronization data, a preamble, payload data, and a suffix.

All this can be provided by a user-defined sequence.

How a Sequence is Defined

The sequence is defined by a SequenceExpression which is formulated in its own language, checked by the Sequence Editor.

The SequenceExpression specifies:

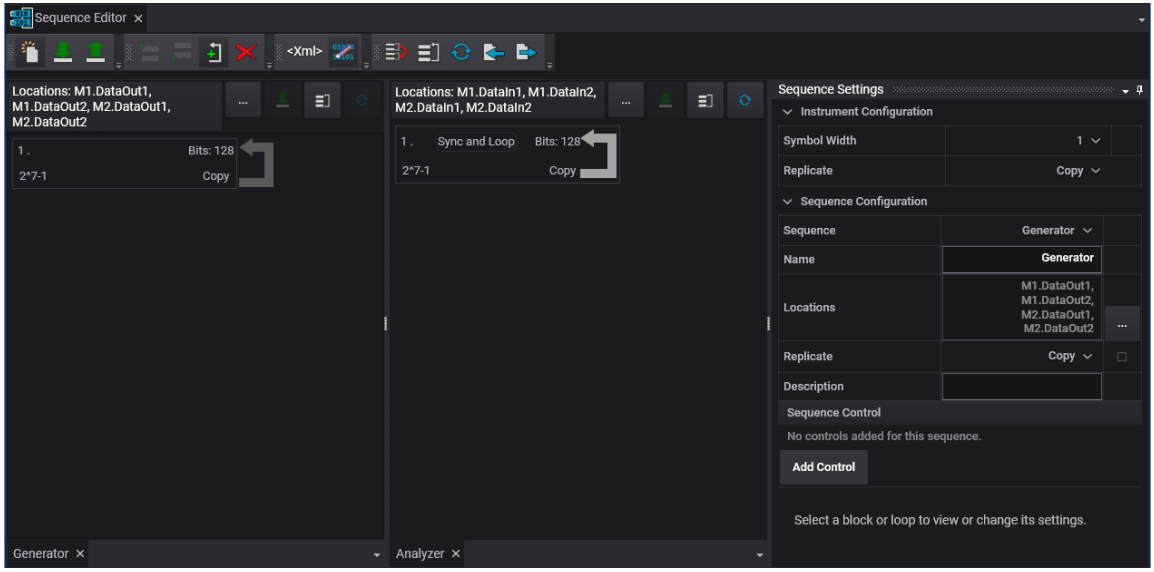
- the sequence start (and break) conditions
- the blocks, their contents, and trigger output
- the loops

How to Launch a Sequence Editor

To launch the **Sequence Editor**:

- Go to the **Menu Bar** > **Patterns** and then select **Sequence Editor**.

  The **Sequence Editor** will appear as shown in the following figure:



The **Sequence Editor** user interface includes the following elements:

- Toolbar
- Sequence Control Pane
- Sequence Settings Window
- Pattern Edit Pane

These GUI elements are described in the section that follows.

Toolbar

The toolbar provides the following convenient sequence editing functions:

Table 57

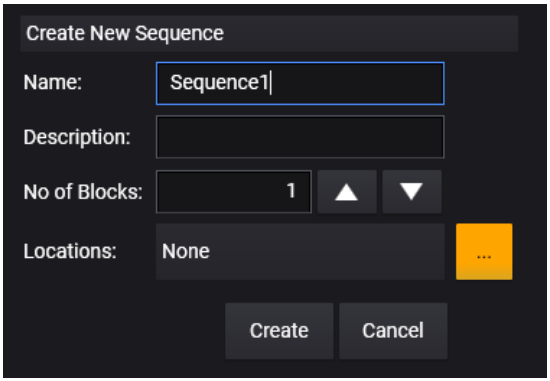
Elements	Name	Description
	New	Click this icon to create a new sequence. Refer to Creating New Sequence on page 616.
	Download	Click this icon to save the modifications that are done using the **Sequence Settings** window on the module. An orange icon indicates that modifications are not yet applied on the module. You can also apply the changes on either generator, or analyzer or both.
	Reload Running Sequence	Click this icon to reload the running sequence settings. Reloading a sequence will discard the changes made in the sequence editor and will reload the current sequence with its factory settings.
	Add Block Before	Click this icon to add a block before selected sequence block.
	Add Block After	Click this icon to add a block after selected sequence block.
	Loop	Click this icon to create a loop in a sequence block. Refer to Creating a Loop on page 619.
	Delete	Click this icon to delete the selected block from the sequence. Deleting a block will also remove all loops that are associated with this block.
<Xml>	<xml>	Click this icon to toggle between the user interface and xml code. The changes made in user interface are also reflected in xml code and vice versa.
	Show Patterns	Shows the patterns in the **Pattern Edit Pane** if the selected block has memory patterns.

Elements	Name	Description
	Break	Click this icon to terminate an infinite loop that is set to "manual" break condition. Sequence execution continues with the next block.
	Restart	Click this icon to interrupt and re-initialize a running sequence.
	Sync	Click this icon to sync the sequences globally.
	Import Sequence	Click this icon to import a sequence. For details, refer to Importing a Sequence on page 617.
	Export Sequence	Click this icon to export a sequence in the desired location. For details, refer to Exporting a Sequence on page 619.

Creating New Sequence

To create a new sequence:

1 Click on the **Create New Sequence** icon present on the toolbar. A **Create New Sequence** dialog will appear which allows you to create a new sequence.:



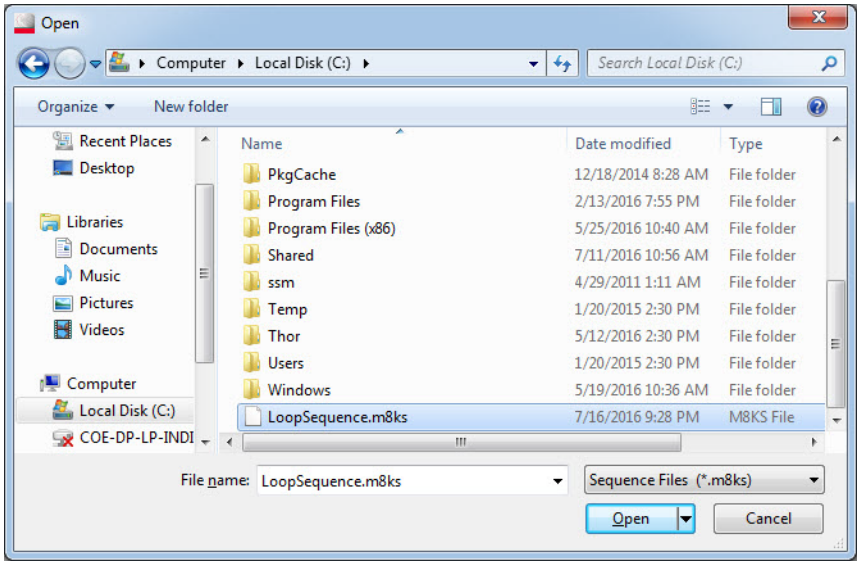
2 Perform the following settings:
   - **Name** - Provide a sequence name.
   - **Description** - Provide a description of the sequence.
   - **No. of Blocks** - Enter the no. of blocks to be added. You can add upto 500 blocks in a sequence.
   - **Locations** - Click on the button to open the **Select Sequence Locations** dialog box. Use this dialog box to select the sequence location. You can either select a single sequence location or multiple locations.
3 Click **Create** to create a sequence.

Importing a Sequence

The M8070B **Sequence Editor** allows you to import the sequences, edit them and then use them for testing and analysis.

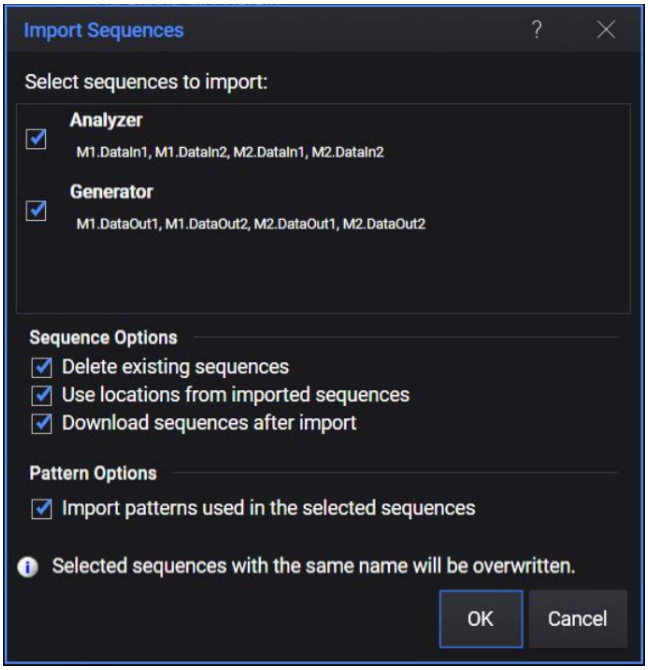
To import a sequence:

1 Click the **Import Sequence** icon. This opens the standard Windows **Open** dialog, where you can locate the sequences.



Please note that you are only allowed to import patterns with **.m8ks** file extension.

2 Click **Open**. A **Import Sequence** dialog will appear as shown in the following figure:



This dialog allows you to select the following sequence and pattern options:

a **Select sequence to import:** Select the check box to import the sequences from generator, analyzer or both.

b **Sequence Options:** Select the check box to delete existing sequences, use location of the imported sequences and download sequence after importing.

c **Pattern Option:** Select this option to also import the patterns used in the selected sequences.

3 Click **OK** to import the sequences.

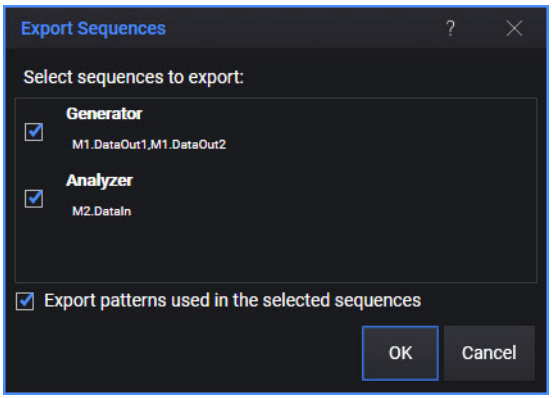
Please note that the selected sequences with the same name will be overwritten.

Exporting a Sequence

The M8070B **Sequence Editor** allows you to export patterns and use it for testing and analysis.

To export a pattern:

1 Click the **Export Sequence** icon. This opens the **Export Sequence** dialog which allows you to export the sequences from Generator, Analyzer or both. Additionally, it also allows you to export the patterns used in the sequences.

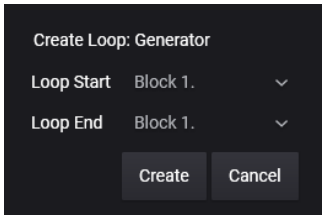


2 Click **OK**. A standard Windows **Save As** dialog will open which allows you to save the sequence under the defined file name and location.

Creating a Loop

To create a loop (if desired):

- Click the **Add Block Before** icon to add the blocks before the selected sequence blocks.
- Click the **Add Block After** icon to add the blocks after the selected sequence blocks.
- Click the **Create Loop** icon. A **Create Loop** dialog will appear as shown in the following figure:



- Specify the start and end block of the loop for the specified sequence (for e.g. generator, analyzer or user-defined sequence).
- Click **Create** to create a loop in the specified blocks.
- Click on the loop indicator. You will see a **Loop Setting** functional block in the **Sequence Setting** window where you can specify the loop count and enable the looping option.

Loop Within Sequences

A loop defines the transition from the end of a block to the beginning of the same or a previous block. It is not possible to jump into an existing loop. It is possible to define loops within loops, but it is not allowed to create multiple loops spanning the same segments.

For information on how to create a loop, refer to Creating a Loop on page 619.

Deleting a loop - It is possible to delete a loop. To delete a loop, select the loop indicator and click **Delete** icon.

Modifying the Existing Sequences

By default, the **Generator** and **Analyzer** sequences already exist whenever you launch a **Sequence Editor**. You can however modify these sequences as per the requirements. Using these options, you can:

- Add and delete the blocks
- Add loops in the blocks
- Specify the settings for each block using the **Sequence Settings** window. For more details, refer to Sequence Setting Window on page 621.

Once the settings are done, click the Download icon to apply the sequence settings either on generator or on analyzer or on both.

NOTE

Please note that there should be at least one block in the sequence.

Remember that you are not allowed to perform delete operation in the block if there is only one block in sequence.

Sequence Setting Window

The **Sequence Setting** window allows you to set the properties for the selected block and sequence. Using this window, you can specify the following settings:

- **Instrument Configuration**. For details, refer to Instrument Configuration on page 622.
- **Sequence Configuration**. For details, refer to Sequence Configuration on page 635.
- **Link Training Configuration**. For details, see Link Training Configuration on page 625
- **Block Data**. For details, refer to Block Data on page 636.
- **Block Settings**. For details, refer to Block Settings on page 640.
- **Block Branches**. For details, refer to Block Branches on page 641.
- **Block Controls**. For details, refer to Block Controls on page 642.

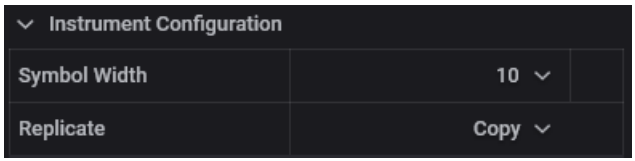
Set to Default Check-Box

Most of the parameters in the **Sequence Setting** window contains a **Set to Default** check-box which gets highlighted when some modifications are done. You can click on this check-box to change the settings to their default values.

The following figure shows how the check-box gets highlighted when you modify the PHY Protocol to PCIe3.

However, when you click on the **Set to Default** check-box, the value changes to None (default value). See the following figure.

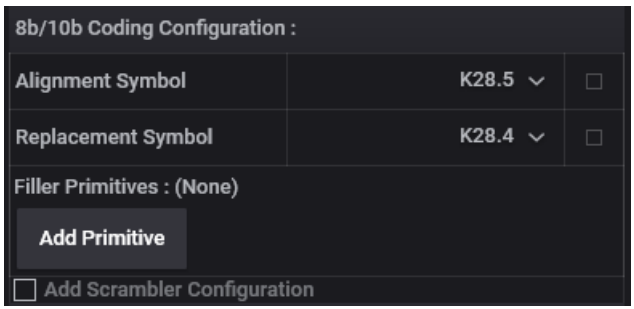
Instrument Configuration



The instrument configuration section provides the following options:

- **Symbol Width**: Use this option to select the symbol width e.g, 1, 10, 130 or 132 bit. Depending upon the symbol width you have selected, you can specify the coding configuration for that particular symbol width.
- **Replicate**: Select the replicate option (Serialized, Copy or Copy plus Phase Adjust).

If the symbol width is 10, you can specify the 8B/10B coding configuration. Using this, you can define alignment symbol, replacement symbol and filler primitives.



The **Alignment Symbol** contains the K28.1, K28.5 and K28.7 symbols.

The **Replacement Symbol** contains the K28.0, K28.4, K28.7, K23.7, K27.7, K29.7 and K30.7 symbols.

Filler Primitives are inserted or deleted for clock tolerance compensation. These are not compared and therefore cannot be counted as errors. **Filler Primitives** contain symbols. A maximum of four alternative filler primitives can be used. Each filler primitive can consist of up to 4 filler symbols. Filler symbols are separated by comma (,). To add filler primitive;

- Click the **Add Primitive** button.
- Enter the **Symbol**. The filler primitive can consist of up to 4 filler symbols.

Wild Cards for Filler Primitives

The wild cards allow you to set one or more out of the maximum of four symbols of a filler primitive as don’t care. In this case, all allowed D and K symbols will match and are removed from incoming DUT data.

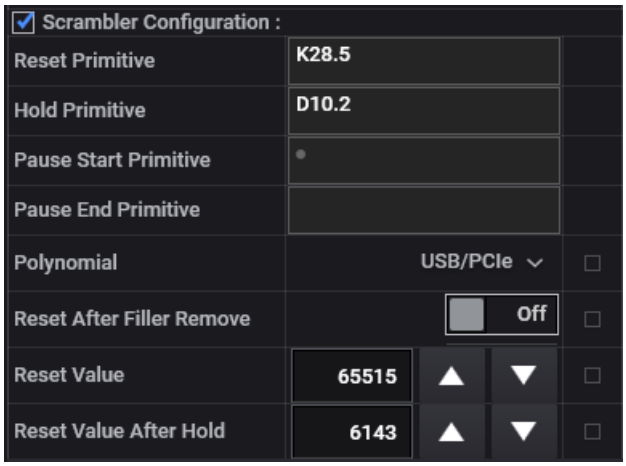
For example:

K28.5, •

Here the dot (•) symbol will be treated as don't care.

Add Scrambler Configuration

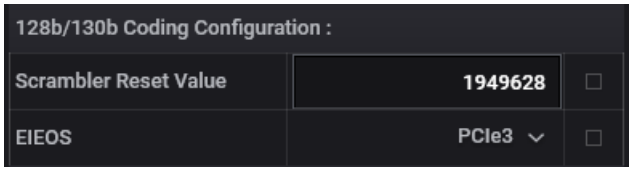
Select the **Scrambler Configuration** check-box to add scrambler configuration to the sequence.



It allows you to:

- Reset Primitive
- Hold Primitive
- Pause Start Primitive
- Pause End Primitive
- Polynomial
- Reset After Filler Remove
- Reset Value
- Reset Value After Hold

If the symbol width is 130, you can specify the 128B/130B coding configuration. Using this, you can define scrambler reset value and EIEOS (Electrical Idle Exit Ordered Set) for PCIe3 or PCIe4.



PCIe/USB/SATA Scrambler Polynomials

For the symbol width 8b/10b, the following scrambler polynomials are used:

- **PCIe/USB** - $G(x) = x^{16} + x^5 + x^4+x^3+1$
- **SATA** - $G(x) = x^{16} + x^{15} + x^{13}+x^4+1$

For the symbol width 128b/130b and 128b/132b, both standards use the same scrambler polynomial as following:

- **PCIe/USB -** $G(x) = x^{23} + x^{21} + x^{16}+x^8+x^5+x^2+1$

Link Training Configuration

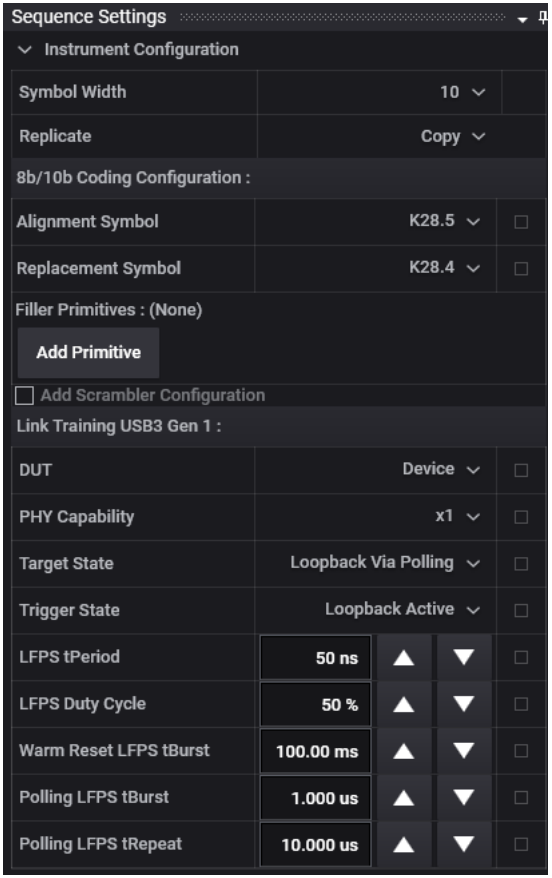
This section allows you to configure link training for USB 3.2 Gen 1, USB 3.2 Gen 2, PCIe 3.0, PCIe 4.0, PCIe 5.0, and PCIe 6.0.

Link Training for USB 3.2 Gen 1 and USB 3.2 Gen 2

The M8070B system software allows you to test the physical layer compliance of a USB 3.2 Gen 1 and USB 3.2 Gen 2 DUT. It provides the parameters which can be configured for link training USB 3.2 Gen 1 and USB 3.2 Gen 2.

If the symbol width is 10, you can configure the link training parameters for USB 3.2 Gen 1 to control LTSSM ((Link Training and Status State Machine). However, if the symbol width is 132, you can configure the link training parameters for USB 3.2 Gen 2 to control LTSSM.

The following figure shows the parameters which can be configured for link training USB 3.2 Gen 1:



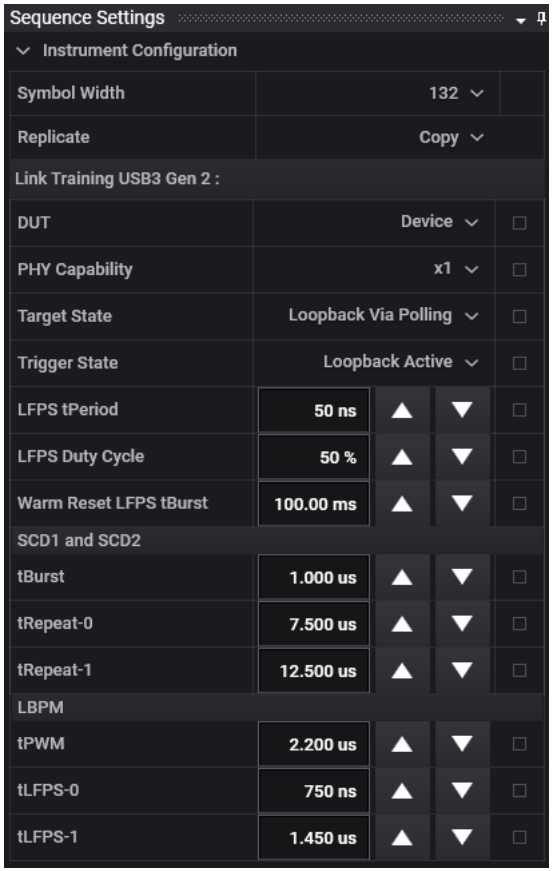
The following parameters are available to configure the link training USB 3.2 Gen 1:

- **DUT** - Specifies which role the BERT should play during link training. It can either be an upstream device for testing a downstream port or vice versa.
- **PHY Capability** - Specifies the PHY capability of the DUT. This selects whether the LTSSM is working in single lane mode (x1) or dual lane mode (x2). By default, the selected value is **x1**. When selecting the option **x2**, then channel 1 takes the role of the config lane during the link training.

Using **x2** requires to have a module with two pattern generators and two error detector channels.

- **Target State** - Determines the target state when bringing up the link.
- **Trigger State** - This parameter determines when the trigger output signal of the LTSSM block should be asserted. Additionally this information can be translated into a trigger pulse on entering or leaving the specified state. This is done by the pulse shaper of the TCRL OUT connector and no direct functionality of the LTSSM.
- **LFPS tPeriod** - Period of the LFPS cycle.
- **LFPS Duty Cycle**- Duty cycle of the LFPS cycle
- **Warm Reset LFPS tBurst**- LFPS triggers transition to Rx.Detect.
- **Polling LFPS tBurst**- Link Training handshake before 5Gb/s.
- **Polling LFPS tRepeat**- Link Training handshake before 5Gb/s.

The following figure shows the parameters which can be configured for link training USB 3.2 Gen 2:



The following parameters are available to configure the link training USB 3.2 Gen 2:

- **DUT Type** - Specifies which role the BERT should play during link training. It can either be an upstream device for testing a downstream port or vice versa.
- **PHY Capability** - Specifies the PHY capability of the DUT. This selects whether the LTSSM is working in single lane mode (x1) or dual lane mode (x2). By default, the selected value is **x1**. When selecting the option **x2**, then channel 1 takes the role of the config lane during the link training.

  Using **x2** requires to have a module with two pattern generators and two error detector channels.

- **Target State** - Determines the target state when bringing up the link.
- **Trigger State** - This parameter determines when the trigger output signal of the LTSSM block should be asserted. Additionally this information can be translated into a trigger pulse on entering or leaving the specified state. This is done by the pulse shaper of the TCRL OUT connector and no direct functionality of the LTSSM.
- **LFPS tPeriod** - Period of the LFPS cycle.
- **LFPS Duty Cycle**- Duty cycle of the LFPS cycle
- **Warm Reset LFPS tBurst**- LFPS triggers transition to Rx.Detect.
- **SCD1 and SCD2** - SuperSpeedPlus Capability Declaration (SCD) is a step for a SuperSpeedPlus port, while in the Polling. LFPS substate, to identify itself as SuperSpeedPlus capable by transmitting Polling. LFPS signals with specific patterns unique to SuperSpeedPlus ports.
- **SuperSpeedPlus LFPS Based PWM Message (LBPM)** - LBPM is defined as a low power signaling mechanism for two SuperSpeedPlus ports to communicate with each other based on LFPS signals. The adoption of Pulse Width Modulation (PWM) is to embed the transmitting clock in data and to allow for easy data recovery at the receiver based on LFPS clock.

For further details on link training for USB 3.2 Gen 1 and USB 3.2 Gen 2, refer to Interactive Link Training on page 698.

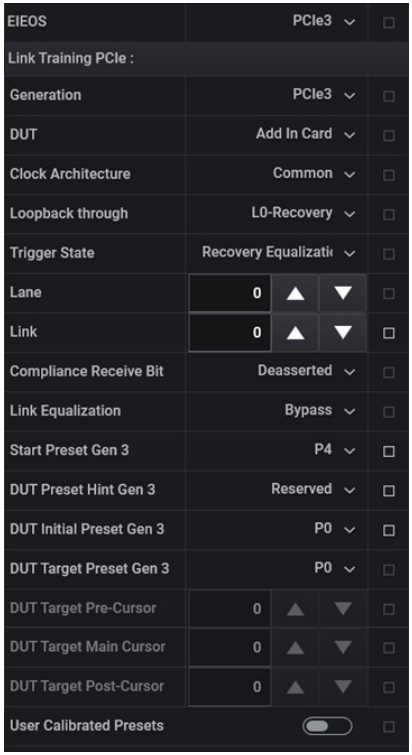
Link Training PCIe 3.0, PCIe 4.0, PCIe5.0, and PCIe6.0 Parameters

The M8070B system software allows you to test the physical layer compliance of a PCIe 3.0, PCIe 4.0, PCIe 5.0, and PCIe 6.0 DUT. It provides the parameters which can be configured for link training PCIe 3.0, PCIe 4.0, PCIe 5.0 and PCIe 6.0.

In case of M8020A, if the symbol width is 130, you can configure the link training parameters for PCIe 3.0 and PCIe 4.0 to control LTSSM ((Link Training and Status State Machine).

In case of M8040A/M8050A, the interactive link training functionality is specified differently by selecting a PHY Protocol from the Sequence Configuration block. For more details, see M8070B Support for PCIe3.0/4.0/5.0/6.0 Link Training using M8040A/M8050A on page 722.

The following figure shows the parameters which can be configured for link training PCIe 3.0:



The following parameters can be configured as an attributes.

- **EIEOS** - The EIEOS (Electrical Idle Exit Ordered Set) allows you to choose the pattern (PCIe3 | PCIe4) to be used for link training.
- **Generation** - Specifies the target link training PCIe Gen3 (8GT/s) or PCIe Gen 4 (16GT/s).
- **DUT Type** - Specifies which role the DUT should play during link training. It can either be an upstream device for testing a downstream port or vice versa.
- **Clock Architecture** - Specifies the clock architecture whether common or separate. In case of common clock, a common RefClk is expected. The M8000 instrument and the DUT run on the same clock. The RefClk is provided by the 'Trig Out' of the clock module of the M8000 instrument. In case of separate clock, the DUT runs on its own RefClk provided by itself or by an external source. The 'Trig Out' of the M8000 instrument is not used as RefClk for the DUT.

- **Loopback through** - Specifies if the real-time equalization is done while going into loopback through L0 / Recovery or through Configuration. When selecting Loopback through L0-Recovery, the LTSSM does a link training as before. Selecting Loopback through Configuration does a link training without real time equalization. When theLoopback through Configuration is selected, all preset parameters are disabled.
- **Trigger State** - Specifies the trigger state. It can be an Add-in-Card (AIC) or a root- complex.
- **Lane** - Specifies the lane number being used.
- **Link** - Specifies the link number being used.
- **Compliance Receive Bit** - Specifies whether the compliance received bit is asserted or deasserted.
- **Link Equalization** - Determines whether link equalization should be performed. It can either be aborted after phase 1 (Bypass) or fully executed. In the second case it can be determined whether only preset or all (i.e. individual cursor) requests should be accepted.
- **Start Preset** - Specifies the preset used by the J-BERT's TX port after switching to Gen 3 operation and when operating as an upstream device.
- **DUT Preset Hint** - Specifies the preset hint being sent by the J-BERT to the DUT during phase 0 of the link equalization procedure. It is only used when the BERT operates as upstream device.
- **DUT Initial Preset** - Specifies the preset the J-BERT transfers to the DUT in phase 0 of the link equalization procedure. It is only used when the BERT operates as an upstream device.
- **DUT Target Preset** - Specifies the preset the J-BERT requests the DUT to switch to during link equalization. Depending on the role the J-BERT is playing, this is done in either phase 2 or 3 of the link equalization training.
- **Speed Change Control** - Specifies whether the speed change to Gen3 (i.e. 8 Gbps) speed will be initiated by DUT or BERT during link training. It is only used when the BERT operates as a downstream device.
  If not specified DUT will initiate the speed change and will also request BERT for the same. It is only used for the DUT type as System Board.
- **User Calibrated Presets** - Specifies whether BERT's Data Out should use user-calibrated presets or standard presets during link training. Enabling it means that BERT's Data Out will use deemphasis/pre-shoot values that had been previously calibrated, otherwise it will use standard deemphasis/pre-shoot values defined by the PCIe3 specification. By default this option is turned off which means that standard presets will be used.

For further details on link training for PCIe 3.0, refer to Interactive Link Training on page 698.

The following figure shows the parameters which can be configured for link training PCIe 4.0:

The following parameters can be configured as an attributes.

- **EIEOS** - The EIEOS (Electrical Idle Exit Ordered Set) allows you to choose the pattern (PCIe3 | PCIe4) to be used for link training.

  Electrical Idle Exit Ordered Set (EIEOS) for 8.0 GT/s Data Rates

Symbol Numbers	Value	Description
0, 2, 4, 6, 8, 10, 12, 14	00h	Symbol 0: EIEOS Identifier A low frequency pattern that alternates between eight 0s and eight 1s.
1, 3, 5, 7, 9, 11, 13, 15	FFh	A low frequency pattern that alternates between eight 0s and eight 1s.

Electrical Idle Exit Ordered Set (EIEOS) for 16.0 GT/s Data Rates

Symbol Numbers	Value	Description
0, 1, 4, 5, 8, 9, 12, 13	00h	Symbol 0: EIEOS Identifier A low frequency pattern that alternates between sixteen 0s and sixteen 1s.
2, 3, 6, 7, 10, 11, 14, 15	FFh	A low frequency pattern that alternates between sixteen 0s and sixteen 1s.

- **Generation** - Specifies the target link training PCIe Gen3 (8GT/s) or PCIe Gen 4 (16GT/s).

  If Gen 4 is selected:

  DUT Target Preset - Cursor is not available in this case for Gen 3

  DUT Target Preset (Gen4) - Cursor can be used instead only for Gen 4
- **DUT Type** - Specifies which role the DUT should play during link training. It can either be an upstream device for testing a downstream port or vice versa.
- **Clock Architecture** - Specifies the clock architecture whether common or separate. In case of common clock, a common RefClk is expected. The M8000 instrument and the DUT run on the same clock. The RefClk is provided by the 'Trig Out' of the clock module of the M8000 instrument. In case of separate clock, the DUT runs on its own RefClk provided by itself or by an external source. The 'Trig Out' of the M8000 instrument is not used as RefClk for the DUT.
- **Loopback through** - Specifies if the real-time equalization is done while going into loopback through L0 / Recovery or through Configuration. When selecting Loopback through L0-Recovery, the LTSSM does a link training as before. Selecting Loopback through Configuration does a link training without real time equalization. When theLoopback through Configuration is selected, all preset parameters are disabled.

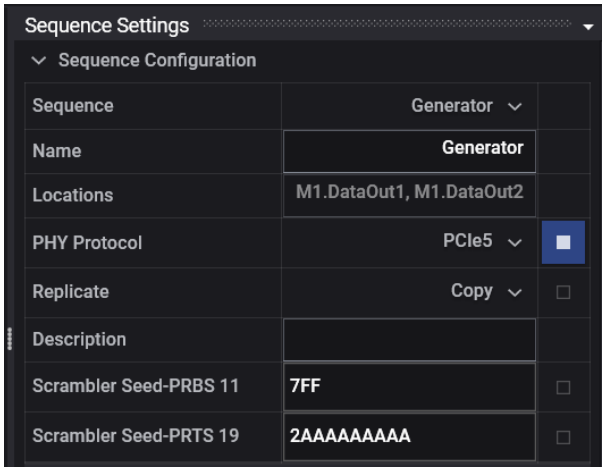
- **Trigger State** - Specifies the trigger state. It can be an Add-in-Card (AIC) or a root- complex.
- **Lane** - Specifies the lane number being used.
- **Link** - Specifies the link number being used.
- **Compliance Receive Bit** - Specifies whether the compliance received bit is asserted or deasserted.
- **Link Equalization** - Determines whether link equalization should be performed. It can either be aborted after phase 1 (Bypass) or fully executed. In the second case it can be determined whether only preset or all (i.e. individual cursor) requests should be accepted.
- **Start Preset** - Specifies the preset used by the J-BERT's TX port after switching to Gen 4 operation and when operating as an upstream device.
- **DUT Preset Hint** - Specifies the preset hint being sent by the J-BERT to the DUT during phase 0 of the link equalization procedure. It is only used when the BERT operates as upstream device.
- **DUT Initial Preset** - Specifies the preset the J-BERT transfers to the DUT in phase 0 of the link equalization procedure. It is only used when the BERT operates as an upstream device.
- **DUT Target Preset** - Specifies the preset the J-BERT requests the DUT to switch to during link equalization. Depending on the role the J-BERT is playing, this is done in either phase 2 or 3 of the link equalization training.
- **Select Start Preset Gen 4** - User Defined

  Defines which values to be used as Start Preset Gen4

  - User_Defined - Start Preset (Gen 4) entered by user.
- **Start Preset Gen 4** - Start Preset Gen 4 value entered by user (P0 – P9).
- **DUT Initial Preset Gen 4** - DUT Initial Preset Gen 4 value entered by user (P0 – P9).
- **DUT Target Preset Gen 4** - DUT Target Preset Gen 4 value entered by user (P0 – P9, Cursor)
- **User Calibrated Presets** - Specifies whether BERT's Data Out should use user-calibrated presets or standard presets during link training. Enabling it means that BERT's Data Out will use deemphasis/pre-shoot values that had been previously calibrated, otherwise it will use standard deemphasis/pre-shoot values defined by the PCIe3 specification. By default this option is turned off which means that standard presets will be used.

For further details on link training for PCIe 4.0, refer to Interactive Link Training on page 698.

Sequence Configuration



The sequence configuration section provides the following options:

- **Sequence**: Allows you to apply a sequence configuration on either Generator, Analyzer or user-created sequences.
- **Name**: Provide the sequence name.
- **Locations**: Specify the locations for the sequence. Use the button available to select the locations.

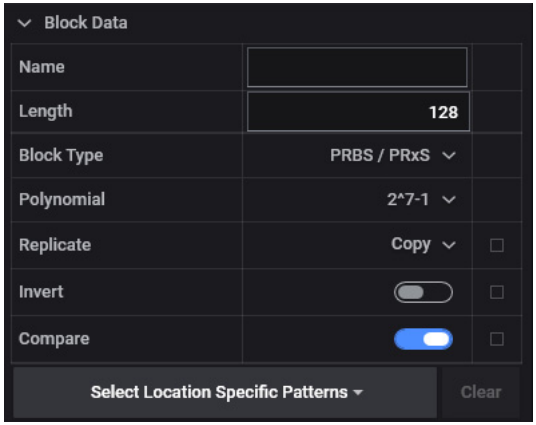
NOTE

Make sure not to use the unused location which are not being used in the test setup. However, if it is used, ensure that the 'Re-Sync' parameter of these locations is set to manual to reduce overall system load caused by unnecessary pattern re-sync attempts.

- **PHY Protocol**: Allows you to select PHY protocol. The available options are PCIe3, PCIe4, PCIe5, PCIe6, USB3 Gen1, and USB3 Gen2.
- **Replicate**: Select the replicate option (Serialized, Copy or Copy plus Phase Adjust).
- **Description**: Add a description to the sequence.
- **Seed PRBS 11**: Input field for Seed PRBS 11. Provide value in Hex.
- **Seed PRTS 19**: Input field for Seed PRTS 19. Provide value in Hex.

- **Scrambler Seed-PRBS 11**: Input field for scrambler seed PRBS 11. Scrambler seed value is only applicable in case of PAM3 line coding and at the **Data Out** location. The scrambler is applicable by enabling the **Scrambler** option available in the **Block Settings** functional block.
- **Scrambler Seed-PRTS 19**: Input field for scrambler seed PRBS 19. Scrambler seed value is only applicable in case of PAM3 line coding and at the **Data Out** location. The scrambler is applicable by enabling the **Scrambler** option available in the **Block Settings** functional block.
- **Inverse Precoding**: Applicable for only PCIe5 PHY Protocol. This option allows you to enable or disable the inverse precoding for PCIe5. This control is only available on the error detector. If enabled, information is required for Precoding in the PG pattern file.

Block Data



The **Block Data** section allows you to:

- Provide a block name.
- Provide a block length.
- Select **Block Type.** The available options are **Clock**, **Pulse**, **PRBS**, **Static**, **Memory Pattern, Squelch** and **Link Training**.
  - For block type as **Clock**, you need to specify the **Divider**, **Replicate** and the **Compare** feature (refer Compare Feature on page 639).

- The **Replicate** feature shows how the serial patterns are split to multiple locations. It has the option options:
  Serialize: In this a pattern is split and distributed to the locations. This is for the parallel side of a serial bus.
  Copy: In this each location gets a copy of the pattern.
  Copy Plus Phase Adjust: In this each location gets a copy of the pattern. Scrambler phases of the different locations are set differently. This is for the parallel side of a serial bus.
- For block type as **Pulse**, you need to specify the **Width**, **Compare** and **Offset** feature.
- For block type as **PRBS**, you need to specify the **Polynomial**, **Replicate**, **Invert** and **Seed (Hex)** feature. Refer to the Table 58 on page -637 and Table 59 on page -638 for the list of available PRBS polynomials.

The following tables shows the PRBS polynomial for M8020A/M8040A that is used to generate the selected PRBS 2^n-1.

Table 58 PRBS polynomials for M8020A/M8040A

PRBS	Shift Register Length	Polynomial	PRBS Length
2^7-1	7	x^7+x^6+1	127
2^9-1	9	x^9+x^5+1	511
2^10-1	10	x^9+x^7+1	1023
2^11-1	11	$x^{11}+x^9+1$	2047
2^13-1	13	$X^{13} + X^{12} + X^2 + X^1 + 1$	8191
2^15-1	15	$x^{15}+x^{14}+1$	32767
2^23-1	23	$x^{23}+x^{18}+1$	8388607
2^23p-1	23	$x^{23}+x^{21}+x^{18}+x^{15}+x^7+x^2+1$	8388607
2^31-1	31	$x^{31}+x^{28}+1$	2147483647
2^33-1	33	$X^{33} + X^{20} + 1$	8589934591
2^35-1	35	$X^{35} + X^{33} + 1$	34359738367

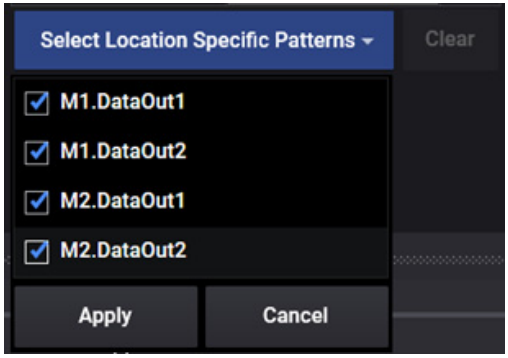
PRBS	Shift Register Length	Polynomial	PRBS Length
2^39-1	39	$X^{39} + X^{35} + 1$	549755813887
2^41-1	41	$X^{41} + X^{38} + 1$	2199023255551
2^45-1	45	$X^{45} + X^{44} + X^{42} + X^{41} + 1$	35184372088831
2^47-1	47	$X^{47} + X^{42} + 1$	140737488355327
2^49-1	49	$X^{49} + X^{40} + 1$	562949953421311
2^51-1	51	$X^{51} + X^{50} + X^{48} + X^{45} + 1$	2251799813685247

The following tables shows the PRBS polynomial for M8194A/M8195A/M8196A that is used to generate the selected PRBS 2^n-1.

Table 59 PRBS polynomials for AWG (M8194A/M8195A/M8196A)

PRBS	Shift Register Length	Polynomial	PRBS Length
2^7-1	7	x^7+x^6+1	127
2^9-1	9	x^9+x^5+1	511
2^11-1	11	$x^{11}+x^9+1$	2047
2^13-1	13	$X^{13} + X^{12} + X^2 + X^1 + 1$	8191
2^15-1	15	$x^{15}+x^{14}+1$	32767

  - For block type as **Static**, you need to specify the **Single Value** and the **Compare** feature.
  - If you select **Block Type** as **Memory Pattern**, a **Select Pattern** window will open which allows you to load the memory patterns.
  - For block type as **Link Training**, you need to specify the **Direction.**
- Click **Select Location Specific Patterns**. This opens with a drop-down selection where you can specify the ports or locations of specific patterns.



- Select the ports or locations and then click **Select**. The settings option for each port or location will be added to the **Block Data** functional block.
- Click **Clear** if you want to remove port or location specific patterns and use single pattern for the block.

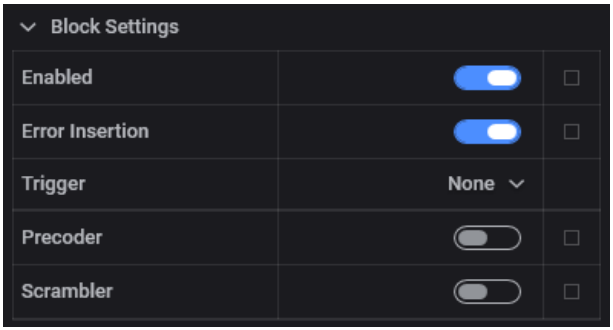
Compare Feature

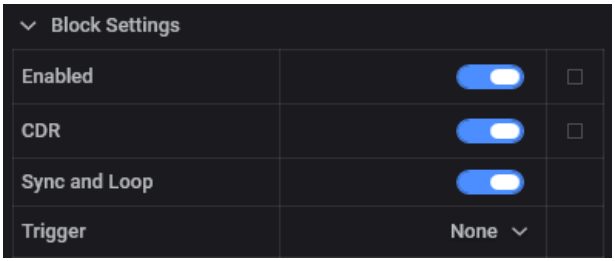
The **Compare** feature allows you to compare the block data for a particular sequence. It provides you the freedom to modify the sequence without deleting the blocks.

When to use/not use this feature

Suppose you created a sequence with multiple blocks. Now, if you want to exclude particular block(s) from that sequence while comparing, instead of deleting the whole sequence, just set the compare functionality “OFF” which in-turn will disable that particular block(s) from the sequence for comparison.

Block Settings





The **Block Settings** allows you to the following:

- **Enabled**: Click the toggle button to enable/disable the block settings on the sequence.
- **Error Insertion**: Click the toggle button to enable/disable the error insertion.
- **Trigger**: Use the drop down option to specify whether you want to apply trigger on either **Pulse** or **Pulse or PRBS Match**.
- **Precoder**: Click the toggle button to enable/disable the Sequence Controlled Precoder. This is applicable for PAM3 and PAM4 only. The Sequence Controlled option must be selected from Data Out Line Coding.
- **Scrambler**: Click the toggle button to enable/disable the Sequence Controlled Scrambler. This is applicable for PAM3 only.
- **CDR**: Click the toggle button to enable/disable the CDR. The Sequence Controlled option must be selected from Data In Line Coding.

- **Sync and Loop**: Click on the toggle button to turn on the **Sync and Loop** feature.

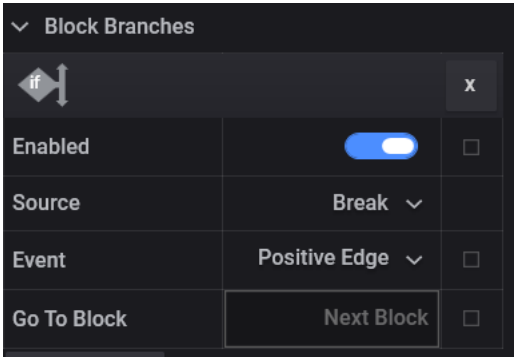
NOTE The Sync feature will be automatically turned on once you turn on the Sync and Loop feature.

NOTE The changes made in the **Block Settings** section are reflected on the selected block.

Block Branches

The **Block Branches** are used to add the branches within the sequence. You can add up to two branches in a sequence.

To add a **Block Branches**, click on the **Add Branch** button. The **Block Branches** section will appear as shown in the following figure:

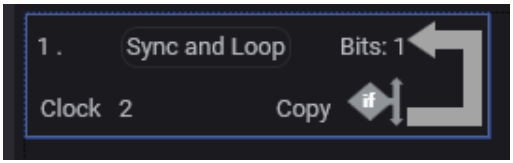


The **Block Branches** section provides the following settings:

- **Source**: Use the drop-down list to specify the source for the branch.
- **Event**: Specify the event for the branch.
- **Go to Block**: Specify the block name to jump.

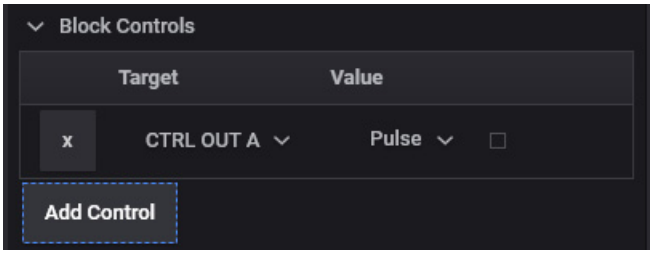
- **Enabled**: Use the ON/OFF toggle button to enable the branching option.
- Click **Add Branch** if you want to add another branch. Up to two branches can be added within the same block.
- Click **Delete** icon to delete the branch.

Once the branching is enabled in a block, the **Block Branches** icon will appear on the sequence block as shown in the following figure:



Block Controls

The **Block Controls** section allows you to provide sink value at Ctrl Out A and Sys Out A/B. These values help you to trigger the given sink at different values that are defined i.e. Low, High or Pulse. Press **Add Control** to add more block controls. You can add up to four block controls.



Editing a Pattern in a Sequence Editor

The **Sequence Editor** user interface contains **Pattern Edit Pane** that allows you to edit the memory patterns.

Make sure to enable the **Show Patterns** option by clicking on the **Show Pattern** icon, present on the toolbar. This will display the **Pattern Edit Pane**, in case it is not visible in the **Sequence Editor**.

To edit a pattern, you have to first load it in the sequence block. To do so:

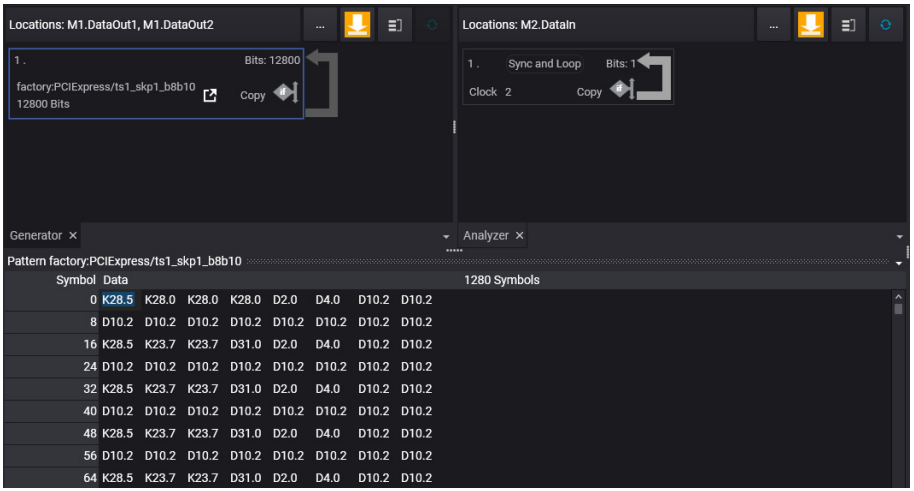
1 Select the block on which the patterns are loaded.

2 Go to **Sequence Setting** window and then select **Block Data** functional block.

3 Select the **Block Type** as **Memory Patterns**. A **Select Pattern** window will open which allows you to load the memory patterns. You can download large memory patterns (up to 2 Gb) on each channel.

4 Select the desired pattern and click **Select**.

5 The pattern will be loaded into the selected block as well as on the **Pattern Edit Pane**. See the following figure:



6 Edit the patterns as explained in the section Pattern Edit Pane on page 674.

Sharing Sequences

The M8070B software currently does not allow the functionality to share the sequences. However, there is a workaround to share sequences.

Follow the given steps:

1. Go to **File** > and click **Save Instrument State..**. Once you save the instrument state, the sequence settings are also saved in the **Settings** folder which is created at the following path:

   "Documents\Keysight\M8070B\Workspaces\Default\User\Settings"
2. Share **Settings** folder.
3. Copy the **Settings** folder at the same path on another system.
4. Go to **File** > and click **Recall Instrument State...**. The sequences will now appear in the **Sequence Editor**.

Using XML Files in the M8070B Sequence Editor

The M8070B **Sequence Editor** lets you define, edit, and manage (import/export) test sequences using XML files. XML files make it easy to share and reuse complex sequence setups.

You can use XML files in the Sequence Editor in several ways:

1. Open the M8070B Sequence Editor and create a new sequence. Once done, click the **<XML>** button to view the XML version of your sequence.

   Or

   Open an existing sequence file (*.m8ks) in the Sequence Editor and then click the **<XML>** button to view its XML code.

   Or

   Copy XML code from another source and paste it directly into the XML view of the **Sequence Editor**.
2. Modify the XML content as required to update or customize your sequence.
3. After editing, click the **Download** button to send the sequence to the connected hardware.
4. If required, export the sequence as an *.m8ks file for saving or sharing.

Example

Here is an example of using an XML file that defines a data sequence for a test equipment sequencer, used in M8198A AWG. The file specifies a sequence of waveform playback instructions, including loop behavior, marker pulses, and conditional branching.

```
<?xml version="1.0" encoding="utf-16"?>
<sequenceDefinition xmlns:xsd="http://www.w3.org/2001/XMLSchema"
xmlns:xsi="http://www.w3.org/2001/XMLSchema-instance"
xmlns="http://www.keysight.com/schemas/M8000/DataSequence">
  <version>1.0.0</version>
  <description />
  <sequence>
<!-- This loop runs a fixed number of times, as specified by the "count" attribute. If "count" is
omitted, the loop runs indefinitely. -->
    <loop count="250000000">
      <segment>
<!-- Marker settings for the "Sample Mrk". These settings apply to all bound locations. -->
        <marker>
          <pulse width="128" />
        </marker>
<!-- Waveform source for this segment. -->
        <waveform source="trace:1" />
      </segment>
    </loop>
<!-- This is an infinite loop, as no "count" attribute isspecified. -->
    <loop>
      <segment>
        <marker>
          <pulse width="128" />
        </marker>
        <waveform source="trace:2" />
<!-- Conditional jump to another segment.
              - "goto" specifies the target segment name.
              - "source" defines the trigger condition:
                - Break: Triggered by clicking the "Break"
                  button in the UI.
                - EventInA / EventInA: External event inputs. -->
```

```
<if source="Break" goto="end" enabled="true"
        />
      </segment>
    </loop>
    <loop>
<!-- Each segment must have a unique name to allow conditional jumps. This segment is named "end".
-->
      <segment name="end">
<!-- Location-specific settings can be defined per target. Note: Marker width must be consistent
across all locations, but offsets may vary. -->
        <target location="M2.DataOut1">
          <marker>
            <pulse offset="0" width="128" />
          </marker>
          <waveform source="trace:3" />
        </target>
        <target location="M2.DataOut2">
          <marker>
            <pulse offset="128" width="128" />
          </marker>
          <waveform source="trace:3" />
        </target>
      </segment>
    </loop>
  </sequence>
</sequenceDefinition>
```

Table 60 on page -647 describes the key components included in the XML file:

Table 60 XML file key components

Element / Attribute	Description
<sequence>	Container for all sequence elements, including loops and segments.
<loop count="250000000">	Loop that repeats a fixed number of times (250 million).
<loop>	Loop without a count attribute; runs indefinitely.
	Defines a segment within a loop; contains waveform and marker settings.
<marker>	Specifies marker pulse settings.
<pulse offset="0" width="128" />	Offset for the marker pulse relative to the start of the segment. Width of the marker pulse in sample units. Has to be the same for all markers within this sequence.
<waveform source="trace:1" />	Specifies the waveform source for the segment (trace:1, trace:2, etc.). Here it specifies the waveform source for the segment trace:1.
<if source="Break" goto="end" enabled="true" />	Conditional jump triggered by a "Break" event, jumping to segment "end".
	Named segment used as a target for conditional jumps.
<target location="M2.DataOut1">	Location-specific settings can be defined to set different marker settings for different outputs.

NOTE

Note that the key components listed in the Table 60 are specific to M8198A AWG sequencing. When defining a sequence in M8070B, some XML components and structure may differ.

For more details on using an XML file to define a data sequence used in M8198A AWG, refer to the M8100 Series User Guide.

User-Defined Sequences

This section describes the basics of user-defined sequences.

A sequence is created and maintained by means of the Sequence Editor. A sequence consists of up to 500 blocks that can be looped. Each block can generate a pause signal (constant 0 or 1), a divided clock signal, a 2^n -1 PRBS, or a user pattern.

Single or multiple blocks can be looped. The sum of the blocks and the counted loops must not exceed 500. An overall loop restarts the sequence after it has come to its end.

Sequence Block Display

A new sequence consists of one block that is infinitely repeated (looped). By default, this block has a length of 512 bits and generates a Pause 0 signal (a continuous stream of zeros). All this is shown on the display.

Sequence Block Parameters

The **Sequence Setting** window allows you to change the contents and the trigger generation of a sequence block.

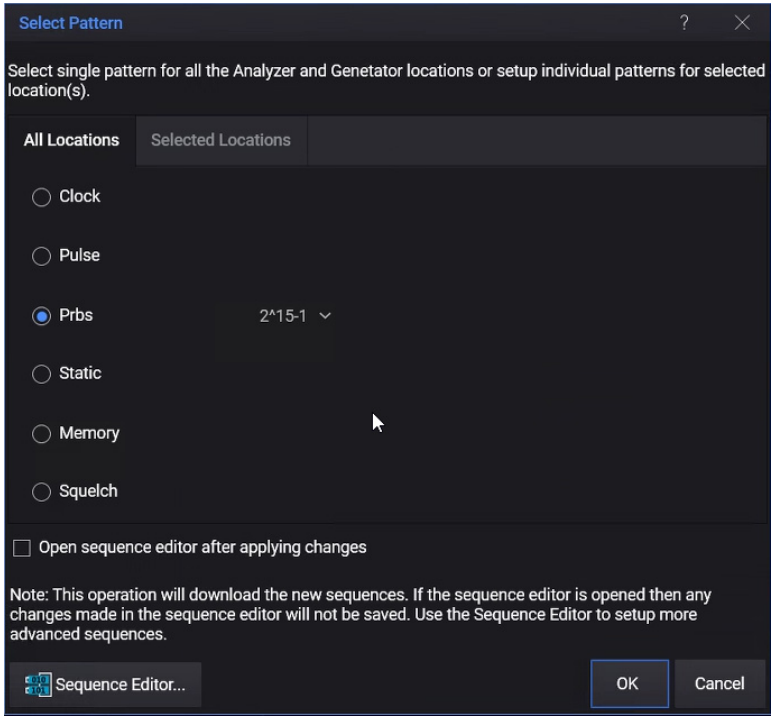
Choices are:

- **Block No.** - Can be up to 500 blocks.
- **Length** - This is the length of the pattern in bits for a standard pattern of 128 bits.
- **Block Type** - Clock, PRBS, Pulse, Static or Memory Patterns.
- **PRBS** - You can choose a PRBS of polynomial 2^n -1. The range of "n" is 7, 10, 11, 15, 23, or 31. You can change the block length, if desired.
- **Divided Clock**: You can use this option to generate the signal at every nth clock pulse.
- **Memory Pattern**: When you select pattern type as memory pattern, a **Select Pattern** dialog will appear. You have to locate the pattern file and then click **OK**. The patterns will be loaded in the sequence.

Select Pattern Dialog

The **Select Pattern** dialog allows you to either select single pattern for all the analyzer and Generator locations or setup individual patterns for selected locations.

NOTE This operation will download the new sequences. If the **Sequence Editor** is already opened, then changes made in the **Sequence Editor** will not be saved.



This dialog provides the following tabs:

All Locations

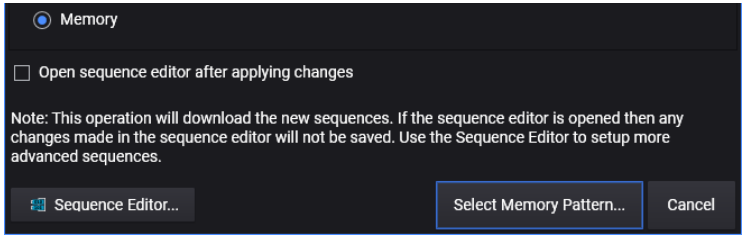
This tab allows you to select a single pattern and download it to all locations.

You to select the pattern from the following options:

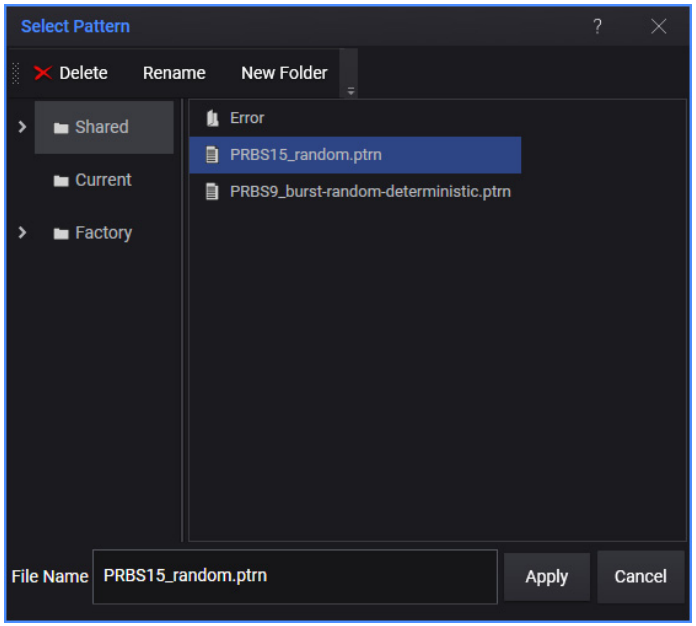
- Clock
- Pulse
- PRBS

  Refer to the Table 58 on page -637 and Table 59 on page -638 for the list of available PRBS polynomials.
- Static - The 1/0 values describe the logic bit content and high/low values relate to the level. Select 0 or Low for low level patterns and 1 or High for high level patterns. If you select the pattern as "inverted", then the value 1 can become low level and 0 can become the high level.
- Squelch (Electrical Idle)
- Memory

  In case the **Memory** option is selected, a **Select Memory Pattern...** button will appear.



When you click this button, the **Select Pattern** dialog will appear.



Once you select the pattern in **Select Pattern** dialog, click **Apply** button to download the pattern.

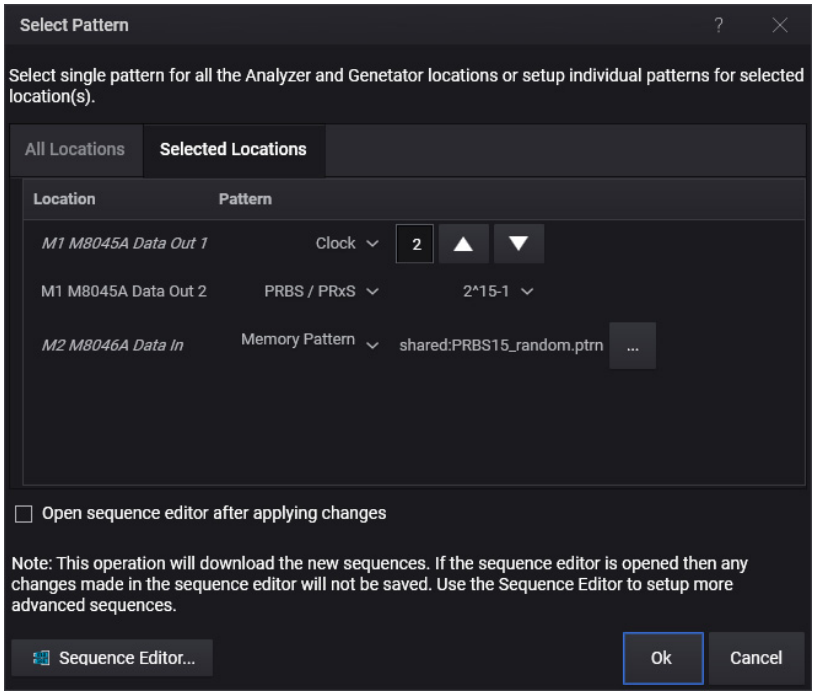
Selected Locations

This tab allows you to setup individual patterns for selected locations. You to select the pattern from the following options:

- Clock
- Pulse
- PRBS

  Refer to the Table 58 on page -637 and Table 59 on page -638 for the list of available PRBS polynomials.
- Static
- Squelch
- Memory

  In case the **Memory** option is selected, a **Select Pattern** dialog will appear to load the memory pattern.



If you wish to open the **Sequence Editor** with the selected patterns, either select the "**Open sequence editor after applying changes**" check-box or click the **Sequence Editor...** button.

Click **Apply** to apply the changes.

Application Specific Patterns

This section describes how to select the patterns for a specific standards. These patterns are applicable for M8045A and AWG (M8194A/M8195A/M8196A) modules.

OIF CEI

OIF CEI QPRBS13-CEI

This pattern is defined in CEI 56G-VSR-PAM4 appendix 16.C.3.1.

1 Select PRBS13-1 from hardware PRBS generator or use the factory pattern available at the following location:

   Factory\CEI\PRBS13Q-CEI_bit

2 Choose Line Coding as PAM4.

3 Set Symbol Mapping to Gray Coded (Default).

OIF CEI QPRBS31-CEI

This pattern is defined in CEI 56G-VSR-PAM4 appendix 16.C.3.2.

1 Select PRBS31-1 from hardware PRBS generator.

2 In the block settings activate the Invert feature of the hardware PRBS generator.

3 Choose Line Coding as PAM4.

4 Set Symbol Mapping to Gray Coded (Default).

IEEE 802.3

IEEE 802.3 QPRBS13

This pattern is defined in IEEE 802.3 clause 94.2.9.3. It is stored in a way that will output the correct PAM4 symbols when Symbol Mapping is set to Gray Coded.

1 Select the factory pattern available at the following location:

   Factory\IEEE\QPRBS13_Lane0_bit_SelectGrayCoded

2 Choose Line Coding as PAM4.

3 Set Symbol Mapping to Gray Coded (Default).

IEEE 802.3 PRBS13Q

This pattern is defined in IEEE 802.3 clause 120.5.11.2.3.

1 Select PRBS13-1 from hardware PRBS generator or use the factory pattern available at the following location:

   Factory\IEEE\PRBS13Q_Lane0_bit

2 Choose Line Coding as PAM4.

3 Set Symbol Mapping to Gray Coded (Default).

For convenience additional lane 1 to lane 3 versions are stored at:

Factory\IEEE\PRBS13Q_Lane1_bit

Factory\IEEE\PRBS13Q_Lane2_bit

Factory\IEEE\PRBS13Q_Lane3_bit

These additional versions are intended for multi-lane applications and using alternative seeds as defined in table IEEE 802.3 94-11.

IEEE 802.3 PRBS31Q

This pattern is defined in IEEE 802.3 clause 120.5.11.2.4.

1 Select PRBS31-1 from hardware PRBS generator.

2 In the block settings activate the Invert feature of the hardware PRBS generator.

3 Choose Line Coding as PAM4.

4 Set Symbol Mapping to Gray Coded (Default).

IEEE 802.3 SSPRQ

The IEEE/SSPRQ_bit_SelectGrayCoded (120.5.11.2.3) pattern corresponds to the pattern as defined in release 1.0 of the spec while IEEE/SSPRQ_bit_SelectGrayCoded_D1p5 (120.5.11.2.5) pattern is the version from Draft 1.5 of the spec. It is stored in a way that will output the correct PAM4 symbols when Symbol Mapping is set to Gray Coded.

1 Select the factory patterns available at the following location:

   Factory\IEEE\SSPRQ_bit_SelectGrayCoded

   Factory\IEEE\SSPRQ_bit_SelectGrayCoded_D1p5

2 Choose Line Coding as PAM4.

3 Set Symbol Mapping to Gray Coded (Default).

Pattern Editor

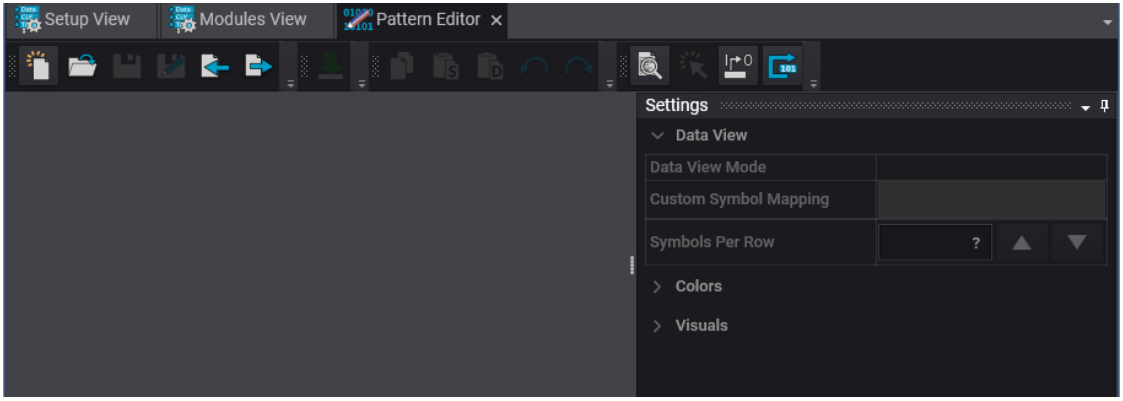
The pattern editor provides an interactive user-interface for creating, editing and importing the patterns.

How to Launch Pattern Editor

To launch the **Pattern Editor**:

- Go to the **Menu Bar** > **Patterns** and then select **Pattern Editor**.

The **Pattern Editor** will appear as shown in the following figure:



The **Pattern Editor** user interface includes the following elements:

- Toolbar
- Settings Window
- Pattern Edit Pane

Toolbar

The toolbar provides the following convenient pattern editing functions:

Table 61

Elements	Name	Description
	New	Click this icon to create a new pattern. For details, refer to Creating New Patterns on page 658
	Open	Click this icon to open a pattern from a file. For details, refer to Opening Existing Patterns on page 661
	Save	Click this icon to save the current pattern. For details, refer to Saving Patterns on page 663.
	Save As	Click this icon to change the properties of current pattern and then save it under different name. For details, refer to Saving Patterns on page 663.
	Import	Click this icon to import patterns, edit them and use them for testing and analysis. For details, refer to Importing Patterns on page 666.
	Export	Click this icon to export patterns in the desired location. These patterns can be used by other instruments for testing and analysis. For details, refer to Exporting Patterns on page 668.
	Download	Click this icon to download the pattern to either all locations or on the selected locations. An orange icon indicates that the pattern is modified and is not yet downloaded to any location(s).

Elements	Name	Description
	Copy	These functions follow Microsoft Windows copy/paste functionality. You can perform the copy/paste operations in the following ways: ▪ Click on Copy/Paste icons ▪ Use keyboard shortcuts (Ctrl+C, Ctrl+V) ▪ Right click and use the context menu options The Copy/Paste function allows you to: ▪ Select either the partial data or the complete symbols in a pattern and copy/paste it anywhere in the pattern. ▪ Use the copy/paste operations for the partial data across multiple instances of Pattern Editor, irrespective of the pattern coding. ▪ Use the paste operation to and from clipboard to Pattern Editor. Please note that the paste operations for the complete pattern symbol is only allowed in the same pattern symbol coding. This icon is only available when the partial data is copied from the pattern. Whenever a paste operation is done using this function, the underline data will be pasted.
	Paste as String	
	Paste as Data	
	Undo	Reverses the last editing action, such as typing, modifying or deleting text. When you do such actions, you can use the Undo command to restore them. Keyboard shortcut - Ctrl + Z
	Redo	Restores the last editing action, such as typing, modifying or deleting text if no other actions have occurred since the last Undo. Keyboard shortcut - Ctrl + R
	Find	Click this icon to open the Find Symbol dialog box and perform the search operation for a specified segment in the pattern. For details, see Find Symbol Dialog Box on page 669.
	Select All	Click this icon to select all the symbols in the pattern. Keyboard shortcut - Ctrl + A
	Block Edit	Click this icon to perform block edit operations on currently selected pattern. For details, refer to Block Edit Operations on page 670.
	Go To	Click this icon if you want to jump to an arbitrary bit position. See Go To Bit Dialog Box on page 671.

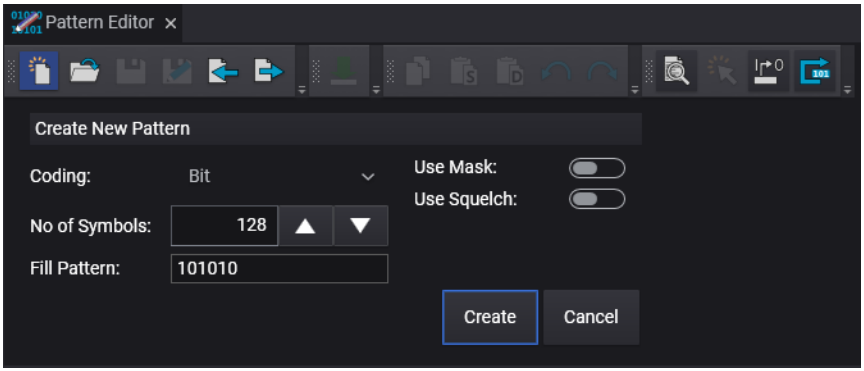
The **Pattern Editor** allows you to perform following tasks on patterns:

- Create a new patterns. For details, refer to Creating New Patterns on page 658.
- Open and already existing patterns. For details, refer to Opening Existing Patterns on page 661.
- Save a patterns. For details, refer to Saving Patterns on page 663.
- Import supported patterns. For details, refer to Importing Patterns on page 666.
- Perform block edit operations. For details, refer to Interactive Link Training on page 698.
- Edit a patterns on **Pattern Edit Pane**. For details, refer to Pattern Edit Pane on page 674.

Creating New Patterns

To create a new pattern:

1 Click the **New** icon present on the tool bar. This opens with the **Create New Pattern** sliding window as shown in the following figure:



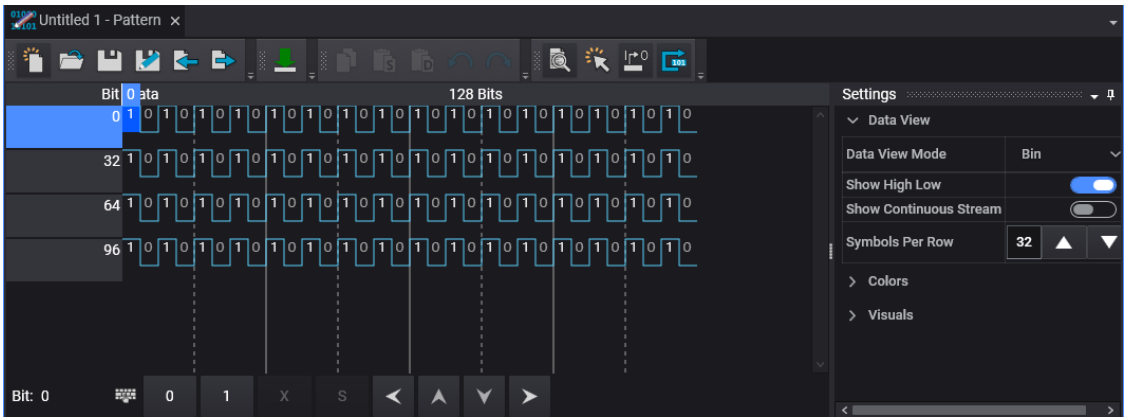
2 Select the coding type. The **Pattern Editor** currently supports the following types of coding:
   - Bit (Binary)
   - 8B/10B
   - 128B/130B
   - 128B/132B

3 Specify the number of symbols. Use the **UP** and **DOWN** button to increase or decrease the number of symbols.

4 Specify the fill patterns.

5 Specify by using the ON/OFF toggle switch whether you want to use **Mask** and **Squelch** (Electric Idle). In **Squelch**, the amplifier output is zero.

6 After you have entered these parameters, click **Create**. The newly created pattern will appear in the **Pattern Editor** pane.



7 Click the **Save** icon to save the pattern. For more details, refer to Saving Patterns on page 663.

Downloading Patterns

You can also download the pattern to either selected locations or on all locations using the **Download Pattern** dialog. To do so, follow the given steps:

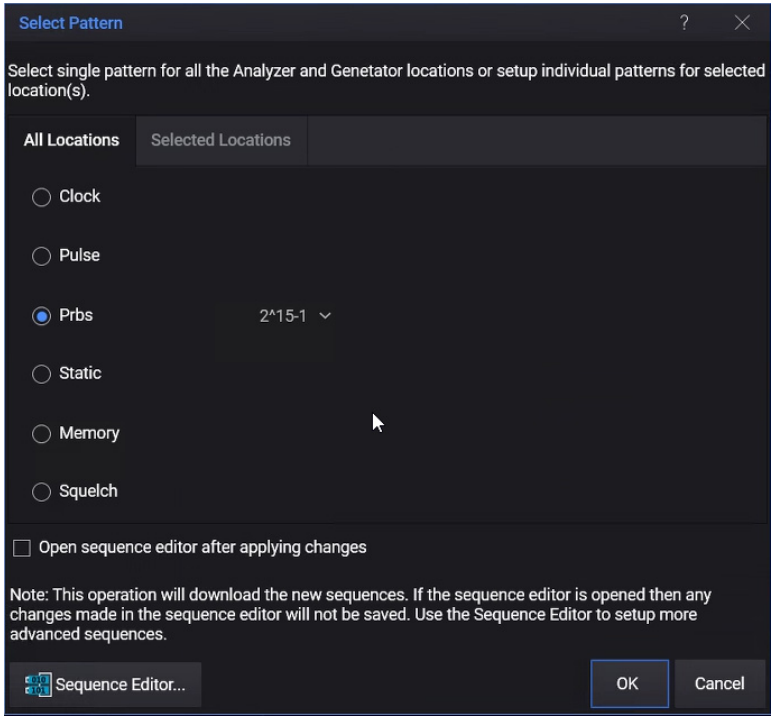
1 Create a new pattern or open an existing pattern.

2 Click on the **Download** button . If the pattern is not saved, a message will appear to save the pattern before downloading.

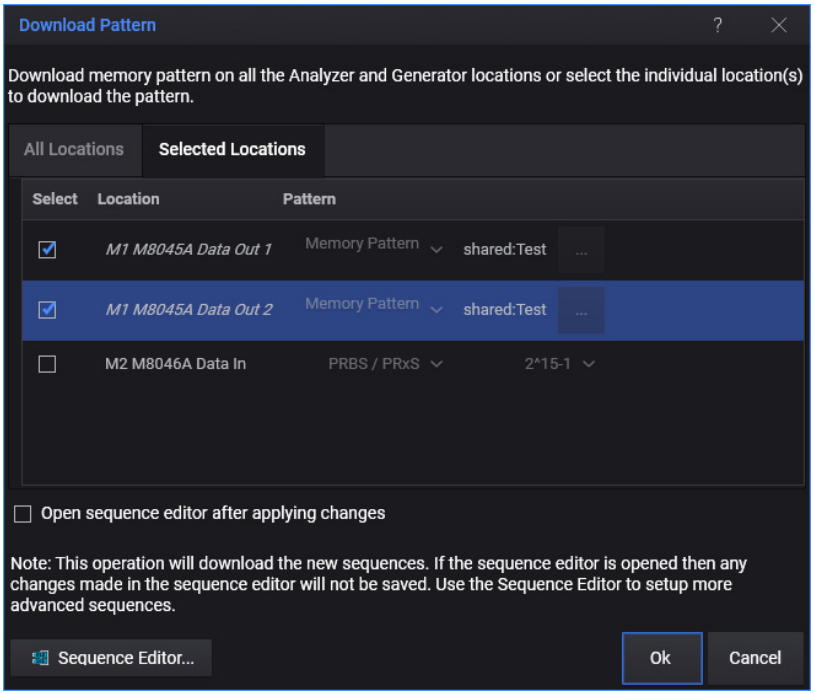
3 Once saved, a **Download Pattern** dialog will appear. This dialog allows you to download the selected pattern to either on all locations or on the selected locations.

This dialog provides the following tabs:

- **All locations** - Use this tab to download the memory pattern on all locations. Since, it is a memory pattern, this dialog disable all other pattern options. Only, the memory pattern option is available.



- **Selected Locations** - Use this tab to download the current pattern to the selected locations. On selecting the check-box, the name of the current pattern will appear.



4 Click **OK** to download the pattern.

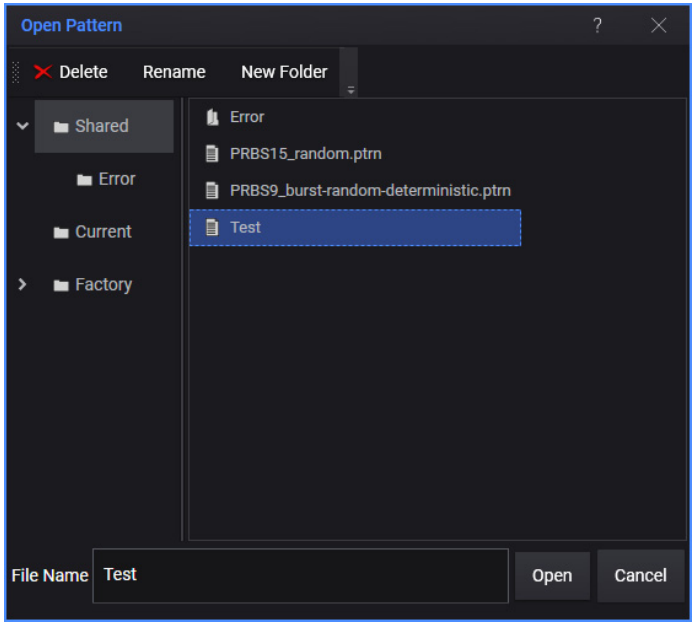
5 If you wish to open the **Sequence Editor** with the selected patterns, either select the "**Open sequence editor after applying changes**" check-box or click the **Sequence Editor...** button and then click **OK**.

Opening Existing Patterns

To open an existing user pattern:

1 Click the **Open** icon present on the tool bar.

This opens the **Open Pattern** dialog, where you can locate and open the desired pattern. You can even perform the operations such as renaming and deleting the pattern file and creating new folders.



You can select the pattern from the following default folders:

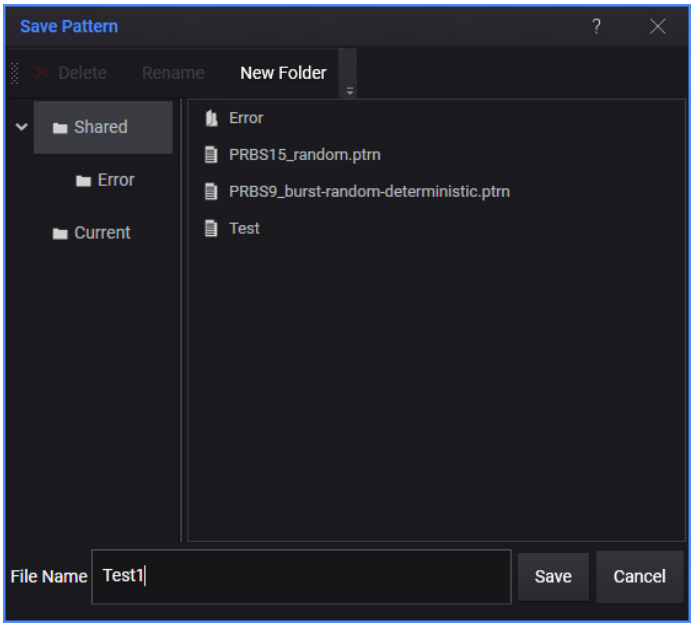
1 **Shared**: Patterns that are shared between settings.
2 **Current**: Patterns that are local to current setting.
3 **Factory**: Factory supplied standard patterns. These patterns are read only and cannot be modified.

2 Click **Open** to load the patterns.
3 To rename a file, select the file and click **Rename**. The filename will become editable.
4 To delete a file, select the file and click **Delete**.
5 To add new folder, select location you want to create your folder and then click **New Folder**.
6 To rename a folder, select the folder and click **Rename**. The folder name will become editable.
7 To delete a folder, select the folder and click **Delete**.

Saving Patterns

To save the current user pattern:

1 Click the **Save** icon present on the tool bar. A **Save Pattern** dialog will appear which allows you to save the patterns under the defined file name and location.

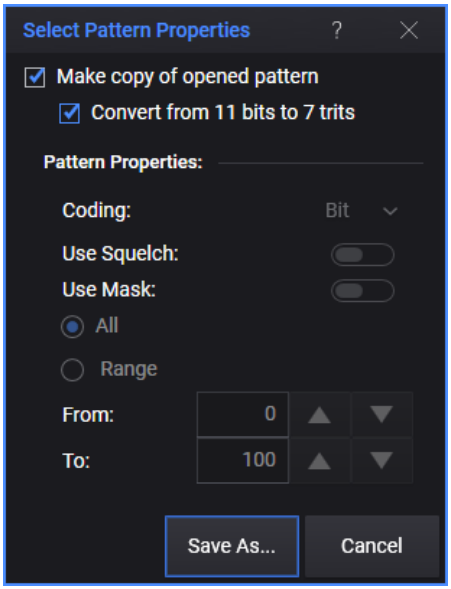


You can use the **Save Pattern** dialog to perform the operations such as renaming and deleting the patterns. You can even create a new folder or save the patterns in the **Current** or **Shared** folders. The current folder is for current users while the shared folder is accessible by all users. If the pattern has already been saved earlier, the saved file will be updated.

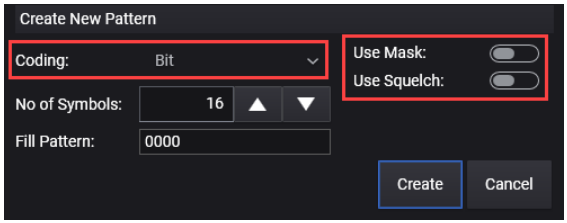
NOTE When naming the pattern file, ensure that the file name does not begin with a number or any special character.

2 Click the **Save As** icon if you wish to change the properties of current pattern and then save it under different name. The current pattern can be either a non-captured pattern or a captured pattern.

a For saving a non-captured pattern, a **Select Pattern Properties** dialog will appear. This dialog provides the following options:

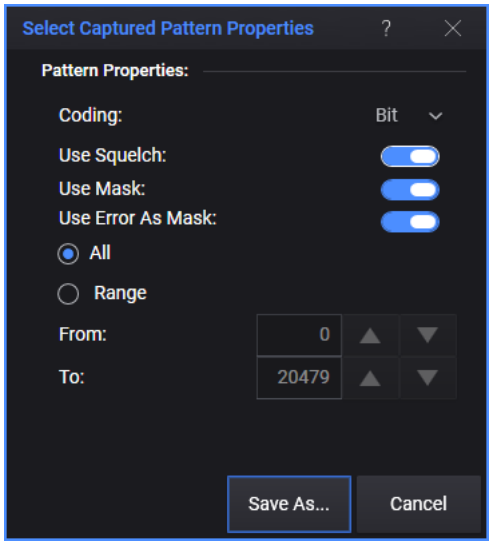


- Make a copy of current pattern with no change in pattern properties.
- Change the properties of current pattern. Using this option, you can change the pattern coding and enable/disable Squelch and Mask.
- You can save the entire pattern or can also provide the pattern range to be saved.
- The **Convert from 11 bits to 7 trits** option will be visible only if **Coding** is set as **Bit**, and **Use Squelch** and **Use Mask** options are disabled during new pattern creation.



- The **Convert from 11 bits to 7 trits** option will only be enabled if the **Make copy of opened pattern** check box is selected.
- If the **Convert from 11 bits to 7 trits** check box is selected, the **Save As** button will convert a group of 11 bits into a group of 7 trits form and display it into PAM3 data view.

b For saving a captured pattern, a **Select Captured Pattern Properties** dialog will appear. This dialog provides the following options:

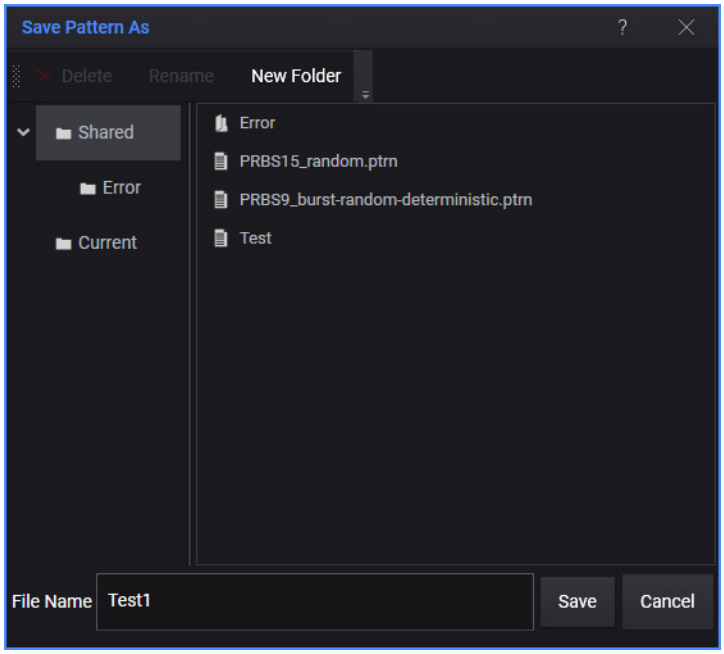


- Change the properties of current pattern. Using this option, you can change the pattern coding and enable/disable **Mask**, **Squelch** and **Error as Mask**.

The **Use Error As Mask** option is only visible when the **Use Mask** option is enabled and coding is same as captured pattern.

- Change the properties of current captured pattern. Using this option, you can change the pattern coding and enable/disable Mask, Squelch and Error as Mask.
- You can save the entire captured pattern or can also provide the pattern range to be saved.
- Click **Override** to remove all errors from the pattern.

3 Press **Save As...** button. A standard **Save As Pattern** dialog box will appear.



4 Specify the name and location and click **Save**.

Importing Patterns

The M8070B **Pattern Editor** allows you to import patterns, edit them and use it for testing and analysis.

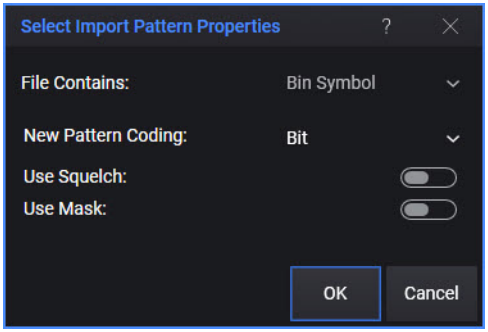
To import a pattern:

1 Click the **Import** icon. This opens the **Select File** dialog which allows you to locate the pattern. You are allowed to import patterns with any file extension (*.ptrn* and *.txt*).

2 Select the pattern and click **Open** in the **Select File** dialog.

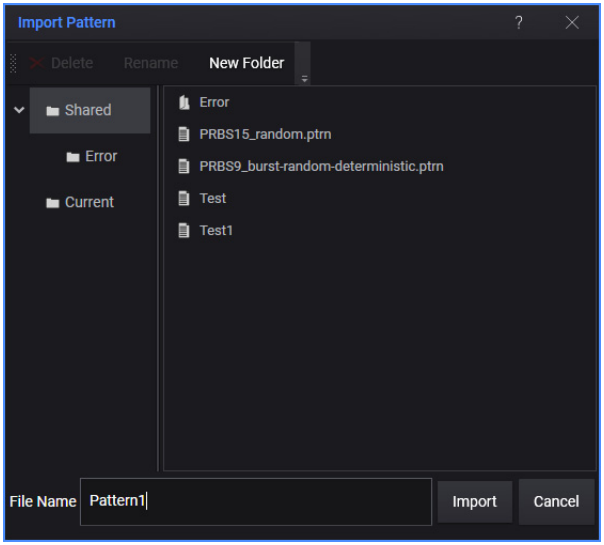
3 If you import a *.ptrn* file, skip the step 4 and go to step 5.

4 However, if you import a *.txt* file, a **Select Import Pattern Properties** dialog will appear:



This dialog allows you to change the pattern coding and enable Squelch and Mask in the pattern.

5 Click **OK**. An **Import Pattern** dialog will appear as shown in the following figure:



6 Choose a location (shared or current) to save the pattern. You can also create a new folder.

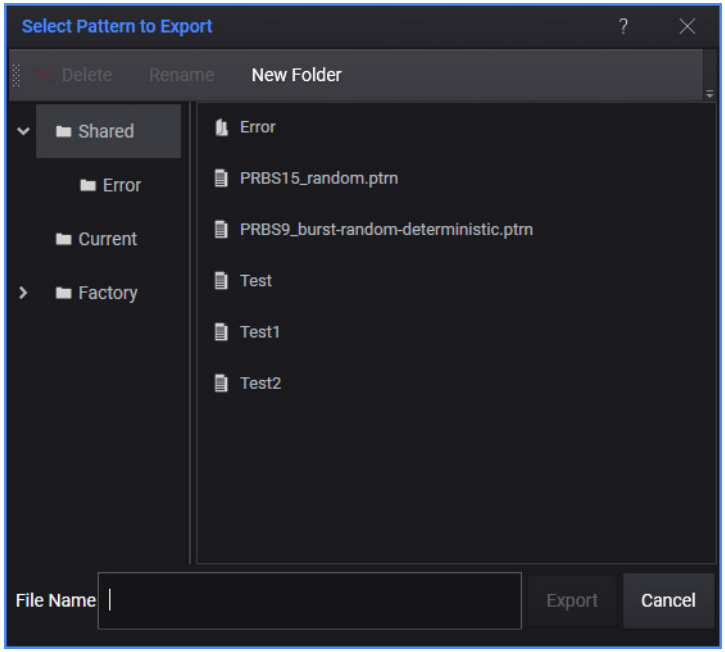
7 Provide a file name and click **Import**. The imported patterns will appear in the **Pattern Edit Pane**.

Exporting Patterns

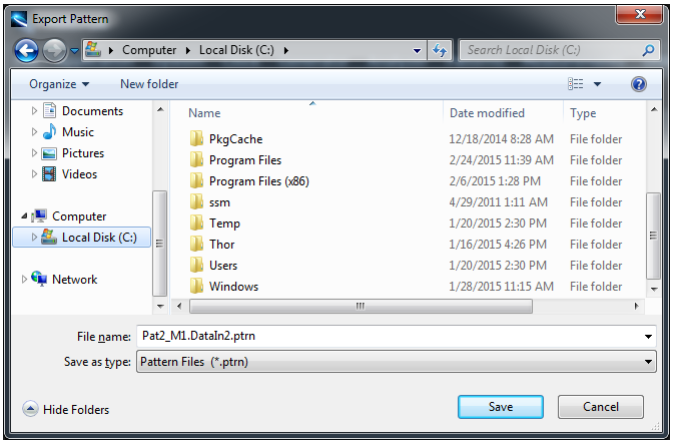
The M8070B **Pattern Editor** allows you to export patterns and use it for testing and analysis.

To export a pattern:

1 Click the **Export** icon. This opens the **Select Pattern to Export** dialog as shown in the following figure:



2 Select the pattern and click **Export**. This opens the **Export Pattern** dialog.



3 Locate the path and file name for the *.prtn* file.

4 Click **Save** to export the data to the specified destination.

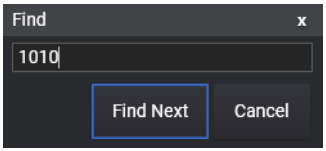
NOTE When naming the pattern file, ensure that the file name does not begin with a number or any special character.

Sharing Patterns

You can share patterns to other users by exporting the pattern to a shared location and later importing that pattern to Pattern Editor. For details on how to export and import patters, refer to Exporting Patterns on page 668 and Importing Patterns on page 666.

Find Symbol Dialog Box

The **Find Symbol** dialog box allows you to search for a specified bit sequence or symbols in the pattern. If you click **Find Next**, the next occurrence of this bit sequence or symbol is highlighted.

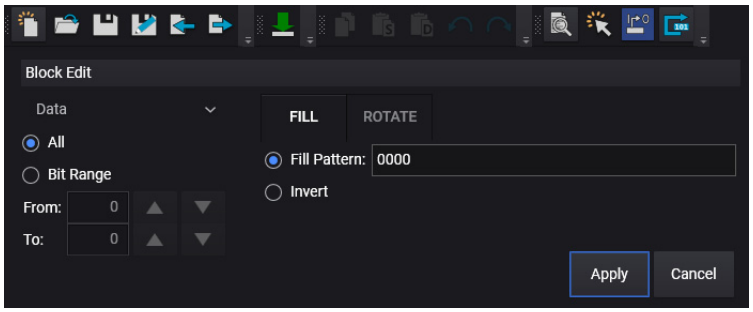


The search pattern can be entered in binary/hex/symbol format, depending on currently selected mode in pattern editor. You can continue editing the pattern while this dialog box is still open.

Block Edit Operations

The **Block Edit** window provides an easy way to modify parts of the pattern or the entire pattern at once. This can be used when setting up a new pattern. It can also be used as an optional technique for editing existing patterns.

Click on the **Block Edit** icon present on the toolbar. The **Block Edit** sliding window will appear as shown in the following figure:



With the **Block Edit** window, you can use the drop-down list to specify whether the block edit operation has to be performed on data or listed attributes. You can also define the range that is to be modified. The available options for the range are:

- **All**

  Choose this option to edit the entire pattern.

- **Range**

  Choose this option to select the range of bits, symbols or blocks entered in the **From** and **To** fields.

The **Block Edit** window contains the following tabs:

- **Fill**

  This tab allows filling the given range in the pattern with the specified value. The available options for the **Fill** tab are:

  - **Fill Pattern**

    Fills the specified value to the given range in the pattern. You can only enter the patterns depending upon the pattern mode (Bit coded or Symbol coded) selected form Data View Mode.

  - **Invert**

    Invert the bits. 0 becomes 1 and 1 becomes 0.

- **Rotate**

  This tab provides the following options:

  - **Rotate Symbol Left by**:

    Treats the pattern data in the specified range as a circular buffer and rotates the bits to the left by the specified amount. No data will be lost and what is at the start of the buffer will be at the end of the buffer after the rotation.

  - **Rotate Symbol Right by**:

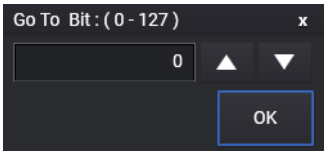
    Treats the pattern data in the specified range as a circular buffer and rotates the bits to the right by the specified amount. No data will be lost and what is at the end of the buffer will be at the start of the buffer after the rotation.

  - **Align to Sequence**:

    Aligns the pattern data in the specified range to a specified pattern sequence.

Go To Bit Dialog Box

The **Go To** dialog box allows you to set the cursor to an arbitrary position in the pattern.



Enter the bit position (=address) or alternatively you can use the UP and DOWN arrow buttons to enter the bit position and then click **OK**. The cursor will be placed in front of the character with the selected bit.

Settings Window

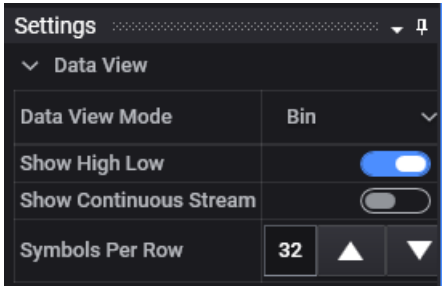
The **Settings Window** allows you to set the visualizations of the currently selected patterns. This helps you to easily identify the data and attributes in the pattern.

The **Settings Window** provides the following options:

Data View

The **Data View** option allows you to set the following:

- **Data View Mode** - Select the data view mode as Bin, Hex, PAM4 No Coding, PAM4 Gray Coding, PAM4 Custom, PAM6 No Coding, PAM6 Custom, PAM8 No Coding and PAM8 Custom coding.
- **Show High Low** - Toggle the ON/OFF switch to display either high or low transition in the patterns. This option is only available in Bit coding.
- **Custom Symbol Mapping** - It appears only when you view the bit pattern as PAM4/6/8 Custom. It allows you to map the consecutive data bits to PAM4/6/8 symbols. The mapping is defined as a comma separated list of bit sequences (e.g. 00, 01, 11, 10).
- **Show Continuous Stream** - Toggle the ON/OFF toggle switch to show continuous stream in the patterns. This option is only available in Bit coding.
- **Symbols Per Row** - Specify a number to view the specified number of symbols in each row.

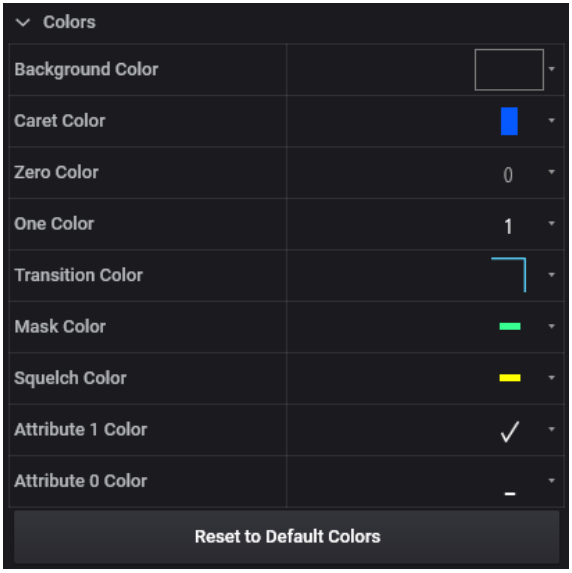


Colors

The **Colors** option allows you to set the following:

- **Background Color** - Changes the background color of the pattern editor pane.
- **Caret Color** - Changes the color of the carat in the pattern.
- **Zero Color** - Changes the color of all occurrences of zeros (0) in the pattern.
- **One Color** - Changes the color of all occurrences of ones (1) in the pattern.
- **Transition Color** - Changes the transition color in the pattern.
- **Mask Color** - Changes the color of the bits that are masked.
- **Squelch Color** - Changes the color of the bits that are squelch.
- **Attribute 1 Color** - Changes the color of attribute 1.
- **Attribute 0 Color** - Changes the color of attribute 0.

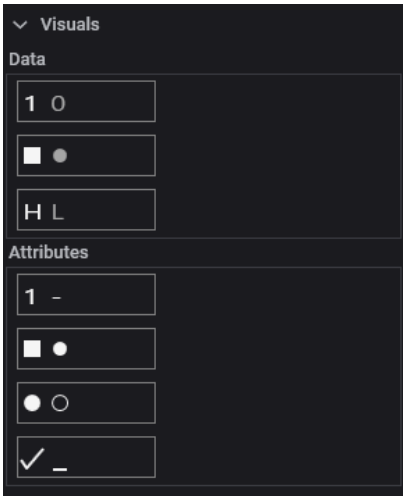
You can at anytime reset the color settings to default colors by pressing the **Reset to Default Colors** button.



Visuals

The **Visual** option allows you to set the following:

- **Data** - Changes the data appearance as selected from the data visual options.
- **Attributes** - Changes the attribute appearance as selected from the attributes visual options.



Pattern Edit Pane

The pattern edit pane displays the pattern and also allows you to edit it.

The pattern edit pane shows the symbol and data. You can edit selected data using the keyboard keys. Remember, the pattern edit pane does not allow you to enter any wrong data.

The pattern edit pane allows you to import and export patterns. For details on how to import and export the patterns, refer to Importing Patterns on page 666 and Exporting Patterns on page 668.

The pattern edit pane also allows you to save the current pattern with other pattern coding. You can right click on the pattern edit pane and use the context menu option (Save As) to save the current pattern or save the selected range of pattern. For details, refer Saving Patterns on page 663.

The pattern edit pane also allows the copy/paste functionality. Once you select the symbols in a pattern, you can copy them and paste it anywhere in the pattern. You can perform the copy/paste operations in the following ways:

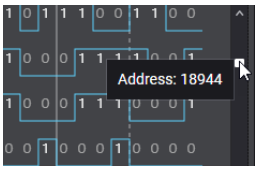
- Click on Copy/Paste icons
- Use keyboard shortcuts (Ctrl+C, Ctrl+V)
- Right click and use the context menu options

Please note that the copy operation only allows a complete symbol to be copied.

It is possible to use the copy/paste operations across multiple instances of Pattern Editor window with same pattern coding.

The pattern edit pane also allows the undo and redo operations. Using this operation you can reverse or restore the last performed action. You can use the keyboard shortcuts (Ctrl+Z) for Undo and (Ctrl+R) for Redo operations.

The pattern edit pane also provides the scrolling feature which can be utilized using the keyboard and mouse. With a keyboard, you can use the up or down arrow keys to move the scrollbar. With a mouse, you can move scroll bar by clicking the scroll arrow at either end of the scroll bars, click empty portions of the scroll bar, or click and drag the scroll box. When you press the scroll bar using the mouse, a tool-tip appears which displays the current position of the symbol number.



Patterns consist of a sequence of symbols. A symbol can have the following type of coding:

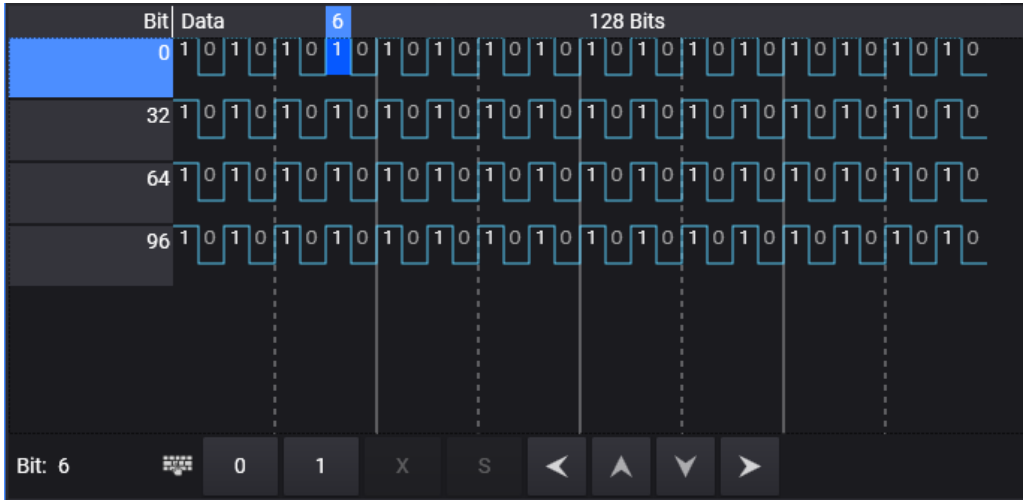
1 Bit (Binary)

2 8B/10B

3 128B/130B

4 128B/132B

The following figure shows the **Pattern Edit Pane** with a bit coded pattern (Binary) pattern:



The bottom of the **Pattern Editor Pane** indicates the position of the selected symbols and buttons to edit them. These buttons are only available when you create a pattern in bit coding and the data view mode is binary (BIN). You can use these buttons to:

0 - Set data 0

1 - Set data 1.

X - Click this toggle button to add/remove mask on a data.

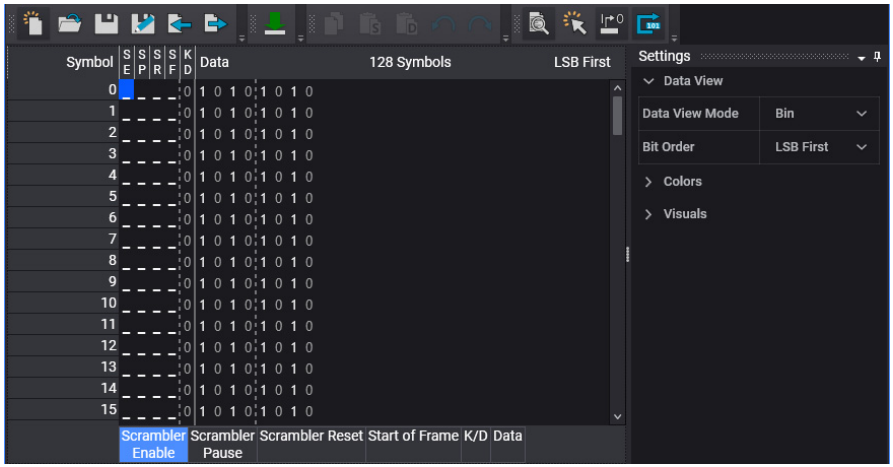
S - Click this toggle button to add/remove squelch on a data.

You can use the buttons as well as the keyboard keys to move the pointer position to the left, right, up and down in the pattern.

In binary mode, when you click on any symbol, its position is displayed as following:

- The top of the **Pattern Editor Pane** displays the index of cursor (symbol) in current row.
- The bottom of the **Pattern Editor Pane** displays the symbol number.

The following figure shows the **Pattern Editor Pane** with a symbol coded (8B/10B) coded pattern:



You can use the **Settings Window** to enhance the visualizations of the current pattern. For details, refer to "Settings Window" on page -672.

Symbol Attributes

A symbol can have additional attributes to modify behavior. They are supported by all symbols. These are:

1 **Mask**: This attribute only affects the **Data In** ports. It specifies if the symbol is actually compared or masked (excluded from compare).

2 **Squelch**: This attribute only affect the **Data Out** ports. If this attribute is 1, a squelch (out of band) level is used.

In addition there are coding specific attributes, to control aspects of the coding like bypassing or using a scrambler.

Editing a Pattern

To edit a pattern:

1 Open an already existing pattern. Refer to Opening Existing Patterns on page 661.

2 If no pattern is available, a new pattern can be created. Refer to Creating New Patterns on page 658.

3 Select the bits to be edited in the patterns.

4 Use the keyboard to enter the required bits. It can be in form of 0 or 1.

5 If the current pattern is in use in some other location(s), then the orange **Download** button will get highlighted when the pattern is modified.

6 Click on the **Download** button to download the pattern. Once it is download, the green **Download** button will appear.

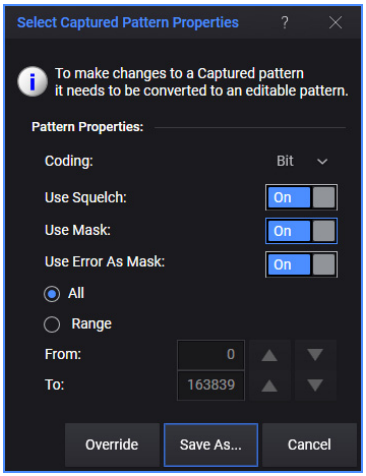
Editing a Captured Pattern

To edit a captured pattern, it needs to be converted to an editable pattern. Follow the given steps make the captured pattern editable:

1 Open an already saved captured pattern. Refer to Opening Existing Patterns on page 661.

2 Select the bits to be edited in the patterns

3 Use the keyboard to enter the required bits. It can be in form of 0 or 1. A **Select Captured Properties** dialog will appear:



4 Change the properties of current pattern. Using this option, you can change the pattern coding and enable/disable **Mask**, **Squelch** and **Error as Mask**.

The **Use Error As Mask** option is only visible when the **Use Mask** option is enabled and coding is same as captured pattern.

5 Click **Override** to remove all errors from the pattern.

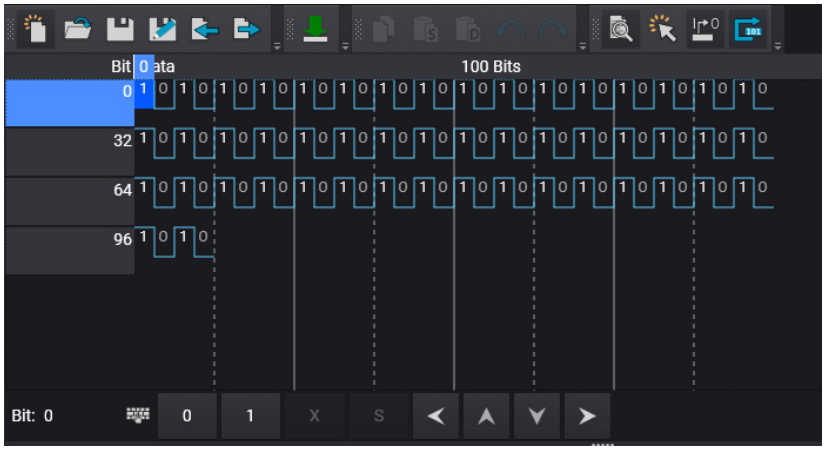
6 Click **Save As**. A **Save Pattern As** dialog will appear.

7 Specify the name and location and click **Save**.

NOTE When naming the pattern file, ensure that the file name does not begin with a number or any special character.

Bit Coding

The following figure shows the pattern edit pane with a bit coded pattern in binary (BIN) mode:



The bottom of the pattern edit pane indicates the position of the selected symbols and buttons to edit them. These buttons are only available when you create a pattern in bit coding and the data view mode is binary (BIN). You can use these buttons to:

0 - Set data 0

1 - Set data 1.

X - Click this toggle button to add/remove mask on a data.

S - Click this toggle button to add/remove squelch on a data.

You can use the buttons as well as the keyboard keys to move the pointer position to the left, right, up and down in the pattern.

The bottom of the pattern edit pane also displays the symbol number which indicates the number.

You can use the **Settings Window** to enhance the visualizations of the current pattern. For details, refer to "Settings Window" on page -672.

To encode a bit coded symbol 1, 2 or 3 bits are needed. This depends on the use of mask and squelch:

Table 62 Plain bit coding without using mask or squelch

Bit offset range	Bit (range) name	Description
0	Data	Data bit

Table 63 Mask is used

Bit offset range	Bit (range) name	Description
0	Data	Data bit
1	Mask	Mask (ignored on DataOut)

Table 64 Squelch is used

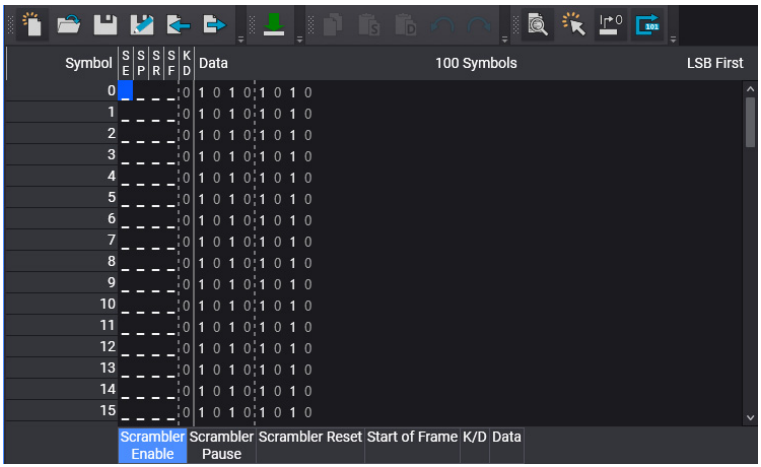
Bit offset range	Bit (range) name	Description
0	Data	Data bit
1	Squelch	Squelch (ignored on DataIn)

Table 65 Mask and Squelch are used

Bit offset range	Bit (range) name	Description
0	Data	Data bit
1	Mask	Mask (ignored on DataOut)
2	Squelch	Squelch (ignored on DataIn)

8B/10B Coding

The following figure shows the pattern edit pane with a 8B/10B coded pattern:



You can use the **Settings Window** to enhance the visualizations of the current pattern. For details, refer to Settings Window on page 672.

This type of pattern contain:

- **Symbol**: 8B/10B coding have 8 bits in one symbol.
- **Attributes**: It has the following attributes:
  - **Mask** - This attribute only affects the **Data In** ports.
  - **Squelch** - This attribute only affects the **Data Out** ports.
  - **Scrambler Enable** - This attribute enables/disables the scrambler.
  - **Scrambler Pause** - This attribute is used to pause scrambler for some special symbol.
  - **Scrambler Reset** - This attribute is used to reset scrambler LFSR (Linear feedback shift register).
  - **Start of frame** - This attribute enables/disables the start of frame marker.
  - **K/D** - This attribute specifies whether the symbol bits are control characters or data.
- **Data** - Specifies data bits.

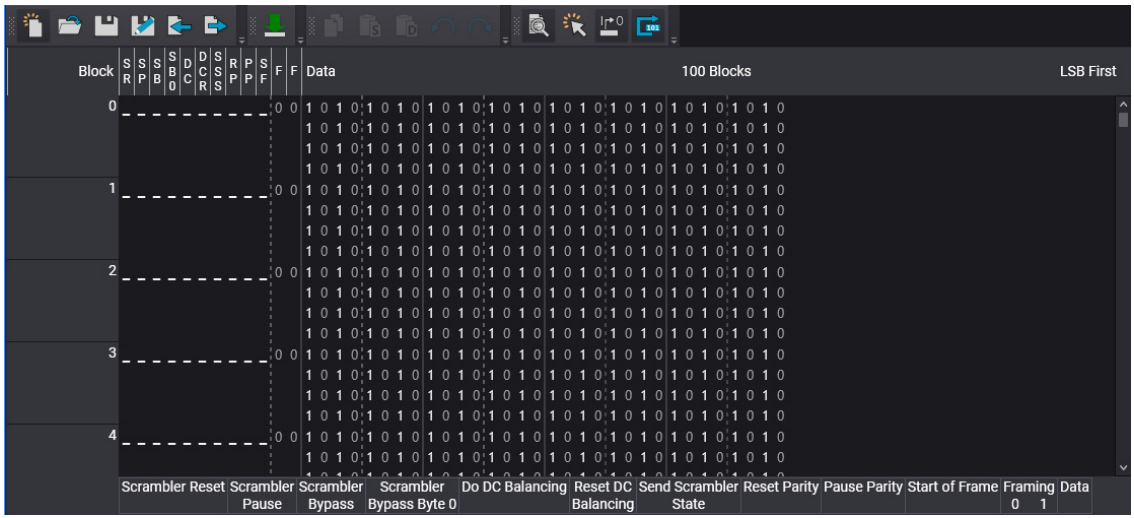
To encode an 8B/10B symbol, 16 bits (2 bytes) are used:

Table 66

Bit offset range	Bit (range) name	Description
7:0	Data	Symbol data
8	K/D	0 = D-character, 1 = K-character
9		Reserved for future use. Must be set to 0
10	Mask	Mask (if present, ignored on DataOut)
11	Squelch	Squelch (if present, ignored on DataIn)
12	Enable Scrambler	Enable Scrambler (ignored on DataIn)
13	Pause Scrambler	Pause Scrambler (ignored on DataIn)
14	Reset Scrambler	Reset Scrambler (ignored on DataIn)
15	Start of Frame	Start of Frame (ignored on DataOut)

128B/130B Coding

The following figure shows the pattern edit pane with a 128B/130B coded pattern:



You can use the **Settings Window** to enhance the visualizations of the current pattern. For details, refer to Settings Window on page 672.

This type of pattern contain:

- **Symbol**: 128B/130B coding having 128 bit in one symbol.
- **Attributes**: It has the following attributes:
- **Mask** - This attribute only affects the **Data In** ports.
- **Squelch** - This attribute only affects the **Data Out** ports.
- **Scrambler Enable** - This attribute enables/disables scrambler.
- **Scrambler Pause** - This attribute is used to pause the scrambler for some special symbol.
- **Scrambler Reset** - This attribute is used to reset the scrambler LFSR (Linear feedback shift register).
- **Scrambler Bypass** - This attribute is used to bypass the scrambling over the symbol.
- **Scrambler Bypass Byte 0** - If this bit is enabled, it does not allow scrambling over the symbol.

  - **Do DC Balancing** - This attribute is used to set DC balancing over symbol.
  - **Reset DC Balancing** - This attribute resets the DC balancing state.
  - **Send Scrambled State** - This attribute specifies whether to send the scrambled state.
  - **Reset Parity** - This attribute is used to reset the parity bit.
  - **Pause Parity** - This attribute is used to pause the parity bit.
  - **Start of frame** - This attribute enables/disables the start of frame marker.
  - **Framing** - This attribute enables/disables the start of frame marker.
- **Data** - Specifies the data bits.

To encode a 128B/130B symbol, 144 bits (18 bytes) are used:

Table 67

Bit offset range	Bit (range) name	Description
1:0	Framing	Framing bits
129:2	Data	Data
130	Mask	Mask (if present, ignored on DataOut)
131	Squelch	Squelch (if present, ignored on DataIn)
132	Reset Scrambler	Scrambler reset (ignored on DataIn)
133	Pause Scrambler	Scrambler pause (ignored on DataIn)
134	Bypass Scrambler	Scrambler bypass
135	Bypass Byte 0 Scrambler	Scrambler bypass byte 0
136	Do DC Balancing	Do DC balancing (ignored on DataIn)
137	Reset DC Balancing	Reset DC balancing (ignored on DataIn)
138	Send Scrambler State	Send scrambler state (ignored on DataIn)
139	Reset Parity	Reset Parity (ignored on DataIn)

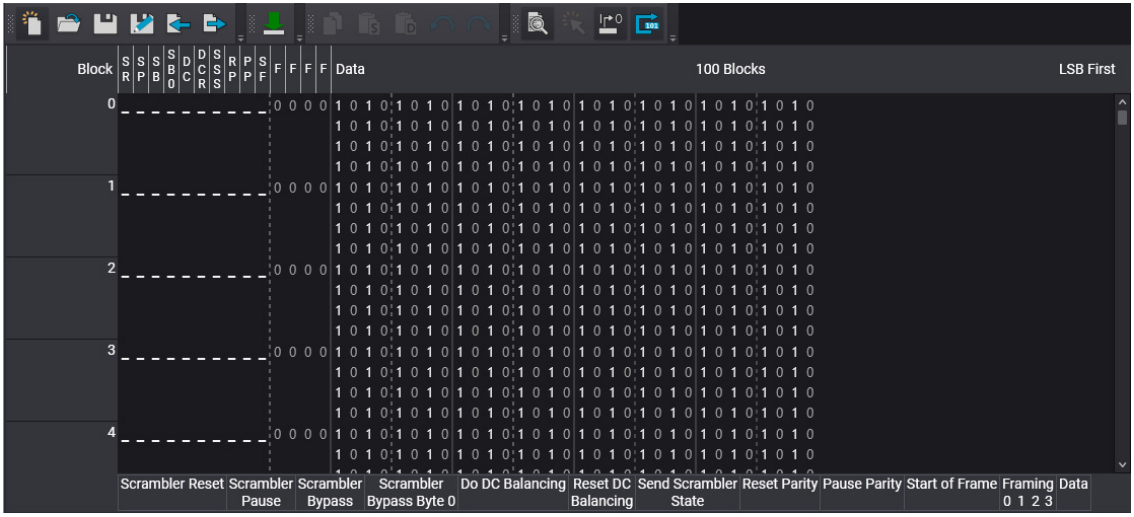
Bit offset range	Bit (range) name	Description
140	Pause Parity	Pause Parity (ignored on DataIn)
141	Start of Frame	Start of Frame (ignored on DataOut)
143:142		Reserved for future use. Must be set to 0

NOTE

When using 128/130 coding pattern contains Sync Symbols to achieve Symbol Alignment. These Sync Symbols need to be at least 16 symbols apart.

128B/132B Coding

The following figure shows the pattern editor pane with a 128B/132B coded pattern:



You can use the **Settings Window** to enhance the visualizations of the current pattern. For details, refer to Settings Window on page 672.

This type of pattern contain:

- **Symbol**: 128B/132B coding having 128 bit in one symbol.
- **Attributes**: It has the following attributes:
  - **Mask** - This attribute only affects the **Data In** ports.
  - **Squelch** - This attribute only affects the **Data Out** ports.
  - **Scrambler Reset** - This attribute is used to reset the scrambler LFSR (Linear feedback shift register).
  - **Scrambler Pause** - This attribute is used to pause the scrambler for some special symbol.
  - **Scrambler Bypass** - This attribute is used to bypass the scrambling over the symbol. If this bit is enabled, it will not allow scrambling over the symbol.
  - **Scrambler Bypass** Byte 0 - If this bit is enabled, it does not allow scrambling over the symbol.
  - **Do DC Balancing** - This attribute is used to set DC balancing over the symbol.
  - **Reset DC Balancing** - This attribute resets the DC balancing state.
  - **Send Scrambled State** - This attribute specifies whether to send the scrambled state.
  - **Reset Parity** - This attribute is used to reset the parity bit.
  - **Pause Parity** - This attribute is used to pause the parity bit.
  - **Start of frame** - This attribute enables/disables the start of frame marker.
  - **Framing 0 1 2 3** - This attribute enables/disables the start of frame marker.
- **Data** - Specifies the data bit.

You can edit selected data using the keyboard.

To encode a 128B/132B symbol, 144 bits (18 bytes) are used:

Table 68

Bit offset range	Bit (range) name	Description
3:0	Framing	Framing bits
131:4	Data	Data
132	Mask	Mask (if present, ignored on DataOut)
133	Squelch	Squelch (if present, ignored on DataIn)

Bit offset range	Bit (range) name	Description
134	Reset Scrambler	Scrambler reset (ignored on DataIn)
135	Pause Scrambler	Scrambler pause (ignored on DataIn)
136	Bypass Scrambler	Scrambler bypass
137	Bypass Byte 0 Scrambler	Scrambler bypass byte 0
138	Do DC Balancing	Do DC balancing (ignored on DataIn)
139	Reset DC Balancing	Reset DC balancing (ignored on DataIn)
140	Send Scrambler State	Send scrambler state (ignored on DataIn)
141	Reset Parity	Reset Parity (ignored on DataIn)
142	Pause Parity	Pause Parity (ignored on DataIn)
143	Start of Frame	Start of Frame (ignored on DataOut)

NOTE

When using 128/132 coding pattern contains Sync Symbols to achieve Symbol Alignment. These Sync Symbols need to be at least 16 symbols apart.

Pattern Capture

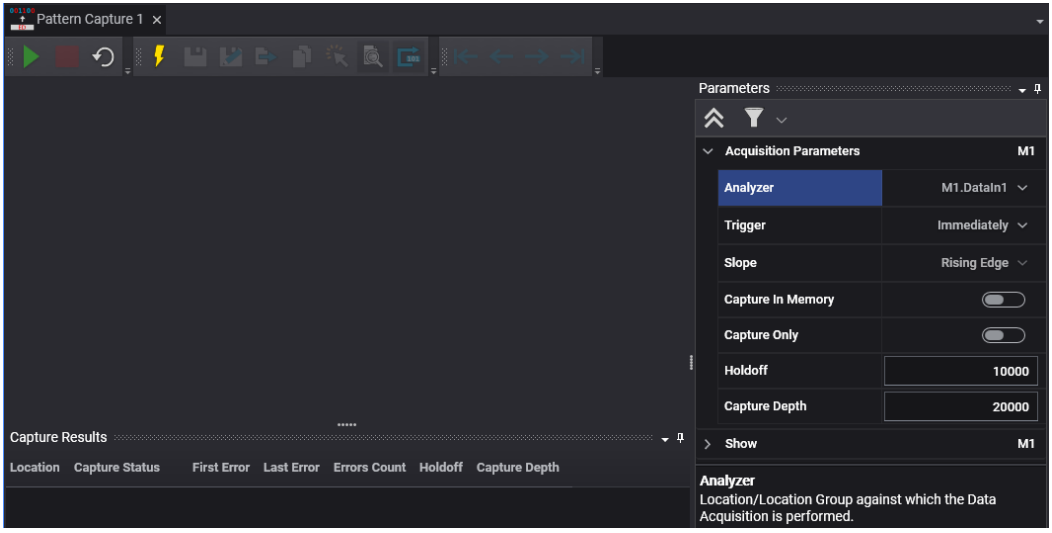
The M8020A/M8040A/M8050A Analyzer captures the data received from the device under test. The captured data bits are displayed in the pattern capture pane in binary or 8b/10b symbol coding. The received data is compared with the expected data and the errored bits/symbols are highlighted. The captured data can be saved for post processing.
The maximum capture memory for M8041A, M8051A and M8046A is 2 Gb and for M8062A is 1 Gb. However, it also depends on the holdoff length which represents the amount of symbols in which the trigger events will be ignored.

How to Launch Pattern Capture Window

To launch the **Pattern Capture** window:

- Go to the **Menu Bar** > **Patterns** and then select **Pattern Capture**.

The **Pattern Capture** window will appear as shown in the following figure:



The **Pattern Capture** window includes the following elements:

- Toolbar
- Pattern Captured Pane
- Captured Results
- Parameters Window

Toolbar

The toolbar provides the following convenient pattern capture functions:

Table 69

Elements	Name	Description
	Start	Starts capturing the current pattern
	Stop	Stops capturing the current pattern
	Reset	Resets the values of acquisition parameters
	Manual Trigger	Manually starts the event that is triggering the capture logic.
	Save Captured Data	Opens the “Save As” dialog which allows to save the captured data patterns as a separate pattern in the workspace (shared/current). Use this option to save the data and the error information. The data is saved as a sequence of one data bit and one error/compared bit. This option enables you to save the captured pattern and view it later, along with the error information (errored bits). This option is applicable only when the 'Capture Only' parameter in the Pattern Capture measurement is set to OFF.
	Save As	Click this icon to change the properties of current pattern and then save it under different name. For details, refer to Saving Patterns on page 663. Use this option to save only the captured data bits, without saving any errored bits information. Additionally, you can use this option to change the pattern properties, such as adding mask/squelch, saving in different encoding, and setting up the range.
	Export	Click this icon to export patterns in the desired location. These patterns can be used by other instruments for testing and analysis. For details, refer to Exporting Patterns on page 668.

Elements	Name	Description
	Copy	Copies the selected data. (Ctrl +A)
	Select All	Click this icon to select all the symbols in the pattern.
	Find	Click this icon to open the Find Symbol dialog box and perform the search operation for a specified segment in the pattern. For details, see Find Symbol Dialog Box on page 669.
	Go To	Click this icon if you want to jump to an arbitrary bit position. See Go To Bit Dialog Box on page 671.
	Error Navigation Buttons	▪ First Error - Takes to the first errored bit in the captured pattern. ▪ Previous Error - Takes to the previous errored bit before the current one in the captured pattern. ▪ Next Error - Takes to the next errored bit after the current one in the captured pattern. ▪ Last Error - Takes to the last errored bit in the captured pattern.

Parameters Window

The **Parameters** window have the following acquisition and show parameters for pattern capture.

Acquisition Parameters

- **Analyzer** - Use this drop-down menu to select the channel against which the data capture has to be performed.
- **Trigger** -Selects the event that is triggering the captured logic. It can be captured on the following four stop events:
  - **Immediately** – Starts capturing the data immediately and displays the captured data.
  - **Error** – Starts capturing the data when it receives an errored bit and displays the captured data.
  - **CTRL IN A** – Waits for a trigger signal from CTRL IN A port and displays the captured data.

  - **CTRL IN B** – Waits for a trigger signal from CTRL IN B port and displays the captured data.
- **Slope** - Selects the edge (rising edge or falling edge) of CTRL IN A or CRL IN B that is triggering the captured logic.
- **Capture In Memory** - Enables you to capture and save the data into system's memory and helps in performance optimization.
  - When the **Capture In Memory** toggle button is **On**, the system saves the data into the internal memory only.
  - When the **Capture In Memory** toggle button is **Off**, the system saves the data into the external hard drive.
- **Capture Only** - Enables you to capture data without comparison.
  - When the **Capture Only** toggle button is **On**, the system captures the data but does not compare to verify if the bit is errored or not.
  - When the **Capture Only** toggle button is **Off**, the system captures the default data.
- **Holdoff** - Defines the minimum of data bits to capture before the trigger event occurs. This value is adjusted to a multiple of the current symbol granularity.
- **Capture Depth** - Defines the minimum of data bits to capture including holdoff. This value is adjusted to a multiple of the current symbol granularity.

Show Parameters

- **View Coded Pattern As** - Displays the coded pattern (8B/10B) in Binary, Hex or Symbol view.
- **View Bit Pattern As** - Displays the captured bit coed pattern in Binary, Hex, PAM3, PAM4 No Coding, PAM4 Gray Coding and PAM4 Custom coding.
- **Symbols Per Row** - Displays the Symbols per row in Binary, Hex, PAM4-No Coding, PAM4-GRAY Coding, and PAM4-Custom view.
- **Custom Symbol Mapping** - It appears only when you view the bit pattern as PAM4 Custom. It allows you to map the consecutive data bits to PAM4 symbols. The mapping is defined as a comma separated list of bit sequences (e.g. 00, 01, 11, 10).

How to Capture a Pattern

The following example explains the steps to capture a pattern to display errored bits.

1 Switch to **Parameters** window.

2 Set the acquasation parameters are shown below:

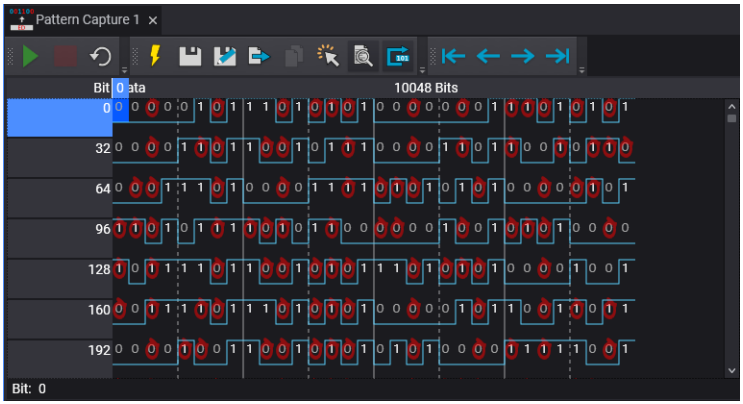
- Location: *M1.DataIn1*
- Trigger: *Error*
- Holdoff: *500*
- Capture Depth: *10000*

3 Click **Start** button. A message “Waiting for Trigger” will appear. You can click **Manual Trigger** to manually trigger the captured logic.

4 The captured data will be displayed in the **Pattern Captured** pane. The errored bits are marked red as shown in the following figure:

Pattern Capture Pane

The **Pattern Capture Pane** displays the captured pattern in the binary or 8b/10b symbol coding.



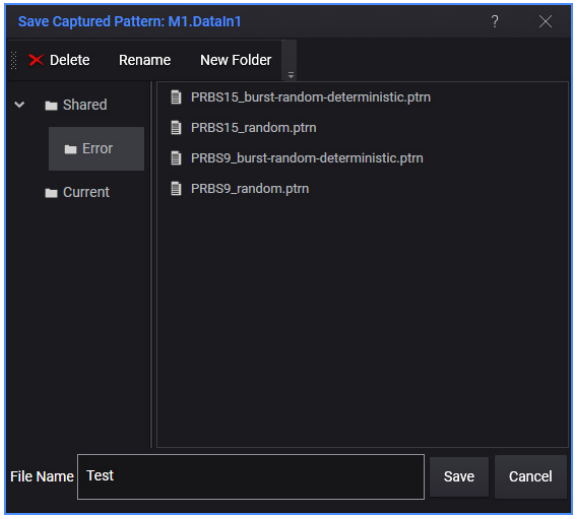
The errored bits in the captured patterns are marked red. You can use the **Error Navigation** buttons to jump to next, previous, first or last error.

Please note that the **Pattern Capture** pane does now allow to editing feature. This means you cannot edit the captured pattern. However, if you want to edit a captured pattern, you have to first save it and then open in the **Pattern Editor**. For details on how to edit pattern, refer to Editing a Pattern on page 677. Using a **Pattern Editor**, you can also save the results in different encoding schemes.

Saving a Captured Pattern

You can save the captured pattern for post processing. To do so;

- Click **Save** icon. This will open a **Save Captured Pattern** dialog.

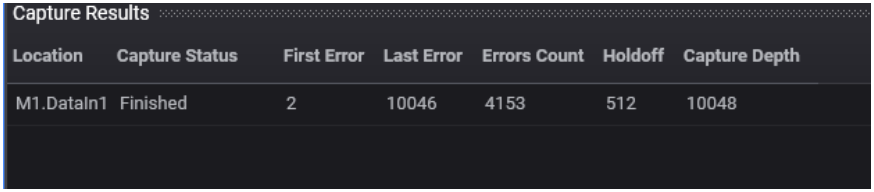


- Specify the folder where it will be saved.
- Enter a file name and click **Save**. The current pattern will be saved under the filename.

You can open the saved file it in the **Sequence Editor** and then download it to module to create a sequences. For details, refer to Sequence Editor on page 613.

Capture Results Pane

The **Capture Results** pane displays the results of the patterns captured.



The results are summarized as following:

- **Location** - Displays the location on which pattern capture is performed.
- **Capture Status** - Displays the current status of the capturing event as ‘Finished’, ‘Stopped’ or ‘Waiting for Trigger’.
- **First Error** - Displays the position of first error bit.
- **Last Error** - Displays the position of last error bit.
- **Errors Count** - Displays the total number of errored bits.
- **Holdoff** - Displays the minimum number of data bits to capture before the trigger event occurs.
- **Capture Depth** - Displays the minimum number of data bits to capture including holdoff.

M8070B Pattern Capture Export Format

The M8070B Pattern Capture feature allows you to capture patterns of data and compare them with expected results. When exporting the captured data, there are two possible formats used based on whether errors were detected. Below is the explanation of how the export file is structured for various cases, including error-free captures, captures with errors, and when mask bits are involved.

Data Viewed as Binary and Hex

1 Error-Free Data

If the captured pattern is error-free, the exported data in the .ptrn file will contain twice the number of bits as captured. Each bit will be followed by an additional bit to indicate whether it is error-free or not. If the Data is viewed as Hex, and we export the captured pattern, it will be exported as Bit.

Example:

- Captured data: 11001100 10101010
- Exported file (binary): 1010000010100000100010001000 (updated)

2 Data with Errors

If the captured pattern contains errors, the exported data will include twice the number of bits as captured. Each bit will be followed by an additional bit to indicate whether it is error-free or contains an error.

- 0 indicates no error (the bit is error-free).
- 1 indicates an error.

Example:

- Captured data: 1100110010101010
- Error in the 3rd bit and the 7th bit.
- Exported file (binary with error indicators): 1010010010100100100010001000 (updated)
- The 3rd and 7th bits are followed by 1, indicating errors.

3 Data with Mask Bits

If mask bits are used in the capture, these will be included in the exported data. Masked bits are treated as “don't care” bits and typically are not compared against the expected pattern and will not be included in the exported pattern file.

Data Viewed as 8b/10b Symbols

1 Error-Free Data

- When viewing the captured data as 8b/10b symbols (which are typically used in high-speed data transmission systems), error-free data will be exported in the form of the bit sequence.
- Each symbol corresponds to an 8-bit data word encoded into a 10-bit transmission format.

Example:

- Captured 8-bit data: 11001100
- Exported as 8b/10b symbol: K28.5

2 Data with Errors

- For captured data with errors, each 8b/10b symbol will be followed by an error indicator. The format will be similar to the binary and hex cases, where 0 represents an error-free symbol and 1 indicates an error.

Example:

- Captured 8-bit data: 11001100
- Error in the 3rd bit.
- Exported file (8b/10b symbols with error): K28.5, error

3 Data with Mask Bits

- Mask bits in the 8b/10b symbols will be indicated similarly to the binary and hex formats, where X or a specific placeholder may be used to denote masked positions.

Example:

- Captured data with mask: 11001100 10101010
- Mask applied on the 5th and 8th positions.
- Exported file (8b/10b symbols with mask): K28.5, masked

Interactive Link Training

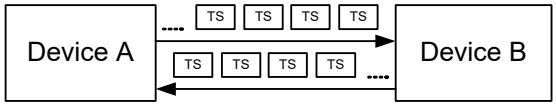
PCI Express 3.0/4.0 Testing

Interactive link training is required for link equalization testing as outlined in the PCI Express (R) Architecture PHY Test Specification.

LTSSM (Link Training and Status State Machine)

Link Training and Status State Machine (LTSSM) is the sub-block that drives and controls the link initialization, and training process for a PCIe device to enable the normal data exchange between the two devices over the link. LTSSM operates at the physical layer level and exchanges physical layer packets (Ordered sets such as TS1 and TS2) to initialize, train, and manage the link.

Two PCIe 3.0/4.0 instruments exchange Training Sequences as shown in the following diagram:



Training Sequences are also used to switch the link to low power states.

LTSSM States

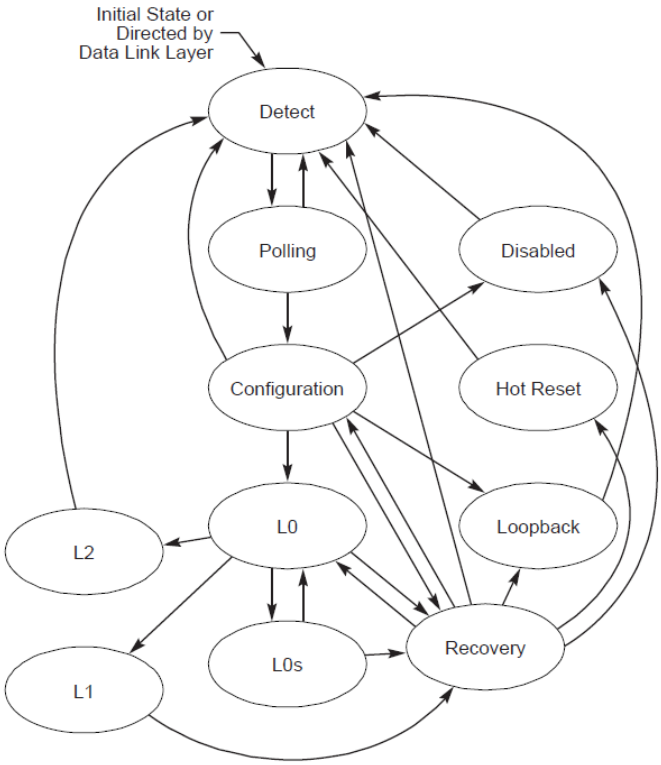
LTSSM transits through various states and sub states during link initialization, training, and management. The entry and exit of each of these states and the exchange of packets (Ordered sets) between the two devices during each state is as per the PCIe specifications.

As per the PCIe specifications, LTSSM has 11 states and further sub-states. These states are referred to frequently in this chapter to describe LTSSM testing using the Keysight LTSSM Tester tool. Following is a list of these states followed by a diagram to illustrate the sequence of these states as per the PCIe specifications.

- Detect
- Quiet
- Polling
- Configuration
- L0
- Recovery

- L0s
- L1
- L2
- Hot Reset
- Disabled
- Loopback

The following figure displays the top-level states of LTSSM.



The Link Training starts in state “Detect”. The purpose of this state is to detect when a far end termination is present. In the “Polling” state, bit lock and Symbol lock are established and Lane polarity is configured. In “Configuration”, both the Transmitter and Receiver are sending and receiving data at the negotiated data rate. In “Recovery”, both the Transmitter and Receiver are sending and receiving data using the

configured Link and Lane number as well as the previously supported data rate(s). An active link that can transport transaction layer packets is in state “L0”. All power management states are entered from this state.

The intent of the “Disabled” state is to allow a configured Link to be disabled until directed or Electrical Idle is exited (i.e., due to a hot removal and insertion) after entering “Disabled”. The “Loopback” is intended for test and fault isolation use.

LTSSM Tests for PCIe 3.0/4.0

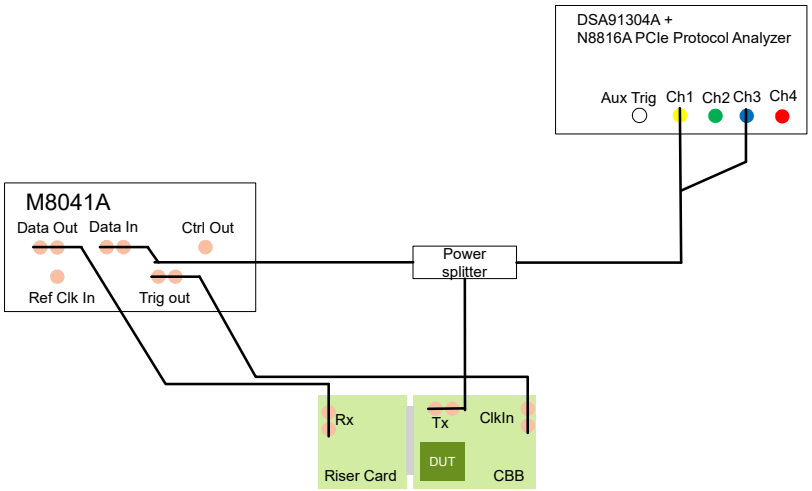
You can execute the following types of LTSSM tests for PCIe 3.0/4.0:

Table 70

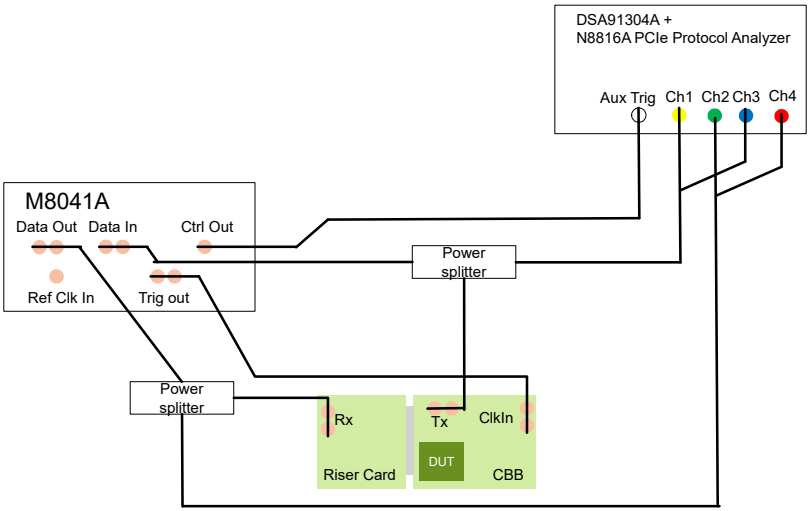
Test Number	Test Name
2.3	Add-in Card Transmitter Initial Tx EQ Test for 8.0GT/s
2.4	Add-in Card Transmitter Link Equalization Response Test for 8GT/s
2.7	System Board Transmitter Link Equalization Response Test for 8GT/s
2.10	Add-in Card Receiver Link Equalization Test for 8GT/s
2.11	System Board Receiver Link Equalization Test for 8GT/s

Test Setup

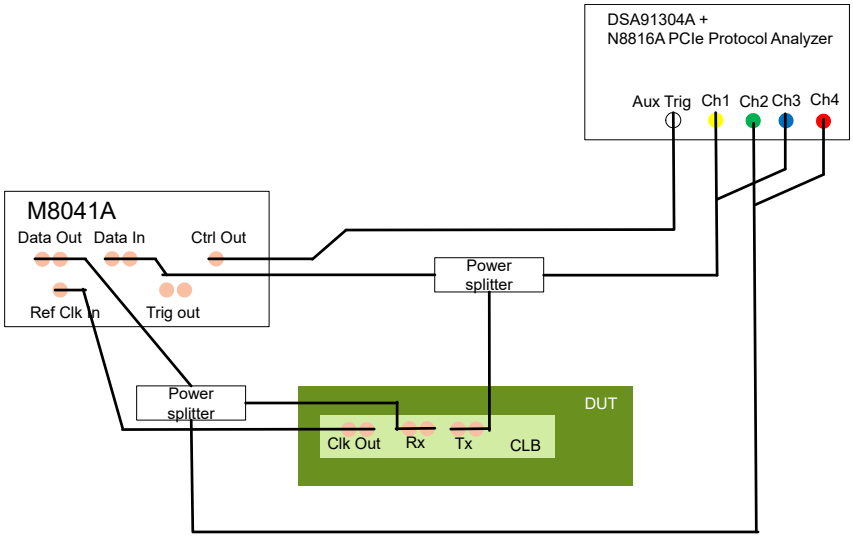
The following block diagram shows the setup for test 2.3:



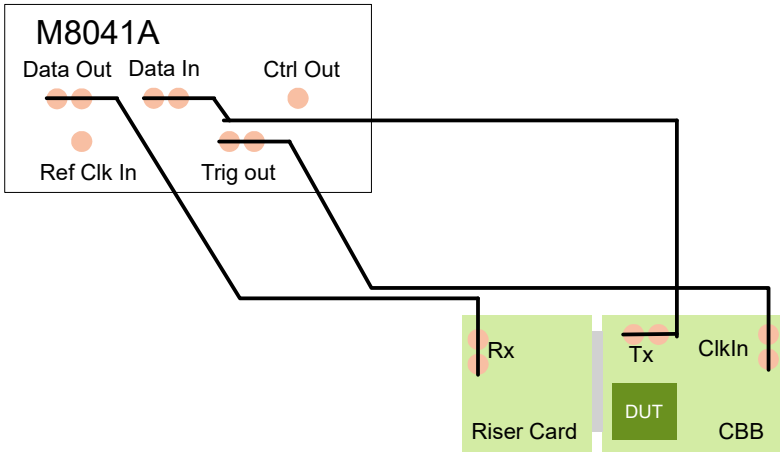
The following block diagram shows the setup for test 2.4:



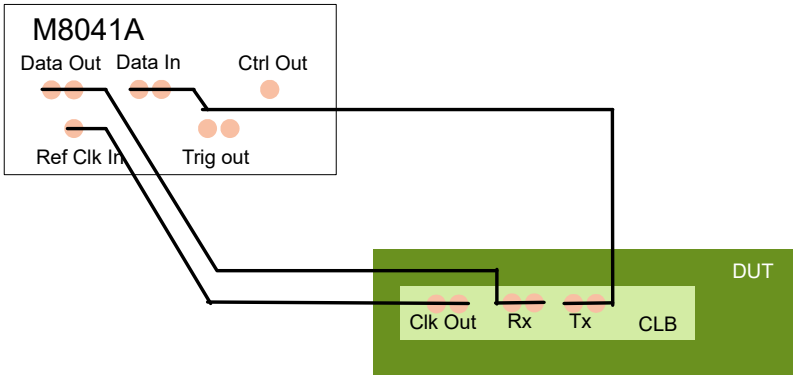
The following block diagram shows the setup for test 2.7:



The following block diagram shows the setup for test 2.10:



The following block diagram shows the setup for test 2.11:



M8070B support for PCIe3.0/4.0 link training using M8020A

Refer the section Link Training Configuration on page 625 for the PCIe 3.0 and PCIe 4.0 parameters which are added to pattern sequence language for specifying certain values to configure the LTSSM.

Link Training Configuration

You can configure the link training parameters to control LTSSM using the **Sequence Settings** window. For details on link training parameters, refer to Link Training Configuration on page 625.

Test Procedure

Follow the given steps to perform link training for test 2.3:

1 In the M8070B software load the instrument state **PCIe_PHY2.3_Test**.

2 Power on the DUT.

3 Enable the **Outputs** of the M8041A.

4 Reset the DUT by pressing the reset button on the CBB.

5 With this setup everything is prepared for capturing the data for the P0 preset. Hit the **Break** button in the **Sequence Editor** to start the link training. If link training was successful the **Status Indicator** should show that the sequencer of the generator is executing block 4 or 5 and that there are no bit errors.

6 Set up the oscilloscope.

7 For shutting down the PCIe link hit the **Break** button again. The sequencer of the generator should return to block 2.

8 Before taking the measurement for P1 the test pattern has to be changed. For this select block 4 of the generator sequence. Under **Sequence Settings** > **Block Data** change the memory pattern to compliancePatternHeaderP1Lane0. This pattern can be found in the **Current** directory. Not changing the pattern will cause the SIG test software to show the wrong preset number, but won't affect the test results otherwise.

9 Do the same for block 4 of the error detector sequence.

10 Under **Sequence Settings** > **Instrument Configuration** > **Link Training PCIe** (3.0 or 4.0) and change the **DUT Initial Preset** to P1.

11 Download the changed sequence.

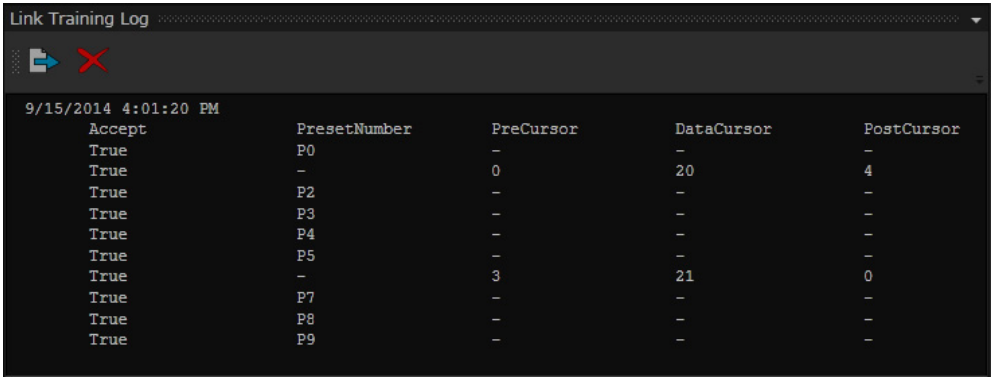
12 Repeat the test as for P0 and then repeat the test procedure for P2 through P9.

13 Start the SIG software and load all captured files into the **Preset Test**.

Link Training Log

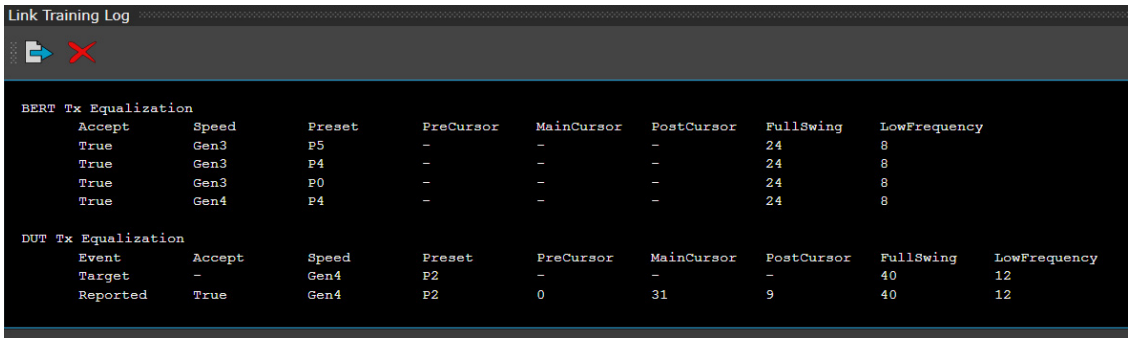
The **Link Training Log** window displays the log generated while initiating the link training test. All information regarding the executed tests and their status are displayed with the date and time stamp. This helps to identify the root cause of a problem. For instance, the **Link Training Log** shows test failure due to an unexpected LTSSM state change.

The following figure shows the log generated by the link training test for PCIe 3.0.



Accept	PresetNumber	PreCursor	DataCursor	PostCursor
True	P0	–	–	–
True	–	0	20	4
True	P2	–	–	–
True	P3	–	–	–
True	P4	–	–	–
True	P5	–	–	–
True	–	3	21	0
True	P7	–	–	–
True	P8	–	–	–
True	P9	–	–	–

The following figure shows the log generated while initiating the link training test for PCIe 4.0:



You can open/close the **Link Training Log** window by clicking on the **Show/Hide Link Training Log** icon present in the status bar. The **Show/Hide Link Training Log** icon with orange background indicates an update or new entry in the link training log.

User Calibrated Presets

It specifies whether BERT's Data Out should use user-calibrated presets or standard presets during link training. Turning it on means that BERT's Data Out will use deemphasis/pre-shoot values that had been previously calibrated, otherwise it will use standard deemphasis/pre-shoot values defined by the PCIe specification (defined below). By default this option is turned off which means that standard presets will be used.

The following table shows standard preset from PCIe specification:

Preset Number	Deemphasis (dB)	Preshoot (dB)
P0	-6.0	0.0
P1	-3.5	0.0
P2	-4.5	0.0
P3	-2.5	0.0
P4	0.0	0.0
P5	0.0	1.8

P6	0.0	2.5
P7	-6.0	3.5
P8	-3.5	3.5
P9	0.0	3.5

M8070B support for USB 3.2 Gen 1/USB 3.2 Gen 2 link training using M8020A/M8040A/M8050A

The M8020A/M8040A/M8050A system allows you to test the physical layer compliance of a USB 3.2 Gen 1 (SuperSpeed) and USB 3.2 Gen 2 (SuperSpeedPlus) DUT.

It provides the following types of testing:

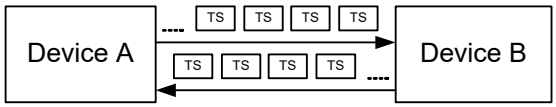
- Transmitter Testing for USB 3.2 Gen 1/USB 3.2 Gen 2
- Receiver Jitter Tolerance Testing for USB 3.2 Gen 1/USB 3.2 Gen 2

The M8070B software provides the parameters which can be configured for link training USB 3.2 Gen 1 and USB 3.2 Gen 2.

LTSSM (Link Training and Status State Machine)

Link Training and Status State Machine (LTSSM) is the sub-block that drives and controls the link initialization, and training process for a USB device to enable the normal data exchange between the two devices over the link. LTSSM operates at the physical layer level and exchanges physical layer packets (Ordered sets such as TS1 and TS2) to initialize, train, and manage the link.

Two USB 3.2 Gen 1/USB 3.2 Gen 2 instruments exchange Training Sequences as shown in the following diagram:



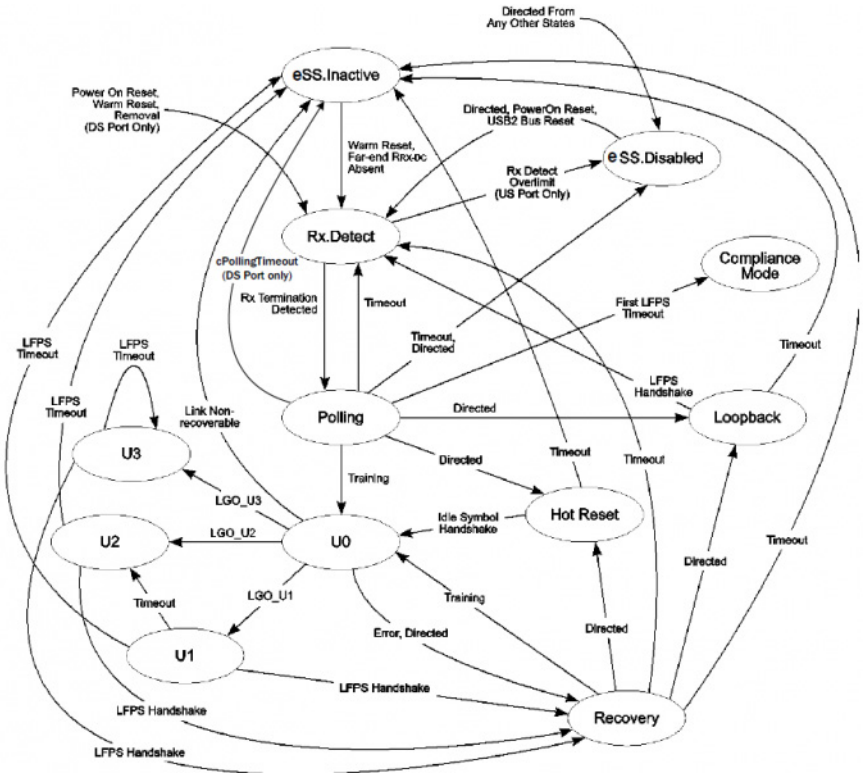
Training Sequences are also used to switch the link to low power states.

LTSSM States

LTSSM transits through various states and sub-states during link initialization, training, power management and error testing. The entry and exit of each of these states and the exchange of packets (Ordered sets) between the two devices during each state is as per the USB specifications.

LTSSM consist of 12 main link states and their sub-states. These states and sub-states are responsible for link initialization, training, power management and error testing.

The following figure displays the top-level states of LTSSM.



The USB 3.2 Gen 1 and USB 3.2 Gen 2 LTSSM consists following states and their sub-states:

1 **Rx.Detect** - Rx.Detect is the power on state of the LTSSM for both a downstream port and an upstream port. It is also the state for a downstream port upon issuing a Warm Reset, and the state for an upstream port upon detecting a Warm Reset from any other link state except eSS.Disabled. The purpose of Rx.Detect is to detect the impedance of far-end receiver termination to ground.

   It contains three sub-states:

   - **Rx.Detect.Reset** - Rx.Detect.Reset is a default reset state used by the two ports to synchronize the operation after a Warm Reset; this substate exits immediately if Warm Reset is not present.
   - **Rx.Detect.Active** - Rx.Detect.Active is a sub-state for far-end receiver termination detection.
   - **Rx.Detect.Quiet** - Rx.Detect.Quiet is a power saving sub-state in which the function of a far-end receiver termination detection is disabled. A port will perform the far-end receiver termination detection periodically during Rx.Detect.

2 **Polling** - Polling is a state for port capability negotiation and link training. During Polling, a Polling.LFPS handshake shall take place between the two ports in SuperSpeed operation before the link training is started. Similarly for SuperSpeedPlus operation, Polling.LFPS based SCD1/SCD2 handshakes, LBPM based port capability negotiation and match, and subsequent port configuration shall take place before SuperSpeedPlus link training is started. Bit lock, block alignment for SuperSpeedPlus operation, symbol lock, lane polarity inversion, and Rx equalization trainings are achieved using TSEQ, SYNC, TS1, and TS2 training ordered sets.

   It contains the following sub-states:

   - **Polling.LFPS** - Polling.LFPS is a substate designed to establish the PHY's DC operating point, and to synchronize the operations between the two link partners after exiting from Rx.Detect. This is also a substate for a port to identify itself based on various Polling.LFPS signatures.
   - **Polling.LFPSPlus** - Polling.LFPSPlus is a substate where the port SuperSpeedPlus operation performs SCD2 handshake, for additional confirmation of the SuperSpeedPlus capability of its link partner.
   - **Polling.PortMatch** - Polling.PortMatch is a substate where the two ports in SuperSpeedPlus operation perform the LBPM handshake, for announcing, matching, and deciding the operation on the highest common capability between the two link partners.

- **Polling.PortConfig** - Polling.PortConfig is a substate where a port configures its PHY according to PHY Capability LBPM matched in Polling.PortMatch, and synchronizes with its link partner in exiting from this substate to Polling.RxEQ. Depending on matched PHY Capability LBPM, a port may configure its PHY for SuperSpeed operation or SuperSpeedPlus operation.
- **Polling.RxEQ** - Polling.RxEQ is a substate for receiver equalization training. A port is required to complete its receiver equalization training.
- **Polling.Active** - Polling.Active is a substate that continues the link's Enhanced SuperSpeed training.
- **Polling.Configuration** - Polling.Configuration is a substate where the two link partners complete the Enhanced SuperSpeed training.
- **Polling.Idle** - Polling.Idle is a substate where the port decodes the TS2 ordered set received in Polling.Configuration and determines the next state.

3 **U0** - U0 is the normal operational state where packets can be transmitted and received. U0 does not contain any substate machines.

4 **Recovery** - The Recovery link state is entered to retrain the link, or to perform Hot Reset, or to switch to Loopback mode. In order to retrain the link and also minimize the recovery latency, the two link partners do not train the receiver equalizers. Instead, the last trained equalizer configurations are maintained.

It contains three sub-states:

- **Recovery.Active** - Recovery.Active is a substate to train the Enhanced SuperSpeed link by transmitting the TS1 ordered sets.
- **Recovery.Configuration** - Recovery.Configuration is a substate designed to allow the two link partners to achieve the Enhanced SuperSpeed handshake by exchanging the TS2 ordered sets.
- **Recovery.Idle** - Recovery.Idle is a substate where a port decodes the link configuration field defined in the TS2 ordered set received during Recovery.Configuration and determines the next state.

5 **Loopback** - Loopback is intended for test and fault isolation. Loopback includes a bit error rate test (BERT) state machine. A loopback master is the port requesting loopback. A loopback slave is the port that retransmits the symbols received from the loopback master.

It contains two sub-states:

- **Loopback.Active** - Loopback.Active is a substate where the loopback test is active. The loopback master is sending data/commands to its loopback slave. The loopback slave is either looping back the data or detecting/executing the commands it received from the loopback master.
- **Loopback.Exit** - Loopback.Exit is a substate where a loopback master has completed the loopback test and starts the exit from Loopback.

SuperSpeedPlus uses some additional LTSSM states to configure the 10G operation mode. LFPS handshake is divided in more states SCD1.LFPS, SCD2.LFPS (SuperSpeedPlus Capability Declaration) and LBPM (low power signaling mechanism for two SuperSpeedPlus ports to communicate with each other).

Link Training Methods

Following are the link training methods for USB 3.2 Gen 1 and USB 3.2 Gen 2:

- WarmReset (only for Devices – upstream ports)

A WarmReset generated by downstream port to upstream port; done when ‘Device’ is selected. A WarmReset consists of a continuous LFPS (Low Frequency Periodic Signal).

Loopback Training

Loopback testing provides a standard way to quantify the bit error rate (BER) for established links between host and device. There is one loopback master and one loopback slave in the loopback configuration. The loopback master is the port that has the Loopback bit asserted in TS2 ordered sets. A loopback slave is the port that retransmits the symbols received from the loopback master. Master checks returned data for errors.

Loopback.Active is a sub-state where the loopback test is active. The loopback master is sending data/commands to its loopback slave. The loopback slave is either looping back the data or detecting/executing the commands it received from the loopback master.

Sequence

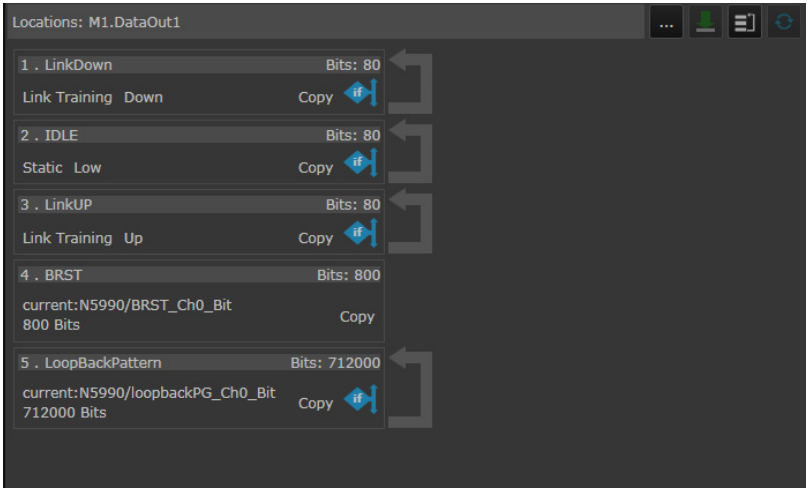
For performing compliance tests the DUT has to be ‘trained’ into loopback mode. The pattern sequencer available in the M8070B software is able to set up a USB 3.2 DUT into the specific loopback mode. The sequencer is also able to send compliance pattern to the DUT and can compare the received pattern with expected pattern for measuring e.g. bit error rates.

The pattern sequence language is based on XML. The pattern sequence language can be created and edited using the Sequence Editor in the M8070B software interface.

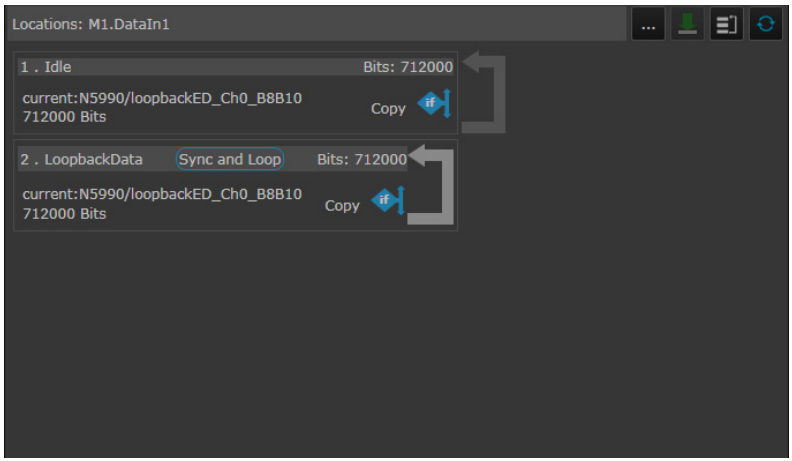
If symbol width 10 or 132 are selected following additional parameters will be visible on the right hand side in the **Sequence Editor** in the **Parameter Window**. On selecting the Symbol Width 10, the parameters for Link Training USB 3.2 Gen 1 are available in the **Parameter Window**. Similarly, on selecting the Symbol Width 132, the parameters for Link Training USB 3.2 Gen 2 are available in the **Parameter Window.**

Refer the section Link Training Configuration on page 625 for the parameters which are added to pattern sequence language for specifying certain values to configure the LTSSM.

The following figure shows an example of the link training sequence for USB 3.2 Gen 1 on Generator:



The following figure shows an example of the link training sequence for USB 3.2 Gen 1 on Analyzer:



Link Training USB 3.2 Gen 1 and USB 3.2 Gen 2 Parameters

The following table shows the parameters which can be configured for link training USB 3.2 Gen 1 and USB 3.2 Gen 2:

Parameter name	Values	Default	Description	Applicable for USB LTSSM USB 3.2 Gen 1/ USB 3.2 Gen 2
DUT Type XML: usbDut	Host Device	Device	Specifies which role the BERT should play during link training. It can be either an downstream port (Host) or an upstream port (Device)	Both
PHY Capability XML: phyCapability	x1 or x2	x1	Specifies the PHY capability of the DUT. When selecting the option **x2**, then channel 1 takes the role of the config lane during the link training.	USB 3.2 Gen1 (5 Gb/s) and USB 3.2 Gen2 (10 Gb/s)
Target State XML: targetState	LoopbackViaPolling	LoopbackVia Polling	Determines the target state when bringing up the link	Both

Trigger State XML: triggerState		RxDetectReset RxDetectActive, PollingLFPS, PollingRxEq, PollingActive, PollingConfiguration, U0 RecoveryActive RecoveryConfiguration LoopbackActive LoopbackExit PollingLFPSPlus PollingPortMatch PollingPortConfig,	LoopbackActive	This parameter determines when the trigger output signal of the LTSSM block should be asserted. Additionally this information can be translated into a trigger pulse on entering or leaving the specified state. This is done by the pulse shaper of the Ctrl Out A connector and no direct functionality of the LTSSM.	Both
LFPS	tPeriod XML: lfps_tPeriod	10 ns – 110 ns	50 ns	Period and Duty cycle of LFPS cycle	Both
	Duty Cycle XML:lfps_dutyCycle	40 % - 60 %	50 %		
Polling.LFPS	tBurst XML: pollingLFPS_tBurst	0.5 µs – 2 µs	1 µs	Link Training handshake before 5Gb/s	USB 3.2 Gen 1
	tRepeat XML: pollingLFPS_tRepeat	5 µs – 20 µs	10 µs		
Warm Reset LFPS	tBurst XML: warmResetLFPS_tBurst	80 ms – 120 ms	100 ms	LFPS trigger transition to Rx.Detect	Both
SCD1 and SCD2	tBurst XML: scd1scd2_tBurst	0.5 µs – 1.5 µs	1 µs	SuperSpeedPlus Capability Declaration (SCD) is a step for a SuperSpeedPlus port, while in the Polling.LFPS substate, to identify itself as SuperSpeedPlus capable by transmitting Polling.LFPS signals with specific patterns unique to SuperSpeedPlus ports.	USB 3.2 Gen 2
	tRepeat0 XML: scd1scd2_tRepeat-0	4 µs – 11 µs	7.5 µs		
	tRepeat1 XML: scd1scd2_tRepeat-1	9 µs – 16 µs	12.5 µs		
SuperSpeedPlus LFPS Based PWM Message (LBPM	tPWM XML: superSpeedPlus_tPWM	1.9 µs – 2.5 us	2.2 µs	LBPM is defined as a low power signaling mechanism for two SuperSpeedPlus ports to communicate with each other based on LFPS signals. The adoption of Pulse Width Modulation (PWM) is to embed the transmitting clock in data and to allow for easy data recovery at the receiver based on LFPS clock.	USB 3.2 Gen 2
	tLFPS-0 XML: superSpeedPlus_tLFPS-0	0.4 µs – 0.9 us	0.750 µs		
	tLFPS-1 XML: superSpeedPlus_tLFPS-1	1.23. µs – 1.9 us	1.450 µs		

Test Setup

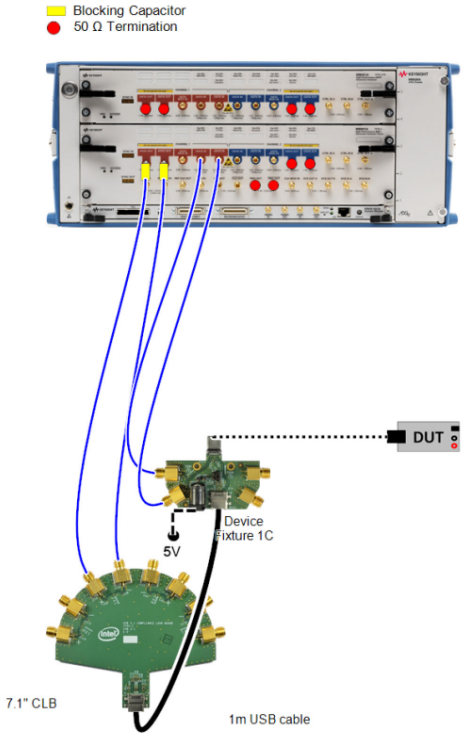
Test Setup Requirements

The following are the test setup requirements to perform a USB link training:

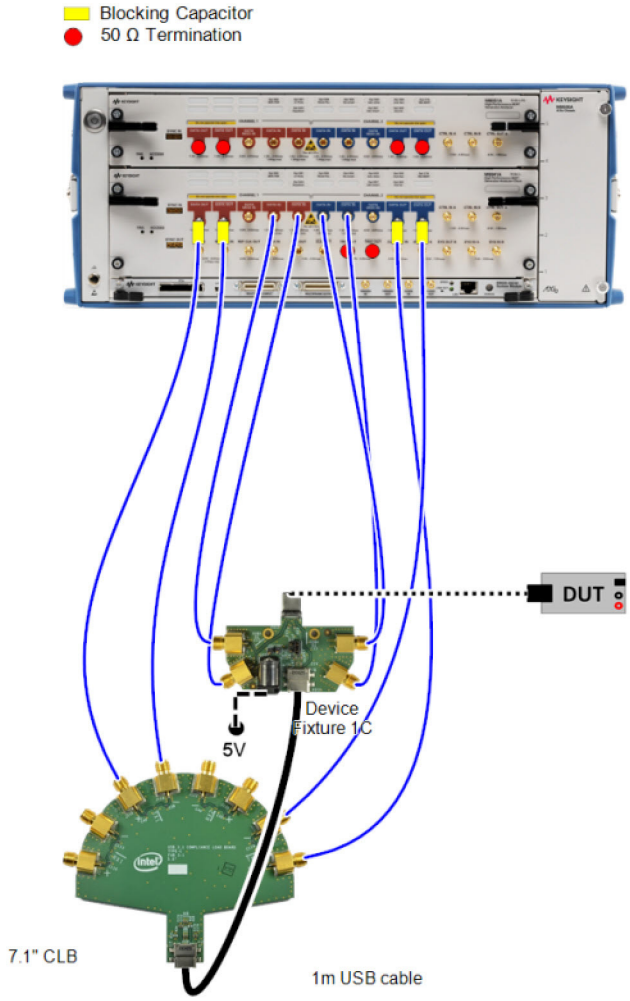
- M8020A with a M8041A and M8051A modules or M8040A with M8045A and M8046A modules or M8050A with M8042A and M8046A modules.
- One Keysight U7242A Fixture
- One 6 inch USB 3.2 Gen 1 cable
- Four SMA cables
- Four 11742A blocking capacitor

M8020A Setup

- M8020A Gen2x1

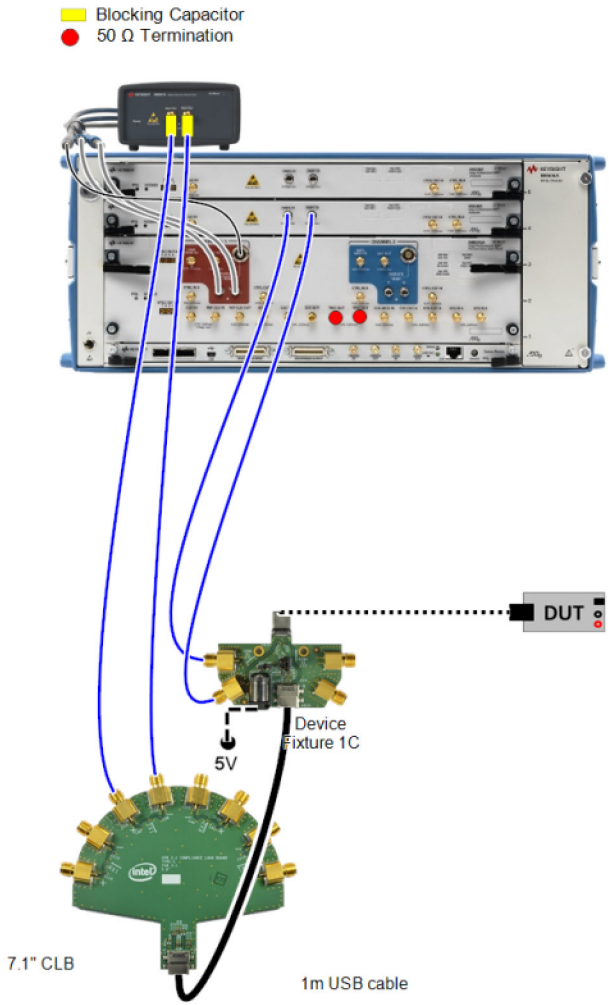


- M8020A Gen2x2

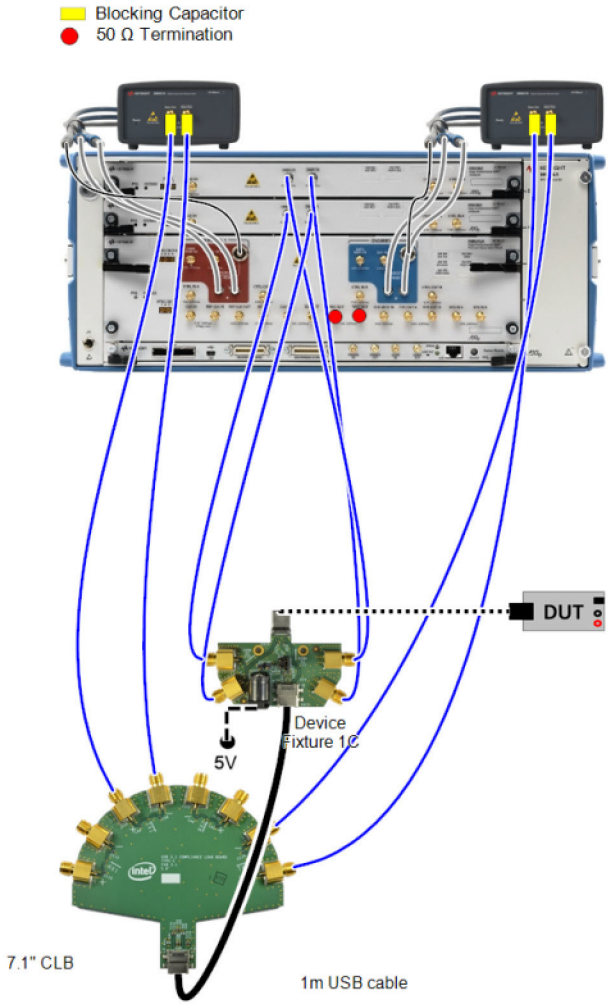


M8040A Setup

- M8040A Gen2x1

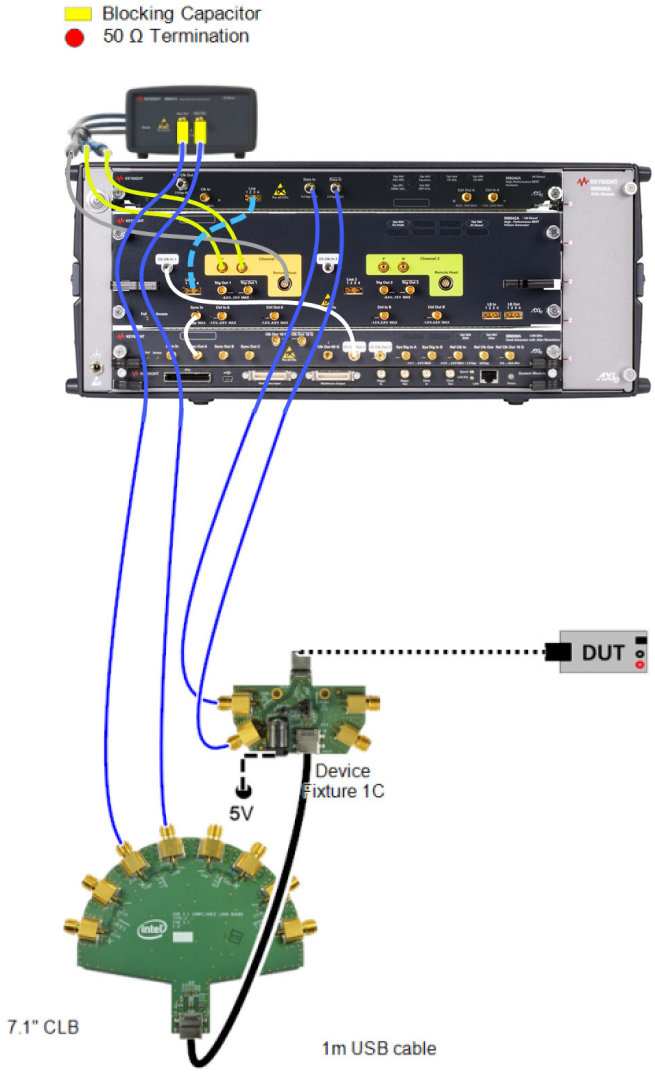


- M8040A Gen2x2

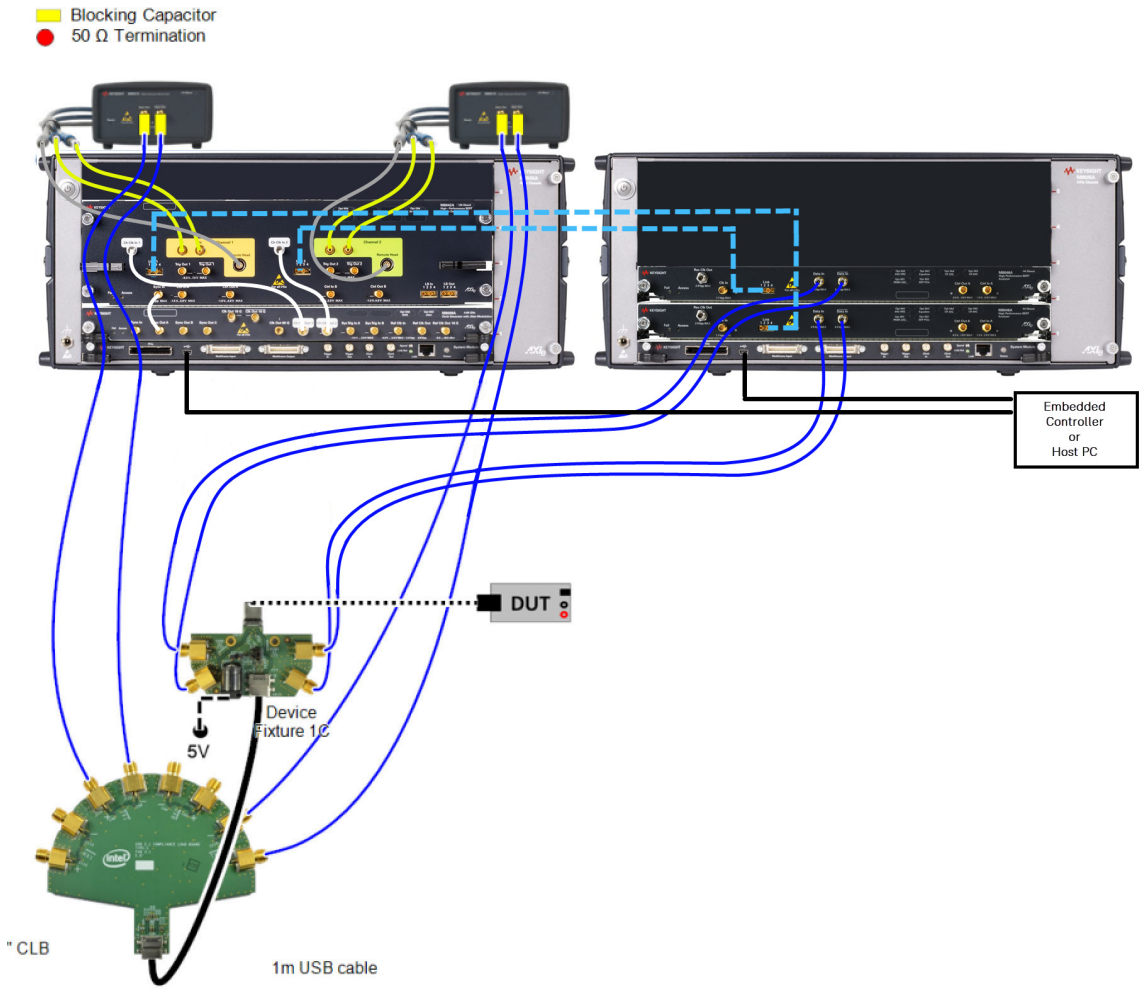


M8050A Setup

- M8050A Gen2x1



- M8050A Gen2x2



Link Training Configuration

You can configure the link training parameters to control LTSSM using the Sequence Settings window. For details on link training parameters, see Link Training Configuration on page 625.

USB 3.2 Gen 1 and USB 3.2 Gen 2 link training is possible with every Pattern Generator channel of a M8020A/M8040A/M8050A module.

Test Procedure

Follow the given steps to perform link training:

1 Load the instrument state in the M8070B software.

2 Power on the DUT.

3 Enable the Outputs of the M8020A/M8040A/M8050A Pattern Generator module.

4 Reset the DUT (disconnect/connect power at the fixture).

5 With this instrument setup everything is prepared for capturing the data. Hit the **Break** button in the **Sequence Editor** to start the link training. If link training is successful, the **Status Indicator** should show that the sequencer of the generator is executing the last block and that there are no bit errors.

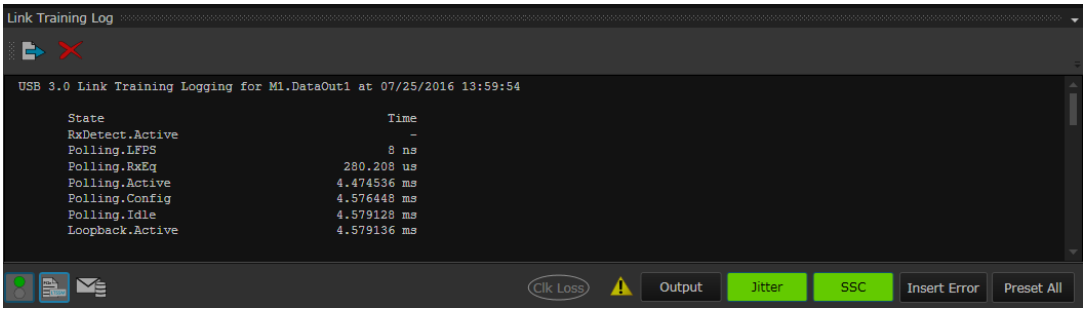
6 For shutting down the link hit the **Break** button again. The sequencer of the generator should return to block 2.

7 Press **Break** button again for starting the link training again.

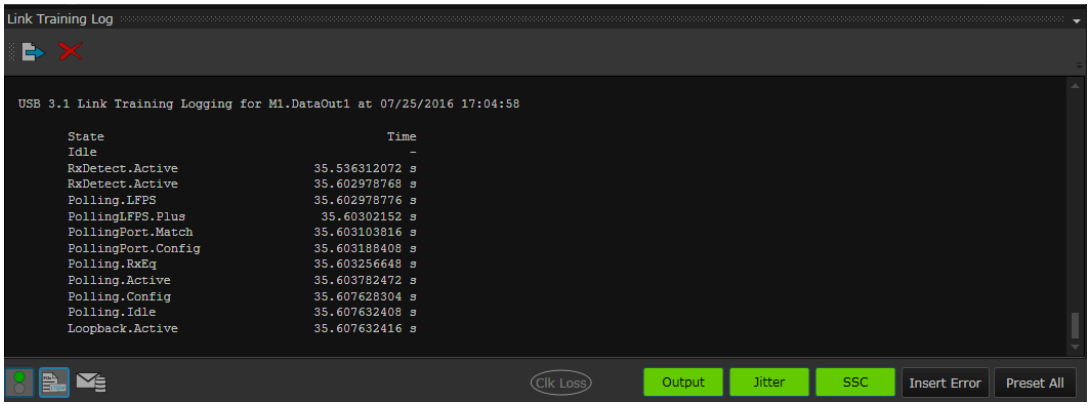
Link Training Log

The **Link Training Log** window displays the log generated while initiating the link training test for USB 3.2 Gen 1 and USB 3.2 Gen 2. All information regarding the executed tests and their status are displayed with the date and time stamp. This helps to identify the root cause of a problem. For instance, the **Link Training Log** shows test failure due to an unexpected LTSSM state change.

The following figure shows the log generated while initiating the link training test for USB 3.2 Gen 1:



The following figure shows the log generated while initiating the link training test for USB 3.2 Gen 2:



You can open/close the **Link Training Log** window by clicking on the **Show/Hide Link Training Log** icon present in the status bar. The **Show/Hide Link Training Log** icon with orange background indicates an update or new entry in the link training log.

M8070B Support for PCIe3.0/4.0/5.0/6.0 Link Training using M8040A/M8050A

The M8040A/M8050A supports interactive link training for PCIe3.0, PCIe4.0, PCIe5.0 and PCIe6.0. This section describes the M8070B support to conduct PCIe3.0/4.0/5.0/6.0 link training by M8040A (M8045A & M8046A) and M8050A (M8042A & M8046A) modules.

Hardware Setup

The interactive link training on M8040A requires a M8045A Pattern Generator module equipped with at least one Data Out and a M8046A Error Detector module.

The interactive link training on M8050A requires a M8042A Pattern Generator module equipped with at least one Data Out and a M8046A Error Detector module.

Both Pattern Generator and Error Detector modules need to be equipped with a (Sequence) Link Connector on their front panels.

For Error Detector module, it is a requirement to be equipped with a built in CDR, these modules also support the Sequence Link connector.

For Pattern Generator modules, every Data Out has its own Link port. Which PG Data Out Link connector is connected to which Error Detector Data In Link connect is queried automatically by the instrument and cannot be specified manually. It is also automatically detected, if a link cable is removed and the link is re-established before another link training run is performed.

The cable part number M8041-61601 is required to connect two link connectors.

Interactive link training is used on each of the two Data Outs of a M8040A/M8050A Pattern Generator module, therefore two DUTs can be trained in parallel when additionally using two M8040A Error Detector modules.

As there is only one differential Trig Out connector on a M8040A/M8050A Pattern Generator module, though using two DUTs in parallel requires splitting the signal by some means to be able to supply two compliance boards with a reference clock.

Licensing

Required Options

License	Instrument Option	Description
M8042A-G32	G32	32 GBd PG for NRZ and PAM-4
M8042A-0G4	0G4	Deemphasis

The minimum M8050A configuration requires options G32 and 0G4 for the PG. Deemphasis optimization is an essential part of PCIe link training.

License	Instrument Option	Description
M8045A-G32	G32	32 GBd PG
M8045A-0G4	0G4	Deemphasis

The minimum M8040A configuration requires options G32 and 0G4 for the PG. Deemphasis optimization is an essential part of PCIe link training.

License	Instrument Option	Description
M8046A-A32	A32	32GBd ED
M8046A-0A3	0A3	Equalizer
M8046A-0A4	0A4	Clock Recovery for 32 GBd
M8046A-0S1	0S1	Interactive Link Training for PCIe 8/16/32 GT/s
M8046A-0S2	0S2	SKP OS Filtering for PCIe 8/16/32 GT/s and CCIX 20/25 Gb/s
M8046A-ON1 (PCIe 6 license)	ON1	PCIe LTTSM for 64 GT/s, requires M8046-0S1/US1
M8046A-ON2 (PCIe 6 license)	ON2	PCIe Filtering of SKP OS Extension for 64 GT/s, requires M8046-0S1 and M8046-0S2

For PCIe 6 link training, the following license combinations are required:

- M8042A: ["G64","0G4"]
- M8045A: ["G64","0G2","0G3","0G4", "0P3", "0P6", "0G9"]
- M8046A: ["A32", "0A4", "0P3", "0P6", "0S1", "0S2", "0S4", "0N1", "0N2"]

The minimum M8040A ED configuration requires options A32 and 0A4 for being able to capture data using the CDR at up to 32 Gb/s.

Additionally, options 0A4 for clock recovery, 0S1 for PCIe link training, and option 0S2 for SKP OS filtering are required.

Recommended Options

These options are not absolutely required for LTSSM usage, but are needed for performing full verification of PCIe functionality of a DUT.

License	Instrument Option	Description
M8045A-0G3	0G3	Jitter
M8045A-0G6	0G6	Reference Clock Input with Multiplying PLL

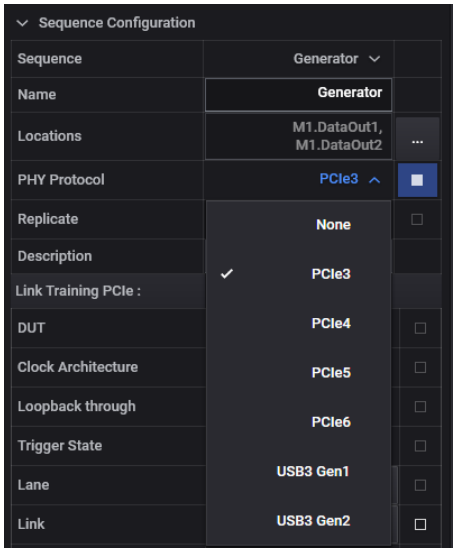
Recommended Packages

To be able to perform a jitter tolerance, bathtub, etc. measurement for DUT debugging/characterization, it is advantageous to have the Advanced Measurement Package for M8000 Series BERT Test Solutions (M8070ADVB)

Sequence Editor

Using PCIe LTSSM functionality

The interactive link training functionality is specified differently by selecting a PHY Protocol from the Sequence Configuration block.



Doing this will show or hide various other sequence specific properties which are only valid for a specific PHY Protocol.

M8040A/M8050A PG

The following additional features will appear in the Sequence Editor, only when selecting one of the PCIe PHY Protocol options inside of sequences which are bound to M8040A/M8050A PG Data Out locations.

PCIe3.0/4.0/5.0/6.0

Link Training PCIe – Allows to modify properties of the link training procedure.

Link Training Sequence Block Type – Perform Link Up/Down

Link Training Trigger – Enable trigger signal asserted on a specific LTSSM state

Link Training Block Branch Events – Perform sequence branching on specific LTSSM events

These features are described in further detail below.

M8040A/M8050A ED

On the error detector the functionality, supporting interactive link training is different compared to the pattern generator.

PCIe3.0/4.0/5.0/6.0 and CCIX

For these PHY Protocol selections SKP OS filtering is automatically enabled. It removes SKP OS symbols contained in the data stream before measuring BER. Doing this is required as the BER is measured against a static memory pattern, but the number of SKP OS symbols contained in the received data stream (sent by a DUT) is variable.

PCIe3.0/4.0/5.0/6.0

Link Training Block Branch Events – Perform sequence branching on certain LTSSM events.

XML Sequence Description

The PHY Protocol for PCIe5 mode is specified the following way.

```
<linkTrainingConfigurations>
  <pcie3 capability="PCIe5" />
</linkTrainingConfigurations>
```

Specifying any of the other PHY protocol modes (e.g. PCIe3 or PCIe4) works accordingly.

The way of specifying the used LTSSM type inside the sequence XML description is backwards compatible to M8020A. Therefore, an already existing M8020A sequence can be reused on a M8040A module without any changes when programmed via SCPI.

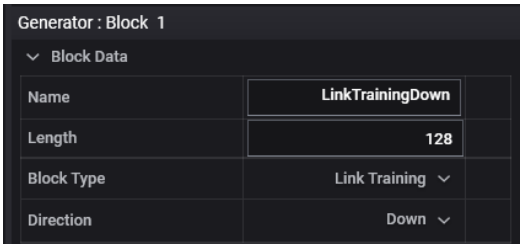
For the <pcie3/> node attributes other than “capability” are ignored by M8040A/M8050A ED modules as these attributes control the LTSSM which driven by the M8040A/M8050A PG.

Link Training Sequence Block Type

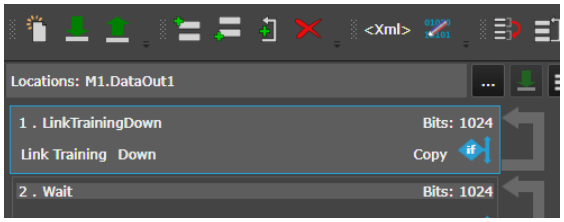
A special “Link Training” sequence block type is selectable for sequences bound to M8040A/M8050A PG locations.

These blocks are used to either start link training up (Link Training block with direction “Up”) to the selected target speed or disable the link (Link Training block with direction “Down”).

Selection of Link Training block type and settings



Representation of Link Training block in graphical sequence view



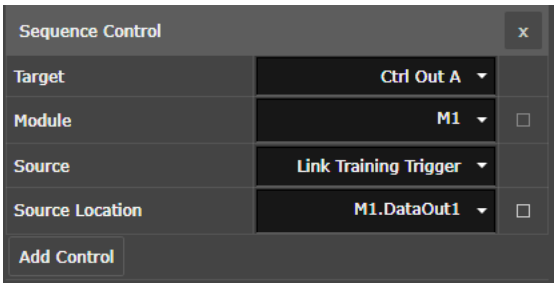
XML Sequence Description

In the sequence XML a LinkTraining Block is defined by using the <linkTraining/> node.

```
<sequence>
  <loop>
    <block length="1024" name="LinkTrainingDown">
      <linkTraining direction="down" />
    </block>
  </loop>
```

Link Training Sequence Controls

Link Training Trigger



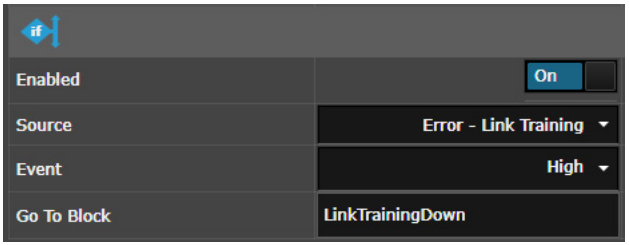

```
<controls>
  <control sink="CtrlOutA" sinkLocation="M1" source="LinkTrainingTrigger" sourceLocation="M1.DataOut1" />
</controls>
```

Link Training Events

Detect State – Link Training

Target State – Link Training

Error State – Link Training




```
<loop>
  <block length="130" name="LinkTrainingUp">
    <linkTraining direction="up" />
    <if source="LinkTrainingTargetState" event="high" />
    <if source="LinkTrainingError" event="high" goto="LinkTrainingDown" />
  </block>
</loop>
```

Scrambler and EIEOS

There is currently no scrambler implemented in M8040A/M8050A. The EIEOS symbols are derived automatically from the selected PCIe generation.

Link Training PCIe

Generation

In contrast to M8020A, this parameter cannot be defined separately and is always derived off the PHY protocol selection. Possible values are either PCIe3/4 or 5.

User Calibrated Presets

This legacy M8020A parameter is not available for M8040A/M8050A, presets are user defined at the respective Data Out and therefore always custom/calibrated.

In case a Data Out is part of a sequence with the PHY Protocol selected as PCIe, the Deemphasis functional block of the channel changes into the PCIe LTSSM preset mode.

With these outputs-specific parameters, it is possible to define the used full swing value and use potentially calibrated deemphasis cursor settings.

PCIe3 and PCIe4

When using PCIe3 or PCIe4, the parameters are generally the same as with M8020A modules.

Lane

The only allowed value for this field is still 0.

Select Start Preset Gen 4

In contrast to M8020A, it is now possible to specify the additional parameter value LTSSM Defined.

- **User Defined**

  Same as M8020A
- **LTSSM Defined**

  This new parameter value uses the setting determined by the LTSSM during Gen 3 training.

PCIe5

Starting with M8040A/M8050A, it is possible for the first time to do link training for PCI Express up to generation 5.

Most of the parameters are the same than with PCIe3 and 4 but some new parameters were introduced and changed.

Lane

When doing PCIe5 is now possible to use the values 0 to 31 for specifying a lane.

Select Start Preset Gen 5

- **User Defined**

  Uses preset value selected in 'Start Preset Gen 4' parameter
- **LTSSM Defined**

  Use the value determined by the LTSSM during Gen4 training

PCIe6

Starting with M8040A/M8050A, it is possible for the first time to do link training for PCI Express up to generation 6.

Most of the parameters are the same than with PCIe3 and 4 but some new parameters were introduced and changed.

Lane

When doing PCIe6 is now possible to use the values 0 to 31 for specifying a lane.

Select Start Preset Gen 6

- User Defined

  Uses preset value selected in 'Start Preset Gen 5' parameter
- LTSSM Defined

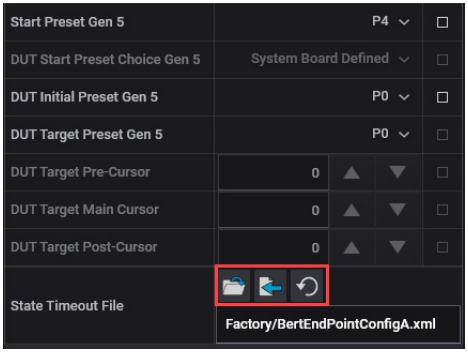
  Use the value determined by the LTSSM during Gen5 training

Configurable State Timeouts in PCIe LTSSM

This feature enables you to select and configure an XML file for state timeouts map. There are two types of XML files available for Addin Card and System Board which enables different DUTs.

- ConfigA
- ConfigB

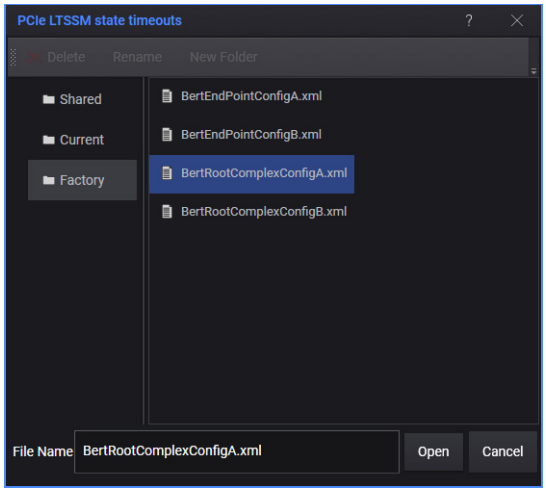
The options used to control this feature is shown in the following figure:



The property "**stateTimeoutMap**" in the Schema corresponds to these UI controls.

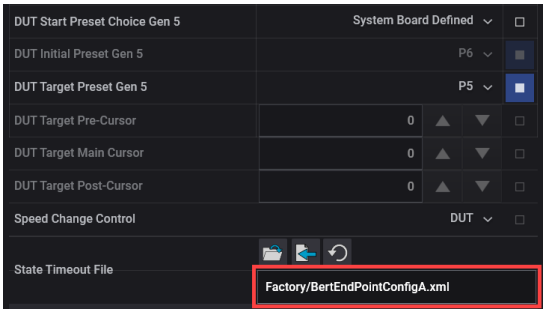
Opening a state timeout file

1 Click the **Open** icon.
The **PCIe LTSSM state timeouts** dialog box appears.



2 Click **Factory** and then select one of the following:
- BertEndPointConfigA.xml
- BertEndPointConfigB.xml
- BertRootComplexConfigA.xml
- BertRootComplexConfigB.xml

3 Click **Open**.
The selected file is displayed.

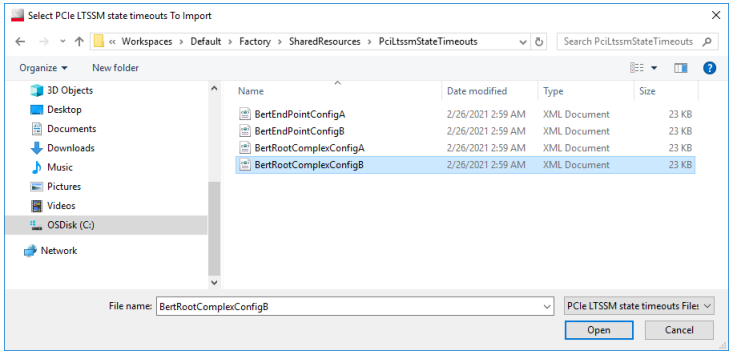


Importing a state timeout file

To import an existing file from any location to M8070B workspace, perform the following steps:

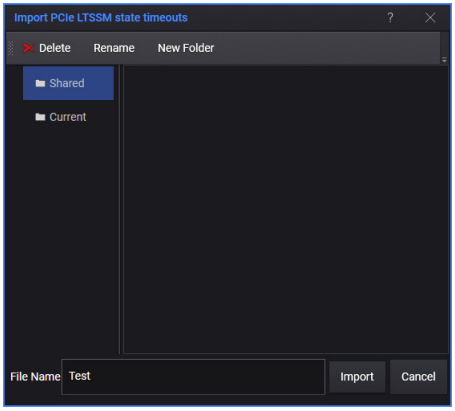
1 Click the **Import** icon.

The **Select PCIe LTSSM state timeouts To Import** dialog box appears.



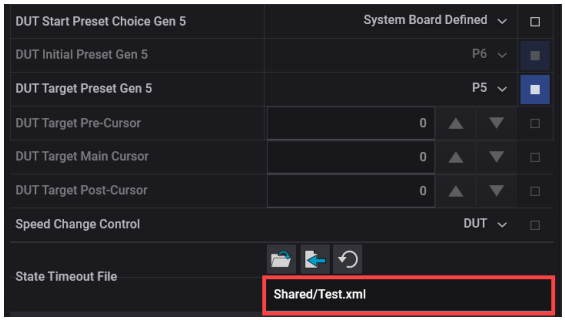
2 Browse the required file, and then click **Open**.

3 In the **Import PCIe LTSSM state timeouts** dialog box, type an appropriate name in the **File Name** text box.



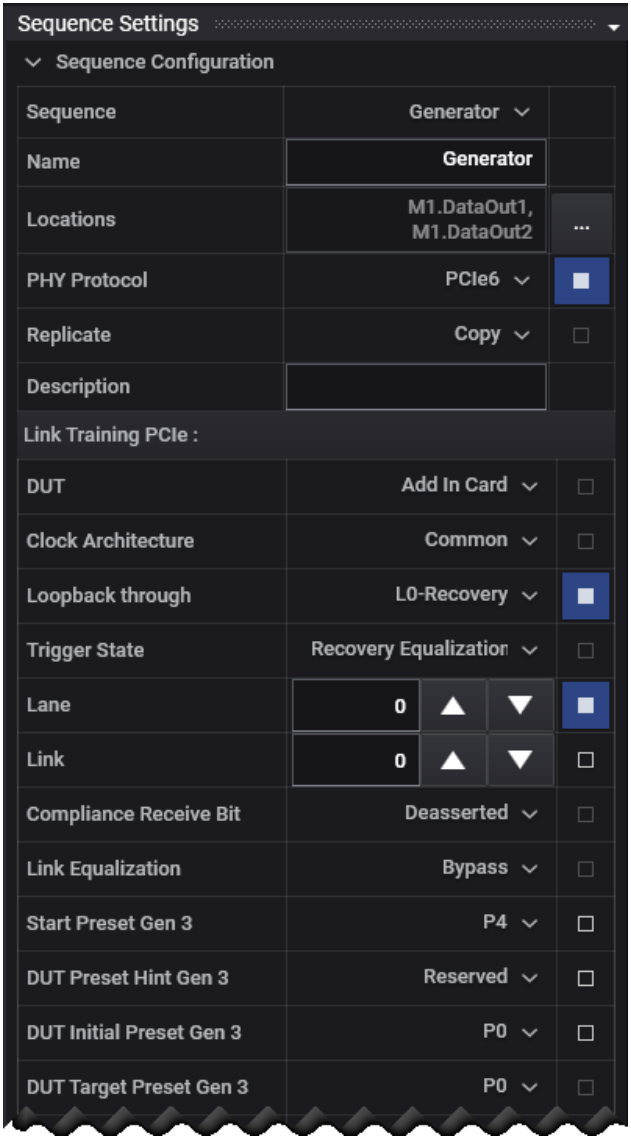
4 Click **Import**.

The selected file is displayed.



PCIe LTSSM Parameters

The parameters used to control the PCIe LTSSM are shown in the following figure:



General Parameters

These parameters are required for general setting up the LTSSM operation.

Name	Possible Values	Description	Used for DUT type
DUT Type	Add-in card System Board	Specifies which role the BERT should play during link training. It can either be an upstream device for testing a downstream port or vice versa.	Both
Target Speed	32.0GT/s 16.0GT/s 8.0GT/s	Determines the target speed when doping the speed change. The Target Speed 32.0GT/s) is applicable for M8040A only.	Both
Loopback through	L0-Recovery Configuration L0-Recovery with Speed Bypass Configuration with Equalization	Determines the target state when bringing up the link. In case of L0-Recovery and Configuration, LTSSM will go through its normal route as before In case of L0-Recovery with Speed Bypass, intermediate speeds (Gen3 and Gen4) will be bypassed. This is only applicable for Gen5 target rate. In case of Configuration with Equalization, equalization will always happen at the Gen5 rate. This is only applicable for Gen5 target rate.	Both
Trigger State	LTSSM States	This parameter determines when the trigger output signal of the LTSSM block should be asserted. Additionally, this information can be translated into a trigger pulse on entering or leaving the specified state. This is done by the pulse shaper of the TCRL OUT connector and no direct functionality of the LTSSM.	Both
Compliance Receive Bit	Deasserted Asserted	Specifies whether the compliance received bit is asserted or de-asserted in TS1.	Both
Ref Clock Architecture	Common, Separate	Defines the PCIe Reference Clock Architecture - common reference clock / separate reference clock.	Both
Link EQ states	Bypass Presets only Full	Determines whether link equalization should be performed. It can either be aborted after phase 1 (Bypass) or fully executed. In the second case it can be determined whether only preset or all (i.e. individual cursor) requests should be accepted.	Both
Lane Number	0-31	The lane number being used.	Both
Send PAD in Loopback.Entry	PAD, Send Lane Number provided in "Lane Number" parameter	Send Lane number as the above selected value or PAD in TS1s in the Loopback.Entry substate.	Both
Link Number	0	The link number being used.	Add-in Card*
BERT Start Preset Gen3	P0-P9	This is the preset used by the BERTs TX port after switching to Gen 3 operation and when operating as an upstream device.	Add-in Card

Name	Possible Values	Description	Used for DUT type
RX Preset Hint	0 (-6 dB) 1 (-7 dB) 2 (-8 dB) 3 (-9 dB) 4 (-10 dB) 5 (-11 dB) 6 (-12 dB) 7 (reserved)	This is the preset hint being sent by the BERT to the DUT during phase 0 of the link equalization procedure. It's only used when the BERT operates as upstream device.	Add-in Card
DUT Start Preset Gen3	P0-P9	This is the preset the BERT transfers to the DUT in phase 0 of the link equalization procedure. It's only used when the BERT operates as an upstream device (2.5G to 8G)	Both
DUT Target Preset Gen3	P0-P9, P10, Cursor†	This is the preset the BERT requests the DUT to switch to during link equalization. Depends on the role the BERT is playing, this is done in either phase 2 or 3 of the link equalization training (8G)	Both
Select BERT Start Preset Gen4	User Defined LTSSM Defined LTSSM EQTS2 defined	Use BERT start preset specified by user or use resulting preset of phase 2 of 8GT/s TXEQ as start preset. LTSSM EQTS2 defined - preset received in the EQTS2 before the speed change. LTSSM will use preset received in EQTS2 if EQTS2 is sent. But if the endpoint does not send EQTS2, it will use the user-defined preset instead.	Add-in Card
BERT Start Preset Gen4	P0-P9	This is the preset used by the BERTs TX port after switching to Gen4 operation and when operating as an upstream device.	Add-in Card
DUT Start Preset Choice Gen4	System Board Defined User Defined	Use the DUT start preset defined either the System Board or the user. For DUT type Add-In Card, only the User Defined option is available. This parameter is grayed out, and User Defined option is set by default. For DUT type System Board, both System Board Defined and User Defined options are available, with User Defined selected by default.	Both
DUT Initial Preset Gen4	P0-P9	This is the preset the BERT transfers to the DUT in phase 0 (Gen4) of the link equalization procedure. It's only used when the BERT operates as an upstream device.	Both
DUT Target Preset Gen4	P0-P9, P10, Cursor†	This is the preset the BERT requests the DUT to switch to during link equalization (Gen4). Depends on the role the BERT is playing, this is done in either phase 2 or 3 of the link equalization training.	Both
Select BERT Start Preset Gen5	User Defined LTSSM Defined LTSSM EQTS2 defined	Use BERT start preset specified by user or use resulting preset of phase 2 of 16GT/s TXEQ as start preset. LTSSM EQTS2 defined - preset received in the EQTS2 before the speed change. LTSSM will use preset received in EQTS2 if EQTS2 is sent. But if the endpoint does not send EQTS2, it will use the user-defined preset instead.	Add-in Card

Name	Possible Values	Description	Used for DUT type
BERT Start Preset Gen5	P0-P9	This is the preset used by the BERTs TX port after switching to Gen5 operation and when operating as an upstream device.	Add-in Card
DUT Start Preset Choice Gen5	System Board Defined User Defined	Use the DUT start preset defined either the system board or the user. For DUT type: Add-In Card, only the User Defined option is available. This parameter is grayed out, and User Defined is set as the default. For DUT type: System Board with loopback mode: "L0-Recovery with Speed Bypass", only the User Defined option is available. This parameter is grayed out, and User Defined is set as the default. For DUT type: System Board with loopback mode: "L0-Recovery", both System Board Defined and User Defined options are available. The default selection is User Defined.	Both
DUT Initial Preset Gen5	P0-P9	This is the preset the BERT transfers to the DUT in phase 0 (Gen5) of the link equalization procedure. It's only used when the BERT operates as an upstream device.	Both
DUT Target Preset Gen5	P0-P9, P10, Cursor[†]	This is the preset the BERT requests the DUT to switch to during link equalization (Gen5). Depends on the role the BERT is playing, this is done in either phase 2 or 3 of the link equalization training.	Both
DUT Target Pre-Cursor @ Target Speed	0-63	This is the pre-cursor value that the BERT requests the DUT to use during link equalization in cursor mode at Target Speed. Depends on the role the BERT is playing this is done in either phase 2 or 3 of the link equalization training. If not specified 0 is used.	Both
DUT Target Main-Cursor @ Target Speed	0-63	This is the main cursor value that the BERT requests the DUT to use during link equalization in cursor mode at Target Speed. Depends on the role the BERT is playing, this is done in either phase 2 or 3 of the link equalization training. If not specified 63 is used.	Both
DUT Target Post-Cursor @ Target Speed	0-63	This is the post-cursor value that the BERT requests the DUT to use during link equalization in cursor mode at Target Speed. Depends on the role the BERT is playing, this is done in either phase 2 or 3 of the link equalization training. If not specified 0 is used.	Both
Select BERT Start Preset Gen 6	User Defined LTSSM Defined	Use BERT start preset specified by user. LTSSM Defined - preset received in EQ TS1 at previous generation(Gen1) will be used.	Both
BERT Start Preset Gen 6	Q0-Q10	This is the preset used by the BERTs TX port after switching to Gen6 operation and when operating as an upstream device.	Both
DUT Start Preset Choice Gen6	System Board Defined User Defined	Use the DUT start preset defined either the system board or the user. For DUT type: Add-In Card, only the User Defined option is available. This parameter is grayed out, and User Defined is selected by default. For DUT type: System Board, both System Board Defined and User Defined options are available, with User Defined set as the default.	Both

Name	Possible Values	Description	Used for DUT type
DUT Initial Preset Gen 6	Q0-Q10	This is the preset the BERT transfers to the DUT in phase 0 (Gen6) of the link equalization procedure. It's only used when the BERT operates as an upstream device. This is enabled when the DUT Start Preset Choice Gen 6 is User Defined.	Both
DUT Target Preset Gen 6	Q0-Q10	This is the preset the BERT requests the DUT to switch to during link equalization (Gen5). Dependent on the role the BERT is playing this is done in either phase 2 or 3 of the link equalization training.	Both
Speed Change Control	Dut Bert	Specifies whether the speed change to Gen3 (i.e. 8Gbps) speed will be initiated by DUT or BERT during link training. It's only used when the BERT operates as a downstream device. If not specified DUT will initiate the speed change and will also request BERT for the same.	System Board
Full Swing (FS)	24-63	This is the sum of the absolute values of all three cursors. Therefore, it specifies the granularity in which cursors can be controlled.	Both
DUT Preset	Q0-Q10	This is the preset value requested in EQ TS1 that BERT requests the DUT to use in Loopback. Entry state after the speed change when attempting link training through Configuration. If not specified, P7 is used.	Both

* When testing a System Board, this parameter must be loaded from the data received from the DUT.

† Valid for Target Speed only, not for transient speeds in between.

Static Parameters

The Low Frequency Parameter

Name	Value	Description
LF	8	The value which corresponds to the minimum differential value that can be generated by the transmitter.

Parameters being controlled by the Sequencer

These parameters are required for testing, but are controlled by the Sequencer. So they are not direct input parameters of the LTSSM.

Name	Possible Values	Description
DUT Test Pattern	Compliance Test Pattern Modified Compliance Pattern	Specified the test pattern being sent out by the Sequencer when the link is up (i.e. LTSSM is in loopback state).

LTSSM States

LTSSM transits through various states and sub states during link initialization, training, and management. The entry and exit of each of these states and the exchange of packets (Ordered sets) between the two devices during each state are as per the PCIe specifications. Following is a list of these states as per the PCIe specifications.

Detect.Active
Polling.Active
Polling.Configuration
Configuration.Linkwidth.Start
Configuration.Linkwidth.Accept
Configuration.Lanenum.Wait
Configuration.Lanenum.Accept
Configuration.Complete
Configuration.Idle
L0
Loopback.Active
Loopback.Exit
Recovery.Equalization.Phase0
Recovery.Equalization.Phase1
Recovery.Equalization.Phase2
Recovery.Equalization.Phase3
Recovery.Speed

For details on LTSSM states, see LTSSM States on page 698.

25GBASE-KR and 100GBASE-KR4 TX EQ Training

MultiGBASE are computer networking standards and are defined in IEEE 802.3. These TX EQ Training applications are installed as a plug-in to the M8070B software. These plug-ins enable to generate the signal according to the specification, to put the Device Under Test (DUT) into a state where the receiver tolerance can be tested.

The MultiGBASE plug-ins have been developed for testing receiver tolerance of MultiGBASE devices against impairments such as jitter and interference.

For details on the 25GBASE-KR and 100GBASE-KR4 TX EQ Training requirements and setup, refer to the Keysight IEEE MultiGBASE TX EQ Training User Guide.

Using M8062A Data Out Squelch Feature

This M8062A Data Out squelch feature is used to squelch the M8062A's Data Out signals as specified in the selected pattern file.

Limitations

Following are the limitations of this feature:

- Minimum duration of signal squelch is 40 ns
- The squelch effects turn on/off only occurs on a raster of 10 ns.
- The squelch duration can only be modified in the granularity of a Symbol Width dependent bit raster
- Squelch/Data accuracy is ± 2 hardware word widths as defined in Table 71 on page -745.
- Inversion switch of Ctrl Out A signal is not supported when using squelch

Hardware Requirements

To use this feature, the M8041A module must be coupled with a M8062A module.

Hardware Setup

To use this feature it is required to connect the predefined cable (M8046A-801) from Ctrl Out A of the M8040A module to the Electrical Idle In of the M8062A module.

Software Usage

Following the given steps to use the M8062A Data Out squelch feature though M8070B software:

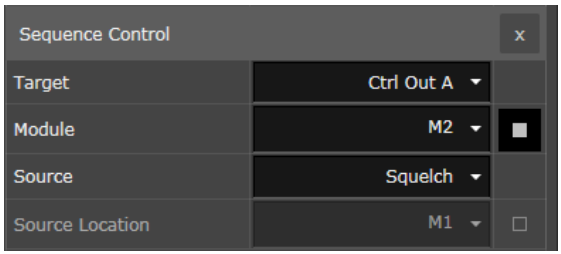
1 From the **Modules View**, activate the Ctrl Out A output of the M8041A module (M1).

2 Change the electrical idle input (squelch input) setting of the M8062A module (M2) to External. This is for external signal to have any effect on the M8062As Data Out.

3 More settings for the **Electrical Idle In** can be changed by selecting the respective module location configured with Elect Idle In.

4 Open the **Sequence Editor**. The squelch can be activated by adding a **Sequence Control** to the M8062A Data Out sequence.

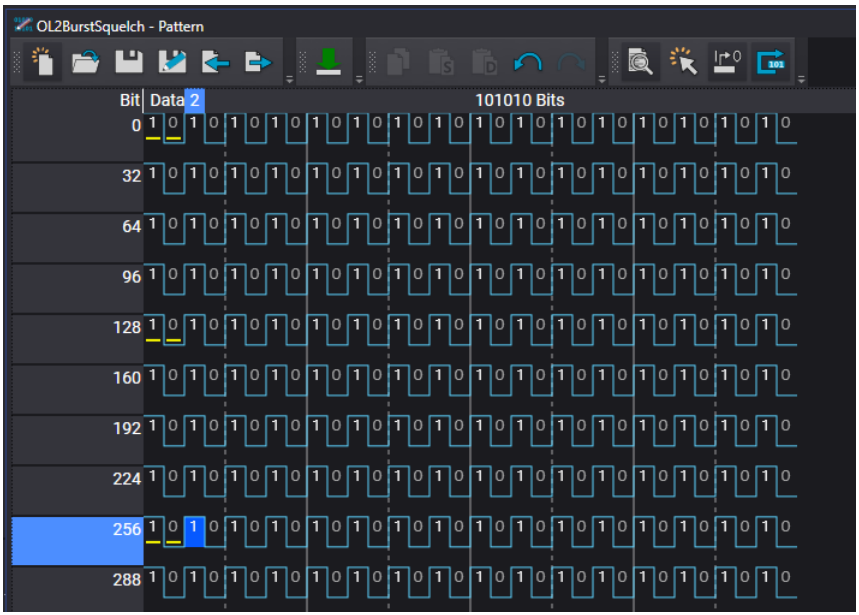
Select the **Target** as **Ctrl Out A**, the **Module** as **M2** (the only valid selection with M8062A usage) and the **Source** as **Squelch**.



5 Alternatively for activating this feature in the GUI it is also possible to specify this setting directly in the XML definition of the sequence. With this it also is possible to activate this feature via SCPI:

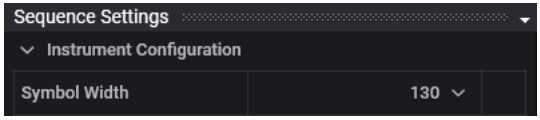
```
<?xml version="1.0" encoding="utf-16"?>
<sequenceDefinition xmlns:xsd="http://www.w3.org/2001/XMLSchema" xmlns:xsi
  <description />
  <symbolWidth>1</symbolWidth>
  <controls>
    <control sink="CtrlOutA" source="Squelch" />
  </controls>
  <sequence>
    <loop>
      <block length="128">
        <prbs polynomial="2^7-1" />
      </block>
    </loop>
  </sequence>
</sequenceDefinition>
```

6 Open the **Pattern Editor** window. When creating a new pattern it is necessary to activate squelch information bits in the pattern. This allows definition of squelched bits by pressing the **S** key or using the respective GUI button. The squelched bits are then underlined by a yellow line.



When defining a pattern containing signal squelching for usage with M8062A it is required to always squelch two bits in a row. This is necessary because the pattern will be downloaded independently into Channel 1 and Channel 2 of the M8041A module driving the M8062A.

By squelching a single bit the whole word will be squelched. Effective word widths used by the hardware depend on the **Symbol Width** setting in the **Sequence Editor**.



The selection thereby results in the following hardware word width for M8041A/M8062A.

Table 71 Hardware word width corresponding to selected symbol width

Symbol Width [bit]	M8041A Word Width [bit]	M8062A Word Width [bit]
1	64	128
10	80	160
130	130	260
132	132	264

For signal squelching to work reliably, it is required that the resulting duration of the squelched blocks is at least 20 ns in length. Otherwise, the Electrical Idle In of the M8062A might miss a signal from the M8041A's Ctrl Out A port.

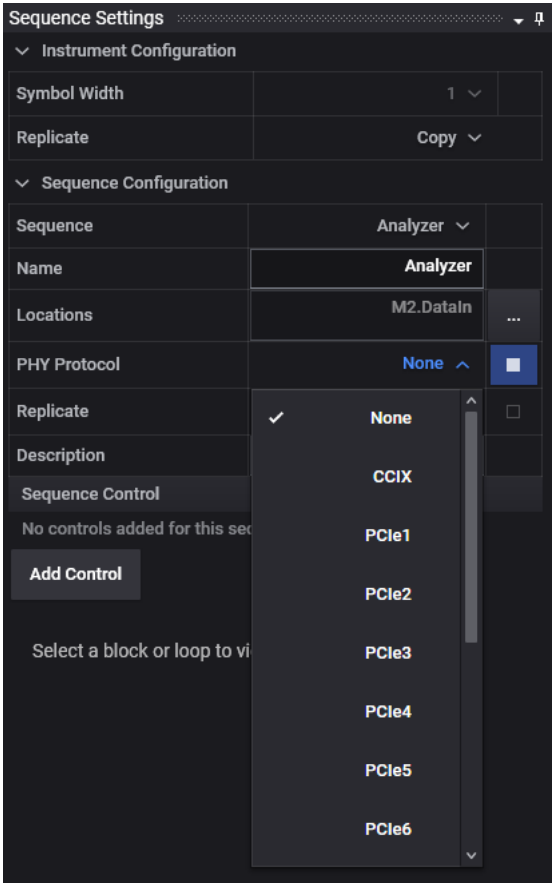
The minimum granularity of a squelch signal is limited by the currently used word width of the M8041A/M8062A combination.

M8046A PHY Protocol Selection (SKP OS Filtering)

PHY Protocol

The M8046A modules allows to specify a PHY protocol which can be supported by a specific sequence. This selection is done in the Sequence Editor when selecting a sequence which is bound to a module supporting this feature.

From the Sequence Editor, go to the Sequence Configuration block in the Sequence Properties side pane and select a PHY Protocol.



The available choices depend on the channels using the sequence.

For M8046A, following are the possible options:

- **M8046A-0S2 (US2, TS2)**: SKP OS Filtering for PCIe. This includes 8b10b and 128b130b coding.

  The available PHY protocol selections for this license are as follows:
  - None - No specific sequence capability
  - CCIX - Dedicated sequence setting for CCIX
  - PCIe1 - Dedicated sequence setting for PCIe1
  - PCIe2 - Dedicated sequence setting for PCIe2
  - PCIe3 - Dedicated sequence setting for PCIe3
  - PCIe4 - Dedicated sequence setting for PCIe4
  - PCIe5 - Dedicated sequence setting for PCIe5
- **M8046A-0N2 (UN2, TN2)**: SKP OS Filtering for PCIe.

  The available PHY protocol selections for this license are as follows:
  - PCIe6 - Dedicated sequence setting for PCIe6
- **M8046A-0S3 (US3, TS3), M8046A-0S4 (US4, TS4)**: SKP OS Filtering for USB. This includes 8b10b and 128b132b coding.

  The available PHY protocol selections for this license are as follows:
  - USB3 Gen1 - Dedicated sequence setting for USB3 Gen1
  - USB3 Gen2 - Dedicated sequence setting for USB3 Gen2
- **M8046A-0S6 (US6, TS6)**: SKP OS Filtering for PCIe. This includes 8b10b and 128b150b coding.

  The available PHY protocol selections for this license are as follows:
  - SATA2 - Dedicated sequence setting for SATA2
  - SATA3 - Dedicated sequence setting for SATA3
  - SAS1 - Dedicated sequence setting for SAS1
  - SAS2 - Dedicated sequence setting for SAS2
  - SAS3 - Dedicated sequence setting for SAS3

The PHY Protocol selection automatically defines the alignment, filler symbol sequences for the selected standard.

There is no option to manually enter these symbols on a sequence for a M8046A.

All of the above selected protocols have the single additional feature that SKP OS filtering is active as soon as the sequence is downloaded.

All of the modules bound to this sequence need to be capable of supporting this feature.

NOTE When selecting a specific PHY protocol on M8046A the maximum allowed data rate is 64GT/s.

NOTE Scrambler will not be available for M8040A.

SKP Ordered Set filtering/removal

The M8046A module supports SKP OS filtering for the PCIe3, PCIe4, PCIe5, PCIe6 and CCIX standards as defined in the respective specification.

NOTE Selection of PCIe 5 is supporting SKP OS symbol filtering as defined in version 0.7.

NOTE SKP OS filtering is available as per installed licenses (0S2, 0S4, 0S6, ON2, and the corresponding upgrade, or trial licenses).

For the new module specific options, please refer to M8040A Licenses on page 833.

This functionality removes all SKP ordered sets from the received data stream. When setting up a sequence for a BER measurement which is bound to the Error Detectors Data In it is required for the pattern to not contain any SKP OS symbols. As these symbols are removed before comparing the received and expected data.

The SKP OS filtering functionality does not discriminate between the different standards but removes all possible SKP OS symbol types in the above mentioned standards.

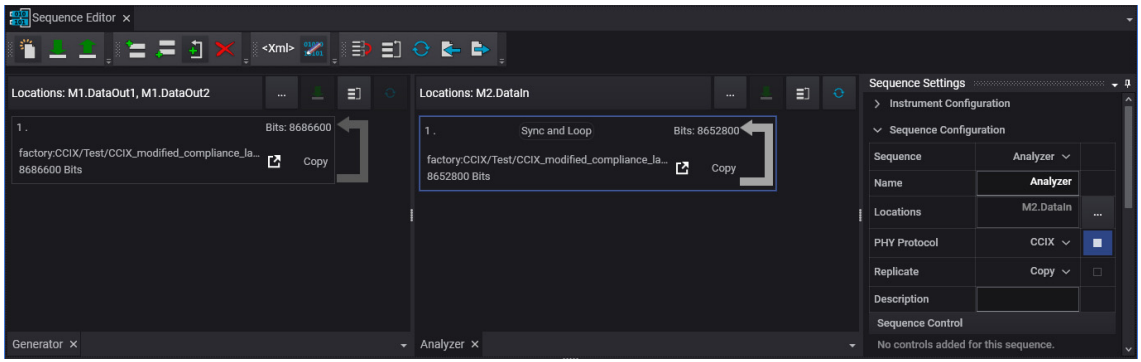
NOTE

In case SKP OS filtering is active the expected pattern must not contain any SKP OS symbols as these will get removed before the received data stream is compared to the expected pattern.

Whenever a SKP OS symbol is removed from the received data stream the expected pattern compare position is pinned down until past the SKP OS symbols duration to be able to compare the data. The necessity for modifying the compare position leads to the need to do a (manual or automatic) pattern re-sync whenever a SKP OS symbol is not recognized by the analyzer. For example because of a bit error or a wrong threshold setting.

Setting up SKP OS filtering

The following picture shows how to setup SKP OS filtering for the CCIX standard when using M8045A and M8046A.



On the Generator pattern, open Factory Patterns dialog and then navigate to e.g. CCIX/Test and select either:

- CCIX_modified_compliance_lane_0_CC_BIT_20G_25G or
- CCIX_modified_compliance_lane_0_IR_BIT_20G_25G

The pattern selection depends on whether the DUT uses a common clock (CC) or derives its own independent reference (IR) clock.

On the Analyzer pattern, open Factory Patterns dialog and then navigate to e.g. CCIX/Test. For the Analyzer pattern there is just a single pattern:

- CCIX_modified_compliance_lane_0_SKPOS_filtering_M8046A_BIT_20G_25G

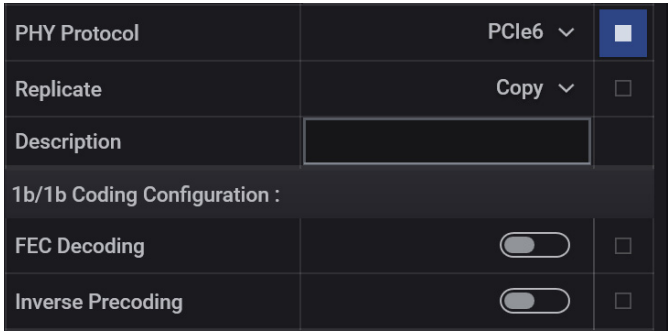
It is required as the difference between the CC and IR generator pattern files lies in the SKP OS symbol count which are getting removed before measuring the BER.

The above pattern is made specifically to fit to the M8046A modules memory granularity.

1b/1b Coding Configuration for PCIe6

The following two parameters are available under 1b/1b Coding Configuration:

- **FEC Decoding**: This option allows you to enable or disable the FEC decoding for PCIe6. When this option is enabled:
  - EIEOS are removed.
  - Information is required for Gray Coding in the PG pattern file. Error Detector will use the Gray coding to analyze the pattern.
  - Information is required for Descrambling in pattern file.
- **Inverse Precoding**: This option allows you to enable or disable the inverse precoding for PCIe6. This control is only available on the M8046A error detector. When this option is enabled, information is required for precoding in the PG pattern file.



Prerequisites

- For PCIe6 PHY protocol on M8046A, the allowed data rate is 64GT/s
- For PCIe6 PHY protocol, the Line Coding is selected as PAM4.

Error Counters available for PCIe6 1b/1b coding

The Error Ratio measurement automatically picks 1b/1b coding counter while opted in Sequence Editor.

The following new error counters are available for PCIe6 1b/1b coding configuration:

- **Filler Bits**: Total number of SKPOS bits removed (this is in terms of number of SKPOS bits).
- **Modified Filler Count**: Number of SKP Ordered Sets of non-nominal length which have been removed.
- **Filler Count**: Total number SKP ordered sets removed (this is in terms of number of SKPOS).
- **Flit Count**: Number of Received Flits.
- **FEC Corrected Bytes**: Number of bytes errored that FEC Decoder can correct.
- **FLIT CRC Error Count**: Number of errors detected in CRC checker.

For details on the common counters, refer to PAM4 symbol error counters on page 781.

The Symbol Errors tab displays the detailed information.

M2.DataIn

From Level \ To Level	0	1	2	3	Compared Symbols	Errored Symbols	Symbol Error Ratio
3	1.47e+19	0	1.42e+16	1.84e+19	1.47e+19	1.47e+19	1.00e+00
2	0	0	1.59e+18	1.31e+19	1.47e+19	1.31e+19	8.92e-01
1	0	1.59e+18	1.31e+19	0	1.47e+19	1.31e+19	8.92e-01
0	1.56e+19	1.76e+19	0	0	1.47e+19	1.76e+19	1.20e+00
					3.43e+18	3.14e+18	9.15e-01

The full detailed symbol counters are available in the **Calculated Results** pane and in the error detector's data tab when setting the 'Results View Mode' to Detailed.

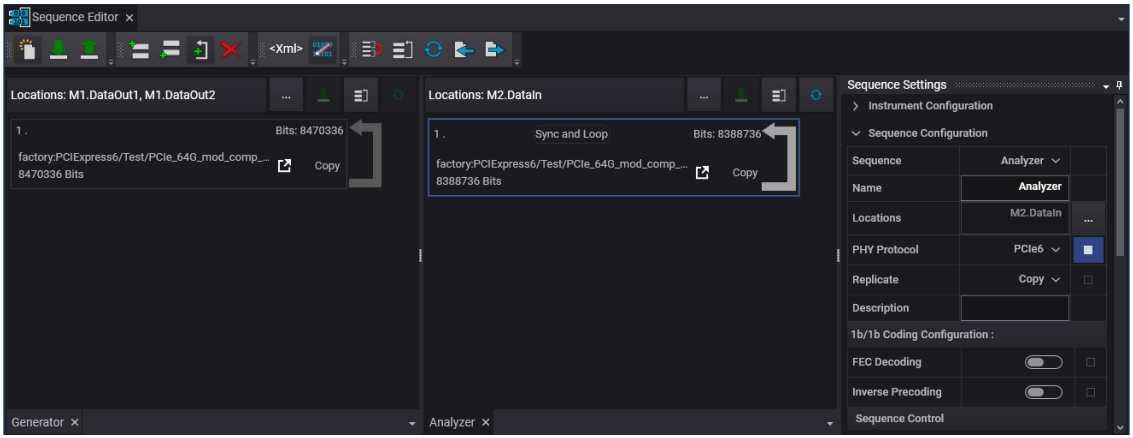
Calculated Results

Location	Show Graphics	Symbol Error Ratio	Compared Symbols	Errored Symbols	Error Ratio	Compared Bits	Errored Bits	Filler Bits	Modified Filler Count	Error Zero Ratio	Compared Zeros	Errored Zeroes	Error One Ratio	Compared Ones	Errored Ones	Filler Count	Flit Count	Fec Corrected Bytes	FLIT CRC Error Count
M2.DataIn		9.15e-01	3.43e+18	3.14e+18	2.50e-01	1.14e+17	2.84e+16	0.00e+00	0.00e+00	2.50e-01	5.68e+16	1.42e+16	2.50e-01	5.68e+16	1.42e+16	0.00e+00	0.00e+00	0.00e+00	0.00e+00

Symbol 2 Errored Symbols	Symbol 3 Received 0	Symbol 3 Received 1	Symbol 3 Received 2	Symbol 3 Received 3	Symbol 3 Error Ratio	Symbol 3 Compared Symbols	Symbol 3 Errored Symbols	Filler Bits	Modified Filler Count	Error Zero Ratio	Compared Zeros	Errored Zeroes	Error One Ratio	Compared Ones	Errored Ones	Filler Count	Flit Count	Fec Corrected Bytes	FLIT CRC Error Count
5.34e+18	6.48e+18	0.00e+00	5.44e+13	8.22e+02	1.00e+00	6.48e+18	6.48e+18	0.00e+00	0.00e+00	2.50e-01	2.17e+14	5.44e+13	2.50e-01	2.17e+14	5.44e+13	0.00e+00	0.00e+00	0.00e+00	0.00e+00
1.07e+19	1.30e+19	0.00e+00	5.44e+13	1.64e+03	1.00e+00	1.30e+19	1.30e+19	0.00e+00	0.00e+00	2.50e-01	2.17e+14	5.44e+13	2.50e-01	2.17e+14	5.44e+13	0.00e+00	0.00e+00	0.00e+00	0.00e+00
2.92e+18	7.48e+18	0.00e+00	5.44e+13	3.29e+03	1.00e+00	7.48e+18	7.48e+18	0.00e+00	0.00e+00	2.50e-01	2.18e+14	5.44e+13	2.50e-01	2.18e+14	5.44e+13	0.00e+00	0.00e+00	0.00e+00	0.00e+00
5.84e+18	1.50e+19	0.00e+00	5.44e+13	6.58e+03	1.00e+00	1.50e+19	1.50e+19	0.00e+00	0.00e+00	2.50e-01	2.18e+14	5.44e+13	2.50e-01	2.18e+14	5.44e+13	0.00e+00	0.00e+00	0.00e+00	0.00e+00
1.17e+19	1.15e+19	0.00e+00	5.44e+13	1.32e+04	1.00e+00	1.15e+19	1.15e+19	0.00e+00	0.00e+00	2.50e-01	2.18e+14	5.44e+13	2.50e-01	2.18e+14	5.44e+13	0.00e+00	0.00e+00	0.00e+00	0.00e+00
4.90e+18	4.47e+18	0.00e+00	5.44e+13	2.63e+04	1.00e+00	4.47e+18	4.47e+18	0.00e+00	0.00e+00	2.50e-01	2.18e+14	5.44e+13	2.50e-01	2.18e+14	5.44e+13	0.00e+00	0.00e+00	0.00e+00	0.00e+00

Setting up SKP OS filtering for PCIe6

The following picture shows how to setup SKP OS filtering for the PCIe6 standard when using M8045A and M8046A.



On the Generator pattern, open the Factory Patterns dialog and then navigate to e.g. PCIe6/Test.

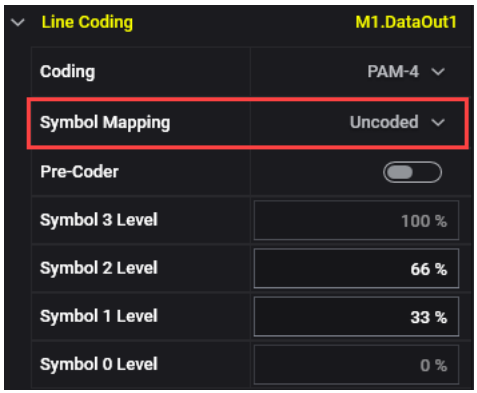
For PG, select the following pattern:

- PCIe_64G_mod_comp_pattern_PG.ptrn

For ED, select the following pattern:

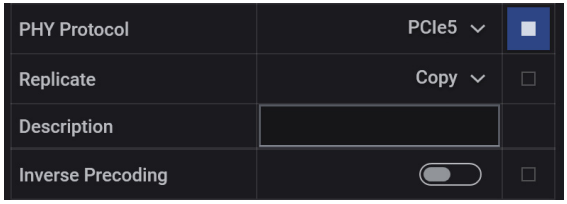
- If FEC Decoding is enabled, select: PCIe_64G_mod_comp_pattern_ED_FEC_enabled.ptrn
- If FEC Decoding is disabled, select: PCIe_64G_mod_comp_pattern_ED_FEC_disabled.ptrn

NOTE Patterns sent in the Factory folder require Symbol Mapping to be selected as "Uncoded".



Inverse Precoding for PCIe 5 PHY Protocol

This option allows you to enable or disable the inverse precoding for PCIe5. This control is only available on the M8046A error detector. When this option is enabled, information is required for precoding in the PG pattern file.

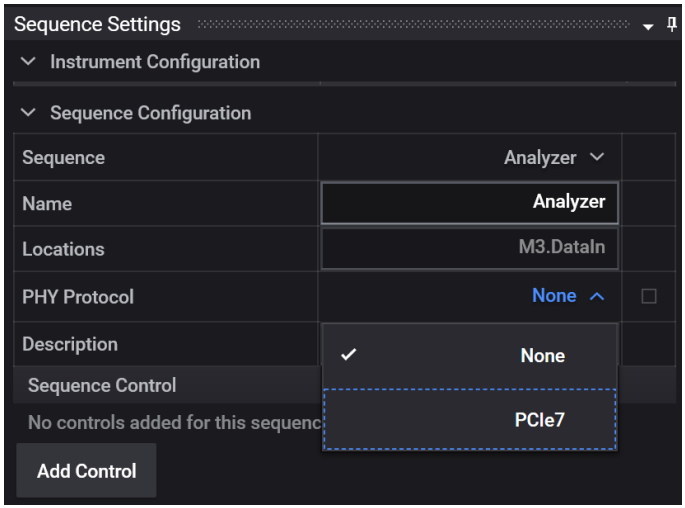


M8043A PHY Protocol Selection (SKP OS Filtering)

PHY Protocol

The M8043A module allows to specify a PHY protocol which can be supported by a specific sequence. This selection is done in the Sequence Editor when selecting a sequence which is bound to a module supporting this feature.

From the **Sequence Editor**, go to the **Sequence Configuration** block in the **Sequence Properties** side pane and select a PHY Protocol. For M8043A, only the PCIe7 protocol is available.



The available choices depend on the channels using the sequence.

For M8043A, the following is the possible option:

- M8043A-0S2 (US2, TS2): SKP OS Filtering for PCIe. For details refer to M8050A Licenses on page 836.

The available PHY protocol selections for this license are as follows:

- None - No specific sequence capability
- PCIe7 - Dedicated sequence setting for PCIe7

The PHY Protocol selection automatically defines the alignment, filler symbol sequences for the selected standard.

There is no option to manually enter these symbols on a sequence for a M8043A.

The PCIe7 protocol, the SKP OS filtering is active as soon as the sequence is downloaded.

NOTE **When selecting PCIe7 PHY protocol on M8043A, the maximum allowed data rate is 128GT/s.**

NOTE **Scrambler will not be available for M8050A.**

Only memory patterns are supported for the 'PCIe7' protocol. Using a PRBS pattern will result in an error. For 'PCIe7', PAM4 line coding should be used, and 1b/1b encoding should be enabled.

SKP Ordered Set filtering/removal

The M8043A module supports SKP OS filtering for the PCIe7 standard as defined in the respective specification.

NOTE **SKP OS filtering is available as per installed licenses (OS2 and the corresponding upgrade, or trial licenses).**

For the new module-specific options, please refer to M8050A Licenses on page 836.

This functionality removes all SKP ordered sets from the received data stream. When setting up a sequence for a BER measurement which is bound to the Error Detectors Data In, it is required for the pattern not to contain any SKP OS symbols. As these symbols are removed before comparing the received and expected data.

NOTE In case SKP OS filtering is active the expected pattern must not contain any SKP OS symbols as these will get removed before the received data stream is compared to the expected pattern.

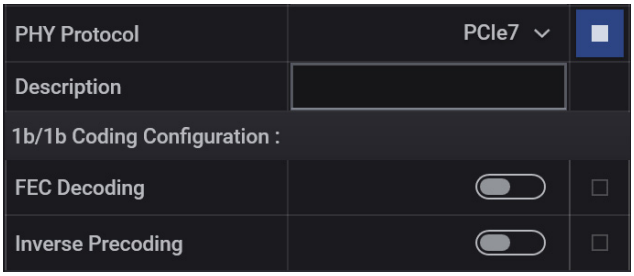
Whenever a SKP OS symbol is removed from the received data stream the expected pattern compare position is pinned down until past the SKP OS symbols duration to be able to compare the data. The necessity for modifying the compare position leads to the need to do a (manual or automatic) pattern re-sync whenever a SKP OS symbol is not recognized by the analyzer. For example, because of a bit error or a wrong threshold setting.

Use the **Sampling Point Setup** window to optimize BER. For details, see How to Optimize BER using a Sampling Point Setup on page 557.

1b/1b Coding Configuration for PCIe7

The following two parameters are available under 1b/1b Coding Configuration:

- **FEC Decoding**: This option allows you to enable or disable the FEC decoding for PCIe7. When this option is enabled:
  - EIEOS are removed.
  - Information is required for Gray Coding in the PG pattern file. Error Detector will use the Gray coding to analyze the pattern.
  - Information is required for Descrambling in pattern file.
- **Inverse Precoding**: This option allows you to enable or disable the inverse precoding for PCIe7. This control is only available on the M8043A error detector. When this option is enabled, information is required for precoding in the PG pattern file.



Prerequisites

- For PCIe7 PHY protocol on M8043A, the allowed data rate is 128GT/s
- For PCIe7 PHY protocol, the Line Coding is selected as PAM4.

Error Counters available for PCIe7 1b/1b Coding

The Error Ratio measurement automatically picks 1b/1b coding counter while opted in Sequence Editor.

The following new error counters are available for PCIe7 1b/1b coding configuration:

- **Filler Bits**: Total number of SKPOS bits removed (this is in terms of number of SKPOS bits).
- **Modified Filler Count**: Number of SKP Ordered Sets of non-nominal length which have been removed.
- **Filler Count**: Total number SKP ordered sets removed (this is in terms of number of SKPOS).
- **Flit Count**: Number of Received Flits.
- **FEC Corrected Bytes**: Number of bytes errored that FEC Decoder can correct.
- **FLIT CRC Error Count**: Number of errors detected in CRC checker.

For details on the common counters, refer to PAM4 symbol error counters on page 781.

The Symbol Errors tab displays the detailed information.

M2.DataIn

From Level \ To Level	0	1	2	3	Compared Symbols	Errored Symbols	Symbol Error Ratio
3	1.47e+19	0	1.42e+16	1.84e+19	1.47e+19	1.47e+19	1.00e+00
2	0	0	1.59e+18	1.31e+19	1.47e+19	1.31e+19	8.92e-01
1	0	1.59e+18	1.31e+19	0	1.47e+19	1.31e+19	8.92e-01
0	1.56e+19	1.76e+19	0	0	1.47e+19	1.76e+19	1.20e+00
					3.43e+18	3.14e+18	9.15e-01

The full detailed symbol counters are available in the **Calculated Results** pane and in the error detector's data tab when setting the 'Results View Mode' to Detailed.

Calculated Results

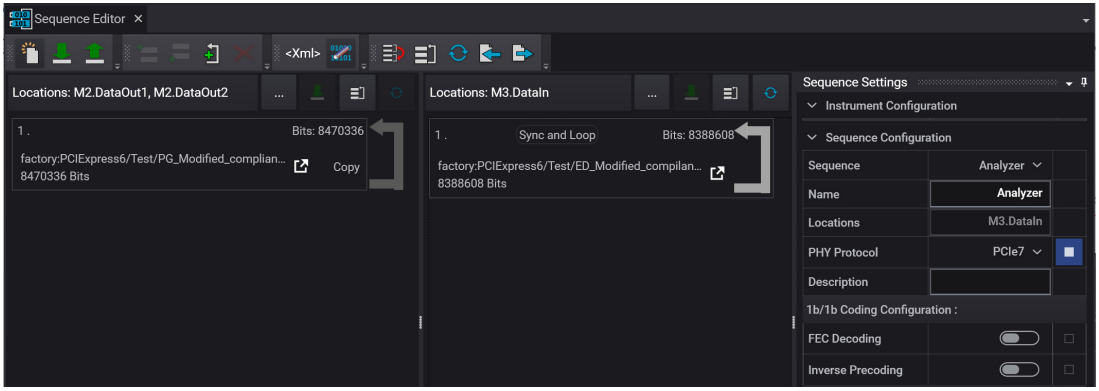
Location	Show Graphics	Symbol Error Ratio	Compared Symbols	Errored Symbols	Error Ratio	Compared Bits	Errored Bits	Filler Bits	Modified Filler Count	Error Zero Ratio	Compared Zeros	Errored Zeroes	Error One Ratio	Compared Ones	Errored Ones	Filler Count	Flit Count	Fec Corrected Bytes	FLIT CRC Error Count
M2.DataIn		9.15e-01	3.43e+18	3.14e+18	2.50e-01	1.14e+17	2.84e+16	0.00e+00	0.00e+00	2.50e-01	5.68e+16	1.42e+16	2.50e-01	5.68e+16	1.42e+16	0.00e+00	0.00e+00	0.00e+00	0.00e+00

Symbol 2 Errored Symbols	Symbol 3 Received 0	Symbol 3 Received 1	Symbol 3 Received 2	Symbol 3 Received 3	Symbol 3 Error Ratio	Symbol 3 Compared Symbols	Symbol 3 Errored Symbols	Filler Bits	Modified Filler Count	Error Zero Ratio	Compared Zeros	Errored Zeroes	Error One Ratio	Compared Ones	Errored Ones	Filler Count	Flit Count	Fec Corrected Bytes	FLIT CRC Error Count
5.34e+18	6.48e+18	0.00e+00	5.44e+13	8.22e+02	1.00e+00	6.48e+18	6.48e+18	0.00e+00	0.00e+00	2.50e-01	2.17e+14	5.44e+13	2.50e-01	2.17e+14	5.44e+13	0.00e+00	0.00e+00	0.00e+00	0.00e+00
1.07e+19	1.30e+19	0.00e+00	5.44e+13	1.64e+03	1.00e+00	1.30e+19	1.30e+19	0.00e+00	0.00e+00	2.50e-01	2.17e+14	5.44e+13	2.50e-01	2.17e+14	5.44e+13	0.00e+00	0.00e+00	0.00e+00	0.00e+00
2.92e+18	7.48e+18	0.00e+00	5.44e+13	3.29e+03	1.00e+00	7.48e+18	7.48e+18	0.00e+00	0.00e+00	2.50e-01	2.18e+14	5.44e+13	2.50e-01	2.18e+14	5.44e+13	0.00e+00	0.00e+00	0.00e+00	0.00e+00
5.84e+18	1.50e+19	0.00e+00	5.44e+13	6.58e+03	1.00e+00	1.50e+19	1.50e+19	0.00e+00	0.00e+00	2.50e-01	2.18e+14	5.44e+13	2.50e-01	2.18e+14	5.44e+13	0.00e+00	0.00e+00	0.00e+00	0.00e+00
1.17e+19	1.15e+19	0.00e+00	5.44e+13	1.32e+04	1.00e+00	1.15e+19	1.15e+19	0.00e+00	0.00e+00	2.50e-01	2.18e+14	5.44e+13	2.50e-01	2.18e+14	5.44e+13	0.00e+00	0.00e+00	0.00e+00	0.00e+00
4.90e+18	4.47e+18	0.00e+00	5.44e+13	2.63e+04	1.00e+00	4.47e+18	4.47e+18	0.00e+00	0.00e+00	2.50e-01	2.18e+14	5.44e+13	2.50e-01	2.18e+14	5.44e+13	0.00e+00	0.00e+00	0.00e+00	0.00e+00

Setting up SKP OS filtering for PCIe7

The following picture shows how to set up SKP OS filtering for the PCIe7 standard when using M8042A and M8043A.

On the **Generator** pattern, open the **Factory Patterns** dialog and then navigate to e.g. **PCIe6** > **Test**.



For Pattern Generator, select one of the following patterns:

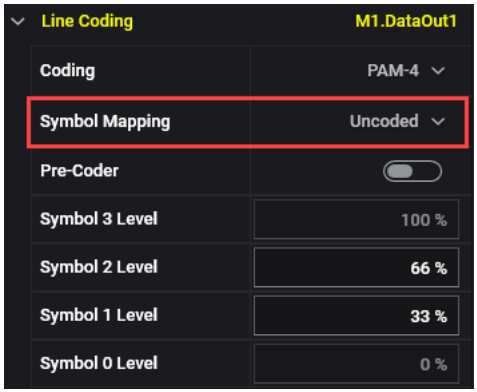
- PG_Modified_Compliance_not_precoded.ptrn
- PG_Modified_Compliance_precoded.ptrn

NOTE If a pre-coded pattern is selected, the 'Inverse Precoding' option under 1b/1b Coding Configuration in the Sequence Editor should be selected.

For Error Detector, select the following pattern:

- If FEC Decoding is enabled, select:
  ED_Modified_compilance_FEC_enable_not_precoded.ptrn
- If FEC Decoding is disabled, select:
  ED_Modified_compliance_FEC_disable_not_precoded.ptrn

NOTE Patterns sent in the Factory folder require Symbol Mapping to be selected as "Uncoded".



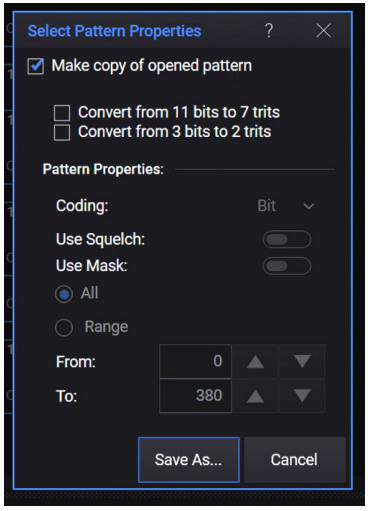
Using Pattern Shift and 3b2s Mapping in M8070B

The pattern shift and 3b2s mapping features are supported by M8045A pattern generator module.

Follow the given steps to use the pattern shift:

1 Open an existing unmapped pattern file or create a new pattern from the **Pattern Editor** window. For details on the **Pattern Editor** window and how to open a pattern file or create a new pattern, refer to the Pattern Editor on page 655.

2 Click on the "**Save As**" button. The following "**Select Pattern Properties**" dialog will appear. This dialog allows you to save the mapped pattern.



3 Select the "**Convert from 3 bits to 2 trits**" option in the dialog and then click "**Save As**" This will open a "**Choose PAM Custom Symbol Mapping**" dialog. This dialog allows you to select the custom mapping file according to which the mapping will be done.

4 Click "**Select**". A "**Save Pattern As**" dialog will appear. Save the pattern file to the desired location and then click "**Save**". The mapped pattern will now appear in the pattern editor with **Data View Mode** changed to PAM3 by default.

5 If you open a pattern file that is already saved using the 3-bit to 2-symbol mapping, you can go to **Settings** > **Data View Mode**, and select the "**PAM3**" coding option. This will show you the PAM3 symbols.

6 Click the **Block Edit** icon available on the toolbar. This will open the **Block Edit** window.

7 In the **Block Edit** window, click the **Rotate** tab to specify the number of symbols you want to shift.

8 Click **Apply**. The pattern is rotated by the number of symbols you have defined. Ensure that the **Data View Mode** is selected as PAM3.

9 Save the rotated pattern again, as described earlier.

10 Repeat this process until all the desired rotated patterns are saved in the memory.

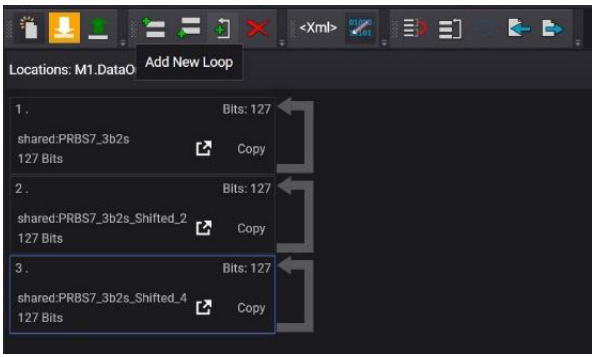
Process for Data Verification

Follow the given steps to verify the 3b2s mapped pattern shift:

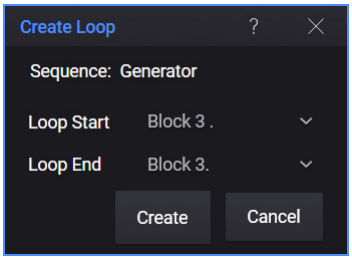
1 From the main menu, click **Patterns** > **Sequence Editor**.

2 Click the "**Add Block**" icon to insert a block after the selected block. You may add the number of blocks equivalent to the shifted patterns you have.

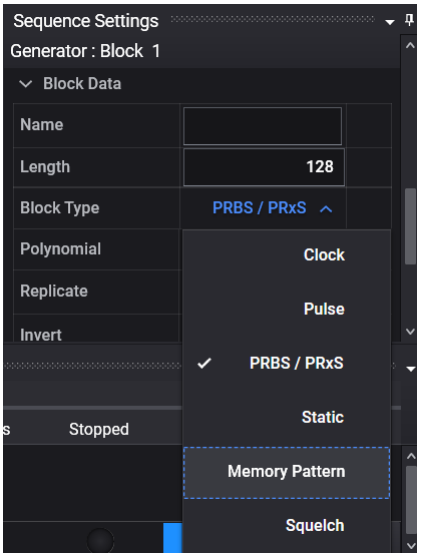
3 Create an infinite loop on the block to avoid any pattern length limitations. To achieve this, click the **Add New Loop** icon available on the toolbar and add the loops as shown in the following figure:



4 Set the same value for the '**Loop Start**' and '**Loop End**' blocks and then click **Create**.



5 In the **Generator: Block** options on the right pane, from the **Block Type** drop-down options, select **Memory Pattern** tab.



6 Load the pattern saved earlier using **Pattern Editor**.

7 Load all the blocks with shifted patterns and then click **Download this sequence** icon to load the entire sequence into memory. Before loading the sequence, ensure to enable the "**Custom Mapping**" option in the **Line Coding** functional block.

8 On the right pane, click **Block Branches** > **Add Branch**.

9 Leave the branch settings to the default values.

10 Add branches to all blocks and then click the download button to download the pattern into memory.

11 After downloading, the pattern loaded into first block is at the output. For example, if you download a simple non-shifted 3b2s mapped pattern, it can be verified in the status indicator.

12 After all the settings are configured, use any of the patterns defined into blocks by clicking the **Break** button, which switches from one block to another.

13 You may optionally use the remote programming SCPI command `:DATA:SEQ:BRE 'M1.System'` (alternative to using the break button in the user interface) to shift to another block. Additionally, use `:DATA:SEQ:REST 'Generator',3` with two identifiers; where the first one is the Sequence name and the second one the block number to switch from one block to another arbitrarily. Also, use `:DATA:SEQ:BLOCK? 'Generator'` to verify the block number currently being executed.

14 The following image shows the pattern shifted by 4 symbols at the output, which can be verified in the status indicator.

15 For more information on the SCPI commands pertaining to this feature, refer to the *M8000 Series Programming Guide*.

16 One of the best practices is to save the instrument state and perform a recall the next time, without repeating the entire procedure all over. To do this, click **File** > **Save Instrument State**.

Known Limitations

Following are the known limitations of using this approach:

1. PRBS is not hardware generated, but the patterns are the same as generated by the hardware.
2. Length of the pattern used must be a multiple of 3.
3. Maximum number of blocks may be set to 500, but it will also be limited by the pattern length & number of times pattern have to be rolled out.
4. Pre-coder feature is not supported.

M8000 Series of BER Test Solutions
User Guide

8 Working with Measurements

Overview / 766
Exploring Measurement User Interface / 767
Error Ratio Measurement / 774

KEYSIGHT TECHNOLOGIES

Overview

The M8070B system software provides the following types of measurements:

- Error Ratio

In addition, the M8070B system software also provides the following measurements will be only available on installing the following plugins:

- **Advanced Measurement Package**

  The **Advanced Measurement Package** provides the following measurements:

  - Output Timing
  - Output Level
  - Jitter Tolerance
  - Eye Diagram
  - Parameter Sweep
  - BER Based Deemphasis

  For details on the measurements provided by **Advanced Measurement Package**, refer to *M8000 Series Advanced Measurement Package User Guide*.

- **Error Distribution Analysis Package**

  The **Error Distribution Analysis Package** provides the following measurement:

  - Error Distribution Analysis

  For details on the measurement provided by **Error Distribution Analysis Package**, refer to *M8000 Series Error Distribution Analysis Package User Guide*.

NOTE

Please note that the M8046A module only supports the following measurements:

- Error Ratio
- Output Timing
- Jitter Tolerance
- Parameter Sweep
- BER Based Deemphasis

Exploring Measurement User Interface

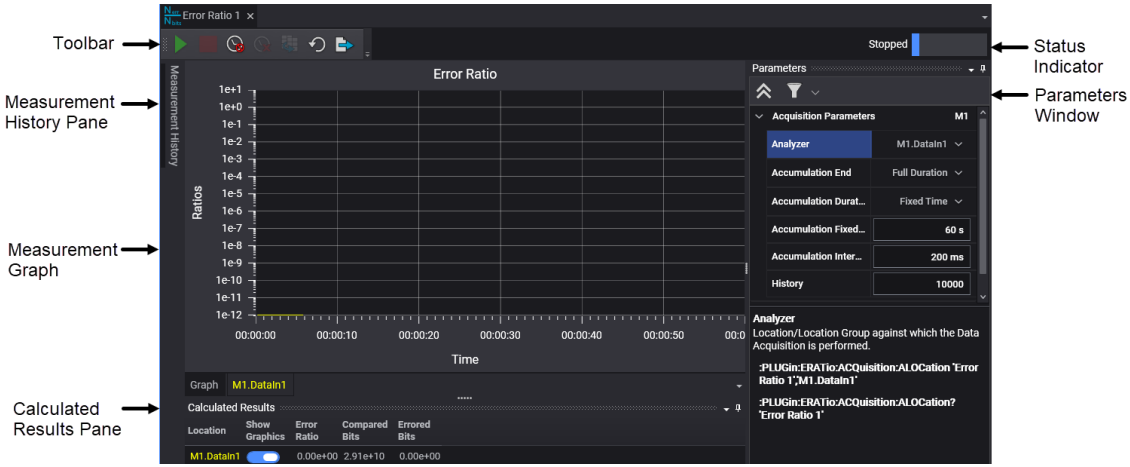
This section describes the functionality provided by the measurement user interface.

Launching the Measurement User Interface

To launch the measurement user interface:

- Go to the **Menu Bar** > **Measurements** and then select the respective measurements (**Error Ratio**, **Output Timing, Output Level** or **Jitter Tolerance**) to launch the measurement user interface.

The following figure shows the measurement user interface:



The measurement user interface has the following GUI elements, which are common to all measurements:

- Toolbar
- Status Indicator
- Measurement History Pane
- Measurement Graph
- Parameter Window
- Calculated Results Pane

Lets discuss these GUI elements in the following sections.

Toolbar

The toolbar contains the following icons:

Table 72

Elements	Name	Description
	Start /Continue Measurement	Starts a measurement.
	Break Measurement	Halts the measurement at that point. Once paused, you can continue the measurement again by pressing **Continue Measurement** icon. Note: This option is not available in **Error Ratio Measurement**.
	Stop Measurement	Stops the measurement.
	Step Into Measurement	Steps further into the measurement. Note: This option is not available in **Error Ratio Measurement**.
	Enable/Disable Measurement Run History	Enables or disables the measurement run history. For details, refer to Measurement History Window on page 769.
	Clear Measurement History	Clears the measurement run history.
	Copy Measurement History Properties	Copies the measurement history properties to the currently running measurement.
	Reset Measurement	Resets the measurement to its default values.
	Export Data to CSV	Exports the measurement data in the CSV file format. For more information, see Exporting Measurement Results on page 773.

Status Indicator

The status indicator shows the current state of a measurement. There can be various states of a measurement, depending on the type of measurement. These may be as follows:

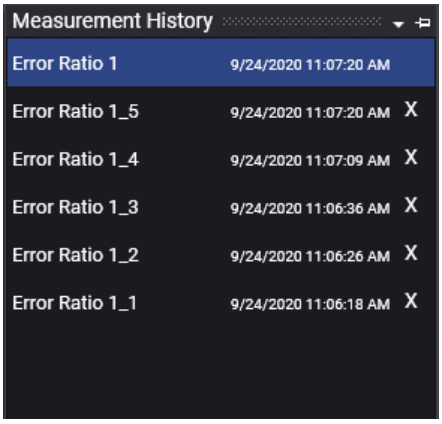
- **Not Started**: Indicates that the measurement has not yet started.
- **Running**: Indicates that the measurement is currently running.
- **Stop**: Indicates that the measurement is stopped.
- **Error**: Indicates an error while executing the measurement which is caused due to invalid parameter settings.
- **Suspended**: Indicates that the measurement is suspended.
- **Finished**: Indicates that the measurement is completed.

The following figure shows the status indicator while the measurement is running:

Measurement History Window

The **Measurement History** window maintains the history of executed measurement along with their time stamp. This allows you to refer to the previously run measurements and compare their results.

The **Measurement History** window is shown in the figure below:



Click the icon to toggle between the enable/disable measurement run history in the Measurement History window.

Copy Measurement History Properties

This feature allows you to copy the properties of run measurement to currently running measurement.

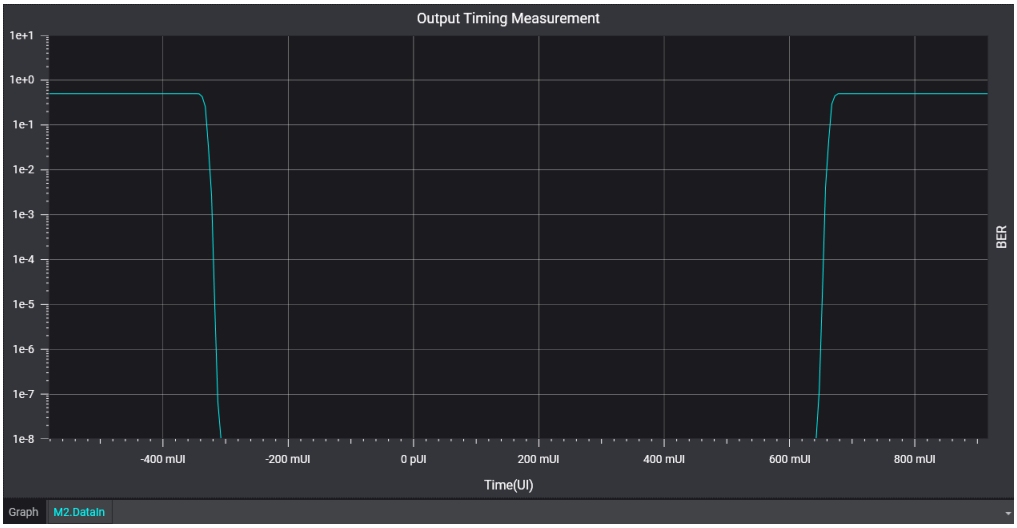
To do so,

- Select a measurement history from the list shown in the **Measurement History** window.
- Click the **Copy Measurement History Properties** icon. The properties of the selected measurement will be copied to the current measurement.

Measurement Graph

The **Measurement Graph** displays the calculated graph and results.

The following figure displays the **Measurement Graph** of the **Output Timing Measurement**.



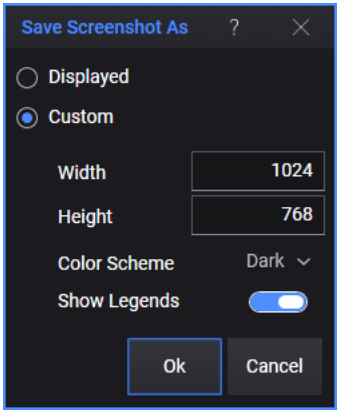
The **Measurement Graph** contains the following tabs:

- **Graph**: Displays the graphical representation of the measurement. The graph varies from measurement to measurement. The details of each measurement graph are further described in their respective sections.
- **Location**: Displays the raw measurement data for that location. However, if you are running measurement for a group, multiple tabs will appear that display the raw measurement for each location.

When you right-click on the **Measurement Graph**, a context menu appears which provides the following options:

- **Turn ON/OFF Fit to view (Ctrl+Home)** - Turns ON/OFF **Fit to view** option.
- **Fit to view (Home)** - Makes the visible area fit to display entire contents.
- **Copy screenshot (F11)** - Copies the screenshot of charts to clipboard.
- **Save screenshot (Ctrl+S)** - Saves the screenshot as an image (PNG) under a name.

  Clicking this option displays the **Save Screenshot As** dialog box.



a On the **Save Screenshot As** dialog box, select one of the following:
   - **Displayed:** Saves the screenshot with default properties.
   - **Custom:** Enables you to set the custom properties of the image. The following properties are available:
     - **Width**: Sets the width value of the image.
     - **Height**: Sets the height value of the image.

- **Color Scheme**: Enables you to select a color scheme for the image. Two options; Dark and Light are available.
- **Show Legends**: Allows you to save the legends in the screenshot.

b Click **OK** to save the screenshot.

- **Quick Help (Alt+F1)** - Opens a window that provides brief information about the dynamic display.

Parameters Window

The **Parameter** window allows you to set the parameters for a location or a group. For each measurement, it contains two types of parameters:

- **Acquisition Parameters** - Pre-Parameters influence how the data for a measurement is collected; changes require a re-run in order to be effective. It also allows you to select a location or location group against which the data acquisition is performed.
- **Evaluation Parameters** - Post-Parameters influence how the collected measurement data is evaluated. Changes do not require a re-run in order to be effective.

The acquisition and evaluation parameters differ from measurement to measurement. The detailed description of these parameters are explained in the sections that follow.

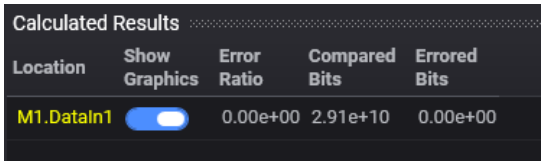
Calculated Results Pane

The **Calculated Results** pane displays the calculated results in the form of measurement parameters for each location. The calculated measurement parameters varies from measurement to measurement.

NOTE

The BER measurement processes at least as many bits as defined by the acquisition parameters, it stops when the end criteria is reached or exceeded. Due to update period and hardware granularities, an individual BER measurement will typically process more bits than configured.

The **Calculated Results** pane is shown in the following figure:



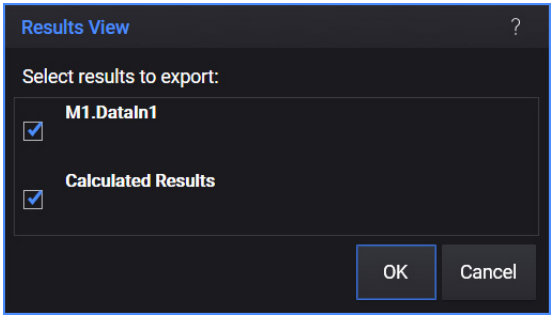
For each location, you can click on the slide button to show/hide the measurement graph.

Exporting Measurement Results

You can export the measurement results to a CSV format. To do so:

1 Click the (Export Data to CSV) button.

The **Results View** dialog will appear that allows you to select one or more results to export:



2 Select the required results, such as, "*M*.DataIn*" or "*Calculated Results*", and so on (depending on the type of measurement).

3 Click **OK**.

A standard **Save As** dialog will appear.

4 Provide a filename and location.

5 Click **Save**.

A confirmation dialog indicates that the measurement results have been successfully exported to a CSV format.

Error Ratio Measurement

Overview

The **Error Ratio Measurement** allows you to collect measurement data over a specific period. This can be used to create test scenarios that are reproducible and comparable. Also, you can let tests run over long times and then evaluate the results afterwards.

NOTE While the error ratio measurement is running, you should not modify the measurement setup, as the measured bit errors do not represent the performance of your DUT under real circumstances.

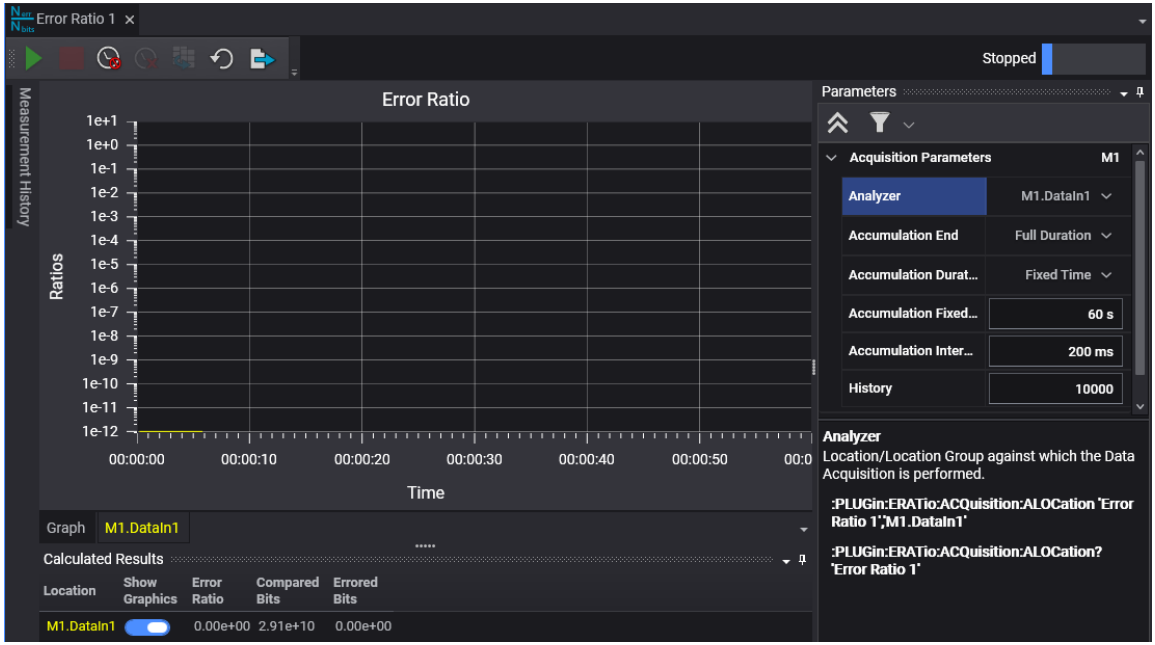
The period of time can be set through the **Parameters** window, an absolute time setting, or the time it takes to measure a specified number of bits or bit errors. The accumulation period should be long enough to make a statistically valid BER measurement.

Launching Error Ratio Measurement

To launch the **Error Ratio Measurement**:

- Go to the **Menu Bar** > **Measurements** and then select **Error Ratio**.

The user interface of **Error Ratio Measurement** will appear as shown in the following figure:



The **Error Ratio** user interface includes the following elements:

- **Toolbar**: For details, refer to Toolbar on page 768.
- **History Pane**: For details, refer to Measurement History Window on page 769.
- **Measurement Graph**: For details, refer to Measurement Graph on page 780.
- **Parameter Pane**: For details, refer to Acquisition and Evaluation Parameters for Error Ratio on page 776.
- **Calculated Results**: For details, refer to Calculated Results on page 783.

Acquisition and Evaluation Parameters for Error Ratio

The **Parameters** window allows you to set the acquisition and evaluation parameters for **Error Ratio** measurement:

Table 73

Parameters	Description	Values
Acquisition Parameters		
Analyzer Location	Location or location group against which the data acquisition is performed.	Use the drop-down list to specify the location or location group.
Accumulation End	Specify the criteria to end accumulation.	Pass/Fail | Full Duration | Number of Bits
Accumulation Duration	Specify the acquisition duration.	Fixed Time | Indefinitely
Accumulation Fix Time	Specifies the duration of the accumulation. This is a conditional parameter and appear when the **Accumulation Duration** as selected as **Fixed Time**.	Min - 1 s Max - 31.5 Ms
Accumulation Interval	Specify the accumulation interval on which the error ratio sample is taken.	Min - 100 µs Max - 2 Ms
Accumulation Stop Criteria	Specify the accumulation end criteria when measurement is run on a group of analyzers.	Per Analyzer | Combined Analyzer
Number of Compared Bits	Specify the number of compared bits for which the error ratio sample is taken. This is a conditional parameter and appear when the **Accumulation End** as selected as **Number of Bits**.	Min - 1E+6 Max - 1E+18
Target Error Ratio	Specifies the target error ratio of the accumulation results. This is a conditional parameter and appear when the **Accumulation End** as selected as **Pass/Fail**.	Min - 1E -18 Max -1E-3
Target Confidence Level	Specifies the target confidence level of the accumulation results. This is a conditional parameter and appear when the **Accumulation End** as selected as **Pass/Fail**.	Min - 0.1 % Max - 99.9 %

Parameters	Description	Values
History	Defines the number of accumulation values that are kept in memory.	Min - 1 Max - 100000
Evaluation Parameters		
Results View Mode	Allows to view the calculated results in either detailed or summarized mode.	Detailed | Summary
Display Error Ratio	Displays the error ratio of the accumulated results. This is a conditional parameter and appear when the **Results View Mode** is selected as “Detailed”.	Erroneous Zero Ratio | Erroneous One Ratio | Error Ratio

How to Run a Measurement

The **Error Ratio** measurement immediately starts calculating the error ratio as soon as it receives a valid signal and the respective error ratio settings are done.

To run an **Error Ratio** measurement, perform the following steps:

- Use the **Parameters** window to select the location or location group for which the data acquisition has to be performed.
- Set the acquisition parameters in the **Parameters** window. For details, refer to Acquisition and Evaluation Parameters for Error Ratio on page 776.
- Click the **Start Measurement** icon to run the measurement. The measurement status indicator will indicate **Running**.

NOTE

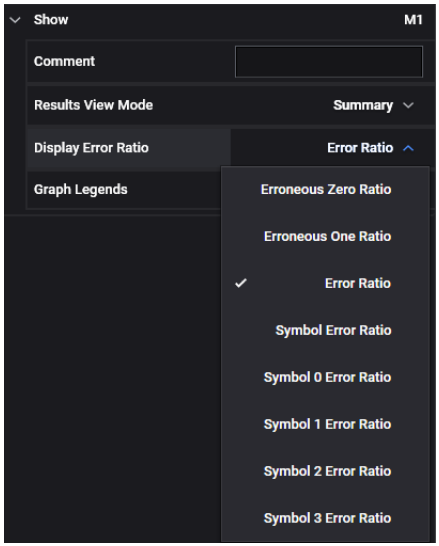
Please note that once you run the measurement you cannot modify the acquisition parameters. However, if you try to modify acquisition parameters by stopping the measurement and then run the measurement, a new instance of measurement will be executed.

NOTE The BER measurement processes at least as many bits as defined by the acquisition parameters, it stops when the end criteria is reached or exceeded. Due to update period and hardware granularities, an individual BER measurement will typically process more bits than configured.

Error Ratio Measurement with PAM4 Symbols

The M8040A modular system allows you to run the **Error Ratio** measurement using the PAM4 symbols. To do so,

- Switch to the **Module View**.
- From the Generator (M8045A), select **Data Out** location. Choose the **Line Coding** as **PAM4** in the **Parameter** window.
- From the Analyzer (M8046A), select **Data In** location. Choose the **Line Coding** as **PAM4** in the **Parameter** window.
- Once done, switch to **Error Ratio** measurement.
- Set the acquisition parameters in the **Parameters** window. For details, refer to Acquisition and Evaluation Parameters for Error Ratio on page 776.
- Click the **Start Measurement** icon to run the measurement. The measurement status indicator will indicate **Running**.
- The **Display Error Ratio** in the **Parameter** window will now show the error ratio for various symbol levels (0-3) as shown in the following figure:



- See Calculated Results on page 783 for the results which are displayed when an **Error Ratio** measurement is performed with PAM4 line coding.

How to Stop a Measurement

To stop an **Error Ratio** measurement:

- Click the **Stop Measurement** icon to stop the measurement.

Measurement Graph

Once you run an **Error Ratio** measurement for a specified duration, the calculated graph and the raw data is shown on the measurement graph as follows:

This graph displays the delta errored 1's ratio, delta errored 0's ratio, and total delta error ratio at data points over the entire accumulation period. The error ratios on the y-axis are set to a range of 1E+0 (100% errors) to 1E-12. The accumulation period is on the x-axis.

Display Change

During accumulation, data will appear to move from left to right on the ratios graph. When the graph is completely filling the display, the x-axis time scale will double. The data graph is then occupying only half of the display and will continue to move to the right again. This will repeat until the accumulation period has ended.

Measurement Data

The following figure shows the raw measurement data for the selected location.

TimeStamp	Symbol Error Ratio	Compared Symbols	Errored Symbols	Error Ratio	Compared Bits	Errored Bits
00:00:20:078	5.00e-01	4.11e+18	2.06e+18	2.50e-01	6.16e+12	1.54e+12
00:00:40:066	5.00e-01	8.22e+18	4.11e+18	2.50e-01	6.16e+12	1.54e+12
00:01:00:080	5.00e-01	1.64e+19	8.22e+18	2.50e-01	6.16e+12	1.54e+12
00:01:21:286	1.14e+00	1.44e+19	1.64e+19	2.50e-01	6.17e+12	1.54e+12
00:01:40:091	1.38e+00	1.04e+19	1.44e+19	2.50e-01	6.17e+12	1.54e+12
00:02:00:034	4.33e+00	2.41e+18	1.04e+19	2.50e-01	6.18e+12	1.54e+12
00:02:20:005	5.00e-01	4.81e+18	2.41e+18	2.50e-01	6.18e+12	1.54e+12
00:02:39:951	5.00e-01	9.62e+18	4.81e+18	2.50e-01	6.18e+12	1.55e+12
00:03:01:093	1.21e+01	7.95e+17	9.62e+18	2.50e-01	6.19e+12	1.55e+12
00:03:20:738	5.00e-01	1.59e+18	7.95e+17	2.50e-01	6.19e+12	1.55e+12

Graph | Symbol Errors | M2.DataIn

Test Times and Confidence Levels

A true **Error Ratio** measurement must be statistically valid. Because it is not possible to predict with certainty when errors will occur, your device must be tested long enough to have confidence in its **Error Ratio** performance.

PAM4 symbol error counters

The PAM4 error counters provide detailed information about the number of times a certain PAM4 symbol has been received for every expected symbol level. This can be used to analyze error mechanism and to optimize threshold settings. The detailed error information is accessible in the error ratio measurement, and via remote commands.

In offline configurations, the error counter simulation supports the PAM4 symbol counters in full detail, but has limitations in reporting plausible numbers for received symbols when the symbol error ratio is high.

The detailed PAM4 counters are available on M8046A (real-time counting in the error detector hardware) and for real-time oscilloscopes (from post-processing the captured waveform).

The Symbol Errors tab displays the detailed information.

M2.DataIn

From Level \ To Level	0	1	2	3	Compared Symbols	Errored Symbols	Symbol Error Ratio
3	1.21e+18	0	1.55e+13	6.29e+06	1.21e+18	1.21e+18	1.00e+00
2	0	0	1.21e+18	0	1.21e+18	0	0.00e+00
1	0	1.21e+18	0	0	1.21e+18	0	0.00e+00
0	6.29e+06	1.21e+18	0	0	1.21e+18	1.21e+18	1.00e+00
					4.83e+18	2.41e+18	5.00e-01

The full detailed PAM4 symbol counters are available in the **Calculated Results** pane and in the error detector's data tab when setting the 'Results View Mode' to Detailed.

Calculated Results

Location	Show Graphics	Symbol Error Ratio	Compared Symbols	Errored Symbols	Error Ratio	Compared Bits	Errored Bits	Symbol 0 Received 0	Symbol 0 Received 1	Symbol 0 Received 2	Symbol 0 Received 3	Symbol 0 Error Ratio	Symbol 0 Compared Symbols	Symbol 0 Errored Symbols	Symbol 1 Received 0	Symbol 1 Received 1	Symbol 1 Received 2	Symbol 1 Received 3
M2.DataIn		0.00e+00	1.42e+14	0.00e+00	0.00e+00	2.85e+14	0.00e+00	3.56e+13	0.00e+00	0.00e+00	0.00e+00	0.00e+00	3.56e+13	0.00e+00	0.00e+00	3.56e+13	0.00e+00	0.00e+00

TimeStamp	Symbol Error Ratio	Compared Symbols	Errored Symbols	Error Ratio	Compared Bits	Errored Bits	Symbol 0 Received 0	Symbol 0 Received 1	Symbol 0 Received 2	Symbol 0 Received 3	Symbol 0 Error Ratio	Symbol 0 Compared Symbols	Symbol 0 Errored Symbols	Symbol 1 Received 0	Symbol 1 Received 1	Symbol 1 Received 2	Symbol 1 Received 3	Symbol 1 Error Ratio	Symbol 1 Compared Symbols	Symbol 1 Errored Symbols
00:00:20:078	5.00e-01	4.11e+18	2.06e+18	2.50e-01	6.16e+12	1.54e+12	6.00e+00	1.03e+18	0.00e+00	0.00e+00	1.00e+00	1.03e+18	1.03e+18	0.00e+00	1.03e+18	0.00e+00	0.00e+00	0.00e+00	1.03e+18	0.00e+00
00:00:40:066	5.00e-01	8.22e+18	4.11e+18	2.50e-01	6.16e+12	1.54e+12	1.20e+01	2.06e+18	0.00e+00	0.00e+00	1.00e+00	2.06e+18	2.06e+18	0.00e+00	2.06e+18	0.00e+00	0.00e+00	0.00e+00	2.06e+18	0.00e+00
00:01:00:080	5.00e-01	1.64e+19	8.22e+18	2.50e-01	6.16e+12	1.54e+12	2.40e+01	4.11e+18	0.00e+00	0.00e+00	1.00e+00	4.11e+18	4.11e+18	0.00e+00	4.11e+18	0.00e+00	0.00e+00	0.00e+00	4.11e+18	0.00e+00
00:01:21:286	1.14e+00	1.44e+19	1.64e+19	2.50e-01	6.17e+12	1.54e+12	4.80e+01	8.22e+18	0.00e+00	0.00e+00	1.00e+00	8.22e+18	8.22e+18	0.00e+00	8.22e+18	0.00e+00	0.00e+00	0.00e+00	8.22e+18	0.00e+00
00:01:40:091	1.38e+00	1.04e+19	1.44e+19	2.50e-01	6.17e+12	1.54e+12	9.60e+01	1.64e+19	0.00e+00	0.00e+00	1.00e+00	1.64e+19	1.64e+19	0.00e+00	1.64e+19	0.00e+00	0.00e+00	0.00e+00	1.64e+19	0.00e+00
00:02:00:034	4.33e+00	2.41e+18	1.04e+19	2.50e-01	6.18e+12	1.54e+12	1.92e+02	1.44e+19	0.00e+00	0.00e+00	1.00e+00	1.44e+19	1.44e+19	0.00e+00	1.44e+19	0.00e+00	0.00e+00	0.00e+00	1.44e+19	0.00e+00
00:02:20:005	5.00e-01	4.81e+18	2.41e+18	2.50e-01	6.18e+12	1.54e+12	3.84e+02	1.04e+19	0.00e+00	0.00e+00	1.00e+00	1.04e+19	1.04e+19	0.00e+00	1.04e+19	0.00e+00	0.00e+00	0.00e+00	1.04e+19	0.00e+00

Calculated Results

The following results are displayed when the bit coded patterns are loaded in **Sequence Editor**:

Calculated Results

Location	Show Graphics	Error Ratio	Compared Bits	Errored Bits	Error Zero Ratio	Compared Zeros	Errored Zeroes	Error One Ratio	Compared Ones	Errored Ones
M2.DataIn		0.00e+00	9.01e+09	0.00e+00	0.00e+00	4.51e+09	0.00e+00	0.00e+00	4.51e+09	0.00e+00

- **Errored Zeros**: Displays the number of errored zeros during the accumulation period.
- **Errored Ones**: Displays the number of errored ones during the accumulation period.
- **Error Bits**: Displays the number of errored bits during the accumulation period.
- **Compared Zeros**: Displays the number of compared zeros during the accumulation period.
- **Compared Ones**: Displays the number of compared ones during the accumulation period.
- **Compared Bits**: Displays the number of compared bits during the accumulation period.
- **Error Ratio**: Displays the ratio of the number of errors to the number of bits.
- **Error Zero Ratio**: Displays the ratio of the number of error zero to the number of bits.
- **Error One Ratio**: Displays the ratio of the number of errors one to the number of bits.
- **Total Words**: Displays the total number of received sequencer words.
- **Frames**: Displays the number of frames received in a time interval.
- **Errored Frames**: Displays the number of errored frames received in a time interval.
- **Frame Error Ratio**: Displays the ratio of the number of frame errors to the number of frames received in the current (or last completed) accumulation period.
- **ConfidenceLevel@TargetErrorRatio**: Displays the percentage of confidence level achieved at specified target error ratio at certain point of time.

- **ErrorRatio@TargetConfidenceLevel**: Displays the number of error ratio achieved at specified confidence level at certain point of time.
- **Results**: Display the measurement result either **Pass** or **Fail**. It is only available when the “Accumulation End” is selected as “Pass/Fail”.

However, when the symbol coded patterns are loaded in **Sequence Editor**, the following results are displayed:

Calculated Results

Location	Show Graphics	Symbol Error Ratio	Received Symbols	Compared Symbols	Errored Symbols	Illegal Symbol Ratio	Illegal Symbols	Filler Symbol Ratio	Filler Symbols	Disparity Error Ratio	Wrong Disparity
M1.DataIn1	On	9.15e-11	2.19e+10	2.19e+10	2.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	4.58e-11	1.00e+00

- **Symbol Error Ratio**: Displays the symbol ratio of the number of errored symbols to the total number of symbols received.
- **Received Symbols**: Displays the total number of Received Symbol Count (all incoming symbols excluding incoming filler symbols) received in a time interval.
- **Compared Symbols**: Displays the number of compared symbols considered for the accumulation period.
- **Errored Symbols**: Displays the number of errored symbols measured during the accumulation period.
- **Illegal Symbol Ratio**: Displays the ratio of the number of Illegal Symbol count to the number of symbols received in the accumulation period.
- **Illegal Symbols**: Displays the total number of Illegal Symbols received in the accumulation period.
- **Filler Symbols Ratio**: Displays the ratio of total no of filler symbols to the number of symbols received during the accumulation period.
- **Filler Symbols**: Displays the total no of filler symbols received during the accumulation period.
- **Disparity Error Ratio**: Displays the ratio of the number of illegal disparity change count to the number of symbols received in the accumulation period.
- **Wrong Disparity**: Displays the total number of wrong disparity received in the accumulation period.
- **Error Ratio**: Displays the ratio of the number of errors to the number of bits.
- **Compared Bits**: Displays the number of compared bits during the accumulation period.

- **Errored Bits**: Displays the number of errored bits during the accumulation period.
- **ConfidenceLevel@TargetErrorRatio**: Displays the percentage of confidence level achieved at specified target error ratio at certain point of time.
- **Results**: Display the measurement result either **Pass** or **Fail**. It is only available when the “Accumulation End” is selected as “Pass/Fail”.
- **Total Words**: Displays the total number of received sequencer words.
- **Frame Error Ratio**: Displays the ratio of the number of frame errors to the number of frames received in the accumulation period.
- **Frames**: Displays the number of frames received in a time interval.
- **Errored** Frames: Displays the number of errored frames received in a time interval.
- **ErrorRatio@TargetConfidenceLevel**: Displays the number of error ratio achieved at specified confidence level at certain point of time.

The following results are displayed when an **Error Ratio** measurement is performed with PAM4 line coding:

Calculated Results

Location	Show Graphics	Symbol Error Ratio	Compared Symbols	Errored Symbols	Error Ratio	Compared Bits	Errored Bits
M2.DataIn		0.00e+00	4.09e+13	0.00e+00	0.00e+00	8.17e+13	0.00e+00

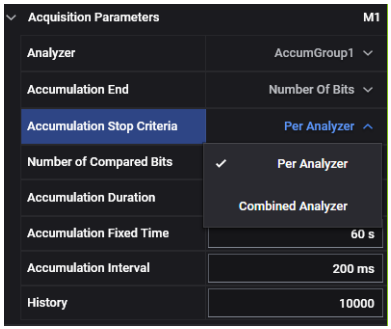
- **Symbol Error Ratio**: Displays the symbol ratio of the number of errored symbols to the total number of symbols received.
- **Errored Symbols**: Displays the number of errored symbols considered for the accumulation period.
- **Compared Symbols**: Displays the number of compared symbols considered for the accumulation period.
- **Error Ratio**: Displays the ratio of the number of errors to the number of bits.
- **Compared Bits**: Displays the number of compared bits during the accumulation period.
- **Errored Bits**: Displays the number of errored bits during the accumulation period.

Error Ratio Measurement for a Group of Analyzers

The error ratio measurement can also be executed on a group of analyzers and combined result will appear in form of Graph, Data Tab and Calculated Results.

To run this, an **Accumulation Stop Criteria** parameter is available under **Acquisition Parameters**. It can be set as "**Per Analyzer**" or "**Combined Analyzer**".

- **Per Analyzer** - Graph, Data Tab and combined Calculated Results will not be visible.
- **Combined Analyzer** - Graph, Data Tab and combined Calculated Results will be visible.



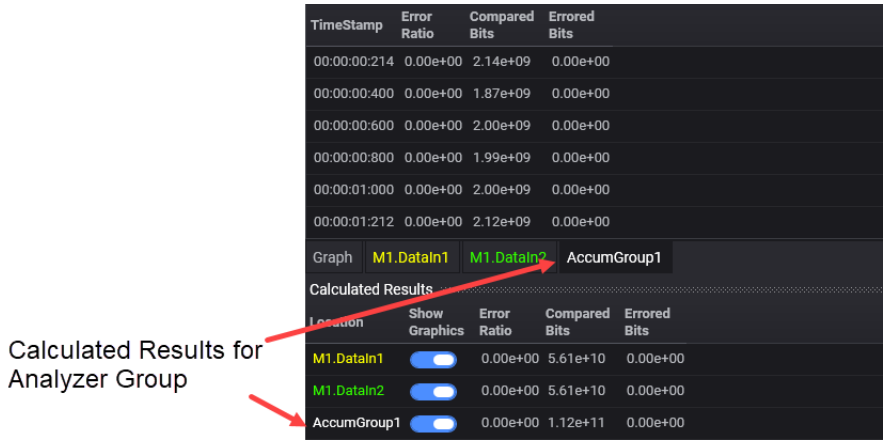
This parameter will be only be available when a group is selected as an analyzer (if the group is having only one location, this will not be available to the user). Also, the availability of this parameter depends on "**Accumulation End**" parameter. If the "**Accumulation End**" is set as "**Full Duration**", it will not be available. However, the results for group of analyzers will be visible in the **Calculated Results**.

Follow the given steps to calculate combined results for an analyzer group:

1. Select the analyzer group.
2. Specify **Accumulation End** as "**Pass/Fail**" or "**Number of Bits**".
3. Specify **Accumulation Stop Criteria** as "**Combined Analyzer**".
4. Specify **Accumulation Duration**, **Fixed Time** and **Interval**.
5. In case the **Accumulation End** is selected as **Pass/Fail**, set **Target Error Ratio** and **Target Confidence Level**.
6. In case the **Accumulation End** is selected as **Number of Bits**, specify **No. of Compared Bits**.

7 Run the measurement.

8 The calculated results for the analyzer group will appear as shown in the following figure:



NOTE The BER measurement processes at least as many bits as defined by the acquisition parameters, it stops when the end criteria is reached or exceeded. Due to update period and hardware granularities, an individual BER measurement will typically process more bits than configured.

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User Guide

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KEYSIGHT TECHNOLOGIES

Overview

The M8070B system software provides the following utilities:

- SCPI Recorder
- Self Test Utility
- Licenses Window
- Preferences Window
- Logger Window
- SCPI Server Information
- Manage Plug-ins
- Manage Instrument Drivers

In addition, the M8070B system software also provides the following utilities. These will be only available on installing the **Advanced Measurement Package** plugin:

- Script Editor
- DUT Control Interface
- SCPI Editor
- Self Test Utility

For details, on the utilities provided by **Advance Measurement Package**, please refer to *M8000 Series Advanced Measurement Package User Guide*.

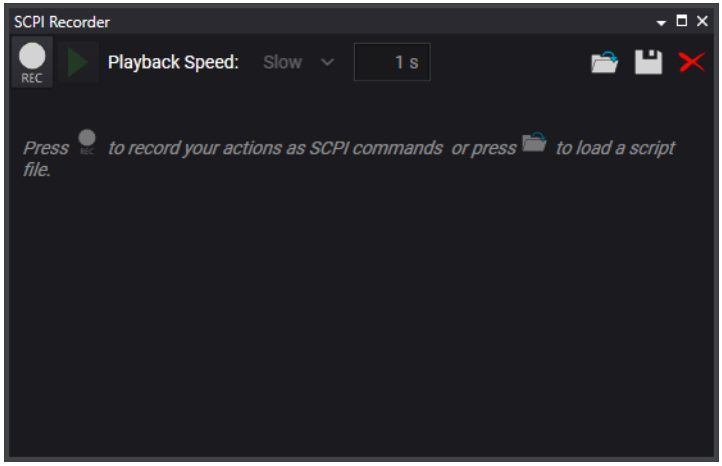
NOTE Please note that the Advanced Measurement Package requires license for its activation. For details on license, see M8070B Plugin Licenses on page 839.

SCPI Recorder

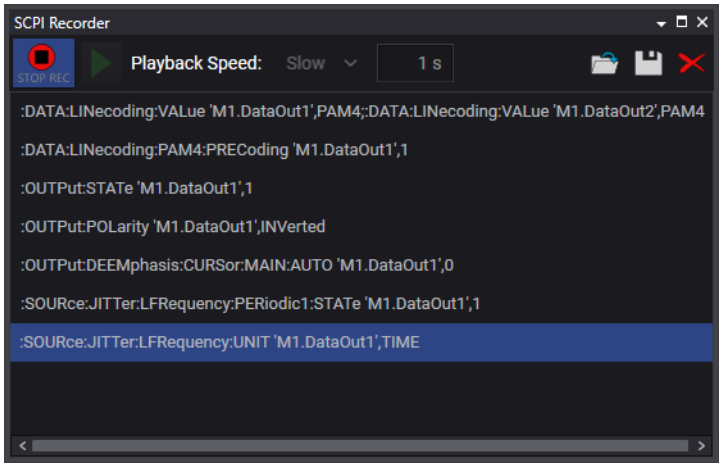
The SCPI recorder is a tool that enables you to quickly discover, record, and learn about the commands needed to perform almost any task remotely. When you've recorded your commands, you can play them back and save them as a macro. Click **REC** button and the recorder performs the following tasks:

- Captures most M8070B setting changes (mouse clicks or keyboard presses).
- Translates the setting into an equivalent SCPI remote-programming command.
- Records the SCPI command within the dialog box.
- Play back the recorded commands.

Click **Menu Bar** > **Utilities** > **SCPI Recorder** to open this dialog box.

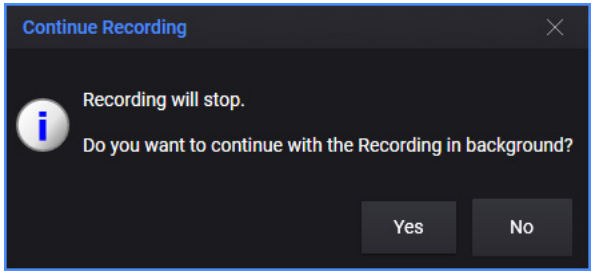


- **Start/Stop Recording** - Click **REC** to begin recording. The button turns red to alert you that any mouse clicks or keyboard presses will be recorded. When you have captured all your commands, click the **STOP REC** button again to end the recording. A **REC** indicator REC will appear on the right side of the menu bar until the recording is going on.



- **Play/Pause Commands** - Click **Play** to play back your recording and observe the commands as they are executed. Playback will only start when you stop the recording the commands. Use **Playback Speed** to control the rate that the commands are played: Slow, Normal, Fast or Custom. In case of Custom, you can set the playback speed from 0 to 120 seconds. During playback, click **PAUSE** to temporarily stop the playback. You can also right-click and then click **Execute** to run a single command from the list of recorded commands.
- **Copy/Paste Recorded Commands** - You can use Windows clipboard to copy your recorded commands. Click on a command to select it. Shift click to select a range of commands. Ctrl click to select non-adjacent commands. Ctrl-A selects all commands. Ctrl-C copies all selected commands. In another application, use Ctrl-V to paste the commands. You can also right-click and then click **Copy**. By copying commands you can create you own sequence of commands and execute them later.
- **Save/Load Recorded Commands** - Click **Save Script File** to save the recorder commands into a script file (.TXT). This file can be reloaded into the dialog box at any time by clicking **Load Script File**. The SCPI script files are ASCII files, so you can edit them as well as create new script files using a text editor.
- **Delete Recorded Commands** - Click **Delete All** to delete all recorded commands from the dialog box. To delete a single command, select the command and press "**Delete"** on your keyboard. Alternatively, you can right-click and then click **Delete**.

- **Run SCPI Recorder in Background** – You can continue the SCPI recording in the background while you perform the other GUI functions. To do so, click on the **SCPI Recorder options** > **Close**. You will see the following message:



- Click “Yes” to continue recording in the background. The **SCPI Recorder** dialog will minimize. You can recall this dialog either on pressing the REC button or clicking on **Utilities** > **SCPI Recorder**.

  On closing the **SCPI Recorder** dialog, all the captured commands will appear in the dialog unless the M8070B software instance is closed.

Self Test Utility

The **Self Test** utility checks the specific system information of the hardware components for basic functionality. On execution, the following results are displayed:

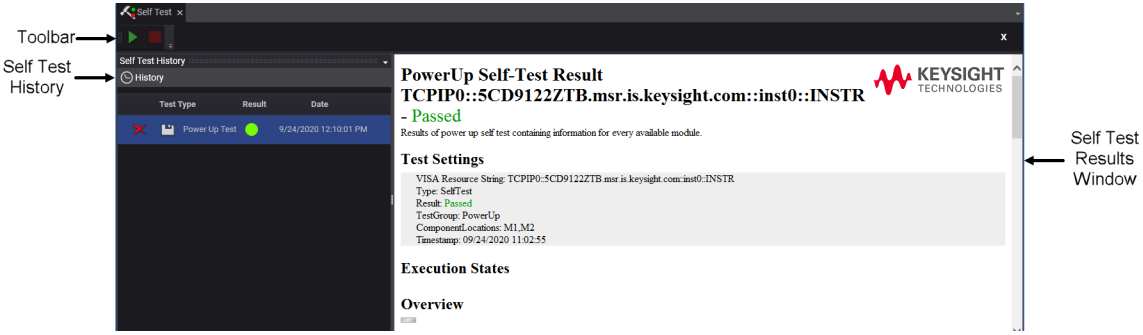
- System related information such as connected modules, serial no. and hardware revision.
- Module related information such as calibration, power supplies and memory controller.

Launching the Self Test Utility

To launch the **Self Test**:

- Go to the **Menu Bar** > **Utilities** and then select **Self Test**.

The **Self Test** utility will appear as shown in the following figure:



The **Self Test** utility consists of the following GUI elements:

- Toolbar
- Self Test History
- Self Test Results Window

Toolbar

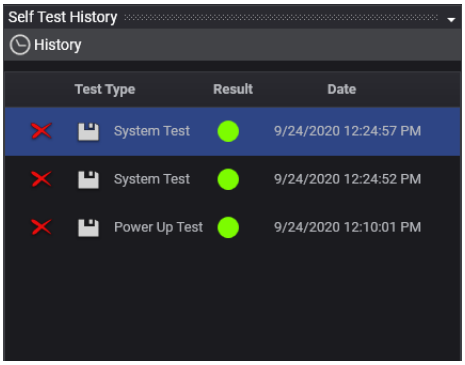
The toolbar provides the following convenient self test functions:

Table 74

Icon	Name	Description
	Execute Self Test	Click this icon to run the self test.
	Abort Self Test	Click this icon abort a self test.
	Save Self Test	Click this icon to save the selected self test from the history. For details, refer to Saving Self Test Results on page 797.
	Delete Self Test	Click this icon to delete the selected self test from the history.
	Close Report	Click this icon to close the self test result.

Self Test History

The **Self Test History** maintains the history of self tests (Passed or Failed) executed by the user. The passed self test results are indicated by green LED while the failed ones are indicated by red LED.



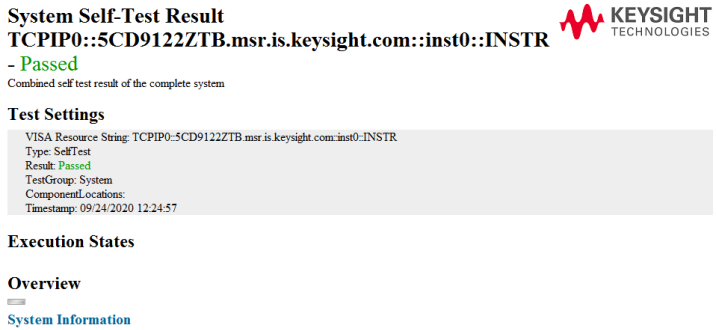
At any point of time, you can double-click on the shown self test entries to view their respective results. Once viewed, you can click on **Close Report** icon to close the self test results.

The **Self Test History** also allows you to save and delete the self test reports. For details, refer to Saving Self Test Results on page 797 and Deleting Self Test Results on page 798.

Self Test Results Window

The **Self Test Results** window displays the results of the executed self test. It display the following results:

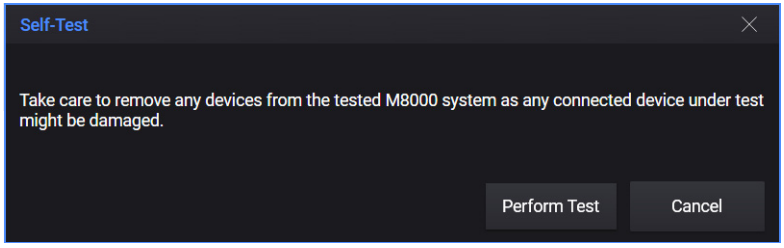
- System related information such as connected modules, serial no. and hardware revision.
- Module related information such as calibration, power supplies and memory controller.



Executing Self Test

To execute a self test:

- Terminate each **Data Out** port with 50 Ω.
- Remove any devices from the tested M8000 system as any connected device under test might be damaged.
- Click the **Execute Self Test** icon. The following message will appear:



- Click on **Perform Test** button present on the message box.
- The self test will start and the status will be indicated by the status indicator that appears on the right side of the toolbar. Once the self test is completed, the results will be shown on the **Self Test Results** window.

CAUTION Before performing a system self-test, terminate each **Data Out** port with 50 Ω. Take care to remove any devices from the tested M8000 system as any connected device under test might be damaged.

Aborting Self Test

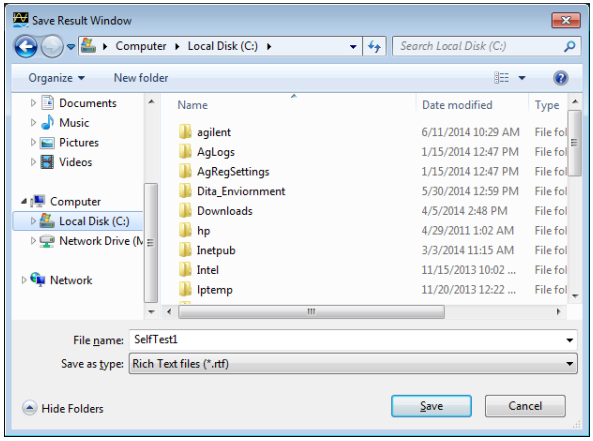
To abort a self test:

- Click **Abort Self Test** icon to abort the self test. The self test will stop and the self test failure entry will be displayed in the **Self Test History**.

Saving Self Test Results

To save the self test results from the **Self Test History**:

- Click the **Save Report** icon. A standard **Save Result** dialog will appear.



- Use the navigation pane to provide a location to save the file.
- Provide a file name and specify the file format. You can save the file in RTF, HTML, XML and TXT formats.
- Click **Save**.

Deleting Self Test Results

To delete a self test entry from the **Self Test History**:

- Click **Delete Report** icon. The entry will be removed from the **Self Test History**.

Licenses Window

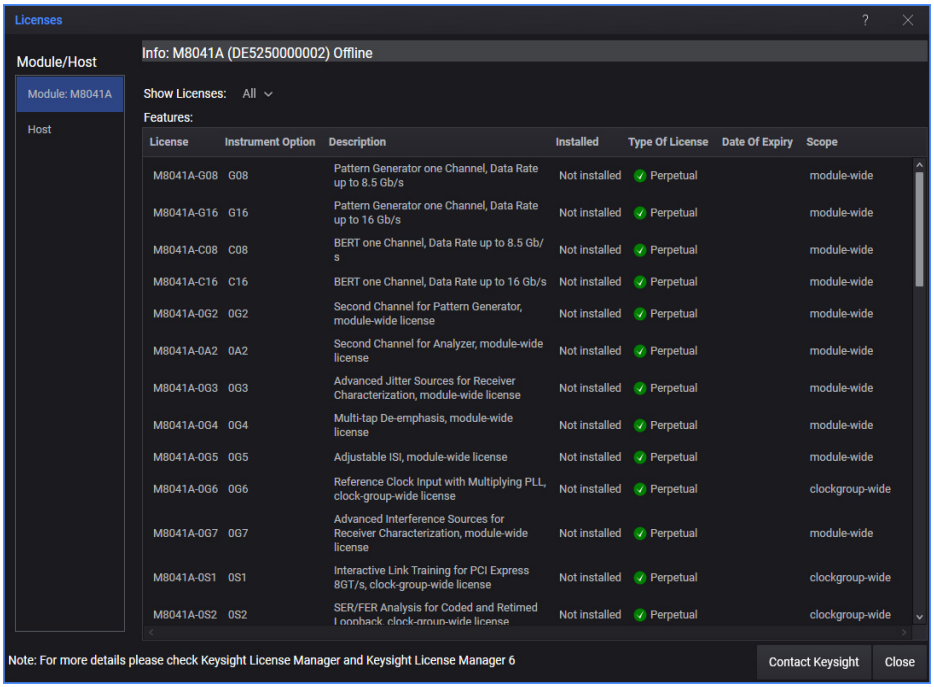
The **Licenses** window displays the license information currently installed in the modules or host.

Launching the Licenses Window

To launch the **Licenses** window:

1 Go to the **Menu Bar** > **Utilities** and then select **Licenses...**.

The **Licenses** window is shown in the following figure:



License	Instrument Option	Description	Installed	Type Of License	Date Of Expiry	Scope
M8041A-G08	G08	Pattern Generator one Channel, Data Rate up to 8.5 Gb/s	Not installed	Perpetual		module-wide
M8041A-G16	G16	Pattern Generator one Channel, Data Rate up to 16 Gb/s	Not installed	Perpetual		module-wide
M8041A-C08	C08	BERT one Channel, Data Rate up to 8.5 Gb/s	Not installed	Perpetual		module-wide
M8041A-C16	C16	BERT one Channel, Data Rate up to 16 Gb/s	Not installed	Perpetual		module-wide
M8041A-0G2	0G2	Second Channel for Pattern Generator, module-wide license	Not installed	Perpetual		module-wide
M8041A-0A2	0A2	Second Channel for Analyzer, module-wide license	Not installed	Perpetual		module-wide
M8041A-0G3	0G3	Advanced Jitter Sources for Receiver Characterization, module-wide license	Not installed	Perpetual		module-wide
M8041A-0G4	0G4	Multi-tap De-emphasis, module-wide license	Not installed	Perpetual		module-wide
M8041A-0G5	0G5	Adjustable ISI, module-wide license	Not installed	Perpetual		module-wide
M8041A-0G6	0G6	Reference Clock Input with Multiplying PLL, clock-group-wide license	Not installed	Perpetual		clockgroup-wide
M8041A-0G7	0G7	Advanced Interference Sources for Receiver Characterization, module-wide license	Not installed	Perpetual		module-wide
M8041A-0S1	0S1	Interactive Link Training for PCI Express 8GT/s, clock-group-wide license	Not installed	Perpetual		clockgroup-wide
M8041A-0S2	0S2	SER/FER Analysis for Coded and Retimed Loopback, clock-group-wide license	Not installed	Perpetual		clockgroup-wide

2 Select an option from the **Show Licenses** drop-down list.

The following options are available:

- **All**: Displays a list of all the licenses. By default, this option is selected.
- **Installed**: Displays a list of installed licenses only.

The **Licenses** window is divided into two panels. The left panel shows the modules/host information. Once you select modules/host, the corresponding license information is shown in the right panel.

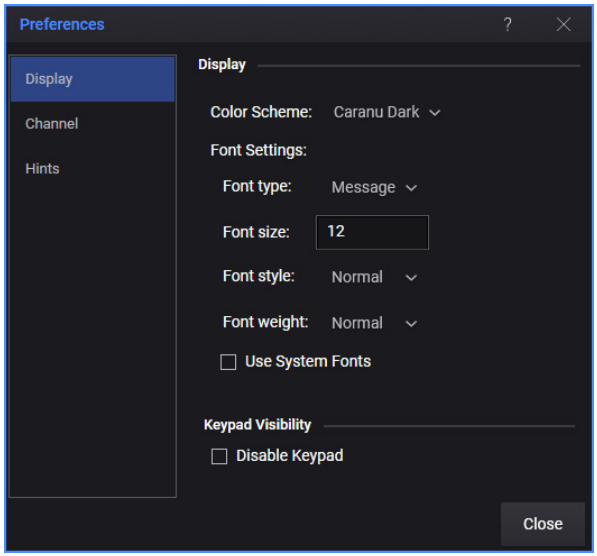
To exit the **Licenses** window, click the **Close** button.

For detailed information on the M8020A licenses, refer to Licenses on page 823.

Preferences Window

The **Preferences** window allows you to set the display and channel settings in the GUI. In addition, you can use this dialog to enable/disable **Parameter** hint dialog on the GUI startup.

To open the **Preferences** window, go to **Menu Bar** > **Utilities** and then select **Preferences...**. The **Preferences** window will appear as shown in the following figure:



The **Preferences** window has the following tabs:

- Display tab
- Channel tab
- Hints tab

Display Tab

The **Display** tab provides the following options:

- **Display** - The **Display** option provides the following choices:
  - **Color Scheme** - Use this option to change the color scheme of the GUI. You can choose between the dark or light scheme. The dark scheme is selected by default.
  - **Font Setting** - Use this option to change the font settings in the GUI.
  - **Use System Fonts** - Select this option to use the system fonts in the GUI.

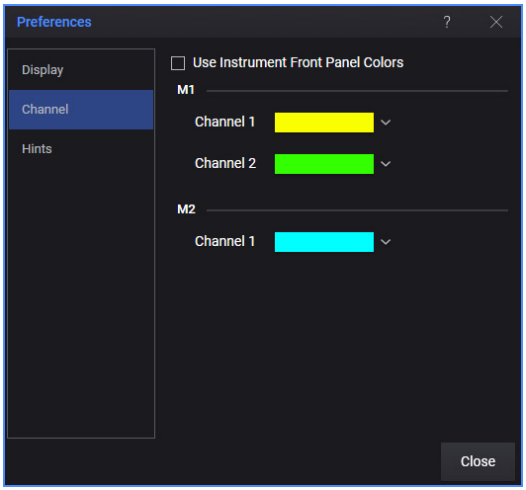
Keypad Visibility

- **Disable Keypad** - Use this option to disable the on-screen numeric keypad in the GUI. The on-screen numeric keypad is enabled by default.

Channel Tab

- The **Channel** tab displays the color schemes applied to the various channels of the connected modules. In addition, this tab also allows you to assign your own color schemes to each individual channel of the connected modules.

  The following figure depicts how the different color schemes are applied to the various channels of the connected modules.

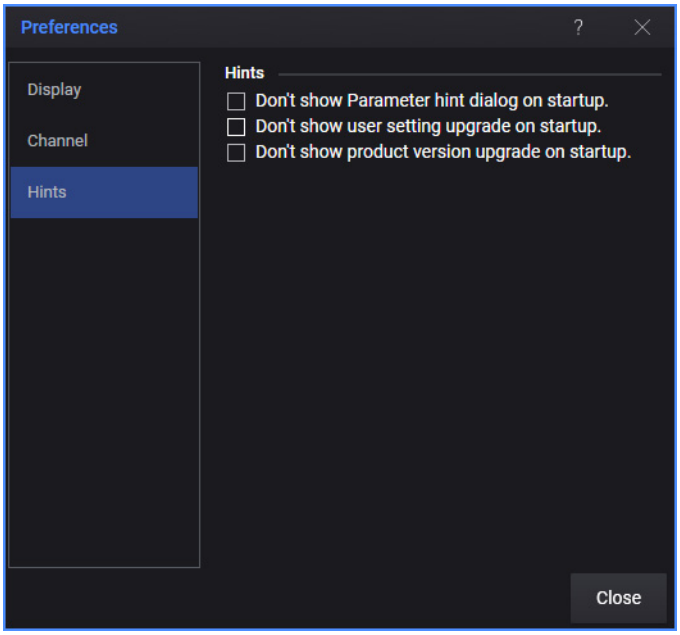


You can also select **Use Instrument Front Panel Colors** option to assign the color which is available on the front panel of the instrument to each individual channel.

NOTE The color schemes assigned to the channels will change if you switch to light color scheme from the **Display Setting** tab.

Hints Tab

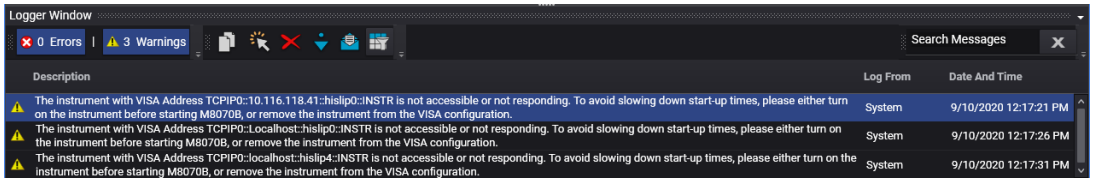
The **Hints** tab allows you to show/hide the **Parameter** hint dialog which appears in the **Setup View** on the GUI startup. For details, see Setup View on page 240. Select/unselected the corresponding check-box to show/hide the **Parameter** hint dialog.



Logger Window

The **Logger** window displays errors, warnings and information messages along with their respective descriptions, applications from where they are generated and their time stamps.

The **Logger** window always appears whenever you launch the M8070B user interface. However, you can open/close this window by clicking on the **Logger** button, present on the status bar.

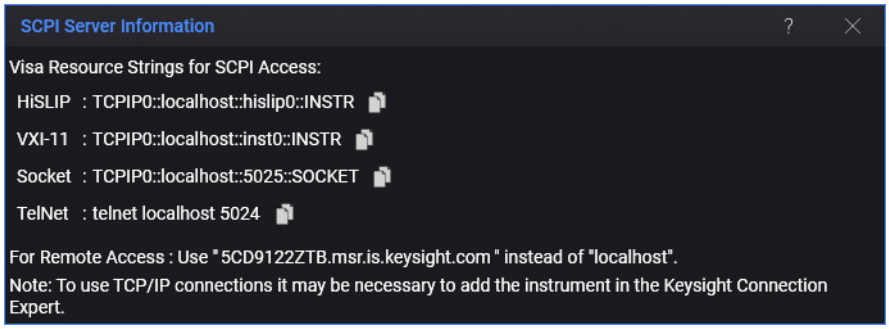


The **Logger** window allows you to:

- **Message Selection** - Use this option to choose whether you want to view errors, warnings or information message.
- **Copy** - Use this option to copy a message. You need to select a message in order to enable copy feature.
- **Select All** - Use this option to select all messages. It also enables copying all messages.
- **Clear Messages** - Use this option to delete all messages.
- **Auto Scroll** - Use this option to enable/disable auto scroll option. When the **Auto Scroll** option is enabled, it will automatically scroll you to the new message without using the scroll bar.
- **Open On Message** - Turn this button OFF if you don't want the Logger window to automatically pop-up whenever a message is received.
- **Column Option** - Use this button to filter the messages either from **Log From** column or **Date and Time** column.
- **Search Messages** - Use this option to search messages by providing an input in the **Search Messages** search box.

SCPI Server Information

This dialog lists the VISA resource and remote access strings to connect instruments.



Manage Plug-ins

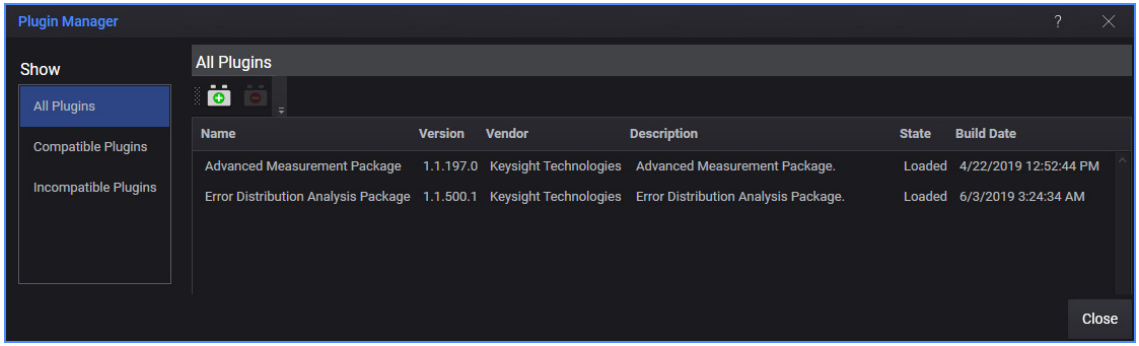
A plug-in is a piece of software application that acts as an add-on to the main software and enhances its capability. Plug-in allows the software to host additional functionality without undergoing a major modification or enhancement. A plug-in is not a permanent part of the software, hence can be installed, uninstalled and updated as and when required.

The M8070B system software for the M8000 Series of BER Test Solutions supports plug-ins. Thus, the present capabilities of M8070B can be further enhanced by simply adding the required plug-ins.

The **Plug-in Manager** simplifies all the tasks related to plug-in management. It displays list of plug-ins that are installed in the software. For each plug-in, it displays the information such as Name, Version, Vendor, Description, State and Build Date. In addition, the **Plug-in Manager** also allows you to install, uninstall and update the plug-ins.

How to Launch Plug-in Manager

To launch **Plug-in Manager**, open the M8070B user interface and then go to **Menu** > **Utilities** and then **Manage Plug-ins...**. The **Plug-in Manager** window will appear as shown in the following figure:



The **Plug-in Manager** window displays two types of plug-ins:

- **Compatible Plug-ins** – plug-ins which are compatible with the current version of software.
- **In-Compatible Plug-ins** – plug-ins which are not compatible with the current version of software.

The **Plug-in Manager** window displays the following information of each plug-in:

- **Name** - Name of the plug-in
- **Verison** - Version no. of the plug-in
- **Vendor** - Vendor/publisher of the plug-in
- **Description** - Brief description of the plug-in
- **State** - State of the plug-in. For details on different plug-in states, see Plug-in States on page 806.
- **Build Date** - Build date of the plug-in

Plug-in States

There can be the following plug-in states:

- **Installed** - When the plug-in is installed but the M8070B software is not re-started. In this case, the installed plug-in is not loaded or it cannot be used. You have re-start the M8070B software in order to load the plug-in.
- **Loaded** - When the plug-in is installed and the M8070B software has been re-started. In this case, the installed plug-in is ready to be used. Remember, you have to restart the M8070B software in order to load the plug-in.
- **Not Loaded** - When the plug-in is installed and but failed to load. In this case, the installed plug-in cannot be used.
- **Version In-Compatible** - When the version of the installed plug-in is not compatible with the current version of M8070B software.
- **Marked to be Installed** - When the plug-in is installed but the M8070B software is not restarted. In this case, the installed plug-in is not loaded, or it cannot be used. You must restart the M8070B software to load the plug-in.
- **Marked to be Upgraded** - When the plug-in is updated but the M8070B software is not restarted. In this case, the updated plug-in is not yet loaded, and it cannot be used. You must restart the M8070B software to load the updated plug-in.
- **Marked to be Uninstalled** - When the plug-in is uninstalled but the M8070B software is not restarted. In this case, the uninstalled plug-in is still shown, you must restart the M8070B software to no longer see the uninstalled plug-in.

How to Install a Plug-in

The **Plug-in Manager** window allows you to install a plug-in.

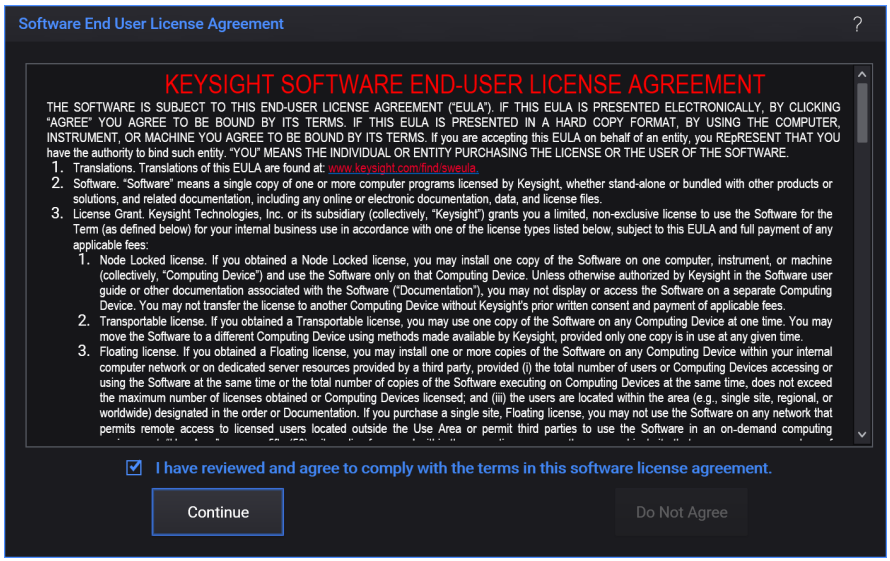
To do so;

1 Download plug-in file from Keysight webpage: www.keysight.com/find/m8000

2 Click **Install Plug-in from File** button. A Windows standard **Open** dialog will appear.

3 Locate the plug-in file (*.M8KP) you want to install and click **OK**.

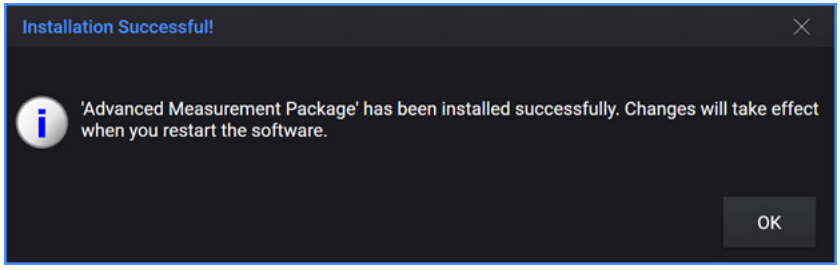
A **Keysight End User License Agreement** window will appear.



4 Select the check-box to accept the Keysight software license agreement and click **Continue** to proceed with plugin installation.

NOTE To proceed with the installation of this software, you must agree to comply with the terms in the software license agreement. Failure to agree the license agreement will prevent the installation process from continuing.

5 On the successful installation of plug-in, the following message will appear:



6 Restart the software. Once you restart the software, the plug-in state will change to **Loaded**. See Plug-in States on page 806.

NOTE Ensure to restart the M8070B software for the changes to take effect.

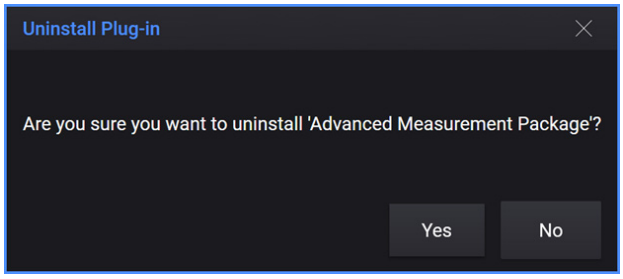
How to Uninstall a Plug-in

The **Plug-in Manager** window allows you to uninstall a plug-in.

To do so;

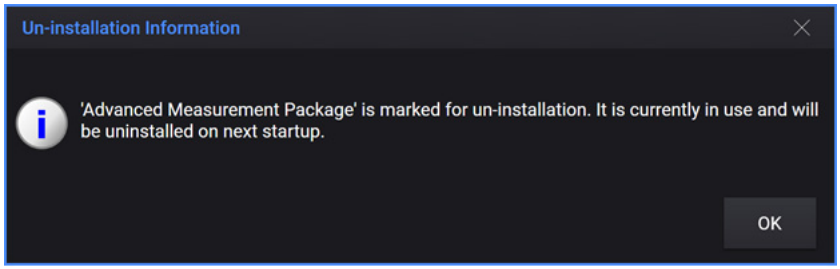
1 Select the plug-in from the list.

2 Click **Uninstall Selected Plug-in** button or right-click on the selected plug-in. The **Uninstall Plug-in** dialog will open.



3 Click **Yes**. If the state of plug-in is **Installed**, then it will be immediately uninstalled from the software.

4 However, if the plug-in is currently in use (**Loaded** or **Not Loaded**), then you will receive the following message.



5 Restart the software. The plug-in will be uninstalled on software startup.

How to Update a Plug-in

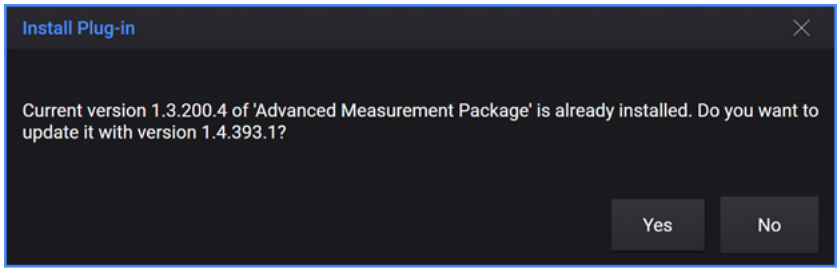
The **Plug-in Manager** window also allows you to update an already installed plug-in.

Following the given steps to update the plug-in with its higher version:

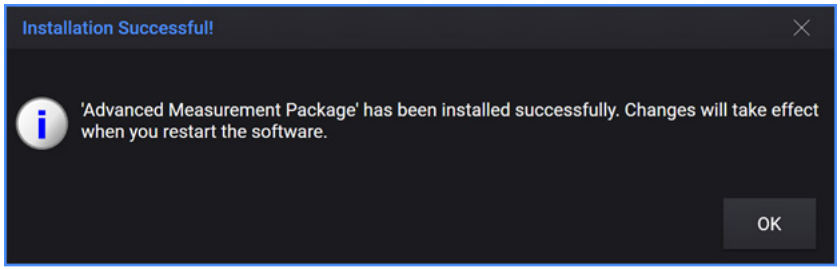
1 Download plug-in file from Keysight webpage: www.keysight.com/find/m8000

2 Click **Install Plug-in from File** button. A Windows standard **Open** dialog will appear.

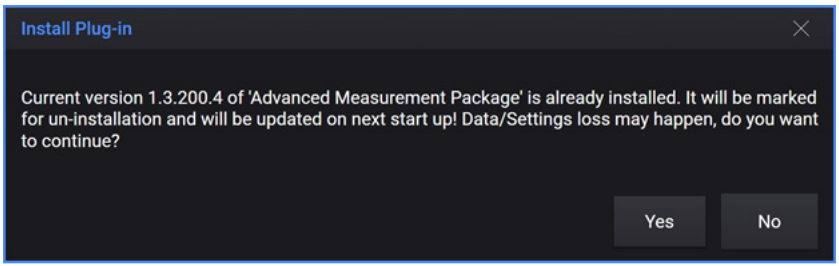
3 Locate the plug-in file (*.M8KP) you want to update and click **OK**. You will see the following message:



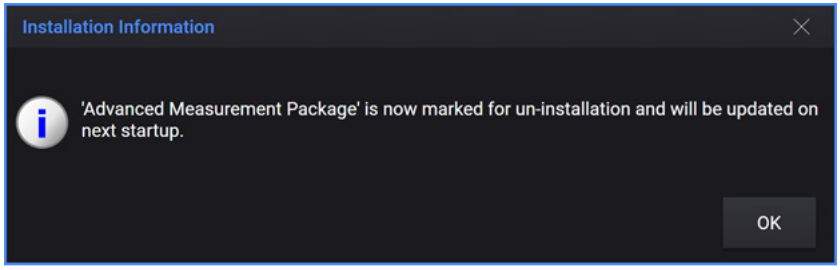
4 Click **Yes**. If the state of plug-in is **Installed**, then it will be immediately updated and the following message will appear:



5 However, if the plug-in is currently in use (**Loaded** or **Not Loaded**), then you will receive the following message.



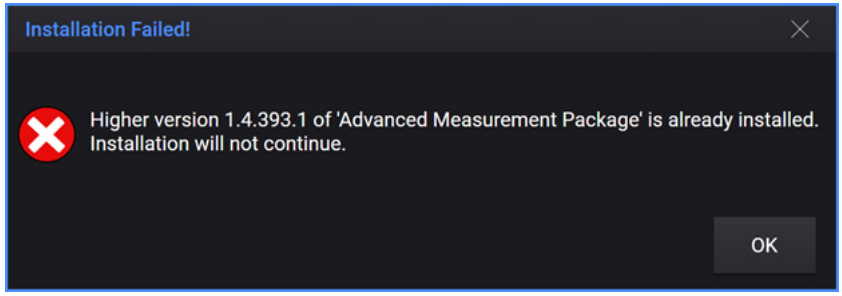
6 Click **Yes**. The following message will appear:



7 Click **OK**. The selected plug-in will be uninstalled from the software. You can now install the new version of that plug-in. For installation procedure, see How to Install a Plug-in on page 807.

NOTE Ensure to restart the M8070B software for the changes to take effect.

The **Plug-in Manager** window does not directly allow you to update an installed plug-in with previous (lower) version. If you try to do so it will give the following error message:



In this case, you have to uninstalled the plug-in and then install the previous (lower) version of that plug-in again.

How to Access an Installed Plug-in Through M8070B User Interface

Follow the steps to access an installed plug-in through M8070B user interface:

1 Launch M8070B software user interface.
2 In the M8070B user interface, go to **Menu Bar** and then click **Application** menu. It will list all installed plug-ins.
3 Select the plug-in.
4 The plug-in user interface will appear in the M8070B software.

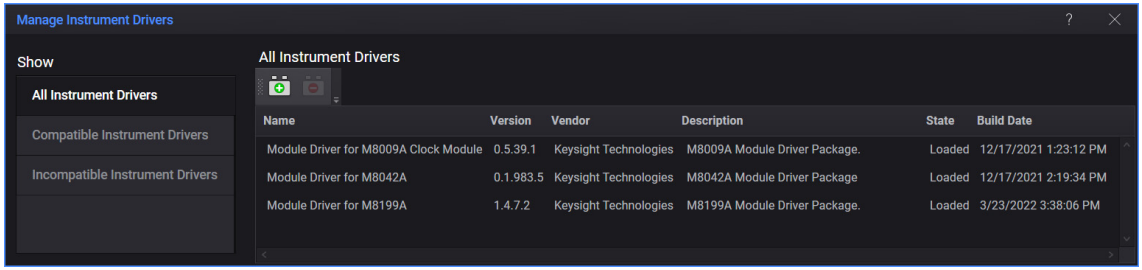
For complete details on how to operate plug-in user interface, refer to the respective plug-in's *User Guide*

Manage Instrument Drivers

The **Manage Instrument Drivers** utility simplifies all the tasks related to instrument driver management. It displays a list of instrument drivers that are installed in the M8070B software. For each instrument driver, it displays information such as Name, Version, Vendor, Description, State, and Build Date. In addition, the **Manage Instrument Drivers** also allows you to install, uninstall, and upgrade the instrument drivers.

How to launch Manage Instrument Drivers window

To launch the **Manage Instrument Drivers** window, open the M8070B user interface and then go to the menu bar. Select **Utilities** and then click **Manage Instrument Drivers...**. The **Manage Instrument Drivers** window appears as shown in the following figure:



The **Manage Instrument Drivers** window displays the following types of instrument drivers:

- **All Instrument Drivers** – shows the list of all compatible and incompatible instrument drivers.
- **Compatible Instrument Drivers** – shows only the instrument drivers which are compatible with the current version of M8070B software.
- **Incompatible Instrument Drivers** – shows only the instrument drivers which are not compatible with the current version of M8070B software.

The **Manage Instrument Drivers** window displays the following information about each instrument driver:

- **Name** - Name of the instrument driver.
- **Version** - Version number of the instrument driver.
- **Vendor** - Vendor/publisher of the instrument driver.
- **Description** - Brief description of the instrument driver.
- **State** - State of the instrument driver. For details on different instrument driver states, see Instrument Driver States on page 814.
- **Build Date** - Build date of the instrument driver.

Instrument Driver States

There can be the following instrument driver states:

- **Installed** - When the instrument driver is installed but the M8070B software is not restarted. In this case, the installed instrument driver is not loaded, or it cannot be used. You must restart the M8070B software to load the instrument driver.
- **Loaded** - When the instrument driver is installed and the M8070B software has been restarted. In this case, the installed instrument driver is ready to be used.

  Remember, you have to restart the M8070B software to load the instrument driver.
- **Not Loaded** - When the instrument driver is installed but failed to load. In this case, the installed instrument driver cannot be used.
- **Version Incompatible** - When the version of the installed instrument driver is not compatible with the current version of M8070B software.
- **Marked to be Installed** - When the instrument driver is installed but the M8070B software is not restarted. In this case, the installed instrument driver is not loaded, or it cannot be used. You must restart the M8070B software to load the instrument driver.
- **Marked to be Upgraded** - When the instrument driver is updated but the M8070B software is not restarted. In this case, the updated instrument driver is not yet loaded, and it cannot be used. You must restart the M8070B software to load the updated instrument driver.
- **Marked to be Uninstalled** - When the instrument driver is uninstalled but the M8070B software is not restarted. In this case, the uninstalled instrument driver is still shown, you must restart the M8070B software to no longer see the uninstalled instrument driver.

Installing Instrument Drivers in the M8070B System Software

The M8070B system software supports instrument drivers. To use these drivers, it is necessary to install the instrument drivers in the M8070B software. The M8070B software comes with a **Manage Instrument Drivers** utility to simplify all the tasks related to instrument driver management.

This section describes how to use the **Manage Instrument Drivers** utility to install, uninstall, and update the instrument drivers in the M8070B system software.

Prerequisites for Instrument Driver Installation

- The latest version of M8070B software which is available either on CD or can be downloaded from Keysight web page.
- Instrument driver file which can be downloaded from Keysight web page.

NOTE

It is not necessary to run the M8070B software with administrator privileges to install, uninstall or upgrade the M8xxxA instrument drivers.

During an installation the USB and PCI-Express drivers get also installed. For this part the Manage Instrument Drivers window opens a dialog box to request administrator privileges to this part. Please press “Continue” to give administrative privileges on a PC running Windows 11 or Windows 10 IoT Enterprise.

Not doing so may result in the installation failure. Please contact your system administrator to provide you the administrative rights.

Locate Documentation

After installing the M8070B software, you will find the required documentation from the Start menu. Select **Keysight M8070B > Keysight M8070B Documentation**.

For module related documents, navigate to:

```
C:\Program Files\Keysight\M8070B\Modules\
%ModuleDriverName%\doc
```

where <ModuleDriverName> is the name of the folder corresponding to the module driver of interest.

You can also visit www.keysight.com/find/m8000 to find the latest versions of related manuals.

Installing/Updating PCI-Express and USB Driver

During a module driver installation or update the related PCI-Express and USB driver will also be installed or updated. For doing this a dialog will request administration privileges.

In some circumstances for a PCI-Express installation it is not enough to restart the M8070B software but to reboot the complete system. You will get a message when the installation or upgrade has completed whether to restart the software only or to reboot the system.

To reboot the system means to stop and restart the chassis and the controller or PC in a defined order one time.

System Reboot Process

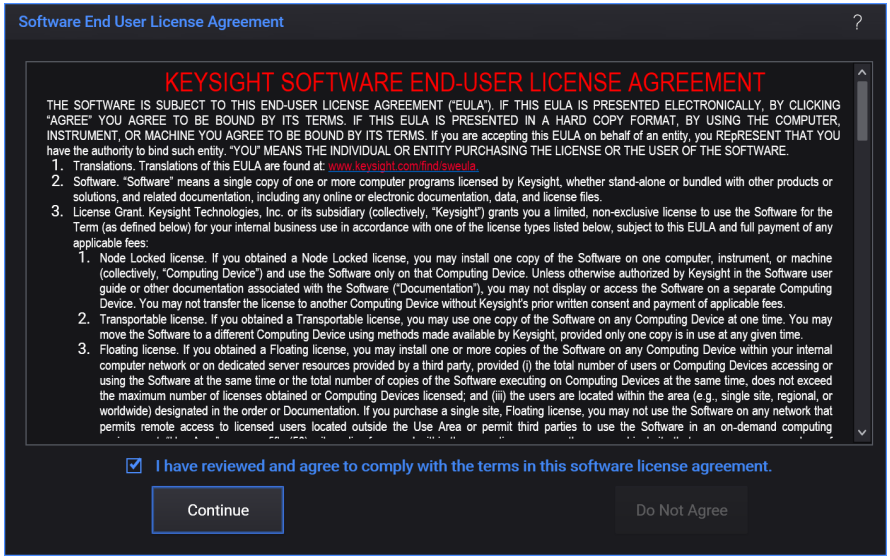
1 Turn off the PC
2 Turn off the AXIe chassis
3 Turn on the AXIe chassis
4 Wait until LEDs on modules present in AXIe chassis (with PCI-Express connection) are turned Green.
5 Turn on the PC

How to Install a Instrument Driver

The **Manage Instrument Drivers** window enables you to install a instrument driver. To do so, perform the following steps:

1 Download the required instrument driver file from the Keysight web page.
2 Click **Install module driver from file** icon. A standard Windows **Open** dialog appears.
3 Locate the instrument driver file (*.M8KM) which you want to install and click **Open**.

A **Software End User License Agreement** window will appear.

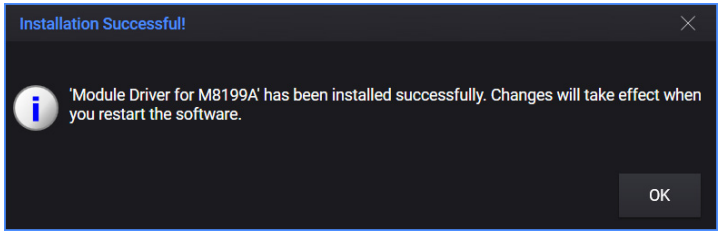


4 Select the check-box to accept the Keysight software license agreement and click **Continue** to proceed with instrument driver installation.

NOTE

To proceed with the installation of this software, you must agree to comply with the terms in the software license agreement. Failure to agree the license agreement will prevent the installation process from continuing.

On the successful installation of the instrument driver, a message similar to the following appears:



5 Restart the software. Once you restart the software, the instrument driver state will change to **Loaded**. See Instrument Driver States on page 814.

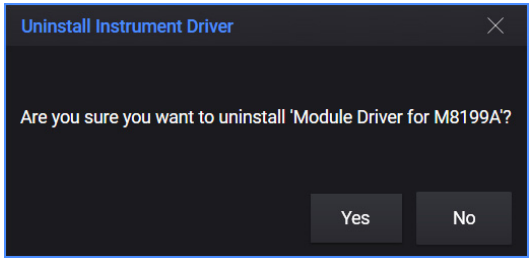
NOTE Ensure to restart the M8070B software for the changes to take effect.

How to Uninstall a Instrument Driver

The **Manage Instrument Drivers** window enables you to uninstall a instrument driver. To do so, perform the following steps:

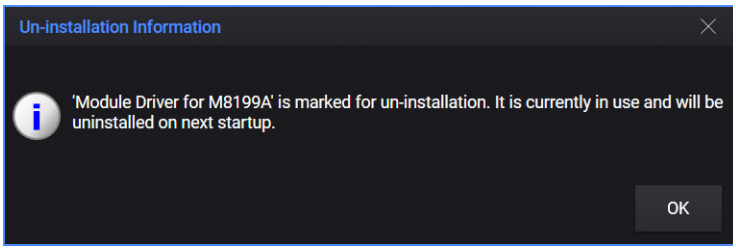
1 Select the instrument driver from the list.

2 Click **Uninstall selected module driver** icon or right-click on the selected instrument driver and select **Uninstall Plugin**. The **Uninstall Instrument Driver** dialog appears.



3 Click **Yes**. If the state of the instrument driver is Installed, then it will be immediately uninstalled from the software.

4 However, if the instrument driver is currently in use (**Loaded** or **Not Loaded**), then you will receive the following message.



5 Restart the M8070B software. The instrument driver will be uninstalled on a software startup.

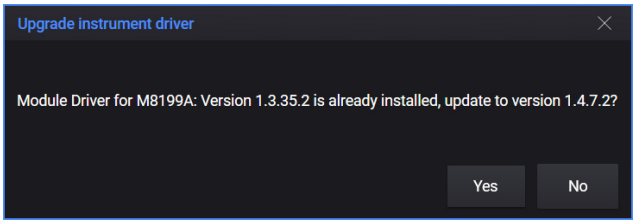
How to Update a Instrument Driver

The **Manage Instrument Drivers** window also enables you to update an already installed instrument driver. Perform the following steps to update the instrument driver with its higher version:

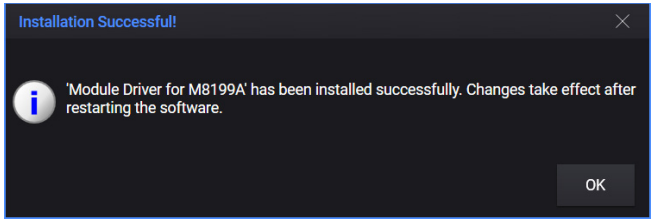
1 Download the latest instrument driver file from Keysight web page.

2 Click **Install module driver from file** icon. A standard Windows **Open** dialog appears.

3 Locate the instrument driver file (*.M8KM) you want to update and click **Open**. You will see the following message:



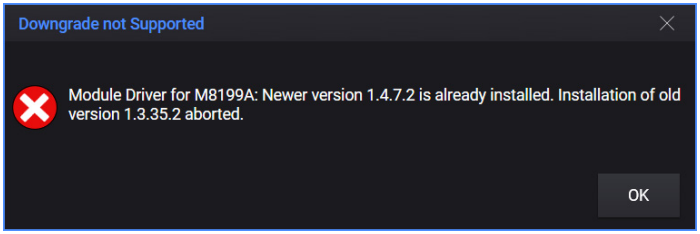
4 Click **Yes**. If the state of instrument driver is **Installed**, then it will be immediately updated, and the following message will appear:



5 Click **OK**. The selected instrument driver will be uninstalled from the software. You can now install the new version of that instrument driver. For the installation procedure, see How to Install a Instrument Driver on page 816.

NOTE Ensure to restart the M8070B software for the changes to take effect.

The **Manage Instrument Drivers** window does not directly allow you to update an installed instrument driver with the previous (lower) version. If you try to do so it will give the following error message:



In this case, you must uninstall the instrument driver and then install the previous (lower) version of that instrument driver again.

How to Access an Installed Instrument Driver through M8070B User Interface

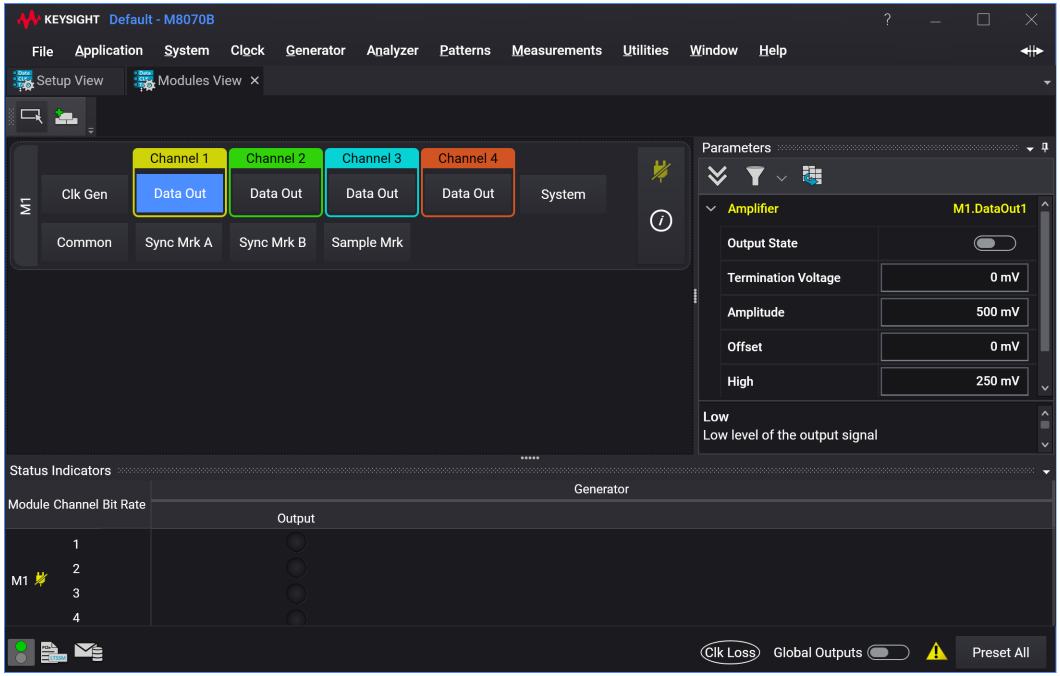
Perform the following steps to access an installed instrument driver through the M8070B user interface:

1 Click **Start** menu and go to **All Programs > Keysight M8070B** and click **Keysight M8070B**.

2 Select the instrument driver from **M8070B Startup Options** dialog box.

3 Click **OK**.

The instrument driver user interface appears in the M8070B software.



M8000 Series of BER Test Solutions
User Guide

10 Licenses

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KEYSIGHT TECHNOLOGIES

Overview

The basic functionality of the M8070B can be used without installing any license. However, for advanced operations, you need to install the M8070B plugins. For details on these plugins, see M8070B Supported Plugins on page 94.

In addition, the M8020A, M8040A and M8050A, being a modular product, includes different sets of modules hosted in an M9505A or M9514A AXI chassis, respectively. Each module has its own licenses corresponding to specific features. Therefore, you need to install these licenses in your instrument in order to use these modules/features.

The licenses for the plugins and modules can be installed using the **Keysight License Utilities**. See Keysight Licensing Utilities on page 842.

License Types

The Keysight Licensing provides four types of licenses:

- **Node-locked** - A node-locked license permits the licensed software to run on only one machine. Each node-locked license is locked to an instrument or computer. Trial licenses are node-locked, subscription licenses. Trial licenses are issued for a particular instrument or computer and are provided free of charge for you to try out a Keysight product.

  A trial license can be of the following two types:

  - **30 days free trial license** - The 30 days free trial license for the M8000 Series of BER Test Solutions can be downloaded using the following weblink: http://www.keysight.com/main/editorial.jspx?cc=IN&lc=eng&ckey=2624767&nid=-32914.1100508&id=2624767
  - **9 months DST license** - The DST license can only be ordered by rental companies and distributors.
- **USB portable** - A USB portable license is locked to a USB dongle (also called a USB key). Systems that run the licensed feature or product must have the license file resident on their hard disks, and have the dongle attached when they run the licensed feature or product.

Node-locked and USB portable licenses may be counted or uncounted. Counted licenses enable a specified number of a given capability. An uncounted license simply unlocks the licensed feature or application on the system where it is installed.

- **Transportable** - A transportable license is a type of node-locked license that can be unlocked from one client host and then locked to another client host, via a network-enabled process performed in conjunction with the Keysight Software Manager website.
- **Floating** - Floating licenses (network licenses) reside on a license server (a separate computer) that can be used on another computer or instrument. Floating licenses can be borrowed for a specified number of days. Once you have borrowed a license, you can disconnect the licensed instrument or computer from the license server and continue to use the license offline for the duration of the borrow period. Some older floating licenses do not support borrowing.

  Generally, floating licenses are intended to be used only for the duration of actual use of an application. In typical cases this is handled automatically, a floating license is checked-out (from the license server) when a user starts the application, and the license is returned to

the license server when the application is closed. If the check-out fails (all available licenses have already been checked-out), the application cannot be used.

Each license is either perpetual (permanent) or subscription (good for a limited amount of time).

These licenses can be installed using the Keysight License Manager. It helps you install licenses on your local machine (instrument or computer), or configure your local machine to use licenses from a remote license server. For details, see Keysight Licensing Utilities on page 842.

Module-Specific Licenses

Module-specific licenses are a specialized type of license that enables a specific module of a modular instrument (such as a PXI or AXIe module). The module-specific license resides on the controller and is bound to both the controller (typically a PC) and the module; the controller by means of the HostID, and the module itself by means of the module serial number which is embedded in the feature name for the license. Module-specific licenses may be time-perishable.

M8020A Licenses

The licenses used by the various modules of M8020A are listed in the following tables:

M8041A - High-Performance BERT Module

M8041A - Basic Selection

Table 75 M8041A - Basic Selection

Product	Option	Description
M8041A-G08	G08	Generator one Channel, Data Rate up to 8.5 Gb/s
M8041A-G16	G16	Generator one Channel, Data Rate up to 16 Gb/s (Upgrade: U16)
M8041A-C08	C08	BERT one Channel, Data Rate up to 8.5 Gb/s
M8041A-C16	C16	BERT one Channel, Data Rate up to 16 Gb/s (Upgrade: UED)

M8041A- Module Functionality

Table 76 M8041A- Module Functionality

Product	Option	Description
M8041A-0G2	0G2	Second Channel for Generator, License
M8041A-0A2	0A2	Second Channel for Analyzer, License
M8041A-0G3	0G3	Advanced Jitter Sources for Receiver Characterization, Module-wide License
M8041A-0G4	0G4	Multi-tap Deemphasis, Module-wide License
M8041A-0G5	0G5	Adjustable ISI, Module-wide License
M8041A-0G6	0G5	Reference Clock Input with Multiplying PLL, Clockgroup-wide License
M8041A-0G7	0G7	Advanced Interference Sources for Receiver Characterization, Module-wide License
M8041A-0S1	0S1	Interactive Link Training for PCI Express, Clockgroup-wide License
M8041A-0S2	0S2	SER/FER Analysis for Coded and Retimed Loopback, Clockgroup-wide License

Product	Option	Description
M8041A-0A3	0A3	Analyzer Equalization, Module-wide License
M8041A–0S3	0S3	Interactive Link Training for USB 3.2 Gen 1 and USB 3.2 Gen 2, Module wide License
M8041A–0S4	0S4	Interactive Link Training for PCI Express for PCI Express 8GT/s and 16GT/s, Clock Group wide License
M8041A-0S1	0S1	Interactive Link Training for PCI Express, 8GT/s, Clock Group wide License
M8041A–0SX	0SX	10GBASE-KR Transmitter Equalization Training, Module-wide License

M8041A - License Upgrades for M8041A High-Performance BERT Module

Table 77 M8041A - License Upgrades for M8041A High-Performance BERT Module

Product	Option	Description
M8041A-U16	U16	Upgrade to 16 Gb/s data rate from M8041A-G08 and M8041A-C08, Module-wide License
M8041A-UED	UED	Upgrade to BERT from M8041A-G08 and M8041A-G16, Module-wide License
M8041A-UG2	UG2	Upgrade to Second Channel for Generator, License
M8041A-UA2	UA2	Upgrade to Second Channel for Analyzer, License
M8041A-UG3	UG3	Upgrade to Advanced Jitter Sources for Receiver Characterization, Module-wide License
M8041A-UG4	UG4	Upgrade to Multi-tap Deemphasis, Module-wide License
M8041A-UG5	UG5	Upgrade to Adjustable ISI, Module-wide License
M8041A-UG6	UG6	Upgrade to Reference Clock Input with Multiplying PLL, Clockgroup-wide License
M8041A-UG7	UG7	Upgrade to Advanced Interference Sources for Receiver Characterization, Module-wide License
M8041A-US1	US1	Upgrade to Interactive Link Training for PCI Express, Clockgroup-wide License
M8041A-US2	US2	Upgrade to SER/FER Analysis for Coded and Retimed Loopback, Clockgroup-wide License
M8041A-UA3	UA3	Upgrade to Analyzer Equalization, Module-wide License
M8041A-US3	US3	Upgrade to Interactive Link Training for USB 3.2 Gen 1 and USB 3.2 Gen 2, Module wide License
M8041A-US4	US4	Upgrade to Interactive Link Training for PCI Express for PCI Express 8GT/s and 16GT/s, Clock Group wide License
M8041A–U14	U14	Upgrade of M8041A-0S1 to 0S4, Interactive Link Training for PCI Express for 8GT/s and 16GT/s, Clock Group wide License

Product	Option	Description
M8041A-US1	US1	Upgrade to Interactive Link Training for PCI Express, 8GT/s, Clock Group wide License
M8041A-USX	USX	Upgrade to 10GBASE-KR Transmitter Equalization Training, Module-wide License
M8041A–UR3	UR3	Upgrade of M8041A-0A3 with latest CTLE Presets, Return-to-Factory
M8041A-US6	US6	Upgrade to SAS-3 transmitter equalization training, module-wide license.

M8051A - High-Performance BERT Module

M8051A- Basic Selection

Table 78 M8051A- Basic Selection

Product	Option	Description
M8051A-G08	G08	Generator one Channel, Data Rate up to 8.5 Gb/s
M8051A-G16	G16	Generator one Channel, Data Rate up to 16 Gb/s (Upgrade: U16)
M8051A-C08	C08	BERT one Channel, Data Rate up to 8.5 Gb/s
M8051A-C16	C16	BERT one Channel, Data Rate up to 16 Gb/s (Upgrade: UED)

M8051A- Module Functionality

Table 79 M8051A- Module Functionality

Product	Option	Description
M8051A-0G2	0G2	Second Channel for Generator, License
M8051A-0A2	0A2	Second Channel for Analyzer, License
M8051A-0G3	0G3	Advanced Jitter Sources for Receiver Characterization, Module-wide License
M8051A-0G4	0G4	Multi-tap Deemphasis, Module-wide License
M8051A-0G5	0G5	Adjustable ISI, Module-wide License

Product	Option	Description
M8051A-0G7	0G7	Advanced Interference Sources for Receiver Characterization, Module-wide License
M8051A-0A3	0A3	Analyzer Equalization, Module-wide License
M8051A–0SX	OSX	10GBASE-KR Transmitter Equalization Training, module-wide license

M8051A - License Upgrades for M8051A High-Performance BERT Module

Table 80 M8051A - License Upgrades for M8051A High-Performance BERT Module

Product	Option	Description
M8051A-U16	U16	Upgrade to 16 Gb/s data rate from M8051A-G08 and M8051A-C08, Module-wide License
M8051A-UED	UED	Upgrade to BERT from M8051A-G08 and M8051A-G16, Module-wide License
M8051A-UG2	UG2	Upgrade to Second Channel for Generator, Module-wide License
M8051A-UA2	UA2	Upgrade to Second Channel for Analyzer, Module-wide License
M8051A-UG3	UG3	Upgrade to Advanced Jitter Sources for Receiver Characterization, Module-wide License
M8051A-UG4	UG4	Upgrade to Multi-tap Deemphasis, Module-wide License
M8051A-UG5	UG5	Upgrade to Adjustable ISI, Module-wide License
M8041A-UG7	UG7	Upgrade to Advanced Interference Sources for Receiver Characterization, Module-wide License
M8051A-UA3	UA3	Upgrade to Analyzer Equalization, Module-wide License
M8051A-U16	U16	Upgrade to 16 Gb/s data rate from M8051A-G08 and M8051A-C08, Module-wide License
M8051A–USX	USX	Upgrade to 10GBASE-KR Transmitter Equalization Training, Module-wide License
M8051A–UR3	UR3	Upgrade of M8051A-0A3 with latest CTLE Presets, Return-to-Factory
M8051A-US6	US6	Upgrade to SAS-3 transmitter equalization training, module-wide license

M8062A 32Gb/s Front-end for J-BERT M8020A High-Performance BERT

M8062A - Basic Selection

Table 81 M8062A - Basic Selection

Product	Option	Description
M8062A-C32	C32	32 Gb/s BERT front-end
M8062A-G32	G32	32 Gb/s Pattern generator front-end

M8062A - Module Functionality

Table 82 M8062A - Module Functionality

Product	Option	Description
M8062A-0G4	0G4	Multi-tap Deemphasis License
M8062A-0G5	0G5	Adjustable Intersymbol Interference (ISI) License
M8062A-0A3	0A3	Analyzer Equalization License
M8062A-0A4	0A4	Clock Recovery up to 32 Gb/s
M8062A–0SC	OSC	100GBASE-KR4 and 25GBASE-KR Transmitter Equalization Training, Module-wide License

M8062A - License Upgrades for M8062A 32Gb/s Front-end for J-BERT M8020A High-Performance BERT

Table 83 M8062A - License Upgrades for M8062A 32Gb/s Front-end for J-BERT M8020A High-Performance BERT

Product	Option	Description
M8062A-UED	UED	Upgrade of M8062A-G32 Pattern Generator to M8062A-C32 BERT License
M8062A-UA3	UA3	Upgrade of M8062A to Analyzer Equalization License
M8062A-UG4	UG4	Upgrade of M8062A to Multi-tap Deemphasis License

Product	Option	Description
M8062A-UG5	UG5	Upgrade of M8062A to Adjustable Intersymbol Interference License
M8062A-UA4	UA4	Upgrade of M8062A to Clock Recovery up to 32 Gb/s
M8062A–USC	USC	Upgrade of 100GBASE-KR4 and 25GBASE-KR Transmitter Equalization Training, module-wide license
M8062A-US6	US6	Upgrade to SAS-3 transmitter equalization training, module-wide license

NOTE In addition to the M8062A-UA4 license, M8062A modules with serial numbers < MY55400300 may also require a hardware upgrade in order to enable the CDR feature.

M8040A Licenses

M8045A Pattern generator and clock module, 32/64 GBd

M8045A - Basic Selection

Table 84 M8045A - Basic Selection

Product	Option	Description
M8045A-G32	G32	Pattern generator one channel NRZ, data rate up to 32 GBd (requires remote head, M8057A/B)
M8045A-G64	G64	Pattern generator one channel NRZ, data rate up to 64 GBd (requires remote head, M8057A/B)
M8045A-0G2	0G2	Second channel, hardware and license (requires remote head, M8057A/B)
M8045A-0G3	0G3	Advanced jitter sources for receiver characterization, module-wide license
M8045A-0G4	0G4	Deemphasis, module-wide license
M8045A-0P3	0P3	PAM4 encoding up to 32 GBd, module-wide license
M8045A-0P6	0P6	Extension to PAM4 encoding up to 64 GBd, module-wide license
M8045A-0G9	0G9	FEC encoding, module-wide license
M8045A-0G6	0G6	Reference Clock Input with Multiplying PLL

M8045A - License Upgrades for M8045A

Table 85 M8045A - License Upgrades for M8045A

Product	Option	Description
M8045A-U64	U64	Upgrade to 64 GBd (requires remote head, M8057A/B)
M8045A-UG2	UG2	Upgrade to second channel, hardware and license (requires remote head, M8057A/B)
M8045A-UG3	UG3	Upgrade to advanced jitter sources for receiver characterization, module-wide license
M8045A-UG4	UG4	Upgrade to deemphasis, module-wide license
M8045A-UP3	UP3	Upgrade to PAM4 encoding up to 32 GBd, module-wide license

Product	Option	Description
M8045A-UP6	UP6	Upgrade to extension to PAM4 encoding up to 64 GBd, module-wide license
M8045A-UG9	UG9	Upgrade to FEC encoding
M8045A-UG6	UG6	Upgrade to reference clock input with multiplying PLL

NOTE Please note that M8045A-UG2 (upgrade to second channel) is a return-to-factory upgrade.

M8046A Analyzer Module, 32/64 GBd

M8046A - Basic Selection

Table 86 M8046A - Basic Selection

Product	Option	Description
M8046A-A32	A32	Analyzer, one channel, data rate up to 32 GBd, NRZ
M8046A-A64	A64	Analyzer, one channel, data rate up to 64 GBd, NRZ
M8046A-0P3	0P3	PAM4 decoding up to 32 GBd, license
M8046A-0P6	0P6	PAM4 Extension up to 58 GBd, License (requires M8046A with S/N> XXXX2000)
M8046A-A03	A03	Equalizer license
M8046A-0A3	0A3	Equalization, license (only needed for > 32 GBd)
M8046A-0A4	0A4	Clock Recovery for 32 GBd
M8046A-0A5	0A5	Clock Recovery for 64 GBd
M8046A-0S1	0S1	Interactive Link Training for PCIe 8/16/32 GT/s
M8046A-0S2	0S2	SKP OS Filtering for PCIe 2.5/5/8/16/32 GT/s and CCIX 20/25 Gb/s
M8046A-0S3	OS3	Interactive Link Training for USB 3.2 Gen1 and Gen2, single lane and dual lane
M8046A-0S4	OS4	SKP OS Filtering for USB 3.2 Gen1 and Gen2

Product	Option	Description
M8046A-0S6	0S6	SKP OS Filtering for SATA2, SATA3, SAS1, SAS2, and SAS3
M8046A-0N1	0N1	PCIe LTTSM for 64 GT/s, requires M8046-0S1/US1
M8046A-0N2	0N2	PCIe Filtering of SKP OS Extension for 64 GT/s, requires M8046A-0S2 or M8046A-US2

M8046A - License Upgrades for M8046A

Table 87 M8046A - License Upgrades for M8046A

Product	Option	Description
M8046A-UP3	UP3	Upgrade to PAM4 decoding up to 32 GBd, license
M8046A-UP6	UP6	Upgrade of M8046A to PAM4 Extension up to 58 GBd, License (requires M8046A-A64, -0A3 or -U64, -UA3)
M8046A-US1	US1	Upgrade to Interactive Link Training for PCIe 8/16/32 GT/s
M8046A-US2	US2	Upgrade to SKP OS Filtering for PCIe 2.5/5/8/16/32 GT/s and CCIX 20/25 Gb/s
M8046A-US3	US3	Upgrade to Interactive Link Training for USB 3.2 Gen1 and Gen2, single lane and dual lane
M8046A-US4	US4	Upgrade to SKP OS Filtering for USB 3.2 Gen1 and Gen2
M8046A-US6	US6	Upgrade to SKP OS Filtering for SATA2, SATA3, SAS1, SAS2, and SAS3
M8046A-UN1	UN1	Upgrade to PCIe LTTSM for 64 GT/s, requires M8046-0S1/US1
M8046A-UN2	UN2	Upgrade to PCIe Filtering of SKP OS Extension for 64 GT/s (Upgrade), requires M8046A-0S2 or M8046A-US2

M8050A Licenses

M8042A Pattern Generator Module

Table 88 M8042A - Basic Selection

Product	Option	Description
M8042A-G32	G32	Pattern generation up to 32 GBd for NRZ and PAM4
M8042A-G64	G64	Pattern generation up to 64 GBd for NRZ and PAM4
M8042A-G12	G12	Pattern generation up to 120 GBd for NRZ and PAM4
M8042A-0G2	0G2	Second channel
M8042A-0G4	0G4	Deemphasis
M8042A-0G6	0G6	Reference clock input with Multiplying PLL
M8042A-0G9	0G9	FEC encoding
M8042A-0P3	0P3	PAM3 Encoding
M8042A-0P6	0P6	PAM6 Encoding for 224 Gbps Interfaces
M8042A-0P8	0P8	PAM8 Encoding for 224 Gbps Interfaces

Table 89 M8042A - License Upgrades for M8042A

Product	Option	Description
M8042A-U64	U64	Upgrade from 32 to 64 GBd for M8042A Pattern Generator including NRZ and PAM4, module-wide license
M8042A-U12	U12	Upgrade from 64 to 120 GBd for M8042A Pattern Generator including NRZ and PAM4, module-wide license
M8042A-UG4	UG4	Upgrade to De-emphasis, module-wide license
M8042A-UG6	UG6	Upgrade to reference clock input with Multiplying PLL
M8042A-UP3	UP3	Upgrade to PAM3 Encoding
M8042A-UP6	UP6	Upgrade to PAM6 Encoding for 224 Gbps Interfaces
M8042A-UP8	UP8	Upgrade to PAM8 Encoding for 224 Gbps Interfaces

M8043A Error Analyzer Module

Table 90 M8043A - Basic Selection

Product	Option	Description
M8043A-A32	A32	Error analysis up to 32.4 GBd for NRZ and PAM4
M8043A-A64	A64	Error analysis up to 64.4 GBd for NRZ and PAM4
M8043A-0A3	0A3	Equalization and De-Embedding capability
M8043A-0S2	0S2	SKP OS Filtering for PCIe7 128 GT/s

Table 91 M8043A - License Upgrades for M8043A

Product	Option	Description
M8043A-U64	U64	Upgrade to error analysis up to 64.4 GBd for NRZ and PAM4
M8043A-UA3	UA3	Upgrade to Equalization and De-Embedding capability
M8043A-US2	US2	Upgrade to SKP OS Filtering for PCIe7 128 GT/s

M8009A Clock Module

Table 92 M8009A - Basic Selection

Product	Option	Description
M8009A-0G3	0G3	Advanced Jitter Modulation for up to two Channels
M8009A-0G6	0G6	Reference Clock Multiplier
M8009A-062	062	Clock Generator two channel 60 GHz

Table 93 M8009A - License Upgrades for M8009A

Product	Option	Description
M8009A-UG3	UG3	Upgrade to Advanced Jitter Modulation for up to two Channels
M8009A-UG6	UG6	Upgrade to Reference Clock Multiplier
M8009A-UR1	UR1	Upgrade of M8009A from one to two channel 60 GHz clock

M8070B Plugin Licenses

Advanced Measurement Package Licenses

Table 94 on page -839 shows the various licenses available for **Advanced Measurement Package Licenses**:

Table 94 Advanced Measurement Package Licenses

License	Description
M8070ADVB-1FP	Advanced Measurement Package for M8000 Series BERT Test Solutions, node-locked perpetual license
M8070ADVB-1TP	Advanced Measurement Package for M8000 Series BERT Test Solutions, transportable perpetual license
M8070ADVB-1NP	Advanced Measurement Package for M8000 Series BERT Test Solutions, floating perpetual license
M8070ADVB-1UP	Advanced Measurement Package for M8000 Series BERT Test Solutions, USB portable perpetual license
M8070ADVB-1FL	Advanced Measurement Package for M8000 Series BERT Test Solutions, node-locked 12 month license
M8070ADVB-1TL	Advanced Measurement Package for M8000 Series BERT Test Solutions, transportable 12 month license
M8070ADVB-1NL	Advanced Measurement Package for M8000 Series BERT Test Solutions, floating 12 month license
M8070ADVB-1UL	Advanced Measurement Package for M8000 Series BERT Test Solutions, USB portable 12 month license
M8070ADVB-1FX	Advanced Measurement Package for M8000 Series BERT Test Solutions,node-locked 24 month license
M8070ADVB-1TX	Advanced Measurement Package for M8000 Series BERT Test Solutions, transportable 24 month license
M8070ADVB-1NX	Advanced Measurement Package for M8000 Series BERT Test Solutions, floating 24 month license
M8070ADVB-1UX	Advanced Measurement Package for M8000 Series BERT Test Solutions, USB portable 24month license
M8070ADVB-1FY	Advanced Measurement Package for M8000 Series BERT Test Solutions, node-locked 36 month license
M8070ADVB-1TY	Advanced Measurement Package for M8000 Series BERT Test Solutions, transportable 36 month license
M8070ADVB-1NY	Advanced Measurement Package for M8000 Series BERT Test Solutions, floating 36 month license
M8070ADVB-1UY	Advanced Measurement Package for M8000 Series BERT Test Solutions, USB portable 36 month license
M8070ADVB-1FF	Advanced Measurement Package for M8000 Series BERT Test Solutions, node-locked 6 month license
M8070ADVB-1TF	Advanced Measurement Package for M8000 Series BERT Test Solutions, transportable 6 month license

M8070ADVB-1NF	Advanced Measurement Package for M8000 Series BERT Test Solutions, floating 6 month license
M8070ADVB-1UF	Advanced Measurement Package for M8000 Series BERT Test Solutions, USB portable 6 month license
M8070ADVB-TRL	Advanced Measurement Package for M8000 Series BERT Test Solutions, 30 days free Trial

Error Distribution Analysis Package Licenses

Table 95 on page -840 shows the various licenses available for **Error Distribution Analysis Package**:

Table 95 Error Distribution Analysis Packagel Licenses

License	Description
M8070EDAB-1FP	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, node-locked perpetual license
M8070EDAB-1TP	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, transportable perpetual license
M8070EDAB-1NP	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, floating perpetual license
M8070EDAB-1UP	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, USB portable perpetual license
M8070EDAB-1FL	Error Distribution Analysis Packagefor M8000 Series BERT Test Solutions, node-locked 12 month license
M8070EDAB-1TL	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, transportable 12 month license
M8070EDAB-1NL	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, floating 12 month license
M8070EDAB-1UL	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, USB portable 12 month license
M8070EDAB-1FX	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, node-locked 24 month license
M8070EDAB-1TX	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, transportable 24 month license
M8070EDAB-1NX	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, floating 24 month license
M8070EDAB-1UX	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, USB portable 24month license
M8070EDAB-1FY	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, node-locked 36 month license
M8070EDAB-1TY	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, transportable 36 month license
M8070EDAB-1NY	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, floating 36 month license
M8070EDAB-1UY	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, USB portable 36 month license
M8070EDAB-1FF	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, node-locked 6 month license

M8070EDAB-1TF	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, transportable 6 month license
M8070EDAB-1NF	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, floating 6 month license
M8070EDAB-1UF	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, USB portable 6 month license
M8070EDAB-TRL	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, 30 days free Trial
M8070EDAB-DST	Error Distribution Analysis Package for M8000 Series BERT Test Solutions, 9 months TBL

Keysight Licensing Utilities

Keysight license management utilities enable you to install, view, transport, borrow, and uninstall the licenses you have purchased for use with Keysight products. The graphical user interface (GUI) gives you a visual representation of the licenses installed on your Keysight Technologies systems and provides access to the following features:

- View the licenses installed on a system
- Install licenses for new capabilities
- Transport licenses from one controller to another
- Borrow the licenses
- Remove licenses for capabilities no longer needed

For detailed information on **License Management Utilities**, refer to the web page: http://www.keysight.com/find/LicenseManager

NOTE

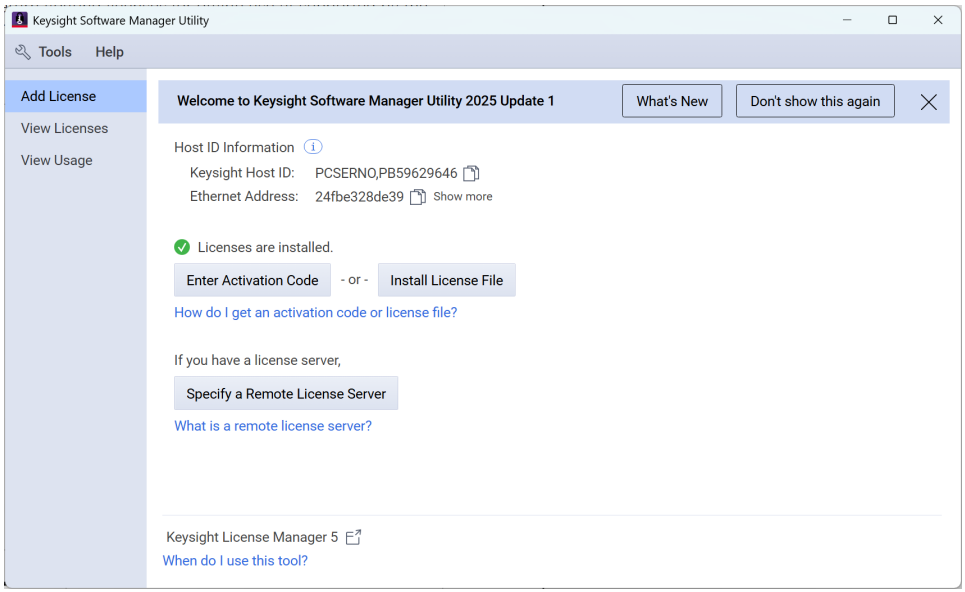
Please note that the **Keysight Software Manager Utility** is installed on your system when you install M8070B system software.

The **License Management Utilities** provides the **Keysight Software Manager Utility** that can be used to manage the licenses. For details, see Keysight Software Manager Utility on page 843.

Keysight Software Manager Utility

This license management utility allows you to manage all types of Keysight licenses for a wide variety of software products and instruments. You can use **Keysight Software Manager Utility** to:

- Install local licenses for your Keysight software
- Specify remote license servers where your software can get floating licenses
- See the Keysight licenses that are available to your software (whether local or remote)
- Borrow and return floating licenses for offline use (if supported by the license server)
- Transport licenses from one host to another.



Node-locked licenses	Install, view, and uninstall
Transportable licenses	Install, view, and transport
USB portable licenses	Install, view, and uninstall
Floating licenses	Install, view, and borrow; additionally, specify a remote (floating) license server

The **Keysight Software Manager Utility** is installed on your system when you install the M8070B software, however, you can download the it at: https://www.keysight.com/in/en/lib/software-detail/computer-software/pathwave-license-manager-download-3135511.html

Installing the Licenses

Adding License using Keysight Software Manager

Prerequisites for Adding a USB License

Before adding a USB license, you must ensure that:

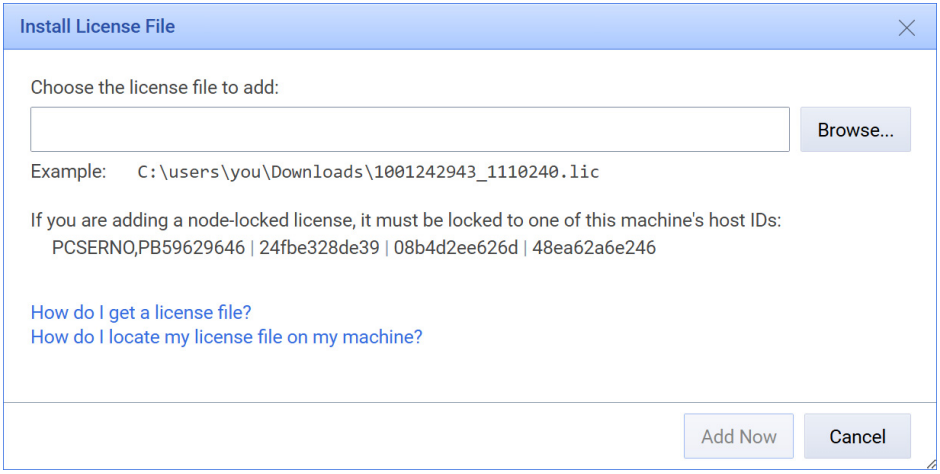
1. Make sure your Keysight application software is installed on this machine.
2. Have a license file that was issued for this machine or for a USB dongle.
   - If you don't have a license file, visit www.keysight.com/find/softwaremanager and follow the steps to request a license.
   - If you have received your license file attached to an email from Keysight, save the file to a location on this machine.
3. If your license is locked to a dongle (USB key, sold separately) rather than to a computer or instrument:
   - You must install a dongle driver. Follow these steps to install the dongle driver:
     - Get the FLEXID10 USB Dongle Driver from http://www.keysight.com/find/LicensingUsbDriver.
     - Extract the .zip file to this machine (Windows only).
     - Execute Setup64.exe (on 64-bit Windows), Setup32.exe (on 32-bit Windows), or the Linux .rpm file (on RHEL).
     - Follow the installer prompts, accepting the default values.
   - Connect the dongle to a USB port on this machine.

NOTE **If you add a license for software that is currently running (for example, to unlock a value-added feature of that software), the software will not immediately recognize the addition of a new license. You'll need to stop and restart the software before it will recognize the new license.**

For more information, you can also refer the *Keysight Licensing Administrator's Guide*: https://literature.cdn.keysight.com/litweb/pdf/5951-5739.pdf

Adding a License

1. Start Keysight Software Manager.
2. Click **Add a License File**.
3. Click **Browse**, browse to the license file on your machine, and click **Open**.
4. License files have the extension *.lic*. A typical license file name looks like this: *10e7c6207e9c_1083337.lic*.
5. Click **Add Now**.



Adding a Floating License

1. Follow the steps from 1 to 5 described in the section Adding a License on page 846.
2. If you are installing a network (floating) license or a counted local license, your machine must be running a local license server process.
3. If the process is not running for any reason, you will not be able to use your counted locked licenses or see them in Keysight Software Manager.
4. When you install Keysight Software Manager on Windows, the installer creates the Windows service EEsof EDA License Server to run this process. The EEsof EDA License Server service will start the license server process whenever you restart your PC.

You will not be able to add a license if it specifies a different port number from Keysight licenses already installed on this machine. You will need to edit your license file(s) to specify the same port number.

Some license files employ an earlier version of Keysight licensing and must be added using the previous license management tool. If you try to add such licenses in Keysight Software Manager, you may see a message directing you to use Keysight License Manager 5. If Keysight License Manager 5 is installed, click the provided button to start it. If it is not installed, you can download it from Keysight License Manager 5.

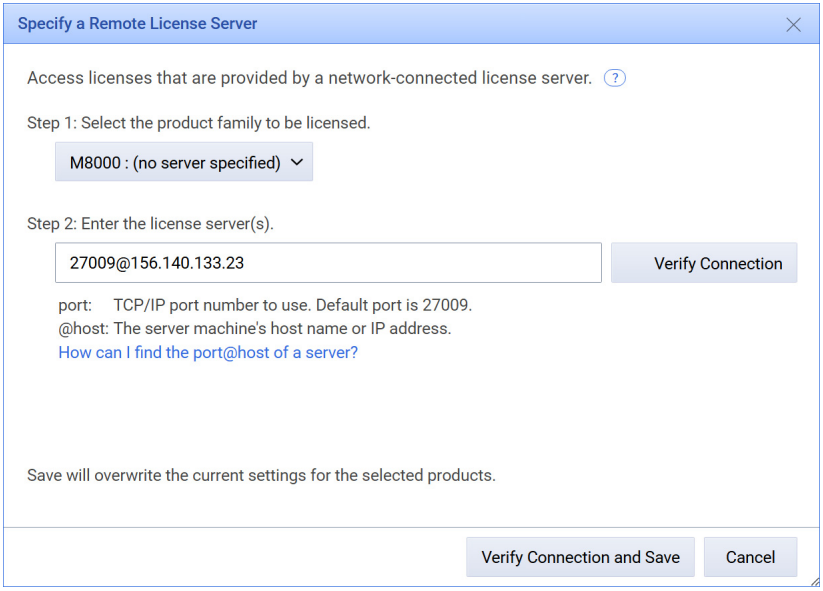
For more information, you can also refer the *Keysight Licensing Administrator's Guide*:
https://literature.cdn.keysight.com/litweb/pdf/5951-5739.pdf

Adding Remote License

To set where your Keysight product gets its floating licenses, open the **Edit Servers** dialog box as follows:

1 Start PathWave License Manager. The **Add License** tab is shown by default.

2 Click **Edit Servers**.



In the **Edit Servers** dialog box:

- The drop-down **Select Product Family** list shows all licensed Keysight products installed on your machine. Select (check) the products that need to use a remote license server(s). For each product, if license servers are already configured, they are listed underneath the product in the drop-down list. Note that any new server(s) you are specifying will be added to any externally-specified remote servers. When done with your selection, click outside the drop-down list to close it.
- Type the **port_number@host_name** of each server. Note the following when entering more than one server:
  - If the servers you are specifying are independent servers, separate them with spaces. Do not use commas. Some examples are:

    ```
    27009@server1.example.com 27009@156.140.133.23
    ```

    ```
    27009@server1.example.com 27009@server2.example.com
    ```

    You can get the port number and host name from your license server administrator (the sysadmin who set up and/or maintains your license server).
  - The port is typically 27009. It is included in the SERVER line of each license file on the server.
  - If your license server runs Windows, you can find its host name by going to **Control Panel** > **System** > **Full computer name**.
  - If your license server runs Linux, use one of the following commands:
    - `hostname`
    - `hostnamectl`
    - `cat /proc/sys/kernel/hostname`

    If you are specifying three servers that have been set up in a three-server redundant configuration (which is an advanced configuration), use commas between the servers.

3 In all ordinary circumstances, you should always specify the port number along with the host name, as shown above. If for some reason you need to specify a host name without a port, you still must include the @ symbol (for example, @server1.example.com).

4 Click **Verify Connection and Save** to complete your setup.

Installing Temporary License (Trial License)

A temporary (trial) license can be of the following two types:

- **30 days free trial license** - The 30 days free trial license for the M8000 Series of BER Test Solutions can be downloaded using the following weblink: http://www.keysight.com/main/editorial.jspx?cc=IN&lc=eng&ckey=2624767&nid=-32914.1100508&id=2624767
- **9 months DST license** - The DST license can only be ordered by rental companies and distributors.

The following procedure shows how to redeem and install a trial license on a dedicated host computer.

1 Locate the **Software License Entitlement Certificate**.

2 Follow the instructions on the **Software License Entitlement Certificate** to redeem your license.

3 You will receive a license file (in an email). The file has the suffix .lic.

4 Follow the instructions in the email to complete the installation of the license file.

5 In the M8070B software interface, verify that the license has been installed by selecting **Utilities** > **Licenses...** then viewing the license status in the **Installed** column.

Installing Module Licenses (not required for M8020A-BU1, M8040A-BU1 and M8050A-BU1)

Module licenses enable specific features in the modules of the M8020A/M8040A/M8050A system. Once a module license has been installed using the **Keysight License Utilities**, the next time the M8070B software and M8020A/M8040A/M8050A hardware are started, the license is recognized by the M8070B software and compared to the module's serial number. If the PC Host ID and serial number match, the EEPROM in the module is programmed and the feature is enabled. Even if the M8070B software license is transported to another host computer, the module feature will remain enabled.

The following procedure shows how to redeem and install a module license.

1 Locate the **Software License Entitlement Certificate**.

2 Follow the instructions on the **Software License Entitlement Certificate** to redeem your license.

3 You will receive a license file (in an email). The file has the suffix .lic.

4 Follow the instructions in the email to complete the installation of the license file.
5 In the M8070B software interface, verify that the license has been installed by selecting **Help** > **Licenses** then viewing the license status in the Installed column.

M8000 Series of BER Test Solutions
User Guide

11 Appendix

Basic Troubleshooting / 852
M8070B Factory Patterns / 854

KEYSIGHT TECHNOLOGIES

Basic Troubleshooting

Updating software components

There are two options to update the M8070B software components.

Option 1: Update from Keysight website

Updated versions of the M8020A, M8040A, M8050A and module specific software components are available on the Keysight website.

To download a software upgrade:

1 Go to http://www.keysight.com/find/M8000.
2 Click **View Technical Support**.
3 Type the model number of the instrument module for which software update is needed and click **Find**. Model number is located on the front panel of the module.
4 Click the **Driver & Software** tab on the module page.
5 Click **Download** to get the latest module specific software components.
6 Install the software components.

Option 2: Update from M8070B system software

1 Go to M8070B menu and click **Help** > **Check for Updates**. This opens the **Software Updates** window which displays the currently installed versions of the M8070B software components.
2 Click **Download** to install the latest software components.

The chassis does not power up

If the chassis or a module does not appear to power up, check the following:

- The circuit breakers at the rear of the chassis are set to the right, which is the **ON** position.
- The AC power cords are connected to a working power source.
- The electrical circuits are not overloaded. Check the combined power requirements of all equipment on the same circuit.
- There are no empty slots in the chassis. Leaving slots empty can overheat the inserted modules, causing them to shut down.

Module is exceptionally hot

- Check that the vent holes on the chassis are not blocked.
- Check that a filler panel module or an instrument module is installed into empty slots on either side of an instrument module.

Contacting Keysight Technologies

To locate a sales or service office near you, go to www.keysight.com/find/contactus.

M8070B Factory Patterns

The M8070B System Software provides a set of example factory supplied standard patterns. These patterns mimic real data packets and standard stress patterns.

NOTE Please note that these patterns are read only and cannot be modified. However, if you modify these patterns, you will have to save them with different name at different location.

CEI

Pattern	Description
CEIstress_bit	CEI Stress pattern
CID_bit	
QPRBS13-CEI_bit	This QPRBS13-CEI pattern is defined by OIF CEI-56G VSR Chapter 16.C.3.1 Draft 13. The quaternary PRBS13 test pattern is a 4-level pattern created by encoding a repeating PRBS13 pattern using Gray code and PAM4 encoding. Each cycle of QPRBS13-CEI is 8191 symbols long. To get correct output symbols the respective generator needs to have Gray Coding selected.
SSPR_bit	
SSPS-16_bit	
SSPS-64_bit	

DisplayPort

Pattern	Description
D24.3_b8b10	contains D24.3 symbols; pattern type is B8B10
DP-TS1_D10.2_b8b10	part of trainings sequence; pattern type is B8B10
DP-TS2_b8b10	part of trainings sequence; pattern type is B8B10
HBR2_SR-BF-BF-SR-256_CompEyePattren_b8b10	DP test pattern, see file name for details; pattern type is B8B10
HBR2_SR-BF-BF-SR-7796_CompEyePattren_b8b10	DP test pattern, see file name for details; pattern type is B8B10

Pattern	Description
HBR2_SR-BS-BS-SR-256_CompEyePattren_b8b10	DP test pattern, see file name for details; pattern type is B8B10
HBR2_SR-CP-CP-SR-256_CompEyePattren_b8b10	DP test pattern, see file name for details; pattern type is B8B10
TPS3_b8b10	part of trainings sequence; pattern type is B8B10
JBERT_CP2520.ptrn	DP test pattern
JBERT_TPS3	part of trainings sequence; pattern type is B8B10
JBERT_TPS4.ptrn	part of trainings sequence; pattern type is B8B10
DP_CP2520_Pattern1_BIT.ptrn	DisplayPort Compliance Eye Pattern (CP2520) Pattern 1
DP_CP2520_Pattern2minus_BIT.ptrn	DisplayPort Compliance Eye Pattern (CP2520) Pattern 2-
DP_CP2520_Pattern2plus_BIT.ptrn	DisplayPort Compliance Eye Pattern (CP2520) Pattern 2+
DP_IDLE_BIT.ptrn	DisplayPort Idle Pattern
DP_TPS1_BIT.ptrn	DisplayPort Link Training Pattern Sequence 1
DP_TPS2_BIT.ptrn	DisplayPort Link Training Pattern Sequence 2
DP_TPS3_BIT.ptrn	DisplayPort Link Training Pattern Sequence 3
DP_TPS4_BIT.ptrn	DisplayPort Link Training Pattern Sequence 4
SQ128_BIT.ptrn	DisplayPort Link Square Pattern (64 1s, 64 0s)
SQ64_BIT.ptrn	DisplayPort Link Square Pattern (32 1s, 32 0s)
UHBR_TPS1_BIT.ptrn	DisplayPort UHBR Link Training Sequence 1

EAQuickStartGuide

Pattern	Description
burst_25_bit	burst length 25
burst_25B_bit	burst length 25
sensetive_7_bit	
sensetive_7B_bit	

FDDI

Pattern	Description
FDDI_Jitter_bit	The Fiber Distributed Data Interface (FDDI) data dependent jitter test pattern is used for testing FDDI components or physical links. The pattern is 1280 bits long and is transmitted continuously during the test by repeating the pattern. The sequence causes a near worst case condition for inter-symbol interference and duty-cycle, baseline wander.
FDDI_Wander_bit	The FDDI baseline wander test pattern is used to test FDDI components for the effects of a change in the average DC level of the signal. The first 45,000 bits are of the code group (01010); the last 45,000 bits are of the code group (10101).
FDDI_Wander_b8b10	The Fiber Distributed Data Interface (FDDI) data dependent jitter test pattern is used for testing FDDI components or physical links.

FiberChannel/Gigabit Ethernet

Pattern	Description
CJTPAT_b8b10	This Fiber Channel Compliant (JTPAT) pattern for jitter tolerance is packaged into a Fiber Channel frame.
CJTPAT_bit	This Fiber Channel Compliant (JTPAT) pattern for jitter tolerance is packaged into a Fiber Channel frame.
CRPAT_b8b10	This Fiber Channel Compliant (RPAT) pattern for jitter generation is packaged into a Fiber Channel frame.
CRPAT_bit	This Fiber Channel Compliant (RPAT) pattern for jitter generation is packaged into a Fiber Channel frame.
CSPAT_b8b10	This Fiber Channel supply noise (SPAT) pattern is packaged into a Fiber Channel frame for use in system level tests.
CSPAT_bit	This Fiber Channel supply noise (SPAT) pattern is packaged into a Fiber Channel frame for use in system level tests.
D21-5_bit	This pattern is used to test Fiber Channel and Gigabit Ethernet elements. It tests random jitter (RJ) and the symmetry of logic transitions. The pattern is composed of alternating logic highs and lows and is repeated continuously. Disparity rules are followed. 1010101010 1010101010 (binary)
JSPAT_b8b10	This Fiber Channel Compliant (JSPAT) pattern unframed using B8B10 format
JSPAT_bit	This Fiber Channel Compliant (JSPAT) pattern unframed using BIT format
JTPAT_b8b10	This is a Fiber Channel jitter tolerance pattern, used to test receiver CDR to large instantaneous phase jumps.
JTPAT_bit	This is a Fiber Channel jitter tolerance pattern, used to test receiver CDR to large instantaneous phase jumps.
JTSPAT_b8b10	This Fiber Channel Compliant (JTSPAT) pattern unframed using B8B10 format
JTSPAT_bit	This Fiber Channel Compliant (JTSPAT) pattern unframed using BIT format

Pattern	Description
K28-5_b8b10	K28.5 pattern, tests random and deterministic jitter.
K28-5_bit	K28.5 pattern, tests random and deterministic jitter.
K28-7_bit	This pattern is used to test Fiber Channel and Gigabit Ethernet elements. It has a large low frequency content that is used to test low frequency random jitter (RJ) and PLL tracking errors. The pattern is composed of five logic highs, followed by five logic lows. This is repeated continuously and disparity rules are followed: 11111 00000 11111 00000 (binary).
RPAT_b8b10	This is a Fiber Channel random data pattern.
RPAT_bit	This is a Fiber Channel random data pattern.
SPAT_b8b10	This is a Fiber Channel supply noise stimulus test pattern.
SPAT_bit	This is a Fiber Channel supply noise stimulus test pattern.

PCI Express

Pattern	Description
compliance_b8b10	Compliance patterns
compliance_bit	Compliance patterns
test_payload_b8b10	Compliance pattern; pattern format B8B10
test_payload_bit	Compliance pattern; pattern format BIT
ts1_b8b10	part of trainings sequence; pattern format B8B10
ts1_bit	part of trainings sequence; pattern format BIT
ts1_skp1_b8b10	part of trainings sequence; pattern format B8B10
ts1_skp1_bit	part of trainings sequence; pattern format BIT
ts1_skp_bit	part of trainings sequence; pattern format BIT
ts2_b8b10	part of trainings sequence; pattern format B8B10
ts2_bit	part of trainings sequence; pattern format BIT

Pattern	Description
ts2_skp_bit	part of trainings sequence; pattern format BIT
ts2_skp2.b8b10	part of trainings sequence; pattern format B8B10
ts2_skp2.bit	part of trainings sequence; pattern format BIT

PCI Express 2

Pattern	Description
Compliance5G_b8b10	
PCIe2_Compliance_b8b10	
PCIe2_trainLB_1_bit	
PCIe2_trainLB_2_bit	
PCIe2_trainLB_3_bit	
TrainLoopback5G_1_bit	
TrainLoopback5G_2_bit	

PCI Express 3

Pattern	Description
Calibration/DMSI_CMSI_cal_BIT	
Calibration/PCIe3_Compliance_lane0_BIT_8G	
Calibration/RJ_SJ_cal_BIT	
Calibration/Step_BIT	
Calibration/TxEQ_cal_BIT	

Pattern	Description
Test/PCIe3_modified_compliance_lane_0_CC_BIT_8G	PCIe 8 GT/s Modified Compliance pattern for lane 0 for common reference clock, version for pattern generator
Test/PCIe3_modified_compliance_lane_0_IR_BIT_8G	PCIe 8 GT/s Modified Compliance pattern for lane 0 for independent reference clock, version for pattern generator
Test/PCIe3_modified_compliance_lane_0_SKPOS_filtering_M8046A_BIT_8G	PCIe 8 GT/s Modified Compliance pattern for lane 0 for common reference as well as independent reference clock, version for error detector operating with SKP OS filtering

PCI Express 4

Pattern	Description
Calibration/DMSI_CMSI_cal_BIT	
Calibration/PCIe4_Compliance_lane0_BIT_16G	
Calibration/RJ_SJ_cal_BIT	
Calibration/Step_BIT	
Calibration/TxEQ_cal_BIT	
Test/PCIe4_modified_compliance_lane_0_CC_BIT_16G	PCIe 16 GT/s Modified Compliance pattern for lane 0 for common reference clock, version for pattern generator
Test/PCIe4_modified_compliance_lane_0_IR_BIT_16G	PCIe 16 GT/s Modified Compliance pattern for lane 0 for independent reference clock, version for pattern generator
Test/PCIe4_modified_compliance_lane_0_SKPOS_filtering_M8046A_BIT_16G	PCIe 16 GT/s Modified Compliance pattern for lane 0 for common reference as well as independent reference clock, version for error detector operating with SKP OS filtering

PCI Express 5

Pattern	Description
Calibration/DMSI_CMSI_cal_BIT	
Calibration/RJ_SJ_cal_BIT	
Calibration/Step_BIT	
Calibration/TxEQ_cal_BIT	
Test/PCIe5_modified_compliance_lane_0_CC_BIT_32G	PCIe 32 GT/s Modified Compliance pattern without precoding for lane 0 for common reference clock, version for pattern generator
Test/PCIe5_modified_compliance_lane_0_IR_BIT_32G	PCIe 32 GT/s Modified Compliance pattern without precoding for lane 0 for independent reference clock, version for pattern generator
Test/PCIe5_modified_compliance_lane_0_SKPOS_filtering_M8046A_BIT_32G	PCIe 32 GT/s Modified Compliance pattern without precoding for lane 0 for common reference as well as an independent reference clock, version for error detector operating with SKP OS filtering
Test/PCIe5_modified_compliance_lane_0_CC_BIT_32G_precoding_off_V2	PCIe 32 GT/s Modified Compliance pattern without precoding for lane 0 for common reference clock, version for pattern generator; precoding deactivated
Test/PCIe5_modified_compliance_lane_0_CC_BIT_32G_precoding_on_V2	PCIe 32 GT/s Modified Compliance pattern without precoding for lane 0 for common reference clock, version for pattern generator; precoding activated
Test/PCIe5_modified_compliance_lane_0_IR_BIT_32G_precoding_off_V2	PCIe 32 GT/s Modified Compliance pattern without precoding for lane 0 for independent reference clock, version for pattern Generator, precoding deactivated
Test/PCIe5_modified_compliance_lane_0_IR_BIT_32G_precoding_on_V2	PCIe 32 GT/s Modified Compliance pattern without precoding for lane 0 for independent reference clock, version for pattern Generator, precoding activated
Test/PCIe5_modified_compliance_lane_0_SKPOS_filtering_M8046A_BIT_32G_V2	PCIe 32 GT/s Modified Compliance pattern without precoding for lane 0 for common reference as well as an independent reference clock, version for error detector operating with SKP OS filtering, for PG v2 patterns

PCI Express 6

Pattern	Description
PG_Modified_compliance_not_precoded	PCIe Gen6 modified compliance pattern with precoding disabled for PG (These are FEC encoded patterns and include SKP Ordered sets).
ED_Modified_compilance_FEC_enable_not_precoded	PCIe Gen6 modified compliance pattern with precoding disabled for ED (These patterns does not contain SKP Ordered sets). These are used when FEC error correction has not been enabled in ED.
ED_Modified_compliance_FEC_disable_not_precoded	PCIe Gen6 modified compliance pattern with precoding disabled for ED (These patterns does not contain SKP Ordered sets and EIEOS ordered sets). These are used when FEC error correction has been enabled in ED. EIEOS ordered sets are not included in these as FEC correction is not performed on EIEOS.
PG_Modified_compliance_not_precoded_IR	Modified compliance pattern for PCI Express 64 GT/s. This version of the pattern is not precoded and the SKP OS insertion rate is for the IR clocking case.
PG_Modified_compliance_precoded	Modified compliance pattern for PCI Express 64 GT/s. This version of the pattern is precoded and the SKP OS insertion rate is for the CC clocking case.
PG_Modified_compliance_precoded_IR	Modified compliance pattern for PCI Express 64 GT/s. This version of the pattern is precoded and the SKP OS insertion rate is for the IR clocking case.

PRBS

Pattern	Description
PRBS7_1-2_bit	PRBS 2^7 with a mark density of 1/2
PRBS7_1-8_bit	PRBS 2^7 with a mark density of 1/8
PRBS7_2-8_bit	PRBS 2^7 with a mark density of 2/8
PRBS7_6-8_bit	PRBS 2^7 with a mark density of 6/8
PRBS7_7-8_bit	PRBS 2^7 with a mark density of 7/8
PRBS10_1-2_bit	PRBS 2^10 with a mark density of 1/2

Pattern	Description
PRBS10_1-8_bit	PRBS 2^10 with a mark density of 1/8
PRBS10_2-8_bit	PRBS 2^10 with a mark density of 2/8
PRBS10_6-8_bit	PRBS 2^10 with a mark density of 6/8
PRBS10_7-8_bit	PRBS 2^10 with a mark density of 7/8
PRBS11_1-2_bit	PRBS 2^11 with a mark density of 1/2
PRBS11_1-8_bit	PRBS 2^11 with a mark density of 1/8
PRBS11_2-8_bit	PRBS 2^11 with a mark density of 2/8
PRBS11_6-8_bit	PRBS 2^11 with a mark density of 6/8
PRBS11_7-8_bit	PRBS 2^11 with a mark density of 7/8
PRBS13_1-2_bit	PRBS 2^13 with a mark density of 1/2
PRBS13_1-8_bit	PRBS 2^13 with a mark density of 1/8
PRBS13_2-8_bit	PRBS 2^13 with a mark density of 2/8
PRBS13_6-8_bit	PRBS 2^13 with a mark density of 6/8
PRBS13_7-8_bit	PRBS 2^13 with a mark density of 7/8
PRBS15_1-2_bit	PRBS 2^15 with a mark density of 1/2
PRBS15_1-8_bit	PRBS 2^15 with a mark density of 1/8
PRBS15_2-8_bit	PRBS 2^15 with a mark density of 2/8
PRBS15_6-8_bit	PRBS 2^15 with a mark density of 6/8
PRBS15_7-8_bit	PRBS 2^15 with a mark density of 7/8
PRBS23_1-2_bit	PRBS 2^23 with a mark density of 1/2
PRBS23_1-8_bit	PRBS 2^23 with a mark density of 1/8
PRBS23_2-8_bit	PRBS 2^23 with a mark density of 2/8
PRBS23_6-8_bit	PRBS 2^23 with a mark density of 6/8
PRBS23_7-8_bit	PRBS 2^23 with a mark density of 7/8
PRBS7-1_1-2_bit	PRBS 2^7-1 with a mark density of 1/2
PRBS9_950_bit	PRBS 2^9-1 with the polynomial x^9+x^5+1

NOTE The mark density (MD) of a binary pattern can be calculated by dividing the number of one bits in the pattern by the length of the pattern.

$$MD = \frac{N_{One}}{N_{One} + N_{Zero}}$$

N_{One} - Number of 1s in the pattern.

N_{Zero} - Number of 0s in the pattern.

The range of mark density is 0.0 to 1.0.

SAS

Pattern	Description
JTPAT_b8b10	Jitter Tolerance Pattern (JTPAT) Minus
SAS_CJTPAT_Repeat_w_all_aligns_b8b10	CJTPAT framed for SAS; includes ALIGNs; uses B8B10 format
SAS_IDLE_CJTPAT_IDLE_ALIGNO_b8b10	IDLE, CJTAPT, IDLE framed for SAS; includes ALIGN 0; uses B8B10 format
scrambled_0-from-grex-demo-board_b8b10	Scrambled 0 pattern captured from G-Series scope demo board; uses B8B10 format

SATA

Pattern	Description
ALIGN_b8b10	Align primitive as defined in SATA standard.
COMP-long-2.6spec_b8b10	Long COMP pattern starting with negative running disparity as defined in SATA standard version 2.6
COMP-long-framed_b8b10	Obsolete long framed COMP pattern
COMP-long_b8b10	Long COMP pattern starting with negative running disparity as defined in SATA standard version 2.5

Pattern	Description
COMP-short-2.6spec_b8b10	Short COMP pattern starting with negative running disparity as defined in SATA standard version 2.6
COMP-short_b8b10	Short COMP pattern as defined in SATA standard version 2.5
Framed_COMP_20070905_2ALIGNs_newLBP_92160_b8b10	Long framed COMP according to SATA standard version 2.6 with 2 ALIGNs
Framed_COMP_20070907_2ALIGNs_oldLBP_92160_b8b10	Long framed COMP according to SATA standard version 2.5 with 2 ALIGNs
HFTP_b8b10	SATA High Frequency Test Pattern
HFTP_w_align_b8b10	SATA High Frequency Test Pattern; includes ALIGNs; uses B8B10 format
HTDP_long_b8b10	SATA long high transition density pattern
HTDP_short_b8b10	SATA long high transition density pattern
LBPspecv2.5-short-w-align_b8b10	SATA lone bit pattern according to SATA standard version 2.5; includes ALIGNs; uses B8B10 format
LBP_long-2.6spec_b8b10	SATA short lone bit pattern according to SATA standard version 2.6
LBP_long_b8b10	SATA long lone bit pattern according to SATA standard version 2.5
LBP_short-2.6spec_b8b10	SATA long lone bit pattern according to SATA standard version 2.6
LBP_short_b8b10	SATA short lone bit pattern according to SATA standard version 2.5
LFSCP_long_b8b10	SATA long low frequency spectral content pattern
LFSCP_short_b8b10	SATA short low frequency spectral content pattern
LTDP_long_b8b10	SATA long low transition density pattern
LTDP_short_b8b10	SATA short low transition density pattern
MFTP_b8b10	SATA mid frequency test pattern
SSOP_long_b8b10	SATA short simultaneous switching outputs pattern starting
SSOP_short_b8b10	SATA short simultaneous switching outputs pattern starting
k28.5_b8b10	K28.5 symbols; uses B8B10 format

USB 3.0

Pattern	Description
Clock_bit	clk/2 pattern; uses BIT format
D0_SCRAMBLED_b8b10	scrambled D0; uses B8B10 format
K25_K27_2SKP_b8b10	debug pattern; uses B8B10 format
K285_D0_b8b10	debug pattern; uses B8B10 format
LFPS_BURST_1us_IDLE_9us_bit	part of trainings sequence; uses BIT format
LFPS_IDLE_9us_BURST_1us_bit	part of trainings sequence; uses BIT format
LFPS_TRIGGER_bit	part of trainings sequence; uses BIT format
TS1_31_2SKP_b8b10	part of trainings sequence; uses B8B10 format
TS1_31_4SKP_b8b10	part of trainings sequence; uses B8B10 format
TS2_2SKP_b8b10	part of trainings sequence; uses B8B10 format
TS2_4SKP_b8b10	part of trainings sequence; uses B8B10 format
TSEQ_b8b10	part of trainings sequence; uses B8B10 format
BRST_2SKP_b8b10	part of trainings sequence; uses B8B10 format
BRST_4SKP_b8b10	part of trainings sequence; uses B8B10 format
COMMA_2SKP_b8b10	debug pattern; uses B8B10 format
COMMA_4SKP_b8b10	debug pattern; uses B8B10 format
CP0_2SKP_SCRAMBLED_b8b10	CP0 compliance pattern containing SKP doubles; pre-scrambled; uses B8B10 format
CP0_2SKP_for_SER_b8b10	CP0 compliance pattern containing SKP doubles; pre-scrambled; uses B8B10 format
CP0_4SKP_for_SER_b8b10	CP0 compliance pattern containing SKP doubles; pre-scrambled; uses B8B10 format
Clock16_bit	clk/16; uses BIT format
Clock8_bit	clk/8; uses BIT format
Clock4_bit	clk/4; uses BIT format
Clock2_bit	clk/2; uses BIT format

XAUI

Pattern	Description
CJPAT_bit	CJTPAT; uses BIT format
CRPAT_b8b10	CRPAT; uses B8B10 format
CRPAT_bit	CRPAT; uses BIT format

MPHY

Pattern	Description
UniPro1-LaneCJTPAT_b8b10	Pattern used for M-PHY Rx jitter tolerance test for 1 lane UniPro (CJTPAT, 8b/10b encoded).
UniPro1-LaneCJTPAT_bit	Pattern used for M-PHY Rx jitter tolerance test for 1 lane UniPro (CJTPAT, bit pattern).
UniPro1-LaneCRPAT_b8b10	Pattern used for M-PHY Tx test for 1 lane UniPro (CRPAT, 8b/10b encoded).
UniPro1-LaneCRPAT_bit	Pattern used for M-PHY Tx test for 1 lane UniPro (CRPAT, bit pattern).
UniPro2-LaneCJTPAT-Lane0_b8b10	Pattern used for M-PHY Rx jitter tolerance test for lane 1 of 2 UniPro (CJTPAT, 8b/10b encoded).
UniPro2-LaneCJTPAT-Lane0_bit	Pattern used for M-PHY Rx jitter tolerance test for lane 1 of 2 UniPro (CJTPAT, bit pattern).
UniPro2-LaneCJTPAT-Lane1_b8b10	Pattern used for M-PHY Rx jitter tolerance test for lane 2 of 2 UniPro (CJTPAT, 8b/10b encoded).
UniPro2-LaneCJTPAT-Lane1_bit	Pattern used for M-PHY Rx jitter tolerance test for lane 2 of 2 UniPro (CJTPAT, bit pattern).
UniPro2-LaneCRPAT-Lane0_b8b10	Pattern used for M-PHY Tx test for lane 1 of 2 UniPro (CRPAT, 8b/10b encoded).
UniPro2-LaneCRPAT-Lane0_bit	Pattern used for M-PHY Tx test for lane 1 of 2 UniPro (CRPAT, bit pattern).
UniPro2-LaneCRPAT-Lane1_bit	Pattern used for M-PHY Tx test for lane 2 of 2 UniPro (CRPAT, bit pattern).
UniPro2-LaneCRPAT-Lane1_b8b10	Pattern used for M-PHY Tx test for lane 2 of 2 UniPro (CRPAT, 8b/10b encoded).

IEEE

Pattern	Description
JP03A_bit	IEEE802.3bj clause 94.2.9.1 for 100GBASE-KP4. The JP03A test pattern is generated prior to PAM4 encoding. JP03A pattern is a repeating (0,3) sequence.
JP03B_bit	IEEE802.3bj clause 84.2.9.2 for 100GABSE-KP4. The JP03B test pattern is generated prior to PAM4 encoding. The JP03B pattern is a repeating sequence of (0,3) repeated 15 times followed by (3,0) repeated 16 times.
PAM4_Linearity_Test_bit	IEEE 802.3bj clause 94.2.9.4 transmitter linearity test pattern. To get correct output symbols the respective generator needs to have Uncoded selected.
PRBS13Q_Lane0_bit	PRBS13Q Lane 0 pattern as defined in IEEE 802.3 clause 120.5.11.2.3. To get correct output symbols the respective generator needs to have Gray Coding selected.
PRBS13Q_Lane1_bit	PRBS13Q Lane 1 pattern as defined in IEEE 802.3 clause 120.5.11.2.3. To get correct output symbols the respective generator needs to have Gray Coding selected.
PRBS13Q_Lane2_bit	PRBS13Q Lane 2 pattern as defined in IEEE 802.3 clause 120.5.11.2.3. To get correct output symbols the respective generator needs to have Gray Coding selected.
PRBS13Q_Lane3_bit	PRBS13Q Lane 3 pattern as defined in IEEE 802.3 clause 120.5.11.2.3. To get correct output symbols the respective generator needs to have Gray Coding selected.
QPRBS13_Lane0_bit_SelectGrayCoded	QPRBS13 Lane 0 pattern as defined in IEEE 802.3 clause 94.2.9.3. To get correct output symbols the respective generator needs to have Gray Coding selected.
SSPRQ_bit_SelectGrayCoded	SSPRQ pattern as defined in IEEE 802.3 clause 120.5.11.2.5. To get correct output symbols the respective generator needs to have Gray Coding selected.
SSPRQ_bit_SelectGrayCoded_D1p5	

USB3.0_LTSSM

Pattern	Description
BRST_Bit	BRST
loopbackED_B8B10	CP0 for ED
loopbackPG_Bit	CP0 for PG

USB3.1_LTSSM

Pattern	Description
CP9_BLOCK_ANALYZER_B128B132	CP9 for ED
CP9_BLOCK_GENERATOR_B128B132	CP9 for PG
IDLE_B128B132	

CCIX

Pattern	Description
Calibration/DMSI_CMSI_cal_BIT	
Calibration/RJ_SJ_cal_BIT	
Calibration/Step_BIT	
Calibration/TxEQ_cal_BIT	
Test/CCIX_modified_compliance_lane_0_CC_BIT_20G_25G	CCIX Modified Compliance pattern for lane 0 for common reference clock, version for pattern generator
Test/CCIX_modified_compliance_lane_0_IR_BIT_20G_25G	CCIX Modified Compliance pattern for lane 0 for independent reference clock, version for pattern generator
Test/CCIX_modified_compliance_lane_0_SKPOS_filtering_M8046A_BIT_20G_25G	CCIX Modified Compliance pattern for lane 0 for common reference as well as independent reference clock, version for error detector operating with SKP OS filtering

PAM3

Pattern	Description
PRTS7_L0_bit	PRTS7 pattern for Lane0
PRTS7_L1_bit	PRTS7 pattern for Lane1
PRTS7_L2_bit	PRTS7 pattern for Lane2
TS2_CLKSW_PRTS7_L0_bit	TS2 Clock switch pattern for lane 0
TS2_CLKSW_PRTS7_L1_bit	TS2 Clock switch pattern for lane 1
TS2_CLKSW_PRTS7_L2_bit	TS2 Clock switch pattern for lane 2
TS2_CLKSW_bit	TS2 Clock Switch pattern
STAIRS64_PAM3_2-bits-per-symbol_bit	Stair pattern with 64 symbols per step to be used if PAM3 encoding is selected.
PRBS11-1_PAM3_2-bits-per-symbol_bit	PRBS11-1 pattern to be used if PAM3 encoding is selected. It is two bits per symbol and only values 0 and 2 are occurring.
PAM3_SQ2	PAM3 square wave patterns of length 2 bytes
PAM3_SQ4	PAM3 square wave patterns of length 4 bytes
PAM3_SQ8	PAM3 square wave patterns of length 8 bytes
PAM3_SQ16	PAM3 square wave patterns of length 16 bytes
PAM3_SQ32	PAM3 square wave patterns of length 32 bytes
PAM3_SQ64	PAM3 square wave patterns of length 64 bytes
PAM3_SQ128	PAM3 square wave patterns of length 128 bytes
PAM3_SQ256	PAM3 square wave patterns of length 256 bytes

PAM6

Pattern	Description
PseudoRandomSymbolDistribution_1024_Symbols_PAM6	Pseudo Random Symbol Distribution: PRBS-like pattern with pseudo random symbol sequence, n symbols. To be used with respective line coding.
PseudoRandomSymbolDistribution_4096_Symbols_PAM6	Pseudo Random Symbol Distribution: PRBS-like pattern with pseudo random symbol sequence, n symbols. To be used with respective line coding.
PseudoRandomSymbolDistribution_8192_Symbols_PAM6	Pseudo Random Symbol Distribution: PRBS-like pattern with pseudo random symbol sequence, n symbols. To be used with respective line coding.
PseudoRandomSymbolDistribution_32768_Symbols_PAM6	Pseudo Random Symbol Distribution: PRBS-like pattern with pseudo random symbol sequence, n symbols. To be used with respective line coding.
PseudoRandomSymbolDistribution_65536_Symbols_PAM6	Pseudo Random Symbol Distribution: PRBS-like pattern with pseudo random symbol sequence, n symbols. To be used with respective line coding.
STAIRS_32SymbolsPerStep_192Symbols_PAM6	STAIRS: 32 symbols per step, 32 * 6 symbols total for PAM6. To be used with respective line coding.

PAM8

Pattern	Description
PseudoRandomSymbolDistribution_1024_Symbols_PAM8	Pseudo Random Symbol Distribution: PRBS-like pattern with pseudo random symbol sequence, n symbols. To be used with respective line coding.
PseudoRandomSymbolDistribution_4096_Symbols_PAM8	Pseudo Random Symbol Distribution: PRBS-like pattern with pseudo random symbol sequence, n symbols. To be used with respective line coding.
PseudoRandomSymbolDistribution_8192_Symbols_PAM8	Pseudo Random Symbol Distribution: PRBS-like pattern with pseudo random symbol sequence, n symbols. To be used with respective line coding.
PseudoRandomSymbolDistribution_32768_Symbols_PAM8	Pseudo Random Symbol Distribution: PRBS-like pattern with pseudo random symbol sequence, n symbols. To be used with respective line coding.
PseudoRandomSymbolDistribution_65536_Symbols_PAM8	Pseudo Random Symbol Distribution: PRBS-like pattern with pseudo random symbol sequence, n symbols. To be used with respective line coding.
STAIRS_32SymbolsPerStep_256Symbols_PAM8	STAIRS: 32 symbols per step, 32 * 8 symbols total for PAM8. To be used with respective line coding.

FEC

Pattern	Description
AlignmentMarkers_802_3cd	
IEEE_802_3cd_RS_544_514_Remote_Fault	IEEE802.3 MAC control word (0x1E) which is Reed Solomon Encoded and formatted according to IEEE802.3cd
IEEE_802_3cd_RS_544_514_Scrambled_Idle	IEEE802.3 MAC control word (0x00) which is Reed Solomon Encoded and formatted according to IEEE802.3cd

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