Getting Started Guide for ADS and PEPro for Power Electronics Applications

Introduction

This is a getting started guide for Advanced Design System (ADS) and Power Electronics Professional (PEPro). In this guide, you will find a step-by-step workflow of using ADS and PEPro for designing a switched-mode power supply. The example of the buck converter used in this guide is available in any install of ADS.

KEYSIGHT

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Evaluation of PathWave ADS

Trends in switched mode power supplies

The trend in switched-mode power supplies is to use wide band gap devices because these enable a higher switching frequency and higher edge speeds (the “di/dt” of the switched loop). These two in turn enable a smaller, lighter, cheaper power supply because the energy storage capacitors and magnetics can be smaller if you top them off more frequently. The higher edge speeds enable higher efficiency because there’s less heat dissipated when you have lower switching losses because the transistors spend less time in the dissipative cross over region.

Schematic view is no longer enough

These high slew rates come with a dark side, in particular the large spike voltage and noise generated by the layout parasitics, particularly inductance, of the PCB layout traces. This phenomenon is often called conductive electromagnetic interference (conductive EMI).

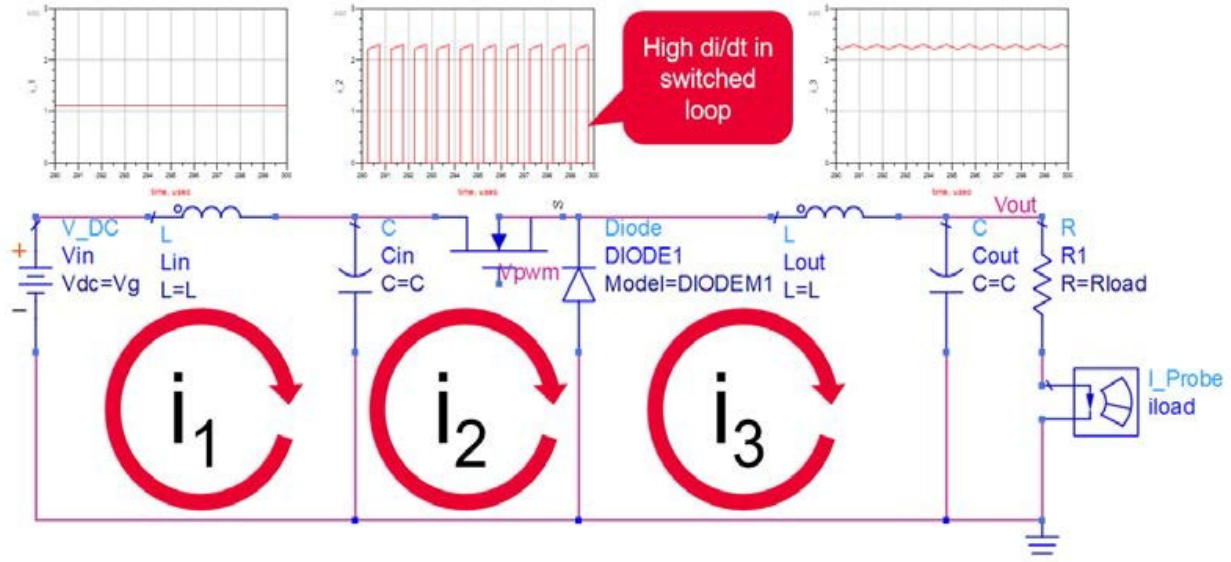


Figure 1. Current loops: Schematic view. Source: Keysight.com

ADS offers an EM-based model of layout parasitics

For example, in the below circuit, the spike voltage in the switch loop gets larger and larger as di/dt gets larger.

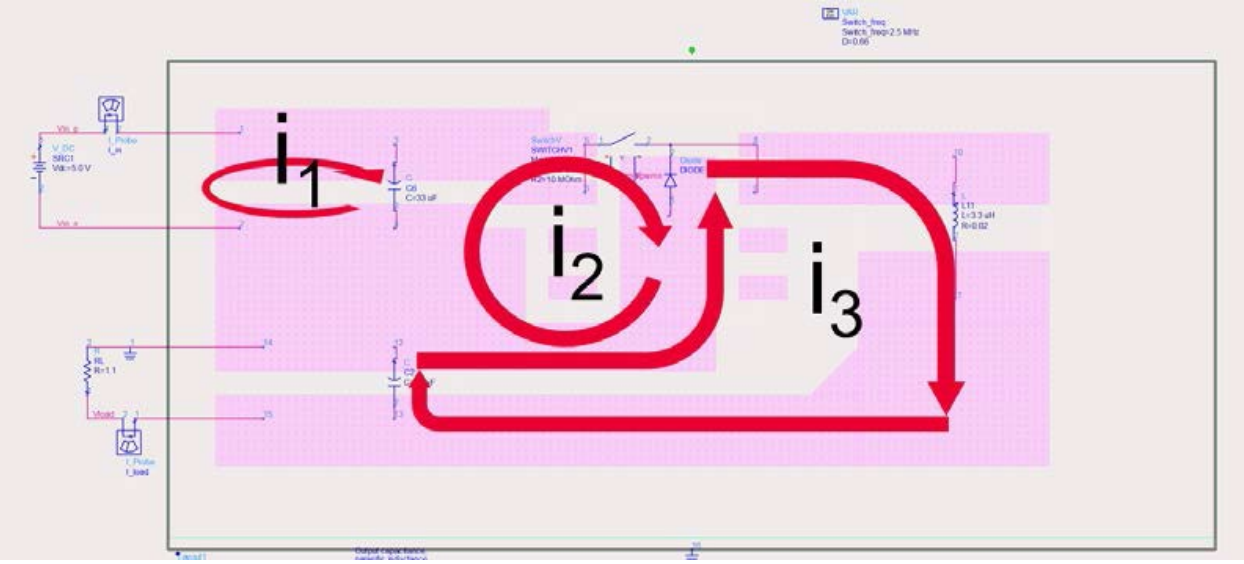


Figure 1. Current loops: Layout view

When to worry about layout parasitics inductance?

$$\tau \rightarrow \frac{\mu_0 l_{loop}}{R_{load}}$$

Rule of Thumb: “If the rise/fall time of the switch loop edges in nanoseconds approaches the quantity on the left (vacuum permeability 1.26 nH/mm times effective switched loop length in mm divided by load resistance in ohms), then layout parasitic will be a concern. We recommend you use ADS to add EM-based model of your PCB traces into your circuit simulation.”

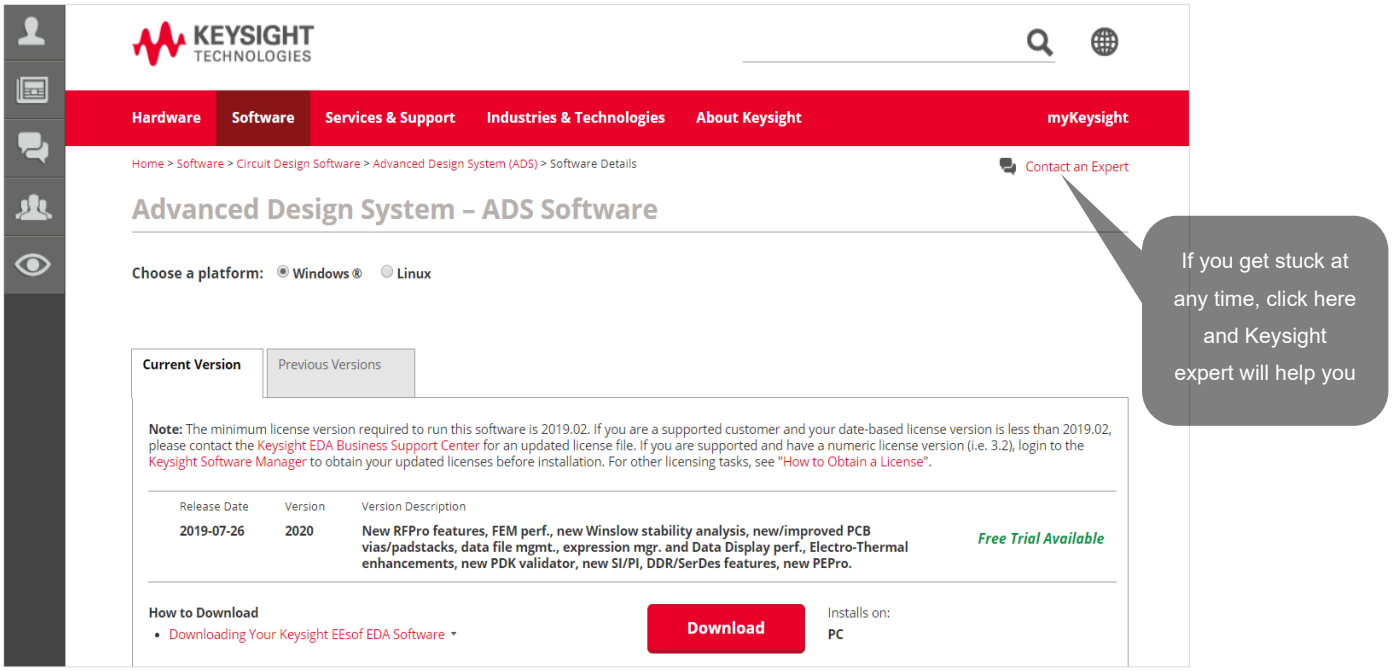
For such a planar loop and with typical circuit values (lloop = 1-10 mm, Rload = 0.1-1.0 ohm), problems begin as the rise time, τ, approaches tens of nanoseconds. The key point here is that ADS has a built in electromagnetic (EM) field solver allows you to extract an EM-based model of the layout parasitics. You can co-simulate regular SPICE-like lumped elements along with the effects of the layout. You can plot the voltage spikes and do "what if..." design space exploration, such as using a ground plane for the return current, to minimize their effects.

See https://www.youtube.com/watch?v=2Qa_KHyjbII

How to Evaluate ADS: Three Steps

Step 1: Download and install the binaries

Go to http://www.keysight.com/find/eesof-ads-latest-downloads



Step 2: Request a no-charge 30-day evaluation license

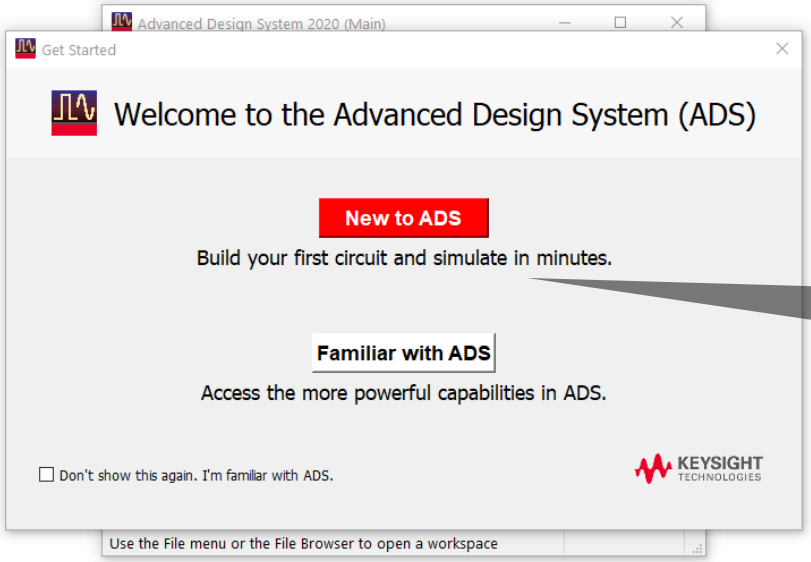
Go to http://www.keysight.com/find/eesof-ads-evaluation

Step 3: Follow this hands-on demonstration

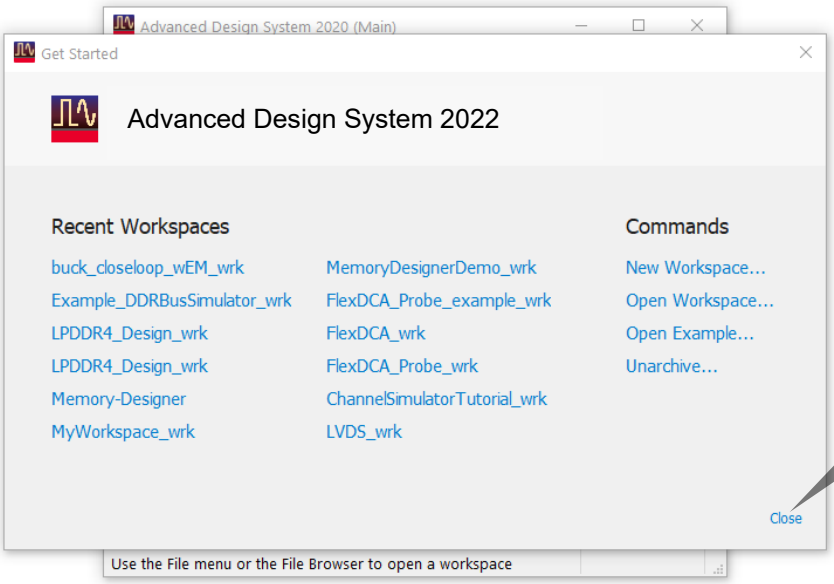
Hands-On Demonstration

Starting Advanced Design System

1. Go to Start > ADS to open Advanced Design System.
2. Select the Familiar with ADS then examine and close the Get Started pop-up window. The ADS main window remains.

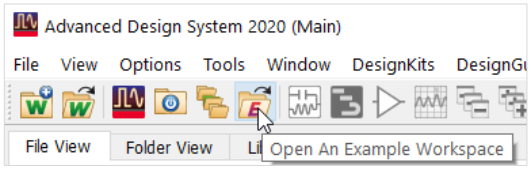


There are two modes: **New to ADS** and **Familiar with ADS**
Select **Familiar with ADS**

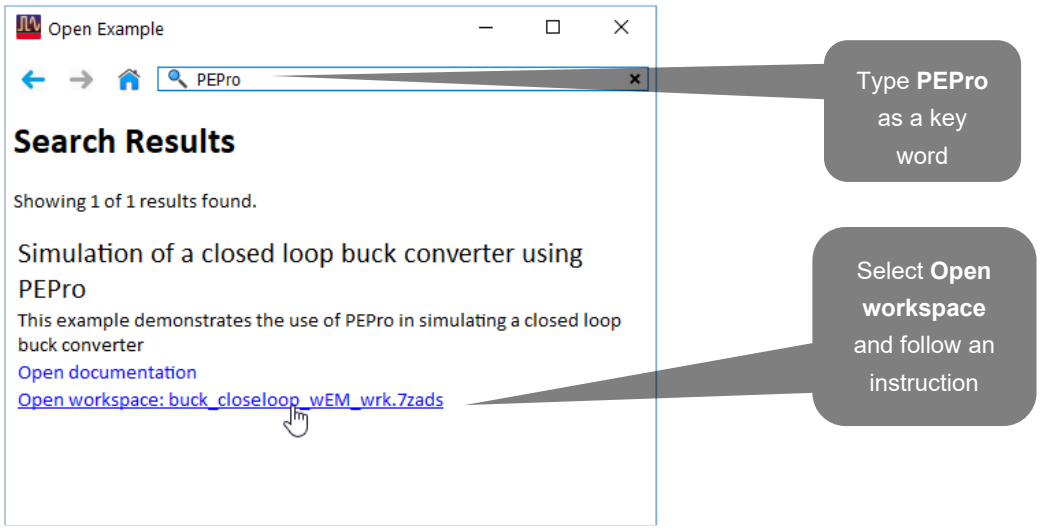


Take a look at the **Get Started** pop-up. Often, it's useful but we're not going to use it in this guide, so close it.

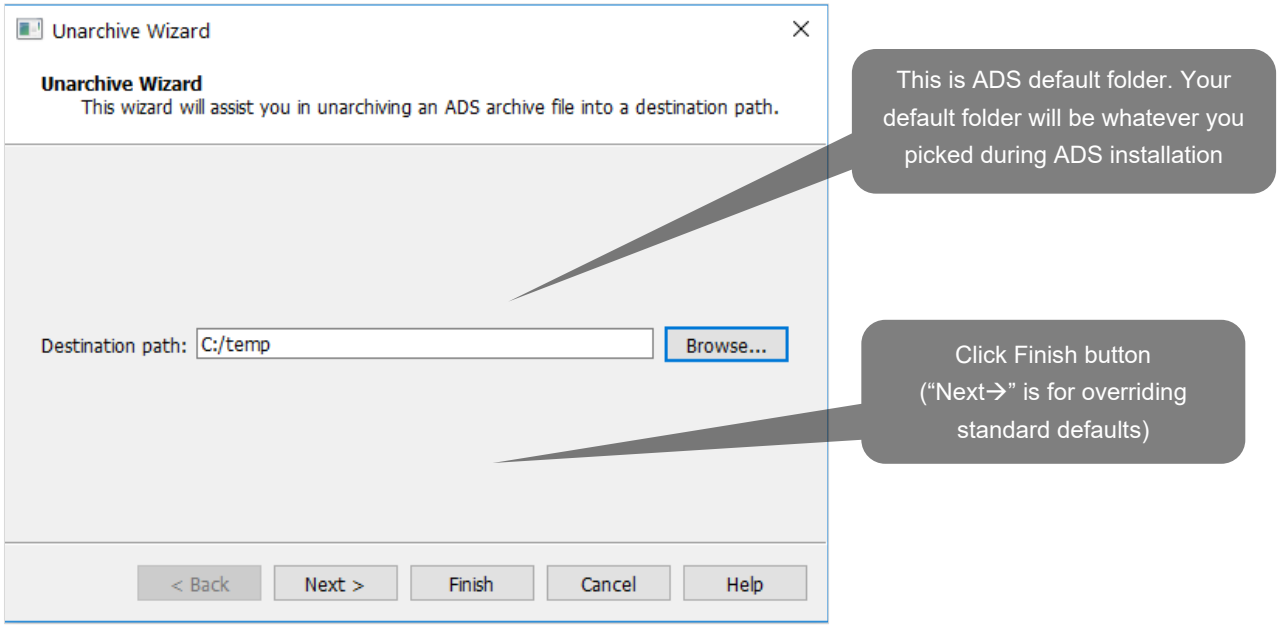
3. From the main window menu bar, select the File > Open > Example… dialog box or click on Open an Example Workspace icon on the top icon bar:



4. In the search filed type PEPro and look at found results below. Select



5. Click Browse and chose a directory to which a workspace/project will be unarchived. Click Finish.



6. Close the Readme and Open Example windows, leaving the main window open.

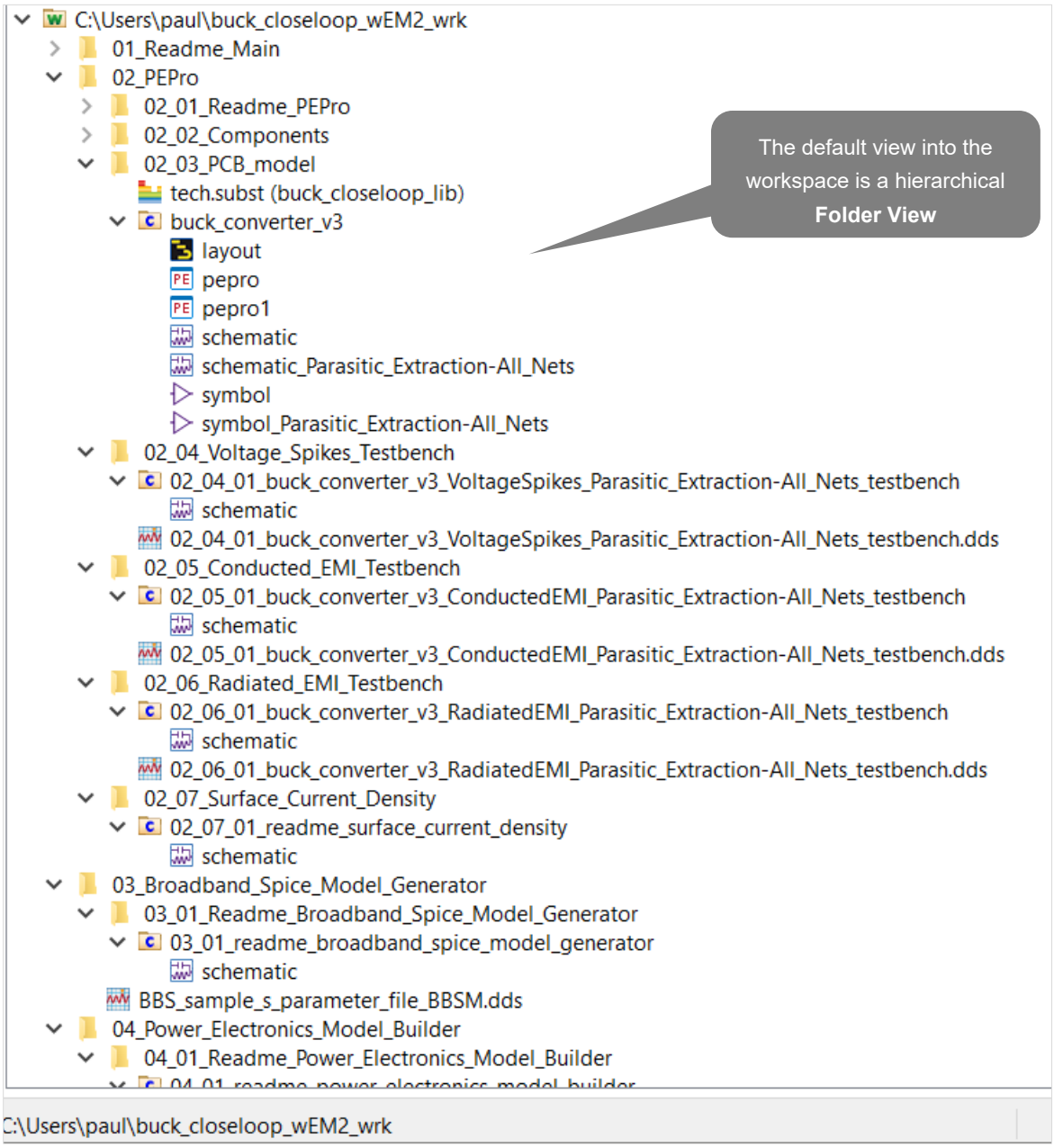
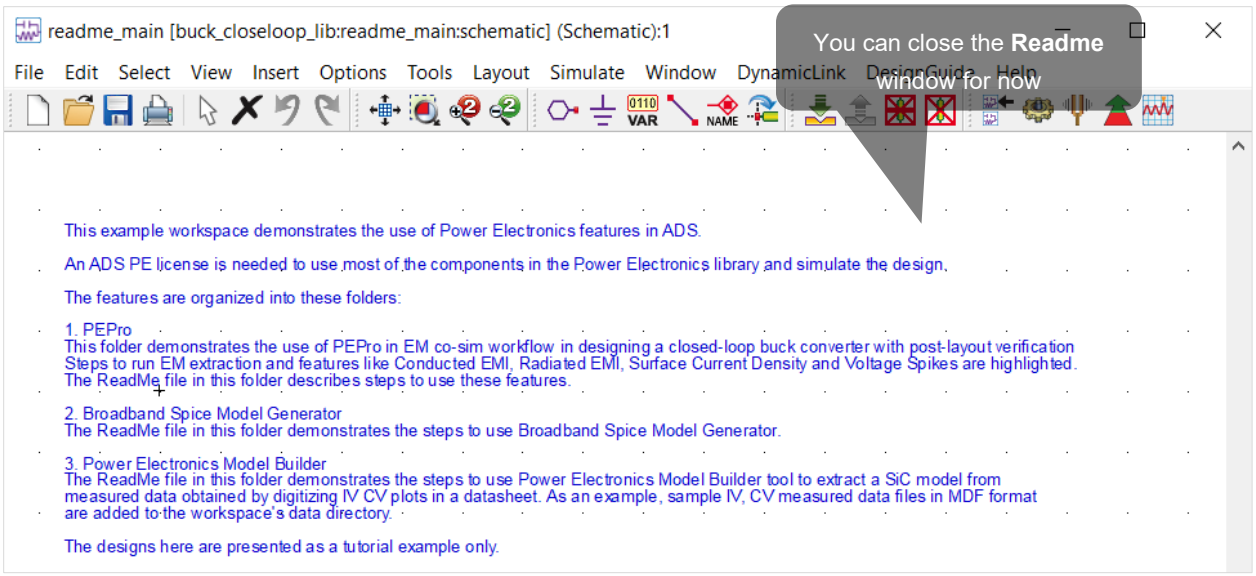


Figure 3. Hierarchical structures of workspace

7. If you open the 01_Readme_Main window, the below description of the content of this workspace.



Simulation of Closed Loop Buck Converter Using PEPro

This example is used to demonstrate the use of PEPro in simulating a closed loop buck converter. A complete simulation flow of using ADS-PEPro in designing a Switched Mode Power Supply (SMPS) can be understood through this example. It contains a component library which includes all the components used in the buck converter design with necessary layout footprints and electrical models. The PCB layout of the buck converter can then be opened in PEPro where the EM model extraction can be done with a few user inputs. Based on the user inputs, proper EM settings will be generated automatically. After the EM model extraction, a post-layout circuit simulation can run to show the impact of PCB layout on the overall module performance.

Multi-Technology in ADS

Workspace, Technology Libraries, Cells, Views

a. A Workspace contains one or more Technology Libraries

Q. Why would you want multiple technologies?

A. For example, chip, package, and board can have their own Technology Library, each with their own namespace, stack up, component library, PDK, etc.

b. A Technology Library contains one or more design units (subcircuits), called Cells.

Q. Why would you want more than one?

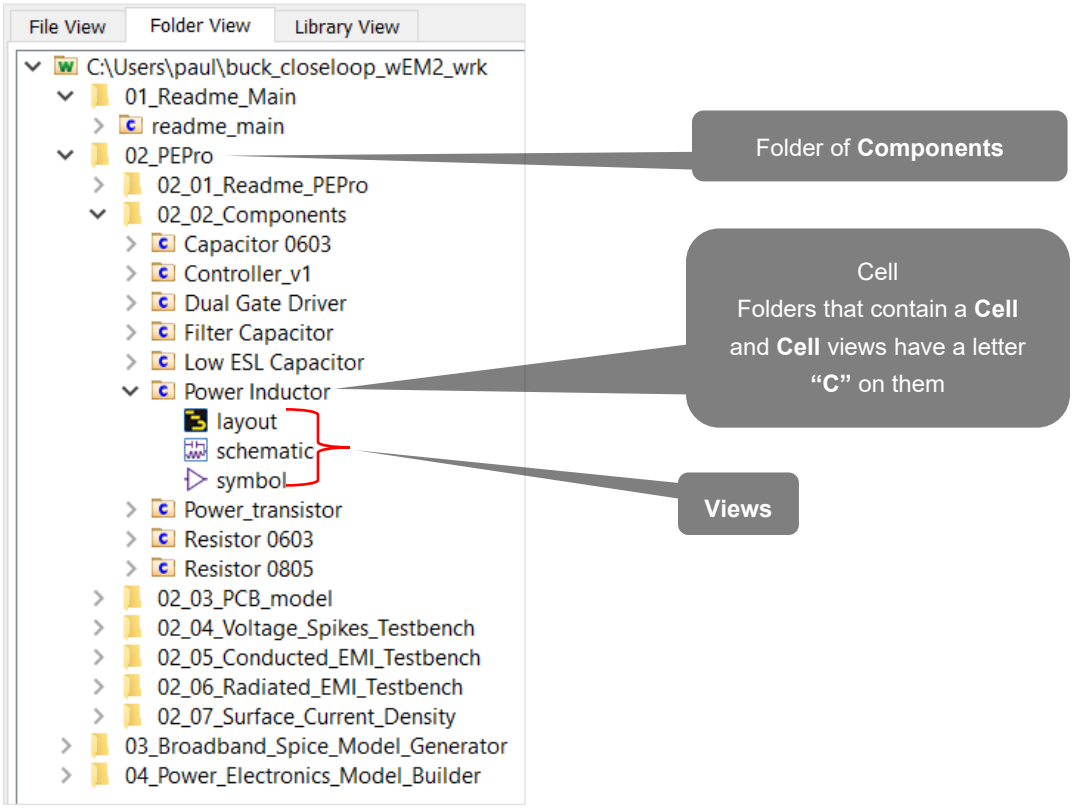
A. You might want hierarchy, for example, subcircuit cells instantiated on a top-level circuit cell. You can even instantiate a cell from one tech. library inside of a cell from another. For example, to place a chip in a package, and a package onto a PCB, just like the real world.

c. A Cell can be viewed in one or more ways, called Views.

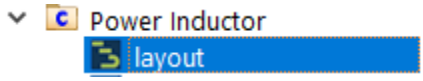
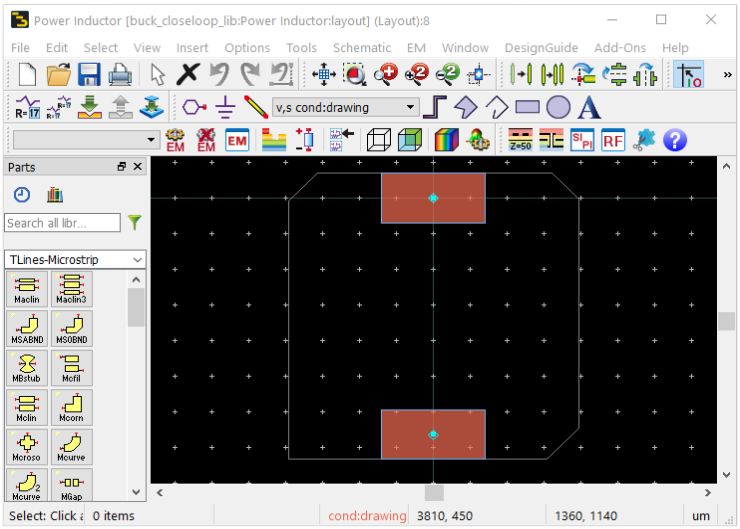
Q. What are the names of some Views?

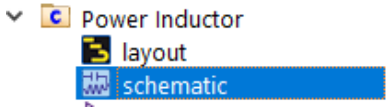
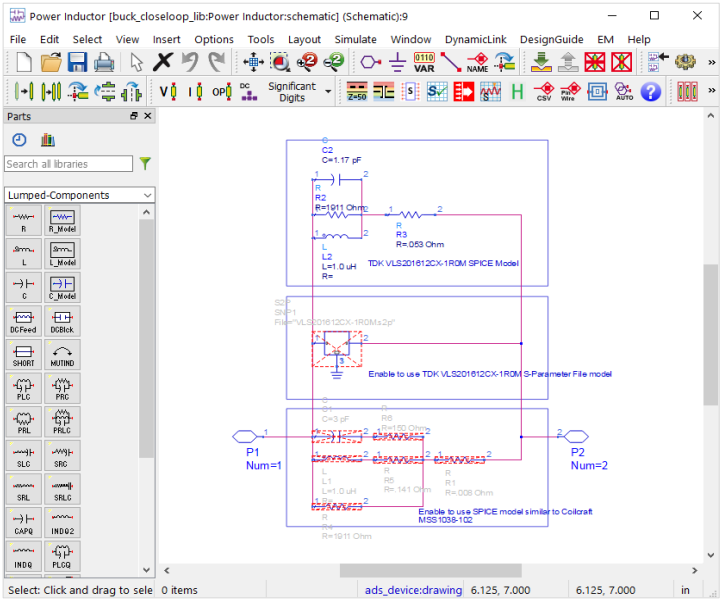
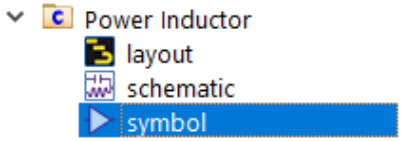
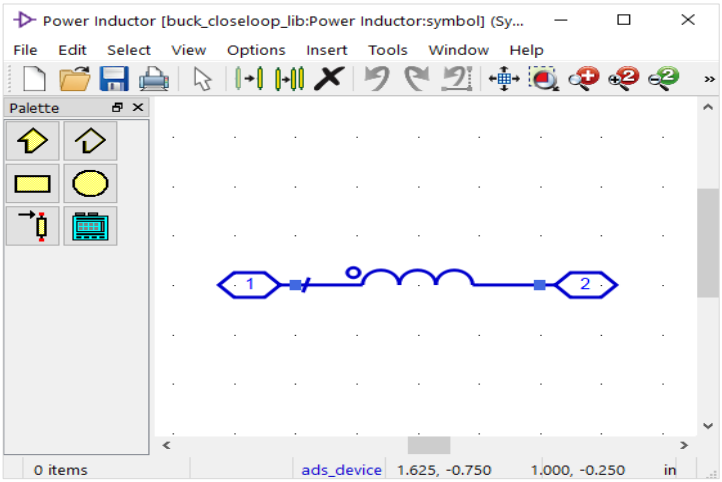
A. The “black box” view is called Symbol view, the circuit view is Schematic, the flat physical view is Layout view, the perspective physical view is called 3D layout view and so on.

Folder of components



For each component you need:

Component	Description
• **Layout** view, which is just a pad or pads with pin(s) on it. 	

Component	Description
• **Schematic** view, you can have different models depending on needs and availability, e.g., models in form of S-parameters data, equations, equivalent circuits made of lumped components etc. 	
• **Symbol** view that represents component(s) in a schematic or layout. 	

The provided schematics and layouts are ready to be simulated. The main design of the closed loop buck converter is in the cell 3 buck_converter_v3.

Double click on schematic view of the buck_converter_v3 cell.

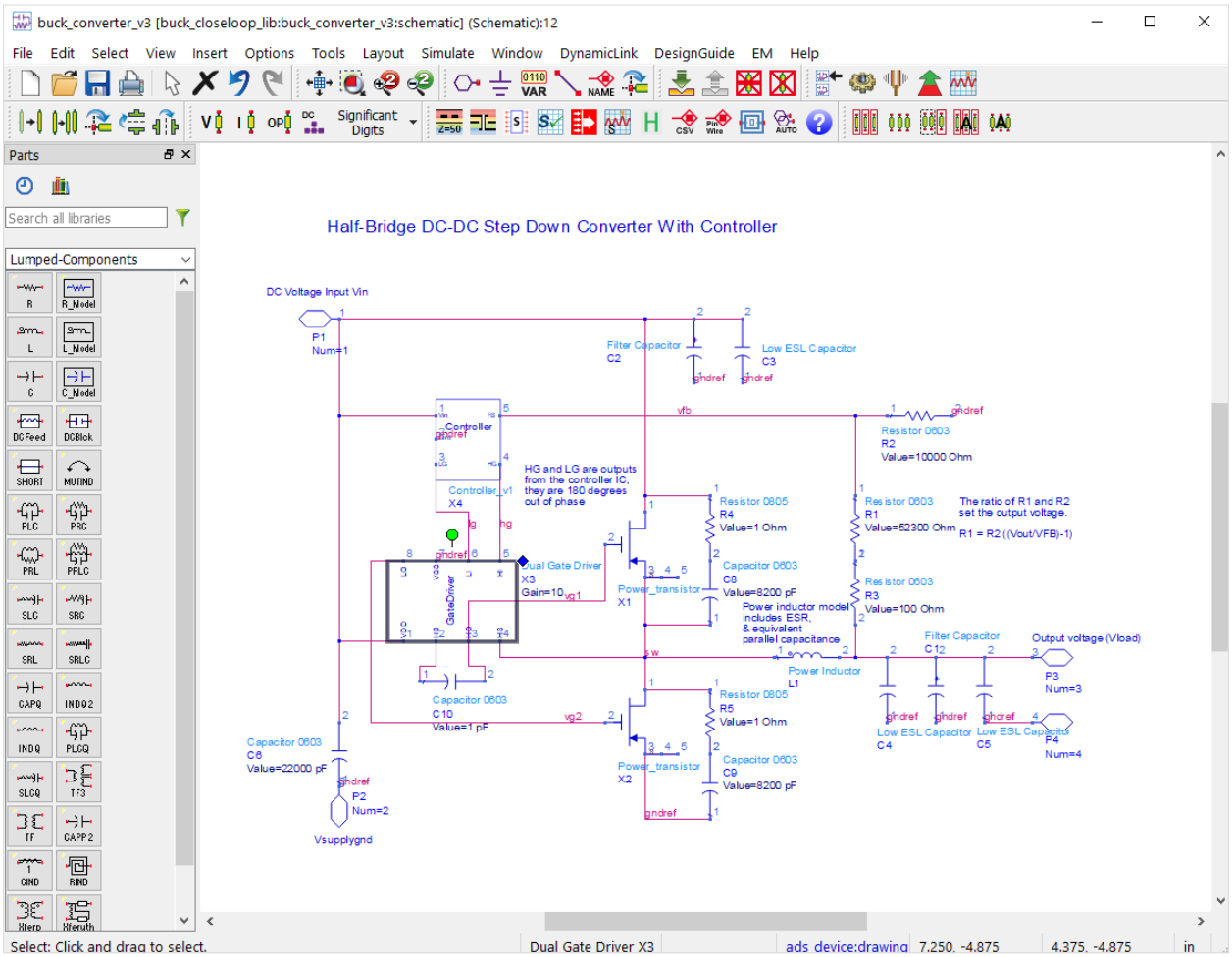
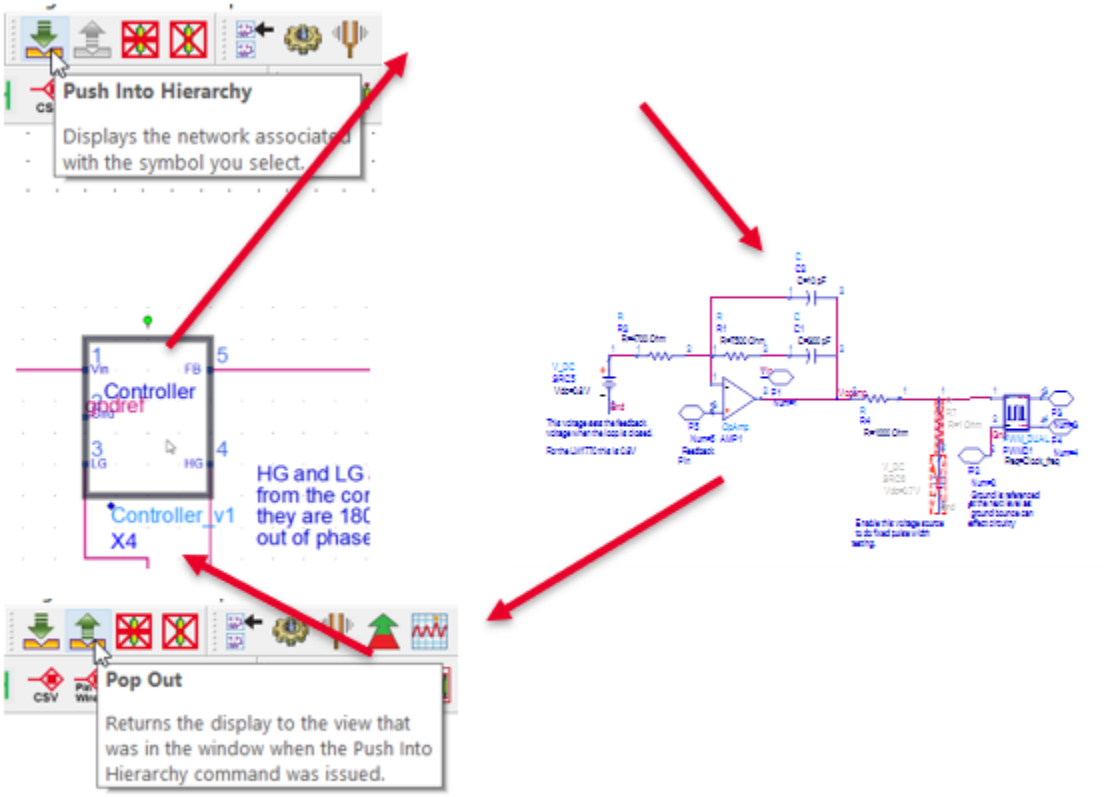


Figure 4. Schematic design of the closed loop buck converter

There is a lot going on here, so maximize the window, and let's take a quick tour…

This view provided a proof-of-concept design using ideal interconnections among all components. Parasitic inductance and capacitance of PCB traces are replaced by ideal connection in this circuit and its result represents the best performance of the design.

To check what is behind every component on the schematic select a component (e.g., Controller, GateDriver or Power Transistor) and Push Into Hierarchy pressing a green arrow icon pointing downwards on the upper tool bar.



To get back to a top-level hierarchy select Pop Out pressing a green arrow icon pointing upwards located next to the previous one.

This is how you can check every component's sub-circuit.

Note: When pushing into hierarchy on a component that has just one hierarchy level ADS will show ERROR Cannot push in.

Double click on layout view of the buck_converter_v3 cell.

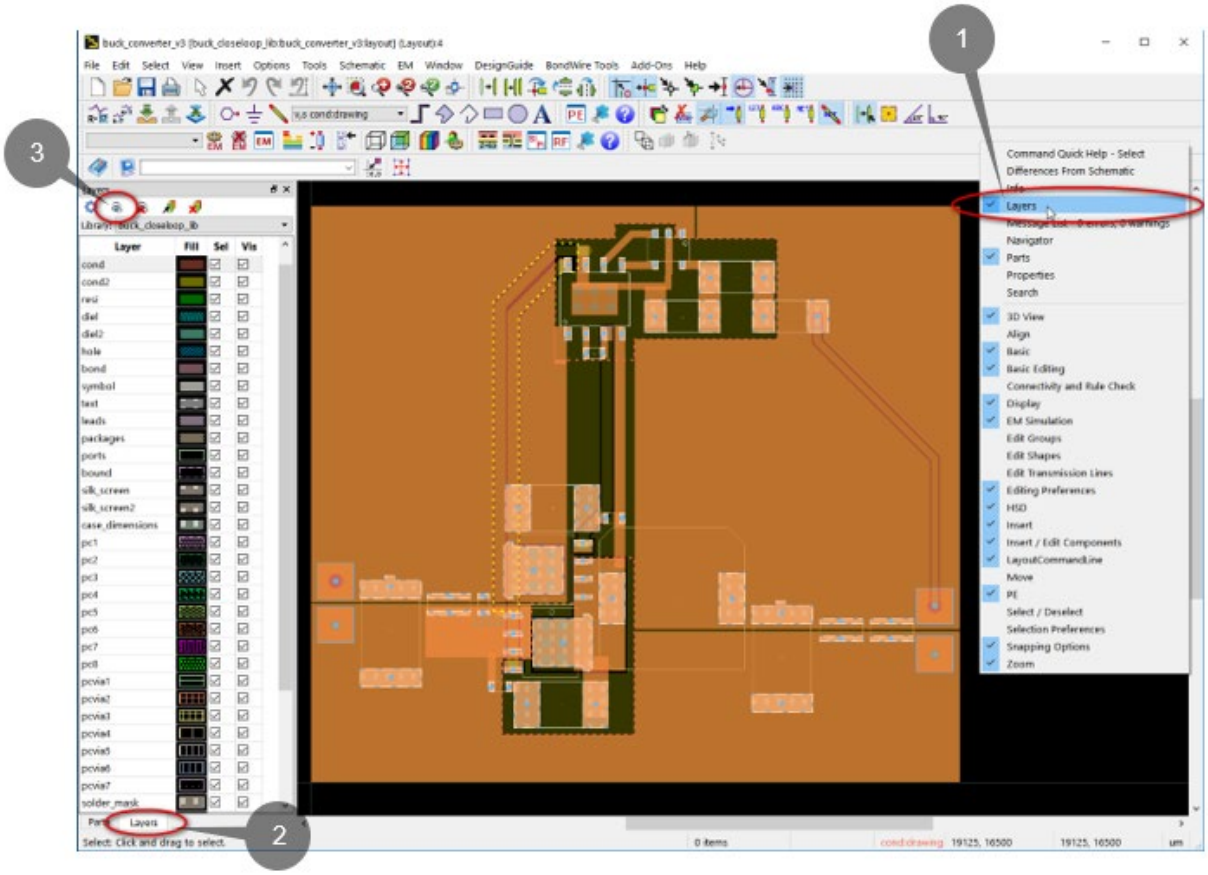


Figure 5. Layout design of the closed loop buck converter

When all layers are not visible right click on upper tool bar field, if not checked then check layers (step 1) select layers tab (step 2) and press Show All Layers icon on top (step 3). This will activate all layers (see Figure 5 Layout design of the closed loop buck converter).

This view provides a possible layout with all the circuit components for this design. It can be then opened in PEPro where an EM model extraction can be performed.

A layout can be designed within ADS or imported from e.g., Allegro, Mentor or other PCB EDA software tools. To import PCB design, make sure imported data files are compliant with ADS accepted formats. ODB++ is a most common format for data exchange among PCB/EDA platforms.

Note: To check other formats or import design go to main ADS window and select: File-> Import -> Design …

The ADS layout window also allows 3D layout visualization. When in a layout window press 3 key to switch to 3D Preview and then press 2 key to get back.

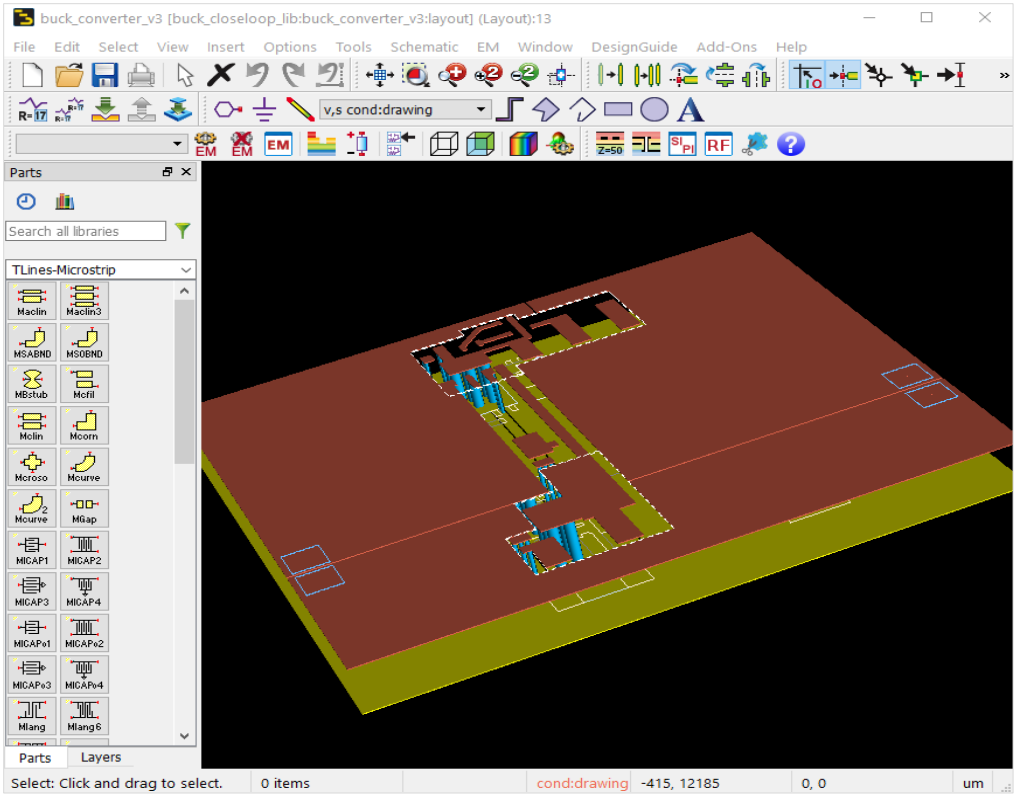


Figure 6. 3D preview of layout design

3D Preview maps geometry drown or imported into the layout window with cross-section of the PCB layer stack specified in the substrate file tech.subst. It can be edited in the substrate editor.

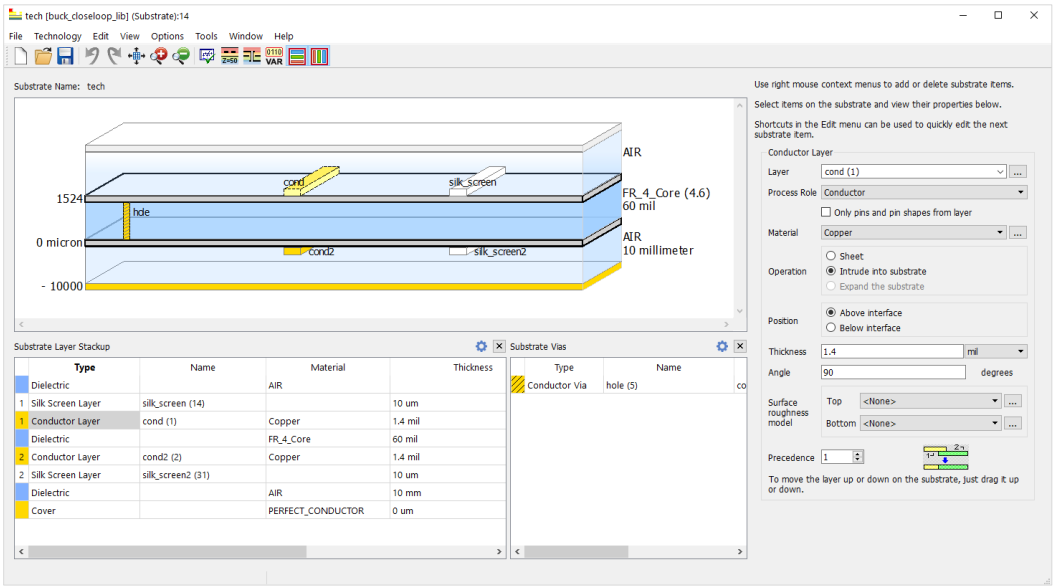
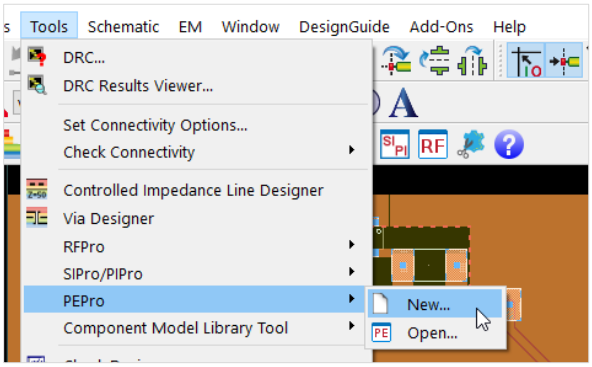


Figure 7. Substrate editor window view

PEPro Setup

In the **layout** window go to **Tools** -> **PEPro** -> **New …**



New PEPro Setup window pops up. Accept default vales and click **OK.**

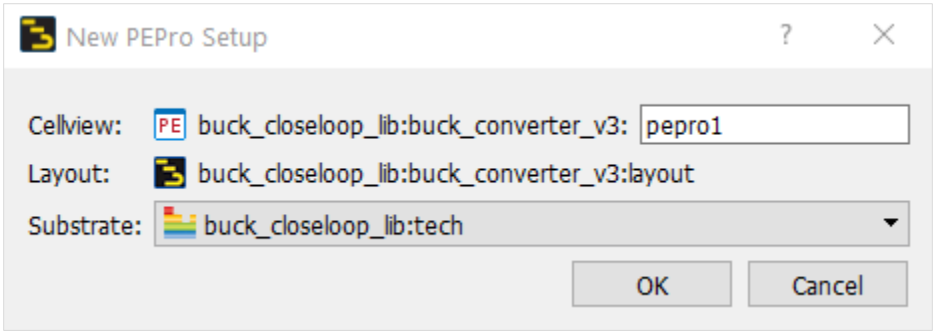
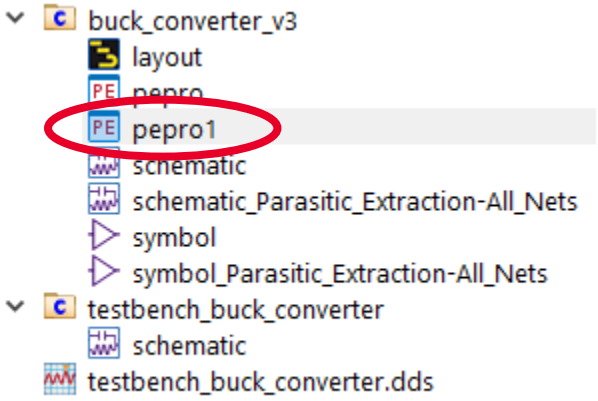


Figure 8. New PEPro Setup window

This will generate a new PEPro setup view instance called **pepro1** (**pepro** is already generated). This view is an integrated EM simulation environment.



PEPro main window opens automatically ready for further setup. See next step.

In the newly opened PEPro main window look at the content of **Project** and **Setup** dockable sub-windows. The **Project** sub-window contains all elements included in the layout i.e., nets, components, pins, etc. The **Setup** sub-window is used for EM analysis of either entire design or only selected nets thus two empty setups **Parasitic Extraction-All Nets** and **Parasitic Extraction-Selected Nets** respectively can be observed.

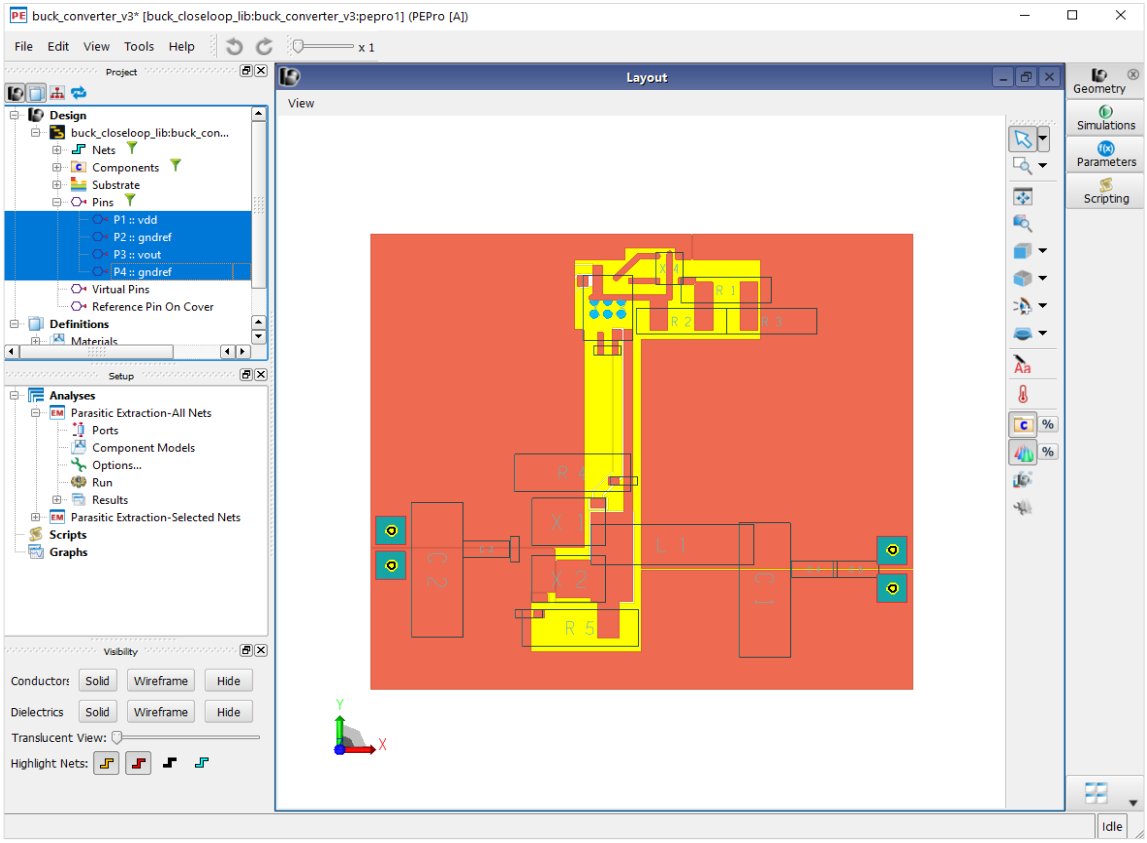
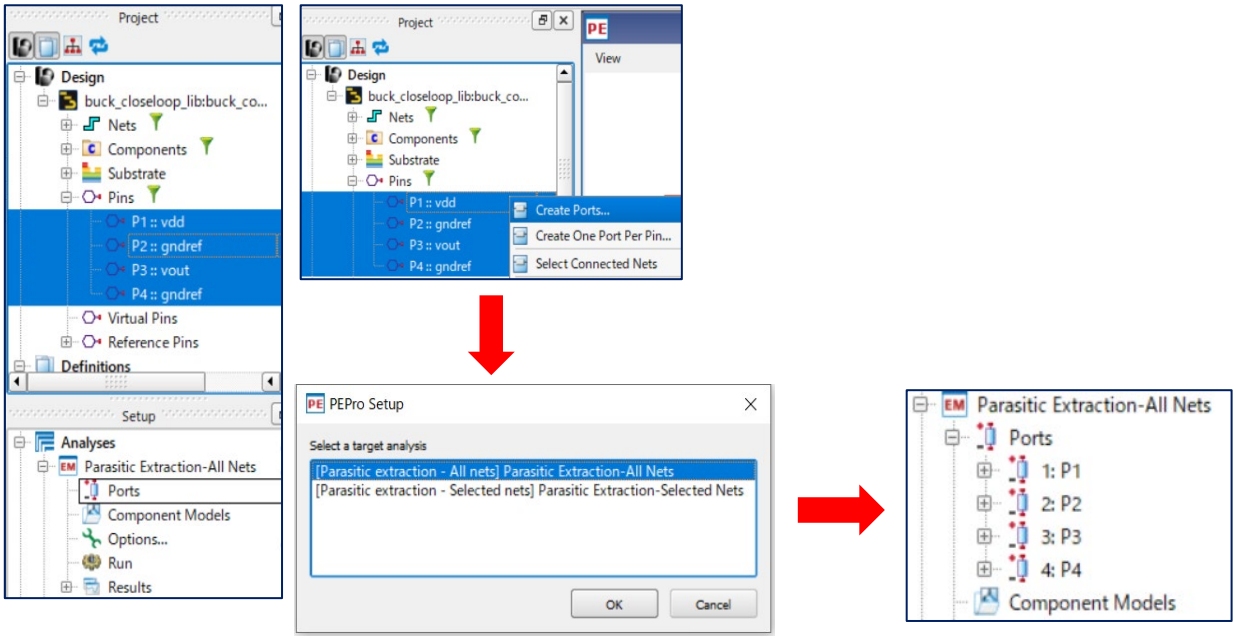


Figure 9. PEPro main window view with the imported layout design

Select all the pins under **Design** -> **Pins** node (see Figure 9 PEPro main window view with the imported layout design), drag them down into **Setup** sub-window and drop onto **Analyses** -> **Parasitic Extraction-All Nets** ->**Ports** node.

Alternatively, select all pins, right click mouse button (RCMB), and chose **Create One Port per Pin**… menu from pop-up window. Then in the **Select a target analysis** window chose desired analysis i.e., **Parasitic Extraction-All Nets**.

Either way will automatically generate ports for each of layout pins referenced to a cover i.e., a reference plane.



The port setup should look like on above right picture.
Note, ground planes in the PCB are floating, they are not connected to a “hard ground” nor reference ground. The reference ground will be an infinite cover indicated in the substrate cross-section as a yellow interface in the bottom.

This cover being an EM reference is conceptually connected to a chassis ground or shield, so this will act as PCB’s chassis – a reference metallization (see Figure 10 Cross-section of the PCB substrate). This also means PCB can’t radiate downwards, i.e., below cover but only upwards above the cover.

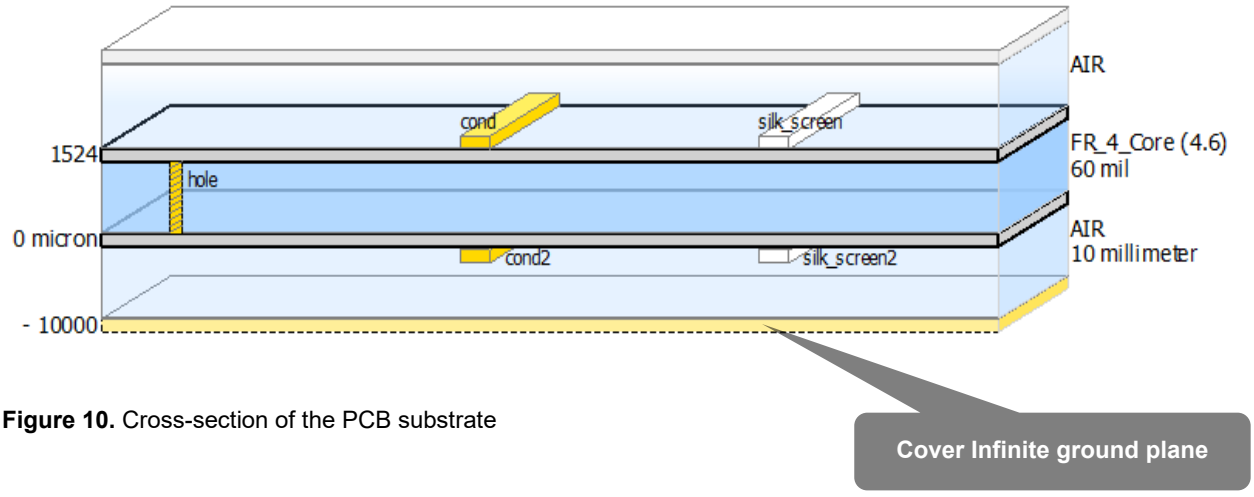
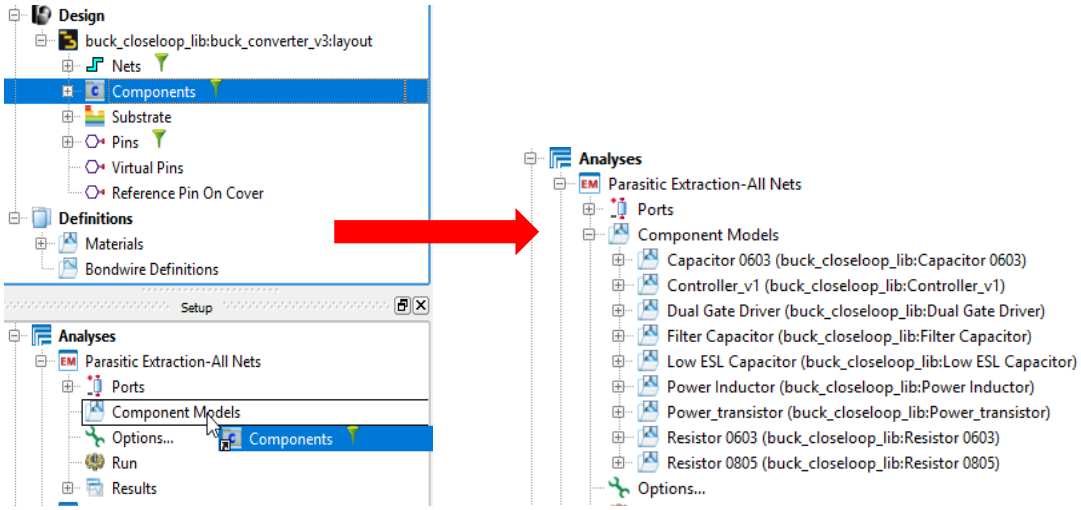


Figure 10. Cross-section of the PCB substrate

Select all the component instances under **Design** -> **Components** node (see picture below), drag them down to **Setup** sub-window and drop onto **Analyses** -> **Parasitic Extraction-All Nets** ->**Component Models** node.

Alternatively, select all components, RCMB and chose **Create Component Models for Analysis** menu from pop-up window. Then in the **Select a target analysis** window chose desired analysis i.e., **Parasitic Extraction-All Nets**.

Either the way will automatically put all the PCB components into **Components Models** branch and set models for each of components' group.



Generally, for each **Component Model** group, you can specify which model must be used for the group and how this component model must be interconnected with the rest of the design.

In this design all of components have its equivalent circuit or schematic model representation thus are not suitable for EM simulation. Due to this fact PEPro will remove them all automatically during EM analysis. They appear again after simulation is completed, i.e., for instance when generating EM model based sub-circuit for Circuit/EM co-simulation.

Expand **Design** ->…->**Nets** node and double check **sw** net is colored in orange. If not, then select the **sw** net and RCMB and chose **Set as Switching** (see Figure 3 PEPro setting switching nets). From now this net will be considered as **Switching**, all the pins on which will be plotted automatically after simulation. If none of the net is set as **Switching** net, when you double click **Generate Voltage Spike Test Bench** under Results, a message window will be displayed. Then, if you do not want to set any net as **Switching** net to display plots, click **Yes** to proceed with testbench generation. If you want to generate display plots for pins on certain nets, click **No**, then set the **Switching** net type as described above.

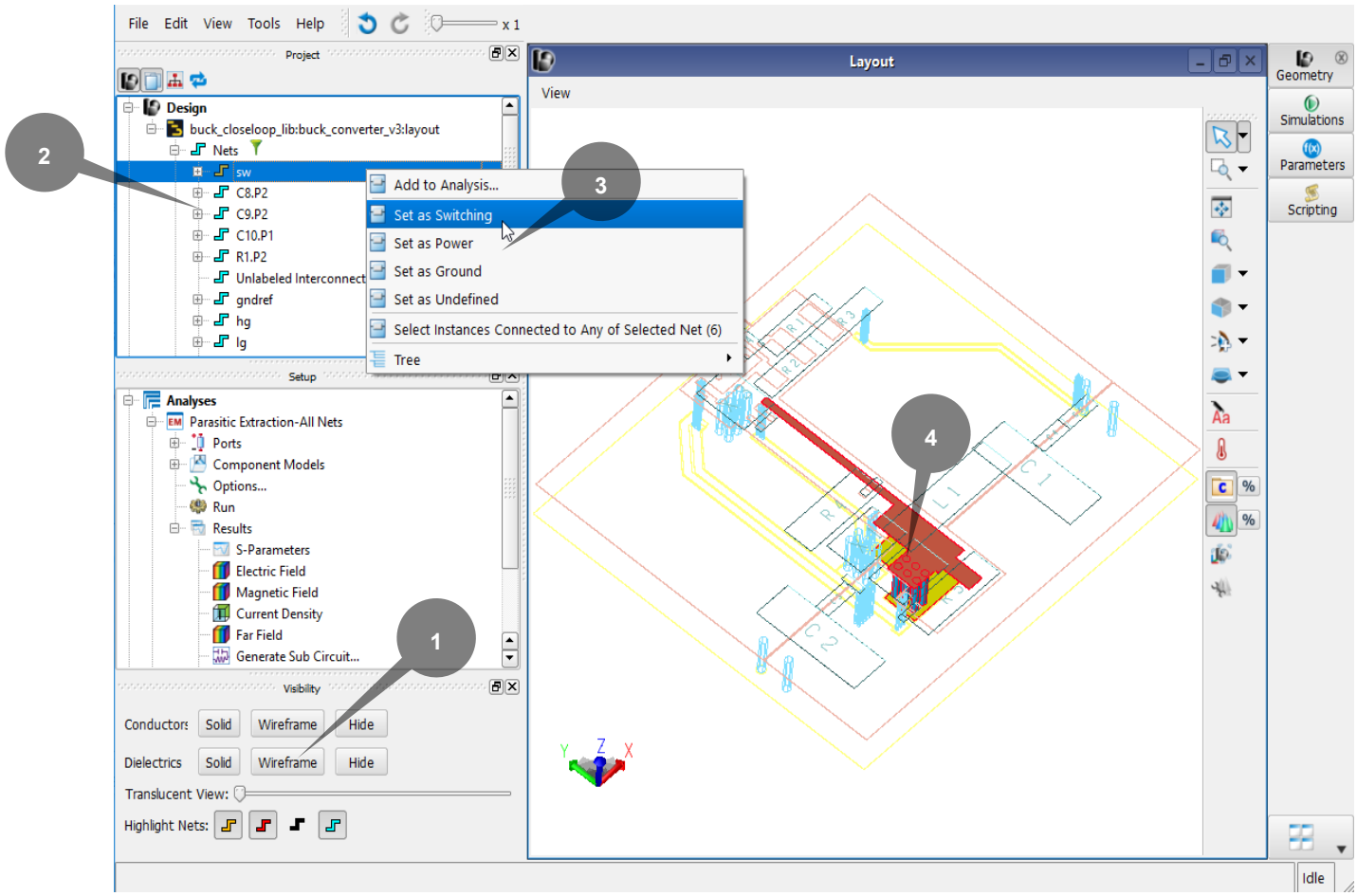


Figure 11. PEPro setting switching nets

Make sure PEPro setup is saved thus in the PEPro main window got to **File** -> **Save.**

Next, expand the analysis of **Parasitic Extraction-All Nets**, double-click **Options…** and open the page of **Frequency Plans**, the tab of **Frequencies** (see Figure 4 PEPro - Options window of a selected Analyses setup).

There are several types of frequency sweeps. For switched mode power converters, we use an automatic frequency plan for switched-mode power supplies (SMPS) in Power Electronics. It creates a composite frequency plan that can capture the most important EM features of a PCB in SMPS circuits. To use this plan, the user needs to provide circuit characteristics in the frequency plan table. Once the required input data is set, the frequency plan will be generated automatically and used in the subsequent EM simulation.

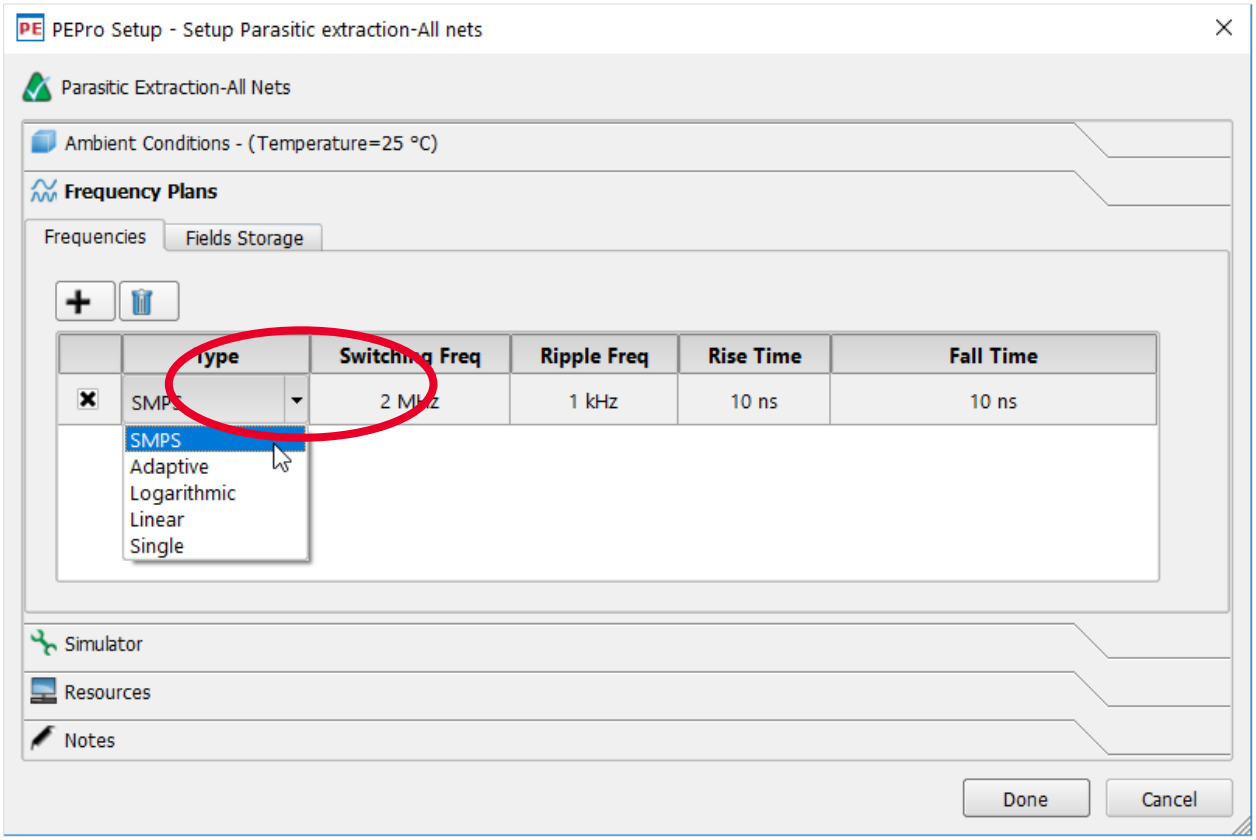


Figure 12. PEPro - Options window of a selected Analyses setup

For this exercise make sure all the **SMPS** parameters (**Switching Freq**, **Ripple Freq**, **Rise Time**, **Fall Time**) have values as depicted in Figure 4 PEPro - Options window of a selected Analyses setup. These parameters are applicable only to SMPS frequency plan type.

In result, for above parameters PEPro will automatically generate following frequency plans:

Linear sweep from 0 MHz to 0.001 MHz with 6 points (step = 0.0002 MHz)

Linear sweep from 0.001 MHz to 0.01 MHz with 10 points (step = 0.001 MHz)

Logarithmic sweep from 0.01 MHz to 2 MHz with 13 points (5 points/decade)

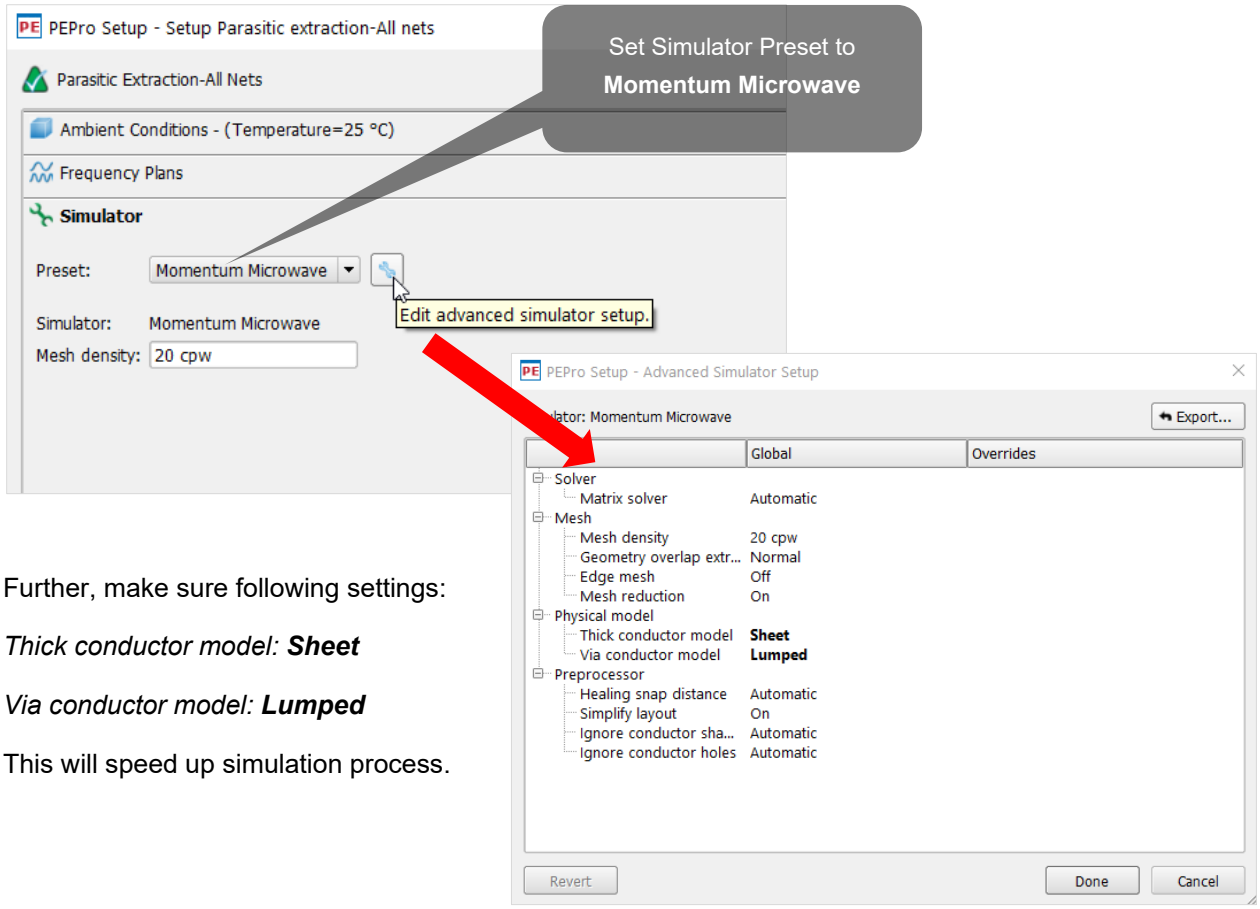
Linear sweep from 2 MHz to 80 MHz with 40 points (step = 2 MHz)

Logarithmic sweep from 80 MHz to 500 MHz with 17 points (20 points/decade)

If necessary, more frequency plans can be added manually in parallel.

Note, SMPS frequency plan parameters are used to automatically configure optimum simulation settings in the generated test benches and to automate the result presentations in the data display window. If the SMPS frequency plan is not used, these parameters are not available to the generated test benches and the user needs to manually set the necessary parameters before launching a simulation.

In the same PEPro Setup Options window go to Simulator page and enter Advance Simulator Setup window.



Further, make sure following settings:

Thick conductor model: ***Sheet***

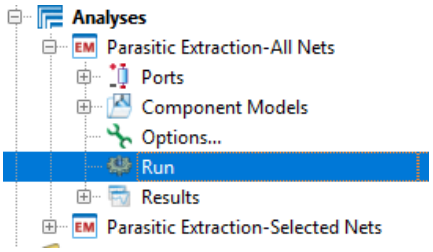
Via conductor model: ***Lumped***

This will speed up simulation process.

Look at rest of the default settings and quit the **Advance Simulator Setup**/**Options** window by pressing **Done**.

To save setup go to **File** -> **Save.**

If necessary, expand the analysis of **Parasitic Extraction-All Nets** and double-click **Run** to start the EM simulation.



The simulation progress can be observed in **Simulations** window. Press **Simulations** button located on the right-hand side PEPro frame (see Figure 5 Simulations window – simulation in progress).

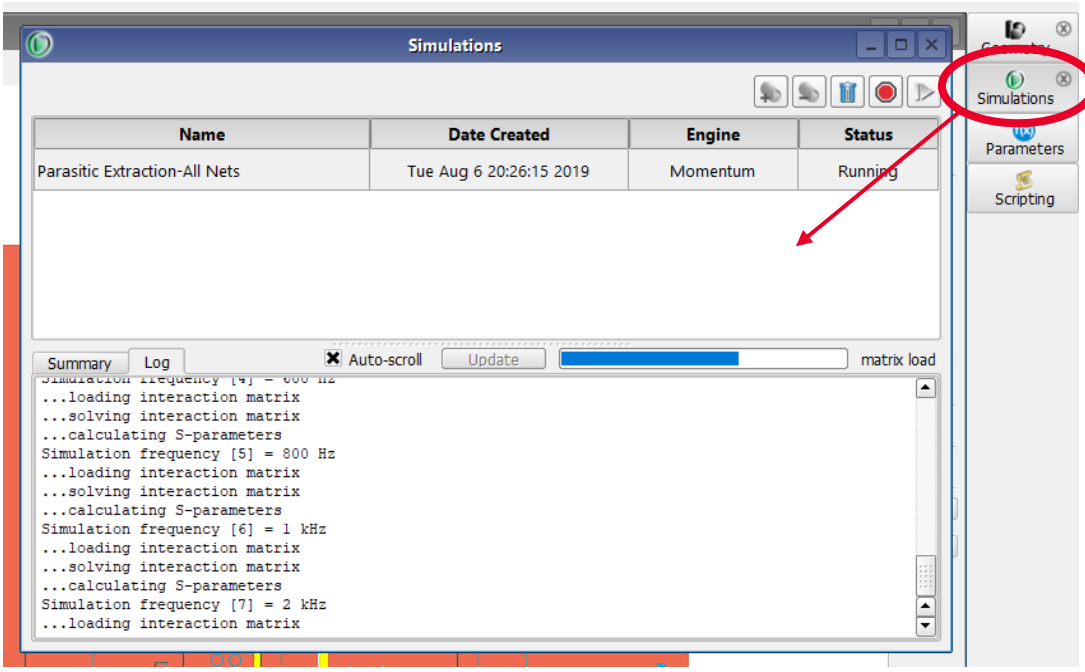


Figure 13. Simulations window – simulation in progress

The simulation will take several minutes depending on available computation resources. When completed close the **Simulations** window.

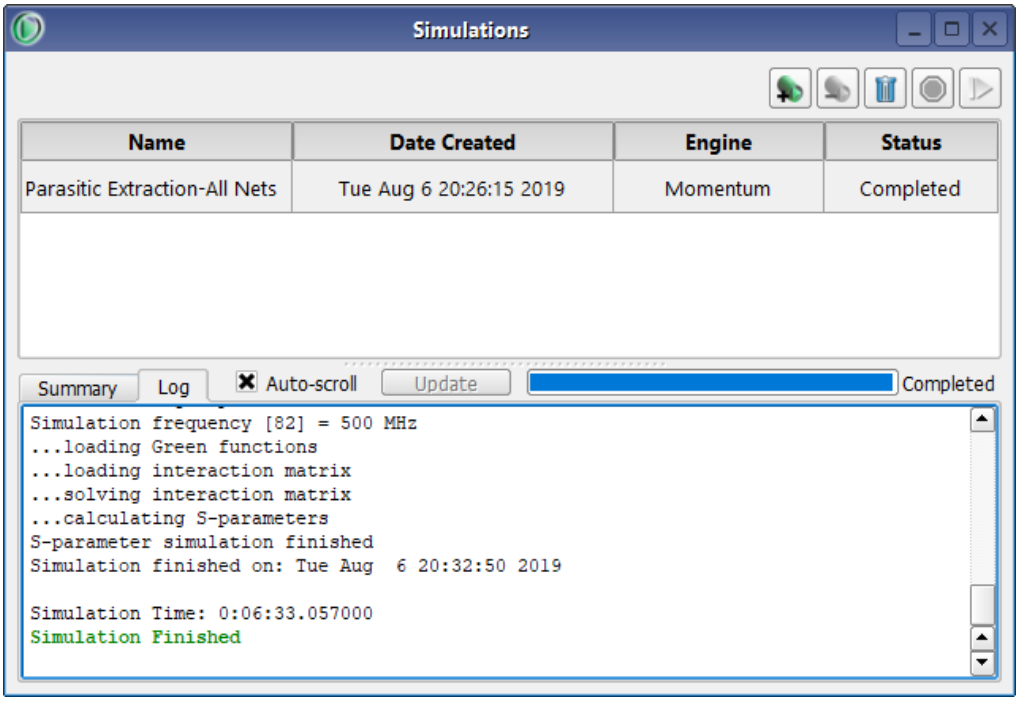
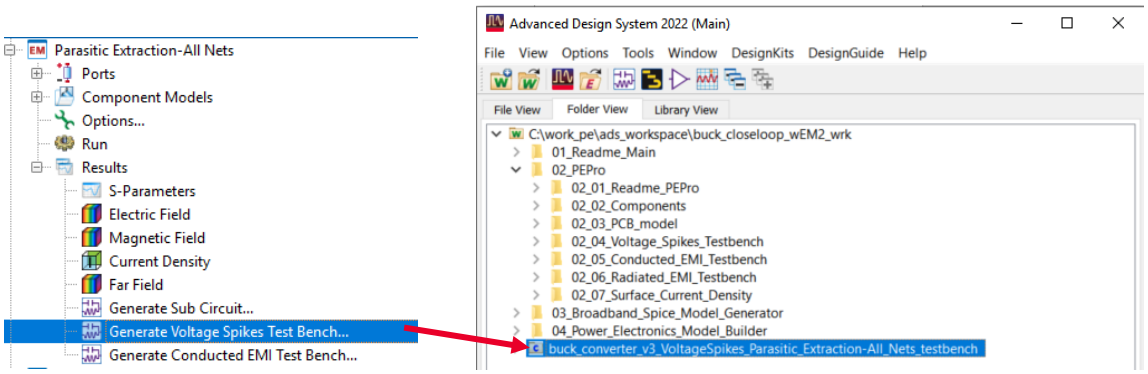


Figure 14. Simulations window – simulation completed

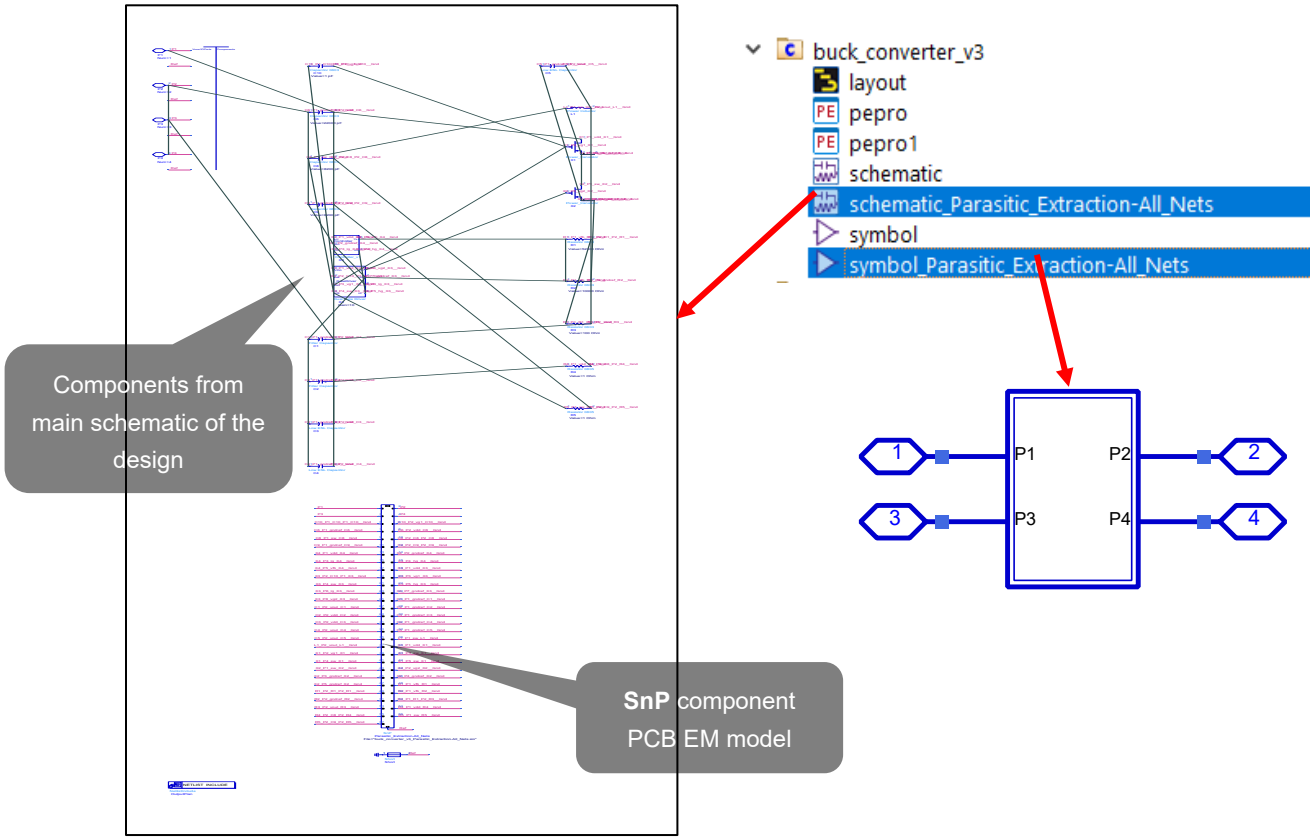
Voltage Spikes Test Bench

Now let's see how to use EM simulation results in a circuit analysis. First, expand **Results** node and double-click on **Generate Voltage Spikes Test Bench**.



This generates a new cell in the workspace with a name according to following syntax: <*original-cell-name*_**VoltageSpikes**_*PEPro-analysis-name*_**testbench**>. So, in our case it is **buck_converter_v3_VoltageSpikes_Parasitic_Extraction-All_Nets_testbench**.

Further, above action generates also two additional important views under buck_converter_v3 cell: schematic_Parasitic_Extraction-All_Nets and symbol_Parasitic_Extraction-All_Nets.



To see more details, open **schematic_Parasitic_Extraction-All_Nets** view and look what's inside. There you

can observe all design components connected without wires. Instead, node names are used to connect appropriate component pins. Flight lines (doted-dashed thin lines) symbolically indicate original schematic connections network.

Further, there is also one significant **SnP** component with 58 pins including reference pin (**Ref**). This is design's PCB electromagnetic model built by PEPro and appropriately connected by node names with components above. This EM model, with scattering parameters behind, represents parasitic effects in PCB

In the ADS main window expand **buck_converter_v3_VoltageSpikes_Parasitic_Extraction-All_Nets_testbench** cell and open schematic view. This is a test bench used to simulate the post-layout circuit performance, particularly the voltage spikes appearing in the design during a normal startup condition (see Figure 7 Voltage Spike Analysis testbench).

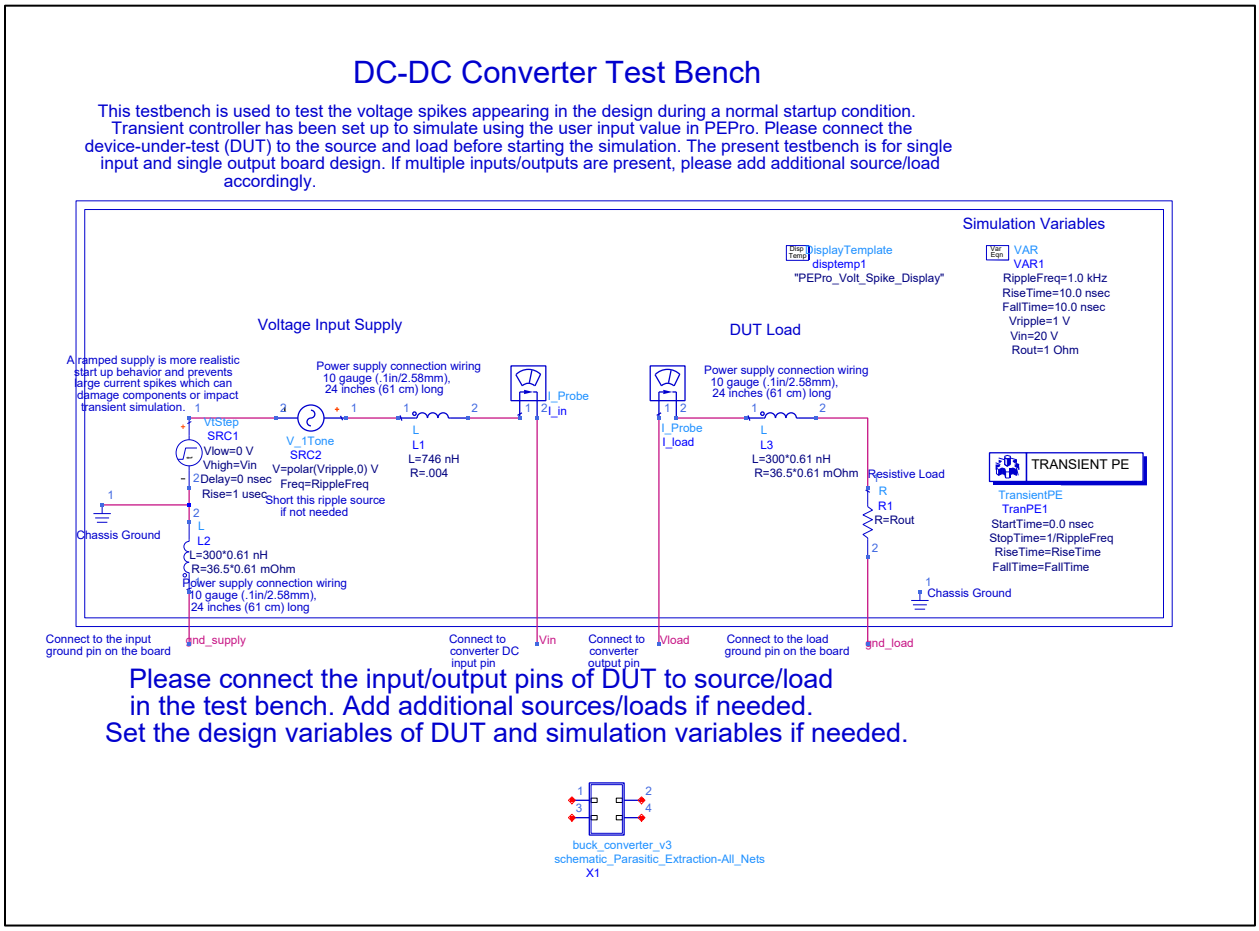
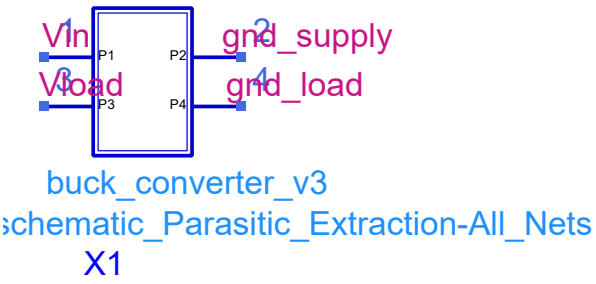


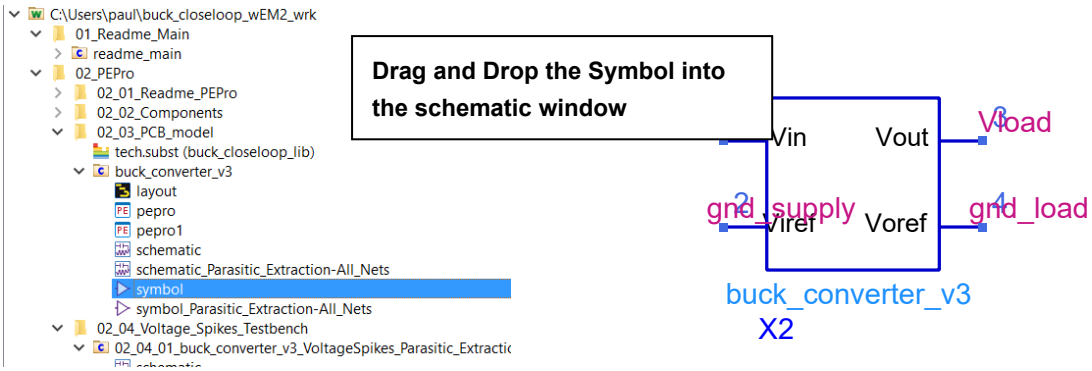
Figure 15. Voltage Spike Analysis testbench

As it states in the schematic description, our DUT, i.e., **buck_converter_v3** component, automatically placed during testbench generation, needs to be connect to the **source** and **load** of the testbench. To do that in the schematic window go to **Insert -> Wire/Pin Label …** and select a pin number 1 of the **buck_converter_v3** component then type net name **Vin** in the edit field attached to a selected pin and press **Enter**. Proceed in the same way for rest of the pins to get final labeling as depicted below. When finished press **Esc** to exit from the node labeling mode in the schematic.

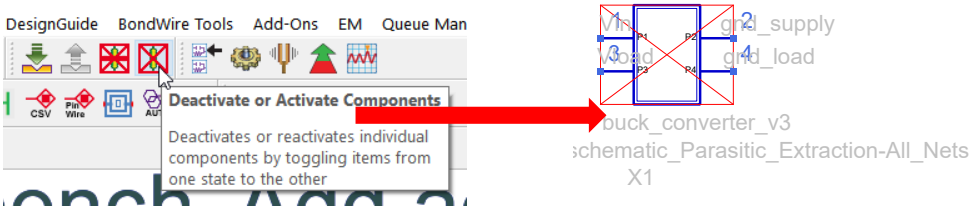


Now we are ready for a transient simulation of the converter represented by the interconnected schematic and EM model circuit. But before that, let's check electrical performance when the converter is modeled only by ideally connected components as depicted in buck_converter_v3 schematic.

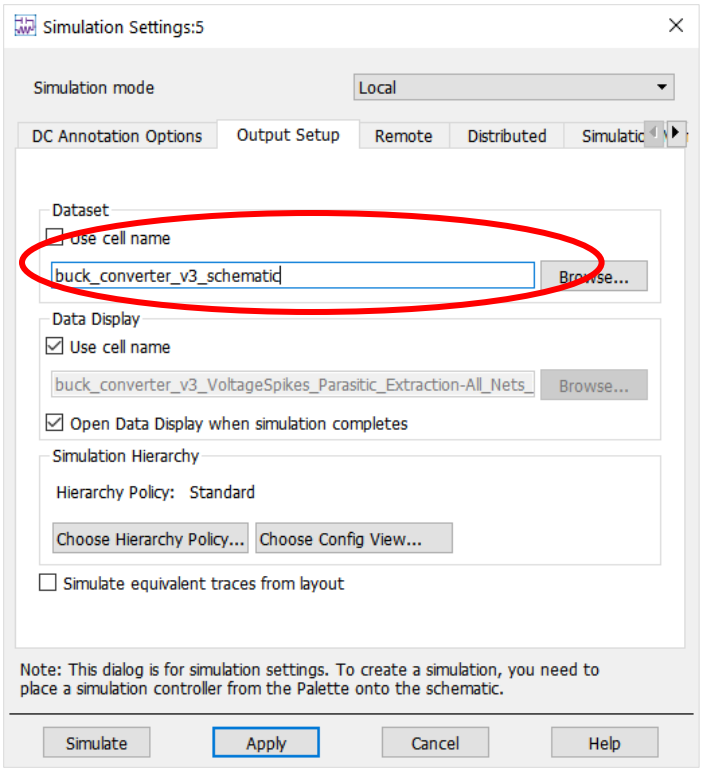
Now drag and drop the **schematic** view of the **buck_converter_v3** into the **schematic** view of **buck_converter_v3_VoltageSpikes_Parasitic_Extraction-All_Nets_testbench** cell and make a proper pin net name assignment as below:



Then make sure the **X1** earlier placed component is deactivated as below:



As a next step go to **Simulate** -> **Simulation Settings** and uncheck **Use cell name** box under **Dataset** field. Then change dataset name to **buck_converter_v3_schematic**



Now press **Apply** and further **Simulate** or **F7**. Alternatively go to **Simulate** -> **Simulate** or press corresponding icon on the tool bar to launch circuit simulation.

When simulation is finished the **DataDisplay** (**DD**)window will pop-up. But let's skip this template for now and see the input and output voltage waveforms.

In **DD** window:

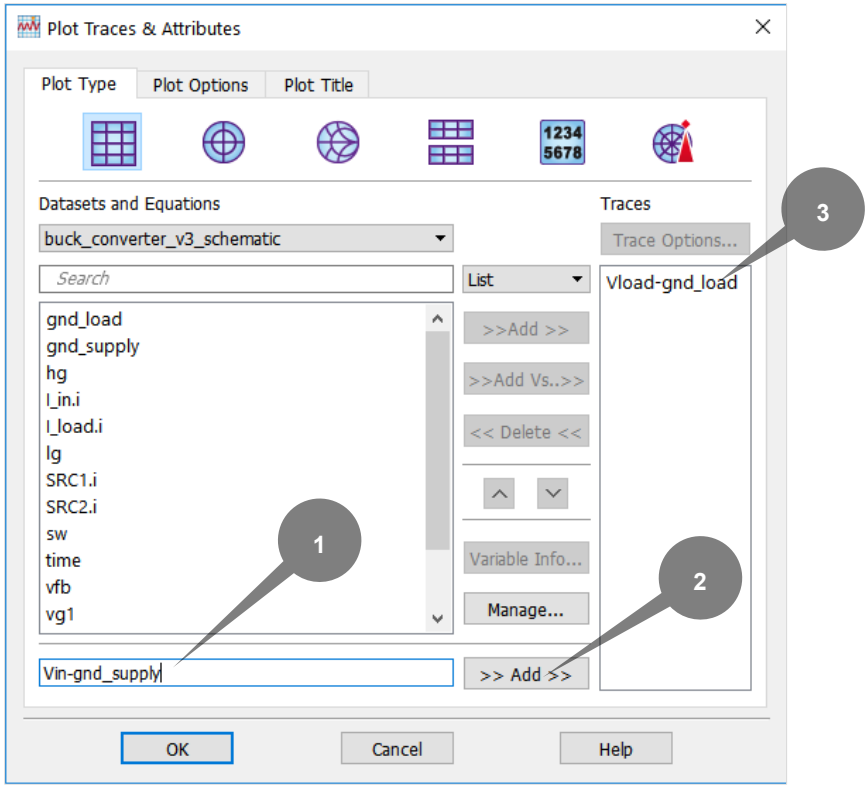
Go to **Page->New Page** and accept default name.

Select Rectangular Plot icon under Palette window and place empty frame on **DD**'s area. **Plot Trace & Attributes** window will open.

In the left bottom ***Enter any Equation*** field type **Vload-gnd_load** equation and press **Add** button next to this entry field. The equation should appear in the right window.

Do as in **@c** and type **Vin-gnd_supply** equation.

When finished press **OK.**



Now a graph with input (blue line) and output (red line) voltage at the buck converter with EM model is shown (see Figure 9 Input & output voltage waveforms). The input ripple and switching noises are suppressed in the output waveform.

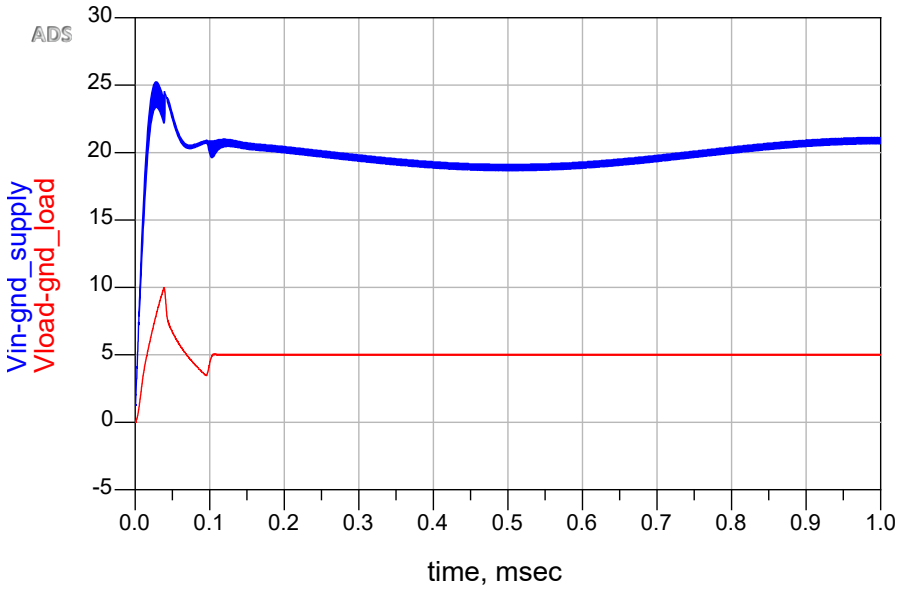


Figure 16. Input & output voltage waveforms

As it can be observed the output voltage **Vload** stabilizes within 0.1ms and settles at 5V further on.

To see a waveform at the switching node inside the converter open another rectangular graph and select **sw** node.

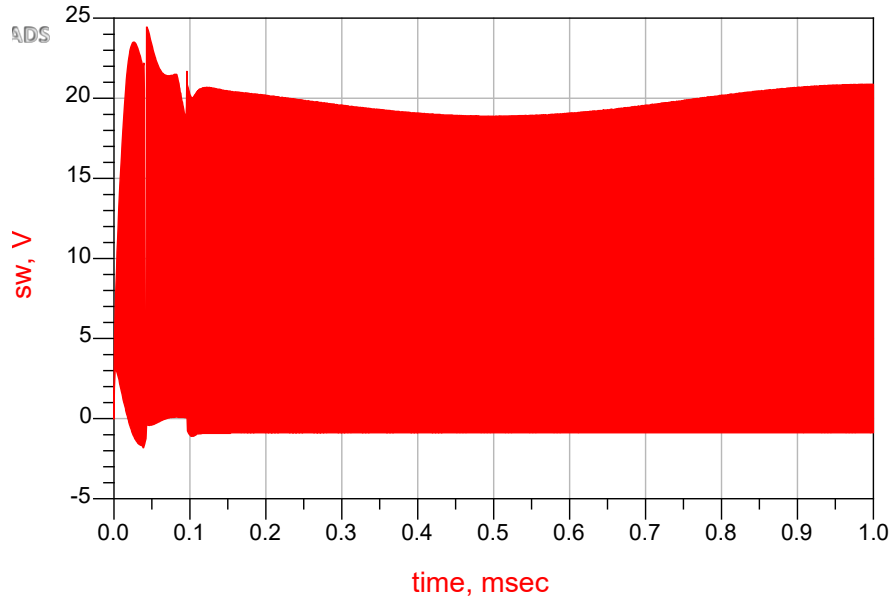
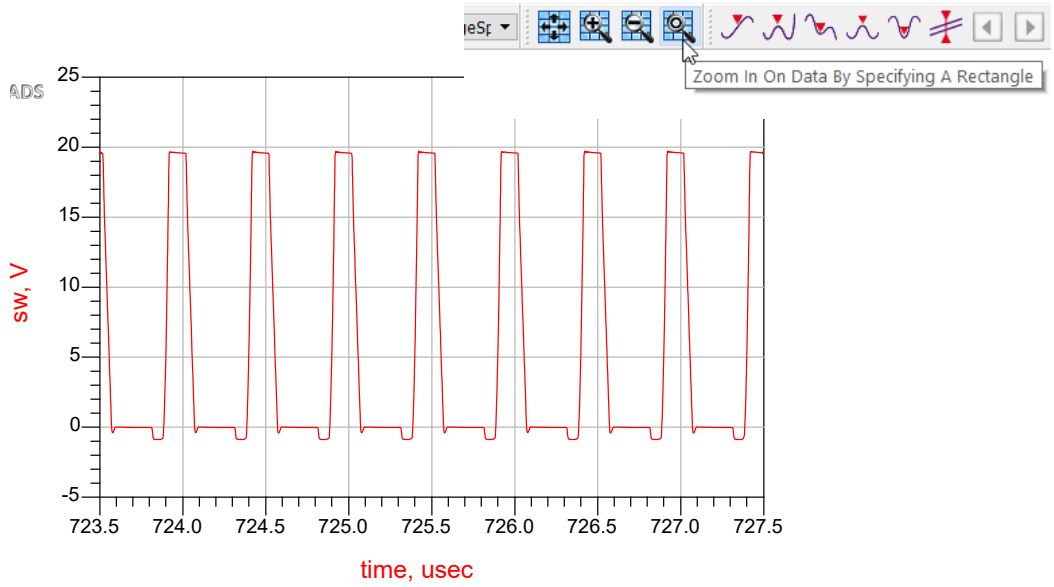


Figure 17. Waveform at the switching node inside the converter

Use **Zoom In On Data By Specifying A Rectangle** function on the selected graph to see more details within selected time period.

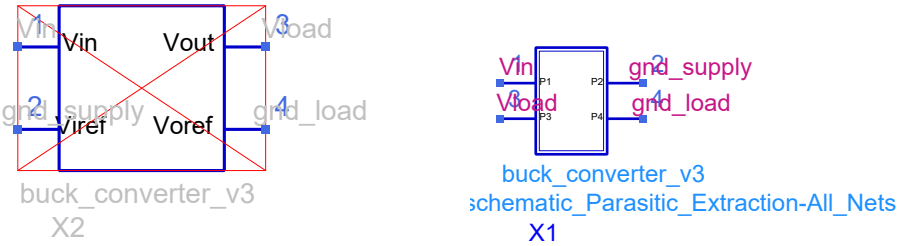


Save **DD** with a default name and close it.

Next let's see the effect of layout parasitics on ripple…

Go to (open) the **schematic** view of the **buck_converter_v3_VoltageSpikes_Parasitic_Extraction-All_Nets_testbench** cell. To speed-up the simulation and limit size of generated dataset, adjust **TransientPE** controller parameters as following: **StopTime = 0.12/RippleFreq**

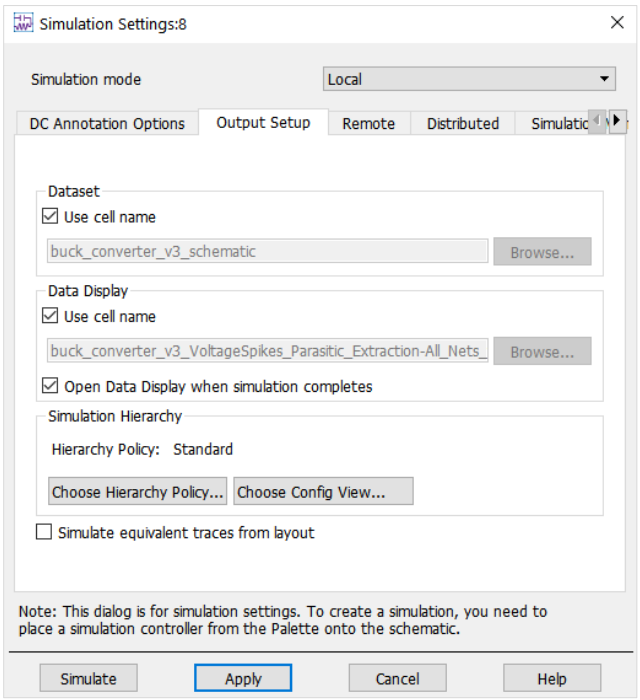
Now make sure the X2 component is de-activated and X1 is activated:



Open **Simulate** -> **Simulation Settings** and check **Use cell name** box under **Dataset** field. This time Transient simulation will generate a dataset with a name of the opened schematic view, i.e. **buck_converter_v3_VoltageSpikes_Parasitic_Extraction-All_Nets_testbench**

Now press **Apply** and further **Simulate** or **F7**.

This time the simulation will take longer and will provide the results considering parasitic effects in PCB.



When simulation is finished the **DataDisplay** window will pop-up showing simulation results in **PEPro_Volt_Spike_Display** template. Press **Yes** if asked for a default dataset.

All pins under the nets that have been assigned the net attribute as Switching will be plotted in the data display automatically.

View Last N Cycles: There is an equation, called **lastNCycles** with a default value of 2. This value controls the last **n** number of cycles displayed in the generated plots.

First Peak Marker: Marker is positioned at the first peak. With baseline marker as the reference and with delta mode on, the first peak marker shows the difference in the dependent values.

Second Peak Marker: Marker is positioned at the second peak. With first peak marker as the reference and with delta mode on, the first peak marker shows the difference in the independent values. This gives the value of the ringing period.

Baseline Marker: Marker is positioned at the baseline.

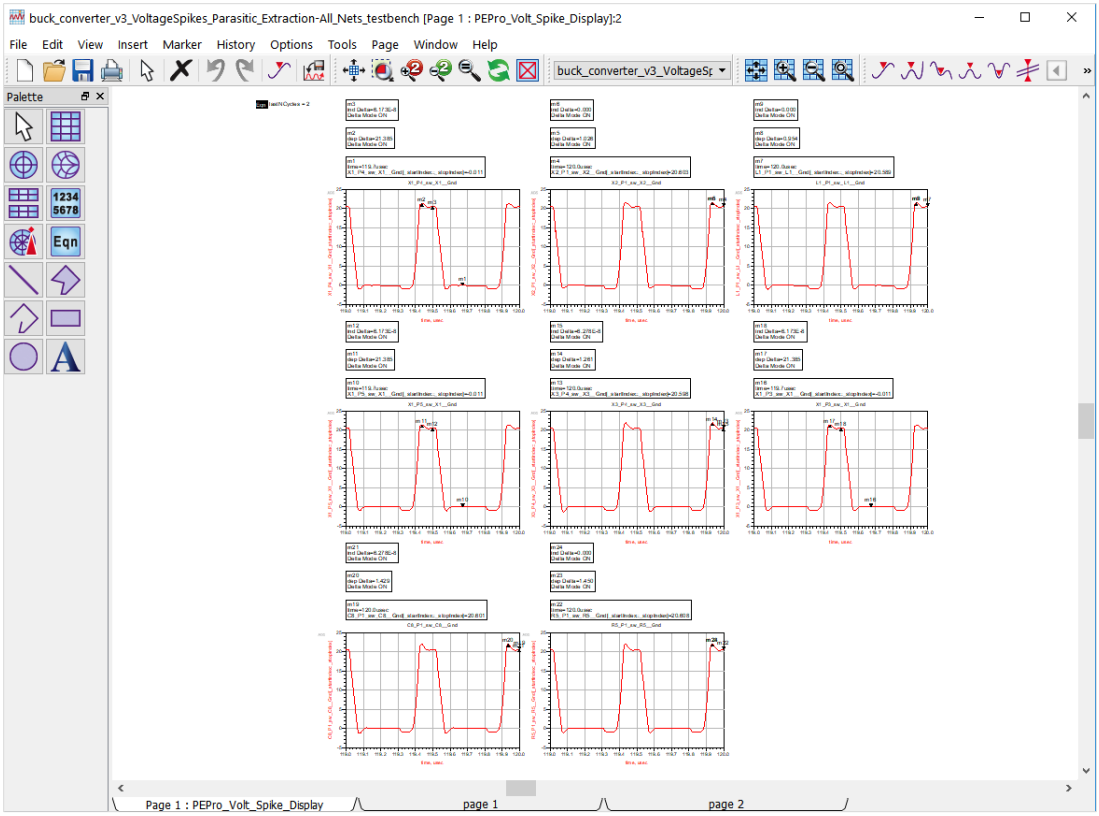
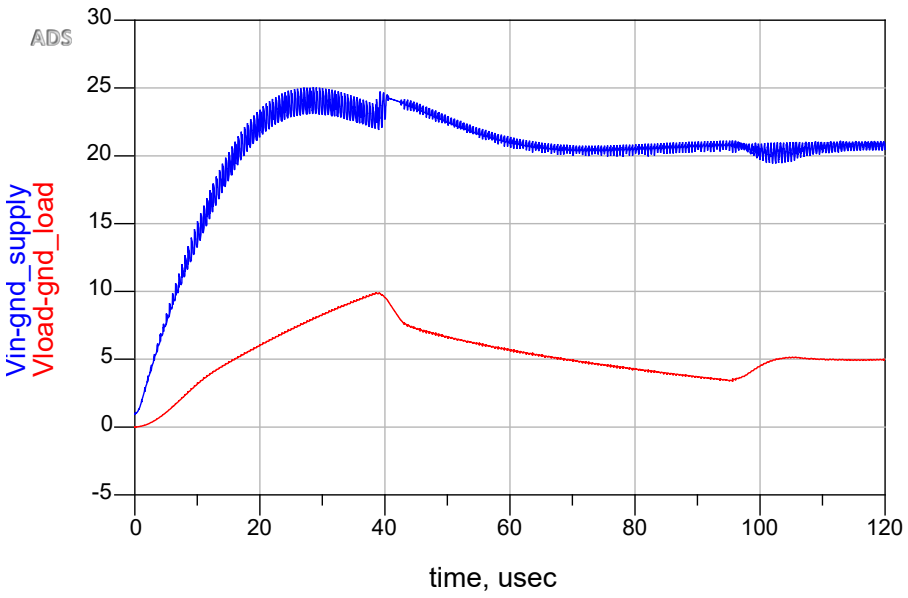


Figure 18. DataDisplay window - Voltage Spike Template

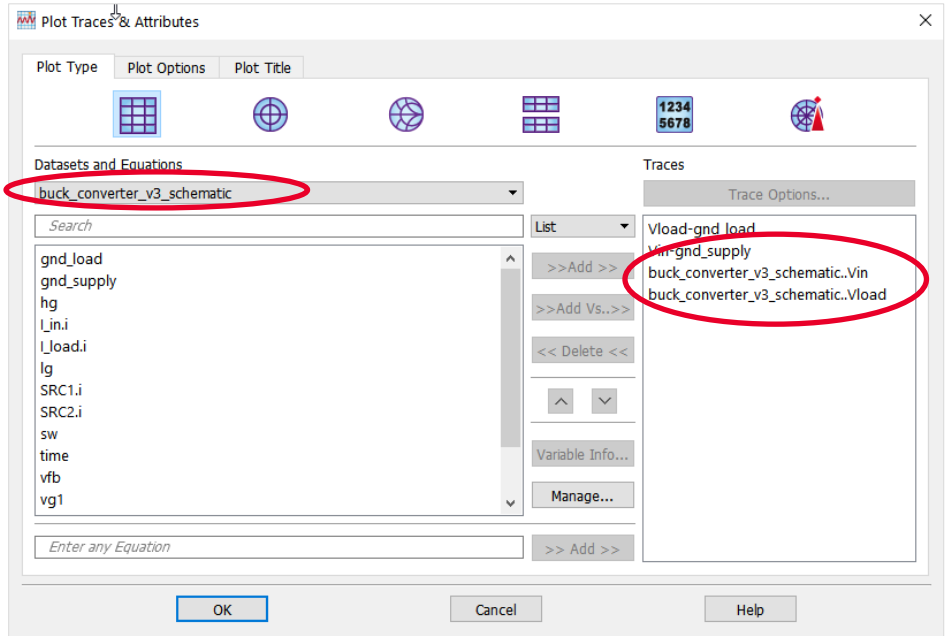
But let's skip this template for now and see the input and output voltage waveforms. For that we can use the same **DataDisplay** window as on Figure 18 DataDisplay window - Voltage Spike Template.

In **DataDisplay** (**DD**) window:

Go to **Page->page2** and now you should see following plot:

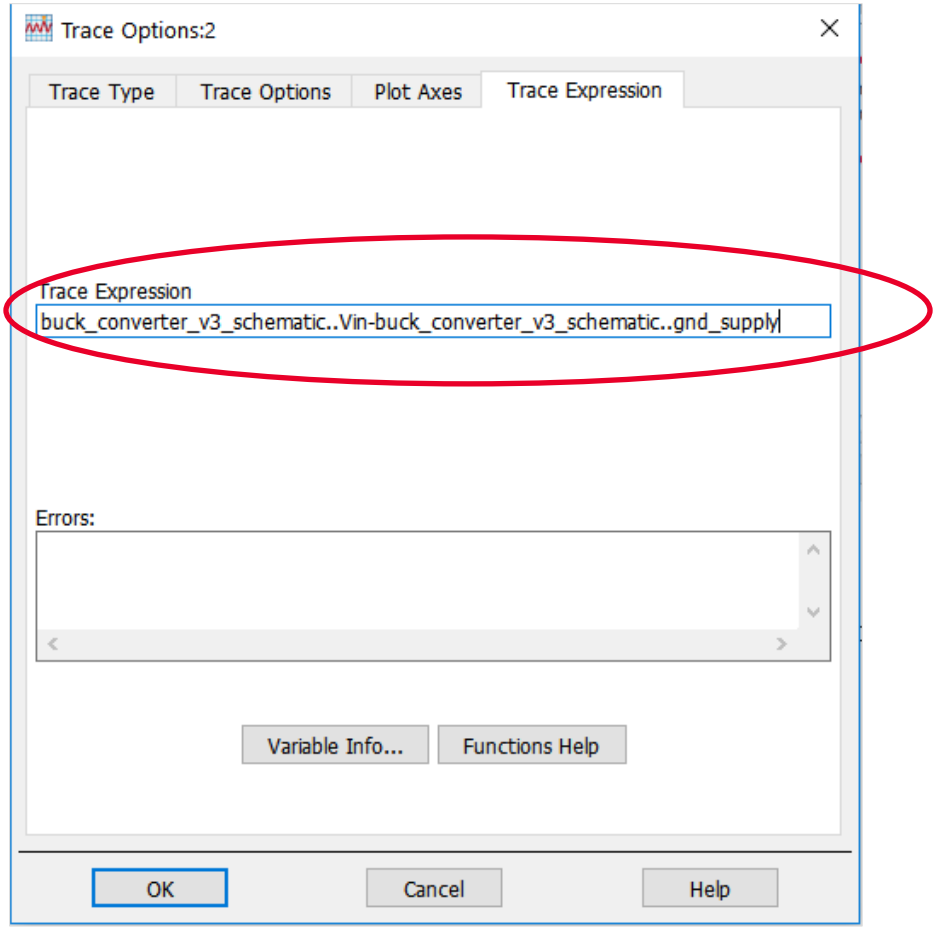


Double-click on the plot and change **Dataset and Equations** to **buck_converter_v3_schematic** and **Add** node voltages **Vin** and **Vload:**



Now double-click on buck_converter_v3_schematic..Vin and edit Trace Expression accordingly:

buck_converter_v3_schematic..Vin-buck_converter_v3_schematic..gnd_supply



When finished press OK then proceed with buck_converter_v3_schematic..Vload:

buck_converter_v3_schematic..Vload-buck_converter_v3_schematic..gnd_load

When finished press **OK.**

Now a graph with input (blue line) and output (red line) voltage at the buck converter with EM model is shown (see Figure 9 Input & output voltage waveforms). The input ripple and switching noises are suppressed in the output waveform.

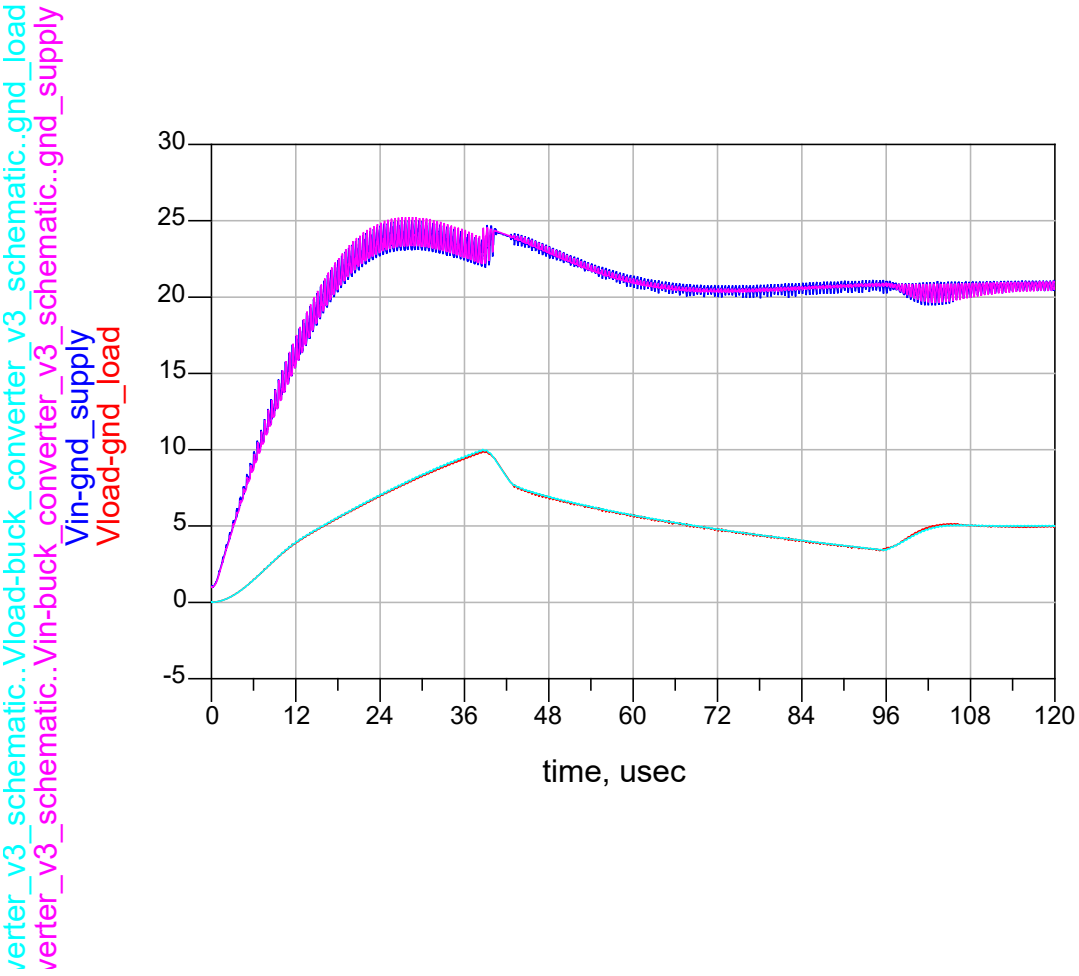


Figure 19. Input & output voltage waveforms: schematic and layout comparison

To compare waveforms at the switching node inside the converter open another rectangular graph and select **X3_P4_sw_X3__Gnd** and **buck_converter_v3_schematic..sw** nodes.

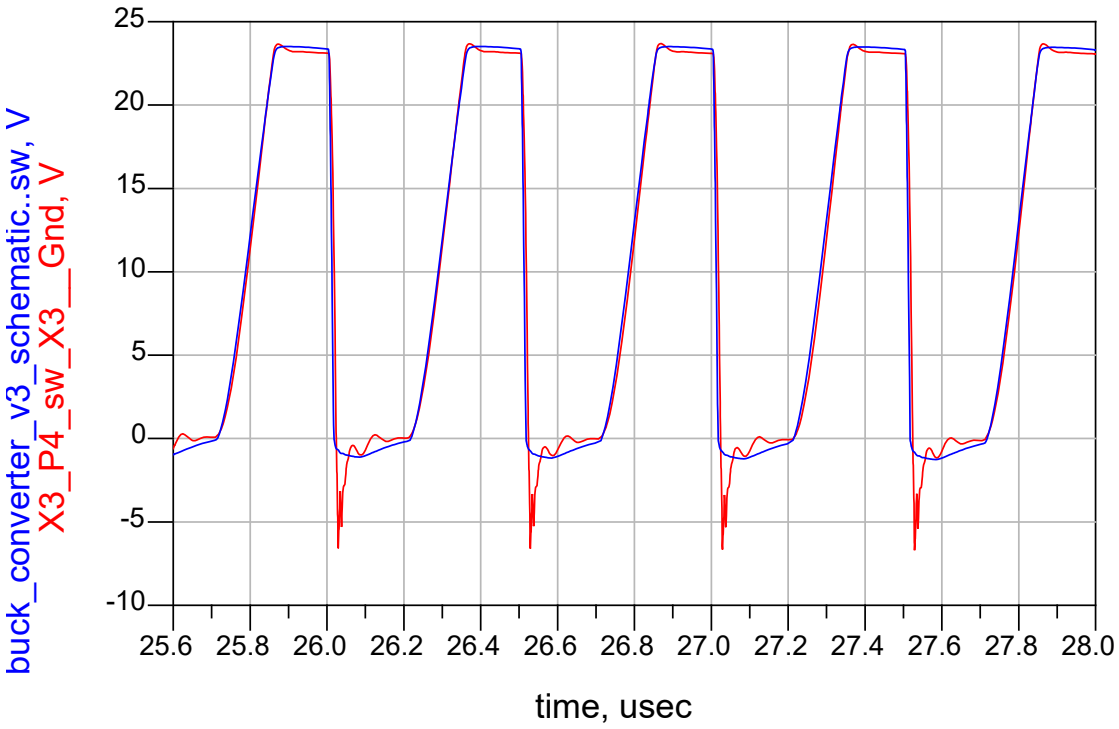
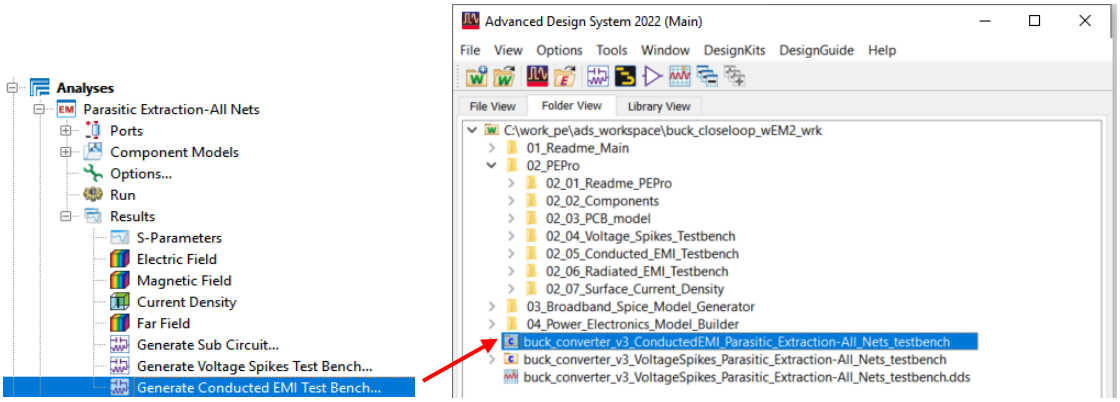


Figure 20. Waveform at the switching node inside the converter: schematic and layout comparison

Conducted EMI analysis

Now we will see how to perform EMI analysis. In ADS main window expand **buck_converter_v3** cell and open **pepro1** view, if not already opened. In the PEPro window go to **Analyses** and expand **Parasitic Extraction-All Nets** -> **Results** setup. Then double-click on **Generate Conducted EMI Test Bench.**



This generates a new cell in the workspace with a name according to following syntax: <*original-cell-name*_**ConductedEMI**_*PEPro-analysis-name*_**testbench**>. So, in our case it is **buck_converter_v3_ConductedEMI_Parasitic_Extraction-All_Nets_testbench**.

In the ADS main window expand **buck_converter_v3_ConductedEMI_Parasitic_Extraction-All_Nets_testbench** cell and open schematic view. This is the conducted EMI test bench.

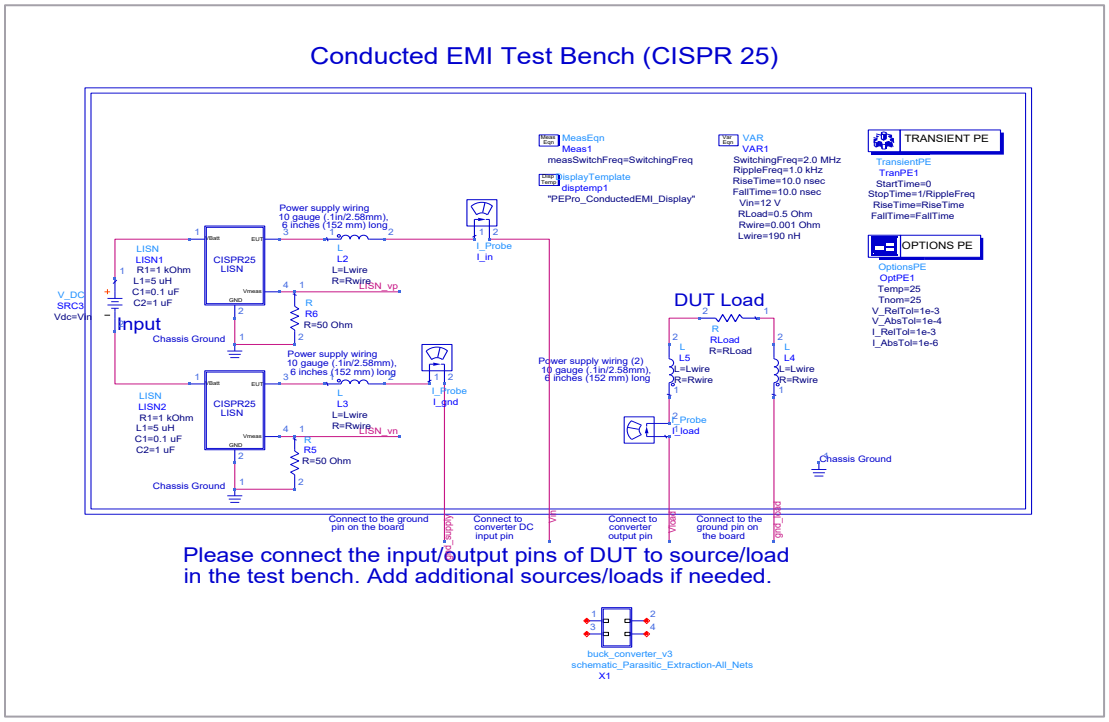


Figure 21. Conducted EMI Test Bench

The test bench schematic includes **TranPE1**, the transient simulation controller (applicable for Power Electronic applications) in which the **RiseTime** and **FallTime** parameters are automatically populated from the **SMPS** frequency plan type in PEPro. The X1 sub-circuit is the Device Under Test (DUT) in the test bench schematic. The sub-circuit is generated in PEPro as the EM-model of the full layout EM-extraction.

Further we can observe **Linear Impedance Stabilization Network** (LISN) component that consists of equivalent circuit of a real LISN hardware. A line impedance stabilization network serves three purposes:

The LISN isolates the power mains from the equipment under test.

The LISN isolates any noise generated by the DUT from being coupled to the power mains.

The signals generated by the DUT are coupled to the X-Series analyzer using a high-pass filter, which is part of the LISN.

In our case the LISN will be used for noise isolation generated by DUT/EUT.

Please make sure DUT terminals are connected to the labeled wires of the conducted EMI test bench:

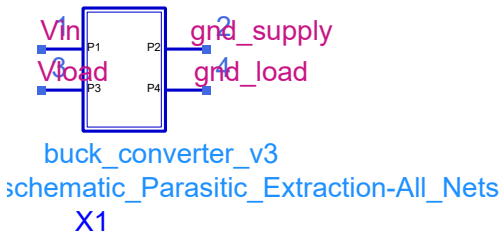
Vin: input DC voltage

gnd_supply: input ground

Vload: output of the converter

gnd_load: output ground

Note, the conducted EMI test bench schematic wire labels are used in the data display template equations and cannot be renamed.

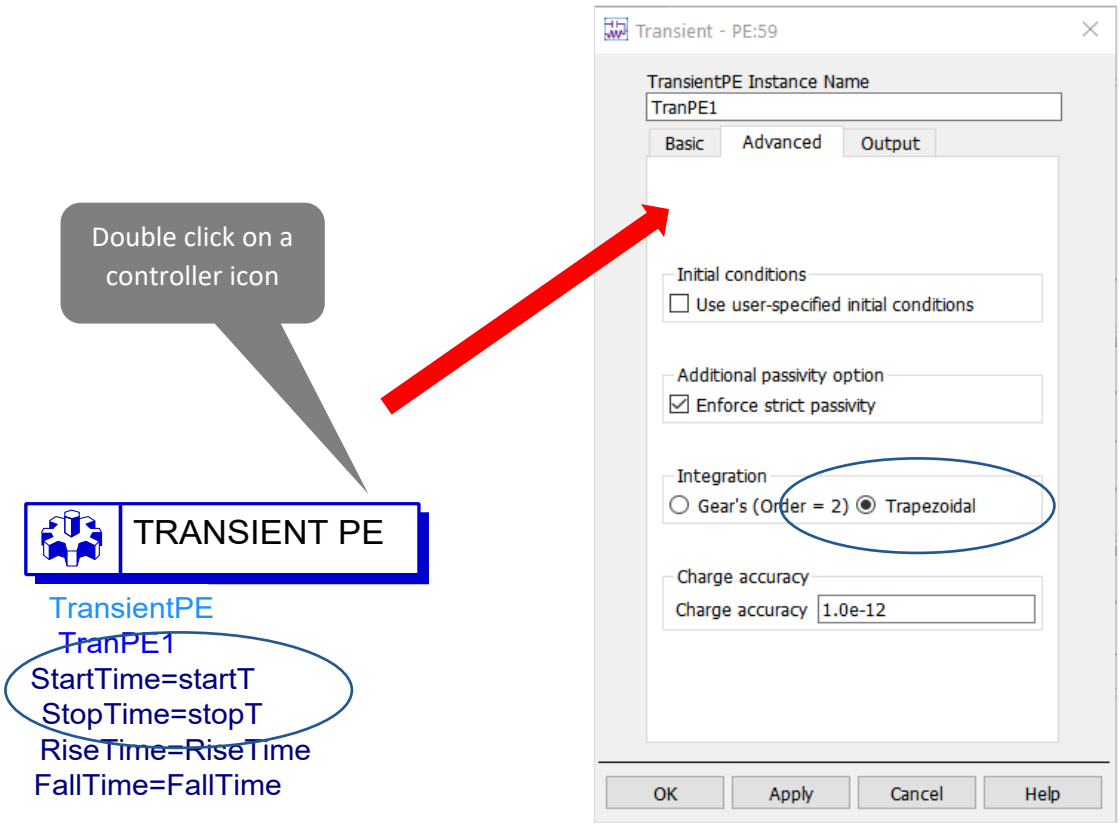


But before testing compliance of entire design (schematic together with layout), let's check whether the schematic itself is EMI compliant. To perform a test drag and drop the **symbol** view of the **buck_converter_v3** into the **schematic** view of **buck_converter_v3_ConductedEMI_Parasitic_Extraction-All_Nets_testbench** cell and make a proper pin net name assignment. Then deactivate EM model and go to **Simulate** -> **Simulation Settings** to uncheck **Use cell name** box and change dataset name to **buck_converter_v3_ConductedEMI_schematic**.

To limit amount of stored data (it may generate substantial size data files), go to **Insert** -> **VAR** and add a new variable component **VAR** into the schematic. Then type equations as depicted in the picture:

We need to make sure data are in steady state thus we will store last 500 switching cycles to compute and display data.

Double-click **TransientPE** controller and adjust accordingly:



This will generate a smaller dataset file and run faster.

Make also sure **Vin = 20V** in the test bench.

Var Eqn
VAR
VAR1
SwitchingFreq=2.0 MHz
RippleFreq=1.0 kHz
RiseTime=10.0 nsec
FallTime=10.0 nsec
Vin=20 V
RLoad=0.5 Ohm
Rwire=0.001 Ohm
Lwire=190 nH

And now press **F7** or go to **Simulate** -> **Simulate** or press corresponding icon on the tool bar to launch the post-layout circuit simulation.

Confirm the conducted EMI simulation results…

After the simulation is completed, a **DD** window is displayed. This window shows the peak spectrums of the SMPS noise (total, differential and common mode noise), calculated from the LISN outputs according CISPR-25 requirements for frequency ranges and spectrum analyzer resolution RBW.

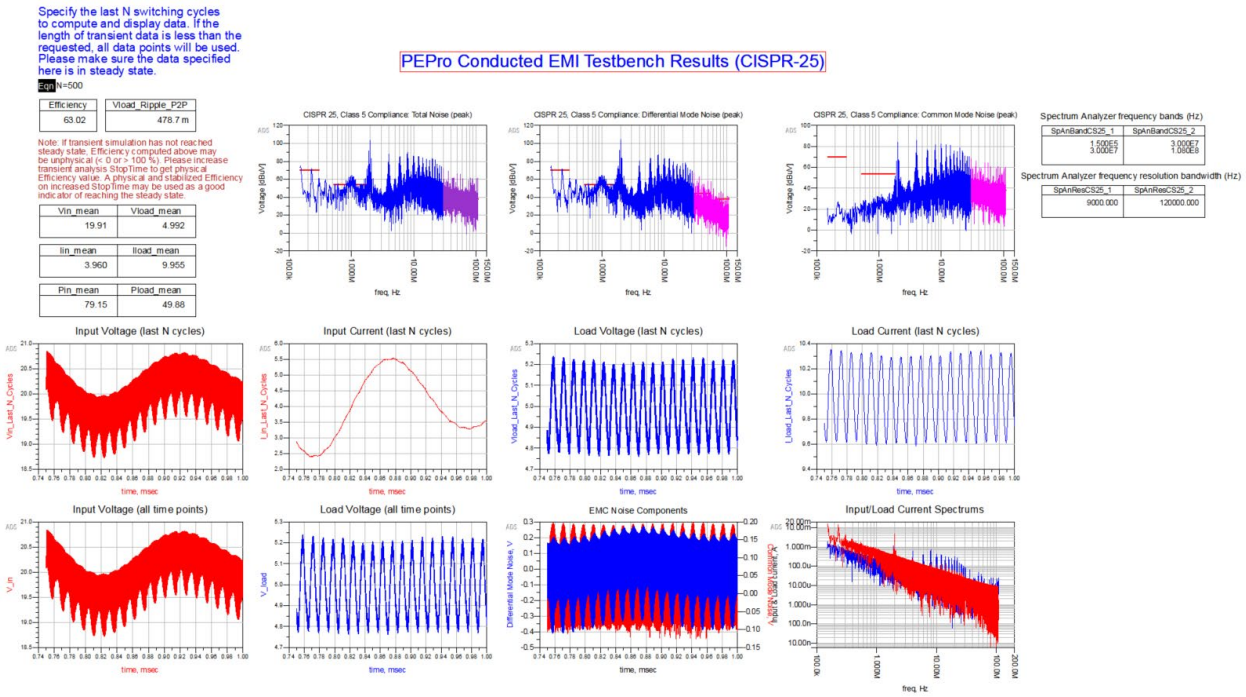


Figure 22. Conducted EMI simulation results of schematic

The results of the EM Co-simulation show a significant increase in noise. In this case it is driven by both differential and common mode noise contributions. You can see noise voltages and the spectral components. There is also an increase in differential mode noise,

Significant voltage spiking and ringing are an issue. Not only does this decrease efficiency, but the voltage spikes can exceed the rating of the transistor, so this can be a real reliability concern. Probing in the lab may or may not uncover the reliability issue as lab measurements are often hampered by equipment and probe locations that can be utilized.

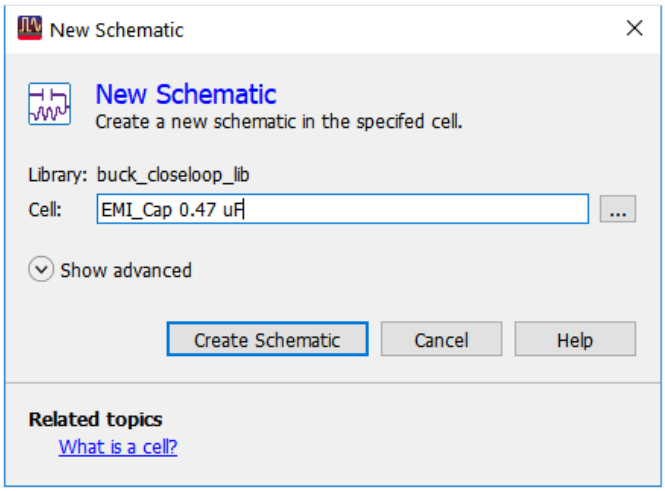
There is significant EMI present on the power leads – well over the spectral mask limits. Lowering the switching speed will cause the overall design to grow in size, which is not desirable, so this is not an option.

These results are obtained even before layout parasitics are added, so the only remedy to reduce EMI is to add EMI filtering to the design.

Let's build EMI Filter!

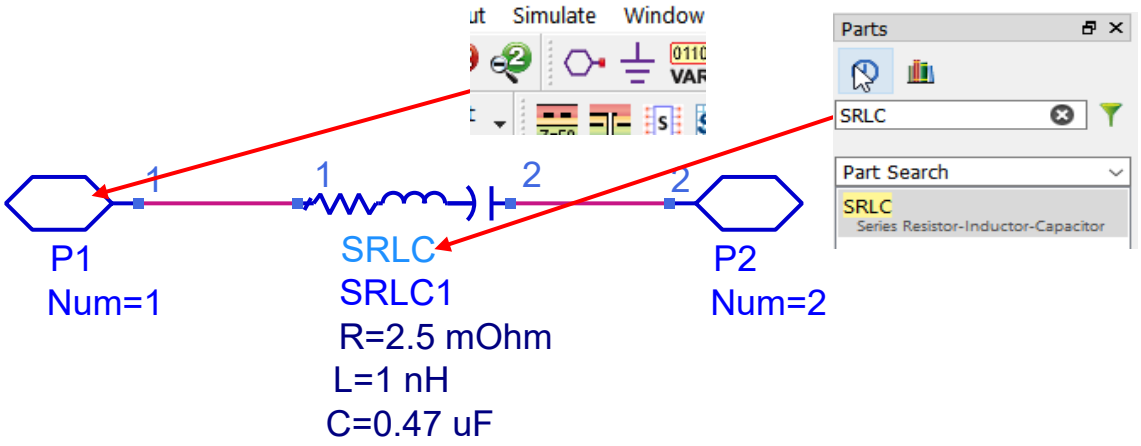
In main ADS window got to **File** -> **New** -> **Schematic** and name it as **EMI_Cap .47uF**

Then press **Create Schematic**. A new schematic will pop-up.



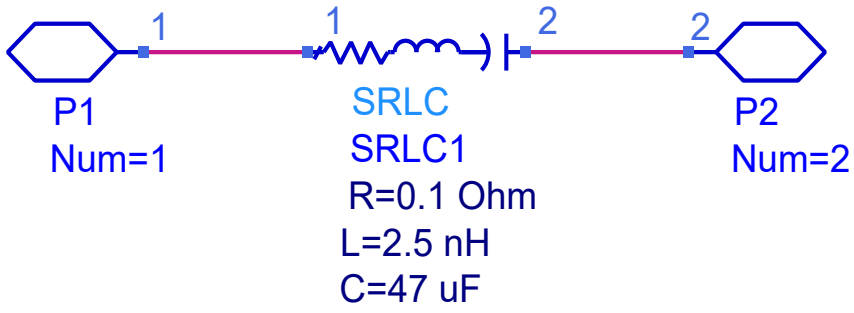
Create circuit as depicted below selecting SRLC component from Lumped-Components library or just searching for it. Then type appropriate values.

Pins can be found on the tool bar:



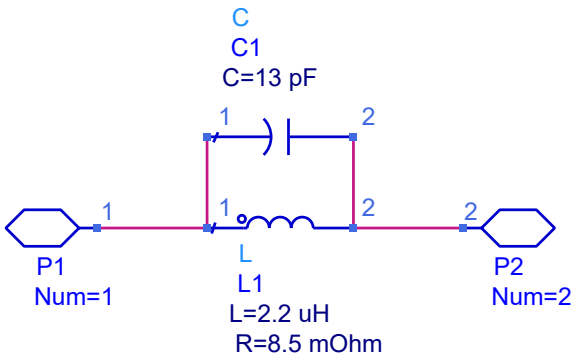
When done save and close schematic.

Now right click on the top **EMI_Cap 0.47uF** cell name and select **Copy cell** providing a new name **EMI_Cap 47uF.** Then edit schematic and change values accordingly:

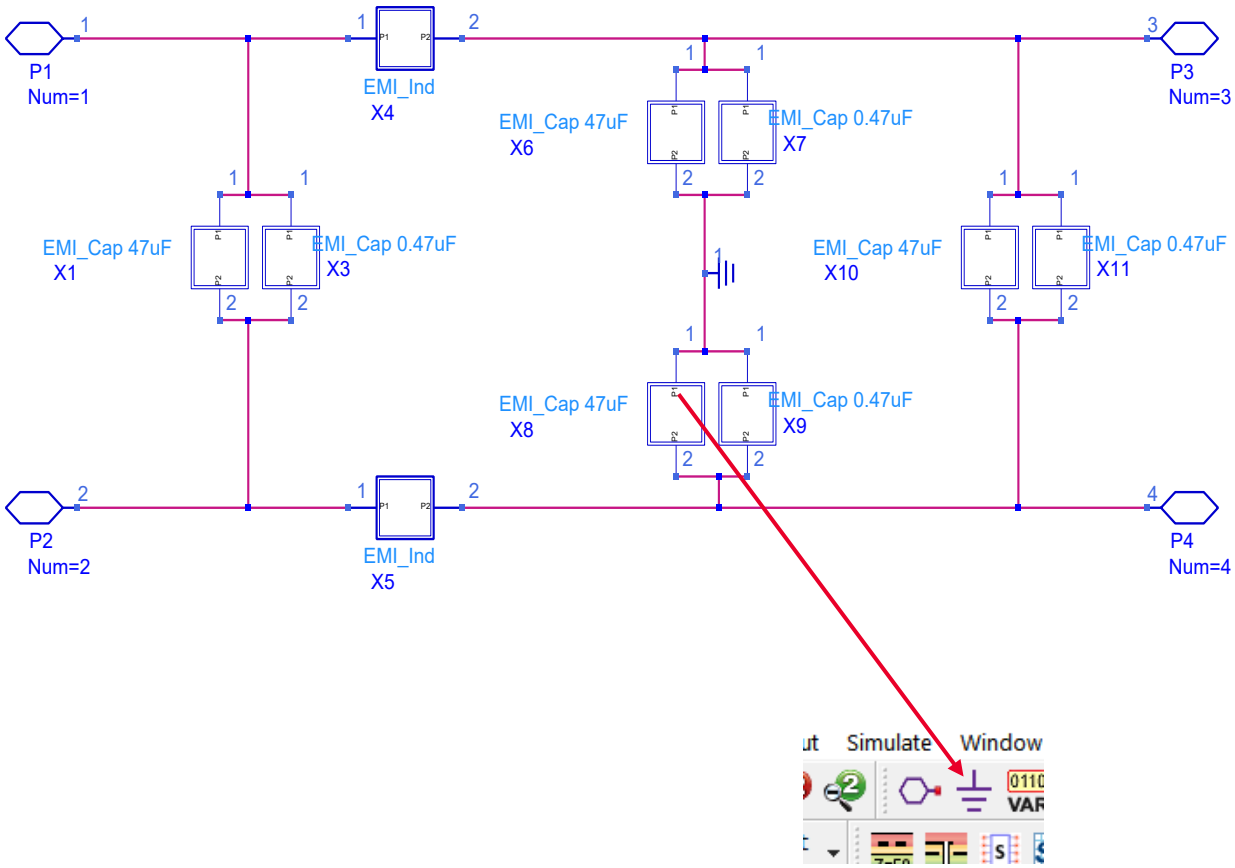


When done save and close schematic.

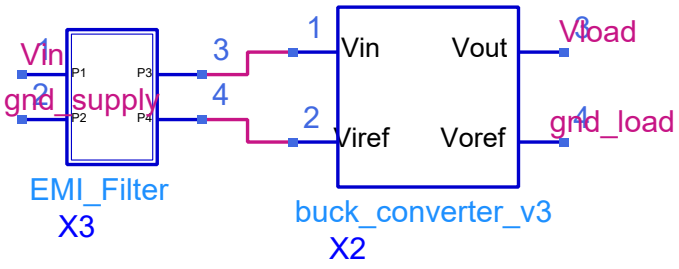
Perform the same step as in **@a** (or by copying previous cells) and create a component/schematic with **EMI_Ind** name**.**



As last step let's make use of created components by dragging and dropping appropriate schematic into a new cell/schematic called: **EMI_Filter.** When asked to generate a symbol respond Yes and proceed further accepting default settings.


P1
Num=1
EMI_Ind
X4
EMI_Cap 47uF
X6
EMI_Cap 0.47uF
X7
P3
Num=3
EMI_Cap 47uF
X1
EMI_Cap 0.47uF
X3
EMI_Cap 47uF
X10
EMI_Cap 0.47uF
X11
EMI_Cap 47uF
X8
EMI_Cap 0.47uF
X9
P2
Num=2
EMI_Ind
X5
P4
Num=4
ut
Simulate
Window

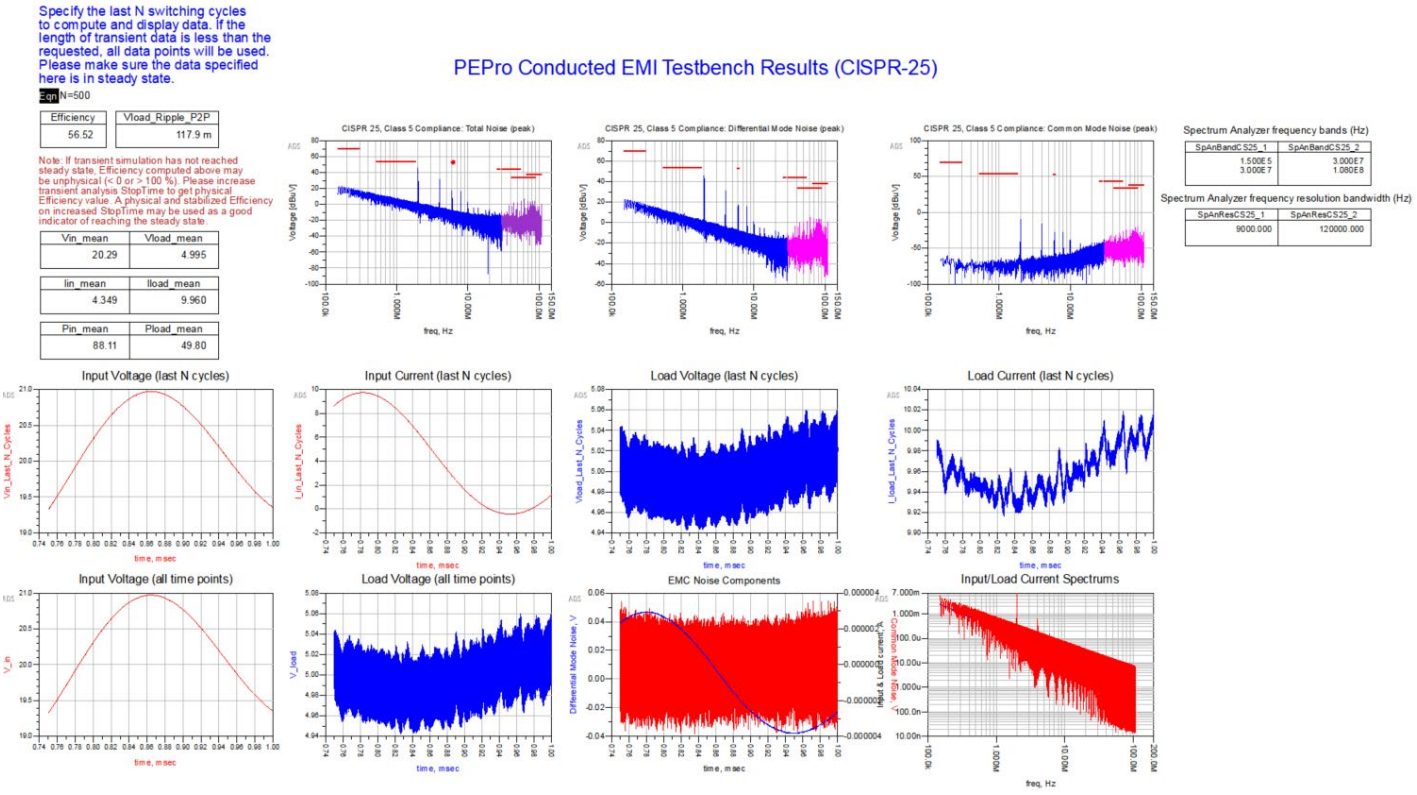
Open the **schematic** view of the **buck_converter_v3_ConductedEMI_Parasitic_Extraction-All_Nets_testbench** cell and drag and drop **EMI_Filter schematic** view into it. Agree to take a symbol generation request and proceed next steps accepting default settings. Connect **EMI_Filter** with **buck_converter_v3 schematic** model as in the picture below:



Make sure there are no net names at the pins 1 & 2 of the **buck_converter_v3 schematic** model, instead those net names are moved to the input pins of the filter. And keep EM model still deactivated.

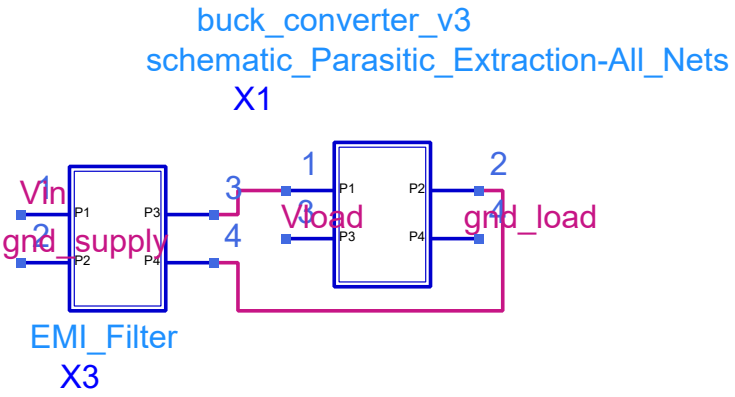
Next, go to Simulate -> Simulation Settings and change Dataset name to buck_converter_v3_ConductedEMI_schematic_EMI_Filter. When done press F7 to start simulation.

After the simulation is completed, a **DD** window is displayed.



This is the performance of the Buck converter after implementation of the EMI filtering. Is the design ready for manufacture?

Let's apply **EMI_Filter** to EM model. To do that make sure both components are connected as it is in the picture below:

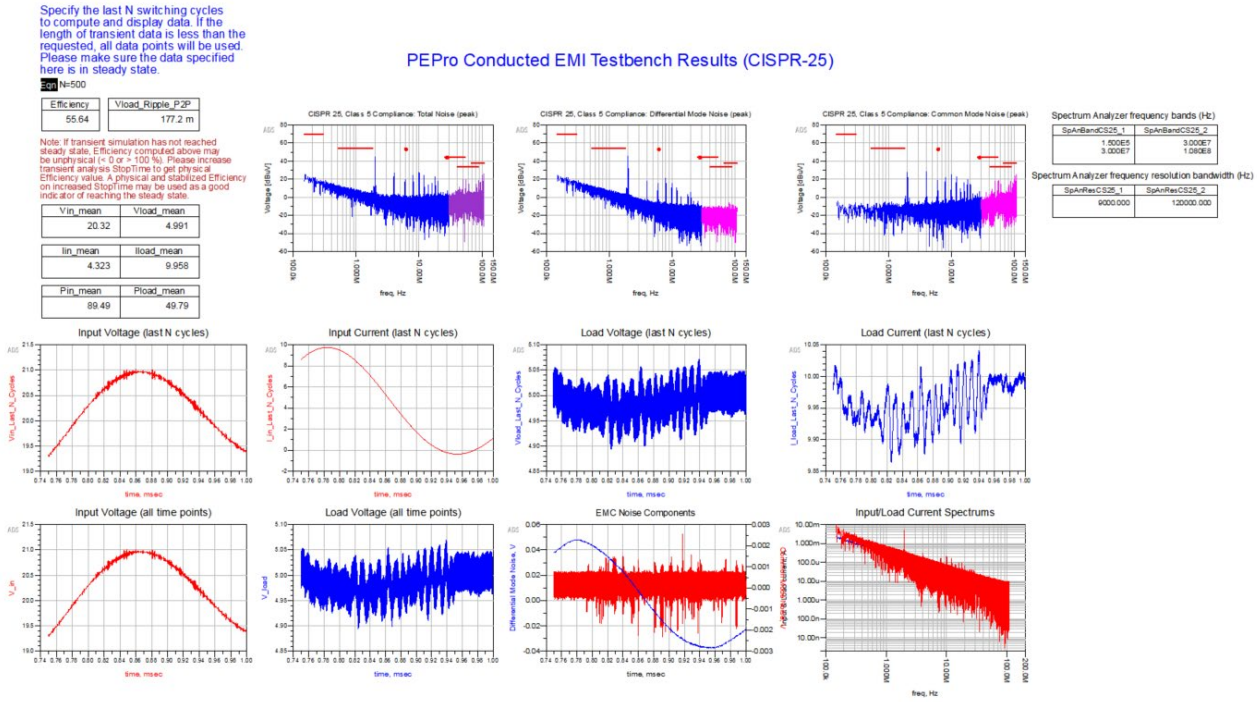


Double check there is no net name between filter and EM model.

Next, go to Simulate -> Simulation Settings and uncheck Use cell name box and change Dataset name to buck_converter_v3_ConductedEMI_Parasitic_Extraction_EMI_Filter name.

When done press **Simulate/F7** to run simulation.

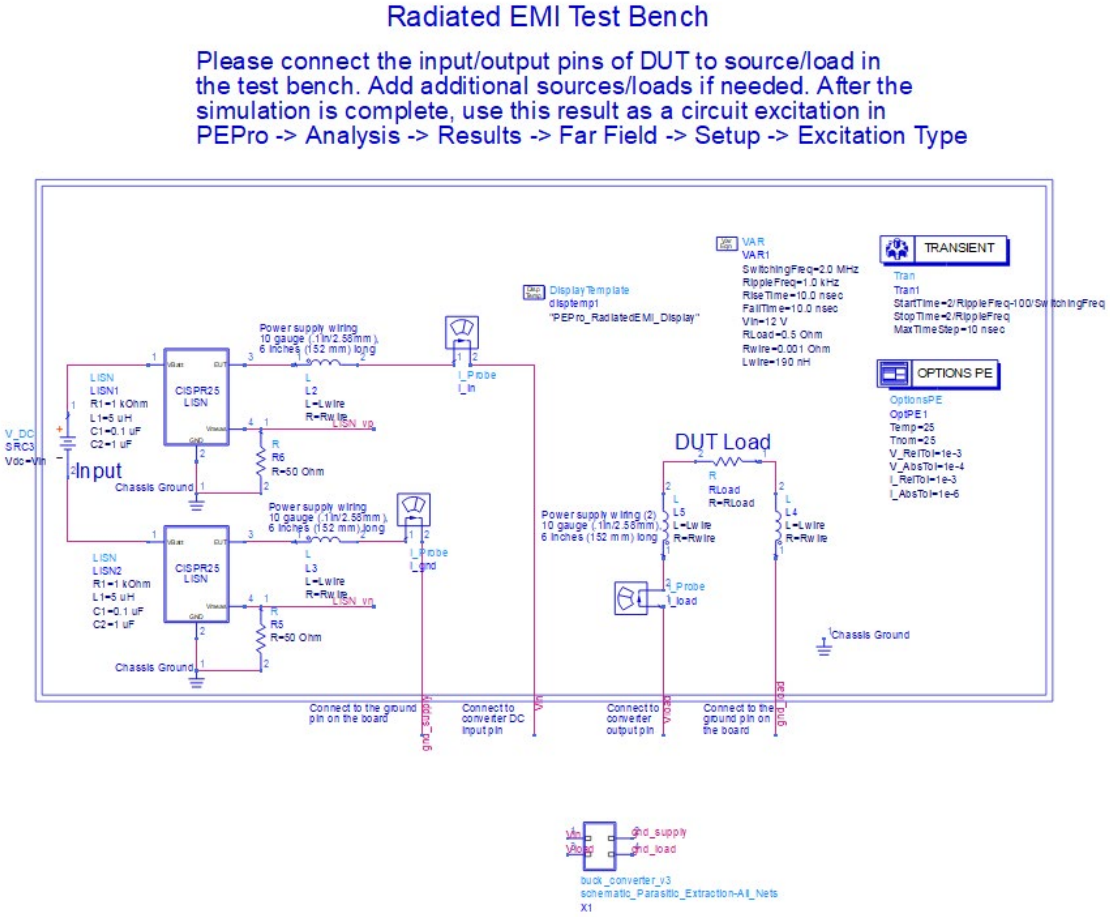
This time after the simulation is completed, a **DD** window displays circuit/EM co-simulation results with EMI filter.

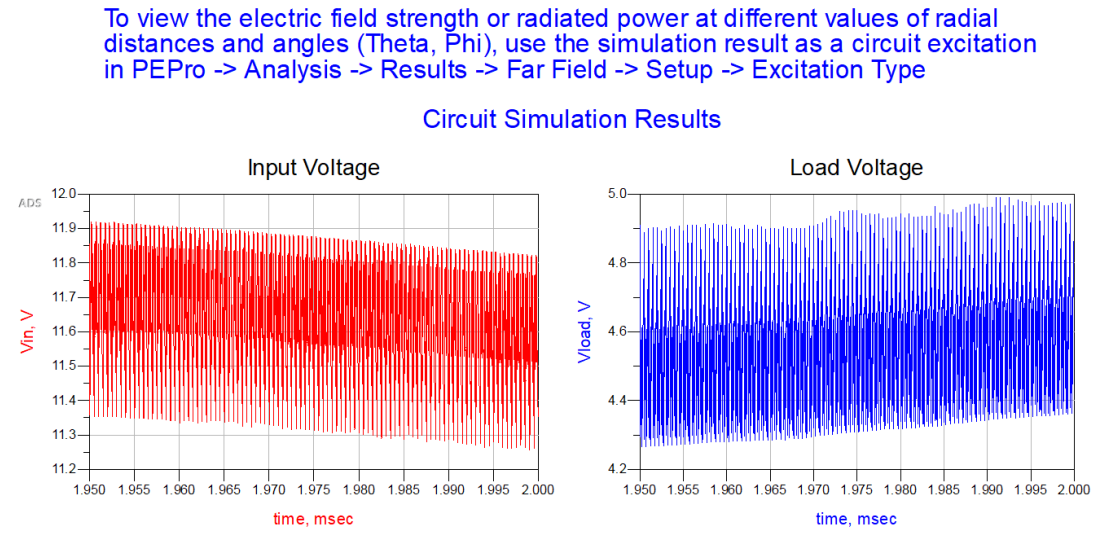


It can be clearly observed both differential and common mode noises were efficiently reduced by EMI filtering. But does it really mean layout itself is noiseless? Well, in this case layout topology has been optimized on purpose but there is still chance for further improvements.

Far field calculation for radiated EMI analysis

The built-in far-field solver in PEPro can help user obtain far-field radiation pattern under specific excitation. The far-field data, including electric field strength and radiation power, can be examined directly in PEPro.





In PEPro, do the following:

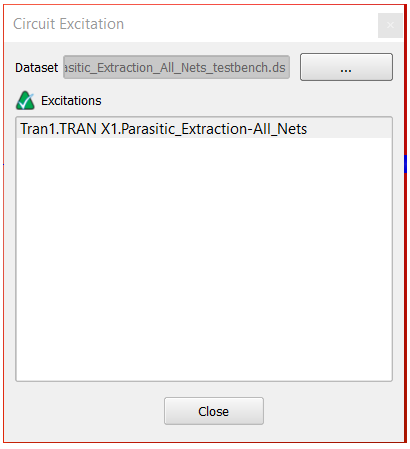
Double-click Far Field in the Results column to open the Far Field viewer.

Select **Circuit Simulation Dataset** from the Excitation Type pull-down menu in the Setup tab at the bottom of the Layout window.

Circuit Simulation Dataset: Press the Select Dataset button and click the […] button in the Circuit Excitation window to open the folder (./data) containing the testbench analysis results. (May be open when you select Circuit Simulation Dataset).

Select buck_converter_v3_RadiatedEMI_Parasitic_Extraction_All_Nets_testbench.ds and press the Open button.

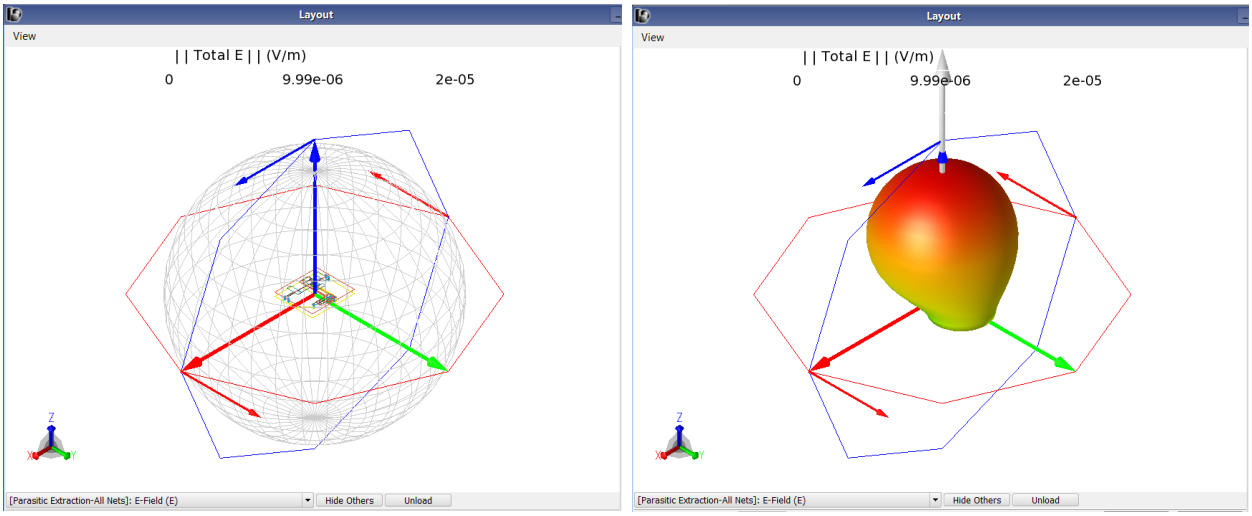
Wait for a while for the dataset to load. Triangular warning mark [!] Becomes green [✔], reading is complete. Press the [Close] button to close the window.



Select Frequency: 2 MHz at Setup tab.

The Far Field of EMI radiations will be displayed as in the picture below.

Radiated EMI Plots:



Surface current density visualization

Getting started:

Open "pepro1" located in 02_PEPro -> 02_03_PCB_model -> buck_converter_v3 -> pepro1, click Run under 'Parasitic Extraction-All Nets_FEM' analysis and wait for the simulation to complete.

Double click "Generate Sub Circuit..." under "Results" in the analysis. This will create or overwrite the existing sub-circuit that can be used in the EM-circuit co-simulation.

Run any one of the following testbenches - Voltage Spikes Testbench, Conducted EMI Testbench or Radiated EMI testbench and wait for the simulation to complete.

Steps to view surface current density by layers -

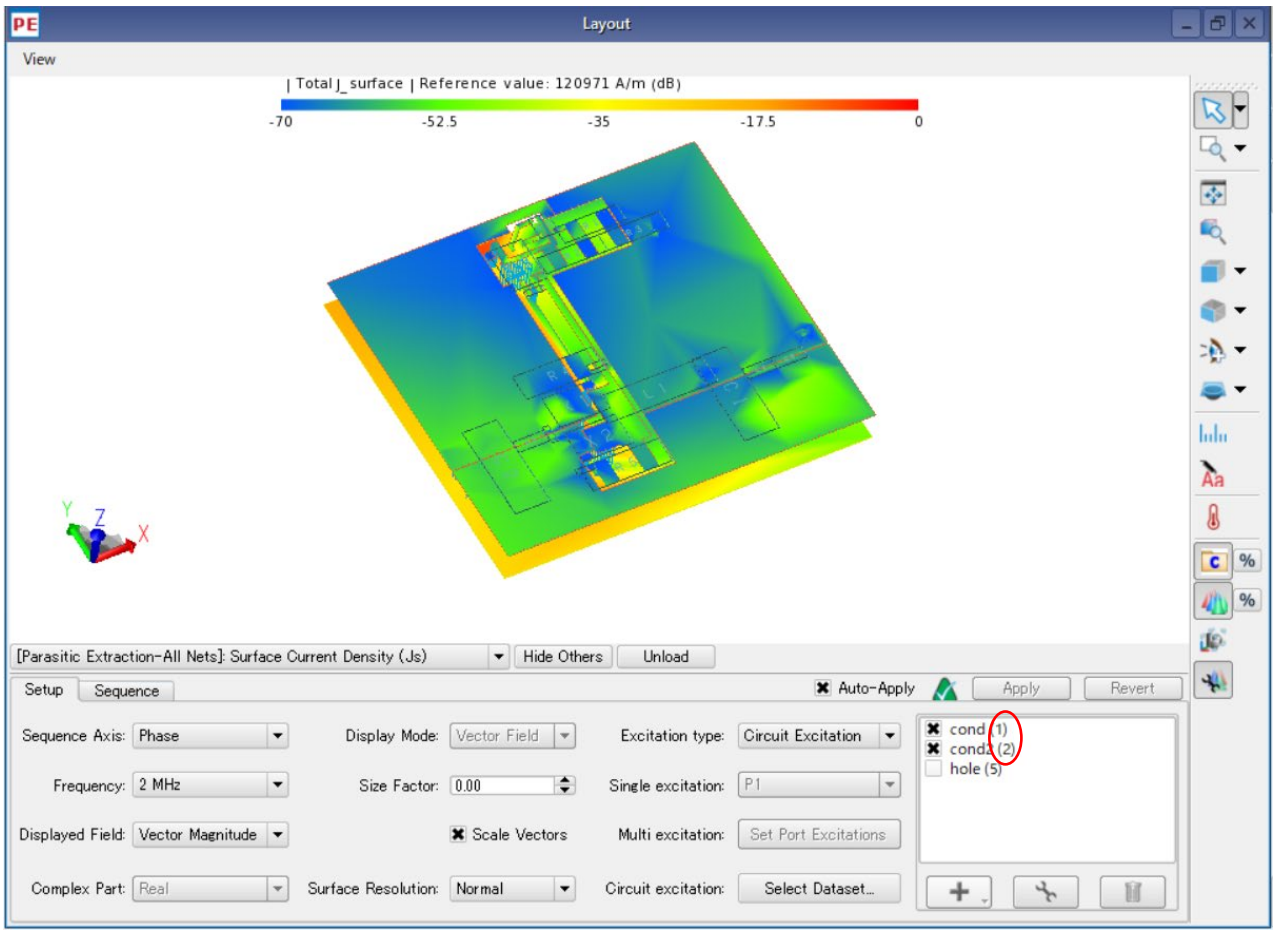
In the PEPro1 window, open "Near Field" under "Results" in the analysis. A 3D graph plotting the selected field component is added in the geometry window.

Select the desired frequency in the Setup tab of the field editing toolbar at the bottom of the window. As an example, you could specify the switching frequency of 2 MHz used in the example.

Select the "Excitation Type" as "Circuit Simulation Dataset" and select the dataset that was generated by simulating the testbench in the workspace's "Data" directory and wait for the dataset to load.

The Setup tab also provides an option on its right side to hide or show specific layers while viewing the surface current density.

The Sequence tab allows you to control how results from different frequencies or results corresponding to different values of the phase can be shown in sequence in the geometry window.



EM field visualization with circuit excitation often yields insights into which traces to focus on. For example, current crowding is often an indicator of excessive inductance. Further, Circuit Excitation allows you to visualize field data such as surface currents and far-field of your EM Model/ EM Co-simulation with any circuit elements contribution from your schematic.

Datasheet-based model builder:

Power Electronics Model Builder tool provides a simplified and fully automated flow to extract a Si/SiC Power MOSFET model from a datasheet.

Steps to extract a model from a measured data.

Launch the tool by going to "Tools" -> "Power Electronics Model Builder" from the Schematic window.

Select Device Type.

Load the measured data. As an example, sample measured data files of a SiC model have been added to the workspace's Data directory. Enable IV checkbox and click "Browse" button to load "Data-IV.mdf" from the Data directory. Enable CV checkbox and click "Browse" button to load "Data-CV.mdf" from the Data directory.
Note: Body diode characteristics can be mentioned if available. In this demo, we are keeping it simple by specifying just the IV and CV data.

Run extraction

Specify a "Data Display Name" if you do not wish to overwrite any previous extraction results. Otherwise, the default Data Display Name is used. Click the "Run Extraction" button. If the button is grayed out, then there should be an error in the above steps. While the extraction is in progress you will be able to see the fitting of IV and CV plots in the data display window that pops up. After the extraction is complete, the measured and final simulated results of IV and CV plots will be shown. Note: If the "Initial Parameter Set" checkbox is enabled and an MPS file is specified, model parameter values from a previous extraction will be used as initial values for the extraction.
Note: Enabling "ANN" will use Keysight's proprietary Artificial Neural Network (ANN) technology for additional optimization to improve the fitting of IV characteristics.

Export

The extracted model can be placed on a schematic or exported to an MPS file.

Download workspace for confirmation

After model extraction, to use a schematic for confirmation, makes it possible to refer to the library in example workspace, GenericPowerMOSFET_Extract_Example_wrk.

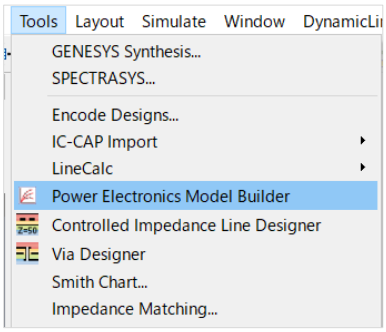
In the ADS main window, select File-> Open-> Examples, type extract in the search field of the Open Example window, select GenericPowerMOSFET_Extract_Example_wrk.7zads and place it in the desired directory.

Then in the ADS main window, select File-> Manage Libraries, if necessary, press the Add Library Definition File button at the bottom left of the Manage Libraries window, select the lib.defs file under GenericPowerMOSFET_Extract_Example_wrk, and click Open Press the Close button respectively.

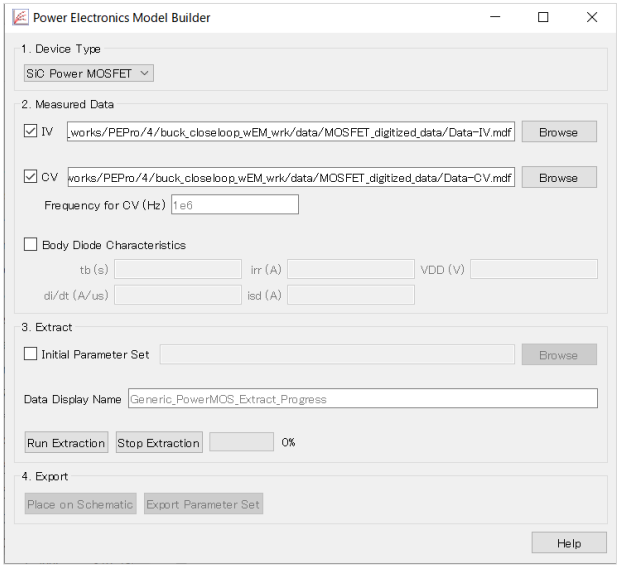
Launch power electronics model builder

Launch Broad Band SPICE Model Generator by performing the following menu operations.

Any Schematic window -> Tools -> Power Electronics Model Builder.



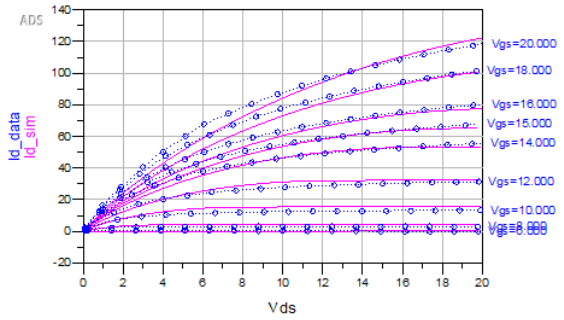
When the Power Electronics Model Builder window opens, click the Browse button for each IV / CV of Measured Data and select each file in mdf format in the _wrk / data / MOSFET_digitized_data directory.



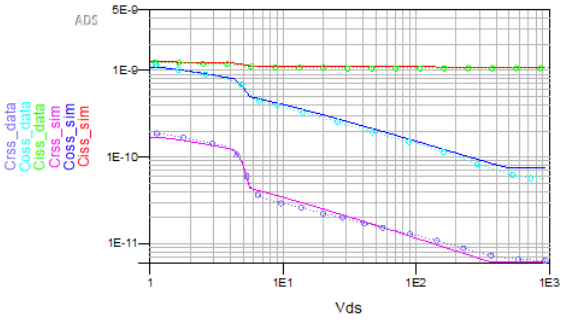
Click the Run Extraction button in the Extract column to execute the extraction.

When the extraction is complete, a data display window will open, where you can compare the Datasheet values with the results.

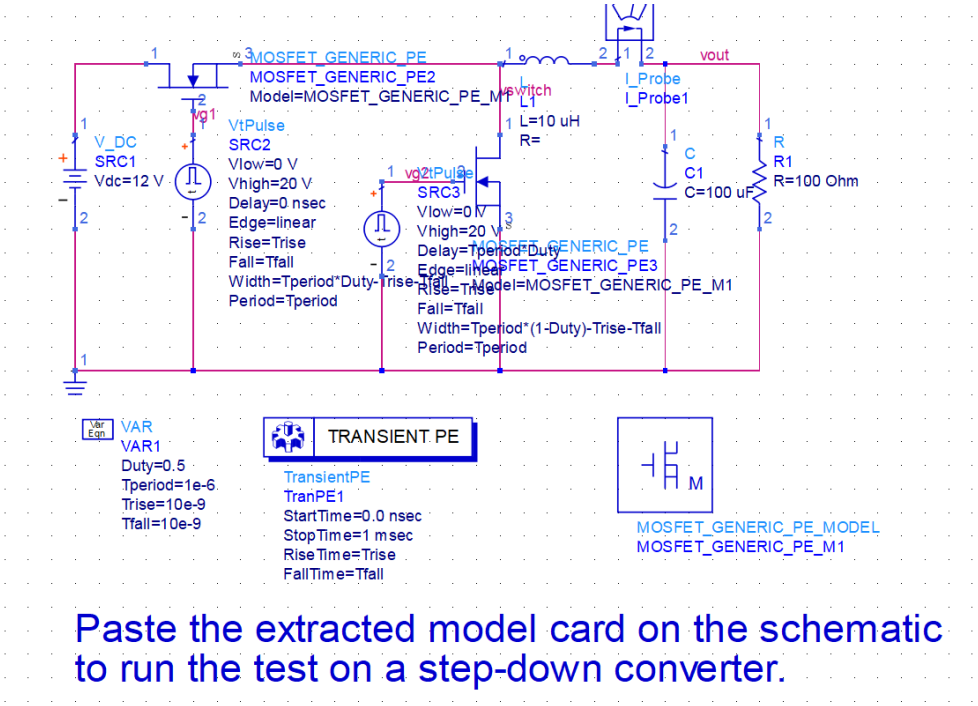
IV Characteristics: Extracted Results vs. Datasheet



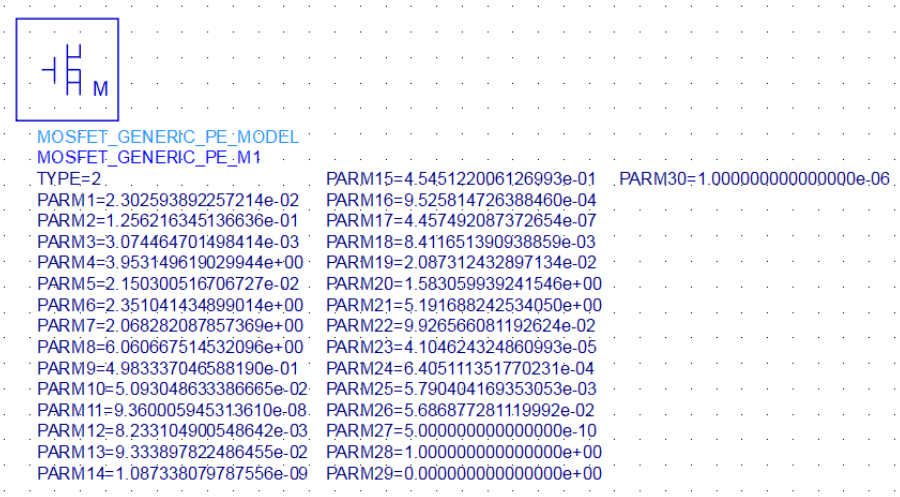
CV Characteristics: Extracted Results vs. Datasheet



After checking the result, click the Place on Schematic button in the Export column to insert and use the model extracted in the desired schematic. Here, open Test_buck_converter in GenericPowerMOSFET_Extract_lib and insert it here.

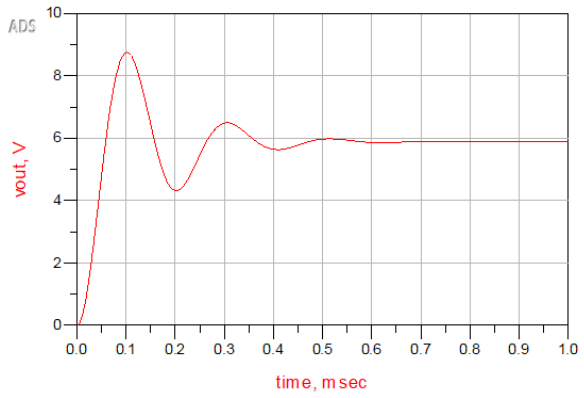


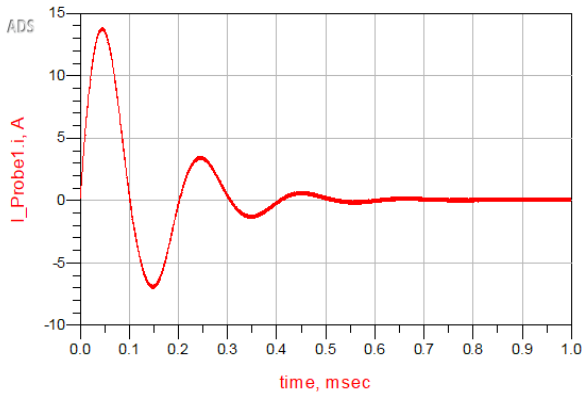
To view the parameters, double-click MOSFET_GENERIC_PE_M1, click the Component Options button in the Edit Instance Parameters window, select Set All in the Parameter Visibility column, and press the OK button twice.



After reviewing the schematic, click the icon to run the simulation.

After the simulation is finished, an empty data display window will open. Select the Rectangular Plot individually, display the vout and I_Plobe1.i data, and check the result.





Creation of a PSPICE Model from S Parameters:

EM-Circuit Co-Simulation is recommended for post-layout analysis, but it is also possible to convert the S-parameters obtained because of analysis with PEPro to a PSPICE compatible model and use it in a PSPICE simulator. However, special care must also be taken to ensure the quality of the transformed model and the accuracy of the circuit simulation in the PSPICE simulator. I will explain them here as well.

In this exercise, you will experience the S-parameter acquisition and the output of the PSPICE model.

(Please perform after completing "PEPro Setup")

Below is the description for how to generate a PSpice compatible equivalent circuit from S-Parameters generated from EM simulation in PEPro.

Note: As an example, a sample s-parameters file "sample_s_parameter_file.ds" in the dataset format is provided in the "data" directory in the workspace, you can skip to step 3 if you wish to use this sample s-parameter file.

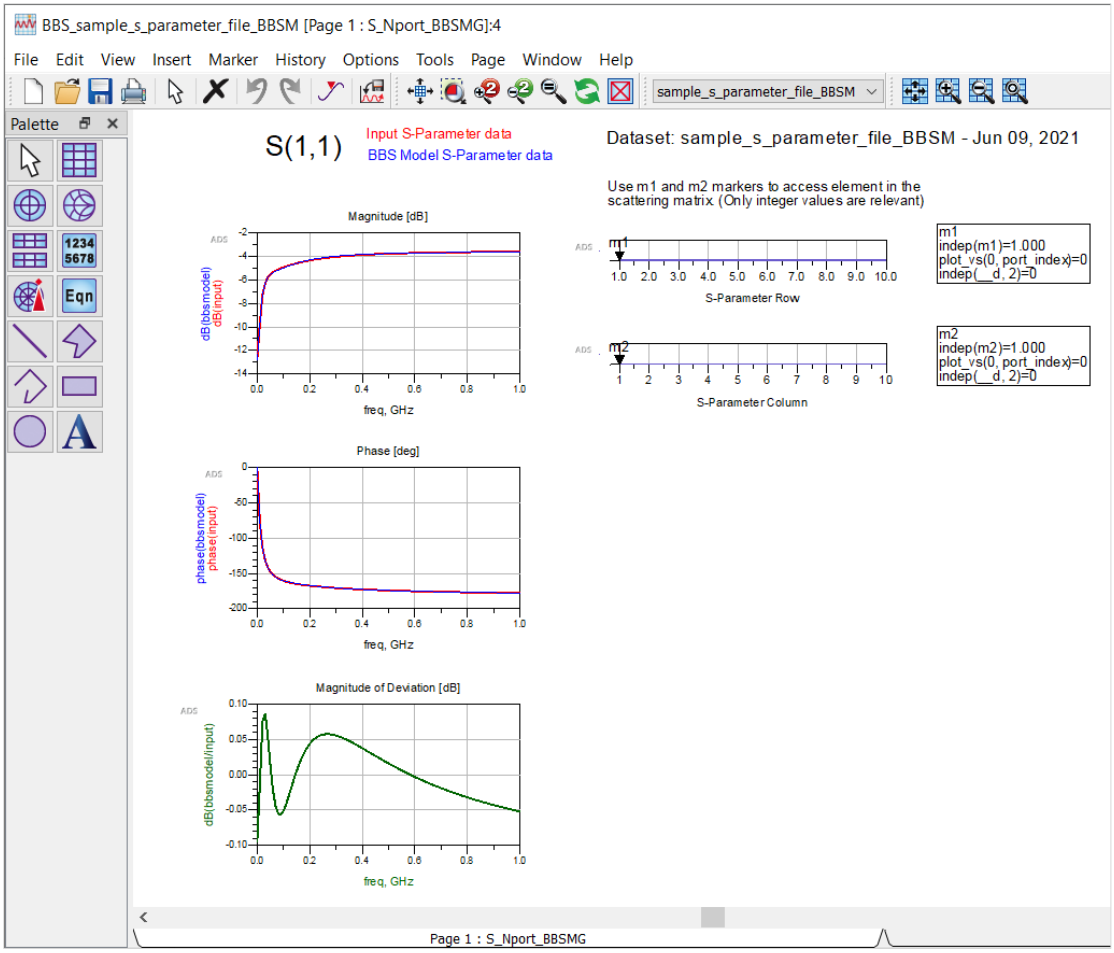
After EM simulation, open S-Parameters window under "Results" -> "S-Parameters" in the Analysis section of PEPro.

From the menu of S-Parameter window, click "File" -> "Save As...", then select Format as "SnP". Click "Export". Then select "touchstone files" from Save as type dropbox and specify a file name. Click save. It will save the S-Parameters file in the directory specified.

Open Broadband SPICE Model Generator from an ADS Schematic window by navigating to "Tools" -> "Spice Model Generator" -> "Start Broad Band Generator". In Broadband SPICE Model Generator window, select File type as "Touchstone", then browse the file saved in step 2. Then from Output section,check PSPICE option and uncheck other options. Specify your preferred output file name prefix, and output directory. Then click the "Start Model Generation" icon on the top task bar. It will generate PSpice compatible equivalent circuit. A file with extension *.psp in your selected output directory will be generated. The dataset window shows the correlation between input s-parameters data and the generated data.

Users can change some settings in "Advanced Input Options" tab by unchecking the box "Use auto-generated values, determined at run-time". Some recommended settings are:

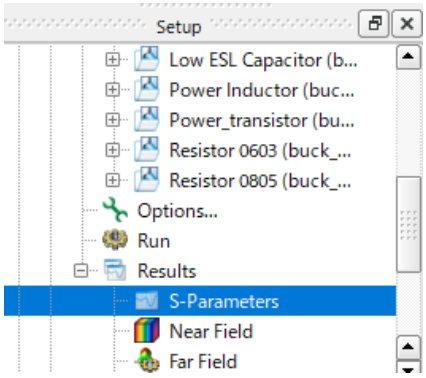
1. The number of poles: set minimum to 1, and maximum to 50. If the maximum is set too small, it may not converge if the Fitting Tolerance (default is 0.005) is set small.
2. Uncheck the option "Mirror poles into left-half plane" when the number of ports is large (> 60).
3. Enforce passivity option would greatly impact run time when the number of ports in S-Parameters is large (>80). If Spice model generator runs too long for your S-parameters file, uncheck this option.



Obtaining a dataset from the analysis results of PEPro

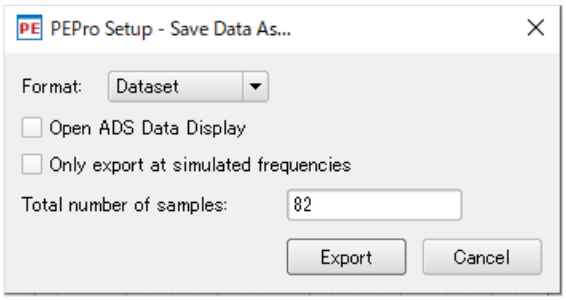
Convert PEPro analysis results to ADS dataset format to create PSPICE models.

Double-click Results -> S-Parameters in the Setup column at the bottom left of the PEPro window.



In the S-Parameters dialog that appears, perform the following menu operations: File-> Save As

The Save Data As dialog will appear. Make sure the Format is "Dataset" and click the "Export" button.

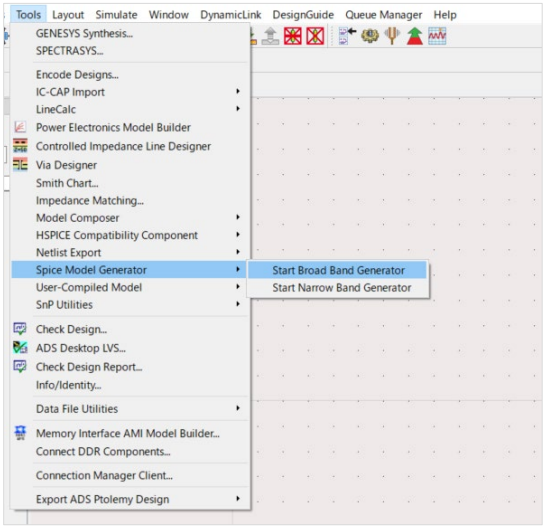


Save the dataset with arbitrary file name. Here, tentatively save the dataset with the name "Translating"

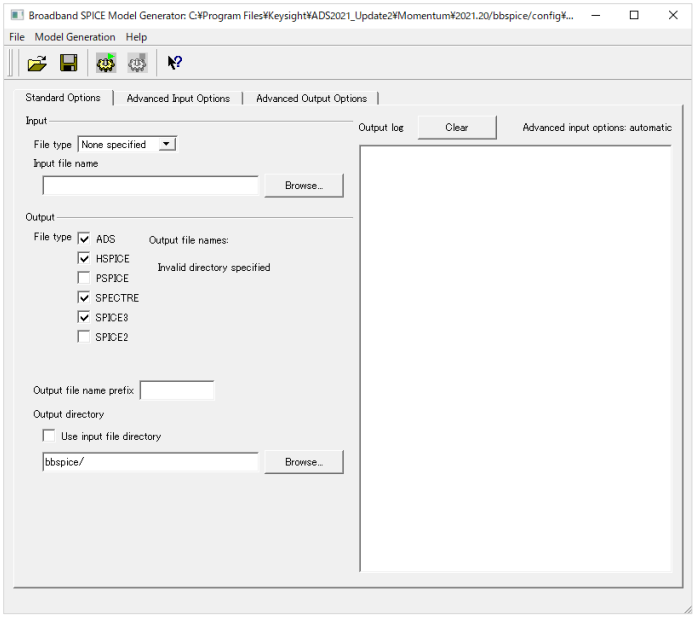
This completes the acquisition of the dataset. Quit PEPro once.

Launch Broad Band SPICE Model Generator

Launch Broad Band SPICE Mdel Generator by performing the following menu operations, any Schematic window- Tools - Spice Model Generator - Start Broad Band Generator.



Broad Band SPICE Model Generator has been launched.



Settings for output of PSPICE model

Make the settings on the Standard Options tab as shown below.

File Type: Set to Dataset

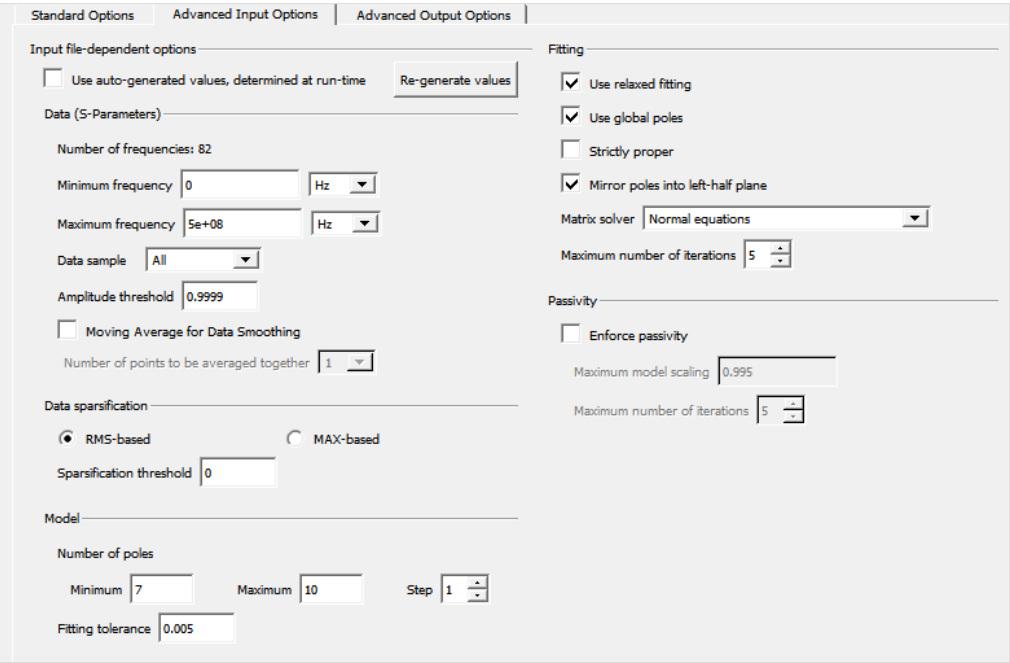
Input file name: Click the Browse button and specify Translating

Output “Check only PSPICE

Select the Advanced Input Options tab and configure the settings as follows: "Uncheck" Use auto-generated values, determined at run-time

Changed Minimum in Number of poles column to "1".

"Uncheck" Enforce passivity



*In this exercise, uncheck Enforce passivity to speed up Model Generation.

Output of PSPICE model

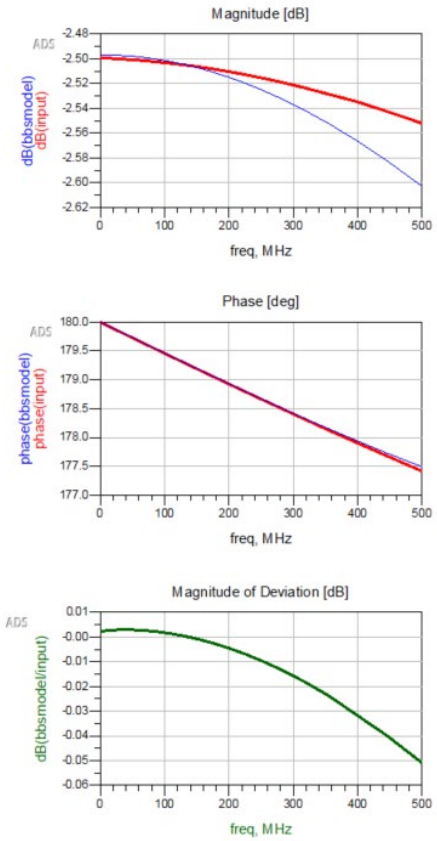
Click the Start Model Generation button to start outputting the model.

The Model Generation status is displayed in the Output log field. Observe it as needed.

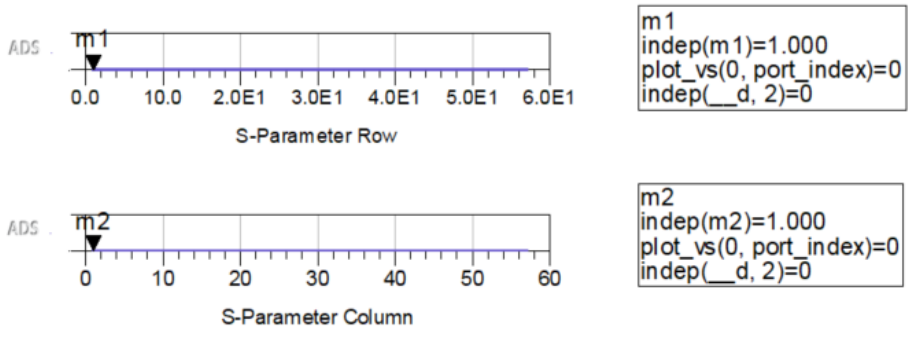
When the output of the model is completed, the data display window will be launched.

Confirmation and changing of result (optional)

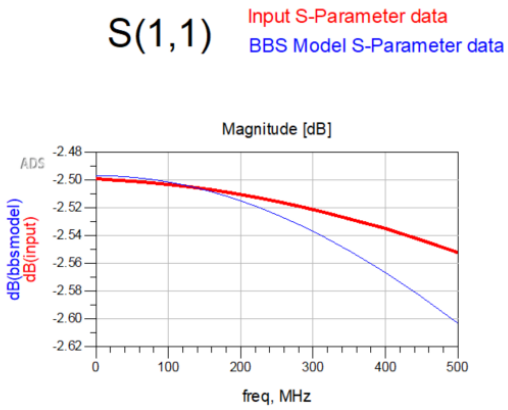
Observe the result on the data display. From top left to bottom left, S-parameters vs PSPICE model magnitude [dB], phase [deg], and PSPICE model-to-S-parameter ratio [dB].



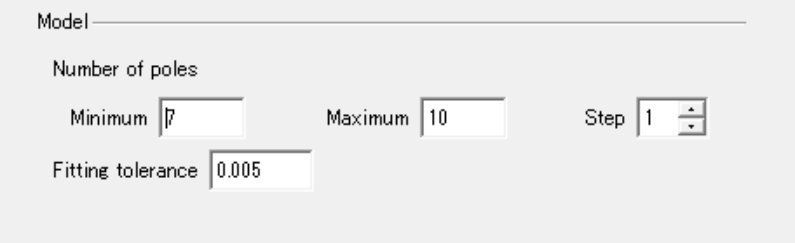
By moving the sliders of "S-Parameter Row" and "S-Parameter Column" on the upper right of the data display, you can check the S-parameter vs. PSPICE model of any combination of S (Row, Column).



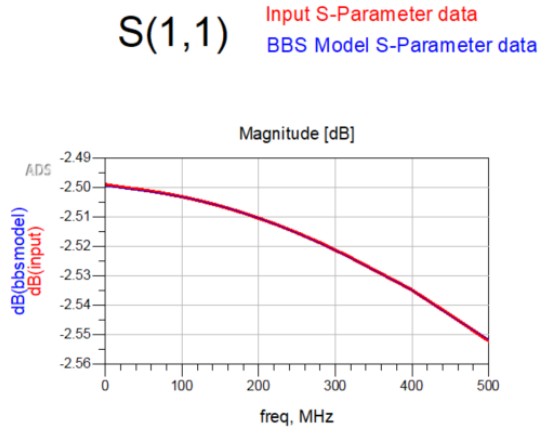
For example, if you check the result of S (1,1), you can see some differences. Please check other things as well.



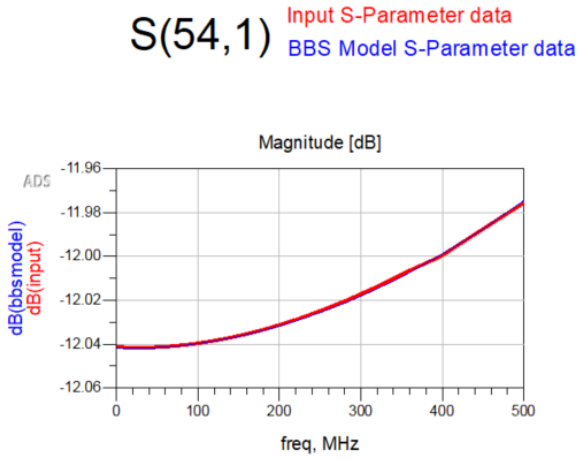
The result is S-parameters and the PSPICE model, with some differences depending on the elements of S (e.g. S (1,1)). This time, in Broad Band SPICE Model Generator, change "Minimum" in the "Number of poles" list on the "Advanced Input Options" tab to "7", generate the Model again, and check the result on the data display again.



Now you can see that the values match relatively well, for example S (1,1).



However, for example S (54,1), there are still differences. This is because SPICE Model Generation uses a lumped constant model to fit values as close as possible to the S-parameters. As long as it is a combination, such a difference can inevitably occur. It is up to you to decide which parameters to use and how to drive them.



This concludes the exercises in this chapter, but in the next section, we will explain the precautions for using the generated model.

Confirmation of result file

Check the psp file created as a result of PSPICE Model Generation.

Open Windows Explorer.

Using Explorer, move to the folder of buck_closeloop_wEM2_wrk.

Under the buck_closeloop_wEM2_wrk folder, there should be a file called Translating.psp in a folder called bbspice. Open it using a text editor (such as WordPad or Notepad).

You should see something like the following: This is the PSPICE compatible model created by ADS. Please use it on a PSPICE compatible simulator as appropriate.

```
* Momentum eesofbbs_64 2021.20 (*) built: Feb 22 2021
*****************************************************

*bbspice subcircuit with consecutive port numbers.

.SUBCKT bbspice_Translating_subckt port_1 port_2 port_3 port_4 port_5 port_6 port_7 port_8 port_9 port_10 port_11
+  port_12 port_13 port_14 port_15 port_16 port_17 port_18 port_19 port_20 port_21 port_22 port_23 port_24 port_25
+  port_26 port_27 port_28 port_29 port_30 port_31 port_32 port_33 port_34 port_35 port_36 port_37 port_38 port_39
+  port_40 port_41 port_42 port_43 port_44 port_45 port_46 port_47 port_48 port_49 port_50 port_51 port_52 port_53
+  port_54 port_55 port_56 port_57  gnd_0

* PORT_1
vi_1 port_1 _net_1 0.000000
vb_1 _net_4 _net_5 0.000000
R_Z0_1 _net_1 _net_2 5.00000000000000e+01
H_b_1 _net_2 gnd_0 vb_1 1.41421356237310e+01
E_v_1 _net_3 gnd_0 port_1 gnd_0 7.07106781186548e-02
H_i_1 _net_4 _net_3 vi_1 3.53553390593274e+00


G_POLE_port1_port1_p1 _net_5 gnd_0 LAPLACE {V(_net_5, gnd_0)} = {-4.28834584661955e-05 / (s*2.36980717533100e-08 + 1.0)}
G_POLE_port1_port1_p2 _net_5 gnd_0 LAPLACE {V(_net_5, gnd_0)} = {-3.00036952293788e-04 / (s*1.63140870861797e-09 + 1.0)}
G_POLE_port1_port1_p3 _net_5 gnd_0 LAPLACE {V(_net_5, gnd_0)} = {-7.36349390854135e-03 / (s*2.34373924963818e-10 + 1.0)}
G_POLE_port1_port1_p4 _net_5 gnd_0 LAPLACE {V(_net_5, gnd_0)} = {1.50734230108810e-02 / (s*1.29663270197934e-10 + 1.0)}
G_POLE_port1_port1_p5 _net_5 gnd_0 LAPLACE {V(_net_5, gnd_0)} = {-6.76096989837526e-01 / (s*9.33246833243505e-13 + 1.0)}
G_POLE_port1_port1_p6 _net_5 gnd_0 LAPLACE {V(_net_5, gnd_0)} = {-2.00877521312457e-12 * (s + 4.04200139167767e+10)
+ / (s^2*3.03336712761958e-21 + s*1.01798621586730e-10 + 1.0)}
G_POLE_port1_port2_p1 _net_5 gnd_0 LAPLACE {V(_net_10, gnd_0)} = {-2.09082098558252e-05 / (s*2.36980717533100e-08 + 1.0)}
G_POLE_port1_port2_p2 _net_5 gnd_0 LAPLACE {V(_net_10, gnd_0)} = {-5.82706492146593e-05 / (s*1.63140870861797e-09 + 1.0)}
G_POLE_port1_port2_p3 _net_5 gnd_0 LAPLACE {V(_net_10, gnd_0)} = {-7.28581647623672e-03 / (s*2.34373924963818e-10 + 1.0)}
G_POLE_port1_port2_p4 _net_5 gnd_0 LAPLACE {V(_net_10, gnd_0)} = {3.19586611262555e-02 / (s*1.29663270197934e-10 + 1.0)}
G_POLE_port1_port2_p5 _net_5 gnd_0 LAPLACE {V(_net_10, gnd_0)} = {7.30194554824242e-02 / (s*9.33246833243505e-13 + 1.0)}
G_POLE_port1_port2_p6 _net_5 gnd_0 LAPLACE {V(_net_10, gnd_0)} = {-5.08087992923765e-13 * (s + 1.92117277759779e+11)
```

Precautions for using the completed PSPICE model

Depending on the number of ports in the generated model, it may take seconds to hours for PSPICE to import the model using the model editor. Alternatively, you can add the model file (.psp file) to be included in the PSPICE simulator search path without using the model editor. The generated model file (.psp file) is easy to use in simulations, so this method can save you a lot of time setting up your circuit in PSPICE.

The generated SPICE compatible model is valid for all simulations (DC, AC, and transient) supported by PSPICE.

When you use the generated model in a PSPICE transient simulation, you may see a warning about non-causal impulse responses in the status window. This is because the conversion algorithms used by PSPICE and ADS are different. Warnings usually do not affect the simulation results and can be safely ignored.

When using the generated model in a PSPICE transient simulation, if the simulated waveform is unexpected, reducing the relative margin of error (RELTOL) may help to obtain more accurate results.

The generated model implicitly references the global ground node (0)

The generated PSPICE model does not retain the port name in the S-parameter file if it exists. Instead, it is output into the SPICE model in exactly the same port order as the S-parameter file. We recommend, to make it easier to build a complete post-layout circuit in a PSPICE compatible simulator, use PEPro's Generate Sub Circuit option and follow the generated schematic to complete the connection on all ports of the PSPICE model.

Conclusion and next steps

In power electronics, ADS can solve problems that SPICE alone cannot:

Layout parasitics cause voltage spikes in high di/dt loops.

ADS incorporates an EM-based model of your PCB traces into the circuit simulation.

“What if…?” design space exploration.

This guide has just a small taste! Contact your Keysight EEsof EDA expert for further e-learning material to meet your needs!