16860 Series Portable Logic Analyzers

KEYSIGHT

SERVICE GUIDE

Notices

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Safety Notices

CAUTION

A CAUTION notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

Additional Safety Notices

This apparatus has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warnings and Cautions

WARNING **Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.**

CAUTION **Do not use this instrument with a power cord other than the one provided by Keysight. The power cord provided is matched to the country of the origin of the order.**
Other power cords may not have appropriate ratings. Therefore, you must not replace the detachable MAINS supply cords by inadequately RATED cords.

WARNING **The instrument is for use only on circuits that are NOT directly connected to mains. It is NOT intended for measurements on CAT II, CAT III, or CAT IV circuits.**

WARNING **Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.**

WARNING **Ensure that the external circuits do not connect to hazardous voltages above 30 V r.m.s., 42.4 V peak and hazardous voltages above 60 V d.c..**

WARNING **If you energize this instrument by an auto transformer (for voltage reduction or mains isolation), the common terminal must be connected to the earth terminal of the power source.**

WARNING **Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.**

WARNING **Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.**

WARNING **Do not install substitute parts or perform any unauthorized modification to the instrument.**

WARNING **Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.**

WARNING **Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.**

WARNING **Do not use the instrument in a manner not specified by the manufacturer.**

NOTE **Perform self-tests (described on page 90) as acceptance tests when receiving the logic analyzer or when the logic analyzer is repaired. The self-tests check the functional operation of the logic analyzer.**

Safety Symbols

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.

Indicates hazardous voltages and potential for electrical shock.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

The C-tick mark is a registered trademark of the Spectrum Management Agency of Australia. This signifies compliance with the Australia EMC Framework regulations under the terms of the Radio Communication Act of 1992.

CE compliance marking to the EU Safety and EMC Directives.

ISM GRP-1A classification according to the international EMC standard.

ICES/NMB-001 compliance marking to the Canadian EMC standard.

KC certification mark to demonstrate compliance with the South Korean EMC requirements.

South Korean Class A EMC declaration:

This equipment is Class A suitable for professional use and is for use in electromagnetic environments outside of the home.

CSA is the Canadian certification mark to demonstrate compliance with the Safety requirements.

The crossed out wheeled bin symbol indicates that separate collection for waste electric and electronic equipment (WEEE) is required, as obligated by DIRECTIVE 2012/19/EU and other National legislation.

Please refer to about.keysight.com/en/companyinfo/environment/takeback.shtml to understand your Trade in options with Keysight in addition to product takeback instructions.

UK CA

This mark denotes compliance with the essential requirements of the following applicable UK regulations:

- Electromagnetic Compatibility Regulations 2016 No. 1091 (as amended)
- Electrical Equipment (Safety) Regulations 2016 No. 1101 (as amended)
- The Restriction of the Use of Certain Hazardous Substances in Electrical & Electronic Equipment Regulations 2012 No. 3032 (as amended)

Keysight 16860 Series Logic Analyzer - At a Glance

The Keysight Technologies 16860 series logic analyzers are portable logic analyzers that range from 34 to 136 logic acquisition channels, depending on the model.

The 16860-series models provide features such as:

- deeper memory
- ¼ channel 10GHz Timing mode
- deskew of timing traces by individual channels
- single as well as multiple clocks support
- advanced clocking capabilities
- clock hysteresis
- various clock modes such as Master, Dual Sample, Master/Slave, and Demultiplex.

This series of logic analyzers can be used:

- at a higher speed (700MHz to 12.5 MSps) for debug, validation and analysis of DDR and LPDDR memory systems.
- at a lower speed (350MHz to 0 MSps) as a medium to high performance general purpose logic analyzer.

Model Comparison

Keysight Model Number	16861A	16862A	16863A	16864A
Logic acquisition channels	34	68	102	136

Features, Logic Acquisition

- 2 M to 128 M samples of memory depth per channel (depending on memory option), software upgradeable.
- 350 MHz or 700 MHz maximum state clock rate (depending on state speed option), software upgradeable.
- Full Channel Timing Mode at 2.5 GHz sampling with 12.5 GHz Timing Zoom.
- Half Channel Timing Mode at 5.0 GHz sampling with 12.5 GHz Timing Zoom

- Quarter Channel Timing Mode at 10 GHz sampling with 12.5 GHz Timing Zoom
- Eye scan (automatic threshold and sample position setup) feature.
- Single-ended and differential probing support

Features, Mainframe

- Built-in 15 inch color touch screen with 1024 x 768 resolution
- Removable hard drive
- 10/100/1000 Base-T LAN port
- USB 2.0 ports (four total, two on front, two on back)
- USB 3.0 ports (two total, both ports are on the back)
- One PCI expansion slot
- One PCI Express x1 expansion slot
- Windows 7 installation
- Keysight Logic and Protocol Analyzer application which takes the complexity out of making logic analyzer measurements. You can perform all operations directly from one window.

To know about these features in detail, refer to the 16860 series logic analyzer Data Sheet (5992-1723EN) on www.keysight.com and the *Logic and Protocol Analyzer online help* installed with the Logic and Protocol Analyzer software.

Supplied Accessories

- USB mouse
- USB keyboard
- Accessory pouch and power cord

Snap the accessories pouch to the top of the 16860 series logic analyzer. Use it to store probe leads, accessories, or manuals. Use the tie-down straps under the flap to conveniently hold pod cables not in use or during transport.

Optional Accessories

- Probes

Service Strategy

The service strategy for this instrument is the replacement of defective assemblies/parts. This service guide contains information for finding a defective assembly by testing and returning it to Keysight Technologies for all service work, including troubleshooting. Contact your nearest Keysight Technologies Sales Office for more details.

Contacting Keysight Technologies

To locate a sales or service office near you, go to www.keysight.com/find/contactus.

In This Service Guide

This book is the service guide for the 16860 series logic analyzer.

This service guide has seven chapters.

Chapter 1, “General Information” contains information about the instrument, lists accessories for the module, gives specifications and characteristics of the instrument, and provides a list of the equipment required for servicing the instrument.

Chapter 2, “Preparing for Troubleshooting or Performance Testing” tells how to prepare the instrument for use.

Chapter 3, “Testing 16860 Series Logic Analyzers Performance” tells how to verify the 16860 series logic analyzer performance with specifications.

Chapter 4, “Calibrating” contains calibration instructions for the instrument (if required).

Chapter 5, “Troubleshooting” contains explanations of self-tests and flowcharts for troubleshooting the instrument.

Chapter 6, “Removing, Replacing, or Returning 16860 Series Logic Analyzer Assemblies” describes how to replace the instrument and assemblies of the instrument, and how to return these to Keysight Technologies.

Chapter 7, “Replaceable Parts” contains a list of replaceable parts available for 16860 Series Logic Analyzers and how to order these parts.

Contents

1 General Information

This chapter lists the accessories and some of the specifications and characteristics for testing and servicing the 16860 series logic analyzer. See the 16860 Series logic analyzer's online help for a full listing of all specifications and characteristics.

Accessories

One or more of the following accessories, sold separately, are required to set up and operate the 16860 series logic analyzer for testing and servicing it.

Probes, Cables, and Accessories

Refer to the 16860 series logic analyzer Data Sheet (5992-1723EN) on www.keysight.com to get a list of supported interposers, probes, and cables for 16860 series logic analyzer. Details of these interposers, probes, and cables are in their respective user guides available on www.keysight.com.

Software

The 16860 series logic analyzer requires:

- Keysight Logic Analyzer software version 06.30 or higher to configure, control, and use the 16860 series logic analyzer.

Specifications

The specifications are the performance standards against which the product is tested.

Table 1 Maximum State Data Rate Specification for the 16860 Series Logic Analyzers

	350 MHz (Base configuration)	700 MHz (Option 700)	350 MHz (Base configuration)
	Single Clock	Single Clock	Multiple Clocks
Maximum state data rate (spec) [1]	▪ Captures data up to 350 Mbps on either edge of a clock up to 350 MHz ▪ Captures data up to 700 Mbps on either edge of the clock up to 700 MHz	▪ Captures data up to 700 Mbps on both edges of a clock up to 350 MHz ▪ Captures data up to 1400 Mbps on both edges of the clock up to 700 MHz	▪ Captures data up to 700 Mbps on any combination of multiple clocks up to 350 MHz

1.Specification (spec): Represents warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of 5 to 40 °C, unless otherwise stated, and after a 45-minute warm-up period. The specifications include measurement uncertainty.

Characteristics

For a full listing of all specifications and characteristics, see the *Keysight* 16860 series logic analyzer *Data Sheet,* literature part number 5992-1723EN available on Keysight's web site (www.keysight.com).

2 Preparing for Troubleshooting or Performance Testing

This chapter provides instructions for preparing the 16860 series logic analyzer for troubleshooting or servicing it.

Operating Environment

The operating environment specifications are listed in the *Keysight* 16860 series logic analyzer *Data Sheet,* literature part number 5992-1723EN available on Keysight's web site (www.keysight.com).

Note the non-condensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Provide protection against internal condensation.

To apply power

1 Connect the supplied power cord to the instrument and to the power source.

This instrument autodetects the line voltage from 100 VAC to 240 VAC. It is equipped with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the model ordered and the country of destination.

2 Turn on the power switch located on the front panel.

For first-time power up considerations and setup steps, refer to the Installation Guide that came with your instrument. To get the most up-to-date installation guide:

- Go to www.keysight.com.
- Search for 16860 Series Logic Analyzers.
- Look under **Technical Support** and then **Document Library**.

To clean the instrument

If the instrument requires cleaning:

1 Remove power from the instrument.
2 Clean the external surfaces of the instrument with a soft cloth dampened with water.
3 Make sure that the instrument is completely dry before reconnecting it to a power source.

To start the user interface

Start the Keysight Logic and Protocol Analyzer application from the Start menu or using a shortcut.

On the desktop, the Keysight Logic Analyzer icon looks like:

Refer to the Keysight Logic and Protocol Analyzer application's on-line help for information on how to operate the user interface.

To test the 16860 series logic analyzer

The 16860 series logic analyzer does not require an operational accuracy calibration or adjustment. After installing the instrument, you can test and use the instrument.

- If you require a test to verify logic analyzer's performance with the specifications, see "Testing 16860 Series Logic Analyzers Performance" on page 23.
- If you require a test to verify correct instrument operation, see "To run the self-tests" on page 90.
- If the instrument does not operate correctly, see "Troubleshooting" on page 81.

3 Testing 16860 Series Logic Analyzers Performance

This chapter provides information on how to test the performance of the 16860 series logic analyzers module against the specifications listed on page 15.

To ensure the 16860 series logic analyzer is operating as specified, software tests (self-tests) and a manual performance test is done. The logic analyzer is considered performance-verified if all of the software tests pass and the manual performance test meets specifications.

The specifications for the 16860 series logic analyzers define a maximum state data rate at which data can be acquired in state mode. The manual performance test (maximum state data rate test) measures the performance and verifies that the logic analyzer meets these specifications.

This logic analyzer supports 2 modes: Multiple Clocks and Single Clock. This chapter provides information on measuring performance in both of these modes.

Test Strategy

Only specified parameters are tested. Specifications are listed on page 15. The test conditions defined in this procedure ensure that the specified parameters are as good as or better than specifications. Not all channels of the logic analyzer will be tested; a sample of channels is tested. The calibration laboratory may choose to elaborate on these tests and test all channels at their discretion.

NOTE **A 16860 series analyzer that is licensed with the Base state clock option (350MHz) needs to be tested at a Keysight Service Center. The Service Center has the capability to test the analyzer at up to the 1.4Gb/s state speed to ensure that the calibration will remain valid even after upgrading it to the 700MHz license.**

Eye Scan is used to adjust the sampling position on every channel. Eye scan must be used to achieve maximum state data rate performance.

The 16860 series logic analyzer supports 2 modes: Multiple Clocks and Single Clock. Performance of the two clocking modes of the Logic Analyzer will be measured separately. In the multiple clock mode, performance of all 4 clocks will be measured, except for the 16861A only 2 pods. In the single clocking mode, data from up to 8 pods (depending on model) will be verified, one pod at a time.

When the logic analyzer acquires data on both edges of the clock, the generator test frequency is set to half of the acquisition speed.

Test Interval

Test the performance of the 16860 series logic analyzer against its specifications at two-year intervals.

Test Record Description

A Performance Test Record for recording the results of each procedure is provided in this chapter. You may want to make copies of the form, and fill-in a copy each time you test the logic analyzer.

Test Equipment

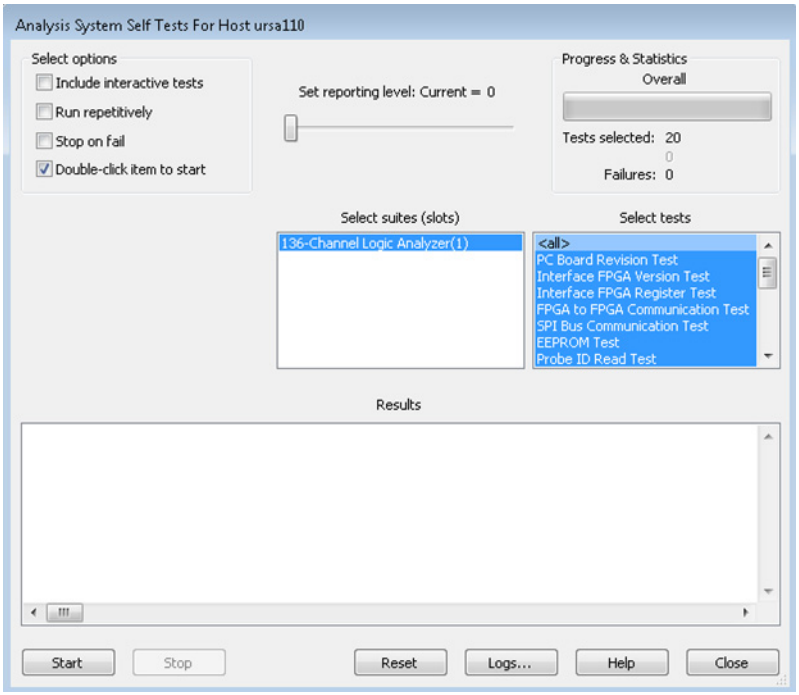
A list of the recommended test equipment is provided. You can use any equipment that satisfies the specifications given. However, the instructions are written with the presumption that you are using the recommended test equipment.

Perform the Self-Tests

Power the 16860 series analyzer on and start the Logic Analyzer application.

1 Before performing the self- tests, disconnect all probes from the logic analyzer.

2 Select **Help**->**Self-Test..**. from the main menu. The **Analysis System Self Tests** window appears.



3 From the **Select suites** list, select the option displayed for 16860. Then, select **All** from the **Select tests** list.

4 Select **Start** to start a complete module self-test. The progress of the self tests is displayed in the **Results** area of the window.

5 When the self-tests are complete, check the **Results** window to ensure that the Result Summary says that all tests passed. If all tests did not pass, refer to "To use the logic acquisition troubleshooting flowcharts" on page 87.

```
---------- Result Summary ----------
All tests passed.

========== End of Analysis System Self Test Run ==========
```

6 Select the **Close** button to close the **Analysis System Self Tests** window.

7 If all self- tests pass, then record "PASS" in the "Logic Analysis System Self-Tests" section of the Performance Test Record (page 77).

Equipment Required for the Performance Test

The following equipment is required for the performance test procedure.

Table 2 Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Pulse Generator (Qty: 1)	≥ 800 MHz, two channels, differential outputs, 150-180 ps rise/fall time (if faster, use transition time converters)	Keysight 81134A or equivalent
150 ps Transition Time Converter (Qty 4)	Required if pulse generator's rise time is less than 150 ps. (Pulse generator conditions: Voffset=1V, δV=250 mV.) Required for 81134A	Keysight 15435A
Flying Lead Probe Set (Qty 2)	A combination of U4201A & E5382A can be used.	Keysight U4203A
SMA/Flying Lead test connectors, (f) SMA to (f) SMA to Flying Lead Probe (Qty 4)	no substitute	See "Assemble the SMA/Flying Lead Test Connectors" on page 27

Assemble the SMA/Flying Lead Test Connectors

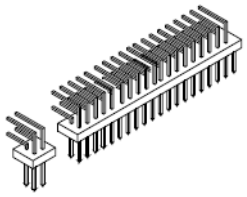
The SMA/Flying Lead test connectors provide a high-bandwidth connection between the logic analyzer and the test equipment. The following procedure explains how to fabricate the four required test connectors.

Table 3 Materials Required for SMA/Flying Lead Test Connectors

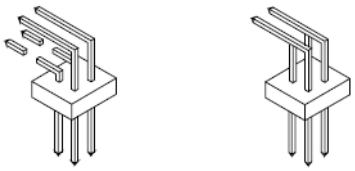
Material	Critical Specification	Recommended Model/Part
SMA Board Mount Connector (Qty 8)		Cinch 142-0701-801 (see www.cinch.com)
Pin Strip Header (Qty 1, which will be separated)	0.100" X 0.100" Pin Strip Header, right angle, pin length 0.230", two rows, 0.110" solder tails, 2 X 40 contacts	3M 2380-5121TG or similar 2- row with 0.1" pin spacing
SMA 50 ohm terminators (Qty 4)	Minimum bandwidth 2 GHz	Cinch 142-0801-866 50 ohm Dummy Load Plug or similar
SMA m-m adapter (Qty 4)		Cinch 142-0901-811 SMA Plug to Plug or similar

1 Prepare the pin strip header:

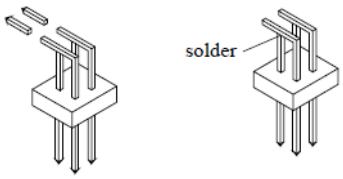
a Cut or cleanly break a 2 x 2 section from the pin strip.



b Trim about 1.5 mm from the pin strip inner leads and straighten them so that they touch the outer leads.



c Trim about 2.5 mm from the outer leads.

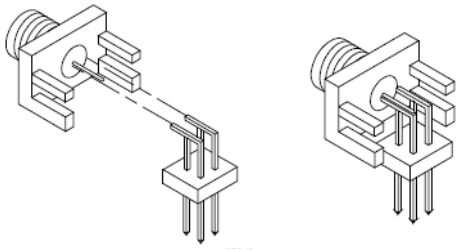


d Using a very small amount of solder, tack each inner lead to each outer lead at the point where they are touching.

2 Solder the pin strip to the SMA board mount connector:

a Solder the leads on the left side of the pin strip to the center conductor of the SMA connector as shown in the diagram below.

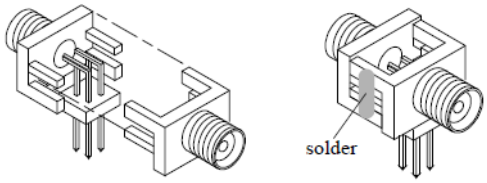
b Solder the leads on the right side of the pin strip to the inside of the SMA connector's frame as shown in the diagram below. Use a small amount of solder.



3 Attach the second SMA board mount connector:

a Re-heat the solder connection made in the previous step, and attach the second SMA connector, as shown in the diagram below. Note that the second SMA connector is upside-down, compared to the first. Add a little solder to make a good connection.

b Solder the center conductor of the second SMA connector to the center conductor of the first SMA connector and the leads on the left side of the pin strip.



c Rotate the assembly 180 degrees and solder the two SMA board mount connector frames together.

4 Check your work:

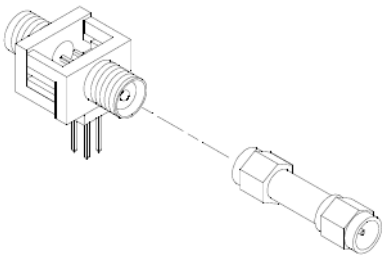
a Ensure that the following four points have continuity between them: The two pins on the left side of the pin strip, and the center conductors of each SMA connector.

b Ensure that there is continuity between each of the two pins on the right side of the pin strip, and the SMA connector frames.

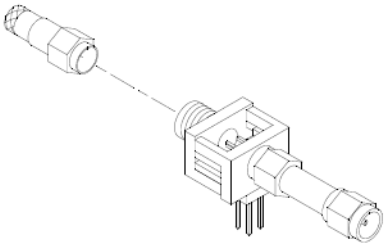
c Ensure that there is NO continuity between the SMA connector center conductor and the SMA connector frame (ground).

5 Finish creating the test connectors:

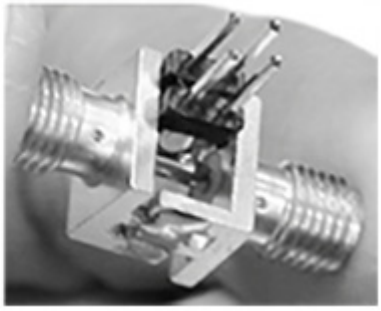
a Attach an SMA m-m adapter to one end of each of the four SMA/Flying Lead test connectors.



b Attach a 50 ohm terminator to the other end of the four SMA/Flying Lead test connectors.



c The finished test connector is shown in the pictures below.

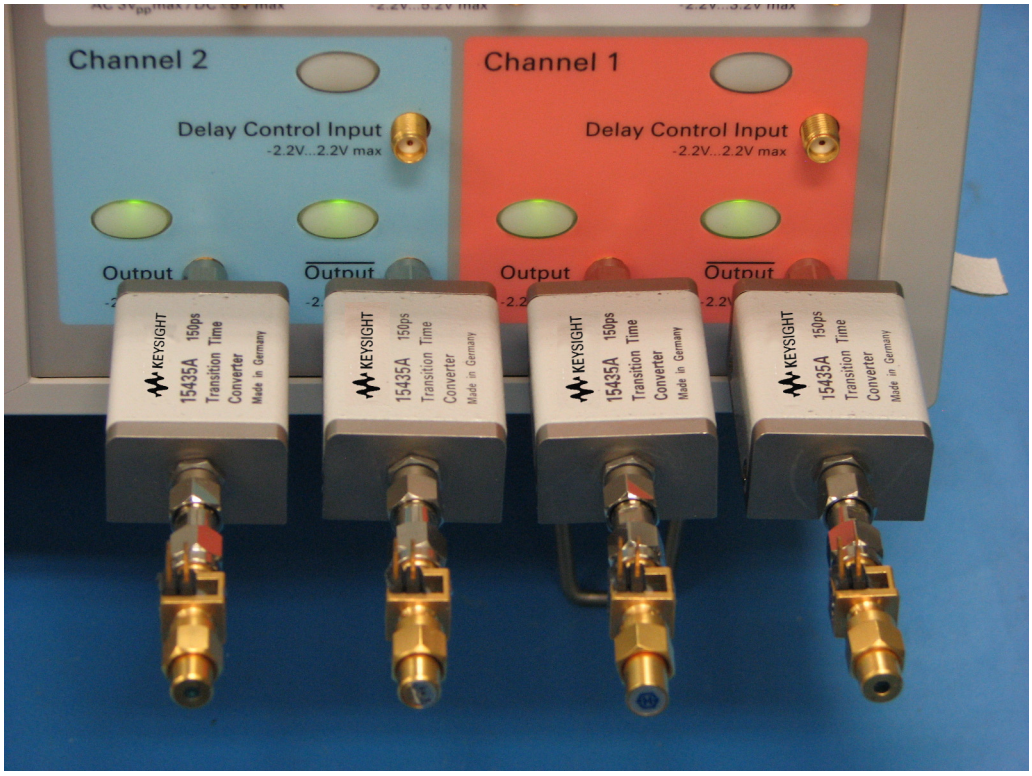


Set Up the Test Equipment

This section explains how to set up the test equipment for the maximum state data rate test.

1 Connect Transition Time Converters (if required) to each of the four outputs of the pulse generator: Channel 1 OUTPUT, Channel 1 OUTPUT (not), Channel 2 OUTPUT, Channel 2 OUTPUT (not).

2 Connect the four SMA/Flying Lead test connectors (see "Assemble the SMA/Flying Lead Test Connectors" on page 27) with 50 ohm terminators to the Transition Time Converters on the 4 pulse generator outputs. (If Transition Time Converters are not required, connect the SMA/Flying Lead test connectors directly to the pulse generator outputs.)



3 Turn on the Pulse Generator. Let all of the test equipment and the logic analyzer warm up for 30 minutes before beginning any test.

4 Load the default configuration into the 81134A Pulse Generator.

- Select Main
- Hit Recall
- Press 0

5 Setup the pulse generator according to the following.

a Set the frequency of the pulse generator:

In this test procedure, the logic analyzer uses both edges of the clock to acquire data. The test frequency is half the test clock rate because data is acquired on both the rising edge and the falling edge of the clock. For the multiple clocks mode, set the frequency to:

- Base Option: Temporarily License the analyzer to full speed and test at 700 Mb/s plus 2% (714 Mb/s). Set the generator to half this or 357 MHz.

- Option 700: Test at 700 Mb/s plus 2% (714 Mb/s). Set the generator to half this or 357 MHz.

This includes the frequency uncertainty of the pulse generator, cabling, and a test margin. If you are using an 81134A pulse generator, the frequency accuracy is ±0.005% of setting.

b Set the rest of the pulse generator parameters to the values shown in the following tables.

Table 4 81134A Pulse Generator Setup

Main	Channel 1	Channel 2
Mode: Pulse/Pattern	Mode: Square ÷ 1	Mode: Square ÷ 1
Freq: set in previous step	**Timing**	**Timing**
Clock Internal	Delay Ctrl Input Off	Delay Ctrl Input Off
	Delay 0 ps	Delay 0 ps
	Pulse Perf: Normal	Pulse Perf: Normal
	Deskew: 0 ps	Deskew: 0 ps
	Levels: Normal, Custom	**Levels: Normal, Custom**
	Ampl: 450 mV	Ampl: 450 mV
	Offset: 0 mV	Offset: 0 mV
	Term Voltage: 0 mV	Term Voltage: 0 mV
	Limit to current Levels: unselected	Limit to current Levels: unselected
	Output: Enable (LED on)	Output: Enable (LED on)
	$\overline{\text{Output}}$: Enable (LED on)	$\overline{\text{Output}}$: : Enable (LED on)


Mode
Pulse/Pattern
Freq
357.000000 MHz
Period
2.80112045 ns
Clock
Internal
Clock In
Start In
Trig Out
Ch 2
Square
Ch 1
Square
Channel 1
Square
Freq. Divider
1
Out
Out_
Ch 2
Timing
Delay Ctrl Input Off
Delay
0 ps
DCycle
50 %
Pulse Perf.
Normal
Deskew
0 ps
Levels
Normal
Custom
Ampl
450 mV
Offset
0 mV
Term. Voltage
0 mV
Limit to current Levels
Main
Channel
Data
Aux
Config

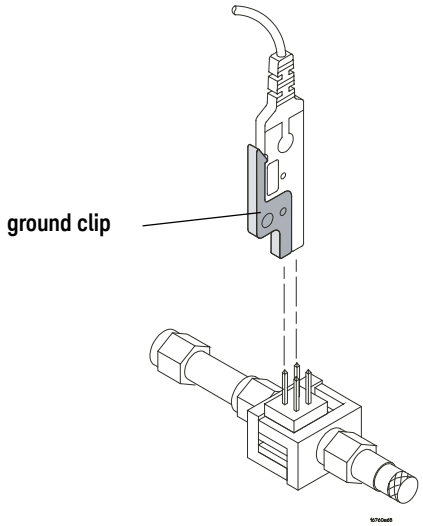
Connect the Test Equipment

Connect the Logic Analyzer Pod to the Pulse Generator

1 Connect one U4203A Flying Lead Probe Set to Pods 1/2 of the 16860 series logic analyzer.

2 If not a 16861A, connect one U4203A Flying Lead Probe Set to Pods 3/4 of the analyzer.

3 Connect the Pod 1 U4203A Flying Lead Probe Set's CLK lead to the pin strip of the SMA/Flying Lead connector at the pulse generator's Channel 1 OUTPUT.



NOTE **On all connections, be sure to use the black ground clip (supplied with the U4203A Flying Lead Probe Set) and orient the leads so that the black clip is connected to one of the SMA/Flying Lead connector's ground pins!**

4 Connect the Pod 1 U4203A Flying Lead Probe Set's CLK (NOT) lead to the SMA/Flying Lead connector at the pulse generator's Channel 1 OUTPUT (NOT). Again, be sure to use the black ground clip and orient the leads so that the black clip is connected to ground.

5 Connect the Pod 1 U4203A Flying Lead Probe Set's bits 2 and 10 to the SMA/Flying Lead test connector's pin strip connector at the pulse generator's Channel 2 OUTPUT.

6 Connect the Pod 1 U4203A Flying Lead Probe Set's bits 6 and 14 to the SMA/Flying Lead test connector's pin strip connector at the pulse generator's Channel 2 OUTPUT (NOT).


81134A
Clock Input
Start Input
Trigger Out
Channel 2
Delay Control Input
Output
KEYSIGHT
15435A

Test the 16860 series Logic Analyzer

The following sections explain how to measure the maximum state data rate.

1 Record the logic analyzer's model and serial number in the Performance Test Record (see page 77). Record your work order number (if applicable) and today's date.

2 Record the test equipment information in the “Test Equipment Used” section of the Performance Test Record.

3 Turn on the frame.

NOTE **Before testing the performance of the logic analyzer, warm-up the logic analyzer and the test equipment for 30 minutes.**

a Plug in the power cord to the power connector on the rear panel of the logic analyzer.

b Connect a key board and a mouse to the frame.

c Press the Standby (Power) button on the front panel of the logic analyzer to power on the logic analyzer.

While the logic analyzer is booting, observe for the following:

- Ensure all of the installed memory is recognized.
- Any error messages.
- Interrupt of the boot process with or without error message.

4 During initialization, check for any failures.

If an error or an interrupt occurs, refer to the chapter “Troubleshooting" on page 81.

5 Start the Keysight Logic Analyzer application if it is not started already.

Create Test Configuration Files

The test consists of multiple setups to test all the various analyzer modes. To make this easier, 4 configuration files will be created. The configuration files will then be used as starting points for the measurement setups.

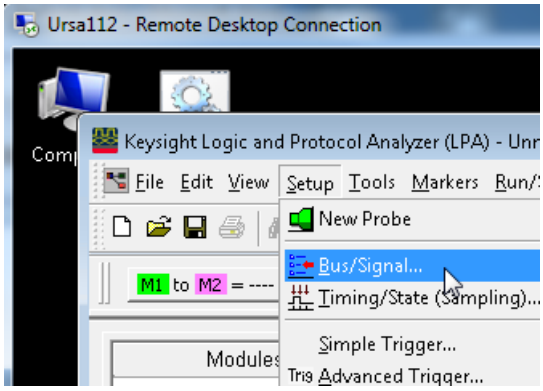
The analyzer has two state modes: Multiple Clocks and Single Clock. Two configuration files will be created for each of these modes. One for finding the maximum clock frequency (no Marker) and another to verify that the data is correct (with Marker).

Create Configuration File 1 - Multiple Clocks (no Marker)

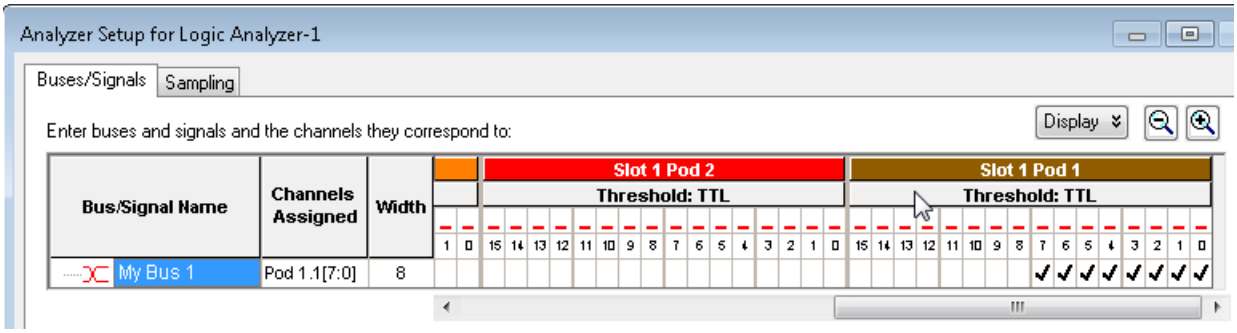
1 Ensure that there is a U4203A connected to Pods 1 and 2. If Pods 3 and 4 exist, connect a U4203A to these pods also.

2 In the Keysight Logic and Protocol Analyzer application, choose **File** > **New**. This puts the logic analyzer into its initial state.

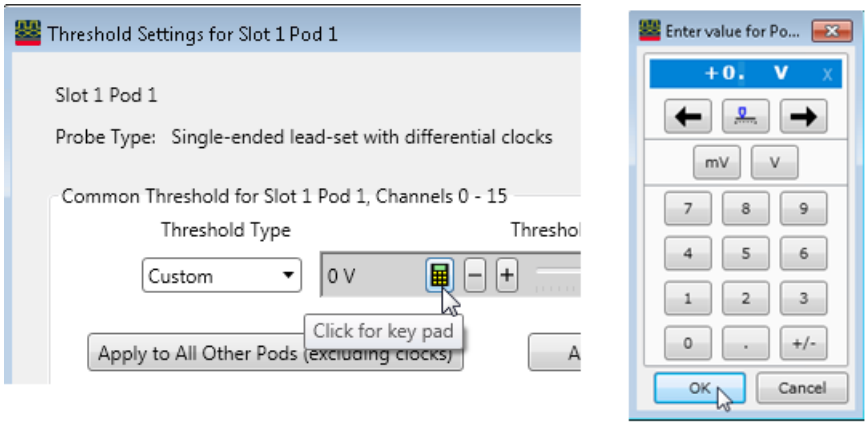
3 From the main drop down menu, select **Setup** then select **Bus/Signal**. The **Analyzer Setup** dialog is displayed.



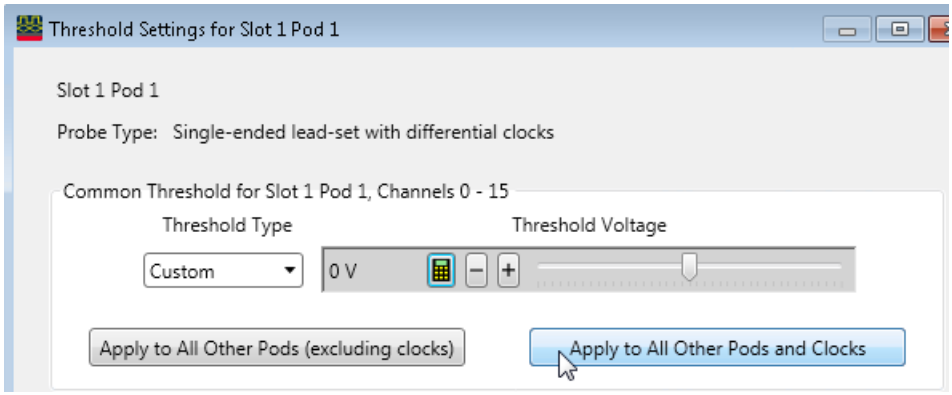
4 In the Analyzer Setup dialog, click the **Threshold** button for Pod 1.



5 The **Threshold Setting** dialog is displayed. Set the Threshold to **0 V**.

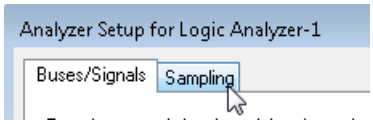


6 Apply this to all Pods and Clocks by clicking the **Apply to All Other Pods and Clocks** button.

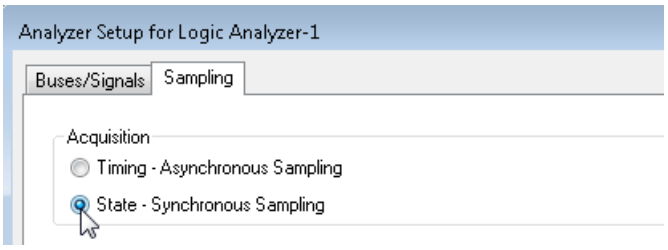


7 Click **Done** to close the Threshold dialog.

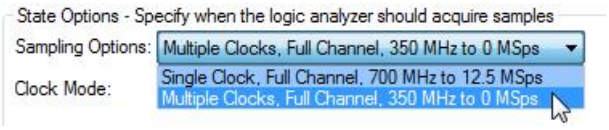
8 Select the **Sampling** tab.



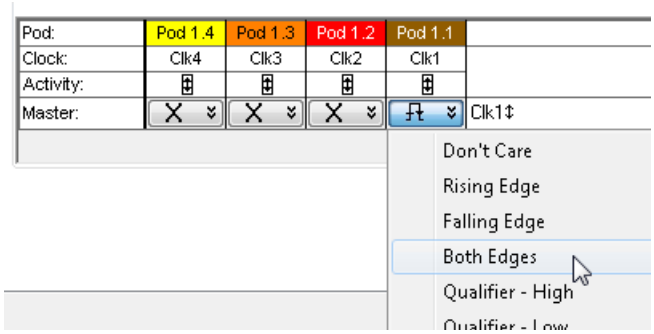
9 In the **Sampling** dialog, set the Acquisition mode to **State - Synchronous Sampling**.



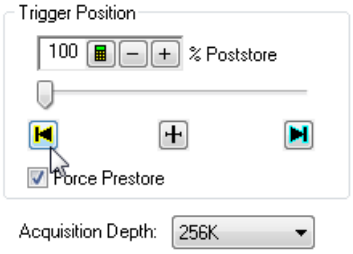
10 Set the State Options to **Multiple Clocks**.



11 Set Pod1 Clock to **Both Edges**. Set other clocks to **Don't Care**.

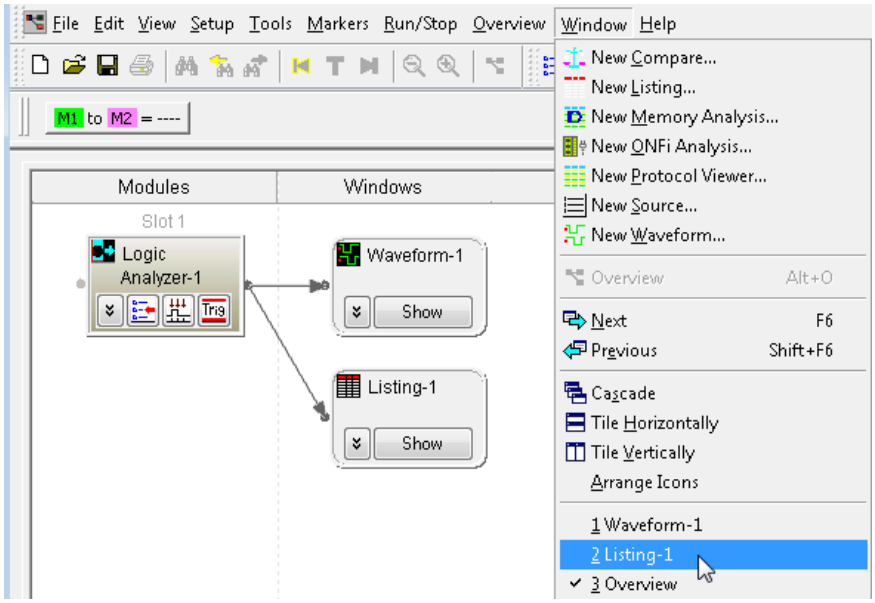


12 Set the Trigger Position to **100% Poststore**. Set Acquisition Depth to **256K**.

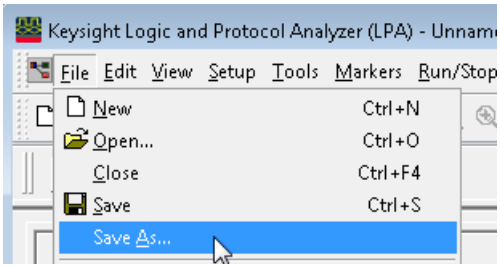


13 Close the Sampling dialog by clicking **OK**.

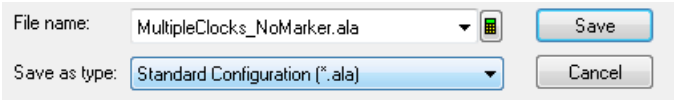
14 Select the Listing Window by selecting **Window** and then **Listing**.



15 Save the configuration by selecting **File** then **Save As ...**.

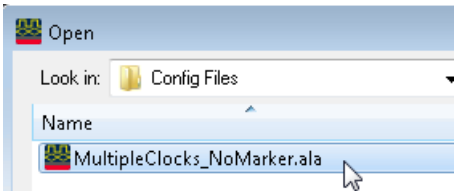


16 In the **Save As** dialog, type the file name **MultipleClocks_NoMarker.ala**. For file options, select **Setup Only**. Then click **Save**.



Create Configuration File 2 - Multiple Clocks (with Marker)

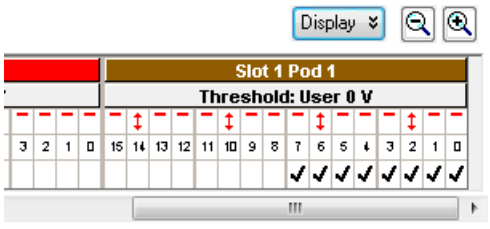
1 Start with the **MultipleClocks_NoMarker** configuration file. Select **File** then **Open**. In the Open dialog select the file and then open. If asked about saving the current configuration, click **No**.

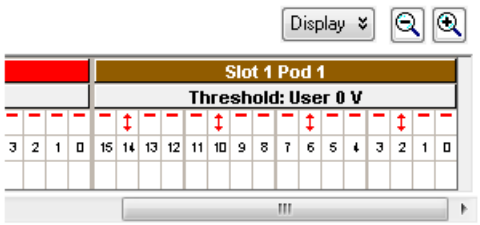


2 Ensure that there is a U4203A connected to Pods 1 and 2. If Pods 3 and 4 exist, connect a U4203A to these pods. The Pod 1 leads should be connected to the generator as described above.

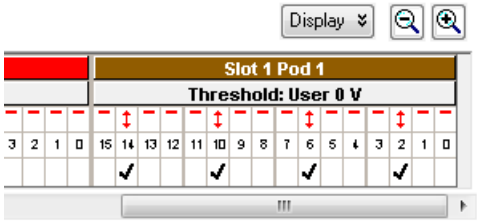
3 From the main drop down menu, select **Setup** and then select **Bus/Signal.** The **Analyzer Setup** dialog is displayed.

4 The activity indicators now show activity on the channels that are connected to the pulse generator. Un-assign all channels. You can do this quickly by clicking on the left-most check mark and dragging to the right across all of the other check marks.



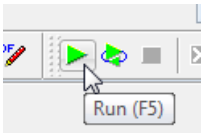


5 Assign bits that are connected, Bits 2, 6, 10, 14.

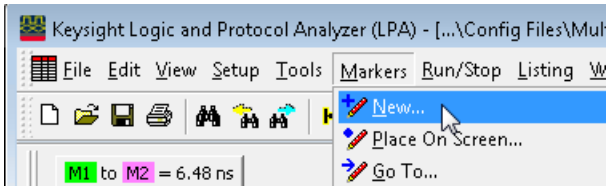


6 Close the Analyzer Setup Dialog Window by clicking **OK**.

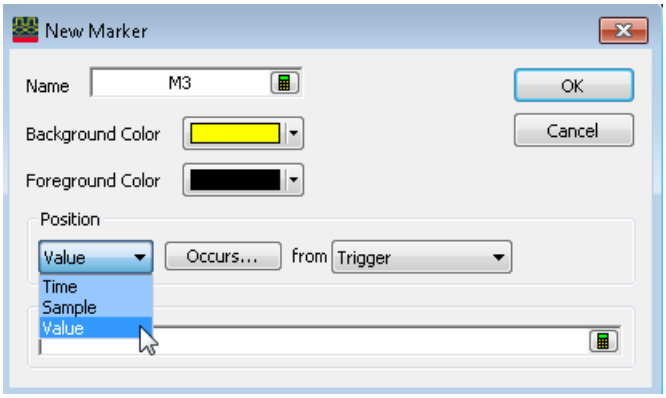
7 Click the **Run** button. The analyzer needs to have data before the Marker can be added.



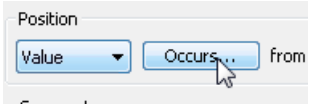
8 Add a new marker by selecting **Marker** and then **New**.



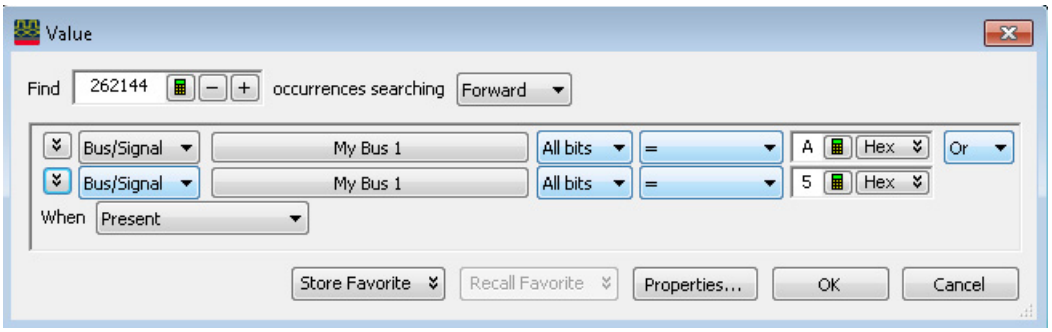
9 In the **New Marker** dialog, change the Position information. Select **Value** in the drop down.



10 Open the Value dialog by clicking the **Occurs** button.



11 In the **Value** dialog, create a marker that looks like the following.

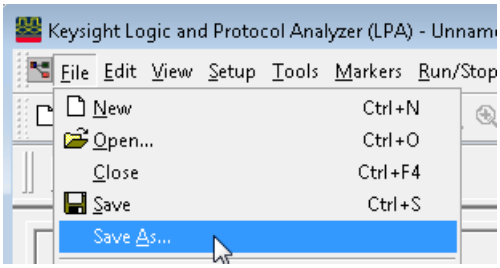


12 In the Value dialog, select the **Properties**... button.

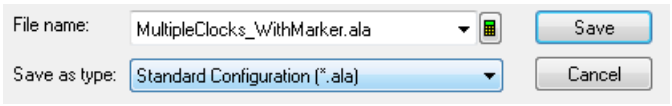
13 In the **Value Properties** dialog, select **Stop repetitive run when value is not found**.

14 Close the Marker dialogs by clicking OK several times.

15 Save the configuration by selecting **File** then **Save As ...**.

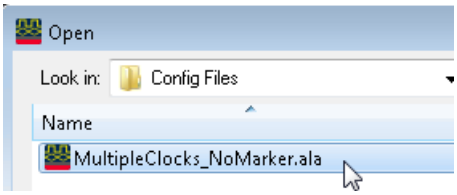


16 In the **Save As** dialog, type the file name **MultipleClocks_WithMarker.ala**. For file options select **Setup Only**. Then click **Save**.



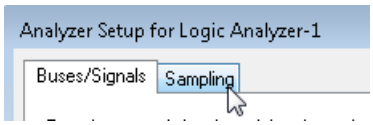
Create Configuration File 3 - Single Clock (no Marker)

1 Start with the **MultipleClocks_NoMarker** configuration file. Select **File** then **Open**. In the **Open** dialog select the file and then open. If asked about saving the current configuration, click **No**.

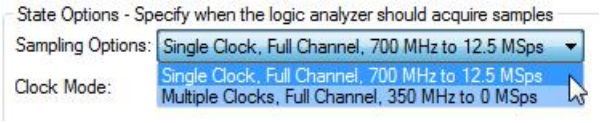


2 Ensure that there is a U4203A connected to Pods 1 and 2. If Pods 3 and 4 exist, connect a U4203A to these pods also. The Pod 1 leads should be connected to the generator as described above.

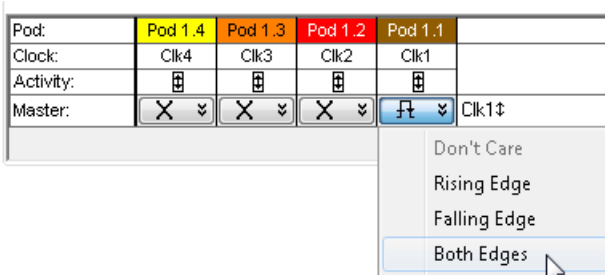
3 Click the **Analyzer Setup > Sampling** tab.



4 In the **State Options** section, change the **Sampling** options to **Single Clock**.

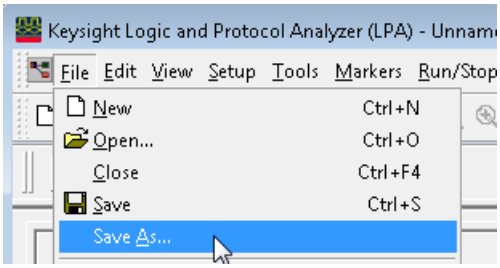


5 In the clock selection area, change the Pod 1 clock to **Both Edges**.

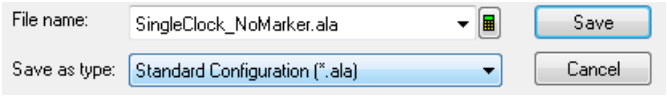


6 Close the dialog by clicking **OK**.

7 Save the configuration by selecting **File** then **Save As ...**.

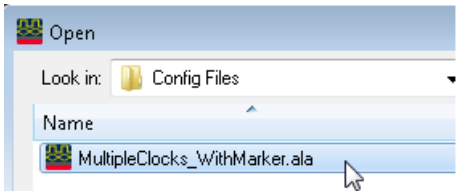


8 In the **Save As** dialog, type the file name **SingleClock_NoMarker.ala**. For file options, select **Setup Only**. Then click **Save**.



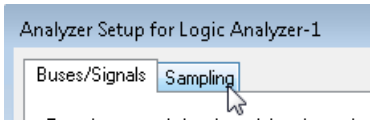
Create Configuration File 4 - Single Clock with Marker

1 Start with the **MultipleClocks_WithMarker** configuration file. Select **File** and then **Open**. In the Open dialog select the file then open. If asked about saving the current configuration, click **No**.

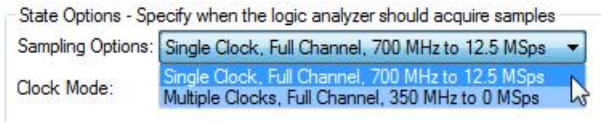


2 Ensure that there is a U4203A connected to Pods 1 and 2. If Pods 3 and 4 exist, connect a U4203A to these pods. The Pod 1 leads should be connected to the generator as described above.

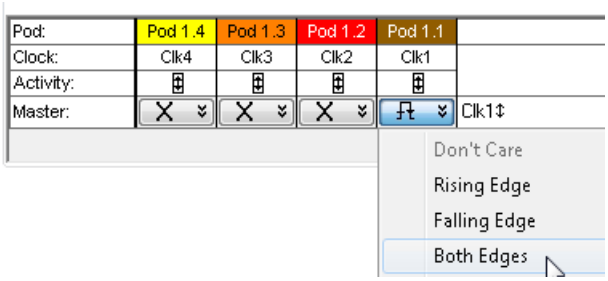
3 Open the **Analyzer Setup Sampling** tab.



4 In the **State Options** section, change the Sampling options to **Single Clock**.

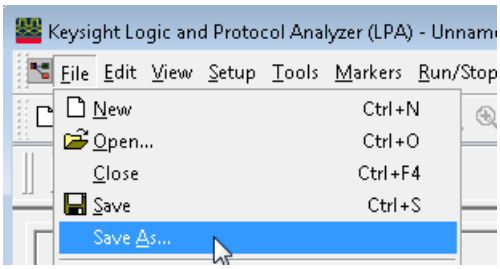


5 In the clock selection area, change the Pod 1 clock to **Both Edges**.

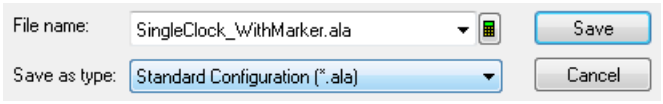


6 Close the dialog by clicking **OK**.

7 Save the configuration by selecting **File** then **Save As ...**.



8 In the **Save As** dialog, type the file name **SingleClock_WithMarker.ala**. For file options, select **Setup Only**. Then click **Save**.



Determine Maximum Data Rate for Multiple Clocks Mode

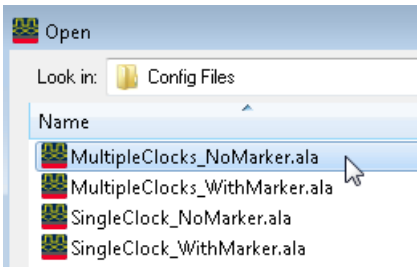
The multiple clocks test measures the maximum data rate of each of the four clocks used for this mode: Pod1, Pod2, Pod3, Pod4. Each Pod / clock is measured separately. The measurement is done in two parts:

- The first part is to determine the maximum clock rate that the analyzer will run at.
- The second part is to verify that the data captured by the analyzer is correct; markers are used to verify the data patterns.

Pod 1 Clock - Maximum Clock Rate

For this test, Pod 1 clock should be connected to Channel 1 of the 81134A.

1 Load the **MultipleClocks_NoMarker.ala** configuration file. If asked to save the current configuration file, click **No**.



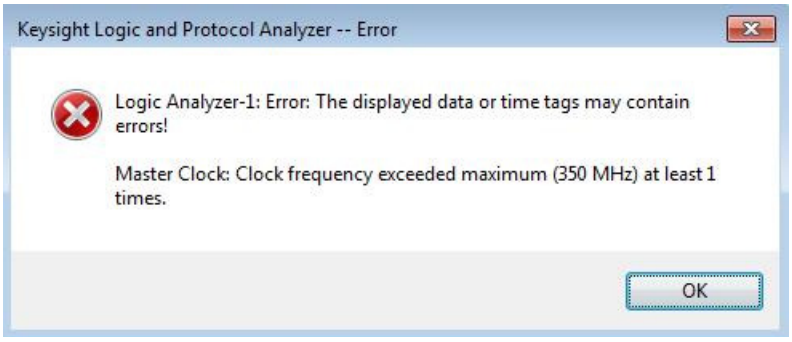
2 Verify that the Generator is set to 357 MHz as a starting point.

3 Click the **Run Repetitive** toolbar button to start a repetitive run on the logic analyzer for acquiring data repeatedly.

4 Acquired data will start appearing in the Listing window.

5 Start increasing the frequency on the pulse generator by 1 MHz increments while simultaneously observing the logic analyzer data acquisition status.

6 Continue increasing the generator frequency until the logic analyzer displays an error that the data could not be displayed, or the clock is too fast. It is possible that the error is caused by noise introduced as the generator frequency is changed.



7 Without changing the frequency, clear the message by clicking **OK**. Then click the **Run Repetitive** toolbar button to start a repetitive run again at the same frequency. Running at the same frequency checks to see if the error message was caused by noise due to the changing of the generator frequency.

8 If the analyzer displays an error again, lower the frequency by 1MHz and run again. If the test does not display an error, increase the frequency by 1 MHz and run again.

9 Continue changing the frequency and running unit the frequency can no longer be increased and the error message not displayed.

10 Set the generator to the highest frequency that did not cause an error.

11 Click **Run Repetitive**  .

12 Wait for logic analyzer to complete 100 acquisitions at the new pulse generator frequency without displaying any error. If an error is displayed, decrease the pulse generator frequency by 1 MHz and then again wait for 100 acquisitions at this new frequency without any error. Repeat this step until you get 100 acquisitions without any error display.

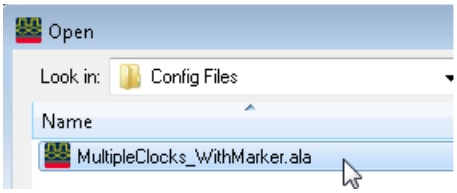
13 Click the **Stop**  toolbar button to stop the data acquisition.

14 Note the generator frequency setting this will be used in the next section to verify the data rate.

Pod 1 Clock - Setup for Maximum Data Rate

To measure the maximum data rate, the starting frequency will be the frequency found in the section above. A new configuration file will be used that has a marker setup to verify that the data patterns are correct. To ensure that the data is sampled correctly, the sample position needs to be set. Eye Scan is used to set the sample points of all the data to the same eye., The following section describes how to do use Eye Scan to do this. This same process will be used during all the other data verification steps later in the procedure.

1 Load the **MultipleClocks_WithMarker.ala** configuration file. If asked to save the current configuration file click **No**.



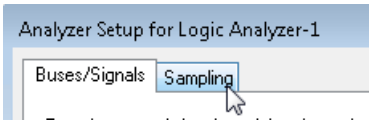
2 Verify that the Generator is set to the frequency found in the last section as a starting point.

3 Adjust the sample position using the procedure in the following section.

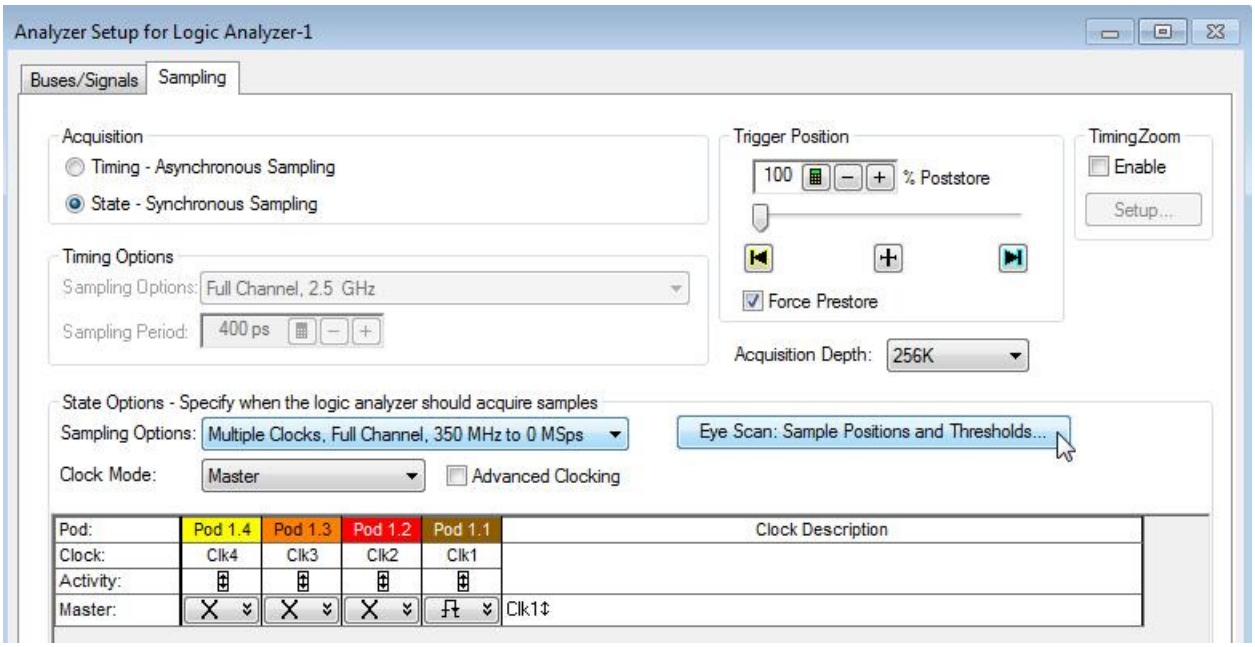
Adjust Sampling Positions using Eye Scan

This Eye Scan procedure will be used before each of the data rate verification steps. This procedure should be followed any time the setup or frequency is changed.

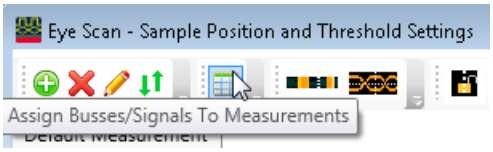
1 Open the sampling setup window.



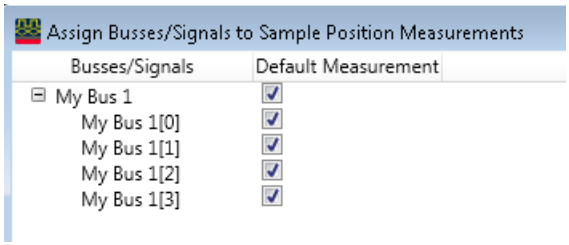
2 Select the **Eye Scan: Sample Positions and Thresholds...** button. The Eye Scan - Sample Positions and Threshold Settings dialog appears.



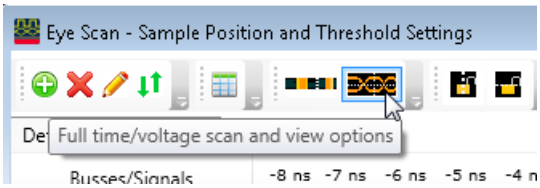
3 Select the **Assign Busses/Signals**.



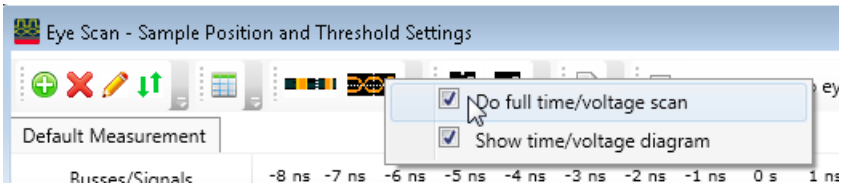
4 In the Buses/Signals section of the dialog, ensure that the check box next to My Bus 1 is checked and the 4 data bits 0-3. Click **OK**.



5 Select **Full time/voltage scan**.

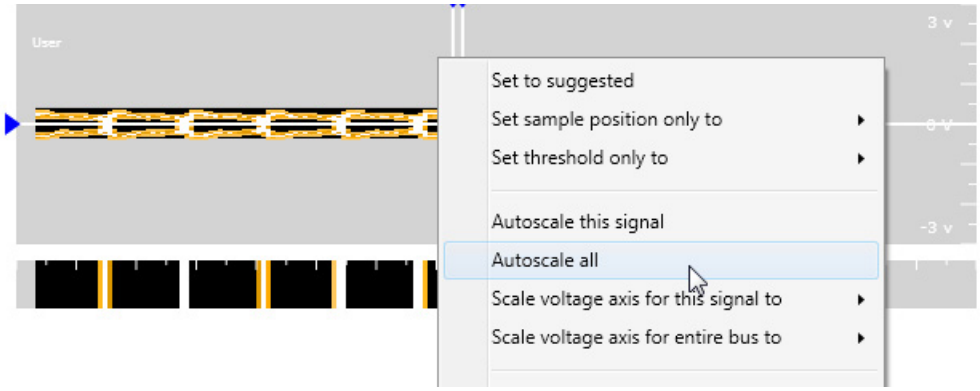


6 In the dialog, set **Do full time/voltage scan** and **Show time/voltage diagram**.

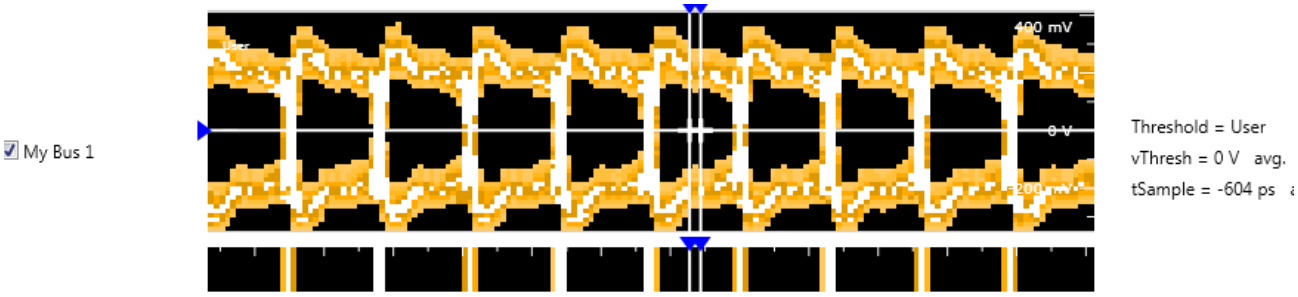


7 Run Eye Scan by clicking the **Run This Measurement** button.

8 If the scan does not fill the scan area, right click in the scan area and select **Autoscale all**.

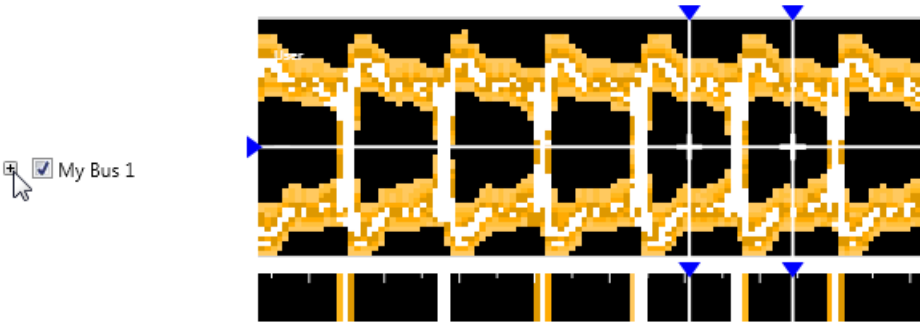


The waveform should now fill the Eye Scan area.

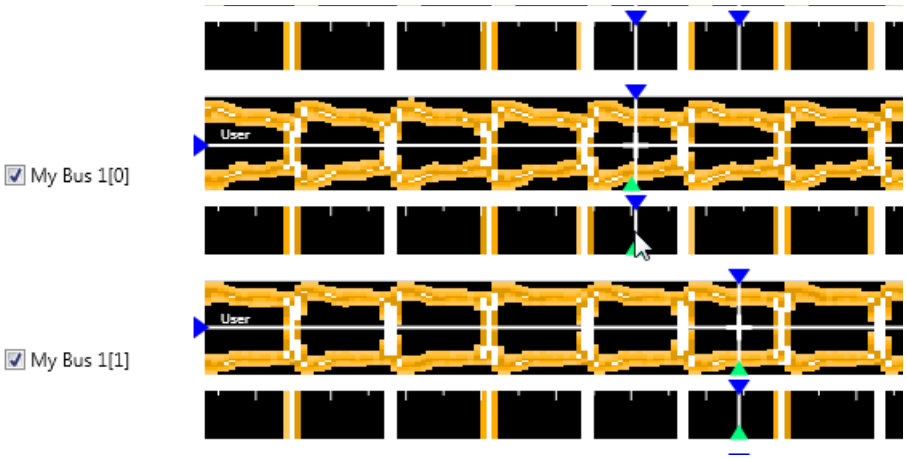


9 Move the sample position of all 4 data bits into the Eye between 0 and -1ns. Using the mouse, grab the vertical lines and move them into the correct eye.

10 If all sample positions are not in the same eye, then click the Plus sign to expand My Bus 1.

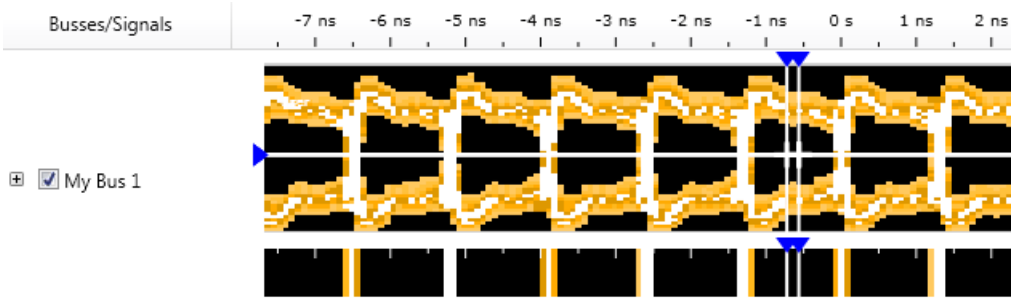


11 Use the mouse to grab the bits that are not in the correct eye and move them into the right eye.



12 After all bit sample positions are in the correct eye, right-click in the My Bus 1 Scan area and select **Set to Suggested**.

13 After setting to suggested, all bits should be centered in their own eye near -.5 ns.



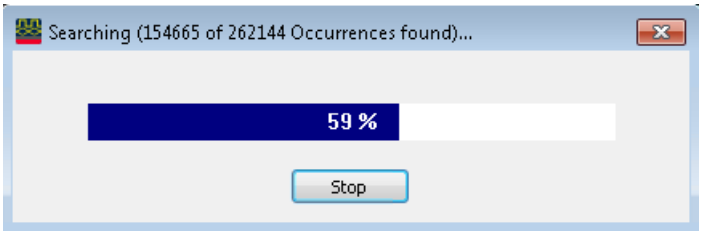
14 Close Eye Scan by clicking **OK**.

15 Close the Sampling dialog by clicking **OK**.

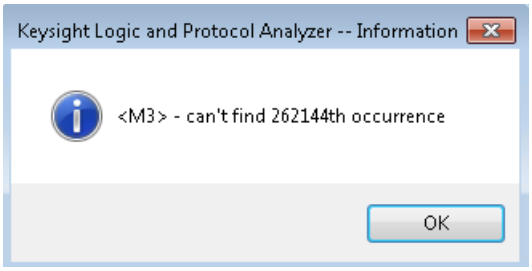
Pod 1 Clock - Measuring Maximum Data Rate

After setting the sample positions, the data capture can now be verified at the frequency found in the clock rate section. The configuration file that was loaded earlier with markers is set up to verify the data pattern. If bad data is found, the marker will cause the repetitive run to stop.

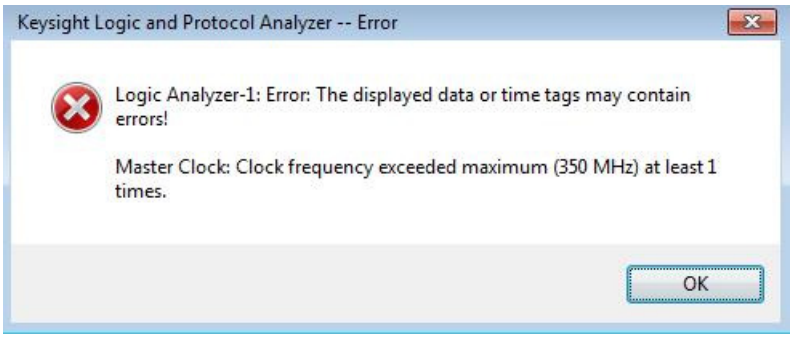
1 Select the **Run Repetitive**  icon. Let the logic analyzer run for about 1 minute. The analyzer will acquire data and the Listing Window will continuously update. A marker search window will appear and show progress.



2 If incorrect data is found, the following window will appear. The data in the listing window should be A's & 5's.



3 If the clock rate is too high, this error message may occur.



4 If either of these messages occur, the generator frequency should be lowered, Eye Scan run and the test rerun.

5 Lower the generator frequency by 1 MHz and rerun the test.

NOTE

If bad data is found or an error message occurs, decrease the pulse generator frequency by 1 MHz and rerun Eye Scan to find the sample position. Run the analyzer again looking for the appropriate number of A's and 5's. After 1 minute, stop the analyzer. Repeat these steps until you get acquisitions without any error display.

6 After the analyzer runs for about 1 minute, select the **Stop** button to stop the acquisition. If the "can't find occurrence" window does not appear, then the analyzer has found good data.

7 For this Pod's Clock, record the generator frequency and the Data Rate in the Maximum State Data Rate section of the "Performance Test Record" on page 77. Remember that the data rate is twice the generator frequency.

Pod 2 Clock - Maximum Clock Rate

1 Load the **MultipleClocks_NoMarker.ala** configuration file. If asked to save the current configuration file, click **No**.

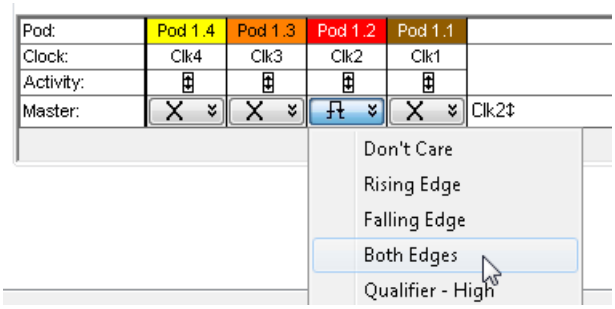
2 Disconnect the U4203A Flying Lead Probe Set from channels 1 & 2 of the 81134A pulse generator output (Bits 2, 6, 10, 14) and clock leads.

3 Connect the probe set from Pod 2 of logic analyzer to the pulse generator channels 1 & 2 output.

- Clock to Channel 1 Output
- Clock (NOT) Channel 1 Output (not)
- Bits 2 & 10 to Channel 2 Output
- Bits 6 & 14 to Channel 2 Output (not)

4 Open the Sampling Tab in the Analyzer Setup dialog by clicking the **Sampling Setup** Icon.

5 In the clock assignment area, set Pod 1 Clock to **Don't Care** and set Pod 2 Clock to **Both Edges**.



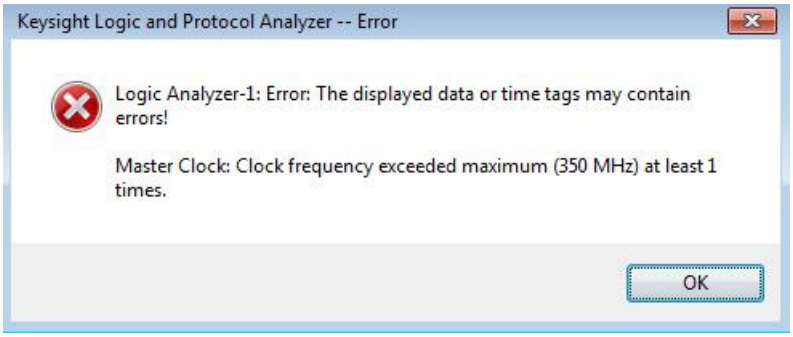
6 Close the dialog by clicking **OK**.

7 Set the generator frequency to 357 MHz as a starting point.

8 Click the **Run Repetitive** toolbar button to start a repetitive run on the logic analyzer for acquiring data repeatedly.Acquired data will start appearing in the Listing window.

9 Start increasing the frequency on the pulse generator by 1 MHz increments while simultaneously observing the logic analyzer data acquisition status.

10 Continue increasing the generator frequency until the logic analyzer displays an error that the data could not be displayed, or the clock is too fast. It is possible that the error is caused by noise introduced as the generator frequency is changed.



11 Without changing the frequency, clear the message by clicking OK. Then click the **Run Repetitive** toolbar button to start a repetitive run again at the same frequency. Running at the same frequency checks to see if the error message was caused by noise due to the changing of the generator frequency.

12 If the analyzer displays an error again, lower the frequency by 1MHz and run again. If the test does not display an error increase the frequency by 1 MHz and run again.

13 Continue changing the frequency and running unit the frequency can no longer be increased and the error message not displayed.

14 Set the generator to the highest frequency that did not cause an error.

15 Click **Run Repetitive** .

16 Wait for logic analyzer to complete 100 acquisitions at the new pulse generator frequency without displaying any error. If an error is displayed, decrease the pulse generator frequency by 1 MHz and then again wait for 100 acquisitions at this new frequency without any error. Repeat this step until you get 100 acquisitions without any error display.

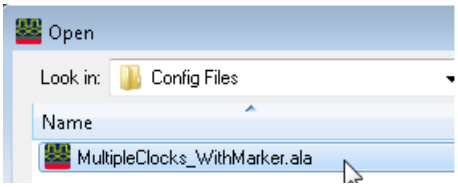
17 Click the **Stop** toolbar button to stop the data acquisition.

18 Note the generator frequency setting this will be used in the next section to verify the data rate.

Pod 2 Clock - Setup for Maximum Data Rate

1 Verify that the Generator is set to the frequency found in the last section as a starting point.

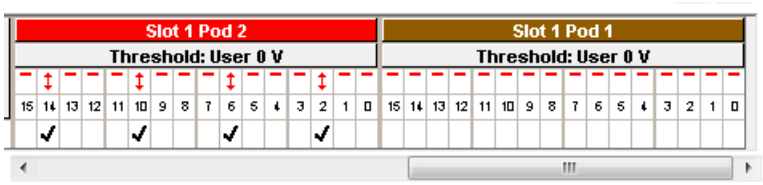
2 Load the **MultipleClocks_WithMarker.ala** configuration file. If asked to save the current configuration file, click **No**.



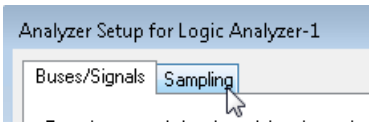
3 Open the **Bus/Signal Setup** dialog by clicking the **Setup** Icon in the tool bar.

4 Unassign the data bits from Pod1.

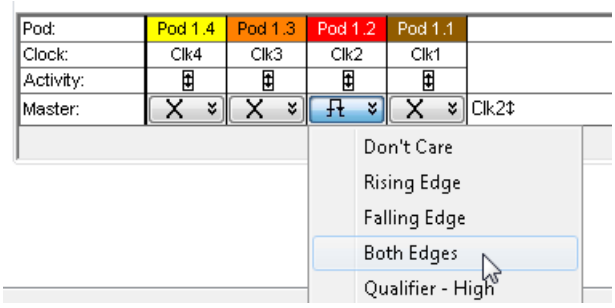
5 Assign bits 2, 6, 10, and 14 of Pod 2.



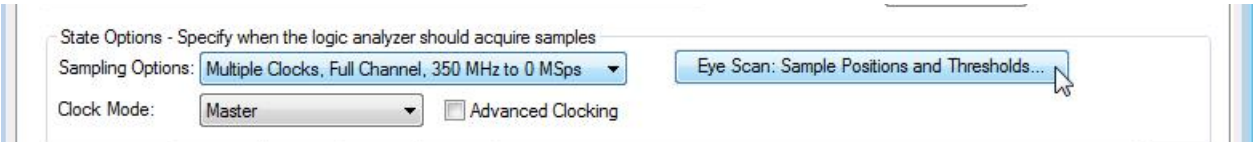
6 Open the **Sampling** tab.



7 In the clock assignment area, set Pod 1 Clock to **Don't Care** and set Pod 2 Clock to **Both Edges**.



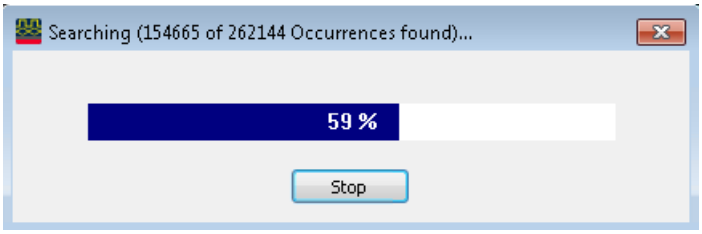
8 Adjust the sample position using the procedure described earlier by clicking the **Eye Scan: Sample Position and Thresholds** button.



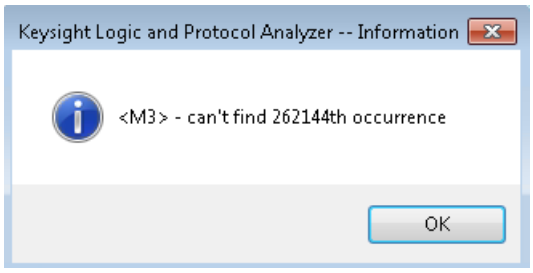
9 Close the dialog boxes by clicking **OK**.

Pod 2 Clock - Measuring Maximum Data Rate

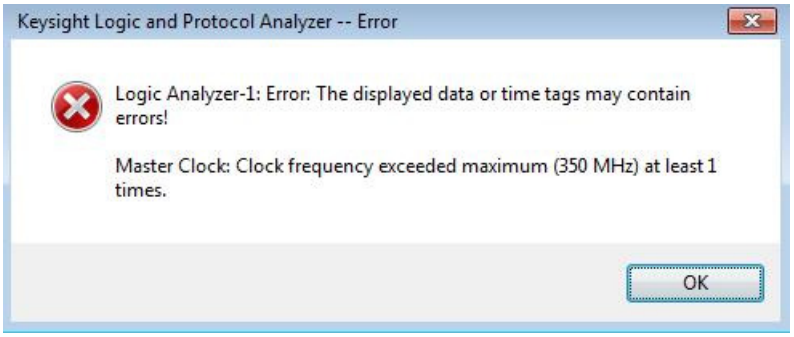
1 Click the **Run Repetitive** icon. Let the logic analyzer run for about 1 minute. The analyzer will acquire data and the Listing Window will continuously update. A marker search window will appear and show progress.



2 If incorrect data is found, the following window appears. The data in the listing window should be A's & 5's.



3 If the clock rate is too high, this error message may occur.



4 If either of these messages occur, the generator frequency should be lowered, Eye Scan should be rerun, and the test should be rerun.

5 Lower the generator frequency by 1 MHz and rerun the test.

6 After the analyzer runs for about 1 minute, click the **Stop** button to stop the acquisition. If the "can't find occurrence" window does not appear, then the analyzer has found good data.

7 For this Pod's Clock, record the generator frequency and the Data Rate in the "Maximum State Data Rate" section of the "Performance Test Record" on page 77. Remember that the data rate is twice the generator frequency.

Pod 3 Clock - Maximum Clock Rate

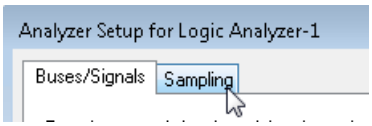
NOTE This section is only applicable to models: 16862A, 16863A & 16864A.

1 Load the **MultipleClocks_NoMarker.ala** configuration file. If asked to save the current configuration file, click **No**.

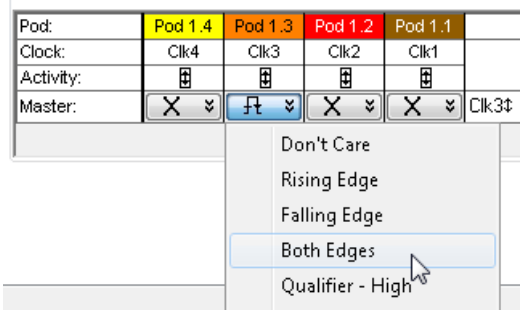
2 Disconnect the U4203A Flying Lead Probe Set from channels 1 & 2 of the 81134A pulse generator output (Bits 2, 6, 10, 14) and clock leads.

3 Connect the probe set from Pod 3 of logic analyzer to the pulse generator channels 1 & 2 output.
- Clock to Channel 1 Output
- Clock (NOT) Channel 1 Output (not)
- Bits 2 & 10 to Channel 2 Output
- Bits 6 & 14 to Channel 2 Output (not)

4 Open the **Sampling** tab in the Analyzer Setup dialog by clicking the **Sampling Setup** Icon.



5 In the clock assignment area, set Pod 1 Clock to **Don't Care** and set Pod 3 Clock to **Both Edges**.



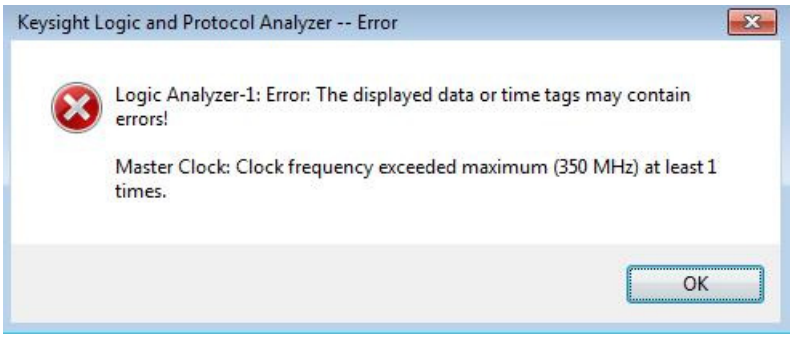
6 Close the dialog by clicking **OK**.

7 Set the generator frequency to 357 MHz as a starting point.

8 Click the **Run Repetitive** toolbar button to start a repetitive run on the logic analyzer for acquiring data repeatedly. Acquired data will start appearing in the Listing window.

9 Start increasing the frequency on the pulse generator by 1 MHz increments while simultaneously observing the logic analyzer data acquisition status.

10 Continue increasing the generator frequency until the logic analyzer displays an error that the data could not be displayed, or the clock is too fast. It is possible that the error is caused by noise introduced as the generator frequency is changed.



11 Without changing the frequency, clear the message by clicking OK. Then click the Run Repetitive toolbar button to start a repetitive run again at the same frequency. Running at the same frequency checks to see if the error message was caused by noise due to the changing of the generator frequency.

12 If the analyzer displays an error again, lower the frequency by 1MHz and run again. If the test does not display an error, increase the frequency by 1 MHz and run again.

13 Continue changing the frequency and running unit the frequency can no longer be increased and the error message not displayed.

14 Set the generator to the highest frequency that did not cause an error.

15 Click **Run Repetitive** .

16 Wait for logic analyzer to complete 100 acquisitions at the new pulse generator frequency without displaying any error. If an error is displayed, decrease the pulse generator frequency by 1 MHz and then again wait for 100 acquisitions at this new frequency without any error. Repeat this step until you get 100 acquisitions without any error display.

17 Click the **Stop** toolbar button to stop the data acquisition.

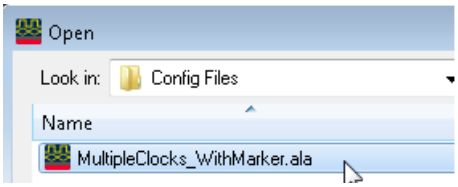
18 Note the generator frequency setting. This will be used in the next section to verify the data rate.

Pod 3 Clock - Setup for Maximum Data Rate

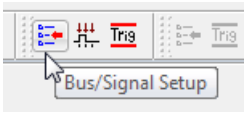
NOTE This section is only applicable to models: 16862A, 16863A & 16864A.

1 Verify that the Generator is set to the frequency found in the last section as a starting point.

2 Load the **MultipleClocks_WithMarker.ala** configuration file. If asked to save the current configuration file, click **No**.

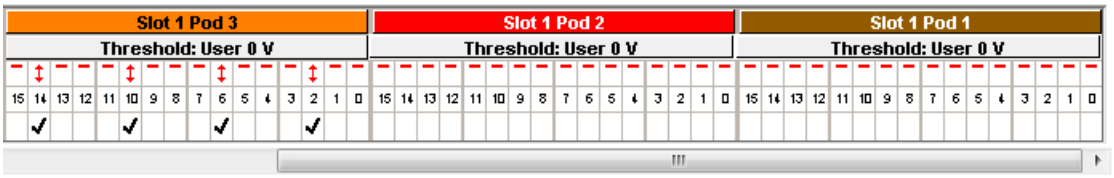


3 Open the **Bus/Signal Setup** dialog by clicking the **Setup** Icon in the tool bar.

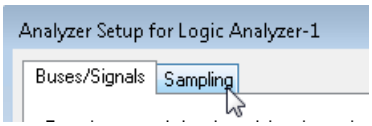


4 Unassign the data bits from Pod1.

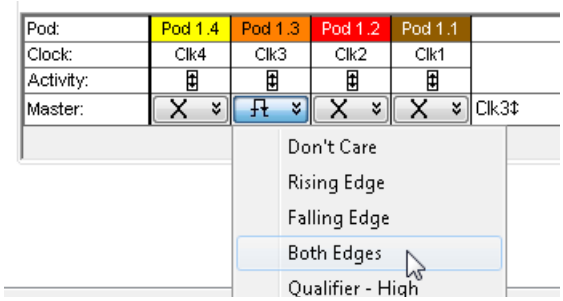
5 Assign bits 2, 6, 10, and 14 of Pod 3.



6 Open the **Sampling** tab.



7 In the clock assignment area, set Pod 1 Clock to **Don't Care** and set Pod 3 Clock to **Both Edges**.



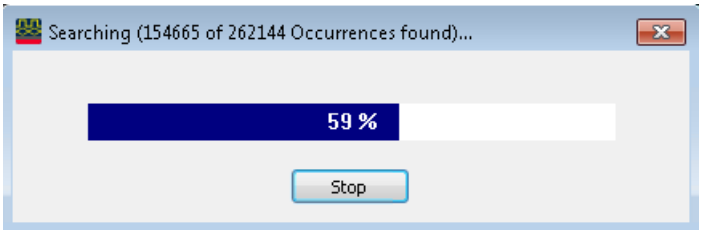
8 Adjust the sample position using the procedure described earlier by clicking the Eye Scan: Sample Position and Thresholds button.

9 Close the dialog windows by clicking **OK**.

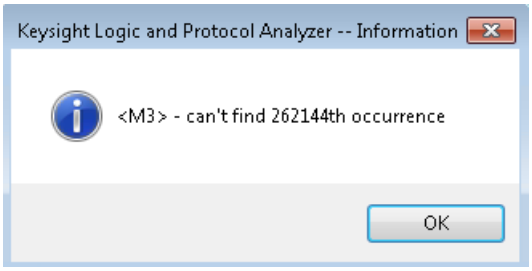
Pod 3 Clock - Measuring Maximum Data Rate

NOTE This section is only applicable to models: 16862A, 16863A & 16864A.

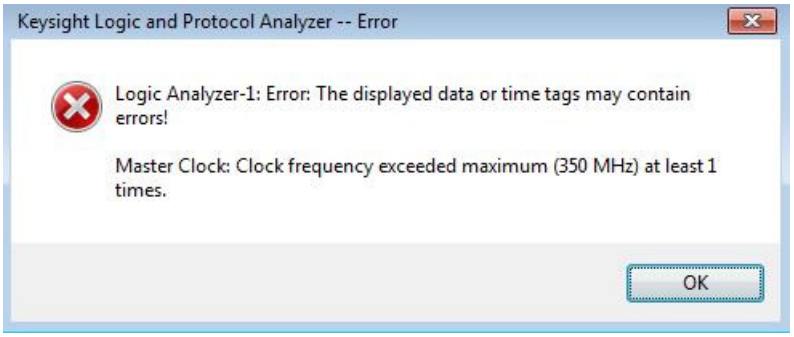
1 Select the **Run Repetitive**  icon. Let the logic analyzer run for about 1 minute. The analyzer will acquire data and the Listing Window will continuously update. A marker search window will appear and show progress.



2 If incorrect data is found, the following window will appear. The data in the listing window should be A's & 5's.



3 If the clock rate is too high, this error message may occur.



4 If either of these messages occur, the generator frequency should be lowered, Eye Scan should be rerun, and the test should be rerun.

5 Lower the generator frequency by 1 MHz and rerun the test.

6 After the analyzer runs for about 1 minute, click the **Stop**  button to stop the acquisition. If the "can't find occurrence" window does not appear, then the analyzer has found good data.

7 For this Pod's Clock, record the generator frequency and the Data Rate in the "Maximum State Data Rate" section of the "Performance Test Record" on page 77. Remember that the data rate is twice the generator frequency.

Pod 4 Clock - Maximum Clock Rate

NOTE This section is only applicable to models: 16862A, 16863A & 16864A.

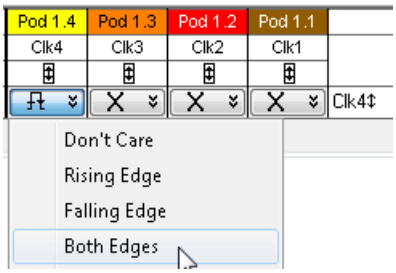
1 Load the **MultipleClocks_NoMarker.ala** configuration file. If asked to save the current configuration file, click **No**.

2 Disconnect the U4203A Flying Lead Probe Set from channels 1 & 2 of the 81134A pulse generator output (Bits 2, 6, 10, 14) and clock leads.

3 Connect the probe set from Pod 4 of logic analyzer to the pulse generator channels 1 & 2 output.
- Clock to Channel 1 Output
- Clock (NOT) Channel 1 Output (not)
- Bits 2 & 10 to Channel 2 Output
- Bits 6 & 14 to Channel 2 Output (not)

4 Open the **Sampling** tab in the Analyzer Setup dialog by clicking the **Sampling Setup** Icon.

5 In the clock assignment area, set Pod 1 Clock to **Don't Care** and set Pod 4 Clock to **Both Edges**.



6 Close the dialog window by clicking **OK**.

7 Set the generator frequency to 357 MHz as a starting point.

8 Click the **Run Repetitive** toolbar button to start a repetitive run on the logic analyzer for acquiring data repeatedly. Acquired data will start appearing in the Listing window.

9 Start increasing the frequency on the pulse generator by 1 MHz increments while simultaneously observing the logic analyzer data acquisition status.

10 Continue increasing the generator frequency until the logic analyzer displays an error that the data could not be displayed, or the clock is too fast. It is possible that the error is caused by noise introduced as the generator frequency is changed.

11 Without changing the frequency, clear the message by clicking OK. Then click the **Run Repetitive** toolbar button to start a repetitive run again at the same frequency. Running at the same frequency checks to see if the error message was caused by noise due to the changing of the generator frequency.

12 If the analyzer displays an error again, lower the frequency by 1MHz and run again. If the test does not display an error, increase the frequency by 1 MHz and run again.

13 Continue changing the frequency and running unit the frequency can no longer be increased and the error message not displayed.

14 Set the generator to the highest frequency that did not cause an error.

15 Click **Run Repetitive** .

16 Wait for logic analyzer to complete 100 acquisitions at the new pulse generator frequency without displaying any error. If an error is displayed, decrease the pulse generator frequency by 1 MHz and then again wait for 100 acquisitions at this new frequency without any error. Repeat this step until you get 100 acquisitions without any error display.

17 Click the **Stop**  toolbar button to stop the data acquisition.

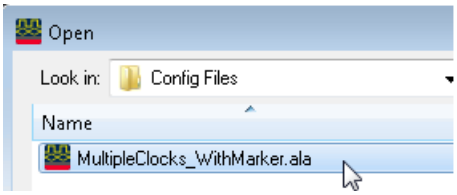
18 Note the generator frequency setting. This will be used in the next section to verify the data rate.

Pod 4 Clock - Setup for Maximum Data Rate

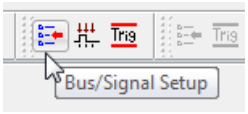
NOTE This section is only applicable to models: 16862A, 16863A & 16864A.

1 Verify that the Generator is set to the frequency found in the last section as a starting point.

2 Load the **MultipleClocks_WithMarker.ala** configuration file. If asked to save the current configuration file, click **No**.

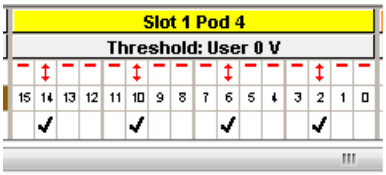


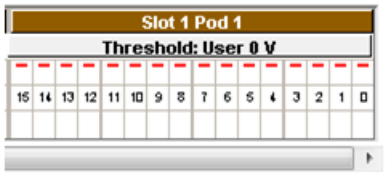
3 Open the **Bus/Signal Setup** dialog by clicking the **Setup** Icon in the tool bar.



4 Unassign the data bits from Pod1.

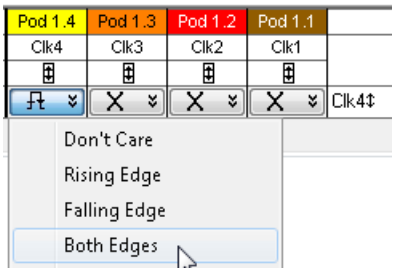
5 Assign bits 2, 6, 10, and 14 of Pod 4.





6 Open the **Sampling** tab.

7 In the clock assignment area, set Pod 1 Clock to **Don't Care** and set Pod 4 Clock to **Both Edges**.



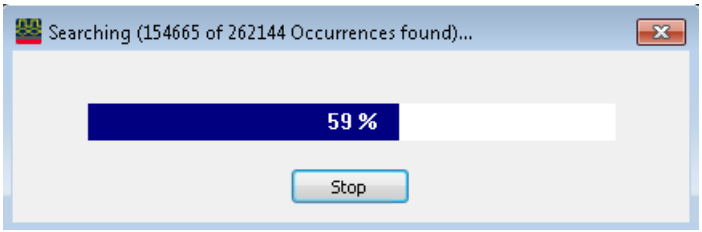
8 Adjust the sample position using the procedure described earlier by selecting "Eye Scan: Sample Position and Thresholds".

9 Close the dialog windows by clicking **OK**.

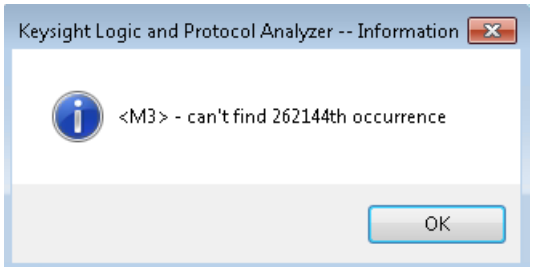
Pod 4 Clock - Measuring Maximum Data Rate

NOTE This section is only applicable to models: 16862A, 16863A & 16864A.

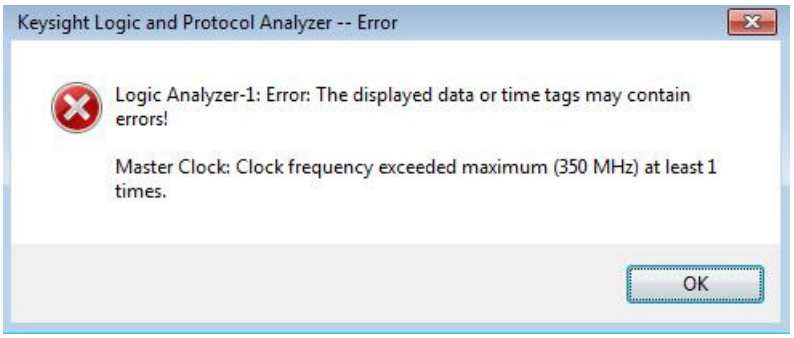
1 Select the **Run Repetitive i**con  . Let the logic analyzer run for about 1 minute. The analyzer will acquire data and the Listing Window will continuously update. A marker search window will appear and show progress.



2 If incorrect data is found, the following window appears. The data in the listing window should be A's & 5's.



3 If the clock rate is too high, the following error message may occur.



4 If either of these messages occur, the generator frequency should be lowered, Eye Scan should be rerun and the test should be rerun.

5 Lower the generator frequency by 1 MHz and rerun the test.

6 After the analyzer runs for about 1 minute, select the **Stop** button to stop the acquisition. If the "can't find occurrence" window does not appear, then the analyzer has found good data.

7 For this Pod's Clock, record the generator frequency and the Data Rate in the "Maximum State Data Rate" section of the "Performance Test Record" on page 77. Remember that the data rate is twice the generator frequency.

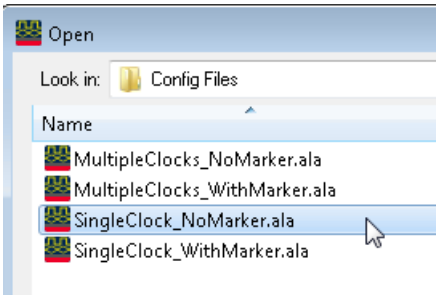
Determine Maximum Data Rate for Single Clock Mode

The single clock test measures the maximum data rate for the single clock mode. This test measures data rates for Rising, Falling, and Both Edge modes. Using Both Edge clocking, it verifies data rates on all pods. The measurement is done in two parts:

- The first part is to determine the maximum clock rate that the analyzer will run at.
- The second part is to verify that the data captured by the analyzer is correct; markers are used to verify the data patterns.

Single Clock Rising Edge - Maximum Clock Rate

1 Load the **SingleClock_NoMarker.ala** configuration file. If asked to save the current configuration file, click **No**.

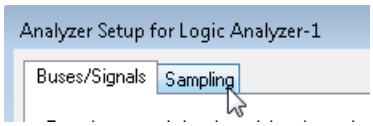


2 Verify that the Generator is set to 714 MHz as a starting point.

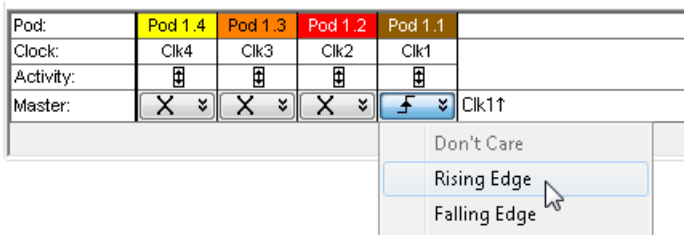
3 Disconnect the U4203A Flying Lead Probe Set from channels 1 & 2 of the 81134A pulse generator output (Bits 2, 6, 10, 14) and clock leads.

4 Connect the probe set from Pod 1 of logic analyzer to the pulse generator channels 1 & 2 output.
- Clock to Channel 1 Output
- Clock (NOT) Channel 1 Output (not)
- Bits 2 & 10 to Channel 2 Output
- Bits 6 & 14 to Channel 2 Output (not)

5 Open the Sampling tab in the Analyzer Setup dialog by clicking the **Sampling Setup** Icon.



6 In the clock assignment area, set Pod 1 Clock to **Rising Edge**.

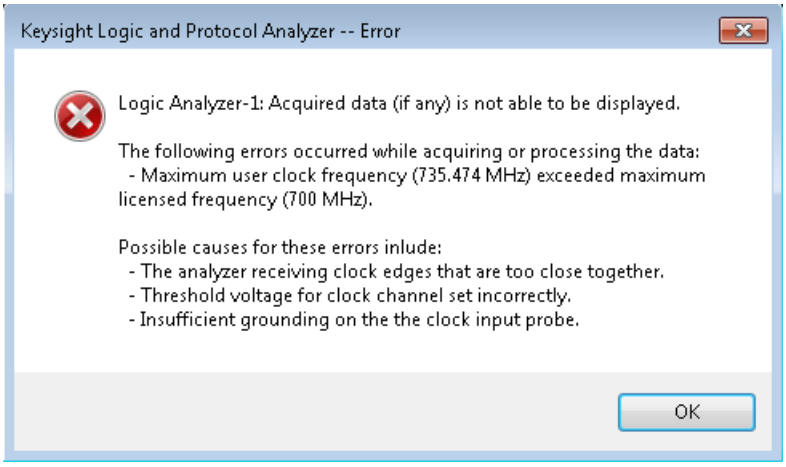


7 Close the dialog windows by clicking **OK**.

8 Click the **Run Repetitive** toolbar button to start a repetitive run on the logic analyzer for acquiring data repeatedly. Acquired data will start appearing in the Listing window.

9 Start increasing the frequency on the pulse generator by 1 MHz increments while simultaneously observing the logic analyzer data acquisition status.

10 Continue increasing the generator frequency until the logic analyzer displays an error that the data could not be displayed, or the clock is too fast. It is possible that the error is caused by noise introduced as the generator frequency is changed.



11 Without changing the frequency, clear the message by clicking OK. Then click the **Run Repetitive** toolbar button to start a repetitive run again at the same frequency. Running at the same frequency checks to see if the error message was caused by noise due to the changing of the generator frequency.

12 If the analyzer displays an error again, lower the frequency by 1MHz and run again. If the test does not display an error, increase the frequency by 1 MHz and run again.

13 Continue changing the frequency and running unit the frequency can no longer be increased and the error message not displayed.

14 Set the generator to the highest frequency that did not cause an error.

15 Click **Run Repetitive** .

16 Wait for logic analyzer to complete 100 acquisitions at the new pulse generator frequency without displaying any error. If an error is displayed, decrease the pulse generator frequency by 1 MHz and then again wait for 100 acquisitions at this new frequency without any error. Repeat this step until you get 100 acquisitions without any error display.

17 Click the **Stop** toolbar button to stop the data acquisition.

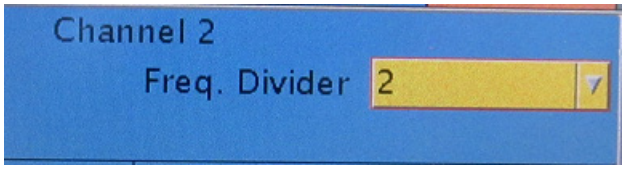
18 Note the generator frequency setting this will be used in the next section to verify the data rate.

Single Clock Rising Edge - Pod 1 Data - Setup for Maximum Data Rate

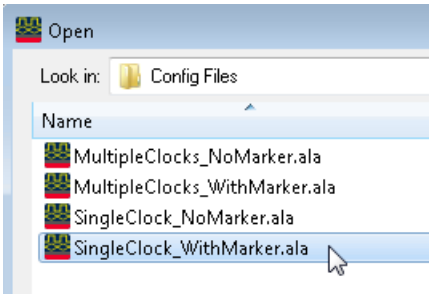
To measure the maximum data rate, the starting frequency will be the frequency found in the section above. A new configuration file will be used that has a marker setup to verify that the data patterns are correct. To ensure that the data is sampled correctly, the sample position needs to be set. Eye Scan is used to set the sample points of all the data to the same eye.

1 On the 81134A, select the channel 2 setup screen. This is the data channel.

2 Set the Channel 2 Freq. Divider to 2.

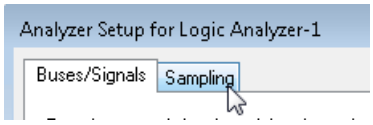


3 Load the **SingleClock_WithMarker.ala** configuration file. If asked to save the current configuration file, click **No**.

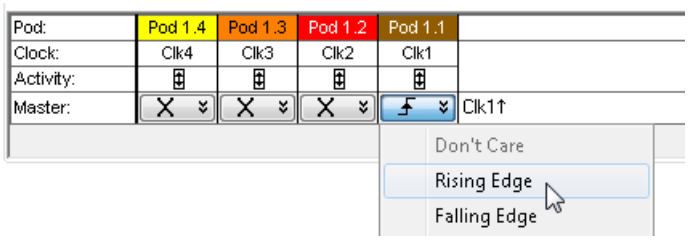


4 Verify that the Generator is set to the frequency found in the last section as a starting point.

5 Open the Sampling tab in the Analyzer Setup dialog by clicking the **Sampling Setup** Icon.



6 In the clock assignment area, set Pod 1 Clock to **Rising Edge**.

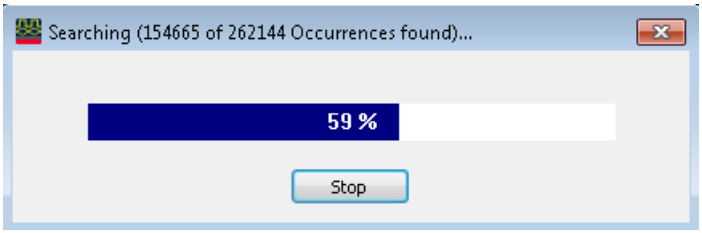


7 Adjust the sample position using the procedure described earlier by clicking the **Eye Scan: Sample Position and Thresholds** button.

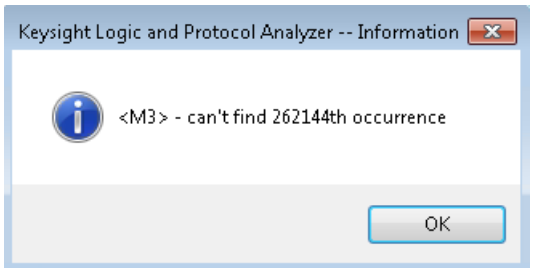
8 Close the dialog windows by clicking **OK**.

Single Clock Rising Edge - Pod 1 Data - Measuring Maximum Data Rate

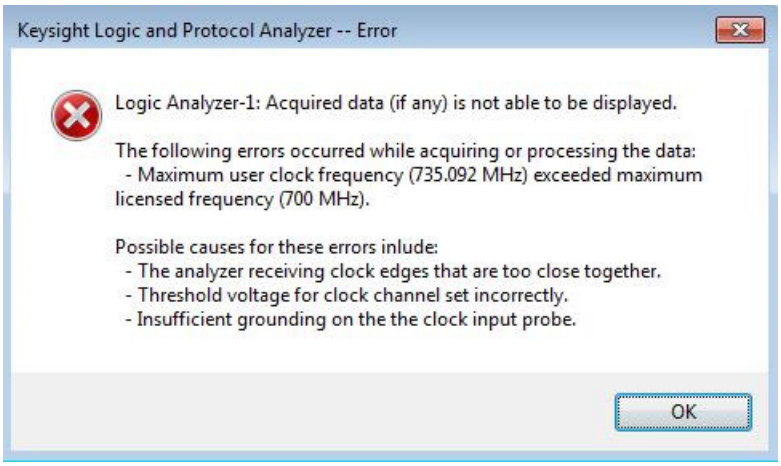
1 Select the **Run Repetitive** icon. Let the logic analyzer run for about 1 minute. The analyzer will acquire data and the Listing Window will continuously update. A marker search window will appear and show progress.



2 If incorrect data is found, the following window will appear. The data in the listing window should be A's & 5's.



3 If the clock rate is too high, this error message may occur.



4 If either of these messages occur, the generator frequency should be lowered, Eye Scan rerun and the test rerun.

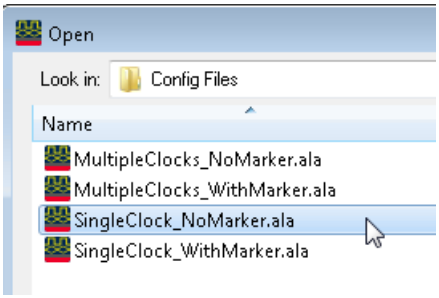
5 Lower the generator frequency by 1 MHz and rerun the test.

6 After the analyzer runs for about 1 minute select the **Stop** button to stop the acquisition. If the "can't find occurrence" window does not appear, then the analyzer has found good data.

7 For Single Clock for Rising Edge record the generator frequency and the Data Rate in the "Maximum State Data Rate" section of the "Performance Test Record. Note: For Single Edge Clocking, the data rate is the same as the generator frequency.

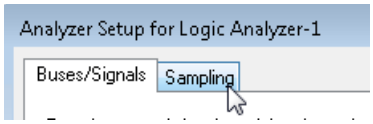
Single Clock Falling Edge - Maximum Clock Rate

1 Load the **SingleClock_NoMarker.ala** configuration file.If asked to save the current configuration file, click **No**.

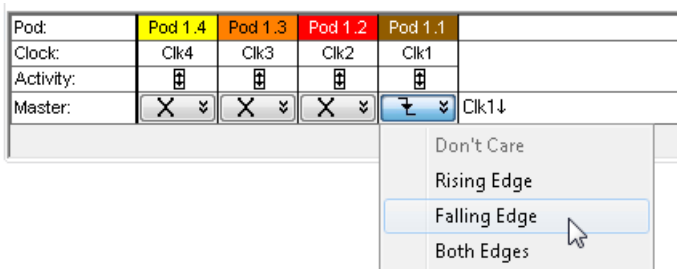


2 Verify that the Generator is set to 714 MHz as a starting point.

3 Open the Sampling tab in the Analyzer Setup dialog by clicking the **Sampling Setup** Icon.



4 In the clock assignment area, set Pod 1 Clock to **Falling Edge**.

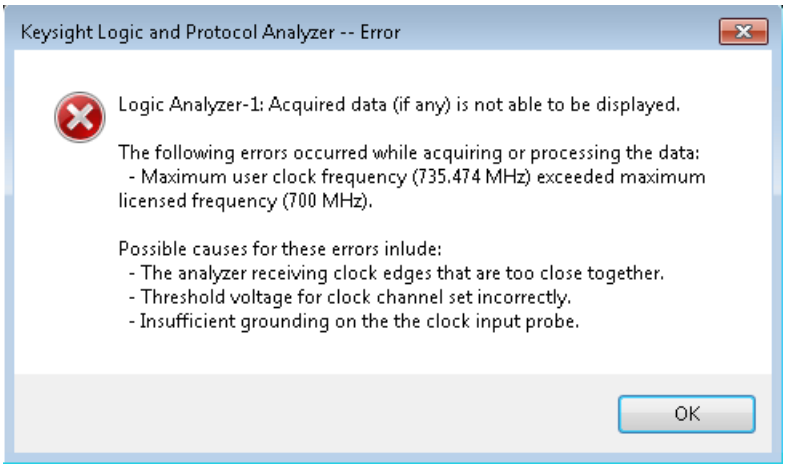


5 Close the dialog windows by clicking OK.

6 Click the **Run Repetitive** toolbar button to start a repetitive run on the logic analyzer for acquiring data repeatedly. Acquired data will start appearing in the Listing window.

7 Start increasing the frequency on the pulse generator by 1 MHz increments while simultaneously observing the logic analyzer data acquisition status.

8 Continue increasing the generator frequency until the logic analyzer displays an error that the data could not be displayed, or the clock is too fast. It is possible that the error is caused by noise introduced as the generator frequency is changed.



9 Without changing the frequency, clear the message by clicking OK. Then click the **Run Repetitive** toolbar button to start a repetitive run again at the same frequency. Running at the same frequency checks to see if the error message was caused by noise due to the changing of the generator frequency.

10 If the analyzer displays an error again, lower the frequency by 1MHz and run again. If the test does not display an error, increase the frequency by 1 MHz and run again.

11 Continue changing the frequency and running unit the frequency can no longer be increased and the error message not displayed.

12 Set the generator to the highest frequency that did not cause an error.

13 Click **Run Repetitive** .

14 Wait for logic analyzer to complete 100 acquisitions at the new pulse generator frequency without displaying any error. If an error is displayed, decrease the pulse generator frequency by 1 MHz and then again wait for 100 acquisitions at this new frequency without any error. Repeat this step until you get 100 acquisitions without any error display.

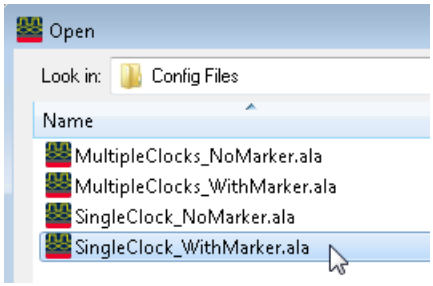
15 Click the **Stop** toolbar button to stop the data acquisition.

16 Note the generator frequency setting. This will be used in the next section to verify the data rate.

Single Clock Falling Edge - Pod 1 Data - Setup for Maximum Data Rate

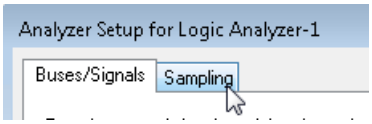
1 On the 81134A, verify that Channel 2 Freq Divide is set to 2.

2 Load the **SingleClock_WithMarker.ala** configuration file. If asked to save the current configuration file, click **No**.

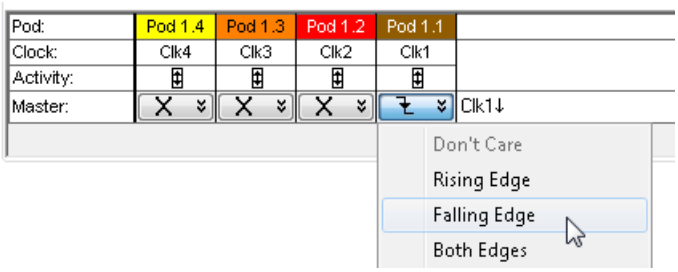


3 Verify that the Generator is set to the frequency found in the last section as a starting point.

4 Open the Sampling tab in the Analyzer Setup dialog by clicking the **Sampling Setup** Icon.



5 In the clock assignment area, set Pod 1 Clock to **Falling Edge**.

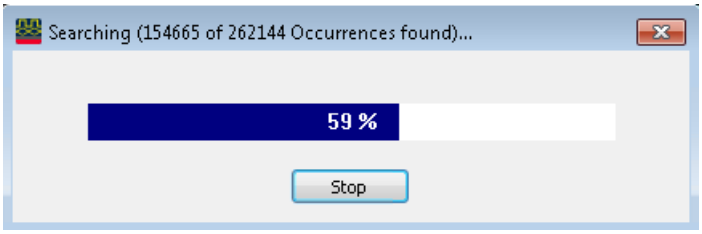


6 Adjust the sample position using the procedure described earlier by clicking the **Eye Scan: Sample Position and Thresholds** button.

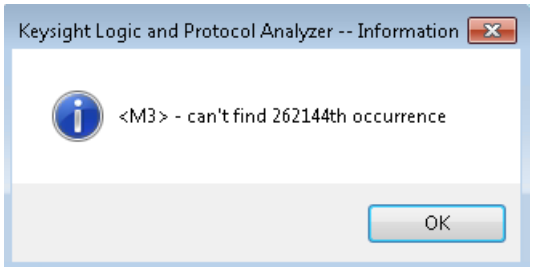
7 Close the dialog windows by clicking **OK**.

Single Clock Falling Edge - Pod 1 Data - Measuring Maximum Data Rate

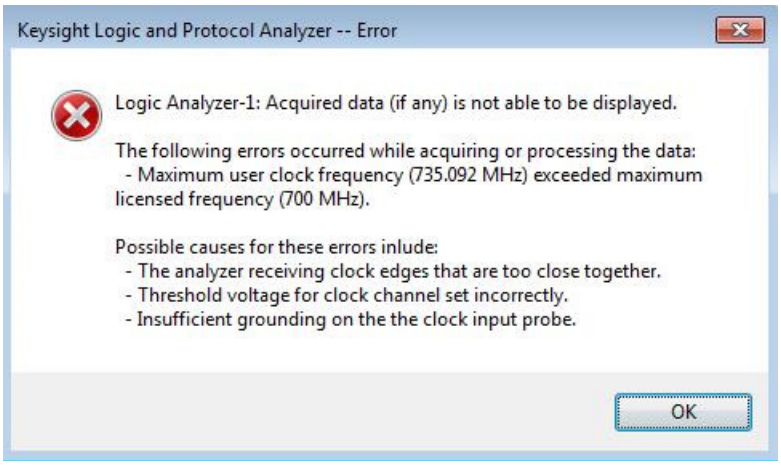
1 Select the **Run Repetitive** icon. Let the logic analyzer run for about 1 minute. The analyzer will acquire data and the Listing Window will continuously update. A marker search window will appear and show progress.



2 If incorrect data is found, the following window will appear. The data in the listing window should be A's & 5's.



3 If the clock rate is too high, this error message may occur.



4 If either of these messages occur, the generator frequency should be lowered, Eye Scan rerun and the test rerun.

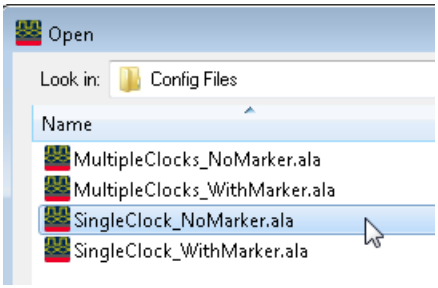
5 Lower the generator frequency by 1 MHz and rerun the test.

6 After the analyzer runs for about 1 minute select the **Stop** button to stop the acquisition. If the "can't find occurrence" window does not appear, then the analyzer has found good data.

7 For Single Clock for Falling Edge, record the generator frequency and the Data Rate in the "Maximum State Data Rate" section of the "Performance Test Record. Note: For Single Edge Clocking, the data rate is the same as the generator frequency.

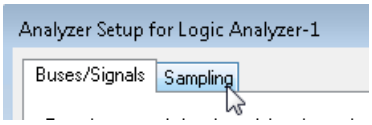
Single Clock Both Edges - Maximum Clock Rate

1 Load the **SingleClock_NoMarker.ala** configuration file. If asked to save the current configuration file, click **No**.

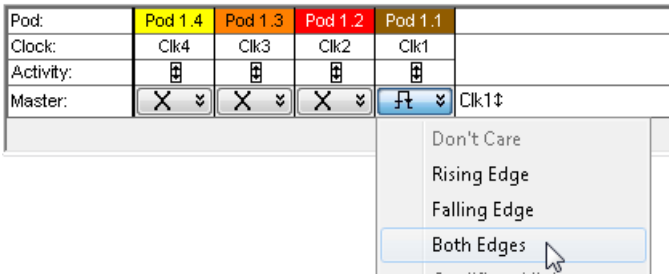


2 Verify that the Generator is set to 714 MHz as a starting point.

3 Open the Sampling tab in the Analyzer Setup dialog by clicking the **Sampling Setup** Icon.



4 In the clock assignment area, set Pod 1 Clock to **Both Edges**.

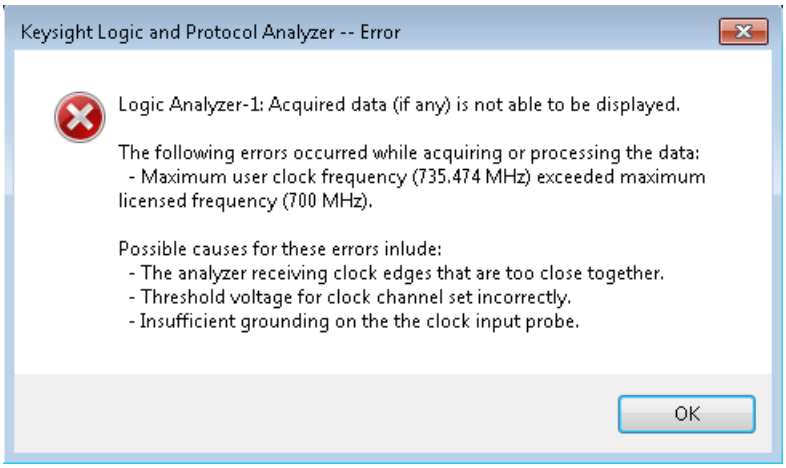


5 Close the dialog windows by clicking OK.

6 Click the **Run Repetitive** toolbar button to start a repetitive run on the logic analyzer for acquiring data repeatedly.Acquired data will start appearing in the Listing window.

7 Start increasing the frequency on the pulse generator by 1 MHz increments while simultaneously observing the logic analyzer data acquisition status.

8 Continue increasing the generator frequency until the logic analyzer displays an error that the data could not be displayed, or the clock is too fast. It is possible that the error is caused by noise introduced as the generator frequency is changed.



9 Without changing the frequency, clear the message by clicking OK. Then click the **Run Repetitive** toolbar button to start a repetitive run again at the same frequency. Running at the same frequency checks to see if the error message was caused by noise due to the changing of the generator frequency.

10 If the analyzer displays an error again, lower the frequency by 1MHz and run again. If the test does not display an error, increase the frequency by 1 MHz and run again.

11 Continue changing the frequency and running unit the frequency can no longer be increased and the error message not displayed.

12 Set the generator to the highest frequency that did not cause an error.

13 Click **Run Repetitive**.

14 Wait for logic analyzer to complete 100 acquisitions at the new pulse generator frequency without displaying any error. If an error is displayed, decrease the pulse generator frequency by 1 MHz and then again wait for 100 acquisitions at this new frequency without any error. Repeat this step until you get 100 acquisitions without any error display.

15 Click the **Stop** toolbar button to stop the data acquisition.

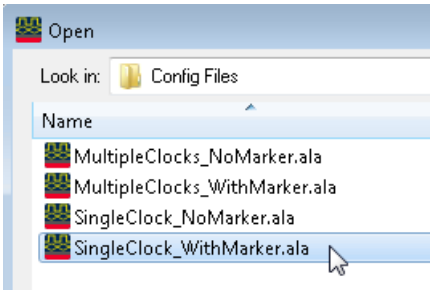
16 Note the generator frequency setting. This will be used in the next section to verify the data rate.

Single Clock Both Edges - Pod 1 Data - Setup for Maximum Data Rate

1 On the 81134A, select the channel 2 setup screen. This is the data channel.

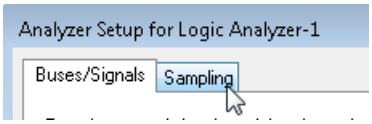
2 Set the Channel 2 Freq. Divider to 1.

3 Load the **SingleClock_WithMarker.ala** configuration file. If asked to save the current configuration file, click **No**.



4 Verify that the Generator is set to the frequency found in the last section as a starting point.

5 Open the Sampling tab in the Analyzer Setup dialog by clicking the **Sampling Setup** Icon.

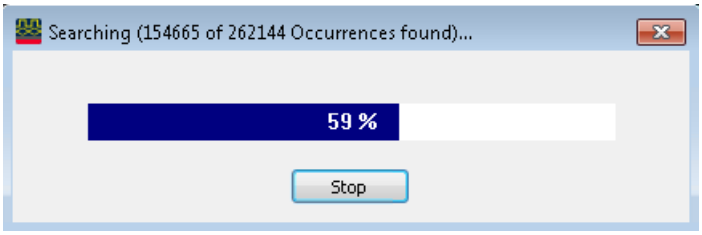


6 Adjust the sample position using the procedure described earlier by clicking the **Eye Scan: Sample Position and Thresholds** button. Select the eye closest to -1 ns.

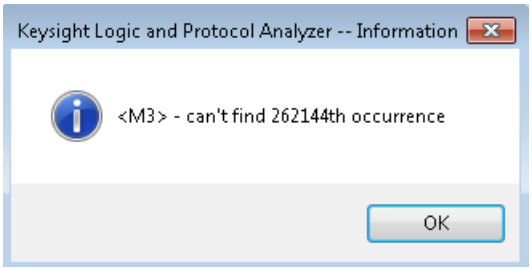
7 Close the dialog windows by clicking OK.

Single Clock Both Edges - Pod 1 Data - Measuring Maximum Data Rate

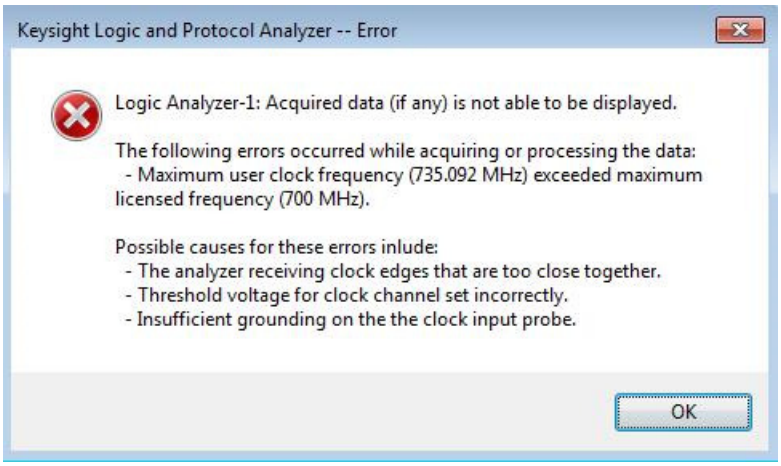
1 Select the **Run Repetitive** icon . Let the logic analyzer run for about 1 minute. The analyzer will acquire data and the Listing Window will continuously update. A marker search window will appear and show progress.



2 If incorrect data is found, the following window will appear. The data in the listing window should be A's & 5's.



3 If the clock rate is too high, this error message may occur.



4 If either of these messages occur, the generator frequency should be lowered, Eye Scan should be rerun and the test should be rerun.

5 Lower the generator frequency by 1 MHz and rerun the test.

6 After the analyzer runs for about 1 minute, select the **Stop** button to stop the acquisition. If the "can't find occurrence" window does not appear, then the analyzer has found good data.

7 For Single Clock for Both Edges Pod1, record the generator frequency and the Data Rate in the "Maximum State Data Rate" section of the "Performance Test Record. Note: For Both Edges Clocking, the data rate is twice the generator frequency.

Single Clock Both Edges - Pod 2 Data - Setup for Maximum Data Rate

The next set of tests use the Pod 1 clocks to verify the data rate on the other pods in Single Clock mode.

NOTE The starting frequency for the following tests (Pods 2-8) will be the frequency found in the ""Single Clock Both Edges - Maximum Clock Rate" section above.

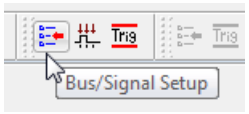
1 Verify that the Generator is set to the frequency found in "Single Clock Both Edges - Maximum Clock Rate section above.

2 Disconnect the U4203A Flying Lead Probe Set from channels 2 of the 81134A pulse generator output (Bits 2, 6, 10, 14). Do not disconnect the clock leads from Pod 1.

3 Connect the probe set from Pod 2 of logic analyzer to the pulse generator channels 2 outputs.

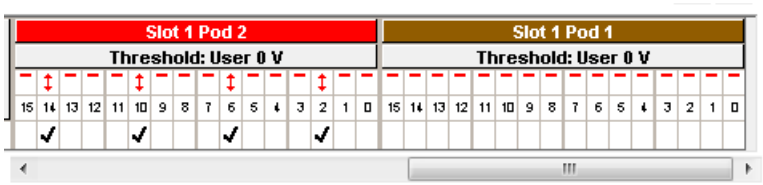
- Bits 2 & 10 to Channel 2 Output
- Bits 6 & 14 to Channel 2 Output (not)

4 Open the **Bus/Signal Setup** dialog by clicking the **Setup** Icon in the toolbar.

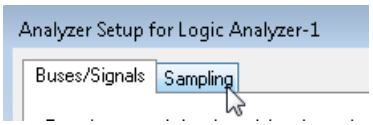


5 Unassign the data bits from Pod1.

6 Assign bits 2, 6, 10, and 14 of Pod 2.



7 Open the **Sampling** tab.

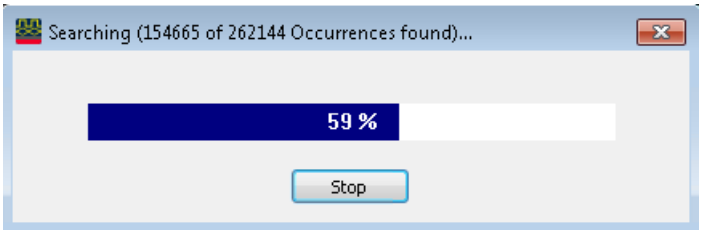


8 Adjust the sample position using the procedure described earlier by clicking the **Eye Scan: Sample Position and Thresholds** button. Select the eye closest to -1 ns.

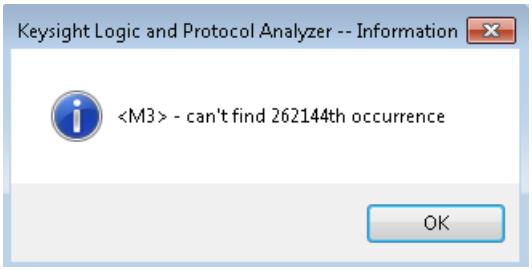
9 Close the dialog windows by clicking **OK**.

Single Clock Both Edges - Pod 2 Data - Measuring Maximum Data Rate

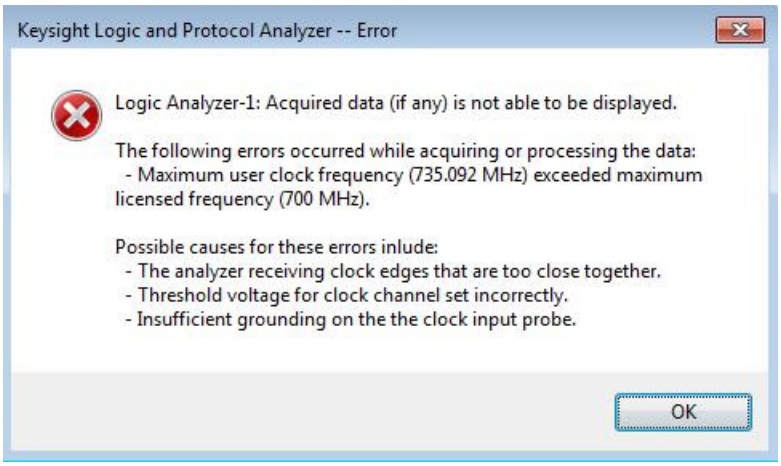
1 Select the **Run Repetitive** icon  . Let the logic analyzer run for about 1 minute. The analyzer will acquire data and the Listing Window will continuously update. A marker search window will appear and show progress.



2 If incorrect data is found, the following window appears. The data in the listing window should be A's & 5's.



3 If the clock rate is too high, the following error message may occur.



4 If either of these messages occur, the generator frequency should be lowered, Eye Scan should be rerun, and the test should be rerun.

5 Lower the generator frequency by 1 MHz and rerun the test.

6 After the analyzer runs for about 1 minute, select the **Stop** button to stop the acquisition. If the "can't find occurrence" window does not appear, then the analyzer has found good data.

7 For Single Clock for Both Edges Pod 2, record the generator frequency and the Data Rate" in the "Maximum State Data Rate" section of the "Performance Test Record. Note: For Both Edges Clocking, the data rate is twice the generator frequency.

Single Clock Both Edges - Pods 3 to 8

For the product models that have more Pods, the data can be verified using the same procedure that was used above for "Single Clock Both Edges - Pod 2 Data". The Pod 1 clock will be used for all other pods. The U4203A cable will need to be moved from Pod 3 & 4 to the other pods as needed.When this is done, the Thresholds will need to be set to 0V. Follow both the Setup and Measurement sections for each pod, connecting to the generator and verifying the data patterns. Record each measured frequency in the "Performance Test Record table for each Pod.

Conclude the State Data Rate Tests

Perform the following steps to properly shut down the logic analyzer session after completing the state mode tests.

End the test.

1 From the Main menu, select **File > Exit**. In the dialog "Do you want to save the current configuration?", click **No**.

2 Disconnect all cables and adapters from the pulse generator.

3 Power down the Analyzer frame.

Performance Test Record

LOGIC ANALYZER MODEL NO.: 16861A, 16862A, 16863A, 16864A	
Logic Analyzer Serial No.	Work Order No.
Date:	Recommended Test Interval - 2 Year/4000 hours
	Recommended next testing:

TEST EQUIPMENT USED
Pulse Generator Model No.
Pulse Generator Serial No.
Pulse Generator Calibration Due Date:

MEASUREMENT UNCERTAINTY
Clock Rate
Pulse Generator Frequency Accuracy: 81134A: ±0.005% of setting. Approx. Cabling Accuracy ±0.005% of setting. 2.01% = ±0.010% Uncertainty + 2% Test Margin.
Setting Base option: (should be tested to the Option 700 level at the service center) Option 700: ▪ 700 MHz + 2% = 714 MHz (Single Clock mode) ▪ 350 MHz + 2% = 357 MHz (Multiple Clocks mode)

TEST RESULTS
Logic Analysis System Self-Tests (Pass/Fail):

TEST RESULTS - Maximum State Data Rate			
Mode: Multiple Clocks (Both Edges)			
	Data Rate (Spec) (Mb/s)	Generator Frequency (MHz)	Measured Data Rate (Mb/s)
Pod 1 Clock	700		
Pod 2 Clock	700		
Pod 3 Clock	700		
Pod 4 Clock	700		

TEST RESULTS - Maximum State Data Rate			
Mode: Single Clock			
	Data Rate (Spec) (Mb/s)	Generator Frequency (MHz)	Measured Data Rate (Mb/s)
Clock - Rising Edge (Data Pod 1)	700		
Clock - Falling Edge (Data Pod 1)	700		
Clock - Both Edges (Data Pod 1)	1400		
Clock - Both Edges (Data Pod 2)	1400		
Clock - Both Edges (Data Pod 3)	1400		
Clock - Both Edges (Data Pod 4)	1400		
Clock - Both Edges (Data Pod 5)	1400		
Clock - Both Edges (Data Pod 6)	1400		
Clock - Both Edges (Data Pod 7)	1400		
Clock - Both Edges (Data Pod 8)	1400		

4 Calibrating

This chapter provides instructions for calibrating the16860 series logic analyzer.

Calibration Strategy

The 16860 series logic analyzer does not require any periodic adjustments or calibration by the user to ensure operational accuracy.

However, Keysight recommends that performance of the 16860 series logic analyzer be tested against its specifications at two-year intervals. This testing is required in order to obtain calibration certification.

You can refer to Chapter 3, “Testing 16860 Series Logic Analyzers Performance" to find detailed information on how to test the performance of the 16860 series logic analyzer.

5 Troubleshooting

This chapter provides instructions for troubleshooting a 16860 logic analyzer that is not operating correctly.

The troubleshooting consists of flowcharts, self-test instructions, a cable test, and how to restore system software.

If you suspect a problem, start at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform the self-tests or the cable test.

The service strategy for the 16860 logic analyzer is the replacement of defective assemblies. You can send this logic analyzer to Keysight Technologies for all service work, including troubleshooting. Contact your nearest Keysight Technologies Sales Office for more details.

Keysight requires that the 16860 logic analyzer unit be repaired only at qualified repair facilities such as the Keysight Repair Centers.

CAUTION **Electrostatic discharge can damage electronic components. Use grounded wrist straps and mats when you perform any troubleshooting procedures to this instrument.**

To use the system troubleshooting flowcharts

Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled references on the charts indicate connections with the other flowcharts or other parts within the same flowchart. Start your troubleshooting at the top of the first flowchart (Figure 1 on page 83).

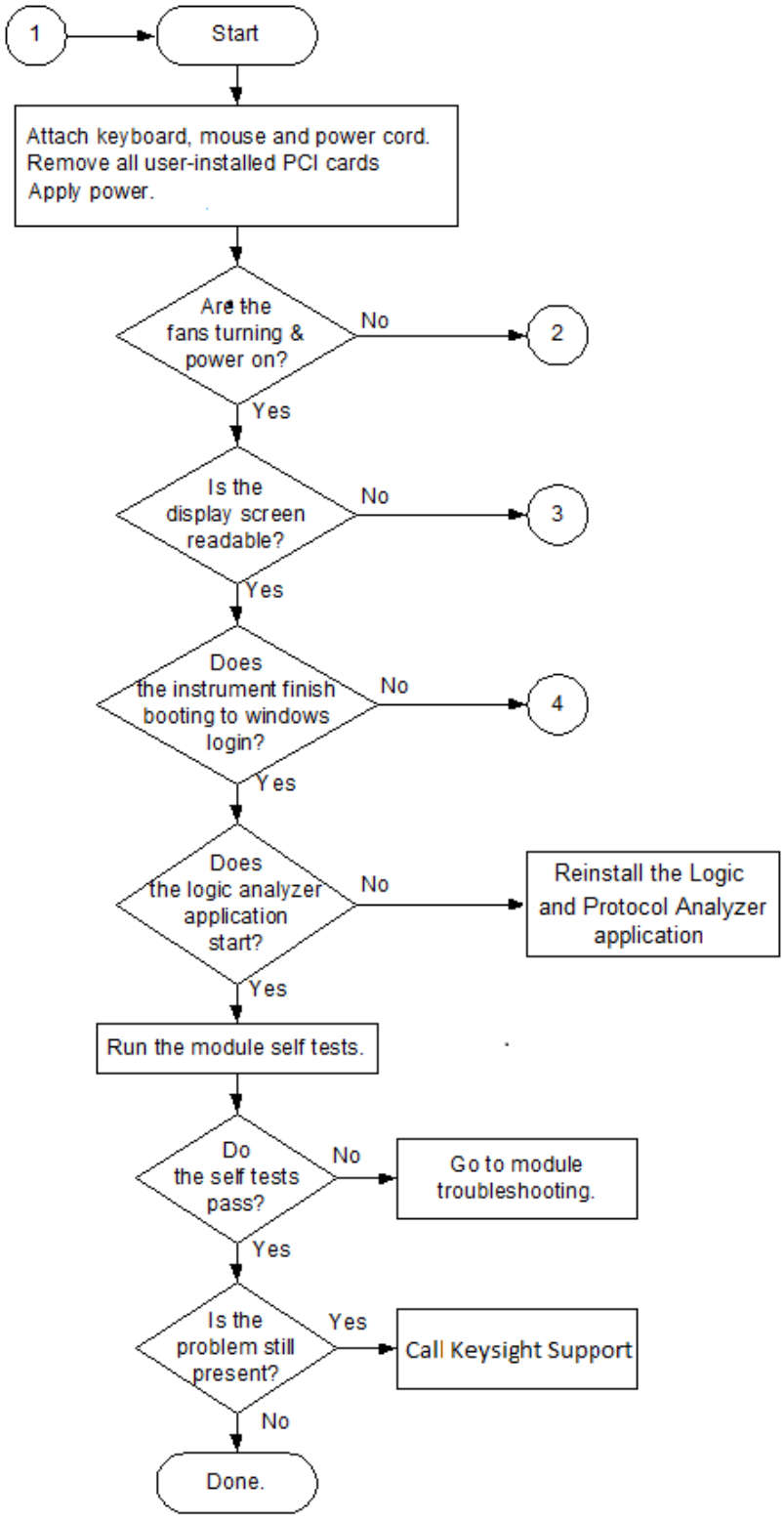


Figure 1 System Troubleshooting Flowchart

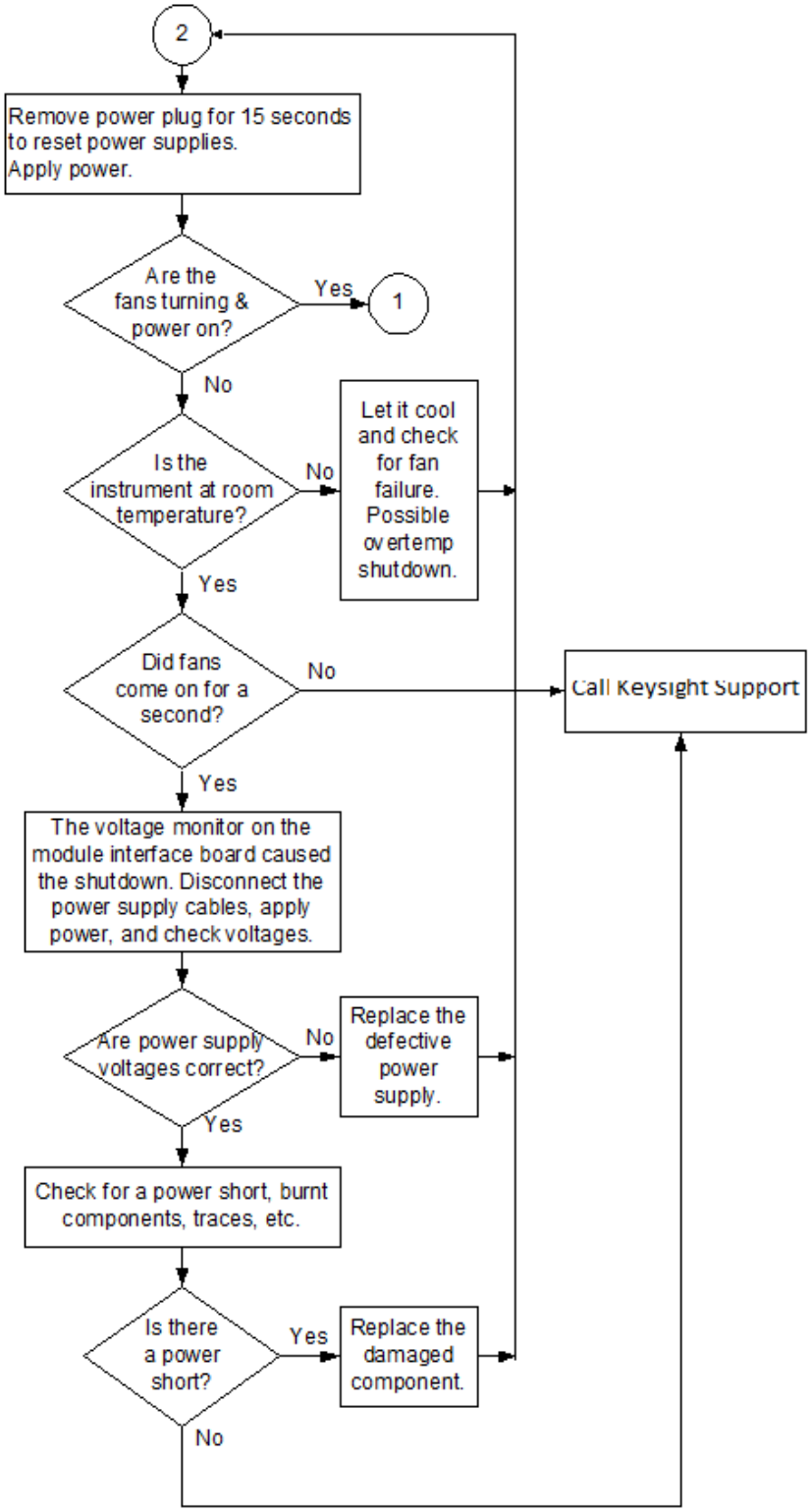


Figure 2 System Power Troubleshooting Flowchart

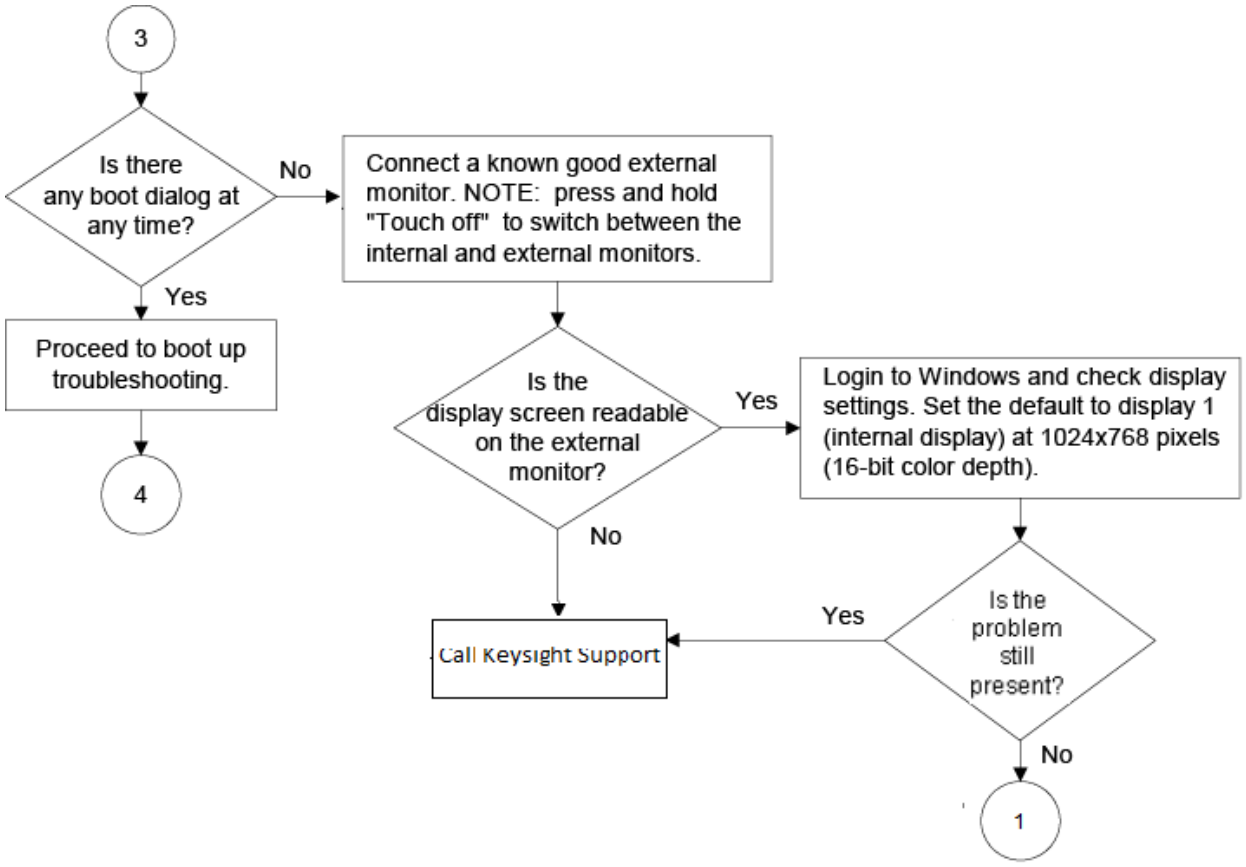


Figure 3 System Display Troubleshooting Flowchart

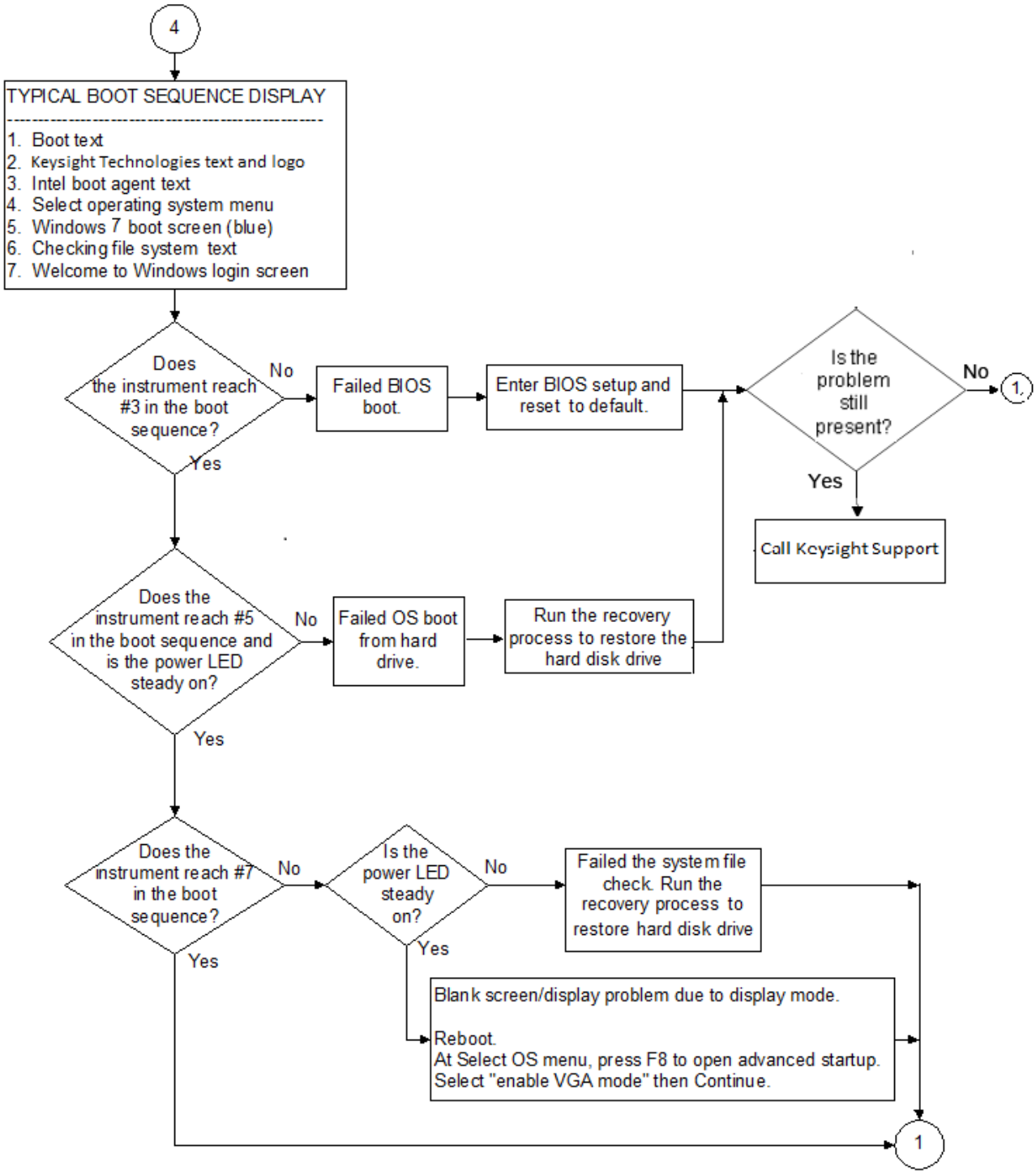


Figure 4 System Boot Up Troubleshooting Flowchart

To use the logic acquisition troubleshooting flowcharts

Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled numbers on the charts indicate connections with the other flowchart. Start your troubleshooting at the top of the first flowchart.

If the instrument still doesn't work correctly after completing all the procedures described in the flowchart, return it to Keysight Technologies for repair. Be sure to include a note describing the problem in detail.

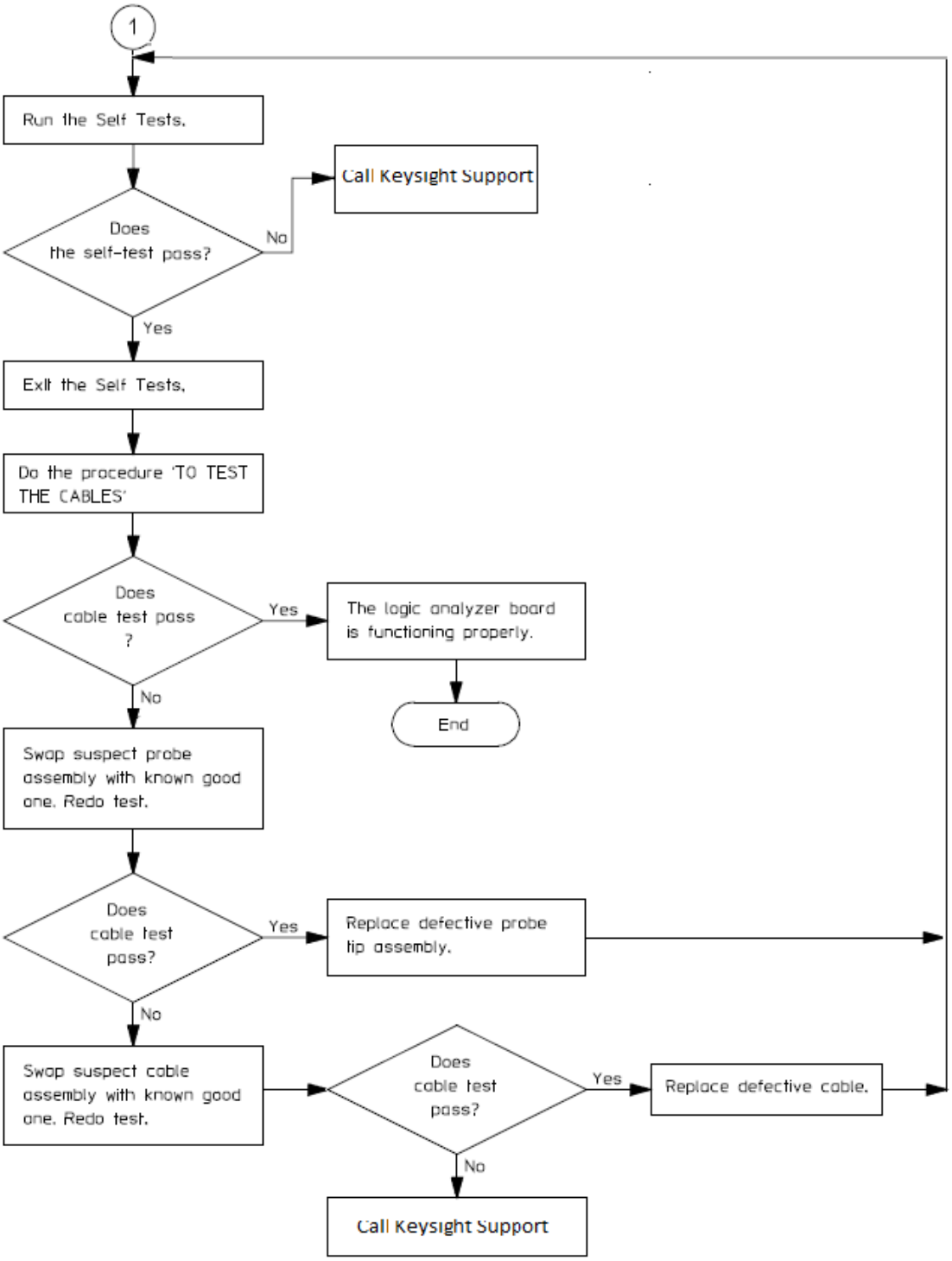


Figure 5 Logic Acquisition Troubleshooting Flowchart

To troubleshoot system power problems

If the system warns you it is powering down before it powers down, it is a fan/overtemp problem. If it just powers down, it is a power supply problem.

If the lights do not come on and if the system powers up momentarily when you plug it in, make sure the power button hasn't become jammed or stuck in the pushed-in position.

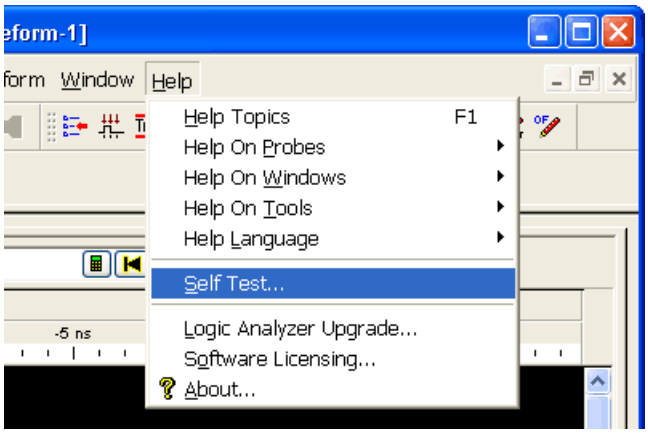
Power Supplies

All 16860 Series logic analyzers have the same 600 W power supply and a second 15 W power supply. The power supplies must remain connected in order to test their output voltages. There are power supply test points on the Frame Interface Board (FIB).

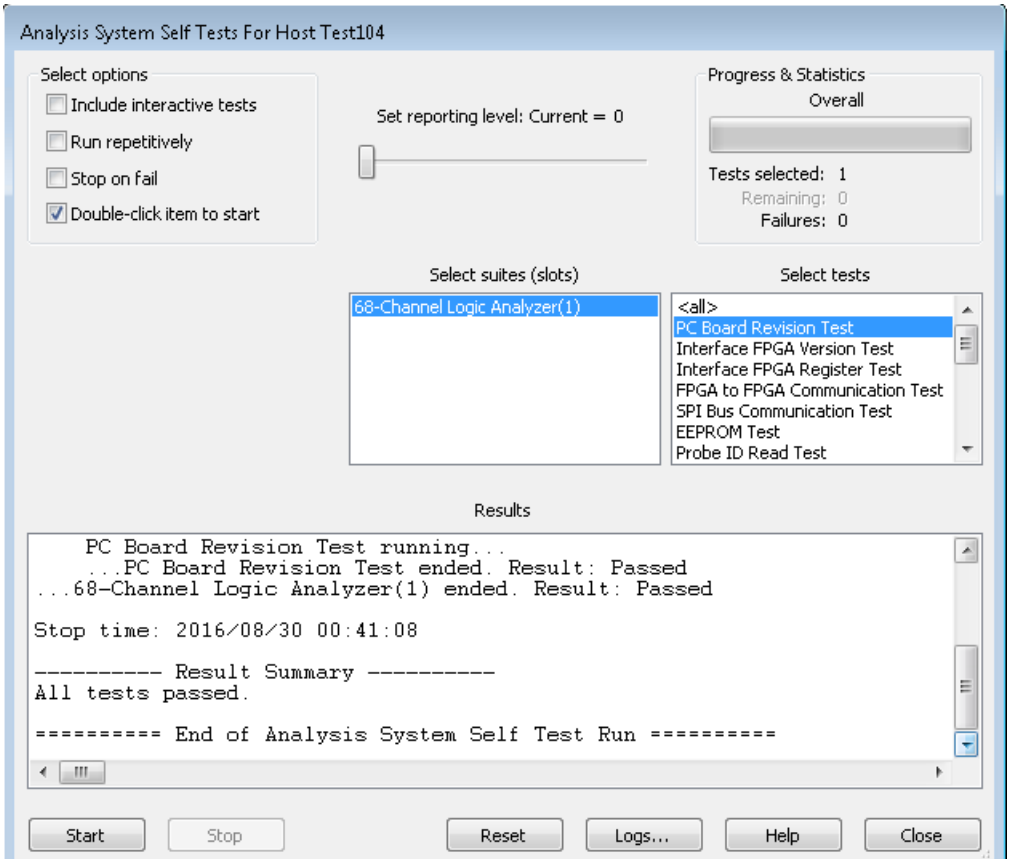
To run the self-tests

The self-tests check the functional operation of the logic analyzer. Perform the self-tests as an acceptance test when receiving the logic analyzer or when the logic analyzer is repaired.

1 In the *Keysight Logic and Protocol Analyzer* application, click **Help**>**Self Test..**.



2 In the **Analysis System Self Test** dialog, double-click the test you want to run.



Logic Acquisition Self-Test Descriptions

The self-tests for the logic analyzer identify the correct operation of major functional areas in the module.

Interface FPGA Version Test

This test verifies that the FPGA program is a version that the software can use. This is necessary because new features will be added to the 16860 logic analyzer that will require both new software and new FPGA bits.

Interface FPGA Register Test

The purpose of this test is to verify that the backplane interface can communicate with the backplane FPGA. The FPGA must be working before any of the other circuits on the board will work. Also, the FPGA generates the board ID code that is returned to identify the module and slot.

FPGA to FPGA Communication Test

This test is only run if there are two or more logic analyzer installed and connected together with the flex cables. The purpose of this test is to verify that the FPGAs can drive and receive the signals correctly.

SPI Bus Communication Test

The purpose of this test is to verify communications over the SPI bus from the Interface FPGA to various devices attached to the SPI bus.

EEPROM Test

The purpose of this test is to verify:

- The address and data paths to the EEPROM.
- That each cell in the EEPROM can be programmed high and low.
- That individual locations can be independently addressed.
- The EEPROM can be block erased.

Probe ID Read Test

The purpose of this test is to verify that the Probe ID values can be correctly read and to verify the functionality of the Digital to Analog Converter by testing the two Probe ID DAC outputs at various voltage levels.

Chip Registers Read/Write Test

The purpose of this test is to verify that each bit in each register of the Analysis chip can be written with a 1 and 0 and read back again. The test also verifies that a chip reset sets all registers to their reset condition (all 0s for most registers).

Freq Synth Lock Detect Test

This test determines if all the voltage-controlled oscillators (VCOs) are working properly.

Acquisition Chip BIST Test

Tests the Timing Zoom memory and other internal memories on the acquisition chip.

Resource Bus Connection Test

The purpose of this test is to verify global resources.

Comparator Programming Test

The purpose of this test is to verify the programming path to each of the comparators.

Comparator/DAC Test

This test is executed only if all probes are detached.

This test uses the pod, bonus, and calibration DACs, the calibration oscillator (implemented in the interface FPGA), the comparators, the connections between the comparators and the Analysis chip, and the activity indicators in the Analysis chip. We verify that we can use the DACs to control the data input to the comparators. We verify that each comparator data channel produces output. We verify that each comparator output is connected to each ASIC data input.

Comparator Delay Test

The comparator delay test verifies the integrity of all the delay line elements for each delay line in the comparators. Each delay line consists of 11 delay elements. When set for maximum delay, all 11 elements are connected in series. If any element is faulty, then data will not propagate through the comparator. If this is the only test failing, then it is almost certainly a bad comparator.

Comparator Zero-Hold Cal Test

Tests the delay elements for each delay line in the comparators. It tests that each delay line can increase its delay in a linear way through a range of delay values.

Comparator Calibrations Test

The purpose of this test is to verify that each of the comparator one-time calibrations can successfully be performed. This verifies that all of the calibration circuitry and components are within the tolerance limits required for proper calibration. This test is executed only if all probes are detached.

Acquisition Memory Write/Read Test

This test checks that each acquisition chip can write data to DDR acquisition memory and read the same data back.

Acquisition Memory Cell Test

Tests every bit of the DDR acquisition memory. The test verifies that every bit can be written to 0 and written to 1 and read back accurately.

ATB (AXIe Trigger Bus) Test

This test verifies the ATB signal connections between the acquisition chips, the interface FPGA and the two 8-bit transceiver chips.

To exit the test system

1 Close the self-test dialog. No additional actions are required.

To restore the system software

Restoring your system software might be necessary for the following reasons:

- Hard drive failure.
- Virus in the system or unstable system.
- Intentional disk clean - for example if you are passing the system to another team or returning it to a rental company and you do not want any data left on it.

The 16860 series of Logic Analyzers have the Windows 7 operating system installed. These systems also have the Keysight Logic and Protocol Analyzer software version 6.30 or later preinstalled.

If you need to restore the logic analysis system software, you run the recovery process on the hard drive of the system. This recovery process uses the hidden partition on the hard drive to restore the hard disk drive back to its original state in which it was shipped. When you run this process, the recovered hard disk drive contains:

- the Windows 7 operating system
- the version of the Logic Analyzer software which was installed when the system was originally shipped and not the latest or upgraded version of the software that might be available at the time of system recovery.
- the license files of any licensed optional products that you had purchased with the Logic Analyzer and that were installed when the system was originally shipped.

NOTE When you run the recovery process, the software licensing Host ID of your logic analyzer may change. If this happens, the restored license files will not work with the new host ID and you will need rehosted license files. To get these files, you can contact your nearest Keysight sales/service office. To locate a sales or service office, go to www.keysight.com/find/contactus.

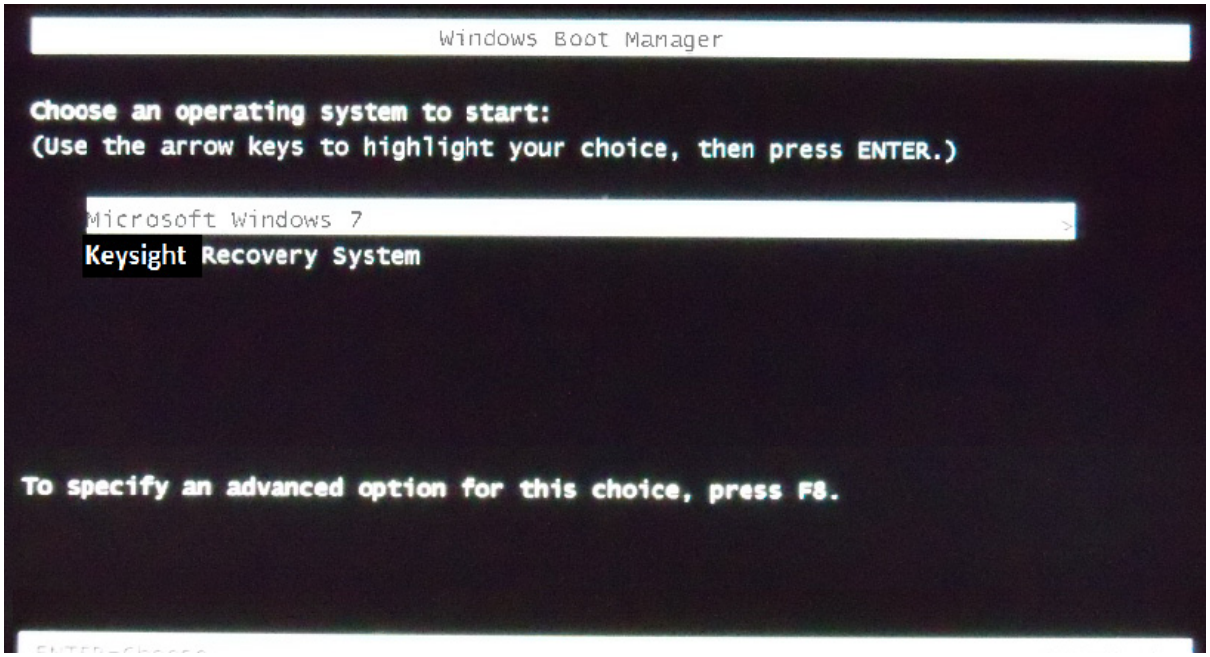
CAUTION Running the recovery process reformats your logic analyzer's hard disk drive to the state in which it was originally shipped to you. All user data files and programs are overwritten when the recovery process runs. Therefore, save your data to a CD or to another machine before you start recovering the system software.

To run the recovery process

1 Shut down and then restart your Logic Analyzer.

While booting up, the Logic Analyzer displays the Windows Boot Manager screen. This screen provides you the following options:

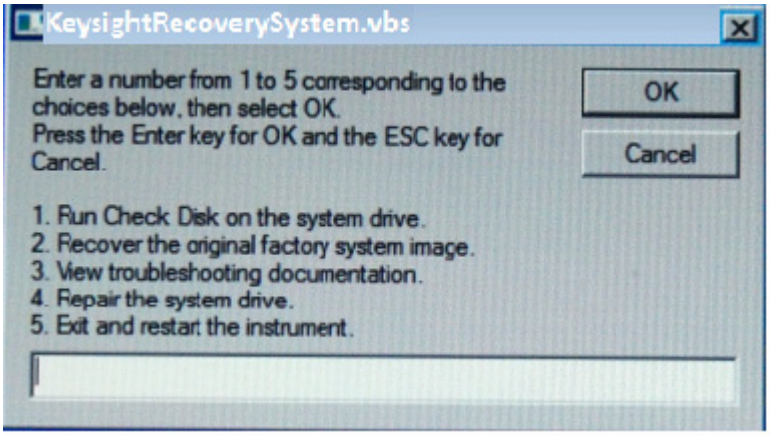
- Microsoft Windows 7 - This is the default selected option. This option starts the Logic Analyzer with the Windows 7 operating system. This is the normal startup of the system.
- Keysight Recovery system - You should select this option when you want to restore/repair your Logic Analyzer software by running the Keysight recovery process.



2 After a few seconds, Logic Analyzer automatically starts with the option selected in the Windows Boot Manager. Select the Keysight Recovery system option in the Windows Boot Manager screen using the arrow keys and then press Enter.

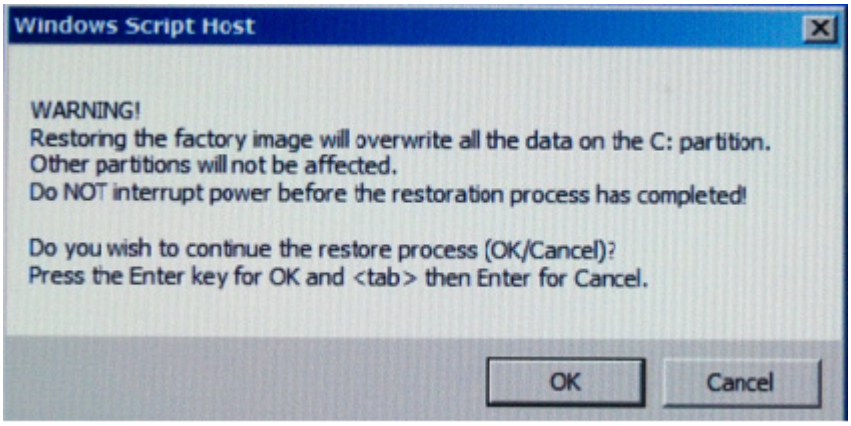
The recovery process starts preparing the system for recovery and displays the following screen with options to choose. You can enter:

- 1 to run Check Disk on the Logic Analyzer's hard disk drive. If the recovery process encounters any problems while running Check Disk, it reports these problems else it returns to the Keysight Recovery system prompt on completion of Check Disk.
- 2 to restore your Logic Analyzer software back to its original state in which it was shipped.
- 3 to view a document that provides information on the recovery process.
- 4 to repair the Logic Analysis system hard disk drive.
- 5 to exit the recovery process and restart the Logic Analyzer in the normal mode.



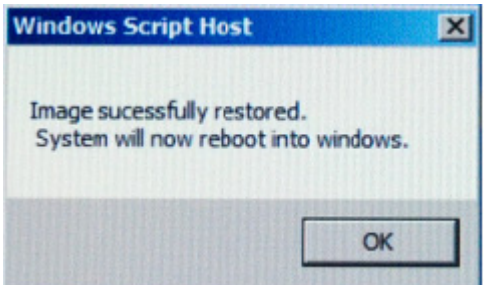
3 Select the second option in the above screen by entering 2 in the text box and clicking OK.

4 A warning message is displayed stating that the recovery process overwrites the data on C: drive. If you want to save your data to a CD or to another machine before you proceed further, then exit the recovery process and save your data. Else, click OK to proceed with the recovery process.



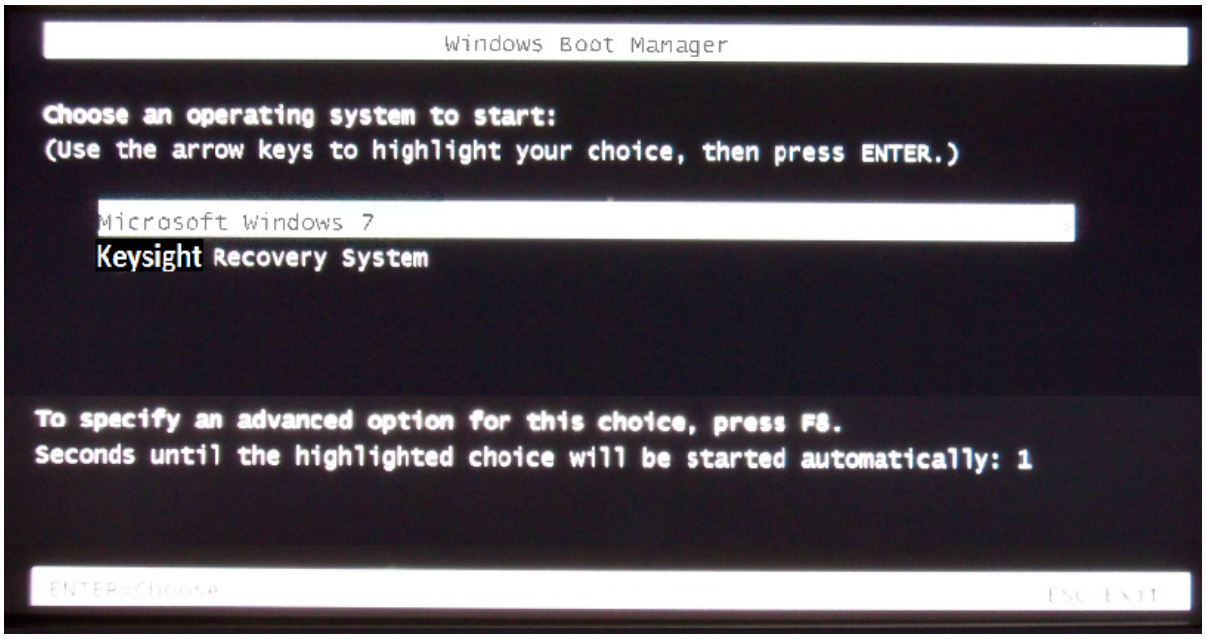
The recovery process starts.

If the recovery process is able to restore the system software successfully, then the following screen is displayed.



5 Click OK to proceed. You Logic Analysis system now reboots to Windows 7.

6 The Windows Boot Manager screen is displayed with Microsoft Windows 7 as the default selection. The system automatically starts with this default selection. Alternatively, you can press Enter to proceed with the default selection.



NOTE

There are situations when you are not able to run the recovery process, (for instance, when the hard disk drive of your system fails) or when running the recovery process does not recover your system software. In such situations, you can send your Logic Analysis system for hard disk repair/replacement to Keysight. Alternatively, you can contact your nearest Keysight sales/service office. To locate a sales or service office, go to www.keysight.com/find/contactus.

Contacting Keysight Service/Support

To locate a sales or service office near you, go to: http://www.keysight.com/find/contactus

To test the logic acquisition cables

This test allows you to functionally verify the logic analyzer cable and the flying lead probe of any of the logic analyzer pods. Only one probe and cable can be tested at a time. Repeat this test for each probe and cable to be tested. Two Flying Lead Probes are required if you need to test pods other than Pod 1 because the clock from Pod 1 will be used to acquire data.

This test allows you to functionally verify U4201A logic analyzer cables and Keysight E5379A probes.

Table 5 Equipment Required to Test Cables

Equipment	Critical Specification	Recommended Part
Stimulus Board	No Substitute	16760-60001
Differential Probes	No Substitute	E5379A (Qty 2)

1 Connect the 16860 logic analyzer to the stimulus board.

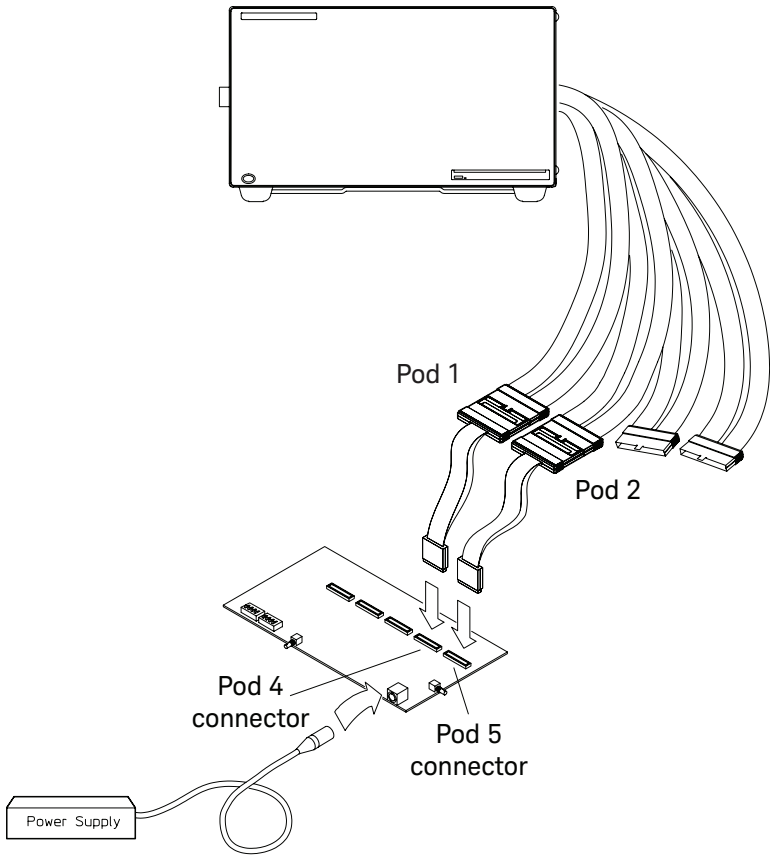
a Connect the Keysight E5379A 90-pin differential probes to the logic analyzer cable (also called “Pods”) to be tested. Start with Pods 1 and 2.

b Connect the E5379A probe from logic analyzer Pod 1 to connector “Pod 4” on the stimulus board.

c Connect the E5379A probe from logic analyzer Pod 2 to connector “Pod 5” on the stimulus board.

d Connect the stimulus board power supply output to the stimulus board power supply connector J82.

e Plug in the stimulus power supply to line power. The green LED DS1 should illuminate showing that the stimulus board is active.



2 Set up the stimulus board

a Configure the oscillator select switch S1 according to the following settings:

- S1 0 (Off).
- S2 1 (On).
- S3 0 (Off).
- Int.

b Configure the data mode switch S4 according to the following settings:

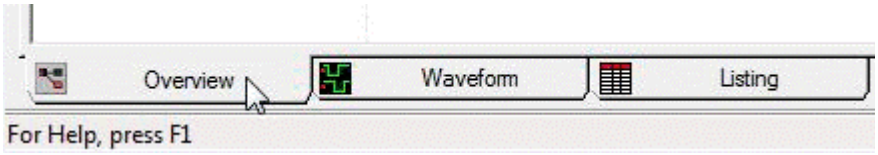
- Even.
- Count.

c Press the Resynch VCO button, then the Counter RST (Counter Reset) button.

3 In the *Keysight Logic and Protocol Analyzer* application, choose **File→New**. This puts the logic analysis system into its initial state.

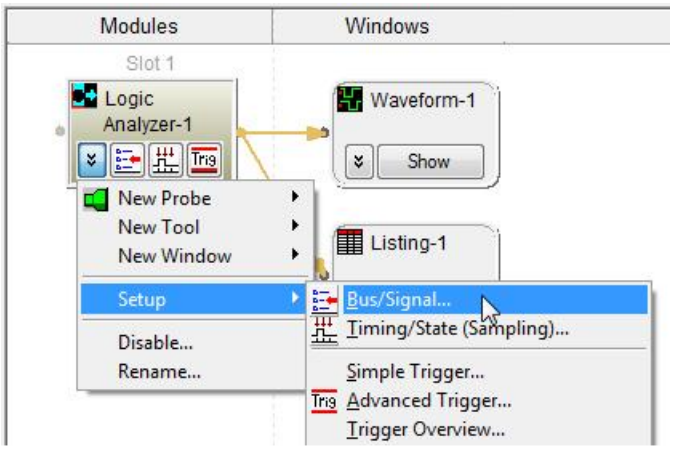
4 Disable all analyzers except the one being tested. This simplifies the instructions and makes module initialization faster.

a Select the **Overview** tab at the bottom of the main window.

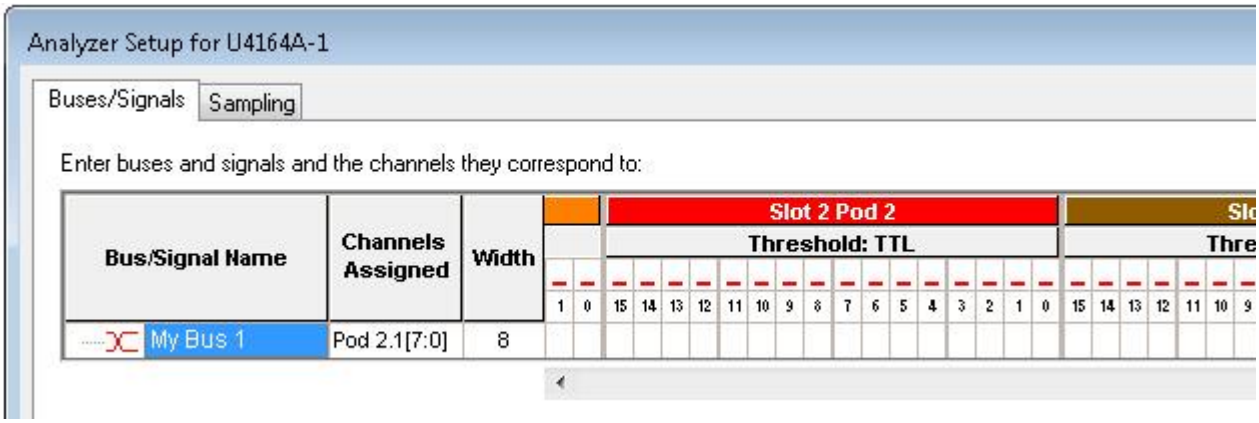


5 Set up the bus:

a In the **Overview** window, select **Setup -> Bus/Signal...** from the module's drop-down menu.

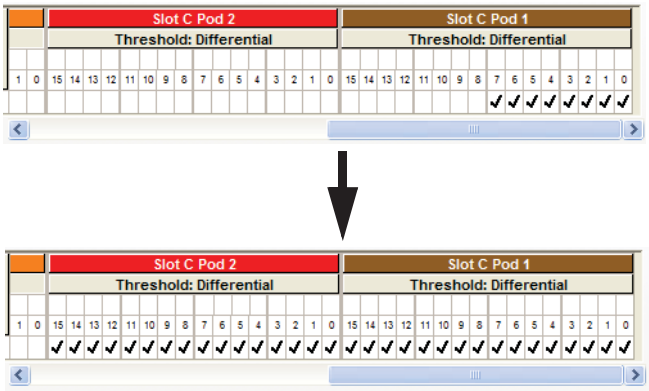


b Scroll if necessary to view the pods you are testing.



c Verify that the pod threshold buttons say "**Threshold: Differential**". If they don't, make sure the correct probes (E5379A) are attached to pods 1 and 2. The threshold is set to Differential automatically when E5379A probes are attached.

d Channels 7 through 0 are already assigned by default. Assign pod 2 channels 15 through 0 and pod 1 channels 15 through 8 by clicking and dragging from the left-most channel box to the right-most channel box. Your display should look like the lower picture when you are done.



6 Select the State sampling mode and set the State Clock options:

a Select the **Sampling** tab of the Analyzer Setup window.

b Select **State - Synchronous Sampling**.

c For State Clock, select **CLK1 Clock** and **Both edges**.

7 Set the trigger position and acquisition memory depth:

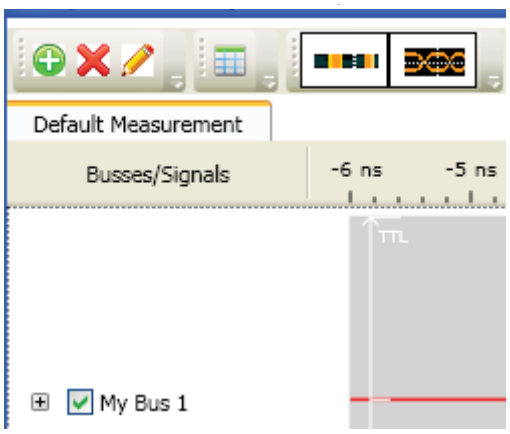
a Set the Trigger Position to **100% Poststore**.

b Set the **Acquisition Depth** to **8K**.

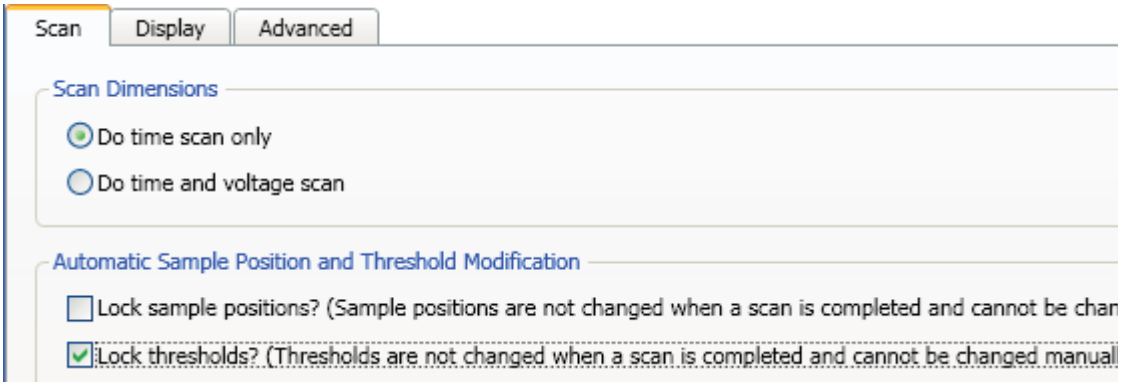
8 Adjust sampling positions:

a Click the **Eye Scan: Thresholds and Sample Positions** button. The **Eyescan - Sample Positions and Threshold Settings** dialog will appear.

b In the "Buses/Signals" section of the Eyescan - Sample Positions and Threshold Settings dialog, make sure the check box next to "My Bus 1" is checked.



c Click **Edit,** select the **Do time scan only** option as the scan dimension and then select the **Lock Thresholds** checkbox.



d Select the **Run This Measurement** button in the **Eyescan - Sample Positions and Threshold Settings** dialog.

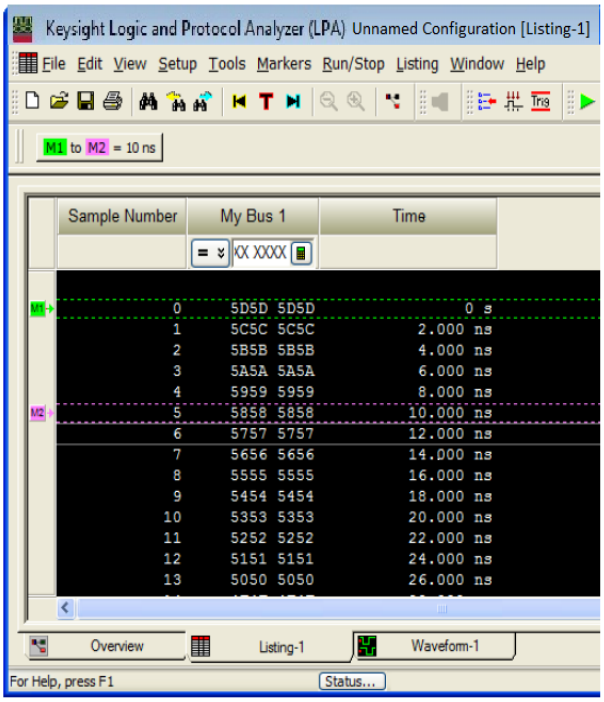
e Make sure the sampling positions are set properly, and re-align any stray channels if necessary.

f Select **OK** to close the **Eyescan - Sample Positions and THreshold Settings** window.

g Select **OK** to close the **Analyzer Setup** window.

9 Switch to the **Listing** window by selecting the **Listing** tab at the bottom of the main window.

10 Click the **Run** icon . The listing should look similar to the figure below when you scroll down a bit.



Scroll down at least 256 samples to verify the data. **My Bus 1** shows four 8-bit binary counters decrementing by 1. If the listing does not look similar to the figure, there is a possible problem with the cable or probe. Cause for cable test failures include:

- Open channel.
- Channel shorted to a neighboring channel.
- Channel shorted to either ground or a supply voltage.

If the test data is not correct, then perform the following step to isolate the failure.

11 Verify the failure:

a Swap the E5379A probes so that the pod 1 cable remains connected to the stimulus board's pod 4 connector and the pod 2 cable remains connected to the stimulus board's pod 5 connector – just using different probes.

b Click the **Run** icon .

If the failure is the same (that is, the error follows the cable) then the cable is faulty.

If the failure switches pods (that is, the error follows the E5379A probe) the probe is faulty.

12 Repeat the cable test for pods 3 and 4:

a Connect the logic analyzer's pod 3 cable to the stimulus board's pod 4 connector.

b Connect the logic analyzer's pod 4 cable to the stimulus board's pod 5 connector.

c In the **Buses/Signals** tab of the Analyzer Setup window, assign the pod 3 and 4 channels to "My Bus 1".

d In the **Sampling** tab of the Analyzer Setup window, for State Clock, select **Both edges**.

e Adjust sampling positions.

f Click the **Run** icon  . In the **Listing** window, check at least 256 samples for failures; if necessary, verify any failures by swapping the E5379A probes.

13 Repeat the cable test (step12) for pod pairs 5 and 6 and 7 and 8 connecting the odd pod cable to the stimulus board's pod 4 connector and the even pod cable to the stimulus board's pod 5 connector:

Return to the troubleshooting flowchart.

6 Removing, Replacing, or Returning 16860 Series Logic Analyzer Assemblies

If the 16860 series logic analyzer's assemblies/parts are found faulty and need to be repaired/replaced, refer to the procedures included in this chapter that guide you how to repair, replace, or return these to Keysight Technologies.

CAUTION Service instructions included in this chapter are for trained service personnel. Do not perform any service or attempt to remove/replace an assembly unless qualified to do so.

KEYSIGHT TECHNOLOGIES

Before you Start

Before you start any repair or replacement work on a 16860 logic analyzer, it is recommended that you perform the tasks described in this section and carefully read and follow the cautions and warnings included in this section.

CAUTION Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when performing any service to this instrument.

CAUTION Damage can occur to electronic components if you remove or replace assemblies when the instrument is on or when the power cable is connected. Do not attempt to remove or install an assembly with the instrument on or with the power cable connected.

WARNING Hazardous voltages exist on the power supply. To avoid electrical shock, disconnect power from the instrument before performing any repair, removal, or replacement procedures. After disconnecting the power, wait at least six minutes for the capacitors on the power supply board to discharge before servicing the instrument.

NOTE Some procedures in this chapter require you to remove other assemblies of the instrument, but do not provide complete instructions to remove these other assemblies. In such cases, refer to the removal procedure for that specific assembly for the instructions on how to remove it.

The pictures included in this chapter are representative. Your logic analyzer parts may look different from these pictures.

Repair Tools Needed

T10, T15, T20 TORX screwdrivers
#1 Pozi-drive screwdriver
5 mm nut driver
9/16" hex socket

Back Up Data and License Files

The logic analyzer license files contain keys for licensed software features of logic analyzer. It is recommended that you back up these license files and any data stored on the logic analyzer's hard drive to a USB flash drive before initiating any major repairs to the logic analyzer. The backup copy is needed to recover data if you encounter any problems that require re-imaging the logic analyzer's hard drive.

You can find the license files in the following directories:

C:\Program Files\Keysight Technologies\Logic Analyzer\License

C:\Program Files\Keysight Technologies\License Server\License Files

For Logic analyzers that use the Keysight License Manager, you can find the license files in the following directory:

C:\Program Files\Agilent\Licensing

If you lose the license files, you can obtain new licenses from Keysight Technologies by providing the licensing host ID.

To obtain the licensing host ID

- From the Keysight Logic and Protocol Analyzer application's main menu, choose **Help**>**Software Licensing....** The Licensing Host ID is displayed in the **Software Licensing** dialog's **Activation** tab.
- For Logic analyzers that use the Keysight License Manager, you can obtain the Keysight License Manager Host ID by performing the following steps:
  1. From the **Start** menu, choose **All Programs** > **Keysight License Manager** > **Keysight License Manager...**
  2. The Host ID is shown on the main page. Copy and paste this Host ID into a text file and then save this file.

Prepare the Logic Analyzer for Disassembly

1. Close the *Keysight Logic and Protocol Analyzer* application.
2. Power off the system using one of the methods described in the table below.
3. Remove the logic analyzer power cord.
4. Move the logic analyzer to a static safe work environment.

Follow cautions and warning listed on page 106 while preparing the Logic Analyzer for disassembly.

To power off the logic analyzer

There are several ways to power off the logic analyzer.

Method to Power Off	Description
Using the Windows Shutdown	1. On the logic analyzer desktop, click **Start** >**Shut Down**. This method of power off does the following: • Closes all programs that are running. • Writes all unsaved data to the disk. • Turns off the power supply. If the system is unplugged while it is off and then plugged back in, the system will not power on until the power button is pressed.
Using a Short Press of the Power Button	Press the power button on a logic analyzer frame for a short time (less than 2 seconds). This method of power off does the following: • Closes all programs that are running. • Writes all unsaved data to the disk. • Turns off the power supply.
Using a Long Press of the Power Button	Press the power button for more than 4 seconds. This will power off the system abruptly. Therefore, you should use this method only when other power off methods have not responded. This method of power off does the following: • Programs that are running will not be shut down. Any data that has not been written to the disk will be lost. • Turns off the power supply. If the system is unplugged while it is off and then plugged back in, the system will not power on until the power button is pressed. If the system does not boot, the hard disk drive will need to be re-imaged.
Unplugging the Power Cord or Power Loss	Unplugging power while the logic analyzer is on or a power loss is similar to the long press of the power button with the following exception: • When the system is plugged back in, it will power up and boot into Windows.

NOTE After powering off the logic analyzer, wait until the fans stop turning (about 15 seconds) before turning the logic analyzer back on. This ensures that internal circuitry restarts in a known state.

Removing and Replacing the Hard Drive, Acquisition Bezel, and Cover

Prerequisites

Ensure that you have completed the tasks listed in the "Before you Start topic.

If the accessory pouch is attached to the logic analyzer, detach the pouch using its four corners.

E5868A and E5869A Additional Removable SSDs

The 1686x-series logic analyzers have a removable Solid State Drive (SSD) imaged with Windows 10 operating system, Logic and Protocol Analyzer application software, and any optional application software ordered with the logic analyzer.

You can remove and replace this SSD with the additional removable SSD without disassembling the logic analyzer.

When to Use which Removable SSD

The following two models of additional removable SSDs are available for 1686x-series logic analyzers.

E5868A	E5869A
E5868A has the drive image required for 1686x-series logic analyzers with the older M900 motherboard.	E5869A has the drive image required for 1686x-series logic analyzers with the newer M910 motherboard.
This SSD has a lighter gray color panel with black text.	This SSD has a darker gray color panel with white text.
	

CAUTION To ensure that you are using the correct model of removable SSD for your 1686x logic analyzer, match the panel color of the additional SSD with the panel color of the SSD you are replacing.

To remove the hard drive, bezel, and cover

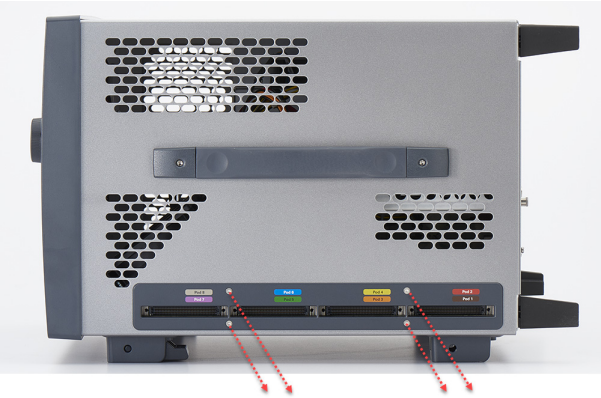
1 Using a flat screwdriver or fingers, loosen the two screws holding the logic analyzer removable hard drive.

Removable hard drive screws

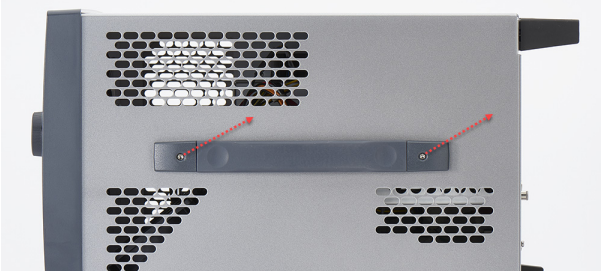
2 Pull the drive tray out to remove the hard disk drive.

3 Using a 5mm nut driver, small flat screwdriver, or fingers, remove any external acquisition cables attached to the logic analyzer.

4 Using a Torx T10 screwdriver, remove the four screws that secure the acquisition bezel, and then remove the acquisition bezel.

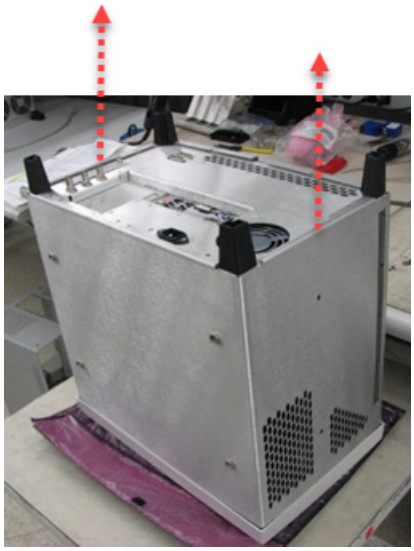


5 Using a Torx T20 screwdriver, remove the two screws that secure the handle assembly, and then remove the handle assembly.



6 While ensuring proper support to protect the front bezel and knob of the logic analyzer, seat the logic analyzer on its front face thereby bringing the back side on top. Using a Torx T10 screwdriver, remove the seven screws (indicated in the photo below) that secure the cover to the chassis.

7 Gently pull the cover upward to remove it.



8 Reverse this procedure to replace the cover, bezel, or hard drive.

CAUTION When reinstalling the handle assembly, ensure that the screws are torqued to 2.372 Newton meters (21 inch pounds) so that they do not work themselves loose.

Removing and Replacing the Front Panel

Prerequisites

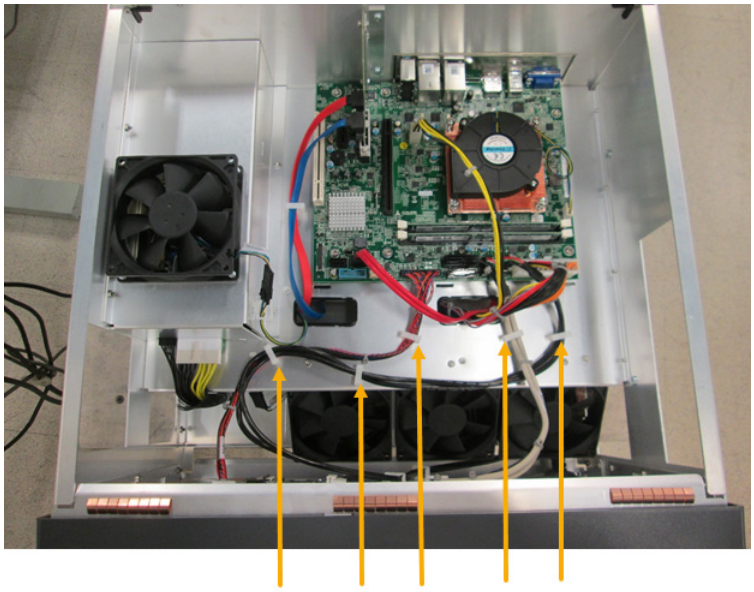
Ensure that you have:

- completed the tasks listed in the "Before you Start topic.
- removed the cover using the procedure listed in "Removing and Replacing the Hard Drive, Acquisition Bezel, and Cover" on page 109.

To remove and replace the front panel of 16860 logic analyzer

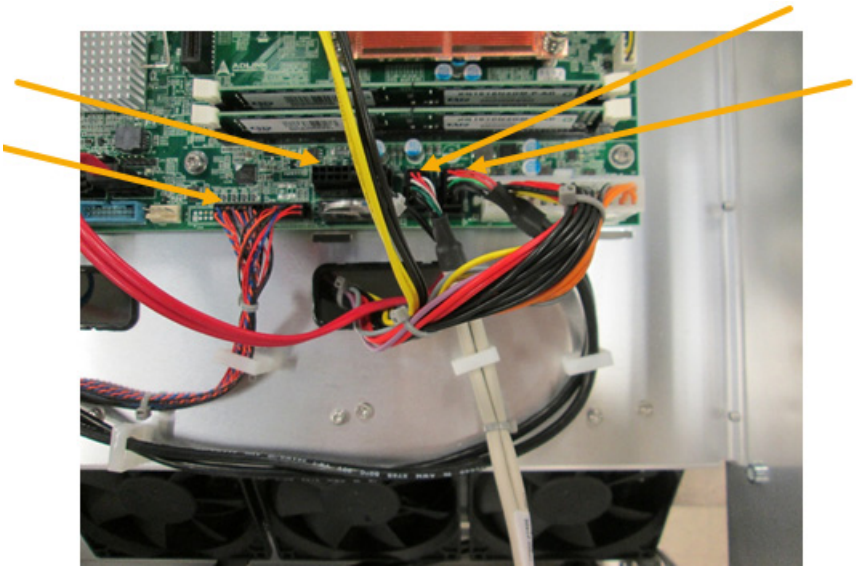
1 From the top of the logic analyzer unit, open the clips that are located around the four cables – *Touchscreen*, *USB*, and *Display* cables. These clips are pointed out in the photo below.

CAUTION Be cautious not to remove these cable clips while opening.

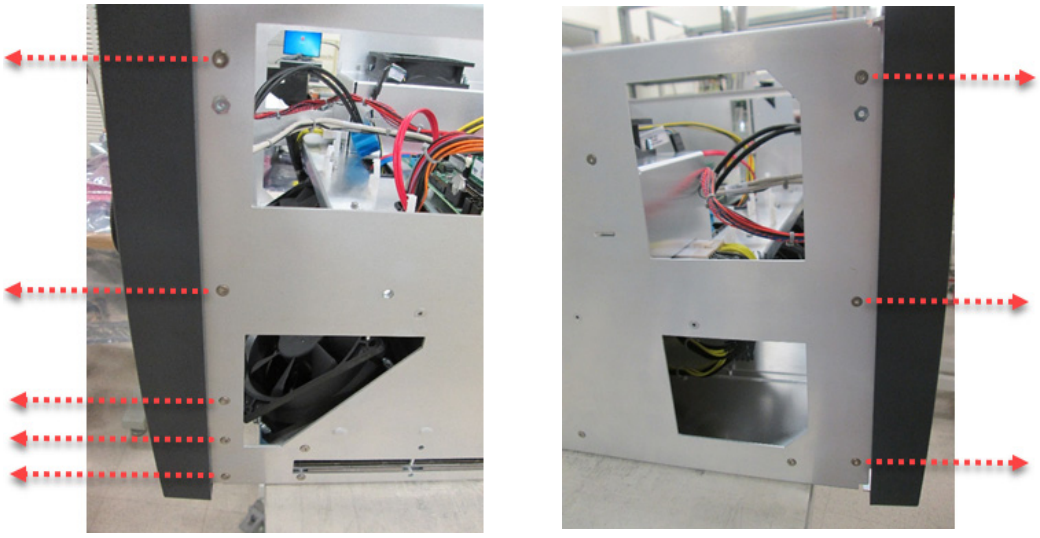


2 Disconnect the four connections (for Touchscreen, USB, and Display cables). These connections are pointed out in the following photo.

CAUTION Before disconnecting the connectors, cautiously look for and open the clips, if any, around these connectors.



3 Using a Torx T10 screwdriver, remove the eight screws (as indicated in the photos below) that secure the front panel to the chassis. The left and right sides of the instrument are displayed in the photos below.



4 Lift the front panel assembly slightly and remove it.

5 Reverse this procedure to install the front panel assembly.

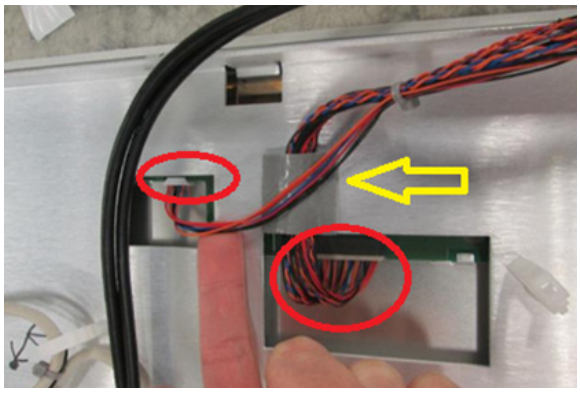
Disassembling the Front Panel

After you have removed the front panel assembly using the procedure described above, you can disassemble the front panel using the procedure given below.

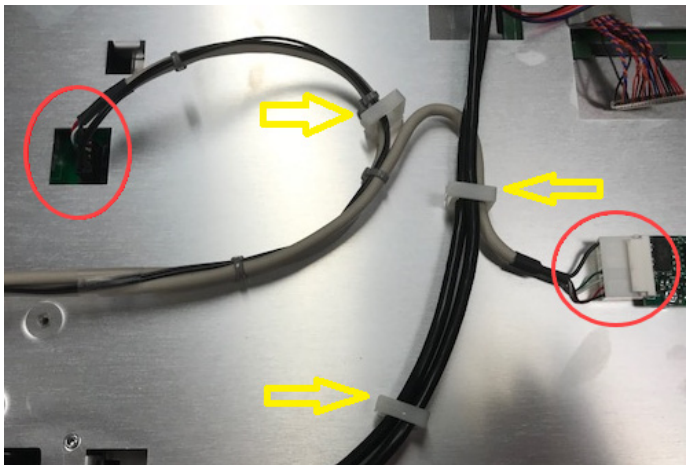
1 Remove the knob on the front panel by gently pulling the knob forward.

2 Carefully disconnect the backlight cable from the two locations on the front panel highlighted in the following photo.

CAUTION **Do not remove the backlight cable from the open-faced adhesive panel unless you need to replace this cable.**

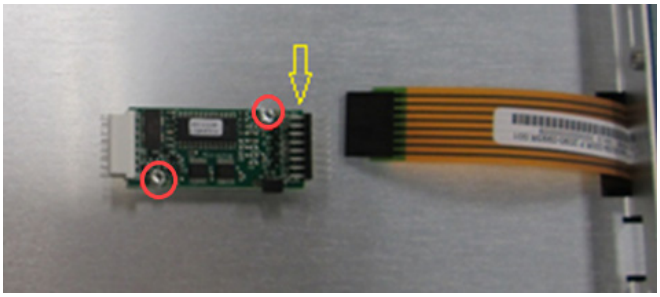


3 Remove the touchscreen cable from the front panel. To do this, first unclip the three clips that hold this cable to the front panel. These clips are pointed out in the photo below. Then disconnect the cable from the two locations encircled in red in the photo below.

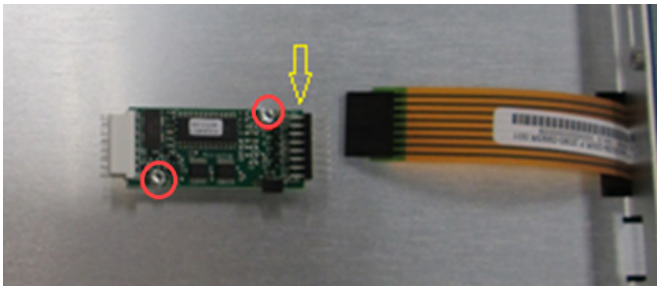


4 Disconnect the touchscreen flat cable from the USB Controller Board as pointed out in the photo below.

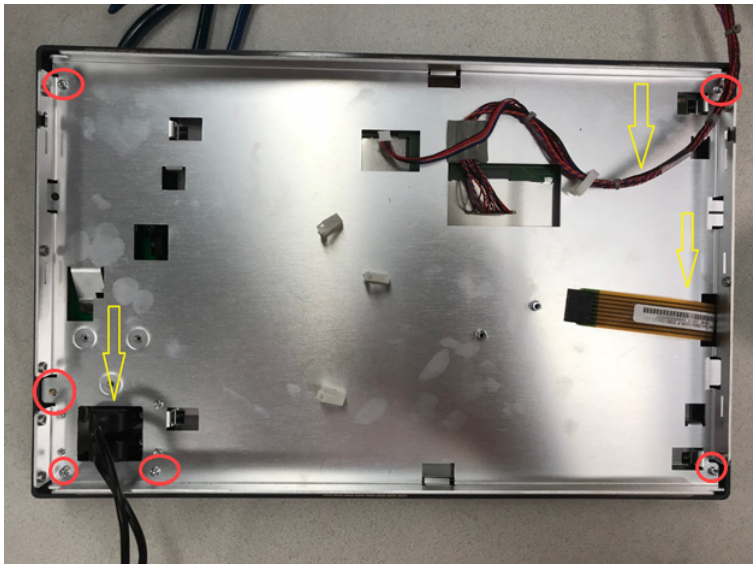
NOTE For reinstallation later, note that the touchscreen flat cable is connected to the lower pins on the USB Controller Board as pointed out in the photo below.



5 Remove the USB Controller Board from the front panel by removing the two screws encircled in the photo below. If necessary, use a Torx T10 screwdriver to remove these.



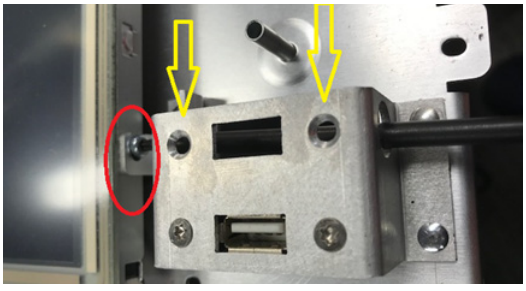
6 Using a Torx T10 screwdriver, remove the six screws that secure the LCD assembly to the front bezel. These screws are encircled in the photo below. Then carefully uninstall the LCD Assembly from the front bezel while ensuring that the three cables on the LCD panel are handled with care. These cables are pointed out in the photo below.



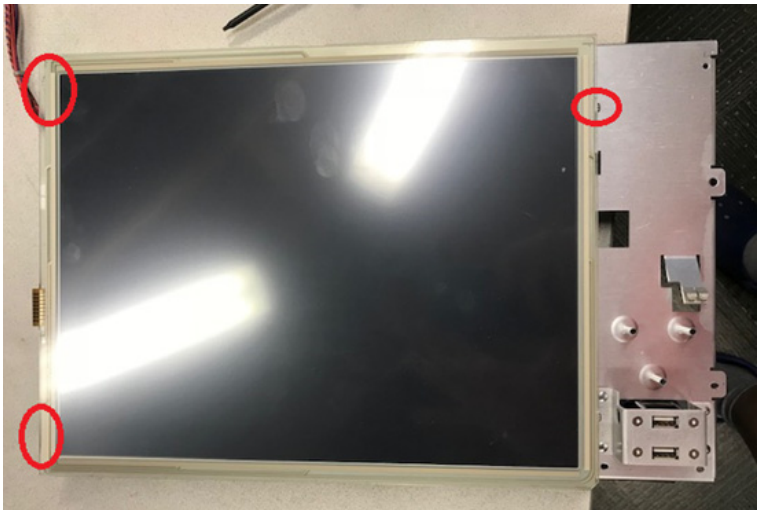
7 Remove the LCD panel from the LCD assembly by performing the following substeps:

a Place the disconnected LCD assembly on the bench with the LCD panel facing up. Be careful of the three cables still attached to the LCD panel.

b Remove the upper USB plug by removing the two screws using a Torx T10 screwdriver. These two screws are pointed out in the photo below. Then thread the Torx T10 screwdriver through the bracket to loosen the screw holding the LCD panel. This screw is encircled in the photo below. Ensure that this screw is just loosened and not removed.



c Remove the other three screws that secure the LCD panel to the LCD assembly. These three screws are encircled in the photo below. Then remove the LCD panel while taking care of the flat cable on the left side of the LCD panel. You may have to do gentle twisting to remove the LCD panel.



Removing and Replacing the Fan Deck

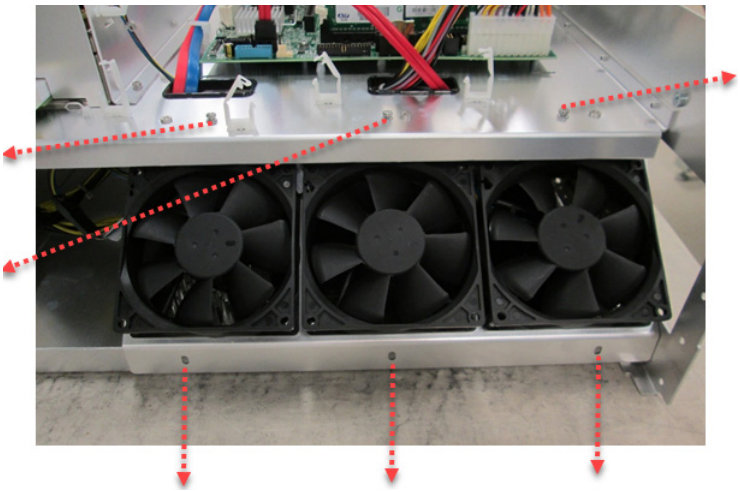
Prerequisites

Ensure that you have:

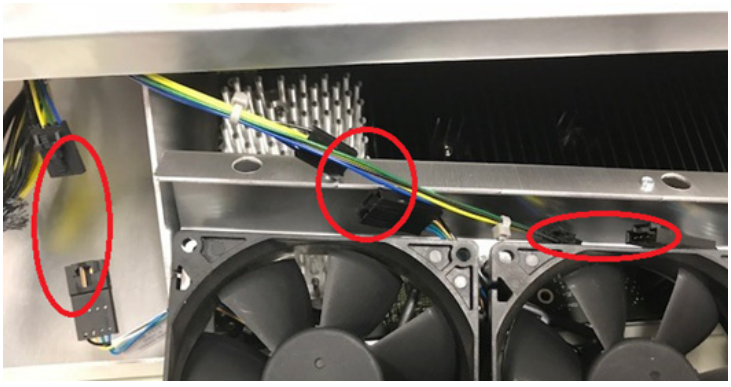
- completed the tasks listed in the "Before you Start topic.
- removed the cover using the procedure listed in "Removing and Replacing the Hard Drive, Acquisition Bezel, and Cover" on page 109.
- removed the front panel using the procedure listed in "Removing and Replacing the Front Panel" on page 113.

To remove and replace the fan deck assembly of 16860 logic analyzer

1 Using a Torx T25 screwdriver. remove the six screws (as indicated in the photo below) that secure the fan deck assembly to the chassis. Then carefully remove the fan deck assembly.



2 From the fan deck assembly, disconnect the three fan control cables (as encircled in the photo below). Then remove the fan.



3 Reverse this procedure to replace the fan.

Removing and Replacing the Acquisition Tray

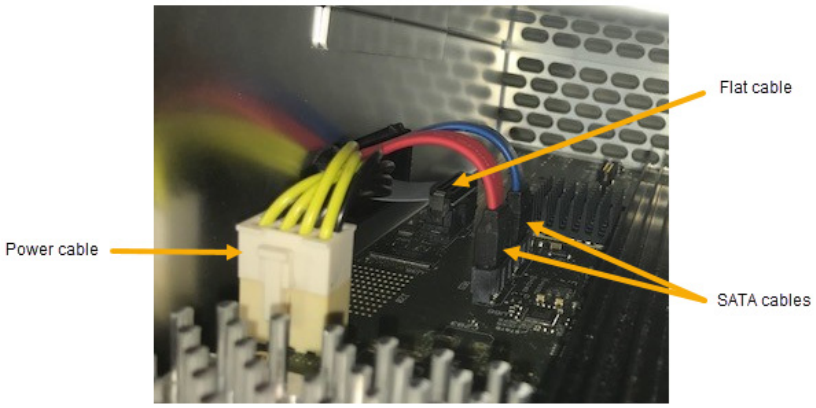
Ensure that you have:

- completed the tasks listed in the "Before you Start topic.
- removed the cover using the procedure listed in "Removing and Replacing the Hard Drive, Acquisition Bezel, and Cover" on page 109.
- removed the front panel using the procedure listed in "Removing and Replacing the Front Panel" on page 113.

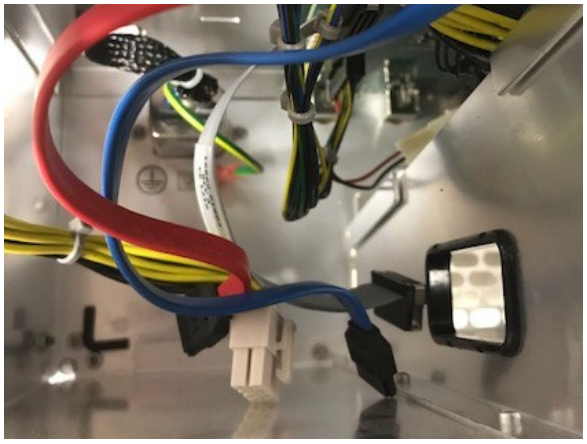
To remove and replace the acquisition tray of 16860 logic analyzer

1 Disconnect the four (*Power, SATA, and flat*) cables from the acquisition board. These cables are pointed out in the following photo.

NOTE For reconnection later, note the relative locations of red and blue SATA cables.

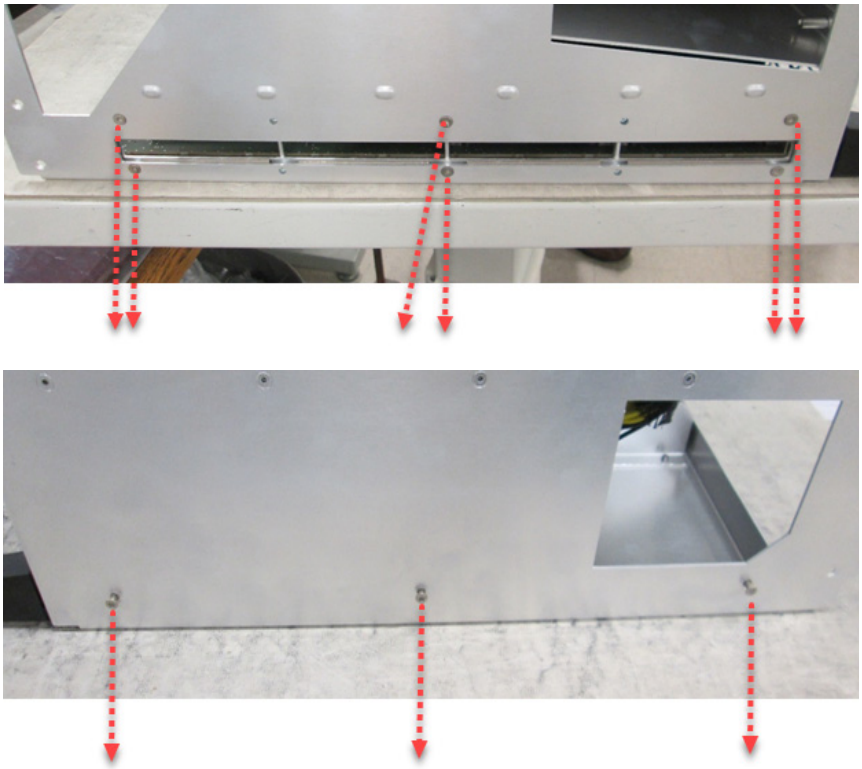


2 Unthread the cables back through the grommeted hole.



3 Using a Torx T10 screwdriver, remove the following screws securing the tray assembly to the chassis:

Nine screws from left and right sides of the chassis



Two screws from rear of the chassis

4 Carefully slide the acquisition tray out of the chassis while ensuring that the gasket on the tray does not snag during removal.

5 Reverse this procedure to replace the tray assembly.

Removing and Replacing the Duct

Prerequisites

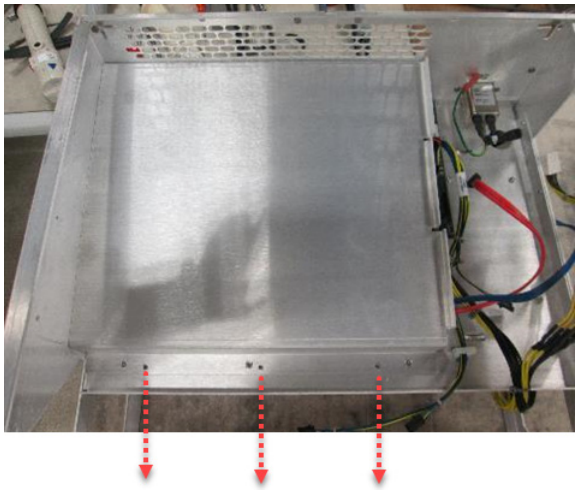
Ensure that you have:

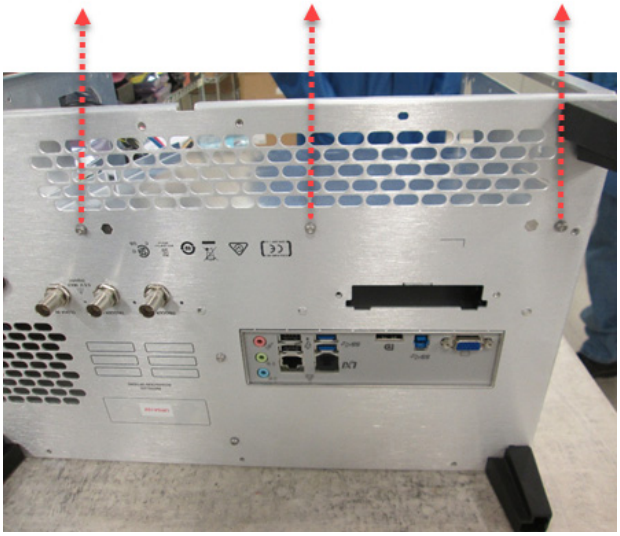
- completed the tasks listed in the "Before you Start topic.
- removed the cover using the procedure listed in "Removing and Replacing the Hard Drive, Acquisition Bezel, and Cover" on page 109.
- removed the front panel using the procedure listed in "Removing and Replacing the Front Panel" on page 113.

To remove and replace the duct of 16860 logic analyzer

1 Keep the chassis upside down on the bench.

2 Remove the six screws on the side and rear of the chassis as indicated in the two photos below,





3 Slide the duct off two standoffs, and then lift it out to remove it.

Removing and Replacing the Motherboard

Prerequisites

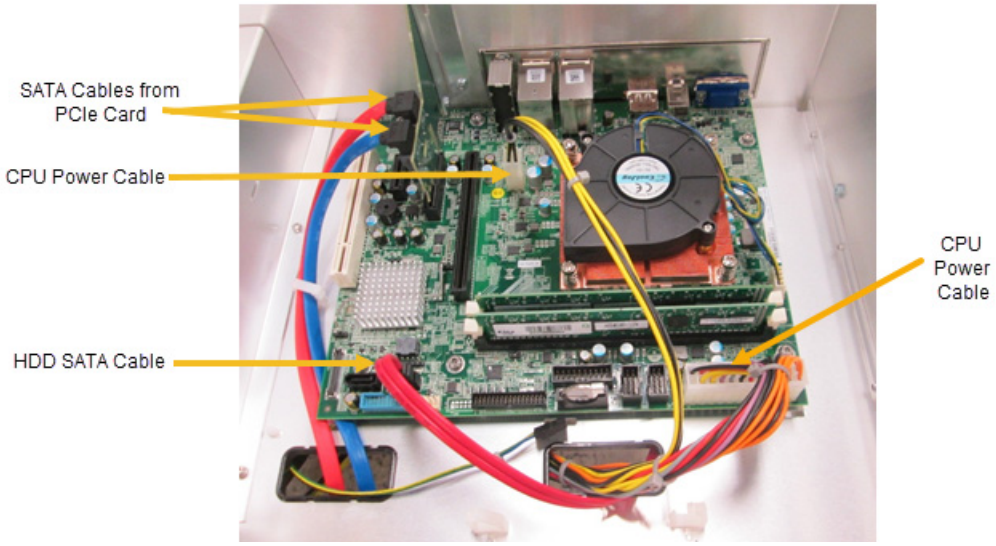
Ensure that you have:

- completed the tasks listed in the "Before you Start topic.
- removed the cover using the procedure listed in "Removing and Replacing the Hard Drive, Acquisition Bezel, and Cover" on page 109.
- removed the front panel using the procedure listed in "Removing and Replacing the Front Panel" on page 113.

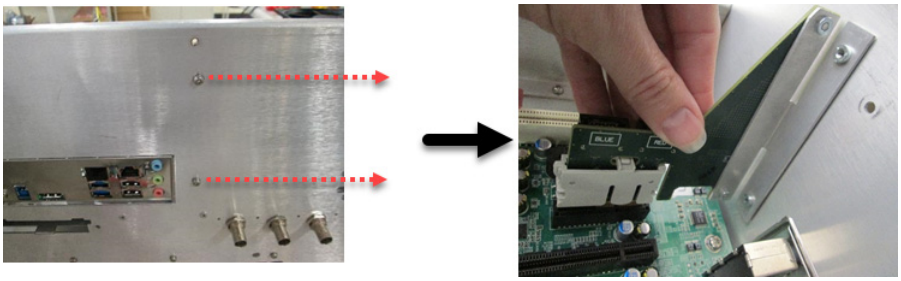
To remove and replace the motherboard of 16860 logic analyzer

1 Disconnect the following cable connections from the motherboard. These are labeled in the photo below.
   - CPU power cables (2 connections)
   - Hard drive SATA cable (1 connection)
   - SATA cables from PCIe card (2 connections)

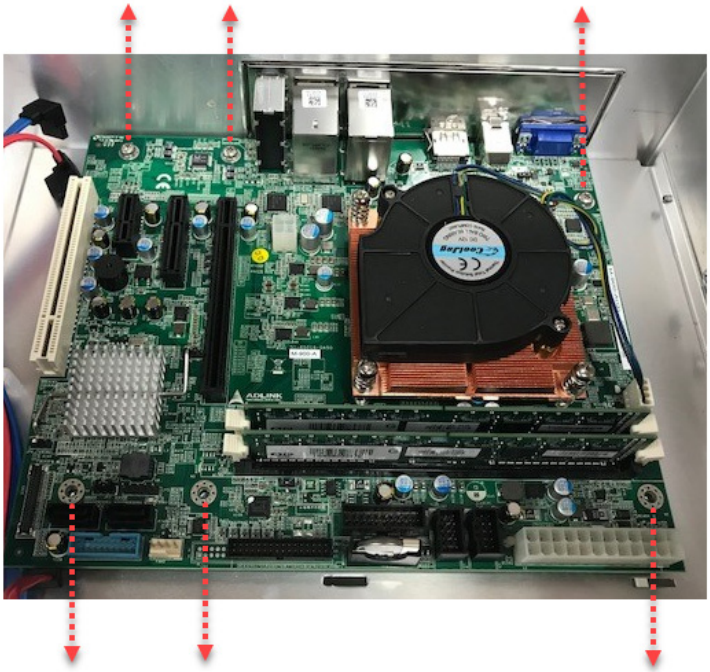
NOTE For reconnection later, note down the relative locations of the red and blue SATA cables from PCIe card.



2 Remove the PCIe card from the motherboard by removing the two screws that secure this card. These screws can be found at the rear of the chassis as displayed in the following photo.



3 Using a Torx T15 screwdriver, remove the six screws that secure the motherboard. These are indicated in the photo below.



4 Remove the motherboard.

5 Reverse this procedure to install the motherboard.

Removing and Replacing the FIB Board

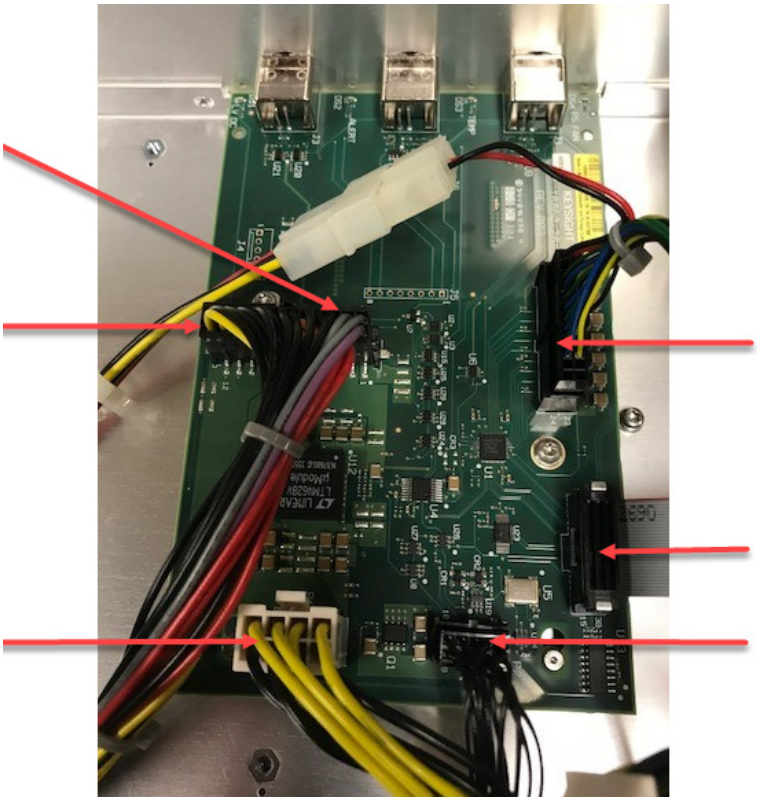
Prerequisites

Ensure that you have:

- completed the tasks listed in the "Before you Start topic.
- removed the cover using the procedure listed in "Removing and Replacing the Hard Drive, Acquisition Bezel, and Cover" on page 109.
- removed the front panel using the procedure listed in "Removing and Replacing the Front Panel" on page 113.

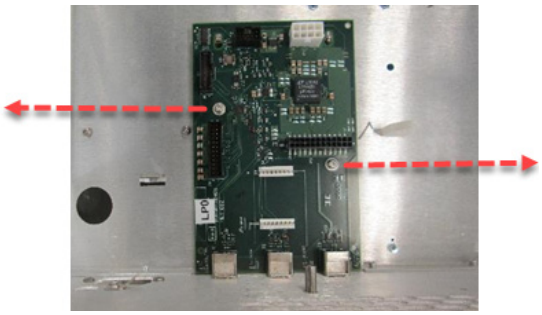
To remove and replace the FIB board of 16860 logic analyzer

1 Disconnect all the cables connected to the FIB board as indicated in the photo below. Before removing, note the locations of these cables for reconnection. If these cable connections are loose, set these aside.



2 Using a 9/16" hex socket, remove the three nuts and three washers from the rear panel.

3 Remove the FIB board by removing the two screws (displayed below) that secure the FIB board to the rear panel. Use a Torx T10 screwdriver.



4 Slide the FIB board slightly forward, lift slightly, then slide it forward and out.

5 Reverse this procedure to install the FIB board.

Removing and Replacing the Power Supply Shroud and Power Supply

WARNING Hazardous voltages exist on the power supply. To avoid electrical shock, disconnect the power from the instrument before performing the following procedures. After disconnecting the power, wait at least six minutes for the capacitors on the power supply board to discharge before servicing the instrument.

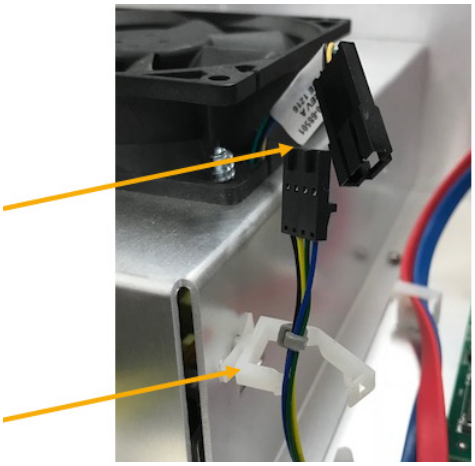
Prerequisites

Ensure that you have:

- completed the tasks listed in the "Before you Start topic.
- removed the cover using the procedure listed in "Removing and Replacing the Hard Drive, Acquisition Bezel, and Cover" on page 109.
- removed the front panel using the procedure listed in "Removing and Replacing the Front Panel" on page 113.

To remove and replace the power supply and its shroud

1 Unclip and then disconnect the Fan power cable as shown in the photo below.



2 Using a Torx T10 screwdriver, remove the four screws that secure the power supply shroud to the frame. Two of these screws are located inside the frame and remaining two are located outside the frame. These screws are displayed in the photos shown below.

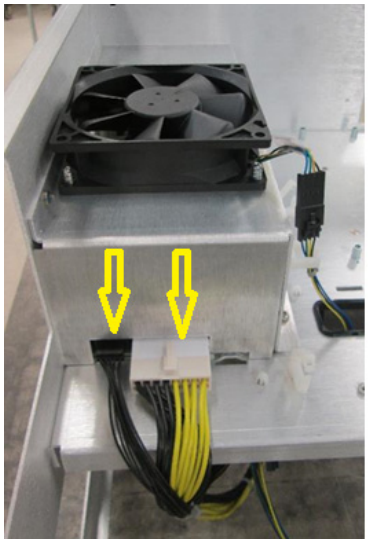
s

Two screws inside the frame

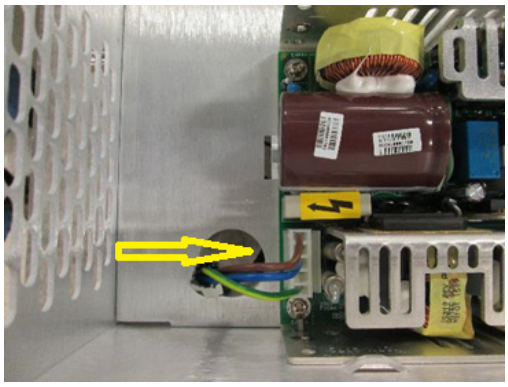
Two screws outside the frame

3 Lift the power supply shroud out and remove it.

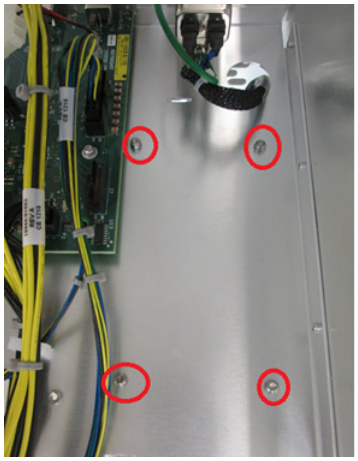
4 Disconnect the 12V **STDBY** power cables from the power supply



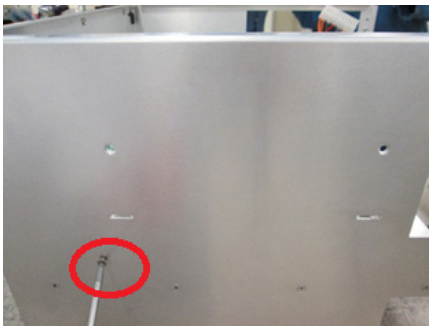
5 Disconnect the AC power cable.



6 Turn the chassis upside down and with a T10 Torx screwdriver, remove the four screws holding it in place.



7 Turn the chassis right side up and with a T10 Torx screwdriver, remove 1 screw through the side of the chassis, and then remove the power supply.



8 Reverse this procedure to install the power supply and its shroud.

Replacing the Battery

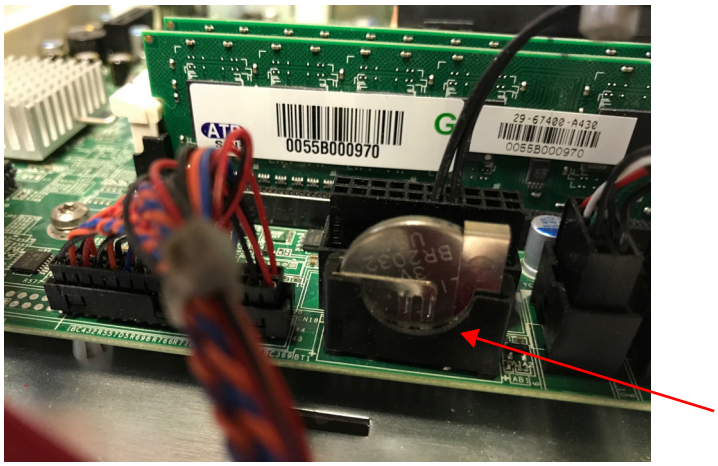
Prerequisites

Ensure that you have:

- completed the tasks listed in the “Before you Start topic.
- removed the cover using the procedure listed in “Removing and Replacing the Hard Drive, Acquisition Bezel, and Cover" on page 109.
- removed the front panel using the procedure listed in “Removing and Replacing the Front Panel" on page 113.

To replace the battery

1 If the battery needs to be replaced, use the **BR2023, 3 V, Poly-Carbonmonofluoride Lithium** battery. The battery location is shown below.



Returning the 16860 Series Logic Analyzer or its Assemblies

Before shipping the 16860 series logic analyzer or its assemblies to Keysight Technologies, contact your nearest Keysight Technologies Sales Office for additional details. Information on contacting Keysight can be found at www.keysight.com/find/contactus.

1 Write the following information on a tag and attach it to the logic analyzer/cable.
   - Name and address of owner.
   - Model number.
   - Serial number.
   - Description of service required or failure indications.

2 Remove accessories from the instrument.

   Only return accessories to Keysight Technologies if they are associated with the failure symptoms.

3 Package the instrument/cable.

   You can use either the original shipping containers, or order materials from an Keysight Technologies sales office.

CAUTION **For protection against electrostatic discharge (ESD), package the module in ESD-safe material.**

4 Seal the shipping container securely, and mark it FRAGILE.

7 Replaceable Parts

This chapter contains information for identifying and ordering replaceable parts for a 16860 Series logic analyzer.

Ordering Replaceable Parts

To order a part, visit us on the web at www.parts.keysight.com or call us in the United States at 1-877-447-7278. Or, you can contact your nearest Keysight Technologies Sales Office for assistance. To locate a sales office near you, go to www.keysight.com/find/contactus.

Exchanging Assemblies

Some assemblies are part of an exchange program with Keysight Technologies. The exchange program allows you to exchange a faulty assembly with one that has been repaired and performance verified by Keysight Technologies.

After you receive the exchange assembly, return the defective assembly to Keysight Technologies. A United States customer has 30 days to return the defective assembly. If you do not return the defective assembly within the 30 days, Keysight Technologies will charge you an additional amount.

This amount is the difference in price between a new assembly and that of the exchange assembly.

For orders not originating in the United States, contact your nearest Keysight Technologies Sales Office for information. To locate a sales office near you, go to www.keysight.com/find/contactus.

For more information on returning assemblies, see “Returning the 16860 Series Logic Analyzer or its Assemblies" on page 131.

Replaceable Parts List

Part Number	Part Description	For Product Model(s)
0960-2796	Touch Screen Controller Board 5V-DC	All models in 16860-series
0960-3207	Motherboard Industrial FlexATX i5-3550S Q77-PCH 8GB	All models in 16860-series
1400-3658	Saddle-Wire snap-in self-locking 16.8X5X14.6-mm Nylon 6/6 Natural	All models in 16860-series
16800-47402	Keypad-touchscreen	All models in 16860-series
16860-0010	Chassis, 1686xA series	All models in 16860-series
16860-04102	Outer cover assembly, 1686xA series	All models in 16860-series
16860-41001	Foot, side	All models in 16860-series
16860-47401	Knob	All models in 16860-series
16860-61601	Cable, AC input	All models in 16860-series
16860-61602	ATX/CPU Power	All models in 16860-series
16860-61603	Cable, 12v bulk standby	All models in 16860-series
16860-61604	Cable, trig/sense	All models in 16860-series
16860-61605	Cable, fan/SSD power	All models in 16860-series
16860-61606	Cable, front panel/touch	All models in 16860-series
16860-61609	Cable, LVDS/Backlight for 45 Display	All models in 16860-series
16860-66402	PCA, front panel 1686xA series	All models in 16860-series
16860-66501	Tested acquisition board assembly, 34 and 68 channel for 16861A or 16862A	16861A 16862A
16860-66502	Tested acquisition board assembly, 102 and 136 channel for 16863A or 16864A	16863A 16864A
16860-66503	Tested Frame Interface Board (FIB) PCA	All models in 16860-series
16860-68501	Fan assembly	All models in 16860-series
16860-68703	Power supply - preset for 1686xA	All models in 16860-series

Part Number	Part Description	For Product Model(s)
16860-68704	PCI Board with bracket	All models in 16860-series
16860-68705	Touchscreen front panel assembly	All models in 16860-series
16860-68723	Removable SSD assembly for E5869A Additional Removable SSD	All models in 16860-series with the newer M910 motherboard
16860-68715	Removable SSD assembly E5868A Additional Removable SSD	All models in 16860-series with the older M900 motherboard
16860-68707	Handle assembly	All models in 16860-series
16860-68708	Fan bracket assembly	All models in 16860-series
16860-68711	Motherboard assembly	1686xA
16860-69501	Refurbished tested acquisition board assembly, 34 and 68 channel for 16861A or 16862A, Exchange	16861A 16862A
16860-69502	Refurbished tested acquisition board assembly, 102 and 136 channel for 16863A or 16864A, Exchange	16863A 16864A
16861-22201	Bezel, 1686xA series	All models in 16860-series
16861-94301	Label, ID 16861A	16861A
16862-94301	Label, ID 16862A	16862A
16863-94301	Label, ID 16863A	16863A
16864-94301	Label, ID 16864A	16864A
16901-61602	Cable-usb dual	All models in 16860-series
2090-0993	Display-Touch Screen 15-in 330.08X254.9X2.215-mm 8-wire resistive	All models in 16860-series
3160-4454	Assembly-Fan with heat-sink 12VDC 92.45X89X30.81mm	All models in 16860-series
5090-4833	Grabber Kit Assembly	All models in 16860-series
54110-40502	Foot-rear	All models in 16860-series
54709-62302	Accessory Pouch	All models in 16860-series
54904-45202	Housing - PCIe cable snap	All models in 16860-series
54904-45203	Housing - PCIe cable receptacle	All models in 16860-series

Part Number	Part Description	For Product Model(s)
54911-94309	Label- PCIO	All models in 16860-series
54932-21204	Bracket - Motherboard	All models in 16860-series
54964-41001	Foot - base	All models in 16860-series
54964-41002	Foot - Tilt Lever	All models in 16860-series
8121-2893	Cable-Assembly SATA Straight to Right-angle 26-AWG 7-Conductor 0.5m Red	All models in 16860-series
8121-2894	Cable-Assembly SATA Straight to Right-angle 26-AWG 7-Conductor 0.5m Blue	All models in 16860-series
8160-1884	Gasket EMI Fingerstock 0.37-in-Wide 0.13-in-THK 16-in-LG Be-Cu bright Sn-plating	All models in 16860-series

NOTE If the battery needs to be replaced, use the BR2023, 3 V, Poly-Carbonmonofluoride Lithium battery.

Index