DDR/LPDDR Post Process Compliance Tool

User Guide

KEYSIGHT TECHNOLOGIES

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CAUTION

A CAUTION notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

Safety Summary

The following general safety precautions must be observed during all phases of operation of this instrument. Failure to comply with these precautions or with specific warnings or operating instructions in the product manuals violates safety standards of design, manufacture, and intended use of the instrument. Keysight Technologies assumes no liability for the customer's failure to comply with these requirements. Product manuals are provided with your instrument on CD-ROM and/or in printed form. Printed manuals are an option for many products. Manuals may also be available on the Web. Go to www.keysight.com and type in your product number in the Search field at the top of the page.

General Do not use this product in any manner not specified by the manufacturer. The protective features of this product may be impaired if it is used in a manner not specified in the operation instructions.

Before Applying Power Verify that all safety precautions are taken. Make all connections to the unit before applying power. Note the instrument's external markings described in “Safety Symbols”.

Ground the Instrument If your product is provided with a grounding type power plug, the instrument chassis and cover must be connected to an electrical ground to minimize shock hazard. The ground pin must be firmly connected to an electrical ground (safety ground) terminal at the power outlet. Any interruption of the protective (grounding) conductor or disconnection of the protective earth terminal will cause a potential shock hazard that could result in personal injury.

Fuses See the user's guide or operator's manual for information about line-fuse replacement. Some instruments contain an internal fuse, which is not user accessible.

Do Not Operate in an Explosive Atmosphere Do not operate the instrument in the presence of flammable gases or fumes.

Do Not Remove the Instrument Cover Only qualified, service-trained personnel who are aware of the hazards involved should remove instrument covers. Always disconnect the power cable and any external circuits before removing the instrument cover.

Cleaning Clean the outside of the instrument with a soft, lint-free, slightly dampened cloth. Do not use detergent or chemical solvents.

Do Not Modify the Instrument Do not install substitute parts or perform any unauthorized modification to the product. Return the product to an Keysight Sales and Service Office for service and repair to ensure that safety features are maintained.

In Case of Damage Instruments that appear damaged or defective should be made inoperative and secured against unintended operation until they can be repaired by qualified service personnel.

CAUTION A CAUTION notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

WARNING **A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.**

Safety Symbols

Table 1 Safety Symbol

Symbol	Description
	Direct current
	Alternating current
	Both direct and alternating current
	Three phase alternating current
	Three phase alternating current
	Earth ground terminal
	Protective earth ground terminal
	Frame or chassis ground terminal
	Terminal is at earth potential
	Equipotentiality
N	Neutral conductor on permanently installed equipment
L	Line conductor on permanently installed equipment
	On (mains supply)
	Off (mains supply)
	Standby (mains supply). The instrument is not completely disconnected from the mains supply when the power switch is in the standby position
	In position of a bi-stable push switch

Symbol	Description
	Out position of a bi-stable push switch
	Equipment protected throughout by DOUBLE INSULATION or REINFORCED INSULATION
	Caution, refer to accompanying documentation
	Caution, risk of electric shock
	Do not apply around or remove from HAZARDOUS LIVE conductors
	Application around and removal from HAZARDOUS LIVE conductors is permitted
	Caution, hot surface
	Ionizing radiation
CAT I	IEC Measurement Category I
CAT II	Measurement Category II
CAT III	Measurement Category III
CAT IV	Measurement Category IV

Compliance and Environmental Information

Table 2 Compliance and Environmental Information

Safety Symbol	Description
	CSA is the Canadian certification mark to demonstrate compliance with the Safety requirements.
	The C-tick mark is a registered trademark of the Spectrum Management Agency of Australia. This signifies compliance with the Australia EMC Framework regulations under the terms of the Radio Communication Act of 1992.
	CE compliance marking to the EU Safety and EMC Directives. ISM GRP-1A classification according to the international EMC standard. ICES/NMB-001 compliance marking to the Canadian EMC standard.

DDR/LPDDR Post Process Compliance—At a Glance

The DDR/LPDDR Post Process Compliance Tool evaluates the captured DDR/LPDDR data against a set of user-defined limits to help you validate that a memory system is operating properly. The bus types supported by this tool are:

- DDR1/2/3/4/5

- LPDDR1/2/3/4/4x/5

The automated test application guides you through the process of selecting and configuring tests, running tests, and evaluating the test results.

The application assumes that the Keysight logic analysis system has already been set up to properly capture DDR data.

To use the automated test application, see:

- Chapter 2, "Starting the DDR/LPDDR Post Process Compliance Tool" on page 15
- Chapter 4, "Setting Up the Test Environment" on page 19
- Chapter 3, "Configuring Tests Limits" on page 21
- Chapter 5, "Selecting Tests" on page 39
- Chapter 6, "Running Tests" on page 49
- Chapter 7, "Automating the Tests" on page 53
- Chapter 8, "Viewing Results" on page 57
- Chapter 9"Viewing/Exporting/Printing the Report" on page 61
- Chapter 10 "Saving Test Projects" on page 67
- Chapter 11, "Creating or Opening a Test Project" on page 69

Contents

1 About the Tool

Overview of the tests

There are two types of tests:

- Tests which check for timing violations
- Tests which check for illegal DDR state transitions

The test limits can be (and must be) configured by the user.

The provided timing violation tests include:

Parameter	Description	Test
$tRAS_{max}$	Row Active time ACTIVATE to PRECHARGE/Auto-PRECHARGE	must be < tRASmax
$tRAS_{min}$	Row Active time ACTIVATE to PRECHARGE/Auto-PRECHARGE	must be > tRASmin
tRP	PRECHARGE to any other command (same bank)	must be > tRP
tCCD	Time between any read or write command	must be > tCCD
tRRD	ACTIVATE to ACTIVATE (any bank)	must be >= tRRD
tFAW	Time for four ACTIVATEs (any bank)	must be >= tFAW
tRFC	REFRESH to REFRESH or ACTIVATE	must be > tRFC
tDARW	ACTIVATE to external READ/WRITE	must be > tDARW
tDRP	Read to Precharge/AutoPrecharge	must be > tDRP
tDRW	Read to Write	must be > tDRW
tDWP	Write to Precharge/AutoPrecharge	must be > tDWP
tDWR	Write to Read	must be > tDWR

Description
READ or WRITE to an inactive row
REFRESH to an active bank
ACTIVATE to an active bank

Compatibility

The DDR/LPDDR Post Process Compliance Tool works for most DDR, DDR2, DDR3, DDR4, DDR5, LPDDR, LPDDR2, LPDDR3, LPDDR4, LPDDR4x, and LPDDR5 systems.

The tool is not able to fully model systems which use the following optional DDR features:

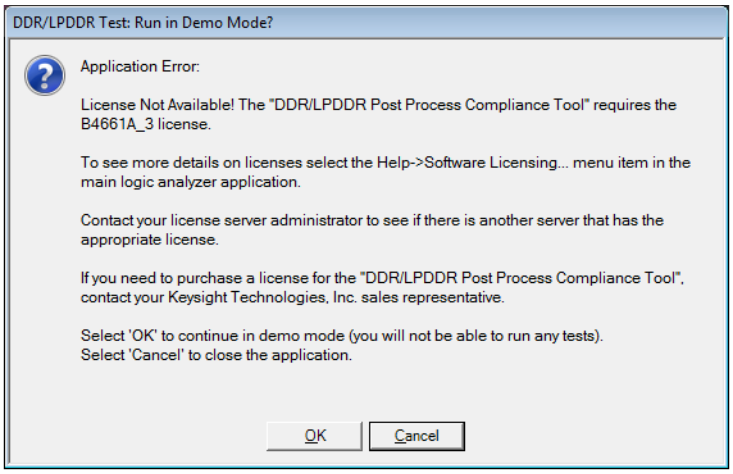
- Partial Array Self-Refresh (PASR)
- Auto Self-Refresh (ASR)
- On-the-fly Burst Length switching

About the software

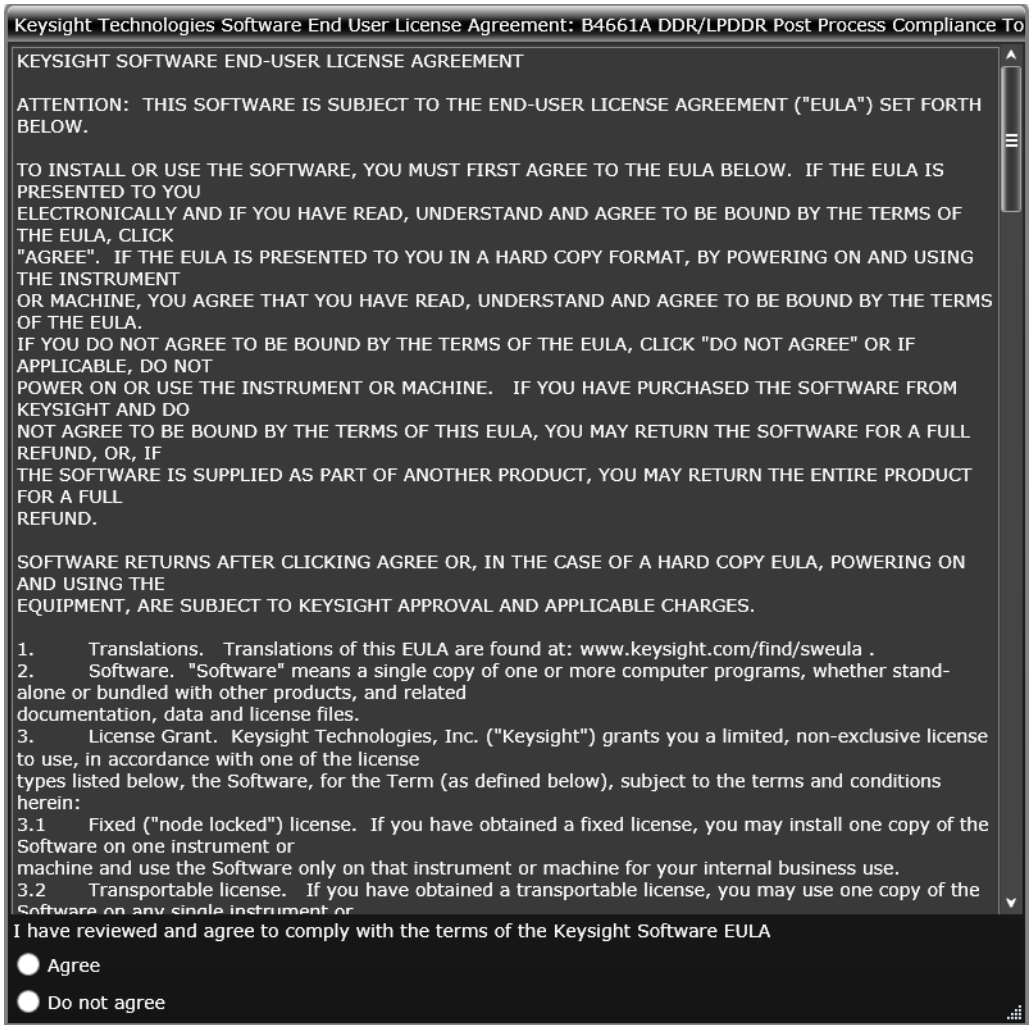
The Post Process Compliance Tool is part of the Keysight B4661A DDR/LPDDR Toolset package. This tool requires that you install the Logic and Protocol Analyzer software version 6.2 or higher. Versions prior to 6.2 do not support this tool.

Software License

The DDR/LPDDR Post Process Compliance Tool requires B4661A_3 license to operate. If this license is not installed in your system, the following license error dialog box is displayed while launching the DDR/LPDDR Post Process Compliance Tool application.

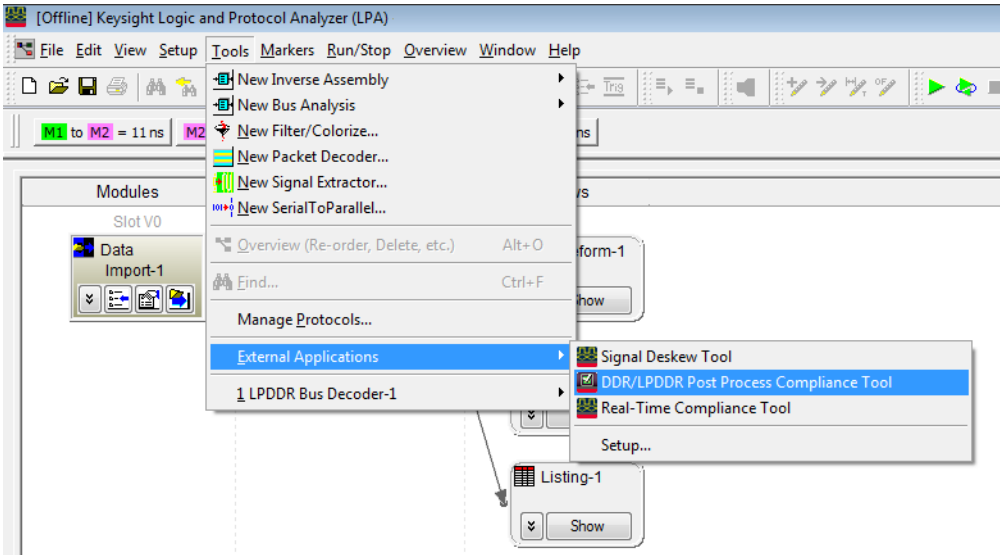


When you are launching the DDR/LPDDR Post Process Compliance Tool for the first time, the Keysight Technologies Software End User License Agreement dialog box appears. You can read the agreement and choose to agree or disagree before proceeding further to use the DDR/LPDDR Post Process Compliance Tool.

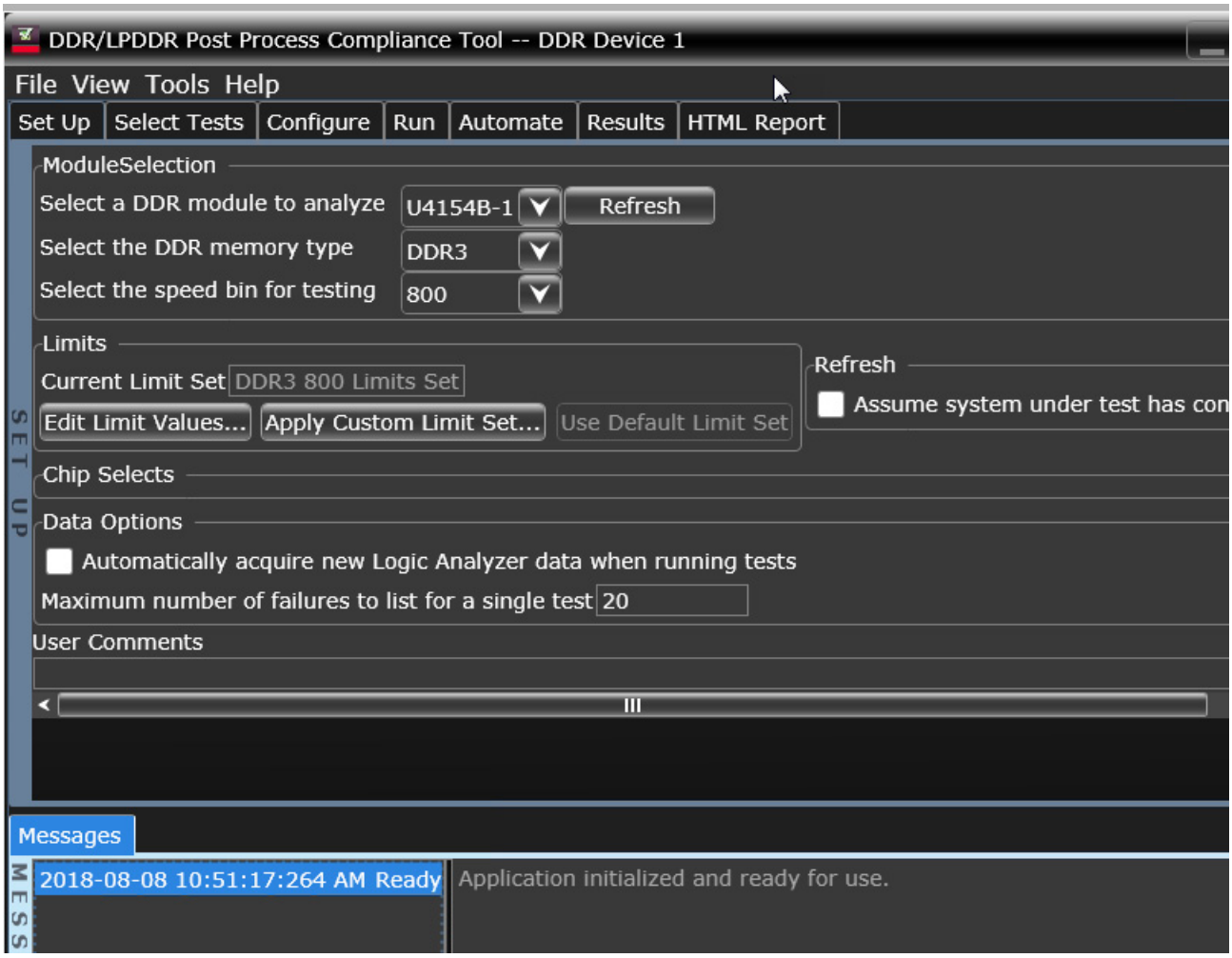


2 Starting the DDR/LPDDR Post Process Compliance Tool

1 From the logic analysis system's main menu, choose **Tools > External Applications > DDR/LPDDR Post Process Compliance Tool**.



The DDR/LPDDR Post Process Compliance Tool window appears.

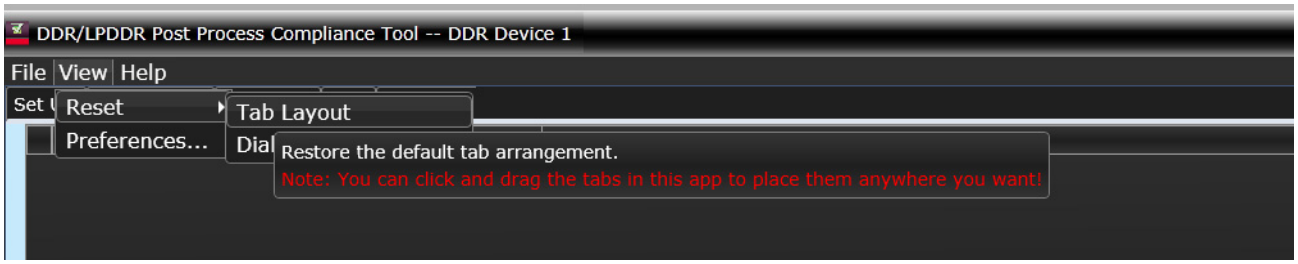


See Also · "To Toggle between the Toolbar" on page 17

Next · "Creating or Opening a Test Project" on page 69

To Toggle between the Toolbar

To toggle between the toolbars, you can click and drag the toolbars accordingly. To keep the default display for the toolbars, select **View>Preferences>Tab Layout** from the menu.



3 Setting Up the Test Environment

1 Click the **Set Up** tab.

2 If more than one DDR bus decoder exists in the logic analysis system setup, select which one to use for the compliance tests from the **Select a DDR module to analyze** listbox.

If only one decoder exists, it will be selected automatically.

If needed, click **Refresh** to update the list. You may need to refresh the list and select a new decoder if you load a new logic analyzer configuration file, or whenever you add or remove a decoder.

3 Select the DDR memory type. The DDR/LPDDR Post Process Compliance Tool can work with any of the following memory bus standards.

- DDR1/2/3 /4/5
- LPDDR1/2/3/4/4x/5

4 Use the options available in the **Limits** section to edit or automatically set the values of the limits associated to the compliance tests. The Post Process Compliance tool will then use these new values to perform compliance testing and to arrive at pass/fail and/or margin information for each test. Refer to the chapter "Configuring Tests Limits" on page 21 to know about these options in detail.

5 From the **Chip Selects** section, select the checkboxes for the chip selects that are being used for the SDRAM. For the post process compliance testing to be correct, make sure that the chip selects that are being used in the system must be enabled and unused chip selects must not be enabled.

If you select **DDR4** or **DDR5** from the **Memory Type** listbox, the **DDR4 Rank Selection Mode** listbox is also displayed in the **Chip Selects** section. You use this listbox to select the appropriate rank addressing mode option based on the rank addressing being used for your DDR4/DDR5 RDIMM device.

In the Standard DDR4/DDR5 rank addressing, there is one CS# (chip select) line for each rank.

In the 3DS rank addressing, there is only one CS# line for all the ranks. Therefore, the logical value of the C (Chip ID) bits is used to identify the rank being addressed in the decode. The number of Chip ID bits to be used for rank identification is as per the 3DS specifications.

From the available 3DS rank addressing options (2-high, 4-high, or 8-high), select the appropriate option based on whether your 3DS device has two, four, or eight logical ranks.

Based on the rank addressing mode that you select, the appropriate number of chip selects are displayed and enabled in the **Chip Selects** section. For instance, if you select the Quad CS rank addressing mode, four chip selects are displayed by default.

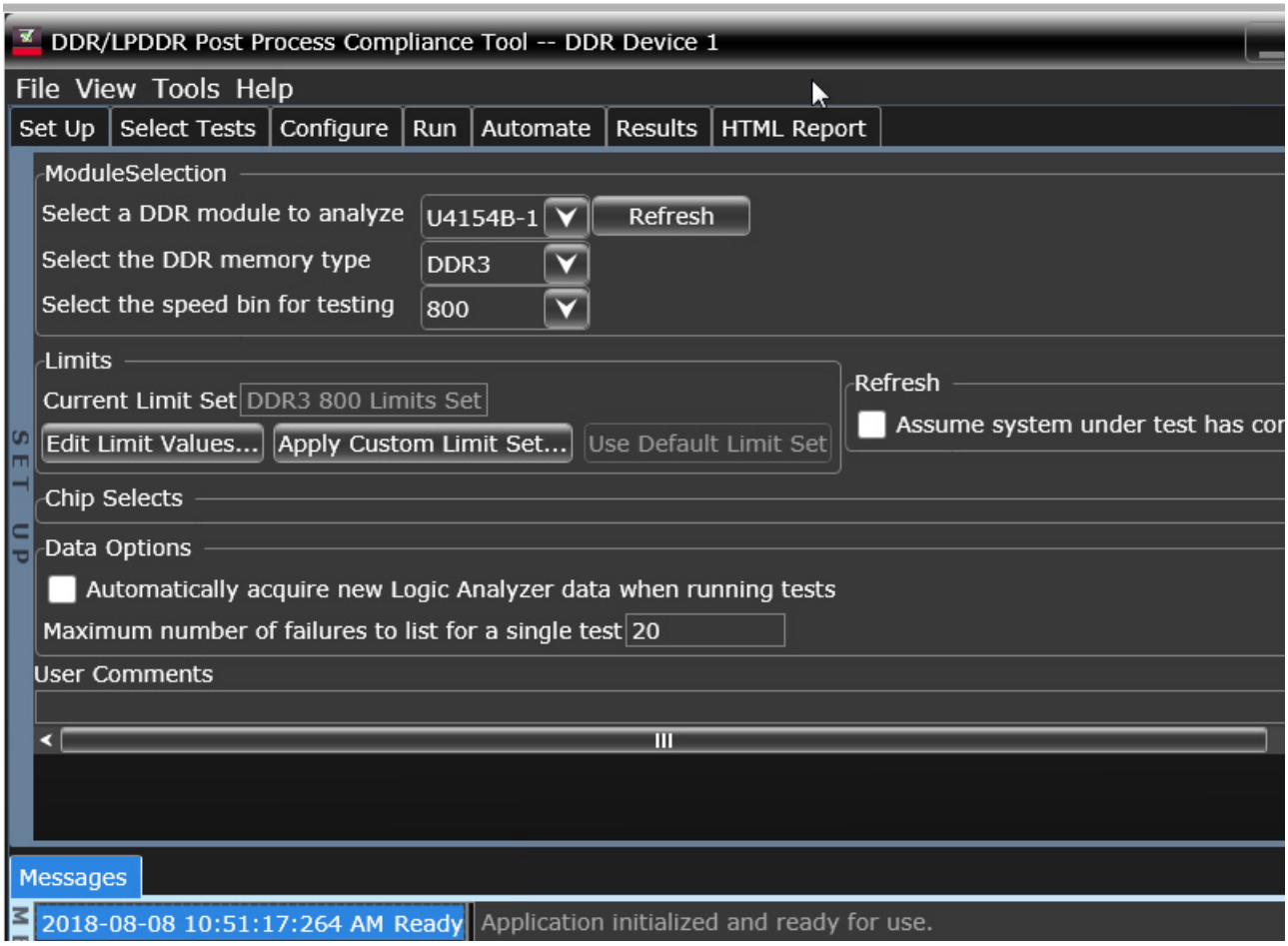
The tests displayed in the **Select Tests** tab vary based on the rank addressing mode that you select in this section. For instance, the tests for same or different logical ranks are displayed if you select one of the 3DS rank addressing mode.

6 From the **Data Options** section, select whether or not you want the tool to automatically acquire new data when compliance tests are run. Whether you plan to run tests once or multiple times, the selection of this checkbox instructs the tool to first run the logic analyzer for data acquisition. When the data acquisition run is complete, the tool starts post processing the newly acquired data by running the selected tests. If you plan to run the tests multiple times or forever, then you

must select this checkbox to ensure that the tool runs the logic analyzer repetitively for data acquisition and then acquires the new data automatically for post processing.

Deselecting this checkbox instructs the tool to use the already acquired data for post processing. The tool does not run the logic analyzer for data acquisition in this case. Therefore, when you deselect this checkbox, you can run the tests only once on existing data.

7 (optional) Describe the test for future reference. The specified **User Comments** will appear on the HTML report which is generated for the test.



Next · "Selecting Tests" on page 39

4 Configuring Tests Limits

While setting up the test environment, you must ensure that the tests limits are as per your specific requirements such as bus speed and bus type. You can do this using various options available in the **Limits** section in the **Set Up** tab.

Each compliance test has a specification parameter (limit) associated with it. The default value of each specification parameter is already set in the Post Process Compliance tool. If required, you can override this default value and set a new value suitable to your specific requirements such as the memory part you are using and certain characteristics of the memory bus. The Post Process Compliance tool will then use these new values to perform compliance testing and to arrive at pass/fail and/or margin information for each test.

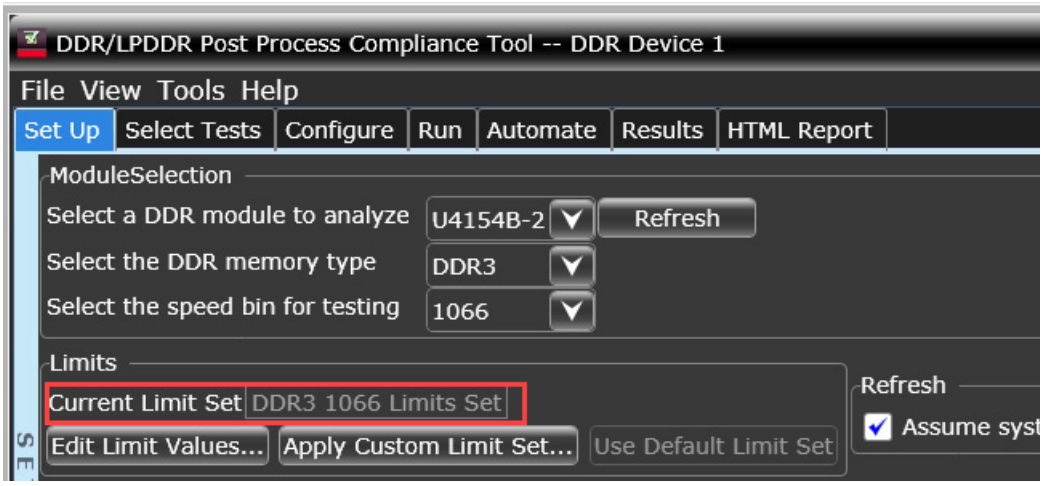
You can set the tests limits in the following ways:

Method	Available for...
Use the default limit set and then manually override the default value of individual test limit(s). See "Using the Default Limit Set and Manually Overriding the Default Value of a Test Limit" on page 22.	All test groups
Use a custom limit set (.lim) file to change the value of test limits in a test group to the values appropriate for a particular bus speed. A number of predefined limit files are installed with the Post Process Compliance tool for the most common bus speeds for all DDR bus types. These files are installed at: *C:\Program Files\Keysight Technologies\Logic Analyzer\ExternalApps\DDRApps\DDRComplianceTool\app\limits* Applying a custom limit file quickly changes all limit values to match the values applicable for a particular bus speed. See "Using a Custom Limits File" on page 24.	All test groups
Set tests limits automatically based on the specific characteristics that you specified for your system. See "Setting Tests Limits Automatically as per your System's Characteristics" on page 25.	DDR4, DDR5, and LPDDR5 test groups
Customize tests limits automatically as per the set of bus settings that you specified for each clock speed. See "Customizing the Compliance Setup to Handle Multiple System Clock Speeds" on page 30.	LPDDR5 test group

These methods are described in this chapter.

Using the Default Limit Set and Manually Overriding the Default Value of a Test Limit

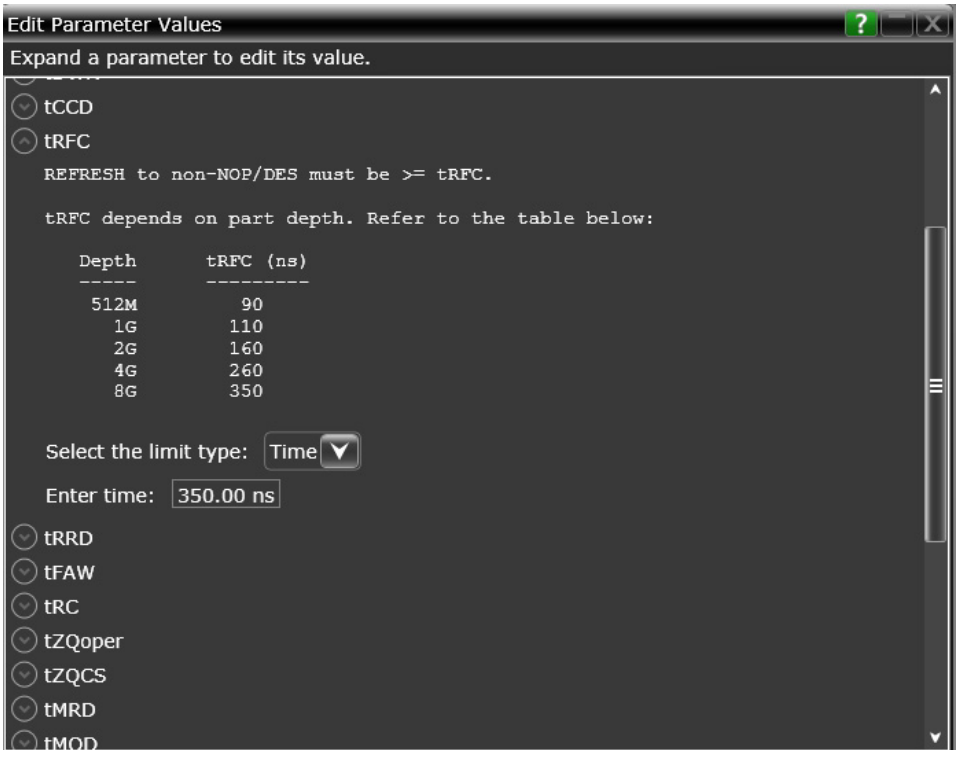
When you select the logic analyzer module and DDR memory type in the Set Up tab, the default limit set applicable to these selections is automatically loaded and displayed as the **Current Limit Set** in the **Limits** section.



If you want to change the value of a test limit from this default limit set, perform the following steps:

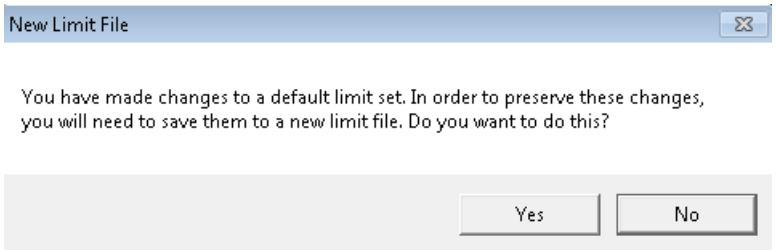
1 In the **Set Up** tab, click **Edit Limit Values....**.

2 The **Edit Parameter Values** dialog box is displayed with the list of all test limits applicable for the test group. Click the down-arrow button displayed with a test limit to view its current value, get more information about it, and view options to modify its value.



3 Click **OK** when you have completed making changes to test limits.

4 To preserve and use these changed tests limits, you need to save these values in a new limit set. This also ensures that the default limit set remains intact with the default values. To save, click **Yes** in the displayed message box and then specify the path and name for a new limits file.

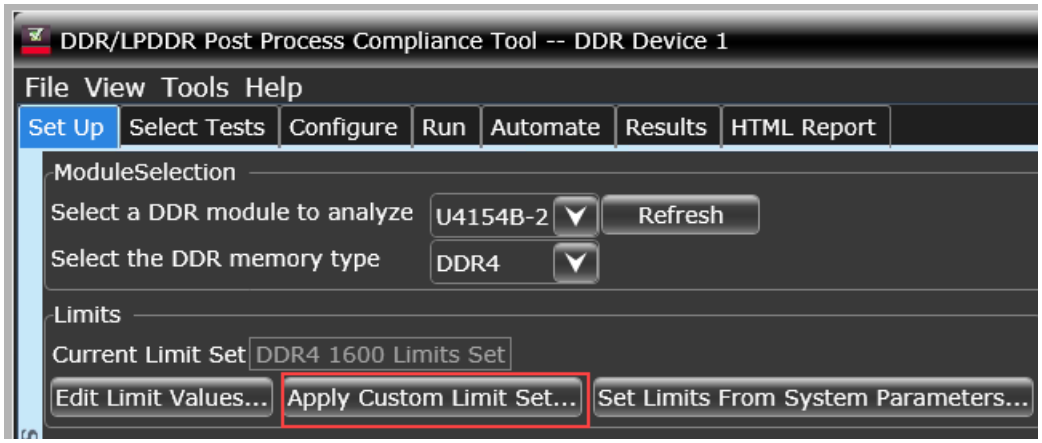


NOTE At any time, you can revert back to the default tests limits by clicking the **Use Default Limit Set** button in the **Limits** section.

See Also "To set the test limits (for information on how to calculate the limits)" on page 36 (for information on how to calculate the limits)

Using a Custom Limits File

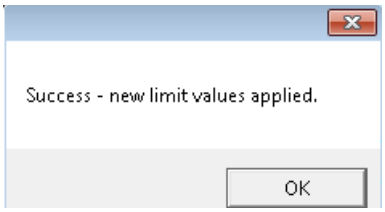
1 Click the **Apply Custom Limit Set...** button displayed in the **Limits** section of the **Set Up** tab.



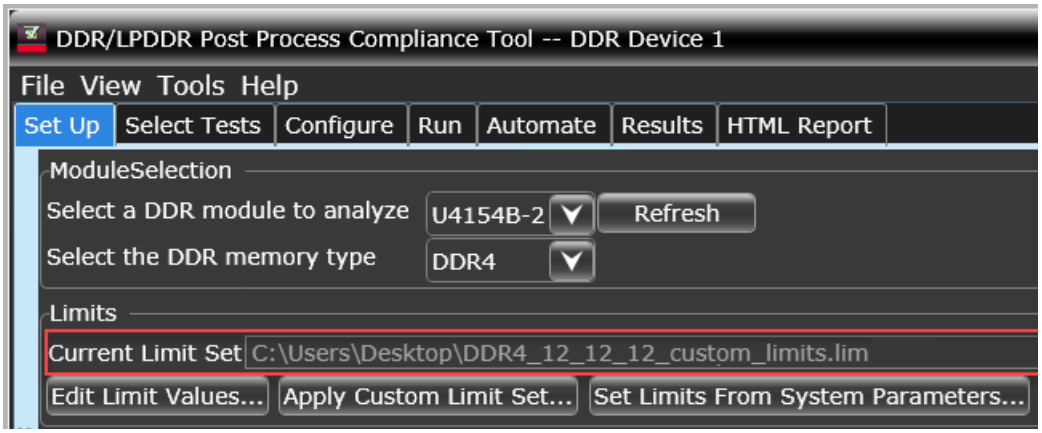
The **Open** dialog box is displayed.

2 Select the customized limits (.lim) file that you want to use and click **Open**.

3 Click **OK** to acknowledge the success message.

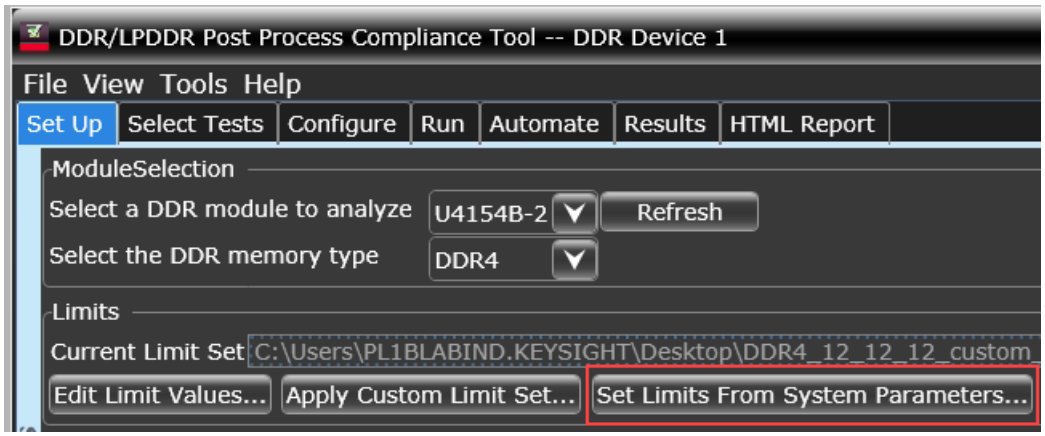


The custom limits file is then displayed as the **Current Limit Set.** All the tests limits are automatically changed to match the values in the custom limits file.



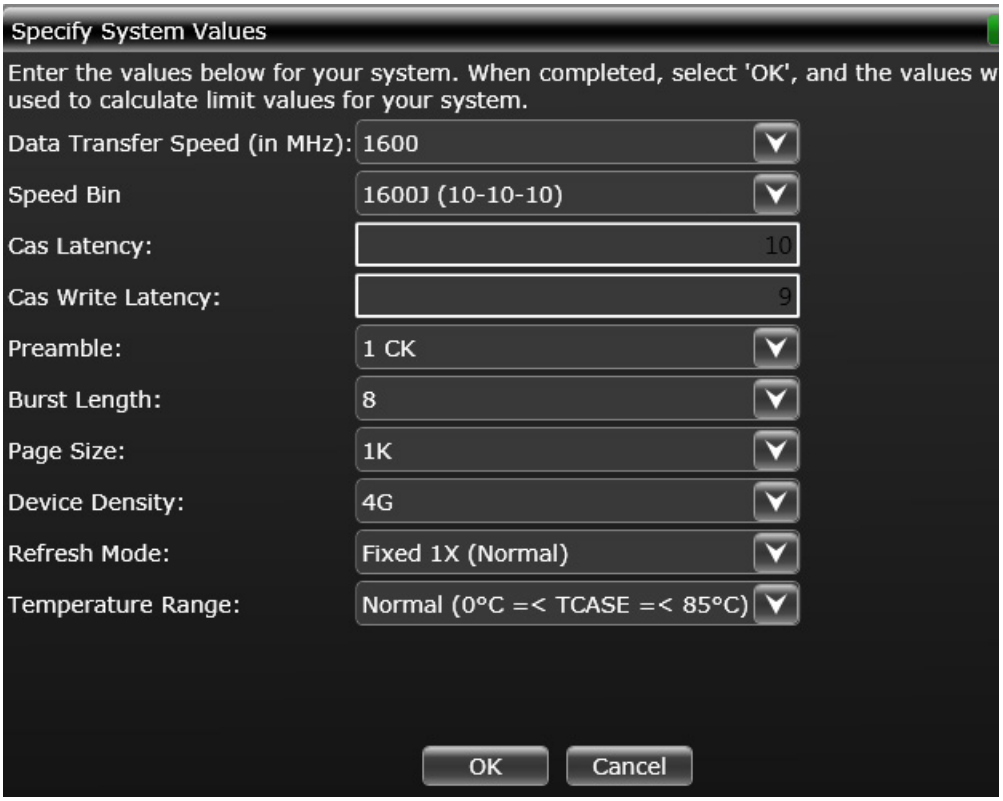
Setting Tests Limits Automatically as per your System's Characteristics

1 Click the **Set Limits From System Parameters...** button displayed in the **Limits** section of the **Set Up** tab.



NOTE The **Set Limits From System Parameters...** button is displayed only for a DDR4, DDR5, or LPDDR5 memory type.

The **Specify System Values** dialog box is displayed.



2 Specify the values matching your system's characteristics and then click **OK**.

All the tests limits are then automatically modified as per the system values that you specified in the Specify System Values dialog box.

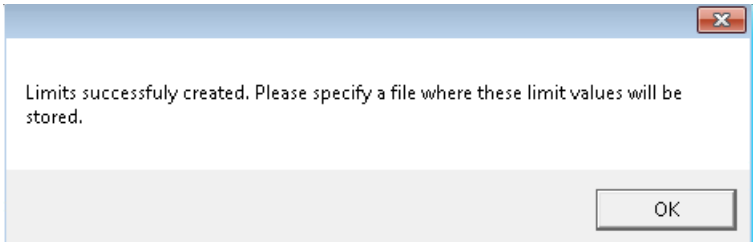
NOTE

For an LPDDR5 bus, you can select whether the bus runs on a single clock speed or at multiple clock speeds in the Specify System Values dialog box.

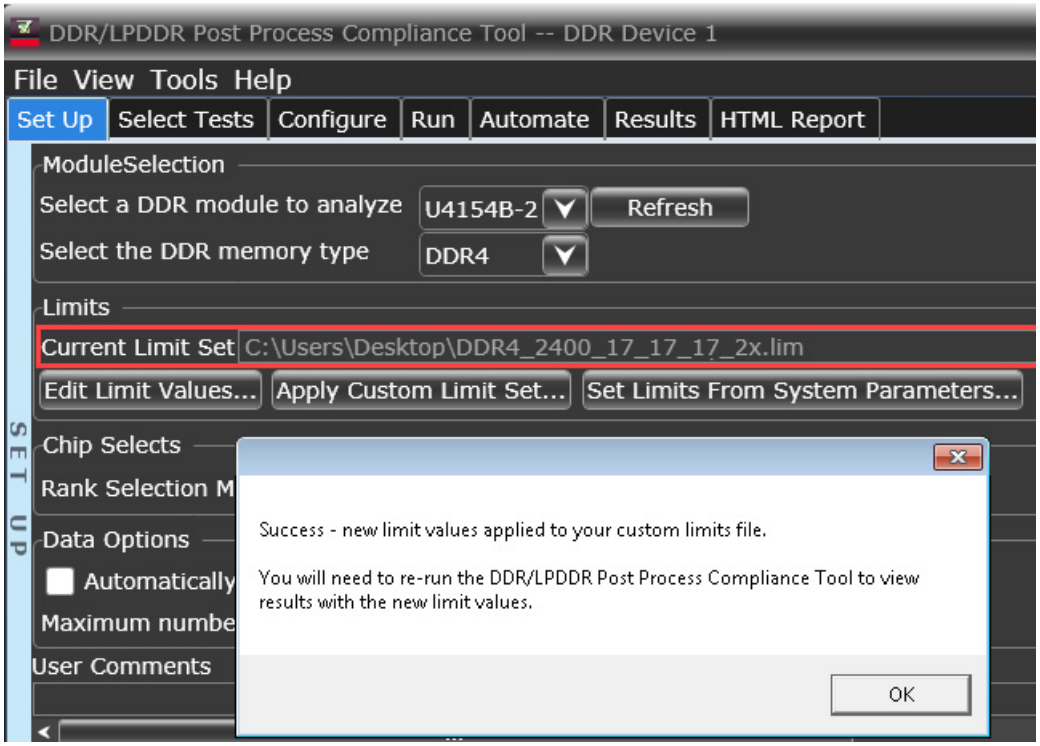
For the multiple clock speeds scenario, you need to specify the relevant bus settings at each possible clock speed for your DUT. This allows the Post Process Compliance tool to automatically calculate correct test limits from the changing bus settings when the system clock speed changes. As a result, the tool can generate the compliance results accurately for systems running at multiple clock speeds.

Refer to the topic "Customizing the Compliance Setup to Handle Multiple System Clock Speeds" on page 30 to know more.

3 To allow the tool to use these changed limits, save these changed limits in a limits (.lim) file by clicking **OK** on the displayed message box and proceeding with saving the limits file.



4 The saved limits file is then displayed as the **Current Limit Set**. Click **OK** to acknowledge the success message.



You can view the changed tests limits in the Edit Parameters Values dialog which can be accessed by clicking the Edit Limit Values button.

NOTE

A test limit value may at times differ slightly from the specifications. This is because the limit value is truncated to a number evenly divisible by 80ps to match the logic analyzer time tagger that works in 80ps ticks. In the example given below, the value of the tRCD limit is set to 12.48ns instead of the 12.5ns in the specifications, because 12.485ns is evenly divisible by 80ps.

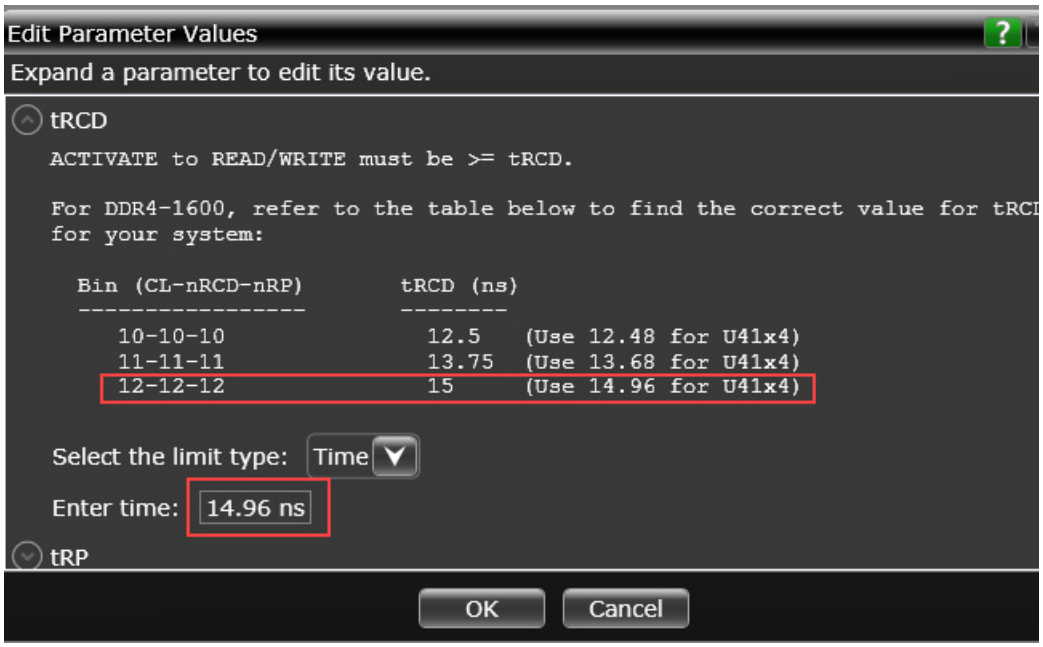
Example of setting tests limits automatically based on system characteristics

The following is an example of how the **tRCD** limit value is changed automatically based on the user-specified system characteristics.

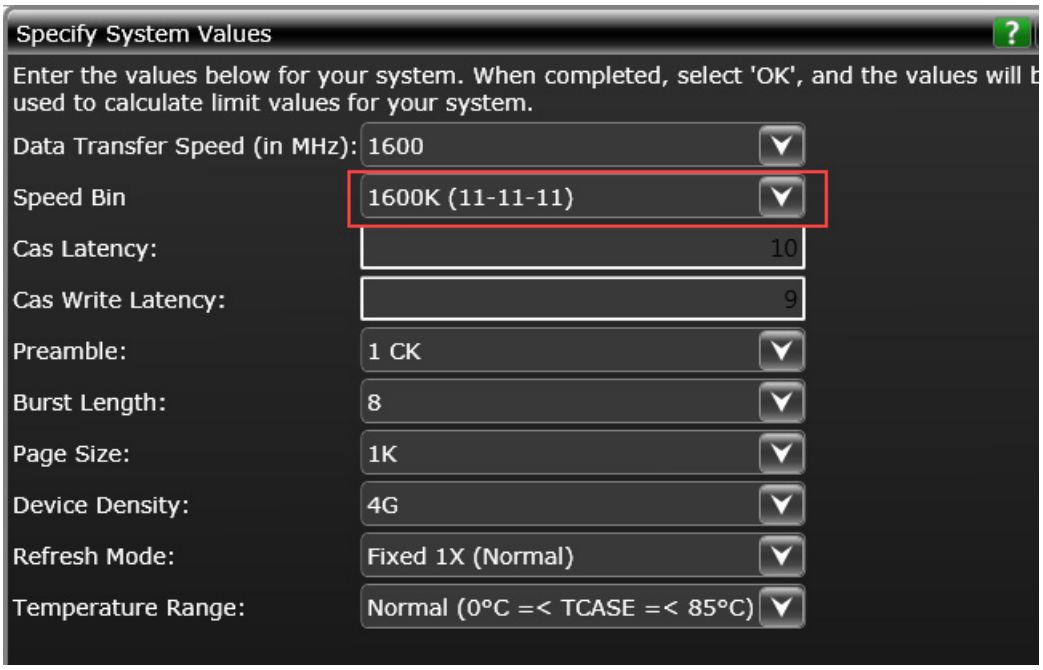
In screen 1, the default value of the tRCD parameter is set to **14.96 ns** (1600L 12-12-12 speed bin).

In screen 2, the Speed Bin system value is changed to **1600K 11-11-11** to match the system characteristics.

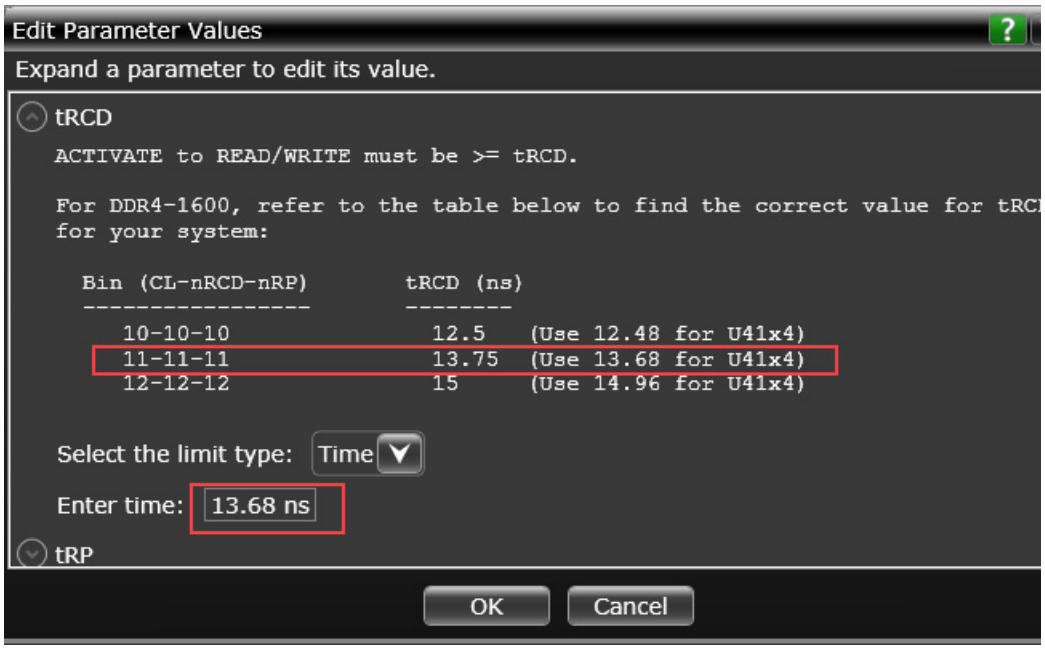
In screen 3, the value of the tRCD parameter is automatically changed to **13.68 ns** (1600K 11-11-11 speed bin) to match the changed Speed Bin system characteristic.



Screen 1 showing the default value of the tRCD parameter



Screen 2 showing the Speed Bin system value changed to 11-11-11



Screen 3 showing the changed tRCD limit value to match the changed speed bin system value

See Also

- "To set the test limits (for information on how to calculate the limits)" on page 36 (for information on how to calculate the limits)

Customizing the Compliance Setup to Handle Multiple System Clock Speeds

The Post Process Compliance tool can perform compliance testing for systems running at:

- a single (fixed) clock speed.
- multiple clock speeds.

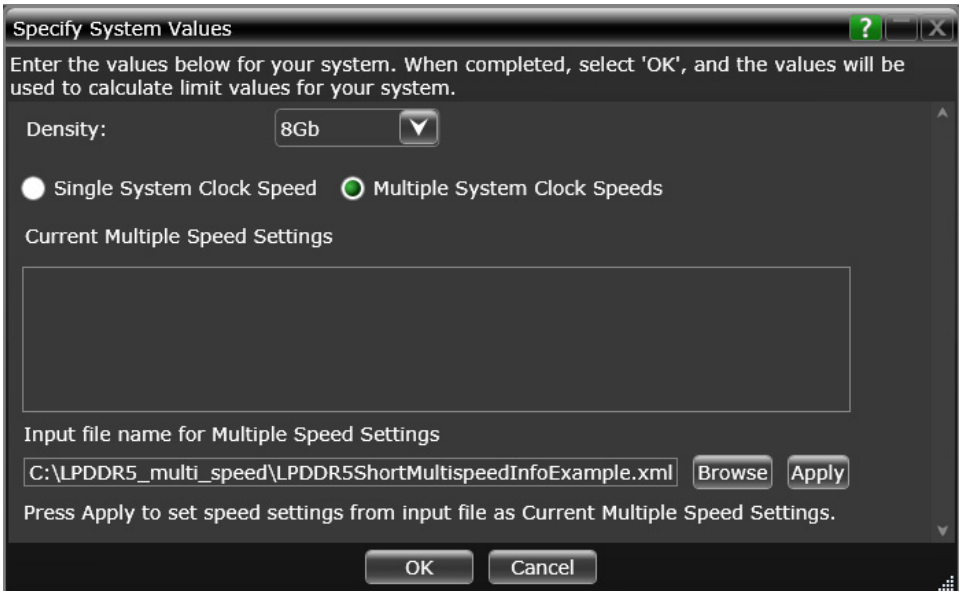
You can customize the compliance setup in the Post Process Compliance tool to indicate whether your LPPDDR5 bus is running at a single clock speed or at multiple clock speeds. This topic describes how to configure the setup to handle multiple clock speeds.

Overview of Multiple Clock Speeds Support

For an LPDDR5 bus running at multiple clock speeds, the change in the system clock speed results in the change in the LPDDR5 bus setting(s). These bus settings usually impact the test limit(s) that the Post Process Compliance tool uses to arrive at pass/fail/margin information for each test. To ensure that the tool calculates correct test limits and generates accurate compliance results for systems changing clock speeds, you need to provide a set of bus settings applicable for each possible clock speed for your DUT. You specify these multiple sets of bus settings in an XML input file described later in this chapter. The format for this file should be as per the format provided in the topic "LPDDR5 Multiple Clock Speeds - XML File Structure and Elements" on page 33. You may also refer to an example of this XML file included in this topic.

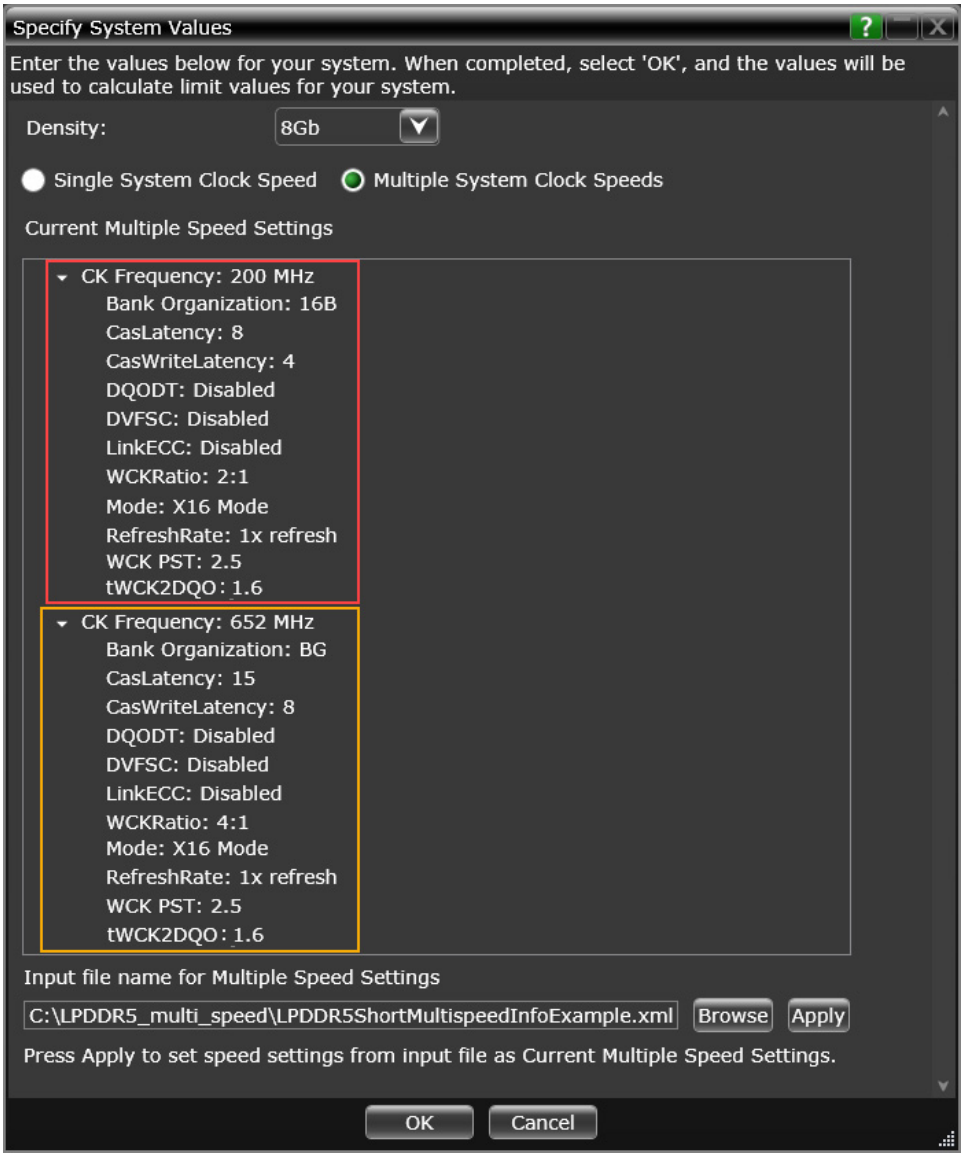
To Customize the Setup for Multiple Clock Speeds

1. Select **LPDDR5** from the **Select the DDR Memory Type** listbox in the **Set Up** tab.
2. Click the **Set Limits From System Parameters...** button displayed in the **Limits** section of the **Set Up** tab. The **Specify System Values** dialog box is displayed.
3. Select the **Density** of your system.
4. Select the **Multiple System Clock Speeds** radio button.
5. On selecting this radio button, the **Input file name for Multiple Speed Settings** field is displayed. Click the **Browse** button displayed with this field to browse and select the XML input file in which you have defined the bus settings for each possible clock speed of your DUT.



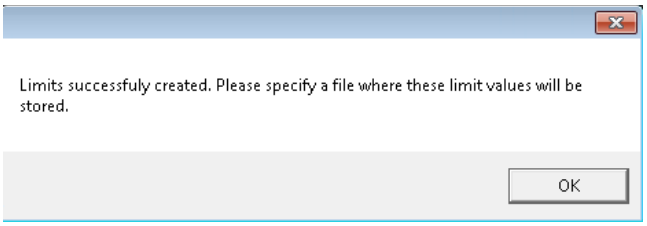
6 Click **Apply** to load the system values from the newly selected XML input file.

On clicking Apply, the bus settings for each possible clock speed of your DUT included in the XML input file are loaded from this file and displayed in the Current Multiple Speed Settings section. An example of these settings loaded from the XML input file is shown below.

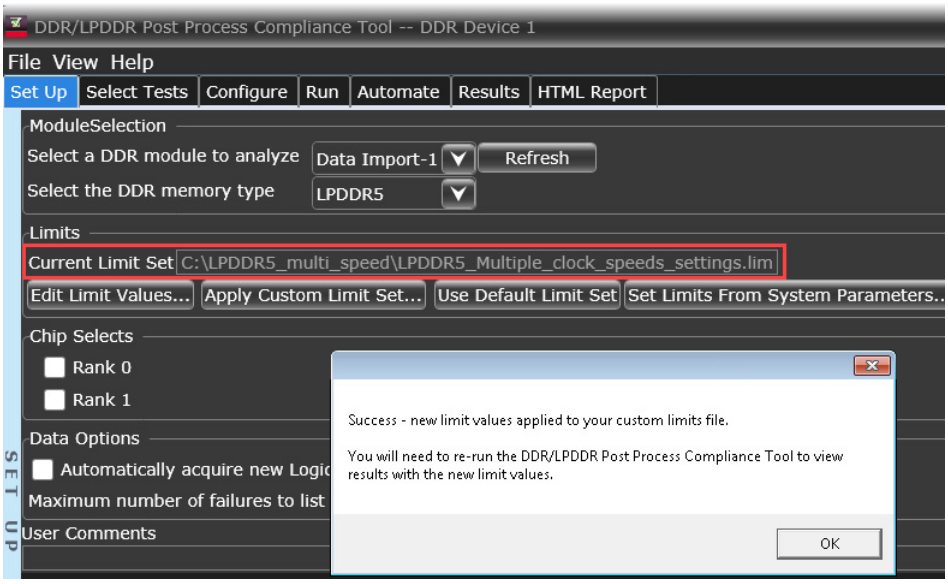


7 Click **OK** to confirm the selections and close the **Specify System Values** dialog box.

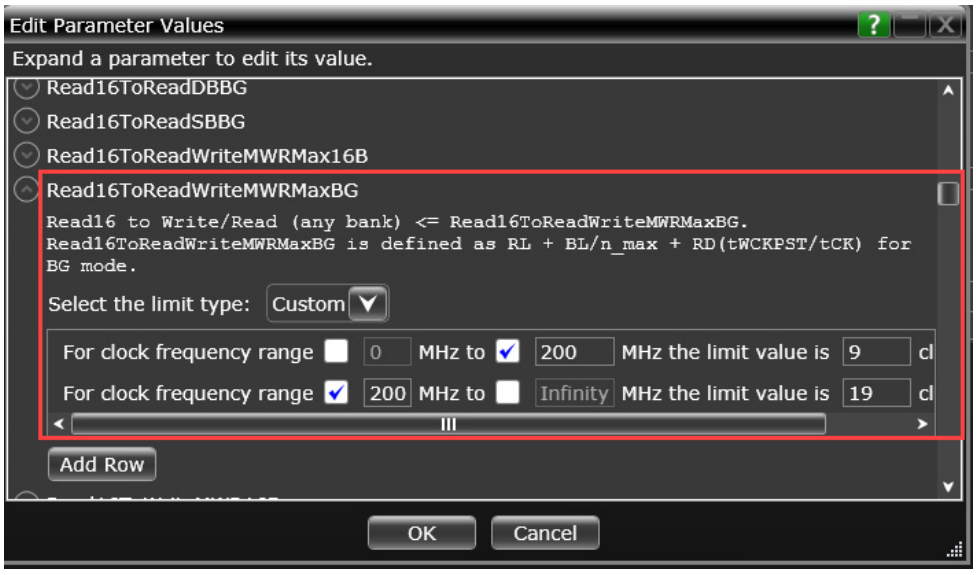
8 The Post Process Compliance tool uses these bus settings to create test limits and displays the following message indicating the successful creation of test limits for different clock speeds. Click **OK** to proceed with saving these newly created test limits in a limits (.lim) file.



9 The saved limits file is then displayed as the **Current Limit Set**. Click **OK** to acknowledge the following success message.



10 If you want to view the new test limit values created for multiple clock speeds, click the E**dit Limit Values...** button.



11 Finally, re-run the tests with the new limit values so that test limits as per the changing system clock speeds are used to arrive at test results.

When the clock speed change is encountered, the Post Process Compliance tool automatically uses the test limits created for that clock speed in the limits file and computes compliance results using these settings.

LPDDR5 Multiple Clock Speeds - XML File Structure and Elements

You can create/edit this XML file using any text editor. This topic describes the format and hierarchy of the XML elements to be followed for this XML file.

XML Elements Hierarchy

The XML elements shown below are for a set of bus settings to be used for a particular clock speed. Depending on the clock speeds possible for your DUT, you can replicate this set with different settings in the XML file.

```
<SystemClockSpeeds>
    <SystemClockSpeed>
        <BankOrganization/>
        <CasLatency/>
        <CasWriteLatency/>
        <DQODT/>
        <DVFSC/>
        <LinkECC/>
        <WCKRatio/>
        <Mode/>
        <RefreshRate/>
        <WCKPST/>
        <RDQSPST/>
        <tWCK2DQO/>
        <WCKFreeRunningMode/>
```

XML Elements Description

These XML elements are described in the table below.

XML Element	Description	Attributes
<SystemClockSpeeds>	The multiple clock speeds settings XML file begins with the <SystemClockSpeeds> element. This element allows you to define one or more sets of bus settings for system's clock speeds.	-
<SystemClockSpeed>	Contains the set of following bus settings to be applied for the clock speed that you specified in the *Value* attribute. ▪ <BankOrganization> - Possible values are 8B, 16B, BG ▪ <CasLatency> ▪ <CasWriteLatency> ▪ <DQODT> - Possible values are Disabled or Enabled. ▪ <DVFSC> - Possible values are Disabled or Enabled. ▪ <LinkECC> - Possible values are Disabled or Enabled. ▪ <WCKRatio> - Possible values are 2:1, 4:1. ▪ <Density> - Possible values are 2Gb, 3Gb, 4Gb, 6Gb, 8Gb, 12Gb, 16Gb, 24Gb, 32Gb. ▪ <Mode> - Possible values are X8 Mode, X16 Mode. ▪ <RefreshRate> - Possible values are Ref8x, Ref6x, Ref4x, Ref3_3x, Ref2_5x, Ref2_0x, Ref1_7x, Ref1_3x, Ref1x, Ref0_75x, Ref0_5x, Ref0_25x, Ref0_25xD, Ref0_125x, Ref0_125xD. ▪ <WCKPST> - Possible values are 2.5, 4.5, 6.5. ▪ <RDQSPST> - Possible values are 0.5, 2.5, 4.5. ▪ <tWCK2DQO> - Maximum value of tWCK2DQO in ns. ▪ <WCKFreeRunningMode> - Possible values are Disabled or Enabled.	***Value -*** *A String representing the clock speed for which the set of bus settings is applicable.* Example <SystemClockSpeed Value="200">

XML File Example

This topic includes an example of the XML input file created in the required format to decode as per the multiple clock speeds of the DUT.

```
<SystemClockSpeeds>
  <SystemClockSpeed Value="200">
      <!-- 8B, 16B, BG -->
      <BankOrganization>16B</BankOrganization>
      <CasLatency>8</CasLatency>
      <CasWriteLatency>4</CasWriteLatency>
      <!-- Disabled, Enabled -->
      <DQODT>Disabled</DQODT>
      <!-- Disabled, Enabled -->
      <DVFSC>Disabled</DVFSC>
      <!-- Disabled, Enabled -->
      <LinkECC>Disabled</LinkECC>
      <!-- 2:1, 4:1 -->
      <WCKRatio>2:1</WCKRatio>
      <!--X8 Mode, X16 Mode -->
      <Mode>X16 Mode</Mode>
      <!-- Ref8x, Ref6x, Ref4x, Ref3_3x, Ref2_5x, Ref2_0x,
      Ref1_7x, Ref1_3x, Ref1x, Ref0_75x, Ref0_5x, Ref0_25x,
      Ref0_25xD, Ref0_125x, Ref0_125xD -->
```

```
        <RefreshRate>Ref1x</RefreshRate>
        <!-- 2.5, 4.5, 6.5 -->
        <WCKPST>2.5</WCKPST>
        <!-- 0.5, 2.5, 4.5 -->
        <RDQSPST>0.5</RDQSPST>
        <!-- tWCK2DQO max value in ns -->
        <tWCK2DQO>1.6 </tWCK2DQO>
        <!-- Disabled, Enabled -->
        <WCKFreeRunningMode>Disabled</WCKFreeRunningMode>
    </SystemClockSpeed>
    <SystemClockSpeed Value="652">
        <BankOrganization>BG</BankOrganization>
        <CasLatency>15</CasLatency>
        <CasWriteLatency>8</CasWriteLatency>
        <DQODT>Disabled</DQODT>
        <DVFSC>Disabled</DVFSC>
        <LinkECC>Disabled</LinkECC>
        <WCKRatio>4:1</WCKRatio>
        <Mode>X16 Mode</Mode>
        <RefreshRate>Ref1x</RefreshRate>
        <WCKPST>2.5</WCKPST>
        <RDQSPST>0.5</RDQSPST>
        <tWCK2DQO>1.6</tWCK2DQO>
        <WCKFreeRunningMode>Disabled</WCKFreeRunningMode>
    </SystemClockSpeed>
</SystemClockSpeeds>
```

To set the test limits (for information on how to calculate the limits)

All timing violation tests are based on compliance limits that are specified by the user. Specify these limits based on the specific DDR memory parts you are using. Limits will vary depending on:

- Memory technology (DDR2, DDR3)
- Speed grade
- Clock speed
- Part density
- User selected options such as Additive Latency and burst length

Units

Some times must be entered in seconds (s). If the data sheet expresses these limits in terms of clock cycles, you will need to convert those limits to seconds.

Each logic analyzer sample has a timestamp. Results will be calculated by subtracting the time stamp of the first event from the timestamp of the second event. Note that the time stamps are only as good as the time stamp resolution of the logic analyzer card being used (this resolution may be as coarse as 2ns; see the Specifications and Characteristics in the logic analyzer's Online help for details). The elapsed time includes time during which the DDR clock is inactive.

Other times must be entered as a number of clock cycles (CK). Results will be calculated by counting the number of logic analyzer samples between the two events.

Additive latency (AL) is normally expressed as a number of clocks (CK). For some calculations, you will need to convert AL to seconds (s) by dividing by the clock rate.

Burst length (BL) is simply an integer (4 or 8).

Definitions of the limits

You will need to look up some of the limits from the part data sheet. You will then calculate values for the derived limits.

Keysight suggests using the formulas here to compute the derived limits. However, it is entirely the responsibility of the user to choose limits that are appropriate for the intended application.

Here are the limits you need to specify:

Parameter	Description	Unit	Suggested Definition	Reference
$tRAS_{max}$	Row Active time ACTIVE to PRECHARGE	s	Part dependent (9 * tREFI)	Data Sheet (tREFI). See DDR3 page 147.
$tRAS_{min}$	Row Active time ACTIVE to PRECHARGE	s	Part dependent	Data Sheet
tDARW	Min ACT to external READ/WRITE	s	tRCD-AL	DDR2)3.5 / DDR3 12.3
tRP	Row Precharge time min PRECHARGE to any other command (same bank)	s	Part dependent	Data Sheet
tDRP	Min Read to Precharge	CK	DDR2: AL + BL/2 + max (tRTP, 2CK) -2CK DDR3: AL + tRTP	DDR2 3.7.1 / DDR3 4.13.3
tDRW	Min Read to Write	CK	DDR2: BL/2 + 2CK DDR3: BL4: RL + CCD/2 + 2CK – WL DDR3: BL8: RL + CCD + 2CK - WL	DDR2 figure 35 / DDR3 figure 35, 36
tRFC	REFRESH command time. min time REFRESH to REFRESH or ACTIVATE	s	Part dependent	Data Sheet
tDWP	Min Write to Precharge	CK	WL + BL/2 + tWR	DDR2 (3.7.2 / DDR3 Figure 49, 50

Parameter	Description	Unit	Suggested Definition	Reference
tDWR	Min Write to Read	CK	DDR2: CL -1 + BL/2 + tWTR DDR3: WL + BL/2 + tWTR	DDR2 Figure 41 / DDR3 Figure 53, 56
tCCD	CAS to CAS delay min time between any read or write command	CK	Part dependent	Data Sheet
tRRD	Min time between two ACTIVATE commans (different banks)	s	Part dependent	Data Sheet
tFAW	Min time for four ACTIVATE commands (different banks)	s	Part dependent	Data Sheet

Values used to calculate the limits

To calculate the limits, you will need to look up or calculate the following values:

Parameter	Description	Unit	Suggested Definition	Reference
AL	Additive Latency	CK, s	User selection	System Design
BL	Burst Length		User selection	System Design
CL	CAS (Read) Latency	CK	Part dependent	Data Sheet
CWL	CAS Write Latency	CK	Part dependent	Data Sheet
RL	Read Latency	CK	AL + CL	DDR3 (see) 3.4.3.4
WL	Write latency	CK	AL + CWL	DDR3 (see) 3.4.3.4
tRCD	RAS to CAS Delay (ACT to internal R/W)	s	Part dependent	Data Sheet
tREFI	Refresh Interval; average time between Refresh commands	s	Part dependent	Data Sheet
tRTP	Internal Read to Precharge	s	Part dependent (max 4CK or 7.5ns)	Data Sheet
tWR	Internal Write Recovery	s	Part dependent	Data Sheet
tWTR	Internal Write to internal Read	s	Part dependent (max 4CK or 7.5ns)	Data Sheet

External Read/Write + AL = Internal Read/Write

Naming conventions

Limits which are normally expressed as maximum or minimum times have names beginning with 't'.

The names of derived timing limits begin with 'tD'. Derived limits are not usually specified directly in the part data sheet. In general, you will compute these from the standard timing parameters.

Limits which are normally expressed as a number of clock cycles have no prefix. In some cases, you may need to convert these to seconds for use by the tool.

Customizing the limits

The definitions are suggestions based on the DDR standards. There is no requirement that the user must set the limits to those specified in the data sheet or in the JEDEC standard. You can set the limits however you like, depending on the goals of your testing.

To load and view the limits, you can either use the default limit set or use customized limit sets. If you are using customized limit sets, you can select the customized compressed archived files (.lim) from your local system. See previous topics in this chapter to know more.

Example limits

Example limit sets is supplied with the Post Process Compliance tool.

The below example is based on a DDR800 part with 6-6-6 timing.

Example part:

- Data sheet: MICRON DDR3 MT41J256-32 Me x 4 x 8 Banks PDF: 09005aef82f1e6e2 Rev. M 9/08 EN
- Speed Grade 25 (6-6-6)
- Clock 400 MHz (2.5ns)
- Data Rate 800 MT/s
- Temperature 0-85C

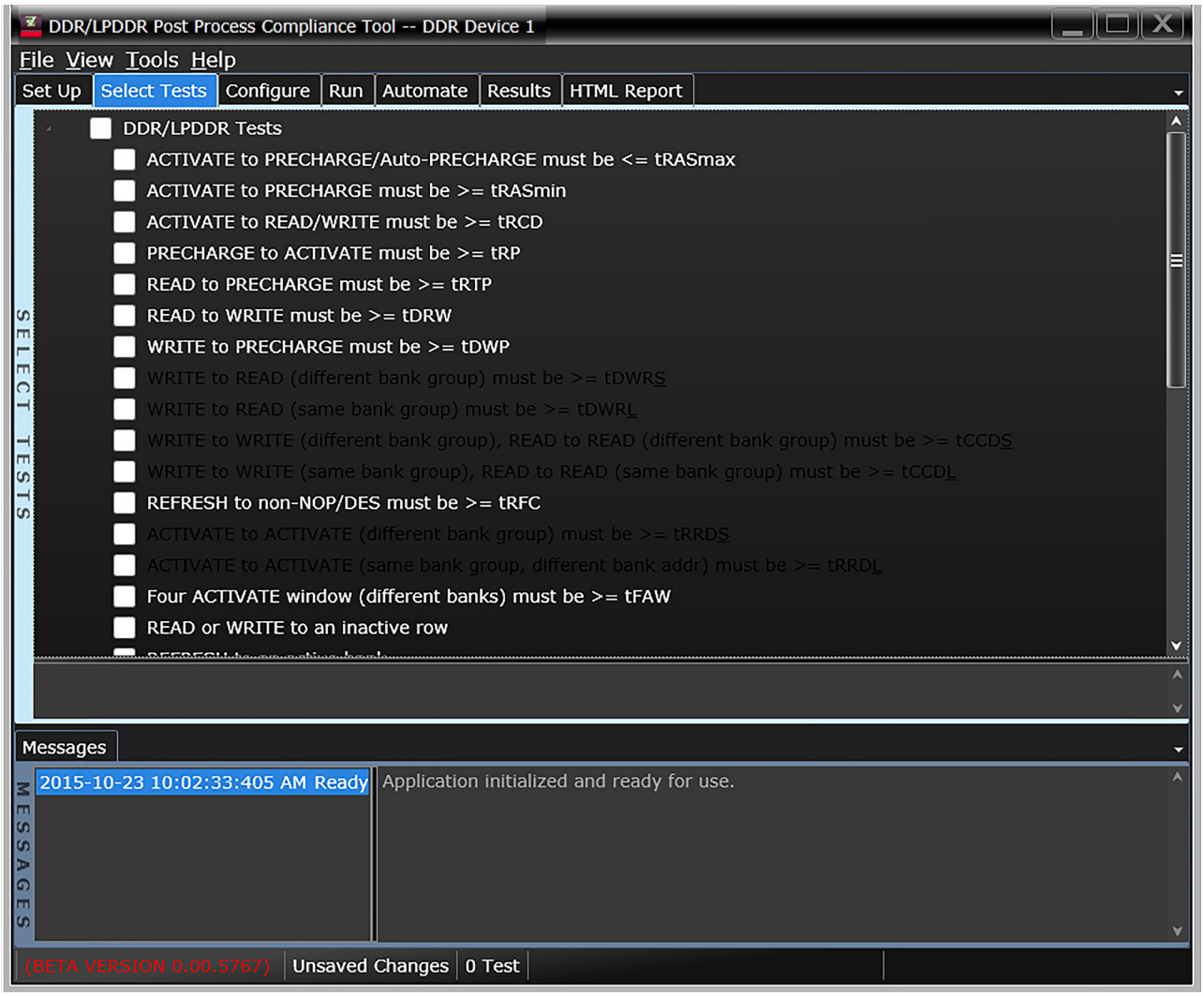
Parameter	Value	Reference
tREFI	7.8 us (low temp)	Data Sheet, page 71
$tRAS_{max}$	70.2us	Data Sheet (tREFI), page 63
$tRAS_{min}$	37.5ns	Data Sheet, page 30
tRP	15ns	Data Sheet, page 30
tCCD	4CK (10ns)	Data Sheet, page 70
tRRD	10ns	Data Sheet, page 30
tFAW	50ns	Data Sheet, page 30
tRFC	110ns	Data Sheet, page 30
tRCD	15ns	Data Sheet, page 30
tRTP	10ns	Data Sheet, page 70
tWR	15ns	Data Sheet, page 70
tWTR	10ns	Data Sheet, page 70
AL	0ns (0CK)	User selected (MR1, 0 means no additive latency)
BL	10ns (8 bursts)	User selected (MR0)
CL	6CK (15ns)	Data Sheet, page 30 (MR0)
CWL	5CK (12.5ns)	Data Sheet, page 116 (MR2)

Parameter	Value
RL	6CK (15ns)
WL	5CK (12.5ns)
tDARW	15ns
tDRP	10ns
tDRW	17.5ns
tDWP	32.5ns
tDWR	27.5ns

References

- DDR2 JEDEC Standard 79-2E, April 2008
- DDR3 JEDEC Standard 79-3C, November 2008

5 Selecting Tests



1 Click the **Select Tests** tab and then select the tests you want to run.

The tests displayed in this tab vary depending on the memory bus type and the rank addressing mode that you selected in the **Set Up** tab. For instance, the tests for same or different logical ranks are displayed if you select a 3DS rank addressing mode.

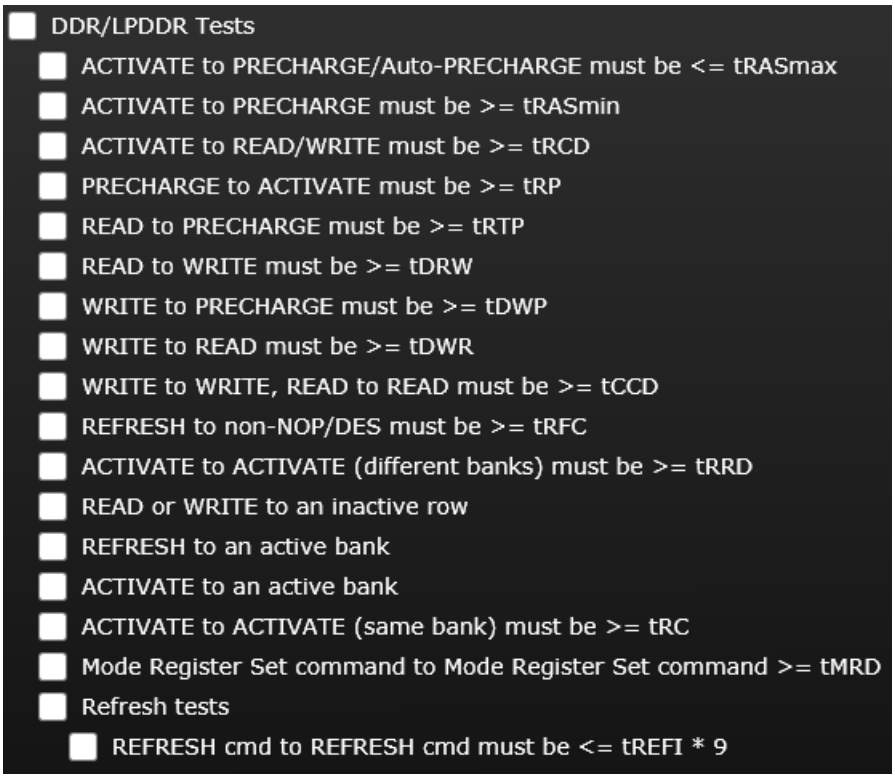
Some things to consider while selecting tests:

- Some tests might not make sense for your system. Do not select those tests.
- Checking a parent node/group will check all available sub-groups/tests.
- Unchecking a parent node/group will uncheck all sub-groups/tests.
- A parent node is checked if all subgroups are checked.
- A parent node is unchecked if ANY subgroup is unchecked.

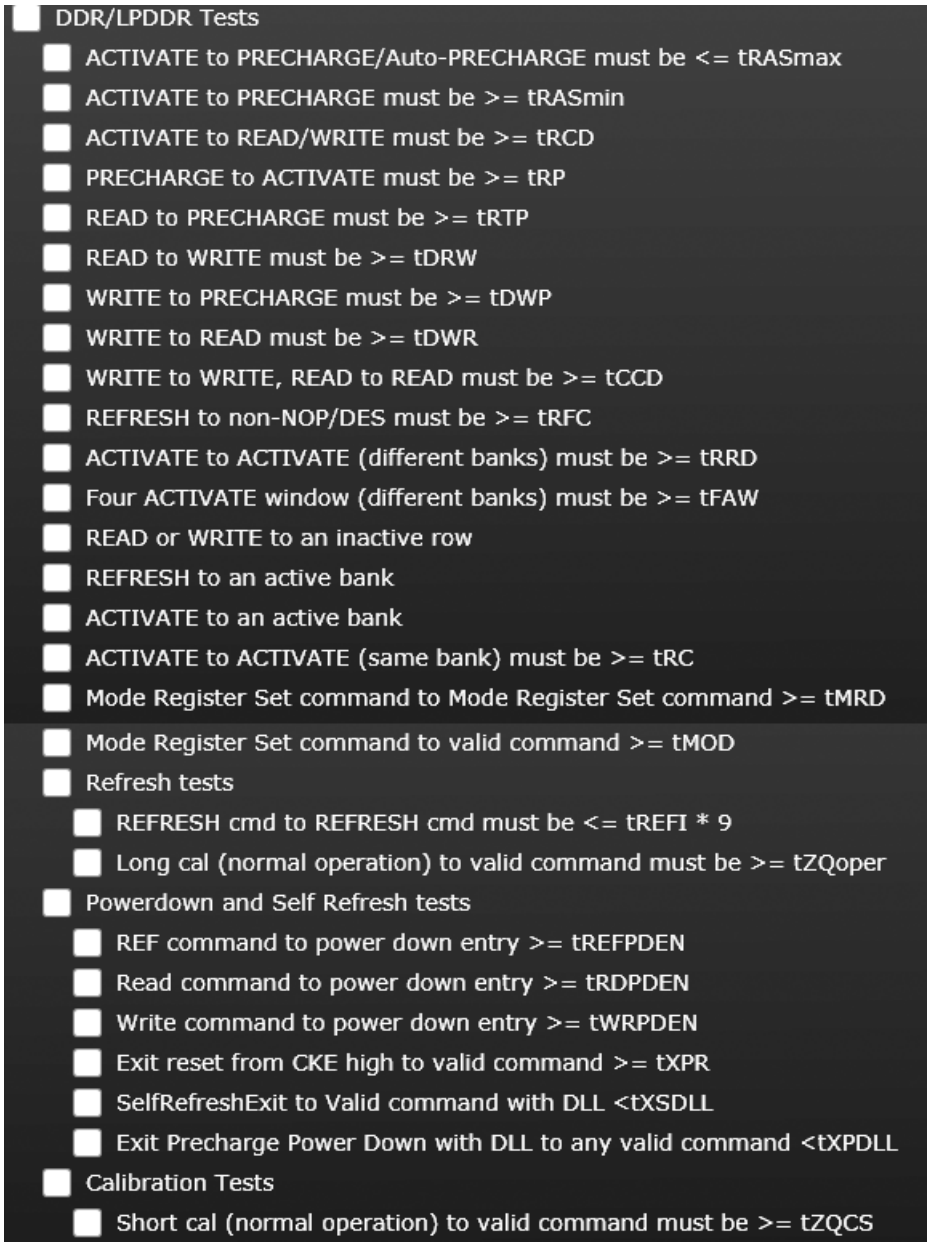
Tests Available With B4661A License (based on Memory type)

The following section lists the tests available for the memory bus types.

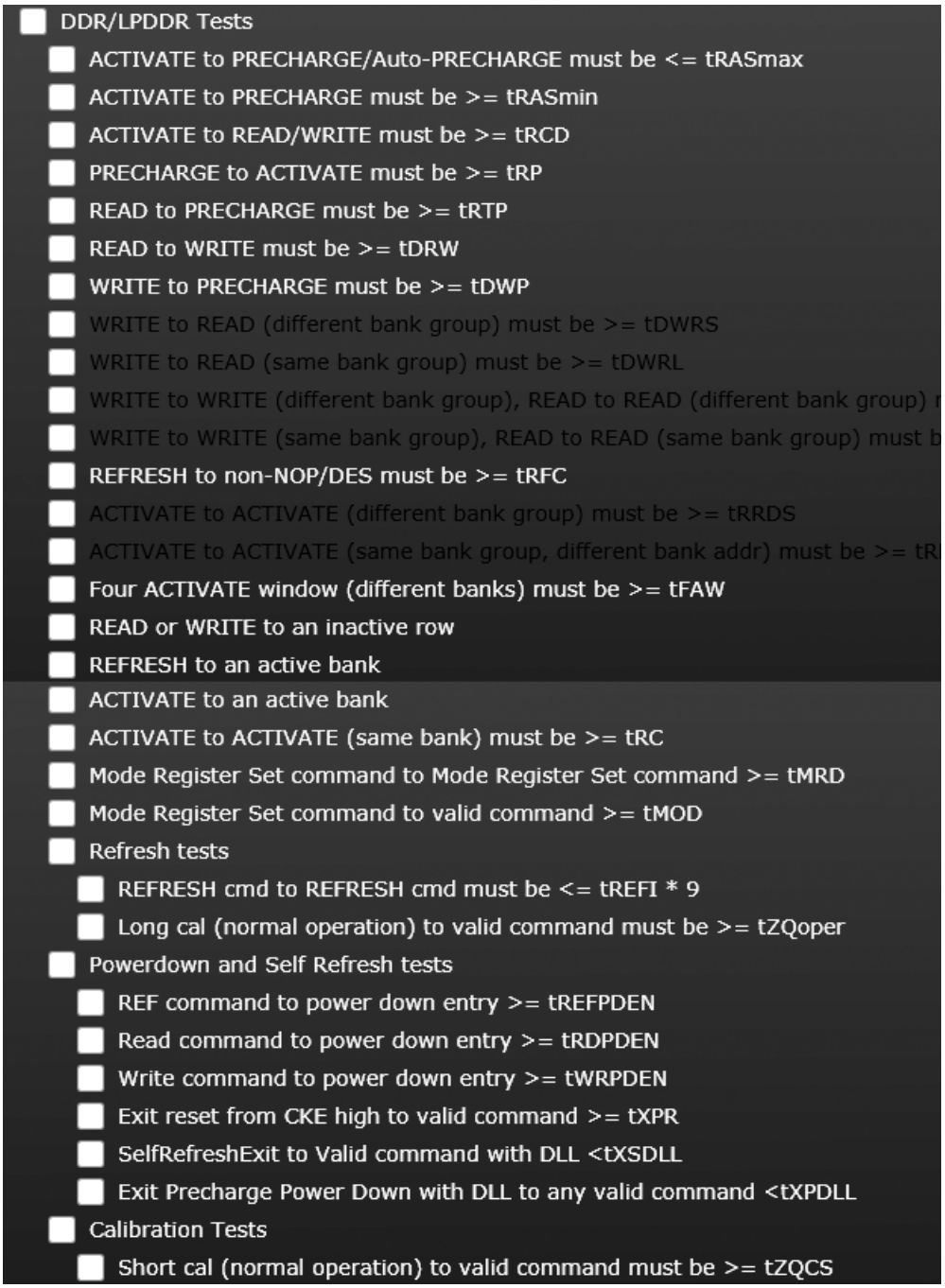
DDR1, 2 tests



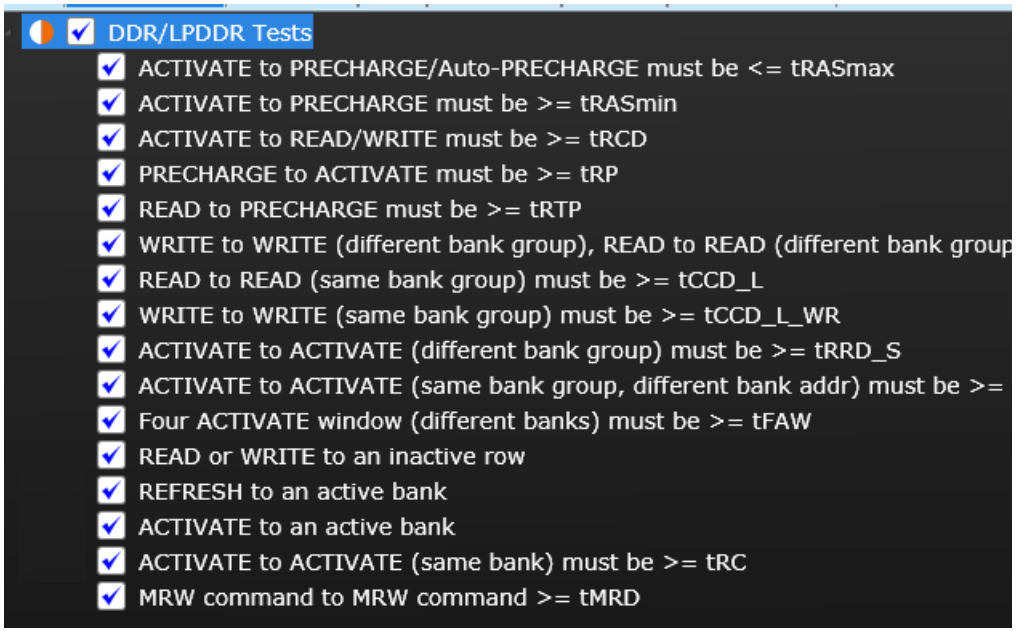
DDR3 tests


DDR/LPDDR Tests
ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax
ACTIVATE to PRECHARGE must be >= tRASmin
ACTIVATE to READ/WRITE must be >= tRCD
PRECHARGE to ACTIVATE must be >= tRP
READ to PRECHARGE must be >= tRTP
READ to WRITE must be >= tDRW
WRITE to PRECHARGE must be >= tDWP
WRITE to READ must be >= tDWR
WRITE to WRITE, READ to READ must be >= tCCD
REFRESH to non-NOP/DES must be >= tRFC
ACTIVATE to ACTIVATE (different banks) must be >= tRRD
Four ACTIVATE window (different banks) must be >= tFAW
READ or WRITE to an inactive row
REFRESH to an active bank
ACTIVATE to an active bank
ACTIVATE to ACTIVATE (same bank) must be >= tRC
Mode Register Set command to Mode Register Set command >= tMRD
Mode Register Set command to valid command >= tMOD
Refresh tests
REFRESH cmd to REFRESH cmd must be <= tREFI * 9
Long cal (normal operation) to valid command must be >= tZQoper
Powerdown and Self Refresh tests
REF command to power down entry >= tREFPDEN
Read command to power down entry >= tRDPDEN
Write command to power down entry >= tWRPDEN
Exit reset from CKE high to valid command >= tXPR
SelfRefreshExit to Valid command with DLL <tXSDLL
Exit Precharge Power Down with DLL to any valid command <tXPDLL
Calibration Tests
Short cal (normal operation) to valid command must be >= tZQCS

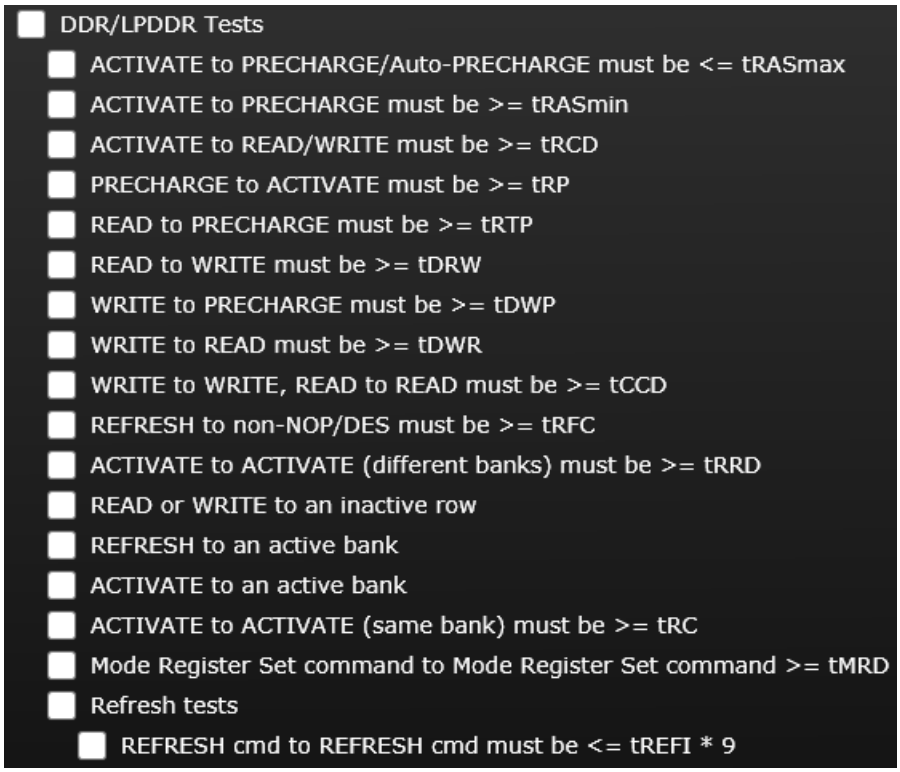
DDR4 Tests


DDR/LPDDR Tests
ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax
ACTIVATE to PRECHARGE must be >= tRASmin
ACTIVATE to READ/WRITE must be >= tRCD
PRECHARGE to ACTIVATE must be >= tRP
READ to PRECHARGE must be >= tRTP
READ to WRITE must be >= tDRW
WRITE to PRECHARGE must be >= tDWP
WRITE to READ (different bank group) must be >= tDWRS
WRITE to READ (same bank group) must be >= tDWRL
WRITE to WRITE (different bank group), READ to READ (different bank group)
WRITE to WRITE (same bank group), READ to READ (same bank group) must b
REFRESH to non-NOP/DES must be >= tRFC
ACTIVATE to ACTIVATE (different bank group) must be >= tRRDS
ACTIVATE to ACTIVATE (same bank group, different bank addr) must be >= tR
Four ACTIVATE window (different banks) must be >= tFAW
READ or WRITE to an inactive row
REFRESH to an active bank
ACTIVATE to an active bank
ACTIVATE to ACTIVATE (same bank) must be >= tRC
Mode Register Set command to Mode Register Set command >= tMRD
Mode Register Set command to valid command >= tMOD
Refresh tests
REFRESH cmd to REFRESH cmd must be <= tREFI * 9
Long cal (normal operation) to valid command must be >= tZQoper
Powerdown and Self Refresh tests
REF command to power down entry >= tREFPDEN
Read command to power down entry >= tRDPDEN
Write command to power down entry >= tWRPDEN
Exit reset from CKE high to valid command >= tXPR
SelfRefreshExit to Valid command with DLL <tXSDLL
Exit Precharge Power Down with DLL to any valid command <tXPDLL
Calibration Tests
Short cal (normal operation) to valid command must be >= tZQCS

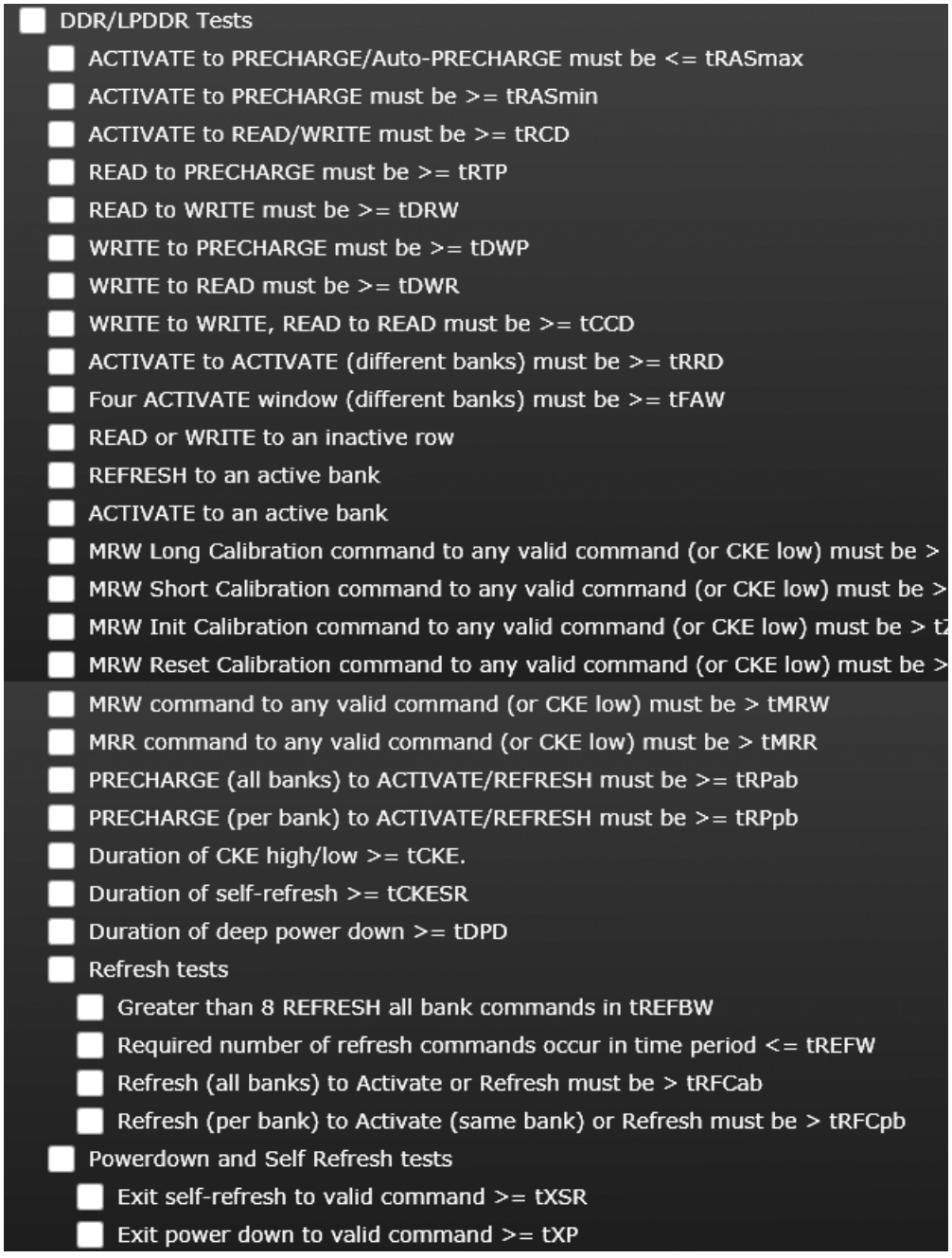
DDR5 Tests



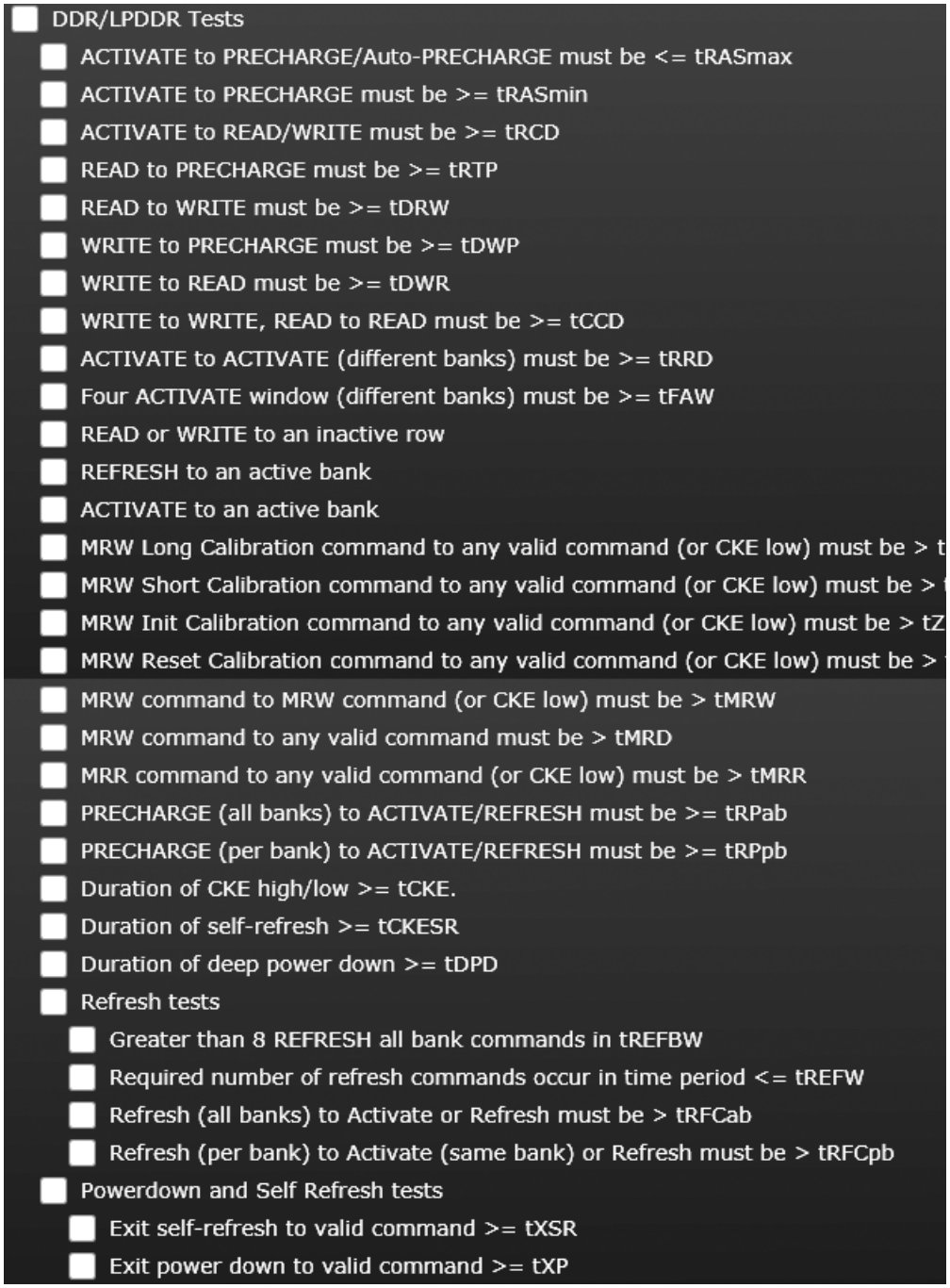
LPDDR tests



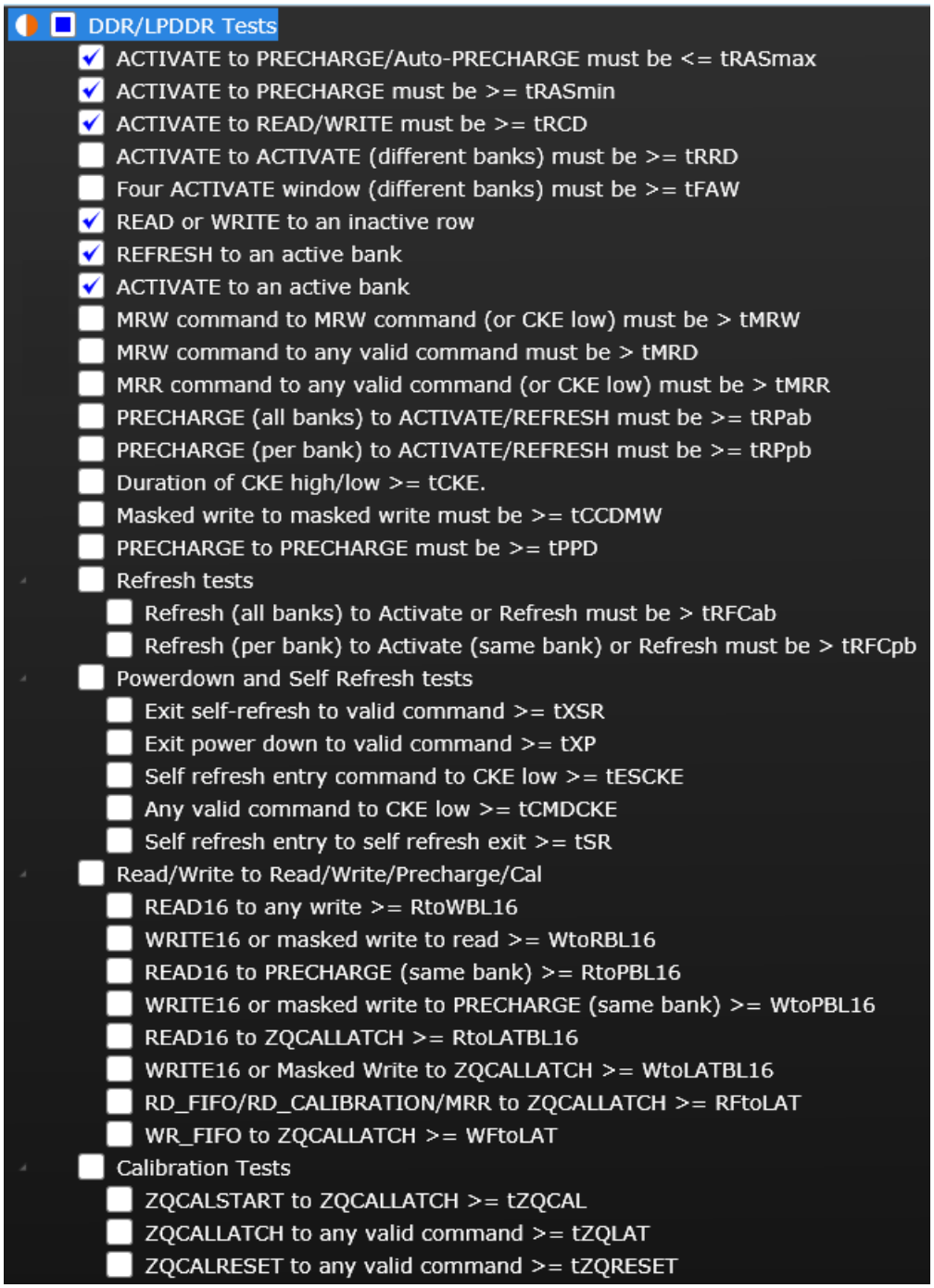
LPDDR2 tests



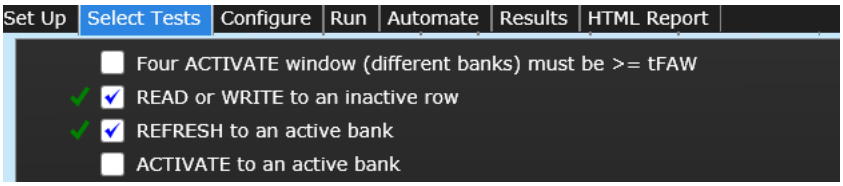
LPDDR3 Tests



LPDDR4 Tests



When Tests Have Already Been Run



The marks have the following meanings:

Marks	Meanings
✓	The test passed.
	The test failed.
	The test has not been run, or no tests in the group have been run.
	The test is currently running.
	Some tests in the group have run and passed.
	Some tests in the group have run and failed.
	Some tests in the group have passed and some have failed; not all of the tests have run.
	All tests in the group have run and passed.
	All tests in the group have run and failed.

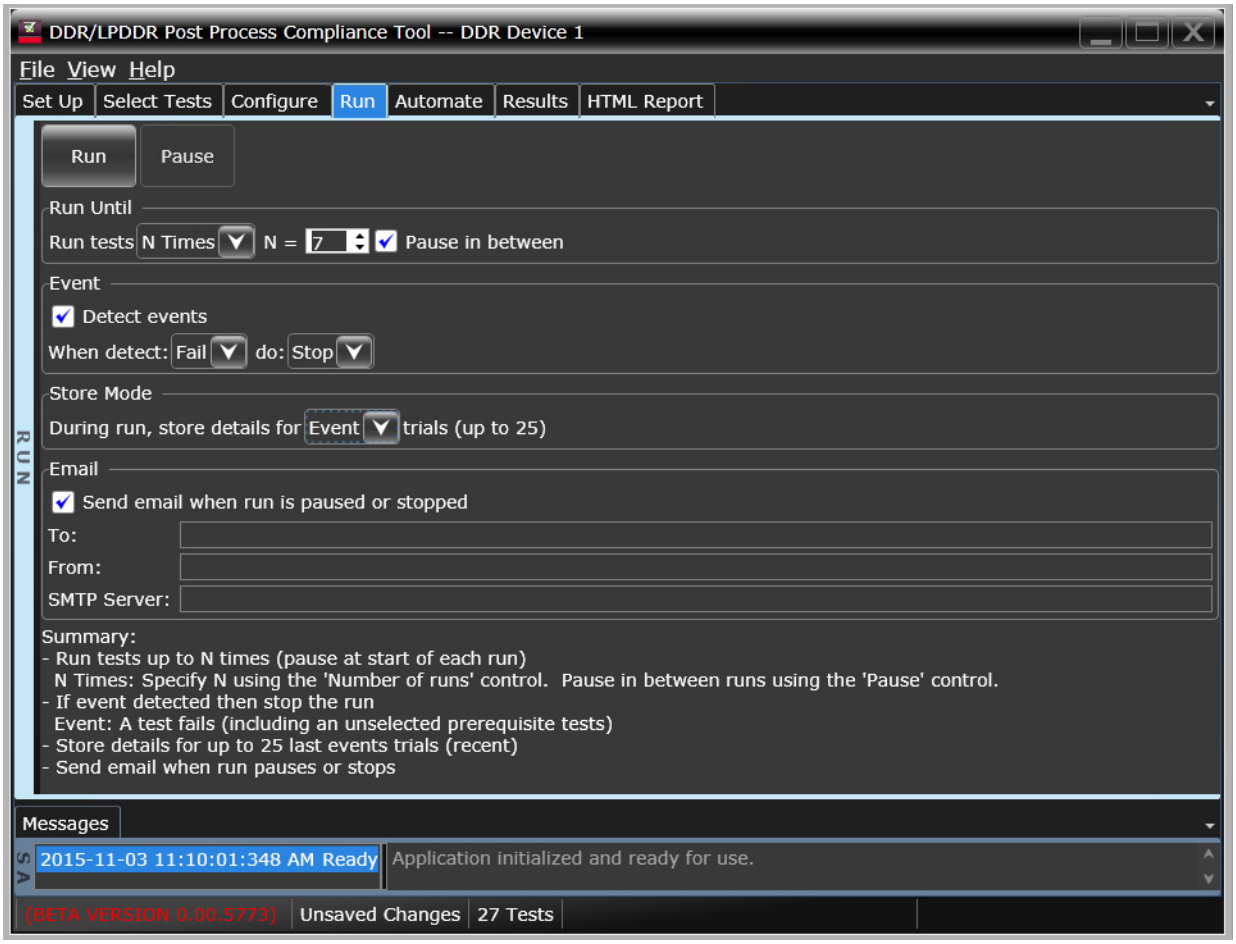
See Also
- "To set the test limits (for information on how to calculate the limits)" on page 36 (for information on how to calculate the limits)
- "About the Tool" on page 11 (for an overview of the tests performed)

Next
- "Configuring Tests Limits" on page 21

6 Running Tests

You can use the **Run** tab to specify how the tests should be run and then run the tests as per these settings.

You can run the tests once or repetitively.



To run the selected tests:

1 Click the **Run** tab.

2 Configure the settings for running the tests.

   a From the **Store Mode** section, select which trial results from the test run(s) you want to store. You can store results for a maximum of 25 trials.

   b From the **Run Until** section, select the number of times you want to run the tests. Following options are available:

   - Once - The tests are run once.

- N Times- The tests are run repetitively for the number of times specified in the Number of Runs field.
- Forever- The tests are run repetitively until you press the Stop button.

If you select **N Times** or **Forever**, make sure you select the **Automatically acquire new logic analyzer data when running tests** checkbox in the **Set Up** tab.

c On selecting the **N Times** option, the **Pause in between** checkbox is displayed. Select this checkbox to instruct the tool to pause the test run after the completion of each run in the repetitive run.

d Select the **Send email when run is paused or stopped** checkbox in the **Email** section to instruct the tool to send a notification email with the information about the test run when the test run completes or pauses. You can specify the SMTP Server and the email address to which email should be sent in the designated place when this checkbox is selected. You can also specify the sender's email address.

e In the **Event** section, select the **Detect Event** checkbox to instruct the tool to perform a specified action when the specified event is detected in the test run. On selecting this checkbox, a listbox is displayed with this checkbox. From this listbox, you can select either Pause or Stop to pause or stop the test run when the selected event is detected during a test run.

f When you select Event in the **Store Mode** section or select the **Detect Event** checkbox, the **When detect:** listbox is displayed to allow you to select the event. When the selected event occurs in the test run, the specified action is performed if the **Detect Event** checkbox is selected or the details for the event are stored if the **Store Mode** is set to **Event**. You can select from the following events:

- Pass - Perform the event action or store the event details when a test passes.
- Fail - Perform the event action or store the event details when a test fails.
- Margin < N - Perform the event action or store the event details when a test result margin is less than the specified minimum required margin percentage.

At times, you may receive warning messages when the selected event does not logically matches with the selected Store Mode. For instance, if the **Store Mode** is **Best**, then you can only use **Pass** as the event. Similarly, if the store mode is **Worst**, you cannot use **Pass** as the event. The tool automatically corrects the event selection in such cases.

While you select the test configurations, the tool automatically keeps documenting the test configurations for your reference in the open listbox in this tab. The **Message** tab displays the list of actions and any warnings if generated.

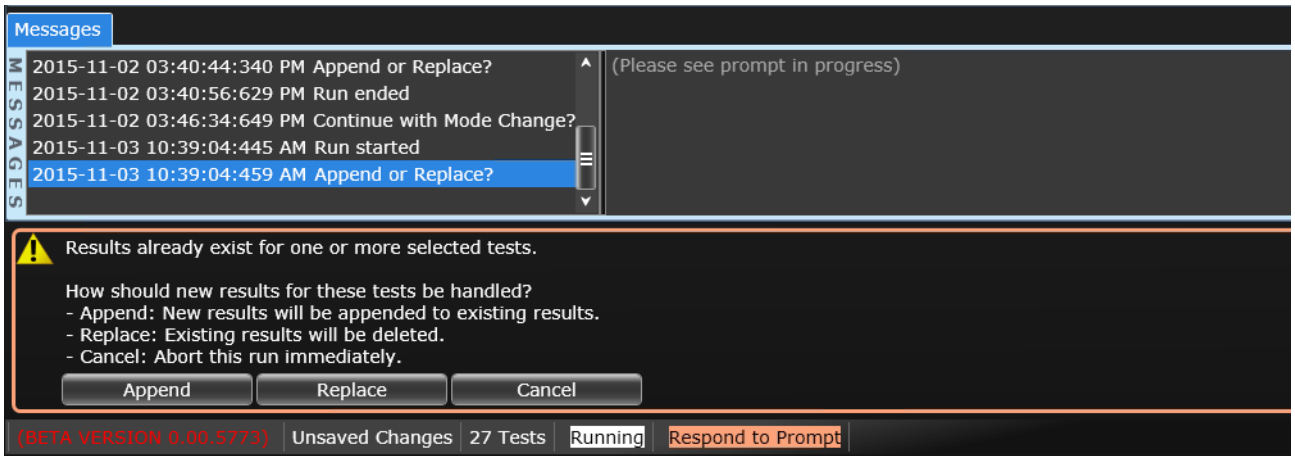
3 Run the tests. There are several ways to run the selected tests:

- Click  in the toolbar. to run all the selected tests.
- Select a branch in the Select Tests tab and then click  in the toolbar to repeatedly run only the tests of the selected branch.
- Click the big **Run** button in the Run tab.

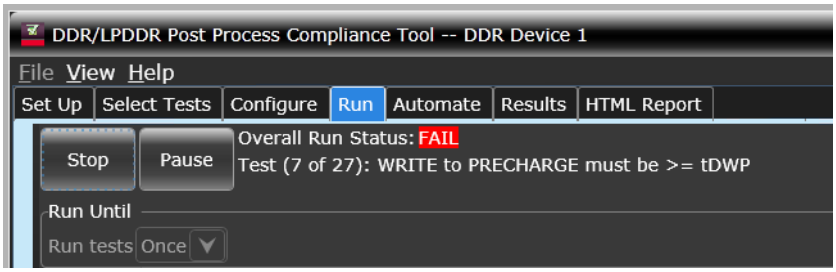
4 If there are existing test results, you are asked if you would like to keep them or re-test (delete) them.

If you would like to keep the existing test results to compare against new results, click **Append**.

Click **Replace** if you would like to delete the existing test results.



5 While the tests are running, status dialogs appear to inform you about the test progress.



When the tests are complete, Results tab is automatically displayed.

See Also
- "To set the display preferences" on page 52

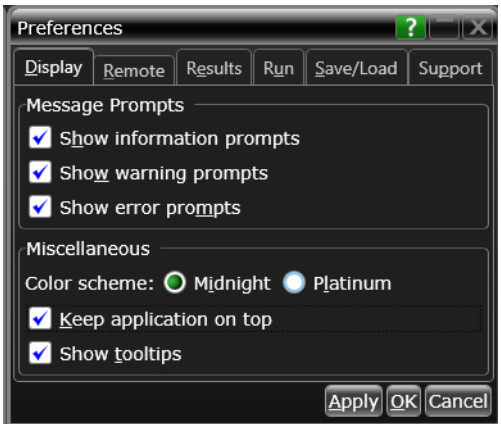
Next
- "Viewing Results" on page 57

To set the display preferences

Information, warning, and error conditions can occur while running tests. The display preferences let you choose whether message dialogs are shown. And, there are other display preferences that affect what happens as tests are run.

1 From the DDR/LPDDR Post Process Compliance Tool's menu, choose **View > Preferences...**.

2 In the Preferences dialog, select the **Display** tab.



3 In the Display tab, you can choose to show the following types of message prompts:

- Information prompts.
- Warning prompts.
- Error prompts.

NOTE Messages that require you to make a choice, such as "OK/Cancel" and "Yes/No" are always enabled.

4 Also, you can choose to:

- **Change the Color Scheme**– Choose a background color from Midnight and Platinum options.
- **Keep application on top** – Always keep the application's main dialog on the top of the logic analyzer application. Note that the mid-run dialogs are always displayed on the top.
- **Show tooltips** – By enabling this option, the tooltips appear as you move the pointer over various controls in the application.

5 Click **Apply** to save the changes and click **OK** to close the Preferences dialog.

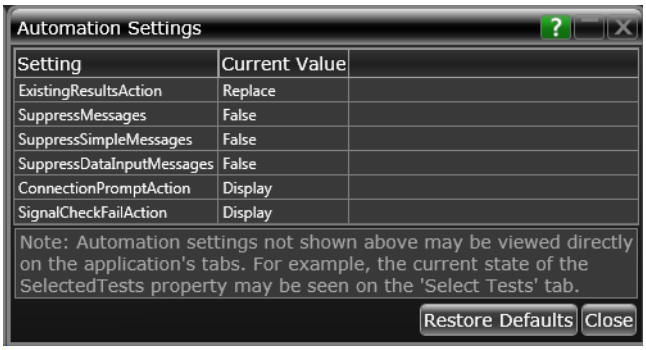
7 Automating the Tests

In the **Automate** tab, you can automate the required tests by selecting either of the following options from the **Execute commands from** section:

- Scripts
- Files

Prerequisites

1 Click **Settings**. The Automation Settings window appears.

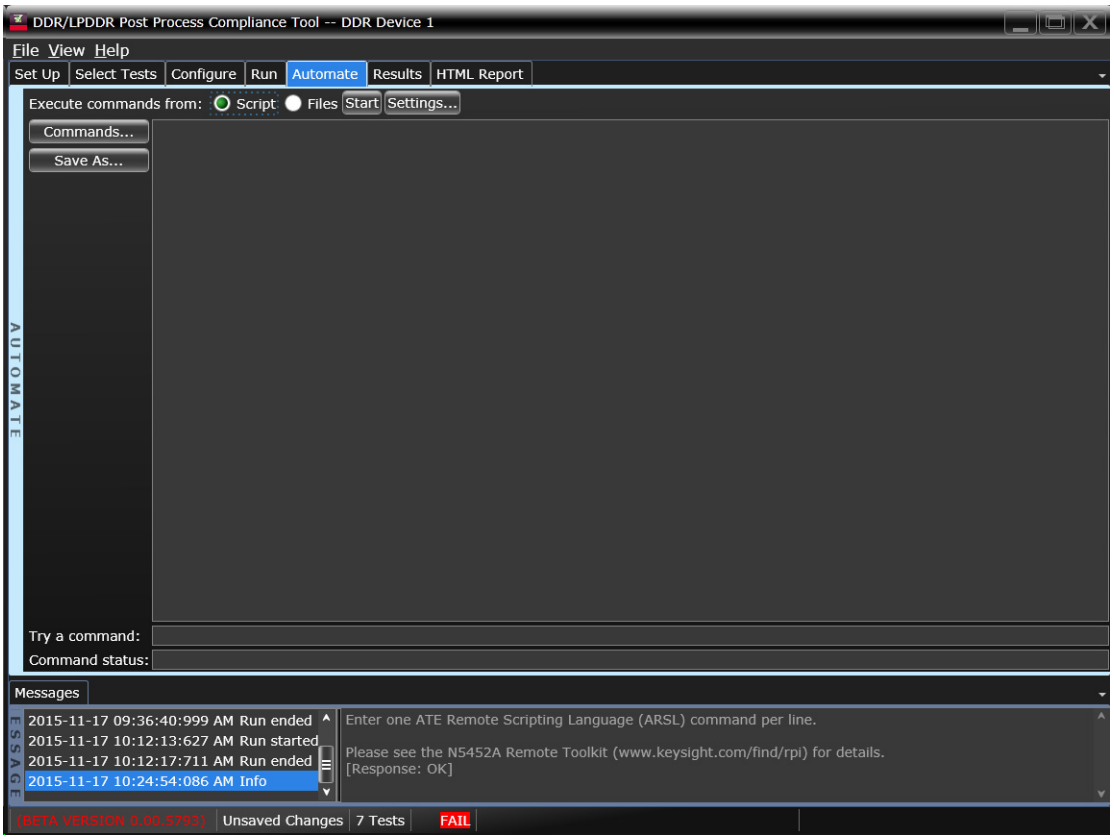


2 Check and change (if required) the appropriate settings and click **Close**.

Automation by Scripts

Perform the following steps to automate the tests by scripts:

1 Write the automation programs/commands in the top pane.



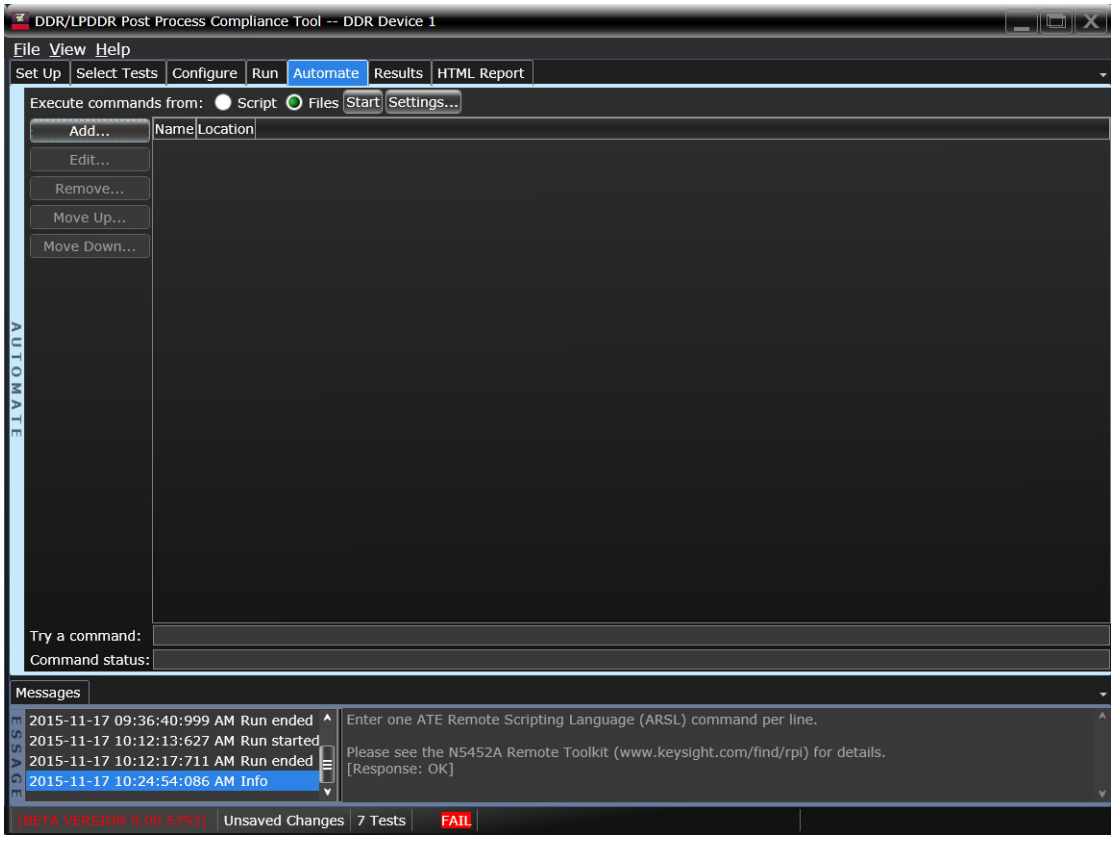
2 Click **Save As...** to save the automation script on your local system.

3 Click **Start**.

Automation by Files

Perform the following steps to automate the tests by files:

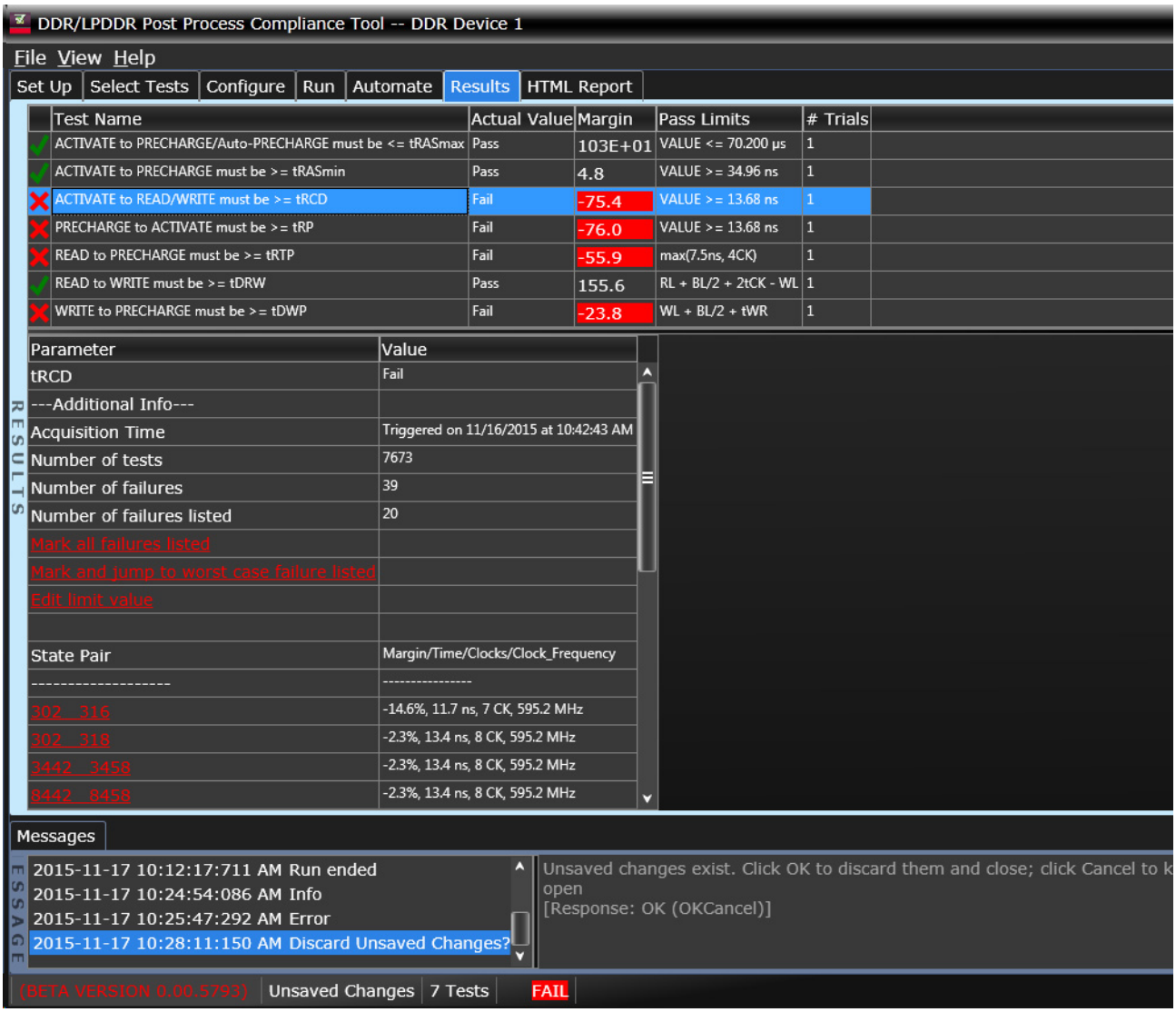
1 Click **Add...** to load the required file. The loaded file is displayed in the upper pane.



2 Click **Start**.

8 Viewing Results

1 Click the **Results** tab.



The Results tab contains three re-sizable panes for test results information. If you select one of the tests in the top pane, details and reference images (if any) are shown in the lower panes.

TIP A quick way to reset all configuration options and delete all test results is to create a new project (see page 69). The new project will have default configuration options.

For each individual test that you selected to run, the tool reports the total number of failures that occurred for that specific test. It can show up to a maximum of *250 failures* in the Details screen for an individual test.

Each limit is measured as the time between two states. Each logic analyzer state has a number and a timestamp. In case of a failure, the numbers of the two states will be reported. Note that the time stamps are only as good as the time stamp resolution of the logic analyzer card being used (this resolution may be as coarse as 2ns; see the Specifications and Characteristics in the logic analyzer's Online help for details).

If a test case is not encountered in the logic analyzer trace:

- In the details for the test, the number of tests will be 0.
- For limit tests, the “Actual Value” column will display “N/A.”
- For pass/fail tests, the “Actual Value” column will display “Pass.”

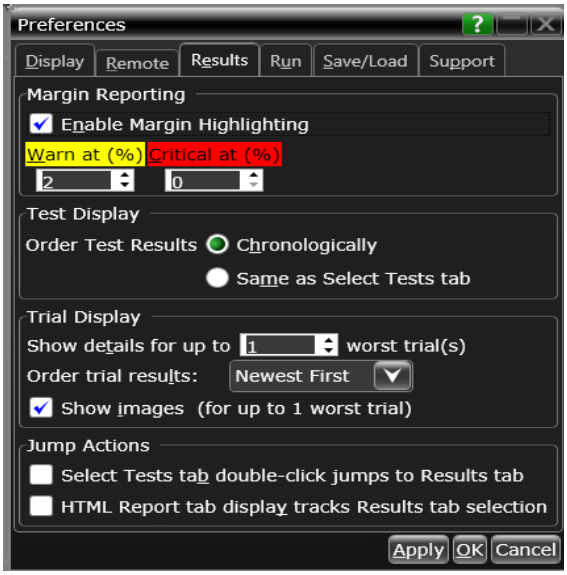
See Also · “To change margin thresholds" on page 59

Next · “Viewing/Exporting/Printing the Report" on page 61

To change margin thresholds

1 From the DDR/LPDDR Post Process Compliance Tool's menu, choose **View>Preferences...**.

2 In the Preferences dialog, select the **Results** tab.



3 In the **Margin Reporting** area, you can:

- Enable or disable margin highlighting.
- You can change the percent of margin at which to give warnings or critical failures.

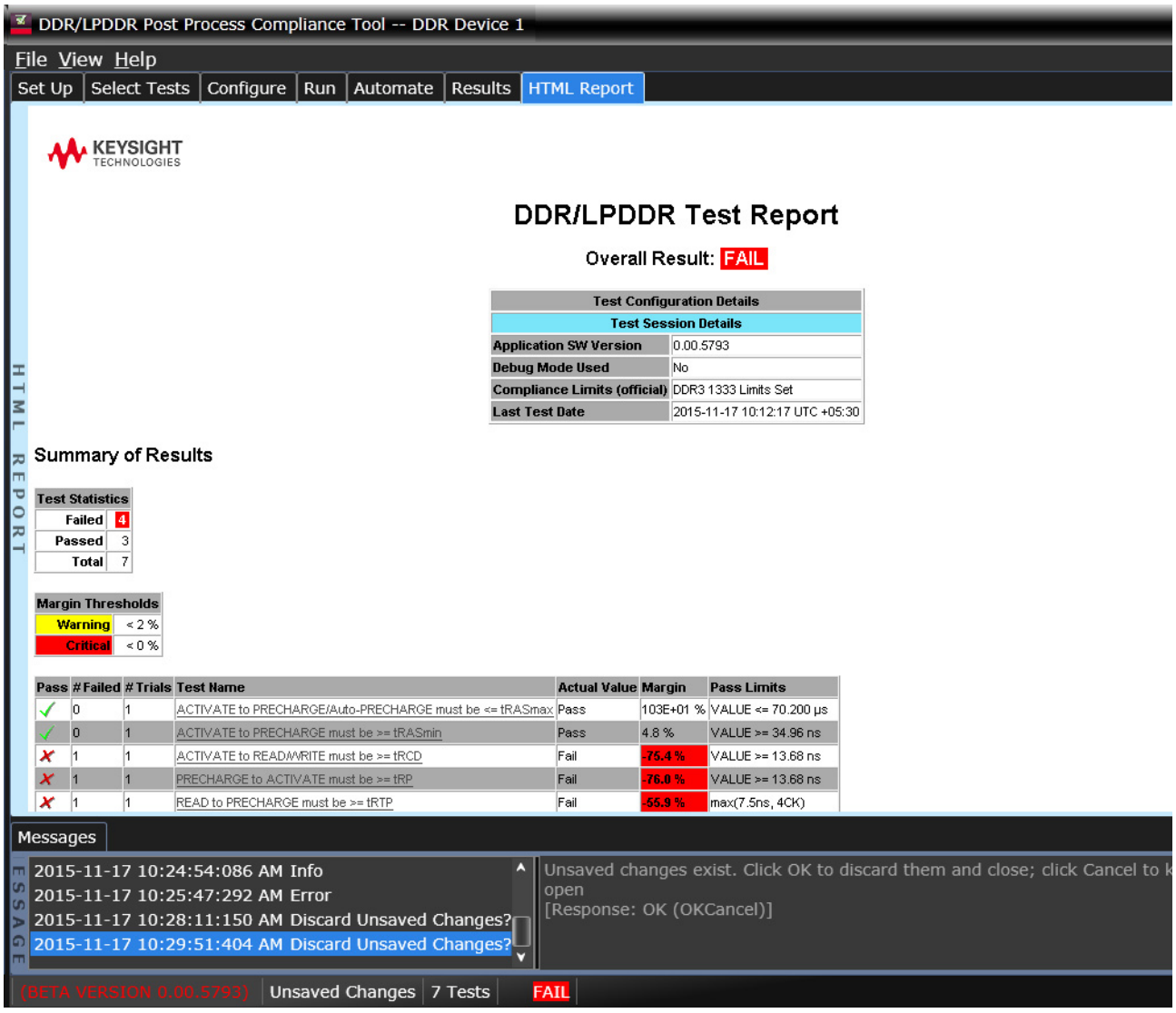
4 Click **OK** to close the Preferences dialog.

NOTE The DDR/LPDDR Post Process Compliance Tool runs the tests one time, so the Trial display options do not apply.

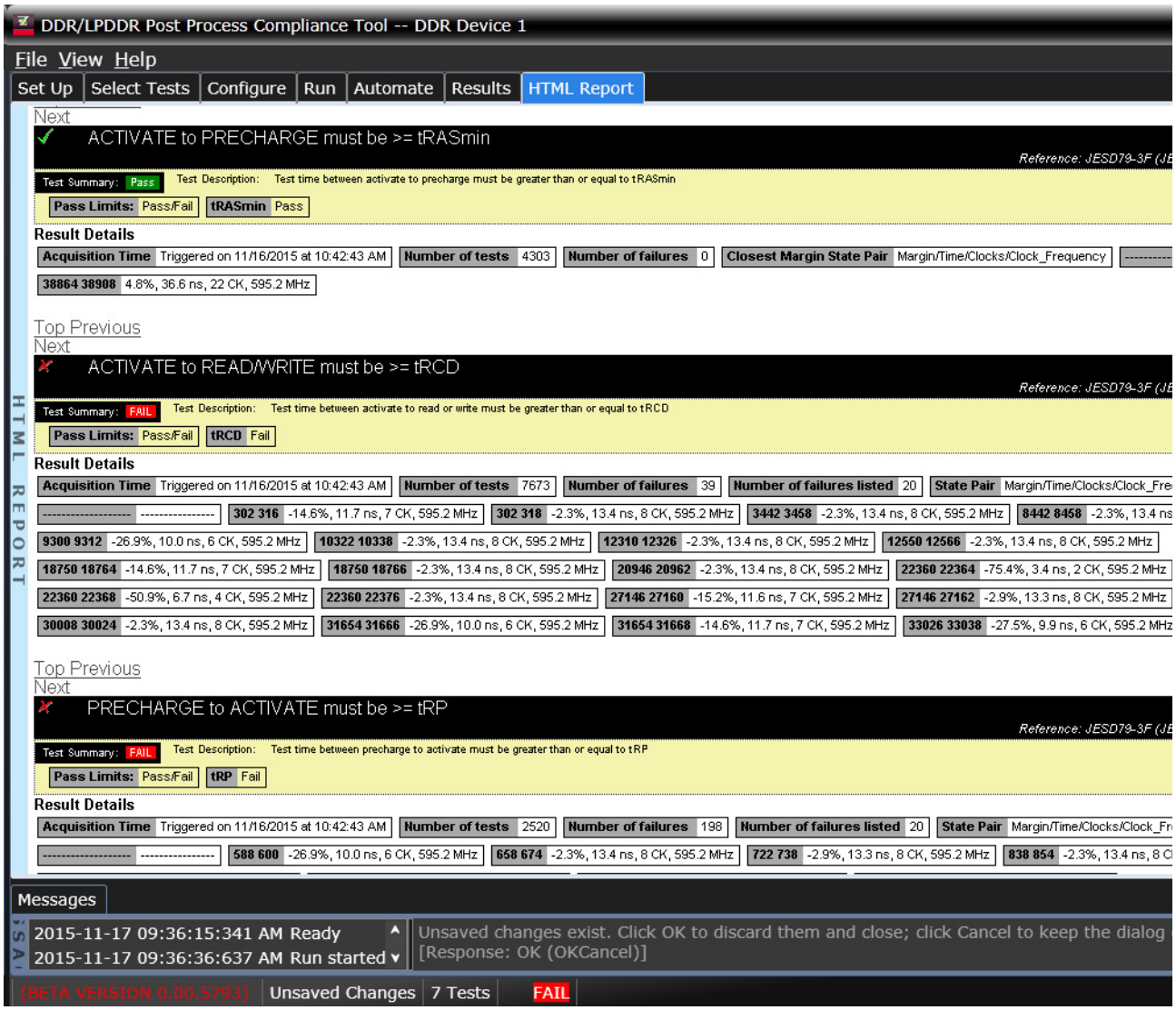
You can set the display order of test result in **Test Display** section.

9 Viewing/Exporting/Printing the Report

- To view the HTML test report, click the **Html Report** tab.



Clicking on any tests under Test Name section displays the details of the particular test result.



See Also · "To export the report" on page 63
· "To print the report" on page 65

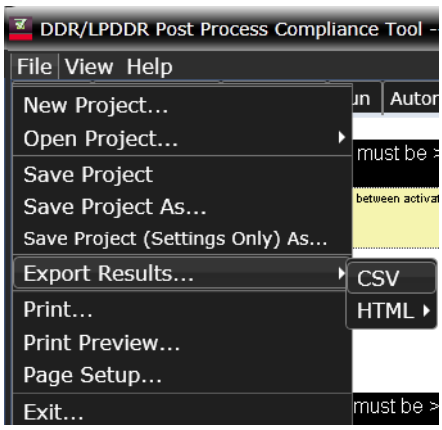
Next · "Saving Test Projects" on page 67

To export the report

1 From the DDR/LPDDR Post Process Compliance Tool's menu, choose **File > Export Results**. There are two options for exporting the HTML test report: CSV or HTML.

To export results in CSV (comma-separated values) format

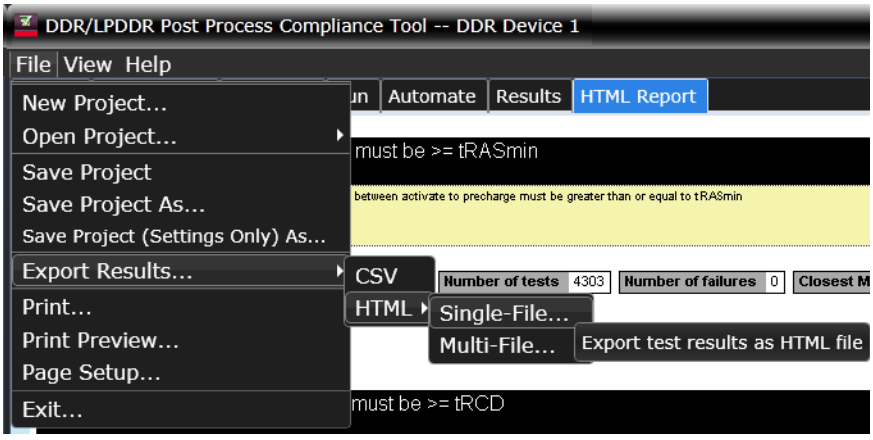
Select the CSV option to export the results as a comma-separated list of values.



The data format is shown in the first line of the exported *.csv file.

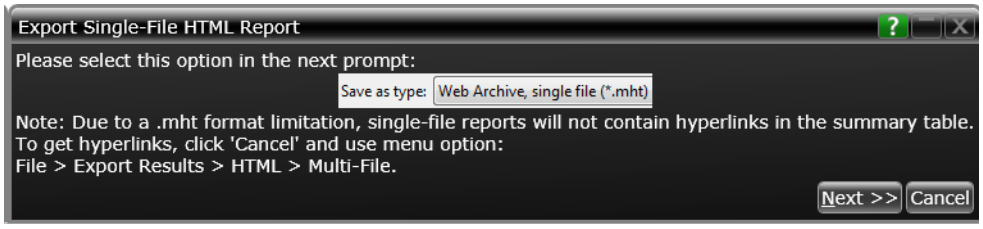
```
Test ID, Test Name, Measured Item, Trial 1 Value
100,"ACTIVATE to PRECHARGE/Auto-PRECHARGE must be < tRASmax",Number of t
ests ,"9"
100,"ACTIVATE to PRECHARGE/Auto-PRECHARGE must be < tRASmax",Number of f
ailures ,"0"
100,"ACTIVATE to PRECHARGE/Auto-PRECHARGE must be < tRASmax",Actual Valu
e,"4.92E-05"
100,"ACTIVATE to PRECHARGE/Auto-PRECHARGE must be < tRASmax",Margin,"29.
9"
```

To export the report in HTML format



There are two options for exporting HTML format test reports:

- **Single-File** – To save a single-file report, use the “save as” type “Web Archive, single file (.mt)”.



NOTE Single-file reports will not contain hyper-links in the summary table (due to a .mht format limitation). If you want these hyper-links, use the multi-file format.

- **Multi-File** – If your report is large and you would like to use links within the report, select the **HTML>Multi-File** option. Selecting the multi-file option exports the results as a set of separate image and HTML files. It creates a folder with the specified name that may be copied to any computer.

  To view the exported report, open the HTML file stored in the folder.

To print the report

- To preview the HTML test report printout, choose **File>Print Preview...** from the menu.
- To print the HTML test report, choose **File>Print...** from the menu.

10 Saving Test Projects

To save test settings and results to the current project directory:

1 Choose **File>Save Project** from the menu.

To save test settings and results to a new project directory:

1 Choose **File>Save Project As...** from the menu.

2 In the Save Project As... dialog, enter the device name and location. Project files will be saved in a directory whose name is the device name.

3 Click **OK**.

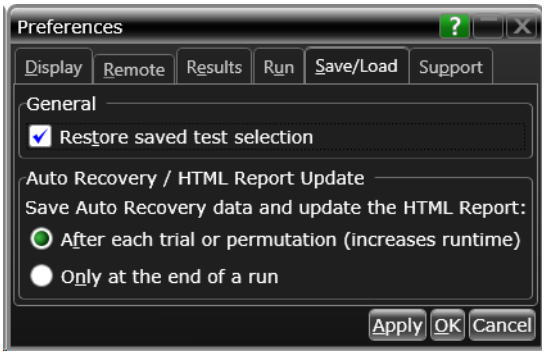
See Also

- "To set AutoRecovery preferences" on page 68

To set AutoRecovery preferences

1 From the DDR/LPDDR Post Process Compliance Tool's menu, choose **View>Preferences...**.

2 In the Preferences dialog, select the **Save/Load** tab.



3 In the **AutoRecovery/HTML Report Update** section, you can choose:

- To auto-save results after each trial or permutation even if the entire multi-trial is not completed. This option enables full recovery.
- To auto-save results only upon the completion of the entire multi-trial.

4 Click **Apply** to save the changes and click **OK** to close the Preferences dialog.

11 Creating or Opening a Test Project

To create a new test project:

1 Choose **File>New Project...** from the menu.
A new, empty project, with all the default settings is created.

To open an existing test project:

1 Choose **File>Open Project...** from the menu.
2 In the Open dialog, browse to a test project directory and select the desired ".proj" file.
3 Click **Open**.

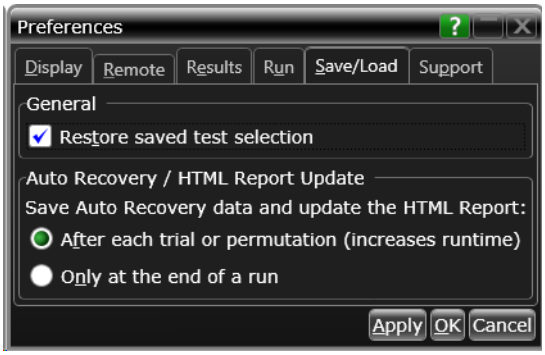
See Also · "To set load preferences" on page 70

Next · "Setting Up the Test Environment" on page 19

To set load preferences

1 From the DDR/LPDDR Post Process Compliance Tool's menu, choose **View>Preferences...**.

2 In the Preferences dialog, select the **Save/Load** tab.



3 In the **Save/Load** tab, you can choose to restore saved test selections when loading a project.

4 Click **Apply** to save the changes and click **OK** to close the Preferences dialog.

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