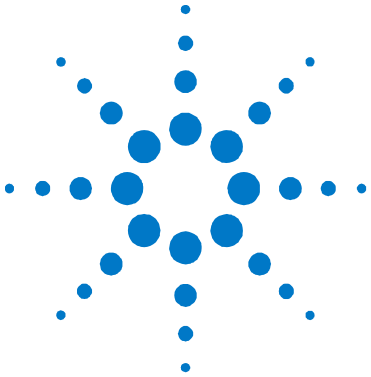

Agilent N4835A

DDR3 DIMM Interposer

Installation Guide

Agilent Technologies

Notices

Manual Part Number

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CAUTION

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WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

Contents

1 Introduction

The Agilent N4835A interposer is manufactured by FuturePlus Systems Corporation, and bear FuturePlus product markings. The FuturePlus product number is FS2351.

Agilent N4835A Interposer Description

The Agilent N4835A DDR3 interposer allows you to capture state data from DDR3 DIMM busses. The included protocol decoder will decode the captured trace and format the information into read, write and other transactions.

The interposer design of this interposer allows any DDR3 connection to be probed while it supports a DDR3 DIMM module.

Interposer Technical Feature Summary

- Quick and easy connection between the DDR3 240 pin DIMM connector and Agilent Logic Analyzers.
- Capture up to 1333MT/s (if the electrical design of the target permits).
- Interposer design does not consume a DDR3 slot.
- Complete and accurate state analysis up to 1333 MT/s.
- Protocol decoder software.
- Uses Auto Sample Position Set-up (eye finder) and Auto Threshold Set-up to locate tight DDR3 data valid windows for optimal state data capture. In addition, DDR3 eye finder software allows sample position setup for targets which cannot be programmed to generate read-only and write-only patterns.

Service and Support

Please contact your Agilent Technologies representative for service and support.

Equipment Supplied

The following components have been shipped with your Agilent N4835A DDR3 interposer:

- Agilent N4835A DDR3 DIMM interposer
- Software Entitlement Certificate for the decoder.

Equipment Required

- Agilent 16900-series logic analysis system
- Four Agilent 16960A logic analyzer cards connected together as a module

Signal Assignments on Interposer Pods

The overlap in the bit ranges (for DQxx) signals between pods occurs because the bits are assigned to pods in the order that they appear physically on the DDR3 DIMM connector, which is not strictly in logical bit order. This allows the interposer layout to better match stub lengths among all DQxx signals.

See Appendix: Signal Mapping for a detailed list of how Logic Analyzer Channels are mapped to signals and DDR3 pins.

Signal Threshold Voltage Settings

DDR3 utilizes the SSTL_15 signaling standard. The nominal threshold is 750 mV. The logic analyzer configuration uses the HSTL threshold which is also 750 mV. Design differences between target platforms or overvoltage settings may require adjustment of the logic analyzers threshold for optimal signal capture. The use of Eye Scan could be crucial in determining where to set these thresholds.

NOTE: The optimal settings may need to be defined either through trial and error or by using Eye Scan. Accurate data capture is very dependent on optimizing these settings and changes of as little as 50mV may have a significant effect.

Definitions

Logic Analyzer Modules

"Module" - A set of logic analyzer cards that have been configured (via cables connecting the cards) to operate as a single logic analyzer whose total available channels is the sum of the channels on each card. A trigger within a module can be specified using all of the channels of that module. Each module may be further broken up into "Machines". A single module may not extend beyond 6 card 16900 frame.

Logic Analyzer Machine

"Machine" - A set of logic analyzer pods from a logic analyzer module grouped together to operate as a single state or timing analyzer.

Mechanical Requirements

Be careful to allow adequate space around the interposer for egress of the logic analyzer cables.

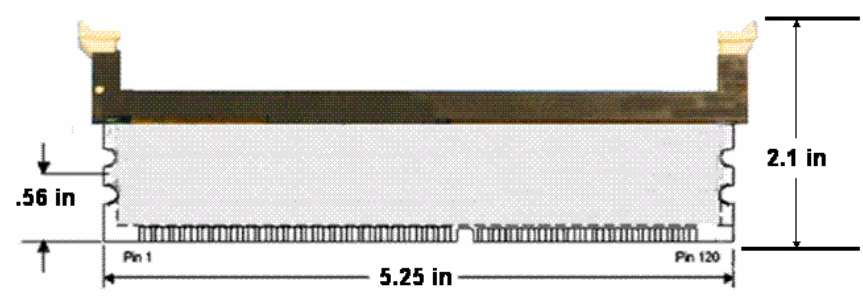


Figure 1 Interposer dimensions: front view

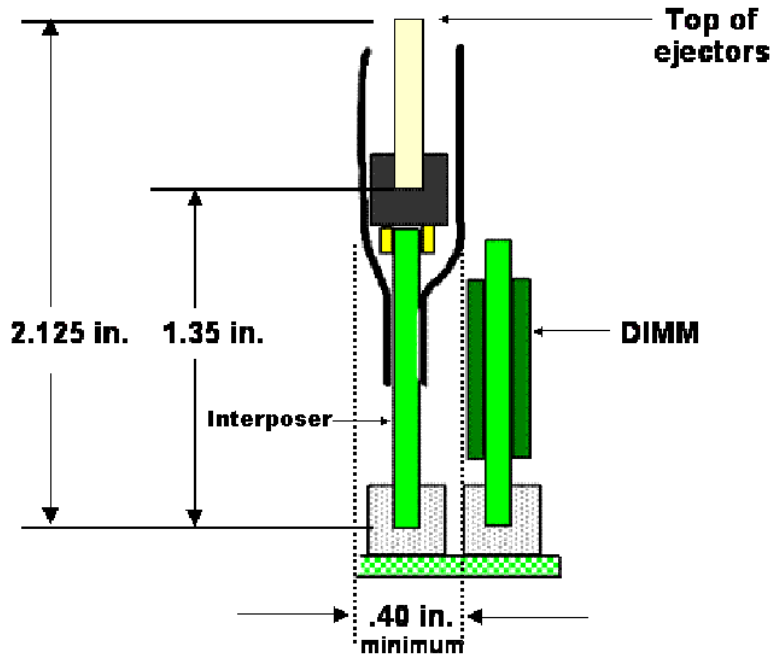


Figure 2 Interposer dimensions: side view

2 Validating Interposer Compatibility With Your Target System

Since the electrical characteristics of each board are different, it is important to verify that the interposer will operate properly in *your* system.

This interposer has been tested and validated in a number of target systems with multiple DIMM vendors and configurations at bus rates up to and including 1333 MT. Because of the range of board layouts and DIMM configurations, Agilent is unable to guarantee compatibility with all DDR3 systems. We recommend that you check compatibility with your system before connecting the logic analyzer to the interposer.

CAUTION **Do not pull on or twist the cables which are attached to the interposer.** The interposer is a precision instrument which should be handled gently. When the interposer is installed, route the cables so that the interposer does not bear the combined weight of the interposer cables and logic analyzer pod cables.

Validating interposer compatibility if your system is working

1. Turn off power to your target system.
2. Install the interposer in your system.

   To connect the interposer to the DDR3 bus, select an available DDR3 slot. Remove the DDR3 DIMM module, if present. Install the DDR3 DIMM module into the 240 pin connector on the top of the Agilent N4835A interposer.
3. Install the DDR3 interposer/DIMM into the target system.

NOTE The target system may not work properly if the interposer is installed into the target system without a DDR3 DIMM installed in the top of the interposer.

4. Apply power to the target and verify that the target functions the same as before with the interposer installed.

Agilent has found that on some marginal targets the interposer causes system failures only in some slots and on some channels. Try the interposer in different slots and on different channels to determine what level of compatibility exists between your target and the interposer.

Agilent has used two different tests for compatibility. If a system is able to boot to an operating system the test for compatibility is to boot to the operating system and then run an application that stresses the memory bus. On other systems an externally loaded memory test has been used to validate compatibility.

Depending upon your need reducing the data rate on the DDR3 bus to 1067MT can often provide compatibility between the interposer and the target when failures occur at 1333 MT.

Validating interposer compatibility if your system is not working

When the target is not functional it is difficult to verify if the interposer will be the cause of future failures. Agilent does not guarantee that the interposer will be compatible in all target systems at 1333 MT. At the time this was written, Agilent has found no system failures at 1067MT. Until the target is functional, Agilent recommends that you restrict the bus rate to 1067MT if possible. The N4835A interposer can capture DDR3 bus activity to help isolate bus signal failures and bus protocol failures.

3 Connecting the DDR3 Interposer to the Logic Analyzer

The Agilent N4835A DDR3 interposer requires four Agilent 16760A cards configured as a single module. This module is normally in slots C-F of the 16900-series logic analysis system.

You may find it easier to connect the logic analyzer cables to the interposer before inserting the interposer into the target system. The Agilent N4835A interposer has fourteen 90 pin pod connections which mate directly to Agilent Logic analyzer cards. Adapter cables are not required. Once a configuration file is loaded refer to the N4835A Probe feature in the Agilent 1690x Overview tab for cable connections.

Following validation of compatibility of the interposer with the target system connect the logic cables to the interposer.

Attaching the logic analyzer cables to the interposer

Attach the cable from each header to a logic analyzer pod, as shown in the following table. This table assumes the logic analyzer cards are in slots C-F.

Header	Pod	Use
Header 1	E1	Control
Header 2	E2	Control
Header 3	F1	Write Data
Header 4	F2	Write Data
Header 5	F3	Write Data
Header 6	F4	Write Data
Header 7	D1	Write Data
Header 8	D2	Write Data
Header 9	D3	Read Data
Header 10	D4	Read Data
Header 11	C1	Read Data
Header 12	C2	Read Data
Header 13	C3	Read Data
Header 14	C4	Write/Control

Using the N4835A Probe tool to see the header-to-pod connections

Once you have loaded a configuration file on the 169xx machine you can find out how to attach the logic analyzer cables to the interposer by going to the workspace and selecting Properties on the N4835A Probe tool icon that appears to the left of DDR3 Module icon.

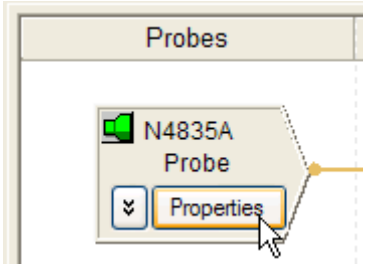


Figure 3 N4835A Probe tool: opening the properties dialog

Once you click on the Properties box a new window will appear showing which analyzer pod attaches to which interposer cable.

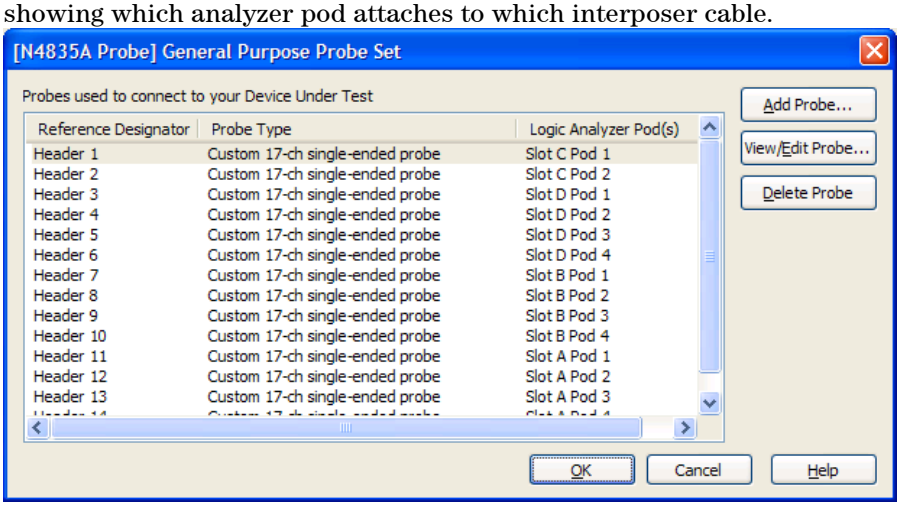


Figure 4 N4835A Probe Set properties dialog

By selecting a line in the N4835A Probe Set and selecting View/Edit Probe ... you can view the mapping between the target signals and the logic analyzer channels.

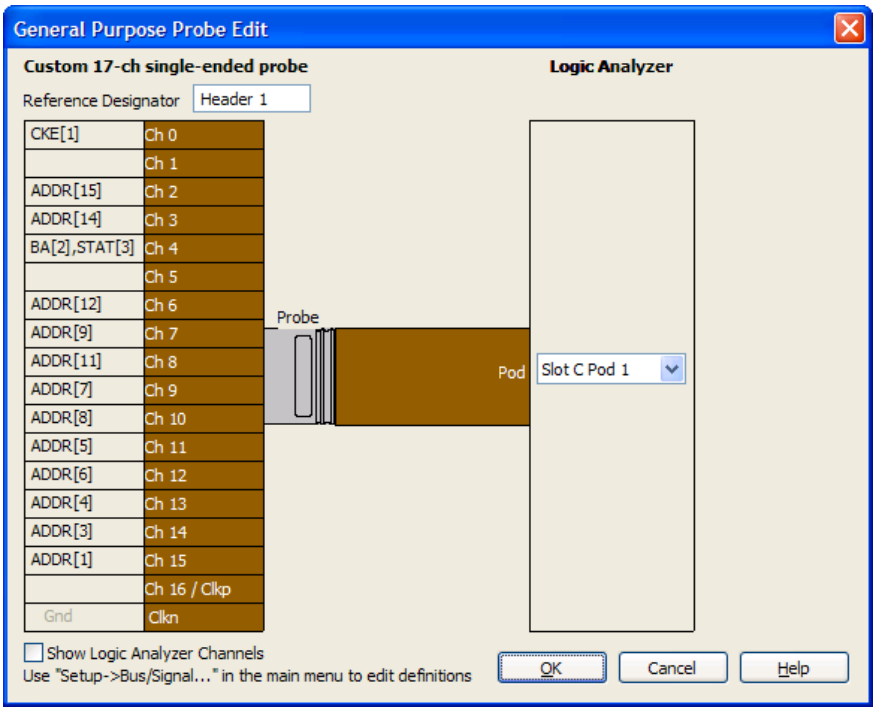


Figure 5 N4835A Probe Set Edit dialog

Connecting to your Target System

To connect the interposer to the DDR3 bus:

1. Turn off power to the target system.
2. Select an available DDR3 slot.
3. Remove the DDR3 DIMM module, if present.
4. Install the DDR3 DIMM module into the 240 pin connector on the top of the Agilent N4835A interposer.
5. Install the DDR3 interposer/DIMM into the target system.

CAUTION **Do not pull on or twist the cables which are attached to the interposer.** The interposer is a precision instrument which should be handled gently. When the interposer is installed, route the cables so that the interposer does not bear the combined weight of the interposer cables and logic analyzer pod cables.

NOTE The target system may not work properly if the interposer is installed into the target system without a DDR3 DIMM installed in the top of the interposer.

Connect the logic analyzer to the headers on the Agilent N4835A interposer, as described in the previous section.

Headers

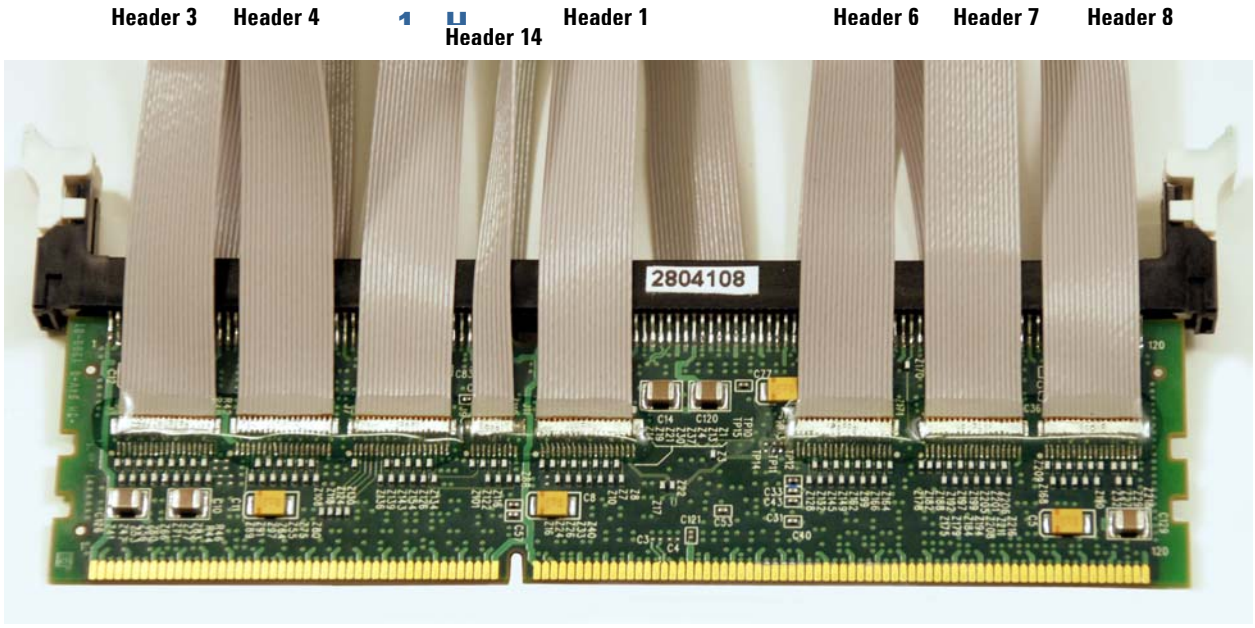


Figure 6 Front side headers

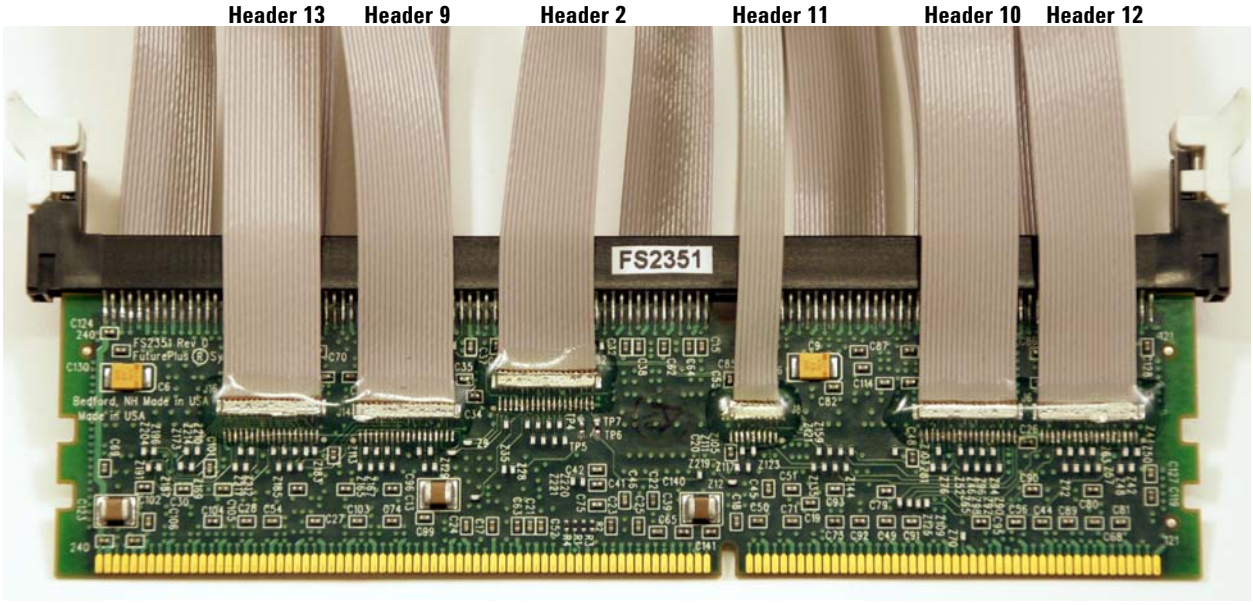


Figure 7 Back side headers

Test Points

There are several test point on the board which you may need to use.

The supplied configuration file assumes that the test points are connected as described below.

TP4 - TP7

The first set of test points are used to select which signals go to the Clk input and the D15 input of Header 2.

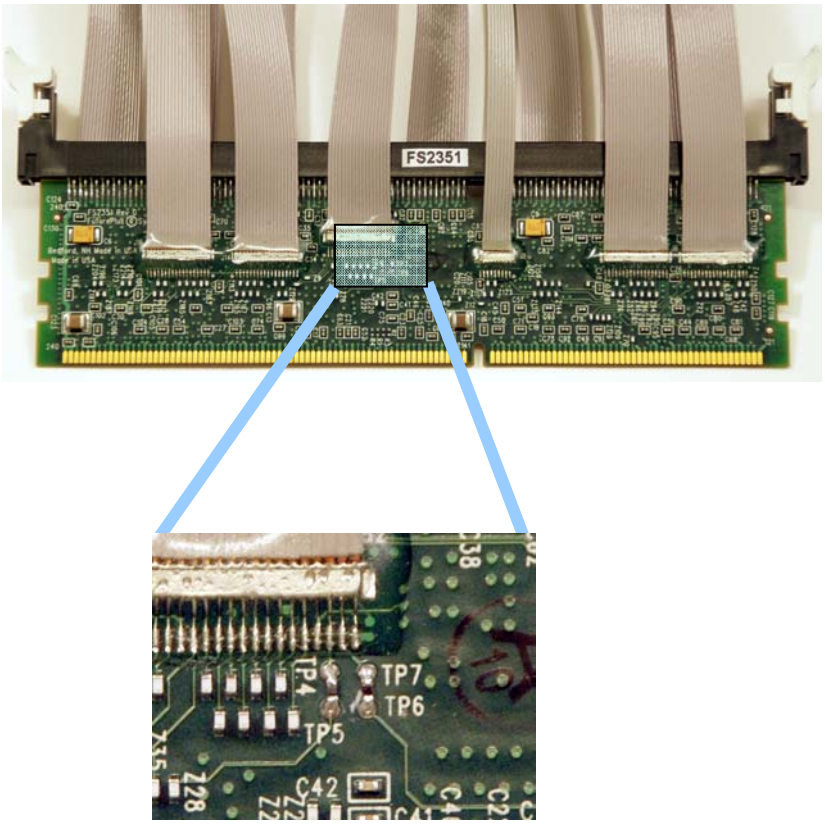


Figure 8 Test points 4, 5, 6, 7

The test points are connected as follows:

TP4: Header 2, signal D15

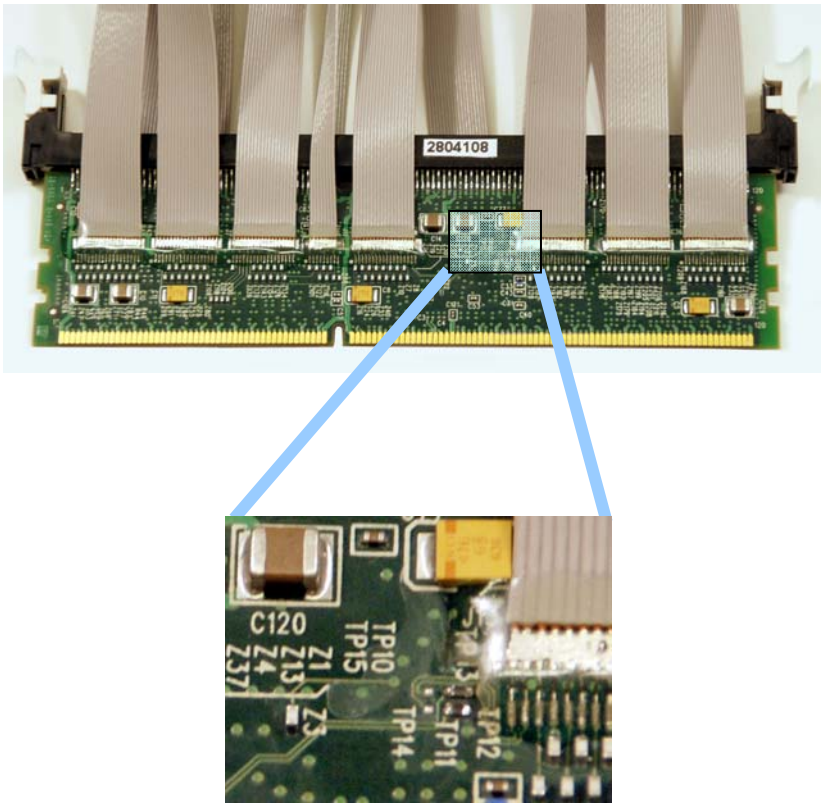
TP5: S0#

TP6: CKE0

TP7: Header 2, Clk

The shipping configuration for the Agilent N4835A is to have CKE0 wired to the Clk input and S0# wired to D15. This is done in the factory by soldering a zero-ohm resistor between TP6 and TP7 and between TP4 and TP5.

TP10-TP15



The test points are connected as follows:

TP10: CK0

TP11: CK0#

TP12: Header 9 Clk

TP13: Header 9 Clk#

TP14: Header 6 Clk

TP15: Header 6 Clk#

A copy of CK0# can be routed to either the Clk input on Header 9 (Read) or Header 6 (Command/Write).

The factory default is CK0# to Header 9 pin 16/17, which is TP10 to TP13 and TP11 to TP12.

To route CK0# to Header 6 connect TP10 to TP15 and TP11 to TP14.

Signal Isolation on the Interposer

All signals sent to the logic analyzer from the Agilent N4835A DDR3 interposer are isolated from the DDR3 DIMM bus by a parallel RC network of 20K ohms and .3 pF. These are placed in a manner to minimize stubs seen by the DIMM bus and to match lengths to the DIMM module so that Data bits and their Strobe/Mask bits are matched to within 20 ps.

The DQ and the CB busses are double probed to provide a read and a write sample of these bits. The probing on these signals consists of a pair of the RC networks in parallel.

The DQS1 and DQS1# signal is also double probed to provide a reference for the read and the write samples in the decoder.

ECC Bits

The ECC bits and their Data Strobe (DQS8) are contained on an extra Header (#14), which will require an additional logic analyzer card in order to probe.

4 Setting Up the Logic Analysis System

Where to find the software

When purchased with a logic analyzer, the application software you ordered is installed and enabled on the instrument hard drive.

If you ordered the application software separately, it is strongly recommended that you download the latest version of the software from the Agilent Web site:

- http://www.agilent.com/find/la-sw-download

To ensure you are notified when new versions are available, sign up for software update notification at:

- http://www.agilent.com/find/emailupdates

Installing the logic analysis system software

The decoder requires version 03.69 or higher of the logic analysis system core software. It is strongly recommended that you download the latest version of the software from the Agilent Web site.

- If you downloaded the software, double-click **SetupLAxxxx.exe** (where xxxx is the version number of the software) then follow the instructions which are displayed.
- If you have a CD, insert the product CD and select **Install Products>Install Agilent Logic Analyzer SetupLAxxxx.exe**, then follow the instructions which are displayed.

Installing the decoder software

- If you downloaded the software, double-click **SetupIASDRAMDDR2DDR3xxxx.exe** then follow the instructions which are displayed.
- If you have a CD, insert the product CD and select **Install Products>Install an Optional Probe>Install Agilent Inverse Assembler for DDR2 & DDR3**, then follow the instructions which are displayed.

The decoder software requires a license before it can be used. Follow the instructions on the Entitlement Certificate to install the license. For more information, go to the Index tab in the online help and click “license.”

Loading a configuration file

You configure the logic analyzer by loading a configuration file. The information in the configuration file includes:

- Signal/bus names and channel assignments for the logic analyzer.
- Tool configuration including logic analyzers, probes, filters, and Listing displays.

One file is provided for the interposer. In most cases, the logic analyzer configuration will be modified to work with your particular DUT, then saved as a custom configuration file.

To load the provided configuration file if the logic analyzer application is not running

1. Check that the interposer is connected to the logic analysis system.
2. Close the logic analyzer window, if it is open.
3. Select Start>All Programs>Agilent Logic Analyzer>SDRAM Default Configs.
4. Click on the N4835ADefault.xml configuration file.
5. When you click on a configuration file, the logic analyzer software will start and configure itself.

When the software has been licensed you are able to load a configuration file. You can access the configuration files by clicking on the folder that was placed on the desktop. When you click on the folder it should open up to display all the configuration files to choose from. If you put your mouse cursor on the name of the file a description will appear telling you what the setup consists of, once you choose the configuration file that is appropriate for your configuration, the 16900 operating system should execute. The protocol decoder automatically loads when the configuration file is loaded. If the decoder does not load, you may load it by selecting tools from the menu bar at the top of the screen and select the decoder from the list.

To load a provided configuration file if the logic analyzer application is running

1. Check that the interposer is connected to the logic analysis system.
2. Select **File>Open...**.
3. Navigate to the configuration file.

   The default location is:

   C:\Documents and Settings\All Users\Documents\Agilent Technologies\Logic Analyzer\Default Configs\Agilent\
4. Select the file and click **Open**.

To save a configuration file

Do not try to overwrite the provided default configuration file. The provided configuration file is read-only.

If you modify the configuration and want to save your work, select **File>Save As...** and save the configuration as an ALA format file.

ALA format configuration files are more complete and efficient than XML format configuration files. See the logic analyzer online help for more information on these formats.

Configuring the logic analysis system

Before you can use the logic analysis system to decode memory bus activity, you must configure it:

1. Load a configuration file.
2. Configure the decoder settings.
3. Set the logic analyzer sampling positions.

NOTE See the online help in the decoder for information on how to configure the decoder and set sampling positions for your target system.

To view the online help for the decoder

Select Help>Help on Tools>Inverse Assembly>DDR Bus Decoder.

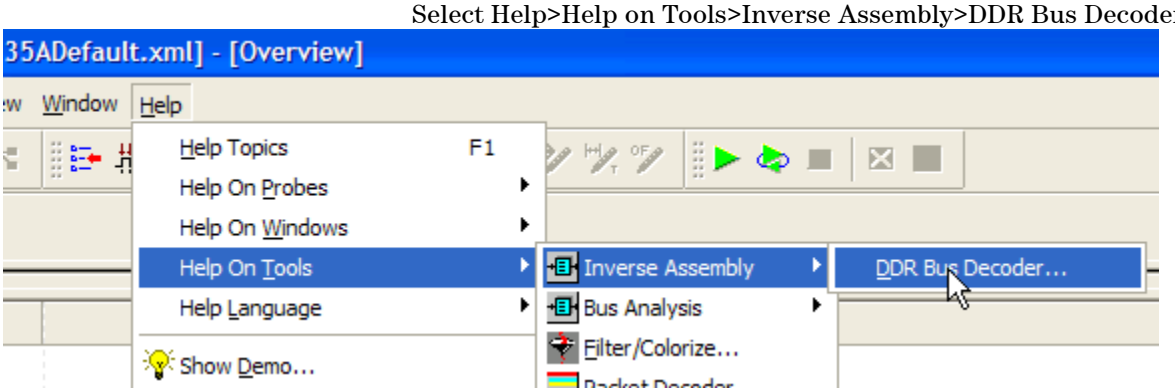


Figure 9 Opening decoder help from the menu bar

To open the decoder properties dialog

- From the Overview display, select **Preferences**.

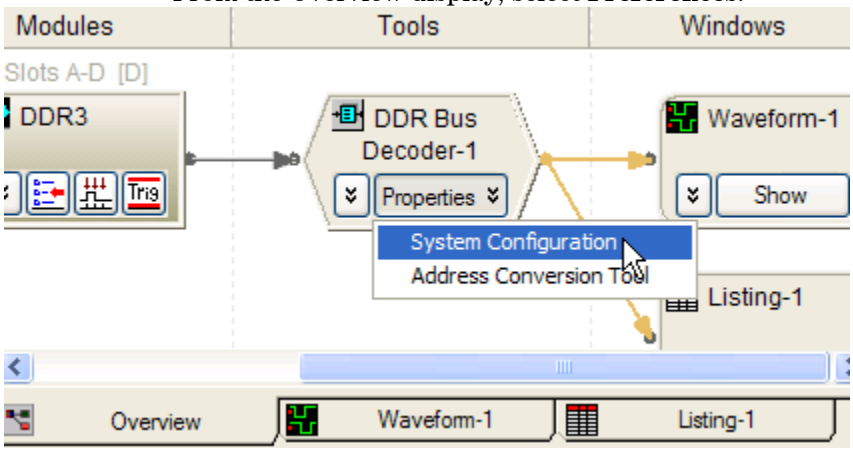


Figure 10 Opening the decoder Properties dialog

Or

- From the menu bar, select Tools>SDRAM Inverse Assembler>System Configuration.

To start the DDR3 eye finder

The DDR3 eye finder is an extension of Agilent's eye finder and eye scan technology. It helps select sample positions for the data signals on the DDR3 bus.

Instructions for using the DDR3 eye finder are in the decoder's online help.

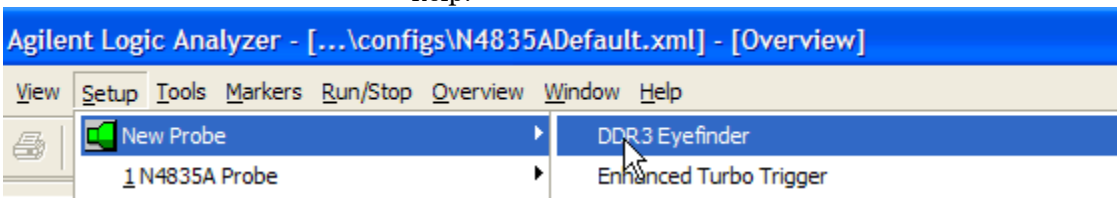


Figure 11 Opening the DDR3 eye finder

Offline analysis

Offline analysis allows you to analyze a trace offline at a PC so it frees up the analyzer for another person to use to capture data.

5 Appendix: Signal Mapping

The following tables show how the Agilent N4835A interposer connects DDR3 DIMM signals to the logic analyzer pods and channels.

The tables here assume four Agilent 16960A logic analyzer cards are set up as one module and loaded into slots C-F in a 16900-series logic analysis system frame.

Header to Pod Connection

Header	C-F Pod	Use
Header 1	E1	Control
Header 2	E2	Control
Header 3	F1	Write Data
Header 4	F2	Write Data
Header 5	F3	Write Data
Header 6	F4	Write Data
Header 7	D1	Write Data
Header 8	D2	Write Data
Header 9	D3	Read Data
Header 10	D4	Read Data
Header 11	C1	Read Data
Header 12	C2	Read Data
Header 13	C3	Read Data
Header 14	C4	Write/Control

Notes on Specific Signals

DM/DQS signals

Some DM and DQS signals share the same pins. The supplied configuration file maps these signals to both the DM_W bus and the DQS bus.

A15/BA3 signals

A15 and BA3 share the same pin (header 1, logic analyzer channel D2). The supplied configuration file assumes A15.

Header 1 - Command

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
Ground	1	2	Ground	
Ground	3	4	NC	
NC	5	6	Ground	
Ground	7	8	D0	**CKE1**
20K ohm to Ground	9	10	Ground	
Ground	11	12	D1	**NC_TEST**
20K ohm to Ground	13	14	Ground	
Ground	15	16	D2	**A15_BA3**
20K ohm to Ground	17	18	Ground	
Ground	19	20	D3	**A14**
20K ohm to Ground	21	22	Ground	
Ground	23	24	D4	**BA2**
20K ohm to Ground	25	26	Ground	
Ground	27	28	D5	**ERR_OUT**
20K ohm to Ground	29	30	Ground	
Ground	31	32	D6	**A12**
20K ohm to Ground	33	34	Ground	
Ground	35	36	D7	**A9**
20K ohm to Ground	37	38	Ground	
Ground	39	40	D8	**A11**
20K ohm to Ground	41	42	Ground	
Ground	43	44	D9	**A7**
20K ohm to Ground	45	46	Ground	
Ground	47	48	D10	**A8**
20K ohm to Ground	49	50	Ground	
Ground	51	52	D11	**A5**

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
20K ohm to Ground	53	54	Ground	
Ground	55	56	D12	**A6**
20K ohm to Ground	57	58	Ground	
Ground	59	60	D13	**A4**
20K ohm to Ground	61	62	Ground	
Ground	63	64	D14	**A3**
20K ohm to Ground	65	66	Ground	
Ground	67	68	D15	**A1**
20K ohm to Ground	69	70	Ground	
Ground	71	72	NC	
NC	73	74	Ground	
Ground	75	76	NC	
NC	77	78	Ground	
Ground	79	80	DP16P/ CLK	**CK0**
CK0N	CLKN 81	82	Ground	
Ground	83	84	NC	
30K ohm to Ground (PID)	85	86	Ground	
Ground	87	88	Ground	
NC	89	90	NC	

Header 2 - Command

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
Ground	1	2	Ground	
Ground	3	4	NC	
NC	5	6	Ground	
Ground	7	8	D0	**ODT1**
20K ohm to Ground	9	10	Ground	
Ground	11	12	D1	**S2n (CS2n)**
20K ohm to Ground	13	14	Ground	
Ground	15	16	D2	**A13**
20K ohm to Ground	17	18	Ground	
Ground	19	20	D3	**S3 (CS3)**
20K ohm to Ground	21	22	Ground	
Ground	23	24	D4	**S1 (CS1)**
20K ohm to Ground	25	26	Ground	
Ground	27	28	D5	**ODT0**
20K ohm to Ground	29	30	Ground	
Ground	31	32	D6	**CAS**
20K ohm to Ground	33	34	Ground	
Ground	35	36	D7	**RAS**
20K ohm to Ground	37	38	Ground	
Ground	39	40	D8	**WE**
20K ohm to Ground	41	42	Ground	
Ground	43	44	D9	**BA1**
20K ohm to Ground	45	46	Ground	
Ground	47	48	D10	**BA0**
20K ohm to Ground	49	50	Ground	
Ground	51	52	D11	**A0**

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
20K ohm to Ground	53	54	Ground	
Ground	55	56	D12	**A10**
20K ohm to Ground	57	58	Ground	
Ground	59	60	D13	**PAR_IN**
20K ohm to Ground	61	62	Ground	
Ground	63	64	D14	**A2**
20K ohm to Ground	65	66	Ground	
Ground	67	68	D15	**S0 (CS0) - TP4**
20K ohm to Ground	69	70	Ground	
Ground	71	72	NC	
NC	73	74	Ground	
Ground	75	76	NC	
NC	77	78	Ground	
Ground	79	80	DP16P/ CLK	**CKE0 - TP7**
20K ohm to Ground	CLKN 81	82	Ground	
Ground	83	84	NC	
30K ohm to Ground (PID)	85	86	Ground	
Ground	87	88	Ground	
NC	89	90	NC	

Header 3 - Write

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
Ground	1	2	Ground	
Ground	3	4	NC	
NC	5	6	Ground	
Ground	7	8	D0	**DQ4**
20K ohm to Ground	9	10	Ground	
Ground	11	12	D1	**DQ0**
20K ohm to Ground	13	14	Ground	
Ground	15	16	D2	**DQ5**
20K ohm to Ground	17	18	Ground	
Ground	19	20	D3	**DQ1**
20K ohm to Ground	21	22	Ground	
Ground	23	24	D4	**DM0_DQS9**
20K ohm to Ground	25	26	Ground	
Ground	27	28	D5	**DQS0n**
20K ohm to Ground	29	30	Ground	
Ground	31	32	D6	**DQS0**
20K ohm to Ground	33	34	Ground	
Ground	35	36	D7	**DQ6**
20K ohm to Ground	37	38	Ground	
Ground	39	40	D8	**DQ2**
20K ohm to Ground	41	42	Ground	
Ground	43	44	D9	**DQ7**
20K ohm to Ground	45	46	Ground	
Ground	47	48	D10	**DQ3**
20K ohm to Ground	49	50	Ground	
Ground	51	52	D11	**DQ12**

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
20K ohm to Ground	53	54	Ground	
Ground	55	56	D12	**DQ8**
20K ohm to Ground	57	58	Ground	
Ground	59	60	D13	**DQ13**
20K ohm to Ground	61	62	Ground	
Ground	63	64	D14	**DQ9**
20K ohm to Ground	65	66	Ground	
Ground	67	68	D15	**DM1_DQS10**
20K ohm to Ground	69	70	Ground	
Ground	71	72	NC	
NC	73	74	Ground	
Ground	75	76	NC	
NC	77	78	Ground	
Ground	79	80	DP16P/ CLK	**DQS1**
DQS1N	CLKN 81	82	Ground	
Ground	83	84	NC	NC
30K ohm to Ground (PID)	85	86	Ground	
Ground	87	88	Ground	
NC	89	90	NC	

Header 4 - Write

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
Ground	1	2	Ground	
Ground	3	4	NC	
NC	5	6	Ground	
Ground	7	8	D0	**VREFDQ**
20K ohm to Ground	9	10	Ground	
Ground	11	12	D1	**VDD**
20K ohm to Ground	13	14	Ground	
Ground	15	16	D2	**DM2_DQS11**
20K ohm to Ground	17	18	Ground	
Ground	19	20	D3	**DQ14**
20K ohm to Ground	21	22	Ground	
Ground	23	24	D4	**DQ10**
20K ohm to Ground	25	26	Ground	
Ground	27	28	D5	**DQ15**
20K ohm to Ground	29	30	Ground	
Ground	31	32	D6	**DQ11**
20K ohm to Ground	33	34	Ground	
Ground	35	36	D7	**DQ20**
20K ohm to Ground	37	38	Ground	
Ground	39	40	D8	**DQ16**
20K ohm to Ground	41	42	Ground	
Ground	43	44	D9	**DQ21**
20K ohm to Ground	45	46	Ground	
Ground	47	48	D10	**DQ17**
20K ohm to Ground	49	50	Ground	
Ground	51	52	D11	**DQS2n**

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
20K ohm to Ground	53	54	Ground	
Ground	55	56	D12	**DQS2**
20K ohm to Ground	57	58	Ground	
Ground	59	60	D13	**DQ22**
20K ohm to Ground	61	62	Ground	
Ground	63	64	D14	**DQ18**
20K ohm to Ground	65	66	Ground	
Ground	67	68	D15	**DQ23**
20K ohm to Ground	69	70	Ground	
Ground	71	72	NC	
NC	73	74	Ground	
Ground	75	76	NC	
NC	77	78	Ground	
Ground	79	80	DP16P/ CLK	**No connection**
Ground	CLKN 81	82	Ground	
Ground	83	84	NC	
30K ohm to Ground (PID)	85	86	Ground	
Ground	87	88	Ground	
NC	89	90	NC	

Header 5 - Write

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
Ground	1	2	Ground	
Ground	3	4	NC	
NC	5	6	Ground	
Ground	7	8	D0	**DQ19**
20K ohm to Ground	9	10	Ground	
Ground	11	12	D1	**DQ28**
20K ohm to Ground	13	14	Ground	
Ground	15	16	D2	**DQ24**
20K ohm to Ground	17	18	Ground	
Ground	19	20	D3	**DQ29**
20K ohm to Ground	21	22	Ground	
Ground	23	24	D4	**DQ25**
20K ohm to Ground	25	26	Ground	
Ground	27	28	D5	**DM3_DQS12**
20K ohm to Ground	29	30	Ground	
Ground	31	32	D6	**DQS3n**
20K ohm to Ground	33	34	Ground	
Ground	35	36	D7	**DQS3**
20K ohm to Ground	37	38	Ground	
Ground	39	40	D8	**DQ30**
20K ohm to Ground	41	42	Ground	
Ground	43	44	D9	**DQ26**
20K ohm to Ground	45	46	Ground	
Ground	47	48	D10	**DQ31**
20K ohm to Ground	49	50	Ground	

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
Ground	51	52	D11	**DQ27**
20K ohm to Ground	53	54	Ground	
Ground	55	56	D12	**CB4**
20K ohm to Ground	57	58	Ground	
Ground	59	60	D13	**CB0**
20K ohm to Ground	61	62	Ground	
Ground	63	64	D14	**CB5**
20K ohm to Ground	65	66	Ground	
Ground	67	68	D15	**RESET**
20K ohm to Ground	69	70	Ground	
Ground	71	72	NC	
NC	73	74	Ground	
Ground	75	76	NC	
NC	77	78	Ground	
Ground	79	80	DP16P/ CLK	**CLK1**
CLK1N	CLKN 81	82	Ground	
Ground	83	84	NC	
30K ohm to Ground (PID)	85	86	Ground	
Ground	87	88	Ground	
NC	89	90	NC	

Header 6 – Write

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
Ground	1	2	Ground	
Ground	3	4	NC	
NC	5	6	Ground	
Ground	7	8	D0	**DM5_DQS14**
20K ohm to Ground	9	10	Ground	
Ground	11	12	D1	**DQ41**
20K ohm to Ground	13	14	Ground	
Ground	15	16	D2	**DQ45**
20K ohm to Ground	17	18	Ground	
Ground	19	20	D3	**DQ40**
20K ohm to Ground	21	22	Ground	
Ground	23	24	D4	**DQ44**
20K ohm to Ground	25	26	Ground	
Ground	27	28	D5	**DQ35**
20K ohm to Ground	29	30	Ground	
Ground	31	32	D6	**DQ39**
20K ohm to Ground	33	34	Ground	
Ground	35	36	D7	**DQ34**
20K ohm to Ground	37	38	Ground	
Ground	39	40	D8	**DQ38**
20K ohm to Ground	41	42	Ground	
Ground	43	44	D9	**DQS4**
20K ohm to Ground	45	46	Ground	
Ground	47	48	D10	**DQS4N**
20K ohm to Ground	49	50	Ground	
Ground	51	52	D11	**DM4_DQS13**

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
20K ohm to Ground	53	54	Ground	
Ground	55	56	D12	**DQ33**
20K ohm to Ground	57	58	Ground	
Ground	59	60	D13	**DQ37**
20K ohm to Ground	61	62	Ground	
Ground	63	64	D14	**DQ32**
20K ohm to Ground	65	66	Ground	
Ground	67	68	D15	**DQ36**
20K ohm to Ground	69	70	Ground	
Ground	71	72	NC	
NC	73	74	Ground	
Ground	75	76	NC	
NC	77	78	Ground	
Ground	79	80	DP16P/ CLK	**TP15**
TP14	CLKN 81	82	Ground	
Ground	83	84	NC	
30K ohm to Ground (PID)	85	86	Ground	
Ground	87	88	Ground	
NC	89	90	NC	

Header 7 -Write

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
Ground	1	2	Ground	
Ground	3	4	NC	
NC	5	6	Ground	
Ground	7	8	D0	**DQS5**
20K ohm to Ground	9	10	Ground	
Ground	11	12	D1	**DQ46**
20K ohm to Ground	13	14	Ground	
Ground	15	16	D2	**DQ42**
20K ohm to Ground	17	18	Ground	
Ground	19	20	D3	**DQ47**
20K ohm to Ground	21	22	Ground	
Ground	23	24	D4	**DQ43**
20K ohm to Ground	25	26	Ground	
Ground	27	28	D5	**DQ52**
20K ohm to Ground	29	30	Ground	
Ground	31	32	D6	**DQ48**
20K ohm to Ground	33	34	Ground	
Ground	35	36	D7	**DQ53**
20K ohm to Ground	37	38	Ground	
Ground	39	40	D8	**DQ49**
20K ohm to Ground	41	42	Ground	
Ground	43	44	D9	**DM6_DQS15**
20K ohm to Ground	45	46	Ground	
Ground	47	48	D10	**DQS6n**

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
20K ohm to Ground	49	50	Ground	
Ground	51	52	D11	**DQS6**
20K ohm to Ground	53	54	Ground	
Ground	55	56	D12	**DQ54**
20K ohm to Ground	57	58	Ground	
Ground	59	60	D13	**DQ50**
20K ohm to Ground	61	62	Ground	
Ground	63	64	D14	**DQ55**
20K ohm to Ground	65	66	Ground	
Ground	67	68	D15	**DQ51**
20K ohm to Ground	69	70	Ground	
Ground	71	72	NC	
NC	73	74	Ground	
Ground	75	76	NC	
NC	77	78	Ground	
Ground	79	80	DP16P/ CLK	**DQS5N**
Ground	CLKN 81	82	Ground	
Ground	83	84	NC	
30K ohm to Ground (PID)	85	86	Ground	
Ground	87	88	Ground	
NC	89	90	NC	

Header 8 - Write

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
Ground	1	2	Ground	
Ground	3	4	NC	
NC	5	6	Ground	
Ground	7	8	D0	**DQ60**
20K ohm to Ground	9	10	Ground	
Ground	11	12	D1	**DQ56**
20K ohm to Ground	13	14	Ground	
Ground	15	16	D2	**DQ61**
20K ohm to Ground	17	18	Ground	
Ground	19	20	D3	**DQ57**
20K ohm to Ground	21	22	Ground	
Ground	23	24	D4	**DM7_DQS16**
20K ohm to Ground	25	26	Ground	
Ground	27	28	D5	**DQS7n**
20K ohm to Ground	29	30	Ground	
Ground	31	32	D6	**DQS7**
20K ohm to Ground	33	34	Ground	
Ground	35	36	D7	**DQ62**
20K ohm to Ground	37	38	Ground	
Ground	39	40	D8	**DQ58**
20K ohm to Ground	41	42	Ground	
Ground	43	44	D9	**DQ63**
20K ohm to Ground	45	46	Ground	
Ground	47	48	D10	**DQ59**

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
20K ohm to Ground	49	50	Ground	
Ground	51	52	D11	**No connection**
20K ohm to Ground	53	54	Ground	
Ground	55	56	D12	**SA0**
20K ohm to Ground	57	58	Ground	
Ground	59	60	D13	**SA1**
20K ohm to Ground	61	62	Ground	
Ground	63	64	D14	**SDA**
20K ohm to Ground	65	66	Ground	
Ground	67	68	D15	**SCL**
20K ohm to Ground	69	70	Ground	
Ground	71	72	NC	
NC	73	74	Ground	
Ground	75	76	NC	
NC	77	78	Ground	
Ground	79	80	DP16P/ CLK	**SA2**
Ground	CLKN 81	82	Ground	
Ground	83	84	NC	
30K ohm to Ground (PID)	85	86	Ground	
Ground	87	88	Ground	
NC	89	90	NC	

Header 9 – Read Duplicates - only data signals

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
Ground	1	2	Ground	
Ground	3	4	NC	
NC	5	6	Ground	
Ground	7	8	D0	**DQ41**
20K ohm to Ground	9	10	Ground	
Ground	11	12	D1	**DQ45**
20K ohm to Ground	13	14	Ground	
Ground	15	16	D2	**DQ40**
20K ohm to Ground	17	18	Ground	
Ground	19	20	D3	**DQ44**
20K ohm to Ground	21	22	Ground	
Ground	23	24	D4	**DQ35**
20K ohm to Ground	25	26	Ground	
Ground	27	28	D5	**DQ39**
20K ohm to Ground	29	30	Ground	
Ground	31	32	D6	**DQ34**
20K ohm to Ground	33	34	Ground	
Ground	35	36	D7	**DQ38**
20K ohm to Ground	37	38	Ground	
Ground	39	40	D8	**DQ43**
20K ohm to Ground	41	42	Ground	
Ground	43	44	D9	**DQ47**
20K ohm to Ground	45	46	Ground	
Ground	47	48	D10	**DQ42**
20K ohm to Ground	49	50	Ground	
Ground	51	52	D11	**DQ33**

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
20K ohm to Ground	53	54	Ground	
Ground	55	56	D12	**DQ37**
20K ohm to Ground	57	58	Ground	
Ground	59	60	D13	**DQ32**
20K ohm to Ground	61	62	Ground	
Ground	63	64	D14	**DQ36**
20K ohm to Ground	65	66	Ground	
Ground	67	68	D15	**RAS**
20K ohm to Ground	69	70	Ground	
Ground	71	72	NC	
NC	73	74	Ground	
Ground	75	76	NC	
NC	77	78	Ground	
Ground	79	80	DP16P/ CLK	**TP13 – CK0**
TP14 – CK0N	CLKN 81	82	Ground	
Ground	83	84	NC	
30K ohm to Ground (PID)	85	86	Ground	
Ground	87	88	Ground	
NC	89	90	NC	

Header 10 - Read Duplicates - only data signals

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
Ground	1	2	Ground	
Ground	3	4	NC	
NC	5	6	Ground	
Ground	7	8	D0	**DQ25**
20K ohm to Ground	9	10	Ground	
Ground	11	12	D1	**DQ27**
20K ohm to Ground	13	14	Ground	
Ground	15	16	D2	**DQ26**
20K ohm to Ground	17	18	Ground	
Ground	19	20	D3	**DQ14**
20K ohm to Ground	21	22	Ground	
Ground	23	24	D4	**DQ10**
20K ohm to Ground	25	26	Ground	
Ground	27	28	D5	**DQ15**
20K ohm to Ground	29	30	Ground	
Ground	31	32	D6	**DQ11**
20K ohm to Ground	33	34	Ground	
Ground	35	36	D7	**DQ20**
20K ohm to Ground	37	38	Ground	
Ground	39	40	D8	**DQ16**
20K ohm to Ground	41	42	Ground	
Ground	43	44	D9	**DQ21**
20K ohm to Ground	45	46	Ground	
Ground	47	48	D10	**DQ17**
20K ohm to Ground	49	50	Ground	

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
Ground	51	52	D11	**DQ31**
20K ohm to Ground	53	54	Ground	
Ground	55	56	D12	**DQ30**
20K ohm to Ground	57	58	Ground	
Ground	59	60	D13	**DQ22**
20K ohm to Ground	61	62	Ground	
Ground	63	64	D14	**DQ18**
20K ohm to Ground	65	66	Ground	
Ground	67	68	D15	**DQ23**
20K ohm to Ground	69	70	Ground	
Ground	71	72	NC	
NC	73	74	Ground	
Ground	75	76	NC	
NC	77	78	Ground	
Ground	79	80	DP16P/ CLK	**DQ19**
20K ohm to Ground	CLKN 81	82	Ground	
Ground	83	84	NC	
30K ohm to Ground (PID)	85	86	Ground	
Ground	87	88	Ground	
NC	89	90	NC	

Header 11 – Read Duplicates - only data (CB) signals

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
Ground	1	2	Ground	
Ground	3	4	NC	
NC	5	6	Ground	
Ground	7	8	D0	**CB5**
20K ohm to Ground	9	10	Ground	
Ground	11	12	D1	**CB1**
20K ohm to Ground	13	14	Ground	
Ground	15	16	D2	**CB0**
20K ohm to Ground	17	18	Ground	
Ground	19	20	D3	**CB4**
20K ohm to Ground	21	22	Ground	
Ground	23	24	D4	**CB6**
20K ohm to Ground	25	26	Ground	
Ground	27	28	D5	**CB2**
20K ohm to Ground	29	30	Ground	
Ground	31	32	D6	**CB7**
20K ohm to Ground	33	34	Ground	
Ground	35	36	D7	**CB3**
20K ohm to Ground	37	38	Ground	
Ground	39	40	D8	
20K ohm to Ground	41	42	Ground	
Ground	43	44	D9	
20K ohm to Ground	45	46	Ground	
Ground	47	48	D10	
20K ohm to Ground	49	50	Ground	
Ground	51	52	D11	

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
20K ohm to Ground	53	54	Ground	
Ground	55	56	D12	
20K ohm to Ground	57	58	Ground	
Ground	59	60	D13	
20K ohm to Ground	61	62	Ground	
Ground	63	64	D14	
20K ohm to Ground	65	66	Ground	
Ground	67	68	D15	
20K ohm to Ground	69	70	Ground	
Ground	71	72	NC	
NC	73	74	Ground	
Ground	75	76	NC	
NC	77	78	Ground	
Ground	79	80	DP16P/ CLK	
20K ohm to Ground	CLKN 81	82	Ground	
Ground	83	84	NC	
30K ohm to Ground (PID)	85	86	Ground	
Ground	87	88	Ground	
NC	89	90	NC	

Header 12 – Read – Duplicates - only data signals

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
Ground	1	2	Ground	
Ground	3	4	NC	
NC	5	6	Ground	
Ground	7	8	D0	DQ4
20K ohm to Ground	9	10	Ground	
Ground	11	12	D1	DQ0
20K ohm to Ground	13	14	Ground	
Ground	15	16	D2	DQ5
20K ohm to Ground	17	18	Ground	
Ground	19	20	D3	DQ1
20K ohm to Ground	21	22	Ground	
Ground	23	24	D4	No connection
20K ohm to Ground	25	26	Ground	
Ground	27	28	D5	No connection
20K ohm to Ground	29	30	Ground	
Ground	31	32	D6	DQ28
20K ohm to Ground	33	34	Ground	
Ground	35	36	D7	DQ6
20K ohm to Ground	37	38	Ground	
Ground	39	40	D8	DQ2
20K ohm to Ground	41	42	Ground	
Ground	43	44	D9	DQ7
20K ohm to Ground	45	46	Ground	
Ground	47	48	D10	DQ3
20K ohm to Ground	49	50	Ground	
Ground	51	52	D11	DQ12

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
20K ohm to Ground	53	54	Ground	
Ground	55	56	D12	DQ8
20K ohm to Ground	57	58	Ground	
Ground	59	60	D13	DQ13
20K ohm to Ground	61	62	Ground	
Ground	63	64	D14	DQ9
20K ohm to Ground	65	66	Ground	
Ground	67	68	D15	DQ24
20K ohm to Ground	69	70	Ground	
Ground	71	72	NC	
NC	73	74	Ground	
Ground	75	76	NC	
NC	77	78	Ground	
Ground	79	80	DP16P/ CLK	DQ29
20K ohm to Ground	CLKN 81	82	Ground	
Ground	83	84	NC	
30K ohm to Ground (PID)	85	86	Ground	
Ground	87	88	Ground	
NC	89	90	NC	

Header 13 – Read Duplicates - only data signals

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
Ground	1	2	Ground	
Ground	3	4	NC	
NC	5	6	Ground	
Ground	7	8	D0	**DQ56**
20K ohm to Ground	9	10	Ground	
Ground	11	12	D1	**DQ46**
20K ohm to Ground	13	14	Ground	
Ground	15	16	D2	**DQ60**
20K ohm to Ground	17	18	Ground	
Ground	19	20	D3	**DQ57**
20K ohm to Ground	21	22	Ground	
Ground	23	24	D4	**DQ61**
20K ohm to Ground	25	26	Ground	
Ground	27	28	D5	**DQ52**
20K ohm to Ground	29	30	Ground	
Ground	31	32	D6	**DQ48**
20K ohm to Ground	33	34	Ground	
Ground	35	36	D7	**DQ53**
20K ohm to Ground	37	38	Ground	
Ground	39	40	D8	**DQ49**
20K ohm to Ground	41	42	Ground	
Ground	43	44	D9	**DQ62**
20K ohm to Ground	45	46	Ground	
Ground	47	48	D10	**DQ58**
20K ohm to Ground	49	50	Ground	
Ground	51	52	D11	**DQ63**

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
20K ohm to Ground	53	54	Ground	
Ground	55	56	D12	**DQ54**
20K ohm to Ground	57	58	Ground	
Ground	59	60	D13	**DQ50**
20K ohm to Ground	61	62	Ground	
Ground	63	64	D14	**DQ55**
20K ohm to Ground	65	66	Ground	
Ground	67	68	D15	**DQ51**
20K ohm to Ground	69	70	Ground	
Ground	71	72	NC	
NC	73	74	Ground	
Ground	75	76	NC	
NC	77	78	Ground	
Ground	79	80	DP16P/ CLK	**DQ59**
20K ohm to Ground	CLKN 81	82	Ground	
Ground	83	84	NC	
30K ohm to Ground (PID)	85	86	Ground	
Ground	87	88	Ground	
NC	89	90	NC	

Header 14 – ECC bits

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
Ground	1	2	Ground	
Ground	3	4	NC	
NC	5	6	Ground	
Ground	7	8	D0	**DM8_DQS17**
20K ohm to Ground	9	10	Ground	
Ground	11	12	D1	**CB1**
20K ohm to Ground	13	14	Ground	
Ground	15	16	D2	**DQS8n**
20K ohm to Ground	17	18	Ground	
Ground	19	20	D3	**DQS8**
20K ohm to Ground	21	22	Ground	
Ground	23	24	D4	**CB6**
20K ohm to Ground	25	26	Ground	
Ground	27	28	D5	**CB2**
20K ohm to Ground	29	30	Ground	
Ground	31	32	D6	**CB7**
20K ohm to Ground	33	34	Ground	
Ground	35	36	D7	**CB3**
20K ohm to Ground	37	38	Ground	
Ground	39	40	D8	**No connection**
20K ohm to Ground	41	42	Ground	
Ground	43	44	D9	**No connection**
20K ohm to Ground	45	46	Ground	
Ground	47	48	D10	**No connection**
20K ohm to Ground	49	50	Ground	
Ground	51	52	D11	**No connection**

Signal connection	SAMTEC Pin number	SAMTEC Pin number	Logic Analyzer channel number	Signal name
20K ohm to Ground	53	54	Ground	
Ground	55	56	D12	**No connection**
20K ohm to Ground	57	58	Ground	
Ground	59	60	D13	**No connection**
20K ohm to Ground	61	62	Ground	
Ground	63	64	D14	**No connection**
20K ohm to Ground	65	66	Ground	
Ground	67	68	D15	**No connection**
20K ohm to Ground	69	70	Ground	
Ground	71	72	NC	
NC	73	74	Ground	
Ground	75	76	NC	
NC	77	78	Ground	
Ground	79	80	DP16P/ CLK	**No connection**
Ground	CLKN 81	82	Ground	
Ground	83	84	NC	
30K ohm to Ground (PID)	85	86	Ground	
Ground	87	88	Ground	
NC	89	90	NC	

6 Characteristics, Regulatory, and Safety Information

Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics.

Table 1 Environmental Characteristics (Operating)

Temperature	20° to + 30° C (+68° to +86° F)
Altitude	4,600 m (15,000 ft)
Humidity	Up to 50% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation on the circuit board. For indoor use only.

Table 2 Inputs and Outputs

To interposer	Memory bus signals from target system
From interposer	High-density connectors for Agilent logic analyzer cards in an Agilent 16900-series logic analysis system.

Safety Notices

This apparatus has been designed and tested in accordance with IEC Publication 61010-1, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warnings

Use only the recommended power supply.

If you energize this instrument by an auto transformer (for voltage reduction or mains isolation), the common terminal must be connected to the earth terminal of the power source.

Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.

Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do not install substitute parts or perform any unauthorized modification to the instrument.

Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.

Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

Do not use the instrument in a manner not specified by the manufacturer.

To clean the instrument

Do not attempt to clean this product.

Safety Symbols

"Caution" or "Warning" risk of danger marked on product. See"Safety Notices" on page 2 and refer to this manual for a description of the specific danger.

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

Regulatory Notices

WEEE Compliance

This product complies with the WEEE Directive (2002/96/EC) marking requirements. The affixed label indicates that you must not discard this electrical/electronic product in domestic household waste.

Product Category: With reference to the equipment types in the WEEE Directive Annex I, this product is classed as a "Monitoring and Control Instrumentation" product.

Do not dispose in domestic household waste.

To return unwanted products, contact your local Agilent office, or see www.agilent.com for more information.

China RoHS

夹层转换板 Interposer

部件名称 Part Name	有毒有害物质或元素 Toxic or Hazardous Substances and Elements					
	铅 Pb	汞 Hg	镉 Cd	六价铬 CrVI	多溴联苯 PBB	多溴二苯醚 PBDE
金属扣件 Metal fasteners	O	O	O	X	O	O
印制电路板 Printed circuit assemblies	X	O	O	O	O	O
电缆和探头 Cables and probes	X	O	O	O	O	O
电缆 Cables	X	O	O	O	O	O
连接器 Connectors	X	O	O	O	O	O
机械部件 Machined parts	X	O	O	O	O	O
其它部件 Other parts	O	O	O	O	O	O

O: 表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T11363-2006 标准规定的限量要求以下。

X: 表示该有毒有害物质至少在该部件某一均质材料中的含量超出SJ/T11363-2006 标准规定的限量要求。

O: Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement in SJ/T11363-2006.

X: Indicates that this toxic or hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement in SJ/T11363-2006.

如果上述表单多于一个，请参考您的订单或者装箱单从上述表格中找到适合您的产品的列表。

If more than one table is shown above, reference your order or packing list to determine which is applicable to your product.