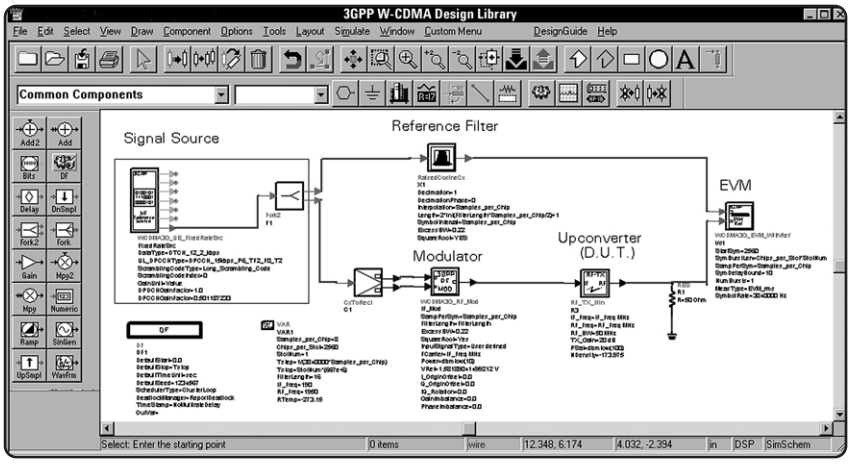
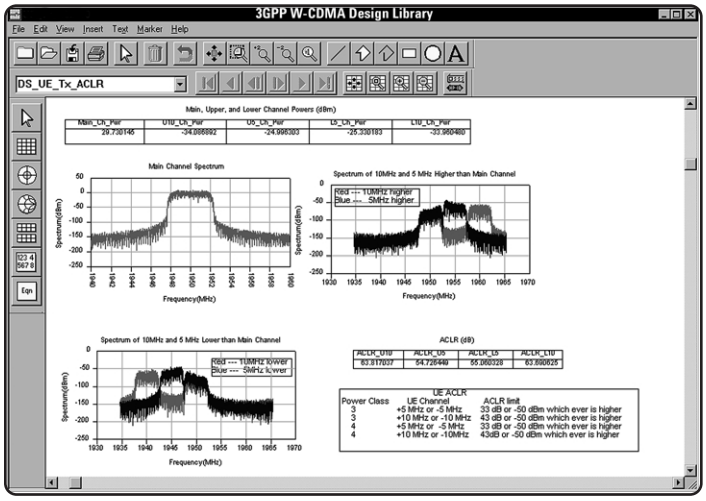
Agilent E8875A/AN
3GPP FDD W-CDMA Design Library
Product Overview





Incorporating the 3GPP FDD W-CDMA Design Library into your design flow:

- **Jump-starts your 3GPP FDD W-CDMA design activities**
- **Enables you to evaluate your designs against the 3GPP FDD W-CDMA transmitter and receiver specifications for measurements such as ACLR, EVM, and BER**
- **Verifies your 3GPP FDD W-CDMA design performance throughout the design and prototyping phase using links to the Agilent ESG-D RF digital signal generator**
- **Shortens your time to market and helps you to achieve first-pass success**

The Third Generation Partnership Project (3GPP) Frequency Division Duplexing (FDD) Wideband Code Division Multiple Access (W-CDMA) Design Library enables you to develop and helps you to evaluate designs against the 3GPP W-CDMA Frequency Division Duplex (FDD) specifications. The 3GPP FDD W-CDMA Design Library contains baseband functionality such as framing, encoding, interleaving, and spreading to model the physical channel in the 3GPP FDD W-CDMA system.

Pre-configured Test and Verification (T&V) designs help you to evaluate your designs against many of the transmitter and receiver tests specified in the 3GPP TS 25.101, TS 25.104, TS 34.121, and TS 25.141 FDD W-CDMA technical specifications. In addition, pre-configured source designs provide standard channel configurations similar to the Agilent ESG-D RF digital signal generator for design verification throughout the prototyping phase.

The 3GPP FDD W-CDMA Design Library is suited for rapid, parallel design cycles that require baseband functionality to start RF, system, and circuit designs before the DSP designs are completed. This library enables you to jump-start your RF, system, and circuit designs using a working baseline before replacing the design library elements with actual DSP designs.

Agilent Technologies

A Comprehensive Design Environment for System, Circuit, and DSP Designs

The 3GPP FDD W-CDMA Design Library is a companion product to Advanced Design System (ADS), a versatile design tool from Agilent EEsof EDA that gives you access to a wide array of RF, analog, and DSP models and simulation capability. Using the design library with ADS enables you to create 3GPP FDD W-CDMA system designs with various levels of abstraction. You can generate a system design by using the behavioral models from the design library and perform system-level tradeoffs and requirements partitioning. The behavioral models can later be replaced with detailed RF/analog circuit designs or DSP designs to determine how they affect the overall system performance.

The 3GPP FDD W-CDMA Design Library is particularly useful for RF engineers. User equipment (UE) and base station (BS) Test and Verification (T&V) designs are pre-configured to help evaluate RF and system designs against the 3GPP FDD W-CDMA specifications. There are T&V designs for evaluating Adjacent-Channel Leakage Ratio (ACLR), Error Vector Magnitude (EVM), Bit Error Rate (BER), and other measurements.

DSP engineers can use the 3GPP FDD W-CDMA baseband elements as an ideal baseline before replacing the baseband elements with their own designs. The baseband elements can be replaced by proprietary algorithms written in C++ or with hardware and software implementations written in HDL and ISS. The C-code model builder, HDL co-simulation, and ISS co-simulation capabilities within ADS allow new designs or existing intellectual property to be functionally verified at the top level with a mixed level of abstraction.

System engineers can take advantage of the ADS links to Agilent test equipment to deliver powerful capability in virtual testing of prototype hardware throughout the design cycle. For example, the ADS link to the ESG-D RF digital signal generator can create real-world signals at any point in the modeled-system design to reflect impairments introduced by the preceding elements. This link lets you evaluate prototype hardware on the bench, using simulation models to supplement sections of the design, which have not yet been fabricated. This unique capability allows you to verify your design performance throughout the design cycle, lowering the risk and reducing the number of design iterations.

The 3GPP FDD W-CDMA Design Library, integrated with the versatile ADS design environment, delivers powerful 3GPP FDD W-CDMA design capability, whether you are modeling RF, DSP, or entire system designs. Design verification using circuit co-simulation, HDL co-simulation, ISS co-simulation, and our unique links to Agilent instrumentation increases your chances of first-time success. It also reduces time to market by allowing system engineers to partition 3GPP FDD W-CDMA design requirements and verify design performance throughout the development cycle.

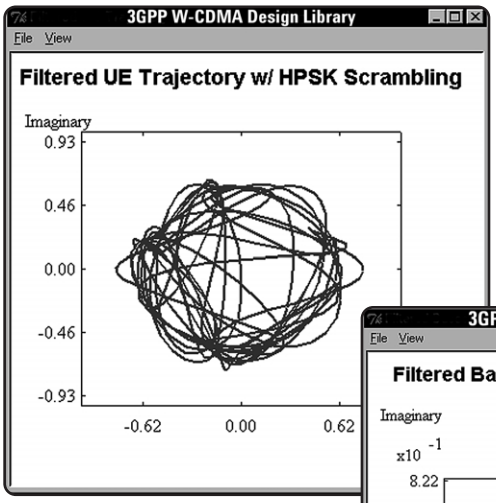


Fig. 3 – Filtered Trajectory of User Equipment (UE) with HPSK Scrambling.

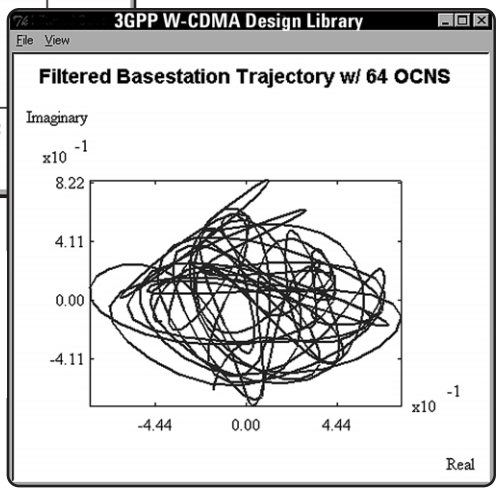


Fig. 4 – Filtered Trajectory of Basestation Test Model Source with 64 OCNS Interferers.

Pre-Built Algorithmic Models

- User Equipment and Base Station Configurable Sources
- Base Station Test Models
- Rate 1/2 and 1/3 Convolutional Coding
- Rate 1/3 Turbo Coding
- Interleaving/De-Interleaving
- Rate Matching and Multiplexing
- 4/8/16/32/64/128/256/512 Orthogonal Variable Spreading Factors (OVSF)
- Hybrid Phase-Shift Keying (HPSK) Complex Scrambling
- 12.2/64/144/384/2048 kbps Data Rates
- Physical Channel Mapping and Multiplexing
- Multiple-Code Channels
- Transport Format Channel Indicator (TFCI)
- Six-Finger Rake Receiver

System Measurements

- Coded or Uncoded Bit Error Rate (BER)
- Block Error Rate (BLER)
- Error Vector Magnitude (EVM)
- Adjacent-Channel Leakage Ratio (ACLR)
- Complimentary Cumulative Distribution Function (CCDF)
- Peak Code Domain Error

The 3GPP FDD W-CDMA Design Models LIbrary The Physical Layer

The 3GPP FDD W-CDMA Design Library models the physical layer, including data and control logical channels, frame segmenting and multiplexing forming the coded-composite transport channel, and the multiplexing for the dedicated physical data and control channels. Multiple transport channels are multiplexed together for transmission onto one physical channel. OVSF codes with multiple spreading factors are used to support multiple data rates, and HPSK modulation is used for uplink scrambling to reduce the peak-to-average ratio. The library also includes a six-finger RAKE receiver to improve reception in cases where the delay spreads are significant.

3GPP FDD W-CDMA supports a flexible structure that accommodates services of various bit rates, ranging from voice to high-data rate applications. The logical channel receives data and control bits from the selected service and adds CRC bits to detect reception errors at the receiver. Rate 1/2 or rate 1/3 convolutional encoding is performed at lower data rates, and turbo encoding is used to improve performance at high-data rates. These behavioral models can be used as a starting point for your designs to provide the baseband functionality needed to evaluate your RF, system, and DSP designs.

3GPP FDD W-CDMA Design Library Specifications

Data Rates

Variable Rate	DCH 8/16/32/64/128/256/512 kbps
Fixed Rate	DCCH 2.4 kbps
	DTCH 12.2/64/144/384/2048 kbps

Physical-Channel Mapping and Multiplexing

DPCH (downlink) 30/60/240/480/960/1920 kbps
DPDCH (uplink) 30/60/240/480/960 kbps
Both support multiple channels

Modulation, Spreading, and Scrambling

QPSK (downlink), BPSK (uplink)
OVSF spreading codes, SF=4/8/16/32/64/128/256/512
Scrambling: Gold codes, HPSK for uplink

Error Correction Rate 1/2 or 1/3 convolutional encoding or turbo encoding

Diversity Six-finger RAKE receiver

User Equipment and Base Station Test and Verification Projects

User equipment (UE) and base station (BS) Test and Verification (T&V) designs help evaluate designs against many of the transmitter and receiver tests outlined in the 3GPP FDD W-CDMA specifications TS 34.121 (UE) and TS 25.141 (BS). Hierarchical designs provide easy-to-use source and demodulation capability with integrated circuit co-simulation.
Data displays are pre-configured with measurements such as ACLR, spectral masks, and peak code domain error. Bit Error Rate (BER) simulations are set up for stand-alone sensitivity measurements or with CW and Orthogonal Complex Noise Simulator (OCNS) interferers present. These T&V designs can be used to evaluate circuit or system designs in the design phase, as well as to demonstrate the 3GPP FDD W-CDMA performance of your designs to your customers.

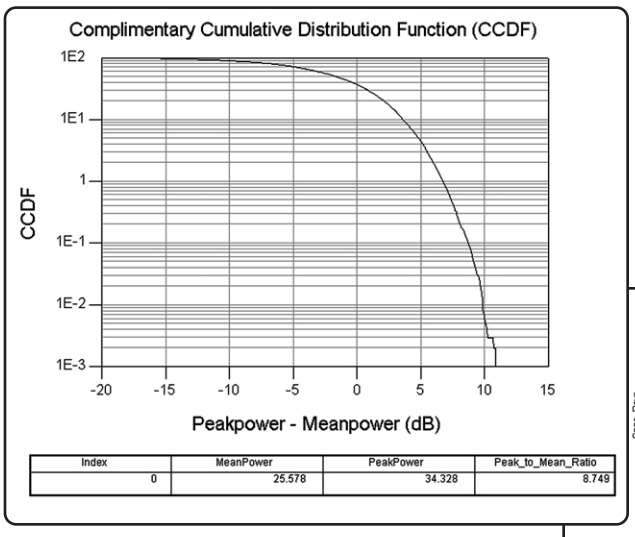
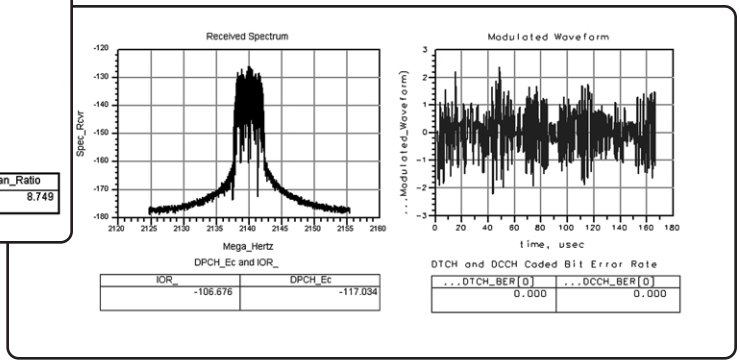


Fig. 5 – Complimentary Cumulative Distribution Function (CCDF) to Evaluate Signal Statistics.

Fig. 6 – Coded Bit Error Rate (BER) for the 12.2 kpbs Reference Downlink Signal.



Uplink Test and Verification Designs

- Transmit power
- Occupied bandwidth
- Out-of-band emissions
- Adjacent-channel leakage ratio (ACLR)
- Intermodulation products
- Modulation accuracy, EVM
- Peak code domain error

Downlink Test and Verification Designs

- Receiver sensitivity level
- Receiver maximum level
- Adjacent-channel selectivity
- Blocking sensitivity
- Intermodulation sensitivity

ESG Signal Source Configurations

Signal source designs offer configurations consistent with some of the uplink and downlink configurations provided by the Agilent ESG-D RF digital signal generator. Using ADS links to Agilent test equipment throughout your design cycle can help you to reduce design iterations and increase your chance for first-pass success.

Product Configuration

The 3GPP FDD W-CDMA Design Library (E8875A/AN) works directly with the DSP Designer Pro (E8821A/AN), Communications System Designer Pro (E8851A/AN), and Premier (E8852A/AN) in the Advanced Design System family of Agilent EEsof EDA products. The E8875 A/AN 3GPP FDD W-CDMA design library is designed for the Frequency Division Duplex (FDD) mode and is not intended to support the Time Division Duplex (TDD) mode.

For other possible product configurations, please contact your local Agilent field sales representative.

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