D9040EDPV eDP Test Application

KEYSIGHT

METHODS OF IMPLEMENTATION

Notices

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Contents

1 Overview

eDP Automated Testing—At a Glance

The Keysight D9040EDPV eDP Test Application for Embedded DisplayPort (eDP) standard provides a framework to use the Keysight Infiniium DSOs or UXRs to perform compliance testing on an Embedded DisplayPort Source device.

The Keysight D9040EDPV eDP Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

The eDP Test Application allows you to choose the eDP standard (either eDP 1.5 or eDP 1.4b) that is implemented on the DUT, based on which you may run compliance tests. Depending on the standard you select, the application provides the following tests:

Table 1 Source Electrical Specification (Differential and Single-Ended) Tests by Standard Reference

Test Name	References	References
	eDP 1.4b	**eDP 1.5**
Eye Diagram	eDP Standard Version 1.4, Section 4.6	RBR, HBR, HBR2 (CTLE): eDP 1.5, Section 4.7.1, Table 4-22 HBR3 (CTLE Only): eDP 1.5, Section 4.7.1, Table 4-23 HBR3 (CTLE + DFE): eDP 1.5, Section 4.7.1, Table 4-24
Non ISI Jitter	DisplayPort Standard Version 1. Revision 2, Table 3-23	RBR, HBR, HBR2 (CTLE): DP CTS 1.4a, Rev 1.0, Section 3.9.5, Table 3-45 HBR3 (CTLE Only): eDP 1.5, Section 4.6.3, Table 4-15 HBR3 (CTLE + DFE): eDP 1.5, Section 4.6.3, Table 4-15
Total Jitter	DisplayPort Standard Version 1. Revision 2, Table 3-23	eDP 1.5, Section 4.6.2, Table 4-14
Deterministic Jitter	DisplayPort Standard Version 1. Revision 2, Table 3-23	eDP 1.5, Section 4.6.2, Table 4-14
Random Jitter	DisplayPort Standard Version 1. Revision 2, Table 3-23	DisplayPort Standard Version 1. Revision 2, Table 3-23
Peak to Peak Differential Voltage	eDP Standard Version 1.4b (Section 4.4, Table 4-9)	eDP 1.5, Section 4.5, Table 4-11
Differential Voltage Level	eDP Standard Version 1.4, Section 4.3	eDP 1.5, Section 4.5, Table 4-11
Pre-Emphasis Level	eDP Standard Version 1.4, Section 4.3	eDP 1.4, Section 4.3

Test Name	References	References
Rise/Fall Time	eDP Standard Version 1.4, Section 4	DP 1.1 CTS, Section 3.6
Inter Pair Skew	eDP Standard Version 1.4, Section 4	RBR, HBR, HBR2: eDP CTG Version 1.0, Section 3.2.5 HBR3: DP 1.4a CTS Version 1.1, Section 3.6, Table 3-33
Main Link Frequency Compliance	eDP Standard Version 1.4, Section 4.4, Table 4-9	eDP 1.5, Section 4.5, Table 4-11
SSC Modulation Frequency	eDP Standard Version 1.4, Section 4.4	DP 2.0, Section 3.5.4, Table 3-38
SSC Modulation Deviation	eDP Standard Version 1.4, Section 4.4	DP 2.0, Section 3.5.4, Table 3-38
Intra Pair Skew	eDP Standard Version 1.4, Section 4	eDP 1.5, Section 4.5, Table 4-12
AC Common Mode Noise	eDP Standard Version 1.4, Section 4	RBR, HBR: DP 2.0, Section D.2, Table D-3 HBR2: DP 2.0, Section D.2, Table D-3 HBR3: DP 2.0, Section D.2, Table D-3
Rise and Fall Time Mismatch	DisplayPort Compliance Test Standard Version 1, Section 3.7	DP 1.1 CTS, Section 3.7
AUX Channel Unit Interval	DisplayPort Standard 1.3, Section 3.4.2, Table 3-4	DisplayPort Standard 1.3, Section 3.4.2, Table 3-4
AUX Channel Eye	DisplayPort Compliance Test Specification Version 1.2b, Section 8.1	DisplayPort Compliance Test Specification Version 1.2b, Section 8.1
AUX Channel Peak to Peak Voltage	eDP Standard Version 1.4b (Section 4.7.1, Table 4-20)	eDP Standard Version 1.5 Section 4.7.1, Table 4-20
AUX Channel Eye Sensitivity Calibration	DisplayPort Compliance Test Specification Version 1.2b, Section 8.2	DisplayPort Compliance Test Specification Version 1.2b, Section 8.2
AUX Channel Eye Sensitivity	DisplayPort Compliance Test Specification Version 1.2b, Section 8.2	DisplayPort Compliance Test Specification Version 1.2b, Section 8.2

Licensing Information

Refer to the *Data Sheet* pertaining to eDP Test Application to know about the licenses you must install along with other optional licenses. Visit "http://www.keysight.com/find/D9040EDPV" and in the web page's **Document Library** tab, you may view the associated Data Sheet.

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

The licensing format for Keysight License Manager 6 differs from its predecessors. See "Installing the License Key" on page 15 to see the difference in installing a license key using either of the applications on your machine.

Required Equipment and Software

Hardware

- Use one of the following Oscilloscope models:
  - Digital Storage Oscilloscopes: All 90000A/90000X/90000Q/V-Series/Z-Series/Q-Series Infiniium scopes with a bandwidth of 16 GHz and above for eDP 1.4b and eDP 1.5.
  - Keysight UXR Oscilloscopes
  - Keyboard, qty=1, (provided with Keysight Infiniium Oscilloscope)
  - Mouse, qty=1, (provided with Keysight Infiniium Oscilloscope)

Following fixtures and accessories are required to run the Keysight D9040EDPV eDP Test Application.

Table 2 Required fixtures and accessories

Required Equipment	Quantity	Recommended Oscilloscope
Embedded DisplayPort Test Point Adapter (Recommended: Wilder eDP TPA 30/40/50)*	1	Infiniium Series
E2655A/B/C Probe De-Skew and Performance Verification Kit	1	Infiniium Series
BNC to SMA Converter	4	For Infiniium 90000A Series
SMA (male) to SMA (male) Converter	4	For Infiniium 90000X, 90000 Q Series, V-Series, Z-Series, Q-Series and UXR Series

* All Wilder Technologies Test Point Adapters require the Wilder Technologies DP-TPA-A Aux Control Board

Table 3 InfiniiMax Series Probe Amplifiers with minimum 12 GHz bandwidth

Required Equipment	Quantity	Recommended Oscilloscope
1169A 12 GHz InfiniiMax II Series Probe Amplifier	5	Infiniium Series
N2832A 13 GHz InfiniiMax III+ Series Probe Amplifier		
N2800A 16 GHz InfiniiMax III Series Probe Amplifier		
MX0023A 25 GHz InfiniiMax RC Probe Amplifier		

Table 4 InfiniiMax Series Probe Head with minimum 12 GHz bandwidth

Required Equipment	Quantity	Recommended Oscilloscope
Physical Layer Tests		
N5380A InfiniiMax II 12 GHz Differential SMA Adapter	3	Infiniium Series
N5444A InfiniiMax III 28 GHz SMA Probe Head		
MX0105A InfiniiMax 20 GHz Differential SMA Probe Head		
AUX Channel Physical Layer Tests		
E2677A InfiniiMax 12 GHz Differential Solder-In	2	Infiniium Series
E2678A/B InfiniiMax 12 GHz Single-Ended/Differential Probe Head & Accessories		

Table 5 Automation Controllers (Optional)

Required Equipment	Quantity	Recommended Oscilloscope
For Source DUT testing, Unigraf DPR-100 Compact Sized DisplayPort Reference Sink	4	Infiniium Series

Software

- The minimum version of Infiniium Oscilloscope Software (see the D9040EDPV eDP Test Application Release Notes)
- D9040EDPV eDP Test Application software

In This Book

This manual describes the tests that are performed by the Keysight D9040EDPV eDP Test Application in more detail; it contains information from (and refers to) the eDP specification and it describes how the tests are performed.

- Chapter 1, “Overview” shows how to install and license the automated test application (if it was purchased separately).
- Chapter 2, “Installing the Test Application and Licenses” explains how to obtain the installer for the automated test application and install the associated licenses (if it was purchased separately).
- Chapter 3, “Preparing to Take Measurements” describes how to launch the Keysight D9040EDPV eDP Test Application and gives a brief overview of how it is used.
- Chapter 4, “eDP Automated Source Differential Tests” describes the differential tests for interoperability verification of eDP sources.
- Chapter 5, “eDP Automated Source Single-Ended Tests” describes the single-ended tests for interoperability verification of eDP sources.
- Chapter 6, “eDP Automated Source AUX Channel Physical Layer Tests” describes the Auxiliary Channel Physical Layer tests for interoperability verification of both eDP source and sink devices along with an optional reference sink / reference source device, respectively.

See Also

The Keysight D9040EDPV eDP Test Application’s Online Help, which describes:

- Starting the eDP Test Application
- Creating or Opening a Test Project
- Setting Up the Test Environment
- Selecting Tests
- Configuring Tests
- Verifying Physical Connections
- Running Tests
- Configuring Automation in the Test Application
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
- Additional Settings in the Test App

2 Installing the Test Application and Licenses

If you purchased the D9040EDPV eDP Test Application separate from your Infiniium oscilloscope, you must install the software and license key.

Installing the Test Application

1 Make sure you have the minimum version of Infiniium Oscilloscope software (see the Keysight D9040EDPV eDP Test Application release notes). To ensure that you have the minimum version, select **Help > About Infiniium...** from the main menu.

2 To obtain the eDP Test Application, go to Keysight website: "http://www.keysight.com/find/D9040EDPV".

3 In the web page's **Trials & Licenses** tab, click the **Details and Download** button to view instructions for downloading and installing the application software.

NOTE You must make sure to accept the installation of the *.NET framework* software, which is required to run the eDP Test Application.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

1 Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.

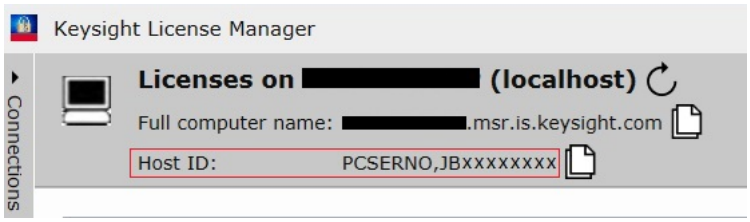

Figure 1 Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager.

3 From the configuration menu, use one of the options to install each license file.

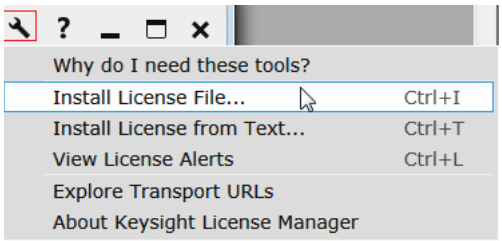

Figure 2 Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

1. Launch Keysight License Manager 6 on your machine, where you wish to run the Test Application and its features.
2. Copy the Host ID, which is the first set of alphanumeric value (as highlighted in Figure 3) that appears in the Environment tab of the application. Note that x indicates numeric values.

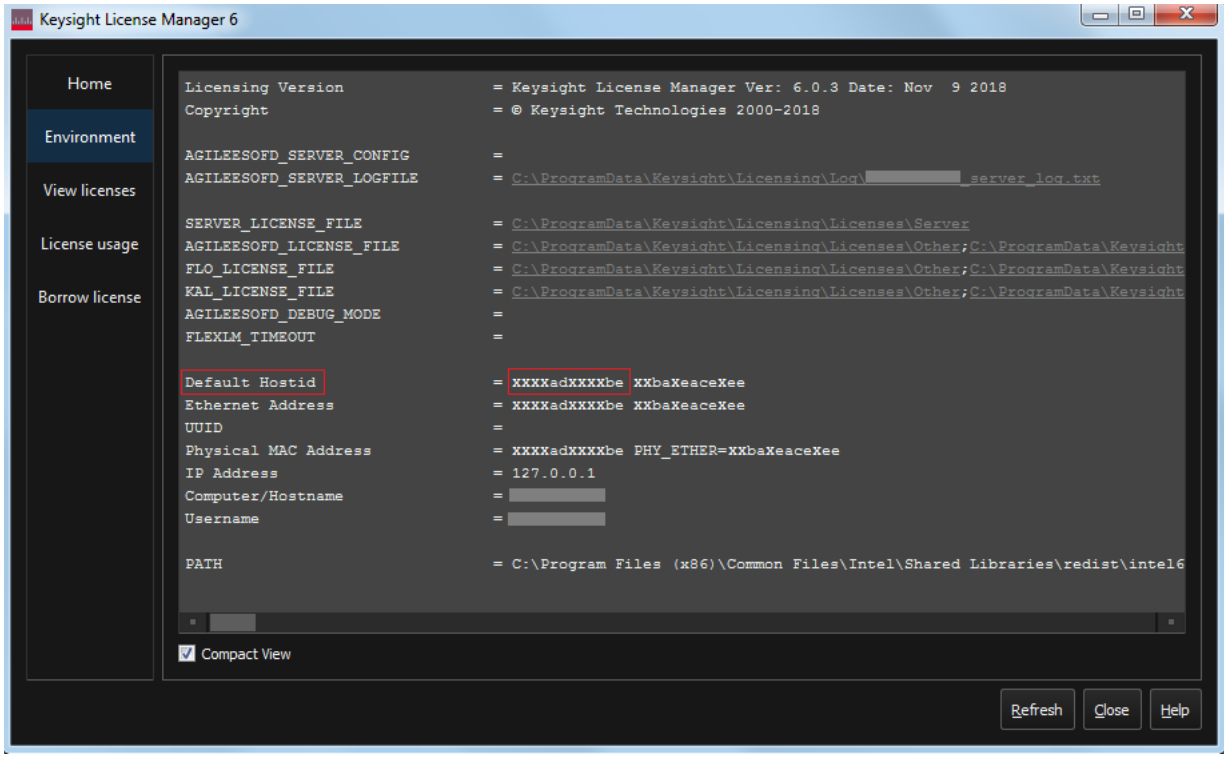

Figure 3 Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager 6.

3 From the Home tab, use one of the options to install each license file.

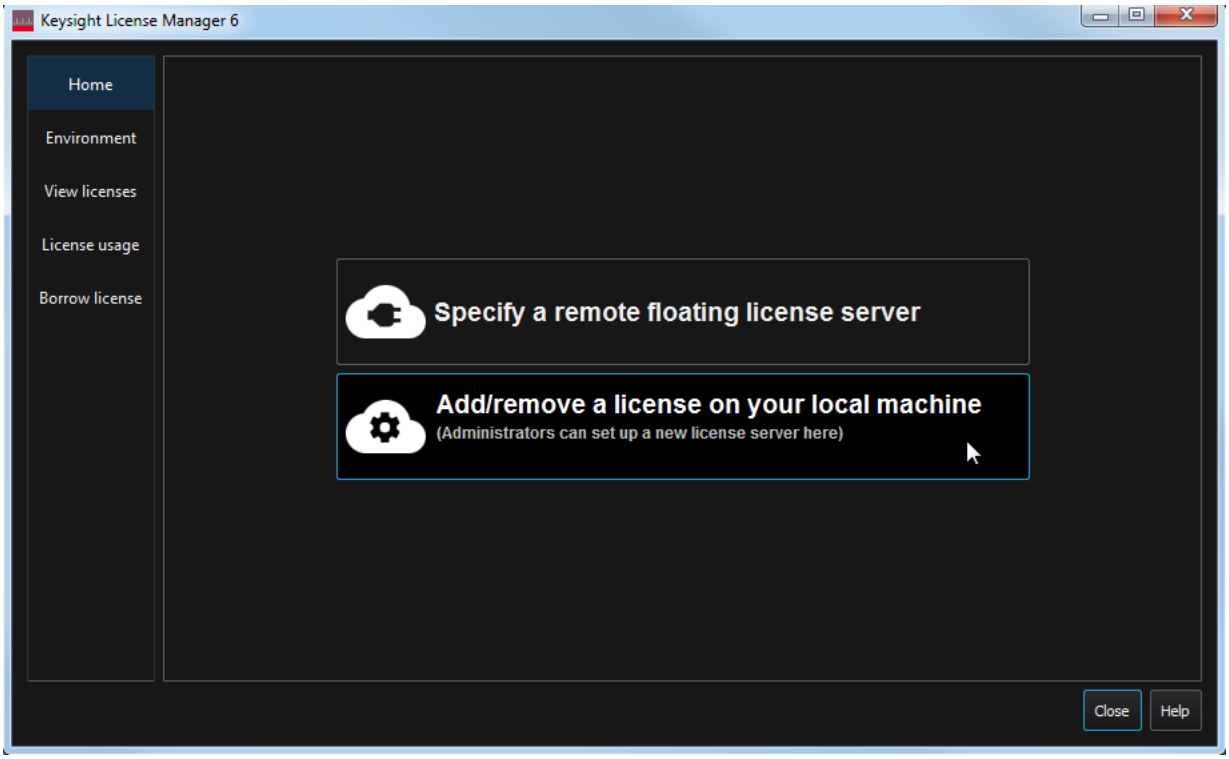

Figure 4 Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

3 Preparing to Take Measurements

Before running the automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this application. After the oscilloscope and probe have been calibrated, you are ready to start the eDP Test Application and perform the measurements.

Calibrating the Oscilloscope

If you have not already calibrated the oscilloscope, refer to the *User Guide* for the respective Oscilloscope you are using.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.

NOTE If you switch cables between channels or other Oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the eDP Test Application

1 Ensure that the eDP Device Under Test (DUT) is operating and set to desired test modes. To start the eDP Test Application: From the Infiniium Oscilloscope's main menu, select **Analyze > Automated Test Apps > D9040EDPV eDP Test App**.

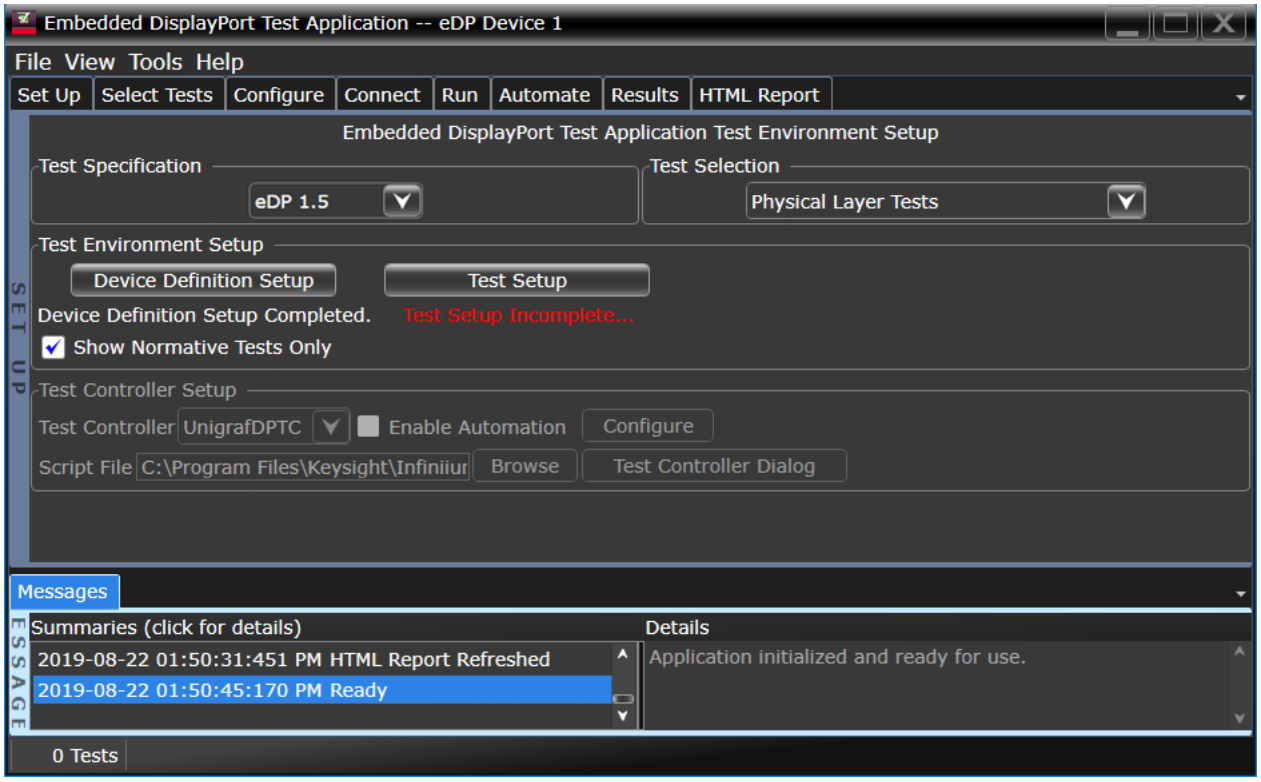

Figure 5 eDP Test Application Main Window

To understand the functionality of the various features in the user interface of the Test Application, refer to the *Keysight D9040EDPV eDP Test Application Online Help* available in the Help menu.

The task flow pane and the tabs in the main pane show the steps you take in running the automated tests:

Set Up	Lets you identify and set up the test environment, including information about the device under test. The Test App includes relevant information in the final HTML report.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (for example, channels used in test, voltage levels, etc.).
Connect	Shows you how to connect the oscilloscope to the device under test for the tests that are to be run.
Run	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automate	Lets you construct scripts of commands that drive execution of the application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE

In the **Configure** tab, the values for all such Configuration parameters that are Oscilloscope-dependent, will correspond to the Oscilloscope Model (DSOs or UXRs), where you are running the Test Application.

Setting Up the Transmission Path Test Point

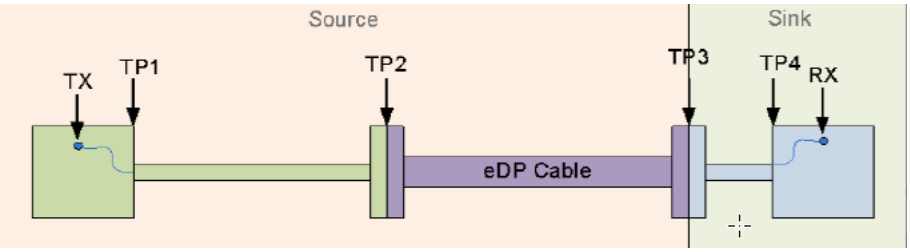

Figure 6 Embedded Link Test Point

The links in an Embedded DisplayPort (eDP) contain a Transmitter (TX) and a Receiver (RX), where the transmitter is connected to the Source device and the receiver to the Sink device. You may optionally set up connectors anywhere along the embedded channel. Taking into account various embedded topologies, eDP provides measurement of the physical layer attributes.

Figure 6 shows a pictorial representation of the embedded link transmission path test points to measure signal voltage and jitter on an embedded channel, which are:

TP1	eDP transmitter package pins
TP2	Source device eDP Cable Connector
TP3	Sink device (panel) eDP Cable Connector
TP4	eDP receiver package pins

Overview on Connection Points for Source Tests

This section describes the tests for interoperability verification of eDP sources. Sources must be tested either at point TP3 or point TP3_EQ, where the latter is placed after the Reference Receiver Equalizer, as shown below in Figure 7. You must also include the actual eDP cable, which the system integrator intends to use (or a properly correlated model of this cable) for source test measurements. The analyzer and test point access fixtures from each test solution provider are identified in this document. Unless specifically stated under the test conditions, all supported lanes for the DUT must be evaluated.

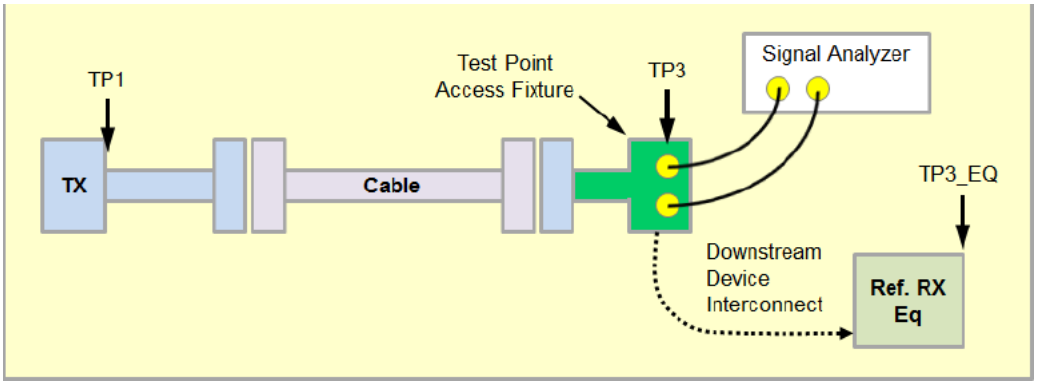

Figure 7 Test Point 3 Connection for Source Tests

The Source Tests broadly include three categories namely:

- Source Differential Tests
- Source Single-Ended Tests
- Source AUX Channel Physical Layer Tests

NOTE All tests performed on the Source DUT are Normative tests only.

4 eDP Automated Source Differential Tests

This section describes the differential tests for interoperability verification of eDP sources.

Eye Diagram Test

Test Overview

The Eye Diagram Test evaluates the waveform to ensure that the timing variables and amplitude trajectories support the overall eDP system objective of Bit Error Rate in data transmission.

The source eye diagram performance provides the best visual aid to assess the interoperability potential by showing the amplitude and timing attributes of the signal and also provides an intuitive understanding of design margin.

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3 and TP3_EQ	
Bit Rate	All bit rates are supported.	
Voltage Level and Pre-emphasis Level	The Source device sets the Voltage level and Pre-emphasis level for each supported data rate, such that it meets the Pass/Fail criteria as specified in the CTG Specification.	
SSC	If the DUT can operate in either the SSC-enabled or the SSC-disabled state, it shall be tested in both conditions.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal.

2 If equalizer is enabled, please set up the equalizer for TP3_EQ, else please skip this step.

3 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.

4 Measure the data rate and validate the test pattern.

5 If random noise is included, use “EZJIT Complete” to perform jitter separation base on the Time Interval Error (TIE) measurement of the signal.

6 Set up the clock recovery base on the clock recovery setting of the configuration variable.

7 Create eye diagram at the middle of the screen. The range of the eye diagram must be more than one Unit Interval (UI) but less than 2.5 UI.

8 To obtain the optimum eye height, compute the eye height at different passing points.

9 Load the eye mask and position it centrally at the middle of the eye diagram.

a To measure with the “Dynamic” eye mask height location, note the center eye mask perimeter value and if required, modify the eye mask height vertices to the optimum eye height location.

- Note the center eye mask and compute the eye mask height and width. The eye mask supports only four vertices point center mask.

- To modify the eye mask height point, shift the eye mask height vertices horizontally between 0.375 UI and 0.625 UI as shown in Figure 8.

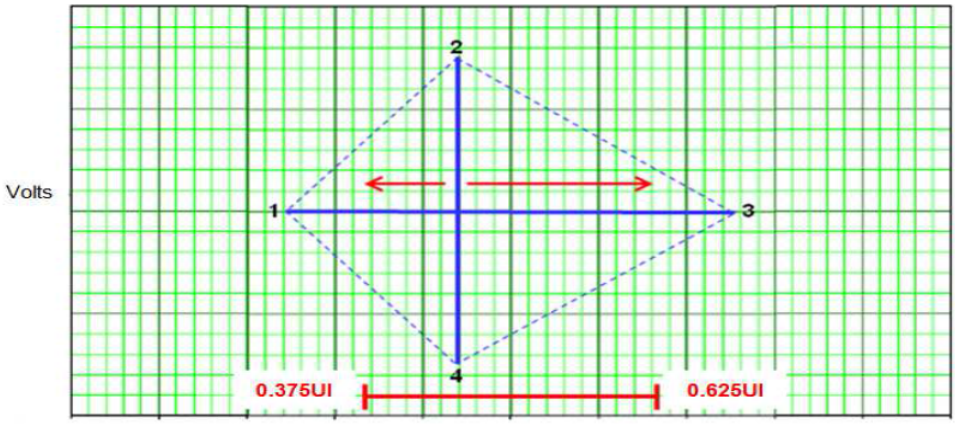

Figure 8 eDP TP3_EQ Eye Mask for eDP 1.4b

b To measure with the “Fixed” eye mask height location, load the eye mask directly without any modification.

10 Run the eye mask until you achieve the required number of UIs.

11 Check for any signal trajectories that may have entered into the eye mask.

Viewing Test Results

The measured eye diagram for the test signal must fall within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

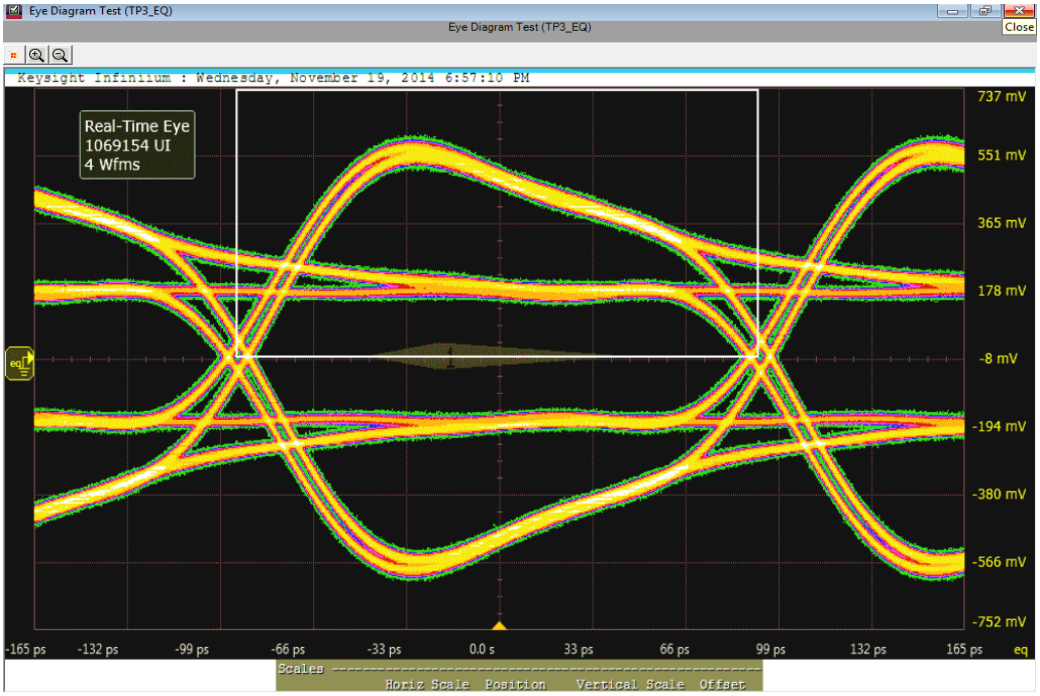

Figure 9 Reference Image for Eye Diagram Test

Non ISI Jitter Test

Test Overview

The Non ISI (Inter Symbol Interference) Jitter Test evaluates the amount of Non ISI jitter accompanying the data transmission.

The overall system jitter budget defines the point of compliance for the Non ISI Jitter Test and the different amounts of jitter allocation that each system component is allowed to contribute. Exceeding any of these limits violates the component level jitter budget. Non ISI jitter must be limited in magnitude because the receiver is unable to compensate any higher amount of jitter.

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3 and TP3_EQ	
Bit Rate	All bit rates are supported.	
Voltage Level and Pre-emphasis Level	The Source device sets the Voltage level and Pre-emphasis level for each supported data rate, such that it meets the Pass/Fail criteria as specified in the CTG Specification.	
SSC	If the DUT can operate in either the SSC-enabled or the SSC-disabled state, it shall be tested in both conditions.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal.

2 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.

3 Measure the data rate and validate the test pattern.

4 Set up the clock recovery base on the clock recovery setting in configuration variable.

5 Use “EZJIT Complete” to perform jitter separation base on the Time Interval Error (TIE) measurement of the signal.

6 Compute the Non ISI Jitter using the following equation:

$$Non\ ISI\ Jitter = Total\ Jitter - Jitter_{ISI}$$

where, $Jitter_{ISI}$ is the ISI Jitter component induced by ISI, which is the peak-to-peak value of the histogram of rising edges or of the histogram of the falling edges, whichever is greater.

NOTE DFE will be enabled by default for HBR3 bit rate.

Viewing Test Results

The measured Non ISI Jitter value for the test signal must fall within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

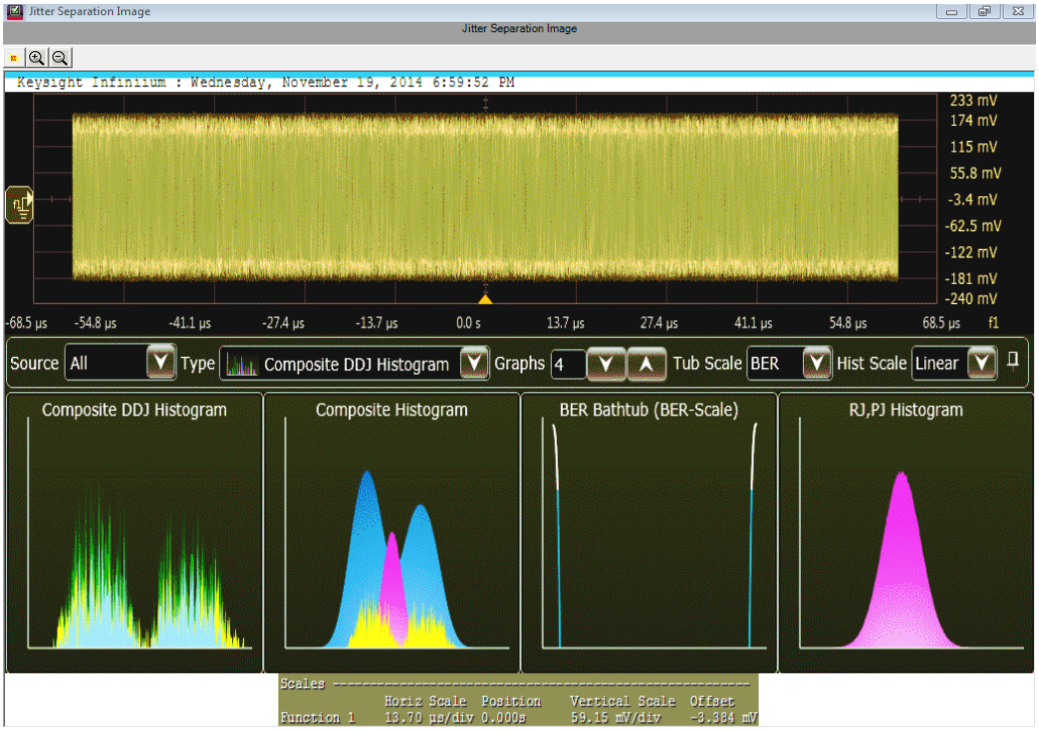

Figure 10 Reference Image for Non ISI Jitter Test

Total Jitter Test

Test Overview

The Total Jitter Test evaluates the total jitter, which is a form of data time interval error (Data-TIE) jitter measurement, which accompanies data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique.

Similar to Non ISI jitter, the overall system jitter budget defines the point of compliance for the Total Jitter Test and allocates different amounts of jitter that each system component is allowed to contribute. Exceeding any of these limits violates the component level jitter budget.

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3 and TP3_EQ	
Bit Rate	All bit rates are supported	
Voltage Level and Pre-emphasis Level	Voltage level and Pre-emphasis level as set for the Eye Diagram test.	
SSC	If the DUT can operate in either the SSC-enabled or the SSC-disabled state, it shall be tested in both conditions.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal.

2 If equalizer is enabled, please set up the equalizer for TP3_EQ, else please skip this step.

3 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.

4 Measure the data rate and validate the test pattern.

5 Set up the clock recovery base on the clock recovery setting of the configuration variable.

6 Use “EZJIT Complete” to perform jitter separation base on the Time Interval Error (TIE) measurement of the signal.

7 Use the Dual Dirac Technique to estimate the Total Jitter for bit error rate of 10^{-9} using the following equation:

$$Total\ Jitter = Deterministic\ Jitter_{dd} + n * Random\ Jitter$$

where, Deterministic $Jitter_{dd}$ is the deterministic jitter, Random Jitter is the random jitter, which is a standard deviation value of an idealized pure noise process and n is the multiplier that is determined by the bit error ratio (n = 12.0 for bit error ration of $1 * 10^{-9}$).

NOTE DFE will be enabled by default for HBR3 bit rate.

Viewing Test Results

The measured value of Total Jitter for the test signal must fall within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

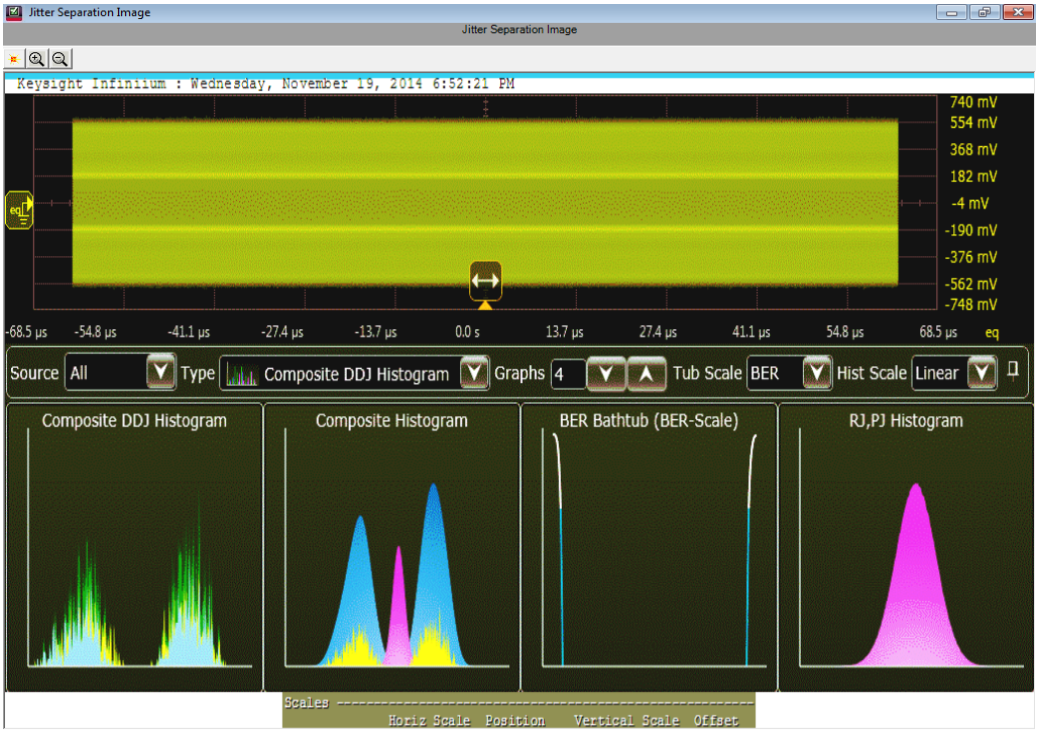

Figure 11 Reference Image for Total Jitter Test

Deterministic Jitter Test

Test Overview

The Deterministic Jitter Test evaluates the deterministic jitter, which is also a form of Data-TIE jitter measurement, accompanying the data transmission.

Similar to the previous types of jitter, the overall system jitter budget defines the point of compliance for the Deterministic Jitter Test and allocates different amounts of jitter that each system component is allowed to contribute. Exceeding any of these limits violates the component level jitter budget.

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3 and TP3_EQ	
Bit Rate	All bit rates are supported	
Voltage Level and Pre-emphasis Level	Voltage level and Pre-emphasis level as set for the Eye Diagram test.	
SSC	If the DUT can operate in either the SSC-enabled or the SSC-disabled state, it shall be tested in both conditions.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal.
2 If equalizer is enabled, please set up the equalizer for TP3_EQ, else please skip this step.
3 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.
4 Measure the data rate and validate the test pattern.
5 Set up the clock recovery base on the clock recovery setting of the configuration variable.
6 Use “EZJIT Complete” to perform jitter separation base on the Time Interval Error (TIE) measurement of the signal.

NOTE DFE will be enabled by default for HBR3 bit rate.

Viewing Test Results

The measured Deterministic Jitter value for the test signal must fall within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

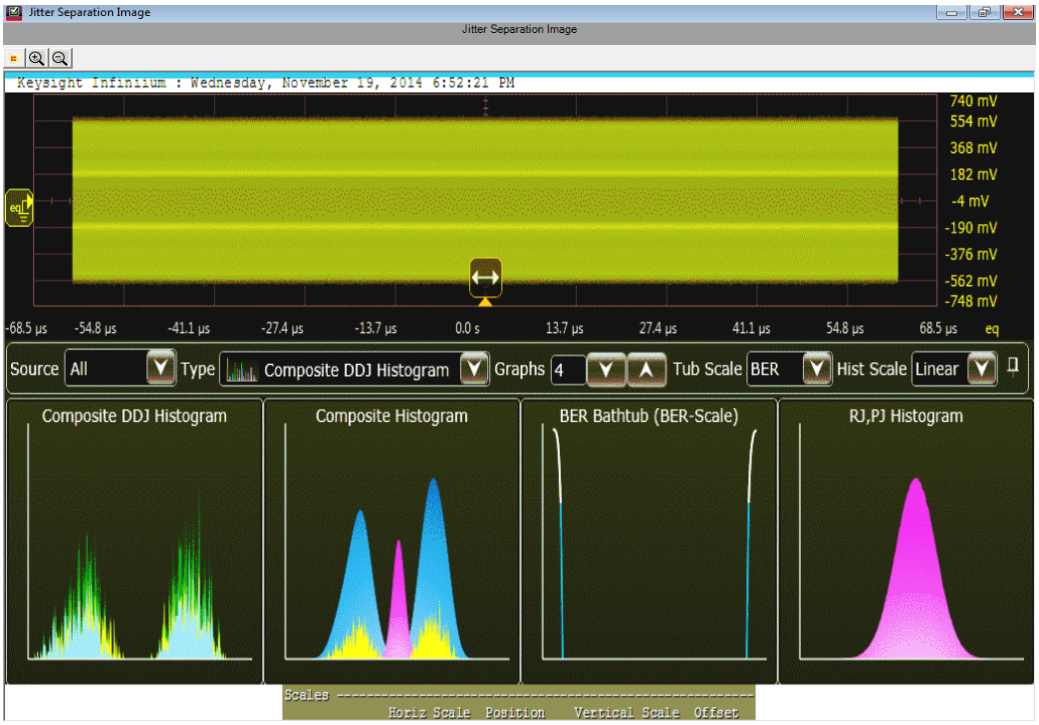

Figure 12 Reference Image for Deterministic Jitter Test

Random Jitter Test

Test Overview

The Random Jitter Test evaluates the random jitter, which is also a form of Data-TIE jitter measurement, accompanying the data transmission.

Similar to the previous types of jitter, the overall system jitter budget defines the point of compliance for the Random Jitter Test and allocates different amounts of jitter that each system component is allowed to contribute. Exceeding any of these limits violates the component level jitter budget.

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3 and TP3_EQ	
Bit Rate	All bit rates are supported.	
Voltage Level and Pre-emphasis Level	Voltage level and Pre-emphasis level as set for the Eye Diagram test.	
SSC	If the DUT can operate in either the SSC-enabled or the SSC-disabled state, it shall be tested in both conditions.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal.
2 If equalizer is enabled, please set up the equalizer for TP3_EQ, else please skip this step.
3 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.
4 Measure the data rate and validate the test pattern.
5 Set up the clock recovery base on the clock recovery setting of the configuration variable.
6 Use “EZJIT Complete” to perform jitter separation base on the Time Interval Error (TIE) measurement of the signal.

NOTE DFE will be enabled by default for HBR3 bit rate.

Viewing Test Results

The measured random jitter value for the test signal must fall within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

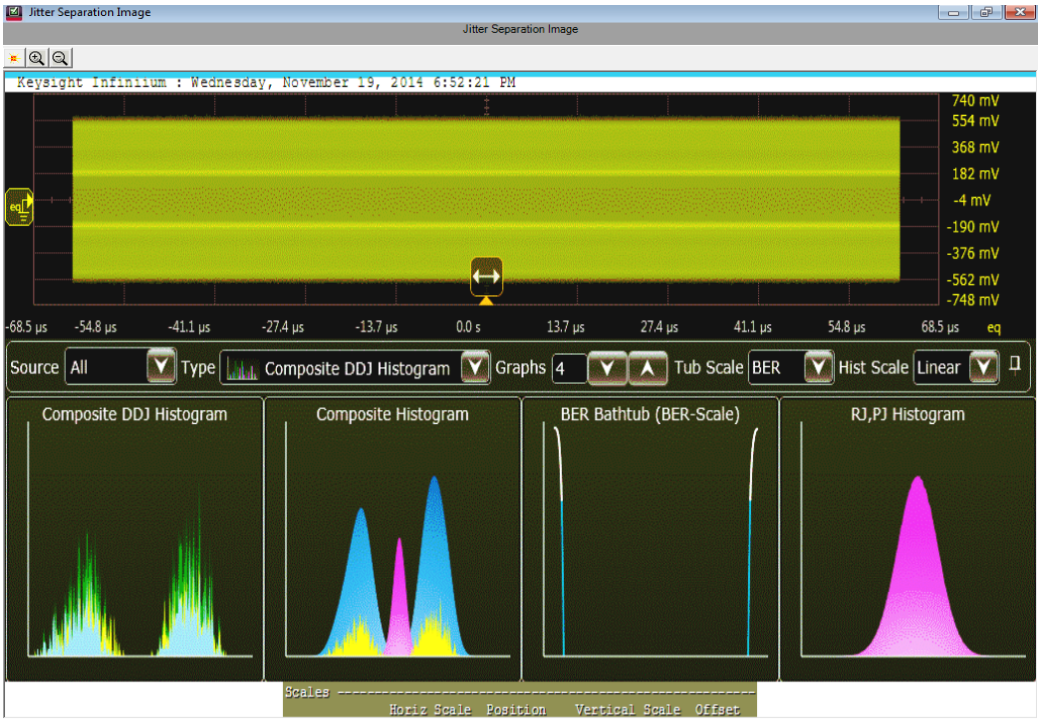

Figure 13 Reference Image for Random Jitter Test

Peak to Peak Differential Voltage Test

Test Overview

The Peak to Peak Differential Voltage Test evaluates the peak to peak voltage accompanying the data transmission.

You can measure the transition and non-transition voltage swings for each supported voltage level and pre-emphasis setting. To obtain the peak to peak voltage, you must combine the High and Low voltage measurements formed within each transition and non-transition voltage swing.

Compute the peak to peak voltages for transition and non-transition voltage swing for a given voltage level and pre-emphasis level (LvlX) using the following equations:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

where $V_{T\_LvlX\_PP}$ is the peak to peak voltage at the transition bit and $V_{N\_LvlX\_PP}$ is the peak to peak voltage at the non transition bit. The constituent voltages $V_{T\_LvlX\_H}$, $V_{T\_LvlX\_L}$, $V_{N\_LvlX\_H}$ and $V_{N\_LvlX\_L}$ are identified in the following figures showing generalized pre-emphasis and non pre-emphasized waveforms.

NOTE **The condition for Level 0 pre-emphasis is identified separately in the following figures but is merely a special case. The measurement of high and low voltage values is an average value derived from a specific number of UI obtained over a certain number of required test patterns.**

For PLTPAT

There are specific qualifying patterns in the 80-Bit Custom pattern (PLTPAT) for 'High' and 'Low' voltage level measurements. These measurements require a 1-1-1-1-1-0-0-0-0-0 balanced pattern and no preconditioning is required on this pattern. The transition voltage measurements, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ is the average value over the 40% to 70% UI points in the transition bit. The non-transition voltage measurement, $V_{N\_LvlX\_H}$ and $V_{N\_LvlX\_L}$ is the average value over three UI points ending at the 50% point of the 5th bit of the five successive transmitted 1s or 0s of the patterns. Refer to Figure 14.

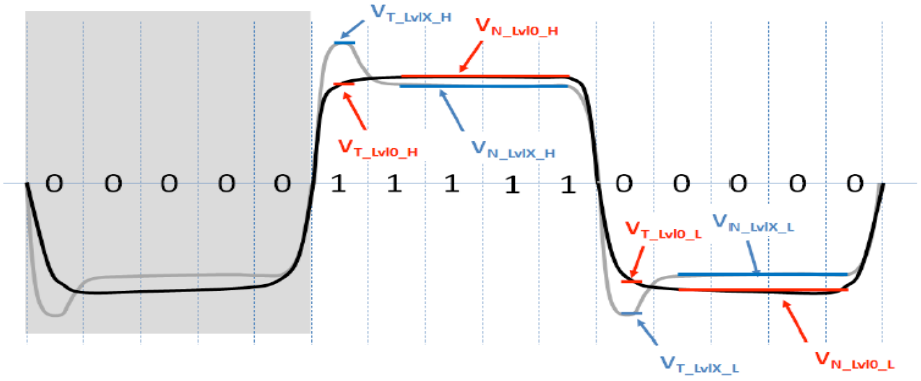

Figure 14 High and Low Voltage Measurement for PLTPAT

For PRBS7

There are specific qualifying patterns in PRBS7 and other sequence for 'High' and 'Low' voltage level measurements. The 'High' level measurements require a 0-1-0-1-1-1-1-1-1-1 pattern and the 'Low' level measurements require a 1-0-1-0-0-0-0-1 pattern. Refer to Figure 15 and Figure 16.The first 3-bits in these patterns are a precondition to the transition measurements. The precondition bits for a transition to high level voltage measurement, are 0-1-0 and for a transition to low level voltage measurement are 1-0-1.

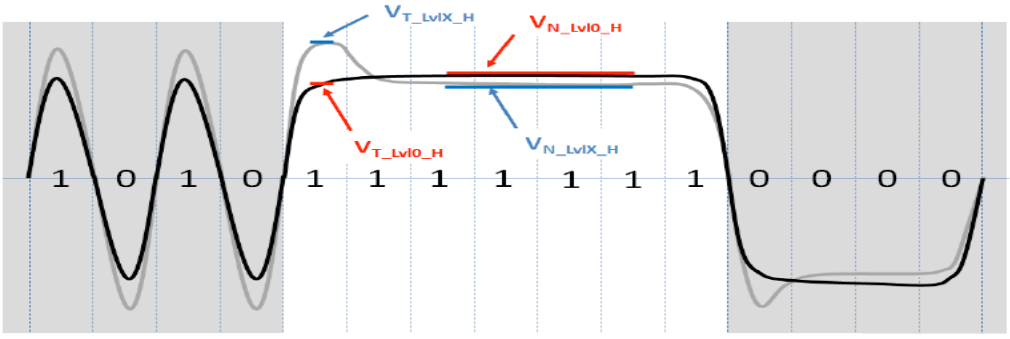

Figure 15 High Voltage Measurement for PRBS7

The transition voltage measurements, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average value over the 40% to 70% UI points in the transition bit. The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average value over three UI points ending at the 50% point of the 6^{th} bit of the seven successive transmitted 1s of the patterns. The non-transition voltage measurement, $V_{N\_LvlX\_L}$ is the average value over two UI points ending at 50% point of the 4^{th} bit of the four successive transmitted 0s of the patterns.

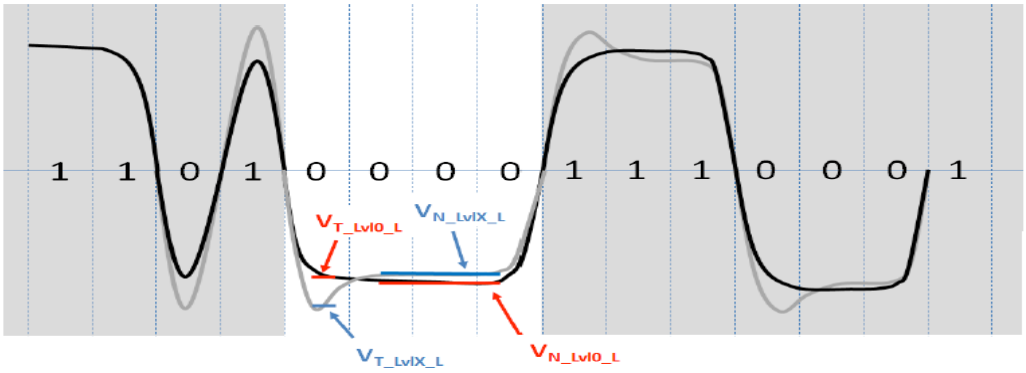

Figure 16 Low Voltage Measurement for PRBS7

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3	
Bit Rate	All bit rates are supported.	
Voltage Level and Pre-emphasis Level	Any Voltage level and Pre-Emphasis level that are compliant to all normative tests run on the Source.	

Specification	eDP Version 1.4b	eDP Version 1.5
SSC	If the DUT can operate in either the SSC-enabled or the SSC-disabled state, it shall be tested in both conditions.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal.

2 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.

3 Measure the data rate and validate the test pattern.

4 Acquire the qualifying test pattern over the specific number of required patterns to measure the high voltage level.

5 Set up the Histogram to measure the average value of high voltage level for both transition and non-transition voltage levels.

6 Acquire the qualifying test pattern over the specific number of required patterns to measure the low voltage level.

7 Set up the Histogram to measure the average value of low voltage level for both transition and non-transition voltage levels.

8 Compute the peak to peak voltage for both transition and non-transition voltage levels using the following equations:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

9 Obtain the value of the peak to peak differential voltage from the worst case of both transition and non-transition voltage measurements using the following equation:

$$V_{PP} = Worst\ Case\ (V_{T\_LvlX\_PP}, V_{N\_LvlX\_PP})$$

Viewing Test Results

The measured value of the peak to peak differential voltage for the test signal must fall within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

Figure 17 Reference Image for Peak to Peak Differential Voltage Test – V_H Transition Bit

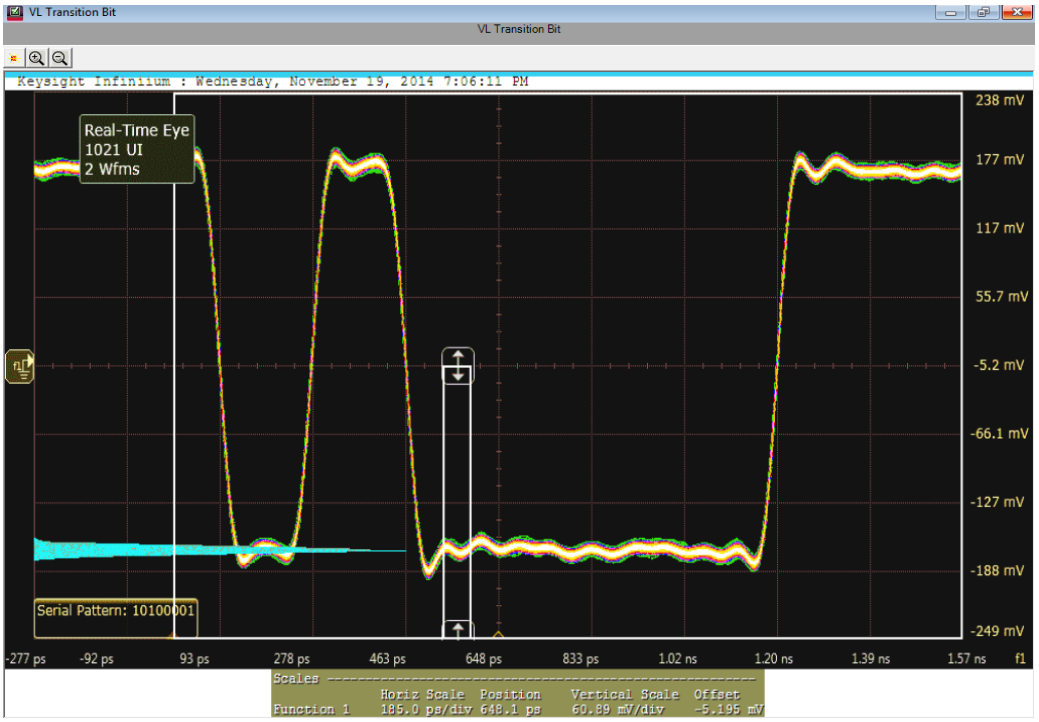

Figure 18 Reference Image for Peak to Peak Differential Voltage Test – V_L Transition Bit

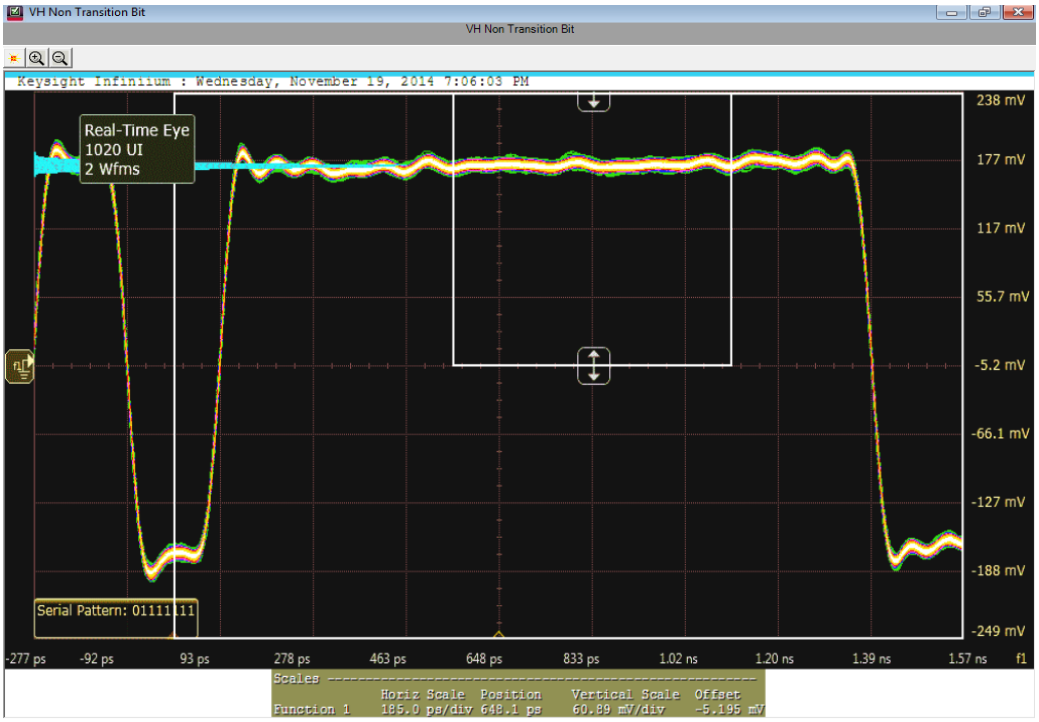

Figure 19 Reference Image for Peak to Peak Differential Voltage Test – V_H Non Transition Bit

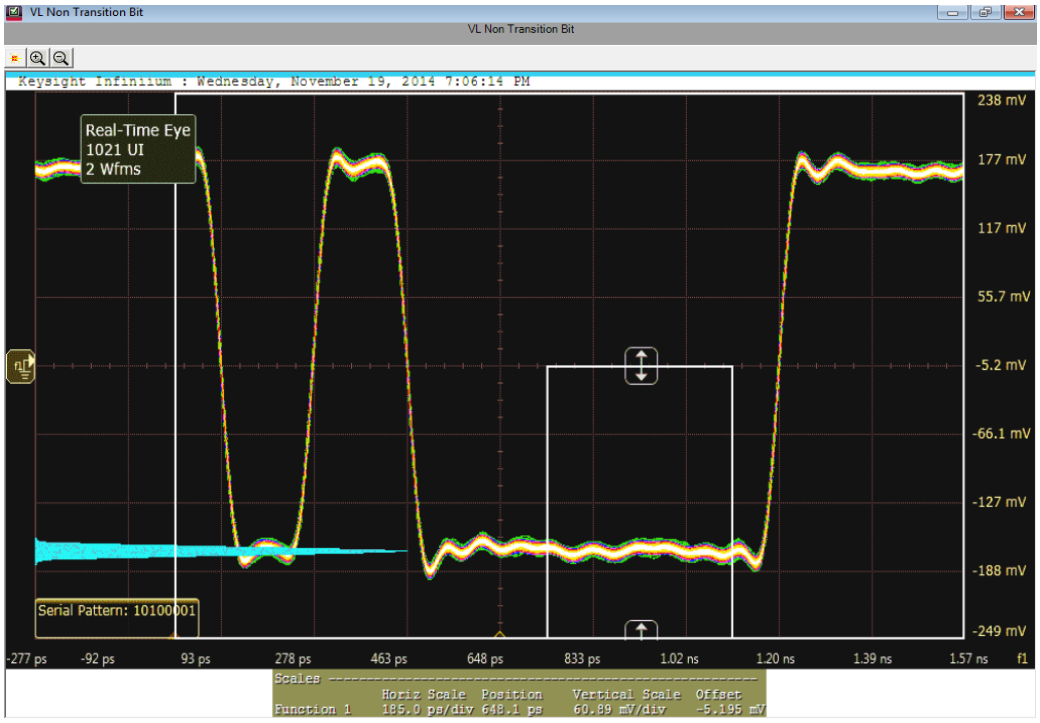

Figure 20 Reference Image for Peak to Peak Differential Voltage Test – V_L Non Transition Bit

Differential Voltage Level Test

Test Overview

The Differential Voltage Level Test evaluates the differential voltage level accompanying the data transmission.

You can define the expected output for each setting of voltage level on the source, such that the output correlates with the system budget elements such as cable loss, receiver EYE minimum/maximum values and PC board transmission line loss. Furthermore, it must be kept in mind that the link must benefit when you increase level settings.

You can measure the transition and non-transition voltage swings for each supported voltage level and pre-emphasis setting. To obtain the peak to peak voltage, you must combine the High and Low voltage measurements formed within each transition and non-transition voltage swing.

Compute the peak to peak voltages for transition and non-transition voltage swing for a given voltage level and pre-emphasis level (LvlX) using the following equations:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

where $V_{T\_LvlX\_PP}$ is the peak to peak voltage at the transition bit and $V_{N\_LvlX\_PP}$ is the peak to peak voltage at the non-transition bit. The constituent voltages $V_{T\_LvlX\_H}$, $V_{T\_LvlX\_L}$, $V_{N\_LvlX\_H}$ and $V_{N\_LvlX\_L}$ are identified in the following figures showing generalized pre-emphasis and non pre-emphasized waveforms.

NOTE **The condition for Level 0 pre-emphasis is identified separately in the following figures but is merely a special case. The measurement of high and low voltage values is an average value derived from a specific number of UI obtained over a certain number of required test patterns.**

For PLTPAT:

There are specific qualifying patterns in the 80-Bit Custom pattern (PLTPAT) for 'High' and 'Low' voltage level measurements. These measurements require a 1-1-1-1-1-0-0-0-0-0 balanced pattern and no preconditioning is required on this pattern. The transition voltage measurements, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ is the average value over the 40% to 70% UI points in the transition bit. The non-transition voltage measurement, $V_{N\_LvlX\_H}$ and $V_{N\_LvlX\_L}$ is the average value over three UI points ending at the 50% point of the 5th bit of the five successive transmitted 1s or 0s of the patterns. Refer to Figure 21.

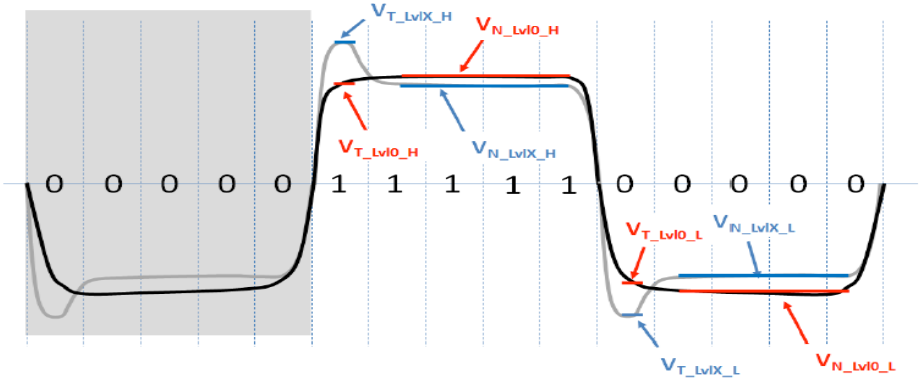

Figure 21 High and Low Voltage Measurement for PLTPAT

For PRBS7:

There are specific qualifying patterns in PRBS7 and other sequence for 'High' and 'Low' voltage level measurements. The 'High' level measurements require a 0-1-0-1-1-1-1-1-1-1 pattern and the 'Low' level measurements require a 1-0-1-0-0-0-0-0-1 pattern. Refer to Figure 22 and Figure 23. The first 3-bits in these patterns are a precondition to the transition measurements. The precondition bits for a transition to high level voltage measurement, are 0-1-0 and for a transition to low level voltage measurement are 1-0-1.

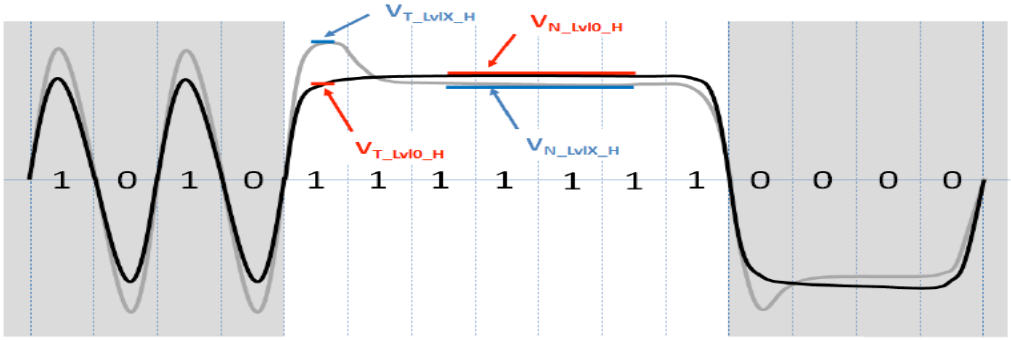

Figure 22 High Voltage Measurement for PRBS7

The transition voltage measurements, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average value over the 40% to 70% UI points in the transition bit. The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average value over three UI points ending at the 50% point of the 6^{th} bit of the seven successive transmitted 1s of the patterns. The non-transition voltage measurement, $V_{N\_LvlX\_L}$ is the average value over two UI points ending at 50% point of the 4^{th} bit of the four successive transmitted 0s of the patterns.

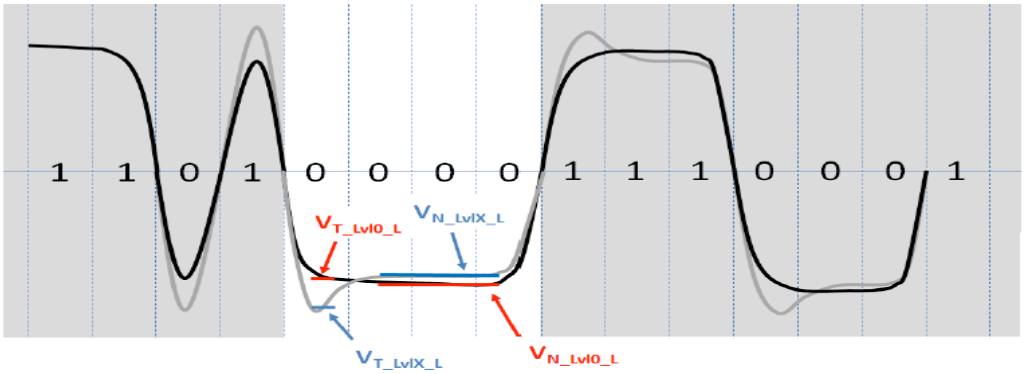

Figure 23 Low Voltage Measurement for PRBS7

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3	
Bit Rate	All bit rates are supported.	
Voltage Level and Pre-emphasis Level	Any Voltage level and Pre-Emphasis level that are compliant to all normative tests run on the Source.	

Specification	eDP Version 1.4b	eDP Version 1.5
SSC	If the DUT can operate in either the SSC-enabled or the SSC-disabled state, it shall be tested in both conditions.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal.

2 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.

3 Measure the data rate and validate the test pattern.

4 Acquire the qualifying test pattern over the specific number of required patterns to measure the high voltage level.

5 Set up the Histogram to measure the average value of high voltage level for both transition and non-transition voltage levels.

6 Acquire the qualifying test pattern over the specific number of required patterns to measure the low voltage level.

7 Set up the Histogram to measure the average value of low voltage level for both transition and non-transition voltage levels.

8 Compute the value of differential voltage level from the peak to peak voltage for non-transition voltage measurement using the following equation:

$$Differential\ Voltage\ Level\ (V_{N\_LvlX\_PP}) = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

Viewing Test Results

The measured value of the differential voltage level for the test signal must fall within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

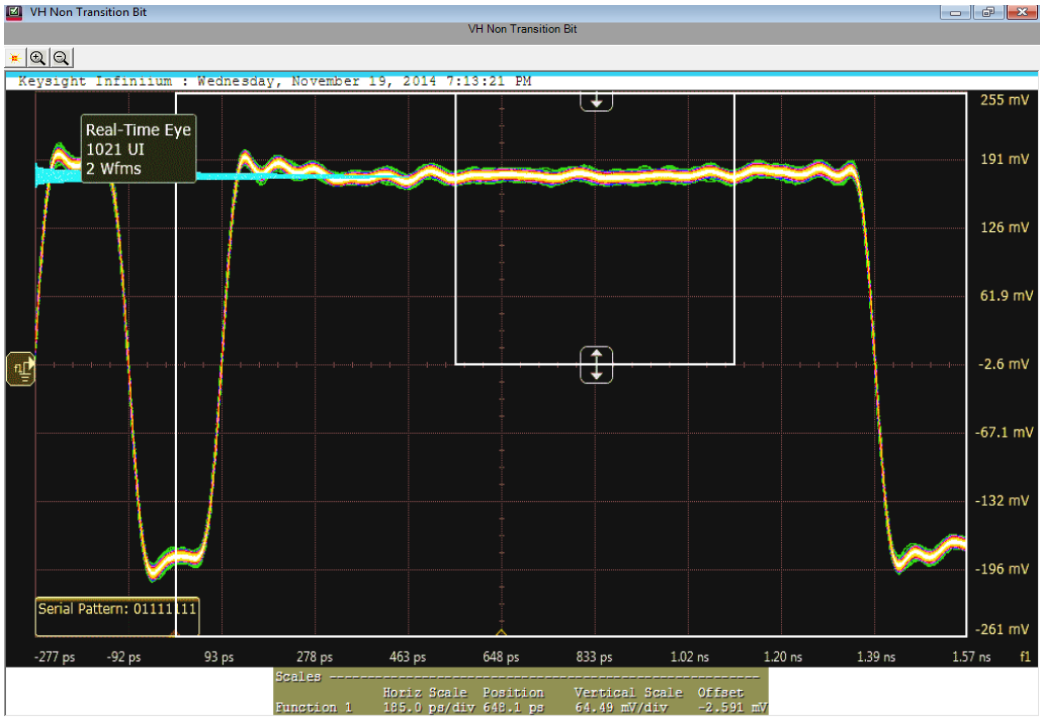

Figure 24 Reference Image for Differential Voltage Level Test – V_H Non Transition Bit

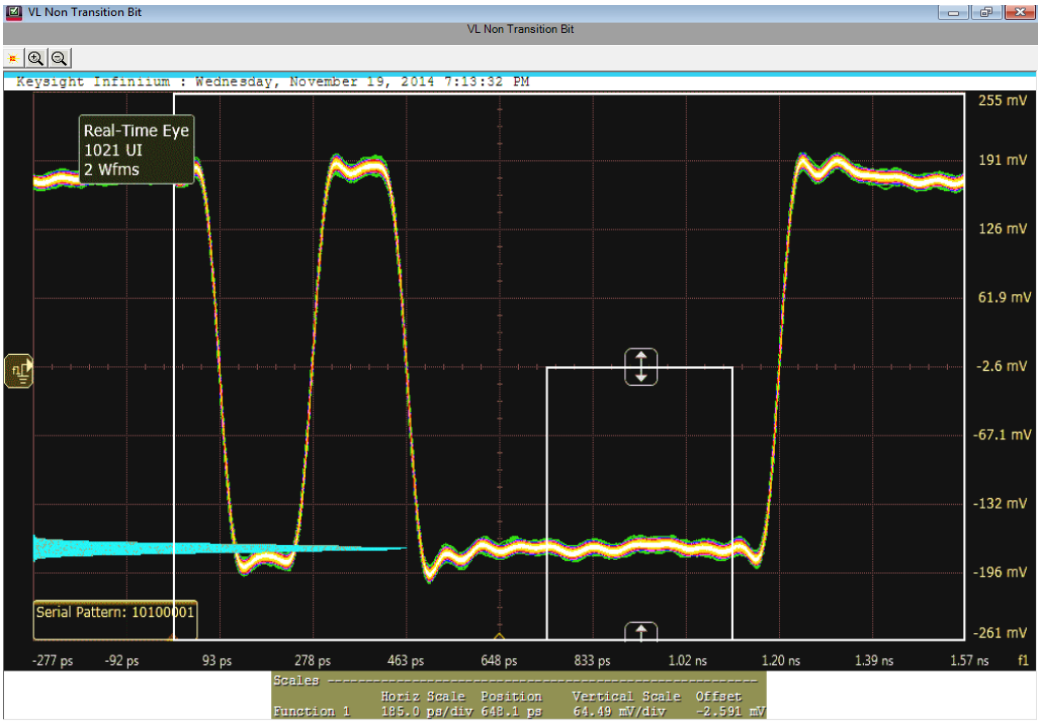

Figure 25 Reference Image for Differential Voltage Level Test – V_L Non Transition Bit

Differential Voltage Level Ratio Test

Test Overview

The Differential Voltage Level Ratio Test evaluates the differential voltage level accompanying the data transmission and ensures that differential voltage level settings are monotonic so that the sink device relies on the source device to incrementally increase upon request by the sink.

You can define the expected output for each setting of voltage level on the source, such that the output correlates with the system budget elements such as cable loss, receiver EYE minimum/maximum values and PC board transmission line loss. Furthermore, it must be kept in mind that the link must benefit when you increase level settings.

You can measure the transition and non-transition voltage swings for each supported voltage level and pre-emphasis setting. To obtain the peak to peak voltage, you must combine the High and Low voltage measurements formed within each transition and non-transition voltage swing.

Compute the peak to peak voltages for transition and non-transition voltage swing for a given voltage level and pre-emphasis level (LvlX) using the following equations:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

where $V_{T\_LvlX\_PP}$ is the peak to peak voltage at the transition bit and $V_{N\_LvlX\_PP}$ is the peak to peak voltage at the non-transition bit. The constituent voltages $V_{T\_LvlX\_H}$, $V_{T\_LvlX\_L}$, $V_{N\_LvlX\_H}$ and $V_{N\_LvlX\_L}$ are identified in the following figures showing generalized pre-emphasis and non pre-emphasized waveforms.

NOTE The condition for Level 0 pre-emphasis is identified separately in the following figures but is merely a special case. The measurement of high and low voltage values is an average value derived from a specific number of UI obtained over a certain number of required test patterns.

For PLTPAT:

There are specific qualifying patterns in the 80-Bit Custom pattern (PLTPAT) for ‘High’ and ‘Low’ voltage level measurements. These measurements require a 1-1-1-1-1-0-0-0-0-0 balanced pattern and no preconditioning is required on this pattern. The transition voltage measurements, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ is the average value over the 40% to 70% UI points in the transition bit. The

non-transition voltage measurement, $V_{N\_LvlX\_H}$ and $V_{N\_LvlX\_L}$ is the average value over three UI points ending at the 50% point of the 5th bit of the five successive transmitted 1s or 0s of the patterns. Refer to Figure 26.

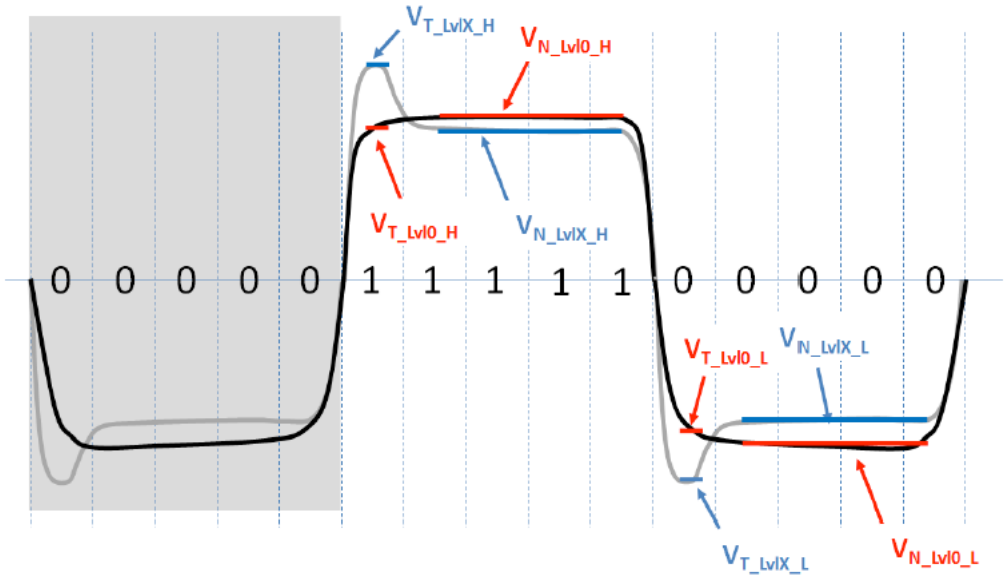

Figure 26 High and Low Voltage Measurement for PLTPAT

For PRBS7:

There are specific qualifying patterns in PRBS7 and other sequence for 'High' and 'Low' voltage level measurements. The 'High' level measurements require a 0-1-0-1-1-1-1-1-1-1 pattern and the 'Low' level measurements require a 1-0-1-0-0-0-0-0-1 pattern. Refer to Figure 27 and Figure 28. The first 3-bits in these patterns are a precondition to the transition measurements. The precondition bits for a transition to high level voltage measurement, are 0-1-0 and for a transition to low level voltage measurement are 1-0-1.

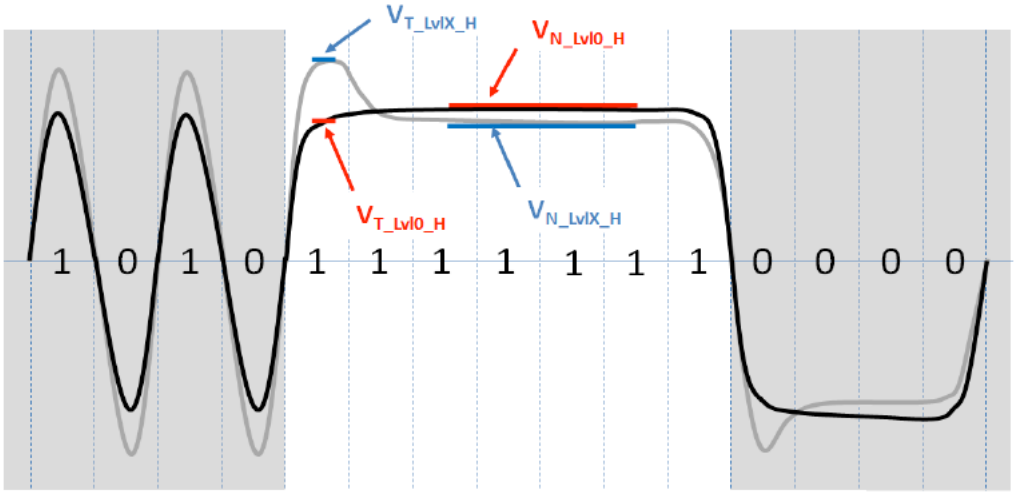

Figure 27 High Voltage Measurement for PRBS7

The transition voltage measurements, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average value over the 40% to 70% UI points in the transition bit. The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average value over three UI points ending at the 50% point of the 6th bit of the seven successive transmitted 1s of the patterns. The non-transition voltage measurement, $V_{N\_LvlX\_L}$ is the average value over two UI points ending at 50% point of the 4th bit of the four successive transmitted 0s of the patterns.

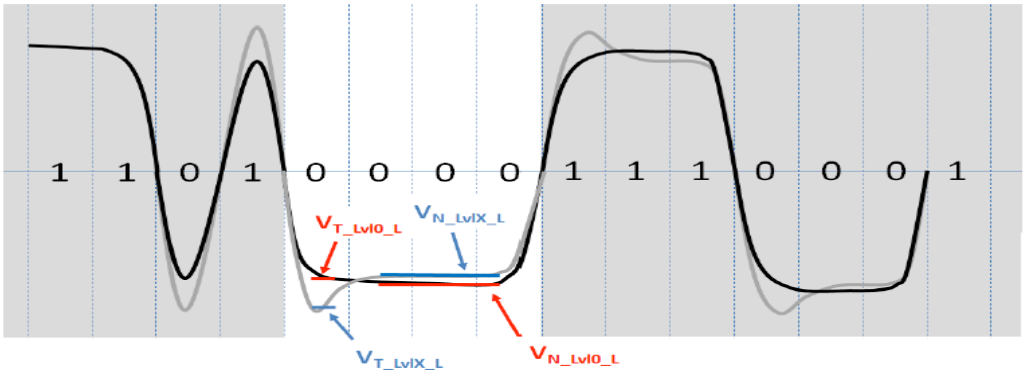

Figure 28 Low Voltage Measurement for PRBS7

For each voltage level and pre-emphasis level setting that you use to run tests, use the following equation to compute Differential Voltage Level Ratio:

$$Differential\ Voltage\ Level\ Ratio = 20 * Log_{10}[V_{PP\_LevelA} / V_{PP\_LevelB}]$$

The following table identifies the peak to peak voltage level A and peak to peak voltage level B used in the calculation of the Differential Voltage Level Ratio.

Measurement	Peak to Peak Voltage Level A	Peak to Peak Voltage Level B
1	Level 1	Level 0
2	Level 2	Level 1
3	Level 3	Level 2

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3	
Bit Rate	All bit rates are supported.	
Voltage Level and Pre-emphasis Level	Any Voltage level and Pre-Emphasis level that are compliant to all normative tests run on the Source.	
SSC	If the DUT can operate in either the SSC-enabled or the SSC-disabled state, it shall be tested in both conditions.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal for Level A.

2 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.

3 Measure the data rate and validate the test pattern.

4 Acquire the qualifying test pattern over the specific number of required patterns to measure the high voltage level.

5 Set up the Histogram to measure the average value of high voltage level for both transition and non-transition voltage levels.

6 Acquire the qualifying test pattern over the specific number of required patterns to measure the low voltage level.

7 Set up the Histogram to measure the average value of low voltage level for both transition and non-transition voltage levels.

8 Compute the peak to peak voltage level A from the peak to peak voltage for non-transition voltage measurement using the following equation:

$$V_{PP\_LevelA} = V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

9 Validate and acquire the signal for Level B.

10 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.

11 Measure the data rate and validate the test pattern.

12 Acquire the qualifying test pattern over the specific number of required patterns to measure the high voltage level.

13 Set up the Histogram to measure the average value of high voltage level for both transition and non-transition voltage levels.

14 Acquire the qualifying test pattern over the specific number of required patterns to measure the low voltage level.

15 Set up the Histogram to measure the average value of low voltage level for both transition and non-transition voltage levels.

16 Compute the peak to peak voltage level B from the peak to peak voltage for non-transition voltage measurement using the following equation:

$$V_{PP\_LevelB} = V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

17 Compute the differential voltage level ratio using the following equation:

$$Differential\ Voltage\ Level\ Ratio = 20 * Log_{10}[V_{PP\_LevelA} / V_{PP\_LevelB}]$$

Viewing Test Results

The measured value of the differential voltage level ratio for the test signal must fall within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

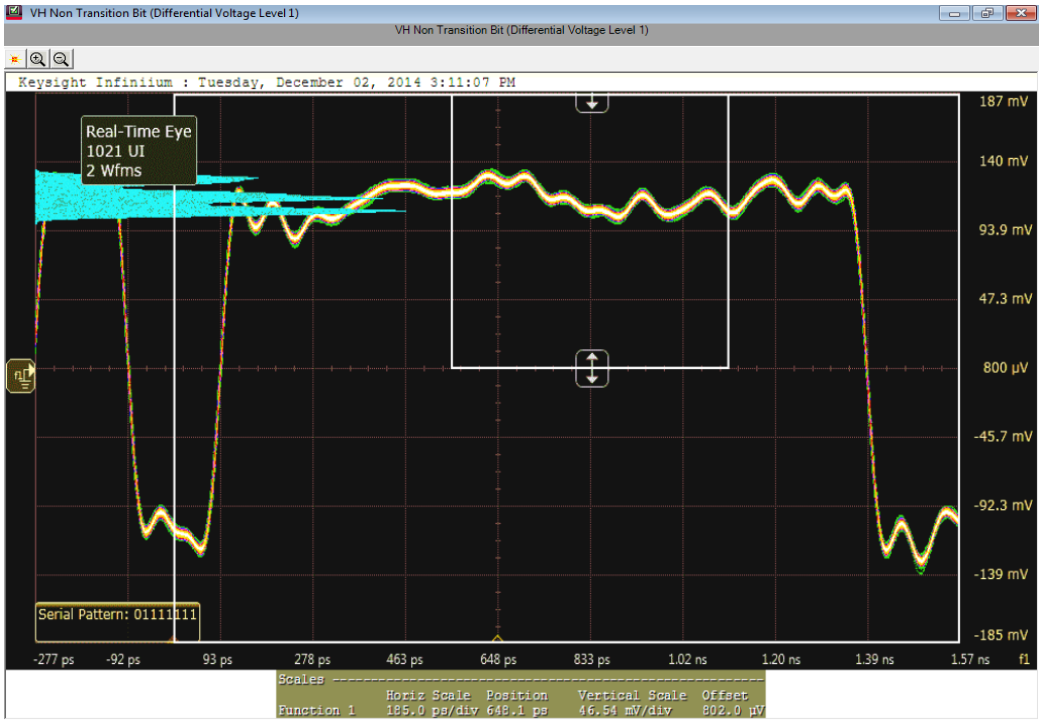

Figure 29 Reference Image for Differential Voltage Level Ratio Test: V_H Non Transition Bit (Level 1)

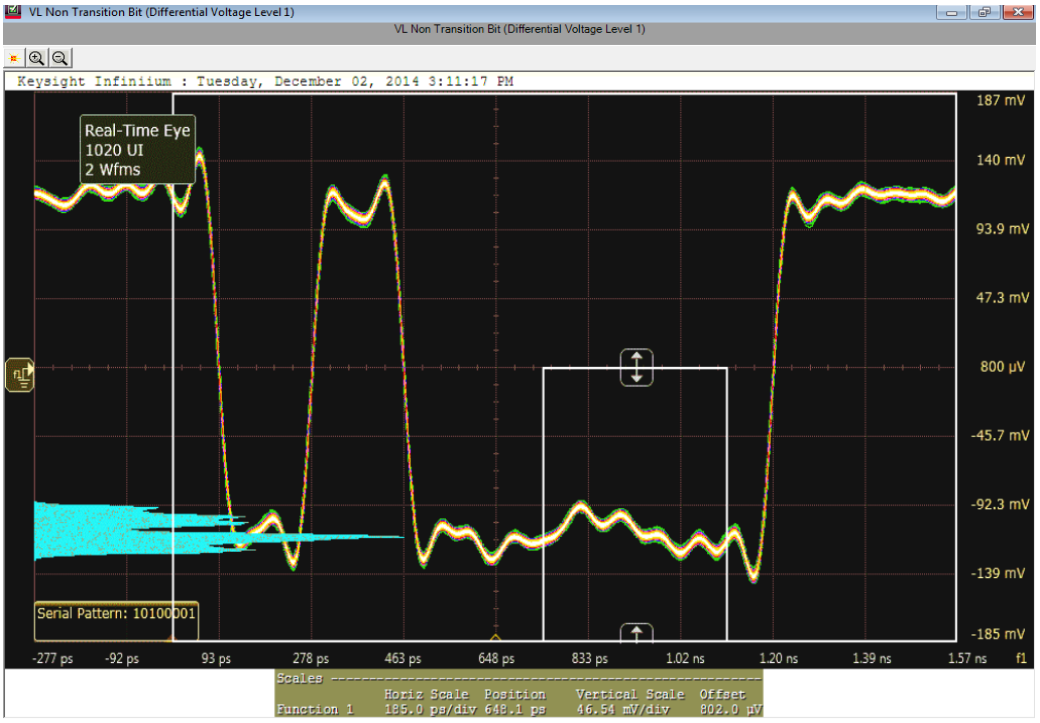

Figure 30 Reference Image for Differential Voltage Level Ratio Test – V_L Non Transition Bit (Level 1)

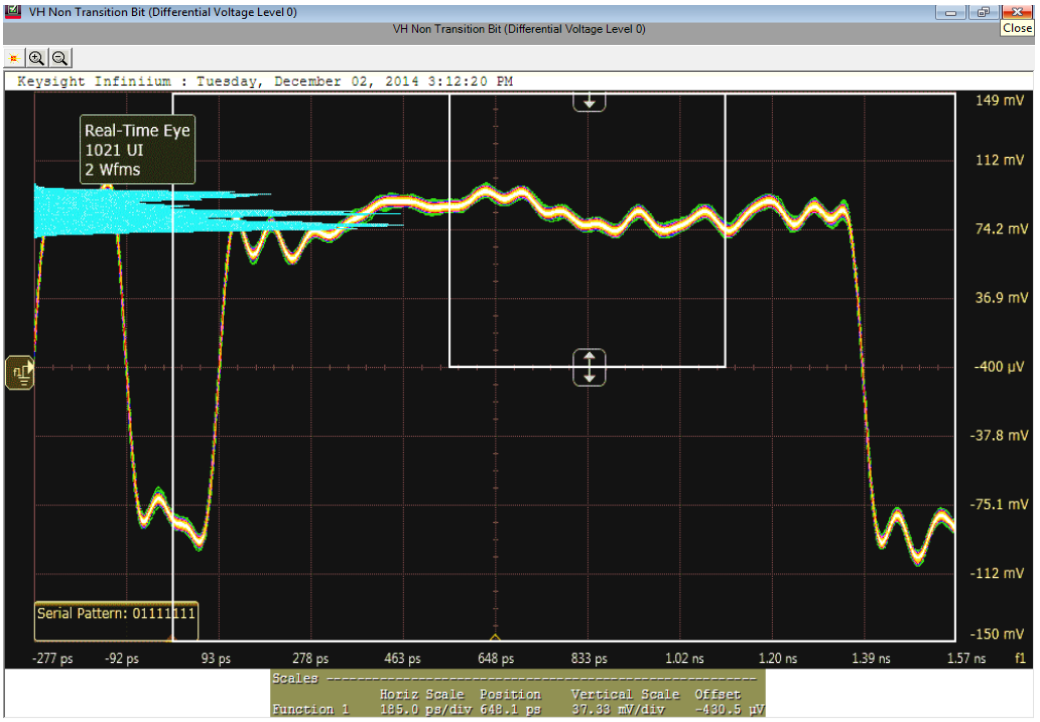

Figure 31 Reference Image for Differential Voltage Level Ratio Test – V_H Non Transition Bit (Level 0)

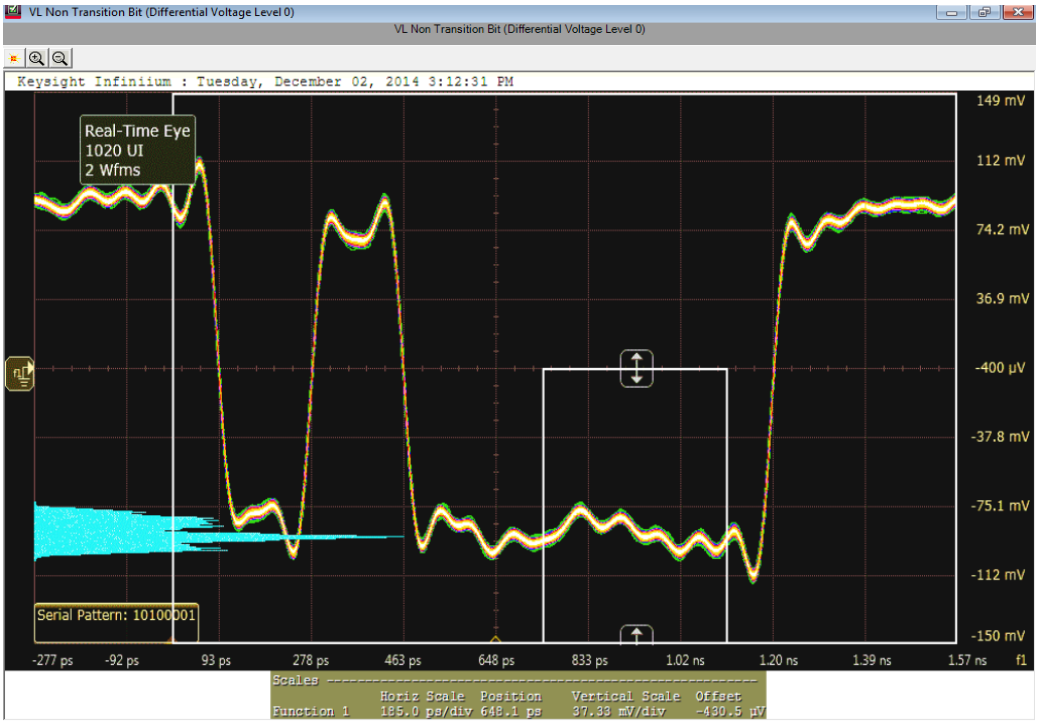

Figure 32 Reference Image for Differential Voltage Level Ratio Test – V_L Non Transition Bit (Level 0)

Pre-Emphasis Level Test

Test Overview

The Pre-Emphasis level Test evaluates the differential voltage level accompanying the data transmission. In other words, this test evaluates the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to validate the accuracy of the pre-emphasis setting.

You can define settings on the source making it capable to pre-emphasize the main link waveform to overcome system losses, for example, losses through PC boards, connectors, and cables. The eDP standard stipulates the relative magnitude of the waveform to overcome specific losses. As pre-emphasis is negotiable, you may enable interoperability within two units, which have substantially different degrees of pre-emphasis, by operating them at different settings. This test ensures that the DUT is compliant to the levels of system loss or the pre-emphasis budget. Also, you may ensure that the any increase in the pre-emphasis setting provides a improved signal to the sink.

You can measure the transition and non-transition voltage swings for each supported voltage level and pre-emphasis setting. To obtain the peak to peak voltage, you must combine the High and Low voltage measurements formed within each transition and non-transition voltage swing.

Compute the peak to peak voltages for transition and non-transition voltage swing for a given voltage level and pre-emphasis level (LvlX) using the following equations:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

where $V_{T\_LvlX\_PP}$ is the peak to peak voltage at the transition bit and $V_{N\_LvlX\_PP}$ is the peak to peak voltage at the non-transition bit. The constituent voltages $V_{T\_LvlX\_H}$, $V_{T\_LvlX\_L}$, $V_{N\_LvlX\_H}$ and $V_{N\_LvlX\_L}$ are identified in the following figures showing generalized pre-emphasis and non pre-emphasized waveforms.

NOTE The condition for Level 0 pre-emphasis is identified separately in the following figures but is merely a special case. The measurement of high and low voltage values is an average value derived from a specific number of UI obtained over a certain number of required test patterns.

For PLTPAT:

There are specific qualifying patterns in the 80-Bit Custom pattern (PLTPAT) for 'High' and 'Low' pre-emphasis level measurements. These measurements require a 1-1-1-1-1-0-0-0-0-0 balanced pattern and no preconditioning is required on this pattern. The transition voltage measurements, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ is the average value over the 40% to 70% UI points in the transition bit. The

non-transition voltage measurement, $V_{N\_LvlX\_H}$ and $V_{N\_LvlX\_L}$ is the average value over three UI points ending at the 50% point of the 5th bit of the five successive transmitted 1s or 0s of the patterns. Refer to Figure 33.

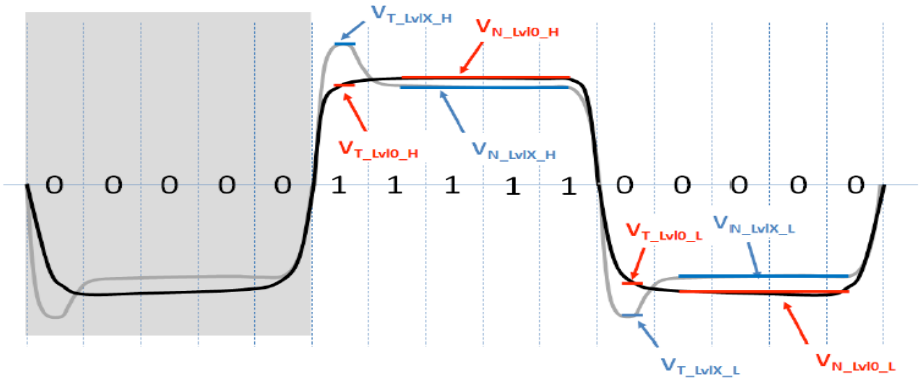

Figure 33 High and Low Voltage Measurement for PLTPAT

For PRBS7:

There are specific qualifying patterns in PRBS7 and other sequence for 'High' and 'Low' voltage level measurements. The 'High' level measurements require a 0-1-0-1-1-1-1-1-1-1 pattern and the 'Low' level measurements require a 1-0-1-0-0-0-0-1 pattern. Refer to Figure 34 and Figure 35. The first 3-bits in these patterns are a precondition to the transition measurements. The precondition bits for a transition to high level voltage measurement, are 0-1-0 and for a transition to low level voltage measurement are 1-0-1.

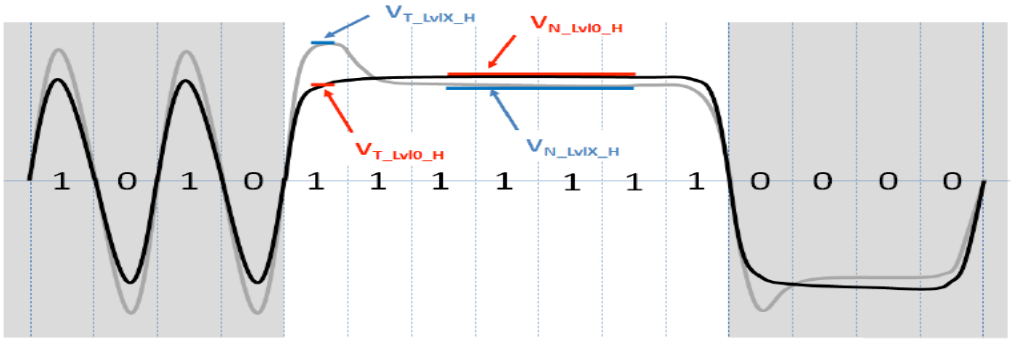

Figure 34 High Voltage Measurement for PRBS7

The transition voltage measurements, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average value over the 40% to 70% UI points in the transition bit. The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average value over three UI points ending at the 50% point of the 6th bit of the seven successive transmitted 1s of the patterns. The non-transition voltage measurement, $V_{N\_LvlX\_L}$ is the average value over two UI points ending at 50% point of the 4th bit of the four successive transmitted 0s of the patterns.

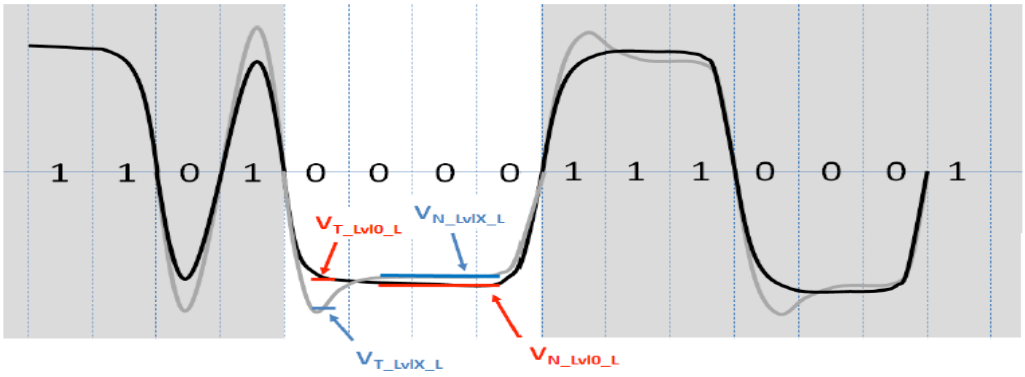

Figure 35 Low Voltage Measurement for PRBS7

For each voltage level and pre-emphasis level setting that you use to run tests, use the following equation to compute Pre-Emphasis level:

$$Pre\text{-}Emphasis\ Level = 20 * Log_{10}[V_{T\_LvlX\_PP} / V_{N\_LvlX\_PP}]$$

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3	
Bit Rate	All bit rates are supported.	
Voltage Level and Pre-emphasis Level	Any Voltage level and Pre-Emphasis level that are compliant to all normative tests run on the Source.	
SSC	If the DUT can operate in either the SSC-enabled or the SSC-disabled state, it shall be tested in both conditions.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal.
2 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.
3 Measure the data rate and validate the test pattern.
4 Acquire the qualifying test pattern over the specific number of required patterns to measure the high voltage level.
5 Set up the Histogram to measure the average value of high voltage level for both transition and non-transition voltage levels.
6 Acquire the qualifying test pattern over the specific number of required patterns to measure the low voltage level.

7 Set up the Histogram to measure the average value of low voltage level for both transition and non-transition voltage levels.

8 Compute the value of peak to peak voltage for both transition and non-transition voltage levels using the following equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

9 Compute the value of pre-emphasis level from the peak to peak voltage for both transition and non-transition voltage levels using the following equation:

$$Pre\text{-}Emphasis\ Level = 20 * Log_{10}[V_{T\_LvlX\_PP} / V_{N\_LvlX\_PP}]$$

Viewing Test Results

The measured value of the pre-emphasis level for the test signal must fall within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

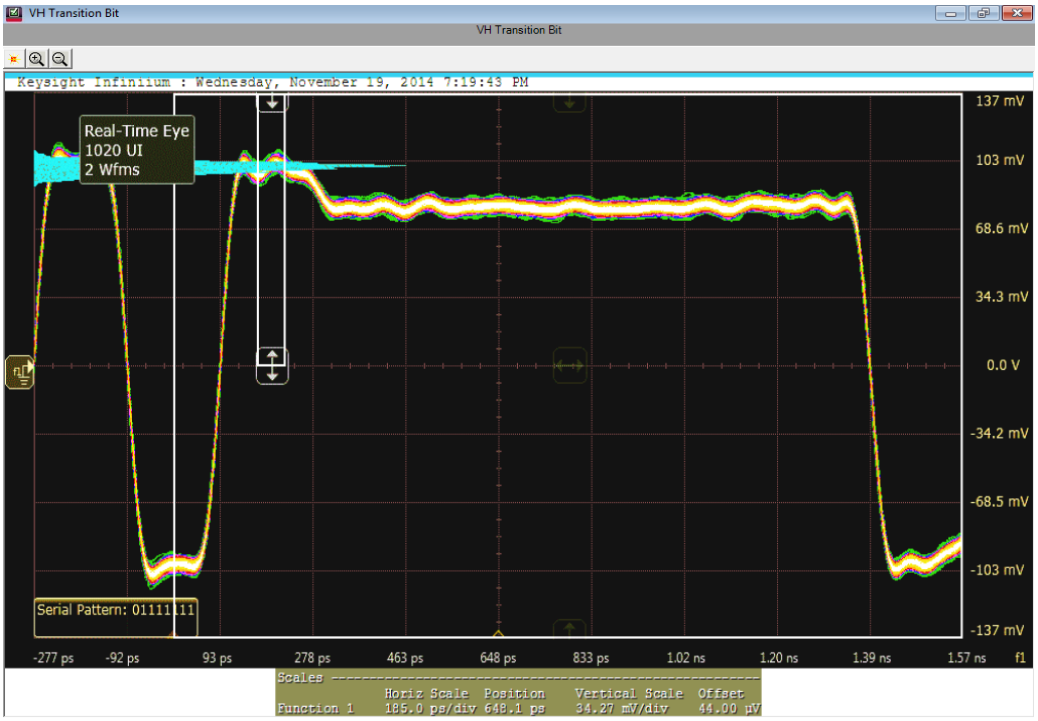

Figure 36 Reference Image for Pre-Emphasis Level Test – V_H Transition Bit

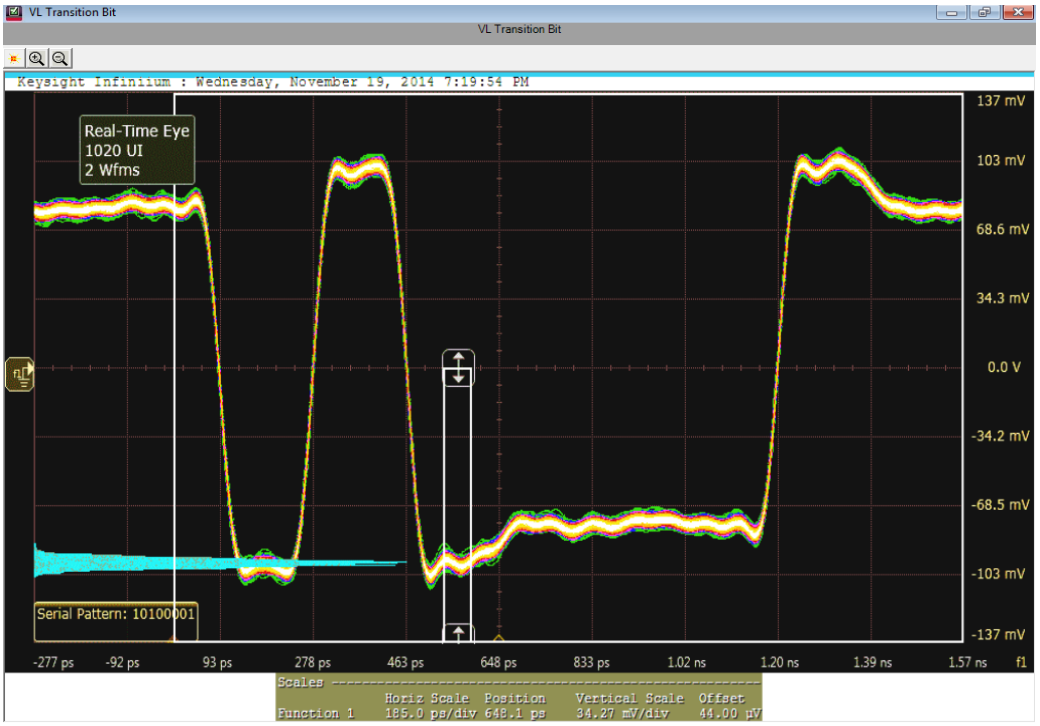

Figure 37 Reference Image for Pre-Emphasis Level Test – V_L Transition Bit

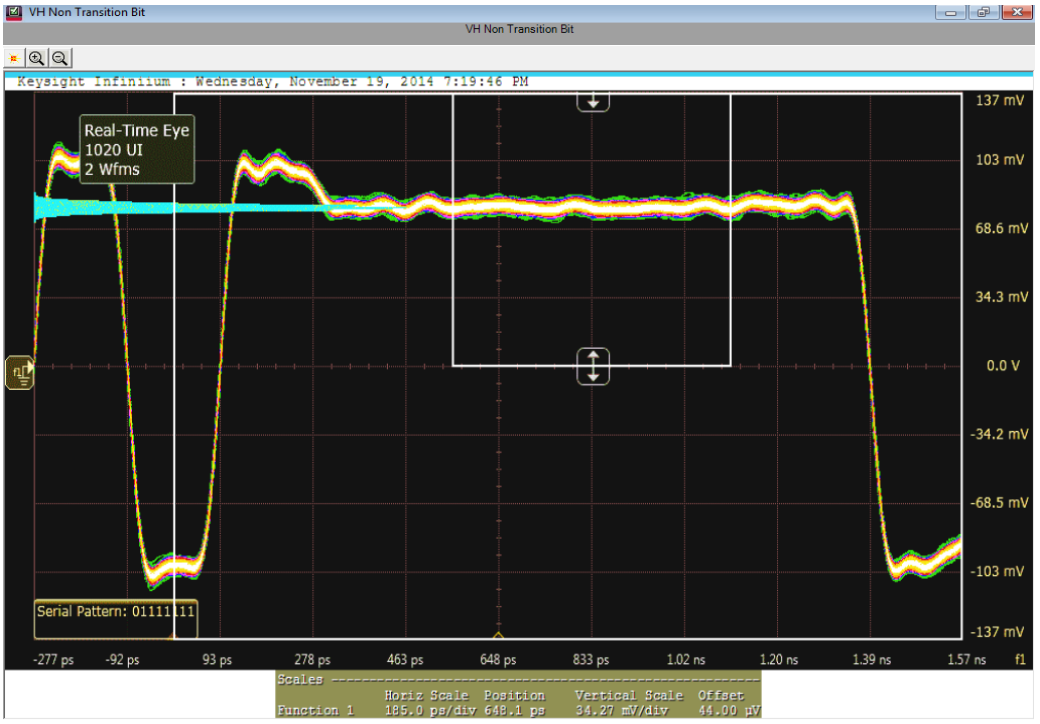

Figure 38 Reference Image for Pre-Emphasis Level Test – V_H Non Transition Bit

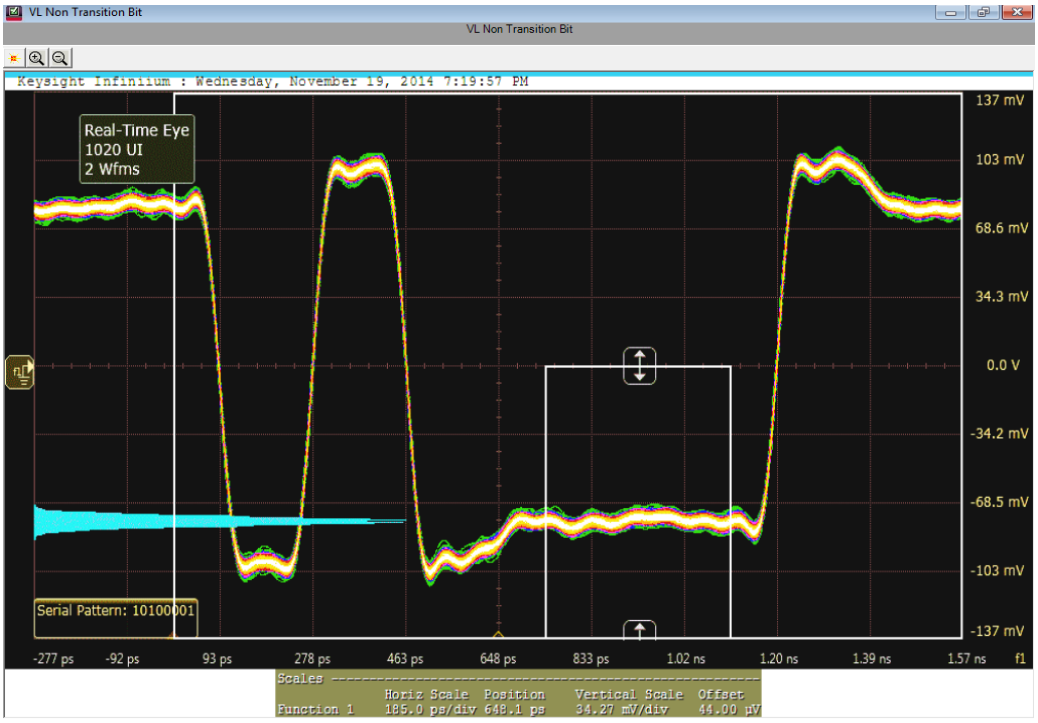

Figure 39 Reference Image for Pre-Emphasis Level Test – V_H Non Transition Bit

Pre-Emphasis Level Delta Test

Test Overview

The Pre-Emphasis Level Delta Test evaluates the differential voltage level accompanying the data transmission. This test also evaluates the effect of pre-emphasis of the Source waveform by measuring the peak differential amplitude to ensure accuracy in the pre-emphasis setting.

You can define settings on the source making it capable to pre-emphasize the main link waveform to overcome system losses, for example, losses through PC boards, connectors, and cables. The eDP standard stipulates the relative magnitude of the waveform to overcome specific losses. As pre-emphasis is negotiable, you may enable interoperability within two units, which have substantially different degrees of pre-emphasis, by operating them at different settings. This test ensures that the DUT is compliant to the levels of system loss or the pre-emphasis budget. Also, you may ensure that the any increase in the pre-emphasis setting provides a improved signal to the sink.

You can measure the transition and non-transition voltage swings for each supported voltage level and pre-emphasis setting. To obtain the peak to peak voltage, you must combine the High and Low voltage measurements formed within each transition and non-transition voltage swing.

Compute the peak to peak voltages for transition and non-transition voltage swing for a given voltage level and pre-emphasis level (LvlX) using the following equations:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

where $V_{T\_LvlX\_PP}$ is the peak to peak voltage at the transition bit and $V_{N\_LvlX\_PP}$ is the peak to peak voltage at the non-transition bit. The constituent voltages $V_{T\_LvlX\_H}$, $V_{T\_LvlX\_L}$, $V_{N\_LvlX\_H}$ and $V_{N\_LvlX\_L}$ are identified in the following figures showing generalized pre-emphasis and non pre-emphasized waveforms.

NOTE The condition for Level 0 pre-emphasis is identified separately in the following figures but is merely a special case. The measurement of high and low voltage values is an average value derived from a specific number of UI obtained over a certain number of required test patterns.

For PLTPAT:

There are specific qualifying patterns in the 80-Bit Custom pattern (PLTPAT) for 'High' and 'Low' pre-emphasis level measurements. These measurements require a 1-1-1-1-1-0-0-0-0-0 balanced pattern and no preconditioning is required on this pattern. The transition voltage measurements, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ is the average value over the 40% to 70% UI points in the transition bit. The

non-transition voltage measurement, $V_{N\_LvlX\_H}$ and $V_{N\_LvlX\_L}$ is the average value over three UI points ending at the 50% point of the 5th bit of the five successive transmitted 1s or 0s of the patterns. Refer to Figure 40.

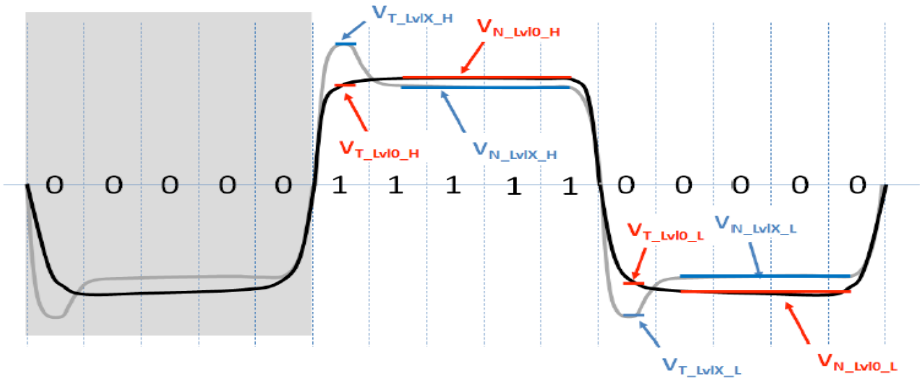

Figure 40 High and Low Voltage Measurement for PLTPAT

For PRBS7:

There are specific qualifying patterns in PRBS7 and other sequence for 'High' and 'Low' voltage level measurements. The 'High' level measurements require a 0-1-0-1-1-1-1-1-1-1 pattern and the 'Low' level measurements require a 1-0-1-0-0-0-0-1 pattern. Refer to Figure 41 and Figure 42. The first 3-bits in these patterns are a precondition to the transition measurements. The precondition bits for a transition to high level voltage measurement, are 0-1-0 and for a transition to low level voltage measurement are 1-0-1.

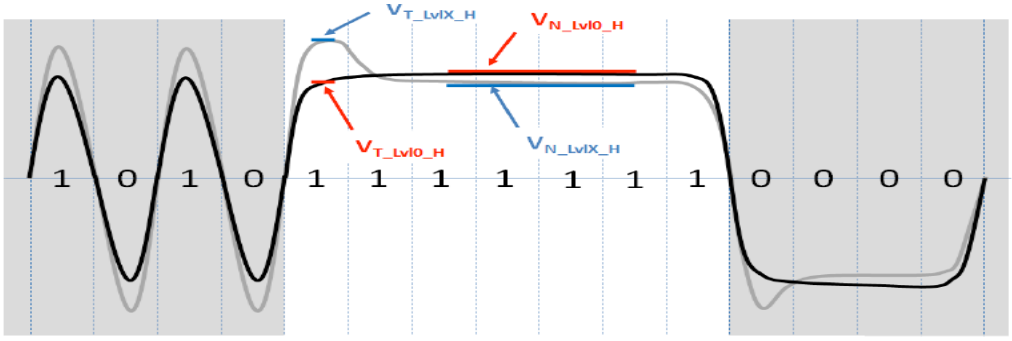

Figure 41 High Voltage Measurement for PRBS7

The transition voltage measurements, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average value over the 40% to 70% UI points in the transition bit. The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average value over three UI points ending at the 50% point of the 6th bit of the seven successive transmitted 1s of the patterns. The non-transition voltage measurement, $V_{N\_LvlX\_L}$ is the average value over two UI points ending at 50% point of the 4th bit of the four successive transmitted 0s of the patterns.

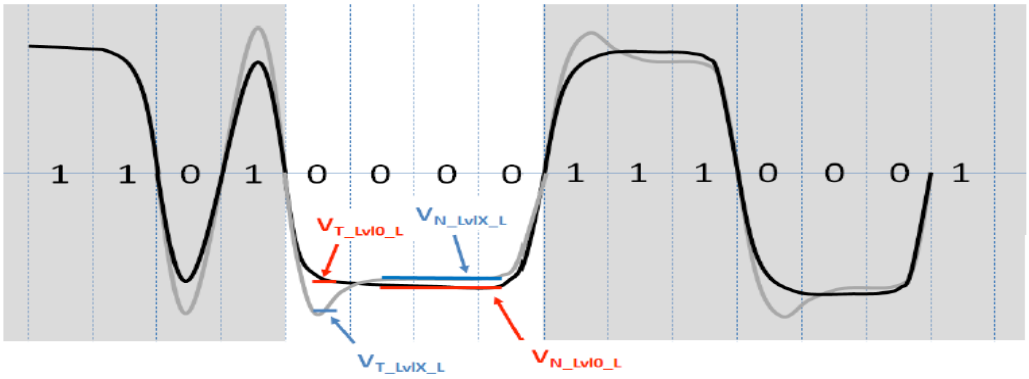

Figure 42 Low Voltage Measurement for PRBS7

For each voltage level and pre-emphasis level setting that you use to run tests, use the following equation to compute Pre-Emphasis level:

$$Pre\text{-}Emphasis\ Level = 20 * Log_{10}[V_{T\_LvlX\_PP} / V_{N\_LvlX\_PP}]$$

Compute the Pre-Emphasis Level Delta using the following equation:

$$Pre\text{-}Emphasis\ Level\ Delta = Pre\text{-}Emphasis\ Level\ A - Pre\text{-}Emphasis\ Level\ B$$

The following table identifies the pre-emphasis level A and pre-emphasis level B used to calculate the Pre-Emphasis Level Delta.

Measurement	Pre-Emphasis Level A	Pre-Emphasis Level B
1	Level 1	Level 0
2	Level 2	Level 1
3	Level 3	Level 2

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3	
Bit Rate	All bit rates are supported.	
Voltage Level and Pre-emphasis Level	Any Voltage level and Pre-Emphasis level that are compliant to all normative tests run on the Source.	
SSC	If the DUT can operate in either the SSC-enabled or the SSC-disabled state, it shall be tested in both conditions.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal for Pre-Emphasis Level A.

2 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.

3 Measure the data rate and validate the test pattern.

4 Acquire the qualifying test pattern over the specific number of required patterns to measure the high voltage level.

5 Set up the Histogram to measure the average value of high voltage level for both transition and non-transition voltage levels.

6 Acquire the qualifying test pattern over the specific number of required patterns to measure the low voltage level.

7 Set up the Histogram to measure the average value of low voltage level for both transition and non-transition voltage levels.

8 Compute the peak to peak voltage for both transition and non-transition voltage measurements using the following equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

9 Compute the Pre-Emphasis Level A from the peak to peak voltage for both transition and non-transition voltage measurements using the following equation:

$$Pre\text{-}Emphasis\ Level\ A = 20 * Log_{10}[V_{T\_LvlX\_PP} / V_{N\_LvlX\_PP}]$$

10 Validate and acquire the signal for Pre-Emphasis Level B.

11 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.

12 Measure the data rate and validate the test pattern.

13 Acquire the qualifying test pattern over the specific number of required patterns to measure the high voltage level.

14 Set up the Histogram to measure the average value of high voltage level for both transition and non-transition voltage levels.

15 Acquire the qualifying test pattern over the specific number of required patterns to measure the low voltage level.

16 Set up the Histogram to measure the average value of low voltage level for both transition and non-transition voltage levels.

17 Compute the peak to peak voltage for both transition and non-transition voltage measurements using the following equations:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

18 Compute the Pre-Emphasis level B from the peak to peak voltage for both transition and non-transition voltage measurements using the following equation:

$$Pre\text{-}Emphasis\ Level\ B = 20 * Log_{10}[V_{T\_LvlX\_PP} / V_{N\_LvlX\_PP}]$$

19 Compute the value for Pre-Emphasis Level Delta from Pre-Emphasis Level A and Pre-Emphasis Level B values using the following equation:

$$Pre\text{-}Emphasis\ Level\ Delta = Pre\text{-}Emphasis\ Level\ A - Pre\text{-}Emphasis\ Level\ B$$

Viewing Test Results

The measured value of pre-emphasis level delta for the test signal must fall within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

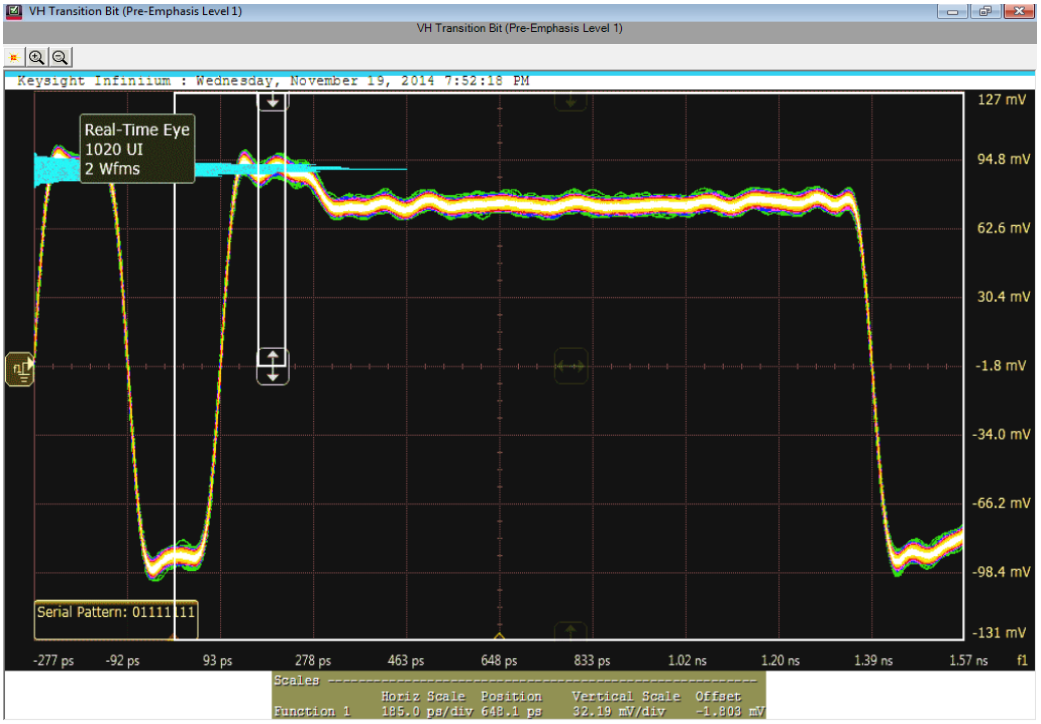

Figure 43 Reference Image for Pre-Emphasis Level Delta Test – V_H Transition Bit (Level 1)

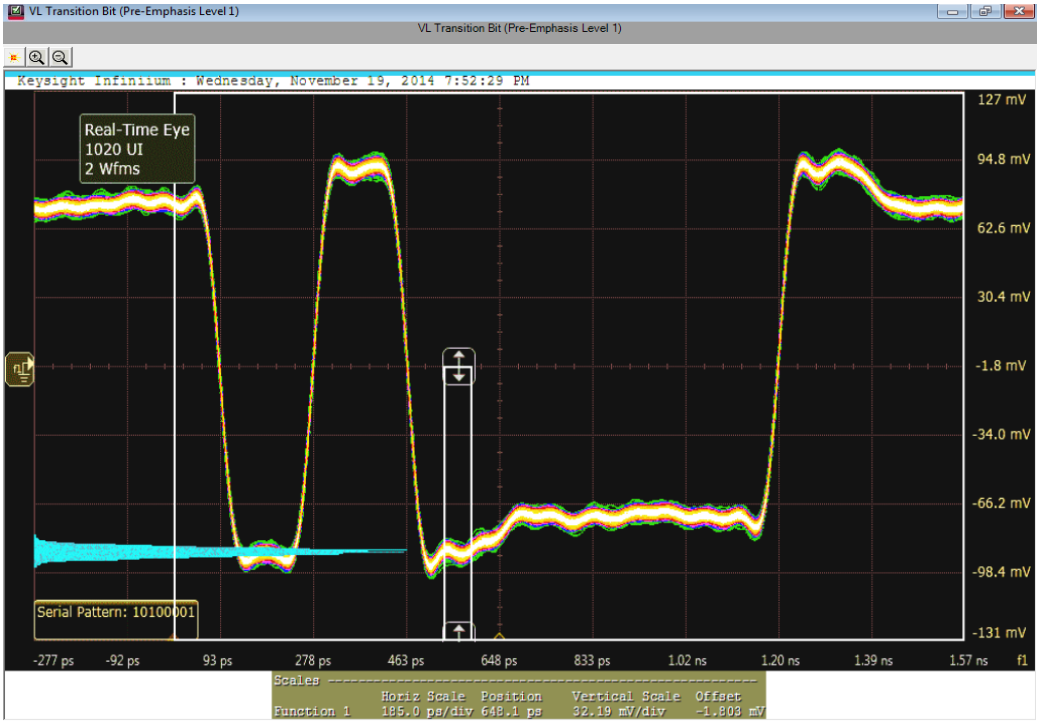

Figure 44 Reference Image for Pre-Emphasis Level Delta Test – V_L Transition Bit (Level 1)

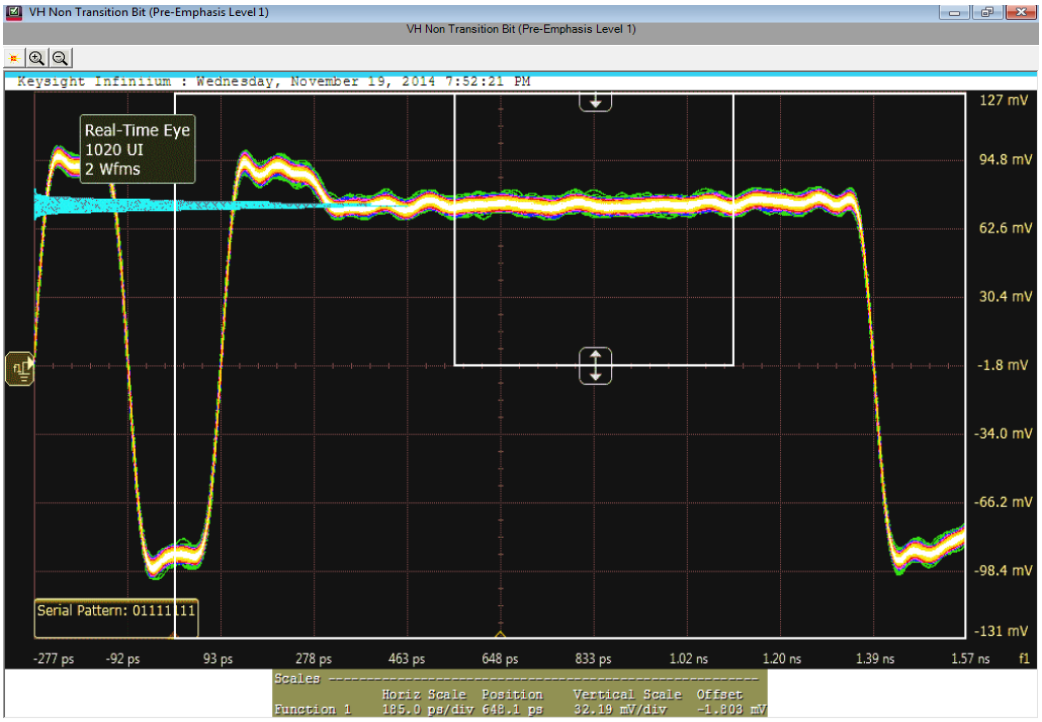

Figure 45 Reference Image for Pre-Emphasis Level Delta Test – V_H Non Transition Bit (Level 1)

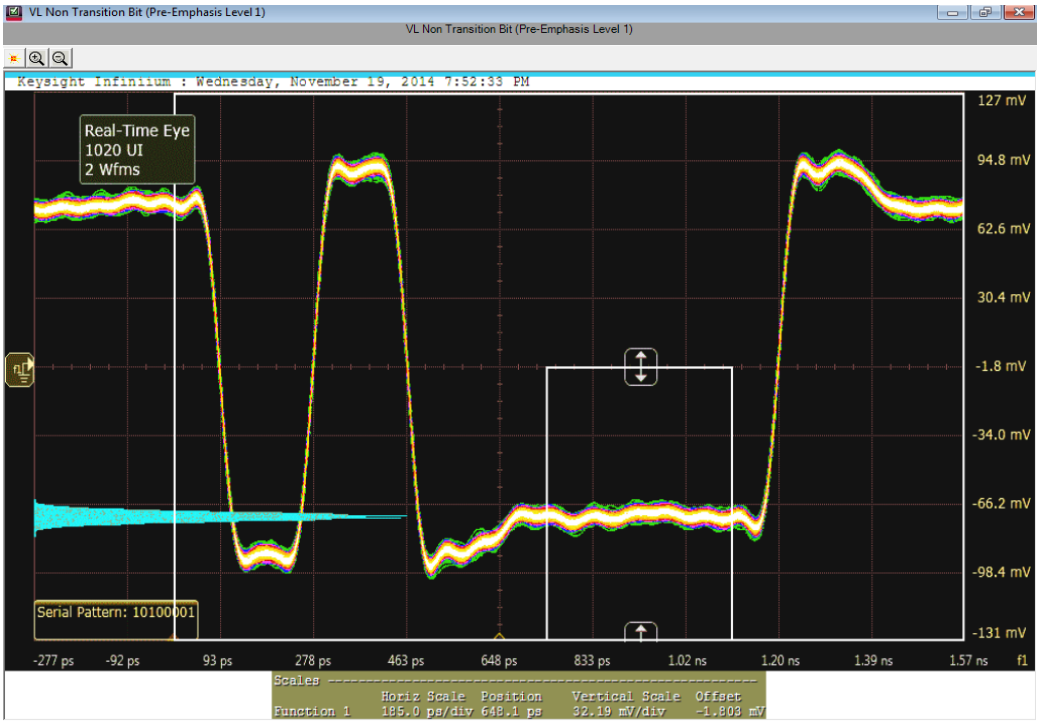

Figure 46 Reference Image for Pre-Emphasis Level Delta Test – V_L Non Transition Bit (Level 1)

Figure 47 Reference Image for Pre-Emphasis Level Delta Test – V_H Transition Bit (Level 0)

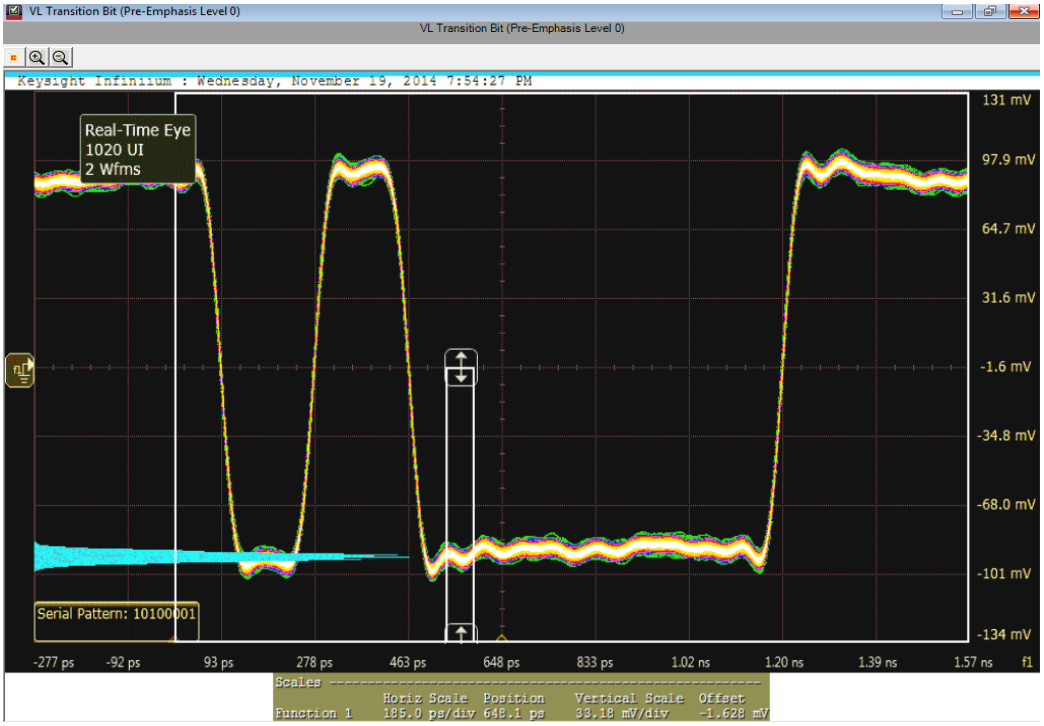

Figure 48 Reference Image for Pre-Emphasis Level Delta Test – V_L Transition Bit (Level 0)

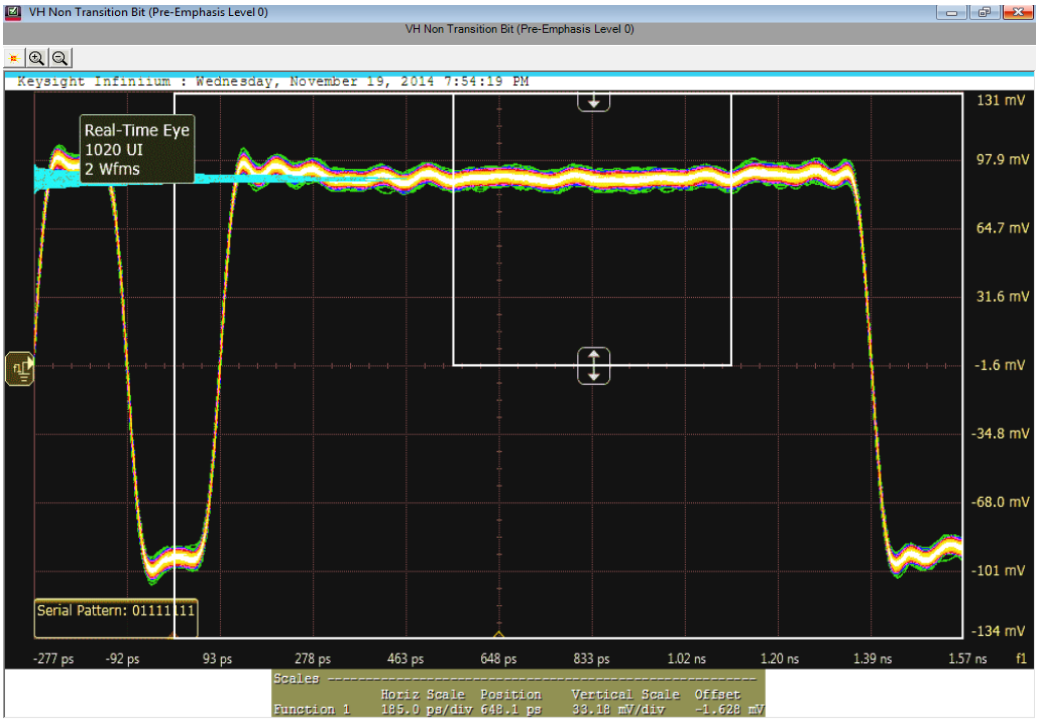

Figure 49 Reference Image for Pre-Emphasis Level Delta Test – V_H Non Transition Bit (Level 0)

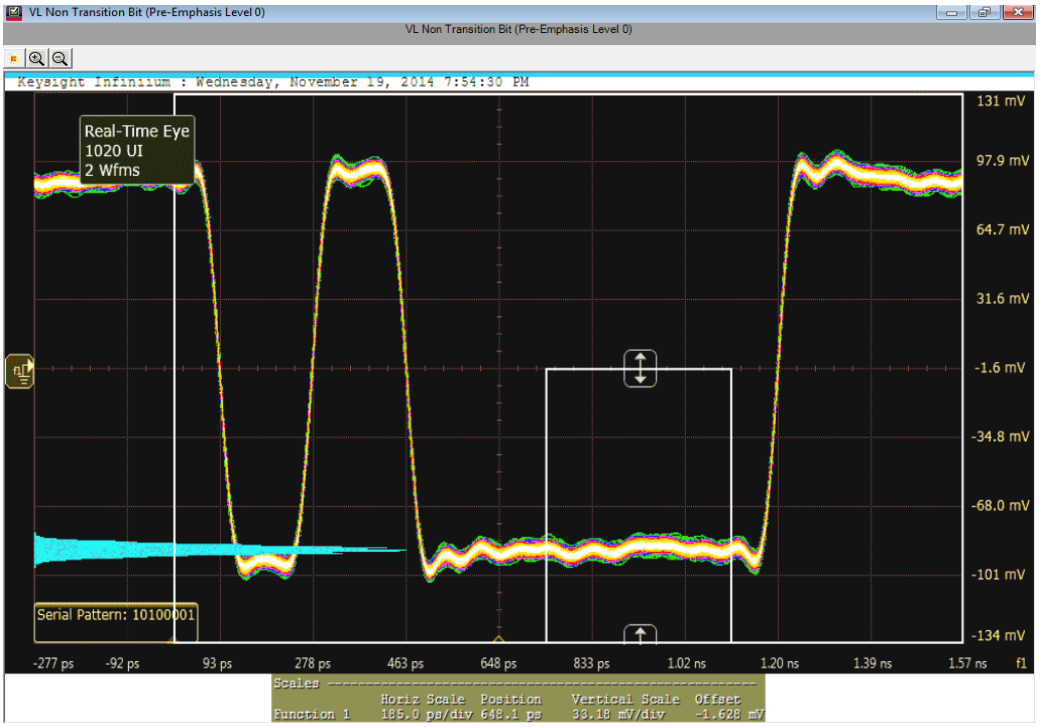

Figure 50 Reference Image for Pre-Emphasis Level Delta Test – V_L Non Transition Bit (Level 0)

Rise/Fall Time Test

Test Overview

The Rise/Fall Time Test evaluates the differential rise and fall time of the main link data lanes. The differential transition time is useful in predicting the Electromagnetic Interference (EMI)/Radio-Frequency Interference (RFI) performance of the channels.

Reduction in the differential transition time increases the eye opening. However, it also increases the time domain crosstalk which, decreases the margin and increases risks of higher EMI/RFI, depending on the type of coupling.

For each lane, use the differential voltage level values to calculate the High and Low levels of differential transition time. The rise time is measured between 20% to 80% of V_L to V_H transition and fall time is measured between 80% to 20% of V_H to V_L transition. The application reports the minimum, maximum and average differential rise and fall time values.

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3	
Bit Rate	Highest bit rate is supported.	
Voltage Level and Pre-emphasis Level	Voltage Level: Level 2 Pre-emphasis Level: Level 0	
SSC	If the DUT can operate in either the SSC-enabled or the SSC-disabled state, it shall be tested in both conditions.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal.
2 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.
3 Measure the data rate and validate the test pattern.
4 Acquire the qualifying test pattern over the specific number of required patterns to measure the high voltage level.
5 Set up the Histogram to measure the average value of high voltage level for both transition and non-transition voltage levels.
6 Acquire the qualifying test pattern over the specific number of required patterns to measure the low voltage level.
7 Set up the Histogram to measure the average value of low voltage level for both transition and non-transition voltage levels.
8 Set up the measurement top and base voltage levels based on the High and Low voltage levels.
9 Set up the measurement threshold to 20%, 50%, 80% of top and base voltage levels.
10 Measure the rise time or fall time of the differential signal.

Viewing Test Results

The measured value of the rise time / fall time for the test signal must fall within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

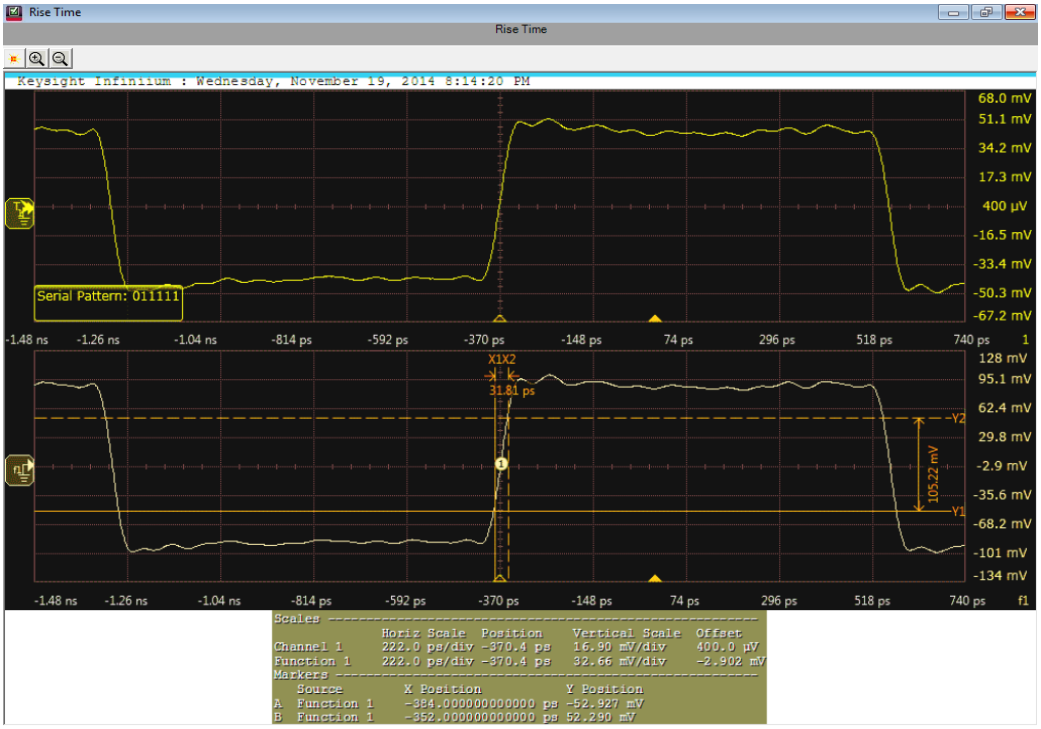

Figure 51 Reference Image for Rise Time Test

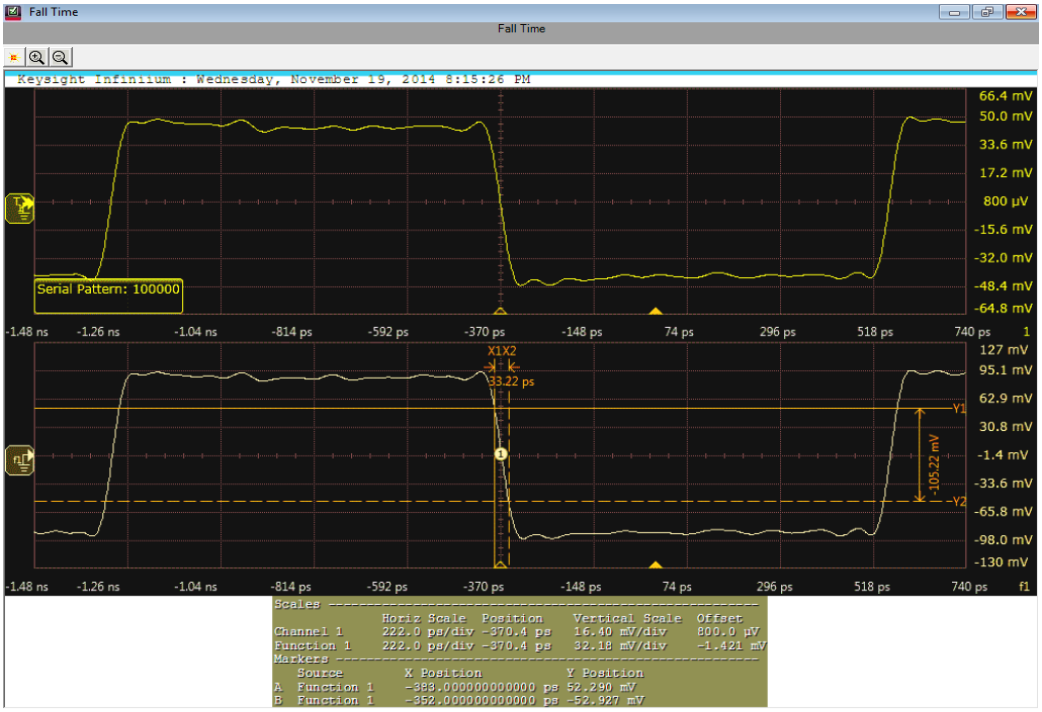

Figure 52 Reference Image for Fall Time Test

Inter Pair Skew Test

Test Overview

The Inter Pair Skew Test evaluates the skew, or time delay, between differential data lanes in the eDP interface.

The eDP interface has the ability to skew or deskew lanes to eliminate simultaneous degradation of concurrent bytes of transmitted data. It is essential to ensure that the combined components of the system do not exceed the elasticity of the receiver.

You may capture waveforms on two lanes simultaneously, which are set up on two measurement channels. Evaluate both waveforms at a common point and measure the time difference between the corresponding edges at the transition point. Locate each edge by determining the point where the waveform crosses the transition amplitude.

$$V_{Transition} = 0 \text{ Volts}$$

The VESA DisplayPort Standard specifies an offset of 20 UI from Lane 0 to Lane 1, Lane 1 to Lane 2 and from Lane 2 to Lane 3. The resultant offset is cumulative, which indicates that the offset between Lane 0 and Lane 2 is 40 UI. Nominal Skew is same as the expected offset between the tested lanes.

$$Inter\ Lane\ Skew = \{1 / NumEdges\}\Sigma \mid T_{Transition\_LaneA} - T_{Transition\_LaneB} \mid - Nominal\ Skew$$

Operation Type	Lane Direction	Lane A	Lane B
Two Lane Operation	Lane 0 to Lane 1	Lane 0	Lane 1
Four Lane Operation	Lane 0 to Lane 1	Lane 0	Lane 1
	Lane 0 to Lane 2	Lane 0	Lane 2
	Lane 0 to Lane 3	Lane 0	Lane 3
	Lane 1 to Lane 2	Lane 1	Lane 2
	Lane 1 to Lane 3	Lane 1	Lane 3
	Lane 2 to Lane 3	Lane 2	Lane 3

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3	
Bit Rate	Highest bit rate is supported.	
Voltage Level and Pre-emphasis Level	Voltage Level: Level 2 Pre-emphasis Level: Level 0	
SSC	If the DUT can operate in either the SSC-enabled or the SSC-disabled state, it shall be tested in both conditions.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal for Lane A.
2 Determine the threshold of the signal by measuring V_{Top} and V_{Base} for Lane A.
3 Measure the data rate and validate the test pattern for Lane A.
4 Validate and acquire the signal for Lane B.
5 Determine the threshold of the signal by measuring V_{Top} and V_{Base} for Lane B.
6 Measure the data rate and validate the test pattern for Lane B.
7 Decode signal for Lane A and Lane B.
8 Search for the inter pair skew pattern from the decoded signal for Lane A and Lane B.
9 Compute the time difference between the corresponding edges at the transition point of Lane A and Lane B.
10 Compute the Inter Lane Skew using the following equation:

$$Inter\ Lane\ Skew = \{1 / NumEdges\}\Sigma \mid T_{Transition\_LaneA} - T_{Transition\_LaneB} \mid - Nominal\ Skew$$

where, Nominal Skew is the expected inter pair skew between Lane A and Lane B.

Viewing Test Results

The measured value of the inter pair skew for the test signal must fall within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

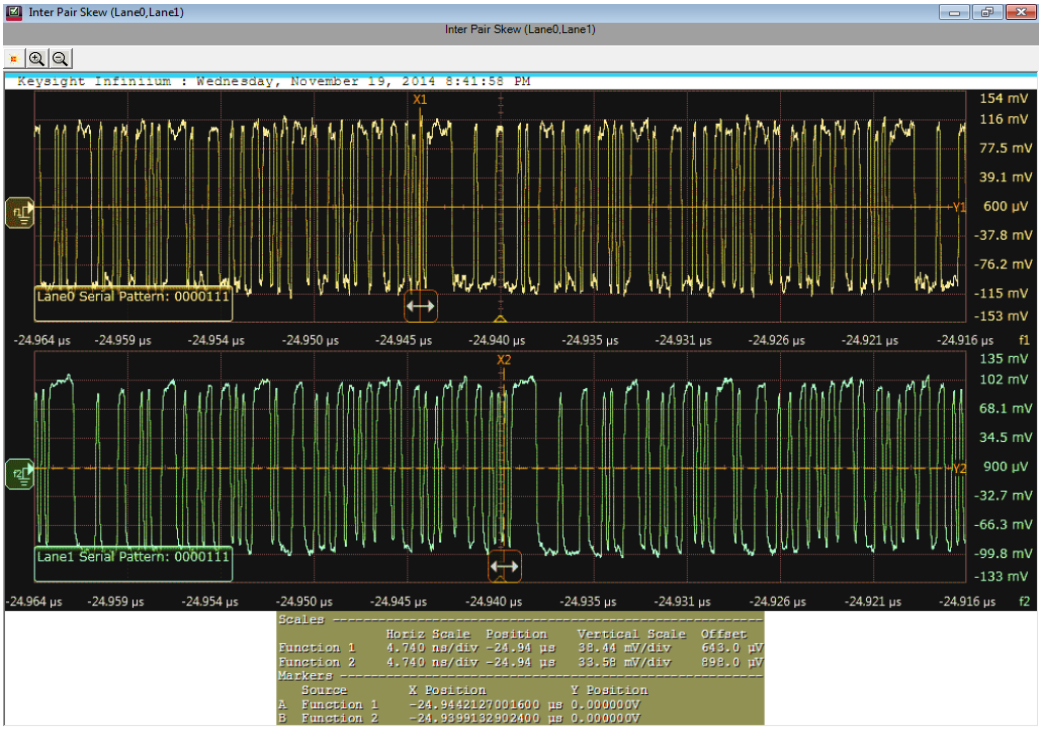

Figure 53 Reference Image for Inter Pair Skew Test

Main Link Frequency Compliance Test

Test Overview

The Main Link Frequency Compliance Test ensures that under any condition, the average transfer rate does not exceed the minimum or maximum frequency range, as defined in the eDP 1.4 Standard. Excessive frequency error from fundamental references results in receiver errors or poses difficulty in tracking.

For SSC Enabled:

The minimum acquisition time is 33.4 micro seconds (µs). The application evaluates at least ten full SSC cycles of the signal, along with evaluating the minimum, maximum and average frequency values while the spread spectrum clocking is active.

For SSC Disabled:

The minimum acquisition time is 33.4 µs, which is comparable to the acquisition time when SSC is enabled. The application evaluates at least ten acquisitions of the signal, along with evaluating the minimum, maximum and average frequency values while the spread spectrum clocking is inactive.

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3	
Bit Rate	All bit rates are supported.	
Voltage Level and Pre-emphasis Level	Any Voltage level and Pre-Emphasis level that are compliant to all normative tests run on the Source.	
SSC	If the DUT can operate in either the SSC-enabled or the SSC-disabled state, it shall be tested in both conditions.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal.

2 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.

3 Measure the data rate and validate the test pattern.

4 For SSC enabled:
   i Set up the clock recovery base on the clock recovery setting of the configuration variable.
   ii Measure the unit interval (UI) of the differential signal.
   iii Set up a measurement trend to capture a range of unit interval values of the differential signal.
   iv Apply a low pass filter to the range of unit interval values.
   v Acquire a signal with an acquisition time that covers one full SSC cycle.
   vi Measure the clock data recovery rate (CDR rate) for at least ten full SSC cycles.
   vii Measure the minimum, maximum and mean unit interval values for at least ten full SSC cycles.
   viii Compute the minimum, maximum and mean data rate values for at least ten full SSC cycles.
5 For SSC Disabled:
   i Set up the clock recovery base on the clock recovery setting of the configuration variable.
   ii Measure the unit interval (UI) of the differential signal.
   iii Set up a measurement trend to capture a range of unit interval values of the differential signal.
   iv Apply a low pass filter to the captured range of unit interval values.
   v Acquire a signal that attains the minimum acquisition time (33.4 µs).
   vi Measure the clock data recovery rate (CDR rate) for at least ten full cycles that attain the minimum acquisition time.
   vii Measure the minimum, maximum and mean unit interval values for at least ten full cycles that attain the minimum acquisition time.
   viii Compute the minimum, maximum and mean data rate values for at least ten full cycles that attain the minimum acquisition time.
6 Compute the Main Link Frequency using the following equation:

*Main Link Frequency = (CDR Rate – Nominal Data Rate) / Nominal Data Rate) * 1E6*

Viewing Test Results

The measured value of the main link frequency for the test signal must fall within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

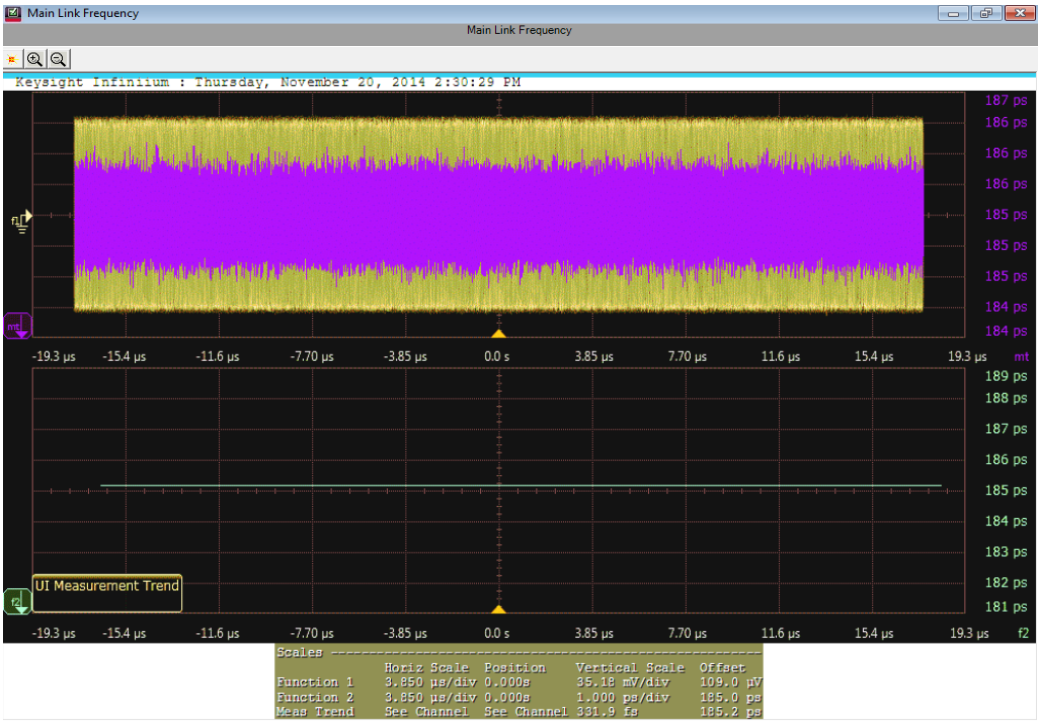

Figure 54 Reference Image for Main Link Frequency Compliance Test

SSC Modulation Frequency Test

Test Overview

The SSC Modulation Frequency Test evaluates the frequency of the SSC modulation and validates that the frequency lies within the specification limits of the eDP Standard. SSC frequency has almost little to no effect on interoperability of eDP sources.

The minimum acquisition time is 33.4 µs. When running this test, it is essential that you use a low pass filter to remove the high frequency non-SSC jitter components. This low pass filter is a 2^{nd} order Butterworth filter with a 3 dB corner frequency of 1.98MHz, which is 60 times more than the highest acceptable SSC frequency of 33kHz. You must conduct this analysis over a minimum of ten full SSC cycles.

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3	
Bit Rate	All bit rates are supported.	
Voltage Level and Pre-emphasis Level	Any Voltage level and Pre-Emphasis level that are compliant to all normative tests run on the Source.	
SSC	Only such DUTs are tested that operate in the SSC-enabled state.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal.
2 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.
3 Measure the data rate and validate the test pattern.
4 Set up the clock recovery base on the clock recovery setting of the configuration variable.
5 Measure the unit interval (UI) value of the differential signal.
6 Set up a measurement trend to capture a range of unit interval values of the differential signal.
7 Apply low pass filter to the range of unit interval values.
8 Measure the frequency of the filtered unit interval range.

Viewing Test Results

The measured value of the SSC modulation frequency for the test signal should be within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

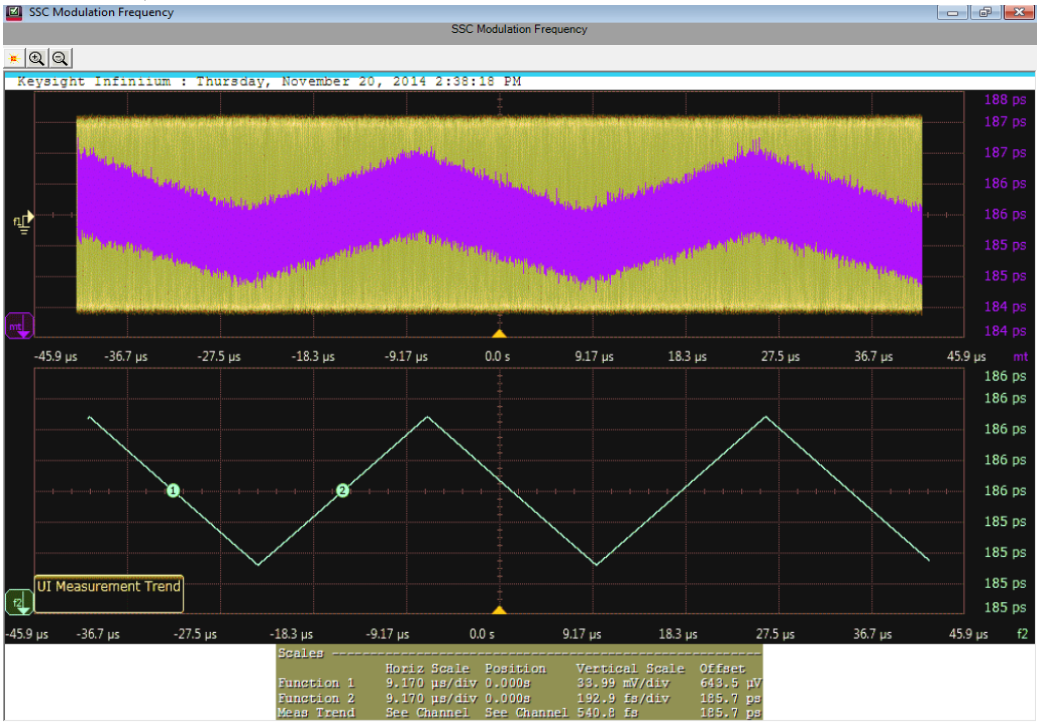

Figure 55 Reference Image for SSC Modulation Frequency Test

SSC Modulation Deviation Test

Test Overview

The SSC Modulation Deviation Test evaluates the range of SSC down-spreading of the transmitter signal in Parts Per Million (PPM). One of the requirements of spread spectrum clocking is that the sink receiver follows the instantaneous frequency of the transmitter signal. This test measures the range of frequency deviation with SSC. The more the frequency deviates from the standard limits, the higher are the risks of interoperability in eDP sources.

The minimum acquisition time is 33.4 µs. When running this test, it is essential that you use a low pass filter to remove the high frequency non-SSC jitter components. This low pass filter is a 2^{nd} order Butterworth filter with a 3 dB corner frequency of 1.98MHz, which is 60 times more than the highest acceptable SSC frequency of 33kHz. You must conduct this analysis over a minimum of ten full SSC cycles.

The application evaluates the minimum and maximum transfer rate for each cycle for at least ten full SSC Cycles. Evaluating the average transfer rate is optional. Calculate the SSC Range by deducting the average of the maximum values of data rates from the average of the minimal values of data rate. Use the following equation:

SSC Range = [Average(Data Rate Min. Values) – Average(Data Rate Max. Values)]

*SSC Modulation Deviation = [SSC Range / Nominal Data Rate] * 1E6*

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3	
Bit Rate	All bit rates are supported.	
Voltage Level and Pre-emphasis Level	Any Voltage level and Pre-Emphasis level that are compliant to all normative tests run on the Source.	
SSC	Only such DUTs are tested that operate in the SSC-enabled state.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal.
2 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.
3 Measure the data rate and validate the test pattern.
4 Set up the clock recovery base on the clock recovery setting of the configuration variable.
5 Measure the unit interval (UI) value of the differential signal.
6 Set up a measurement trend to capture a range of unit interval values of the differential signal.
7 Apply low pass filter to the range of unit interval values.
8 Measure the frequency of the filtered unit interval range.
9 Acquire a signal with an acquisition time that covers one full SSC cycle.
10 Measure the clock data recovery rate (CDR rate) for at least ten full SSC cycles.
11 Measure the minimum, maximum and mean unit interval values for at least ten full SSC cycles.
12 Compute the SSC Modulation Deviation using the following equations:

SSC Range = [Average(Data Rate Min. values) – Average(Data Rate Max. values)]

*SSC Modulation Deviation = [SSC Range / Nominal Data Rate] * 1E6*

Viewing Test Results

The measured value of the SSC modulation deviation for the test signal should be within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

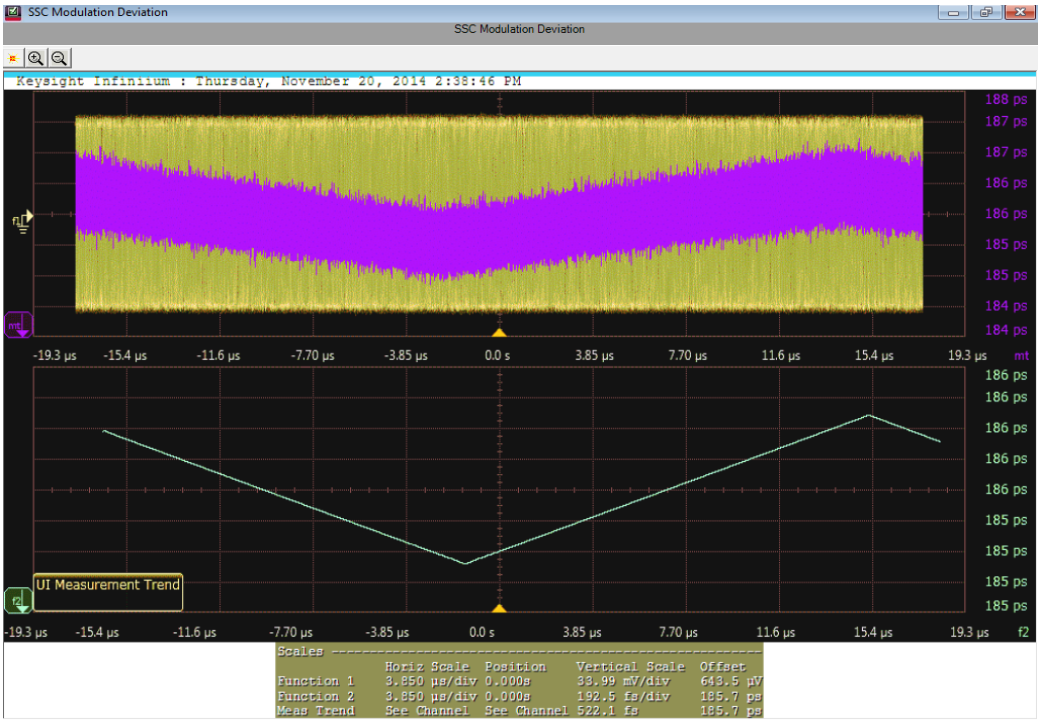

Figure 56 Reference Image for SSC Modulation Deviation Test

5 eDP Automated Source Single-Ended Tests

This section describes the single-ended tests for interoperability verification of eDP sources.

Intra Pair Skew Test

Test Overview

The Intra Pair Skew Test evaluates the skew, or time delay, between the n and p legs of the differential pairs of the eDP interface. You may use these measurements to predict the EMI/RFI performance of the channels.

Intra-Pair Skew in the channel affects the signal during transition and results in a reduction of the eye height. The Eye Diagram Test captures the impact of the intra-pair skew.

Prior to taking measurements, you must ensure that the measurement instrument is de-skewed and compensated to achieve accurate results.

The application captures waveforms of both signal polarities (n and p) simultaneously on one lane, by using two single-ended measurement channels. The rising edge of the data true signal (D+) is compared with the falling edge of the complementary signal (D-), and the rising edge of the complementary signal is compared to falling edge of the data true signal. Determine the point where the waveform crosses the transition amplitude to find the time of transition.

For each lane composed of two single-ended signals D+ and D-, calculate the High and Low Voltage levels for each single-ended signal by measuring the average value over the range of 0.6-0.75 UI, which lies past the rising edge for V_H and past the falling edge for V_L.

Establish the skew timing threshold as the median voltage between V_H and V_L.

$$V_{Threshold\_D+} = (V_{H\_D+} + V_{L\_D+}) / 2$$

$$V_{Threshold\_D-} = (V_{H\_D-} + V_{L\_D-}) / 2$$

Calculate the intra pair skew by summing all skew values (high to low and low to high skew values) and divide the total by the number of edges. Use the following equation:

$$Intra\ Pair\ Skew = \{1/NumEdges\}\Sigma\{[(T_{Trans\_D+\_Rise} - T_{Trans\_D-\_Fall}) + (T_{Trans\_D+\_Fall} - T_{Trans\_D-\_Rise})]/2\}$$

The intra pair skew is measured for each supported lane:

- Lane 0+ and Lane 0-
- Lane 1+ and Lane 1-
- Lane 2+ and Lane 2-
- Lane 3+ and Lane 3-

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3	
Bit Rate	Highest bit rate is supported.	
Voltage Level and Pre-emphasis Level	Any voltage level and pre-emphasis level are compliant to all source normative tests	
SSC	If the DUT can operate in either the SSC-enabled or the SSC-disabled state, it shall be tested in both conditions.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal.

2 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.

3 Measure the data rate and validate the test pattern.

4 Acquire the qualifying test pattern over the specific number of required patterns to measure the high voltage level for the single-ended plus signal.

5 Set up the Histogram to measure the average value of high voltage level for the single-ended plus signal.

6 Acquire the qualifying test pattern over the specific number of required patterns to measure the low voltage level for the single-ended plus signal.

7 Set up the Histogram to measure the average value of low voltage level for the single-ended plus signal.

8 Compute the threshold voltage for the single-ended plus signal using the following equation:

$$V_{Threshold\_D+} = (V_{H\_D+} + V_{L\_D+}) / 2$$

9 Acquire the qualifying test pattern over the specific number of required patterns to measure the high voltage level for the single-ended minus signal.

10 Set up the Histogram to measure the average value of high voltage level for the single-ended minus signal.

11 Acquire the qualifying test pattern over the specific number of required patterns to measure the low voltage level for the single-ended minus signal.

12 Set up the Histogram to measure the average value of low voltage level for the single-ended minus signal.

13 Compute the threshold voltage for the single-ended minus signal using the following equation:

$$V_{Threshold\_D-} = (V_{H\_D-} + V_{L\_D-}) / 2$$

14 Search the intra pair skew pattern for $D+_{Rise}$ to $D-_{Fall}$ from the single-ended plus signal using InfiniiScan Generic Serial trigger.

15 Compute the time difference between the corresponding edges at the transition point of D+ and D- over a specific number of required patterns.

16 Search the intra pair skew pattern for $D+_{Fall}$ to $D-_{Rise}$ from the single-ended plus signal using InfiniiScan Generic Serial trigger.

17 Compute the time difference between the corresponding edges at the transition point of D+ and D- over a specific number of required patterns.

18 Compute the Intra Lane Skew using the following equation:

$$Intra\ Pair\ Skew = \{1/NumEdges\}\Sigma\{[(T_{Trans\_D+\_Rise} - T_{Trans\_D-\_Fall}) + (T_{Trans\_D+\_Fall} - T_{Trans\_D-\_Rise})]/2\}$$

NOTE **DFE will be enabled by default for HBR3 bit rate.**

Viewing Test Results

The measured intra pair skew for the test signal must fall within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

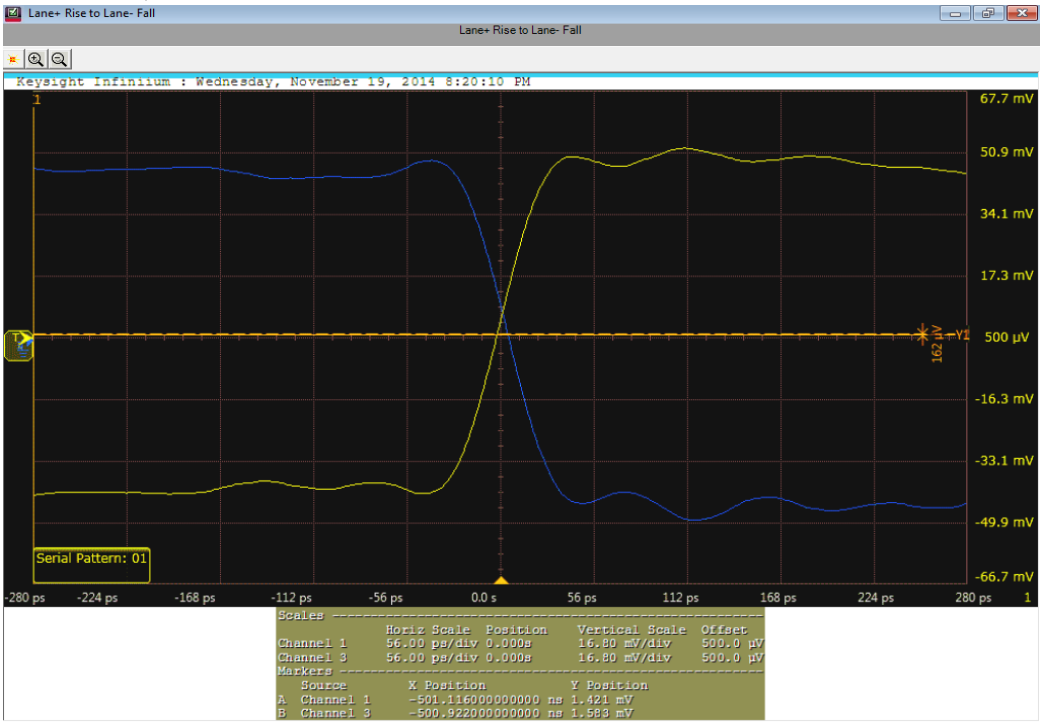

Figure 57 Reference Image for Intra Pair Skew Test

AC Common Mode Noise Test

Test Overview

The AC Common Mode Noise Test reports the common mode noise (unfiltered RMS) present in the main link differential pairs. You may use these measurements to predict the EMI/RFI performance of the channels.

The conversion of the main link signal from differential mode to common mode reduces the eye. This effect is already taken into account during the eye measurement. Any increase in the common mode noise that occurs due to crosstalk does not affect the channel margin measured at TP3_EQ.

Prior to taking measurements, you must ensure that the measurement instrument is de-skewed and compensated to achieve accurate results.

Calculate the value of the common mode noise using the following equation:

$$V_{TX\text{-}AC\text{-}CM} = (V_{TX\text{-}PLUS} + V_{TX\text{-}MINUS}) / 2$$

Calculate the value of the common mode noise RMS using the following equation:

$$V_{TX\text{-}AC\text{-}CM\_RMS} = [(X_1^2 + X_2^2 + X_3^2 + ... + X_n^2) / n]^{0.5}$$

The common mode noise is measured for each supported lane:

- Lane 0+ and Lane 0-
- Lane 1+ and Lane 1-
- Lane 2+ and Lane 2-
- Lane 3+ and Lane 3-

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3	
Bit Rate	All bit rates are supported.	
Voltage Level and Pre-emphasis Level	Any Voltage level and Pre-Emphasis level that are compliant to all normative tests run on the Source.	
SSC	If the DUT can operate in either the SSC-enabled or the SSC-disabled state, it shall be tested in both conditions.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal.

2 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.

3 Measure the data rate and validate the test pattern.

4 Set up the common mode signal from the single-ended plus and single-ended minus signals using the following equation:

$$V_{TX\text{-}AC\text{-}CM} = (V_{TX\text{-}PLUS} + V_{TX\text{-}MINUS}) / 2$$

5 Apply low pass filter to the common mode signal, if filter is enabled.

6 Measure the value of the RMS voltage for the common mode signal, excluding the DC component.

NOTE DFE will be enabled by default for HBR3 bit rate.

Viewing Test Results

The measured value of the AC common mode noise for the test signal is within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

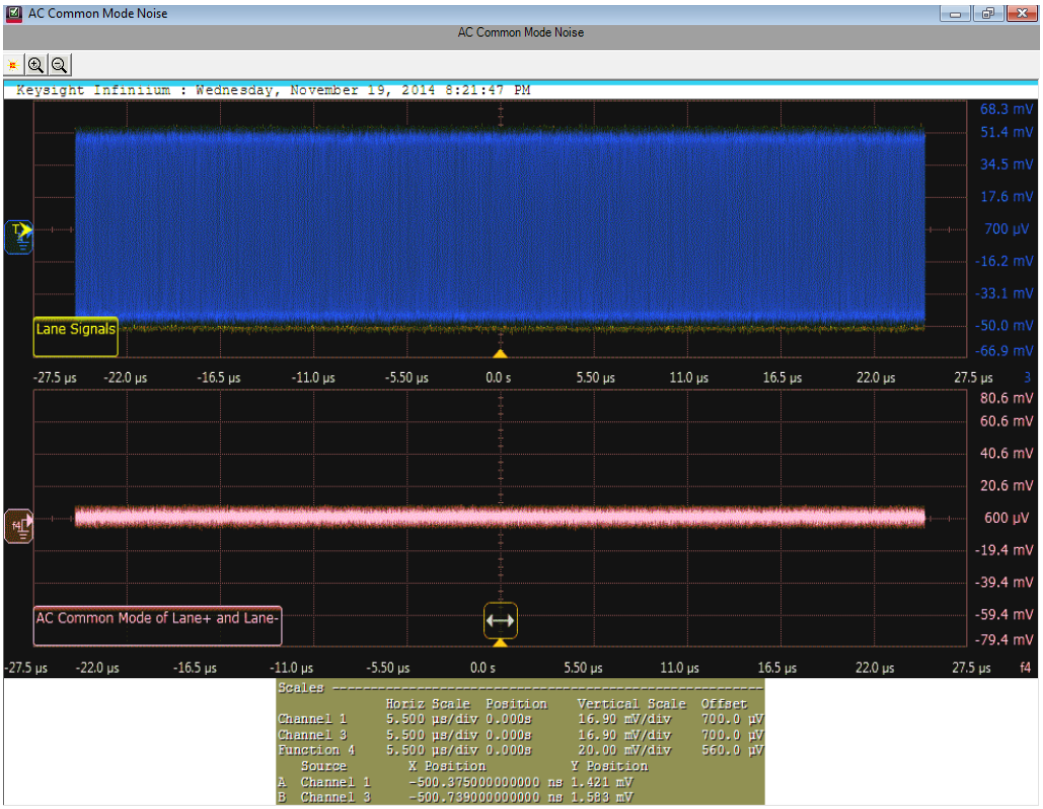

Figure 58 Reference Image for AC Common Mode Noise Test

Single-Ended Rise and Fall Time Mismatch Test

Test Overview

The Single-Ended Rise/Fall Time Mismatch Test evaluates the difference that may occur between the rise and fall times of the main link data lanes.

Test Conditions

Specification	eDP Version 1.4b	eDP Version 1.5
Test Point	TP3	
Bit Rate	Highest bit rate is supported.	
Voltage Level and Pre-emphasis Level	Voltage Level: Level 2 Pre-emphasis Level: Level 0	
SSC	If the DUT can operate in either the SSC-enabled or the SSC-disabled state, it shall be tested in both conditions.	
Test Lane	All test lanes must generate a test pattern to induce crosstalk.	
Test Pattern	Any of the supported test patterns	

Test Procedure

1 Validate and acquire the signal.

2 Determine the threshold of the signal by measuring V_{Top} and V_{Base}.

3 Measure the data rate and validate the test pattern.

4 Acquire the qualifying test pattern over the specific number of required patterns to measure the high voltage level for single-ended plus signal.

5 Set up the Histogram to measure the average value of high voltage level for single-ended plus signal.

6 Acquire the qualifying test pattern over the specific number of required patterns to measure the low voltage level for single-ended plus signal.

7 Set up the Histogram to measure the average value of low voltage level for single-ended plus signal.

8 Acquire the qualifying test pattern over the specific number of required patterns to measure the high voltage level for single-ended minus signal.

9 Set up the Histogram to measure the average value of high voltage level for single-ended minus signal.

10 Acquire the qualifying test pattern over the specific number of required patterns to measure the low voltage level for single-ended minus signal.

11 Set up the Histogram to measure the average value of low voltage level for single-ended minus signal.

12 Set up the measurement top and base voltage levels based on the High and Low voltage levels.

13 Set up the measurement threshold to 20%, 50%, 80% of top and base voltage levels.

14 Measure the rise time or fall time of the single-ended signal.

15 For single-ended plus (SEplus) rising and single-ended minus (SEminus) falling:

$T_{Mismatch\_rising}$ = 1/(Number of Edges) * ∑ {(SEplus rising time – SEminus falling time) / (SEplus rising time + SEminus falling time) / 2} *100%

16 For single-ended plus (SEplus) falling and single-ended minus (SEminus) rising:

$T_{Mismatch\_falling}$ = 1/(Number of Edges) * ∑ {(SEplus falling time – SEminus rising time) / (SEplus falling time + SEminus rising time) / 2} *100%

17 Mismatch time ($T_{Mismatch}$) is measured as:

$T_{Mismatch}$ = Max value between $T_{Mismatch\_rising}$ and $T_{Mismatch\_falling}$

NOTE DFE will be enabled by default for HBR3 bit rate.

Viewing Test Results

The measured value of the rise time and fall time mismatch for the test signal must fall within the conformance limit of the specifications for the CTG Test mentioned under the “References” column of Table 1.

For each test trial, click the **Results** tab to view the results. Click the desired test to view its result. The lower pane contains the displays the detailed description of the test results. A sample reference image based on the measured values is captured by the oscilloscope. Click the sample reference image to view the details. For information about viewing the test results, refer to **Viewing Results** in the online help.

6 eDP Automated Source AUX Channel Physical Layer Tests

This section describes common tests for verification of eDP source devices.

Connection Setup for AUX Channel Tests

Perform the following steps before you run the Auxiliary Channel tests on the source device:

1 Click **Connection Setup** in the **Set Up** tab.

2 **DUT Type** is by default selected as **Source**.

3 Select **Yes** in **Reference Device** if a reference sink (for DUT Type Source) is attached to the DUT.

4 Click **Next**.

5 Select either **Differential Probe** or **Single-Ended** in the **Connection Type** area.

6 Assign Channels for AUX lanes according to the **Connection Type**.

7 Click **Next**.

8 In the **Trigger Setup** area, define the oscilloscope parameters to trigger on an Auxiliary signal during testing:

- **Hold Off Time** – The oscilloscope minimum hold off time before triggering the next waveform. Note that any Auxiliary transaction from the source must receive a reply from the sink in 400 us, else such a transaction is considered a timeout. Hold off time, in such cases, represents the minimum idle time before each Aux transaction is initialized. It is defaulted to 300 us which is a safe timing value for most devices tested in the lab. Most devices respond much faster than 300 us.
- **Trigger Level** – The AUX Channel signal level on which to trigger. Note that for a bi-directional signal (where a reference sink is attached), you must set the trigger level such that it crosses both the source command and the sink reply signal. Figure shows correct and incorrect trigger levels.
- **Vertical Scale** – The oscilloscope vertical scale. Set the vertical to make sure that all signals are visible on the oscilloscope display.
- **Offset** – Set the offset so that the center point is aligned with the center of the oscilloscope display.
- **Upper Threshold/Lower Threshold** – The threshold level of signal must be set properly so that both upper and lower thresholds cross both the source and sink signals when the DUT is attached with a reference sink. The threshold levels are important parameters because they are used for edge detection when decoding a source command from a sink reply.
- Click the **Learn** button to access the information guide about the trigger setup parameters. However, note that the learning guide may not necessarily work due to variation in the actual Auxiliary signals, owing to different manufacturers. Keysight recommends that you must check to make sure that the parameters are correctly set as previously described.
- Click **Verify** and follow the instructions, if you wish to check the AUX Channel trigger.
- You may **Save** or **Load** the trigger setup configuration as a **.tsf* file.

9 Click **OK**.

10 In **Acquisition Mode**, select the **Offline** check box if waveform acquisition and analysis are not available on a live Infiniium Oscilloscope and saved waveforms are being used instead.

11 For **Offline** acquisition, select the test category that requires waveforms.

12 Define the number of waveform acquisitions.

13 Click the **Start Acquisition** button to start capturing and saving waveforms.

14 Click **Finish** to return to the **Set Up** tab.

AUX Channel Unit Interval Test

Test Overview

The objective of the test is to evaluate the AUX Channel waveform, ensuring that the overall variation of the Manchester transaction Unit Interval stays within the specification limits.

Test Conditions

Parameter	Condition
Test Point	Source–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink

Test Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Trigger Setup.
2 Generate FUNC1 signal, which is the differential signal of the AUX Channel.
3 Generate FUNC3 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery.
5 Set up the parameter of the measurement trend:
   a Set up the Unit Interval measurement for the differential AUX Channel signal.
   b Set up the frequency measurement for the Clock signal.
   c Set up the measurement trend.
6 Set up the waveform Histogram on the measurement trend:
   a Initialize AUX Channel transactions and acquire the differential AUX Channel signal.
   b Identify the first and the last points for the desired transaction.
   c Zoom-in on the desired transaction.
   d Set up the Vertical Waveform Histogram on the measurement trend within the desired transaction.
   e Obtain the measurement for the mean, maximum and minimum values of the waveform Histogram.
7 Repeat step 6 ten times.
8 Report the measurement results.

PASS Condition

Manchester Transaction Unit Interval (UIMAN):

- Minimum = 0.4 µsec
- Maximum = 0.6 µsec

AUX Channel Eye Test

Test Overview

The objective of this test is to evaluate the transmitter AUX Channel waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions

Parameter	Condition
Test Point	Source–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink

Test Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Trigger Setup.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC3 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

6 Set up the waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

7 Set up the parameters for the Mask Test.

   a Load the eye mask based on the settings in the Configuration Variable.

   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

   c Initialize the AUX Channel transaction and run the eye mask until 10 waveforms are folded.

8 Check for any signal trajectories entering into the mask.

9 Report the measurement results.

PASS Condition

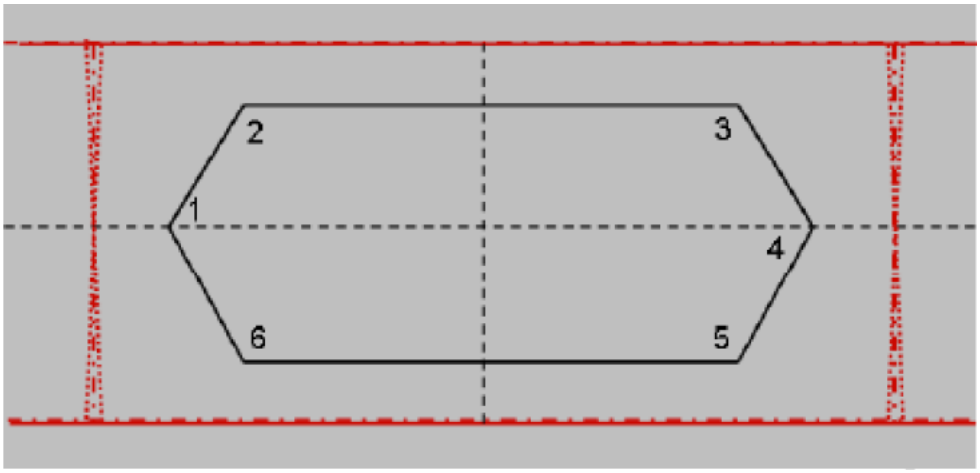

Figure 59 AUX Channel EYE MASK for Manchester Transactions

Table 6 TP3 Eye Mask Vertices for Source DUT for eDP 1.3

Point	Time (from Eye center)	Minimum Voltage Value at Six Veritces (mV)
1	-185ns	0
2	-135ns	135
3	135ns	135
4	185ns	0
5	135ns	-135
6	-135ns	-135

AUX Channel Peak to Peak Voltage Test

Test Overview

The objective of the test is to evaluate the transmitter AUX Channel Waveform, ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Parameter	Condition
Test Point	Source–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink

Test Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Trigger Setup.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC3 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

6 Set up the horizontal waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

7 If you have selected the “AUX Channel Eye Test” under the Select Tests tab of the compliance application:

   a Set up the parameter of the Mask Test:

      i Load the eye mask based on the settings in the Configuration Variable.

      ii Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

      iii Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.

   b Check for any signal trajectories entering into the mask.

8 Set up the waveform histogram on the AUX Channel eye diagram.

   a Set up the vertical waveform histogram on the AUX Channel eye diagram to measure the peak to peak voltage.

9 Report the measurement results.

PASS Condition

Table 7 Embedded DisplayPort (eDP 1.3) AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage for Source	0.27V	1.36V

Table 8 Embedded DisplayPort (eDP 1.4 and 1.4b) AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage for Source	0.14V	1.36V

AUX Channel Eye Sensitivity Calibration

Test Overview

The objective of this test is to calibrate the peak-to-peak voltage of the transmitter AUX Channel waveform by reference device (reference source or reference sink), ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Parameter	Condition
Test Point	Source–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink

Test Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.
2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Trigger Setup.
3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.
4 Generate FUNC3 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery.
6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the waveform Histogram on the AUX Channel eye diagram:
   a Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.
   b Set up the vertical waveform Histogram of width 0.6 UI at the center of the AUX Channel eye diagram.
   c Measure the V_{TOP} and VBASE using the waveform Histogram mean value.
8 Repeat Step 8 three times.
9 Report the measurement results.

PASS Condition

Table 9 DisplayPort AUX Channel Peak-to-Peak Voltage for Channel Eye Sensitivity Calibration

Parameter	Min	Max
AUX Peak-to-Peak voltage for Channel Eye Sensitivity Calibration	0.24V	0.28V

AUX Channel Eye Sensitivity Test

Test Overview

The objective of the test is to evaluate the sensitivity to the AUX Channel Eye Opening of the DUT as per the specification limits.

Test Conditions

Parameter	Condition
Test Point	Source–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink

Test Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.
2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Trigger Setup.
3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery.
5 Initialize the AUX Channel transaction and acquire the differential AUX Channel signal
6 Check if the reference device could detect the transaction or not.
7 Decode the AUX Channel signal and check whether the transaction passed or failed.
8 Report the measurement results.

PASS Condition

Determine whether the AUX Channel communication is successful. For example, the Transmitter DUT sends an AUX Request to the Reference Receiver. The Reference Receiver acknowledges and the Transmitter DUT responds to the to indicate that the acknowledgment was successfully received.

PASS = No errors observed in the response

FAIL = One or more errors observed

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