Deep Storage with Xilinx ChipScope Pro and Agilent Technologies FPGA Trace Port Analyzer

Product Overview

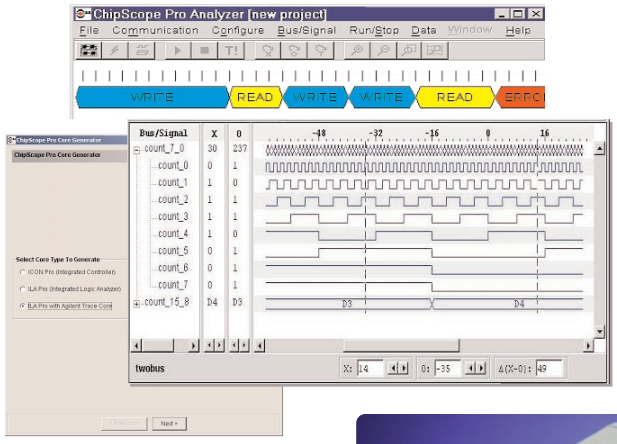

Figure 1. Combine the Agilent E5904B option 500 FPGA trace port analyzer with Xilinx ChipScope Pro tools to create a more powerful in-circuit debug environment.

Debug Systems with FPGAs More Effectively

Quickly and accurately debug systems that include large, fast field programmable gate arrays (FPGAs) with a powerful Agilent Technologies FPGA trace port analyzer. Agilent and Xilinx have teamed to deliver a high-value solution that couples the advantages of Xilinx's ChipScope on-chip logic and bus analysis with Agilent's fast and deep external trace storage—at a price that fits your budget.

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Agilent Technologies

Features and Benefits

Solve Debug Challenges

Debugging systems that include leading-edge FPGAs can be challenging. To capture traces, internal nodes must be routed out to FPGA pins. Critical internal FPGA nodes may not be readily accessible to pins where a traditional logic analyzer can probe. Pins available for debug may be limited in number. Deep traces may be required to capture a sufficient event history.

Agilent and Xilinx now offer a better solution. Supporting a wide range of Xilinx FPGAs, the solution combines the powerful capabilities of the:

- Agilent FPGA trace port analyzer
- Agilent trace core
- Xilinx ChipScope Pro tools

Key Benefits

The Agilent FPGA trace port analyzer solution expands the capabilities available in ChipScope Pro tools, delivering unique benefits that help you effectively find in-circuit functional bugs at a price within your budget. This solution allows you to:

- Efficiently debug using a fraction of the normally required debug pins
- Collect deep memory traces (up to 2 M states on each acquisition channel)
- Trigger on events internal to the FPGA
- Acquire synchronous trace capture up to 200 MHz
- Perform high-speed JTAG cable communication

Deep Trace Capture

To use the deep trace capture available in the Agilent trace port analyzer, insert debug cores in the FPGA using the ChipScope Pro tools. These cores include the:

- Xilinx Integrated CONtrol (ICON)
- Xilinx Integrated Logic Analyzer (ILA)
- Agilent trace core (ATC)

These debug cores enable communication with the ChipScope Pro user interface to configure a measurement and view the resulting trace capture on the ChipScope Pro viewer.

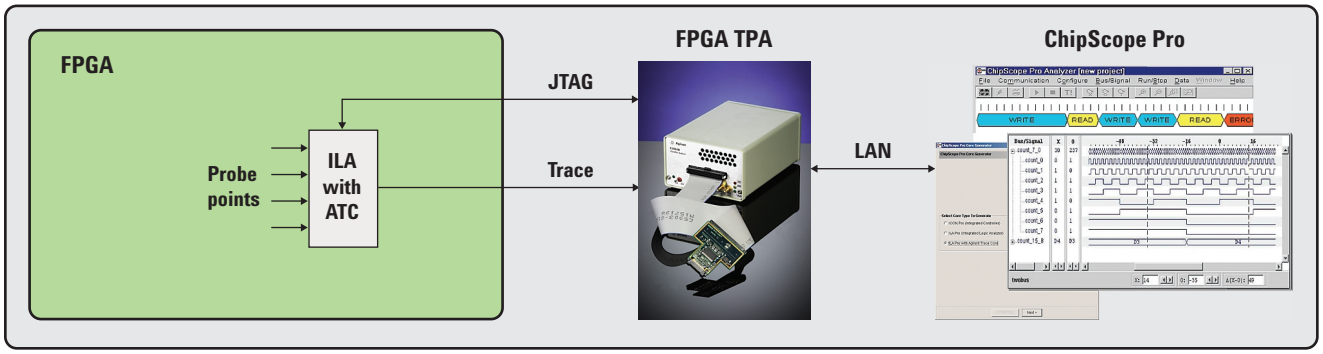


Figure 2. The LAN-based Agilent trace port analyzer (TPA) communicates to the target FPGA via JTAG. The Agilent trace core (ATC) reduces the number of pins required to collect trace information. The Agilent trace port analyzer exports captured trace to ChipScope Pro via LAN for viewing.

Features and Benefits (continued)

Agilent Trace Core (ATC)

Each license of ChipScope Pro includes Agilent trace cores that can be inserted into the FPGA design. A variety of cores are available to match the number of FPGA pins available to collect trace data using the external memory of the trace port analyzer.

The cores can use time-division multiplexing for debug pin-count reduction. Slower internal FPGA circuit speeds yield higher pin compression levels. Pick the core best suited for your measurement and insert the core into your design using the ChipScope Pro Core Inserter or Core Generator. The pin compression ratio takes into account:

- Speed of the circuit being measured
- Maximum speed of the associated I/O driver
- Number of internal nodes probed
- Real-time trace depth

After the core is inserted into your design, configure the trigger condition in the ChipScope Pro Analyzer software. The input clock into the Agilent trace core must be free running (not gated). Agilent's FPGA trace port analyzer will capture real-time trace data and stop when the trace buffer is full. This trace capture is exported via LAN to the ChipScope Pro Analyzer for analysis.

Maximum Internal FPGA Clock Domain Frequency and Trace Depth	Available Number of Internal Probe Points				
Up to 50 MHz with 500 K states	11	27	43	59	75
Up to 100 MHz with 1 M states	5	13	21	29	37
Up to 200 MHz with 2 M states	3	7	11	15	19
Required number of FPGA pins	4	8	12	16	20

Table 1. Configurable Agilent trace core adapts to your debug needs.

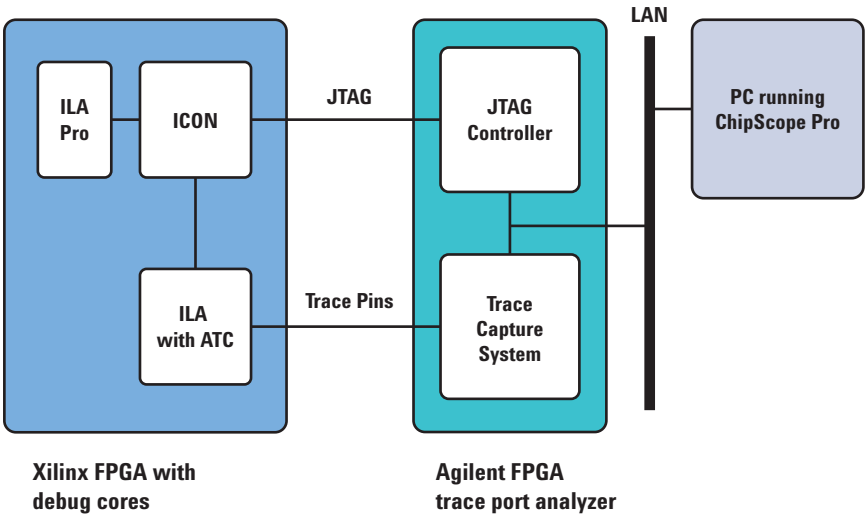


Figure 3. Block diagram of connection between key components of the combined Agilent and Xilinx solution. On a single FPGA, the JTAG controller can communicate with multiple ILA Pro cores and one ILA with ATC core.

Comparisons to Alternative Solutions

Connection to Target System
To maintain signal fidelity required for high-speed measurements, Agilent provides pinout information so you can design a low-profile mictor connector on your target system early in the development process. This also minimizes board space required for debug.

Alternative Comparisons
Agilent's LAN-based FPGA trace port analyzer combines a powerful high-speed real-time trace with a high-performance cable in an instrument that fits in the palm of your hand. Compared to using Xilinx's ChipScope Pro and FPGA block RAM for trace storage, the Agilent Xilinx enhanced solution gives you the power to:

- Preserve internal FPGA block RAM for your design by using external trace memory
- Take deeper traces—up to 2 M states
- Obtain LAN-based high performance cable capabilities for FPGA configuration download and communication between ChipScope Pro and on-chip debug cores

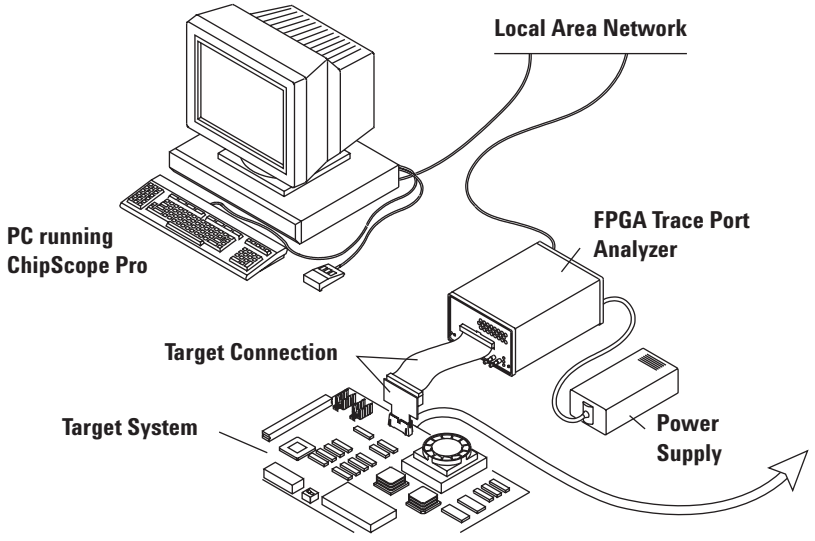
Compared to a traditional logic analysis-based trace system, the FPGA trace port analyzer solution:

- Requires fewer pins dedicated for debug
- Costs much less
- Requires significantly less bench top space
- Provides a high-performance channel for communication with the FPGA JTAG port

Agilent Logic Analysis
Agilent's FPGA trace port analyzer provides insight into in-circuit functional debug issues.

As a complement for in-circuit debug, Agilent's 16700 Series and 1680/1690 Series of logic analyzers offer an even richer set of capabilities to solve more complex problems. These LAN-based logic analyzers can be accessed remotely. They provide high-performance state and timing measurements and feature a wide set of additional features such as protocol triggering and decode, serial analysis, and email notification when the trigger condition is met.

Connect the logic analyzer to the same mictor connector used by the FPGA trace port analyzer. Import trace files captured using Xilinx ILA into the 16700 Series logic analyzers. An application note (see "Related Literature") describes how to time correlate these measurements with other 16700 Series logic analysis measurements.



No Connect[1]	1	2	No Connect[1]
No Connect[1]	3	4	No Connect[1]
No Connect[1]	5	6	ATCLK
No Connect[1]	7	8	No Connect[1]
No Connect[1]	9	10	No Connect[1]
TDO	11	12	Vref
No Connect[1]	13	14	No Connect[1]
TCK	15	16	ATD19
TMS	17	18	ATD18
TDI	19	20	ATD17
No Connect[1]	21	22	ATD16
ATD15	23	24	ATD7
ATD14	25	26	ATD6
ATD13	27	28	ATD5
ATD12	29	30	ATD4
ATD11	31	32	ATD3
ATD10	33	34	ATD2
ATD9	35	36	ATD1
ATD8	37	38	ATD0

[1] These pins *must* be true no-connects. They are reserved.

Figure 4. Designing in a mictor connector for both JTAG control and trace capture ensures signal fidelity and simplifies connection to the target system. Recommended pinout is shown above. The pinout also supports trace collection from the Virtex II Pro PowerPC (PPC) core when an Agilent E5904B #060 PPC 405 trace port analyzer or an IBM PPC RISCTrace is used.

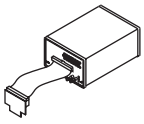
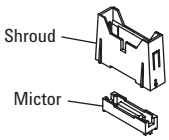
Technical Specifications and Ordering Information

Technical Specifications

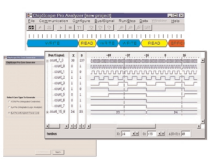
Supported Xilinx FPGA Families	Virtex-II, and Virtex-II Pro 2X Agilent trace core (for pin reduction) requires 1 DCM and 1 GBUF 4X Agilent trace core requires 1 DCM and 2 GBUFs Spartan-II, Spartan-IIE, Virtex, and Virtex-E Agilent trace core (for pin reduction) design requirements: Input clock must be routed through DDL-designated pad For 2X Agilent trace core, clock frequency limited to max FCKINLF For 4X Agilent trace core, clock frequency limited to FCKINLF/2, and output of a DLL must be input to adjacent DLL.
Chip Scope Pro Support	Version 5.1i or higher.
Cable Capabilities	Communication with host PC/workstation via LAN. Maximum JTAG TCK rate of 30 MHz. Download speed up to 10 Mbits/sec. Fast FPGA configuration download. Fast upload of ILA Pro trace data into ChipScope Pro via JTAG when FPGA block RAM is used to store trace measurement. No requirement of power from target. Support for multiple Xilinx and non-Xilinx devices on the JTAG scan chain. Long scan chains should be buffered.
FPGA Trace Port Analyzer Characteristics	Up to 2 M trace states. Memory is reduced by 50% with time tags enabled. Up to 200 MHz synchronous acquisition speed. Support from 1.8 V to 3.3 V logic levels. Time tags with 9 ns resolution. Support for one timebase per FPGA trace port analyzer.

The User's Guide, available via the internet, contains additional information on target requirements, design considerations, and other topics related to this solution.

Ordering Information

Agilent Model/Part #		Description
	E5904B #500	FPGA Trace Port Analyzer: Provides trace capabilities, high-performance cable, cable with mictor connector, and interface compatibility with ChipScope Pro.
	1252-7431	One 38-pin Mictor connector.
	E5346-44701	One Mictor connector support shroud* for PC board thickness up to 1.57 mm (0.062").
	E5346-44704	One Mictor connector support shroud* for PC board thickness up to 3.175 mm (0.125").
	E5346-44703	One Mictor connector support shroud* for PC board thickness up to 4.318 mm (0.700").

* Mictor connector shroud to provide additional strain relief between the probe and the connector.

Xilinx ChipScope Pro Tools	Description
Order directly from Xilinx or Xilinx distributors. www.xilinx.com/chipscope 	ChipScope Pro Core generator. ChipScope Pro Core inserter. ILA Pro (Integrated Logic Analyzer). IBA Pro (Integrated Bus Analyzer). ChipScope Pro Analyzer (interface for setting trigger and viewing captured trace data). Agilent trace core (time division multiplexing core to decrease the number of FPGA output pins required for debug).

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Related Literature

Publication Title	Publication Type	Publication Number
Agilent 1680 and 1690 Series Logic Analyzers	Brochure	5988-2675ENUS
16700 Series Logic Analysis System	Product Overview	5968-9661E
Probing Solutions for Logic Analysis Systems	Application Note	5968-4632E
Using the Agilent 16700 Series Logic Analysis System with the Xilinx ChipScope ILA	Application Note	5988-0643EN
Agilent Technologies E5904B Option 060 Trace Port Analyzer for IBM PowerPC Series Microprocessors	Brochure	5988-5254EN

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(fax) 0800 286 331

Other Asia Pacific Countries:
(tel) (65) 6375 8100
(fax) (65) 6836 0252
Email: tm_asia@agilent.com

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