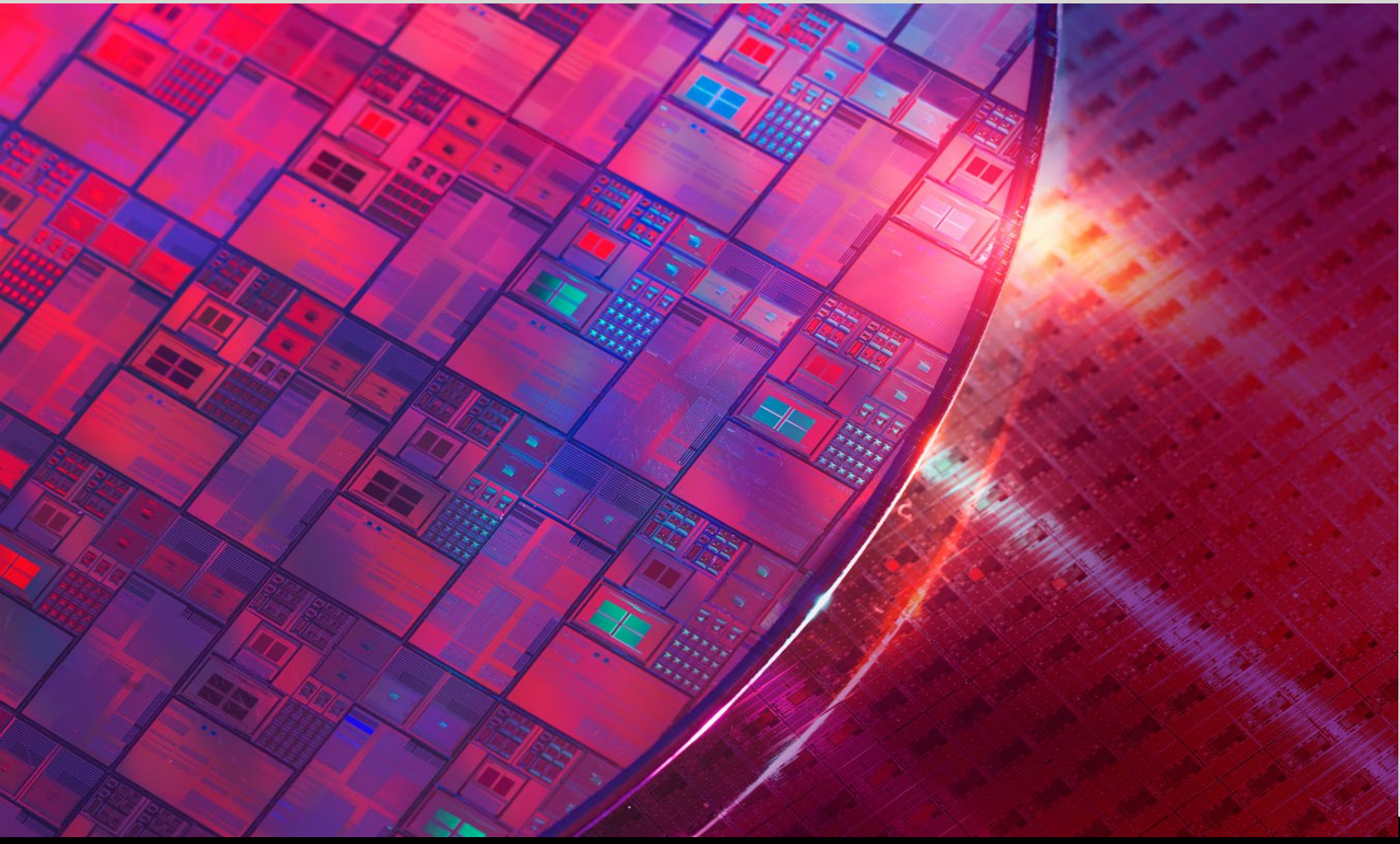
PRODUCT BROCHURE



Keysight EDA Solutions for Semiconductor Foundries

Accelerate Silicon and III-V Innovations Beyond Moore's Law

KEYSIGHT

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Introduction

In the rapidly evolving realm of Integrated Circuits (ICs), the convergence of innovation and reliability stands as a critical imperative for semiconductor foundries worldwide.

As the semiconductor industry approaches a potential trillion-dollar valuation by 2030[1], driven by advanced process technologies, 5G / 6G innovations, and Artificial Intelligence (AI), foundries play a pivotal role in accelerating these IC innovations from inception to realization.

For foundry leaders, the primary focus has been shortening time-to-market and maximizing product performance and yield— rapidly and boldly — to position their organizations at the vanguard of these unprecedented growth opportunities. Yet they are also facing a set of existential challenges, from keeping up with the process technologies and lowering production costs to grappling with the talent implications.

Addressing these challenges requires comprehensive solutions that integrate advanced device modeling, circuit design and simulation technologies, and process and data management. Keysight Technologies shines as a trailblazer, offering a total solution that supports the entire engineering lifecycle—from device characterization and modeling to Process Development Kit (PDK) creation and verification.

Purpose of This Brochure

In this brochure, we explore the critical factors foundries must consider at each stage of the device modeling and PDK development flow. By showcasing Keysight EDA's comprehensive solutions, we demonstrate how it becomes a key enabler in driving the evolution of ICs beyond Moore’s Law.

- The opening section addresses the primary challenges for silicon and III-V foundries, spanning from device modeling to PDK creation and effective data management.
- Chapters 2 to 5 describe the various Keysight EDA offerings, from IC-CAP to the newly integrated Keysight Design Data and IP Management (formerly known as Cliosoft). They illustrate how Keysight tools intertwine to improve PDK quality while reducing time-to-market and production costs.
- Beyond software, we offer customized services that augment the foundries' in-house capabilities, improving operational efficiency and accelerating innovation.

[1] https://www.mckinsey.com/industries/semiconductors/our-insights/the-semiconductor-decade-a-trillion-dollar-industry

Overview: Modeling and PDK Creation Flow

The semiconductor device modeling and PDK generation cycle is a complex process that requires precision and expertise to meet the required specifications. During the cycle, iterations, optimizations, and validations ensure that the final PDK meets the desired performance and standards.

The flow begins with designing a test structure based on specifications and requirements for the IC. Then, modeling teams must gather measured data from various devices across wafers and temperatures for accurate characterization and modeling. Once data is collected, engineers analyze it to understand device behaviors under various conditions. Using specialized software, they extract key parameters and optimize the model to ensure its robustness. The model is rigorously tested and verified against expected outcomes. The final step is the creation and verification of the PDK, which includes running circuit and layout simulations and managing PDK releases and associated data.

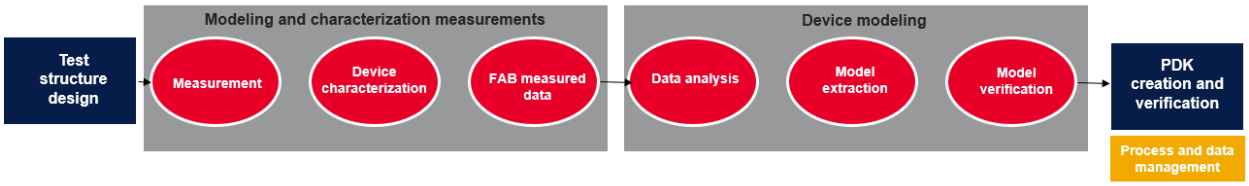


Figure 1. A simplified modeling and PDK flow for foundries

Key Challenges

- Accurate and precise measurements become more difficult due to device miniaturization, high frequencies, temperature dependency, and dynamic performance characteristics.
- Model extraction becomes more time-consuming and data-intensive, with III-V technologies introducing intricate thermal and Electronic Magnetic (EM) effects.
- Despite the pressure to bring products to market, extracting and verifying the quality of a model library can take months. Shorter product cycles mean that PDK creation must be done quickly, which can lead to mistakes and oversights.
- Home-grown modeling solutions lead to siloed workflows and manual data processes. Modeling engineers spend excessive time writing programs to adapt the tools to their needs instead of improving the model extraction and quality.

To address these challenges, Keysight can help accelerate the success of foundries and our mutual customers at every stage by providing not only powerful software but also hardware and customized services.

Keysight EDA: A Total Solution to Innovate Faster and Smarter

Keysight provides comprehensive solutions for device characterization, device modeling, PDK creation and verification, and process and data management.

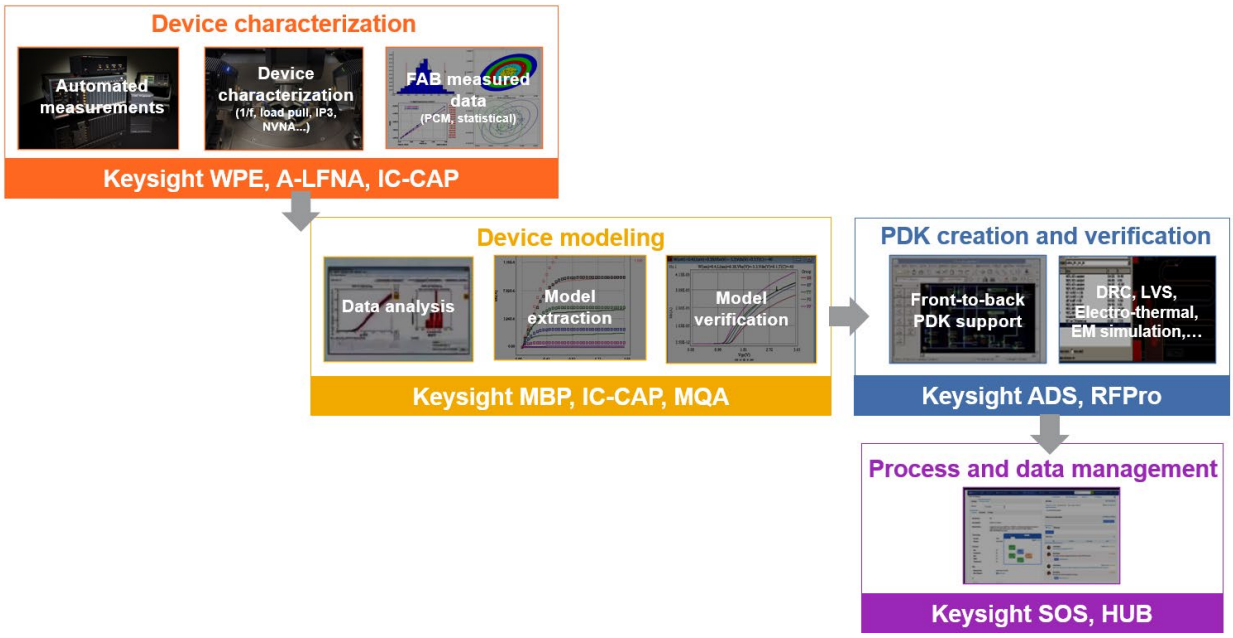


Figure 2a. PDK creation flow for silicon technologies and key Keysight EDA offerings

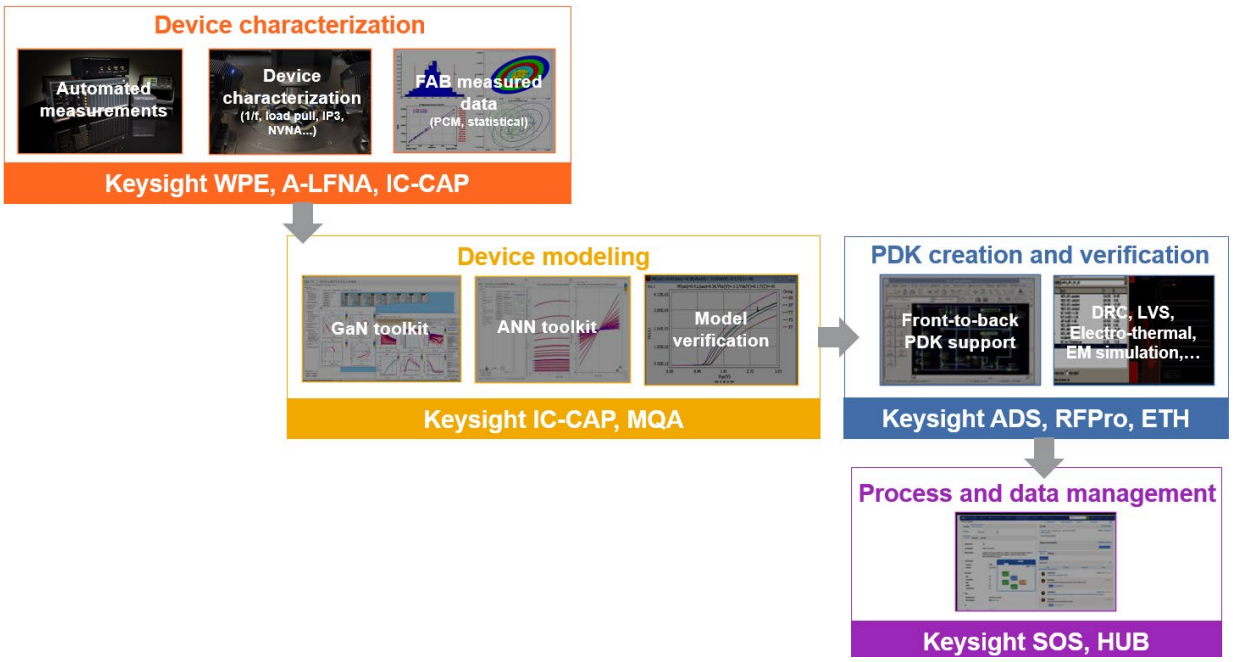


Figure 2b. PDK creation flow for III-V technologies and key Keysight EDA offerings

Step 1: Device Characterization

Gathering measured data from various devices across wafers and temperatures is paramount. However, measurements become more difficult due to the smaller device size, high frequencies, temperature dependency, and dynamic performance characteristics.

Wafer-level measurements

Consistent measurement across the wafer must be ensured to minimize errors. Correctly setting up and operating multiple instruments is time-consuming. Keysight WaferPro Express (WPE) automates wafer-level measurement across temperatures with built-in instrument support and ready-to-use, turnkey measurement routines.

Low-Frequency noise measurements

1/f noise measurement takes a long time. Visualizing device corners at high frequency, detecting extremely low noise, and capturing noise at high currents is challenging. Conducting accurate RTN Ton/Toff analysis is necessary. Keysight Advanced Low-Frequency Noise Analysis (A-LFNA) offers a comprehensive suite of tools for LFN noise analysis. It supports detailed 1/f noise measurement with multi-decade optimal RBW and includes capabilities for extremely low device noise measurement and high-power noise measurement at a few amperes of current. A-LFNA also enables Ton/Toff analysis for RTN.

Step 2: Device Modeling

Once the valid measurements have been obtained, the process moves to the device modeling stage. Model extraction complexity varies with the technology and specific device model. Device modeling software is instrumental at this stage, offering advanced graphics, links to circuit simulators, optimizers, and manual tuners to extract parameters.

Silicon device modeling

Fitting data from multiple geometries and the secondary effects, including statistical variation, layout proximity effects, and aging, takes considerable time. Engineers may have to spend excessive time writing codes to develop their own extraction flows.

Keysight MBP and IC-CAP provide easy-to-use, turnkey model generation packages for industry-standard and proprietary models. Modeling engineers can perform auto-parsing and in-situ modification of model libraries. Besides, MBP offers a turnkey global statistical and mismatch modeling package and a built-in SPICE simulator for the fastest response. IC-CAP offers RF support and turnkey packages.

III-V device modeling

It is important to model key features, such as thermal and trapping effects. Correctly setting up pulsed IV measurements and importing pulsed IV data are crucial issues.

IC-CAP provides comprehensive packages enabling key feature extraction, like thermal and trapping. Its ANN Modeling Toolkit produces accurate device models from measurement data. It also offers a Python module to import pulsed IV and SP data into the platform automatically. Besides, leveraging extracted model cards in ADS to accelerate the modeling cycle is easy.

Model validation

Each model requires numerous simulations for quality assurance, which results in an overwhelming volume of data. Yet engineers may still be uncertain about the final SPICE library's error-free status. Identifying defects in your model library intelligently. Creating model reports involves repetitive tasks. Benchmarking different model versions, simulators, and technologies.

Keysight MQA simplifies model validation by automating the creation of netlists and compiling relevant data. With intelligent, rule-based algorithms, it automates error flagging, cross-model and model-to-data comparison, customizable report generation, comprehensive library QA, cross-simulator model comparison, SPICE model-based simulator regression, and foundry model acceptance test.

Step 3: PDK Creation and Verification

The third step is PDK creation and verification, which presents several challenges due to RF circuits' high-frequency nature and stringent performance requirements. Key challenges include accurately modeling RF-specific device behaviors such as parasitics, substrate effects, and distributed elements.

Silicon foundry PDK development

Silicon foundry PDKs contain device and model libraries for the design and simulation of RFICs in Keysight Advanced Design System (ADS) and GoldenGate, process data, and other foundry-specific attributes for EM simulation with RFPro.

Using these PDKs within the ADS design environment accesses its proven circuit, EM, thermal, RF system, statistical simulation, and unique module-level multi-technology physical design and verification capabilities to ensure first-pass successful silicon.

III-V foundry PDK development

III-V Foundry PDKs for GaAs, InP and GaN processes are jointly developed by the foundry and Keysight for use with ADS and validated with the foundry. They contain device libraries for simulation and layout, verification rules for Design Rule Check (DRC) and Layout vs. Schematic (LVS), process technology data for EM and Electro-Thermal simulations, and other foundry-specific attributes for the design of III-V MMICs.

Using these PDKs within the ADS design environment accesses its proven circuit, EM, thermal, RF system, statistical simulation, and unique module-level multi-technology physical design/verification capabilities to ensure successful first-pass MMICs.

Step 4: Process and Data Management

Data challenges related to advanced-node PDKs are becoming increasingly significant as the size and complexity of model files for each PDK configuration increase exponentially. Traditional data management systems based on spreadsheets are insufficient and error prone.

Customer reference designs are created in collaboration between customers and foundries during PDK development. Bugs in the EDA toolchain are tracked and fixed through intermediate PDK releases with simulation reports. An automated mechanism is necessary for reliable releases across all customers.

Keysight Design Data Management (SOS) streamlines hardware design project management from beginning to end. It supports composite design objects, facilitates collaboration across multiple sites, and tracks the relationship between design issues and changes.

Keysight IP Management (HUB) can centralize IP management, reuse, and traceability. It enables IP sharing and tracking, facilitates bug investigation, and generates usage reports for compliance.

Figure 3. Keysight offers foundries a total solution for modeling and PDK development

Product Features and Benefits

WaferPro Express (WPE)

WaferPro Express provides a unified measurement platform for faster setup and execution of wafer-level DC / CV / RF measurements. It provides turnkey drivers and test routines for various instruments and wafer probers. Within a consistent GUI, WPE supports wafer-mapping measurement and real-time data sanity checks.

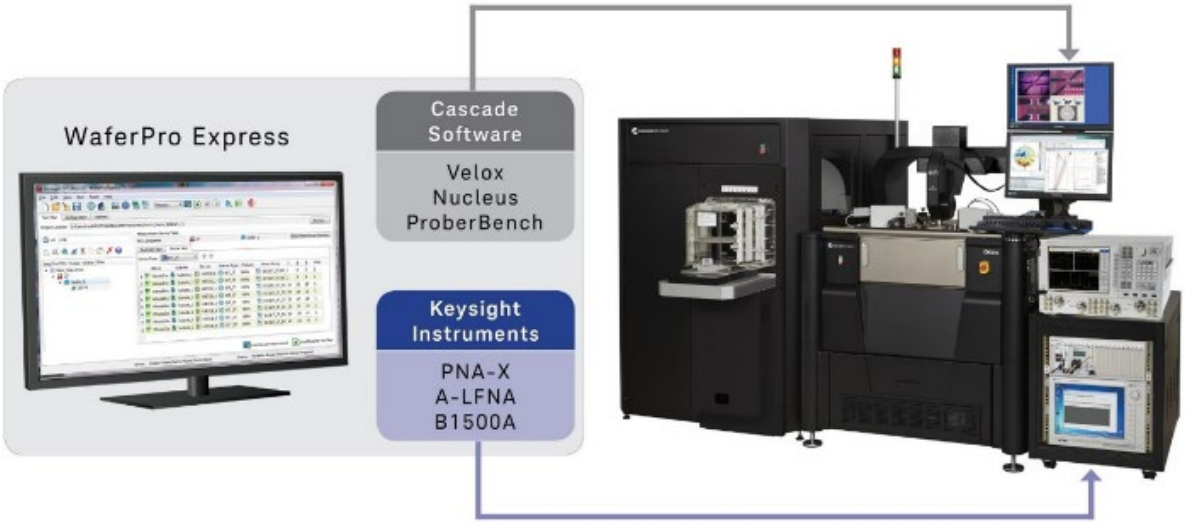


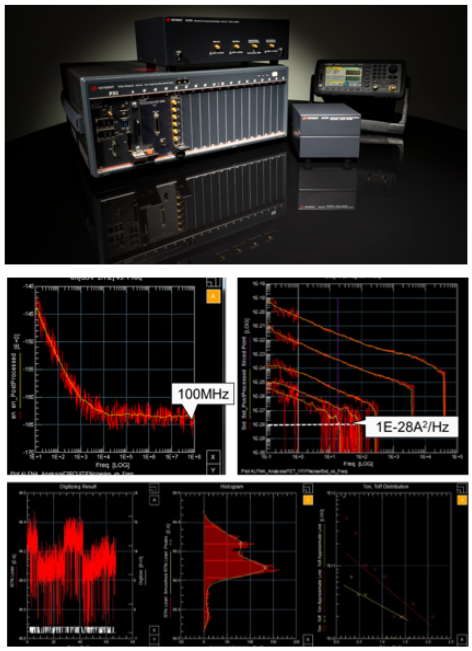
Figure 4. Automated wafer measurement solution

Benefits	Features
Reduce time-to-first measurement	• Turnkey drivers for common instruments, interfaces, and OS • Turnkey test algorithms for CMOS, BJT, and other major technologies • MBP-ready measurement routines for CMOS and BJT devices • Support promoted PXIe SMU add-on for A-LFNA
Simplify automated test setup	• Modern and intuitive UI to define wafer maps and test plans • Exclusive integration of FormFactor Velox and WinCal software • Automated RF calibration in conjunction with FormFactor WinCal
Increase measurement productivity	• Advanced data display and Wafer Data Mapping viewer • Control wafer temperature and prober chuck positioning automatically • HDF5 database for handling high-volume data • 50+ turnkey instrument drivers
Tackle advanced measurement issues	• Python 3 and PEL programming for powerful customization capabilities • Measurement driver implementation • Configurable matrix drivers

Advanced Low-Frequency Noise Analysis (A-LFNA)

Foundries need to provide PDK's with simulation models of the primitive devices, including noise effects on transistors (BJT, CMOS, etc.) and resistors. The noise models must be measured across all possible bias currents, temperatures, and device geometries.

Keysight A-LFNA enables fast, accurate, and repeatable Low-Frequency Noise (LFN) measurements on numerous device types. Through seamless integration with WPE, it enables turnkey noise measurement and the measurement of DC characteristics, capacitance, and RF S-parameters while automating wafer prober control and test suite.



Specifications	A-LFNA (E4727B)
Measurable devices	FET, BJT, Diode Resistor, Circuit
Maximum analog bandwidth	0.03Hz – 100MHz
Vamp noise floor	-185dBV^2/Hz =0.56nV/√Hz
Vamp corner frequency	15Hz
Minimum Sid	1×10^{-28}A^2/Hz
Minimum Id	30pA
Maximum voltage	±200V
Maximum current (>0.1A Measurement needs external test jig)	>±0.1A e.g. >1A
Noise measurement time (Typical data)	32 sec

Figure 5. A-LFNA enables turnkey noise measurements for 1/f noise and RTN in all types of semiconductor devices

Features

- Allows extremely low noise measurement, such as transistor linear region noise, and noise measurement in extremely low bias current
- Measures high-power device noise even in a high current like 1A
- Measures DC characteristics, 1/f noise, and random telegraph noise in less time and with fewer steps and conducts data analysis
- Enables a complete integrated on-wafer solution with automated control of all major wafer probing systems through FormFactor partnership

Model Builder Program (MBP)

Keysight MBP is a complete modeling solution that integrates SPICE simulation, model parameter extraction, and model library generation. It supports the latest standard models, including BSIM-BULK, BSIM-CMG, and BSIM-IMG, for logic, analog, and RF designs.

In addition to compact models, MBP supports macro (subcircuit) and Verilog-A models.

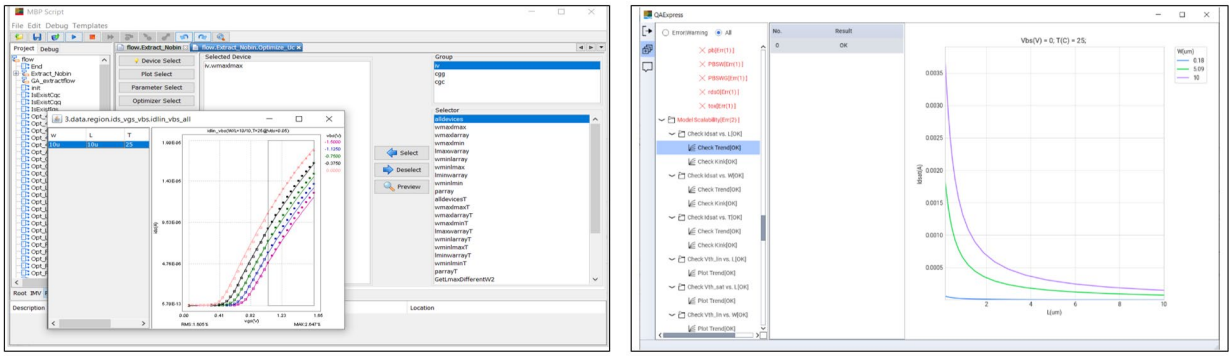


Figure 6. Examples of MBP automated extraction flow and QA Express

Key features

- Automated, fully customizable extraction flow for industry-standard models, allowing for accessing MBP functions via script API and running Python scripts
- QA Express, a one-click model QA function during model parameter tunning, which supports pre-defined check function and customizable geometry, bias, and rule to check
- Comprehensive support for local mismatch, global statistical models, re-centering, and corner tweaking
- Internal SPICE engine – Real-time model simulation and parameter tuning
- Aging model support – MOSRA Level 1,3, API; AgeMOS, URI; TMI
- Advanced HSPICE Link – A new and exclusive link to PrimeSim HSPICE
- Model creation without programming – Equation Viewer, IMV/DP support, customization of modeling graphs, parameter guide, etc.

IC-CAP

Keysight IC-CAP is the industry standard software for characterizing and modeling DC, analog, and RF semiconductor devices. IC-CAP extracts accurate models and sub-circuits for high-speed/digital, analog, power electronics, and power RF applications. It offers device engineers and designers a state-of-the-art modeling tool that fills numerous modeling needs, including automated instrument control, data acquisition, parameter extraction, graphical analysis, simulation, optimization, and statistical analysis. IC-CAP combines these capabilities in a flexible, automated, and intuitive software environment to extract efficiently and accurately active, passive, and user-defined devices and circuits.

Model Generator (MG) is a new workflow manager in IC-CAP that helps device modeling engineers perform model extraction on any device 30% faster.

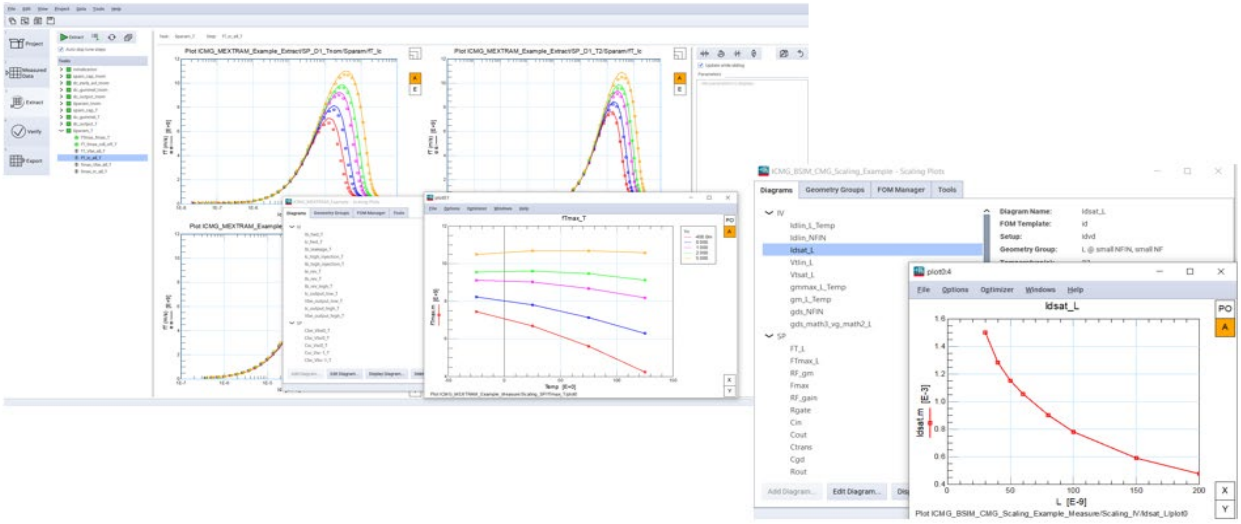


Figure 7. Examples of extraction flow and scaling plot with IC-CAP MG

In addition, Model Generator Recentering uses tuning and optimization techniques to efficiently adjust important parameters to adapt the model to the new targets.

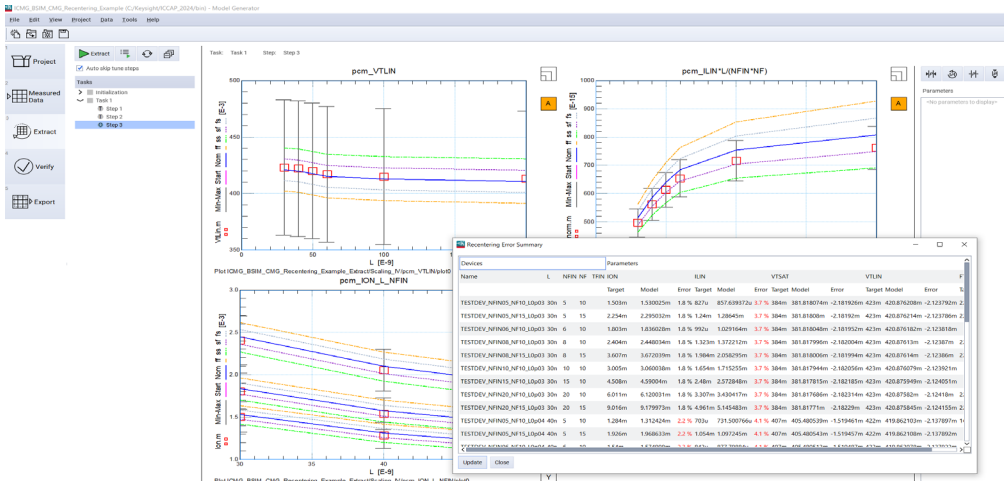


Figure 8. An example of re-centering with IC-CAP

The Keysight ANN implementation in IC-CAP has unique capabilities compared to other ANN solutions as it generates ANN from partial derivative data. It enables the fastest possible device or circuit evaluations in any design phase. Engineers can explore the circuit consequences of novel technologies where models are unavailable or inaccurate.

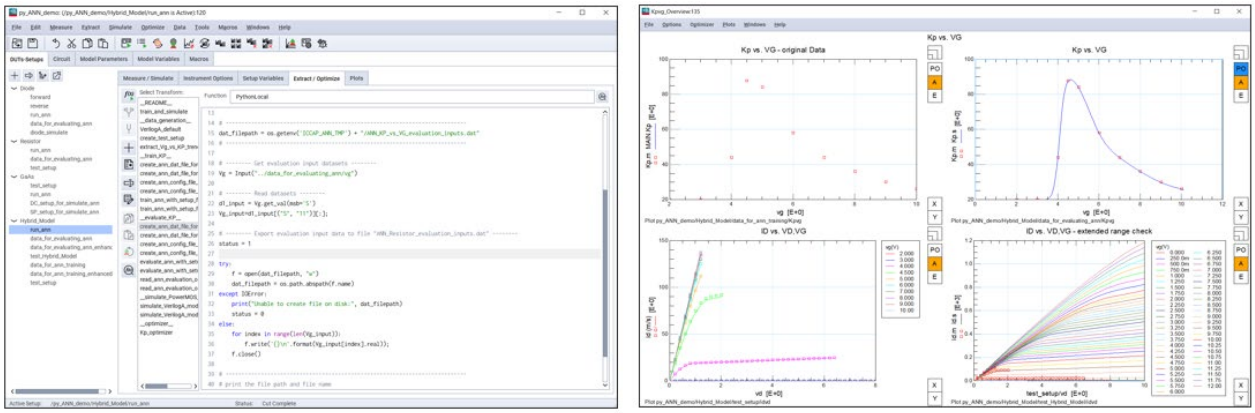


Figure 9. Examples of ANN modeling with IC-CAP

Silicon and III-V modeling packages and examples

IC-CAP provides powerful turnkey extraction packages for various device models.

- CMC industry-standard CMOS models: BSIM3, BSIM4, BSIMSOI, PSP, HiSIM, BSIM-BULK, and HiSIM_HV. The CMOS Extraction packages share the same architecture, making it possible to use the same measured data to extract different CMOS models.
- Comprehensive BJT and HBT model packages for VBIC, Gummel Poon, Keysight ADS HBT, and Mextram models.
- If you are new to GaN modeling or the new CMC models, the IC-CAP CMC GaN basic extraction flow examples for ASM-HEMT and MVSG_CMC can save you valuable time. Keysight developed the extraction flow in collaboration with the model developers. The step-by-step extraction guide lets you quickly learn the model fundamentals and how to extract the core parameters.

Silicon	
CMOS modeling	BSIM3 BSIM4 BSIMSOI PSP HiSIM HiSIM_HV
BJT and HBT modeling	VBIC Gummel-Poon MEXTRAM

III-V	
GaN modeling	ASM-HEMT MVSG_CMC Angelov-GaN Keysight DynaFET
GaAs modeling	EEHEMT Angelov
InP modeling	ADS HBT

Figure 10. IC-CAP provides extraction routines for industry-standard and Keysight proprietary models

Learn more about other supported models in IC-CAP

Model Quality Assurance (MQA)

Keysight MQA offers a collection of comprehensive SPICE model validation procedures, interfaces, and utilities that can thoroughly check SPICE model quality and automate QA and reporting procedures for silicon and III-V technologies. MQA meets critical industry requirements by rigorously checking model quality, plotting model characteristics, and customizing output targets with comprehensive rules while employing easy-to-use interfaces and utilities.

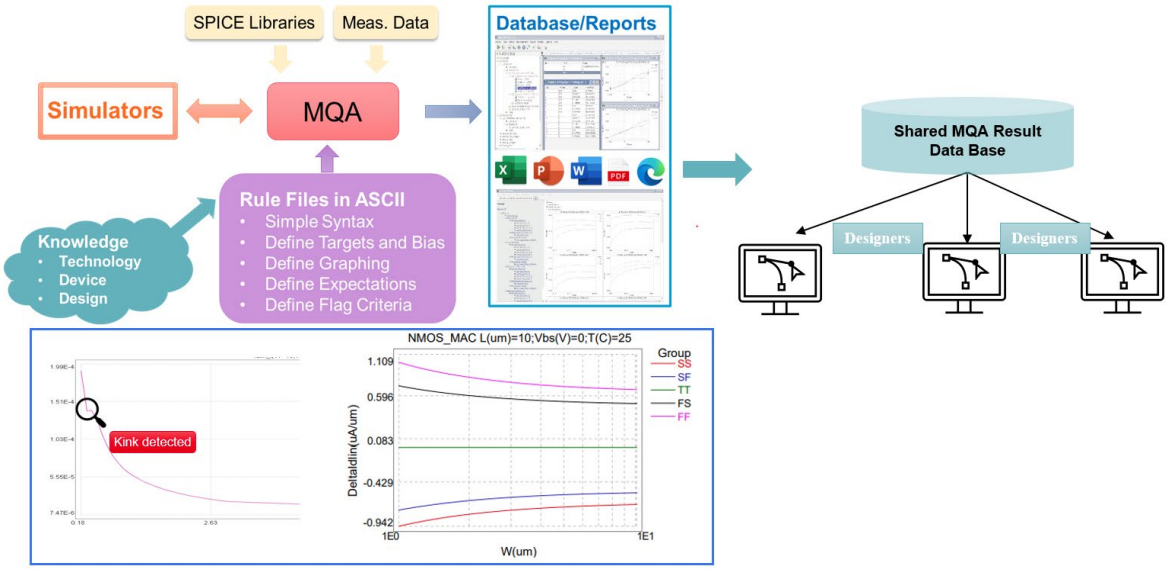


Figure 11. A workflow for model verification

Features

Qualification tools

- Flexible and fully customizable rules and checking functions
- Measurement QA, model comparison, corner model QA, and Monte Carlo analysis
- Integrated rules to ensure quality while overlaying measured data and simulation
- Customizable user-defined plots and tables with Python script

Design interface (foundry interface) tool

- Support for different commercial simulators to ensure industry-standard results

Documentation tool

- Automatic QA report generation and customization
- Templates supporting Word, PowerPoint, and HTML formats

Advanced Design System (ADS)

Keysight Advanced Design System (ADS) is Keysight's leading RF, microwave, signal integrity, and power integrity design platform. It combines schematic, layout, circuit, electro-thermal co-simulation, and three full-wave 3D EM technologies with Integrated Circuit (IC), package, laminate, PCB, and 3D EM component co-design in one software tool to dramatically improve productivity and reduce cost. ADS works closely with foundries and component vendors to provide simulation libraries to its extensive installed base of over 25,000 users.

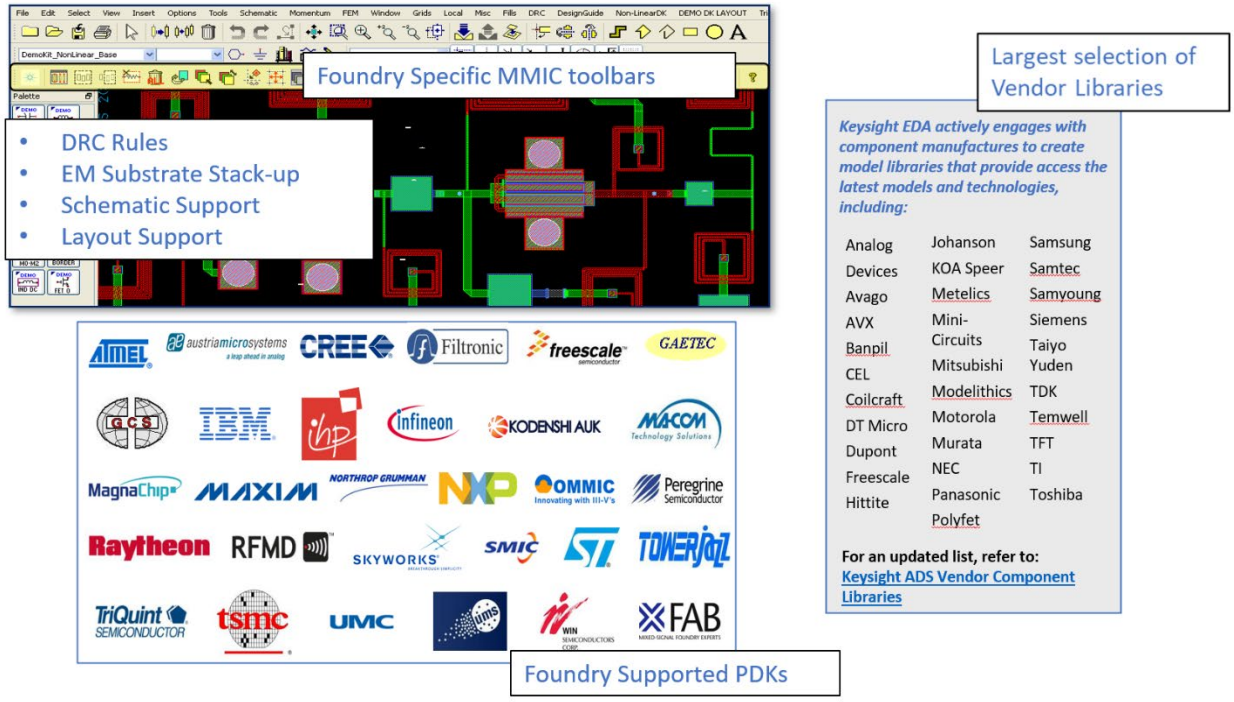


Figure 12. Foundry PDKs for ADS enable the design success of RFIC, MMIC and RF modules

To accelerate design cycles, ADS provides:

- Easy-to-use DesignGuides, including over 300 examples covering specific application circuits, tutorials, wizards, pre-configured set-ups and displays, and best practices
- Direct, native access to 3D planar and full 3D EM field solvers
- Broadest RF and MW PDK coverage, endorsed by leading foundry and industry partners
- EDA and design flow integration with companies such as Cadence, Mentor, and Zuken
- Optimization Cockpit for real-time feedback and control when using any of 12 powerful optimizers
- X-parameter model generation from circuit schematic and Keysight's Nonlinear Vector Network Analyzer (NVNA) for nonlinear high-frequency design
- Up-to-date Wireless Libraries for design and verification of the emerging wireless standards

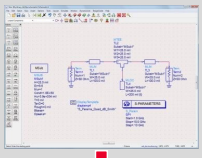
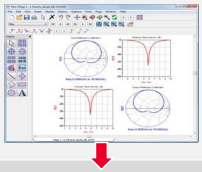
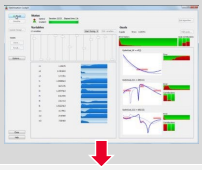
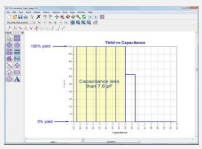
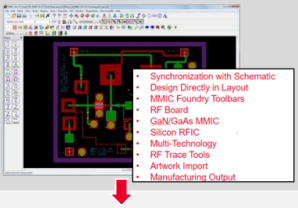
ADS front end design	Features
	**Schematic capture** • Enables quick, easy entry of schematics and simulation setup • Accelerates first-pass design success with industry-leading simulation technologies • Avoids wasteful hardware iterations
	**Data display** • Powerful post-processing offering valuable design insights • Optimal design performance without multiple re-simulations
	**Tuning** • Quickly and easily achieve desired performance by interactive tuning of any design parameters • Gain design insights from effects of tuned components on circuit performance and sensitivity to component values **Optimization cockpit** • Control circuit optimization to improve performance • Adjust constraints with optimization cockpit to achieve a realizable range of parameter values
	**Statistical analysis** • DFM/Statistical tools identifies sensitive component parameters that affects performance • Reduces sensitivity to process variations • Increases production yield

Figure 13. Front-end design with ADS

ADS back-end design	Features
	**RF layout** • Offers a full-featured RF Centric layout tool, • Generates and assembles multi-technology layouts of RF modules, RFIC, MMIC, and RF PCB • Integrates with RFPro 3D EM simulator

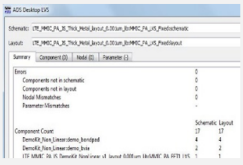
	**Layout verification**
	• ADS integrated and interactive desktop, ensuring RF physical layouts are ready for production
	  • Design Rule Check (DRC)
	  • Layout Vs. Schematic (LVS)

Figure 14. Back-end design with ADS

RFPro

Keysight RFPro is an electromagnetic design environment for RF and microwave circuit designers. It automates EM circuit co-simulation to account for EM effects on circuit performance in 3D IC layouts, packaging, interconnects, transitions, and PCB boards.

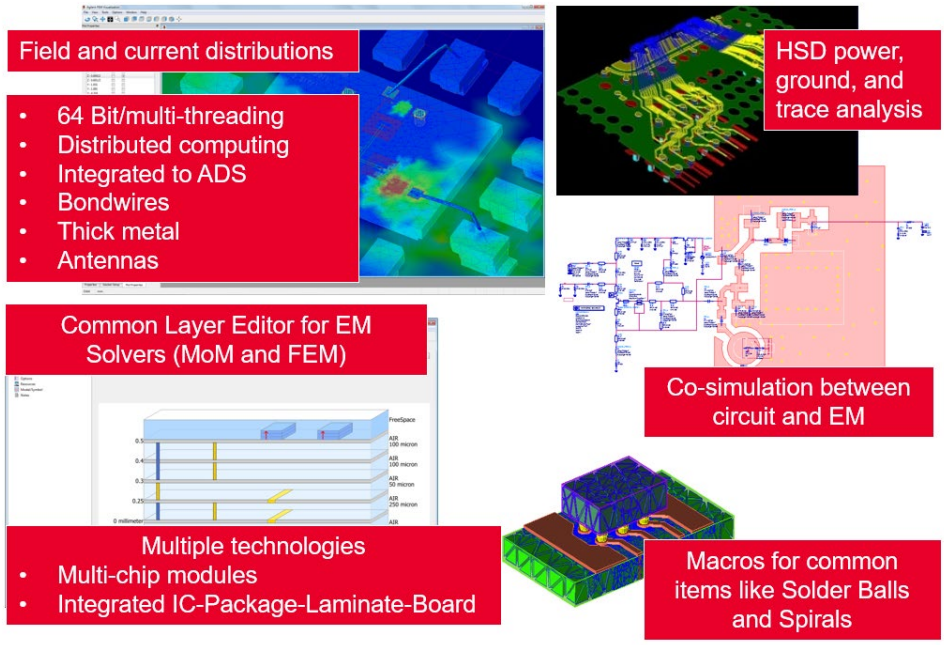


Figure 15. Run 3D EM analysis with RFPro to account for all EM effects on circuits

Through seamless integration with ADS, RFPro enables interactive access to EM analysis for tuning and optimization of RF circuits during design just like circuit simulators.

Integration	Solver	Layout
1. IC and packaging EM-circuit analysis in a single environment with an interactive 3D view	1. Full 3D FEM and planar 3D Momentum solvers from the same environment	1. Interactive EM simulation on any section of the layout without manual isolation (“cookie cut”)
2. Same interface for Keysight ADS, Cadence Virtuoso, Synopsys Design Compiler, and Mentor Tanner	2. Automatic expert setup of EM and EM-circuit analysis ensures trustworthy results	2. No need to manually extract EM and circuit components for separate simulation
3. Preserves OpenAccess (OA) design database integrity without the need for file translations	3. Sweep physical and electrical parameters easily from the same environment	3. Automatic data stitching of EM ports to circuit nodes for error-free EM-circuit co-simulation
4. Maintains full traceability of EM data origin from design changes and simulator used	4. The same interface to launch the HFSS solver	

Chiplet PHY Designer

Keysight has introduced Chiplet PHY Designer, a high-speed digital design and simulation tool. It provides Die-to-Die (D2D) interconnect simulation, crucial for verifying performance in heterogeneous and 3D Integrated Circuit (IC) designs, commonly known as chiplets. This electronic design automation (EDA) tool is the industry's first to offer in-depth modeling and simulation capabilities, enabling chiplet designers to verify compliance with the Universal Chiplet Interconnect Express™ (UCIe™) standard. UCIe is emerging as the leading chiplet interconnect specification, fostering a broad ecosystem for chiplet interoperability and commerce.

The Chiplet PHY simulator analyzes the impact of forward clocking using single-ended signaling and higher bit error rates on the die-to-die interconnect performance of chiplets. It models and simulates UCIe-based compliance measures, including the voltage transfer function. Leveraging Keysight EDA's technology and successful track record in simulating complex physical layer standards (such as SerDes and memory), this simulator contributes to chiplet design and validation.

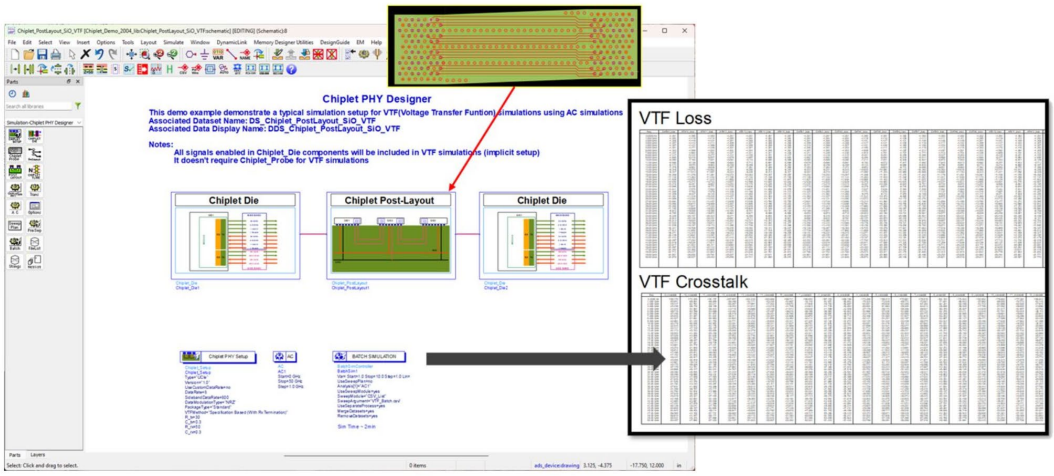


Figure 16. Keysight EDA's unique and powerful solution for Chiplet System Design.

Features

- Supports UCIe physical layer standard – automated parsing of signals following the standard naming conventions, automated connections between multiple dies through package interconnects, standard driven simulation setup such as speed grade, and intuitive measurement setup through specialized probe component.
- Measurement of Voltage Transfer Function (VTF) – precisely computes a VTF to ensure UCIe specification compliance
- Support for different commercial simulators to ensure industry-standard results

Electro-Thermal (ETH) Simulation for III-V Foundry

Keysight ETH simulation suite integrates with the transient and steady-state circuit simulators in ADS to enhance circuit simulation accuracy. It accurately models the layout-dependent, localized electro-thermal effects that impact device characteristics and degrade RF/Microwave circuit performance and reliability, which traditional circuit simulations often overlook.

Based on Keysight's industry-proven Heatwave simulation technology, the ETH simulation suite enables the accurate design of amplifiers and densely integrated RF modules that must handle not only steady-state but also transient pulsed and modulated RF signals.

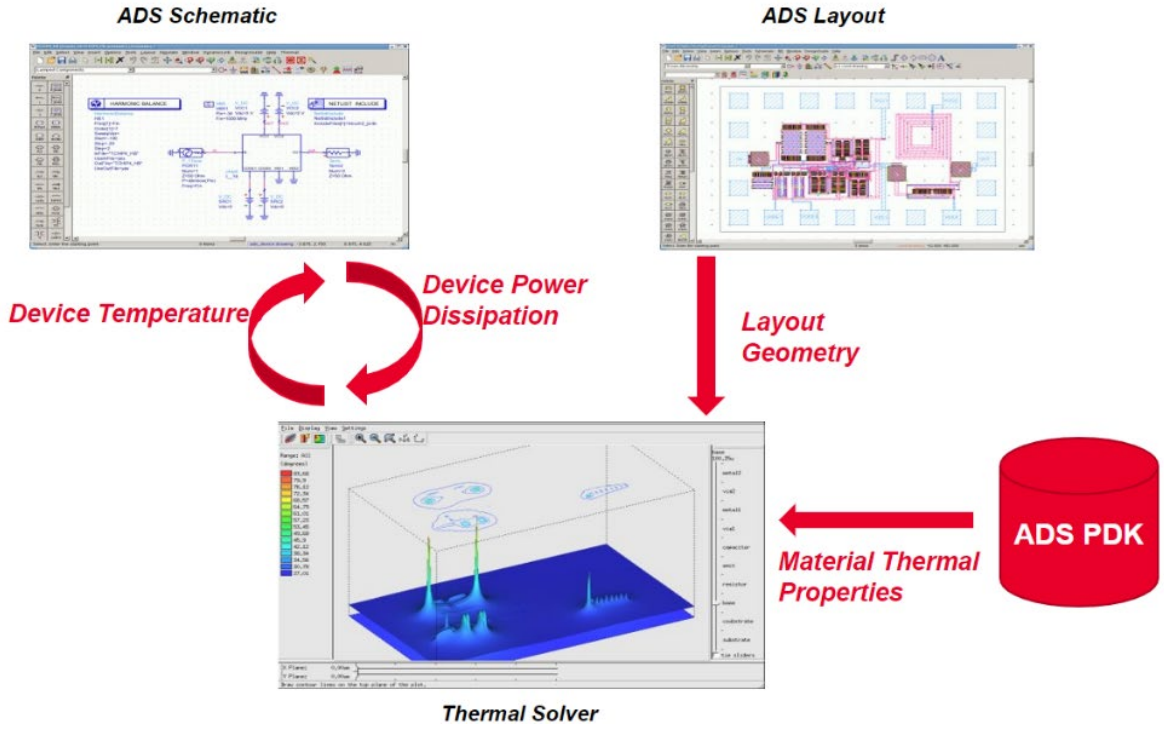


Figure 17. Keysight Electro-Thermal (ETH) simulation solution

The ETH simulation suite significantly accelerates transient electro-thermal simulations—typically by 10x and up to 100x—enhancing RF performance and electro-thermal reliability during iterative design rather than one-time signoff verification.

This tool also enables predictable dynamic electro-thermal simulations, such as RF performance and reliability degradation under pulsed and modulated signal excitation and the location and timing of detrimental transient temperature spikes, allowing for proactive mitigation before hardware production and deployment.

Moreover, for every 10 degrees Celsius of localized temperature increase, the time to failure (MTTF) of an electronic component is reduced by ½. Thus, device temperature data monitoring is vital to avoid costly post-deployment failures, recalls, and reparations. The ETH simulation ssuite enables 3D temperature mapping to enhance layout design robustness.

Process and Data Management

Keysight Design Data Management (SOS) and IP Management (HUB) help foundries streamline PDK development and release cycles by providing a single source of truth for all the pieces of data that make up the PDK. They facilitate design and knowledge-sharing processes and automate the release workflows with custom technical and legal / compliance signoffs.

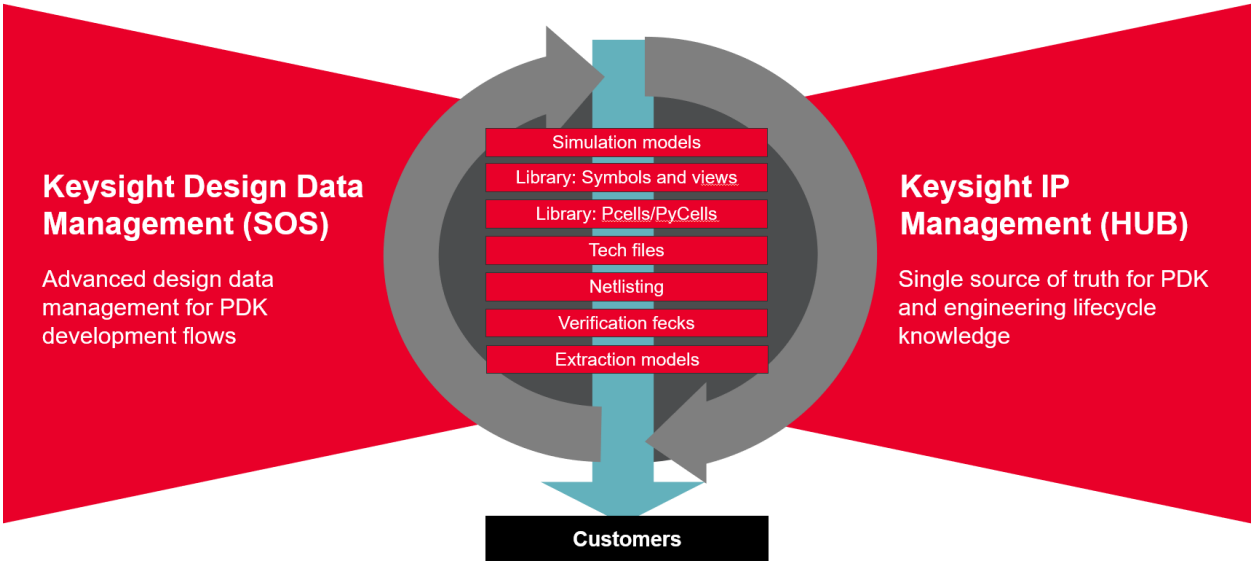


Figure 18. Keysight process and data management for foundries

Keysight SOS is a flexible, scalable, and secure platform for managing hardware designs and projects from concept to tape-out.

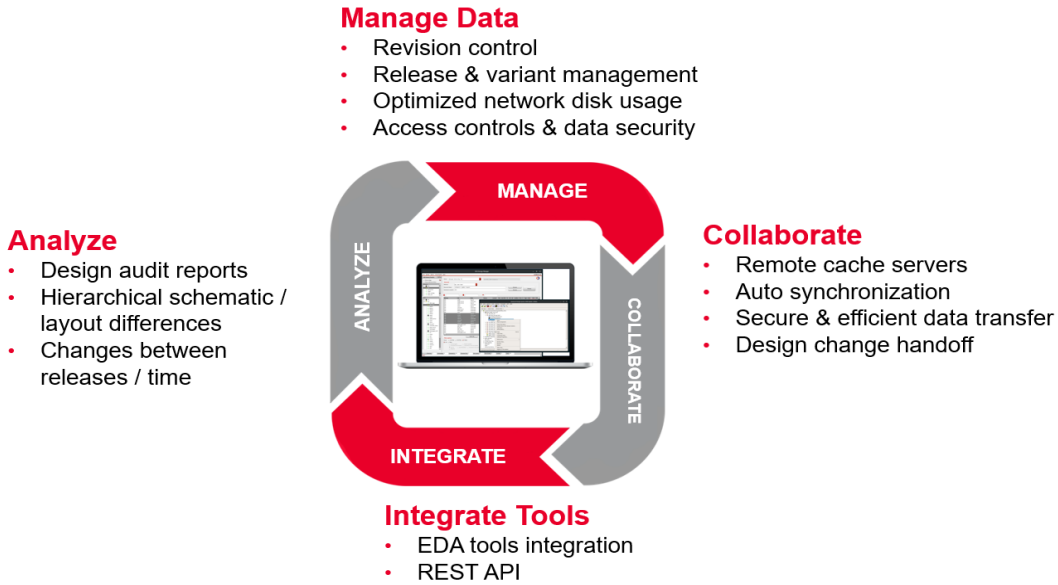


Figure 19. Keysight Design Data Management (SOS) features

Keysight SOS seamlessly integrates with hardware design tools from Electronic Design Automation (EDA) vendors such as Cadence and Synopsys and software configuration tools like Git, Subversion, and Perforce. The platform also enables advanced revision control, release and derivative design management, and interfaces for issue tracking.

Keysight IP Management (HUB) is designed to streamline the PDK release management process, enhance multi-site collaboration, and elevate design teams' productivity. Keysight HUB optimizes the PDK release workflow by:

- Enhancing tracking of release manifests and tracing releases to customers
- Enabling real-time cross-partner collaboration
- Automating release and legal review and signoff
- Simplifying analytics and compliance reporting

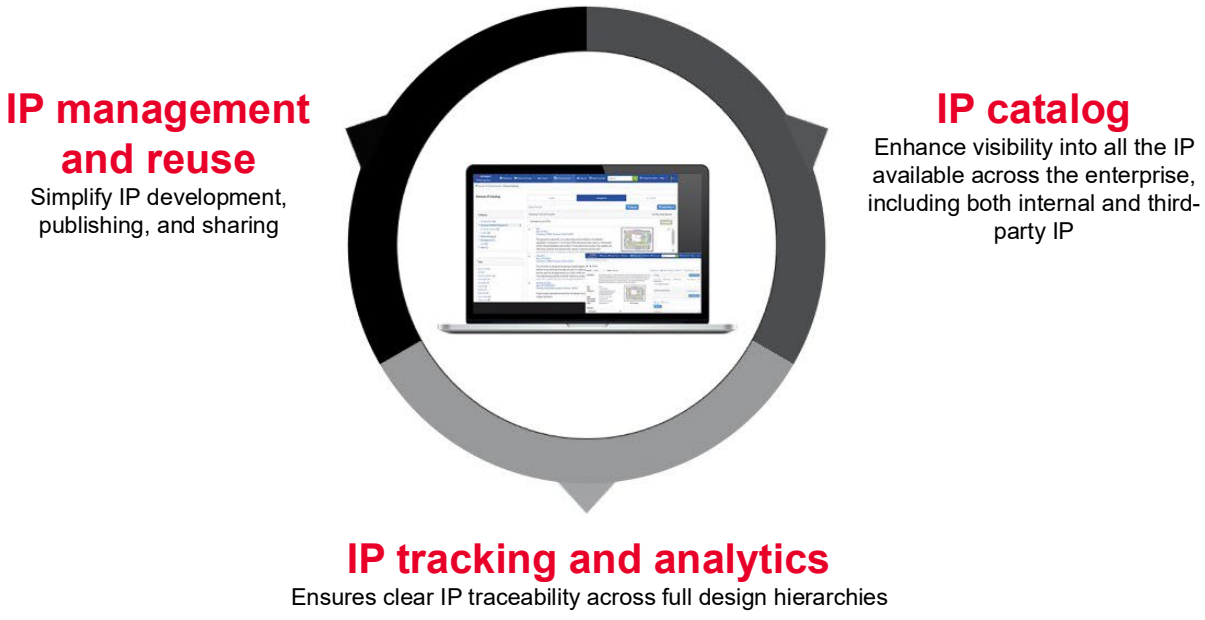


Figure 20. Keysight IP Management (HUB) features

Comprehensive Services for Foundries

At Keysight, we leverage our extensive test and design experience in working with some of the world's largest major foundries and design houses to bring you cutting-edge, tailor-made solutions. Our commitment to excellence, reliability, and innovation defines our comprehensive suite of services. For different foundries, we tailor our solutions to address specific challenges in a targeted manner.

Silicon Foundry Service Solutions

Keysight provides silicon DC, RF, and SOI model test key design solutions crafted to meet the highest standards. As a premium vendor of electrical test and measurement equipment, Keysight Services equips your projects with tools that set industry benchmarks, elevating precision for DC, CV, RF, 1/f noise, and mapping measurements.

Our device modeling services are designed to support every stage of your project—from model extraction to the final quality assurance processes. We provide a full spectrum of modeling tools coupled with diverse extraction packages (i.e., CMOS / FinFET / SOI baseband or RF), ensuring that your project transitions smoothly through each phase.

Expand your project capabilities with our versatile PDK and RDK services tailored for various platforms. Whether you are tackling specialized applications or need broad compatibility, Keysight provides the flexibility and specialized support essential for your project's success.

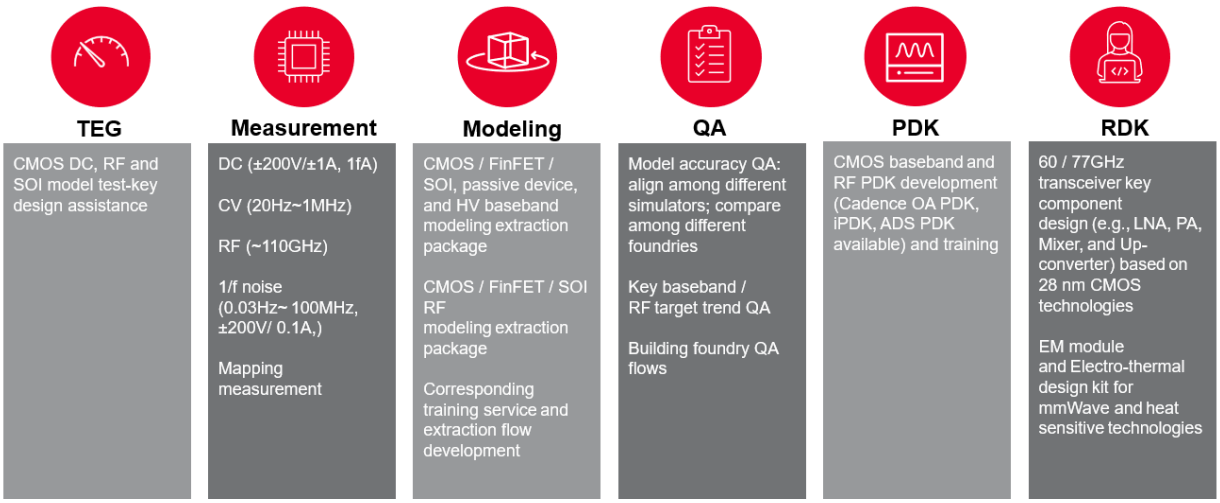


Figure 21. Keysight Services for silicon foundries

III-V Foundry Service Solutions

Keysight Services for III-V foundries combine complete device modeling tools, reference-related experience in worldwide foundries, rapid delivery time, reliable industry partnerships, and integrated training to ensure your team's success. Our professional teams leverage advanced project management methods and global resources to achieve zero failure rates in previous projects.

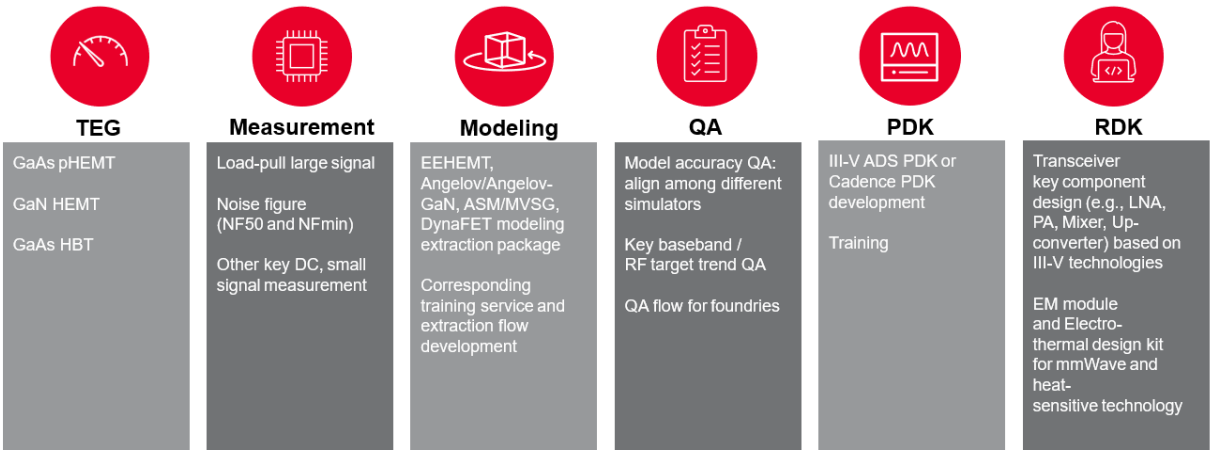


Figure 22. Keysight Services for III-V foundries

Other Services

Behavioral model consulting

The service covers SAW/ BAW resonator, Cryogenic MOS, and linear device modeling

Hybrid ANN modeling consulting

The hybrid-ANN modeling consulting service includes both passive device modeling (inductor, capacitor, and resistor) and active device (FET / HEMT small signal modeling) The model produced by the ANN solution is both general and precise, allowing customers to easily extract it without any prior modeling experience. This generated model is technology-independent, making it simple to maintain. Additionally, the model computes quickly and is infinitely differentiable, ensuring smooth performance.

Basic, 3rd party tool integration and advanced function development

Our comprehensive PDK pipeline ensures project success with excellent multi-platform compatibility and proven expertise from collaborations with large worldwide foundries.

Basic	Third-party tool integration	Advanced
1. Device artworks and symbols: schematic, Pcell, symbols, palate, callback function, model file 2. Rule decks: DRC, LVS 3. ADS EM or RFPro or QuantumPro stack-up files: Substrate structure, derived layers, materials	1. Import of Cadence Virtuoso's layout into Keysight ADS to build the EM structure 2. Export of 3D EM structure into third-party EM tools	1. Customized toolbar development: layout advanced toolbar, editing operation, and shortcut 2. Die symbol auto-creation 3. Other advanced function development (i.e., BOM part number list export, bonding diagram labeling, and custom advanced function) 4. PDK Licensing

Conclusion

The semiconductor industry is at a massive inflection point. On one hand, devices featuring trillions of transistors and wide bandgap semiconductors are making waves across the electronic design industry. The combination of exploding volume of data and more complex models significantly increases pressure to meet time-to-market expectations. On the other hand, regional initiatives such as the CHIPS Act create unprecedented demand and growth opportunities.

Foundry leaders will need to focus strategically on modernizing workflows to boost productivity and unlock areas of opportunity.

Keysight EDA is at the forefront of this shift, working in close collaboration with foundries to deliver high-quality models and PDKs tailored for Si, SiGe, GaAs, InP, and GaN processes. Our software and services form a total solution covering test structure design, device characterization and modeling, PDK creation, validation, and process and data management. Partner with Keysight EDA to innovate faster and smarter beyond Moore's Law.

For More Information

Download IC-CAP Technical Overview and MBP Technical Overview to learn the latest features and model extraction packages.

To extract GaN models more efficiently, read How to Extract the ASM-HEMT Model for GaN RF Devices including Thermal Effects and Trapping Extraction of GaN HEMTs.

Learn our success stories: KIOXIA Accelerates PDK Development by using Keysight Device Modeling Software, Determined the Low-Frequency Noise Source in Cryogenic Operation

Request a free trial of Keysight device characterization and modeling software: IC-CAP, MBP, MQA, and WaferPro Express.