Keysight DDR5 Decoder

User's Guide

KEYSIGHT TECHNOLOGIES

Notices

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CAUTION

A CAUTION notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

Safety Summary

The following general safety precautions must be observed during all phases of operation of this instrument. Failure to comply with these precautions or with specific warnings or operating instructions in the product manuals violates safety standards of design, manufacture, and intended use of the instrument. Keysight Technologies assumes no liability for the customer's failure to comply with these requirements. Product manuals are provided with your instrument on CD-ROM and/or in printed form. Printed manuals are an option for many products. Manuals may also be available on the Web. Go to www.keysight.com and type in your product number in the Search field at the top of the page.

General Do not use this product in any manner not specified by the manufacturer. The protective features of this product may be impaired if it is used in a manner not specified in the operation instructions.

Before Applying Power Verify that all safety precautions are taken. Make all connections to the unit before applying power. Note the instrument's external markings described in “Safety Symbols”.

Ground the Instrument If your product is provided with a grounding type power plug, the instrument chassis and cover must be connected to an electrical ground to minimize shock hazard. The ground pin must be firmly connected to an electrical ground (safety ground) terminal at the power outlet. Any interruption of the protective (grounding) conductor or disconnection of the protective earth terminal will cause a potential shock hazard that could result in personal injury.

Fuses See the user's guide or operator's manual for information about line-fuse replacement. Some instruments contain an internal fuse, which is not user accessible.

Do Not Operate in an Explosive Atmosphere Do not operate the instrument in the presence of flammable gases or fumes.

Do Not Remove the Instrument Cover Only qualified, service-trained personnel who are aware of the hazards involved should remove instrument covers. Always disconnect the power cable and any external circuits before removing the instrument cover.

Cleaning Clean the outside of the instrument with a soft, lint-free, slightly dampened cloth. Do not use detergent or chemical solvents.

Do Not Modify the Instrument Do not install substitute parts or perform any unauthorized modification to the product. Return the product to an Keysight Sales and Service Office for service and repair to ensure that safety features are maintained.

In Case of Damage Instruments that appear damaged or defective should be made inoperative and secured against unintended operation until they can be repaired by qualified service personnel.

CAUTION A CAUTION notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

WARNING **A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.**

Safety Symbols

Table 1 Safety Symbol

Symbol	Description
	Direct current
	Alternating current
	Both direct and alternating current
	Three phase alternating current
	Three phase alternating current
	Earth ground terminal
	Protective earth ground terminal
	Frame or chassis ground terminal
	Terminal is at earth potential
	Equipotentiality
N	Neutral conductor on permanently installed equipment
L	Line conductor on permanently installed equipment
	On (mains supply)
	Off (mains supply)
	Standby (mains supply). The instrument is not completely disconnected from the mains supply when the power switch is in the standby position
	In position of a bi-stable push switch

Symbol	Description
	Out position of a bi-stable push switch
	Equipment protected throughout by DOUBLE INSULATION or REINFORCED INSULATION
	Caution, refer to accompanying documentation
	Caution, risk of electric shock
	Do not apply around or remove from HAZARDOUS LIVE conductors
	Application around and removal from HAZARDOUS LIVE conductors is permitted
	Caution, hot surface
	Ionizing radiation
CAT I	IEC Measurement Category I
CAT II	Measurement Category II
CAT III	Measurement Category III
CAT IV	Measurement Category IV

Compliance and Environmental Information

Table 2 Compliance and Environmental Information

Safety Symbol	Description
	CSA is the Canadian certification mark to demonstrate compliance with the Safety requirements.
	The C-tick mark is a registered trademark of the Spectrum Management Agency of Australia. This signifies compliance with the Australia EMC Framework regulations under the terms of the Radio Communication Act of 1992.
	CE compliance marking to the EU Safety and EMC Directives. ISM GRP-1A classification according to the international EMC standard. ICES/NMB-001 compliance marking to the Canadian EMC standard.

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DDR5 Decoder

User's Guide

1 DDR5 Decoder – Overview

The Keysight DDR5 Decoder software lets you decode and view transactions and commands from a DDR5 SDRAM memory bus in your device under test.

This decoder works with the Keysight Logic and Protocol Analyzer software application (in online / offline mode) to decode the acquired DDR5 traces. The data acquisition can be done using a compatible Keysight Logic Analyzer module. See "Required Hardware, Software, and Licenses" on page 2 for details.

The decoded DDR5 data can then be viewed and analyzed using the Listing window in the Logic and Protocol Analyzer application. DDR5 data is displayed as raw hexadecimal data in this window. The decoder does not inverse assemble the data payload. It shows the decode of the traffic at any given point in the trace.

Flow of steps to use the DDR5 Decoder

1. Install the required software and licenses.
2. Set up the logic analyzer module, probing hardware, and connections to DUT.
3. Configure the Logic and Protocol Analyzer software setup and DDR5 Decoder settings as per your testing requirements.
4. Capture DDR5 data.
5. View and analyze the decoded data in the Listing window.

Related Tools

- The *DDR Setup Assistant* is a wizard-like application that helps you set up your logic analyzer properly for DDR data capture and analysis. It guides you through the setup process and automates setting threshold voltages and sample positions for control/address signals. For more information, see DDR Setup Assistant - At a Glance.
- The *DDR Eyescan* tool helps you set the logic analyzer threshold and sampling positions for read data and write data signals.
- The *LPDDR5 Decoder* tool to decode and view transactions and commands from an LPDDR5 SDRAM memory bus.
- The *DDR/LPDDR Memory Analysis Viewer* to analyze the captured DDR/LPDDR memory data using various charts and statistical data such as traffic statistics, bus utilization, refresh rate analysis, and data for Read/Write commands.

When to Use the DDR5 Decoder

There are situations when the DDR5 Decoder is more suitable and provides key benefits as compared to the Keysight DDR/LPDDR Memory Analysis viewer. Following are examples of such situations.

- The DDR5 Decoder does not decode the entire trace in one go. At a time, it decodes only that specific portion of your trace that you are currently viewing in its Listing window. This significantly reduces the time it takes to decode and display results. This is especially useful when you have a long trace to decode and you want to immediately view the decoded information.

- The DDR5 Decoder can show information from multiple subchannels of your DDR5 memory design in a single Listing window. The subchannels information is time-correlated and presented as separate columns in a single listing window. This eliminates the need to have a separate viewer for each subchannel's information.

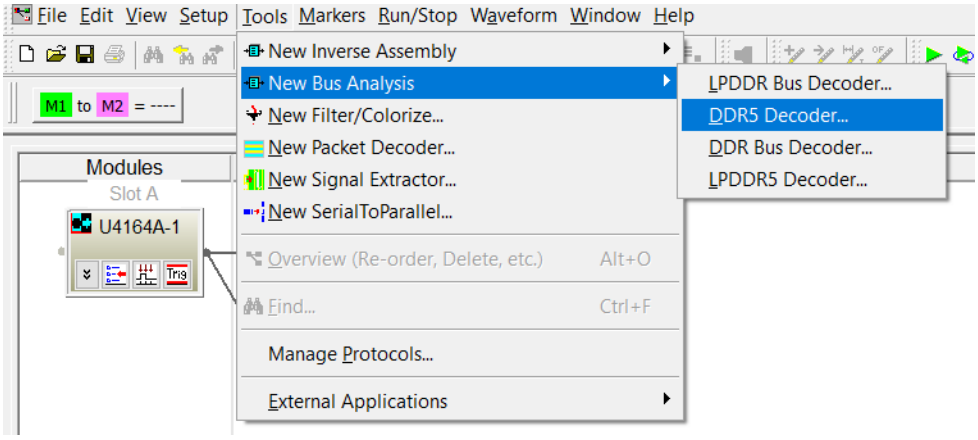
While DDR5 Decoder has key strengths, it is recommended to use the DDR/LPDDR Memory Analysis viewer instead of DDR5 Decoder in the following situations:

- If you want to specify how your SDRAM address components (rank, bank, row, and column addresses) are used to construct an overall physical address so that the reconstructed address can be displayed for each read or write operation. then you should use the DDR/LPDDR Memory Analysis viewer. The DDR5 Decoder does not support physical address reconstruction.
- If you want to view the details (memory address and Read/Write data) for the individual Read or Write commands, then you should use the Details tab of the DDR/LPDDR Memory Analysis viewer. The DDR5 Decoder does not show the data associated with a Read or Write command.
- If you want to do higher-level analysis such as analyzing your SDRAM's traffic statistics, Refresh rate, or performance measurements for data transfer rates and memory utilization, then you should use various charts and statistics provided in different tabs of the DDR/LPDDR Memory Analysis viewer. The DDR5 Decoder does not provide any of these higher-level analysis features and is focused on displaying traffic decode at a given point in the trace.

Required Hardware, Software, and Licenses

Required Hardware	Required Software	Required License
▪ U4164A Logic Analyzer module to capture DDR5 data ▪ DDR5 memory bus probes such as W5643A DDR5 78-ball BGA Interposer	▪ Logic and Protocol Analyzer software version 7.0 or higher ▪ DDR5 Decoder software These can be downloaded and installed from: www.keysight.com/find/lpa-sw-download	No separate license is needed specifically for the DDR5 Decoder. However, you must have installed the following standard memory license for DDR5. *B4661A-5TP/5FP/5NP DDR5 Analysis and Compliance Validation license* Without this license, you can only view and analyze the decoded DDR5 data from an existing .ala file in offline mode.

On installing the DDR5 Decoder software, you can access this tool from the following location in the Logic and Protocol Analyzer GUI.



2 Setting Up DDR5 Bus Decode

The topics in this section describe how to set up the logic analysis system hardware and software components for DDR5 bus decode.

Hardware Setup for DDR5 Bus Decode

1. Connect the probe to your device under test (DUT).
2. Connect the logic analyzer pods to the probe.

Each probe has its own user's guide that describes in detail how to make these connections. You can download the user's guide from the probe's page at www.keysight.com.

CAUTION When you are working with the logic analyzer, be sure to power down both the analyzer and device under test before disconnecting or connecting cables or probes. Otherwise, you may damage circuitry in the analyzer or device under test.

Logic Analyzer Measurement Setup for DDR5 Bus Decode

To configure the Logic Analyzer measurement setup for DDR5 decode, you use the DDR Setup Assistant. This tool is available at no charge as part of the Keysight B4661A memory analysis software package.

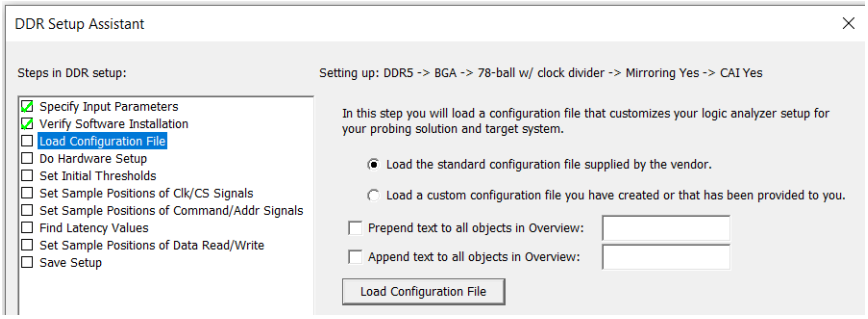
The DDR Setup Assistant is a wizard-like application that helps you set up your logic analyzer properly for DDR data capture and analysis. This tool simplifies the measurement setup by guiding you through the setup process and automating the threshold voltages and sample positions settings for control/address signals.

The following two scenarios are applicable when using the DDR Setup Assistant to create Logic Analyzer measurement setup.

Scenario 1: You are using a standard probing solution

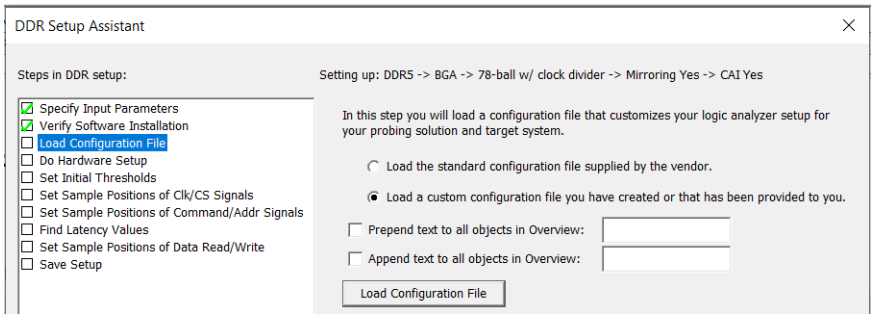
In this case, a standard DDR5 configuration file is available for the probing solution being used. A set of standard DDR5 configuration files is provided when you install the DDR5 Decoder software.
The DDR Setup Assistant wizard automatically:

- loads the appropriate standard configuration file matching the standard probing solution details that you provided in the wizard.
- sets the required buses and signals.
- adds the DDR5 Decoder tool and a Listing window in the Logic and Protocol Analyzer GUI.



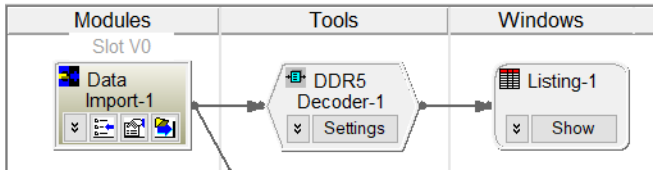
Scenario 2: You are using a custom probing solution

In this case:
1. Create your own custom DDR5 configuration file. You use the DDR Custom Configuration Creator tool installed with the B4661A Memory Analysis SW package to create custom files.
2. Run the DDR Setup Assistant and load your custom configuration file in the third step of the wizard as shown below.



See: "To create a configuration file" on page 6

Sample Logic Analyzer Setup for DDR5 Decode



NOTE In the logic analyzer measurement setup, the DDR5 Decoder tool can be attached to the U4164A Logic Analyzer module or a Data Import module as displayed in the above screen. You can also attach a Filter tool to the DDR5 Decoder tool to filter the decoded data display based on your specific analysis requirements. But you cannot attach the DDR5 Decoder tool to another decoder or Memory Analysis Viewer.

To create a configuration file

The Keysight-provided configuration files are valid only when used with the corresponding memory probe and DRAM for which these are designed.

If you are using some other probing scheme or have a unique DRAM configuration that is not addressed by these standard configuration files, then you must create your own configuration file using the DDR Custom Configuration Creator tool. This tool simplifies the procedure of custom configuration file creation and ensures that all the layout information (buses and signals definitions) needed by DDR5 Decoder is included in the created configuration file.

This tool is included in the Keysight B4661A DDR/LPDDR Tools package and is available only after you install this package.

To know more about this tool, refer to its online help that gets installed with this tool's software.

To configure DDR5 Decoder Settings

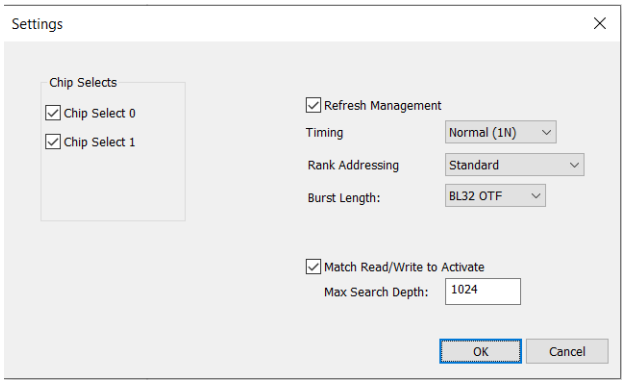
To ensure that the acquired DDR5 data is decoded accurately, you need to configure the DDR5 Decoder settings. Use the Settings dialog to tell the decoder which chip selects will be used by your device under test and to specify how the decoder should work.

To access the Settings dialog

From the main menu bar, select **Tools** > **DDR5 Decoder** > **Settings**.

or

In the **Overview** display, click the **Settings** button on the DDR5 Decoder tool.



Field	Description
Chip Selects	You must enable all chip selects that are being used in the system to ensure that the decoder functions correctly. Likewise, any chip selects that are not used must not be enabled.
Refresh Management	Select this checkbox if your DDR5 bus is using the Refresh Management (RFM) feature and therefore you want to instruct the decoder to account for the occurrence of Refresh Management commands.
Timing	Select the Timing option that matches the timing mode in which your memory bus is operating.
Rank Addressing	Select the appropriate rank addressing mode option based on the rank addressing being used for your DDR5 bus. In the Standard rank addressing, there is one CS# (chip select) line for each rank. In the 3DS rank addressing, there is only one CS# line for all ranks. Therefore, the logical value of the C (Chip ID) bits is used to identify the rank being addressed in the decode. The number of Chip ID bits to be used for rank identification is as per the 3DS specifications. From the available 3DS rank addressing options (2-high, 4-high, 8-high, or 16-high), select the appropriate option based on whether your 3DS device has two, four, eight, or sixteen logical ranks.
Burst Length	Select the burst length applicable to your SDRAM that is, how many data bytes are written to or read from the SDRAM after a Read or a Write command is given along with row and column address. The burst length options vary depending on the memory type. The option BL32 OTF (On the Fly) indicates that burst length can vary for each Read/Write command. If you select this option, the decoder automatically determines if the burst length of the operation is 16 or 32. The option BC8 OTF (On the Fly) indicates that burst length can vary for each Read/Write command. If you select this option, the decoder automatically determines if the burst length of the operation is 8 or 16.
Match Read/Write to Activate	Select this checkbox if you want the decoder to match the Read and Write commands to the corresponding Activate commands in the captured data.
Max Search Depth	This field is enabled only when you select the Match Read/Write to Activate checkbox. This field allows you to specify the limit for the number of row addresses that the Decoder should search to find a matching Activate corresponding to a Read or a Write command in the captured data. The default value is 1024. This limit is specially useful when: - you have qualified the storage to NOT store the Activates. - the Activate may not be available for some read/write commands. For instance, during the initialization phase of the DDR5 bus. By specifying a shorter search limit, you can significantly reduce the processing time taken by the decoder in searching extensively for the matching Activates in situations such as those mentioned above. However, if you notice that the search limit is so short that the Activates present in the trace are not being found by Decoder and the decode for Read/Write is showing "Row Address = Unknown", then you can increase this limit.

Sampling Positions

Sampling positions tell the logic analyzer when each signal is valid. Correct sampling positions are required for Command and Address, Read Data, and Write Data to reliably capture data on your bus.

NOTE The DDR Setup Assistant tool automatically sets the required sampling positions on your DDR command, address, and data read and write signals.

If you need assistance in setting sampling positions correctly, please contact your Keysight Technologies representative.

3 Capturing Data

To capture data, the logic analyzer must run a measurement and then end the measurement (either manually or by detecting a trigger).

1 Set the logic analyzer with the desired trigger.
2 Run the logic analyzer.
3 Run the device under test.

The logic analyzer will trigger when the specified condition is found on the bus.

4 Understanding DDR5 Decode Displayed in the Listing Window

The decoded DDR5 bus data is displayed as various columns in the Listing window. These columns can be categorized in the following two categories:

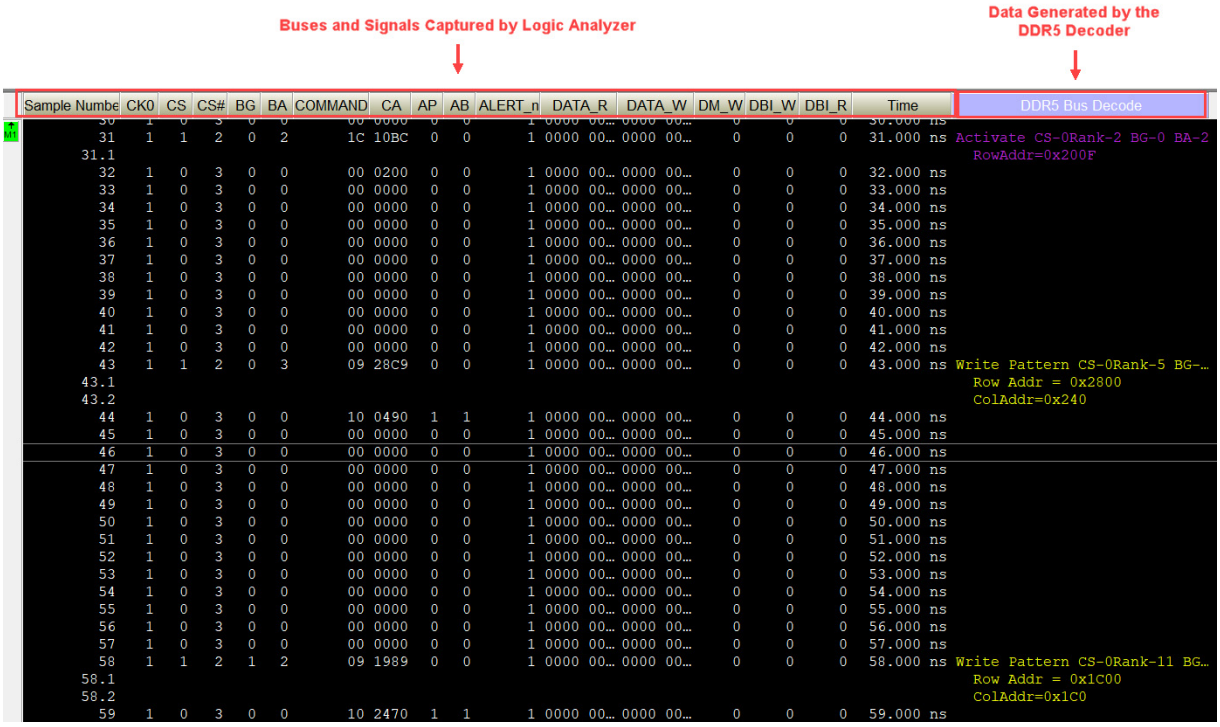
- Buses and signals captured by logic analyzer
- Data generated by the DDR5 Decoder

NOTE

The DDR5 buses / signals labels displayed in the Listing differ based on whether or not the probe that you are using has a clock divider.

When a probe is used with a clock divider, the logic analyzer clock runs at half the speed of the DDR5 bus clock and the dual sampling mode is used to capture two samples of the DDR5 bus per clock edge.

These dual samples require two labels for each signal (one for each sample). For example, CS_1ST# and CS_2ND# labels for the two samples of CS#.



Sample Numbe	CK0	CS	CS#	BG	BA	COMMAND	CA	AP	AB	ALERT_n	DATA_R	DATA_W	DM_W	DBI_W	DBI_R	Time	DDR5 Bus Decode
31	1	1	2	0	2		1C 10BC	0	0	1	0000 00…	0000 00…	0	0	0	31.000 ns	Activate CS-0Rank-2 BG-0 BA-2
31.1																	RowAddr=0x200F
32	1	0	3	0	0		00 0200	0	0	1	0000 00…	0000 00…	0	0	0	32.000 ns	
33	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	33.000 ns	
34	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	34.000 ns	
35	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	35.000 ns	
36	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	36.000 ns	
37	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	37.000 ns	
38	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	38.000 ns	
39	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	39.000 ns	
40	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	40.000 ns	
41	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	41.000 ns	
42	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	42.000 ns	
43	1	1	2	0	3		09 28C9	0	0	1	0000 00…	0000 00…	0	0	0	43.000 ns	Write Pattern CS-0Rank-5 BG-…
43.1																	Row Addr = 0x2800
43.2																	ColAddr=0x240
44	1	0	3	0	0		10 0490	1	1	1	0000 00…	0000 00…	0	0	0	44.000 ns	
45	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	45.000 ns	
46	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	46.000 ns	
47	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	47.000 ns	
48	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	48.000 ns	
49	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	49.000 ns	
50	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	50.000 ns	
51	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	51.000 ns	
52	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	52.000 ns	
53	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	53.000 ns	
54	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	54.000 ns	
55	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	55.000 ns	
56	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	56.000 ns	
57	1	0	3	0	0		00 0000	0	0	1	0000 00…	0000 00…	0	0	0	57.000 ns	
58	1	1	2	1	2		09 1989	0	0	1	0000 00…	0000 00…	0	0	0	58.000 ns	Write Pattern CS-0Rank-11 BG…
58.1																	Row Addr = 0x1C00
58.2																	ColAddr=0x1C0
59	1	0	3	0	0		10 2470	1	1	1	0000 00…	0000 00…	0	0	0	59.000 ns	

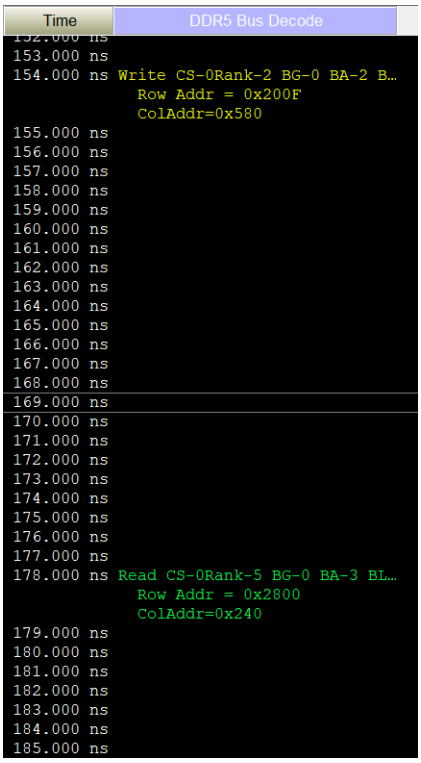
Data Generated by the DDR5 Decoder

The decoder generates the following column, which is displayed in the listing in addition to the input buses captured by logic analyzer.

DDR5 Bus Decode

This column contains decoded data from the memory bus. Decoded commands may cover two or rows (a main row and subrow(s)).

The following screen shows a sample DDR5 decode column.

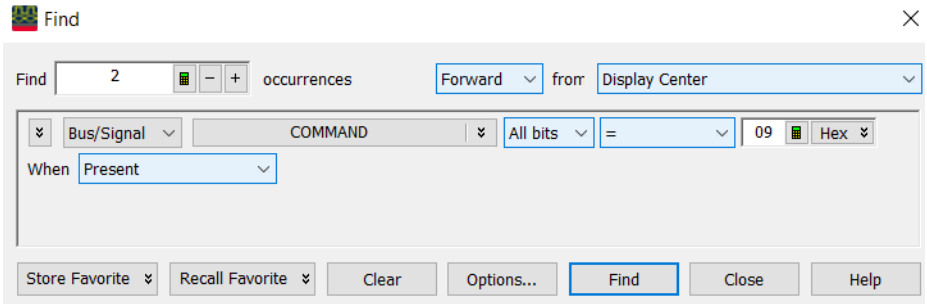


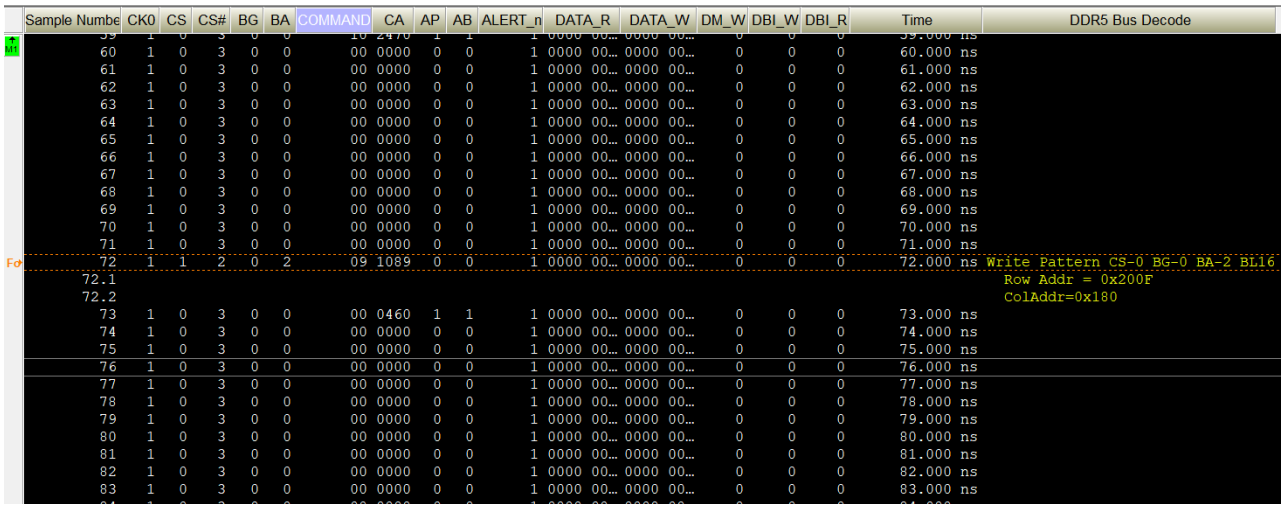
Decode Errors

The decoder cannot decode a state if you have not enabled one ore more chip selects or if the input buses/signals required by the decoder are not present.

To find commands of a specific type in the listing

1. Open the Find dialog by choosing **Edit > Find...** from the menu bar.
2. For the bus/signal name, choose **Command**.
3. Select the command you wish to find.
4. Specify the bus/signal pattern event you wish to find.
5. Click **Find**. The occurrence of the specified pattern is highlighted and is placed at the center of the display.





To filter or colorize decoded data display

In the logic analyzer measurement setup, you can add the Filter tool with the DDR5 Decoder tool. The Filter tool lets you specify the filtering criteria based on which the decoded data displayed in the Listing can be shown, hidden, or colorized.

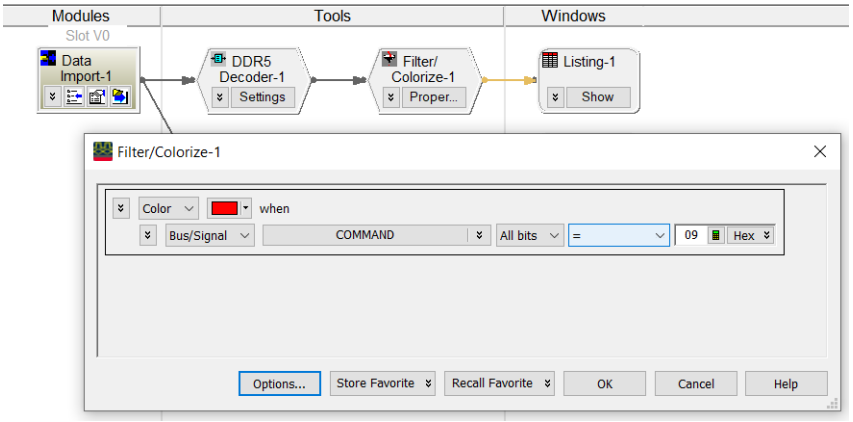
Filtering allows faster analysis in two ways.

First, you can filter unneeded information out of the Listing display. For example, hiding the data for all Chip Selects except the one you are analyzing.

Second, you can isolate particular operations by hiding all other operations. For example, you can show just write commands, without the associated data.

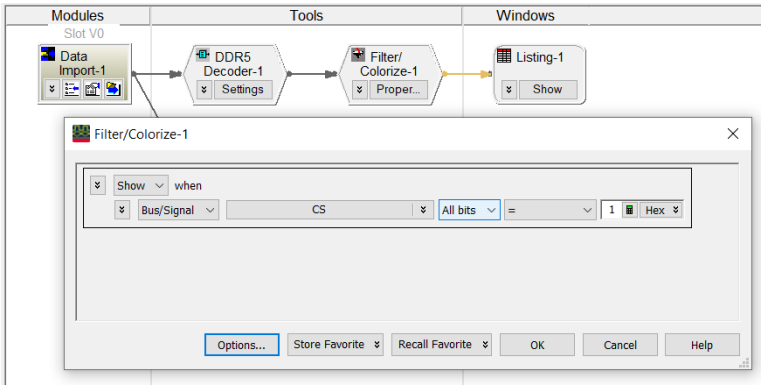
The filter settings filter only the display of data in the Listing. These settings do not filter the data storage by the logic analyzer. You can examine the same data with different settings, for different analysis requirements.

Example of a colorized display in decoded data



Sample Numbe	CK0	CS	CS#	BG	BA	COMMAND	CA	AP	AB	ALERT_n	DATA_R	DATA_W	DM_W	DBI_W	DBI_R	Time	DDR5 Bus Decode
37	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	37.000 ns	
38	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	38.000 ns	
39	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	39.000 ns	
40	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	40.000 ns	
41	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	41.000 ns	
42	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	42.000 ns	
43	1	1	2	0	3	09 28C9	0	0	1	0000 00…	0000 00…	0	0	0	43.000 ns	Write Pattern CS-0 BG-0 BA-3 BL16
43.1																Row Addr = 0x2800
43.2																ColAddr=0x240
44	1	0	3	0	0	10 0490	1	1	1	0000 00…	0000 00…	0	0	0	44.000 ns	
45	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	45.000 ns	
46	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	46.000 ns	
47	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	47.000 ns	
48	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	48.000 ns	
49	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	49.000 ns	
50	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	50.000 ns	
51	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	51.000 ns	
52	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	52.000 ns	
53	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	53.000 ns	
54	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	54.000 ns	
55	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	55.000 ns	
56	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	56.000 ns	
57	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	57.000 ns	
58	1	1	2	1	2	09 1989	0	0	1	0000 00…	0000 00…	0	0	0	58.000 ns	Write Pattern CS-0 BG-1 BA-2 BL16
58.1																Row Addr = 0x1C00
58.2																ColAddr=0x1C0
59	1	0	3	0	0	10 2470	1	1	1	0000 00…	0000 00…	0	0	0	59.000 ns	
60	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	60.000 ns	
61	1	0	3	0	0	00 0000	0	0	1	0000 00…	0000 00…	0	0	0	61.000 ns	

Example - filtering the display based on a particular Chip Select (CS 1 in this example)



Sample Numbe	CK0	CS	CS#	BG	BA	COMMAND	CA	AP	AB	ALERT_n	DATA_R	DATA_W	DM_W	DBI_W	DBI_R	Time	DDR5 Bus Decode
4	1	1	2	0	3	00 28C0	0	0	1	0000 00…	0000 00…	0	0	0	4.000 ns	Activate CS-0 BG-0 BA-3
4.1																	RowAddr=0x2800
18	1	1	2	1	2	00 1980	0	0	1	0000 00…	0000 00…	0	0	0	18.000 ns	Activate CS-0 BG-1 BA-2
18.1																	RowAddr=0x1C00
31	1	1	2	0	2	1C 10BC	0	0	1	0000 00…	0000 00…	0	0	0	31.000 ns	Activate CS-0 BG-0 BA-2
31.1																	RowAddr=0x200F
43	1	1	2	0	3	09 28C9	0	0	1	0000 00…	0000 00…	0	0	0	43.000 ns	Write Pattern CS-0 BG-0 BA-3 BL16
43.1																	Row Addr = 0x2800
43.2																	ColAddr=0x240
58	1	1	2	1	2	09 1989	0	0	1	0000 00…	0000 00…	0	0	0	58.000 ns	Write Pattern CS-0 BG-1 BA-2 BL16
58.1																	Row Addr = 0x1C00
58.2																	ColAddr=0x1C0
72	1	1	2	0	2	09 1089	0	0	1	0000 00…	0000 00…	0	0	0	72.000 ns	Write Pattern CS-0 BG-0 BA-2 BL16
72.1																	Row Addr = 0x200F
72.2																	ColAddr=0x180
90	1	1	2	0	3	0D 28ED	0	0	1	0000 00…	0000 00…	0	0	0	90.000 ns	Write CS-0 BG-0 BA-3 BL16
90.1																	Row Addr = 0x2800
90.2																	ColAddr=0x240
114	1	1	2	1	2	0D 198D	0	0	1	0000 00…	0000 00…	0	0	0	114.000 ns	Write CS-0 BG-1 BA-2 BL32
114.1																	Row Addr = 0x1C00
114.2																	ColAddr=0x1C0
122	1	1	2	1	2	0D 198D	0	0	1	0000 00…	0000 00…	0	0	0	122.000 ns	Write (Dummy)
146	1	1	2	0	2	0D 108D	0	0	1	0000 00…	0000 00…	0	0	0	146.000 ns	Write CS-0 BG-0 BA-2 BL32
146.1																	Row Addr = 0x200F
146.2																	ColAddr=0x180
154	1	1	2	0	2	0D 108D	0	0	1	0000 00…	0000 00…	0	0	0	154.000 ns	Write (Dummy)
178	1	1	2	0	3	1D 28FD	0	0	1	0000 00…	0000 00…	0	0	0	178.000 ns	Read CS-0 BG-0 BA-3 BL16
178.1																	Row Addr = 0x2800
178.2																	ColAddr=0x240

If you want to prevent certain data from being stored, then use the logic analyzer's storage qualification feature.

See Also

The filter/colorize tool in the Logic Analyzer Online Help

5 Troubleshooting the DDR5 Decoder

The following are a few checks and recommended solutions that can help you avoid, diagnose, and resolve problems faced when using the DDR5 Decoder.

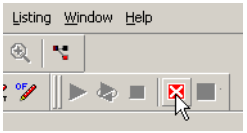
Hardware Related Checks

- The logic analyzer cards should be firmly seated in the logic analysis system frame.
- Logic analyzer pods should be connected to the proper connectors and probes. All cables and probes should be seated properly ensuring that there are no bent pins or poor probe connections.
- The device under test should be "On" and running properly.

Software Related Checks

Ensure that you have loaded the correct configuration file for the probe you are using. Signals are mapped differently, depending on which configuration file is loaded.

Common Problems and Recommended Solutions

Problem	Cause	Recommended Solution
Logic analyzer "hangs up" just after capturing a trace and the following status message is displayed at the bottom of the screen. 	This indicates that the decoder is busy decoding the captured data.	If the "Processing" message doesn't go away after a minute or two, it is possible that the decoder is searching through an enormous number of idle states in between "meaningful" states. In such a situation, you can use the Cancel button to stop the decoder. 
No trace list display	The trigger specification may be incorrect for the data you want to capture, or the trace memory may be only partially filled.	▪ Check your trigger sequence to ensure that it will capture the events of interest. ▪ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.
Logic analyzer won't power up	If logic analyzer power is cycled when the logic analyzer is connected to a device under test that remains powered up, the logic analyzer may not be able to power up. Some logic analyzers are inhibited from powering up when they are connected to a device under test that is already powered up.	Remove power from the device under test, then disconnect all logic analyzer cabling. This will allow the logic analyzer to power up. Reconnect logic analyzer cabling after power up.

Problem	Cause	Recommended Solution
Erratic trace measurements		Do a full reset of the device under test before beginning the measurement. Ensure that your device under test meets the timing requirements of the applicable JEDEC bus standard. See Capacitive loading. If the device under test design has extremely close timing margins, loading from probes may cause incorrect functioning and give erratic trace results. Ensure that you have sufficient cooling for the device under test while the probes are installed.
Capacitive loading	Excessive capacitive loading can degrade signals, resulting in incorrect capture, or system lockup in the microprocessor. All probes add additional capacitive loading, as can custom probe fixtures you design for your application.	Careful layout of your device under test can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz. Remove as many pin protectors, extenders, and adapters as possible.
No decoding or incorrect decoding	This problem may be due to incorrect synchronization, modified configuration, incorrect connections, or a hardware problem in the device under test. A locked status line can cause incorrect or incomplete decoding.	▪ Ensure that each logic analyzer pod is connected to the correct connector. ▪ There is not always a one-to-one correspondence between analyzer pod numbers and connector numbers. Probes must supply address, data, and status information to the analyzer in a predefined order. ▪ Check the activity indicators for status lines locked in a high or low state. ▪ Check that the signals on the device under test are routed to the connector according to the manual for your probe. ▪ Verify that the required input buses have not been modified from their default values. These buses must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. Some analysis probes also require other data labels. ▪ Verify that storage qualification has not excluded storage of all the needed states. ▪ Verify that the sampling positions are correctly configured.

If you still have difficulty using the decoder after trying these suggestions, please contact your Keysight Technologies representative.