Errata

Title & Document Type: 83590A RF Plug-In Operating and Service Manual

Manual Part Number: 83590-90005

Revision Date: February 1982

About this Manual

We've added this manual to the Agilent website in an effort to help you support your product. This manual provides the best information we could find. It may be incomplete or contain dated information, and the scan quality may not be ideal. If we find a better copy in the future, we will add it to the Agilent website.

HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, life sciences, and chemical analysis businesses are now part of Agilent Technologies. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A. We have made no changes to this manual copy.

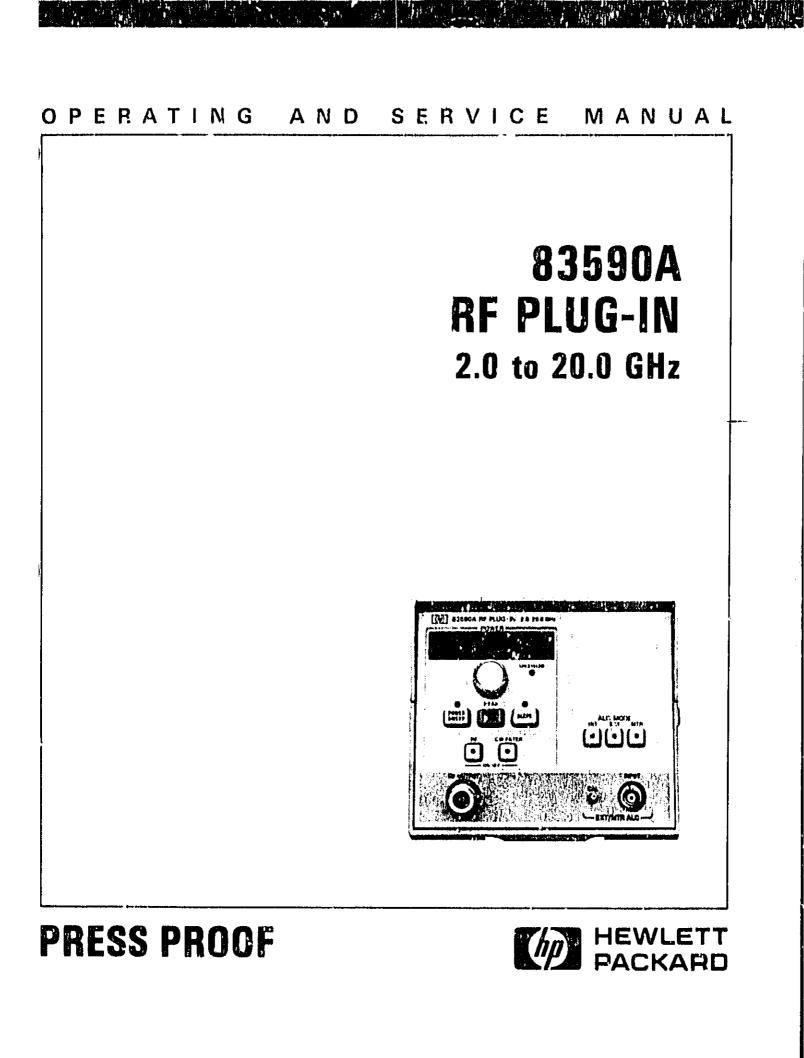
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CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

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For any assistance, contact your nearest llewlett-Packard Sales and Service Office Addresses are provided at the back of this manual.

83590A RF PLUG-IN (Including Options 002, 004, and 005)

SERIAL NUMBERS

This manual applies directly to HP Model 83590A RF Plug-In having serial number prefix 2146A.

With changes described in Section VII this manual also applies to instruments with serial numbers prefixed 2143A.

For additional information about serial numbers, refer to INSTRUMENTS COVERED BY MANUAL in Section I.

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MANUAL PART NO. 83590-90006 Microfiche Part No. 83590-80006

Printed: FEBRUARY 1982



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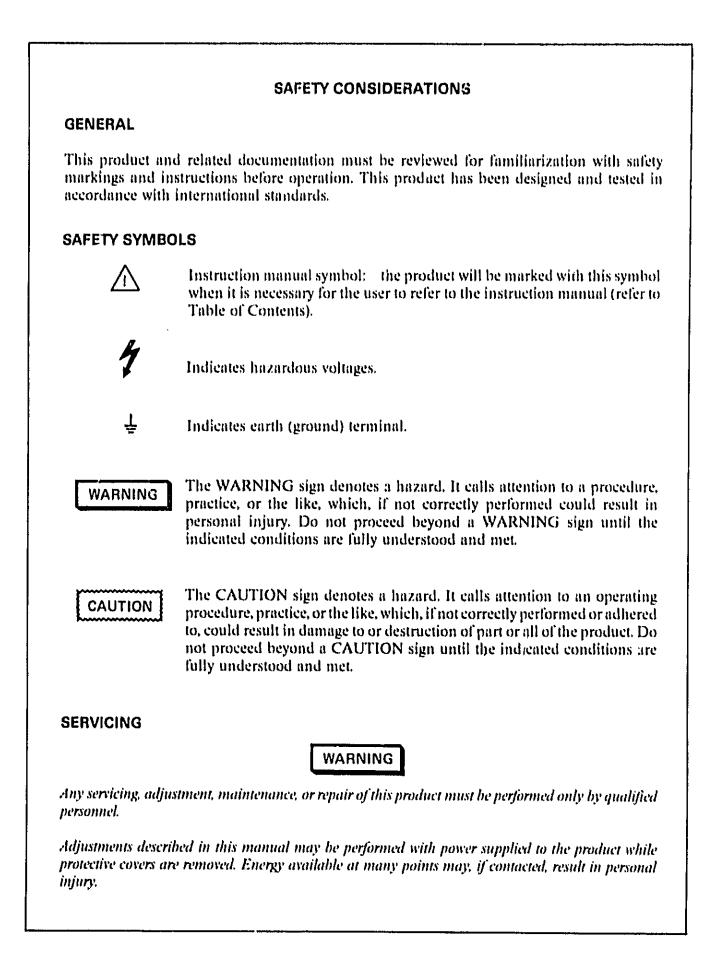
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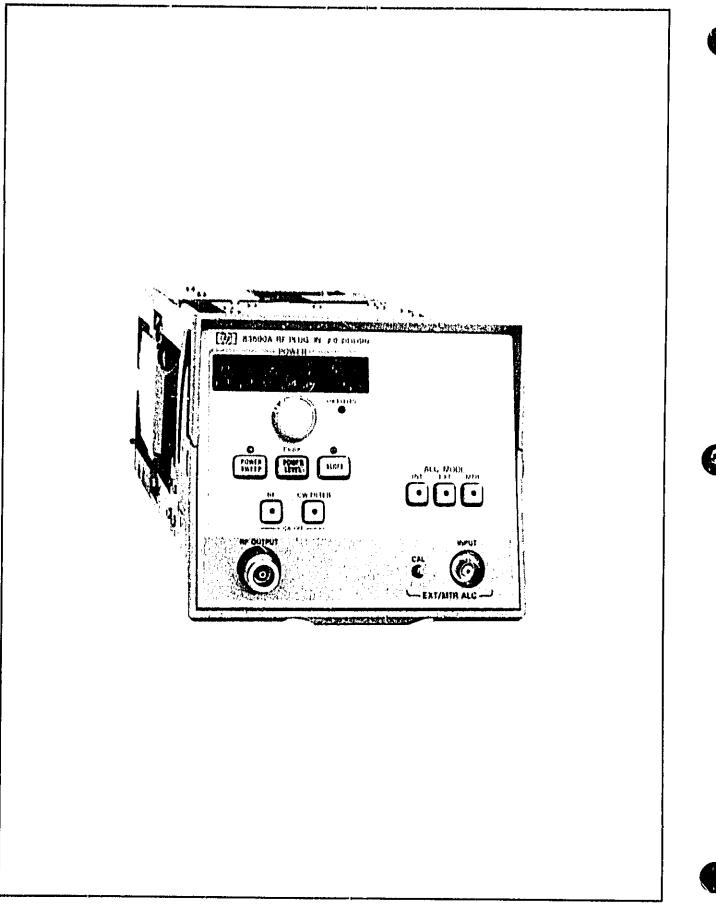
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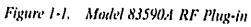
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General Information

Model 83590A





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SECTION I GENERAL INFORMATION

1-1. INTRODUCTION

1-2. This Operating and Service Manual contains information required to install, operate, test, adjust, and service the Hewlett-Packard Model 83590A RF Plug-in, Figure 1-1 shows the Model 83590A,

1-3. This manual is divided into eight major sections which provide the following information:

- a. SECTION I, GENERAL INFORMATION, includes a brief description of the instrument, safety considerations, specifications, supplemental characteristics, instrument identification, options available, accessories available, and a list of recommended test equipment.
- b. SECTION II, INSTALLATION, provides information for initial inspection, preparation for use, storage, and shipment.
- e. SECTION III, OPERATION, explains the frequency resolution characteristics of the RF Plug-in in CW and swept frequency modes. Operating instructions include FM switch parameter settings, and crystal and power meter leveling instructions. A description of front and rear panel features and Plug-in error codes is also given.
- d. SECTION IV, PERFORMANCE TESTS, presents procedures required to verify that performance of the RF Plug-in is in accordance with published specifications.
- e. SECTION V, ADJUSTMENTS, presents procedures required to properly adjust and align the Model 83590A RF Plug-in after repair.
- SECTION VI, REPLACEABLE PARTS, provides information required to order all parts and assemblies.
- g. SECTION VII, MANUAL BACKDATING CHANGES, provides backdating informa-

tion required to make this manual compatible with earlier shipment configurations.

h. SECTION VIII, SERVICE, provides an overall instrument block diagram with troubleshooting and repair procedures. Each assembly within the instrument is covered on a separate Service Sheet which contains a circuit description, schematic diagram, component location diagram, and troubleshooting information to aid in the proper maintenance of the instrument.

1-4. Supplied with this manual is an Operating Information Supplement. This is simply a copy of the first three sections of the manual, which should be kept with the instrument for use by the instrument operator.

1-5. On the front cover of this manual is a "Microfiche" part number. This number may be used to order 10- by 15-centimeter (4- by 6-inch) microfilm transparencies of the manual. Each microfiche contains up to 60 photo duplicates of the manual pages. The microfiche package also includes the latest Manual Changes sheet as well as all pertinent Service Notes.

1-6. Refer any questions regarding this manual, the Manual Changes sheet, or the instrument to the nearest HP Sales/Service Office. Always identify the instrument by model number, complete name, and complete serial number in all correspondence. Refer to the inside rear cover of this manual for a worldwide listing of HP Sales/Service Offices.

1-7. SPECIFICATIONS

1-8. Listed in Table 1-1 are the specifications for the Model 83590A RF Plug-in. These specifications are the performance standards, or limits, against which the instrument may be tested. Table 1-2 lists the RF Flug-in supplemental performance characteristics. Supplemental performance characteristics are not specifications but are typical characteristics included as additional information for the user. **General Information**

Model 83590A

Annuman 19641 Jean			Fraqu	oncy Bands (l	GHz)	
Accurncy (25°C ±5°C)		2,0 to 7,0	7.0 to 1	3,6 13.6	to 20,0	2.0 to 20.0
CW Mode		±5 MHz	±10 MI	lz ±10) MHz	······
All Sweep Modes (Sweep time >100 ms)		±20 MHz	±25 MI	łz ±30) MHz	±50 MH7 ²
Frequency Markers (Sweep time ≥100 ms)		±20 MHz ±,5% of sweep width	±25 MI ±.5% o sweep wi	۲ ±.,) MHz 5% of p width	土50 MHz ² 土.5% of sweep width
Stability						· · · · · · · · · · · · · · · · · · ·
With 10% Line Voltage Cl	nange	土50 kHz	±100 kl	12 土15	0 kHz	±150 kHz
With 10 dB Power Level C	Change	土200 kHz	±400 kl	12 土60	0 kHz	土600 kHz
With 3:1 Lond SWR		±100 kHz	±200 kl	lz. ±30	0 kHz	±300 kHz
With Time (in a 10 minut period after one hour war		<±100 kHz	<±200 k	Hz <±3	00 kHz	<±300 kHz
Residual FM, Peak (10 Hz to 10 kHz Bandwid (CW Mode with CW Filte		<5 kHz	<7 kH	z. <9	kHz	······
		POWER OL	ITPUT		••••••••••••••••••••••••••••••••••••••	
			Frequency I	lands (GHz)		
	2.0 to 7.0	7.0 to 13.5	13.5 to 18,6	13.5 to 20,0	2,0 to 18,	6 2.0 to 20.0
Maximum Levoled Output Power ^{2, 3, 4} (25°C)	+10 dBm	+10 dBm	+10 dBm	+8 dBm	+10 dBn	1 +8 dBm
	+	1	I among the second s			<u> </u>

Table 1-1. Specifications for Model 83590A Installed in Model 8350A (1-of 3)

1-2

With Option 002

Power Level Accuracy¹⁰

With Option 002⁵

(at 0 dB attenuator step)

(Internally Leveled)

+8,5 dBm

<±1.3 dB

<±1.5 dB

37

+8 dBm

<±1.3 dB

<±1.5 dB

+7 dBm

<±1,4 dB

<±1.6 dB

+5 dBm

<±1,4 dB

<±1.6 dB

+7 dBm

<±1.5 dB

<±1.7 JB

+5 dBm

<±1.5 dB

<±1.7 dB

1 3

Model 83590A

		POWER OUT	יטד (Cont'd)			<u></u>			
Minimum Settable Power: - With Option 002; -75 dl				, -						
			-		Atte	inuntor S	Setting (d	B)		
Attenuator Accuracy	rrequency i	langa (GHz) -	10	20	31	0 41	C 60		60	70
(±dB referenced from the 0 dB setting)	2.0 - 12,4		(),6	0.7	0,	9 1.	8 2,0		2.2	2.3
	12.4 -	- 18.0	07	0,9	1.:	2 2,0	0 2.3		2.5	2,8
· · · · · · · · · · · · · · · · · · ·	18.0 -	- 20,0	0.9	1,5	2.:	5 3,0	3.2		3.3	3.5
Power Variation (at specified Maximum Leve	start			Fraqu	ency	Bauds ((3Hx)			le ; , , , , , , , , , , , , , , , , , ,
Power or below)		2.0 to 7.0		7.0; to 13.5		13.6	i to 20		2.0 to 20	
Internally Leveled		±0.7 dB		±0.7 dB ±0		±0	8 dB		±0.9 JB	
Externally Leveled Negative Crystal Detec (Sweep time >100 ms)	tor ⁶	±0,2 dB	e d ^a	±0.2 J	ецэ В 1916) ₁₁ ±0	.2 dB		±0.3	dB
Externally Leveled Power Meter ⁷		±0,2 dB		±0,2 di		±0.2 dB			±0.2 dB	
Residual AM in 100 kHz Ban (in dB below carrier and at specified Maximum Leveled		≥50 dB	:	³ '≥50 dB ≥50 dB		≥50 dB				
Spurious Signals (at specified Maximum Leve	led Powar)			· · · · · · · · · · · · · · · · · · ·			; · } 		:	
Hurmonics (in dB below)	entrier)	>25 dB	1	>25 dB >25 dB		>25 dB				
Non-Harmonics		>50 dB		>50 dB >50 dB		>50 dB				
Oútput SWA (Internally Le	veled)	<1.9		<1.9		<	<1.9		<1,9	
With Option 002		<2.1		<2,1) <	2.1		<2.	1
Power Sweep ⁹		1.	Fr	equency (lands	(GHz)				
Power Sweep?	2.0 to 7.0	7.0 to 13,5	13.	5 to 18,6	13,5	to 20.0	.U1 to 11	8.6	2.0	to 20
Calibrated Range: ⁹	>15 dB	>15 dB	>	•15 dB	>1	3 dB	>15 di	3	>1	3 dB
With Option 002:	>13.5 dB	>13 dB	>	12 dB	<	0 dB	>12 dI	3	>1() dB

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AN CARD

Table 1-1. Specifications for Model 83590A Installed in Model 8350A (2 of 3)

1-3

General Information

Model 83590A

	MODUL/TION !	
External AM	9 - 9 - 9 - 9 - 9 - 9 - 9 - 9 - 9 - 9 -	
Maximum Input: 15V		,
Internal AM		
Selectable (by internal jumper in modulation allows operation wi	n 8350A) to 1 kHz or 27.8 kHz square th HP 8755A/B/C Swept Amplitude A	wave modulation . The 27.8 kHz nalyzer.
On/Off Ratio: ≥30 dB below a	pecified Maximum Leveled Power.	
Symmetry: 40/60		
External FM	= = -==== 1,	
Maximum Deviations for Modu	lation Frequencies:	
Modulation Frequency	Cross-Ovar Couplari	Direct Coupled
DC to 100 Hz		±12 MHz
100 Hz to 1 MHz	±7 MHz	±7 MHz
1 MHz to 2 MHz	±5 MHz	±5 MH2
2 MHz to 10 MHz	±1 MHz	
		±1 MHz
:	GENERAL SPECIFICATIONS	:
Minimum Sweep Time (over full b	•	1
Minimum Sweep Time (over single	•	
	d switch points at approximately 7.0 c	GHz, and 13.5 GHz
RF Output Connector. Type N F	emale	
1		
¹ Unless otherwise noted, all speci	fications are at the RF OUTPUY connector	er and at 0° to 55°C.
2 For temperatures greater than 25	C, maximum leveled output power typica	lly degrades .1 dB/°C.
³ Wher, RF Output is peaked with	PEAK control.	
4 0.5 dB lower for Option 004,	1	
⁵ Attenuator switch points are ever	y 10 dB starting at -5 dBm indicated pow	'er.
6 Excludes coupler and detector va specified maximum leveled power	riation. Crystal detector output should be r.	between -10 mV and -200 mV at
7 Use HP Model 432A/B/C Power	Meter. Sweep time typically ≥5 seconds/G	Hz but not ≤10 seconds.
⁸ Power Swaep and Slope Compen	sation total must not exceed the specified	Power Sweep calibrated range.
9 With Option 002, in power sween a	or slope functions, power can exceed the atte ceds 10 dB (i.e., if the calibrated range is 12 d	minimentan bu the encount that the

Table 1-1. Specifications for Model 83590A Installed in Model 8350A (3 of 3)

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Valuue in this table are not specific	NOTE ations, but are typic	al characteristics in	icluided for user info	ormation,
F	REQUENCY CHARAC	TERIS/ICS		
		Fraquancy I	Bonds (GHz)	
Acouracy (25°C ±5°C)	2.0 to 7.0	7,0 to 13,5	13.5 to 20.0	2.0 to 20.0
CW Mode Typically	±2 MHz	±3 MHz	±4 MHz	
Manual Sweep	≾30 MHz	≤30 MHz	≤30 MHz	≤100 MH7
All Sweep Modes (Sweep time 10 ms to 100 ms)	≤±6 MHz	≤:±8 MHz	≤±10 MH2	≤±35 MH7
Sweep Mode Linearity ²	≤:±2 MHz	≤±4 MHz	≤±6 MHz	≤±10 MH)
Stability with Temporature	±200 kHz/°C	±400 k11//°C	±600 kHz/°C	±:600 kHz/°0
0	UTPUT CHARACT	ERISTICS I		J,,,,,,,
Stability with Temperature (at specif Power Variation (at specified Maximum Externally leveled with Negative Cry	Leveled Power o	r below)	9.1 dB/°C	
Spurious Signals	·		lands (GHz)	.
(in 4D below carrier and at specified Maximum Leveled Power)	2.0 to 7.0	7.0 to 13,5	13.5 to 20.0	2.0 to 20.0
Harmonics and Subharmonics	>40 JB	>35 dB	>35 dB	>35 dB
Non Harmonies Typically	>55 dB	>55 년8	>55 dB	>55 dB
Power Sweep 3 Accuracy (Including Linearity): Ty Resolution (Displayed): 0.1 dB	nically ±1.5 dB		L	L
Slope Compensation 3				

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Table 1-2. Supplemental Performance Characteristics for Model 83590A Installed in Model 8350A (1 of 2)

Table 1-2. Supplemental Performance Characteristics for Model 83590A Installed in Model 8350A (2 of 2)

	MODULATION CHARACTERISTICS
External AM	
Frequency Response: Typicall	ly 100 kHz
Input Impedance: Approxima	rely 10k Ohm
Range of Amplitude Control:	Typically 15 dB
Sensitivity: Typically I dB/V	
Pulse in	
TTL Compatible: Logic high •	= RF on, Logic low = RF off
7.0 to 20.0 GHz: Squarewave r	-
2.0 to 7.0 GHz;	
Rise/Fall Time: Typically 10	0 ns
Minimum Pulse Width:	
Leveled: Typically 1 μs	ŝ
Unleveled Power level so	et to +20 dBm: Typically 100 ns
External FM	
Frequency Response (DC to 2 N	MHz): Typically ±3 dB
Sensitivity (Switch selectable)	
Typically -20 MHz/V (FM N	Aode)
Typically -6 MHz/V (Phase-	
Imput Impedance: 2000 On	ms nominal
	GENERAL CHARACTERISTICS I
Frequency Reference Output: 1 V/	GHz ±25 mV (2 to 18 GHz) rear panel BNC output.
	7 GHz fundamental oscillator output, nominally 1 dBm.
Woight: Net 6.0 kg (13.2 lb.); Sl	hipping 9.2 kg (20 lb.)
	eristics are at the RF OUTPUT connector and at 0° to 55°C.
2 With respect to the SWEEP OUT vi 3 Power Sweep and Slope Compensat	ottage, tion must not exceed the specified Power Sweep calibrated range,
	ir slope functions, power can exceed altenuator step by the amount that the

4 With Option 002 in nower sweep or slope functions, power can exceed attenuator step by the amount that the Power Sweep calibrated range exceeds 10 dB (i.e., if the calibrated range is 12 dB, power can exceed the attenuator step by 2 dB).

5 Excludes coupler and detector variation. Crystal detector output should be between -10 mV and -200 mV at specified maximum leveled power.

1-9. SAFETY CONSIDERATIONS

1-10. This product has been manufactured and tested in accordance with international safety standards. Before operation, this product and related documentation must be reviewed for familiarization with safety markings and instructions. A complete listing of Safety Considerations precedes Section 1 of this manual.

1-11. INSTRUMENTS COVERED BY MANUAL

1-12. Attached to the rear panel of the instrument is a serial number plate. A typical serial number plate is shown in Figure 1-2. The serial number is in two parts. The first four digits followed by a letter comprise the serial number prefix. The last five digits form the sequential suffix that is unique to each instrument. The content of this manual applies directly to instruments having the same serial number prefix as those listed on the title page of this manual under SERIAL NUMBER.

1-13. An instrument manufactured after the printing of this manual may have a serial prefix that is not listed on the title page. An unlisted serial prefix indicates that the instrument is different from those documented in this manual. The manual for the instrument is then supplied with a Manual Changes supplement that contains information which documents the differences.

1-14. In addition to change information, the Manual Changes supplement contains information for correcting errors in the manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is keyed to the manual's print date and part number, both of which appear on the title page. Complimentary, copies of the Manual Changes supplement rare available on request from Hewlett-Packard.

1-15. For information concerning a serial number prefix that is not listed on the title page or in the Manual Changes Supplement, contact your nearest Hewlett-Packard Sales/Service Office.

1-16. DESCRIPTION

1-17. The Model 83590A is an RFPlug-in which has been designed for use with the Model 8350A

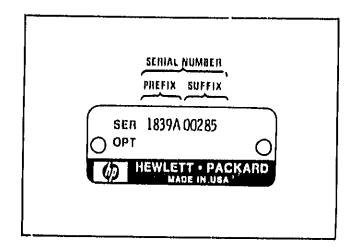


Figure 1-2, Typical Serial Number Plate

Sweep Oscillator. The Model 83590A covers the frequency range of 2 to 20.0 GHz in three bands. A YIG oscillator is used as the tunable RF frequency source of all bands. The YIG oscillator fundamental frequency is used for Band 1 (2.0 to 7.0 GHz). A YIG Tuned Multiplier (YTM) is used to multiply the YIG oscillator frequency for Bands 2 and 3 (6.9 to 13.5 GHz and 13.4 to 20.0 GHz).

1-18. Mot el 83590A front par el functional controls, pushbuttons, and the Rotary Pulse Generator (RPG), are monitored by the Model 8350A via the RF Plug-in interface circuits. The Mouet 8350A generates a tuning voltage according to the mode of operation (CW, START/STOP, CF/ Δ F). This signal is scaled and offset by the Plug-in to provide a voltage ramp (in swept modes) proportional to the YIG oscillator frequency. The Model 83590A tuning circuits accept the tuning ramp output from the Model 8350A and convert it to a current which drives the YIG oscillator tuning coil.

1-19. The standard Model 83590A offers internally leveled RF output power. Internal (INT), External (EXT), and Power Meter (MTR) leveling are available as selected by the front panel pushbuttons. A front panel EXT/MTR ALC input connector and gain control (CAL) are provided to use with an external leveling loop. A front panel LED indicates when the RF output becomes unleveled. The RF output level is controlled by the Model 83590A RPG, the Model 8350A data entry controls (keypad and step keys), or through HP-IB control via the Model 8350A.

1-20. A power sweep function allows the RF output power to be swept at least 10 dB during CW mode or swept frequency modes. Power sweep is

selected by the front panel POWER SWEEP pushbutton. Slope compensation control is also available by selecting the SLOPE pushbutton and rotating the Model 83590A RPG or manipulating the Model 8350A data entry controls. The power sweep function and slope compensation may both be selected and modified through HP-IB control $v^{i_{\rm H}}$ the Model 8350A.

1-21. The RF output may be internally or externally amplitude modulated, or externally frequency modulated. Internal square wave modulation frequency is selectable by a Model 8350A internal jumper to be either 1 kHz or 27.8 kHz (for use with the Model 8755 Swept Amplitude Analyzer). Rear panel BNC connectors accept an external AM or FM frequency. FM coupling (direct coupled or cross-over) and sensitivity is selected by an internal configuration switch in the Model 83590A. Refer to Section III, Operation, of this manual for detailed information on the configuration switch.

1-22. A rear panel 1V/GHz signal corresponds to the RF output frequency. This output voltage may by used as a reference for pretuning external equipment in phase locking applications. (The Model 8410B/8411A Network Analyzer utilizes this output in such a configuration.)

1-23. The RF output may be turned off by the RF ON/OFF pushbutton. RF power ON is indicated by the LED in the center of the pushbutton. Additionally, in CW mode, the CW FILTER, when selected, places a capacitor across the YIG oscillator tuning coil to filter high frequency noise which would appear at the RF output. All front panel functions, with the exception of the EXT/MTR ALC CAL adjustments, may be set or altered by computer control via the HP-IB bus connection on the Model 8350A.

1-24. OPTIONS

1-25. Option 002, 70 dB Attenuator

1-26. Option 002 instruments contain a digitally controlled attenuator just before the RF output. Up to 70 dB of attenuation in 10 dB steps is automatically selected as required to attenuate the RF output power to the indicated level. The continuously variable power level function operates as in a standard instrument with the data entry controls.

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1-27. Option 004, Rear Panel RF Output

1-28. Option 004 instruments have the Type N RF output connector and the BNC EXT/MTR ALC input connector on the rear panel instead of the front panel.

1-29. Option 005, APC-7 [®]• RF Output Connector

1-30. Option 005 instruments have an APC-7 RF output connector.

1-31. EQUIPMENT REQUIRED BUT NOT SUPPLIED

1-32. To have a complete operating sweep oscillator unit, the Model 83590A RF Plug-in must be installed in a Model 8350A Sweep Oscillator. Refer to Section II, Installation, in this manual for a detailed description of RF Plug-in installation.

1-33, EQUIPMENT AVAILABLE

1-34. Service Accessories

1-35. A Service Accessory Kit (HP Part Number 08350-60020) is available for servicing the Model 83590A RF Plug-in and the Model 8350A Sweep Oscillator. HP Part Numbers for the individual pieces of the kit are provided in Table 1-3. The accessory kit includes:

- Two 44-pin printed circuit board extenders. These boards have keyed slots which allow them to be used in each of the keyed pe board receptacles in the Model 83590A, and in the Model 8350A as well.
- An RF Plug-in extender cable set that provides all electrical connections when the RF Plug-in is removed from the Sweep Oscillator. The RF Plug-in Interface connector (P2) and the Power Supply Interface connector (P1) are extended by separate cables.
- One Hex Balldriver for use in Model 8350A front panel repairs.
- One 16-pin and one 20-pin I.C. Test Clip for probing integrated circuits.

1-36. A listing of service accessories available including service cables, wrenches, adapters, and extender boards is given in Table 1-3.

*APC-7 $^{\circ}$ is a registered trademark of the Bunker-Ramo Corporation.

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1-37. Model 8410B/8411A Network Analyzer

1-38. The Model 8350A Sweep Oscillator, with the Model 83590A RF Plug-in installed, is compatible with the HP Model 8410B Network Analyzer system. The combination of the Model 8410B Network Analyzer, the Model 8411A Frequency Converter, and an appropriate display Plug-in forms a phasemeter and a ratiometer for direct phase and amplitude ratio measurement on RF voltages. These measurements can be made on single frequencies and on swept frequencies from 2 to 18 GHz. The Model \$350A/83590A combination is capable of operation over this full frequency range. The Model 8410B has an Auto-Frequency range mode which gives it the capability of automatically tracking the Model 8350A Sweep Oscillator over octave and multi-octave frequency bands. Two interconnections to the Model 8350A are necessary to ensure that the Model 8410B will phase lock properly. The Model 8410B Source Control Cable (HP 08410-60146) connects the Model 8410B rear panel SOURCE CONTROL connector to the Model 8350A rear panel PROGRAMMING CONNECTOR, Additionally, the Model 83590A RF Plug-in rear panel 1V/GHz output connects to the Model 8410B rear panel FREQ REF INPUT. The Model 8410B Source Control Cable connector pins and signals are illustrated in the Model 8350A Sweep Oscillator Operating and Service Manual.

1-39. Model 8755 Frequency Response Test Set

1-40. The Model 8350A Sweep Oscillator with the Model 83590A RF Plug-in installed is compatible with the Model 8755 Frequency Response Test Set for broadband swept scalar

measurements. The Model 8350A provides internal 27.8 kHz square wave amplitude modulation of the RF output, eliminating unnecessary cable connections to the Model 8755 or the use of an external modulator. The Model 8350A can also produce alternate sweeps through use of the ALT n function which works in conjunction with the channel switching circuits in the Model 8755C. This permits Channel 1 on the Model 8755C to respond only to the Model 8350A current state and Channel 2 to the alternate state, A single cable (HP Part Number 8120-3174) connects between the Model 8350A rear panel ALT SWP INTERFACE connector and the Model 8755C front panel ALT SWP INTERFACE connector.

1-41. Power Meters and Crystal Detectors

1-42. The RF output can be externally leveled using the HP Model 432 Power Meter or negative polarity output crystal detectors. Refer to Section III Operation of this manual for detailed information on leveling techniques that may be used with the Model 8350A/RF Plug-in combination.

NOTE

The Model 435A and 436A Power Meters should not be used in Model 8350A/Model 83590A externel leveling systems.

1-43. RECOMMENDED TEST EQUIPMENT

1-44. Equipment required for testing and adjusting the instrument is listed in Table 1-4. Other equipment may be substituted if it meets or exceeds the critical specifications indicated in the table.

Nome	HP Part Number	Description
44-pin printed circuit hourd extender	08350-60031*	Extends printed circuit boards
RF Plug-in Extender Cables	08350-60034* 08350-60035*	Extends RF Plug-in Interface connector (P2) Extends RF Plug-in Power Supply Interface connector (P1
Adjustment Tool	8830-0024	Fits miniature adjustment slot on potentiometers
Wrenches	08555-20097 8710-0946	5/16"slotted box/open end 15/64" open end
Service Cables	8120-1578 83525-60019	18" Coax with SMA (m) connector on each end 10" coax with SMB snap on (f) and SMA (m)
Adapters	1250-07777 1250-0082 1250-1404 1250-1158 1250-0674 1250-0675 1250-069	Type N (f) to BNC (m) Type N (m) to BNC (m) Type N (l) to SMA (f) SMA (l) to SMA (l) SMA (l) to SMB (m) SMA (l) to SMC (m) SMB snap on (m) to SMB snap on (m)
Hex Balldriver	8710-0523*	Removes front panel hold down plate hex screws in \$350A
IC Test Clip	400-0979+ 400-0979+	16-pin IC test clip 20-pin IC test clip

Table 1-3. Service Accessories Available

Instrument	Critical Specifications	Recommended Model	Use*
Sweep Oscillator	No substitute	UP 8350A	Р,А,Т
Digital Voltmeter (DVM)	Range:50V to +50V Accuracy: ±0,01% Input Impedance: >10M Ohms	HP 3456A	A,T
Oscilloscope	Dual Channel Bandwidth: de to 100 MHz Vertical Sensitivity: <5 mV/DIV Horizontal Sweep Rate: <0.1µ S/DIV External Sweep Capability	HP 1740A	Р,А,Т
Oscilloscope Probe	1:1 General Purpose Probe	HP 10009B	٨
Frequency Counter	Frequency Range: 2 to 20.0 GHz Input Impedance: 50 Ohms Resolution: <1 MHz	HP 5343A	Р,А
Spectrum Analyzer	Frequency Range: 2 to 20.0 GHz Residual FM: <100 Hz	11P 8565A or 11P 8566A	Р,Т

Table 1-4. Recommended Test Equipment (1 of 3)

Instrument	Critical Specifications	Recommended Model	Use*
Swept Amplitude Analyzer	Capable of Transmission Measurements Power Resolution: <0.25 dB	HP 8755C	^
Display Mainframe	Compatible with 8755C Swept Amplitude Analyzer	HP 180T/TR, 182T/TR	٨
Detectors (2)	Compatible with Swept Amplitude Analyzer Frequency Range: 2 to 20,0 GHz Power Range: -20 to +10 dBm	HP 11664B	^
Frequency Meter	Frequency Accuracy: <0,17% Calibration Increments: <2 MHz Frequency Range: 2,0 to 4,0 GHz 4.0 to 12,4 GHz 12,4 to 18 GHz	HP 536A HP 537A HP P532A	л л л
Function Generator	Frequency Range: 0.1 Hz to 10 MHz Sinewave and squarewave output Output Level: 10Vp-p into 50 Ohms Output Level Flatness: <13% from 10 Hz to 100 kHz <10% from 100 kHz to 10 MHz	HP 3312A	P,A,T
Power Meter	Power Range: 20 to +10 dBm (No substitute when used for external power meter leveling).	HP 432A	Р,А
Thermistor Sensor	Frequency Range: 2 to 20.0 GHz Maximum SWR: <1.75	HP 8478B	Р.А
Thermistor Sensor	Frequency Range 18 to 20,0 GHz Maximum SWR: <2,0	HP K486	P,A
Adaptor	Waveguide to APC 3.5 (f) (for use with HP K486)	HP K281C	۸
Power Meter	Power Range: 1 µ W to 100 mW	HP 436A	Р,А
Power Sensor	Frequency Range 2 to 20,0 GHz	HP 8485A	Р,А
Crystal Detector**	Frequency Response: 2 to 20,0 GHz Maximum Input Power: 100 mW	HP 8473C	P,A
Attenuator**	Frequency Range: 2 to 20,0 GHz Maximum Input Power: +20 dBm Attenuation: 20 dB ±1.0 dB 20 dB ±0.8 dB 6 dB ±0.6 dB	Weinschel Model M9-20 Weinschel Model M9-10 Weinschel Model M9-6	Р Р,А Р

.

Table 1-4. Recommended Test Equipment (2 of 3)

Instrument	Critical Specifications	Recommended Model	Use*
Power Splitter**	Frequency Range: 2 to 20,0 GHz Maximum Input Power: ≥+20 dBm	Weinschel Model 1579A	Р,А
Directional Coupler	Frequency Range: 2.0 to 18 GHz Nominal Coupling: >22 dB Maximum Coupling Variation: ± 1 dB Minimum Directivity: 26 dB	HP 11691D	р
RMS Volumeter	dB Range: - 20 to70 dBm (0 dBm = 1 mV into 600 ohms) Frequency Range: 10 Hz to 10 MHz Accuracy: ±5% of full scale	dBm ≈ 1 mV into 600 ohms) equency Range: 10 Hz to 10 MHz	
Air Line Extension (2 required)	Impedance: 50 Ohms Frequency Range: de to 18 GHz Reflection Coefficient: 0,018 to 0,001 (times the frequency in GHz)	ent: 0,018 to 0.001	
Step Attenuator	Frequency Range: de to 18 GHz Incremental Attenuation: 0 to 70 dB in 10 dB steps Calibration Accuracy: <10.1 dB at all steps	HP 8495B Option 890	р
Adjustable Short	Frequency Range: 2 to 18 GHz Impedance: 50 ±1.5 Ohms	Maury Microwave 1953-2	p
DC Power Supply	DC Output: 0 to 6.5Vde ±0.05 Vde	HP 6214A	٨
50 Ohm Termination	Type N, 50 ±0.5 Ohms	HP 909A	р
Delay Line Discriminator	Refer to Figure 1-3,		Р, А
PC Board Extender	44-pin, extends printed circuit boards	HP Part No, 08350-60031	A, T

Table 1-4. Recommended Test Equipment (3 of 3)

ton rearing at trequencies of who this, the following

ATTENUATORS 20 dB HP 8419B Option 020 10 dB HP 8419B Option 010 6 dB HP 8491B Option 006 3 dB HP 8491B Option 003

POWER SPLITTER HP 11667A

CRYSTAL DETECTOR UP 8470B

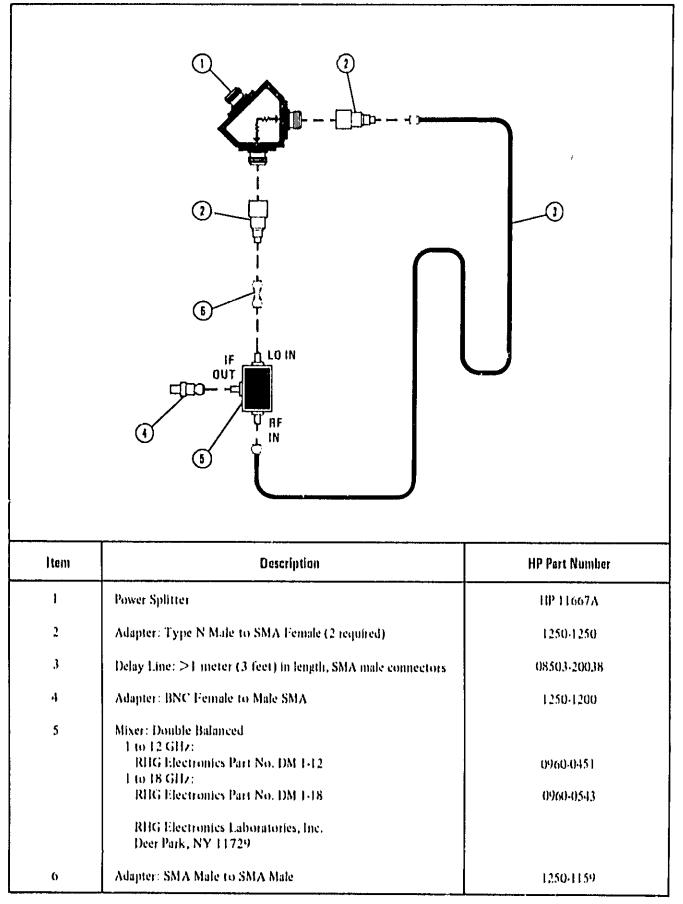


Figure 1-3. Delay Line Discriminator

1-13/1-14



SECTION II

2-1. INTRODUCTION

2-2. This section provides installation instructions for the Model 83590A RF Plug-in. This section also includes information about initial inspection, damage claims, preparation for use, packaging, storage, and shipment.

2-3. INITIAL INSPECTION

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. The contents of the shipment should be as shown in Figure 1-1, Procedures for checking electrical performance are given in Section IV, Performance Tests, of this Operating and Service Manual. If the instrument combination does not pass the electrical Performance Tests, refer to Section V, Adjustments, of this manual. If, after the adjustments have been made, the instrument combination still fails to meet specifications, and a circuit malfunction is suspected, refer to troubleshooting procedures in Section VIII, Service, in this manual, If the instrument does not pass the above electrical tests, if the shipment contents are incomplete, or if there is mechanical damage or defect, notify the nearest Hewlett-Packard office. If the shipping container is damaged, or if the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement without waiting for claim settlement.

2-5. PREPARATION FOR USE

2-6. Power Requirements

2-7. When the Model 83590A RF Plug-in is properly installed, it obtains all power through the rear panel interface connector from the Model 8350A Sweep Oscillator.

2-8. RF Plug-in Configuration Switch

2-9. The Model 83590A RF Plug-in has a configuration switch (A3S1) located on the A3

Digital Interface Board. This switch must be preset prior to RF Plug-in operation in the Model 8350A. The configuration switch is an 8-section multiple switch. Each separate switch corresponds to a separate RF plug-in function such as FM sensitivity selection, FM input coupling selection (direct coupled or cross-over), RF power level at power on (maximum or off), and Option 002 Step Attenuator operation. Refer to Section III, Operation, in this manual for a complete description of the configuration switch and instructions on how to set the switches.

2-10. Interconnections

2-i1. There are two rear panel interconnections from the Model 83590A RF Plug-in to the Model 8350A Sweep Oscillator. These are the RF Plug-in Interface connector (P2) and the Power Supply Interface Connector (P1). A complete listing of pins and associated signals for these connectors is provided in Figures 2-1 and 2-2.

2-12. Mating Connectors

2-13. All of the externally mounted connectors on the Model 83590A are listed in Table 2-1. Opposite each connector is an industry identification, the HP part number of a mating connector, and the part number of an alternate source for the mating connector. For HP part numbers of the externally mounted connectors themselves, refer to Section VI, Replaceable Parts, of this manual.

2-14. Operating Environment

2-15. Temperature. The instrument may be operated in temperatures from 0°C to +55°C.

2-16. Humidity. The instrument may be operated in environments with humidity from 5% to 80% relative at +25°C to +40°C. However, the instrument should also be protected from temperature extremes which cause condensation within the instrument.

2-17. Altitude. The instrument may be operated at altitudes up to 4572 meters (15,000 feet).

63580A	Connector	Mating Connector		
Connector Name	Industry Identification	HP Part No.	Alternate Source	
J1 RF INPUT	Type N (f)	1250-0882	Specialty Connector 25-P1 17-2	
J2 EXT/MTR ALC INPUT	BNC (1)	1250-0256	Specialty Connector 25-P118-1	
J3 AUX OUTPUT	Type N (f)	1250-0882	Specialty Connector 25-P117-2	
J4 PULSE IN	BNC (1)	1250-0256	Specialty Connector 25-P1 18-1	
J5 1V/GHz	BNC (I)	1250-0256	Specialty Connector 25-P1 18-1	

Table 2-1. Model 83590A Mating Connectors

2-18. Cooling. When the Model 83590A RF Plug-in is properly installed in the Model 8350A Sweep Oscillator, it obtains all of its cooling airflow by forced ventilation from the fan in the Model 8350A. A diagram showing the various cooling airflow paths within the sweep oscillator is given in Section II. Ir stallation, of the Model 8350A Sweep Oscillator Operating and Service Manual. Ensure that all airflow passages in the Model 8350A and the Model 83590A are clear before installing the RF Plug-in in the Sweep Oscillator.

2-19. Instaliation instructions

2-20. To operate as a completely functional Sweep Oscillator, the Model 83590A RF Plug-in must be installed in a Model 8350A Sweep Oscillator. To install the Model 83590A RF Plug-in in the Model 8350A Sweep Oscillator:

- a. Set the Model 8350A mainframe LINE switch to OFF.
- Remove all connectors and accessories from the front and rear panel connectors of the Model 83590A to prevent them from being damaged.
- c. Position the RF Plug-in unit latching handle in the fully raised position. The latching handle should spring easily into the raised position and be held by spring tension.

- d. Ensure that the Model 8350A RF Plug-in channel is clear, align the RF Plug-in in the channel and slide it carefully into place toward the rear of the channel. It should slide easily without binding.
- e. The drawer latch handle slot will engage with the locking pin just before the RF Plugin is fully seated in position.
- f. Press the latch handle downward,while still pushing in on the RF Plug-in, until the drawer latch is fully closed and the front panel of the RF Plug-in is aligned with the Sweep Oscillator front panel.

2-21. STORAGE AND SHIPMENT

2-22. Environment

2-23. The instrument may be stored or shipped in environments within the following limits;

Temperature..... -40°C to +75°C Humidity..... 5% to 95% relative at 0° to +40°C Altitude Up to 15240 meters (approximately 50,000 feet)

2-24. The instrument should also be protected from temperature extremes which may cause condensation in the instrument.

2-2

2-25. Packaging

2-26. Original Packaging. Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. A complete diagram and listing of packaging materials dredfor the Model 83590A is shown in Figure 2-3. If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number (located on rear panel serial plate). Mark the container FRAGILE to assure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

2-27. Othor Packaging. The following general instructions should be used for repackaging with commercially available packaging materials:

a. Wrap the instrument in heavy paper or plastic. If shipping to a Hewlett-Packard Office or Service Center, attach a tag indicating the type of service required, return address, model number, and full serial number.

- b. Use a strong shipping container.
- c. Use enough shock-absorbing material around all sides of the instrument to provide a firm cushion and to prevent movement inside the container. Protect the control panel with cardboard.
- d. Seal the shipping container securely.
- e. Mark the shipping container FRAGILE to assure careful handling.
- f. In any correspondence, refer to the instrument by model number and full serial number.

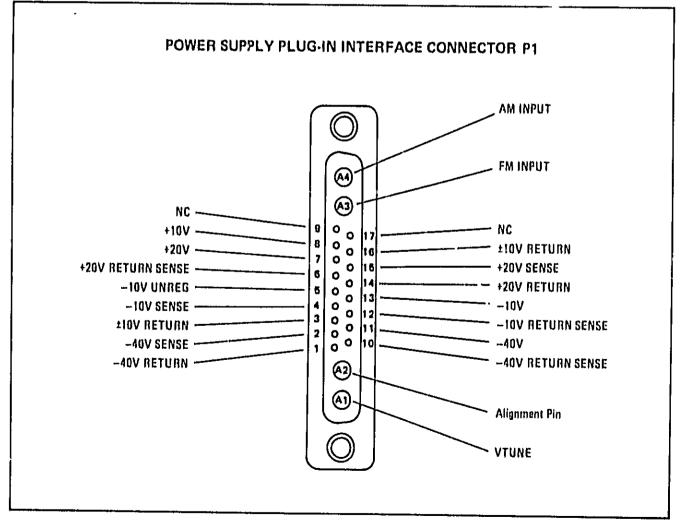
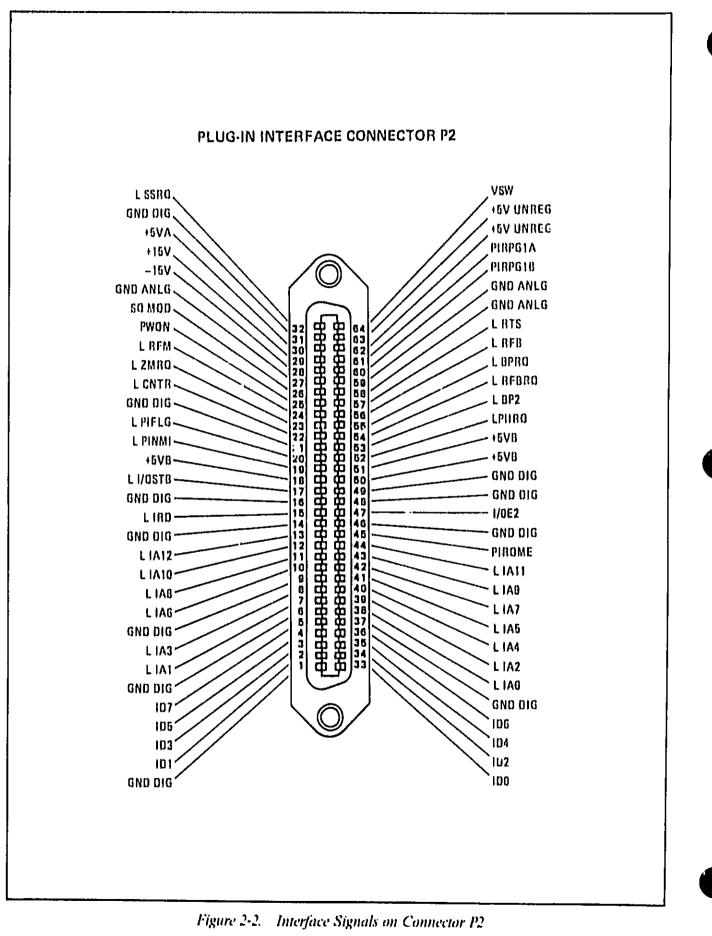


Figure 2-1. Interface Signals on Connector PI

Installation



2-4

Installation

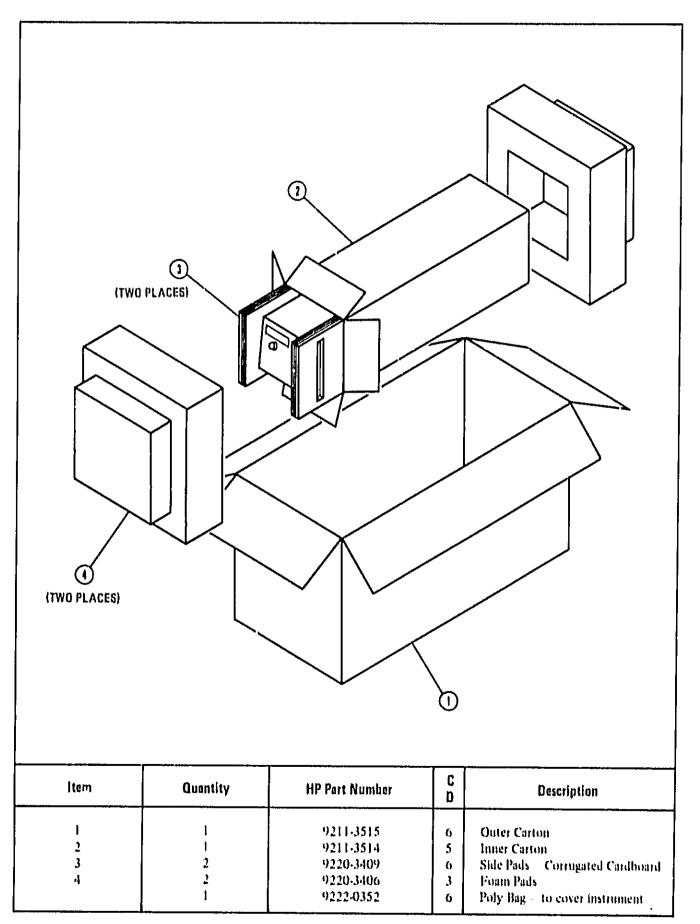


Figure 2-3. Packaging for Shipment Using Factory Packaging Materials

OPERATION

and the second second

Model 83590A

Operation

SECTION III OPERATION

3-1. INTRODUCTION

3-2. This section is divided into four major sections. Operating Characteristics explains the bandswitching and frequency resolution characteristics in CW and swept modes. Front and rear panel Panel Features are shown with illustrated descriptions. Operating Instructions provide a front panel frequency calibration procedure, configuration switch setting instructions, and crystal detector and pewer meter leveling instructions. Operator's Maintenance includes information on the Plug-in error codes, fuses, and service tags.

3-3. OPERATING CHARACTERISTICS

3-4 Bandswitching and Resolution

3-5. The following paragraphs describe the bandswitching and frequency resolution characteristics of the 83590A RF Plug-in.

3-6. The 83590A 2 to 20 GHz RF output is provided in three bands. When sweeping a range of frequencies larger than a single band, the switching between these bands is done automatically. Careful selection of sweep frequencies may avoid problems associated with bandswitching such as harmonics, sweep time, stability, or switching discontinuities. Figure 3-1 illustrates the bandswitching points in the sequential and single band sweep modes.

3-7. Two areas relating to frequency resolution must be considered: these are input resolution and displayed resolution. Input resolution refers to the number of bits (8 bits = 256 points) in the digital to analog converter (DAC) used to generate the tuning voltage for a particular mode of operation. Table 3-1 cross-references input resolution with each DAC used. Displayed frequency resolution refers to the number of digits shown on the 8350A FREQUENCY displays.

3-8. Figure 3-2 is a simplified block diagram of the frequency tuning circuits. The net tuning voltage results from the summation of the three DAC outputs. With this DAC configuration the START/STOP sweep mode is computed by the microprocessor into a center frequency and a ΔF sweep width. Therefore the operation of all sweeps are set with a center frequency and sweep width. The center frequency is specified by the center frequency (CF) DAC and the Vernier DAC, and the sweep width is determined by the ΔF DAC.

3-9. The CF DAC has 12 bits, hence 4096 points across any of the Plug-in frequency bands (including overrange). The analog output ranges from zero to ten volts, which is used to coarsely specify the center frequency output of the Plug-in. These parameters give the CF DAC a resolution of 0.024% (2.5mV) over the full band (including overrange).

3-10. Resolution of Center Frequency is enhanced by a summed voltage generated by an 8-bit (256 pcints) Vernier DAC. Vernier range is set to $\pm 0.05\%$ of bandwidth (including overrange). In multiband Plug-ins, total range of the vernier will vary with each band sweep. Vernier resolution is determined by dividing $\pm 0.05\%$ bandwidth by 256 points (128 points either side of CF). The voltage range of the total 256 points on the Vernier DAC is equal to four points on the 12-bit CF DAC (two points on either side of CF). This increases CF resolution from 0.024%(2.5mV) to 0.00038% (.04mV), and improves the relative accuted of the CF by a similar factor.

NOTE

When the vamier is adjusted through its zeropoint, the CF DAC is incromented or decremented by the total value of the vernier (2 points on the CF DAC). At this time the accuracy of the Center Frequency is again entirely dependent on the CF DAC, 0.005% of bandwidth.

3-11. The ΔF DAC has 10 bits (1024 points). The analog output from this DAC ranges from -5 to +5 volts to produce an even sweep on either side of the center frequency. The Δ resolution improves with narrower sweep widths. For broad

Operation

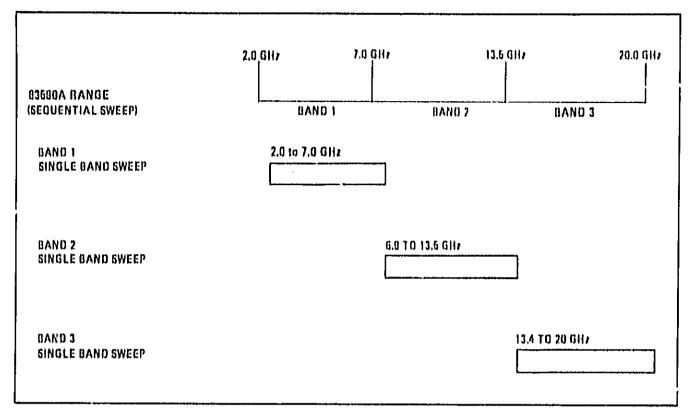


Figure 3-1. Bandswitching in Sequential and Single Band Sweep Modes

sweeps, the resolution is 0.1% of the full band. Greater resolution is provided for sweep widths less than 1/8 of the full band range. At these sweep widths, the resolution is improved to 0.012% of the full band.

3-12. Center Frequency is always displayed with 1 MHz resolution. Likewise, Vernier values are always displayed at 10 kHz resolution. Display resolutions for ΔF values vary with sweep width. Figure 3-3, illustrates the ΔF mode displayed resolution values versus displayed ΔF frequency sweep widths.

3-13. PANEL FEATURES

3-14. Front and rear panel features are described in Figure 3-4 and 3-5, respectively. Numbered callouts on the features described match numbered descriptions below each figure.

3-15. OPERATORS CHECKS

3-16. The Operator's Checks portion (Local and Remote) of the 8350A Sweep Oscillator manual provides a quick evaluation of both 8350A and 83590A main functions. Error codes 50 to 99, displayed on the 8350A FREQUENCY display, are reserved to indicate Plug-in related problems. The 8350A Local Check covers the Sweep Oscillator and RF Plug-in. If the correct indications are not obtained, trouble may be in either of the units. If the RF Plug-in is suspected, follow the troubleshooting information in Section VIII, Service, in this manual, to isolate the problem.

3-17. OPERATING INSTRUCTIONS

3-18. Peaking RF Output Power

3-19. Due to normal "aging" of the 83590A, it may be necessary to peak the RF output power to obtain the specified maximum leveled power. The front panel PEAK function is accessed by pressing SHIFT PEAK. In order to monitor the effect of the Peaking function on the RF Output, the 83590A must be set for an unleveled power condition. This can be accomplished by setting the ALC MODE to External (without an external detector) or increasing the Power setting until the RF output is unleveled. With the Peal, function selected and an unleveled RF output, the POWER control should be adjusted to maximize the RF output power over the entire frequency range.

3-20. Internal Leveling

3-21. The most convenient method of RF output leveling is internal leveling. A portion of the RF output is coupled out of an internal directional detector, producing a dc voltage proportional to

3-2

Operation

	Voltage		Fraquan	cy Resolution	
DAC Used	Resolution	Bond 1 2,0 to 7,0 GHz	Band 2 7.0 to 13.6 GHz	Band 3 13,5 to 20 GHz	Full Sweep 2 to 20 GHz
CF Vernier ∆F 1-1/8 of band ∆F 1/8-1/64 of band ∆F ≤1/64 of band	2,5 mV 40 µV 10 mV 1,25 mV 0,156 mV	1,17 MHz 18,25 kHz 4,67 MHz ,584 MHz 73,0 kHz	1,65 MHz 25,78 kHz 6,60 MHz ,825 MHz 103,2 kHz	1,65 MHz 25,78 kHz 6,60 MHz ,825 MHz 103,2 kHz	5,08 MHz 79,38 kHz 20,30 MHz 2,54 MHz 317,2 kHz

Table 3-1, Input Resolution

the RF output signal. This detected de voltage is applied to the ALC circuit.

3-22, External Crystal Detector Leveling

3-23. RF output power may also be leveled externally using a power splitter (or external directional coupler) and a negative output crystal detector. This leveling system uses a power splitter to sample a portion of the RF output signal with a crystal detector to produce a de voltage propertional to the RF output power level. The detector output voltage is compared with an internal reference voltage, and the difference volvage changes the output power level to keep a constant RF output power level, A directional coupler may be used instead of a power splitter to sample the RF signal for the leveling loop. Directional couplers are usually narrow band devices, whereas the power splitter has a flatter frequency response over a wide frequency range. The advantage of a directional coupler is that it does not have as great a coupled loss as the 6 dB loss encountered with the power splitter, therefore, a higher maximum leveled power output may be obtained. Figure 3-6 illustrates a typical crystal detector leveling setup.

3-24. External Power Meter Leveling

3-25. RF output power may also he leveled with a power meter and power splitter (or directional coupler) as shown in Figure 3-7. The sweep time is limited to greater than 100 seconds when this leveling method is used. A sample of the RF output signal is routed to a power meter which produces a dc output voltage proportional to the RF input signal level. This de voltage is applied to the 83590A ALC circuits and compared with an internal reference voltage. A difference voltage is produced and amplified by the ALC amplifier before being applied, as modulator drive, to a PIN Modulator.

3-26. External FM

3-27. The 83590A RF output signal can be frequency modulated using an external modulating signal applied to the 8350A rear panel FM INPUT connector. The external FM function provides a means of obtaining an output frequency that varies under the control of an external modulating signal. A positive-going voltage at the FM INPUT causes output frequency to decrease, while a negative-going voltage causes output frequency to increase. The sensitivity and coupling of the modulating signal may be set via configuration switch (A3S1). Figure 3-9 lists the available configuration switch settings. The configuration switch settings override 8350A Sweep Oscillator non-volatile memory settings at Instrument Preset.

3-28. External Amplitude Modulation

Pulse Modulation (PULSE IN Con-3-29, nector on Plug-inj. The PULSE IN connector provides pulsed or square wave modulation, where the RF output is switched on and off. This input provides an on/off power ratio of greater than 30 dB below specified maximum leveled power. The PULSE IN input is normally at a TTL HIGH (approximately +3 volts de). When a TTL LOW signal (approximately () volts de) is applied, the RF output is turned off. To get the best pulse modulation performance, the RF output power should be set at +20 dBm. With this power setting. a pulse repetition rate of up to 1 MHz is achievable in the 2 to 7.0 CHz frequency bands. With leveled power in this frequency range, pulse repetition rates may be up to 100 kHz. In the 7.0 to 20.0 GHz frequency bands, RF power may be square-wave modulated at repetition rates up to

3-3

Operation

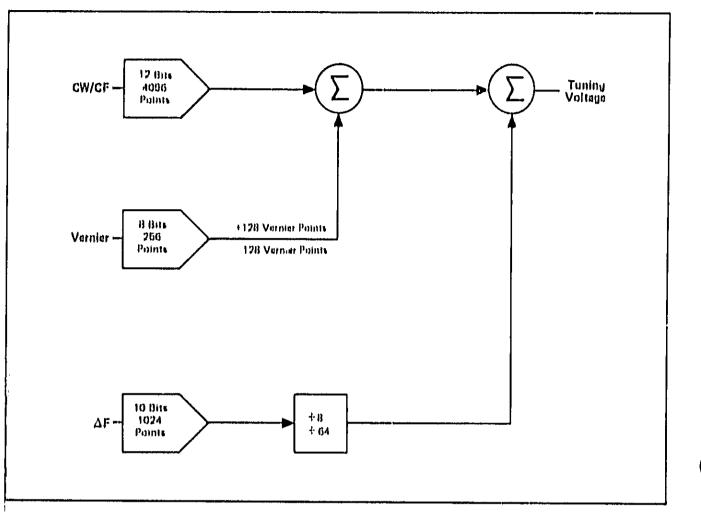
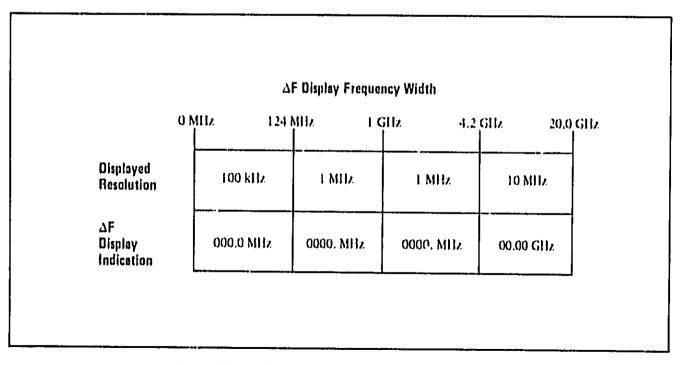
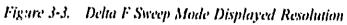


Figure 3-2. Simplified Tuning Voltage Block Diagram





3-4

1

30 kHz at any power output setting. The input impedance for TTL level signals is approximately 500 ohms. If the PULSE IN circuit is driven beyond TTL levels, the input impedance is reduced to approximately 200 ohms due to the diode clamping action. See the specifications and supplemental characteristics in Section 1 for more details on the modulation characteristics when using this input.

3-30, Amplitude Modulation (AM INPUT Connector on B350A). The AM INPUT provides linear amplitude changes (up to approximately [5 dB) proportional to the modulating input voltage. It is limited to a frequency response of about 100 kHz. For maximum depth of modulation (i.e. maximum modulation index), the RF power level should be set to the middle of the control range (e.g. +2.5 dBm for a Plug-in with calibrated power control from -5 to +10 dBm). For Plug-ins equipped with Option 002 (70 dB step attenuator), the middle of the attenuator range should be selected. The center of the power control range may be selected with the front panel power control or by applying a de bias voltage on the external modulating signal. A positive (+) de voltage into the AM INPUT causes a decrease in RF output power; a negative (-) de voltage causes an increase in RF output power.

3-31. RF Power Control

3-32. The RF power set at power-up (during Instrument Preset) may be either maximum power (+10 dBm) or RF power OFF as selected by the configuration switch (A3S1). Refer to Figure 3-9 for this setting. Configuration switch settings relating to the specific model Plug-in used and Option 002 Step Attenuator equipped instruments must be set prior to operation. Configuration switch number 7 is set at the factory and should not be changed.

3-33. Option 002 Stop Attenuator

3-34. With Option 002 installed, the RF output power may be continuously controlled from +10 dBm to -75 dBm. When the selected POWER setting goes below -5 dBm, the step attenuator increments as required in 10 dB steps to a maximum attenuation of 70 dB. Within the individual 10 dB steps of the attenuator, the ALC loop adjusts the power output to the power level programmed by the front panel POWER control. SHIFT Pressing **POWER SWEEP** allows control of power within the ALC range without changing attenuator settings. The display in the SHIFT POWER SWEEP mode disregards

attenuator settings and only displays the ALC setting. Pressing SHIFT SLOPE allows control of attenuator steps without affecting ALC setting. In this mode the attenuator setting is displayed.

3-35. Alternate Sweep Mode

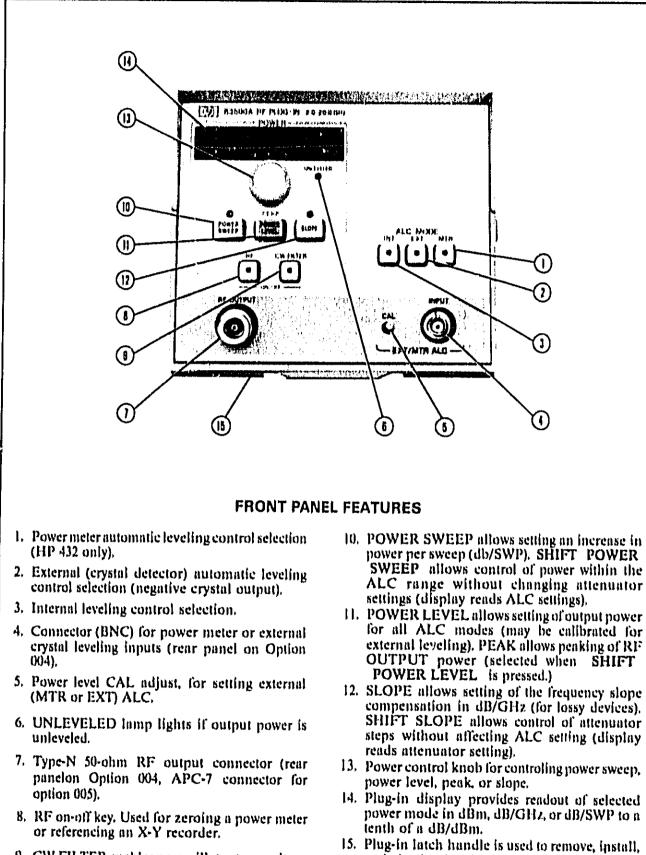
3-36. If the 83590A changes frequency bands (e.g. Band I to Band 3) between each sweep, the minimum sweep time recommended is 100 milliseconds. This allows enough time for the bandswitch operation and settling time for the fundamental oscillator for the next sweep.

3-37. If Option 002 attenuator is installed, and alternate sweep mode is selected, a slow sweep default condition of 1 second/sweep may occur. This, default condition only occurs when the POWER settings of the two alternate sweeps require the attenuator to switch after each sweep. The attenuator is prevented from switching faster than 1 step per second to prevent damage to the attenuator relay coils due to overheating.

3-38. Phase-Lock Operation

3-39. The 83590A RF Plug-in RF output (CW) signal may be phase-locked to an external reforence oscillator by using an external phaselock signal applied to the 8350A rear panel FM INPUT connector. The phase-lock function provides a means of obtaining a very stable CW frequency by transferring the frequency stability of the reference oscillator to the 8350A Sweep Oscillator. If the CW frequency starts to drift, the phase difference between the CW frequency and the reference frequency (reference oscillator) is detected, producing a de voltage. The de voltage is returned to the FM INPUT as a correction signal which restores the CW frequency to its previous point. Stability of the RF output CW frequency is thus determined by the stability of the reference oscillator. The 83590A CW frequency used for phase-locking may be either the RF output or the fundamental oscillator frequency available at the rear panel AUX OUTPUT, Configuration switch (A3S1) switch position 8 must be set for the source of the CW frequency used for phase-locking (Figure 3-9). The CW filter should be turned off in phase lock operation. Although the front panel RF output can be used for phase-locking, this would require a broadband coupling device and a harmonic mixer capable of producing acceptable harmonic content up to 20 GHz. Therefore, it is preferable to use the rear panel AUX OUTPUT for phase-locking. See Figure 3-8, **,** '

Model 83590A



- CW FILTER enables an oscillator tune voltage filter when in CW mode.
- and latch the RF Plug-ir; in the Sweep Oscillator.

Figure 3-4. Front Panel Features

for an example of phase-locking with the rear panel AUX Output.

3-40. OPERATOR'S MAINTENANCE

3-41. Plug-in Error Codes

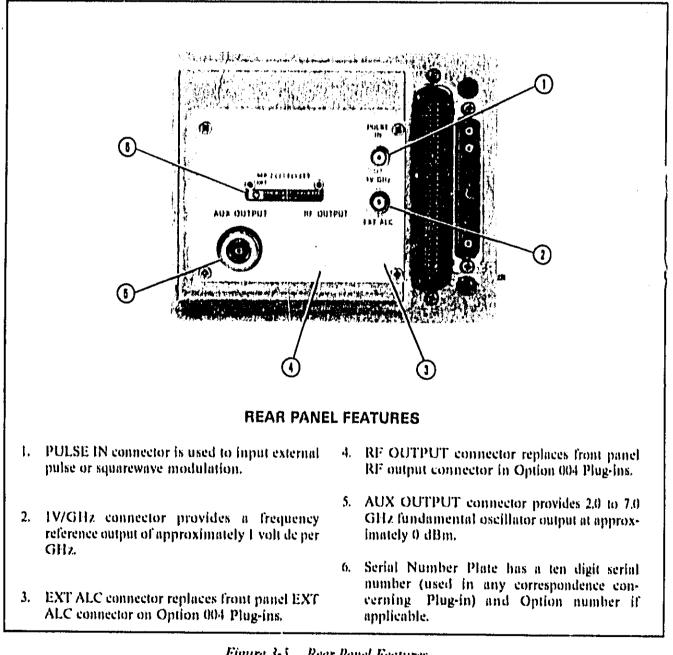
3-42. The 8350A FREQUENCY window will display RF Plug-in error codes (50 to 99) or Sween Oscillator error codes. Information necessary to interpret Plug-in error codes may be found in Section VIII, Service, in this manual,

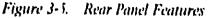
3-43. Fusns

3-44. Power circuits for the Model 83590A RF Plug-in are fused in the 8350A Sweep Oscillator. See the 8350A Sweep Oscillator Operating and Service Manual for fuse locations and replacement instructions.

3-46. **Blue Service Tags**

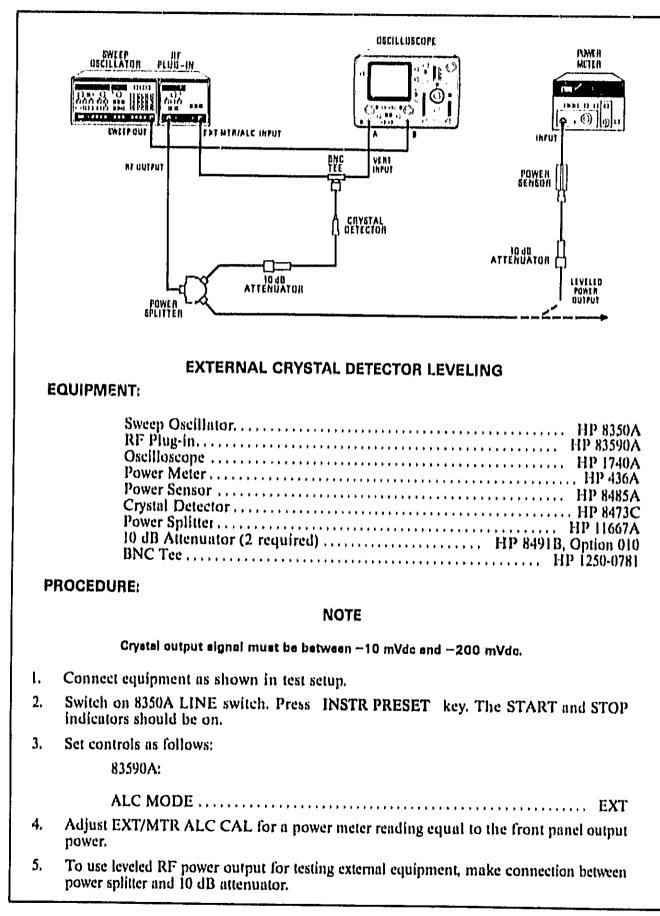
3-46. If the 83590A RF Plug-in requires service, the instrument may be sent to your local HP service organization as described in Section II. Installation, in this manual, Before sending the instrument back, fill out and attach one of the blue service tags. Record any error codes noted on the failure symptoms/special control settings portion of the tag.





3-7

Operation



Model 83590A

Operation

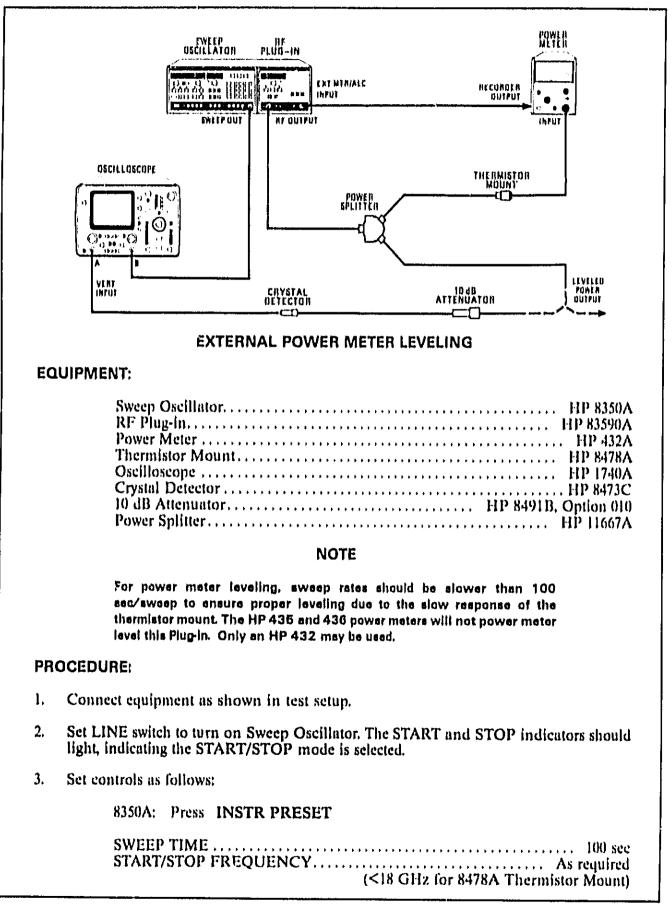
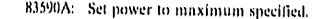


Figure 3-7. External Power Meter Leveling (1 of 2)

Operation

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Model B3590A



ALC MODE..... MTR

- 4. Select +10 dBm range on power meter.
- 5. Adjust 83590A EXT/MTR ALC CAL for a +7 dBm reading on the 432A power meter. Press 8350A SWEEP TRIGGER SINGLE key twice to set single sweep mode and start a sweep.
- 6. To use level RF power output for testing external equipment, make connection between power splitter and 10 dB attenuator.

Figure 3-7. External Power Meter Leveling (2 of 2)

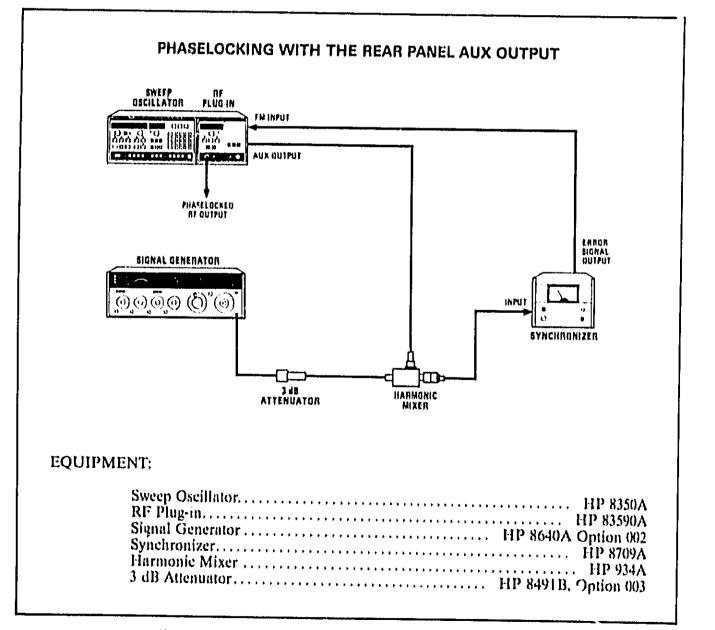


Figure 3-8. Phaselocking with the Rear Panel Output (1 of 2)

3-10

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3.09 to 4.12

4,12 to 5,14

5,14 to 6,16

6,16 to 7,0

Operation

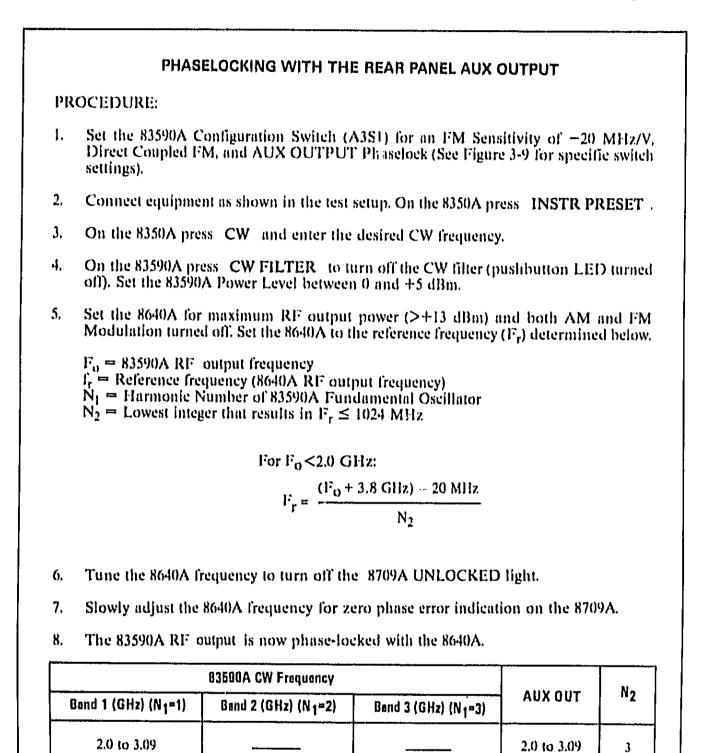


Figure 3-8. Phaselocking with the Rear Panel Output (2 of 2)

13.5 to 15.42

15,42 to 18,48

18.48 to 20.0

7.0 to 8.24

8.24 to 10.24

10,24 to 12.32

12.32 to 13.5

4

5

6

7

3.09 to 4,12

4.12 to 5,14

5.14 to 6.16

6.16 to 7.0

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Operation

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							FRC	ONT PA	NEL
Description			S	witch	Numb	er		T	
	1	2	3	4	5	6	7	8	
Normal Sweep Sequential Sweep Only	0	X X	x x	x x	x x	x x	х х	x x	
No RF Power at Instrument Preset Maximum RF Power at Instrument Preset	x x	X X	x x	1 0	x x	X X	x x	x x	1
-6 MHz/V FM Sensitivity -20 MHz/V FM Sensitivity	x x	x x	x x	x x	1	x x	x x	x x	
Direct-Coupled FM (20 MHz/V) Cross-Over Coupled FM	x x	X X	x x	x x	x x	1 0	x x	x x	
Step Attenuator Option 002 Installed No Step Attenuator	x x	x x	x x	x x	x x	x x	1 0	x x	
AUX OUT Phase Lock RF OUTPUT Phase Lock	x x	x x	x x	x x	x x	x x	x x	1 0	
N	OTES	5	LI		<u> </u>	. <u> </u>]	
Positions:		2.	Sw	itch	is set	at th	e fact	tory a	s follows:
witch Closed = Low (Ground)		s					-1		5 7 8
)2.		Positi	on	0 X		0	0 0) • 0
	Sequential Sweep Only No RF Power at Instrument Preset Maximum RF Power at Instrument Preset -6 MHz/V FM Sensitivity -20 MHz/V FM Sensitivity Direct-Coupled FM (-20 MHz/V) Cross-Over Coupled FM Step Attenuator Option 002 Installed No Step Attenuator AUX OUT Phase Lock RF OUTPUT Phase Lock RF OUTPUT Phase Lock N Positions: witch Open = High witch Closed = Low (Ground) on't Care aries, 1 if Opt 002, 0 if no Opt 00	1Normal Sweep0Sequential Sweep Only1No RF Power at Instrument PresetXMaximum RF Power at Instrument PresetX-6 MHz/V FM SensitivityX-6 MHz/V FM SensitivityXDirect-Coupled FM (20 MHz/V)XCross-Over Coupled FMXStep Attenuator Option 002 Installed No Step AttenuatorXAUX OUT Phase Lock RF OUTPUT Phase LockXNOTESPositions:witch Open = High witch Closed = Low (Ground) on't Care aries, 1 if Opt 002, 0 if no Opt 002.	12Normal Sweep0XSequential Sweep Only1XNo RF Power at Instrument PresetXXMaximum RF Power at Instrument PresetXX-6 MHz/V FM SensitivityXX-20 MHz/V FM SensitivityXX-20 MHz/V FM SensitivityXXDirect-Coupled FM (-20 MHz/V)XXCross-Over Coupled FMXXStep AttenuatorXXOption 002 InstalledXXNo Step AttenuatorXXAUX OUT Phase LockXXRF OUTPUT Phase LockXXNOTESPositions:2.witch Open = High witch Closed = Low (Ground) on't Care aries, 1 if Opt. 002, 0 if no Opt. 002.S	Description123Normal Sweep0XXSequential Sweep Only1XXNo RF Power at Instrument PresetXXXMaximum RF Power at Instrument PresetXXX-6 MHz/V FM SensitivityXXX-20 MHz/V FM SensitivityXXX-20 MHz/V FM SensitivityXXXDirect-Coupled FM (20 MHz/V)XXXCross-Over Coupled FMXXXStep Attenuator Option 002 Installed No Step AttenuatorXXXAUX OUT Phase LockXXXRF OUTPUT Phase LockXXXNOTESPositions:2.Swwitch Open = High wrich Closed = Low (Ground) on't Care aries, 1 if Opt 002, 0 if no Opt 002.Switch	Description1234Normal Sweep Sequential Sweep Only0XXXNo RF Power at Instrument PresetXXX1Maximum RF Power at Instrument PresetXXX1-6 MHz/V FM SensitivityXXXXX-6 MHz/V FM SensitivityXXXXX-20 MHz/V FM SensitivityXXXXXDirect-Coupled FM (-20 MHz/V)XXXXXStep Attenuator Option 002 Installed No Step AttenuatorXXXXAUX OUT Phase Lock RF OUTPUT Phase LockXXXXXNOTESPositions:2.Switch No.witch Open = High witch Closed = Low (Ground) on't CareSwitch No.Pasition	Description12345Normal Sweep Sequential Sweep Only0XXXXXNo RF Power at Instrument Preset Maximum RF Power at Instrument PresetXXX1X-6 MHz/V FM Sensitivity -20 MHz/V FM SensitivityXXXX1X-6 MHz/V FM Sensitivity -20 MHz/V FM SensitivityXXXX1XMitz/V FM Sensitivity -20 MHz/V FM SensitivityXXXXXX1-6 MHz/V FM Sensitivity -20 MHz/V FM SensitivityXXXXXX1-6 MHz/V FM Sensitivity -20 MHz/V FM SensitivityXXXXXX1-6 MHz/V FM Sensitivity -20 MHz/V FM SensitivityXXXXXX1-20 MHz/V FM Sensitivity Cross-Over Coupled FMXXXXXXXStep Attenuator Option 002 Installed No Step Attenuator AUX OUT Phase Lock RF OUTPUT Phase LockXXXXXXXNOTES2.Switch No. 12Positions:2.Switch No. 12Position 02.1 for Opt 002, 0 if no Opt 002.22	123456Normal Sweep Sequential Sweep Only0XXXXXXNo RF Power at Instrument Preset Maximum RF Power at Instrument PresetXXX1XXX-6 MHz/V FM Sensitivity -20 MHz/V FM SensitivityXXXX1XX-6 MHz/V FM Sensitivity -20 MHz/V FM SensitivityXXXX1XDirect-Coupled FM (-20 MHz/V) Cross-Over Coupled FMXXXXX1XDirect-Coupled FM (-20 MHz/V) Cross-Over Coupled FMXXXXX1XStep Attenuator Option 002 Installed No Step Attenuator No Step Attenuator AUX OUT Phase LockXXXXXXXNOTESNOTES2.Switch is set at the Positions:Switch No. 123Positions: aries, 11123Position0XX	Switch NumberDescription1234567Normal Sweep Sequential Sweep Only0XXXXXXNo RF Power at Instrument Preset Instrument PresetXXX1XXXX-6 MHz/V FM Sensitivity -20 MHz/V FM SensitivityXXXX1XXX-6 MHz/V FM Sensitivity -20 MHz/V FM SensitivityXXXX1XX-6 MHz/V FM Sensitivity -20 MHz/V FM SensitivityXXXXX1XDirect-Coupled FM -0 02 Installed No Step Attenuator 	Description12345676Normal Sweep Sequential Sweep Only0XXXXXXXXNo RF Power at Instrument Preset Maximum RF Power at Instrument PresetXXX1XXXXX-6 MHz/V FM Sensitivity -20 MHz/V FM SensitivityXXXX1XXXX-6 MHz/V FM Sensitivity -20 MHz/V FM SensitivityXXXX1XXXDirect-Coupled FM (-20 MHz/V) Cross-Over Coupled FMXXXXX1XXStep Attenuator Option 002 Installed No Step AttenuatorXXXXXX1XNOTESNOTES2.Switch No.123456Positions:2.Switch No.123456

1

PERFORMANCE.

CHECK

SECTION IV PERFORMANCE TESTS

4-1. INTRODUCTION

4-2. The procedures in this section test the electrical performance of the 83590A RF Plugin/8350A Sweep Oscillator combination with the specifications of the Plug-in used as the performance standards. These specifications may be found in Section I of this manual. Due to the extended frequency range of the 83590A, the performance tests in the 8350A Operating and Service Marual do not apply. None of the tests require access to the interior of the 83590A RF Plug-in.

NOTE

Allow the 83590A RF Plug-in and 8350A Sweep Oscillator to warm up for one hour prior to doing any performance tests.

4-3. EQUIPMENT REQUIRED

4-4. Equipment required to test is listed in the Recommended Test Equipment table in Section I of this manual. Any equipment that satisfies the critical specifications given in the table may be substituted for the recommended model.

4-5. OPERATION VERIFICATION

4.6. Operation Verification consists of performing the tests listed in paragraph 4-13 steps 1 to 11 and paragraph 4-14 steps 1 to 13. Operation Verification of the HP-IB functions may be verified by executing the program listed in Section IV of the 8350A Operating and Service Manual. These tests provide reasonable assurance that the Sweep Oscillator and Plug-in are functioning properly and should meet the needs of an incoming inspection (80% verification).

4-7. TEST RECORD

4-8. Table 4-16 provides a tabulated index of the performance tests, their acceptable limits, and a column for recording actual measurements.

4-9. TEST SEQUENCE

4-19. The performance tests should be performed in the order they occur.

4-11. CALIBRATION CYCLE

4-12. The performance tests in this section should be performed at intervals of six months or less for the 83590A.

Performance Tests

Model 83590A

PERFORMANCE TESTS

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Performance Test	83690A Adjustment	8350A Adjustment	
4-13. Frequency Range and Accuracy			
CW Accuracy	5-14, 5-16, 5-17	5,19	
Swept Frequency Accuracy	5-15 thru 5-19, 5-23		
Marker Accuracy	5-14 thru 5-19, 5-23	5-20	
4-14, Jutput Amplitude Power Variations at Maximum Power Power Level Accuracy Power Meter Leveling Power Sweep	5-25 thru 5-28 5-27 5-29		
4-15. Frequency Stability		5-11	
4-16. Residual FM		5-11	
4-17. Spurious Signals Nonharmonies	5-21		
4-10, Residuel AM	5-21, 5-28	5-11	
4-20, External FM	5-30		
4-21. AM On/Off Ratio Square-wave Symmetry	5-2K		

2.3.1. 1.1 n...... 125

4-13. FREQUENCY RANGE AND ACCURACY TEST

SPECIFICATION:

Frequency Range: 2,0 to 20,0 GHz

Frequency Accuracy:

Bands (GHz)	2.0 to 7.0	7.0 to 13,5	13,5 to 20.0	2.0 to 20.0
CW Mode	±5 MHz	±10 MHz	±15 MHz	· - •
All Sweep Modes	±20 MHz	±25 MHz	±30 MHz	±50 MHz
F	±20 MHz	±25 MHz	±30 MHz	±50 MHz
Frequency Markers	±0,5% of sweep width	±0.5% of sweep width	±0.5% of sweep width	±0.5% of sweep width

4-13. FREQUENCY RANGE AND ACCURACY TEST (Cont'd)

DESCRIPTION:

A frequency counter is used to check frequency range and accuracy in the CW mode. The frequency counter is also used to check swept frequency accuracy and markers in the START/STOP mode.

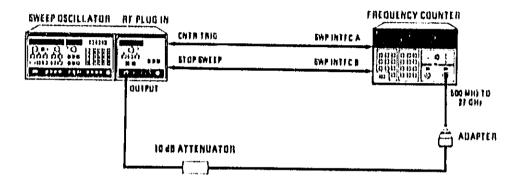


Figure 4-1. Frequency Range and CW Accuracy Test Setup

EQUIPMENT:

Sweep Oscillator.	LED \$350 A
	1111 21314
10-dB Attenuator. HP 8491B, Adaptor Tuno N Country	ACPCC 111
Adaptar Time N Country of the a construction of the 8491 B.	Option 010
Adapter, Type-N female to SMA female	.1250-1404

PROCEDURE:

- 1. Connect equipment as shown in Figure 4-1.
- 2. Set controls as follows:

Frequency Counter

LINE	')
Impedance Switch	`

3. Press 8350A INSTR PRESET Note that the Sweep Oscillator display indicates a START frequency of 2 GHz and a STOP frequency of 20 GHz.

4-13. FREQUENCY RANGE AND ACCURACY TEST (Cont'd)

Frequency Range

- 4. Press 8350A CW key and enter a CW frequency of 2 GHz. If frequency observed on frequency counter is greater than 2 GHz rotate 8350A CW control counterclockwise until frequency on counter is at or below 2 GHz.
- 5. Enter a CW frequency of 20.0 GHz. If frequency observed on frequency counter is lower than 20.0 GHz rotate the 8350A CW control clockwise until the frequency counter reading is at or above 20.0 GHz.

CW Frequency Accuracy

6. Check CW frequency accuracy for each CW frequency listed in Table 4-2. Verify the frequency counter indication at the three points on each band is within the accuracy tolerance in Table 4-2. Follow the sequence of frequencies listed for each band from top to bottom to avoid band crossover problems.

Bands (Accuracy)							
Band 1 (±6 MHz)	Band 2 (±10 MHz)	Band 3 (±15 MHz)					
4.0 GHz	10 G11z	17.0 GHz					
2.0 GHz	7.1 GHz	14.0 GHz					
7.0 GHz	13.5 GHz	20.0 GHz					

Table 4-2. CW Frequency Accuracy

Swept Frequency Accuracy

- 7. Press frequency counter RESET, SWP M (Light on), Plue Key, 1KHz, Press 8350A INSTR PRESET and set sweep time to 105 msec.
- 8. Press the START and STOP frequencies on the 8350A for each band listed in Table 4-3.
- 9. Press 8350A START, SHIFT, then M2. Check the frequency counter reading for the START frequency listed in Table 4-3 and record on the test card.
- 10. Press 8350A STOP. SHIFT, then M2. Check the frequency counter reading for the STOP frequency listed in Table 4-3 and record on the test card.
- 11. Repeat steps 9 through 11 for each band listed.

Performance Tests

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4-13. FREQUENCY RANGE AND ACCURACY TEST (Cont'd)

Band	Start	Stop	Tolerance	
Full Band	2.0 GHz	20.0 GHz	±50 MHz	
Band I	2.0 GHz	7.0 GHz	±20 MHz	
Band 2	7,0 GHz	13.5 GHz	±25 MHz	
Band 3	13.5 GHz	20.0 GHz	±30 MHz	

Table 4-3. Swept Frequency Accuracy Table

Frequency Marker Accuracy

- 12. Press 8350A INSTR PRESET and set sweep time to 105 msee.
- 13. Set first band's START STOP frequencies as listed in Table 4-4.
- 14. Set the 8350A markers to the frequency listed and verify that the frequency counter readings are within tolerance. Enter marker to be checked, then SHIFT M2.
- 15. Set the START and STOP frequencies for each band listed and repeat the previous step with the markers set as listed.

Bond	Sweep Range		Marker Frequencies					
weil4	Start	Stop	Mt	M2	M3	M4	M5	Tolerance
Full Band	2.0 to 20) GHz	3 GHz	6 GHz	10 GHz	14 GHz	18 GHz	±140 MHz
Band 1	2.0 to 7.0	0 GHz	3.0 GHz	6.0 GHz			·· <u></u>	±45 MHz
Band 2	7.0 to 13,	5 GHz	8.0 GHz	12 GHz				±58 MHz
Band 3	13.5 to 2	0 GHz	15.0 GHz	18.0 GHz				±63 MHz

Table 4-4. Frequency Marker Accuracy

4-14, OUTPUT AMPLITUDE TEST

SPECIFICATION:

	Frequency Bands (GHz)							
	2.0 to 7.0	7,0 to 13.6	13,6 to 10,6	13.6 to 20.0	2.0 to 18.6	2.0 to 20.0		
Maximum Loveled Output Power ^{2, 3, 4} (25°C)	+ 10 dBm	+10 dBm	+10 dBm	+8 dBm	+10 dBm	+8 dBm		
With Option 002	+8.5 dBm	+8 dBm	+7 dBm	+5 dBm	+7 dBm	+5 dBm		
Power Level Accuracy ^(t) (Internally Leveled)	<±1.3 dB	<±1.3 dB	<±1.4 dB	<±1.4 dB	<±1.5 dB	<±1.5 dB		
With Option 002 ⁵ (at 0 dB attenuator step)	<±1.5 dB	<±1.5 dB	<±1.6 dB	<±1.6 dB	<±1.7 dB	<±1.7 dB		

Minimum Settevia Power: -5 dBm

With Option 002: -75 dBm

Power Variation	Frequency Bends (GHz)						
(at specified Maximum Leveled Power or below)	2,0 to 7,0	7.0 to 13.5	13.6 to 20	2.0 to 20			
Internally Leveled	±0.7 dB	±0.7 dB	±0.8 dB	±0.9 dB			
Externally Leveled Negative Crystal Detector ⁶ (Sweep time >100 ms)	±0.2 dB	±0.2 dB	±0.2 dB	±0.2 aB			
Externally Leveled Power Meter ⁷	±0.2 dB	±0.2 dB	±0.2 dB	±0.2 dB			

DESCRIPTION:

A Power Meter is used to check power level accuracy, maximum leveled output power and power variations.

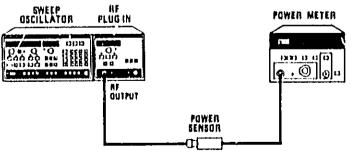


Figure 4-2. Output Amplitude Test Setup (Using HP 436A Power Meter)

4-14. OUTPUT AMPLITUDE TEST (Cont'd)

EQUIPMENTE

Sweep Oscillator,	8350A
Power Meler Hp	436A
Power Sensor	ARSA
Power Meter	412A
Thermistor Mount	8478R
Thermistor Mount	CARGA -
Crystal Detector. HP H	1473C
19 9D AUCHURIOF, AND AND AND A Woincohol Mada	10.10
Power Splitter	579A
Adapta Ture New Land Adapta	740A
Adapter, Type N male to SMA female	-1250
AMADUCE WAVEVILLE IN A DOMAD	10127
BNC TEE	-0781

PROCEDURE:

- 1. Connect equipment as shown in Figure 4-2,
- 2. Press 8350A INSTR PRESET , set SWEEP to MAN.

Maximum Leveled Power and Power Variations

- 3. Set START and STOP frequencies and POWER LEVEL for the first frequency range listed in Table 4-5 (2.0 to 7.0 GHz e. +10 dBm).
- 4. Slowly tune the 8350A FREQUENCY/TIME control and note the minimum power level in the band. Leave the frequency at this low power point.
- 5. Adjust 83590A POWER control for a power meter reading equal to the specified maximum leveled output power.
- 6. Slowly tune the 8350A FREQUENCY/TIME control through the frequency band. Note and record maximum power deviation on test record card.
- 7. Repeat steps 3 through 6 for the other frequency band settings listed in Table 4-5.

Frequency Nange	Maximum Levaled Power		Power Sweep Range	
	(Standard)	(Option 002)	(Standard)	(Optiun 002)
2.0 to 7.0 GHz 7.0 to 13.5 GHz 13.5 to 18.6 GHz 13.5 to 20 GHz 2.0 to 18.6 GHz 2.0 to 20 GHz	+ 10 dBm + 10 dBm + 10 dBm + 10 dBm + 8 dBm + 10 dBm + 8 dBm	+8.5 dBm +8 dBm +7 dBm +5 dBm +7 dBm +5 dBm	15 dB/SWP 15 dB/SWP 15 dB/SWP 13 dB/SWP 15 dB/SWP 13 dB/SWP	13.5 dB/SW ^{**} 13 dB/SWP 12 dB/SWP 10 dB/SWP 12 dB/SWP 10 dB/SWP 10 dB/SWP

Table 4-5. Frequency and Power Settings

4-14. OUTPUT AMPLITUDE TEST (Cont'd)

Power Level Accuracy, Range and Power Sweep

- 8. Set START and STOP frequencies and POWER LEVEL for the first frequency band in Table 4-5 (2.0 to 7.0 GHz at +10 dBm). Engage the 83590A POWER SWEEP, set the dB/SWP level to 16dB/SWP. Disengage POWER SWEEP key.
- Slowly tune the 8350A FREQUENCY/TIME control through the frequency band and note the maximum power level variations above and below the displayed power level setting. Record these on the test record.
- 10. Press 83590A POWER LEVEL key. Use the 8350A 🖤 key to step the power down 1 dB.
- 11. Repeat steps 9 and 10 to check power level accuracy over the full calibrated range (down to -5 dBm).
- 12. Adjust the FREQUENCY/TIME control for highest frequency and note power ineter level. Engage **POWER SWEEP** and set it for maximum leveled power (UNLEVELED light off). Record power meter level change on test record.
- 13. Repeat steps 8 through 12 for the frequencies and power levels listed in Table 4-5.

Power Meter Leveling

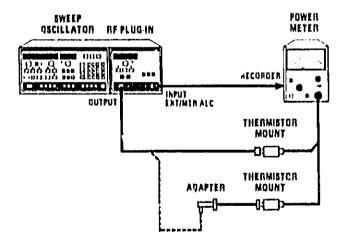


Figure 4-3. Power Meter Leveling Test Setup (Using HP 432A Power Meter)

- 14. Connect equipment as shown in Figure 4-3 using HP 8478B Thermistor Mount.
- 15. Press 8350A INSTR PRESET, set STOP frequency to 18 GHz. Set SWEEP TIME to 100 seconds and SWEEP TRIGGER to SINGLE.
- 16. Adjust ALC EXT/MRT CAL control and power meter range switch for a power meter indication corresponding to the 83590A POWER display.
- 17. Press SWEEP TRIGGER SINGLE key and note power meter variations.

4-14. OUTPUT AMPLITUDE TEST (Cont'd)

- 18. When SWP light goes out, press 8350A CW and set a CW frequency of 18 GHz. Note the power meter indication.
- 19. Change to the K486A Thermistor Mount and adjust the ALC EXT/MTR CAL control for the same power meter indication noted in step 17.
- 20. Set the Sweep Oscillator for a START/STOP frequency of 18 to 20 GHz and a SWEEP TIME of 10 seconds.
- 21. Press SWEEP TRIGGER SINGLE key and note power variations. The combined variations from step 16 and 20 should be $\leq \pm 0.2$ dB.

External Crystal Detector Leveling

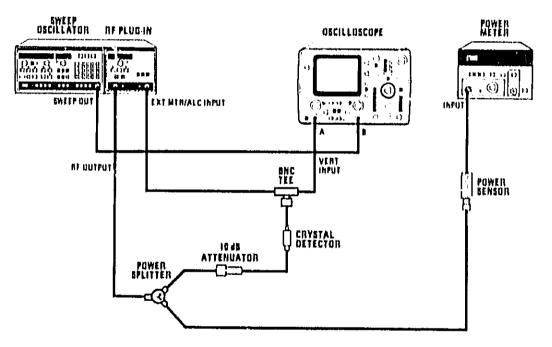


Figure 4-4. Crystal Detector Leveling Test Setup (Using HP 436A Power Meter)

- 22. Connect equipment as shown in Figure 4-4. Press 8350A INSTR PRESET and set SWEEP TIME to 100 milliseconds. Set the oscilloscope for external sweep mode (A vs B).
- 23. Press 8350A CW . Adjust the oscilloscope to the center graticule, Adjust the 83590A POWER LEVEL to decrease the power meter indication by 0.4 dB. Note the new trace position on the oscilloscope: the area between the trace and the center graticule represents the leveling tolerance of ± 0.2 dB.
- 24. Press 8350A START .
- 25. Adjust the oscilloscope trace position so that the lowest point of the trace is on the center graticule. The highest point of the trace should be within the leveled variation limits established in step 22.

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4-15. FREQUENCY STABILITY TEST

SPECIFICATION:

Stability	Frequency Bands (GHz)			
Stautitty	2.0 to 7.0	7.0 to 13.6	13.5 to 20.0	2.0 to 20.0
With 10% Line Voltage Change	±50 kHz	±100 kHz	±150 kHz	±150 kHz
With 10 dB Power Level Change	土200 kHz	±400 kHz	±600 kHz	±600 kHz
With 3:1 Lond SWR	土100 kHz	±200 kHz	±300 kHz	±300 kHz
With Time (in a 10 minute period after one hour warmup)	<±100 kHz	<±200 kHz	<±300 kHz	<±300 kHz

DESCRIPTION:

A frequency counter is used to check frequency change due to line voltage changes, time (10 minutes), output power level changes, and load impedance changes.

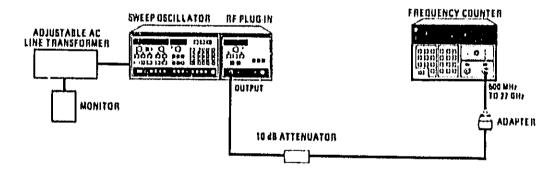


Figure 4-5. Frequency Change with Line Voltage Change

EQUIPMENT:

NOTE

More than one model number is listed for some test equipment. Use only the equipment needed to cover the line voltage used.

Sweep Oseillator.	HD 8350A
ricquency Counter.	110 62.12.8
10 dB Attenuator	HP 8491B Ontion 010
10 dB Attenuator . 3 dB Attenuator . Admitter The Net State of Sta	HP 8491B Ontion (0)3
Adapter, Type-N, female to SMA female	HP 1250-1404

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4-15. FREQUENCY STABILITY TEST (Cont'd)

Adjustable AC Line Transformer and monitor (Select for line voltage nee	eded)
100-120 volt General Radio W	5MTB -
120 V Monitor RCA WV	120B
220-240 volt	
240V Monitor RCA WV	503A
3 dB Attenuator Weinschel Mod	
Adjustable Short Maury Microwave I	

PROCEDURE:

Frequency Change with Line Voltage Change

- L. Connect equipment as shown in Figure 4-5 and set 8350A LINE switch to ON.
- 2. Set adjustable line transformer using suitable monitor to the line voltage set on the 8350A power module. Press the 8350A INSTR PRESET and CW key and enter a CW frequency of 6.0 GHz. Rotate frequency counter SAMPLE RATE knob to HOLD, press SET, OFS MHz, Blue Key, then rotate the Frequency Counter SAMPLE RATE knob counter-clockwise back to the normal position.

Nominal Line Voltage	100V	115/120V	220V	240V
Low Line Voltage	90V	108V	198V	216V
High Line Voltage	105V	126V	231 V	252V

Table 4-6. High and Low Line Voltage Selection Table

- 3. Set adjustable line consformer to the low line voltage using suitable monitor which corresponds to the corresponds to the correspondence frequency displayed on counter.
- 4. Set adjustable line transformer using suitable monitor to the high line voltage using suitable monitor which corresponds to the selected nominal voltage. Check and record on the test record card step 4 the difference frequency displayed on counter.
- 5. Repeat steps 2 through 4 for the frequencies listed in Table 4-7.

Band	CW Frequency	Frequency Change
Band 1	6.0 GHz	±50 kHz
Band 2	12.0 GHz	±100 kHz
Band 3	18 GHz	±150 kHz

Table 4-7. Frequency Change with Line Voltage Change



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Model 83590A

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4-15. FREQUENCY STABILITY TEST (Cont'd)

Frequency Change with Time (10 minutes)

- Set adjustable line transformer voltage to nominal. Enter POWER LEVEL 1 0 dBm, then CW 6 GHz (wait one minute for frequency counter and Oscillator to settle).
- 7. Rotate the frequency counter SAMPLE RATE knob to HOLD, press SET, OFS MHZ, Blue Key, then rotate the Frequency Counter SAMPLE RATE knob counter-clockwise back to the normal position. The counter is now indicating frequency change with time. Wait 10 minutes while observing frequency count for maximum frequency change and record this maximum change on the performance test record card step 7.
- 8. Repeat steps 6 and 7 for the other frequencies shown in Table 4-8.

Bond	CW Frequency	Frequency Change
Band 1	6,0 GHz	±100 kHz
Band 2	12.0 GHz	±200 kHz
Band 3	18 GHz	±300 kHz

Table 4-8, Frequency Change with Time

Frequency Change with 10 dB Power Level Change

- 9. Enter CW 6 GHz.
- 10. Rotate the frequency counter SAMPLE RATE knob to HOLD, press SET, OFFSET, Blue Key, then rotate the frequency counter SAMPLE RATE knob counter-clockwise back to the normal position. Enter POWER LEVEL 0 dBm, Verify the frequency change is less than given in Table 4-9.
- 11. Repeat steps 9 and 10 for the other frequencies given in Table 4-9.

Band	CW Frequency	Frequency Change
Band 1	6.0 GHz	±200 kHz
Band 2	12.0 GHz	±400 kHz
Band 3	18 GHz	±600 kHz

Table 4-9. Frequency Change with Power Level Change

4-15. FREQUENCY STABILITY TEST (Cont'd)

Frequency Change With 3:1 Load SWR

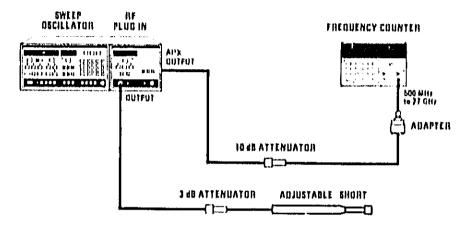


Figure 4-6. Frequency Change with 3:1 Load SWR Test Setup

- 12. Connect equipment as shown in Figure 4-6. Press the 8350A INSTR PRESET, CW 6 GHz, then POWER LEVEL 1 0 dBm.
- 13. Since the frequency of the AUX OUTPUT is being counted, a multiplication factor must be entered for bands 2 and 3 only to yield actual RF OUTPUT frequency errors. No factor is needed for band 1. In band 2 press SET, ..., (decimal point), 2, and ENTER on counter. In band 3, press SET, ..., 3, and ENTER.
- 14. On counter rotate the SAMPLE RATE knob clockwise to HOLD, press SET, OFS MHZ, Blue Key, then rotate the SAMPLE RATE knob counter-clockwise to the normal position on the Frequency Counter.
- 15. Adjust the adjustable short through its range while observing the frequency counter for the greatest plus and minus frequency change. Check that the peak-to-peak frequency change is less than given in Table 4-10.
- 16. Enter the next CW frequency and repeat steps 14 and 15. To clear the counter multiplication factor, press SET . . and ENTER .

Band	CW Frequency	Frequency Change
Band I	6.0 GHz	±100 k**z
Band 2	12.0 GHz	±200 kHz
Band 3	18 GHz	±300 kHz

Table 4-10. Frequency Change wit	h 3:1	Lovd SWR
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Performance Tests

Model 83590A

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PERFORMANCE TESTS

4-16. RESIDUAL FM TEST

SPECIFICATION:

10 Hz to 10 kHz Bandwidth, CW mode with CW Filter 2.0 to 7.0 GHz: <5 kHz (peak) 7.0 to 13.5 GHz: <7kHz (peak) 13.5 to 20 GHz: <9 kHz (peak)

DESCRIPTION:

The CW RF output signal is slope-detected by using the linear portion of a spectrum analyzer resolution bandwidth filter in the zero-span mode.

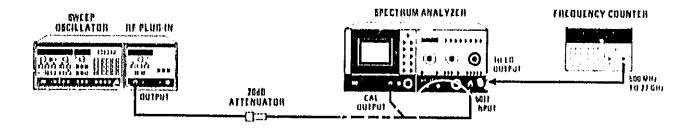


Figure 4-7. Residual FM Test Setup

EQUIPMENT:

Sweep Oscillator.	HP 8350A
Spectrum Analyzer	HP 8565A
Prequency Counter	HD 51.11A
10 dB Attenuator Weinschel	Model 9-10

PROCEDURE:

- 1. Connect equipment as shown in Figure 4-7. Connect the spectrum analyzer CAL OUTPUT to the spectrum analyzer input.
- 2. Press 8350A INSTR PRESET , CW . Enter a CW frequency of 6.0 GHz.

NOTE

To mimimize drift, allow five minutes warmup before continuing with test.

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4-16. RESIDUAL FM TEST (Cont'd)

3. Set spectrum analyzer controls as follows:

TUNING
FREQUENCY SPAN/DIV
RESOLUTION BW
INPUT ATTEN. -30 dB
REFERENCE LEVEL10 dBm
AMPLITUDE SCALE.
AUTO STABILIZER
SWEEP TIME/DIV
BASELINE CLIPPER
VIDEO FILTER

- 4. Adjust spectrum analyzer TUNING to center the 100 MHz CAL OUTPUT signal on the spectrum analyzer display.
- 5. Adjust spectrum analyzer REFERENCE LEVEL controls to place the peak of the signal trace at the reference level (top) graticule line.
- 6. Reduce RESOLUTION BW to 100 kHz and FREQUENCY SPAN/DIV to 100 kHz while keeping the signal centered with the FINE TUNING control. The spectrum analyzer display should be as shown in Figure 4-8.

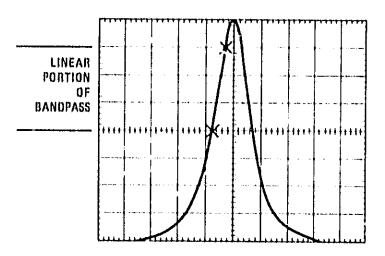


Figure 4-8. Spectrum Analyzer Display for Residual FM

- Set the FREQUENCY SPAN MODE to ZERO SPAN and adjust the FINE TUNING control counterclockwise to position the CRT trace on the center horizontal graticule. Note the frequency counter indication: _______ kHz.
- 8. Adjust the FINE TUNING control clockwise to position the CRT trace on the seventh graticule (one division below the Reference Level). Be sure to stay tuned on the lower frequency side of the signal bandpass. Note the frequency counter indication:

4-16. RESIDUAL FM TEST (Cont'd)

- 9. The spectrum analyzer demodulation sensitivity per division is calculated as one third of the difference frequency between the frequencies noted in steps 7 and 8. Calculate the demodulation sensitivity: <u>kHz/Div.</u>
- 10. Connect the 1350A RF OUTPUT signal to the spectrum analyzer.
- 11. Set spectrum analyzer controls as , ollows:

TUNING.	6.00 GHz
FREQUENCY SPAN/DIV	5 MHz
AMPLITUDE SCALE	LIN
REFERENCE LEVEL	$\pm 10 \text{ dBm}$

- 12. Adjust spectrum analyzer REFERENCE LEVEL controls to place the peak of the signal trace at the reference level (top) graticule line.
- 13. Reduce FREQUENCY SPAN/DIV to 0 while keeping the signal centered on the CRT with the FINE TUNING control.
- 15. Position the trace between the fifth and seventh graticules by turning the FINE TUNING control counterclockwise. STORE a single trace.
- 16. Note the maximum peak-to-peak deviation in divisions of the CRT trace. The peak deviation is one-half the peak-to-peak deviation. Multiply the peak deviation by the modulation sensitivity calculated in step 8.

Residual FM (kHz) = (peak-to-peak deviation/2) X (demodulation sensitivity)

- 17. Verify that residual FM is within tolerance given in Table 4-11.
- 18. R¹ peat steps 11 through 17 with spectrum analyzer and RF Plug-in tuned to each frequency listed in Table 4-11.

Band	CW Frequency	Rosidusi FM
Band 1	6.0 GHz	<8 kHz
Band 2	12.0 GHz	<15 kHz
Band 3	18,0 GHz	<15 kHz

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Table 4-11. Residual FM

4-17. SPURIOUS SIGNALS TEST

SPECIFICATIONS:	Frequency Bands (GHz)			
	2.0 to 7.0	7.0 to 13.5	13.5 to 20	2.0 to 20
Harmonics (in dB below carrier)	>25 dB	>25 dB	>25 dB	>25 dB
Non-Harmonics	>50 dB	>50 dB	>50 dB	>50 dB

DESCRIPTION:

RF output signal from Sweep Oscillator is displayed on a spectrum analyzer to verify that harmonic and non-harmonic spurious signals are at or below the specified level.

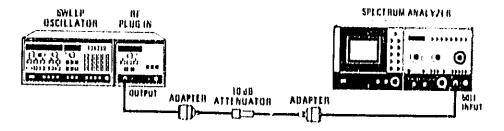


Figure 4-9. Spurious Signals Test Setup

EOUIPMENT:

Sweep Oscillator.	LTD \$350A
Spectrum Analyzer	
10 dB Attenuator. Weinsch	ACOCK III ADODA
Adapter Tupo N mala to SMA Const.	iel Model 9-10
Adapter, Type N male to SMA female	HP 1250-1250
Adapter, Type N female to SMA female	HP 1250-1562

PROCEDURE:

- I. Connect equipment as shown in Figure 4-9.
- 2. Set controls as follows:

8565A: Set all Normal Settings (controls marked with green) FREQUENCY BAND GHz 1.7 to 4.1 INPUT ATTEN 10 dB REF LEVEL dBm. +10 dBm FREQUENCY SPAN MODE. FULL BAND
8350A Press INSTR PRESET, CW, 2 GHz,
83590A POWER Specified Maximum Leveled Power CW FILTER ON

4-17. SPURIOUS SIGNALS TEST (Cont'd)

NO LE

The spectrum analyzer originates some mixing products that may appear on the display, if a signal is in question, increase the spectrum analyzer input attenuation by 10 dB, note if signal decreases in amplitude by 10 dB, then return the attenuator to the original position. If the signal in question comes from an external source, it will change by 10 dB. If the signal in question originates in the spectrum analyzer, the level will either change by greater or less than 10 dB or may not change at all.

The 8350A CW control when being rotated may generate some noise spikes. These signals should disappear when rotation is stopped.

If a spurious signal is found that appears out of specifications check the fundamental signal amplitude to ensure it is at maximum specified power. Then check spurious level by substituting a known amplitude signal on the spectrum analyzer.

 Adjust the 8350A CW control through the entire frequency range of the RF Plug-in (2.0 to 20.0 GHz) and check for harmonic and non-harmonic spurious signals. The specifications for harmonic and non-harmonic signals are listed below.

Frequency Band (83590A)	Harmonics dB helow carrier	Nonharmonics dB below carrier
2.0 to 7,0 GHz	>25 dB	>50 d))
7,0 to 13,5 GHz	>25 dB	>50 dB
13.5 to 20 GHz	>25 dB	>50 dB

Tably 4-12, Spurious Signals Specifications

4-18. OUTPUT SWR TEST (INTERNALLY LEVELED)

SPECIFICATION:

Output SWR: <1.9 Option 002: <2.1

DESCRIPTION:

The RF Output signal is measured using a directional coupler, crystal detector, and oscilloscope. The signal at the oscilloscope contains (1) the incident signal from the oscillator, and (2) the reflected signal. The reflected signal is developed as follows: The incident signal travels down the 20 cm air lines, encounters the open end, and is reflected back to the source. If the reflected signal at the RF OUTPUT connector encounters a perfect 50-ohm source match, no signal is reflected back. However, the greater the mismatch, the greater the reflected signal. This reflected signal either adds to or subtracts from the incident signal. This variation is displayed on the oscilloscope.

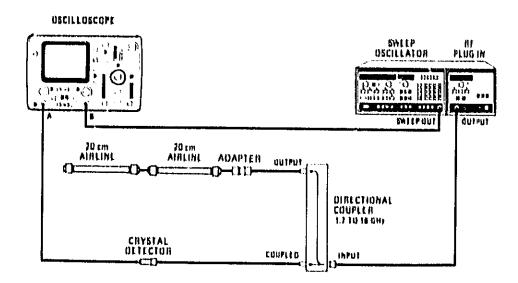


Figure 4-10. Output SWR Test Setup

EQUIPMENT:

Sweep Oscillator	ne such
Crystal Detector	1170112
20-cm Air Lines (2 required)	116673

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Model 83590A

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4-18. OUTPUT SWR TEST (Cont'd)

PROCEDURE

- 1. Connect equipment as shown in Figure 4-10. Put oscilloscope in A vs. B mode, and adjust horizontal offset and Channel B sensitivity so the trace fills the screen.
- 2. Press INSTR PRESET, START, 2, GHz, STOP 1 8 GHz on 8330A. Set DISPL BLANKING off and RF BLANKING on.

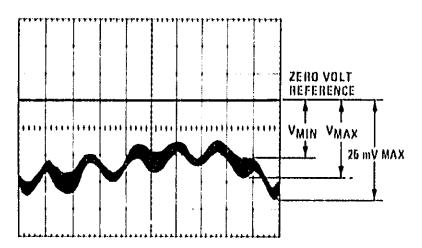


Figure 4-11. Typical Low Frequency Swept SWR Measurement

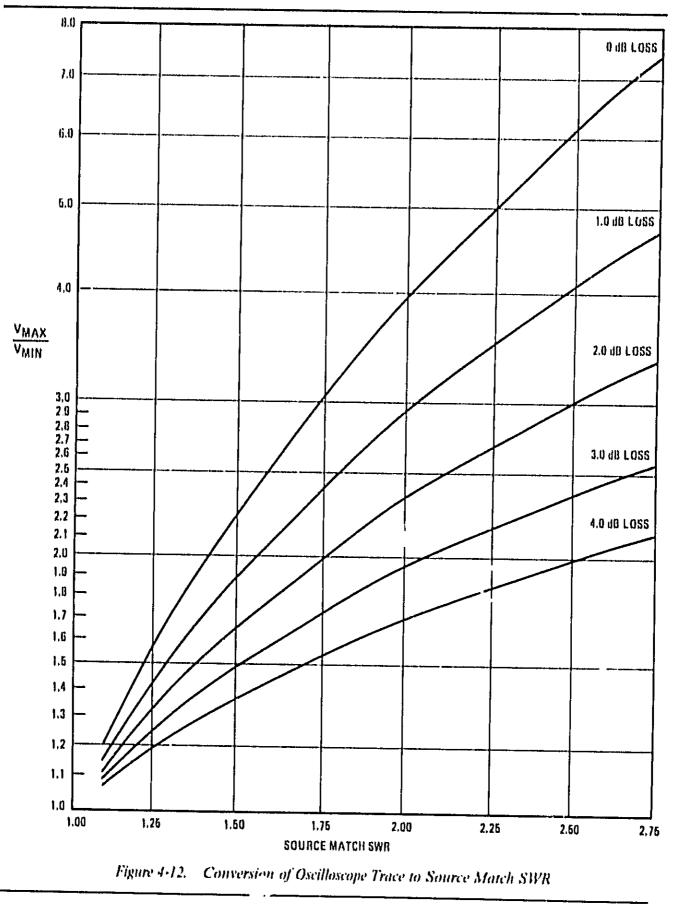
- 3. Adjust POWER control on Plug-in for a maximum output power of -25 millivolts peak trace on oscilloscope display in order to keep crystal in source law output range.
- 4. Select points on trace where V MAX/V MIN appear to have greatest separation and calculate V MAX/V MIN for each point (see Figure 4-11).
- 5. Convert greatest V MAX/V MIN ratio noted in step 10 into source match SWR using Figure 4-12 on the 0 dB loss line. The SWR should be less than 1.9 (2.1 for Option (02).

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PERFORMANCE TESTS

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4-19. RESIDUAL AM

SPECIFICATION:

Residual AM in 100 kHz Bandwidth: \geq 50 dB (in dB below carrier and at specified maximum leveled power).

DESCRIPTION:

The RF Output signal from the RF Plug-in is amplitude modulated with a square wave from the 8350A. This modulated signal is us/d to establish a reference on the RMS voltme or that is 9 dB below actual carrier signal. The 9 dB reduction occurs because of voltmeter response to square wave and square-law response of crystal detector. Modulation is then removed and the magnitude of the Residual AM component is measured with respect to established reference.

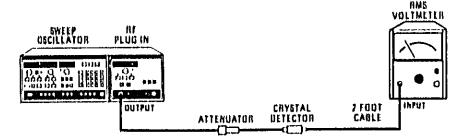


Figure 4-13. Residual AM Test Setup

EQUIPMENT:

Sweep Oscillator.	HP 8350A
RMS Voltmeter	HP 3400A
Crystal Detector HP 8470B	Option 012
Attenuator Refer to PRO	OCEDURE
60 cm (24 in) cable (Limits bandwidth to approximately 100 kHz)	HP 11170B

PROCEDURE:

- 1. Connect equipment as shown in Figure 4-13 using a 20 dB attenuator.
- 2. Press INSTR PRESET, CW, engage □ MOD (1 kHz or 27.8 kHz), disengage DISPL BLANK.

NOTE

A 41 dB decrease in the RMS voltmeter indication corresponds to a 50dB reduction in signal level. A correction factor of 9 dB is added because of the RMS voltmeter response to a square wave and the square-law response of the crystal detector.

- 3. Set POWER LEVEL to +10 dBm and CW frequency to 6 GHz.
- 4. Vary attenuation using 3 dB, 6 dB, and 10 dB attenuators until reading on RMS voltmeter is $-28 \text{ dB} \pm 3 \text{ dB}$. Note voltmeter reading.

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Model 83590A

Performance Tests

PERFORMANCE TESTS

4-19. RESIDUAL AM (Cont'd)

- Disengage □□ MOD. Change RMS voltmeter range switch to obtain an on-scale indication. Calculate the difference between this reading and the indication noted in step 4. Add 9 dB to compensate for square-law inequities, and verify this meets the tolerance in Table 4-13.
- 6. Engage ⊔⊓MOD . Repeat steps 4 and 5 for frequencies given in Table 4-13.

Øand	CW Frequency	Residual AM (dB below cerrier)
Band 1	6.0 GHz	>50 dB
Band 2	12.0 GHz	>50 dB
Band 3	18,0 GHz	>50 dB

Table 4+13. Residual AM

4-20. EXTERNAL FREQUENCY MODULATION TEST

SPECIFICATION:

Modulation Frequency	Cross-Over Coupled	Direct Coupled
DC to 100 Hz:	±75 MHz	±12 MHz
100 Hz to 1 MHz;	±7 MH2	±7 MHz
1 MHz to 2 MHz:	±5 MH2	±5 MHz
2 MHz to 10 MHz:	±1 MHz	±1 MHz

DESCRIPTION:

The RF Output is modulated with an external signal at 100 Hz, 1 MHz, 2 MHz and 10 MHz. The 100 Hz deviation is measured directly on a spectrum analyzer. The deviation at the higher frequencies is found by using a delay line discriminator to observe an increase in the modulation on an oscilloscope until distortion is observed. This frequency change is measured on a frequency counter.

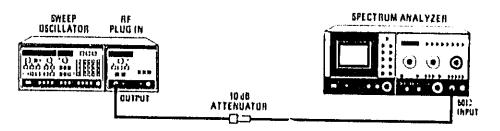


Figure 4-14. 100 Hz External Frequency Modulation Test Setup

4-20. EXTERNAL FREQUENCY MODULATION TEST (Cont'd)

EQUIPMENTE

Sweep Oscillator.	HP 8350A
Spectrum Analyzer	HP 8565A
Frequency Counter	HP 5343A
Function Generator	
Oscilloscope Any general purpose oscillosco	ope such as
HP 1222A	or 1740A
0 dB Attenuator HP 8491B	Option 010
Power Splitter	HÞ 11667A -
Delay Line Discriminator (See	Figure 1-3)

' Add a 50Ω load and BNC Tee to each oscilloscope input.

PROCEDURE:

100 Hz Modulation

- 1. Ensure that modulation sensitivity is set to -20 MHz/volt and modulation coupling to DC (see Figure 3-10 Configuration Switch). Connect equipment as shown in Figure 4-14.
- 2. Press 8350A INSTR PRESET, CW and disengage the DISPL BLANK key. Disengage RF Plug-in CW FILTER key. Center fundamental signal on spectrum analyzer CRT display. Set function generator frequency to 100 Hz sinewave and amplitude to full counterclockwise. Adjust function generator amplitude control slowly clockwise while monitoring display on spectrum analyzer. Deviation from center line should be symmetrical at first then become non-symmetrical as deviation increases.
- 3. Note point at which deviation becomes non-symmetrical and verify that it is greater than ± 12 MHz.
- 4. Turn 8350A LINE switch to off. Remove RF Plug-in and switch modulation coupling to crossover (see Figure 3-10 Configuration Switch). Install the RF Plug-in and turn the 8350A line switch to ON. Then repeat steps 2 and 3. The highest symmetrical deviation frequency should be greater than ± 75 MHz.

>100 Hz FM Modulation

- 5. Set function generator frequency to 1 MHz. Set both oscilloscope inputs to 50Ω .
- 6. Set function generator output amplitude to 0.1 volt p-p output. Connect equipment as shown in Figure 4-15 with function generator output not connected. Adjust CW and CW VERNIER for a delay line discriminator output of 0 volts as observed on Channel A of the oscilloscope. Note frequency counter reading.

4-20. EXTERNAL FREQUENCY MODULATION TEST (Cont'd)

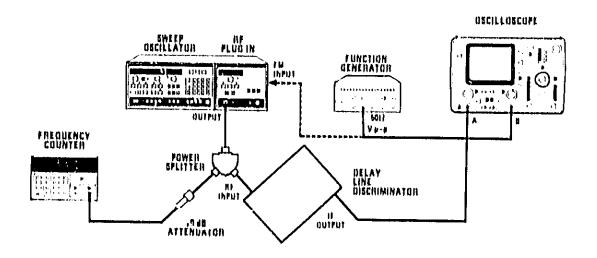
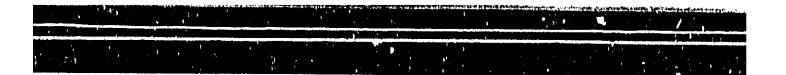


Figure 4-15. >100 Hz Frequency Modulation Test Setup

- Connect the function generator output to 8350A FM INPUT (rear panel) and adjust Channel A of the oscilloscope for a clear display of the function generator sinewaye.
- 8. Increase the function generator output amplitude until the deviation displayed on Channel A becomes non-symmetrical or distorted. Use Channel B of the oscilloscope to monitor the function generator output. If the output is offset the test is invalid.
- 9. Mark the peak of the sinewave displayed on Channel A with a grease pencil. Remove the function generator output from FM INPUT and adjust CW/CW VERNIER to the grease pencil mark. Calculate the difference between the present frequency counter reading and the previous reading (step 6). Verify frequency difference is greater than minimum given in Table 4-14 below for the FM frequency range tested.
- 10. Repeat steps 6 through 9 with the function generator set at 2 MHz and at 10 MHz. Verify the results according to Table 4-14 below.
- 11. Change mode of Plug-in modulation coupling and repeat steps 6 through 10. Verify the results according to Table 4-14 below.

Modulation Frequency	Direct Coupled	Cross-Over Coupled
L MHz	±7 MHz	±7 MHz
2 MHz	±5 MHz	±5 MH2
10 MHz	±1 MHz	±1 MHz

Table 4-14, External Frequency Modulation



Performance Tests

Model 83590A

PERFORMANCE TESTS

4-21. AM ON/OFF RATIO AND SQUARE WAVE SYMMETRY TEST

SPECIFICATION:

On/Off Ratio: ≥30 dB

Symmetry: 40/60

DESCRIPTION:

The AM ON/OFF ratio is checked on the amplitude axis of a video triggered spectrum analyze: display, The symmetry is checked by calculating the on/off time ratio on the frequency axis.

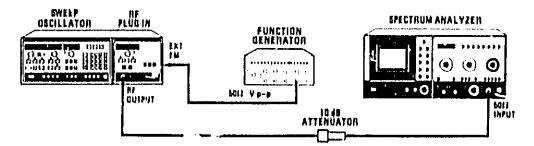


Figure 4-16. AM ON/OFF Ratio and Square Wave Symmetry Test Setup

EQUIPMENT:

Sweep Oseilintor	HP 8350A
10 dB Attenuator HP 8491B Spectrum Analyzer	Option 020
Spectrum Analyzer	HP 8565A

PROCEDURE:

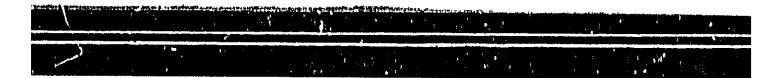
- Connect equipment as shown in Figure 4-16. Press 8350A INSTR PRESET CW
 4 GHz and engage □ MOD. Set 83590A POWER LEVEL to +10 dBm.
- 2. Set controls as follows:

8565A:

Set all Normal settings (controls marked with green)

10.15

FREQUENCY BAND GHZ	3.8 to 8.5 GHz
INPUT ATTENUATION	10 dB
REFERENCE LEVEL	10 dBm
FREQUENCY SPAN MODE	ZERO SPAN
SWEEP TRIGGER	VIDEO
RESOLUTION BW	3 MHz
AUTO STABILIZER	ÒFF
SWEEP TIME/DIV	nsec for 1 kHz



Model 83590A

Performance Tests

4-13

PERFORMANCE TESTS

4-21. AM ON/OFF RATIO AND SQUARE WAVE SYMMETRY TEST (Cont'd)

- 3. Adjust spectrum analyzer TUNING control to center 4 GHz signal on CRT. Adjus, REFERENCE LEVEL to set signal on top trace. Verify that the AM ON/OFF ratio (peak-to-peak signal variation) is greater than 30 dB.
- 4. Verify that the squarewave symmetry of the observed signal is between 40 and 60 percent.

4-22. STEP ATTENUATOR ACCURACY TEST (OPI'ION 002)

SPECIFICATION:

Attenuator Accuracy	Attenuator Setting (dB)						
	10	20	30	40	50	60	70
2,0 to 12,4 GHz	0,6	0,7	0,9	1.8	2,0	2.2	2.3
12.4 to 18 GHz	0.7	0,9	1.2	2.0	2.3	2.5	אי
18 to 20 GHz	0,9	L.3	2,5	3,0	3.2	3,3	3.5

DESCRIPTION:

The Plug-in RF output is compared to a specially calibrated attenuator and displayed on a spectrum analyzer.

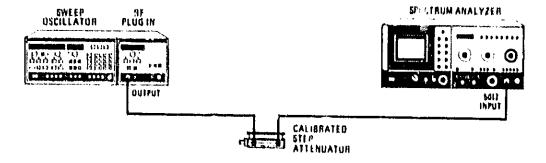


Figure 4-17. Attenuator Accuracy Test Setup

EQUIPMENT:

Sweep Oseillator	the stens
TTD DDD	
Spectrum Analyzer	5A Opt. 890
	HP 8565A

4-22. STEP ATTENUATOR ACCURACY TEST (OPTION 002) (Cont'd)

PROCEDURE:

Connect equipment as shown in Figure 4-17. Press 8350A INSTR PRESET, CW
 4 GHz. Set the 83590A POWER LEVEL to ±4 dBm.

2. Set controls as follows:

Step Altenuator

Spectrum Analyzer

Set all normal settings (controls marked with green)
INPUT ATTEN
PREQUENCY SPAN/DIV
PREQUENCY SPAN MODEL
VIDEO FILIER, and a substant an
FREQUENCY BAND

- 3. Press 8350A POWER LEVEL, STEP SIZE, 1, 0, and dBm/dB.
- 4. Note the actual attenuation values on the calibrated step attenuator's (Option 890) calibration report at the frequency and attenuation steps used. Calculate the Reference Attenuation Error for each step as shown below; record this error in the Attenuation Error column of Table 4-15.

Attenuation Error = (Cal. Ref Atten. - Cal. Step Atten.) - (Ref. Setting - Step Setting)

For example, with a Reference setting of 70 dB, the calculation for the 30 dB step setting is as follows (Note that the actual attenuation stepped in this example is 38.75 dB (69.55 dB - 30.80 dB) :

Example Calibration Report values:

70 dB setting is actually 69.55 dB 30 dB setting is actually 30.80 dB

Attenuation Error = (69.55 dB - 30.80 dB) - (70 dB - 30 dJ) = -1.25 dB

- 5. Adjust spectrum analyzer TUNING control to center notch on Sweep Oscillator output signal. Reduce spectrum analyzer FREQUENCY SPAN/DIV to .2 MHz and recenter TUNING control. Press FREQUENCY SPAN MODE ZERO SPAN key and adjust FINE TUNING to peak signal on spectrum analyzer display. Adjust spectrum analyzer REFERENCE LEVEL VERNIER for a trace at the center graticule line. Press 1 dB/DIV and recenter trace.
- 6. Press the 8350A 🖘 key and decrease the reference attenuation by 10 dB.

4-22. STEP ATTENUATOR ACCURACY TEST (OPTION 002) (Cont'd)

- 7. Record the power level variation from the center graticule (reference) on the spectrum analyzer display (be sure to designate the direction of change: \pm is above and \pm is below the reference).
- 8. Algebraically add the Attenuation Error and Deviation from 0 reference and record the sum in the Attenuator Accuracy column of T 5 le 4-15 below. Repeat steps 6 and 7 for the other attenuation values.

Reference Setting #70 dB	Attenuation Error	Deviation from 0 rof	Attenuator Accuracy
70-60			
70-50			······································
70-40			/
70-30	<u></u>		
70-20		·	
7010			
700			<u></u>

Table 4-15. Step Attenuator Accuracy

- 9. Press 8350A CW 1 5 GHz , Repeat the test at 15 GHz.
- 10. Press 8350A CW I B GHz. Repeat the test at 18 GHz.

Limits	Step	Conditions	Lower Limit	Monsured Value	Upper Limit
4-13. Frequency Range and Accuracy	,			<u></u>	
CW Accuracy					
, , , , , , , , , , , , , , , , , , ,	4.	Start frequency = 2.0 GHz			
	5.	Stop frequency = 20 GHz	20 (11)2		2.0 (11)
2.0 to 7.0 GHz: ±5 MHz					
ro in 10 CH18 To BH11	6 .	CW frequency = 4 GH ₂	3.995 (31)	-	4.005 (311,
		CW frequency = 2.0 GHz CW frequency = 7.0 GHz	1.995 G11z		2.005 GHz
		contrapacticy = 73/0112	0.995 GHz		7.005 GH
7.0 10 13.5 こ月7: 出10 M目2		CW frequency = 10 GHz	9.99 GHz		10.01 GH7
		CW frequency = 7.1 GHz	7.09 GHz		- 7.11 GHz
		CW frequency = 13.5 GHz	13:49 (311)		13.51 GHz
13.5 to 20 GHz: ±15 MHz		CW frequency = 17.0 GHz	10,000,000		
		CW frequency = 14.0 GHz	16.985 CH12 13.985 CH12		17.015 GH
	i	CW frequency = 20.0 GHz	19.985 CH12		14.015 CH1 20.015 CH1
Swept Frequency Accuracy					20.015 Off
2.0 to 20 GHz: ±50 MHz	9,	Stude Fasting and a start			
	10.	Start frequency = 2.0 GHz Stop frequency = 20 GHz	1.95 GHz		2.05 GHz
•	,	and requercy - so citiz	19.95 G117		20.05 GHz
2.0 to 7.0 GHz: ±20 MHz	- 11.	Start frequency = 2.0 GHz	1.98 GHz		2.02 (111)
		Stop frequency = 7.0 GHz	6.98 GHz		7.02 (1112
7.0 to 13.5 GHz: ±25 MHz		Start frequency = 7.0 GHz			
		Stop frequency = 13.5 GHz	6.975 GH		7.025 GHz
		and requerey 1515 CHIV	13.475 GHz		13.525 GR7
13.5 to 20 GHz: ±30 MHz		Start frequency \$214 JH7	13.47 (31)		13.53 (3)17
		Stop frequency = 20 GHz	19.97 GHz		20.03 GHz
darker Accuracy					
2.0 to 20 GHz: ±140 MHz	14.	MI = 3 GHz	2.66 (111)		• • • • • • •
		$M_2 = 6 GH_2$	5.86 GHz		3.14 (311)
		M3 = 10 GHz	9.86 GHz		6.14 GHZ 10.14 GHZ
		M4 - 14 GH2	13.86 GHz		H.H.GH.
		M5 = 18 GHz	37.66 GHz		
2.0 to 7 GHz: ±45 MHz	15.	$M1 = 3 GH_2$	2.955 GHz		
		M2 = 0 GHz	5.955 GHz		3.045 GHZ
7 to 13.5 GHz: ±58 MHz		$M1 \mapsto 8 G11_2$	7.942 G112		5.045 CH17 5.058 CH12
13.5 to 20 GHz: ±63 MHz		$M_2 = 12 GH_2$	11.942 GHz		2.058 GHZ
του το και χητης - που ΜΠΙΥ		MI == 15 GHz	14.937 (117)		5.063 CH1/
		M2 - 18 (3H)	17.937 GHz		8/063/GHz
4, Output Amplitude		<u> </u>			
ower Variations at Max. Power:	6.	1.0 to 7.0 GHz @ +10 dBm	-+10 dBm	-+	-11.4 dBm

Table 4-16,	Performance	Test	Record	(1)	181
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SPECIFICATIONS TESTED	Stop	TEST Conditions	Lower Limit	Moasured Vatuo	Uppør Limit
Power Variations at Max Power: (Cont'd)	7.	7.0 to 13.5 GHz ④ +10 dBm 13.5 to 18.6 GHz ⑥ +10 dBm 13.5 to 20 GHz ⑥ +8 dBm 2.0 to 18.6 GHz ⑥ +10 dBm 2.0 to 18.6 GHz ⑥ +8 dBm	+ 10 dBm + 10 dBm + 8 dBm + 10 dBm + 10 dBm + 8 dBm		+11.4 dBm +11.6 dBm +9.6 dBm +11.8 dBm +5.8 dBm
Option (0)2:	6. 7.	2.0 to 7.0 GHz @ +8.5 dBm 7.0 to 13.5 GHz @ +8 dBm 13.5 to 18.6 GHz @ +7 dBm 13.5 to 20 GHz @ +5 dBm 2.0 to 18.6 GHz @ +7 dBm 2.0 to 20 GHz @ +5 dBm	+8.5 dBm +8 dBm +7 dBm +5 dBm +7 dBm +5 dBm +5 dBm		+9.9 dBm +9.4 dBm +8.6 dBm +6.6 dBm +8.8 dBm +6.8 dBm
Power Level Accuracy 2.0 to 7.0 GHz	9, 10, 11,	Power = ± 10 dBm = ± 9 dBm = ± 8 dBm = ± 7 dBm = ± 5 dBm = ± 5 dBm = ± 45 dBm = ± 44 dBm = ± 3 dBm = ± 2 dBm = ± 1 dBm = ± 1 dBm = -1 dBm = -3 dBm = -3 dBm = -5 dBm	+8.7 dBm +7.7 dBm +6.7 dBm +6.7 dBm +4.7 dBm +3.7 dBm +2.7 dBm +1.7 dBm +0.7 dBm -0.3 dBm -1.3 dBm -2.3 dBm -3.3 dBm -5.3 dBm -6.3 dBm		+11.3 dBm +10.3 dBm +9.3 dBm +8.3 dBm +7.3 dBm +6.3 dBm +6.3 dBm +5.3 dBm +4.3 dBm +4.3 dBm +1.3 dBm +0.3 dBm -0.7 dBm -1.7 dBm -2.7 dBm -3.7 dBm
7.0 to 3.5 G]];	9, 10, 11,	Power == +10 dBm == +9 dBm == +8 dBm == +7 dBm == +6 dBm == +5 dBm == +4 dBm == +3 dBm == +3 dBm == +1 dBm == -1 dBm == -3 dBm == -4 dBm == -5 dBm	+8.7 dBm +7.7 dBm +6.7 dBm +5.7 dBm +3.7 dBm +3.7 dBm +2.7 dBm +1.7 dBr +1.7 dBr -0.3 dBm -1.3 dBm -3.3 dBm -4.3 dBm -5.3 dBm -6.3 dBm		+11.3 dBm +10.3 dBm +9.3 dBm +8.3 dBm +7.3 dBm +7.3 dBm +6.3 dBm +5.3 dBm +4.3 dBm +4.3 dBm +1.3 dBm +0.3 dBm -0.7 dBm -1.7 dBm -2.7 dBm -3.7 dBm
13.5 to 18.6 CF37	9), 10,	Power = +10 dBm ∞ +9 dBm	+8.6 dBm +7.6 dBm		+114 dBm +104 dBm

Table 4-16. Performance Test Record (2 of 8)

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SPECIFICATIONS TESTED Limits	Stap	TEST Conditions	Lower Limit	Menaured Volue	Uppar Limit
13.5 to 18.6 GHz (Cont'd)	11.	- +8 dBm - +7 dBm - +7 dBm - +6 dBm - +5 dBm - +3 dBm - +3 dBm - +2 dBm - +1 dBm 1 dBm 2 dBm 3 dBm 3 dBm 5 dBm	+6 5 dBm +5 5 dBm +4.c dBm +3.6 dBm +2.6 dBm +1.6 dBm +0.6 dBm -0.4 dBm -1.4 dBm -2.4 dBm -3.4 dBm -5.4 dBm -6.4 dBm		+9.4 dlm +8.4 dlm +7.4 dlm +6.4 dlm +5.4 dlm +4.4 dlm +3.4 dlm +2.4 dlm +1.4 dlm +0.6 dlm -1.6 dlm -2.6 dlm -3.6 dlm
13.5 to 20 CJ1}z	9, 10, 11,	Power = 4.8 dBm = 4.7 dBm = 4.6 dBm = 4.6 dBm = 4.4 dBm = 4.3 dBm = 4.3 dBm = 4.2 dBm = 4.4 dBm = -1 dBm = -2 dBm = -3 dBm = -5 dBm	+ 6.6 dBm + 5.6 dBm + 4.6 dBm + 3.6 dBm + 2.6 dBm + 1.6 dBm + 1.6 dBm - 0.4 dBm - 1.4 dBm - 2.4 dBm - 3.4 dBm - 5.4 dBm - 6.4 dBm		+9.4 dBm +8.4 dBm +7.4 dBm +6.4 dBm +5.4 dBm +3.4 dBm +3.4 dBm +1.4 dBm +1.4 dBm -0.6 dBm -1.6 dBm -3.6 dBm
2.0 to 18.6 CD17	9, 10, 11	Power = +10 dBm = +0 dBm = +8 dBm = +8 dBm = +7 dBm = +6 dBm = +6 dBm = +4 dBm = +3 dBm = +4 dBm = -1 dBm = -2 dBm = -3 dBm = -5 dBm	+8.5 dBm +7.5 dBm +6.5 dBm +6.5 dBm +5.5 dBm +4.5 dBm +1.5 dBm +0.5 dBm -0.5 dBm -1.5 dBm -1.5 dBm -2.5 dBm -3.5 dBm -3.5 dBm -5.5 dBm -6.5 dBm		+11.5 dBm +10.5 dBm +9.5 dBm +8.5 dBm +7.5 dBm +6.5 dBm +5.5 dBm +4.5 dBm +4.5 dBm +1.5 dBm +1.5 dBm +0.5 dBm -0.5 dBm -1.5 dBm -2.5 dBm -3.5 dBm
2.0 to 20 Cillz	ч. (d),	Power == +6 dlim == +7 dlim	465 dBm 45.5 dBm		49.5 dBm 48.5 dBm

Table 4-16. Performance Test Record (3 of 8)

4-32

SPECIFICATIONS TESTED Limits	Stop	TEST Conditions	Lower Limit	Monauroit Voluo	Uppor Limit
2.0 to 20 OHz (Cont'd)	11.	- 46 dBm - 45 dBm - 43 dBm - 43 dBm - 43 dBm - 41 dBm - 0 dBm 1 dBm 2 dBm 3 dBm 5 dBm	+4.5 dlm +3.5 dlm +2.5 dlm +1.5 dlm -0.5 dlm -0.5 dlm -1.5 dlm -2.5 dlm -3.5 dlm -4.5 dlm -5.5 dlm -5.5 dlm		+7.5 dBm +6.5 dBm +5.5 dBm +4.5 dBm +3.5 dBm +1.5 dBm +0.5 dBm -2.5 dBm -2.5 dBm -3.5 dBm
Option (802: 2.0 to 7.0 Cilly	9. 0. 1.	Power = +8.5 dBm = +7.5 dBm = +6.5 dBm = +5.5 dBm = +4.5 dBm = +4.5 dBm = +2.5 dBm = +1.5 dBm = -0.5 dBm = -2.5 dBm = -4.5 dBm = -4.5 dBm = -5 dBm	+7 dBm +6 dBm +5 dBm +3 dBm +3 dBm +2 dBm +1 dBm -1 dBm -2 dBm -3 dBm -4 dBm -5 dBm -6 dBm		+40 dlim +9 dlim +8 dlim +8 dlim +7 dlim +6 dlim +5 dlim +5 dlim +4 dlim +1 dlim +1 dlim 0 dlim -1 dlim -2 dlim -3 dlim -3 dlim
7.0 io 13.5 Ciji <i>p</i>	9 10. 11.	Power = -+8 dBm = +7 dBm = +6 dBm = +5 dBm = +4 dBm = +3 dBm = +2 dBm = +1 dBm = -1 dBm = -1 dBm = -2 dBm = -3 dBm = -3 dBm = -5 dBm	+0.5 dBm +5.5 dBm +4.5 dBm +4.5 dBm +3.5 dBm +2.5 dBm +1.5 dBm -0.5 dBm -2.5 dBm -3.5 dBm -5.5 dBm -5.5 dBm		4-9.5 (IIIm +8.5 dBm +7.5 dBm +6.5 dBm +5.5 dBm +3.5 dBm +3.5 dBm +2.5 dBm +1.5 dBm +0.5 dBm +0.5 dBm -0.5 dBm -1.5 a, a -2.5 dBm -3.5 adm
13.5 to 18.6 (3)17	9, 10, 11,	Power == 4-7 dBm == 4-6 dBm == 4-5 dBm	+5.4 dBm +4.4 dBm +3.4 dBm		48.6 dBm 47.6 dBm 46.6 dBm

Table 4+16. Performance Test Record (4 of 8)

SPECIFICATIONS TESTED	Stop	TEST Conditions	Lowar Limit	Monsurad Value	Upper Limit
13.5 to 18.6 (Confd)		+4 dBm +3 dBm +2 dBm +1 dBm +1 dBm 1 dBm 2 dBm 3 dBm 3 dBm 5 dBm	+2.4 dBm +1.4 dBm +0.4 dBm -0.6 dBm -1.6 dBm -2.6 dBm -3.6 dBm -5.6 dBm -5.6 dBm		+56 dBm +4.6 dBm +3.6 dBm +2.6 dBm +1.6 dBm +0.6 dBm -0.4 dBm -1.4 dBm -2.4 dBm -3.4 dBm
13.5 10 20 4112	9. 10. 11.	Power = +5 dlim = +4 dlim = +3 dlim = +2 dlim = +1 dlim = 0 dlim = -1 dlim = -2 dlim = -3 dlim = -5 dlim	4-3.4 dBm +2.4 dBm +1.4 dBm +0.4 dBm -0.6 dBm -1.6 dBm -2.6 dBm -3.6 dBm -5.6 dBm -6.6 dBm		+6.6 dBm +5.6 dBm +4.6 dBm +5.6 dBm +2.6 dBm +1.6 dBm +0.6 dBm -0.4 dBm -1.4 dBm -2.4 dBm -3.4 dBm
2.0 to 18.6 Citty	9. 10. 11.	Power = 4-7 dBm = 4-6 dBm = 4-5 dPm = 4-3 dBm = 4-2 dBm = 4-1 dBm = -1 dBm = -2 dBm = -3 dBm = -5 dBm	+5.3 dBm +3.3 dBm +3.3 dBm +2.3 dBm +2.3 dBm +1.3 dBm +0.3 dBm -0.7 dBm -1.7 dBm -2.7 dBm -3.7 dBm -5.7 dBm -5.7 dBm -6.7 dBm		+8.7 dBm +7.7 dBm +6.7 dBm +5.7 dBm +4.7 dBm +4.7 dBm +2.7 dBm +1.7 dBm +0.7 dBm -0.3 dBm -1.3 dBm -3.3 dBm
2.0 to 20 (3)17	9. 10. 11.	Power = +5 dBm = +4 dBm = +3 dBm = +2 dBm = +1 dBm = 0 dBm = -1 dBm = -2 dBm = -3 dBm = -5 dBm	+3.3 dBm +2.3 dBm +1.3 dBm +0.3 dBm -0.7 dBm -1.7 dBm -2.7 dBm -3.7 dBm -4.7 dBm -5.7 dBm -5.7 dBm		+6.7 dBm +5.7 dBm +4.7 dBm +3.7 dBm +2.7 dBm +2.7 dBm +1.7 dBm +0.7 dBm -0.3 dBm -1.3 dBm -2.3 dBm -3 3 dBm

Table 4-16. Performance Test Record (5 of 8)

S /ECIFICATIONS TESTED Limits					Upper Limit
Power Sweep 2.0 to 7.0 GHz 7.0 to 13.5 GHz 13.5 to 18.6 GHz 13.5 to 20 GHz 2.0 to 18.6 GHz 2.0 to 20 GHz	12. 13.	Power Level = -5 dllm	+10 dBm +10 dBm +10 dBm + 8 dBm +10 dBm + 8 dBm		
Option 002 2.0 to 7.0 GHz 7.0 to 13.5 GHz 13.5 to 18.6 GHz 13.5 to 20 GHz 2.0 to 18.6 GHz 2.0 to 20 GHz	12. 13.	Power Level =5 dBm	+8.5 dBm +8 dBm +7 dBm +5 dBm +7 dBm +7 dBm +5 dBm		
Power Meter Leveled <±0.2 dB	20.			• •	<±0.2 dB
Crystal Det Leveled <±0.2 dB	24.				<±0.2 dB
 4-15. Frequency Stability 10% Line Voltage Change: Band 1, 6 GH2: <±50 kHz Band 2, 12 GHz: <±100 kHz Band 3, 18 GHz: <±150 kHz 	3. 4. 5.	Low line frequency change High line frequency change Low line frequency change High line frequency change Low line frequency change High line frequency change		· · · · · · · · · · · · · · · · · · ·	<±50 kHz <±50 kHz <±100 kHz <±100 kHz <±150 kHz <±150 kHz
^w ime (10 minutes): Band 1, 6 (1)12: ≤±100 kHz Band 2, 12 GHz: ≤±200 kHz Band 3, 18 GHz: ≤±300 kHz	7. B.	Maximum deviation in 10 minutes Maximum deviation in 10 minutes Maximum deviation in 10 minutes			≤±100 kHz ≤±200 kHz ≤±200 kHz
10 dB Power Change: Band 1, 6 GHz: ≤±200 kHz Band 2, 12 GHz: ≤±400 kHz Band 3, 18 GHz: ≤±600 kHz	10. 11.	Frequency change with power Frequency change with power Frequency change with power			≤±200 k117 ≤±400 k117 ≤±600 k117
3:1 Load SWR: Band 1, 6 GH7: ≤±100 kHz Band 2, 12 GH7: ≤±200 kHz Band 3, 18 GH7: ≤±300 kHz	15. 16.	3:1 SWR 3:1 SWR 3:1 SWR		· · ·	≤±100 k117 ≤±200 k117 ≤±300 k117

Table 4-16. Performance Test Record (6 of 8)

Model 83590A

SPECIFICATIONS TESTED Limits	Stop	TEST Conditions	Lower Limi+	Monsurad Valuo	Uppor Limi+
4-16, Residual FM 2.0 to 7 CH22: <5 kH2	17.	CW frequency = 6 GHz			<5 kHz
7.0 to 13.5 GHz: <7 kHz 13.5 to 20 GHz: <9 kHz	18.	CW frequency = 12 GHz CW frequency = 18 GHz			<7 kHz <9 kHz
4-17. Sputious Signate					
Harmonic: 2.0 to 7 GHz: >-25 dB 7 to 13.5 GHz: >-25 dB 13.5 to 20 GHz: >-25 dB Non-harmonic:	3.	Measure relative to carrier	>-25 dB >-25 dB >-25 dB >-25 dB		
2.0 to 7 CHz: >-50 dB 7 to 13.5 GHz: >-50 dB 13.5 to 20 GHz: >-50 dB			>-50 dB >-50 dB >-50 dB		
4-18, Output SWR					
Standard: <1.9 Option 002: <2.1	5.	Range: 2 to 18 GH7			≺1.9 ≺2.1
4-10, Residuel AM		······································			
6 GHz: ≥ -50 dB 12 GHz: ≥ -50 dB 18 GHz: ≥ -50 dB 6 GHz: ≥ -50 dB 12 GHz: ≥ -50 dB 13 GHz: ≥ -50 dB 14 GHz: ≥ -50 dB 15 GHz: ≥ -50 dB 16 GHz: ≥ -50 dB 18 GHz: ≥ -50 dB	5. 6,	Measure relative to carrier Measure relative to carrier			≥-50 dB ≥-50 dB ≥-50 dB ≥-50 dB ≥-50 dB ≥-50 dB ≥-50 dB
4-20, External FM					
Direct Coupled: DC to 100 Hz: ≥±12 MHz Cross Over Coupled: DC to 100 Hz: ≥±75 MHz Direct/Cross Over Coupling	1. 3. 4.	A3S1. Close switch 5, open 6 A3S1: Close switch 6	≥±12 MH7 ≥±75 MH2		
100 Hz to 1 MHz: ≥±7 MHz 1 to 2 MHz: ≥±5 MHz 2 to 10 MHz: ≥±1 MHz	9, 10,		≥±7 MH2 ≥±5 MH2		
	н.	A3S1: Change switch 6 from previous setting	≥±1 MH/ ≥±7 MH/ ≥±5 MH/ ≥±1 MH/		
4-21. AM On/Olf Ratio Squere-Wave Symmetry					
On/Off Ratio: >30 dB below specified maximum leveled power	1.	CW frequency = 4 GHz Power = +10 dBm			
Symmetry of ON/OFF time: 40/60	3. 4.		>30 dH 40%		60%

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Table 4-16. Performance Test Record (7 of 8)

Model 83590A

Performance Tests

SPECIFICATIONS TESTED Limits		Step	TEST Conditions			Lowar Limit	Monsurod Valuo	Upper Limit	
4-22. Step Atter (Option 002) (Referenced In 2.0 to 12.4 (})	əm 0 dB)	l. 2.	Power -	ency = 4.0 (F4.0 dBm Attenuation					
Attn. Step	Accuracy		Ref. Attn. Step	Atin. Error	-+	Daviation from 0 raf,			
10 dB	≤±0.6 dB	4.	70 - 60		1,			T	
20 dB	≤±0.7 dB	7.	70 - 50			E			5±0.6 dB
30 dB	≤±0.9 dB	B.	70 - 40						≦±0.7dB
40 413	≤±1.8 dB		70 - 30		+				≤±0.9 dB ≤±1.8 dB
50 dB	≤±2.0 dB		71) - 20		4				≤∓50 dB
60 JB	:조±2,2 dB		70 - 10		+] [≤±2.2 dB
70 dB	≤±2.3 dB		70 - 0		+				≤∓53 (B
12.4 to 18 GH;		9.	Power = +	ncy = 15 G 4.0 dBm Attenuation		70 dB			
Attn. Step	Ассигасу		Ref. Attn. Step	Attn. Error	+	Deviation from 0 ref.			
10 dB	≤±0.7 JB		70 - 60		+				
20 113	≤±0.9 dB		70 - 50						≤±0.7 dB
30 dB	≤±1.2 dB		70 - 40		+				≤±0.9 dB
40-013	≤±2.0 dB		70 - 30		+				≦±1.2 dB
50 dB	≤±2.3 dB		70 - 20		T +				≤±2.0 dB
60 dB	≤±2.5 dB		70 - 10		4				≤±2.3 dB
70 dB	≤±2.6 JB		70 - 0		4				≾±2.5 dB ≤±2.8 dB
10 to 20 GHz		10,	CW frequer Power = +-	4.0 dBm			·		
A		-	Reference /						
Attn. Step	Accuracy		Btep	Attn. Error	+	Deviation from 0 ref.			
10 dB	≤±0.9 dB		70 - 60		+				
20 dB	≦±1.5 dB		70 - 50		+		1		≤±0.9 d]] ≤±1.6 d]]
30 dB	52.5 dB		70 - 40		+				≤±1.5 dB ≤±2 5 dB
40 dB	≤±3.0 dB		70 - 30		+				≤#30 dB
ALC 111	≤±3.2 dB		79 - 20		+				≥#30.0B
50 AB			70 - 10		+				
60 dB	≤±3.3 dB		10 - 10 I		- T I	I			
	5±3.3 dB ≤±3.5 dB	-	70 - 10 70 - 0		+				≤#3.3 dB

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Table 4-16. Performance Test Record (8 of 8)

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ADJUSTMENTS

1.

Model 83590A

Adjustments

SECTION V ADJUSTMENTS

St. 255 14 15 154 11 23

5-1. INTRODUCTION

5-2. This section provides adjustment procedures for the Model 83590A RF Plug-in. These procedures should not be performed as roatine maintenance but should be used (1) after replacement of a part or component, or (2) when performance tests show that the specifications of Table 1-1 cannot be met. Table 5-1 lists all of the adjustments by reference designation, adjustment name, adjustment paragraph, and description. Each procedure includes a test setup illustration and one or more adjustment location illustrations. Table 5-2 lists the adjustment included in this section.

NOTE

Allow the 83590A RF Plug-in and the 8350A Sweep Oscillator to warm up for 30 minutes prior to making any adjustments.

5-3. SAFETY CONSIDERATIONS

5-4. Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition Service and adjustments should be performed only by a skilled person who is aware of the hazard involved.

WARNING

Adjustments in this section are performed with power supplied to the instrument while protective covers are removed There are voltages at points in the instrument which can, if contacted, cause personal injury. Be extremely careful. Adjustments should be performed only by a skilled person who is aware of the hazard involved. Capacitors inside the instrument may still be charged, even if the instrument has been disconnected from its source of supply.

NOTE

Use a non-metallic adjustment tool whenever possible.

6-5. EQUIPMENT REQUIRED

5-6. The equipment required for the adjustment procedures is listed in Section I of this manual. If the test equipment recommended is not available, other equipment may be used if its performance meets the critical specifications listed in the table. The specified equipment required for each adjustment is referenced in each procedure.

5-7, FACTORY-SELECTED COMPONENTS

5-8. Table 5-3 contains a list of factory-selected components that includes the reference disignation, the related adjustment procedure, the allowable range of values, and the basis of selection. Nominal values are given for the factory-selected components, designated by an asterisk (*), on the schematic diagram and in the replacement parts list. HP Part Numbers for selected values are given in Table 5-4.

5-9. RELATED ADJUSTMENTS

5-10. Interactive adjustments are noted in the adjustment procedures. Table 5-5 indicates by paragraph numbers the adjustments that must be performed if an assembly has been repaired or replaced or if an adjustment has been made to an assembly.

5-11. ADJUSTMENT PROCEDURES

5-12. A djustment procedures are given in the proper sequence to allow for interrelated adjustments.

Reference Designation	Adjustmant Nome	Adjustmont Paragraph	Description
A2RI	GAIN	5-24	Sets gain of frequency reference in Bands 1, 2, and 3 (1V/GHz).
A2R4	OFFSET	5-24	Sets offset of frequency reference in Bands 1, 2, and 3 (1 V/GHz).
A3S1	Configuration Switch	5-13	Selects Plug-in code, power-up power level, FM sensitivity, FM modulation coupling, step attenuator Option Code, normal or sequential sweep option, and phase-lock operation.
A4R3	1.141	5-25	Sets power calibration at the high end of the power range (+10 dBm) in Band 1.
A4R5	11.0	5-25	Sets power calibration at the low end of the power range (5 dBm) in Bands 1, 2, and 3,
A4R8	I MD	5-25	Sets power calibration at the middle of the power range (+7-dBm) in Bands 1, 2, and 3.
A4R9	PM	5-27	Sets power meter leveling calibration.
A4R11	GAIN	5-28	Sets gain of ULL Main ALC Amplifier.
A4R47	OFS 1	5-25	Adjusts for zero offset threagh U7-Q6 Log Amplifier circuit.
A4R56	OFS 2	5-25	Adjusts for zero offset through U5 Log Amplifier circuit.
A4R59	OFS 3	5-25	Adjusts for zero offset through US-Q1 Sample and Hold circuit.
A4R67	OFS 4	5-25	Adjusts for zero offset through UEI Main ALC Amplifter,
A5C14	LO	5-30	Adjusts low frequency for best frequency response flatness through U10,
A5R18	EM OPESET	5-30	Adjusts shape of U10 Video Amplifier compensation network response.
A5R19	EM -	5-,10	Sets DC offset of U10 Video Amplifier.
A5R34	BP 1	5-26	Breakpoint that works with SLI (Slope 1) for ALC flatness.
A5R36	BP 2	5+26	Breakpoint that works with SL2 (Slope 2) for ALC flatness.
A5R38	BP 3	5-26	Breakpoint that works with SL3 (Slope 3) for AEC flatness.
A5R40	BP 4	5+26	Breakpoint that works with SL4 (Slope 4) for ALC flatness,
A5R41	SL I	5-26	Slope adjustment for best ALC flatness.
A5R42	SL 2	5-20	Slope adjustment for best ALC flatness.

Table 5-1 Adjustable Components (1 of 4)

Reference Designation	Adjustment Name	Adjustment Paragraph	Description
A5R43	SL 3	5-26	Slope adjustment for hest ALC flatness,
A5R44	SL 4	5-20	Slope adjustment for best ALC flatness.
A5R48	SLP	5-26	Sets overall slope of internal leveling ALC.
A5R50	PWSP	5.29	Sets range for power sweep.
A5R75	HI	5.30	Works in conjunction with C14 to set frequency response flatness of FM Coil.
A6R12	с	5-20, 5-21	Adjusts YTM SRD bias to peak power in all bands at fow power settings.
A6R16	TV GAIN	5-15	Sets the gain of U6 Tune Voltage buffer amplifier.
A6R21	DAC CAL	5-15	Adjusts the gain of US Variable Gain Amplifier during all single band sweeps.
A6R24	B3	5-15, 5-23	Adjusts the gain of U5 Variable Gain Amplifier in Band 3 during sequential sweeps.
A6R26	112	5-15, 5-23	Adjusts the gain of US Variable Gain Amplither in Band 2 during sequential sweeps.
A6R28	BI	5-15, 5-23	Adjusts the gain of US Variable Gain Amplifier in Band 1 during sequential sweeps.
A6R.34	10V OFFSET	5-15	Offsets the 10 volt reference voltage to U15.
A6R37	SP	5-15	Offsets input voltage to U24A forward sweep bandswitch amplifier,
A6R63	3HL	5-20, 5-21	Adjusts balance of SRD Bias circuit.
A6R68	211	5-20, 5-21	Adjusts YTM SRD bias at high power, high frequency end of Band 2.
A6R69	311	5-20, 5-21	Adjuity () TM SRD bias at high power, high frequency end of Band 3,
A6R73	2L	5-20, 5-21	Adjusts YTM SRD blas at high power, low frequency end of Band 2.
A6R74	3L	5-20, 5-21	Adjusts YTM SRD bias at high power, low frequency end of Band 3.
A6R78	Т	5-20, 5-21	Adjusts YTM SRD bias at an intermediate power level for Bands 2 and 3.
A7R10	SGL HI	5-22	Adjusts offset of YTM delay compensation signal at the high end of single band sweeps.

Table 5-1. Adjustable Components (2 of 4)

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Reference Designation	Adjustment Name	Adjustment Paragraph	Description
A7R12	SGL LO	5-22	Adjusts offset of YTM delay compensation signal at the low end of single hand sweeps.
A7R18	X.	5-16	Adjusts offset of U20 delay compensation amplifier to minimize the difference between CW and ΔF ±0 with YTM delay compen- sation circuits.
A7R19	GAIN	5-16	Adjusts the Scaled Voltage Tune DAC input signal to U21 YTM Summing Amplifier.
A7R22	ZRO	5-16	Adjusts supply correction voltage to U21 YTM Summing Amplifier.
A7R24	OFS	5-16	Adjusts Offset DAC input signal to U21 YTM Summing Anaph- fier.
A7R42	SEQ III	5-22	Adjusts offset of YTM delay compensation signal at high end of sequential band sweeps.
A7R43	SEQ LO	5-22	Adjusts offset of YTM delay compensation signal at low end of sequential hand sweeps.
A7R45	SEQ TC	5-22	Adjusts gain of YTM delay compensation signal in sequential band sweeps.
A7R46	SGL TC	5-22	Adjusts gain of YTM delay compensation signal in single band sweeps.
A7R51	BLOFS	5-20	Adjusts offset of U21 Summing Amplifier in single band sweeps.
A7R55	RTC COMP	5-22	Adjusts the pulse width of YTM retrace compensation signal.
A7SI	OFFSET	5-20	Adjusts low end of band YTM to YO tracking at slow sweep speeds.
A752	GAIN	5+20	Adjusts high end of band YTM to YO tracking at slow sweep speeds.
A8R10	BI	5-19	Adjusts YO delay compensation at high frequency end of hand.
A8R12	LO	5-19	Adjusts YO delay compensation at low frequency end of band.
A8R13	7.	5-16, 5-19	Adjusts offset to minimize the difference between CW and ΔF ±0 with YO delay compensation circuits.
A8R19	GAIN	5-16	Adjusts Scaled Voltage Tune DAC input signal to U20'Summing Amplifier.
A8R22	ZRO	5-16	Adjusts supply correction voltage to U20 Summing Amplifier.

Table 5-1. Adjustable Components (3 of 4)

5-4

Roference Designation	Adjustment Name	Adjustment Parograph	Description
A8R24	OFS	5-16	Adjusts Offset DAC input signal to U20 Summing Amplifier.
A8R44	10V	5-14	Sets 10 volt reference voltage source.
A8R55	RTC COMP	5-18	Adjusts the pulse width of the YO retrace compensation signal.
A851	OFFSET	5-17	Adjusts the low end of band YO frequency accuracy.
A852	GAIN	5-17	Adjusts the high end of band YO frequency accuracy.
A13A1R4		none	Factory adjusted.
AHAARH		none	Factory adjusted.
AD4A1R13		none	Factory adjusted.
ADAARIA		none	Factory adjusted.
A14AIR15		none	Factory adjusted.
AI4A1R16		none	Factory adjusted.
A14ATR18		none	Factory adjusted.

Table 5-1, Adjustable Components (4 of 4)

Paragraph	Adjustments	Paragraph	Adjustments
5-13	Configuration Switch A3S1	5-22	YTM Delay Compressition
5-1-4	-10 Volt Reference On A8 YO Driver	5-23	Band Overlan Adjustment
5-15	Sweep Control Adjustments	5-24	Frequency Reference 1V/GHz Output
5-16	YO and YTM DAC Calibration	5-25	ALC Adjustments
5.17	Preliminary Frequency Accuracy	5-26	ALC Internally Leveled Flatness Adjustment
5-18	YO Retrace Compensation	5.27	Power Meter Leveling Calibration
5-19	YO Delay Compensation	5-28	ALC Gain Adjustment
5-20	Slow Speed YTM to YO Tracking	5-29	Power Sweep
5-21	SRD Bias	5-30	FM Driver Adjustments

Table 5-2. Adjustments

Table 5-3. Factory Selected Components

Reference Designator	Adjustment Paragraph	Allowable Renge of Velues	Basis of Selection
A5R31	5-30	200 to 300 Ohms	Selects scaling of current drive of YO FM coil near 100 kHz.
A7K34	none		Selected at factory to correct for frequency nonlinearity in YTM.
A7R35-39	none		
A7R6671	none		
A8R36	none		Selected at factory to correct for 'requency nonlinearity in the YO.
A8R37-39	none		
AI3AIRI	none		Selected at factory to optimize YO band- width, power, and harmonics.
A13A1R2	none		

	TYPE: Fixe	0 to 4						
	WATTAGE: TOLERANC	120	5 at 125° C)	
Value (12)	HP Part Number	C D	Value (L2)	tie Part Number	C D	Value (12)	HP Part Number	
10.0	0757-0346	;	404	0698-0082	7	.1.5K	0757-0199	
11.0	0757-0378	0	511	0757-0416	7	23.78	CO98-3158	
12.1	0757-0379		562	0757-0417	<u> </u>	26.4K	0698-3159	
13.3	0698-3427	0	619	0757-0418	9	28.7K	0698-3449	
14.7	0698-3428		681	0757-0419	0	31.6K	0698-3160	
16,2	0757-0382	6	750	0757-0420	3	34.8K	9757-0123	
17.8	0757 0294	9	825	0757-0421	4	38.3K	0698-3161	
19,6	0698-3429	2	909	0757-0422	5	- 42.2K	0698-3450	
21.5	0698-3430	5	LOK	0757-0280	3	-46.4K	0698-3162	
23.7	0698-3431	h	1.1K	0757-0424	7	= 51.1K	0757-0458	
26.1	0698-3432	7	1.21K	0757-0274	5	56.2K	0757-0459	
28.7	0698-3433	N	1.33K	0757-0317	7	61.9K	0757-0460	
31.6	0757-0180	2	1.47K	0757-1094	9	- 68.1K	075740461	
34.8	0698-3434	9	1.62K	0757-0428		- 75.0K	0757-0462	
38,3	0698-3435	0	1.78K	0757-0278	9	82.5K	0757-0463	
42.2	0757-0316	6	1.96K	0698-0083	8	90.9K	0757-0464	
46.4	0698-4037	0	2.15K	0698-0084	9	100K	075740465	
51.1	0757-0394	0	2.37K	0698-3150	6	110K	0757-0466	
56.2	0757-0395	1	2.61K	0698-0085	0	121K	0757-0467	
61.9	0757-0276	7	2.87K	0698-3151	7	133K	0698-3451	
68.1	0757-0397	3	3.16K	0757-0279	0	147K	0698-3452	
75.0	0757-0398	-4	3.48K	0698-3152	8	162K	0757-0470	
82.5	0757-0399	5	3.83K	0698-3153	9	178K	0698-3243	
90.0	0757-0400	9	4.22K	0698-3154	0	196K	0698-3453	
100	0757-0401	0	4.64K	0698-3155		215K	0698-3454	
110	0757-0402		5.11K	0757-0438	3	2.37K	0698-3266	
121	0757-0403	2	5.62K	0757-0200	7	261K	0698-3455	
133	0698-3437	2	6.19K	0757-0290 0757-0439	5	287K	0698-2456	
147	0698-3438	3	6.81K	0757-0440	4	316K	0698-3457 0698-3458	
162	0757-0405	4	7.50K	0757-0441	8	348K	0698-3459	
178	0698-3439	4	8.25K	0757-0288		383K 422K	0698-3460	
196	0698-3440	8	9.09K 10.0K	0757-0442	9	4228 464K	0698-3260	
215	0698-3441	9	10.0K	0757-0443	ů,	909K	5757 / 17 ° 47 m 5 15 J	
237	0698-3442	4	12.1K	0757-0444	ı ï			
261	0698-3132	0	13.3K	0757-0289	2			
287	0698-3443		13.38	0698-3156	2			
36	0698-3444		14.78 16.2K	0757-0447	4			
348	0698-3445	3	10.2K 17.8K	0698-3136	8			
383 422	0698-3446 0698-3447		17.6K	0698-3157	3			

Table 5-4.	IIP Part Numbers	of Standard	Value Re	placement	Components.
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Assembly Changed or Repaired	Rolated Assomblies (in order of Adjustments)	Perform the Following Paragraph Number
A1/A2 Front Panel	٨2	5-24
A3 Digital Interface	٨3	5-13
A4 ALC	٨4, ٨5	5-25 thru 5-28
A5 FM	A4, A5	5-25 thru 5-30
A6 Sweep Control	A6, A8, A7	5-15 thru 5-23
A7 YTM Driver	A6, A8, A7	5-15 thru 5-23
A8 YO Driver	A6, A8, A7	5-15 thru 5-23
A12 Switched YIG Tuned Multiplier	A6, A8, A7, A2	5-15 thru 5-20, 5,23, 5-24
A13 2.0 – 7,0 GHz Oscillator	A6, A8, A7, A2, A5	5-15 thru 5-20, 5-23, 5-24, 5-30
A14 Power Amplifter	٨4, ٨5	5-25 thru 5-28
A16 Modulator/Coupler	٨4, ٨5	5-25 thru 5-28
AT1 Isolator	Α4, Α5	5-25 thru 5-28
DC2 Directional Coupler	Λ4, Λ5	5+25 thru 5+28

Table 5-5, Related Adjustments

5-13. CONFIGURATION SWITCH A351

REFERENCE:

Performance Test: None. Service Sheet: A3

DESCRIPTION:

Switch A3S1 is set at the factory for a combination of operating modes. (Refer to Table 5-6.) Other operating modes are selected by setting the eight switches on A3S1.

PROCEDURE:

NOTE

All adjustment procedures assume that A3S1 is set to the factory setting unless otherwice specified in the test. If other procedures are to be performed, set A3S1 to the factory setting until the procedures are completed, then set A3S1 to the desired operating mode before putting the instrument back in service.

- 1. Refer to Table 5-6 and determine if factory selected mode set at A3S1 is correct for your application.
- 2. Set configuration switch A3S1 (Figure 5-1) for the desired operating mode.
- 3. Press INSTR PRESET to set the instrument into the operating mode selected by the configuration switch.

NOTE

INSTR PRESET must be pressed after the configuration switch positions are modified in order to set the instrument immediately to the desired operating mode set by the configuration switch.

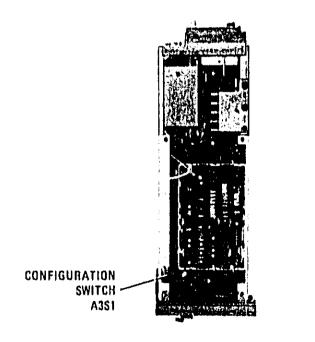


Figure 5-1. Configuration Switch A3S1 Location

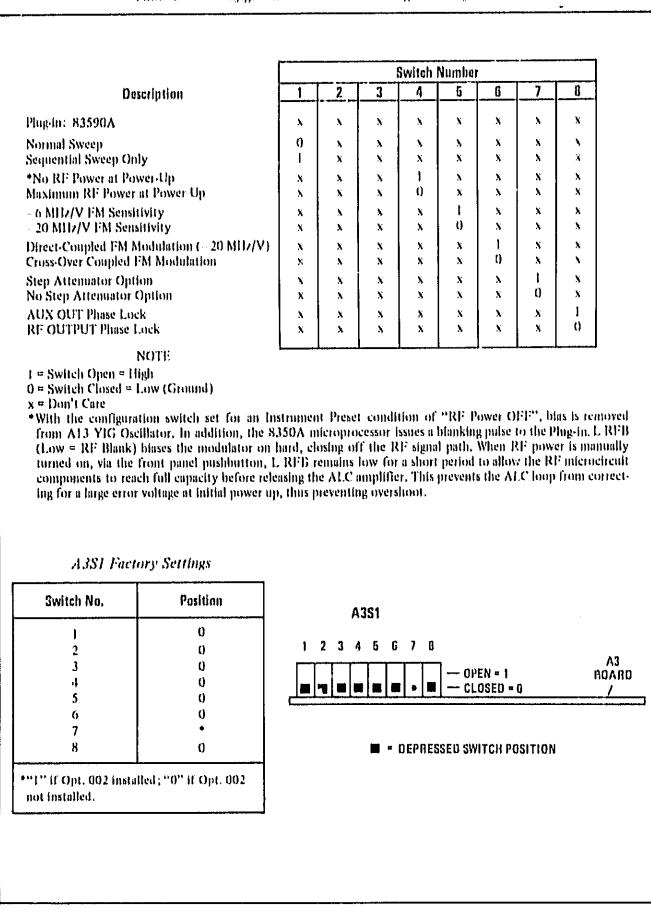


Table 5-6. Configuration Switch on A3 Digital Im space Board

5-10

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ADJUSTMENTS

5-14, -10 VOLT REFERENCE ON A8 YO DRIVER

REFERENCE

Performance Test: Paragraph 4-13 Service Sheet: A8

DESCRIPTION:

The -10 volt reference voltage source on the A8 YO Driver hoard is used as a reference voltage for the DACs on the A4 ALC, A6 Sweep Control, the A7 YTM Driver, and the A8 YO Driver hoards. The -10 volt reference output voltage is set by the A8R44 -10V adjustment while monitoring A8TP12.

A8

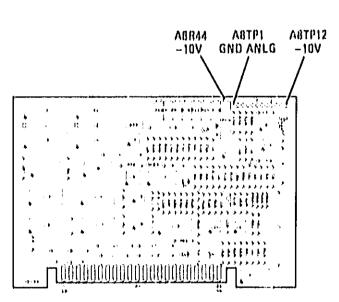


Figure 5-2. -10V Reference Adjustment Location

EQUIPMENT:

Digital Voltmeter	HP 3456A
Sweep Oscillator.	HP 8350A

PROCEDURE:

1. Connect the DVM to A8TP12 (-10V) with reference to A8TP1 (GND ANLG).

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2. Adjust A8R44 -10V for a DVM reading of -10 ± 0.001 Vdc. Refer to Figure 5-2 for -10 volt reference adjustment location.

5-15. SWEEP CONTROL ADJUSTMENTS

REFERENCE:

Performance Test: Paragraph 4-13 Service Sheet: A6

DESCRIPTION:

With the tuning voltage (VTUNE) set to $\pm 10V$ (CW frequency of 20 GHz), the TV Buffer is set for unity gain, and the DAC CAL adjustment is set to equalize the Bandswitch Comparator DAC and TV Buffer inputs to the Variable Gain Amplifier (DAC CAL is set for 0V at A6TP4). The $\pm 10V$ OFFSET adjustment is then set to offset the Variable Gain Amplifier output by $\pm 10V$. The gain of the Variable Gain Amplifier is then calibrated at the low end of each frequency band. The 83590A is then swept across its full frequency range and the Switch Point adjust A6R37 (SP) is adjusted to set the bandwitch points.

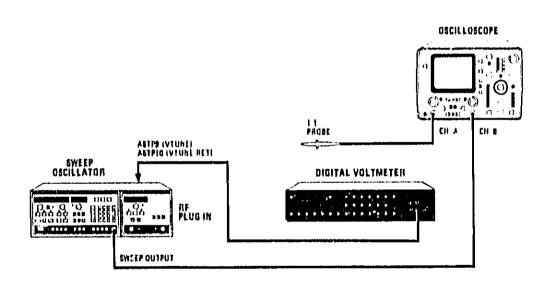


Figure 5-3. Sweep Control Adjustments Test Setup

EQUIPMENT:

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Digital Voltmeter	HP 3456A
Oscilloscope	HP 1740A
1:1 Probe	
Sweep Oscillator.	HP 8350A

Model 83590A

Adjustments

ADJUSTMENTS

5-15, SWEEP CONTROL ADJUSTMENTS (Cont'd)

PROCEDURE:

- 1. Ensure that A3S1 switch position 1 is in the OPEN (up) position. Refer to Adjustment Paragraph 5-13 for instructions on setting A3S1.
- Set up the equipment as shown in Figure 5-3 with the DVM connected to A6TP9 (VTUNE) and with the reference probe connected to A6TP10 (VTUNE RET). Do not connect the Oscilloscope probe yet. Allow the instrument to warm up for 1 hour.
- 2. On the 8350A, press INSTR PRESET 2 0 GHz VERNIER .
- 4. Adjust the 8350A FRFQ VERNIER for a DVM reading of 10 \pm 0.001 Vdc.

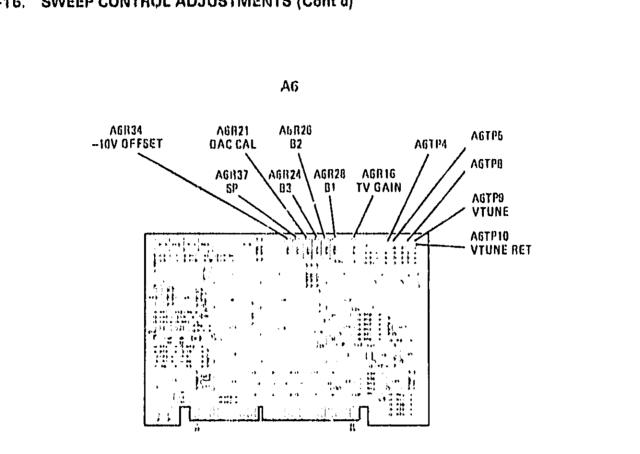
NOTE

The following voltage measurement procedures on the AG Sweep Control board are made with the DVM reference probe connected to ABTP1 (which is electrically the same as motherboard ground).

- 5. Connect the DVM to A6TP5 and adjust A6R16 (TV GAIN) for a DVM reading of -10 ± 0.001 Vdc. Refer to Figure 5-4 for sweep control adjustment locations.
- 6. Connect the DVM to A6TP4 and adjust A6R21 (DAC CAL) for a DVM reading of 0 ± 0,001 Vde.
- 7. Connect the DVM to A6TP8 (BVTUNE) and adjust A6R34 for a DVM reading of -10 ± 0.001 Vde.
- 8. On the 8350A, press CW 1 3 . 5 GHz .
- Connect the DVM to A6TP5 and adjust the 8350A FREQ VERNIER control for a DVM reading of -6.38889 ± 0.00005 Vdc.
- 10. Connect the DVM to A6TP8 and adjust A6R24 (B3) for a DVM reading of 0 ± 0.001 Vde.
- 11. On the 8350A, press CW 7 GHz.

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- 12. Connect the DVM to A6TP5 and adjust the 8350A FREQ VERNIER control for a DVM readin; of -2.77778 ± 0.00005 Vdc.
- 13. Connect the DVM to A6TP8 and adjust A6R26 (B2) for a DVM reading of 0.001 Vde.
- 14. On the 8350A, press CW 2 , 0 GHz .
- 15. Connect the DVM to A6TP5 and adjust the 8350A FREQ VERNIER control for a DVM reading of 0±0,00005 Vde.





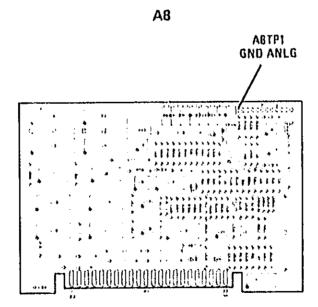


Figure 5-4. Sweep Control Adjustment Locations

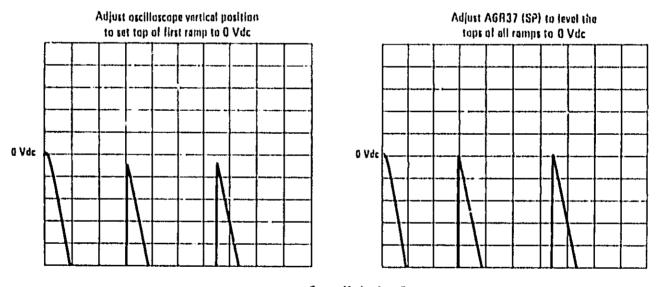
ADJUSTMENTS

5-15. SWEEP CONTROL ADJUSTMENTS (Cont'd)

- 16. Connect the DVM to A6TP8 and adjust A6R28 (B1) for a DVM reading of 0 ± 0.001 Vdc.
- 17. On the 8350A, press INSTR PRESET .
- 18. Connect the Oscilloscope probe to A6TP8. Set the Oscilloscope settings as follows:

Mode	. A vs B
Vertical Sensitivity	0.5 V/DIV
Coupling	DC

19. Adjust the oscilloscope vertical position control to set the top of the first full 0 to -10 volt sweep ramp on the centerline as shown in Figure 5-5.



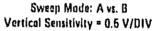


Figure 5-5. Sweep Control Adjustment Waveforms

- 20. Adjust A6R37 (SP) to bring the tops of the remaining 0 to -10 volt sweep ramps to the center graticule as shown in Figure 5-5.
- 21. If A3S1 switch position 1 was modified in step 1 of this procedure, reset it to the closed (down) position as described in Adjustment Paragraph 5-13 before continuing with the adjustment procedures.

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5-16. YO AND YTM DAC CALIBRATION

REFERENCE:

Performance Test: Paragraph 4-13 Service Sheet: A7 and A8

DESCRIPTION:

The 8350A is set for a CW frequency of 20 GHz and then fine-tuned for a tuning voltage (VTUNE) of $\pm 10V$. The Hex Data Write feature of the 8350A is used to load each DAC with either all ones or all zeros. The A8 YO Driver is adjusted first. With both the Scaled Voltage Tune and Offset DACs loaded with all zeros, the YO Collector output is monitored and the $\pm 20V$ Tracking Amplifier ZRO adjustment is set. Each DAC is then loaded with all ones and the respective Offset or Gain adjustment is set. The A7 YTM Driver is adjusted the same way. The 8350A is then set into the Swept CW mode and the Delay Compensation circuits on both A7 and A8 are adjusted for a 0V output.

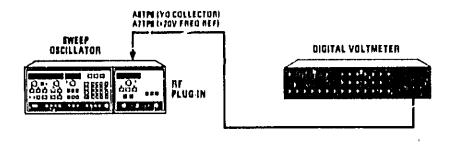


Figure 5-6. YO and YTM DAC Calibration Test Setup

EQUIPMENT:

Digital Voltmeter	HP 3456A
	HP 8350A

PROCEDURE:

- 1. Connect the equipment as shown in Figure 5-6 with the DVM connected to A6TP9 (VTUNE) and the reference probe connected to A6TP10 (VTUNE RET). Refer to Figure 5-7 for test point and diastment locations. Allow the RF Plug-in to warm up for 1 hour.
- 2. On the 8350A, press INSTR PRESET CW 2 0 GHz.
- 3. Adjust the 8350A FREQ VERNIER for a DVM reading of 10 ± 0.001 Vdc.
- 4. Float the ground on the DVM. Connect the DVM to A8TP6 (YO COLLECTOR) with the reference probe connected to A7TP8 (+20V FRE/_c REF).

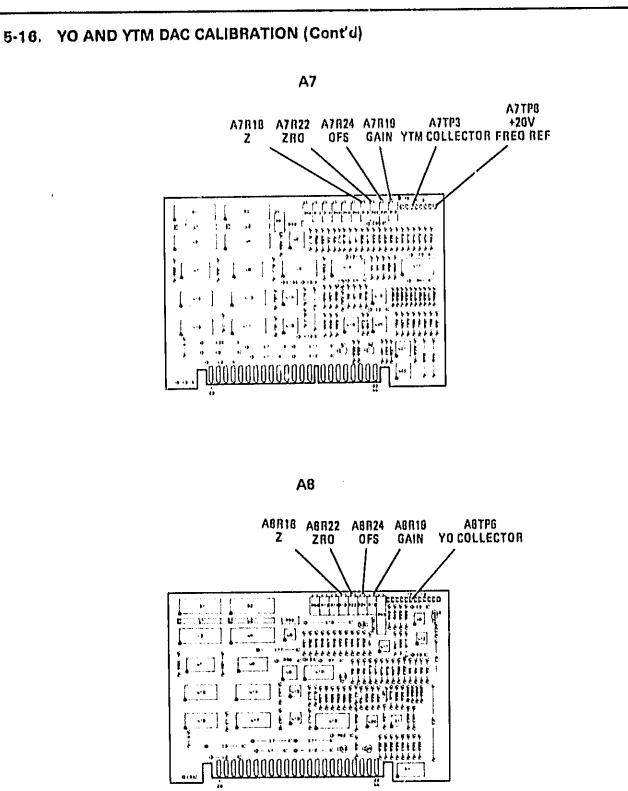


Figure 5-7. YO and YTM DAC Calibration Adjustment Locations

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ADJUSTMENTS

5-16, YO AND YTM DAC CALIBRATION (Cont'd)

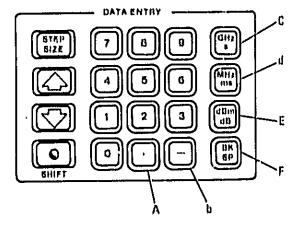


Figure 5-8. Front Panel Hexadecimal Entry Keys

5. Use the Hex Data Write feature to write all zeros to both DACs on the A8 YO Driver:

SHIFT 0 0	Enters hex data command
2 GHz 8 0	Address location 2C80
M2	Hex Data Write
0 0	Enter hex data 00
🛖 0 0	Increment address to 2C81 and write 00
(0 0	Increment address to 2C82 and write 00
📥 0 0	Increment address to 2C83 and write 00

- 6. Adjust A8R22 (ZRO) for a DVM reading of -7.000 ± 0.001 Vdc.
- 7. Use the Hex Data Write feature to write zeros to the Scaled Voltage Tune DAC and ones to the Offset DAC as follows:

**	Decrement address to 2C80
0 BKSP	Enter hex data 0F
🛖 0 F	Increment address to 2C81 and write 017
🛖 0 F	Increment address to 2C82 and write 0F
🛖 0 F	Increment address to 2C83 and write 0F

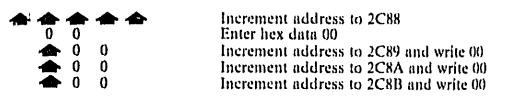
- 8. Adjust A8R24 (OFS) for a DVM reading of -20.000 ± 0.001 Vdc.
- 9. Use the Hex Data Write feature to write ones to the Scaled Voltage Tune DAC and zeros to the Offset DAC as follows:

-	-	₩.	Decrement address to 2C80
F	0		Enter hex data F0
	F	0	Increment address to 2C81 and write F0
- 1	F	0	Increment address to 2C82 and write F0
· 📥	F	0	Increment address to 2C83 and write F0

ADJUSTMENTS

5-16. YO AND YTM DAC CALIBRATION (Cont'd)

- 10. Adjust A8R19 (GAIN) for a DVM reading of -26.500 ± 0.001 Vdc.
- 11. Use the Hex Data Write feature to write all zeros to both DACs on the A7 YTM Driver as follows:



- 12. Connect the DVM to A7TP3 (YTM COLLECTOR) with the reference probe still at A7TP8 (+20V FREQ REF). Adjust A7R22 (ZRO) for a DVM reading of -3.000 ± 0.001 Vdc.
- 13. Use the Hex Data Write feature to write zeros to the Scaled Voltage Tune DAC and ones to the Offset DAC as follows:

\bullet	-	-	Decrement address to 2C88
0	BK	SP	Enter hex data 0F
	0	F	Increment address to 2C89 and write 0F
	0	F	Increment address to 2C8A and write 0F
	0	F	Increment address to 2C8B and write 0F

- 14. Adjust A7R24 (OFS) for a DVM reading of -19.500 ± 0.001 Vdc.
- 15. Use the Hex Data Write feature to write ones to the Scaled Voltage Tune DAC and zeros to the Offset DAC as follows:

BKSP 0	Decrement address to 2C88 Enter hex data F0
🛧 F 0	Increment address to 2C89 and write F0
🛖 F 0	Increment address to 2C8A and write F0
📥 F 0	Increment address to 2C8B and write F0

- 16. Adjust A7R19 (GAIN) for a DVM reading of -9.500 ± 0.001 Vdc.
- 17. On the 8350A, press INSTR PRESET SHIFT CW.
- 18. Connect the DVM to A7TP4 with reference to A8TP1 (GND ANLG).
- 19. Adjust A7R18 (Z) for a DVM reading of 0.000 \pm 0.001 Vdc.
- 20. Connect the DVM to A8TP9 with reference to A8TP1 (GND ANLG).

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21. Adjust A8R18 (Z) for a DVM reading of 0.000 \pm 0.001 Vdc.

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5-17, FREQUENCY ACCURACY

REFERENCE:

Performance Test: Paragraph 4-13 Service Sheet: A8

DESCRIPTION:

The 83590A CW frequency is set first to the low end and then to the high end of Band 2. Special calibration modes are used for this procedure (SHIFT 90 for the low end of Band 2 and SHIFT 91 for the high end of 3 and 2). When the output frequency matches the front panel frequency display, the calibration switches on A8 are set for the appropriate correction factor. A8S1 calibrates the lower portion of the band and A8S2 calibrates the high section of the band.

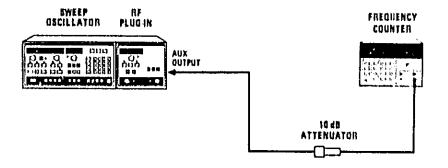


Figure 5-9. Frequency Accuracy Test Setup

EQ	U	I	р	N	1	E	Þ	1	Т	1
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Frequency Counter	HP 5343A
10 dB Attenuator	Option 010
Sweep Oscillator	HP 8350A

PROCEDURE:

1. Connect the equipment as shown in Figure 5-9 with the Frequency Counter connected to the 83590A rear panel AUX OUTPUT connector through the 10 dB attenuator. Allow the equipment to warm up for 1 hour.

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ADJUSTMENTS

5-17. FREQUENCY ACCURACY (Cont'd)

- 2. On the 8350A, press INSTR PRESET CW 6 . 9 GHz SAVE 1.
- 3. On the 8350A, press CW 1 3 , 5 GHz SAVE 2.
- 4. On the 5343A, press SET , 2 ENTER. This sets the Frequency Counter in a mode which displays twice the input frequency. This step is necessary to compensate for the frequency of the rear panel AUX OUTPUT, which is the YO fundamental frequency, approximately half of the 8350A displayed frequency in Band 2.

Low End Frequency Calibration

- 5. On the 8350A, press RECALL 1 , The 8350A FREQUENCY display should show 6,900 GHz.
- 6. On the 8350A, press SHIFT 9 0 to select the low end frequency calibration mode.
- 7. Adjust the 83590A POWER control if necessary to display 6.900 \pm 0.003 GHz on the Frequency Counter.
- 8. Set switch A8S1 for the hexadecimal value displayed in the 83590A POWER display. Refer to Figure 5-10 for the location of the frequency calibration switches. Refer to Figure 5-11 for an illustration of the calibration switch configuration.
- 9. On the 8350A, press RECALL 1 . Verify that the Frequency Counter reads 6.900 \pm 0.010 GHz.

High End Frequency Calibration

- 10. On the 8350A, press RECALL 2. The 8350A FREQUENCY display should show 13.500 GHz.
- 1). On the 8350A, press SHIFT 9 1 to select the high end frequency calibration mode.
- 12. Adjust the 83590A POWER control if necessary to display 13.500 ± 0.003 GHz on the Frequency Counter.
- 13. Set switch A8S2 for the value displayed in the 83590A POWER display in the same manner as that described in step 8.
- 14. On the 8350A, press RECALL 2 . Verify that the Frequency Counter reads 13.500 \pm 0.010 GHz.
- 15. On the 8350A, press RECALL 1 . Manually adjust the 8350A CW FREQUENCY control across band 2 (6.9 to 13.5 GHz) and check for Frequency Counter readings which correspond to the displayed 8350A FREQUENCY display reading (± 10 MHz). If necessary repeat steps 5 through 14.

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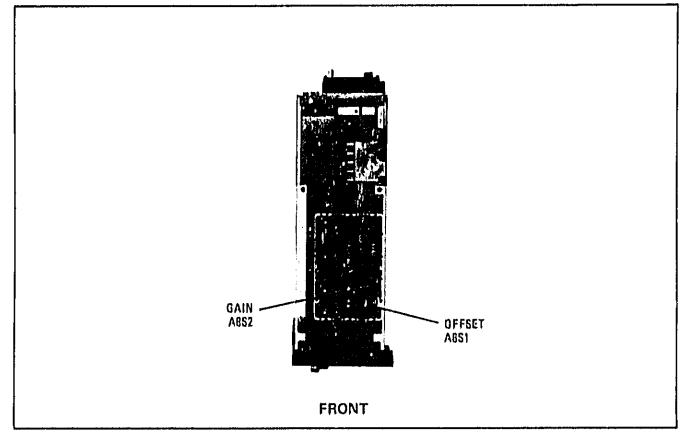


Figure 5-10. Frequency Calibration Adjustment Location

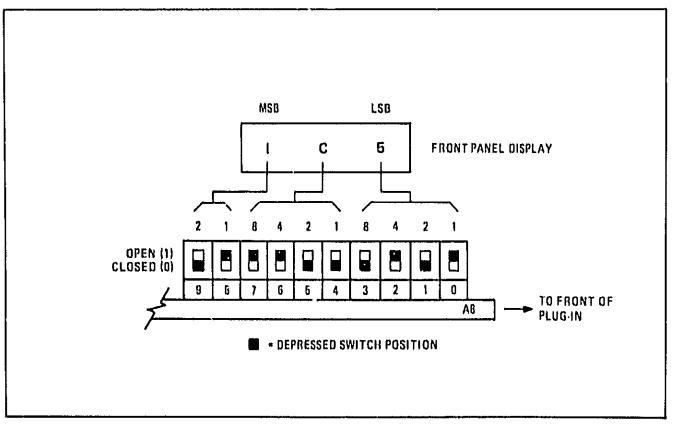


Figure 5-11. A8S1 and A8S2 Frequency Calibration Switch Configuration

ART 1 104.9

5-18. YO RETRACE COMPENSATION

REFERENCE:

Performance Test: Paragraph 4-13 Service Sheet: A8

DESCRIPTION:

During sweep retrace and each bandswitch, the YO frequency is forced to the required beginning frequency of the next band by the retrace compensation circuit. This circuit is adjusted to maximize the YO frequency setding time before sweeping the next band. An external frequency meter is set to the YO frequency for the start of the next band. The width of the frequency meter pip corresponds to how long the YO has settled at the correct start frequency.

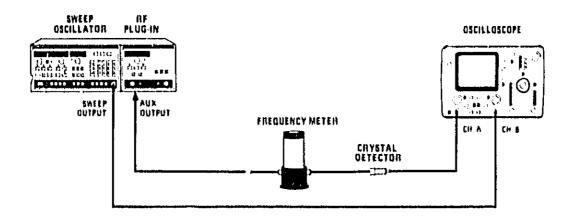


Figure 5-12, YO Retrace Compensation Test Setup

EQUIPMENT:

Oscilloscope Crystal Detector	HP 1740A HP 8470B
Frequency Meter (3.7 to 12.4 GHz) Frequency Meter (0.96 to 4.2 GHz)	HP 537A
Sweep Oscillator.	HP 8350A

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5-18. YO RETRACE COMPENSATION (Cont d)

PROCEDURE:

NOTE

This procedure requires that A351 is set to the factory-set position. Refer to Table 5-6.

- 1. Connect the equipment as shown in Figure 5-12 with the oscilloscope connected through the detector and 536A Frequency Meter to the 83590A rear panel AUX OUTPUT. On the 8350A, press INSTR PRESET ; set the RF Blanking on. Allow the equipment to warm up for 1 hour.
- 2. Set the oscilloscope controls as follows:

Channel B DC	
Channel B Sensitivity 2 Volts/Div.	
Horiz, Sweep	
Delayed Sweep	
Display CHOP	
Trigger	
Sweep Mode MAIN	

- 3. Adjust the vertical sensitivity of Channel A on the oscilloscope to bring the trace to center screen.
- 4, Set the 536A Frequency Meter to 3.5 GHz.

AND A DESCRIPTION OF A

5. Use the delayed sweep vernier to set the delayed part of the trace on the bandswitch point between Band 1 and Band 2 as shown in Figure 5-13.

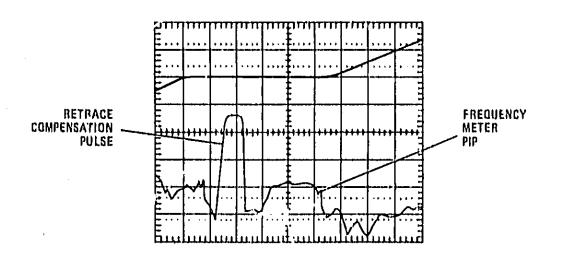


Figure J-13. YO Retract Compensation Pulse

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ADJUSTMENTS

5-18. YO RETRACE COMPENSATION (Cont'd)

- 6. On the oscilloscope, go to delayed sweep and fine-adjust the Frequency Meter to set the frequency pip near center screen.
- 7. Start with ABR55 (RTC COMP) fully clockwise and adjust it for the widest and flattest pip while moving the Frequency Meter to track the bandswitch frequency. A well adjusted retrace compensation pulse is shown in Figure 5-13.

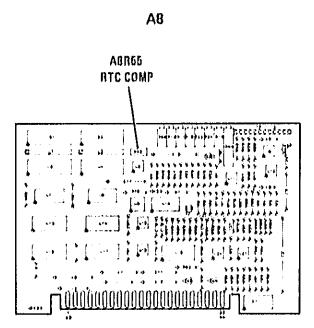


Figure 5-14. YO Retrace Compensation Adjustment Location

- 8. Select main sweep on the oscilloscope and adjust the delayed sweep vernier to move the delayed portion of the sweep to the bandswitch point between Band 2 and Band 3.
- 9. Replace the 536A Frequency Meter with the 537A and set it to 4.49 GHz.
- 10. On the oscilloscope, go to delayed sweep and fine adjust the wavemeter to set the frequency pip near center screen. If the previous Band 1 to Band 2 adjustment was made properly, this bandswitch point will look the same. If it does not, repeat steps 4 through 10 for the best compromise.

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5-19. YO DELAY COMPENSATION

REFERENCE:

Performance Test: Paragraph 4-13 Service Sheet: A8

DESCRIPTION:

This circuit compensates for the delay in the RF sweep output that occurs at fast sweep speeds. An external frequency meter is used to generate a frequency-dependent marker which is aligned with a tuning ramp-dependent marker generated from the 8350A mainframe. Sweep time is decreased, and delay in the YO is observed as the difference between the two marker pips.

Delay compensation adjustments are made while observing the shift between marker pips at a sweep time of 10 milliseconds (worst case for single-band sweeps). At sweep times greater than 100 msec, delay should not exceed ± 15 MHz (the difference between CW and Swept Frequency accuracies).

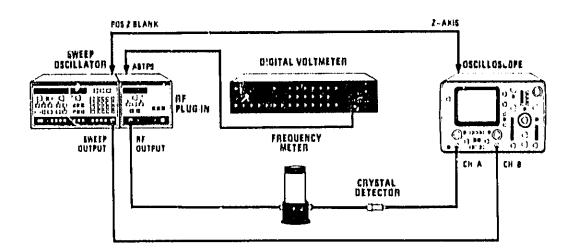


Figure 5-15. YO Delay Compensation Test Setup

EQUIPMENT:

WINDOW STATES

Digitel Voltmeter	HP 3456A
Oscilloscope	HP 1740A
Frequency Meter (3.7 to 12.4 Gifz)	HP 537A
Frequency Meter (12.4 to 18 GHz)	HP P532A
Crystal Detector	HP 8470B
Sweep Oscillator	HP 8350A

5-19. YO DELAY COMPENSATION (Cont'd)

PROCEDURE:

NOTE

This procedure requires that A361 is set to the factory-set position. Refer to Table 5-6.

- 1. Connect the equipment as shown in Figure 5-15 with the 537A Frequency Meter. On the 8350A, press INSTR PRESET and allow the equipment to warm up for 1 hour.
- 2. Set the oscilloscope for A versus B sweep mode to obtain a display of amplitude versus frequency.
- 3. On the 8350A, press CW.
- 4. Measure and note the DC voltage at A8TP9.
- 5. On the 8350A, press CF $\Delta F = 0$ MHz.
- 6. Adjust A8R18 (Z) for a DVM reading equal to the reading noted in step 4. Remove the DVM test leads.
- 7. On the 8350A, enter the front panel data as follows:

INSTR PRESET START 6 . 9 GHz STOP 3 5 GHz 1 SWEEP TIME 1 0 ms MI 7 2 GHz AMPTD MKR **RF BLANK** SAVE 2

- 8. On the 8350A, press SWEEP TIME 2 0 0 ms SAVE 1.
- 9. On the 8350A, press M2 1 3 , 2 GHz SAVE 3 ,
- 10. On the 8350A, press SWEEP TIME 1 0 ms SAVE 4.
- 11. On the 8350A, press RECALL 1.
- 12. Expand the oscilloscope trace at the marker by centering the marker on the oscilloscope then setting the oscilloscope for a magnified horizontal trace. Set the 537A Frequency Meter so that the peak of the pip is on the leading edge of the 7.2 GHz marker.
- 13. On the 8350A, press RECALL 2.
- 14. Adjust A8R12 (LO) so that the peak of the 537A Frequency Meter pip is on the leading edge of the marker.

ADJUSTMENTS

5-18. YO DELAY COMPENSATION (Cont'd)

- 15. Verify that the delay is accurate by manually adjusting the sweep time from 10 ms to 200 ms. Reset ABR12 (LO) as necessary for the best compromise in overall delay setting (minimum delay per change in sweep time). The position of the 537A Frequency Meter pip should typically stay within ± 15 MHz as read on the Frequency Meter across the 10 ms to 200 ms range.
- 16. On the 8350A, press RECALL 3 .
- 17. Replace the 537A Frequency Meter with the P532A and set 6 to that the peak of the pip is coincident with the leading edge of the 13.2 GHz market
- 18. On the 8350A, press RECALL 4.
- 19. Adjust ABR10 (H1) so that the peak of the Frequency Meter is coincident with the leading edge of the marker.
- 20. Verify that the delay is accurate by manually adjusting the sweep time from 10 ms to 200 ms. Reset A8R10 (HI) as necessary for the best compromise in overall delay setting (minimum delay per change in sweep time). The position of the Frequency Meter pip should typically stay within ±15 MHz as read on the P532A Frequency Meter across the 10 ms to 200 ms sweep speed range.

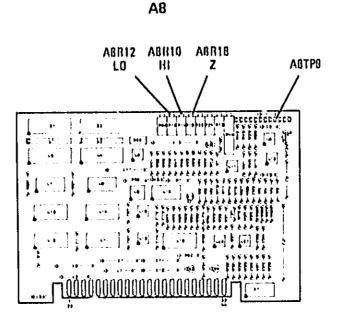


Figure 5-16. YO Delay Compensation Adjustment Location

5-20. SLOW SPEED YTM TO YO TRACKING

REFERENCE:

Performance Test: Paragraph 4-13 Service Sheet: A6 and A7

DESCRIPTION:

The 83590A is set to sweep Bands 2 and 3 (7 to 20 GHz), and the ALC loop is opened by selecting the External ALC mode. The SRD Bias for the Switched YTM is preset and requires further adjustment according to Paragraph 5-21. Special calibration modes are selected (SHIFT 92 for the beginning of Band 2 and SHIFT 93 for the rest of the sweep). The output power is peaked for each calibration mode, and the appropriate correction factor is entered with the calibration switches. A7S1 calibrates the lower part of Band 2 and A7S2 calibrates the higher frequencies.

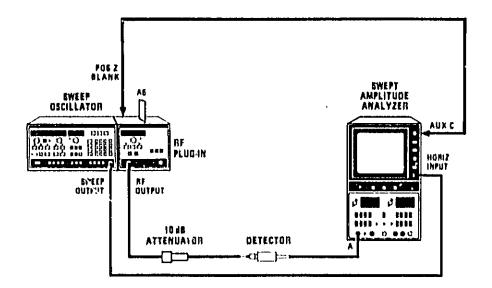


Figure 5-17. Slow Speed YTM and YO Tracking Test Setup

EQUIPMENT:

Swept Amplitude Analyzer	HP 8755C
Display Mainframe	. HP 182T
Detector	HP 11664B
10 dB Attenuator Weinschel M	
Sweep Oscillator	HP 8350A
Extender Board HP	08350-60031

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5-20. SLOW SPEED YTM TO YO TRACKING (Cont'd)

PROCEDURE:

NOTE

This procedure requires that A3S1 is set to the factory-set position. Refer to Table 5-6.

NOTE

During this adjustment, a localized drop in power may occur. This drop in power is due to the YTM being overdriven and is called squagging. If squagging occurs in Band 2, adjust AGR68 and R73 to eliminate the squagging and to maximize power across the band. If squagging occurs in Band 3, adjust AGR69 and R74.

- 1. Connect the equipment as shown in Figure 5-17 with the 83590A A6 Sweep Control Board on an extender. Allow the equipment to warm up for 1 hour.
- On the 8350A press INSTR PRESET START 7 GHz SWEEP TIME 2 0
 0 ms □[¬]MOD . On the 83590A, press EXT ALC MODE . The unleveled lamp should be lit.
- 3. Presct A6R63 (3HL) to midrange. Refer to Figure 5-18 for adjustment locations.
- 4. Preset A6R78 (T) and A6R12 (C) 1/4 turn from the full counter-clockwise position.
- 5. Select 1 dB/Division display resolution on the 8755C and center the display.
- 6. On the 8350A, press SHIFT 9 2 to enable the YTM OFFSET DAC subroutine. Using the 83590A POWER control, peak the power within the first graticule of the display.
- 7. Enter the number displayed on the 83590A POWER display into A7S1 as shown in Figure 5-20. Refer to Figure 5-19 for the switch location.
- 8. On the 8350A, press SHIFT 9 3 to enable the YTM GAIN DAC subroutine. Using the 83590A POWER control, peak the power within the last graticule of the display.
- 9. Enter the number displayed on the 83590A POWER display into A7S2 as shown in Figure 5-20. Refer to Figure 5-19 for the switch location.
- 10. On the 8350A, press INSTR PRESET so that the new calibration data will be entered from the current switch settings.
- 11. On the 8350A, press STOP 7 GHz. On the 83590A, press EXT ALC MODE .
- 12. Adjust A7R51 (B1 OFS) to maximize the Band 1 displayed trace minimum power points.

ADJUSTMENTS

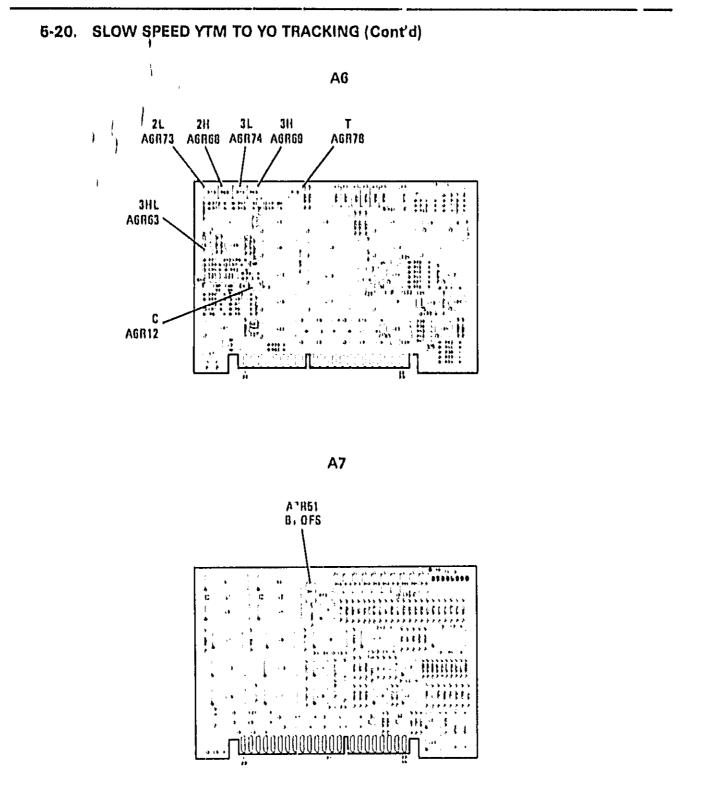


Figure 5-18. Slow Speed YTM to YO Tracking Adjustment Locations

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Adjustments

Model 83590A

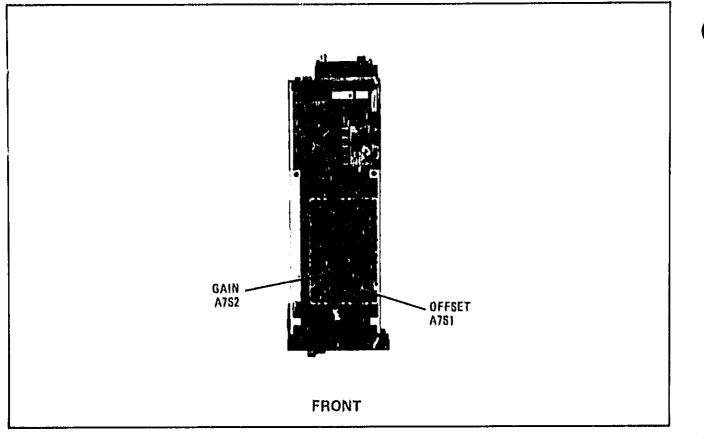


Figure 5-19. YTM to YO Tracking Calibration Switch Location

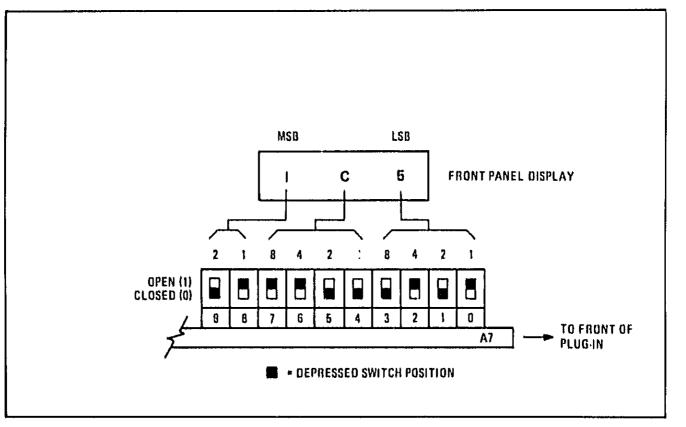


Figure 5-20. YTM to YO Tracking Calibration Switch Configuration

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5-21. SRD BIAS

REFERENCE:

Performance Test: Paragraphs 4-17, 4-19 Service Sheet: A4 and A6

DESCRIPTION:

The High Power SRD Bias is set by peaking the 8755C displayed trace with A6R68 (2H) and A6R73 (2L) in Band 2, and A6R69 (3H) and A6R74 (3L) in Band 3.

The Low and Mid Power SRD Bias is adjusted by inserting a voltage source through a 1 kOhm current-limiting resistor into the MOD 1 signal path in place of the A4 ALC board output. With the 83590A at maximum RF output power level, the voltage is increased (from a starting point of 0.6 Vde to a maximum of 5.0 Vde) to set the RF output to a point just above the noise level of the 8755C. At this point, A6R63 (3HL) is adjusted until minimum slope is obtained on an Oscilloscope display, and A6R12 (C) is adjusted to peak the power in Bands 2 and 3. The voltage from the Power Supply is decreased until the display on the 8755C reaches a point halfway between full RF out and the previous point. A6R78 (T) is adjusted to optimize the power at this intermediate point. The Power Supply is then removed.

The YTM fundamental feedthrough is suppressed while Bands 2 and 3 are swept. A ratio measurement is taken to determine system error and is subtracted from the ratio of a filtered RF path (fundamental feedthrough only) and an unfiltered RF path. A6R78 (T) is then adjusted until the harmonics specification is met.

EQUIPMENT:

Swept Amplitude Analyzer
Display Mainfrance,
Detectors (2)
6 dB Attenuator
10 dB Attenuator Weinschei Model M9-10
20 dB Altenuator
Directional Coupler
Power Supply,
Low Pass liller (0.8 GHz).
Storage Normalizer
Use moscope
Extender Board
Sweep Oscillator
1 kOhm Resistor

PROCEDURE:

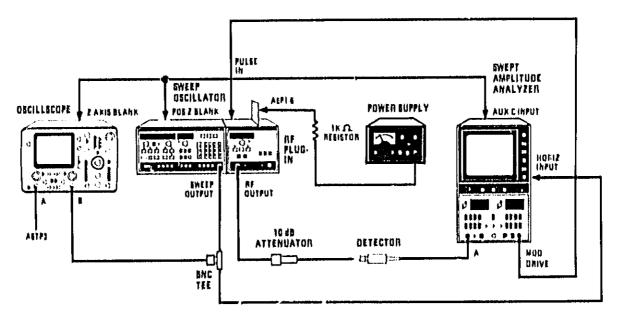
NOTE

Turn the 8350A LINE power OFF when removing or installing PC boards.

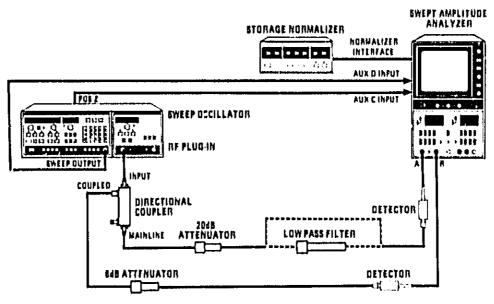
NOTE

This procedure requires that A3S1 is set to the factory-set position (refer to Table 5-6).

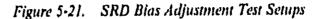
SRD Blas (Cont'd)



a) Low and Mid Power Test Setup



b) YTM Fundamental Feedthrough Test Setup





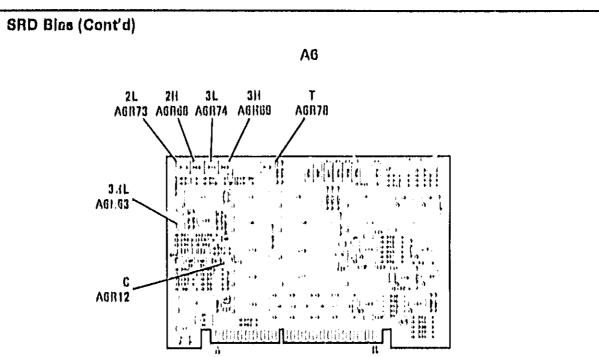


Figure 5-22. SRD Blas Adjustment Location

High Power SRD Blas

- Connect the equipment as shown in Figure 5-17 with the 83590A A6 Sweep Control board on an extender. With the LINE power OFF, remove the 83590A A4 ALC board. Connect the 8755C MODULATOR DRIVE output to the 83590A rear-panel PULSE IN connector.
- 2. Allow the equipment to warm up for one hour.
- 3. On the 8350A press INSTR PRESET START 7 GHz SWEEP TIME 2 0 0 ms.
- 4. Set the 8755C display resolution for 5 dB/DIV and center the display.
- 5. Adjust A6R73 (2L) and A6R68 (2H) until Band 2 is at maximum power across the band. A6R73 adjusts the low frequency end of Band 2 and A6R68 adjusts the h²sh end.
- 6. Adjust A6R74 (3L) and A6R69 (3H) until Band 3 is at maximum power across the band. A6R74 adjusts the low frequency end of Band 3 and A6R69 adjusts the high end.
- 7. Repeat steps 5 and 6 in order to obtain optimum power across the display.
- 8. Check the YO to YTM tracking to ensure it has not changed (refer to paragraph 5-20). If retracking is necessary, adjust A6R68, R69, R73, and R74 as necessary to eliminate any squegging that may have occurred.

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SRD Bins (Cont'd)

Low and Mid Power SRD Blas

- Set up the equipment as shown in Figure 5-21a, with a 1 kOhm resistor connected to A6P1-6 (reference to ground). Remove the 83590A A4 ALC hoard. Connect the 8755C Swept Amplitude Analyzer MODULATOR DRIVE output to the 83590A rear-panel PULSE IN connector.
- 10. Allow the equipment to warm up for one hour.
- 11. On the 8350A, press INSTR PRESET START 7 GHz SWEEP TIME 2 0 0 ms
- 12. Set the 8755C display resolution for 10 dB/DIV and adjust the display to the top graticule. On the 1740A Oscilloscope, select A vs B, set Channel 1 to .5 V/DIV, set Channel 2 to 1 V/DIV, and DC-couple Channels 1 and 2.
- 13. On the 8755C, select the R DISPLAY and note the position of the trace. This is the noise floor of the 8755C. Return to the A DISPLAY.
- Set the Power Supply voltage at .6 Vdc and increase the voltage until the lowest point of the 8755C display is 10 dB above the noise floor (do not exceed 5 Vdc).
- 15. Monitor A6TP3 with the Oscilloscope and adjust A6R63 until minimum slope (flat display) is obtained.
- 16. Monitor the 8755C display and adjust A6R12 until optimum power is obtained for Bands 2 and 3.
- 17. Reduce the Power Supply voltage until the power displayed on the 8755C rises to a level approximately halfway between maximum power output (0 volts from the Power Supply) and the previous point.
- 18. Adjust A6R78 to optimize the power in Bands 2 and 3 at this intermediate power level.

YTM Fundamental Feedthrough

- 19. Set up the equipment as shown in Figure 5-21b without the Low Pass Filter, and with the 83590A A4 ALC board installed.
- 20. Allow the equipment to warm up for one hour.
- 21. On the 8350A, press INSTR PRESET START 8 GHz SWEEP TIME 2 0 0 ms □□ MOD .
- 22. On the 8755C, select A/R DISPLAY and 5 dB/DIV. Center the display.
- 23. On the 8750A, press SELECT CH 1 and DISPLAY STORE INPUT. The display now shows the system error between Channel A and Channel R.
- 24. Press REFERENCE MEMORY STORE and then DISPLAY INPUT -MEM. The trace on the 8755C should be flat, showing that system errors have been removed. Note the position of the trace and the REFERENCE LEVEL. This will be used as a reference in step 27.

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SRD Blas (Conta)

- 25. Install the Low Pass Filter at the location shown in Figure 5-21b.
- 26. Adjust the REFERENCE LEVEL so that the entire trace is on the display. The YTM fundamental feedthrough is now displayed on the 8755C.
- 28. Determine how many dB the trace is below the reference position established in step 24. If necessary, adjust A6R78 (T) until the trace is greater than 25 dB below the reference.
- 28. Follow the performance test in paragraph 4-14 to ensure that power specifications are met. If specifications are not met, repeat the adjustments in paragraphs 5-20 and 5-21.

5-22. YTM DELAY COMPENSATION

REFERENCE:

Performance Test: Paragraph 4-14 Service Sheet: A7

DESCRIPTION:

The YTM Delay Compensation circuit is adjusted to optimize YTM to YO tracking over varying sweep rates. Adjustments are provided for sequential sweeps (multiband) and single band sweeps.

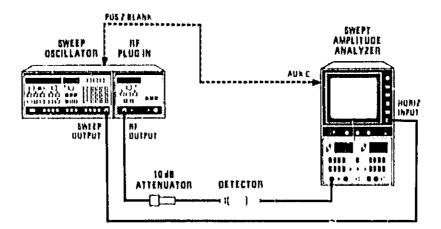


Figure 5-23. YTM Delay Compensation Adjustment Test Setup

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EQUIPMENT:

Swept Amplitude Analyzer	HP 8755C
Display Mainframe	HP 182T
Delector	HP 11664B -
10 dB Attenuator Weinschel Me	
Sweep Oscillator	HP 8350A

6-22, YTM DELAY COMPENSATION (Cont'd)

PROCEDURE:

NOTE

This procedure requires that A361 is set to the factory-set postion. Refer to Table 5-6.

1. Connect the equipment as shown in Figure 5-23. Do not connect the BNC cable between the 8350Å rear panel POS Z BLANK and the 182T AUX C connector yet. Preset A7R45 (SEQ TC) fully counter-clockwise. Refer to Figure 5-24 for adjustment locations. Allow the equipment to warm up for 1 hour.

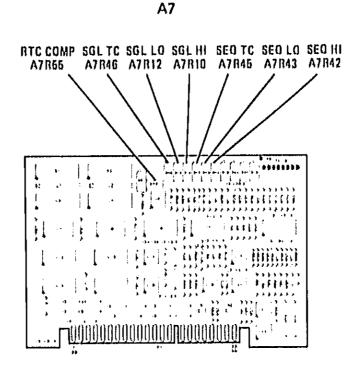


Figure 5-24. YTM Delay Compensation Adjustment Locations

- 2. On the 8350A and 83590A press INSTR PRESET □ MOD EXT ALC MODE SAVE 1 SWEEP TIME 0 . 5 s SAVE 2.
- 3. Press RECALL 1 . Adjust A7R45 (SEQ TC) for the highest power with the best defined (brightest) bandswitch point between Band 2 and Band 3.

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5-22. YTM DELAY COMPENSATION (Cont'd)

- Connect a BNC cable from the 8350A rear panel POS Z BLANK connector to the 182T rear panel AUX C connector.
- 5. Adjust A7R43 (SEQ LO) for maximum power at the beginning of Band 2.
- 6. Adjust A7R42 (SEQ HI) for maximum power at the end of Band 3.
- 7. On the 8350A, iterate between **RECALL** 1 and **RECALL** 2 while readjusting A7R42 (SEQ H1) and A7R43 (SEQ LO) as necessary to minimize the power level changes.
- 8. On the 8350A, press START 7 . I GHz SWEEP TIME 3 0 ms.
- 9. Adjust A7R55 (RTC COMP) for maximum power in Band 2.
- 10. Vary the 8350A START FREQUENCY control from 2 GHz to 20 GHz to check for power variations. Readjust A7R42 (SEQ HI), A7R43 (SEQ LO), and A7R55 (RTC COMP) as necessary to minimize any droop in power (particularly near 20 GHz). The worst case droop should not exceed 0.5 dB as the START frequency is varied. If this step cannot be met, repeat the Slow Speed YTM to YO Tracking Adjustments.
- 11. On the 8350A and 83590A, press_INSTR PRESET_____ MOD_EXT_ALC MODE .
- 12. Repeatedly press SINGLE SWEEP TRIGGER while watching the displayed power level. Readjust A7R42 (SEQ HI) and A7R43 (SEQ LO) as necessary to minimize the power level difference between a 30 ms single sweep and a 30 ms INT sweep.
- 13. On the 8350A and 83590A, press INSTR PRESET □ MOD START 6 . 9 GHz STOP 1 3 . 5 GHz EXT ALC MODE .
- 14. Preset A7P.46 (SGL TC) fully counter-clockwise.
- 15. While continuously changing the SWEEP TIME control for a sweep speed from 10 ms to 100 ms, adjust A7R12 (SGL LO) to maximize the power at the low end of Band 2. In the same manner, adjust A7R10 (SGL HI) to maximize the power at the high end of Band 2. Then adjust A7R46 (SGL TC) to maximize the power at the very start of the band.
- 16. On the 8350A, press START 1 3 , 4 GHz STOP 2 0 GHz. Vary the sweep speed as in step 15 and note any drop in power. If the change is greater than 0.5 dB, make slight adjustments to A7R10 (SGL HI) and A7R12 (SGL LO). If it is necessary to adjust A7R10 (SGL HI) and A7R12 (SGL LO), repeat step 15 and 16 until the power variation while adjusting sweep time is less than 0.5 dB.

5-23. BAND OVERLAP

REFERENCE:

Performance Test: Paragraph 4-13 Service Sheet: A6

DESCRIPTION:

The 83590A is set to sweep across each bandswitch point. A frequency meter is set to the bandswitch frequency and the gain of the Variable Gain Amplifier on the A6 Sweep Control assembly is adjusted for a smooth frequency transition between bands.

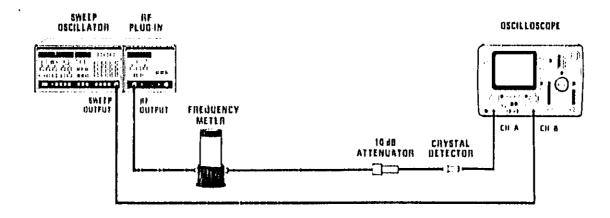


Figure 5-25. Band Overlap Adjustment Test Setup

EQUIPMENT:

Oscilloscope	HP 1740A
Frequency Meter (3.7–12.4 GHz)	HP 537A
Frequency Meter (12.4–18 GHz)	HP P532A
10 dB Attenuator HP 8491B	Option 010
Crystal Detector	HP 8470B
Sweep Oscillator	HP 8350A

PROCEDURE:

NOTE

This procedure requires that A3S1 be set to the factory-set position. Refer to Table 5-6.

- 1. Connect the equipment as shown in Figure 5-25 with the 537A Frequency Meter in the test setup. Allow the equipment to warm up for 1 hour.
- 2. On the 8350A, press INSTR PRESET CF 7 GHz ΔF 1 5 0 MHz.

5-40

그는 아이가 잘 못 하는 것 같아요. 이 가장 같아요. 이 가장 하는 것이 가지 않아요. 이 것을 수 있는 것 같아요.

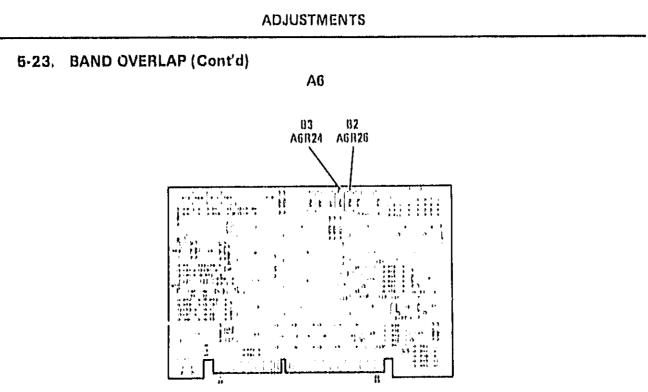
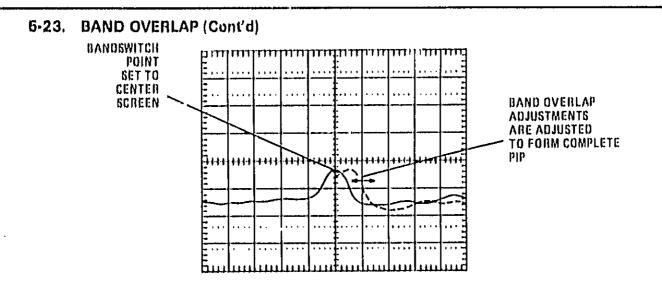


Figure 5-26. Band Overlap Adjustment Locations

- 3. Set the oscilloscope for A versus B display mode to display amplitude versus frequency. Center the display on screen.
- 4. Set the 537A Frequency Meter to 7.0 GHz.
- 5. Center the bandswitch point on the display using the 8350A FREQUENCY control.
- 6. Adjust the Frequency Meter to put the left half of the pip on the left side of the switch point.
- 7. Adjust A6R26 (B2) to bring the right side pip over to the switch point so that the right half of this pip mates with the left half of the other as shown in Figure 5-27. Refer to Figure 5-26 for the adjustment location. The pip should be undisturbed as it moves through the bandswitch point.
- 8. Replace the 537A Frequency Meter with the P532A and set it to 13.5 GHz.
- 9. On the 8350A, press CF 1 3 . 5 GHz.
- 10. Repeat steps 5 through 7 but, this time, adjust A6R24 (B3) in step 7.

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ADJUSTMENTS





5-24, FREQUENCY REFERENCE 1V/GHz OUTPUT

REFERENCE:

Performance Test: Paragraph 4-13. Service Sheet: A2

DESCRIPTION:

The frequency reference rear panel output is adjusted for 1 Volt per GHz output. Example: 2 GHz = 2 Volts: 3 GHz = 3 Volts, etc.

EQUIPMENT:

Percenting a second s	
Sweep Oscillator	HP 8350A

PROCEDURE:

NOTE

Frequency Accuracy must be adjusted correctly (Paragraph 5-17) before adjusting Frequency Reference 1 V/GHz output.

- Connect the equipment with the DVM connected to the rear panel 1V/GHz Frequency Reference connector, J4. Allow the equipment to warm up for 1 hour.
- 2. Adjust A2R4 (OFFSET) to the center of its mechanical range. Refer to Figure 5-28 for the adjustment location.
- 3. On the 8350A, press CW 8 GHz.

0

4. Adjust A2R4 (OFFSET) for a DVM reading of 8.000 ±0.005 Vdc.

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ADJUSTMENTS

5-24. FREQUENCY REFERENCE 1V/GHz OUTPUT (Cont'd)

- 5. On the 8350A, press CW 1 5 GHz.
- 6. Adjust A2R1 (GAIN) for a DVM reading of 15.000 ±0.005 Vdc.
- 7. Repeat steps 2 through 6 until there is no change.

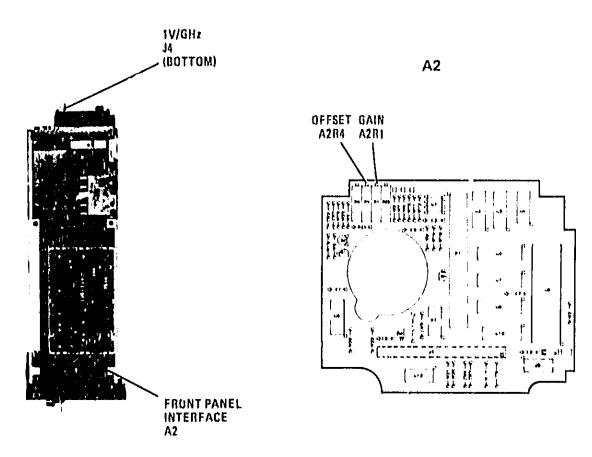


Figure 5-28. Frequency Reference Adjustment Locations

5-25, ALC ADJUSTMENT

NOTE

Complete adjustment of the leveling loop requires several procedures to be performed in the order prescribed from paragraphs 5-25 through 5-26. Deviation from this routine may cause improper leveling and/or power variation problems.

REFERENCE:

Performance Test: Paragraph 4-14. Service Sheet: A4

DESCRIPTION:

Adjustments compensate for DC offsets in the detected RF path and the Main ALC Amplifier. Power is roughly calibrated and low band flatness is optimized.

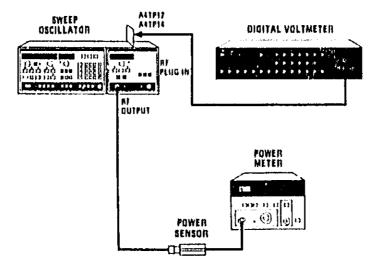


Figure 5-29. ALC Adjustment Test Setup

EQUIPMENT:

Digital Voltmeter	HP 3456A
Power Meter	HP 436A
Thermistor Mount	HP 8485A
Extender Board	08350-60031
Sweep Oscillator	HP 8350A

5-25, ALC ADJUSTMENT (Cont'd)

PROCEDURE

NOTE

Turn AC power OFF when removing or installing PC boards.

NOTE

This procedure assumes that A3S1 is set to the factory-set position (Table 5-6), and that the B350A Sweep Oscillator, 27.6 kHz square wave modulation is selected.

1. Remove A5 FM Driver board. Place A4 assembly on an extender board. Sweep the full range of the Plug-in at any leveled power. Preset the following adjustments as indicated:

A4R47	(OFS	1)	,						• •		•	,		 •	•	,		•	,		• •	,	•	•	•			• •	Midrange
A4R56	(OFS	2)		• •	•			,			•			 ,	,	,	,	,	,	. ,	 	,	,	,	•			•	
A4R59	(OFS	3)			,	, ,	,				•		, ,		,		,				 	,	,	•	•	,	, ,	• •	Midrange
A4R67	OFS	4)	,		,					,					,	,	,	,			 	,			•				Midrange
AIRIT	İGAII	NÍ.	,		,		,			,			, ,			•	,		,	• •	 		,		,	•		• •	Midrange
																													Fully CW

2. Float the ground on the Digital Voltmeter and measure the voltage between A4TP12 and A4TP14. Refer to Figure 5-30 for adjustment locations. Adjust A4R47 (OFS 1) for 0.000 ± 0.001 Vdc.

A4

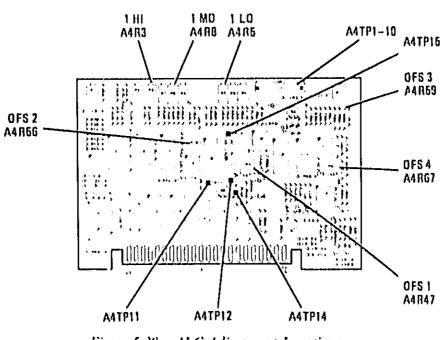


Figure 5-30. ALC Adjustment Locations

5-25. ALC ADJUSTMENT (Cont'd)

- Attach a jumper from A4TP11 to ground. Connect the DVM to A4TP11 and A4TP5 and adjust A4R56 (OFS 2) for a DVM reading of 0.000 ±0.001 Vdc. Remove the jumper.
- 4. Connect the DVM between A4TP12 and A4TP15 (floating ground). Adjust A4R59 (OFS 3) for a DVM reading of 0.000 ±0.001 Vdc.
- 5. On the 8350A, press CW and ensure that the power is leveled (83590A UNLEVELED light off). Connect the DVM to P1 pin 15/37 (analog ground) and A4TP7 and adjust A4R67 (OFS 4) for a DVM reading of 0,000 ±0.001 Vdc.
- 6. Turn instrument Line power OFF. Remove A4 assembly from the extender board and reinsert A4 directly into the instrument. Turn ON Line power to instrument. Connect Power Meter sensor to RF OUTPUT.
- 7. On the 8350A press CW 2 . 0 GHz . Set POWER for Plug-in front panel reading of -3 dBm. Adjust A4R5"1 LO" for an RF OUTPUT power of -3 dBm ±0.1 dB.
- 8. Set POWER for Plug-in front panel reading of +7 dBm. Adjust A4R8 "1 MD" for an RF OUTPUT power of +7 dBm ±0.1 dB.
- 9. herate steps 7 and 8 until both low and midpower ranges are calibrated.
- 10. Set POWER for Plug-in front panel reading of +10 dBm. Adjust A4R3 "1 HI" for an RF OUTPUT power of +10 dBm ±0.1 dB. This roughly calibrates the RF power. Fine calibration is documented in a later procedure.
- 11. Reinstall the A5 FM board assembly.

ADJUSTMENTS

5-26. ALC INTERNAL LEVELED FLATNESS

NOTE

Complete adjustment of the leveling loop requires several procedures to be performed in the order prescribed from paragraphs 5-26 through 5-28. Deviation from this routine may cause improper leveling end/or power variation problems.

REFERENCE:

Performance Test: Paragraph 4-14. Service Sheet: A5

DESCRIPTION:

Four parallel circuits on the A5 assembly provide adjustments for ALC flatness. BP1 through BP4 and SL1 through SL4 determine the slope of the flatness compensation signal input to the A4 ALC assembly. Breakpoint potentiometers (BP1-4) determine the frequency at which the corresponding slope potentiometers (SL1-4) begin to affect power output leveling.

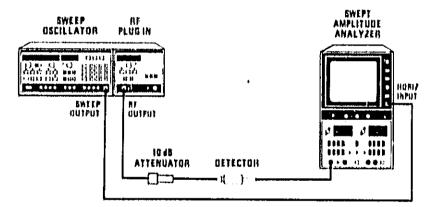


Figure 5-31. Internal Leveling Adjustment Test Setup

EQUIPMENT:

Swept Amplitude Analyzer	HP 8755C
Display Mainframe	HP 182T
Defector	HP 11664B -
10 dB Attenuator Weinschel Mot	
Sweep Oscillator	HP 8350A

PROCEDURE:

NOTE

This procedure requires that A3S1 is set to the factory-set position (Table 5-6), and that the 8350A Sweep Oscillator, 27.8 kHz square wave modulation is selected.

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5-26. ALC INTERNAL LEVELED FLATNESS (Cont'd)

1. Connect equipment as shown in Figure 5-31 with the 8755C monitoring the RF output through the 10 dB attenuator. On the 8350A, press INSTR PRESET LF MOD . Allow the equipment to warm up for 1 hour.

NOTE

The following step negates any power variation companisation by effectively removing the ALC Power Variation Adjustments from the leveling circuitry. This step may be omitted if RF power variation approaches specified limits.

 Adjust all breakpoint potentiometers fully clockwise to effectively remove the circuit from the leveling loop (A5R34 (BP1), A5R36 (BP2), A5R38 (BP3), and A5R40 (BP4)). Refer to Figure 5-32 for adjustment locations.

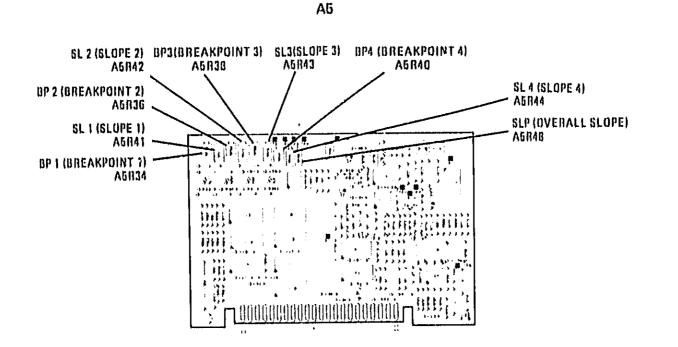


Figure 5-32. Internal Leveling Adjustment Locations

- 3. Adjust A5R48 (SLP) for best overall flatness.
- 4. Set breakpoint adjustments A5R34, A5R36, A5R38, and A5R40 (BP1-4) and slope adjustments A5R41 through A5R44 (SL1-4) for best overall flatness. (BP1 and SL1 are interdependent adjustments, as are BP2 and SL2, etc.). The breakpoint potentiometers determine the frequency at which the slope adjustments will take effect. This is observed as a pivot point on the CRT trace.

Model B3590A

2

Adjustments

ADJUSTMENTS

5-27. POWER METER LEVELING CALIBRATION

NOTE

Complete adjustment of the leveling loop for Power Mater leveling requires several procedures to be performed in the order prescribed from paragraphs 5-25 through 5-28. Deviation from this routine may cause improper leveling and/or power variation problems.

REFERENCE:

Performance Test: Paragraph 4-14. Service Sheet: A4

DESCRIPTION:

Power Meter leveling gain potentiometer A4R9 (PM) calibrates loop gain to full-scale deflection of the leveling meter.

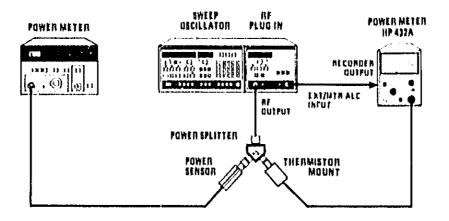


Figure 5-33. Power Meter Leveling Calibration

EQUIPMENT:

Power Meters	HI	р	432/	N ai	nd HP 436A
Thermistor Mount					
Power Sensor					
Power Splitter		,			HP 11667A
Sweep Oscillator		•			HP 8350A

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Adjustments

Model 83590A

ADJUSTMENTS

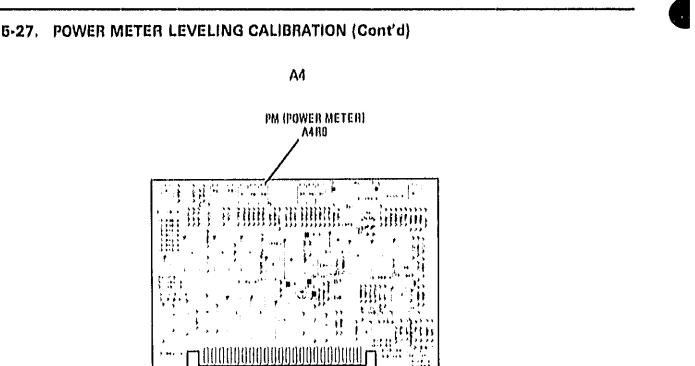


Figure 5-34. Power Meter Adjustment Location

PROCEDURE:

- Connect equipment as shown in Figure 5-33. On the 8350A, press INSTR PRESET CW and select a frequency at midband. Set the RF power level to -2 dBm, as indicated on the 85590A POWER display. Allow the equipment to warm up for 1 hour.
- 2. Select the 0 dB range on the HP 432A Power Meter. Both meters should read approximately -8 dBm. Note the insertion loss through the Power Splitter (typically 6 dB).
- 3. On the 83590A, press MTR and adjust the EXT CAL control to reset the 432A to the same power measured in step 1.
- 4. Increase the 83590A power level until the 432A Power Meter reaches full scale deflection (83590A RF output equals approximately +6 dBm). Adjust A4R9 (PM) until the 436A Power Meter indication is equal to the 83590A POWER display minus the power splitter insertion loss noted in step 1 (approximately 6 dB). Refer to Figure 5-34 for the adjustment location.
- 5. Alternately set the 83590A POWER to -2 dBm (and adjust the 83590A EXT CAL control) and then set the 83590A POWER to +6 dBm (and adjust A4R9 (PM) control) to obtain best compromise (where further adjustment of each is unneccessary).

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ADJUSTMENTS

5-28, ALC GAIN ADJUSTMENT

NOTE

Complete adjustment of the leveling loop requires several procedures to be performed in the order prescribed from paragraphs 5-25 to 5-28. Deviation from this rountine may cause improper leveling and/or power variation problems.

REFERENCE

Performance Test: Paragraphs 4-14, 4-19 and 4-21 Service Sheet: A4

DESCRIPTION:

A4R11 (GAIN) in the input leg of A4U11 adjusts the gain of the Main ALC Amplifier on the A4 assembly, A4R11 (GAIN) is adjusted for maximum possible gain without producing oscillations.

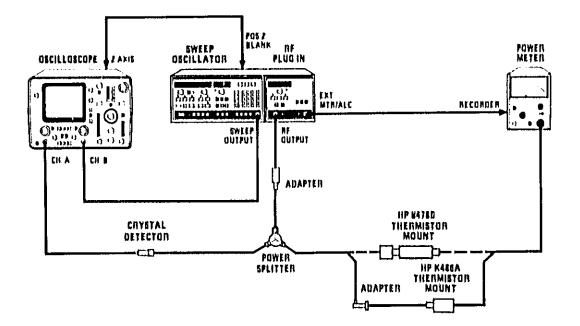


Figure 5-35. ALC Gain Adjustment Test Setup

EQUIPMENT:

Sweep Oscillator HP 8350A	١
Oscilloscope HP 1740A	\$
Crystal Detector HP 8473C	
Power Meter	
Thermistor Mount (0.01 to 18 GHz) HP 8478E	5
Thermistor Mount (18 to 26.5 GHz) HP K486A	
Waveguide to APC 3.5(f) Adapter (18 to 26.5 GHz) HP K281C	•
Power Splitter Weinschel Model 1579A	•
Type N(m) to SMA(I) Adapter HP 1250-1250	ļ

5-28. ALC GAIN ADJUSTMENT (Cont'd)

PROCEDURE:

NOTE

This procedure requires that A381 is set to the factory-set position.

1. Connect the equipment as shown in Figure 5-35 with the 8478B Thermistor Mount connected to the Power Splitter. Preset A4R11 (GAIN) fully counterclockwise. Refer to Figure 5-36 for the adjustment location. Allow the equipment to warm up for 1 hour.

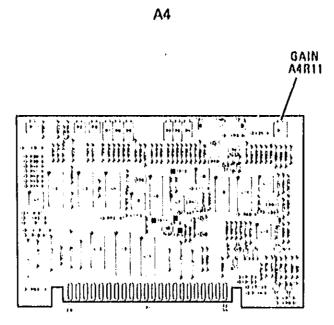


Figure 5-36. ALC Gain Adjustment Location

2. On the 8350A, press INSTR PRESET STOP 1 8, 0 GHz SWEEP TIME 1 0 0 s.

- 3. On the Oscilloscope, select A ve. us B mode to display a plot of amplitude versus frequency. Set the Channel A Vertical Sensitivity for 0.01 volts/division and ac coupling. Set the Channel B Vertical Sensitivity for 1 volt/division and de coupling. Adjust the horizontal position and vertical position controls for a stable display at mid screen.
- 4. On the 8350A, press CW.
- 5. Set the Power Meter RANGE switch to +5 dBm. Note the Power Meter needle position.

6. On the 83590A, press MTR ALC MODE .

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ADJUSTMENTS

5-28, ALC GAIN ADJUSTMENT (Cont'd)

- 7. If necessary, adjust the output power with the 83590A front panel EXT CAL control to position the Power Meter needle to the same reading noted in step 4. Then decrease the Power Meter range switch by three 5 dB steps to -10 dB. This attenuates the output power by 15 dB which causes the 83590A output power to be near the low end of its power range (approximately -5 dBm).
- 8. On the 8350A, press START .
- 9. Observe the trace dot as it sweeps across the CRT. Adjust A4R11 (GAIN) clockwise, increasing the gain of the ALC loop, until the trace dot begins to oscillate. Then reduce the gain slightly to eliminate the oscillations so that a sharp trace dot is obtained.
- 10. Set the 83590A to maximum leveled RF output power by returning the Power Meter range switch to the +5 dB position. Observe the trace through the entire sweep to ensure that no oscillations occur. If oscillations do occur, reduce the gain slightly by turning A4R11 (GAIN) counterclockwise.
- 11. On the 8350A, press INSTR PRESET STOP 1 8 . 0 GHz to set the 83590A to internal leveling.
- 12. Adjust the Oscilloscope Channel A vertical sensitivity to obtain the internally leveled sweep trace at center screen. If oscillations are present, further reduce the loop gain by adjusting A4R11 (GAIN) counterclockwise.
- 13. Reduce the 83590A RF output power by rotating the 83590A POWER control until the 83590A POWER display reads -5 dBm. Observe a full sweep. If oscillations occur, reduce the gain further by adjusting A4R11 (GAIN) counterclockwise.
- 14. Reconnect the equipment with the K486A Thermistor Mount and the Adapter connected to the Power Splitter as shown in Figure 5-35.
- 15. On the 8350A, press INSTR PRESET START 1 7 , 5 GHz STOP 2 0 GHz SWEEP TIME 1 0 0 s.
- 16. On the Oscilloscope, adjust the horizontal position and vertical position controls for a stable display at mid screen.
- 17. On the 8350A, press CW.
- 18. Set the Power Meter RANGE switch to +5 dBm. Note the Power Meter needle position.
- 19. On the 83590A, press MTR ALC MODE .
- 20. If necessary, adjust the output power with the 83590A front panel EXT CAL control to position the Power Meter needle to the same reading noted in step 16. Then, decrease the Power Meter range switch by three 5 dB steps to -10 dB. This attenuates the output power by 15 dB which causes the 83590A output power to be near the low end of its power range (approximately -5 dBm).
- 21. On the 8350A, press START.
- 22. Observe the trace dot as it sweeps across the CRT. If oscillations occur, reduce the gain by adjusting A4R11 (GAIN) counterclockwise.

Adjustments

Model 83590A

ADJUSTMENTS

5-28. ALC GAIN ADJUSTMENT (Cont'd)

- 23. Set the 83590A to maximum leveled RF output power by returning the Power Meter range switch to the +5 dB position. Observe the trace through the entire sweep to ensure that no oscillations occur with the 83590A at maximum power. If oscillations do occur, further reduce the gain slightly by turning A4R11 (GAIN) counterclockwise.
- 24. On the 8350A, press INSTR PRESET START 1 7 , 5 GHz to set the 83590A to internal leveling.
- 25. Adjust the Oscilloscope Channel A vertical sensitivity to obtain the internally leveled sweep trace at center screen. If oscillations are present, further reduce the loop gain by adjusting A4R11 (GAIN) counterclockwise.
- Reduce the 83590A RF output power by rotating the 83590A POWER control until the 83590A POWER display reads -5 dBm. Observe a full sweep. If oscillations occur, reduce the gain further by adjusting A4R11 (GAIN) counterclockwise.

5-29, POWER SWEEP

REFERENCE:

Performance Test: Paragraph 4-14. Service Sheet: A5

DESCRIPTION:

A 10 dB/sweep power sweep mode is selected and the resultant is displayed on the 8755C Swept Amplitude Analyzer. Output of the Power Sweep circuit is adjusted for the correct sweep.

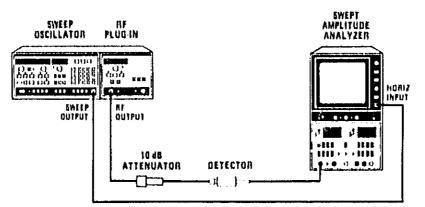


Figure 5-37. Power Sweep Test Setup

EQUIPMENT:

Swept Amplitude Analyzer Display Mainframe	HP 8755C HP 182T
Detector	HP 11664B -
10 dB Attenuator,	HP 8350A

Model 83590A

Adjustments

ADJUSTMENTS

5-29. POWER SWEEP (Cont'd)

PROCEDURE:

NOTE

ALC gain adjustments (paragraph 5-27) must be checked before power sweep adjustment is made.

NOTE

This procedure requires that A3S1 is not to the factory-net position (Table 5-6), and that the B350A Sweep Oscillator, 27.8 kHz square wave modulation is selected.

- 1. Connect equipment as shown in Figure 5-37. On the 8350A, press INSTR PRESET ☐ MOD . Allow the equipment to warm ap for 1 hour.
- 2. On the 8350A, press SHIFT CW .
- 3. On the 83590A, press POWER LEVEL. Then, on the 8350A, press 0 dBm.
- 4. On the 83590A, press POWER SWEEP . Then, on the 8350A, press $\beta=0-dB$.
- 5. While observing the 8755C display of the RF output, adjust A5R50 (PWSP) for a power level change across the display of 10 dB (10dB/sweep). Refer to Figure 5-38 for the adjustment location.

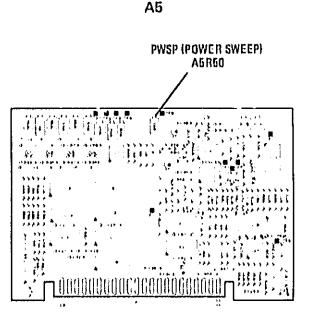


Figure 5-38. Fower Sweep Adjustment Location

5-30. FM DRIVER

REFERENCE

Performance Test: Paragraph 4-20 Service Sheet: A5

DESCRIPTION:

The FM Driver high frequency offset is adjusted for zero volt drive with no FM modulation applied. A delay-line discriminator is used to detect and display FM modulation on an oscilloscope. Adjustments are for best overall frequency response from DC to 10 MHz. Compliance to a supplemental characteristic $\sigma/\pm 3$ dB FM flatness is checked between DC and 2 MHz.

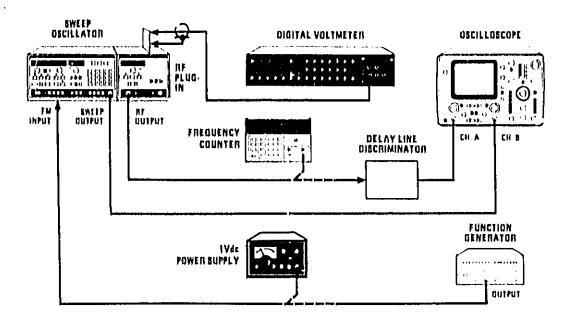


Figure 5-39. Test Setup for FM Driver Adjustments

EQUIPMENT:

Digital Voltmeter (DVM)		HP 3456A
* elny Line Discriminator.		Figure 1-3
Frequency Counter		HP 5343A
DC Power Supply		HP 6213A
Sweep Oscillator	· • • • • • • • • • • • • • • • • • • •	HP 8350A

Model 83590A

Adjustments

ADJUSTMENTS

5-30. FM DRIVER (Cont'd)

PROCEDURE:

NOTE

Turn AC power OFF when removing or installing PC boards.

NOTE

This procedure requires that A3S1 is set to the factory-set position (refer to Table 5-6).

FM Offset

- 1. Connect the equipment as shown in Figure 5-39. Connect the Frequency Counter to the 83590A RF OUTPUT connector. Do not connect the Power Supply or Function Generator to the 8350A rear panel FM INPUT connector yet. Allow the equipment to warm up for 1 hour.
- Connect the DVM between A5 pin 21 and A5TP7 (HIGH FREQ FM RET). Refer to Figure 5-40 for adjustment procedure locations. Adjust A5R19 (FM OFFSET) for a DVM reading of 0.000 ±0.001 Vdc.

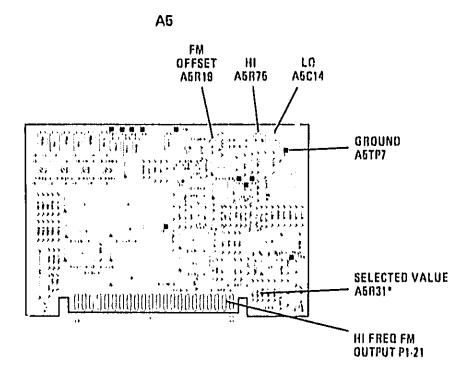


Figure 5-40. Location of A5 FM Driver Adjustments

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Adjustments

Model 83590A

ADJUSTMENTS

5-30. FM DRIVER (Cont'd)

3. Disconnect the DVM and set the equipment controls as follows:

B350A SWEEP OSCILLATOR

CW FREQUENCY		GHz
FREQUENCY Sweep Mode	Press SHIFT CW (swept	CW)
CW VERNIER		ON
SWEEP TRIGGER		
RF BLANK		OFF

83590A RF PLUG IN

POWER LEVEL	+10 dBm	
CW FILTER	OFF	
ALC MODE	INT	

Configuration switch A3S1 on Digital Interface board (Table 5-6) set as follows:

Switch Position	1	2	3	4	5	6	7	8
Position	0	x	Х	0	Q	0	*	0

Positions: 1=Open; 0=Closed; X=Don't care * "0" if no Option 002; "1" if Option 002 installed.

NOTE

The A361 switch positions select the 83580A code, maximum RF power at power-up, -20 MHz/V FM sensitivity, cross-over coupled FM modulation (AC coupled), and C, ition 002 code (if installed).

3312A FUNCTION GENERATOR

RANGE	IMHz
FREQUENCY	
FUNCTION	
Amplitude	Set output for 100 mV p-p
	s displayed on Oscilloscope
	with 50 Ohm input

1740A OSCILLOSCOPE

MODE	A vs. 1	3
	50 Ohm	
	V/DIV	
	NPUT	
CHANNEL B	//DIV	l

Model 83590A

Adjustments

ADJUSTMENTS

6-30. FM DRIVER (Cont'd)

Frequency Response

- 4. Connect the Frequency Counter to the 83590A RF OUTPUT. Connect a +1 Vde power supply to the 8350A rear panel FM INPUT. A shift in frequency of approximately -20 MHz should occur on the Frequency Counter when +1 Vde is applied. (This shows correct FM modulation sensitivity.) Connect the Delay Line Discriminator to the 83590A RF OUTPUT and connect the Function Generator to the 8350A rear panel FM INPUT connector.
- Adjust the 8350A CW FREQUENCY and CW VERNIER for a waveform at the center of the oscilloscope CRT. Adjust the oscilloscope Channel A CAL control for a trace 4 divisions high centered on the CRT.
- Manually sweep the Function Generator frequency from DC to 100 kHz. Select resistor A5R31 so that the amplitude of the CRT waveforms at Function Generator frequencies of 100 Hz and 100 kHz are the same ±0.2 divisions on the CRT. Refer to Figure 5-40 for A5R31 location. Refer to Table 5-3 for the allowable range of values for A5R31.
- Manually sweep the Function Generator frequency from DC to 10 MHz. Adjust A5C14 (LO) and A5R75 (HI) controls to obtain the most constant overall response from DC to 10 MHz. Repeat this step several times.
- 8. Check that the ± 3 dB FM flatness supplemental characteristic is met between DC and 2 MHz as follows. Manually sweep the Function Generator frequency between DC and 2 MHz. On the oscilloscope, note the maximum and minimum response points as shown in Figure 5-41. Maximum point (+3dB) can be up to 5.6 divisions, and minimum point (-3 dB) can be down to 2.8 divisions.

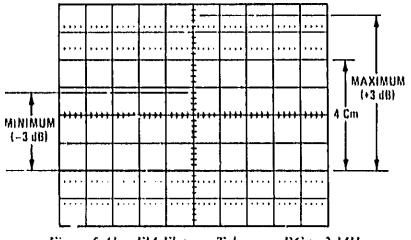


Figure 5-41. FM Flatness Tolerance, DC to 2 MHz

- If the FM flatness supplemental characteristic in step 10 above is not met, repeat steps 8 and 9 above and make compromise adjustments in the DC to 2 MHz range to meet the requirements.
- 10. Reset the A3S1 Configuration Switch as indicated in Table 5-6.



Model 83590A

6-1. INTRODUCTION

6-2. This section contains information for ordering parts. Table 6-1 lists the available exchange assemblies. Table 6-2 lists abbreviations used in the parts list and the names and addresses that correspond to the manufactuzers' code numbers. Table 6-3 lists all replaceable parts in reference designator order.

6-3. EXCHANGE ASSEMBLIES

6-4. Table 6-1 lists assemblies within the instrument that may be replaced on an exchange basis, thus affording a considerable cost savings. Exchange, factory repaired and tested assemblies are available only on a trade-in basis; therefore, the defective assemblies must be returned for credit. For this reason, assemblies required for spare parts stock must be ordered by the new assembly part number.

6-5. ABBREVIATIONS

6-6. Table 6-2 contains three major sections: Reference Designations expands the designators used in the parts list: Abbreviations defines all abbreviations used in the descriptions of replaceable parts; Manufacturers Code List references the name and address of a typical manufacturer with the code number provided in the parts list.

6-7. REPLACEABLE PARTS LIST

6-8. Table 6-3 is the list of replaceable parts and is organized as follows:

- a. designation.
- b. order by reference designation.
- Miscellaneous parts. С.

SECTION VI REPLACEABLE PARTS

Electrical assemblies and their components in alpha-numerical order by reference

Chassis-mounted parts in alpha-numerical

6-9. The information given for each part consists of the following:

- a. The Hewlett-Packard part number.
- b. Part number check digit (CD).
- e. The total quantity (Qty) in the instrument.
- d. The description of the part.
- e. A typical manufacturer of the part in a fivedigit code.
- f. The manufacturer's number for the part.

6-10. The total quantity for each part is given only once – at the first appearance of the part number in the list.

NOTE

Total quantities for optional assemblies are totaled by assembly and not integrated into the standard list.

6-11. ILLUSTRATIONS

6-12. Figure 6-1, Mechanical Parts, provides the location of the replaceable mechanical parts listed in Table 6-3. These parts are denoted with reference designation prefix "MP". Figure 6-2, Attaching Hardware, references the Hewlett-Packard part number for the hardware used, with at least one location within the instrument. Figure 6-3 provides an exploded view of the front panel RF output connector and lists the Hewlett-Packard part number for all replaceable items.

6-13. ORDERING INFORMATION

6-14. To order a part listed in the Replaceable Parts List, quote the Hewlett-Packard part number with its check digit (CD), indicate the quantity, and address the order to the nearest Hewlett-Packard office. The check digit will ensure accurate and timely processing of your ordei.

6-15. To order a part that is not listed in the Replaceable Parts List, include the instrument model number, instrument serial number, description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-16. SPARE PARTS KIT

6-17. Stocking spare parts for an instrument is

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often done to ensure quick return to service after a malfunction occurs. Hewlett-Packard has a "Spare Parts Kit" available for this purpose. The kit consists of selected replaceable assemblies and components for this instrument. The contents of the kit and the "Recommended Spares" list for this instrument may be obtained on request and the "Spare Parts Kit" may be ordered through your nearest Hewlett-Packard office.

Reference Designation	New Pert Number	Rebuilt-Exchange Part Number	Description
A12	5986-7341	5086-6341	Switched YTM
A13	5086-7335	5086-6335	YO 2.0 to 7.0 GHz
A14	5086-7342	5986-6342	Power Amp. 2.0 to 7,0 GHz
		NOTE	<u> </u>
	For module ex	change procedure, see Sect	ion VIII.

Table 6-1. Exchange Parts

Table 6-2.	Manufacturers Code List, Reference Designations, and Abbreviations (1-of 3)
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	MANUFACTURERS CODE	LIST	
MFR. No.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000 0003J 0004G 01121 01295 02111 03888 04713 06001 066665 07263 11236 06066 17856 17856 18324 19701 24355 24546 25058 27014 28480 30983 32997 34371 34649 51642 56289 72136 73138	ANY SATISFACTORY SUPPLIER NIPPON ELECTRIC CO UNITRODE COMPUTER PRODUCTS CORP ALLEN-BRADLEY CO TEXAS INSTR INC SEMICOND CMPNT DIV SPECTROL ELECTRONICS CORP KDI PYROFILM CORP MOTOROLA SEMICONDUCTOR PRODUCTS GE CO ELEK CAP & BAT PROD DEPT PRECISION MONOLITIES INC FAIRCHILD SEMICONDUCTOR DIV CTS OF BERNE INC SPRAGUE ELEC CO SEMICONDUCTOR DIV SILICONIX INC SIGNETICS CORP MEPCO/ELECTRA CORP ANALOG DEVICES INC CORNING GLASS WORKS (BRADFORD) SIEMENS CORP NATIONAL SEMICONDUCTOR CORP HEWLETT-PACKARD CO CORPORATE HQ MEPCO/ELECTRA CORP BOURNS INC TRUMPOT PROD DIV HARRIS SEMICON DIV HARRIS-IN TERTYPE INTEL CORP CENTRE ENGINEERING INC SPRAGUE ELFCTRIC CO ELECTRO MOTIVE CORP SUB IEC BECKMAN INSTRUMENTS INC HELIPOT DIV	MILWAUKEE V DALLAS T CTTY OF IND C WHIPPANY N PHOENIX A IRMO S SANTA CLARA C MOUNTAIN VIEW C BERNE H CONCORD N SANTA CLARA C SUNNYVALE C MINERAL WELLS T NORWOOD N BRADFORD P ISELIN N SANTA CLARA C PALO ALTO C SAN DIEGO C RIVERSIDE C MELBOURNE F MOUNTAIN VIEW C STATE COLLEGE P NORTH ADAMS M WILLIMANTIC C	AA S3204 YI 53204 YX 75222 YA 91745 YJ 07981 YZ - 85062 29063 YA 95050 YA 94042 N 46711 SH 03301 YA 95054 YA 94086 YA 94086 YA 94086 YA 95051 YA 95051 YA 95051 YA 92507 YA 925051 YA 95051 YA 95051 YA 96026 YA 92634

Table 6-2. Manufacturers Code List, Reference Designations, and Abbreviations (2 of 3)

Α.,	Assembly
	Alienuator, Isolator,
	Limiter, Termination
Civ	Capacitor
	Diode, Diode Thyristor, Step ecovery Diode (SCR), Varactor
	Directional Coupler
DS.	Annunctator, Lamp, Light aitting Diode (LED), Signaling
	 Device (Audible or Visible)
E	Miscellaneous
F	Hectrical Part

٨

A Across Flats, Acrylic,
Air (Dry Method), Ampere
ADJ Adjust, Adjustment
ALC Alcohol.
Automatic Level Control
AMP Amperage
AMPL Amplifier
ANLG Analog
ASSY Assembly
ASTBL Astable
ATTEN Attenuation,
Attenuator
AWG American Wire Gage

B

BD	Board, Bundle
	. Baume, Beryllium
BFR	Before, Buffer
BLK	Black, Blank, Block
BNC	. Type of Connector
BSC	Basie
BVR	Reverse Breakdown
	Voltage

С

C Capacitance, Capacitor, Center Tapped, Centistoke,
Ceramic, Cermet, Circular
Mil Foot, Closed Cup,
Cold, Compression
CBL Cable
CER Ceramie
CH Center Hole
CHAM Chamfer
CHAN Channel

REFERENCE	DESIGNATIONS
------------------	--------------

FL Filter
House concerns that Hardware
Junior Electrical Connector
(Stationary Portion), Jack
Relay
L
MP Miscellaneous
Mechanical Part
Production Electrical Connector
(Movable Portion), Plug
Q Silicon Controlled Rectifier
(SCR), Transistor,
Trinde Thyristor
R Resistor

ABBREVIATIONS

COAX Coaxial
COM Commercial, Common
CONN Connect.
Connection, Connector
CONT Contact, Continuous,
Control, Contro Her
CONV Converter
CP Cadm/um Plate,
Candle Power, Cantipoise,
Conductive Plastic, Cone Point

D

D Deep, Depletion,
Depth, Diameter, Direct Current
D/A Digital-to-Analog
DAP Diallyl Phthalate
DB Decibel, Double Break
DC Direct Current,
Double Contact
DBL
DCDR Decoder
DEG Degree
DIA Diameter
DIFF Differential
DIP Dual In-Line Package
DO Package Type Designation
DRVR Driver

E

E... Enamel (Insulation, Enhancement, Extension) E-MODE... Enhancement Mode EPROM.... Eraseable Programmable Read Only Memory EXCL Excluding, Exclusive EXT.... Extended, Extension, External, Extinguish

and the second second second second second

5	Switch
1	Transformer
JP	a a success of the point of the
$\mathbf{D}_{1,1}$	a constant Integrated Circuit,
	Microcircuit
VR	 Breakdown Diode (Zener).
	Voltage Regulator
W	Cable
	Transmission Path, Wire
	o de la composition de Speker
$\mathbf{Y}_{i,i}$	 Crystal Unit:
	(Piezoelectric, Quartz)
2	Tuned Cavity, Tuned Circuit

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For Contract Fahrenheit, Farad.
Female, Film (Resistor), Fixed,
Flange, Flint, Fluorine, Frequency
FEM Female
FF Flange, Female
Connection: Flip Hop
FM Flange, Male Connection.
Foam, Frequency Modulation
FT Current Gain Bandwidth
Product (Transition Frequency);
Feet, Foot
FXD Fixed

G

GEN	
	Generator
GL	Glass
GP General	Purpose, Group

\mathbf{H}

H Henry, Hermaphrodite, High, Hole Diameter, Hot, Hub Inside Diameter, Hydrogen HD Hand, Hard, Head, Heavy Duty HEX Hexadecimal, Hexagon, Hexagonal

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IC	Collector Current,
	Integrated Circuit
ID	Identification,
	Inside Diameter

Table 6-2. Mantyacturers Code 1.18, Reference Designations, and Abbreviations (5-0)-57				
DF Forward Current.	N	5		
Intermediate Frequency	N-CHAN N-Channel	SUR Screw, Scrub,		
IMPD Impedance	N-CIIAN	Silicon Controlled Rectifier		
IN Inch, Indium	Metal Oxide Semiconductor	SGL		
INP Input	NO Normally Open, Number	SHIFT		
INT Integral.	NPN Negative	SL Silicon, Square Inch		
Intensity, Internal	Positive Negative (Transistor)	SIG Signal, Significant		
INTL Internal, International	NS Nanosecond,	SIP Single In-Line Package		
INV Inven, Invener	Non-Shorting, None	SKT Skin, Socket		
		SLDR Solder		
1	O	SM Samarium, Seam,		
		Small, Square Meter,		
IFET Effect Transistor	OCTL Octal	Sub Modular, Sotominiature		
	OD Olive Drab,	SMB Subminiature,		
к	Outside Diameter	B Type (Snap-On Connector)		
ha hath he contra	OP Operational	SQ Square		
K Kilo, Potassium	OPT Optical, Option, Optional	STL Steel		
KB Kaob	OXD Oxide	52 Size		
	n	r		
h.	p	TA Ambient		
	PC Picocoulomb.	Temperature, Tant aum		
LED Light Emitting Diode	Piece, Printed Circuit	TC Thermoplastic		
LG Length, Long	PCB Printed Circuit Board	THD Thread, Threaded		
LIN, Linear, Linear Taper,	PD Pad, Palladium, Pitch	THR Thick		
Linearity LK Link, Lock	Diameter, Power Dissipation	TO Package Type		
	PKG Package	Designation, Troy Ounce		
LKG Leakage, Locking LKWR Lockwasher	PL Phase Lock.	TPL Triple		
LS., Loudspeaker, Low	Plain, Plate, Plug	TRIG Trigger, Triggerable,		
Power Schottky, Series Inductance	PLSTC Plastic	Trigeering, Trigonometry		
LUM Luminous	PNP Positive Negative	TRMR Trimmer		
Prostate entry and a second seco	Positive (Transistor)	TRN Turn, Turns		
M	POLYE	TTL Tan Translucent.		
(\$)	POS Position, Positive	Transistor Transistor Logic		
M * Jale, Maximum. Mega,	POZL Pozidriv Recess	u		
Mil, Milli, Mode, Momentary,	PRCN Precision	UNCT Undercut		
Mounting Hole Centers,	PRP Purple, Purpose	UF Microfarad		
Mounting Hole Diameter	PT Part. Pint.	OF STREET, STREET, DUCIDING		
MA Milliampere	Platinum, Point, Pulse Time	v		
MACH Machined	PVC Polyvinyl Chloride	V Vanadium, Variable,		
MAX Maximum	PW., Power Wirewound,	Violet, Volt, Voltage		
MCD Millicandela	Pulse Widtn	VA Volt Ampere		
MICPROC Microprocessor	0	VDC Volts. Direct Current		
MISC Miscellaneous	Q	VID Video		
MLD Mold, Molded	QUAD Set of Four	33.0		
MM Magnetized Material	• • • • • • • • • • • • • • • • • • • •	W Water Manager		
(Restricted Articles Code);	R	W Walt, Wattage,		
Millimeter		White, Wide, Width, Wire		
MOD Model, Modified,	RES Research, Resistance,	WB Wide Band		
Modular, Modulated, Modulator	Resistor, Resolution	WD Width, Wood		
MOSFET Metal Oxide	KET Retaining	х		
Semiconductor Field	RF Radio Frequency	XSTR Transistor		
Effect Transistor	RGLTR Regule for			
MTG Mounting	RKR Rocker	Ŷ		
SITR Meter	RND Round	YTM YIG Tuned Multiplier		
MULTIPLNR Multiplexer	RPG Rotary Pulse Generator	2		
MUW Music Wire MW Milliwatt	RR	Z ZNR Zener		
176 77 15				

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Table 6-2. Manufacturers Code List. Reference Designations, and Abbreviations (3 of 3)

Replaceable Parts

Reference Designation	HP Part Nur ber	0 0	Qty	Description	Mfr Code	Mir Part Number
A1	83840-80008	7	1	NOAND ABBEMBLY FRONT PANEL (DOEB NOT INCLUDE ATHMST ROTARY MILEE GENERATION)	89480	83840 SCOOR
A1C1 A1C7 A1C3 A1C4 A1C4 A1C6	0160 4084 0180 3811 0180 4084 0180 4084 0180 4084	件 7 日 社 社	01 1 1	CAPACITUR FAD TUP ATON BOVIC CER CAPACITUR FAD TOUT ATON BOVIC CER CAPACITUR FAD TUP ATON BOVIC CER CAPACITUR FAD TUP ATON BOVIC CER CAPACITUR FAD TUP ATON TOVIC TA	算数本的() 算数本的() 算数本的() 算数本数() 算数本数()	0160 AUBA 0180 781 1 0160 4084 0160 4084 9160 4084
A1051 A1053 A1053 A1053 A1055 A1055	1890-0487 1890-0487 1890-0670 1890-0670 1890-0670	7700) 6	NOT ASSIGNED LED LANP LUM (NT=1NCD IF=50MA MAS BVH=6V LED LANP LUM (NT=1NCD IF=50MA MAS BVH=6V LED LANP LUM (NT=1NCD IF=50MA MAS BVH=6V LED LAMP LUM (NT=1NCD IF=50MA MAS BVH=6V	28480) 28480) 28480 28480	6082-4684 6082-4684 6082-4160 6082-4160
A1060 A1067 - A1061 3	1090-0406	0	1	led lang frights incorptions war bring a Not assights	384B()	6()#3-#6#4
A10514 A10516	1890 6670	0		LED LAMP LUM INT=THEO IT=TOMA MAX BVN=BV LED LAMP LUM INT=THEO IT=TOMA MAX BVN=BV	28480 28480	6082-4960 6082-4960
A10518 A10517 A10518 A10519	1990 0670 1990 7699 1990 0699 1990 0699	0 3 3 3	3	LIDIAMP UMINIPINO IPIDMA MAX BUR-BU IIDIGHT BAR MODULI UMINIPINO IIDIGHT BAR MODULI UMINIPINO IIDIGHT BAR MODULI UMINIPINO	78460 98480 78480 78480 78480	EUN7-4160 1681-4360 1681-4360 1684-3360
ALUI Almini	1261-4822	$ \cdot $	3	CONNECTION BUILTIN M POST TYPE	JN 480	1261-4827
Albp3 Albp3 Albp4 Albp4 Albp5 Albp3	2860-0008 2180-0087 0280-1233	נ 4 5	1 1 2	NOT AUGIGATO NUT-HER (DE CHAN 1/4-22-THO-084-IN-THR NOT AGGIGATO VAGUERAR INTL T 1/4 IN-EBU-IN-IC GRACER BEFCIALTY 480 IN 14 - 178 IN OD	00000 28480 00000	orofn dy depeniality 2180 dog 2 Groen dy depeniality
A181 A187 A183 A184	0698-3444 2100-3786	۰ ۲	L	ngt Abbighed Negistum 316 f.%. 136W f TC=02 foo Not Asbighed Nebistum-van Control CP fok to% lin	34648 38480	C4-1/8 10 3168 7 2100 3268
A) NB A) NB A) NB A) NB A) NB	0698-8820 3757-0398 0757-0398 0757-0398	7 4 4	1	NUT ASSIGNED RESISTOR 4 84 1% 186W FTC=03 100 RESISTOR 76 1% 186W FTC=03 100 HESISTOR 76 1% 186W FTC=03 100 RESISTOR 76 1% 186W FTC=03 100	78480 74548 74548 74548 74548	0888-8870 64-1-8-10-7810 64-1-8-10-7810 64-1-8-10-7810 64-1-8-10-7810
ATRICE	6060-8444	,	۱	NOTARY PULSE GENERATOR	28480	LCOU BAAA
A181 A182 A183 V184 A188	5060-9438 5070-9438 5050-9438 5050-9438 5050-9438	77777		Publikutton Bwitch PC Wount Publikutton Bwitch PC Wount Publikutton Bwitch PC Wount Publikutton Bwitch PC Mount Publikutton Bwitch PC Mount	28480 28480 28480 28480 28480 28480	6060 8436 6080 8436 6080 8436 6080 8436 6080 8438
A)65- A1511	****			NOT ABBIGNED		
A1612 A1613 A1614	6060-8436 6060-8438 6060-0435	;;		ривнвиттон бултен ре-моинт Рибнвиттон бултен ре-моинт Рибнриттон бултен ре-моинт	28480 28480 28480 28480	5060 8436 5060 8436 5080 8436
A1U1 A1U2 A1U3	1810 0174 1890 0738 1810 0403	0 }	; [NETWORK NES 15 DIPJOO O DHM X 8 Display-num seg 5 char 187-u Ned Network-Nebistor N1-R15 JJD DHM 23%	28480 28480 01121	1810-0174 1840-0728 3168-231
A1>D517 A1>D518 A1>D518	1700 0901 1700 0901 1700 0901	? ?	1	SOCRET-BTRP # CONT SIP DIMBLDN SOCRET-BTRP # CONT SIP DIMBLDR SOCRET-BTRP # CONT SIP DIMBLDR	78480 78480 78480	1200-0801 1200-0801 1200-0801
tutia	1261-8828	6	- 1	CONNECTOR IS PIN M POST TYPE	38480	1261-842#
A3 A3C1	83580-60067 0160-4084			BOAND ABBEMPLY BUB PANEL	28480	N3N80-80087
AJCJ AJCJ AJCJ AJCA	0160-4084 0160-4084 0160-4084	#1 #1 #1		CAPACITOR FAD. TUF 210% EOVIDC CEN CAPACITOR FAD. TUF 210% EOVIDC CEN CAPACITOR FAD. TUF 210% EOVIDC CEN	28440 28460 28460 28460	0120-4084 D120-4184 D120-4184 D120-4184
AJCB	0160-0174	8	•	NOT ASSIGNED CAPACITOR FRO ATUF +80-JUN JBVDC CEN	38480	0160-0174
	0100-3870	;	28	CAPACITOR FRD 10F 130% BOVDC CER CAPACITOR FRD 010F 130% TOOVDC CER CAPACITOR FRD 33PF B% 300VDC CER 0130	2#480 2#480 3#480	0180-1084 0180-3878 0180-3875
AJCRI AJCRJ	1801-0033 1801-0033	;	10	DIOUS-GEN PHP LEOV TOUMA DO-T DIODE-GEN PHP LEOV TOUMA DO-T	28480 28480	1801-0033 1011-0033
AJCHA AJCHA AJCHB	1801-0033	2		DIODE-GEN FAP TROV JOONA DO-J NOT ASSIGNED NOT ASSIGNED	28480	1941-0022
A3CR6 A3CR7	1801-0023 1801-0023	3		Diode Jen Prp 1807 Joona Do-J Diode Jen Prp 1807 Joona Do-J	7#480 7#480	1901-0033 1901-0033
셨다	1261-4827	,		connector eq pin m post type hat assightly	28480	1261-4827
			- Faa	introduction to this section for ordering information		

Table 6-3. Replaceable Parts

See introduction to this section for ordering information *Indicates factory selected value

Model 83590A

Reference Designation	HP Part Number	0 D	Qty	Dascription	Mfr Code	Mfr Part Numbor
<u>AIL?</u>	1200 0508 0490 0918	0) 11	;	SIX RET IC LE CUPET DIP BERN HELAY REED TA BOOMA LOOVING BVING CENL	78480) 48480	1 POO ORDU QABO ODIN
A7L1	0100-1010	•	1	induction in ciral denne for	2848()	8100-1018
AJNFI AJNFJ AJNFJ AJNFA	0380 0773 0380 0773 0380 0773 0380 0773	0 0 0 0	•	6 BPACEN INVEON 6 IN 43 164 IN 10 BPACEN INVEON 6 IN 43 165 IN 10 BPACEN INVEON 6 IN 43 165 IN 10 BPACEN HVT ON 6 IN 43 165 IN 13	00000 00000 00000	01074 By CESCEPTION 01074 By CESCEPTION 01074 By CESCEPTION 01054 By CESCE07005
A3P1	1961 B491	'	ŧ	COMMECTOR 26 PH F 1981 TYL	284BD	1763-6405
A201 A202 A203 A203 A204	1864-0474 1863-0318 1864-0474 1865-0473	4 1 4 0	٢	пального крыто в го-2 наму га - нолна Пальнатов кнаг гар то-2000му га нолна Пальнатов как в го-2 нолжу га нолна? Пальнатов мозгат в сная г-моот	04713 78480 04713 17850	pheadi 1863 usia pheadi Vilukm
A3H1 A3H3 A3H3 A3H4 \3H6	7100 3056 0757 0389 0698 3788 7100 3109 0757 0485	8 1 1 7 1 7	1111	NY DIGNON YINGH AN TONIC DIOL (ADV 17-TNN NY DIGNON YI DA YIN YY DWY TICHOR TNO NY DIGNON YI DA YIN YY DWY TICHOR TNO NY DIGNON-TNGHI YIN TONIC DIOL (ADV 17-TNN NY DIGNON-TNGHI YIN TONIC DIOL (ADV 17-TNN NY DIGNON-TNGHI YIN TONIC DIOL (ADV 17-TNN)	07111 24648 24648 32887 34648	43F607 C4 V # 10 F1677 C4 V # 10 F1677 300F1-707 C4 V # 10 1003 F
аўны Азні Азні Азні Азні	\$10033064 036704403 0608-2461 07630560 0763-0560 0763-0442	n 7 0 3 9	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	мерібніли-тили вок тож с виле Ард Гелики и бібліли у билі та Тариустісторатора и бібліли тари талі тариустісторатора и бібліли талі тариустісторатора и бібліли ток талі тариустісторатора	07111 74648 74648 74648 74648	43PE03 C4-128-103E01-7 C4-128-1035333 C4-128-103001-7 C4-128-1030023
A3M11 A3M12 A3M13 A3M13 A3M14 A3M16	07670173 0698-3163 0698-3431 0767-0438 0698-3166	3 U 5 3 2	7 J D A	$\begin{array}{l} H(5)(51)(1)(34)(1)(1)(1)(1)(1)(1)(1)(1)(1)(1)(1)(1)(1)$	28480) 24646 1)3888 24646 24646	0767-0123 C4 1 / 8-T0 3831-7 PM166-1 / 8-T0 7287-7 C4 1 / 8 T0 5 L1 1 C4-1 / 8 T0 1472 7
AJNIN AJNIF AJN 8 AJN 8	0767 0465 0767 0789	15 2	r	NOTASSISHED NEISTON ROOK IN, I JAWY TC=02 100 NEISTOR I JAN IN, I JAWY TC=02 100 NOTASEISHEI	24646 19701	64-128-116-1003-8 19746-128-116-1337-8
A3875	0767 0442	5		NEELSTUR TOK THE TRAVET TOHOTOO	74640 74640	C4-328 10-1002 1
A3N33 A3N33 A3N33 A3N33 A3N3A A3N3B A3N3B	0767-0465 0767-0465 2100-3054 0698-7760 0698-7760 0698-7760 0698-7770	6 6 7 7 6	ť	н бібілі норк іж. Ізбуу Іс-оз Іоо ні бібілі порк іж. Ізбуу Іс-оз Іоо на бібілі тамія вок Гох с біді-лі). Ізтіку ні бібілі пок іх. Обуу Іс-оз Іоо ні бібіля Іок іх. Обуу Іс-оз Іоо на бібіля біт іх. Обуу Іс-оз Іоо на бібіля біт іх. Обуу Іс-оз Іоо	74640 07111 74640 74640 74640	C4-1/B 10-1003 / C4-1/B 10 1003 / C3-1/B 10 1003 / C3-1/B 10 1002 0 C3-1/B 10 1002 0 C3-1/B 10 611H 0
A21P1 A21P2 A21P3	d£d0 0810 8560 0850 8560 0850 8560 0850	0 0 0	10	TERMINAL TEST MINIT PCD TERMINAL TEST MINIT PCD TERMINAL TEST MINIT PCD	00000 00000 00000	i adea av debcription Gadea av debcription Gadea av debcription
A3U1 A3U2 A3U3 A3U3 A3U4 A3U6	1876-0097 1858-0047 1858-0047 1870-1416 1870-1730	0 0 1 1	3 5 6 4	IC OP AMP OP INIAL TO BE PAD TRANSISTOR ARIAN TO PHY PLATC OP TRANSISTOR ARRAY TO PHY PLATC OP IC SCIENTET THE TILL SERVICE TRIG COM IC FF TTLLS D-TYPE PAG-EDGE-TRIG COM	78480 13606 13606 01785 01785	1878 0002 ULN 7003A ULN 7003A Shy74654M Shy746543M
AJUS AJUJ AJUB AJUS AJUS AJUS	1870-7760 1870-1730 1870-1730 1870-1730 1876-0417 1868-0049	6 6 6 6 1	1 D	ic Nicitioc-Accebb NM05 IC PF TELES D-TYPE POB EDGE-TRIG CDM IC PF TELES D-TYPE POB EDGE-TRIG CDM IC FY TELES D-TYPE POB EDGE-TRIG CDM IC SYNTCH ANLE ODAD 16 DIP C FRG TRANSIBTUR ARRAY 16 INN PLSTC DIP	34E40 01996 01996 21014 13606	D4779-5 647465734 647465734 1213320 121-3320 121-78034
A3017 A3017 A3007	1810 0268 1876 0205 8159 0005) 0 0	ł	NETWORK-NEB (6-51910 OK OHM K 8 10 TIMEN 13 WARE JJAWAS W PVC 1132 BIX	0112 18324 28480	7064103 NEBBA REB 0006
EA.	83380 80007	•		BOAND ABBEMBLY DIC NT	28480	N3880 80007
A3C1 A3C7 A3C3 A3C4 A3C6	0160 0127 0180 0127 0180 0127 0180 0127 0180 0127 0180 3537	****	8	CAPACITUR FAD TUF 170X 26VDC CLR PAPACITUR FAD TUF 170X 26VDC CLR CAPACITUR FAD TUF 170X 36VDC CLR CAPACITUR FAD TUF 170X 36VDC CLR CAPACITUR FAD 880PF 15X 110VDC NICA	38480 38480 38480 38480 38480 38480	01600177 016001377 016001377 016001377 0160013537
AJCO	0140-0500	1	1	CAPACITOR/FED 4701, 70% 7050C TA	38480	0180 0500
A311 A314F1	1251-4827 E040-6852	1	•	CONNECTOR BO-PSN M AUST TYPE	78480	1261-4827
AJAP	1000 8046	1	1	татвастоя. Влаљи Ехтрастов рук D31 воаро	78480 78480	6040-6867 6000-9046
AJH1 AJH7 AJH3 AJH4 AJB1	07670478 0698-3163 0698-3163 0698-3163 0698-7717 3101-7743	1 9 6 6	1 4 1	РЕБІВІОН І ВІА ІЪ, ІЗБИУ Г ІС+03 100 ПЕБІБІОН З ВЗА ІЪ, ІЗБИУ Г ІС+03 100 РЕБІВІОН З ВЗА ІЪ, ІЗБИУ Г ІС+03 100 НЕБІБІОН ІОО ІЪ, ОБУУ Г ІС+03 100 БУИТСН-КАН ПІР НАЛ АББУ В-1А, ОБА ЗОУОС	74648 74648 74648 74648 74648 78680	C4-1/8-T0-1871-7 C4-1/8-T0-3831-7 C4-1/8-T0-3831-7 C4-1/8-T0-3831-7 C3-1/8-T0-10018-0 3101-7743
1024 5025 4024 4024 4025	83890 8000 83890 800 02 1828 0389 1820 7041 1820 7041 1820 7006	73070 070		IC-NMUS 32K EFROM PROGRAMMED IC-NMUS 32K EFROM PROJRAMMED IC TIMER TTL MUNU/ASTRL IC TIMER TTL MUNU/ASTRL IC TIMER NMOS	78480 78480 01795 04713 00075	83890 80001 83890 80003 ht888 Mc68831P UP08363D

Table 6-3. Replaceable Parts

See introduction to this section for ordering information *Indicates factory selected velue

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Reference Designation	HP Part Number	0	Qty	Description	Mir Codo	Mir Port Number
A3U8 A3U8 A3U8 A3V8 A3V8 A3V10	1870-1707 1870-1107 1870-1107 1870-1418 1870-1418	10010	1 3 1	IC GATE TTLLE NAAD ITL 3 DP IC GATE TTLLE NAAD GUAD 2 DP IC GATE TTLLE NAAD GUAD 2 DP IC SCONTT - TROJ TLLE DV DLA L DP IC SCONTT L 53 - TD 8 DAT 3 DP IC SCONDETTL 15 - TO 8 DAT 3 DP	01705 01705 01705 01705 01705	6477456104 6477456004 6477456144 647456144 647456144
A3U11 A3U17 A3U13 A3U13 A3U14 A3U16	3820-1418 1810-0238 1820-1238 1820-1403 1820-1418	0110	1 1	IC SCHAILT-THUS THE IS HY HES A HIP ALTWORK-REB AD DRAGOD ORM & B IC BEDR THE IS 3-10 BENAL 3 HIP IC BEDR THE IS 3-10 BENAL 3 HIP IC BEDR THE IS NOT HER HIP IS A HIP	01706 13238 01706 01706 01706	5N 141 61 AM 181 - 3 H Luù 5N 144 61 38N 5N 141 63 J AN 5N 141 61 AN
A3U18 A3U17 A3U18 A3U18	1810 0336 1870 7076 1870 7076 1810 0338	;	;	АЛУЧНА ЛЕБ 18-001000 ОНА 8 В IC MISC 111 15 IC MISC 113 15 IC MISC 113 15 АЛУЧНА НЕБ 18 101000 ОНА 8 В	11736 01786 01786 11736	161-3 MIDO 61/14163480 61/14163480 51/14163480 701-3 MIDO
*	Fages cases	•		BOARD ABBEWELY ALC	28480	#3880 appas
ААСІ А427 А423 ААСЗ ААСА ААСВ	0350 0177 0180 0274 0180 0274 0180 0274 0180 0274 0180 0274	2	•	CAPACITOR FED THE ETOX FAVOR CER CAPACITOR FED TOUT FIDS, TONIC TA CAPACITOR FED TOUT FIDS, TONIC TA CAPACITOR FED TOUT FIDS, TONIC TA CAPACITOR FED TOUT FIDS, TONIC TA	38480 68280 68280 68280 68280 68280 68280	1160 0*77 15001058007087 18001058007087 18001088007087 18001088007087
А4СВ А457 А458 А458 А458 А4510	0160 3879 0160 4084 0160 4084 0160 3871 0160 3879	7 11 15 11 1	,	CAPACITOR FAD OTUP 170% TOOVIC CER CAPACITOR FAD TUP FOX BOVIC CER CAPACITOR FAD TUP FOX BOVIC CER CAPACITOR FAD 33UF FOX BOVIC CER CAPACITOR FAD 31UF FOX DOV C CER	78480 78480 78480 78480 78480 78480	01603F94 016134066 016134066 016034084 036031871 01603876
A4C11 A4C17 A4C13 A4C13 A4C14 A4C16	0160 3870 0160 4084 0160 4084 0160 3874 0160 3874 0160 0127	/ H H H 7 7	a	CAPACITOR FOD DTUF (70% LOUVICETER CAPACITOR FOD TUF (70% DOVIC CER CAPACITOR FOD TUF (70% DOVIC CER CAPACITOR FOD TUF (70% 700VIC CER CAPACITOR FOD TUF (70% 70VIC CER	38480 78480 78480 38480 38480 38480	0160 3870 0160 4084 0380-4084 0160-3874 0160-3874 0160-1177
AAC18 AAC17 AAC18 AAC18 AAC18 AAC18 AAC20	01604084 01604084 01600572 01600574	8 8 1 2	3	CAPACITOR FED TOF FOOL BOYDS CEN CAPACITOR FED TOF FOOL BOYDS CER CAPACITOR FED FOORF FOOL BOYDS CER NOF ASSIGNTO CAPACITOR FED DEFOL FED NOOVDS CER	28480 28480 28480 28480 28480	0160-4084 0160-4084 0160-6084 0160-6572 0160-0574
A4C71 A4C72 A4C72 A4C73 A4C74 A4C76	0160 0128 0160 0946 0160 4064 0160 4084	3 7 8 8	}	CAPACITOR FOD 7 20F 170% BOVIC CER CAPACITOR FOD DITOPT 15% TOOVIC MICA CAPACITOR FOD TUP 730% BOVIC CER CAPACITOR FOD TUP 170% BOVIC CER NOT ASBURIT	78480 28480 28480 28480 28480	01600138 01600946 01604084 01604084
AAC715 AAC77 AAC78 AAC28 AAC30 AAC30 AAC30 AAC34	0160 4084 0160 4084	8		NOT ASSIGNED CAPACITOR FND TUF 270X BOVDC CER NOT ASSIGNED CAPACITOR FND TUF 170X BOVDC CER NOT ASSIGNED	78480 78480	0160 4084 0160 4084
A4C36 A4C36 A4C37	0160-3870 0160-3870	6	13	CAPACITOR FAD Q1UF 120% TOQVDC CER CAPACITOR FAD TOOOPF 120% TOQVDC CER NOT ASSIGNED	28480 28480	0160 3810 0160 3810
A4CR) A4CP2 A4CP3 A4CP3 A4CP4 A4CP6	1901-1098 1901-0536 1901-1098	;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;	13	NOT ASSUMED NOT ASSUMED DIODE-SWITCHING IN4150 BUV ZOGMA 4:45 DIODE-SWITCHING IN4150 BUV ZOGMA 4:45 DIODE-SWITCHING IN4150 BUV ZOGMA 4:45	00040 78480 00040	184160 1901 (636 184160
A4CB8 A4CB7 A4CB8 A4CB9 A4CB9 A4CB10	1901-1098 1901-1098	;		Dudt-Bwitching In4160 Boy Jooma Ans Didd-Bwitching In4160 Boy Jooma Ans Aut Assignto Dudt-Switching In4160 Boy Jooma Ans Not Assignto	00040 00040 00040	184180 184160 184160
A4CR11 A4CR12 A4CR13 A4CR14 A4CR16 A4CR16	1901-0636 1901-0636 1901-0636 1901-1098	н У 9 1		NOT ASSIGNED DRODE-SM SIG SCHOTTRY DRODE-SM SIG SCHOTTRY DRODE-SM SIG SCHOTTRY DRODE-SWITCHING IN4160 BOY TOOMA 4NS NUT ASSIGNED	78480 78480 78480 28480 0004g	1801-0636 1803-0636 1903-0636 1904-0636 1944-60
A4.j1 A4.j7 A4.L1 A4.L2 A4.L2 A4.L2	1268-0124 1268-0124 8140-0210 8140-0210 8140-0210	7 7 1 1 1	11	SHUNT-PROGRAMMABLE I DBL PN 6ET SHUNT-PROSRAMMABLE I DBL PN 6ET INDUCTOR NY CII-NLD IODIH 6% 186DX 366LG INDUCTOR RF CII-NLD IODIH 6% 186DX 366LG INDUCTOR RF CII-NLD IODIH 6% 186DX 366LG	28480 28480 28480 28480 28480 28480	1268 0124 1268 0124 0140 0210 0140 0210 0140 0210
алмрі Алмр <u>7</u> Алмр3	6040-6848 6000 8043 1261-4032	1 0 0	5	EXTRACTOR VELLOW PN PC BOARD EXTRACTOR CONNECTOR-BGL CONT BKT 021-IN B5C-52	28460 28460 28460	EU40 EN48 6000 8043 1261-4832
A401 A402 A403 A404	1864 0286	3	2	TRANSISTON J FET 204393 N CHAN D NODE TRANSISTON DUAL NEN FO-400NW TRANSISTON J FET 204393 N CHAN D MODE NOT ASSIGNED	01795 78480 04713	3N4301 1864 u786 3N4303
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				Attraction to this metion by outcome advances		

Table 6-3. Replaceable Parts

See introduction to this section for ordering information *Indicates factory selected value

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Model 83590A

Reference Designation	HP Part Number	C D	Qiy	Description	Mfr Godø	Mfr Part Numbor
A4136 A4136 A4137 A4137 A4136 A4130 A4130 A41310	1864 (7386 1865-0473 1865-0473 1865-0473	7 6 6	6	NOT ASSIGNED TRANSISTOR DUAL NEW PD=400NW TRANSISTOR NOSELET & CIAN E-MOOL TRANSISTOR NOSELET & CIAN E-MOOL NOT ASSIGNED FRANSISTOR FRE 2N3208 SETO 18 PD=280NW	78480 17860 17868 17868	1804 0346 Vividem Vividem Jivstuu
A4(3) 1 A4(3) 2 A4(3) 2 A4(3) 3 A4(3) 4 A4(3) 6	1854 (J404 1853 (D0)7 1855 (J473	1) 1) 1)	;	нот Абвилго Нот Абвилго Тимбилов нен 61 то 18 го- зеому Тимбилов гля унутата 61 то 18 го- зеому Тимбилов Мобест и симп I-моот	78480 04713 17855	1864 0404 2N 3264 VN 106M
A4016 A4017	1866-0111	0		TRANSISTISH MOSELET N CHAN E MOOL NUT ASSIGNED	17868	VN HDEM
Алп) Алп7 Алп3 Алпа Алпа Алпа	2100-2616 2100-2611	7	L	NOT ASSIGNED NOT ASSIGNED RESISTON-TRAIN FOON ION & SIDE-ADJ 1-TRH NOT ASSIGNED RESISTON-TRAIN EON ION & SIDE-ADJ 17-TRN	30483 37497	E160W204 32023-1-603
алия Алия Алия Алия Алия Алия	2100 0870 2100-1740 0767-0416	6 0 7	40	Not Assissed Not Assissed Из Instan Imm Ion Ion с бют-Арј 17-трн Из Instan Imm BK Ion с бют-Арј 17-трн Из Битар B11 19, 136007 тс-Арј 100	37897 78480 74648	38832-1-103 2100-3248 C4-1-8-10-51187
A4R11 A4R17 A4R17 A4R13 A4R14 A4R16	7100-7633 0498-7367 0498-7368	6 7 3	ì	MEDIDITION TRAIN IN TONIC SIDE-ADJ I-TRIV MEDIDITI 7 DN IN OBWY TC-OFTOO REDIDITION 7 DN IN OBWY TC-OFTOO MOT ASSIGNED NOT ASSIGNED	30983 74845 74845	L160A107 C3-178 TV 7601 G C3-178-TV 8981-6
A4816 A4817 A4818 A4810 A4820	0498-7763 0698-7760 0698-7760 0698-7763	8 6 7 1)	3 	NOT ASSIGNED MEDISTOR & THE 13, ABW F TC-03 100 REDISTOR 37 & H 13, ABW F TC-03 100 REDISTOR 10K 13, ABW F TC-03 100 REDISTOR 13 3F 13, ABW F TC-03 100	7484 <i>4</i> 74846 74846 74846 74846	C3 1/8-10 61 11-6 C3 1/8 10 21 62-6 C3 1/8 10 21 62-6 C3 1/8-10-1332 6
A4R21 A4R22 A4R23 A4R24 A4R24 A4R26	0608-1274 0698-120) 0757-0484 0698-1260	2000	1	NEGISTUR 38 3K I & USW FTC-03100 TEGISTUR ITN I & USW FTC-03100 REGISTUR HO BK I & 125WFTC-03100 REGISTUR 33 FK I & USW FTC-03100 NOT ASSIGNED	74848 74848 74848 74848	C3-178-10-3137-05 C3-178-10-11(2):0 C4-178-10-10(2):0 C3-178-10-2377-0
А4178 А4177 А4178 А4178 А4179 А4170	0498-7760 0498-7777 0498-6846	1 4 3		NGT ASSIGNED RESISTOR TOX IN OBWETC=01100 RESISTOR 422 IN OBWETC=01100 RESISTOR 6425 BN 138WFTC=0180 NGT ASSIGNED	74848 74848 74848	C3-178-10-1002-6 C3-178-10-4338-6 NC66-178-12-6431-0
A41131 A41137 A41133 A41134 A41136	7837-0110 U608-7769	1	1	THENMISTOR BOD & OHM TC++ 7%-C DTG REDISTOR 9 D9K 1% D5WF TC+0±100 NOT ASSIGNED NOT ASSIGNED NOT ASSIGNED	78480 74646	0827-0118 102-178-10-8081-6
алраб Алраб Алраб Алраб Алраб Алраб Алраб Алраб	0696-7717 0698-7743 0698-7743 0698-7743 0658-7743	9 0 1 1		RESISTON 100 IN 06WFTC-02100 RESISTOR 198K IN 06WFTC-02100 RESISTOR 100 IN 06WFTC-02100 RESISTOR 198K IN 06WFTC-03100 RESISTON 198K IN 06WFTC-03100	74548 74545 74545 74540 74540 74540	C3-178-10-1000-6 C3-178-10-1000-6 C3-178-10-1000-6 C3-178-10-1000-6 C3-178-10-1001-6 C3-178-10-1001-6
а4841 А4847 А4843 А4844 А4846	-JCH4-7383 -JCH4-7387 -JCH8-7373 -JCH8-7375 -JCH8-7375			RESISTUR BO 9K 1% UBWF TC-01100 HESISTUR 19 6K 1% GBWF TC-01100 RESISTUR 31 6K 1% GBWF TC-01100 RESISTUR 37 K1% GBWF TC-01100 NUT ASSIGNED	74848 74848 74848 74848 74848	C3-1/8-10-8002 G C3-1/8-10-1807 G C3-1/8-10-1807 G C3-1/8-10-4222 G
алпас Алпа7 Алпа8 Алпа8 Алпа9* Алпа9*	0698-1197 2100 7030 0757 0471 0698-8016	19 0 4 8	1 3 3 7	AEGISTOR 23 7 1% OBW / TC-01100 HEGISTOR TRMR 70% 10% C 10P-ADJ 1-TRN REGISTOR 75% 1% 125W / TC-01100 REGISTOR 75% 1% OBW / TC-01100 NOT ASSIGNED	24046 73138 24646 28460	C3-1/8-T00-2387-G #2PR708 C4-1/8-T0-8288 0408-8615
АЛЛБТ АЛЛБ7 АЛЛБ3	0698-7782 0698-7249	3	;	RESISTOR 57 6K 1% 06WF TC-02100 RESISTOR 3 ARK 1% 06WF TC-02100 NOT ASSIGNED	74646 74646	C3-1/8-T0-8262-G C3-1/8-T0-2481-G
алра Алра	0698-7269 0692-7260	;		RESISTOR BOOK IN DOWF TC-OLIDO RESISTOR TOK IN DOWF TC-OLIDO	74546 74546	C3-1,8-10-9091-0 C3-1,8-10-1012-0
A4855 A4857 A4858 A4858 A4859 A4859	2100-2030 0767-0280 0767-0280 2100-1986	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		REGISTOR-TRAIN 20K 10% C 10P-ADJ 1-1RN REGISTOR 1K 1% 12BWF 1C=02100 REGISTOR 1K 1% 12BWF 1C=02100 REGISTOR-TRAIN 1K 10% C 10P ADJ 1-TRN NOT ASSIGNED	73138 24646 24646 73138	87#130k C4-174-T0-1001+F C4-178-T0-1001+F 82FA1k 82FA1k
А4701 А4802 А4802 А4864 А4864 А4865	0698-7269 0698-7270 0757-0447 0757-0240 0693-7260	4 9 4 3 7	3	PESISTOR 9 09K 1% 05WF TC=01100 RESISTOR 76 1K 1% 05WF TC=01100 RESISTOR 16 7K 1% 176WF TC=01100 RESISTOR 16 7K 1% 175WF TC=01100 RESISTOR 16K 1% 05WF TC=01100	24646 24646 24646 24646 24646 24646	C3-1/8-10-9081-0 C3-1/8-10-3817-0 C4-1/8-10-1823-F C4-1/8-10-1823-F C3-1/8-10-1007-0

Table 6-3. Replaceable Parts

See introduction to this section for ordering information *Indicates factory selected value

Table	0-J.	Replaceable	Parts

Reference Designation	HP Part Number	C D	ûty	Description	Mfr Goda	Mir Part Number
алнан Алнат Алнат Алнан Алнар Алнар	07670418 31001030 0858-7358 0688-3440) 5)))	1 b	NEBISION 511 14 125221 1C-01100 NEBISION-TIMME JOK 10X C 10PADJ 1-108 NEBISION 1X 1X 05921 1C-01100 NEBISION 1X 1X 05921 1C-01109 NOT ASSIGNED	74848 73138 74848 74848	C4-128-1061101 NPENDOR C3-128-10-1001-0 C4-128-10-1001-1
A4/171 A4/172 A4/172 A4/173 A4/174 A4/176	13498 0085 0757 0778 0698 7777 0698 7751 0698 7747	() # 5 5 0	2 1 1	NE 51510A 2 514 1% 124W4 10-01100 RE51510A 1 JHK 1% 124W4 10-01100 RE51510B 51 K 1% 05W4 10-01100 RE51510B 4 224 K % 05W4 10-01100 RE51510B 2 578 1% 05W4 10-01100	74040 74040 74040 74040 74040 74040	2 C4-12/8-10 2631-2 C3-12/8-10 5781-7 C3-12/8-10 5112-43 C3-12/8-10 4727-6 C3-12/8-10 2621-6
алть Алть Алть Алть Алть Алть	0767-0390 0767-0274 0698-7234 0167-0304 0167-0304 0698-3440	8 6 0 7	3	NEGISTON 82 6 1% 126WF 1C-03100 REGISTOR 1218 1% 126WF 1C-03100 REGISTOR 856 1% 06WF 1C-03100 REGISTOR 61 1 1% 126WF 1C-03100 REGISTOR 518 1% 126WF 1C-03100	74848 74848 74848 74848 74848 74848	C4-12-8-10-826N3 C4-12-8-10-12-11-7 C3-12-8-10-826N-03 C4-12-8-10-826N-05 C4-12-8-10-1926N-1
А4981 — А4988 А4989 А4989 А4989	0699-7744 0899-7763		,	NOT ASSIGNED NESIS108 2 18K 15. 08/07 TC=0±100 RESISTOR 1 1K 15. 08/07 TC=0±100 NOT ASSIGNED	74646 74646	C3-128-10-2161-0 C3-128-10-1102-0
ааниј Ааниј Ааниј Ааниј Ааниј	0688-7717 0688-7763 0688-7773	U 1 1	•	NOT ASSIGNED REGISTOR 100 TX (IBW) TC+01100 REGISTOR 5 TX TX (IBW) TC+01100 REGISTOR 261 TX (IBW) TC+01100	74646 74646 74646	C3-128-10-1008-0 C3-128-10-8113-0 C3-128-10-2818-0
A4898 A4898 A4899 A4899 A48100	0688-3187 0837 0085 0167 0780 0767 0410	1 8 1 1 0	; ;	NOT ASSIGNED RESIGNED 10 AK 1% 126WF TC-03100 THERNISTOR ROU 880 OHM TC-176/C DEG REFISTOR 1K 1% 126WF TC-03100 RESISTOR 881 1% 126WF TC-02100	74646 78480 74646 74646 74646	C4-12-8-10-1002-7 0837-0086 C4-12-8-10-1001-7 E4-128-10-8818 F
A4TP1- A4TP10 A4TP11				Ph5 0H J1		
A41P12 A41P13 A41P14	0360 0535	0		TERMINAL TEST POINT PCB TERMINAL TEST POINT PCB NUT ASSIGNED TERMINAL TEST POINT PCB	00000	onden hv description
A41P16 A4U1	0360 0516	Ŭ B	,	TERMINAL TEST POINT PCB TERMINAL TEST POINT PCB	00000	onden by Debchiption Orden by Debchiption
A4U2 A4U2 A4U2 A4U4 A4U6	1876 0417 1870 0816 1876 0810 1876 0810	8 7 1 7	1	ic op and low-noise to be pro ic byntch ani g duad is od c pro ic op and frich duad is od c pro anlig multiplatis-chan centip ic op and low-biagh-impo to 59 pro	78480 27014 06868 78480 04713	1876-0761 († 13333) Um († 7 1876-0610 († 3666-
A4U8 A4U7 A4U8 A4U9 A4U9	1826-0610 1826-0447 1826-0421 1826-0417 1826-0417 1820-1197	12800	1	ANLG MULTIPLER 4-CHAN CERDIP IC OP AMP 558 TO 9 PKG IC OP AMP 559 TO 90 PKG IC SV9TEH ANLG GUAD 16-DIPC FKG IC GATE TTELS NAND QUAD 2-INP	28480 27014 27014 27014 27014 01285	1874 0810 (F787)((M310)((F13333)) SN74(SOOR
A4UI1 A4UI7 A4UI3 A4UI3 A4UI8	1876 0318 1870-1716 1870-1710 1876 0752 1876 0752	73823	8 L	IC OP AMP LOW BIAS H-IMPD TO 89 FAD IC DCDR ITL & S-TO-B-LINE 3 INP IC FF TTL & S-TO-B-LINE 3 INP IC FF TTL & S-INPE POS-LIDGE-TRIG COM IC COMP 17-B-D/A-B-DIPC FAD IC COMPARATOR FROM TO BU FAD	04713 01705 01795 74365 01795	LF 368G 6N / AL 61 3RN 6N / AL 67 3RN AD 764 2 DD LM 31 LL
алуп) Алуп2 Алуп2 Алуп3 Алуп4 Алуп5	1807 0040 1807-0048 1907-0041 1907-3670 1907-3670	77466	2	DIODE-2NR 6 10V 5% DO-35 PD= 4W DIODE-2NR 6 10V 5% DO-35 PD= 4W DIODE-2NR 6 11V 5% DO-35 PD= 4W DIODE-2NR 4 22V 5% DO-7 PD= 4W 10=-074% DIODE-2NR 4 22V 5% DO-7 PD= 4W 10=-074%	78480 78480 28480 78480 78480 78480	1802-0048 1802-0048 1802-0041 1802-3010 1802-3010
AAWI AAW2 AAW3	*1680005 81680005 81680005	0 0 0		WRE 22AWS W PVC 1 N22 BOC WRE 22AWS W PVC 1 N22 BOC WRE 22AWS W PVC 1 N22 BOC	78480 28480 38480 38480	8159-0005 8159-0005 8159-0005
A5	83882-8000B	6		GOAND ABSEMBLY-FM	28480	83882-80008
АВС1 АВС2 АВС3 АВС4 АВСВ	0160 0575 0160 0572 0160-4084 0160-0945 0160-0575	4 1 8 7 4	•	CAPACITOR-FAD 0410F 120% 60VDC CER CAPACITOR-FAD 2200PF 120% 100VDC CER CAPACITOR-FAD 10F 120% 60VDC CER CAPACITOR-FAD 810PF 15% 100VDC MICA CAPACITOR-FAD 0470F 120% 60VDC CER	28480 28480 28480 26480 26480 28480	0160-0675 0160-0672 0160-4084 0160-0945 0160-0575
АВСВ АВС7 АВС8 АВС9 АВС9 АВС9	G180-2247 0180-3879 0180-3879 0180-3879 0180-3879 0180-3879	1777777	1	CAPACITOR-FAD 3 8FF ± 35FF 600VDC CER CAPACITOR FAD 01UF ±20% 100VDC CER CAPACITOR FAD 01UF ±20% 100VDC CER CAPACITOR-FAD 01UF ±20% 100VDC CER CAPACITOR-FAD 01UF ±20% 100VDC CER	28460 28480 28480 28480 28480 28480	0160-2247 0160-2879 0160-2879 0160-3879 0160-3879
A5C11 A5C12	0140 0198 0160-2199	b Z	1	CAPACITOR FED 200FF 10% 200VDC NICA CAPACITOR FED 20FF 10% 200VDC NICA	72136 28460	DN18F201J0300WV1CR C160-2188
A8C13 A8C14 A8C16	0121-0446 0100-3878	6 7	·	NOT ASSIGNED CAPACITOR V TRMR-CER & 5-20PT 180V CAPACITOR FXD 01UF 220% 100VDC CER	28480 28460	0121-0448 0160-2879
A5C18 A5C17	0160-3878 0160-3878	;		CAPACITOR FAD DIUF 120% TOOVDC CER CAPACITOR FAD DIUF 120% TOOVDC CER	28480 28480	0160-3879 0160-3879
]				ntroduction to this section for ordering information		

See introduction to this section for ordering information *Indicates factory selected value

Reference Designation	HP Part Numbor	C D	Qty	Description	Mir Goda	Mfr Part Number
ABCIB	0100 3810	,		CAPACIEDILEND DEUE EDON TOOVIC CER	28480	0160 1870
A6C10 A6C70	0160 2240	1	;	нот асбільтр Сарасновтро а ріутуріт воруюстти	2H4NU	0160.2240
ABC71 AbC77 AbC75 AbC76 AbC76	0160-4084 0160-4084 0160-3870	0 8 7		NOT ABBIGHED NOT ABBIGHED CAPACITOREFD TUP E70% BOVDC CER CAPACITOREFD TUP E70% BOVDC CER CAPACITOREFD DTUP E70% TODVDC CER	784NO 784NO 784NO 784NO	(1)60-4084 (5)60-4084 (5)60-3670
A&C76 A&C77 A&C77 A&C70 A&C70	0160 3874 0160 4084 0160 4084 0180 7617 0180 7617	2 15 16 1	4	CAPACITOR F D. HIPF F BYY JDOVIC CER CAPACITOR F D. TUF F DV BOVIC CER CAPACITOR F D. TUF F DV BOVIC CER CAPACITOR F D B BUF F TOX BVDC TA CAPACITOR F DD B BUF F TOX BVDC TA	78480 28480 28480 26088 26088 26088	отор.3874 отор.4084
ABC31 ABC33 AEC33 AEC34 AEC34 AEC36	0180;617 0180;717 0180;7707 0180;0474 0180;0474	1 5 4 4	1	САРАСНОН-РЭО О ВИР 110%, 15V0С ТА САРАСНОН-РЭО О ВИР 110%, 15V0С ТА САРАСНОН-РЭО 1000 F 10%, 16V0С ТА САРАСНОН-РЭО 1607 5 10%, 2005С ТА САРАСНОН-РЭО 1607 5 10%, 2005С ТА	26088 26088 66280 26480 26480	D8889518355 D888518355 16001072001087 0180 0474 0180 0474
АБСІВ АБСІ7 АБСІ8 АБСІ8 АБСІ8 АБСІ8	0180-0474 0380-0474 0380-0474 0380-0474 0380-0474 0380-0474	****		CAPACITOR FAD. I BUT LTON, 70VDC TA CAPACITOR FAD. 1 BUT LTON, 70VDC TA CAPACITOR FAD. 1 BUT LTON, 70VDC TA CAPACITOR FAD. 1 BUT LTON, 70VDC TA CAPACITOR FAD. 0 TUF F70N, 100VDC CTB	28480 28480 28480 28480 28480 28480	01800474 01800474 01800474 01800474 01800474 0180-3870
ABCAT	0160 2249	3		CAPACITOR FOD A 7PF ± 26FF 800V/C CFR	18480	0180-2240
лься) Абси? Абсиз Абсия Абсия Абсив	1801-0033 1601-0033 1801-0047 1801-0047 1801-0047 1801-1098	7788	,	Diode gen prip trov 200MA DO-7 Diode gen prip trov 200MA DO-7 Diode Switching 20V 76MA 1065 Diode Switching 20V 76MA 1065 Diode Switching 1NA 160 60V 200MA 465	28480 28460 28460 28480 28480 00240	1001-0033 1001-0033 1001-0037 1001-0047 1001-0047 104160
АВСИВ АВСИЯ АВСИЯ АВСИЯ	1001-1098 1001-1098 1001-1098	1 1 1 0		Diddl-Gwitching 1n4160 Goy 700na 4n5 Diddl-Gwitching 1n4160 Goy 700na 4n5 Diddl-Gwitching 1n4160 Goy 700na 4n5 Diddl-Gm Gig Cchottry	00040 00040 00040 78460	IN4160 IN4160 IN4160 IN4160 IN01-0636
A6K1 A6K2	0490-0916 0490-1063	6	I	HELAY HEED TA BOOMA TORVOC BVDC-COIL HELAY HEED TA BOOMA BOVDC BVDC COIL TRVA	26460 26460	0490-0916 0490-1053
ADL1 AdlJ AdlJ AdlA AdlA	8100-1675 9100-1619 9100-1619 9100-1619 9100-1619	07787	4	INDUCTOR RECHARD 230H 6%, 1860X-1860G INDUCTOR RECHARD 6 BUH 10% INDUCTOR RECHARD 6 BUH 10% CULTORID INDUCTOR RECHARD 6 BUH 10%	78480 28480 28480 28480 28480 28480 28480	8100-1675 9100-1610 9100-1610 08603-80001 9100-1610
A515	8100-1619	7		INDUCTOR REACH-MED & BUH 10%	28480	0100-1619
абмрі Абмрэ Абмрэ Абмрэ Абмра Абмра	6040 6861 6000 8043 4230 0146 4230 0146 4230 0146	20000	1	EXTRACTOR IN P.C. BOARD EXTRACTOR INSULATOR BEAD GLASS INSULATOR BEAD GLASS INSULATOR BEAD GLASS	78460 78460 78460 78460 78460 78460	6040 NH61 6000 8043 4330 0146 4330 0146 4330 0146
абыра Абырт Абырт	4330-0145 4330-0145 4335-0145	000		INSULATOR READ GLASS INSULATOR READ GLASS INSULATOR BEAD GLASS	78480 78480 78480 78480	4330 0145 4330 0145 4330 0146
AB101 AB102 AB103 AB104 AB104 AB106	1854-0520 1854-0520 1854-0520 1854-0520 1854-0520 1854-0425	0 0 0 0 5	1	TRANSISTOR DUAL NPN PD-760MW TRANSISTOR DUAL NPN PD-760MW TRANSISTOR DUAL NPN PD-760MW TRANSISTOR DUAL NPN PD-760MW TRANSISTOR DUAL NPN PD-760MW	78480 28480 28480 28480 28480 78480 78480	1854 0576 1854 0576 1854 0526 1854 0526 1854 0526 1854 0415
авлі Авля Авля Авля Авля Авля Авля Авля Авля	0688-0083 0688-3164 0698-3164 0698-3164 0698-3164 0767-0430 0767-0430 0767-0430 0767-0430 0698-3168 0698-3168 0698-6160 0699-0174	8 0 0 0 4 4 4 6 0	9 5 7 7 6	RESISTON 1 VEK 1% 175WF 1C-01100 RESISTON 4 22K 1% 175WF 1C-01100 RESISTON 4 22K 1% 175WF 1C-01100 RESISTOR 4 27K 1% 175WF 1C-01100 RESISTOR 4 77K 1% 175WF 1C-01100 RESISTOR 6 81K 1% 175WF 1C-01100 RESISTOR 737K 1% 175WF 1C-01100 RESISTOR 737K 1% 175WF 1C-0125 RESISTOR 10 7K 1% 175WF 1C-0125	24646 24647 24646 24646 24646 24646 24646 24646 24646 24646 26480 26480	C4-326 TO 1083-F C4-326 TO 4223-F C4-326 TO 4223-F C4-126 TO 4223-F C4-126 TO 4223-F C4-126 TO 4223-F C4-126 TO 6811-F C4-326 TO 6811-F C4-327
АБН13 Абн13 Абн13 Абн14 Абн16	0698-3166 0698-0083 0698-3448 0757-0394 0757-0394	1 15 15 15 15 15 15 15 15 15 15 15 15 15	7	PEGIGTOR 4 B4K 1% 128W/TC-01100 PEGIGTOR 1 06K 1% 126W/TC-01100 REGIGTOR 2011% 126W/TC-01100 REGIGTOR 511 1% 126W/TC-01100 REGIGTOR 511 1% 126W/TC-01100	74648 74648 74648 74648 74648 74648	C4-12B-1034641-F C4-128340-1081-F C4-128340-98010F C4-128340-9810F C4-128340-1081883-F C4-128-10851883-F
АБЛІБ АВЛІ7 Авлія Авлія Авлія Авлія	0767-0442 0767-0442 2100-3749 11767-0468	9007	1	NOT ASSIGNED PESISTOR 10K 1% 125WF 1C-01100 PESISTOR 10K 1% 125WF 1C-01100 PESISTOR TRMR 5K 10% C SIDE-ADJ 17-TRN RESISTOR 51 1K 1% 125WF 1C-01100	24546 24546 28460 24545 24545	C4-1/8-10-3002-F C4-1/8-10-3002-F 2300-3749 C4-1/8-10-5312-F
45871 488727 48823 48823 48824	0698-3136 0698-5161 0698-3161	18 16 17	1	RESISTOR 17 8K 1% 126WFTC-011W RESISTOR 10K 1% 126WFTC-0125 RESISTOR 287K 1% 126WFTC-01100 NOT ASSIGNED	24546 28480 24545	C4-1/8-70-1787-7 0898-6360 C4-1/8-10-2871-7
				1		

Table 6-3. Replaceable Parts

See introduction to this section for ordering information *Indicates factory selected value

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Reference Designation	HP Part Numbør	C D	۵ty	Doscription	Mfr Goda	Mfr Part Number
Аблуб Аблуб Аблуб Аблуб Аблуб Аблуб Аблуб Аблуб	0608 0093 0608 008 3 0767 0387 0767 0387 0767 0387	10 10 10 10 4	,	NOT ASSIGNTD REDISTORT OF THE T28WE TC-01 GO PEDISTORT OF THE T28WE TC-01 GO PEDISTORT OF THE T28WE TC-01 GO REDISTORT OF THE T28WE TC-01 GO REDISTORT OF THE T28WE TC-01 GO	2464n 2464n 10701 10701 2464n	C4-17 H 113-1401 F C4-17 H 113-1401 F OFAC1 - H-103-1804 F OFAC1 - H-103-1804 F C4-17 H 103-1804 F
аризт, Аризу Аризу Аризу Ариза Ариза	L767-0401 0767-0403 0898-7780 2190-7674 0698-7780	1) 7 1 3 1	4 7 6 4	R16(610)) 100 1% 17600 7 (⊂07100) R16(610)) 121 1% 12600 7 (⊂07100) R16(610) 88 1% 1% 0500 7 (⊂07100) R16(610) 11808 600 10% € 600 400 1 100	74648 74648 74648 10483 74648	C4 1. 8 10-101-7 C4 1. 8 10 17 18 7 C3 1. 8 10 17 18 7 C3 1. 8 10 88 17 6 C3 1. 8 10 88 17 6
арнар 1 сная 1 сная 1 сная 1 сная 1 слая 1 слая	2100 7674 0698-7280 2100-7674 0698-7260 2100-7674	3131		РЕБІЗІОЛ-ТРЫВ 800-ТОК С 600-АОД 1-ТРК РЕБІЗІОЛ ВИТЬ 1К ОВУУ Л ГС-ОТТОО РЕБІЗІП-ТРЫЙ 800-ТОК С 601-АОД 3-ТРК РЕБІЗГОЛ-ТРЫЙ 80У ТОК С 601-АОД 3-ТРКУ РЕБІЗГОЛ-ТРЫЙ 600-ТОК С 601-АОД 3-ТРКУ	20082 24640 20083 24640 20082	47607601 (2.3-#70.6#15.4) (7607601 (7-1.#710.8#17.4) (7607601)
арма I Арма 7 Арма 7 Арма 7 Арма 6 Арма 6	2100-2611 2100-2611 2100-2611 2100-2611 2100-2611 0767-0442	1 1 1 1 0		REBETUR-TAMP DUN TON L BIDE-ADJ 17-TAN Ngaistur-tamp dun ton C bide-Adj 17-Tan Rebetur-tamp dun ton C bide-Adj 17-Tan Rebetur-tamp dun ton C bide-Adj 17-Tan Rebetur tamp dun ton C bide-Adj 17-Tan Rebetur ton ton 178997 R*01100	37007 37007 37007 37007 37007 37007 74440	37878-1-803 37878-1-803 37878-1-803 37878-1-803 64-1-8-10-1603
арнар Арнар Арнар Арнар Арнар Арнер	0767 0470 0767 0470 7100 3768 0688-7780 7100 3748	0 1 1 1 1	4 3	небібтов 780 тм. 176W (тс=0,150) небібтов 780 тм. 176W (тс=0,150) небібтов 780 тм. 176W (тс=0,150) небібтов 78 тк. тм. 6697 (тс=0,160) небібтов 7848 тм. 6697 (тс=0,160) небібтов 7848 тм. 6697 (тс=0,17718)	74040 74040 74040 74040 74040 74040	C4-1-H 13-761 } C4-1-H-19-761 } 2100-3780 C3-1-H 10-8817 G 2100-3749
Арнуј Арнуј Арнуј Арнуј Арнуј	0688 1188 0698 3188 0767 0348 0767 0348 0767 0348 0767 0348		6	REDITION 14 TR 12 176WF 10-01100 REDITION 14 TR 12 176WF 10-01100 REDITION 10 12 176WF 10-01100 REDITION 10 12 176WF 10-01100 REDITION 10 12 176WF 10-01100	; 4648 24648 24648 24648 24648 24648	C4-1-B-13 1477 7 C4-1-B-13 1477 7 C4-1-B-13 14183 1 C4-1-B-13 14183 1 C4-1-B-13 14183 1 C4-1-B-13 14183 1
Абрая Абрая Абрая Абрая Абрая Абрая Абрая	1)767-0348 0767-0348 0767-0348 0698-6360 0698-6360	7 7 7 8 8		REGISTUR TO 1:4 176WF 1C-01100 REGISTUR TO 1:4 176WF 1C-01100 REGISTUR TO 1:4 176WF 1C-01100 REGISTUR TO: 176WF 1C-0176 REGISTUR TO: 1:4 176WF 1C-0176	74648 74648 74648 78460 78460	64-17, N-TO-10N0-1 64-17, N-TO-10N0-1 64-17, N-TO-10N0-1 0508-6380 0508-6380
Арна) Арна7 Арна7 Арна Арна4 Арга6	13898 5 181 1598 5 ** 1757-0487 1698 533 1698 533 1757-0789	6 6 9 9 7	1 2	РЕВІБТОЛ ТОК ТЖ. Т26007 ГС=0326 НЕВІБТОЛ ТОК ТЖ. Т26007 ГС=0326 НЕВІБТОЛ Т21К ТЖ. Т26007 ГС=0326 НЕВІБТОЛ 42К ТЖ. Т26007 ГС=0376 РЕВІБТОЛ Т3 3К ТЖ. Т26007 ГС=03100	78480 78480 74548 76480 19703	0608 6360 0608 6360 C4 t, 8-10 5253-1 0608 6363 MFACT/8-10 5332-F
алиса Алиса Алиса Алиса Алиса Алиса Алиса Алиса Алиса Алиса	1888-8383 1888-3443 1888-3443 1888-3443 1888-3443 1888-3443	0444	;	PEBISTOR 406 1% 126WF 1C=0176 HEBSTOR 427 1% 126WF 1C=01700 PEBISTOR 427 1% 126WF 1C=01100 PEBISTOR 427 1% 126WF 1C=01100 PEBISTOR 427 1% 126WF 1C=01100	78480 74648 74648 74648 74648 74648	0698 8383 C4-17 8-10 42384 C4-17 8-10 42384 C4-18 10 42284 C4-18 10 42284 C4-17 10 42284
абиј) Абиј; Абиј; Абија Абија	0698-3447 0698-3447 0767-0280 0767-0280 2767-0280 2100-2672	4 4 3 3 3 1	,	HEISTOR 477 1% 176WF1C-01100 HEISTOR 477 1% 176WF1C-01100 REISTOR 477 1% 176WF1C-01100 HEISTOR 1K1% 176WF1C-01100 HEISTOR 1K1% 10K10% C 600L40011488	74648 74648 74648 74648 74648 30983	C4-1, H-10 47783 C4-1, H-10 47783 C4-1, H-10 4013 C4-1, H-10 10013 C4-1, H-10 10013 L1003403
авнув Авнур У Аув Авнув Авнув Авнео	0767-0780 0767-0780 0698-3168 0767-0403 0698 0087	33421	,	ИСБІБТОВ ТА ТА Т78W7 ТС-01100 ИСБІБТОВ ТА ТА Т78W7 ТС-01100 ИСБІБТОВ Т278 ТА Т28W7 ТС-01100 ИСБІБТОВ 484 ТА Т28W7 ТС-01100 ИСБІБТОВ 484 ТА Т28W7 ТС-01100	54648 34648 74648 34648 34648 34648	C4-1, 8-10-1003-7 C4-1, 8-10-1003-7 C4-1, 8-10-2377 F C4-1, 8-10-2378 F C4-1, 8-10-2788 F C4-1, 8-10-2788 F
АВТРІ АВТРЭ АВТРЭ Автра Автра Автра	0360 0535 0360 0535 0360 0535 0360 0535 0360 0535	00000		HERMINAL TEST POINT PCIE TRIMINAL TEST POINT PCIE TRIMINAL TEST POINT PCIE TERMINAL TEST POINT PCIE TERMINAL TEST POINT PCIE	00000 00000 00000 00000 00000	ORDEA BY DI SCRIPTION ORDEA BY DI SCRIPTION ORDEA BY DI SCRIPTION ORDEA BY DI SCRIPTION ORDEA BY DI SCRIPTION
451PG 451P7 451P8 451P0 451P10	0160 0515 0160 0515 0160 0515 0160 0515 0160 0515	0000000		TENNINAL TEST POINT PCB TENNINAL TEST POINT PCB TENNINAL TEST POINT PCB TENNINAL TEST POINT PCB TENNINAL TEST POINT PCB	00000 00000 00000 00000 00000	orden by description orden by description orden by description orden by description orden by description
A51P11 A5U1 A5U2	0180-0515 1810-0708 1810-0708	U M U		TERNINAL TEST POINT PCB NETWORK-RES 8-51210 UK OHM K-7 NETWORK-RES 8-51258 UK OHM K-7	00000	UNITE BY DESCRIPTION
ABU3 ABU4 ABUB	1876-0418 1876-0418 1810-0321	0 1 1	; ; ;	и с вулски развина и клиж к / и с вулски Алька рида на вине с кла h Liwonk, NLS и бира / к цим х / h Liwonk, NLS и бира / ракани х /	27711A 01121 01121	FURACES (F133310) 708/377 708314
ABUK ABUJ Abub Abub Abub	1870-1186 1876-097 1876-0349 1876-0558 1876-0558 1876-0558	8]] 8 2	, , ,	IC FF TFL US D-TYFE POS-EDGE-TRIG COM IC OP AMP GP DUAL TO 80 PAS IC V RGUTR TO 39 IC VIGUTR TO 39 IC WIDFBAND AMPL VID TO 100 FAG	01206 28480 07263 27014 18374	5N74L5174N 1826-0002 UA78N06HL 1M337H NE802N
A5U13	1876-0478	,	,	іс бултен альц в Дір р рац	01796	heolop

See introduction to this section for ordering information *Indicates factory selected value

	and of contract conferences in the presented of the second device of the second by the second presented of the second	
Figure 1 (1997) And 1 (1997)		

Model 83590A

Reference Designation	HP Part Number	0 D	Qty	Description	Mfr Gada	Mfr Port Numbor
Abul 2 Abul 3 Abul 4 Abul 6	1876 0418 1876 0418 1876 0418 1876 0867	5 5 5		RE BYNTELLANG OUAD 16 DIP C PAIS IE BYNTEH ANG OUAD 16 DIP C PAIS IE DIP AMP OF DUAD 14 DIP C PAIS NOT AND OF DUAD 14 DIP C PAIS NOT ANSIGNED	27014 27014 27014	(813331)) (813731)) (813731) (81248)
Abute Abut Abuta Abuta Abute	1820-1188 1828-0689 1820-1218 1826-0700 1810-0224	8 5 5 0 0	1 1 1	IC FF TTL 65 D-TYFE POS FD91F-1886 (33M 80 (33M H B D/A TS D9F4 PAS 80 (32DH TTL 65 D-103H CHAE 2 4MP 80 (0P AMP MH 14-60PC PAS 80 (0P AMP MH 14-60P2 10A (34M F 4	01286 24366 01285 34321 01121	507 745 63 7433 A1376 74 A13 637 741 63 3839 1143 - 64 108 6 508 10 33 3
Abusi	1810.0366	1	٠	артууны ну б о бирээн н сины ж б	a) (2)	JUNA721
абул1 Абун2	1907-3007 1907-3007	3		0001-766 ; 377 65 00 7 PD= 4W TC=+0745 0801-766 7 377 65 00 7 PD= 4W TC=+0745	78480 28480	1807-3007
ADWI ADWJ ADWJ	4160 000b	IJ	,	WHE JJAWI W PVC 1277 HOC NDF A550(511) NDF A550(511)	384BU	N159 0005
ABWA Abwa	8198 COOP 8198 COOP	0 0		WHE ZAWAS WINE 1872 HOC WHE ZAWAS WINE 1872 HOC	78480 78480	8169 (00)5 8169 (00)5
Абуля Абуул	6160-0005 6160-0005	0		WRI 77AWS W PVC 1877 ROC WRIE 77AWS W PVC 1877 ROC	28480 28480	8160 (MD) 8160 (MD)
AB	#3880 60054	3		BOAND ABBEMBLY SWEEP CONTROL	28480	
АВГ 1 - Ар "л: Алса Алса Абс <i>7</i>	0180-0118 0180-0118 0180-2815		H J	NOT ASEIGNED CAPACITION FOD B BUF FTOM SEVIX: TA CAPACITION FOD B BUF FTOM SEVIX: TA CAPACITION FOD FOOUL FFOM TOVIX: TA	66780 60780 78480	16006865803687 16006865803687 0180-7816
ADC8 ADC9 ABC10 ABC11 ADC13	L 01#0-0776 01#0-0778 	6 ñ	b	NDT ASSIGNED CAPACITOR FAD 22011 10% 16VDC TA CAPACITOR FAD 22011 10% 16VDC TA NOT ASSIGNED NOT ASSIGNED	60769 60789	16007762001687 1600776201687
AFC13 AV C14 AuC16 AEC16 AEC17	0160-3878 0160-0673 0160-0673 0160-3878 0160-3878	0 2 1 6		NOT ASSIGNED CAPACITOR FAD 1000PF / 20% 100VIX: CER CAPACITOR FAD 4700PF / 20% 100VIX: CER CAPACITOR FAD 1000PF / 20% 100VIX: CER CAPACITUR FAD 1000PF / 20% 100VIX: CER	78480 7時末世(1) 7時4世(1) 7時4世(1) 7時4世(1)	0160 3678 0160-0673 0160-3678 0160-3678
AEC18 A5C18 AEC30 AEC31 AEC33	0180 0575 0180 3878 0180 4084 0180 4084	4 11 11		NOT ASSIGNED CAPACITOR FAD (14707 ± 20% BOVDC CEN CAPACITOR FAD 1000F/ ± 20% TOOVICC CEN CAPACITOR FAD 100 FUT F20% BOVDC CEN "APACITOR FAD 10F 120% BOVDC CEN	7約4約1) 7約4約1) 7約4約1) 7約4約0 7約4約0	01000576 01603878 01604084 01604084
АБС73 Абс74 Абс76 Абс76 Абс76 Абс77	0160-3870 0160-3870 0160-3878 0160-3878 0160-3878 0160-0576	7 7 6 4		CAPACITOR FAD OFUF ±20% TOOVDC CER CAPACITOR FAD OFUF ±20% TOOVDC CER CAPACITOR FAD TOOVPF ±20% TOOVDC CER CAPACITOR FAD TOOVPF ±20% TOOVDC CER CAPACITOR FAD TOOVPF ±20% SOVDC CER	78480 78480 78480 78480 78480 78480	0360-3070 0340-3070 0360-3070 0360-2670 0360-3670 0360-0676
A6C78	0160-3874	,		CAPACIT	28480	0180-2874
АВСН) Авсн7 Авсн7 Авсн7 Авсн4 Авсн6	1801-0535 1801-0535 1801-0535 1801-0550 1801-0050	0 0 0 1 1 1	Ø	Diode-6M Big Bennttry Diode-8M Big Bennttry Diode-8M Big Bennttry Diode-6M Big Bennttry Diode-6M Tening Hov 700MA 7A5 DO 35 Diode-6M Tening Hov 700MA 7A5 DO 35	78480 78480 78480 78480 78480 78480	1901-0577 1901-0535 1901-0535 1901-0250 1901-0250
АЛСИО АЛСИЈ АЛСИЈ	1901-0050 1901-0050	;		DIODE-5W1CHING BOY 200MA 2N5 DO 35 DIODE-5W1CHING BOY 200MA 2N5 DO 35 NOT ASSIGNTD NOT ASSIGNTD	28480 28480	1801 0060 1801 0060
	1801-0050	1		DIODE-SWITCHING BOY ZOON'A ZNS DO 36	28480 28480	1901-0080 1001-0080
A6CR11 A6CR12 A8CR13	1901-0050 1901-0050 1901-0033	3		DIORY-EWITCHING BOV 200MA 2NS DO 36 DIORY-EWITCHING BOV 200MA 2NS IX) 26 DIORY GP 160V 200MA D7	28480 28480 28480	1901 9000 1901 9000 1901-0033
Adl: Adl7 Adl3	9140-0137 9140-0137 98693-80001	9	ň	INDUCTOR RECENTED TWILD TWILD TWILD TO A 46LG O- 80 INDUCTOR RECENTED TWILD TWILD TWILD TWILD TO A 46LG O- 80 COULTONOID	28480 28480 28480	8140-0137 9140-0137 08603-80003
лемрі Лемрі	6040 £ 49 5003 9043	8	1	ENTRACTOR PC BOARD BLUE IN PC BOARD ENTRACTOR	78480 78460	6040 6849 6009 904 3
A501	1855-0423 1854-0423 1856-0423 1856-0423 1854-0018 1853-0405	07.07	3 1 1	TRANSISTUR MOBEET N CHAN E-MOOL TRANSISTUR NEN 2N2222A SI TO 18 FD-800 VW TRANSISTUR NEN 2N2222A SI TO 18 FD-800 VW TRANSISTUR NEN SI TO 18 FD-260NW TRANSISTUR PRP SI FD-200NW FT-860MH2	17866 04713 17866 28480 04713	VN10KM 2N2222A VN10KA 1864 0010 2N4200
A8(12 A6(13 A6(14 A6(15	1601.0-00			1	04713	2N4209

Table 6-3. Replaceable Parts

Reference Designation	HP Part Numbor	C D	Qty	Description	Mfr Code	Mfr Part Number
АСНІ Авнэ Авнэ Авна Авна Аднь	0757.0280	1		hijt Acompt D Hijt Acompt D Nijt Acompt D Hijt Acompt D Hijt Chill F (m, 1765) F (-0) (00)	24b4#	C4-1-8 10 1001 F
Апно Абн7 Адни Адни Адни)	0767-1004 0608-3446 0767 0401 0608-7,740 0608-7,740	8 3 0 7 4	\$	816161031478435475497100 816161013134345475497100 81616101404555697100 81616101408455697100 816161014084556941000	74648 74648 74648 74648 74648	C4 1-0-10 1471-7 C4 1-0-10 302-7 C4 3-0-10 10 1 C4 3-0-10 10 10027 C4 1 8-3 10027
АВН11 АВН12 АВН13 АВН14 АЛН16	2100-1738 0767-0447 0767-0760 0698-8460	8 8 9 9	10	NOT ANDIONED REDISTOR-THARLOR TONIC TOPIADUSTIPN REDISTOR FOR IN: 126WFT (C-01100) REDISTOR FRIN, 126WFT (C-01100) REDISTOR 6100 TO STATE AVFT (C-014)	32007 24646 24646 24646 26460	3770(++)-103 (4 : H-10-1002) (4 : H-10-1002) (6 : H-10-1002) (6 : H-10-1002) (6 : H-10-1002) (6 : H-10-1002) (6 : H-10-103) (6 : H-10-103) (7
АБНІВ Абрія Абрія Абрія Абрія	2100-3758 0658-8469 0698-8469 0698-8469 0698-8469 0699-10642	6 1) 00 1	1	N 5151 ON TAME 20 YON C 5001 ADJ 17 TAN AF51510A 6 80K YN YWY TC-074 AR51510A 6 90K YN YWY TC-074 AF51510A 6 90K YN YWY TC-074 AF51510A YOK YN YWY TC-076	28480 28480 28480 28480 28480 28480 28480	5100 3266 0608 8460 0608 8469 0608 8469 0608 0643
AE 1171 AE 1175 AB 1173 AB 1173 AB 1174 AB 1176	2100-3357 0688 0831 0688 0831 2100-3737 0688 0933	13 15 19 17 19	1 1 3	ПЕБІЗГІЛІ-ТРИЛЕТОО ТОЧЕС БИЛЕ АЛІ І / ТРИ REBISTUR 9 06K ТХ ТИУ / ТС-ОТВ REBISTUR 77 307K ТХ ТИУ / ТС-ОТВ REBISTUR 77 307K ТХ ТИУ / ТС-ОТВ REBISTUR 77 307K ТХ ТИУ / ТС-ОТВ	28483 28483 28483 28483 28480 28480	,100-3367 000-0631 000-0631 2100-3732 000-3732 000-0033
Абијо Абијј Абији Абији Абији	7100-3737 0688 0034 7100-3737	7 4 J	1	₩61510H-TANH 600 10± C 5031-ADJ 17 TAN ₩515-DA 35 #50K 1± 1₩7 TC=016 ₩61510H-TANH 600 10± C 5031-ADJ 17-TAN NOT ASSIGNED NOT ASSIGNED	70480 28480 78480	7100 3735 0800 0934 7100 3737
ABN31 ABN32 ABN33 ABN34 ABN34 ABN36	0608 6469 0608 6469 0608 6469 0608 6469 2100-3765 0654 6469	0 0 0 4 0	1	REGISTOR BUDN 1% 1WF 1C-0+4 REGISTOP BUDN 1% 1WF 1C-9+4 REGISTOR BUDN 1% WF 1C-0+4 REGISTOR BUDN 1% 10% C GUDT-ADJ 17-TRN REGISTOR BUDN 1% 1WF 1C-0+4	28480 28480 28480 28480 28480 28480	0698.8469 0598.8469 0608.6469 2100.3765 0508.8469
аллэл Аллэт Аллэт Аллэн Аллэн Аллэн Аллэн Аллан	0848-8827 7100-3760 0698-6827 0699-0164 0698-6867	4 1) 4 15 11	57	ALSISTUA I M 1%, 178WF IC-01100 REDISTOR-TRMR 206 10%, C SIDE-ADJ 17-TRN REDISTOR I M %, 17EWF IC-01100 REDISTOR 7 26, 1%, 17EWF IC-0110 REDISTOR 7 36%, 26%, 17EWF IC-0100	28480 28480 28480 28480 28480 28480	0608 6827 2114)-3760 0608 6837 0608 61837 0608 6863 0608 6863
авна 1 Авна 7 Авна 7 Авна 4 Авна 4 Авна 6	0167-0447 0698-3760 0698-3160 0767-0447 0698-3760	6 6 9 9	4 7	RE5/510R 10K 1% 176WF 1C-0:100 RE5/510R 464K 1% 176WF 1C-0:100 RE5/510R 464K 1% 126WF 1C-0:100 RE5/510R 10K 1% 126WF 1C-0:100 RE5/510R 464K 1% 126WF 1C+0:100	74646 78480 74646 74646 74646	C4-128-T0-1002-1 0608-3260 C4-128-10-22331-1 C4-128-10-100233 0608-3280
Алиа Алиа Алиа Алиа Алиа Алиа Алиа Алиа	0698-3150 0767 0471 0767 0421 0767 0421 0898-3447 0698-3447	15 4 4 7		RE5/5108 2.378 1% 126W F 10-03 100 RE5/5108 826 1% 126W F 10-03 100 RE5/5108 826 1% 126W F 10-03 100 RE5/5108 826 1% 126W F 10-03 100 RE5/5108 186 1% 126W F 10-03 100	24848 24848 24848 24848 24848	(4+1/8+10-7371) (4+1/8+10-8351) (4+1/8-11-8351) (4+1/8+10-8351) (4+1/8+10-8351) (4+1/8+10-1088)
АЛРЫ Алры Алры Алры Алры Алры	0698-3446 0698-0684 0767-0394 0698-3463 0698-8627	70074	3	NE61510134835.126WFTC-01100 NE615101316K15.126WFTC-01100 NE6151016113527770 RE615101168K15.126WFTC-01100 RE615101168K15.126WFTC-01100	24546 24546 24546 24546 26460	C4-1 8-TO 34681 C4-1 8-TO 7161-2 C4-1 8-TO 7181-2 C4-1 8-TO 1083-2 C4-1 8-TO 1083-2 O688-8877
аблаа (блаа) 8608а 8609а 8600а	0698-3169 0698-3786 0767-0780 0698-7736 0698-7736	6 6 7 7 7	j I	РЕБІБТОР 28 ТА ТА ТАБУ 7 ТС-ОД 100 НЕБІБТОР ХАЛА ТА ТАБУ 7 ТС-ОД 100 НЕБІБТОР ТА ТА ТАСУ 7 ТС-ОД 100 ЯБІБТОР ТА ТА ТАСУ 7 ТС-ОД 100 ЯБІБТОР БІ ТА ТА ОБУУ 7 ТС-ОД 100	54848 24848 24848 24848 24848 24848	C4-17/B 112-261221 C4-17/B 112-251337 C4-17/B 112-237337 C4-17/B 112-120117 C4-17/B 112-120117 C4-17/B 112-25
Абрбі Алра? Абраз Абра4 Алра6	0898-7277 0767 0468 2100 2030 0898-7760	 		АББІБТОЛ БІ ТК ТК. ОБУУ Г ТСНОТТОР НЕБІБТОЛ БІ ТК ТК. Т2БУУ Г ТСНОТТОР ВЕБІБТОЛ ГАЛИ 20К ТОК С ТОР АОД 5-ТРИ ЯББІБТОЛ ГАЛИ 30К ТОК С ТОР АОД 5-ТРИ НОГ АББИЛЕД	,4848 '4846)3997 74646	C4-57 (5 11) 5 11 (7 7 C4-17 (8 11) 5 11 (7 0 3 1 (9) - 5 - 20 3 C3-17 (8 10 100 (7 7
Абі-бө Абі-ба Абі-ан Абінен Абінен Абінен	0698-7272 0698-7253 2100-2516 2100-2516 2100-2516	1 1 1 1		RESISTOR 31 6K 1% 05WF 1C=0±100 RESISTOR 511K 1% 05WF 1C=0±100 RESISTOR 1RMR 100K 10% C 5IDI-ADJ 1-TRN RESISTOR 1RMR 100K 10% C 5IDI-ADJ 1-TRN NOT ASSIGNED	74646 74646 37097 32057	C3-178-19-2167-6 C3-128-10-6110-6 J3789-104 J3399-104
абяті Арят; Хонт; Асят4 Абят6	0698-7237 0608-7242 7100-7621 2100-2621	9 5 0 0		RESISTOR FIR IN DEW FILL OF TOO RESISTOR FIRM IN OBWEILS OF TOO RESISTOR TRAIN IN TONIC SUBLACLET TRA RESISTOR TRAIN IN TONIC SUBLACLET TRA NOT ASTRONED	74640 74646 37897 37887	C3 1/8 10/110/16 C3 1/8 1780 6 3329W-1-202 3329W-1-202
АВН76 Абр77 Абр77 Абр78 Адр76 Адр76 Адр76	0698 7283 0698 7786 7100-2897 0689-7743 0689-7743 0688-3167	****		REBISTOR BO 9+ 14, 12EWFTC ±100 REBISTOR 110K 14, 05WFTC-01100 REBISTOR 14MR 144 204 C 50C ADJ 1 184 RE55TOR 1 94K 14, 05WFTC-01100 REBISTOR 2 48K 14, 05WFTC-01100	24646 24648 32887 24646 24646	C3-1, B-1()-0(B2-6 C3-1, B-1()-11(0)-6 J320W-1-108 C3-1, B-1()-5861-6 C4-1, B-1()-3483-7

Table 6-3. Replaceable Parts

See introduction to the section for ordering information *Indicates factory selected value

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Reference Designation	HP Part Number	0 D	CIY	Description	Mfr Codo	Mfr Part Numbor
An fin 1 An fin 2	0688-7760 CR98-7743	1		19855130 100 (5. 26002 10-03 100) 19865130 1986 (5. 36002 10-03 100)	24040 24640	C2 1. 8 10 1081 G C3 1/8 10 10 10 15
AD1#1 AD1#2 AD1#2 AD1#4 AD1#16 AD1#16	1961 489 1961 489 1961 489 1961 489 1961 489 1961 489	4		034647 (108-10 205 M 2051-1514 (136647 138-10 205 M 2054-1514 (136647 138-10 205 M 2054-1514 (136667 138-10 205 M 2054-1514 (136667 130-16) 205 M 2054-1514	28480 28480 28480 28480 28440 28440	1361-4637 1361-4637 1561-4637 1561-4637 1361-4637
AD 14'0 AD 14'7 AD 14'1 AD 14'1 AD 14'1 AD 14'1	1981-4833 361 4833 1981 4837 1981-4837 1981-4837 1981-4833	4		CONTECTOR TO THE MENDED TO FE CONTECTOR TO FILE MENDED TO FE	20480 20480 20480 20480 20480 20480	1761-4677 1761-4677 1761-4677 1761-4677 17614677
AB133 AB133 AB133 AB134 AB136 AB136) #26 () 22() 1920 121 1920 121 1920 120 1920 () 220 1926 () 421	4 15 16 4 7	6 1 10	IC BYMTCH ANGLEQUAD TO GIPC PNG IC GATE TTE EN EXCON COARD 2 HIP IC TE TTE EN EXCENTION FOIL THAT CTIM IC TE TTE EN EXCENTION FOIL THAT CTIM IC OP AMP 4000 DHAT TO 80 CAG	00865 01785 01785 01785 07685 28480	639 (771) 64746688 64746674 647746674 647974 1878 (747) 1878 (747)
kitiji Kitiji Kitiji	1825-0421	1	,	IC OP AMP (1955-1904) 123 00 FM3 NOT ASSISTED IN A INCLUSION AND AND AND ADDITION	26480 01.185	1826-0423 Notat N 1445
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	18870 1917 1870 1930 1874 19417	ő N	'	- IC FF 315 3 8 D 1518 PD8 F7817-1903 IC FF 715 55 D 1518 P35 F7817-1903 IC RWSTEIF ANSIS PDWAIF 18-30P C PAG	01285 01285 27014	6N 741 6 74AN EN 741 67 73N LF 7 3 3 3 3 0
486499 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 48649 486649 48649 48649 48649 48649 4864946649 48649 48649 48649 4866	167634457 167634677 1876374777 187667776 187667776 187667776	n n 3 3 7	b	IC 65541CH AND GHAD 10-00°C (150) IF A THE & 65 5471 POS ED03-1883 IC DRVR 114 EB UNE DRVR 0C11 IC COMPARATOR 1966 100 00 APO IC OP AMP 1059 DRIFT 10 80 PFG	27014 01295 01295 01295 01295 28480	171333313 65774157445 65774157445 15776154 1577615471
UE1117 UE117 UE117 UE118 UE178 UE1781	1830 (748) 1870-(714) 1876 (757) 1878 (747) 1878 (747) 1878 (747)	1 3 2 1 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2	١	18 GATE TTE ES AND DOAD 7 INP 18 DY 18 DTE ES 3-10 BEINE 3 INP 18 DY 19 DTE ES 3-10 BEINE 3 INP 18 DY 19 DY 19 DE TE 10 BEFES 18 DP AMP EDW DRUT TO BEFES 18 DP AMP EDW DRUT TO BEFES	01705 01705 74355 78480 38480	6777416000 67774161386 AD764380 18761077 187610771
UNU27 UNU27 UNU23 UNU24 UNU24 UNU26	1870-1707 1870-1187 1876-1907 1876-1907	1 11 2 3		іс (JATE TTL L6 NAND TYL 3 INP іс (JATE TTL L6 NAND CJAD 2 INP іс сіліралатын Ріссу то 80 гжд іс сірамрагруда то 80 гжд іс оргамр дар Кіласто 90 гжд істра Албаліта	01798 01796 01796 01796 78480	6N 741 61 CN 6N 741 6000 1 M 31 1 6 1 H 7 H 100 97
LEU20	1850 (J) 86	5		IC OP AND SPCC 10 00	31.000	CA 3080
avni avvi	1801-2002 1807-2002	1 0		DIDDE-FNB 2 37V 6N DO-J PD+ AW 10+- 07AN WIRE 22AWA3 W PSC 1522 ROC	20480 20480	1907-3002 #156-0065
8173 8773 8754	8160-0X0D	U		hot Abbunto Whit JJAWG W PAT 1873 Roc Not Abbunto	20480	816B (XXI)5
<b>N7</b>	新1888-8008-8008-8008-800-800-800-800-800-	4		BD ASSY YTM DNIVTA (DOES NOT INCLUDE DO- I'N 14 ADI N P2 OR FACTURY SLLECT RESISTORS 1124° THRUNCH R30° AND HRS° THRUNUI HFT°)	28480	83686 60368
NJC) NJCJ NJCJ NJC4 NJC6	0160-4084 0160 2877 0160 0167 0160-2870 0160-2877	8 6 1 7 6	ł	CAPACITUR FRD 10F 170% E000C CER CAPACITUR FRD 100FF 170% 70050C ALB CAPACITUR FRD 10770F 110% 70050C CER CAPACITUR FRD 1010F 170% 70050C CER CAPACITUR FRD 100FF 170% 70050C CER	28480 28480 28480 28480 28480 28480	01604004 63303077 01600167 01603870 01603877
NJCH NICJ NICH NICH NICHO	01600674 01800118 01800118 01807818 01807818 01800118	1		САРАСНОЙ РАЙ ФЛЛИР + 10Х ТООХИССЕН САРАСНОЙ РАЙ В ВИИТ ТОХ ЗБУЮСТА САРАСНОЙ РАЙ В ВИИТ ТОХ ЗБУЮСТА САРАСНОЙ РАЙ ВОСТ ГОХ ТОУЮСТА САРАСНОЙ РАЙ В ВИИТ ТОХ ЗБУЮСТА	78480 56280 56280 78480 56280	01600674 16006865703507 16006865903507 01807815 16006865903587
N7C11 N7C12 N7C12 N7C14 N7C18	01800778 01600674 01601870 01603878 01603878	ñ 37 6		CAPACITOR END 220F1 10% 16MDC TA CAPACITOR END 0220F1 10% 160MDC CER CAPACITOR END 1010 - 20% 100MDC CER CAPACITOR END 1000FF 120% 100MDC CER CAPACITOR END 1000FF 120% 100MDC CER	567#¥ 28460 28460 28460 28460 28480	1600770501687 0160 0674 0160 7879 0160 7879 0160 7878 0160 3878
NTC18 NTC13 NTC18 NTC18 NTC10 NTC20	0180-0676 0180-2731 0160-3874 0160-4084 0160-4084 0160-0228	4 1) 7 8 6		CAPACITUM END OFFUE FOR BOVIN CEM CAPACITUM END 2 744 ETON BOVIN CEM CAPACITUM END 1047 E BHY 200400 CEM CAPACITUM END 14F E 20N BOVING CEM CAPACITUM END 2244 ETON BOVING TA	28480 25480 25480 28480 28480 55289	0160 0635 0160 7731 0160 3874 0160-4084 16003783901587
M(7)	0180-2784	e	1	CAPACITUR FOID 3 SUF FOON SOUDC TA	06761	NDB 51%-335-20/0042
NJCHI NJCHJ NJ PJ NJCH4 NJCH3	1801-0535 1801-0535 1801-0033 1801-0033 1801-0033	9 ] ] ] ] ] ] ] ] ]	7	0001-8M Big Behottry Diodi-8M Big Behottry Diodi-6D FRI Hov 200MA DO 7 Diodie Gen FRI Hov 200MA DO 7 Diodie Gen FRI Hov 200MA (NO 7	38480 78480 28480 28480 28480 28480	1631-0636 1801-0638 1801-0633 1801-0633 1804-0633
176110 176117 176119	1901-0032 1901-0626 1901-0032	7 0 7		Diode-gen Prip 1809 200MA DO-7 Diode-em 51g Schottry Diode-gen Prip 1809 200MA DO-7	78480 28480 28480	1801-0013 1801-0013

## Table 6-3. Replaceable Paris

See introduction to this set uon for ordering information *Indicates factory selected value

Reference Designation	HP Port Numbor	C D	Qiy	Description	Mfr Coda	Mfr Part Numbor
A7680	1001 0636	U		ліял-ба ба всняттку	78481)	1001 0535
ATIS	1200-0626	1	۱.	BOCKET IC 20 CONT DIP DIP 6188	38480	1700-0876
AJL 1 AJL 7 AJL 3	9140-0137 9140-0137 08503-80901	1		INDUCTOR RECEIVED INCOMENTATION AND AND A COMENT INDUCTOR RECEIVED INCOMENTATION AND A COMENT CORE TORORD	78480 78480 78480 78480	91400137 91400137 4 503#0001
ајмрі Ајмрј Ајмрј Ајмрј	1,040 8844 1,000 8043 1,200 0173 1,200 0173	0 0 1	1	I STRACTOR BOARD PN PC BOARD ESTRACTOR INSULATOR SETR OAP GL INSULATOR-SETR OAP GL	78480 78480 78460 78460 78460	6040 nH44 6000 8043 1700 0373 1700 0373
A7P1 A7P2	1261-7204	•	۱	NOT ADDINT D HEADER 20 FIN	284NO	1261-7204
A70) A702	1862-0044 1863-0044	3	4	10ANE16108 ENE 61 10-29 ED-19-17-200MH2 18AN516108 ENE 61 10-29 ED-19-17-200MH2	28480 28480	1863 0044 1863 0044
АЛЛ АЛЛ АЛЛ АЛЛ АЛЛ АЛЛ АЛЛ АЛЛ	UF57-0443 0757-0430 0757-0458 0757-0458 0757-0442 0698-3449	b ] 7 U 0		RESISTOR LER 1% 126WF 1C-02100 RESISTOR 760 1% 126WF 1C-01100 RESISTOR 81 1% 1% 126WF 1C-01100 RESISTOR 81 1% 126WF 1C-01100 RESISTOR 2875 1% 126WF 1C-01100	74648 74648 74648 74648 74648 74648	C4-128-10-11077 C4-128-10-763-7 C4-128-10-763-7 C4-128-131-1007-1 C4-128-142-28737
АЛКВ Алкт Алкв Алкв Алкв Алкв	0688 0083 0888 0083 0757 0447 0757 0447 2100-3611	8 9 9 1		РЕБЕТОВ Т. ВС., 12, 125 W F. 10-01, 100 ВЪБТОВ Т. ВАК 12, 125 W F. 10-01, 100 ВЪБТОВ 104 13, 125 W F. 10-01, 100 ВЪБТОВ 104, 13, 125 W F. 10-01, 100 ВЪБТОВ-ТАКИВ ВОК 102, 0 БОД-АДЈ 17-18 ВЕБТОВ-ТАКИВ ВОК 102, 0 БОД-АДЈ 17-18 ВЕБТОВ 5 87К 12, 125 W F. 10-01, 100	74648 74648 74513 74548 74548 37087	C4-17H-10-1981-7 C4-17H-10-1981-7 C4-17H-10-1982-7 C4-17H-110-1882-7 37073-1-503
AJB11 AJB12 AJB12 AJB13 AJB13 AJB16	0757-0700 7100 3611 0757-0447 0757-0447 0698-3760	7 1 4 9 9	1	PEDISTOR 6 87K 1% 175W/ 1C-01100 PEDISTOR FRANK UK 10% C BOL ADJ 17-TRN REISTOR 16 2K 1% 175W/ 1C-01100 REISTOR 10K 1% 175W/ 1C-01100 REISTOR 464K 1% 175W/ 1C-01100	74646 37007 74646 74646 74646 76480	C4-17,8-10,8621-9 32835-1-603 C4-17,8-10,162279 C4-17,8-10,1622-9 0698-2260
А/П.В А/П.В А/П.В А/П.В А/Г/О А/Г/О	0757-0780 0698-1457 7100-1611 2100-1737 0699 0796	7 15 1 7 7 7	1	Атбібтій ік із. 126991.10-031.00 Абібтій зійк із. 126991.10-031.00 Абібтій зійк із. 126991.10-031.00 Абібтій аймана або гос сбійсарі 17.184 Абібтій ; 2068. 13. 1991.10-044	74648 78480 37897 78480 78480	(4-1, 8-10-1001-) 0808-3457 37027-1-603 3700-3737 0890-9788
A3471 A3472 A34723 A3473 A3473 A3473	0600-6406 7100-3746 0600 0600 7100-3767 0600 0401	1 15 10 10	4	РЕБІБТОЛ В ВАК. 1 %, 1 № 7 ТС-0+4 НЪБІЗТОЛ-ТРАРА БА, 10%, С БІОТ АДЈ 37-ТРА НЪБІЗТОЛ-ТРАРА БА, 10%, 1 €С 0+4 НЪБІБТОЛ-ТРАРА 100 ТОХ С БІОТ АДЈ 17-ТРА РЕБІБТОЛ 0.0416, 1 %, 1 № 7 ТС-0+4	28480 28480 28480 28480 28480 28480	0698-0405 2100-3240 0699-0803 2100-3262 0699-0001
A7078 A7071 A7028 A7070 A7070 A7070	0598-8950 0598-8950 0757-0444 0757-0442 10757-0442	N 4 1 9 2	1 4 2 2 3	невіятоні лбик (ж. 128997 ГС-01 (ж) періятоні так (ж. 1997 ГС-01 (ж) періятоні так (ж. 1997 ГС-01 (то періятоні так (ж. 12899 ГС-01 (то періятоні тарк (ж. 12897 ГС-01 (то)	78480 78480 74646 74646 74646	0688 8860 0688 8489 (4),4:10:4317,4 (4),4:10:4317,4 (4),4:10:1037,4 (4),10:10:1633,4
атрэі Арээ Арээ Агрээ Агрэа Агрэа	0767 07447 0767 0774 0698-2462	10 15 1		REDISTUR TOK 1% 126WFTC-01100 REDISTUR 121K 1% 126WFTC-01100 REDISTUR 100K 1% 126WFTC-01100 RACTORY BELECTED NOT REPLACEABLE FACTORY BELECTED NOT REPLACEABLE	74646 74646 7 46	C4-U-8-10 1002+F C4-U-8-10 1711+F C4-U-8-10-1982 F
A7H36* A7H37* A7H38* A7H38* A7H40	1350B-#489	4		FACTORY BLLECTED, NOT REPLACEABLE FACTORY BLLECTED, NOT REPLACEA, LE FACTORY BLLECTED, NOT REPLACEA, LE FACTORY BLLECTED, NOT REPLACEABLE REDISTOR (BK: 13), 1397 (C=0.100)	28440	មិតម៉ង់ សំ4អមិ
Ajka) Ajkaj Ajkaj Ajka Ajka	0608 6406 2100 3611 2100 3760 0611 1037 2100 3763	1 9 10 7	7	REBISTOR B BAN, 1%, 1097 TC=0+4 REBISTOR-TRIMB BON TOX, C BIDT-ADJ 17-TRN REBISTOR TRMB TON TOX, C BIDT-ADJ 17-TRN REBISTOR TEN TA TW PAY TC=0, 70 REBISTOR-TRMR TOX, FOR C BIDT-ADJ 17-TRN	78480 37097 37997 38480 58480	UGUH (14UN 3707A-1-603 3707A-1-703 0411-1037 2400-3763
A7N48 A7N47 A7N48 A7N48 A7N60	2100-3611 0767-0789 '9767-0440 0698-6771 0698-8877	1273	1	PE665108-16MR 808 109 C 6602-803 17-16N R565108 13 38 13, 176393 1C-01100 R5665108 7 56 13, 126997 1C-01100 R565108 108 13, 126997 1C-0126 R665108 108 13, 126997 1C-0126	3300 F 10701 24540 28480 28480	32023-1-803 NF4C1-8-11-1322-} C4-1-8-10-7801 F UCOB B721 UCOB NP2F
ајны Ајны Ајныј Ајны Ајны Ајны	2100 0870 0696 8827 0696 3169 0698 8968 2100 2517	0 4 5 7 4	;	РЕБІБТОЛ-ТАМИ ТОК ТОХ С БІДЕ-АДІ 17-ТРИ НБІБТОЛ ІМ 1Х, 12569 Г ГС-ОТ ІОО РЕБІБТОЛ 26 ТК ТХ 12669 Г ГС-ОТ ІОО РЕБІБТОЛ 26 ТК ТХ 12669 Г ГС-ОТ ІОО РЕБІБТОЙ-ТАМИ ВОК ІОХ С БІДЕ-АДІ 1-ТРИ	33997 28480 24648 28480 28480 20683	3202X-1-103 0600 n827 C4-1, b 10-2012 / C407, b06b 11500503
аль Аль Альр Альр Альр Альс	0767 0780 0767 0780 0767 0443 0811-1037 0688 008+	1 0 0	,	Азбібтолік і х. 12600 fC=03100 Азбібтолів віда і № 12600 fC=03100 Азбібтоліо IX 12600 fC=03100 Азбібтолія IX 12600 fC=03100 Азбібтолія IX 12600 fC=03100	74646 10701 74646 78480 78480 74616	C4-12(B-13)-1001(F AFAC)2(2-10)(FB1)F C4-12(B-10)-10027(F OB151-1037) C4-12(B-10)(F1057) C4-12(B-10)(F1057)
A1061 A1062 A1063	0608-0084 0757 5+45 0757-0444			ребібтон 7 ток і 1 78 м/ то-оттой Небібтог ток і 1 78 м/ то-оттой Ребібтон 17 тк і 1 76 м/ то-оттой	74840 74640 74640	64-178-10-2161-4 64-178-10-100274 64-178-10-10-1212
			1			

Table 6-3. Replaceable Parts

See introduction to this section for ordering information *Indicates factory selected value

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Designation         Num           Arres         01670           Arres         01000           Arres         01000           Arres         10000           Arres         10000           Arres         17616           Arre	4 4 9443 9443 9444 9443 9445 9455 9555 957744 9555 957754 9575 9575 9575 9575 9575	900 3880 BF 000000 333330 H6443 87773 778887	1 3 4 17 7 7 7	REBISTOR 100-1X       17600/1C-0100         MEDISTOR 100-1X       17600/1C-01100         IACTORY BILLCTED NOT REPLACEABLE         FACTORY BILLSTOR NOT REPLACEABLE         FACTORY BILLSTOR NOT REPLACEABLE         CONNICTOR BILL NOT NOT REPLACEABL	Code 74045 74045 74045 74045 74045 74045 74045 74046 78480 78480 78480 78480 78480 78480 78480 78480 78480 78480 78480 00000 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 01705 0000000000	C4-1/8-10-1002-7 C4-1/8-10-1002-7 C4-1/8-10-1002-7 C4-1/8-10-1002-7 C4-1/8-10-1002-7 C4-1/8-10-0128-7 C4-1/8-10-0128-7 C4-1/8-10-0128-7 C4-1/8-10-012-7 C4-1/8-10-012-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02-7 C4-1/8-10-02
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A752         3101 0/           A757         3101 0/           A7107         1/b1-87           A7108         1/b1-87           A7109         1/b1-87           A701         1/b1-97           A701         1/b26-01           A701         1	571 573 573 573 573 573 573 575 575 575 575	F 00000 0000 13330 #6443 87773 7788	17 4 3 2	<ul> <li>ANTCH PER DIP BER ADDY TO TA UDA JOVIC</li> <li>CONNECTOR &amp; PEN M POST INP CONNECTOR &amp; PEN M POST INP CONNECTOR &amp; PEN M POST INP CONNECTOR BEEN M POST INP CONTRELES TO BEED TO BEED TO IC DRAFT ILS LINE OWN POST IC DRAFT ILS BEEN DO BEEN DI CONTRELES INPOST OF POST IC DRAFT ILS BEEN DO BEED TO IC FETTI AND OUAD TO BEED C PAG IC OP AMP LOW DRAFT TO BE PAG</li> <li>IC CONV 17-8 DATA 18-DIP C PAG</li> <li>IC OP AMP LOW DRAFT TO BE PAG</li> <li>IC CONV 17-8 DATA 18-DIP C PAG</li> <li>IC OP AMP LOW DRAFT TO BE PAG</li> <li>IC CONV 17-8 DATA 18-DIP C PAG</li> <li>IC OP AMP LOW DRAFT TO BE PAG</li> <li>IC CONV 17-8 DATA 18-DIP C PAG</li> <li>IC OP AMP LOW DRAFT TO BE PAG</li> <li>IC CONV 17-8 DATA 18-DIP C PAG</li> </ul>	78480 78480 78480 78480 78480 78480 78480 78480 78480 00000 01121 01121 01121 01121 01121 01121 01121 01121 01205 01205 04885 04713 01205 74355 74355 74355 74355 74355	3101 0471 1781-6618 1781-6618 1781-6618 1781-6618 1781-6618 1781-6618 1781-6618 1781-6618 1781-6618 08088 BY DESCRIP KDN 7104727 3104727 3104727 3104727 3104727 3104727 3104727 3104727 3104727 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 310472 310472 310472 310472 310472 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 310472 310472 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6618 3101-6
ATTP2         Jobie           ATTP2         Jobie           ATTP3         Jobie           ATU3         Influg           ATU3         Influg           ATU4         Influg           ATU5         Influg           ATU5 <td>198 199 199 199 199 199 199 199 199 199</td> <td>0000 0000 13330 86443 87773 7788</td> <td>4 7 2</td> <td>CONNECTOR BANK M POST TYP OTHER COR BANK M POST TYP CONNECTOR BANK M POST TYP TELMMINAL TEST POINT POST TYP CONNECTOR BANK M POST TYP TELMMINAL TEST POINT POST TELMMINAL TEST POINT POST CONNECTOR PONE CONNECTOR PONE CO</td> <td>78480 78480 78480 78480 78480 78480 78480 78480 00000 0171 0171 0171 0171 0171 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 00000 00000 00000 00000 00000 000000 0000</td> <td>1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1271-6616 1271-6617 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 1270-6710 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0000 13330 86443 87773 7788	4 7 2	CONNECTOR BANK M POST TYP OTHER COR BANK M POST TYP CONNECTOR BANK M POST TYP TELMMINAL TEST POINT POST TYP CONNECTOR BANK M POST TYP TELMMINAL TEST POINT POST TELMMINAL TEST POINT POST CONNECTOR PONE CONNECTOR PONE CO	78480 78480 78480 78480 78480 78480 78480 78480 00000 0171 0171 0171 0171 0171 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 0170 00000 00000 00000 00000 00000 000000 0000	1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1261-6616 1271-6616 1271-6617 1270-6710 1270-6710 1270-6710 1270-6710 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ATTP7         155.5           ATTP7         155.5           ATTP7         155.5           ATTP7         155.5           ATTP7         1810.0           ATU1         1810.0           ATU2         18           ATU2         18           ATU3         1810.0           ATU3         1870.7           ATU4         1870.7           ATU5         1870.0           ATU10         1870.0           ATU11         1870.0           ATU12         1870.0           ATU13         1870.0           ATU14         1870.0           ATU15         1870.0           ATU14         1870.0           ATU15         1870.0           ATU14         1870.0           ATU15         1870.0           ATU14         1870.0           ATU15         1870.0           ATU	124 133 1777 1777 180 184 1077 1077 1077 1077 1077 1077 1077 107	0000 33330 M6443 M7773 776M	2	CONNICTOR & PNN M POST ISP CONNICTOR & PNN M POST ISP TERMINAL 15 BT POINT PCD STRUCTOR & PNN M POST ISP TERMINAL 15 BT POINT PCD STRUCTURE REG 10 5019 2 K OHAL S U IC SAVE TIL IS LINE ORVER OCTL IC SAVE TIL IS LINE ORVER OCTL IC DRVE TIL IS LINE ORVER OCTL IC DRVE TIL IS LINE ORVER OCTL IC TRUE TIL IS LINE ORVER OCTL IC TRUE TIL IS BUS QUAD IC ORIGINAL IS BUS QUAD IC ORT IS IS A STRUCT SAVE IS A STRUCT AND IS A STRUCT IC OP AMP SOVER ON TO STRUCT A STRUCT IC OP AMP SOVER IS TO STRUCT AND IC OP AMP SOVERIAS IS IN PD DUAD 14 DIP C IC OP AMP SOVER IS TO STRUCT AND BOTH TO STRUCT IC OP AMP SOVER IS TO STRUCT AND IC CONV 17-8 DAVA 18-DIP C PRO	2#480 98480 00000 01121 01125 01205 01205 01205 04213 04213 01205 24355 24450 01205 24450 01205	1261-6618           1261-6618           0H018 BY DESCRIP ION           2104222           204225           5N7416744N           6N74161244N           6N74161244N           6N74161244N           6N7416124AN           6N7416126128AN           6N7416128AN
A7U2     18     50       A7U3     18     60       A7U4     1870     1876.01       A7U5     1870.16     1876.01       A7U5     1870.16     1876.01       A7U8     1870.11     1876.01       A7U1     1876.01     1876.01       A7U1     1876.01     1876.01       A7U1     1876.01     1876.01       A7U10     1876.02     1876.01       A7U12     1876.04     1876.04       A7U13     1876.04     1876.04       A7U14     1876.04     1876.04       A7U15     1876.04     1876.04       A7U16     1876.04     1876.04       A7U17     1876.04     1876.04       A7U18     1876.04     1876.04       A7U19     1876.04     1876.04       A7U10     1876.04     1876.04       A7U11     1876.04     1876.04       A7U21     1876.04     1876.04       A7U21     1876.04     1876.04       A7U21     1876.04     1876.04       A7U21     1876.04     1876.04       A800     1876.04     1876.04       A800     1876.04     1876.04       A800     1876.04     1876.04       A800	774 56 64 774 775 71 86 71 86 71 86 71 86 71	3330 80443 87773 7788	2	h tryonk he to 500 2 m onto 5 ú IC SAM TTL IS LINE ONVRIACTI IC DRVR TTL IS LINE ONVRIACTI IC DRVR TTL IS LINE ONVRIACTI IC DRVR TTL IS LINE ONVRIACTI IC INFIT TTL IS DUS QUAD IC INFIT TTL IS DUS QUAD IC INFIT TTL IS DUS QUAD 2-INP IC SAMTCH AND QUAD 16-DIP C PAG IC OP AMP SOW BIAS II IM PD DUAD 14-DIP C IC IF TTL IS D-TYPE POS-I DGE-TRIG DOM IC ODY 12-II D-A 18-DIP C PAG IC OP AMP SOW DIAS II TO 90 PAG IC OP AMP SOW DIAS II TO 90 PAG IC OP AMP LOW DRIFT TO 90 PAG IC ODY 12-II D-A 18-DIP C PAG IC OP AMP LOW DRIFT TO 90 PAG IC OP AMP LOW DRIFT TO 90 PAG IC ODY 12-II D-A 18-DIP C PAG	01171 01705 01705 01705 01705 01706 04703 04713 01705 74355 74450 78480 01705	210222 by 7415744y by 7415744y by 7415744y by 7415774 by 7715 by 7711 by 7711b
A7UB         1870 11           A7UB         1876 07           A7U1         1876 07           A7U13         1876 07           A7U14         1876 07           A7U15         1876 07           A7U16         1876 07           A7U17         1876 07           A7U18         1870 04           A7U19         1876 07           A7U10         1876 07           A7U11         1876 07           A7U10         1876 07           A7U21         1876 04           A8020         0180 04           A8021         0180 04           A8021         0180 04           A8021         <	44 700 700 87 71 80 71 80 71 80 71	0443 87773 778 H	,	IC GATE TTLLS ADD DUAD 2-INP IC SWITCH AND GAD IS DIP C PAG IC SWITCH AND GUAD IS DIP C PAG IC OF AMP LOW BIAS IS INP D DUAD 14-DIP C IC OF AMP LOW BIAS IS INP D DUAD 14-DIP C IC CONV 12-IS DATE POST DUE-TRIG COM IC CONV 12-IS DATE TO 93 PAG IC OF AMP LOW DRIFT TO 93 PAG IC OF AMP LOW DRIFT TO 93 PAG IC OF AMP LOW DRIFT TO 93 PAG IC CONV 12-IS DATE SOURCE PAG IC CONV 12-IS DATE SOURCE PAG	01286 06866 04713 01286 24366 28480 78480 01286	6N 741 50770 6W 07703 6W 07703 MC 340048L 5N 741 51 74N AD78438D 10780 471 10780 0471 1028 0471 5N 741 51 38N
A1013         1856 07           A1014         1876 04           A1015         1876 07           A1010         1876 07           A1011         1876 04           A1011         1807 04           A2027         1876 04           A1011         1807 04           A2027         1876 04           A1011         1807 04           A2027         1876 04           A101         1800 01           A2010         1800 01           A2010         1800 01           A2010         1800 01           A2010	67 71 10 71 61 61 71	7773 7788	,	К СОЛУ 17-0 В/А 16-01С СРАС К ОЛ АНУ КОУ ОЛИТТО 90 РАС I СОР АНУ КОУ ОЛИТТО 90 РАС I СОР АНУ КОУ ОЛИТТО 90 РАС I СОСЛИТТЕ 15 2-110-0-1105 2-16Р I ССОЛУ 17-0 Б/А 16-01Р СРАС I С ОЛУ 17-0 Б/А 16-01Р СРАС	24365 28480 28480 01285	AD76478D 1878 0471 1878 0471 5874651388
ATUIN         1956 04           ATUIN         1956 04           ATUIN         1876 07           ATUIN         1876 07           ATUIN         1876 07           ATUIN         1876 07           ATUIN         1876 04           ATUIN         1876 04           ATUIN         1876 04           ATUIN         1876 04           ATUIN         1807-01           ATUN         0160-421           ATUN         0160-421           ATUN         0160-421           ATUN         0160-01           ATUN         0160-01           ATUN         0160-01	71 61 68 71	2 8	,	IC OP AMP LOW OBJET FO DD PKG	24366 L	AD 184 180
A7\//// 1407-01 A8 82882-4 A8C1 0180-401 A8C2 0180-401 A8C2 0180-401 A8C2 0180-401 A8C3 0180-40 A8C4 0180-40 A8C4 0180-40 A8C4 0180-40 A8C4 0180-01 A8C8 0180-01	1	- I	-	- "C OR AMP LOW NOISE TO BD PAG - IC MULTIFLIEN ANLS TO BOO PAG - IC OP AMP LOW DRIFE TO BD PAG	7848J 78480 78480 78480 78480	AD764380 1826-0473 1826-0473 1826-0261 1826-0268 1826-0473
All         B3BB2-4           ABC1         G150-40           ABC2         G150-40           AFC3         G150-40           AFC3         G150-40           AFC3         G150-40           AFC3         G150-40           AFC3         G150-40           AFC4         G150-35           AFC5         O160-43           AFC7         O160 01           AFC7         O160 01           AFC7         O160 01           AFC8         O160-01		7		IC OP ANP LOW DRIFT TO BD PKG	78480	1876 0471
ABC1 0160 400 ABC2 0160 401 AFC3 0160 401 AFC3 0160 05 ABC6 0160 40 ABC6 0160 40 ABC7 0160 05 AFC7 0160 01 AFC7 0160 01 AFC7 0160 01 AFC7 0160 01 AFC8 0160 78		1	,	DRDL-2545825556300-1620-15910++0823	20480	1902-0197
ABC2         (160-43)           AFC3         (180-43)           AFC4         (180-38)           ABC4         (180-38)           ABC5         (180-38)           ABC6         (180-43)           ABC6         (180-43)           ABC7         (180-38)	0003	1		BOARD ASSEMBLY YO DRIVEN (DOES NOT INCLUDE B-FNI HEADLE PE OILF ACTURY- Ellect Resistors rate through R399 AND HER* Through RE01]	28480	83882-80002
ABCY 018001 ABCN 018001 ABCN 018001	89 61 79	8 0 4 7 6	ĩ	CAPACITOR FXD TUF 120% 60VD/ CFR CAPACITOR FXD TUDI'F 16PF 200VD	28480 61043 38480 38480 61842	0160 4084 200 200 NPO 1013 0160 0183 0160 2878 700 700 NPO 1013
	10 10 10			CAPACITUR FAD 0470F 130% BOVDC CER CAPACITUR FAD 8 BUF 110% 36VDC TA CAPACITUR FAD 8 BUF 110% 36VDC TA CAPACITUR FAD 8 BUF 110% 36VDC TA CAPACITUR FAD 8 BUF 110% 36VDC TA	78467 E0789 E0789 78400 E0789	0160 0676 1600685×03687 1600685×03687 0180-7816 1600685×03587
AB-11         0180.07;           AEC12         0160.04;           AB-13         0360.40;           AB-14         0160.38;           AB-15         0360.38;	74 14 74	0 2 # 7 0		CAPACITOR FAID 2204 + 10% 18MOC TA CAPACITOR FAID 0220F ± 20% 100MOC CER CAPACITOR FAID 10F 20% 60MOC CER CAPACITOR FAID 100F 1 ± 8FF 200MOC CER CAPACITOR FAID 1000FF ± 20% 100MOC CER	883NB 384N0 38480 38480 38480 38480	160()7265001687 0160 0574 0160-4084 0160-3874 0160-3874 0160-3878
ABCIN 0180-30 ABCI7 0180-30 ABCI7 0180-30 ABCI8 0180-30 ABCI9 0160-38 0160-38 0160-38 0160-38 0160-38	36 54 74	3 4 8 0	:	CAPACITOR NAD 2007 F10N BOVIC TA CAPACITOR FAD 5007 F10N BOVIC TA CAPACITOR FAD 10F 120N BOVIC CIR CAPACITOR FAD 10000F1 220N 100VIC CIR CAPACITOR FAD 220F1 10N 23VDC TA	28480 55289 28480 28480 28480	0180-1070 1000008200082 0160-4084 0100-4084 0180-2731
ABC21 0180-218 ARCR1 1901-051	. [	0	· ·	CAPACITOR FED 2000F120% 20VDC TA	10030	бөј авьст
ABCH2 1001063		2		Dade BM Big Bengtiky Dide 5M Big Bengtiky Not Assigned	38480 38480	1901-0538 1901-0539
ABCN4 1001003 ABCP5 1001003		3		DRUDE-GEN FRF EROV ZOOMA (XC- Z DRUDE-GEN FRF EROV ZOOMA (XC- Z	28480 28480	1 (01-0013

# Table 6-3. Replaceable Paris

See introduction to this section for ordering information Plinificates factory selected value

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					rame ors, Replaceable Parts		
	Reference Designation	HP Part Numbor	C D	Qty	Description	Mfr Code	Mfr Part Number
	AUCIII ABCIII ABCIII	1801-0023 1801-0025 1801-0023	202		DHDH GIW PRP 1809 200MA DH F DHDH GIW PRP 1809 200MA DH F DHDH GIW PRP 1809 200MA DH F	20400 28460 28400	1001-0013 1001-0636 1001-0033
	(LBA	1200-0465		1	SUCKET-IC B CONT DIP BLDB	28480	1200.0466
	AUNT	0490-0016	1 10		RELAY REED TA BOOMA TOOVIDC BVDC OD L	2848D	0400-0016
	A811 A817 A813	8140-0337 8140-0137 08503-80001	1 1 1		INDUCTOR RECHARD TAILON, DDD 4603 0+60 INDUCTOR NECHARD TAILON, DDD 4603 0+60 COLETORDI-1	28480 26480 28480	8140-0137 0140-0137 08603-80001
	Авмрі Авмрі Авмрі Діярі	6040 6846 6000 8043 1300 0173 1300 0173	0 9 0 0	1	Р.С. ВОАРД ЕХТРАСТОВ РУК Р.С. ИСАРД СХТРАСТОВ И КОЛОН-КSTR ОДР 01 И КОЦАТОВ УБТВ ОДР 01	2月4日() 2日4日() 2日4日() 2日4日() 2日4日()	6040 6846 6000 8043 1700 0173 1200 0173
ĺ	ABP2	1261-2203	1	1	HEADLR B PIN	18480	1261-1203
	ABI31 ABI32 ABI32 ABI34	1863-0281 1863-0281 1863-0044 1863-0044	11 11 7 7	7	ТКАКБІБТОВ FNP 2020076 5: ТО-ТВ РО-400МW ТКАКБІБТОВ FNP 2020176 5: ТО-ТВ РО-400МW ТКАКБІБТОВ FNP 5: ТО-ТЯ 2010077 ТКАКБІБТОВ FNP 5: ТО-21 РО-ТW FT-2001017	04713 04713 28480 28480	9N JUO JA 9N JUO JA 1863 0044 1863 0044
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	АЛНО Алн7 Алн7 Алн9 Алн9 Алн9	0608-0083 0608-0083 0357-0442 0357-0442 2100-0670	N 11 11 11 11 11		REGISTOR FOR THE TOWN TOWN TOWN REGISTOR FOR THE TOWN TO STOLENOU TO THE REGISTOR FOR THE TOWN TO STOLENOU TO THE	34046 34640 34640 34646 33087	C4-178-TD-1981-F C4-178-TD-1981-F C4-178-TD-1902-F C4-178-TD-1902-F C4-178-TD-1902-F 31872-1-103
	ABN11 ABN17 ABN13 ABN14 ABN16	0698-3188 2100-3782 0767-0480 0787-0442 0698-3482	1	1	R\$66510H 4.04H 1%, '6WF TC=03100 R166510H 7HMR 600H 10% C 600E A0317-TRN R166510H 68 0K 1%, 126WF TC=03100 R166510H 168 1%, 126WF TC=03100 R166510H 147K 1%, 126WF TC=03100	74646 78480 74646 74646 74646	CA-120-30-4043-3 2300-3763 CA-120-0102-7 CA-120-103-102-7 CA-120-103-100-7 CA-120-10-10-7 CA-120-10-7 CA-120-10-7 CA-120-10-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-120-7 CA-
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	АБЙ?   Абй? 2 Алй? 3 Алй? 4 Абй? 6	0600 0406 2100 0646 0609 0700 2100 2768 0609 0708	14074	1	ПЕБІБТОН В БАК І№, 3W7 TC+0+4 РЕБІБТОР-ТАЛЯ 1К 10% С БІЛІ-АДІ 37-ТАН ПЕБІБТОВ 21 ІК І№ 7 TC+0+4 ПЕБІБТОВ-ТАЛИ 20010№ С БІРГ-АДІ 47-ТАН РЕБІБТОВІ 11.478К І№ 1W7 TC+0+4	58480 37997 78480 78480 78480 78480	0688 6408 3297×-1-107 0608 0788 3100-3788 0699 0768
	A8A26 A8A27 A8A28 A8A28 A8A28 A8A28 A8A20	0767-0470 0648 8480 0767-0447 0767-0447 0767-0447 0767-0470	3 4 9 9 3		RESISTOR 1828 13, 126WF 10-02100 RESISTOR 181 13, 134F 10-02100 RESISTOR 101 13, 126WF 10-02100 RESISTOR 10131, 256WF 10-02100 RESISTOR 16213, 13, 126WF 10-02100	74848 78480 74648 74648 74648 74648	C4-1-18-30-1823-7 0898 8480 C4-1-8-10-100327 C4-128-10-100327 C4-128-10-1823-7
	Авқзі Авқзі Алнээ Аялза Авлзі? Авлзі?	0767-0442 0767-0274 0698-3463	0 6 2		RESISTING TON THE 12500 FTC-01100 RESISTOR 121N THE 12500 FTC-01100 RESISTOR 121N THE 12600 FTC-01100 PACTOR STICTCED NOT REPLACEABLE FACTORY 51 (CTED NOT REPLACEABLE	34648 34648 74648 74648	C4-178-TD-1002-F C4-178-TD-1211-F C4-178-TD-1882-F C4-178-TD-1882-F
	Абрја) Абрја) Абра) Абра ( Абра (	0608-8489 0698-8489 0698-84,2	4	1	FACTORY 6FTECTED NOT REPLACEABLE FACTORY 6FTECTED NOT REPLACEABLE REGISTOR 16N 1% 1WF TC=0+4 REGISTOR 864N 1% 1WF TC=0+4 REGISTOR 2.663N 1% 1WF TC=016	78480 78480 78480 78480	0646 8489 0686 5405 0686 8472
	ляр43 Авр44 Авр46 Авр46 Авр46 Авр47	0698-6409 7100-2161 0699-0518 0757-0416 0757-0416	4 6 7 7	1	РСБ1510Л 19 68№ 1% 1971 1С=0+4 НЕБ1510Л-ТРАИЛ 20К 10% С ВІДЕ-АДЈ 17-ТРИ НЕБ1510Л 11 480К 1% 1971 ТС=0+4 РГБ1510Л 611 1% 12697 1С=0+100 РЕБ1510Л 611 1% 12697 1С=0+100	78480 07111 78480 74648 74648	0008-8409 439203 0009-0518 C4-1/4-T0-65110-7 C4-5/8-T0-65110-7
	АВЛАВ Авла Авла Авла Авла Авла Авла	0767-0418 0767-0438 0767-0438 0767-0438 0767-0438 0767-0438	7 3 3 3 7 7	1	NE6510N 611 1% 126977 10-01100 NE6610R 6 118 1% 726977 10-01100 NE6610R 6 118 1% 726977 10-01100 NE6610R 6 118 1% 726977 10-01100 NE66510R 6 18 1% 726977 10-01100	74640 74646 74646 74646 74648 78480	C4-1/8-10-61417 C4-1/8-10-61417 C4-1/8-10-61417 C4-1/8-10-61417 Q167-Q180
ł	A8663	0698-3169			RESISTON 28 UK 13, 126W F 10+0+100	24546	64.1.4.10.2612.8

## Table 6-3. Replaceable Parts

See introduction to this section for ordering information *Indicates factory selected value

 $\begin{array}{l} \text{RE51510R 76 IN 1X 126WF 1C=0 (100)} \\ \text{RE510R 514F IX 126WF 1C=0 (100)} \\ \text{RE510R 514F IX 126WF 1C=0 (100)} \\ \text{RE510R 1MMR 50N 10X C 510L AD 1-1RM} \\ \text{RE510R 510R 100N 1X 126WF 1C=0 (100)} \\ \text{RE51510R 100N 1X 126WF 1C=0 (100)} \\ \end{array}$ 

ALBISTOF 316×11×12639 TC+02100 ALBISTOR 104 11×12639 TC+02100 ALBISTOR 104 11×12639 TC-02100 ALBISTOR 2164 11×12639 TC-02100 ALBISTOR 2111 11×12639 TC-02100

CA-1+0-10-2612-F 0698-8968 [160860] C4-1+8-10-6111-F C4-1+8-10-1003-F

0698-3467 C4-128 T0-1002-4 C4-128 T0-2361-4 C4-128 T0-2361-4 C4-128 T0-2361-4 C4-128 T0-2632 #

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0698-3467 0767-0442 0698-0084 0698-0084 0698-3466

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Reference Designation	HP Part Number	C D	Ωιγ	Description	Mfr Gode	Mfr Part Number
A82163 A82164 A82166 A82166 A82167	0698-3167 0767-0780 0698-3166 0767-0447 0767-0790	8 17 10 0	1	FEBISTON 34FK IX 126W/FEC-0+100 FEBISTON 34FK IX 126W/FEC-0+100 FEBISTON 147K IX 126W/FEC-0+100 FEBISTON 0K IX 126W/FEC-0+100 FEBISTON 840K IX 126W/FEC-0+100	74640 74640 74640 74640 10301	C4-178-10 3483-7 C4-178-10 10017 C4-178-10 10017 C4-178-10 1477-7 C4-178-10 10027 MF4C378-113-81817
АВН66* Авнов*				PACTORY 61 LECTED, NOT NEPLACE, BLE PACTORY 61 LECTED, NOT NEPLACE, ALL		
A867	3101-0471 3101-0471	ň		SWITCH HAN GIP AAN AESY 10 3A ODA JOVIX SWITCH HAN GIP AAN AESY 10 3A CDA JOVIX	28460 28400	3101 (347) 3101 (347)
AB1P1 Ab1P2 Ab1P3 Ab1P3 Ab1P4 Ab1P6	1261-6026 1261-6026 1261-6026 1261-6026 1261-6026 1261-6026	22222	17	CONNECTOR 17-PM M P051 15P1 CONNECTOR 17-PM M P051 15P1 CONNECTOR 17-PM M P051 15P1 CONNECTOR 17-PM M P051 15P1 CONNECTOR 17-PM M P051 15P1	78400 78400 78400 78400 78400	1761-6036 1761-6036 1761-6036 1861-6036
ABTP6 ABTP7 ABTP8 ABTP0 ABTP10	1261-6026 1261-6026 1261-6026 1261-6026 1261-6026	37777		CONNECTOR 17-IN M POST INFO CONNECTOR 17-IN M POST INFO CONNECTOR 17-IN M POST INFO CONNECTOR 17-IN M INST INFO CONNECTOR 17-IN M INST INFO	38480 38480 38480 38480 38480 38480 38480	1361-6036 1361-6036 1361-6036 1361-66 11 1361-66
A81P11 A81P12	1761-6976 1761-6976	3		CONNECTOR 12-PM M POST TYPE CONNECTOR 12-PM M POST TYPE	JMAND JMAND	1761-6076 1761-6076
ABU1 ABU2 ABU2 ABU4 ABU6	1810 0277 1810 0277 1830 0277 1830 2074 1870-2074 1878 0471	3		NETWORK-RES TO SIP2 JK OHM K 0 NETWORK-RES TO SIP2 JK OHM K 0 IC DRVR TTE LES LINE DIVR OCCL IC RIVR TTE LES LINE DIVR OCCL IC UP AMP ECAY ORIFT TO 99 PFG	01121 01121 01205 01205 01205 28480	71()A777 71()A777 51()A777 51()A1574A14 51741574A14 51879 ()A71
ABUB ABUT ABUT ABUB BUBA ABUD	1875-0475 1870-1558 1870-1144 1875-0150 1876-0753	7 8 5 0 3		ic gynten anler hidip p pag ic ben the le bus guad ic hate the le bon duad p-inp ic hwer the Mono-Astra ic op and low bias himpo guad 14 did c	01785 01755 01785 01785 01785 04713	14801C# 5177415175AW 517741507M N1886P MC341048L
АЛИ) 1 АЛИ) 2 АЛИ) 3 АЛИ) 4 АЛИ) 4 АЛИ) 6	1826-0471 1826-0768 1820-1198 1820-0762 1826-0762 1826-0471	7 日 日 フ フ フ		IC OP ANP LOW OBJET TO 00 FAG IC MULTIPLICH ANLO TO TOO IP 0 IC FETLAS DO TYPE POGED GATHIG COM IC CONVERTAD OBJET TO 00 PAG	78480 79480 01795 74365 7840	1826 ()A33 1826 ()A35 Biy Jalbi Faiy A)7842815 1826 ()A35
АЦИ16 Аби17 Ави18 Ави19 Ави19	1820-1216 1826-0262 1826-0271 1826-0220 1826-0220	33747		IC DCDN TTL LS 3-TO B-LINE 3-INP IC CDNV 13-R D/A 16-DIP C PAG IC OP AMP LOW DRIFT TD 80 PAG F 6WTTCH ANLG DUAD 16-DIP C PAG F 0P AMP LOW DRIFT TD 08 PAG	01785 74355 78480 06865 78480	BN74L5138N AJ76478D 18700473 Byv0783 18763471
A8U21	1826 0421	,		IC OP AMP LOW DIVIT TO UP PKG	20400	1820-0421
алунт Алунј Алунј Алунј Алунј Алунј	1007-0107 1002-0876 1002-0876 1002-0876 1002-0876 1002-3070	1000	2 1	DIODL-7NH 87 6V 5% DO-16 PD-1V - (C++ 087% DIODL-7NH 16878 6 7V 5% DO-7 PC - 76W DIODL-7NH 16878 6 7V 5% NO-7 PC - 76W DIODL-7NH 16878 6 7V 5% DO-7 FD- 75'V DIODL-7NH 16778 6% DO-76 PD- 4W	78480 04713 04713 04713 04713 78480	1902-0197 18820 18820 18820 18820 1902-3070
AB	83838-80010	,		BUAND ABBEMBLY-TRANSISTOR HEAT SINK	<b>?8480</b>	#3835-8003D
AUC1 AUC7	0180/0201 0180-1735	3	ŗ	INCLUDES PC BOF" D.CI, AND C2 ONLY CAPACITOR FAD TUFE TON BOVDC TA CAPACITOR FAD 220F±10% BOVDC TA	66780 66780	16001052003647 16007244003642
AULI AULI AULI AULA	\$700 0041 \$700 0041 \$700 0043 \$700 0043 \$3575 70034	5 5 5	3 1	INSULATOR-ESTRALIJNINIJN INSULATOR-ESTRALUNINIJA INSULATOR-ESTRALUNINIJA INSULATOR-ESTRALUNINUM INACEINO I AD	78400 78400 78400 78400 78400	1 700 004 3 1 200 004 3 1 200 704 3 1 200 704 3 1 3 5 7 5 700 34
Agmpi Agmpi Agmpi Agmpi Agmpi Agmpi Agmpi	61676.70036 7160 0116 7160 0116 7160 0116 7260 0116 7360 0116 7360 0116		) Ď	HEAT SINK SCREW-IJACH 6-32, 31; -H & G PAN HD POZI SCREW-MACH 6-3; 31; -H & G PAN HD POZI SCREW-MACH 6-3; 31; -H & G PAN HD POZI	78480 00000 00000 00000 00000 00000 00000 0000	H3B36-20, "4 Order by Description Order by Description Order by Description Order hy Description Order hy Description Order hy Description
AU()) AU()7 AU()3	1854 0080 1854 0080 1820 0430	15 10 1	2	твальбытов нри ві 10-3 FD= 1000 F1 — МН2 Твальбтов нри ві 10-3 FD= 1000 F1= 30 H2 іс 300 V писти 10-3	28480 28480 107283	1854 (0280) 1854 (0280) 181300N
AID	83585-6006B	•		BOARD ABBEMBLY MOTHER	28480	#38#8-#008B
A10C1 A10C2 A10C2 A10C3 A10C4 A10C5	0160-3879 0160-3879 0160-3879 0160-3879 0160-3879	7777		CAPACITOR FAD OTUF F70% TOOVIC CER CAPACITOR FAD DTUF F70% TOOVIC CER	28480 28480 28480 28480 28480 28480	0160-31,70 0160-3870 0160-3870 0160-3870 0160-3870
A10C6 A10C7	0160-3678 0160-3878	;		CAPACITOR FAD OTHER FOR TOOVIC CER CAPACITOR FAD OTHER FOR TOOVIC CER	20480	0160-3879 1160-3879

## Table 6-3. Replaceable Parts

See introduction to this section for ordering information Plodicates factory selected value

Reference Designation	HP Part Numbar	0 D	Οιγ	Description	Mfr Godo	Mfr Part Numbør
A 133 A1032 A1032 A1034 A1034 A1036	1261-6878 1261-8867 1261-3188 1261-3188 1263-8667 1263-8667	376	- - -	CONTECTOR DO PAR M POST NYE CONTECTOR DO PAR M POST NYE CONTECTOR DO PAR M POST NYE DACETTECTA CONTECTOR STOR DACETTECTA CONTECTOR STOR DACETTECTA CONTECTOR STOR	2040) 2040) 2040) 2040) 2040) 2040) 2040)	1 pa 1 a bi p 1 pa 1 a bi p 1 pa 1 a bi bi 1 pa 2 a bi a bi 1 pa 2
nic-t <del>A</del>	1269.0267	י	,	123449 CT08 19 FMB M PC 59 0004	20480	186110868
атсырт Атолирэ Атолирэ Атолира Атолира Атолира	1701-1110 1701-1110 1701-1110 1701-1110 1701-1110 1701-1110		6	NA ABIZING KEN IN EDIE LUID NA ABIZING KEN IN EDIE LUID NA ABIZING KEN IN EDIE CODIS NA ABIZING KEN IN EDIE CODIS NA ABIZING KEN IN EDIE CODIS	74480 20480 20480 20480 20480 20480	
ATURI	0608 NW17	י	L I	ብታ አስይተርያዙ የተተለጉ የይቆለም የ በር ቀርን ታ የእንት	\$#48D	OPAN FRIS
A10)-A1 A10)-A2 A10)-A3 A10)-A4 A10)-A4 A10)-A5	1301-1386 1301-1386 1301-1386	0 0 0	4	hot Abbisht", hot Abbisht", confiction PC (Bot ## Confiction # Provid confiction PC (Bot ## Confiction # Provid confiction PC (Bot ## Confiction # Provid confiction PC (Bot ## Confiction # Provid	58480 58480 58480	1861-1386 1861-1386 1861 1386
A105A8 A105A7 A105A8 A105A8 A105A9	1261-1386 1261-1386 1261-1386 1261-1386	1 1 1 4	I	COMMECTOR IN CLOSE #2 CONT-ROW # ROWS COMMECTOR IN LOSE #2 CONT-ROW # ROWS COMMECTOR IN LOSE #2 CORT-ROW # ROWS COMMECTOR IN LOSE # CONT-ROW # ROWS	JH400 JH400 JH400 JH400 JH400	1361   1966 1961   1986 1961   286 1961   1977
A12 A12 A12A1	BUB8-7341 boxb x341	7	١	BWITCHED YIG TUNED MUSTIFUEN EKCHANDE COBB 7343 VIM RD ASSY SWITCHED YIM HEATEN P/D A17	88480 88480	6086-2343 bunn b345
A17A1C1 A17A1C7 A17A1C7	0100 2055 0100 2055 0100 0048	0	; 1	АЪЭ БОТ БЕРАВАТЕЧ ИГТАСТАВСТ ГАРАСЛЪЯ ГЪО ЛЪЦІ – ВО ДОХ. ТОХУОС СЕВ ГАРАСЛЪЯ ГЪО ЛЪЦІ – ВО ДОХ. ТОХУОС СЕВ САРАСЛЪЯ БО ДОЛІ – ГБ-ТОХ. БОУЮС АТ	24480 38480 68280	andronances neu tupp neu tupp
A) JAICHI A) JAICHI A) JAICI A) JAICI A) JAICI	1001 0033 1251-3172 1251-3172 1251-3172	2	п	From - 41 N FRP 13/09 2000A (00 2 Connector Sal Cost See 02-IN (85-52 ****) Connector Six Cost Set 02-IN (85-52 ****) Connector Six Cost Set 02-IN (85-52 In)	26480 26480 26480 26480 26480	1401-0023 1261-0177 1261-0177 1261-0177 1261-0177
414414 414414 114414	1261-2172 1200-0607	7   1		CONNECTOR SUL CONTENT OF IN BUC 67 MAD SOCKET IC TO CONT OUP BLOK	)84461) 28481)	1100 0501
A17A1MP1 A17A1MP2	1707-0011 126-0173	0	1	51641 6066 T23 87 T23 38 C6 P563LAT0R 86TR DAP 05	20481) 24400	1100 0111
A12A101	1863 0038	4	1	налывтан гар ы го за го-турт-тоорну	ş#48I)	fillpa coan
A17A101 A17A107 A17A107 A17A104 A17A104 A17A106	0167 0466 0767 0466 0767 0447 0698 3167 0698 3167	8 8 9 9 10		NEDENIA LOOM 13, EEDWEETC=01 100 NEDENIA LOOM 13, EEDWEETC=01 100 NEDENIA LOM 13, EEDWEETC=01 100 NEDENIA 46 M 13, EEDWEETC=01 100 NEDENIA 46 M 13, EEWEETC=00 100	24648 24648 24648 24648 24648 24648 01121	14-1-0-10-20-20-20-20-20-20-20-20-20-20-20-20-20
A12A120 A12A102	0757-0447 0698-3154	8		пельтия та да та тария то-оттий перьтия а рак та тария то-оттий	24646 24646	K4-1, H-TD-16, # F F4-1-7-113-4723-F
A1 3A1 1F1 A1 3A1 1F3 A1 3A1 1F3 A1 3A1 1F3 A1 3A1 1F4 A1 3A1 U1	1351-0800 1351-0800 1351-0800 1351-0800 1351-0800 1351-0381	0 0 0 0 0 0 0	11)	CONNECTOR BOL CONTINUE 14-MM RSC 87-50 CONNECTOR BOL CONTINUE 14-6M RSC 87-50 IC OF AMPL LONG NO 881-TO 881-740	20480 20480 20480 20480 20480 20480	1761-0600 1761-0600 1761-0600 1761-0600 1876-0761
ALZALURI	1002 01 /6	0	1	0800-758 47 6V 6N 00 15 PD+1W 10++ 081N	284813	1807 01 Jn
A13 A13E1 A13	8048-7338 6001-1660 6061-6660	5	1	ювсикатом в 0 - 7 0 юнв пъблатом в >снанов Бовя-7336 обславон	38480 38480 78480 78480	BORB-733B COUL-1660 CUBB A335
1401				RD AND Y USCILLATUR BIAS P. () AT 3 AND NUT BEPARATELY REPLACEABLE		
A13A1C1 A13A1C2	0180 0177	;		CAPACITOR FAD THE FOX FRVDC CIR CAPACITOR FAD THE FOX FRVDC CIR	28480 28480	01600177 01600177
ALJAICH	1801 0033 1261 0600	u		DIODE-OEN MEP EROY ZOOMA DO-F KOMNECTOR BOL CONT PN 1-14-MM 888-67-69	28480 28480	1001.0033 1261-0600
A13A143 A13A143 A13A14	1261 0600 1261 0600 1261 0600	000		CONNECTOR SOLCONT INFLICA MULABC SP SO CONNECTOR SOLCONT INFLICA MULABC SP SO CONNECTOR SOLCONT INFLICA MULAC SP SO	78480 78480 78480	17610800 17610800 17610800
A13A115 A13A115	1761 0600	0		CONNECTOR BOLCONT PN 114-PM BBC BF BO CONNECTOR BOLCONT PN 114-PM BBC BF BO CONNECTOR BOLCONT PN 114 MM BBC BF BO	JHANO JHANO JHANO	1261-0600
	1700 0607	0		SOCIETIC DE CONTONTE DE BLOR CONTICTOR DE SMENTE CO QUIM	JHARD JHARD	1200 0002
A13A1401	1261-3172		1	CONNECTOR DE GUNT BET OF IN BEC BE IND	78480 78480	1261-2112
				r introduction to this section for ordering information		

# Table 6-3. Replaceable Parts

Bee introduction to this section for ordering information Pindicalas factory aslected value

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Reference Designation	HP Part Number	0 0	Oty	Description	Mfr Gode	Mfr Part Numbar
AT AA AA AA AA AA AA AA AA AA AA AA AA AA AA	0161 0710 3100 1833	11		PACTORS BARECTED FOR REPLACEATER PACTORS BARECTED FOR REPLACEATER PERINDER STARE TO FOR REPLACEATER PERINDER STARE IN TRAVER CONCEADER BESIDER TRAVER IN TO C. BRIE ADE T. TRAV	64640 30983	(4-1, # 11) 21 #1-1    1230=1127
NI 3A1 VIII NI 3A1 VII2 NI 3A1 VII2	1007-0678 1807-0675 1807-0187		7	рини ули 6 то уло (ю) 16 мр-ти то- (хил рини ули 6 то уло (ю) 16 мр-ти то- (хил рини ули 6 то уло (ю) 16 мр-ти то- (хил рини ули иу бу (х) (х) 16 мр-ти то- (хил	\$1148() \$1148() \$1148() \$1148()	1907-0678 1907-0678 1907-0197
A) 4 A) 4	6088-7343 CORD 0347	:	١	POWEN AMPEITIEN EDUNADUE DOBR 1247 AMPEITIEB	88480 28480	80 <b>86-7342</b> 5480-6342
884A1			+	ND ANNY ANP DIAN FANT DE ATR AND NOT NEPARATELY DE DY ACEADLE		
NIAAICI NIAAICI NIAAICI NIAAICI NIAAICI	010003174 01001704 01001704 01001704 0100701 01010701 01010701	80077	4	CAPACITOR FOD A THE CRU JON TONIC CLIP CAPACITOR FOD A THE LOS BY IC TA CAPACITOR FOD A THE LOS BY IC TA CAPACITOR FOD THE LOS BY IC TA CAPACITOR FOT THE LOS BY IC TA CAPACITOR FOT THE LOS BY IC TA	78480) 50780 50780 50780 50780 50780	1)101)124 160()41024()300 160()41024()300 60()240524()304 160()100524()304 160()100524()304 160()100524()304 160()100524()304 160()100524()304 160()100524()304 160()100524()304 160()10054()304 160()10054()304 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()3054 160()10054()30554 160()10054()30554 160()10054()30554 160()10054()30554 160()10054()30554 160()10054()30554 160()10054()30554 160()10054()30554 160()10054()30554 160()10054()30554 160()10054()30554 160()10054()30554 160()10054()30554 160()10054()30554 160()10054()30554 160()10054()30554 160()10054()30554 160()10054()30554 160()10054()30554 160()10054()30554 160()100554 160()100554 160()100554 160()100554 160()100554 160()100554 160()100554 160()100554 160()100554 160()100554 160()100554 160()100554 160()100554 160()100554 160()100554 160()100554 160()100554 160()100554 160()100554 160()100554 160()100554 160()1005554 160()10055554 160()1005555555555555555555555555555555555
NIAA168 NIAA167 NIAA168	0180 1704 0180 1704 0180 0174	0 1 1 1		CAPACITOR FOD A FULL TON BYDE TA CAPACITOR FOD A FULL TON BYDE TA CAPACITOR FOD A FULL TON BYDE TA CAPACITOR FOD A FULL TO FON FRYDE CER	60789 60789 20480	1 (1)14 7 (1) (0) (1) (1) 1 (1)14 7 (1) (0) (1) (1) 1) (1)1 (1) (1)1 (1)1 (1)1 (1)
NI 4 A I E N NI 4 A I E A NI 4 A I E A NI 4 A I E A	1261-3172 1261-3172 1261-3172 1261-3172 1261-3172	;   ;   ;		Connecton box content of in Abc. 67 NND Connecton box content of in Abc. 67 NND	58481) 58481) 58481) 58481) 58481) 58481)	1 2 6 1 - 31 7 2 1 5 6 1 - 31 7 2 1 7 6 1 - 31 7 7 1 7 6 1 - 31 7 7 1 7 6 1 - 31 7 7
N) 4 A 1 } 6 N) 4 A 1 4 7 N 4 A 1 4 M N 4 A 1 1 H N 4 A 1 L HI	1201-3172 1201-3172 1201-3172 1201-3172 1201-3172			COMMECTOR BOL CONT BAT 03 IN BBC 87 MAD LONDECTOR DOL CONT BAT 03 IN BBC 67 MAD COMPLETOR DOL CONT BAT 03 IN BBC 67 MAD COMPLETOR DOL CONT BAT 03 IN BBC 87 MAD COMMECTOR DOL CONT BAT 03 IN BBC 87 MAD	28480 58480 28480 26480 26480 36480 38480	1361-3179 1961-3879 1961-3879 1961-3879 1961-3879 1961-3879
1441111 1441117	181.3117	;		кончестоя бы конт быт оз ін нас-ал ныр кончестоя босконт быт оз ін нас ал ныр	38441) 38481)	1701-31 <i>77</i> 1701-3177
14A3J1 14A3M23	1100.0601	0 6		ыжылтыс таканатана бараган Казактар акта арагы	20480 20480	1200 0607 1200 0113
1441005 1441005 1441005 1440055	0380 0377 0380 0377 0380 0377 0380 0377	0000	n	BPACEN INT ON UNF IN LG 167-01-0 BPACEN INT ON DAF-16 LG 167-01-10 FPACEN INT ON DAF-16 LG 167-01-10 FPACEN INT ON DAF-1641 167-05-10	00000 00000 00000 00000	orden by description orden by description orden by description orden by description orden by description
1 4 4 1 3 2 4 1 4 4 1 5 2 7 1 4 4 1 5 2 7 1 4 4 1 5 2 79 1 4 4 1 5 2 79	0380 0387 0380 0577 0380 0577 0380 0577 0380 0377	0000		8PACER HVT (NY 082 (5.50-552 (5.60) 8PACER HVT (15, 162-(5, 152 (5, 16) 8PACER HVT (15, 082 (5, 152 (5, 152 (5, 16) 8PACER BVT (15, 082 (5, 16) (15) (15) (15)	00000 00000 00000 00000	onden by Dependent Onden  Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Ondent Onden
14A103	1004-0427 1003-0213	;		транвівтор при зврада бі то ти ро-солым Чанвівтор рыр знара бі то в ро-ту	84.11 61111	JNJJJJA JNAJ36
144171 144172 144172 144174 144176	6508-3443 6767-0490 9698-3441 9698-3441 9698-3441 9767-9789	0 3 # 8 3	1 1	A SYSTEM FIFT I STATE I FOW FICTOFIC PESISTEM FISTING IN TERM FICTOFIC PESISTEFIC IN TRAVETIC PESISTEM IN THE TRAVETIC PERISTOP IN THE TRAVETIC-OFICE PERISTOP IN THE TRAVETIC-OFICE	34540 34540 34540 34540 34540 34540	C4 1 / P-103 20 20 20 C4-1 / 20-103 20 1 2 C4-1 / 20-103 21 0 C4-1 / 20-103 21 0 C4-1 / 20-103 1001 -}
144170 144197 144197 144198 1441970 1441910	01637-03198 03637-0343-7 03637-0343-7 03637-0340-0 01886-23443	7 10 10 10	}	PE6181034 100 1 % AVEFC=02100 PE6181034 602 1 % 126VyF 1C=02100 PE6181034 802 1 % 126VyF 1C=02100 PE618104 803 1 % 126VyF1C=02100 PE618104 816 1 % 126VyF1C=02100	58480 34646 34646 34646 34646 34646	07670108 C4-1/8-1068781 C4-1/8-1090897 C4-1/8-10900897 C4-1/8-1091687
1441011 1441012 1441015 1441014				FACTURY ADJUSTED FOR PERCEASEANEE FOT ASSIGNTD FACTORY ADJUSTED FOT PERCEASE FACTURY ADJUSTED FOT NEFACEASE FACTURY ADJUSTED FOT NEFACEASEE		
14A11118 14A11137 14A11138 14A11138 14A11130	1)16113447	9		FACTORY ADJUSTED INOT RELACEABLE NOT ABSUGNED FACTORY ADJUSTED. NOT REPLACEABLE REDISTOR FOR TN: TEPNYETCHOLTOO NOT ABSUGNED	54640	C4-128-T0-1002-8
14A)X21 14A)X22 14A)X23 14A)X24 14A)X24 14A)X24	07670447 07670447 07670447 07670441 07670441	5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5		$\begin{array}{llllllllllllllllllllllllllllllllllll$	74040 74040 74040 74040 74040	L4 178-10-1007 F F4-178-10-1007 F F4-178-10-1007-F F4-178-10-1007-F F4-178-10-1007-F
1421428 1421427 1421428 1424428	0761	10 11 2		REB5100 106 1% 178007 10-03 100 RE55100 882 1% 178007 10-03 100 RE55100 121 1% 128007 10-03 100 RE5510610	34640 34640 34640	C4+878-113-1002-7 C4+978-113-662113 C4+178-113-622113
14A1N50 14A1N51	0498-0084 0498-0084	8		NEDISTOR 2 184 PS 12602 1000 REDISTOR 2 184 PS 12602 100	74648 74648	64-128-10-21812 64-128-10-21812

## Table 6-3. Replaceable Parts

Bee introduction to this section for orbiting information *Indicates factory selected value

Reference Designation	HP Part Number	0 D	Ωιγ	Description	Mfr Gode	Mfr Part Numbor
A14A1V3 A14A1V32	1907-0551		7	08001-2768-0-199-05-00-16-90-199-10-1-0223 02001-2768-12-19-05-05-16-09-199-10-1-0643	20400 20400	1007-0661 1902-0078
Alb				NOTABBIGNED		
Ale	60#8-718#	•	1	MODULATOR/COUPLEN	28480	8086-7167
ALEAL	N3600 80012	3	L I	враяр авбемвеч моруссирти	28480	83680 60013
AIDAICHI AIDAIJI AIDAIJI AIDAIJI AIDAIJI AIDAINPI AIDAINPI AIDAINPI AIDAINPI	1001-0639 1760 0645 1761 0645 1761-7313 0380 0843 0380 0843 0380 0843 0380 0843	78850000	4	DIO'TI 5M BIG GCHIDTNY CONNECTOR HE SM 5NP M PC 50 DHM CONNECTOR 5N 5NP M PC 50 DHM CONNECTOR 5GL CONT 5NF DA-IN 85G 57 FND STANDOFF-RIVET OF 175 IN 5G 4-40 THD STANDOFF-RIVET OF 175 IN 5G 4-40 THD STANDOFF-RIVET OF 175 IN 5G 4-40 THD STANDOFF-RIVET OF 175 IN 5G 4-40 THD	78480 78480 78480 78480 78480 78480 78480 78480 78480	1901 0539 1250 0543 1260 0543 1261 2353 0380 0543 0380 0543 1380- 143 0380 0443
A17				NOT ARRIGHED		
A18				NOT AREIGNED		
ATI	0960 0016	0	,	MIRCELLANEOUR PARTR 1501AT01-2 0 7 0 GH2	28480	0960-0638
CBI	86280 60046	ь	,	LOHCD DETECTOR	28480	0000-0038 86790-60046
CN2 CN5	1901-0033	3		Diode-gen Frip 1807 Jogna dg-7 Diode gen Frip 1807 Jogna dg-7	78480 78480	1801 0033
DC1	0056 0148	,	1	DIFLETIONAL COUPLER 1 7 - 200 GHZ	78480	0955-0148
E   E 7	5040-0146 5040-0346	;	7	INSULATOR CONNECTOR INSULATOR CONNECTOR	78480 28480	6040 0346 6040 0346
41	86760 60008	2	3	CONNECTOR ASSEMBLY TYPE-5	78480	86780-60008
17 17 14 16	1320 0118 1320 0118 1320 0118	3	,	Connecton af BNC TEM BGL-ROLEFA BO-DRM Connecton Abelmbly Train Connecton af BNC FEM BGL-ROLEFA BO ORM Connecton af BNC FEM BGL-ROLEFA BO-ORM	28480 28480 28480 28489 28489	1260-0118 88780-60008 1260-0118 1260-0118
нрі НРЭ НРЭ НРЭ Нара	0370-3073 83828-00008 4040-1698 83890-00001	10 12 13 4		N108-374 JACK 26-IN-10 OVER IN: WN100W DISPLAY FRONT PANEL-DRIFS	28480 28480 28480 28480 28480	0170-3023 83636-0006 83696-0006 83680-00001
мра мра мру мру мру	6041-0786 6040-8873 6041-1976 6041-1974 6041-1976	6 7 4 7 3	B 7 1	NEY CAP LITE NEY CAP-JADE GRAY NEY CAP-BLOPK NEY CAP-POWER LEVEL NEY CAP-POWER LEVEL NEY CAP-POWER SWEEP	78480 78480 78480 78480 78480 76480	6041-0785 6040-0873 6041-1876 6041-1876 6041-1876
MP10 MP11 MP12 MP13 AdP14	0050-2022 0050-2087 0050-2089 0050-2088 83525-20028	8 0 7 1 0		CASTING AL FRAME (INI) CASTING AL OCCULATON BRAF* "T CASTING AL INCAT SINK IF CASTING AL INCAT SINK SHIELD REAR	28480 28480 28480 28480 28480 28480 28480	0060-7037 0060-7087 0060-7088 0060-7088 83576-70038
12415 12416 12417 12417 12418 12418	1400-1096 113526-20037 113592-20018 113592-20018 113526-20029 10510-1148	6 0 5 1 2		FEIPFASTENEN 400 X. 300 X. 090 HI, BE SHIELD-FRONT GIDERAIL UFPER RIGHT CASTING FRONT RETAINER PUSH ON NU-TO-BHFT EXT	78480 78480 78480 78480 78480 78480	1400-1095 83525-20037 83592-20038 83525-20039 0510-1148
MP30 MP31 MP33 MP33 MP34	81697-20017 83682-00008 0060-2068 83682-00006	e 2 9 1		Sidenail Upperseet Sidenail Upperseet Casting al Heat Sink, R7 Bracket-Hoglandr Nut Assigned	28480 28480 28480 28480 28480	N3682-20017 N3692-2001 N3692-00008 N3693-00006
MF25 MF26 MF27	83636 00010 1460-1861	1) 10		GUARD WHELORM MUW BLK OXD	28480 28480	83575-00010 1460-1851
MP3	83626-10033	8	1	NOT ASSIGNED LATCH-SCREW	28480	83676-20033
MP10 MP10 MP11 MP15	83838-30040 83882-00-109 83882-00-109 83882-00-109 83882-10018 83882-10018	4 4 7 4 0		LATCH BRACAET-COUPLER S'DI RAIL-LOWER RIGHT SUBRAIL-LOWER RIGHT WITE HOLDER	78480 78480 78480 78480 78480 78480	83875-20040 83892-00009 83892-20018 83892-20018 83892-20018
NP34 NP36 NP37 NP37 NP38	83597-00003 6860-0002	8	•	NUT ASSIGNED PANLL-REAP NOT ASSIGNED NUT ASSIGNED PUTG HOLE DOME-HD FOR B-D HOLE STL	28480	83582 00003
MP39	6980-0003		;	PLUG-HOLE DOME-HD FOR 35-0 HOLE STL	28480 28480	6360-0003
MP40	83580-00007	0	· •	BRACKET-MODULATOR/COUPLER	26460	83980.000.1
#1 #2	D611-3673 D611-3673	9	,	MEDISTUR MATCHED BET WIREWOUND CHASSIS REDISTUR MATCHED BET WIREWOUND CHASSIS	28460 28460	0811-3773 0811-3673
					1	

# Table 6-3. Replaceable Parts

See introduction to this section for ordering information Pindicates factory selected value

Designation	HP Port Numbor	C D	Ωιγ	Description	Mír Gade	Mfr Part Numbor
W1 W2 W4 W5	63697-70046 #3697-70046 #3697-80076 #3697-80076 #3697-8001# #3697-8001#	1 1 1 1 1 1 1 1 1 1 1	1	CREAR COUPLER OUTINT CARLE COAR EXT WITH ALC CARLE ASSY RIBBON ROUT PANEL CARLE ASSY RIBBON RE SECTION CARLE COAR PULSE IN	78480 78480 78480 78480 78480 78480	83602-20046 03602-60021 83602-60026 83602-60018 83602-60018
W5 W1 W0 W10	83590 60013 83526 60039 93592 60013 3592 60015	4 3 6 8	9	CABLE COAN HED, PULSE MOD CABLE COAN GRAY DE DECOR CABLE COAN GRAY DE DECOR CABLE COAN BLUE EM NGT A55"SNED	28480 28480 28480 2840 2840	83600 6001 1 83636 60020 83693-6001 2 83693-6001 6
WE1 W12 W13 W14 W16	63697-60020 83697-60011 83697-60014 83690-60014 83690-60016 83697-20047	64.67.7	1	CABLE COAK OREEN ENLIN CABLE CUAK BROWN, AM IN CABLE CUAK BROWN, AM IN CABLE COAK BUILDON DE BECTRON CABLE DE DC2/VIA	78480 78480 78480 78480 78480 78480	83882-80070 8381 - 0011 83 14 8 00018 8 00018 8 00018
W18 W17 W18 W19 W70	83682 20039 83682 20038 83680 20022	2 1 1	1	CABLE-BEATIZYTM CABLE-BERSYN AMPIZATT NOT ASSIGNED NOT ASSIGNED CABLE-RE SEMERICID ATSZATA	78480 78480 78480	n3607+70030 H3607+70030 H3607+70037
W21 W22 W24 W24 W26 W26 W27 W27 W27	83590-70070 83590-70070 83575-60074	U D	8	NOT ASSIGNED NOT ASSIGNED NOT ASSIGNED NOT ASSIGNED CAFLE RF, SEAR RIGHT AT 7A16 CABLE IV, SEAR RIGHT AT 87/J3 AUX OUTPUT NOT ASSIGNED CABLE ASSEMDS / NOVER SUFPEY	28480 28480 28480	n 3690-20020 83690-20020 83625-80024
A10 A10 P1	6065-7371 87622-00010	0		CABLE ASSEMBLY HIBBON-REAR CONN CABLE ASSEMBLY HIBBON-REAR CONN OPTION DUT ATTENUATOR, PROGRAMMABLE, 70 DB (UPT 002 DNLY) BRACKET ATTENUATOR	28480 28480 28480	6086-7371 #3520-60056
WB W18 W20 W21	43642-60073 63642-20048 83642-20060 83642-20060 83642-20020	6 2 1 0		CABLE-CHAR DETACTOR GRAY (DELETE 6FD W8) CABLE-RIA DC2-YTAI (DELETE 6FD W16) CAILE-READD-REOUTPUT CAILE-READD-REOUTPUT CAILE-REOC7-A10	28480 28480 28480 28480 28480	83687-60073 83687-70078 83687-70078 83687-70078
NP1 N 7	6060 0126 6060 0107	9	8	OPTION 004 PLING HOLE 8260 HOLE (DELLTE MP38) PLUG HOLE FOR 760 HOLE (DELETE MP38)	28480 28480	6960 0105 6960 0107
W7 W8 W15 W27	93692-60024 83692-60023 83692-20048 83692-20062	0	*	CABLE-COAR EXT, MIN ALCIUPT OCHIDELETE 5TO W2) CABLE-COAR DETECTOR GRAY (DIELE 5TO W8) CABLE-TO DC2-YTALICLELE 5TO W16) CABLE-TO DC2-YTEAN PANEL NE (STIPUT	28480 28480 28480 28480 28480	83692-20024 83692-20048 83692-20048 83692-20062
ונ	63687-60077	,	٩	OPTION 008 CONNECTOR ASSEMBLY, APC-7 (DELETE STD J1) OPTION 002 AND CO4	284BU	N3602 f0027
A19 A19MP1 MP1 MP2	6086-7371 83587-0001-) 6080-0108 6980-0107	10 7 10 10	9	ATENUATOR, PROGRAMMABLE, 1000 BRACKEI-ATTENUATOR IS UG-HOKE AZED HOLE (DELETE MP38) PLUG-HOLE FOR DED HULE (DELETE MP39)	78480 78480 78480 78480 78480	6086-1311 6460-010 63592-00010 63592-00010
W2 W8 W15 W31 W33	83597-60074 83597-60073 83597-50048 83597-70048 83597-70051	0 8 0 8	1	CABLE COAN ENT/ MTR ALC (DELETE 610 W7) CABLE COAN DETECTOR (RAN (DELETE 610 W8) CABLE-10 OC 2/ MA (DELETE 610 W16) CABLE-RF 0C2/ A10 CABLE-RF A10, REAR PANEL RF OUTPUT	28480 28480 28480 28480 28480 28480	63697 60074 63697-6073 53697-2048 83697-2048 83697-2048
ALQ Algmpi Ji	5085-7371 83597-00010 83597-00077	0	8	OPTION 002 AND 005 ATTENUATOR, PROGRAMMABLE, 70 DB BRACKET ATTENUATOR CONNECTOR ASSEMBLY, ARC+7 (DELETE 5TD J1)	28480 28480 28480	6086-7373 838-2-00010 838-2-0007
WB W16 W20 W21	83692-00023 83692-20048 83692-20060 83692-20050 83692-20020	6 1 7 0	1 1 1	CABLE COAN DETECTOR GRAY (DELETE STO WB) CABLE-RF DC2: YTM (DELETE STO W18) CABLE-RF A10-RF DUTPUT CABLE-RF DC2: A10	7#480 , 80 76480 78480	8 750 2 500 2 3 5 350 2 - 2004 P 4 350 2 - 20050 8 350 2 - 20020
11 W7	#35#2-60027 #35#2-60024 #35#2-60023	2	1	OPTION 004 AND 008 CONNECTOR ASSEMBLY, AIC-7 (DELETE 5TD J)] CABLE COAK EXT/MTH ALC(OPT_D04)(DELETE 5TD W7) CABLE-COAK DETECTOR GRAY (DELETE 5TD W8)	28480 28480 28480	63692-60027 83692-60027 83692-60023

# Table 6-3. Replaceable Parts

 Infroduction to this section for ordering information *Indicates factory selected value

# **Replaceable Parts**

Reference Designation	HP Part Numbor	C D	Ωtγ	Description	Mfr Code	Mfr Part Number
W18 W37	83697-70048 83697-70067	2	1	CABLE-REDC2/VIN (DELETE STD W18) CABLE-REDC2/REAR PAREL REDUTEDT	28480 28480	#3682-2004# #3682-20062
	ľ			OPTION DOS AND DOS AND DOS		
614 1940 11	6086-7371 83887-00010 83887-60027	) ; ;	1 1	ATTENUATOR PROGRAMMABLE, 2000 BRACKET-ATTENUATON CONNECTOR ASSEMBLY, ARC 2 (DELETE 510 JT)	78480 78480 78480 78480	6066-7371 63692-00010 83692-60027
W1 W1 W31 W33 W33	63693-80024 83692-80023 83692-20046 83692-20039 83692-20051	0 8 0 8	9 5 1 1	CABLE COAN ENT/MIN ALC (L/LETE BID W7) CABLE COAN DETECTOR "MAY (DELETE BID W7) CABLE-RF (DC2/MIA (D* LETE BID W16) CABLE-RF (DC2/MIA) (D* LETE BID W16) CABLE-RF AND/REAR PANEL RF (DUTPUT	7848) 7848) 78480 78480 78480 78480	61587-60074 83592-80073 H3597-70046 85697-70079 83597-70051
	ĺ		i	ATTACHING HARDWARE		
				NOTE BER FIQURE 6-3-FOR ATTACHING HANDWARE LECATIONS		
k	0620 0128	8		5CREW-MACH 2-66 120-IN LG 100 DEG	00000	ONDER BY DESCRIPTION
2 4 6 8	0570-0177 0570-0165 0674-0781 7200-0101 2200-0101	0 3 3 0 7	67 78 10	SCREW MACH 2-86 188-IN LG PAN-IHD POZI SCREW-MACH 2-88 378-IN LG 82 DEG SCREW-HDS 4-20 B-IN-LG PAN-IHD-POZI SEL SCREW-MACH 4-40 188-IN LG PAN-IHD POZI SCREW MACH 4-40 28 IN LG PAN-IHD POZI	00060 00000 28480 00000 00000	orofa by description oroer by description ora of by description order by description order by description
7 89 10 11	2200 0105 2200 0107 2200 0113 2200 0113 2200 0164 2360 0115	4 6 4 6 4	0 0 2 2 2 3	ECREW-MACH 4-40 312-IN-LG PAN-IHD PO21 ECREW-MACH 4-40 378-IN-LG PAN-IHD PO21 ECREW-MACH 4-40 878-IN-LG PAN-IHD PO21 ECREW-MACH 4-40 188-IN-LG UNCE 82 DEG ECREW-MACH 6-32 312-IN-LG PAN-IHD PO21	01000 (*1000 00000 00000 00000	Orola by Discription Orola by Discription Orola by Discription Orola by Discription Orola by Discription
17 13 14 16	2360 0117 2360 0118 2260 0128 2360 0182 2360 0182 2360 0187	8 0 6 7	3 7 4 3 0	SCREW MACH 8-32 378-IN-LG PAN-HD PO21 ICREW MACH 8-32 438 IN LG PAN-HD PO21 ICREW MACH 8-32 1-IN LG PAN HD PO21 ICREW MACH 8-32 312-IN-LG P2 DEG ICREW MACH 8-32 312-IN-LG P2 DEG ICREW MACH 8-33 335-IN-LG P2N-HD PO21	00000 00000 00000 00000 00000	order by Description Order by Description Order by Description Order by Description Order by Description
17 18 10 20 21	2260-0333 2360-0334 2510-0051 2260-0309 2420-0309	8 6 3 5	16 8 7 6 5	6СЛЕW-МАСН В-32-28-IN-LG 100-JEL ВСЛЕW-МАСН В-32-312-IN-LG 8СПЕW-МАСН В-32-312-IN-LG 8СПЕW-МАСН В-32-625-IN-LG (AN-HD-PO2) NUT-HEX-W/LKWR 8-40-314D 1004-IN-ТНК NUT-HEX-W/LKWR 8-32-8HD 1009-IN-THK	77.480 1. 10 0., 30 00000 00000	7360-0333 7360-0334 Grulf by Description Order by Description Croff by Description
77 73 74 76 76	2850-0001 2850-0132 2850-0177 1250-1142 2180-0004	8 9 9 9	4   1   1   2	NUT-HER DBL-CHAM 3/8-32-THD 094-IN-THK NUT-HER-DBL-CHAM 7/16-28-THD 094-IN-THK NUT-HER-DBL-CHAM 1/4-36-THD 06-IN-THK WASHER-LK-INTL T 1/2 IN 26-TH ID WASHER-LK-INTL T 1/2 IN 26-TH ID WASHER-LK-INTL T NO 4-118-IN-ID	00000 00000 26480 28480 28480	080FR BY DI SCRIPTION ORDER BY DESCRIPTION 2850-0177 1750-1147 2180-0004
27 28 29 30 31	2100-0014 2190-0016 2100-0104 0360-0366 0260-1190	1 3 0 2 5	6 7 7 1 1	WASHER-LK INTL T NO 2 080-IN-ID WASHER-LK INTL T 328 IN 377-IN-ID WASHER-LK INTL T 328 IN 377-IN-ID TERMINAL-SLOR LUG PL-MTG FOR-85-SCR TERMINAL-SLOR LUG PL-MTG FOR-83/8-SCR	28480 28480 28480 28480 28480 28480	2100-0014 2100-0016 2100-0104 0360-036L 0360-1180
37	10160-1012	Ů	,	ILBMINAL-SLOB LUG LK-MTG FOR-#3/8-5CR	26460	0360-1832
			ļ			
			ĺ			

# Table 6-3. Replaceable Parts

See introduction to this section for ordering information *Indicates fectory selected value

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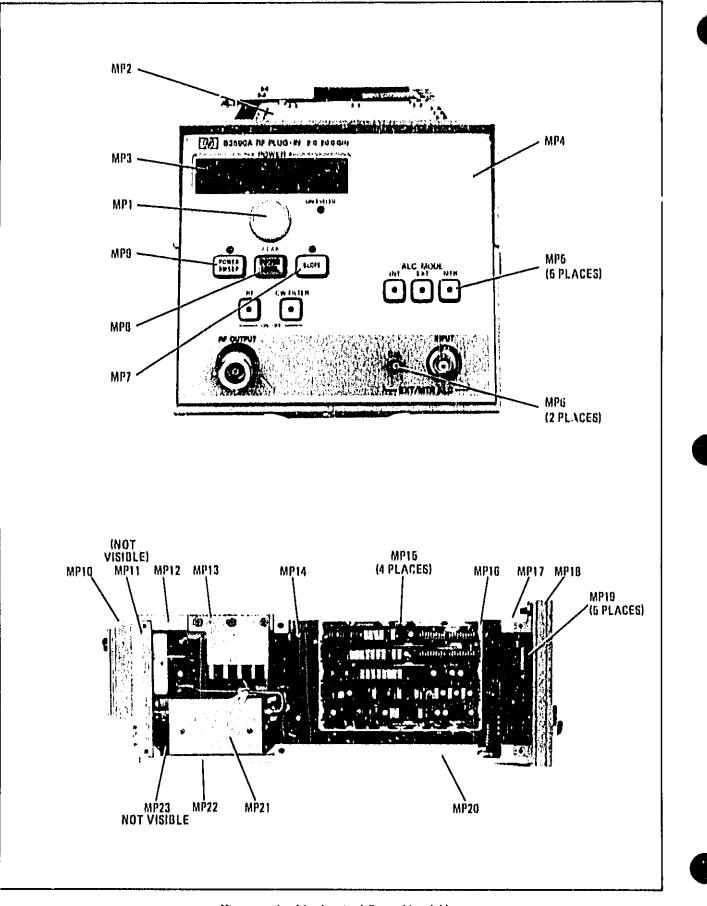


Figure 6-1. Mechanical Parts (1 of 3)

6-24

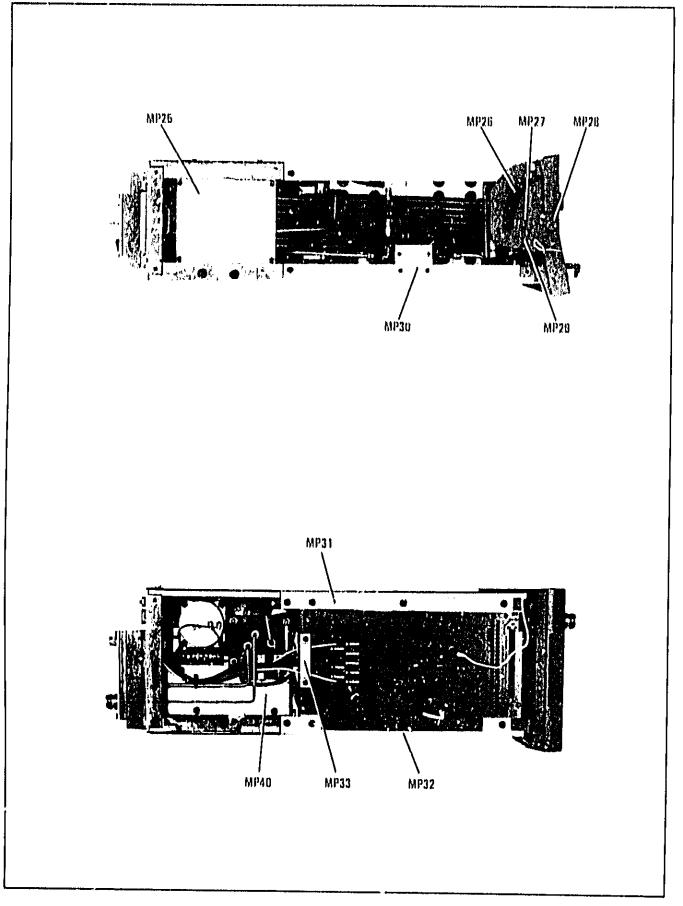
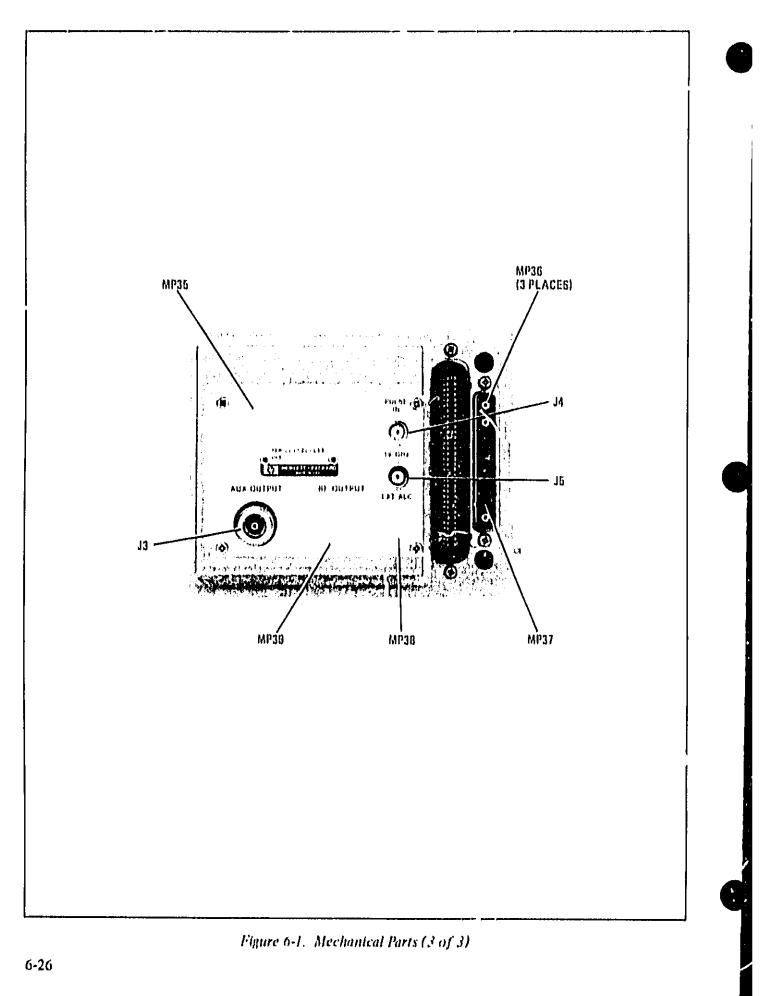


Figure 6-1. Mechanical Parts (2 of 3)

6-25

Model 83590A



**Replaceable Parts** 

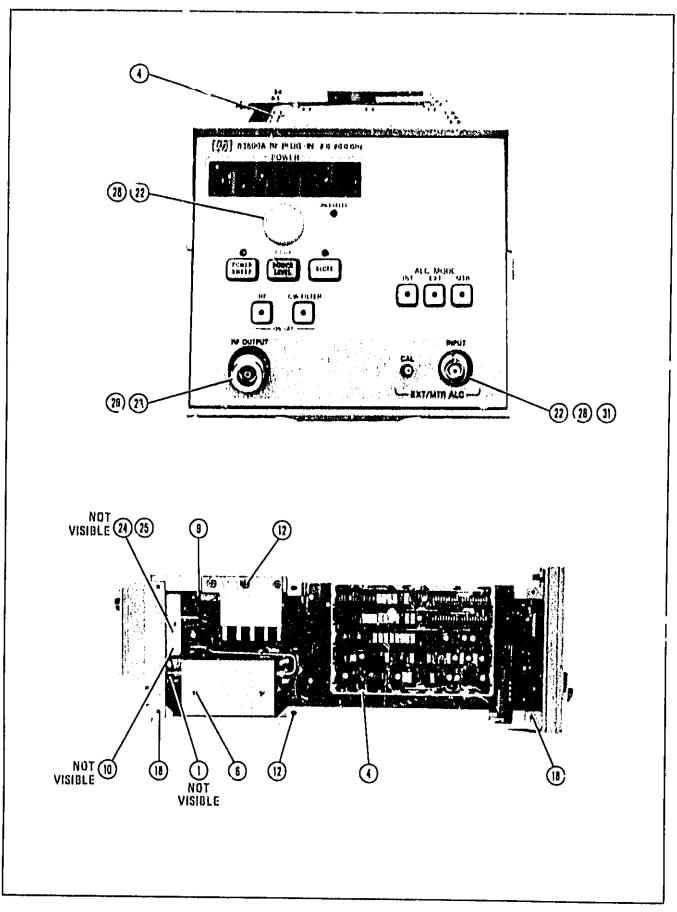
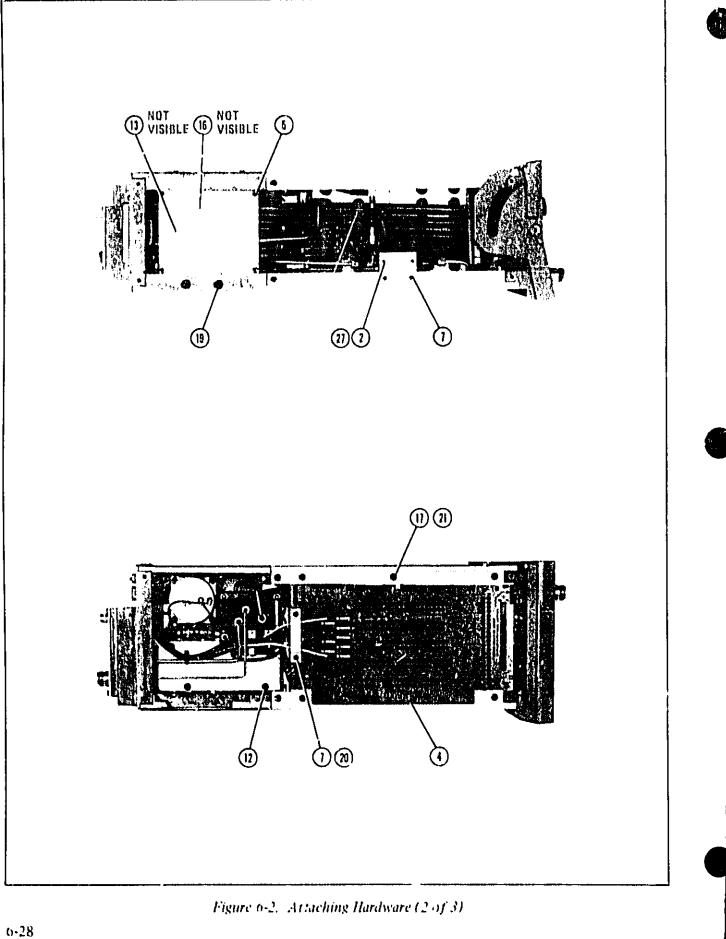


Figure 6-2. Attaching Hardware (1 of 3)

Model 83590A



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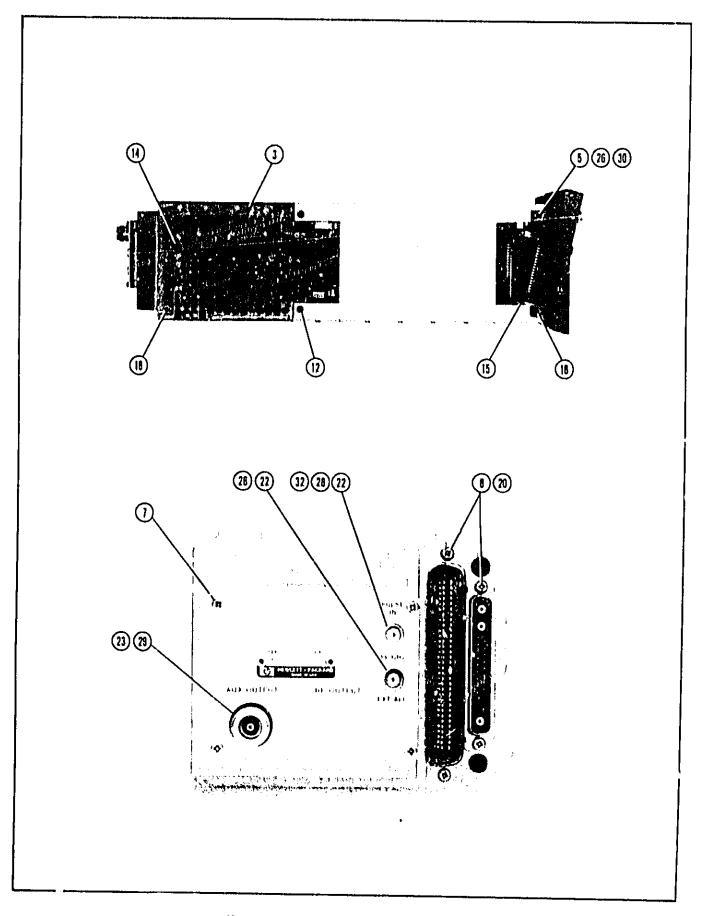


Figure 6-2. Attaching Hardware (3 of 3)

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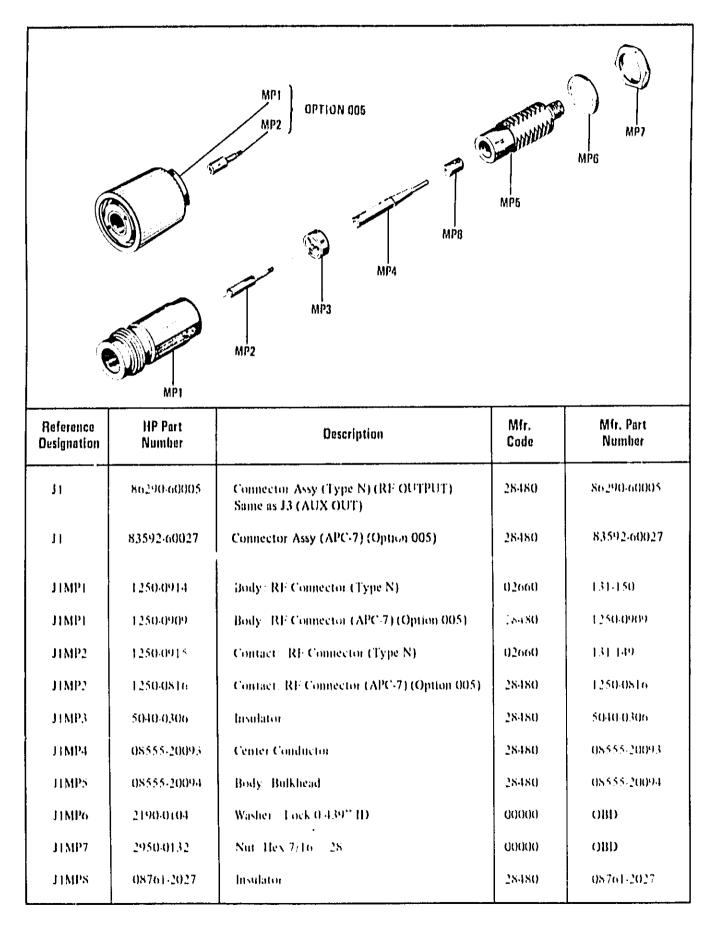


Figure 6-3. RF Output Connector, Exploded View

#### 7-1. INTRODUCTION

7-2. This manual has been written for and applies directly to instruments with serial numbers prefixed as indicated on the title page. Earlier versions of the instrument (serial numbers prefixed lower than the ones indicated on the title page) may be slightly different in design or appearance. The purpose of this section of the manual is to document these differences.

7-3. With the information provided in this section, this manual can be corrected so that it applies to any earlier version or configuration of the instrument. Later versions of the instrument (serial numbers prefixed higher than the ones indicated on the title page) are documented in a yellow Manual Changes supplement.

#### 7-6. MANUAL CHANGE INSTRUCTIONS

#### CHANGE A

Page 6-7, Table 6-3: Change A4 HP and Mfr. Part Number to 83590-60053, CD 2, Change A4CR4 to HP Part Number 1901-1098 CD 1, DIODE-SWITCHING 1N4150 50V 200MA 4NS, Mfr. Code 0004G, Mfr. Part Number 1N4150.

Page 6-8, Table 6-3: Change A4R49* to A4R49 (fixed value).

Page 8-47, Figure 8-34: A) from this Manual.

## **SECTION VII** MANUAL BACKDATING CHANGES

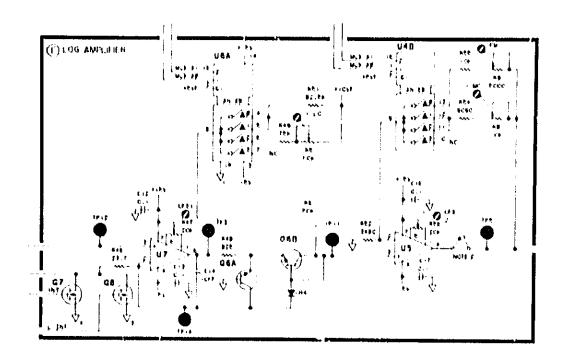
7-4. To adapt this manual to an earlier instrument, refer to Table 7-1 and make the manual backdating changes listed opposite your instrument serial number or serial number prefix.

7-5. For additional important information about serial number coverage, refer to INSTRUMENTS COVERED BY THE MANUAL in Section I.

Table 7-1.	Manual Backdating Changes by
	Serial Number Prefix

Sorial Profix	Make Manual Change
2143A	A

Change the A4 ALC Part Number in the top left-hand corner of the A4 schematic to 83590-60053. Change the SERIAL PREFIX in the bottom left-hand corner of the page to 2143A. Replace block E LOG AMPLIFIER with Figure 7-1, P/O A4 ALC Schematic Diagram (CHANGE





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1967 CE 1884666 (2016) DEG DEZ GRON 👘 🔹 1820 Kifer Houd, Gunnyvalu, California 94080, Teophime 4087/38 8658

TITLE: 035900 Manuel Changes Kincluding 027, 20, 0 32)

#### PART NUMBER: 03590-90005

MICROFICHE: 03590-90006

PRINT DATE: 2/82

**UPDATE: 2/89** 

PRINTED IN THE U.S.A.

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- 14 1 H The product related to this manual is no longer in production ŧŧ Ħ at the Hewlett-Packard Corporation. The manual is maintained ۴. ¥ on a microfiche master at Direct Marketing Division. As a H service to our customers we are providing a hordcopy print of Ħ the microfiche. The print is produced at Direct Marketing Ħ Division using a TAMERAN 1000-F Autoprint Microfiche Printing Ħ System. In addition, we are providing a duplicate of the H microfiche Lo providu maximum flexibility for our customers. H 1

# MANUAL CHANGES SUPPLEMENT

#### HP 83590A RF Plug-in

#### NOTE

MANUAL IDENTIFICATION

Manual Change Supplements are revised as often as necessary to keep manuals as current and accurate as possible. Hewlett-Packard recommends that you periodically order the latest edition of this supplement. Copies are available through any HP office. When ordering copies, quote the supplement part number from the bottom of this page, or the model number and print date from the title page of the manual.

Manual Parl Number: 83590-90005 Date Printed: February 1982

This supplement contains important information for correcting manual errors and for adapting the manual to instruments containing improvements made after the printing of the manual.

TO USE THIS SUPPLEMENT: Make all changes applicable to the serial prefix or number of your instrument as indicated in the following reference table.

Note that there may be more than one Title Page and/or Parts Cross-Reference Table included in this supplement. The last change(s) applicable to your instrument will contain the most current information for these specific pages.

NEW ITEM, CHANGED ITEM

HP Part Number 83590-91033 (For HP Internal Use Only) Part of HP Part Number 83590-90033 Microfiche Part Number 83590-90034



Printed in U.S.A.



#### 83590-90005

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# Model 83590A

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III - NEW ITEM

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1-6
1 - 7
1 - 8
1-9
1 - 10
2-11

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HP 83590A

Serial Prefix or Number	Make Manual Changes
2410A	2 - 7, 9 - 12
2411A	2, 3, 5, 9 - 14
2412A	2, 3, 5, 9, 11 - 15
2413A	2, 3, 5, 9, 11 - 16
2428A	2, 3, 5, 9, 11 - 17
2451A	2, 3, 5, 9, 11 - 18
2502A	2, 3, 5, 9, 11 - 19
2507A	2, 3, 5, 9, 11 - 20
2519A	2, 3, 5, 9, 11, 13 - 21
2543A	2, 3, 5, 9, 11, 13 - 22
2602A	2, 3, 5, 9, 13 - 23
2619A	2. 3. 5. 9. 13 - 74
2645A	2. 3. 5. 9. 13 - 25
2718A	2, 3, 5, 9, 13-16, 18-26
2726A	2, 3, 5, 9, 13-16, 18-27
2809A	2, 3, 5, 9, 13-16, 18-24, 26, 28

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#### ■ HNEW ITEM

Sorial Prefix Number	Change Number	Assemblies Affected	New Assembly Part Number	Manual Sections Affected
2216A	l	A2	83590-60060	Replaceable Parts Service
2217A	2	N/A ¹	N/A	Replaceable Parts
2221A	3	AI, AI6	N/A	Replaceable Parts
2233A	4	A4	N/A	Replaceable Parts
2234A	5	A16	5086-7395	Replaceable Parts
2249A	6	A4	N/A	Replaceable Parts Service
2252A	7	A4	N/A	Replaceable Parts Service
2306A	8	A6	N/A	Replaceable Parts Service
2313A	9	N/A	N/A	General Information
2315A	10	A3	83590-60073	Replaceable Parts Service
[,] 2338A	Ц	A2	83590-60072	Replaceable Parts Service
241.0A	12	A6	83590-60091	Replaceable Parts Service
2411A	13 and 14	N/A A4	N/A 83590-60077	General Information Operation Performance Tests Adjustments Replaceable Parts Service
2412A	15	A3	83525-60080	Replaceable Parts Service
2413A	16	A2 and A7	N/A 83595-60068	Replaceable Parts Service
2428A	17	A3	N/A	Replaceable Parts
2451A	18	A7	N/A	Rep aceable Paris Service
2502A	19	A10	83595-60078	Replaceable Parts Service

Numbered Changes Index (1 of 2)[,]

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Number	ed Changes	Index (2 of 2)	
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Sərial Prefix Number	Change Number	Assemblies Affected	New Assembly Part Number	Manual Sections Affected
2507A	20	A14	83592-60113	Replaceable Parts Service
2519A	21	A6	83590-60106	Replaceable Parts Service
2543A	22	Mechanical Parts	N/A	Replaceable Parts
2602A	23	A2	83590-60122	General Information Installation Operation Adjustments Replaceable Parts Service
2619A	24	A8	83595-60070	Adjustments Replaceable Parts Service
2645A	25	A4	83590-60098	Replaccable Parts / Service
2718A	26	A3	N/A	None
2726A	27	A4 .	N/A	Replaceable Parts
2809A	28	A4	83590-60135	Performance Tests Replaceable Parts Service

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#### MANUAL IDENTIFICATION

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HP Model Number: HP 83590A Manual Part Number: 83590-90005 Date Printed: February 1982

## UPDATES through CHANGE 27

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incorporate all UFDATES first, then make all changes appropriate for your instrument (see the preceding Serial Prefix reference table).



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11.5

HP Part Number 83590-90035 (For HP Internal Use Only) Part of HP Part Number 83590-90033

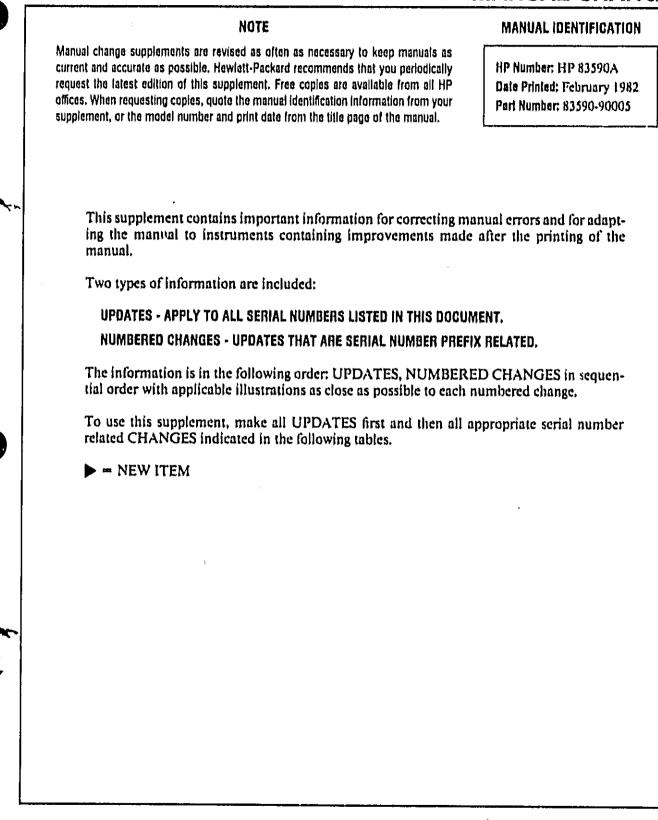
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Change Updates - 27

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# MANUAL CHANGES





NOVEMBER 12, 1987

Printed in U.S.A.

#### 83590-90005

## ► - NEW ITEM

Serial Prefix or Number	Make Manual Changes
2216A	1
2217A	1, 2
2221A	1-3
2233A	1-4
2234A	1 – 5
2249A	1-6
2252A	1 - 7
2306A	1 - 8
2313A	1-9
2315A	1 - 10
2338A	2 - 11

# HP 83590A

Serial Prefix or Number	Make Manual Changes
2410A	2 - 7, 9 - 12
2411A	2, 3, 5, 9 - 14
2412A	2, 3, 5, 9, 11 - 15
2413A	2, 3, 5, 9, 11 - 16
2428A	2, 3, 5, 9, 11 – 17
2451A	2, 3, 5, 9, 11 - 18
2502A	2, 3, 5, 9, 11 - 19
2507A	2, 3, 5, 9, 11 - 20
2519A	2, 3, 5, 9, 11, 13 - 21
2543A	2. 3, 5, 9, 11, 13 - 22
2602A	2, 3, 5, 9, 13 - 23
2619A	2, 3, 5, 9, 13 - 24
2645A	2, 3, 5, 9, 13 - 25

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Model 83590A

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# NEW ITEM

Number	Change Number	Assemblies Afrected	New Assembly Part Number	Manual Sections Affected
2216A	1	A2	83590-60060	Replaceable Parts Service
2217A	2	N/A	N/A	Replaceable Parts
2221A	3	A1, A16	N/A	Replaceable Parts
2233A	4	A4	N/A	Replaceable Parts
2234A	5	A16	5086-7395	Replaceable Parts
2249A	6	A4	N/A	Replaceable Parts Service
2252A	.7	A4	N/A	Replaceable Parts Service
2306A	8	A6	N/A	Replaceable Parts Service
2313A	9	N/A	N/A	General Information
2315A	10	A3	83590-60073	Replaceable Parts Service
2338A	11	A2	83590-60072	Replaceable Parts Service
2410A	12	A6	83590-60091	Replaceable Parts Service
2411A	13 and 14	N/A A4	N/A 83590-60077	General Information Operation Performance Tests Adjustments Replaceable Parts Service
2412A	15	A3	83525-60080	Replaceable Parts Service
2413A	16	A2 and A7	N/A 83595-60068	Replaceable Parts Service
2428A	17	A3	N/A	Replaceable Parts

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NEW ITEM

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# HP 83590A

# Numbered Changes Index

Serial Prefix Number	Change Number	Assemblies Affected	New Assembly Part Number	Manual Sections Affected	
2451A	18	A7	N/A	Replaceable Parts Service	
2502A	19	A10	83595-60078	Replaceable Parts Service	
2507A	20	A14	83592-60113	Replaceable Parts Service	
2519A	21	A6	83590-60106	Replaceable Paris Service	
2543A	22	Mechanical Parts	N/A	Replaceable Parts	
2602A	23	A2	83590-60122	General Information Installation Operation Adjustments Replaceable Parts Service	
2619A	24	A8	83595-60070	Adjustments Replaceable Parts Service	
2645A	25	A4	83590-60098	Replaceable Parts Service	

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# UPDATES

Inside Cover:

Replace the warranty statement with the following warranty statement.

#### CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members,

#### WARRANTY

This Hewlett-Packard instrument product is warranted against defects in material and workmanship for a period of one year from date of delivery, or, in the case of certain major components listed in section six of this Operating and Service manual, for the specified period. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.



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## LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED, HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

**EXCLUSIVE REMEDIES** 

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

#### ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.



UPDATES

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#### **UPDATES APPLY TO ALL SERIALS**

UPDATES

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# UPDATES

Title Page: Delete Option 005,

Page 1-1:

After paragraph 1-8 add the following:

	's Declaration
NOTE	NOTE
This is to certify that this product meets the radio frequency interference requirements of Directive FTZ 1046/1984. The German Bundespost has been notified that this equipment was put into circulation and has been granted the right to check the product type for compliance with these requirements. Note: If test and measurement equipment is oper- ated with unshielded cables and/or used for mea- surements on open set-ups, the user must insure that under these operating conditions, the radio fre- quency interference limits are met at the border of his premises. ModelHP 63590A	Hiermit wird bescheinigt, dass dieses Gerät/Systen in Übereinstimmung mit den Bestimmungen von Postverfügung 1046/84 funkentstört ist. Der Deutschen Bundespost wurde das Inverkehr bringen dieses Gerätes/Systems angezeigt und die Berechtigung zur Überprüfung der Serie auf Ein haltung der Bestimmungen eingeräumt. Zusatzinformation für Mess- und Testgeräte: Werden Mess- und Testgeräte mit ungeschirmter Kabeln und/oder in offenen Messaufbauten ver wendet, so ist vom Betreiber sicherzustellen, dass die Funk-Entstörbestimmungen unter Betriebs- bedingungen an seiner Grundstücksgrenze ein- gehalten werden.
Page 1-2, Table 1-1: Delete all references to Stability with Time (in a 10-mi) Page 1-5, Table 1-2: Add STABILITY WITH TIME (in a 10-minute period 2.0 to 7.0; < ± 100 kHz 7.0 to 13.5; < ± 200 kHz 13.5 to 20.0; < ± 300 kHz 2.0 to 20.0; < ± 300 kHz	nute period after one-hour warmup). after one hour warmup at the same frequency setting):
Page 1-6, Table 1-2:	
Page 1-6, Table 1-2; Change the PULSE IN characteristics as follows: Pulse in (2.0 to 20.0 GHz) TTL compatible: Logic high = RF on, Logic low-	=RF off error for 8755 compatibility up to 2 dB, typically 1 dB)

**UPDATES APPLY TO ALL SERIALS** 

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## 83590-90005

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HP 83590A

	Page 4-2, Section 4-13:	
	Change the specification for CW Mode (13.5 to 20.0) to $\pm 10$ MHz.	
	Page 4-10, Paragraph 4-15, SPECIFICATION: Delete all references to Stability with Time (in a 10-minute period after one hour warmup).	
	Page 4-12, Paragraph 4-15; Delete Frequency Change with Time (10 minutes), Delete steps 6 through 8, Delete Table 4-8,	
	Page 4-16, Table 4-11; Change Residual FM tolerances to: 5 kHz, 7 kHz, 9 kHz,	4
	Page 4-30, Table 4-16, Section 4-13: Change 13.5 to 20 GHz Accuracy to ± 10 MHz. Change lower and upper limits at 17,0 GHz to 16,99, 17,010. Change lower and upper limits at 14,0 GHz to 13,99, 14,010. Change lower and upper limits at 20,0 GHz to 19,99 20,010.	
1	Page 4-35, Table 4-16, Section 4-15: Delete all references to time (10 minutes) specifications.	
ļ	<ul> <li>³age 5-21, Paragraph 5-17;</li> <li>Add [INSTR PRESET] before [RECALL] in step 9.</li> <li>Add [INSTR PRESSET] before [RECALL] in step 14.</li> <li>After step 15, add the following:</li> <li>16. On the P3540A/B press [INSTR PRESET] [GW] [5] [0] [MHz]. While observing the frequency counter display, adjust the 83590A FREQ CAL control for 50 MHz.</li> </ul>	
F	Page 5-29, Paragraph 5-20; Replace Paragraph 5-20 on pages 5-29 through 5-32 with 5-20, SLOW SWEEP SYTM TO YO TRACKING (UPDATES) contained in this document.	
F	age 5-33, Paragraph 5-21: Replace Paragraph 5-23 on pages 5-33 through 5-37 with 5-21, SRD BIAS (UPDATES) contained in this document.	
P	age 5-51, Paragraph 5-28. Replace Paragraph 5-28 on pages 5-51 through 5-54 with 5-28. ALC GAIN ADJUSTMENT (UPDATES) contained in this document.	2 ° <b>4</b>
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# UPDATES APPLY TO ALL SERIALS

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UPDATES

#### HP 83590A - .

# UPDATES (Cont'd) Page 6-2, Paragraph 6-17;

Add the following after paragraph 6-17:

Two Year Warranty and Restored Exchange Parts

The microcircuit parts listed in Table 6.0 are provided with either a two-year warranty from the date of purchase and/or a restored exchange parts program,

A two-year warranty applies to both an original component and to one that is purchased as a replacement part either new or restored through the support life of the instrument. The restored exchange parts program allows a defective component to be exchanged for a factory-restored part which provides a substantial reduction in replacement cost. In addition, if the original component is covered by a two-year warranty, the exchanged component will also have a two-year warranty from the date of purchase. Table 6-0 below identifies the components within the instrument that have a two-year warranty as well as those that are available as restored exchange parts.

Reference Designation	Doscription	Two-Year Warranty	Restored Exchange Part
A12 :	Switched YTM	Yes	Yes
A13	YO 2.3 - 6.7 GHz	Yes	Yes
A14 (	2 - 7 GHz Power Amp	Yes	Yes
A16	Mod/Coupler	Yes	No

Table 6+0,	Two-Year	Warranty and	l Restored	Exchange Parts
------------	----------	--------------	------------	----------------

#### Page 6-2, Table 6-1:

Change A12 New Part Number to 83592-60065, Rebuilt Part Number to 83592-60066, Description to Switched YTM Kit.

Change A13 New Part Number to 83590-60066, Rebuilt Part Number to 83590-60067, Description to YO 2.0 to 7.0 GHz Kit.

Add A19, New Part Number 83592-60123, Rebuilt Part Number 83592-60124, Description 70dB ATTENUA *OR (OPT. 002).

#### Page 6-5, Table 6-3:

Change AIRPGI to HP and Mfr. Part Number 0960-0683, CD 3 (recommended replacement). Change A2JI to HP and Mfr. Part Number 125:-5926, CD 3 (recommended replacement).

#### Page 6-6, Table 6-3;

Change A2R1 to: 2100-3103, CD 5, RESISTOR-TRMR 10K 10% C SIDE-ADJ 17-TRN, 04568, 889PR10K.

Change A2U9 to HP and Mfr. Part Number 1826-1186, CD 8 (recommended replacement).

Change A3 to HP and Mfr. Part Number 83525-60980, CD 6, DIGITAL INTERFACE ASSEMBLY (does not include A3U1 and A3U2).

Change A3J1 to HP and Mfr. Part Number 1251-5926, CD 3 (recommended replacement).

Change A3UI and A JU2 to A3UI/A3U2 (not separately replaceable), HP and Mfr. Part Number 83590-60074, CD 7, EPROM Replacement Kit (recommended replacement).

Change A3U5 to HP and Mfr. Part Number 1820-3093, CD 8 (recommended replacement).

#### Page 6-7, Table 6-3:

Add A3XUI and A3XU2, HP and Mfr. Part Number 1200-054., CD I, SOCKET-IC 24-CONT DIP-SLDR (recommended addition).



#### **UPDATES APPLY TO ALL SERIALS**

× E : 83	590-90005 HP 83590	)A		HP	83590A
$E = E_{\rm e} = \frac{1}{2} \left( \frac{1}{2} + \frac{1}{2} \right) \left( 1$					
	UPDATES (Cont'd)				UPDATES (Cont'd)
	Page 6-9, Table 6-3: Change A4UI to HP and Mir, Part Number 1826-1058,	•		:	Page 8-69, Figure 8-17; In Block E DELAY CO
	Change A4U2 to HP and Mir. Part Number 1826-1186, CD 8 (recommended replacement). Change A4U9 to HP and Mir. Part Number 1826-1186, CD 8 (recommended replacement). Change A4VR4 to Part Number 1902-0111, CD 9, DIODE-ZNR 1N753A 6, 2V 5% DO-7 PD=, 4W (recommended				Page 8-73, Figure 8-73; Delete A13A1C2 fro
، ا	replacement).				Page 8-75, Figure 8-76; Delete A13A1C2 (re
	Page 6-14, Table 6-3: Change A6U10 to HP and Mfr. Part Number 1826-1186, CD 8 (recommended replacement). Change A6U11 to HP and Mfr. Part Number 1826-1186 (recommended replacement).			_	On the male connect short) and label [
	Page 6-16, Table 6-3; Change A7U19 to HP and Mfr. Part Number 1826-1349, CD 5 (recommended replacement).	.•			
	Page 6-19, Table 6-3: Change A12 to HP and Mfr. Part Number 83592-60065, CD 8, SWITCHED YIG TUNED MULTIPLIER KIT.	1 ¹		•	
3 ^{- 1}	Change A12 to HP and Mfr. Part Number 83592-60066, CD 9, EXCHANGE 83592-60065 SWITCHED YTM KIT.				
:	Change A13 to HP and Mfr. Part Number 83590-60066, CD 7, OSGILLATOR 2.U-7.0 GHz KIT. Change A13 to HP and Mfr. Part Number 83590-60067, CD 8, EXCHANGE 83590-60066 OSC. KIT, Delete A13AIC2 (recommended deletion).	1 : : :			
1	<ul> <li>Page 6-21, Table 6-3: Change A16 to HP and Mfr. Part Number 5086-7395, CD 7 (recommended replacement), Change J1 to HP and Mfr. Part Number 5061-5304, CD 2, CONNECTOR ASSY TYPE-N APC-7 DC BLOCK (recommended replacement),</li> <li>Change J3 to HP and Mfr. Part Number 5061-5386, CD 0 (recommended replacement).</li> <li>Delete MP6, KEY CAP-JADE GRAY, Add E3, HP and Mfr. Part Number0960-0055, CD 1, CONNECTOR AND WIRE: RF SHORT.</li> <li>Change MP3 to HP and Mfr. Part Number 83522-20028, CD 5,</li> </ul>				. ;
; ; ;	Prge 6-22. Table 6-3: Change W13 to HP Part Number 83592-c0014, CD 7. Under Option 002, Option 004, and Option 002 and 004, change both HP and Mfr. Number of W8 to 83592-60012. CD 5. Under OPT, 002 change the following item: A19 HB and Mfr. Part Number 83592 (0122, CD 9, EXCITATION to TERRITION TO PROPER to SUPPORT				
	Al9 HP and Mfr. Part Number 83592-60123, CD 9, EXCHANGE ATTENUATOR 70 dB (OPT. 002 ONLY). Under OPT. 004change the following items: MPI to HP and Mfr. Part Number 83592-20062, CD 1. W32 to HP and Mfr. Part Number 83590-20024, CD 3.	«پ	р 1 - 1 - 2 - 2 - 2 - 2 - 2 - 2 2 - 3 - 2 - 2	•	
,	Under GPT, 002 and 004 change the following litms: A19 to HP and Mir. Part Number 83592-60123, CD 9, MP2 to HP and Mir. Part Number 83592-20063, CD 2, W33 to HP and Mir. Part Number 83590-20025, CD 4. Since OPT, 005 is no longer available, delete all references to OPT, 005 and combinations with other options. Specifically, delete titles and parts references associated with APTION 005, OPTION 002 and 005, UPTION 004 and 005, and UPTION 002, 004, and 005.	¥		<b>₩</b>	,
	Page 5-24, Figurn 6-1: Delete MP 6.		en an		
	Page 8-31, Figure 8-18 (AI/A2 Schematic): Change A2RI to 10K.				
	Page 8-57, Figure 8-44; Change the designation of the resistor between U19 and U20 to R32.	a state	and the second		
6	UPDATES APPLY TO ALL SERIALS	;		UPD	ATES
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-17; Y COMPENSATION change the value of R17 to 287K.

1-73: 2 from the component locations diagram (recommended deletion),

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8-76; 2 (recommended deletion), mentor to the left of J2, draw a connecting line from the center conductor to the outer conductor (a bel E3,

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# UPDATES APPLY TO ALL SERIALS

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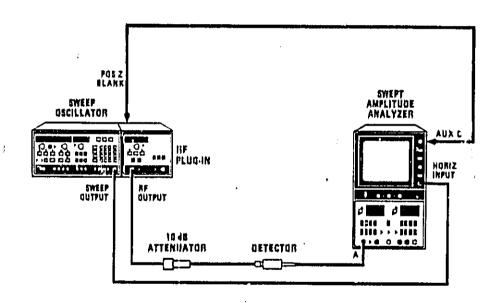
#### 5-20. SLOW SWEEP SYTM TO YO TRACKING (UPDATES)

**REFERENCE**:

Performance Test: Paragraph 4-13 Service Sheet: A6 and A7

#### DESCRIPTION;

To obtain optimum output power, the Switched Yittrium-Iron-Garnet tuned multiplier (SYTM) passband peaking should track the output of the Yittrium-Iron-Garnet Oscillator (YO). The 83590A is set to sweep Bands 2 and 3 (7 to 20 GHz), and the Automatic Leveling Control (ALC) loop is opened by selecting the External (EXT) ALC MODE. The Step Recovery Diode (SRD) Bias for the SYTM is preset and will be adjusted in Paragraph 5-21. Special calibration modes are used for this procedure (SHIFT 92 for OFFSET and SHIFT 93 for GAIN of the frequency sweep). The output power is peaked for each calibration mode, and the appropriate calibration constant is entered into the calibration switches, A7S1 stores the OFF-SET constant, and A7S2 stores the GAIN constant.





#### EQUIPMENT:

Swept Amplitude . Display Mainfram	Analyzer	* * * * * *	• • • • • • • • • • • • • • • • • • • •	HP 8755C
Detector				Weinschel Model M9-10
Sweep Oscillator	• • • • • • • • •	* * * * * * *	• • • • • • • • • • • • • • • • • • •	



#### UPDATES APPLY TO ALL SERIALS

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# 5-20. SLOW SWEEP SYTM TO YO TRACKING (UPDATES) (Cont'd) PROCEDURE:

#### NOT'E

This procedure requires that A3S1 is set to the factory-set position. Refer to Table 5-6.

#### NOTE

During this adjustment, a localized drop in power may occur. This drop in power is due to the SRD bleing over blased and is called squegging. If squegging occurs in Band 2, adjust A6R68 and R73 to eliminate the squegging and to maximize power across the band. If squegging occurs in Band 3, adjust A6R69 and R74.

- I. Connect the equipment as shown in Figure 5417. Allow the equipment to warm up for one hour.
- 2. On the 8350A/B, press [INSTR PRESET] [START] [7] [GHz] [SWEEP TIME] [2] [0] [0] [ms] [ LT MOD]. On the 83590A press [EXT ALC MODE]. The unleveled lamp light should be lit.
- 3. Preset A6R78 (T) one quarter turn from full clockwise position.
- 4. Select 5 dB/DIV display resolution on the 8755C and center the display,
- 5. On the 8350A/B, press [SHIFT] [9] [2] to enable the SYTM OFFSET DAC sub-routine. Using the 83590A POWER control, peak the power in the beginning of Band 2.
- 6. On the 8350A/B, press [SHIFT] [9] [3] to enable the SYTM GAIN DAC sub-routine. Using the 83590A POWER control, peak the power at the end of Band 3. Maximum peaking occurs when the power at the high end of Band 3 has been optimized without the power in other bands dropping out.
- 7. Iterate between steps 5 and 6. SHIFT 92/93 are interactive so the adjustments must be alternated until the best compromise is found.
- 8. Press [SHIFT] [9] [2]. Set A7SI to the Hex-code on the plug-in display. Press [SHIFT] [9] [3]. Set A7S2 to the Hex-code on the plug-in display.
- 9. Press [INSTR PRESET] on the 8350A/B so that the new calibration data will be entered from the current switch settings.
- 10. On the 8350A/B, press [STOP] [7] [GHz] [ UT MOD] [SWEEP TIME] [4] [0] [0] [ms]. On the 83590A, press [EXT ALC MODE].
- 11. Adjust A7R51 (BI OFS) to maximize the minimum power points of the Band 1 displayed trace.

#### 5-21. SRD BIAS (UPDATES)

#### **REFERENCE**;

Performance Test: Paragraphs 4-17, 4-19 Service Sheet A4 and A6

#### **DESCRIPTION:**

The High Power SRD Bius is set by peaking the 8755C displayed trace with A6R68 (2H) and A6R73 (2L) in Band 2, A6R69 (3H) and A6R74 (3L) in Band 3.

The Low and Mid Power SRD Bias is adjusted by inserting a voltage through a 511 ohm currentlimiting resistor to directly bias the Modulator/Splitter. With the 83590A at maximum RF output, the power supply voltage is increased (minimum voltage 0.5 Vdc, maximum voltage 5.0 Vdc) to set the RF output power just above the 8755C noise floor. Then A6R65 (3HL) is adjusted until minimum slope is obtained on the oscilloscope display. The voltage from the power supply is decreased until the lowest part of the trace, on the 8755C display, is 10 dB above the noise floor. Then A6R12 (C) is adjusted to peak the power in Bands 2 and 3. The power supply is then removed.

The 8750A is used to normalize system errors so an accurate measurement of the SYTM fundamental feedthrough can be made. A low pass filter is then inserted before the detected 8755C input. A comparison between the normalized and low pass inputs are made to determine the SYTM fundamental feedthrough.

#### EQUIPMENT:

Swept Amplitude Analyzer
Display Mainframe
Detectors (2)
6 dB Attenuator
10 dB Attenuator
20 dB Attenuator
Directional Coupler
Power Supply
Low Pass Filter (6.8 GHz) HP 11684A
Storage Normalizer ,
Uscilloscope
Extender Board
Sweep Oscillator
511 ohm Resistor

#### PROCEDURE:

JPDATES

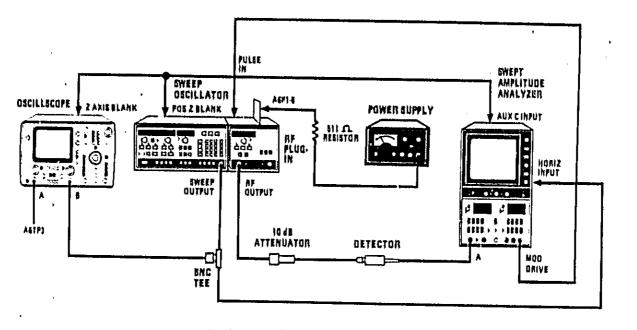
#### NOTE

Turn the 8350A/B LINE power OFF when removing or installing PC boards.

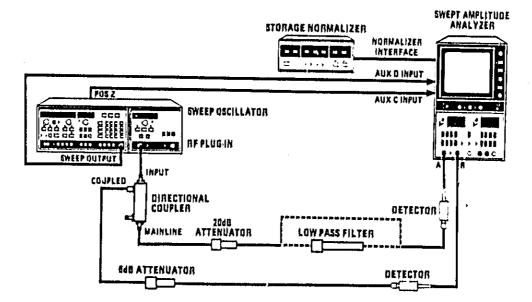
This procedure requires that A3S1 is set to the factory-set position (refer to Table 5-6).

#### **UPDATES APPLY TO ALL SERIALS**





a) Low and Mid Power Test Setup



b) YTM Fundamental Feedthrough Test Setup

Figure 5-21. SRD Bias Adjustment Test Setups

**UPDATES APPLY TO ALL SERIALS** 

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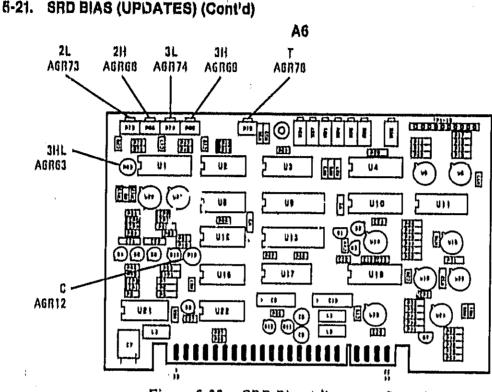


Figure 5-22. SRD Bias Adjustment Locations

#### High Power SRD Blas

- 1. Connect the equipment as shown in Figure 5-21a with the 83590A A6 Sweep Control board on an extender. Do not connect the power supply. With the LINE power OFF, remove the 83590A A4 ALC board. Connect the 8755C MODULATOR DRIVE output to the 83590A rear panel PULSE IN connector.
- 2. Allow the equipment to warm up for one hour.
- 3. On the 8350A/B press [INSTR PRESET] [START] [6] [.] [9] [GHz] [STOP] [1] [3] [.] [5] [GHz] [SWEEP TIME] [4] [0] [0] [ms]. On the 83590A select the [EXT ALC MODE].
- 4. Set the 8755C display resolution for 5 dB/DIV and center the display.
- 5. Set up a zero volt reference on the ocilloscope,

#### NOTE

BEFORE beginning each adjustment, preset the potentiometer to the point where one side of the trace on the oscilloscope display is below zero volts. Adjustment locations labeled 2L and 3L set the left side of the displayed trace. Adjustment locations labeled 2H and 3H set the right side of the displayed trace. DO NOT preset more than one potentiometer at a time.

- 6. Observe the 8755C display, adjust A6R73 (2L) to peak the power at the low end of Band 2 without the power squegging. Then adjust A6R78 (2H) to peak the rest of the band. Iterate between (2L) and (2H) to peak the power across the band without any squegging.
- 7. On the 8350A/B press [START] [1] [3] [.] [4] [GHz] [STOP] [2] [0] [GHz]. Adjust A6R74 (3L) for the low end of Band 3 and A6R69 (3H) for the rest of the band to peak the power without squegging.

UPDATES

UPDATES APPLY TO ALL SERIALS

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#### 5-21, SRD BIAS (UPDATES) (Cont'd)

8. Check the SYTM to YO tracking to ensure it has not changed (refer to Paragraph 5-20). If retracking is necessary, repeat the steps above to eliminate any squegging that may have occurred.

Low and Mid Power SRD Blas



The voltage connected to A6P1-6 is to blas the Modulator/Splitter directly, if A6P1-7 (+10Vdc supply) is shorted to A6P1-6, the Modulator/Splitter will be damaged.

- 9. Set up the equipment as shown in Figure 5-21a, with a 511 ohm resistor connected to A6P1-6 (reference to ground). Remove the 83590A A4 ALC board, Connect the 8755C Swept Amplitude Analyzer MODULATOR DRIVE output to the 83590A rear-panel PULSE IN connector.
- 10. Allow the equipment to warm up for one hour.
- 11. On the 8350A/B, press [INSTR PRESET] [SWEEP TIME] [2] [0] [0] [ms] [START] [7] [GHZ]. Set the power on the 83590A to 20dB.
- 12. Set the 8755C display resolution for 10 dB/DIV and adjust the display to the top graticule. On the 1740A Oscilloscope, select A vs B, set Channel A to .5 B/DIV, set Channel B to 1 V/ DIV, and DC-couple Channels A and B.
- 13. Set the 6214A voltage to .5 Vdc. Increase the voltage until the highest power point is 10 dB above the noise floor (DO NOT EXCEED 5 Vdc).
- 14. Monitor A6TP3 with the oscilloscope and adjust A6R63 until minimum slope (llat display) is obtained.
- 15. Decrease the 6214A voltage until the power at the lowest point between 6.9 and 20 GHz is 10 dB above the noise floor.
- 16. Set A6R12 (C) to a centered position and then adjust to peak the power between 6.9 and 20 GHz. Using the voltage source, keep the RF power at or near 10dB above the noise floor, then repeak A6R12 (C). If the power of the sweep drops at any frequency, maximum peaking has been exceeded.
- 17. Repeat step 14 to verify baseline flatness, readjust A6R63 as needed.

#### Threshold

#### NOTE

# For this adjustment to be accurate, the attenuator must be in the 0.0dB step. (Opt 002 only)

- 18. On the 8350A/B press [INSTR PRESET]. Set the power level on the 83590A to -5dB.
- 19. Observe the 8755C with a 1dB/DIV reference. Preset A6R78 (T) clockwise then adjust A6R78 (T) counter-clockwise until squegging and/or oscillations are eliminated.
- 20. Observe the 8755C trace, increase power slowly to maximum specified power out. If squegging or oscillations reoccur, readjust A6R78 (T) in small increments. If excessive adjustment of A6R78 (T) is required, the SRD bias may be misadjusted.

#### 5-21. SRD BIAS (UPDATES) (Cont'd)

#### SYTM Fundamental Feedthrough

- 21. Set up the equipment as shown in Figure 5-21b without the Low Pass Filter, and with the 83590A A4 ALC board installed.
- 22. Allow the equipment to warm up for one hour.
- 23. On the 8350A/B, press [INSTR PRESET] [START] [8] [GHz] [SWEEP TIME] [2] [0] [0] [ms] [LTIMOD].
- 24. On the 8755C, select A/R DISPLAY and 5 dB/DIV. Center the display.
- 25. On the 8750A, press [SELECT CH 1], and [DISPLAY STORE INPUT]. The display now shows the system error between Channel A and Channel R.
- 26. Press [REFERENCE MEMORY STORE] and then [DISPLAY INPUT-MEM]. The trace on the 8755C should be flat, showing that system errors have been removed. Note the position of the trace and the REFERENCE LEVEL. This will be used as a reference in step 27.

27. Install the Low Pass Filter at the location shown in Figure 5-21b.

- 28. Adjust the REFERENCE LEVEL so that the entire trace is on the display. The SYTM fundamental feedthrough is now displayed on the 8755C,
- 29. Determine how many dB the trace is below the reference position established in step 24. If the trace is less than 25dB below the reference between 8 GHz and 20 GHz, repeat paragraph 5-21.

UPDATES

#### **UPDATES APPLY TO ALL SERIALS**

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#### 5-28. ALC GAIN ADJUSTMENT (UPDATES)

NOTE

Complete adjustment of the leveling loop requires several procedures to be performed in the order prescribed, from Paragraph 5-25 through 5-28. Deviation from this routine may cause improper leveling and/or flatness problems.

#### **REFERENCE**;

Performance test: 8350A/B Paragraph 4-14, Service Sheet: A4

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#### DESCRIPTION:

A4R15 in the input leg of A4U9 adjusts the gain of the Main ALC Amplifier. A4R15 is adjusted for maximum possible gain without producing oscillations.

#### EQUIPMENT

<b>Function Generator</b>			•	• •	•	•	• •	• •	•			•	,			,	• •		•	• 1	• •			• •	•					• 1	• •	F	HI	23	312	A	
Oscilloscope	• •	•	•	• •	Þ	•	F I	• •	•	,	• •	•	•	• •	٠	٠	• •	• •	٠	•	• •	۲		• •	•	•	• •	+	٠	F 1	• •	•	HI	<u>ן</u> י	740	A	
Detector	••	•	• •	• •	•	•	••	• •	•	• •	• •	•	۰ ،	• • • •	•	• •	• •	• •	) }	, , ,	••	•	• •	••	ŀ	- I	p	ģ	49	)	Å		ru Opj	io:	נ / <del>ו</del> 101	C 10	

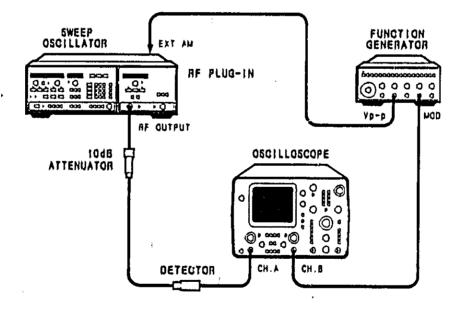


Figure 5-35. ALC Gain Adjustment Test Setup

#### **UPDATES APPLY TO ALL SERIALS**

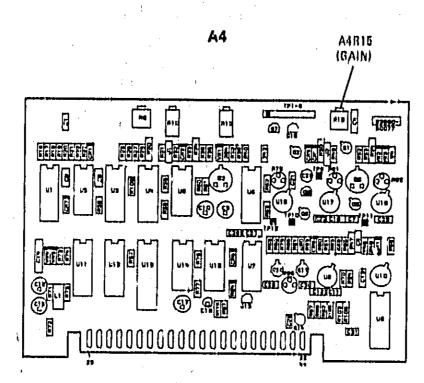
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# 5-28. ALC GAIN ADJUSTMENT (UPDATES) (Cont'd)

This procedure assumes that A3S1 is set to the factory-set position (Table 5-6).

NOTE





### PROCEDURE:

1. Connect Vp-p output on HP 3312A to 1740 CHANNEL A INPUT.

2. Set instrument controls as follows:

#### 8350A/B SWEEP OSCILLATOR

START	
83590A RF PLUG-IN	
POWER LEVEL	
3312A FUNCTION GENERATO	
MODULATION SWP MODULATION RANGE Hz (KN')B)	;

#### **UPDATES APPLY TO ALL SERIALS**

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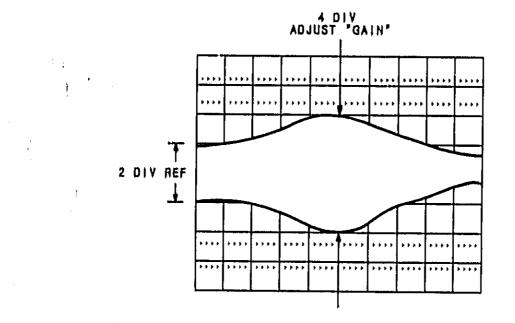


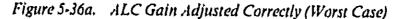
### 5-28. ALC GAIN ADJUSTMENT (UPDATES) (Cont'd)

#### 1740A OSCILLOSCOPE

MODE	• •			•		• •		•	*	•	• •		ŀ			• •		•					• •	• •	Þ					•	• •					M	A	IN	1
CHANNEL A INPUT	•							ι.																									1					40	•
CHANNEL A V/DIV	,	,					•																														J,	hν	r -
CHANNEL B INPUT			• •	• •					• •				• •					• •							<b>F</b> 1												. 1	)(	
CHANNEL B Y/DIV	•	,	•	Þ	٠	• •		۲	•	•	•	• •	,	•	۲	• 1	• •	, ,	٠	•	• •	•	٠	• •	• •		•	• •	•	•	Þ			•	,			I۷	r -
DISPLAY		•	•	Þ	• 1	• •	,	٠	Þ	•	• •	• •	ŀ	٠	•	• •		Þ	•		• •		F I	• •	•	¥	• •	•	,	F	₽ I	, ,			•	• •		. A	<b>L</b>

- 3. Adjust 1740A vertical and horizontal position knobs for waveform at the center of oscilloscope CRT. Adjust START knob, below SWP button, for 10 kHz as displayed on oscilloscope, Turn MODULATION RANGE Hz to 100 and VERNIER to 10K.
- 4. Connect equipment as shown in Figure 5-35.
- 5. On 1740A select A vs B MODE and set CHANNEL A to ,005/DIV,
- 6. Adjust the far left side of the signal for 2 divisions pk-pk by using the CAL on the CHANNEL A knob.
- 7. While monitoring CHANNEL A, manually sweep the entire plug-in frequency range and udjust the ALC,"GAIN" (A4R15) for 4 divisions of peaking at the plug-in frequency where the highest gain peaking occurs. (See Figure 5-36a)





#### UPDATES

UPDATES APPLY TO ALL SERIALS

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#### CHANGE 1

This change documents a new Front Panel Interface.

Page 6-5, Table 6-3;

Change A2 to HP and Mfr. Part Number 83590-60060, CD 1.

Page 6-6, Table 6-3;

Change A2Q4 to 1854-0477, CD 7, Qty 1, TRANSISTOR NPN SI CHIP FT = 1,3 GHZ, 02037, SMCS1005. Add A2R27, 0698-7260, CD 7, RESISTOR 10K 1% .05W F TC = 0±100, 24546, C3-1/8-TO-1002-G.

. Add A2R28, 0698-7205, CD 0, Qty I, RESISTOR 51.1 1%,05W F TC=0±100, 03292, C3-1/8-TO-51R1-F, Delete A2U11.

Add A2U13, 1820-1199, CD 1, Qty I, IC INV TTL LS HEX 1-INP, 01698, SN74LS04N,

Page 8-31, Figure 8-12:

Replace the FRONT Component Locations diagram with A2 Front Panel Interface, Component Locations (CHANGE I) from this document.

Page 8-31, Figure 8-18;

Change the A2 FRONT PANEL INTERFACE part number in the top left-hand corner of the A2 schematic to 83590-60060.

Change the SERIAL PREFIX in the bottom left-hand corner of the page to 2216A.

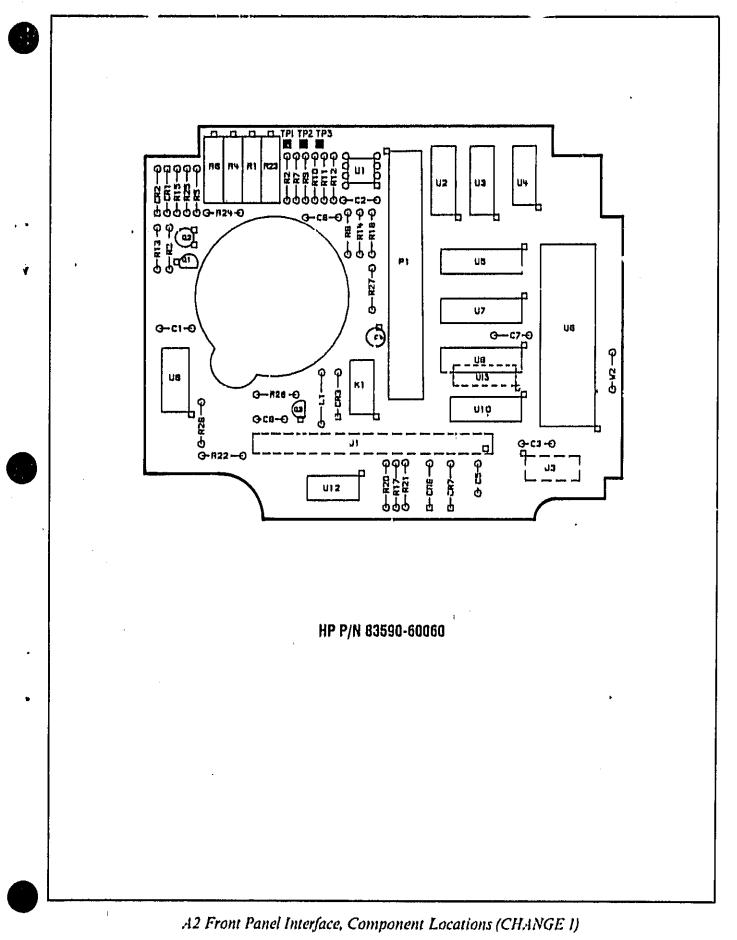
Replace blocks A through G with the partial schematic P/O A2 Front Panel Interface, Schematic Diagram (CHANGE I) from this document.



CHANGE I

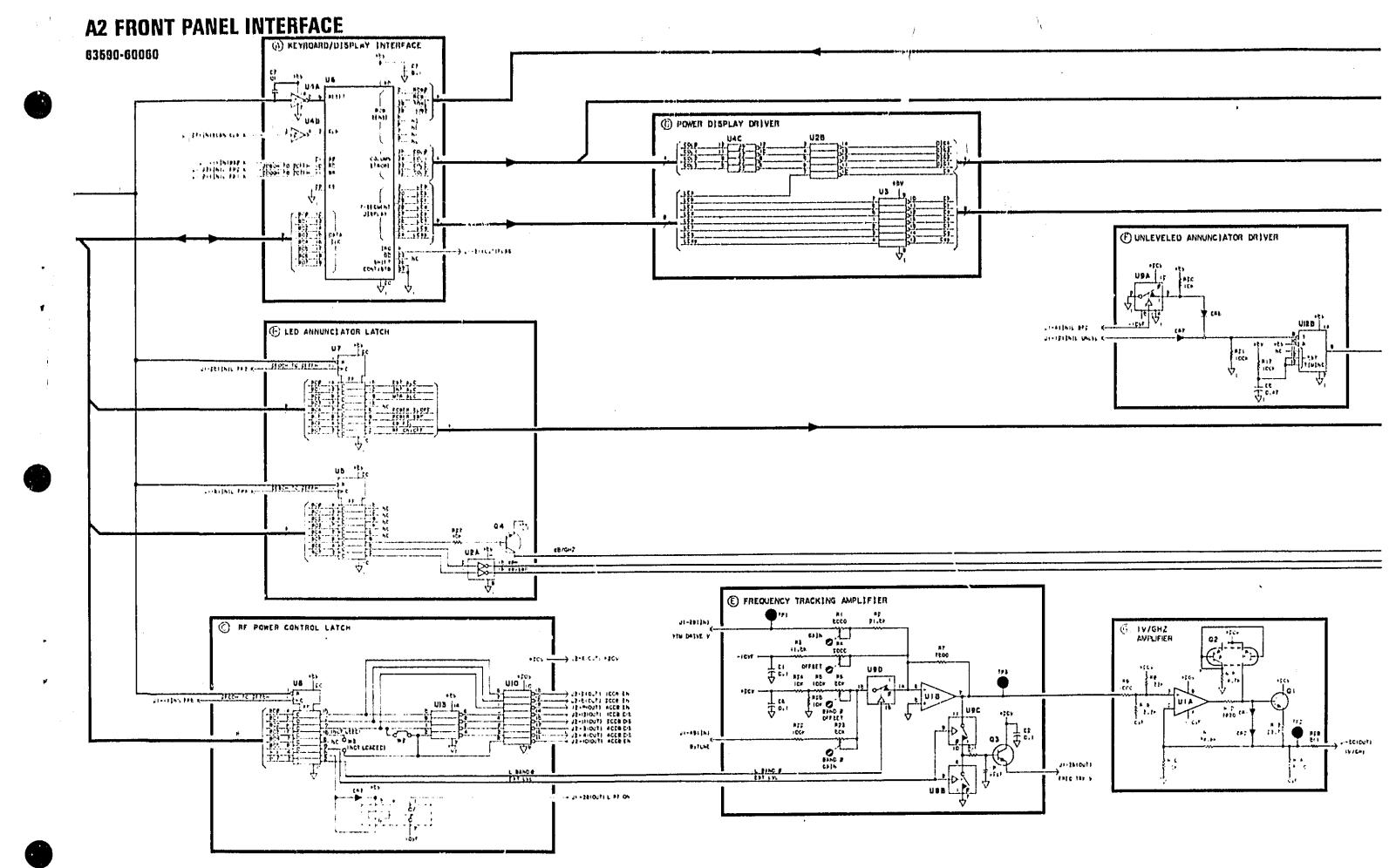
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83590-90005



CHANGE I

1-3/1-4



PIO A2 Front Panel Interface, Schematic Diagram (CHANGE 1)

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## CHANGE 2

#### This change documents a new RF output connector,

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#### Page 6-30, Figure 6-3;

Replace Figure 6-3 with Figure 6-3. RF Output Connector (CHANGE 2) from this document.

CHANGE 2

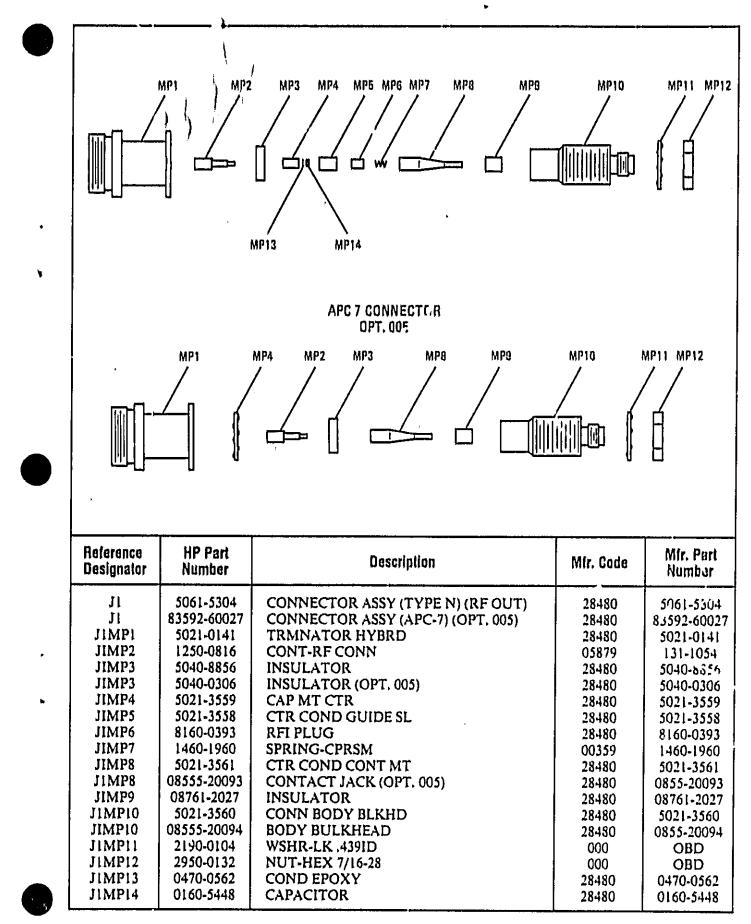


Figure 6-3. RF Output Connector (CHANGE 2)

CHANGE 2

#### CHANGE 3

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HP 83590A

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This change documents a new connector on A16 Modulator/Coupler.

Page 6-5, Table 6-3;

Change AIR4 to HP and Mfr. Part Number 2100-4022, CD 0,

Page 6-21, Table 6-3:

Change A16A1J3 to HP and Mfr. Part Number 1251-3172, CD 7, CONNECTOR-SGL CONT SKI ,03-IN-BSC-SZ-RND,

Delete MP6, KEY CAP-JADE GRAY,



CHANGE 3

3-1/3-2

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### **CHANGE 4**

#### This change increases the compensation effect of the 1 HI adjustment in Band 1.

Page 6-8, Table 6-3;

Change A4R23 to HP Part Number 0698-3162, CD 0, RESISTOR 46.4K 1% .125W F TC=0±100, Mir. Part Number C4-1/8-TO-4642-F.

Change A4R24 to HP Part Number 0698-7262, CD 9, RESISTOR 12,1K 1% .05W F TC=0±100, Mir. Part Number C3-1/8-TO-1212-F.

#### Page 8-47, Figure 8-34:

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In Block **C POWER LEVEL REFERENCE**, change the value of R23 to 46.4K and change the value of R24 to 12.1K. Change the SERIAL PREFIX number in the lower left-hand corner of the page to 2233A. ٠

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#### CHANGE 5

## This change incorporates an improved Modulator/Coupler,

Page 6-21, Table 6-3: Change A16 HP and Mfr. Part Number to 5086-7395, CD 7,

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#### **CHANGE 6**

This change modifies the A4 ALC Board to minin,ize squarewaye overshoot,

Page 6-8, Table 6-3;

Change A4R11 to HP Part Number 2100-2521, CD 0, RESISTOR-TRMR 2K 10% Mir, Code J2: 37, Mir, Part Number 3329W-1-202.

Page 6-9:

5

Change A4R66 to HP Part Number 069%-132, CD 4, RESISTOR 261 1%, Mfr. Part Number C4-1/8-TO-2610-F. Change A4R71 to A4R71*, FACTORY SELECTED - NOT REPLACEABLE. Change A4R80 to A4R80*, FACTORY SELECTED-NOT REPLACEABLE. Change A4R97 to A4R97*, FACTORY SELECTED-NOT REPLACEABLE.

Page 8-47, Figure 8-14;

Change the SERIAL PREFIX number in the bottom left-hand corner to 2249A.

In Block I MAIN ALC AMP change the value of R66 to 261 and change the value of R11 to 2000,

In Block J UNLEVELED SIGNAL change the value of R71 to 2870.

In Block K PIN MOD 1 DRIVER change R80 to R80*, value 511; and change R97 to R97*, value 30,0K.

3

#### **CHANGE 7**

This change adds further improvements to the A4 ALC Board to compensate for modulator variations.

Page 6-", Table 6-3;

Change A4C35 to HP Part Number 0160-0574, CD 3, CAPACITOR ,022µF, Delete A4CR13,

Add A4MP4, HP Part Number 1251-1277, CD 9, Qiy 3, TERMINAL POST.

Page 6-8, Table 6-3:

Change A4R11 to HP Part Number 2100-2489, CD 9, RESISTOR-TRMR 5K.

Page 6-9, Table 6-3;

Change A4R66 to HP Part Number 0757-0416, CD 7, RESISTOR 511. Change A4R71 to A4R71*, FACTORY SELECTED-NOT REPLACEABLE. Change A4R89 to HP Part Number 0698-7267, CD 4, RESISTOR 19.6K. Change A4R90 to HP Part Number 0698-7257, CD 2, RESISTOR 7.5K. Delete  $\sim$ 4R97, Add A4R101*, FACTORY SELECTED-NOT REPLACEABLE. Add A4R102, HP Part Number 0757-0424, CD 7, RESISTOR 1.1K 1% .125W F TC = 0 ± 100. Add A4R103, HP Part Number 0757-0394, CD 0, RESISTOR 51.1 1% .125W F TC = 0 ± 100.

Page 6-13, Table 6-3;

Change A6R53 to HP Part Number 0698-3429, CD 2, RESISTOR 19.6.

Page 8-47, Figure 8-29 (A4 Component Locations):

Dejete R97.

Move R98 to a location directly above and parallel to CR15.

Move R78 to a location directly below Q15 and Q16 and parallel to R98,

Delete CR13 and in its place insert R103.

Add R101, mounted on the far side of the board. R101 is located diagonally between the top of R77 and the top of R90,

Add R102, mounted on the far side of the board, R102 is located diagonally between the bottom of R80 and a feedthrough pad below Q10 (where the top of R78 was formerly connected).

Page 8-47, Figure 8-34 (A4 Schematic):

In Block H SAMPLE AND HOLD DRIVER change the value of C35 to ,022µF,

In Block I MAIN ALC AMP:

Change the value of R66 back to 511,

7

Change the value of R11 to 5000.

In Block J UNLEVELED SIGNAL change R71 to R71* and change the nominal value back to 2610, Replace Block K PIN MOD I DRIVER with P/O Figure 8-34, A4 ALC Schematic Diagram (CHANGE 7) from this

document.

Page 8-57, Figure 8-49 (A6 Sweep Control Schematic): In Block J PULSE MODULATION, change the value of R53 to 19.6,

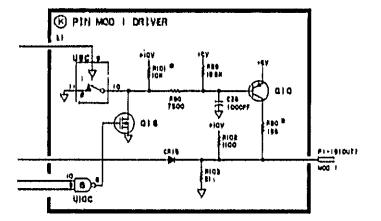
CHANGE 7

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P/O A4 ALC Schematic Diagram (CHANGE 7)

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CHANGE 7

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7-3/7-4

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#### CHANGE 8

This change modifies the AG Sweep Control Assembly for Improved modulator compatibility,

Page 6-12, Table 6-3;

Add A6MP3, HP Part Number 0360-0124, CD 3, CONNECTOR-SOL CONT PIN .04-IN-BSC-SZ RND, Change A6R51 to 0698-7225, CD 4, RESISTOR 348 1% .05W F TC = 0 ± 100, 28480, 0698-7225,

Page 6-14, Table 6-3:

Add A6R83, 0698-7242, CD 5, RESISTOR 1,78K 1%,05W F TC=0±100, 24546, C3-1/8-TO-1780-G, Add A6R84, 0698-7238, CD 9, RESISTOR 1,21K 1%,05W F TC=0±100, 24546, C3-1/8-TO-1210-G,

#### Page 8-57, Figure 8-44;

Add Figure 8-44A. A6 Component Mounting Diagram (CHANGE 8) from this document.

Page 8-57, Figure 8-49:

#### CHANGE 8

8-1/8-2

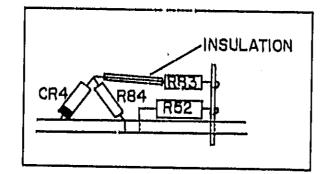
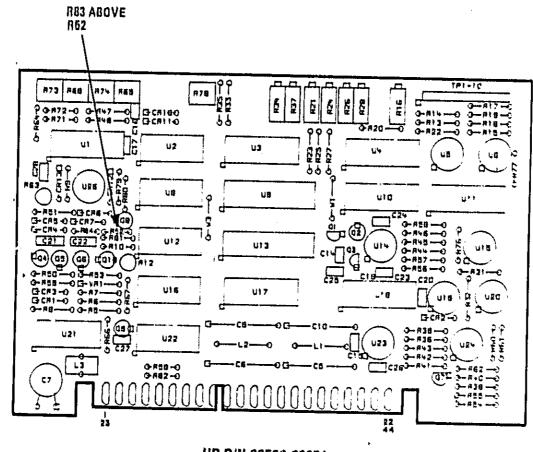


Figure 8-44A. A6 Component Mounting Diagram (CHANGE 8)



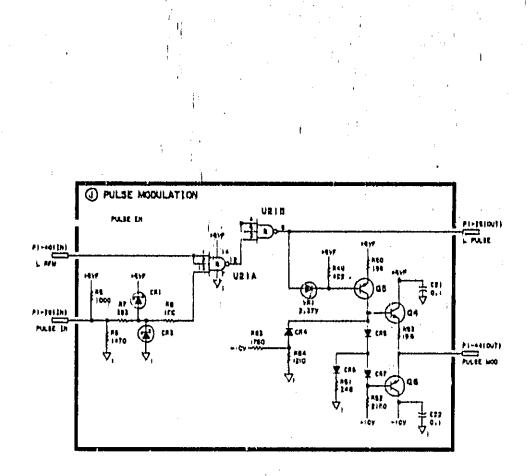
HP P/N 83590-60054

Figure 8-44. A6 Sweep Control Component Locations (CHANGE 8)

CHANGE 8

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8-3/8-4





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#### CHANGE 9

#### This change improves the output power specifications.

#### Page 1-2, Table 1-1, POWER OUTPUT:

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Change the specifications as follows:

Maximum L	eveled Output Po	war;							
2.0 to 7.0 GHz + 10 dBm	7.0 to 13.5 GHz + 10 dBm	13.5 to 18.6 GHz + 10 dBm	13.5 to 20.0 GHz + 10 dBm	2.0 to 18.6 GHz + 10 dBm	2,0 to 20 GHz +10 dBm				
With Option 002									
+8.5 dBm	+8 dBm	+8 dBm	+7 dBm	+7 dBm	+7 dBm				

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Note that the maximum leveled output power for the standard instrument is now  $\pm 10$  dBm across the entire frequency band.

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CHANGE 10

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10-1/10-2

#### CHANGE 10

#### This change update the A3 Digital Interface Board with revised firmware (Revision 4).

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Puge 6-6, Table 6-3:

Change A3 Digital Interface Board to HP Mfr, Part Number 83590-60073, CD 6. Change A3U1 to 83590-80003, CD 4, Qty I, EPROM Lw, Change A3U2 to 83590-80004, CD 5, Qty I, EPROM Hi,

#### Page 8-35, Figure 8-23;

Change the A3 DIGITAL INTERFACE part number in the top left-hand corner of the schematic to 83590-60073, Change the SERIAL PREFIX in the bottom left-hand corner of the schematic to 2315A.

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### SHANGE 11

(Supersedes CHANGE 1)

#### This change incorporates a new A2 Sub Panel Board.

#### Page 6-5, Table 6-3;

Change the A2 Board Assembly Sub Panel part number to 83590-60072, CD 5,

#### Page 6-6, Table 6-3;

Add A2VRI, 1902-004I, CD 4, DIODE-ZNR 5.11V 5% DO-35 PD=.4W.

#### Page 8-31, Figure 8-12;

Replace the Component Locations Diagram with the A2 Front Panel Interface, Component Locations (CIIANGE II) from this document. Note that U13 is now mounted on the front of the board.

#### Page 8-31, Figure 8-18:

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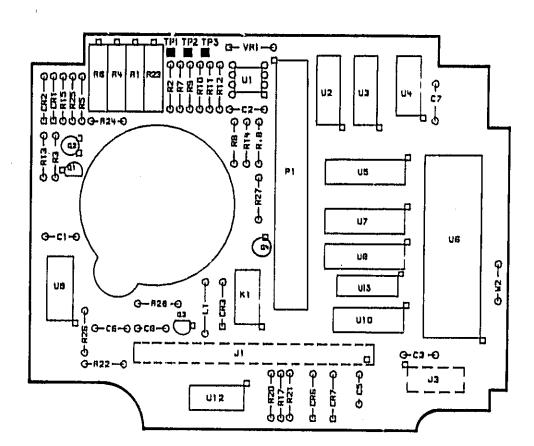
Change the A2 FRONT PANEL INTERFACE part number in the top left-hand corner of the A2 Schematic to 83590-60072.

Change the SERIAL PREFIX in the bottom left-hand corner of the page to 2338A. In Block G (IV/GHz Amplifie:) and VRI across R12, anode connected pin 1 of UIA.



CHANGE II

11-1/11-2



HP P/N 83690-60072

A2 Front Panel Interface, Component Locations (CHANGE 11)

CHANGE II

11-3/11-4

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#### CHANGE 12 (Supersedes CHANGE 8)

This change incorporates a new A6 Sweep Control Board,

Page 6-12, Table 6-3: Change the A6 Sweep Control Assembly HP and Mfr. Number to: 83590-60091, CD 8.

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Page 8-57, Figure 8-44 (A6 Component Locations): Replace Figure 8-44 with Figure 8-44 (CHANGE 12) in this change sheet.

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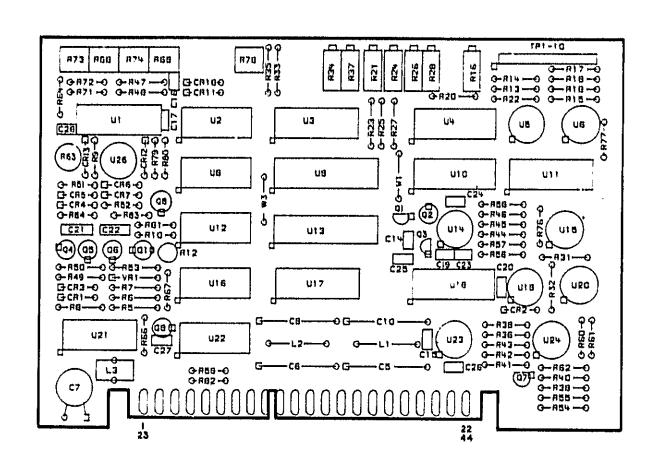
Page 8-57, Figure 8-49 (A6 Schematic):

Change the A6 SWEEP CONTROL part number in the top left-hand corner of the A6 Schematic to 83590-60091. Change the SERIAL PREFIX in the bottom left-hand corner of the page to 2410A.



CHANGE 12

12-1/12-2



HP P/N 83593-60091

Figure 8-44. A6 Sweep Control Component Locations (CHANGE 12)

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CHANGE 12

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12-3/12-4

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### CHANGE 13

Change not applicable.

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#### CHANGE 13

CHANGE D

13-1/13-2

#### **CHANGE 14**

(Supersedes CHANGES 4, 0, and 7)

This change introduces a new ALC board. It is new possible to power meter level the plug-in with the HP 430A and HP 430A as well as the HP 432A.

Page 1-4, Table 1-1, Note 9:

Replace with the following: "Use the HP 432A/B/C, HP 436A, or HP 438A power meters. Both the HP 436A and 438A must be used on the top three (least sensitive) ranges. However, the HP 438A may also be used on the fourth range by programming the response of the power meter's filter as follows: Set the HP 438A to range two, and press [MANFILTER] [1] [ENTER]. See the HP 438A Operating and Service Manual for further instructions. Sweep time 100 seconds for full sweep, typically greater than or equal to 5 seconds per GHz but not less than 10 seconds."

Page 1-9, Paragraph 1-42:

Replace the first sentence with the following: "The RF output can be externally leveled using HP Model 432A/B/C, 436A, or 438A power meters or negative polarity output crystal detectors." Delete the note below the paragraph.

Page 1-11, Table 1-4;

Across from the first listed "Power Meter" under Orlical Spacifications delete: "(No substitute when used for external power meter leveling)," Under Recommanded Model add: "HP 436A," "HP 438A."

Across from the first listed "Thermistor Sensor" under Recommended Madel delete: "HP 8478B" and replace with: "Unit compatible with power meter being used."

Across from the second listed "Thermistor Sensor" under Recommended Model delete: "HP K486" and replace with: "Unit compatible with power meter being used."

Page 3-3, Paragraph 3-25:

Add the following: "For power meter leveling (ALC MODE [MTR]), the power meter is used in conjunction with the internal leveling loop. Low frequency variations are handled by the power meter, and high frequency variations are handled by the internal leveling loop."

Page 3-6, Figure 3-4, Number 1: Delete: "(HP 432 only),"

Page 3-9, Figure 3-7:

Under EQUIPMENT change the Power Meter listing to: "HP 432A/B/C, 436A, 438A." Change the Thermistor Mount listing to: "Any sensor compatible with the power meter being used."

Under the NOTE delete: "The HP 435 and 436 power meters will not power meter level this plug-in. Only an HP 432 may be used." and add: "When using an HP 436A power meter, enable RANGE HOLD to lock power meter in one range," Under PROCEDURE, number 5, delete all reference to "HP 432A."

#### Page 4-2, Table 4-1:

Across from "Squarewave Symmetry" under 83580A Adjusimeni add "5-27."

Page 4-8, Power Meter Leveling:

Insert "13a. External leveling is shown using the HP 432A, HP 8478B, and HP K486A. However, the HP 432A/ B/C, 436A, 438A meters and compatible sensors may also be used."

Page 5-2, Table 5-1:
Change A4R3 to A4R8.
Change A4R5 to A4R12.
Change A4R8 to A4R10.
Delete the line beginning with A4R9.
Change A4R11 to A4R15. Under Description, change U11 to U9.
Change A4R47 to A4R81. Under Description, change U7-Q6 to U17-Q9.
Change A4R56 to A4R82. Under Description, change U5 to U18.
Change A4R59 to A4R78. Under Description, change U8-Q1 to U16-Q6.
Delete the line beginning with A4R67.



14-1

#### 83590-90005

#### Page 5-6, Table 5-2:

Across from 5-27 under "Adjustments," delete "Power Meter Leveling Calibration" and replace with "Squarewave Symmetry Adjustment (CHANGE 14),"

#### Page 5-44, 5-29. ALC Adjustment:

Replace pages 5-44 through 5-46 with the 5-25. ALC ADJUSTMENT (CHANGE 14) procedure in this document.

#### Page 5-49, POWER METER LEVELING OALIBRATION:

Delete pages 5-49 and 5-50 and replace with 6-27. SQUAREWAVE SYMMETRY ADJUSTMENT (OHANGE 14) procedure in this document.

#### Pages 5-51 to 5-54; ALC GAIN ADJUSTMENT:

Replace all reference to A4R11 with A4R15,

#### Page 5-51, DESCRIPTION: Change A4UI1 to A4U9,

#### Page 5-51, EQUIPMENT:

Across from "Power Meter," add: "436A, and 438A,"

Across from both Thermistor Mounts delete: "HP 8478A" and "HP K486," and replace with "Unit compatible with power meter being used."

#### Page 5-54, Paragraph 5-36;

Add the following steps:

- "27. With the Model 83590A set to -5 dBm, press [INSTR PRESET] [OW]. Set the oscilloscope to a 10 us sweep time. If the GAIN control (A4R15) has been over adjusted, the shape of the squarewave on the oscilloscope will be distorted,"
- "28. Back off on A4R15 and observe the squarewave. If the shape of the squarewave improves, back of untithere is no more change. If there is no change, in the shape of squarewave as A4R15 is adjusted, return it to its initial position."

#### Page 6-7, Table 6-3;

Replace the parts list for the A4 Assembly with A4 Replaceable Parts (CHANGE 14) from this document.

#### Page 8-19, A4 ALC Assembly:

Add the following paragraph at the end of the A4 ALC assembly description:

"when used in the ALC MODE [MTR], the A4 ALC assembly uses both the power meter and the internal leveling loop to level the power. Each loop has a separate log amplifier. The output of the "internal" log amplifier is sent through a high pass R-C filter and combined with the output of the power meter log amplifier. This composite signal represents the actual RF power. The power meter leveling loop responds to low frequency variations, while the internal loop responds to high frequency variations,"

### Page 8-35, A4 AUTOMATIC LEVELING CONTROL (ALC), CIRCUIT DESCRIPTION:

Replace pages 8-35 to 8-46 with the A4 ALC CIRCUIT DESCRIPTION (CHANGE 14) from this document.

#### Page 8-47, Figure 8-28;

Replace Figure 8-28 with Figure 8-28. A4 ALC Block Diagram (CHANGE 14) from this document. Note this is a fold-out page.

#### Page 8-47, Figure 8-29;

Replace Figure 8-29, with Figure 8-29. A4 ALC Component Locations (CHANGE 14) from this document.



**CHANGE 14 (Contd)** 

Page 8-47, Table 8-12: Replace Table 8-12 with Table 8-12. Leveling Control Lines (CHANGE 14) from this document.

Page 8-47, A4P1 Pin-out Table:

Replace the A4P1 Pin-out Table with A4P1 Pin-out Table (CHANGE 14) from this document.

Page 8-47, Figure 8-32:

Under NOTE, change the middle paragraph to read: "Adjustment of the EXT/MTR ALC CAL screw will affect the waveforms at TPS and TPS, Adjust the CAL screw until the correct waveforms are obtained."

Page 8-47, Figure 8-33;

Replace Figure 8-33 with Figure 8-33. Open Loop Waveforms (CHANGE 14) from this document.

Page 8-47, Figure 8-34;

Replace Figure 8-34 with Figure 8-34, A4 ALC Schematic Diagram (CHANGE 14) from this document. Note this is a fold-out page.

CHANGE 14

14-3/14-4



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### 5-25. ALC ADJUSTMENT (CHANGE 14)

#### NOTE

Complete adjustment of the ALC leveling loop requires procedures to be performed in the order prescribed, from Paragraph 5-25 through 5-28. Deviation from this routine may cause improper leveling and/or power variation problems.

#### **REFERENCE**:

Performance Test: Paragraph 4-14, Service Sheet: A4

#### DESCRIPTION:

Adjustments compensate for DC offsets in the detected RF path and the Main ALC Amplifier. Power is roughly calibrated and low band flatness is optimized.

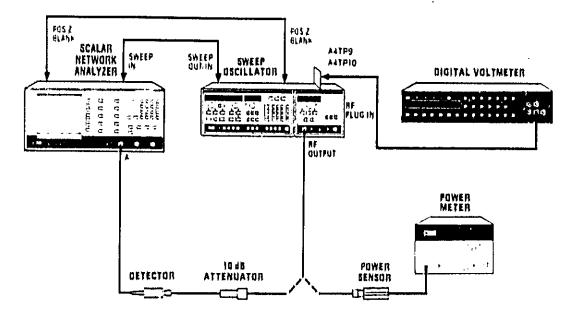


Figure 5-29. ALC Adjustment Test Setup

#### EQUIPMENT;

Digital Voltmeter	HP 3455A
Power Meter	. HP 436A
Thermistor Mount	HP 8485A
Scalar Network Analyzer	HP 8756A
Detector	HP 11664B
Extender Board HP 08	3350-60031
10 dB Attenuator	8493C-010
Sweep Oscillator	HP 8350A

#### CHANGE 14

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### 5-25. ALC ADJUSTMENT PROCEDURE (CHANGE 14) (Cont'd)

PROCEDURE;

#### NOTE

#### Turn AC power OFF when removing or installing PC boards.

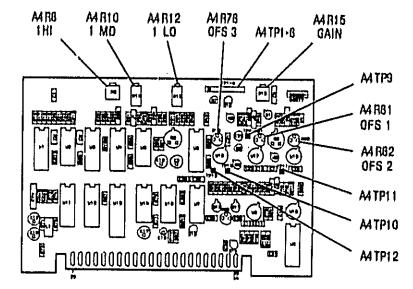
#### NOTE

This procedure assumes that A3S1 is set to the factory-set position (Table 5-6), and that the 8350A/B Sweep Oscillator 27.8 kHz squarewave modulation is selected.

1. Remove the A5 FM Driver board. Put the A4 assembly on an extender board. Press [INSTR **PRESET]** [CW]. Sweep the full range of the plug-in at any leveled power. Preset the following adjustments as indicated:

A4R8I (OFS I)	1	• •	• •	•	•	ŀ	•	• •	•	•	÷	•	Þ	• •	• •	•	•	• 1	, ,	• •	٠	Þ	,	• •	•	•	<b>,</b> 1	• •	•	۲	▶ 1	• •	• •	•	•	٠	<b>*</b> 1	• •	. Midrange
A4R82 (OFS 2) A4R78 (OFS 3)	,	. ,		,	÷		• 1			٠	×	•		• •		,		• 1		•			•		•		•	•							,				. Midrange –
A4R15 (GAIN) A4R8 (1 HI)	, , ,	•	•	•	•	•   •	• •	• •	•	+	•	•	н і н і	••	•	•	+	• •	F F	•	•	•	• •	• •	•	•	) ) )	• •	•	•	F 8	• •	• •	•	•	• • 1	• •	• •	Midrange Fully CW

A4





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### 5-25. ALC ADJUSTMENT PROCEDURE (CHANGE 14) (Cont'd)

- 2. Float the ground on the Digital Voltmeter and measure the voltage between A4TP9 and A4TP10, Refer to Figure 5-30 for adjustment locations, Adjust A4R81 (OFS 1) for 0,000 ± 0,001 Vdc.
- 3. Attach a jumper from A4TP11 to ground. Connect the DVM to A4TP4 (reference to ground) and adjust A4R82 (OFS 2) for a DVM reading of 0.000  $\pm$  0.001 Vdc, Remove the jumper.
- 4. Connect the DVM between A4TP12 and A4TP9 (floating ground), Adjust A4R78 (OFS 3) for a DVM reading of 0,000 ± 0,001 Vdc,
- 5. Set the HP 8350A/B LINE power to OFF. Remove the A4 assembly from the extender board and reinsert the A4 assembly directly into the instrument. Set the HP 8350A/B LINE power to ON and press [CW][2][.][0][GHz s]. Connect the Power Meter censor to the HP 83590A RF OUTPUT,
- 6. Set the HP 83590A for a POWER reading of -5 dBm, Adjust A4R12 (1 LO) for an RF output power at the HP 83590A connector of  $-5 \pm 0.1$  dBm.
- 7. Set the HP 83590A for a POWER reading of  $\pm 7$  dBm. Adjust A4R10 (1 MD) for an RF output power at the HP 83590A connector of  $\pm 7 \pm 0.1$  dBm.
- 8. Iterate steps 7 and 8 until both low and midpower ranges are calibrated and no readjustment is necessary.
- 9. Set the HP 83590A for a front panel POWER reading of  $\pm 10$  dBm, Adjust A4R8 (1 HI) for an RF output power at the HP 83590A connector of  $\pm 10 \pm 0.1$  dBm.
- 10. Reinstall the A5 FM board assembly.

#### 5-27. SQUAREWAVE SYMMETRY ADJUSTMENT (CHANGE 14)

#### NOTE

Complete adjustment of the ALC leveling loop requires several procedures to be performed in the order prescribed from paragraphs 5-25 to 5-28. Deviation from this routine may cause improper leveling and/or power variation problems.

Turn AC power OFF when removing or installing PC boards.

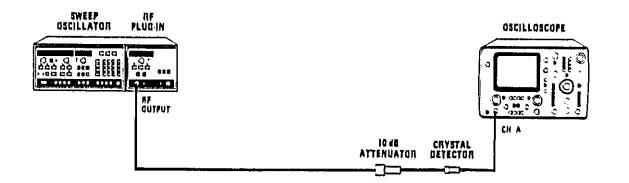
This procedure assumes that A3S1 is set to the factory-set position (Table 5-6).

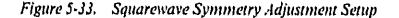
**REFERENCE:** 

Performance Tests: Paragraph 4-21 Service Sheet: A4

#### DESCRIPTION:

C23 (SYM 1) and R99 (SYM 2) minimize overshoot of the squarewave. R92 adjusts the duty cycle of the squarewave,





#### **EQUIPMENT:**

Sweep Oscillator	HP 8350A/B
Oscilloscope	HP 1740A
Diode Detector	НР 8473С
Attenuator	.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,

HP 83590A 83590-90005 5-27. SQUAREWAVE SYMMETRY ADJUSTMENT (CHANGE 14) (Cont'd) Α4 MG23 **MR15 GYM 1** GAIN -2 B 1.00 Q 1117 Θ 0000000000000000061 MR90 SYM 2

Figure 5-34a. Squarewave Symmetry Adjustment Locations

**MR92** 

#### **PROCEDURE:**

1, Connect the equipment as shown in Figure 5-33, with A4 on an extender board. On the HP 8350A/B, press [INSTR PRESET] [CW] [ LT MOD]. Set the RF power level to 0 dBm and allow the equipment to warm up for one hour,

#### NOTE

#### Insure that you do not overdrive the detector as this will distort the squarewave,

- 2. On the oscilloscope, select MAIN SWEEP with a 10µs/DIV time. Set Channel A to .005V/ DIV and Channel B to IV/DIV.
- 3. Press [CW] [3] [GHz s]. Alternately adjust C23 (SYM 1) and R99 (SYM 2) for the waveform shown in Figure 5-34b.
- 4. Press [CW] [10] [GHz s]. Check that the squarewave resembles that shown in Figure 5-34b. If not, adjust C23 and R99 for best squarewave while alternately checking the squarewave at 3 GHz.
- 5. Repeat step 4 for 15 and 20 GHz. Optimize the shape of the squarewave over the entire range of the plug-in. Naturally there will be slight variations at each end of the plug-in's range.
- 6. With the A4 board on an extender, there may be a slight "pip" on the detected signal. This will disappear when the board is mounted in the plug-in,
- 7. If you are unable to obtain the correct waveshape, you may need to adjust the value of R92. Replace R92 with a potentiometer having a mid range value the same as that of R92, Vary its resistance until 50% duty cycle is obtained. Remove the potentiometer and measure its value. Replace with a fixed resistor closest to the measured value,

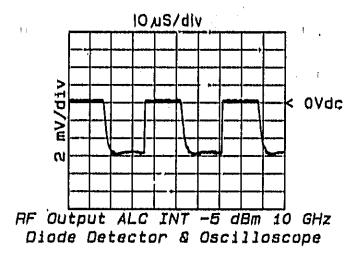
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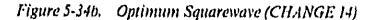
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### Model 83590A Parts List (CHANGE 14) (1 of 5)

Reference Designation	HP Part Number	C D	۵ty	Description	Mir. Gade	Mfr. Port Numbor
44	83590-00177	2	)	ND AY + ALC	26480	83590-60077
AICI	0160-3879	1	4	CAPACITOR/FXD.01UF ±20% 100VDC CER	28480	0100-3879
A4C3	0160-2617	1	1	CAPACITOR-FXD 6.8 UF ± 10% 35VDC TA	25088	DOREGSIBJSK
A-1C4	10100-0945	2	1	CAPACITOR/FXD 910PF ± 5% 100VDC MICA	26460	0160-0945
みもじた	()  6()-4()84	ß	7	CAPACITOR-FXD .IUF ±20% 50VDC CER	28460	0160-4084
A4C7	0160-3874	2	2	CAPACITOR-FXD 10PF ±.5PF 200VDC CER	28460	0160-3874
AACE	480-4084	8		CAPACITOR-FXD JUF ±20% 50VDC CER	28480	0160-4084
1409	0160-4064	8		CAPACITOR-FXD JUF ± 20% SUVDC CER	28480	0160-4084
A4C10	0180-2697	7	- 4	CAPACITOR/FXD IOUF ± 10% 25VDC TA	26460	0160-2697
44C11	0160-3879	7		CAPACITOR-FXD 01UF ± 20% 100VDC CER	26480	0160-3879
44012	0160-3879	7		CAPACITOR-FXD.01UF ±20% 100VDC CER	26460	0110-3879
A4C13	0160-4084	8		CAPACITOR-FXD.IUF ±20% 50VDC CER	28460	0160-4084
34014	4)[6()-4)[27	2	1	CAPACITOR-FXD IUF ± 20% 23VDC CER	28480	0[60-0]27
24215	0160-2697	7		CAPCITOR-FXD JOUF ± 10% 25VDC TA	28480	0160-2697
A4C16	0160-2697	7		CAPACITOR-FXD 10UF ± 10% 25VDC TA	26460	0160-2697
A4C17	0150-2697	7		CAPACITOR-FXD IOUF ± 10% 25VDC TA	26440	0160-2697
AACH	0180-2661	5	1	CAPACITOR/FXD LUF ± 10% 50VDC TA	25066	DIROGSTASOR
A4C19	0)60-4064	16		CAPACITOR/FXD .1UF ± 20% 50VDC CER	26460	0160-4064
A4C20	0160-4084	N.		CAPACITOR/FXD .IUF ±20% 50VDC CER	28480	0160-4084
A4C21	0160-0572	1		CAPACITOR-FXD 2200PF ± 20% 100VDC CER	26460	0160-0372
44C22	0160-3674	2		CAPACITORIFXD IOPF ±.5PF 200VDC CER	26480	0160-3674
A4C23	0121-03448	8	1	CAPACITOR-V TRMR-CER 2.5-5PF 63V PC-MTG	28480	0121-0448
A4C25	0160-4064	6		CAPACITOR-FXD JUF ± 20% 50VDC CER	26460	0160-4084
A4C26	0160-3679	7		CAPACITOR/FXD.01UF ±20% 100VDC CER	26480	0160-3679
A4C28	0160-0572	ţ		CAPACITOR-FXD 2200PF ± 20% 100VDC CER	26460	0160-0372
A4C29	0160-3873	L	2	CAPACITOR-FXD 4.7PF ±.5PF 200VDC CER	28460	0160-3573
A4C30	0160-3873	1		CAPACITOR-FXD 4.7PF ±.5PF 200VDC CER		0160-3873
A4C31	0160-3679	7		CAPACITOR-FXD 01UF = 20% 100VDC CER	26480	0160-3679
AACRI	1901-1098	I	Ô	DIODE SWITCHING INSISO SOV 200MA 4NS		1901+1098
A4CR3	1901-0535	9	4	DIODE - SM SIG SCHOTTKY		1901-0535
A4CR4	1901-1098	ļ		DIODESWITCHING IN4150 50V 200MA 4NS		1901+1098
A4CR5	1901+1098	J		DIODESWITCHING IN4150 50V 200MA 4NS	26460	1901-1098
A4CR7	1901-0535	9		DIODE - SM SIG SCHOTTKY		1901-0535
AICRE	1901-0535	4		DIODE - SM SIG SCHOTTKY		1901-0535
A4CR9	1901-0535	9		DIODE - SM SIG SCHOTTKY		1901-0535
A4CB11	1901+1098	1		DIODE SWITCHING IN4150 50V 200MA 4NS	28460	1901-1048

CHANGE 14

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## Model 83590A Parts List (CHANGE 14) (2 of 5)

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Reference Designation	,HP Part Number	C D	۵ıy	Description	Mfr. Code	Mfr. Part Number
4431	12581124	7	2	PINPROGRANING DUNPER .30 CONTACT	91506	013647561
A4J2	12581124	7		PINPROGRAMING DUNPER .30 CONTACT	91506	013647561
AALL	91408210	1	1	INDUCTOR #FCHHLD LOOUH 5% 166DX 205LG	20409	91400210
A4622	50406040	1	L	BOARD EXTR YELLOW	20400	50406040
A4HP3	58089043	6	ĺ.	PIN	28469	5100-9013
, AAMPA	12514932	9	ī	CONNECTORSGL CONT SKT . 421-THRSCSZ	91506	L6G1AG141
AANPS	71212679	Ó	i	LOL-IN 03596 .14-IN-WD .4-IN-LG	20400	71212679
A401	10530007	7	,	TRANSISTOR PHP 2H3251 BI TO10 PD=361KU	04713	283251
A4Q2	10548484	ġ.	i	TRANSISTOR WPH SI TOLO PD+360HU	28481	18540404
A4Q3	18541295	7	2	TRANSIGTORDUAL HPN PD=400HW	20400	18548295
A4QS	10551306	ý	2	TRANSISTOR JFET 2H4392 HCHAH DHODE	84713	
A4Q6	10551304	ý	•			284392
13.1.140	14331999	,		TRANSISTOR JFET 2N4372 NCHAN DNODE	84713	284392
A4Q7	10550423	5	5	TRANS BTOR HOSFET HCHAN EHODE	17856	VHLERM
A408	18556423	Ś		TRANSLATOR NOSFET HCHAN EHODE	17856	VHLOKN
A407	10540295	7		TRANSISTORDUAL NPH PD=401NH	2040	10544295
AAQLD	18531316	í	2	TRANGISTORDUAL PHP PD=SIANW	2840	10530316
AARLL	18531316	i	•	TRANSISTORDUAL PHP PD=Stehu	2040	16534316
A4913	10551423	5		TRANSISTOR NOSFET NCHAN ENODE	17856	-
A4014	10530451	ś	1	TRANSISTOR PHP 2N3799 SI TU18 PD=361HW		VHLAKK
A4Q16	1055-0423	ŝ	•	TEAUCIETOR MORTET D. CUAN C. MODE	01295	213797
	10134489	3		TRANSISTOR NOSFET NCHAN EHODE	17856	VNLOKN
8488	21002515	2	1	RESIGTORTANK 200K LOX C SIDEADJ LTRN	36703	ETSEV284
A4810	21808678	6	1	REGISTORTHER LOK LOX C SIDEADJ 17THE		3292X1103
A4812	21483753	2	Í.	REBISTORTRHR 208K LOX C SIDEADJ 17TAH		21443753
A4815	21102409	9	- í	REGISTORTRNR SK LOX C SILVADJ LTAH	31703	ETSIX512
A4R16	16907253	ß	2	REGISTOR 5.11K LZ JOSH F TC-41100	24546	CJ1/BT05111F
(AR17	16907253	O		REGISTOR 5.11K 12 .45W F YC=4+144	24546	MT . 1 40 TA 10111
AARIO	1690-7257	2	1	REGISTOR 7.5% LX .45% F TCHA+LAR		C31/8715111F
A4R17	16707263	ĩ	2		24546	C31/8117511F
A4828	16707250	3	Ĩ	RESIGTOR 13.3K 12 .05W F TC=0+100	24546	C31/8T11332F
A4821		6		REGISTOR 0.25K 1X .05W F TC=0+100	24546	CJ1/8TI8251F
N3461	16987261	19	2	REDISTOR LLK 12 .459 F TC=\$ <u>+</u> 148	24546	C31/0T8L102F
A4R22	16987262	9	1	RESISTOR 12.1K 1X .45W F TC+4+148	24546	CJ1/8T11212F
A4R23	16987276	5	i	REGISTOR 46.4K 12 .45W F TC=8+100	24546	CJ1/0T14642F
A4825	1698-7261	ā	•	NEGISTOR LIK IX ,850 F TC+8+188	24546	
A4R26	16987268	7	9	REGISTOR IN IN	24546	C31/8781182F
A4827	06907231	2	-			CJ-+1/0T0L002F
		-	1	RESIGTOR 619 IX .85W F TC=84188	24546	C31/8T06148F
A4R2B	\$6907254	9	4	RESISTON 5.62K 17 .05W F TC=02100	24546	C31/8T05621F
AARIC	• 0371119	7	٠	THERMISTOR ROD SKOHM TC=+.72/CDEG	28484	10371119
AARIL	4690- 1279	8	1	RESISTOR &1.9K IX .85W F TC+84100	24546	C31/0T06192F
A4832	\$69B· -7264	i.	- i	RESISTOR 14.7% 12 .85W F TC+8+108	24546	C]1/GTI1472F
A4833	46997248	2	ź	RESISTOR 3.40K 12 .45W F TC+4-104	24546	C31/8T13401F
		-	•	Conserves action by them to prove \$2588	N7370	#4FV#I#348feeb



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CHANGE 14

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### Model 83590A Parts List (CHANGE 14) (3 of 5)

Reference Designation	HP Part Number	C D	۵ty	Description	Mir. Cade	Mfr. Part Number
A4837	0698 <b>145</b> 7	6	1	RESISTOR 316K 12 1250 F TC+0+100	20400	86983457
A4R35	96907260	7		REGISTOR LOK IX USU F TC+04100	24546	C3-+1/0T81802-+F
A4R36	94907269	?		REBISTOR LOX LX OSW F TC+02100	24546	C31/8T11002F
A4810 A4819	96907243	6	5	REBIGTOR 1.96K 17 85W F TC+8+108	24546	C31/0T01961F
N9847	( 06907202	3	ł	REGISTOR 02.5K IZ 05W F IC=0+100	24546	C31/0T00252F
A48498	06907200	9	1	RESISTOR 147K 12 OSW F TC=0±180	24546	C31/0T01473F
A4R4L	\$6907204	5	i	RESISTOR LOOK LT OSU F TC+0+100	24546	C31/8T01003F
A4R42	46907256	1	3	REGISTOR &. OIK IX USW F TC+0+LOU	24546	C31/0T06811F
A4R46	46907234	5	2	REGISTOR 025 12 05W F TC+01100	24546	C31/0T4025RF
A4847	00370005	6	L.	THERMISTOR ROD 500OHN TC++ 7X/CDEG	20400	08370085
A4840	06907230	9	1	REGIGTOR L.21K 12 .45W F TC=4+104	24546	C]1/0T01211F
A4R49	\$698- ·7215	ġ.	j	REGISTOR 51 1 12 .054 F TC+1+100	24546	C31/0T05181F
A4R50	47571399	5	1	RESISTOR 02.5 12 .1254 F TC+14100	24546	C41/0T80285F
A4851	16987236	7	1	REGISTOR IN 12 .05W F TC=0+100	24546	C31/0T81801F
A4R52	16967229	0	2	RESISTOR SIL 12 . ISU F TC+82188	24546	C3-+1/0-+T0-+511#F
A4853	16907232	3	2	REBISTOR BOL 1X .05W F TC=01100	24546	C31/0T06018F
A4854	16903151	7	i.	RESISTOR 2.07K 12 125W F TC+1111	24546	C41/0T1207LF
A4856	\$6907268	7		REGISTOR LOK 12 . USU F TC=0+140	24546 .	
A4857	f6997240	2		REGISTOR 3.40K 1X .45W F TC+0+100	24546	C31/0T43481F
A4RSO	46907256	1		RESISTOR 6.81K 12 .85W F TC+8+100	24546	CJ1/0T46811F
A4R59	Aton					
A4844	96987229	G		REGISTOR 511 12 .05W F TC=0±180	24546	C31/0T05118F
A4R41	86987247 86987219	6 5	2	REGISTOR 2.07K LX .05W F TC+01100	24546	C31/0T42071F
A4862	16707212	9	3	RESISTOR 196 12 . ISW F TC=1+146	24546	CJ1/QTO1968F
AAR63	\$6907243	6	3	REGISTOR 100 12 .05W F TC=00100 Resistor 1.96K 12 .05W F TC=00100	24546 24546	C]1/0701998F C]1/0791961F
						•
A4R64 A4R63	\$6907256 \ 04907227	ł		AEBISTOR 6.81K 12 .05W F TC+0+100	24546	C31/0T06011F
A4R49	96987222	1	1	RESISTOR 261 12 .85W F TC+8+100	24546	C31/8T0261KF
A4870	1849B+-7277	6 9	ŀ	REDIGTOR SLIK IX .85W F TC=0+100	24546	C31/0T15112F
A4R71	06907216 06907266	Ś	ł	RESISTOR 2.61K 1X .45W F TC=8+100	24546	C31/8T12611F
01074	40107200	2	*	REGISTOR 21.5K 12 .05W F TC+0+100	24546	C31/0112152F
A4R72	46907212	9		REGISTOR 188 1% 85W F TC+8+180	24546	C3L/8T0LIORF
A4R73	06987212	9		RESISTOR 140 12 ASW F TC+02100	24546	C31/8T01408F
<u>84874</u>	86987243	6		REGISTOR 1.96K 12 .05W F TC+0+100	24546	C31/8T01961F
A4875	86987274	3	1	REGIGTOR 30.3K IX ASW F TC=04100	24546	C31/8T03832F
A4R76	86987260	7		REGISTOR LOK 1% .054 F TC+0±LOO	24546	C31/8T81802F
A4877	86987260	7		REGISTOR 10X 12 .05W F TC+04100	24546	C31/8T81842F
A4R7B	21101906	9	1	RESISTORTANR IN LAX C TOPADJ 1 TAN	71138	QZPRIK
A4879	96987269	7		REDIGTOR LOK 17 .45W F TC+8+100	24546	C31/0T01002F
AARED	16987215	9		RESISTOR 51.1 IX .05W F TC+8+180	24546	C3-+1/8T051R1+-F
A4R01	21802038	6	2	RESISTORTRNR 20K 10X C TOPADJ 1TRN	; ;130	GZPRZAK
A4882	21802930	6		REGISTOR- THMR 20K 10X C TOPADJ 1TRH	73138	02PR20K

CHANGE 14

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HP 83590A

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83590-90005



A4 ALC TRCUBLESHOOTING (CHANGE 14) (Cont'd)

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## Model 83590A Parts List (CHANGE 14) (4 of 5)

Reference Designation	HP Part Number	C D	aty	Description	Mir. Gada	Mfr. Part Number
A4R83	0698-7234	5		RESISTOR 825 1% .05W F TC = 0 ± 100	24546	C3+1/8+T0+825R4F
AARBA	0691-7232	j		RESISTOR 681 1% 05W FTC-0 ± 10024546	24546	CJ-1/B-TO-0HIR-F
AARBS	0098-7260	7		RESISTOR 10K 1%.05W / TC=0 ± 10024546	24/46	C3-1/8-TO-1002-F
A4RH7	0698-7243	٥		RESISTOR 1.96K 1% .05W F TC=0 ± 100	24546	C3-1/8-TO-1961-F
ATREE						
	0698-7264	Ĭ	2	RESISTOR 14.7K 1% 05W FTC=0±100	24546	CJ-1/8-TO-1472-F
A4869	0698-7263	0		RESISTOR 13,3K 1%.05W FTC=0±100	24546	C3-1/8-TO-1332-F
A4R90	0698-7264	ļ		RESISTOR 14.7K 1%.05W FTC=0±100	24546	C3+1/8-TO-1472-F
A41391	0698-7240	3	ļ	RESISTOR 1.47K 1% 05W FTC=0 ± 100	24546	C3+1/#+TO+1471+F
.441192	0698-7270	4	ł	RESISTOR 26.1K Ph.05W FTC=0±100	24546	CJ-1/8-TO-2612-17
A4R93	0698-7260	7		RESISTOR 10K 1%.05W FTC=0±100	24546	C3-1/16-T43-1002-F
A4R94	0698-7242	5	l I	RESISTOR 1.74K 1%.05W F TC=0±100	24546	CJ-1/8-TO-1781-F
A4R96	13698-7251	ő		RESISTOR 4.22K 1% .05W FTC=0 ± 100	24546	CJ-1/8-TO-1221-F
A4R97	0698+7267	4		RESISTOR 19.6K 1% .05W FTC=0 ± 100	24546	CJ-1/8-TO-1962-1-
A4R96	0698-7257	2	1	RESISTOR 7.3K 1%.05W F TC=0±100	28480	0698-7257
A4R99	2100-1738	y	1	RESISTOR-TRMR 10K 10% C TOP-ADJ 1-TRN	73138	B20R10K
A4R103	0757-0424	7	i	RESISTOR 1.1K 1% .125W FTC=0±100	24546	C4-1/8-TO-1103-F
A4R105	0698-7205	Ó	,	RESISTOR \$1.1 1%.05W FTC=0 ± 100	24546	CJ-I/B-TO-SIRI-F
A4R106	0698-1440	ĩ	I.	RESISTOR 196 1% .125W FTC=0 ± 100	24546	C4-1/8-TO-196R-F
AARIOS	0698-8827	Å	i	RESISTOR IN 1%,125W FTC=0±100	28460	069658627
A4R110	0698-7243	6		· · · ·		
A4TPL8	1251-5618	0	1	RESISTOR 1.96K 1% .05W FTC=0±100	24546	C3-1/8-TO-1961-F
A4TP9	0360-0535	0	4	CONNECTOR & PIN M POST TYPE	26460	1251+5618
A4TP10	0360-0535	0	۰.	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TPI	0360-0335	U ()		TERMINAL TEST POINT PCD	0000	ORDER BY DESCRIPTION
AATPI2	0300-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
	0100-0311	U		TERMINAL TEST POINT	00000	order by description
A4U1	1826-1186	ß	3	IC SWITCH ANLO QUAD 16-DIP-C PKO		
A4U2	1826-0616	7	2	ic op amp pren guad 14-dip-e pko	Donoș	OPTIEY
AHU3	1826-0610	1	2	IC MULTIPLXR 4-CHAN-ANLO DUAL 16-DIP-C	06665	MUX24FQ
AAUA	1826-0417	6		IC SWITCH ANLO QUAD 16 DIP/C PKG	27014	LF13333D
A4U5	1820-0616	7		IC OP AMP PRCN QUAD 14-DIP-C PKG	06665	OPTIEY
AHUa	1826-0610	1		IC MULTIPLXR 4-CHAN-ANLG DUAL 16-DIP-C	00005	MUX24FQ
A4U7	1620-1197	9	t	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74L500N
A4U8	1826-1186	6		IC SWITCH ANLO QUAD 16-DIP-C PKG		141 Part-1-11 -
A4U9	1826-0319	7	2	IC OP AMP WB TO-99 PKG	A3500	AD3591
74A10	1826-0026	3	1	IC COMPARATOR PRCN TO-99 PKO	01295	LMJIIL
A4U11	1826-0752	2	1	IC CONV 12-B-D/A 16-DIP-C PKG	24355	AD7542BD
A4U12	1820-1216	5	i	IC DCDR TTL LS 3-TO-B-LINE 3-INP	01295	SN7RLS138
A4U13	1820-1730	6	í	IC FF TTL LS D-TYPE POS-EDDE-TRID COM	01295	3N74L5273N
A4U14	1820-1199	i	i	IC INV TTL LS HEX LINP	01295	SN74LS04N
A4U15	1820-1196	ó	í	IC GATE TTL LS NAND QUAD MINP	01295	SN74LS03N
A4U16	1626-0.21	8				
A4010 A4017	1826-0447	8 2		IC OP AMP OP TO-99 PKG	27014	LNIJIOH
יועיה	104040447	4	ł	іс ор амр Wb то-99 рКо	27014	LF25711

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	model	1.1.1	<i>7471 I</i>			
Reference Designation	ilP Pait Number	C D	۵ty	Description	Mír. Gade	Mfr. Part riumber
A4ULB	1826+319	7		IC OF ANY NO TO99 PKG	A3510	AD3591
A4V81 A4V92 A4V93 A4V84 A4V84	19828041 19828111 19823070 19828049 19828849 19828849	49522	112	DIODEZHR 5.11V 5% DO35 PD+.44 DIODEZHR 1H753A 6.2V 5% DO7 PD+.44 DIODEZHR 4 22V 5% DO35 PD+.44 DIODEZHR 6.19V 5% DO35 PD+.44 DIODEZHR 6.19V 5% DO35 PD+.44	20400 20400 20400 20400 20400 20400	19020041 19020111 19023070 19020049 19020049
A494	81598085	0	ł	AEGISTORZERO DINS 22 ANG LEAD DIA	20408	01590005

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### Model 83590A Parts List (CHANGE 14) (5 of 5)



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#### A4 AUTOMATIC LEVELING CONTROL (ALC), CIRCUIT DESCRIPTION (CHANGE 14)

The A4 Automatic Leveling Control (ALC) assembly is part of a closed loop power leveling function, designed to control the amplitude of the RF output power. The **General** section below describes loop operation, including some components external to the A4 assembly. The rest of this operational theory is devoted to detailed description of the circuits found on the A4 assembly.

#### General

The circuits which accomplish power control and power leveling can be divided into two categories: internal loop circuitry, and external components of the loop. Figure 8-24 illustrates this theme.

The Power Level Reference leg of the ALC establishes the desired power level. This is accomplished by pressing the plug-in **[POWER LEVEL]** pushbutton and rotating the RPG or entering the desired reference on the Model 8350A/B front panel DATA ENTRY keys. This leg of the ALC is not an interdependent part of the loop, as shown in Figure 8-24.

The Detector leg of the ALC loop samples the actual RF output power and produces a voltage proportional to RF amplitude. This voltage is converted to log scale and compared with the Power Level Reference signal. If the voltages at the summing junction are not of equal magnitude an error voltage is generated. This error voltage is amplified and converted to a current drive for the RF modulators, which vary the transmitted RF power to correct the error and achieve the desired RF power level.



#### Address Decoder and Control Latches A

U12 is a 3-to-8 decoder, selecting address 2C07H when it is present on the address bus. This address serves as a chip enable for octal latch U13. Information on the data bus is then latched into U13 and used throughout the A4 assembly. U14 and U15 have been added to provide the proper outputs for all 3 ALC leveling modes.

#### Detector Inputs and Selection Switches B

Control lines MUX A0B and MUX A1B are encoded with leveling mode and band selection information. The lines are decoded in Table 8-12. U6 decodes these control lines to select the proper detector input for the desired operating mode.

EXT/MTR ALC input provides external crystal leveling capability within the -10 to -200 n:V range and power meter leveling capability within the 0 to +1V range, VR4 and VR5 provide protection against transients. Two Schottky diodes, CR1 and CR2, are mounted between the EXT/MTR ALC connector and the front panel casting for similar protection.

When MTR (power meter) leveling is selected, the power meter (HP 432A/B/C, 436A, or 438A) is used in conjunction with the internal leveling detector. U1A routes the power meter signal to a separate POWER METER LOG AMPLIFIER. The internal leveling detector is routed through U6B and the input sample and hold to the main log amplifier. The internal leveling detector compensates for the response of the power meter and prevents instability while at the same time permitting reasonable sweep times.



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#### A4 (ALC), CIRCUIT DESCRIPTION (CHANGE 14) (Cont'd)

#### Sample and Hold Drivers K

Q10 and Q11 act as complementary pairs, controlling the Input Sample and Hold, and Error Sample and Hold circuits respectively. The complementary pairs improve action of the sampling FETS Q5 and Q6 by reducing the error signal passed through gate to source capacitance. The sample and hold function of the ALC loop is used in conjunction with pulse and square wave modulation. When L PULSE ENABLE is high, and either L PULSE or SQ MOD input is low, Q10A and Q11B turn on causing Q10B and Q11A to turn off, thereby initializing the HOLD mode,

The frequency of the sampling mode is dependent on the L PULSE or SQ MOD input. When the system is used with the HP 8756A Scalar Network Analyzer, the SQ MOD input is a 27.8 kHz square wave, controlling the gates of Q5 (Block I) and Q6 (Block E). (Refer to Model 8350A/B Operating and Service Manual, Section V, for 27.8/I kHz Oscillator adjustment). A time delay set by R64 and C26 causes an approximate 5  $\mu$ sec delay, enabling the RF signal to come to full power before releasing HOLD and thus preventing overshoot. The sample level is maintained during the OFF pulse, thus preventing saturation of the Log and Main ALC amplifiers,

The SQ MOD input is also connected to the PIN MOD 1 Driver (Block N) for RF modulation when the Model 8350A/B internal squarewave modulation is used,

#### Input Sample and Hold E

The Input Sample and Hold function prevents the Log Amplifier from saturating during pulse and squarewave modulation.

U16 is a unity gain follower with internal feedback whick buffers the detector input. R78 compensates for the offset voltage of the operational amplifier. Q6 and C21 perform the sample and hold function, C23 is used to reduce error due to the gate to source capacitance of Q6.

#### Power Meter Log Amplifier F

The Power Meter Log Amplifier is used in conjunction with the Log Amplifier in ALC MODE [MTR]. The Power Meter Log Amplifier sets the power level and takes care of low frequency variations, while the Log Amplifier takes care of the high frequency variations.

U5B is a unity gain follower which buffers the input of R5D, Logarithmic scaling is performed by Q3A in the feedback loop of U5D. The base-emitter voltage of Q3A is exponentially related to its collector current, hence the logarithmic action of the amplifier. Q3B compensates the Log Amp over temperature. U5A is a standard non-inverting amplifier, with its gain controlled by R33 and R32. CR3 prevents oscillation in the Log Amplifier.

#### Log Amplifier G

The logarithmic scaling function is performed by Q9A in the feedback loop of U17, Q9A collector current is proportional to the voltage at TP10 and exponentially related to its baseemitter voltage. Therefore, Q9A emitter voltage is logarithmically related to the input voltage at TP10.

Q9B compensates the Log Amp against changes in reverse saturation current with temperature.

CR9 clamps the output of U18 to 0.6V above the input voltage to U17, preventing oscillations.

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#### A4 (ALC), CIRCUIT DESCRIPTION (CHANGE 14) (Cont'd)

U6A decodes MUX A0B and MUX A1B (Table 8-12) to select the proper offset voltage for power calibration at the low end of the plug-in power range. In EXTernal ALC, the power level calibration is set with the front panel EXT CAL potentiometer,

U18 amplifies the logged output for comparison with the Power Level Summing Signal (Block H). R9 and R10 adjust the gain of U18, and calibrate midrange power levels for their respective bands.

Guarded-gate FETs Q7, Q8 and Q16 select the appropriate detector return for INTernal, EXTernal, and PM (power meter) leveling.

#### Power Level Reference C Power Level Summing H

U11 is a 12-bit microprocessor-compatible digital to analog converter (DAC), which latches data in three 4-bit nibbles. The -10V REF input sets the DAC for a maximum outut (TP2) of +10V. The voltage at TP2 is the product of -10V REF and the fractional binary input of the DAC.

The voltage at TP1 is the sum of several voltages, depending on the operating mode of the plugin. U2A sums PWR SWP/COMP and AM inputs. In addition, selected feedback resistors R7 and R8 reduce gain to compensate for detector deviation from square-law at the upper limits of the plug-in power range.

The EXT CAL input is summed through amplifier U2C, R30, in the feedback loop of U2C, provides temperature compensation for the Log Amplifier and detectors.

#### Error, Sample and Hold I

The Error, Sample and Hold function prevents the Main ALC Amp from saturating during pulse and square wave modulation.

U2D pin 10 is the summing junction for the Power Level Summing output, Log Amplifier output, and FREQ TRK V is a 0 to 5 volt ramp proportional to the YTM DRIVE Voltage, R1 (SLP) adjusts the overall slope of Band 0.

Under leveled power conditions, the voltage at U2D pin is zero. A non-zero voltage represents an error and forces a change in modulator current until power is again level.

U2D buffers the error voltage. Q5 and the following integrating circuit (U9) perform the sample and hold. C7 eliminates error due to the gate to source capacitance of Q5.

#### Log Amplifier Selector J

The Log Amplifier Selector circuit selects through path for the Log Amplifier, or combines its output with that of the Power Meter Log Amplifier (MTR). In MTR, R84 and C3 act as a high pass filter, to shape the output of the Log Amplifier, which is then combined with the Power Meter Log Amplifier output. The combination of the two prevents instability when using certain power meters.

In switch U4: A and B are open, C is closed in INT or EXT DET mode. The opposite is true in MTR mode.

CHANGE 14

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#### 83590-90005

#### A4 (ALC) CIRCUIT DESCRIPTION (CHANGE 14) (Cont'd)

#### Main ALC Amp L Unleveled Signal M

Both inputs to integrator U9 are at virtual ground under leveled power conditions, allowing for immediate response to an input error voltage,

R15 optimizes the speed at which the loop responds to power level changes,

L RFB goes low during bandswitching to blank the RF power, thus preventing the loop from saturating. When Model 8350A/B RF BLANK is selected, L RFB goes low during retrace and U1D closes, pulling current through C4, forcing TP5 high and turning on the PIN modulators.

Under unleveled conditions, VR2 and VR3 will clamp the output of U9 at approximately +5 and -7 volts, preventing negative or positive saturation. When the output of U9 approaches -2 volts, comparator U10 activates the front panel LED indicating unleveled power.

U8D is not used.

Collector current in common-base transistor QI is exponentially related to the base-emitter voltage. The PIN modulator is driven exponentially to maintain constant loop gain.

Emitter-follower Q2, CR5 and CR4 control the gain of the exponential current drive,

#### PIN Mod 1 Driver N

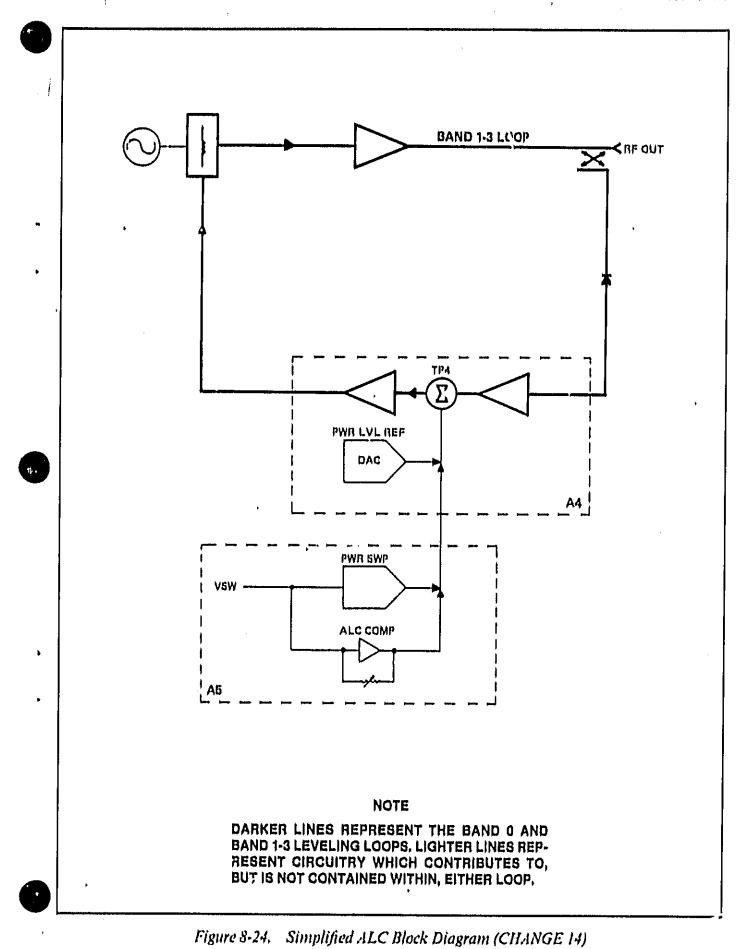
14-22

R105 compensates for the loss of modulator sensitivity with increasing bias current, Q13 and Q14 act to fully turn the modulator on when either SQ MOD or RF blanking is selected.

R92 is factory selected to match the modulator for best square wave modulation symmetry.

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CHANGE 14

14-23/14-24



#### NOTE

#### To ensure that Option 002 plug-ins remain in the same attenuator setting during troubleshooting, press [SHIFT] [POWER SWEEP]. This allows full ALC control without changing attenuator settings.

Since the Automatic Leveling Control (ALC) function of the Model 83590A RF Plug-In includes many individual components arranged in a highly interdependent closed loop, the scope of the A4ALC Troubleshooting section extends well beyond the limits of the A4 assembly. Portions of the A5 FM Driver accombly, and several microcircuit components which contribute to the power leveling function, are discussed below.

The ALC loop is a complex feedback loop which monitors the RF output power and continuously corrects for any deviation from the desired power level. Because it is a closed system, it is difficult to isolate causes from effect when a problem arises. Therefore, the key to troubleshooting is to examine individual components, correlating the expected output for a particular input signal.

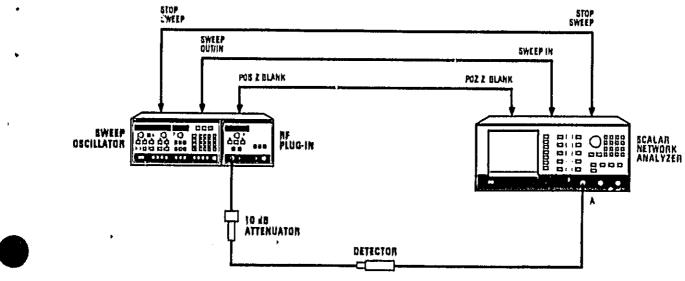
This troubleshooting outline is organized into two major sections: Troubleshooting Symptoms, and Troubleshooting Diagnostics. The section entitled "Symptoms" (1) characterizes possible failure modes, (2) provides some general troubleshooting hints, and (3) refers the reader to more detailed procedures found under "Diagnostics."

#### **Troubleshooting Symptoms**

The procedures outlined below help to systematically characterize the failure as quickly as possible. The following failure symptoms are discussed:

RPG/POWER DISPLAY FAILURE UNLEVELED (LED) FLATNESS/OSCILLATIONS (Power Dropouts) FULL UNCEVELED POWER NO POWER (Single Band) NO POWER (All Bands) POWER SWEEP/FLATNESS

Evaluating the specific failure may require an HP 432A/B/C, 436A, or 438A Power Meter or the HP 8756A Scalar Network Analyzer with the Model 11664B Detector. (However, a crystal detector with an "A vs B" oscilloscope may often be substituted.) Figure 8-25 configures a typical test setup. Initiate all tests with the **[INSTR PRESET]** condition.





#### **RPG / POWER DISPLAY FAILURE**

Check that the POWER display changes when either the RPG is rotated or data is antered via the Model 8350A/B keyboard. This verifies that the digital information is reaching the mainframe, is properly processed, and is then displayed.

• If the display is flashing rapidly or showing random patterns, refer to A1/A2 Front Panel or A3 Digital Interface Troubleshooting. If the RPG causes a change in the measured RF power level, but the POWER display remains the same, refer to A1/A2 Troubleshooting. If the RPG produces no response whatsoever, or if the front panel display is blank, refer to A1/A2 Troubleshooting, and trace the problem back to the Model 8350A/B mainframe,

#### UNLEVELED (LED)

If the UNLEVELED light turns on during the sweep, enter a sweep time of 20 seconds (i.e. one second per GHz). Observe the SWP light on the Model 8350A/B Sweep Oscillator, and determine at which times during the sweep the UNLEVELED light turns on.

- If the UNLEVELED light remains lit during retrace, suspect problems in the front panel annunciator drivers. Refer to AI/A2 Troubleshooting.
- If the UNLEVELED light is on during the entire forward sweep, suspect components common to all bands.

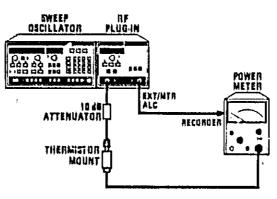


Figure 8-26, Power Meter Leveling Setup





- If the UNLEVELED light flashes on briefly three times during the sweep (at 7 and 13.5 seconds into the trace), the problem occurs at the bandswitch points. Check for the RF blanking (L RFB) pulses during bandswitch at A4P1-29, as shown in Figure 8-30. If the signal is missing, trace the problem back through the Model 8350A/B, to the blanking request (L RFBRQ) line on the RF Plug-In A6 assembly, If L RFB is present, but A4TP5 does not clamp at greater than or equal to +4 Vdc during blanking, suspect A4U2D or A4U9.
- If the UNLEVELED light flashes briefly during the sweep, but does not imply any of the above failure modes, check power flatness. See below.

#### FLATNESS / OSCILLATIONS (Power Dropouts)

Monitor the RF output with the HP 8756A as shown in Figure 8-25. Optimize the output power with the front panel PEAK control.

- If the power level is constant across the sweep within approximately 5 dB, then the Plug-In may only require ALC flatness adjustments. Refer to Section V, Adjustments, in this manual, for the Internal Leveled Flatness adjustment procedure.
- If the measured power level lies between +10 and -5 dBm, but cannot be controlled via the front panel, refer to the Digital Control section under Troubleshooting Diagnostics.
- If the trace appears chopped or broken, the loop may be oscillating. Refer to Section V, Adjustments, in this manual, and perform the ALC Gain adjustment procedure.

#### FUL!. UNLEVELED POWER (One or More Builds)

If power is unleveled in one Band only, select a sweep width within the unleveled band(s). If power is unleveled in all bands, continue to sweep the plug-in's full range,

- Attempt to level the power externally using the HP 432A/B/C, 436A, or 438A Power Meter as shown in Figure 8-26. Select MTR leveling, and enter a 100 second sweep time. If the RF power is now leveled, the failure is most likely in the detectors or the Detector Selection Switch, A4U6. Refer to the following paragraph. If this does not prove to be the case, the problem may be in the two analog switches U3B and U6A. It may be necessary to perform the ALC adjustments in Section V of this manual.
- Check the Detector Selection Switch by entering a CW frequency within the band or leveling mode in question and trace the detector voltage through U6B. If the input to be selected does not match the output, check the MUX A0 and MUX A1 lines (see Table 8-12), Also check U12 and U13 as described under Digital Control.
- Check the voltage at TP5. If it is greater than or equal to +5 Vdc, suspect the Mod Drivers or Modulator. If it is below -2 Vdc, suspect the Detectors and Detector Leg.



14-27

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#### A4 ALC TROUBLESHOOTING (CHANGE 14) (Cont'd)

NO POWER (Shigle Band Only)

If no power is detected in one band, but there is leveled power in another band, suspect the components of the RF path appropriate to the faulty band within the ALC loop.

#### NOTE

Turn off LINE switch before removing or installing any assembly.

With the ALC assembly removed from the plug-in, 27.8 kHz squarewave modulation from the Model 8350A/B is not available. However, the HP 8756A 27.8 kHz squarewave can be connected to the rear panel PULSE iN connector to maintain HP 8756A compatibility.

- To check the RF components, remove the A4 ALC assembly from its socket. This removes all bias from the modulator, and should allow maximum power through the RF path in all bands. If full power (at least +12 dBm from 2 to 20 GHz) is then detected in all bands, the RF Amplifier (A14), the DC Return (A15), the Isolator (AT1), and the YTM (A12) are verified. Suspect primarily the appropriate detector. Also inspect the modulator, as well as the A4 Mod Driver and Detector Selection Switch.
- If the RF signal for all bands is missing, check the A6 SRD and PIN Diode Bias circuit.

NO POWER (All Bands)

#### NOTE

## Turn off line power before removing or installing any assembly.

- If no power is detected in any band, remove the A4 ALC assembly. This removes all bias from the modulator, and should allow full RF power to be transmitted. If there is still no power, check the rear panel AUX OUTPUT for approximately 0 dBm to verify that the A13 YIG Oscillator is providing an RF output. Refer to RF Troubleshooting for details.
- If removing the A4 assembly causes full unleveled RF power to appear, reinstall the board and check A4TP5. If less than -2 Vdc is present, verify that the voltage across R49 is zero. If A4TP5 is greater than +5 Vdc, suspect any circuitry between the Detector Selection Switch and A4TP5, particularly the Log Amp.

#### **POWER SWEEP / FLATNESS**

• If power increases smoothly with frequency, and POWER SWEEP is NOT selected, suspect problems with the A5 FM Driver assembly,

#### NOTE

### Turn off line power before removing or installing any assembly.

Remove the A5 board from the plug-in. It the situation improves, suspect a failure on the A5 assembly.

• If the RF power is leveled within approximatley 5 dB, refer to Section V, Adjustments, in this manual, and perform the Internal Leveled Flatness adjustment procedure.

HP 83590A

#### A4 ALC TROUBLESHOOTING (CHANGE 14) (Cont'd)

#### **Troubleshooting Diagnostics**

The triubleshooting information below is organized into functional areas:

DIGITAL CONTROL REFERENCE POWER LEVEL СН **DETECTCRS / DETECTOR SELECTION SWITCH** B, CR1 DETECTOR LEG E F G MODULATOR LEG | L MOD DRIVER Ν MODULATOR A13 SAMPLE AND HOLD EK

DIGITAL CONTROL Α

Address Decoder U12 and Control Latch U13 control digital switches throughout the A4 assembly. Their operation can be confirmed by performing the Hex Data Rotation Write at address 2C07 Hex. Enter the following keystrokes:

[SHIFT] [0] [0]	Enters Hex Data command
[2] [GHz e] [0] [7]	Address location 2C07 (U13)
[M4]	Hex Data Rotation Write

Check the outputs of U13 for the waveforms shown in Figure 8-2.



If any output signal is missing or misplaced, check the data lines agains Figure 8-2. If no output is found, look for activity at U13 pin 11. Check for L INST1 and BA3 to pulse low, while BAO, BAI, and BA2 pulse high. If these pulses are missing, trace the problem back to A3 Digital Interface.

If the Digital Control section is working, the primary outputs of U13 are easily controlled by selecting the appropriate front panel function while in the CW sweep mode. (e.g., BI is held high by selecting a CW frequency in Bands 1 through 3; selecting MTR leveling holds the PM line high, etc.).

#### **REFERENCE POWER LEVEL** CH

The Reference Power Level Leg produces a voltage proportional to the desired power level. This signal is a summation of the absolute power reference, AM, detector compensation, and power sweep signals.

The detector compensation and power sweep signals are generated on the A5 FM Driver assembly, If an A5 failure is suspected, refer to troubleshooting information on the A5 Service Sheet. Unless A5 is suspect, simplify A4 troubleshooting by turning off the line nower and removing the A5 assembly, Although power sweep will be disabled and the power flatness will be lost, the ALC Loop should still level without the signals provided by the A5 assembly.

DAC UII establishess the absolute power level. The -10V REF from the A6 assembly is scaled to yield from 0 Vdc (-5 dBm displayed) to the +10 Vdc (+20 dBm displayed) at TP2. (This breaks down to a voltage step of 0,40 Vdc per 1,0 dB of power over the dynamic range, or 6,00 Vdc at + 10 dBm.

A self-test routine is available to exercise the ALC DAC. Enter:

[SHIFT] [5] [0]

The waveform in Figure 8-31 should be seen at TP2. Note that the exercise routine for the 12-bit DAC yields a staircased waveform with 13 levels. The first step shows the maximum +10 Vdc output with all bits high. The following levels represent the voltage at TP2 with successive bits loaded high in order from the Most Significant Bit to the Least Significant Bit.

• If the waveform at TP2 is not correct, check for -10V REF, and trace any problem back to the A8 assembly. Look for activity on L INST1, BA0, and BA1, BA2 and BA3 should pulse high as each new DAC value is loaded, pulsing the CS line (U14 pin 8) low. If any of these lines, or a data line, appears dead, trace the problem back to the A3 assembly.

U2A adds PWR SWP/COMP and AM, and provides detector flatness compensation at higher power levels with CR1. Use the EXT MTR mode to bypass this diode while troubleshooting.

U2C adds the front panel amplitude adjustment (EXT CAL) used with external leveling. The following levels should be seen at TPI with A5 removed and INT leveling selected: +0.3 Vdc for -5 dBm, and +7.0 Vdc for +20 dBm. An amplitude modulation (AM) signal of 1.0 V p-p at PI-4 will produce roughly 260 mV p-p at TPI. (Note that U3A and CR1 in the feedback path around U2A change the gain depending on the band and the desired power level. This may result in a 1.0 Vdc difference between bands at +20 dBm.)

#### DETECTOR CR1 / DETECTOR SELECTION SWITCH B

The detector CR1 is tested simply by checking the output voltage under full leveled power or full unleveled power conditions.

#### NOTE

The 27.8 kHz modulation signal required for HP 8756A compatibility is not available from the Model 8350A/B when the A4 assembly is removed from the plug-in, and must be supplied from the HP 8756A through one of its rear panel MODULATOR DRIVE connectors.

- If no power is measured in the suspected band, turn off the line power and remove the A4 assembly. Return power to the instrument. (If there is still no RF power, suspect components of the RF path. Refer to RF Troubleshooting.) If full unleveled RF power is obtained, apply a narrow strip of cellophane tape to the pin-edge connector at P1-19 to isolate the output of the modulator driver from the modulators. Reinstall the A4 board. This removes bias from the modulator, allowing full RF power transmission, while providing detector bias.
- If full leveled power (+10 dBm from 2 to 20 GHz) or full unleveled power (at least +2 dB higher than leveled) is measured, sweep only the band in question and check the voltages at the detector input against the values shown in Table 8-11. (Use high-impedance 10:1 probes.)

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### A4 ALC TRCUBLESHOOTING (CHANGE 14) (Cont'd)

	Full Levoled + 10 dBm	Full Uniovolod + 20 dBm
Bands 1-3 (A4P1-20)	-100  to  -120  mV	−200 to −600 mV

#### Table 3-11, Detector Voltages

- If the detector is working and the Detector Selection Switch is suspected, sweep only in the faulty band and monitor TP12 for the voltages seen at the selected input of U6B.
- If the EXT/MTR ALC INPUT circuits are suspected, select the desired moce and supply a test signal (low-level DC or sine wave) in the front panel BNC connector, and trace it through U6B at A4TP12,

#### NOTE

# Remove any tape applied to edge connector pins in the previous procedure.

#### DETECTOR LEG E F G

The Detector Leg of the ALC loop includes components between the Detector Selection Switch and the Error Summing Amplifier U2D.

Before troubleshooting the Detector Leg, be sure the Detector and Detector Selection Switch are working correctly. See above.

The Detector Leg can be effectively tested by using the Open Loop method of troubleshooting. This procedure utilizes the external leveling mode (EXT) by supplying an external DC voltage or sine wave to the EXT/MTR ALC INPUT connector. This method breaks the ALC Loop and allows waveforms to be checked against known test signals. See Figure 8-32.

#### MODULATOR LEG | L

The Modulator Leg includes the Error Sample & Hold and the Main ALC Amp.

U2D is a non-inverting unity-gain summing amplifier. Under leveled conditions, both U2D pin 10 and TP8 should be nearly 0.0 Vdc. Under any conditions (except during "hold"), U2D pin 10 and TP8 should be at the same voltage. If not, suspect U2D, Q5, or the Sample & Hold Driver.

U9 forms an inverting integrator. When TP8 is positive, TP5 should be at -7 Vdc. If not, suspect U1D or U9. When TP8 is negative, TP5 should be at +5 Vdc. If this is not the case, suspect U9.

- The following procedure can be used to check U^oD and U9;
  - 1. Use a jumper to ground A4TP11,
  - 2. Set power for -5 dBm at any CW frequency.
  - 3. Press Model 23590A [EXT] ALC.



- 4. To check U2D, monitor U2D pin 10 and TP8 while adjusting the EXT/MTR ALC CAL screw between the extremes of its range, Both U2D pin 10 and TP8 should vary between approximately +0.5 and -0.5 Vdc,
- 5. Verify U9 by adjusting the CAL screw as described above and monitoring TP5. Since U9 is an integrator, TP5 should saturate and clamp (due to VR2 and VR3) at -7 Vdc and +5 Vdc, respectively, (When sweeping across a bandswitch point, RF blanking pulses will saturate TP5 at +5 Vde regardless of input.)
- 6. Remove jumper from A4TPH to ground,

Further troubleshooting of the Modulator Leg can be continued by following the Open Loop procedure outlined in Figure 8-32 and checking for the waveforms provided in Figure 8-33.

#### MODULATOR DRIVER N

The voltage-to-current conversion and current gain needed to drive the modulators is provided by Q2 and Q1 on the output of the Main ALC Amplifier. As the voltage increases at TP5 so does the current to the modulator, shunting more RF energy to ground and allowing less to pass through. Since the modulator is essentially current-controlled, the voltages measured at TP6, PI-19, and PI-44 do not vary much over a wide range of modulator attenuations.

Q2 is an emitter-follower followed by a common-base stage (Q1), with two diodes in between. Check the biases and base-emitter voltages to see if the transistors are damaged.

To establish a bias level for the Mod Driver stages, TP5 can be forced high (+5 Vdc). Using a jumper, ground A4TP11. Press Model 8350A/B [CW] and select a CW frequency in the appropriate band. Select [EXT] ALC, and enter an RF power level of -5 dBm via front panel controls. Rotate the EXT/MTR ALC CAL knob fully counterclockwise. Verify a signal level of approximately +5 Vdc at TP5. Remove jumper from A4TP11 to ground.

R92 is adjusted for 50% duty cycle of the square wave.

 Set the HP 8350A/B to CW, SQ MOD on. Connect the RF output to a crystal detector and oscilloscope. While observing the square wave, adjust R92 for 50% duty cycle.

#### MODULATOR

The internal modulator for this plug-in is housed in a combination microcircuit package with Modulator/Coupler. Figure 8-27 provides a simplified schematic for this positive-bias, shunt-type attenuator. As more current is supplied through the modulator bias pin, the shunt diode turns on harder, sinking more RF power to ground and allowing less to reach the front panel.

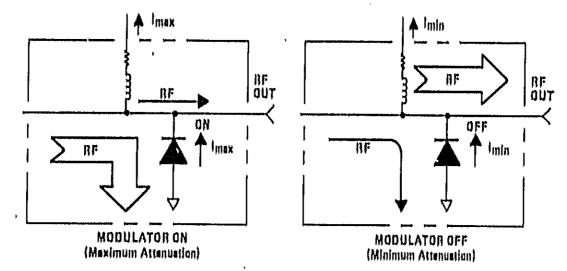


Figure 8-27. Simplified Modulator Schematic

The modulator is checked simply by noting whether the actual RF attenuation is appropriate to the modulation bias present.

#### NOTE

#### Turn off line power before removing or installing any assembly.

- If low or no RF power is observed, remove all modulator bias current simply by removing the A4 assembly from the Motherboard. With no bias current, the RF power should pass through the modulator unhindered. If this is not the case, check the modulator diode as follows:
  - 1. Select Model 83590A [EXT] ALC. Attach a jumper from A4TP11 to ground. Enter -5 dBm RF power, and select a CW frequency in the appropriate band. Rotate the EXT/MTR ALC CAL knob fully clockwise. This should result in -7 Vdc at TP5, essentially removing bias from the modulator. Measure the voltage across R49. It should be 0V. If this is not the case, isolate each modulator from its drive circuitry by applying a piece of cellophane tape to the pin edge connection: P1-19. If the voltage across R49 now measures 0V, the modulator diode is probably shorted. If the voltage across R49 still does not measure 0V, suspect the band blanking circuitry U8C and Q14. Remove jumper fron: A4TP11 to ground.

#### NOTE

#### Remove any tape applied to the pin edge connectors in the previous procedure.

- If the modulator appears to be functioning properly, check the following RF levels with a power meter or spectrum analyzer. When checking power levels internal to the RF signal path, ensure that all critical ports are terminated in 50 ohms.
  - 2. If power is low in all bands, check the RF level at the rear panel AUX OUTPUT connector. Refer to the RF Schematic Diagram at the end of Section VIII for the proper levels. Check the RF levels around the Power Amplifier A14 with no modulation. A14 should output approximately +26 dBm with about +13 dBm at the input.

- If maximum unleveled RF power is observed, attempt to achieve maximum attenuation (minimum RF transmitted), Select Model 83590A [EXT] ALC, Attach a jumper from A4TP11 to ground, Enter -5 dBm RF power, and select a CW frequency in the appropriate band. Rotate the EXT/MTR ALC CAL knob fully counterclockwise, The voltage level at TP5 should be +5 Vdc, Concurrently, the voltage level at the output of the Mod Driver, PI-19, should be approximately +0.6 Vdc to +0.8 Vdc,
  - 1. If the voltages are significantly higher than this, the modulator diode is probably open.
  - 2. Check TP6 for approximately +2.0 Vdc. The difference between the test point and the corresponding pin-edge connector gives an indication of how much current is flowing to the modulator.

#### SAMPLE AND HOLD E K

There are adjustments to improve the shape of the squarewave, C23 in block E and R99 in block K are used to eliminate offset in the Input Sample and Hold, and Error Sample and Hold circuits respectively. They act to effectively cancel charge passed through the gate to source capacitance of the FET. Refer to Paragraph 5-27 for the proper adjustment procedures. **A4** 

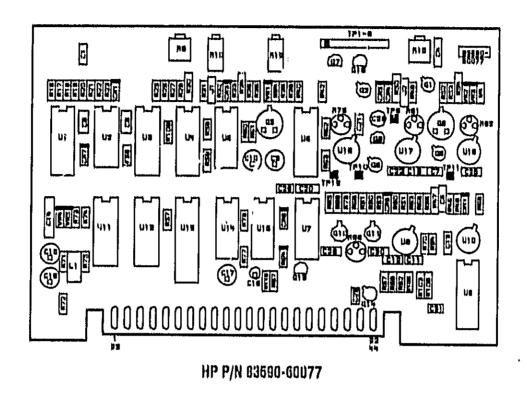


Figure 8-29. A4 ALC Component Locations (CHANGE 14)

CHANGE 14

14-35/14-36

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Lovaling	DATA BUS									
Lovaling Mada	PM	Mux A1B	Mux AOB	Mux At	Mux A0					
INT 0 (not used	Ļ.	Н	В	H	H					
INT	J.,	н	L	Н	L					
ext	L	L	Н	l.	H					
PMO (rut used	н	H	Н	L	L					
PM I	H	н	L	L	L					

Table 8-12, Leveling Control Lines (CHANGE 14)



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14-37/14-38

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## A401 Pin-out Table (CIIANGE 14)

<u> </u>	Ì			
PIN	BIGNAL	10	TO/FROM	FUNCTION
1 23	EXT DET NET	IN	J2	р
	EXT DET	IN	J2	В
2	L UNLVL	OUT	A0P1+40, A10J1+12	M
24	Ext oal	IN	A10J1+41	
3 25	PWR REF	OUT	NOT USED NOT USED	Ç
4 20	AM	IN	P1-M NOT USED	C
5	PWR 6W/COMP	IN	A5P1+23	C
27	+5V	IN	A3P1+6,7	P
6 20	-15V	IN	NOT USED P2-20	p
7	+10V	IN	P1+8	ր
20	L AFB	IN	P2+56	Լ N
B 30	GND DIG GND DIG			p p
0	BD1	IN	A3P1-0	A, C
31	BD0	IN	A3P1-31	A, C
10	BD3	N	A3P1+10	A, C
32	BD2	N	A3P1+32	A, C
11	BA1	IN	A3P1+11	A, C
33	BAL'	IN	A3P1-33	A, C
12	8A7	IN	A3P1+12	A, C
34	8A2	IN	A3P1+34	A, C
13	805	IN	A3P1-13	A
35	804	IN	A3P1-35	
14	BD7	IN	A3P1+14	A
36	BD6	IN	A3P1+36	
15 37	GND ANLG GND ANLG			p p
16 38	+15V	IN	NOT USED P2-20	р
17	-10V	IN	P1+13	р
39	-40V	IN	P1+11	Р
18	L INSTI		A3P1+8	A C
40	SQ MOD		P2+26	K, N
19	MOD 1	OUT	A10E1	N
41	L PULSE	IN	AGP1+25	K
20	INT DET	IN	ORI	B
42	INT DET RET	IN	CRI	
21 43	-10V REF	IN	NOT USED ABH1-3	0
22 44	MOL DRIVE	OUT	NOT USED NOT USED	L

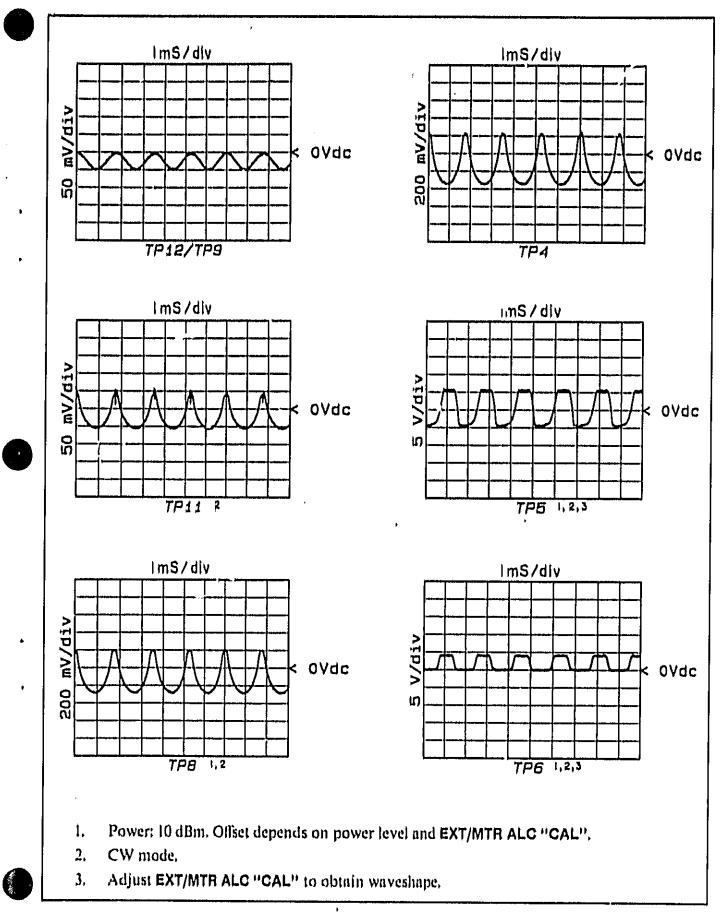
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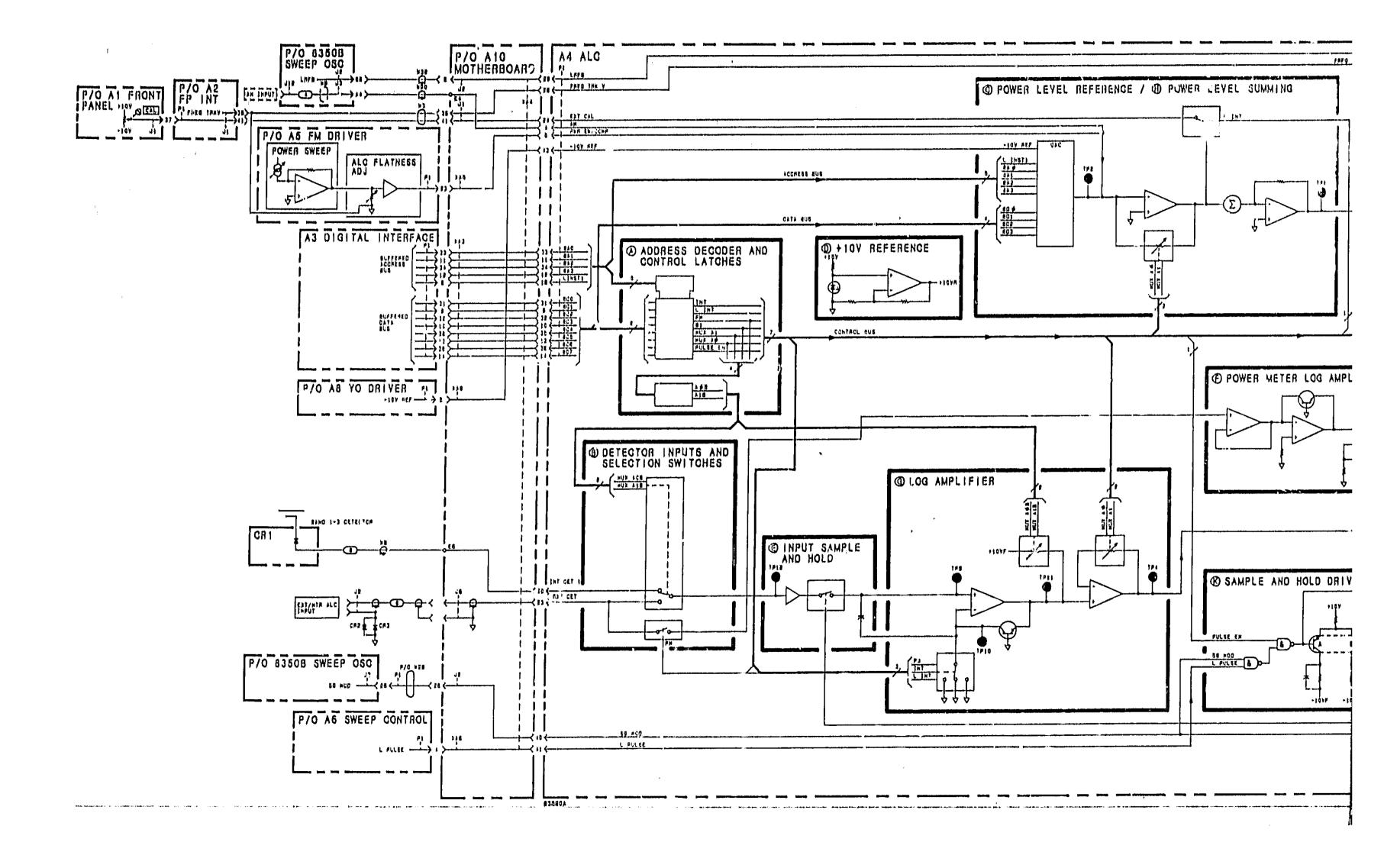
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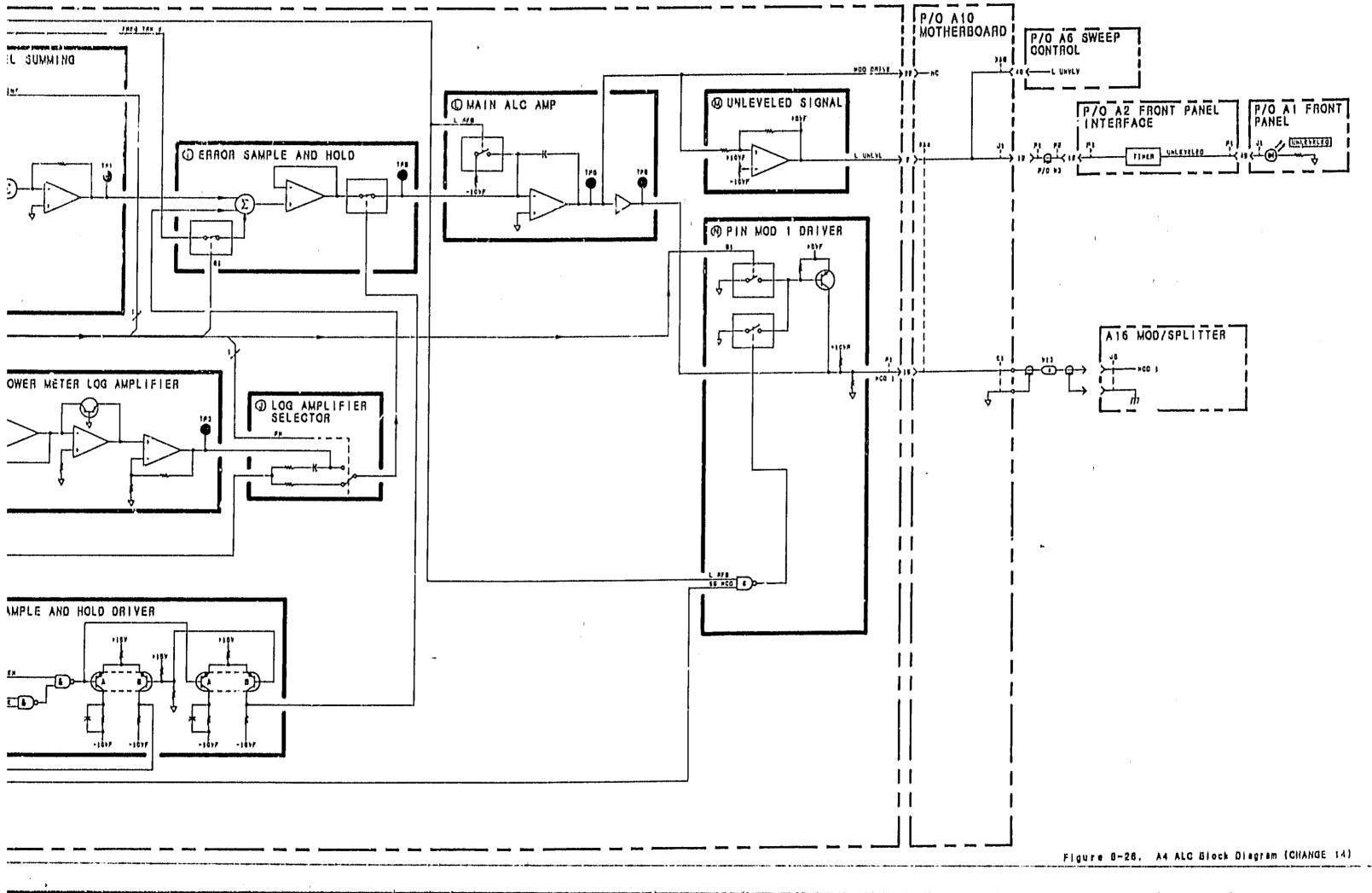
CHANGE 14

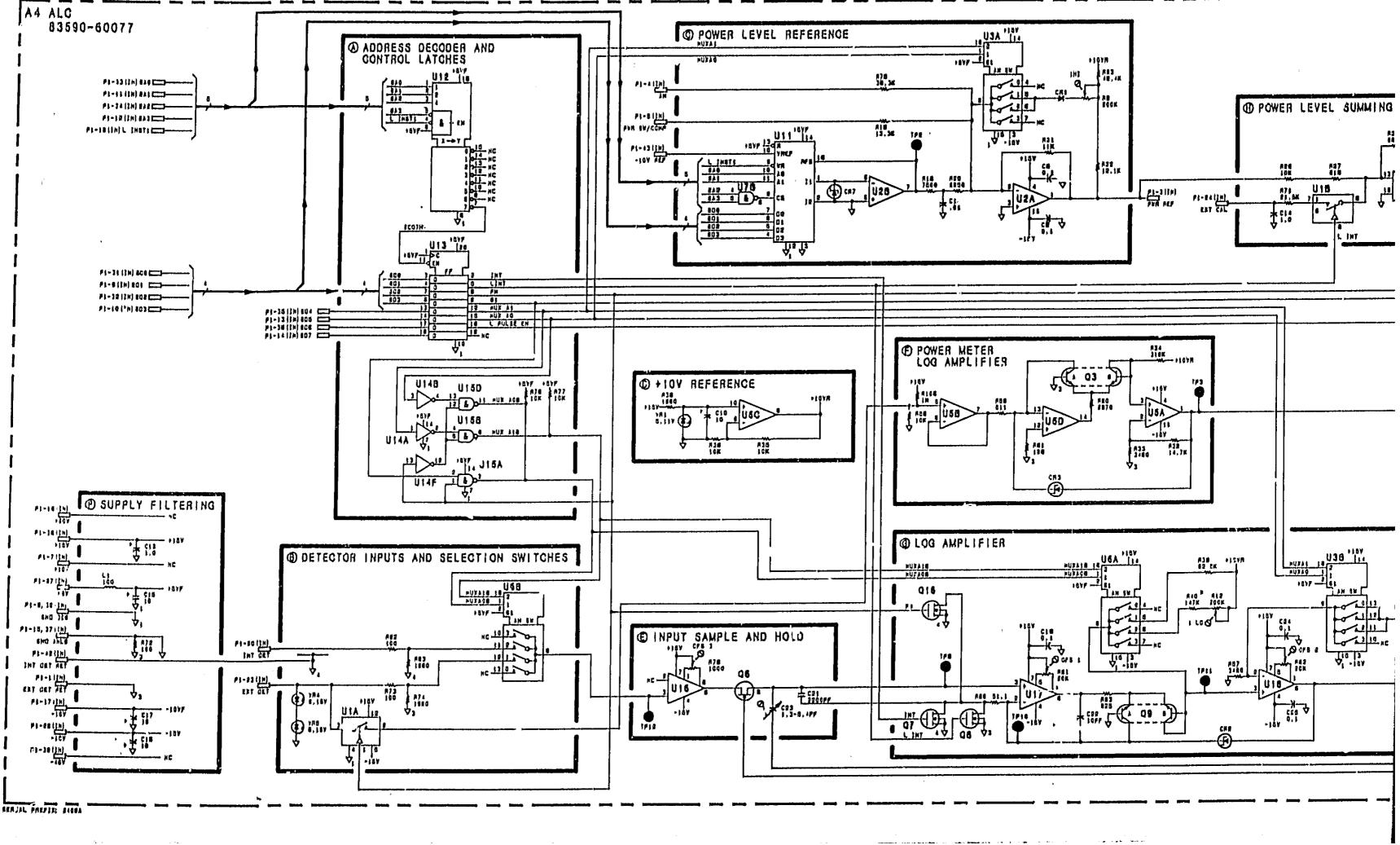
14-39/14-40



### Figure 8-33. Open Loop Waveforms (CHANGE 14)

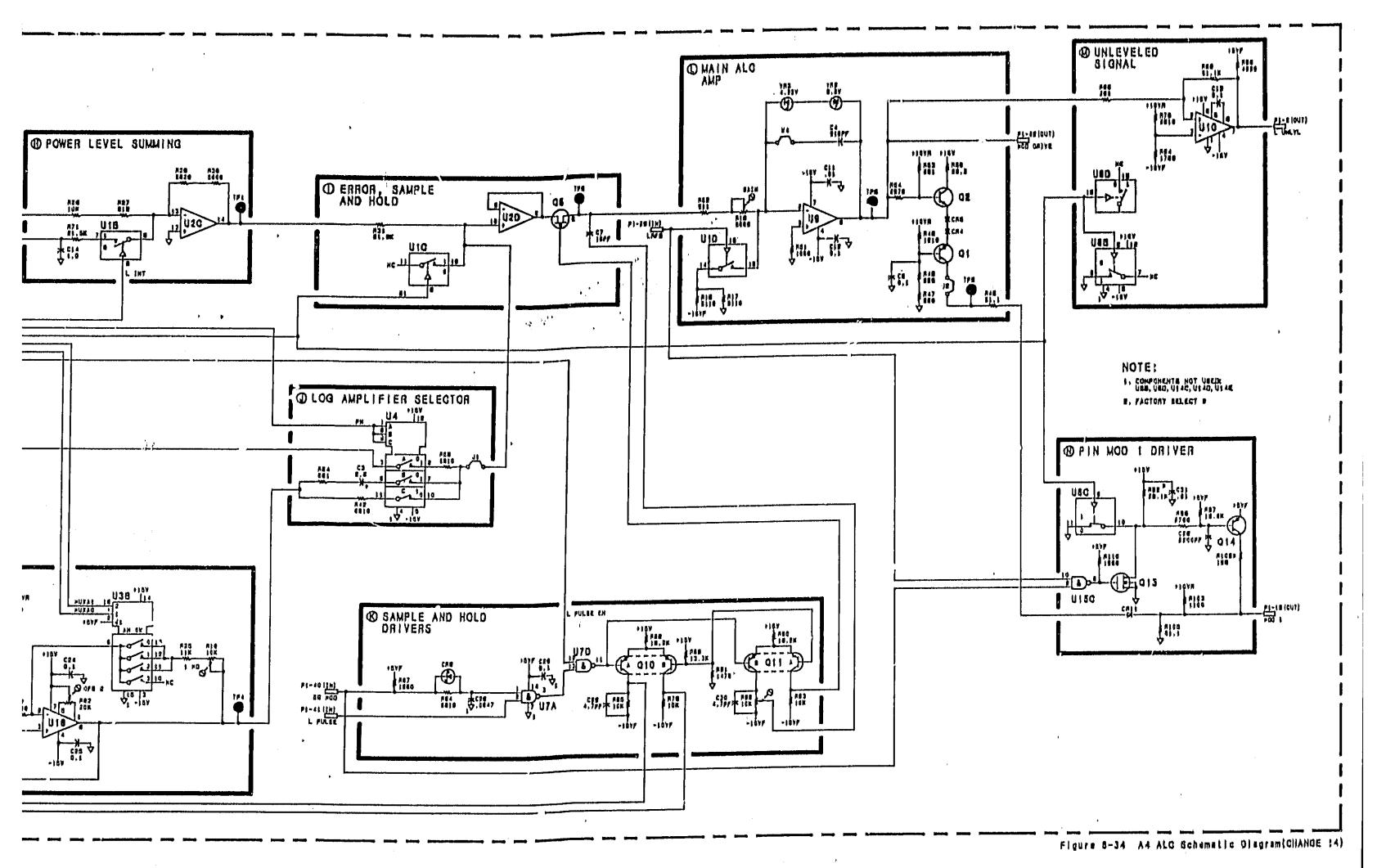






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# OHANGE 15

(Suparzeilas OlIANGE 10)

## This change installs Revision 6 firmware.

Page 6-6, Table 6-3:

Change A3 to HP and Mfr. Part Number 83525-60080 CD 6, DIGITAL INTERFACE ASSEMBLY (does not include A3U) and A3U2).

Change A3UI to HP and Mfr. Part Number 83590-80006 CD 7.

Change A3U2 to HP and Mfr. Part Number 83590-80007 CD 8,

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Page 8-35, Figure 8-23;

Change A3 DIGITAL INTERFACE part number in the top left-hand corner of the schematic to \$3525-60080, Change the SERIAL PREFIX in the bottom left-hand corner of the schematic to 2412A,

CHANGE 15

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#### **OHANGE 16**

This change incorporates modifications to the A2 Sub Panel Board and A7 YTM Driver Board,

Page 6-6, Table 6-3;

Change A2R1 to HP Part Number 2100-3103, CD *,

Page 6-14, Table 6-3;

Change the A7 YTM Driver assembly HP and Mfr. Part Number to 83595-60068, CD 4,

Page 6-15, Table 6-3:

Change A7R52 to: 0698-6358, CD 2, RESISTOR 100K .1% .125W F TC =  $0 \pm 25$ , 28480, 0698-6358, Change A7R64 to: 0698-6977, CD 1, RESISTOR 30K .1% .125W F TC =  $0 \pm 25$ , 28480, 0698-6977, Change A7R65 to: 0757-0438, CD 3, RESISTOR 5.11K .1% .125W F TC =  $0 \pm 100$ , 28480, 0757-0438, Change A7R66 to: 0757-0438, CD 3, RESISTOR 5.11K .1% .125W F TC =  $0 \pm 100$ , 28480, 0757-0438, Change A7R66 to: 0757-0438, CD 3, RESISTOR 5.11K .1% .125W F TC =  $0 \pm 100$ , 28480, 0757-0438, Change A7R66 to: 0698-6362, CD 8, RESISTOR 1K .1% .125W F TC =  $0 \pm 25$ , 28480, 0698-6362, Change A7R68 to: 0698-8469, CD 0, RESISTOR 6.99K .1% .1W F TC =  $0 \pm 4$ , 28480, 0698-8469, Delete A7CR6,

Page 8-63, Figure 8-52 (A7 Component Location*): Delete R68, Change R66 to R68, Change CR6 to R66,

Page 8-63, Figure 8-60 (A7 Schematic):

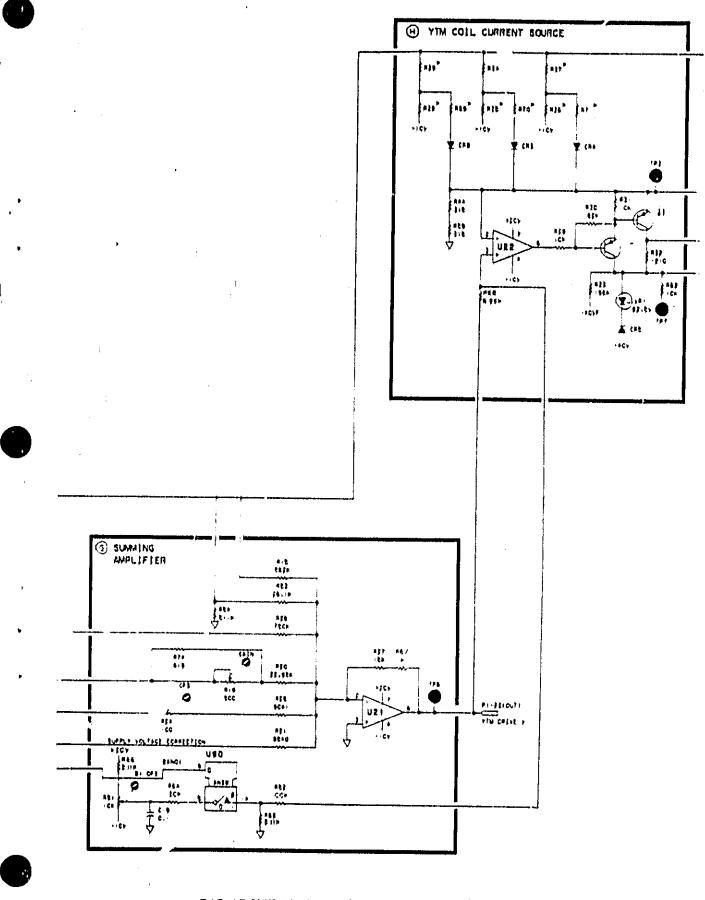
Replace the function blocks © SUMMING / MPLIFIER and H YTM GOIL OURRENT SOURCE with P/O, 47 Y7 / DRIVER SCHEMATIC DIAGRAM (CHANGE 16) in this document.

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Change the part number in the top left-hand corner of the schematic to; 83595-60068, Change the SERIAL PREFIX in the bottom left-hand corner of the page to 2413A.

83590-90005





CHANGE IN

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16-3/16-4

# CHANGE 17

(Supersedes Part Numbers in CHANGE 15)

This change installs Revision 7 firmware,

Page 6-6, Table 6-3;

Change A3U1 to HP and Mfr. Part Number 83590-80010, CD 3, Change A3U2 to HP and Mfr. Part Number 83590-80011, CD 4,

CHANGE 17

17-1/17-2

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#### CHANGE 18

This change documents the increase in range of the sequential-band delay compensation adjustments,

Page 6-15, Table 6-3:

Change A7R42 to HP and Mfr. Part Number 2100-0544, CD 3, RES-TRMR 100K 10%. Change A7R43 to HP and Mfr. Part Number 2100-3611, CD 1, RES-TRMR 50K 10%.

Page 8-63, Figure 8-60;

In block E DELAY COMPENSATION change the following items: A7R42 to 100K

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* A7R43 to 50K



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CHANGE 18

## **OHANGE 19**

This change documents a revision to the Motherboard Assembly and Power Supply Gables.

Page 6-18, Table 6-3: Change A10 to HP and Mfr. Part Number 83595-60078, CD 6,

Page 6-19, Table 6-3: Change Al0J2 to HP and Mfr. Part Number 1251-6952, CD 7, Change Al0J3 to HP and Mfr. Part Number 1251-6343, CD 0,

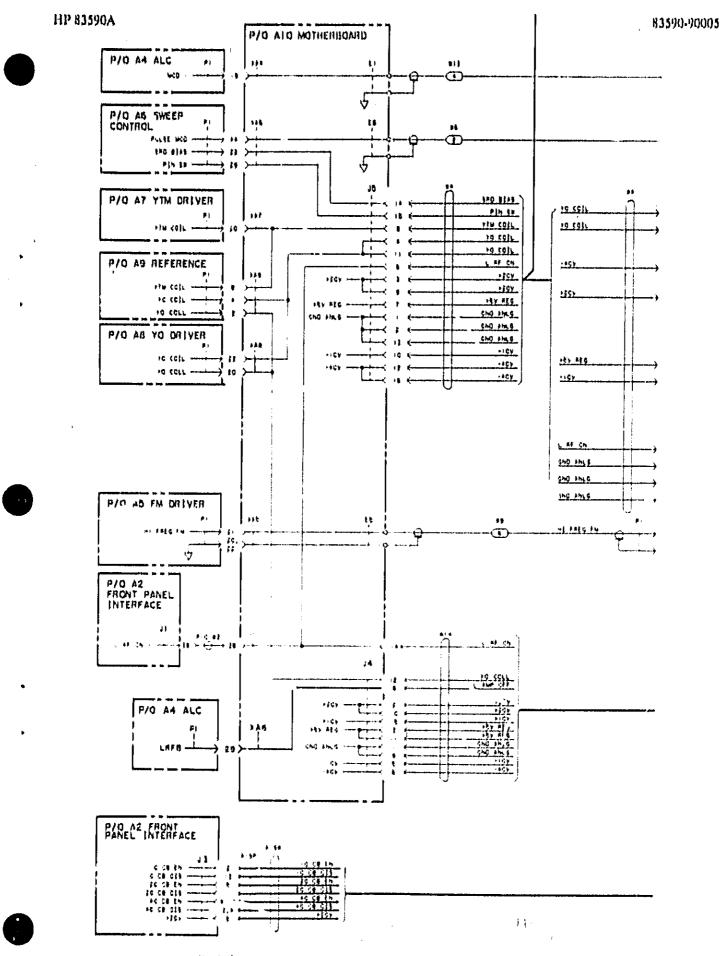
Page 6-22, Table 6-3: Change W28 to HP and Mfr, Part Number 83525-60066, CD 8,

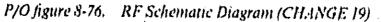
Page 8-75, Figure 8-76, RF Schematic Diagram: Replace left part of Figure 8-76 with P/O Figure 8-76. RF Schematic Diagram (CHANGE 19) in this document,

Page 8-76, Figure 8-79. All Motherboard Component Locations: Replace Figure 8-79 with Figure 8-79. All Motherboard Component Locations (CHANGE 19) in this document.

Page 8-81, Table 8-15. 83590A Motherboard Wiring List (5 of 5): Replace Table 8-15 with Table 8-15. 83590A Motherboard Wiring List (5 of 5) (CHANGE 19) in this document.

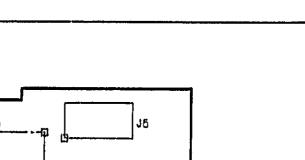
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CHANGE 19

19-3/19-4



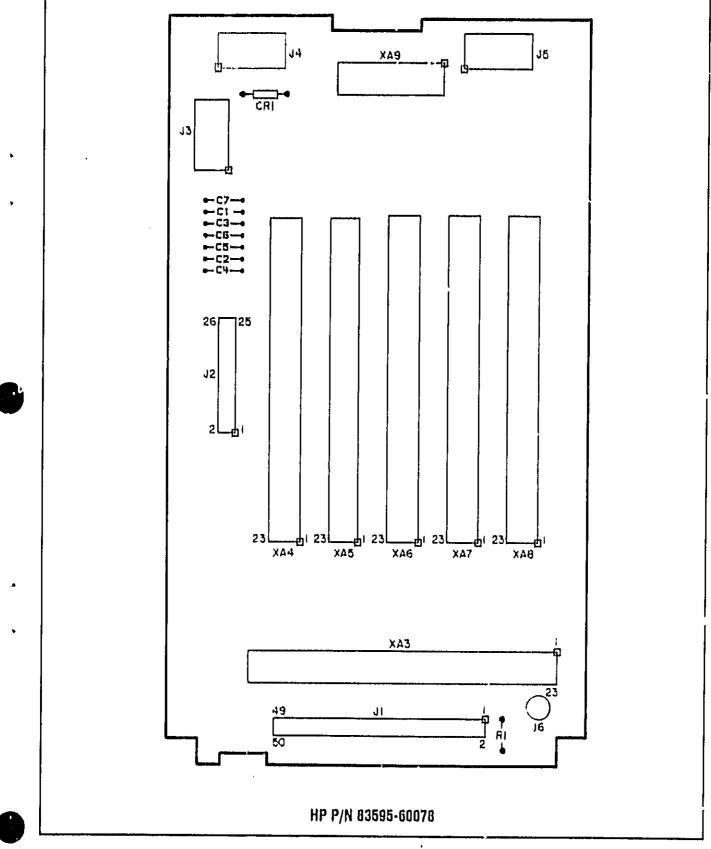


Figure 8-79. A10 Motherboard, Component Locations (CHANGE 19)

CHANGE 19

19-5/19-6

83590-90005

Signal Mnemonic Source		5	Power Supply	   Piup-la	Dig intfe				Sweep	YTM A7P1	УО А8р1	Ref Resistor ABP1	F,P, Interface A10J1	P/O Plug-in Interface A10J2	Power Supply Interface A10J3	YO/YTM Ribbon Cable A10J5	RF Ribbon Cable A10J4	Miscellaneous
	Mnemonic Description		Interface P2	A3P1	AJI	FM A5P1		Control AGP1										
+20V +20V RET +20V RET SENSE +20V SENSE	P1+7 P1+14 , P1+6 P1+16	+20V Regulated +20V Return +20V Return Sense +20V Sense	7 14 6 15				16	16		16	16	3,11	42		7 14 6 15	3,9	2,10	C7
+15V	P2-29	+15V Regulated		29			30	ЗB	36	38	38			15				CG
+10V +/10V RET	P1-0 P1-3, 16	+10V Regulated +/10V Return	6 3, 16				7	7	7	7	7		40		8 3,6		16	C5
+6V +5VA +5VB +6V REG +6V UNRFG	A3P1+6,7 P2+30 P2+18,60,51 A9P1+7 P2+63	+5V Internal for RF Plug-In +5V for 0350A +5V for RF Plug-In +5V Regulated +5V Unregulated		30 18,60,61 63	6,7	, 35,36,38	27	27	27	27	27	7 12	2	18,20		7	3,11	C4
-10V -10V RET SENSE -10V SENSE -10V UNREG	P1-13 P1-12 P1-4 P1-6	–10V Regulated –10V Return Sense –10V Sense –10V Unregulated	13 12 4 5				17	17	17	17	17		40	;	13 12 4 5	10	Б	C3
-15V	P2-2B	-15V Regulated		28			28	28	28	28	28			13				C2
-40V -40V RET -40V RET SENSE -40V SENSE	P1+11 P1+1 P1+10 P1+2	-40V Regulated -40V Return -40V Return Sense -40V Sense	11 1 10 2				6,39			6,39	6,39				11 1 10 2	12,16	6	CI
GND ANLG	W28P1-8 P2-27,68,69	Analog Ground					15,37	15,37	37,41 43	15,10, 24,26, 29 37	15,19, 24,26, 29,37	6	48	10,11, 12,24	10,12,14 16,1,3,6	1,2 13	1,9	C1-C7, R1
סום מאס	P2-1,6,14, 16,21,31, 37,46,48 49	Digital Ground		1,6,14, 16,21,31, 37,46,48, 49	4,5		B,30	8,30	B,30	B,30	B,30	5	ß		•			R1
GND SENSE	W28P1-4	Analog Ground Sense													4			

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l 1 Coaxial Cable

² Shielded Cable

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* Not used on this assembly

 Table 8-15.
 83590A Motherboard Wiring List (5 of 5)
 (CHANGE 19)

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This change documents a replacement kil and an exchange replacement kil for the Power Amplifier Assembly,
Page 6-2, Table 6-1; Change A14 New Part Number to 83592-60113, Rebuilt Part Number to 83592-60114, Description to Power A 2.3 to 7.0 GHz Kit.
Page 6-20, Table 6-3; Change A14 to HP and Mfr. Part Number 83592-50113, CD 7, POWER AMPLIFIER KIT, Change A14 to HP and Mfr. Part Number 83592-60114, CD 8, EXCHANGE POWER AMPLIFIER KIT.
Page 6-20, Table 6-3;
Change Al4AlC4 to HP part number 0180-0228, 22ufd 15V CD 5,
Add A14A1C9 HP part number 0160-4084, .lufd 50V CD 8,
Add Al4AICR1 and Al4AICR2 HP part number 1901-0033, 180V 2A CD 2,
Change A14A111 to HP part number 1200-0482 CD 5.
Change Al4AIMPI to HP part 5021-5320 CD 8.
Change Al4AIMP3 to HP part number 1251-3172 CD 4. Change Al4AIMP5 to HP part number 1200-0173 CD 5.
Add Al4AlQ3 HP part number 1854-0477 CD 7.
Add A14A1Q4 HP part number 1853-0281 CD9.
Page 6-21, Table 0-3;
Add A14A1R32 HP part number 0698-7253 5.11K 1% .05W CD 0,
Add A14A1R33 HP part number 0698-7284 100K 1% .05W CD 5.
Add A14A1R34 HP part number 0698-7270 26.1K 1% .05W CD 9.
Add A14A1R35 HP part number 0698-7243 1,96K 1%,05W CD 6.
Add A14A1R36 HP part number 0698-7234 825 1%,05W CD 5,
Add Al4A1R37 HP part number 0698-7257 7.5K 1%,05W CD 2. Add Al4A1R38 HP part number 0698-3438 147 1%,12W CD 3.
Add A14A1R39 HP part number 0698-7284 100K 1% ,05W CD 5.
Add A14A1R40 HP part number 0698-3440 196 1%,12W CD 7.
Add Al4AlU2 HP part number 1826-1058 CD 3.

Page 8-75, Figure 8-76;

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Replace blocks AI4AI and AI4 with P/O Figure 8-76. RF Schematic Diagram (CHANGE 20), Change Serial Prefix on bottem left corner to 2507A.

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CHANGE 20

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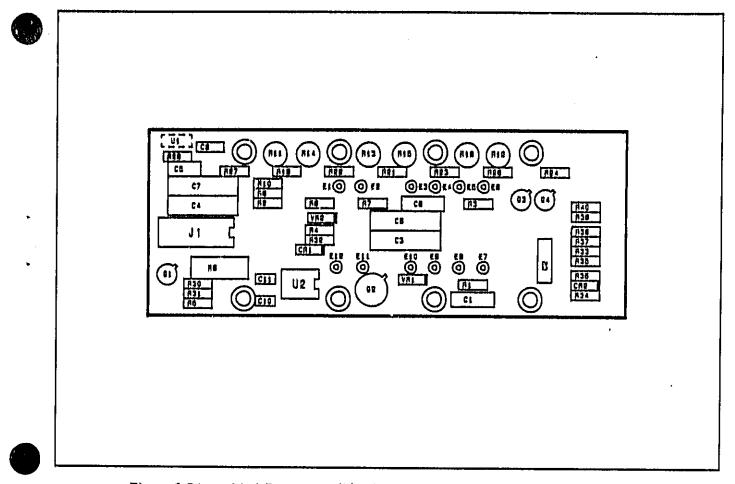
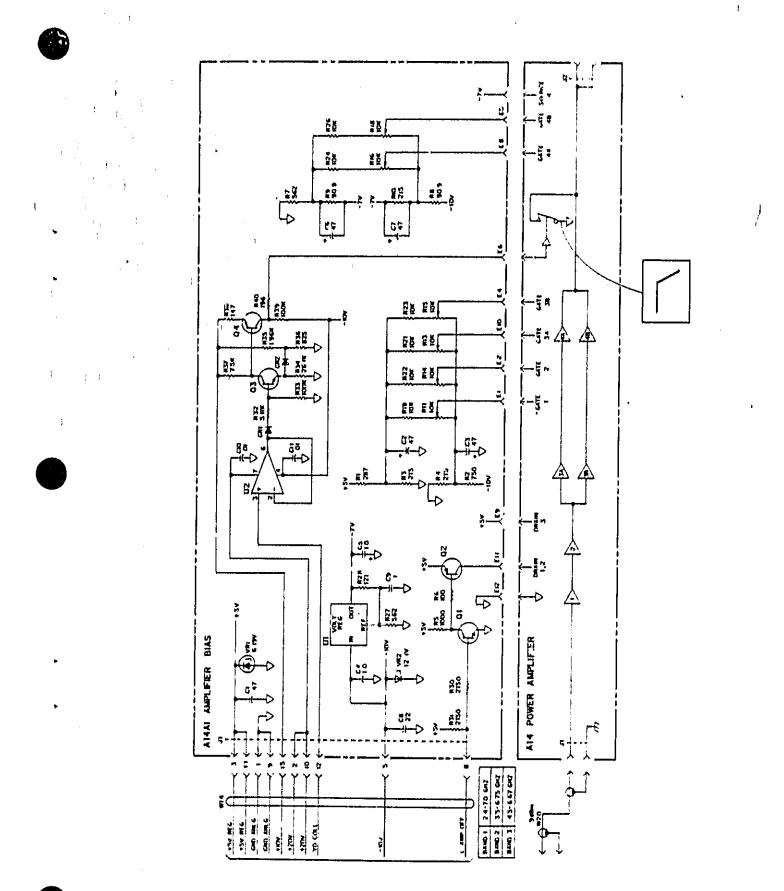


Figure 8-74. Al4Al Power Amplifier Bias, Component Locations (CHANGE 20)

83590-90005



P/O Figure 8-76. RF Schematic Diagram (CHANGE 20)

CHANGE 20

20-5/20-6

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## **CHANGE 21**

# This change documents a modified A6 Sweep Control Assembly, (Supersedes Change 12)

Page 6-12, Table 6-3;

Replace All the information shown for A6 with P/O Table 6-3, Replaceable Parts (CHANGE 21) (1 of 3) in this document.

Page 6-13, Table 6-3;

Replace All the information shown for A6 with P/O Table 6-3. Replaceable Parts (CHANGE 21) (2 of 3) in this document.

Page 6-14, Table 6-3;

- Replace All the information shown for A6 with P/O Table 6-3. Replaceable Parts (CHANGE 21) (3 of 3) in this document.
- Page 8-57, Figure 8-44. A6 Sweep Control Component Locations: Replace Figure 8-44 with Figure 8-44. A6 Sweep Control Component Locations (CHANGE 21) in this document.

#### Page 8-57, Figure 8-49, A6 Sweep Control Schematic Diagram:

Replace Figure 8-49 with Figure 8-49. A6 Sweep Control Schematic Diagram (CHANGE 21) supplied in this document.

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Reference Designation	HP Part Number	00		Description	Mir Code	Mir Part Numbe
A6	83550-60106	6	1	BOARD ASSEMBLY-SWEEP CONTROL	2B400	
A6C1- A6C4 A8C5 A6C5 A6C5	0160-2617 0160-2617		2	NOT ASSIGNED CAPACITORIEXO 6.8UF++10% 38VDC TA CAPACITORIEXO 8.8UF++10% 38VDC TA	68289 66289	1600665X603862 1600666X603862
ASC7 ASC8 ASC9 ASC10 ASC11	0180-2815 0180-0228 0180-0228	1	1	CAPACITOR-FXD 100UF++20% 10VDC TA NOT ASSIGNED CAPACITOR-FXD 22UF++10% 16VDC TA CAPACITOR-FXD 22UF++10% 16VDC TA CAPACITOR-FXD 22UF++10% 16VDC TA NOT ASSIGNED	20480 68289 66289	0180.6818 16002262801682 16002262801682
A6C12 A6C13 A6C14 A6C15 A6C15	3140-3878 C160-0673 0160-3878	6 2 5	6 1	NOT ASSIGNED NOT ASSIGNED CAPACITOR-FXD 1000PF + 20% 100VDC CER CAPACITOR-FXD 1000PF + 20% 100VDC CER CAPACITOR-FXD 1000PF + 20% 100VDC CER	28480 28480 F6480	0160-3678 0160-0573 016C-3078
A6C17 A6C18 A6C19 A6C20 A6C21	0160-3878 0160-0678 0160-3878 0160-3878 0160-4084	6 4 6 8	2	CAPACITOR,FXD 1000PF +-20% 100VDC CER NOT ASSIGNED CAPACITOR,FXD .047UF +-20% EQVDC CER CAPACITOR,FXD 100PF +-20% 100VDC CER CAPACITOR,FXD 1UF +-20% 50VDC CER	28480 28480 28480 28480	0160-3878 0160-3875 0160-3878 0160-4864
ABG22 ABG23 ABG24 ABG26 ABG26 ABG26	0160-4084 0160-3879 0160-3878 0160-3878 0160-3878	87766	2	CAPACITOR-FXD.1UF +20% 50VDC CER CAPACITOR-FXD.01UF +20% 100VDC CER CAPACITOR-FXD.01UF +20% 100VDC CER CAPACITOR-FXD.100PF +20% 100VDC CER CAPACITOR-FXD.1000PF +20% 100VDC CER	28480 28480 28480 28480 28480	0160.4004 0160.3070 0160.3070 0160.3070 0160.3070
A6C27 A6C28	0160-0675		1	CAPACITOR FXD .04TUF + 20% EQVDG CER CAPACITOR FXD 10PF + EPF 200VDG CEP	164.60 264.60	0160-0678
AGCR1 AGCR2	1901-0535	9	3	DIODE-5M EIG SCHOTTKY DIODE-5M EIG SCHOTTKY	28400 28400	1901-0535
A6CR3 A6CR4 A6CR5 A6CR5 A6CR5 A6CR7	1901-0535 1901-0050 1901-0050 1901-0050 1901-0050	8 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	7	DIODE-SM SIG SCHOTTKY DIODE-SMITCHING EQV 200MA ENS DO-35 DIODE-SWITCHING EQV 200MA ENS DO-35 DIODE-SWITCHING EQV 200MA ENS DO-35 DIODE-SWITCHING EQV 200MA ENS DO-35	28480 20460 28480 28480 28480 28480	1501-0635 1601-0050 1601-0050 1601-0050 1501-0050
A6CIT8 A6CIT8 A6CIT8 A6CIT10 A6CIT12	1901-0050 1901-0050 1901-0050			NOT ASSIGNED NOT ASSIGNED DIODE-SWITCHING BOV 200MA 2NS DO-35 DIODE-SWITCHING BOV 200MA 2NS DO-36 DIODE-SWITCHING BOV 200MA 2NS DO-36 DIODE-SWITCHING BOV 200MA 2NS DO-36	28400 28400 28400 28400	1801.0050 1801.0050 1801.0050
ASCR13	1801-0033	2	1	DIODE-GEN PRP 180V 200MA DO-7	28480	1001+0033
4611 4612 4613	9140-0137 9140-0137 08503-80001	8	2	INDUCTOR RF-CH-MLD IMH 6% 2DX A6LG 0+60 INDUCTOR RF-CH-MLD IMH 6% 2DX A6LG G-60 COIL-TORCID	26460 28460 26400	8140-0137 8140-0137 06603-60001
лемрі Лемрі Лемрі	6040-6648 6000-9043 9360-0124	8 5 7	1	EXTRACTOR P.C. BOARD BLUE PN-P.C. BOARD EXTRACTOR CONNECTOR-SGL CONT PIN 04-IN-BSC-52 RND	28480 28480 28480	8040.6849 8000.9043 0360.0124
NGC1 NGC2 NGC3 NGC4 NGC5	1855-0423 1854-0477 1855-0423 1854-0019 1853-0405	07078	1212	TRANSISTOR MOSFET N-CHAN E-MODE TRANSISTOR NPN 202222A SI TO-18 PO+500MW TRANSISTOR MOSFET N-CHAN E-MODE TRANSISTOR NPN SI TO-18 DO-350MW TRANSISTOR PNP SI PO-300MW FT+850MHZ	17856 04713 17858 28480 04713	VN10KM EN2222A VN10KM 1654-0019 EN4200
6C8 6C7 6C8 6C9 6C9 6C10	1853-0405 1855-0423 1854-0404 1854-0477 1853-0281	9 5 0 7 8	8 1	TRANSISTER FNP SI PD-JOOMW FT-BEOMHZ TRANSISTOR MOSFET N-CHAN E-MOCE TRANSISTOR NPN SI TO-18 PD-JEOMW TRANSISTOR NPN 2N2222A SI TO-18 PD-600MW TRANSISTOR PNP 2N2807A SI TO-18 PD-400MW	04713 17866 28480 04713 04713	ENAE00 VN10KM 1654.0404 EN2222A EN2607A
6011 6012	1854-0809 1854-0809	ß	2	TRANSISTOR NPN 2N2368A 61 TO-18 PD-360MW TRANSISTOR NPN 2N2368A 51 TO-18 PD-360MW	28400 28400	1854-0809 1854-0809
6A) 6R2				NOT ASSIGNED NOT ASSIGNED		
673 674 676 676 677	0787.0260 0787.1094 0698-3446	1	3	NOT ASSIGNED NOT ASSIGNED RESISTOR 1X 1%, 126W F TC=0++100 RESISTOR 1 ATK 1% 125W F TC=0++100 RESISTOR 133 1%, 125W F TC=0++100	24846 24846 24846	C4.1,8.T0.1001.F C4.1,8.T0.1471.F C4.1/8.T0.383R.F
678 679 6710 6711 6712	0757-0401 0658-7260 0698-7267 0688-7283 2100-1738	C 7 4 4 9		FEDISTOR 100 1% .126W F TC=0+.100 FEDISTOR 10K 1% .06W F TC=0+.100 FEDISTOR 19.5K 1% .06W F TC=0+.100 FEDISTOR B0.5K 1% .06W F TC=0+.100 FEDISTOR-TRMR 10K 10% C TC=0.4.100 FEDISTOR-TRMR 10K 10% C TC=0.4.00 1.TRN	24546 24546 24546 24546 24546	C3-1/8-T0-101.F C3-1/8-T0-1002.F C3-1/8-T0-1962.F C3-1/8-T0-80082.F

# PIO Table 6.3 - Ronlaceable Power (CILINGE )IV (1 of )



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Reference Designation	HP Part Number	0	aiy	Description	Mir Gode	Mir Part Number
A6(7) 3 A6(7) 4 A6(7) 6 A6(7) 6 A6(7) 6 A6(7) 7	0757.0442 0757.0280 0658.8469 2100.3756 0658.6459	81080 000	3 8 1	REDISTOR IOK 1% .128W F TC=0+-100 REDISTOR IN 1% .126W F TC=0+-100 REDISTOR 8.9% .1% .126W F TC=0+4 REDISTOR .5% .1% .1% C SIDE.ADJ 17-TRN REDISTOR 6.99% .1% .1W F TC=0+4	24548 24648 26400 26400 26400 26400 26400	C4.1/0.70.1002.F C4.1/0.70.1001.F 0690.0469 2100.37b0 0696.0469
A6710 A6719 A6720 A6721 A6722	0090-8469 0698-8469 0699-0642 2100-3767 0609-0031	00768		REGISTOR 6.664	58480 59480 58480 58480 58480 28480	0680.0469 0680.8469 2679.0542 2100.1167 2100.1167
A6723 A6724 A6726 A6726 A6726 A6727	6699.0833 2100-3732 0688.0933 2100-3732 6689.6834	97970	2	REDISTOR 27.382K.1%.1W FTC=0+-5 REDISTOR-TRIMF.600.10% C 6IDE-ADJ 17-TRN REDISTOR-TRIMF.1%.1W FTC=0+-5 REDISTOR-TRIMF.600.10% C 6IDE-ADJ 17-TRN REDISTOR 35.660K.1%.1W FTC=0+-5	20480 26460 28460 28460 28460	0666.0933 2100.3732 0669.0933 2100.3732 0669.0934
Абгі20 Абгі20 Абгі30 Абгі31 Абгі32	2100-1732 0698-8469 0698-8469	7	1	RESISTOR-TRIMR 600 10% C SIDE-ADJ 17-TRN NOT ASSIGNED NOT ASSIGNED RESISTOR 6.89K .1% .1W F TC-0+4 RESISTOR 6.89K .1% .1W F TC-0+4	26480 26480 76460	2100-3732 0658-6465 0688-6465
A6H]] A6H]4 A6H]6 A6H]6 A6H]7	0696-0469 2100-3785 0698-0469 0698-0469 0698-0627 2100-3760	04048	1 2	REDISTOR 6.99K 1% 1W FTC-0.4 REDISTOR JAM 80 10% C BIDE, ADJ 17.TEN REDISTOR 6.99K 1% 1W FTC-0.4 REDISTOR 6.99K 1% 12W FTC-0.4 REDISTOR 1M 1% 12W FTC-0.4 REDISTOR JTRM 20K 10% C BIDE.ADJ 17.TEN	20100 20400 20400 20400 20400 20400 20400	0664.8469 2100-1785 0658.0469 0658.027 2100-3750
AER18 AER19 AER40 AER41 AER42	0698-0827 0699-0154 0699-0154 0698-6867 0787-0442 0698-3260	4 6 9 9	2	RESISTOR 1M 1% .126W F TC=0+.100 RESISTOR 7.2K .1% .126W F TC=0+.26 RESISTOR 7.2K .25% .126W F TC=0+.20 RESISTOR 16K 1% .126W F TC=0+.100 RESISTOR 464K 1% .126W F TC=0+.100	20480 20480 26460 24646 28460 28646	0698-0827 0698-0164 (6698-608 C4-1/8-TC-1002-F 0699-3260
аспа 3 Аспаа Аспаа Аспаб Аспаб Аспа 7	0668-3160 0757-0442 0688-3260 0688-3260 0767-0421	5 9 5 4	2 R	RESISTOR 2.37% 1% .125W F TC=0+100 RESISTOR 10K 1% .125W F TC=0+100 RESISTOR 464K 1% .125W F TC=0+100 RESISTOR 2.37K 1% .125W F TC=0+100 RESISTOR 225 1% .125W F TC=0+100	24546 24546 26480 24546 24546 24546	C4.1/8.T0.2371.F C4.1/8.T0.1002.F 0688-3260 C4.1/8.T0.2371.F C4.1/8.T0.2371.F C4.1/8.T0.825R.F
лепля Лепля Лепго Лепго Лепго	0767.0421 C680.3447 O656.3440 O688.7212 C690.0064	4 4 7 8 8	1	RESISTCR 828 1% ,125W F TC=0+100 RESISTOR 422 1% ,125W F TC=0+100 RESISTOR 186 1% ,125W F TC=0+100 RESISTOR 186 1% ,125W F TC=0+100 RESISTOR 8,15K 1% ,125W F TC=0+100	24546 24543 24546 24546 24546 24546	C4-1/8-T0-826R.F C4-1/8-T0-422R.F C4-1/8-T0-186R.F C3-1/8-T0-100R.F C4-1/8-T0-2181.F
Аблај Аблај Аблај Аблаб Аблаб Аблаб	C658.3425 C658.463 C658.463 C658.6827 C658.3168 C658.3266	22400	¦ ¦	RESISTOR 19.6 14.126W F TC-0+100 RESISTOR 19.6 14.126W F TC-0+100 RESISTOR 11.126W F TC-0+100 RESISTOR 26.14 14.126W F TC-0+100 RESISTOR 25.14 14.126W F TC-0+100	03668 24646 26460 24646 24646 24646	PMC68.1/8.T0.19R6.F C4.1/8.T0.1863.F C680.8827 C4.1/8.T0.2812.F C4.1/8.T0.2373.F
AERE0 AERE9 AERE9 AERE0 AERE1 AERE2	0767.0280 6690.7236 6668.7277 6668.7277 6767.0468	27 6 7	† 2	RESISTOR 1K 1% .125W F TC+0++100 RESISTOR 1K 1% .05W F TC-0++100 RESISTOR 51.1K 1% .05W F TC-0++100 RESISTOR 51.1K 1% .05W F TC+0++100 RESISTOR 51.1K 1% .125W F TC+0++100	24546 24546 24545 24545 24545 24546	C4-1/8-T0-1001,F C3-1/8-T0-1001,F C3-1/8-T0-5112,F C3-1/8-T0-5112,F C4-1/8-T0-5112,F
AER43 AER44 AER66 AER66 AER67	2100.2030 C658.7260 C658.7272 C658.7272	5 7 1 6	י ן	RESISTCR.TRMR 20K 10% C TOP.ADJ 1.TRN RESISTCR 10K 1% 05W F TC=0100 NOT ASSIGNED RESISTCR 31 6K 1% 05W F TC=0100 RESISTCR 5.11K 1% 05W F TC=0100	73138 24646 24646 24646	62PP2CK C3-1/8-T0-1002.F C3-1/8-T0-3162.F C3-1/8-T0-5111.F
АЄПЕВ Аепев Аепто Аеп70 Аеп71 Аеп72	2100-2516 2100-2516 C688-7237 C688-7242	3	2	REDISTOR TRAIN 100K 10% C SIDE, ADJ 1.TRN REDISTOR TRAIN 100K 10% C SIDE, ADJ 1.TRN NOT ASSIGNED RESISTOR 1.1K 1% 00W F TC-0+100 RESISTOR 1.7K 1% CEW F TC-0+100	12887 12887 24646 24646	3226W-1-104 3328W-1-104 C3-1/8-T0-1101-F C3-1/8-T0-1781-F
леп73 Леп74 Леп76 Леп76 Леп76 Леп77	2100.2521 2100.2521 CEGE-7263 0558-7285	004	2	RESISTOR.TRMR # 10% C BICE.ADJ 1.TRN RESISTOR.TRMR # 10% C BICE.ADJ 1.TRN NOT ASBIGNED RESISTOR 110K 1% 06W F TC=0100 RESISTOR 110K 1% 06W F TC=0100	20903 20903 24546 24546	ETE0x202 ETE0x202 C3.1/8.T0.40092.F C3.1/8.T0.1103.F
ACA78 ACA78 ACA07 ACA07 ACA07 ACA07 ACA07 ACA07 ACA07 ACA07 ACA07 ACA07 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78 ACA78	2100.2692 C689.7243 C688.3162 C688.7260 C688.7260 C688.7243	67876	1	REBISTOR-TRMR IM 20% C SIDE-ADJ 1-TRN RESISTOR 1.96K 1% .06W F TC-0+.100 RESISTOR 2.46K 1% .128W F TC-0+.100 RESISTOR 10K 1% .06W F TC-0+.100 REBISTOR 1.56K 1% .06W F TC-0+.100	1098] 28460 24546 24546 24546	ET60X105 C609.7243 C4.1/8-T0.3481.F C3.1/8-T0.1022.F C3.1/8-T0.1081.F
АСПОЈ Аспој Аспој Аспој Аспој Аспој	C668.7210 C668.7210 C658.7260 C658.7260 C658.7260 C659.7260	E 0 7 7 7	1	FEGISTCR 1.78K 1% CEW F TC=0100 FEGISTCR 1 21K 1% CEW F TC=0100 FEGISTCR 1 21K 1% CEW F TC=0100 FEGISTCR 1CK 1% CEW F TC=0100 FEGISTCR 10K 1% CEW F TC=0100	24546 24546 24546 24546 24546 24546	C).1/8.T0.1781.F C).1/0.T0.1211.F C).1/8.T0.1002.F C).1/8.T0.1002.F C3.1/8.T0.1002.F
467P) 467P2 467P3 467P4	1261-4672 1261-4672 1261-4672 1261-4672		10	Connector Io.Pin M Post Type Connector Io.Pin M Post Type Connector Io.Pin M Post Type Connector Io.Pin M Post Type	78400 28400 20400 26400 26400	1281-4672 1281-4672 1281-4672 1281-4672

# P/O Tuble 6-3. Replaceable Parts (CHANGE 21) (2 of 3)

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CHANGE 21

21-5

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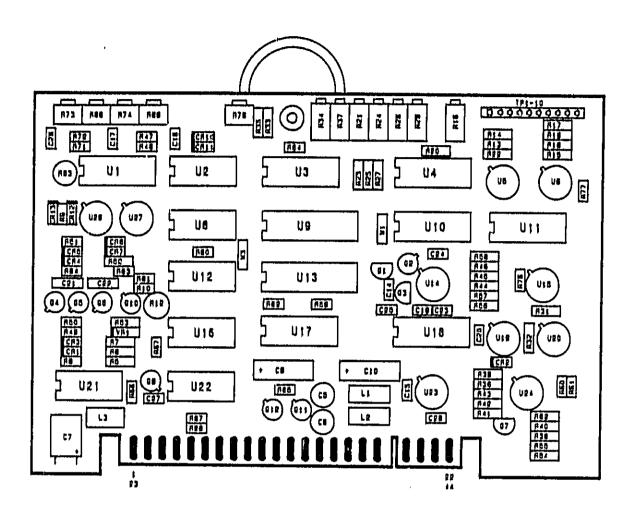
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Referance Designation	HP Part Number	CD	aty	Description	Mir Code	Mir Part Number
A6TP6 A6TP6 A6TP7 A6TP9 A6TP9	1261-1672 1251-1672 1251-1672 1251-1672 1251-1672 1251-1672 1261-1672	4		CONNECTOR 10-PIN M POST TYPE CONNECTOR 10-PIN M POST TYPE CONNECTOR 10-PIN M POST TYPE CONNECTOR 10-PIN M POST TYPE CONNECTOR 10-PIN M POST TYPE	26460 26460 26460 26460 26460 26460	1261.4672 1261.4672 1261.4672 1261.4672 1261.4672 1261.4672
A6TP10 A6U1 A6U2	1281-4672 1826-0720 1820-3211		2	CONNECTOR 10-PIN M POST TYPE IC SWITCH ANLG GUAD 16-DIP-C PKG IC GATE TTL LS EXCL-OR GUAD 2-INP	29480 06865	1251-4672 5W-02FO
AGUS Agua Agua Agua Agua Agua	1020-1196 1026-0720 1026-0471 1028-0471 1028-0471 1020-1112	0 + 22	1 5 2	IC FF TTL LE D-TYPE POS-EDGE-TRIG COM IC SWITCH ANLG OUAD 16-DIP-C PKG IC CP AMP LOW-DIRFT TO-89 PKG IC OP AMP LOW-DRIFT TO-89 PKG NOT ASSIGNED K FF TTL LE D-TYPE POS-EDGE-TRIG	01295 01295 06665 20490 20490 20490 01295	SN74LS08N SN74LS174N SW.02FO 1026-0471 1028-0471 EN74LS74AN
AGUS AGUIO AGUI2 AGUI3	1020-1730 1020-1100 1026-1100 1020-1102 1020-1112 1020-2024	6 8 9 9 1	1 2 1	C FF TTL LS D-TYPE POS.EDGE.TRIG COM ANALOG SWITCH & SPST IU -CERDIP ANALOG SWITCH & SPST IS -CERDIP ANALOG SWITCH & EPST IS -CERDIP C FF TTL LS D-TYPE POS-EDGE.TRIG C DRVR TTL LS LINE DRVR OCTL	01295 25480 53480 01295 01295	SN74L5273N 1826-1186 1826-1885 SN74L524AN SN74L524AN
NEU14 NEU16 NEU16 NEU17 NEU10	1826-0026 1826-0471 1820-1246 1820-1216 1820-1218 1828-0752	12872	2	IC COMPARATOR PRCN TO.58 FKG IC OP AMP LOW DRIFT TO.58 FKG IG GATE TTL LS AND OUAD 21MP IC DCDR TTL LS J.TO.8-LINE J.INP IC DCDR TTL LS J.TO.8-LINE J.INP IC DCNV 12:0-D/A 18-DIP.C FKG	01296 28400 01295 01295 24365	LM311L 1026-0471 EN74L506N SN74L512CN AD7642CD
6018 6020 6021 6022 6023	1826-0471 1826-0471 1820-1202 1820-197 1826-0646	22783	1	K op amp low.orift to.89 pkg K op amp low.orift to.89 pkg K gate ttl ls nand tpl J.inp K gate ttl ls nand ouad 2.inp K comparator prcn to.89 pkg	26400 26400 01295 01295 01295	1826-0471 1826-0471 SN74LS10N SN74LS00N LM311L
6U24 6U26 6U26 6U27	1826-0092 1826-0185 1826-0915	1 8 9	1 1 1	IC OP AMP GP DUAL TO-89 PKG NOT ASSIGNED IC OP AMP SPCL TO-98 PKG IC OP AMP LOW-BIAS-H-IMPD B-DIP-C PKG	28480 JL685 01285	1628-0092 CA3060 TL071ACJG (PER HP DWG)
6VR1 6W1	1902-3002	2	1	DIODE-2NR 2.37V 5% DO-7 PD= AW TC=- 074%	26460	1802-3002
6W2 6W3	8159-0005	0	2	RESISTER-ZERO OHMS 22 AWG LEAD DIA NOT ASSIGNED NOT ASSIGNED	£6480	6125.0005

# P/O Table 6-3. Replaceable Parts (CHANGE 21) (3 of 3)

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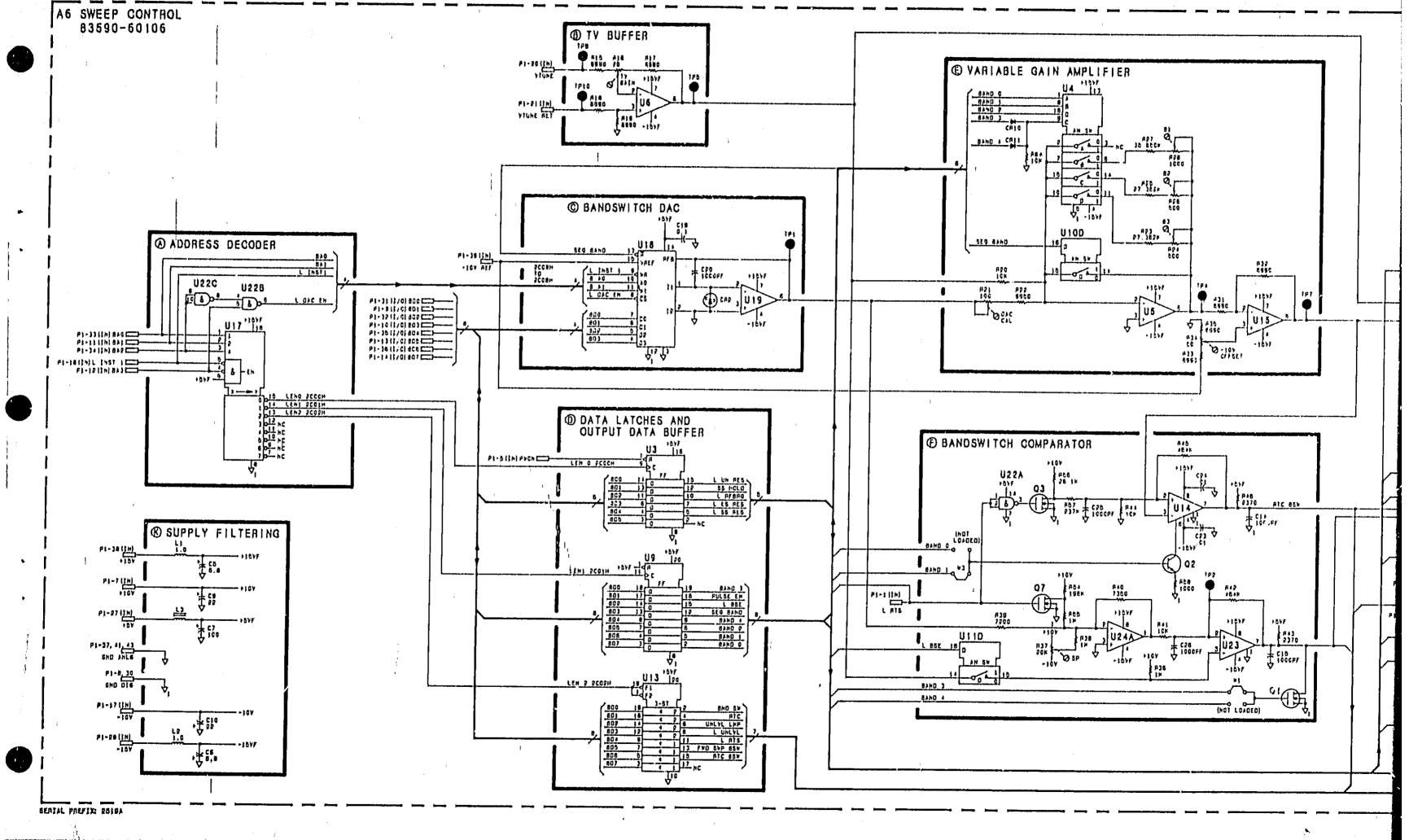
CHANGE 21



HP P/N 83590-60106

Figure 8-44. .46 Sweep Control Component Locations (CH.4NGE 21)

CHANGE 21



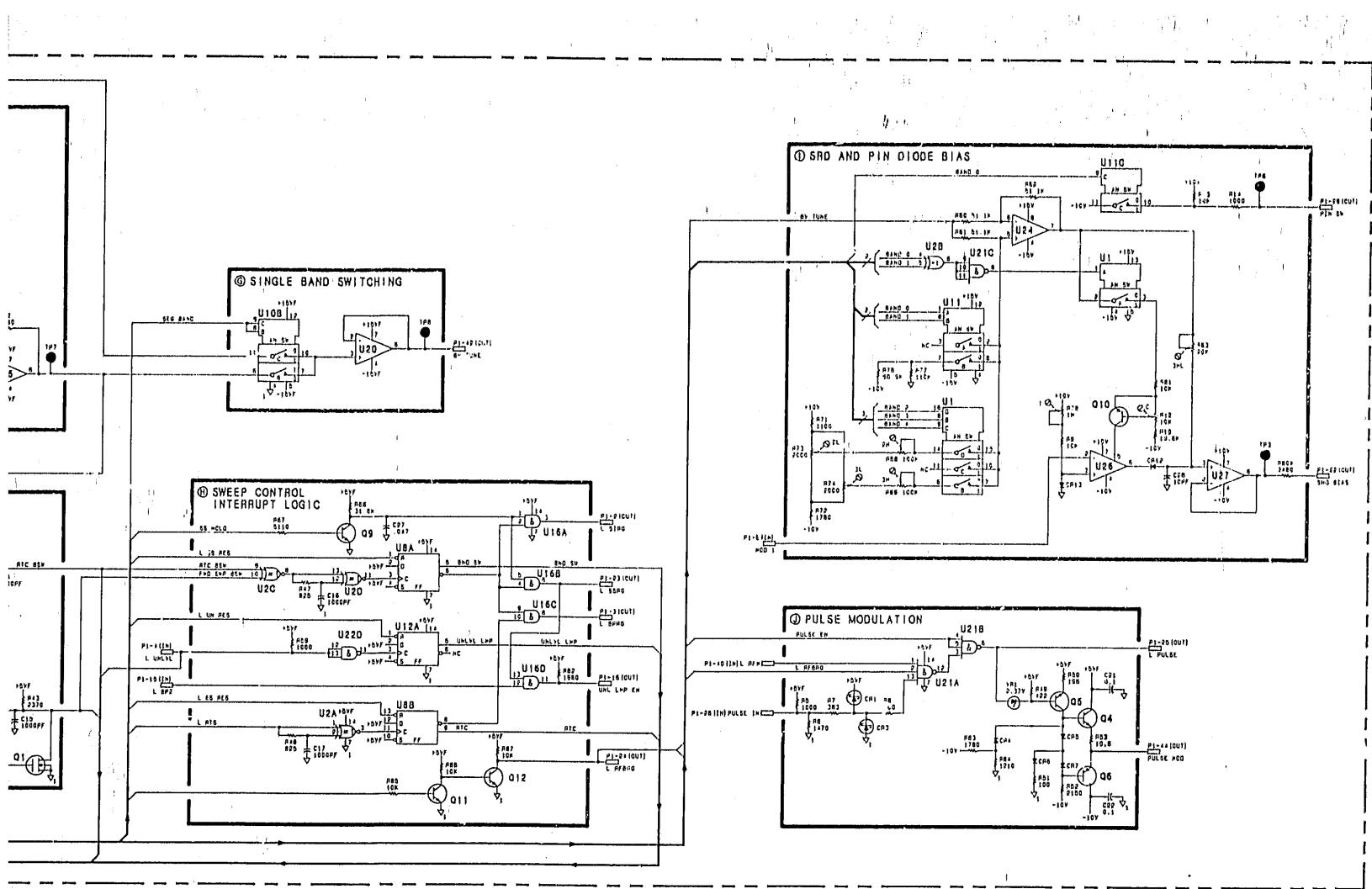


Figure 8-49, A5 Sweep Control, Schematic Diagram(CHANGE 21).

CHANGE 22 !

This change documents a new Front Panel casting and dress panel.

Page 6-21, Table 6-3;

Change MP4, FRONT PANEL-DRESS to HP Part Number 83590-00008, CD 1. Change MPI8, CASTING-FRONT in HP Part Number 83545-20081, CD 7, Change MP19, RETAINER-PUSH CN to HP Part Number 0510-1267, CD 6. Change MP 28, LATCH-SCREW to HP Part Number 83525-20039, CD 0.

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CHANGE 22

83590-90005

# HP 83590A



► CHANGE 23 (Supersodes CHANGE 11)

This change documents a selectable FREQUENCY REFERENCE output.

Throughout the manual there are references to the 1.0 V/OHz rear panel output. Change all references to include 0.5 V/GHz. What follows are some specific ateas to change.

Prge 1-6, Table 1-2, (Supplemental Performance Characteristics): Under GENERAL CHARACTERISTICS: Change Frequency Reference Output to, selectable, 1.0 V/GHz ± 25 mV (0.0) to 18 GHz) or 7.5 V/GHz ± 25 mV (0.01 to 26,5 GHz) rear panel BNC output.

Page 1-8, paragraph 1-22; Change to read as follows: applications.

Page 3-12; ment.

Add the following:



The frequency reference selection switch must be set to the 1.0 V/GHz position bofore performing this adjustment. Refe; 'o Figure 3-10,

Page 6-5, Table 6-3; Change A2 to HP and Mfr. Part Number 83590-60122, CD 6. Add A2C9 HP and Mir. Part Number 0160-4808, CD 4, CAPACITOR-FXD CER 470 pF 100 WV.

Page 6-6, Table 6-3; Change to the following:

Reference HP Part Designation Number A2R8 6757-046 A2R9 0698-725 A2R10 0698-632 A2R11 0698-663 A2R18 0698-315

Add the following:

Reference **HP** Part Designation Number A2R27 A2R29 A2SI A2VR1

0698-543 3101-275 1902-0041

Delete A2R28.

22-1/22-2

CHANGE 23

A rear panel 1.0 V/GHz (0.5 V/GHz) signal corresponds to the RF output frequency up to 18 GHz (26.5 GHz). This output voltage is selectable and muy be used as a reference for pretuninig external equipment. The HP 8410B/8411A network analyzer utilizes the 1.0 V/OHz output for phase-locking. The HP 83554A/55A/56A millimeter-wave source module uses the 0.5 V/GHz as its frequency reference for millimeter frequency

After page 3-12 add page 3-13/3-14, Figure 3-10. Frequency Reference Selection Switch provided in this docu-

Page 5-43, paragraph 5-24, FREQUENCY REPERENCE IV/GHz OUTPUT:

NOTE

HP Port Numbor	CD	Description
G757-0463 0698-7251 0698-6320 0698-6630 0698-6630 0698-3159	4 6 8 3 5	RESISTOR-FXD 82.5K 1% .125W RESISTOR-FXD 4.22K 1% .05W RESISTOR-FXD 5K 0.1% .125W RESISTOR-FXD 20K 0.1% .125W RESISTOR-FXD 26.1K 1% .125W
1g:		
HP Part Number	00	Description
0698-7260 0698-5437 3101-2751 1902-0041	7 6 1 4	RESISTOR-FXD 10K 1%,05W RESISTOR-FXD 12K 0,1%,125W Switch Rocker 2 Position Dip 1A Diode-ZNR 5.11V 5% DO-35 PD=,4W

23-1

# **CHANGE 23 (Cont'd)**

#### Page 6-21, Table 6-3;

Change MP35 to HP and Mfr. Part Number 83592-00028, CD 7.

# Page 8-25, paragraph titled 1V/6Hz Frequency Tracking Amplifier A2: £ 1V/GHz Amplifier A2: G:

Add the following: When A2S1 is closed 0.5 V/GHz frequency reference output is selected. UIA is now scaled to provide 0.5 V per GHz up to 26,5 GHz.

Page 8-31, Figure 8-12:

Replace the Components Location Diagram with Figure 8-12, A2 Front Panel Interface, Components Locations (CHANGE 23) provided in this document.

Page 8-31, Figure 8-18;

Replace Figure 8-18 with Figure 8-18. AI Front Panel/A2 Front Panel Interface, Schematic Diagram (CIIANGE 23) provided in this document.

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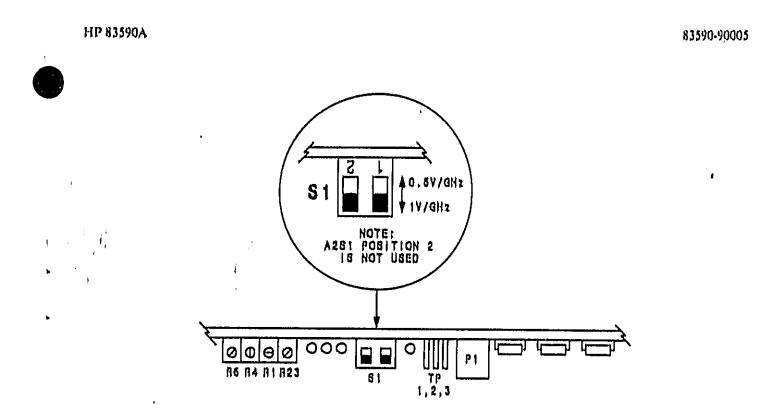


Figure 3. 10. A2 Frequency Reference Selection Switch (CHANGE 23)

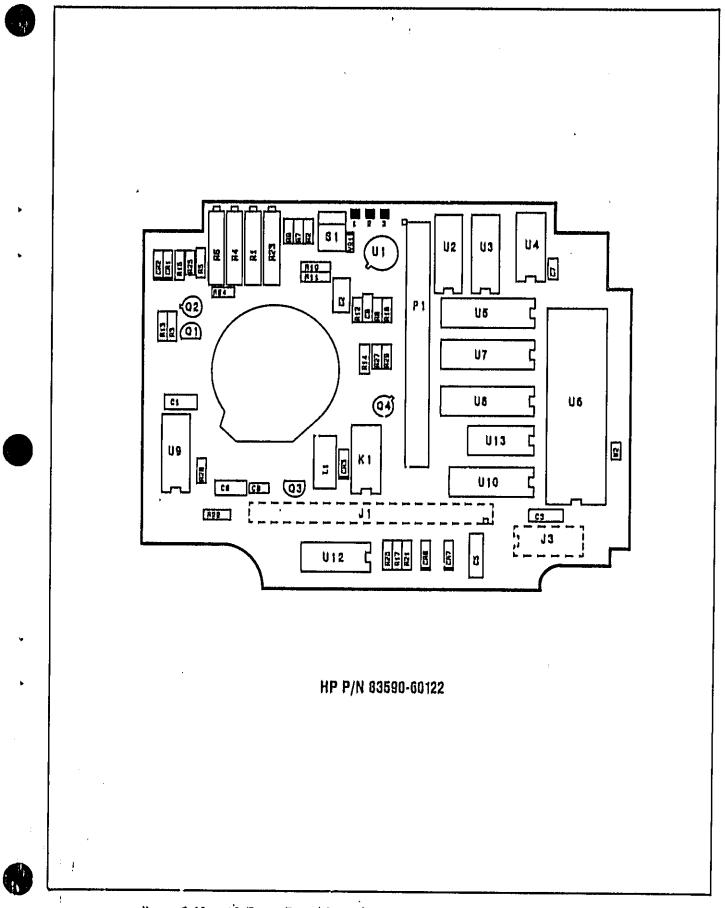
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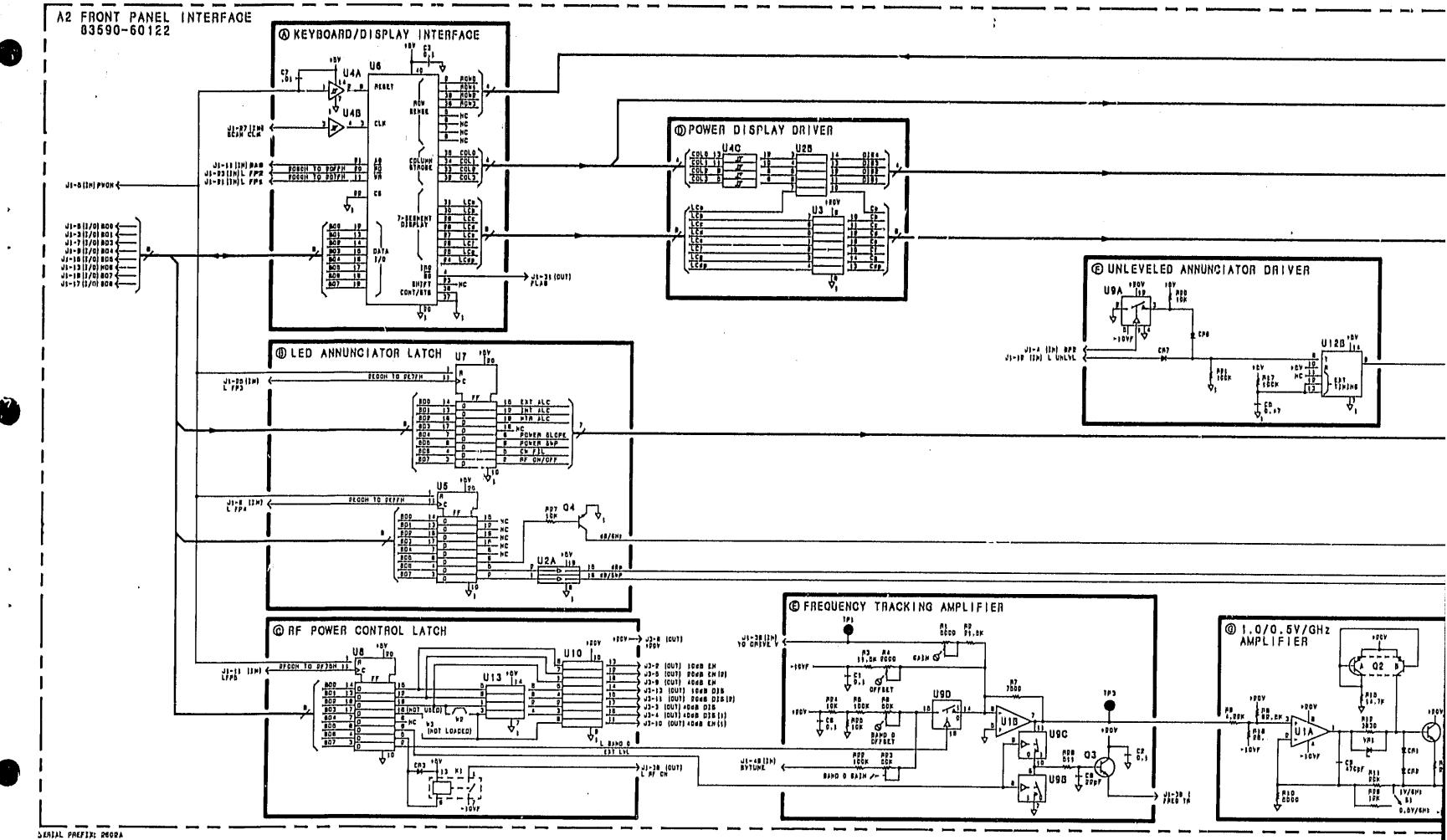


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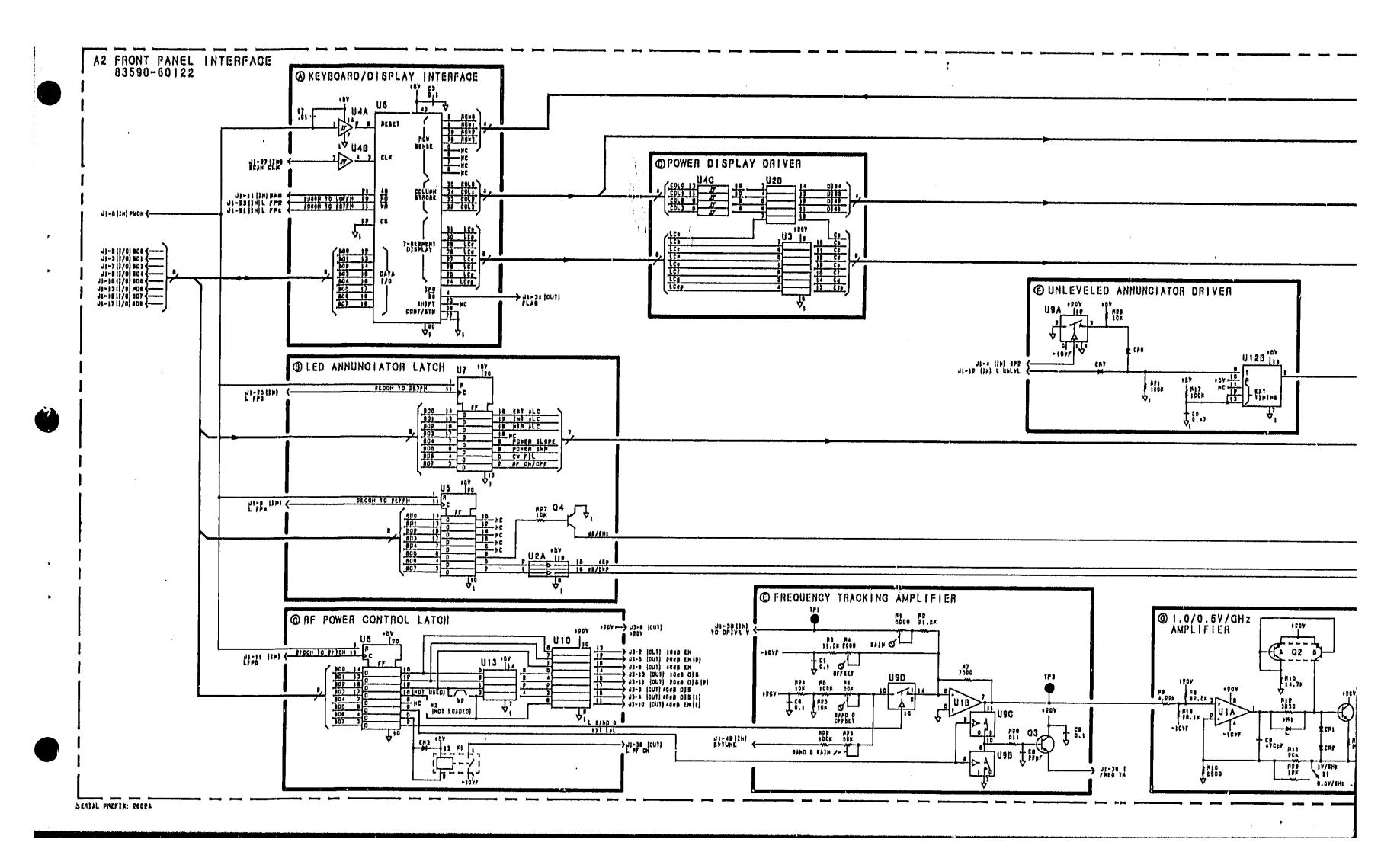
rigure 8-12, A2 Front Panel Interface, Component Locations (CHANGE 23)

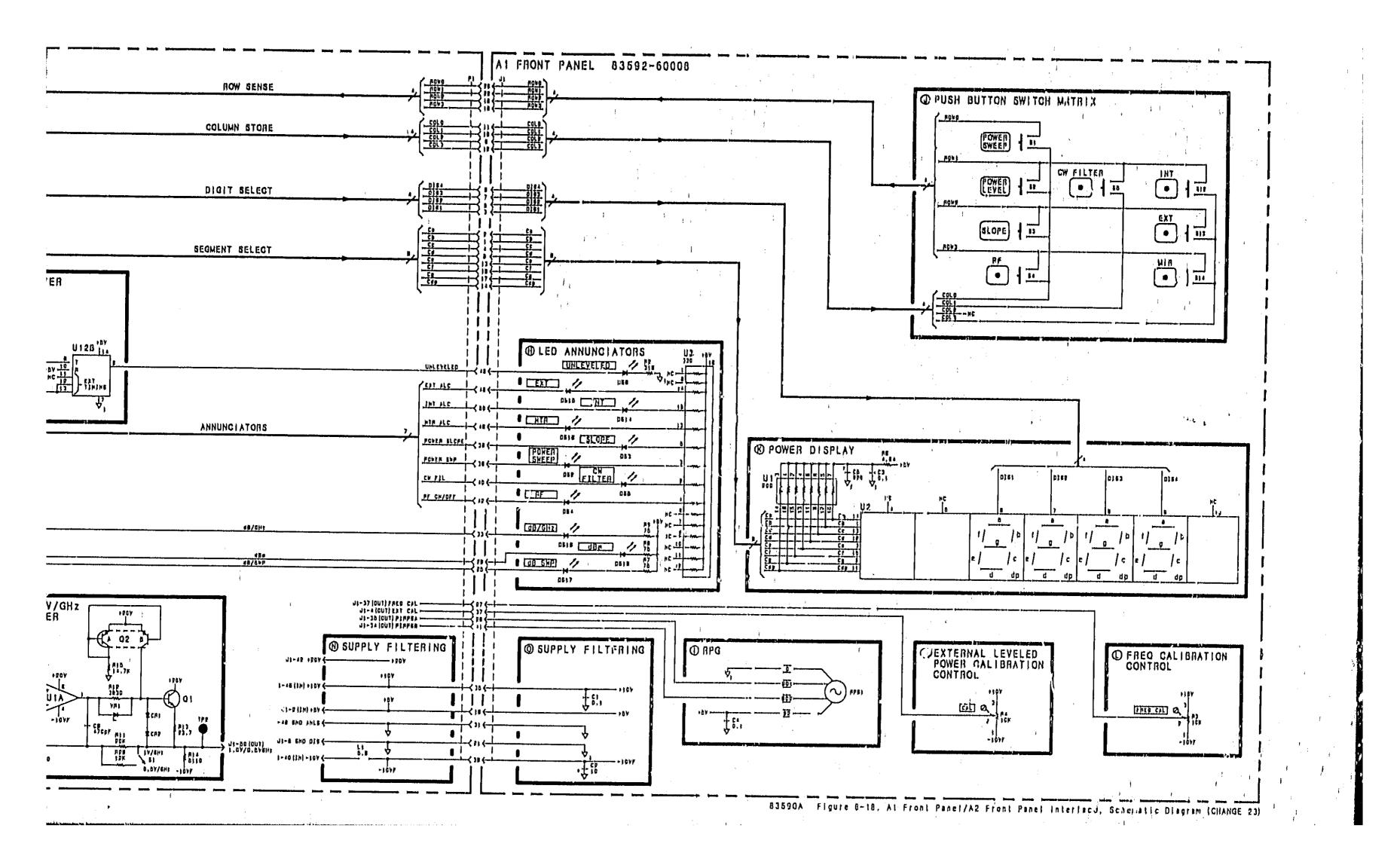
**CHANGE 23** j ´ +

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#### **CHANGE 24**

#### This change documents a new YO Driver Board Assembly,

On the pages listed below, replace the figures with the new figures given,

#### Adjustmonth

Page 5-11, Figure 5-2, - 10V Reference Adjustment Location.
Page 5-14, Figure 5-4, Sweep Control Adjustment Location.
Page 5-17, Figure 5-7, YO and YTM DAC Calibration Adjustment Location.
Page 5-25, Figure 5-14. YO Retrace Compensation Adjustment Location.
Page 5-28, Figure 5-16, YO Delay Compensation Adjustment Location.

#### Service

Page 8-69, Figure 8-63, A8 YO Driver, Component Locations,

Page 8-69, Figure 8-71. A8 YO Driver, Schematic Diagram: Replace Block I YIG COIL CURRENT SOURCE with the partial schematic P/O A8 YO Driver, Schematic Diagram (CHANGE 30) from this document.

#### Page 6-16, Table 6-3;

Change the A8 Part No. to 83595-60070, CD 8, 83595-60070, Add A8C22, 0160-3879, CD 7, CAPACITOR .01UF +20% 100VDC CER, 02010, SR201C103MAA. Add A8C23, 0160-3879, CD 7, CAPACITOR .01UF +20% 100VDC CER, 02010, SR201C103MAA. Add A8C24, 0160-3878, CD 6, CAPACITOR .001UF +20% 100VDC CER, 02010, SR201C102MAA. Add A8C25, 0160-4801, CD 7, CAPACITOR 100 PF + 5% 100VDC CER, 02010, SA101A101JAA.

#### Page 6-17, Table 6-3;

Add A8CR9, 1901-0033, CD 2, DIODE-GEN PRP 180V 200MA DO-35, 00046, NDP692,

#### Page 6-18, Table 6-3;

Add A8R70, 0698-7220, CD 9, RESISTOR 215 1% .05W FTC=+100, 00746, CRB20. Add A8R71, 0698-7220, CD 9, RESISTOR 215 1% .05W FTC=+100, 00746, CRB20.

Page 8-69, Figure 8-71 in the upper left hand corner. Change the Part No. 83592-60002 to 83595-60070.

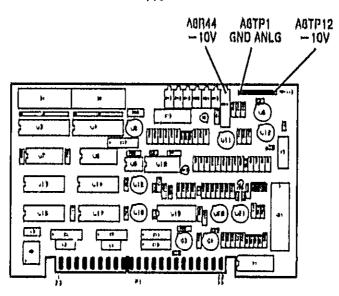
Page 8-69, Figure 8-71 in the lower left hand corner: Change the Serial Prefix 2620A.



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HP P/N 83595-60070

Figure 5-2. - 10V Reference Adjustment Location (CHANGE 24)

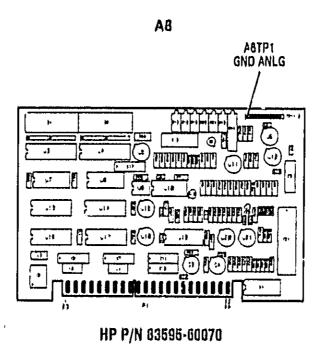


Figure 5-4. Sweep Control Adjustment Locations (CHANGE 24)

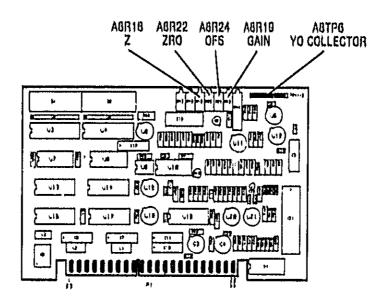
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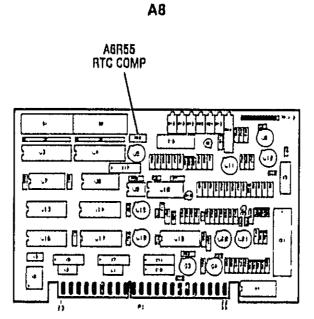


A8



HP P/N 03595-60070

Figure 5-7. YO and YTM DAC Calibration Adjustment Locations (CHANGE 24)



HP P/N 83595-60070

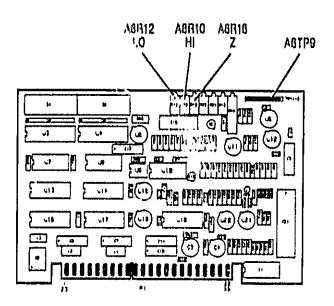
Figure 5-14. YO Retrace Compensation Adjustment Location (CHANGE 24)

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A8



HP P/N 83595-60070

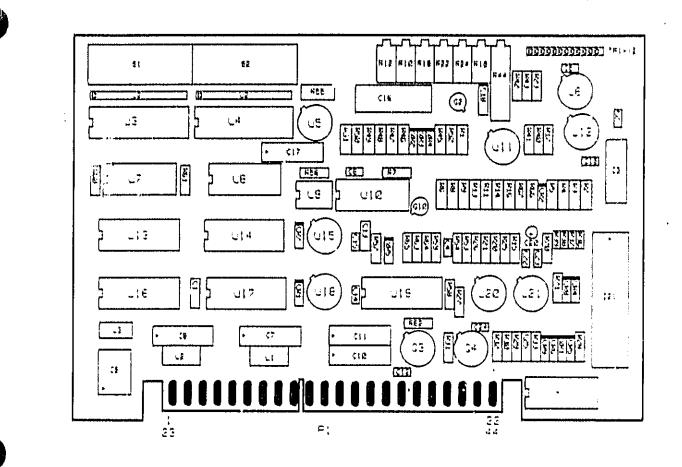
Figure 5-16, YO Delay Compensation Adjustment Location (CHANGE 24)



CHANGE 24

24-7/24-8

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HP P/N 83595-60070

Figure 8-63. A8 YO Driver, Component Locations (CHANGE 24)



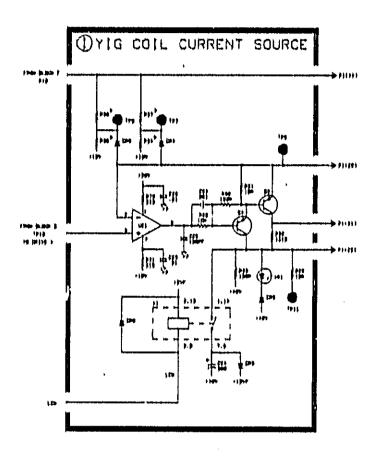
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HP P/N 03595-00070

P/O Figure 8-71. A8 YO Driver, Schematic Diagram (CHANGE 24)

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# ► OHANGE 25

This change documents the addition of a jumper to the A4 ALC assembly, it does not change any electrical functions of the ALC. Change 14 in this document is assumed to be incorporated prior to making the changes written in this change (Change 25),

Section VL/Replaceable Parist

Change A4 ALC assembly to HP and Mfr. Part Number 83590-60098, CD 5.

Add A4W6, HP and Mfr, Part Number 8159-0005, CD 0, RESISTOR-ZERO OHMS 22 AW6 LEAD DIA.

Page 8-47, Figure 8-29: Replace the Compos

Replace the Components Location Diagram with Figure 8-29, A4 ALC, Component Locations (CHANGE 25) provided in this document.

Poge 8-47, Figure 8-34;

Add A4W6 in series with the input to U15C pin 9 located in block N, PIN MOD 1 DRIVER.



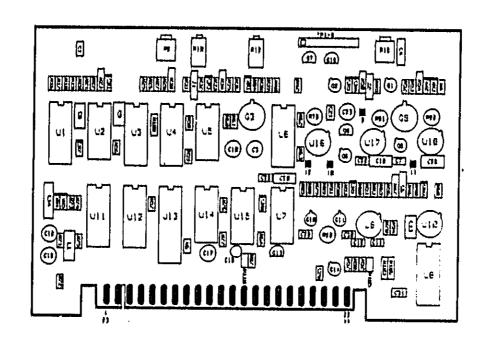
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CHANGE 25

83590-90005

HP 83590A





HP P/N 83590-60098

Figure 8-29. A4 ALC Component Locations (CHANGE 25)

# ADDENDUM

# MANUAL CHANGES

NOTE

This ADDENDUM contains important information of the kind normally contained in the attached MANUAL CHANGES supplement but received too late to be included. Use the ADDENDUM to correct your manual in the same way you use the MANUAL CHANGES supplement.

MANUAL IDENTIFICATION

HP Number: HP 83590A Data Printad: Feb. 1982 Part Number: 83590-90005

NEW ITEM

Serial Profix or Number	Mako Manual Changos
2718A	2, 3, 5, 9, 13-16, 18-26
2726A	2, 3, 5, 9, 13-16, 18-27



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Addendum Date: June I, 1987 For Manual Changes Dated: November 12, 1986



HP 83590A

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# ► - NEW ITEM

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	Sorial Profix No,	Chango Numbor	Assemblies Affected	Now Assembly Part Number	Manual Socilons Alfociad
	2718A	20	AG	N/A	Nonø
•	2726A	27	A4 83592-60077 83592-60132	N/A	Replaceable Parts

# NUMBERED CHANGES INDEX

HP 83590A

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#### **OHANGE 26**

This change documents a serial prefix change only,

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HP 82550A



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#### ► CHANGE 27 Page 6-8, Table 6-3:

Change A4R64 to 1,96K onms HP part number 0698-7256, CD 1,

Page 6-9, Table 6-3; Change A4U7 to HP part number 1820-1425, CD 6,

Page 8-47, Figure 8-34 (Block K): Change A4R64 to 1,96K ohms.

NOTE: A4R64 and A4U7 are interactive components, therefore, they both must be changed at the same time,



#### MANUAL IDENTIFICATION

HP Model Number: HP 83590A Manual Part Number: 83590-90005 Date Printed: February 1982

#### **CHANGE 28**

Change 28 documents cerial number prefix 2809A.

This change documents a new A4 assembly,

#### INSTRUCTIONS

Replace — Replace the existing manual page(s) with the page(s) provided in this change. These page(s) supersede the existing page(s) in the manual, provided that the serial number prefix of your instrument is the same or higher than the one indicated on this page. To keep your documentation applicable to all versions of instruments, place the superseded page(s) in the MANUAL BACKDATING section of your manual.

#### Replace the following pages:



Title Page 5-1 through 5-6 5-45 through 5-52 6-7 through 6-10 8-37 through 8-47

HP Part Number 83590-90036 (For HP Internal Use Only) Part of HP Part Number 83590-90033

Change 28 28-1/28-2



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#### SERIAL NUMBERS

This manual applies directly to HP 83590A RF plug-in having serial number prefix 2148A.

For Instruments with serial prefix 2143A and below, refer to Section 7, Manual Backdating

For additional information about serial numbers, refer to INSTURMENTS COVERED BY MANUAL in Section 1.

Manual Changes Supplement Print Date: 1 FEBRUARY 1988

Change	Documents Prefix	Change	Document <del>a</del> Prefix	Changa	Documente Prefix
1	2216A	17	2420A		
2	2217A	18	2451A		
3	2221A	10	2502A		
4	2233A	20	2507A		
6	2234A	21	2519A		
6	2240A	22	2543A		
7	2252A	23	2602A		
8	2306A	24	2610A		•
0	2310A	25	2645A		
10	2315A	26	2718A		
11	2338A	27	2726A		
12	2410A	28	2809A		
13	2411A	1			
14	2411A				
15	2412A				
16	2413A				

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MANUAL PART NO, 83890-90005 Microfiche Part Number 83590-90006

Printed: FEBRUARY 1982





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#### CERTIFICATION

Hewlett-Packard Company certifies that this product mat its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

#### WARRANTY

This Hewlett-Packard Instrument product is warranted against defects in material and workmanship for a period of one year from date of delivery. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall propay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

#### LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance,

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ers:

Model 83590A

Adjustments

# SECTION V ADJUSTMENTS

#### 5-1. INTRODUCTION

5-2. This section provides adjustment procedures for the Model 83590A RF Plug-in. These procedures should not be performed as routine maintenance but should be used (1) after replacement of a part or component, or (2) when performance tests show that the specifications of Table 1-1 cannot be met. Table 5-1 lists all of the adjustments by reference designation, adjustment name, adjustment paragraph, and description. Each procedure includes a test setup illustration and one or more adjustment location illustrations. Table 5-2 lists the adjustment included in this section.



#### NOTE

Allow the B3590A RF' Plug-in and the 8550A Sweep Oscillator to warm up for 30 minutes prior to making any adjustments.

#### 5-3. SAFETY CONSIDERATIONS

5-4. Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition. Service and adjustments should be performed only by a skilled person who is aware of the hazard involved.

# WARNING

Adjustments in this section are performed with power supplied to the instrument while protective covers are removed. There are voltages at points in the instrument which can, if contacted, cause personal injury. Be extremely careful. Adjustments should be performed only by a skilled person who is aware of the hazard involved. Capacitors inside the instrument may still be charged, even if the instrument has been disconnected from its source of supply,

#### NOTE

Use a non-metallic adjustment tool whenover possible.

#### **B-B, EQUIPMENT REQUIRED**

5-6. The equipment required for the adjustment procedures is listed in Section I of this manual. If the test equipment recommended is not available, other equipment may be used if its performance meets the critical specifications listed in the table. The specified equipment required for each adjustment is referenced in each procedure.

#### 5-7. FACTORY-SELECTED COMPONENTS

5-8. Table 5-3 contains a list of factory-selected components that includes the reference designation, the related adjustment procedure, the allowable range of values, and the basis of selection. Nominal values are given for the factory-selected components, designated by an asterisk (*), on the schematic diagram and in the replacement parts list. HP Part Numbers for selected values are given in Table 5-4.

#### 5-9, RELATED ADJUSTMENTS

5-10. Interactive adjustments are noted in the adjustment procedures. Table 5-5 indicates by paragraph numbers the adjustments that must be performed if an assembly has been repaired or replaced or if an adjustment has been made to an assembly.

#### 5-11. ADJUSTMENT PROCEDURES

5-12. Adjustment procedures are given in the proper sequence to allow for interrelated adjustments.

Change 28

# Adjustments

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Reference Designation	Adjustment Neme	Adjustment Paragraph	Description
A2R1	GAIN	5+2+4	Sets gain of frequency reference in Bands 1, 2, and 3 (1V/GHz),
A2R4	OFFSET	5+2:4	Sets offset of frequency reference in Bands 1, 2, and 3 (1 V/GHz),
A3S1	Configuration Switch	5-13	Selects Plug-in code, power-up power level, FM sensitivity, FM modulation coupling, step attenuator Option Code, normal or sequential sweep option, and phase-lock operation.
A4R6	I LO	5-26	Sets power calibration at the low end of the power range $(-5 \text{ dBm})$ .
A4R49	IН	5-26	Sets power calibration at the high end of the power range (+10 dBm).
A4R54	IMD	5-26	Sets power calibration at the middle of the power range (0 dBm),
A4R59	SYM	5-25	Sets best square wave symmetry,
A5C14	LO	5-30	Adjusts low frequency for best frequency response flatness through U10,
A5R18	FM OFFSET	5+30	Adjusts shape of U10 Video Amplifier compensation network response.
A5R19	FM	5+30	Sets DC offset of U10 Video Amplifier,
A5R34	6P (	5-26	Breakpoint that works with SLI (Slope 1) for ALC flatness.
A5RJ6	BP 2	5+26	Breakpoint that works with SL2 (Slope 2) for ALC flatness,
A5R38	BP 3	5-26	Breakpoint that works with SL3 (Slope 3) for ALC flatness,
A5R40	BP 4	5-26	Breakpoint that works with SL4 (Slope 4) for ALC flatness,
A5R41	SLI	5-26	Slope adjustment for best ALC flatness,
A5R42	SL 2	5-26	Slope adjustment for best ALC flatness.

Table 5-1, Adjustable Components (1 of 4)

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Table 5-1. Adjustable Components (2 of 4)

Reference Designation	Adjustment Name	Adjustment Paragraph	Description
A5R43	SL 3	5-28	Slope adjustment for best ALC flatness.
A5R44	SL 4	5-28	Slope adjustment for best ALC flatness,
A5R48	slp	5-23	. Sets overall slope of internal leveling ALC.
A5R50	PWSP	5-29	Sets range for power sweep.
A5R75	н	5+30	Works in conjunction with C14 to set frequency respon flatness of FM Coil.
A6R12	c	5-20, 5-21	Adjusts YTM SRD bics to peak power in all bands at lo power settings.
A6R16	TV GAIN	5.15	Sets the gain of U6 Tune Voltage buffer amplifier.
A6R21	DAC CAL	5-15	Adjusts the gain of U5 Variable Gain Amplifier during all sing band sweeps.
A6R24	B.	5-15, 5-23	Adjusts the gain of U5 Variable Gain Amplifier in Band 3 durir sequential sweeps.
A6R26	82	5-15, 5-23	Adjusts the gain of U5 Variable Gain Amplifier in Band 2 durin sequential sweeps.
A6R28	B1	5-15, 5-23	Adjusts the gain of U5 Variable Gain Amplifier in Band 1 durin sequentic, sweeps,
A6R34	-IOV OFFSET	5-13	Offsets the -10 volt reference voltage to U15.
A6R37	sp	5-15	Offsets input voltage to U24A forward sweep bandswite amplifier.
A6R63	3HL	5-20, 5-21	Adjusts balance of SRD Bias circuit.
A6R68	214	5+20, 5+21	Adjusts YTM SRD bias at high power, high frequency en- of Band 2.
A6R69	3H	5-20, 5-21	Adjusts YTM SRD bias at high power, high frequency enorgy of Band 3.
A6R73	2L.	5-20, 5-21	Adjusts YTM SRD bias at high power, low frequency end o Band 2.
A6R74	3L	5-20, 5-21	Adjusts YTM SRD bias at high power, low frequency end o Band 3,
A6R78	т	5-20, 5-21	Adjusts YTM SRD bias at an intermediate power level for Bands 2 and 3.
A7R]0	SGL HI	5-22	Adjusts offset of YTM delay compensation signal at the high end of single band sweeps.

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5-3

# Adjustments

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Reference Designation	Adjustment Namo	Adjustment Peregraph	Description
A7R12	SGL LO	5-22	Adjusts offset of YTM delay compensation signal at the low end of single band sweeps.
л7R18	2	5.16	Adjusts offset of U20 delay compensation amplifier to minimize the difference between CW and AF ±0 with YTM delay compen- sation circuits.
A7R19	GAIN	5.16	Adjusts the Scaled Voltage Tune DAC input signal to U21 YTM Summing Amplither.
A7R22	ZRO	5+16	Adjusts supply correction voltage to U21 YTM Summing Amplifier.
A7R24	OFS	5+16	Adjusts Offset DAC input signal to U21 YTM Summing Ampli- fier.
A7R42	SEQ HI	5-22	Adjusts offset of YTM delay compensation signal at high end of sequential band sweeps.
A7R43	SEQ LO	5-22	Adjusts offset of YTM delay compensation signal at low end of sequential band sweeps.
A7R45	SEQ TC	5-22	Adjusts gain of YTM delay compensation signal in sequential band sweeps.
A7R46	SGL TC	5-22	Adjusts gain of YTM delay compensation signal in single band sweeps.
A7R51	BLOFS	5-20	Adjusts offset of U21 Summing Amplifier in single band sweeps.
A7R55	RTC COMP	5+22	Adjusts the pulse width of YTM retrace compensation signal.
A7S1	OFFSET	5+29	Adjusts low end of band YTM to YO tracking at slow sweep speeds.
A752	GAIN	5-20	Adjusts high end of band YTM to YO tracking at slow sweep speeds.
ABRIO	н	5-19	Adjusts YO delay compensation at high frequency end of band.
A8R12	LO	5-19	Adjusts YO delay compensation at low frequency end of band.
A8R18	Z	5+16, 5-19	Adjusts offset to minimize the difference between CW and $\Delta F$ ±0 with YO delay compensation circuits.
ABR19	GAIN	5-16	Adjusts Scaled Voltage Tune DAC input signal to U20 Summing Amplifier.
A8R22	ZRO	5-16	Adjusts supply correction voltage to U20 Summing Amplifier.

Table 5-1. Adjustable Components (3 of 4)



Table 5-1, Adjustable Components (4 of 4)

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Reference Designation	Adjustment Nama	Adjustment Paragraph	Dascription
ABR24	ors	5+16	Adjusts Offset DAC input signal to U20 Summing Amplifier.
A8R44	-10V	5-1-4	Sets -10 volt reference voltage source.
A8R55	RTC COMP	5-18	Adjusts the pulse width of the YO retrace compensation signal.
A851	OFFSET	5.17	Adjusts the low end of band YO frequency accuracy.
A852	GAIN	5+17	Adjusts the high end of band YO frequency accuracy.
AI3AIR4		pone	Factory adjusted.
AI4AIRH		none	Factory adjusted,
AL4ATRI3		none	Factory adjusted,
A14A1R14		none	Factory adjusted.
AL4ALR15		none	Factory adjusted.
AI4AIR16		none	Factory adjusted.
A14AIRI8		none	Factory adjusted.
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Paragraph	Adjustments	Parngraph	Adjustments
5+13	Configuration Switch A3S1	5.22	YTM Delay Compensation
5-14	-10 Volt Reference On AB YO Driver	5+23	Band Overlap Adjustment
5-15	Sweep Control Adjustments	5-24	Frequency Reference 1V/GHz Output
5-16	YO and YTM DAC Calibration	5-25	Sample & Hold Compensation
5-17	Preliminary Frequency Accuracy	5-26	ALC Power Calibration
5-18	YO Retrace Compensation	5.27	ALC Gnin Check
5-19	YO Delay Compensation	5-28	Internal Leveled Flatness
5-20	Slow Speed YTM to YO Tracking	5-29	Power Sweep
5-21	SRD Blas	5+30	FM Driver Adjustments

Table 5-2, Adjustments

Table 5-3. Factory Selected Components

Reference Designator	Adjustment Paragraph	Allowable Range of Values	Basis of Selection
A4R72	5-27		Selected at factory for best ALC gain
A5R31	5-30	200 to 300 Ohms	Selects scaling of current drive of YO FM coil near 100 kHz.
A7R34	none		Selected at factory to correct for frequency nonlinearity in YTM.
A7R35-39	none		
A7R66-71	none		
A8R36	none		Selected at factory to correct for frequency nonlinearity in the YO.
A8R37-39	none		
Aljairi	nane		Selected at factory to optimize YO band- width, power, and harmonics.
A13A1R2	none		

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# 5-25. Sample & Hold Compensation

NOTE: To completely adjust the leveling loop, perform procedures 5-25 through 5-28 in the order given. Doing these adjustments out of order can cause leveling and/or power variation problems.

#### EQUIPMENT

Sweep Oscillator Mainframe
Extender Board
Adapter 3,5(f) to Type-n(m)
Oscilloscope
Crystal Datactor
10 dB Attenuator
Adapter 3.5(f) to Type-N(m) HP Part Number 1250-1744

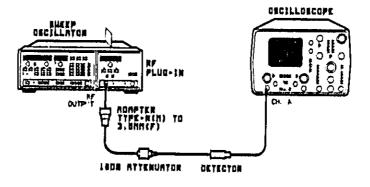


Figure 5-33, Sample & Hold Test Setup

### PROCEDURE

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NOTE: Turn AC power OFF when you remove or install an assembly.

- NOTIE: This procedure assumes that A3S1 is set to the factory-set position.
- 1. With AC power OFF, put the A4 ascembly on an extender board and connect the equipment as shown in Figure 5-33.

# 5-25. Sample & Hold Compensation (Cont'd)



- a. Turn power on and press [INSTR PRESET],
- b. Press [CW] [2] [.] [5]] [GHz].
- c. Turn square wave modulation on.

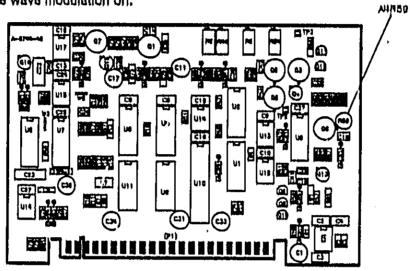


Figure 5-34, Sample & Hold Compensation Adjustment Locations

- 3. Observing the RF output on the oscilloscope, adjust A4R59 for the best square wave.
- 4. Install the A4 assembly in the plug-in and re-check the square wave. Repeat steps 3 and 4 as necessary,



# 5-26. ALC Power Calibration

NOTE: To completely adjust the leveling loop, perform procedures 5-25 through 5-28 in the order given. Doing these adjustments out of order can cause leveling and/or power variation problems.

#### EQUIPMENT

· · · · · · · · · · · · · · · · · · ·
Sweep Oscillator Mainframe
Scalar Network Analyzer
Detector
10 dB Attenuator , , , , , , , , , , , , , , , , , , ,
Adapter 3.5(1) to Type-n(m) HP P/N 1250-1744
Power Meter HP 436A
Power Sensor HP 8485A
Adapter 3.5(f) to Type-N(m) HP Part Number 1250-1744
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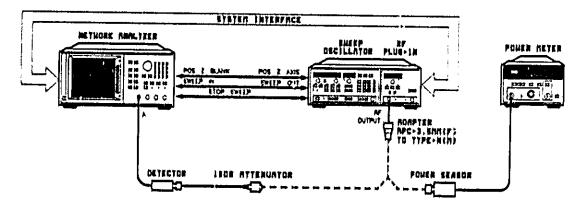


Figure 5-35. ALC Power Calibration Adjustment Setup

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# 5-26. ALC Power Calibration (Cont'd)

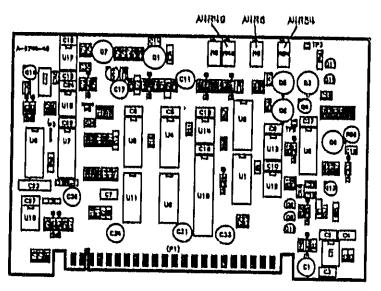


Figure 5-36. ALC Power Calibration Adjustment Locations

# PROCEDURE

NOTE: This procedure assumes that A3S1 is set to the factory-set position.

- 1. Connect the network analyzer as shown in Figure 5-35, and press [INSTRPRESET] on the analyzer.
- 2. On the sweep oscillator, press [CW] [2] [.] [4] [GHz].
- 3. Repeat the following, as necessary:
  - a. Set power to -5 dBm and adjust A4R6 for  $-5 \pm 0.1$  dBm.
  - b. Set power to 0 dBm and adjust A4R54 for 0  $\pm$  0.1 dBm,
  - c. Set power to +10 dBm and adjust A4R49 for +10  $\pm$ 0.1 dBm.
- 4. To check the power accuracy, step from -5 to 10 dBm in 1 dB increments. The power meter reading should be within  $\pm 0.1$  dBm at each setting.

5-48

5-27. ALC Gain Check

NOTE: To completely adjust the leveling loop, perform procedures 5-25 through 5-28 in the order given. Doing these adjustments out of order can cause leveling and/or power variation problems.

#### EQUIPMENT

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Function Generator	
Oscilloscope	
10 dB Attenuator HP 6493C O	ption 010
Adapter 3.5(I) to Type-n(m) HP P/N 1	250-1744

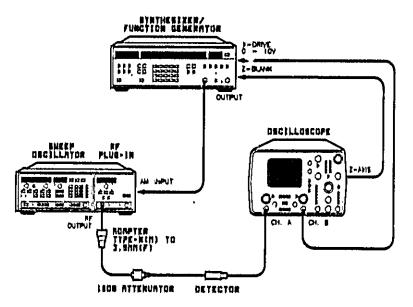


Figure 5-36a, ALC Gain Check Test Setup

#### PROCEDURE

NOTE: This procedure assumes that A3S1 is set to the factory-set position.

1. On the function generator, connect the Vp-p output to the oscilloscope CHANNEL A INPUT.

# 5-27. ALC Gain Check (Cont'd)

2,	Set instrument controls as follows:
	Sweep Oeciliator: Start
	RF Plug-In: Power Level
	Function Generator:       1 kHz         Stop Frequency       300 kHz         Function       [m]         Time       0.5 sec         Amplitude       2V
	Oscilloscope: Mode

- 3. Connect the equipment as shown in Figure 5-36a,
- 4. On the oscilloscope, use the CHANNEL A knob CAL to adjust the left edge of the signal for two divisions p-p,

Channel B V/Div Display

- Monitoring CHANNEL A, manually sweep the plug-in frequency range and note the frequency at which the highest gain peaking occurs. This point should measure less than four divisions p-p (see Figure 5-36b).
- 6. Change the plug-in power level to +3 dPm and repeat step 5, adjusting the oscilloscope for a two division p-p display at the left edge of the CRT.
- 7. Change the plug-in power level to +i0 dBm (+7 dBm for option 002) and repeat step 5, adjusting the oscilloscope for a two division p-p display at the left edge of the CRT.

# 5-27. ALC Gain Check (Cont'd)

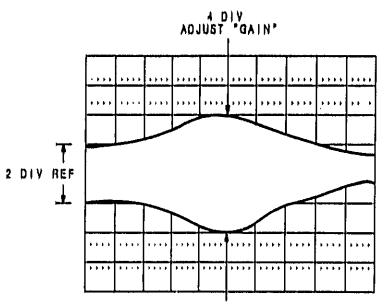


Figure 5-36b, Maximum Allowable ALC Gain Peak

8. If the gain is too high, increase A4R72. An increasing value decreases loop gain,

NOTE: Extreme value changes can affect the bandwidth and stability of A4U17B (the mod driver).

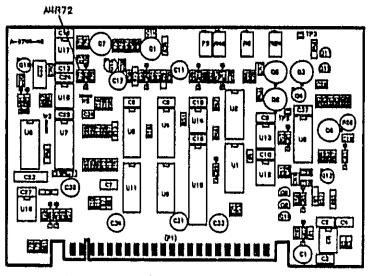


Figure 5-36c, ALC Gain Adjustment Locations

### 5-28. Internal Leveled Flatness

NOTE: To completely adjust the leveling loop, perform procedures 5-25 through 5-28 in the order given. Doing these adjustments out of order can cause leveling and/or power variation problems.

#### DESCRIPTION

Four parallel circuits on the A5 assambly provide adjustments for ALC flatness. BP1 through BP4, and SL1 through SL4 determine the shape of the flatness compensation signal.

#### EQUIPMENT

Sweep Oscillator Mainframe	* * * * * * * * * * * * * * * * * * * *	. HP 8350
Soslar Network Analyzer	****	HP 8757A
Detector	• • • • • • • • • • • • • • • • • • •	P 85025B
10 dB Attenuator		Intion 010
Adapter 3,5(1) to Type-n(m)	···· HP P/N	1250-1744

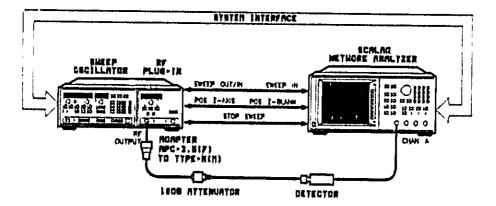


Figure 5-36d. Internal Leveled Flatness Adjustment Test Setup

### PROCEDURE

1. Connect the equipment as shown in Figure 5-36d and allow 30 minutes for warm-up.

# 5-28. Internal Leveled Flatness (Cont'd)

- 2. On the scalar network analyzer:
  - a. Press [PRESET], and select [CHANNEL 2 OFF],
  - b. Press [SYSTEM], and select [MODE DC].
  - c. Select [CAL] [DC DET ZERO] [MANUAL].
- 3. On the plug-in, turn the RF power off.
- 4. On the analyzer, select [CONT].
- 5. On the plug-in, press [RF] to turn the power back on.

The sweep oscillator/RF plug-in should be in full sweep range, and the sweep time should be 0.2 seconds.

### **Preset the Adjustments**

6. Set A5R34, A5R36, A5R38, and A5R40 (BP1 to 4) fully CW. Set A5R41 through A5R44 (SL1 to 4) to mid-range.

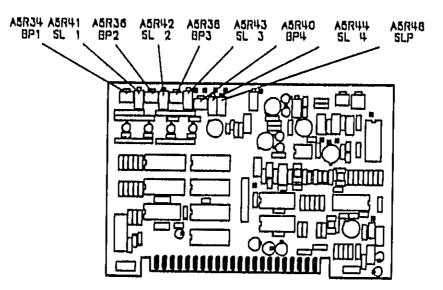


Figure 5-36e. Internal Leveled Patness Adjustment Locations

- 7. On the scalar network analyzer:
  - a. Press [SCALE] [1] [dB].
  - b. Press [REF] and select [REF LEVEL]. Use the rotary knob to center the trace on the display.
  - c. Adjust [REF POSN] to center the reference line (see Figure 5-36f),
- 8. Adjust A5R48 (SLP) for the flattest scalar network analyzer display (see Figure 5-36g),



#### 5-28. Internal Leveled Flatness (Cont'd)

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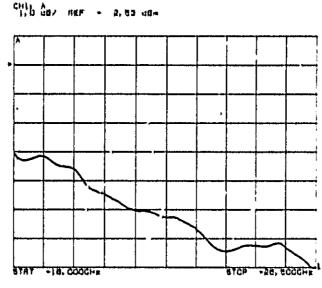


Figure 5-36f. Trace Before Adjustments

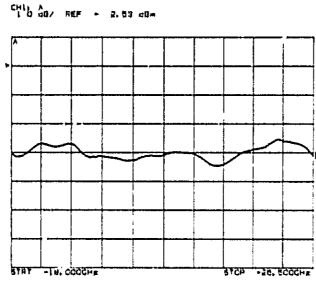


Figure 5-36g. Trace After Main Slope Adjustment

- The following adjustments affect the displayed output from left to right, with A5R34 (BP1) and A5R41 (SL1) having the greatest affect. Adjust the breakpoint and slope adjustments in pairs (e.g. adjust A5R34 (BP1) and A5R41 (SL1) before you continue to A5R36 (BP2) and A5R42 (SL2), etc.).
- 10. Identify the breakpoint (it appears as a pivot point on the trace). Adjust A5R34 (BP1) so that the adjustment point lies, as closely as possible, on the breakpoint.

If needed, use the scalar network analyzer SCALE function to increase the displayed resolution.

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# 5-28. Internal Leveled Flatness (Cont'd)

- 11. Adjust A6R41 (SL1) to rotate the slop: and bring it closer to a flatter display, iterate between A5R34 (BP1) and A5R41 (SL1) for the flattest display.
- 12. Repeat step 11 for the following adjustment pairs:

A5R36 (BP2) and A5R42 (SL2) A5R36 (BP3) and A6R43 (SL3) A5R40 (BP4) and A5R44 (SL4)

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The final, properly adjusted trace should be similar to Figure 5-36h. If the trace is not adjusted properly, return to step 6. Do not attempt to readjust from the middle of the processes,

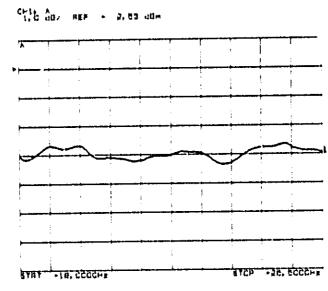


Figure 5-36h. Properly Adjusted Power

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#### Table 6-3, Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3U6 A3U7 A3U7 A3U9 A3U9 A3U10	1820-1502 1810-1197 1850-1416 1850-1216 1850-1216 1850-1416	7 8 6 3 6	1 3 7	IC GATE TTL LE NAND TPL 3-INP IC GATE TTL LE NAND GUAD B-INP IC SCHMITT-TRIG TTL LE INV HEX 1-INP IC DCDR TTL LE 3-TO-B-LINE 3-INP IC SCHMITT-TRIG TTL LE INV HEX 1-INP	01298 01298 01298 01298 01298 01298	ENTALBION ENTALEGOON ENTALEGOAN ENTALEIJAN ENTALBIAN
A3U11 A3U12 A3U12 A3U13 A3U14 A3U16	1820-1418 1810-0338 1820-1818 1820-1818 1820-1418	8 7 3 8 8	3	IC SCHWITT-TRIG TTL LE INV HEX I-INP NETWORK-RES 16-DIP100 0 OHM X 8 IC DCDR TTL LE 3-TO-8-LINE 3-INP IC BER TTL LE NON-INV HEX 1-INP IC SCHWITT-TRIG TTL LE INV HEX 1-INP	01596 11230 01596 01296 01296	5N74LE1AN 781-3-R100 6N74L5138N 6N74L5138A 6N74L514N
A3U16 A3U17 A3U18 A3U18 A3U18	1810-0338 1850-5078 1850-5078 1850-5078 1810-0338	7 4 7	2	NETWORK-RES 16-DIP100 0 OHM X 8 IC MISG TTL LS IC MISG TTL LS NETWORK-RES 16-DIP100 0 OHM X 8	11226 01295 01295 11236	761-3-R100 8N74L524EN 8N74L524EN 761-3-R100
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HP Part Reference Description Designation Number м 83880-80138 Board Assembly-ALD 0150-3771 0160-4054 0160-4054 0160-4054 1 0 UF PCAP 0.1 UF CAP 0.1 UF CAP 0.1 UF CAP 0.1 UF CAP MO AAC2 AAC3 AAC3 AAC4 AAC8 0160-4084 0.1 UF CAP 0.1 UF CAP 1 0 UF CAP 0.1 UF CAP 0.1 UF CAP AACS 0160-4084 0160-4084 0160-4838 A4CT A4CE AACI AAGIO 0160-4084 0160-4084 0180-3770 0160-4084 0160-4084 0160-3679 0160-3679 1.2 UF PCAP 0.1 UF CAP 0.1 UF CAP 0.01 UF CAP 0.1 UF CAP A4G11 A4G12 A4G13 A4G14 A4G14 A4G16 0150-4084 0150-3833 0150-3879 0150-3875 0150-3874 0.1 UF CAP 92 UF PCAP 0 01 UF CAP 92 DF PCAP 10 DF CAP A4C16 A4C17 AAG18 AAG19 A4C20 MC21 Not Assigned 910 pF CAP 2.2 uF PCAP 0.1 uF CAP 0.1 uF CAP 0160-0945 0150-0128 0160-4084 0160-4064 A4C22 A4C23 1C24 A4C28 Not Assigned 0.1 uF CAP 0.01 uF CAP 2200 pF CAP A4C26 A4C26 A4C27 A4C28 A4C29 A4C30 0160-4064 0160-3879 0160-0572 Not Assigned A4C31 A4C32 A4C33 A4C34 A4C34 A4C35 10 UF PCAP 10 UF PCAP 10 UF PCAP 10 UF PCAP 2200 CF CAP 0180-3831 0180-3831 0180-3831 0180-3831 0180-3831 0160-0572 A4C38 A4C37 A4C38 A4C38 Not Assigned 0.1 uF CAP \$200 pF CAP 0.01 uF CAP 0160-4084 9160-0672 0160-3878 10 pF CAP 220 pF CAP 100 pF CAP AACAD 0160-3874 A4C41 A4C42 0160-0673 0160-4389 PIN DIODE PIN DIODE PIN DIODE Not Assigned SCHOTTKY DIODE AACRI 1901-1098 A4CR2 A4CR3 A4CR3 A4CR4 A4CR5 1901-1098 1901-0535 AACR6 AACR7 AACR8 AACR8 AACR8 AACR10 1001+1098 PIN DIODE Not Assigned Not Assigned P-N DIODE 1901-1098 1001-0535 ECHOTTKY DIODE 1001-0535 1001-0535 AACRII SCHOTTKY DIODE SCHOTTKY DIODE Not Assigned AACR12 AACR13 1261-2194 1261-2194 1261-2194 1261-2194 1261-2194 5000-9043 5040-6848 CONN BOL CONT 02 CONN BOL CONT 02 CONN BOL CONT 02 CONN BOL CONT 02 PIN AAMP1 A4MP3 A4MP3 A4MP3 A4MP4 A4MP6 A4MP6 EXTRACTOR, YELLOW See introduction to this section for ordering information.

Table 6-3, Replaceable Parts



Indicates factory selected value.



Reference Designation	HP Part Number	Deed	ription
A4Q1 A4Q2 A4Q3 A4Q3 A4Q4 A4Q8	1683-0075 1683-0075 1683-0078 1688-0188 1684-0298	TRANSISTOR, DUAL PNP TRANSISTOR, DUAL PNP TRANSISTOR, DUAL PNP N-CHANNEL JFET TRANSISTOR, DUAL NPN	
A4Q6 A4Q7 A4Q8 A4Q9 A4Q10	1883-0318 1883-0078 1885-0423 1888-0423 1888-0423 1888-0423	TRANSISTOR, DUAL PNP TRANSISTOR, DUAL PNP N-CHAN E-MODE MOSFET H-CHAN E-MODE MOSFET N-CHAN E-MODE MOSFET	
A4Q11 A4Q12 A4Q12 A4Q14 A4Q16 A4Q16	1855-0423 1853-0451 1854-0477 1858-0386	Not Assigned N-CHAN E-PODE MOGFET TRANSISTOR, PNP Not Assigned TRANSISTOR, NPM N-CHAN JFET	
A4R1 A4R2 A4R3 A4R4 A4R4 A4R5	0898-7284 0698-7284 0698-7284 0698-7285	100K.06W RESISTOR 100K.06W RESISTOR 100K.06W RESISTOR 100K.06W RESISTOR 110K.06W RESISTOR Not Asugaed	
Ала Алар Ала Ала Алар Алар	2100-3753 0696-7280 0696-7272	TRIMMER RESISTOR 177 200K 86.1K 06W RESISTOR Not Assigned Not Assigned 31 6K 06W RESISTOR	
A48)1 A4812 A4813 A4814 A4814	0596-7252 0596-7254 0596-7255 0596-7255	12.1K 05W REGISTOR 6.62K 06'Y REGISTOR Not Assigned 909 05W REGISTOR 13.3K 05W REGISTOR	
A4816 A4817 A4818 A4819 A4820	0698-7263 0698-7260 0696-7260	23.7K .06W RESISTOR TOK 06W RESISTOR TOK 06W RESISTOR Not Assigned Not Assigned	
84821 84822 84823 84824 84826	0698-7212 0698-7243 0698-7212	Ict Assumed Not Assumed 100.06W RESISTOR 1.PGK 05W RESISTOR 100.05W RESISTOR	
аля26 Аля27 Лая26 Дая29 Аля30	0698-7212 0698-7243 0698-7238 C898-8827 0698-7238	100 08W RESISTOR 1.90K 08W RESISTOR 1.21K 08W RESISTOR 1M 125W RESISTOR 1M 05W RESISTOR	
A4R3) A4R32 A4R33 A4R34 A4R35	0698-7243 0698-7248 0698-7242 0698-8824 0698-7270	1 96K 06W RESISTOR 3.16K 06W RESISTOR 1.96K 06W RESISTOR 862K .124W RESISTOR 26.1K 06W RESISTOR	
л4738 Алгэт Алгэт Алгэв Алгэ Алга	0896-7284 0698-7234 0698-7224 0698-7212 0698-3483	100K OGW RESISTOR 825 OGW RESISTOR 316 OGW RESISTOR 100 OGW RESISTOR 196K 128W RESISTOR	
лапат Лапа2 Лапа3 Лапа Лапа5	0668-7243 0698-7233 0698-7233 0698-7260	1.56K 05W RESISTOR 750 05W PESISTOR 750 .05W RESISTOR 10K 0LW RESISTOR Not Assigned	
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# Table 6-3, Replaceable Parts

Reference Designation	HP Part Number	Description
A41146 A41147 A41148 A41148 A41148 A41149 A41150	0696-6969 0698-7238 0698-7247 2100-3749	SIBK JESW RESISTOR IK JOW RESISTOR 2.87K JOBY RESISTOR TRIMMER RESISTOR 17T SK Not Abagned
A4R51 A4R52 A4R53 A4R54 A4R54	0696-7237 0696-7246 0696-7248 2100-3759	1.1K. OBW RESISTON 2.61K OBW RESISTON 3.61K DBW RESISTON 7.61K DBW RESISTON TRIMMER RESISTON 37T EX Not Assigned
A4766 A4767 A4768 A4769 A4769	0698-7243 0698-7243 2100-2216 0698-7263	Not Assigned 1.56K OSW RESISTOR 1.66K OSW RESISTOR TRIMMER RESISTOR 17 6K 5.11K OSW RESISTOR
A4861 A4862 A4863 A4864 A4864 A4866	0696-7242 0698-7265 0698-7257 0698-7251	1.78K DEW RESISTOR 16.2K DEW RESISTOR 7.8K DEW RESISTOR 4.22K DEW RESISTOR NOT Assigned
AARGG AARG7 AARG8 AARG8 AAR70	0698-7247 0811-1887 0690-7243 0698-7285 0698-7243	2.87K .05W RESISTOR 0 OKM. 95W RESISTOR 1.96K .05W RESISTOR 110K .05W RESISTOR 1.96K .05W RESISTOR
A4871 A4872* A4873 A4874 A4876	0696-7223 0696-7246 0767-0421 0696-7212 0696-7265	287 06W RESISTOR 2.61K 06W RESISTOR 825.123W RESISTOR 110.06W RESISTOR 16.2K 05W RESISTOR
А4176 А4177 А4178 А4179 А4179 А41780	0698-7246 0698-7219 0698-7277	2.51K.06W RESISTOR Not Assigned 196 06W RESISTOR 61.1K.06W RESISTOR Not Assigned
A4R81 A4R82 A4R83 A4R84 A4R86	0668-7251 0668-7269 0668-7267 0698-7267 0698-7274 0698-3440	4.22K 08W RESISTOR R3.7K .08W RESISTOR 19 4K 08W RESISTOR 2.67K .08W RESISTOR 196 .125W RESISTOR
A4R86 A4R87 A4R88 A4R89 A4R99 A4R90	0668-7584	Not Assigned 100K 05W RESISTOR Not Assigned Not Assigned Not Assigned
A4R91 A4R92 A4R93 A4R94 A4R95		Nat Assigned Nat Assigned Nat Assigned Nat Assigned Nat Assigned
AAR96 Aar97 Aar98 Aar99 Aar99	0692-7550	Nat Assigned Nat Assigned Nat Assigned Nat Assigned Nat Assigned 10K G6W REGISTL
A417101 A417102	0698-7284 0698-7246	100K DEW RESISTOR 2.16K DEW RESISTOR



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# Table 6-3, Replaceable Parts

Reference Designation	HP Part Number	Description
A4B71	0637-0119	тнелывтов вк. лърва с
А4ТР1 А4ТР2 А4ТР3 А4ТР4-7	0360-0838 0360-0838 0360-0838 1281-7624	PCB TEBT POINT PCB TEBT POINT PCB TEBT POINT TRBT POINT HEADER
AAU) AAU2 AAU3 AAU4 MAU6	1826-0010 1826-0010 1826-1128 1826-1186 1826-1186 1826-0018	Мрі мих.24 Мрі мих.24 LF 412 риль, ор-Амр Рмі бу-05 Рмі ор-11 оцар ор-Амр
A4U6 A4U7 A4U8 A4U9 A4U9 A4U10	1826-1186 1826-1186 1820-1428 1820-1216 83892-60087	PMI 5W-06 PMI 5W-06 TTL OUAD 1-INPUT NAND TTL J-8 DECODER TTL PAL20X8, PROGRAMMED
A4V)) A4V)2 A4V)3 A4V)4 A4V16	1826-0782 1826-0982 1828-1048 1828-0782 1828-0782	АD7642 12-ВІТ DAC Рмі OP-37 Рмі OP-97 Рмі OP-97 LF 412 DUAL OP-AMP
AU18 AU17	1826-1221 1826-128	LM 311 COMPARATON LF 412 DUAL OP-AMP
4741 4742 4743 4744	1902-0049 1902-0049 1902-3070 1902-3070	6.18V ZENER DIODE 6.18V ZENER DIODE 4.22V ZENER DIODE 4.22V ZENER DIODE
NAWI NAW2 NAW3	8159-0006 1450-1489 1450-1489	O OHM RESISTOR SERVICE JUMPER SERVICE JUMPER
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#### Table 6-3. Replaceable Parts

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Reference Designation	HP Part Number	0 D	aly	Description	Mfr Gode	Mfr Part Number
AS	83892-60008	•		BOAND ABBEMBLY-FM	<b>F</b> 8480	\$38\$2+60008
ABC1 ABC2 ABC3 ABC4 ABC5	0160-0678 0160-0678 0160-4084 0160-0948 0160-0948	4 1 8 2 4	•	CAPACITOR FXD 047UF # FON BOVDC CER CAPACITOR FXD 8200HF # FON IOVDC CER CAPACITOR FXD 1 UF # FON EVDD CER CAPACITOR FXD 910FF # 6% IOVDC MICA CAPACITOR FXD 947UF # 6% IOVDC CER	58480 58480 58480 58480 58480 58480	0160-0575 0160-0572 0160-4084 0160-0945 0160-0975
A8C8 A8C7 A8C8 A8C8 A8C9 A8C9	0160-9247 0160-3879 0160-3879 0160-3879 0160-3879	17777	٩	CAPACITOR-FXD 3 9PF & E8PF 600YDG CEN CAPAICOTR-FXD 01UF & F0% 100YDG CEN CAPACITOR-FXD 01UF & F0% 100YDG CEN CAPACITOR-FXD 01UF & F0% 100YDG CEN CAPACITOR-FXD 01UF & F0% 100YDG CEN	28480 28480 28480 28480 28480 28480	)160-8247 G100-3879 G160-3879 G160-3879 G160-3879 G160-3879
A6C11 A6C12 A6C13	0140-0158	62	1	CAPACITOR-FXD 500PF # A6% 300VDC MICA CAPACITOR-FXD 30PF # 8% 300VDC MICA NOT A55IGNED	72138 68480	DM18F201 J0300WW1C4 0160-0199
ABCIA ABCIA	0121-0448 0160-3879	6 7	)	CAPACITOR-V TRUR-CEN 4 8-50PF 160V CAPACITOR-FXD DIUF ± 50% 100VDG CER	58480 58480	0121-0446 0150-3879
ABC16 ABC17	0160-3879 0160-3879	7		CAPACITON-FXD OLUF + FON 100VDC CEN CAPACITON-FXD OLUF + FON 100VDC CEN	58480 38480	0160-3879 0160-3879
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Table 6-3. Replaceable Parts

Reference Deelgnation	HP Part Number	D D	aty	Devaription	Mfr Code	Mfr Part Number
NIC) 8 NIC1 8 NIC1 9 NIC1 0	0180-3478 0180-3478	7	•	CAPACITOR PRD 010F #30% TOOVDC CER NOT ASSIGNED CAPACITOR PRD A FPF #38PF BOOVDC CER	28480 28480	0140-3878 0160-3248
MC3) MC33 MC33 MC34 MC38	0160-4064 0160-4064 0160-3879	•		NOT ASSIGNED HOT ASSIGNED CAPACITOR-FRD. IUF & ION BOYDC CEN CAPACITOR-FRD. IUF & ION BOYDC CEN CAPACITOR-FRD. DI UF & ION TOOYDC CEN	18480 18480 18480	0)80-4084 0180-4084 -0180-3879
4630 4637 4638 4639 4630	0180-3874 0180-4084 0180-4084 0180-2817 0180-2817		4	CAPACITOR FXD 10PF & BPF BOOVDC CER CAPACITOR FXD 1UF #20R BOVDC CER CAPACITOR FXD 1UF #20R BOVDC CER CAPACITOR FXD BUF#10R 38VDC TA CAPACITOR FXD BAUF#10R 38VDC TA	28480 28480 28480 28088 28088 28088	G) 80-3874 01 80-4084 01 80-4084 048-631 838K Danacai 838K
4C3) 4C33 4C33 4C34 4C38	0180-2817 0180-2817 0180-2207 0180-0474 0180-0474		1	CAPACITOR FRD 8.8UF±10% 38VDC TA CAPACITOR FRD 8.8UF±10% 38VDC TA CAPACITOR FRD 100UF±10% 10VDC TA CAPACITOR FRD 18UF±10% 20VDC TA CAPACITOR FRD 18UF±10% 20VDC TA	25088 25088 55288 26480 28480	0678031838x D678031838x 15001078801072 0180-0474 0180-0474
AC38 AC37 AC38 AC38 AC38 AC40	0)80-0474 0180-0474 0180-0474 0180-0474 0180-0474 0180-3879			CAPACITOR-PAD IBUF±10% 30VOC TA CAPACITOR-PAD IBUF±10% 20VOC TA CAPACITOR-PAD IBUF±10% 20VOC TA CAPACITOR-PAD IBUF±10% 20VOC TA CAPACITOR-PAD 01UF 220% 100VDC CER	28480 38480 28480 28480 28480	0180-0474 0180-0474 0180-0474 0180-0474 0180-0474 0180-3879
4C11 8CR1 8CR3 8CR3 8CR4 8CR4	0180-2248 1901-0033 1901-0033 1901-0047 1901-0047 1901-1088	2	ł	, CAPACITOR-FXD A.7PF B.25PF BOOYDC CER DIODE-GEN PRP 180V FOGMA DO-Y DIODE-GEN PRP 180V FOGMA DO-Y DIODE-BWITCHING FOV 78MA 10NB DIODE-BWITCHING FOV 78MA 10NB DIODE-BWITCHING 1NA 150 BOY 200MA ANS	28480 78480 78480 78480 78480 96480 90043	0180-2249 1901-0033 1901-0035 1901-0047 1901-0047 1901-0047
BCRA BCRJ BCRA BCRA	1901-1098 1901-1098 1901-1098 1901-0938			LHOOE-BANTCHING INAL BO BOY 200MA ANS DIODE-BWITCHING INAL BO BOY 200MA ANS	00044 00044 00044 28480	1N4180 IN4180 IN4180 IN4180 IN60-0938
8 K 1 8 K 2	0480-0818		1	NELAY/REED TA BOOMA TOOVDC BVDC-COIL NELAY/REED ZA BOOMA BOVDC BVDC-COIL TOVA	28480	0480-0818
81,1 61,2 61,3 61,4 61,6	9100-1828 9100-1818 9100-1818 9100-1818 06802-80001 9100-1818	011181	1	INDUCTOR RECHALD 33UH BE JERDX388LG INDUCTOR RECHALD SAUH BE JERDX388LG INDUCTOR RECHALD SAUH SON COLLTOR RECHALD SAUH SON	38480 38480 38480 78480 38480	9100-1826 9100-1826 9100-1818 9100-1818 9100-1818
BLO	8100-1618	2		INDUCTOR NF-CH-MLD 4.8UH 10%	28480	8100-1618
	8040-8881 8000-9043 4330-0148 4330-0148 4330-0148		•	Extractor PNIPC Board Extractor Insulator-Bead glass Insulator-Bead glass Insulator-Bead glass	38480 28480 28480 28480 28480 28480	6040-8881 6000-9043 4330-0148 4330-0148
	4330-0148 4330-0148 4330-0148			Hulator Read Glass Neulator Read Glass Hulator Read Glass	28480 2855C 78480	4330-0148 4330-0148 4330-0148
(G) (G2 (G4 (G4	1884-0838 1884-0838 1884-0838 1884-0838 1884-0838 1884-0478	0000	4	Transistor dual HPH PD-750MW Transistor dual HPH PD-750MW Transistor dual HPH PD-760MW Transistor dual HPH PD-760MW Transistor dual HPH PD-750MW	28480 28480 28480 28480 28480 28480	1854-0520 1854-0520 1854-0520 1854-0520 1854-0520
n) N2 N3 N6 N6 N6 N6 N6 N6 N6 N6 N6 N6 N6 N6 N6	0488-0083 0484-3184 0484-3184 0484-3184 0484-3184 0787-0438 0787-0438 0787-0438 0787-0438 0787-0438 0484-3188 0484-0124	8000044480	2 2 2 4	MESIETOR 1.88K 1%.128W F TC=0±100 MESIETOR 4.32K 1%.128W F TC=0±100 MESIETOR 4.32K 1%.128W F TC=0±100 MESIETOR 4.22K 1%.128W F TC=0±100 MESIETOR 4.22K 1%.138W F TC=0±100 MESIETOR 6.81K 1%.138W F TC=0±100 MESIETOR 10.1%.138W F TC=0±100 MESIETOR 10.2K 1%.128W F TC=0±28 MESIETOR 10.2K 1%.128W F TC=0±28	24848 24848 24848 24848 24848 24848 24848 24848 24848 24848 28480 28480	C4-1/B-TC-1881.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 L4-1/B-TC-4221.7 C4-1/B-TC-4221.7 C4-1/B-TC-4221.7 C4-1/B-TC-4221.7 C4-1/B-TC-4221.7 C4-1/B-TC-4221.7 C4-1/B-TC-4221.7 C4-1/B-TC-4221.7 C4-1/B-TC-4221.7 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-4221.8 C4-1/B-TC-42
N11 N12 N12 N14 N16	0688-3168 0688-003 0698-3448 0787-0384 0787-0384		2	NEBETOR & 84K 1% .12BW F TC=0±100 MEDIETOR 1.86K 1% .12BW F TC=0±100 AEDIETOR 383 1% .12BW F TC=0±100 AEDIETOR 383 1% .12BW F TC=0±100 AEDIETOR 81.1 1% .12BW F TC=0±100	24848 44848 44848 54848 54848	C4-1/4-T0-441.F C4-1/4-T0-441.F C4-1/4-T0-163.F C4-1/4-T0-163.F C4-1/4-T0-161.F
N   0 N 7 N 1 N 2 N 2 O	0787-0442 0787-0442 2100-3748 0787-0488	8 9 6 7	3	NOT ABBIGNED MEDISTOR 10K 1%, 125W F TC=0±100 REDISTOR 10K 1%, 125W F TC=0±100 REDISTOR 10K 1%, 125W F TC=0±100 REDISTOR B1.1K 1%, 125W F TC=0±100	74548 74548 78480 21,448	C4-1/8-T0-1002-# C4-1/8-T0-1002-# 2100-2748 C4-1/8-T0-8112-#
N31 N32	0488-3138 0488-4360 0488-3181		1	NESIGTOR 17.8K 1%.128W F TC=0±100 NESIGTOR 10K.1%.128W F TC=0±28 NESIGTOR 2.87K 1%.128W F TC=0±100	24848 28480 24840	C4-1/& TC-1782+F 0688-0360 C4-1/& TC-2871+F

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Change 28

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# A4 ALC (AUTOMATIC LEVELING CONTROL) ASSEMBLY CIRCUIT DESCRIPTION

# INTRODUCTION

The A4 ALC assembly is part of a closed loop power leveling function that controls the RF output power amplitude. The following describes both loop operation, including some components external to the A4 assembly, and the A4 assembly circuits.

### GENERAL

The power control and power leveling circuits can be broken into two categories: internal loop circuitry, and components external to the loop (see Figure U-24).

The ALC power level reference leg establishes the desired power level. To use this leg, either press the plug-in [POWER LEVEL] key and rotate the RPG, or enter the desired reference using the sweep oscillator front panel data entry keys. The ALC leg is not an interdependent part of the loop.

The ALC loop feedback path samples the actual RF output power and produces a voltage proportional to the RF amplitude. This voltage is converted to log scale and compared with the power level reference signal. If the voltages at the summing junction are not of equal magnitude, an error voltage is generated that is amplified and converted to a current drive for the RF modulators, which vary the transmitted RF power to correct the error.

# POWER LEVEL REFERENCE, BLOCK B

A 12-bit DAC (U11) is controlled by the sweep oscillator microprocessor. Depending on the plug-in operating mode, the DAC's output is summed with:

- AM
- power sweep
- detector compensation (vs frequency)
- an offset voltage used to calibrate the loop at the extreme low end of its power range.
- external and power meter leveling

The reference voltage is negative, decreasing approximately 300 mV per dB change in power level. A thermistor compensates for the log amp's 0.3%/*C temperature coefficient. R17 sums the reference and feedback voltages.



# **DIGITAL CONTROL/DECOPING, BLOCK D**

U9 decodes lines from the sweep oscillator microprocessor to enable U10, a 24-pin PAL, whose 10 outputs control analog switches and logic gates on the board. U10 latches in data at each bandswitch or when the ALC mode is changed from the front panel.

U10 logic:

<ul> <li>B1 always h</li> </ul>	lgh
---------------------------------	-----

- PM high in power meter leveling
- LINT low in internal leveling
  - INT the complement of L INT L SLP low in internet leveling (i
    - low in internal leveling (L SLP -L INT +B1)
- EXT high in external leveling
- L PULSE EN low when pulse modulation is enabled (always)
- MUX A0, A1, A1B see Table 8-12

	DATA BUS						
Mux A0	Mux A1	Mux A1B	PM	Leveling Mode			
Н	н	н	L	INT 0 (not used)			
L.	Н	Н	L	INT I			
H	Ĺ.	L	Ļ	EXT			
L	L.	Н	Н	PM 0 (not used)			
- L	I.	н	Н	PM I			

Table 8-12, Leveling Control Lines

# LOGARITHMIC FEEDBACK AMPLIFIERS, BLOCK G

There are two logarithmic feedback amplifiers:

### The Power Meter Logger

U5C and Q1, switched in by U4A, form a non-inverting logger that amplifies a positive voltage. R30 forms a voltage divider with the power meter's internal source impedance, keeping the logger input voltage less than 0.5V. R29 applies a small positive voltage to the logger input when the plug-in is not in power meter leveling.

When the logger input is negative, CR6 provides feedback for U6C, protecting Q1, U17A forms a buffer (with a gain of five) and the phase lead network for loop compensation. In power meter mode, U6A switches the power meter logger into the loop summing node through R37.



# The Dual-Slope Logger

U12 (a non-inverting buffer with a gain of approximately seven), 13, and 14 form the internal dual-slope logger. Q8, Q9, and Q10 switch between the internal and external detector returns. GR1 clamps U13, similarly to CR6 in the power meter logger. Q5 forms a dual current source to bias the logger's breakpoint. The breakpoint current is set by R49 and R50, and selected by U2A, R46 sets the logger zero-crossing current, which corresponds to a -2 mV detector input voltage.

U14 is a non-inverting buffer whose gain is adjusted by R54 and R55 (selected by U2B) for power level calibration. CR11, R44, and C42 clamp the logger output from going too far negative. CR9 provides feedback for U14. In internal and external leveling, U6C switches the internal logger to the loop summing node through R51, and U6D switches the internal logger to the summing node through C17 (a differentiating capacitor), Q4, and R39, Q4 acts as a sample and hold switch for the charge on C17 when 27.8 kHz square wave modulation is used in the power meter leveling mode.

#### MAIN ALC AMPLIFIER, BLOCK C SAMPLE AND HOLD DRIVER, BLOCK L

C22 and R64 set the time constant for integrator U16A, whose input is the weighted sum of the reference voltage and the logger output voltage. VR1 and VR2 clamp to +7V on the integrator output. When W3 is removed and power meter leveling is used, U6B switches in C23 to increase the time constant, lowering the loop gain. Q16, C20 and C40 sample and hold in pulse modulation, 27.8 kHz square wave modulation, and RF blanking during bandswitch and retrace.

Q16 and Q4 are controlled by the sample and hold driver. The collectors of Q6 drive Q16 and C20 differentially. R59 adjusts the differential signal amplitude to C20, compensating for the gate-source capacitance of Q16, C19 and C40 optimally match the rise time on the Q6 drive lines. Q6 is a switching circuit (one-half of the pair is always off).

The loop is on hold when L RFB is active (bandswitces and blanking pulses), and when the RF is turned off in square wave modulation or pulse modulation. To keep the loop in the hold mode long enough for all switching translents to subside, each input to Q6 is delayed by one of three delay networks, one each for square wave modulation, pulse modulation, and blanking.

### BAND 1 PIN MODULATOR DRIVER, BLOCK J

The output of the current source formed by U17B, Q7, and Q15 is approximately proportional to the exponential of the input voltage (with a scaling factor). C35 and R71 provide stability for U17B, and help reduce residual AM on the RF output. R72 adjusts the gain of this circuit.

Be careful when adjusting the value of R72 (factory select value); increasing the value reduces the stability margin of U17B, and reducing the value lowers the bandwidth and can, if lowered too much, also hurt stability, CR2 provides U17B feedback when the input is positive, and C26 compensates for parasitic capacitance at the inverting input of U17B to ground.

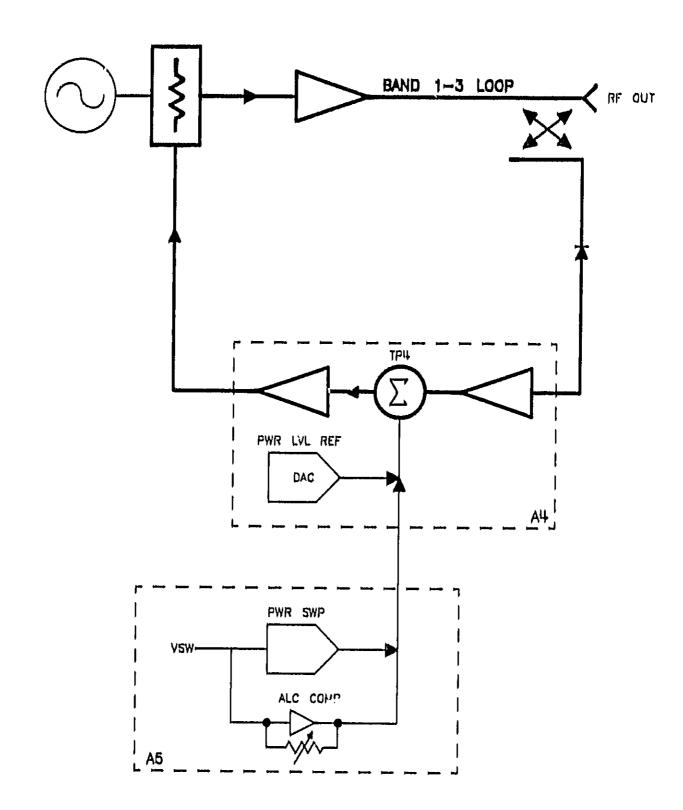
For open loop control and troubleshooting, remove W2 and connect TP6 to TP5 through a 10K resistor. The front panel power control then affects the output power over a small range,



HP 83590A

8-39/8-40





# NOTE

Darker lines represent the band 1-3leveling loop. Lighter lines represent circultry that contributes to, but is not contained within, the loop,

Figure 8-41. Simplified ALC Block Diagram

# A4P1 PIn-Outs

.

MP1				
PIN	SIGNAL	1/0	TO/FROM	FUNCTION
1 23	EXT DET RET	IN	J2	р
	EXT DET	IN	J2	В
2	L UNLVL	OUT	AGP1-40, A10J1-12	M
24	EXT CAL		A10J1-41	H
3 25	PWR REF	OUT	NOT USED NOT USED	C
4 26	AM	IN	P1-A4 NOT USED	C
5	PWR 5W/COMP	IN	A5P1-23	C
27	+5V	IN	A3P1-6,7	P
6 28	- 15V	IN	NOT USED P2-28	р
7	+ 10V	IN	P1+8	Р
29	L RF9	IN	P2+56	1,0
8 30	gnd dig gnd dig			р р
9	BD1	IN	A3P1-9	A, C
31	BD0	IN	A3P1-31	A, C
10	BD3	IN IN	A3P1-10	A, C
32	BO2		A3P1-32	A, C
11	BA1	IN	A3P1-11	A, C
33	BA0	IN	A3P1-33	A, C
12	BA3	IN	A3P1-12	A, C
34	BA2	IN	A3P1-34	A, C
13	BD5	IN IN	A3P1-13	A
35	BD4		A3P1-35	A
14	807	IN	A3P1-14	A
36	606	IN	A3P1-36	A
15 37	GND ANLG GND ANLG			թ թ
16 38	+15V	IN	NOT USED P2-29	Р
17	- 10V	IN	P1-13	р
39	- 40V	IN	P1-11	Р
18	L INST1	IN	A3P1-8	A, C
40	SQ MOD	IN	P2-26	K. O
19	MOD 1	OUT	A10-E1	N
41	L PULSE	IN	A6P1-25	K
20	INT DET 1	IN	CR1	6
42	INT DET RET	IN	CR1	8
21 43	- 10V REF	IN	NOT USED A8P1-3	С
22 44	MOD DRIVE	OUT	NOT USED NOT USED	L

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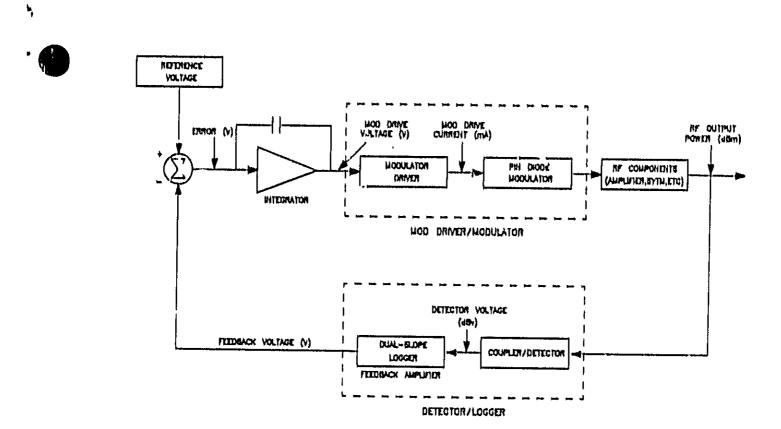
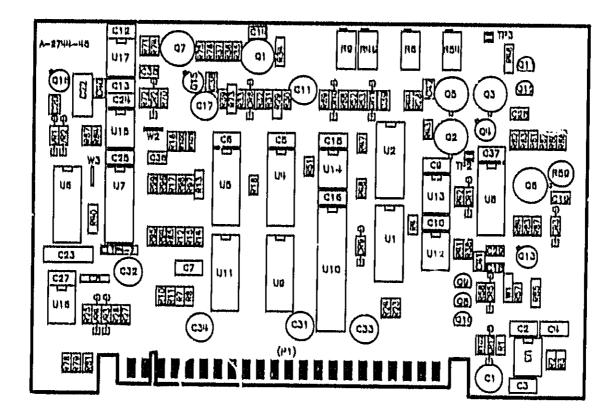


Figure 8-28. A4 ALC, Block Diagram



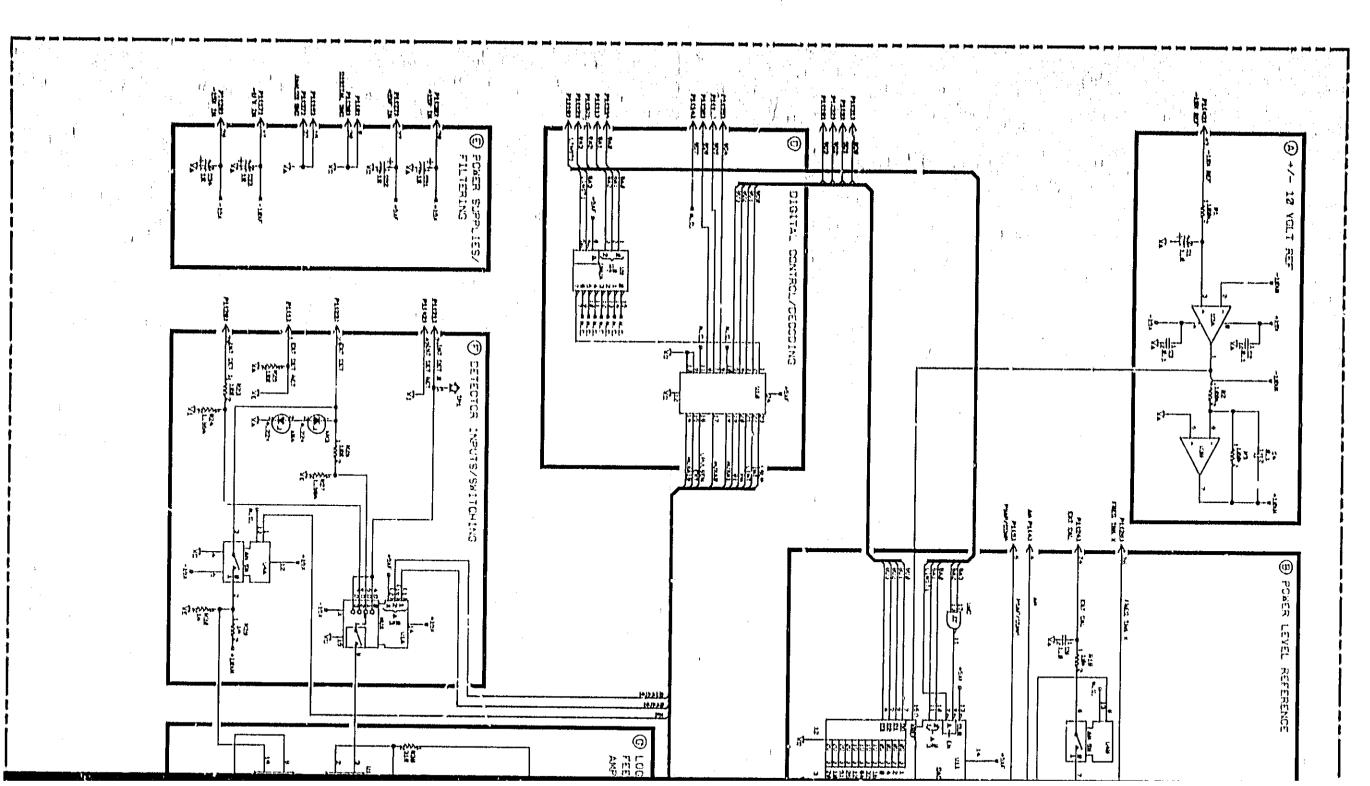
HP 83590A



HP Part Number 03590-00135

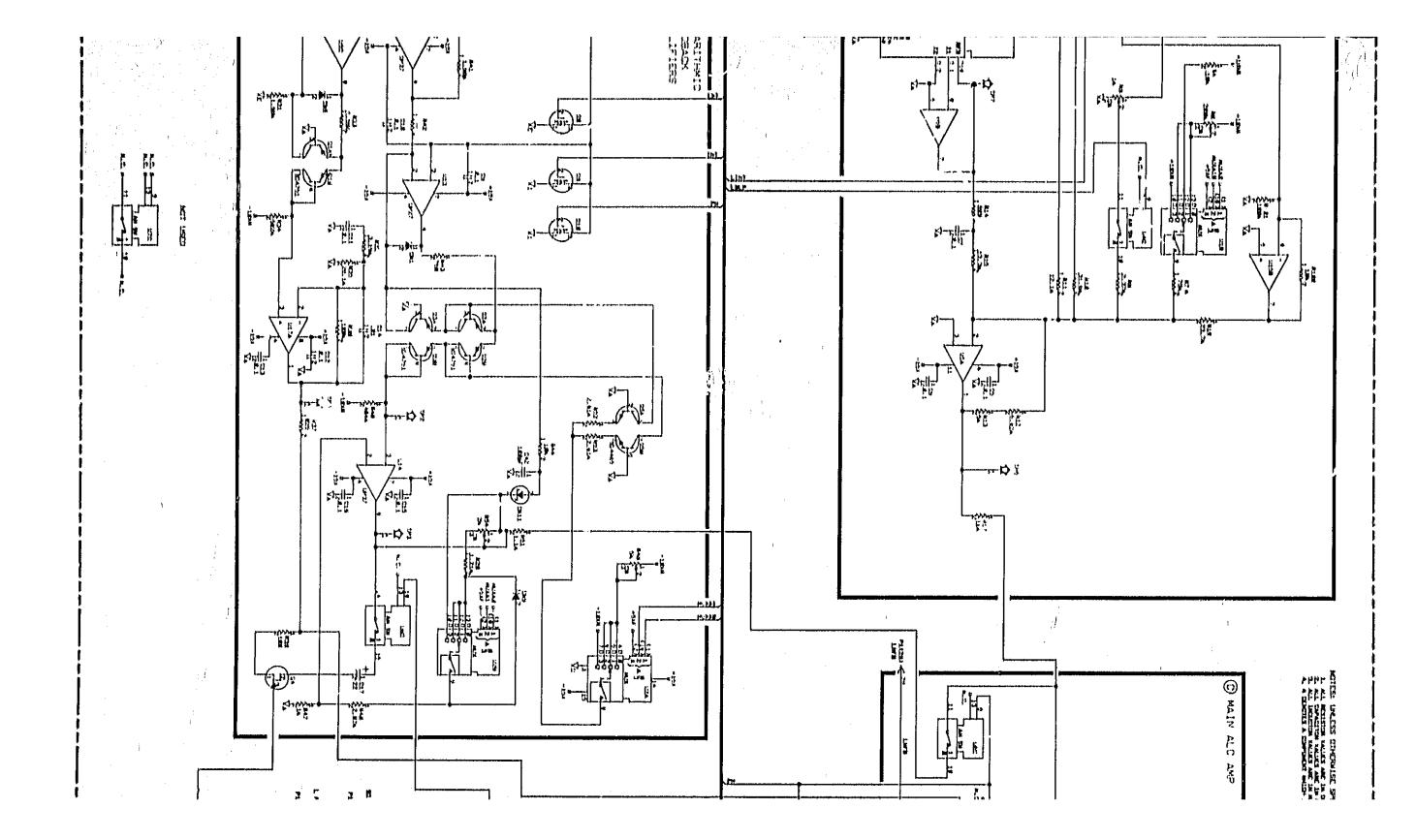
Figure 8-29. A4 ALC Component Locations

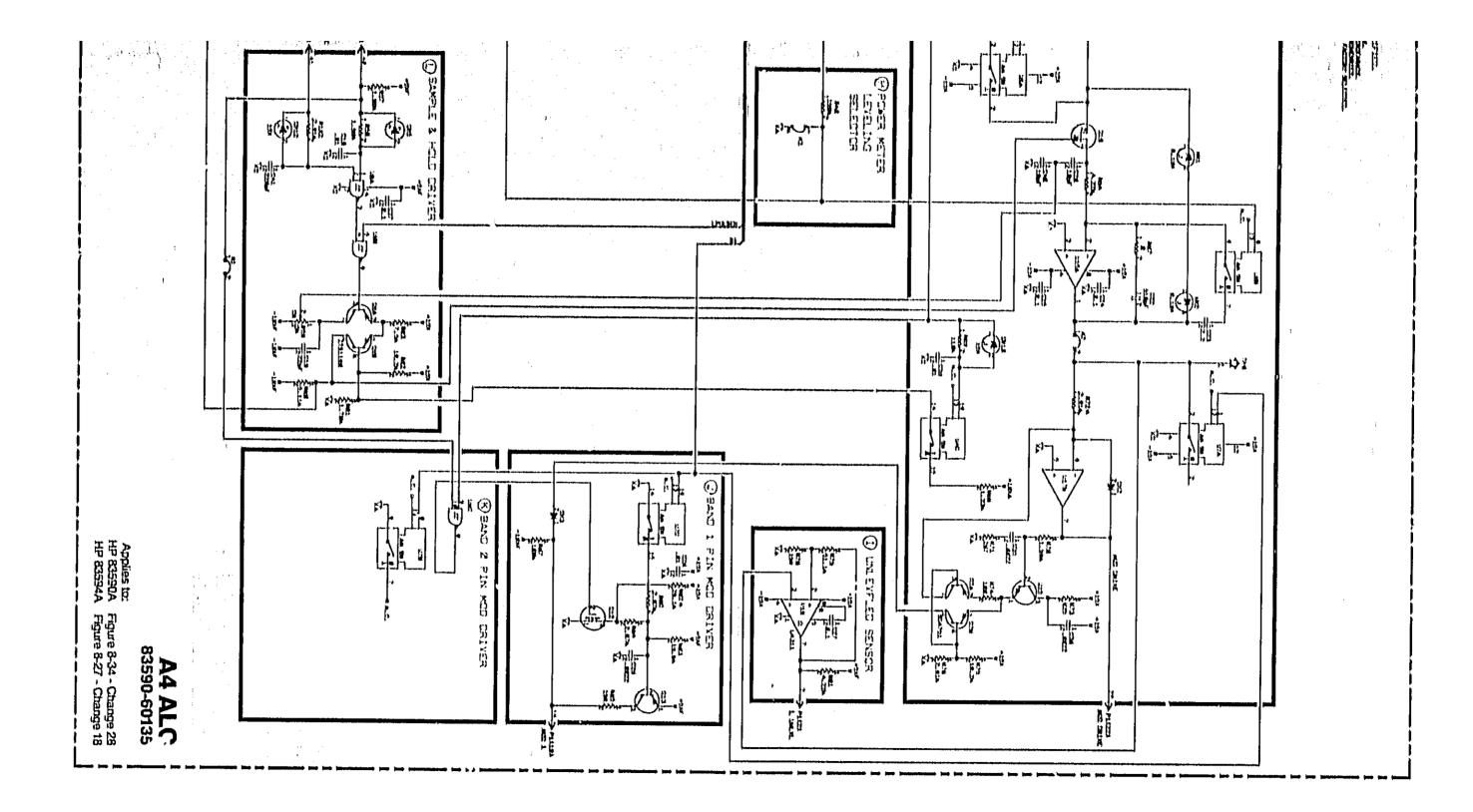
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INCLUMENTS II II I DESCRIPTION





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# MANUAL IDENTIFICATION

IIP Madel Number: 11P 83590A Manual Part Number: 83590-90005 Date Printed: February 1982

# **OHANGE 32**

Change 32 documents sorial praix 2030A.

This change documents an improvement to the AO YO driver assembly.

## INSTRUCTIONS

Replace the title page with the title page in this change packet,

Page 6-16, Table 6-3: Change A8C16 to 0160-3742, CD3, Capacitor-MPC 1.0µf 50V

Page 6-17, Table 6-3: Change A8R49, R50, and R51 to 0757-0465, CD6, Resistor 100K 1% 0.12W

Page 8-69; Replace Figure 8-71 with Figure 8-71 in this change packet.

HP Part Number 83590-90041 (For HP Internal Use Only) Part of HP Part Number 83590-90033

Change 32 32-1/32-2



# HP 83590A RF PLUG-IN (Including Options 002 and 004)

# SERIAL NUMBERS

This manual applies directly to HP 63590A RF plug-in having serial number prefix 2146A.

For instruments with serial prefix 2143A and below, refer to Section 7 Manual Backdating

For additional information about serial numbers, refer to INSTRUMENTS COVERED BY MANUAL in Section 1.

Change	Documents Prefix	Changa	Documanta Prafix	Change	Documents Prefix
1	2216A	17	2428A		
2	2217A	18	2451A		
3	2221A	10	2502A		
А	2233A	20	2507A		
5	2234A	21	2510A		
6	2249A	22	2543A		
7	2252A	23	2602A		
8	2306A	24	2619A		
0	2313A	25	26457		
10	2315A	26	2718		
11	2338A	27	2726A		
12	2410A	28	2809A		
13	2411A	29	N/A		
14	2411A	30	N/A		
15	2412A	31	2036A		
16	2413A	32	2830A		

Manual Changes Supplement Print Date: 1 NOV 1988

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MANUAL PART NO, 83500-00005 Microfiche Part Number 83590-90006

Printed: FEBRUARY 1982



# CERTIFICATION

Hewlett-Packard Company cartilies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other international Standards Organization members.

# WARRANTY

This Hewlett-Packard instrument product is warranted against detects in material and workmanship for a period of one year from date of delivery. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be detective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

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# LIMITATION OF WARRANTY

The loregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

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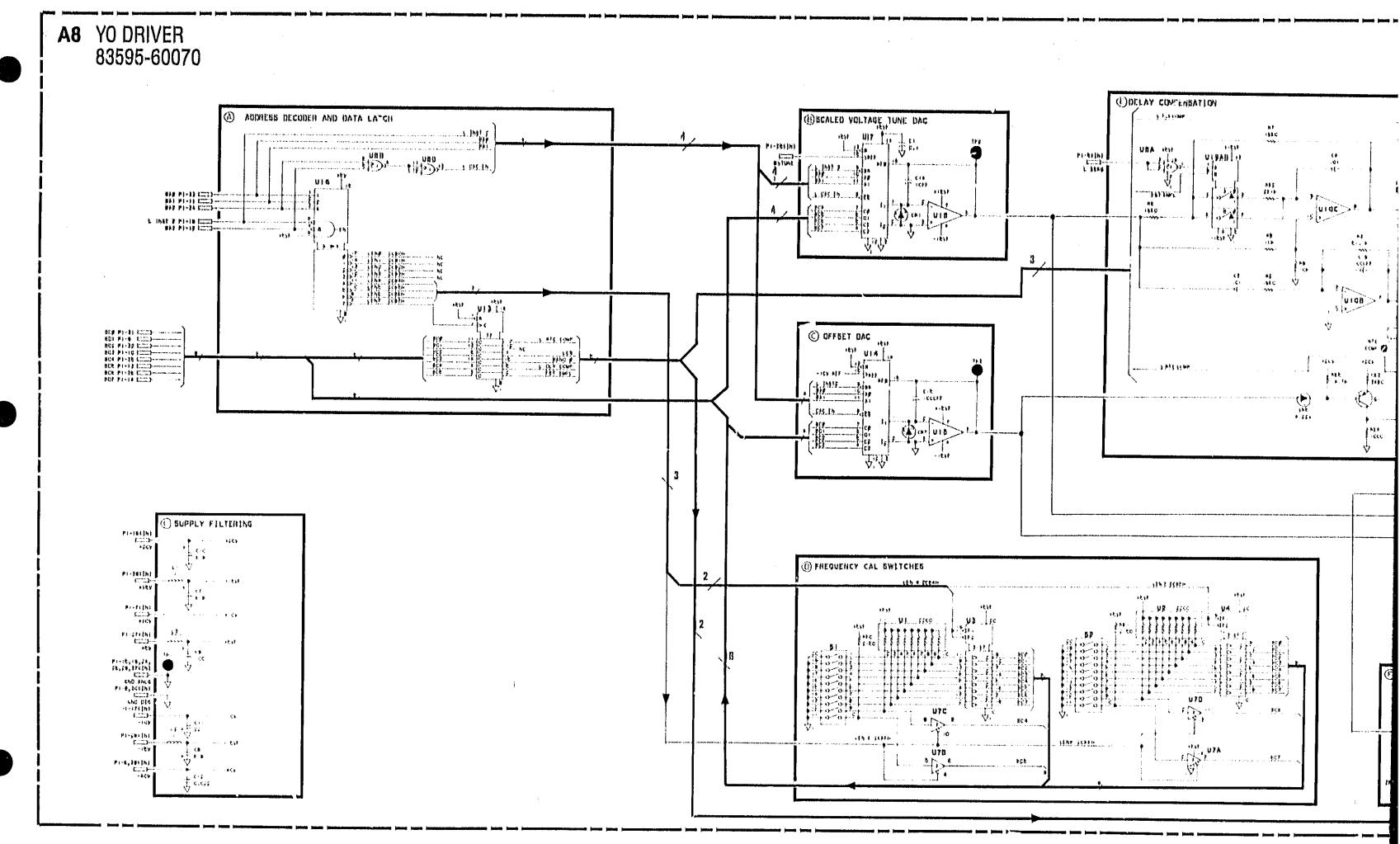
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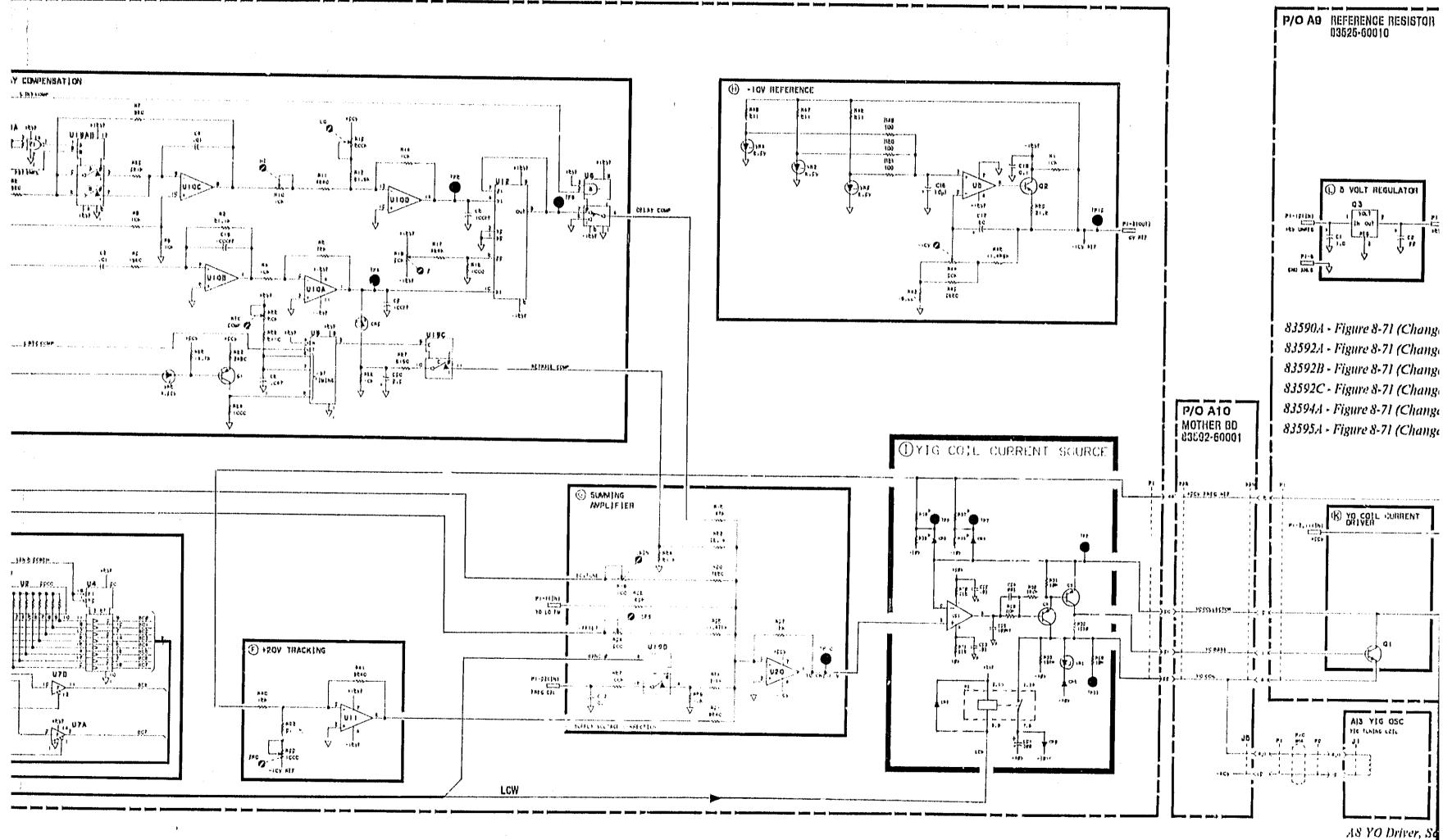
## ASSISTANCE

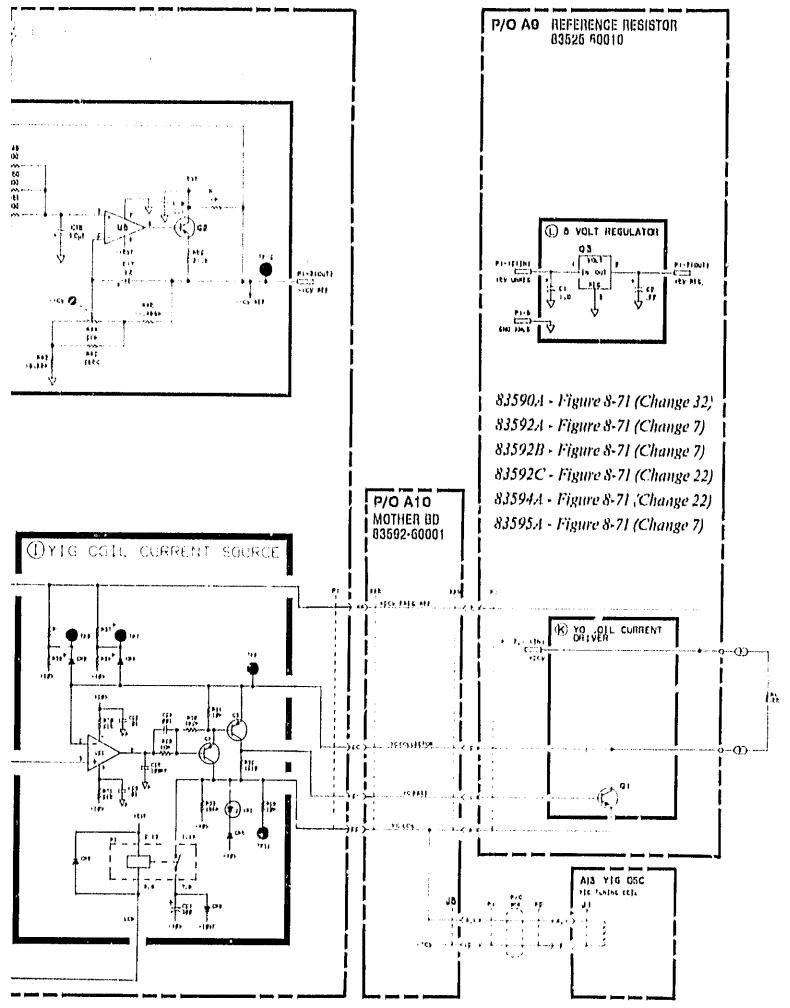
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BED 1







A8 YO Driver, Schematic Diagram

# SERVICE Information

# SECTION VIII SERVICE

# 8-1. INTRODUCTION

8-2. This section provides instructions for troubleshooting and repairing the Model 83590A RF Plug-in. Information includes circuit descriptions, troubleshooting procedures, block diagrams, schematics, and component location maps for each PC board assembly.

# WARNING

Adjustments or repairs inside the B35CA/B3590A with the top or bottom cover removed and the ac power connected should be avoided whenever possible. Any procedure regulring a cover to be removed from the instrument and ac power connected to the mainframe SHOULD BE PERFORMED ONLY BY QUALIFIED SERVICE PERSONNEL WHO ARE AWARE OF THE HAZARDS INVOLVED, With the ac power cable connected to the instrument, the sc line voltage is present on the terminals of the line power module on the rear panel, and at the LINE power switch, whether the switch is ON or OFF. The sc line voltage on these terminals can, if contacted, produce fatal electrical shock. You must also be aware that capacitors inside the instrument may remain charged even though the instrurient has been disconnected from its ac power source.

After you have completed a repair, check the instrument carefully to make sure all safety features are intact and functioning, and that all protective grounds are solidly connected.

# 8-3. SERVICE SHEETS

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8-4. Each service sheet pertains to a specific assembly and they are arranged in assembly number order. Table 8-1 provides a Service Sheet Index.

8-5. Service Sheets fold out and up to facilitate access to reference material. Block diagrams appear on the fold-down apron. Component location maps, PC board pin-edge connections,

and pertinent circuit information (e.g., waveforms) are found on the fold-up apron of the service sheet, with the schematic directly below. Circuit description and assembly level troubleshooting are located on pages immediately preceding the sevice sheet.

# 8-6. SCHEMATIC DIAGRAM NOTES

8-7. Figure 8-1, Schematic Diagram Notes, provides definitions to schematic symbols.

# 8-8. MNEMONICS

-8-9. The Motherboard Wiring List (Service Sheet A10) lists alphabetically and defines all 83590A signal mnemonics, references the pointto-point distribution of each signal to and from the PC board sockets and the cable connectors on the A10 Motherboard assembly, and identifies the signal source. This table is located on the A10 Service Sheet.

# 8-10. SERVICE AIDS

8-11. Two Extender Cable Assemblies, HP Part Number 08350-60034 (64 pin) and 08350-60035 (17 pin), are designed to power the RF Plug-in when it is removed from the 8350A Sweep Oscillator for troubleshooting. These service aids are recommended for convenience in servicing the 83590A.

8-12. A 44-pin extender board (HP Part No. 08350-60031) is available to allow access to printed circuit board assembly components while maintaining electrical contact with the Plug-in. This and other service aids are referenced in Section I, Table 1-3, of this manual.

# 8-13. TROUBLESHOOTING

The second s



Improper methods of discharging the -40 Volt supply may result in damage to the instrument. Refer to the 8350A Sweep Oscillator Operating and Service Manual for these procedures.

8-1

Assembly	Fig. No.	Assembly	Fig. No,
OVERALL		AG SWEEP CONTROL	
Circuit Description/Troubleshooting		Circuit Description/Troubleshooting	
Simplified Overall Block Overall Block Diagram	8-7 8-8	Block Diagram Component Locations Schematic	8-43 8-44 8-49
A1/A2 FRONT PANEL		A7/A9 YTM DRIVER/ REFERENCE RESISTOR	
Circuit Description/Troubleshouting		Circuit Description/Troubleshooting	
Block Diagram Front Panel A1 Component Locations Front Panel Interface A2	8-10 8-11	Block Diagram YTM Driver A7 Component Locations Reference Resistor A9	8-51 8-52
Component Locations Schematic	8-12 8-18	Component Locations Schematic	8-50 8-60
A3 DIGITAL INTERFACE		A8/A9 YO DRIVER/ REFERENCE RESISTOR	
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A4 ALC		RF SECTION	
Circuit Description/Troubleshooting		Circuit Description/Troubleshooting	
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		A16A1 Component Locations RI Section Schematic	8-75 8-76
A5 FM DRIVER		A10 MOTHERBOARD	
Circuit Description/Troubleshooting Block Diagram Component Locations Schematic	8-38 8-39 8-42	Component Locations Cable List Tuble 8-15 Wiring List Table 8-16 53590A	<u>8</u> .79
		Major Assemblies Locations	8-80

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	8	ASIC COM	PONENT SYMBOLOG	Y	
H, L, C	Resistance is in ohee), inductance is in (\$) (h benries, capacitance ()	<b>C</b>	Pin Edge Connector output of PC board.	E	FET Field Effect Tran- sistor (N-channel).
	in microfarads, unless otherwise noted		Indicates wire or cable color code same as resistor color		FET: Field Ethici Tran- sistor-Guarded gate- (N channel),
P/0 *	Part of. Indicates a factory set-	(jr)	code. First number indicates base color, second and third	55	Duat Transistor.
0-	ected component. Panel Control,		numbers indicate colored stripes.	$\bigcirc$	Transistor NPN
0	Screwdriver adjustment.	Q	Indicates shielding con- ductor for cables.	÷ C	Transistor PNP
	Encloses front panel designation.	~ <i>\</i>	Indicates a plug-in connection,	₩	Electrolytic Capacitor.
C	Encloses rear panel designation.		Indicates a soldered or mechanical connection.	-)  ^{!.} .	Toroid: Magnetic core inductor,
	Circuit assembly border- line,	¢	Connection symbol in- dicating a male con- nection.	-	
* pan any ina ina any	Other assembly border- line,		Connection symbol in- dicating a frinale con-	-4>	Operational Amplifier.
	Heavy line with arrows indicates path and dir- ection of main signal.	Ň	nection.	01 01	Fuse
<b>-</b>	Indicates path and dir- ection of main feed-	-**	Resistor.	و ا	Pushbutton Switch.
·	back.	- <b>^</b> tr	Variable Resistor.	$\gamma_{\circ}$	Toggle Switch,
- <u>Ļ</u> -	Earth ground symbol, Assembly ground, May	-	General purpose diode,	-620-	Thermal Switch
Ŷ	be accompanied by a number or letter to spec- ify a particular ground,	Þ	Breakdown Diode: Zener	(Ľ)	Summing Point.
<i>\</i>	Chassis ground,	·()//	Light-Emitting Diode.	$\sim$	Oscilletor; RPG (Rotary Pulse Generator).
<u>"/</u>	Represents n number of transmission paths,			(81)	Fan, Motor.
-	Test Point: Terminal provided for test probe.	(	SCR (Silicon Controlled Rectifier).	(( ))	Toroidal Transformer
		LOGI	C SYMBOLOGY		
<b>(b)</b>	AND Gate	1110	NOR Gate		Inverter
(i)	OR Gate	¥-)>	Exclusive OR Gate	0	Negation symbol. Line is active low.
4	NAND Gate	$\sum$	Buffer/Amphilier	[>	Indicated edge-sensitive input.

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Figure 8-1. Schematic Diagram Notes (1-of 3)

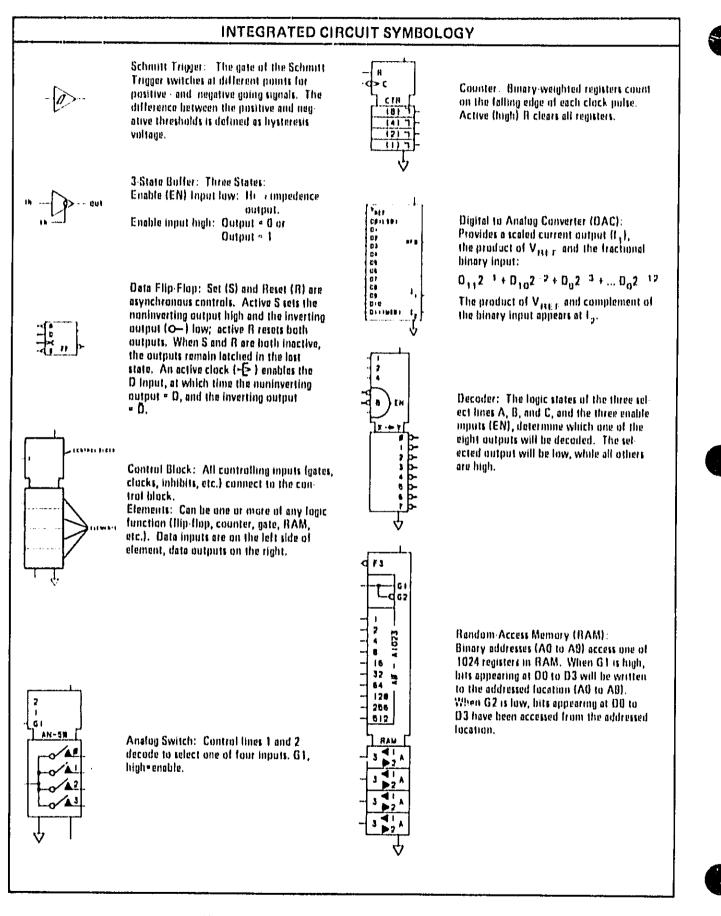


Figure 8-1. Schematic Diagram Notes (2 of 3)

	FUNCTION LABEL ABBREVIATIONS							
Ľ	Adder	♦	Open Collector	LED	Light-Emitting Diade			
	Amplifier/Buffer	<u>'</u> 1	Monostable Multivibrator	мих	Multiplexer			
Л.	Schmitt Trigger	800	Binary Coded Decimal	RAM	Randam-Access Memory			
8	AND	CTR	Counter	REG	Registor			
≥ı	OR	DVC	Digital-to-Analog Converter	ROM	Read Only Memory			
×1	Exclusive OR	FF	Flip-Flop	npg	Rotary Pulse Generator			
X-+Y	Encoder, Decoder	1/0	Input/Output					

	r	LINE L	ABEL ABBREVIATIONS		
ск, с	Clock Input	MSB	Most Significant Bit	т	Trigger Input (Monostable)
D	Data or Delay Input (Flip-Flop)	⁰	Output	wn	Write
EN	Enable	đ	Not Q Complement of Q	+1	Count Up
F	3-State Enable Input	R	Reset or Clear Input	-1	Count Down
G	Gating Input	RD	Read	3-ST	3-State (placed by function
LSB	Least Significant Bit	S	Set Input		

Figure 8-1. Schematic Diagram Notes (3 of 3)

8-14. Troubleshooting is generally divided into two maintenance levels in this manual. The first level isolates the problem to a circuit or assembly. SELF-TEST (described in paragraph 8-16) together with the Overall Block Diagram and Troubleshooting hints, helps to isolate the problem source to a particular assembly.

8-15. The second maintenance level isolates the trouble to the component. Operator-initiated tests, schematic diagrams, and circuit descriptions for each assembly aid in troubleshooting to the component level.

# 8-16. SELF-TEST

8-17. 8350A software provides microprocessor and operator-initiated checks. These checks verify the proper functioning of the majority of the 8350A and 83590A digital circuitry and a portion of the analog devices.

8-18. Whenever the 8350A is powered ON, or the front panel INSTR PRESET pushbutton is pressed, instrument SELF-TEST is initiated. Instrument SELF-TEST checks a number of circuits in both the 8350A and the 83590A. If a failure in the 83590A is detected during SELF-TEST, error code E001 will be displayed. Table 8-2 lists other error codes associated with the 83590A RF Plug-in.

8-19. If the front panel displays an error code, refer to the Overall Block Diagram and Trouble-shooting section. This section will help the operator to define the troubled area.

# 8-20. OPERATOR-INITIATED TESTS

8-21. The 8350A microprocessor services several operator-initiated tests of the 83590A to check functions which are not exercised during SELF-TEST. The tests may be initiated by making the appropriate key entry indexed in Table 8-3.

8-22. Access to most of the 83590A digital circuitry can be achieved through local programming with the following key entry commands:

Function	Key Entry
Hex Address Entry	SHIFT 0 0 M1 * (enter hex address)
Hex Data WRITE	M2 (enter data: two hex digits)
Hex Data READ	M3
Hex Data Rotation Write	M4
Hex Addressed Fast Read	M5

*To address a different location, press M1 and enter the new address, or use the increment keys  $\Rightarrow \Rightarrow$  to step to the new address.

By entering the Hex address location of a specific device, that device can be exercised. (Addresses are supplied next to the mnemonic on each schematic. Also, circuit descriptions usually include Address Decoder Tables to define the addresses used on that particular assembly.) Hex address entry must be made prior to any of the following:

Error Cade	Circuit Testad
1E001	Addresses 83590A ROM and reads Check Sum back to 8350A.
E050	Erroneous Front Panel Pushbutton Flag.
E051	Erroneous Front Panel Pushbutton Code received by 8350A Microprocessor.
E052	Checks for Timer Failure In A3.
E053	Checks PIA circuits in A3.

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Table S-2, Error Codes Associated with 83590A

8-6

Power Level DAC	٨.4	Аятр2
Power Sweep DAC	A5	А5ТРБ
Scale/Offset DACs	A7,A8	А7ТРІ, А7ТРУ, АВТР2, АВТР3
Address Decoder; checks major address decoder lines.	A7,A8	A3U6, A3U7, A3U9, A3U13
Address Decoder; checks individual board address decoders.	A4 thru A8	Address Decoders
Interrupt Control	A3	A3U4 pin 38
Bandswitch DAC	Α6	A61Pt
	Power Sweep DAC Scale/Offset DACs Address Decoder; checks major address decoder lines. Address Decoder; checks individual board address decoders. Interrupt Control	Power Sweep DAC     A5       Scale/Offset DACs     A7,A8       Address Decoder; checks inajor     A7,A8       Address Decoder; checks inajor     A7,A8       Address Decoder; checks individual     A4 thrn A8       board address decoders.     A3

Table 8-3. Operator Initiated Self Test Routines Available

# NOTE

Before addressing an 83590A component, determine whether or not the 8350A microprocessor can READ or WRITE to that particular device The majority of 83590A digital chips do NOT have both READ and WRITE capabilities.

- HEX DATA WRITE, M2, allows the operator to write any combination of hex data bytes to the addressed device. The outputs can then be checked to see if the device is functioning properly.
- HEX_DATA_READ, M3, allows the operator to read the outputs of an addressed device.
- HEX DATA ROTATION WRITE, M4, strobes a '1' (high state) through a column of zeroes (low states) to the addressed device. In effect, Hex Data Rotation Write is a rapid WRITE mode, exercising the addressed device in real time. The microprocessor inputs the data continuously, without servicing interrupts from the rest of the instrument. Latch enable lines, inputs, and outputs can be checked in this mode. Figure 8-2 illustrates the appropriate waveforms.

 HEX ADDRESSED FAST READ, M5, provides an operator-initiated check for verification of the data bus, in which the addressed device is clocked in real time. Latch outputs can be traced from the onboard location back through the data bus to the microprocessor. At each buffer, verify TTL level response to the enable pulse. Enable line waveforms are shown in Figure 8-3.

# 8-23. HEXADECIMAL

8-24. Hexadecimal is the number system used to locally address the 8350A and 83590A logic components. Available operator initiated self test routines are indexed in Table 8-3.

8-25. The hexadecimal system uses 16 digits: 0 through 9 and A through F. Since 16 is the fourth power of two, four-bit binary numbers can be expressed with one hexadecimal digit, making local programming easier. Table 8-4 provides hexadecimal conversions to binary and decimal equivalents.

8-26. When the 8350A is in the Hex Data WRITE mode (refer to paragraph 8-22), several front panel keyboard pushbuttons convert to hexadecimal digit entries. The Hex numbers assigned to the DATA ENTRY keys are shown in Figure 8-4.

# Model 83590A



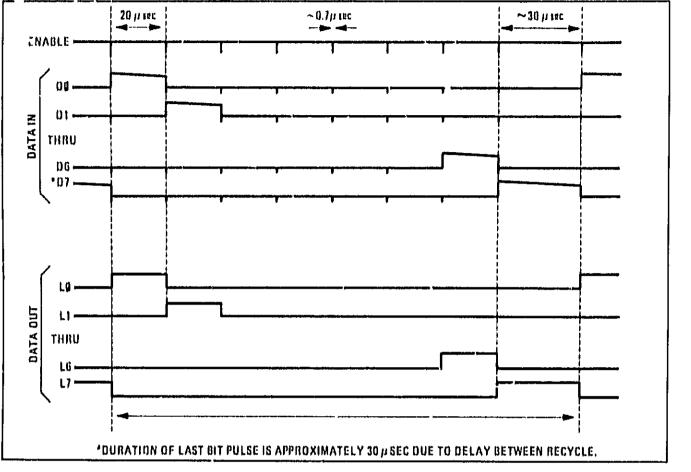


Figure 8-2 Hex Data Rotation Write Bit Pattern

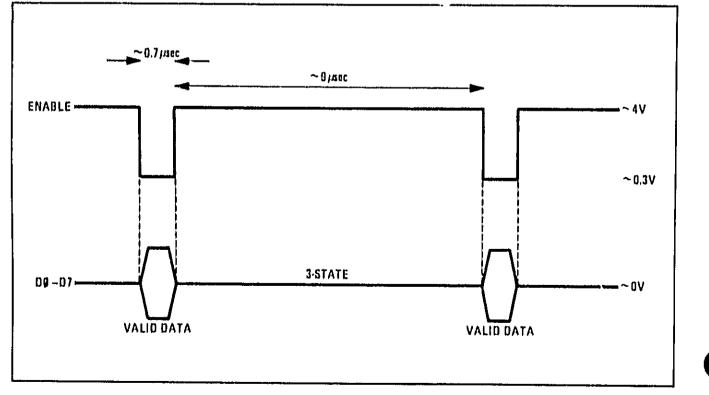


Figure 8-3. Hex Addressed Fast Read - Timing Diagram

8-8

Hexidecimal	Binary	Dacimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	. н
9	1001	9
Λ	1010	10
b	1011	I 11
С	1100	12
4	1101	13
E	1110	14
F	1111	15

Table 8-4. Hexadecimal Equivalents

Figure 8-4. Hex Entry Keys

# 8-27. RECOMMENDED TEST EQUIPMENT

8-28. Test equipment required to maintain the Model 83590A is listed in Section I. If the equipment listed is not available, equipment that meets the minimum specifications shown may be substituted.

# 8-29. REPAIR

# 8-30. Module Exchange Program

8-31. This instrument may be quickly repaired by replacing a defective module with a restoredexchange module. To support the module repair concept, Hewlett-Packard has set up a module exchange program.

8-32. The procedure for using the module exchange program is given in Figure 8-5. When you locate the defective module, order a replacement module through the nearest Hewlett-Packard sales office. The restored-exchange module will be sent immediately directly from a customer service replacement parts center. When you receive the exchange module, return the defective module in the same special carton in which the exchange module was received. DO NOT return a defective module to Hewlett-Packard until you receive the exchange module.

8-33. If you are not going to return the defective module to Hewlett-Packard, or if you are ordering

a module for spare parts stock, etc., order a new module using the new module part number listed in Table 6-3.

8-34. The Hewlett-Packard module exchange program allows you to obtain a fully tested and guaranteed restored-exchange module at a reduced price. (The reduced price is contingent upon return of the defective module to Hewlett-Packard.) Assemblies available for module exchange are listed in Table 6-1.

# 8-35. Replacing YO A13, YTM A12, YO Driver A8, or YTM Driver A7

8-36. Each YIG Oscillator (YO) or YIG Tuned Multiplier (YTM) requires a unique set of resistors to be installed on its respective driver board (A7 or A8) for proper YIG coil drive. The values of these resistors are documented on labels attached to the side of the 83590A near the RF section. If the driver assembly (A7 or A8) is replaced, the resistor header containing these resistors must be installed on the new board. Also, if the YO or YTM is replaced, the resistor header shipped with the YO or YTM must be installed on the driver board in place of the old resistors. (In some cases, some or all of the resistors may be deleted, depending on the drive requirements of the individual YO or YTM.)

Service

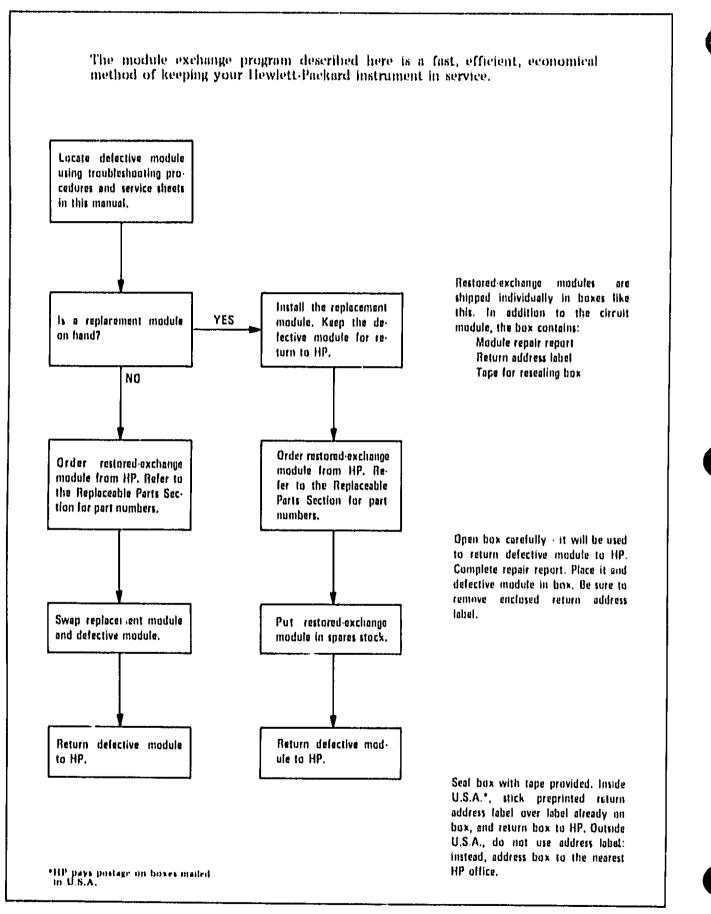


Figure 8-5. Module Exchange Procedure

8-10

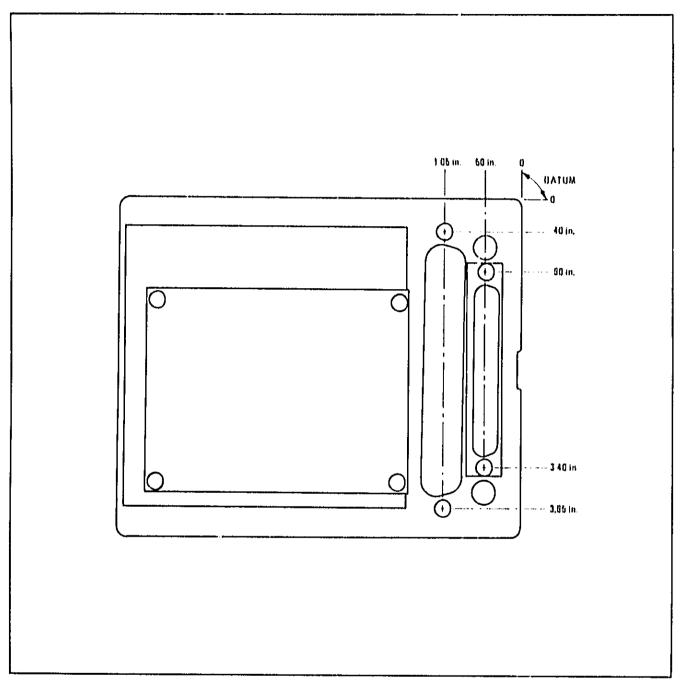


Figure 8-6. Rear Panel Connector Alignment

# 8-37. Rear Panel Connector Replacement

8-38. When replacing rear panel connector P1, connector P2 also must be partially removed to remove P1 from the rear panel ca: - ig.

8-39. When reassembling rear panel connectors P1 and P2 into the casting, alignment is very critical to ensure proper interface with the mating 8350A connectors. Align the center of the attaching bolts with a steel rule and tighten in

place in accordance with the placement drawing in Figure 8-6.

# 8-40. AFTER-SERVICE PRODUCT SAFETY CHECKS

8-41. Visually inspect the interior of the instrument for any signs of abnormal internally generated heat, such as discolored printed circuit boards or components, damaged insulation, or evidence of arcing. Determine and remedy the cause of any such condition.

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# 83590A RF PLUG-IN OVERALL BLOCK DIAGRAM DESCRIPTION

The operating principles of the 83590A RF Plug-in are described in two levels. The Functional Block Diagram Description describes major functional areas of the instrument. The Overall Block Diagram Description discusses the theory in greater depth, and outlines the breakdown of functions among the various instrument assemblies.

# FUNCTIONAL BLOCK DIAGRAM DESCRIPTION

The HP Model 83590A RF Plug-in, used with the 8350A Sweep Oscillator, covers the 2.0 to 20.0 GHz frequency range in three bands with up to +10 dBm of leveled RF power (+8 dBm between 18.6 and 20.0 GHz). In addition to internal leveling, external detectors or power meters can be used to level the RF power. Furthermore, the 83590A can sweep power proportional to either frequency or sweep.

The 83590A can be broken down into four functional sections:

- Digital Control and Front Panel
- Frequency Control
- Power Control (ALC)
- RF Section

The functional description for each of these four functions is described briefly below.

# Digital Control/Front Panal

The entire 83590A is digitally controlled by the 8350A microprocessor. It must be emphasized that nearly all functions are commanded by the 8350A; very few activities take place without microprocessor intervention.

The Digital Control section of the 83590A is the focal point of all communication between Plug-in and mainframe. It receives commands ordered by the microprocessor along the 8350A's instrument bus. Once in the 83590A, these commands are decoded and routed to the appropriate part of the Plug-in to control virtually every capability. The Digital Control section also contains a block of Read Only Memory (ROM), which provides the microprocessor with the constants and program software tailored to the Plug-in. The Digital Control section, then, is the control center for the entire Plug-in.

The Front Panel Interface is the communication link between the front panel displays or controls and the rest of the Plug-in. It receives and stores information to be presented by the numerical display or annunciators through the Digital Control block, and continuously refreshes the display. It also receives the user's commands through the front panel pushbuttons and Rotary Pulse Generator (RPG), and sends them back through the Digital Control block to the 8350A microprocessor. Certain analog signals, such as EXT/MTR ALC, pass through the Front Panel Interface directly to the appropriate part of the 83590A.

# **Frequency Control**

The Frequency Control block is responsible for converting the tuning ramp (VTUNE) from the 8350A Sweep Oscillator into drive currents for controlling the YIG Oscillator (YO) and YIG Tuned Muliplier (YTM). The tuning voltage is offset, scaled and buffered to provide a buffered tuning voltage for both the YO and YTM drivers. The two drivers each digitally scale and offset the buffered tuning voltage (BVTUNE) to yield tuning voltages that enable

# Model 83590A

the YTM (which is basically a harmonic generator followed by a tunable bandpass filter) to track the YO fundamental frequency or one of its harmonics (Bands 2 and 3 use the second and third harmonics of the YO). Each driver develops a delay compensation signal that is summed with the scaled tuning voltage on each driver to compensate for delay in the YO or YTM. Lastly, low-frequency components of external frequency modulation (FM) are filtered and also summed in to produce total YO and YTM control voltages. However the YO and YTM are current controlled devices, so Current Drivers convert the control voltages to drive currents for the YO and YTM.

The high-frequency FM components cannot be summed in with the drive currents due to the limited dynamic response of the YO and YTM. The YO contains a separate coil that allows smaller yet faster frequency modulation. The amount of deviation is limited and is within the bandpass characteristics of the YTM, so the YTM does not require any frequency control for high-frequency modulation.

The Sweep Interrupt block monitors the tuning voltage (VTUNE) when the 83590A is performing a sweep requiring more than one band. When a tuning voltage corresponding to the end of a band is sensed, these circuits temporarily stop the sweep ramp and interrupt the 8350A microprocessor. The microprocessor then prepares the Plug-in for the new band, including new scaling and offset values, and continues the sweep.

# Power Leveling (ALC)

The Power Control circuits determine the RF output power level, and ensure that the power is constant across the sweep. A feedback loop detects the RF power level, compares it with a reference voltage, and adjusts modulators in the RF path to correct for amplitude errors.

The power level is digitally programmed from the 8350A Sweep Oscillator. A scaled sweep ramp to provide the power slope or power sweep function is added, yielding a reference power level.

RF detectors provide a voltage proportional to the actual RF power level. This is then compared to the desired reference power level voltage to produce an error voltage. The error is then amplified to drive RF modulators and correct the output power level.

# **RF Section**

The RF Section includes the high-frequency microcircuits and their bias components which produce and amplify the RF output.

The 2 to 20.0 GHz frequency range is covered in three bands. The YIG Oscillator (YO) is the tunable source for all bands. Bands 1 through 3 are obtained by amplifying the direct YO output and then generating harmonics in the YTM. The YTM contains a tunable bandpass filter that is tuend to the desired RF output frequency. As a result the YTM passes the desired RF output frequency and rejects unwanted harmonics.

A directional coupler with detector senses the RF power level and sends a voltage to the ALC circuit for power leveling.

In Option 002 instruments, a programmable step attenuator is included to provide up to -70 dB of additional output power control range.

# **OVERALL BLOCK DIAGRAM DESCRIPTION**

# DIGITAL CONTROL/FRONT PANEL

# A3 Digital Interface

The A3 Digital Interface assembly acts as the 83590A's distribution center, receiving digital commands from the 8350A Sweep Oscillator and routing them to the appropriate assembly within the Plug-in.

The Buffer receives the digital control (including timing), data, and address signals from the 8350A Sweep Oscillator's Instrument Bus. The control and address lines are uni-directional and pass only to the Plug-in, whereas the data lines are bi-directional and carry information both to and from the Plug-in. A single buffer returns the Plug-in flag (L PHFLG) to the 8350A, indicating that a Plug-in front panel key was pushed.

The Address Decoder provides the major control lines which eventually direct data to the correct part of the Plug-in. Address and control lines are decoded to produce enable lines: two for ROM, three for the Configuration Switches/Interrupt Control, five for the Front Panel, and two for the remainder of the Plug-in assemblies.

The ROM (Read Only Memory) stores program software and constants used by the 8350A microprocessor while executing routines dedicated to the Plug-in. Two address decoding lines, plus address lines, select the byte of data to be sent back to the 8350A.

The Configuration Switch/Interrupt Control circuits serve a dual purpose. The Configuration Switch encodes information about the Plug-in options used, and certain user-defined parameters. During INSTR PRESET and power-on, the switch positions are read by the 8350A microprocessor, then used to configure the 83590A according to the parameters selected. As Interrupt Control, the circuits monitor the L SIRQ line, and send an interrupt (L PHRQ) to the 8350A to begin each bandswitch. During a bandswitch, the Interrupt Control is programmed to count down time intervals specified by the microprocessor. At the end of these intervals, the L PHRQ line is again activated to notify the 8350A that the time interval has elapsed.

The RF Plug-in Interface buffers the data and address lines for use throughout the rest of the RF Plug-in. The data bus is bi-directional, so that the 8350A can read information from the A2 Front Panel Interface, A6 Sweep Control, A7 YTM Driver, and A8 YO Driver assemblies. The control lines, which complete the internal bus, come directly from the Address Decoder. This internal bus sends control messages and data for DACs to digital interface cucuits on each assembly. These digital interface circuits are essentially buffers between the digital and analog circuits.

# A2 Front Panel Interface, A1 Front Panel

# NOTE

# Due to their strong functional internalation, the A2 Front Panel Interface and A1 Front Panel assemblies are discussed together.

The A2 Front Panel Interface and A1 Front Panel assemblies are primarily responsible for displaying the status and power fevel of the RF Plug-in, and transmitting pushbutton and RPG commands back to the 8350A Sweep Oscillator for processing. Front panel analog adjustments, and the analog IV/GHz rear panel output, are also processed on these assemblies.

### 8-14



Service.

The Keyboard/Display Interface performs two functions. As a Keyboard Interface, it strobes the columns of the Pushbutton Switch Matrix, while sensing the row lines. When a key is pushed, the row line tracks the strobed column line corresponding to that key. The Keyboard Interface detect this, sets the FLAG line to alert the microprocessor, and transmits the encoded data back to the 8350A for processing. As a Display Interface, the same column strobes are buffered and used to drive the digits of the Power Display. While a digit is enabled, the appropriate seven-segment data stored inside the Display Interface is buffered to drive the segments. The scanning is done at a fast rate to avoid flickering.

The Annunciator Interface stores data to drive the LED Annunciators that display the status of various functions. However, the Unleveled annunciator is not digitally controlled, but is driven from a separate Unleveled circuit which monitors the ALC assembly.

The Power Control interface digitally controls several functional areas. Three of the lines are buffered by the Attenuator Control, which operates the A19 Step Attenuator in instruments equipped with Option 00°. The RF On circuits control the biasing for the A13 YIG Oscillator and the A17 Amplifier. When the RF is turned off, the bias to these assemblies is removed, shutting off the oscillator and amplifier for minimum RF output.

The Frequency Tracking Amplifier and 1V/GHz blocks are the only active analog circuits on the A2 and A1 assemblies. The Frequency Tracking Amplifier monitors the YTM DRIVE V, a voltage propartional to the RF output frequency. Its output tracks the RF output frequency, and is used to compensate for frequency-dependent non-linearities in the ALC loop. The 1V/GHz circuit further processes this signal to produce a rear-panel output supplying 1 Vdc per GHz of output frequency for use with external equipment.

Miscellaneous front panel controls must pass through the A1 and A2 assemblies. The RPG produces pulses when rotated, and sends them directly back to the 8350A Sweep Oscillator to be decoded and processed to adjust the power or fine-tune the YTM bandpass frequency. The EXT/MTR ALC CAL adjusts the absolute power level when external detector or power meter leveling is used.

# FREQUENCY CONTROL

The Frequency Control section of the Plug-in is responsible for determining the actual RIoutput frequency. Based on the tuning voltage VTUNE and digital data, the correct drive currents are developed for tuning the A13 YIG Oscillator and A12 YIG Tuned Multiplier. Frequency Modulation (FM) is also processed in these circuits.

# A6 Sweep Control

The A6 Sweep Control assembly scales and offsets the tuning voltage from the 8350A Sweep Oscillator to provide a series of 0 to -10V ramps (one ramp for each band) during a multiband sweep. For single band sweeps, the A6 Sweep Control assembly just buffers and inverts the the 0 to 10V VTUNE ramp from the 8350A.

The Bandswitch Comparator and Sweep Control/Interrupt Logic sections monitor the buffered tuning voltage. When the sweep ramp requires a change of band, this circuit issues "stop sweep" and blanking pulse requests. At the same time, an interrupt is sent to the mainframe through the A3 assembly, requesting service for the bandswitch. After this point, the microprocessor completes the bandswitch sequence through the Sweep Control circuits.

SRD and PIN Switch Bias circuits control the Switched YTM for band selection and Step Recovery Diode (SRD) biasing. The SRD BIAS output optimizes the SRD biasing for the frequency band of operation.

# AB YO Driver, A9 Reference Resistor Assembly

The A8 YO Driver assembly scales and offsets the buffered tuning voltage from the A6 Sweep Control assembly and converts it to a current for controlling the A13 YIG Oscillator (YO) frequency.

The buffered tuning voltage BVTUNE is scaled, offset, and summed with various correction signals to produce the tuning current for the A13 YIG Oscillator. The scaling and offsetting is used to change the frequency range of the YIG Oscillator depending on the band of operation. For each band, the 0 to 10V ramp must tune the YIG Oscillator over a different frequency range as shown in Table 8-5.

	YO Frequency Range (GHz)	
2.0	2.0 to 7.0 GHz	
3.5	.5 to 6.75 GHz	
4.5	.5 to 6.67 GHz	

Table 8-5,	YO Frequency	Bands
------------	--------------	-------

The Scaling and Offset DACs are also used to compensate for differences in oscillator sensitivities. The amount of scaling and offset is set by the Frequency Cal switches. At initial power on or Instrument Preset, the status of the Cal switches is read by the 8350A and stored in RAM. This information is then used along with frequency range (band) information to program the DACs. The -10V Reference generates a stable voltage source used as a reference on the A6 Sweep Control, A7 YTM Driver, A8 YO Driver, and A4 ALC assemblies.

The Delay Compensation circuit produces signals to compensate for time delay in the YIG Oscillator response. The coils in the YO are used to set up a strong controlled magnetic field to control the RF frequency. Due to inductive reactance of the electromagnets, there is a delay between the applied voltage and resultant current flow through the coils. The Delay Compensation circuit monitors the scaled tuning voltage, and from its amplitude and slope produces a signal added to the YO DRIVE V to compensate for swept frequency errors that would occur because of the response delays.

The  $\pm 20V$  Tracking circuit monitors the  $\pm 20V$  supply, producing an output which follows this voltage. Since the current through the YO is referenced to this supply, this prevents power supply drift or noise from creating frequency errors.

The summing junction adds together the scaled tuning voltage, offset, delay compensation, +20V tracking voltage, and offset compensation. The YO LO FM from the A5 FM Driver (described below) is also added. The product is the YO DRIVE V, a signal proportional to the YO frequency.

The remainder of the A8 circuits and the A9 components convert the YO DRIVE V to a current to control the YO frequency. The final current drive transistor is controlled by the A8 assembly. The current through this transistor, and hence the YO, generates a proportional voltage across the chassis-mounted reference resistor, which is monitored and compared to the YO DRIVE V. Any errors between the two are corrected in a closed loop, producing a current proportional to the YO DRIVE V. Compensation elements (Comp) correct for nonlinearities in the YO. If the YO is replaced, this section of circuitry requires changing.

In CW mode, a relay connects a large capacitor across the YO's coll. The capacitor resists changes in the YO current to reduce residual FM noise.

The Frequency Cal switches set the frequency end-point accuracy. These switches are set when the Plug-in is calibrated, and are read by the 8350A during Instrument Preset or initial power on. This information is used to program the Scale and Offset DACs.

## A7 YTM Driver, A9 Reference Resistor Assembly

The A7 YTM Driver assembly scales and offsets the buffered tuning voltage from the A6 Sweep Control assembly and converts it to a current for controlling the A12 YIG Tuned Multiplier (YTM) frequency.

The buffered tuning voltage BVTUNE is scaled, offset, and summed with various correction signals to produce the tuning current for the A12 YTM. The scaling and offsetting is used to change the frequency range of the YTM depending on the band of operation. For each band, the 0 to 10V ramp must tune the YTM over a different frequency range as shown in Table 8-6.

Band	YTM Frequency Bange (GHz)		
Band I	2.0 (o) 7.0 GHz		
Band 2	7.0 to 13.5 GHz		
Band 3	13,5 to 20,0 GHz		

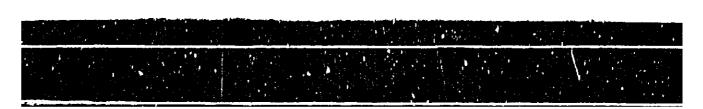
Table 8-6, YTM Frequency Bands

The Scaling and Offset DACs are also used to compensate for differences in YTM sensitivities. The amount of scaling and offset is set by the Frequency Cal switches. At initial power on or Instrument Preset, the status of the Cal switches is read by the 8350A and stored in RAM. This information is then used along with frequency range (band) information to program the DACs. The -10V Reference from the A8 YO Driver is a stable voltage source used as a reference for the Offset DAC.

The Delay Compensation circuit produces signals to compensate for time delay in the YTM response. The coils in the YTM are used to set up a strong controlled magnetic field to control the RF bandpass frequency. Due to inductive reactance of the electromagnets, there is a delay between the applied voltage and resultant current flow through the coils. The Delay Compensation circuit monitors the scaled tuning voltage, and from its amplitude and slope produces a signal ...dded to the YTM DRIVE V to compensate for swept bandpass frequency errors that would occur because of the response delays.

The  $\pm 20V$  Tracking circuit monitors the  $\pm 20V$  supply, producing an output which follows this voltage. Since the current through the YTM is referenced to this supply, this prevents power supply drift or noise from creating bandpass frequency errors.

The summing junction adds together the scaled tuning voltage, offset, delay compensation,  $\pm 20V$  tracking voltage, and offset compensation. The YTM LO FM from the A5 FM Driver (described below) is also added. The product is the YTM DRIVE V, a signal proportional to the RF Output frequency.



The remainder of the A7 circuits and the A9 components convert the YTM DRIVE V to a current to control the YTM bandpass frequency. The final current drive transistor is controlled by the A7 assembly. The current through this transistor, and hence the YTM, generates a proportional voltage across the chassis-mounted reference resistor, which is monitored and compared to the YTM DRIVE V. Any errors between the two are corrected in a closed loop, producing a current proportional to the YTM DRIVE V. Compensation elements (Comp) correct for nonlinearities in the YTM. If the YTM is replaced, this section of circuitry requires changing.

The Frequency Cal switches set the YTM's frequency end-point accuracy for tracking the YO frequency. These switches are set when the Plug-in is calibrated, and are read by the 8350A during Instrument Preset or initial power on. This information is used to program the Scale and Offset DACs.

# P/O A5 FM Driver

The A5 FM Driver assembly splits the external FM signal, passed through the mainframe, into two frequency ranges (Low Frequency and High Frequency). The low frequency modulation is added to the main coil tuning voltages for both the YO and YTM; the high frequency modulation is routed to a separate coil inside the YO dedicated to high-frequency FM.

The external FM Input is routed to the A5 FM Driver assembly, where it splits into two paths. One path is lowpass filtered, removing high frequency components; the other path is highpass filtered, removing low frequency components. The filters are matched in stop-band response, such that one picks up where the other leaves off. Two Sensitivity Select circuits determine the FM sensitivity (RF Output deviation of -20 or -6 MHz/volt) and select either ecossover or direct coupling.

The low frequency path is further divided into two paths, one for driving the YIG Oscillator and the other for the YTM. Since, for Bands 2 and 3, the RF output is actually a harmonic of the YO frequency, the FM sensitivity of the YO (in relation to changes ir, the RF output frequency) varies between bands. Also, if the rear panel Aux Output (YO fundamental frequency) is used for phaselocking, the FM sensitivity for the YTM varies between bands. Thus, variable gain amplifiers (controlled by band select logic) scale the FM driver outputs according to the band of operation and phaselock source (as selected by the A3S1 Configuration Switch).

The YO LO FM is eventually added to the YO DRIVE V, and modulates the YO output frequency through its main coils. The YTM LO FM is added to the YTM DRIVE V, and modulates the YTM bandpass frequency through its main coils. Thus, for low frequency modulation, both the YO and YTM track each other in frequency.

The YO and YTM main coils cannot respond to fast deviations due to inductive and magnetic delays. Therefore, the YO contains a separate, small, but fast-acting "FM coil". The HI FREQ FM is sent to this coil, allowing limited high-frequency modulation. Since this modulation is limited, and does not extend beyond the bandwidth of the YTM, no high-frequency modulation is required for the YTM.

# ALC/POWER CONTROL

The A4 ALC assembly, and parts of the A5 FM Driver assembly, are responsible for power level control. Power leveling is accomplished by detecting the RF output power level, comparing it to a fixed reference voltage, and adjusting RF modulators to correct for power errors. This results in constant RF power level across the entire sweep. The absolute RF power is digitally controlled, and can be set between  $\pm 10$  and  $\pm 5$  dBm. (Instruments with Option 002 use an RF step attenuator to achieve power control down to  $\pm 75$  dBm. However, this is not part of the leveling loop.) The power sweep and power slope functions are obtained by adding a scaled voltage ramp offset to the reference power level.

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# A4 ALC Assombly

The A4 ALC assembly receives its inputs from the various detectors, and selects one of them for leveling. The sources include Detector CR1, the external input (external negative detector), and a third position which inverts the polarity of the external input (power meter detection). The selected detector voltage is proportional to the peak RF amplitude. The Input Sample & Hold stores the detected level during pulse modulation. This prevents subsequent circuits from saturating when the RF power drops out during blanking or pulse modulation. The Logger amplifier produces a voltage proportional to the log of peak RF amplitude, and essentially represents the RF power level in dB.

The reference, or desired, power level is established digitally by a 12-bit DAC, scaling the -10V REF from the A8 assembly. This establishes a voltage proportional to the desired output level in dBm. The External AM signal from the 8350A Sweep Oscillator, and the PWR/SWP COMP signal from the A5 FM Driver assembly (described below), are summed in to produce PWR REF, a voltage proportional to the desired RF output power.

The second summing junction adds the External Cal input from the front panel. This offset voltage is used to calibrate absolute power when external leveling is used. The final product of the power reference chain is a reference voltage representing the desired RF output amplitude.

The ultimate goal of the leveling loop is to make the actual RF power equal to the desired RF power. A third summing junction compares the voltages representing these two quantities, and yields a signal representing the error between actual and desired power. This error voltage is sampled and held during pulse modulation to prevent subsequent circuits from saturating. The held error signal is amplified, and the RF blanking signal added to switch off the RF power during bandswitch, retrace, and internal squarewave modulation (from the 8350A), without saturating any other components in the path. An additional circuit monitors the input to the modulator drivers, and lights a front panel Unleveled LED if this voltage exceeds the normal range for leveled power.

# P/O A5 FM Driver

The A5 FM Driver assembly includes circuits to produce the PWR/SWP COMP signal added to yield the PWR REF. The Power Sweep function is achieved by scaling the VSW sweep voltage with a DAC. By programming the appropriate scale factor, a voltage representing dB/GHz or dB/Sweep is produced.

The ALC Compensation is a "four breakpoint, adjustable slope network" which compensates for fixed frequency-dependent nonlinearities in the RF path, typically the couplers and detectors. Its input is FREQ TRK V, a voltage proportional to frequency. This signal drives an array of four pairs of transistors, whose outputs are summed together to yield the ALC compensation signal. The gain of each transistor, and the voltage at which they conduct, is adjustable. A ninth adjustment adds the FREQ TRK V directly. In this way, a complicated compensation function, approximated by five straight lines, is produced.

The Power Sweep DAC adds a ramp voltage to the power reference signal when the Power Sweep or Power Slope functions are activated. Its input, VSW, is a sweep ramp that essentially tracks the tuning voltage, but always runs from 0 to 10 Vdc. A digitally programmable multiplying DAC scales this voltage according to the dB/SWP or dB/GHz value selected. (If these functions are disabled, the DAC is set to its minimum value.) This ramp is added to the ALC Compensation signal described above, and added to the Power Reference signal on the A4 assembly.

# RF SECTION

The RF Section includes the microcircuits and their bias boards that produce the actual RF output power. These components include A13, A14, A16, A19, AT1, DC2, and CR1.

The A13 YIG (Yttrium-Iron-Garnet) Oscillator (YO) is the fundamental frequencycontrollable microwave source for the 83590A RF Plug-in, ranging from 2.0 to 7.0 GHz. The YO's frequency is determined by the current flowing through large electromagnetic coils inside, supplied by the A8 and A9 assemblies. Due to the response-time limitations of the main coils, a smaller coil with a much faster response but limited range is used to modulate the output frequency when faster rates are needed.

The A16 Modulator/Coupler provides pulse modulation and amplitude control for leveling, and couples part of the YO output to the rear panel AUX OUTPUT connector.

For Bands 1 through 3, the fundamental YO output is amplified by the A14 Power Amplifier. The AT1 Isolator provides 20 dB of isolation between the Power Amplifier and the A12 YTM. The fundamental YO frequency from the isolator is applied to a Step recovery Diode (SRD) in the YTM. The SRD passes not only the fundamental frequency, but also generates an output that is rich in harmonics. The YIG Tuned Filter is a bandpass filter that is tuned to the desired RF output frequency by the A7 YTM Driver. Thus, the YTM uses the YO fundamental frequency to generate an RF output corresponding to either the YO fundamental frequency (Band 1) or one of its harmonics (Bands 2 and 3).

The A17 Amplifier boosts the mixed-down low-power output from the A18 assembly. The amplifier also serves to remove unwanted high-frequency mixing products. The A17A1 Amplifier Bias assembly is connected directly to the microcircuit, has no adjustable or replaceable parts, and is not separately replaceable.

The A15 DC Return allows YTM bias currents to pass to ground, while preventing them from affecting other circuits.

The DC2 Directional Coupler directs a portion of the RF energy to Detector CRI, producing a voltage proportional to the RF power level for leveling.

The RF output is finally directed to the front panel RF Output connector. On instruments with Option 004, different cabling takes the output to the rear panel connector. On instruments with Option 002, the A19 RF Step Attenuator is included, providing from 0 to 70 dB of attenuation in 10 dB steps. This attenuated output is then routed to the front panel connector (Option 002 only) or rear panel connector (Option 002 with Option 004).

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# **B3590A OVERALL TROUBLESHOOTING**

The purpose of this troubleshooting information is to provide an aid in isolating a problem in the 83590A to a specific assembly. Further troubleshooting information is supplied with each service sheet to isolate the problem to the component level.

The first step in overall troubleshooting is to identify the symptom(s) and determine under what conditions the problem exists. If the problem is an RF Plug-in error code (E001 or E050 through E053) refer to the Error Code section of this troubleshooting procedure. Also ensure that the 8350A used with the 83590A is calibrated and functionally operating.

A failure in the 83590A normally affects one of the following functions.

- Front Panel/Digital Control Probable symptoms are error code E001, incorrect annunciator or digit displays, inability to control operation from front panel, or erratic instrument response to front panel entries. The problem is generally on the A1, A2, or A3 assemblies, or with the RF Plug-in/8350A interface.
- Frequency Control Frequency control problems include frequency inaccuracy, sweep control problems or power losses due to the YTM not tracking the YO frequency. If the 8350A VTUNE output and power supplies are verified, the problem is most likely on the A5, A6, A7, A8, or A9 assemblies, or in the RF Section. If a frequency accuracy problem occurs only during swept operation, and the inaccuracy increases with faster sweep times, the problem is most likely with the Delay Compensation circuit on the A8 YO Driver assembly. Power losses that can be corrected with the front panel PEAK control indicate that the YO/YTM Tracking needs calibration (Refer to Section V, Adjustments).
- Power Control Typical problems are no RF Output, maximum unleveled RF output, or excessive power level variations. The problem is most likely with the A4, A5, or RF Section. If the trouble is limited to power sweep and slope control, the problem is most likely with the Power Sweep DAC on the A5 assembly. If low power is the problem, try adjusting the front panel PEAK control to peak the power. If the power losses are eliminated, perform the YO/YTM Tracking adjustments in Section V.
- RF Path Problems associated with high-frequency microcircuits include spurious or harmonic distortion, no RF power, or full unleveled RF power. For a harmonic distortion problem, refer to Section V, Adjustments, For power problems, try peaking the power with the front panel PEAK control, then refer to the A4 ALC Troubleshooting before suspecting the RF components.

Once the problem is identified, exercise the RF Plug-in to determine under what conditions the problem exists. Some important conditions to check are:

 Sweep Mode related — Is problem only for swept modes of operation, or does it also exist in CW operation? If problem still exists in CW operation, troubleshoot in this mode (it is easier to check waveforms and voltages in CW operation). For problems that occur only for swept operation, check if problem exists for single band sweeps. If the problem occurs only for multiband sweeps, suspect the Bandswitch control circuit on the A6 Sweep Control assembly.

- Control related Try different methods of entering data (i.e. RPG, Data Entry Keys, or increment/decrement keys). If the problem is related to a specific control, troubleshoot that control and respective circuits. If the problem is related to a specific type of control (e.g. pushbuttons) refer to the AI/A2 service sheet and troubleshoot the respective interface circuit.
- Sweep Time related Swept frequency accuracy problems that get worse with faster sweep times are probably caused by the Delay Compensation circuit on the A8 YO Driver assembly. If it is necessary to adjust the front panel PEAK control for different sweep times, the trouble is probably caused by the Delay Compensation circuit on the A7 YTM Driver.

# Error Codes

RF Plug-in error codes are displayed in the 8350A left FREQUENCY display. The error codes may be generated as a result of the Instrument Preset self test (E001, E052, or E053), or during normal instrument operation (error codes E050 or E051). A description of each error code is provided in Table 8-7. Further troubleshooting information for c ich error code follows.

**Error Code E001.** Error code E001 indicates that the 8350A microprocessor is unable to properly read Plug-in ROM. Initial checks should be made to verify proper mating of rear panel connectors with the 8350A. Also check cable connections to the A3 Digital Interface and ensure A3 is properly installed. Refer to the A3 service sheet for specific troubleshooting information.

**Error Code E050.** Error code E050 is generated when the 8350A microprocessor responds to an RF Plug-in keyboard flag and no key has been pressed. Check the logic state of the FLAG input to the A3 Digital Interface (A3P1 pin 42). It should be a stable logic low until a front panel key is pressed (when it is briefly strobed high). If it is not a stable low, refer to the A2 service sheet for further troubleshooting. If FLAG is a stable low, check that the L PIFLG output of A3 (A3J1 pin 39) is a stable high and pulses low when a front panel key is pressed. If necessary, trace the logic state of L PIFLG on the 8350A A3 Microprocessor.

**Error Code E051.** Error code E051 indicates that an invalid keycode is received by the 8350A microprocessor. Refer to the A1/A2 service sheet to troubleshoot the keyboard matrix and Keyboard/Display Interface circuit.

**Error Code E052.** Error code E052 is generated if there is a problem with the Interval Timer on the A3 Digital Interface. A test routine is run at power-on or when Instrument Preset self test is initiated. If Error code E052 is generated, refer to the A3 Digital Interface service sheet for further troubleshooting.

**Error Code E053.** Error Code E053 is generated at power-on or Instrument Preset when there is a problem with the Peripheral Interface Adapter (PIA) on the A3 Digital Interface. If error code E053 is generated, refer to the A3 Digital Interface service sheet for further troubleshooting.

# **Digital Control/Front Panel**

A digital control problem usually affects the entire Plug-in, but may disable only a section of the instrument. Generally, a digital control problem is indicated by a front panel failure. If the problem is limited to a specific type of control (pushbutton or RPG) or display (annunciator or digital display), the indication is that of a front panel failure. An RPG failure may indicate problems on the front panel assemblies of the 8350A mainframe, where RPG pulses are decoded. If multiple front panel functions are inoperative or erratic, the problem is most likely a digital control problem. Detailed troubleshooting procedures for checking front panel operation are provided in the A1/A2 service sheet. For digital control problems, refer to the A3 Digital Interface service sheet, and check the address, data, and control line outputs of the A3 assembly.

When there is a problem with a digital-to-analog interface (DAC), the symptom is generally a discontinuity in the analog response.

#### **Frequency Control**

Troubleshooting a frequency control problem can be greatly simplified by first defining the conditions under which the problem exists. When troubleshooting, the RF Plug-in should be operating in the least complicated mode that exhibits the frequency control problem. For instance, a CW frequency is less complicated than a swept mode, and a single band sweep is less complicated than a multiband sweep.

#### NOTE

## To ensure accurate frequency counter readings, check for adequate RF output power.

**Frequency Accuracy Problem for All Bands.** Frequency accuracy problems that affect all bands are most likely caused by the A8 YO Driver being out of calibration. Perform the related adjustments in Section V before further troubleshooting.

**Swept Frequency Accuracy Problem.** A frequency accuracy problem that occurs only during swept frequency modes is typically a delay compensation problem. Refer to the A8 YO Driver for further troubleshooting.

#### Power Control

Power control problems normally fall into one of the following catagories.

- No RF Output Power
- Maximum Unleveled RF Output Power (no power control)
- Excessive power variations

**No RF Output Power.** Remove the A4 ALC assembly; the RF OUTPUT power should go to a maximum level. If not, the trouble is in the RF Section. If the RF OUTPUT goes to maximum, the problem is in the A4 ALC assembly.

**Maximum Unlevaled RF Output Powor.** Check leveling in External and Meter leveling modes. If power is leveled for these modes, the problem is with the internal detector. Otherwise, refer to the troubleshooting information for the A4 ALC assembly.

#### Service

**Excossive Power Variations.** Refer to the troubleshooting information for the A4 ALC assembly.

Low Power. If unable to obtain specified maximum leveled power try peaking the power with the front panel PEAK function. Set the 83590A to External ALC mode (this opens the ALC loop), press SHIFT POWER LEVEL, and adjust the POWER control to maximize the RF Output power over the 2.0 to 20 GHz frequency range. If this works, perform the YO/YTM Tracking adjustments in Section V. Otherwise refer to the RF Section service sheet for further troubleshooting.

#### **RF Section**

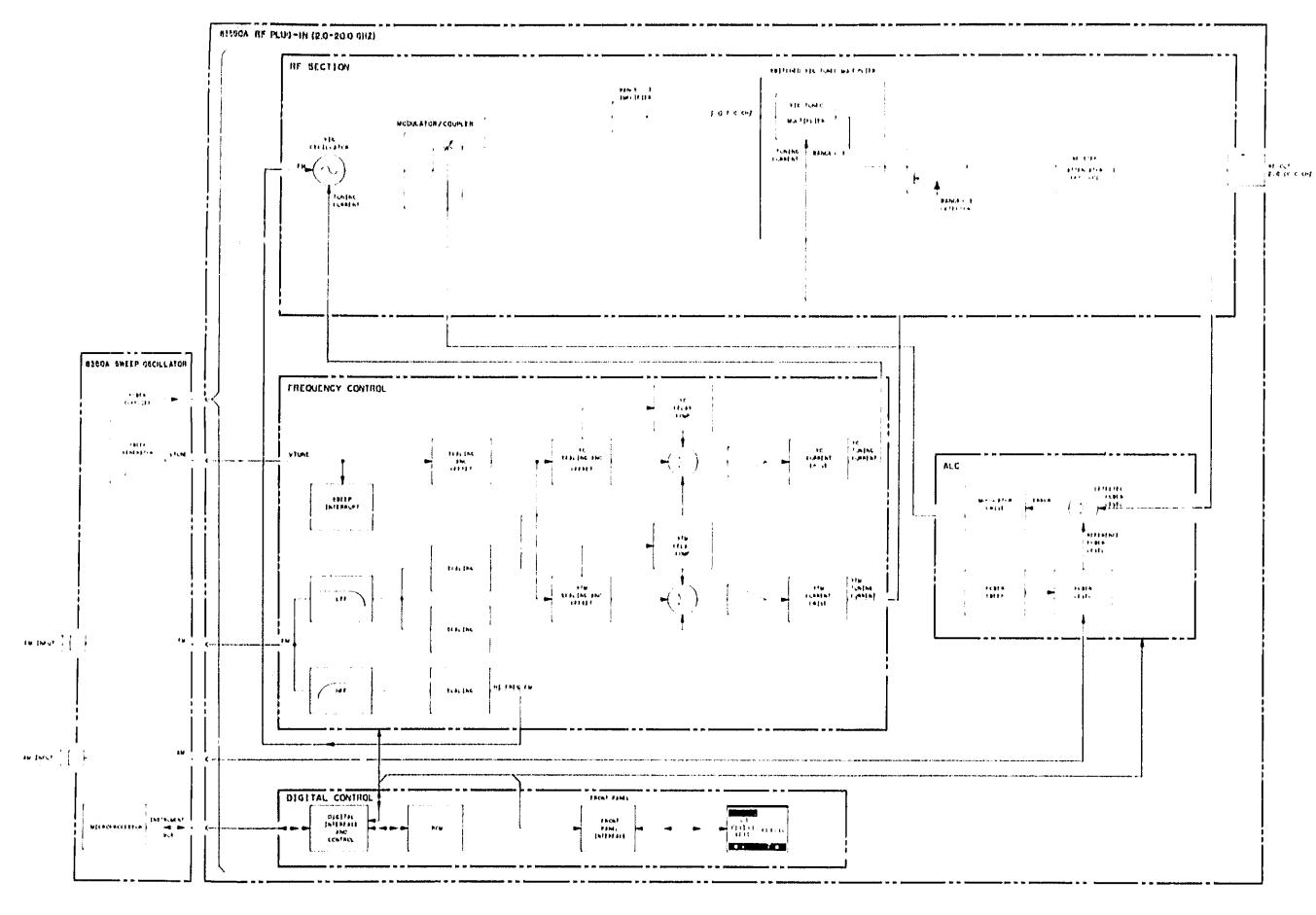
RF Section problems are usually indicated by no RF Power, full unleveled RF power, excessive harmonics, or spurious responses. For an RF power problem refer to the Power Control section of this troubleshooting information.

Error Code Function Tested		Operator Initiated Test	t Troubleshooting Hints		
E001	8350A/83590A		Check the RF Plug-in connections and cable connections to A3. Do Hex Data Write to front panel and Hex Data Read of A3S1 Configuration switch. See E001 Trouble- shooting in this procedure for specifics.		
E050	Plug-in keyboard		Check PIFLG		
E051	Invalid key code	SUNFT 04	See A1/A2 service sheets for further troubleshooting.		
E052	Interval Timer	SHIFT 55	See A3 service sheet for further troubleshooting.		
E053	РІА	SIMFT 55	See A3 service sheet for further troubleshooting.		

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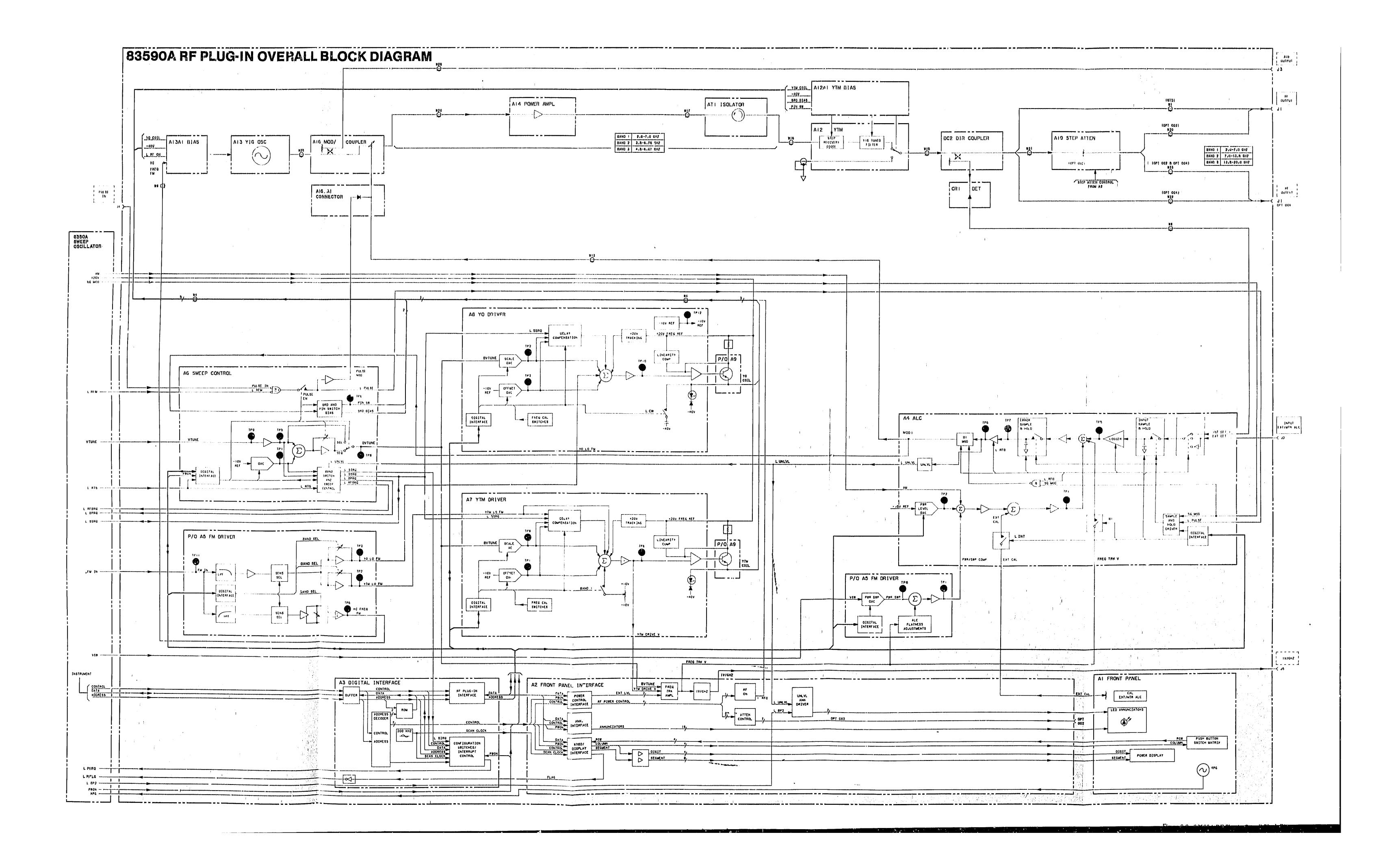
Table 8-7	83590A	Error	Codes
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Figure 8-7, 83590A RF Plug-in Simplified Block Diagram





#### A1 FRONT PANEL and A2 FRONT PANEL INTERFACE, CIRCUIT DESCRIPTION

#### GENERAL

The AI Front Panel and A2 Front Panel Interface assemblies provide communication between the instrument and the user. Reyboard and RPG commands are transmitted to the 8350A microprocessor for appropriate action. The numerical power level and Plug-in status information is displayed on front nanel LEDs, External ALC power calibration and frequency calibration inputs are passed through the front panel to the Plug-In. Also, the programmable step attenuator controls and "1V/GHz" outputs are processed on the A2 assembly,

#### **KEYBOARD**

Push Button Switch Matrix	A1:	$(\mathbf{j})$
Keybcard/Display Interface	A2:	

The push button keyboard is arranged in a column-row matrix. The column lines are sequentially strobed, while the row lines are simultaneously sensed to determine when a key is depressed. The matrix scanning and sensing, along with the debouncing functions, are performed by U6, the Keyboard/Display Interface. U6 is a large-scale integrated device canable of monitoring the keyboard without continual attention from the 8350Å microprocessor. When a key is depressed. U6 eliminates contact bounce, encodes and stores the column/row information in an internal register, and sets the FLAG line. When the microprocessor detects the flag, the keyboard codes are read from U6 and processed.

#### POWER DISPLAY

Power Display A1: (K)

Keyboard/Display Interface A2: (A)

Power Display Driver A2: (D)

The numerical power display is a four-digit, seven-segment LED configuration. Only one digit is enabled at any one time by the DIGn lines. These lines are continuously scanned by the buffered keyboard column lines from U6. providing a flicker-free display. The seven-segment and decinal point information corresponding to the enabled digit is provided by buffered lines. from U6. When the display is undated, data is sequentially written into U6 from the microprocessor and stored internally. U6 is then responsible for scanning the display without requiring constant attention from the 8350A.

#### UNLEVELED ANNUNCIATOR DRIVER

LED Annuncistors A1: (H)

Unleveled Annuncistor Driver A2: (F)

U12A is one half of a dual timer serving as a triggered monostable, or one-shot. When the unleveled condition is detected, the trigger line pulses low. The monostable then goes high for a 50 millisecond period beginning at the trigger's falling edge. This ensures that the LED will stay lit long enough to be visible when triggered by a very narrow pulse. When L BP2 (Low=Blanking Pulse) is low and U9A is open, the trigger input is held high by CR6 so that the monostable cannot be triggered during retrace.

#### LED ANNUNCIATOR LATCH

LED Annunciators A1: (H) LED Annungiator Latch A2: (B)

Octal latches U7 and U5 control the various front panel and push button LED annunciators. When clocked by the FP3 or FP4 line from the A3 Digital Interface assembly, the latches store a byte of data from the data bus, and fight the LEDs determined by the bit pattern, (Low=ON).

#### RF POWER CONTROL LATCH A2; (C)

UR is a hex latch which stores six of eight data bits when clocked by the FP5 line from A3. These data lines control the programmable step attenuator (Option (002), RF on/off relay, and "IV/GHz" circultry. The step attenuator has 10, 20, and 40 dB pads internally, combining to provide up to 70 dB of attenuation in 10 dB steps. The enable (ENn) lines are inverted by U10A to provide disable (DISn) signals. The attenuator is a latching relay type, so that current is drawn only during switching. When the Plug-in RF OFF is selected, relay KI opens and shuts down the RF path. When K1 is open, blas is removed from the low band RF amplifier (to increase on/off ratio), and the YIG Oscillator and the RF are shut off. CR3 protects U8 from high transient voltages when K1 turns off.

#### 1V/GHz

Frequency Tracking Amplifier A2: (E)

#### 1V/GHz Amplifier A2: (G)

UIB scales and offsets the YTM tuning voltage for the IV/GHz circuit, providing a 0 to 6 volt ramp proportional to frequency. Switch U9D introduces an additional offset in the low frequency band only, since the RF output frequency is mixed down from a higher YO frequency. When internal leveling is used, U9C passes this voltage through Q3 to the A4 ALC and A5 FM Driver assemblies where it is used to compensate for frequency-dependent nonlinearities in various elements of the leveling loop. When external leveling is selected, U9B turns off Q3 to disable the compensation circuitry.

UIA further offsets and scales this voltage to provide 1V per GHz up to 18 GHz. where UIA approaches the limit of its power supplies (current source Q2) increases this upper limit beyond the level UIA atone can produce). The IV/GHz output is scaled regardless of the band chosen. This output is available at the rear panel of the Plug-in for use with 8410B Network Analyzers.

#### RPG (Rotary Pulse Generator) A1; (1)

#### External Leveled Power Calibration Control A1: (M)

The RPG provides control as selected by the keys below it (Power Sweep, Power Level, Peak, Slope), and encodes rotation into digital form for the microprocessor to use, providing a digitally-compatible control with an analog "feel". The two RPG lines pass directly to the 8350A's A2 Front Panel Interface assembly, passing through both Plug-in and mainframe motherboards. CAL adjustment introduces an offset to the leveling loop to match absolute RF power output to external leveling devices.

#### A1/A2 Troubleshooting

NOTE

Troubleshooting information for both the A1 Front Panel and A2 Pront Panel Interface assemblies is combined. All reference designators refer to the A2 assembly unless otherwise noted.

#### NOTE

The entire Plug-in depends on the A3 Digital Interface negembly for control, address, and data signals. Before troubleshooting the A1/A2 sesembly, verify proper functioning of A3. See Overall Troubleshooting for verification procedures.

Visually inspect the cabling inside the Plug-in for damaged or loose connections. Check that the large ribbon cable connections (W29, P1 and P2) are properly seated over the correct pins on Motherboard A10J2 and A3 Digital Interface A3J1. (On Plug-ins with Opt 002 Attenuator, W29P2 may be difficult to see). Check that W3 ribbon cable connections are securely sealed over A1011 and A2J1.

Check power supplies to the front panel: +5V at A10XA3, pins 6 and 7. Then check continuity between these points and A1011, pin 2.

#### Digital Display

The Plug-in display can be directly commanded by the 8350A microprocessor using Hex Data Write (see paragraph 8-22 for an explanation of Hex Data programming). An effective test pattern can be input which toggles the states of adjacent segment lines. The pattern should detect shorted lines or defective flipflops. Press 8350A CW. Enter key sequence:

	-	0 ms	0 0	0		Hex Data mode Address location 2d00 (U6) Hex Data Write
		•	5	5	•	Enters four hex bytes: 55 AA 55 AA

The pattern seen in the Plug-in display should match that shown in Figure 8-9. If the patterns match, the stug-in display is working properly, and any failures are probably due to the mainframe or Plug-in ROM.

#### Error Codes

Error codes E050 and E051 indicate a communication problem between the Front Panel Interface assembly and the 8350A microprocessor. Code implications and further troubleshooting hints are discussed later, under the subheading Keyboard.

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#### Figure 8-9. Display Test Pattern

If any of the digits in the display window appear to be stuck, or if the above test fails, remove the front panel and check the 200 kHz SCAN CLR at U6, pin 3. If no signal is detected, trace the line back through U4B to the A3 Digital Interface assembly.

Then, check the DIG1 through DIG4 lines for sequential low pulses. These can be accessed at the back of A1/A2 interconnect A2P1, pins 3, 5, 7, and 9. If they are absent, trace the problem back to U6.

The seven-segment lines, Ca through Cg, and Cdp, can be tested by programming the test pattern in Figure 8-9, then verifying activity at A2P1 Trace any problems back to U6.

To check for burned out display LEDs, make the key entry outlined above, except enter data: 0 0 0 0 0 0 0 0 0 . All segments, with decimal points, should light up.

Display problems may be due to A3 Digital Interface failures. Check the L FPI line at U6, pin 11, using Hex Data Rotation Write (see paragraph 8-22 for details).

SHIFT 0 0 Hex Data mode 2 MHz ms 0 0 Address location 2d00 (U6) Hex Data Rotation Write Md

The data lines should also be checked in this mode. (Input and output patterns 2440 are illustrated in Figure 8-2.) Trace any problems back through A3.

#### Annunciators

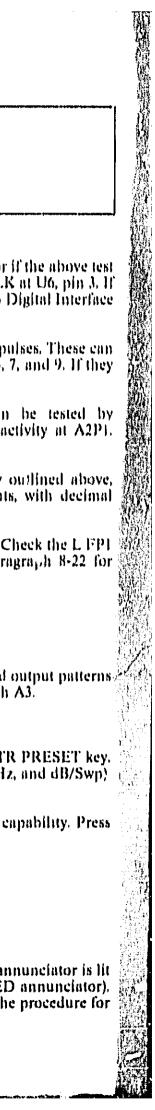
Check for burned out LEDs by pressing and holding the INSTR PRESET key. All LEDs should light, except for units indicator (dBm, dB/GHz, and dB/Swp) and UNLEVELED annunciators.

Use Hex Data Write as follows, to check annunciator control capability. Press 8350A CW and enter:

SHIFT 0	0	Hex Data mode
2 dBm dB	00	Address location 2E00 (U7)
M2		Hex Data Write
5 5		Hex Data 55
• •		Hex Data AA

Alternate between 55 and AA, and check that each addressed annunciator is lit for one case and out for the other (excluding the UNLEVELED annunciator). Plug-in annunciators are controlled by two locations. Repeat the procedure for address location 2E80 (U5).

SHANGE BREAMING SLOC SPREYELFS I SHANNA



If these tests fail, remove the front panel assembly to expose the A2 assembly. Use Hex Data Rotation Write as follows:

SHIFT 00Hex Data mode2dBm dB00Address location 2100 (107)M4Hex Data Rotation Write

Theck the enable lines for activity. The data bus inputs and latched outputs should also be checked for the patterns illustrated in Figure 8-2. Units annunicators are buffered by inverters, and drive current through the LED to ground rather than sinking current from 4-5V. The outputs of these buffers can be checked during Hex Data Rotation Write.

The UNLEVELED light is driven by pulse-stretching timer U12A, which is disabled by U9A during retrace. Check that U9, pin 3, is high during retrace (approximately 4Vdc), and low during forward sweep. The UNLEVELED light should be lit when the available power is insufficient for leveling to the desired reference level (typically several dB beyond specified maximum leveled power).

If the UNLEVELED light is not functioning properly, select 8350A RF BLANK and disengage 83590A RF to turn the power off. In this mode, L UNLVL, J1-12, should be low during forward sweep, and high during retrace. Connect oscilloscope channel B to the 8350A Sweep Out, and select the A vs B mode to externally sweep the oscilloscope with the 8350A sweep ramp. Check the input (pin 6) and output (pin 5) of timer U12A. The output of U12 goes high for an initial low pulse at the Trigger input (T), and remains high for a period of approximately 50 milliseconds. Subsequent trigger pulses, occurring within the timing cycle, will not affect the output. However, if the Trigger input remains low for a longer duration than the timing cycle, the output will remain high for the duration of the trigger signal. If no trigger signal is present, check diodes CR5 and CR7, or trace the problem back to the A4 assembly.

#### Keyboard

The keyboard matrix is scar.ned continuously by U6. This LSI device continuously strobes the column lines, senses the row lines for depressed keys, eliminates contact bounce, stores the key code internally, and flags the 8350A to recover the key code. Troubleshooting is difficult because the device is so complicated, but it is worthwhile to check all signals to and from U6, probing directly on the pins of the chip, before replacing it.

Error codes E050 and E051 generally indicate U6-related problems:

- E050 occurs when the microprocessor has received a flag (L PIFLG) from the Plug-in (indicating a front panel key was pressed), but cannot recover the keycode (indicating that the key was NOT pressed). Check the FLAG output from A2U6 (accessible at A3P1-42). It should be TTL low, approximately 0 volts. Pressing a front panel pushbutton should result in a very rapid pulse. If the line appears to be locked high, replace A2U6. If it is good, check inverter A3U10F (accessible at A3J1-39) to see if it is locked low.
- E051 occurs when the key code received by the microprocessor cannot be decoded. This indicates a failure in A2U6 or a bad Row Sense line. If the Row Sense lines are good, troubleshoot the keyboard matrix with a continuity checker.

To troubleshoot the Plug-in keyboard matrix, initiate the Key Code Test. Enter SHIFT 0. 4. Thereafter, when any Plug-in front panel key is pressed, the appropriate hexadecimal key code should appear in the mainframe FREQUENCY/TIME display window. The appropriate key codes are given in Table 8-8.

If this test indicates further troubleshooting, remove the front panel to make A2 accessible while connections between the front panel, Plug-in, and mainframe are still intact.

If the numerical display is blank, check power supplies on A2.

Check U6, pin 3, for the 200 kHz SCAN CLK signal. If it is missing, trace the problem back through U4B to the A3 Digital Interface assembly.

Initiate Hex Data Rotation Write and check the I. FP2 line for activity:

SHIFT 0 0	Hex Data mode
2 MHz ms 0 0	Address location 2d00 (U6)
M4	Hex Data Rotation Write

The data line inputs should also be checked in this mode. The pattern should match that shown in Figure 8-2.

Check the COL0 through COL3 lines for sequential low pulses, as shown in Figure 8-13.

If the patterns are absent, but the 200 kHz clock is present, the problem is probably U6. Ensure that problems in U4B or the A1 assembly are not tying the lines down.

If the column strobes are present, probe both the column and row line corresponding to the key in question at U6. Observe the traces while pushing the button. The two lines should track each other. If they track, but the microprocessor can't read the codes from U6, and the data bus is good, the problem is probably in U6.

If row and column do not track, separate the A1 and A2 assemblies and troubleshoot the keyboard matrix with 5 continuity tester.

#### **Rotary Pulse Generator (RPG)**

The RPG is a means of converting rotational information into digital signals which can be read by the microprocessor. The hardware components needed to decode the Plug-in RPG (counter and sign latch) are located on the 8350A A2 Front Panel Interface assembly. Some failures which appear to be in the Plug-in RPG, (e.g., 'run-away' POWER display or a locked-up sign) are likely to be caused by failures in the 8350A.

If the Plug-in RPG appears to be dead, remove the bottom cover of the 8350A and probe A10J1, pins 34 and 36. Check for the waveforms shown in Figure 8-14, while slowly rotating the RPG. If the signals are present, trace the PIRPGA and PIRPGB lines through the 8350A to the mainframe A2 assembly. Refer to 8350A A2 Service Sheet for more information.

#### Analog Circuitry

Analog circuitry on the A2 Front Panel Interface processes the YTM DRIVE V signal to produce the 1V/GHz rear panel output and FREQ TRK V, used in the ALC loop.

Check that the YTM DRIVE V signal is present at TP1. It should resemble the waveform shown in Figure 8-15. If it doesn't, trace the problem back to the A7 YTM Driver assembly.

If it is present, check TP3 for the waveform shown in Figure 8-16. If it is present on the A2 assembly, but FREQ TRK V is missing on the A4 and A5 boards, probe the emitter of Q3 for the same waveform offset by approximately 6.6 Vdc.

Analog switches U9B, U9C, and U9D are controlled by latch U8. These switches turn off FREQ TRK V when external leveling is used. These can be exercised by using Hex Data Write. Press 8350A CW and enter:

SHIFT 0 0	Hex Data mode
2 BKSP 0 0	Address location 21700 (U8)
M2	Hex Data Write
0 0	Enters hex byte 00
BKSP BKSP	Enters hex byte FF

Note that these switches are not identical. U9B is open for logic 0, while U9C and U9D are closed.

The 1V/GHz Amplifier adds one more stage of gain and offset to FREQ TRK V, producing a scaled tuning ramp to follow the RF output frequency at exactly 1 Vdc per GHz. Check the rear panel 1V/GHz BNC output jack for the ramp. If it is absent, check TP2 for the waveform shown in Figure 8-17. If there is no signal at TP2, but there is a ramp at TP3, the problem is in U1A.

#### **RF Power Control Latch**

U8 stores commands for the RF Step Attenuator (Option 002 only) and the RF ON line, which supplies -10V bias for components in the RF path. It also controls analog switches used for the signals mentioned above.

Hex Data Rotation Write can be used to verify the outputs of U8.

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#### NOTE

In Option 002 Plug-ins, disconnect the attenuator cable at A2J3 before initiating Hex Data Rotation Write. The bit pattern shifts too fast to actuate the attenuator properly, and may damage it.

Service

Initiate the check as follows:

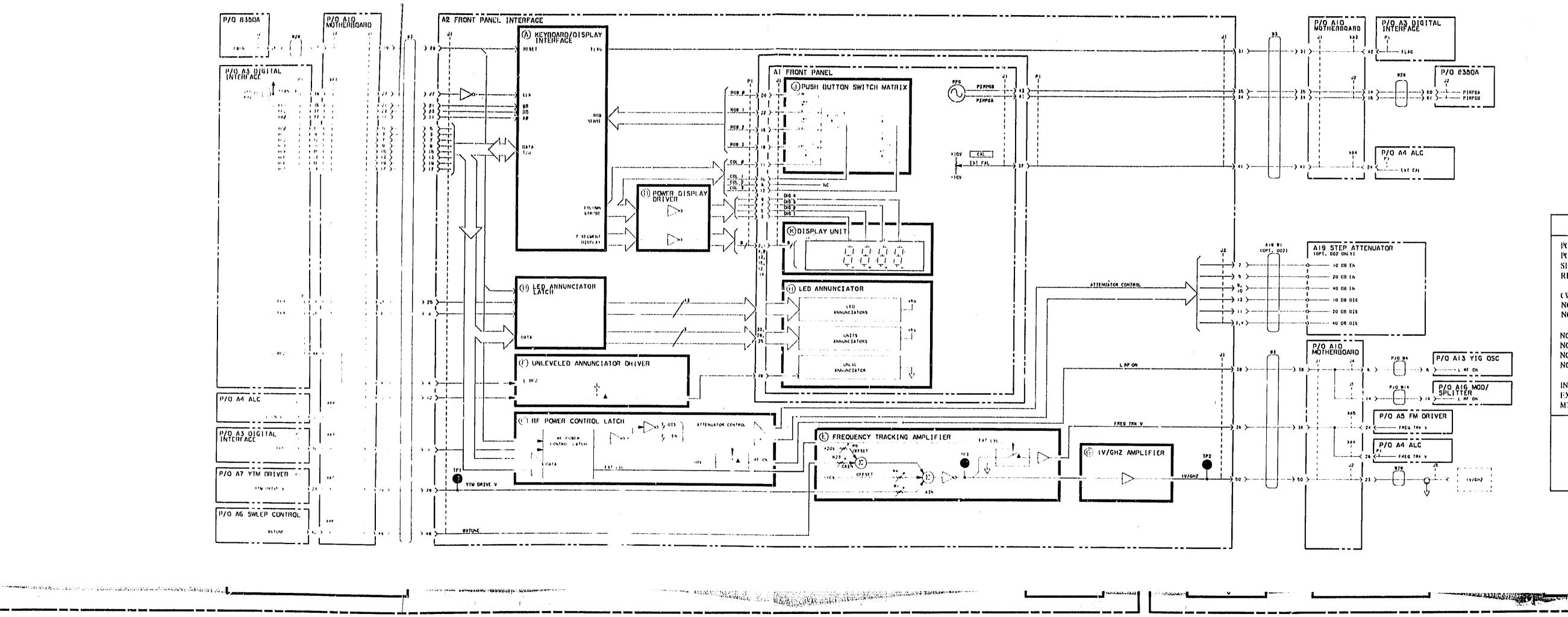
SHIFT 0	0		Hex Data mode
2 BKSP	0	()	Address location 21-00 (U8)
M4			Hex Data Rotation Write

Check L FP5 line for activity. Check data lines for patterns illustrated in Figure 8-2.

To check the RF ON relay, K1, make the same key entries as above, except enter M2 for Hex Data Write. Then alternate between data inputs: 0 0 and BKSP BKSP (FF). The RF ON line should toggle from 0 Vde to -10 Vde. If there is no change, check U8, pin 12, for high and low levels. If the output is locked high, check the protection diode, CR3, before replacing U8. However, if CR3 is open, U8 may be damaged by actuating the relay. If the output at pin 12 is locked low, replace U8. If U8 pin 12 changes levels properly, replace relay K1.

#### Miscellaneous

The EXT/MTR ALC CAL offset is generated by A1 potentiometer, with the wiper running between  $\pm 10$  Vdc and  $\pm 10$  Vdc. If the signal is absent, check for the  $\pm 10$ V and  $\pm 10$ V supplies. If the offset voltages still cannot be produced, replace the defective potentiometer, R4.



SERIAL PREFIX: 2146A

A DESCRIPTION OF THE PARTY OF T

P/0 #4 P/0 A13	YIG OSC
• >	ON
P/0 NI4 P/0 AIG SPLITTE I4 >	MOD/ R on
P/O A5 FM DRIVER	
P/O A4 ALC PI 76 C FALG TRF V	
	y/GH2 .

Kay	Code	Column	Row	
POWER SWEEP	95	i)	0	
POWER LEVEL	9A	0	L	
SLOPE	4)4)	0	2	
RF	98	0	3	
CW FILTER	92	1	ł	
NOT USED	91	L	2	
NOT USED	90	1	3	
NOT USED	86	1	U	
NOT USED	8A	3	1	
NOT USED	89	1	2	
NOT USED	**	2	3	
INT	82	3	L	
EXT	81	3	2	
MTR	80	,1	3	

Table 8-8. Plug-In Key Codes

• ••

If depressing a key results in the wrong keycode being displayed, read the associated column and row lines. Troubleshoot with a continuity checker. If the matrix lines are good, suspect A2U6.

No keycode is defined for Row 0 at Column 1 or Column 3. A problem in this area of the matrix may result in Error Code E051.

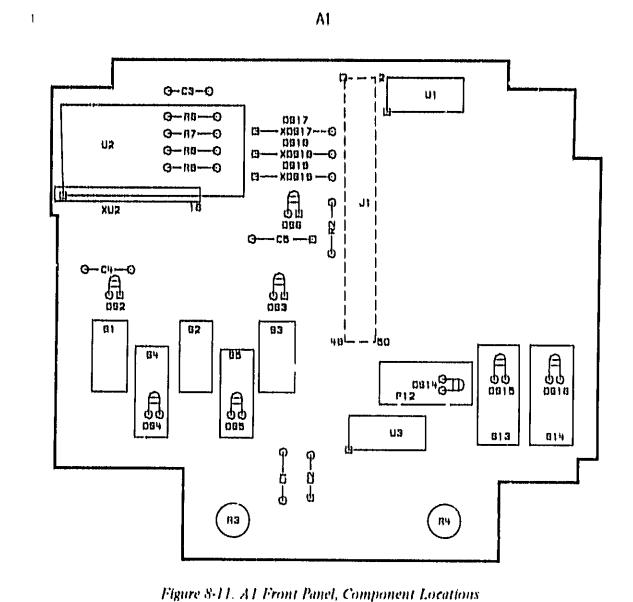


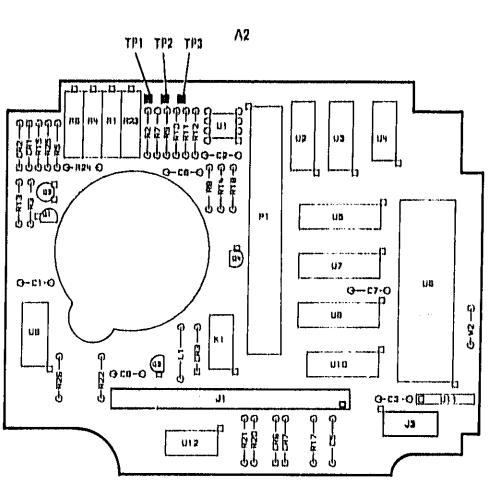
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Figure 8-10, A1 Front Panel/A2 Front Panel Interface, Block Diagram

Figure 8-18, A1 Front Panel/A2 Front Panel Interface, Schematic Diagram

REALIZE





Shaded components on far side,

Figure 8-12, A2 Front Panel Interface, Component Locations

## NOTES

1. THE FOLLOWING KEY ENTRIES PROVIDE FRONT PANEL ACCESS FOR A DATA WRITE/READ OPERATION TO/FROM THE ADDRESSED LOCATION:

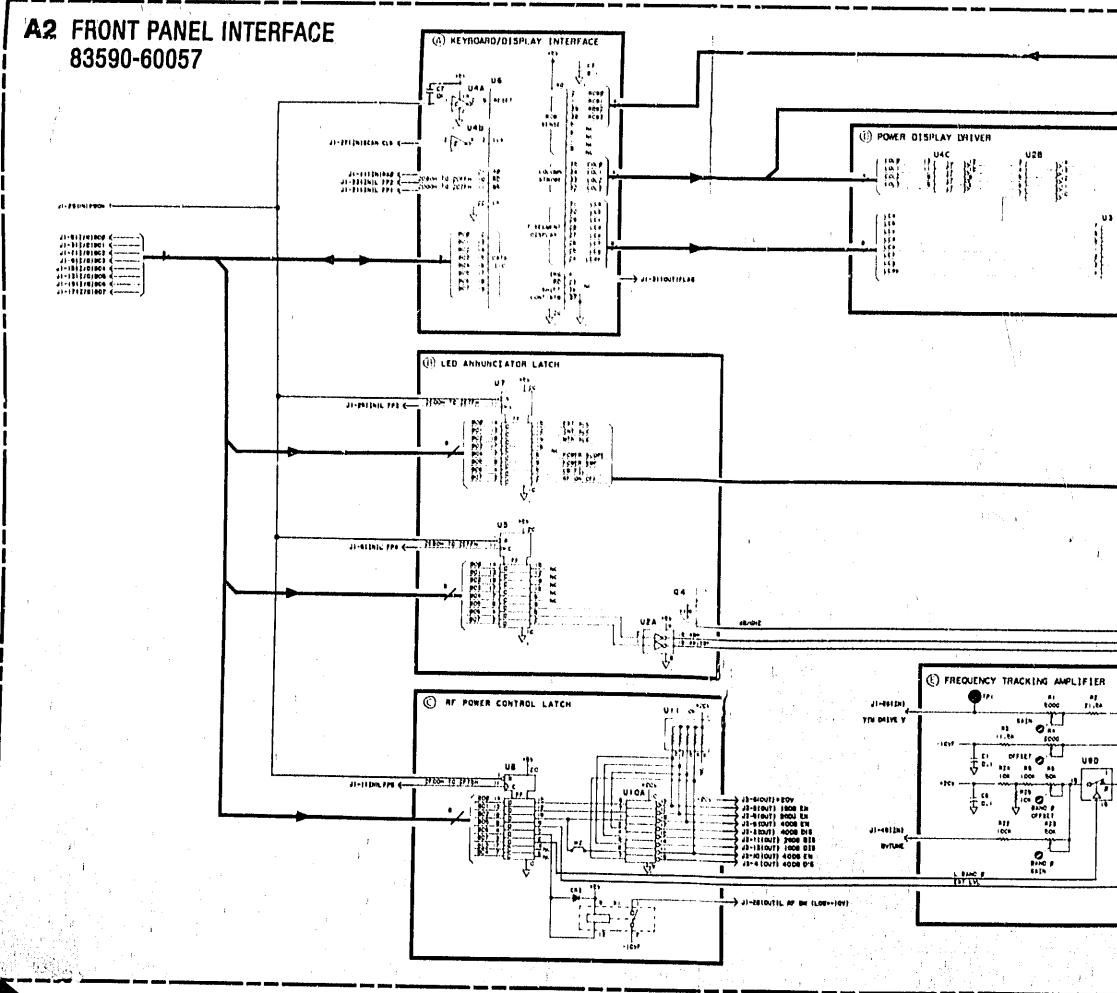
FUNCTION *Hex Address Entry Hex Data WRITE Hex Date HEAD **Hex Data Rotation Write** 

Hax Addressed Fast Head

KEY ENTRY SHIFT O O (enter hex address) M2 (enter data: two hax digits) M3 M4 M5

*TO ADDRESS A DIFFERENT LOCATION, PRESS MI AND ENTER THE NEW ADDRESS, OR USE THE INCREMENT KEYS 📣 🗢 TO STEP TO THE NEW ADDRESS. TO PREVENT THE MICROPROCESSOR FROM SERVICING THE BANDSWITCH INTERRUPT, PRESS

8350A CW .



PREFIX: 2148A

PIN	SIGNAL	1/0	толяном	FUNCTION
1	L FP5 +5V	IN IN	A3P1-30 A3P1-6,7	C 0
3	801	1/0	A3P1-9	ABC
4	UN LMP EN			F ADD
0 (j	BDD L FP4	1/0 1N	A3P1-31 A3P1-26	ABC B
7	BD2 GND DIG	1/0	A3P1-32	ABC
0 10	803	1/0	A3P1-10 NOT USED	ABC
11 12	OAO L UNLVL	IN IN	A3P1-33 A4P1-2	A F
13 14	806	1/0	A3P1-13 NOT USED	ABC
16 16	804	1/0	A3P1-36 NOT USED	ABC
17 18	807	1/0	A3P1-14 NOT USED	ABC
10 20	806	1/0	A3P1-36 NOT USED	ABC
21 22	L FP1	IN	A3P1-16 NOT USED	A
23 24	L FP2	IN	A3P1-37 NOT USED	٨
26 26	L FP3	IN	A3P1-16 NOT USED	ß
27 28	SCAN CLK	IN	A3P1-38 Not Used	A
29 30	PWON	IN	P2-25 NOT USED	ABC
31 32	FLAG	OUT	A3P1-42 NOT USED	٨
33 34	PIRPGD	OUT	NOT USED P2-61	
36 36	PIRPGB FREQ TRK V	OUT OUT	P2-60 A4P1-36,A5P1-24	E
37 38	FREG CAL L RF ON	OUT OUT	A8P1-23 A10J4-G,A10J5-14	C
39 40	YTM DRIVE V -10V	IN IN	A7P1-23 P1-13	E O
11 42	EXT CAL +20V	OUT IN	A4P1-24 P1-7	0
13 44			NOT USED NOT USED	
15 46	+10V	IN	NOT USED PI-8	0
7 48	GND ANLG		NOT USED	0
0 60	BVTUNE 1V/GHz	IN OUT	AGP1-42 J4, A 10J2-23	EG

		A21	1 – AIJT INTER	ACONNECT JA	ak	
	A2P1					A1J1
	PIN	BLOCK	BIGNAL	TO/FROM	BLOCK	PIN
	1	0 0	Ch Ca	×+∳ ∳	ĸ	1 2
	9 -1	0 0	0101 Cc		ĸ	3
	<u>م</u> 6	D A	DIG2 COL2	··••	K	<u>5</u> 6
	7	a a	0163 Cil	·••	ĸ	7 8
	9 10	D A	D164 COL1	*** **********************************	K	10
	11	A A	COLO COL3	-+	J	11
	13 14	0 0	Ce Cdp	··	ĸ	13
	15 16		Cf ROW2	·• ••	K	15 16
	17 18	D A	Cu Nowa	-+	K	17
	10 20	N	+6V NOW1		U J	10 20
ľ	21 22	N	GND DIG ROW1			21 22
	23 24		NOT USED NOT USED	-		23 24
ŀ	25 26	U	db/SWP NOT USED	••	H	25 26
ŀ	27 20		FRED CAL NOT USED	8-	L	27 28
-	20 30	<u>u</u>	dBm NOT USED	-•	H	20 30
ľ	31 32	N	GND ANLG NOT USED		0	31 32
ſ	33 34	B	dB/GH7 NOT USED	•	н	33 34
ľ	35 36	N B	+10V POWER SWP	•	0 H	35 36
ľ	37 38	B	EXT CAL PWR SLOPE	•- -•	L H	37 38
ŀ	39 40	 B	NOT USED CW FIL	-•	н	39 40
	41 42	B	PINPGB RF ON/OFF	•		41 42
	43		PIRPGA NOT USED	•-	1	43 44
ŀ	45 46	0	NOT USED MTR ALC	-+	н	45 46
ŀ	47 48	в	NOT USED EXT ALC		<u>н</u> Н	40 47 48
┢	49 50	FB	UNLEVELED	-+	H H H	49 50
L	55			·	<u>n</u>	uu -

		6CAN U4B,	I CLK PIN 3	ſ
	COL 3 DIG 1	UB, PI J2, PI	N 32 N 3	•
	COL 2 DIG 2	UG, PI J2, PI	IN 33 N G	ł
	COL 1 DIG 3	116, PI 32, PH	N 34 N 7	P
	COL Ø DIG 4	UG, PI J2, PI	N 35 N U	-
PIRPG	IA A10J	1-43		Ģ
PINPO	30 A10J	1-41		
			-4	

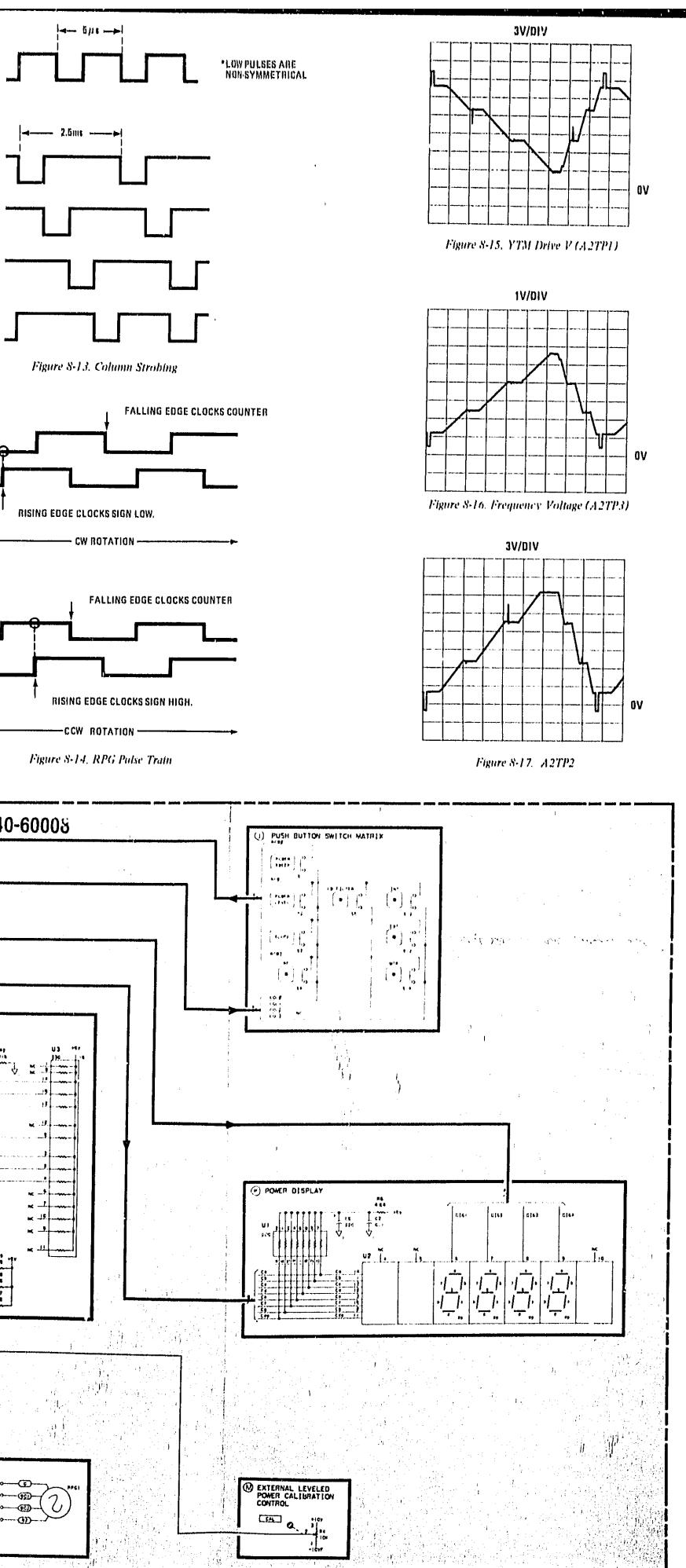
PIRPGA A10J1-43

PIRPGB A10J1-41

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	A1 FRONT PANEL 83540
	$4 \xrightarrow{(15)2 \dots (15)2}_{(5)1 \dots (15)2} 4$ $(5)1 \xrightarrow{(15)2 \dots (15)2}_{(5)1 \dots (15)2}$ $(9)1 \xrightarrow{(15)2 \dots (15)2}_{(15)2 \dots (15)2}$ $4 \xrightarrow{(15)2 \dots (15)2}_{(15)2 \dots (15)2} 4$
1997 - Andrew State Construction of the Andrew State Construction	$   \begin{array}{ccccccccccccccccccccccccccccccccccc$
· · · · · · · · · · · · · · · · · · ·	59 ( , <u>59</u> 59 ( , <u>6459</u> 59 ( , <u>6459</u> 59 ( , <u>6459</u> 59 ( , <u>6459</u> 59 ( , <u>6459</u> (1) LED ANNUNCIATORS
A-AIRIUM, WARK S SIT (47)	
	UI-BAIDUTIPEAPEA



#### A3 DIGITAL INTERFACE. CIRCUIT DESCRIPTION

The A3 Digital Interface assembly receives digital address, data, and control signals from the 8350A Sweep Oscillator. These signals are processed and then routed to the rest of the RF Plug-in. The ROM (Read-Only Memory) contains software dedicated to the RF Plug-in. The Interrupt Control circuit provides timing signals (which are controlled by the 8350A A3 Microprocessor) during band-switching and at the beginning and end of each sweep. The A3 Digital Interface also provides data and timing information for the A2 Front Panel Interface and AI Front Panel assemblies, as well as data, address and control signals for the rest of the RF Plug-in.

#### Sweep Oscillator Interface (A)

The digital data, address, and control signals from the 8350A Sweep Oscillator pass through the RF Plug-in interconnect and ribbon cable to Ji on the A3 Digital Interface assembly. They are buffered and inverted by Schmitt trigger inverters before passing on to the rest of the RF Plug-in, 100-ohm resistors in series with each line are included to reduce ringing on the instrument bus. U7A and U7D enable the bi-directional data buffer when either the Plug-in ROM (L BPIROME) or the Plug-in itself (L BI/OE2) is enabled. Blanking pulse L BP2 passes directly through A3 and is not buffered. It is used on the A2 Front Panel Interface for blanking the UNLEVELED light during retrace. Lastly, U10F receives the FLAG from the A2 Front Panel Interface and passes it back to the Sween Oscillator.

#### Address Decoder (B)

The Address Decoder decodes the address and control lines to provide control signals throughout the RF Plug-in. Table 8-9 shows the decoded address lines and where they are used in the RF Plug-in.

#### ROM (C)

The RF Plug-in's Read-Only Memory consists of two 4k by 8-bit ROMs. This memory contains all of the firmware dedicated to the individual RF Plug-in for use by the microprocessor in the 8350A. Addresses 4000H through 4FFFH are read from UI, while 5000H through 5FFFH are found in U2. The A12 line. decoded in the Address Decoder, selects which ROM is enabled. The remaining twelve address lines (A0 through A11) determine the individual ROM address being read.

#### 200 kHz Clock (D)

U3 is a simple oscillator with external timing elements configured to provide a stable 200 kHz pulse train. This signal is used to clock the Interrupt Control counters in U5 for interrupt timing. The 200 kHz clock is also used on the A2 Front Panel Interface to scan the keyboard and refresh the display.

#### Interrupt Control/Configuration Switch (E)

Triple programmable counter U5 contains three programmable down-counters and control circuitry. The counters are preloaded by the data bus, then downcounted by the 200kHz Clock. When the count reaches zero, a pulse is produced on the corresponding output. In this way, the microprocessor can command a time interval of any duration, and will receive an interrupt when the count-down is complete.

#### Table 8-9. Digital Interface Address Decoding

Mnemonia	Addross	Aildress Decoder Components	Components Addressed	Noail or Write	Description
L WR	28001146 2871511	(4)	A3U5	Witte	Write data to program mable interval tinser.
L RD	288011 10 261444	UP)	A3U5	Read	Read data from progr mable interval timer.
L PIAE	290011 to 2915141	U7B, U7C, U8A, U10D	Азця	RD/WR	Enable Peripheral Inte face Adapter, (Also addressed 2B00H to 2BFF)
I. INSTI	2C0011 to 2C71714	UTOD, UT3	A4, A5, A6	Write	Write control for Ad- ALC, A5 FM Driver, and A6 Sweep Contro
L INST2	2C8011 to 2C171711	U)0D, 1113	А7, А8	RD/WR	Write to A7 YTM Driv and A8 YO Driver Control and read Offs and Gain switches,
L FPI	2D00H to 2D7FH	U10D, U13	Λ2	Write	Write to front panel displays.
L FP2	2D80H to 2DF941	U10D, U13	λ2	Read	Read front panel keyboard.
1 FP3	2E0011 (o 2E71-11	U10D, U13	Λ2	Write	Write to front panel annunciators
I. 1/D4	2158011 to 21517511	U10D, U13	A2	Write	Write to front panel annunciators
L FP5	2150013 to 21571511	U10D, U13	٨2	Write	Write to RF control latch
L ROMI	400011 to 4FFFH	U6C, U10A, U10B	A3U1	Read	Fnable ROM UI
L ROM2	500011 to 5151511	U6B, U10B	A3U2	Read	Enable ROM U2

U4 is a Peripheral Interface Adapter (PIA) which controls the interrupts from U5 and reads the configuration switch, S1. As an interrupt controller, U4 can be microprocessor-programmed to mask or enable any of four possible interrupts. These interrupts mark the end of important timing intervals used during bandswitching.

Configuration Switch SI is encoded with information about the type of RF Plug-in and the options included, as well as operator-chosen parameters such as FM sensitivity and power-up conditions. (See Table 8-10 for details.) The microprocessor addresses U4 to read the switch status at power-on or when

Instrument Preset is initiated, and uses the information in subsequent calculations involving frequency range, power range, marker values, and many other Plug-in dependent parameters.

#### RF Plug-In Interface (F)

U17 and U14 buffer the address and data signals required throughout the rest of the RF Plug-in, U17 is a bi-directional, 8-bit data buffer, enabled when BI/OSTB, A10, and BI/OE2 are all high. Its direction is controlled by the L WRITE line, UH is enabled by L BI/OE2 to pass four address lines (A0 through A3) to the rest of the RF Plug-in's circuitry.

#### TROUBLESHOOTING

The A3 Digital Interface assembly is the principle exchange for digital data, address, and timing signals used throughout the RF Plug in. The Read Only Memory (ROM) on the A3 assembly contains software and constants used for Plug-in interrupt routines. Major enable lines used on the front panel and throughout the Plug-in are decoded on this assembly. Note that some digital control lines (e.g. the Stop-Sweep Request (L SSRO) and RPG lines) do not pass through the Digital Interface assembly.

A failure in the A3 Digital Interface typically disables the entire RF Plug-in, and causes large errors in frequency, amplitude, and control. The front panel displays will probably be inoperative, and front panel controls will not produce any effect.

The 8350A Sweep Oscillator may or may not be disabled by a Plug-in failure. A simple test to determine whether the 8350A is at fault is to remove the Plug-in and press INSTR PRESET on the 8350A. If E001 is displayed, the 8350A is probably good. A different error code, especially E005, indicates problems in the 8350A

#### General Troubleshooting

Visually inspect the Plug-in for damage, frayed cables, and loose connectors. Check ribbon cable W29 between the Plug-in interface and A3 assembly. Check the ribbon cable in the 8350A leading from its motherboard to the Plug-in interface.

Check the +5VB line at A3J1 pins 35, 36, or 38, to make sure power is being supplied to the Plug-in. The A3 assembly supplies +5V to the rest of the Plug-in; check A3P1 pins 6 or 7 for +5Vdc.

Check configuration switch A3S1 and make sure that it corresponds to the model, options, and user-configurations as shown in Table 8-10.

The A3 Digital Interface assembly is made accessible for service with the following procedure:

- 1. Remove the RF Plug-in from the 8350A.
- 2. Disconnect W29P1 from A3J1, and remove the A3 assembly from the Plug-
- 3. Replace the Plug-in in the 8350A.
- 4. Remove the top cover of the 8350A.

- 5. Insert a 44-pin extender board into A10XA3.

Make sure that the A3 assembly is firmly seated into its motherboard socket, and that ribbon cable connections are making good contact. Perform the Hex Data Read by entering: SHIFT 0 0 Enters the Hex Data command 4 0 0 0 Address location 4000 M3 Hex Data Read The 8350A FREQUENCY/TIME display should indicate 55; increment the address to 4001 by pressing 
, the FREQUENCY/TIME display should indicate AA. If these numbers are read, the data lines and the 4000H ROM enable line are functional. If these tests do not execute, run the Hex Data Rotation Write by entering: SHIFT 0 0 Enters the Hex Data Write command Address location 4000 4 0 0 0 Må Hex Data Rotation Write Check the 4000H line to UI for activity, and troubleshoot the address decoding circuitry if there is none, Repeat the above key sequence substituting address location 5 0 0 0. Check the 5000H line to U2 for activity. The address lines can be checked by using the Hex Data Write feature of the 8350A. Alternate ones and zeros are written on the address lines when writing to address location 5555H or 2AAAH. By performing a Hex Data Write to each address location, all thirteen address lines are pulsed high and low. On the 8350A, enter: Enters the Hex Data Command SHIFT 0 0 Address location 5555 5 5 5 5 Hex Data Rotation Write Check that all even address lines (A0, A2,... A12) are pulsed high, and all odd address lines (A1, A3, . . . A11) are low. On the 8350A, enter: SHIFT 0 0 Enters Hex Data command Address location 2AAA 2 . . . Hex Data Rotation Write M4 Check that all odd address lines are pulsed high and all even address lines are Other Error Codes Error Codes E052 and E053 indicate a failure on the A3 Digital Interface assembly. These codes, along with troubleshooting hints related to that error, are listed below. Error Code EO52 Error Code E052 indicates a failure in Triple Programmable Timer U5 or the 200 kHz Clock 8-32

and a second s

6. Install the A3 assembly on the extender board, and reconnect W29P1. RF Plug-in Solf Test Major portions of the A3 Digital Interface assembly and the Instrument Bus Instrument Preset or nower-on. The Plug-in ROM is tested by rending a test pattern out of ROM, then ensures that the data bus, address bus, and major timing lines to the A3 Instrument Bus. normal operation, and are discussed in greater detail below. The L IRD, FLAG, and PIIRQ lines are not tested by the routine, nor are the internal data (BD0 - BD7) and address (BA0 - BA3) busses. An Error Code indicates a failure in specific components. If Self Test passes, these components are very probably working correctly. Hence, the troubleshooting information below is broken into three sections: • Error Code E001 "Plug-in Failure" • Other Error Codes • No Error Code Displayed Refer to the appropriate section indicated by the Self Test results. • 8350A/Plug-in interface • Connections between 8350A/Plug-in interface and A3 assembly • Plug-in buffers • ROM Address Decoding ROM

connecting it to the 8350A are tested by the Self Test routine performed at performing a "checksum" on the entire range of ROM. If the test passes, this assembly, as well as the ROM address decoding and ROM itself, are good. If the test fails, error code E001 appears, indicating a fault in these components or the Other Error Codes (between E050 to E099) indicate specific problems in the Plug-in. These can occur either at Instrument Preset or power-on, or during

Error Code E001 Error Code E001 indicates a failure in one or more of the following areas: • Connections between 8350A/Plug-in interface and Instrument Bus The Instrument Bus internal to the 8350A is checked during Self Test and will produce error E005 on failure. However, branches from the Instrument Bus leading to the Plug-in are not tested. In the 8350A, check cables between the Motherboard and the 8350A chassis connectors J2 and J3 leading to the Plug-in for damage or loose connections. Likewise, in the 83590A, check the cabling between chassis P1 and P2 and the Al0 Motherboard or A3 Digital Interface. Next, check the individual pins and sockets of the 8350A/Plug-in interface connectors for bent or missing pins.

- _____ igramnier. program
- mer. Interlso
- 14
- ver. ontrol f Driver
- Offset

#### Model 83590A

First check the 200 kHz Clock. The SCAN CLK line is accessible at U3 pin 3, at the top of the A3 assembly, so it is not necessary to remove the A3 board to test it. The output frequency should be approximately 200 kHz. The palse train is NOT symmetrical, and has TTL levels. If no clock signal is found, suspect U3.

If the SCAN CLK is present, yet E052 occurs, then the failure is probably with U5. Press SHIFT 5 5, and check the L WR and L RD lines for the waveforms shown in Figure 8-21. If either control line is inactive, troubleshoot the address decoder U9. If the control lines are working, check the CTR 0 and CTR 1 waveforms as shown in Figure 8-21. If they are incorrect, replace U5.

#### Error Code E053

E053 generally indicates a failure in the PIA, U4. However, the problem might be in the output stages of U5. Enter SHIFT 5-5, and check CTR 0 and CTR 1 waveforms as shown in Figure 8-21. If they are correct, U5 is functional. Next, check the L PIAE line as shown in Figure 8-21, and make sure the L WRITE line shows activity. If not, troubleshoot the appropriate address decoding circuitry or buffer. Then, check L PIIRQ for the squarewave shown in Figure 8-21. If it is inactive, replace U4.

#### No Error Code

It no error code occurs and the 0350A displays show the correct start and stop frequencies of the Plug-in, the Plug-in Self Test passed successfully. This verifies the Instrument Bus to the Plug-in, data and address busses on the A3 Digital Interface assembly, and Plug-in ROM. Any Plug-in failures which are traced back to the A3 assembly are due to failures in one or more of the following areas:

- Address Decoding
- Plug-in Buffers
- Interrupt Control/Configuration Switch
- Miscellaneous Control Lines

If problems occur only when a multiband sweep is performed, suspect the programmable timer, U5. If the 8350A displays show the wrong frequencies, first check configuration switch S1 against Table 8-10, and then troubleshoot the PIA, U4.

#### Address Decoder

The primary address decoding for the Plug-in occurs on the A3 assembly. The enable lines are then passed on to the rest of the instrument. The Major Address Decoder Test can be utilized to check all these lines. Enter:

#### SHIFT 5 3

Then check the outputs of U6B, U6C, U7B, U9, and U13 for the signals shown in Figure 8-22. The address lines have been verified by the Self Test. Therefore, if the L PIAE or ROM enable lines are faulty, troubleshoot the discrete address decoding logic involving U6, U7, U8, and U10, and replace the defective component. If other pulses are missing or displaced, replace the appropriate decoder, U9 or U13.

Service

#### Plug-In Interface

U14 and U17 buffer the address and data lines for use throughout the Plug-in. The address and data busses on the A3 assembly have been verified by the Instrument Preset Self Test. Therefore, if address or data is not being passed to another assembly, the fault lies with U14, U17, U6A, or a motherboard connection.

The address lines can be exercised by performing the Minor Address Decoder Test. On the 8350A, enter:

SHIFT 5 4 Minor Address Decoder Test

Verify activity on each of the buffered address lines (BA0 - BA3).

Data lines can be verified by performing a Data Rotation Write to any address location between 2C00H and 2FFFH. On the 8350A, enter:

CW SHIFT 0 0	Set 8350A into CW mode Enters the Hex Data command
2 GHz 6 0 0 M4	Address location 2C00
141.4	Hex Data Rotation Write

Check for activity on each of the buffered data lines (BD0 - BD7), and check for shorts between lines.

#### Interrupt Timer/PIA

The PIA is responsible for two functions:

- Reading the Configuration Switch
- Routing the Interrupts from the Triple Timer

#### NOTE

Before changing the Configuration Switch settings, write down the switch positions and return the switches to their original settings after troubleshooting.

The PIA's read capability can be checked by entering:

CW	Sets the 8350A into CW mode
SHIFT 0 0	Enters Hex Data command
2 9 0 0	Address location 2900
M3	Hex Data Read

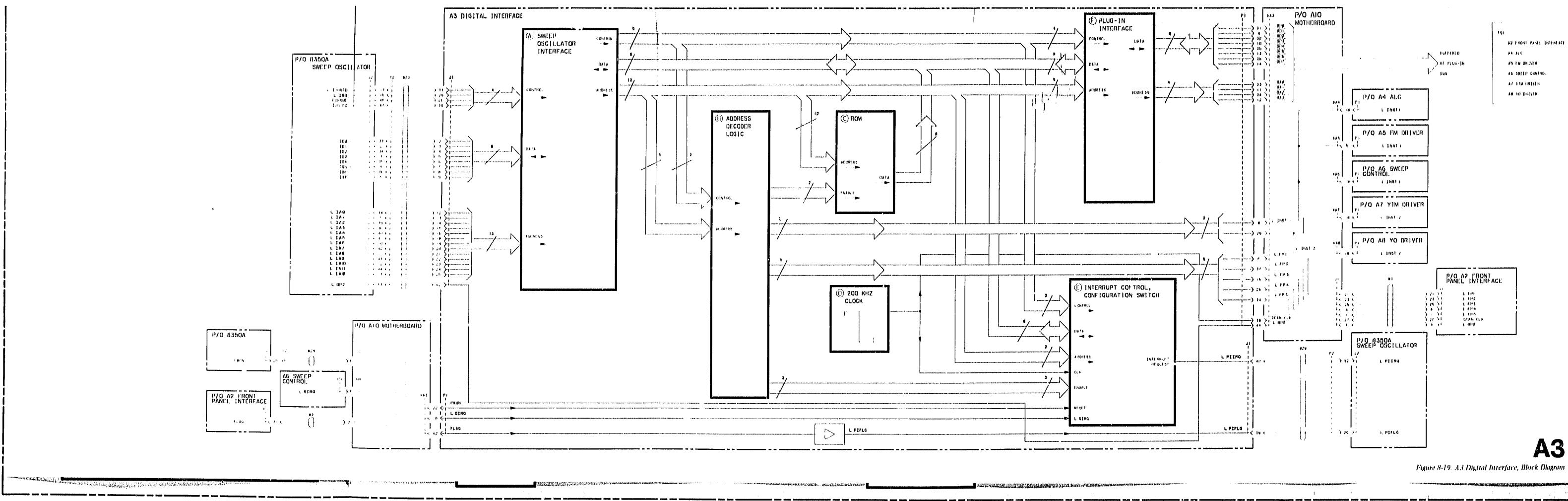
Watch the display change as the Configuration Switch is toggled.

The Triple Timer and PIA's interrupt masking capability are tested using a special routine at INSTR PRESET or power-on. Error Codes E052 or E053 are displayed if a failure is detected. If these error codes are found, or if either U4 or U5 are suspect for other reasons, a special test pattern can be accessed by entering:

#### SHIFT 5 5 Interrupt Control Test

The waveforms shown in Figure 8-20 should be observed. Refer to "Other Error Codes" for details on these error codes and the SHIFT 5 5 Operator Initiated Self Test.

-----



SERIAL PREFIX: 2146A

Figure 8-23, A3 Digital Interface, Schematic Diagram



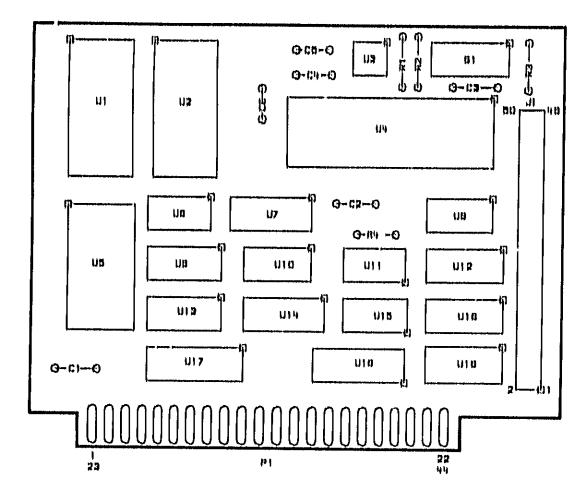


Figure 8-20 A3 Digital Interface, Component Locations

#### NOTES

1. THE FOLLOWING KEY ENTRIES PROVIDE FRONT PANEL ACCESS FOR A DATA WRITE/READ OPERATION TO/FROM THE ADDRESSED LOCATION

FUNCTION *Hex Address Entry

Hox Data WRITE

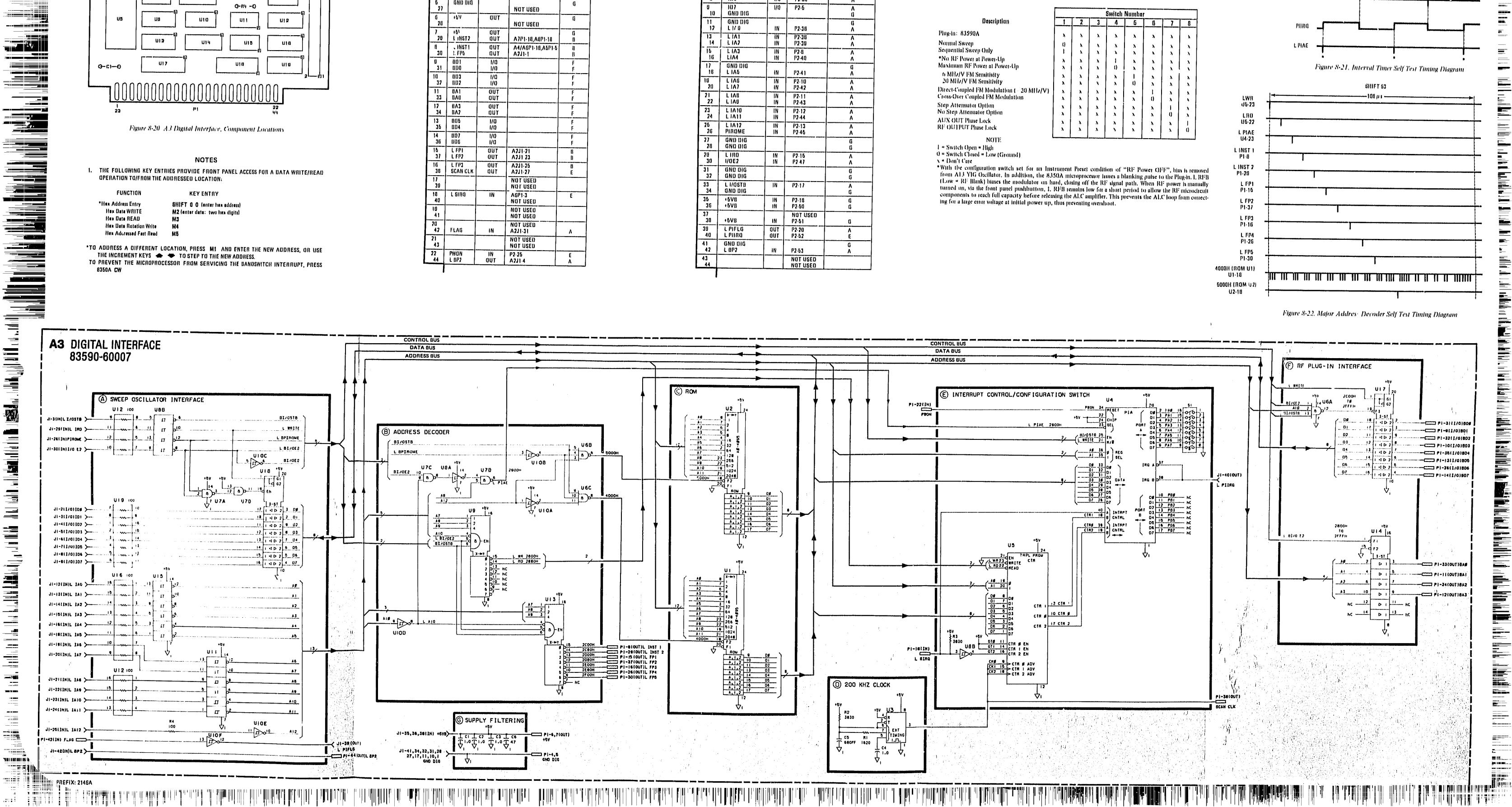
Hex Data READ

____

----

____

- KEY ENTRY SHIFT 0 0 (unter hen address) M2 (enter date: two hex digita) Mt Hex Date Rotation Write M4 Han Aduressed Fast Read Mő
- TO ADDRESS A DIFFERENT LOCATION, PRESS MI AND ENTER THE NEW ADDRESS, OR USE THE INCREMENT KEYS 🔶 🗢 TO STEP TO THE NEW ADDRESS. TO PREVENT THE MICROPROCESSOR FROM SERVICING THE BANDSWITCH INTERRUPT, PRESS 8350A CW



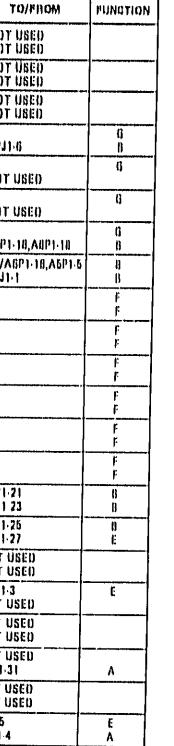
	1 23			NOT USED NOT USED
	2 24		••	NOT USED
	3 26		**	NOT USED
	4 26	OND DIG L FP 4		A2J1-6
	6 27	OND DIG		· · · · · · · · · · · · · · · · · · ·
	6	+6V	our	NOT USED
	20	+61		NOT USED
	20	L INST2		A7P1-18,A8P
	8 30	. INST 1 1. FP6		A4/A6P1-18, A2J1-1
	8	801 000	1/0 1/0	***
	10	803 002	1/0 1/0	
	11	UAI	OUT	
	12	BAU		•
		BA2	OUT	
	13 35	805 804	1/0 1/0	
	14 36	807 806	1/0 1/0	
	15 37	L FP1 L FP2	UUT OUT	A2J1-21 A2J1 23
	16 38	L FP3 6CAN CLK	UUT OUT	A2J1-25 A2J1-27
	17			NOT USED
	18	L SINO	IN	AGP1-3
	40	·		NOT USED
	41			NOT USED
	20 42	FLAG	IN	NOT USED A2J1-31
	21 43		<del></del>	NOT USED NOT USED
	22 44	PWON L BP2	IN OUT	P2-25 A2J1-4
	the second se			

A921

PIN

BIONAL

1/0



PIN	SIGNAL	1/0	πο/۴ηρη	FUNCTION
1	AND DIG 100	1/0	P2-33	
3	101	1/0	P2-2	×
<u>4</u>	102	<u> </u>	P2-34	Λ
15 13	103 104	1/0 1/0	P2+3 P2+36	
7 13	105 106	1/0 1/0	P2-4 P2-30	٨
- U	107	1/0	P2.6	ΛΛ
	GND DIG			0
11	GND D10   L17 D	IN	P2-38	ů A
13	LIAI		P2-38	<u> </u>
14	L 1A7	<u>IN</u>	P2-30	Ä
16 16		IN IN	P2-8 P2-40	Λ Λ
17	GND DIG			<u> </u>
10	LIAS	IN	P2-41	Ä
18 20	L 1AB L 1A7	IN IN	P2-10 P2-42	A
21	LIAB	IN	P2-11	Α
22 23		<u> </u>	P2-43	Α
24	L 1A10 L 1A11	IN IN	P2-12 P2-44	A A
26	LIA12	IN	P2-13	٨
26	PIROME GND DIG	<u> </u>	<u>P2-46</u>	<u>^</u>
28	GND DIG			0 0
20 30	LIRD	IN	P7-15	٨
30	1/0E2 GND DIG	IN	P2 47	<u>^</u>
32	GND DIG			6 6
33 34	L I/OSTB	IN	12-17	٨
36	GND DIG +5VB		P2-18	0
36	+5VB	IN IN	P2-50	G G
37	. 2310		NOT USED	
30 39	+6VB L PIFLG		P2/51	6
40	LPHRQ		P2-20 P2-52	A E
41 42	GND DIG			G
43	L BP2	IN	P2-63 NOT USED	Α
44			NOT USED	

				Switch	Numba	r		
Description		2	3	1	6	ß	7	6
Plug-in: 83590A	X	A A	X	X	X	>	λ	×
Normal Sweep	0	X		X	N	X	X	
Sequential Sweep Only		X	Ň	X	Ň	l X	ŝ	
No RF Power at Power-Up	λ	λ		1	X	X		
Maximum RF Power at Power-Up	- X -	3	X	0	X	X		
n MH7/V FM Sensitivity 20 MH7/V FM Sensitivity	x x	X X	x	X	0	X	x	X
Direct-Coupled FM Modulation (= 20 MHz/V)	x	x	X	X X	X		A A	х Х
ross-Over Coupled FM Modulation	- X	λ	X	X	- <b>N</b> -	0	λ.	٩.
tep Attenuator Option	- X	X	X	N	А	λ		Ň
to Step Attenuator Option	- X	λ	×	× 1	- X	λ	0	- λ
AUN OUT Phase Lock AF OUTPUT Phase Lock	X	X	N N	X	A X	N N	X	 0

1 . Switch Open # High 0 = Switch Closed = Low (Ground)

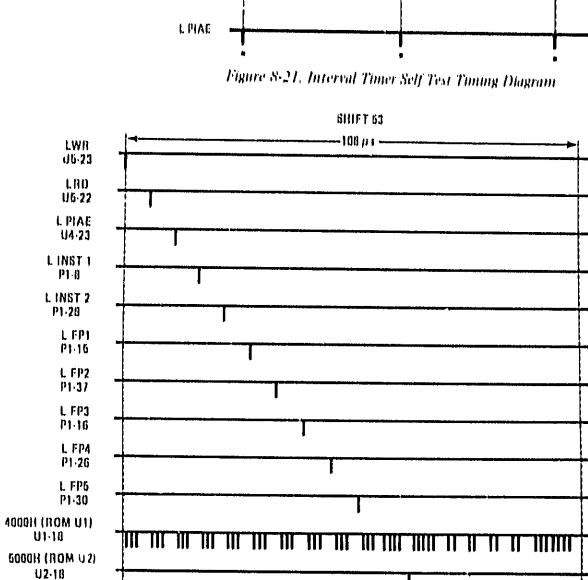
x # Don't Care

"With the configuration switch set for an Instrument Preset condition of "RF Power OFF", bias is removed from A13 YIG Oscillator. In addition, the 8350A microprocessor issues a blanking pulse to the Plug-in, I. RFB (Low # RF Blank) biases the modulator on hard, closing off the RF signal path. When RF power is manually turned on, via the front panel pushbutton, I. RFB remains low for a short period to allow the RF microcheult components to reach full capacity before releasing the ALC amplifier. This prevents the ALC loop from correcting for a large error voltage at initial power up, thus preventing overshoot.



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Table 8.10. Configuration Switch on 3.3 District Interface Road



I, WB

CTHO

CHTI

PHRO

*NOTE: THESE DEPRESENT

MULTIPLE PULSES

OCCURING IN OUICK SUCCESSION.

6HIFT 65

Figure 8-22. Major Address Decoder Self Test Timing Diagram

#### A4 AUTOMATIC LEVELING CONTROL (ALC). CIRCUIT DESCRIPTION

The A4 Automatic Level Control (ALC) assembly is part of a closed loop por leveling function, designed to control the amplitude of the RF output poy The General section below describes loop operation, including so components external to the A4 assembly. The rest of this operational theory is devoted to detailed description of the circuits found on the A4 assembly.

#### Gonoral

The circuits which accomplish power control and power leveling can be broken into two categories: internal loop circuitry, and external components of the loop. Figure 8-24 illustrates this theme.

The Power Level Reference leg of the ALC establishes the desired power level. This is accomplished by pressing the Plug-in POWER LEVEL pushbutton and rotating the RPG or entering the desired reference on the 8350A front panel DATA LNTRY keys. This leg of the ALC is not an interdependent part of the toop as shown in Figure 8-24.

The Detector leg of the ALC loop samples the actual RF output power and produces a voltage proportional to RF amplitude. This voltage is converted to log scale and compared with the Power Level Reference signal. If the voltages at the summing junction (TP4) are not of equal magnitude an error voltage is generated. This error voltage is amplified and converted to a current drive for the RF modulators which vary the transmitted RF power to correct the error and achieve the desired RF power level.

#### Address Decoder and Control Latches (A)

U12 is a 3-to-8 decoder, selecting address 2C0711 when it is present on the address hus. This address serves as a chip enable for octal latch U13. Information on the data bus is then latched into U13 and used throughout the A4 assembly.

#### Detector inputs and Selection Switches (B)

Control lines MUX A0 and MUX A1 are encoded with leveling mode and band selection information. The lines are decoded in Table 8-12, U6 decodes these control lines to select the proper detector input for the desired operating mode.

EXT/MTR ALC input provides external crystal leveling canability within the -10 to -200 mV range, VR1 and VR2 provide protection against transients. Two schottky diodes, CR2 and CR3, are mounted between the ENT/MTR ALC connector and the front panel casting for similar protection.

When MTR (power meter) leveling is selected, UI inverts the positive RECORDER output (approximately 0 to +1 Vdc full scale) of the HP 432A, R41 and C9 compensate for power meter response. Additional compensation occurs in the Main ALC Amp (1).

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Sample and Hold Driver (H)

Q2B switches between saturation and cutoff, controlling both of the sampling FETs, Q1 and Q3. The Sample and Hold function of the ALC loop is used in conjunction with pulse modulation. When PULSE ENABLE is high, and either I. PULSE or SQ MOD input is low, Q2B will saturate, initiating the Hold mode,

The frequency of the sampling mode is dependent on the L PULSE or SO MOD input. When the system is used with the HP 8755 Swept Amplitude Analyzer, the SO MOD input will be a 27.8 kHz square wave, controlling the gates of Q1 (D) and Q3 (Q). (Refer to 8350A Operating and Service Manual, Section V, for 27.8/1 kHz Oscillator adjustment.) This ensures that sampling occurs only during the ON pulse. The sample level is maintained during the OFF pulse, thus preventing saturation of the Log and Main ALC amplifiers.

The SQ MOD input is also connected to the PIN Mod d and PIN Mod 1 Drivers (C) for RF modulation when using the 8350A internal squarewave modulation.

#### Input Sample and Hold (D)

The Input Sample and Hold function prevents the Log Amplifier from saturating during pulse modulation.

U8 is a unity gain follower with internal feedback which buffers the detector input. R59 compensates for the offset voltage of the operational amplifier. QI and Cll perform the sample and hold function. O7 and O8 in the Log Amplifier select the appropriate detector return for INTernal and EXTernal leveling modes.

#### Log Amplifier (E)

The logarithmic scaling function is performed by Q6A in the feedback loop of U7. Q6A collector current is proportional to the voltage at TP12 and exponentially related to its base-emitter voltage. Therefore, Q6A emitter voltage is logarithmically related to the input voltage at TP12.

Q6B compensates the Log Amp against changes in reverse saturation current with temperature.

CR4 provides a positive current path preventing U7 from saturating when the input is greater than or equal to 0 volts.

U6 decodes MUX A0 and MUX A1 (Table 8-12) to select the proper offset voltage for power calibration at the low end of the Plug-in power range. In EXTernal ALC, the power level calibration is set with the front panel EXT CAL potentiometer.

U5 amplifies the logged output for comparison with the Power Level Summing (f) signal. R7 and R8 adjust the gain of U5, and calibrate midrange power levels for their respective bands. R9 is selected during power meter leveling to adjust the gain of the log amp for compatibility with the HP 432A Power Meter.

Guarded-gate FETs, Q7 and Q8, select the appropriate detector return for INTernal and EXTernal leveling.

## Power Lovel Reference (C) Power Level Summing (F)

U14 is a 12-bit microprocessor-compatible D/A converter, which latches data in three 4-bit nibbles. The -10V REF input sets the DAC for a maximum output (TP2) of  $\pm 10V$ . The voltage at TP2 is the product of  $\pm 10$  VREF and the fractional binary input of the DAC.

The voltage at TP1 is the sum of several voltages, depending on the operating mode of the Plug-in. U3A sums PWR SWP/COMP and AM inputs. In addition, selected feedback resistor R3 reduces gain to compensate for detector deviation from square-law at the upper limits of the Plug-in power range.

The EXT CAL input is summed through amplifier U3C, R31, in the feedback loop of U3C, provides temperature compensation for the Log Amplifier and detectors.

#### Error, Sample and Hold (G)

TP4 is the summing junction for the Power Level Summing output, Log Amplifier output, and FREQ TRK V. FREQ TRK V is a 0 to 5 volt ramp proportional to the YTM DRIVE Voltage.

Under leveled power conditions, the voltage at TP4 is zero. A non-zero voltage reprenties an error and forces a change in modulator current until power is again level.

U3D buffers the error voltage. Q3 provides sample and hold capability during nulse modulation. R69 reduces the coupling effect of parasitic capacitance in

### Main ALC Amp () Unlevel Signal (J)

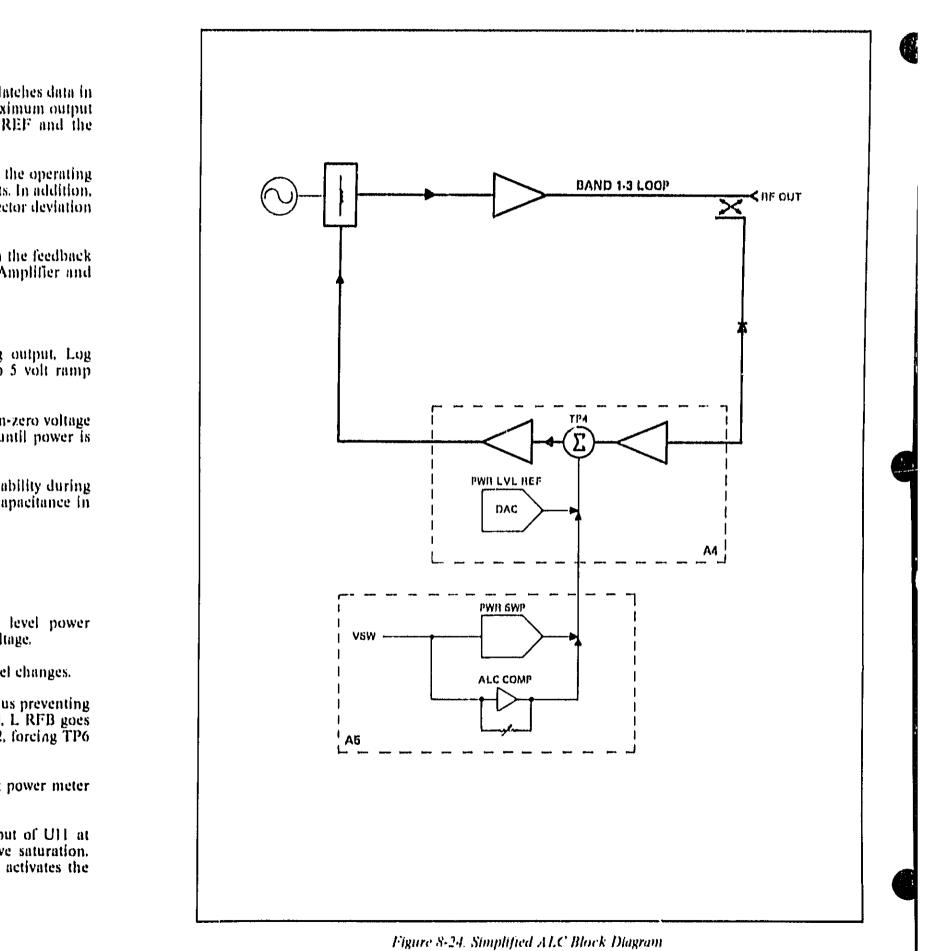
Both inputs to integrator UII are at virtual ground under level power conditions, allowing for immediate response to an input error voltage.

R11 optimizes the speed at which the loop responds to power level changes.

L RFB goes low during bandswitching to blank the RF power, thus preventing the loop from saturating. When 8350A RF BLANK is selected, L RFB goes low during retrace also: U2D closes, pulling current through C22, forcing TP6 high and turning on the PIN modulators.

C21 compensates for the response time of the ALC loop during power meter leveling to prevent oscillations.

Under unleveled conditions, VR4 and VR5 will clamp the output of U11 at approximately -4 and +4 volts, preventing negative or positive saturation. When the output of U11 approaches -2 volts, comparator U15 activates the front panel LED indicating unlevele power.



Collector current in common base transistor Q14 is exponentially related to the base-emitter voltage. P1N modulators are driven exponentially to maintain constant loop gain.

Emitter follower Q13, CR7, and CR9 control the gain of the exponential current drive,

PIN Mod O Driver

PIN Mod 1 Driver (K)

R97 compensates for the loss of modulator sensitivity under high power conditions.

Q10 (K) increases isolation in Band I by shutting off the modulator in the inactive band. Q16 and Q17 also provide square wave modulation and RF blanking, when selected.

#### A4 ALC TROUBLESHOOTING

Since the Automatic Level Control (ALC) function of the 83590A RF Plug-in includes many individual components arranged in a highly interdependent closed loop, the scope of the A4 ALC troubleshooting section extends well beyond the limits of the A4 assembly. Portions of the A5 FM Driver assembly, and several microcircuit components which contribute to the power leveling function, are discussed below.

The ALC "loop" is a complex feedback loop which monitors the RF output power and continuously corrects for any deviation from the desired power level. Because it is a closed system, it is difficult to isolate cause from effect when a problem arises. The key to troubleshooting, then, is to examine individual components, correlating the expected output for a particular input signal.

This troubleshooting outline is organized into two major sections: Troubleshooting Symptoms and Troubleshooting Diagnostics. The section entitled "Symptoms" (1) characterizes possible failure modes, (2) provides some general troubleshooting hints, and (3) refers the reader to more detailed procedures found under "Diagnostics".

#### Troubleshooting Symptoms

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The procedures outlined below help to systematically characterize the failure as quickly as possible. The following failure symptoms are discussed:

RPG / POWER DISPLAY FAILURE UNLEVELED (LED) FLATNESS / OSCILLATIONS (Power Drop-outs) FULL UNLEVELED POWER NO POWER (Single Band) NO POWER (All Bands) POWER SWEEP / FLATNESS

Evaluating the failure mode may require an HP 432A Power Meter or the HP 8755C Swept Amplitude Analyzer with the 11664B Detector. (However, a crystal detector with an "A vs B" oscilloscope may often be substituted.) Figure 8-25 configures a typical test set up. Initiate all tests with the INSTR PRESET condition.

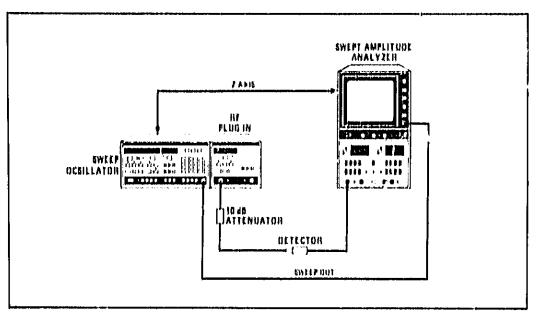


Figure 8-25, Typical ALC Troubleshooting Setup

#### **RPG / POWER DISPLAY FAILURE**

Check that the POWER display changes when either the RPG is rotated or data is entered via the 8350A keyboard. This verifies that the digital information is reaching the mainframe, is properly processed, and is then displayed.

• If the display is flashing rapidly or showing random patterns, refer to A1/A2 Front Panel or A3 Digital Interface troubleshooting. If the RPG causes a change in the measured RF power level, but the POWER display remains the same, refer to A1/A2 troubleshooting. If the RPG produces no response whatsoever, or if the front panel display is blank, refer to A1/A2 troubleshooting, and trace the problem back to the 8350A mainframe.

#### UNLEVELED (LED)

If the UNLEVELED fight turns on during the sweep, enter a sweep time of 20 seconds (i.e. one second per GHz). Observe the SWP light on the 8550A Sweep Oscillator, and determine at which times during the sweep the UNLEVELED light turns on.

• If the UNLEVELED light remains lit during retrace, suspect problems in the front panel annunciator drivers. Refer to A1/A2 troubleshooting.

- It the UNLEVELED light is on during the entire forward sweep, suspect components common to all bands.
- If the UNLEVELED light flashes on briefly twice during the sweep (at 7 and 13.5 seconds into the trace), the problem occurs at the bandswitch points. Check for the RF blanking (L RFB) pulses during bandswitch at A4P1-29, as shown in Fig. 8-30. If the signal is missing, trace the problem back through the 8350A, to the blanking request (L RFBRQ) line on the RF Plug-in A6 assembly. If L RFB is present, but A4TP6 does not clamp at ±4 Vdc during blanking, suspect A4U2D or A4U11.
- If the UNLEVELED light flashes briefly during the sweep, but does not imply any of the above failure modes, check power flatness. See below.

FLATNESS / OSCILLATIONS (Power Drop-outs)

Monitor the RF output with the HP 8735C as shown in Fig. 8-25. Optimize the output power with the front panel PEAK control.

- If the power level is constant across the sweep within approximately 5 dB, then the Plug-in may only require ALC flatness adjustments. Refer to Section V, Adjustments, in this manual, for the Internal Leveled Flatness adjustment procedure.
- If the measured power level lies between +10 and −5 dBm, but can't be controlled via the front panel, refer to the Digital Control section under Troubleshooting Diagnosis.
- If the trace appears chopped or broken the loop may be oscillating. Refer to Section V, Adjustments, in this manual, and perform the ALC Gain adjustment procedure.

FULL UNLEVELED POWER (One or More Bands)

If power is unleveled in Band 1 or Bands 2-3 only, select a sweep width within the unleveled band(s). If power is unleveled in all bands, continue to sweep the Plug-in's full range.

• Attempt to level the power externally using the HP 432A Power Meter as shown in Figure 8-26. Select MTR leveling, and enter a 100 seconds sweep time. If the RF power is now leveled then the failure is most likely in the detectors or the Detector Selection Switch, A4U6. Refer to the following paragraph. If this does not prove to be the case, the problem may be in the two analog switches U4B and U6A. It may be necessary to perform the ALC adjustments in Section V of this manual.

#### Model 83590A

#### Service

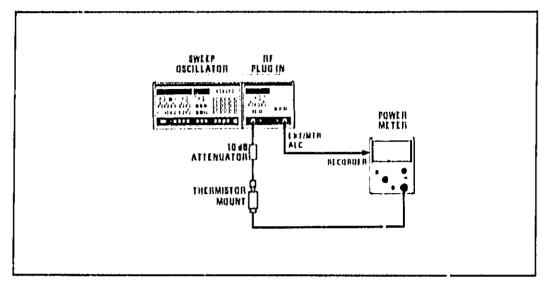


Figure 8-26. Power Meter Leveling Setup (Using HP 432A Power Meter)

- Check the Detector Selection Switch by entering a CW frequency within the band or leveling mode in question and trace the detector voltage through U6B. If the input to be selected doesn't match the output, check the MUX A0 and MUX A1 lines (see Table 8-12). Also check U12 and U13 as described under Digital Control.
- Check the voltage at TP6. If it is at +4 Vdc, suspect the Mod Drivers or Modulators. If it is below -2 Vdc, suspect the Detectors and Detector Leg.

NO POWER (Single Band Only)

If no power is detected in one band, but there is leveled power in another band, suspect the components of the RF path appropriate to the faulty band within the ALC loop.

#### NOTE

Turn off line switch before removing or installing any assembly.

With the ALC assembly removed from the Plug-in, 27.8 kHz squitte wave modulation from the 8350A is not available. Howavar, the 8755 27.8 kHz equare wave can be connected to the rear panel PULSE IN connector to maintain 8755 compatibility.

- To check the RF components, remove the A4 ALC assembly from its socket. This removes all bias from the modulator, and should allow maximum power through the RF path in all bands. If full power (over +12 dBm) is then detected in all bands, the RF amplifier (A14), and YTM (A12) are verified. Suspect primarily the appropriate detector. Also inspect the modulator, as well as the A4 Mod Drivers and Detector Selection Switch.
- If there is no RF signal in any of the bands, check the A6 SRD and PIN Diode Bias circuit.



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#### NOTE

# Turn off line power before removing or installing any assembly.

- If no power is detected in any band, remove the A4 ALC assembly. This removes all bias from the modulator, and should allow full RF power to be transmitted. If there is still no power, check the rear panel AUX OUTPUT for approximately 0 dBm to verify that the A13 YIG Oscillator is providing an RF output. Refer to RF Troubleshooting for details.
- If removing the A4 assembly causes full unleveled RF power to appear, reinstall the board and check A4TP6. If less than -2 Vdc is found, verify that TP9 is approximately -8 Vdc in Bands 1-3. If A4TP6 is at +4 Vdc, suspect any circuitry between the Detector Selection Switch and A4TP6, particularly the Log Amp.

#### **POWER SWEEP / FLATNESS**

 If power increases smoothly with frequency, and POWER SWEEP is NOT selected, suspect problems with the A5 FM Driver assembly.

#### NOTE

Turn off line power before removing or installing any assembly.

Remove the A5 board from the Plug-in. If the situation improves, suspect a failure on the A5 assembly.

 If the RF power is leveled within approximately 5 dB, refer to Section V, Adjustments, in this manual, and perform the Internal Leveled Flatness adjustment procedure.

#### **Troubleshooting Diagnostics**

The troubleshooting information below is organized into functional areas:

DIGITAL CONTROL (A) REFERENCE POWER LEVEL (C) (F) DETECTORS / DETECTOR SELECTION SWITCH (B), DCI, CRI DETECTOR LEG (D) (E) MODULATOR LEG (C) (I) MOD DRIVERS (L) (K) MODULATORS (A17, A13)

DIGITAL CONTROL (A)

Address Decoder U12 and Control Latch U13 control digital switches throughout the A4 assembly. Their operation can be confirmed by performing the Hex Data Rotation Write at address 2C07 Hex. Enter the following key strokes:

SHIFT 0 2 GHz 5 M4	-	7	Enters Hex Data Command Address location 2C07 (U13) Hex Data Rotation Write
*** *			FICE DUM NOMINAL WINC

Service.

Check the outputs of U13 for the waveforms shown in Figure 8-2.

 If any output signal is missing or misplaced, check the data lines against Figure 8-2. If no output is found, look for activity at U13 pin 11. Check for L INST1 and BA3 to pulse low, while BA0, BA1, and BA2 pulse high. If these pulses are missing, trace the problem back to A3 Digital Interface.

If the Digital Control section is working, the primary outputs of U13 are easily controlled by selecting the appropriate front panel function while in the CW sweep mode, (e.g., B1 is held high by selecting a CW frequency in Bands 1 through 3; selecting MTR leveling holds the PM line high, etc.).

REFERENCE POWER LEVEL (C) (F)

The Reference Power Level Leg produces a voltage proportional to the "desired" power level. This signal is a summation of the absolute power reference, AM, ALC compensation, and power sweep signals.

The ALC compensation and power sweep signals are generated on the A5 FM Driver assembly. If an A5 failure is suspected, refer to troubleshooting information on the A5 Service Sheet. Unless A5 is suspect, simplify A4 troubleshooting by turning off the line power and removing the A5 assembly. Although power sweep will be disabled and the power flatness will be lost, the ALC loop should still level without the signals provided by the A5 assembly.

DAC U14 establishes the absolute power level. The -10V REF from the A6 assembly is scaled to yield from 0 Vdc (-5 dBm displayed) to +10 Vdc (+20 dBm displayed) at TP2. (This breaks down to a voltage step of 0.40 Vdc per 1.0 dB of power over the dynamic range, or 6.00 Vdc at +10 dBm.)

A self-test routine is available to exercise the ALC DAC. Enter:

SHIFT 5 0

The waveform in Figure 8-31 should be seen at TP2. Note that the exercise routine for the 12-bit DAC yields a staircased waveform with 13 levels. The first step shows the maximum +10 Vdc output with all bits high. The following levels represent the voltage at TP2 with successive bits loaded high in order from the Most Significant bit to the Least Significant Bit.

• If the waveform at TP2 is not correct, check for -10V REF, and trace any problem back to the A8 assembly. Look for activity on L INST 1, BA0, and BA1. BA2 and BA3 should pulse high as each new DAC value is loaded, pulsing the CS line (U14 pin 8) low. If any of these lines, or a data line, appears dead, trace the problem back to the A3 assembly.

U3A adds PWR SWP/COMP and AM, and provides detector flatness compensation at higher power levels with CR2 and CR3. Use the EXT MTR mode to by-pass these diodes while troubleshooting.

U3C adds the front panel amplitude adjustment (EXT CAL) used with external leveling. The following levels should be seen at TP1 with A5 removed and INT leveling selected:  $\pm 0.3$  Vdc for  $\pm 5$  dBm, and  $\pm 7.0$  Vdc for  $\pm 20$  dBm. An amplitude modulation (AM) signal of 1.0 Vp-p at P1-4 will produce roughly 260 mV p-p at TP1. (Note that U4A, CR2, and CR3 in the feedback path around U3A change the gain depending on the band and desired power level. This may result in a 1.0 Vdc difference between bands at  $\pm 20$  dBm.)

#### DETECTORS / DETECTOR SELECTION SWITCH (B), DCI, CRI

Detector CR1 is tested simply by checking the output voltages under full leveled power or full unleveled power conditions.

#### NOTE

# The 27.8 kHz modulation signal required for 0766 compatibility is not available from the 0350A when the A4 assembly is removed from the Plug-in and must be supplied from the 0766 through the rear panel PULSE IN connector.

• If no power is measured in the suspected band, turn off the line power and remove the A4 assembly. Return power to the instrument. (If there is still no RF power, suspect components of the RF path. Refer to RF Troubleshooting.) If full unleveled RF power is obtained, apply two narrow strips of cellophane tape to the pin-edge connector to isolate the outputs of the modulator drivers from the modulators (P1-19 and P1-44). Reinstall the A4 board. This removes bias from the modulators, allowing full RF power transmission, while providing detector bias.

If full leveled power (+10 dBm) or full unleveled power (at least +12 dBm) is measured, sweep only the band in question and check the voltages at the detector inputs against the values shown in Table 8-11. (Use high-impedance 10:1 probes.)

	Full Lavalad +10 dBm	Full Unleveled +20 dBm
Bands 1-3 (A4P1-20)	-100 to -120 mV	−200 to −600 mV

Table 8-11. Detector Voltages

If the Detectors are working and the Detector Selection Switch is suspected, sweep only in the faulty band and monitor TP15 for the voltages seen at the selected input of U6B.

If the EXT/MTR ALC INPUT circuits are suspected, select the desired mode and supply a test signal (low-level DC or sine wave) in the front panel BNC connector, and trace it through U6B at A4TP15.

#### NOTE

# Remove any tape applied to edge connector pins in the previous procedure.

#### DETECTGR LEG

The "Detector Leg" of the ALC loop includes components between the Detector Selection Switch and the Error Summing Amplifier U3D.

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Before troubleshooting the Detector Leg, he sure the Detectors and Detector Selection Switch are working correctly. See above.

The Detector Leg can be effectively tested by using the Open Loop method of troubleshooting. This procedure utilizes the external leveling mode EXT by supplying an external DC voltage or sine wave to the EXT/MTR ALC INPUT connector. This method breaks the ALC loop and allows waveforms to be checked against known test signals. See Figure 8-32.

#### MODULATOR LEG

The "Modulator Leg" includes the Error Sample & Hold and the Main ALC Amp.

U3D is a non-inverting unity-gain summing amplifier. Under leveled conditions, both TP4 and TP7 should be nearly 0.0 Vdc. Under any conditions (except during "hold"), TP4 and TP7 should be at the same voltage. If not, suspect U3D, Q3, or the Sample & Hold Driver.

U11 forms an inverting integrator. When TP7 is positive, TP6 should be at -4 Vdc. If not, suspect U2D or U11. When TP7 is negative, TP6 should be at +4 Vdc. If this is not the case, suspect U11.

- The following procedure can be used to check U3D and U11:
  - I. Remove jumper W3.
  - 2. Set power for -5 dBm at any CW frequency.
  - 3. Press 83590A EXT ALC.
  - 4. To check U3D, monitor TP4 and TP7 while adjusting the EXT/MTR ALC CAL knob between the extremes of its range. Both TP4 and TP7 should vary between approximately +0.5 and --0.5 Vdc.
  - 5. Verify U11 by adjusting the CAL knob as described above and monitoring TP6. Since U11 is an integrator, TP6 should saturate and clamp (due to VR4 and VR5) at -4 Vde and +4 Vde, respectively. (When sweeping across a bandswitch, RF blanking pulses will saturate TP6 at +4 Vde regardless of input.)
  - 6. Reinstall jumper W3.

-----

Further troubleshooting of the Modulator Leg can be continued by following the Open Loop procedure outlined in Figure 8-32 and checking for the waveforms provided in Figure 8-33.

#### MODULATOR DRIVERS

The voltage-to-current conversion and current gain needed to drive the modulator is provided by Q13 and Q14 on the output of the Main ALC Amplifier. As the voltage increases at TP6 so does the current to the Modulator, shunting more RF energy to ground and allowing less to pass through. Since the modulator is essentially current-controlled, the voltages measured at TP9, P1-19, and P1-44 do not vary much over a wide range of modulator attenuations.

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Q13 is an emitter-follower followed by a common-base stage (Q14), with two diodes in between. Check the biases and base-emitter voltages to check for damaged transistors.

 To establish a bias level for the Mod Driver stage, TP6 can be forced high (+4 Vdc). Remove jumper W3. Press 8350A CW and select a CW frequency in the appropriate band. Select EXT ALC, and enter an RF power level of -5 dBm via front panel controls. Rotate the EXT/MTR ALC CAL knob fully counter-clockwise. Verify a signal level of approximately +4 Vdc at TP6. Reinstall jumper W3.

#### **MODULATORS**

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The internal modulator for this Plug-in is housed in a combination microcircuit package, A16 Modulator/Coupler. Figure 8-27 provides a simplified schematic for these positive-bias shunt-type attenuators. As more current is supplied through the modulator bias pin, the shunt diode turns on harder, sinking more RF power to ground and allowing less to reach the front panel.

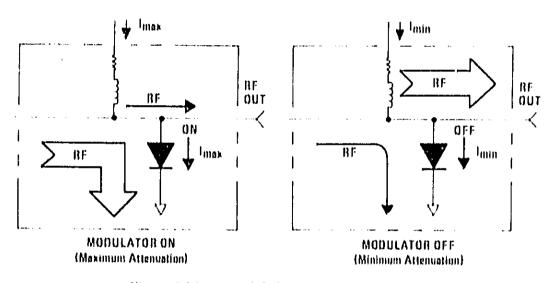


Figure 8-27. Simplified Modulator Schematic

The modulator is checked simply by noting whether the actual RF attenuation is appropriate to the modulation bias present:

#### NOTE

## Turn off line power before removing or installing any assembly.

 If low or no RF power is observed, remove all modulator bias currents simply by removing the A4 assembly from the motherboard. With no bias current, the RF power should pass through the modulator unhindered. If this is not the case, check the modulator diode as follows:

1

 Select 83590A EXT ALC. Remove jumper W3. Enter -5 dBm RF power, and select a CW frequency in the appropriate band. Rotate the EXT/MTR ALC CAL knob fully clockwise. This should result in -4 Vde at TP6, essentially removing bias from the modulator. Check for 0 Vde at TP9. If this is not the case, isolate the modulator from the drive circuitry by applying a piece of cellophane tape to the pin edge connection P1-19. If TP9 still does not measure 0 Vde, the modulator diode may be shorted.

#### NOTE

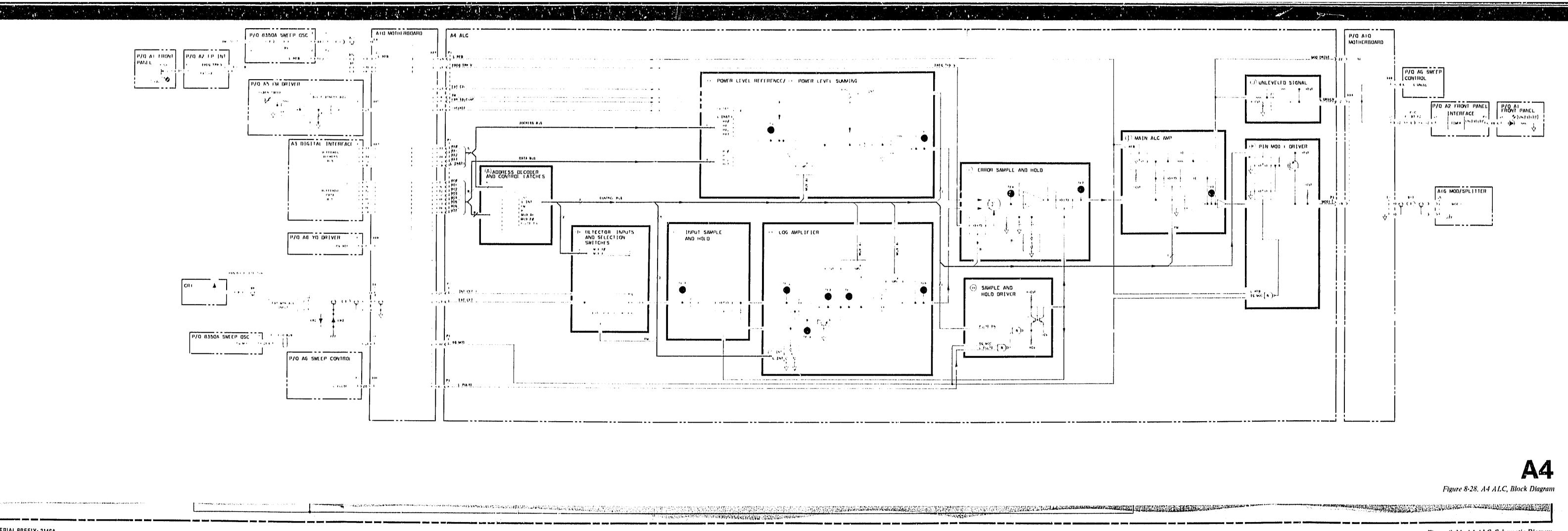
Remove any take applied to the pin edge connectors in the previous procedure.

- If the modulator appears to be functioning properly, check the following RF levels with a Power Meter or Spectrum Analyzer. When checking power levels internal to the RF signal path, ensure that all critical ports are terminated in 50 ohms.
  - If power is low in all bands, check the RF level at the rear panel AUX OUT connector. Refer to the RF Schematic Diagram at the end of Section VIII for the proper levels.
  - 3. Check the RF levels around A14 Power Amplifier with no modulation. A14 should output approximately +26 dBm with about +13 dBm at the input.
- If maximum unleveled RF power is observed, attempt to achieve maximum attenuation (minimum RF transmitted). Select 83590A EXT ALC, Remove jumper W3. Enter -5 dBm RF power, and select a CW frequency in the appropriate band. Rotate the EXT/MTR ALC CAL knob fully counter-clockwise. The voltage level at TP6 should be +4 Vdc. Concurrently, the voltage level at the output of the Mod Driver, P1-19, should be approximately +0.6 Vdc to +0.8 Vdc.
  - 1. If the voltage is significantly higher than this, the modulator diode is probably open.
  - 2. Check TP9 for approximately +2.0 Vdc. The difference between the test point and the corresponding pin-edge connector gives an indication of how much current is flowing to the modulator.

Service

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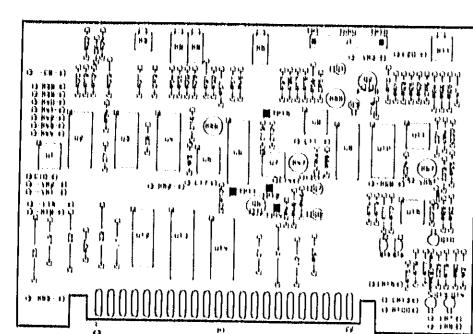
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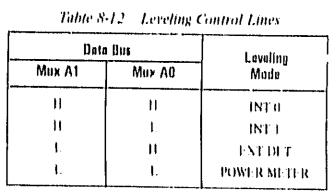
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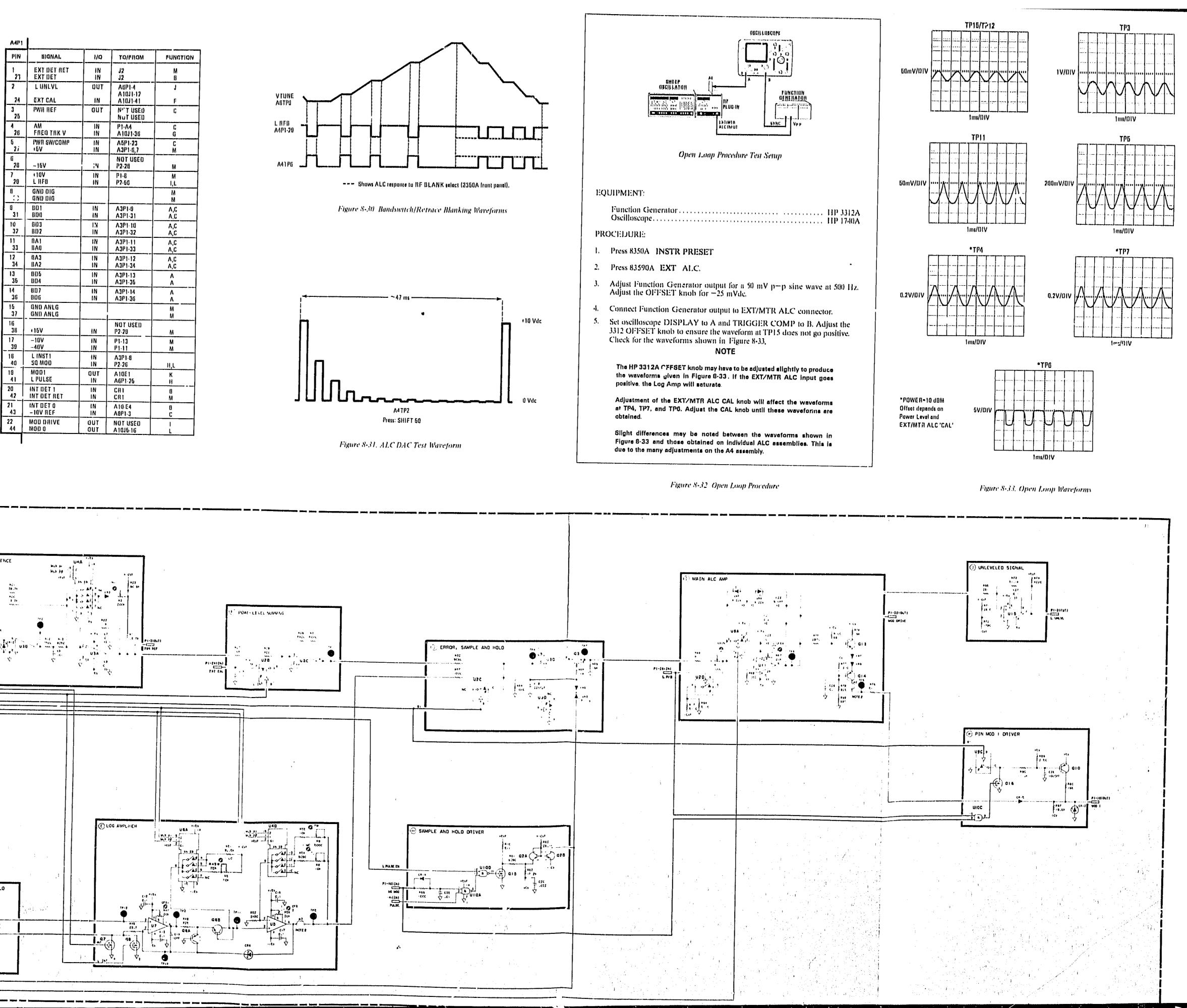
Figure 8-34, A4 ALC, Schematic Diagram 8-47

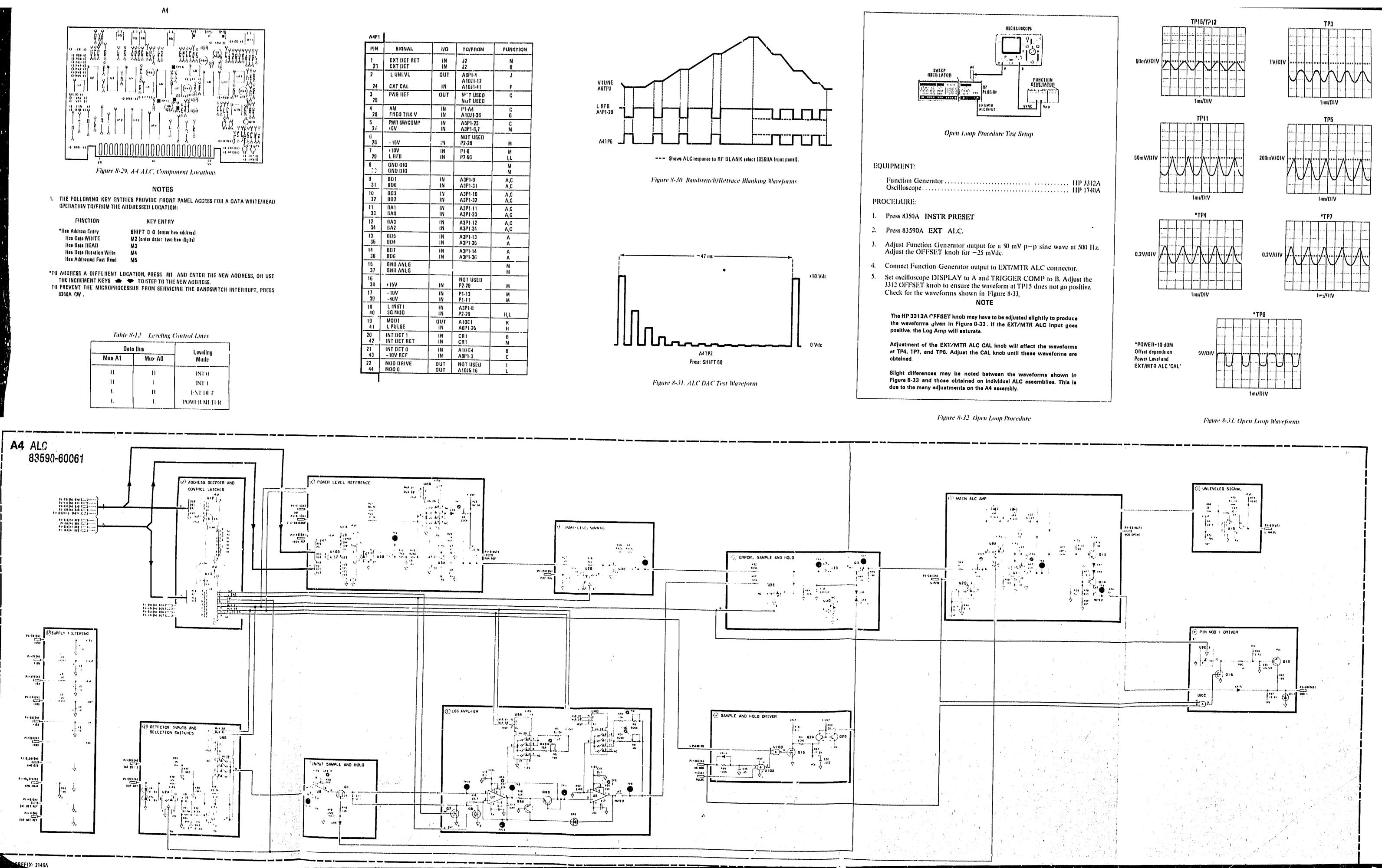


OPERATION TO/FROM THE ADDRESSED LOCATION:

Hax Data WHITE Hax Data READ







#### A5 FM DRIVER, CIRCUIT DESCRIPTION

The A5 FM Driver is divided into three major sections: the YO/YTM Main Coll #M Drivers, the YO FM Coll Driver, and the ALC Flatness Adjustments and hower Sweep circuits for the A4 ALC assembly.

The FM input signal from the rear panel of the 8350A Sweep Oscillator provides the input to both the YO/YTM Main Coil and FM Coil Driver circuits. For low frequency FM inputs, the YO and YTM Band Select Amplifiers scale and buffer the FM signal to produce outputs that are summed with the tuning voltage on their respective driver board assemblies (A7 YTM Driver and A8 YO Driver). Thus, these low frequency FM outputs are an extra tuning voltage input to the YO and YTM drivers, and may be used for phase locking, frequency offsetting, or low frequency FM applications (where up to 75 MHz deviations are required). The FM Coil Driver scales and buffers the FM input signal to produce the current drive for the FM coil in the YIG oscillator for smaller deviation but wideband (up to 10M11z) FM applications. A current drive for the YTM is not necessary because the YTM bandwidth 's wide enough to pass small frequency variations. Relay switches provide the option of selectable sensitivities of -6 or -20 MH2/Volt and/or DC coupling the FM input to the FM Coll Driver circuits. In the DC coupling mode, the main coll driver is shut off and the FM Coll Driver operates over the frequency range of DC to 10 MHz with -20 MH2/Volt sensitionty. The relay switches are controlled by the state of the Configuration Switch on the A3 Digital Interface board.

The ALC Flatness Adjustments circuit is used to flatten output power versus frequency by introducing an error voltage into the ALC reference channel. The Power Sweep circuit is activated by the front panel POWER SWEEP pushbutton and produces a scaled ramp that is summed with the ALC reference. voltage causing the output power to increase level versus sweep (the amount of which is selected on the front panel).

### YO and YTM Main Coll FM Drivers (C)(D)(H)

The YO and YTM Main Coil FM Drivers scale and buffer the 8350A rear panel FM input signal for FM frequencies between DC and 700 Hz to produce two outputs which are summed with the tuning voltage for the YO main coil on the A8 YO Driver board and the YTM on the A7 YTM Driver board, Low Frequency Amplifier/Filter and the YO and YTM Band Select Amplifiers make up the YO and YTM Main Coll FM Driver. The FM input signal is filtered by 700 Hz low-pass filter R2/C1 and buffered by difference amplifier U7A. The gain of U7A is approximately 1.4. The output of U7A drives both the YO and YTM Band Select Amplifier circuits. Relay K2 is used to control the overall gain of inverting amplifiers U7B and U14D for the two sensitivities by changing the value of the input resistance. Relay K2 is either open or closed (shorting acrossparallel resistors R8 and R78) according to the state of control line 6 MH2/V SEL (1 = -6 MHz/Volt, 0 = -20 MHz/Volt sensitivity). The state of control line 6MH2/V SEL is determined by the position of the Configuration Switch on the A3 Digital Interface board. Since the YTM may be tuned to the second or third harmonic of the YO, the LO FM outputs to the YO and YTM drivers must be scaled according to the band of operation. This scaling is accomplished by the YO and YTM Band Select Amplifier circuits. The gain of each amplifier is set by the YO and YTM SEL inputs to the analog switches in their feedback paths Table 8-13 lists the logic levels of these lines for each band. The YO Band Select Amplifier output (TP3) is summed directly with main coil tuning voltage on the A8 YO Driver board, and the YTM Band Select Amplifier output (TP2) is

summed directly with the YTM tuning voltage on the A7 YTM Driver board, The YO and YTM Band Select Amplifiers are shut off with analog switches U3C and UI3A when the DC coupling mode is selected (on The A3 board Configuration Switch) causing control line 1. LO FM OFF (Low = Low Frequency FM OFF) to be true,

## YO FM Coll Driver (E)(F)(1)

The YO FM Coll Driver scales and buffers the 8350A rear panel FM input for frequencies between DC and 10MHz to produce an output current that drives the YO FM coll. The FM Coll Driver is made up of a high-pass filter, buffers Q5A and Q5B, video amplifier U10, operational amplifier U19, and unity gain follower U20. The high-pass filter is made up of capacitors C2 through Co and resistors R11 and R12. The filter has a 3dB cutoff frequency of about 700112. When the FM Driver is configured for the "crossover" mode as determined by the position of the Configuration Switch on the A3 Digital Interface hoard, the FM Coll Driver passes FM input signals above 700Hz and the low pass filter in the Main Coll Driver circuits will pass signals below 700Hz. If the DC coupling mode is selected, the Main Coll Driver is shut off and control line L DC COUPLE is true, activating relay R1. This shorts the high-pass filter network, and the FM Driver is active for frequencies of DC to 10MHz.

Selectable sensitivities of -6MH2/Volt and -20MH2/Volt are available and determined by the state of control line 6MH1/V SEL (1 = -6MH1/V, 0 =  $-20MH_2/V$ ). When 6MH2/V SEL is high, relay K2 is open and the FM input is scaled by a resistive divider made up of R11 and R12. When 6MHHV S11, is low, relay K2 is activated, shorting capacitors C4-C6 and resistor R11. The combination of C2, C3 and R12 still forms a high-pass filter with a cutoff of 700112. Note that in the DC coupled mode the sensitivity is always -20MHz/Volt

The output of the filter network is limited to about ± 3V with a network made up of VR1, VR2, R14, R15, CR3, and CR4. Q5A and Q5B are connected as emitter followers and buffer the output of the filter network to video amplifier U10. Analog switch U11 is always set to switch position zero. Frequency response shaping to compensate for the roll-off versus frequency of the FM coll is produced by the network made up of C11, C12, C14, R21, R22, R23, R75, and L1 connected across pins 9 and 4 of U10. This network is actually in the emitter of the input differential amplifier of U10 producing greater gain with decreasing impedance. Figure 8-35 shows the approximate response versus frequency of the YO FM coil and the compensation network. Adjustments R19 (FM OFFSET), R75 (111), and C14 (LO) adjust the shape of the compensation network response.

The differential output of U10 drives the wideband Output Current Driver, U19 and U20. The voltage difference between the outputs of U10 at pins 6 and 7 is converted to a proportional current which directly drives the YO FM coll. The overall vot age gain of the Output Current Driver is determined by the YO SEL inputs to analog switches UI2B, C, and D and is selected according to the frequency band of operation. Resistive divider R30 through R32 sets the FM coil drive scale factor.

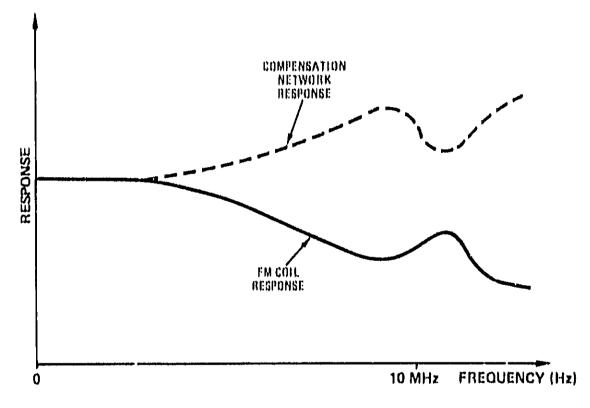
#### Address Decoder (A)

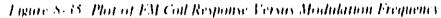
Address Decoder U18 generates three control lines (L EN 4, L EN 5 and L EN 6) by decoding the state of address lines BA0-3 and control line L INST 1. L EN 4 (Low Enable 4) and LEN6 (Low Enable 6) load data into the Control Latches and L EN 5 (Low Enable 5) loads data into the Power Sweep DAC.

#### Control Latches (C)

Control latch U6 stores the state of six control lines that are used to control the amplification factor of the FM input signal according to the frequency band of the RF output. The control lines are loaded into U6 from data bus lines BD0-BD5 when the *I*. EN 6 signal from UI8 makes a low to high transition.

Control Latch U16, stores the state of four control lines that are used to set the signal path and amplification factor of the FM input signal. The state of the control lines is determined by the position of switches 5 and 6 of the Configuration Switch on the AJ Digital Interface board. The control lines are loaded into U16 from Data bus lines BD2-BD5 when the L EN 4 signal from UIR makes a low to high transition.





#### ALC Flatness Adjustments (1)

The purpose of the ALC Flatness Adjustment circuit is to produce an RF OUTPUT signal that is as flat as possible across the entire frequency band. The input of the ALC flatness circuit is a 0 to 5 Volt ramp (in full sweep) labeled FREQ TRK V (Frequency Tracking Voltage). This ramp is dependent on the frequency START and STOP settings, so it will always be at least a portion of the 0 to 5 Volt range.

The FREQ TRK V ramp is applied to four parallel circuits, each one adjusted to take effect at a different frequency (i.e., voltage threshold of FREQ TRK V) as the sweep progresses from START to STOP. Since the four circuits are identical (Q1, Q2, Q3, Q4), only the Q1 circuit will be discussed. Q1A is connected as a diode, is all ays conducting, and is in the circuit for temperature compensation

of QIB. The setting of adjustment RP1 (R34) determines at what point on the input ramp QIB will conduct. When the summing point at the junction of U2C and R33 is at zero volts or greater, Q1B will conduct. The junction of resistors UIB and UIA forms another summing point. UIB applies a positive-going ramp from QIB to this summing point, and a negative-going ramp comes through UIA from the output of ULIC. Slope adjustment SLI adjusts the amount of negative-going ramp contributed to the summing junction through UIA, and thus determines the resultant contribution of the QI circuit to the input of UDIA. That is, the resultant signal may be either a positive-going ramp or a negativegoing ramp as required to make the RF OUTPUT signal flat over that frequency seement.

The composite correction signals from the four flatness adjustment circuits (Q) through 04) are summed at the input of U14A, then are applied to the Power Level Reference in the ALC circuit. TP1 shows this composite correction signal. Overall tilt is adjusted by SLP (Slope) adjustment R48.

#### Power Sweep (P)

When POWER SWEEP mode is selected at the front panel, L EN 4 (Low Enable 4) is generated by U18, enabling U17 on. This allows power sweep data from data lines BDO through BD7 to be loaded into U17. This data selects the gain of - U14B by connecting or removing resistors in series with the input to U14B. The signal nath of the VSW voltage sweep signal (0 to +10V) is through the selected gain resistors in U17 to input pin 6 of U14B. The feedback resistor for UI4B is also within U17 and is internally connected to the input of the amplitier stage. The output of UI4B is summed at the input of UI4A with the ALC flatness signal, then goes through amplifier A14A to the Power Level Reference in the ALC circuit.

When the Plug-in front panel SLOPE key is depressed, data lines BD0 through BD7 redefine the gain of the Power Sweep circuit to compensate the slope of the RF output in d3/GHz.

#### A5 FM DRIVER TROUBLESHOOTING

For troubleshooting purposes, the A5 FM Driver is divided into three groups.

- YO/YTM Main Coll FM Driver and YO FM Coll Driver circuits.
- FM Configuration Control circuits.
- Power Sweep and ALC Flatness Adjustment circuits.

#### YO/YTM Main Coll FM Driver and YO FM Coll Driver Troubleshooting

The most likely indication of a failure in these circuits is unpredictable or no-FM operation. A failure in these circuits can also cause excessive residual FM or frequency offset.

Troubleshooting is divided into two ranges of modulation frequency. For FM frequencies less than or equal to 700 Hz, Table 8-14 provides voltages for troubleshooting. For FM frequencies greater than or equal to 700 Hz, Figure 8-41 provides waveforms for troubleshooting. The voltages and waveforms are arranged horizontally by test point and vertically by the FM input frequency. Figure 8-40 shows the test setup required to obtain the waveforms.

#### NOTE

# Before sitering the switch settings on A381, write down the present configuration. Beturn the switches to their original status after troubleshooting.

Prior to performing the test procedure, preset the A3S1 Configuration Switch sections 5, 6, and 8 to the closed (0) position. Several of the troubleshooting waveforms require different switch settings. A description of each switch setting follows.

- For 6 MHz/V sensitivity set A3S1-5 to the open (1) position.
- For 20 MHz/V sensitivity set A351-5 to the closed (0) position.
- For DC coupled mode -- set A3S1-6 to the open (1) position.
- For cross-over coupled mode set A3S1-6 to the closed (0) position.
- For Front Panel Phaselock mode set A3S1–8 to the closed (0) position.
- For the AUX OUT Phaselock mode set A3S1-8 to the open (1) position.

#### NOTE

#### The 0350A front panel INSTR PRESET pushbutton must be pressed after each switch position change in order for the selection mode to take effect.

- 1. Adjust the Function Generator frequency and amplitude controls to obtain a 1 volt peak-to-peak waveform at TP11 for the frequency tested.
- 2. Verify the waveforms and voltages in the corresponding row.

	Front Panel Physe Lock (A3S1-B=0)			Aux Out Phase Lock (A381-1)		
	01	B2	03	81	82	B3
YO SEL I	0	I	1	()	0	()
YO SEL 2	o	0	1	t	1	
YO SEL 3	0	0	0	0	0	0
YTM SEL 1		1	0	I	0	0
YTM SEL 2	0	0	0	0	l l	0
YTM SEL 3	0	0	0	0	0	

Table 8-13. YO and YTM Gain Select Truth Table

#### FM Configuration Control Circuits Troubleshooting

The FM configuration control circuits include the Address Decoder, Control Latches, relays K1 and K2, and analog switches U3C and U11. Incorrect or no operation in a specific configuration mode is the most likely result of a failure in these circuits. The troubleshooting procedure for these circuits uses several of the 8350A Sweep Oscillator operator initiated self tests. Separate tests for each section of the configuration control circuits are provided in the following paragraphs.

Addross Docodor. Check proper Address Decoder operation by performing a Minor Address Decoder Self Test.

On the 8350A, enter:

SHIFT 5 4 Minor Address Decoder Test

Check the Address Decoder outputs L EN4, L EN5, and L EN6 as shown in Figure 8-36.

**Control Latohos.** Control latches U6 and U16 are checked by performing a hexadecimal data rotation write to U6 and U16, and then checking the outputs for the waveforms shown in Figure 8-2. The Oscilloscope should be triggered from pin 15 of the addressed data latch.

Exercise U16 with Hex Data Rotation Write, Enter:

SHIFT 0 2 GHz 8 M4	-0 0	4	Enters Hex Data command Address location 2C04 (U16) Hex Data Rotation Write

Check the outputs of U16 against waveforms shown in Figure 8-2.

To check control latch U6, press_INSTR_PRESET_then repeat the above key entry sequence using address location 2C06.

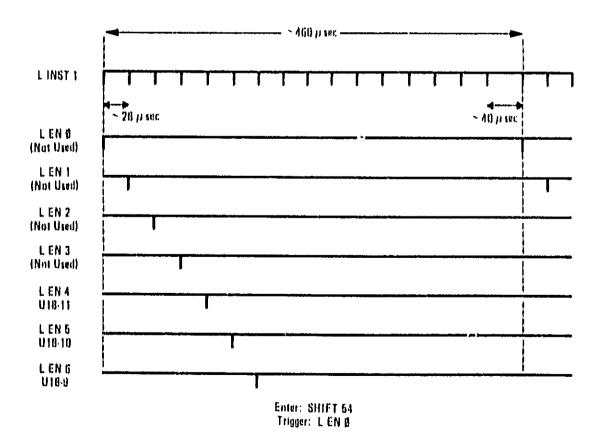


Figure 8-36 Address Decoder Timing Diagrams

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Service

**Bolays K1 and K2.** A known FM input is applied and the waveform at TP4 is monitored. The Hex Data Write feature of the 8350A is used to control relays K1 and E2. Connect equipment as shown in Figure 8-40. Adjust the function generator for a 500 Hz. 1 V peak-to-peak output with a 4-0.5 Vdc offset (use function generator offset control).

To check relay K1, enter on the 8350A:

SHIFT 0	0		Enters Hex Data command
2 GHZ 8	- ()	丙	Address location 2C04 (U16)
M2, 8			Hex Data Write A8

Relay KI should be open. Verify that there is a signal centered around 0 Vdc at TP4.

On the 8350A, enter:

M2 8 B Hex Data Write 88

Relay K1 should now be closed. Verify that the signal at TP4 is offset from being centered around 0 Vdc.

To check relay K2, enter on the 8350A:

M2 BK SP 8 Hex Data Write F8

Relay K2 should be closed. Note the level of the signals at TP3 and TP4.

Open relay K2 by entering on the 8350A:

M2 dBm dB 0 Hex Data Write E8

Relay K2 should now be open. Verify that the level of the signals at TP3 and TP4 is less than previously noted.

**High/Low FM Switching.** Analog switches U3C, U13A, and U11 are checked by using the Hex Data Write feature of the 8350A to control the switches. A known FM input is applied and switch operation is verified.

Connect equipment as shown in Figure 8-40. Adjust the function generator for a 500 Hz 1V peak-to-peak output.

On the 8350A, enter:

SHIFT 0 0	Enters the Hex Data command
2 GHz () 4	Address location 2C04 (U16)
M2 dBm dB 8	Hex Data Write E8

Analog switches U3C and U13A should be closed. Verify there is a signal at TP3 and TP2.

On the 8350A, enter:

M2 dBm dB 0 Hex Data Write 1:0

Service

Analog switches U3C and U13A should be open. Verify that there is no signal at TP3 and TP2.

On the 8350A, enter:

M2 dBm dB 8 Hex Data Write E8

Analog switch U11 should be set to the zero position. Verify that a signal is present at TP6.

On the 8350A, enter:

M2 dBm dB GH2 Hex Data Write EC

Analog switch U11 should be set to the one position. Verify that no signal is present at TP6.

#### Power Sweep/ALC Adjustments Troubleshooting

The most likely indication of a failure in these circuits is either incorrect or no operation of the Power Sweep function or inability to adjust the output power flatness. The Power Sweep DAC U17 is exercised by initiating the Power Sweep DAC self test, and the DAC output is checked at TP8. On the 8350A, enter:

SHIFT 5 1 Initiate Power Sweep DAC self test

Verify the waveform at TP8 corresponds with the waveform in Figure 8-37.

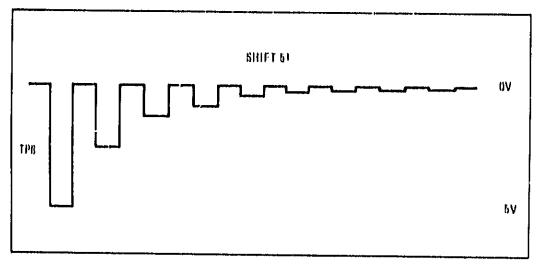
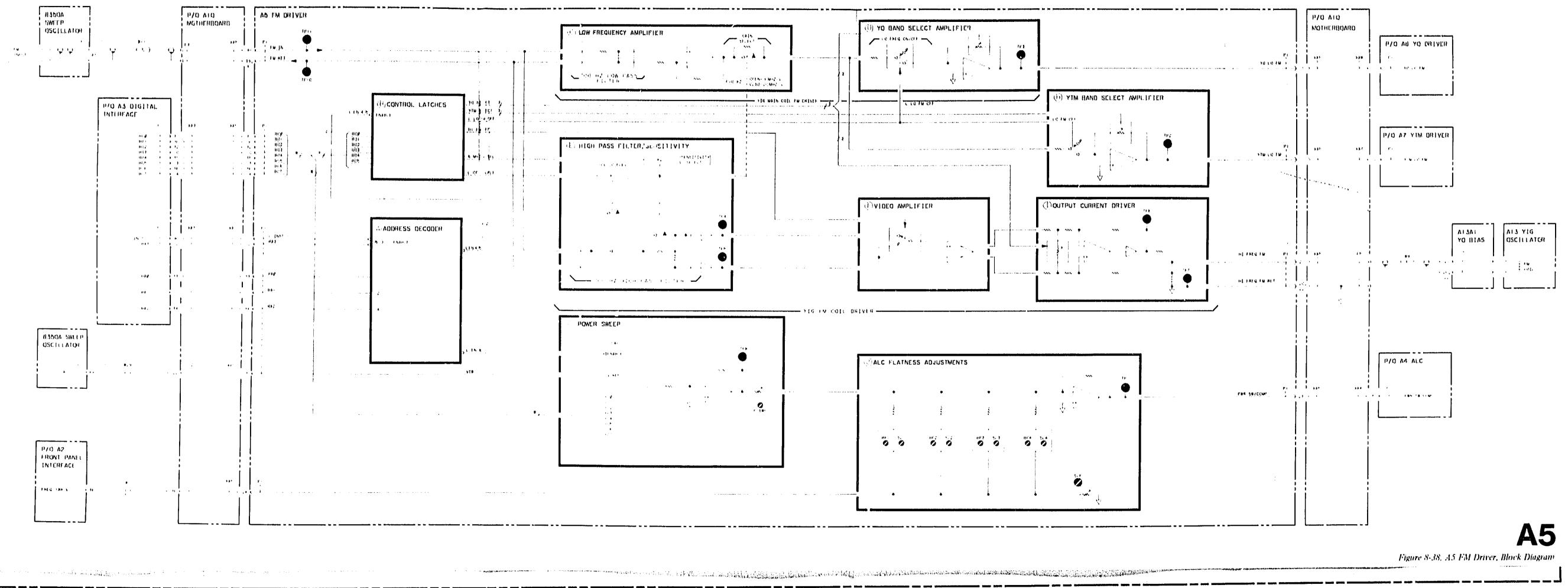


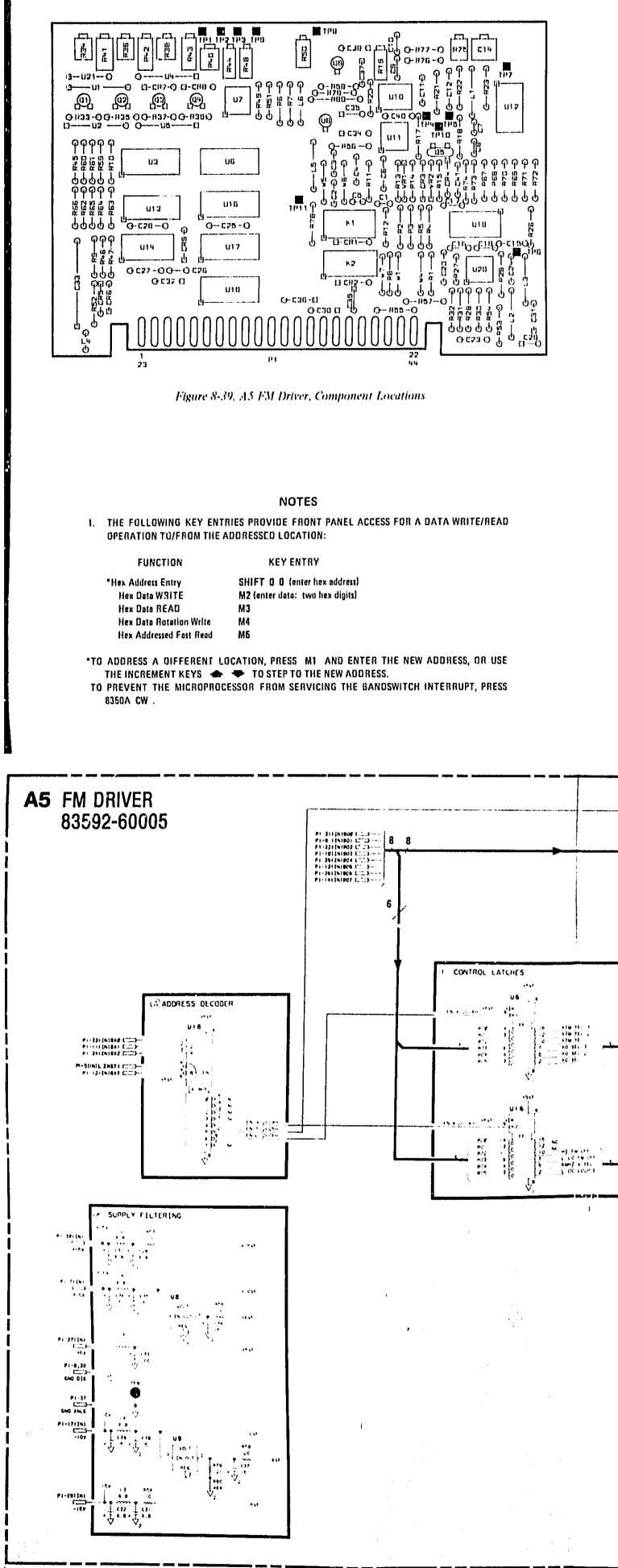
Figure 8-32 Power Sweep DAC Self Test Waveform

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SERIAL PREFIX: 2146A

Figure 8-42. A5 FM Driver, Schematic Diagram 8-53

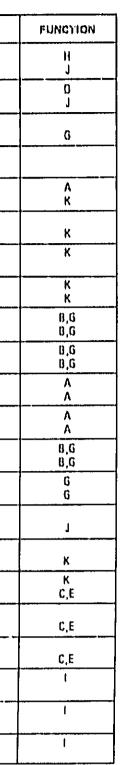


AG

ABP1 PIN TO/FROM 1/0 SIGNAL OUT OUT A7P1-1 YTM LO FM A4P1-5 PWR SW/COMP 23 YO LO FM FREG TRK V OUT IN A6P1-1 2 24 A2J1-36 NOT USED 3 26 IN P2-64 V6W NOT USED 26 NOT USED 5 L INST 1 27 +5V A3P1-0 IN IN A3P1-6,7 NOT USED 6 20 -- 15V P2-28 IN 7 +10V IN P1-B 29 NOT USED B GND DIG 30 GND DIG A3P1-9 A3P1-31 8 BD1 31 BD0 IN IN IN A3P1-10 IN A3P1-32 10 BD3 32 BD2 11 BA1 33 BA0 IN IN A3P1-11 A3P1-33 12 BA3 34 BA2 IN IN A3P1-12 A3P1-34 13 BD5 36 BD4 IN IN A3P1-13 A3P1-35 IN IN 14 BD7 36 BD6 A3P1-14 A3P1-36 15 GND ANLG 37 GND ANLG NOT USED 16 30 IN NOT U IN P2-29 NOT USED +20V +15V IN P1-13 IN P1-A3 -10V 30 FM RET NOT USED 18 40 IN P1-A3 FMIN NOT USED 19 IN PT-A3 41 FM RET 20 HI FRED FM RET OUT AI3AIJI 42 NOT USED 21 OUT A13A1J1 HI FRED FM 43 NOT USED A13A1J1 OUT HI FREQ FM RET NOT USED

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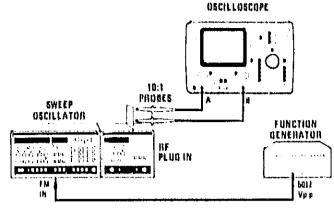
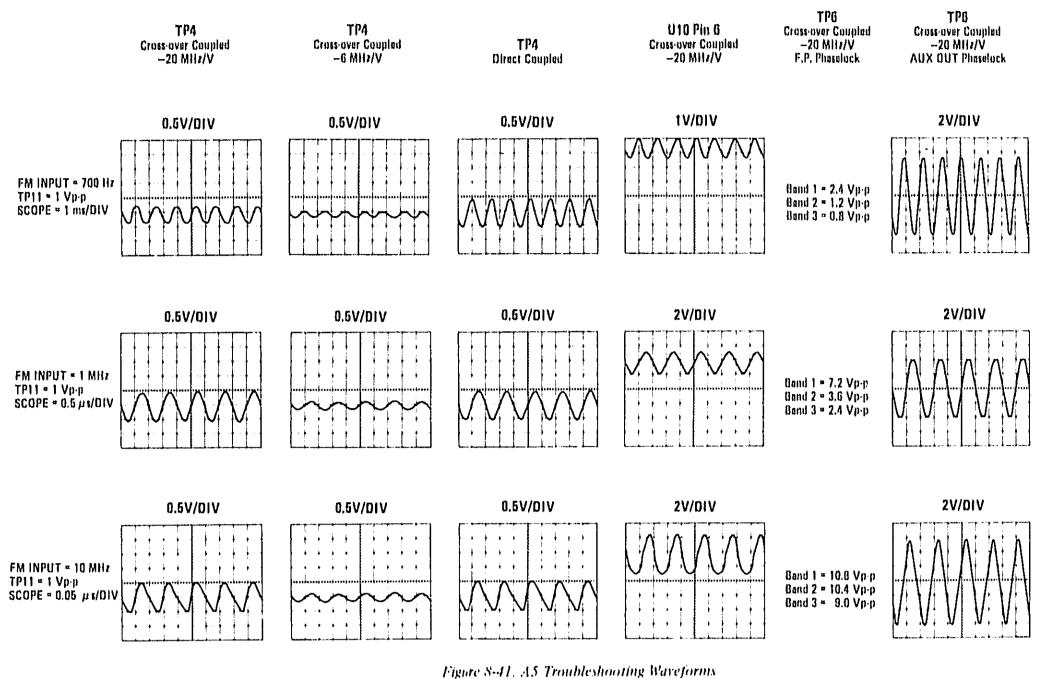
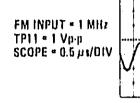


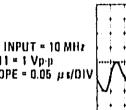
Figure 8-40, A5 Troubleshooting Test Secup

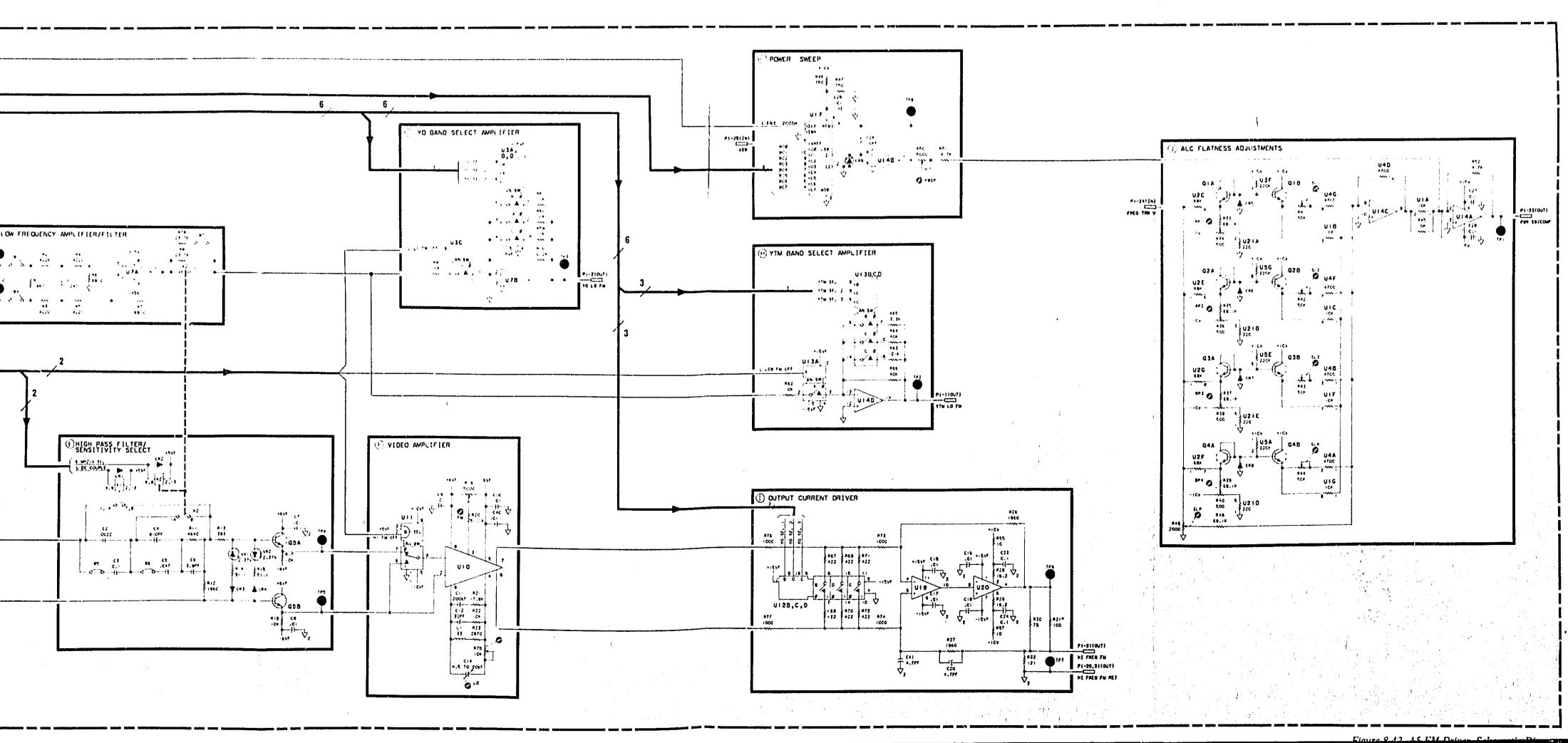


Setup Condition	U7·7	TP2		TP3	
		20 MHz/V	6 MHz/V	20 MHz/V	6 MHz/V
FM INPUT = 100 Hz A6TP11 = 1Vp·p F.P. Phaselock (A3S1-8 Closed)	.8Vp-p All Bands	.8Vp-p All Bands	.48Vp-p All Bands	Band 1 = .8Vp-p Band 2 = .4Vp-p Band 3 = .28Vp-p	Band 2 = .24Vp-p
FM INPUT = 100 Hz A5TP11 = 1Vp-p AUX OUT Phaselock (A3S1-8 Open)	.8Vp-p All Bands	Band 1 = .8Vp-p Band 2 = 3.2Vp-p Band 3 = 4.8Vp-p	Band 1 ≈ .4BVp-p Band 2 ≈ .96Vp-p Band 3 ≈ 1.44Vp-p	.8Vp-p All Bands	.48Vp-p All Bands
FM INPUT = 700 Hz A5TP11 = 1Vp·p F.P. Phoselock (A3S1-8 Closed)	.64Vp-p All Bands	.64Vp-p All Bands	.2Vp p All Bands	Band 1 = .64Vp·p Band 2 = .32Vp·p Band 3 = .22Vp·p	
FM INPUT = 700 Hz A5TP11 = 1Vp·p AUX OUT Phaselock (A3S1-8 Opzn)	.64Vp·p All Bands	Band 1 = .64Vp-p Band 2 = 1.28Vp-p Band 3 = 1.9Vp-p	Band I = .2Vp⋅p Band 2 = .4Vp⋅p Band 3 = .6Vp⋅p	.68 Vp-p All Bands	.2Vp·p All Bands

Band 3 = 1.9Vp-p Band 3 = .6Vp-p







#### A6 SWEEP CONTROL, CIRCUIT DESCRIPTION

#### General

The Sweep Control assembly buffers and scales the VTUNE (Tuning Voltage) from the 8350A mainframe for use by the A7 YTM and A8 YO Driver assemblies. The A6 assembly also controls each bandswitch sequence. The SRD and PIN Diode Bias circuit provides optimum biasing of the YTM Step Recovery diode for the frequency band selected and also biases the YTM PIN diode switch to select the YTM RF input for Bands I through 3. The Pulse Modulation circuit provides a drive current (PULSE MOD) to pulse modulate the RF output power. This modulation is initiated by the rear panel Pulse In input or the amplitude marker from the 8350A mainframe.

#### Address Decoder (A)

The A6 Sweep Control uses hexadecimal address locations 2C00 through 2C0B. L INSTI, BA0, BA1, and the L DAC EN output of U8D are decoded by the Bandswitch DAC as hexadecimal addresses 2C08 through 2C0B. U17 is a 3-to-8 decoder that is enabled when L INST1 and address line BA3 are both low, U17 decodes address lines BA0 through BA2.

#### Date Latches and Output Date Buffer (D)

Two octal latches (U3 and U9) store various signals including the digital data for controlling the Bandswitch Comparator and Sweep Control/Interrupt Logic circuits.Each latch is clocked by a separate line from the Address Decoder to store the byte of data appearing on the Data Bus. The data is latched into U3 and U9 when their respective L EN clock inputs pulse low. Refer to the various circuit function blocks for detailed descriptions of these control lines.

Output buffer U13 outputs data to the 8350A microprocessor that relates to the current status of the sweep. Data is output when the L EN2 clock input to U13 is pulsed low.

#### Tuning Voltage Buffer Amplifier (B)

U6 receives the tuning voltage from the 8350A mainframe and buffers it for use on the rest of the board. The circuit is arranged as a differential amplifier, with the tuning signal appearing at the inverting input and the cable shield at the noninverting terminal. This provides good common mode rejection to eliminate noise picked up on the cable. The waveform at TP5 is an inverted ramp, ranging from 0 to -10V for single band sweeps (Band 1, 2, or 3), or for sweeping the ful frequency range of the Plug-in. However, if the Configuration Switch (A3SI) in the A3 Digital Interface is selected for Sequential Sweep mode only, the tuning voltage (VTUNE) is not rescaled to a 0 to +10V ramp for single band sweeps. Figure 8-47 shows the tuning voltage waveform for a 2.0 to 20.0 GHz sween.

#### Bandswitch DAC (C)

Bandswitch DAC U18 provides an offset voltage at TP1 that is proportional to the next bandswitch point. This voltage is used as a reference voltage by the Bandswitch Comparator for initiating the next bandswitch sequence. This voltage is also summed with the output of the TV Buffer in the Variable Gain Amplifier.

N N

U18 is a 12-bit multiplying DAC which scales a stable -10V REF voltage according to the binary pattern loaded at its inputs. Inverting amplifier UI9 works with the DAC's internal feedback resistor to provide a programmable off et voltage between 0 and +10V at TP1. See Figure 8-47. CR2 protects the DAC from turn-on transients. C20 and the DAC's internal feedback resistor determine the bandwidth of the circuit.

For single band sweeps, the DAC is held in a reset condition by a logic low on the SEQ BAND input. This causes the voltage at TP 2 to be held at 0 volts.

#### Variable Gain Amplifier (E)

The purpose of the Variable Gair Amplifier is to reseale the tuning voltage input into a series of 0 to -10V ramps, with each ramp corresponding to a frequency band (Band 1, 2, or 3). The Bandswitch DAC output is summed in as an offset voltage to set the amplifier output to 0V at the beginning of each band. Amplifier gain is changed by analog switch U4 selecting a different feedback resistor for each band. Potentiometers B0 through B3 set the amplifier gain for each band. Analog switch U10D shorts across the feedback resistors for single band sweeps to disable the amplifier.

Figure 8-47 shows the relationship between the TV Buffer output, Bandswitch DAC output, and the resultant Variable Gain Amplifier output for a 2.0 to 20 GHz sween.

#### Single Band Switching (G)

The Single Band Switching circuit selects between the Variable Gain Amplifier output and the TV Buffer output to provide BVTUNE (Buffered Tune Voltage) to the YO and YTM Driver assemblies. The SEQ BAND (Sequential Band) input to analog switch UI0B determines which input is used for BVTUNE. When the 83590A is sweeping a single band only, SEO BAND is a logic low, and the TV Buffer output is selected. When the 83590A is in a multiband sweep or the configuration switch on A3 is set for Sequential Sweep mode only, SEQ BAND is a logic high, and the output of the Variable Gain Amplifier is selected. U20 is a noninverting voltage follower.

#### Bandswitch Comparator (F)

The Bandswitch Comparator circuit generates a FWD SWP BSW output to initiate each bandswitch during forward sweeps, and RTC BSW to generate each bandswitch during a sweep retrace.

A bandswitch point during a forward sweep is initiated by comparator U23. The buffered tuning voltage (TP5) appears at the inverting input of comparator U23. When the tuning voltage reaches a bandswitch point tas determined by the reference voltage applied to the inverting input of U23), the output of U23 changes. R42 provides hysteresis feedback to U23. If the selected frequency sweep does not require changing bands, switch UHD is opened, and R36 pulls the input to the comparator to +10V disabling the bandswitch circuitry. The reference voltage for comparator U23 (TP2) is supplied by the Bandswitch DAC through operational amplitier U24A. This reference voltage is set during retrace or a bandswitch point to correspond to the next bandswitch point. The SP adjustment provides an offset to set accurate bandswitch points. During a sweep retrace, L RTS goes low to turn off Q7. This places a positive offset voltage at the inverting input of U24A and effectively disables comparator U23 during sweep

retrace by offsetting the reference voltage beyond any bandswitch points generated by Retrace Comparator U14. FET Q1 is turned on when Band 3 is selected; this grounds the comparator output to disable a bandswitch at the end of a sweep.

Retrace Comparator UI4 initiates a bandswitch during a sweep retrace each time the Variable Gain Amplifier output (TP7) equals 0V. During sweep retrace, the L RTS input (inverted by U22A) turns on FET Q3, to set a flV reference at the noninverting input of comparator UI4. The inverting input comes from the Variable Gain Amplifier. Each time the amplifier output reaches 0V, comparator U14 outputs a logic high to initiate a bandswitch. During a forward sweep, FET Q3 is turned off, and a positive offset voltage is applied through R56 and R57. This offsets the reference input beyond any bandswitch points generated by the Forward Sweep Bandswitch Comparator (U23). When Band 1 is selected, QI is turned on to disable comparator UI4 from initiating a bandswitch at the end of a sweep retrace.

Sweep Control/Interrupt Logic (H)

#### NOTE

#### Most of the signals discussed in this section are illustrated in Figuro B-48,

The Sweep Control/Interrupt Logic circuit provides the stop sweep (L SSRQ), Blanking Request (L BPRQ) and Sweep Interrupt (L SIRO) signals at bandswitch points. End of Sweep Interrupt circuitry (U8B) provides requests for interrupts at the beginning or end of sweep.

Whenever the Bandswitch Comparator outputs an active FWD SWP BSW or RTC BSW the output of U2C goes high. Pin 13 of U2D is prevented from tracking pin 12 by C16. Consequently, the output of the XOR, U2D, will go high everytime U2C changes states. Each pulse from U2D clocks flip-flop U8A.

The high output at U8A performs three functions: 1)U16B issues a L SSRQ (Low=Stop Sweep Request) to halt the sweep ramp generator in the 8350A mainframe; 2) UI6A issues a L BPRQ (Low=Blanking Pulse Request) for display blanking during bandswitching; and 3) U16C issues a L SIRQ (Low=Sweep Interrupt Request) to alert the 8350A microprocessor that a bandswitch needs to be made.

The microprocessor now takes over control of the bandswitch by writing command bits to Data Latch U3. First, the SSHOLD (Stop Sweep Hold) line goes high, maintaining the stop sweep (L SSRQ) and blanking (L BPRQ) requests. Simultaneously, the L SSRES (Low=Stop Sweep Reset) line goes low, resetting U8A and clearing the interrupt request (L SIRO). The microprocessor now reads buffer U13 to determine what caused the sweep interrupt request (Forward Sweep Bandswitch, Retrace Bandswitch, Start or End of Retrace, or the Unleveled indicator turned on). Based on this information, the microprocessor blanks the RF power (when L RFBRO goes low), updates the DACs, changes the Variable Gain Amplifier gain, changes various banddependent control lines, and readies the Plug-in for sweeping the new band. After the YO has settled, the RF power is turned back on. After the RF power has come up, the sweep is resumed and the display is unblanked by releasing the SSHOLD line. The time intervals required for YO settling and RF power-up are provided by the programmable counter on the A3 Digital Interface assembly.

In addition to bandswitch points, the microprocessor is also interrupted at the beginning and end of each sweep. Each time L RTS (Low=Retrace Strobe) changes from high to low, or low to high, U2A pulses high, (Pin 2 of U2A is prevented from tracking pin 1 by C17, Consequently, the output of XOR U2A will pulse high everytime L RTS changes states). Each pulse from U2A clocks flip-flop U8B. The noninverting output of U8B is ORed together with the bandswitch interrupt to pull L SIRQ low and request microprocessor attention. L RTS is read through U13 to determine whether the forward sweep is beginning (L RTS=high) or ending (L RTS=low). U8B is then reset by L ESRES, and the microprocessor services the interrupt.

L RFBRQ goes low during bandswitch and sends an RF Blank Request to the 8350A to produce the blanking signal L RFB, for the A4 ALC assembly.

#### SRD AND PIN DIODE BIAS

The SRD and PIN Diode Bias circuit provides two bias voltages for the Switched YIG Tuned Multiplier (YTM). For Bands 1 through 3, analog switch UIIC is closed, and a negative bias is applied to the diode, enabling Bands 1 through 3.

The Step Recovery Diode in the YTM is biased by SRD BIAS. This bias is optimized for each band and changes in power level. Voltage follower/Subtractor U24 provides a voltage for optimum biasing of the SRD for each frequency band. BVTUNE is applied to both its inverting and noninverting inputs. If only BVTUNE was applied (and both inputs have the same gain) the U24 output would always be zero volts. Analog switches UIIA and UIIB sum in offset voltages for Band 1 resulting in a large negative bias to ensure maximum feedthrough of the fundamental oscillator frequency. Analog switches UID, UIB and UIC provide an offset and affect the noninverting input gain. As a result, the U24 output for Bands 2 through 3 is offset from 0V (as determined by the two band "L" adjustments) with the slope determined by the two band "H" adjustments.

U26 is a variable gain differential amplifier tht provides an output current for Bands 2 and 3 for controlling the SRD BIAS. The amplifier gain is determined by the U24 output applied through analog switch U1A to U26 pin 5. Analog switch UIA is open for Band 1, so the SRD BIAS for these bands is determined only by the output of U24 (applied through R63 to the base of Q8). Threshold adjustment A6R78 (T) determines at what modulator drive voltage (MOD 1) that nower level compensation is provided. CR12 prevents U26 from affecting SRD BIAS when MOD 1 is more positive than the threshold voltage set by R78(T).

#### Pulse Modulation (J)

The Pulse Modulation circuit provides a PULSE MOD output to the A16 Modulator/Coupler that is used to pulse modulate the RF output. The L PULSE output is used on the A4 ALC assembly in a sample and hold circuit to maintain a leveled power condition (refer to the A4 Circuit Description for more details). The L PULSE output goes active low when either the L RFM (Low= RF Marker from the 8350A) or PULSE IN (from the rear panel Pulse In connector) go low. If the PULSE IN input from the rear panel exceeds a TTL level, it is translated to a TTL level by the resistor diode network on the U21A pin 13 input. When the L PULSE output is active low (switching RF power of), Q4 is biased on and Q6 is biased off: this provides a positive bias to t^b PIN diode in the modulator and attenuates the RF output power. When L PULSE is a logic high, Q6 is biased on and Q4 is biased off; this provides a negative bias to the PIN diode in the modulator so that it has no effect on the RF power level.

#### A6 SWEEP CONTROL TROUBLESHOOTING

The A6 Sweep Control assembly reseales the tuning voltage (VTUNE) from the 8350A for use by the A7 YTM Driver and A8 YO Driver. The A6 assembly also initates all bandswitch sequences.

#### NOTE

Unloss specifically stated otherwise, the troubleshooting waveforms and voltages described below occur when the Plug-in is sweeping neross its full range (INSTR PRESET conditions).

#### **Buffered Tuning Voltage**

#### NOTE

The BVTUNE output is normally scaled by the Variable Gain Amplifier only for multiband (sequential) sweeps (with the TV Buffer output used for single band sweeps). However, the A3S1 Configuration Switch (position 1) may be set to disable the selection of the TV Buffer output for single band sweeps. This procedure assumes that A3S1 switch position 1 is set to the open positon, thus enabling the A6 assembly to change sceling of the BVTUNE signal for single band and multiband sweeps.

A failure with the BVTUNE signal may cause both the YO and YTM to sweep between improper frequency endpoints, or not sweep at all. For a full band SWEEP (2.0 to 20 GHz), the BVTUNE output at TP8 should be a series of 0 to -10V ramps (See Figure 8-47). For a single band sweep (e.g. 2.0 to 7.0 GHz). BVTUNE should be a single 0 to -10V ramp.

- 1. If both waveforms are incorrect, verify the TV Buffer output at TP5.
- 2. If BVTUNE is incorrect for only the full band sweep, the problem is most likely with the Bandswitch DAC, Variable Gain Amplifier, or the Bandswitch circuitry. (The TV Buffer is verified in single band sweep.)
- a. Check the Bandswitch DAC output at TP1 as shown in Figure 8-47. If this signal is incorrect, run the Bandswitch DAC test by entering SHIFT 5 6. Then check TP1 for the waveform shown in Figure 8-46
- b. Verify correct operation of the Variable Gain Amplifier by checking waveforms at TP4 and TP7 according to Figure 8-47. If any of the voltage levels are slightly out of tolerance, perform the Sweep Control and Band Overlap adjustments in Section V. If the voltage at TP4 is 0V, verify that analog switch U10D is open.

- c. Verify operation of the bandswitch circuitry under the **interrupt Control** section.
- 3. If BVTUNE is incorrect only for single band sweeps, verify that the SEQ BAND input to analog switch U10B,C is a logic low when sweeping only a single band. Also verify that Configuration Switch A3S1 switch number 1 is in the open position.

#### Interrupt Control

Symptoms of an interrupt failure may include loss of sweep, portions of the sweep trace missing, or failure to sweep across a bandswitch.

- 1. Verify operation of the Bandswitch Comparator by checking the FWD SWP BSW (U23 pin 7) and RTC BSW (U14 pin 7) waveforms as shown in Figure 8-48.
  - a. If the FWD SWP BSW signal is not correct, check the Bandswitch DAC output at TP1 and the TV Buffer output at TP5 as shown in Figure 8-47.
  - b. If the RTC BSW signal is incorrect, check the Variable Gain Amplifier output at TP7. Also verify that the noninverting input to U14 is about 0V during a sweep retrace.
- 2. With an Oscilloscope, check the following edge-connector pins: P1-3 (L SIRQ), P1-1 (L RTS), and P1-23 (L SSRQ). The appropriate waveforms are shown in Figure 8-48.
  - a. L RTS should go low at the end of each forward sweep. If it does not, race the problem back through the Plug-in interconnect to the 8350Å.
  - b. L SIRQ should pulse low briefly for end-of-sweep interrupts. If these pulses are missing, but L RTS is present, suspect U2A, U8B, U16C, or control lines from U3.
  - c. L SIRQ should also pulse low for bandswitch interrupts. If these pulses are missing, but FWD SWP BSW and RTC BSW show the proper waveforms, suspect U2C/D, U8A, U16C, or control lines from U3.
  - d. If L SIRQ stays low, or the pulses are exceptionally wide, check U3 with the procedure outlined under **Digital Control** section. If U3 is functioning, the 8350A microprocessor probably did not receive the interrupt. Trace this signal back to the 8350A.

#### Digital Control

The Address Decoder and the Data Latches and Output Data Buffer comprise the digital control for the A6 assembly. A failure in these components usually results in large frequency errors, and will often disable the bandswitch circuitry.

To check the address decoding circuitry enter SHIFT 5 4 and perform the following:

1. Examine L INST1 (P1-18) for activity. If none is found, troubleshoot the A3 assembly.

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- 2. If L INSTI is functional, check each of the L RNn lines (U17) for the pulses shown in Figure 8:45. If these are incorrect, but the address lines show activity, replace 1117. If the address lines seem locked high or low, would shout the address buffer on the A3 assembly.
- 3 To shock output buffer U13, press INSTR PRESET . Set the 8350A for a 5-second sweep rate and make the following key entry:

84HFT 0	1)		Enters thy Hex Data command
2 (117.8	ρ	2	Address location 2002 (1113)
M3			Hex Deta Read

The box digits displayed in the 8350A front panel FREQUENCY/TIME "finlow should change as the status read by U13 changes between forward sweep and retrace. Raising the power level until the UNLEVELED light comes on should also change the status bit being read by U13.

d. Insurvise 1/3 and 1/9 with Hex Data Rotation Write. Enter:

- 5741FT - 0	()		Enters Hex Data command
2 4112.6	0	()	Address location 2C00 (1/3)
Mil			Hex Data Rotation Write

Check the outputs of U3 against the waveforms shown in Figure 8-2. Verify operation of U9 by substituting hex address 2C01 (U9) in the procedure above.

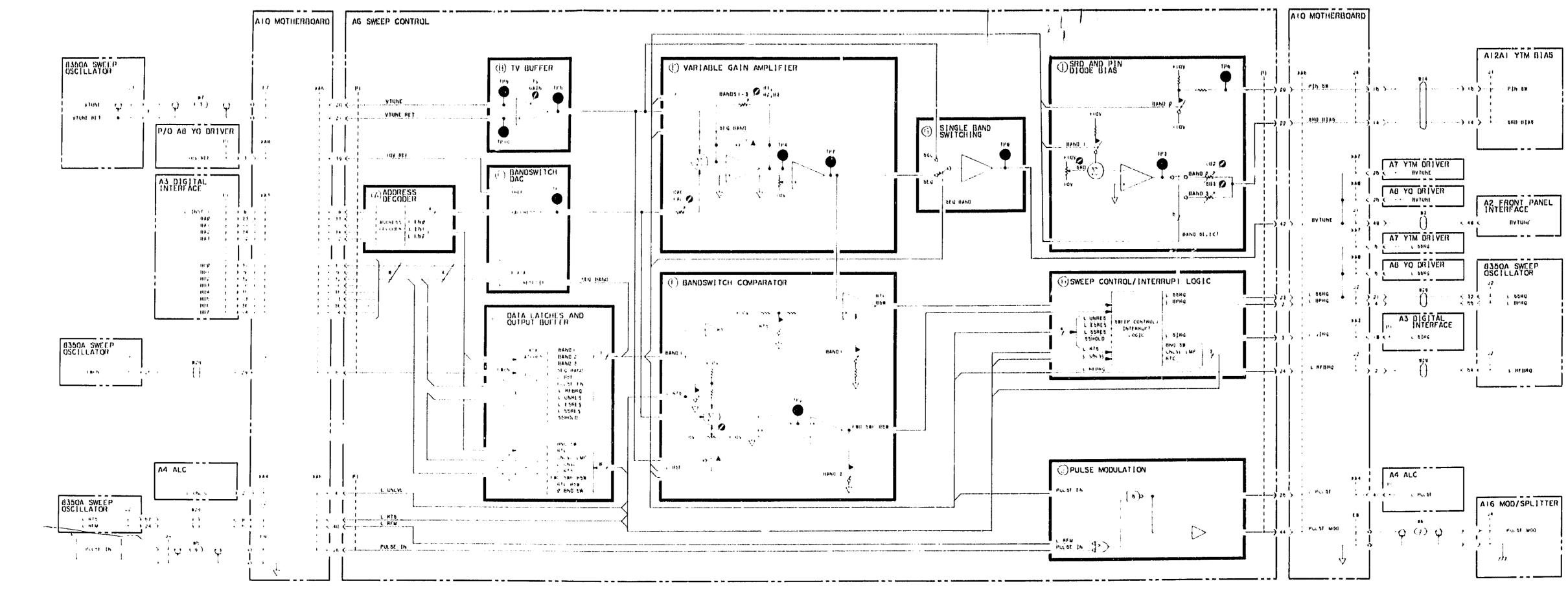
#### BRD and PIN Dloda Blas

A failure in the PIN Diode Bias circuit is indicated by a decrease or complete loss of RF output power for Bands 1-3. Check that the voltage at TP6 is -4.8V for Bands 1-3.

A failure in the SRD Bias circuit is usually indicated by low RF output power in Bands 1-3. Check that the voltage at TP3 is -5V for Band 1. If these voltages are correct, perform the SRD Bias adjustment in Section V.

#### Pulso Modulation

The Pulse Modulation circuit can be checked by entering an amplitude marker on the 8350A and checking for activity on the 1. PULSE and PULSE MOD outputs. If I. PULSE has activity, but PULSE MOD does not, disconnect. We at A1044 to eliminate the possibility of the modulator loading down the signal.



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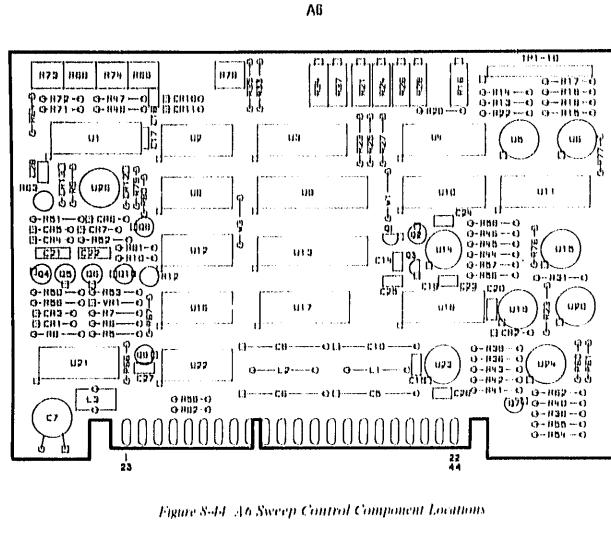
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Figure 8-43 A6 Sweep Control, Block Dlagram

Figure 8-49 A6 Sweep Control, Schematic Diagram

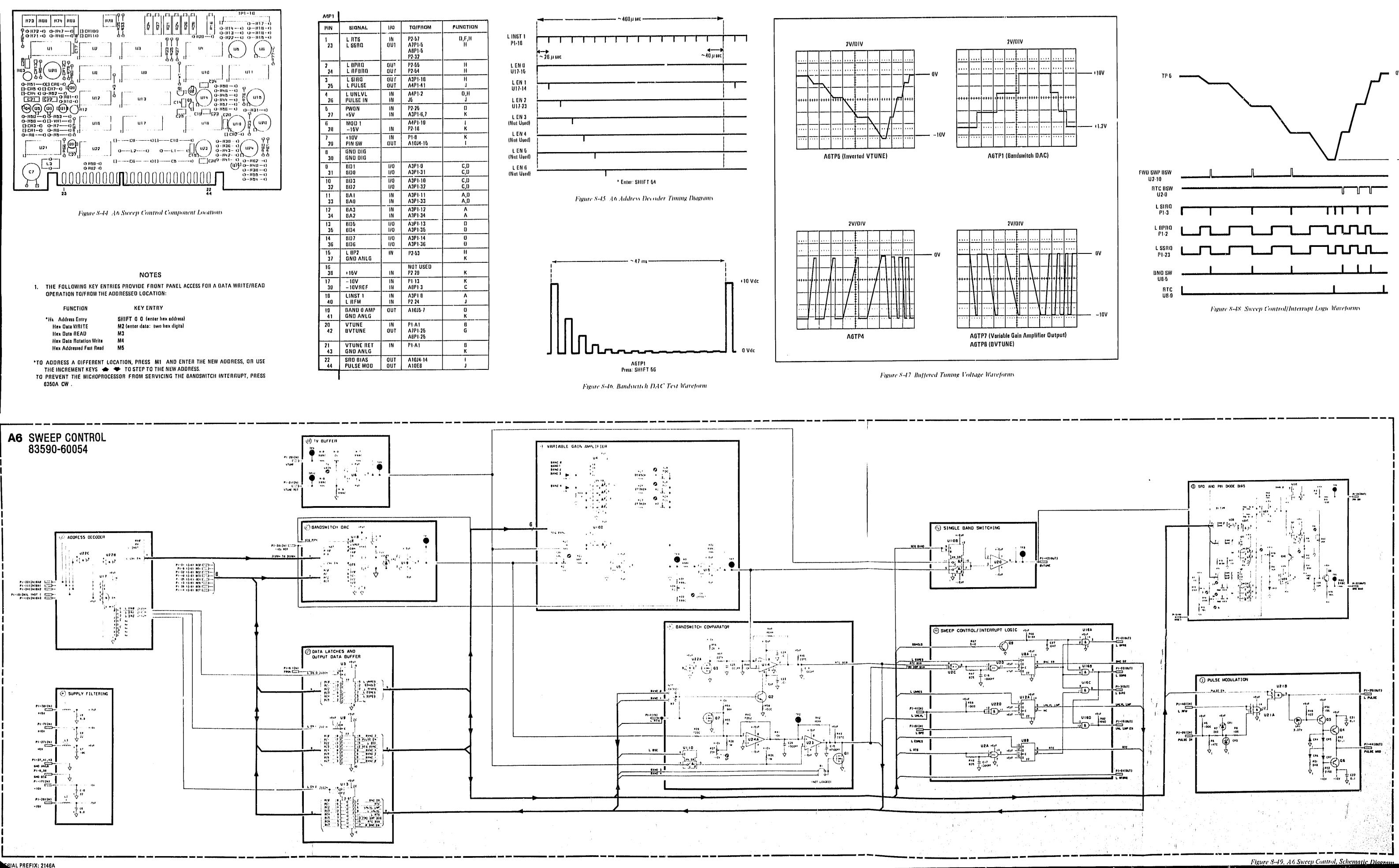
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Hex Data WRITE Rex Data READ

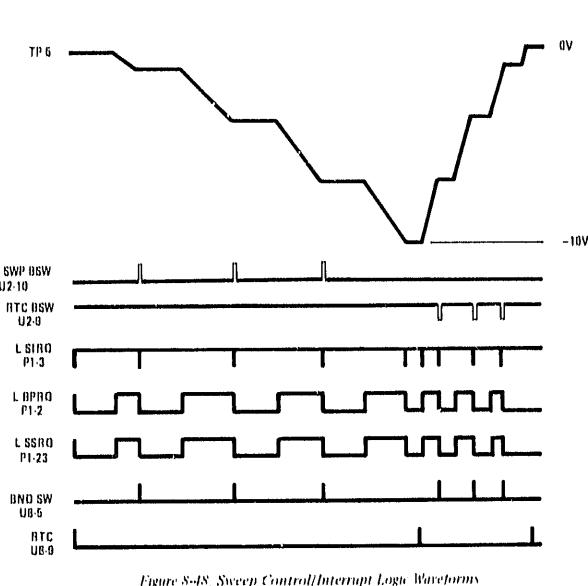
- M3 - M4 M5

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A8P1				
PIN	SIGNAL	0/1	то/рном	FUNCTION
1 23	L RTS L 5580	IN DUT	P2+67 A7P1+6 A8P1+6 P2-32	D,F,H H
2 24	L OPRO	700	P2/66	11
	L REDRO	100	P2/64	1
3 26	L SIRO	007	A3P1-10	H
	L PULSE	007	A4P1-41	J
4	L UNLVL	IN	A4P1-2	1,0
26	PULSE IN	IN	JG	J
5	PWON	IN	P2-26	0
27	+5V	IN	A3P1-6,7	K
6	MOD 1	IN	A4P1+10	і
28	-16V		P2+18	К
7	+10V	1N	P1/8	к
20	PIN 6W	0UT	A10J4/15	
8 30	GND DIG GND DIG			
0	8D1	1/0	A3P1-0	C,D
31	8D0	1/0	A3P1-31	C,D
10	803	1/0	A3P1-10	C,D
32	802	1/0	A3P1-32	C,D
11	BAT	IN	A3P1-11	A,0
33	BAO	IN	A3P1-33	A,0
12	8A3	IN	A3P1-12	A
34	8A2	IN	A3P1-34	A
13	805	1/0	A3P1-13	D
36	804	1/0	A3P1-36	D
14	8D7	0/1	A3P1-14	0
36	8D6	1/0	A3P1-36	
15 37	L BP2 GND ANLG	IN	P2+63	H K
16 38	+16V	IN	NOT USED P2 20	ĸ
17	– 10V	IN	P1-13	K
30	– 10VREF	IN	A0P1-3	C
10	LINST 1	IN	A3P1 0	۸
40	L RFM	IN	P2-24	۱
19 41	BAND 0 AMP GND ANLG	our	A 10J5-7	0 К
20 42	VTUNE BVTUNE	IN OUT	P1-A1 A7P1-26 ABP1-26	B G
21 43	VTUNE RET GND ANLG	IN	P1-A1	B K
22	SRD BIAS	OUT	A 10J4-14	ו
44	PULSE MOD	OUT	A 10EB	ג



#### A7 YTM DRIVER / A9 REFERENCE RESISTOR, CIRCUIT DESCRIPTION

#### NOTE

All reference designators refer to the A7 assembly unless otherwise noted,

#### General

The A7 YTM Driver assembly converts the buffered tuning voltage from the A6 Sweep Control assembly into a drive current. The A9 Ref Resistor assembly provides the current driver to control the frequency of the YIG Tuned Multiplier (YTM).

Multiplying Digital-to-Analog Converters (DACs) scale and offset the buffered tuning voltage to the frequency end-points in each band. Delay compensation is generated and summed with the tuning voltage. Also summed with the tuning voltage are low frequency external FM and a Band 1 offset. The resultant waveform at TP6 is then converted to a current-drive for the YTM's Main Coil.

#### Address Decoder and Data Latch (A)

The A7 YTM Driver uses hexadecimal address locations 2C88 through 2C8F. L INST2, BAU, BAL, and the L DAC EN output of U8C are decoded by the Scaled Voltage Tune and Offset DACs as hexadecimal addresses 2C88 through 2C8B. (Note that these addresses from U16 are not used.) U16 is a 3-to-8 decoder that is enabled when L INST2 is active low and address line BA3 is active high. U16 decodes address lines BA0 through BA2.

U12 is a control latch which stores commands from the 8350A for the control lines used on the A7 YTM Driver assembly, primarily for delay compensation. The command byte is latched into U12 when L EN 7 pulses low. Refer to the Delay Compensation, and Summing Amplifier sections for detailed descriptions of these control lines.

#### Scaled Voltage Tune DAC (B) Offsut DAC (C)

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The Scaled Voltage Tune and Offset DACs function together to determine the bandpass frequency of the YTM. The Offset DAC determines the start frequency of each band while the Scaling DAC sets scales the BVTUNE input to tune the YTM over the required frequency range for each band.

BVTUNE is a series of 0 to -10V ramps with each ramp corresponding to a frequency band. DAC U17 scales each ramp differently according to the frequency range the YTM must sweep to cover the frequency range of the band. (See SCVTUNE waveform at TP9 in Figure 8-56.) Since the YTM is not used as a filter for Band 0, the DAC output is set to 0V for Band 0.

U17 and U13 are 12-bit microprocessor-compatible DACs, which latch data in three four-bit nibbles. These DACs share the same address locations, but are loaded by different data lines (D0-D3 load U13 and D4-D7 load U17).

U17 scales the buffered tuning voltage (BVTUNE) according to the binary pattern loaded at its inputs. Inverting amplifier U18 is included in the feedback path to convert the current output of the DAC to a voltage. CR1 prevents

transients from damaging the DAC during turn-on. C18, along with the DAC's internal feedback resistor, determines the bandwidth of the circuit. The waveform at TP9 is a scaled ramp (sawtooth waveform for multiband sweeps), with a maximum range of 0 to +10Vdc. See Figure 8-56.

U13 scales a stable -10V REF voltage according to the binary pattern loaded at its inputs. Inverting amplifier U14 works with the DAC's internal feedback resistor to provide a programmable offset voltage between 0 and +10Vdc at TP1. See Figure 8-57, CR7 protects the DAC from turn-on transients. C15 and the DAC's internal feedback resistor determine the bandwidth of the circuit.

Delay Compensation (E)

The delay compensation circuit is used to compensate the A12 YTM for the inherent inaccuracy caused by delay in the magnets at fast sweeps. SCVTUNE (a scaled ramp from the Scaled Voltage tune DAC), OFFSET (an offset voltage that sets the start frequency of each band), and YTM LO FM (a voltage proportional to the low frequency FM applied to the 8350A rear panel FM INPUT) are summed by U19 to provide a voltage with a slope proportional to the change in YTM frequency. This voltage ramp is sent to two separate signal processors: 1) a Voltage Follower/Subtractor whose output is equal to zero at start of sweep and at the band switch points. The amplitude is proportional to sweep width; and 2) a Differentiator whose output is proportional to the rate of frequency change while sweeping. These two signals are then multiplied in the Analog Multiplier U20. The delay compensation is summed into the main coil driver voltage in the Summing Amplifier.

During retrace, and momentarily during bandswitching, analog switch U10B closes. In this condition, UIIC together with R6, R8, R9, and R7 form a subtractor circuit. Both inputs are the input signal so they cancel in the operational amplifier and the resulting output is 0V, regardless of the input level. With U10B closed, C4 charges to one half the value of the input signal (R8 and R9 form a voltage divider). Ul0B opens again during the sweep which leaves only C4 in the feedback path of UIIC. Since there is no discharge path with U10B and U10A open, C4 remains charged to the level it had just before U10B was opened. UHC now operates as a voltage tollower, with the output level shifted by the voltage across C4. Therefore, the output of U11C has one half the slope of the input signal and returns to 0V whenever U10B is closed during retrace and bandswitching. Two sets of scaling (HI) and offset (LO) adjustments on the output of UIIC accurately scale and offset the Voltage Follower/Subtractor output for both a single (SGL) and sequential (SEQ) band sweep. Analog switches UI0D and UI0C select the correct input for inverting amplifier UIID. The output generated at TP5 is one input to the analog multiplier.

If the sweep is stopped momentarily, such as when an external counter is used, L SSRQ is pulled low by the 8350A mainframe. When U9A is closed by a low on the L SSRQ control line to U8A, C4 slowly recharges through R62. Thes when L SSRQ is pulled the output of ULIC will begin to go to zero volts, but may or may not reach zero volts depending on the length of time L SSRQ was pulled. When L SSRQ goes high again and the sweep continues, U9A opens and U11C resumes its voltage follower operation.

The U19 summing anplifier output is also applied to a Differentiator (U11B) with a time constant that is selected by analog switches U9A and U9B. By selecting either C6 (for sequential sweep) or C13 (for single band sweep) in

parallel with C3, the UI1B output is scaled for either single or multiband (sequential) sweeps. The output is amplified and inverted by UIIA and is applied at TP2 to the second input of the analog multiplier. The output at TP4 is connected to U20 pin 7 to provide feedback for an operational amplifier internal to U20. The Z adjust at U20 pin 6 allows nulling of the offset voltage appearing at DLY COMP. This is done when in CF  $\Delta$ F mode where  $\Delta$ F equals zero.

During sweep retrace, the YTM must change frequency rapidly from the high end of its range to the low end, and does not have enough time to naturally settle to the proper start frequency. Unless the YTM is forced to the low end of its range, this could result in a frequency tracking error, and a resultant loss of output power, at the start of each sweep. In order to force the YTM to settle quicker, C17 is charged during the YTM retrace by the differentiator output through CR2. Timer U5 is triggered by L RTC COMP at the end of sweep retrace. The timer pulse output momentarily closes analog switch U9C, and C17 discharges through R57 and is applied as Retrace Compensation to the Summing Amplifier. This compensation voltage forces the YTM to the low end of its range to avoid frequency tracking errors after a retrace. The amount of compensation applied is proportional to the pulse width of the timer output. and is adjusted by R55.

#### +20V Tracking (F)

Inverting amplifier U15 monitors the +20V line used to supply current to the YTM. If the +20V supply becomes loaded down or drifts, the YTM Main Coll current and, consequently, the YTM bandpass frequency, will try to change. However, UI5 senses any drift in the +20V FREQ REF line, and provides a correction signal so that the resultant YTM DRIVE Voltage (TP6) is compensated for the drift. ZRO adjustment R22 compensates for inaccuracies between U15 and summing amplifier U21.

#### Summing Amplifier (G)

U21 provides the summing point for the scaled tuning and offset voltages, and provides a drive voltage (YTM DRIVE V) for the Current Driver. Several correction signals are summed at this junction:

SCVTUNE provides the scaled ramp portion of theYTM DRIVE Voltage. R19, GAIN, fine-tunes the range of the scaling DAC.

OFFSET adjusts the YTM DRIVE Voltage so that the YTM Coil is driven between the proper end points, as determined by the front panel controls. R24, 'OFS', line-tunes the range of the Offset DAC.

SUPPLY VOLTAGE CORRECTION provides a compensation signal, from the +20V Tracking / mplifier, to offset changes in the reference supply.

DLY COMP, from the Delay Compensation circuit, is added to correct for lags in the response time of the YTM. This compensation is derived from SČVTUNE.

RTC COMP, from the Delay Compensation circuit, is a momentary correction voltage that forces the YTM to the low end of its frequency range after a sweep retrace. This compensation is derived from SCVTUNE.

BI OFS is summed in through U9D when the BAND I line from U12 is

YTM LO FM sums low frequency components of external FM signals onto the drive voltage when crossover coupling of the FM signal is selected. (Configuration switch A3SI provides this adjustment. Refer to the A3 Service Sheet for further detail.) Due to the response time limitations of the YIG Oscillator's main coil, only frequencies below 700 Hz are passed from the A5 FM Driver assembly to the A7 YTM assembly.

#### Frequency Cal Switches/Output Data Buffers (D)

DIP switches S1 and S2, with their corresponding data bus buffers, are used to digitally calibrate the low and high end frequencies in Band 2. The data on these switches is read by the microprocessor during power-up and INSTR PRESET and is used to calculate the settings for the Scale and Offset DACs. SI, with pullup resistor package UI, is read through U3 when enabled by L EN4. SI determines the value of the Offset DAC and calibrates the low end frequency. S2, with pull-up resistor package U2, is read through U4 when enabled by L ENS. This establishes the Scale DAC values, and calibrates the high end frequency. The ninth and tenth bits from SI and S2 are read through  $U\overline{7}$ .

SI and S2 switch positions encode binary numbers to set up the Offset and Scaling DACs. Refer to the Frequency Accuracy adjustment procedure in Section V for instructions. Figure 8-55 illustrates the switch configurations.

YTM Coll Current Source (H)

YTM Coll Current Driver A9 (1)

The YTM Coil Current Driver works with the chassis mounted Reference Resistor R2 and YTM Coil Driver A9Q2 to drive a current proportional to the drive voltage through the YTM's main tuning coil.

U22, Q1, Q2, and A9Q2 comprise a voltage-to-current converter and current driver for the YTM's main coll. The non-inverting input of U22 receives the YTM DRIVE Voltage signal. The inverting input of U22 monitors the voltage drop across reference resistor R2, which is directly proportional to the coil current. If the drive current is not tracking the drive voltage, U22 will produce an error voltage to correct the difference. Emitter-follower Q2 and commonemitter-stage QI provide the current gain needed to drive A9Q2. Q2 and Q1 emitter currents are also drawn through chassis mounted R2, and therefore, sensed by U22, VR1 and CR5 protect the current drive transistors by limiting voltage spikes due to sudden changes in the coil current. R33 helps to dampen ringing caused by the parasitic capacitance and the inductance of the YTM coll.

CR3, CR4, CR6, CR8, and their associated factory-select resistors provide a four break-point compensation network to correct for non-linearities in the YTM characteristics.

#### NOTE

The values of the factory-select resistors are stamped on a label, attached to the RF casting. Matching resistor sets (mounted on a header) are supplied with replacement YTMs and must be installed on the A7 YTM assembly. The new label indicating the replacement resistor values should be attached to the RF casting.

If the A7 YTM Driver Assembly is replaced, the shaping resistors from the defective board (which are mounted on a header) must be reinstalled in the new assembly.

#### NOTE

#### if the YTM needs little or no compensation, nome or all of the factory-select resistors may be omitted.

#### A7 YTM Driver/A9 Reference Resistor Assemblies Troublesheeting

#### NOTE

#### All reference designators refer to the A7 assembly, unless otherwise noted.

The A7 YTM Driver and A9 Reference Resistor assemblies are primarily responsible for controlling the YTM bandpass frequency. A failure in these assemblies usually results in a low RF power output. (Power losses that change with sweep time are usually related to delay compensation.) Power losses that may be corrected with the front panel PEAK control may be due to improper calibration. The problem may be relieved by performing the Frequency Accuracy adjustment in Section V.

#### Gonoral

Check that all power supply voltages are present.  $\pm 20V$  (on the A7 assembly) and  $\pm 40V$  (on the A12A1 assembly) supply the YTM. Ensure that cable plugs are correctly seated over the correct jacks throughout the Plug-in. With the line power off, remove and reseat the A7 assembly to assure good motherboard contact.

#### NOTE

Unless specifically stated otherwise, the troubleshooting waveforms and voltages described below occur when the Plug-in is sweeping across its full range (INSTR PRESET conditions).

#### Sweep Circuitry

A failure in the sweep circuitry may cause the YTM to tung between improper frequency endpoints, or not sweep at all. If the YTM Drive Voltage is incorrect or missing, the instrument will have low RF output power for Bands 1 through 3.

- 1. Check the YTM DRIVE V (TP6) for the waveform shown in Figure 8-59. If this waveform is correct, troubleshooting should continue with the YTM Current Driver section below.
  - a. If YTM DRIVE V is incorrect, check BVTUNE (A6TP8) for a series of 0 to -10V ramps. If they are missing or of the wrong amplitude, refer to the A6 Sweep Control service sheet for further troubleshooting.
  - b. If the waveform at TP6 appeared to be level-shifted, check -10 VREF (A8TP12) for exactly -10 °de. Next, with the Plug-in sweeping its entire range, check OFFSET (TP1) for the waveform in Figure 8-57. If this signal is incorrect, select a CW frequency of 20.0 GHz and press SHIFT 5 2. Check TP1 for the waveform shown in Figure 8-54. If this fails, check address decoding using the Digital Control troubleshooting procedure described below.

- 2. If BVTUNE is conset, check SCVTUNE (TP9) against the waveform shown in Figure 8.56. If it appears to be bad, run the Scale DAC Test by setting a CW frequency of 20.0 GHz and pressing SHIFT 5 2. Check that U17 pln 15 is at =10 Vdc. Then check TP9 for the waveform shown in Figure 8.56. If this fails, check address decoding using the Digital Control troublesh opting below.
- 3. Check +20V FREQ REF (TP8) for +20 Vdc ±10 mV. If it is not, trace the supply voltage back to the 8350Å. Then check that SUPPLY VOLTAGE CORRECTION (U15 pin 6) is at approximately -10 Vdc. If it is not, troubleshoot U15.
- Finally, check that the summing junction, U21 pin 2, is at 0 Vdc. If it is not, troubleshoot U21.

#### **Delay Compensation**

A failure in the Delay Compensation circuit is usually indicated by RF output power variations that change with sweep time. The delay compensation has little offect at sweep times greater than 100 milliseconds. On the 8350A enter-INSTR PRESET and check waveforms in Figure 8-58.

#### YTM Drive Circuits

 Check +20V FREQ REF at TPB for +20V ±10 mV. If it is not, troubleshoot back to the mainframe supply.

The circultry surrounding U22 and A9Q2 is responsible for converting the YTM DRIVE V to a drive current for the YTM coll. A failure here will usually result in extreme RF power losses for Bands 1-3.

- 2. Press INSTR PRHSET to sweep the entire range of the Plug-in. Check TP7 for the waveform shown in Figure 8-59. This represents the voltage (not the current) across the YTM's main coil, and will give an indication as to whether current is passing through the coil. If this waveform is correct, subpact the A12 YTM or the SRD Bias circuit on the A6 Sweep Control assembly. Refer to the RF Section Service Sheet.
- Check TP3, This voltage should track the YTM DRIVE V (Figure 8-59). If it does not, troubleshoot U22, Q1, Q2, chassis mounted R2, and A9Q2.
  - a. Chase's mounted R2 should be checked by removing the A9 assembly from the instrument. The ohnesser reading should be approximately 59Ω.
  - b. While the A9 assembly is removed from the instrument, check the collector-base and base-emitter junctions of A9Q2 with an olummeter. These junctions should show only a few hundred ohms when forward blased, and a high impedance in the reverse direction. If A9Q2 is found to be shorted or opened, make sure that protection diodes VR1 and CR5 are good before replacing the transistor.
  - c. Q1 and Q2 can be checked, using the procedure above, while they are still in the circuit. The line power should be off.
  - d. If the above check verify the components, replace U22.

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#### Digital Control

The Address Decoder and Data Latch and Frequency Cal Switches comprise the digital control for the A7 assembly. A failure in these components usually results in large power losses for Bands 1 through 3, and will often cause an unleveled power condition.

To check the address decoding circuitry enter SHIFT 5 4 and perform the following:

- 1. Examine L INST2 (PI-18) for activity. If none is found, troubleshoot the A3 assembly.
- 2. If L INST2 is functional, check each of the L ENn lines (U16) for the pulses shown in Figure 8-53. If these are incorrect, but the address lines show activity, replace U16. If the address lines seem locked high or low, troubieshoot the address buffer on the A3 assembly.

#### NOTE

U3, U4, and U7 are checked by reading data while changing switch rettings. Before altering the switch settings on A781 and A782, write down the present configuration. Return the switches to their original statue after troubleshooting. If this is not done, the frequency endpoints will have to be recallbrated.

3. To check output buffer U7, press INSTR PRESET, and make the following key entry:

SHIFT	Ű	0		Enters the Hex Data command
2 GHz	. n	8	dBm dB	Address location 2C8E (U7)
M3				Hex Data Read

The hex digits displayed in the 8350A front panel FREQUENCY/TIME window should change when the S1 and S2 switch positions 8 and 9 are toggled.

- 4. U3 and U4 can each be checked with Hex Data Read (see above) at address 2C8C or 2C8D. The hex digits should change when the corresponding Freq Cal switches are changed.
- 5. Exercise U12 with Hex Data Rotation Write. Enter:

SHIFT	0	0		Enters Hex Data command
2 GHz	5	8	BKSP	Address location 2C8F (U12)
M4				Fiex Data Rotation Write

Check the outputs of U12 against the waveforms shown in Figure 8-2.

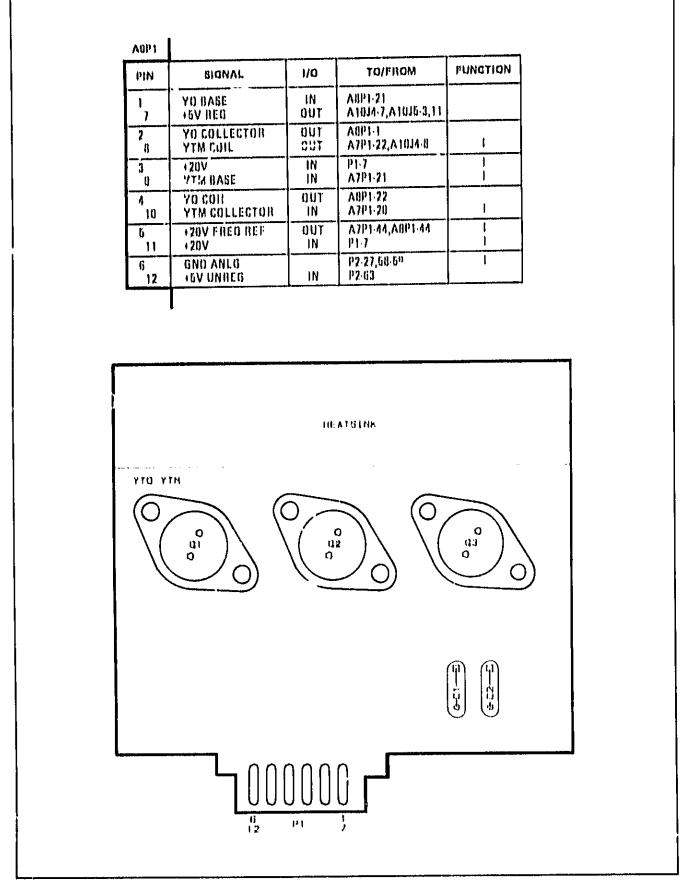
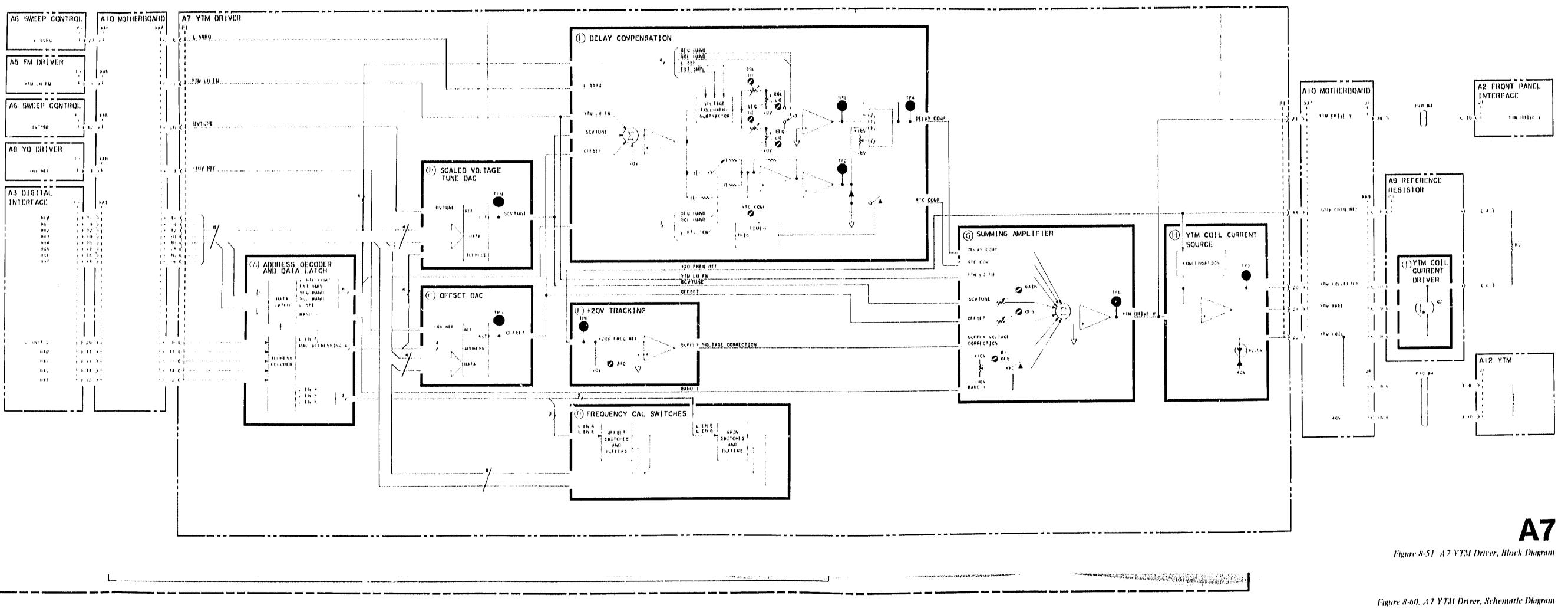


Figure 8-50, A9 Reference Resistor, Component Locations

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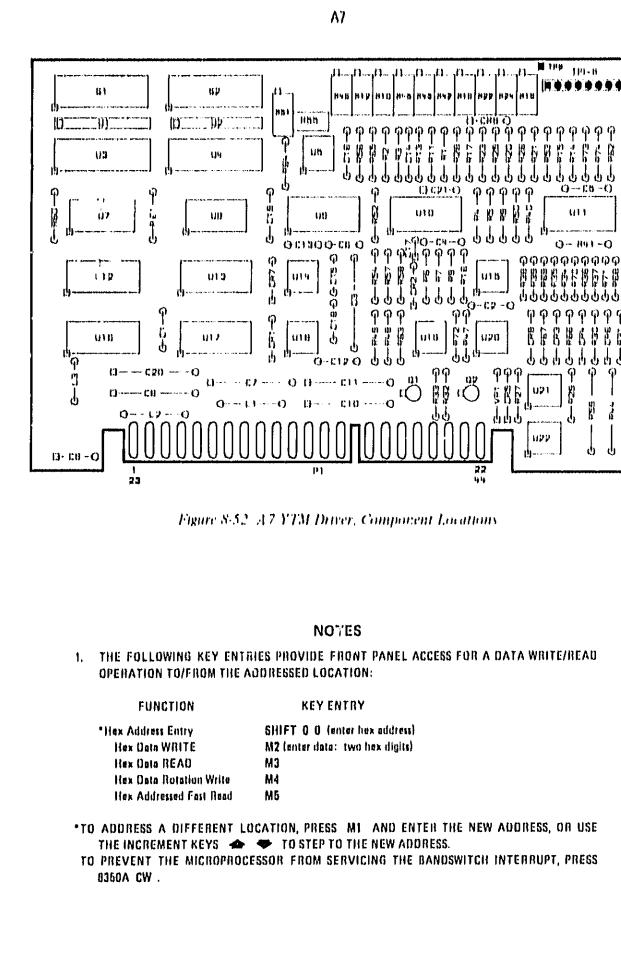
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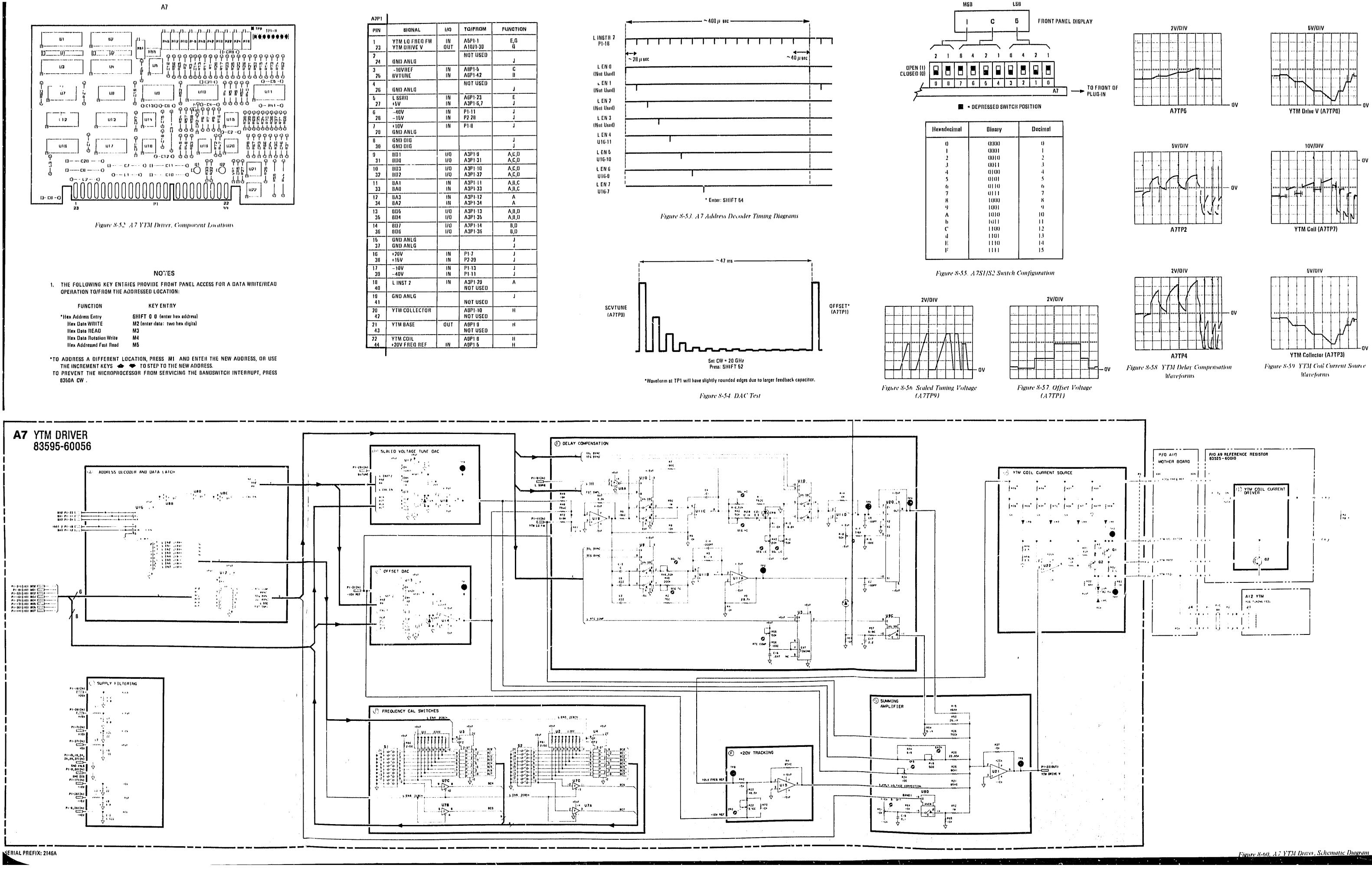
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SERIAL PREFIX: 2146A

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#### AB YO DRIVER / A9 REFERENCE RESISTOR, CIRCUIT DESCRIPTION

#### NJTE

#### All inference designators infer to the AB assembly unless otherwise noted.

#### **GENERAL**

The AB YO Driver assembly converts the buffered tuning voltage from the A6 Sweep Control assembly into a drive current. The A9 Ref Resistor assembly provides the current driver to control the frequency of the YIG Oscillator (YO).

Multiplying Digital-to-Analog Converters (DACs) scale and offset the buffered uning voltage to the frequency end-points in each band. Delay compensation is generated and summed with the tuning voltage. Also summed with the tuning voltage is low frequency external FM. The resultant waveform at TP10 is then converted to a current-drive for the YO's Main Coil.

#### Address Decodor and Data Latch (A)

The AB YO Driver uses hexadecimal address locations 2C80 through 2C87. L. INST2, BA0, BA1, and the L DACEN output of USD are decoded by the Scaled Voltage Tune and Offset DACs as hexadecimal addresses 2C80 through 2C83. (Note that these addresses from U16 are not used.) U16 is a 3-to-8 decoder that is enabled when L INST2 and address line BA3 are both low. U16 decodes address lines BA0 through BA2.

1013 is a control latch which stores commands from the 8350A for the control lines used on the A8 YO Driver assembly, primarily for delay compensation. The command byte is latched into U13 when L EN 7 pulses low. Refer to the Delay Compensation, Summing Amplifier, and YO Coil Current Source sections for detailed descriptions of these control lines.

#### Banled Voltage Tune DAC B Offeet DAC C

The Scaled Voltage Tune and Offset DACs function together to determine the frequency of the YIG oscillator. The Offset DAC determines the start frequency of each band while the Scaling DAC scales the BVTUNE input to tune the YIG oscillator over the required frequency range for each band.

BVTUNE is a series of 0 to ~10V ramps with each ramp corresponding to a frequency band. DAC 017 scales each ramp differently according to the frequency range the YO must sweep to cover the frequency range of the band. (See SCVTUNE waveform at TP2 in Figure 8-67.)

U17 and U14 are 12-bit microprocessor-compatible DACs, which latch data in three four-bit nibbles. These DACs share the same address locations, but are loaded by different data lines (D0-D3 load U14 and D4+D7 load U17).

U17 scales the buffered tuning voltage (BVTUNE) according to the binary pattern loaded at its inputs, inverting amplifier U18 is included in the feedback path to convert the current output of the DAC to a voltage, CR1 prevents transients from damaging the DAC during turn-on. C14, along with the DAC's internal feedback resistor, determines the bandwidth of the circuit. The waveform at TP2 is a scaled ramp (sawtooth waveform for multiband sweeps), with a maximum range of 0 to 4 10Vdc. See Figure 8-67.

U14 scales a stable -10V REF voltage according to the binary pattern loaded at its inputs. Inverting amplifier U15 works with the DAC's internal feedback resistor to provide a programmable offset voltage between 0 and  $\pm 10Vde$  at TP3. See Figure 8-68. CR7 protects the DAC from turn-on transients. C15 and the DAC's internal feedback resistor determine the bandwidth of the circuit.

#### Delay Compensation (E)

The delay compensation block circuitry is used to compensate the A13 YIG Oscillator for the inherent inaccuracy caused by delay in the magnets at fast sweeps. The input signal is SCVTUNE, a scaled ramp from the Scaled Voltage ture DAC, the slope of which is proportional to the change in frequency. SC VTUNE is sent to two separate signal processors: 1) a Voltage Follower/Subtractor whose output is equal to zero at start of sweep and at the band switch points. The amplitude is proportional to the rate of frequency change while sweeping. These two signals are then multiplied in the Analog Multiplier UI2. If the Sweep Oscillator is in a swept mode, U6 enables the delay compensation which is summed into the main coil driver voltage in the Summing Amplifier.

During retrace, and momentarily during bandswitching, analog switch U19B closes. In this condition, U10C together with R6, R8, R9, and R7 form a subtractor circuit. Both inputs are the input signal so they cancel in the operational amplifier and the resulting output is 0V, regardless of the input level. With U19B closed, C4 charges to one half the value of the input signal (R8 and R9 form a voltage divider). U19B open: again during the sweep which leaves only C4 in the feedback path of U10C. Since there is no discharge path with U19B and U19A open, C4 remains charged to the level it had just before U19B was opened. U10C now operates as a voltage follower, with the output level shifted by the voltage across C4. Therefore, the output of U10C has one half the slope of the input signal an , returns to 0V whenever U19B is closed during retrace and bandswitching. The output of U10C is scaled by the H1 adjust potentiometer and is applied, with an offset from the LO adjust potentiometer, to inverting amplifier U10D. The output generated at TP5 is one input to the analog multiplier.

If the sweep is stopped momentarily, such as when an external counter is used, L SSRQ is pulled low by the 8350A mainframe. When U19B is closed by a low on the L SSRQ control line to U8A, C4 slowly recharges through R62. Thus when L SSRQ is pulled the output of U10C will begin to go to zero volts, but may or may not reach zero volts depending on the length of time L SSRQ was pulled. When L SSRQ goes high again and the sweep continues, U19A opens and U10C resumes its voltage follower operation.

SCVTUNE is also applied to Differentiator &3 and U10B. The output is amplified and inverted by U10A and is applied at TP4  $\Box$  the second input of the analog multiplier. The output at TP9 is connected to U12 pin 7 to provide feedback for an operational amplifier internal to U12. The Z adjust at U12 pin 6 allows nulling of the offset voltage appearing at DLY COMP. This is done when in CF  $\Delta$ F mode where  $\Delta$ F equals zero.

During sweep retrace or at bandswitch points, the YIG Oscillator must change frequency rapidly from the high end of its range to the low end, and does not have enough time to naturally settle to the proper start frequency. Unless the YC is forced to the low end of its range, this could result in a frequency error at the start of each sweep and each bandswitch point. In order to force the YO to settle quicker, C20 is charged during the YO retrace by the differentiator output through CR2. Timer U9 is triggered by L RTC COMP at each bandswitch point and at the end of sweep retrace. The timer pulse output momentarily closes analog switch U19C, and C20 discharges through R67 and is applied as Retrace Compensation to the Summing Amplifier. This compensation voltage forces the YO to the low end of its range to avoid frequency errors after a retrace or bandswitch. The amount of compensation applied is proportional to the pulse width of the timer output, and is adjusted by R55. As the 83590A is sequent ally sweeping up between bands, the frequency range the YO must retrace to (each the start frequency of the next band decreases. Thus, the amount of retrace compensation required is reduced. The timer output pulse width is reduced accordingly. This is accomplished by inverting the Offset DAC output through Q1, and applying this negative voltage to the timer control voltage input at U9 pin 5. VR5 level shifts the Offset DAC output for proper biasing of QL

#### +20V Tracking (F)

Inverting amplifier U11 monitors the +20V line used to supply current to the YIG Oscillator. If the +20V supply becomes loaded down or drifts, the YO Main Coil current and, consequently, the frequency, will try to change. However, U11 senses any drift in the +20V FREQ REF line, and provides a correction signal so that the resultant YO DRIVE Voltage (TP10) is compensated for the drift. ZRO adjustment R22 compensate for inaccuracies between U11 and amming amplifier U20.

#### Summing Amplifier (G)

U20 provides the summing point for the scaled tuning and offset voltages, and provides a drive voltage (YO DRIVE V) for the Current Driver. Several correction signals are summed at this junction:

SCVTUNE provides the scaled ramp portion of the YO DRIVE Voltage. R19 GAIN, fine-tunes the range of the scaling DAC.

OFFSET adjusts the YO DRIVE Voltage so that the YO Coil is driven between the proper end points, as determined by the front panel controls. R24, 'OFS', fine-tunes the range of the Offset DAC.

SUPPLY VOLTAGE CORRECTION provides a compensation signal, from the +20V Vracking Amplifier, to offset changes in the reference supply.

DLY COMP, from the Delay Compensation circuit, is added to correct for lags in the response time of the YIG Oscillator. This compensation is derived from SCVTUNE.

RTC COMP, from the Delay Compensation circuit, is a momentary correction voltage that forces the YIG oscillator to the low end of its frequency range after a sweep retrace and each bandswitch point. This compensation is derived from SCVTUNE. YO LO FM sums low frequency components of external FM signals onto the drive volvage when crossover coupling of the FM signal is selected. (Configuration switch A3S1 provides this adjustment. Refer to the A3 Service Sheet for further detail.) Due to the response time limitations of the YIG Oscillator's main coil, only frequencies below 700 Hz are passed from the A5 FM Driver assembly to the A8 YO assembly.

#### -10V Reference (H)

Operational amplifier U5 generates a -10V output from the -6.2V reference voltage at its noninverting input. The amplifier gain is determined by feedback resistors R43, R44, and R45. Emitter follower Q2 provides the current. The -6.2V reference in ut to U5 is developed across 3 parallel zencr diodes to reduce noisc. Further noise reduction is provided by the RC network on the noninverting input of U5 and C17 across the feedback path. -15VF, through R1, provides the initial start-up bias.

#### Frequency Cal Switches/Output Data Buffers (D)

DIP switches S1 and S2, with their corresponding data bus buffers, are used to digitally calibrate the low and high end frequencies in Band 2. The data on these switches is read by the microprocessor during power-up and INSTR PRESTT and is used to calculate the settings for the Scale and Offset DACs. S1, with pull-up resistor package U1, is read through U3 when enabled by L EN4. S1 determines the value of the Offset DAC and calibrates the low end frequency. S2, with pull-up resistor package U2, is read through U4 when enabled by L EN5. This establishes the Scale DAC values, and calibrates the high end frequency. The math and tenth bits from S1 and S2 are read through U7.

S) and S2 switch positions encode binary numbers in set up the Offset and Scaling DACs. Refer to the Frequency Accuracy adjustment procedure in Section V for instructions. Figure 8-66 illustrates the switch configurations.

#### YO Coll Current Source () YO Joll Current Driver A9 (K)

The YIG Coil Current Driver works with the chassis mounted Reference Resistor RI and YO Coil Driver A9Q1 to drive a current proportional to the drive voltage through the YIG's main tuning coil.

U21, Q3, Q4, and A9Q1 comprise a voltage-to-current converter and current driver for the YO's main coll. The non-inverting input of U21 receives the YO DRIVE Voltage signal. The inverting input of U21 monitors the voltage drop across reference resistor R1, which is directly proportional to the coll current. If the drive current is not tracking the drive voltage, U21 will produce an error voltage to correct the difference. Emitter-follower Q4 and common-emitter-stage Q3 provide the current gain needed to drive A9Q1, Q4 and Q3 emitter currents are also drawn through chassis mounted R1, and therefore, sensed by U21, VR1 and CR5 protect the current drive transistors by limiting voltage spikes due to sudder, changes in the coll current. R33 helps to dampen ringing caused by the parasitic capacitance and the inductance of the YO coll. When 8350A CW and 83590A CW FILTER are selected, L CW goes low, energizing relay K1. C21 filters out noise in the YIG coil current, reducing the residual FM noise in the CW mode.

CR4, CR8, and their associated factory-select resistors provide a two break-point compensation network to correct for non-linearities in the YO characteristics.

#### NOTE

The values of the factory-select resistors are stemped on a label, attached to the RF casting. Matching resistor sets (mounted on a header) are supplied with replacement YOs and must be installed on the AB YO assembly. The new label indicating the replacement resistor values should be attached to the RF casting.

If the AB YO Driver Assembly is replaced, the shaping resistors from the defective board (which are mounted on a header) must be reinstalled in the new assembly.

#### NOTE

If the YO needs little or no compensation, some or all of the factory-select resistors may be omitted.

#### +6V Regulator A9 (L)

A9Q3 is a  $\pm 5$ Vdc regulator mounted in a single package. It receives the  $\pm 5$ V UNREG line (slightly more than 5V) from the mainframe, and regulates it for use in the Plug-in RF components.

#### AB YO Driver/A9 Reference Resistor Assemblies Troubleshooting

#### NOTE

### All reference designators refer to the AB assembly, unless otherwise noted.

The A8 YO Driver and A9 Reference Resistor assemblies are primarily responsible for controlling the RF output frequency. A fullure in these assemblies usually results in large frequency errors that may, or may not, be independent of sweep time. (Frequency errors that change with sweep time are usually related to felay compensation.) Frequency errors on the order of 500 MHz or less may ie due to improper calibration. The problem may be relieved by performing the Frequency Accuracy adjustment in Section V.

#### General

Check that all power supply voltages are present.  $\pm 20V$  (on the AB asembly) and  $\pm 40V$  (on the A13A1 assembly) supply the YO. Ensure that eable plugs are correctly seated over the correct jacks throughout the Plug-in. With the line power off, remove and reseat the AB assembly to assure good motherboard contact.

#### NOTE

Unless specifically stated otherwise, the troubleshooting waveforms and voltages described below occur when the Plug-in is aweeping across its full range (INSTR PRESET conditions).

#### Sweep Circuitry

A failure in the sweep circuitry may cause the YIG to sweep between improper frequency endpoints, or not sweep at all. If the YO Drive Voltage is missing, the instrument may toggle between two or more CW frequencies.

- 1. Check the YO DRIVE V (TP10) for the waveform shown in Figure 8-70. If this waveform is correct, troubleshooting should contine with the YO Current Driver section below.
  - a. If YO DRIVE V is incorrect, check BVTUNE (A6TP8) for a series of 0 to -10V ramps. If they are missing or of the wrong amplitude, refer to the A6 Sweep Control service sheet for further troubleshooting.
  - b. If the waveform at TP10 appeared to be level-shifted check -10 VREF (TP12) for exactly -10 Vdc. Next, with the Plug-in sweeping its entire range, check OFFSET (TP3) for the waveform in Figure 8-68. If this signal is incorrect, select a CW frequency of 20.0 GHz and press SHIFT -5 2. Caeck TP3 for the waveform shown in Figure 8-65. If this fails, check address decoding and the DAC latches using the Digital Control troubleshooting procedure described below.
- If BVTUNE is correct, check SCVTUNE (TP2) against the waveform shown in Figure 8-67. If it appears to br bad, run the Scale DAC Test by setting a CW frequency of 20.0 GHz and pressing SHIFT 5 2. Check that U17 pin 15 is at -10 Vdc. Then check TP2 for the waveform shown in Figure 8-65. If this fails, check address decoding using the Digital Control troubleshooting below.
- 3. Check +20V FREQ REF (A7TP12) for +20 Vde ±10 mV. If it is not, trace the supply voltage back to the 8350A. Then check that SUPPLY VOLTAGE CORRECTION (U11 pin 6) is at approximately -7.5 Vde. If it is not, troubleshoot U11.
- 4. Finally, check that the summing junction, U20 pin 2, is at 0 Vdc. If it is not, troubleshoot U20.

#### **Delay Componsistion**

A failure in the Delay Compensation circuit is indicated by frequency errors that change with sweep time. For sweep times greater than 100 milliseconds, delay compensation has little effect on the frequency accuracy. On the 8350A, enter INSTR PRESET and check waveforms in Figure 8-69.

#### YO Drive Circuits

1. Check 420V FREQ REF at A7TP12 for 420V ±10 mV. If it is not, troubleshoot back to the mainframe supply.

The circuitry surrounding U21 and A9Q1 is responsible for converting the YO DRIVE V to a drive current for the YO coil. A failure here will usually result in extreme frequency errors.

- 2. Press INSTR PRESET to sweep the entire range of the Plug-in. Check TP11 for the waveform shown in Figure 8-70. This represents the voltage (not the current) across the YO's main coil, and will give an indication as to whether current is passing through the coil. If this waveform is correct, suspect the YIG oscillator. Refer to the RF Section Service Sheet.
- 3. Check TP6. This voltage should track the YO DRIVE V (Figure 8-70). If it does not, troubleshoot U21, Q3, Q4, chassis mounted R1, and A9Q1.
  - a. To verify proper operation of U21, ground TP6 (R1 is a 25 Watt resistor). Prets 8350A CW. Vary the voltage at U21 pin 3 by changing the CW frequency as indicated on the front panel (20.0 GHz  $= -5V_i 2.4$  GHz = +12V). With TP6 at 0 Vdc, U21 pin 6 should be at approximately + 29 Vdc for positive input voltages, and approximately -10 Vdc for negative input voltages. If it is not, replace U21.
  - b. Chassis mounted R1 should be checked by removiag the A9 assembly from the instrument. The ohmmeter reading should be approximately 155Ω.
  - c. While the 49 assembly is removed from the instrument, check the collector-base and base-emitter junctions of A9Q1 with an ohmmeter. These junctions should show only a few hundred ohms when forward biased, and a high impedance in the reverse direction. If A9Q1 is found to be shorted or opened, make sure that protection diodes VR1 and CR5 are good before replacing the transistor.
  - d. Q3 and Q4 can be checked, using the procedure above, while they are still in the circuit. The line power should be off.

#### Digital Control

The Address Decoder and Data Latch, and Frequency Cal Switches comprise the digital control for the A8 assembly. A failure in these components usually results in large frequency errors.

To check the address decoding circulary enter SHIFT 5 4 and perform the following:

- 1. Examine L INST2 (P1-18) for activity. If none is found, troubleshoot the A3 assembly.
- 2. If L INST2 is functional, check each of the L ENn lines (U16) for the pulses shown in Figure 8-64. If these are incorrect, but the address lines show activity, replace U16. If the address lines seem locked high or low, troubleshoot the address buffer on the A3 assembly.

#### NOTE

U3, U4, and U7 are checked by reading data while changing switch settings. Before sitering the switch settings on ABS1 and AES2, write down the present configuration. Beturn the switches to their original status after troubleshooting. If this is not done, the frequency endpoints will have to be recalibrated.

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3. To check output buffer U7, press INSTR PRESET, and make the following key entry:

SHIFT 0	0		Enters the Hex Data command
2 GHz 6	8	6	Address location 2C86 (U7)
M3			Hex Data Read

The hex digits displayed in the 8350A front panel FREQUENCY/TIME window should change as the S1 and S2 switch positions 8 and 9 are toggled.

- 4. U3 and U4 can each be checked with Hex Data Read (see above) at address 2C84 or 2C85. The hex digits should change when the corresponding Freq Cal switches are changed.
- 5. Exercise U13 with Hex Data Rotation Write. Enter:

SHIFT 0	0		Enters Hex Data command
2 GHz s	8	7	Address location 2C87 (U13)
M4			Hex Data Rotation Write

Check the outputs of U13 against the waveforms shown in Figure 8-2.

#### -10V REFERENCE

Check TP12 for -10 Vde  $\pm 1$  mV. If this voltage is incorrect, perform the -10V Reference adjustment procedure provided in Section V of this manual. If the adjustment cannot be made, check the anodes of VR2-4 for -6.2 Vdc. If a voltage is incorrect, replace the zener diode. Check U5 pins 2 and 3 for -6.2 Vde  $\pm 0.15$  mV. If either measurement is incorrect, troubleshoot U5 and associated circuitry.

#### **5V Regulator**

Check A9U1 pin 1 for slightly over +5 Vdc (+5V UNREG from the 8350A). Remove RF ribbon cables W4 and W14 to check for the possibility of excess loading. Then check A9U1 pin 2 for +5 Vdc. If incorrect, replace A9U1.

#### **CW Filter**

Relay K1 and C2¹, duce residual FM by filtering the noise from the YO Coil current. The relay a unted by a line from U13. To check the data line, press 8350A CW . Enter

SHIF 2 G	•		0 8	-	Enters Hex Data command Address location 2C87 (UI3)
 M2	117.	ŋ	D	,	Hex Data Write
0 0	1	BK	SP	BKSP	Enters hex data 00 and FF

Alternate between 00 and FF. Check U13, pin 7. If it is inactive, make sure protection diode CR6 is good. Then replace U13,

If U13 is working, alternate between 00 and FF, as described above, and verity that contacts in relay K1 are opening and closing.

Model 83590A

Service

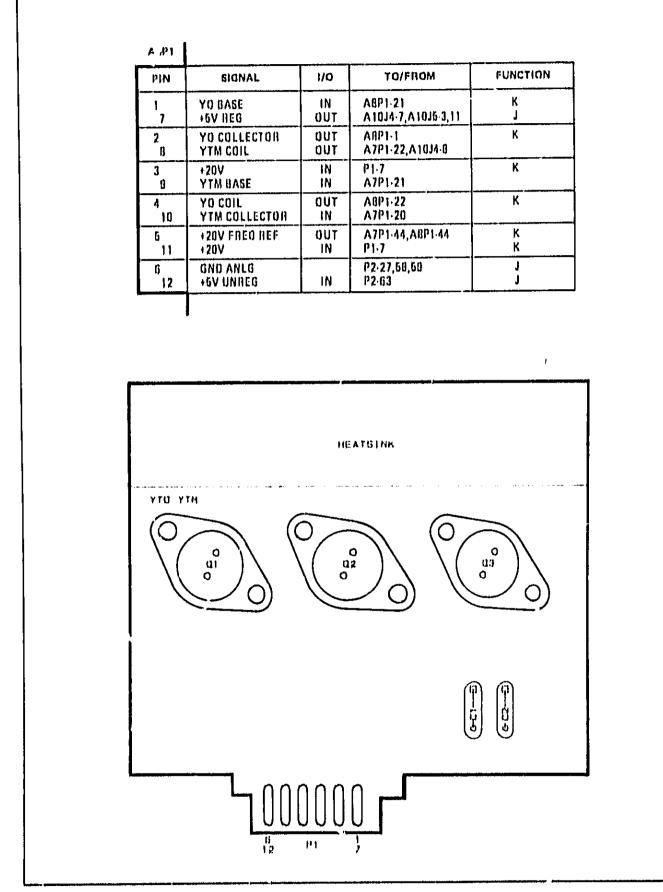
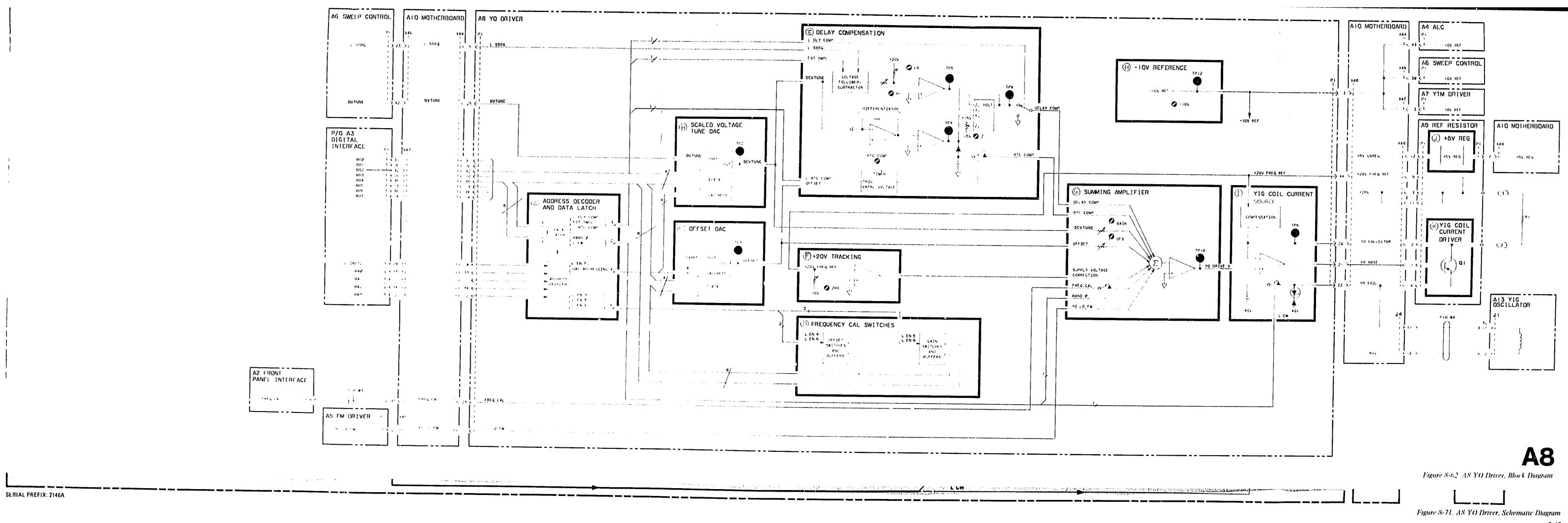
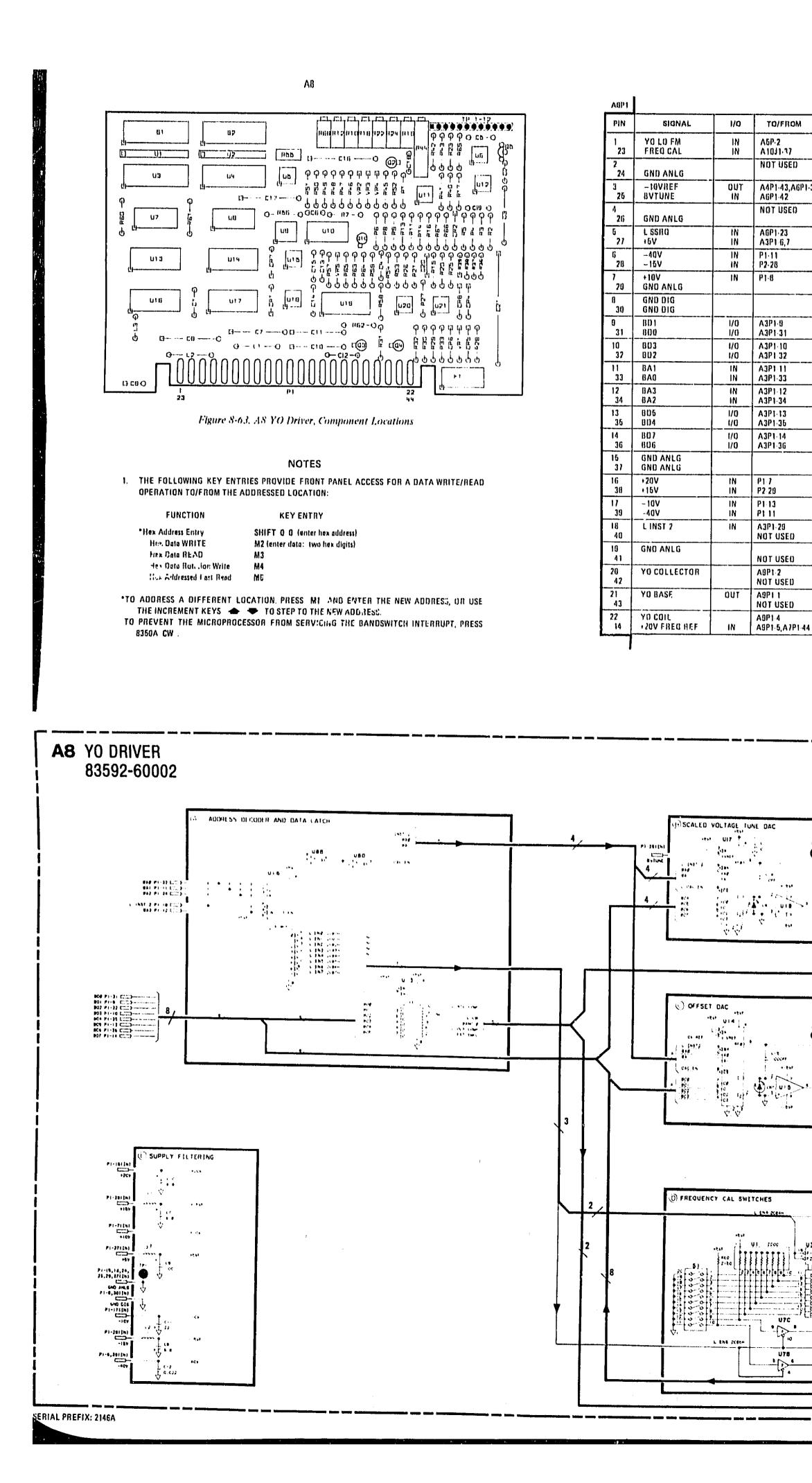


Figure 8-61. A9 Reference Resistor, Component Locations



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NOT USED

NOT USED

P1-11

P2-28

A3P1-9

A3P1-31

NOT USED

NOT USED

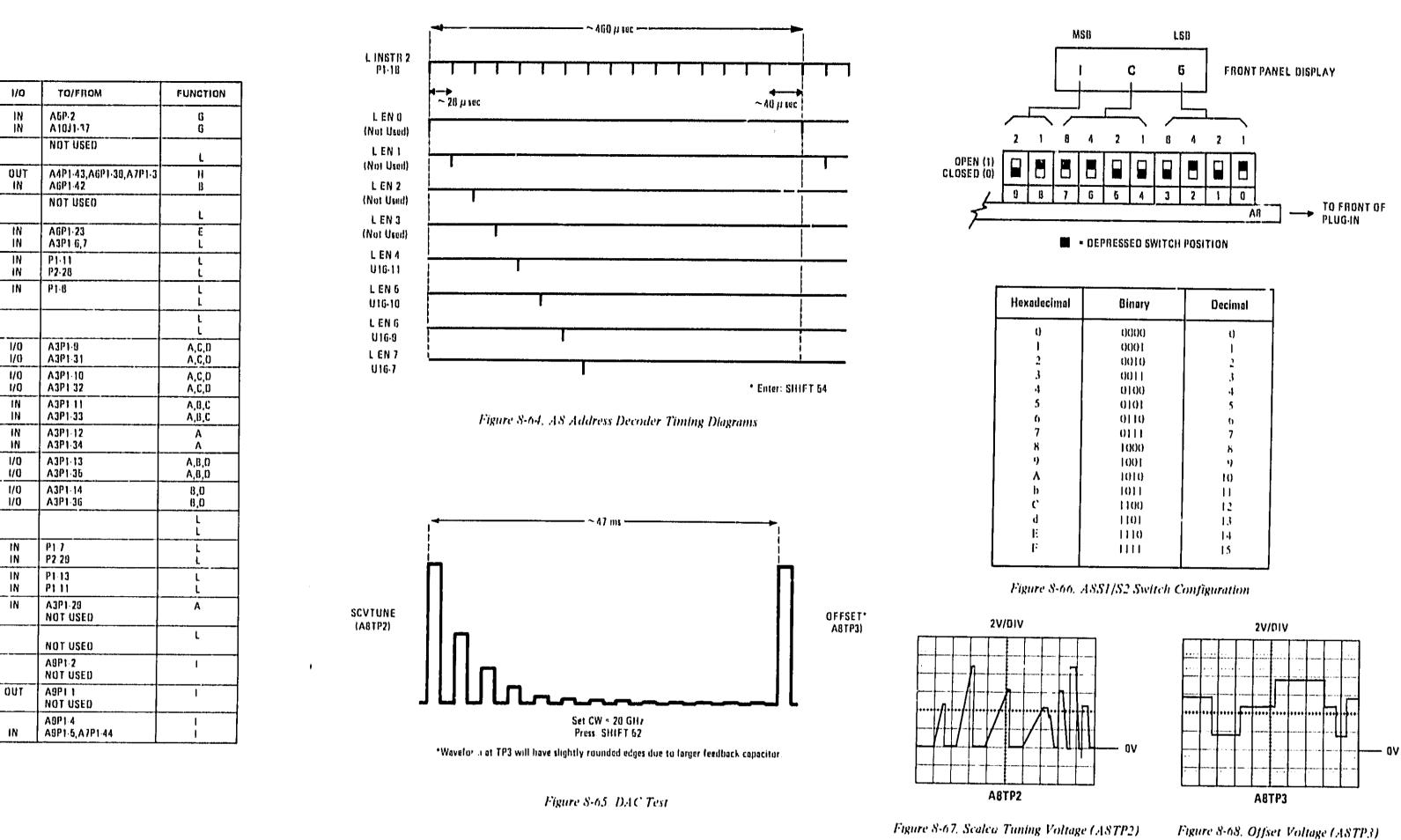
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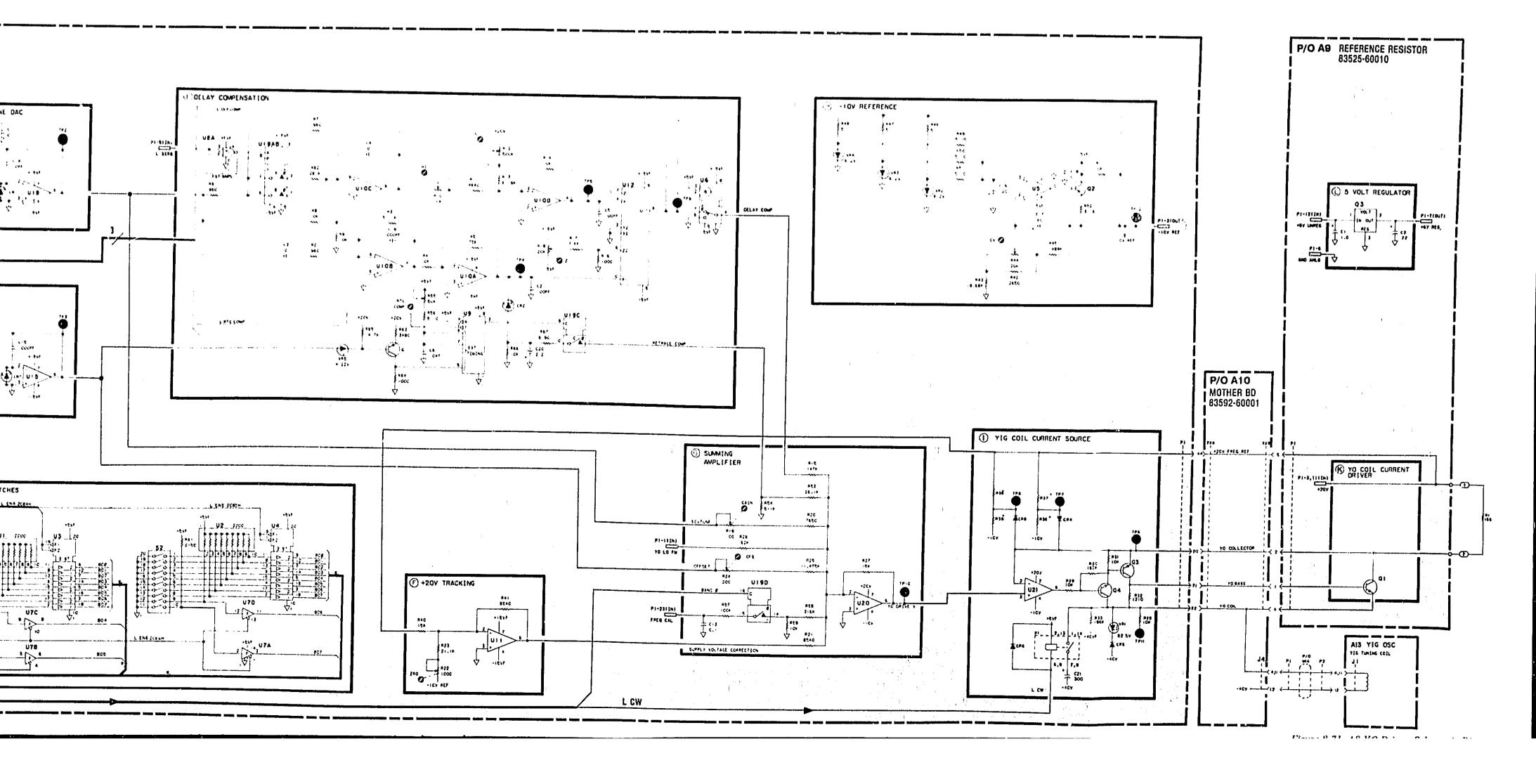
NOT USED

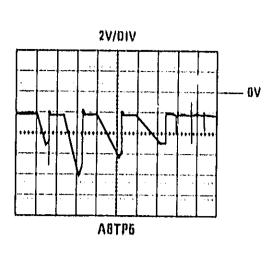
A9P1-2

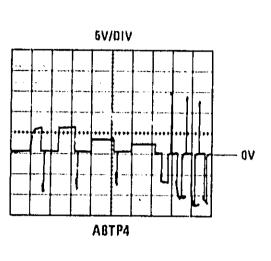
A9P11

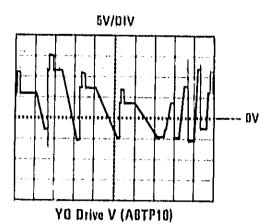
A9P1-4

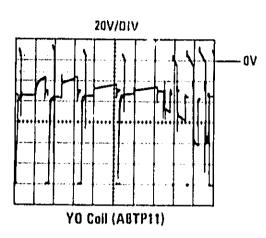


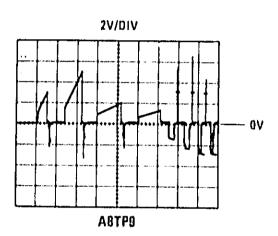


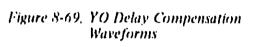












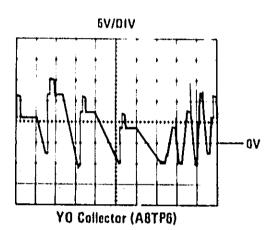


Figure 8-70. YO Coll Current Source Waveforms

#### **RF SECTION. CIRCUIT DESCRIPTION**

The RF Section includes the high frequency microcircuits, with their bias boards, that produce the actual RF output power. These components include A12, A13, A14, A16, A19, AT1, DC2, and CR1. All other Plug-in assemblies function essentially to control these RF components. The connections between microcircuits and other assemblies are provided on the Overall Block Diagram. Refer to the Overall Block Diagram circuit description for a more general, functional description.

#### NOTE

Assembly circuit descriptions are discussed in signal flow order. Headings indicate in which frequency bandle) the assembly is active.

#### BANDS 1 THRU 3

#### A13 YIG Oscillator

The A13 YIG (Yttrium-Iron-Garnet) Oscillator (YO) is a solid-state tunable microwave source. Its output frequency ranges from 2.0 to 7.0 GHz, with approximately +12 to +14 dBm of output power. The Oselllator's resonant tank circuit is basically a small YIG sphere with a resonant frequency which depends on the surrounding magnetic field strength. The magnetic field is established by an opposing pair of electromagnetic "main coils." Changing the current through the colls changes the magnetic field strength, and hence the frequency of oscillation. The sphere is lightly coupled to a bipolar transistor, providing the gain necessary to sustain oscillation. A FET amplifier provides the final output power gain.

The A13A1 YO Bias assembly supplies the biasing for the Oscillator and YO Amplifier. This board is matched to the YO, and cannot be separately replaced. The bias assembly provides zener protection against high voltage transients that appear across the main coils. It also supplies current for a resistive heater that helps maintain the Oscillator at a constant temperature. Factory adjustment R4optimizes the FET gate bias for minimum harmonics.

#### A16 Modulator/Coupler

The A16 Modulator/Coupler provides a modulator which is used for leveling and pulse modulation. The RF input from the YO is coupled off and supplied to the rear panel AUX OUTPUT with a power level of approximately 0 dBm.

The Modulator/Coupler uses a PIN diode modulator. The PULSE MOD input switches its PIN diode modulator full on or full off, and provides an RF on off ratio of greater than 30 dB.

The MOD 1 input provides amplitude control for Bands 1 through 3 and is used for amplitude feveling.

#### A14 Power Amplifier

The A14 Power Amplifier amplifies the fundamental YO output, covering the 2.0 to 7.0 GHz range. The Amplifier provides approximately 25 dB of gain at maximum leveled power.

The A14A1 Amplifier Bias assembly contains several factory adjusted bias adjustments. These are adjusted at the factory to minimize Larmonics

#### AT1 Isolator

AT1 provides 20 dB of isolation and is accountable for less than 1 dB of insertion loss. ATT improves the match to the YTM. BANDS 1 THROUGH 3

#### A12 YTM

The A12 Switched YIG Tuned Multiplier (YTM) RF input is applied through an impedance matching circuit to a Step Recovery Diode (SRD) which has an output that is rich in harmonics. The SRD BIAS applied to the diode is changed for each band to optimize the generation of the harmonic used for that band (Band 1 = Fundamental, Band 2 = Second Harmonic, Band 3 = Third Harmonic). The YIG Tuned Filter is a tunable bandpass filter which is tuned to the RF output frequency by the YTM Coil drive-current supplied by the A7 YTM Driver.

The filter's bandpass frequency is determined by a small YIG sphere with a resonant frequency that depends on the surrounding magnetic field strength. The magnetic field is established by an opposing pair of electromagnet colls. Changing the current through the coils changes the magnetic field strength, and hence the bandpass frequency.

The dynamic response of the YTM free how fast the bandpass frequency. changes for a fast change in coil current) is litened, due to the inductive and magnetic delays of the electromagnet coils and poles. Delay compensation circuits help during a sweep, but frequency modulation is limited to low modulation frequencies. Since the range of deviation for high-frequency modulation is limited by the YIG oscillator, the RF frequency stays within the bandpass of the YTM, and the YTM does not need to be modulated at higher rutes

The J2 switched input is not used in the 83590A RF Plug-in.

#### **DC2** Directional Coupler

The DC2 Directional Coupler has a ~16 dB coupling coefficient. The reversecoupled port is terminated. The coupled output is sent to the CRI Detector for leveling in Bands 1 through 3. The insertion loss is less than 0.8 dB, not including the coupled power loss.

#### CR1 Detector

The CRI Detector rectifies and filters the RF output coupled by the DC2 Directional Coupler for leveling in Bands 1 through 3. The internal diode is biased by circuitry on the A4 assembly.

#### A19 Step Attenuator (Option 002 Only)

On RF Plug-ins equipped with Option 002, the A19 Step Attenuator provides 70 dB of attenuation in 10 dB steps. Combined with the range of the ALC loop, this yields a maximum power range of +10 to -75 dBm. The Step Attenuator functions as three fixed attenuators, with 10, 20, and 40 dB of attenuation. (The 40 dB attenuator is actually two 20 dB attenuators which are selected as a pair.)

Latching relays close contacts which either insert these attenuators in the RF path or bypass them. The control and drive circuitry for the Attenuator is located on the A2 Front Panel Interface assembly. The insertion loss, with 0 dB attenuation selected, may be as much as 5 dB at 20 GHz (See specifications in Section D.

#### **RF OUTPUT Connector**

On Standard, Option 002, or Option 005 instruments, the RF output is directed to the front panel. On plug-ins with Option 004 (with or without other options). the output is directed to the rear panel. The standard RF output connector is a female type-N; for Option 005, the RF output connector is an APC-7 connector.

#### RF PATH TROUBLESHOOTING

#### NOTE

Many BF path failure symptoms are closely related to A4 ALC. failures. Refer to A4 Troubleshooting for additional informa-

The RF Path consists of the microcircuits and their bias boards that produce the actual front-panel RF output. These microcircuits are sealed, cannot be repaired, and are costly to replace. Ensure that associated control circuits (i.e. the other printed circuit boards) are working correctly before replacing any microcircuit components. When certain of a failure in the RF components, isolate the problem to a single microcircuit assembly.

Four RF assemblies have bias boards attached directly to the microcircuit packages:

• The bias boards for A12 through A14 contain factory adjusted or factory selected components, and cannot be separately replaced. If a bias board component (e.g. protection diode or transistor) has been externally damaged, it is acceptable (and economical) to replace that individual component. However, a bias board failure often indicates a failure inside the microcircuit and may require that the entire assembly be replaced.

#### WARNING

Many microcircuits are extremely sensistive to static electric discharges (more so when the microcircuits are removed from their bias boards or control circuits).

Before handling a microcircuit, discharge your own body by touching the instrument chassis or microcircuit package. Avoid touching the center conductors of the RF connectors and bias feed-throughs at all times.

Microcircuits should be stored and transported in staticprotective packaging. Never package microcircuits with styrofoam, cellophane (unless treated for static), or adhesive

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Do not attempt to test any microalraults, at a bins fendthrough or the RF connectors, with an ohumater. Resistence mousurements are rarely useful, and will often destroy a working microcircuit. Mensure DC voltages at the bins foodthroughs with a high-impedance DC voltmeter only with blas or control connections intact.

The following troubleshooting procedure traces power levels through the RF path. RF measurements should be made with a high-frequency spectrum analyzer or an RF power meter. A type-N female to SMA adapter, along with a short flexible RF cable terminated at both ends with SMA male connectors, will make troubleshooting easier.

Breaking RF connections within the ALC loop will cause the loop to go unleveled, producing abnormally high power levels (up to +20 dBm) and harmonic destortion. In Bands 1 through 3, the ALC loop includes connections between A6 Mod/Coupler and DC2 Directional Coupler. (Figure 8-24, within the A4 Troubleshooting section, provides a graphic definition of the loop.) If necessary, the modulators may be externally blased using the Open Loop Procedure described in the A4 Troubleshooting Section. If possible, avoid breaking the ALC loop to make RF measurements. In any case, It is a good idea to begin troubleshooting just outside the ALC loop.

#### Failure Symptoms

The information below should be used to help systematically troubleshoot to the individual RF assembly. Based on the failure symptom, the components most likely to have failed are listed, with the most probable failure cited first Hints for ensuring that the RF Path is actually responsible for the failure are also given. For troubleshooting information related to a specific assembly, refer to Microcircuit Verification By Assembly below.

#### NOTE

All references to test points, pin connections, etc., can be locuted on the RF Schematic.

NO RF POWER - All Bands

• A13 YIG OSCILLATOR. A YO failure is indicated if the RF power at the rear panel AUX OUTPUT connector is less than +10 dBm (nominally 0 dBm). Check power supplies and bias levels, L RF ON (TP-"ON") should be at -10 Vde. TP "G" should be approximately -2 Vde. Check TP "M" for the waveform entitled YO COIL, Figure 8-70, within the A8 Service Sheet. This waveform represents the current across the main coil. Check the RF output directly at the YO for approximately +14 dBm at several frequencies.

• A16 Modulator/Coupler. A Modulator/Coupler failure is indicated if there is not at least -10 dBm at the rear panel AUX OUTPUT connector. Disconnect PULSE MOD input to AI6AIJ1 to eliminate the possibility of the Pulse Modulation circuit (on the A6 Sweep Control assembly) turning the RF power off. If there is still no RF output power, check the Modulator/Coupler output power at A16J2.

• Al2 Switched YTM. The easiest place to access the Al2 YTM RF output is at the W15 input to DC2 Directional Coupler. Also check the YTM power supplies and bias voltages.

Model 83590A

NO RF POWER - Bands 1--3

• A16 Modulator/Coupler. Remove the A4 assembly. This removes all bias current from the modulator and provides an unrestricted path for RF. If full unleveled power is achieved, refer to A4 Troubleshooting. If Bands 1–3 remain dead, disconnect W20 and check the RF output directly out of A16 (open loop power should measure approximately ±9 dBm).

• Al4 Power Amplifier. Check power supplies. Verify that L AMP OFJis a logic high (it is pulled high on AHA1 and is a no-connection on the Al0 Motherboard). The easiest place to access the Al4 output power is at the output of the AT1 Isolator (approximately ±26 dBm). If there is no power at this point check the power directly at the Al4 output

• A12 Switched YTM. Verify the PIN SW control voltage (A6TP6) is -5V for Bands 1-3. The easiest place to access the YTM RF output is at the W15 input to DC2 Directional Coupler.

#### MAXIMUM RF UNLEVELED POWER - All Bands

Refer to this symptom under A4 Troubleshooting.

#### MAXIMUM UNLEVELED RF POWER -- Bands 1-3

• CRI DETECTOR. Select a CW frequency in Band 1 and check for maximum unleveled RF output power. Check the output of CRI for approximately -0.05 Vdc, using an SMC tee or by probing A4P1-20.

• A16 Modulator/Coupler. If CR1 will output about -0.05 Vdc, check that A4TP6 is at  $\pm 4$  Vdc. If not troubleshoot A4. Then check MOD 1. It should be slightly negative. If it is approximately  $\pm 4$  Vdc the modulator diode is open. If MOD 1 is near 0.0 Vdc while A4TP6 measures  $\pm 4$  Vdc, check A4 Mod Drivers and the connections to the modulator.

#### HARMONIC DISTORTION - All Bands

• A13 YIG OSCII LATOR. Refer to Section V. Adjustments, and perform the harmonic adjustments. If harmonics are still unacceptable in all bands check the spectral purity of the YO output. If harmonics are less than 14 dB below the fundamental, replace A13.

#### HARMONIC DISTORTION - Bands 1-3

• Al4 Power Amplifier. Check power supplies and biases. Check power levels into Al4. Measuring power or spectral content into or out of Al4 will break the ALC loop and cause distortion even without a failure. Refer to A4 Troubleshooting and perform the Open Loop Procedure. This procedure externally biases the modulators to level RF power while the ALC loop is open.

#### POWER DROP-OUTS - Any Band

• A13 YIG OSCILLATOR. If power is present and leveled across part of a band, but drops out entirely for the rest of the band, suspect A13. Check for power dropouts at the rear panel AUX OUTPUT connector.

POWER HOLE - Any Band

• Check all RF connections in the proper loop(s). Narros-band power dips or "holes" are usually the result of loose or faulty R⁺ -connections. Tighten all RF connectors internally. Secure the front-panel RF connection, inspect the front-panel RF connector for damage or wear, and clean or replace parts as necessary. Section VI, Replaceable Parts, provides an exploded view of this connector.

DC BIAS AT RF OUTPUT

• A12 Switched YTM. The YTM provides the DC blocking function for the 83590A output port. If a DC bias exists at the front-panel connector, the failure is almost certainly in A12.

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Service

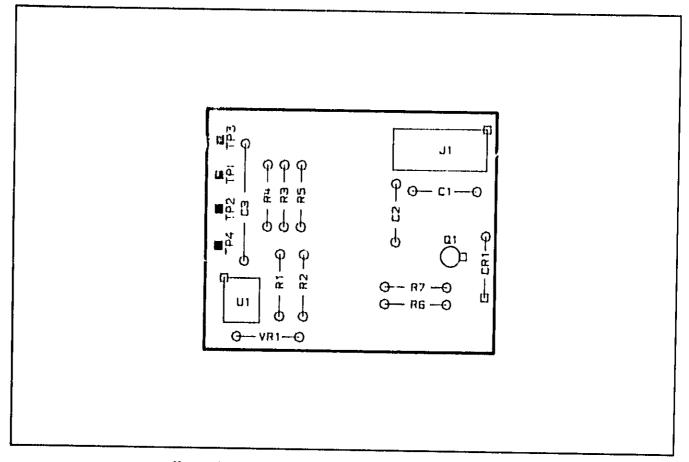


Figure 8-72, AI2AI YTM Bias, Component Locations

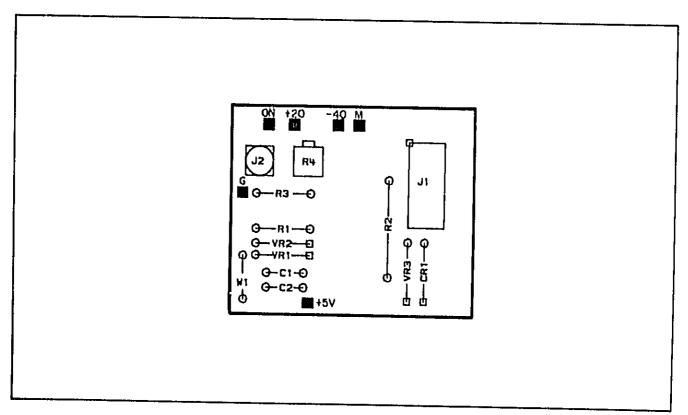


Figure 8-73. A13A1 YO Blas, Component Locations

Service

Model 83590A

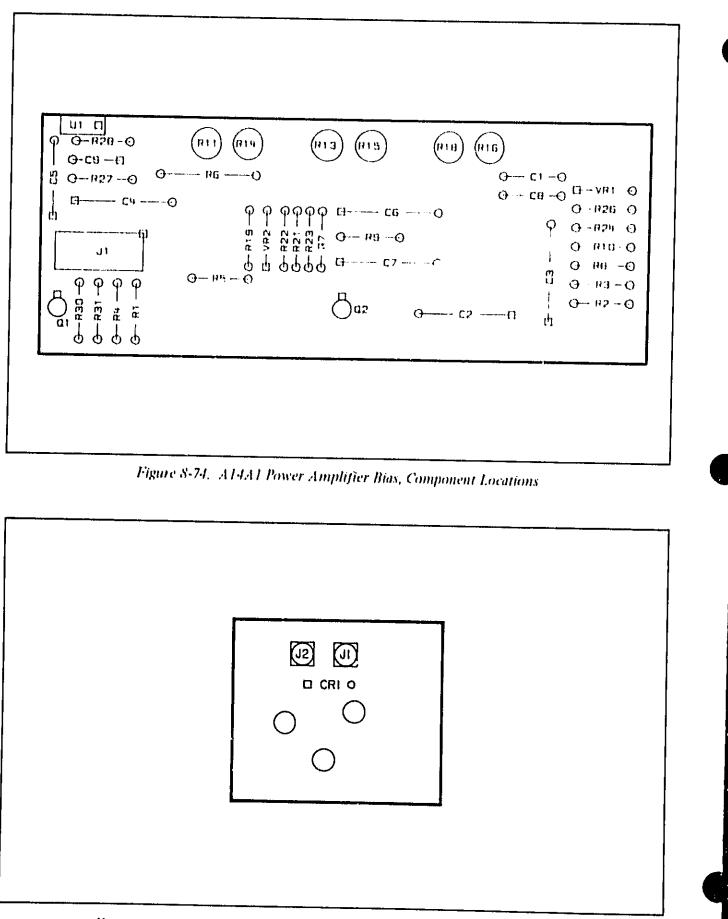
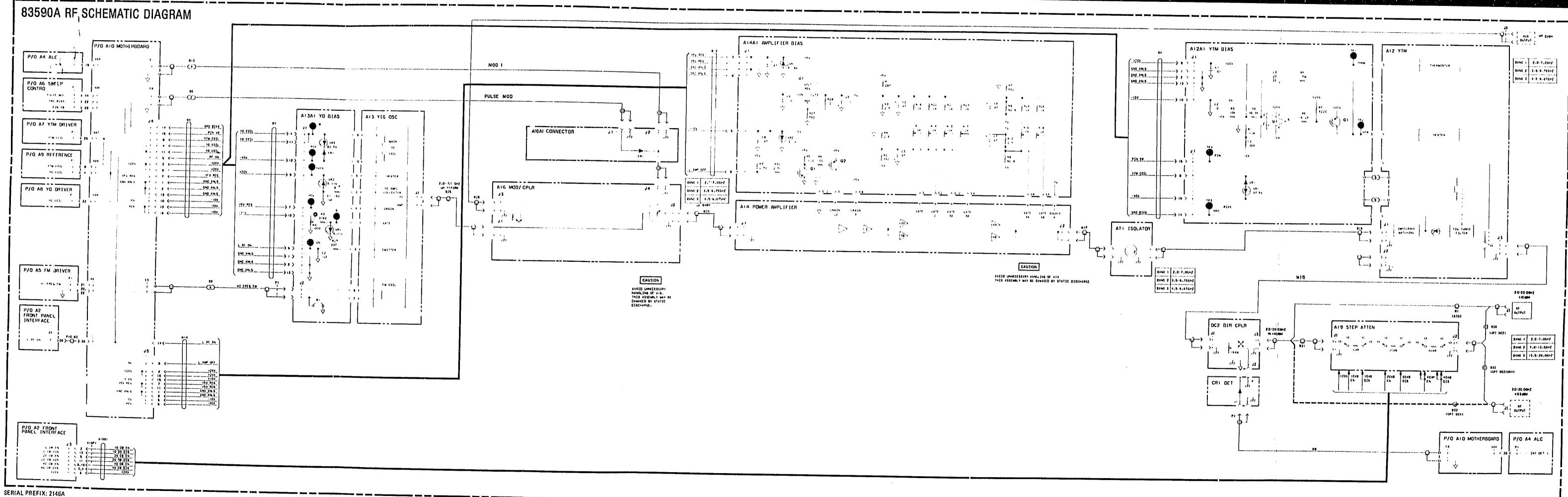
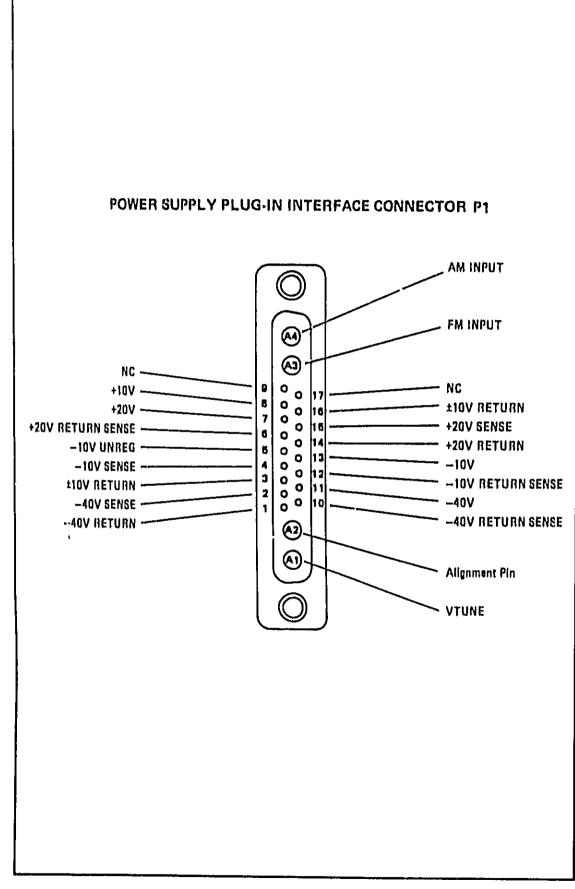


Figure 8-75. A16A1 Modulator/Coupler Connector, Component Locations



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Figure 8-76. RF Schematic Diagram



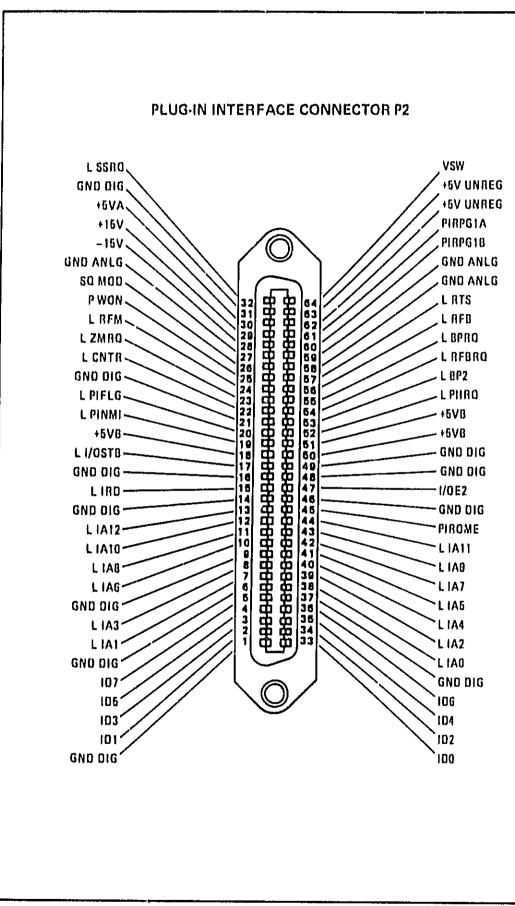


Figure 8-77. Interface Signals on Connector P1

Figure 8-78. Interface Signals on Connector P2

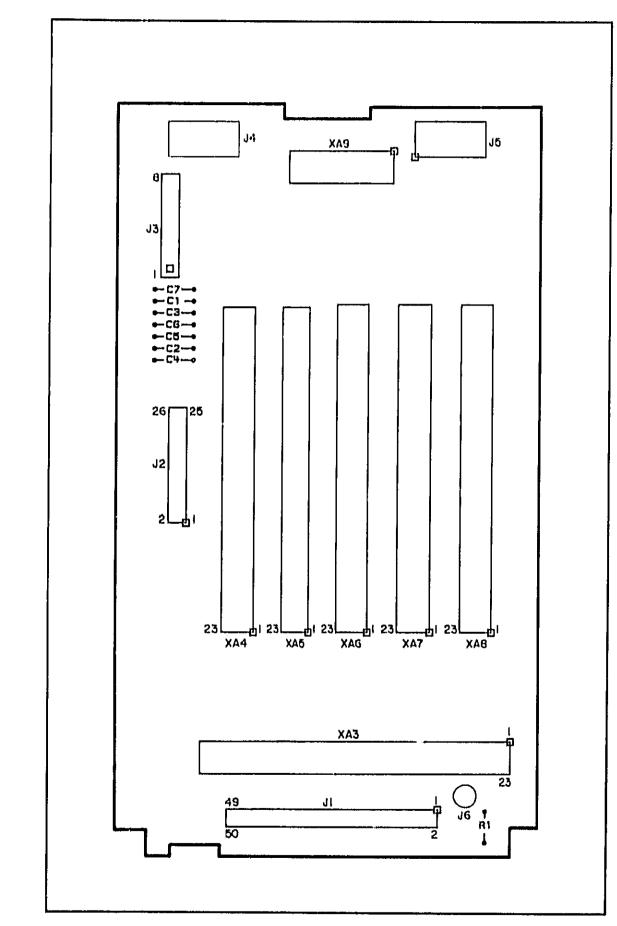


Figure 8-79. A10 Motherboard, Component Locations

Mnemonic	Signal Source	Mnemonic	Power Supply	₽lug-in	Digir	terface			Sweep			Ref	F,P,	7/0 Plug-in	Power	YO/YTM	RF	
	bource	Description	Interface P1	Interface P2	A3P1	A3J1	ALC A4P1	FM A5P1		YTM A7P1	YO ABP1	Resistor AUP1	Interface A10J1	Interface A10J2	Supply Interface A10J3	Ribbon Cable A10 J5	Ribbon Cable A10J4	Miscellaneous
AM L AMP OFF BAND 0 AMP	P1+A4 None A6P1+19	Amplitude Modulation L=Amplifier Off (Not Used) Band 0 RF Amplifier Enable	A4-C				4		10								B	E2.C ¹
BA0 BA1 BA2 BA3	A3P1-33 A3P1-11 A3P1-34 A3P1-12	Bullered Addr Ø Bullered Addr 1 Bullered Addr 2 Bullered Addr 3			33 11 34 12		11 11 34 12	33 11 34 12	33 11 34 12	33 11 34 12	33 11 34 12		11				7	
BD9 BD1 BD2 BD3	A3P1-31 A3P1-0 A3P1-32 A3P1-10	Buffered Data 9 Buffered Data 1 Buffered Data 2 Buffered Data 3			31 9 32 10		31 9 32 10	31 0 32 10	31 9 32 10	31 9 32 10	31 8 32 10		5 3 7 9					
BD4 BO5 BD6 BD7	A3P1-35 A3P1-13 A3P1-36 A3P1-14	Buffered Data 4 Buffered Data 5 Buffered Data 6 Buffered Data 7			35 13 36 14		35 13 36 14	35 13 36 14	36 13 36 14	36 13 36 14	35 13 36 14		15 13 19 17					
L BPAQ L BP2 BVTUNE L CNTA	AGP1-2 P2-53 AGP1-42 P2-22	L=Blanking Pulse Request L=Blanking Pulse Buffered Tune Vollage L=Counter Trigger (Not Used)		63 22	44	42			2 15 42	25	25		49	A				
EXT DET EXT DET RET EXT CAL	A10J6 A10J6 A10J1-41	External Leveling Input External Leveling Return External Leveling Power Cal					23 1 24						41					J6⋅C ¹ J6⋅S ²
FLAG	A10J1-31	Front Panel Flag			42	t-							31		<u></u>	<u> </u>	<u> </u>	·
FM IN FM IN RET	P1	Frequency Modulation Input Frequency Modulation Return	A3.C ¹ A3.S ²						40 39, 41									E3·C ¹ E3·S ²

¹ Coaxial Cable

2 Shielded Cable

* Not used on this assembly

Table 8-15, 83590A Motherboard Wiring List (1 of 5) 8-77

	Signal		Power Supply	Plug-in	Dig Ir	sterface			Sweep					P/O	Power	YO/YTM	RF	
Mnemonic	Source	Mnemonic Description	Interface P1	Interface P2	A3P1	A311	ALC A4PT	FM A5P1	Control AGP1	<u>ҮТ:М</u> А7Р1	YO	Ref Resistor A9P1	F.P. Interface	Plug-in Interface	Supply Interface	Ribbon Cable	Ribbon Cable	
L FP1 L FP2 L FP3 L FP4 L FP5	AJP1-16 AJP1-37 A3P1-16 AJP1-26 AJP1-30	L+F.P. Display Write L+F.P. Keyboard Read L+F.P. Annunciator Write L+F.P. Annunciator Write L+F.P. RF Control			15 37 16 26 30							AUPT	A 10J1 21 23 25 6	A 10J2	A10J3	A 10J5	A 10J4	Miscellanak
FREG CAL FREG TRK V	A10J1-37 A10J1-36	Band O Freq Cal Freq Tracking Voltage					26	24			23		37					
HI FREQ FM HI FREQ FM RET	A5P1-21 A6P1-20,22	YO FM Call Drive YO FM Call Return						21					36					
L IA0 L IA1 L IA2 L IA3	P2-38 P2-7 P2-39 P2-8	Instr Bus – Inv Addr ð Instr Bus – Inv Addr 1 Instr Bus – Inv Addr 2 Instr Bus – Inv Addr 3		38 7 30 8		12 13 14 15		20,22										E6-C ¹ E6-S ²
- 1A4 - 1A5 - 1A6 - 1A7 - 1A8	P2:40 P2:41 P2:10 P2:42 P2:11	Instr Bus – Inv Addr 4 Instr Bus – Inv Addr 5 Instr Bus – Inv Addr 6 Instr Bus – Inv Addr 7 Instr Bus – Inv Addr 8		40 41 10 42 11		16 18 19 20 21												
IA0 IA10 IA11 IA12	P2-43 P2-12 P2-44 P2-13	Instr Bus – Inv Addr 9 Instr Bus – Inv Addr 10 Instr Bus – Inv Addr 11 Instr Bus – Inv Addr 11 Instr Bus – Inv Addr 12		43 12 44 13		22 23 24 26												<u> </u>
0 1 2 3	P2-2 P2-34	Instr Bus – Data O Instr Bus – Data 1 Instr Bus – Data 2 Instr Bus – Data 3		33 2 34 3		2 3 4 6												
4 5 5 7	P2-4 P2-36	Instr Bus Dato 4 Instr Bus Dato 5 Instr Bus Dato 6 Instr Bus Dato 7		35 4 36 5		6 7 8 9												

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¹ Coaxial Cable ² Shielded Cable

Table 8-15, 83590A Motherboard Wiring List (2 c * 5) 8-78

	<b>_</b>		Po <del>wa</del> Supply	Plug-in	Dig In	lertace			Sweep			<b>P-4</b>		P/O	Power	YO/YTM	RF	<u> </u>
Mnemonia	Bigisal Bostace	Mnomunic Doscription	linterface P3	Interface P2	A3P1	1 LEA	ALC A4P1	FM A6P1	Control AGP1	YTM A7P1	YO ABP1	Redutor A0P1	F.P. Interface A10J1	Plug-in Interface A 10J2	Supply Interface A10J3	Ribbon Cable A1035	Ribbon Cable ATC 14	
1. INST1 1. INST2	A3P1-8 A3P4-29	L=Plug in Cantrol L=Plug in Control			11 20	·	10	6	10	18	113							Miscellaneous
INT DET 0 INT DET 1 INT DET HET	J4-h CI11 CI11	Band D RF Datactor (NDT USED) Band 1 RF Datactor Band 1 RF Datactor Band 1 RF Datactor Saturn					21 20 42								·			E4-C ¹ E6-C ¹
140 E9 1, 1708TB 1, 1810	P2:47 P2:17 P2:16	Plug-In 170 Enable Inv 170 Strabe L=Inste Rus Anact		47 17 15		00 03 20												E6.5 ²
MOD D MOD 1 MOD DHIVE	A4P1-44 A4P1-10 A4P1-22	Band D RF Modulation (NOT UGED) Bands 1 – 3 RF Modulation Modulator Drive (Nos Used)					44 19 22		0								16	E1-C ¹
L PIFLO L PINO L PINMI PIN SW PIROME PIROM PINOB	A3A10J1-40 (NG) A6P1-20 P2-45 A10J1-38	L*Plug-In Flag L=Plug-In Interrupt Request L*Plug-In Non-Maskable Interrupt PIN Diode Switch for YTM Plug-In ROM Enable Plug-In RPG A Plug-In RPG B		20 62 10 45 60 61		30 40 26			70				35 34	14		16		
Pulbe in L Pulbe Pulbe Mod Pwon Pwo Inf Pwo Bw/Comp	ABP1-26 ABP3-44 P2-26 A4P1-0	External Pulse Input L=13F Polse Mod Pulse Modulation Power On Power Level Reference (Not Used) Power Sweep, Level Compensation		25	22		41 J G	23	26 26 44 6				20	7				E9-C ¹ E8
L 8F0 L 8F840 L 8FM L 8FM L 8F0 N 8	A6P1-24 P2-24 A10J3-38	L-ISF Blanking L-ISF Blanking Bequest L-ISF Marker - 10V-ISF On; 0V-ISF Off L-ISP Strobe		56 54 24 57			20		24 40				30	6 2 6 8		6	14	,,

¹Coastal Cable ²Shinhfed Cable

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			Pawer Cupply	Plug-in	Dig In	terface			Sweep			Ref	۴.P.	P/Q Plug-in	Power Supply	YO/YTM Ribbon	RF Ribbon	
Mnemonic	Signat Source	Mnemonic Description	Interface P1	Interface P2	A3P1	ลมเ	ALC A4P1	FM A6P1	Control AGP1	YTM A7P1	YO A8P1	Resistor A9P1	Interface A 10J1	Interface A 10J2	Interface A10J3	Cable A10J5	Cable A10J4	Miscellaneous
SCAN CLK L SIRO	A3P1-38 A6P1-3	F.P. Scan Clock L=Sweep Interrupt Request			38 18				3				27					
SQ MOD	P2-26	Square Modulation (27.8,1.0 kHz)		26			40 ·					<u> </u>						
SRD BIAS L SSRO UNL LMP EN L UNLVL	A0P1-22 A6P1-23 A6P1-16 A4P1-2	Step Recovery Diode Biss L=Stop Sweep Request Unleveleo Lemp Enable L=Unleveled		32			,		22 23 16 4	5	5		4	21		14		
VSW VTUNE VTUNE RET	P2:64 P1:A1 P1:A1	Sweep Voltage Tune Voltage Tune Voltage Return	A1-C ¹ A1-S ²	64				25	20 21				- 12	22				E7.C ¹
YO BASE YO COIL YO COLLECTOR YO LO FM	ABP1-21 ABP1-22 ABP1-20 A6P1-2	YO Current Drive Control YO Coll Current YO Rel Resistor Sense YO Low Freq FM (Main Coil)						2			21 22 20	1 4 2				4,11		E 7.S ²
YTM BASE YTM COIL YTM COLLECTOR YTM DRIVE V YTM LO FM	A7P1-21 A7P1-22 A7P1-20 A7P1-23 A5P1-1	YTM Current Drive Control YTM Coll Current YTM Ref Resistor Sense YTM Drive Voltage YTM Low Frequency FM								21 22 20 23		9 B 10	39			B		
IV/GHz	A10J1-50	1V per GHz Output											50					
-10V REF 20V FREO REF	A8P1-3 A9P1-5	-10V Reference Voltage +20V Frequency Reference Sense					43		39	3	3 44			23				J4'BNC)

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¹Coaxial Cable ²Shielded Cabl<del>e</del> Not used on this assembly

Table 8-15, 83590A Motherboard Wiring List (4 of 5) 8-80

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		······································	Power Supply	Plug-In	Dig	Intfc			6weep			Ref	if,p,	P/O Plug-In	Power Supply	YO/YTM Ribbon	RF Ribbon	
Mnemonia	6ignal Source	Mnemonic Description	Interface P1	Interface P2	A3P1	A3J1	ALC A4P1	FM A6P1	Control AGP1	УТМ А7Р1	YO ABP1	Resistor ABP1	Interface A10J1	Interface A10J2	Interface A10J3	Cable A10J5	Cable A10J4	Miscellaneous
+20V +20V RET +20V RET SENSE +20V SENSE	P1-7 P1-14 P1-6 P1-15	+20V Regulated +20V Return +20V Return Sense +20V Sense	7 14 6 16				16	16		16	16	3,11	42		3 6	3,9	2,10	C7
+15V	P2-29	+16V Regulated		20			30	36	38	30	38			15				C6
+10V +/10V RET	Р1-8 Р1-3	+10V Regulated +/-10V Return	6 3				1	7	7	7	7		46		2		16	Cõ
+6V +6VA +6VB +6V REG +6V REG +6V UNREG	A3P1-6,7 P2-30 P2-18,50,61 A9P1-7 P2-63	+5V Internal for RF Plug-In +5V for 8350A +5V for RF Plug-In +5V Regulated +5V Unregulated		30 18,50,61 63	6,7	35,36,38	27	27	27	27	27	7 12	2	1B,20		7	3,11	C4
-10V -10V RET SENSE -10V SENSE -10V UNREG	P1+13 P1+12 P1-4 P1+5	–10V Regulated –10V Return Sense –10V Sense –10V Unregulated	13 12 4 6				17	17	17	17	17		40		6	10	5	C3
-15V	P2-2B	-15V Regulated		28			28	213	28	26	28			13				C2
-40V -40V RET -40V RET SENSE -40V SENSE	P1-11 P1-1 P1-10 P1-2	-40V Regulated -40V Return -40V Return Sense -40V Sense	11 1 10 2				6,39			6,39	6,30				7	12,16	G	C1
GND ANLG	W28P1-8 P2-27,58,59	Analog Ground					15,37	16,37	37,41 43	15,19, 24,26, 29 37	16,19, 24,26, 20,37	G	413	10,11, 12,24	ß	1,2 13	1,9	C1-C7, R1
GND DIG	P2-1,6,14, 16,21,31, 37,46,48 49	Digital Ground		1,6,14, 16,21,31, 37,46,46, 49	4,6		8,30	8,30	8,30	8,30	8,30		8					R1
GND SENSE	W28P1+4	Analog Ground Sense	1											·····	4			

¹ Coaxial Cable

2 Shielded Cable

* Not used on this assembly

## Table 8-15. 83590A Motherboard Wiring List (5 of 5)

Cable Description Connections Cable Description WI Cable Assembly, Rigid, RF, RF Out DC2 Directional Coupler WIR Not Assigned н Front Panel RF Output (Type N) ₩2 Cable Assembly, Coax, Blue 12 Front Panel EXT/MTR ALC Input W19 Not Assigned V1010 Motherboard ₩3 Cable Assembly, Ribbon, Front Panel A1011 Motherboard W20 Cable Assembly, Rigid, RI A211 Front Panel W4 Cable Assembly, Ribbon, RF Section A10J4 Motherboard W21 Not Assigned A12 YTM A13 YO W22 Not Assigned ₩5 Cable Assembly, Coax, White, Pulse In ]4 Rear Panel BNC (Pulse In) A10E9 Motherboard W23 Not Assigned W6 Cable Assembly, Coax, Red, Pulse Mod A10E8 Motherhoard A16 Modulator/Coupler W24 Not Assigned Cable Assembly, Coax, Orange, Viune ₩7 PIAL Rear Panel Interface A10E7 Motherboard W25 Cable Assembly, Rigid, RI W8 Cable Assembly, Coax, Gray CRI Detector (Bands 1-3) A10E6 Motherboard W26 Cable Assembly, Rigid, RI ₩9 Cable Assembly, Coax, Blue, FM A10E5 Motherboard A12A1J2 YO (FM Coil) W27 Not Assigned W10 Not Assigned WH Cable Assembly, Coax, Green, FM In ATOE3 Motherboard W12 Cable Assembly, Coax, Brown, AM In P1-A4 Rear Panel Interface W28 Cable Assembly, Power Su A10E2 Motherhoard W13 Cable Assembly, Coax, Yellow, Mod 1 ATOET Motherboard W29 Cable Assembly, Ribbon Modulator/Coupler A16 W14 Cable Assembly, Ribbon, RF Section A10J5 Motherboard A14A1JL Power Amplifier (2.0 - 20.0 GHz) W15 Cable Assembly, Rigid, RF A12 YTM DC2 **Directional Coupler** W16 Cable Assembly, Rigid, RF ATT Isolator A12 YTM W17 Cable Assembly, Rigid, RF A14 Power Amplifier (2.0 20.0 GHz) ATI Isolator

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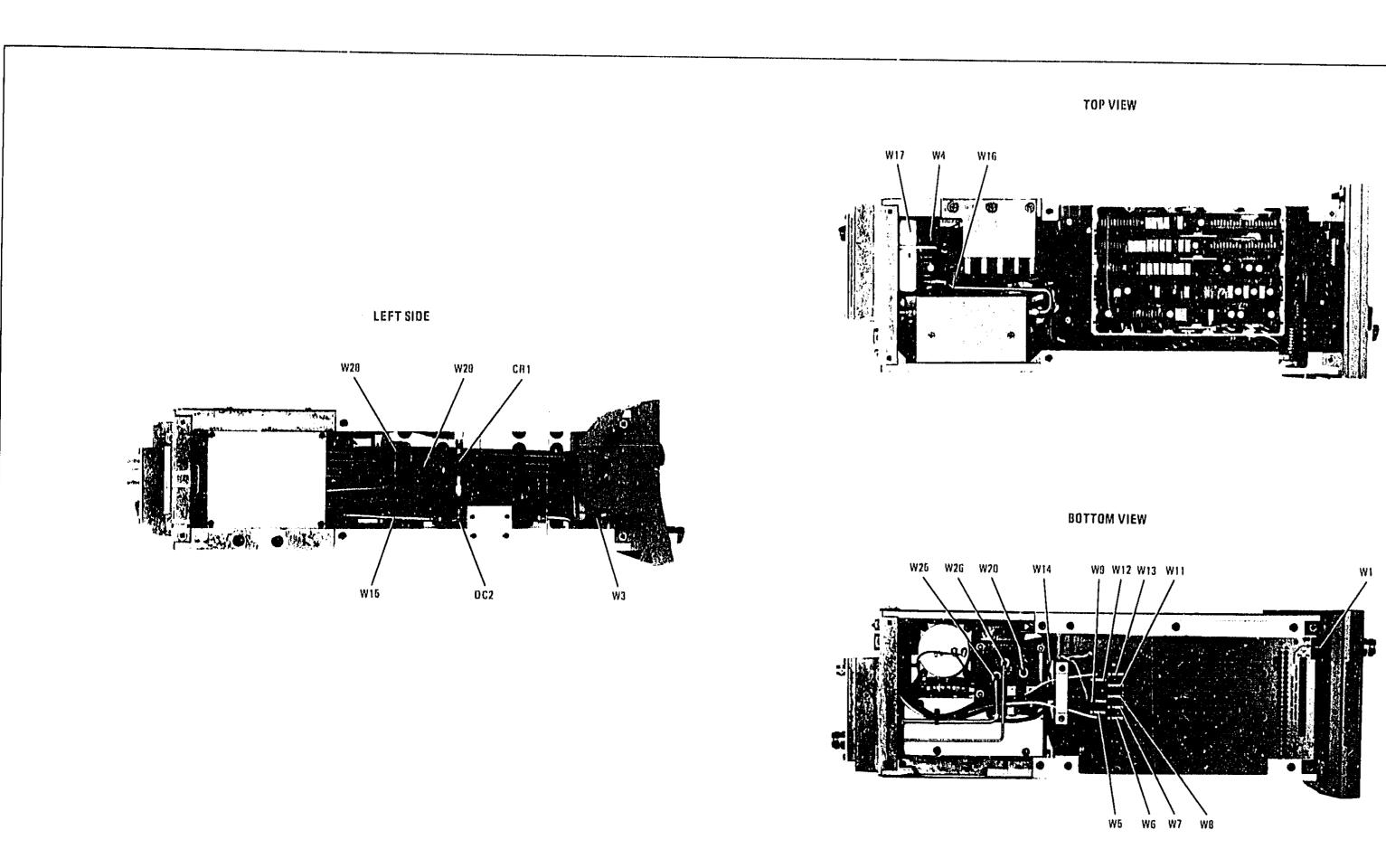
Table 8-16, 4	HP 83590A	Cable List	110	[2]
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Table 8-16.	HP 83590A	Cable	List (2 of 2)
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	Cable	Description		Connections
pe N)	WIR	Not Assigned		
' Input	W19	Not Assigned		
	W20	Cable Assembly, Rigid, RF	A16 A14	Modulator/Coupler Power Amplifler (2.0 – 30.0 GHz)
	W21	Not Assigned		
	W22	Not Assigned		
	W23	Not Assigned		
	W24	Not Assigned		
	W25	Cable Assembly, Rigid, RF	A13 A16	Y0 Modulator/Coupler
	W26	Cable Assembly, Rigid, RF	A   6 J 3	Modulator/Coupler Rear Panel Type N (AUX OUTPUT)
	W27	Not Assigned		
	W28	Cable Assembly, Power Supply	P1 A10J3	Rear Panel Interface Motherhoard
	W29	Cable Assembly, Ribbon	P2 A3J3 A10J2	Rear Panel Interface Dígital Interface Board Motherboard
iHz)			35	Rear Panel BNC (1V/GHz Output)
(Hz)				



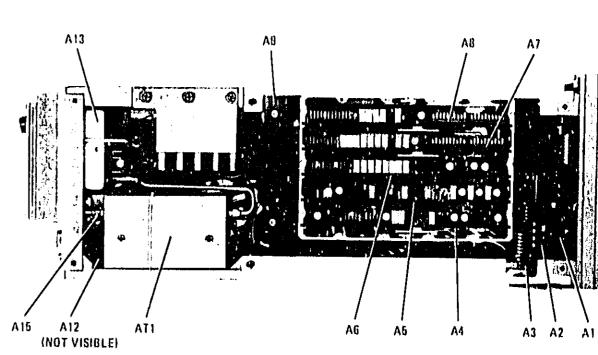
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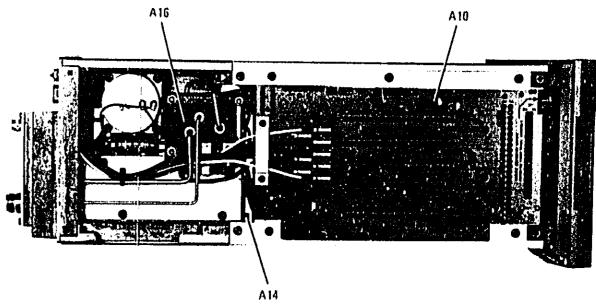
# TOP VIEW A13

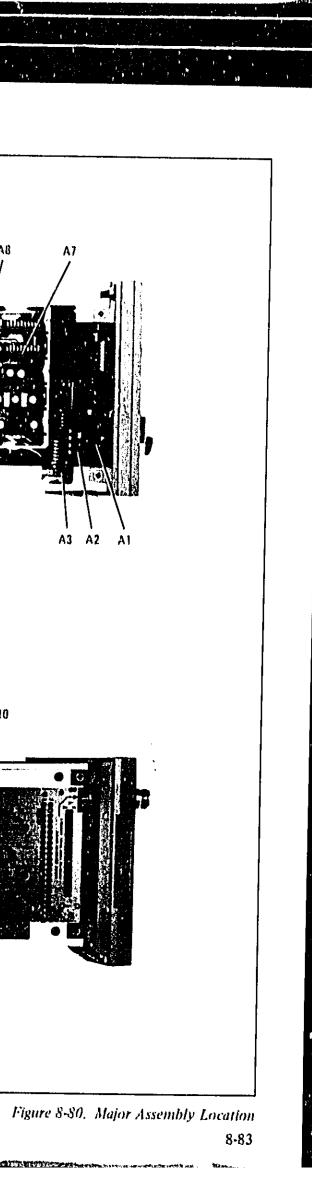
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BOTTOM VIEW





# CHANGES

#### MANUAL CHANGES

MANUAL	<b>IDENTIFICATION</b>
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Manual change supplements are revised as often as necessary to keep manuals as current and accurate as possible. Hewlett-Packard recommends that you periodically request the latest edition of this supplement. Free copies are available from all HP offices. When requesting copies, quote the manual identification information from your supplement, or the model number and print date from the title page of the manual.

NOTE

HP Number: HP 83590A Date Printed: February 1982 Part Number: 83590-90005

This supplement contains important information for correcting manual errors and for adapting the manual to instruments containing improvements made after the printing of the manual.

Two types of information are included:

UPDATES - APPLY TO ALL SERIAL NUMBERS.

N'IMBERED CHANGES - UPDATES THAT ARE SERIAL NUMBER PREFIX RELATED.

The information is in the following order: UPDATES, NUMBERED CHANGES in sequential order with applicable illustrations as close as possible to each numbered change.

To use this supplement, make all UPDATES and all appropriate serial number related CHANGES indicated in the following tables.

NEW ITEM

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NOVEMBER 12, 1986



Printed in U.S.A.

#### 83590-90005



ΗP	83590A	
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Berisl Prefix or Number	Make Manual Changes
2216A	1
2217A	1, 2
2221A	1 - 3
2233A	1 - 4
2234A	1-5
2249A	1-6
2252A	1 - 7
2306A	1 - 8
2313A	1 - 9
2315A	1 - 10
2338A	2-11
2410A	2 - 7, 9 - 12

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Serial Prefix or Number	Make Manual Changes
2411A	2, 3, 5 9 - 14
2412A	2, 3, 5, 9, 11 - 15
2413A	2, 3, 5, 9, 11 - 16
2428A	2, 3, 5, 9, 11 - 17
2451A	2, 3, 5, 9, 11 - 18
2502A	2, 3, 5, 9, 11 - 19
2507A	2, 3, 5, 9, 11 - 20
2519A	2, 3, 5, 9, 11, 13 - 21
2543A	2, 3, 5, 9, 11, 13 - 22
2602A	2, 3, 5, 9, 13 - 23
2619A	2, 3, 5, 9, 13 - 24
2645A	2, 3, 5, 9, 13 - 25



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► - NEW ITEM



Serial Profix Numbor	Chango Number	Assemblies Affected	Now Assombly Part Number	Manual Sacilons Attacted						
2216A	1	A2	83590-60060	Replaceable Parts Service						
2217A	2	N/A	N/A	Replaceable Parts						
2221 A	3	AI, A16	N/A	Replaceable Parts						
2233A	4	A4	N/A	Replaceable Parts						
2234A	5	A16	5086-7395	Replaceable Parts						
2249A	6	A4	N/A	Replaceable Parts Service						
2252A	7	A4	N/A	Replaceable Paris Service						
2306A	8	A6	N/A	Replaceable Parts Service						
2313A	9	N/A	General Information							
2315A	10	A3	83590-60073	Replaceable Parts Service						
2338A	11	A2	£3590-60072	Replaceable Parts Service						
2410A	12	A6	83590-60091	Replaceable Parts Service						
2411A	13 and 14	N/A A4	N/A 8355:1+60077	General Information Operation Performance Tests Adjustments Replaceable Parts Service						
2412A	15	A3	83525-60080	Replaceable Parts Service						
2413A	16	A2 and A7	N/A 83595-60068	Replaceable Parts Service						
2428A	17	A3	N/A	Replaceable Parts						

## Numbered Changes Index

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 ► - NEW ITEM

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Serial Profix Number	Changa Numbar	Assemblies Affected	New Assembly Part Number	Manual Sections Affected
2451A	18	۸7	N/A	Replaceable Parts Service
2502A	19	A10	83595-60078	Replaceable Parts Service
2507A	20	A14	83592-60113	Replaceable Paris Service
2519A	21	A6	83590-60106	Replaceable Paris Service
2543A	22	Mechanical Parts	N/A	Replaceable Parts
2602A	23	A2	83590-60122	General Information Installation Operation Adjustments Replaceable Parts Service
2619A	24	AB	\$3595-60070	Adjustments Replaceable Parts Service
2645A	25	A4	83590-60098	Replaceable Parts Service

## Numbered Changes Index

HP 83590A

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## UPDATES

Inside Cover: Replace the warranty statement with the following warranty statement.

## CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

## WARRANTY

This Hewlett-Packard instrument product is warranted against defects in material and workmanship for a period of one year from date of delivery, or, in the case of certain major component: listed in section six of this Operating and Service manual, for the specifical period. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

## LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER B/ SED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

#### ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

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## UPDATES

Title Page: Delete Option 005.

Page 1-1: After paragraph 1-8 add the following:



## Manufacturer's Declaration

#### NOTE

This is to certify that this product meets the radio frequency interference requirements of Directive FTZ 1046/1984. The German Bundespost has been notified that this equipment was put into circulation and has been granted the right to check the product type for compliance with these requirements.

Note: If test and measurement equipment is operated with unshielded cables and/or used for measurements on open set-ups, the user must insure that under these operating conditions, the radio frequency interference limits are met at the border of his premises.

Model HP 83590A

#### NOTE

Hiermit wird bescheinigt, dass dieses Gerät/System in Übereinstimmung mit den Bestimmungen von Postverfügung 1046/84 funkentstört ist.

Der Deutschen Bundespost wurde das Inverkehrbringen dieses Gerätes/Systems angezeigt und die Berechtigung zur Überprüfung der Serie auf Einhaltung der Bestimmungen eingeräumt.

Zusatzinformation für Mess- und Testgeräte:

Werden Mess- und Testgeräte mit ungeschirmten Kabeln und/oder in offenen Messaufbauten verwendet, so ist vom Betreiber sicherzustellen, dass die Funk-Entstörbestimmungen unter Betriebsbedingungen an seiner Grundstücksgrenze eingehalten werden.

Page 1-2, Table 1-1:

Delete all references to Stability with Time (in a 10-minute period after one-hour warmup).

```
Page 1-5, Table 1-2:
```

Add STABILITY WITH TIME (in a 10-minute period after one hour warmup at the same frequency setting);

2.0 to 7.0: < ± 100 kHz 7.0 to 13.5: < ± 200 kHz 13.5 to 20.0: < ± 300 kHz 2.0 to 20.0: < ± 300 kHz

## Page 1-6, Table 1-2:

Change the PULSE IN characteristics as follows:

```
Pulse in (2.0 to 20.0 GHz)

TTL compatible: Logic high - RF on, Logic low - RF off

Squarewave modulation up to 30 kHz (absolute error for 8755 compatibility up to 2 dB, typically 1 dB)

Rise/Fall Time:

Unleveled: Rise Time 5 μs

Fall Time 5μs

Leveled: Rise Time 7 μs

Settling Time 7 μs

Fall Time 5 μs
```

Page 1-8:

Delete Paragraphs 1-29 and 1-30.

UPDATES

## UPDATES APPLY TO ALL SERIALS

#### 83590-90005

**UPDATES** (Cont'd)

Page 4-2, Section 4-13:

Defet: Table 4-8.

Page 4-16, Table 4-11:

Change the specification for CW Mode (13.5 to 20.0) to ±10 MHz. Page 4-10, Postaph 4-15, SPECIFICATION: Desteral references to Stability with Time (in a 10-minute period after one hour warmup). Page 4-12, Paragraph 4-15: Delete F equency Change with Time (10 minutes). Deletcisteps 6 through 8. Change Residual FM tolerances to: 5 kHz, 7 kHz, 9 kHz. Page 4-30, Table 4-16, Section 4-13: Change 13.5 to 20 GHz Accuracy to ±10 MHz. Change lower and upper limits at 17.0 GHz to 16.99, 17.010.

Change lower and upper limits at 20.0 GHz to 19.99, 20.010. Page 4-35, Table 4-16, Section 4-15: Delete all references to time (10 minutes) specifications.

Change lower and upper limits at 14.0 GHz to 13.99, 14.010.

Page 5-21, Paragraph 5-17: Add [INSTR PRESET] before [RECALL] in step 9. Add [INSTR PRESSET] before [RECALL] in step 14.

After step 15, add the following:

16. On the 83540A/B press [INSTR PRESET] [CW] [5] [0] [MHz]. While observing the frequency counter display. adjust the 83590A FREQ CAL control for 50 MHz.

Page 5-29, Paragraph 5-20:

Replace Paragraph 5-20 on pages 5-29 through 5-32 with 5-20. SLOW SWEEP SYTM TO YO TRACKING (UPDATES) contained in this document.

Page 5-33, Paragraph 5-21: Replace Paragraph 5-21 on pages 5-33 through 5-37 with 5-21. SRD BIAS (UPDATES) contained in this document.

Page 5-51, Paragraph 5-28;

Replace Paragraph 5-28 on pages 5-51 through 5-54 with 5-28. ALC GAIN ADJUSTMENT (UPDATES) contained in this document.

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HP 83590A

## **UPDATES** (Cont'd)

Page 6-2, Paragraph 6-17;

Add the following after paragraph 6-17:

Two Year Warranty and Restored Exchange Parts

The microcircuit parts listed in Table 6.0 are provided with either a two-year warranty from the date of purchase and/or a restored exchange parts program.

A two-year warranty applies to both an original component and to one that is purchased as a replacement part either new or restored through the support life of the instrument. The restored exchange parts program allows a defective component to be exchanged for a factory-restored part which provides a substantial reduction in replacement cost. In addition, if the original component is covered by a two-year warranty, the exchanged component will also have a two-year warranty from the date of purchase. Table 6-0 below identifies the components within the instrument that have a two-year warranty as well as those that are available as restored

Reference Designation	Description	Two-Year Warranty	Restored Exchange Part
A12 A13 A10	Switched YTM YO 2.3 - 6.7 GHz 2 - 7 GHz Power Amp Mod/Coupler	Yes Yes Yes Yes	Yes Yes Yes No

Table 6-0. Two-Year Warranty and Restored Exchange Parts



## Page 6-2, Table 6-1:

Change A12 New Part Number to 83592-60065, Rebuilt Part Number to 83592-60066, Description to Switched

Change A13 New Part Number to 83590-60066, Rebuilt Part Number to 83590-60067, Description to YO 2.0 to

Add A19, New Part Number 83592-60123, Rebuilt Part Number 83592-60124, Description 70dBATTENUATOR

## Page 6-5, Table 6-3;

Change AIRPG1 to HP and Mfr. Part Number 0960-0683, CD 3 (recommended replacement). Change A2J1 to HP and Mfr. Part Number 1251-5926, CD 3 (recommended replacement).

## Page 6-6, Table 6-3:

Change A2R1 to: 2100-3103, CD 5, RESISTOR-TRMR 10K 10% C SIDE-ADJ 17-TRN, 04568, 889PR10K. Change A2U9 to HP and Mfr. Part Number 1826-1186, CD 8 (recommended replacement).

Change A3 to HP and Mfr. Part Number 83525-60080, CD 6, DIGITAL INTERFACE ASSEMBLY (does not include A3UI and A3U2). Change A3J1 to HP and Mfr. Part Number 1251-5926, CD 3 (recommended replacement).

Change A3U1 and A3U2 to A3U1/A3U2 (not separately replaceable), HP and Mfr. Part Number 83590-60074, CD 7, EPROM Replacement Kit (recommended replacement). Change A3U5 to HP and Mfr. Part Number 1820-3093, CD 8 (recommended replacement).

#### Page 6-7, Table 6-3:

Add A3XU1 and A3XU2, HP and Mfr. Part Number 1200-0541, CD 1, SOCKET-IC 24-CONT DIP-SLDR (recommended addition).



## UPDATES APPLY TO ALL SERIALS

## **UPDATES** (Cont'd)

Page 6-9, Table 6-3; Change A4U1 to HP and Mfr. Part Number 1826-1058, Change A4U2 to HP and Mfr. Part Number 1826-1186, CD 8 (recommended replacement). Change A4U9 to HP and Mfr. Part Number 1826-1186, CD 8 (recommended replacement). Change A4VR4 to Part Number 1902-0111, CD 9, DIODE-ZNR IN753A 6.2V 5% DO-7 PD = .4W (recommended replacement). Page 6-14, Table 6-3; Change A6U10 to HP and Mfr. Part Number 1826-1186, CD 8 (recommended replacement). Change A6U11 to HP and Mfr. Part Number 1826-1186 (recommended replacement). Page 6-16, Table 6-3; Change A7U19 to HP and Mfr. Part Number 1826-1349, CD 5 (recommended replacement). Page 6-19, Table 6-3; Change A12 to HP and Mfr. Part Number 03592-60065, CD 8, SWITCHED YIG TUNED MULTIPLIER KIT. Change A12 to HP and Mfr. Part Number 83592-60066, CD 9, EXCHANGE 83592-60065 SWITCHED YTM KIT. Change A13 to HP and Mfr. Part Number 83590-60066, CD 7, OSCILLATOR 2.0-7.0 GHz KIT. Change A13 to HP and Mfr. Part Number 83590-60067, CD 8, EXCHANGE 83590-60066 OSC. KIT. Delete AI3AIC2 (recommended deletion). Page 6-21, Table 6-3; Change A16 to HP and Mfr. Part Number 5086-7395, CD 7 (recommended replacement). Change JI to HP and Mfr. Part Number 5061-5304, CD 2, CONNECTOR ASSY TYPE-N APC-7 DC BLOCK (recommended replacement). Change J3 to HP and Mfr. Part Number 5061-5386, CD 0 (recommended replacement). Delete MP6, KEY CAP-JADE GRAY. Add E3, HP and Mfr. Part Number0960-0055, CD 1, CONNECTOR AND WIRE: RF SHORT. Change MP3 to HP and Mfr. Part Number 83522-20028, CD 5. Page 6-22, Table 6-3; Change W13 to HP Part Number 83592-60014, CD 7. Under Option 002, Option 004, and Option 002 and 004, change both HP and Mfr. Number of W8 to 83592-60012. CD 5. Under OPT. 002 change the following item: Al9 HP and Mfr. Part Number 83592-60123, CD 9, EXCHANGE ATTENUATOR 70 dB (OPT. 002 ONLY). Under OPT. 004change the following items: MPI to HP and Mfr. Part Number 83592-20062, CD 1. W32 to HP and Mfr. Part Number 83590-20024, CD 3. Under OPT. 002 and 004 change the following items: Al9 to HP and Mfr. Part Number 83592-60123, CD 9. MP2 to HP and Mfr. Part Number 83592-20063, CD 2. W33 to HP and Mfr. Part Number 83590-20025, CD 4. Since OPT. 005 is no longer available, delete all references to OPT. 005 and combinations with other options. Specifically, delete titles and parts references associated with OPTION 005, OPTION 002 and 005, OPTION 004 and 005, and OPTION 002, 004, and 005. Page 6-24, Figure 6-1: Delete MP 6. Page 8-31, Figure 8-18 (A1/A2 Schematic): Change A2R1 to 10K. Page 8-57, Figure 8-44: Change the designation of the resistor between U19 and U20 to R32.

## **UPDATES** (Cont'd)

Page 8-69, Figure 8-17: In Block E DELAY COMPENSATION change the value of R17 to 287K.

Page 8-73, Figure 8-73;

Delete AI3AIC2 from the component locations diagram (recommended deletion).

Page 8-75, Figure 8-76:

Delete AI3AIC2 (recommended deletion).

On the male connector to the left of J2, draw a connecting line from the center conductor to the outer conductor (a short) and label E3.

UPDATES

## UPDATES APPLY TO ALL SERIALS

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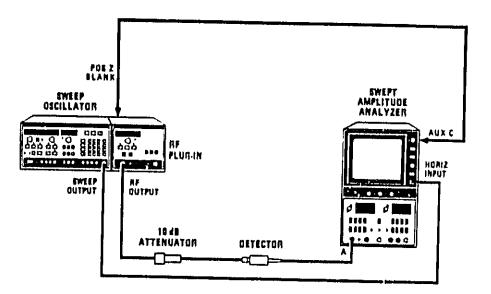
## 5-20. SLOW SWEEP SYTM TO YO TRACKING (UPDATES)

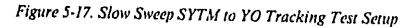
**REFERENCE**:

Performance Test: Paragraph 4-13 Service Sheet: A6 and A7

## DESCRIPTION:

To obtain optimum output power, the Switched Yittrium-Iron-Garnet tuned multiplier (SYTM) passband peaking should track the output of the Yittrium-Iron-Garnet Oscillator (YO). The 83590A is set to sweep Bands 2 and 3 (7 to 20 GHz), and the Automatic Leveling Control (ALC) loop is opened by selecting the External (EXT) ALC MODE. The Step Recovery Diode (SRD) Bias for the SYTM is preset and will be adjusted in Paragraph 5-21. Special calibration modes are used for this procedure (SHIFT 92 for OFFSET and SHIFT 93 for GAIN of the frequency sweep). The output power is peaked for each calibration mode, and the appropriate calibration constant is entered into the calibration switches. A7SI stores the OFF-SET constant, and A7S2 stores the GAIN constant.





## EQUIPMENT:

Swept Amplitude	Analyzer	HD 8755C
mohina mininini		110 10 505
Detector		FIP 1821
10 dB Attenuator		HP 11664B
Swan Ocallinton	Weinschel	Model M9-10
Sweep Oscillator	······································	HP 8350A/B

## **UPDATES APPLY TO ALL SERIALS**

## 5-20. SLOW SWEEP SYTM TO YO TRACKING (UPDATES) (Cont'd)

#### **PROCEDURE:**

#### NOTE

This procedure requires that ASJ1 is set to the factory-set position. Refer to Table 5-6.

## NOTE

During this adjustment, a localized drop in power may occur. This drop in power is due to the SRD being over blased and is called squegging, if squegging occurs in Band 2, adjust A6R68 and R73 to eliminate the squegging and to maximize power across the band. If squegging occurs in Band 3, adjust A6R69 and R74.

- 1. Connect the equipment as shown in Figure 5-17. Allow the equipment to warm up for one hour.
- 2. On the 8350A/B, press [INSTE PRESET] [START] [7] [GHz] [SWEEP TIME] [2] [0] [0] [ms] [ L n MOD]. On the 83590A press [EXT ALC MODE]. The unleveled lamp light should be lit.
- 3. Preset A6R78 (T) one quarter turn from full clockwise position.
- 4. Select 5 dB/DIV display resolution on the 8755C and center the display.
- 5. On the 8350A/B, press [SHIFT] [9] [2] to enable the SYTM OFFSET DAC sub-routine. Using the 83590A POWER control, peak the power in the beginning of Band 2.
- 6. On the 8350A/B, press [SHIFT] [9] [3] to enable the SYTM GAIN DAC sub-routine. Using the 83590A POWER control, peak the power at the end of Band 3. Maximum peaking occurs when the power at the high end of Band 3 has been optimized without the power in other bands dropping out.
- 7. Iterate between steps 5 and 6. SHIFT 92/93 are interactive so the adjustments must be alternated until the best compromise is found.
- 8. Press [SHIFT] [9] [2]. Set A7S1 to the Hex-code on the plug-in display. Press [SHIFT] [9] [3]. Set A7S2 to the Hex-code on the plug-in display.
- 9. Press [INSTR PRESET] on the 8350A/B so that the new calibration data will be entered from the current switch settings.
- 10. On the 8350A/B, press [STOP] [7] [GHz] [ LT MOD] [SWEEP TIME] [4] [0] [0] [ms]. On the 83590A, press [EXT ALC MODE].
- 11. Adjust A7R51 (B1 OFS) to maximize the minimum power points of the Band 1 displayed trace.

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## 5-21. SRD BIAS (UPDATES)

**REFERENCE:** 

Performance Test: Paragraphs 4-17, 4-19 Service Sheet A4 and A6

## DESCRIPTION:

The High Power SRD Bias is set by peaking the 8755C displayed trace with A6R68 (2H) and A6R73 (2L) in Band 2, A6R69 (3H) and A6R74 (3L) in Band 3.

The Low and Mid Power SRD Bias is adjusted by inserting a voltage through a 511 ohm currentlimiting resistor to directly bias the Modulator/Splitter. With the 83590A at maximum RF output, the power supply voltage is increased (minimum voltage 0.5 Vdc, maximum voltage 5.0 Vdc) to set the RF output power just above the 8755C noise floor. Then A6R63 (3HL) is adjusted until minimum sl  $\supset$ e is obtained on the oscilloscope display. The voltage from the power supply is decreased until the lowest part of the trace, on the 8755C display, is 10 dB above the noise floor. Then A6R12 (C) is adjusted to peak the power in Bands 2 and 3. The power supply is then removed.

The 8750A is used to normalize system errors so an accurate measurement of the SYTM fundamental feed through can be made. A low pass filter is then inserted before the detected 8755C input. A comparison between the normalized and low pass inputs are made to determine the SYTM fundamental feed through.

## EQUIPMENT:

Swept Amplitude Analyzer
Display Mainframe
Detectors (2)
Detectors (2)
6 dB Attenuator
10 dB Attenuator
UD Walmah at the three as
511 ohm Resistor
HP 0757-0416

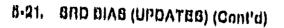
## PROCEDURE:

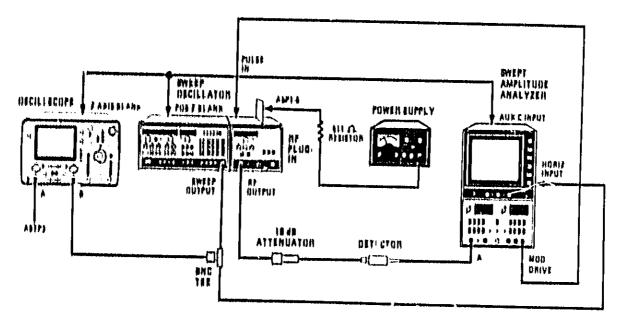
#### NOTE

Turn the 8350A/B LINE power OFF when removing or installing PC boards.

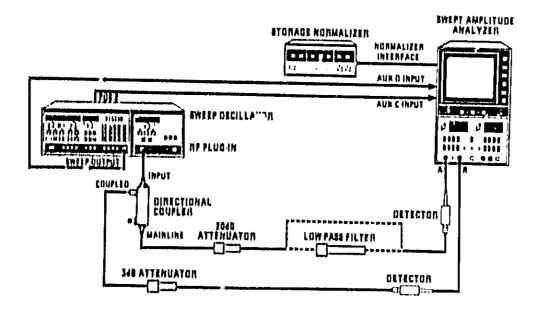
This procedure requires that A3S1 is set to the factory-set position (refer to Table 5-6).

UPDATES





a) Low and Mid Power Test Seinp



b) YTM Fundamental Feedthrough Test Setup

Figure 5-21. St.D Bias Adjustment Test Setups



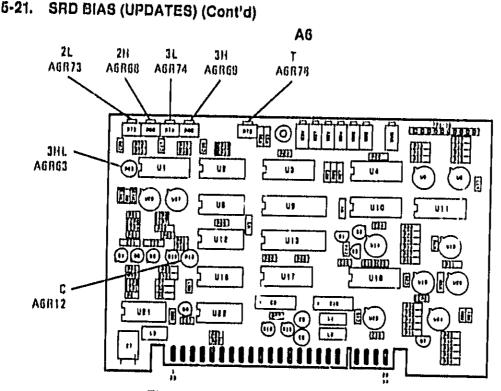


Figure 5-22. SRD Bias Adjustment Locations

## High Power SRD Blas

- 1. Connect the equipment as shown in Figure 5-21a with the 83590A A6 Sweep Control board on an extender. Do not connect the power supply. With the LINE power OFF, remove the 83590A A4 ALC board. Connect the 8755C MODULATOR DRIVE output to the 83590A rear panel PULSE IN connector.
- 2. Allow the equipment to warm up for one hour.
- 3. On the 8350A/B press [INSTR PRESET] [START] [6] [.] [9] [GHz] [STOP] [1] [3] [.] [5] [GHz] [SWEEP TIME] [4] [0] [0] [ms]. On the 83590A select the [EXT ALC MODE].
- 4. Set the 8755C display resolution for 5 dB/DIV and center the display.
- 5. Set up a zero volt reference on the ocilloscope,

## NOTE

BEFORE beginning each adjustment, preset the potentiometer to the point where one side of the trace on the oscilloscope display is below zero volts. Adjustment locations labeled 2L and 3L set the left side of the displayed trace. Adjustment locations labeled 2H and 3H set the right side of the displayed trace. DO NOT preset more than one potentiometer at a time.

- 6. Observe the 8755C display, adjust A6R73 (2L) to peak the power at the low end of Band 2 without the power squegging. Then adjust A6R78 (2H) to peak the rest of the band. Iterate between (2L) and (2H) to peak the power across the band without any squegging.
- 7. On the 8350A/B press [START] [1] [3] [.] [4] [GHz] [STOP] [2] [0] [GHz]. Adjust A6R74 (3L) for the low end of Band 3 and A6R69 (3H) for the test of the band to peak the power without squegging.

UPDATES

## 5-21. SRD BIAS (UPDATES) (Cont'd)

8. Check the SYTM to YO tracking to ensure it has not changed (refer to Paragraph 5-20). If retracking is necessary, repeat the steps ab ve to eliminate any squegging that may have occurred.

Low and Mid Power SRD Blas



# The voltage connected to A6P1-6 is to bias the Modulator/Splitter directly. If A6P1-7 ( + 10Vdc supply) is shorted to A6P1-6, the Modulator/Splitter will be damaged.

- 9. Set up the equipment as shown in Figure 5-21a, with a 511 ohm resist connected to A6P1-6 (reference to ground), Remove the 83590A A4 ALC board, Connect the 8755C Swept Amplitude Analyzer MODULATOR DRIVE output to the 83590A rear-panel PULSE IN connector.
- 10. Allow the equipment to warm up for one hour.
- 11. On the 8350A/B, press [INSTR PRESET] [SWEEP TIME] [2] [0] [0] [ms] [START] [7] [GHZ]. Set the power on the 83590A to 20dB.
- 12. Set the 8755C display resolution for 10 dB/DIV and adjust the display to the top graticule. On the 1740A Oscilloscope, select A vs B, set Channel A to .5 B/DIV, set Channel B to 1 V/ DIV, and DC-couple Channels A and B.
- 13. Set the 6214A voltage to .5 Vdc. Increase the voltage until the highest power point is 10 dB above the n lise floor (DO NOT EXCEED 5 Vdc).
- 14. Monitor A6TP3 with the oscilloscope and adjust A6R63 until minimum slope (flat display) is obtained.
- 15. Decrease the 6214A voltage until the power at the lowest point between 6.9 and 20 GHz is 10 dB above the noise floor.
- 16. Set A6R12 (C) to a centered position and then adjust to peak the power between 6.9 and 20 GHz. Using the voltage source, keep the RF power at or near 10dB above the noise floor, then repeak A6R12 (C). If the power of the sweep drops at any frequency, maximum peaking has been exceeded.
- 17. Repeat step 14 to verify baseline flatness, readjust A6R63 as needed.
- Threshold

#### NOTE

## For this adjustment to be accurate, the attenuator must be in the 0.0dB step. (Opt 002 only)

- 18. On the 8350A/B press [INSTR PRESET]. Set the power level on the 83590A to -5dB.
- 19. Observe the 8755C with a ldB/DIV reference. Preset A6R78 (T) clockwise then adjust A6R78 (T) counter-clockwise until squegging and/or oscillations are eliminated.
- 20. Observe the 8755C trace, increase power slowly to maximum specified power out. If squegging or oscillations reoccur, readjust A6R78 (T) in small increments. If excessive adjustment of A6R78 (T) is required, the SRD bias may be misadjusted.

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## UPDATES APPLY TO ALL SERIALS

UPDATES

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## 5-21. SRD BIAS (UPDATES) (Cont'd)

## SYTM Fundamental Feedthrough

- 21. Set up the equipment as shown in Figure 5-21b without the Low Pass Filter, and with the 83590A A4 ALC board installed.
- 22. Allow the equipment to warm up for one hour.
- 23. On the 8350A/B, press [INSTR PRESET] [START] [0] [GHz] [SWEEP TIME] [2] [0] [0] [0] [ms] [ UT MOD].
- 24. On the 8755C, select A/R DISPLAY and 5 dB/DIV. Center the display.
- 25. On the 8750A, press [SELECT CH 1], and [DISPLAY STORE INPUT]. The display now shows the system error between Channel A and Channel R.
- 26. Press [REFERENCE MEMORY STORE] and then [DISPLAY INPUT-MEM]. The trace on the 8755C should be flat, showing that system errors have been removed. Note the position of the trace and the REFERENCE LEVEL. This will be used as a reference in step 27.
- 27. Install the Low Pass Filter at the location shown in Figure 5-21b.
- 28. Adjust the REFERENCE LEVEL so that the entire trace is on the display. The SYTM fundamental feedthrough is now displayed on the 8755C.
- 29. Determine how many dB the trace is below the reference position established in step 24. If the trace is less than 25dB below the reference between 8 GHz and 20 GHz, repeat paragraph 5-21.

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## 5-28. ALC GAIN ADJUSTMENT (UPDATES)

## NOTE

Complete adjustment of the leveling loop requires several procedures to be performed in the order prescribed, from Paragraph 5-25 through 5-28. Deviation from this routine may cause improper leveling and/or flatness problems.

## **REFERENCE:**

Performance test: 8350A/B Paragraph 4-14. Service Sheet: A4

## **DESCRIPTION:**

A4R15 in the input leg of A4U9 adjusts the gain of the Main ALC Amplifier. A4R15 is adjusted for maximum possible gain without producing oscillations.

## EQUIPMENT

Function Generator	
Function Generator	HP 3312A
Detector 10 dB Attenuaror	HP 8473C
0 dB Attenuator	A Option 010

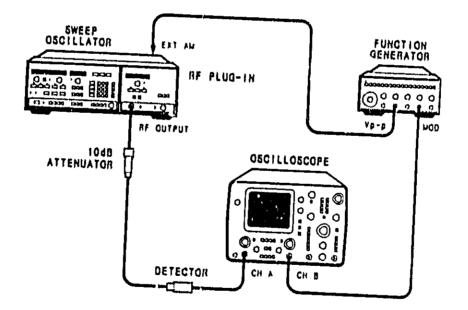
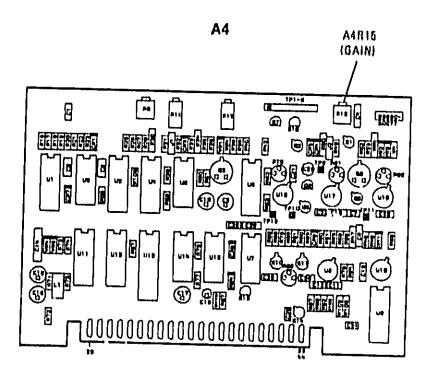


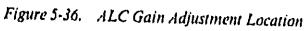
Figure 5-35. ALC Gain Adjustment Test Setup

## 5-28. ALC GAIN ADJUSTMENT (UPDATES) (Cont'd)

## NOTE

This procedure assumes that A3S1 is set to the factory-set position (Table 5-6).





## **PROCEDURE:**

- 1. Connect Vp-p output on HP 3312/ .o 1740 CHANNEL A INPUT.
- 2. Set instrument controls as follows:

## 8350A/B SWEEP OSCILLATOR

START
83590A RF PLUG-IN
POWER LEVEL
MODULATIONSWPMODULATION RANGE Hz (KNOB)0VERNIER0FUNCTION0RANGE Hz (BUTTON)(~)FREQUENCY100KAMPLITUDE5VERNIER1

UPDATES APPLY TO ALL SERIALS

UPDATES

HP 83590A

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## 5-28. ALC GAIN ADJUSTMENT (UPDATES) (Cont'd)

## 1740A OSCILLOSCOPE

MODE																																			,			
CHANNEL A INPUT	•	•••	•	•••		•		•	•	* *	•	1	• •	•	•	•	•	• •	•	•	•	• •	•	٠	•	•	• •	•	,	•	٠	•	• •	Ŋ	47	M	N	
CHANNEL A INPUT CHANNEL A V/DIV		• •	• •	• •	•	• •	•	•	• •	•	•	• 1	• •	,	•	• •	• •	•	٠	•	• •	•	٠	,	• •	•	•	٠	٠	•	• 1	• •	,	•	• •	A	C	
CHANNEL A V/DIV CHANNEL B INPUT	• •	•	• •	٠	• •	• •	•	•	• •	٠	• •	•	•	•	• •	•	•	٠	,	• •	,	÷	÷	•	• •	,	•	•	,	• •	•	•		• •		1/2	V	
DISPLAY	•	• •	٠	• •	٠	۰,	• •	•	•	• •	÷	•	• •	•	,	,	• •			,	• 1	, ,	,	•	,		.,			,	,	•					A	

- 3. Adjust 1740A vertical and horizontal position knobs for waveform at the center of oscilloscope CRT. Adjust START knob, below SWP button, for 10 kHz as displayed on oscilloscope. Turn MODULATION RANGE Hz to 100 and VERNIER to 10K.
- 4. Connect equipment as shown in Figure 5-35.
- 5. On 1740A select A vs B MODE and set CHANNEL A to .005/DIV.
- 6. Adjust the far left side of the signal for 2 divisions pk-pk by using the CAL on the CHANNEL A knob.
- 7. While monitoring CHANNEL A, manually sweep the entire plug-in frequency range and adjust the ALC "GAIN" (A4R15) for 4 divisions of peaking at the plug-in frequency where the highest gain peaking occurs. (See Figure 5-36a)

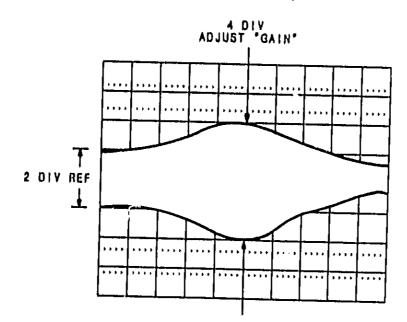


Figure 5-36a. ALC Gain Adjusted Correctly (Worst Case)



## CHANGE 1

This change documents a new Front Panel Interface.

Page 6-5, Table 6-3;

Change A2 to HP and Mfr. Part Number 83590-60060, CD I.

Page 6-6, Table 6-3;

Change A2Q4 to 1854-0477, CD 7, Qty I, TRANSISTOR NPN SI CHIP FT = 1.3 GHZ, 02037, SMCS1005. Add A2R27, 0698-7260, CD 7, RESISTOR 10K 1% .05W F TC =  $0 \pm 100$ , 24546, C3-1/8-TO-1002-G. Add A2R28, 0698-7205, CD 0, Qty I, RESISTOR 51.1 1% .05W F TC =  $0 \pm 100$ , 03292, C3-1/8-TO-51R1-F. Delete A2U11. Add A21113 1820-1199, CD 1, Out 1, IC INW TTL 1.0 Methods and

Add A2U13, 1820-1199, CD I, QIY I, IC INV TTL LS HEX 1-INP, 01698, SN74LS04N.

Page 8-31, Figure 8-12:

Replace the FRONT Component Locations diagram with A2 Front Panel Interface, Component Locations (CHANGE I) from this document.

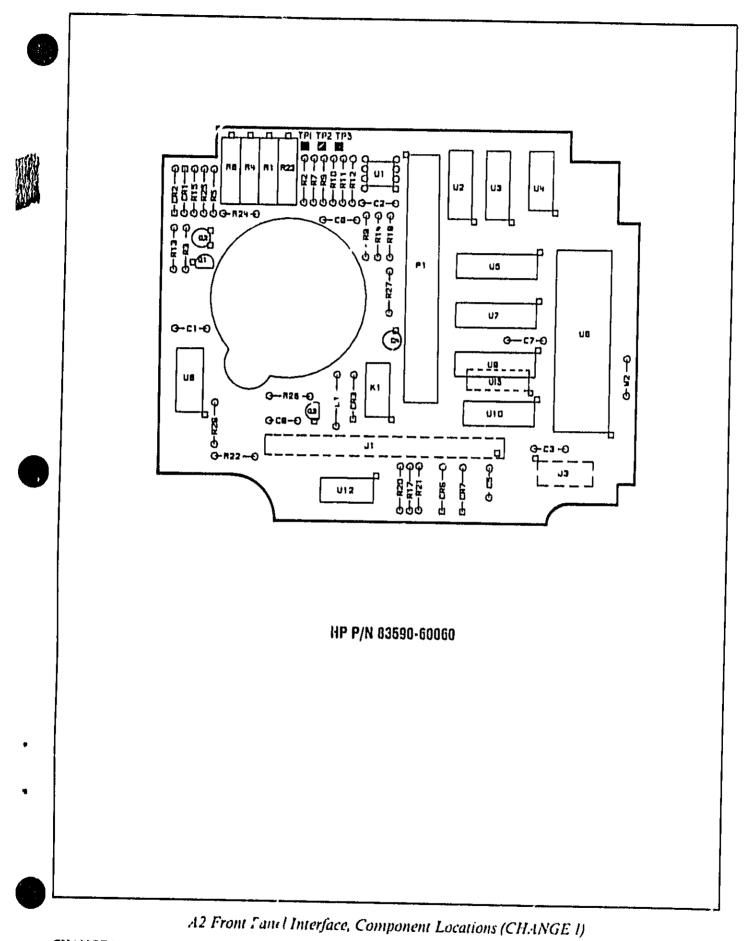
Page 8-31, Figure 8-18:

Change the A2 FRONT PANEL INTERFACE part number in the top left-hand corner of the A2 schematic to 83590-60060.

Change the SERIAL PREFIX in the bottom left-hand corner of the page to 2216A.

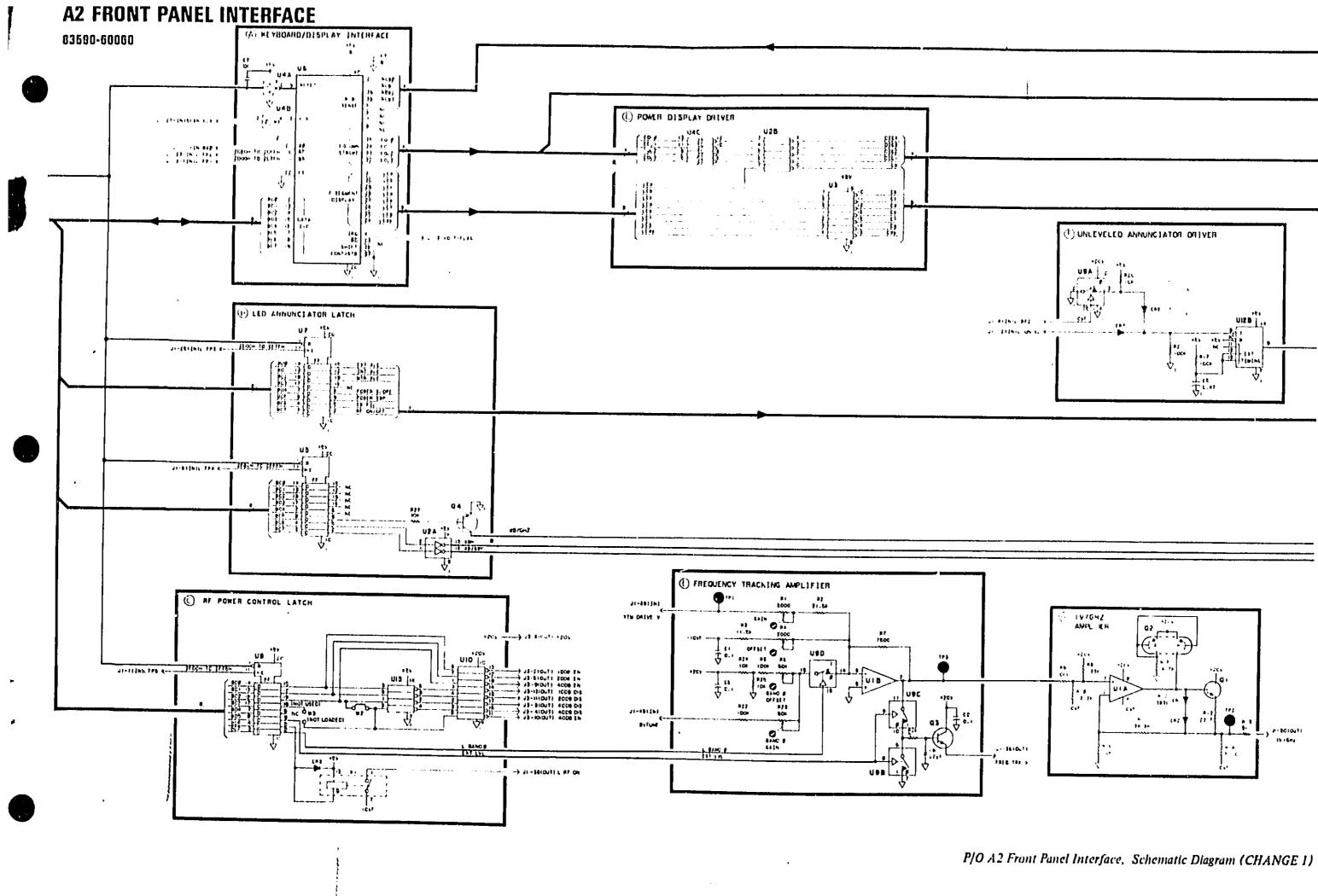
Replace blocks A through G with the partial schematic P/O A2 Front Panel Interface, Schematic Diagram (CHANGE I) from this document.





CHANGE |

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## CHANGE 2

This change documents a new RF output connector.

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Page 6-30, Figure 6-3: Replace Figure 6-3 with Figure 6-3. RF Output Connector (CHANGE 2) from this document.



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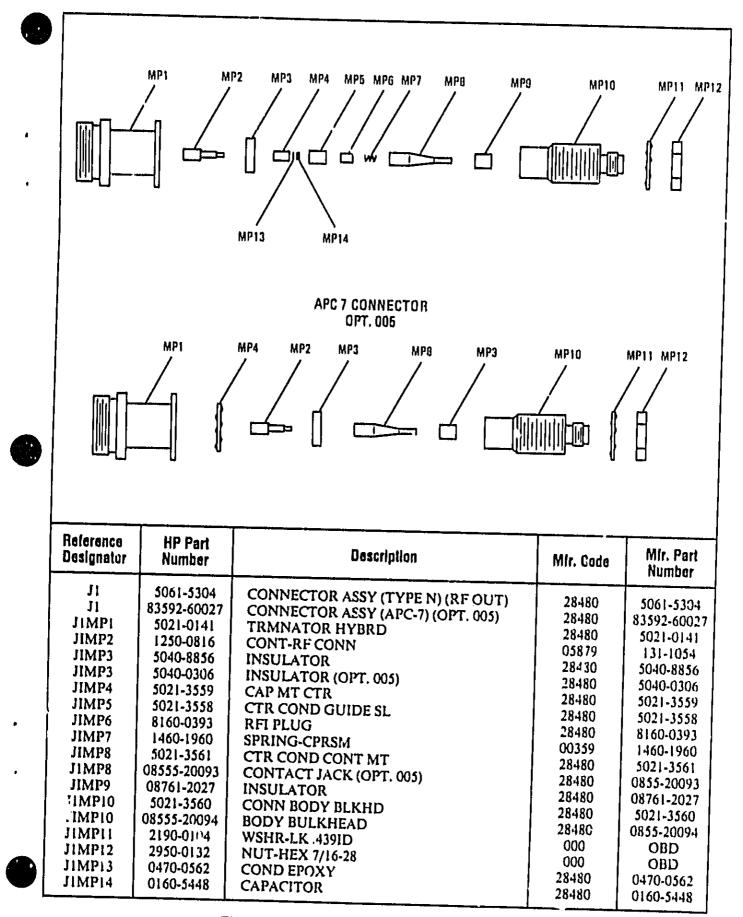


Figure 6-3. RF Output Connector (CHANGE 2)

CHANGE 2



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## **CHANGE 3**

This change documents a new connector on A10 Modulator/Coupler.

- Page 6-5, Table 6-3: Change AIR4 to HP and Mfr. Part Number 2100-4022, CD 0.
- Page 6-21, Table 6-3;
  - Change A16A1J3 to HP and Mfr. Part Number 1251-3172, CD 7, CONNECTOR-SGL CONT SKI.03-IN-BSC-SZ-
  - Delete MP6, KEY CAP-JADE GRAY.



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**CHANGE 3** 

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## OHANGE 4

This change increases the compensation effect of the 1 Hi adjustment in Dand 1.

Page 6-8, Table 6-3;

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Change A4R23 to HP Part Number 0698-3162, CD 0, RESISTOR 46.4K 1% .125W F TC=0±100, Mfr. Part Number C4-1/8-TO-4642-F.

1.5

Change A4R24 to HP Part Number 0698-7262, CD 9, RESISTOR 12.1K 1% .05W F TC=0±100, Mfr. Part Number C3-1/8-TO-1212-F.

## Page 8-47, Figure 8-34:

In Block C POWER LEVEL REFERENCE, change the value of R23 to 46,4K and change the value of R24 to 12.1K. Change the SERIAL PREFIX number in the lower left-hand corner of the page to 2233A.





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## CHANGE 5

This change incorporates on improved Modulator/Coupler.

Page 6-21, Table 6-3: Change A16 HP and Mir. Part Number to 5086-7395, CD 7.



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CHANGE 5

5-1/5-2

## CHANGE 6

## This change modifies the A4 ALC Board to minimize squarewaye overshoot.

Pag: 6-8, Table 6-3;

Change A4R11 to HP Part Number 2100-2521, CD 0, RESISTOR-TRMR 2K 10% Mfr. Code 32997, Mfr. Part Number 3329W-1-202.

Page 6-9;

Change A4R6c to HP Part Number 0098-3132, CD 4, RESISTOR 261 1%, Mfr. Part Number C4-1/8-TO-2610-F. Change A4R71 to A4R71°, FACTORY SELECTED - NOT REPLACEABLE. Change A4R80 to A4R80°, FACTORY SELECTED-NOT REPLACEABLE. Change A4R97 to A4R97°, FACTORY SELECTED-NOT REPLACEABLE.

## Page 8-47, Figure 8-34:

Change the SERIAL PREFIX number in the bottom left-hand corner to 2249A. In Block I MAIN ALC AMP change the value of R66 to 261 and change the value of R11 to 2000. In Block J UNLEVELED SIGNAL change the value of R71 to 2870. In Block K PIN MOD 1 DRIVER change R80 to R80°, value 511; and change R97 to R9/°, value 30.0K.



CHANGES

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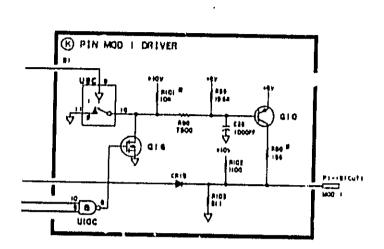
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CHANGE 7 This change adds further improvements to the A4 ALC Board to compensate for modulator variations. Page 6-7, Table 6-3: Change A4C35 to HP Part Number 0160-0574, CD J, CAPACITOR .022µF. Delete A4CR13, Add A4MP4, HP Part Number 1251-1277, CD 9, Qty 3, TERMINAL POST. Page 6-8, Table 6-3: Change A4RII to HP Part Number 2100-2489, CD 9, RESISTOR-TRMR 5K. Page 6-9, Table 6-3; Change A4R66 to HP Part Number 0757-0416, CD 7, RESISTOR 511. Change A4R71 to A4R71*, FACTORY SELECTED-NOT REPLACEABLE. Change A4R89 to HP Part Number 0698-7267, CD 4, RESISTOR 19.6K. Change A4R90 to HP Part Number 0698-7257, CD 2, RESISTOR 7.5K. Delete A4R97. Add A4RI01*, FACTORY SELECTED-NOT REPLACEABLE. Add A4R102, HP Part Number 0757-0424, CD 7, RESISTOR 1.1K 1% .125W F TC = 0 ± 100. Add A4R103, HP Part Number 0757-0394, CD 0, RESISTOR 51.1 1% .125W F TC=0±100. Page 6-13, Table 6-3: Change A6R53 to HP Part Number 0698-3429. CD 2, RESISTOR 19.6. Pege 8-47, Figure 8-29 (A4 Component Locations): Delete R97. Move R98 to a location directly above and parallel to CR15. Move R78 to a location directly below Q15 and Q16 and parallel to R98. Delete CR13 and in its place insert R103. Add R101, mounted on the far side of the board. R101 is located diagonally between the top of R77 and the top of R90. Add R102, mounted on the far side of the board. R102 is located diagonally between the bottom of R80 and a feedthrough pad below Q10 (where the top of R78 was formerly connected). Page 8-47, Figure 8-34 (A4 Schematic): In Block H SAMPLE AND HOLD DRIVER change the value of C35 to .022µF. In Block I MAIL ......CAMP: Change the value of R66 back to 511, Change the value of R11 to 5000, In Block J UNLEVELED SIGNAL change R71 to R71* and change the nominal value back to 2610. Replace Block K.PIN MOD I DRIVER with P/O Figure 8-34, A4 ALC Schem. . . c Diagram (CHANGE 7) from this document. Page 8-57, Figure 8-49 (A6 Sweep Control Schematic): In Block J PULSE MODULATION, change the value of R53 to 19,6,

CHANGE 7

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83590-90005



P/O A4 ALC Schematic Diagram CHANGE 7)

CHANGE 7

## CHANGE 8

This change modifies the A6 Sweep Control Assembly for improved modulator compatibility.

Page 6-12, Table 6-3: Add A6MP3, HP Part Number 0360-0124, CD 3, CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND. Change A6R51 to 0698-7225, CD 4, RESISTOR 348 1% .05W F TC=0±100, 28480, 0698-7225. Page 6-14, Table 6-3: Add A6R83, 0698-7242, CD 5, RESISTOR 1.78K 1% .05W F TC=0±100, 24546, C3-1/8-TO-1780-O. Add A6R84, 0698-7238, CD 9, RESISTOR 1.21K 1% .05W F TC=0±100, 24546, C3-1/8-TO-1210-G. Page 8-57, Figure 8-44; Add F(much 8-44;

Add Figure 8-44A. A6 Component Mounting Diagram (CHANGE 8) from this document.

Page 8-57, Figure 8-49;

Replace Block J PULSE MODULATION with P/O Figure 8-49. A6 Sweep Control Schematic (CHANGE 8) from this document.



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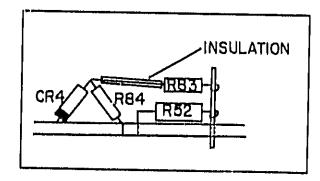


Figure 8-44A. A6 Component Mounting Diagram (CHANGE 8)

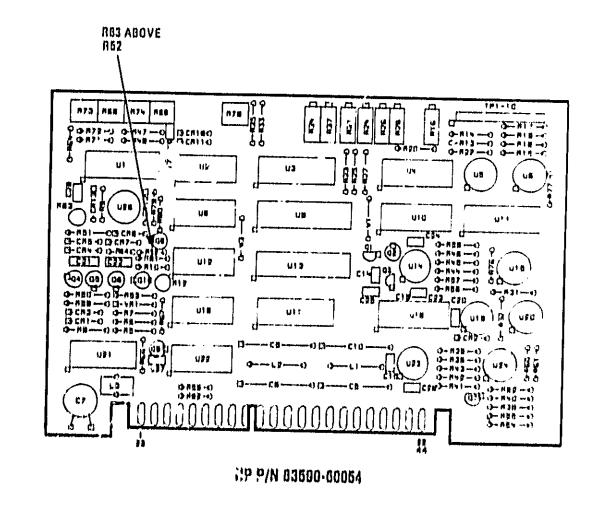


Figure 8-44. A6 Sweep Control Component Locations (CIIANGE 8)

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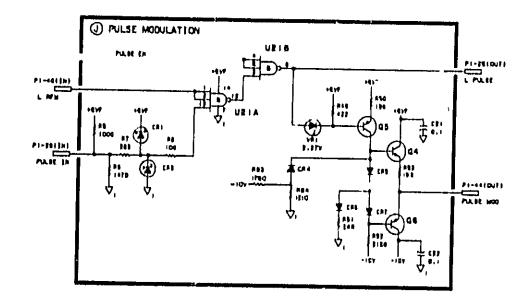
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## HP 83590A

## CHANGE 9

This change improves the output power specifications.

Page 1-2, Table 1-1, POWER OUTPUT: Change the specifications as follows:

Maximum L	oveled Oulput Po	wer:			
2.0 to 7.0 GHz + 10 dBm	7.0 to 13.5 GHz + 10 dBm	13.5 to 18.6 GHz + 10 dBm	13.5 to 20.0 GHz + 10 dBm	2.0 to 10.6 GHz +10 dBm	2.0 to 20 GHz + 10 dBm
With Option	002	<b></b>			
+8.5 dBm	+8 dBm	+8 dBm	+7 dBm	+7 dBm	+7 dBm

Note that the maximum leveled output power for the standard instrument is now +10 dBm across the entire frequency band.



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## CHANGE 10

This change updates the A3 Digital interface Board with revised firmware (Revision 4).

Page 6-6, Table 6-3:

Change A3 Digital Interface Board to HP Mfr. Part Number 83590-60073, CD 6. Change A3U1 to 83590-80003, CD 4, Qty I, EPROM Lw. Change A3U2 to 83590-80004, CD 5, Qty I, EPROM Hi.

## Page 8-35, Figure 8-23:

Change the A3 DIGITAL INTERFACE part number in the top left-hand corner of the schematic to 83590-60073. Change the SERIAL PREFIX in the bottom left-hand corner of the schematic to 2315A.



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## CHANGE 11 (Supersedes CHANGE 1)

This change incorporates a new A2 Sub Panel Board.

- Page 6-5, Table 6-3; Change the A2 Board Assembly Sub Panel part number to 83590-60072, CD 5.
- Page 6-6, Table 6-3: Add A2VRI, 1902-0041, CD 4, DIODE-ZNR 5.11V 5% DO-35 PD-.4W.

## Page 8-31, Figure 8- .2:

Replace the Component Locations Diagram with the A2 Front Panel Interface, Component Locations (CHANGE 11) from this document. Note that U13 is now mounted on the front of the board.

Page 8-31, Figure 8-18;

Change the A2 FRONT PANEL INTERFACE part number in the top left-hand corner of the A2 Schematic to 83590-60072.

Change the SERIAL PREFIX in the bottom left-hand corner of the page to 2338A.

In Block @ (IV/GHz Amplifier) add VRI across R12, anode connected : in 1 of UIA,

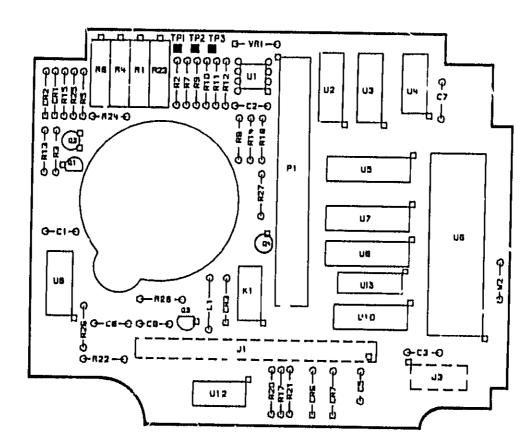
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HP P/N 03590-60072

A2 Front Panel Interface, Component Locations (CHANGE II)

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#### GHANGE 12 (Supersedes CHANGE 8)

This change incorporates a new A6 Sweep Control Board.

Page 6-12, Table 6-3: Change the A6 Sweep Control Assembly HP and Mfr. Number to: 83590-60091, CD 8.

Page 8-57, Figure 8-44 (A6 Component Locations): Replace Figure 8-44 with Figure 8-44 (CHANGE 12) in this change sheet.

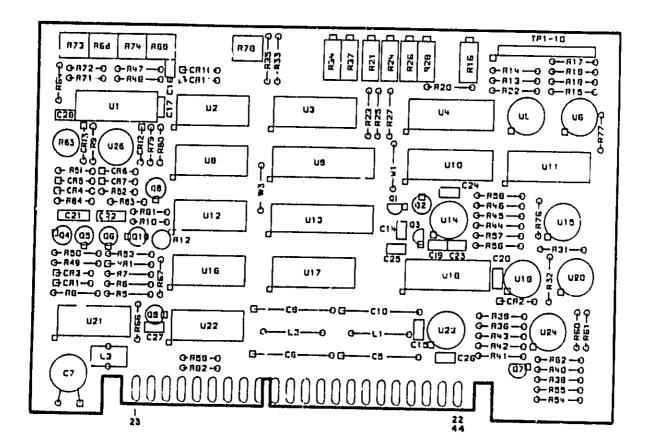
Page 8-57, Figure 8-49 (A6 Schematic):

Change the A6 SWEEP CONTROL part number in the top left-hand corner of the A6 Schematic to 83590-60091. Change the SERIAL PREFIX in the bottom left-hand corner of the page to 2410A.



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HP P/N 83590-60091

Figure 8-44. A6 Sweep Control Component Locations (CHANGE 12)

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Change not applicable.



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#### CHANGE 14

(Supersedes CHANGES 4, 6, and 7)

This change introduces a new ALC board. It is now possible to power meter level the plug-in with the HP 436A and HP 438A as well as the HP 432A.

Page 1-4, Table 1-1, Note 9:

Replace with the following: "Use the HP 432A/B/C, HP 436A, or HP 438A power meters. Both the HP 436A and 438A must be used on the top three (least sensitive) ranges. However, the HP 438A may also be used on the fourth range by programming the response of the power meter's filter as follows: Set the HP 438A to range two, and press [MANFILTER] [1] [ENTER]. See the HP 438A Operating and Service Manual for further instructions. Sweep time 100 seconds for full sweep, typically greater than or equal to 5 seconds per GHz but not less than 10 seconds."

#### Page 1-9, Paragraph 1-42;

Replace the first sentence with the following: "The RF output can be externally leveled using HP Model 432A/B/C, 436A, or 438A power meters or negative polarity output crystal detectors." Delete the note below the paragraph.

#### Page I-II, Table I-4;

Across from the first listed "Power Meter" under Critical Specifications delete: "(No substitute when used for external power meter leveling)." Under Recommended Model add: "HP 436A," "HP 438A."

Across from the first listed "Thermistor Sensor" vivler Recommended Model delete: "HP 8478B" and replace with: "Unit compatible with power meter being used."

Across from the second listed "Thermistor Sensor" under Recommended Model delete: "HP K486" and replace with: "Unit compatible with power meter being used."

#### Page 3-3, Paragraph 3-25;

Add the following: "For power meter leveling (ALC MODE [MTR]), the power meter is used in conjunction with the internal leveling loop. Low frequency variations are handled by the power meter, and high frequency variations are handled by the internal leveling loop."

Page 3-6, Figure 3-4, Number 1: Delete: "(HP 432 only)."

#### Page 3-9, Figure 3-7:

Under EQUIPMENT change the Power Meter listing to: "HP 432A/B/C, 436A, 438A." Change the Thermistor Mount listing to: "Any sensor compatible with the power meter being used."

Under the NOTE delete: "The HP 435 and 436 power meters will not power meter level this plug-in. Only an HP 432 may be used." and add: "When using an HP 436A power meter, enable RANGE HOLD to lock power meter in one range." Under PROCEDURE, number 5, delete all reference to "HP 432A."

#### Page 4-2, Table 4-1:

Across from "Squarewave Symmetry" under 83590A Adjustment add "5-27."

#### Page 4-8, Power Meter Leveling:

Insert "13a. External leveling is shown using the HP 432A, HP 8478B, and HP K486A. However, the HP 432A/ B/C, 436A, 438A meters and compatible sensors may also be used."

#### Page 5-2, Table 5-1:

Change A4R3 to A4R8. Change A4R5 to A4R12. Change A4R8 to A4R10. Delete the line beginning with A4R9. Change A4R11 to A4R15. Under Description, change U11 to U9. Change A4R47 to A4R81. Under Description, change U7-Q6 to U17-Q9. Change A4R56 to A4R82. Under Description, change U5 to U18. Change A4R59 to A4R78. Under Description, change U8-Q1 to U16-Q6. Delete the line beginning with A4R67.

#### CHANGE 14

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CHANGE 14 (Conl'd)	
Page 5-0, Table 5-2; Across from 5-27 under "Adjustments," delete "Power Meter Leveling Calibration" and replace with "Squarewave Symmetry Adjustment (CHANGE 14)."	
Page 5-44, 5-29. ALC Adjustment: Replace pages 5-44 through 5-46 with the 5-25. ALC ADJUSTMENT (CHANGE 14) procedure in this document.	•
Page 5-49, POWER METER LEVELING CALIBRATION: Delete pages 5-49 and 5-50 and replace with 5-27. SQUAREWAVE SYMMETRY ADJUSTMENT (CHANGE 14) procedure in this document.	•
Pages 5-51 to 5-54; ALC GAIN ADJUSTMENT: Replace all reference to A4R11 with A4R15.	
Page 5-51, DESCRIPTION: Change A4U11 to A4U9.	
Page 5-51, EQUIPMENT: Across from "Power Meter," add: "436A, and 438A." Across from both Thermistor Mounts delete: "HP 8478A" and "HP K486," and replace with "Unit compatible with power meter being used."	
<ul> <li>Page 5-54, Paragraph 5-36:</li> <li>Add the following steps:</li> <li>"27. With the Model 83590A set to -5 dBm, press [INSTR PRESET] [GW]. Set the oscilloscope to a 10 us sweep time. If the GAIN control (A4R15) has been over adjusted, the shape of the squarewave on the oscilloscope will be distorted."</li> </ul>	
"28. Back off on A4R15 and observe the squarewave. If the shape of the squarewave improves, back off until there is no more change. If there is no change, in the shape of squarewave as A4R15 is adjusted, return it to its initial position."	
Page 6-7, Table 6-3; Replace the parts list for the A4 Assembly with A4 Replaceable Parts (CHANGE 14) from this document.	
Page 8-19, A4 ALC Assembly: Add the following paragraph at the end of the A4 ALC assembly description: "when used in the ALC MODE [MTR], the A4 ALC assembly uses both the power meter and the internal leveling loop to level the power. Each loop has a separate log amplifier. The output of the "internal" log amplifier is sent through a high pass R-C filter and combined with the output of the power meter log amplifier. This composite signal represents the actual RF power. The power meter leveling loop responds to low frequency variations, while the internal loop responds to high frequency variations."	
Page 8-35, A4 AUTOMATIC LEVELING CONTROL (ALC), CIRCUIT DESCRIPTION: Replace pages 8-35 to 8-46 with the A4 ALC CIRCUIT DESCRIPTION (CHANGE 14) from this document.	
Page 8-47, Figure 8-28: Replace Figure 8-28 with <i>Figure 8-28. A4 ALC Block Diagram (CHANGE 14)</i> from this document. Note this is a fold-out page.	-
Page 8-47, Figure 8-29: Replace Figure 8-29, with Figure 8-29. A4 ALC Component Locations (CHANGE 14) from this document.	

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#### CHANGE 14 (Contd)

#### Page 8-47, Table 8-12:

Replace Table 8-12 with Table 8-12. Leveling Control Lines (CHANGE 14) from this document.

#### Page 8-47, A4PI Pin-out Table:

Replace the A4PI Pin-out Table with A4PI Pin-out Table (CHANGE 14) from this document.

Page 8-47, Figure 8-32:

Under NOTE, change the middle paragraph to read: "Adjustment of the EXT/MTR ALC CAL screw will affect the waveforms at TP8 and TP5. Adjust the CAL screw until the correct waveforms are obtained."

#### Page 8-47, Fig: re 8-33:

Replace Figure 8-33 with Figure 8-33. Open Loop Waveforms (CHANGE 14) from this document.

#### Page 8-47, Figure 8-34;

Replace Figure 8-34 with Figure 8-34. A4 ALC Schematic Diagram (CHANGE 14) from this document. Note this is a fold-out page.



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# 5-25. ALC ADJUSTMENT (CHANGE 14)

#### NOTE

Complete adjustment of the ALC leveling loop requires procedures to be performed in the order prescribed, from Paragraph 5-25 through 5-28. Deviation from this routine may cause improper leveling and/or power variation problems.

#### **REFERENCE:**

Performance Test: Paragraph 4-14. Service Sheet: A4

#### **DESCRIPTION:**

Adjustments compensate for DC offsets in the detected RF path and the Main ALC Amplifier. Power is roughly calibrated and low band flatness is optimized.

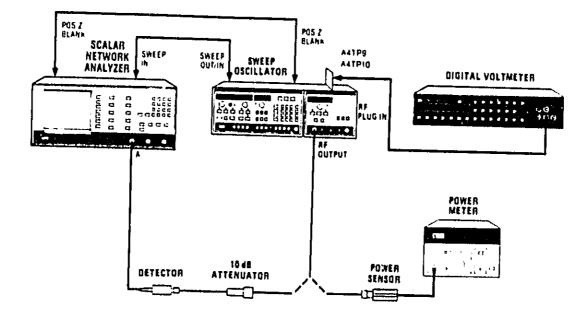


Figure 5-29. ALC Adjustment Test Setup

#### EQUIPMENT:

Digital Voltmeter	
Digital Voltmeter Power Meter Thermistor Mount	HP 3455A
Thermistor Mount	HP 436A
Thermistor Mount Scalar Network Analyzer	HP 8485A
Detector	P 11664B
Sweep Oscillator	
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# 5-26. ALC ADJUSTMENT PROCEDURE (CHANGE 14) (Cont'd)

**PROCEDURE:** 

#### NOTE

# Turn AC power OFF when removing or installing PC boards.

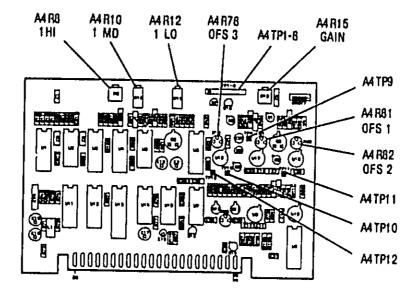
#### NOTE

This procedure assumes that A3S1 is set to the factory-set position (Table 5-6), and that the 8350A/B Sweep Oscillator 27.8 kHz squareways modulation is selected.

1. Remove the A5 FM Driver board. Put the A4 assembly on an extender board. Press [INSTR **PRESET**] [CW]. Sweep the full range of the plug-in at any leveled power. Preset the following adjustments as indicated:

A4R81 (OFS 1)	* * * * * * * * * * * * * * * * * * * *	Midrange
A4R82 (OFS 2)	· · · · · · · · · · · · · · · · · · ·	Midranao
A4R78 (OFS 3)		Midninge
AARIS (GAIN)		Midrange
		Midrange
74K0 (1 HI)	• • • • • • • • • • • • • • • • • • • •	Fully CW

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## 5-25. ALC ADJUSTMENT PROCEDURE (CHANGE 14) (Cont'd)

- Float the ground on the Digital Voltmeter and measure the voltage between A4TP9 and A4TP10. Refer to Figure 5-30 for adjustment locations. Adjust A4R81 (OFS 1) for 0.000 ± 0.001 Vdc.
- 3. Attach a jumper from A4TP11 to ground. Connect the DVM to A4TP4 (reference to ground) and adjust A4R82 (OFS 2) for a DVM reading of 0.000 ± 0.001 Vdc. Remove the jumper.
- 4. Connect the DVM between A4TP12 and A4TP9 (floating ground). Adjust A4R78 (OFS 3) for a DVM reading of 0.000 ± 0.001 Vdc.
- 5. Set the HP 8350A/B LINE power to OFF. Remove the A4 assembly from the extender board and reinsert the A4 assembly directly into the instrument. Set the HP 8350A/B LINE power to ON and press [CW] [2] [.] [0] [GHz 6]. Connect the Power Meter sensor to the HP 83590A RF OUTPUT.
- 6. Set the HP 83590A for a POWER reading of -5 dBm. Adjust A4R12 (1 LO) for an RF output power at the HP 83590A connector of  $-5 \pm 0.1$  dBm.
- 7. Set the HP 83590A for a POWER reading of +7 dBm. Adjust A4R10 (1 MD) for an RF output power at the HP 83590A connector of  $+7 \pm 0.1$  dBm.
- 8. Iterate steps 7 and 8 until both low and midpower ranges are calibrated and no readjustment is necessary.
- 9. Set the HP 83590A for a front panel POWER reading of  $\pm 10 \text{ dBm}$ . Adjust A4R8 (1 HI) for an RF output power at the HP 83590A connector of  $\pm 10 \pm 0.1 \text{ dBm}$ .
- 10. Reinstall the A5 FM board assembly.

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## 5-27. SQUAREWAVE SYMMETRY ADJUSTMENT (CHANGE 14)

#### NOTE

Complete adjustment of the ALC leveling loop requires several procedures to be performed in the order prescribed from paragraphs 5-25 to 5-28. Deviation from this routine may cause improper leveling and/or power variation problems.

Turn AC power OFF when removing or installing PC boards.

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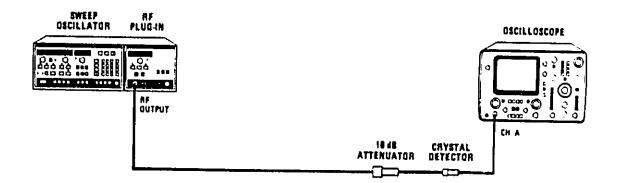
This procedure assumes that A3S1 is set to the factory-set position (Table 5-6).

**REFERENCE:** 

Performance Tests: Paragraph 4-21 Service Sheet: A4

#### DESCRIPTION:

C23 (SYM 1) and R99 (SYM 2) minimize overshoot of the squarewave. R92 adjusts the duty cycle of the squarewave.



## Figure 5-33. Squarewave Symmetry Adjustment Setup

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#### **EQUIPMENT:**

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Sweep Oscillator		0A/B
Uscilloscope	HP1	7403
Didde Delector	· · · · · · · · · · · · · · · · · · ·	473C
Altenuator	HP 8491E	3-010



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# 5-27. SQUAREWAVE SYMMETRY ADJUSTMENT (CHANGE 14) (Cont'd)

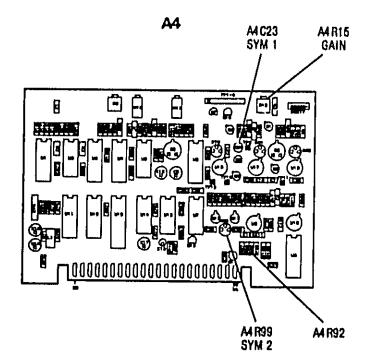


Figure 5-34a. Squarewave Symmetry Adjustment Locations

#### PROCEDURE:

1. Connect the equipment as shown in Figure 5-33, with A4 on an extender board. On the HP 8350A/B, press [INSTR PRESET] [CW] [ I MOD]. Set the RF power level to 0 dBm and allow the equipment to warm up for one hour.

#### NOTE Insure that you do not overdrive the detector as this will distort the squarewave.

- 2. On the oscilloscope, select MAIN SWEEP with a 10µs/DIV time. Set Channel A to .005V/ DIV and Channel B to 1V/DIV.
- 3. Press [CW] [3] [GHz s]. Alternately adjust C23 (SYM 1) and R99 (SYM 2) for the waveform shown in Figure 5-34b.
- 4. Press [CW] [10] [GHz s]. Check that the squarewave resembles that shown in Figure 5-34b. If not, adjust C23 and R99 for best squarewave while alternately checking the squarewave at 3 GHz.
- 5. Repeat step 4 for 15 and 20 GHz. Optimize the shape of the squarewave over the entire range of the plug-in. Naturally there will be slight variations at each end of the plug-in's range.
- 6. With the A4 board on an extender, there may be a slight "pip" on the detected signal. This will disappear when the board is mounted in the plug-in.
- 7. If you are unable to obtain the correct waveshape, you may need to adjust the value of R92. Replace R92 with a potentiometer having a mid range value the same as that of R92. Vary its resistance until 50% duty cycle is obtained. Remove the potentiometer and measure its value. Replace with a fixed resistor closest to the measured value.

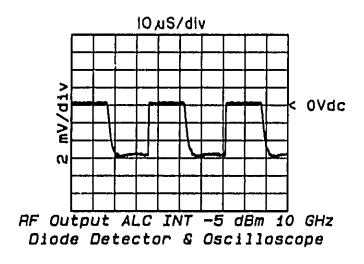


Figure 5-34b. Optimum Squarewave (CHANGE 14)

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HP <b>53590</b> A		83590-90005		HP 83590A						83590-900
						Model	83590A Parts List (CF	IANGE 14) (1 of 5)		
•				Reference Designation	HP Part Number	C O		scription	Mir. Code	
1				А4 А4С1 А4С3 А4С4 А4С6 А4С6	83590-60077 0160-3879 0180-2617 0160-0945 0160-4084 0160-3874	2 7 1 2 8 2	4 CAPACITOR-FXD OLUF 1 CAPACITOR-FXD 6.8 UF 1 CAPACITOR-FXD 910PF 7 CAPACITOR-FXD 1UF ±	± 20% 100VDC CER ± 10% 35VDC TA ± 5% 100VDC MICA 20% 50VDC CER	28460 25088 28480 28480	83590-60077 0160-3879 D6R8G51B35K 0160-0945 0160-4084
<b>`</b>	THIS PAGE INTENTIONALLY LEFT BLANK			A4C8 A4C9 A4C10 A4C11 A4C12	0160-4084 C / 60-4084 0180-2697 0160-3879 0160-3879	8 6 7 7 7	CAPACITOR-FXD.IUF ± CAPACITOR-FXD.IUF ±	20% 50VDC CER 20% 50VDC CER : 10% 25VDC TA ± 20% 100VDC CER	28480 28480 28480 28480 28480	0160-3874 0160-4084 0160-4084 0180-2697 0160-3879 0160-3879
			т. А.,	A4C13 A4C14 A4C15 A4C16 A4C16	0160-4084 0160-0127 0180-2697 0180-2697 0180-2697	B 2   7 7 7	CAPACITOR-FXD.IUF ± CAPACITOR-FXDIUF ± CAPCITOR-FXDIOUF ± CAPACITOR-FXDIOUF ± CAPACITOR-FXDIOUF ±	20% 50' DC CER 20% 25VDC CER 0% 25VDC TA 10% 25VDC TA	28480 28480 28480 28480 28480	0160-4084 0160-0127 0160-2697 0180-2697 0180-2697
				A4C18 A4C19 A4C20 A4C21 A4C22	0180-2661 0160-4084 0160-4084 0160-0572 0160-3874	5   8   2 2	CAPACITOR-FXD  UF ±1 CAPACITOR-FXD  UF ± CAPACITOR-FXD  UF ± CAPACITOR-FXD 2200PF CAPACITOR-FXD 10PF ±	0% 50VDC TA 20% 50VDC CER 20% 50VDC CER ± 20% 100VDC CER	25088 28480 28480 28480	DTROGSTA 50K 0160-4084 0160-4084 0160-4084 0160-0572 0160-3874
				A4C23 A4C25 A4C26 A4C28 A4C28 A4C29	0121-0448 0160-4084 0160-3879 0160-0572 0160-3873	8 1 8 7 1 1 1 2	CAPACITOR-V TRMR-CEF CAPACITOR-FXD.IUF ± 2 CAPACITOR-FXD.01UF ± CAPACITOR-FXD 2200PF CAPACITOR-FXD 4.7PF ±	20% 50VDC CER 20% 100VDC CER ± 20% 100VDC CER	28460 28480 28480	0 21-0448 0163-4084 9160-3879 3160-0572 3160-3873
					0160-3873 0160-3879	1 7	CAPACITOR-FXD 4.7PF ± CAPACITOR-FXD 01UF ±			3160-3873 3160-3879
				A4CR) A4CR3 A4CR4 A4CR5	1901-1098 1901-0535 1901-1098 1901-1098	6 9 4   	DIODE SWITCHING INSI DIODE - SM SIG SCHOTTK DIODE SWITCHING IN41 DIODE SWITCHING IN415	Y 10 50V 200MA 4NS	8480 8480	1901-1098 1901-0535 1901-1098 1901-1098
				A4CR7 A4CR8 A4CR9 A4CR11	1901-0535 1901-0535 1901-0535 1901-1098	9 9 1	DIODE - SM SIG SCHOTTK DIODE - SM SIG SCHOTTK DIODE - SM SIG SCHOTTK DIODE - SM SIG SCHOTTK DIODE SWITCHING IN415	Y 1 Y 1	8480 ( 8480	901-0535 901-0535 901-0535 901-1096
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	Theory of the second	14-11/14-12		CHANGE 14						14-13

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# Model 83590, Parts List (CHANGE 14) (2 of 5)

Reference Designation	HP Part Nymber	C D	Διγ	Description	Mfr. Code	Mir. Part Number
#481	12581124	7	2			
A432	12501124		F	FINPROGRAMING DUMPER .34 CONTACT FINPROGRAMING DUMPER .30 CONTACT	91586 91586	813647561 813647561
AALI	91488218	i.	1	INDUCTOR RFCHMLD 1000H 5X 166DX 305LG	28480	91480210
A4192	58486848	1	L	POADD EXTR YELLOW		
A4H# 3	51019043	6	i		2844C	50106848
A4hp4	12514932	9	i	CONNECTORSGL CONT SKT 021INBSCSZ	28480	5100-9013
AANJS	71217679	ą	i	LBL-IN 03590 14-IN-VD 4-IN-LG	91506 28480	LSG1AGL41 71212679
A401	10538887	7	ı			
A402	18541484	í	1	TRANSISTOR PHP 2H3251 ST TO18 PD+3AINW	84713	5H2521
A4Q3	18541295	;	2	TRANSISTOR WEN ST TOIB PD=J64HU	28461	18548484
A405	10554396	ý	2	TRANSISTOR-DUAL HPH PD=486HW	2848\$	18540295
A404	10551386	9	2	TRANSISTOR JFRT 2H4392 HCHAN DHODE	44713	2H4392
	1022	7		TRANSISTOR JFET 21/4392 NCHAN DHODE	84713	284392
P4Q7	10551423	5	5	TRANSISTOR NOSFET NCHAN E NODE		
A401	1055-1423	ŝ	•	TRANSISTOR NOSFET HCHAN EHODE	17856	VHLERK
A4Q9	18541295	-		TRANSISTOR	17856	VHLERH
A4210	18534316	í	2	TRANSISTORDUN, PHP PD=SITH	28408	18541295
A4911	1853+316	i	•	TRANSISTORDUAL PAP PD-SERING	26481 28461	18531316 18531316
A4913		-			F4101	10394970
A4Q14	18551423	5		TRANSISTON NOSPET NCHAN ENODE	17856	VNLAKN
A4GL6	10534451	3	1	TRANSISTOR PAP 2NJ799 ST TO18 PD-346HW	11295	283799
01910	1855#423	5		TRANSISTOR NOSFET NCHAN EHODE	17856	VHLEKN
AARE	21002515	2	ſ	STATESTATETANK 284K 182 C BIDEADJ LTAN		
A4810	2188-8678	6	i	AEGISTOR - TRHR LEK LEX C SIDE-ADJ 17-TRH		ETSBU284
A4812	21183753	2	i	ESTITION THE THE THE LET C STOR AND 17-THY	32997	3292X1103
AARLS	21802489	Ŷ	i	RESISTOR TRHE 248X 18X C SIDEADJ 17TRH		21103753
AIRLE	14787253	ġ	ż	RESISTORTRNR SK LOX C SIDEADJ 1TRN	34983	ETSIX512
			£	RESISTOR 5.11K 12 .45W F TC+82188	24546	C31/8T85111F
A4R17	16987253	8		RESISTOR 5.11K 12 .45W F TC+4±144	24546	
AARIB	4987257	2	1	REBISTOR 7.5K LT .454 F TC+4+188	24546	C31/8T45111F
M4R19	\$4987263		2	RESISTOR 13.3% 17 . ISU F TC-ELLES	24546	C31/8767581F
A4R28	698-7258	3	ī	RESISTOR B.25K IX . ISU F TC-BALLE	24546	CJ1/8TI1332F
A4821	4678-7261	8	2	REBISTOR LIK IX . 854 F TC-4+LEE	24546	C31/8T48251F C31/8T41142F
MR22	16987262	9	1	-		
A4823	1698-7276	5	-	RESISTOR 12.1K IX .45W F TC+8+188	24546	CJ1/8T01212F
A4825	1678-7261	8	1	RESISION 46.4K 12 .45W F TC=8+188	24546	C31/8784642F
A4R25	14787268	7		RESISTOR LIK 12 . ISW F TC-1+118	24546	C31/0T\$1182F
A4827	16987231	2		RESISTOR LER IX ISW F TC-8+188	24546	C31/8T81482F
	1010	۲	1	RESISTOR ALT IX	24546	C31/8T06198F
A4#29	1698-7254	9	1	RESISTOR 5.62K 1X .05W F TC+01100	24546	CJ1/8TE5621F
A4RIO	88378119	7	4		28484	\$837\$119
A4R31	1678-7279	0	1		24546	
A4812	#69B7264	1	1		24546	C3-+1/8T46192F
A4R33	16797248	2	2	SCRIPTON & JAN IN AND A SA	24546	C]1/8T 1472F C]1/8T ]481F

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# Model 83590A Parts List (CHANGE 14) (3 of 5)

, Reference Designation	HP Part Number	C 0	Qıy	Description	Mfr. Cade	Mir. Part Number
A4834	#6F81457	6	L	46516708 316K 1X 1250 F TC+0+100	28480	1100 Jaco
A4R35	P4987244	7	•	KESIGTOR LOK 12 OSW F TC-RALOR	24546	86983457 Clast/0.57414476
A4#16	85547264	7		REGISTOR LAK IZ ASU F TC-4+144	24546	CJ1/8T81802F CJ1/8T81882F
A4R33	16497243	6	5	RESISTOR 1.96K 12 ISU F TC+8+188	24546	
A4819	16767282	3	i	RESISTOR 02.5X IX 05W F TC=0+100	24546	C31/8T81961F C31/8T80252F
A4R488	66987280	9	1	RESISTOR 147X 12 85W F TC+8+188	24546	C31/0T01473F
A4R41	16997284	5	- L	RESISTOR LANK IX OSU F TC+E-188	2454L	CJ1/8T#1#03F
A4R42	46987256	1	3	RESISTOR 4.81K 12 850 F TC=8+108	24546	CJ1/0T06811F
A4R46	16967234	5	2	RESISTOR 025 12 054 F TC+0+100	24546	C31/011025RF
A4817	\$837\$\$85	6	i	THERMISTOR ROD 600OHN TC++ 7X/CDEG	20401	18371185
A4R48	86987238	9	3	REGISTOR L 21K 12 .05W F TC+0±100	24546	C31/8T41211F
A4R49	16987215	٩	1	RESISTOR SILL IX .85W F TC+8+188	24546	CJ1/8105181F
A4858	17571399	- 5	1	REGISTOR 02.5 12 .1250 F TC+0+100	24546	C41/0T802R5F
A4R5L	16787236	7	1	RESISTOR IN 12 .054 F TC+84184	24546	C11/8181841F
A4R52	16987229	6	2	RESISTOR SIL IX ISW F TC-FELLO	24546	C31/0105118F
A4853	1498-7232	3	2	RESISTOR 681 17 .454 F TC+0±100		
A4R54	1678-3151	7	ĩ	RESISTOR 2.87% 12 1254 F TC+6+100	24546	C31/8T06818F
A4R56	14987268	7	•	RESIGTOR LAK 1X JASH F TC-44140	24546	C41/8142871F
A4857	8699-7248	2		RESISTOR 3.48K 12 .45U F TC+84148	24546	C3L/8T11112 -F
A4RSO	1678-7256	ĩ		RESISTOR & BIK IX USU F TC-84188	24546 24546	C]1/8T1]461F C]1/8-+T16811F
A4859	A100 0000	_		•		•
	16787229	G		RESISTOR SIL 12 .45W F TC+84184	24546	C31/8T0S118F
A4R68 A4R61	1678-7247	1	2	RESISTOR 2.07K 12 ISU F TC+84100	24546	C31/8T12871F
	6987219	6	1	RESISTOR 176 12 ISW F TC-4+104	24546	C31/8T01968F
A4862 .	698-7212	9	3	RESISTOR LEG 12 ISW F TOURLESS	24546	C31/8T01888 ++F
A4863	£6987243	6		RESISTOR LIPOK 12 USU F TOUGELOU	24546	C31/0T81961F
A4864	86987256	1		RESISTOR &. BLK 12 ISU F TC+8+180	24546	
A4848	16787222	i	1	RESISTOR 261 1X . 454 F TC+4+144	24546	C31/8T16811F
A4R69	16987277	6	1	RESISTOR 51.1K 12 . SSN F TC-84188		C31/8T02618F
A4R78	16787246	9	i	RESISTOR 2.61K 12 .450 F TC+4+144	24546	C31/8T85112F
A4R71	1478-7268	5	i	RESISTOR 21.5K IX .45W F TC-44188	24526 24546	C31/8782611F C31/8782152F
A4R72	14787212	,		RESISTOR SEE 12 . ISU F TOURALOR	24546	
A4873	16787212	9		RESISTOR LOB 17 . ISU F TC-42100	24546	C31/8T01#0RF
A4874	44987243	6		RESISTOR 1.76K 12 .85W F TC-8+188		CJ1/8TO1808F
A4R75	86787274	3	1	RESISTOR 38.3K IX OSW F TC-84188	24546	CJ1/BT41961F
A4876	46987264	7	•	RESISTOR LER LZ . ISU F TC-4110	24546 24546	C31/8783832F C31/8T81882F
A4R77	86987268	7		_		
A4R78	21481986	9	i.	RESISTOR LAK 1X .85W F TC=8+188 RESISTORTRHR 1K 18% C TOPADJ 1TRH	24546	C21/0711002F
A4879	1679-7261	;	•	HERISTON CONTRACTOR AND AND A CONTRACTOR AND AND A CONTRACTOR AND A CONTRA	73130	82PR1K
AARE	16787215	í.		RESISTOR 16K 12 .45W F TC+84188	24546	C31/8T11402F
AARBI	2100-2030	6	2	RESISTOR 51.1 12 USW F TC=0+100 RESISTORTRNR 20K 102 C TOPADJ 1TRN	24546 73138	C31/8T05181F 8298248
A4882	21402030	6		RESISTORTRMR 28K 18X C TOPADJ 1TRN	73130	O2PR20K

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# Model 83590, AParts List (CHANGE 14) (4 of 5)

Neferance	in nav				11 49 69	
Designation	iiP Pari Number			Description	Mir. Gada	Mir. Part Numbar
A4R#3	0698-7334			RESISTOR 405 1% 03W F TC=6 \$ 100	24540	
A-1214	(IA98-7232			BUSIL FOR AND IN USAY IS TRUMPLY INDUSAN	24340	
A41385	10498-7260			RESISTOR 10K 1% 05W F TC = 0 = 10024 40	24346	
A4R87	0694-7243	Ą		RESISTOR L96K IN OSW F TCHO ± 100	24546	C3-1/8-TO-1/02-F
A4X88	0698-7364				49290	C3-1/8-TO-1961-F
A 41489	0698-7263	1		AKSISTOR 14.7K 19.05W FTC=0±100	24546	C3-1/8-TO-1412-F
AHILAD	0696-7364	i		RESISTOR 13 JK 1% OSW F TC=0 x 100	24346	C3-1/8-TO-1332-F
A4891	1)498+724/3		,	RESISTOR 14.7K 1% OSW FTC=0 ± 100	24540	C3-1/8-TO-1472-F
A4893	0098-7270	4		RESISTOR 1.47K 19.05W FTC-0+100	24540	CJ-1/8-TO-1471-F
	********	4	I	RESISTOR 26 IK IN 03W F TCHOX (0)	24546	C3-1/8-TO-2612-F
A+1393	0498-7260	1		RUSBEER ION IN DOW PTO HOR IOD	• • • •	
A+B94	0698-7242	j	1	RUBISTOR 1.788 19,03W F TC=0±100	24544	C3-1/16-TO-1002-F
44 <u>11</u> 98	0494-1251	ó	i	RESISTOR 4.328 1% 05W F TC=0±100	24546	C3-1/8-TO-1784-P
A4R97	0498-7207	ä	,	RESISTOR 19.6K 14.05W F TC=0.4.100	24546	C3-1/8-TO-4221-P
AABVA	10098-7257	- 2	I.	RESISTOR 7.3K 1%.03W F TC=0±100	24540	C3+1/8+TO+1962+F
			•		26480	1698-7257
A41149	2100-1738	¥	I.	RESISTOR-TRMR IOK ION C TOP-ADJ I-TRN	73138	#300 LOL
A4B101	07\$7:0424	1	1	RESISTOR 1.1K 1%,123W F TC+0±100	24346	820RIOK
A48103	0498-7203	Ð		REDISTOR \$1.1 1% ASW FTC=0 ± 100	24346	C4-1/6-TO-1101-F
A41106	0698+3449	7		RESISTOR 196 PM. 125W F TC -0 + 100	24346	CJ-1/B-TO-SIRJ-F
A41U10#	0498-8827	4	1	RESISTOR IN 19.125W FTC-0±100	24 24 34 3	C4-1/8-TO-196R-F
A4R110	0698-7243				19401	0698-8827
A472154	1231-5614	6 ()		RESISTOR LYNK (* .05W F TC+0 a 10)	24546	C3-1/8-TO-1961-F
A4TP9	0160-0515	0		CONNECTOR I-PIN M POST TYPE	28480	1251-3018
A4TPIO	0360-0533	0	ļ	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TPL	0360-0315	ů,		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A41912	0360 0333	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
	********	ų		TERMINAL TEST POINT	00000	ORDER BY DESCRIPTION
84U1	1830-1185		)	IC SWITCH AND QUAD IN DIPC PKO		
A41J2	1820-0616	7	1	IC OP AMP PRON QUAD IA DIPC PRO		
A4U3	#76-0610	1	2	IC MULTIPLAR 4-CHAN-ANLO DUAL 16-DIP-C	00003	OPHIEY
A41JA	1826-0417	6		IC SWITCH ANI. Q QUAD '6-DIP-C PKO	00003	MUN24FQ
A41/3	1120-0616	Ŷ.		IC OP AMP PRON QUAD 14 DIPC PRO	27014	LFIJJJD
4.4424					1)600	CP-HEY
A4110 A4117	1770-0610	1		IC MULTIPLAR 4-CHAN-ANLO DUAL IS-DIP-C	36661	MUN24FQ
	18-0-1197	¥	1	IC UATE TTL LS NAND OLJAD LINP	0129	SN74LS00N
Addit	1826-1386	N.		IC SWITCH AND QUAD IS DIRC PKG		art reporte
A4U9	1836-0319	1	2	IC OP AMP WE TO 95 PKG	A3500	AD3391
A4010	1876-0026	3	1	IC COMPARATOR PRCF TU-99 PKG	01295	LMDHL
A4U11	1826-0732	2	1		*****	ENVIC
AIUIZ	1820-1216	5	ł	ICCONY 12-B-D/A 14-DIP-C PKG	24355	AD75428D
AIUIS	1820-1730	6	i	IC DCDR TTL LS & TO-B-LINE J-INP	01293	SN7RL5136
AIUH	1020-1199	ĩ	i	IC FF TTL LS D-TYPE POS-EDGE-TRIO COM	01295	SN74L5271N
A41/15	1420-1198	ΰ	ł	ICINV TTL LS HEX HINP	01295	SN14LS04N
	1-14-14,1111	¥.	ł	IC DATE TTL IS NAMD QUAD 24NP	01295	5N74L503N
A4U16	1826-0021	i i	1	іс ор амрар точурка	1701 -	
A41J17	1826-0447	2	1	IC OP AMP WB TO 99 PKG	27014 27014	LM31011
				·· ·· · · · · · · · · · · · · · · · ·	41414	LF25713



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#### HP 33590A

#### 83590-90005

Model 83590A Parts List (CHANGE 14) (5 of 3)							
-	Balesence Designation	HP Part Number	C D	۵ty	Description	Mír. Cade	Mír. Part Number
	44110	1826+31+	7		IC OP ANP WE TO99 PKG	A3580	AD3591
•	A4UE1 A4UE2 A4UE3 A4UE4 A4UE5	19828841 19828111 19828170 19828849 19828849	4 9 5 2 2	1 1 2	DIODEZHR 5 ILV 5X DO35 PD=.44 DIODEZHR 5 ILV 5X DO35 PD=.44 DIODEZHR 4 22V 5X DO35 PD=.44 DIODEZHR 6 ISV 5X DO35 PD=.44 DIODEZHR 6 ISV 5X DO35 PD=.44	20480 20408 20490 20490 28408 28488	19828841 19828611 19823878 19828849 19828849
	A4U4	01596865	9	١	RESISTORZERO DIVIS 22 AVG LEAD DIA	28468	01570005



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CHANGE 14

14-17/14-18



# A4 AUTOMATIC LEVELING CONTROL (ALC), CIRCUIT DESCRIPTION (CHANGE 14)

The A4 Automatic Leveling Control (ALC) assembly is part of a closed loop power leveling function, designed to control the amplitude of the RF output power. The **General** section below describes loop operation, including some components external to the A4 assembly. The rest of this operational theory is devoted to detailed description of the circuits found on the A4 assembly.

#### General

The circuits which accomplish power control and power leveling can be divided into two categories: internal loop circuitry, and external components of the loop. Figure 8-24 illustrates this theme.

The Power Level Reference leg of the ALC establishes the desired power level. This is accomplished by pressing the plug-in **[POWER LEVEL]** pushbutton and rotating the RPG or entering the desired reference on the Model 8350A/B front panel DATA ENTRY keys. This leg of the ALC is not an interdependent part of the loop, as shown in Figure 8-24.

The Detector leg of the ALC loop samples the actual RF output power and produces a voltage proportional to RF amplitude. This voltage is converted to log scale and compared with the Power Level Reference signal. If the voltages at the summing junction are not of equal magnitude an error voltage is generated. This error voltage is amplified and converted to a current drive for the RF modulators, which vary the transmitted RF power to correct the error and achieve the desired RF power level.

## Address Decoder and Control Latches A

U12 is a 3-to-8 decoder, selecting address 2C07H when it is r esent on the address bus. This address serves as a chip enable for octal latch U13. Informatic a on the data bus is then latched into U13 and used throughout the A4 assembly. U14 and U15 have been added to provide the proper outputs for all 3 ALC leveling modes.

# Detector Inputs and Selection Switches B

Control lines MUX A0B and MUX A1B are encoded with leveling mode and band selection information. The lines are decoded in Table 8-12. U6 decodes these control lines to select the proper detector input for the desired operating mode.

EXT/MTR ALC input provides external crystal leveling capability within the -10 to -200 mV range and power meter leveling capability within the 0 to +1V range. VR4 and VR5 provide protection against transients. Two Schottky Giodes, CR1 and CR2, are mounted between the EXT/MTR ALC connector and the front panel casting for similar protection.

When MTR (power meter) leveling is selected, the power meter (HP 432A/B/C, 436A, or 438A) is used in conjunction with the internal leveling detector. U1A routes the power meter signal to a separate POWER METER LOG AMPLIFIER. The internal leveling detector is routed through U6B and the input sample and hold to the main log amplifier. The internal leveling detector compensates for the response of the power meter and prevents instability while at the same time permitting reasonable sweep times.



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# A4 (ALC), CIRCUIT DESCRIPTION (CHANGE 14) (Cont'd)

#### Sample and Hold Drivers K

Q10 and Q11 act as complementary pairs, controlling the Input Sample and Hold, and Error Sample and Hold circuits respectively. The complementary pairs improve action of the sampling FETS Q5 and Q6 by reducing the error signal passed through gate to source capacitance. The sample and not all function of the ALC loop is used in conjunction with pulse and square wave modulation. When L PULSE ENABL E is high, and either L PULSE or SQ MOD input is low, Q10A and Q11B turn on causing Q10B and Q11A to turn off, thereby initializing the HOLD mode.

The frequency of the sampling mode is dependent on the L PULSE or SQ MOD input. When the system is used with the HP 8756A Scalar Network Analyzer, the SQ MOD input is a 27.8 kHz square wave, controlling the gates of Q5 (Block I) and Q6 (Block E). (Refer to Model 8350A/B Operating and Service Manual, Section V, for 27.8/I kHz Oscillator adjustment). A time delay set by R64 and C26 causes an approximate 5  $\mu$ sec delay, enabling the RF signal to come to full power before releasing HOLD and thus preventing overshoot. The sample level is maintained during the OFF pulse, thus preventing saturation of the Log and Main ALC amplifiers.

The SQ MOD input is also connected to the PIN MOD 1 Driver (Block N) for RF modulation when the Model 8350A/B internal squarewave modulation is used.

#### Input Sample and Hold E

The Input Sample and Hold function prevents the Log Amplifier from saturating during pulse and squarewave modulation.

U16 is a unity gain follower with internal feedback whick buffers the detector input. R78 compensates for the offset voltage of the operational amplifier. Q6 and C21 perform the sample and hold function. C23 is used to reduce error due to the gate to source capacitance of Q6.

#### Power Meter Log Amplifier F

The Power Meter Log Amplifier is used in conjunction with the Log Amplifier in ALC MODE [MTR]. The Power Meter Log Amplifier sets the power level and takes care of low frequency variations, while the Log Amplifier takes care of the high frequency variations.

U5B is a unity gain follower which buffers the input of R5D. Logarithmic scaling is performed by Q3A in the feedback loop of U5D. The base-emitter voltage of Q3A is exponentially related to its collector current, hence the logarithmic action of the amplifier. Q3B compensates the Log Amp over temperature. U5A is a standard non-inverting amplifier, with its gain controlled by R33 and R32. CR3 prevents oscillation in the Log Amplifier.

#### Log Amplifier G

The logarithmic scaling function is performed by Q9A in the feedback loop of U17. Q9A collector current is proportional to the voltage at TP10 and exponentially related to its baseemitter voltage. Therefore, Q9A emitter voltage is logarithmically related to the input voltage at TP10.

Q9B compensates the Log Amp against changes in reverse saturation current with temperature.

CR9 clamps the output of U18 to 0.6V above the input voltage to U17, preventing oscillations.



## A4 (ALC), CIRCUIT DESCRIPTION (CHANGE 14) (Cont'd)

U6A decodes MUX A0B and MUX A1B (Table 8-12) to select the proper offset voltage for power calibration at the low end of the plug-in power range. In EXTernal ALC, the power level calibration is set with the front panel EXT CAL potentiometer.

U18 amplifies the logged output for comparison with the Power Level Summing Signal (Block H). R9 and R10 adjust the gain of U18, and calibrate midrange power levels for their respective bands.

Guarded-gate FETs Q7, Q8 and Q16 select the appropriate detector return for INTernal. EXTernal, and PM (power meter) leveling.

#### Power Level Reference C Power Level Summing H

U11 is a 12-bit microprocessor-compatible digital to analog converter (DAC), which latches data in three 4-bit nibbles. The -10V REF input sets the DAC for a maximum outut (TP2) of +10V. The voltage at TP2 is the product of -10V REF and the fractional binary input of the DAC.

The voltage at TPI is the sum of several voltages, depending on the operating mode of the plugin. U2A sums PWR SWP/COMP and AM inputs. In addition, selected feedback resistors R7 and R8 reduce gain to compensate for detector deviation from square-law at the upper limits of the plug-in power range.

The EXT CAL input is summed through amplifier U2C. R30, in the feedback loop of U2C, provides temperature compensation for the Log Amplifier and detectors.

#### Error, Sample and Hold I

The Error, Sample and Hold function prevents the Main ALC Amp from saturating during pulse and square wave modulation.

U2D pin 10 is the summing junction for the Power Level Summing output, Log Amplifier output, and FREQ TRK V is a 0 to 5 volt ramp proportional to the YTM DRIVE Voltage. R1 (SLP) adjusts the overall slope of Band 0,

Under leveled power conditions, the voltage at U2D pin is zero. A non-zero voltage represents an error and forces a change in modulator current until power is again level.

U2D buffers the error voltage. Q5 and the following integrating circuit (U9) perform the sample and hold. C7 eliminates error due to the gate to source capacitance of Q5.

#### Log Amplifier Selector J

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The Log Amplifier Selector circuit selects through path for the Log Amplifier, or combines its output with that of the Power Meter Log Amplifier (MTR). In MTR, R84 and C3 act as a high pass filter, to shape the output of the Log Amplifier, which is then combined with the Power Meter Log Amplifier output. The combination of the two prevents instability when using certain power meters.



In switch U4: A and B are open, C is closed in INT or EXT DET mode. The opposite is true in MTR mode.

CHANGE 14

19119, 54

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# A4 (ALC) CIRCUIT DESCRIPTION (CHANGE 14) (Cont'd)

Main ALC Amp L Unleveled Signal M

Both inputs to integrator U9 are at virtual ground under leveled power conditions, allowing for immediate response to an input error voltage,

R15 optimizes the speed at which the loop responds to power level changes.

L RFB goes low during bandswitching to blank the RF power, thus preventing the loop from saturating. When Model 8350A/B RF BLANK is selected, L RFB goes low during retrace and U1D closes, pulling current through C4, forcing TPS high and turning on the PIN modulators.

Under unleveled conditions, VR2 and VR3 will clamp the output of U9 at approximately +5 and -7 volts, preventing negative or positive saturation. When the output of U9 approaches -2 volts, comparator U10 activates the front panel LED indicating unleveled power.

U8D is not used.

Collector current in common-base transistor Q1 is exponentially related to the base-emitter voltage. The PIN modulator is driven exponentially to maintain constant loop gain.

Emitter-follower Q2, CR5 and CR4 control the gain of the exponential current drive.

#### PIN Mod 1 Driver N

R105 compensates for the loss of modulator sensitivity with increasing bias current. Q13 and Q14 act to fully turn the modulator on when either SQ MOD or RF blanking is selected.

R92 is factory selected to match the modulator for best square wave modulation symmetry.

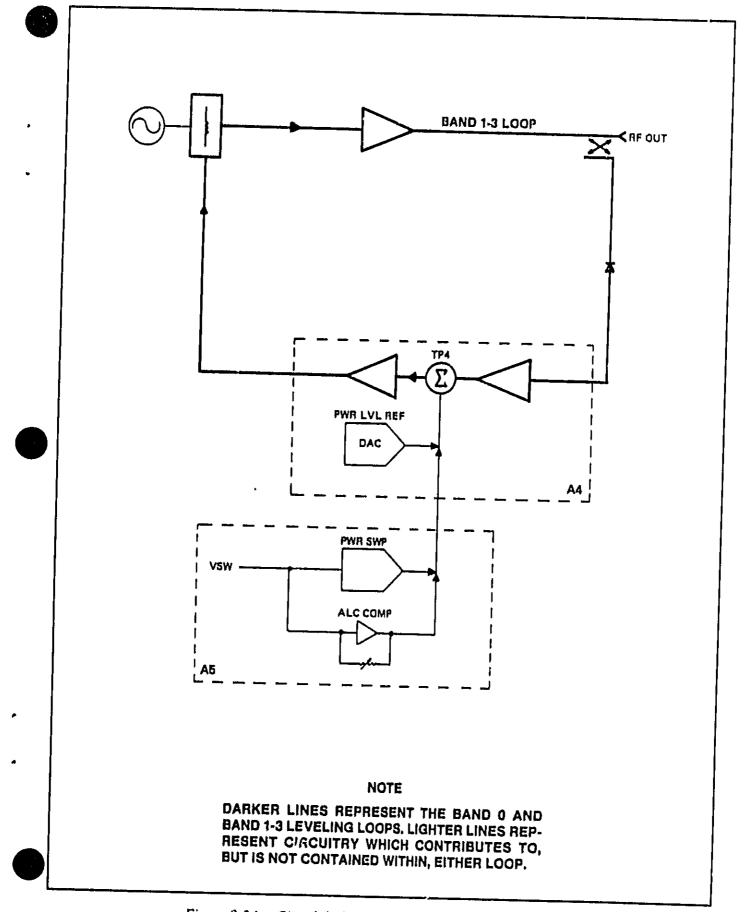


Figure 8-24. Simplified ALC Block Diagram (CHANGE 14)

**CHANGE 14** 

14-23/14-24



# A4 ALC TROUBLESHOOTING (CHANGE 14) (Cont'd)

#### NOTE

# To ensure that Option 002 plug-ins remain in the same attenuator setting during troubleshooting, press [SHIFT] [POWER SWEEP]. This allows full ALC control without changing attenuator settings.

Since the Automatic Leveling Control (ALC) function of the Model 83590A RF Plug-In includes many individual components arranged in a highly interdependent closed loop, the scope of the A4 ALC Troubleshooting section extends well beyond the limits of the A4 assembly. Portions of the A5 FM Driver assembly, and several microcircuit components which contribute to the power leveling function, are discussed below.

The ALC loop is a complex feedback loop which monitors the RF output power and continuously corrects for any deviation from the desired power level. Because it is a closed system, it is difficult to isolate causes from effect when a problem arises. Therefore, the key to troubleshooting is to examine individual components, correlating the expected output for a particular input signal.

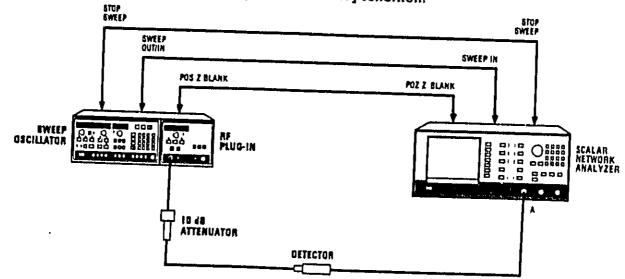
This troubleshooting outline is organized into two major sections: Troubleshooting Symptoms, and Troubleshooting Diagnostics. The section entitled "Symptoms" (1) characterizes possible failure modes, (2) provides some general troubleshooting hints, and (3) refers the reader to more detailed procedures found under "Diagnostics."

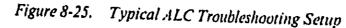
#### Troubleshooling Symptoms

The procedures outlined below help to systematically characterize the failure as quickly as possible. The following failure symptoms are discussed:

RPG/POWER DISPLAY FAILURE UNLEVELED (LED) FLATNESS/OSCILLATIONS (Power Dropouts) FULL UNLEVELED POWER NO POWER (Single Band) NO POWER (All Bands) POWER SWEEP/FLATNESS

Evaluating the specific failure may require an HP 432A/B/C, 436A, or 438A Power Meter or the HP 8756A Scalar Network Analyzer with the Model 11664B Detector. (However, a crystal detector with an "A vs B" oscilloscope may often be substituted.) Figure 8-25 configures a typical test setup. Initiate all tests with the [INSTR PRESET] condition.





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# A4 ALC TROUBLESHOOTING (CHANGE 14) (Cont'd)

# **RPG / POWER DISPLAY FAILURE**

Check that the POWER display changes when either the RPG is rotated or data is entered via the Model 8350A/B keyboard. This verifies that the digital information is reaching the mainframe, is properly processed, and is then displayed.

 If the display is flashing rapidly or showing random patterns, refer to A1/A2 Front Panel or A3 Digital Interface Troubleshooting. If the RPG causes a change in the measured RF power level, but the POWER display remains the same, refer to A1/A2 Troubleshooting. If the RPG produces no response whatsoever, or if the front panel display is blank, refer to A1/A2 Troubleshooting, and trace the problem back to the Model 8350A/B mainframe.

#### UNLEVELED (LED)

If the UNLEVELED light turns on during the sweep, enter a sweep time of 20 seconds (i.e. one second per GHz). Observe the SWP light on the Model 8350A/B Sweep Oscillator, and determine at which times during the sweep the UNLEVELED light turns on.

- If the UNLEVELED light remains lit during retrace, suspect problems in the front panel annunciator drivers. Refer to A1/A2 Troubleshooting.
- If the UNLEVELED light is on during the entire forward sweep, suspect components common to all bands.

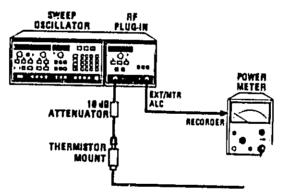


Figure 8-26. Power Meter Leveling Setup



## A4 ALC TROUBLESHOOTING (CHANGE 14) (Cont'd)

- If the UNLEVELED light flashes on briefly three times during the sweep (at 7 and 13.5 seconds into the trace), the problem occurs at the bandswitch points. Check for the RF blanking (L RFB) pulses during bandswitch at A4P1-29, as shown in Figure 8-30. If the signal is missing, trace the problem back through the Model 8350A/B, to the blanking request (L RFBRQ) line on the RF Plug-In A6 assembly. If L RFB is present, but A4TP5 does not clamp at greater than or equal to +4 Vdc during blanking, suspect A4U2D or A4U9.
- If the UNLEVELED light flashes briefly during the sweep, but does not imply any of the above failure modes, check power flatness. See below.

# FLATNESS / OSCILLATIONS (Power Dropouts)

Monitor the RF output with the HP 8756A as shown in Figure 8-25. Optimize the output power with the front panel PEAK control.

- If the power level is constant across the sweep within approximately 5 dB, then the Plug-In may only require ALC flatness adjustments. Refer to Section V, Adjustments, in this manual, for the Internal Leveled Flatness adjustment procedure.
- If the measured power level lies between +10 and -5 dBm, but cannot be controlled via the front panel, refer to the Digital Control section under Troubleshooting Diagnostics.
- If the trace appears chopped or broken, the loop may be oscillating. Refer to Section V, Adjustments, in this manual, and perform the ALC Gain adjustment procedure.

# FULL UNLEVELED POWER (One or More Bands)

If power is unleveled in one Band only, select a sweep width within the unleveled band(s). If power is unleveled in all bands, continue to sweep the plug-in's full range.

- Attempt to level the power externally using the HP 432A/B/C, 436A, or 438A Power Meter as shown in Figure 8-26. Select MTR leveling, and enter a 100 second sweep time. If the RF power is now leveled, the failure is 1 nost likely in the detectors or the Detector Selection Switch, A4U6. Refer to the following paragraph. If this does not prove to be the case, the problem may be in the two analog switches U33 and U6A. It may be necessary to perform the ALC adjustments in Section V of this manual.
- Check the Detector Selection Switch by entering a CW frequency within the band or leveling mode in question and trace the detector voltage through U6B. If the input to be selected does not match the output, check the MUX A0 and MUX A1 lines (see Table 8-12). Also check U12 and U13 as described under Digital Control.
- Check the voltage at TP5. If it is greater than or equal to  $\pm 5$  Vdc, suspect the Mod Drivers or Modulator. If it is below -2 Vdc, suspect the Detectors and Detector Leg.



# A4 ALC TROUBLESHOOTING (CHANGE 14) (Cont'd)

#### NO POWER (Single Band Only)

If no power is detected in one band, but there is leveled power in another band, suspect the components of the RF path appropriate to the faulty band within the ALC loop.

#### NOTE

Turn off LINE switch before removing or installing any assembly.

With the ALC assembly removed from the plug-in, 27.8 kHz squarewave modulation from the Model 8350A/B is not available. However, the HP 8756A 27.8 kHz squarewave can be connected to the rear panel PULSE IN connector to maintain HP 8756A compatibility.

- To check the RF components, remove the A4 ALC assembly from its socket. This removes all bias from the modulator, and should allow maximum power through the RF path in all bands. If full power (at least +12 dBin from 2 to 20 GHz) is then detected in all bands, the RF Amplifier (A14), the DC Return (A15), the Isolator (AT1), and the YTM (A12) are
   verified. Suspect primarily the appropriate detector. Also inspect the modulator, as well as the A4 Mod Driver and Detector Selection Switch.
- If the RF signal for all bands is missing, check the A6 SRD and PIN Diode Blas circuit.

#### NU POWER (All Bands)

#### NOTE

# Turn off line power before removing or installing any assembly.

- If no power is detected in any band, remove the A4 ALC assembly. This removes all bias from the modulator, and should allow full RF power to be transmitted. If there is still no power, check the rear panel AUX OUTPUT for approximately 0 dBm to verify that the A13 YIG Oscillator is providing an RF output. Refer to RF Troubleshooting for details.
- If removing the A4 assembly causes full unleveled RF power to appear, reinstall the board and check A4TP5. If less than -2 Vdc is present, verify that the voltage across R49 is zero. If A4TP5 is greater than +5 Vdc, suspect any circuitry between the Detector Selection Switch and A4TP5, particularly the Log Amp.

#### POWER SWEEP / FLATNESS

 If power increases smoothly with frequency, and POWER SWEEP is NOT selected, suspect problems with the A5 FM Driver assembly.

#### NOTE

# Turn off line power before removing or installing any ascenibly.

Remove the A5 board from the plug-in. If the situation improves, suspect a failure on the A5 assembly.

• If the RF power is leveled within approximatley 5 dB, refer to Section V, Adjustments. in this manual, and perform the Internal Leveled Flatness adjustment procedure.

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## A4 ALC TROUBLESHOOTING (CHANGE 14) (Cont'd)

#### **Troubleshooting Diagnostics**

The troubleshooting information below is organized into functional areas:

DIGITAL CONTROL A	
REFERENCE POWER LEVEL C H	
DETECTORS / DETECTOR SELECTION SWITCH	B, CR
DETECTOR LEG E F G	
MODULATOR LEG   L	
MOD DRIVER N	
MODULATOR A13	
SAMPLE AND HOLD E K	

DIGITAL CONTROL A

Address Decoder U12 and Control Latch U13 control digital switches throughout the A4 assembly. Their operation can be confirmed by performing the Hex Data Rotation Write at address 2C07 Hex. Enter the following keystrokes:

[SHIFT] [0] [0] [2] [GHz s] [0] [7] [M4]

Enters Hex Data command Address location 2C07 (U13) Hex Data Rotation Write

- Check the outputs of U13 for the waveforms shown in Figure 8-2.
- If any output signal is missing or misplaced, check the data lines agains Figure 8-2. If no output is found, look for activity at U13 pin 11. Check for L INSTI and BA3 to pulse low, while BA0, BA1, and BA2 pulse high. If these pulses are missing, trace the problem back to A3 Digital Interface.

If the Digital Control section is working, the primary outputs of U!3 are easily controlled by selecting the appropriate front panel function while in the CW sweep mode. (e.g., BI is held high by selecting a CW frequency in Bands I through 3; selecting MTR leveling holds the PM line high, etc.).

#### REFERENCE POWER LEVEL C H

The Reference Power Level Leg produces a voltage proportional to the desired power level. This signal is a summation of the absolute power reference, AM, detector compensation, and power sweep signals.

The detector compensation and power sweep signals are generated on the A5 FM Driver assembly. If an A5 failure is suspected, refer to troubleshooting information on the A5 Service Sheet. Unless A5 is suspect, simplify A4 troubleshooting by turning off the line power and removing the A5 assembly. Although power sweep will be disabled and the power flatness will be lost, the ALC Loop should still level without the signals provided by the A5 assembly.



DAC U11 establishess the absolute power level. The -10V REF from the A6 assembly is scaled to yield from 0 Vdc (-5 dBm displayed) to the +10 Vdc (+20 dBm displayed) at TP2. (This breaks down to a voltage step of 0.40 Vdc per 1.0 dB of power over the dynamic range, or 6.00 Vdc at +10 dBm.

A self-test routine is available to exercise the ALC DAC. Enter:

#### [SHIFT] [5] [0]

The waveform in Figure 8-31 should be seen at TP2. Note that the exercise routine for the 12-bit DAC yields a staircased waveform with 13 levels. The first step shows the maximum  $\pm 10$  Vdc output with all bits high. The following levels represent the voltage at TP2 with successive bits loaded high in order from the Most Significant Bit to the Least Significant Bit.

 If the waveform at TP2 is not correct, check for -10V REF, and trace any problem back to the A8 assembly. Look for activity on L INST1, BA0, and BA1. BA2 and BA3 should pulse high as each new DAC value is loaded, pulsing the CS line (U14 µin 8) low. If any of these lines, or a data line, appears dead, trace the problem back to the A3 assembly.

U2A adds PWR SWP/COMP and AM, and provides detector flatness compensation at higher power levels with CRI. Use the EXT MTR mode to bypass this diode while troubleshooting.

U2C adds the front panel amplitude adjustment (EXT CAL) used with external leveling. The following levels should be seen at TPI with A5 removed and 1NT leveling selected: +0.3 Vdc for -5 dBm, and +7.0 Vdc for +20 dBm. An amplitude modulation (AM) signal of 1.0 V p-p at PI-4 will produce roughly 260 mV p-p at TP1. (Note that U3A and CR1 in the feedback path around U2A change the gain depending on the band and the desired power level. This may result in a 1.0 Vdc difference between bands at +20 dBm.)

DETECTOR CR1 / DETECTCR SELECTION SWITCH B

The detector CR1 is tested simply by checking the output voltage under full leveled power or full unleveled power conditions.

#### NOTE

The 27.8 kHz modulation signal required for HP 8756A compatibility is not available from the Model 8350A/B when the A4 assembly is removed from the plug-in, and must be supplied from the HP 8756A through one of its rear panel MODULATOR DRIVE connectors.

- If no power is measured in the suspected band, turn off the line power and remove the A4 assembly. Return power to the instrument. (If there is still no RF power, suspect components of the RF path. Refer to RF Troubleshooting.) If full unleveled RF power is obtained, apply a narrow strip of cellophane tape to the pin-edge connector at P1-19 to isolate the output of the modulator driver from the modulators. Reinstall the A4 board. This removes bias from the modulator, allowing full RF power transmission, while providing detector bias.
- If full leveled power (+10 dBm from 2 to 20 GHz) or full unleveled power (at least +2 dB higher than leveled) is measured, sweep only the band in question and check the voltages at the detector input against the values shown in Table 8-11. (Use high-impedance 10:1 probes.)

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#### A4 ALC TROUBLESHOOTING (CHANGE 14) (Cont'd)

Table 8-11. Detector Voltages

	Full Leveled + 10 dBm	Full Unlevaled +20 dBm
Bands 1-3 (A4P1-20)	-100 to -120 mV	−200 to −600 mV

• If the detector is working and the Detector Selection Switch is suspected, sweep only in the faulty band and monitor TP12 for the voltages seen at the selected input of U6B.

• If the EXT/MTR ALC INPUT circuits are suspected, select the desired mode and supply a test signal (low-level DC or sine wave) in the front panel BNC connector, and trace it through U6B at A4TP12.

#### NOTE

# Remove any tape applied to edge connector ping in the previous procedure.

#### DETECTOR LEG E F G

The Detector Leg of the ALC loop includes components between the Detector Selection Switch and the Error Summing Amplifier U2D.

Before troubleshooting the Detector Leg, be sure the Detector and Detector Selection Switch are working correctly. See above.

The Detector Leg can be effectively tested by using the Open Loop method of troubleshooting. This procedure utilizes the external leveling mode (EXT) by supplying an external DC voltage or sine wave to the EXT/MTR ALC INPUT connector. This method breaks the ALC Loop and allows waveforms to be checked against known test signals. See Figure 8-32.

#### MODULATOR LEG | L

The Modulator Leg includes the Error Sample & Hold and the Main ALC Amp.

U2D is a non-inverting unity-gain summing amplifier. Under leveled conditions, both U2D pin 10 and TP8 should be nearly 0.0 Vdc. Under any conditions (except during "hold"), U2D pin 10 and TP8 should be at the same voltage. If not, suspect U2D, Q5, or the Sample & Hold Driver.

U9 forms an inverting integrator. When TP8 is positive, TP5 should be at -7 Vdc. If not, suspect U1D or U9. When TP8 is negative, TP5 should be at +5 Vdc. If this is not the case, suspect U9.

- The following procedure can be used to check U2D and U9:
  - 1. Use a jumper to ground A4TP11.
  - 2. Set power for -5 dBm at any CW frequency.
  - 3. Press Model 83590A [EXT] ALC.

CHANGE 14

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# A4 ALO TROUBLEBHOOTING (CHANGE 14) (Cont'd)

- To check U2D, monitor U2D pin 10 and TPB while adjusting the EXT/MTR ALC CAL screw between the extremes of its range. Both U2D pin 10 and TP8 should vary between approximately +0.5 and -0.5 Vde.
- 5. Verify U9 by adjusting the CAL screw as described above and monitoring TP5. Since U9 is an integrator, TP5 should saturate and clamp (due to VR2 and VR3) at -7 Vdc and +5 Vdc, respectively. (When sweeping across a bandswitch proc URF blanking pulses will saturate TP5 at +5 Vdc regardless of input.)
- 6. Remove jumper from A4TPH to ground.

Further troubleshooting of the Modulator Leg can be continued by following the Open Loop procedure outlined in Figure 8-32 and checking for the waveforms provided in Figure 8-33.

#### MODULATOR DRIVER N

The voltage-to-current conversion and current gain needed to drive the modulators is provided by Q2 and Q1 on the output of the Main ALC Amplifier. As the voltage increases at TP5 so does the current to the modulator, shunting more RF energy to ground and allowing less to pass through. Since the modulator is essentially current-controlled, the voltages measured at TP6, PI-19, and PI-44 do not vary much over a wide range of modulator attenuations.

Q2 is an emitter-follower follow I by a common-base stage (Q1), with two diodes in between. Check the biases and base-emitter voltages to see if the transistors are damaged.

 To establish a bias level for the Mod Driver stages, TP5 can be forced high (+5 Vdc). Using a jumper, ground A4TP11. Press Model 8350A/B [CW] and select a CW frequer by in the appropriate band. Select [EXT] ALC, and enter an RF power level of -5 dBm via front panel controls. Rotate the EXT/MTR ALC CAL knob fully counterclockwise. Verify a signal level of approximately +5 Vde at TP5. Remove jumper from A4TP11 to ground.

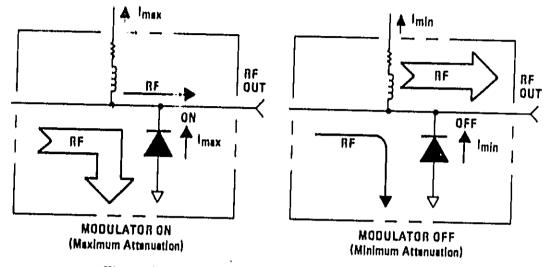
R92 is adjusted for 50% duty cycle of the square wave.

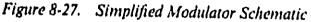
• Set the HP 8350A/B to CW, SQ MOD on. Connect the RF output to a crystal detector and oscilloscope. While observing the square wave, adjust R92 for 50% duty cycle.

#### MODULATOR

The internal modulator for this plug-in is housed in a combination microcircuit package: A16 Modulator/Coupler, Figure 8-27 provides a simplified schematic for this positive-bias, shunttype attenuator. As more current is supplied through the modulator bias pin, the shunt diode turns on harder, sinking more RF power to ground and allowing less to reach the front panel.

# A4 ALC TROUBLESHOOTING (CHANGE 14) (Cont'd)





The modulator is checked simply by noting whether the actual RF attenuation is appropriate to the modulation bias present.

#### NOTE

Turn off line power before removing or installing any assembly.

- If low or no RF power is observed, remove all modulator bias current simply by removing the A4 assembly from the Motherboard. With no bias current, the RF power should pass through the modulator unhindered. If this is not the case, check the modulator diode as follows:
  - 1. Select Model 83590A **[EXT]** ALC. Attach a jumper from A4TP11 to ground. Enter -5 dBm RF power, and select a CW frequency in the appropriate band. Rotate the EXT/MTR ALC CAL knob fully clockwise. This should result in -7 Vdc at TP5, essentially removing bias from the modulator. Measure the voltage across R49. It should be 0V. If this is not the case, isolate each modulator from its drive circuitry by applying a piece of cellophane tape to the pin edge connection: P1-19. If the voltage across R49 now measures 0V, the modulator diode is probably shorted. If the voltage across R49 still does not measure 0V, suspect the band blanking circuitry U8C and Q14. Remove jumper from A4TP11 to ground.

#### NOTE

#### Remove any tape applied to the pin edge connectors in the previous procedure.

- If the modulator appears to be functioning properly, check the following RF levels with a
  power meter or spectrum analyzer. When checking power levels internal to the RF signal
  path, ensure that all critical ports are terminated in 50 ohms.
  - 2. If power is low in all bands, check the RF level at the rear panel AUX OUTPUT connector. Refer to the RF Schematic Diagram at the end of Section VIII for the proper levels. Check the RF levels around the Power Amplifier A14 with no modulation. A14 should output approximately +26 dBm with about +13 dBm at the input.

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# A4 ALC TROUBLESHOOTING (CHANGE 14) (Cont'd)

- If maximum unleveled Ri- power is observed, attempt to achieve maximum attenuation (minimum RF transmitted). Select Model 83590A [EXT] ALC. Attach a jumper from A4TP11 to ground. Enter - 5 dBm RF power, and select a CW frequency in the appropriate band. Rotate the EXT/MTR ALC CAL knob fully counterclockwise. The voltage level at TP5 should be +5 Vdc. Concurrently, the voltage level at the output of the Mod Driver. P1-19, should be approximately +0.6 Vdc to +0.8 Vdc.
  - 1. If the voltages are significantly higher than this, the modulator diode is probably open.
  - 2. Check TP6 for approximately + 2.0 Vdc. The difference between the test point and the corresponding pin-edge connector gives an indication of how much current is flowing to the modulator.

#### SAMPLE AND HOLD E K

There are adjustments to improve the shape of the squarewave. C23 in block E and R99 in block K are used to eliminate offset in the Input Sample and Hold, and Error Sample and Hold circuits respectively. They act to effectively cancel charge passed through the gate to source capacitance of the FET. Refer to Paragraph 5-27 for the proper adjustment procedures.

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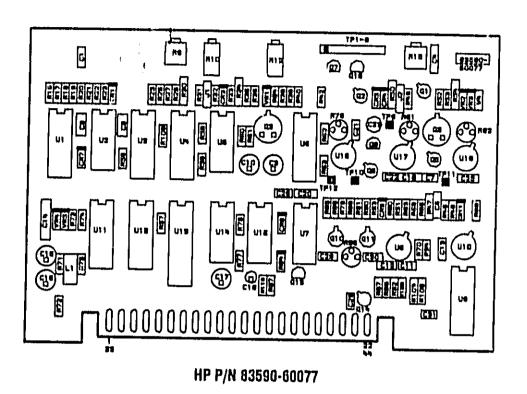


Figure 8-29, A4 ALC Component Locations (CHANGE 14)

CHANGE 14

14-35/14-36

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Table 8-12. Leveling Control Lines (CHANGE 14)

	Levelinn				
Mux A0	Mux A1	Mux A0B	Mux A1B	PM	Leveling Mode
Н	Н	Н	H	Ļ	INT 0 (not used
L	н	L	Н	L	INT I
H	Ĺ	н	L	L	EXT
L	L	Н	Н	н	PM 0 (not used)
L	L	L	н		PM I

CHANGE 14

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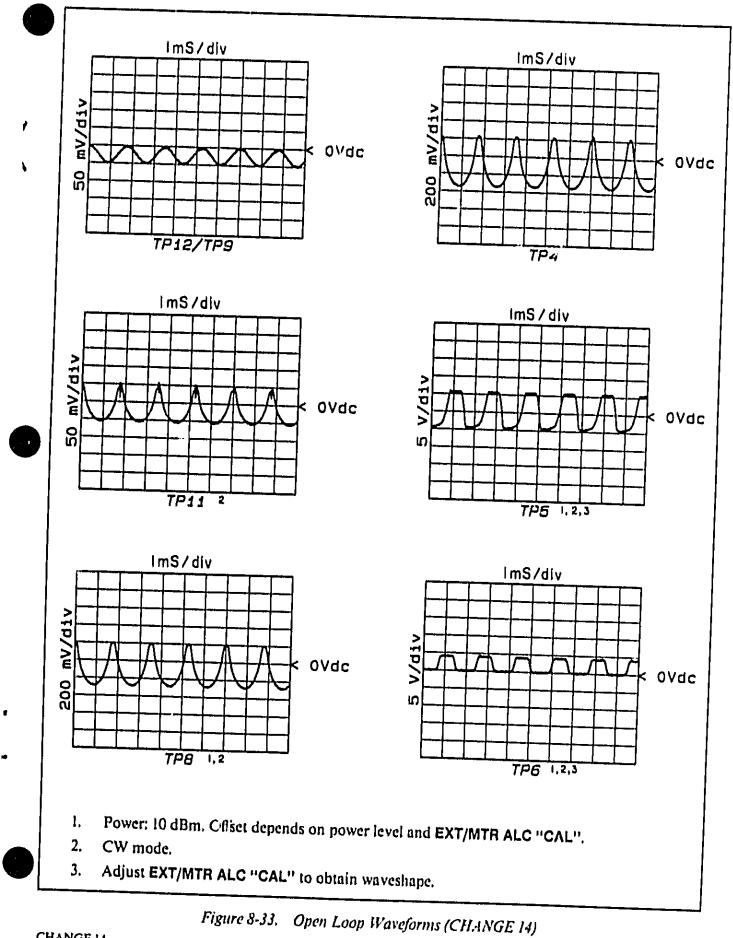
A4P1				
PIN	SIGNAL	vo	TO/FROM	FUNCTION
1 23	EXT DET RET	IN	J2	۹
	EXT DET	IN	J2	۵
2	L UNLVL	OUT	A6P1-40, A10J1-12	M
24	Ext gal	IN	A10J1-41	H
3 25	PWR REF	OUT	NOT USED NOT USED	C
4 26	٨M	IN	P1-AA NOT USED	C
5	PWR SW/COMP	N N	A5P1+23	C
27	+5V		A3P1+6,7	P
6 28	-15V	IN	NOT USED P2-28	þ
7	+10V	IN	P1+8	р
29	L RFB	IN	P2+56	Ц N
8 30	GND DIG GND DIG			P P
9	8D1	IN	A3P1+9	A, C
31	8D0	IN	A3P1+31	A, C
10	803	in	A3P1-10	A, C
32	802	In	A3P1-32	A, C
11	BA1	IN	A3P1-11	A, C
33	BAO	IN	A3P1-33	A, C
12	BA3	IN	A3P1-12	A, C
34	BA2	IN	A3P1-34	A, C
13	8D5	IN	A3P1-13	A
35	8D4	IN	A3P1-35	
14	607	IN	A3P1-14	A
36	806	IN	A3P1-36	
15 37	GND ANLG GND ANLG			P P
16 36	+15V	IN	NOT USED P2-29	Р
17	-10V	IN	P1-13	Р
39	10V	IN	P1-11	Р
18	L INSTI	IN	A3P1-8	A, C
40	SQ MOD	IN	P2-26	K, N
19	MOD 1	OUT	A10E1	N
41	L PULSE	IN	A&P1-25	K
20	INT DET	IN	CRI	8
42	INT DET RET	IN	CRI	
21 43	-10V REF	IN	NOT USED ABP1-3	C
22 44	MOD DRIVE	OUT	NOT USED NOT USED	L

# A401 Pin-out Table (CHANGE 14)



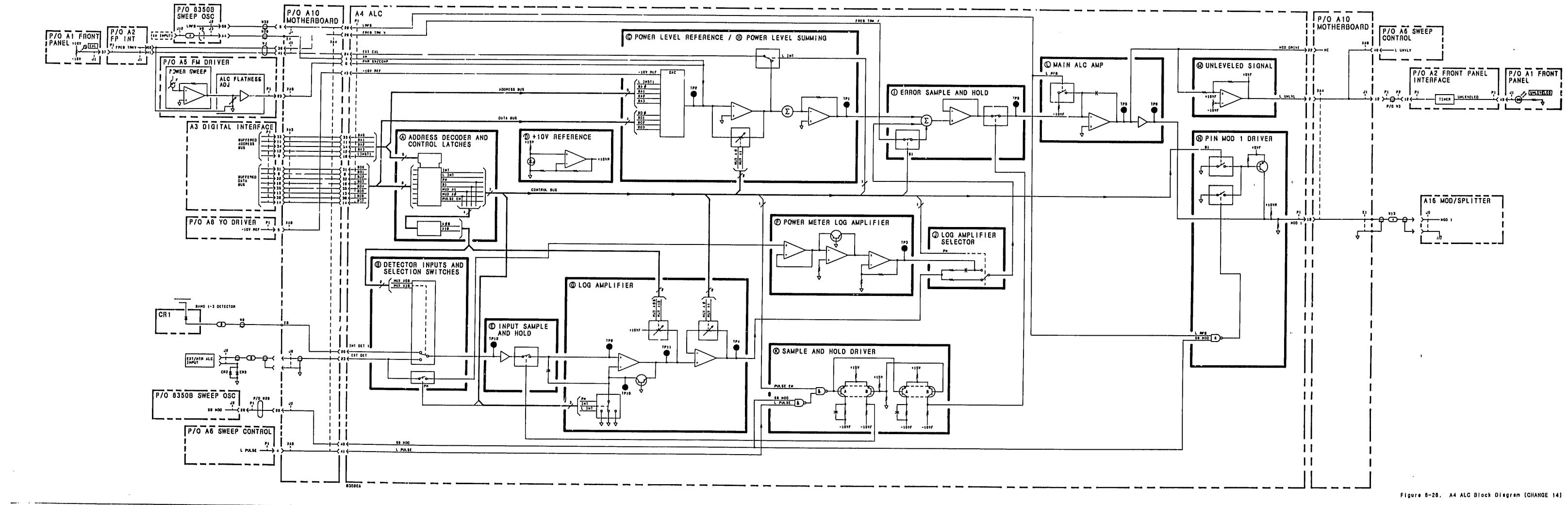
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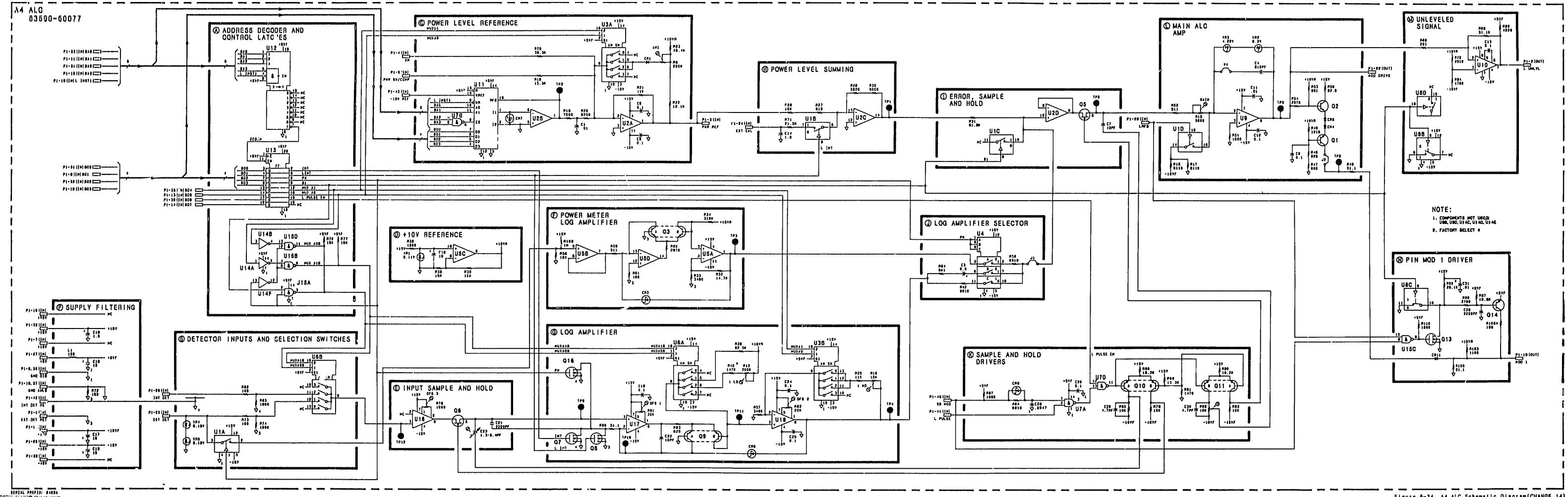


CHANGE 14

14-41/14-42







Finure 8-34 A4 ALC Schematic Diagram(CHANGE 14)

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### CHANGE 15

### (Supersedes CHANGE 10)

### This change Installs Revision 6 firmware,

Page 6-6, Table 6-3:

Change A3 to HP and Mfr. Part Number 83525-60080 CD 6, DIGITAL INTERFACE ASSEMBLY (does not include A3U1 and A3U2). Change A3U1 to HP and Mfr. Part Number 83590-80006 CD 7.

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Change A3U2 to HP and Mfr. Part Number 83590-80006 CD 7. Change A3U2 to HP and Mfr. Part Number 83590-80007 CD 8.

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- Page 8-35, Figure 8-23;
  - Change A3 DIGITAL INTERFACE part number in the top left-hand corner of the schematic to 83525-60080. Change the SERIAL PREFIX in the bottom left-hand corner of the schematic to 2412A.



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#### CHANGE 16

## This change incorporates modifications to the A2 Sub Panel Board and A7 YTM Driver Board.

Page 6-6, Table 6-3: Change A2R1 to HP Part Number 2100-3103, CD •.

Page 6-14, Table 6-3;

Change the A7 YTM Driver assembly HP and Mfr. Part Number to 83595-60068, CD 4.

#### Page 6-15, Table 6-3:

Change A7R52 to: 0698-6358, CD 2, RESISTOR 100K .1% .125W F TC =  $0 \pm 25$ , 28480, 0698-6358. Change A7R64 to: 0698-6977, CD 1, RESISTOR 30K .1% .125W F TC =  $0 \pm 25$ , 28480, 0698-6977. Change A7R65 to: 0757-0438, CD 3, RESISTOR 5.11K .1% .125W F TC =  $0 \pm 100$ , 28480, 0757-0438. Change A7R66 to: 0757-0438, CD 3, RESISTOR 5.11K .1% .125W F TC =  $0 \pm 100$ , 28480, 0757-0438. Change A5R67 to: 0698-6362, CD 8, RESISTOR 1K .1% .125W F TC =  $0 \pm 25$ , 28480, 0698-6362. Change A7R68 to: 0698-8469, CD 0, RESISTOR 1K .1% .125W F TC =  $0 \pm 25$ , 28480, 0698-6362. Change A7R68 to: 0698-8469, CD 0, RESISTOR 6.99K .1% .1 W F TC =  $0 \pm 4$ , 28480, 0698-8469. Delete A7CR6.

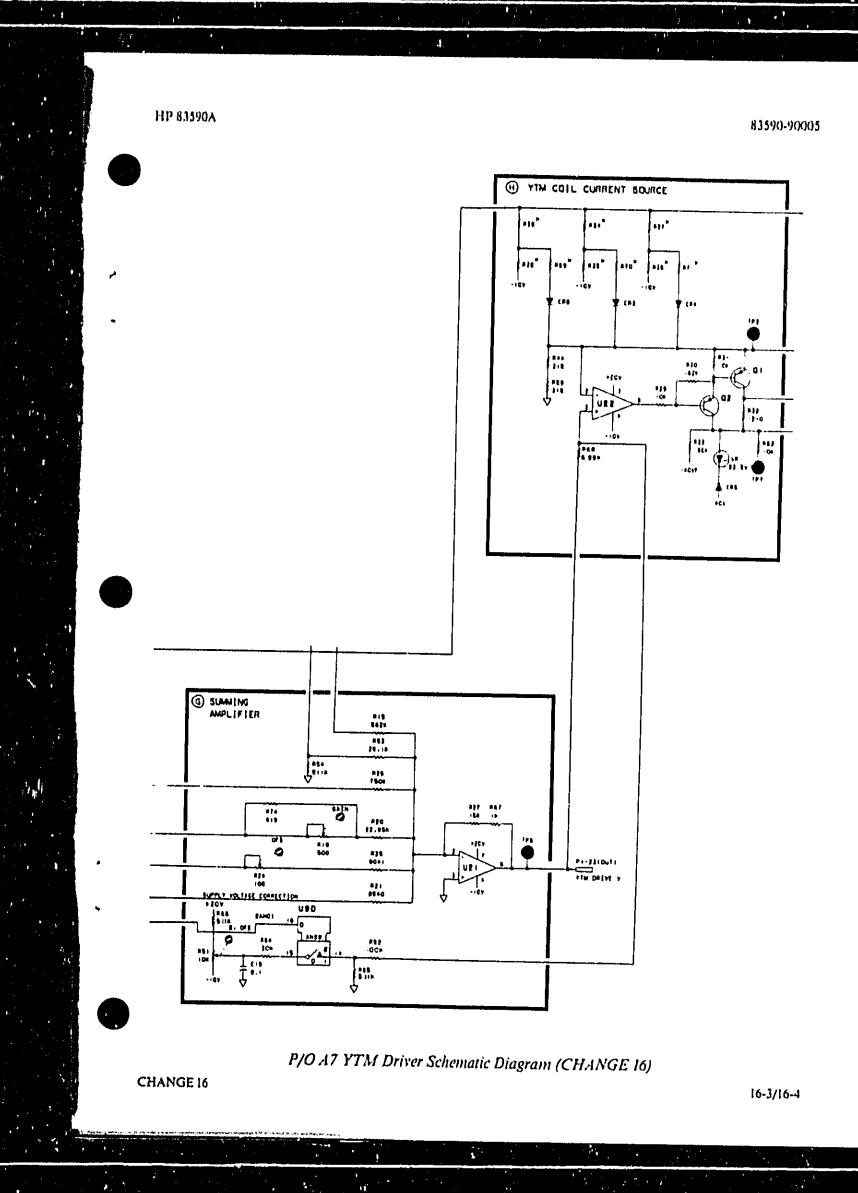
Page 8-63, Figure 8-52 (A7 Component Locations): Delete R68, Change R66 to R68, Change CR6 to R66,

Page 8-63, Figure 8-60 (A7 Schematic):

Replace the function blocks G SUMMING AMPLIFIER and H YTM COIL CURRENT SOURCE with P/O A7 YTM DRIVER SCHEMATIC DIAGRAM (CHANGE 16) in this document. Change the part number in the top left-hand corner of the schematic to: 83595-60068.

Change the SERIAL PREFIX in the bottom left-hand corner of the page to 2413A.

CHANGE 16



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### CHANGE 17

(Supersedes Part Numbers in OHANGE 15)

## This change installs Revision 7 firmware.

Page 6-6, Table 6-3:

Change A3UI to HP and Mfr. Part Number 83590-80010, CD 3. Change A3U2 to HP and Mfr. Part Number 83590-80011, CD 4.

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CHANGE 17

17-1/17-2

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### CHANGE 18

# This change documents the increase in range of the sequential-band delay compensation adjustments.

Page 6-15, Table 6-3: Change A7R42 to HP and Mfr. Part Number 2100-0544, CD 3, RES-TRMR 100K 10%. Change A7R43 to HP and Mfr. Part Number 2100-3611, CD 1, RES-TRMR 50K 10%.

Page 8-63, Figure 8-60;

In block E DELAY COMPENSATION change the following items: A7R42 to 100K A7R43 to 50K



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### **CHANGE 19**

This change documents a revision to the Motherboard Assembly and Power Supply Cables.

Page 6-18, Table 6-3: Change A10 to HP and Mfr. Part Number 83595-60078, CD 6.

Page 6-19, Table 6-3: Change A10J2 to HP and Mfr. Part Number 1251-6952, CD 7. Change A10J3 to HP and Mfr. Part Number 1251-6343, CD 0.

Page 6-22, Table 6-3: Change W28 to HP and Mfr. Part Number 83525-60066, CD 8.

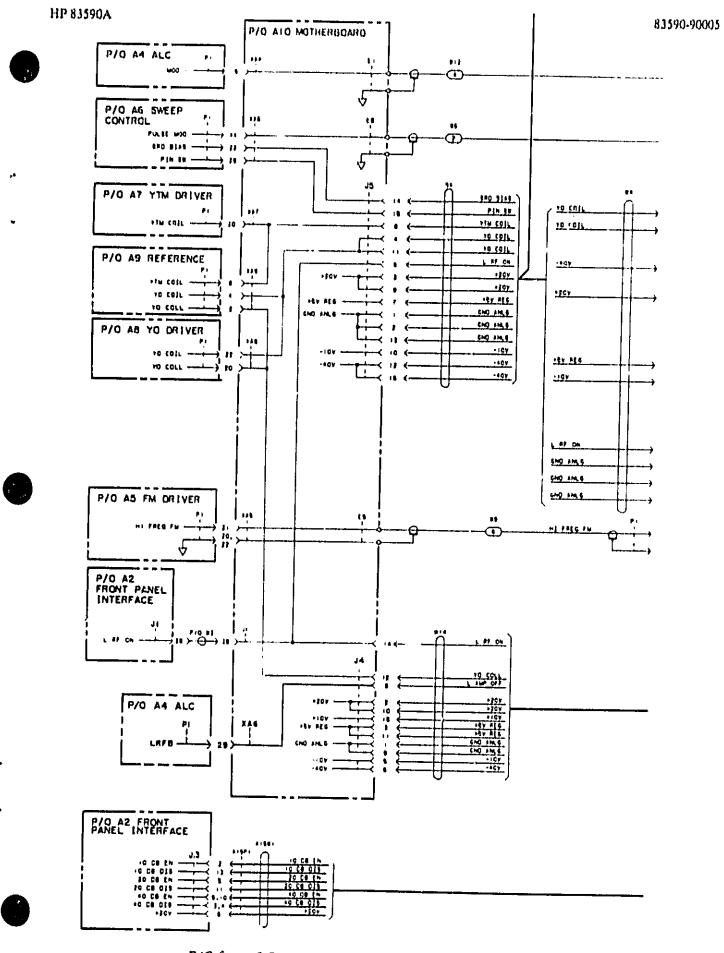
Page 8-75, Figure 8-76. RF Schematic Diagram: Replace left part of Figure 8-76 with P/O Figure 8-76. RF Schematic Diagram (CHANGE 19) in this document.

Page 8-76, Figure 8-79. All Motherboard Component Locations: Replace Figure 8-79 with Figure 8-79. All Motherboard Component Locations (CHANGE 19) in this document.

Page 8-81, Table 8-15. 83590A Motherboard Wiring List (5 of 5): Replace Table 8-15 with Table 8-15. 83590A Motherboard Wiring List (5 of 5) (CHANGE 19) in this document.







P/O figure 8-76. RF Schematic Diagram (CHANGE 19)

CHANGE 19

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19-3/19-4

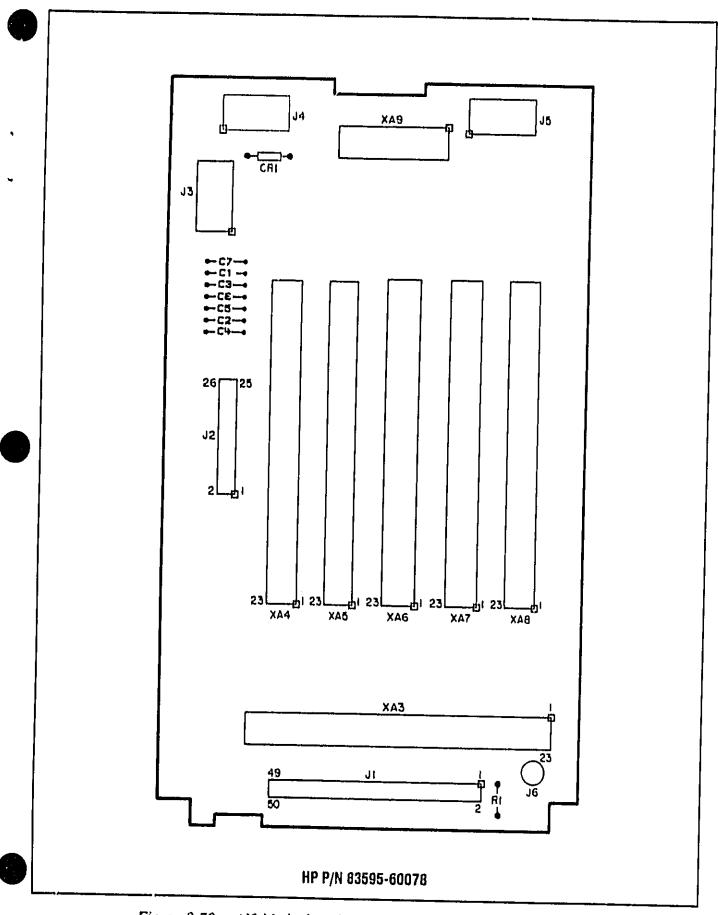


Figure 8-79. A10 Motherboard, Component Locations (CHANGE 19)

CHANGE 19

			Power Supply	Plug-In	Dig	intle	]		Sweep			Ref	F.P.	P/O Plug-in	Power Supply	YO/YTM Ribbon	NF Ribbon	Miscellaneous
Mnemonic	Signal Source	Mnemonic Description	Interface P1	Interface P2	A3P1	ritea	ALC A4P1	РМ Абр1	Control AGP1	YTM A7P1	YO ABP1	Resistor A9P1	Interface A10J1	Interface A10J2	Interface A10J3	Cable A.0J5	Cable AtoJ4	
+20V +20V RET +20V RET SENSE +20V SENSE	P1-7 P1-14 P1-6 P1-16	+20V Regulated +20V Return +20V Return Sense +20V Sense	7 14 6 15				16	16		16	16	3,11	47		7 14 6 15	3,0	7,10	C7
+15V	P2-29	+15V Regulated		20		1	38	38	38	ЭН	36			15				CG
+10V +/-10V RET	P1-8 P1-3, 16	+10V Regulated +/-10V Return	8 3, 16				7	,	7	7	7		46				16	C5
+5V +5VA +5VB +5V REG +5V UNREG	A3P1+6,7 P2-30 P2-18,50,51 A9P1+7 P2-63	+6V Internal for RF Plug-In +6V for 8360A +6V for RF Plug-In +6V Regulated +6V Unregulated		30 18,50,51 63	6,7	35,36,38	27	27	27	27	27	7	2	18,20		7	3,11	
-10V -10V RET SENSE -10V SENSE -10V UNREG	P1-13 P1-12 P1-4 P1-5	-10V Regulated -10V Return Sense -10V Sense -10V Unregulated	13 12 4 5				17	17	17	17 •	17		40	15,70	13 12 4 5	10	6	C4 C3
-15V	P2-2B	-16V Regulated		28			28	28	28	28	28			13				C2
-40V -40V RET -40V RET SENSE -40V SENSE	P1-11 P1-1 P1-10 P1-2	–40V Regulated –40V Return –40V Return Sense –40V Sense	11 1 10 2				6,30			6,39	6,39				11 1 10 2	12,16	6	C1
GND ANLG	W28P1-8 P2-27,58,59	Analog Ground					15,37	16,37	43	16,19, 24,26, 20 37	15,19, 24,26, 29,37	G	4B	10.11, 12,24	19.12,14 16,1,3,6	1,2 13	1,0	C1-C7, R1
GND DIG	P2·1,6,14, 16,21,31, 37,46,48 49	Digital Ground		1,6,14, 16,21,31, 37,46,48, 49	4,5		8,30	8,30	B,30	B,30	Ø,30		ß					Β١
GND SENSE	W28P1-4	Analog Ground Sense										· · · · ·			4			

1 Coaxial Cable

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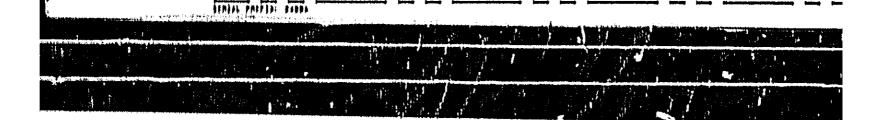
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2 Shielded Cable

* Not used on this assembly

Table 8-15. 83590A Motherboard Wiring List (5 of 5) (CHANGE 19)



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83590-90005

OHANGE 20 This change documents a replacement kil and an exchange replacement kil for the Power Amplifier Assembly. Page 6-2, Table 6-1: Change A14 New Part Number to 83592-60113, Rebuilt Part Number to 83592-60114, Description to Power Amp. 2.5 to 7.0 OHz Rit. Page 6-29, Table 6-3: Chiloge A14 to HP and Mfr. Part Number 83592-00113, CD 7, POWER AMPLIFIER RIT. Change Ald to HP and Mfr. Part Number 83592-60114, CD 8, EXCHANGE POWER AMPLIFIER KIT. Page 6-20, Table 6-3; Change AI (AIC4 to HP part number 0180-0228, 22ufil 15V CD 5, Add AI4AIC9 HP part number 0160-4084, Jufil 50V CD 8, Add Al-AICRI and Al-AICR2 HP part number 1901-0033, 180V 2A CD 2. Change AI4AUI to HP part number 1200-0482 CD 5. Change AIAAIMPI to HP part 5021-5320 CD 8, Change A14A1h1P3 to HP part number 1251-3172 CD 4. Change AI4AIMP5 to HP part number 1200-0173 CD 5. Add AI4AIQ3 IIP part number 1854-0477 CD 7. Add A14A1Q4 HP part number 1853-0281 CD9, Page 6-21, Table 6-3; Add A14A1R32 HP part number 0698-7253 5.11K 1% .05W CD 0. Add A14A1R33 HP part number 0698-7284 100K 19 .05W CD 5. Add A14A1R34 HP part number 0698-7270 26,1K 1% ... 5W CD 9, Add A14A1R35 HP part number 0698-7243 1.96K 1% ,05W CD 6, Add A14A1R36 HP part number 0698-7234 825 1% .05W CD 5. Add A14A1R37 HP part number 0698-7257 7.5K 1% .05W CD 2. Add A14A1R38 HP part number 0698-3438 147 1% ,12W CD 3. Add A14A1R39 HP part number 0698-7284 100K 1% ,05W CD 5. Add A14A1R40 HP part number 0698-3440 196 1% ,12W CD 7. Add AIAAIU2 HP part number 1826-1058 CD 5. Page 8-74, Figure 8-74: Replace Figure 8-74 with Figure 8-74. AI4AI Power Amplifier Bias, Component Locations (CHANGE 20). Page 8-75, Figure 8-76: Replace blocks AHAI and AIA with P/O Figure 8-76. RF Schematic Diagram (CHANGE 20), Change Serial Prefix on bottem left corner to 2507A.

CHANGE 20

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83590-90005

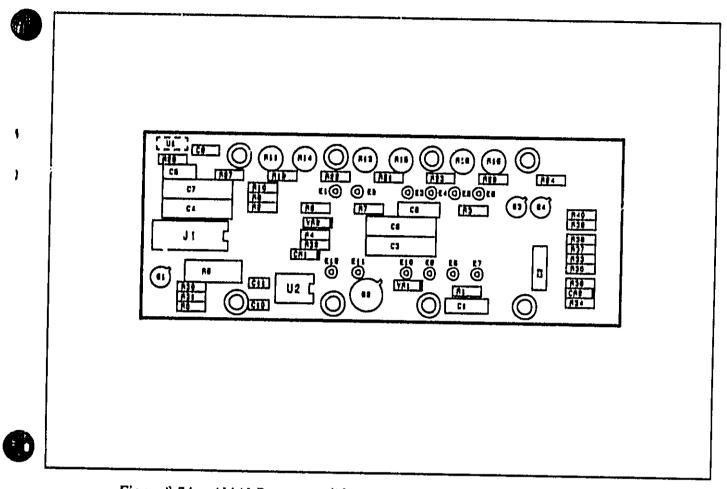
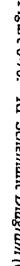


Figure 8-74. AI4AI Power Amplifier Bias, Component Locations (CHANGE 20)

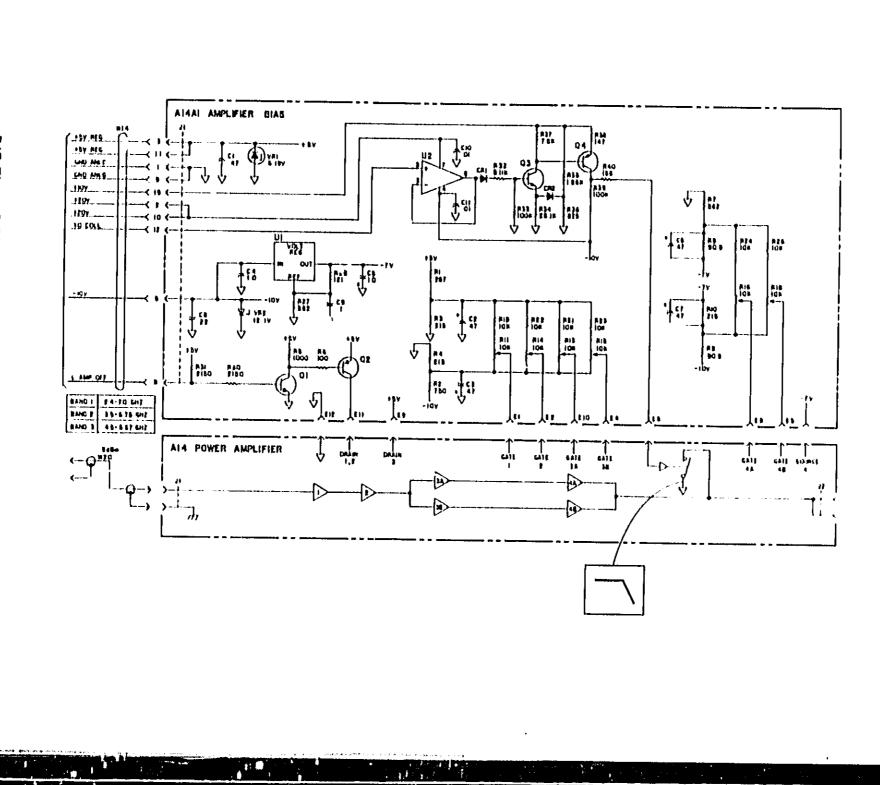
CHANGE 20

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20-5/20-6

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	CHANGE 21
-	This change documents a modified AG Sweep Control Assembly. (Supersedes Change 12)
	Page 6-12, Table 6-3; Replace All the information shown for A6 with P/O Table 6-3. Replaceable Parts (CHANGE 21) (1 of 3) in this document.
	Page 6-13, Table 6-3: Replace All the information shown for A6 with P/O Table 6-3. Replaceable Parts (CHANGE 21) (2 of 3) in this document.
	Page 6-14, Table 6-3: Replace All the information shown for A6 with P/O Table 6-3. Replaceable Parts (CHANGE 21) (3 of 3) in this document.
	Page 8-57, Figure 8-44. A6 Sweep Control Component Locations: Replace Figure 8-44 with Figure 8-44. A6 Sweep Control Component Locations (CHANGE 21) in this document.
	Page 8-57, Figure 8-49. A6 Sweep Control Schematic Diagram: Replace Figure 8-49 with Figure 8-49. A6 Sweep Control Schematic Diagram (CHANGE 21) supplied in this document.

CHANGE 21

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21-1/21-2

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	Reference Designation	HP Part Number		8 ai	iy 	Description	Mir Gode	Mir Part Number
	Aŭ	63590-00100		5 1		BOARD ASSEMBLY-SWEEP CONTROL	28480	
	ABC1. ABCA ABC5 ABC6	0100-2617 0100-2617		2		NGT ASSIGNED CAPACITOR-FRD & BUF++10% JSVDC TA CAPACITOR-FRD & BUF++10% JSVDC TA	66209	[60D685)x8032837
	A6C7 A6C8	0100-2816				CAPACITOR-FXD 100UF+-20% 10VDC TA	86289 26490	150D685X9035832 0180-2818
	A6C9 A6C10 A6C11	0100-0228 0100-0228	8			NOT ASSIGNED CAPACITOR FAD 220F+10% ISVDC TA CAPACITOR FAD 220F+10% ISVDC TA NOT ASSIGNED	68789 68789	1600726#801682 1600726#801682
	A6C12 A6C13			1		NOT ASSIGNED NOT ASSIGNED		
	ABC14 ABC15 ABC16	0160-3878 0160-0673 0160-3878		8		CAPACITORI.FXD 1000PF +-20% 100VDG CER CAPACITORI.FXD 4700PF +-20% 100VDG CER CAPACITORI.FXD 1000PF +-20% 100VDG CER	75400 26480 75400	0180-3878 0180-0573 0160-1078
	A0017 A6018	0160-3878	•	1	ĺ	CAPACITOR-FXD 1000PF +-20% 100VDG CER	28480	0160-34/0
	ABC19 ABC20 ABC21	0160-0675 0160-3878 0160-4064		2 2		CAPACITOR FXD .047UF +-20% 60VDC CER CAPACITOR FXD 1000PF +-20% 100VDC CER CAPACITOR FXD .10F +-20% 60VDC CER	264.00 264.00 264.00	0160-0675 0160-3878 0160-4064
	A8C22 A8C23 A8C24 A8C25	0150-4064 0150-3678 0150-3678 0150-3678		2		CAPACITOR FID . IUF - ROW BOYDG CER GAPACITOR FXD .01UF - 20% 100YDC CER CAPACITOR FXD .01UF - 20% 100YDC CER CAPACITOR FXD .01UF - 20% 100YDC CER	28480 28480 26480	0180-4084 0180-3878 0180-3879
	A8C28 A8C27	0160-3078			!*	CAPACITOR FED 1000PF PON 100VDC CER CAPACITOR FXD 1000PF 20% 20VDC CER	25480 25480	0160-3070
	ABC28	0150-0678 0160-3874		1	!'	CAPACITOR FXD_04TUF + 20% 60VDG CER CAPACITOR FXD_10PF +- BPF 200VDG CER	26480 29480	0180-0675 0150-3074
	A6CR1 A6CR2	1901-0535 1901-0535		1		DIODE-SM 513 SCHOTTKY DIODE-SM 513 SCHOTTKY	264.60 264.60	1801-0535
	A6CR) A6CR4 A8CR6 A8CR6 A8CR7	1901-0635 1901-0050 1901-0050 1901-0050 1901-0050 1901-0050	0 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	1		Diode-SM Big Schottry Diode-SMTCHING Boy 200MA 2NS DO.35 Diode-NMTCHING Boy 200MA 2NS DO.35 Diode-NMTCHING Boy 200MA 2NS DO.35 Diode-SMTCHING Boy 200MA 2NS DO.35	26460 26480 26480 26480 26480 26490	1901-0535 1901-0050 1901-0050 1901-0050 1901-0050
	A0CI18 A6CI18 A0CI10 A0CI11 A0CI12	1801-0050 1801-0050 1801-0050	1			NOT ASSIGNED NOT ASSIGNED NODE-SWITCHING BOY 200MA 2NS DO-35 NODE-SWITCHING BOY 200MA 2NS DO-35 NODE-SWITCHING BOY 200MA 2NS DO-35	79490 79490 79490	1901-0050 1901-0050 1901-0050 1901-0050
	ACRIJ	1901-0033	2	t		DODE-GEN PRP 1809 200MA DO-7	28490	1901-0033
17	AGLI AGL2 AGL3	8140-0137 8140-0137 08503-80001		2	- I 🗖	NOUCTOR RF-CH-MLD 1MH 5% 20X,45L0 0=60 NOUCTOR RF-CH-MLD 1MH 5% 20X,45L0 0=60 XXL-TORXID	28480 26480 28480	8140-0137 8140-0137 11503-80001
17	лбар) Лбар2 Лаар2 Лаар3	5010-6649 5000-9043 0350-01g4	e 0 3	1		IXTRACTOR P.C. BOARD BLUE WI-P.C. BOARD EXTRACTOR XONNECTOR-SGL CONT PIN .04-IN-BSC-52 RND	26480 26480 26480 26480	5040-6849 5000-9043 0360-0124
	80) 802 803 804 804	1858-0473 1854-0477 1858-0423 1854-0018 1853-0405	5 7 5 3 8	3 2 1 2		RANSISTOR MOSFET N-CHAN E-MODE RANSISTOR NPN 2N2222A SI TO-18 PO-600MW RANSISTOR MOSFET N-CHAN E-MODE RANSISTOR NPN SI PO-100 PD-360MW RANSISTOR PNP SI PO-300MW FT-850MHZ	17856 04713 17868 28480 04713	VN10KM BN2222A VN10KM 1854-0018 Etv4205
	606 607 608 609 609 6010	1653-0405 1855-0423 1854-0404 1854-0477 1853-0281	9 6 7 9	1 1		RANGISTOR PNP SI PO-JOOMW FT-850MHZ RANGISTOR MOSET N-CHAN E-MODE RANGISTOR NPN SI TO-18 PD-JOOMW RANGISTOR NPN 21/22/2A SI TO-18 PD-400MW RANGISTOR PNP 21/2807A SI TO-18 PD-400MW	04713 17856 28480 04713 04713	2N4209 VNIOKM 1854.0404 2N2222A 2N2907A
	8011 6012	1854-0909 1854-0909	9	2	11	RANSISTOR NPN 2N2368A SI TO-18 PD-360MW Ransistor NPN 2N2368A SI TO-18 PD-360MW	26480 25480	**.54-06//8 1854-0508
	6A) 6R2				N	OT ASSIGNED OT ASSIGNED		
	6R3 674 6R5 6R5 6R7	0787-0290 0787-1094 0690-3446	1 8 1	]   1	2222	07 ASSIGNED 07 ASSIGNED 505107 14 19, 125W F TC=0+100 505107 14 19, 125W F TC=0+100 505107 14 17, 19, 125W F TC=0+100	24546 24546 24546 24546	C4-1/6-T0-1001.F C4-1/8-T0-1471.F C4-1/8-T0-1471.F
	578 579 5710 5711 5712	0757-0401 0658-7260 0658-7267 0658-7283 2100-1739	0 7 4 8	1 6 1 2 1		SISTOR 100 1 % .125W F TC=0+.100 SISTOR 10K 1% .05W F TC=0+.100 SISTOR 18 K 1% .06W F TC=0+.100 SISTOR 19.0K 1% .05W F TC=0.100 SISTOR 50 K 1% .05W F TC=0.100 SISTOR 50 K 1% .05W F TC=0.100	24548 24548 24548 24548 24548 73138	C4+1/8-T0-101-6-404-F C3-1/8-T0-1002-F C3-1/8-T0-1062-F C3-1/8-T0-8082-F G3-1/8-T0-8082-F B2PR10K

## P/O Table 6-3. Replaceable Parts (CHANGE 21) (1 of 3)

CHANGE 21

21-3/21-4

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P/O Table 6-3. Replaceable Parts (CHANGE 21) (2 of 3)

Reference Designation	HP Part Number	D	aly	Description	Mir Code	Mfr Part Number
AGA12 Vol16 Vol16 Vol16	0787-0442 0787-0280 0696-0459 8100-3788 0696-8488	1 0 0 0	3 0	RESISTOR 10K 1% .125W F TC-0+-100 RESISTOR 1K 1% .125W F TC-0+-100 RESISTOR 8.88K .1% .1W F TC-0+-100 RESISTOR 8.88K .1% .1W F TC-0+4 RESISTOR 8.88K .1% .1W F TC-0+4	24548 24548 24548 25480 25480 25480 56490	C4-1/0-T0-1002.F C4-1/0-T0-1001.F OdB0-0409 2100-3765 D690-0409
A6718 A6719 A6721 A6721 A6722	0494-8488 0494-8488 0498-0442 2100-3767 0495-0431	0016	1	RESISTOR 6.894 .1% .1W FTC-0+4 RESISTOR 8.894 .1% .1W FTC-0+4 RESISTOR 104 .1% .1W FTC-0+4 RESISTOR 104 .1% .1W FTC-0+5 RESISTOR 8.96K .1% .1W FTC-0+5	F8480 F8480 F8480 F8480 F8480	0690-8469 0698-0489 0699-042 9100-3767 0699-0631
A 6/123 A 6/124 A 6/128 A 6/126 A 6/127	0689-0933 8100-3132 0688-0933 2100-3132 0686-0934	8-8-0	8 2 1	RESISTOR 27 322X .1% .1W F TC-0+.8 RESISTOR 17RMR 600 10% C 500E-ADJ 17-TRN RESISTOR 27.32X .1% .1W F TC-05 RESISTOR 38.000 10% C 500E-ADJ 17-TRN RESISTOR 38.660K .1% .1W F TC-0-6-5	264 B0 764 B0 264 B0 264 B0 264 B0 264 B0	0499.0933 9100-3752 0699.0933 2100-3752 0699.0934
A67720 A67729 A6730 A6731	8100-3732 0690-4488	7	1	REDISTOR-TRMR BOO 10% C SIDE-ADJ 17-TRIV NOT ASSIGNED NOT ASSIGNED REDISTOR 8 984,1% .1W F TC-0+4	26400 E6460	2100-3732
AGR 32 AGR 33 AGR 33 AGR 35 AGR 36 AGR 37	0600-8459 0600-8469 2100-3765 0696-8469 0496-5627 2106-3760	0 0 4 0 4 0	1	REDISTOR 6.99K .1% .1W FTC=0+4 REDISTOR 6.99K .1% IW FTC=0+4 REDISTOR-TRAR 50 10% C 505E-ADJ 17-TRN REDISTOR 6.99K .1% IW FTC=0+4 REDISTOR 1M 1% .12% FTC=0+100	26460 28100 20400 21400 26400 26400	0699-8489 0699-8489 0699-8489 2100-1786 0599-8489 0599-8489 0598-8489
16738 16738 16738 16740 16741 16742	0494-9437 0699-0164 0696-6967 0757-0442 0698-3250		1	RESISTOR-TRANS 20K 10% C SDE ADU 17-TRAY RESISTOR 1M 1% ,125W F TC-0+-100 RESISTOR 7.2K,1% ,125W F TC-0+-25 RESISTOR 7.3K,25% ,125W F TC-0+-50 RESISTOR 7.5K,25% ,125W F TC-0+-100 RESISTOR 464K 1% ,125W F TC-0+-100	26400 25400 27460 24646 26466 25460	2100-3750 0698-0627 0688-0154 0698-5687 C4-1/8-T0-1002-F 0696-3260
6743 6744 6746 6746 6747	0696.3150 0767.0442 0696.3240 0696.3160 0767.0421		2	RESISTOR 8.37K 1% .125W # TC-0+100 RESISTOR 10K 1% .125W # TC-0+100 RESISTOR 484K 1% .125W # TC-0+100 RESISTOR 484K 1% .126W # TC-0+100 RESISTOR 9.37K 1% .126W # TC-0+100 RESISTOR 925 1% .126W # TC-0+100	24546 24545 26460 24548 24548	C4-1/8-10-2371.F C4-1/8-10-1002.F 0660-3200 C4-1/8-10-2371.F C4-1/8-10-025R.F
61748 61749 61750 61751 61752	0787-0421 0698-3447 0690-3440 0690-7812 0698-0004	4 / / #		RESISTOR 826 1% .125W F TC-0+-100 RESISTOR 422 1% .125W F TC-0+-100 RESISTOR 104 1% .125W F TC-0+-100 RESISTOR 106 1% .06W F TC-0+-100 RESISTOR 2.16K 1% .125W F TC-0+-100	24848 24846 24846 24846 24848	C4-1/8-T0-826/LF C4-1/8-T0-4221:F C4-1/8-T0-196R-F C3-1/8-T0-100R-F C4-1/8-T0-100R-F C4-1/8-T0-2161:F
6053 6754 6755 6755 8756 6757	0896-3429 0696-3463 0696-8627 0696-3188 0696-3266	82466		RESISTOR 18 4 1% .125W F 1C=0+.100 RESISTOR 196K 1% .125W F 1C=0+.100 RESISTOR 1M 1% .125W F TC=0+.100 RESISTOR 231K 1% .125W F TC=0+.100 RESISTOR 237K 1% .125W F TC=0+.100	03888 24546 26490 24546 24546 24546	PME88-1/8-T0-19R6.F C4-1/8-T0-1683.F O698.0927 C4-1/8-T0-2812.F C4-1/8-T0-2373.F
9758 9759 9769 9780 6781 19782	0767-028J 0696-7234 0696-7277 0696-7277 0767-0458	77987	1 2 1	REDISTOR 1K 1% ,125W F TC=0+100 REDISTOR 1K 1% ,04W F TC=0+100 REDISTOR 81.1K 1% ,04W F TC=0+100 REDISTOR 81.1K 1% ,04W F TC=0+100 REDISTOR 81.1K 1% ,125W F TC=0+100	24545 24546 24546 24545 24545	C4-1/8-T0-1001.F C3-1/8-T0-1001.F C3-1/8-T0-8112.F C3-1/8-T0-8112.F C3-1/8-T0-8112.F C4-1/8-T0-8112.F
876) 8764 8765 8766 8767	2100-2030 0698-7260 0698-7272 0498-7253	;	, İ	RESISTOR-TRAIN 20K 10% C TOP.ADJ 1-TRN RESISTOR 10K 1% .05W F TC-0+100 NOT ASSIGNED RESISTOR 31.6K 1% .03W F TC-0+100 RESISTOR 5.11K 1% .03W F TC-0+100	73130 24546 24546 24546	82PH20K C3-1/8-T0-1002-F C3-1/8-T0-3162-F C3-1/8-T0-3111-F
5768 5769 5770 5771 5771	2100-2516 2100-2516 0696-1237 0698-1242	) 8	,	RESISTOR TRAIR 100K 10% C SIDE ADJ 1-TRN RESISTOR TRAIR 100K 10% C SIDE ADJ 1-TRN NOT ASSOLNED RESISTOR 1.1K 1% .03W F TC=0+100 REFISTOR 1.1K 1% .03W F TC=0+100	12897 32897 24548 24546	3328W.1.104 3328W.1.104 C3-1/8-T0.1801.F C3-1/8-T0.1801.F
5173 5174 5176 5176 5177	2100-2521 2100-2521 0696-7283 0696-7285	0	2	RIGISTOR-TRIMR 2X 10% C GDE-ADJ 1-TRN REDISTOR-TRIMR 2X 10% C GDE-ADJ 1-TRN NOT ASSOCHED RESISTOR 90 9K 1% .03W F TC-0+-100 REDISTOR 110K 1% .03W F TC-0+-100	20903 30993 24645	E150x202 E150x202 C1-1/8-T0-4092.F
176 179 179 180° 181 181	2100-2692 0689-7743 0696-3162 0696-7260 0696-7243	4 7 8 7		RESISTOR-TRIMR IM 20% C SIDE-ADJ I-TRIN RESISTOR JABK I% 00W F TC-0+-100 RESISTOR JABK I% 126W F TC-0+-100 RESISTOR JABK I% 126W F TC-0+-100 RESISTOR IDK 1% 00W F TC-0+-100 RESISTOR J. JOK 1% 00W F TC-0+-100	30883 28480 24548 24546	C3-1/8-T0-1103-F ET60x106 0689-7243 C4-1/8-T0-3481-F C3-1/8-T0-1981-F C3-1/8-T0-1981-F
R93 R94 R95 R96 R97	0698-7238 0698-7260 0698-7260	5 9 7 7 7	•	RESISTOR 1.78K 1% .0C.//FTC=0+-100 RESISTOR 1.21K 1% .0GW/FTC=0+-100 RESISTOR 10K 1% .0GW/FTC=0+-100 RESISTOR 10K 1% .0GW/FTC=0+-100 RESISTOR 10K 1% .0GW/FTC=0+-100	24546 24546 24546 24546 24546	C3-1/8-70-1981-F C3-1/8-70-1211-F C3-1/8-70-1002-F C3-1/8-70-1002-F C3-1/8-70-1002-F C3-1/8-70-1002-F
TP1 TP2 TP3 17 4				20NNEGTON 10-PNN M POST TYPE DONNECTOR 10-PNN M POST TYPE 20NNECTOR 10-PNN M POST TYPE 20NNEGTOR 10-PNN M POST TYPE	26400 26400	1261-4672 1261-4672 1261-4672 1261-4672



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Reference Designation	HP Part Number	0 D	aly	Description	Mir Code	Mir Part Number
AUTP5 AGTP6 AGTP7 AGTP0 AGTP0 AGTP0	1261-4672 1261-4872 1261-4872 1261-4672 1261-4872	4		CONNECTOR 10-PW M POST TYPE CONNECTOR 10-PW M POST TYPE CONNECTOR 10-PW M POST TYPE CONNECTOR 10-PW M POST TYPE CONNECTOR 10-PW M POST TYPE	F3480 28480 29480 26480 26480 26480	1261-4672 1261-4672 1261-4672 1261-4672 1261-4672
A61P10 AGUI	1261-4072	4		CONNECTOR LOUPIN M POST TYPE	20400	1251-4672
AGU2 AGU3	1678-0720 1020-1211 1820-1196			IC SWITCH ANLS QUAD 16-DIPLC PKG IC DATE TTL LE EXCL-OR QUAD 2-INP IC FF TTL LE D-TYPE POS-EDGE TRIG COM	00665 01285 01295	5W-02FQ 5N741586N 5N7415174N
NGUA NGUB NGU7 NGU7	1624-0720 1629-0471 1826-0471 1820-1112	4 2 2 2 0	6	IG SWITCH ANLG QUAD 18-DIP.C PKG IC OP AMP LOW-DRIFT TO:99 PKG IG OP AMP LOW-DRIFT TO:99 PKG NOT ASSIGNED	06565 25400 25400	5W-02FO 1026-0471 1026-0471
1009 10010 10011 10012	1820-1730 1926-1180 1826-1180 1820-1180		1 2	IG FF TTL LS D-TYPE POS-EDGE-TING IG FF TTL LS D-TYPE POS-EDGE-TING COM ANALOG SWITCH & SPST 18 -CENDIP ANALOG SWITCH & SPST 18 -CENDIP G FF TTL LS D-TYPE POS-EDGE-TING IG FF TTL LS D-TYPE POS-EDGE-TING	01295 01295 26480 26480	5N74L57AAN 5N74L5273N 1020-1106 1026-1106
6V14	1820-2024	5	1	C DRVR TTL LE LINE DRVR OCTL	01295	SN74LB74AN SN74L5244N
8018 6016 6017 6018	1826-0471 1820-1246 1820-1216 1826-0762			IC OP AMP LOW DRAFT TO BE PAG IC GATE TTL LE AND OUAD 2 JAP IC DOOR TTL LE 3 AND OUAD 2 JAP IC DOOR TTL LE 3 JAP IC DOOR Y 12-B-D/A 18-DIP-C PAG	01295 28480 01295 01295 24365	(1431) 1628-0471 16741500N 5N7415136N A0764260
6U18 6U20 6U21 8U21 8U23	1826-0471 1826-0471 1820-1202 1820-1187 1826-0026		1	ic op Amp Low-Drait to 99 pro 10 op Amp Low-Draft to 99 pro 10 gate tt. LS nang tr. Junp 16 gate tt. LS nang ouad 2.1np 16 gametr. LS nang ouad 2.1np 16 gametr. LS nang ouad 2.1np	28480 28430 01285 01295 01295	1826-0471 1828-0471 SV74LSION SV74LSION LMJ1L
8J24 8J25	1828-0052	!	;	IC OP AMP OP DUAL TO BE PKG	26480	1826-0092
5U26 5U27	1826-0185		1 1	ic op amp spci, to 99 prg ic op amp low-biashtunpo 8-diplo prg	3.665 01295	CA3080 TE071ACJG (PER HP DWG)
IVAL	1902-3002	3	1	DIODE-ZNR 2.37V 6% DO-7 PD+ 4W TC++ 074%	20400	1902-3002
iw1 iw2 iw3	8159-0005	0		REBISTOR-ZERO OHMS 22 AWG LEAD DIA NOT ASSIGNED NOT ASSIGNED	28480	8159-0006
W4	8158-0005	0	1	RESISTOR-ZERO CHIMS 22 AWG L ZAD DIA	20400	8158-0005
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		l				

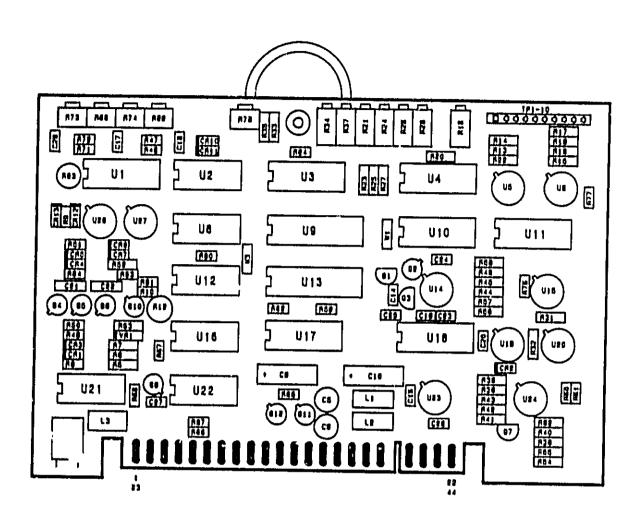
### P/O Table 6-3. Replaceable Parts (CHANGE 21) (3 of 3)

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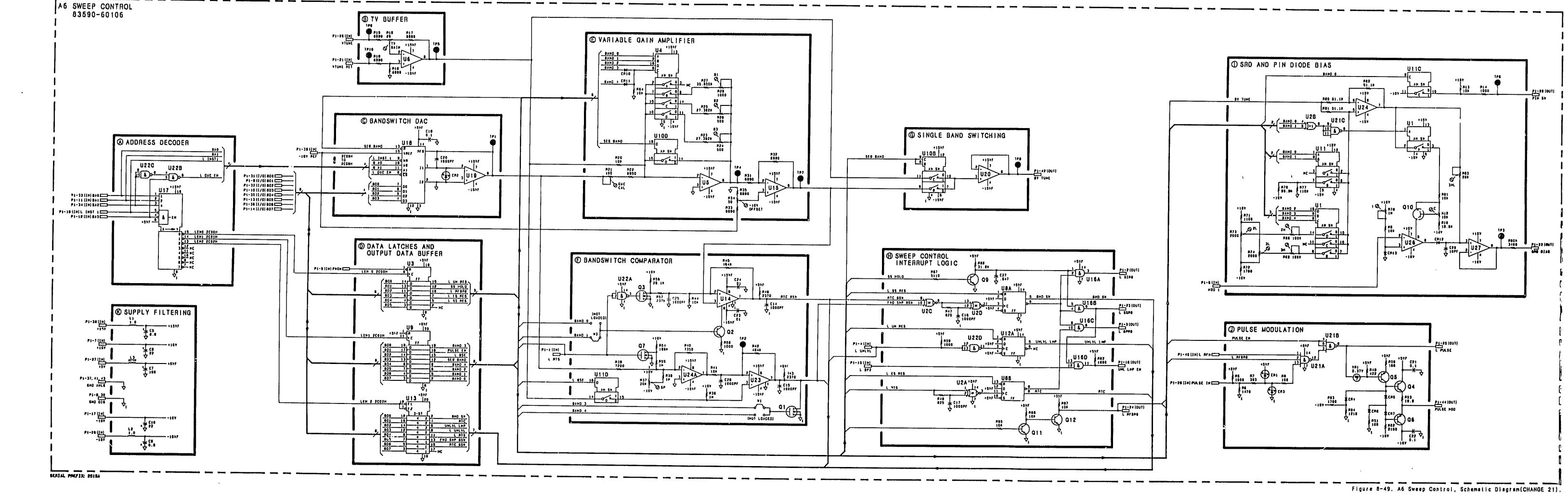


HP P/N 83590-60106

Figure 8-44. A6 Sweep Control Component Locations (CHANGE 21)

CHANGE 21

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### CHANGE 22

This change documents a new Front Panel casting and dress panel.

Page 6-21, Table 6-3:

Change MP4, FRONT PANEL-DRESS to HP Part Number 83590-00008, CD 1. Change MP18, CASTING-FRONT to HP Part Number 83545-20081, CD 7. Change MP19, RETAINER-PUSH ON to HP Part Number 0510-1267, CD 6. Change MP 28, LATCH-SCREW to HP Part Number 83525-20069, CD 0.

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### 🕨 OHANGE 23

(Auperandes OHAHOR 11)

### This change documents a selectable FREQUENCY REFERENCE output.

Throughout the manual there are references to the 1.0 V/OHz rear panel output. Change all references to include 0.5 V/OHz. What follows are some specific areas to change.

Page 1-6, Table 1-2, (Supplemental Performance Characteristics);

Under ORNENAL CHANAOTENISTIOS

Change fraquency fisierance Output to, selectable, 1.0 V/OHz  $\pm 25$  mV (0.0) to 18 OHz or 0.5 V/OHz  $\pm 25$  m / (0.01 to 26.5 OHz) rear panel BNC output.

Page 1-8, paragraph 1-22:

Change to read as follows:

A rear panel 1.0 V/OHz (0.5 V/OHz) signal corresponds to the RF output frequency up to 18 GHz (26.5 GHz). This output voltage is selectable and may be used as a reference for pretuning external equipment. The HP 8410B/8411A network analyzer utilizes the 1.0 V/OHz output for phase-locking. The HP 83554A/55A/56A millimeter-wave source module uses the 0.5 V/OHz as its frequency reference for millimeter frequency applications.

#### Page 3-12:

After page 3-12 add page 3-13/3-14, Figure 3-10. Frequency Reference Selection Switch provided in this document.

#### Page 5-43, paragraph 5-24, FREQUENCY REFERENCE IV/OHz OUTPUT: Add the following:



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#### NOTE

The frequency reference selection switch must be set to the 1.0 V/GHz position before performing this adjustment. Refer to rigure 3-10.

Page 6-5, Table 6-3;

Change A2 to HP and Mfr. Part Number 83590-60122, CD 6.

Add A2CY HP and Mfr. Part Number 0160-4808, CD 4, CAPACITOR-FXD CER 470 pF 100 WV.

Page 6-6, Table 6-3: Change to the following:

Notoranco Dosignation	HP Part Number	0D	Description
A2R8 A2R9 A2R10 A2R11 A2R18 Add the follo	0757-0463 0698-7251 0698-6320 0698-6630 0698-3159 wine:	4 6 3 5	RESISTOR-FXD 82.5K 1%.125W RESISTOR-FXD 4.22K 1%.05W RESISTOR-FXD 5K 0.1%.125W RESISTOR-FXD 20K 0.1%.125W RESISTOR-FXD 26.1K 1%.125W
Roference Designation	HP Part Numbor	CD	Description
A2R27 A2R29 A2S1 A2VR1	0698-7260 0698-5437 3101-2751 1902-0041	7 6 1 4	RESISTOR-FXD 10K 1%,05W RESISTOR-FXD 12K 0.1%,125W SWITCH ROCKER 2 POSIT ON DIP 1A DIODE-ZNR 5.11V 5% DO-35 PD=,4W



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Delete A2R28,

#### CHANGE 23

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CHANGE 23 (Cont'd)	
Page 6-21, Table 6-3: Change MP35 to HB and MG. Dest Number 83502 00020, CD P	
Change MP35 to HP and Mfr. Part Number 83592-00028, CD 7.	
Page 8-25, paragraph titled 1V/OHz Frequency Tracking Amplifier A2: E 1V/OHz Amplifier A2: G: Add the following: When A2SI is closed 0.5 V/OHz frequency reference output is selected. UTA is now scaled to provide 0.5 V per GHz up to 26.5 GHz.	
	4
Page 8-31, Figure 8-12:	
Replace the Components Location Dingram with Figure 8-12. A2 Front Panel Interface, Components Locations (CHANGE 23) provided in this document.	j
Page 8-31, Figure 8-18:	
Replace Figure 8-18 with Figure 8-18. AI Front Panel/A2 Front Panel Interface, Schematic Diagram (CHANGE 23) provided in this document.	

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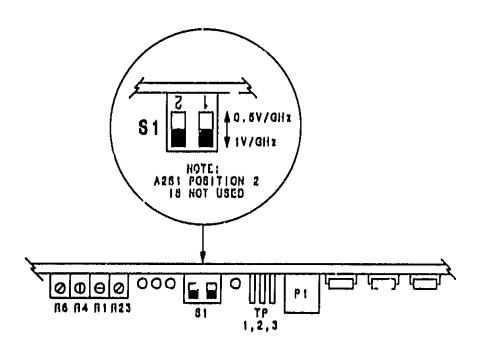


Figure 3-10. A2 Frequency Reference Selection Switch (CHANGE 23)

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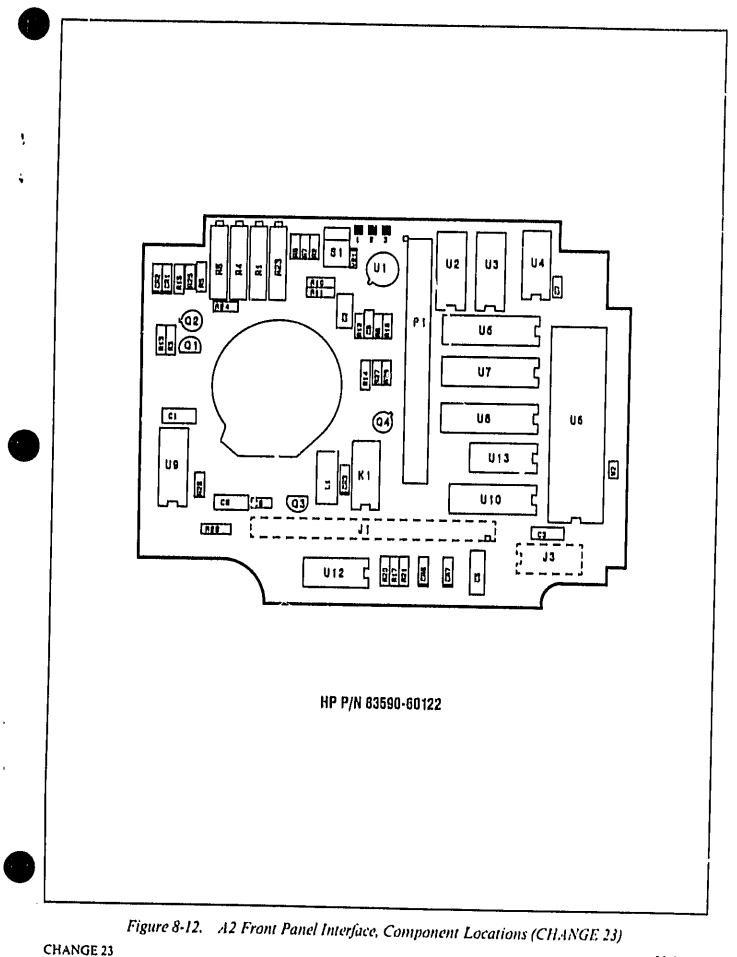
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CHANGE 23

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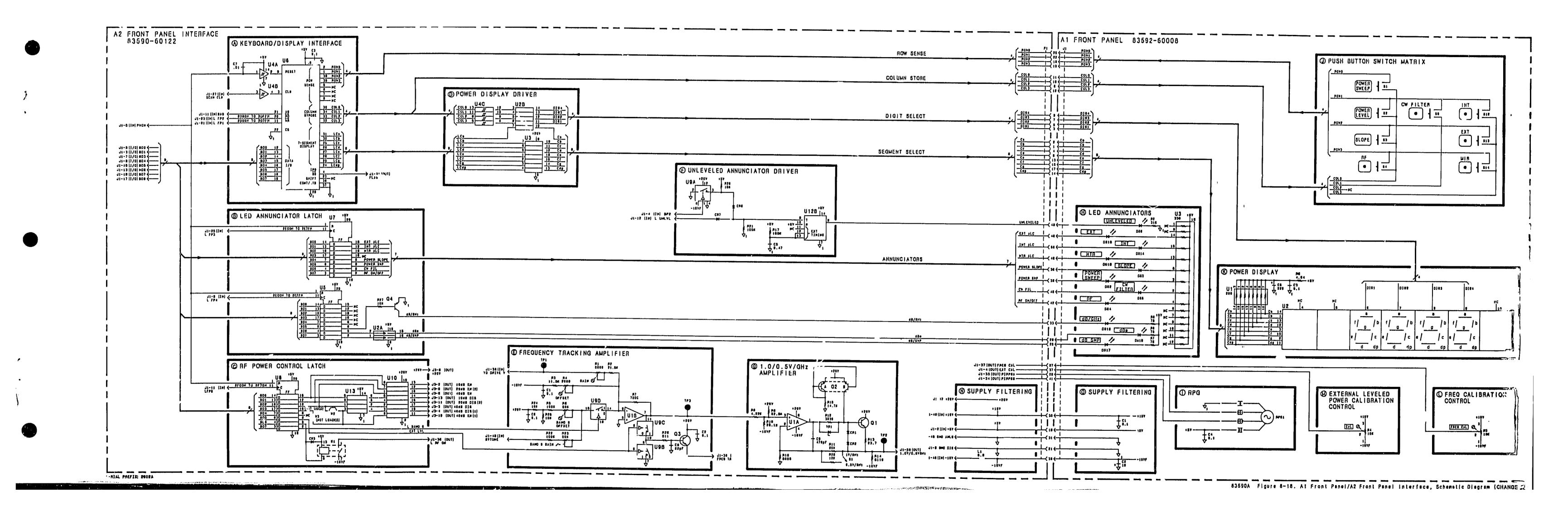


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#### CHANGE 24

## This change documents a new YO Driver Board Assembly.

On the pages listed below, replace the figures with the new figures given.

#### Adjustments

Page 5-11, Figure 5-2. - 10V Reference Adjustment Location.

- Page 5-14, Fis are 5-4, Sweep Control Adjustment Location.
- Page 5-17. Ligure 5-7. YO and YTM DAC Calibration Adjustment Location.
- Page 5-7.5, Figure 5-14. YO Retrace Compensation Adjustment Location.
- Page 5-28, Figure 5-16. YO Delay Compensation Adjustment Location.

#### Service

Page 8-69, Figure 8-63. A8 YO Driver, Component Locations.

Page 8-69, Figure 8-71. A8 YO Driver, Schematic Diagram:

Replace Block | YIG COIL CURPENT SOURCE with the partial schematic P/O A8 YO Driver, Schematic Diagram (CHANGE 30) from this document.

#### Page 6-16, Table 6-3;

Change the A8 Part No. to 83595-50070, CD 8, 83595-60070. Add A8C22, 0160-3879, CD 7, CAPACITOR .01UF + 20% 100VDC CER, 02010, SR201C103MAA. Add A8C23, 0160-3879, CD 7, CAPACITOR .01UF + 20% 100VDC CER, 02010, SR201C103MAA. Add A8C24, 0160-3878, CD 6, CAPACITOR .001UF + 20% 100VDC CER, 02010, SR201C102MAA. Add A8C25, 0160-4801, CD 7, CAPACITOR 100 PF + 5% 100VDC CER, 02010, SA101A101JAA.

Page 6-17, Table 6-3;

Add A8CR9, 1901-0033, CD 2, DIODE-GEN PRP 180V 200MA DO-35, 00046, NDP692.

Page 6-18, Table 6-3:

Add ABR70, 0698-7220, CD 9, RESISTOR 215 1% .05W FTC= +100, 00746, CRB20. Add ABR71, 0698-7220, CD 9, RESISTOR 215 1% .05W FTC= +100, 00746, CRB20.

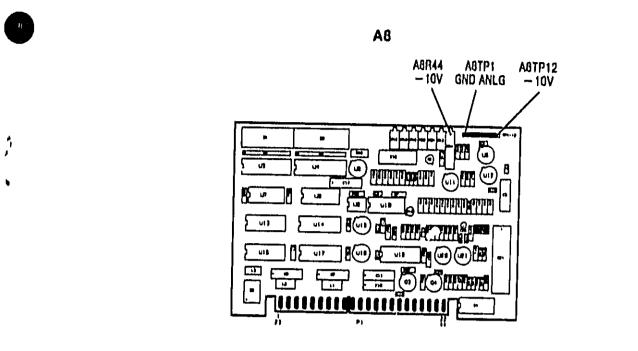
#### Page 8-69, Figure 8-71 in the upper left hand corner: Change the Part No. 83592-60002 to 83595-60070.

#### Page 8-69, Figure 8-71 in the lower left hand corner: Change the Serial Prefix 2620A.

CHANGE 24

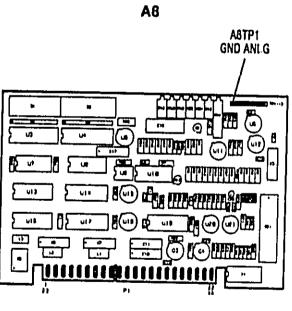
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Figure 5-2. - 10V Reference Adjustment Location (CHANGE 24)

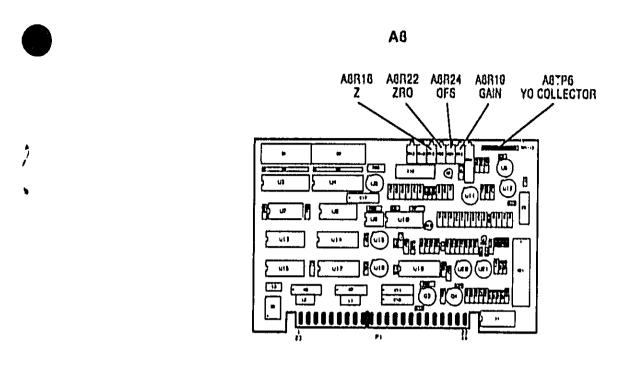


HP P/N 83595-60070

Figure 5-4. Sweep Control Adjustment Locations (CHANGE 24)

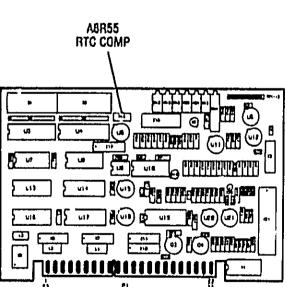
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HP P/N 83595-60070

Figure 5-7. YO and YTM DAC Calibration Adjustment Locations (CHANGE 24)

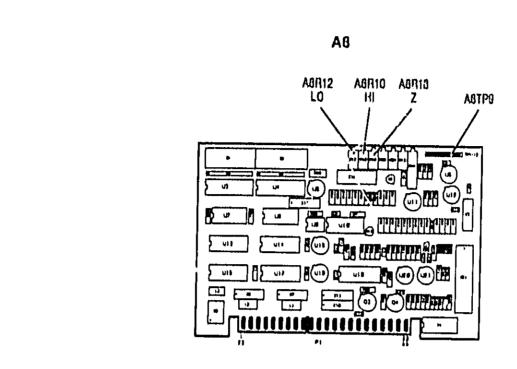


HP P/N 83595-60070

Figure 5-14. YO Retrace Compensation Adjustment Location (CHANGE 24)

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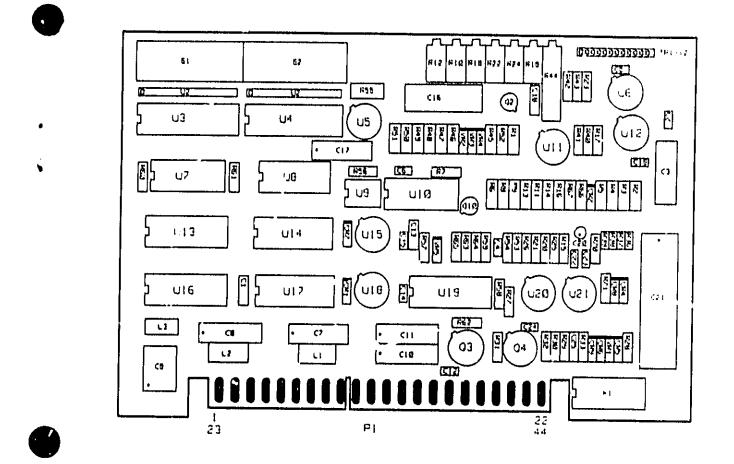
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CHANGE 24



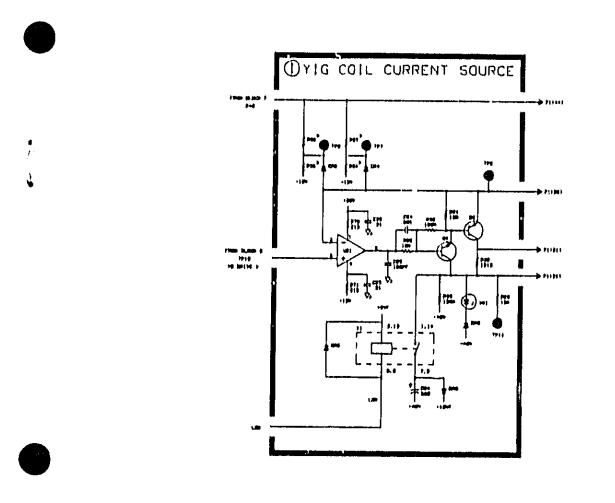
HP P/N 83595-60070

Figure 8-63. A8 YO Driver, Component Locations (CHANGE 24)

CHANGE 24

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24-9/24-10



HP P/N 83595-60070

P/O Figure 8-71. A8 YO Driver, Schematic Diagram (CHANGE 24)

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### ► OHANGE 25

This change documents the addition of a jumper to the A4 ALC assembly, it does not change any electrical functions of the ALC. Change 14 in this document is assumed to be incorporated prior to making the changes written in this change (Change 26).

Section VI, Replaceable Parts:

Change A4 ALC assembly to HP and Mfr. Part Number 83590-60098, CD 5,

Add A4W6, HP and Mfr. Part Number 8159-0005, CD 0, RESISTOR-ZERO OHMS 22 AW6 LEAD DIA.

#### Page 8-47, Figure 8-29:

Replace the Components Location Diagram with Figure 8-29. A4 ALC, Component Locations (CHANGE 25) provided in this document.

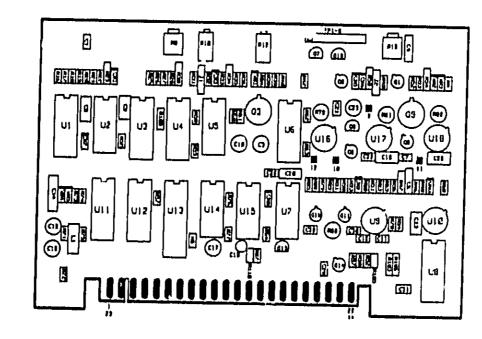
#### Page 8-47, Figure 8-34;

Add A4W6 in series with the input to U15C pin 9 located in block N, PIN MOD I DRIVER,

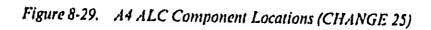


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