

Keysight EEsof EDA

W2324 High Capacity Layout Pre-processor Element

Data Sheet

Key Features

The Advanced Design System (ADS) High Capacity Layout Pre-processor Element has the following capabilities when used in a high-speed digital design flow:

- Imports large PCB design files in ODB++ format into a pre-processor GUI
- Allows critical net selection and cookie cutting
- Exports processed segment of PCB to ADS Layout for EM modeling using Momentum and FEM Element
- Supports import of netnames and components

Overview

The High Capacity Layout Pre-processor Element is an ODB++ file format import and pre-processing tool that enables you to select the environment immediately around critical nets in preparation for electromagnetic (EM) modeling. This type of pre-processing is useful in high-speed digital design where the printed circuit board (PCB) is very complex and whose total geometry exceeds the capacity of an EM-based field solver. The solution is to focus in on a handful of critical nets, for example, a differential pair connecting two Serializer/Deserializer (SERDES) integrated circuits (ICs) that are a victim of crosstalk from one or more aggressor traces. An example of such a trace is shown in figure 2. Note that the board has been “cookie cut”, meaning a convex hull with a user-defined margin has been defined, leaving a portion of the board whose complexity is within the capacity constraints of full-accuracy, full-wave EM field solvers such as Momentum and FEM Element.

High Speed Digital Design Flow

A typical high-speed digital workflow including High Capacity Layout Pre-processor Element is shown in figure 1.

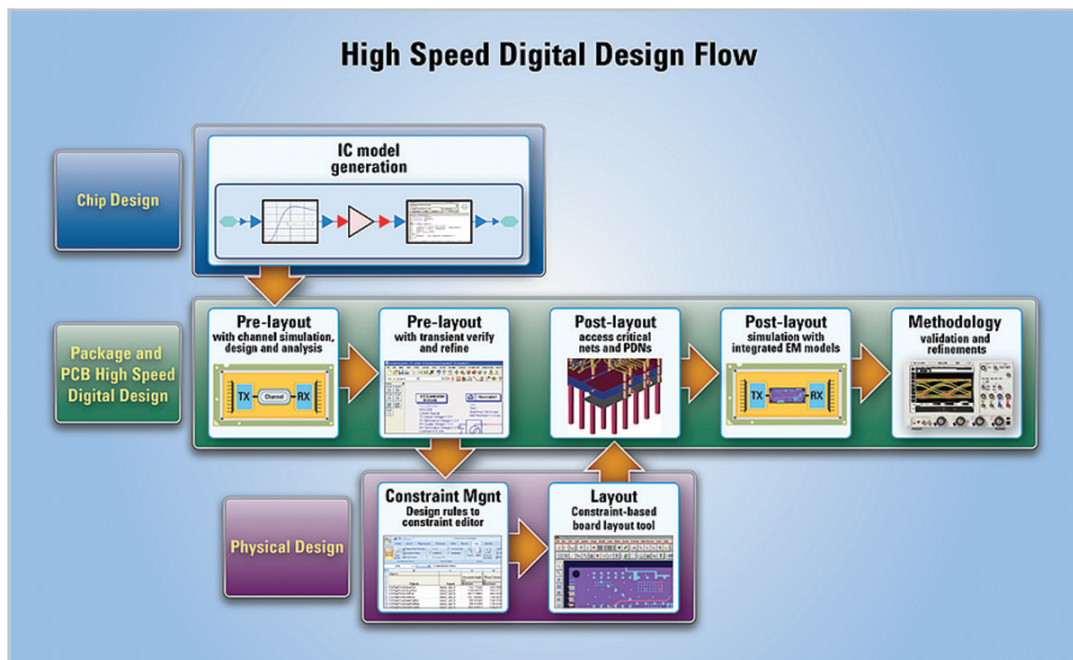


Figure 1
The High Capacity Layout Pre-processor is central to this high-speed digital design flow. The middle bar (green) and lower bar (purple) encloses steps performed by the signal integrity engineer in ADS, and by the physical designer in the third-party enterprise PCB tool, respectively. The task in the upper (blue) bar is performed by the chip designer.

First, the signal integrity engineer combines vendor IC models with a pre-layout “placeholder” for the channel. Typically this placeholder is created from the ADS Multi-Layer Models (MLM) transmission line library possibly supplemented with EM-based via models. The goal of the pre-layout simulation batches is to explore the design space and optimize IC settings (such as the transmitter (Tx) SERDES pre-emphasis filter taps and the receiver (Rx) SERDES equalizer taps and clock/data recovery (CDR) circuit settings), stack up, controlled impedance line geometry, and via design.

These parameters are given to the physical designer to load into the Constraint Editor of the auto-router of a third-party enterprise PCB tool such as Expedition from Mentor Graphics. Once the board is routed, post-layout artwork is available in ODB++ file format.

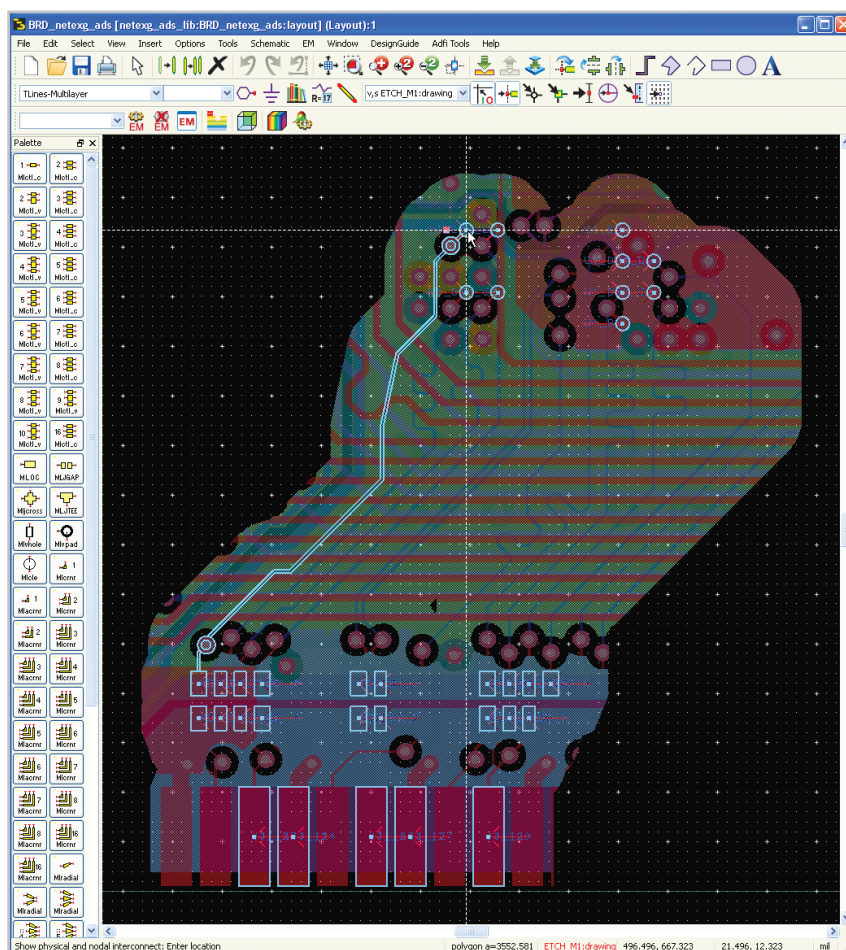


Figure 2.
One of several critical nets is highlighted in cyan. Note that this very large PCB has been “cookie cut,” with the left hand edge being a convex hull that includes this leftmost net and a margin around it.

The signal integrity engineer selects the critical nets and pre-processes the important section of the PCB for EM modeling. The resulting EM model is used to “swap out” the pre-layout placeholder with the characteristics of the actual post-layout design. In this way the candidate layout can be verified before manufacturing. If the candidate design has issues such as excessive crosstalk, the signal integrity engineer can adjust the critical area in the ADS Layout “sandbox” (for example by added stitching vias or guard traces) and solve the new candidate until a satisfactory adjustment is proven in. The physical designer then applies the knowledge from the ADS experimentation to the “golden” copy of the design in the third-party enterprise PCB tool for first pass success. This methodology avoids the expensive, time consuming, and non-deterministic “cut and try” approach to qualifying the post-layout, namely serial fabrication and measurement of multiple prototypes.

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