PathWave Test Sync Executive 2023 Programming Example 3:

PathWave Test Sync Executive integration with PathWave FPGA

KEYSIGHT

PROGRAMMING EXAMPLE

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KS2201A – Programming Example 3 – PathWave Test Sync Executive Integration with PathWave FPGA

In this programming example we show how to establish communication between a sequence of real-time instruction designed using PathWave Test Sync Executive and a custom FPGA (*Field Programmable Gate Array*) design integrated into the sandbox of a Keysight instrument using Keysight PathWave FPGA software.

Introduction

This document is organized as follows. First, a "System Setup" section explains all the mandatory software and firmware components to be installed before the programming example can run. Secondly, a "Programming Example Overview" section describes the application use case of this programming example including expected measurement results. The next section contains detailed explanations on how to use the HVI (Hard Virtual Instrument) API (Application Programming Interface) to implement the real-time algorithms of this example. Finally, the conclusions are outlined.

NOTE: Please review in detail the System Requirements outlined in the next section and install all the necessary software (SW) and firmware (FW) components before executing this programming example code.

System Setup

Please review the following system requirements and install the necessary pieces of software (SW), firmware (FW), and driver following the instructions provided in this section. To download the programming example code and necessary files please visit www.keysight.com/find/KS2201A-programming-examples . To download the latest PathWave Test Sync Executive installer and documentation, please visit www.keysight.com/find/KS2201A-downloads. The rest of the software installers, FPGA firmware, drivers, and other components mentioned in this section can be found on www.keysight.com

System Requirements

To run this series of programming examples, all the necessary pieces of SW need to be installed on the external PC or internal chassis controller that is used to control the PXI chassis. FPGA FW of PXI instruments can be instead programmed using the "Hardware Manager" window of SD1 Software Front Panel (SFP) or the "Firmware Update" window of the "Utilities" menu of the SFP of M5xxx or M9xxx instruments.

The list below refers to the whole KS2201A Prog. Examples series. Please check the next section of this document for info about the exact instrument models necessary to run this programming example. You will need to install SW and FW only for the instrument models that you are using to run this example. You do not need to install KF9000B PathWave FPGA if you are not programming your instrument FPGA with a custom design.

The versions of software, FPGA firmware, drivers, and other components that were used to test this programming example are listed below. Newer versions of the SW driver or FPGA FW used to test this example are also typically expected to work. For complete details about SW and FW compatibility please visit www.keysight.com/find/ks2201a-firmware-version-requirements.

List of **tested** versions of software, Keysight instrument drivers, and FPGA firmware:

1. Software versions:
   - Python 3.9.13 64-bit, including Python packages time, numpy, matplotlib
   - Keysight KS2201A PathWave Test Sync Executive 2023 (v3.19.2)
   - Keysight KF9000B PathWave FPGA 2022 Update 1.0 (v3.7.15.0)
2. Keysight instrument driver versions:
   - Keysight IO Libraries Suite 2023 (v18.3.29324.3)
   - Keysight PXIe Chassis Family Driver v1.7.913.1
   - Keysight M9546A High-Performance Reference Clock Source Driver v1.1.282.1

- Keysight SD1 Drivers, Libraries, and SFP v3.4.8
- Keysight M5302A Drivers, Libraries, and SFP v1.3.51002
- Keysight M5300A Drivers, Libraries, and SFP v1.1.51002
- Keysight M5200A Drivers, Libraries, and SFP v1.1.51004
- Keysight M9032A / M9033A Drivers, Libraries, and SFP v1.1.225.0

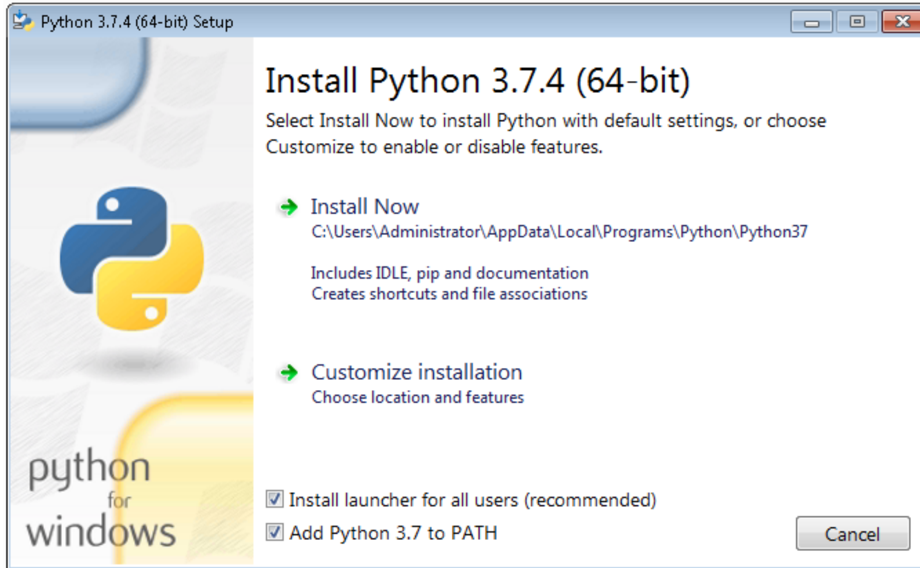
3. Keysight instrument FPGA FW versions (to be installed using Keysight instrument SFP):
   - Keysight Chassis M9019A firmware v2019EnhTrig
   - Keysight Chassis M9046A firmware v2023A
   - M3202A AWG v4.3.0
   - M3201A AWG v4.4.0
   - M3102A Digitizer v2.3.0
   - M5302A Digital I/O v5.9.42
   - M5300A RF AWG v1.1.414
   - M5200A Digitizer v1.1.409
   - M9032A System Synchronization Module v0.1.248
   - M9033A System Synchronization Module v4.1.248

NOTE The above-mentioned list of instrument drivers and firmware requirements includes all the Keysight PXIe instruments compatible with KS2201A. Please check the next section of this document for info about the exact instrument models necessary to run this programming example. Users can modify the example code to include additional compatible instruments. To run this example you need to install only the drivers of the instruments you use.

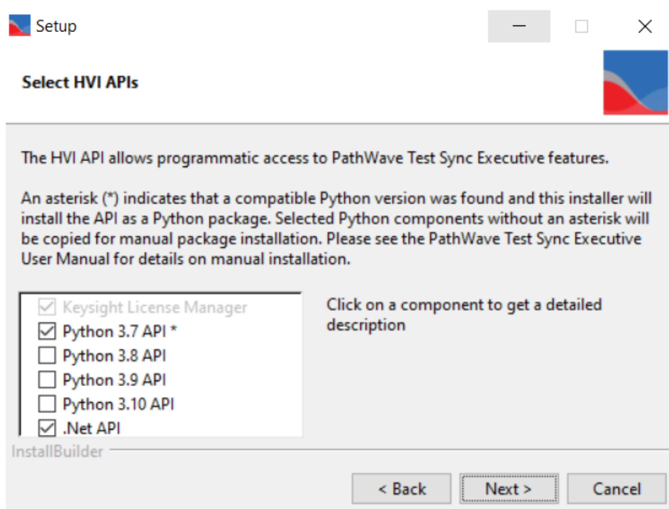
NOTE PathWave Test Sync Executive **licenses** must be installed before running the programming example Python code. To request and install a license please consult the PathWave Test Sync Executive User Manual available on www.keysight.com.

How to Install Python 3.x 64-bit

This programming example requires you to install Python 64-bit version equal to or greater than 3.7.x for all users. The Python installer can be downloaded from the Python official webpage https://www.python.org. Make sure you add Python 3.x to the PATH system Variable. This can be done at the installation step by checking the right checkboxes as shown in the screenshot below.



Once Python is installed, you can install KS2201A. When running the KS2201A installer, it will detect which Python 3.x 64-bit is installed in your system and is compatible with the `keysight_hvi` package delivered by the installer. The detected compatible version(s) will appear with a check in its checkbox. In the screenshot example below the Python 3.7 API is checked and will be installed. If you wish to install other instances of the `keysight_hvi` package, compatible with other Python 3.x 64-bit versions, then please manually check other additional checkboxes at this step of the installation procedure.



NOTE

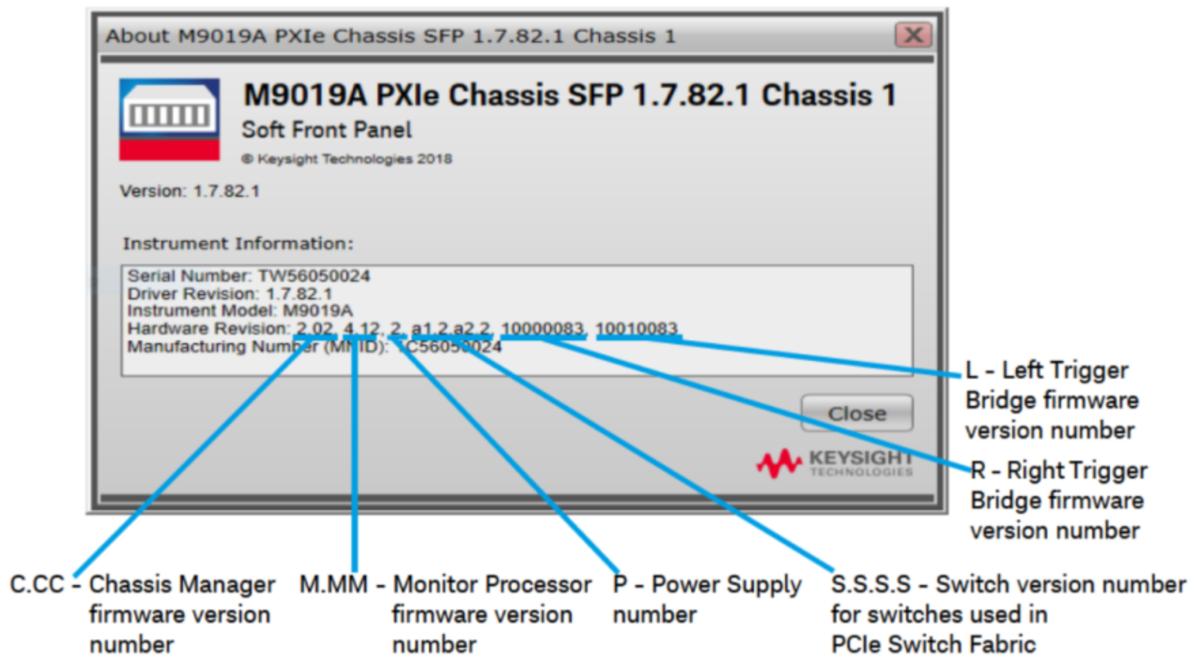
PathWave Test Sync Executive programming examples require the Python packages *time* , *numpy* and *matplotlib* . These packages can be installed using the Python package installer pip. For more information about pip and how to use it, please visit https://pypi.org/project/pip/.

NOTE

Users installing Python through a distribution that is different than the one available from the Python official webpage https://www.python.org (e.g. Anaconda distribution) need to make sure that their PATH environment Variable includes the path to set up the HVI API Python library. This can be done by adding to the programming example Python code a line that includes that path, for example: sys.path.append(C:\Program Files\Keysight\PathWave Test Sync Executive <year>\api\python) where year shall be replaced with the year of the release you are using, for example <year> = 2022.

How to Install Chassis Driver, SFP and Firmware

To ensure the system compatibility described above, please install IO Libraries and chassis driver first, both are available on www.keysight.com . This programming example was tested on chassis model M9019A using the chassis driver and chassis firmware versions listed above. If you are using another chassis model, we advise you to install the same firmware version and its compatible chassis driver. When installing the Keysight Chassis Family Driver, PXIe Chassis SFP (Software Front Panel) software is automatically installed. Chassis firmware version can be checked and updated using PXIe Chassis SFP. Please see screenshots below referring to Keysight Chassis model M9019A as an example on how to check the chassis firmware version from the info in the help window of the PXIe Chassis SFP. Chassis firmware update can be performed using the "Firmware Update" window found in the "Utilities" menu of the PXIe Chassis SFP. For more info please read PXIeChassisFirmwareUpdateGuide.pdf available on www.keysight.com.



M9019A Firmware Version Components

Firmware Component	2017	2018	2019StdTrig	2019EnhTrig
Chassis Manager	2.02	2.02	2.02	2.02
Monitor Processor	3.11	3.11	4.12	4.12
Switch version number for switches used in PCIe Switch Fabric	a1.2.a2.2	a1.2.a2.2	a1.2.a2.2	a1.2.a2.2
Right Trigger Bridge	0	10000083	0	10000083
Left Trigger Bridge	0	10010083	0	10010083

How to Install PathWave Test Sync Executive, Keysight Instrument Driver and FPGA Firmware

After installing your development environment (Python or C#), and installing the chassis, the next step is to install PathWave Test Sync Executive and the drivers for the Keysight instruments that you are using. After installing all the necessary software, the instrument FPGA firmware can be updated from their Software Front Panel (SFP) installed together with the instrument drivers. For more details on how to install SW and FPGA FW for Keysight instruments, please visit the instrument technical support page on www.keysight.com.

How to Install KF9000B PathWave FPGA

Some programming examples include PathWave FPGA project files designed using **KF9000B PathWave FPGA**. To install KF9000B and obtain a license please consult the product webpage on www.keysight.com. PathWave FPGA also requires Xilinx Vivado software to run. For further information please consult the PathWave FPGA User Manual on www.keysight.com.

Multi-Chassis System Setup using the M9032A/M9033A PXIe System Synchronization Module

In a multi-chassis system connected with Keysight PXIe System Synchronization Modules, you must include one SSM in each chassis that is part of the system. Each SSM must be inserted in the **timing slot** of your chassis. This is typically slot 10 in Keysight 18-slot chassis, but it can be a different slot number in different chassis models. The SSMs are connected to each other with System Sync cables.

One SSM is automatically chosen as a leader and it is used to synchronize all the instruments in the multi-chassis system. The SSM chosen as leader is the SSM that has no incoming connection to its System Sync Upstream port. The leader SSM distributes a replica of the reference clock signal to the SSMs located in the other chassis. It does this through point-to-point connections between System

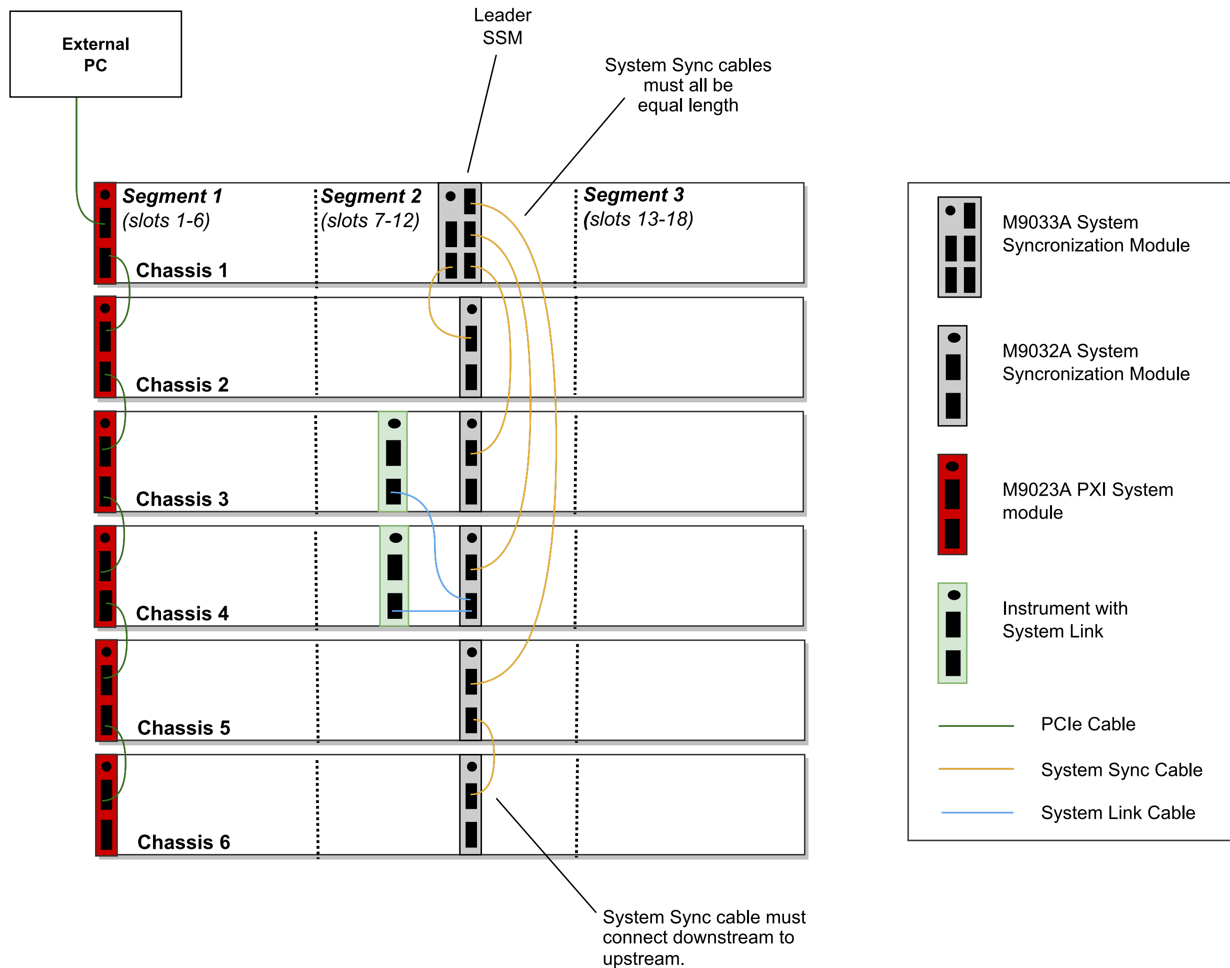
Sync Downstream/Upstream ports. In the example multi-chassis system shown in the following diagram, the leader SSM is in Chassis 1.

A multi-chassis PXIe system may be configured to use many different reference options. For a list of those options and descriptions of how to configure them, see the section *Clocking* in this document. For one of those reference options, an SSM is chosen as a leader and uses its internal Oven Controlled Crystal Oscillator (OCXO) clock to synchronize all the instruments included in the multi-chassis system.

NOTE

A Multi-chassis system based on the older M9031A modules required an external reference clock generator to distribute the precise common 10 MHz reference clock signal across different chassis. In the multi-chassis topology delivered by PathWave Test Sync Executive, the SSM assumes the function of the **reference clock signal generator/distributor**, by sharing a reference clock generated by an internal PLL. This PLL can be fed by different sources (as explained later in this document) including the OCXO inside the SSM, which generates a 10 MHz sine wave. An external 10 or 100 MHz reference signal can still be connected to the SSM SClk / Ref Input port, to sync it together with other clusters.

The following diagram shows an example of a 6 chassis system connected with SSMs. In this system an M9033A SSM in chassis 1 distributes the reference clock to four M9032A SSMs located in each of the other chassis. The SSM in chassis 5 also forwards the clock to a sixth chassis.



For further information please refer to the KS2201A System Setup Guide available on www.keysight.com/find/KS2201A-downloads.

Programming Example Overview

This programming example illustrates the following functionalities:

1. Read/write data from/to an HVI sequence to/from an HVI Memory Map inserted in an instrument FPGA sandbox.
2. Read/write data from/to an HVI sequence to/from an HVI Register bank inserted in an instrument FPGA sandbox.
3. Read/write PXI line values through instrument FPGA sandbox.
4. Usage of HVI Actions and Events to communicate with an instrument FPGA sandbox.

These functionalities are implemented using the combination of Keysight PathWave Test Sync Executive and Keysight PathWave FPGA software.

How to Run this Programming Example

This programming example is set up to execute in simulation mode. To execute the Python code on real HW instruments, change the option for simulated hardware to False:

```
# Simulated HW Option
hardware_simulated = True
```

Afterward, it is necessary to specify the actual chassis number and slot number where the real PXI instruments are located. Update the model numbers of the PXI instruments used, if they are different than the instrument models used in this programming example. This example uses PXI instruments from the Keysight M3xxx family. The first step to control such instruments is to create an object using the open() method from the SD1 API. For a complete description of the SD1 API open() method and its options please consult the SD1 3.x Software for M320xA / M330xA Arbitrary Waveform Generators User's Guide.

Each PXI instrument is described in the code using a module description class that contains the module model number, chassis number, slot number and options. Chassis and slot number in the code snippet below must be updated before running the programming example:

```
"""
Define HW Platform
"""
# Define module descriptors below with your instruments information
self.module_descriptors = [
    ModuleDescriptor('M3202A', 2, 4, self.options, self.leader_engine),
    ModuleDescriptor('M3202A', 2, 10, self.options, self.follower_engine)]

class ModuleDescriptor:
"Descriptor for module objects"
def __init__(self, model_number, chassis_number, slot_number, options, engine_name):
self.model_number = model_number
self.chassis_number = chassis_number
self.slot_number = slot_number
self.options = options
self.engine_name = engine_name
```

The chassis to be used in the programming example must be specified and listed by chassis number:

```
# Update list of chassis numbers included in the programming example
self.chassis_list = [1, 2]
```

In the case of a multi-chassis setup, define each System Sync Module and its connections:

```
# Multi-chassis setup
# Define the System Sync Modules included in your system.
self.ssm_options = ''
self.ssm_simulation_options = 'Simulate=true,DriverSetup=Model=M9033A'
self.system_sync_modules_descriptors = [
    SystemSyncModuleDescriptor('PXI0::CHASSIS1::SLOT10::INDEX0::INSTR', self.ssm_options),
    SystemSyncModuleDescriptor('PXI0::CHASSIS2::SLOT10::INDEX0::INSTR', self.ssm_options)]
# For each SSM define which SSM is connected to its downstream connectors.
# Each connectivity item is a triple (ssm1_chassis, ssm1_downstream_connector_number, ssm2_
chassis)
self.ssm_connections = [
    SystemSyncModuleConnection(ssm1_chassis=1, ssm1_downstream_connector_number=1, ssm2_
chassis=2)]
```

Please note that in every programming example, PXI trigger resources need to be reserved so that the HVI instance can use them for their execution. PXI lines to be assigned as trigger resources to HVI can be selected by updating the code snippet below:

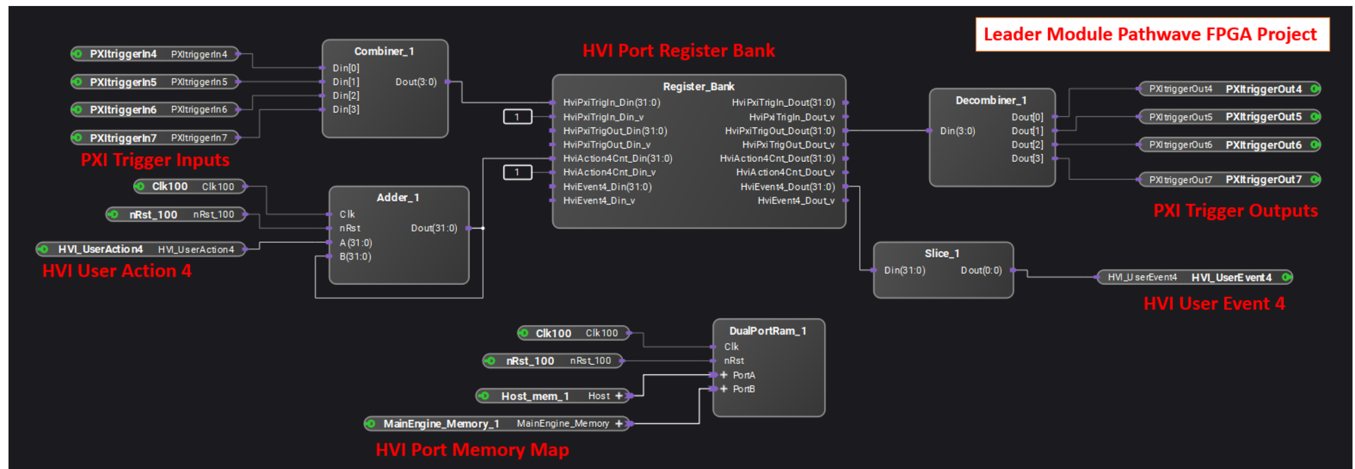
```
# Assign triggers to HVI object to be used for HVI-managed synchronization, data sharing, etc #
NOTE: In a multi-chassis setup ALL the PXI lines listed below need to be shared among each M9031
board pair by means of SMB cable connections
self.pxi_sync_trigger_resources = [ kthvi.TriggerResourceId.PXI_TRIGGER0,
kthvi.TriggerResourceId.PXI_TRIGGER1, kthvi.TriggerResourceId.PXI_TRIGGER2,
kthvi.TriggerResourceId.PXI_TRIGGER3]
```

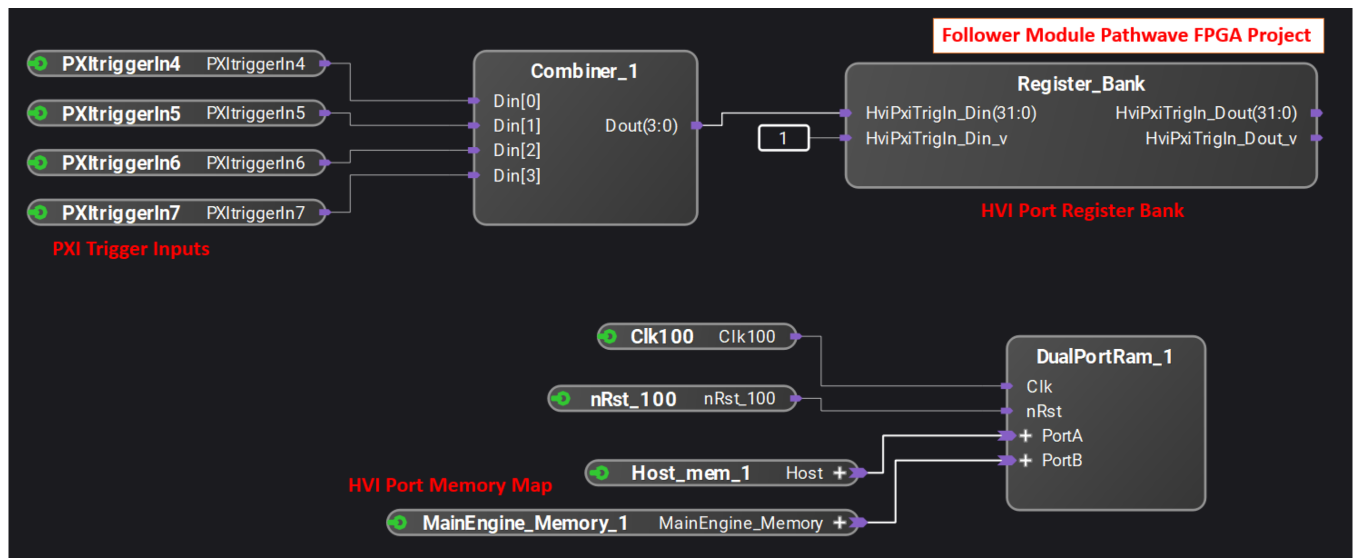
PXI lines allocated to be used as HVI trigger resources cannot be used by the programming example for other purposes. The vector pxi_sync_trigger_resources specified above must include at least the necessary number of PXI lines for the programming example to execute. Please check the programming example code for the actual number of PXI lines that needs to be reserved. The HVI compiler also returns, for a given HVI sequence, the number of necessary PXI lines that must be reserved.

In this programming example, PXI lines 4-7 are used to exchange information between leader and follower modules through the instrument FPGA sandbox. Therefore, PXI lines 4-7 cannot be added as HVI PXI trigger resources in the code snippet above.

PathWave FPGA Project

This programming example is based on the implementation of custom blocks within the FPGA sandbox of both the leader and follower modules. The pictures below illustrate the PathWave FPGA projects for the leader module and follower module respectively.





In the pictures above we can distinguish the following blocks:

- HVI Memory Map: This block enables the exchange of data between an HVI sequence and an instrument FPGA sandbox by using a serial interface based on reading/writing data arrays.
- HVI Register Bank: This block enables the exchange of data between an HVI sequence and an instrument FPGA sandbox by reading/writing any of the registers in the bank.

- PXI Trigger I/O : These ports enables reading/writing of the PXI line on the chassis backplane from the FPGA sandbox of an M3xxx instrument.
- HVI User Action : Actions are signals sent from an instrument HVI engine to the outside (the FPGA sandbox in this case). They can be associated with a PXI line, an internal/external trigger, or any of the product-defined actions.
- HVI User Event : Events are signals sent from the outside (the FPGA sandbox in this case) to an instrument HVI engine. They can be associated with a PXI line, an internal/external trigger, or any of the product-defined events.

PathWave FPGA project files provided with this programming example are targeting M3202A AWG model. However, projects can be easily adapted to target different M3xxx PXI instruments. This re-targeting functionality is explained in the PathWave FPGA User Guide . For a complete overview of Keysight PathWave FPGA and more information about all its functionalities please visit www.keysight.com.

Measurement Results

When the Python application code correctly executes, it shows a list of registers and memory blocks that are loaded to FPGA sandbox of both leader and follower engines when loading the .k7z files generated by compiling the PathWave FPGA projects described in the previous sub-section of this document. Afterward, the HVI sequence starts to execute and waits for the user to trigger a user event, it executes a user action (user action 4) each time the user hits the enter key. The executed FPGA sandbox actions are counted at each iteration. Another counter starting from 1000 is incremented and read back after writing it to a dual port RAM. The user action counter value is written to PXI lines value so that it can also be read by the follower module.

User events and actions available in an instrument FPGA sandbox depends on the specific instrument capability and are documented in the instrument documentation and user guides. In particular, documentation of user action 4 and user event 4 used in this programming example (represented by blocks "HVI_UserAction4" and "HVI_UserEvent4" in the leader module PathWave FPGA project) can be found in the *M32xxA Arbitrary Waveform Generators User's Guide*.

A more detailed programming example execution is described as follows. Within the *Sync Multi-Sequence Block* (SMSB) 'FPGA Read/Write Operations', all the four type of possible read/write operation to/from an FPGA sandbox register or memory map are performed. HVI register and HVI memory maps are part of the PathWave FPGA blockset "RealTime HVI" and they are described in details in the PathWave FPGA User Manual. The first statements reads a register in the FPGA sandbox (register 'Register_Bank_HviAction4Cnt' in the PathWave FPGA project) that is connected to a counter of user action 4 instances. The value is read into an HVI register named 'Action4 Counter'. The subsequent FPGA write operation writes the user action 4 counter value into an FPGA register connected to PXI lines 4-7 outputs. This way the user action 4 counter value is written to PXI lines with a resolution of 4 bits. The following two statements validate the memory map read/write by first writing the value of a register counter called 'Memory Map Counter' into the memory map (block "MainEngine_Memory1" in the PathWave FPGA projects) and then reading it back. The counter starts from 1000 and users can verify the counter value is written and read back correctly from the memory map during the example execution. Due to the 4 bits resolution the counters reading the values written to the PXI lines are reset every time the counting reaches a multiple of 16.

The next SMSB contains a register read operation in both local HVI sequences of leader and follower instruments. Both leader and follower modules have a register in their sandbox that is connected to PXI lines 4-7 inputs in the sandbox. This way both modules can read the PXI line's values through that register, and hence can read the user action 4 counter value that was previously written in those lines. The HVI sequence then waits for an user event 4 which can be generated by the user by pressing Enter from the console. Once the user event 4 is received, the HVI sequence triggers an user action 4 instance that is counted by the counter register connected to the user action 4 input in the sandbox.

Finally in the last SMSB of the HVI sequence, all the HVI register counters are incremented. The registers value increments are printed out on the console terminal at each iteration of the programming example. See the screenshot below as an example of the programming example execution on the console terminal.

OUTPUT TERMINAL DEBUG CONSOLE PROBLEMS

```
Register size [bytes]: 4096
Register address offset [bytes]: 0
Register access: MemoryMap
Register name: MainEngine_Memory_1
Register size [bytes]: 1024
Register address offset [bytes]: 0
Register access: MemoryMap
Register name: Register_Bank_HviPxiTrigIn
Register size [bytes]: 1
Register address offset [bytes]: 1024
Register access: RW
Register name: Register_Bank_HviPxiTrigOut
Register size [bytes]: 1
Register address offset [bytes]: 1025
Register access: RW
Register name: Register_Bank_HviAction4Cnt
Register size [bytes]: 1
Register address offset [bytes]: 1026
Register access: RW
Register name: Register_Bank_HviEvent4
Register size [bytes]: 1
Register address offset [bytes]: 1027
Register access: RW

Registers contained in Secondary Module:
Register name: Host_mem_1
Register size [bytes]: 4096
Register address offset [bytes]: 0
Register access: MemoryMap
Register name: Register_Bank_PC_PxiTrigIn
Register size [bytes]: 4
Register address offset [bytes]: 4096
Register access: RW
Register name: MainEngine_Memory_1
Register size [bytes]: 1024
Register address offset [bytes]: 0
Register access: MemoryMap

-------------------
System Definition
-------------------
The PathWave Test Sync Executive API installed on your system has an HVI core version 1.15.3

HW Instruments:
- Model: M3202A in chassis: 1, slot: 14, HVI Engine Name: PrimaryEngine, HVI core version: 1.14.2, HVI Engine FPGA IP version: 1.6.0
- Model: M3202A in chassis: 1, slot: 15, HVI Engine Name: SecondaryEngine, HVI core version: 1.14.2, HVI Engine FPGA IP version: 1.6.0
System Sync Modules:
- System Sync Module in chassis: 1, slot: 10 with 1 Upstream Ports and 4 Downstream Ports
```

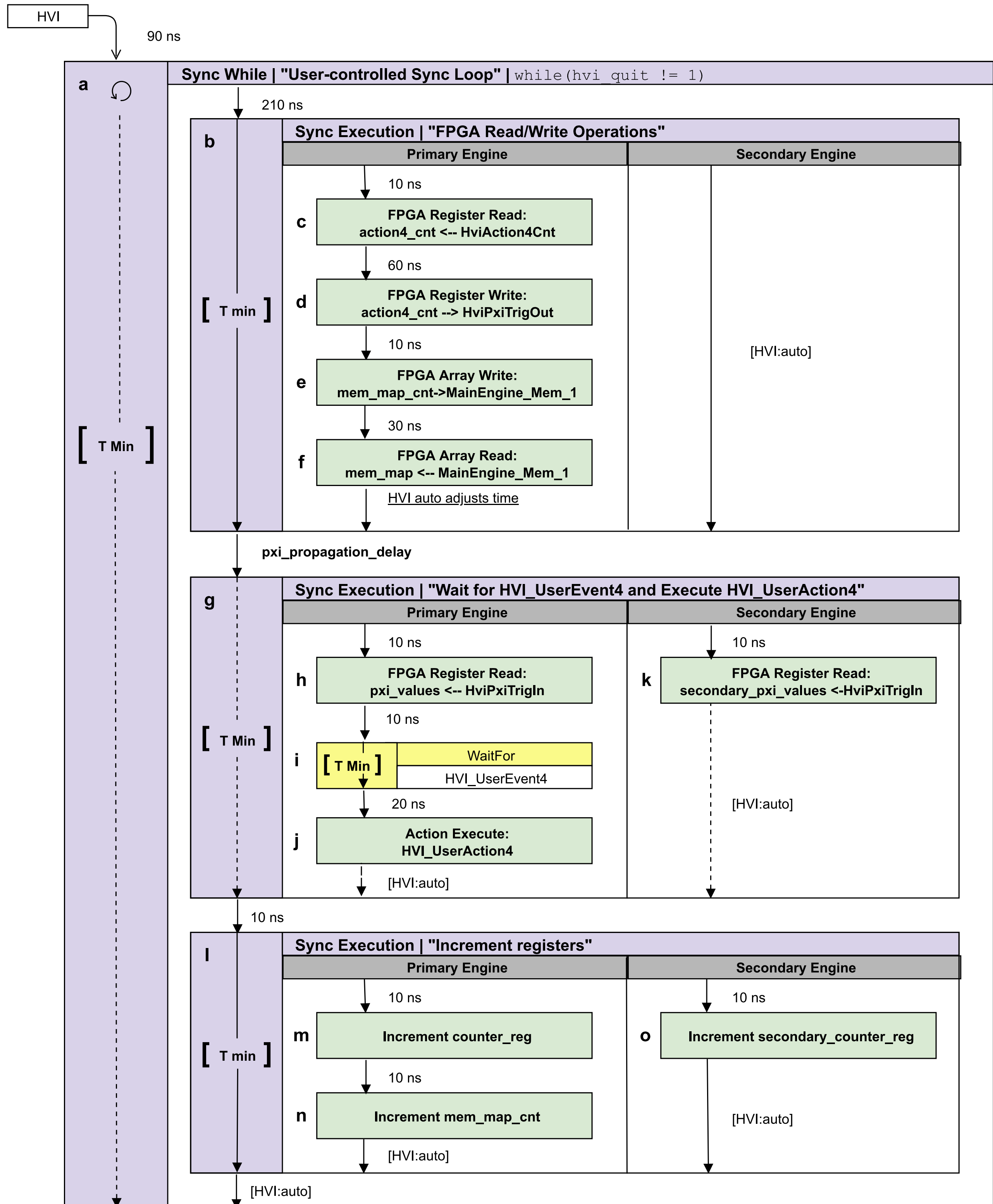
```
----------------------
Program HVI Sequences
----------------------
Initializing the defined system...
Programming the HVI sequences...
Programmed HVI sequences exported to file
-------------------
Execute HVI
-------------------
Compiling HVI...

HVI Compiled
This HVI needs to reserve 2 PXI trigger resources to execute
HVI Loaded to HW
HVI Running...
N. of User Actions counted at primary module: action4_cnt = 0
Value written to the FPGA Memory Map: mem_map = 1000
Value read by Primary Module from FPGA PXI inputs: pxi_values = 0
Value read by Secondary Module from FPGA PXI inputs: secondary_pxi_values = 0
Counter value: counter_reg = 0
Secondary counter value: secondary_counter_reg = 0
Mem. Map counter value: mem_map_counter_reg = 1000
Press enter to trigger a User Event and execute a User Action, press q to exit

N. of User Actions counted at primary module: action4_cnt = 1
Value written to the FPGA Memory Map: mem_map = 1001
Value read by Primary Module from FPGA PXI inputs: pxi_values = 1
Value read by Secondary Module from FPGA PXI inputs: secondary_pxi_values = 1
Counter value: counter_reg = 1
Secondary counter value: secondary_counter_reg = 1
Mem. Map counter value: mem_map_counter_reg = 1001
Press enter to trigger a User Event and execute a User Action, press q to exit

N. of User Actions counted at primary module: action4_cnt = 2
Value written to the FPGA Memory Map: mem_map = 1002
Value read by Primary Module from FPGA PXI inputs: pxi_values = 2
Value read by Secondary Module from FPGA PXI inputs: secondary_pxi_values = 2
Counter value: counter_reg = 2
Secondary counter value: secondary_counter_reg = 2
Mem. Map counter value: mem_map_counter_reg = 1002
Press enter to trigger a User Event and execute a User Action, press q to exit
q
Releasing HW...
Modules closed
```

The example measurement results shown in the execution screenshot above can be measured on an oscilloscope as well, by using an M9031A module to connect the PXI lines 4-7 to oscilloscope channels and visualize their value update at each iteration of the programming example execution. The next section of this document provides further details about the HVI sequences executed and each HVI statement contained in them.

HVI Application Programming Interface (API): Detailed Explanations

PathWave Test Sync Executive implements the next generation of HVI technology and delivers the HVI Application Programming Interface (API). This section explains how to implement the use case of this programming example using HVI API. The sequence of operations executed by each of the instruments using HVI technology is explained in the diagram below. The diagram depicts the HVI sequences executed within this programming example and the HVI statements used to program the sequences. Every HVI statement is described in detail later in this section, referencing with a letter the equivalent block in the HVI diagram and explaining in detail the corresponding HVI API code block and the HVI functionalities that it implements.

Please note that the start delays of HVI statement inserted in the following HVI diagram are set to very specific values. Unless differently specified, those values correspond to the minimum latencies that can be used for those start delays. Please consult Chapter 7 of the PathWave Test Sync Executive User Manual for detailed information about the timing constraint and latency of each HVI statement execution.



NOTE: 10 ns is the FPGA clock period for M3xxxA instruments

NOTE The duration of each iteration of the Sync While loop used in this example is unknown due to the unknown execution time of the Wait statement used inside the loop. The unknown duration is represented by the dotted arrows in the HVI diagram. Due to its unknown duration, it is not possible to use the Sync While duration property to specify how long each loop iteration should last.

NOTE Fixed delays can be parametrized in HVI sequences by using Python Variables. For example, the Python Variable *pxi_propagation_delay* is used to parametrize the start delay between the synchronized multi-sequence blocks "FPGA Read/Write operations" and "Wait for HVI_UserEvent4 and Execute HVI_UserAction4". Thie *pxi_propagation_delay* is necessary to allow enough time for the Action4 counter register to write its value to the PXI lines, before the leader and follower modules try to read that same value. This way we ensure the value read is up to date.

To implement a Variable delay in an HVI sequence, the WaitTime statement shall be used instead. More information can be found in the KS2201A User Manual.

To include HVI in an application, follow these three fundamental steps:

1. System definition: define all the necessary HVI resources, including platform resources, engines, triggers, registers, actions, events, etc.
2. Program HVI sequences: define all the statements to be executed within each HVI sequence
3. Execute HVI: compile, load to HW and execute the HVI

The following sub-sections describe in detail how these three steps are implemented for this example. For further explanations about any of the concepts, please refer to the PathWave Test Sync Executive User Manual .

System Definition

The definition of HVI resources is the first step of an application using HVI. The API class *SystemDefintion* enables you to define all necessary HVI resources. HVI resources include all the platform resources, engines, triggers, registers, actions, events, etc. that the HVI sequences are going to use and execute. Users need to declare them up front and add them to the corresponding collections. All HVI Engines included in the programming need to be registered into the *EngineCollection* class instance. HVI resources are described in detail in the PathWave Test Sync Executive User Manual . The HVI resource definitions are summarized in the code snippets below.

Python

```
# Create system definition object
my_system = kthvi.SystemDefinition("MySystem")


def define_hvi_resources(sys_def, module_dict, config):
    """
    Configures all the necessary resources for the HVI application to execute: HW platform,
engines, actions, triggers, etc.
    """
    # Define HW platform: chassis, interconnections, PXI trigger resources, synchronization, HVI
clocks
    define_hw_platform(sys_def, config)
    # Define all the HVI engines to be included in the HVI
    define_hvi_engines(sys_def, module_dict)
    # Define FPGA actions, events and other configurations
    define_fpga_resources(sys_def, module_dict, config)
```

Define Platform Resources: Chassis, PXI triggers, Synchronization

All HVI instances need to define the chassis and eventual chassis interconnections using the *SystemDefinition* class. System Sync Modules can be defined using the *add_sync_module* method of the interconnects interface. PXI trigger lines to be reserved by HVI for its execution can be assigned using the *sync_resources* interface of the *SystemDefinition* class. The *SystemDefinition* class also allows you to add additional clock frequencies that the HVI execution can synchronize with. For further information, please consult the section "HVI Core API" of the PathWave Test Sync Executive User Manual .

```
def define_hw_platform(sys_def, config):
    """
    Define HW platform: chassis, interconnections, PXI trigger resources, synchronization, HVI
clocks
    """
    # Define chassis resources
    # For multi-chassis setup details see programming example documentation
    for chassis_number in config.chassis_list:
        if config.hardware_simulated:
# This simulation options require to install the chassis driver:
# sys_def.chassis.add_with_options(chassis_number, 'Simulate=True,DriverSetup=Model=M9019A')
# As an alternative, the GenericPxieChassis allows to run simulations without installing the
chassis driver
            sys_def.chassis.add(chassis_number,
'Simulate=True,DriverSetup=Model=GenericPxieChassis')
        else:
            sys_def.chassis.add(chassis_number)

# Define System Sync Modules (SSMs)
    if config.system_sync_modules_descriptors:
        interconnects = sys_def.interconnects
        ssm_list = []
        for descriptor in config.system_sync_modules_descriptors:
            if config.hardware_simulated:
                ssm = interconnects.add_sync_module(descriptor.resource_id, config.ssm_
simulation_options)
            else:
                ssm = interconnects.add_sync_module(descriptor.resource_id, descriptor.options)
            ssm_list.append(ssm)
```

```
# Define connections between SSMs
if config.ssm_connections:
    for connection in config.ssm_connections:
        connector_number = connection.ssm1_downstream_connector_number
        for ssm in ssm_list:
            if ssm.chassis == connection.ssm1_chassis:
                ssm1 = ssm
            if ssm.chassis == connection.ssm2_chassis:
                ssm2 = ssm
        # Implement each user-defined connection
        try:
            # Set connection. SSMs have always one upstream port
            ssm1.connectivity.systemsync_downstream[connector_number].set_connection
(ssm2.connectivity.systemsync_upstream[1])
        except:
            exit("Exception! Please check the valued defined for SyncModule resource ids,
chassis numbers and connections")

    # Assign the defined PXI trigger resources
    sys_def.sync_resources = config.pxi_sync_trigger_resources
    # Assign clock frequencies that are outside the set of the clock frequencies of each HVI
engine
    # Use the code line below if you want the application to be in sync with the 10 MHz clock
    sys_def.non_hvi_core_clocks = [10e6]
```

Define HVI Engines

All the HVI Engines to be included in the HVI instance must be registered into the *EngineCollection* class instance. Each HVI Engine object added to the engine collection contains collections of its own that enable you to access the actions, events and triggers that each specific engine will control and use within the HVI.

Python

```
"""
Define names of HVI engines, actions, events, triggers, registers
"""
# HVI engine names
self.leader_engine = "LeaderEngine"
self.follower_engine = "FollowerEngine"



def define_hvi_engines(sys_def, module_dict):
    # Define all the HVI engines to be included in the HVI
    # For each instrument to be used in the HVI application add its HVI Engine to the HVI Engine
Collection
    for engine_name, module in zip(module_dict.keys(), module_dict.values()):
        sys_def.engines.add(module.instrument.hvi.engines.main_engine, engine_name)
```

Define HVI Actions, Events, Triggers

In this programming example, each AWG needs to trigger both an FP pulse and a waveform very precisely. To do this, the AWG trigger actions are issued from within the HVI execution. In the HVI use model, actions need to be added to the action collection of each HVI engine before they can be executed. FP trigger needs to be added to the HVI Trigger Collection and configured. The code snippets below show how this is done in this programming example.

Python

```
# HVI events and actions
self.hvi_user_event_4 =  "FpgaUserEvent4"
self.hvi_user_action_4 = "FpgaUserAction4"

"""
Define names of FPGA sandbox resources
"""
# Bitstream files generated by compiling PathWave FPGA project files
self.leader_project_file = "../bitfiles/HviPortExampleLeader.k7z"
self.follower_project_file = "../bitfiles/HviPortExampleFollower.k7z"
# Sandbox name defined by each instrument. See SD1 3.x User Guide for further info
self.M3xxx_sandbox = "sandbox0" # The M3xxx_sandbox name is not arbitrary and cannot be changed
# FPGA Sandbox resource names
# NOTE The FPGA resource names are not arbitrary. They correspond to the names defined in the
PathWave FPGA project files
self.num_leader_regs = 6 # number of mem. maps and registers placed in the leader PathWave FPGA
project
self.num_follower_regs = 3 # number of mem. maps and registers placed in the follower PathWave
FPGA project
self.memory_map = "MainEngine_Memory_1"
self.reg_action4_cnt = "Register_Bank_HviAction4Cnt"
self.reg_event4 = "Register_Bank_HviEvent4"
self.reg_pxi_out = "Register_Bank_HviPxiTrigOut"
self.reg_pxi_in = "Register_Bank_HviPxiTrigIn"
self.follower_reg_pxi_in = "Register_Bank_HviPxiTrigIn"

def define_fpga_resources(sys_def, module_dict, config):
    """
    Define FPGA actions, events and other configurations
    """
    # Leader module, follower module
    leader_module = module_dict[config.leader_engine].instrument
    follower_module = module_dict[config.follower_engine].instrument
    # Events: add FpgaUserEvent4 to the list of events of the leader engine
    fpga_user_event4 = leader_module.hvi.events.fpga_user_4
    sys_def.engines[config.leader_engine].events.add(fpga_user_event4, config.hvi_user_event_4)
    # Actions: add FpgaUserAction4 to the list of actions of the leader engine
    fpga_user_action4 = leader_module.hvi.actions.fpga_user_4
    sys_def.engines[config.leader_engine].actions.add(fpga_user_action4, config.hvi_user_action_
4)
    # Get engine sandbox
    sandbox_name = config.M3xxx_sandbox
```

```
    leader_sandbox = sys_def.engines[config.leader_engine].fpga_sandboxes[sandbox_name]
    follower_sandbox = sys_def.engines[config.follower_engine].fpga_sandboxes[sandbox_name]
    # Load to the sandboxes .k7z project created using Pathwave FPGA
    # This operation is necessary for HVI to list all the FPGA blocks contrined in the designed
FPGA FW
    leader_sandbox.load_from_k7z(config.leader_project_file)
    follower_sandbox.load_from_k7z(config.follower_project_file)
    # Enable PXI lines to be written from the FPGA sandbox of leader engine only using
FPGATriggerOutConfig()
    # NOTE: Only one PXI module per segment shall be allowed to write backplane PXI lines. It
would cause conflicts and misbehavior to configure the PXI lines for the follower engine also
    leader_module.FPGATriggerConfig(externalSource=keysightSD1.SD_
TriggerExternalSources.TRIGGER_PXI4, direction =keysightSD1.SD_FpgaTriggerDirection.INOUT,
polarity= keysightSD1.SD_TriggerPolarity.ACTIVE_LOW, syncMode = keysightSD1.SD_SyncModes.SYNC_
NONE, delay5Tclk=0)
    leader_module.FPGATriggerConfig(externalSource=keysightSD1.SD_
TriggerExternalSources.TRIGGER_PXI5, direction =keysightSD1.SD_FpgaTriggerDirection.INOUT,
polarity= keysightSD1.SD_TriggerPolarity.ACTIVE_LOW, syncMode = keysightSD1.SD_SyncModes.SYNC_
NONE, delay5Tclk=0)
    leader_module.FPGATriggerConfig(externalSource=keysightSD1.SD_
TriggerExternalSources.TRIGGER_PXI6, direction =keysightSD1.SD_FpgaTriggerDirection.INOUT,
polarity= keysightSD1.SD_TriggerPolarity.ACTIVE_LOW, syncMode = keysightSD1.SD_SyncModes.SYNC_
NONE, delay5Tclk=0)
    leader_module.FPGATriggerConfig(externalSource=keysightSD1.SD_
TriggerExternalSources.TRIGGER_PXI7, direction =keysightSD1.SD_FpgaTriggerDirection.INOUT,
polarity= keysightSD1.SD_TriggerPolarity.ACTIVE_LOW, syncMode = keysightSD1.SD_SyncModes.SYNC_
NONE, delay5Tclk=0)
    follower_module.FPGATriggerConfig(externalSource=keysightSD1.SD_
TriggerExternalSources.TRIGGER_PXI4, direction =keysightSD1.SD_FpgaTriggerDirection.IN,
polarity= keysightSD1.SD_TriggerPolarity.ACTIVE_LOW, syncMode = keysightSD1.SD_SyncModes.SYNC_
NONE, delay5Tclk=0)
    follower_module.FPGATriggerConfig(externalSource=keysightSD1.SD_
TriggerExternalSources.TRIGGER_PXI5, direction =keysightSD1.SD_FpgaTriggerDirection.IN,
polarity= keysightSD1.SD_TriggerPolarity.ACTIVE_LOW, syncMode = keysightSD1.SD_SyncModes.SYNC_
NONE, delay5Tclk=0)
    follower_module.FPGATriggerConfig(externalSource=keysightSD1.SD_
TriggerExternalSources.TRIGGER_PXI6, direction =keysightSD1.SD_FpgaTriggerDirection.IN,
polarity= keysightSD1.SD_TriggerPolarity.ACTIVE_LOW, syncMode = keysightSD1.SD_SyncModes.SYNC_
NONE, delay5Tclk=0)
    follower_module.FPGATriggerConfig(externalSource=keysightSD1.SD_
TriggerExternalSources.TRIGGER_PXI7, direction =keysightSD1.SD_FpgaTriggerDirection.IN,
polarity= keysightSD1.SD_TriggerPolarity.ACTIVE_LOW, syncMode = keysightSD1.SD_SyncModes.SYNC_
NONE, delay5Tclk=0)
```

Program HVI Sequence

Once the HVI resources are defined, you can program the HVI sequence of measurement actions to be executed by each HVI engine. HVI sequences can be programmed using the *Sequencer* class. HVI execution happens through a global sequence (defined by the *SyncSequence* class) that takes care of synchronizing and encapsulating the local sequences corresponding to each HVI engine included in the application. In this programming example, the HVI global sync sequence consists of a synchronized while statement containing three synchronized multi-sequence blocks.

Python

```
# Create sequencer object
sequencer = kthvi.Sequencer("MySequencer", my_system)
```

```
def program_fpga_interaction_sequence(sequencer, config):
    """
    This method programs the HVI sequence of this application.
    Different HVI statements are encapsulated as much as possible in separated SW methods to
help users visualize
    the programmed HVI sequences.
    The programming example documentation on www.keysight.com contains an HVI diagram that
graphically represents the programmed HVI sequence.
    """
    # Define registers within the scope of the outmost sync sequence
    define_registers(sequencer, config)
    # Define Sync While condition
    hvi_quit = sequencer.sync_sequence.scopes[config.leader_engine].registers[config.hvi_quit]
    sync_while_condition = kthvi.Condition.register_comparison(hvi_quit,
kthvi.ComparisonOperator.NOT_EQUAL_TO, 1)
    # Add Sync While statement
    sync_while = sequencer.sync_sequence.add_sync_while("User-controlled sync loop", 90, sync_
while_condition)
    # Program sync loop
    program_sync_loop(sync_while.sync_sequence, config)
```

Define HVI Registers

HVI registers correspond to very fast access physical memory registers in the HVI Engine located in the instrument HW (e.g. FPGA or ASIC). HVI Registers can be used as parameters for operations and modified during the sequence execution (same as Variables in any programming language). The number and size of registers is defined by each instrument. The registers that users want to use in the HVI sequences need to be defined beforehand into the register collection within the scope of the corresponding HVI Sequence. This can be done using the RegisterCollection class that is within the Scope object corresponding to each sequence. HVI Registers belong to a specific HVI Engine because they refer to HW registers of that specific instrument. Registers from one HVI Engine cannot be used by other engines or outside of their scope. Note that currently, registers can only be added to the HVI top SyncSequence scopes, which means that only global registers visible in all child sequences can be added. HVI registers are defined in this programming example by the code snippet below.

Python

```
# HVI register names
self.hvi_quit = "HVI Quit"
self.action4_cnt = "Action4 Counter"
self.counter_reg = "Loop Counter"
self.mem_map = "Memory Map Value"
self.mem_map_counter = "Memory Map Counter"
self.pxi_values = "PXI Values"
self.follower_pxi_values = "Follower PXI Values"
self.follower_counter_reg = "Follower Counter"



def define_registers(sequencer, config):
    """
    Defines all registers for each HVI engine in the scope af the global sync sequence
    """
    # Define registers for leader engine
    leader_engine_register_collection = sequencer.sync_sequence.scopes[config.leader_
engine].registers
    hvi_quit = leader_engine_register_collection.add(config.hvi_quit, kthvi.RegisterSize.SHORT)
    hvi_quit.initial_value = 0
    action4_cnt = leader_engine_register_collection.add(config.action4_cnt,
kthvi.RegisterSize.SHORT)
    action4_cnt.initial_value = 0
    counter_reg = leader_engine_register_collection.add(config.counter_reg,
kthvi.RegisterSize.SHORT)
    counter_reg.initial_value = 0
    mem_map = leader_engine_register_collection.add(config.mem_map, kthvi.RegisterSize.SHORT)
    mem_map.initial_value = 0
    mem_map_counter = leader_engine_register_collection.add(config.mem_map_counter,
kthvi.RegisterSize.SHORT)
    mem_map_counter.initial_value = 1000
```

```
    pxi_values = leader_engine_register_collection.add(config.pxi_values,
kthvi.RegisterSize.SHORT)
    pxi_values.initial_value = 0
    # Define registers for leader engine
    follower_engine_register_collection = sequencer.sync_sequence.scopes[config.follower_
engine].registers
    follower_counter_reg = follower_engine_register_collection.add(config.follower_counter_reg,
kthvi.RegisterSize.SHORT)
    follower_counter_reg.initial_value = 0
    follower_pxi_values = follower_engine_register_collection.add(config.follower_pxi_values,
kthvi.RegisterSize.SHORT)
    follower_pxi_values.initial_value = 0
```

Synchronized While

This corresponds to statement (a) in the HVI diagram. Synchronized While (Sync While) statements belongs to the set of HVI Sync Statements and are defined by the API class *SyncWhile*. A Sync While enables you to synchronously execute multiple local HVI sequences until a user-defined condition is met, that is, the sync while condition. For local sequences to be defined within the Sync While, it is necessary to use synchronized multi-sequence blocks.

Python

```
# Define sync while condition
sync_while_condition = kthvi.Condition.register_comparison(hvi_quit,
kthvi.ComparisonOperator.NOT_EQUAL_TO, 1)
# Add Sync While Statement
sync_while = sync_sequence.add_sync_while('User-controlled sync loop', 90, sync_while_condition)
```

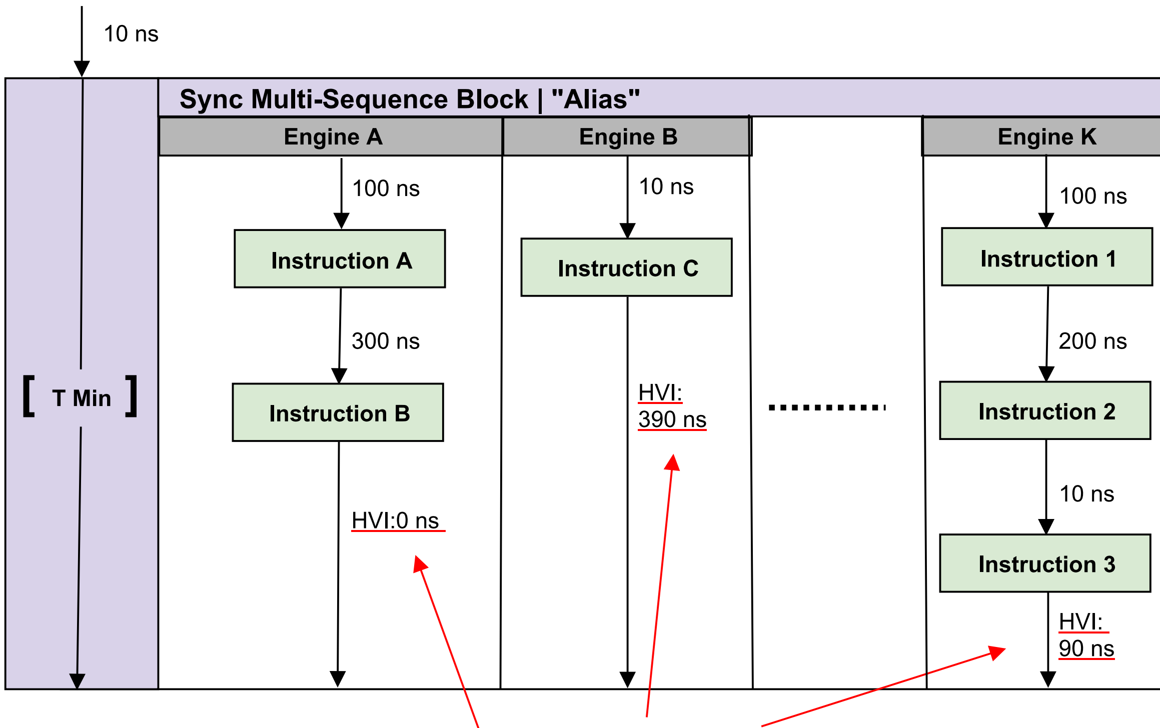
Synchronized Multi-Sequence Block

This corresponds to statements (b, g, l) in the HVI diagram. Synchronized multi-sequence blocks are defined by the API class *SyncMultiSequenceBlock*. This type of Sync statement synchronizes all the HVI engines that are part of the sync sequence. It allows you to program each HVI Engine to do specific operations by exposing a local sequence for each engine. By calling the API method *add_multi_sequence_block()*, a synchronized multi-sequence block is added to the Sync (global) Sequence.

Python

```
# Add 1st Sync Multi-Sequence Block to the Sync While sequence
sync_block_1 = sync_sequence.add_sync_multi_sequence_block('FPGA Read/Write Operations', 210)
```

Within the Synchronized Multi-Sequence Block (SMSB), users can define which statement each local engine is going to execute in parallel with the other engines. Local HVI sequences start and end synchronously their execution within the sync multi-sequence block. Users can define the exact amount of time each local HVI statement starts to execute with respect to the previous one. HVI automatically calculates the execution time of each local sequence and adjusts the execution of all local sequences within the multi-sequence block so that they can deterministically end altogether within the synchronized multi-sequence block. See the general case example in the figure below for additional details.



Please note that the Sync Multi-Sequence Block has an execution duration time labeled as "T Min" in the figure above. The "T Min" default value for any sync statement corresponds to the minimum time necessary to complete the operations included inside. KS2201A Update 1.0 release provides the *Duration* property in Sync Statement objects that allows users to set an arbitrary duration value larger than "T Min". The timing at the end of each local sequence is automatically adjusted by HVI according to the duration specified by the user for the SMSB. In the case of duration "T min", HVI will automatically add no time to the local sequence with the longest duration and adjust the other sequences accordingly, as in the example depicted in the figure above. The resolution for HVI-defined time adjustment at the end of a sync multi-sequence block corresponds to the 10 ns FPGA clock period for an application including instruments that are all within the Keysight M3xxx family. For further explanations about the timing of HVI sequence execution please refer to the KS2201A PathWave Test Sync Executive User Manual available on www.keysight.com

FPGA Register Read

This corresponds to statements (c, h, k) in the HVI diagram. *InstructionFpgaRegisterRead* is an HVI core instruction that enables reading an HVI Register Bank placed into an FPGA sandbox design. The value read from the HVI Port Register will be written into a destination HVI register.

Python

```
# Access the local sequence from the Sync Multi-Sequence Block
leader_sequence = sync_block.sequences[config.leader_engine]
# Previously defined registers and FPGA resources
action4_cnt = sync_sequence.scopes[config.leader_engine].registers[register_names.action4_cnt]
fpga_reg_action4_cnt = leader_sequence.engine.fpga_sandboxes[hvi_res_names.M3xxx_sandbox].fpga_
registers[config.reg_action4_cnt]


# Read FPGA Register Register_Bank_HviAction4Cnt
readFpgaReg0 = leader_sequence.add_instruction('Read FPGA Register_Bank_HviAction4Cnt', 10,
leader_sequence.instruction_set.fpga_register_read.id)
readFpgaReg0.set_parameter(leader_sequence.instruction_set.fpga_register_read.destination.id,
action4_cnt)
readFpgaReg0.set_parameter(leader_sequence.instruction_set.fpga_register_read.fpga_register.id,
fpga_reg_action4_cnt)
```

FPGA Register Write

This corresponds to statement (d) in the HVI diagram. *InstructionFpgaRegisterWrite* is an HVI core instruction that enables writing an HVI Register Bank placed into an FPGA sandbox. The value to be written into the HVI Register Bank is taken from an HVI register or from a literal.

Python

```
# Access the local sequence from the Sync Multi-Sequence Block
leader_sequence = sync_block.sequences[config.leader_engine]
# Previously defined registers and FPGA resources
action4_cnt = sync_sequence.scopes[config.leader_engine].registers[register_names.action4_cnt]
fpga_reg_pxi_out = leader_sequence.engine.fpga_sandboxes[hvi_res_names.M3xxx_sandbox].fpga_
registers[config.reg_pxi_out]


# Write FPGA Register Register_Bank_HviPxiTrigOut
# Register_Bank_HviPxiTrigOut is connected to PXI lines Outputs.
# The value written to the FPGA register will be written to PXI lines
# NOTE: Please allow at least 60 ns between these instructions to ensure
# the HVI register action4_cnt is updated before writing its content to PXI lines
writeFpgaReg0 = leader_sequence.add_instruction('Write FPGA Register_Bank_HviPxiTrigOut', 60,
leader_sequence.instruction_set.fpga_register_write.id)
writeFpgaReg0.set_parameter(leader_sequence.instruction_set.fpga_register_write.fpga_
register.id, fpga_reg_pxi_out)
writeFpgaReg0.set_parameter(leader_sequence.instruction_set.fpga_register_write.value.id,
action4_cnt)
```

FPGA Memory Map Write

This corresponds to statement (e) in the HVI diagram. *InstructionFpgaArrayWrite* is an HVI core instruction that allows writing to an HVI Memory Map placed into an FPGA sandbox. The value to be written into the HVI Memory Map is taken from an HVI register or from a literal.

Python

```
# Access the local sequence from the Sync Multi-Sequence Block
leader_sequence = sync_block.sequences[config.leader_engine]
# Previously defined registers and FPGA resources
mem_map_counter = sync_sequence.scopes[config.leader_engine].registers[register_names.mem_map_
counter]
fpga_memory_map = leader_sequence.engine.fpga_sandboxes[hvi_res_names.M3xxx_sandbox].fpga_
memory_maps[config.memory_map]


# Write Memory Map
# At each iteration a different value is written to the memory map
writeMemoryMap = leader_sequence.add_instruction('Write FPGA Memory Map', 10, leader_
sequence.instruction_set.fpga_array_write.id)
writeMemoryMap.set_parameter(leader_sequence.instruction_set.fpga_array_write.fpga_memory_
map.id, fpga_memory_map)
writeMemoryMap.set_parameter(leader_sequence.instruction_set.fpga_array_write.value.id, mem_map_
counter)
writeMemoryMap.set_parameter(leader_sequence.instruction_set.fpga_array_write.fpga_memory_map_
offset.id, 0)
```

FPGA Memory Map Read

This corresponds to statement (f) in the HVI diagram. *InstructionFpgaArrayRead* is an HVI core instruction that enables reading an HVI Memory Map. The value read from the HVI Memory Map will be written into a destination HVI register.

Python

```
# Access the local sequence from the Sync Multi-Sequence Block
leader_sequence = sync_block.sequences[config.leader_engine]
# Previously defined registers and FPGA resources
mem_map = sync_sequence.scopes[config.leader_engine].registers[register_names.mem_map]
fpga_memory_map = leader_sequence.engine.fpga_sandboxes[hvi_res_names.M3xxx_sandbox].fpga_
memory_maps[config.memory_map]


# Read Memory Map
# Reads the value that was written to the block RAM connected to the memory map
# NOTE: Please allow at least 30 ns between these instructions to ensure data is written
# correctly through the memory map before you read it back
readMemoryMap = leader_sequence.add_instruction('Read FPGA Memory Map', 30, leader_
sequence.instruction_set.fpga_array_read.id)
readMemoryMap.set_parameter(leader_sequence.instruction_set.fpga_array_read.fpga_memory_map.id,
fpga_memory_map)
readMemoryMap.set_parameter(leader_sequence.instruction_set.fpga_array_read.destination.id, mem_
map)
readMemoryMap.set_parameter(leader_sequence.instruction_set.fpga_array_read.fpga_memory_map_
offset.id, 0)
```

Wait Statement

This corresponds to statement (i) in the HVI diagram. The wait statement is a local flow control statement that can be implemented using the API class *WaitStatement*. This sequence block sets an instrument to wait for a condition. The condition can be defined by a trigger, an event, or any combination of them through the usage of logical operators. In this programming example, the wait statement is used to set the leader engine to wait for an event generated by the FPGA sandbox, more specifically the event called 'HVI_UserEvent4'. The wait condition is defined by the wait mode and the sync mode. The wait mode *.WaitMode.TRANSITION* makes sure the wait condition is triggered precisely at the time instant when the event is activated. The sync mode .SyncMode.IMMEDIATE sets the wait event statement to let the execution continue immediately, that is, as soon as the event is received.

Python

```
# Wait for FPGA_User_Event4
# Define the condition for the wait statement
wait_condition = kthvi.Condition.event(hvi.engines[hvi_resources.leader_engine_name].events[hvi_
resources.hvi_user_event_4])
# Add wait statement
leader_sequence = sync_block.sequences[config.leader_engine]
waitEvent = leader_sequence.add_wait('Wait for FPGA_User_Event4', 10, wait_condition)
waitEvent.set_mode(kthvi.WaitMode.TRANSITION, kthvi.SyncMode.IMMEDIATE)
```

Action Execute

This corresponds to statement (j) in the HVI diagram. Actions to be used within an HVI sequence need to be added to the instrument HVI engine using the API 'add' method of the *ActionCollection* class. Once the wanted actions are added within the list of the instruments' HVI engine actions, an instruction to execute them can be added to the instrument's HVI sequence using the HVI API class *InstructionsActionExecute*. One or multiple actions can be executed at the same time within the same 'Action Execute' instruction.

Python

```
# AWG local sequences can be accessed from within the Sync Multi-Sequence Block
leader_sequence = sync_block.sequences[config.leader_engine]
# Action execute instruction: execute action 4
instAction4 = leader_sequence.add_instruction('Execute Action 4', 20, leader_
sequence.instruction_set.action_execute.id)
instAction4.set_parameter(leader_sequence.instruction_set.action_execute.action.id, leader_
sequence.engine.actions[hvi_res_names.hvi_user_action_4])
```

Register Increment

This corresponds to statements (m, n, o) in the HVI diagram. A register increment can be implemented within an HVI sequence using an instance of the API instruction class *InstructionsAdd*. The same instruction can be used to add registers and constant values (operands) and put the result in another register (result). The register to be incremented must have been previously added to the scope of the corresponding HVI engine.

Python

```
# AWG local sequences can be accessed from within the Sync Multi-Sequence Block
leader_sequence = sync_block.sequences[config.leader_engine]
#
# Increment counter register
instr = leader_sequence.add_instruction('Increment counter register', 10, leader_
sequence.instruction_set.add.id)
instr.set_parameter(leader_sequence.instruction_set.add.left_operand.id, counter_reg)
instr.set_parameter(leader_sequence.instruction_set.add.right_operand.id, 1)
instr.set_parameter(leader_sequence.instruction_set.add.destination.id, counter_reg)
```

Export the Programmed HVI Sequences to Text Format

KS2201A provides a feature to export the programmed HVI sequences to text format, which can be used both as a development and debug tool. The sequences can be exported using the to_string() method of the SyncSequence class, as illustrated in the code snippet below. Once exported to text format, the HVI sequences can be written to a text file or displayed on the console output. An example text file containing the HVI sequences exported from this programming example is provided together with this example's files.

```
# Generate HVI sequence description text
output = sequencer.sync_sequence.to_string(kthvi.OutputFormat.DEBUG)
print("Programmed HVI sequences exported to file")
```

Compile, Load, Execute the HVI Instance

Once the HVI sequences are programmed by defining all the necessary HVI statements, you can compile, load and execute the HVI. Compile, load and run functionalities can be accessed from the *Hvi* class.

Compile HVI

The compilation operation is performed by calling the compile() API method. This operation processes all the info related to the HVI application, including the necessary HVI resources and the

HVI statements included in the HVI sequences. The compilation generates a binary compiled output that can be loaded to the hardware instruments for their HVI engine to execute it. As an output, the compile() API method provides an object that can tell the user how many PXI sync resources are necessary to be reserved to execute the HVI application.

Python

```
# Compile HVI sequences
hvi = sequencer.compile()
print(hvi.compile_status.to_string())
print("HVI Compiled")
print("This HVI programming example needs to reserve {} PXI trigger resources to execute".format
(len(hvi.compile_status.sync_resources)))
```

Load HVI to Hardware

The API method load_to_hw() loads to each HVI engine the binary output obtained from the HVI compilation so that the HVI engine programmed into their digital HW (FPGA or ASIC) can execute it.

Python

```
# Load HVI to HW: load sequences, configure actions/triggers/events, lock resources, etc.
hvi.load_to_hw()
```

Execute HVI

HVI execution is controlled by the run() API method. HVI can be run in a blocking or non-blocking mode. In this programming example the non-blocking mode is used. By using this execution mode, SW execution can interact through registers read/write with the HVI sequence execution.

Python

```
# Execute HVI in non-blocking mode
# This mode allows SW execution to interact with HVI execution
hvi.run(hvi.no_wait)
print('HVI Running...')
```

Release Hardware

API method release_hw() shall be called once the HVI execution is finished to release all the HW resources that were reserved during the HVI execution, including the PXI trigger resources that had been locked by HVI for its execution.

Python

```
# Unlock and release HW resources
hvi.release_hw()
print("Releasing HW...")
```

Further HVI API Explanations

Detailed explanations of each class and functionality of the HVI API can be found in the PathWave Test Sync Executive User Manual or in the Python help file that is provided with the HVI installer, available at: C:\Program Files\Keysight\PathWave Test Sync Executive <year>\api\python\Help\index.html, where <year> shall be replaced with the year of the release you are using, for example <year> = 2023.

Conclusions

This programming example illustrated how to use Keysight PathWave Test Sync Executive together with Keysight PathWave FPGA. Custom FPGA blocks are designed using Keysight PathWave FPGA and loaded to the sandbox of two modular instruments. The two instruments execute HVI sequences that can communicate with the custom FPGA blocks programmed into the sandbox of the module FPGA. Using an HVI Memory Map or HVI Register Bank the HVI sequence can read/write values to any of such blocks inserted in the instrument sandbox. This programming example has also shown how HVI sequence and FPGA sandbox of an instrument can communicate by using actions and events. The exchanged information can also be written to PXI lines from the instrument sandbox. This way the information is shared among all the chassis instruments that have access to the same PXI lines. As an example, this feature was used in this programming example to share the register value connected to a counter of sandbox user actions.

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