Keysight D9030DDRC DDR3 Compliance Test Application

Methods of Implementation

KEYSIGHT TECHNOLOGIES

Notices

Software Version

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DDR3 Compliance Test Application — At A Glance

The Keysight D9030DDRC DDR3 Compliance Test is a DDR3 (Double Data Rate 3) test solution that covers electrical, clock, and timing parameters of the JEDEC (Joint Electronic Device Engineering Council) specifications. The software helps you in testing all the un-buffered DDR3 device under test (DUT) compliance, with the Keysight Infiniium oscilloscopes.

There are 2 main categories of test modes:

- Compliance Tests - These tests are based on the DDR3 JEDEC compliance specifications and are compared to corresponding compliance test limits.
- Custom Tests - These tests are not based on any compliance specification. The primary use of these tests is to perform signal debugging.

The DDR3 Compliance Test:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Allows you to determine the number of trials for each test, with the new multi trial run capability.
- Provides detailed information of each test that has been run. The result of maximum 64 worst trials can be displayed at any one time.
- Creates a printable HTML report of the tests that have been run.

The minimum number of probes required for the tests are:

- Clock tests - 1 probe
- Electrical tests - 3 probes
- Timing tests - 3 probes
- Custom tests - 3 probes

NOTE

The tests performed by the DDR3 Compliance Test are intended to provide a quick check of the physical layer performance of the DUT. These testing are not a replacement for an exhaustive test validation plan.

DDR3 SDRAM electrical, clock and timing test standards and specifications are described in the *JEDEC* document. For more information, please refer to the JEDEC web site at www.jedec.org.

Required Equipment and Software

In order to run the DDR3 automated tests, you need the following equipment and software:

- D9030DDRC DDR3 Test Application software
- Use one of the following Oscilloscope models:
  - Keysight DSO9000A-Series, DSO90000A-Series and DSOX90000A / Q / Z / V-Series Oscilloscopes with a minimum bandwidth of 8.0 GHz (recommended) for accurate measurements. For faster speed grade devices, a minimum bandwidth of 13.0 GHz bandwidth is recommended.
  - Keysight UXR Oscilloscope
  - Keysight MXR Oscilloscope
- The minimum version of Infiniium oscilloscope software (see the D9030DDRC test application release notes).
- D9030DDRC DDR3 Compliance Test Application software license
- RAM reliability test software.
- 1169A/B, 1168A/B, 1134A/B, 1132A/B or 1131A/B InfiniiMax probe amplifiers.
- N5381A/B or E2677A/B differential solder-in probe head, N5425A/B ZIF probe head or N5426A ZIF tips, E2678A/B differential socketed probe head.
- Any computer motherboard system that supports DDR3 memory.
- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Precision 3.5 mm BNC to SMA male adapter, Keysight p/n 54855-67604, qty = 2 (provided
- with the Keysight 54855A and 80000B series oscilloscopes)
- 50-ohm Coax Cable with SMA Male Connectors – 24-inch or less RG-316/U or similar, qty = 2, matched length
- Keysight also recommends using a second monitor to view the compliance test application.

NOTE **Keysight D9030DDRC DDR3 Compliance Test Application supports MXR oscilloscope.**

Below are the required licenses:

- D9030DDRC DDR3 Compliance Test Application license.
- E2688A Serial Data Analysis and Clock Recovery software license.

Following table displays the sampling rates for Keysight 90000 X-Series oscilloscope and UXR-Series oscilloscope:

Table 1 Sampling Rates for 90000X-Series Oscilloscope and UXR-Series Oscilloscope

Keysight 90000 X-Series Oscilloscope Sampling Rates	Keysight UXR -Series Oscilloscope Sampling Rates
MAX (Default)*	MAX (Default)*
	128 GSa/s
80 GSa/s	64 GSa/s
40 GSa/s	32 GSa/s
20 GSa/s	16 GSa/s
10 GSa/s	08 GSa/s

* The MAX sampling rate values are different for 90000X-Series and UXR-Series oscilloscope. For 90000X-Series, the MAX value is 80 GSa/s, and for UXR-Series, the MAX value is 128 GSa/s.

In This Book

This manual describes the tests that are performed by the DDR3 Compliance Test in more detail; it contains information from (and refers to) the *JEDEC specifications*, and it describes how the tests are performed.

- Chapter 1, “Installing the DDR3 Compliance Test Application" shows how to install and license the automated test application software (if it was purchased separately).
- Chapter 2, “Preparing to Take Measurements" shows how to start the DDR3 Compliance Test and gives a brief overview of how it is used.
- Chapter 3, “Clock Plus Tests Group" describes the V_{SEH} and V_{SEL} tests for Clock Plus signals and the AC overshoot and undershoot tests probing and method of implementation.
- Chapter 4, “Clock Minus Tests Group" describes the V_{SEH} and V_{SEL} tests for Clock Minus signals and the AC overshoot and undershoot tests probing and method of implementation.
- Chapter 5, “Clock Plus and Minus Cross Point Tests Group" describes the V_{IX} test for Clock Plus and Minus Point.
- Chapter 6, “Clock Differential Tests Group" shows how to run various Electrical Test, Timing Tests at AC Level, Timing Tests for Rising Edge Measurement and Timing Tests for Pulse Measurement.
- Chapter 7, “Strobe Plus Tests Group" describes the V_{SEH} and V_{SEL} tests for Strobe Plus signals and the AC overshoot and undershoot tests probing and method of implementation.
- Chapter 8, “Strobe Minus Tests Group" describes the V_{SEH} and V_{SEL} tests for Strobe Minus signals and the AC overshoot and undershoot tests probing and method of implementation.
- Chapter 9, “Strobe Plus and Minus Cross Point Tests Group" describes the V_{IX} test for strobe plus and minus point.
- Chapter 10, “Strobe Differential Tests Group" shows how to run various Electrical Test and Timing Tests.
- Chapter 11, “Data Tests Groups" shows how to run various Write Cycles and Read Cycles.
- Chapter 12, “Data Mask Tests Group" describes how to run the data mask timing tests.
- Chapter 13, “Command,Address Tests Group" describes the command and address timing tests which include the address and control input setup time as well as the address and control input hold time.
- Chapter 14, “Chip Select Tests Group" describes how to run the chip select tests.
- Chapter 15, “Clock Enable Tests Group" describes how to run the clock enable tests.

See Also

- The D9030DDRC DDR3 Compliance Test's Online help, which describes:
  - D9030DDRC DDR3 Automated Testing—At a Glance
  - Starting the D9030DDRC DDR3 Test Application
  - Creating or Opening a Test Project
  - Setting Up the Test Environment
  - Selecting Tests
  - Configuring Tests
  - Verifying Physical Connections
  - Running Tests
  - Configuring Automation in the Test Application
  - Viewing Results
  - Viewing HTML Test Report
  - Exiting the Test Application
  - Additional Settings in the Test App

Contents

1 Installing the DDR3 Compliance Test Application

If you have purchased the D9030DDRC DDR3 Compliance Test Application separately, you need to install the software and license key.

Installing the Software

1. Make sure you have the minimum version of Infiniium oscilloscope software (see the Keysight D9030DDRC DDR3 Compliance Test Application release notes) by choosing **Help > About Infiniium...** from the main menu.
2. To obtain the D9030DDRC, go to Keysight website: http://www.keysight.com/find/D9030DDRC.
3. The link for D9030DDRC will appear. Click on it and follow the instructions to download and install the application software.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

1 Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.

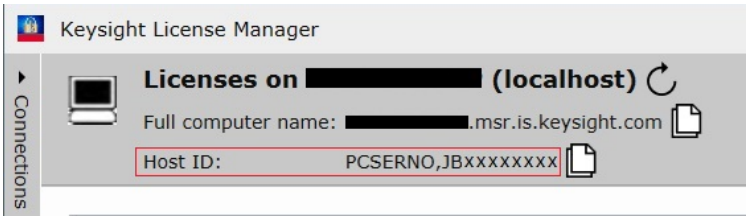


Figure 1 Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager.

3 From the configuration menu, use one of the options to install each license file.

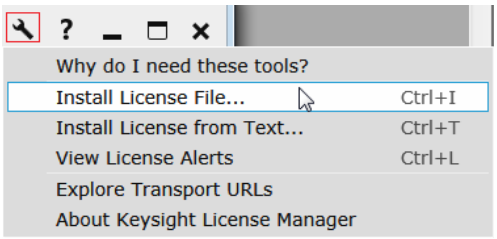


Figure 2 Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

1. Launch Keysight License Manager 6 on your machine, where you wish to run the Test Application and its features.
2. Copy the Host ID, which is the first set of alphanumeric value (as highlighted in Figure 3) that appears in the Environment tab of the application. Note that x indicates numeric values.

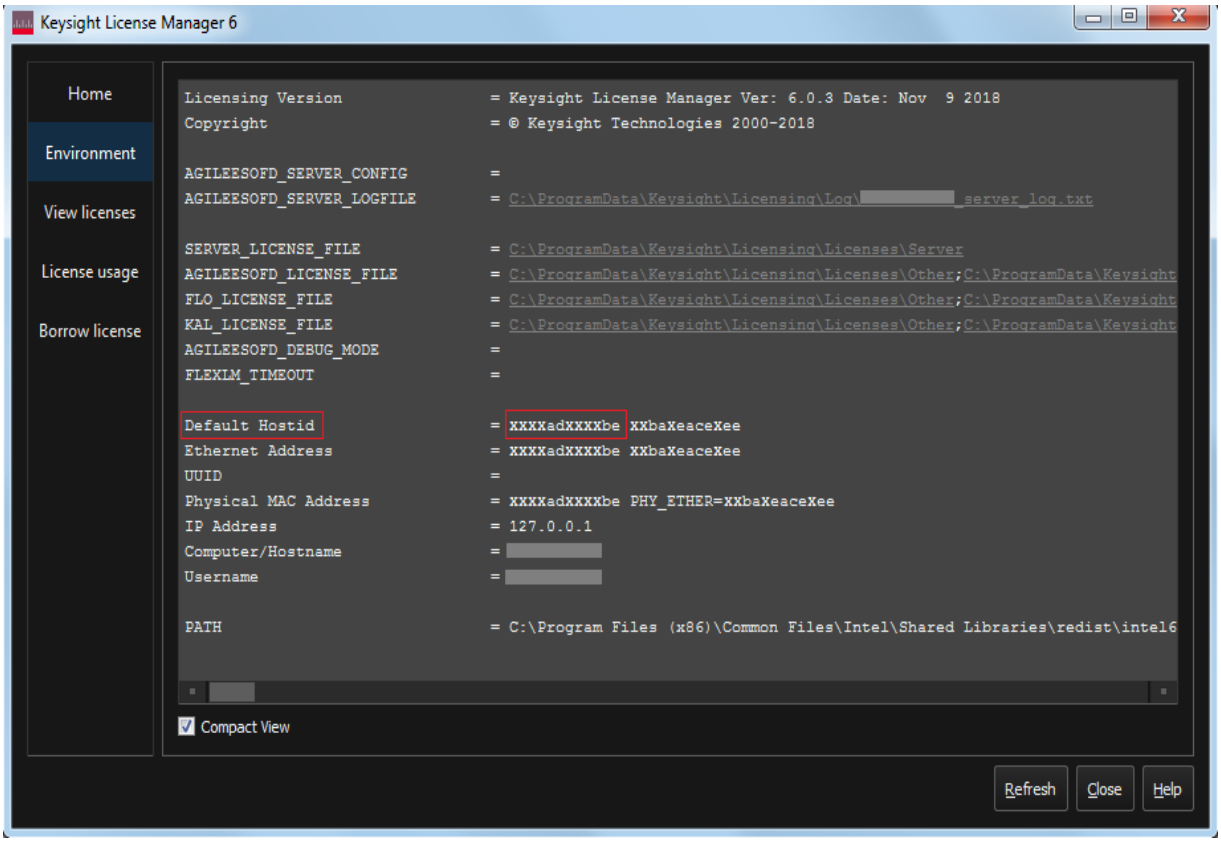


Figure 3 Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.
2 Launch Keysight License Manager 6.
3 From the Home tab, use one of the options to install each license file.

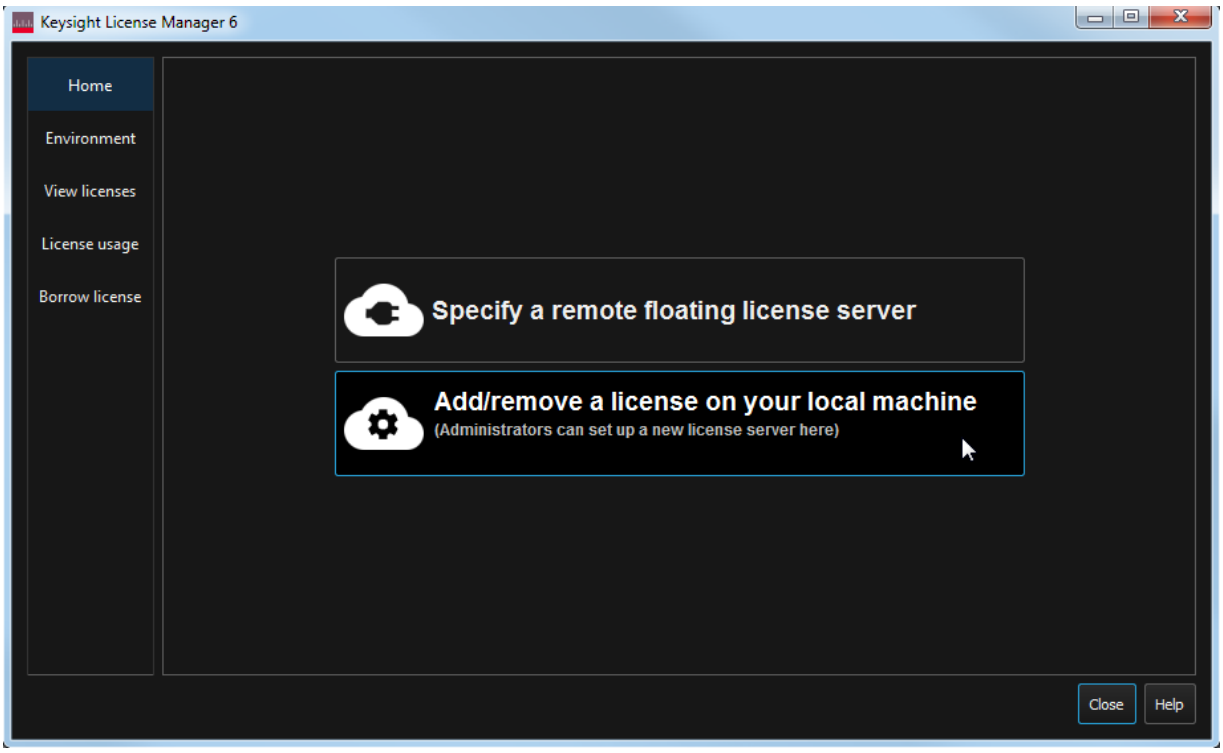


Figure 4 Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

2 Preparing to Take Measurements

Before running the DDR3 automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this DDR3 application. After the oscilloscope and probe have been calibrated, you are ready to start the Keysight D9030DDRC DDR3 Compliance Test Application and perform the measurements.

Calibrating the Oscilloscope

If you haven't already calibrated the Oscilloscope, refer to the documentation provided with the Oscilloscope model being used to perform tests.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities** > **Calibration** menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the DDR3 Compliance Test Application

1 Ensure that the RAM reliability test software is running in the computer system where the Device Under Test (DUT) is attached. This software performs tests to all unused RAM in the system by producing a repetitive burst of read-write data signals to the DDR3 memory.

2 To start the Keysight D9030DDRC DDR3 Compliance Test Application: From the Infiniium oscilloscope's main menu, choose **Analyze** > **Automated Test Apps** > **D9030DDRC DDR3 Test App**.

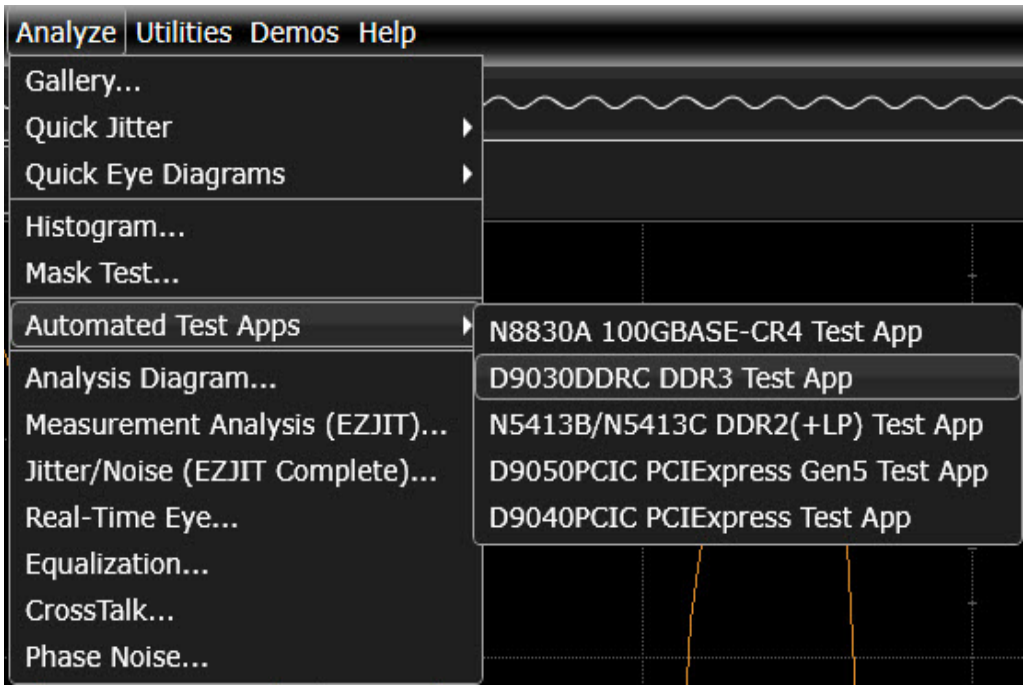


Figure 5 Infiniium oscilloscope's main menu

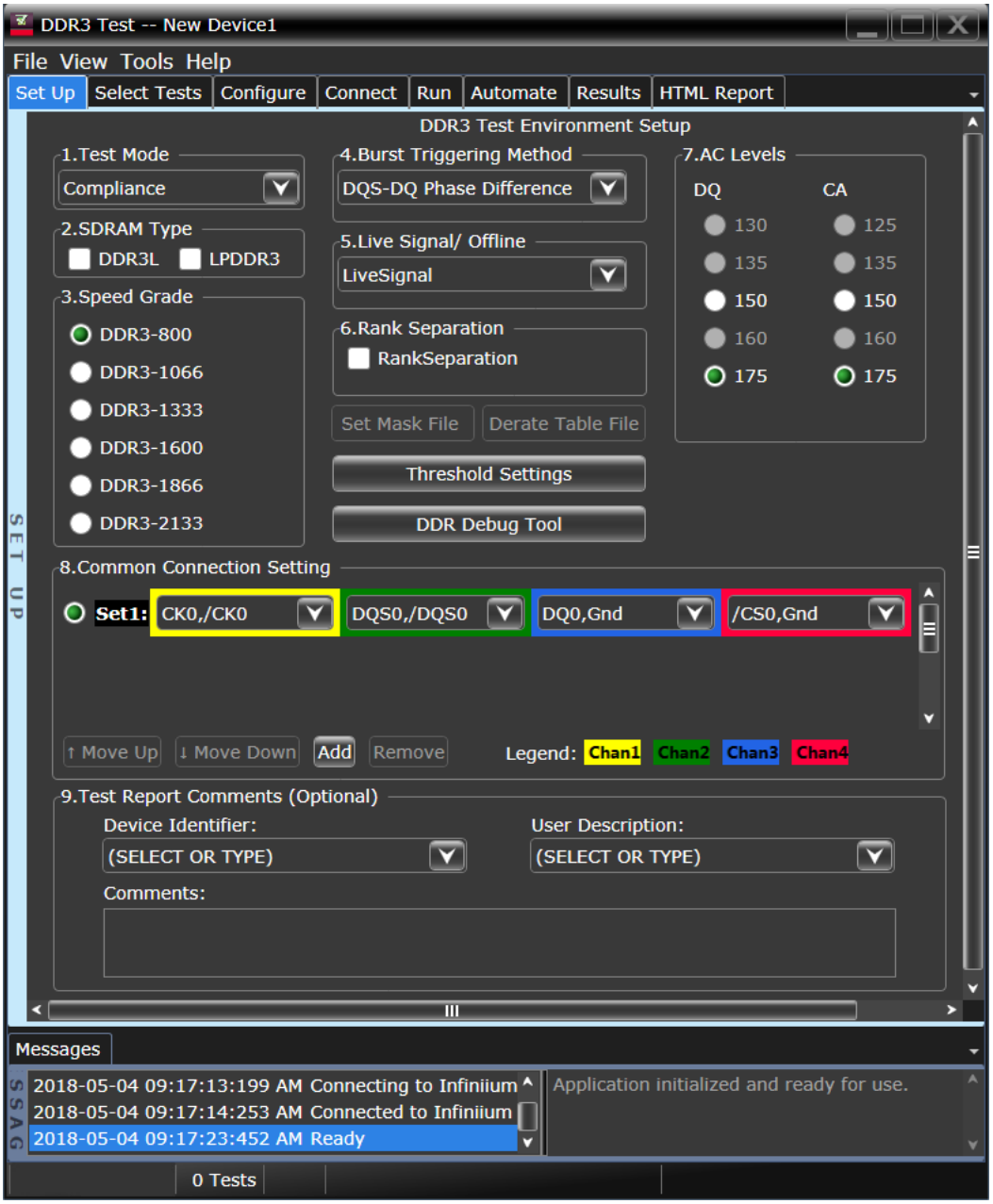


Figure 6 Default view of the DDR3 Compliance Test Application

NOTE If the Keysight D9030DDRC DDR3Test App does not appear in the Automated Test Apps menu, then it has not been installed (see Chapter 1, “Installing the DDR3 Compliance Test Application”)

Figure 5 and Figure 6 show the DDR3 Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Tab	Description
Set Up	Lets you identify and set up the test environment, including information about the device under test.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters. The information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automation	Lets you construct scripts of commands that drive execution of the application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE When you close the DDR3 application, each channel's probe is configured as single-ended or differential depending on the last DDR3 test that was run.

Correlation between Signal Group and PUT

Among the various options available under the **Set Up** tab of the Keysight D9030DDRC DDR3 Compliance Test Application, which filter the list of tests in the **Select Tests** tab; one of the features is the **Common Connection Setting**. Using this feature, when you select the Pin Under Test (PUT) that is connected to each Oscilloscope Channel, the Test Application displays one or more tests/test categories either as available or unavailable. Table 2 and Table 3 list the signal group for the corresponding PIN that you select using the **Common Connection Setting** feature.

The signal groups that are required to run various DDR3/DDR3L/LPDDR3 tests are:

- Clock Differential
- Clock Plus
- Clock Minus
- Strobe Differential
- Strobe Plus
- Strobe Minus
- Data
- Data Mask
- DDR3_CommandAddress
- DDR3_CommandAddress_ChipSelect
- LPDDR3_CommandAddress
- LPDDR3_ChipSelect
- LPDDR3_ClockEnable
- Not in Use (if a Channel does not have any test signal)

NOTE

The signal group “DDR3_CommandAddress_ChipSelect” is a subset of “DDR3_Command_Address”.

To make all such tests available, which require the signal group “DDR3_CommandAddress”, you may select either “DDR3_CommandAddress” or “DDR3_CommandAddress_ChipSelect”.

To make all such tests available, which require the signal group “DDR3_Command_Address_ChipSelect” only, you must select only “DDR3_CommandAddress_ChipSelect”. Selecting any other signal group will show such tests as unavailable.

Table 2 Correlation between Signal Group and selected PUT for DDR3/DDR3L tests

Common Connection Setting PUT	Signal Type	Signal Group
Not_In_Use	NA	NotInUse
CK0,/CK0 to **CK2,/CK2**	Clock_DCK0 to Clock_DCK2	Clock Differential
CK0,Gnd to **CK2,Gnd**	Clock_SCK0 to Clock_SCK2	Clock Plus
/CK0,Gnd to **/CK2,Gnd**	Clock_NCK0 to Clock_NCK2	Clock Minus
DQS0,/DQS0 to **DQS8,/DQS8**	Strobe_DDQS0 to Strobe_DDQS8	Strobe Differential
DQS0,Gnd to **DQS8,Gnd**	Strobe_SDQS0 to Strobe_SDQS8	Strobe Plus
/DQS0,Gnd to **/DQS8,Gnd**	Strobe_NDQS0 to Strobe_NDQS8	Strobe Minus
DQ0,Gnd to **DQ71,Gnd**	Data_DQ0 to Data_DQ71	Data
DM0,Gnd to **DM7,Gnd**	DM_DM0 to DM_DM7	Data Mask
/CS0,Gnd & **/CS1,Gnd**	Control_NCS0 & Control_NCS1	DDR3_CommandAddress_ChipSelect
BA0,Gnd to **BA2,Gnd**	Control_BA0 & Control_BA2	DDR3_CommandAddress
/RAS,Gnd	Control_NRAS	
/WE,Gnd	Control_NWE	
/CAS,Gnd	Control_NCAS	
CKE0,Gnd & **CKE1,Gnd**	Control_CKE0 & Control_CKE1	
ODT0,Gnd & **ODT1,Gnd**	Control_ODT0 & Control_ODT1	
A0,Gnd to **A15,Gnd**	Address_A0 to Address_A15	

Table 3 Correlation between Signal Group and selected PUT for LPDDR3 tests

Common Connection Setting PUT	Signal Type	Signal Group
Not_In_Use	LP_NA_	NotInUse
CK_t,CK_c	LP_Clock_DCK	Clock Differential
CK_t,GND	LP_Clock_SCK	Clock Plus
CK_c,GND	LP_Clock_NCK	Clock Minus
DQS0_t,DQS0_C to **DQS3_t,DQS3_c**	LP_Strobe_DDQS0 to LP_Strobe_DDQS3	Strobe Differential
DQS0_t,GND to **DQS3_t,GND**	LP_Strobe_SDQS0 to LP_Strobe_SDQS3	Strobe Plus
DQS0_c,GND to **DQS3_c,GND**	LP_Strobe_NDQS0 to LP_Strobe_NDQS3	Strobe Minus
DQ0,GND to **DQ31,GND**	LP_Data_DQ0 to LP_Data_DQ31	Data
DM0,GND to **DM3,GND**	LP_DM_DM0 to LP_DM_DM3	Data Mask
CS_n,GND	LP_Control_NCS	LPDDR3_ChipSelect
CKE,GND	LP_Control_CKE	LPDDR3_ClockEnable
CA0,GND to **CA9,GND**	LP_CommandAddress_CA0 to LP_CommandAddress_CA9	LPDDR3_CommandAddress

Signal requirements for test availability

Table 4 displays a comprehensive list of the tests that are made available for one or more signals that you can select in the Compliance Test Application, using the **Common Connection Setting** feature.

Table 4 Availability of tests based on required signals for SDRAM Types DDR3 & DDR3L

Test Group Name	Test Group Category	Available tests	Required signals
Clock Plus	Electrical Tests	VSEH(Clock Plus)	▪ Clock Plus
		VSEL(Clock Plus)	▪ Clock Plus
		Overshoot Amplitude / Area for Clock Plus Tests	▪ Clock Plus
		Undershoot Amplitude / Area for Clock Plus Tests	▪ Clock Plus
		SlewR on Setup Region	▪ Clock Plus
		SlewF on Setup Region	▪ Clock Plus
		SlewR on Hold Region	▪ Clock Plus
		SlewF on Hold Region	▪ Clock Plus
Clock Minus	Electrical Tests	VSEH(Clock Minus)	▪ Clock Minus
		VSEL(Clock Minus)	▪ Clock Minus
		Overshoot Amplitude / Area (Clock Minus)	▪ Clock Minus
		Undershoot Amplitude / Area (Clock Minus)	▪ Clock Minus
		SlewR on Setup Region	▪ Clock Minus
		SlewF on Setup Region	▪ Clock Minus
		SlewR on Hold Region	▪ Clock Minus
		SlewF on Hold Region	▪ Clock Minus
Clock Plus and Minus Cross Point		VIX for Clock	▪ Clock Plus ▪ Clock Minus
Clock Differential	Electrical Test	VIHdiff.CK(AC)	▪ Clock Differential
		VILdiff.CK(AC)	▪ Clock Differential
		VIHdiff.CK	▪ Clock Differential
		VILdiff.CK	▪ Clock Differential
	Timing Tests at AC level	tDVAC(Clock)	▪ Clock Differential

Test Group Name	Test Group Category	Available tests	Required signals
Clock Differential	Timing Tests for Rising Edge Measurements	tjit(CC) Rising Edge Measurement	▪ Clock Differential
		tCK(avg) Rising Edge Measurement	▪ Clock Differential
		tjit(per) Rising Edge Measurement	▪ Clock Differential
		tERR(nper) Rising Edge Measurement	▪ Clock Differential
	Timing Tests for Pulse Measurements	tCH(avg) Average High Measurement	▪ Clock Differential
		tCL(avg) Average Low Measurement	▪ Clock Differential
		tJIT(duty-high/low) Jitter Average High/Low Measurements	▪ Clock Differential
		tCH(abs) Absolute clock HIGH pulse width	▪ Clock Differential
		tCL(abs) Absolute clock LOW pulse width	▪ Clock Differential
Strobe Plus	Electrical Tests	VSEH(Strobes Plus)	▪ Strobe Plus ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		VSEL(Strobes Plus)	▪ Strobe Plus ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		Overshoot Amplitude / Area (Strobes Plus)	▪ Strobe Plus
		Undershoot Amplitude / Area (Strobes Plus)	▪ Strobe Plus
		SlewR on Setup Region	▪ Strobe Plus ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SlewF on Setup Region	▪ Strobe Plus ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SlewR on Hold Region	▪ Strobe Plus ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SlewF on Hold Region	▪ Strobe Plus ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)

Test Group Name	Test Group Category	Available tests	Required signals
Strobe Minus	Electrical Tests	VSEH(Strobes Minus)	▪ Strobe Minus ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		VSEL(Strobes Minus)	▪ Strobe Minus ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		Overshoot Amplitude/Area (Strobes Minus)	▪ Strobe Minus
		Undershoot Amplitude/Area (Strobes Minus)	▪ Strobe Minus
		SlewR on Setup Region	▪ Strobe Minus ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SlewF on Setup Region	▪ Strobe Minus ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SlewR on Hold Region	▪ Strobe Minus ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SlewF on Hold Region	▪ Strobe Minus ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
Strobe Plus and Minus Cross Point		VIX for Strobe	▪ Strobe Plus ▪ Strobe Minus ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
Strobe Differential (Write Cycle)	Electrical Tests	VIHdiff.DQS(AC)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		VILdiff.DQS(AC)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		VIHdiff.DQS	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		VILdiff.DQS	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)

Test Group Name	Test Group Category	Available tests	Required signals
Strobe Differential (Write Cycle)	Timing Tests	tDQSS	▪ Clock Differential ▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tDQSH	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tDQSL	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tDSS	▪ Clock Differential ▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tDSH	▪ Clock Differential ▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tWPRE	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tWPST	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tDVAC(Strobe)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)

Test Group Name	Test Group Category	Available tests	Required signals
Strobe Differential (Read Cycle)	Electrical Tests	VOHdiff(AC)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		VOLdiff(AC)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SRQdiffR	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SRQdiffF	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
	Timing Tests	tLZ(DQS) / tLZ(DQS) for Low Power / tHZ(DQS) / tHZ (DQS) for Low Power	▪ Clock Differential ▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tRPRE	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tRPST	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tQSH	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tQSL	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tDQSCK	▪ Clock Differential ▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)

Test Group Name	Test Group Category	Available tests	Required signals
Data (Write Cycle)	Electrical Tests	VIH.DQ(AC)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		VIH.DQ(DC)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		VIL.DQ(AC)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		VIL.DQ(DC)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SlewR on Setup Region	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SlewF on Setup Region	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SlewR on Hold Region	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SlewF on Hold Region	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)

Test Group Name	Test Group Category	Available tests	Required signals
Data (Write Cycle)	Timing Tests	tDS(base)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tDH(base)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tDS-Diff(derate)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tDH-Diff(derate)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tDIPW	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tVAC(Data)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
Data (Read Cycle)	Electrical Tests	VOH(AC)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		VOH(DC)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		VOL(AC)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		VOL(DC)	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SRQseR	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SRQseF	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)

Test Group Name	Test Group Category	Available tests	Required signals
Data (Read Cycle)	Timing Tests	tHZ(DQ)	▪ Clock Differential ▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tLZ(DQ)	▪ Clock Differential ▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tDQSQ	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		tQH	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
Data (Electrical Overshoot/Undershoot Tests)		Overshoot Amplitude/Area (Data)	▪ Data
		Undershoot Amplitude/Area (Data)	▪ Data
Data (Read/Write Eye-Diagram Tests)		User Defined Real-Time Eye Diagram Test For Read Cycle	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		User Defined Real-Time Eye Diagram Test For Write Cycle	▪ Strobe Differential ▪ Data ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)

Test Group Name	Test Group Category	Available tests	Required signals
Data Mask (Write Cycle)	Electrical Tests	VIH.DQ(AC)	▪ Strobe Differential ▪ Data Mask ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		VIH.DQ(DC)	▪ Strobe Differential ▪ Data Mask ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		VIL.DQ(AC)	▪ Strobe Differential ▪ Data Mask ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		VIL.DQ(DC)	▪ Strobe Differential ▪ Data Mask ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SlewR on Setup Region	▪ Strobe Differential ▪ Data Mask ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SlewF on Setup Region	▪ Strobe Differential ▪ Data Mask ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SlewR on Hold Region	▪ Strobe Differential ▪ Data Mask ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
		SlewF on Hold Region	▪ Strobe Differential ▪ Data Mask ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
	Timing Tests	tDIPW	▪ Strobe Differential ▪ Data Mask ▪ DDR3_CommandAddress_ChipSelect (If Rank Separation is enabled)
Data Mask (Electrical Tests)	Overshoot/Undershoot	Overshoot Amplitude/Area (Data Mask)	▪ Data Mask
		Undershoot Amplitude/Area (Data Mask)	▪ Data Mask

Test Group Name	Test Group Category	Available tests	Required signals
Command,Address	Electrical Tests	VIH.CA(AC)	▪ DDR3_CommandAddress, or DDR3_CommandAddress_ChipSelect
		VIH.CA(DC)	▪ DDR3_CommandAddress, or DDR3_CommandAddress_ChipSelect
		VIL.CA(AC)	▪ DDR3_CommandAddress, or DDR3_CommandAddress_ChipSelect
		VIL.CA(DC)	▪ DDR3_CommandAddress, or DDR3_CommandAddress_ChipSelect
		SlewR on Setup Region	▪ DDR3_CommandAddress, or DDR3_CommandAddress_ChipSelect
		SlewF on Setup Region	▪ DDR3_CommandAddress, or DDR3_CommandAddress_ChipSelect
		SlewR on Hold Region	▪ DDR3_CommandAddress, or DDR3_CommandAddress_ChipSelect
		SlewF on Hold Region	▪ DDR3_CommandAddress, or DDR3_CommandAddress_ChipSelect
		Overshoot Amplitude/Area (Command, Address)	▪ DDR3_CommandAddress, or DDR3_CommandAddress_ChipSelect
		Undershoot Amplitude/Area (Command, Address)	▪ DDR3_CommandAddress, or DDR3_CommandAddress_ChipSelect
	Timing Tests	tIS(base)	▪ Clock Differential ▪ DDR3_CommandAddress, or DDR3_CommandAddress_ChipSelect
		tIH(base)	▪ Clock Differential ▪ DDR3_CommandAddress, or DDR3_CommandAddress_ChipSelect
		tIS(derate)	▪ Clock Differential ▪ DDR3_CommandAddress, or DDR3_CommandAddress_ChipSelect
		tIH(derate)	▪ Clock Differential ▪ DDR3_CommandAddress, or DDR3_CommandAddress_ChipSelect
		tIPW	▪ DDR3_CommandAddress, or DDR3_CommandAddress_ChipSelect
		tVAC(CA)	▪ DDR3_CommandAddress, or DDR3_CommandAddress_ChipSelect
	Eye-Diagram Tests	User Defined Real-Time Eye Diagram Test For Command Address	▪ Clock Differential ▪ DDR3_CommandAddress, or DDR3_CommandAddress_ChipSelect

Table 5 Availability of tests based on required signals for SDRAM Type LPDDR3

Test Group Name	Test Group Category	Available tests	Required signals
Clock Plus	Electrical Tests	VSEH(Clock Plus)	▪ Clock Plus
		VSEL(Clock Plus)	▪ Clock Plus
		Overshoot Amplitude / Area for Clock Plus Tests	▪ Clock Plus
		Undershoot Amplitude / Area for Clock Plus Tests	▪ Clock Plus
Clock Minus	Electrical Tests	VSEH(Clock Minus)	▪ Clock Minus
		VSEL(Clock Minus)	▪ Clock Minus
		Overshoot Amplitude / Area (Clock Minus)	▪ Clock Minus
		Undershoot Amplitude / Area (Clock Minus)	▪ Clock Minus
Clock Plus and Minus Cross Point		VIXCA for Clock	▪ Clock Plus ▪ Clock Minus
Clock Differential	Electrical Test	VIHdiff.CK(AC)	▪ Clock Differential
		VILdiff.CK(AC)	▪ Clock Differential
		VIHdiff.CK(DC)	▪ Clock Differential
		VILdiff.CK(DC)	▪ Clock Differential
	Timing Tests at AC level	tDVAC(Clock)	▪ Clock Differential
	Timing Tests for Rising Edge Measurements	tCK(abs) Rising Edge Measurement	▪ Clock Differential
		tjit(CC) Rising Edge Measurement	▪ Clock Differential
		tCK(avg) Rising Edge Measurement	▪ Clock Differential
		tjit(per) Rising Edge Measurement	▪ Clock Differential
		tERR(nper) Rising Edge Measurement	▪ Clock Differential
	Timing Tests for Pulse Measurements	tCH(avg) Average High Measurement	▪ Clock Differential
		tCL(avg) Average Low Measurement	▪ Clock Differential
		tJIT(duty-high/low) Jitter Average High/Low Measurements	▪ Clock Differential
		tCH(abs) Absolute clock HIGH pulse width	▪ Clock Differential
		tCL(abs) Absolute clock LOW pulse width	▪ Clock Differential
Strobe Plus	Electrical Tests	VSEH(Strobes Plus)	▪ Strobe Plus ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		VSEL(Strobes Plus)	▪ Strobe Plus ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		Overshoot Amplitude / Area (Strobes Plus)	▪ Strobe Plus
		Undershoot Amplitude / Area (Strobes Plus)	▪ Strobe Plus

Test Group Name	Test Group Category	Available tests	Required signals
Strobe Minus	Electrical Tests	VSEH(Strobes Minus)	▪ Strobe Minus ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		VSEL(Strobes Minus)	▪ Strobe Minus ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		Overshoot Amplitude/Area (Strobes Minus)	▪ Strobe Minus
		Undershoot Amplitude/Area (Strobes Minus)	▪ Strobe Minus
Strobe Plus and Minus Cross Point		VIXDQ - Strobe Cross Point Voltage Test	▪ Strobe Plus ▪ Strobe Minus ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
Strobe Differential (Write Cycle)	Electrical Tests	VIHdiff.DQS(AC)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		VILdiff.DQS(AC)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		VIHdiff.DQS (DC)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		VILdiff.DQS (DC)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)

Test Group Name	Test Group Category	Available tests	Required signals
Strobe Differential (Write Cycle)	Timing Tests	tDQSS	▪ Clock Differential ▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tDQSH	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tDQSL	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tDSS	▪ Clock Differential ▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tDSH	▪ Clock Differential ▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tWPRE	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tWPST	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tDVAC(Strobe)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)

Test Group Name	Test Group Category	Available tests	Required signals
Strobe Differential (Read Cycle)	Electrical Tests	VOHdiff(AC)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		VOLdiff(AC)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		SRQdiffR	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		SRQdiffF	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
	Timing Tests	tLZ(DQS) for Low Power	▪ Clock Differential ▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tHZ(DQS)	▪ Clock Differential ▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tRPRE	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tRPST	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tQSH	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tQSL	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tDQSCK	▪ Clock Differential ▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)

Test Group Name	Test Group Category	Available tests	Required signals
Data (Write Cycle)	Electrical Tests	VIH.DQ(AC)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		VIH.DQ(DC)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		VIL.DQ(AC)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		VIL.DQ(DC)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
	Timing Tests	tDS(base)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tDH(base)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tDS-Diff(derate)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tDH-Diff(derate)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tDIPW	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tVAC(Data)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)

Test Group Name	Test Group Category	Available tests	Required signals
Data (Read Cycle)	Electrical Tests	VOH(AC)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		VOH(DC)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		VOL(AC)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		VOL(DC)	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		SRQseR	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		SRQseF	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
	Timing Tests	tHZ(DQ) for Low Power	▪ Clock Differential ▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tLZ(DQ) for Low Power	▪ Clock Differential ▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tDQSQ	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tQH	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
Data (Electrical Overshoot/Undershoot Tests)		Overshoot Amplitude/Area (Data)	▪ Data
		Undershoot Amplitude/Area (Data)	▪ Data
Data (Read/Write Eye-Diagram Tests)		User Defined Real-Time Eye Diagram Test For Read Cycle	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		User Defined Real-Time Eye Diagram Test For Write Cycle	▪ Strobe Differential ▪ Data ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)

Test Group Name	Test Group Category	Available tests	Required signals
Data Mask (Write Cycle)	Electrical Tests	VIH.DQ(AC)	▪ Strobe Differential ▪ Data Mask ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		VIH.DQ(DC)	▪ Strobe Differential ▪ Data Mask ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		VIL.DQ(AC)	▪ Strobe Differential ▪ Data Mask ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		VIL.DQ(DC)	▪ Strobe Differential ▪ Data Mask ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
	Timing Tests	tDS(base)	▪ Strobe Differential ▪ Data Mask ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tDH(base)	▪ Strobe Differential ▪ Data Mask ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tDS-Diff(derate)	▪ Strobe Differential ▪ Data Mask ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tDH-Diff(derate)	▪ Strobe Differential ▪ Data Mask ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tDIPW	▪ Strobe Differential ▪ Data Mask ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
		tVAC(Data Mask)	▪ Strobe Differential ▪ Data Mask ▪ LPDDR3_ChipSelect (If Rank Separation is enabled)
Data Mask (Electrical Overshoot/Undershoot Tests)		Overshoot Amplitude/Area (Data Mask)	▪ Data Mask
		Undershoot Amplitude/Area (Data Mask)	▪ Data Mask

Test Group Name	Test Group Category	Available tests	Required signals
Command,Address	Electrical Tests	VIH.CA(AC)	▪ LPDDR3_CommandAddress
		VIH.CA(DC)	▪ LPDDR3_CommandAddress
		VIL.CA(AC)	▪ LPDDR3_CommandAddress
		VIL.CA(DC)	▪ LPDDR3_CommandAddress
		Overshoot Amplitude/Area (Command, Address)	▪ LPDDR3_CommandAddress
		Undershoot Amplitude/Area (Command, Address)	▪ LPDDR3_CommandAddress
	Timing Tests	tISCA(base)	▪ Clock Differential ▪ LPDDR3_CommandAddress
		tIHCA(base)	▪ Clock Differential ▪ LPDDR3_CommandAddress
		tISCA(derate)	▪ Clock Differential ▪ LPDDR3_CommandAddress
		tIHCA(derate)	▪ Clock Differential ▪ LPDDR3_CommandAddress
		tIPWCA	▪ LPDDR3_CommandAddress
		tVAC(CA)	▪ LPDDR3_CommandAddress
	Eye-Diagram Tests	User Defined Real-Time Eye Diagram Test For Command Address	▪ Clock Differential ▪ LPDDR3_CommandAddress
Chip Select	Electrical Tests	Overshoot Amplitude/Area (Chip Select Tests)	▪ LPDDR3_ChipSelect
		Undershoot Amplitude/Area Chip Select Tests	▪ LPDDR3_ChipSelect
	Timing Tests	tISCS(base)	▪ Clock Differential ▪ LPDDR3_ChipSelect
		tIHCS(base)	▪ Clock Differential ▪ LPDDR3_ChipSelect
		tISCS(derate)	▪ Clock Differential ▪ LPDDR3_ChipSelect
		tIHCS(derate)	▪ Clock Differential ▪ LPDDR3_ChipSelect
		tIPWCS	▪ LPDDR3_ChipSelect
Clock Enable	Electrical Tests	Overshoot Amplitude / Area) (Clock Enable)	▪ LPDDR3_ClockEnable
		Undershoot Amplitude / Area (Clock Enable)	▪ LPDDR3_ClockEnable
	Timing Tests	tCKE	▪ Clock Differential ▪ LPDDR3_ClockEnable
		tISCKE	▪ Clock Differential ▪ LPDDR3_ClockEnable
		tIHCKE	▪ Clock Differential ▪ LPDDR3_ClockEnable

3 Clock Plus Tests Group

This section provides the Methods of Implementation (MOIs) for Clocks Plus Tests using a Keysight Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

NOTE **Both XYZ# and $\overline{XYZ}$ refer to complement. Thus, CK# is the same as $\overline{CK}$.**

Probing for Clock Plus Tests

When performing the Clock Plus tests for Clocks, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Clock Plus tests for Clocks may look similar to the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance application for the exact number of probe connections.

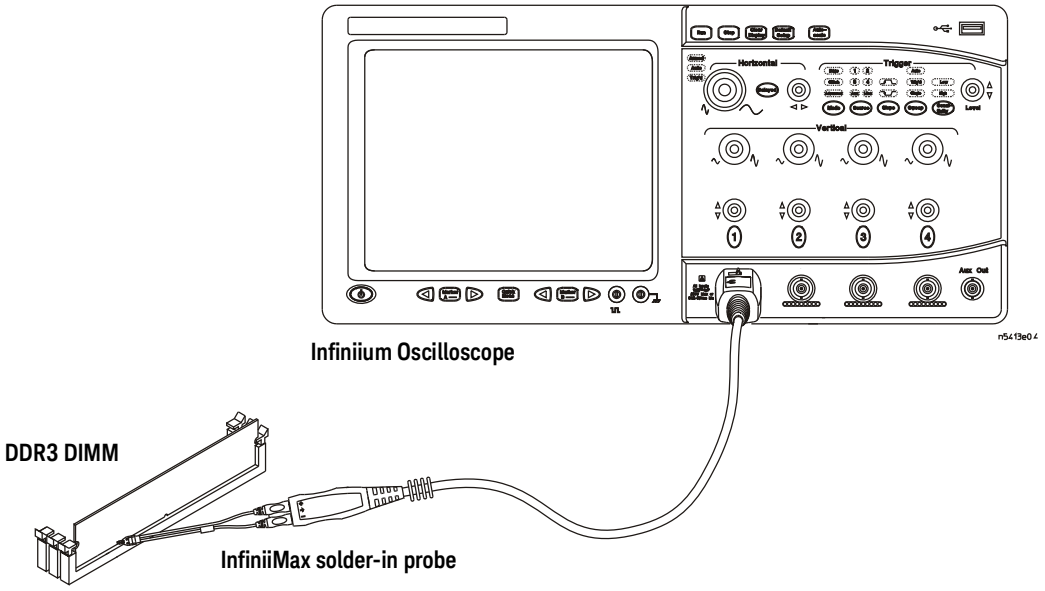


Figure 7 Probing for Clock Plus Tests

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 7 are just examples).

For more information on the probe amplifiers and differential probe heads, refer to the respective user guide for Probes.

Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the **Set Up** tab.

6 Select the **Test Mode**, **SDRAM Type, Speed Grade**, and **AC Levels** options.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

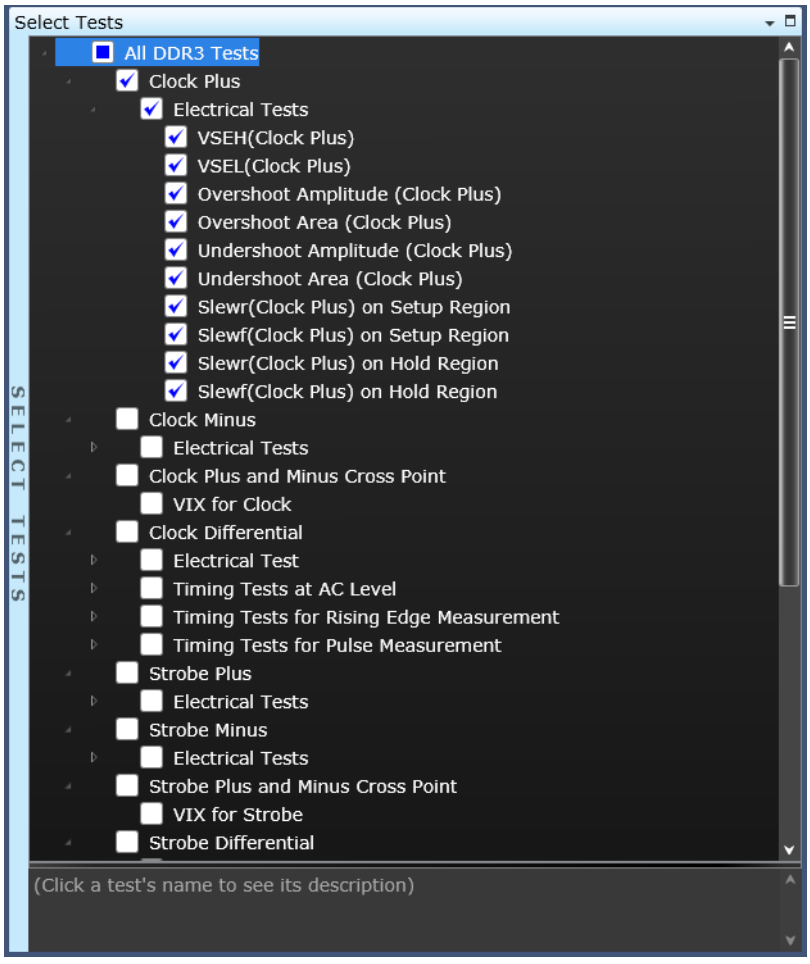


Figure 8 Selecting Clock Plus Tests

Electrical Tests

VSEH(Clock Plus)

Test Overview

The purpose of this test is to verify that the maximum voltage of the high pulse must be within the conformance limit of the V_{SEH} value as specified in the JEDEC specification.

The value of V_{DD} (which directly affects the conformance limit) is set to 1.5V for DDR3 and 1.2V for LPDDR3. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DD}.

Modes Supported

- DDR3, DDR3L, and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Plus Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 6 Single-ended Levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL# or DQSU#

Symbol	Parameter	DDR3-800/1066/1333/1600		Units
		Min	Max	
V_{SEH}	Single-ended high level for clocks	$(V_{DD}/2) + 0.175$	Note 3[a]	V

a: Refers to Note 3 in Table 27 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Table 7 Single-ended Levels for CK_t, DQS_t, CK_c, and DQS_c

Symbol	Parameter	Value		Units	Notes
		Min	Max		
$V_{SEH(AC)}$	Single-ended high level for CK_t, CK_c	$(V_{DDCA}/2) + 0.220$	Note 3[c]	V	1[a], 2[b]

a: Refers to Note 1 in Table 39 of the *JEDEC Standard JESD209-3*. For CK_t, CK_c, use $V_{SEH}/V_{SEL(ac)}$ of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use $V_{IH}/V_{IL(ac)}$ of DQs.

b: Refers to Note 2 in Table 39 of the *JEDEC Standard JESD209-3*. $V_{IH(ac)}/V_{IL(ac)}$ for DQs is based on V_{REFDQ}; $V_{SEH(ac)}/V_{SEL(ac)}$ for CA is based on V_{REFCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

c: Refers to Note 3 in Table 39 of the *JEDEC Standard JESD209-3*. These values are not defined, however.the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.5 “Overshoot and Undershoot Specifications” on page 92 of the specification document.

Test References

- *See Table 27 in Section 8.3 of the DDR3 SDRAM Specification, JEDEC Standard JESD79-3E, July 2010* and
- *See Figure 124 and Table 40 in Section 7 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Precondition the oscilloscope.
2 Trigger on a rising edge of the clock signal under test.
3 Find all valid Clock positive pulses in the entire waveform. A valid Clock positive pulse starts at the V_{REF} crossing on a valid Clock rising edge and ends at the V_{REF} crossing on the following valid Clock falling edge.
4 For the first valid Clock positive pulse, zoom in on the pulse so that it appears on the oscilloscope’s display and measure T_{MAX}.
5 Measure V_{TIME} at the found T_{MAX} to obtain the maximum voltage of the pulse. Consider the V_{TIME} measurement result as the V_{SEH} value.
6 Continue the previous step with another nine valid positive pulses that were found in the waveform.
7 Determine the worst result from the set of V_{SEH} measured.

Expected/Observable Results

- The worst measured V_{SEH} must be within the specification limit.

VSEL(Clock Plus)

Test Overview

The purpose of this test is to verify that the minimum voltage of the low pulse must be within the conformance limit of the V_{SEL} value as specified in the JEDEC specification.

The value of V_{DD} (which directly affects the conformance limit) is set to 1.5V for DDR3 and 1.2V for LPDDR3. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DD}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Plus Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 8 Single-ended Levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL#, and DQSU#

Symbol	Parameter	DDR3-800/1066/1333/1600		Units
		Min	Max	
V_{SEL}	Single-ended low level for clocks	Note 3[a]	$(V_{DD}/2)$ - 0.175	V

a: Refers to Note 3 in Table 27 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (V_{IH}(dc) max, V_{IL}(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Table 9 Single-ended Levels for CK_t, DQS_t, CK_c, and DQS_c

Symbol	Parameter	Value		Units	Notes
		Min	Max		
$V_{SEL(AC)}$	Single-ended low level for CK_t, CK_c	Note 3[c]	$(V_{DDCA}/2)$ - 0.220	V	1[a], 2[b]

a: Refers to Note 1 in Table 39 of the *JEDEC Standard JESD209-3*. For CK_t, CK_c, use V_{SEH}/V_{SEL}(ac) of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use V_{IH}/V_{IL}(ac) of DQs.

b: Refers to Note 2 in Table 39 of the *JEDEC Standard JESD209-3*. V_{IH}(ac)/V_{IL}(ac) for DQs is based on V_{REFDQ}; V_{SEH}(ac)/V_{SEL}(ac) for CA is based on V_{REFCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

c: Refers to Note 3 in Table 39 of the *JEDEC Standard JESD209-3*. These values are not defined, however.the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits (V_{IH}(dc) max, V_{IL}(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.5 “Overshoot and Undershoot Specifications” on page 92 of the specification document.

Test References

- See *Table 27 in Section 8.3 of the DDR3 SDRAM Specification, JEDEC Standard JESD79-3E, July 2010* and
- See *Figure 124 and Table 40 in Section 7 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1. Precondition the oscilloscope.
2. Trigger on a rising edge of the clock signal under test.
3. Find all valid Clock negative pulses in the entire waveform. A valid Clock negative pulse starts at the V_{REF} crossing on a valid Clock falling edge and ends at the V_{REF} crossing on the following valid Clock rising edge.
4. For the first valid Clock negative pulse, zoom in on the pulse so that it appears on the oscilloscope’s display and measure T_{MIN}.
5. Measure V_{TIME} at the found T_{MIN} to obtain the minimum voltage of the pulse. Consider the V_{TIME} measurement result as the V_{SEL} value.
6. Continue the previous step with another nine valid negative pulses that were found in the waveform.
7. Determine the worst result from the set of V_{SEL} measured.

Expected/Observable Results

- The worst measured V_{SEL} must be within the specification limit.

Overshoot Amplitude / Area for Clock Plus Tests

Test Overview

The Overshoot test can be divided into two sub-tests: Overshoot amplitude and Overshoot area.

The purpose of this test is to verify that the overshoot value of the test signal found from all regions of the acquired waveform is lower than or equal to the conformance limit of the maximum peak amplitude allowed for overshoot as specified in the JEDEC specification.

When there is an overshoot, the area is calculated based on the overshoot width and overshoot amplitude. The Overshoot area should be lower than or equal to the conformance limit of the maximum overshoot area allowed as specified in the JEDEC specification.

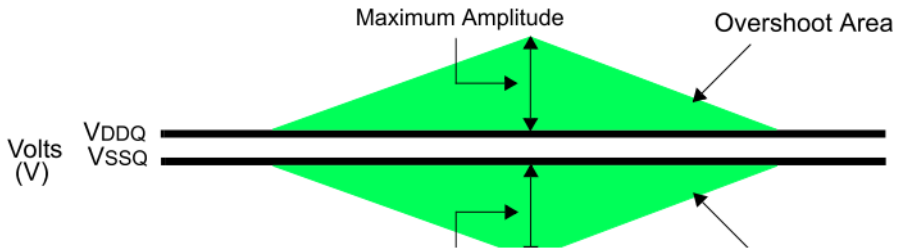


Figure 9 Clock Overshoot

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Plus Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 10 AC Overshoot Specification for Clock and Mask Pins

Parameter	Specification					
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133
Maximum peak amplitude allowed for overshoot area	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V
Maximum overshoot area above V_{DDQ}	0.25 V/ns	0.19 V/ns	0.15 V/ns	0.13 V/ns	0.11 V/ns	0.10 V/ns

Table 11 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for overshoot area	Max	0.35		V
Maximum area above V_{DD}	Max	0.12	0.10	V-ns

Test References

- See *Figure 100 and Table 37 in Section 9 of the DDR3 SDRAM Specification, the JEDEC Standard JESD79-3E, July 2010* and
- See *Figure 126 and Table 49 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Set the number of sampling points to 2M samples.

2 Sample/acquire signal data and then perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Find the Overshoot Region across acquired waveform. Overshoot Region start at rising VDDQ (or VDDCA) crossing and end at falling VDDQ (or VDDCA) crossing.

4 Within Overshoot Region #1, perform the following steps:

i Evaluate Overshoot Amplitude by performing the following steps:
a. Use TMAX and VMAX to get time stamp of maximum voltage on overshoot region of the acquired waveform.
b. Calculate: Overshoot Amplitude = VMAX – VDDQ (or VDDCA).

ii Evaluate Area below VDDQ (or VDDCA) = (Overshoot Region End – Overshoot Region Start) * VDDQ (or VDDCA).

iii Evaluate Total Area above 0 volt by using Trapezoidal Method Area Calculation as shown in following figure:

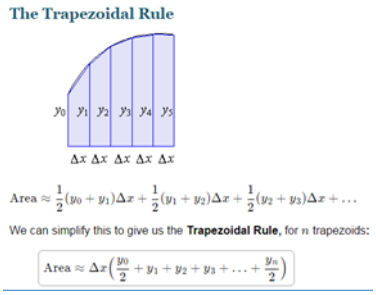


Figure 10 Trapezoidal Rule

iv Calculate area above VDDQ (or VDDCA) = Total area above 0 volt - area below VDDQ (or VDDCA).

v Store calculated result below for later worst case finding process:

- Overshoot Amplitude
- Area above VDDQ (or VDDCA)

5 Repeat the previous step for the rest Overshoot Region found in acquired waveform.

6 Find the worst result below from stored result.

7 Compare the test result to the compliance test limit.
   - Overshoot Amplitude
   - Area above VDDQ (or VDDCA)

Expected/Observable Results

- The measured maximum overshoot amplitude for the test signal must be less than or equal to the maximum overshoot value.
- The calculated overshoot area value must be less than or equal to the maximum overshoot area allowed.

Undershoot Amplitude / Area for Clock Plus Tests

Test Overview

The Undershoot Test can be divided into two sub-tests: Undershoot amplitude and Undershoot area.

The purpose of this test is to verify that the undershoot value of the test signal found from all regions of the acquired waveform is less than or equal to the conformance limit of the maximum peak amplitude allowed for undershoot as specified in the *JEDEC specification*.

When there is an undershoot, the area is calculated based on the undershoot width. The Undershoot area should be less than or equal to the conformance limit of the maximum undershoot area allowed as specified in the *JEDEC specification*.

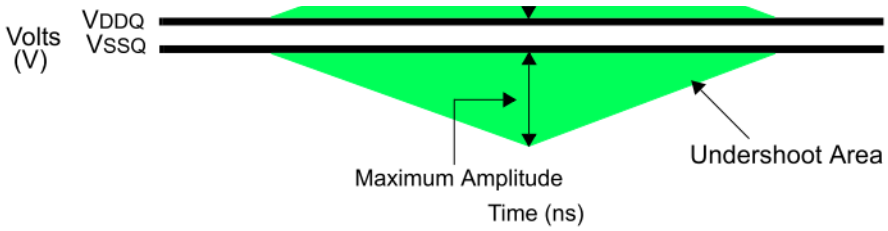


Figure 11 Clock Undershoot

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Plus Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 12 AC Undershoot Specification for Clock, Data, Strobe and Mask Pins

Parameter	Specification					
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133
Maximum peak amplitude allowed for undershoot area	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V
Maximum undershoot area below V_{SSQ}	0.25 V/ns	0.19 V/ns	0.15 V/ns	0.13 V/ns	0.11 V/ns	0.10 V/ns

Table 13 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for undershoot area	Max	0.35		V
Maximum area below V_{SS}	Max	0.12	0.10	V-ns

Test References

- See *Table 37 and Figure 100 in Section 9 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Figure 126 and Table 49 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Set the number of sampling points to 2M samples.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Obtain the undershoot region. Undershoot Region starts at falling 0 volt crossing and end at rising 0 volt crossing.

4 Within Undershoot region #1, perform the following steps:

   i Evaluate Undershoot Amplitude by performing the following steps:
   a. Use TMIN and VMIN to get time stamp of maximum voltage on undershoot region of the acquired waveform.
   b. Calculate: Undershoot Amplitude = 0- VMIN

   ii Evaluate total area below 0 volt by using Trapezoidal Method Area Calculation (refer to Figure 10)

   iii Store Calculated result below for later worst case finding process:

   - Undershoot Amplitude
   - Total area below 0 volt

5 Repeat the previous step for the rest Undershoot Region found in acquired waveform.

6 Find the worst result below from stored result.

7 Compare test result to the compliance test limit.

   - Undershoot Amplitude
   - Total area below 0 volt

Expected/Observable Results

- The measured minimum voltage value for the test signal must be less than or equal to the maximum undershoot value.
- The calculated undershoot area value must be less than or equal to the maximum undershoot area allowed.

SlewR on Setup Region

Test Overview

The purpose of this test is to calculate the rising slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Plus Signals

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire the signal.

2 Find all valid rising edges in the whole acquisition. A valid rising edge starts at VIL (ac) crossing and end at following VIH (ac) crossing.

3 For all valid rising edges, find the transition time, delta TR which is time starts at VREF crossing and end at following VIH (ac) crossing. Then calculate Rising Slew.

$$\text{Rising Slew} = \frac{V_{IH(ac)}\ \text{min} - V_{REF}}{\text{delta TR}}$$

4 Determine the worst result from the set of SlewR measured.

Expected/Observable Results

- The calculated Rising Slew value for the test signal shall meet the user defined limit.

SlewF on Setup Region

Test Overview

The purpose of this test is to calculate the falling slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Modes Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Plus Signals

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire the signal.

2 Find all valid falling edges in the whole acquisition. A valid falling edge starts at VIH (ac) crossing and end at following VIL (ac) crossing.

3 For all valid falling edges, find the transition time, delta TF which is time starts at VREF crossing and end at following VIL (ac) crossing. Then calculate Falling Slew.

$$\text{Falling Slew} = \frac{V_{REF} - V_{IL(ac)}\ \text{max}}{\text{delta TF}}$$

4 Determine the worst result from the set of SlewF measured.

Expected/Observable Results

- The calculated Falling Slew value for the test signal shall meet the user defined limit.

SlewR on Hold Region

Test Overview

The purpose of this test is to calculate the rising slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Plus Signals

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire the signal.

2 Find all valid rising edges in the whole acquisition. A valid rising edge starts at VIL (ac) crossing and end at following VIH (ac) crossing.

3 For all valid rising edges, find the transition time, delta TR which is time starts at VREF crossing and end at following VIH (ac) crossing. Then calculate Rising Slew.

$$Rising\ Slew = \frac{V_{REF} - V_{IL(DC)}}{\text{delta TR}}$$

4 Determine the worst result from the set of SlewR measured.

Expected/Observable Results

- The calculated Rising Slew value for the test signal must meet the user defined limit.

SlewF on Hold Region

Test Overview

The purpose of this test is to calculate the falling slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Plus Signals

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire the signal.

2 Find all valid falling edges in the whole acquisition. A valid falling edge starts at VIH (ac) crossing and end at following VIL (ac) crossing.

3 For all valid falling edges, find the transition time, delta TF which is time starts at VREF crossing and end at following VIL (ac) crossing. Then calculate Falling Slew.

$$Falling\ Slew = \frac{V_{IH(DC)} - V_{REF}}{\text{delta TF}}$$

4 Determine the worst result from the set of SlewF measured.

Expected/Observable Results

- The calculated Falling Slew value for the test signal shall meet the user defined limit.

4 Clock Minus Tests Group

This section provides the Methods of Implementation (MOIs) for Clock Minus tests for Clocks using a Keysight Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

NOTE Both XYZ# and $\overline{XYZ}$ refer to complement. Thus, CK# is the same as $\overline{CK}$.

Probing for Clock Minus Tests

When performing the Clock Minus tests for Clocks, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Clock Minus tests for Clocks may look similar to the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance application for the exact number of probe connections.

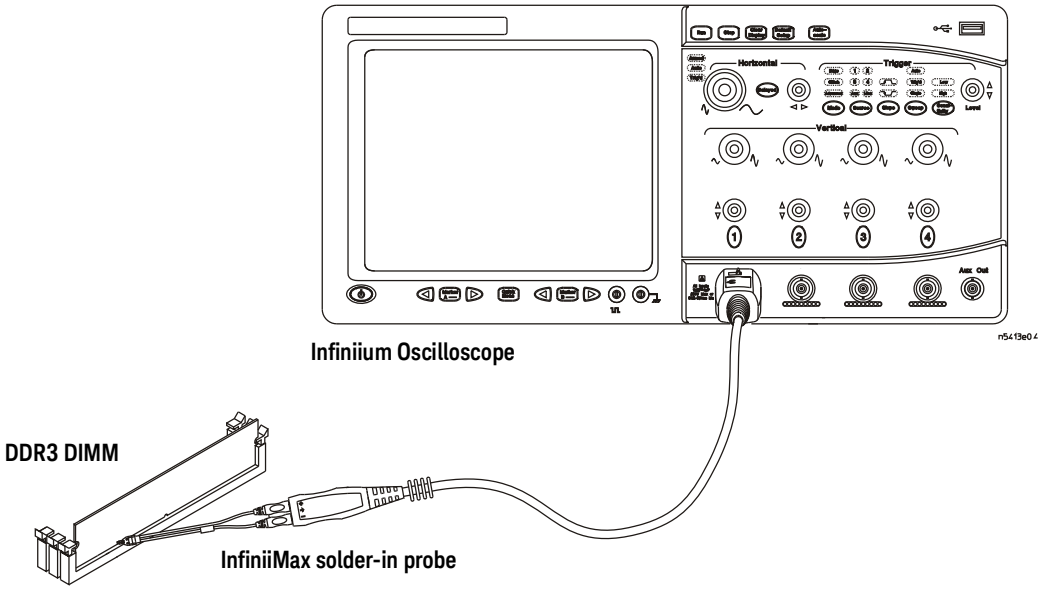


Figure 12 Probing for Clock Minus Tests

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 12 are just examples).

For more information on the probe amplifiers and differential probe heads, refer to the respective user guide for Probes.

Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the **Set Up** tab.

6 Select the **Test Mode**, **SDRAM Type**, **Speed Grade**, and **AC Levels** options.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

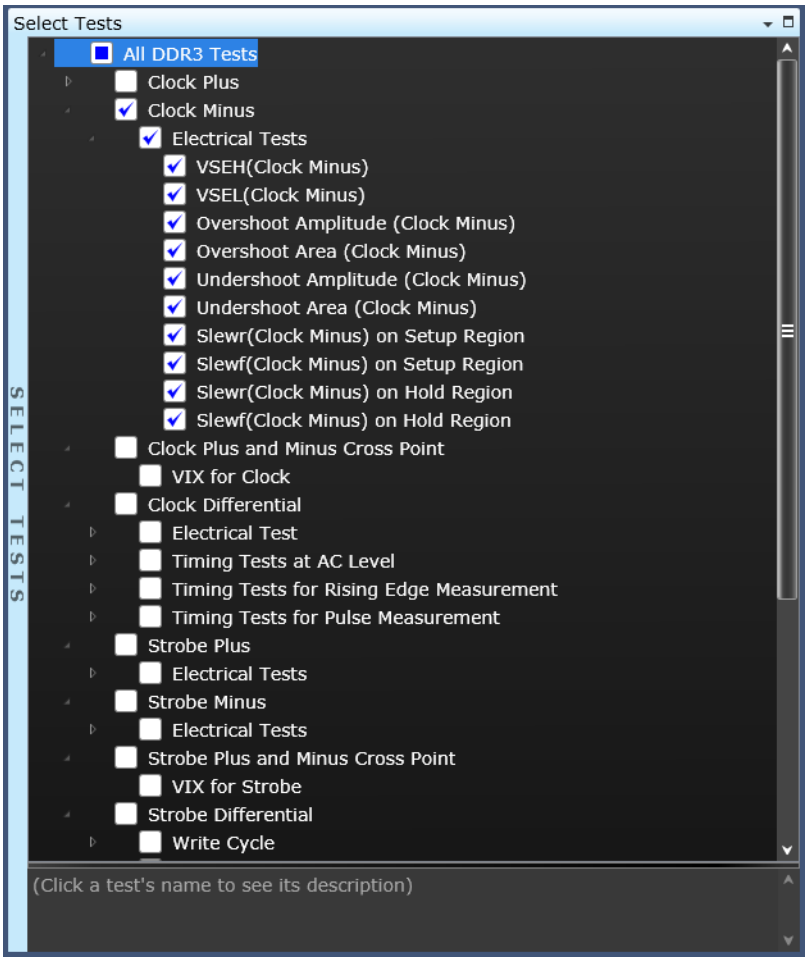


Figure 13 Selecting Clock Minus Tests

Electrical Tests

VSEH(Clock Minus)

Test Overview

The purpose of this test is to verify that the maximum voltage of the high pulse must be within the conformance limit of the V_{SEH} value as specified in the JEDEC specification.

The value of V_{DD} (which directly affects the conformance limit) is set to 1.5V for DDR3 and 1.2V for LPDDR3. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DD}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Minus Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 14 Single-ended Levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL# or DQSU#

Symbol	Parameter	DDR3-800/1066/1333/1600		Units
		Min	Max	
V_{SEH}	Single-ended high level for clocks	$(V_{DD}/2) + 0.175$	Note 3[a]	V

a: Refers to Note 3 in Table 27 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Table 15 Single-ended Levels for CK_t, DQS_t, CK_c, and DQS_c

Symbol	Parameter	Value		Units	Notes
		Min	Max		
$V_{SEH(AC)}$	Single-ended high level for CK_t, CK_c	$(V_{DDCA}/2) + 0.220$	Note 3[c]	V	1[a], 2[b]

a: Refers to Note 1 in Table 39 of the *JEDEC Standard JESD209-3*. For CK_t, CK_c, use $V_{SEH}/V_{SEL(ac)}$ of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use $V_{IH}/V_{IL(ac)}$ of DQs.

b: Refers to Note 2 in Table 39 of the *JEDEC Standard JESD209-3*. $V_{IH(ac)}/V_{IL(ac)}$ for DQs is based on V_{REFDQ}; $V_{SEH(ac)}/V_{SEL(ac)}$ for CA is based on V_{REFCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

c: Refers to Note 3 in Table 39 of the *JEDEC Standard JESD209-3*. These values are not defined, however.the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.5 “Overshoot and Undershoot Specifications” on page 92 of the specification document.

Test References

- See *Table 27 in Section 8.3 of the DDR3 SDRAM Specification, JEDEC Standard JESD79-3E, July 2010* and
- See *Figure 124 and Table 40 in Section 7 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3, December 2011*.

Measurement Algorithm

1 Precondition the oscilloscope.

2 Trigger on a rising edge of the clock signal under test.

3 Find all valid Clock positive pulses in the entire waveform. A valid Clock positive pulse starts at the V_{REF} crossing on a valid Clock rising edge and ends at the V_{REF} crossing on the following valid Clock falling edge.

4 For the first valid Clock positive pulse, zoom in on the pulse so that it appears on the oscilloscope's display and measure T_{MAX}.

5 Measure V_{TIME} at the found T_{MAX} to obtain the maximum voltage of the pulse. Consider the V_{TIME} measurement result as the V_{SEH} value.

6 Continue the previous step with another nine valid positive pulses that were found in the waveform.

7 Determine the worst result from the set of V_{SEH} measured.

Expected/Observable Results

- The worst measured V_{SEH} must be within the specification limit.

VSEL(Clock Minus)

Test Overview

The purpose of this test is to verify that the minimum voltage of the low pulse must be within the conformance limit of the V_{SEL} value as specified in the JEDEC specification.

The value of V_{DD} (which directly affects the conformance limit) is set to 1.5V for DDR3 and 1.2V for LPDDR3. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DD}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Minus Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 16 Single-ended Levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL#, and DQSU#

Symbol	Parameter	DDR3-800/1066/1333/1600		Units
		Min	Max	
V_{SEL}	Single-ended low level for clocks	Note 3[a]	$(V_{DD}/2)$ - 0.175	V

a: Refers to Note 3 in Table 27 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Table 17 Single-ended Levels for CK_t, DQS_t, CK_c, and DQS_c

Symbol	Parameter	Value		Units	Notes
		Min	Max		
$V_{SEL(AC)}$	Single-ended low level for CK_t, CK_c	Note 3[c]	$(V_{DDCA}/2)$ - 0.220	V	1[a], 2[b]

a: Refers to Note 1 in Table 39 of the *JEDEC Standard JESD209-3*. For CK_t, CK_c, use $V_{SEH}/V_{SEL(ac)}$ of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use $V_{IH}/V_{IL(ac)}$ of DQs.

b: Refers to Note 2 in Table 39 of the *JEDEC Standard JESD209-3*. $V_{IH(ac)}/V_{IL(ac)}$ for DQs is based on V_{REFDQ}; $V_{SEH(ac)}/V_{SEL(ac)}$ for CA is based on V_{REFCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

c: Refers to Note 3 in Table 39 of the *JEDEC Standard JESD209-3*. These values are not defined, however.the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.5 “Overshoot and Undershoot Specifications” on page 92 of the specification document.

Test References

- See *Table 27 in Section 8.3 of the DDR3 SDRAM Specification, JEDEC Standard JESD79-3E, July 2010* and
- See *Figure 124 and Table 40 in Section 7 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3, December 2011*.

Measurement Algorithm

1 Precondition the oscilloscope.

2 Trigger on a rising edge of the clock signal under test.

3 Find all valid Clock negative pulses in the entire waveform. A valid Clock negative pulse starts at the V_{REF} crossing on a valid Clock falling edge and ends at the V_{REF} crossing on the following valid Clock rising edge.

4 For the first valid Clock negative pulse, zoom in on the pulse so that it appears on the oscilloscope's display and measure T_{MIN}.

5 Measure V_{TIME} at the found T_{MIN} to obtain the minimum voltage of the pulse. Consider the V_{TIME} measurement result as the V_{SEL} value.

6 Continue the previous step with another nine valid negative pulses that were found in the waveform.

7 Determine the worst result from the set of V_{SEL} measured.

Expected/Observable Results

- The worst measured V_{SEL} must be within the specification limit.

Overshoot Amplitude / Area (Clock Minus)

Test Overview

The Overshoot tests can be divided into two sub-tests: Overshoot amplitude and Overshoot area.

The purpose of this test is to verify that the overshoot value of the test signal found from all regions of the acquired waveform is lower than or equal to the conformance limit of the maximum peak amplitude allowed for overshoot as specified in the JEDEC specification.

When there is an overshoot, the area is calculated based on the overshoot width and overshoot amplitude. The Overshoot area should be lower than or equal to the conformance limit of the maximum overshoot area allowed as specified in the JEDEC specification.

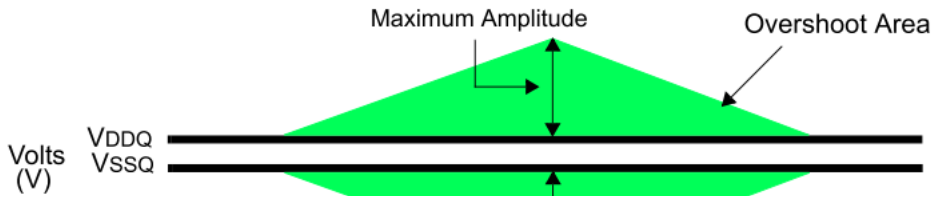


Figure 14 Clock and Mask Overshoot

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Minus Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 18 AC Overshoot Specification for Clock and Mask Pins

Parameter	Specification					
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133
Maximum peak amplitude allowed for overshoot area	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V
Maximum overshoot area above V_{DDQ}	0.25 V-ns	0.19 V-ns	0.15 V-ns	0.13 V-ns	0.11 V-ns	0.10 V-ns

Table 19 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for overshoot area	Max	0.35		V
Maximum area above V_{DD}	Max	0.12	0.10	V-ns

Test References

- See *Figure 100 and Table 37 in Section 9 of the DDR3 SDRAM Specification, JEDEC Standard JESD79-3E, July 2010* and
- See *Figure 126 and Table 49 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Set the number of sampling points to 2M samples.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Obtain the overshoot region. Overshoot region starts at the rising VDDQ (or VDDCA) crossing and ends at the falling VDDQ (or VDDCA) crossing.

4 Within Overshoot region #1, perform the following steps:

i Evaluate Overshoot Amplitude by performing the following steps:

- Use TMAX and VMAX to get time stamp of maximum voltage on overshoot region of the acquired waveform.
- Calculate: Overshoot Amplitude = VMAX – VDDQ (or VDDCA).

ii Evaluate Area below VDDQ (or VDDCA) = (Overshoot Region End – Overshoot Region Start) * VDDQ (or VDDCA).

iii Evaluate Total Area above 0 volt by using Trapezoidal Method Area Calculation as shown in following figure:

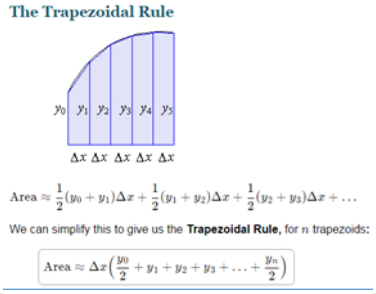


Figure 15 Trapezoidal Rule

iv Calculate area above VDDQ (or VDDCA) = Total area above 0 volt - area below VDDQ (or VDDCA).

v Store calculated result below for later worst case finding process:

- Overshoot Amplitude
- Area above VDDQ (or VDDCA)

5 Repeat the previous step for the rest Overshoot Region found in acquired waveform.

6 Find the worst result below from stored result. Compare test result to the compliance test limit.

- Overshoot Amplitude
- Area above VDDQ (or VDDCA)

Expected/Observable Results

- The measured maximum voltage value must be less than or equal to the maximum overshoot value.
- The calculated Overshoot area value must be less than or equal to the maximum Overshoot area allowed.

Undershoot Amplitude / Area (Clock Minus)

Test Overview

The Undershoot Test can be divided into two sub-tests: Undershoot amplitude and Undershoot area.

The purpose of this test is to verify that the undershoot value of the test signal found from all regions of the acquired waveform is less than or equal to the conformance limit of the maximum peak amplitude allowed for undershoot as specified in the *JEDEC* specification.

When there is an undershoot, the area is calculated based on the undershoot width. The Undershoot area should be less than or equal to the conformance limit of the maximum undershoot area allowed as specified in the *JEDEC* specification.

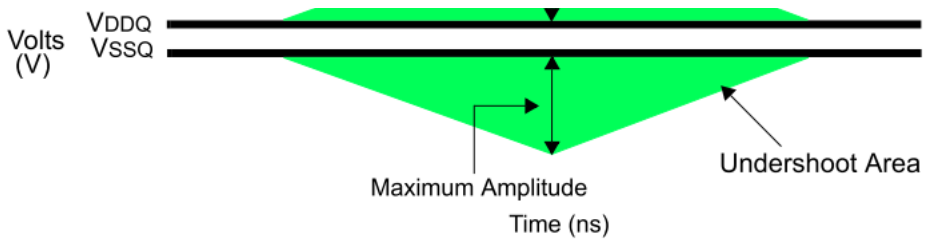


Figure 16 Clock Undershoot

Modes Supported

- DDR3, DDR3L, and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Minus Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 20 AC Undershoot Specification for Clock, Data, Strobe and Mask Pins

Parameter	Specification					
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133
Maximum peak amplitude allowed for undershoot area	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V
Maximum undershoot area below V_{SSQ}	0.25 V-ns	0.19 V-ns	0.15 V-ns	0.13 V-ns	0.11 V-ns	0.10 V-ns

Table 21 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for undershoot area	Max	0.35		V
Maximum area below V_{SS}	Max	0.12	0.10	V-ns

Test References

- See *Figure 100 and Table 37 in Section 9 of the DDR3 SDRAM in the JEDEC Standard JESD79-3E, July 2010.*
- See *Figure 126 and Table 49 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Set the number of sampling points to 2M samples.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Obtain the undershoot region. Undershoot Region starts at falling 0 volt crossing and end at rising 0 volt crossing.

4 Within Undershoot region #1, perform the following steps:

   i Evaluate Undershoot Amplitude by performing the following steps:
   a. Use TMIN and VMIN to get time stamp of maximum voltage on undershoot region of the acquired waveform.
   b. Calculate: Undershoot Amplitude = 0- VMIN

   ii Evaluate total area below 0 volt by using Trapezoidal Method Area Calculation (refer to Figure 15)

   iii Store Calculated result below for later worst case finding process:

   - Undershoot Amplitude
   - Total area below 0 volt

5 Repeat the previous step for the rest Undershoot Region found in acquired waveform.

6 Find the worst result below from stored result.

7 Compare test result to the compliance test limit.

   - Undershoot Amplitude
   - Total area below 0 volt

Expected/Observable Results

- The measured minimum voltage value for the test signal must be less than or equal to the maximum undershoot value.
- The calculated undershoot area value must be less than or equal to the maximum undershoot area allowed.

SlewR on Setup Region

Test Overview

The purpose of this test is to calculate the rising slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Modes Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Minus Signals

Signals required to perform the test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.

Test References

There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire the signal.

2 Find all valid rising edges in the whole acquisition. A valid rising edge starts at VIL (ac) crossing and end at following VIH (ac) crossing.

3 For all valid rising edges, find the transition time, delta T_R which is time starts at VREF crossing and end at following VIH (ac) crossing. Then calculate Rising Slew.

$$\text{Rising Slew} = \frac{V_{IH(ac)}\ \text{min} - V_{REF}}{\text{delta TR}}$$

4 Determine the worst result from the set of SlewR measured.

Expected/Observable Results

- The calculated Rising Slew value for the test signal shall meet the user defined limit.

SlewF on Setup Region

Test Overview

The purpose of this test is to calculate the falling slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Modes Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Minus Signals

Signals required to perform the test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above

Test References

There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire the signal.
2 Find all valid falling edges in the whole acquisition. A valid falling edge starts at VIH (ac) crossing and end at following VIL (ac) crossing.
3 For all valid falling edges, find the transition time, delta T_F which is time starts at VREF crossing and end at following VIL (ac) crossing. Then calculate Falling Slew.

$$\text{Falling Slew} = \frac{V_{REF} - V_{IL(ac)}\ \text{max}}{\text{delta TF}}$$

4 Determine the worst result from the set of SlewF measured.

Expected/Observable Results

- The calculated Falling Slew value for the test signal shall meet the user defined limit.

SlewR on Hold Region

Test Overview

The purpose of this test is to calculate the rising slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Modes Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Minus Signals

Required Signals that are needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire the signal.

2 Find all valid rising edges in the whole acquisition. A valid rising edge starts at VIL (ac) crossing and end at following VIH (ac) crossing.

3 For all valid rising edges, find the transition time, delta TR which is time starts at VREF crossing and end at following VIH (ac) crossing. Then calculate Rising Slew.

$$Rising\ Slew = \frac{V_{REF} - V_{IL(DC)}}{\text{delta TR}}$$

4 Determine the worst result from the set of SlewR measured.

Expected/Observable Results

- The calculated Rising Slew value for the test signal shall meet the user defined limit.

SlewF on Hold Region

Test Overview

The purpose of this test is to calculate the falling slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Minus Signals

Required Signals that are needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire the signal.

2 Find all valid falling edges in the whole acquisition. A valid falling edge starts at VIH (ac) crossing and end at following VIL (ac) crossing.

3 For all valid falling edges, find the transition time, delta TF which is time starts at VREF crossing and end at following VIL (ac) crossing. Then calculate Falling Slew.

$$Falling\ Slew = \frac{V_{IH(DC)} - V_{REF}}{\text{delta TF}}$$

4 Determine the worst result from the set of SlewF measured.

Expected/Observable Results

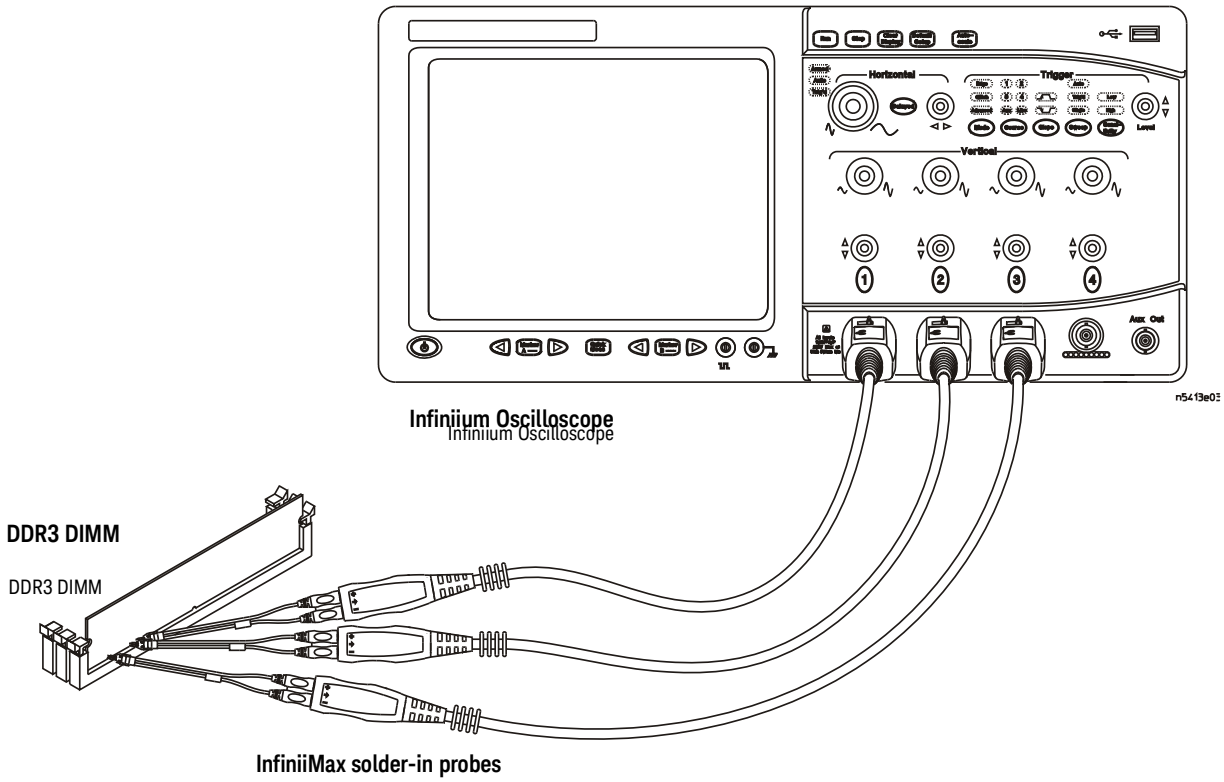
- The calculated Falling Slew value for the test signal shall meet the user defined limit.

5 Clock Plus and Minus Cross Point Tests Group

This section provides the Methods of Implementation (MOIs) for Clock Plus and Minus Cross Point tests using a Keysight Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

Probing for Clock Plus and Minus Cross Point Tests

When performing the Clock Plus and Minus Cross Point tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Clock Plus and Minus Cross Point tests may look similar to the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance application for the exact number of probe connections.



InfiniiMax solder-in probes

Figure 17 Probing for Clock Plus and Minus Cross Point Tests

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 17 are just examples).

For more information on the probe amplifiers and differential probe heads, refer to the respective user guide for Probes.

Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform test on all unused RAM on the system by producing repetitive burst of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the **Set Up** tab.

6 Select the **Test Mode**, **SDRAM Type, Speed Grade**, and **AC Levels** options.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

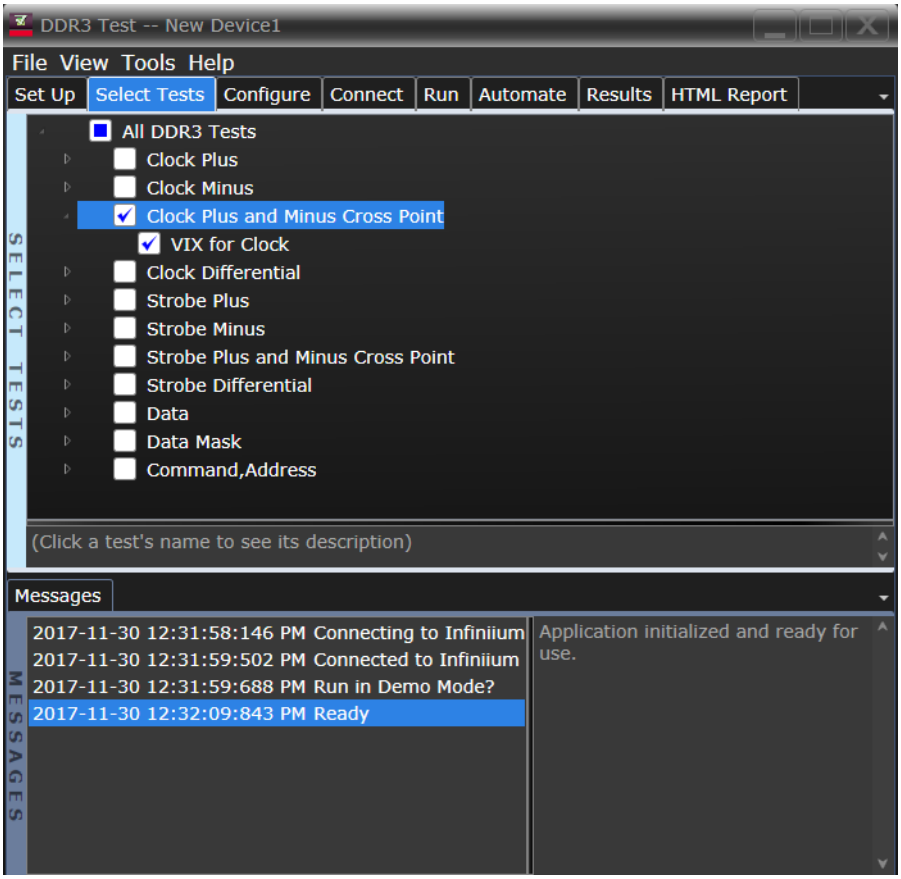


Figure 18 Selecting Clock Plus and Minus Cross Point Tests

VIX for Clock

Test Overview

The purpose of this test is to verify crossing point voltage value of the input differential pair test signals is within the conformance limits of the VIX (ac) as specified in the JEDEC specification.

The value of VDDQ which directly affect the conformance upper limit is default to 1.5V for typical DDR3 and 1.35V for DDR3L but users have the flexibility to change this value.

Modes Supported

- DDR3 and DDR3L

Signal cycle of Interest

- Write

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Plus Signals and Clock Minus Signals

Signals required to perform the test on the oscilloscope

- Clock Plus Signals
- Clock Minus Signals

Test Definition Notes from the Specification

Table 22 Cross Point Voltage for Differential Input Signals (CK, DQS)

Symbol	Parameter	DDR3-800/1066/1333/1600/1866/2133		Units
		Min	Max	
$V_{IX(CK)}$	Differential Input Cross Point Voltage relative to $V_{DDCA}/2$ for CK, CK#	-150	150	mV
		-175	175	mV

Table 23 Cross Point Voltage for Differential Input Signals (CK, DQS)

Symbol	Parameter	DDR3L-800, 1066, 1333 & 1600		Units
		Min	Max	
V_{IXC}	Differential Input Cross Point Voltage relative to $V_{DDCA}/2$ for CK, CK#	-150	150	mV

Test References

- See *Figure 94 and Table 28 in Section 8 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Table 23 in Section 11of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1, July 2010.*

Measurement Algorithm

1 Sample/Acquire data waveforms.
2 Use Subtract FUNC to generate the differential waveform from the 2 source input
3 Fine all differential CLK crossing that cross 0V.
4 Use VTime to get the actual crossing point voltage value using the time stamp obtained
5 For each cross point voltage, calculate the final result. VIX(AC) = cross point voltage - VDD/2.
6 Determine the worst result from the set of VIX(AC) measured.

Expected/Observable Results

- The measured crossing point value for the differential test signals pair must be within the conformance limit of the $V_{IX(AC)}$ value.

VIXCA for Clock

Test Overview

The purpose of this test is to verify crossing point voltage value of the input differential pair test signals is within the conformance limits of the VIXCA as specified in the JEDEC specification

Modes Supported

- LPDDR3

Signal cycle of Interest

- Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Plus Signals and Clock Minus Signals

Signals required to perform the test on the oscilloscope

- Clock Plus Signals
- Clock Minus Signal

Test Definition Notes from the Specification

Table 24 Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	Min	Max	Units
V_{IXCA}	Differential Input Cross Point Voltage relative to $V_{DDCA/2}$ for CK_t,CK_c	-120	120	mV

Test References

- See *Figure 123 and Table 41 in Section 7 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Sample/Acquire the data waveforms.
2 Use Subtract FUNC to generate the differential waveform from the 2 source input
3 Find all the differential CLK crossing that cross 0V.
4 Use VTime to get the actual crossing point voltage value using the timestamp obtained
5 For each cross point voltage, calculate the final result. VIXCA= cross point voltage - VDDCA/2
6 Determine the worst result from the set of V_{IXCA} measured.

Expected/Observable Results

- The measured crossing point value for the differential test signals pair must be within the conformance limit of the VIXCA value.

6 Clock Differential Tests Group

This section provides the Methods of Implementation (MOIs) for Clock Differential tests using a Keysight Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

Probing for Clock Differential Tests

When performing the Clock Differential tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Clock Differential tests may look similar to the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance application for the exact number of probe connections.

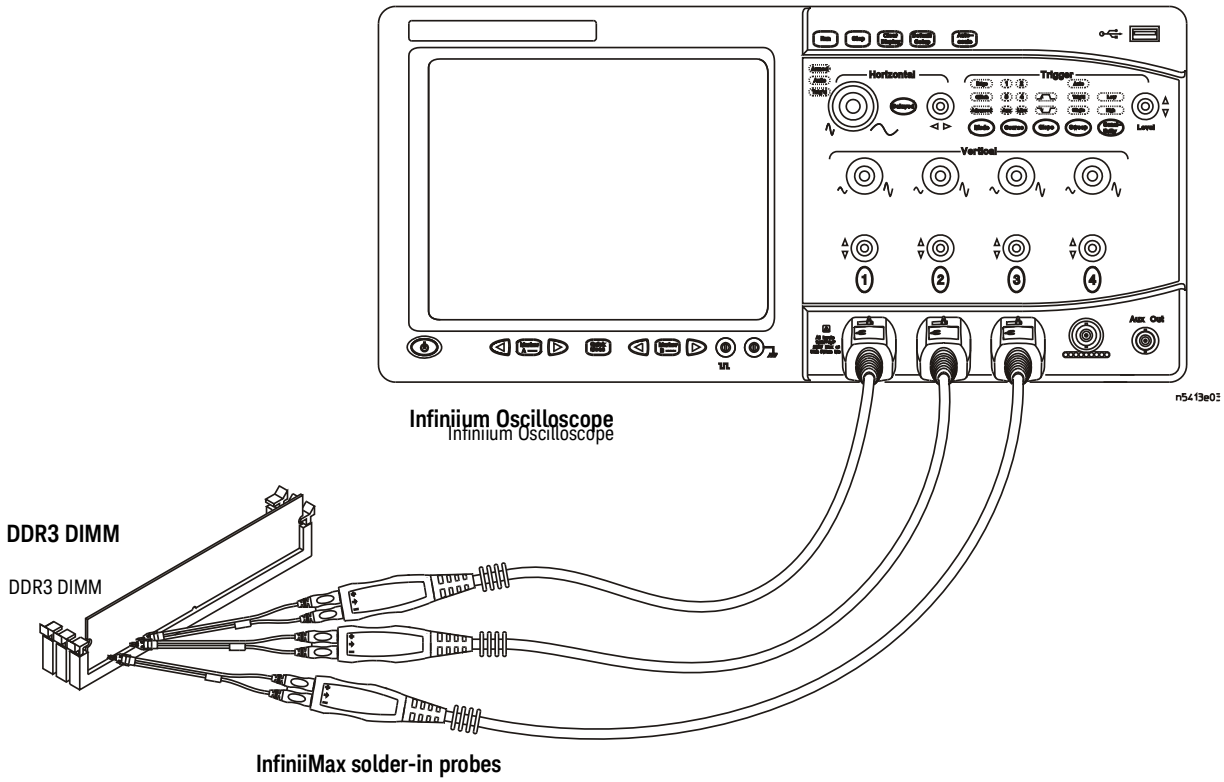


Figure 19 Probing for Clock Differential Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 19 are just examples).

For more information on the probe amplifiers and differential probe heads, refer to the respective user guide for Probes.

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Test Procedure

1 Start the automated test application as described in “Starting the DDR3 Compliance Test Application" on page 25.
2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform test on all unused RAM on the system by producing repetitive burst of read-write data signals to the DDR3 memory.
3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.
4 Connect the oscilloscope probes to any channels of the oscilloscope.
5 In the DDR3 Test application, click the **Set Up** tab.
6 Select the **Test Mode**, **SDRAM Type, Speed Grade**, and **AC Levels** options.
7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

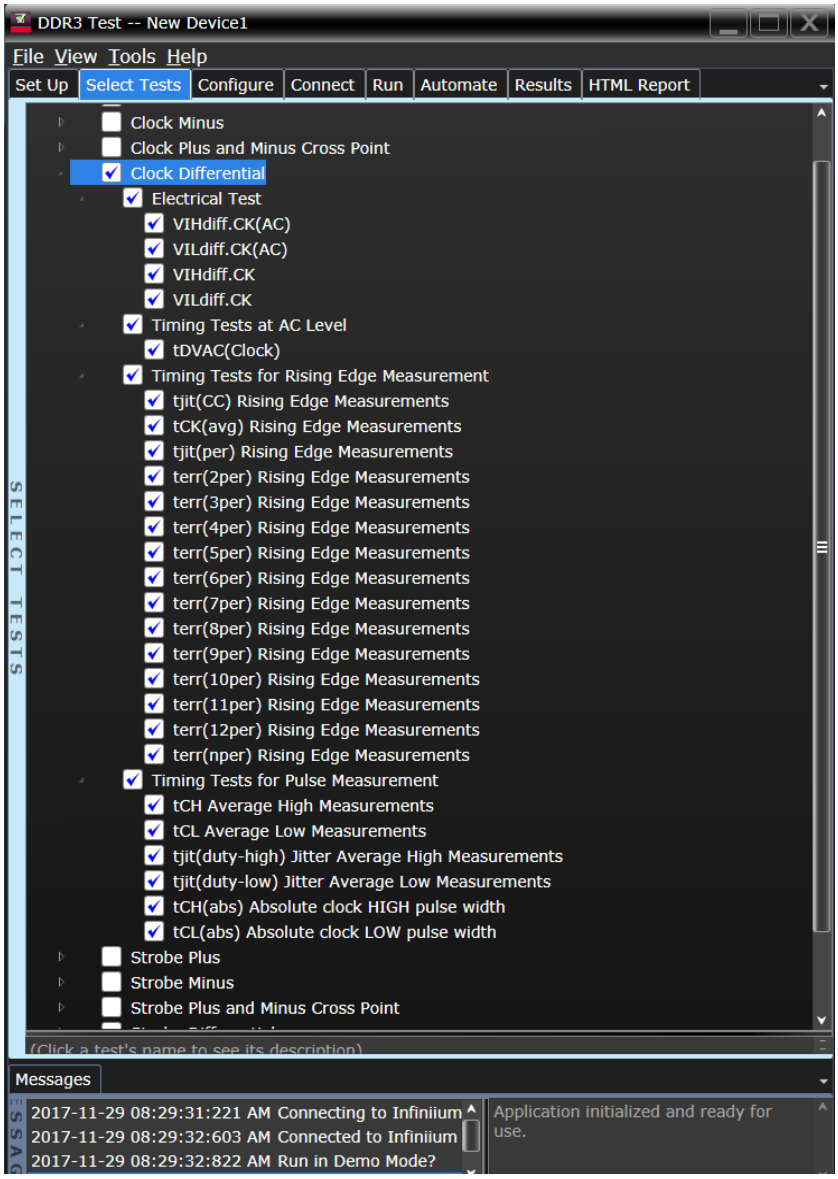


Figure 20 Selecting Clock Differential Tests

Electrical Tests

VIHdiff.CK(AC)

Test Overview

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{IHdiff(AC)}$ value as specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance limit) is set to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of $V_{IH(AC)}$ (which directly affects the conformance limit) is set according to the *JEDEC specification* based on the selected Data Rate, Test Type, and AC Level. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of $V_{IH(AC)}$.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 25 Differential AC and DC Input Levels

Symbol	Parameter	DDR3-800/1066/1333/1600		Units
		Min	Max	
$V_{IHdiff(AC)}$	Differential input high AC for clock	2 x ($V_{IH(AC)}$ - V_{REF})	Note 3[a]	V

a: Refers to Note 3 in Table 27 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Table 26 Differential AC and DC Input Levels

Symbol	Parameter	Value		Unit	Notes
		Min	Max		
$V_{IHdiff(AC)}$	Differential input high AC	2 x ($V_{IH(AC)}$ - V_{REF})	Note 3[b]	V	2[a]

a: Refers to Note 2 in Table 36 of the *JEDEC Standard JESD209-3*. For CK_t - CK_c, use $V_{IH}/V_{IL(AC)}$ of CA and V_{REFCA}; for DQS_t - DQS_c, use $V_{IH}/V_{IL(AC)}$ of DQs and V_{REFDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

b: Refers to Note 3 in Table 36 of the *JEDEC Standard JESD209-3*. These values are not defined, however.the single-ended signals CK_t, CK_c, DQS_t and DQS_c need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.5 “Overshoot and Undershoot Specifications” on page 92 of the specification document.

Test References

- See *Table 25 in Section 8.3 of the DDR3 and SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Table 38 in Section 7 of the LPDDR3 and SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Precondition the oscilloscope.
2 Trigger on a rising edge of the clock signal under test.
3 Find all valid Clock positive pulses in the entire waveform. A valid Clock positive pulse starts at the 0V crossing on a valid Clock rising edge and ends at the 0V crossing on the following valid Clock falling edge.
4 For the first valid Clock positive pulse, zoom in on the pulse so that it appears on the oscilloscope’s display and perform the VTOP measurement. Take the VTOP measurement result as the $V_{IHdiff(AC)}$ value.
5 Continue the previous step with another nine valid positive pulses that were found in the waveform.
6 Determine the worst result from the set of $V_{IHdiff(AC)}$ measured.

Expected/Observable Results

- The worst measured $V_{IHdiff(AC)}$ must be within the specification limit.

VILdiff.CK(AC)

Test Overview

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{ILdiff(AC)}$ value as specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance limit) is set to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of $V_{IL(AC)}$ (which directly affects the conformance limit) is set according to the *JEDEC specification* based on the selected Data Rate, Test Type, and AC Level. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of $V_{IL(AC)}$.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 27 Differential AC and DC Input Levels

Symbol	Parameter	DDR3-800/1066/1333/1600		Units
		Min	Max	
$V_{ILdiff(AC)}$	Differential input low AC for clock	Note 3[a]	2 x ($V_{IL(AC)}$ - V_{REF})	V

a: Refers to Note 3 in Table 25 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Table 28 Differential AC and DC Input Levels

Symbol	Parameter	Value		Unit	Notes
		Min	Max		
$V_{ILdiff(AC)}$	Differential input low AC	Note 3[b]	2 x ($V_{IL(AC)}$ - V_{REF})	V	2[a]

a: Refers to Note 2 in Table 36 of the *JEDEC Standard JESD209-3*. For CK_t - CK_c, use $V_{IH}/V_{IL(AC)}$ of CA and V_{REFCA}; for DQS_t - DQS_c, use $V_{IH}/V_{IL(AC)}$ of DQs and V_{REFDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

b: Refers to Note 3 in Table 36 of the *JEDEC Standard JESD209-3*. These values are not defined, however.the single-ended signals CK_t, CK_c, DQS_t and DQS_c need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.5 “Overshoot and Undershoot Specifications” on page 92 of the specification document.

Test References

- See *Table 25 in Section 8.3 of the DDR3 and SDRAM Specification in the JEDEC Standard JESD79-3E,July 2010* and
- See *Table 38 in Section 7 of the LPDDR3 and SDRAM in the JEDEC Standard JESD209-3, December 2011*.

Measurement Algorithm

1 Precondition the oscilloscope.
2 Trigger on a rising edge of the clock signal under test.
3 Find all valid Clock negative pulses in the entire waveform. A valid Clock negative pulse starts at the 0V crossing on a valid Clock falling edge and ends at the 0V crossing on the following valid Clock rising edge.
4 For the first valid Clock negative pulse, zoom in on the pulse so that it appears on the oscilloscope’s display and perform the VBASE measurement. Take the VBASE measurement result as the $V_{ILdiff(AC)}$ value.
5 Continue the previous step with another nine valid negative pulses that were found in the entire waveform.
6 Determine the worst result from the set of $V_{ILdiff(AC)}$ measured.

Expected/Observable Results

- The worst measured $V_{ILdiff(AC)}$ must be within the specification limit.

VIHdiff.CK(DC)

Test Overview

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{IHdiff(DC)}$ value as specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance limit) is set to 0.6V for LPDDR3. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of $V_{IH(DC)}$ (which directly affects the conformance limit) is set according to the *JEDEC specification* based on the selected Data Rate, Test Type, and AC Level. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of $V_{IH(DC)}$.

Modes Supported

- LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 29 Differential AC and DC Input Levels

Symbol	Parameter	Value		Units
		Min	Max	
$V_{IHdiff(DC)}$	Differential input high	2 x ($V_{IH(DC)}$ - V_{REF})	Note 3[a]	V

a: Refers to Note 3 in Table 27 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Test References

- See *Table 38 in Section 7 of the LPDDR3 and SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Precondition the oscilloscope.
2 Trigger on a rising edge of the clock signal under test.
3 Find all valid Clock positive pulses in the entire waveform. A valid Clock positive pulse starts at the 0V crossing on a valid Clock rising edge and ends at the 0V crossing on the following valid Clock falling edge.
4 For the first valid Clock positive pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform the VTOP measurement. Take the VTOP measurement result as the $V_{IHdiff(DC)}$ value.
5 Continue the previous step with another nine valid positive pulses that were found in the waveform.
6 Determine the worst result from the set of $V_{IHdiff(DC)}$ measured.

Expected/Observable Results

- The worst measured $V_{IHdiff(DC)}$ must be within the specification limit.

VILdiff.CK(DC)

Test Overview

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{ILdiff(DC)}$ value as specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance limit) is set to 0.6V for LPDDR3. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of $V_{IL(DC)}$ (which directly affects the conformance limit) is set according to the *JEDEC specification* based on the selected Data Rate, Test Type, and AC Level. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of $V_{IL(DC)}$.

Modes Supported

- LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 30 Differential AC and DC Input Levels

Symbol	Parameter	Value		Units
		Min	Max	
$V_{ILdiff(DC)}$	Differential input low	Note 3[a]	2 x ($V_{IL(DC)}$ - V_{REF})	V

a: Refers to Note 3 in Table 25 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Test References

- See *Table 38 in Section 7 of the LPDDR3 and SDRAM in the JEDEC Standard JESD209-3, December 2011*.

Measurement Algorithm

1 Precondition the oscilloscope.
2 Trigger on a rising edge of the clock signal under test.
3 Find all valid Clock negative pulses in the entire waveform. A valid Clock negative pulse starts at the 0V crossing on a valid Clock falling edge and ends at the 0V crossing on the following valid Clock rising edge.
4 For the first valid Clock negative pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform the VBASE measurement. Take the VBASE measurement result as the $V_{ILdiff(DC)}$ value.
5 Continue the previous step with another nine valid negative pulses that were found in the entire waveform.
6 Determine the worst result from the set of $V_{ILdiff(DC)}$ measured.

Expected/Observable Results

- The worst measured $V_{ILdiff(DC)}$ must be within the specification limit.

VIHdiff.CK

Test Overview

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window must be within the conformance limit of the V_{IHdiff} value as specified in the JEDEC specification.

Modes Supported

- DDR3 and DDR3L

Signal(s) cycle of Interest

- Clock Signals

Signals of Interest

- Read or Write

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 31 Differential AC and DC Input Levels

Symbol	Parameter	DDR3-800/1066/1333/1600		Units	Notes
		Min	Max		
$V_{IHdiff(AC)}$	Differential input high AC for clock	+0.200	Note 3[b]	V	1[a]

a: Refers to Note 3 in Table 25 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Test References

- See *Table 25 in Section 8.3 of the DDR3 and SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010.*

Measurement Algorithm

1. Precondition the oscilloscope.
2. Trigger on a rising edge of the clock signal under test.
3. Find all valid Clock positive pulses in the entire waveform. A valid Clock positive pulse starts at the 0V crossing on a valid Clock rising edge and ends at the 0V crossing on the following valid Clock falling edge.
4. For the first valid Clock positive pulse, zoom in on the pulse so that it appears on the oscilloscope’s display and perform the VTOP measurement. Take the VTOP measurement result as the V_{IHdiff} value.
5. Continue the previous step with another nine valid positive pulses found in the waveform.
6. Determine the worst result from the set of V_{IHdiff} measured.

Expected/Observable Results

- The worst measured V_{IHdiff} must be within the specification limit.

VILdiff.CK

Test Overview

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window must be within the conformance limit of the V_{ILdiff} value as specified in the JEDEC specification.

Modes Supported

- DDR3 and DDR3L

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 32 Differential AC and DC Input Levels

Symbol	Parameter	DDR3-800/1066/1333/1600		Units	Notes
		Min	Max		
$V_{ILdiff(AC)}$	Differential input low AC for clock	Note 3[b]	-0.200	V	1[a]

a: Refers to Note 1 in Table 36 of the *JEDEC Standard JESD209-3*. Used to define a differential signal slew rate. For CK_t - CK_c, use $V_{IH}/V_{IL(dc)}$ of CA and V_{REFCA}; for DQS_t - DQS_c, use $V_{IH}/V_{IL(dc)}$ of DQs and V_{REFDQ}; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.

b: Refers to Note 3 in Table 36 of the *JEDEC Standard JESD209-3*. These values are not defined, however.the single-ended signals CK_t, CK_c, DQS_t and DQS_c need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.5 “Overshoot and Undershoot Specifications” on page 92 of the specification document.

Test References

- See *Table 25 in Section 8.3 of the DDR3 and SDRAM Specification in the JEDEC Standard JESD209-3, July 2010.*

Measurement Algorithm

1 Precondition the oscilloscope.

2 Trigger on a rising edge of the clock signal under test.

3 Find all valid Clock negative pulses in the entire waveform. A valid Clock negative pulse starts at the 0V crossing on a valid Clock falling edge and ends at the 0V crossing on the following valid Clock rising edge.

4 For the first valid Clock negative pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform the VBASE measurement. Take the VBASE measurement result as the V_{ILdiff} value.

5 Continue the previous step with another nine valid negative pulses found in the entire waveform.

6 Determine the worst result from the set of V_{ILdiff} measured.

Expected/Observable Results

- The worst measured V_{ILdiff} must be within the specification limit.

Timing Tests at AC Level

tDVAC(Clock)

Test Overview

The purpose of this test is to verify that the time of the clock signal above $V_{IHdiff(AC)}$ and below $V_{ILdiff(AC)}$ must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Signal

Signals required to perform the test on the oscilloscope

- Clock Signal (CK)

Test References

- See *Figure 91 in Section 8 of the DDR3 and SDRAM Specification in the JEDEC Standard JESD79-3F, July 2012*.

Measurement Algorithm

1. Precondition the oscilloscope.
2. Trigger on the rising edge of the clock signal under test.
3. Find all crossings on the rising/falling edge of the signal under test that crosses $V_{ILdiff(AC)}$.
4. Find all crossings on the rising/falling edge of the signal under test that crosses $V_{IHdiff(AC)}$.
5. tVAC(Clock) is the time starting from a rising $V_{IHdiff(AC)}$ cross point and ending at the following falling $V_{IHdiff(AC)}$ cross point.
6. tVVAC(Clock) is the time starting from a falling $V_{ILdiff(AC)}$ cross point and ending at the following rising $V_{ILdiff(AC)}$ cross point.
7. Collect all tVAC(Clock).
8. Determine the worst result from the set of tVAC(Clock) measured.
9. Report the value of the worst tDVAC(Clock). No compliance limit check is performed on this test.

Expected/Observable Results

- The worst measured tVAC(Clock) value must be within the specification limit.

Timing Tests for Rising Edge Measurement

tjit(CC) Rising Edge Measurement

Test Overview

This test is applicable to the Rising Edge Measurement. The purpose of this test is to measure the difference in the clock period between two consecutive clock cycles. The tJIT(cc) Rising Edge Measurement measures the clock period from the rising edge of a clock cycle to the next rising edge.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 33 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
Cycle-to-Cycle Period Jitter	tJIT(cc)	200		180		160		ps

Parameter	Symbol	DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	
Cycle-to-Cycle Period Jitter	tJIT(cc)	120		100		ps

Table 34 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
Maximum Clock Jitter Between Two Consecutive Clock Cycles (with allowed jitter)	tJIT(cc), allowed	MAX	160	140	ps

Test References

- See *Table 68 and 69 in Section 13 of the DDR3 and SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Table 64 in Section 11 of the LPDDR3 and SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

Example input test signal
Frequency: 1 KHz, Number of cycles acquired: 202.

1 Measure the difference between every adjacent pair of periods.
2 Generate 201 measurement results.
3 Check the results for the smallest and largest values (worst case values).
4 Compare the test results against the compliance test limits.

Expected/Observable Results

- The tjit(CC) measurement value must be within the conformance limits as specified in the JEDEC specification.

tCK(avg) Rising Edge Measurement

Test Overview

This test is applicable to the Rising Edge Measurement. tCK(avg) is average clock period within 200 consecutive cycle window. The tCK(avg) Rising Edge Measurement measures the period from the rising edge of a cycle to the next rising edge within the waveform window.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 35 DDR3-800 Speed Bins and Operating Conditions

Speed Bin			DDR3-800D		DDR3-800E		Units
CL - nRCD - nRP			5-5-5		6-6-6		
Parameter		Symbol	Min	Max	Min	Max	
CL = 6	CWL = 5	tCK(avg)	2.5	3.3	2.5	3.3	ns

Table 36 DDR3-1066 Speed Bins and Operating Conditions

Speed Bin			DDR3-1066E		DDR3-1066F		DDR3-1066G		Units
CL - nRCD - nRP			6-6-6		7-7-7		8-8-8		
Parameter		Symbol	Min	Max	Min	Max	Min	Max	
CL = 8	CWL = 6	tCK(avg)	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns

Table 37 DDR3-1333 Speed Bins and Operating Conditions

Speed Bin			DDR3-1333F (optional)		DDR3-1333G		DDR3-1333H		DDR3-1333J (optional)		Units
CL - nRCD - nRP			7-7-7		8-8-8		9-9-9		10-10-10		
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
CL = 10	CWL = 7	tCK(avg)	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	ns

Table 38 DDR3-1600 Speed Bins and Operating Conditions

Speed Bin			DDR3-1600G (optional)		DDR3-1600H		DDR3-1600J		DDR3-1600K (optional)		Units
CL - nRCD - nRP			8-8-8		9-9-9		10-10-10		11-11-11		
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
CL = 11	CWL = 8	tCK(avg)	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	ns

Table 39 DDR3-1866 Speed Bins and Operating Conditions

Speed Bin			DDR3-1333F (optional)		DDR3-1333G		DDR3-1333H		DDR3-1333J (optional)		Units
CL - nRCD - nRP			10-10-10		11-11-11		12-12-12		13-13-13		
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
CL = 13	CWL = 9	tCK(avg)	1.07	< 1.25	1.07	< 1.25	1.07	< 1.25	1.07	< 1.25	ns

Table 40 DDR3-2133 Speed Bins and Operating Conditions

Speed Bin			DDR3-1600G (optional)		DDR3-1600H		DDR3-1600J		DDR3-1600K (optional)		Units
CL - nRCD - nRP			11-11-11		12-12-12		13-13-13		14-14-14		
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
CL =14	CWL = 10	tCK(avg)	0.938	< 1.07	0.938	< 1.07	0.938	< 1.07	0.938	< 1.07	ns

Table 41 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
Average Clock Period	tCK(avg)	MIN	1.5	1.25	ns
		MAX	100		

Test References

- See *Tables 62 to 67 in Section 12 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010* and
- See *Table 63 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

Example input test signal:
Frequency: 1 KHz, Number of cycles acquired: 202.

1 This measurement measures a sliding “window” of 200 cycles.
2 First, calculate the average period value for periods 1-200.
3 Calculate the average period value for periods 2-201.
4 Calculate the average period value for periods 3-202 (by now, 3 measurement results are generated).
5 Check the results for the smallest and largest values (worst case values).
6 Compare the test results against the compliance test limits.

Expected/Observable Results

- The tCK(avg) measurement value must be within the conformance limits as specified in the JEDEC Specification.

tjit(per) Rising Edge Measurement

Test Overview

This test is applicable to the Rising Edge Measurement. The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signals of Interest

- Clock Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 42 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Unit
		Min	Max	Min	Max	Min	Max	
Clock Period Jitter	tJIT(per)	-100	100	-90	90	-80	80	ps

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Unit
		Min	Max	Min	Max	Min	Max	
Clock Period Jitter	tJIT(per)	-70	70	-60	60	-50	50	ps

Table 43 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
Clock Period Jitter (with supported jitter)	tJIT(per), allowed	MIN	-80	-70	ps
		MAX	80	70	

Test References

- See T*able 68 and 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010* and
- See *Table 63 in Section 11 of the DDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

Example input test signal:
Frequency: 1 KHz, Number of cycles acquired: 202.

1 This measurement measures the difference between every period inside a 200 cycle window with the average of the whole window.
2 First, calculate the average for periods 1-200.
3 Measure the difference between period #1 and the average. Save the result as a measurement result.
4 Measure the difference between period #2 and the average. Save the answer.
5 Continue this same procedure until period #200 is compared to the average (200 measurements are generated).
6 Slide the window by one and measure the average of 2-201.
7 Compare period #2 with the new average. Continue the comparison for period #3, #4, .. #200, #201 (200 more measurements are generated, 400 total now).
8 Next, slide the window by one and measure the average of periods 3-202.
9 Compare period #3 with the new average. Continue the comparison for period #4, #5, #201, #202 (200 more measurements so now the total is 600 measurements).
10 Check these 600 measurements for the smallest and largest values (worst case values).
11 Compare test result to compliance test limit.

Expected/Observable Results

- The tJIT(per) measurement value must be within the conformance limits as specified in the JEDEC specification.

tERR(nper) Rising Edge Measurement

Test Overview

This Cumulative Error (across “n” cycles) test is applicable to the Rising Edge Measurement. The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock. Supported measurements include multiple cycle windows with values of “n” (for “n” cycles) where n > 5 but less than 50.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 44 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Cumulative error across 2 cycles	tERR(2per)	-147	147	-132	132	-118	118	-103	103	ps
Cumulative error across 3 cycles	tERR(3per)	-175	175	-157	157	-140	140	-122	122	ps
Cumulative error across 4 cycles	tERR(4per)	-194	194	-175	175	-155	155	-136	136	ps
Cumulative error across 5 cycles	tERR(5per)	-209	209	-188	188	-168	168	-147	147	ps
Cumulative error across 6 cycles	tERR(6per)	-222	222	-200	200	-177	177	-155	155	ps
Cumulative error across 7 cycles	tERR(7per)	-232	232	-209	209	-186	186	-163	163	ps
Cumulative error across 8 cycles	tERR(8per)	-241	241	-217	217	-193	193	-169	169	ps
Cumulative error across 9 cycles	tERR(9per)	-249	249	-224	224	-200	200	-175	175	ps
Cumulative error across 10 cycles	tERR(10per)	-257	257	-231	231	-205	205	-180	180	ps
Cumulative error across 11 cycles	tERR(11per)	-263	263	-237	237	-210	210	-184	184	ps
Cumulative error across 12 cycles	tERR(12per)	-269	269	-242	242	-215	215	-188	188	ps
Cumulative error across n= 13, 14, 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 + 0.68ln(n))*tJIT(per)max								ps

Table 45 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	
Cumulative error across 2 cycles	tERR(2per)	-88	88	-74	74	ps
Cumulative error across 3 cycles	tERR(3per)	-105	105	-87	87	ps
Cumulative error across 4 cycles	tERR(4per)	-117	117	-97	97	ps
Cumulative error across 5 cycles	tERR(5per)	-126	126	-105	105	ps
Cumulative error across 6 cycles	tERR(6per)	-133	133	-111	111	ps
Cumulative error across 7 cycles	tERR(7per)	-139	139	-116	116	ps
Cumulative error across 8 cycles	tERR(8per)	-145	145	-121	121	ps
Cumulative error across 9 cycles	tERR(9per)	-150	150	-125	125	ps
Cumulative error across 10 cycles	tERR(10per)	-154	154	-128	128	ps
Cumulative error across 11 cycles	tERR(11per)	-158	158	-132	132	ps
Cumulative error across 12 cycles	tERR(12per)	-161	161	-134	134	ps
Cumulative error across n= 13, 14, 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 + 0.68ln(n))*tJIT(per)max				ps

Table 46 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Units
			1333	1600	
Cumulative error across 2 cycles	tERR(2per), allowed	MIN	-118	-103	ps
		MAX	118	103	
Cumulative error across 3 cycles	tERR(3per), allowed	MIN	-140	-122	ps
		MAX	140	122	
Cumulative error across 4 cycles	tERR(4per), allowed	MIN	-155	-136	ps
		MAX	155	136	
Cumulative error across 5 cycles	tERR(5per), allowed	MIN	-168	-147	ps
		MAX	168	147	
Cumulative error across 6 cycles	tERR(6per), allowed	MIN	-177	-155	ps
		MAX	177	155	
Cumulative error across 7 cycles	tERR(7per), allowed	MIN	-186	-163	ps
		MAX	186	163	
Cumulative error across 8 cycles	tERR(8per), allowed	MIN	-193	-169	ps
		MAX	193	169	

Parameter	Symbol	Min/Max	Data Rate		Units
			1333	1600	
Cumulative error across 9 cycles	tERR(9per), allowed	MIN	-200	-175	ps
		MAX	200	175	
Cumulative error across 10 cycles	tERR(10per), allowed	MIN	-205	-180	ps
		MAX	205	180	
Cumulative error across 11 cycles	tERR(11per), allowed	MIN	-210	-184	ps
		MAX	210	184	
Cumulative error across 12 cycles	tERR(12per), allowed	MIN	-215	-188	ps
		MAX	215	188	
Cumulative error across n = 13, 14, 15... 19, 20 cycles	tERR(nper), allowed	MIN	tERR(nper), *allowed* MIN = (1 + 0.68ln(n))*tJIT(per), *allowed* MIN		ps
		MAX	tERR(nper), *allowed* MAX = (1 + 0.68ln(n))*tJIT(per), *allowed* MAX		

Test References

- See *Table 68 and 69 in Section 13 of the DDR# and SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011*.

Measurement Algorithm

Example input test signal:
Frequency: 1 kHz, Number of cycles acquired: 202.

1 tERR(2per) is similar to tJIT(per), except it makes a small 2-cycle window inside the big 200 cycle window and compares the average of the small window with the average of the big window.

2 First, calculate the average for periods 1-200.

3 Calculate the average of periods 1-2.

4 Measure the difference between these two averages and save this as a measurement result.

5 Calculate the average of period 2-3 and measure the difference between this average and the big window average.

6 Continue this same procedure until it compares the average of periods 199-200 to the big window average (so far, 199 measurement result generated).

7 Next, slide the big window by one and repeat, starting by comparing the average of periods 2-3 with the new big window average until it finishes by comparing periods 200-201 with the big window (by now 199 more measurements have been taken for a total of 398 measurements so far).

8 Slide the big window by one again and repeat the same procedure (making a total of 597 measurement values).

9 Check the 597 results for the smallest and largest values (worst case values).

10 Compare the test result to the compliance limit.

11 tERR(3per) is the same as tERR(2per) except the small window size is 3 periods wide. tERR(4per) uses small window size of 4 periods, and tERR(5per) uses 5 periods.

12 tERR(6-10per) executes tERR(6per), tERR(7per), tERR(8per), tERR(9per) and tERR(10per), combines all the measurement results together into one big pool and checks for the smallest and largest value.

13 tERR(11-50per) does the same for tERR(11per) through tERR(50per).

Expected/Observable Results

- The tERR measurement value must be within the conformance limits as specified in the JEDEC Specification.

tCK(abs) Rising Edge Measurement

Test Overview

tCK(abs) is absolute clock period within 200 consecutive cycle window. The purpose of this test is to measures the period from the rising edge of a cycle to the next rising edge within the waveform window.

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Read or Write cycle

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 47 AC Timing

Symbol	Parameter	Min/Max	Data Rate		Units
			1333	1600	
$t_{CK(abs)}$	Absolute clock period	MIN	$t_{CK(avg)}MIN + t_{JIT(avg)}MIN$	Note 3[a]	ns

a: Refers to Note 3 in Table 27 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Test References

- See *Table 64 in Section 11 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3, December 2011*.

Measurement Algorithm

Example input test signal:
Frequency: 1 kHz, Number of cycles acquired: 202.

1. First, calculate the maximum period value for periods 1-202.
2. Calculate the minimum period value for periods 1-202.
3. For above two result, check for the worst cases.
4. Compare the test result to the compliance limit.

Expected/Observable Results

- The tCK(abs) measurement value must be within the conformance limits as specified in the JEDEC specification.

Timing Tests for Pulse Measurement

tCH(avg) Average High Measurement

Test Overview

The purpose of this test is to measure the average duty cycle of all the positive pulse widths within a window of 200 consecutive cycles.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Signal(s) of Interest

- Clock Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 48 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
Average High Pulse Width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	
Average High Pulse Width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)

Table 49 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
Average High Pulse Width	tCH(avg)	MIN	0.45		tCK(avg)
		MAX	0.55		

Test References

- See *Table 68 and 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010* and
- See *Table 64 in Section 11 of the DDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

Example input test signal:
Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding “window” of 200 cycles.
2. Measure the width of the high pulses 1-200 and determine the average value for this window. (generated 1 measurement result).
3. Measure the width of the high pulses 2-201 and determine the average value for this window. (by now, generate a total of 2 measurement results).
4. Measure the width of the high pulses 3-202 and determine the average value for this window. (by now, generate a total of 3 measurement results).
5. Check the total 3 results for the smallest and largest values (worst case values).
6. Compare the test results against the compliance test limits.

Expected/Observable Results

- The tCH measurement value must be within the conformance limits as specified in the JEDEC Specification.

tCL(avg) Average Low Measurement

Test Overview

The purpose of this test is to measure the average duty cycle of all the negative pulse widths within a window of 200 consecutive cycles.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 50 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
Average Low Pulse Width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCL(avg)

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	
Average Low Pulse Width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCL(avg)

Table 51 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
Average Low Pulse Width	tCL(avg)	MIN	0.45		tCK(avg)
		MAX	0.55		

Test References

- See *Table 68 and 69 in Section 13 of the DDR3 and SDRAM Specification in the JEDEC Standard JESD79-3E July 2010* and
- See *Table 64 in Section 11 of the DDR3 and SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

Example input test signal:
Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding “window” of 200 cycles.
2. Measure the width of the low pulses 1-200 and determine the average value for this window. (generated 1 measurement result).
3. Measure the width of the low pulses 2-201 and determine the average value for this window. (by now, generate a total of 2 measurement results).
4. Measure the width of the low pulses 3-202 and determine the average value for this window. (by now, generate a total of 3 measurement results).
5. Check the total 3 results for the smallest and largest values (worst case values).
6. Compare results against the compliance test limits.

Expected/Observable Results

- The tCL measurement value must be within the conformance limits as specified in the JEDEC Specification.

tJIT(duty-high/low) Jitter Average High/Low Measurements

Test Overview

The Half Period Jitter tJIT(duty) can be divided into tJIT(CH) Jitter Average High and tJIT(LH) Jitter Average Low. The tJIT(CH) Jitter Average High Measurement measures between a positive pulse width of a cycle in the waveform, and the average positive pulse width of all cycles in a 200 consecutive cycle window.

The tJIT(LH) Jitter Average Low Measurement measures between a negative pulse width of a cycle in the waveform and the average negative pulse width of all cycles in a 200 consecutive cycle window.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 52 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
Duty Cycle Jitter	tJIT(duty)	-	-	-	-	-	-	ps

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	
Duty Cycle Jitter	tJIT(duty)	-	-	-	-	-	-	ps

NOTE Due to the unavailability of limit values for this test parameter in the specification document, the limit for this test is left open by setting the minimum and maximum to very large values (min = -99E36, max = 99E36).

Table 53 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
Duty Cycle Jitter (with supported jitter)	tJIT(duty), allowed	MIN	min((tCH(abs), min - tCH(avg), min), (tCL(abs), min - tCL(avg), min)) * tCK(avg)		ps
		MAX	max((tCH(abs), max - tCH(avg), max), (tCL(abs), max - tCL(avg), max)) * tCK(avg)		

Test References

- See *Table 68 and 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

Example input test signal:
Frequency: 1 KHz, Number of cycles acquired: 202.

tJIT(CH):

1 This measurement measures the difference between every high pulse width inside a 200 cycle window with the average of the whole window.
2 First calculate the average for high pulse width 1-200.
3 Measure the difference between high pulse width #1 and the average. Save the answer as a measurement result.
4 Measure the difference between high pulse width #2 and the average. Save the answer as a measurement result.
5 Continue this same procedure until high pulse #200 is compared to the average (200 measurements).
6 Slide the window by one and measure the average of 2-201.
7 Compare high pulse #2 with the new average. Continue the comparisons for high pulse width #3, #4, #200, #201 (200 more measurements so 400 total so far).
8 Slide the window by one and measure the average of 3-202.
9 Compare high pulse width #3 with the new average. Continue the comparisons for high pulse width #4, #5, ... #201, #202 (200 more measurements so 600 total measurements).
10 Check these 600 results for the smallest and largest values (worst case values).
11 Compare the test results against the compliance test limits.

tJIT(LH):

12 This measurement is similar to tJIT(CH) above except, instead of using high pulse widths, it uses low pulse widths for testing comparison.

Expected/Observable Results

- The tJIT(duty) measurement value must be within the conformance limits as specified in the JEDEC Specification.

tCH(abs) Absolute clock HIGH pulse width

Test Overview

The purpose of this test is to measure the absolute duty cycle of all the positive pulse widths within a window of 200 consecutive cycles.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Clock Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 54 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333			
		Min	Max	Min	Max	Min	Max	Units	Notes
Absolute Clock High Pulse Width	tCH(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	25

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133			
		Min	Max	Min	Max	Min	Max	Units	Notes
Absolute Clock High Pulse Width	tCH(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	25

Table 55 AC Timing

Parameter	Symbol	Min/Max	Data Rate				Unit
			1333	1600	1866	2133	
Absolute Clock High Pulse Width	tCH(abs)	MIN	0.43				tCK(avg)
		MAX	0.57				

Test References

- See *Table 68 and 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3F July 2012* and
- See *Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3B, August 2013.*

Measurement Algorithm

Example input test signal:
Frequency: 1 KHz, Number of cycles acquired: 202.

1 Find the average period, tCK(avg) for cycle 1-202.
2 Find the maximum high pulse width, PWMAX(s) for cycle 1-202.
3 Find the minimum high pulse width, PWMIN(s) for cycle 1-202.
4 Calculate PWMAX(tCK)= PWMAX(s)/ tCK(avg).
5 Calculate PWMIN(tCK)= PWMIN(s)/ tCK(avg).
6 Check PWMAX(tCK) and PWMIN(tCK) for the worst cases values.
7 Compare test result to compliance test limit.

Expected/Observable Results

- The absolute tCH measurement value must be within the conformance limits as specified in the JEDEC Specification.

tCL(abs) Absolute clock LOW pulse width

Test Overview

The purpose of this test is to measure the absolute duty cycle of all the negative pulse widths within a window of 200 consecutive cycles.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signals of Interest

- Clock Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 56 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333			
		Min	Max	Min	Max	Min	Max	Units	Notes
Absolute Clock Low Pulse Width	tCL(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	26[a]

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133			
		Min	Max	Min	Max	Min	Max	Units	Notes
Absolute Clock Low Pulse Width	tCL(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	26[a]

a: Refers to Note 26 in Table 68 of the *JEDEC Standard JESD79-3F*. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

Table 57 AC Timing

Parameter	Symbol	Min/Max	Data Rate				Unit
			1333	1600	1866	2133	
Absolute Clock Low Pulse Width	tCL(abs)	MIN	0.43				tCK(avg)
		MAX	0.57				

Test References

- See *Table 68 and 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3F July 2012* and
- See *Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3B, August 2013*.

Measurement Algorithm

Example input test signal:
Frequency: 1 KHz, Number of cycles acquired: 202.

1 Find the average period, tCK(avg) for cycle 1-202.
2 Find the maximum low pulse width, PWMAX(s) for cycle 1-202.
3 Find the minimum low pulse width, PWMIN(s) for cycle 1-202.
4 Calculate PWMAX(tCK)= PWMAX(s)/ tCK(avg).
5 Calculate PWMIN(tCK)= PWMIN(s)/ tCK(avg).
6 Check PWMAX(tCK) and PWMIN(tCK) for the worst cases values.
7 Compare test result to compliance test limit.

Expected/Observable Results

- The absolute tCL measurement value must be within the conformance limits as specified in the JEDEC Specification.

7 Strobe Plus Tests Group

This section provides the Methods of Implementation (MOIs) for Strobe Plus tests for Strobe Signals using a Keysight Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ refer to complement. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Strobe Plus Tests

When performing the Strobe Plus tests for Strobe Signals the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Strobe Plus tests for Strobes may look similar to the following diagram. Refer to the Connection tab in the DDR3 Electrical Performance Compliance application for the exact number of probe connections.

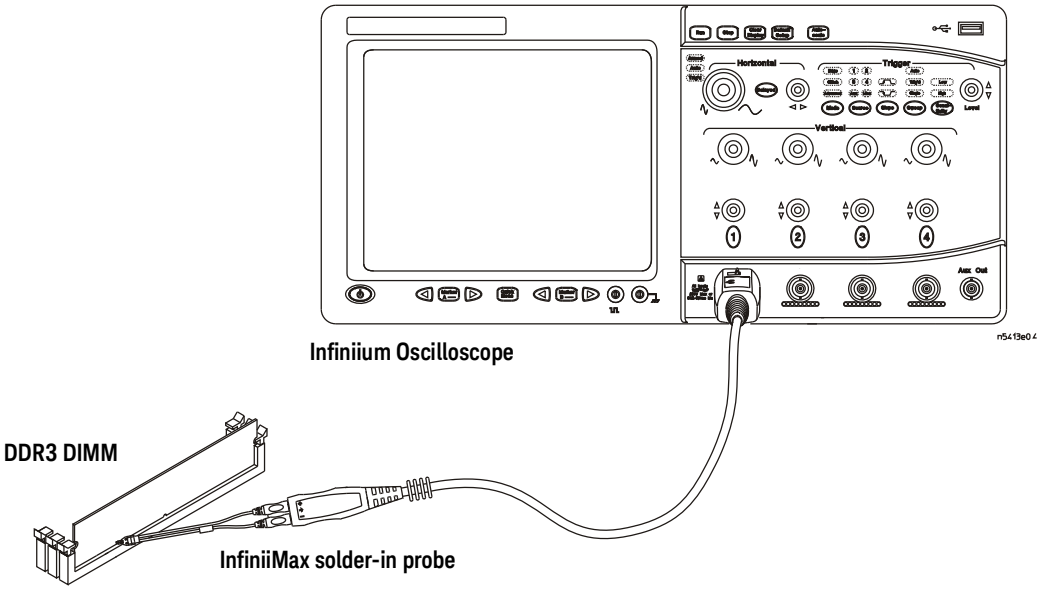


Figure 21 Probing for strobe plus tests

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 21 are just examples).

For more information on the probe amplifiers and differential probe heads, refer to the respective user guide for Probes.

Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the **Set Up** tab.

6 Select the **Test Mode**, **SDRAM Type, Speed Grade**, and **AC Levels** options.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

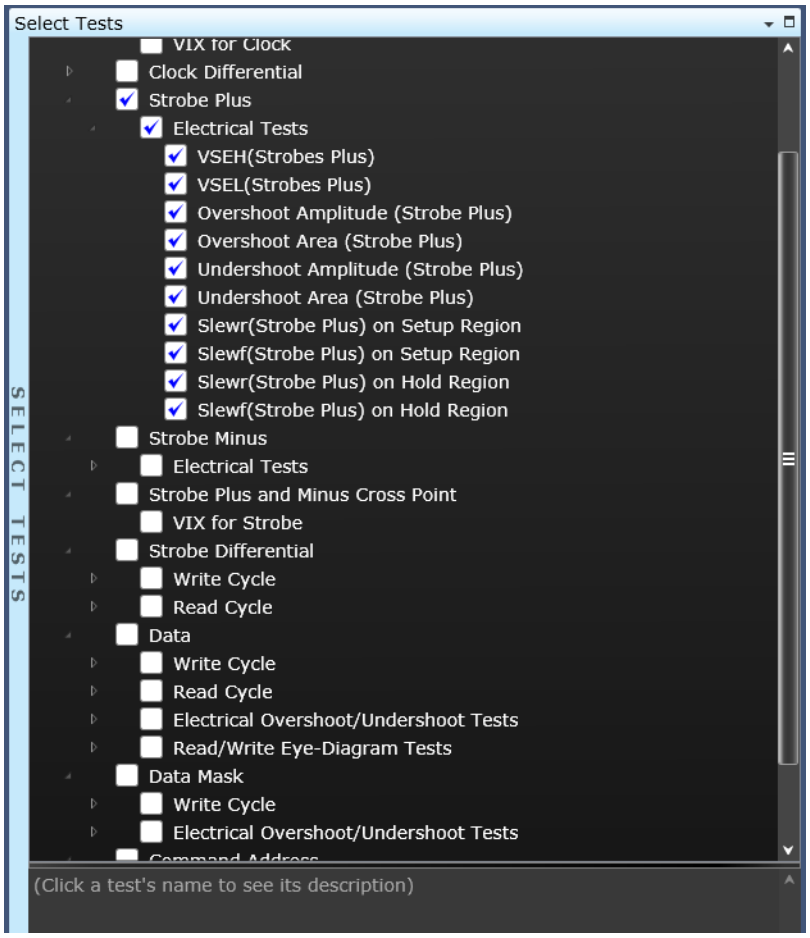


Figure 22 Selecting Strobe Plus Tests

Electrical Tests

VSEH(Strobes Plus)

Test Overview

The purpose of this test is to verify that the maximum voltage of the high pulse must be within the conformance limit of the V_{SEH} value as specified in the JEDEC specification.

The value of V_{DD} (which directly affects the conformance limit) is set to 1.5V for DDR3 and 1.2V for LPDDR3. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DD}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write cycle

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Plus Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQ

Test Definition Notes from the Specification

Table 58 Single-ended Levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL# or DQSU#

Symbol	Parameter	DDR3-800/1066/1333/1600		Units
		Min	Max	
V_{SEH}	Single-ended high level for strobes	$(V_{DD}/2) + 0.175$	Note 3[a]	V

a: Refers to Note 3 in Table 27 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Table 59 Single-ended Levels for CK_t, DQS_t, CK_c, and DQS_c

Symbol	Parameter	Value		Units	Notes
		Min	Max		
$V_{SEH(AC)}$	Single-ended high level for strobes	$(V_{DDQ}/2) + 0.220$	Note 3[c]	V	1[a], 2[b]

a: Refers to Note 1 in Table 39 of the *JEDEC Standard JESD209-3*. For CK_t, CK_c, use $V_{SEH}/V_{SEL(ac)}$ of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use $V_{IH}/V_{IL(ac)}$ of DQs.

b: Refers to Note 2 in Table 39 of the *JEDEC Standard JESD209-3*. $V_{IH(ac)}/V_{IL(ac)}$ for DQs is based on V_{REFDQ}; $V_{SEH(ac)}/V_{SEL(ac)}$ for CA is based on V_{REFCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

c: Refers to Note 3 in Table 39 of the *JEDEC Standard JESD209-3*. These values are not defined, however.the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.5 “Overshoot and Undershoot Specifications” on page 92 of the specification document.

Test References

- See *Table 27 in Section 8.3 of the DDR3 SDRAM Specification, JEDEC Standard JESD79-3E, July 2010* and
- See *Figure 124 and Table 40 in Section 7 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid strobe positive pulses in this burst. A valid strobe positive pulse starts at the V_{REF} crossing on a valid strobe rising edge and ends at the V_{REF} crossing on the following valid strobe falling edge.
4 For the first valid strobe positive pulse, zoom in on the pulse so that it appears on the oscilloscope’s display and measure T_{MAX}.
5 Measure V_{TIME} at the found T_{MAX} to get the maximum voltage of the pulse. Consider V_{TIME} measurement result as the V_{SEH} value.
6 Continue the previous step for the rest of the valid strobe positive pulses that were found in the burst.
7 Determine the worst result from the set of V_{SEH} measured.

Expected / Observable Results

- The worst measured V_{SEH} must be within the specification limit.

VSEL(Strobes Plus)

Test Overview

The purpose of this test is to verify that the minimum voltage of the low pulse must be within the conformance limit of the V_{SEL} value as specified in the JEDEC specification.

The value of V_{DD} (which directly affects the conformance limit) is set to 1.5V for DDR3 and 1.2V for LPDDR3. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DD}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write cycle

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Plus Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQ

Test Definition Notes from the Specification

Table 60 Single-ended Levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL#, or DQSU#

Symbol	Parameter	DDR3-800/1066/1333/1600		Units
		Min	Max	
V_{SEL}	Single-ended low level for strobes	Note 3[a]	$(V_{DD}/2)$ - 0.175	V

a: Refers to Note 3 in Table 27 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Table 61 Single-ended Levels for CK_t, DQS_t, CK_c, DQS_c

Symbol	Parameter	Value		Units	Notes
		Min	Max		
$V_{SEL(AC)}$	Single-ended low level for strobes	Note 3[c]	$(V_{DDQ}/2)$ - 0.220	V	1[a], 2[b]

a: Refers to Note 1 in Table 39 of the *JEDEC Standard JESD209-3*. For CK_t, CK_c, use $V_{SEH}/V_{SEL(ac)}$ of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use $V_{IH}/V_{IL(ac)}$ of DQs.

b: Refers to Note 2 in Table 39 of the *JEDEC Standard JESD209-3*. $V_{IH(ac)}/V_{IL(ac)}$ for DQs is based on V_{REFDQ}; $V_{SEH(ac)}/V_{SEL(ac)}$ for CA is based on V_{REFCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

c: Refers to Note 3 in Table 39 of the *JEDEC Standard JESD209-3*. These values are not defined, however.the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.5 “Overshoot and Undershoot Specifications” on page 92 of the specification document.

Test References

- See *Table 27 in Section 8.3 of the DDR3 SDRAM Specification*, *JEDEC Standard JESD79-3E, July 2010* and
- See *Figure 124 and Table 40 in Section 7 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid strobe negative pulses in this burst. A valid strobe negative pulse starts at the V_{REF} crossing on a valid strobe falling edge and ends at the V_{REF} crossing on the following valid strobe rising edge.
4 For the first valid strobe negative pulse, zoom in on the pulse so that it appears on the oscilloscope’s display and measure T_{MIN}.
5 Measure V_{TIME} at the found T_{MIN} to get the minimum voltage of the pulse. Consider the V_{TIME} measurement result as the V_{SEL} value.
6 Continue the previous step for the rest of the valid strobe negative pulses that were found in the burst.
7 Determine the worst result from the set of V_{SEL} measured.

Expected/Observable Results

- The worst measured V_{SEL} must be within the specification limit.

Overshoot Amplitude / Area (Strobes Plus)

Test Overview

The Overshoot test can be divided into two sub-tests: Overshoot amplitude and Overshoot area.

The purpose of this test is to verify that the overshoot value of the test signal found from all regions of the acquired waveform is lower than or equal to the conformance limit of the maximum peak amplitude allowed for overshoot as specified in the JEDEC specification.

When there is an overshoot, the area is calculated based on the overshoot width and overshoot amplitude. The Overshoot area should be lower than or equal to the conformance limit of the maximum overshoot area allowed as specified in the JEDEC specification.

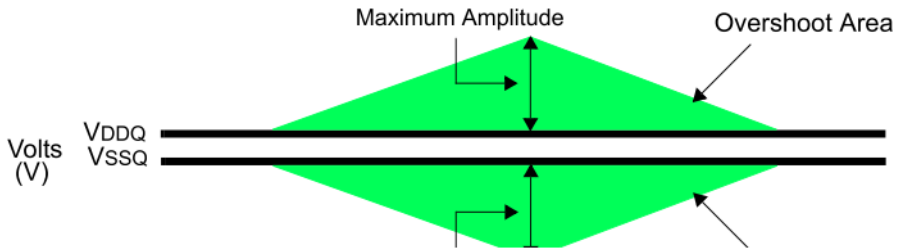


Figure 23 Strobe Overshoot

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write cycle

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Plus Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 62 AC Overshoot Specification for Strobe and Mask Pins

Parameter	Specification					
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133
Maximum peak amplitude allowed for overshoot area	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V
Maximum overshoot area above V_{DDQ}	0.25 V/ns	0.19 V/ns	0.15 V/ns	0.13 V/ns	0.11 V/ns	0.10 V/ns

Table 63 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for overshoot area	Max	0.35		V
Maximum area above V_{DD}	Max	0.12	0.10	V-ns

Test References

- See *Figure 100 and Table 37 in Section 9 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Figure 126 and Table 49 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Set the number of sampling points to 2M samples.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Obtain the overshoot region. Overshoot region starts at the rising VDDQ crossing and ends at the falling VDDQ crossing.

4 Within Overshoot region #1, perform the following steps:

i Evaluate Overshoot Amplitude by performing the following steps:
a. Use TMAX and VMAX to get time stamp of maximum voltage on overshoot region of the acquired waveform.
b. Calculate: Overshoot Amplitude = VMAX – VDDQ.

ii Evaluate Area below VDDQ = (Overshoot Region End – Overshoot Region Start) * VDDQ.

iii Evaluate Total Area above 0 volt by using Trapezoidal Method Area Calculation as shown in following figure:

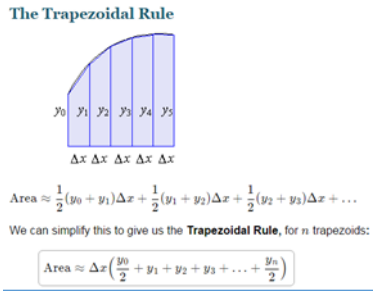


Figure 24 Trapezoidal Rule

iv Calculate area above VDDQ = Total area above 0 volt - area below VDDQ.

v Store calculated result below for later worst case finding process;

- Overshoot Amplitude
- Area above VDDQ

5 Repeat the previous step for the rest Overshoot Region found in acquired waveform.

6 Find the worst result below from stored result.

7 Compare test result to the compliance test limit.

- Overshoot Amplitude
- Area above VDDQ

Expected/Observable Results

- The measured maximum voltage value must be less than or equal to the maximum overshoot value.
- The calculated Overshoot area value must be less than or equal to the maximum Overshoot area allowed.

Undershoot Amplitude / Area (Strobes Plus)

Test Overview

The Undershoot Test can be divided into two sub-tests: Undershoot amplitude and Undershoot area.

The purpose of this test is to verify that the undershoot value of the test signal found from all regions of the acquired waveform is less than or equal to the conformance limit of the maximum peak amplitude allowed for undershoot as specified in the *JEDEC specification*.

When there is an undershoot, the area is calculated based on the undershoot width. The Undershoot area should be less than or equal to the conformance limit of the maximum undershoot area allowed as specified in the *JEDEC specification*.

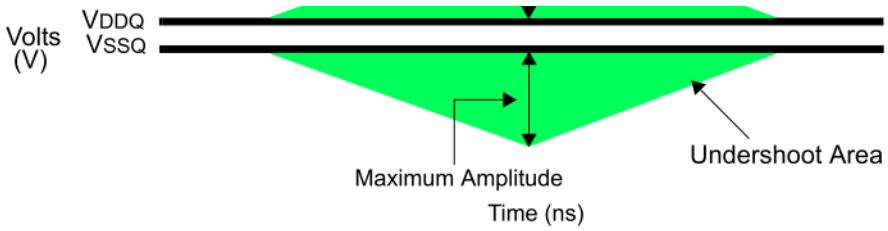


Figure 25 Strobe Undershoot

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write cycle

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Plus Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 64 AC Undershoot Specification for Clock, Data, Strobe and Mask Pins

Parameter	Specification					
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133
Maximum peak amplitude allowed for undershoot area	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V
Maximum undershoot area below V_{SSQ}	0.25 V/ns	0.19 V/ns	0.15 V/ns	0.13 V/ns	0.11 V/ns	0.10 V/ns

Table 65 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for undershoot area	Max	0.35		V
Maximum area below V_{SS}	Max	0.12	0.10	V-ns

Test References

- See *Figure 100 and Table 37 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Figure 126 and Table 49 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Set the number of sampling points to 2M samples.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Obtain the undershoot region. Undershoot Region starts at falling 0 volt crossing and end at rising 0 volt crossing.

4 Within Undershoot region #1;

   i Evaluate Undershoot Amplitude by performing the following steps:
   a. Use TMIN and VMIN to get time stamp of maximum voltage on undershoot region of the acquired waveform.
   b. Calculate: Undershoot Amplitude = 0- VMIN

   ii Evaluate total area below 0 volt by using Trapezoidal Method Area Calculation (refer to Figure 24)

   iii Store Calculated result below for later worst case finding process:

   - Undershoot Amplitude
   - Total area below 0 volt

5 Repeat the previous step for the rest Undershoot Region found in acquired waveform.

6 Find the worst result below from stored result.

7 Compare test result to the compliance test limit.

   - Undershoot Amplitude
   - Total area below 0 volt

Expected/Observable Results

- The measured minimum voltage value for the test signal must be less than or equal to the maximum undershoot value.
- The calculated undershoot area value must be less than or equal to the maximum undershoot area allowed.

SlewR on Setup Region

Test Overview

The purpose of this test is to calculate the rising slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Modes Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Plus Signals (supported by Data Signals)

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin.

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Test Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)

2 Take the first valid WRITE burst found.

3 Find all valid rising edges in the said burst. A valid rising edge starts at VIL (ac) crossing and end at following VIH (ac) crossing.

4 For all valid rising edges, find the transition time, delta TR which is time starts at VREF crossing and end at following VIH (ac) crossing. Then calculate Rising Slew.

$$\text{Rising Slew} = \frac{V_{IH(ac)}\ \text{min} - V_{REF}}{\text{delta TR}}$$

5 Determine the worst result from the set of SlewR measured.

Expected/Observable Results

- The calculated Rising Slew value for the test signal shall meet the user defined limit.

SlewF on Setup Region

Test Overview

The purpose of this test is to calculate the falling slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Modes Supported

- DDR3 and DDR3L

Signal cycle of interest:

- WRITE

Require Read/Write separation

- Yes

Signal(s) of Interest:

- Data Strobe Plus Signals(supported by Data Signals)

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)

2 Take the first valid WRITE burst found.

3 Find all valid falling edges in the said burst. A valid falling edge starts at VIH (ac) crossing and end at following VIL (ac) crossing.

4 For all valid falling edges, find the transition time, delta TF which is time starts at VREF crossing and end at following VIL (ac) crossing. Then calculate Falling Slew.

$$\text{Falling Slew} = \frac{V_{REF} - V_{IL(ac)}\ \text{max}}{\text{delta TF}}$$

5 Determine the worst result from the set of SlewF measured.

Expected/Observable Results

- The calculated Falling Slew value for the test signal shall meet the user defined limit.

SlewR on Hold Region

Test Overview

The purpose of this test is to calculate the rising slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Plus Signals (supported by Data Signals)

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)

2 Take the first valid WRITE burst found.

3 Find all valid rising edges in the said burst. A valid rising edge starts at VIL (ac) crossing and end at following VIH (ac) crossing.

4 For all valid rising edges, find the transition time, delta TR which is time starts at VIL(DC) crossing and end at following VREF crossing. Then calculate Rising Slew.

$$Rising\ Slew = \frac{V_{REF} - V_{IL(DC)}}{\text{delta TR}}$$

5 Determine the worst result from the set of SlewR measured.

Expected/Observable Results

- The calculated Rising Slew value for the test signal shall meet the user defined limit.

SlewF on Hold Region

Test Overview

The purpose of this test is to calculate the falling slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Plus Signals (supported by Data Signals)

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)

2 Take the first valid WRITE burst found.

3 Find all valid falling edges in the said burst. A valid falling edge starts at VIH (ac) crossing and end at following VIL (ac) crossing.

4 For all valid falling edges, find the transition time, delta TF which is time starts at VIH(DC) crossing and end at following VREF crossing. Then calculate Falling Slew.

$$Falling\ Slew = \frac{V_{IH(DC)} - V_{REF}}{\text{delta TF}}$$

5 Determine the worst result from the set of SlewF measured.

Expected/Observable Results

- The calculated Falling Slew value for the test signal shall meet the user defined limit.

8 Strobe Minus Tests Group

This section provides the Methods of Implementation (MOIs) for Strobe Minus tests for Strobe Signals using a Keysight Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to complement. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Strobe Minus Tests

When performing the Strobe Minus tests for Strobe Signals, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Strobe Minus tests for Strobes may look similar to the following diagram. Refer to the Connection tab in the DDR3 Electrical Performance Compliance application for the exact number of probe connections.

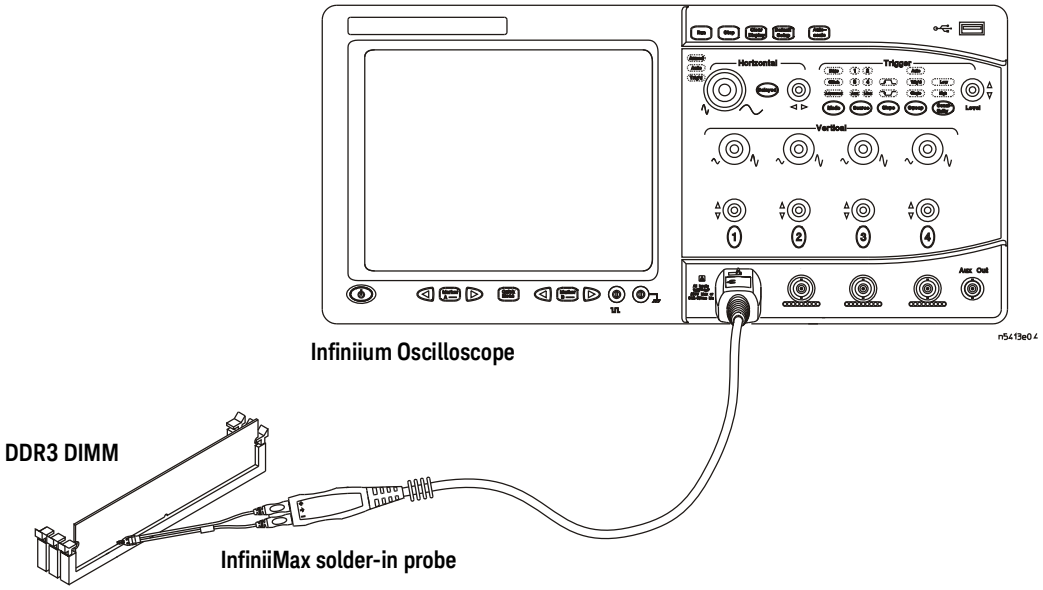


Figure 26 Probing for strobe plus tests

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 26 are just examples).

For more information on the probe amplifiers and differential probe heads, refer to the respective user guide for Probes.

Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the **Set Up** tab.

6 Select the **Test Mode**, **SDRAM Type, Speed Grade**, and **AC Levels** options.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

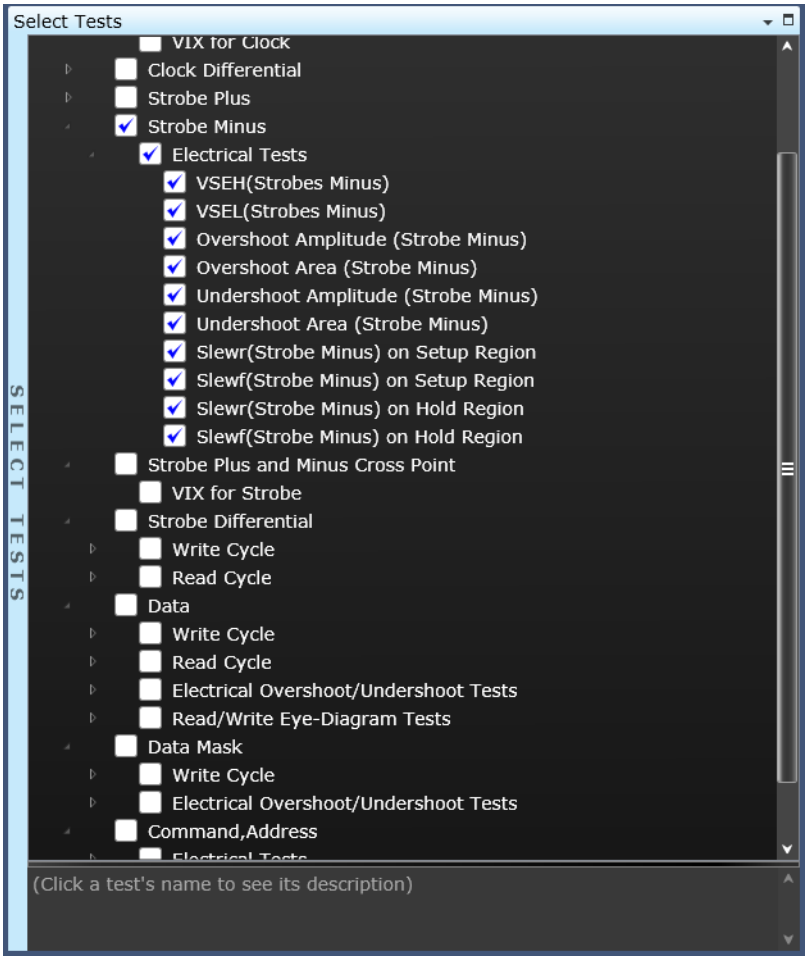


Figure 27 Selecting Strobe Minus Tests

Electrical Tests

VSEH(Strobes Minus)

Test Overview

The purpose of this test is to verify that the maximum voltage of the high pulse must be within the conformance limit of the V_{SEH} value as specified in the JEDEC specification.

The value of V_{DD} (which directly affects the conformance limit) is set to 1.5V for DDR3 and 1.2V for LPDDR3. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DD}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write cycle

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Minus Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQ

Test Definition Notes from the Specification

Table 66 Single-ended Levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL# or DQSU#

Symbol	Parameter	DDR3-800/1066/1333/1600		Units
		Min	Max	
V_{SEH}	Single-ended high level for strobes	$(V_{DD}/2) + 0.175$	Note 3[a]	V

a: Refers to Note 3 in Table 27 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Table 67 Single-ended Levels for CK_t, DQS_t, CK_c, and DQS_c

Symbol	Parameter	Value		Units	Notes
		Min	Max		
$V_{SEH(AC)}$	Single-ended high level for strobes	$(V_{DDQ}/2) + 0.220$	Note 3[c]	V	1[a], 2[b]

a: Refers to Note 1 in Table 39 of the *JEDEC Standard JESD209-3*. For CK_t, CK_c, use $V_{SEH}/V_{SEL(ac)}$ of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use $V_{IH}/V_{IL(ac)}$ of DQs.

b: Refers to Note 2 in Table 39 of the *JEDEC Standard JESD209-3*. $V_{IH(ac)}/V_{IL(ac)}$ for DQs is based on V_{REFDQ}; $V_{SEH(ac)}/V_{SEL(ac)}$ for CA is based on V_{REFCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

c: Refers to Note 3 in Table 39 of the *JEDEC Standard JESD209-3*. These values are not defined, however.the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.5 “Overshoot and Undershoot Specifications” on page 92 of the specification document.

Test References

- See *Table 27 in Section 8.3 of the DDR3 SDRAM Specification, JEDEC Standard JESD79-3E, July 2010* and
- See *Figure 124 and Table 40 in Section 7 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid strobe positive pulses in this burst. A valid strobe positive pulse starts at the V_{REF} crossing on a valid strobe rising edge and ends at the V_{REF} crossing on the following valid strobe falling edge.
4 For the first valid strobe positive pulse, zoom in on the pulse so that it appears on the oscilloscope’s display and measure T_{MAX}.
5 Measure V_{TIME} at the found T_{MAX} to get the maximum voltage of the pulse. Consider V_{TIME} measurement result as the V_{SEH} value.
6 Continue the previous step for the rest of the valid strobe positive pulses that were found in the burst.
7 Determine the worst result from the set of V_{SEH} measured.

Expected / Observable Results

- The worst measured V_{SEH} must be within the specification limit.

VSEL(Strobes Minus)

Test Overview

The purpose of this test is to verify that the minimum voltage of the low pulse must be within the conformance limit of the V_{SEL} value as specified in the JEDEC specification.

The value of V_{DD} (which directly affects the conformance limit) is set to 1.5V for DDR3 and 1.2V for LPDDR3. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DD}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write cycle

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Minus Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQ

Test Definition Notes from the Specification

Table 68 Single-ended Levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL#, or DQSU#

Symbol	Parameter	DDR3-800/1066/1333/1600		Units
		Min	Max	
V_{SEL}	Single-ended low level for strobes	Note 3[a]	$(V_{DD}/2)$ - 0.175	V

a: Refers to Note 3 in Table 27 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Table 69 Single-ended Levels for CK_t, DQS_t, CK_c, DQS_c

Symbol	Parameter	Value		Units	Notes
		Min	Max		
$V_{SEL(AC)}$	Single-ended low level for strobes	Note 3[c]	$(V_{DDQ}/2)$ - 0.220	V	1[a], 2[b]

a: Refers to Note 1 in Table 39 of the *JEDEC Standard JESD209-3*. For CK_t, CK_c, use $V_{SEH}/V_{SEL(ac)}$ of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use $V_{IH}/V_{IL(ac)}$ of DQs.

b: Refers to Note 2 in Table 39 of the *JEDEC Standard JESD209-3*. $V_{IH(ac)}/V_{IL(ac)}$ for DQs is based on V_{REFDQ}; $V_{SEH(ac)}/V_{SEL(ac)}$ for CA is based on V_{REFCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

c: Refers to Note 3 in Table 39 of the *JEDEC Standard JESD209-3*. These values are not defined, however.the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.5 “Overshoot and Undershoot Specifications” on page 92 of the specification document.

Test References

- See *Table 27 in Section 8.3 of the DDR3 SDRAM Specification, JEDEC Standard JESD79-3E, July 2010* and
- See *Figure 124 and Table 40 in Section 7 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid strobe negative pulses in this burst. A valid strobe negative pulse starts at the V_{REF} crossing on a valid strobe falling edge and ends at the V_{REF} crossing on the following valid strobe rising edge.
4 For the first valid strobe negative pulse, zoom in on the pulse so that it appears on the oscilloscope’s display and measure T_{MIN}.
5 Measure V_{TIME} at the found T_{MIN} to get the minimum voltage of the pulse. Consider the V_{TIME} measurement result as the V_{SEL} value.
6 Continue the previous step for the rest of the valid strobe negative pulses that were found in the burst.
7 Determine the worst result from the set of V_{SEL} measured.

Expected/Observable Results

- The worst measured V_{SEL} must be within the specification limit.

Overshoot Amplitude/Area (Strobes Minus)

Test Overview

The Overshoot test can be divided into two sub-tests: Overshoot amplitude and Overshoot area.

The purpose of this test is to verify that the overshoot value of the test signal found from all regions of the acquired waveform is lower than or equal to the conformance limit of the maximum peak amplitude allowed for overshoot as specified in the JEDEC specification.

When there is an overshoot, the area is calculated based on the overshoot width and overshoot amplitude. The Overshoot area should be lower than or equal to the conformance limit of the maximum overshoot area allowed as specified in the JEDEC specification.

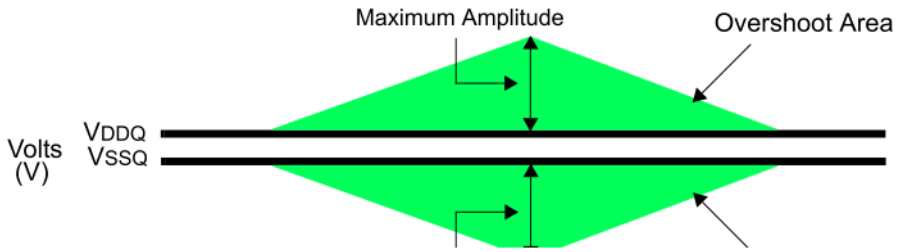


Figure 28 Strobe Overshoot

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Data Strobe Minus Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 70 AC Overshoot Specification for Strobe and Mask Pins

Parameter	Specification					
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133
Maximum peak amplitude allowed for overshoot area	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V
Maximum overshoot area above V_{DDQ}	0.25 V/ns	0.19 V/ns	0.15 V/ns	0.13 V/ns	0.11 V/ns	0.10 V/ns

Table 71 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for overshoot area	Max	0.35		V
Maximum area above V_{DD}	Max	0.12	0.10	V-ns

Test References

- See *Figure 100 and Table 37 in Section 9 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010* and
- See *Figure 126 and Table 49 in Section 8 of the LPDDR3 SDRAM Specification n in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Set the number of sampling points to 2M samples.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Obtain the overshoot region. Overshoot region starts at the rising VDDQ crossing and ends at the falling VDDQ crossing.

4 Within Overshoot region #1:

i Evaluate Overshoot Amplitude by performing the following steps:
a. Use TMAX and VMAX to get time stamp of maximum voltage on overshoot region of the acquired waveform.
b. Calculate: Overshoot Amplitude = VMAX – VDDQ.

ii Evaluate Area below VDDQ = (Overshoot Region End – Overshoot Region Start) * VDDQ.

iii Evaluate Total Area above 0 volt by using Trapezoidal Method Area Calculation as shown in following figure:

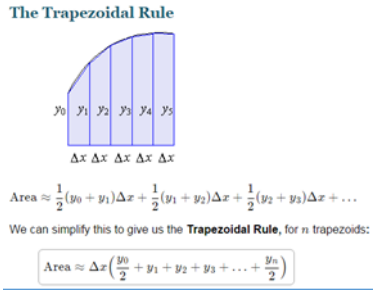


Figure 29 Trapezoidal Rule

iv Calculate area above VDDQ = Total area above 0 volt - area below VDDQ.

v Store calculated result below for later worst case finding process:

- Overshoot Amplitude
- Area above VDDQ

5 Repeat the previous step for the rest Overshoot Region found in acquired waveform.

6 Find the worst result below from stored result.

7 Compare test result to the compliance test limit.

- Overshoot Amplitude
- Area above VDDQ

Expected/Observable Results

- The measured maximum voltage value must be less than or equal to the maximum overshoot value.
- The calculated Overshoot area value must be less than or equal to the maximum Overshoot area allowed.

Undershoot Amplitude/Area (Strobes Minus)

Test Overview

The Undershoot Test can be divided into two sub-tests: Undershoot amplitude and Undershoot area.

The purpose of this test is to verify that the undershoot value of the test signal found from all regions of the acquired waveform is less than or equal to the conformance limit of the maximum peak amplitude allowed for undershoot as specified in the *JEDEC specification*.

When there is an undershoot, the area is calculated based on the undershoot width. The Undershoot area should be less than or equal to the conformance limit of the maximum undershoot area allowed as specified in the *JEDEC specification*.

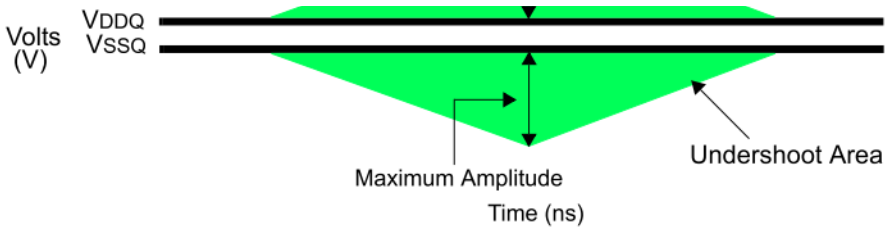


Figure 30 Strobe Undershoot

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Data Strobe Minus Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 72 AC Undershoot Specification for Clock, Data, Strobe and Mask Pins

Parameter	Specification					
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133
Maximum peak amplitude allowed for undershoot area	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V
Maximum undershoot area below V_{SSQ}	0.25 V/ns	0.19 V/ns	0.15 V/ns	0.13 V/ns	0.11 V/ns	0.10 V/ns

Table 73 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for undershoot area	Max	0.35		V
Maximum area below V_{SS}	Max	0.12	0.10	V-ns

Test References

- See *Figure 100 and Table 37 in Section 9 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Figure 126 and Table 49 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1. Set the number of sampling points to 2M samples.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Obtain the undershoot region. Undershoot Region starts at falling 0 volt crossing and end at rising 0 volt crossing.
4. Within Undershoot region #1, perform the following steps:
   - i Evaluate Undershoot Amplitude by performing the following steps:
     a. Use TMIN and VMIN to get time stamp of maximum voltage on undershoot region of the acquired waveform.
     b. Calculate: Undershoot Amplitude = 0- VMIN
   - ii Evaluate total area below 0 volt by using Trapezoidal Method Area Calculation (refer to Figure 29)
   - iii Store Calculated result below for later worst case finding process:
     - Undershoot Amplitude
     - Total area below 0 volt
5. Repeat the previous step for the rest Undershoot Region found in acquired waveform.
6. Find the worst result below from stored result.
7. Compare test result to the compliance test limit.
   - Undershoot Amplitude
   - Total area below 0 volt.

Expected/Observable Results

- The measured minimum voltage value for the test signal must be less than or equal to the maximum undershoot value.
- The calculated undershoot area value must be less than or equal to the maximum undershoot area allowed.

SlewR on Setup Region

Test Overview

The purpose of this test is to calculate the rising slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Modes Supported

- DDR3 and DDR3L

Signal cycle of interest:

- WRITE

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Minus Signals (supported by Data Signals)

Required Signals that are needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)

2 Take the first valid WRITE burst found.

3 Find all valid rising edges in the said burst. A valid rising edge starts at VIL (ac) crossing and end at following VIH (ac) crossing.

4 For all valid rising edges, find the transition time, delta TR which is time starts at VREF crossing and end at following VIH (ac) crossing. Then calculate Rising Slew.

$$\text{Rising Slew} = \frac{V_{IH(ac)}\ \text{min} - V_{REF}}{\text{delta TR}}$$

5 Determine the worst result from the set of SlewR measured.

Expected/Observable Results

- The calculated Rising Slew value for the test signal shall meet the user defined limit.

SlewF on Setup Region

Test Overview

The purpose of this test is to calculate the falling slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Minus Signals (supported by Data Signals)

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)

2 Take the first valid WRITE burst found.

3 Find all valid falling edges in the said burst. A valid falling edge starts at VIH (ac) crossing and end at following VIL (ac) crossing.

4 For all valid falling edges, find the transition time, delta TF which is time starts at VREF crossing and end at following VIL (ac) crossing. Then calculate Falling Slew.

$$\text{Falling Slew} = \frac{V_{REF} - V_{IL(ac)}\ \max}{\text{delta TF}}$$

5 Determine the worst result from the set of SlewF measured.

Expected/Observable Results

- The calculated Falling Slew value for the test signal shall meet the user defined limit.

SlewR on Hold Region

Test Overview

The purpose of this test is to calculate the rising slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Modes Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Minus Signals (supported by Data Signals)

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)
2. Take the first valid WRITE burst found.
3. Find all valid rising edges in the said burst. A valid rising edge starts at VIL (ac) crossing and end at following VIH (ac) crossing.
4. For all valid rising edges, find the transition time, delta TR which is time starts at VIL(DC) crossing and end at following VREF crossing. Then calculate Rising Slew.

$$Rising\ Slew = \frac{V_{REF} - V_{IL(DC)}}{\text{delta TR}}$$

5. Determine the worst result from the set of SlewR measured.

Expected/Observable Results

- The calculated Rising Slew value for the test signal shall meet the user defined limit.

SlewF on Hold Region

Test Overview

The purpose of this test is to calculate the falling slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Modes Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Minus Signals (supported by Data Signals)

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)

2 Take the first valid WRITE burst found.

3 Find all valid falling edges in the said burst. A valid falling edge starts at VIH (ac) crossing and end at following VIL (ac) crossing.

4 For all valid falling edges, find the transition time, delta TF which is time starts at VIH(DC) crossing and end at following VREF crossing. Then calculate Falling Slew.

$$Falling\ Slew = \frac{V_{IH(DC)} - V_{REF}}{\text{delta TF}}$$

5 Determine the worst result from the set of SlewF measured.

Expected/Observable Results

- The calculated Falling Slew value for the test signal shall meet the user defined limit.

9 Strobe Plus and Minus Cross Point Tests Group

This section provides the Methods of Implementation (MOIs) for Strobe Plus and Minus Cross Point tests using a Keysight Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application .

Probing for Strobe Plus and Minus Cross Point Tests

When performing the Strobe Plus and Minus Cross Point tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Strobe Plus and Minus Cross Point tests may look similar to the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance application for the exact number of probe connections.

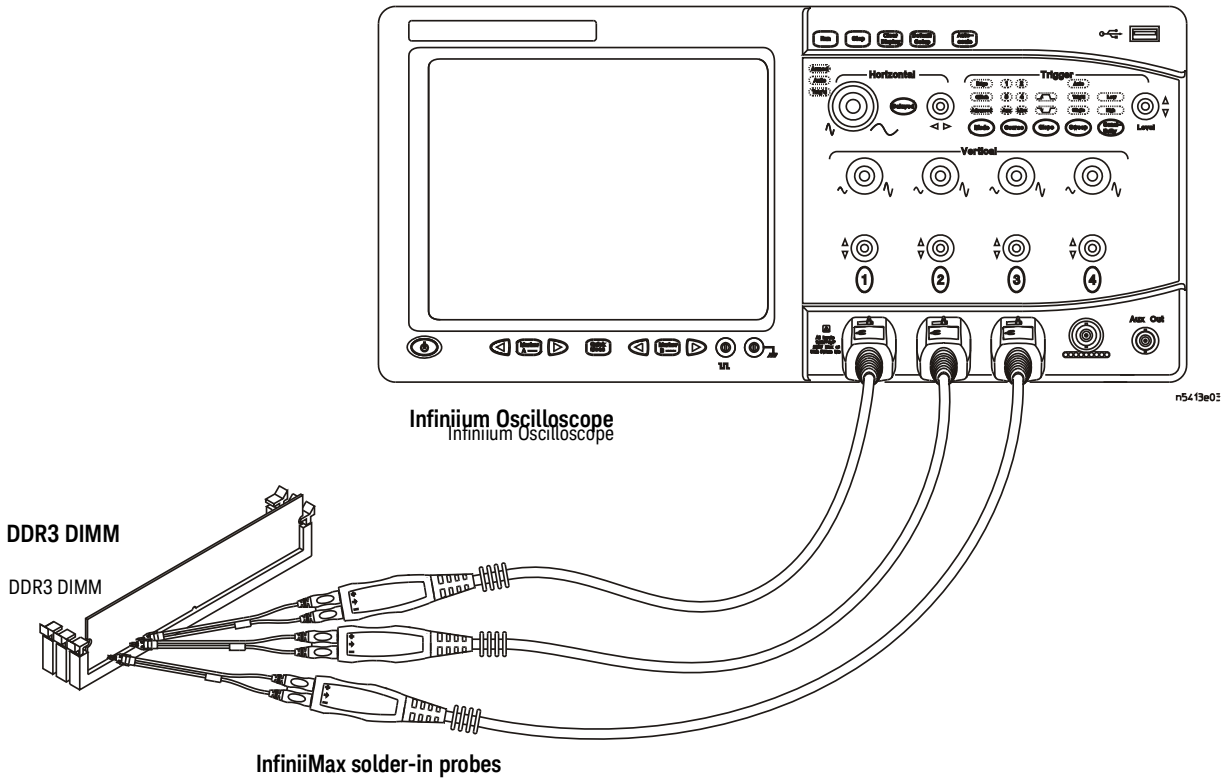


Figure 31 Probing for Strobe Plus and Minus Cross Point Tests

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 31 are just examples).

For more information on the probe amplifiers and differential probe heads, refer to the respective user guide for Probes.

Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform test on all unused RAM on the system by producing repetitive burst of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the **Set Up** tab.

6 Select the **Test Mode**, **SDRAM Type, Speed Grade**, and **AC Levels** options.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

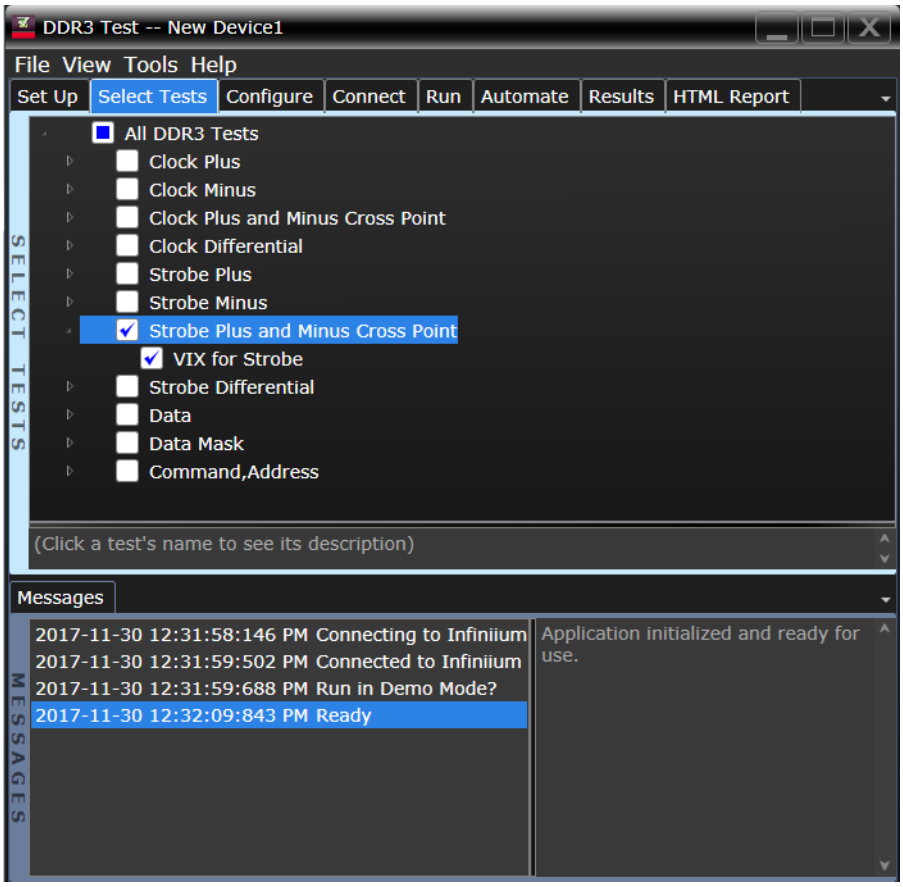


Figure 32 Selecting Strobe Plus and Minus Cross Point Tests

VIX for Strobe

Test Overview

The purpose of this test is to verify the crossing point voltage value of the input differential pair test signals is within the conformance limits of the V_{IXDQ} as specified in the JEDEC specification.

The value of VDDQ which directly affect the conformance upper limit is default to 1.5 V for typical DDR3 and 1.35V for DDR3L but users have the flexibility to change this value.

Modes Supported

- DDR3 and DDR3L

Signal cycle of Interest

- Write cycle

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Plus Signals and Data Strobe minus Signals (supported by Data Signals) OR

Signals required to perform the test on the oscilloscope

- Pin Under Test, PUT = Data Strobe Plus Signal.
- Pin Under Test, PUT = Data Strobe Minus Signals
- Supporting Pin = Data Signals

Test Definition Notes from the Specification

Table 74 Cross Point Voltage for Differential Input Signals (CK, DQS)

Symbol	Parameter	DDR3-800/1066/1333/1600/1866/2133		Units	Notes
		Min	Max		
$V_{IX(DQS)}$	Differential Input Cross Point Voltage relative to $V_{DDQ}/2$ for DQS_t, DQS_c	-150	150	mV	1[a], 2[b]

a: Refers to Note 1 in Table 40 of the *JEDEC Standard JESD209-3*. The typical value of $V_{IX(AC)}$ is expected to be about $0.5 \times V_{DD}$ of the transmitting device, and $V_{IX(AC)}$ is expected to track variation in V_{DD}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.

b: Refers to Note 2 in Table 40 of the *JEDEC Standard JESD209-3*. For CK_t and CK_c, $V_{Ref} = V_{RefCA(DC)}$. For DQS_t and DQS_c, $V_{Ref} = V_{RefDQ(DC)}$.

Table 75 Cross Point Voltage for Differential Input Signals (CK, DQS)

Symbol	Parameter	DDR3L-800, 1066, 1333 & 1600		Units	Notes
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DDQ}/2$ for DQS_t, DQS_c	-150	150	mV	1[a], 2[b]

a: Refers to Note 1 in Table 40 of the *JEDEC Standard JESD209-3*. The typical value of $V_{IX(AC)}$ is expected to be about $0.5 \times V_{DD}$ of the transmitting device, and $V_{IX(AC)}$ is expected to track variation in V_{DD}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.

b: Refers to Note 2 in Table 40 of the *JEDEC Standard JESD209-3*. For CK_t and CK_c, $V_{Ref} = V_{RefCA(DC)}$. For DQS_t and DQS_c, $V_{Ref} = V_{RefDQ(DC)}$.

Test References

- See *Figure 94 and Table 28 in Section 8 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See T*able 23 in Section 11 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1, July 2010.*

Measurement Algorithm

1 Sample and acquire the data waveforms.
2 Use the Subtract FUNC to generate the differential waveform from the two source inputs.
3 Split the read and write burst of the acquired signal.
4 Take down the first valid WRITE burst.
5 Find all differential DQS crossings that cross 0V.
6 Use VTime to get the actual crossing point voltage value using the timestamps obtained.
7 For each cross point voltage, calculate the final result:
8 V_{IXDQ} = cross point voltage - $V_{DD}/2$
9 Determine the worst result from the set of V_{IXDQ} measured.

Expected/Observable Results

- The measured crossing point value for the differential test signals pair must be within the conformance limit of the V_{IXDQ} value.

VIXDQ - Strobe Cross Point Voltage Test

Test Overview

The purpose of this test is to verify crossing point voltage value of the input differential pair test signals is within the conformance limits of the VIXDQ as specified in the JEDEC specification.

Mode Supported

- LPDDR3 only

Signal cycle of interest

- WRITE

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Plus Signals and Data Strobe Minus Signals (supported by Data Signals)

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = Data Strobe Plus Signals
- Pin Under Test, PUT = Data Strobe Minus Signals
- Supporting Pin = Data Signals

Test Definition Notes from the Specification

Table 76 Single-ended Levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL# or DQSU#

Symbol	Parameter	DDR3-800/1066/1333/1600		Units
		Min	Max	
V_{IXDQ}	Differential Input Cross Point Voltage relative to $V_{DDQ}/2$	-120	120	V

a: Refers to Note 3 in Table 27 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (V_{IH}(dc) max, V_{IL}(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Test References

- See *Figure 123 and Table 41 in Section 7 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1. Sample/Acquire data waveforms.
2. Use Subtract FUNC to generate the differential waveform from the 2 source input
3. Split read and write burst of the acquired signal.
4. Take the first valid WRITE burst found.
5. Find all differential DQS crossing that cross 0V.
6. Use VTime to get the actual crossing point voltage value using the timestamp obtained
7. For each cross point voltage, calculate the final result. VIXDQ = cross point voltage - VDDQ/2.
8. Determine the worst result from the set of VIXDQ measured.

Expected/Observable Results

- The measured crossing point value for the differential test signals pair must be within the conformance limit of the VIXDQ value.

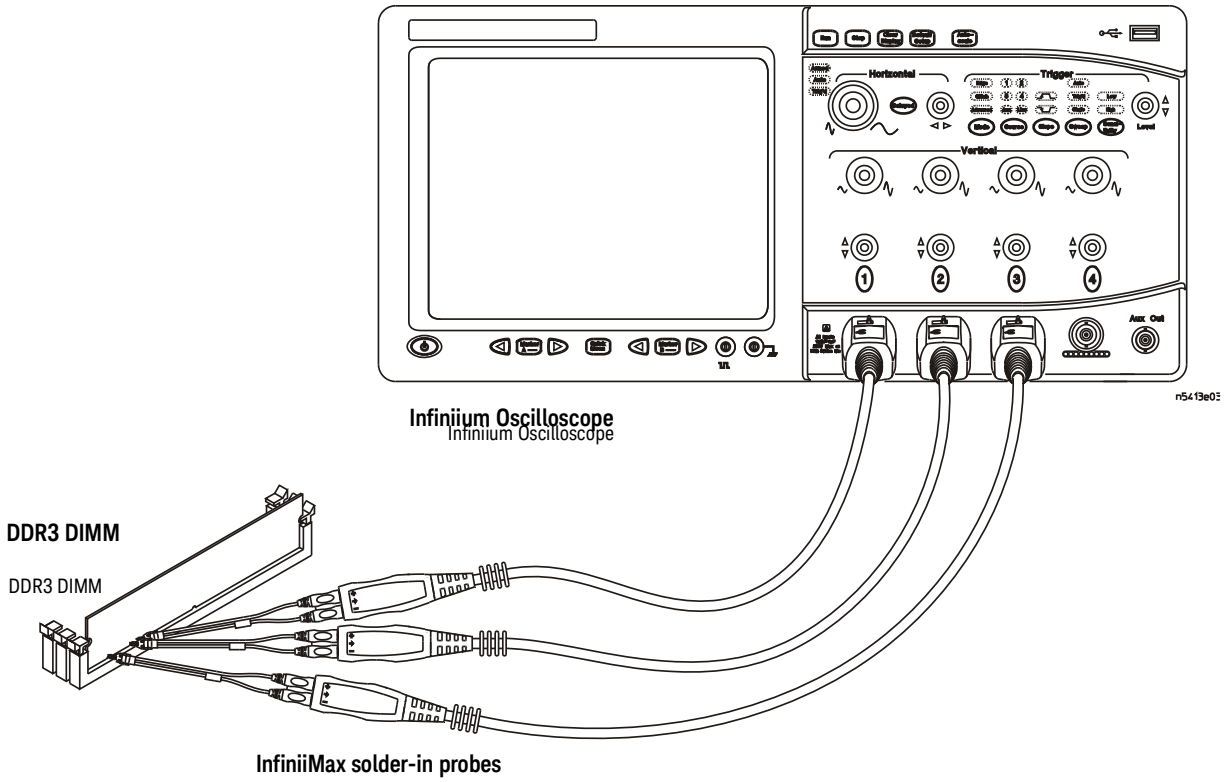
10 Strobe Differential Tests Group

This section provides the Methods of Implementation (MOIs) for Strobe Differential tests using a Keysight Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ refer to complement. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Strobe Differential Tests

When performing the Data Strobe Timing tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for Strobe Differential tests may look similar to the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.



InfiniiMax solder-in probes

Figure 33 Probing for Strobe Differential Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 33 are just examples).

For more information on the probe amplifiers and differential probe heads, refer to the respective user guide for Probes.

Test Procedure

1 Start the automated test application as described in “Starting the DDR3 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the Set Up tab.

6 Select the Speed Grade, Test Mode, SDRAM Type, and AC Levels options.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

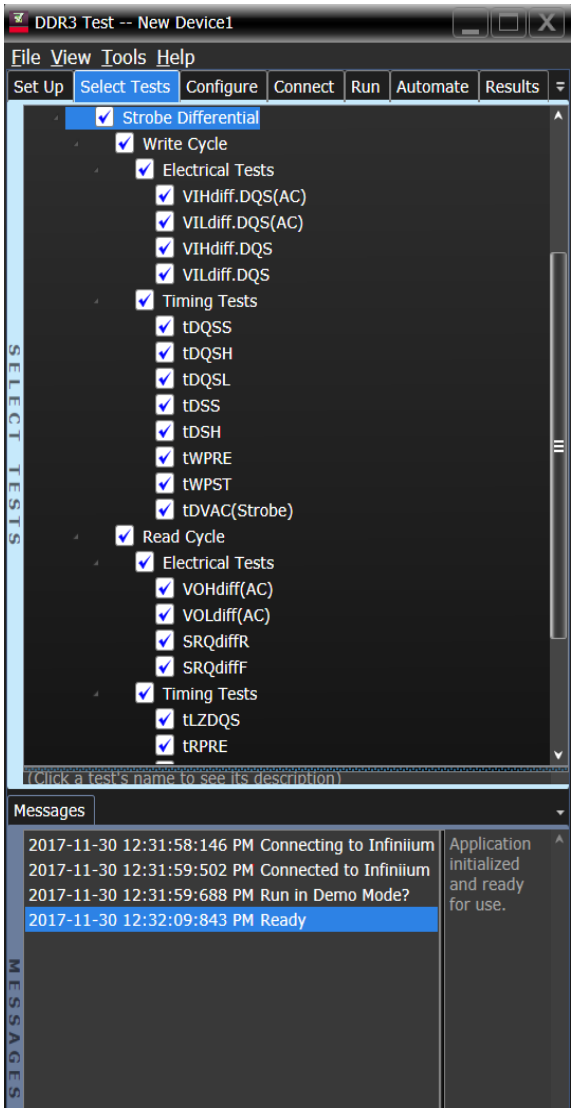


Figure 34 Selecting Strobe Differential Tests

Write Cycle Electrical Tests

VIHdiff.DQS(AC)

Test Overview

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{IHdiff(AC)}$ value as specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance limit) is set to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of $V_{IH(AC)}$ (which directly affects the conformance limit) is set according to the *JEDEC specification* based on the selected Data Rate, Test Type, and AC Level. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of $V_{IH(AC)}$.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQ

Test Definition Notes from the Specification

Table 77 Differential AC and DC Input Levels

Symbol	Parameter	DDR3-800/1066/1333/1600		Units
		Min	Max	
$V_{IHdiff(AC)}$	Differential input high AC for strobe	2 x ($V_{IH(AC)}$ - V_{REF})	Note 3[a]	V

a: Refers to Note 3 in Table 25 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Table 78 Differential AC and DC Input Levels

Symbol	Parameter	Value		Units	Notes
		Min	Max		
$V_{IHdiff(AC)}$	Differential input high AC	2 x ($V_{IH(AC)}$ - V_{REF})	Note 3[b]	V	2[a]

a: Refers to Note 3 in Table 25 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Test References

- *See Table 25 in Section 8.3 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E,July 2010* and
- See *Table 38 in Section 7 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid Strobe positive pulses in this burst. A valid Strobe positive pulse starts at the 0V crossing on a valid Strobe rising edge and ends at the 0V crossing on the following valid Strobe falling edge.

4 For the first valid Strobe positive pulse, zoom in on the pulse so that it appears on the oscilloscope’s display and perform the VTOP measurement. Take the VTOP measurement result as the $V_{IHdiff(AC)}$ value.

5 Continue the previous step for the rest of the valid Strobe positive pulses found in the burst.

6 Determine the worst result from the set of $V_{IHdiff(AC)}$ measured.

Expected/Observable Results

- The worst measured $V_{IHdiff(AC)}$ must be within the specification limit.

VILdiff.DQS(AC)

Test Overview

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{ILdiff(AC)}$ value as specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance limit) is set to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of $V_{IL(AC)}$ (which directly affects the conformance limit) is set according to the *JEDEC specification* based on the selected Data Rate, Test Type, and AC Level. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of $V_{IL(AC)}$.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write cycle

Require Read/Write separation

- Yes

Signal(s) of Interest

- Write cycle

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQ

Test Definition Notes from the Specification

Table 79 Differential AC and DC Input Levels

Symbol	Parameter	DDR3-800/1066/1333/1600		Units
		Min	Max	
$V_{ILdiff(AC)}$	Differential input low AC for strobe	Note 3[a]	2 x ($V_{IL(AC)}$ - V_{REF})	V

a: Refers to Note 3 in Table 25 of the *JEDEC Standard JESD79-3E*. These values are not defined, however.the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Table 80 Differential AC and DC Input Levels

Symbol	Parameter	Value		Units	Notes
		Min	Max		
$V_{ILdiff(AC)}$	Differential input low AC for strobe	2 x ($V_{IL(AC)}$ - V_{REF})	Note 3[b]	V	2[a]

a: Refers to Note 2 in Table 36 of the *JEDEC Standard JESD209-3*. For CK_t - CK_c, use $V_{IH}/V_{IL(AC)}$ of CA and V_{REFCA}; for DQS_t - DQS_c, use $V_{IH}/V_{IL(AC)}$ of DQs and V_{REFDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

b: Refers to Note 3 in Table 36 of the *JEDEC Standard JESD209-3*. These values are not defined, however.the single-ended signals CK_t, CK_c, DQS_t and DQS_c need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.5 “Overshoot and Undershoot Specifications” on page 92 of the specification document.

Test References

- See *Table 25 in Section 8.3 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Table 38 in Section 7 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid Strobe negative pulses in this burst. A valid Strobe negative pulse starts at the 0V crossing on a valid Strobe falling edge and ends at the 0V crossing on the following valid Strobe rising edge.

4 For the first valid Strobe negative pulse, zoom in on the pulse so that it appears on the oscilloscope’s display and perform the VBASE measurement. Take the VBASE measurement result as the $V_{ILdiff(AC)}$ value.

5 Continue the previous step for the rest of the valid Strobe negative pulses found in the burst.

6 Determine the worst result from the set of $V_{ILdiff(AC)}$ measured.

Expected/Observable Results

- The worst measured $V_{ILdiff(AC)}$ must be within the specification limit.

VIHdiff.DQS (DC)

Test Overview

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{IHdiff(DC)}$ value as specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance limit) is set to 0.6V for the typical LPDDR3 test type. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of $V_{IH(DC)}$ (which directly affects the conformance limit) is set according to the *JEDEC specification* based on the selected Data Rate, Test Type, and AC Level. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of $V_{IH(DC)}$.

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Write cycle

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQ

Test Definition Notes from the Specification

Table 81 Differential AC and DC Input Levels

Symbol	Parameter	Value		Units	Notes
		Min	Max		
$V_{IHdiff(DC)}$	Differential input high DC	2 x ($V_{IH(DC)}$ - V_{REF})	Note 3[b]	V	1[a]

a: Refers to Note 1 in Table 36 of the *JEDEC Standard JESD209-3*. Used to define a differential signal slew rate. For CK_t - CK_c, use $V_{IH}/V_{IL(dc)}$ of CA and V_{REFCA}; for DQS_t - DQS_c, use $V_{IH}/V_{IL(dc)}$ of DQs and V_{REFDQ}; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.

b: Refers to Note 3 in Table 36 of the *JEDEC Standard JESD209-3*. These values are not defined, however.the single-ended signals CK_t, CK_c, DQS_t and DQS_c need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.5 “Overshoot and Undershoot Specifications” on page 92 of the specification document.

Test References

- See *Table 38 in Section 7 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3, December 2011*.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid Strobe positive pulses in this burst. A valid Strobe positive pulse starts at the 0V crossing on a valid Strobe rising edge and ends at the 0V crossing on the following valid Strobe falling edge.

4 For the first valid Strobe positive pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform the VTOP measurement. Take the VTOP measurement result as the $V_{IHdiff(DC)}$ value.

5 Continue the previous step for the rest of the valid Strobe positive pulses found in the burst.

6 Determine the worst result from the set of $V_{IHdiff(DC)}$ measured.

Expected/Observable Results

- The worst measured $V_{IHdiff(DC)}$ must be within the specification limit.

VILdiff.DQS (DC)

Test Overview

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{ILdiff(DC)}$ value as specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance limit) is set to 0.6V for the typical LPDDR3 test type. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of $V_{IL(DC)}$ (which directly affects the conformance limit) is set according to the *JEDEC specification* based on the selected Data Rate, Test Type, and AC Level. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of $V_{IL(DC)}$.

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQ

Test Definition Notes from the Specification

Table 82 Differential AC and DC Input Levels

Symbol	Parameter	Value		Units	Notes
		Min	Max		
$V_{ILdiff(DC)}$	Differential input low	Note 3[b]	2 x ($V_{IL(DC)}$ - V_{REF})	V	1[a]

a: Refers to Note 1 in Table 36 of the *JEDEC Standard JESD209-3*. Used to define a differential signal slew rate. For CK_t - CK_c, use $V_{IH}/V_{IL(dc)}$ of CA and V_{REFCA}; for DQS_t - DQS_c, use $V_{IH}/V_{IL(dc)}$ of DQs and V_{REFDQ}; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.

b: Refers to Note 3 in Table 36 of the *JEDEC Standard JESD209-3*. These values are not defined, however.the single-ended signals CK_t, CK_c, DQS_t and DQS_c need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.5 “Overshoot and Undershoot Specifications” on page 92 of the specification document.

Test References

- See *Table 38 in Section 7 of the DDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid Strobe negative pulses in this burst. A valid Strobe negative pulse starts at the 0V crossing on a valid Strobe falling edge and ends at the 0V crossing on the following valid Strobe rising edge.

4 For the first valid Strobe negative pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform the VBASE measurement. Take the VBASE measurement result as the $V_{ILdiff(DC)}$ value.

5 Continue the previous step for the rest of the valid Strobe negative pulses found in the burst.

6 Determine the worst result from the set of $V_{ILdiff(DC)}$ measured.

Expected/Observable Results

- The worst measured $V_{ILdiff(DC)}$ must be within the specification limit.

VIHdiff.DQS

Test Overview

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window must be within the conformance limit of the V_{IHdiff} value as specified in the JEDEC specification.

Modes Supported

- DDR3 and DDR3L

Signal cycle of Interest

- Write cycle

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQ

Test Definition Notes from the Specification

Table 83 Differential AC and DC Input Levels

Symbol	Parameter	Value		Units
		Min	Max	
$V_{IHdiff(AC)}$	Differential input high AC for strobe	+0.200	Note 3[a]	V

a: Refers to Note 3 in Table 36 of the *JEDEC Standard JESD209-3*. These values are not defined, however.the single-ended signals CK_t, CK_c, DQS_t and DQS_c need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.5 “Overshoot and Undershoot Specifications” on page 92 of the specification document.

Test References

- See *Table 25 in Section 8.3 of the DDR3 SDRAM Specification, JEDEC Standard JESD79-3E, July 2010.*

Measurement Algorithm

1. Acquire and split read and write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid Strobe positive pulses in this burst. A valid Strobe positive pulse starts at the 0V crossing on a valid Strobe rising edge and ends at the 0V crossing on the following valid Strobe falling edge.
4. For the first valid Strobe positive pulse, zoom in on the pulse so that it appears on the oscilloscope’s display and perform the VTOP measurement. Take the VTOP measurement result as the V_{IHdiff} value.
5. Continue the previous step for the rest of the valid Strobe positive pulses found in the burst.
6. Determine the worst result from the set of V_{IHdiff} measured.

Expected/Observable Results

- The worst measured V_{IHdiff} must be within the specification limit.

VILdiff.DQS

Test Overview

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window must be within the conformance limit of the V_{ILdiff} value as specified in the JEDEC specification.

Modes Supported

- DDR3 and DDR3L only

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQ

Test Definition Notes from the Specification

Table 84 Differential AC and DC Input Levels

Symbol	Parameter	Value		Units	Notes
		Min	Max		
$V_{ILdiff(AC)}$	Differential input low ac for strobe	Note 3[a]	-0.200	V	1[a]

a: Refers to Note 3 in Table 36 of the *JEDEC Standard JESD209-3*. These values are not defined, however.the single-ended signals CK_t, CK_c, DQS_t and DQS_c need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.5 “Overshoot and Undershoot Specifications” on page 92 of the specification document.

Test References

- See *Table 25 in Section 8.3 of the DDR3 SDRAM Specification in the JEDEC Standard JESD209-3 July 2010*.

Measurement Algorithm

1. Acquire and split read and write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid Strobe negative pulses in this burst. A valid Strobe negative pulse starts at the 0V crossing on a valid Strobe falling edge and ends at the 0V crossing on the following valid Strobe rising edge.
4. For the first valid Strobe negative pulse, zoom in on the pulse so that it appears on the oscilloscope’s display and perform the VBASE measurement. Take the VBASE measurement result as the V_{ILdiff} value.
5. Continue the previous step for the rest of the valid Strobe negative pulses found in the burst.
6. Determine the worst result from the set of V_{ILdiff} measured.

Expected/Observable Results

- The worst measured V_{ILdiff} must be within the specification limit.

Write Cycle Timing Tests

tDQSS

Test Overview

The purpose of this test is to verify that the time interval from the data strobe output (first DQS rising edge) access time to the reference clock which is the previous of the associated clock (crossing point) must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- DDR3, DDR3L [for LPDDR3, refer to the tDQSS-Low Power test]

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signal (supported by Data Signal)
- Clock Signal

Signals required to perform the test on the oscilloscope

- Data Strobe Signal (DQS)
- Data Signal (DQ)
- Clock Signal

Optional signal required to separate the DQS signals for the different ranks of memory

- Chip Select Signal

Test Definition Notes from the Specification

Table 85 – Timing Parameters by Speed Bin

Symbol	Parameter	DDR3-800/1066/1333		Units
		Min	Max	
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.25	0.25	tck(avg)

Table 86 – Timing Parameters by Speed Bin

Symbol	Parameter	DDR3-1600/1866/2133		Units
		Min	Max	
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.27	0.27	tck(avg)

Test References

- See *Figure 44 and Table 68 & 69 in Section 13 of the DDR3 SDRAM Specification JEDEC Standard JESD79-3E, July 2010.*

Measurement Algorithm

1 Acquire and split the Read and Write bursts of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid rising DQS middle crossings in the said burst.

4 Find the first DQS rising edge by searching the earliest rising cross point among all found DQS cross points. Take the found point (first DQS rising edge) as the tDQSS strobe point.

5 Find the *closest Clock - DQS*; the Clock middle rising cross point that is closest to the first DQS rising edge.

6 Find the tDQSS Clock point which is the Clock middle rising cross point that is located at the one cycle before the *closest Clock - DQS*. Compare the tDQSS strobe point to the tDQSS Clock point as a test result. Mathematically, the test result = tDQSS strobe point - tDQSS Clock point.

7 Display the test result by locating the marker to the tDQSS strobe point and the tDQSS clock point at the measurement location on the waveform.

8 Compare the test result to the compliance test limit.

Expected/Observable Results

- The worst measured tDQSS value must be within the specification limit.

tDQSH

Test Overview

The purpose of this test is to verify that the width of the high level of the data strobe signal is within the conformance limit as specified in the JEDEC Specification.

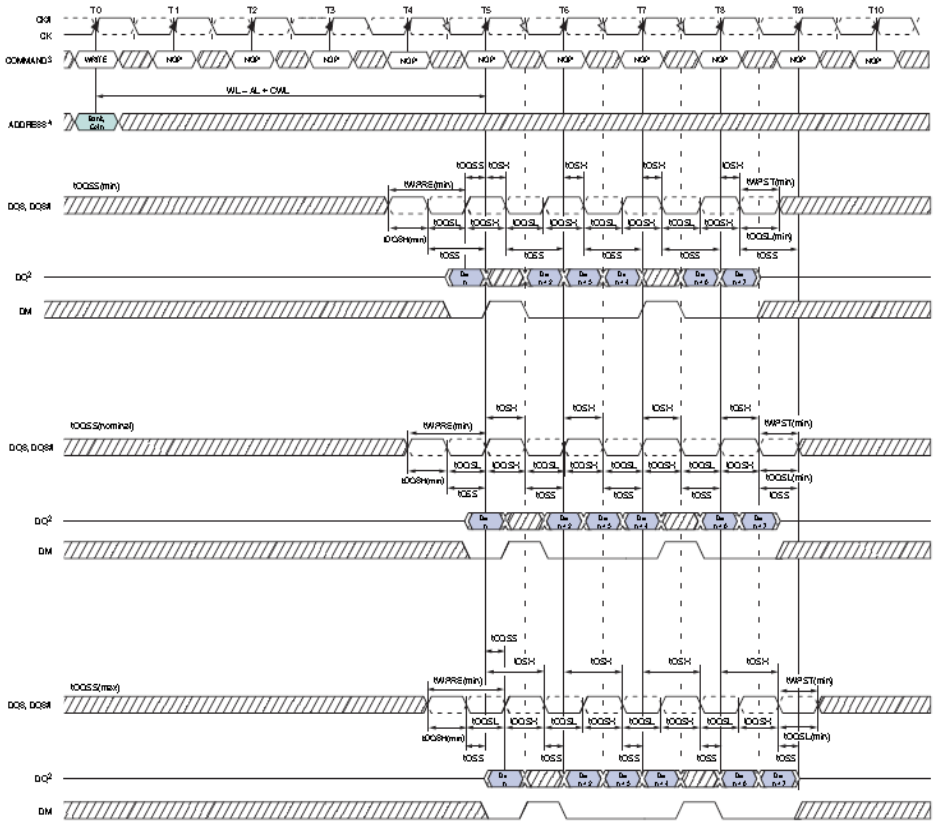


Figure 35 DQS Input High Pulse Width

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)

Optional signal required to separate the DQS signals for the different ranks of memory

- Chip Select Signal

Test Definition Notes from the Specification

Table 87 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)

Table 88 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
DQS input high level width	tDQSH	MIN	0.4		tCK(avg)

Test References

- See *Figure 44 and Table 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010* and
- See *Figure 121 and Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Acquire and split the Read and Write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising and falling DQS crossings in the said burst.
4 tDQSH is the time starting from a rising edge of the DQS and ending at the following falling edge.
5 Collect all tDQSH.
6 Determine the worst result from the set of tDQSH measured.

Expected/Observable Results

- The measured p-width of the data strobe signal must be within specification limit.

tDQSL

Test Overview

The purpose of this test is to verify that the width of the low level of the clock signal is within the conformance limit as specified in the JEDEC Specification.

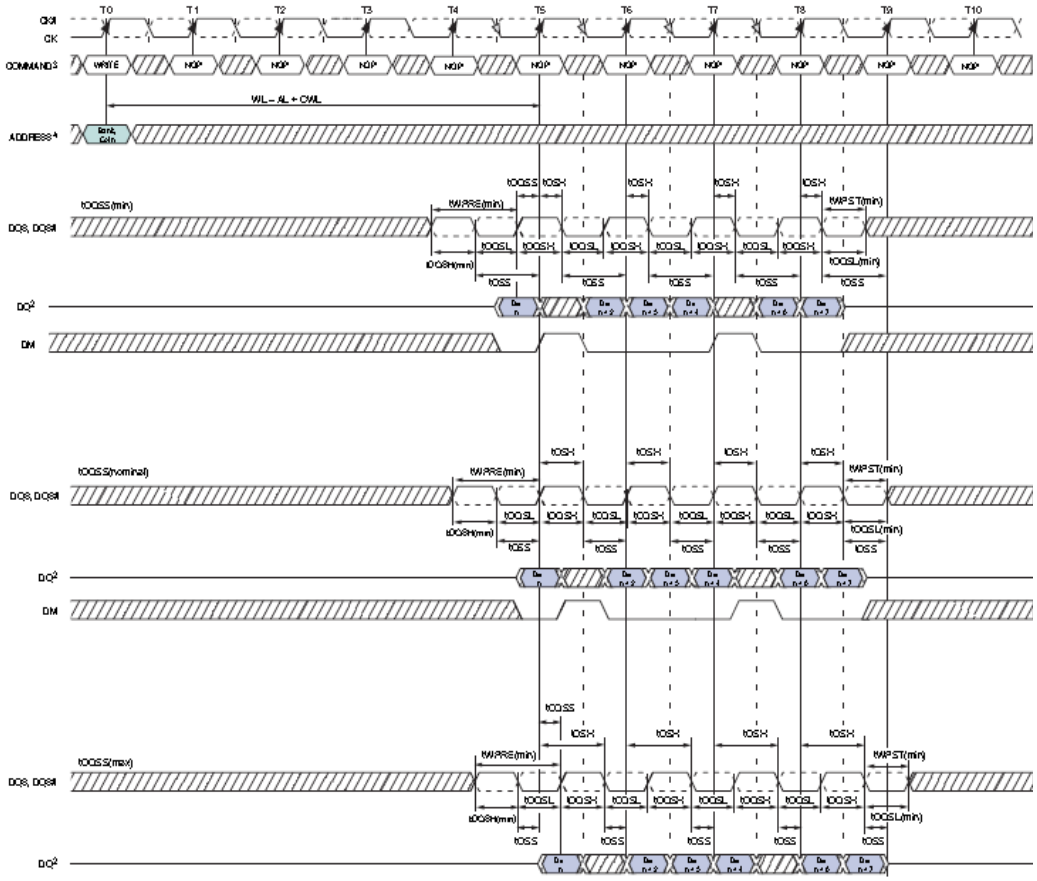


Figure 36 DQS Input Low Pulse Width

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)

Optional signal required to separate the DQS signals for the different ranks of memory

- Chip Select Signal

Test Definition Notes from the Specification

Table 89 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR-2133		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)

Table 90 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
DQS input low level width	tDQSL	MIN	0.4		tCK(avg)

Test References

- See *Figure 44 and Table 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Figure 121 and Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Acquire and split the Read and Write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising and falling DQS crossings in the said burst.
4 tDQSL is the time starting from a falling edge of the DQS and ending at the following rising edge.
5 Collect all tDQSL.
6 Determine the worst result from the set of tDQSL measured.

Expected/Observable Results

- The measured n-width of the clock signal must be within specification limit.

tDSS

Test Overview

The purpose of this test is to verify that the time interval from the falling edge of the data strobe (DQS falling edge) output access time to the clock setup time, is within the conformance limit as specified in the JEDEC Specification.

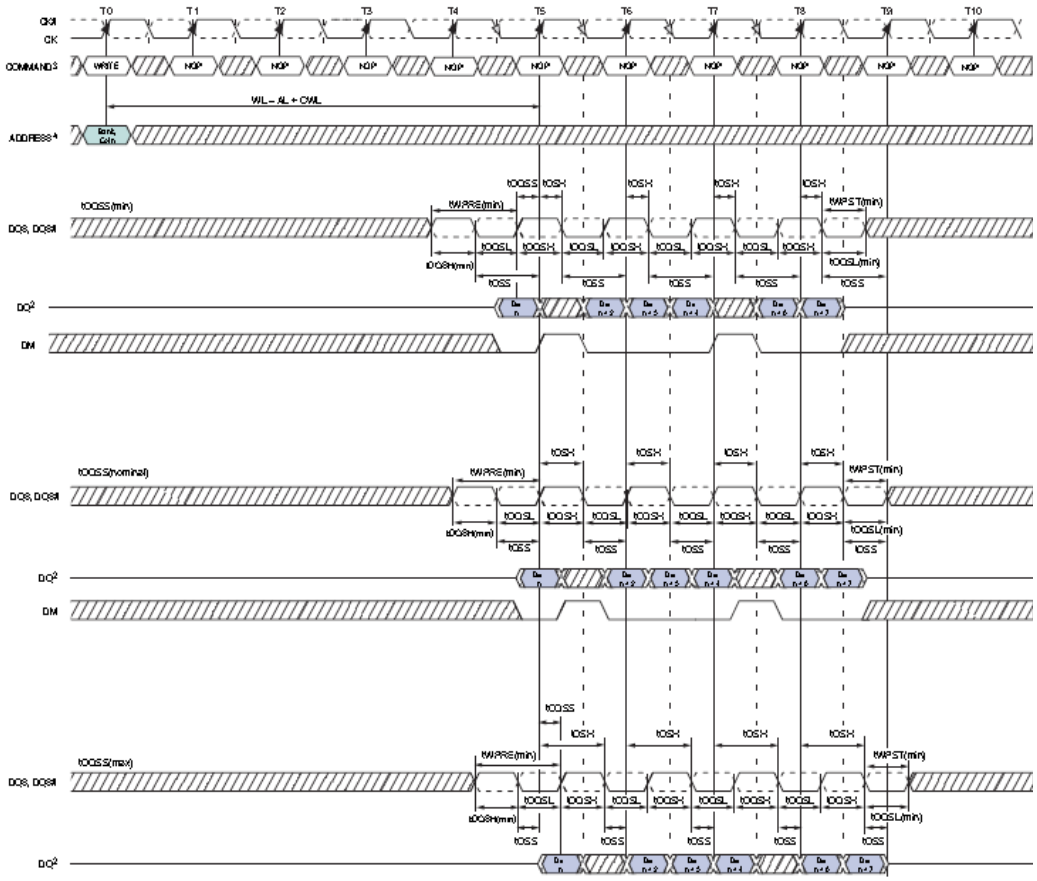


Figure 37 DQS Falling Edge to CK Setup Time

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the DQS signals for the different ranks of memory

- Chip Select Signal

Test Definition Notes from the Specification

Table 91 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	-	0.2	-	0.2	-	tCK(avg)

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.18	-	0.18	-	0.18	-	tCK(avg)

Table 92 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
DQS falling edge to CK setup time	tDSS	MIN	0.2		tCK(avg)

Test References

- See *Figure 44 and Table 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010* and
- See *Figure 122 and Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid falling DQS crossings in the said burst.
4. For all falling DQS crossings found, locate all nearest next rising Clock edges.
5. tDSS is the time between falling DQS crossings and the Clock rising edges found.
6. Collect all tDSS.
7. Determine the worst result from the set of tDSS measured.

Expected/Observable Results

- The measured time interval between the falling edge of the data strobe access output to the associated clock setup time must be within the specification limit.

tDSH

Test Overview

The purpose of this test is to verify that the time interval from the falling edge of the data strobe output access time to the hold time of the clock, must be within the conformance limit as specified in the JEDEC Specification.

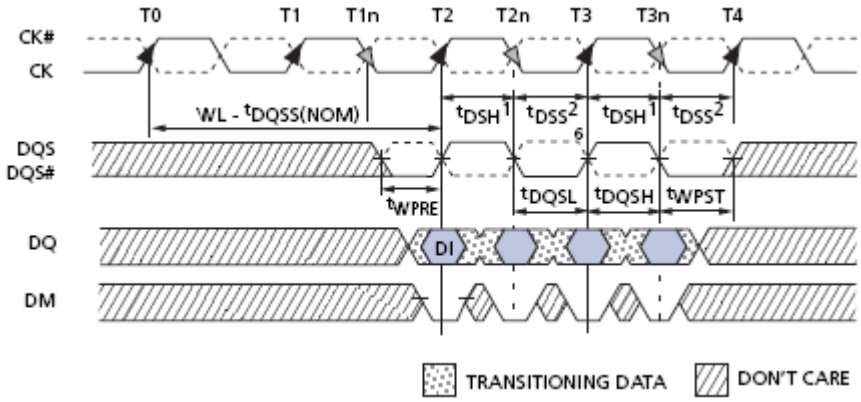


Figure 38 DQS Falling Edge Hold Time

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the DQS signals for the different ranks of memory

- Chip Select Signal

Test Definition Notes from the Specification

Table 93 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.2	-	0.2	-	0.2	-	tCK(avg)

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.18	-	0.18	-	0.18	-	tCK(avg)

Table 94 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
DQS falling edge hold time from CK	tDSH	MIN	0.2		tCK(avg)

Test References

- See *Figure 44 and Table 68 and 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010* and
- See *Figure 122 and Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all the valid falling DQS crossings in the said burst.
4. For all falling DQS crossings found, locate all nearest prior rising Clock edges.
5. tDSH is the time between falling DQS crossings and the Clock rising edges' crossing point found.
6. Collect all tDSH.
7. Determine the worst result from the set of tDSH measured.

Expected/Observable Results

- The measured time interval between the falling edge of the data strobe hold time from the associated clock crossing edge must be within the specification limit.

tWPRE

Test Overview

The purpose of this test is to verify that the time when the DQS starts to drive low (preamble behavior) to the first DQS signal crossing for the Write cycle, is within the conformance limit as specified in the JEDEC Specification.

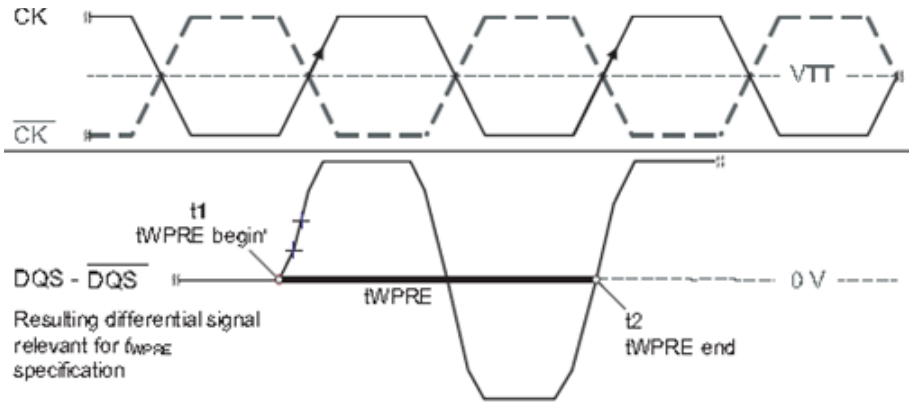


Figure 39 tWPRE Transitions and Endpoints Calculation

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the DQS signals for the different ranks of memory

- Chip Select Signal

Test Definition Notes from the Specification

Table 95 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# falling edge hold time from CK, CK# rising edge	tWPRE	0.9	-	0.9	-	0.9	-	tCK(avg)

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# falling edge hold time from CK, CK# rising edge	tWPRE	0.9	-	0.9	-	0.9	-	tCK(avg)

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
Write preamble	t_{WPRE}	MIN	0.8		tCK(avg)

Test References

- See *Figure 45 and Table 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010* and
- See *Figure 121 and Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011*.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find tLZBeginPoint of the said burst. (See notes on Find tLZBeginPoint (DQS))
4 Find the first rising edge on DQS of the found burst.
5 tWPRE is the time interval of the found rising DQS edge to the tLZBeginPoint found.
6 Report tWPRE.

Expected/Observable Results

- The measured tWPRE must be within the specification limit.

tWPST

Test Overview

The purpose of this test is to verify that the time when the DQS is no longer driving (from high/low state to high impedance) from the last DQS signal crossing (last bit of the write data burst) for the Write cycle, is within the conformance limit as specified in the JEDEC Specification.

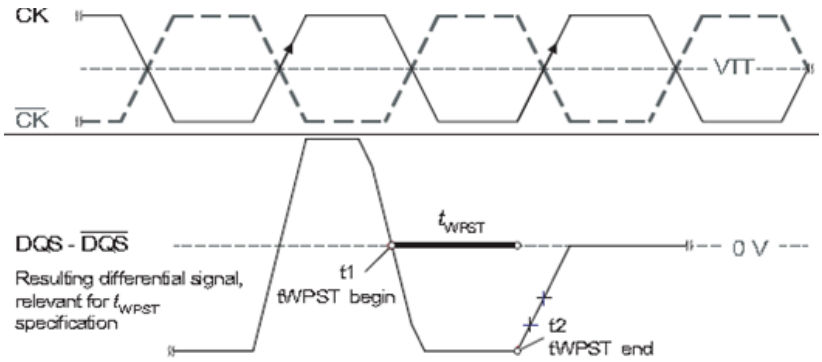


Figure 40 tWPST Transitions and Endpoints Calculation

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the DQS signals for the different ranks of memory

- Chip Select Signal

Test Definition Notes from the Specification

Table 96 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	tCK(avg)

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	tCK(avg)

Table 97 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
WRITE Postamble	tWPST	MIN	0.4		tCK(avg)

Test References

- See *Figure 46 and Table 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010* and
- See *Figure 121 and Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Acquire and split the Read and Write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find tHZEndPoint of the said burst.
4 Find the last falling edge on DQS prior to the tHZEndPoint found.
5 tWPST is the time between the falling DQS edge's crossings and the tHZEndPoint found.
6 Report tWPST.

Expected/Observable Results

- The measured time interval between the last DQS signal crossing point and the point where the DQS starts to transit from high/low state to high impedance must be within the specification limit.

tDVAC(Strobe)

Test Overview

The purpose of this test is to verify that the time of the strobe signal above $V_{IHdiff(AC)}$ and below $V_{ILdiff(AC)}$ must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- DDR3, DDR3L, and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope

- Data Strobe Signal (DQS)
- Data Signal (DQ)

Optional signal required to separate the DQS signals for the different ranks of memory

- Chip Select Signal

Test References

- See *Figure 91 in Section 8 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3F, July 2012.*

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising and falling DQS crossings at the $V_{IHdiff(AC)}$ and $V_{ILdiff(AC)}$ levels in the said burst.
4. tDVAC(Strobe) is the time starting from a DQS rising $V_{IHdiff(AC)}$ cross point and ending at the following DQS falling $V_{IHdiff(AC)}$ cross point.
5. tDVAC(Strobe) is the time starting from a DQS falling $V_{ILdiff(AC)}$ cross point and ending at the following DQS rising $V_{ILdiff(AC)}$ cross point.
6. Collect all tDVAC(Strobe).
7. Determine the worst result from the set of tDVAC(Strobe) measured.
8. Report the value of the worst tDVAC(Strobe).

Expected/Observable Results

- The worst measured tDVAC(Strobe) value must be within the specification limit.

Read Cycle Electrical Tests

VOHdiff(AC)

Test Overview

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{OHdiff(AC)}$ value as specified in the JEDEC specification.

The value of V_{DD} (which directly affects the conformance limit) is set to 1.5V for DDR3 and 1.2V for LPDDR3. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DD}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQ

Test Definition Notes from the Specification

Table 98 Differential AC and DC Output Levels

Symbol	Parameter	DDR3-800/1066/1333/1600	Units
$V_{OHdiff(AC)}$	AC differential output high measurement level	+ 0.2 x V_{DDQ}	V

Table 99 Differential AC and DC Output Levels

Symbol	Parameter	Value	Unit	Notes
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	+ 0.2 x V_{DDQ}	V	1[a]

a: Refers to Note 1 in Table 43 of the *JEDEC Standard JESD209-3*. I_{OH} = -0.1mA.

Test References

- See *Table 31 in Section 8.3 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010* and
- See *Table 44 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid Strobe positive pulses in this burst. A valid Strobe positive pulse starts at the 0V crossing on a valid Strobe rising edge and ends at the 0V crossing on the following valid Strobe falling edge.

4 For the first valid positive pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform the VTOP measurement. Take the VTOP measurement result as the $V_{OHdiff(AC)}$ value.

5 Continue the previous step for the rest of the valid Strobe positive pulses that were found in the burst.

6 Determine the worst result from the set of $V_{OHdiff(AC)}$ measured.

Expected/Observable Results

- The worst measured $V_{OHdiff(AC)}$ must be within the specification limit.

VOLdiff(AC)

Test Overview

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{OLdiff(AC)}$ value as specified in the JEDEC specification.

The value of V_{DD} (which directly affects the conformance limit) is set to 1.5V for DDR3 and 1.2V for LPDDR3. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DD}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQ

Test Definition Notes from the Specification

Table 100 Differential AC and DC Output Levels

Symbol	Parameter	DDR3-800/1066/1333/1600	Units
$V_{OLdiff(AC)}$	AC differential output low measurement level	- 0.2 x V_{DDQ}	V

Table 101 Differential AC and DC Output Levels

Symbol	Parameter	Value	Units	Notes
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	- 0.2 x V_{DDQ}	V	2[a]

a: Refers to Note 2 in Table 43 of the *JEDEC Standard JESD209-3*. I_{OL} = 0.1mA.

Test References

- See *Table 31 in Section 8.3 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010* and
- See *Table 44 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid Strobe negative pulses in this burst. A valid Strobe negative pulse starts at the 0V crossing on a valid Strobe falling edge and ends at the 0V crossing on the following valid Strobe rising edge.

4 For the first valid negative pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform the VBASE measurement. Take the VBASE measurement result as the $V_{OLdiff(AC)}$ value.

5 Continue the previous step for the rest of the valid Strobe negative pulses that were found in the burst.

6 Determine the worst result from the set of $V_{OLdiff(AC)}$ measured.

Expected/Observable Results

- The worst measured $V_{OLdiff(AC)}$ must be within the specification limit.

SRQdiffR

Test Overview

The purpose of this test is to verify that the differential output slew rate for rising edge of the test signal must be within the conformance limit of the SRQdiff value as specified in the JEDEC specification.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQ

Test Definition Notes from the Specification

Table 102 Differential Output Slew Rate

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential Output Slew Rate	SRQdiff	5	10	5	10	5	10	5	10	5	12	5	12	V/ns

Table 103 Differential AC and DC Output Levels

Parameter	Symbol	Value		Units
		Min	Max	
Differential output slew rate (RON = 40Ω ± 30%)	SRQdiff	4.0	8.0	V/ns

Test References

- See *Figure 97 and Table 35 in Section 8.3 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3F July 2012* and
- See *Figure 127 and Table 48 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid Strobe rising edges in this burst. A valid Strobe rising edge starts at the $V_{OLdiff(AC)}$ crossing and ends at the following $V_{OHdiff(AC)}$ crossing.
4 For all valid Strobe rising edges, find the transition time, T_R, which is the time that starts at the $V_{OLdiff(AC)}$ crossing and ends at the following $V_{OHdiff(AC)}$ crossing. Then calculate SRQdiffR = $[V_{OHdiff(AC)} - V_{OLdiff(AC)}]/T_R$.
5 Determine the worst result from the set of SRQdiffR measured.

Expected/Observable Results

- The worst measured SRQdiffR must be within the specification limit.

SRQdiffF

Test Overview

The purpose of this test is to verify that the differential output slew rate for falling edge of the test signal must be within the conformance limit of the SRQdiff value as specified in the JEDEC specification.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQ

Test Definition Notes from the Specification

Table 104 Differential Output Slew Rate

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential Output Slew Rate	SRQdiff	5	10	5	10	5	10	5	10	5	12	5	12	V/ns

Table 105 Differential Output Slew Rate

Parameter	Symbol	Value		Units
		Min	Max	
Differential output slew rate (RON = 40W ± 30%)	SRQdiff	3.0	8.0	V/ns

Test References

- See *Figure 97 and Table 35 in Section 8.3 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3F July 2012* and
- See *Figure 127 and Table 48 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid Strobe falling edge in this burst. A valid Strobe falling edge starts at the $V_{OHdiff(AC)}$ crossing and ends at the following $V_{OLdiff(AC)}$ crossing.

4 For all valid Strobe falling edges, find the transition time, T_R, which is the time that starts at the $V_{OHdiff(AC)}$ crossing and ends at the following $V_{OLdiff(AC)}$ crossing. Then calculate SRQdiffF = $[V_{OHdiff(AC)} - V_{OLdiff(AC)}]/T_R$.

5 Determine the worst result from the set of SRQdiffF measured.

Expected/Observable Results

- The worst measured SRQdiffF must be within the specification limit.

Read Cycle Timing Tests

tHZ(DQS)

Test Overview

tHZ(DQS) Test - DQS high-Z from clock.
The purpose of this test is to verify that the time when DQS no longer driving (*from Low state to the High-impedance state) to the reference clock signal crossing must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- DDR3 and DDR3L; for LPDDR3, please refer to the “tHZ(DQS) for Low Power” test

Signal Cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signal (supported by Data Signal) OR
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope

- Data Strobe Signal (DQS)
- Data Signal (DQ)
- Clock Signal (CK)

Optional signal required to separate the DQS signals for the different ranks of memory

- Chip Select Signal

Test Definition Notes from the Specification

Table 106 AC Timing - DDR3 and DDR3L

Parameter	Symbol	Min/Max	Data Rate						Unit
			800	1066	1333	1600	1866	2133	
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	MAX	400	300	250	225	195	180	ps

Test References

- See *Table 68 and 69 in Section 13.1 and 13.2, respectively, of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3F, July 2012 Revision.*

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Validate the read and write bursts obtained in the previous step. Invalid bursts are disregarded.
3 Take the first valid READ burst found.
4 Find tHZEndPoint on the DQS signal of the said burst.
5 Find the nearest Clock rising edge.
tHZ(DQS) is the time interval between Clock rising edge's crossing point and tHZEndPoint.
6 Report tHZ(DQS).

Expected/Observable Results

- The measured tHZ(DQS) value must be within the specification limit.

tHZ(DQS) for Low Power

Test Overview

tHZ(DQS) Test (Low Power)- DQS high-Z from clock.
The purpose of this test is to verify that the time when DQS no longer driving (*from Low state to the High-impedance state) to the reference clock signal crossing must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- LPDDR3; for DDR3 and DDR3L, please refer to the “tHZ(DQS)” test

Signal Cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signal (supported by Data Signal) OR
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope

- Data Strobe Signal (DQS)
- Data Signal (DQ)
- Clock Signal (CK)

Optional signal required to separate the DQS signals for the different ranks of memory

- Chip Select Signal

Test Definition Notes from the Specification

Table 107 AC Timing - LPDDR3

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	2133	
DQS High-Z from Clock	tHZ(DQS)	MAX	tDQSCK (MAX) - 100		ps

Test References

- *See Table 64 in Section 11.4 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3B, August 2013.*

Measurement Algorithm

1 Acquire and split Read and Write burst of the acquired signal.

2 Take the first valid Read burst found.

3 Find the Strobe tLZ start point of the said burst.

4 Find the RL Clock Edge (tDQSCK clock edge reference):

   i Find all DQS middle rising cross point in the said burst.(See notes on threshold).

   ii Find first DQS rising edge by search the earliest rising cross point among all found DQS middle cross point.

   iii Find the closest Clock - DQS : the Clock middle cross point that closest to first DQS rising edge.

   iv Find RL Clock Edge (tDQSCK clock edge reference) which clock middle crosspoint that before closest Clock – DQS at tDQSCK Delay (cycle). By default, tDQSCK Delay is three cycle. In example, for tDQSCK Delay = 3, tDQSCK clock point is clock middle crosspoint that three clock before closest Clock – DQS . For tDQSCK Delay = 5, tDQSCK clock point is clock middle crosspoint that five clock before closest Clock – DQS . tDQSCK Delay is configurable in configuration page.

5 Define BL (Bit Length) = the number of strobe middle crosspoint.

6 Find "RL+BL/2" Clock Edge: Clock middle rising cross point that BL/2 cycle after RL Clock Edge.

7 Compare Strobe tHZ end point to "RL+BL/2"Clock Edge point as test result. Mathematically: test result= Strobe tHZ end point - "RL+BL/2"Clock Edge point.

8 Display the test result by spot to measurement location on waveform and locate the marker to Strobe tHZ end point and Clock middle cross point of test result.

9 Compare test result to compliance test limit.

Expected/Observable Results

- The measured tHZ(DQS) value must be within the specification limit.

tLZ(DQS)

Test Overview

tLZ(DQS) Test DQS low-impedance time from CK#/CK.
The purpose of this test is to verify that the time when DQS start driving(*from tristate to High/Low state) to the clock signal crossing must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- DDR3, DDR3L [for LPDDR3, refer to the tLZ(DQS) (Low Power) test]

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signal (supported by Data Signal) OR
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope

- Data Strobe Signal (DQS)
- Data Signal (DQ)
- Clock Signal (CK)

Optional signal required to separate the DQS signals for the different ranks of memory

- Chip Select Signal

Test Definition Notes from the Specification

Table 108 Timing Parameters by Speed Bin

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-800	400	-600	300	-500	250	-450	255	ps

Table 109 Timing Parameters by Speed Bin

		DDR3-1866		DDR3-2133		Units
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-390	195	-360	180	ps

Test References

- See *Figure 30 and Table 68 & 69 in Section 13 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010.*

Measurement Algorithm

1 Acquire and split Read and Write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find tLZBeginPoint of the said burst. (See notes on Find tLZBeginPoint (DQS))
4 Find the nearest Clock rising edge.
5 tLZ(DQS) is the time interval of the found Clock rising edge's crossing point to the tLZBeginPoint found.
6 Report tLZ(DQS).

Expected/Observable Results

- The measured tLZ(DQS) value must be within the specification limit.

tLZ(DQS) for Low Power

Test Overview

tLZ(DQS) Test (Low Power) - DQS low-Z from clock.
The purpose of this test is to verify that the time when DQS starts driving (*from the tri-state to the Low state) to the reference clock signal crossing must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- LPDDR3 [for DDR3 and DDR3L, refer to the tLZ(DQS) test]

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope

- Data Strobe Signal (DQS)
- Data Signal (DQ)
- Clock Signal (CK)

Optional signal required to separate the DQS signals for the different ranks of memory

- Chip Select Signal

Test Definition Notes from the Specification

Table 110 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
DQS Low-Z from Clock	tLZ(DQS)	MIN	tDQSCK (MIN) - 300		ps

Test References

- See *Figure 119 and Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Acquire and split Read and Write burst of the acquired signal.
2 Take the first valid Read burst found.
3 Find the Strobe tLZ start point of the said burst.
4 Find the RL Clock Edge (tDQSCK clock edge reference):
   i Find all DQS middle rising cross points in the said burst.
   ii Find the first DQS rising edge by searching the earliest rising cross point among all found DQS middle cross points.
   iii Find the *closest Clock - DQS*; the Clock middle cross point that is closest to the first DQS rising edge.
   iv Find the RL Clock Edge (tDQSCK clock edge reference) which is the Clock middle cross point that is before the *closest Clock - DQS* at the tDQSCK Delay (cycle). By default, the tDQSCK Delay consists of three cycles. For example, when the tDQSCK Delay = 3, the tDQSCK Clock point is the Clock middle cross point that is located at the three clocks before the *closest Clock - DQS*. When the tDQSCK Delay = 5, the tDQSCK Clock point is the Clock middle cross point that is located at the five clocks before the *closest Clock - DQS*. The tDQSCK Delay can be configured at the Configure page.
5 Find “RL-1” Clock Edge; the previous Clock middle rising cross point of the RL Clock Edge.
6 Compare the Strobe tLZ start point to the “RL-1” Clock Edge point as a test result. Mathematically, the test result = Strobe tLZ start point - “RL-1” Clock Edge point.
7 Display the test result by locating the marker to the Strobe tLZ start point and the Clock middle cross point of the test result at the measurement location on the waveform.
8 Compare the test result to the compliance test limit.

Expected/Observable Results

- The measured tLZ(DQS) value must be within the specification limit.

tRPRE

Test Overview

The purpose of this test is to verify that the time when the DQS start driving low (*preamble behavior) to the first DQS signal crossing for the Read cycle must be within the conformance limit as specified in the *JEDEC Standard* specification.

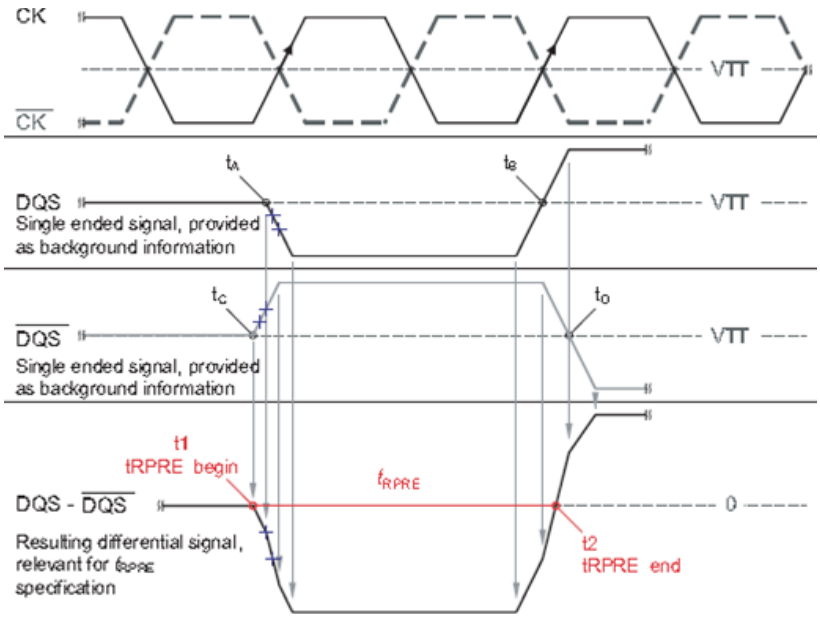


Figure 41 tRPRE Transitions and Endpoints Calculation

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the DQS signals for the different ranks of memory

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 111 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# differential READ Preamble	tRPRE	0.9	Note 19[a]	0.9	Note 19[a]	0.9	Note 19[a]	tCK(avg)

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# differential READ Preamble	tRPRE	0.9	Note 19[a]	0.9	Note 19[a]	0.9	Note 19[a]	tCK(avg)

a: Refers to Note 19 in Table 69 of the *JEDEC Standard JESD79-3E*. The maximum read preamble is bound by tLZ(DQS)min on the left side and tDQSCK(max) on the right side.See Figure 28 – "Clock to Data Strobe Relationship" on page 58 of the specification document.

Table 112 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
READ Preamble	tRPRE	MIN	0.9		tCK(avg)

Test References

- See *Figure 31 and Table 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010* and
- See *Figure 119 and Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid READ burst found.
3. Find tLZBeginPoint of the said burst.
4. Find the first rising edge on DQS of the found burst.
5. tRPRE is the time between the rising DQS edge and the tLZBeginPoint found.
6. Report tRPRE.

Expected/Observable Results

- The measured time interval of the point where the DQS starts to transit from tristate (high impedance state to low state) to the DQS signal crossing point for the Read cycle must be within the specification limit.

tRPST

Test Overview

The purpose of this test is to verify that the time when the DQS is no longer driving (from high/low state to high-impedance) to the last DQS signal crossing (last bit of the data burst) for the Read cycle is within the conformance limit as specified in the JEDEC Specification.

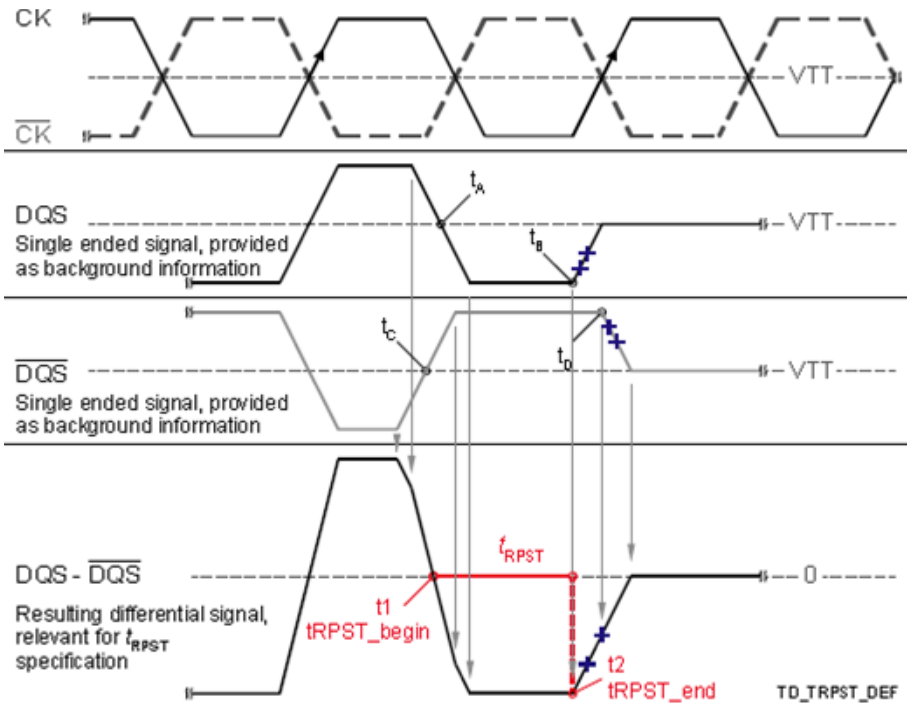


Figure 42 tRPST Transitions and Endpoints Calculation

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)

Optional signal required to separate the DQ signals for the different ranks of memory

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 113 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11[a]	0.3	Note 11[a]	0.3	Note 11[a]	tCK(avg)

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11[a]	0.3	Note 11[a]	0.3	Note 11[a]	tCK(avg)

a: Refers to Note 11 in Table 68 and 69 of the *JEDEC Standard JESD79-3E*. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See Figure 28 – "Clock to Data Strobe Relationship" on page 58 of the specification document.

Table 114 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
READ Postamble	tRPST	MIN	0.3		tCK(avg)

Test References

- See *Figure 32* and *Table 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010* and
- See *Figure 119* and *Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011*.

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid READ burst found.
3. Find tHZEndPoint of the said burst.
4. Find the last falling edge on DQS prior to the tHZEndPoint found.
5. tRPST is the time between the falling DQS edge's crossings and the tHZEndPoint found.
6. Report tRPST.

Expected/Observable Results

- The measured time interval between the last DQS signal crossing point to the point where the DQS starts to transit from high/low level to high impedance for the Read cycle must be within the specification limit.

tQSH

Test Overview

The purpose of this test is to verify that the width of the high level of the Data Strobe signal must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope

- Data Strobe Signal (DQS)
- Data Signal (DQ)

Optional signal required to separate the DQS signals for the different ranks of memory

- Chip Select Signal

Test Definition Notes from the Specification

Table 115 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
DQS output high pulse width	tQSH	MIN	tCH(abs) - 0.05		tCK(avg)

Test References

- See *Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Acquire and split the Read and Write bursts of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQS crossings in the said burst.
4 tQSH is the time starting from a rising edge of the DQS and ending at the following falling edge.
5 Collect all tQSH.
6 Determine the worst result from the set of tQSH measured.

Expected/Observable Results

- The worst measured tQSH value must be within the specification limit.

tQSL

Test Overview

The purpose of this test is to verify that the width of the low level of the Data Strobe signal must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope

- Data Strobe Signal (DQS)
- Data Signal (DQ)

Optional signal required to separate the DQS signals for the different ranks of memory

- Chip Select Signal

Test Definition Notes from the Specification

Table 116 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
DQS output low pulse width	tQSL	MIN	tCL(abs) - 0.05		tCK(avg)

Test References

- See *Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Acquire and split the Read and Write bursts of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQS crossings in the said burst.
4 tQSL is the time starting from a falling edge of the DQS and ending at the following rising edge.
5 Collect all tQSL.
6 Determine the worst result from the set of tQSL measured.

Expected/Observable Results

- The worst measured tQSL value must be within the specification limit.

tDQSCK

Test Overview

The purpose of this test is to verify that the time interval from data strobe output (DQS Rising Edge) access time to the nearest rising/falling edge of the clock must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- DDR3, DDR3L [for LPDDR3, refer to the tDQSCK (Low Power) test]

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope

- Data Strobe Signal (DQS)
- Data Signal (DQ)
- Clock Signal (CK)

Optional signal required to separate the DQS signals for the different ranks of memory

- Chip Select Signal

Test Definition Notes from the Specification

Table 117 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		
		Min	Max	Min	Max	Min	Max	Units
DQS,DQS# rising edge output access time from rising CK, CK#	tDQSCK)	-400	400	-300	300	-255	255	ps

Table 118 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-1866		DDR3-2133		
		Min	Max	Min	Max	Units
DQS,DQS# rising edge output access time from rising CK, CK#	tDQSCK)	-195	195	-180	180	ps

Test References

- See *Figure 28* and *Table 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010*.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)
2. Take the first valid READ burst found.
3. Find all valid rising DQS crossings at Vref in the said burst. (See notes on threshold)
4. For all DQS crossings found, locate the nearest rising Clock crossing at 0V. (See notes on threshold)
5. Take the time different from DQS crossing to the corresponding Clock crossing as the tDQSCK.
6. Determine the worst result from the set of tDQSCK measured.

Expected/Observable Results

- The measured tDQSCK value must be within the specification limit.

11 Data Tests Groups

This section provides the Methods of Implementation (MOIs) for Data tests using a Keysight Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

Probing for Data Tests

When performing the Data tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Data tests may look similar to the following diagram. Refer to the Connection tab in the DDR3 Electrical Performance Compliance application for the exact number of probe connections.

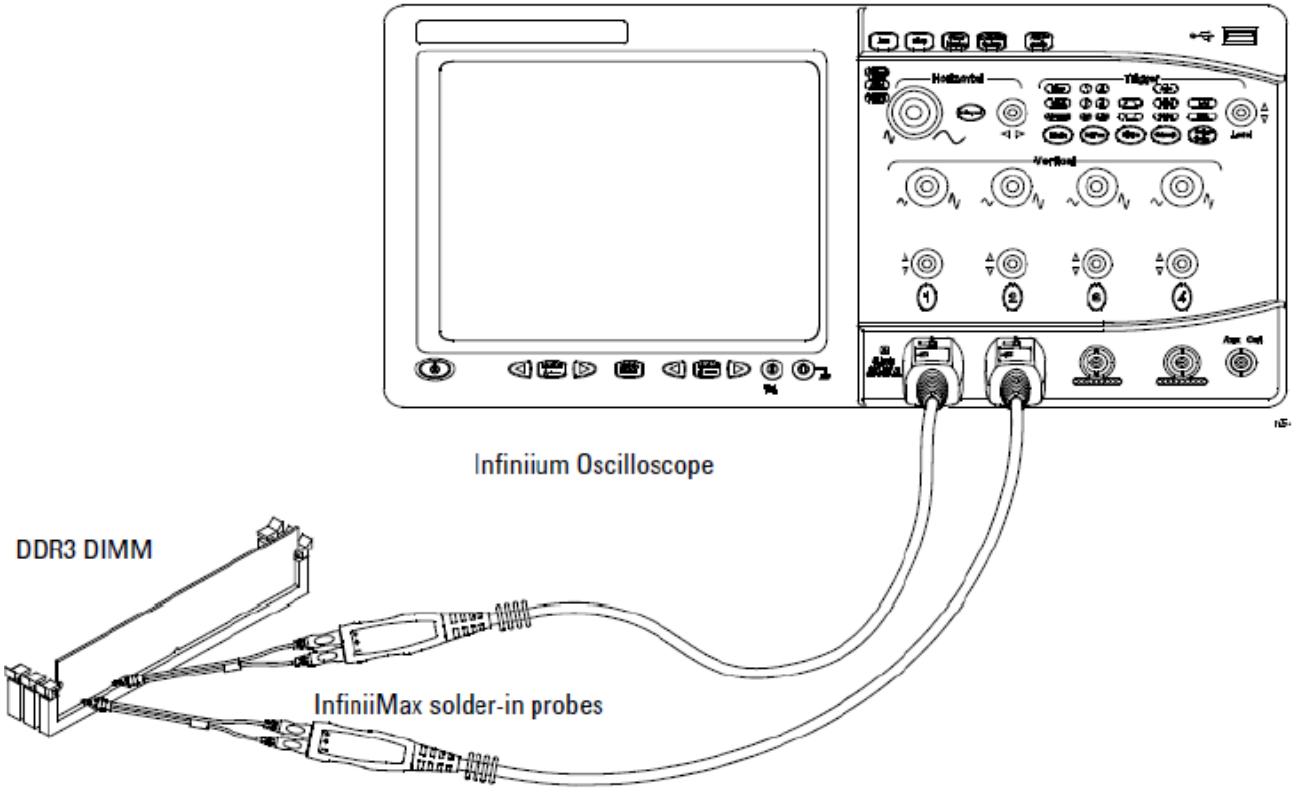


Figure 43 Probing for Data Tests with Two Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 43 are just examples).

For more information on the probe amplifiers and differential probe heads, refer to the respective user guide for Probes.

Test Procedure

1 Start the automated test application as described in “Starting the DDR3 Compliance Test Application" on page 25.
2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR3 memory.
3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.
4 Connect the oscilloscope probes to any channels of the oscilloscope.
5 In the DDR3 Test application, click the **Set Up** tab.
6 Select the **Test Mode**, **SDRAM Type, Speed Grade**, and **AC Levels** options.
7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

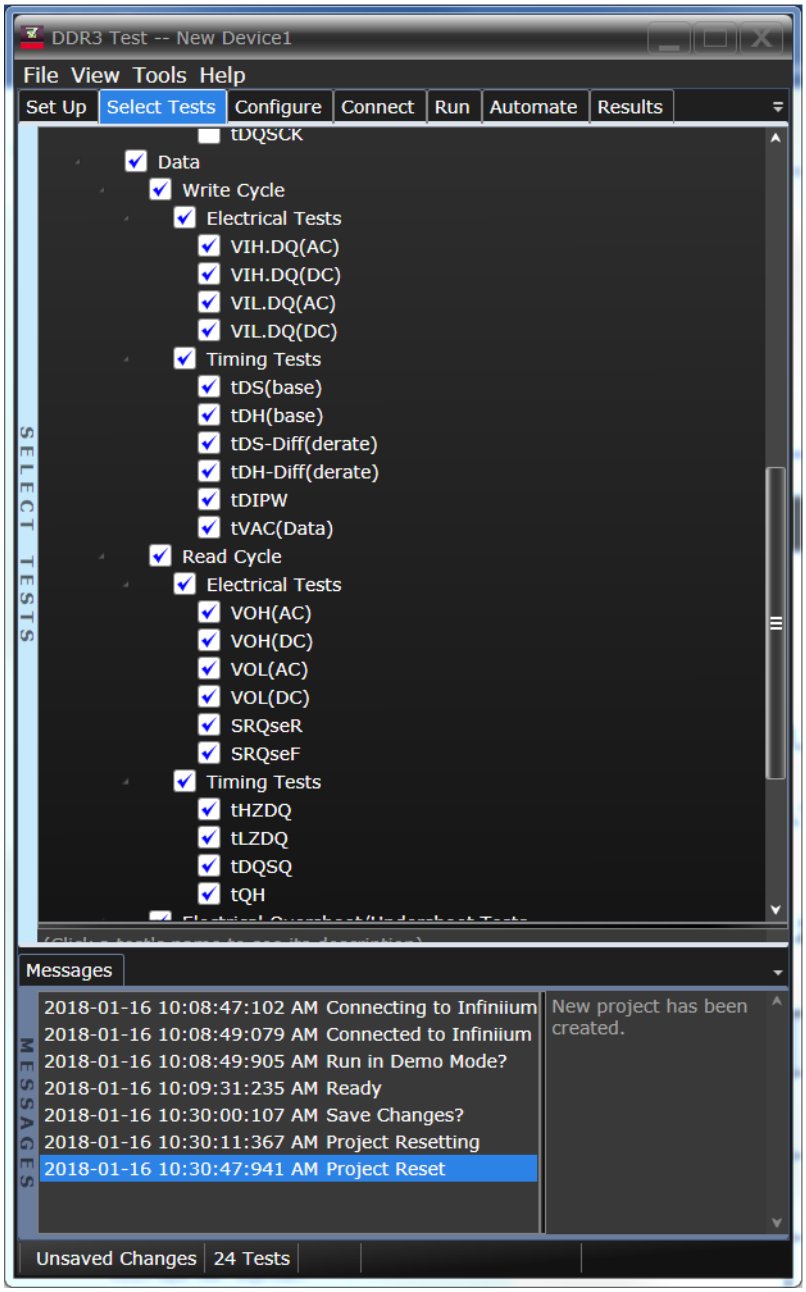


Figure 44 Selecting Data Tests

Write Cycle Electrical Tests

VIH.DQ(AC)

Test Overview

The purpose of this test is to verify that the voltage level of the test signal at tDS (DM and DQ input setup time in JEDEC specification) with reference to the DQS signal is greater than the conformance lower limits of the $V_{IH(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signals (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQS

Test Definition Notes from the Specification

Table 119 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-800/1066/1333/1600		DDR3-1866/2133		Units
		Min	Max	Min	Max	
$V_{IH,DQ(AC\ 175)}$	AC input logic high	V_{REF} + 0.175	Note 2[a]	-	-	V
$V_{IH,DQ(AC\ 150)}$	AC input logic high	V_{REF} + 0.150	Note 2[a]	-	-	V
$V_{IH,DQ(AC\ 135)}$	AC input logic high	-	-	V_{REF} + 0.135	Note 2[a]	V

a: Refers to Note 2 in Table 24 of the *JEDEC Standard JESD79-3E. See* section 9.6 "Overshoot and Undershoot Specifications" on page 126 of the specification document.

Table 120 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3L-800/1066		DDR3-1333/1600		Units
		Min	Max	Min	Max	
$V_{IH,DQ(AC\ 160)}$	AC input logic high	V_{REF} + 0.160	Note 2[a]	-	-	V
$V_{IH,DQ(AC\ 135)}$	AC input logic high	V_{REF} + 0.135	Note 2[a]	V_{REF} + 0.135	Note 2[a]	V

a: Refers to Note 2 in Table 5 of the *JEDEC Standard JESD79-3-1*. See section 9.6.2 of "Overshoot and Undershoot Specifications" of the *JEDEC Standard JESD79-3E*.

Table 121 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IH,DQ(AC)}$	AC input logic high	V_{REF} + 0.150	Note 2[b]	V	1[a], 2[b], 5[c]

a: Refers to Note 1 in Table 35 of the *JEDEC Standard JESD209-3*. For DQ input only pins. $V_{Ref} = V_{RefDQ(DC)}$.

b: Refers to Note 2 in Table 35 of the *JEDEC Standard JESD209-3*. See section 8.5 "Overshoot and Undershoot Specifications" on page 92 of the specification document.

c: Refers to Note 5 in Table 35 of the *JEDEC Standard JESD209-3*. For reference: $V_{ODTR}/2$ +/- 12mV.

Test References

- See *Table 24 in Section 8.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010,*
- See *Table 5 in Section 3.2 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1, July 2010* and
- See *Table 37 in Section 7 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IH(AC)}$ in the said burst.
4 For all DQ crossings found, locate all next DQS crossings that cross 0V.
5 Calculate the time where the test result is taken. Calculation is expressed as $T_{TESTRESULT} = T_{DQS\ MIDPOINT} - tDS$.
(tDS - DM and DQ input setup time in JEDEC specification which due to speed grade.)
6 Take voltage level of DQ signal at $T_{TESTRESULT}$ as the test result for $V_{IH(AC)}$.
7 Collect all $V_{IH(AC)}$.
8 Determine the worst result from the set of $V_{IH(AC)}$ measured.

Expected/Observable Results

- The voltage level of the test signal at tDS with reference to the DQS signal must be greater than or equal to the minimum $V_{IH(AC)}$ value.

VIH.DQ(DC)

Test Overview

The purpose of this test is to verify that the histogram minimum value of the test signal within the sampling window (from signal tDS to tDH with reference to the DQS signal) is within the conformance limits of the $V_{IH(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. Users may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of VDD which directly affects the conformance lower limit is set to 1.50V for typical DDR3, 1.35V for DDR3L and 1.2V for LPDDR3. Users may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customize test limit set based on different values of VDD.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signals (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQS

Test Definition Notes from the Specification

Table 122 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-800/1066/1333/1600		DDR3-1866/2133		Units
		Min	Max	Min	Max	
$V_{IH,DQ(DC\ 100)}$	DC input logic high	V_{REF} + 0.100	V_{DD}	V_{REF} + 0.100	V_{DD}	V

Table 123 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3L-800/1066		DDR3L-1333/1600		Units
		Min	Max	Min	Max	
$V_{IH,DQ(DC\ 90)}$	DC input logic high	V_{REF} + 0.09	V_{DD}	V_{REF} + 0.09	V_{DD}	V

Table 124 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IHDQ(DC)}$	DC input logic high	V_{REF} + 0.100	V_{DDQ}	V	1[a]

a: Refers to Note 1 in Table 35 of the *JEDEC Standard JESD209-3*. For DQ input only pins. $V_{Ref} = V_{RefDQ(DC)}$.

Test References

- See *Table 24 in Section 8.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010,*
- See *Table 5 in Section 3.2 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1, July 2010* and
- See *Table 37 in Section 7 of the DDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid rising DQ crossings that cross $V_{IH\ (DC)}$ in the said burst.

4 For all DQ crossings found, locate all next DQS crossings that cross midpoint. (0V for differential DQS and V_{REF} for single ended DQS.)

5 Setup the histogram function settings.

6 Set the histogram window as follows:

   i Ax: X-time position of tDS (DM and DQ input setup time in JEDEC specification) before DQS crossing midpoint.

   ii Bx: X-time position of tDH (DM and DQ input hold time in JEDEC specification) after DQS crossing midpoint.

   iii By: Y-position at V_{REF} voltage level.

   iv Ay: Top of the displaying window to make sure it covers the maximum level of the respective signal.

7 Use histogram 'Minimum' value as the test result for $V_{IH(DC)}$.

8 Collect all $V_{IH\ (DC)}$.

9 Determine the worst result from the set of $V_{IH\ (DC)}$ measured.

Expected/Observable Results

- The histogram minimum value of the test signal within the sampling window (from signal tDS to tDH with reference to the DQS signal) must be within the specification limits.

VIL.DQ(AC)

Test Overview

The purpose of this test is to verify that the voltage level of the test signal at tDS (DM and DQ input setup time in JEDEC specification) with reference to the DQS signal is lower than the conformance lower limits of the $V_{IL(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signals (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQS

Test Definition Notes from the Specification

Table 125 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-800/1066		DDR3-1333/1600		DDR3-1866/2133		Units
		Min	Max	Min	Max	Min	Max	
$V_{IL,DQ(AC\ 175)}$	AC input logic low	Note 2[a]	V_{REF} - 0.175	-	-	-	-	V
$V_{IL,DQ(AC\ 150)}$	AC input logic low	Note 2[a]	V_{REF} - 0.150	Note 2[a]	V_{REF} - 0.150	-	-	V
$V_{IL,DQ(AC\ 135)}$	AC input logic low	-	-	-	-	Note 2[a]	V_{REF} - 0.135	V

a: Refers to Note 2 in Table 24 of the *JEDEC Standard JESD79-3E. See* section 9.6 "Overshoot and Undershoot Specifications" on page 126 of the specification document.

Table 126 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3L-800/1066		DDR3L-1333/1600		Units
		Min	Max	Min	Max	
$V_{IL,DQ(AC\ 160)}$	AC input logic low	Note 2[a]	V_{REF} - 0.160	-	-	V
$V_{IL,DQ(AC\ 135)}$	AC input logic low	Note 2[a]	V_{REF} - 0.135	Note 2[a]	V_{REF} - 0.135	V

a: Refers to Note 2 in Table 5 of the *JEDEC Standard JESD79-3-1*. See section 9.6.2 of "Overshoot and Undershoot Specifications" of the *JEDEC Standard JESD79-3E*.

Table 127 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IL,DQ(AC)}$	AC input logic low	Note 2[b]	V_{REF} - 0.150	V	1[a], 2[b], 5[c]

a: Refers to Note 1 in Table 35 of the *JEDEC Standard JESD209-3*. For DQ input only pins. $V_{Ref} = V_{RefDQ(DC)}$.

b: Refers to Note 2 in Table 35 of the *JEDEC Standard JESD209-3*. See section 8.5 "Overshoot and Undershoot Specifications" on page 92 of the specification document.

c: Refers to Note 5 in Table 35 of the *JEDEC Standard JESD209-3*. For reference: $V_{ODTR}/2$ +/- 12mV.

Test References

- See *Table 24 in Section 8.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010,*
- See *Table 5 in Section 3.2 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1, July 2010 and*
- See *Table 37 in Section 7 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid falling DQ crossings that cross $V_{IL\ (AC)}$ in the said burst.

4 For all DQ crossings found, locate all next DQS crossings that cross midpoint. (0V for differential DQS and V_{REF} for single ended DQS.)

5 Calculate the time where the test result is taken. Calculation is expressed as $T_{TESTRESULT} = T_{DQS\ MIDPOINT} - tDS$.
(tDS - DM and DQ input setup time in the JEDEC specification due to speed grade.)

6 Take voltage level of DQ signal at $T_{TESTRESULT}$ as the test result for $V_{IL(AC)}$.

7 Collect all $V_{IL(AC)}$.

8 Determine the worst result from the set of $V_{IL(AC)}$ measured.

Expected/Observable Results

- The voltage level of the test signal at tDS with reference to the DQS signal must be less than or equal to the maximum $V_{IL(AC)}$ value.

VIL.DQ(DC)

Test Overview

The purpose of this test is to verify that the histogram maximum value of the test signal within the sampling window (from signal tDS to tDH with reference to the DQS signal) is within the conformance limits of the $V_{IL(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signals (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQS

Test Definition Notes from the Specification

Table 128 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-800/1066/1333/1600		DDR3-1866/2133		Units
		Min	Max	Min	Max	
$V_{IL,DQ(DC\ 100)}$	DC input logic low	V_{SS}	V_{REF} - 0.100	V_{SS}	V_{REF} - 0.100	V

Table 129 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3L-800/1066		DDR3-1333/1600		Units
		Min	Max	Min	Max	
$V_{IL,DQ(DC\ 90)}$	DC input logic low	V_{SS}	V_{REF} - 0.09	V_{SS}	V_{REF} - 0.09	V

Table 130 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IL,DQ(DC)}$	DC input logic low	V_{SSQ}	V_{REF} - 0.100	V	1[a]

a: Refers to Note 1 in Table 35 of the *JEDEC Standard JESD209-3*. For DQ input only pins. $V_{Ref} = V_{RefDQ(DC)}$.

Test References

- See *Table 24 in Section 8.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010*,
- See T*able 5 in Section 3.2 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1 July 2010* and
- See *Table 37 in Section 7 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid falling DQ crossings that cross $V_{IL(DC)}$ in the said burst.

4 For all DQ crossings found, locate all next DQS crossings that cross midpoint. (0V for differential DQS and V_{REF} for single ended DQS.)

5 Setup the histogram function settings.

6 Set the histogram window as follows:

   i Ax: X-time position of tDS (DM and DQ input setup time in JEDEC specification) before DQS crossing midpoint.

   ii Bx: X-time position of tDH (DM and DQ input hold time in JEDEC specification) after DQS crossing midpoint.

   iii By: Y-position at V_{REF} voltage level.

   iv Ay: Top of the displaying window to make sure it covers the maximum level of the respective signal.

7 Use histogram 'Minimum' value as the test result for $V_{IL(DC)}$.

8 Collect all $V_{IL(DC)}$.

9 Determine the worst result from the set of $V_{IL(DC)}$ measured.

Expected/Observable Results

- The histogram maximum value of the test signal within the sampling window (from signal tDS to tDH with reference to the DQS signal) must be within the specification limits.

SlewR on Setup Region

Test Overview

The purpose of this test is to calculate the rising slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation:

- Yes

Signal(s) of Interest

- Data Signals (supported by Data Strobe Signals)

Required Signals that are needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)

2 Take the first valid WRITE burst found.

3 Find all valid rising edges in the said burst. A valid rising edge starts at VIL (ac) crossing and end at following VIH (ac) crossing.

4 For all valid rising edges, find the transition time, delta TR which is time starts at VREF crossing and end at following VIH (ac) crossing. Then calculate Rising Slew.

$$\text{Rising Slew} = \frac{V_{IH(ac)}\ \text{min} - V_{REF}}{\text{delta TR}}$$

5 Determine the worst result from the set of SlewR measured.

Expected/Observable Results

- The calculated Rising Slew value for the test signal shall meet the user defined limit.

SlewF on Setup Region

Test Overview

The purpose of this test is to calculate the falling slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signals (supported by Data Strobe Signals)

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid falling edges in the said burst. A valid falling edge starts at VIH (ac) crossing and end at following VIL (ac) crossing.
4 For all valid falling edges, find the transition time, delta TF which is time starts at VREF crossing and end at following VIL (ac) crossing. Then calculate Falling Slew.

$$\text{Falling Slew} = \frac{V_{REF} - V_{IL(ac)}\ \text{max}}{\text{delta TF}}$$

5 Determine the worst result from the set of SlewF measured.

Expected/Observable Results

- The calculated Falling Slew value for the test signal shall meet the user defined limit.

SlewR on Hold Region

Test Overview

The purpose of this test is to calculate the rising slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signals (supported by Data Strobe Signals)

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid rising edges in the said burst. A valid rising edge starts at VIL (ac) crossing and end at following VIH (ac) crossing.

4 For all valid rising edges, find the transition time, delta TR which is time starts at VIL(DC) crossing and end at following VREF crossing. Then calculate Rising Slew.

$$Rising\ Slew = \frac{V_{REF} - V_{IL(DC)}}{\text{delta TR}}$$

5 Determine the worst result from the set of SlewR measured.

Expected/Observable Results

- The calculated Rising Slew value for the test signal shall meet the user defined limit.

SlewF on Hold Region

Test Overview

The purpose of this test is to calculate the falling slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

Mode Supported

DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signals (supported by Data Strobe Signals)

Required Signals that are needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)

2 Take the first valid WRITE burst found.

3 Find all valid falling edges in the said burst. A valid falling edge starts at VIH (ac) crossing and end at following VIL (ac) crossing.

4 For all valid falling edges, find the transition time, delta TF which is time starts at VIH(DC) crossing and end at following VREF crossing. Then calculate Falling Slew.

$$Falling\ Slew = \frac{V_{IH(DC)} - V_{REF}}{\text{delta TF}}$$

5 Determine the worst result from the set of SlewF measured.

Expected/Observable Results

- The calculated Falling Slew value for the test signal shall meet the user defined limit.

Write Cycle Timing Tests

tDS(base)

Test Overview

The purpose of this test is to verify that the time interval from the data (DQ rising/falling Edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC Specification.

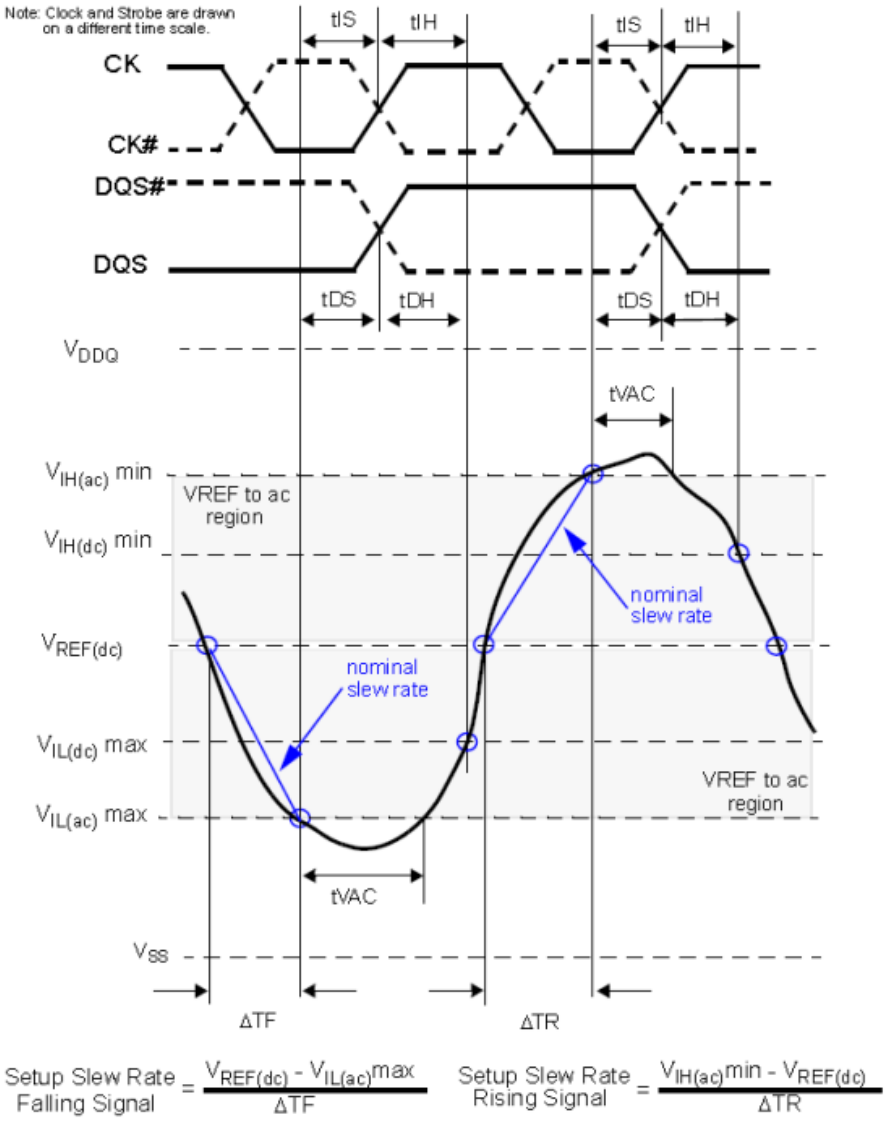


Figure 45 Nominal Slew Rate and t_{VAC} for Setup Time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope

- Data Signal, DQ
- Data Strobe Signal, (DQS as Supporting Signal). Use differential connection (DQS+ and DQS-)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 131 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Data setup time to DQS, DQS# referenced to Vih(ac), Vil(ac) levels	tDS(base) AC 175	75	-	25	-	-	-	-	-	ps
Data setup time to DQS, DQS# referenced to Vih(ac), Vil(ac) levels	tDS(base) AC 150	125	-	75	-	30	-	10	-	ps

Parameter	Symbol	DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	
Data setup time to DQS, DQS# referenced to VIH(AC)/ VIL(AC) levels	tDS(base) AC 150	TBD		TBD		ps
Data setup time to DQS, DQS# referenced to VIH(AC)/ VIL(AC) levels	tDS(base) AC 135	TBD		TBD		ps

Table 132 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Data setup time to DQS, DQS# referenced to Vih(ac), Vil(ac) levels	tDS(base) AC 160	90	-	40	-	-	-	-	-	ps
Data setup time to DQS, DQS# referenced to Vih(ac), Vil(ac) levels	tDS(base) AC 135	140	-	90	-	45	-	25	-	ps

Table 133 Data Setup and Hold Base-Values

[ps]	Data Rate		Reference
	1600	1333	
tDS(base)	75	100	VIH/L(AC) = VREF(DC) ± 150mV

Test References

- See *Figure 115 and Table 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010*,
- See *Table 6 in Section 4 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1, July 2010* and
- See *Figure 129 to 132 and Table 68 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split Read and Write bursts in the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross Vih(ac) in the said burst.
4 Find all valid falling DQ crossings that cross Vil(ac) in the same burst.
5 For all DQ crossings found, locate all next DQS crossings that cross 0V.
6 tDS is defined as the time between the DQ crossing and the DQS crossing.
7 Collect all tDS.
8 Find the worst tDS among the measured values and report the value as the test result.

Expected/Observable Results

- The worst measured tDS must be within the specification limit.

tDH(base)

Test Overview

The purpose of this test is to verify that the time interval from the data (DQ rising/falling edge) hold time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC Specification.

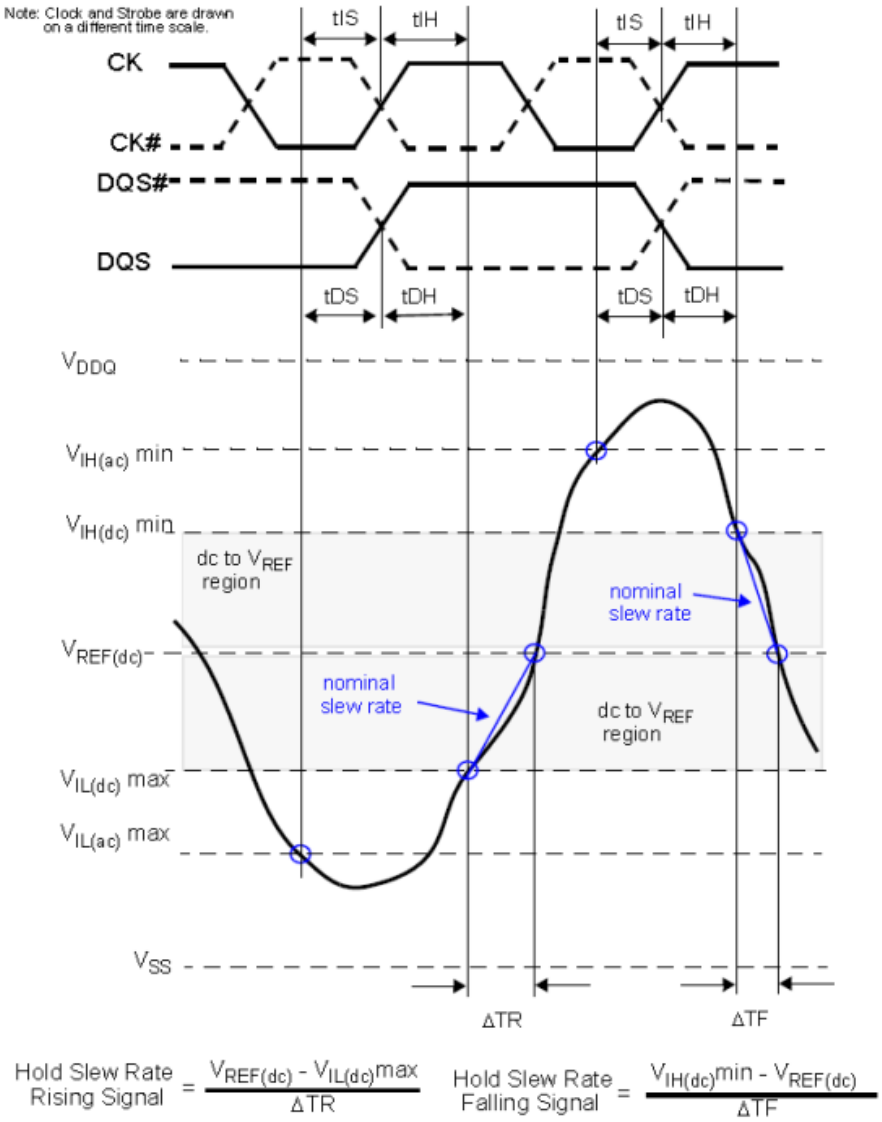


Figure 46 Nominal Slew Rate for Hold Time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock)

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal). Use differential connection (DQS+ and DQS-)

Optional signal required to separate the signals for the different Ranks

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 134 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Data setup time to DQS, DQS# referenced to VIH(DC)/ VIL(DC) levels	tDH(base) DC 100	150	-	100	-	65	-	45	-	ps

Parameter	Symbol	DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	
Data setup time to DQS, DQS# referenced to VIH(DC)/VIL(DC) levels	tDH(base) DC 100	TBD		TBD		ps

Table 135 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Data setup time to DQS, DQS# referenced to VIH(DC)/VIL(DC) levels	tDS(base) DC 90	160	-	110	-	75	-	55	-	ps

Table 136 Data Setup and Hold Base-Values

[ps]	Data Rate		Reference
	1600	1333	
tDH(base)	100	125	VIH/L(DC) = VREF(DC) ± 100mV

Test References

- See *Figure 116 and Table 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010*,
- See *Table 6 in Section 4 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1, July 2010* and
- See *Figure 129 to 132 and Table 68 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split Read and Write bursts in the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IL(DC)}$ in the said burst.
4 Find all valid falling DQ crossings that cross $V_{IH(DC)}$ in the same burst.
5 For all DQ crossings found, locate all next DQS crossings that cross 0V.
6 tDH is defined as the time between the DQ crossing and the DQS crossing.
7 Collect all tDH.
8 Find the worst tDH among the measured values and report the value as the test result.

Expected/Observable Results

- The worst measured tDH must be within the specification limit.

tDS-Diff(derate)

Test Overview

The purpose of this test is to verify that the time interval from data (DQ rising/falling edge) setup time to the associated DQS crossing edge must be within the conformance limit as specified in the JEDEC Specification.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope

- Data Signal (DQ) or Data Mask Signal (DM)
- Data Strobe Signal (DQS as Supporting Signal). Use differential connection (DQS+ and DQS-)

Optional signal required to separate the signals for the different Ranks

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 137 Data Setup and Hold Base-Values

Units (ps)	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Reference
tDS (base) AC 175	75	25	-	-	-	-	$V_{IH/L(AC)}$
tDS (base) AC 150	125	75	30	10	-	-	$V_{IH/L(AC)}$
tDS (base) AC 135	-	-	-	-	TBD	TBD	$V_{IH/L(AC)}$
tDH (base) DC 100	150	100	65	45	TBD	TBD	$V_{IH/L(DC)}$

Table 138 Derating Values DDR3-800/1066 tDS/DH - AC/DC based Alternate AC 175 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 175 Threshold -> VIH(AC) = VREF(DC) + 175 mV, VIL(AC) = VREF(DC) - 175 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	88	50	88	50	88	50	-	-
	1.5	59	34	59	34	59	34	67	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	-2	-4	-2	-4	6	4
	0.8	-	-	-	-	-6	-10	2	-2
	0.7	-	-	-	-	-	-	-3	-8
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 175 Threshold -> VIH(AC) = VREF(DC) + 175 mV, VIL(AC) = VREF(DC) - 175 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	14	12	22	20	-	-	-	-
	0.8	10	6	18	14	26	24	-	-
	0.7	5	0	13	8	21	18	29	34
	0.6	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-30	-26	-22	-10

NOTE 1. Empty cell contents are defined as not supported.

Table 139 Derating Values DDR3-800/1066/1333/1600 tDS/DH - AC/DC based Alternate AC 150 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	75	50	75	50	75	50	-	-
	1.5	50	34	50	34	50	34	58	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	0	-4	-0	-4	8	4
	0.8	-	-	-	-	-0	-10	8	-2
	0.7	-	-	-	-	-	-	8	-8
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	16	12	24	20	-	-	-	-
	0.8	16	6	24	14	32	24	-	-
	0.7	16	0	24	8	32	18	40	34
	0.6	-15	-10	23	-2	31	8	39	24
	0.5	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	7	-26	15	-10

NOTE 1. Empty cell contents are defined as not supported.

Table 140 Derating Values DDR3-1866/2133 tDS/DH - AC/DC based Alternate AC 135 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	68	50	68	50	68	50	-	-
	1.5	45	34	45	34	45	34	53	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	-2	-4	-2	-4	10	4
	0.8	-	-	-	-	3	-10	11	-2
	0.7	-	-	-	-	-	-	14	-8
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	18	12	26	20	-	-	-	-
	0.8	19	6	27	14	35	24	-	-
	0.7	22	0	30	8	38	18	46	34
	0.6	25	-10	33	-2	41	8	49	24
	0.5	-	-	29	-16	37	-6	45	10
	0.4	-	-	-	-	30	-26	38	-10

NOTE 1. Empty cell contents are defined as not supported.

Table 141 Data Setup and Hold Base-Values

Units (ps)	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Reference
tDS (base) AC 150	90	40	-	-	$V_{IH/L(AC)}$
tDS (base) AC 135	140	90	45	25	$V_{IH/L(AC)}$
tDH (base) DC 90	160	110	75	55	$V_{IH/L(DC)}$

Table 142 Derating Values DDR3-800/1066 tDS/DH - AC/DC based Alternate AC 160 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based AC 160 Threshold -> VIH(AC) = VREF(DC) + 160 mV, VIL(AC) = VREF(DC) - 160 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	80	45	80	45	80	45	-	-
	1.5	53	30	53	30	53	30	58	38
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	-1	-3	-1	-3	7	5
	0.8	-	-	-	-	-3	-8	5	1
	0.7	-	-	-	-	-	-	3	-5
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based AC 160 Threshold -> VIH(AC) = VREF(DC) + 160 mV, VIL(AC) = VREF(DC) - 160 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	15	13	23	21	-	-	-	-
	0.8	13	9	21	17	29	27	-	-
	0.7	11	3	19	11	27	21	35	37
	0.6	8	-4	16	4	24	14	32	30
	0.5	-	-	4	-6	12	4	20	20
	0.4	-	-	-	-	-8	-11	0	5

NOTE 1. Empty cell contents are defined as not supported.

Table 143 Derating Values DDR3-800/1066/1333/1600 tDS/DH - AC/DC based Alternate AC 135 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	68	45	68	45	68	45	-	-
	1.5	45	30	45	30	45	30	53	38
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	2	-3	2	-3	10	5
	0.8	-	-	-	-	3	-8	11	1
	0.7	-	-	-	-	-	-	14	-5
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	18	13	26	21	-	-	-	-
	0.8	19	9	27	17	35	27	-	-
	0.7	22	3	30	11	38	21	46	37
	0.6	25	-4	33	4	41	14	49	30
	0.5	-	-	29	-6	37	4	45	20
	0.4	-	-	-	-	30	-11	38	5

NOTE 1. Empty cell contents are defined as not supported.

Table 144 Data Setup and Hold Base-Values

[ps]	Data Rate		Reference
	1600	1333	
tDS(base)	75	100	VIH/L(AC) = VREF(DC) ± 150mV

Table 145 Derating Values LPDDR3 tDS/DH - AC/DC based AC 150

ΔtDS, ΔtDH derating in [ps] AC/DC based AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV DC 100 Threshold -> VIH(DC) = VREF(DC) + 100 mV, VIL(DC) = VREF(DC) - 100 mV									
		DQS_t, DQS_c Differential Slew Rate							
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ, DM Slew Rate V/ns	4.0	38	25	38	25	38	25	-	-
	3.5	32	21	32	21	32	21	32	21
	3.0	25	17	25	17	25	17	25	17
	2.5	-	-	15	10	15	10	15	10
	2.0	-	-	-	-	0	0	0	0
	1.5	-	-	-	-	-	-	-25	-17
	1.0	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV DC 100 Threshold -> VIH(DC) = VREF(DC) + 100 mV, VIL(DC) = VREF(DC) - 100 mV							
		DQS_t, DQS_c Differential Slew Rate					
		4.0V/ns		3.0V/ns		2.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ, DM Slew Rate V/ns	4.0	-	-	-	-	-	-
	3.5	-	-	-	-	-	-
	3.0	25	17	-	-	-	-
	2.5	15	10	15	10	-	-
	2.0	0	0	0	0	0	0
	1.5	-25	-17	-25	-17	-25	-17
	1.0	-75	-50	-75	-50	-75	-50

NOTE 1. Empty cell contents are defined as not supported.

Test References

- See *Figure 115 & 117 and Table 76, to 79 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010,*
- See *Table 11, 12 & 13 in Section 4 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1July 2010* and
- See *Figure 129 to 132 and Table 68 & 69 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

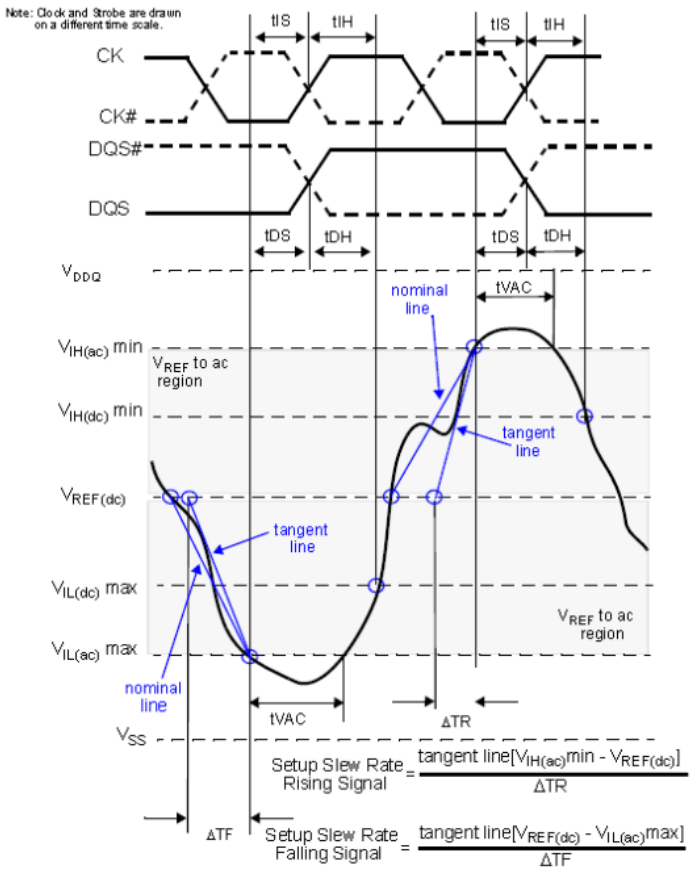


Figure 47 Tangent Line for Setup Time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

Measurement Algorithm

1 Acquire and split Read and Write bursts in the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross VIH(AC) in the said burst.
4 Find all valid falling DQ crossings that cross VIL(AC) in the same burst.
5 For all DQ crossings found, locate all next DQS crossings that cross 0V.
6 tDS is defined as the time between the DQ crossing and the DQS crossing.
7 Collect all tDS.
8 Find the worst tDS among the measured values and report the value as the test result.
9 Measure the mean slew rate for all the DQ and DQS edges.
10 Use the mean slew rate for DQ and DQS to determine the ΔtDS derating value based on the derating tables.
11 The test limit for tDS test = tDS(base) + ΔtDS.

Expected/Observable Results

- The worst measured tDS must be within the specification limit.

tDH-Diff(derate)

Test Overview

The purpose of this test is to verify that the time interval from data (DQ rising/falling edge) hold time to the associated DQS crossing edge must be within the conformance limit as specified in the JEDEC Specification.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signal (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal). Use differential connection (DQS+ and DQS-)

Optional signal required to separate the signals for the different Ranks

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 146 Data Setup and Hold Base-Values

Units (ps)	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Reference
tDS (base) AC 175	75	25	-	-	-	-	$V_{IH/L(AC)}$
tDS (base) AC 150	125	75	30	10	-	-	$V_{IH/L(AC)}$
tDS (base) AC 135	-	-	-	-	TBD	TBD	$V_{IH/L(AC)}$
tDH (base) DC 100	150	100	65	45	TBD	TBD	$V_{IH/L(DC)}$

Table 147 Derating Values DDR3-800/1066 tDS/DH - AC/DC based Alternate AC 175 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 175 Threshold -> VIH(AC) = VREF(DC) + 175 mV, VIL(AC) = VREF(DC) - 175 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	88	50	88	50	88	50	-	-
	1.5	59	34	59	34	59	34	67	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	-2	-4	-2	-4	6	4
	0.8	-	-	-	-	-6	-10	2	-2
	0.7	-	-	-	-	-	-	-3	-8
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 175 Threshold -> VIH(AC) = VREF(DC) + 175 mV, VIL(AC) = VREF(DC) - 175 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	14	12	22	20	-	-	-	-
	0.8	10	6	18	14	26	24	-	-
	0.7	5	0	13	8	21	18	29	34
	0.6	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-30	-26	-22	-10

NOTE 1. Empty cell contents are defined as not supported.

Table 148 Derating Values DDR3-800/1066/1333/1600 tDS/DH - AC/DC based Alternate AC 150 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	75	50	75	50	75	50	-	-
	1.5	50	34	50	34	50	34	58	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	0	-4	-0	-4	8	4
	0.8	-	-	-	-	-0	-10	8	-2
	0.7	-	-	-	-	-	-	8	-8
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	16	12	24	20	-	-	-	-
	0.8	16	6	24	14	32	24	-	-
	0.7	16	0	24	8	32	18	40	34
	0.6	-15	-10	23	-2	31	8	39	24
	0.5	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	7	-26	15	-10

NOTE 1. Empty cell contents are defined as not supported.

Table 149 Derating Values DDR3-1866/2133 tDS/DH - AC/DC based Alternate AC 135 Threshold

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	68	50	68	50	68	50	-	-
	1.5	45	34	45	34	45	34	53	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	-2	-4	-2	-4	10	4
	0.8	-	-	-	-	3	-10	11	-2
	0.7	-	-	-	-	-	-	14	-8
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	18	12	26	20	-	-	-	-
	0.8	19	6	27	14	35	24	-	-
	0.7	22	0	30	8	38	18	46	34
	0.6	25	-10	33	-2	41	8	49	24
	0.5	-	-	29	-16	37	-6	45	10
	0.4	-	-	-	-	30	-26	38	-10

NOTE 1. Empty cell contents are defined as not supported.

Table 150 Data Setup and Hold Base-Values

Units (ps)	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Reference
tDS (base) AC 150	90	40	-	-	$V_{IH/L(AC)}$
tDS (base) AC 135	140	90	45	25	$V_{IH/L(AC)}$
tDH (base) DC 90	160	110	75	55	$V_{IH/L(DC)}$

Table 151 Derating Values DDR3-800/1066 tDS/DH - AC/DC based Alternate AC 160 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based AC 160 Threshold -> VIH(AC) = VREF(DC) + 160 mV, VIL(AC) = VREF(DC) - 160 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	80	45	80	45	80	45	-	-
	1.5	53	30	53	30	53	30	58	38
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	-1	-3	-1	-3	7	5
	0.8	-	-	-	-	-3	-8	5	1
	0.7	-	-	-	-	-	-	3	-5
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based AC 160 Threshold -> VIH(AC) = VREF(DC) + 160 mV, VIL(AC) = VREF(DC) - 160 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	15	13	23	21	-	-	-	-
	0.8	13	9	21	17	29	27	-	-
	0.7	11	3	19	11	27	21	35	37
	0.6	8	-4	16	4	24	14	32	30
	0.5	-	-	4	-6	12	4	20	20
	0.4	-	-	-	-	-8	-11	0	5

NOTE 1. Empty cell contents are defined as not supported.

Table 152 Derating Values DDR3-800/1066/1333/1600 tDS/DH - AC/DC based Alternate AC 135 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	68	45	68	45	68	45	-	-
	1.5	45	30	45	30	45	30	53	38
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	2	-3	2	-3	10	5
	0.8	-	-	-	-	3	-8	11	1
	0.7	-	-	-	-	-	-	14	-5
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	18	13	26	21	-	-	-	-
	0.8	19	9	27	17	35	27	-	-
	0.7	22	3	30	11	38	21	46	37
	0.6	25	-4	33	4	41	14	49	30
	0.5	-	-	29	-6	37	4	45	20
	0.4	-	-	-	-	30	-11	38	5

NOTE 1. Empty cell contents are defined as not supported.

Table 153 Data Setup and Hold Base-Values

[ps]	Data Rate		Reference
	1600	1333	
tDH(base)	100	125	VIH/L(DC) = VREF(DC) ± 100mV

Table 154 Derating Values LPDDR3 tDS/DH - AC/DC based AC 150

ΔtDS, ΔtDH derating in [ps] AC/DC based AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV DC 100 Threshold -> VIH(DC) = VREF(DC) + 100 mV, VIL(DC) = VREF(DC) - 100 mV									
		DQS_t, DQS_c Differential Slew Rate							
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ, DM Slew Rate V/ns	4.0	38	25	38	25	38	25	-	-
	3.5	32	21	32	21	32	21	32	21
	3.0	25	17	25	17	25	17	25	17
	2.5	-	-	15	10	15	10	15	10
	2.0	-	-	-	-	0	0	0	0
	1.5	-	-	-	-	-	-	-25	-17
	1.0	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV DC 100 Threshold -> VIH(DC) = VREF(DC) + 100 mV, VIL(DC) = VREF(DC) - 100 mV							
		DQS_t, DQS_c Differential Slew Rate					
		4.0V/ns		3.0V/ns		2.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ, DM Slew Rate V/ns	4.0	-	-	-	-	-	-
	3.5	-	-	-	-	-	-
	3.0	25	17	-	-	-	-
	2.5	15	10	15	10	-	-
	2.0	0	0	0	0	0	0
	1.5	-25	-17	-25	-17	-25	-17
	1.0	-75	-50	-75	-50	-75	-50

NOTE 1. Empty cell contents are defined as not supported.

Test References

- See *Figure 116 & 118* and *Table 76, 77, 78 & 79 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010,*
- See *Table 11,12 & 13 in Section 4 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010* and
- See *Figure 129,130, 131 & 132* and *Table 68 & 69 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

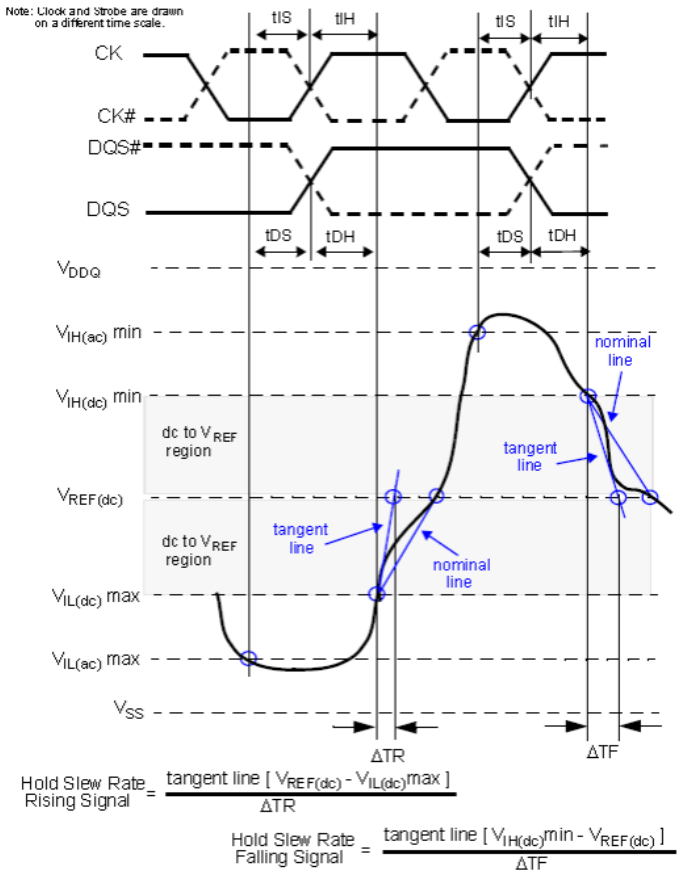


Figure 48 Tangent Line for Hold Time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock)

Measurement Algorithm

1 Acquire and split Read and Write bursts in the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IL(DC)}$ in the said burst.
4 Find all valid falling DQ crossings that cross $V_{IH(DC)}$ in the same burst.
5 For all DQ crossings found, locate all next DQS crossings that cross 0V.
6 tDH is defined as the time between the DQ crossing and the DQS crossing.
7 Collect all tDH.
8 Find the worst tDH among the measured values and report the value as the test result.
9 Measure the mean slew rate for all the DQ and DQS edges.
10 Use the mean slew rate for DQ and DQS to determine the ΔtDH derating value based on the derating tables.
11 The test limit for tDH test = tDH(base) + ΔtDH.

Expected/Observable Results

- The worst measured tDH must be within the specification limit.

tDIPW

Test Overview

The purpose of this test is to verify that the width of the high or low level data signal is within the conformance limit as specified in the *JEDEC specification*.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope

- Data Signal (DQ)
- Data Strobe Signal (DQS; must use a differential DQS connection)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Table 155 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
DQ and DM Input pulse width for each input	tDIPW	600	-	490	-	400	-	ps

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	
DQ and DM Input pulse width for each input	tDIPW	360	-	320	-	280	-	ps

Table 156 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
DQ and DM input pulse width	tDIPW	MIN	0.35		tCK(avg)

Test References

- See *Tables 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010* and
- See *Table 64 in Section 11 of the DDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split Read and Write bursts in the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising and falling DQ crossings at V_{REF} in the said burst.
4 tDIPW is the time starting from a rising/falling edge of the DQ and ending at the following falling/rising (the following edge must not be in the same direction) edge.
5 Collect all tDIPW.
6 Determine the worst result from the set of tDIPW measured.

Expected/Observable Results

- The worst measured tDIPW must be within the specification limit.

tVAC(Data)

Test Overview

The purpose of this test is to verify that the time of the data signal above $V_{IH(AC)}$ and below $V_{IL(AC)}$ must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope

- Data Signal (DQ)
- Data Strobe Signal (DQS)

Optional signal required to separate the DQS signals from different ranks of memory

- Chip Select Signal)

Test References

- See *Figures 110, 111 & 112 in Section 13 of the DDR3 and SDRAM Specification in the JESD79-3F, July 2012.*

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising and falling DQ crossings at the $V_{IH(AC)}$ and $V_{IL(AC)}$ levels in the said burst.
4. tVAC (Data) is the time starting from a DQ rising $V_{IH(AC)}$ cross point and ending at the following DQ falling $V_{IH(AC)}$ cross point.
5. tVAC (Data) is the time starting from a DQ falling $V_{IL(AC)}$ cross point and ending at the following DQ rising $V_{IL(AC)}$ cross point.
6. Collect all tVAC (Data).
7. Determine the worst result from the set of tVAC (Data) measured.
8. Report the value of the worst tVAC (Data). No compliance limit checking is performed for this test.

Expected/Observable Results

- The worst measured tVAC (Data) value must be within the specification limit.

Read Cycle Electrical Tests

VOH(AC)

Test Overview

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window is greater than the conformance limits of the $V_{OH(AC)}$ value specified in the JEDEC specification.

The value of V_{TT} which directly affects the conformance lower limit is defaulted to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. User may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{TT}.

The value of V_{DDQ} which directly affects the conformance lower limit is defaulted to 1.50V for typical DDR3, 1.35V for DDR3L and 1.2V for LPDDR3. User may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DDQ}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signals (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test, PUT = Data Signals
- Supporting Pin = Data Strobe Signals

Test Definition Notes from the Specification

Table 157 Single-Ended AC and DC Output Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600	Units	Notes
$V_{OH(AC)}$	AC output logic high measurement level (for output SR)	V_{TT} + 0.1 x V_{DDQ}	V	1[a]

a: Refers to Note 1 in Table 30 of the *JEDEC Standard JESD79-3E*. The swing of ± 0.1 x V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to $V_{TT} = V_{DDQ}/2$.

Table 158 Single-Ended AC and DC Output Levels

Symbol	Parameter	Value	Unit	Notes
$V_{OH(AC)}$	AC output logic high measurement level (output slew rate)	V_{REFDQ} + 0.12	V	-

Test References

- See *Table 30 in Section 9.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Table 43 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid positive pulses. A valid positive pulse starts at V_{REF} crossing at valid rising edge and ends at V_{REF} crossing at the following valid falling edge.

4 Zoom in on the first valid positive pulse and perform V_{TOP} measurement. Take the V_{TOP} measurement result as $V_{OH(AC)}$ value.

5 Continue the previous step with the rest of the valid positive pulses that were found in the burst.

6 Determine the worst result from the set of $V_{OH(AC)}$ measured.

Expected/Observable Results

- The high level voltage value of the test signal must be greater than or equal to the $V_{OH(AC)}$ value in the specification.

VOH(DC)

Test Overview

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window is greater than the conformance limits of the $V_{OH(DC)}$ value specified in the JEDEC specification.

The value of V_{DDQ} which directly affects the conformance upper limit is defaulted to 1.50V for typical DDR3, 1.35V for DDR3L and 1.2V for LPDDR3. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customize test limit set based on different values of V_{DDQ}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signals (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test, PUT = Data Signals
- Supporting Pin = Data Strobe Signals

Test Definition Notes from the Specification

Table 159 Single-Ended AC and DC Output Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600	Units
$V_{OH(DC)}$	DC output logic high measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V

Table 160 Single-Ended AC and DC Output Levels

Symbol	Parameter	Value	Unit	Notes
$V_{OH(DC)}$	DC output logic high measurement level (for IV curve linearity)	0.9 X V_{DDQ}	V	1[a]

a: Refers to Note 1 in Table 30 of the *JEDEC Standard JESD209-3*. I_{OH} = -0.1mA.

Test References

- See *Table 30 in Section 9.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Table 43 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid positive pulses. A valid positive pulse starts at V_{REF} crossing at valid rising edge and ends at V_{REF} crossing at the following valid falling edge.
4 Zoom in on the first valid positive pulse and perform V_{TOP} measurement. Take the V_{TOP} measurement result as $V_{OH(DC)}$ value.
5 Continue the previous step with the rest of the valid positive pulses that were found in the burst.
6 Determine the worst result from the set of $V_{OH(DC)}$ measured.

Expected/Observable Results

- The high level voltage value of the test signal must be greater than or equal to the $V_{OH(DC)}$ value in the specification.

VOL(AC)

Test Overview

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window is lower than the conformance lower limits of the $V_{OL(AC)}$ value specified in the JEDEC specification.

The value of V_{TT} which directly affects the conformance lower limit is defaulted to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. Users may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{TT}.

The value of V_{DDQ} which directly affects the conformance lower limit is defaulted to 1.50V for typical DDR3, 1.35V for DDR3L and 1.2V for LPDDR3. Users may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DDQ}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signals (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test, PUT = Data Signals
- Supporting Pin = Data Strobe Signals

Test Definition Notes from the Specification

Table 161 Single-Ended AC and DC Output Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600	Units	Notes
$V_{OL(AC)}$	AC output low measurement level (for output slew rate)	V_{TT} - 0.1 x V_{DDQ}	V	1[a]

a: Refers to Note 1 in Table 30 of the *JEDEC Standard JESD79-3E*. The swing of ± 0.1 x V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to $V_{TT} = V_{DDQ}/2$.

Table 162 Single-Ended AC and DC Output Levels

Symbol	Parameter	Value	Unit	Notes
$V_{OL(AC)}$	AC output logic low measurement level (for output slew rate)	V_{REFDQ} - 0.12	V	-

Test References

- See *Table 30 in Section 9.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Table 43 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid negative pulses. A valid negative pulse starts at V_{REF} crossing at valid falling edge and ends at V_{REF} crossing at the following valid rising edge.

4 Zoom in on the first valid negative pulse and perform V_{BASE} measurement. Take the V_{BASE} measurement result as $V_{OL(AC)}$ value.

5 Continue the previous step with the rest of the valid negative pulses that were found in the burst.

6 Determine the worst result from the set of $V_{OL(AC)}$ measured.

Expected/Observable Results

- The low level voltage value of the test signal must be lower than or equal to the minimum $V_{OL(AC)}$ value.

VOL(DC)

Test Overview

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window is lower than the conformance lower limits of the $V_{OL(DC)}$ value specified in the JEDEC specification.

The value of V_{DDQ} which directly affects the conformance lower limit is defaulted to 1.50V for typical DDR3, 1.35V for DDR3L and 1.2V for LPDDR3. Users may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customize test limit set based on different values of V_{DDQ}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signals (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test, PUT = Data Signals
- Supporting Pin = Data Strobe Signals

Test Definition Notes from the Specification

Table 163 Single-Ended AC and DC Output Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600	Units
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.2 x V_{DDQ}	V

Table 164 Single-Ended AC and DCput Levels

Symbol	Parameter	Value	Unit	Notes
$V_{OL(DC)}$ (ODT disabled)	DC output logic low measurement level (for output slew rate)	0.1 x V_{DDQ}	V	2[a]

a: Refers to Note 2 in Table 42 of the *JEDEC Standard JESD209-3*. I_{OL} = 0.1mA.

Test References

- See T*able 30 in Section 9.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Table 43 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid negative pulses. A valid negative pulse starts at V_{REF} crossing at valid falling edge and ends at V_{REF} crossing at the following valid rising edge.
4 Zoom in on the first valid negative pulse and perform V_{BASE} measurement. Take the V_{BASE} measurement result as $V_{OL(DC)}$ value.
5 Continue the previous step with the rest of the valid negative pulses that were found in the burst.
6 Determine the worst result from the set of $V_{OL(DC)}$ measured.

Expected/Observable Results

- The low level voltage value of the test signal must be lower than or equal to the minimum $V_{OL(DC)}$ value.

SRQseR

Test Overview

The purpose of this test is to verify that the rising slew rate value of the test signal is within the conformance limit of the SRQser value specified in the JEDEC specification.

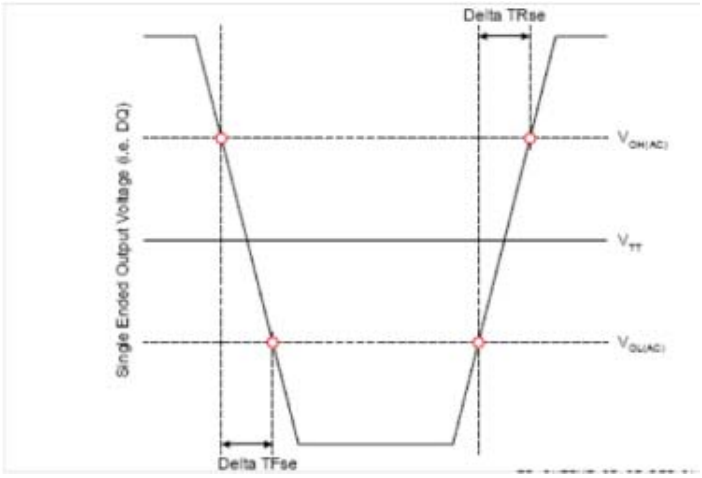


Figure 49 SRQseR

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signals (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test, PUT = Data Signals
- Supporting Pin = Data Strobe Signals)

Test Definition Notes from the Specification

Table 165 Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$\frac{V_{OH(AC)}-V_{OL(AC)}}{\Delta TRse}$

Table 166 Output Slew Rate (Single-Ended))

Parameters	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	2.5	5	2.5	5	2.5	5	TBD	5	2.5	5	2.5	5	V/ns

Table 167 Output Slew Rate (Single-ended)

Parameter	Symbol	Value		Units
		Min	Max	
Single-ended Output Slew Rate (RON = 40W ± 30%)	SRQse	2	4.0	V/ns

Test References

- *See Figure 96 and Table 32 & 33 in Section 9 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010 and*
- *See Figure 128 and Table 46 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid rising edges in the said burst. A valid rising edge starts at $V_{OL\ (AC)}$ crossing and end at following $V_{OH\ (AC)}$ crossing.

4 For all valid rising edges, find the transition time, ΔTR which is time starts at $V_{OL\ (AC)}$ crossing and end at following $V_{OH\ (AC)}$crossing. Then calculate SRQseR.

$$SRQseR = \frac{V_{OH(AC)} - V_{OL(AC)}}{TR}$$

5 Determine the worst result from the set of SRQseR measured.

Expected/Observable Results

- The calculated Rising Slew/SRQseR value for the test signal must be within the specification limit.

SRQseF

Test Overview

The purpose of this test is to verify that the falling slew rate value of the test signal is within the conformance limit of the SRQseF value specified in the JEDEC specification.

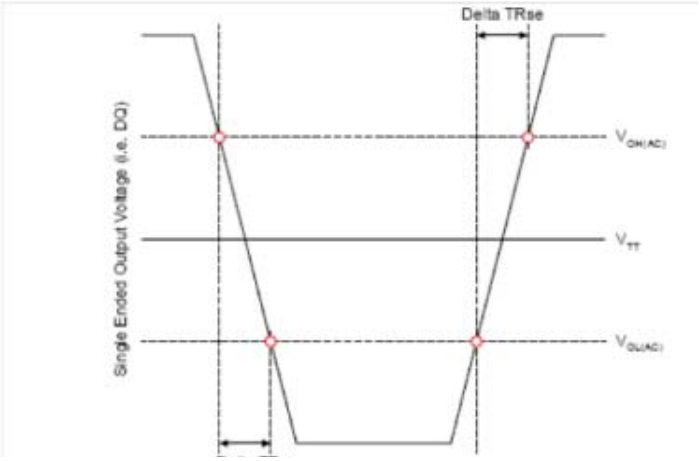


Figure 50 SRQseF

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signals (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope

- Pin Under Test, PUT = Data Signals
- Supporting Pin = Data Strobe Signals

Test Definition Notes from the Specification

Table 168 Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$\frac{V_{OH(AC)}-V_{OL(AC)}}{\Delta TFse}$

Table 169 Output Slew Rate (Single-Ended))

Parameters	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	2.5	5	2.5	5	2.5	5	TBD	5	2.5	5	2.5	5	V/ns

Table 170 Output Slew Rate (Single-ended)

Parameter	Symbol	Value		Units
		Min	Max	
Single-ended Output Slew Rate (RON = 40W ± 30%)	SRQse	2	4.0	V/ns

Test References

- *See Figure 96 and Table 32 & 33 in Section 9 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010 and*
- *See Figure 128 and Table 46 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid falling edges in the said burst. A valid falling edge starts at $V_{OH\ (AC)}$ crossing and end at following $V_{OL\ (AC)}$ crossing.

4 For all valid falling edges, find the transition time, ΔTR which is time starts at $V_{OH\ (AC)}$ crossing and end at following $V_{OL\ (AC)}$crossing. Then calculate SRQseF.

$$SRQseF = \frac{V_{OH(AC)} - V_{OL(AC)}}{TR}$$

5 Determine the worst result from the set of SRQseF measured.

Expected/Observable Results

- The calculated Falling Slew/SRQseF value for the test signal must be within the specification limits.

Read Cycle Timing Tests

tHZ(DQ)

Test Overview

tHZ(DQ) Test – DQ out high-impedance time from CK#/CL
The purpose of this test is to verify that the time when the DQ is no longer driving (from high state OR low state to the high impedance state), to the clock signal crossing, is within the conformance limits as specified in the JEDEC Specification.

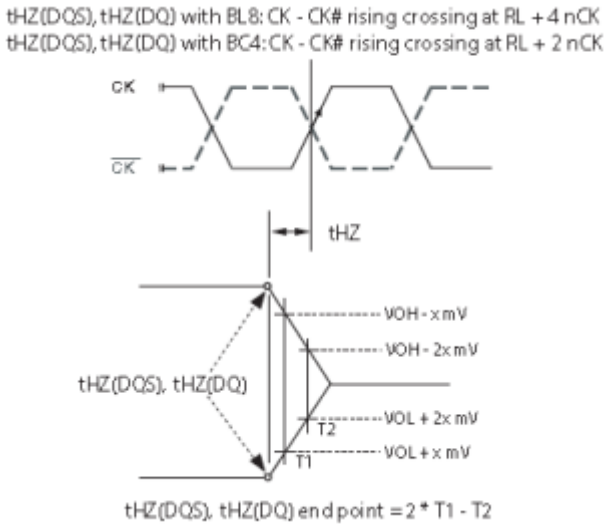


Figure 51 DQ Out High Impedance Time From CK/CK#

Modes Supported

- DDR3 and DDR3L [For LPDDR3, refer to the tHZ(DQ) (Low Power) test]

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signal (supported by Data Strobe Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 171 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
DQ high impedance time from CK/$\overline{CK}$	tHZ(DQ)	-	400	-	300	-	250	ps

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	
DQ high impedance time from CK/$\overline{CK}$	tHZ(DQ)	-	225	-	195	-	180	ps

Test References

- *See Figure 30 and Table 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010.*

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid READ burst found.
3. Find tHZEndPoint of the said burst.
4. Find the nearest Clock rising crossing.
5. tHZ(DQ) is the time interval between the found Clock rising edge's crossing point and the tHZEndPoint.
6. Report tHZ(DQ).

Expected/Observable Results

- The measured tHZ(DQ) must be within the specification limit.

NOTE Some designs do not have tristate at V_{REF} (for example, 0.9V). This test is not guaranteed when this scenario happens, as there is no significant point of where the driver has been turned-off.

tLZ(DQ)

Test Overview

tLZ(DQ) Test – DQ low-impedance time from CK#/CK
The purpose of this test is to verify that the time when the DQ starts driving (from high impedance state to high/low state), to the clock signal crossing, is within the conformance limit as specified in the JEDEC Specification.

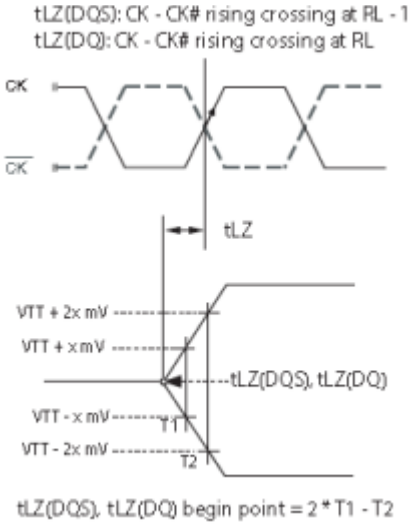


Figure 52 DQ Low-Impedance Time from CK/CK#

Modes Supported

- DDR3 and DDR3L [for LPDDR3, refer to the tLZ(DQ) (Low Power) test]

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signal (supported by Data Strobe Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 172 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
DQ low impedance time from CK/CK#	tLZ(DQ)	-800	400	-600	300	-500	250	ps

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	
DQ low impedance time from CK/CK#	tLZ(DQ)	-450	225	-390	195	-390	180	ps

Test References

- *See Figure 30 and Table 68 & 69 in Section 13 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010.*

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid READ burst found.
3. Find tLZBeginPoint of the said burst.
4. Find the nearest Clock rising crossing.
5. tLZ(DQ) is the time interval between the found Clock rising edge's crossing point and the tLZBeginPoint.
6. Report tLZ(DQ).

Expected/Observable Results

- The measured tLZ(DQ) must be within the specification limit.

tHZ(DQ) for Low Power

Test Overview

tHZ(DQ) Test (Low Power) - DQ high-Z from clock.
The purpose of this test is to verify that the time when DQ no longer driving (*from High state OR Low state to the High-impedance state) to the reference clock signal crossing must be within the conformance limit as specified in the JEDEC specification

Modes Supported

- LPDDR3, [for DDR3 and DDR3L, refer to the tHZ(DQ) test]

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signal (supported by Data Strobe Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 173 Timing Parameters by Speed Bin

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
DQ High-Z from Clock	tHZ(DQ)	MAX	tDQSCK (MAX) +(1.4 x tDQSQ (MAX))		ps

Test References

- *See Figure 119 & 120 and Table 64 in Section 11 of the DDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)
2 Take the first valid READ burst found.
3 Find tHZEndPoint of the said burst. (See notes on Find tHZEndPoint (DQ))

4 Find RL Clock Edge (tDQSCK clock edge reference);
   i Find all DQS middle rising cross point in the said burst.(See notes on threshold).
   ii Find first DQS rising edge by search the earliest rising cross point among all found DQS middle cross point.
   iii Find the closest Clock - DQS : the Clock middle cross point that closest to first DQS rising edge.
   iv Find RL Clock Edge (tDQSCK clock edge reference) which clock middle crosspoint that before closest Clock – DQS at tDQSCK Delay (cycle). By default, tDQSCK Delay is three cycle. In example, for tDQSCK Delay = 3, tDQSCK clock point is clock middle crosspoint that three clock before closest Clock – DQS . For tDQSCK Delay = 5, tDQSCK clock point is clock middle crosspoint that five clock before closest Clock – DQS . tDQSCK Delay is configurable in configuration page.
5 Define BL (Bit Length) = the number of DQS middle cross point.
6 Find “RL+BL/2” Clock Edge: Clock middle rising cross point that BL/2 cycle after RL Clock Edge.
7 Compare Data tHZ end point to “RL+BL/2” Clock Edge point as test result. Mathematically: test result= Data tHZ end point - “RL+BL/2” Clock Edge point.
8 Display the test result by spot to measurement location on waveform and locate the marker to Data tHZ end point and Clock middle cross point of test result.
9 Compare test result to compliance test limit.

Expected/Observable Results

- The measured tHZ(DQ) must be within the specification limit.

tLZ(DQ) for Low Power

Test Overview

tLZ(DQ) Test (Low Power) – DQ low-Z from clock

The purpose of this test is to verify that the time when the DQ starts driving (from high impedance state to high/low state), to the clock signal crossing, is within the conformance limit as specified in the JEDEC Specification.

Modes Supported

- LPDDR3 [for DDR3 and DDR3L refer to the tLZ(DQ) test]

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signal (supported by Data Strobe Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 174 Timing Parameters by Speed Bin

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
DQ Low-Z from Clock	tLZ(DQ)	MIN	tDQSCK (MIN) -300		ps

Test References

- *See Figure 119 & 120 and Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3, December 2011.*

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)

2 Take the first valid READ burst found.

3 Find Data tLZ begin point of the said burst. (See notes on Find tLZBeginPoint (DQ))

4 Find RL Clock Edge (tDQSCK clock edge reference);

   i Find all DQS middle rising cross point in the said burst.(See notes on threshold).

   ii Find first DQS rising edge by search the earliest rising cross point among all found DQS middle cross point.

   iii Find the closest Clock - DQS : the Clock middle cross point that closest to first DQS rising edge.

   iv Find RL Clock Edge (tDQSCK clock edge reference) which clock middle crosspoint that before closest Clock – DQS at tDQSCK Delay (cycle). By default, tDQSCK Delay is three cycle. In example, for tDQSCK Delay = 3, tDQSCK clock point is clock middle crosspoint that three clock before closest Clock – DQS . For tDQSCK Delay = 5, tDQSCK clock point is clock middle crosspoint that five clock before closest Clock – DQS . tDQSCK Delay is configurable in configuration page.

5 Compare Data tLZ begin point to RL Clock Edge point as test result. Mathematically: test result= Data tLZ begin point – RL Clock Edge point.

6 Display the test result by spot to measurement location on waveform and locate the marker to Data tLZ begin point and Clock middle cross point of test result.

7 Compare test result to compliance test limit.

Expected/Observable Results

- The measured tLZ(DQ) must be within the specification limit.

tDQSQ

Test Overview

The purpose of this test is to verify that the time interval from the data strobe output (DQS rising and falling edge) access time to the associated data (DQ rising and falling) signal is within the conformance limit as specified in the *JEDEC Standard*.

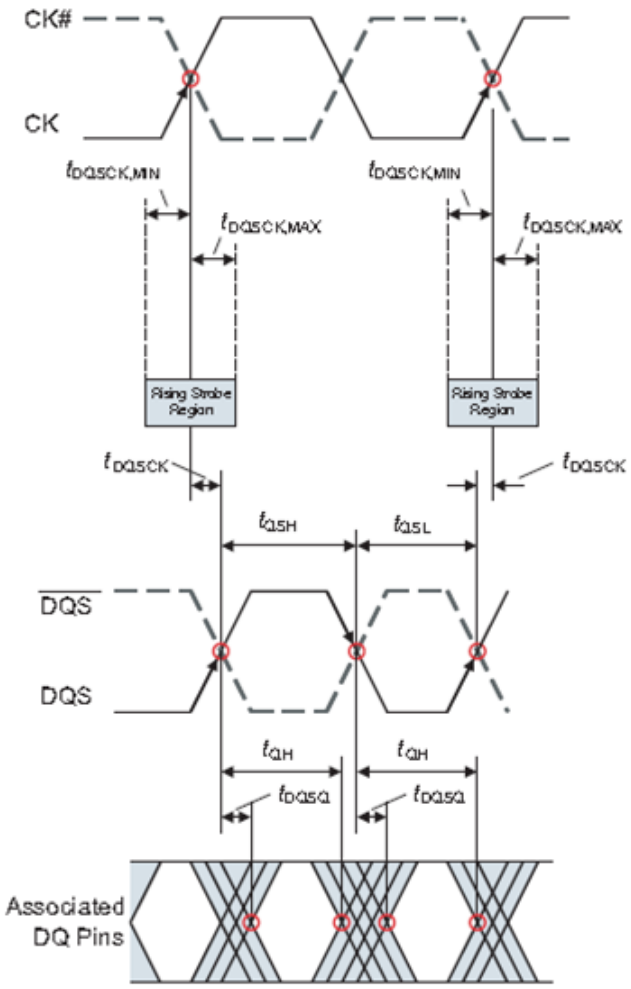


Figure 53 DQS-DQ Skew for DQS and Associated DQ Signals

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)

Optional signal required to separate the signals for the different Ranks

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 175 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	200	-	150	-	125	ps

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	100	-	85	-	75	ps

Table 176 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Units
			1333	1600	
DQS-DQ skew	tDQSQ	MAX	165	135	ps

Test References

- *See Figure 27 and Table 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010 and*
- *See Figure 119 and Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid rising and falling DQ crossings at V_{REF} in the said burst.
4. For all DQ crossings found, locate the nearest DQS crossing (rising and falling).
5. Take the time difference between the DQ crossing and DQS crossing as the tDQSQ.
6. Determine the worst result from the set of tDQSQ measured.

Expected/Observable Results

- The worst measured tDQSQ must be within the specification limit.

tQH

Test Overview

The purpose of this test is to verify that the time interval from the data output hold time (DQS rising and falling edge) from the DQS (rising and falling edge) is within the conformance limit as specified in the JEDEC Specification.

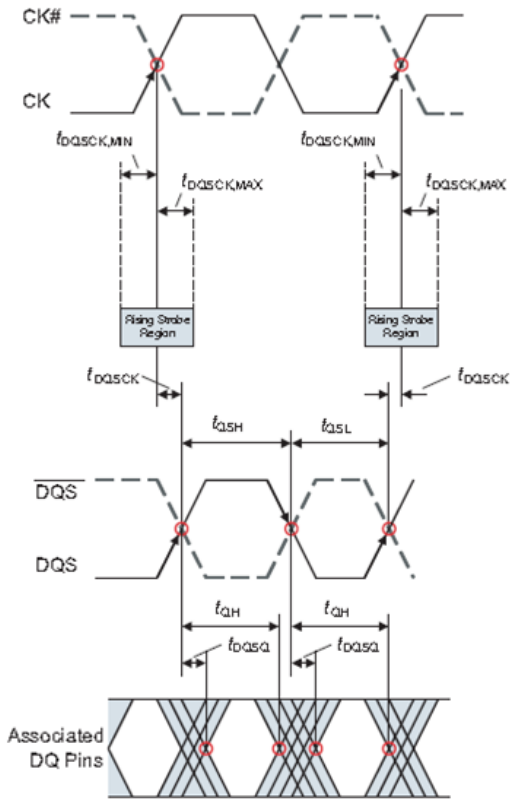


Figure 54 DQ/DQS Output Hold Time From DQS

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 177 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	0.38	-	tCK(avg)

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	0.38	-	tCK(avg)

Table 178 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
DQ/DQS output hold time from DQS	tQH	MIN	MIN (tQSH, tQSL)		ps

Test References

- *See Figure 27 and Table 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- *See Figure 119 and Table 64 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Acquire and split Read and Write bursts in the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQ crossings at V_{REF} in the said burst.
4 For all DQ crossings found, locate the nearest DQS rising crossing.
5 Using the found DQS rising crossing, locate the DQS rising crossing prior.
6 Take the time difference between the DQ crossing and DQS crossing as the tQH.
7 Determine the worst result from the set of tQH measured.

Expected/Observable Results

- The measured time interval between the data output hold time and the associated data strobe signal must be within specification limit.

Electrical Overshoot/Undershoot Tests

Overshoot Amplitude/Area (Data)

Test Overview

The purpose of this test is to verify that the overshoot value of the test signal found from all regions of the acquired waveform is lower than or equal to the conformance limit of the maximum peak amplitude allowed for overshoot as specified in the JEDEC specification.

When there is an overshoot, the area is calculated based on the overshoot width and overshoot amplitude. The Overshoot area should be lower than or equal to the conformance limit of the maximum overshoot area allowed as specified in the JEDEC specification.

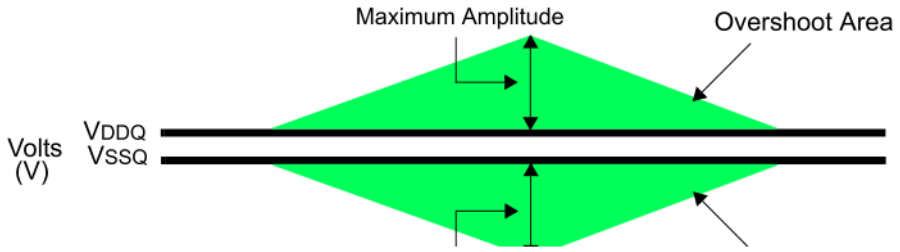


Figure 55 Data Overshoot

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Data Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 179 AC Overshoot Specification for Data and Mask Pins

Parameter	Specification					
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133
Maximum peak amplitude allowed for overshoot area	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V
Maximum overshoot area above V_{DDQ}	0.25 V/ns	0.19 V/ns	0.15 V/ns	0.13 V/ns	0.11 V/ns	0.10 V/ns

Table 180 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for overshoot area	Max	0.35		V
Maximum area above V_{DD}	Max	0.12	0.10	V/ns

Test References

- *See Figure 100 and Table 37 in Section 9 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- *See Figure 126 and Table 49 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Set the number of sampling points to 2M samples.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Obtain the overshoot region. Overshoot region starts at the rising VDDQ crossing and ends at the falling VDDQ crossing.

4 Within Overshoot region #1, perform the following steps:

i Evaluate Overshoot Amplitude by performing the following steps:
a. Use TMAX and VMAX to get time stamp of maximum voltage on overshoot region of the acquired waveform.
b. Calculate: Overshoot Amplitude = VMAX – VDDQ.

ii Evaluate Area below VDDQ = (Overshoot Region End – Overshoot Region Start) * VDDQ.

iii Evaluate Total Area above 0 volt by using Trapezoidal Method Area Calculation as shown in following figure:

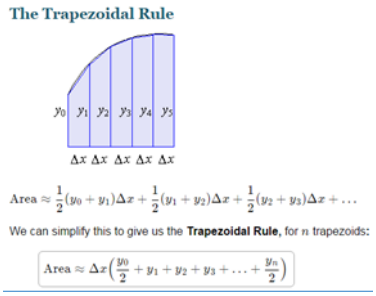


Figure 56 Trapezoidal Rule

iv Calculate area above VDDQ = Total area above 0 volt - area below VDDQ.

v Store calculated result below for later worst case finding process:

- Overshoot Amplitude
- Area above VDDQ

5 Repeat the previous step for the rest Overshoot Region found in acquired waveform.

6 Find the worst result below from stored result. Compare test result to the compliance test limit.

- Overshoot Amplitude
- Area above VDDQ

Expected/Observable Results

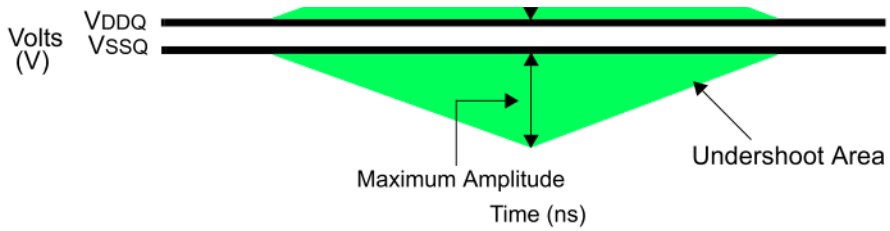
- The measured maximum voltage value must be less than or equal to the maximum overshoot value.
- The calculated Overshoot area value must be less than or equal to the maximum Overshoot area allowed.

Undershoot Amplitude/Area (Data)

Test Overview

The purpose of this test is to verify that the undershoot value of the test signal found from all regions of the acquired waveform is less than or equal to the conformance limit of the maximum peak amplitude allowed for undershoot as specified in the *JEDEC specification*.

When there is an undershoot, the area is calculated based on the undershoot width. The Undershoot area should be less than or equal to the conformance limit of the maximum undershoot area allowed as specified in the *JEDEC specification*.



Data Undershoot

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Data Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 181 AC Undershoot Specification for Clock, Data, Strobe and Mask Pins

Parameter	Specification					
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133
Maximum peak amplitude allowed for undershoot area	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V
Maximum undershoot area below V_{SSQ}	0.25 V/ns	0.19 V/ns	0.15 V/ns	0.13 V/ns	0.11 V/ns	0.10 V/ns

Table 182 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for undershoot area	Max	0.35		V
Maximum area below V_{SS}	Max	0.12	0.10	V/ns

Test References

- See *Figure 100 and Table 37 in Section 9 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Figure 126 and Table 49 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Set the number of sampling points to 2M samples.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Obtain the undershoot region. Undershoot Region starts at falling 0 volt crossing and end at rising 0 volt crossing.

4 Within Undershoot region #1, perform the following steps:

   i Evaluate Undershoot Amplitude by performing the following steps:
   a. Use TMIN and VMIN to get time stamp of maximum voltage on undershoot region of the acquired waveform.
   b. Calculate: Undershoot Amplitude = 0- VMIN

   ii Evaluate total area below 0 volt by using Trapezoidal Method Area Calculation (refer to Figure 56)

   iii Store Calculated result below for later worst case finding process:

   - Undershoot Amplitude
   - Total area below 0 volt

5 Repeat the previous step for the rest Undershoot Region found in acquired waveform.

6 Find the worst result below from stored result. Compare test result to the compliance test limit.

   - Undershoot Amplitude
   - Total area below 0 volt

Expected/Observable Results

- The measured minimum voltage value for the test signal must be less than or equal to the maximum undershoot value.
- The calculated undershoot area value must be less than or equal to the maximum undershoot area allowed.

Read/Write Eye-Diagram Tests

User Defined Real-Time Eye Diagram Test For Read Cycle

Test Overview

The purpose of this test is to automate all the required setup procedures required in order to generate an eye diagram for the DDR3 data READ cycle.

The additional feature of having a mask test is allow users to perform evaluations and debugging on the eye diagram created.

Mode Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of interest

- READ

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signals (supported by Data Strobe Signals)

Required Signals that are needed to perform this test on oscilloscope:

- Pin Under Test, PUT = DQ Signals
- Supporting Pin = DQS Signals

Test References

- There is no available test specification on eye testing in JEDEC specifications. Mask testing is definable by the customers for their evaluation tests usage.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)
2. Gather the list of start time of each Read Burst.
3. Gather the list of end time of each Read Burst.
4. Save acquired DQS into new waveform file in BIN format. Name it “DQS.bin”.
5. Measure VMinDQS which is the minimum voltage of DQS for the whole acquisition.
6. Modify “DQS.bin” waveform file to ignore unwanted region. It is done where within each of the region below, set the sampling voltage at VMinDQS.
   - Region #1:from start of acquisition to start time of Read burst #1.
   - Region #2:from end time of Read burst #1 to start time of Read burst #2. Continue this until from end time of Read burst #n-1 to start time of Read burst #n. note n=number of Read burst.
   - Region #3:from end time of the last Read burst to the end of acquisition.
7. Rename modified “DQS.bin” into “DQSEyeFilt.bin”.
8. Load acquired data signal into WMemory2. Then use Function3 as “Magnify/Duplicate” of Loaded Waveform Memory.
9. Load “DQSEyeFilt.bin” into WMemory4. Then use Function2 as “Magnify/Duplicate” of Loaded Waveform Memory.

10 Setup Clock Recovery settings on SDA.
:Explicit clock, Source = Function2(DQSEyeFilt), Rise/Fall Edge

11 Setup measurement threshold values for the Function3(Data) and the Function2(DQSEyeFilt).

12 Setup fix time scale and time position values for Function3(Data) and Function2(DQSEyeFilt).

13 Turn ON Color Grade Display option.

14 Identify the X1 value for re-adjustment of selected test mask.

15 Setup Mask Test settings. (Load default Test Mask on screen)

16 Turn ON Real Time Eye on SDA.

17 Start mask test until eye diagram folded.

18 Return total failed UnitInterval as a test result.

Expected/Observable Results

- Generation of an eye diagram for the DDR3 data READ cycle and loading of a default test mask pattern.
- The test will show a fail status if the total failed UnitInterval is greater than 0.

User Defined Real-Time Eye Diagram Test For Write Cycle

Test Overview

The purpose of this test is to automate all the required setup procedures required in order to generate an eye diagram for the DDR3 data WRITE cycle.

The additional feature of having a mask test is allow users to perform evaluations and debugging on the eye diagram created.

Mode Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of interest

- WRITE

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Signals (supported by Data Strobe Signals)

Required Signals that are needed to perform this test on oscilloscope:

- Pin Under Test, PUT = DQ Signals
- Supporting Pin = DQS Signals

Test References

- There is no available test specification on eye testing in JEDEC specifications. Mask testing is definable by the customers for their evaluation tests usage.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)
2 Gather the list of start time of each Write Burst.
3 Gather the list of end time of each Write Burst.
4 Save acquired DQS into new waveform file in BIN format. Name it “DQS.bin”.
5 Measure VMinDQS which is the minimum voltage of DQS for the whole acquisition.
6 Modify “DQS.bin” waveform file to ignore unwanted region. It is done where within each of the region below, set the sampling voltage at VMinDQS.
   - Region #1:from start of acquisition to start time of Write burst #1.
   - Region #2:from end time of Write burst #1 to start time of Write burst #2. Continue this until from end time of Write burst #n-1 to start time of Write burst #n. note n=number of Write burst.
   - Region #3:from end time of the last Write burst to the end of acquisition.
7 Rename modified “DQS.bin” into “DQSEyeFilt.bin”.
8 Load acquired data signal into WMemory2. Then use Function3 as “Magnify/Duplicate” of Loaded Waveform Memory.
9 Load “DQSEyeFilt.bin” into WMemory4. Then use Function2 as “Magnify/Duplicate” of Loaded Waveform Memory.
10 Setup Clock Recovery settings on SDA.
: Explicit clock, Source = Function2(DQSEyeFilt), Rise/Fall Edge

11 Setup measurement threshold values for the Function3(Data) and the Function2(DQSEyeFilt).
12 Setup fix time scale and time position values for Function3(Data) and Function2(DQSEyeFilt).
13 Turn ON Color Grade Display option.
14 Identify the X1 value for re-adjustment of selected test mask.
15 Setup Mask Test settings. (Load default Test Mask on screen)
16 Turn ON Real Time Eye on SDA.
17 Start mask test until eye diagram folded.
18 Return total failed UnitInterval as a test result.

Expected/Observable Results

- Generation of an eye diagram for the DDR3 data WRITE cycle and loading of a default test mask pattern.
- The test will show a fail status if the total failed UnitInterval is greater than 0.

12 Data Mask Tests Group

This section provides the Methods of Implementation (MOIs) for Data Mask tests using a Keysight Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

Probing for Data Mask Tests

When performing the Data Mask tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Data Mask tests may look similar to the following diagram. Refer to the Connection tab in the DDR3 Electrical Performance Compliance application for the exact number of probe connections.

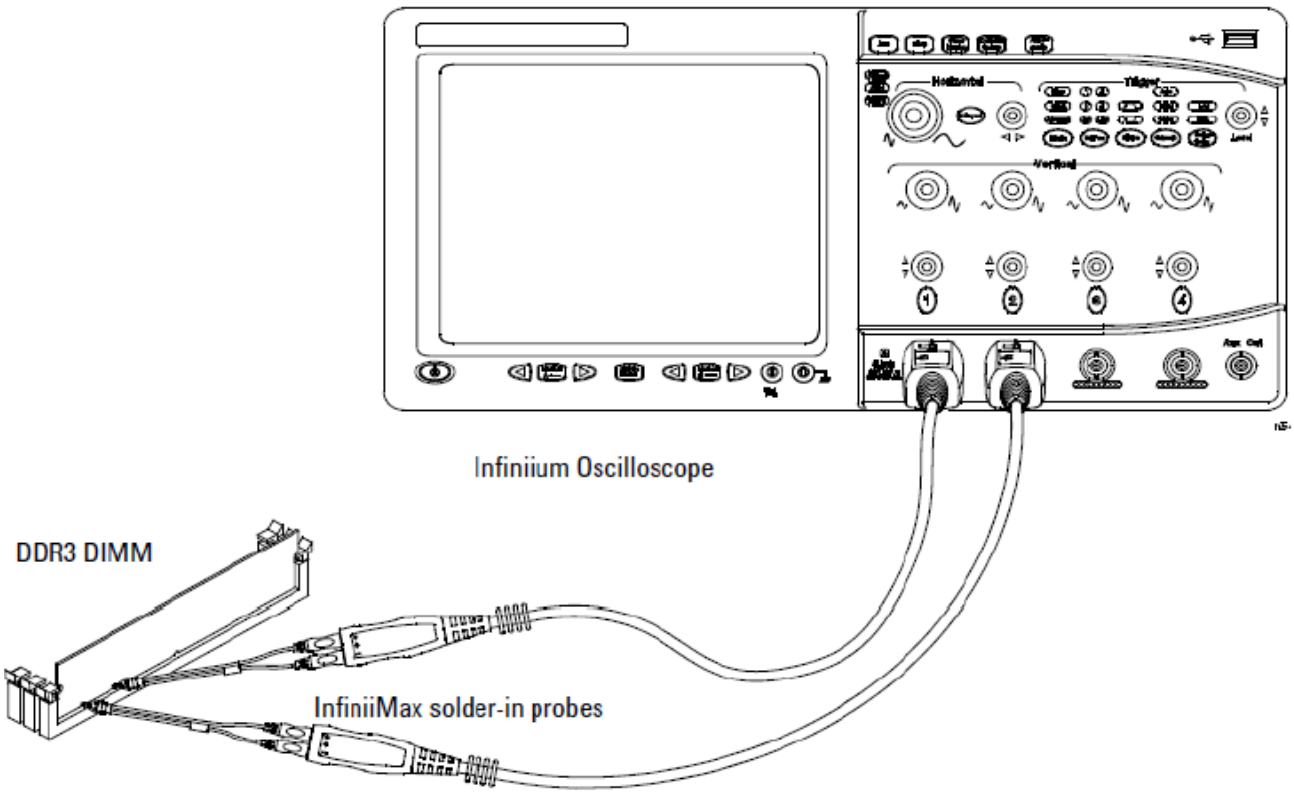


Figure 57 Probing for Data Mask Tests with Two Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 57 are just examples).

For more information on the probe amplifiers and differential probe heads, refer to the respective user guide for Probes.

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Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the **Set Up** tab.

6 Select the **Test Mode**, **SDRAM Type, Speed Grade**, and **AC Levels** options.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

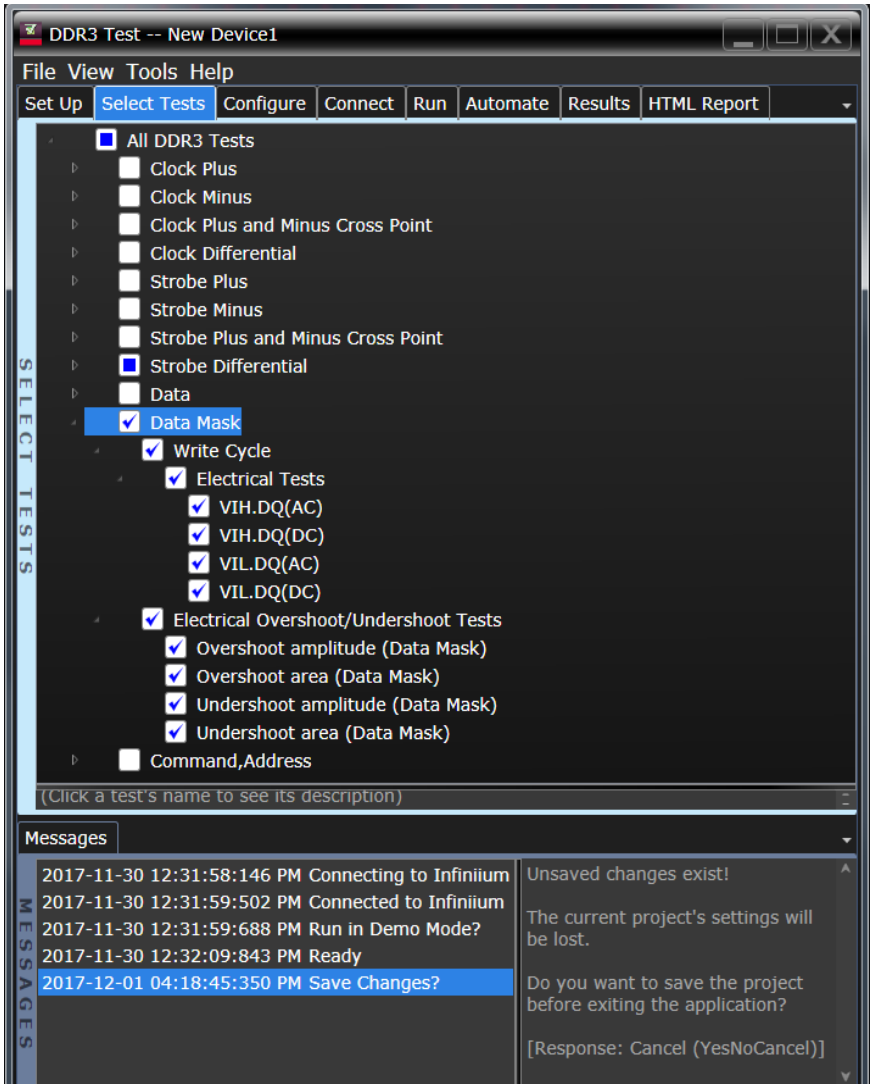

Figure 58 Selecting Data Mask Tests

Electrical Tests

VIH.DQ(AC)

Test Overview

The purpose of this test is to verify that the voltage level of the test signal at tDS (DM input setup time in JEDEC specification) with reference to the DQS signal is greater than the conformance lower limits of the $V_{IH(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Mask Signals (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQS

Test Definition Notes from the Specification

Table 183 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-800/1066/1333/1600		DDR3-1866/2133		Units
		Min	Max	Min	Max	
$V_{IH,DQ(AC\ 175)}$	AC input logic high	V_{REF} + 0.175	Note 2[a]	-	-	V
$V_{IH,DQ(AC\ 150)}$	AC input logic high	V_{REF} + 0.150	Note 2[a]	-	-	V
$V_{IH,DQ(AC\ 135)}$	AC input logic high	-	-	V_{REF} + 0.135	Note 2[a]	V

a: Refers to Note 2 in Table 24 of the *JEDEC Standard JESD79-3E. See* section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Table 184 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3L-800/1066		DDR3-1333/1600		Units
		Min	Max	Min	Max	
$V_{IH,DQ(AC\ 160)}$	AC input logic high	V_{REF} + 0.160	Note 2[a]	-	-	V
$V_{IH,DQ(AC\ 135)}$	AC input logic high	V_{REF} + 0.135	Note 2[a]	V_{REF} + 0.135	Note 2[a]	V

a: Refers to Note 2 in Table 5 of the *JEDEC Standard JESD79-3-1*. See section 9.6.2 of "Overshoot and Undershoot Specifications" of the *JEDEC Standard JESD79-3E*.

Table 185 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IH,DQ(AC)}$	AC input logic high	V_{REF} + 0.150	Note 2[b]	V	1[a], 2[b], 5[c]

a: Refers to Note 1 in Table 35 of the *JEDEC Standard JESD209-3*. For DQ input only pins. $V_{Ref} = V_{RefDQ(DC)}$.

b: Refers to Note 2 in Table 35 of the *JEDEC Standard JESD209-3*. See section 8.5 "Overshoot and Undershoot Specifications" on page 92 of the specification document.

c: Refers to Note 5 in Table 35 of the *JEDEC Standard JESD209-3*. For reference: $V_{ODTR}/2$ +/- 12mV.

Test References

- See *Table 24 in Section 8.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010,*
- See *Table 5 in Section 3.2 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1, July 2010* and
- See *Table 37 in Section 7 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid rising DM crossings that cross $V_{IH(AC)}$ in the said burst.

4 For all DM crossings found, locate all next DQS crossings that cross 0V.

5 Calculate the time where the test result is taken. Calculation is expressed as $T_{TESTRESULT} = T_{DQS\ MIDPOINT} - tDS$.
(tDS - DM input setup time in JEDEC specification which due to speed grade.)

6 Take voltage level of DM signal at $T_{TESTRESULT}$ as the test result for $V_{IH(AC)}$.

7 Collect all $V_{IH(AC)}$.

8 Determine the worst result from the set of $V_{IH(AC)}$ measured.

Expected/Observable Results

- The voltage level of the test signal at tDS with reference to the DQS signal must be greater than or equal to the minimum $V_{IH(AC)}$ value.

VIH.DQ(DC)

Test Overview

The purpose of this test is to verify that the histogram minimum value of the test signal within the sampling window (from signal tDS to tDH with reference to the DQS signal) is within the conformance limits of the $V_{IH(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. Users may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of VDD which directly affects the conformance lower limit is set to 1.50V for typical DDR3, 1.35V for DDR3L and 1.2V for LPDDR3. Users may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customize test limit set based on different values of VDD.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Mask Signals (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQS

Test Definition Notes from the Specification

Table 186 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-800/1066/1333/1600		DDR3-1866/2133		Units
		Min	Max	Min	Max	
$V_{IH,DQ(DC\ 100)}$	DC input logic high	V_{REF} + 0.100	V_{DD}	V_{REF} + 0.100	V_{DD}	V

Table 187 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3L-800/1066		DDR3L-1333/1600		Units
		Min	Max	Min	Max	
$V_{IH,DQ(DC\ 90)}$	DC input logic high	V_{REF} + 0.09	V_{DD}	V_{REF} + 0.09	V_{DD}	V

Table 188 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IHDQ(DC)}$	DC input logic high	V_{REF} + 0.100	V_{DDQ}	V	1[a]

a: Refers to Note 1 in Table 35 of the *JEDEC Standard JESD209-3*. For DQ input only pins. $V_{Ref} = V_{RefDQ(DC)}$.

Test References

- See *Table 24 in Section 8.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010,*
- See *Table 5 in Section 3.2 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1, July 2010* and
- See *Table 37 in Section 7 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid rising DM crossings that cross $V_{IH\ (DC)}$ in the said burst.

4 For all DM crossings found, locate all next DQS crossings that cross midpoint. (0V for differential DQS and V_{REF} for single ended DQS.)

5 Setup the histogram function settings.

6 Set the histogram window as follows:

- Ax: X-time position of tDS (DM input setup time in JEDEC specification) before DQS crossing midpoint.
- Bx: X-time position of tDH (DM input hold time in JEDEC specification) after DQS crossing midpoint.
- By: Y-position at V_{REF} voltage level.
- Ay: Top of the displaying window to make sure it covers the maximum level of the respective signal.

7 Use histogram 'Minimum' value as the test result for $V_{IH(DC)}$.

8 Collect all $V_{IH\ (DC)}$.

9 Determine the worst result from the set of $V_{IH\ (DC)}$ measured.

Expected/Observable Results

- The histogram minimum value of the test signal within the sampling window (from signal tDS to tDH with reference to the DQS signal) must be within the specification limits.

VIL.DQ(AC)

Test Overview

The purpose of this test is to verify that the voltage level of the test signal at tDS (DM input setup time in JEDEC specification) with reference to the DQS signal is lower than the conformance lower limits of the $V_{IL(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Mask Signals (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQS

Test Definition Notes from the Specification

Table 189 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-800/1066		DDR3-1333/1600		DDR3-1866/2133		Units
		Min	Max	Min	Max	Min	Max	
$V_{IL,DQ(AC\ 175)}$	AC input logic low	Note 2[a]	V_{REF} - 0.175	-	-	-	-	V
$V_{IL,DQ(AC\ 150)}$	AC input logic low	Note 2[a]	V_{REF} - 0.150	Note 2[a]	V_{REF} - 0.150	-	-	V
$V_{IL,DQ(AC\ 135)}$	AC input logic low	-	-	-	-	Note 2[a]	V_{REF} - 0.135	V

a: Refers to Note 2 in Table 24 of the *JEDEC Standard JESD79-3E. See* section 9.6 "Overshoot and Undershoot Specifications" on page 126 of the specification document.

Table 190 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3L-800/1066		DDR3L-1333/1600		Units
		Min	Max	Min	Max	
$V_{IL,DQ(AC\ 160)}$	AC input logic low	Note 2[a]	V_{REF} - 0.160	-	-	V
$V_{IL,DQ(AC\ 135)}$	AC input logic low	Note 2[a]	V_{REF} - 0.135	Note 2[a]	V_{REF} - 0.135	V

a: Refers to Note 2 in Table 5 of the *JEDEC Standard JESD79-3-1*. See section 9.6.2 of "Overshoot and Undershoot Specifications" of the *JEDEC Standard JESD79-3E*.

Table 191 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IL,DQ(AC)}$	AC input logic low	Note 2[b]	V_{REF} - 0.150	V	1[a], 2[b], 5[c]

a: Refers to Note 1 in Table 35 of the *JEDEC Standard JESD209-3*. For DQ input only pins. $V_{Ref} = V_{RefDQ(DC)}$.

b: Refers to Note 2 in Table 35 of the *JEDEC Standard JESD209-3*. See section 8.5 "Overshoot and Undershoot Specifications" on page 92 of the specification document.

c: Refers to Note 5 in Table 35 of the *JEDEC Standard JESD209-3*. For reference: $V_{ODTR}/2$ +/- 12mV.

Test References

- See *Table 24 in Section 8.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010,*
- See *Table 5 in Section 3.2 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Table 37 in Section 7 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid falling DM crossings that cross $V_{IL\ (AC)}$ in the said burst.

4 For all DM crossings found, locate all next DQS crossings that cross midpoint. (0V for differential DQS and V_{REF} for single ended DQS.)

5 Calculate the time where the test result is taken. Calculation is expressed as $T_{TESTRESULT} = T_{DQS\ MIDPOINT} - tDS$.
(tDS - DM input setup time in the JEDEC specification due to speed grade.)

6 Take voltage level of DM signal at $T_{TESTRESULT}$ as the test result for $V_{IL(AC)}$.

7 Collect all $V_{IL(AC)}$.

8 Determine the worst result from the set of $V_{IL(AC)}$ measured.

Expected/Observable Results

- The voltage level of the test signal at tDS with reference to the DQS signal must be less than or equal to the maximum $V_{IL(AC)}$ value.

VIL.DQ(DC)

Test Overview

The purpose of this test is to verify that the histogram maximum value of the test signal within the sampling window (from signal tDS to tDH with reference to the DQS signal) is within the conformance limits of the $V_{IL(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Mask Signals (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin = DQS

Test Definition Notes from the Specification

Table 192 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-800/1066/1333/1600		DDR3-1866/2133		Units
		Min	Max	Min	Max	
$V_{IL,DQ(DC\ 100)}$	DC input logic low	V_{SS}	V_{REF} - 0.100	V_{SS}	V_{REF} - 0.100	V

Table 193 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3L-800/1066		DDR3-1333/1600		Units
		Min	Max	Min	Max	
$V_{IL,DQ(DC\ 90)}$	DC input logic low	V_{SS}	V_{REF} - 0.09	V_{SS}	V_{REF} - 0.09	V

Table 194 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IL,DQ(DC)}$	DC input logic low	V_{SSQ}	V_{REF} - 0.100	V	1[a]

a: Refers to Note 1 in Table 35 of the *JEDEC Standard JESD209-3*. For DQ input only pins. $V_{Ref} = V_{RefDQ(DC)}$.

Test References

- See *Table 24 in Section 8.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010*,
- See *Table 5 in Section 3.2 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Table 37 in Section 7 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid falling DM crossings that cross $V_{IL(DC)}$ in the said burst.

4 For all DM crossings found, locate all next DQS crossings that cross midpoint. (0V for differential DQS and V_{REF} for single ended DQS.)

5 Setup the histogram function settings.

6 Set the histogram window as follows:

- Ax: X-time position of tDS (DM input setup time in JEDEC specification) before DQS crossing midpoint.
- Bx: X-time position of tDH (DM input hold time in JEDEC specification) after DQS crossing midpoint.
- By: Y-position at V_{REF} voltage level.
- Ay: Top of the displaying window to make sure it covers the maximum level of the respective signal.

7 Use histogram 'Minimum' value as the test result for $V_{IL(DC)}$.

8 Collect all $V_{IL(DC)}$.

9 Determine the worst result from the set of $V_{IL(DC)}$ measured.

Expected/Observable Results

- The histogram maximum value of the test signal within the sampling window (from signal tDS to tDH with reference to the DQS signal) must be within the specification limits

SlewR on Setup Region

Test Overview

The purpose of this test is to calculate the rising slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Mask Signals (supported by Data Strobe Signal)

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin = DQS

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)
2. Take the first valid WRITE burst found.
3. Find all valid rising edges in the said burst. A valid rising edge starts at VIL (ac) crossing and end at following VIH (ac) crossing.
4. For all valid rising edges, find the transition time, delta TR which is time starts at VREF crossing and end at following VIH (ac) crossing. Then calculate Rising Slew.

$$\text{Rising Slew} = \frac{V_{IH(ac)}\ \text{min} - V_{REF}}{\text{delta TR}}$$

5. Determine the worst result from the set of SlewR measured.

Expected/Observable Results

- The calculated Rising Slew value for the test signal shall meet the user defined limit.

SlewF on Setup Region

Test Overview

The purpose of this test is to calculate the falling slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- Yes

Signal(s) of Interest:

- Data Mask Signals (supported by Data Strobe Signal)

Required Signals that are needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin = DQS

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)

2 Take the first valid WRITE burst found.

3 Find all valid falling edges in the said burst. A valid falling edge starts at VIH (ac) crossing and end at following VIL (ac) crossing.

4 For all valid falling edges, find the transition time, delta TF which is time starts at VREF crossing and end at following VIL (ac) crossing. Then calculate Falling Slew.

$$\text{Falling Slew} = \frac{V_{REF} - V_{IL(ac)}\ \text{max}}{\text{delta TF}}$$

5 Determine the worst result from the set of SlewF measured.

Expected/Observable Results

- The calculated Falling Slew value for the test signal shall meet the user defined limit.

SlewR on Hold Region

Test Overview

The purpose of this test is to calculate the rising slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Mask Signals (supported by Data Strobe Signal)

Required Signals that are needed to perform this test on oscilloscope:

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin = DQS

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)
2 Take the first valid WRITE burst found.
3 Find all valid rising edges in the said burst. A valid rising edge starts at VIL (ac) crossing and end at following VIH (ac) crossing.
4 For all valid rising edges, find the transition time, delta TR which is time starts at VIL(DC) crossing and end at following VREF crossing. Then calculate Rising Slew.

$$Rising\ Slew = \frac{V_{REF} - V_{IL(DC)}}{\text{delta TR}}$$

5 Determine the worst result from the set of SlewR measured.

Expected/Observable Results

- The calculated Rising Slew value for the test signal shall meet the user defined limit.

SlewF on Hold Region

Test Overview

The purpose of this test is to calculate the falling slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Mask Signals (supported by Data Strobe Signal)

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.
- Supporting Pin = DQS

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)

2 Take the first valid WRITE burst found.

3 Find all valid falling edges in the said burst. A valid falling edge starts at VIH (ac) crossing and end at following VIL (ac) crossing.

4 For all valid falling edges, find the transition time, delta TF which is time starts at VIH(DC) crossing and end at following VREF crossing. Then calculate Falling Slew.

$$Falling\ Slew = \frac{V_{IH(DC)} - V_{REF}}{\text{delta TF}}$$

5 Determine the worst result from the set of SlewF measured.

Expected/Observable Results

- The calculated Falling Slew value for the test signal shall meet the user defined limit.

Timing Tests

tDS(base)

Test Overview

The purpose of this test is to verify that the time interval from the data mask (DM rising/falling Edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC Specification.

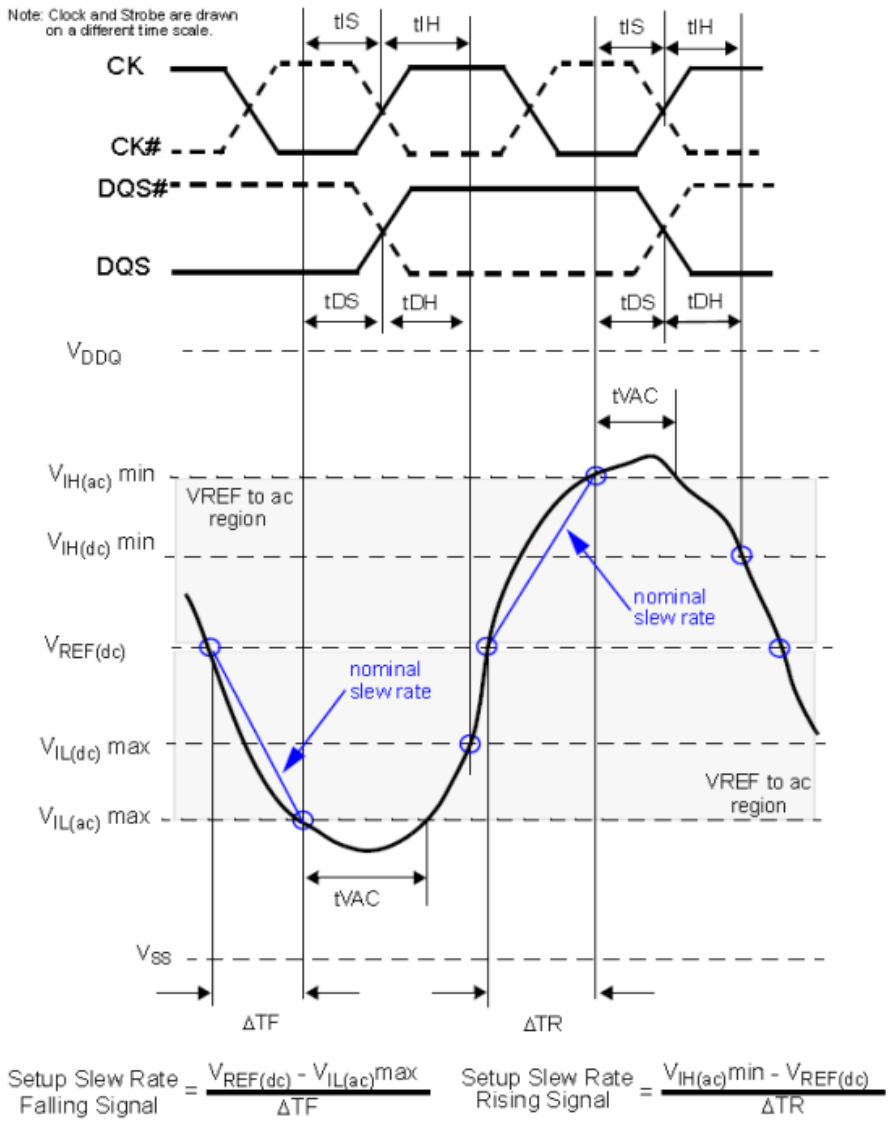

Figure 59 Nominal Slew Rate and t_{VAC} for Setup Time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

Modes Supported

- LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Mask Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope

- Data Mask Signal, DM
- Data Strobe Signal, (DQS as Supporting Signal). Use differential connection (DQS+ and DQS-)

Optional signal required to separate the signals for the different Ranks

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 195 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Data setup time to DQS, DQS# referenced to VIH(AC)/VIL(AC) levels	tDS(base) AC 175	75	-	25	-	-	-	-	-	ps
Data setup time to DQS, DQS# referenced to VIH(AC)/VIL(AC) levels	tDS(base) AC 150	125	-	75	-	30	-	10	-	ps

Parameter	Symbol	DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	
Data setup time to DQS, DQS# referenced to VIH(AC)/VIL(AC) levels	tDS(base) AC 150	TBD		TBD		ps
Data setup time to DQS, DQS# referenced toVIH(AC)/VIL(AC) levels	tDS(base) AC 135	TBD		TBD		ps

Table 196 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Data setup time to DQS, DQS# referenced to VIH(AC)/VIL(AC) levels	tDS(base) AC 160	90	-	40	-	-	-	-	-	ps
Data setup time to DQS, DQS# referenced to VIH(AC)/VIL(AC) levels	tDS(base) AC 135	140	-	90	-	45	-	25	-	ps

Table 197 Data Setup and Hold Base-Values

[ps]	Data Rate		Reference
	1600	1333	
tDS(base)	75	100	VIH/L(AC) = VREF(DC) ± 150mV

Test References

- See *Figure 129 to 132 and Table 68 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split Read and Write bursts in the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DM crossings that cross Vih(ac) in the said burst.
4 Find all valid falling DM crossings that cross Vil(ac) in the same burst.
5 For all DM crossings found, locate all next DQS crossings that cross 0V.
6 tDS is defined as the time between the DM crossing and the DQS crossing.
7 Collect all tDS.
8 Find the worst tDS among the measured values and report the value as the test result.

Expected/Observable Results

- The worst measured tDS must be within the specification limit.

tDH(base)

Test Overview

The purpose of this test is to verify that the time interval from the data mask (DM rising/falling edge) hold time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC Specification.

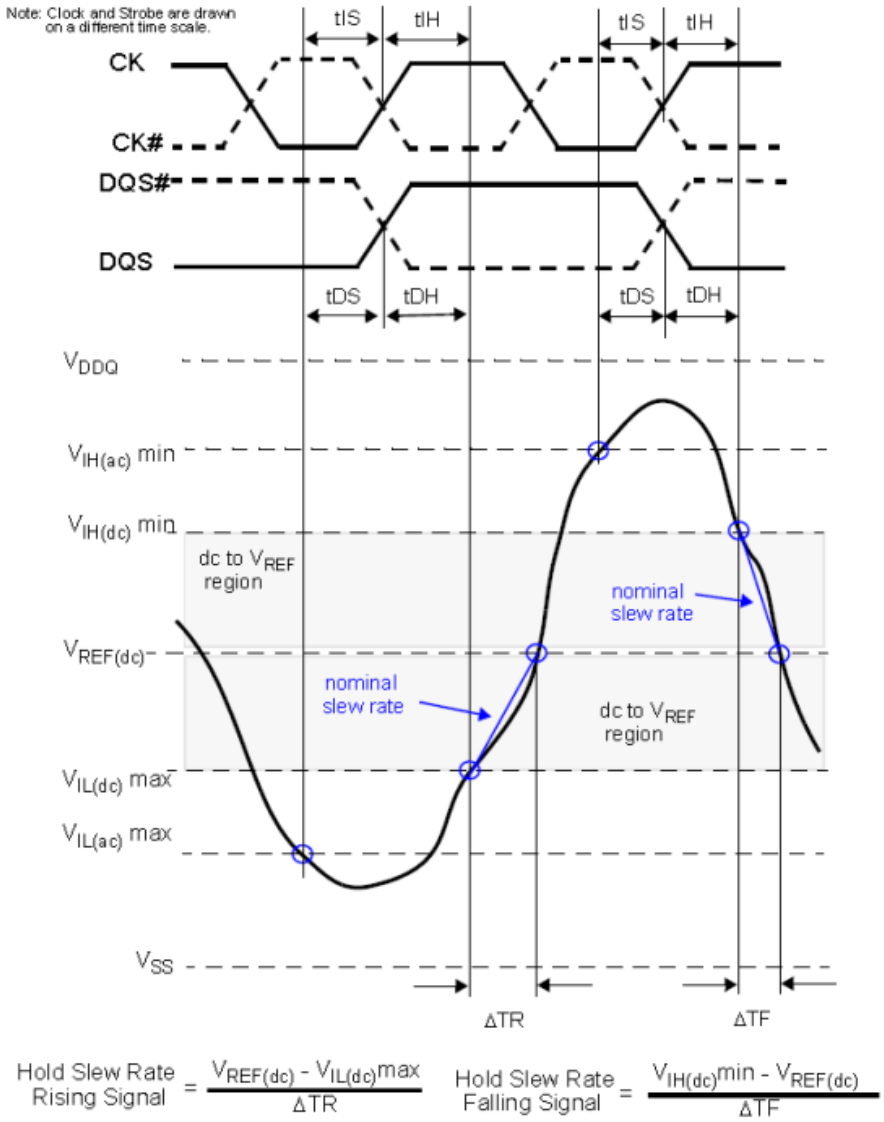

Figure 60 Nominal Slew Rate for Hold Time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock)

Modes Supported

- LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Mask Signal (DM)

Signals required to perform the test on the oscilloscope

- Data Mask Signal (DM)
- Data Strobe Signal (DQS as Supporting Signal). Use differential connection (DQS+ and DQS-)

Optional signal required to separate the signals for the different Ranks

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 198 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Data setup time to DQS, DQS# referenced to VIH(DC)/ VIL(DC) levels	tDH(base) DC 100	150	-	100	-	65	-	45	-	ps

Parameter	Symbol	DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	
Data setup time to DQS, DQS# referenced to VIH(DC)/ VIL(DC) levels	tDH(base) DC 100	TBD		TBD		ps

Table 199 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Data setup time to DQS, DQS# referenced to VIH(DC)/ VIL(DC) levels	tDS(base) DC 90	160	-	110	-	75	-	55	-	ps

Table 200 Data Setup and Hold Base-Values

[ps]	Data Rate		Reference
	1600	1333	
tDH(base)	100	125	VIH/L(DC) = VREF(DC) ± 100mV

Test References

- See *Figure 129 to 132 and Table 68 in Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split Read and Write bursts in the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DM crossings that cross $V_{IL(DC)}$ in the said burst.
4 Find all valid falling DM crossings that cross $V_{IH(DC)}$ in the same burst.
5 For all DM crossings found, locate all next DQS crossings that cross 0V.
6 tDH is defined as the time between the DM crossing and the DQS crossing.
7 Collect all tDH.
8 Find the worst tDH among the measured values and report the value as the test result.

Expected/Observable Results

- The worst measured tDH must be within the specification limit.

tDS-Diff(derate)

Test Overview

The purpose of this test is to verify that the time interval from data mask (DM rising/falling edge) setup time to the associated DQS crossing edge must be within the conformance limit as specified in the JEDEC Specification.

Modes Supported

- LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Mask Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope

- Data Mask Signal (DM)
- Data Strobe Signal (DQS as Supporting Signal). Use differential connection (DQS+ and DQS-)

Optional signal required to separate the signals for the different Ranks

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 201 Data Setup and Hold Base-Values

Units (ps)	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Reference
tDS (base) AC 175	75	25	-	-	-	-	$V_{IH/L(AC)}$
tDS (base) AC 150	125	75	30	10	-	-	$V_{IH/L(AC)}$
tDS (base) AC 135	-	-	-	-	TBD	TBD	$V_{IH/L(AC)}$
tDH (base) DC 100	150	100	65	45	TBD	TBD	$V_{IH/L(DC)}$

Table 202 Derating Values DDR3-800/1066 tDS/DH - AC/DC based Alternate AC 175 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 175 Threshold -> VIH(AC) = VREF(DC) + 175 mV, VIL(AC) = VREF(DC) - 175 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	88	50	88	50	88	50	-	-
	1.5	59	34	59	34	59	34	67	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	-2	-4	-2	-4	6	4
	0.8	-	-	-	-	-6	-10	2	-2
	0.7	-	-	-	-	-	-	-3	-8
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 175 Threshold -> VIH(AC) = VREF(DC) + 175 mV, VIL(AC) = VREF(DC) - 175 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	14	12	22	20	-	-	-	-
	0.8	10	6	18	14	26	24	-	-
	0.7	5	0	13	8	21	18	29	34
	0.6	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-30	-26	-22	-10

NOTE 1. Empty cell contents are defined as not supported.

Table 203 Derating Values DDR3-800/1066/1333/1600 tDS/DH - AC/DC based Alternate AC 150 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	75	50	75	50	75	50	-	-
	1.5	50	34	50	34	50	34	58	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	0	-4	-0	-4	8	4
	0.8	-	-	-	-	-0	-10	8	-2
	0.7	-	-	-	-	-	-	8	-8
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	16	12	24	20	-	-	-	-
	0.8	16	6	24	14	32	24	-	-
	0.7	16	0	24	8	32	18	40	34
	0.6	-15	-10	23	-2	31	8	39	24
	0.5	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	7	-26	15	-10

NOTE 1. Empty cell contents are defined as not supported.

Table 204 Derating Values DDR3-1866/2133 tDS/DH - AC/DC based Alternate AC 135 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	68	50	68	50	68	50	-	-
	1.5	45	34	45	34	45	34	53	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	-2	-4	-2	-4	10	4
	0.8	-	-	-	-	3	-10	11	-2
	0.7	-	-	-	-	-	-	14	-8
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	18	12	26	20	-	-	-	-
	0.8	19	6	27	14	35	24	-	-
	0.7	22	0	30	8	38	18	46	34
	0.6	25	-10	33	-2	41	8	49	24
	0.5	-	-	29	-16	37	-6	45	10
	0.4	-	-	-	-	30	-26	38	-10

NOTE 1. Empty cell contents are defined as not supported.

Table 205 Data Setup and Hold Base-Values

Units (ps)	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Reference
tDS (base) AC 150	90	40	-	-	$V_{IH/L(AC)}$
tDS (base) AC 135	140	90	45	25	$V_{IH/L(AC)}$
tDH (base) DC 90	160	110	75	55	$V_{IH/L(DC)}$

Table 206 Derating Values DDR3-800/1066 tDS/DH - AC/DC based Alternate AC 160 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based AC 160 Threshold -> VIH(AC) = VREF(DC) + 160 mV, VIL(AC) = VREF(DC) - 160 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	80	45	80	45	80	45	-	-
	1.5	53	30	53	30	53	30	58	38
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	-1	-3	-1	-3	7	5
	0.8	-	-	-	-	-3	-8	5	1
	0.7	-	-	-	-	-	-	3	-5
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based AC 160 Threshold -> VIH(AC) = VREF(DC) + 160 mV, VIL(AC) = VREF(DC) - 160 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	15	13	23	21	-	-	-	-
	0.8	13	9	21	17	29	27	-	-
	0.7	11	3	19	11	27	21	35	37
	0.6	8	-4	16	4	24	14	32	30
	0.5	-	-	4	-6	12	4	20	20
	0.4	-	-	-	-	-8	-11	0	5

NOTE 1. Empty cell contents are defined as not supported.

Table 207 Derating Values DDR3-800/1066/1333/1600 tDS/DH - AC/DC based Alternate AC 135 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	68	45	68	45	68	45	-	-
	1.5	45	30	45	30	45	30	53	38
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	2	-3	2	-3	10	5
	0.8	-	-	-	-	3	-8	11	1
	0.7	-	-	-	-	-	-	14	-5
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	18	13	26	21	-	-	-	-
	0.8	19	9	27	17	35	27	-	-
	0.7	22	3	30	11	38	21	46	37
	0.6	25	-4	33	4	41	14	49	30
	0.5	-	-	29	-6	37	4	45	20
	0.4	-	-	-	-	30	-11	38	5

NOTE 1. Empty cell contents are defined as not supported.

Table 208 Data Setup and Hold Base-Values

[ps]	Data Rate		Reference
	1600	1333	
tDS(base)	75	100	VIH/L(AC) = VREF(DC) ± 150mV

Table 209 Derating Values LPDDR3 tDS/DH - AC/DC based AC 150

ΔtDS, ΔtDH derating in [ps] AC/DC based AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV DC 100 Threshold -> VIH(DC) = VREF(DC) + 100 mV, VIL(DC) = VREF(DC) - 100 mV									
		DQS_t, DQS_c Differential Slew Rate							
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ, DM Slew Rate V/ns	4.0	38	25	38	25	38	25	-	-
	3.5	32	21	32	21	32	21	32	21
	3.0	25	17	25	17	25	17	25	17
	2.5	-	-	15	10	15	10	15	10
	2.0	-	-	-	-	0	0	0	0
	1.5	-	-	-	-	-	-	-25	-17
	1.0	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV DC 100 Threshold -> VIH(DC) = VREF(DC) + 100 mV, VIL(DC) = VREF(DC) - 100 mV							
		DQS_t, DQS_c Differential Slew Rate					
		4.0V/ns		3.0V/ns		2.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ, DM Slew Rate V/ns	4.0	-	-	-	-	-	-
	3.5	-	-	-	-	-	-
	3.0	25	17	-	-	-	-
	2.5	15	10	15	10	-	-
	2.0	0	0	0	0	0	0
	1.5	-25	-17	-25	-17	-25	-17
	1.0	-75	-50	-75	-50	-75	-50

NOTE 1. Empty cell contents are defined as not supported.

Test References

- See *Figure 129 to 132 and Table 68 & 69 in the JEDEC Standard JESD209-3E, December 2011*.

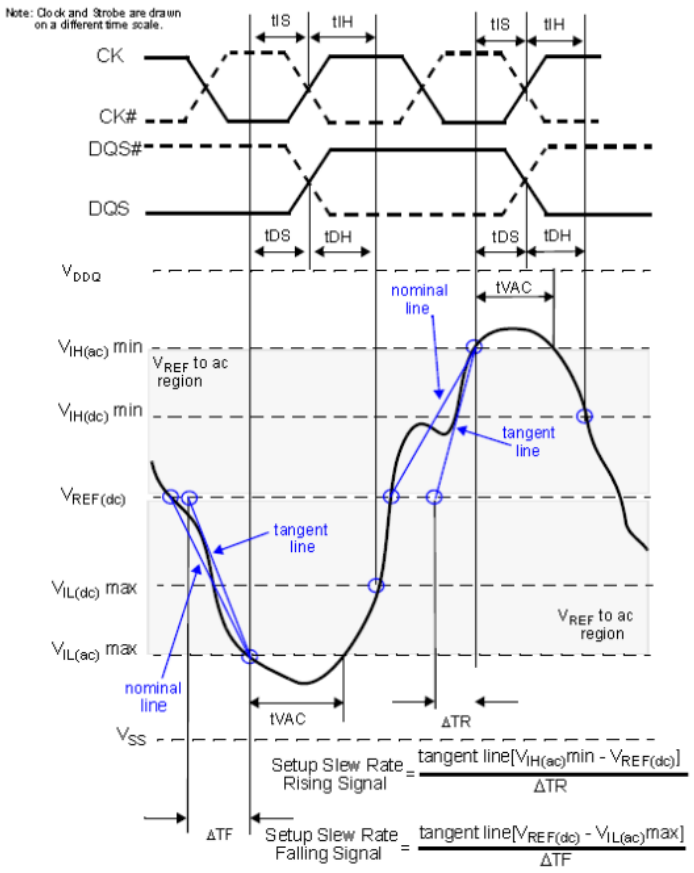

Figure 61 Tangent Line for Setup Time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

Measurement Algorithm

1 Acquire and split Read and Write bursts in the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DM crossings that cross VIH(AC) in the said burst.
4 Find all valid falling DM crossings that cross VIL(AC) in the same burst.
5 For all DM crossings found, locate all next DQS crossings that cross 0V.
6 tDS is defined as the time between the DM crossing and the DQS crossing.
7 Collect all tDS.
8 Find the worst tDS among the measured values and report the value as the test result.
9 Measure the mean slew rate for all the DM and DQS edges.
10 Use the mean slew rate for DM and DQS to determine the ΔtDS derating value based on the derating tables.
11 The test limit for tDS test = tDS(base) + ΔtDS.

Expected/Observable Results

- The worst measured tDS must be within the specification limit.

tDH-Diff(derate)

Test Overview

The purpose of this test is to verify that the time interval from data mask (DM rising/falling edge) hold time to the associated DQS crossing edge must be within the conformance limit as specified in the JEDEC Specification.

Modes Supported

- LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Mask Signal (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope

- Data Mask Signal (DM as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal). Use differential connection (DQS+ and DQS-)

Optional signal required to separate the signals for the different Ranks

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 210 Data Setup and Hold Base-Values

Units (ps)	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Reference
tDS (base) AC 175	75	25	-	-	-	-	$V_{IH/L(AC)}$
tDS (base) AC 150	125	75	30	10	-	-	$V_{IH/L(AC)}$
tDS (base) AC 135	-	-	-	-	TBD	TBD	$V_{IH/L(AC)}$
tDH (base) DC 100	150	100	65	45	TBD	TBD	$V_{IH/L(DC)}$

Table 211 Derating Values DDR3-800/1066 tDS/DH - AC/DC based Alternate AC 175 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 175 Threshold -> VIH(AC) = VREF(DC) + 175 mV, VIL(AC) = VREF(DC) - 175 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	88	50	88	50	88	50	-	-
	1.5	59	34	59	34	59	34	67	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	-2	-4	-2	-4	6	4
	0.8	-	-	-	-	-6	-10	2	-2
	0.7	-	-	-	-	-	-	-3	-8
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 175 Threshold -> VIH(AC) = VREF(DC) + 175 mV, VIL(AC) = VREF(DC) - 175 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	14	12	22	20	-	-	-	-
	0.8	10	6	18	14	26	24	-	-
	0.7	5	0	13	8	21	18	29	34
	0.6	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-30	-26	-22	-10

NOTE 1. Empty cell contents are defined as not supported.

Table 212 Derating Values DDR3-800/1066/1333/1600 tDS/DH - AC/DC based Alternate AC 150 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	75	50	75	50	75	50	-	-
	1.5	50	34	50	34	50	34	58	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	0	-4	-0	-4	8	4
	0.8	-	-	-	-	-0	-10	8	-2
	0.7	-	-	-	-	-	-	8	-8
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	16	12	24	20	-	-	-	-
	0.8	16	6	24	14	32	24	-	-
	0.7	16	0	24	8	32	18	40	34
	0.6	-15	-10	23	-2	31	8	39	24
	0.5	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	7	-26	15	-10

NOTE 1. Empty cell contents are defined as not supported.

Table 213 Derating Values DDR3-1866/2133 tDS/DH - AC/DC based Alternate AC 135 Threshold

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	68	50	68	50	68	50	-	-
	1.5	45	34	45	34	45	34	53	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	-2	-4	-2	-4	10	4
	0.8	-	-	-	-	3	-10	11	-2
	0.7	-	-	-	-	-	-	14	-8
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	18	12	26	20	-	-	-	-
	0.8	19	6	27	14	35	24	-	-
	0.7	22	0	30	8	38	18	46	34
	0.6	25	-10	33	-2	41	8	49	24
	0.5	-	-	29	-16	37	-6	45	10
	0.4	-	-	-	-	30	-26	38	-10

NOTE 1. Empty cell contents are defined as not supported.

Table 214 Data Setup and Hold Base-Values

Units (ps)	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Reference
tDS (base) AC 150	90	40	-	-	$V_{IH/L(AC)}$
tDS (base) AC 135	140	90	45	25	$V_{IH/L(AC)}$
tDH (base) DC 90	160	110	75	55	$V_{IH/L(DC)}$

Table 215 Derating Values DDR3-800/1066 tDS/DH - AC/DC based Alternate AC 160 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based AC 160 Threshold -> VIH(AC) = VREF(DC) + 160 mV, VIL(AC) = VREF(DC) - 160 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	80	45	80	45	80	45	-	-
	1.5	53	30	53	30	53	30	58	38
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	-1	-3	-1	-3	7	5
	0.8	-	-	-	-	-3	-8	5	1
	0.7	-	-	-	-	-	-	3	-5
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based AC 160 Threshold -> VIH(AC) = VREF(DC) + 160 mV, VIL(AC) = VREF(DC) - 160 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	15	13	23	21	-	-	-	-
	0.8	13	9	21	17	29	27	-	-
	0.7	11	3	19	11	27	21	35	37
	0.6	8	-4	16	4	24	14	32	30
	0.5	-	-	4	-6	12	4	20	20
	0.4	-	-	-	-	-8	-11	0	5

NOTE 1. Empty cell contents are defined as not supported.

Table 216 Derating Values DDR3-800/1066/1333/1600 tDS/DH - AC/DC based Alternate AC 135 Threshold

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	68	45	68	45	68	45	-	-
	1.5	45	30	45	30	45	30	53	38
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	2	-3	2	-3	10	5
	0.8	-	-	-	-	3	-8	11	1
	0.7	-	-	-	-	-	-	14	-5
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	18	13	26	21	-	-	-	-
	0.8	19	9	27	17	35	27	-	-
	0.7	22	3	30	11	38	21	46	37
	0.6	25	-4	33	4	41	14	49	30
	0.5	-	-	29	-6	37	4	45	20
	0.4	-	-	-	-	30	-11	38	5

NOTE 1. Empty cell contents are defined as not supported.

Table 217 Data Setup and Hold Base-Values

[ps]	Data Rate		Reference
	1600	1333	
tDH(base)	100	125	VIH/L(DC) = VREF(DC) ± 100mV

Table 218 Derating Values LPDDR3 tDS/DH - AC/DC based AC 150

ΔtDS, ΔtDH derating in [ps] AC/DC based AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV DC 100 Threshold -> VIH(DC) = VREF(DC) + 100 mV, VIL(DC) = VREF(DC) - 100 mV									
		DQS_t, DQS_c Differential Slew Rate							
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ, DM Slew Rate V/ns	4.0	38	25	38	25	38	25	-	-
	3.5	32	21	32	21	32	21	32	21
	3.0	25	17	25	17	25	17	25	17
	2.5	-	-	15	10	15	10	15	10
	2.0	-	-	-	-	0	0	0	0
	1.5	-	-	-	-	-	-	-25	-17
	1.0	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtDS, ΔtDH derating in [ps] AC/DC based AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV DC 100 Threshold -> VIH(DC) = VREF(DC) + 100 mV, VIL(DC) = VREF(DC) - 100 mV							
		DQS_t, DQS_c Differential Slew Rate					
		4.0V/ns		3.0V/ns		2.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ, DM Slew Rate V/ns	4.0	-	-	-	-	-	-
	3.5	-	-	-	-	-	-
	3.0	25	17	-	-	-	-
	2.5	15	10	15	10	-	-
	2.0	0	0	0	0	0	0
	1.5	-25	-17	-25	-17	-25	-17
	1.0	-75	-50	-75	-50	-75	-50

NOTE 1. Empty cell contents are defined as not supported.

Test References

- See *Figure 129,130, 131 & 132* and *Table 68 & 69 in Section 11of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

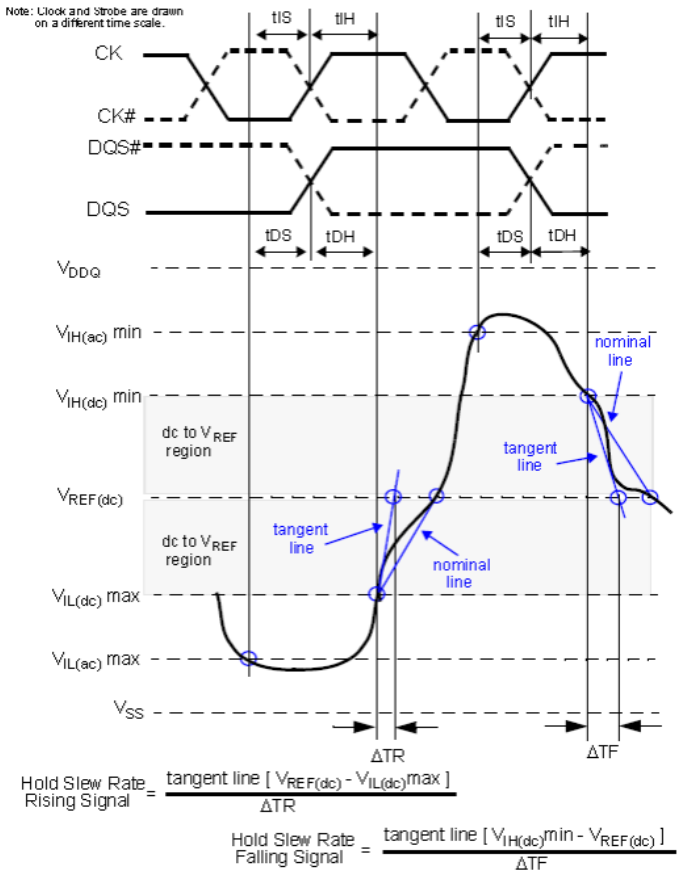

Figure 62 Tangent Line for Hold Time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock)

Measurement Algorithm

1 Acquire and split Read and Write bursts in the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DM crossings that cross $V_{IL(DC)}$ in the said burst.
4 Find all valid falling DM crossings that cross $V_{IH(DC)}$ in the same burst.
5 For all DM crossings found, locate all next DQS crossings that cross 0V.
6 tDH is defined as the time between the DM crossing and the DQS crossing.
7 Collect all tDH.
8 Find the worst tDH among the measured values and report the value as the test result.
9 Measure the mean slew rate for all the DM and DQS edges.
10 Use the mean slew rate for DM and DQS to determine the ΔtDH derating value based on the derating tables.
11 The test limit for tDH test = tDH(base) + ΔtDH.

Expected/Observable Results

- The worst measured tDH must be within the specification limit.

tDIPW

Test Overview

The purpose of this test is to verify that the width of the high or low level data mask signal is within the conformance limit as specified in the *JEDEC specification*.

Modes Supported

- DDR3, DDR3L, and LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Mask Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope

- Data Mask Signal (DM)
- Data Strobe Signal (DQS; must use a differential DQS connection)

Optional signal required to separate the signals for the different Ranks

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Table 219 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
DQ and DM Input pulse width for each input	tDIPW	600	-	490	-	400	-	ps

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	Min	Max	
DQ and DM Input pulse width for each input	tDIPW	360	-	320	-	280	-	ps

Table 220 AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
DQ and DM input pulse width	tDIPW	MIN	0.35		tCK(avg)

Test References

- See *Tables 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E July 2010* and
- See *Table 64 in Section 11 of the DDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Acquire and split Read and Write bursts in the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising and falling DM crossings at V_{REF} in the said burst.
4 tDIPW is the time starting from a rising/falling edge of the DM and ending at the following falling/rising (the following edge must not be in the same direction) edge.
5 Collect all tDIPW.
6 Determine the worst result from the set of tDIPW measured.

Expected/Observable Results

- The worst measured tDIPW must be within the specification limit.

tVAC(Data Mask)

Test Overview

The purpose of this test is to verify that the time of the data mask signal above $V_{IH(AC)}$ and below $V_{IL(AC)}$ must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- LPDDR3

Signal cycle of Interest

- Write

Require Read/Write separation

- Yes

Signal(s) of Interest

- Data Mask Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope

- Data Mask Signal (DM)
- Data Strobe Signal (DQS)

Optional signal required to separate the DQS signals from different ranks of memory

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory)

Test References

- See *Figures 79 & 81 in Section 11 of the DDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising and falling DM crossings at the $V_{IH(AC)}$ and $V_{IL(AC)}$ levels in the said burst.
4. tVAC (Data) is the time starting from a DM rising $V_{IH(AC)}$ cross point and ending at the following DQ falling $V_{IH(AC)}$ cross point.
5. tVAC (Data) is the time starting from a DM falling $V_{IL(AC)}$ cross point and ending at the following DM rising $V_{IL(AC)}$ cross point.
6. Collect all tVAC (Data).
7. Determine the worst result from the set of tVAC (Data) measured.
8. Report the value of the worst tVAC (Data). No compliance limit checking is performed for this test.

Expected/Observable Results

- The worst measured tVAC (Data) value must be within the specification limit.

Electrical Overshoot/Undershoot Tests

Overshoot Amplitude/Area (Data Mask)

Test Overview

The Overshoot test can be divided into two sub-tests: Overshoot amplitude and Overshoot area.

The purpose of this test is to verify that the overshoot value of the test signal found from all regions of the acquired waveform is lower than or equal to the conformance limit of the maximum peak amplitude allowed for overshoot as specified in the JEDEC specification.

When there is an overshoot, the area is calculated based on the overshoot width and overshoot amplitude. The Overshoot area should be lower than or equal to the conformance limit of the maximum overshoot area allowed as specified in the JEDEC specification.

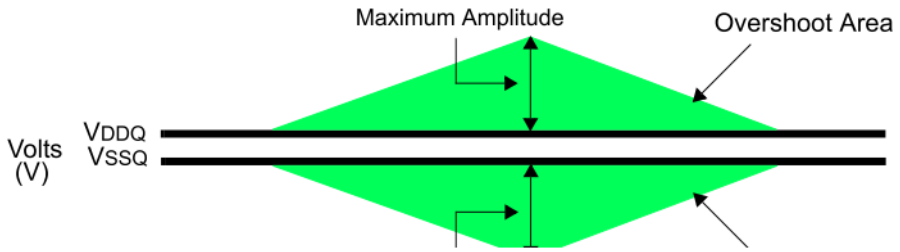

Figure 63 Data Mask Overshoot

Modes Supported

- DDR3, DDR3L, and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Data Mask Control Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 221 AC Overshoot Specification for Data Mask Pins

Parameter	Specification					
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133
Maximum peak amplitude allowed for overshoot area	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V
Maximum overshoot area above V_{DDQ}	0.25 V/ns	0.19 V/ns	0.15 V/ns	0.13 V/ns	0.11 V/ns	0.10 V/ns

Table 222 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for overshoot area	Max	0.35		V
Maximum area above V_{DD}	Max	0.12	0.10	V/ns

Test References

- *See Figure 100 and Table 37 in Section 9 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010*
- *See Figure 126 and Table 49 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Set the number of sampling points to 2M samples.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Obtain the overshoot region. Overshoot region starts at the rising VDDQ crossing and ends at the falling VDDQ crossing.

4 Within Overshoot region #1, perform the following steps:

   i Evaluate Overshoot Amplitude by performing the following steps:
   a. Use TMAX and VMAX to get time stamp of maximum voltage on overshoot region of the acquired waveform.
   b. Calculate: Overshoot Amplitude = VMAX – VDDQ.

   ii Evaluate Area below VDDQ = (Overshoot Region End – Overshoot Region Start) * VDDQ.

   iii Evaluate Total Area above 0 volt by using Trapezoidal Method Area Calculation as shown in following figure:

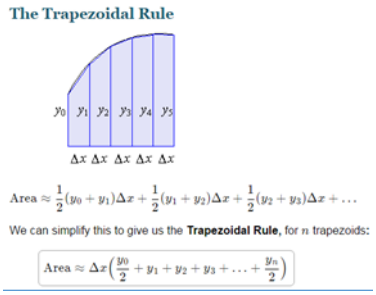

Figure 64 Trapezoidal Rule

iv Calculate area above VDDQ = Total area above 0 volt - area below VDDQ

v Store calculated result below for later worst case finding process:

- Overshoot Amplitude
- Area above VDDQ

5 Repeat the previous step for the rest Overshoot Region found in acquired waveform.

6 Find the worst result below from stored result. Compare test result to the compliance test limit.

- Overshoot Amplitude
- Area above VDDQ

Expected/Observable Results

- The measured maximum voltage value must be less than or equal to the maximum overshoot value.
- The calculated Overshoot area value must be less than or equal to the maximum Overshoot area allowed.

Undershoot Amplitude/Area (Data Mask)

Test Overview

The Undershoot Test can be divided into two sub-tests: Undershoot amplitude and Undershoot area.

The purpose of this test is to verify that the undershoot value of the test signal found from all regions of the acquired waveform is less than or equal to the conformance limit of the maximum peak amplitude allowed for undershoot as specified in the *JEDEC specification*.

When there is an undershoot, the area is calculated based on the undershoot width. The Undershoot area should be less than or equal to the conformance limit of the maximum undershoot area allowed as specified in the *JEDEC specification*.

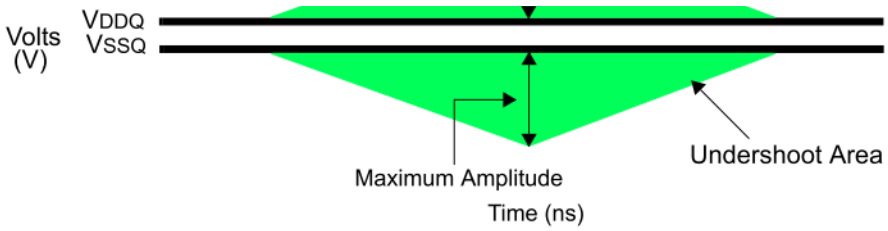

Figure 65 Data Mask Undershoot

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Data Mask Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 223 AC Undershoot Specification for Data Mask Pins

Parameter	Specification					
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133
Maximum peak amplitude allowed for undershoot area	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V
Maximum undershoot area below V_{SSQ}	0.25 V/ns	0.19 V/ns	0.15 V/ns	0.13 V/ns	0.11 V/ns	0.10 V/ns

Table 224 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for undershoot area	Max	0.35		V
Maximum area below V_{SS}	Max	0.12	0.10	V/ns

Test References

- See *Figure 100 and Table 37 in Section 9 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Figure 126 and Table 49 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Set the number of sampling points to 2M samples.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Obtain the undershoot region. Undershoot Region starts at falling 0 volt crossing and end at rising 0 volt crossing.

4 Within Undershoot region #1, perform the following steps:

   i Evaluate Undershoot Amplitude by performing the following steps:
   a. Use TMIN and VMIN to get time stamp of maximum voltage on undershoot region of the acquired waveform.
   b. Calculate: Undershoot Amplitude = 0- VMIN

   ii Evaluate total area below 0 volt by using Trapezoidal Method Area Calculation (refer to Figure 64)

   iii Store Calculated result below for later worst case finding process:

   - Undershoot Amplitude
   - Total area below 0 volt

5 Repeat the previous step for the rest Undershoot Region found in acquired waveform.

6 Find the worst result below from stored result. Compare test result to the compliance test limit.

   - Undershoot Amplitude
   - Total area below 0 volt

Expected/Observable Results

- The measured minimum voltage value for the test signal must be less than or equal to the maximum undershoot value.
- The calculated undershoot area value must be less than or equal to the maximum undershoot area allowed.

13 Command,Address Tests Group

This section provides the Methods of Implementation (MOIs) for Command, Address tests using a Keysight Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application DDR3 Compliance Test Application.

Probing for Command, Address Tests

When performing the Command, Address tests, the DDR3 Compliance Test ApplicationDDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Command, Address tests may look similar to the following diagram. Refer to the Connection tab in the DDR3 Electrical Performance Compliance application for the exact number of probe connections.

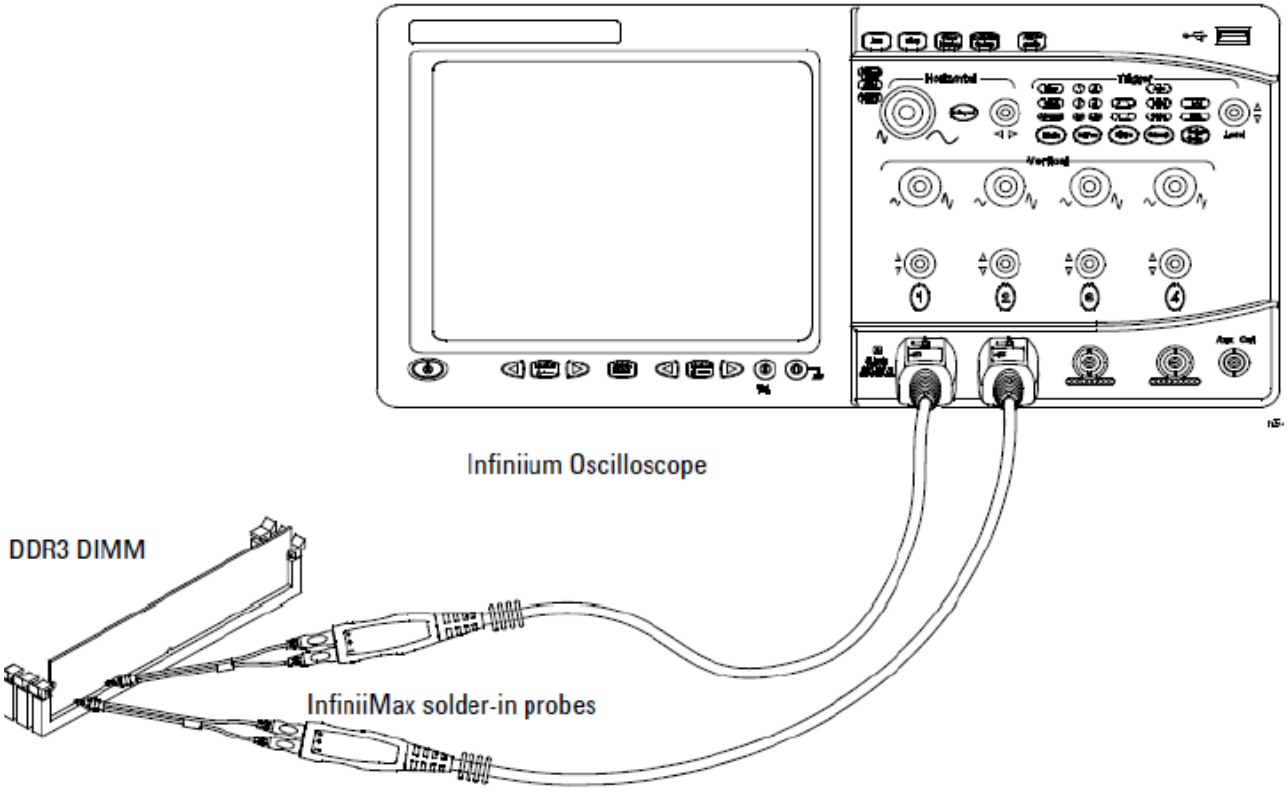

Figure 66 Probing for Command, Address with Two Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test ApplicationDDR3 Compliance Test Application.DDR3 Compliance Test Application (The channels shown in Figure 66 are just examples).

For more information on the probe amplifiers and differential probe heads, refer to the respective user guide for Probes.

Test Procedure

1. Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 25.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR3 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the **Set Up** tab.

6 Select the **Test Mode**, **SDRAM Type, Speed Grade**, and **AC Levels** options

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

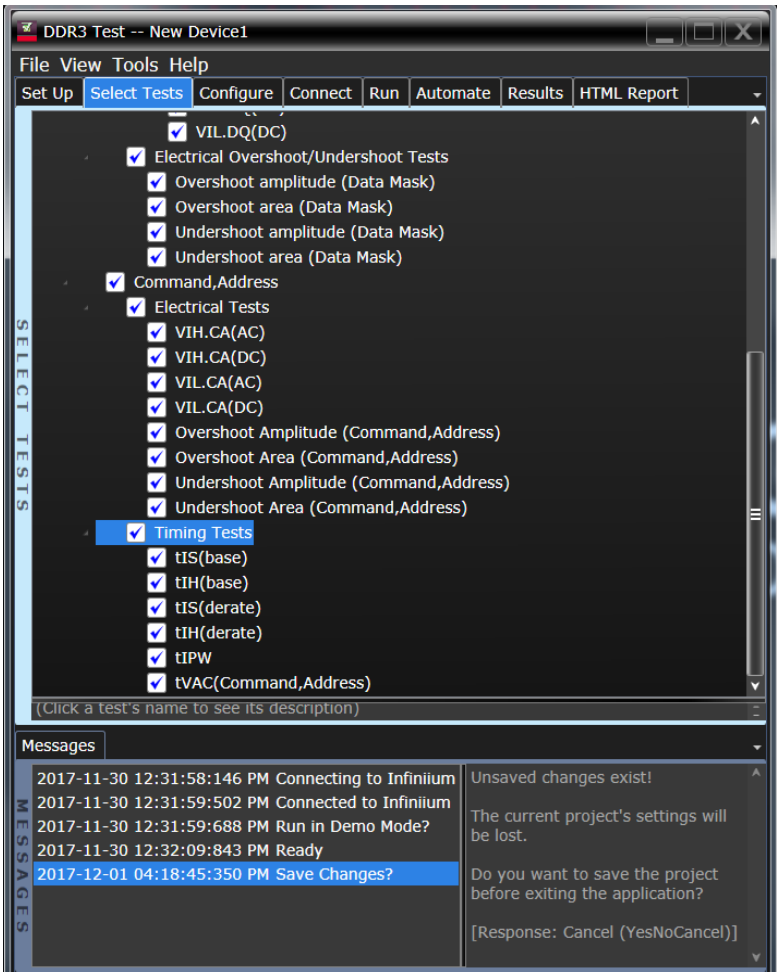

Figure 67 Selecting Command, Address Tests

Electrical Tests

VIH.CA(AC)

Test Overview

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window is greater than the conformance lower limits of the $V_{IH.CA(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Address Signals OR
- Control Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 225 Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-800/1066/1333/1600		DDR3-1866/2133		Units
		Min	Max	Min	Max	
$V_{IH,CA(AC\ 175)}$	AC input logic high	V_{REF} + 0.175	Note 2[a]	-	-	V
$V_{IH,CA(AC\ 150)}$	AC input logic high	V_{REF} + 0.150	Note 2[a]	-	-	V
$V_{IH,CA(AC\ 135)}$	AC input logic high	-	-	V_{REF} + 0.135	Note 2[a]	V
$V_{IH,CA(AC\ 125)}$	AC input logic high	-	-	V_{REF} + 0.125	Note 2[a]	V

a: Refers to Note 2 in Table 23 of the *JEDEC Standard JESD79-3E*. See section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Table 226 Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3L-800/1066		DDR3L-1333/1600		Units
		Min	Max	Min	Max	
$V_{IH,CA(AC\ 160)}$	AC input logic high	V_{REF} + 0.160	Note 2[a]	V_{REF} + 0.160	Note 2[a]	V
$V_{IH,CA(AC\ 135)}$	AC input logic high	V_{REF} + 0.135	Note 2[a]	V_{REF} + 0.135	Note 2[a]	V

a: Refers to Note 2 in Table 4 of the *JEDEC Standard JESD79-3-1*. See section 9.6.1 of "Overshoot and Undershoot Specifications" of *JEDEC Standard JESD79-3E*.

Table 227 Single-Ended AC and DC Input Levels for CA and CS_n Inputs

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IH,CA(AC)}$	AC input logic high	V_{REF} + 0.150	Note 2[b]	V	1[a], 2[b]

a: Refers to Note 1 in Table 33 of the *JEDEC Standard JESD209-3*. For CA and CS_n input only pins. $V_{Ref} = V_{RefCA(DC)}$.

b: Refers to Note 2 in Table 33 of the *JEDEC Standard JESD209-3*. See section 8.5 "Overshoot and Undershoot Specifications" on page 92 of the *specification document*.

Test References

- See *Table 23 in Section 8.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010,*
- See *Table 4 in Section 3.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1, July 2010* and
- See *Table 35 in Section 7 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Obtain sample or acquire signal data.

2 Find all valid positive pulses. A valid positive pulse starts at V_{REF} crossing at valid rising edge and ends at V_{REF} crossing at the following valid falling edge.

3 Zoom in on the first valid positive pulse and perform V_{TOP} measurement. Take the V_{TOP} measurement result as $V_{IH.CA(AC)}$ value.

4 Continue the previous step with another nine valid positive pulses that were found in the burst.

5 Determine the worst result from the set of $V_{IH.CA(AC)}$ measured.

Expected/Observable Results

- The high level voltage value of the test signal must be greater than or equal to the minimum $V_{IH.CA(AC)}$ value.

VIH.CA(DC)

Test Overview

The purpose of this test is to verify that the histogram mode value of the test signal within a valid sampling window is within the conformance limits of the $V_{IH(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of VDD which directly affect the conformance lower limit is set to 1.50V for typical DDR3, 1.35V for DDR3L and 1.2V for LPDDR3. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customize test limit set based on different values of VDD.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Address Signals OR
- Control Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 228 Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-800/1066/1333/1600		DDR3-1866/2133		Units
		Min	Max	Min	Max	
$V_{IH,CA(DC\ 100)}$	DC input logic high	V_{REF} + 0.100	V_{DD}	V_{REF} + 0.100	VDD	V

Table 229 Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3L-800/1066		DDR3L-1333/1600		Units
		Min	Max	Min	Max	
$V_{IH,CA(DC\ 90)}$	DC input logic high	V_{REF} + 0.09	V_{DD}	V_{REF} + 0.09	VDD	V

Table 230 Single-Ended AC and DC Input Levels for CA and CS_n Inputs

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IH,CA(DC)}$	DC input logic high	V_{REF} + 0.100	V_{DDCA}	V	1[a]

a: Refers to Note 1 in Table 33 of the *JEDEC Standard JESD209-3.* For CA and CS_n input only pins. $V_{Ref} = V_{RefCA(DC)}$.

Test References

- See *Table 23 in Section 8.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010,*
- See *Table 4 in Section 3.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1, July 2010 and*
- See *Table 35 in Section 7 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Obtain sample or acquire signal data.

2 Find all valid positive pulses. A valid positive pulse starts at V_{REF} crossing at valid rising edge and ends at V_{REF} crossing at the following valid falling edge.

3 Zoom in on the first valid positive pulse and perform V_{TOP} measurement. Take the V_{TOP} measurement result as $V_{IH.CA(DC)}$ value.

4 Continue the previous step with another nine valid positive pulses that were found in the burst.

5 Determine the worst result from the set of $V_{IH.CA(DC)}$ measured.

Expected/Observable Results

- The high level voltage value of the test signal must be greater than or equal to the minimum $V_{IH.CA(DC)}$ value.
- The high level voltage value of the test signal also must not be greater than maximum $V_{IH.CA\ (DC)}$ value which is VDD for DDR3/DDR3L or VDDCA for LPDDR3.

VIL.CA(AC)

Test Overview

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window is lower than the conformance lower limits of the VIL(AC) value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. Users may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Address Signals OR
- Control Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 231 Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-800/1066/1333/1600		DDR3-1866/2133		Units
		Min	Max	Min	Max	
$V_{IL,CA(AC\ 175)}$	AC input logic low	Note 2[a]	V_{REF} - 0.175	-	-	V
$V_{IL,CA(AC\ 150)}$	AC input logic low	Note 2[a]	V_{REF} - 0.150	-	-	V
$V_{IL,CA(AC\ 135)}$	AC input logic low	-	-	Note 2[a]	V_{REF} - 0.135	V
$V_{IL,CA(AC\ 125)}$	AC input logic low	-	-	Note 2[a]	V_{REF} - 0.125	V

a: Refers to Note 2 in Table 23 of the *JEDEC Standard JESD79-3E*. See section 9.6 “Overshoot and Undershoot Specifications” on page 126 of the specification document.

Table 232 Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3L-800/1066		DDR3L-1333/1600		Units
		Min	Max	Min	Max	
$V_{IL,CA(AC\ 160)}$	AC input logic low	Note 2[a]	V_{REF} - 0.160	Note 2[a]	V_{REF} - 0.160	V
$V_{IL,CA(AC\ 135)}$	AC input logic low	Note 2[a]	V_{REF} - 0.135	Note 2[a]	V_{REF} - 0.135	V

a: Refers to Note 2 in Table 4 of the *JEDEC Standard JESD79-3-1*. See section 9.6.1 of “Overshoot and Undershoot Specifications” of *JEDEC Standard JESD79-3E*.

Table 233 Single-Ended AC and DC Input Levels for CA and CS_n Inputs

Symbol	Parameter	Min	Max	Unit	Notes
$V_{ILCA(AC)}$	AC input logic low	Note 2[b]	V_{REF} - 0.150	V	1[a], 2[b]

a: Refers to Note 1 in Table 33 of the *JEDEC Standard JESD209-3.* For CA and CS_n input only pins. $V_{Ref} = V_{RefCA(DC)}$.

b: Refers to Note 2 in Table 33 of the *JEDEC Standard JESD209-3.* See section 8.5 "Overshoot and Undershoot Specifications" on page 92 of the *specification document*.

Test References

- See *Table 23 in Section 8.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010,*
- See *Table 4 in Section 3.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1, July 2010* and
- See *Table 35 in Section 7 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Obtain sample or acquire signal data.

2 Find all valid negative pulses. A valid negative pulse starts at V_{REF} crossing at valid falling edge and ends at V_{REF} crossing at the following valid rising edge.

3 Zoom in on the first valid negative pulse and perform V_{BASE} measurement. Take the V_{BASE} measurement result as $V_{IL.CA\ (AC)}$ value.

4 Continue the previous step with another nine valid negative pulses.

5 Determine the worst result from the set of $V_{IL.CA\ (AC)}$ measured.

Expected/Observable Results

- The histogram mode value of the test signal must be less than or equal to the maximum $V_{IL(AC)}$ value.

VIL.CA(DC)

Test Overview

The purpose of this test is to verify that the histogram mode value of the test signal within a valid sampling window is within the conformance limits of the $V_{IL(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.75V for typical DDR3, 0.675V for DDR3L and 0.6V for LPDDR3. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Modes Supported

- DDR3, DDR3L, and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Address Signals OR
- Control Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 234 Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-800/1066/1333/1600		DDR3-1866/2133		Units
		Min	Max	Min	Max	
$V_{IL,CA(DC\ 100)}$	DC input logic low	V_{SS}	V_{REF} - 0.100	V_{SS}	V_{REF} - 0.100	V

Table 235 Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3L-800/1066		DDR3L-1333/1600		Units
		Min	Max	Min	Max	
$V_{IL,CA(DC\ 90)}$	DC input logic low	V_{SS}	V_{REF} - 0.09	V_{SS}	V_{REF} - 0.09	V

Table 236 Single-Ended AC and DC Input Levels for CA and CS_n Inputs

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IL,CA(DC)}$	DC input logic low	V_{SSCA}	V_{REF} - 0.100	V	1[a]

a: Refers to Note 1 in Table 33 of the *JEDEC Standard JESD209-3*. For CA and CS_n input only pins. $V_{Ref} = V_{RefCA(DC)}$.

Test References

- See *Table 23 in Section 8.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010,*
- See *Table 4 in Section 3.1 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1, July 2010* and
- See *Table 35 in Section 7 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Obtain sample or acquire signal data.

2 Find all valid negative pulses. A valid negative pulse starts at V_{REF} crossing at valid falling edge and ends at V_{REF} crossing at the following valid rising edge.

3 Zoom in on the first valid negative pulse and perform V_{BASE} measurement. Take the V_{BASE} measurement result as $V_{IL.CA(DC)}$ value.

4 Continue the previous step with another nine valid negative pulses.

5 Determine the worst result from the set of $V_{IL.CA(DC)}$ measured.

Expected/Observable Results

- The low level voltage value of the test signal must be less than or equal to the maximum $V_{IL.CA\ (DC)}$ value.
- b.The high level voltage value of the test signal also shall be not greater than maximum VIH.CA (DC) value which is VDD for DDR3/DDR3L or VDDCA for LPDDR3.

SlewR on Setup Region

Test Overview

The purpose of this test is to calculate the rising slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- No

Signal(s) of Interest

- Command, Address Signals

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire the signal.

2 Find all valid rising edges in the whole acquisition. A valid rising edge starts at VIL (ac) crossing and end at following VIH (ac) crossing.

3 For all valid rising edges, find the transition time, delta TR which is time starts at VREF crossing and end at following VIH (ac) crossing. Then calculate Rising Slew.

$$\text{Rising Slew} = \frac{V_{IH(ac)}\ \text{min} - V_{REF}}{\text{delta TR}}$$

4 Determine the worst result from the set of SlewR measured.

Expected/Observable Results

- The calculated Rising Slew value for the test signal shall meet the user defined limit.

SlewF on Setup Region

Test Overview

The purpose of this test is to calculate the falling slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- No

Signal(s) of Interest

- Command, Address Signals

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire the signal.

2 Find all valid falling edges in the whole acquisition. A valid falling edge starts at VIH (ac) crossing and end at following VIL (ac) crossing.

3 For all valid falling edges, find the transition time, delta TF which is time starts at VREF crossing and end at following VIL (ac) crossing. Then calculate Falling Slew.

$$\text{Falling Slew} = \frac{V_{REF} - V_{IL(ac)}\ \text{max}}{\text{delta TF}}$$

4 Determine the worst result from the set of SlewF measured.

Expected/Observable Results

- The calculated Falling Slew value for the test signal shall meet the user defined limit.

SlewR on Hold Region

Test Overview

The purpose of this test is to calculate the rising slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- No

Signal(s) of Interest

- Command, Address Signals

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire the signal.

2 Find all valid rising edges in the whole acquisition. A valid rising edge starts at VIL (ac) crossing and end at following VIH (ac) crossing.

3 For all valid rising edges, find the transition time, delta TR which is time starts at VIL(DC) crossing and end at following VREF crossing. Then calculate Rising Slew.

$$Rising\ Slew = \frac{V_{REF} - V_{IL(DC)}}{\text{delta TR}}$$

4 Determine the worst result from the set of SlewR measured.

Expected/Observable Results

- The calculated Rising Slew value for the test signal shall meet the user defined limit.

SlewF on Hold Region

Test Overview

The purpose of this test is to calculate the falling slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

NOTE Select **Custom** from the **Test Mode** drop-down options under the **Set Up** tab for this test to appear in the **Select Tests** tab.

Mode Supported

- DDR3 and DDR3L

Signal cycle of interest

- WRITE

Require Read/Write separation

- No

Signal(s) of Interest

- Command, Address Signals

Required Signals that are needed to perform this test on oscilloscope

- Pin Under Test, PUT = any of the signal of interest defined above.

Test References

- There is no available test specification limit of Input Signal Minimum Slew Rate in JEDEC specifications.

Measurement Algorithm

1 Acquire the signal.

2 Find all valid falling edges in the whole acquisition. A valid falling edge starts at VIH (ac) crossing and end at following VIL (ac) crossing.

3 For all valid falling edges, find the transition time, delta TF which is time starts at VIH(DC) crossing and end at following VREF crossing. Then calculate Falling Slew.

$$Falling\ Slew = \frac{V_{IH(DC)} - V_{REF}}{\text{delta TF}}$$

4 Determine the worst result from the set of SlewF measured.

Expected/Observable Results

- The calculated Falling Slew value for the test signal shall meet the user defined limit.

Overshoot Amplitude/Area (Command, Address)

Test Overview

The Overshoot test can be divided into two sub-tests: Overshoot amplitude and Overshoot area.

The purpose of this test is to verify that the overshoot value of the test signal found from all regions of the acquired waveform is lower than or equal to the conformance limit of the maximum peak amplitude allowed for overshoot as specified in the JEDEC specification.

When there is an overshoot, the area is calculated based on the overshoot width and overshoot amplitude. The Overshoot area should be lower than or equal to the conformance limit of the maximum overshoot area allowed as specified in the JEDEC specification.

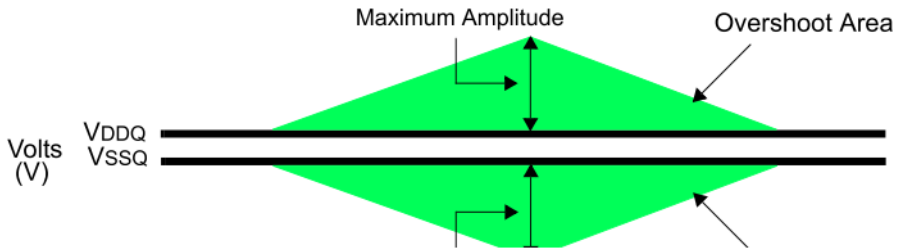

Figure 68 Command Address Overshoot

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Command, Address Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 237 AC Overshoot Specification for Address and Control Pins

Parameter	Specification					
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133
Maximum peak amplitude allowed for overshoot area	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V
Maximum overshoot area above V_{DD}	0.67 V/ns	0.5 V/ns	0.4 V/ns	0.33 V/ns	0.28 V/ns	0.25 V/ns

Table 238 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for overshoot area	Max	0.35		V
Maximum area above V_{DD}	Max	0.12	0.10	V-ns

Test References

- See *Figure 99 and Table 36 in Section 9 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1, July 2010* and
- See *Figure 126 and Table 49 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Set the number of sampling points to 2M samples.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Obtain the overshoot region. Overshoot region starts at the rising VDD (or VDDCA) crossing and ends at the falling VDD (or VDDCA) crossing.

4 Within Overshoot region #1, perform the following steps:

   i Evaluate Overshoot Amplitude by performing the following steps:
   a. Use TMAX and VMAX to get time stamp of maximum voltage on overshoot region of the acquired waveform.
   b. Calculate: Overshoot Amplitude = VMAX – VDD (or VDDCA).

   ii Evaluate Area below VDD (or VDDCA) = (Overshoot Region End – Overshoot Region Start) * VDD (or VDDCA).

   iii Evaluate Total Area above 0 volt by using Trapezoidal Method Area Calculation as shown in following figure:

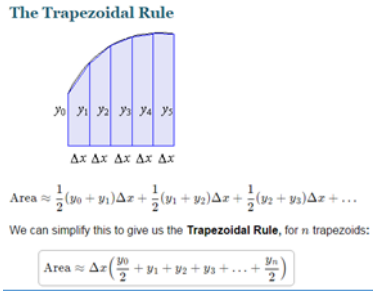

Figure 69 Trapezoidal Rule

iv Calculate area above VDD (or VDDCA) = Total area above 0 volt - area below VDD (or VDDCA).

v Store calculated result below for later worst case finding process:

- Overshoot Amplitude
- Area above VDD (or VDDCA)

5 Repeat the previous step for the rest Overshoot Region found in acquired waveform.

6 Find the worst result below from stored result. Compare test result to the compliance test limit.

- Overshoot Amplitude
- Area above VDD (or VDDCA)

Expected/Observable Results

- The measured maximum voltage value must be less than or equal to the maximum overshoot value.
- The calculated Overshoot area value must be less than or equal to the maximum Overshoot area allowed.

Undershoot Amplitude/Area (Command, Address)

Test Overview

The Undershoot Test can be divided into two sub-tests: Undershoot amplitude and Undershoot area.

The purpose of this test is to verify that the undershoot value of the test signal found from all regions of the acquired waveform is less than or equal to the conformance limit of the maximum peak amplitude allowed for undershoot as specified in the *JEDEC specification*.

When there is an undershoot, the area is calculated based on the undershoot width. The Undershoot area should be less than or equal to the conformance limit of the maximum undershoot area allowed as specified in the *JEDEC specification*.

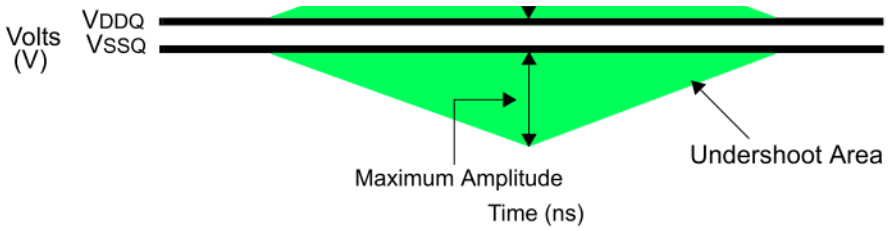

Figure 70 Command, Address Undershoot

Modes Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write separation

- No

Signal(s) of Interest

- Command, Address Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 239 AC Undershoot Specification for Address and Control Pins

Parameter	Specification					
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133
Maximum peak amplitude allowed for undershoot area	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V
Maximum undershoot area below V_{SS}	0.67 V/ns	0.5 V/ns	0.4 V/ns	0.33 V/ns	0.28 V/ns	0.25 V/ns

Table 240 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for undershoot area	Max	0.35		V
Maximum area below V_{SS}	Max	0.12	0.10	V/ns

Test References

- See *Figure 99 and Table 36 in Section 9 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1, July 2010* and
- See *Figure 126 and Table 49 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011*.

Measurement Algorithm

1 Set the number of sampling points to 2M samples.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Obtain the undershoot region. Undershoot Region starts at falling 0 volt crossing and end at rising 0 volt crossing.

4 Within Undershoot region #1, perform the following steps:

   i Evaluate Undershoot Amplitude by performing the following steps:
   a. Use TMIN and VMIN to get time stamp of maximum voltage on undershoot region of the acquired waveform.
   b. Calculate: Undershoot Amplitude = 0 - VMIN

   ii Evaluate total area below 0 volt by using Trapezoidal Method Area Calculation (refer to Figure 69)

   iii Store Calculated result below for later worst case finding process;

   - Undershoot Amplitude
   - Total area below 0 volt

5 Repeat the previous step for the rest Undershoot Region found in acquired waveform.

6 Find the worst result below from stored result. Compare test result to the compliance test limit.

   - Undershoot Amplitude
   - Total area below 0 volt

Expected/Observable Results

- The measured minimum voltage value for the test signal must be less than or equal to the maximum undershoot value.
- The calculated undershoot area value must be less than or equal to the maximum undershoot area allowed.

Timing Tests

tIS(base)

Test Overview

The purpose of this test is to verify that the time interval from the address or control (rising or falling edge) setup time to the associated clock crossing edge is within the conformance limits as specified in the JEDEC Specification.

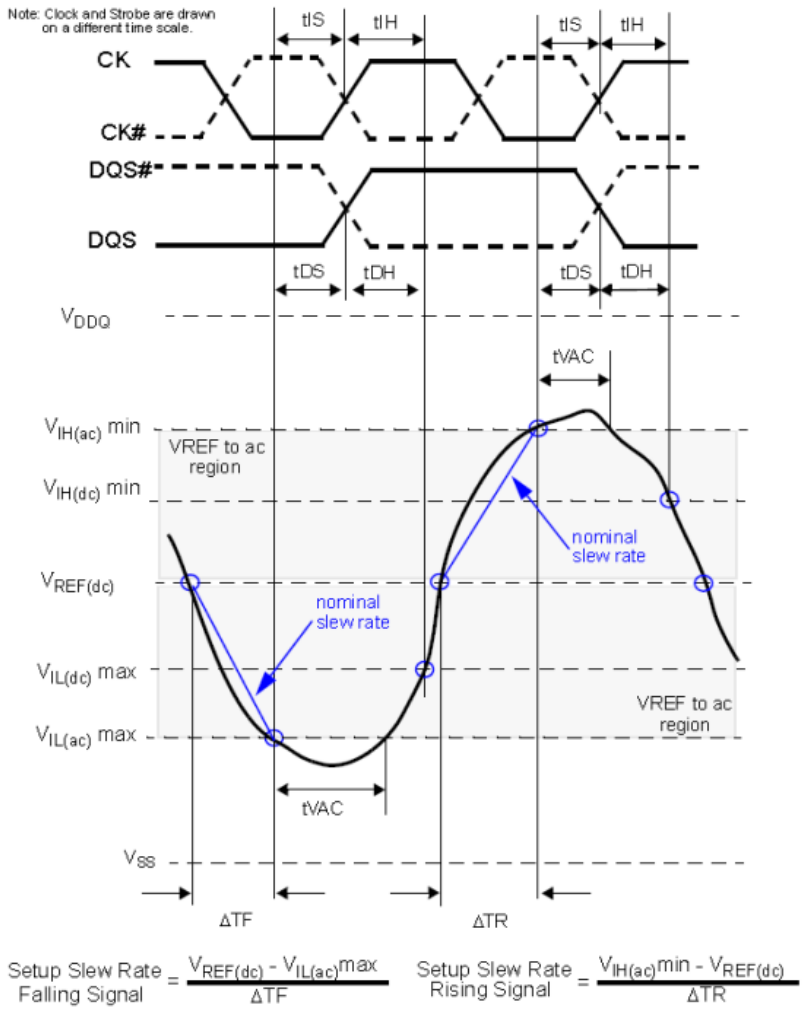

Figure 71 Nominal Slew Rate and t_{VAC} for Setup Time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

Modes Supported

- DDR3 and DDR3L

Signal cycle of Interest

- Write

Require Read/Write separation

- No

Signal(s) of Interest

- Address or Control Signal
- Clock Signal

Signals required to perform the test on the oscilloscope

- Address or Control Signal
- Clock Signal

Test Definition Notes from the Specification

Table 241 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Command and Address setup time to CK, CK# referenced to Vih(ac)/Vil(ac) levels	tIS(base) AC 175	200	-	125	-	65	-	45	-	ps
Command and Address setup time to CK, CK# referenced to Vih(ac)/Vil(ac) levels	tIS(base) AC 150	350	-	275	-	190	-	170	-	ps

Parameter	Symbol	DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	
Command and Address setup time to CK, CK# referenced to Vih(ac)/Vil(ac) levels	tIS(base) AC 150	TBD		TBD		ps
Command and Address setup time to CK, CK# referenced to Vih(ac)/Vil(ac) levels	tIS(base) AC 125	TBD		TBD		ps

Table 242 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Command and Address setup time to CK, CK# referenced to Vih(ac)/Vil(ac) levels	tIS(base) AC 160	215	-	140	-	80	-	60	-	ps
Command and Address setup time to CK, CK# referenced to Vih(ac)/Vil(ac) levels	tIS(base) AC 135	365	-	290	-	205	-	185	-	ps

Test References

- See *Figure 111 and Table 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Table 6 in Section 4 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1 July 2010.*

Measurement Algorithm

1 Precondition the oscilloscope.
2 Trigger on either rising or falling edge of the address/control signal under test.
3 Find all crossings on rising edge of the signal under test that cross $V_{IH(AC)}$.
4 Find all crossings on falling edge of the signal under test that cross $V_{IL(AC)}$.
5 For all crossings found, locate the nearest clock crossing that crosses 0V.
6 Take the time difference between the signal under test's crossing and the corresponding clock crossing as tIS.
7 Collect all measured tIS.
8 Report the worst tIS measured as the test result.
9 Compare the test result against the compliance test limit.

Expected/Observable Results

- The measured time interval between the address/control setup time and the respective clock crossing point must be within the specification limit.

tIH(base)

Test Overview

tIH(base) - Address and Control Input Hold Time. The purpose of this test is to verify that the time interval from the address or control (Addr/Ctrl rising or falling edge) hold time to the associated clock crossing edge is within the conformance limits as specified in the JEDEC Specification.

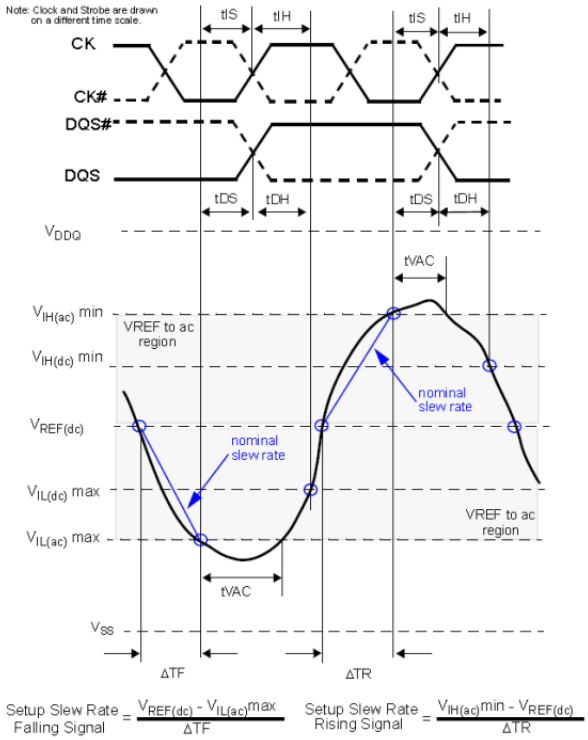

Figure 72 Nominal Slew Rate and t_{VAC} for Setup Time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

Modes Supported

- DDR3 and DDR3L

Signal cycle of Interest

- Write

Require Read/Write separation

- No

Signal(s) of Interest

- Address or Control Signal
- Clock Signal

Signals required to perform the test on the oscilloscope

- Address or Control Signal
- Clock Signal

Test Definition Notes from the Specification

Table 243 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Command and Address setup time from CK, CK# referenced to Vih(dc)/Vil(dc) levels	tIH(base) DC 100	275	-	200	-	140	-	120	-	ps

Parameter	Symbol	DDR3-1866		DDR3-2133		Units
		Min	Max	Min	Max	
Command and Address setup time from CK, CK# referenced to Vih(dc)/Vil(dc) levels	tIH(base) DC 100	TBD		TBD		ps

Table 244 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Command and Address setup time from CK, CK# referenced to Vih(dc)/Vil(dc) levels	tIH(base) DC 90	285	-	210	-	150	-	130	-	ps

Test References

- See *Figure 111 and Table 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Table 6 in Section 4 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1 July 2010.*

Measurement Algorithm

1 Precondition the oscilloscope.
2 Trigger on either rising or falling edge of the address/control signal under test.
3 Find all crossings on rising edge of the signal under test that cross $V_{IL(DC)}$.
4 Find all crossings on falling edge of the signal under test that cross $V_{IH(DC)}$.
5 For all crossings found, locate the nearest Clock crossing that crosses 0V.
6 Take the time difference between the signal under test's crossing and the corresponding clock crossing as tIH.
7 Collect all measured tIH.
8 Report the worst tIH measured as the test result.
9 Compare the test result against the compliance test limit.

Expected/Observable Results

- The measured time interval between the address/control (Add/Ctrl) hold time and the respective clock crossing point must be within the specification limit.

tIS(derate)

Test Overview

The purpose of this test is to verify that the time interval from address or control (Address/Control rising/falling edge) setup time to the associated clock crossing edge must be within the conformance limit as specified in the JEDEC Specification.

Modes Supported

- DDR3 and DDR3L

Signal cycle of Interest

- Write

Require Read/Write separation

- No

Signal(s) of Interest

- Address or Control Signal
- Clock Signal

Signals required to perform the test on the oscilloscope

- Address or Control Signal
- Clock Signal

Test Definition Notes from the Specification

Table 245 ADD/CMD Setup and Hold Base-Value for 1V/ns

Units (ps)	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Reference
tIS (base) AC 175	200	125	65	45	-	-	VIH/L(AC)
tIS (base) AC 150	350	275	190	170	-	-	VIH/L(AC)
tIS (base) AC 135	-	-	-	-	-	-	VIH/L(AC)
tIS (base) AC 125	-	-	-	-	-	-	VIH/L(AC)
tIH (base) DC 100	275	200	140	120	-	-	$V_{IH/L(DC)}$

Table 246 Derating Values DDR3-800/1066/1333/1600 tIS/tIH - AC/DC based Alternate AC 175 Threshold

DtIS, DtIH derating in [ps] AC/DC based Alternate AC 175 Threshold -> VIH(AC) = VREF(DC) + 175 mV, VIL(AC) = VREF(DC) - 175 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		DtIS	DtIH	DtIS	DtIH	DtIS	DtIH	DtIS	DtIH
CMD/ADD Slew Rate V/ns	2.0	88	50	88	50	88	50	96	58
	1.5	59	34	59	34	59	34	67	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-2	-4	-2	-4	-2	-4	6	4
	0.8	-6	-10	-6	-10	-6	-10	2	-2
	0.7	-11	-16	-11	-16	-11	-16	-3	-8
	0.6	-17	-26	-17	-26	-17	-26	-9	-18
	0.5	-35	-40	-35	-40	-35	-40	-27	-32
	0.4	-62	-60	-62	-60	-62	-60	-54	-52

DtIS, DtIH derating in [ps] AC/DC based Alternate AC 175 Threshold -> VIH(AC) = VREF(DC) + 175 mV, VIL(AC) = VREF(DC) - 175 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		DtIS	DtIH	DtIS	DtIH	DtIS	DtIH	DtIS	DtIH
CMD/ADD Slew Rate V/ns	2.0	104	66	112	74	120	84	128	100
	1.5	75	50	83	58	91	68	99	84
	1.0	16	16	24	24	32	34	40	50
	0.9	14	12	22	20	30	30	38	46
	0.8	10	6	18	14	26	24	34	40
	0.7	5	0	13	8	21	18	29	34
	0.6	-1	-10	7	-2	15	8	23	24
	0.5	-19	-24	-11	-16	-2	-6	5	10
	0.4	-46	-44	-38	-36	-30	-26	-22	-10

Table 247 Derating Values DDR3-800/1066/1333/1600 tIS/tIH - AC/DC based Alternate AC 150 Threshold

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	75	50	75	50	75	50	83	58
	1.5	50	34	50	34	50	34	58	42
	1.0	0	0	0	0	0	0	8	8
	0.9	0	-4	0	-4	0	-4	8	4
	0.8	0	-10	0	-10	0	-10	8	-2
	0.7	0	-16	0	-16	0	-16	8	-8
	0.6	-1	-26	-1	-26	-1	-26	7	-18
	0.5	-10	-40	-10	-40	-10	-40	-2	-32
	0.4	-25	-60	-25	-60	-25	-60	-17	-52

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	91	66	99	74	107	84	115	100
	1.5	66	50	74	58	82	68	90	84
	1.0	16	16	24	24	32	34	40	50
	0.9	16	12	24	20	32	30	40	46
	0.8	16	6	24	14	32	24	40	40
	0.7	16	0	24	8	32	18	40	34
	0.6	-15	-10	23	-2	31	8	39	24
	0.5	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	7	-26	15	-10

Table 248 Derating Values DDR3-1866/2133 tIS/tIH - AC/DC based Alternate AC 135 Threshold

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	68	50	68	50	68	50	76	58
	1.5	45	34	45	34	45	34	53	42
	1.0	0	0	0	0	0	0	8	8
	0.9	2	-4	2	-4	2	-4	10	4
	0.8	3	-10	3	-10	3	-10	11	-2
	0.7	6	-16	6	-16	6	-16	14	-8
	0.6	9	-26	9	-26	9	-26	17	-18
	0.5	5	-40	5	-40	5	-40	13	-32
	0.4	-3	-60	-3	-60	-3	-60	6	-52

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	84	66	92	74	100	84	108	100
	1.5	61	50	69	58	77	68	85	84
	1.0	16	16	24	24	32	34	40	50
	0.9	18	12	26	20	34	30	42	46
	0.8	19	6	27	14	35	24	43	40
	0.7	22	0	30	8	38	18	46	34
	0.6	25	-10	33	-2	41	8	49	24
	0.5	21	-24	29	-16	37	-6	45	10
	0.4	14	-44	22	-36	30	-26	38	-10

Table 249 Derating Values DDR3-1866/2133 tIS/tIH - AC/DC based Alternate AC 125 Threshold

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 125 Threshold -> VIH(AC) = VREF(DC) + 125 mV, VIL(AC) = VREF(DC) - 125 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	63	50	63	50	63	50	71	58
	1.5	42	34	42	34	42	34	50	42
	1.0	0	0	0	0	0	0	8	8
	0.9	4	-4	4	-4	4	-4	12	4
	0.8	6	-10	6	-10	6	-10	14	-2
	0.7	11	-16	11	-16	11	-16	19	-8
	0.6	16	-26	16	-26	16	-26	24	-18
	0.5	15	-40	15	-40	15	-40	23	-32
	0.4	13	-60	13	-60	13	-60	32	-52

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 125 Threshold -> VIH(AC) = VREF(DC) + 125 mV, VIL(AC) = VREF(DC) - 125 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	79	66	87	74	95	84	103	100
	1.5	58	50	66	58	74	68	82	84
	1.0	16	16	24	24	32	34	40	50
	0.9	20	12	28	20	36	30	44	46
	0.8	22	6	30	14	38	24	46	40
	0.7	27	0	35	8	43	18	51	34
	0.6	32	-10	40	-2	48	8	56	24
	0.5	31	-24	39	-16	47	-6	55	10
	0.4	29	-44	37	-36	45	-26	53	-10

Table 250 ADD/CMD Setup and Hold Base-Value for 1V/ns

Units (ps)	DDR3L-800	DDR3L-1066	DDR3L-1333	DDR3L-1600	Reference
tIS (base) AC 150	215	140	80	60	$V_{IH/L(AC)}$
tIS (base) AC 135	365	290	205	185	$V_{IH/L(AC)}$
tIH (base) DC 100	285	210	150	130	$V_{IH/L(DC)}$

Table 251 Derating Values DDR3-800/1066 tIS/tIH - AC/DC based Alternate AC 160 Threshold

ΔtIS, ΔtIH derating in [ps] AC/DC based AC 160 Threshold -> VIH(AC) = VREF(DC) + 160 mV, VIL(AC) = VREF(DC) - 160 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ Slew Rate V/ns	2.0	80	45	80	45	80	45	-	-
	1.5	53	30	53	30	53	30	58	38
	1.0	0	0	0	0	0	0	8	8
	0.9	-1	-3	-1	-3	-1	-3	7	5
	0.8	-3	-8	-3	-8	-3	-8	5	1
	0.7	-5	-13	-5	-13	-5	-13	3	-5
	0.6	-8	-20	-8	-20	-8	-20	0	-12
	0.5	-20	-30	-20	-30	-20	-30	-12	-22
	0.4	-40	-45	-40	-45	-40	-45	-32	-37

ΔtIS, ΔtIH derating in [ps] AC/DC based AC 160 Threshold -> VIH(AC) = VREF(DC) + 160 mV, VIL(AC) = VREF(DC) - 160 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ Slew Rate V/ns	2.0	96	61	104	69	112	79	120	95
	1.5	69	46	77	54	85	64	93	80
	1.0	16	16	24	24	32	34	40	50
	0.9	15	13	23	21	31	31	39	47
	0.8	13	9	21	17	29	27	37	43
	0.7	11	3	19	11	27	21	35	37
	0.6	8	-4	16	4	24	14	32	30
	0.5	-4	-14	4	-6	12	4	20	20
	0.4	-24	-29	-16	-21	-8	-11	0	5

Table 252 Derating Values DDR3-800/1066/1333/1600 tIS/tIH - AC/DC based Alternate AC 135 Threshold

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ Slew Rate V/ns	2.0	68	45	68	45	68	45	-	-
	1.5	45	30	45	30	45	30	53	38
	1.0	0	0	0	0	0	0	8	8
	0.9	2	-3	2	-3	2	-3	10	5
	0.8	3	-8	3	-8	3	-8	11	1
	0.7	6	-13	6	-13	6	-13	14	-5
	0.6	9	-20	9	-20	9	-20	17	-12
	0.5	5	-30	5	-30	5	-30	13	-22
	0.4	-3	-45	-3	-45	-3	-45	6	-37

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ Slew Rate V/ns	2.0	84	61	92	69	100	79	108	95
	1.5	61	46	69	54	77	64	85	80
	1.0	16	16	24	24	32	34	40	50
	0.9	18	13	26	21	34	31	42	47
	0.8	19	9	27	17	35	27	43	43
	0.7	22	3	30	11	38	21	46	37
	0.6	25	-4	33	4	41	14	49	30
	0.5	21	-14	29	-6	37	4	45	20
	0.4	14	-29	22	-21	30	-11	38	5

Test References

- *See Figure 111 & 113 and Table 70 to 74 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- *See Table 7 to 9 in Section 4 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1 July 2010.*

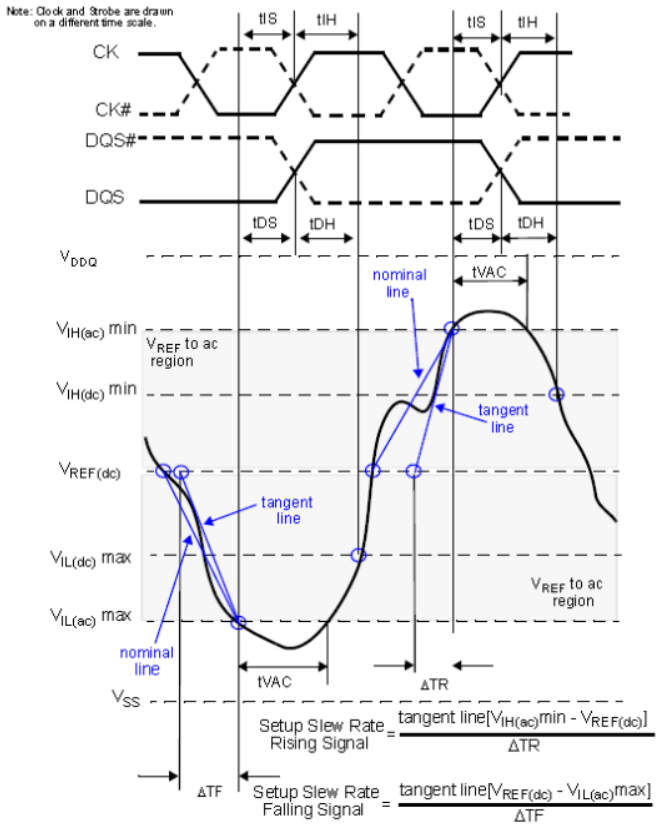

Figure 73 Tangent Line for Setup Time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

Measurement Algorithm

1 Precondition the oscilloscope.
2 Trigger on either rising or falling edge of the address/control signal under test.
3 Find all crossings on rising edge of the signal under test that cross $V_{IH(AC)}$.
4 Find all crossings on falling edge of the signal under test that cross $V_{Il(AC)}$.
5 For all crossings found, locate the nearest Clock crossing that crosses 0V.
6 Take the time difference between the signal under test's crossing and the corresponding clock crossing as tIS.
7 Collect all measured tIS.
8 Report the worst tIS measured as the test result.
9 Measure the mean slew rate for all the ADD/CMD and CK edges.
10 Use the mean slew rate for ADD/CMD and CK to determine the ΔtIS derating value based on the derating table.
11 The test limit for tIS test = tIS(base) + ΔtIS.

Expected/Observable Results

- The measured time interval between address/control (Add/Ctrl) setup time to respective clock crossing point must be within the specification limit.

tIH(derate)

Test Overview

The purpose of this test is to verify that the time interval from address or control (Add/Ctrl rising/falling edge) hold time to the associated clock crossing edge must be within the conformance limit as specified in the JEDEC Specification.

Modes Supported

- DDR3 and DDR3L

Signal cycle of Interest

- Write

Require Read/Write separation

- No

Signal(s) of Interest

- Address or Control Signal
- Clock Signal

Signals required to perform the test on the oscilloscope

- Address or Control Signal
- Clock Signal

Test Definition Notes from the Specification

Table 253 ADD/CMD Setup and Hold Base-Value for 1V/ns

Units (ps)	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Reference
tIS (base) AC 175	200	125	65	45	-	-	$V_{IH/L(AC)}$
tIS (base) AC 150	350	275	190	170	-	-	$V_{IH/L(AC)}$
tIS (base) AC 135	-	-	-	-	-	-	$V_{IH/L(AC)}$
tIS (base) AC 125	-	-	-	-			$V_{IH/L(AC)}$
tIH (base) DC 100	275	200	140	120	-	-	$V_{IH/L(DC)}$

Table 254 Derating Values DDR3-800/1066/1333/1600 tIS/tIH - AC/DC based Alternate AC 175 Threshold

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 175 Threshold -> VIH(AC) = VREF(DC) + 175 mV, VIL(AC) = VREF(DC) - 175 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	88	50	88	50	88	50	96	58
	1.5	59	34	59	34	59	34	67	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-2	-4	-2	-4	-2	-4	6	4
	0.8	-6	-10	-6	-10	-6	-10	2	-2
	0.7	-11	-16	-11	-16	-11	-16	-3	-8
	0.6	-17	-26	-17	-26	-17	-26	-9	-18
	0.5	-35	-40	-35	-40	-35	-40	-27	-32
	0.4	-62	-60	-62	-60	-62	-60	-54	-52

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 175 Threshold -> VIH(AC) = VREF(DC) + 175 mV, VIL(AC) = VREF(DC) - 175 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	104	66	112	74	120	84	128	100
	1.5	75	50	83	58	91	68	99	84
	1.0	16	16	24	24	32	34	40	50
	0.9	14	12	22	20	30	30	38	46
	0.8	10	6	18	14	26	24	34	40
	0.7	5	0	13	8	21	18	29	34
	0.6	-1	-10	7	-2	15	8	23	24
	0.5	-19	-24	-11	-16	-2	-6	5	10
	0.4	-46	-44	-38	-36	-30	-26	-22	-10

Table 255 Derating Values DDR3-800/1066/1333/1600 tIS/tIH - AC/DC based Alternate AC 150 Threshold

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	75	50	75	50	75	50	83	58
	1.5	50	34	50	34	50	34	58	42
	1.0	0	0	0	0	0	0	8	8
	0.9	0	-4	0	-4	0	-4	8	4
	0.8	0	-10	0	-10	0	-10	8	-2
	0.7	0	-16	0	-16	0	-16	8	-8
	0.6	-1	-26	-1	-26	-1	-26	7	-18
	0.5	-10	-40	-10	-40	-10	-40	-2	-32
	0.4	-25	-60	-25	-60	-25	-60	-17	-52

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	91	66	99	74	107	84	115	100
	1.5	66	50	74	58	82	68	90	84
	1.0	16	16	24	24	32	34	40	50
	0.9	16	12	24	20	32	30	40	46
	0.8	16	6	24	14	32	24	40	40
	0.7	16	0	24	8	32	18	40	34
	0.6	-15	-10	23	-2	31	8	39	24
	0.5	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	7	-26	15	-10

Table 256 Derating Values DDR3-1866/2133 tIS/tIH - AC/DC based Alternate AC 135 Threshold

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	68	50	68	50	68	50	76	58
	1.5	45	34	45	34	45	34	53	42
	1.0	0	0	0	0	0	0	8	8
	0.9	2	-4	2	-4	2	-4	10	4
	0.8	3	-10	3	-10	3	-10	11	-2
	0.7	6	-16	6	-16	6	-16	14	-8
	0.6	9	-26	9	-26	9	-26	17	-18
	0.5	5	-40	5	-40	5	-40	13	-32
	0.4	-3	-60	-3	-60	-3	-60	6	-52

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	84	66	92	74	100	84	108	100
	1.5	61	50	69	58	77	68	85	84
	1.0	16	16	24	24	32	34	40	50
	0.9	18	12	26	20	34	30	42	46
	0.8	19	6	27	14	35	24	43	40
	0.7	22	0	30	8	38	18	46	34
	0.6	25	-10	33	-2	41	8	49	24
	0.5	21	-24	29	-16	37	-6	45	10
	0.4	14	-44	22	-36	30	-26	38	-10

Table 257 Derating Values DDR3-1866/2133 tIS/tIH - AC/DC based Alternate AC 125 Threshold

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 125 Threshold -> VIH(AC) = VREF(DC) + 125 mV, VIL(AC) = VREF(DC) - 125 mV									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	63	50	63	50	63	50	71	58
	1.5	42	34	42	34	42	34	50	42
	1.0	0	0	0	0	0	0	8	8
	0.9	4	-4	4	-4	4	-4	12	4
	0.8	6	-10	6	-10	6	-10	14	-2
	0.7	11	-16	11	-16	11	-16	19	-8
	0.6	16	-26	16	-26	16	-26	24	-18
	0.5	15	-40	15	-40	15	-40	23	-32
	0.4	13	-60	13	-60	13	-60	32	-52

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 125 Threshold -> VIH(AC) = VREF(DC) + 125 mV, VIL(AC) = VREF(DC) - 125 mV									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	79	66	87	74	95	84	103	100
	1.5	58	50	66	58	74	68	82	84
	1.0	16	16	24	24	32	34	40	50
	0.9	20	12	28	20	36	30	44	46
	0.8	22	6	30	14	38	24	46	40
	0.7	27	0	35	8	43	18	51	34
	0.6	32	-10	40	-2	48	8	56	24
	0.5	31	-24	39	-16	47	-6	55	10
	0.4	29	-44	37	-36	45	-26	53	-10

Table 258 ADD/CMD Setup and Hold Base-Value for 1V/ns

Units (ps)	DDR3L-800	DDR3L-1066	DDR3L-1333	DDR3L-1600	Reference
tIS (base) AC 150	215	140	80	60	$V_{IH/L(AC)}$
tIS (base) AC 135	365	290	205	185	$V_{IH/L(AC)}$
tIH (base) DC 100	285	210	150	130	$V_{IH/L(DC)}$

Table 259 Derating Values DDR3-800/1066 tIS/tIH - AC/DC based Alternate AC 160 Threshold

ΔtIS, ΔtIH derating in [ps] AC/DC based AC 160 Threshold -> VIH(AC) = VREF(DC) + 160 mV, VIL(AC) = VREF(DC) - 160 mV									
		CK, CK# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	80	45	80	45	80	45	-	-
	1.5	53	30	53	30	53	30	58	38
	1.0	0	0	0	0	0	0	8	8
	0.9	-1	-3	-1	-3	-1	-3	7	5
	0.8	-3	-8	-3	-8	-3	-8	5	1
	0.7	-5	-13	-5	-13	-5	-13	3	-5
	0.6	-8	-20	-8	-20	-8	-20	0	-12
	0.5	-20	-30	-20	-30	-20	-30	-12	-22
	0.4	-40	-45	-40	-45	-40	-45	-32	-37

ΔtIS, ΔtIH derating in [ps] AC/DC based AC 160 Threshold -> VIH(AC) = VREF(DC) + 160 mV, VIL(AC) = VREF(DC) - 160 mV									
		CK, CK# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	96	61	104	69	112	79	120	95
	1.5	69	46	77	54	85	64	93	80
	1.0	16	16	24	24	32	34	40	50
	0.9	15	13	23	21	31	31	39	47
	0.8	13	9	21	17	29	27	37	43
	0.7	11	3	19	11	27	21	35	37
	0.6	8	-4	16	4	24	14	32	30
	0.5	-4	-14	4	-6	12	4	20	20
	0.4	-24	-29	-16	-21	-8	-11	0	5

Table 260 Derating Values DDR3L-800/1066/1333/1600 tIS/tIH - AC/DC based Alternate AC 135 Threshold

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		CK, CK# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	68	45	68	45	68	45	-	-
	1.5	45	30	45	30	45	30	53	38
	1.0	0	0	0	0	0	0	8	8
	0.9	2	-3	2	-3	2	-3	10	5
	0.8	3	-8	3	-8	3	-8	11	1
	0.7	6	-13	6	-13	6	-13	14	-5
	0.6	9	-20	9	-20	9	-20	17	-12
	0.5	5	-30	5	-30	5	-30	13	-22
	0.4	-3	-45	-3	-45	-3	-45	6	-37

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC 135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV									
		CK, CK# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	84	61	92	69	100	79	108	95
	1.5	61	46	69	54	77	64	85	80
	1.0	16	16	24	24	32	34	40	50
	0.9	18	13	26	21	34	31	42	47
	0.8	19	9	27	17	35	27	43	43
	0.7	22	3	30	11	38	21	46	37
	0.6	25	-4	33	4	41	14	49	30
	0.5	21	-14	29	-6	37	4	45	20
	0.4	14	-29	22	-21	30	-11	38	5

Table 261 CA and CS_n Setup and Hold Base-Values for 2V/ns

[ps]	Data Rate		Reference
	1600	1333	
tIH(base)	100	125	VIH/L(DC) = VREF(DC) ± 100mV

Table 262 Derating Values tIS/tIH - AC/DC based AC 150

ΔtISCA, ΔtIHCA, ΔtISCS, ΔtIHCS derating in [ps] AC/DC based AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV DC 100 Threshold -> VIH(DC) = VREF(DC) + 100 mV, VIL(DC) = VREF(DC) - 100 mV									
		CK_t, CK_c Differential Slew Rate							
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew Rate V/ns	4.0	38	25	38	25	38	25	-	-
	3.5	32	21	32	21	32	21	32	21
	3.0	25	17	25	17	25	17	25	17
	2.5	-	-	15	10	15	10	15	10
	2.0	-	-	-	-	0	0	0	0
	1.5	-	-	-	-	-	-	-25	-17
	1.0	-	-	-	-	-	-	-	-

NOTE 1. Empty cell contents are defined as not supported.

ΔtISCA, ΔtIHCA, ΔtISCS, ΔtIHCS derating in [ps] AC/DC based AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV DC 100 Threshold -> VIH(DC) = VREF(DC) + 100 mV, VIL(DC) = VREF(DC) - 100 mV							
		CK_t, CK_c Differential Slew Rate					
		4.0V/ns		3.0V/ns		2.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew Rate V/ns	4.0	-	-	-	-	-	-
	3.5	-	-	-	-	-	-
	3.0	25	17	-	-	-	-
	2.5	15	10	15	10	-	-
	2.0	0	0	0	0	0	0
	1.5	-25	-17	-25	-17	-25	-17
	1.0	-75	-50	-75	-50	-75	-50

NOTE 1. Empty cell contents are defined as not supported.

Test References

- See *Figure 112 &114 and Table 70 to 74 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3E, July 2010* and
- See *Table 4 in Section 7 to 9 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3-1 July 2010.*

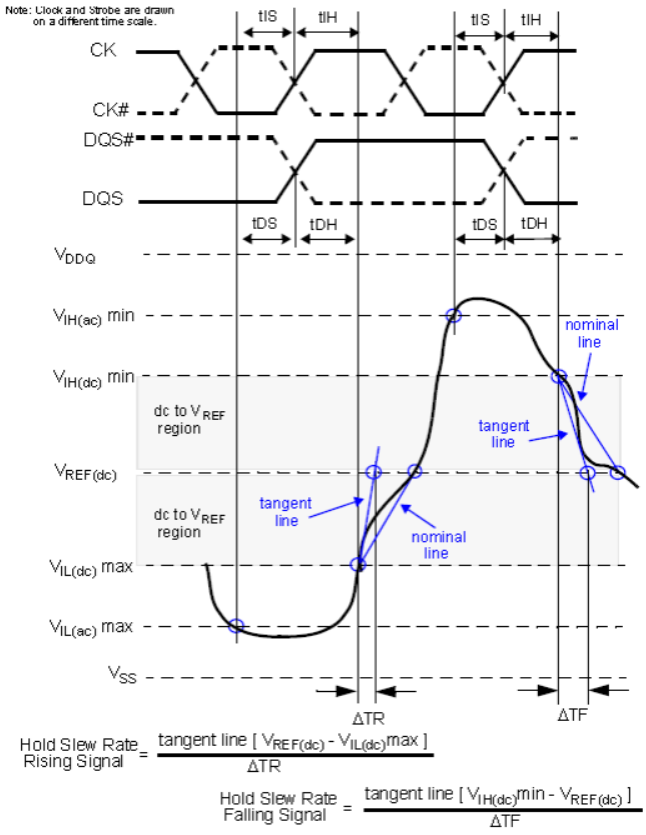

Figure 74 Tangent Line for Setup Time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

Measurement Algorithm

1 Precondition the oscilloscope.
2 Triggered on either rising or falling edge of the address/control signal under test.
3 Find all crossings on rising edge of the signal under test that cross Vil(dc).
4 Find all crossings on falling edge of the signal under test that cross Vih(dc).
5 For all the crossings found, locate the nearest Clock crossings that cross 0V.
6 Take the time different of the signal under test's crossings to the corresponding clock crossing as tIH.
7 Collect all measured tIH.
8 Report the worst tIH measured as test result.
9 Measure the mean slew rate for all the ADD/CMD and CK edges.

Expected/Observable Results

- Use the mean slew rate for ADD/CMD and CK to determine the ΔtIH derating value based on the derating tables.
- The test limit for tIH test = tIH(base) + ΔtIH.

tISCA(base)

Test Overview

The purpose of this test is to verify that the time interval from command/address (command/address rising/falling edge) setup time to the associated clock crossing edge must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Write

Require Read/Write separation

- No

Signal(s) of Interest

- Command/Address Inputs Signal
- Clock Signal

Signals required to perform the test on the oscilloscope

- Command/Address Inputs Signal
- Clock Signal

Test Definition Notes from the Specification

Table 263 CA Setup and Hold Base Values

unit [ps]	Data Rate				reference
	1333	1600	1866	2133	
$t_{ISCA(base)}$	100	75	-	-	$V_{IH/L(ac)} = V_{REF(dc)}$ +/- 150mV
$t_{ISCA(base)}$	-	-	62.5	47.5	$V_{IH/L(ac)} = V_{REF(dc)}$ +/- 135mV

Test References

- See *Figure 5, 77, 78, 79 & 80 and Table 65 in the Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3B, August 2013.*

Measurement Algorithm

1 Precondition the oscilloscope.
2 Trigger on either rising or falling edge of the command/address signal under test.
3 Find all crossings on rising edge of the signal under test that cross $V_{IH(AC)}$.
4 Find all crossings on falling edge of the signal under test that cross $V_{IL(AC)}$.
5 For all the crossings found, locate the nearest Clock crossing that crosses 0V.
6 Take the time difference between the signal under test's crossing and the corresponding clock crossing as tISCA.
7 Collect all measured tISCA.
8 Report the worst tISCA measured as the test result.
9 Compare the test result against the compliance test limit.

Expected/Observable Results

- The measured time interval between the command/address setup time to respective clock crossing point must be within the specification limit.

tIHCA(base)

Test Overview

The purpose of this test is to verify that the time interval from command/address (command/address rising/falling edge) hold time to the associated clock crossing edge must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Write

Require Read/Write separation

- No

Signal(s) of Interest

- Command/Address Inputs Signal
- Clock Signal

Signals required to perform the test on the oscilloscope

- Command/Address Inputs Signal
- Clock Signal

Test Definition Notes from the Specification

Table 264 CA Setup and Hold Base Values

unit [ps]	Data Rate				Reference
	1333	1600	1866	2133	
$t_{IHCA(base)}$	125	100	80	65	$V_{IH/L(dc)} = V_{REF(dc)}$ +/- 100mV

Test References

- See *Figure 5, 77, 78, 79 & 80 and Table 65 in the Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3B, August 2013.*

Measurement Algorithm

1 Precondition the oscilloscope.
2 Trigger on either rising or falling edge of the command/address signal under test.
3 Find all crossings on rising edge of the signal under test that cross $V_{IL(DC)}$.
4 Find all crossings on falling edge of the signal under test that cross $V_{IH(DC)}$.
5 For all the crossings found, locate the nearest Clock crossing that crosses 0V.
6 Take the time difference between the signal under test's crossing and the corresponding clock crossing as tIHCA.
7 Collect all measured tIHCA.
8 Report the worst tIHCA measured as the test result.
9 Compare the test result against the compliance test limit.

Expected/Observable Results

- The measured time interval between the command/address hold time to respective clock crossing point must be within the specification limit.

tISCA(derate)

Test Overview

The purpose of this test is to verify that the time interval from Command/Address (Command/Address rising/falling edge) setup time to the associated clock crossing edge must be within the conformance limit as specified in the JEDEC Specification.

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Write

Require Read/Write separation

- No

Signal(s) of Interest

- Command/Address Inputs Signal
- Clock Signal

Signals required to perform the test on the oscilloscope

- Command/Address Inputs Signal
- Clock Signal

Test Definition Notes from the Specification

Table 265 CA Setup and Hold Base Values

unit [ps]	Data Rate				reference
	1333	1600	1866	2133	
$t_{ISCA(base)}$	100	75	-	-	$V_{IH/L(ac)} = V_{REF(dc)}$ +/- 150mV
$t_{ISCA(base)}$	-	-	62.5	47.5	$V_{IH/L(ac)} = V_{REF(dc)}$ +/- 135mV

Table 266 Derating values tIS/tIH - ac/dc based AC15

Δt_{ISCA}, Δt_{IHCA}, Δt_{ISCS}, Δt_{IHCS} derating in [ps] AC/DC based
AC 150 Threshold -> $V_{IH(ac)} = V_{REF(dc)}$ + 150 mV, $V_{IL(ac)} = V_{REF(dc)}$ - 150 mV
DC 100 Threshold -> $V_{IH(dc)} = V_{REF(DC)}$ + 100 mV, $V_{IL(dc)} = V_{REF(dc)}$ - 100 mV

		CK_t, CK_c Differential Slew Rate											
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew Rate V/ns	4.0	38	25	38	25	38	25	38	25	38	25	-	-
	3.0	-	-	25	17	25	17	25	17	25	17	38	29
	2.0	-	-	-	-	0	0	0	0	0	0	13	13
	1.5	-	-	-	-	-	-	-25	-17	-25	-17	-12	-4

NOTE 1. Empty cell contents are defined as not supported.

Table 267 Derating values tIS/tIH - ac/dc based AC135

Δt_{ISCA}, Δt_{IHCA}, Δt_{ISCS}, Δt_{IHCS} derating in [ps] AC/DC based AC 135 Threshold -> $V_{IH(ac)} = V_{REF(dc)} + 135$ mV, $V_{IL(ac)} = V_{REF(dc)} - 135$ mV DC 100 Threshold -> $V_{IH(dc)} = V_{REF(DC)} + 100$ mV, $V_{IL(dc)} = V_{REF(dc)} - 100$ mV												
		CK_t, CK_c Differential Slew Rate											
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew Rate V/ns	4.0	34	25	34	25	34	25	34	25	34	25	-	-
	3.0	-	-	23	17	23	17	23	17	23	17	34	29
	2.0	-	-	-	-	0	0	0	0	0	0	11	13
	1.5	-	-	-	-	-	-	-23	-17	-23	-17	12	-4

NOTE 1. Empty cell contents are defined as not supported.

Test References

- See *Figure 5, 77, 78, 79 & 80 and Table 65, 67 & 68 in the Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3B, August 2013.*

Measurement Algorithm

1 Precondition the oscilloscope.
2 Trigger on either rising or falling edge of the Command/Address signal under test.
3 Find all crossings on rising edge of the signal under test that cross $V_{IH(AC)}$.
4 Find all crossings on falling edge of the signal under test that cross $V_{IL(AC)}$.
5 For all the crossings found, locate the nearest Clock crossing that crosses 0V.
6 Take the time difference between the signal under test's crossing and the corresponding clock crossing as tISCA.
7 Collect all measured tISCA.
8 Report the worst tISCA measured as the test result.
9 Measure the mean slew rate for Command/Address and CK edges.
10 Use the mean slew rate for Command/Address and CK to determine the ΔtIS derating value based on the derating tables.
11 The test limit for tISCA test - tISCA (base) + ΔtIS

Expected/Observable Results

- The measured time interval between the command/address setup time to respective clock crossing point must be within the specification limit.

tIHCA(derate)

Test Overview

The purpose of this test is to verify that the time interval from Command/Address (Command/Address rising/falling edge) hold time to the associated clock crossing edge must be within the conformance limit as specified in the JEDEC Specification.

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Write

Require Read/Write separation

- No

Signal(s) of Interest

- Command/Address Inputs Signal
- Clock Signal

Signals required to perform the test on the oscilloscope

- Command/Address Inputs Signal
- Clock Signal

Test Definition Notes from the Specification

Table 268 CA Setup and Hold Base Values

unit [ps]	Data Rate				reference
	1333	1600	1866	2133	
$t_{IHCA(base)}$	125	100	80	65	$V_{IH/L(dc)} = V_{REF(dc)}$ +/- 100mV

Table 269 Derating values tIS/tIH - ac/dc based AC150

$\Delta t_{ISCA}, \Delta t_{IHCA}, \Delta t_{ISCS}, \Delta t_{IHCS}$ derating in [ps] AC/DC based AC 150 Threshold -> $V_{IH(ac)} = V_{REF(dc)}$ + 150 mV, $V_{IL(ac)} = V_{REF(dc)}$ - 150 mV DC 100 Threshold -> $V_{IH(dc)} = V_{REF(dc)}$ + 100 mV, $V_{IL(dc)} = V_{REF(dc)}$ - 100 mV													
		CK_t, CK_c Differential Slew Rate											
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew Rate V/ns	4.0	38	25	38	25	38	25	38	25	38	25	-	-
	3.0	-	-	25	17	25	17	25	17	25	17	38	29
	2.0	-	-	-	-	0	0	0	0	0	0	13	13
	1.5	-	-	-	-	-	-	-25	-17	-25	-17	-12	-4

NOTE 1. Empty cell contents are defined as not supported.

Table 270 Derating values tIS/tIH - ac/dc based AC135

Δt_{ISCA}, Δt_{IHCA}, Δt_{ISCS}, Δt_{IHCS} derating in [ps] AC/DC based AC 135 Threshold -> $V_{IH(ac)} = V_{REF(dc)} + 135$ mV, $V_{IL(ac)} = V_{REF(dc)} - 135$ mV DC 100 Threshold -> $V_{IH(dc)} = V_{REF(dc)} + 100$ mV, $V_{IL(dc)} = V_{REF(dc)} - 100$ mV												
		CK_t, CK_c Differential Slew Rate											
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew Rate V/ns	4.0	34	25	34	25	34	25	34	25	34	25	-	-
	3.0	-	-	23	17	23	17	23	17	23	17	34	29
	2.0	-	-	-	-	0	0	0	0	0	0	11	13
	1.5	-	-	-	-	-	-	-23	-17	-23	-17	-12	-4

NOTE 1. Empty cell contents are defined as not supported.

Test References

- See *Figure 5, 77, 78, 79 & 80 and Table 65, 67 & 68 in the Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3B, August 2013.*

Measurement Algorithm

1 Precondition the oscilloscope.

2 Trigger on either rising or falling edge of the Command/Address signal under test.

3 Find all crossings on rising edge of the signal under test that cross $V_{IL(DC)}$.

4 Find all crossings on falling edge of the signal under test that cross $V_{IH(DC)}$.

5 For all the crossings found, locate the nearest Clock crossing that crosses 0V.

6 Take the time difference between the signal under test's crossing and the corresponding clock crossing as tIHCA.

7 Collect all measured tIHCA.

8 Report the worst tIHCA measured as the test result.

9 Measure the mean slew rate for Command/Address and CK edges.

10 Use the mean slew rate for Command/Address and CK to determine the ΔtIH derating value based on the derating tables.

11 The test limit for tIHCA test - tIHCA (base) + ΔtIH

Expected/Observable Results

- The measured time interval between the command/address hold time to respective clock crossing point must be within the specification limit.

tIPW

Test Overview

The purpose of this test is to verify that the width of the high or low level of address or control signal must be within the conformance limit as specified in the JEDEC Specification.

Modes Supported

- DDR3 and DDR3L

Signal cycle of Interest

- Write

Require Read/Write separation

- No

Signal(s) of Interest

- Address Signal or Control Signal

Signals required to perform the test on the oscilloscope

- Address Signal or Control Signal

Test Definition Notes from the Specification

Table 271 Timing Parameters by Speed Bin (Cont'd)

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Control and Input pulse width for each input	tIPW	900	-	780	-	620	-	560	-	ps	28

Table 272 Timing Parameters by Speed Bin (Cont'd)

Parameter	Symbol	DDR3-1866		DDR3-2133		Units	Notes
		Min	Max	Min	Max		
Control and Input pulse width for each input	tIPW	535	-	470	-	-ps	28

Test References

- *See Table 68 & 69 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3F July 2012.*

Measurement Algorithm

1. Precondition the oscilloscope.
2. Trigger on either rising or falling edge of the address or control signal under test.
3. Find all crossings on rising/falling edge of the signal under test that cross Vref.
4. tIPW is the time started from a rising/falling edge of the signal under test and ended at the following falling/rising (following edge should not be in the same direction) edge.
5. Collect all tIPW.
6. Determine the worst result from the set of tIPW measured.

Expected/Observable Results

- The worst measured tIPW must be within the specification limit.

tIPWCA

Test Overview

The purpose of this test is to verify that the width of the high or low level of Command/Address signal must be within the conformance limit as specified in the JEDEC Specification.

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Write

Require Read/Write separation

- No

Signal(s) of Interest

- Command/Address Signal

Signals required to perform the test on the oscilloscope

- Command/Address Inputs Signal

Test Definition Notes from the Specification

Table 273 AC Timing (cont'd)

Parameter	Symbol	Min/Max	Data Rate				Unit
			1333	1600	1866	2133	
Command Address Input Parameters[5]							
Address and Control Input Pulse Width	t_{IPWCA}	MIN		0.35			$t_{CK(avg)}$

Test References

- See *Table 64 in the Section 11 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3B, August 2013*.

Measurement Algorithm

1 Precondition the oscilloscope.
2 Trigger on either rising or falling edge of the Command/Address signal under test.
3 Find all crossings on rising/falling edge of the signal under test that cross Vref.
4 tIPWCA is the time started from a rising/falling edge of the signal under test and ended at the following falling/rising (following edge should not be in the same direction) edge.
5 Collect all tIPWCA.
6 Determine the worst result from the set of tIPWCA measured.

Expected/Observable Results

- The worst measured tIPWCA must be within the specification limit.

tVAC(CA)

Test Overview

The purpose of this test is to verify that the time of the command/address signal above $V_{IH(AC)}$ and below $V_{IL(AC)}$ must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- DDR3, DDR3L and LPDDR3

Signals of Interest

- Command/Address Signal or Control Signal

Signals required to perform the test on the oscilloscope

- Command/Address Signal or Control Signal

Test References

- *See Figure 110 to 112 in Section 13 of the DDR3 SDRAM Specification in the JEDEC Standard JESD79-3F, July 2012.*

Measurement Algorithm

1. Precondition the oscilloscope.
2. Trigger on either the rising or falling edge of the command/address/control signal under test.
3. Find all crossings on the rising/falling edge of the signal under test that crosses $V_{IL(AC)}$.
4. Find all crossings on the rising/falling edge of the signal under test that crosses $V_{IH(AC)}$.
5. tVAC(CA) is the time starting from a rising $V_{IH(AC)}$ cross point and ending at the following falling $V_{IH(AC)}$ cross point.
6. tVAC(CA) is the time starting from a falling $V_{IL(AC)}$ cross point and ending at the following rising $V_{IL(AC)}$ cross point.
7. Collect all tVAC(CA).
8. Determine the worst result from the set of tVAC(,CA) measured.
9. Report the value of the worst tVAC(CA). No compliance limit checking is performed for this test. You need to check the test status (pass/fail) manually based on worst tVAC(CA) and slew rate reported.

Expected/Observable Results

- The worst measured tVAC(CA) value must be within the specification limit.

Eye-Diagram Tests

User Defined Real-Time Eye Diagram Test For Command Address

Test Overview

The purpose of this test is to automate all the required setup procedures required in order to generate an eye diagram for the Command Address signal.

The additional feature of having a mask test is allow users to perform evaluations and debugging on the eye diagram created.

Mode Supported

- DDR3, DDR3L and LPDDR3

Signal cycle of interest

- WRITE

Require Read/Write separation

- No

Signal(s) of Interest

- Command Address Signal (Supported by Clock Signal)

Required Signals that are needed to perform this test on oscilloscope

- Command Address Signal
- Clock Signal

Test References

- There is no available test specification on eye testing in JEDEC specifications. Mask testing is definable by the customers for their evaluation tests usage.

Measurement Algorithm

1 Acquire the Clock and CommandAddress signal.
2 Load acquired CommandAddress signal into WMemory4. Then use Function4 as “Magnify/Duplicate” of Loaded Waveform Memory.
3 Load Clock signal into WMemory1. Then use Function1 as “Magnify/Duplicate” of Loaded Waveform Memory.
4 Setup Clock Recovery settings on SDA.
:Explicit clock, Source = Clock, Rise/Fall Edge
5 Setup measurement threshold values for the Function4(CommandAddress) and the Function1(Clock).
6 Setup fix time scale and time position values for Function4(CommandAddress) and Function1(Clock).
7 Turn ON Color Grade Display option.
8 Identify the X1 value for re-adjustment of selected test mask.
9 Setup Mask Test settings. (Load default Test Mask on screen)
10 Turn ON Real Time Eye on SDA.
11 Start mask test until eye diagram folded.
12 Return total failed UnitInterval as a test result.

Expected/Observable Results

- Generation of an eye diagram for the Command Address signal and loading of a default test mask pattern.
- The test will show a fail status if the total failed UnitInterval is greater than 0.

14 Chip Select Tests Group

This section provides the Methods of Implementation (MOIs) for Chip Select tests for Chip Select Signals using a Keysight Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

NOTE Both XYZ# and $\overline{XYZ}$ refer to complement. Thus, CK# is the same as $\overline{CK}$.

Probing for Chip Select Tests

When performing the Chip Select tests for Chip Select Signals, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Chip Select tests may look similar to the following diagram. Refer to the Connection tab in the DDR3 Electrical Performance Compliance application for the exact number of probe connections.

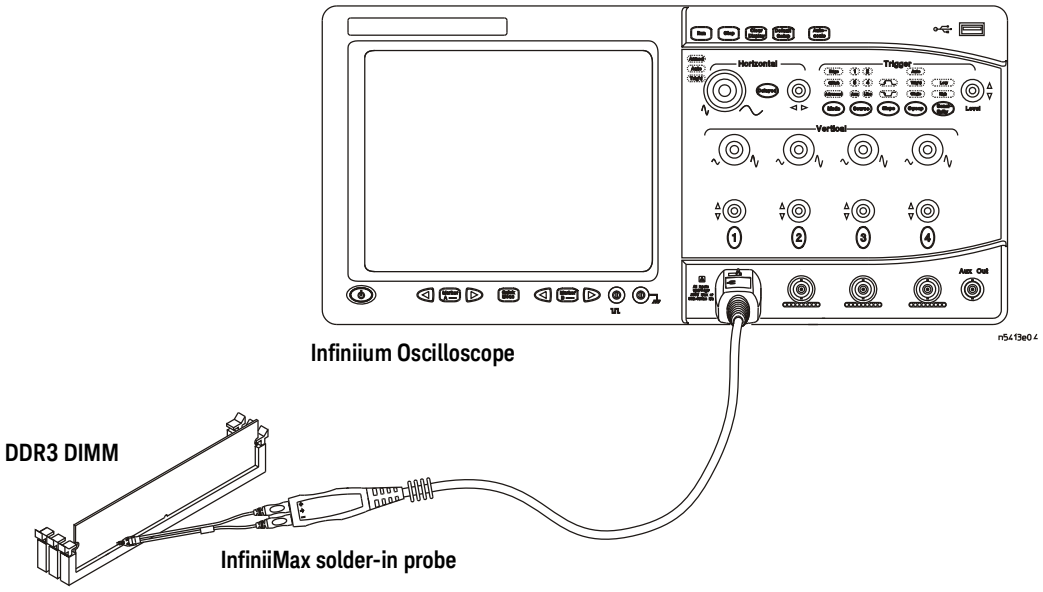

Figure 75 Probing for Chip Select tests

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 75 are just examples).

For more information on the probe amplifiers and differential probe heads, refer to the respective user guide for Probes.

Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the **Set Up** tab.

6 Select the **Test Mode**, **SDRAM Type, Speed Grade**, and **AC Levels** options.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

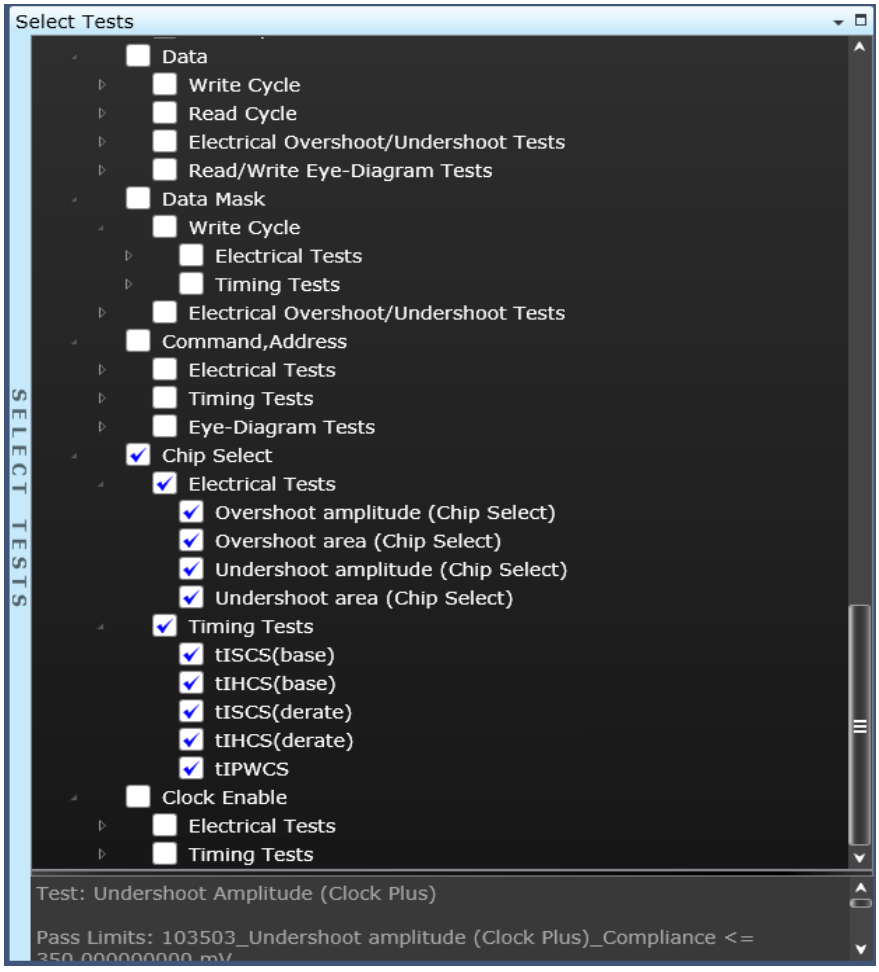

Figure 76 Selecting Chip Select Tests

Electrical Test

Overshoot Amplitude/Area (Chip Select Tests)

Test Overview

The Overshoot test can be divided into two sub-tests: Overshoot amplitude and Overshoot area.

The purpose of this test is to verify that the overshoot value of the test signal found from all regions of the acquired waveform is lower than or equal to the conformance limit of the maximum peak amplitude allowed for overshoot as specified in the JEDEC specification.

When there is an overshoot, the area is calculated based on the overshoot width and overshoot amplitude. The Overshoot area should be lower than or equal to the conformance limit of the maximum overshoot area allowed as specified in the JEDEC specification.

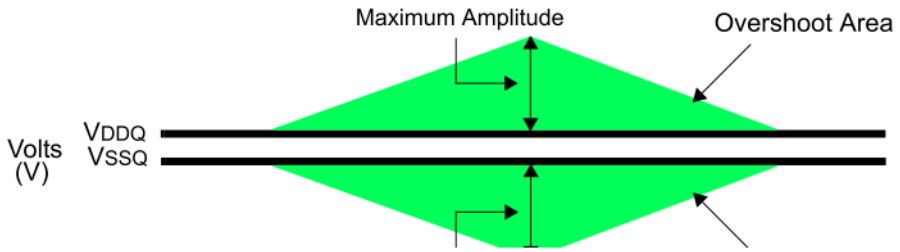

Figure 77 Clock Overshoot

Modes Supported

- LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Chip Select Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 274 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for overshoot area	Max	0.35		V
Maximum area above V_{DD}	Max	0.12	0.10	V/ns

Test References

- See *Figure 126 and Table 49 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Set the number of sampling points to 2M samples.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Obtain the overshoot region. Overshoot region starts at the rising VDD (or VDDCA) crossing and ends at the falling VDD (or VDDCA) crossing.

4 Within Overshoot region #1, perform the following steps:

i Evaluate Overshoot Amplitude by performing the following steps:
a. Use TMAX and VMAX to get time stamp of maximum voltage on overshoot region of the acquired waveform.
b. Calculate: Overshoot Amplitude = VMAX – VDD (or VDDCA).

ii Evaluate Area below VDD (or VDDCA) = (Overshoot Region End – Overshoot Region Start) * VDD (or VDDCA).

iii Evaluate Total Area above 0 volt by using Trapezoidal Method Area Calculation as shown in following figure:

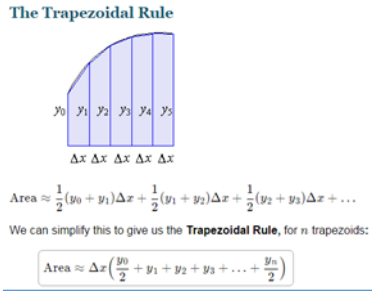

Figure 78 Trapezoidal Rule

iv Calculate Area above VDD (or VDDCA) = Total area above 0 volt - area below VDD (or VDDCA).

v Store Calculated result below for later worst case finding process;

- Overshoot Amplitude
- Area above VDD (or VDDCA)

5 Repeat the previous step for the rest Overshoot Region found in acquired waveform.

6 Find the worst result below from stored result. Compare test result to the compliance test limit.

- Overshoot Amplitude
- Area above VDD (or VDDCA)

Expected/Observable Results

- The measured maximum overshoot amplitude for the test signal must be less than or equal to the maximum overshoot value.
- The calculated overshoot area value must be less than or equal to the maximum overshoot area allowed.

Undershoot Amplitude/Area Chip Select Tests

Test Overview

The Undershoot Test can be divided into two sub-tests: Undershoot amplitude and Undershoot area.

The purpose of this test is to verify that the undershoot value of the test signal found from all regions of the acquired waveform is less than or equal to the conformance limit of the maximum peak amplitude allowed for undershoot as specified in the *JEDEC specification*.

When there is an undershoot, the area is calculated based on the undershoot width. The Undershoot area should be less than or equal to the conformance limit of the maximum undershoot area allowed as specified in the *JEDEC specification*.

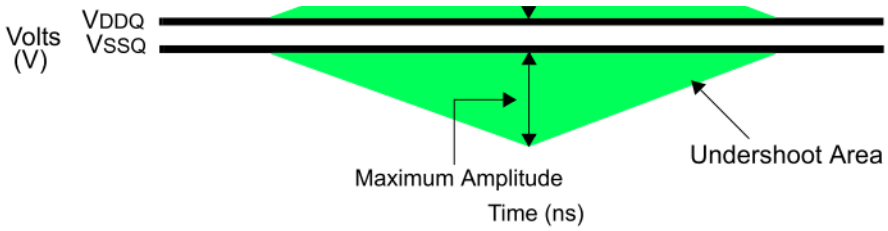

Figure 79 Clock Undershoot

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Read or Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Chip Select Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 275 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for undershoot area	Max	0.35		V
Maximum area below V_{SS}	Max	0.12	0.10	V/ns

Test References

- See *Figure 126 and Table 49 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Set the number of sampling points to 2M samples.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Obtain the undershoot region. Undershoot Region starts at falling 0 volt crossing and end at rising 0 volt crossing.

4 Within Undershoot region #1, perform the following steps:

   i Evaluate Undershoot Amplitude by performing the following steps:
   a. Use TMIN and VMIN to get time stamp of maximum voltage on undershoot region of the acquired waveform.
   b. Calculate: Undershoot Amplitude = 0- VMIN

   ii Evaluate total area below 0 volt by using Trapezoidal Method Area Calculation (refer to Figure 78)

   iii Store Calculated result below for later worst case finding process:

   - Undershoot Amplitude
   - Total area below 0 volt

5 Repeat the previous step for the rest Undershoot Region found in acquired waveform.

6 Find the worst result below from stored result. Compare test result to the compliance test limit.

   - Undershoot Amplitude
   - Total area below 0 volt

Expected/Observable Results

- The measured minimum voltage value for the test signal must be less than or equal to the maximum undershoot value.
- The calculated undershoot area value must be less than or equal to the maximum undershoot area allowed.

Timing Test

tISCS(base)

Test Overview

The purpose of this test is to verify that the time interval from Chip Select (Chip Select rising/falling edge) setup time to the associated clock crossing edge must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Signal
- Chip Select Signal

Signals required to perform the test on the oscilloscope

- Clock Signal
- Chip Select Signal

Test Definition Notes from the Specification

Table 276 cs_n Setup and Hold Base Values

Unit	Data Rate				References
	1333	1600	1866	2133	
$t_{ISCS(base)}$	215	195	-	-	$V_{IH/L(AC)} = V_{REF(DC)}$ +/-150 mV
$t_{ISCS(base)}$	-	-	162.5	13.75	$V_{IH/L(AC)} = V_{REF(DC)}$ +/-135 mV

Test References

- See *Figure 5, 77,78,79 & 80 and Table 66 in Section 11 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3B, August 2013*.

Measurement Algorithm

1 Pre-condition the scope.
2 Triggered on either rising or falling edge of the Chip Select signal.
3 Find all the crossings on rising edge of the signal under test that cross VIH(AC).
4 Find all the crossings on falling edge of the signal under test that cross VIL(AC).
5 For all the crossings found, locate the nearest Clock crossings that cross 0 V.
6 Take the time difference of the signal under test's crossings to the corresponding clock crossing as tISCS.
7 Collect all the measured tISCS.
8 Report the worst tISCS measured as test result.
9 Compare the test result to the compliance test limit

Expected/Observable Results

- The measured time interval between Chip Select setup time to respective clock crossing point must be within the specification limit.

tIHCS(base)

Test Overview

The purpose of this test is to verify that the time interval from Chip Select (Chip Select rising/falling edge) hold time to the associated clock crossing edge must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Chip Select Signal
- Clock Signal

Signals required to perform the test on the oscilloscope

- Chip Select Signal
- Clock Signal

Test Definition Notes from the Specification

Table 277 cs_n Setup and Hold Base Values

Unit	Data Rate				References
	1333	1600	1866	2133	
$t_{IHCS(base)}$	240	220	180	155	$V_{IH/L(DC)} = V_{REF(DC)}$ +/-100 mV

Test References

- See *Figure 5, 77, 78, 79 & 80 and Table 66 in Section 11of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3B, August 2013.*

Measurement Algorithm

1 Pre-condition the scope.
2 Triggered on either rising or falling edge of the Chip Select signal.
3 Find all the crossings on rising edge of the signal under test that cross VIL(DC).
4 Find all crossings on falling edge of the signal under test that cross VIH(DC).
5 For all the crossings found, locate the nearest Clock crossings that cross 0 V.
6 Take the time difference of the signal under test's crossings to the corresponding clock crossing as tIHCS.
7 Collect all the measured tIHCS.
8 Report the worst tIHCS measured as test result.
9 Compare the test result to the compliance test limit.

Expected/Observable Results

- The measured time interval between Chip Select hold time to respective clock crossing point must be within the specification limit.

tISCS(derate)

Test Overview

The purpose of this test is to verify that the time interval from Chip Select (Chip Select rising/falling edge) setup time to the associated clock crossing edge must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Signal
- Chip Select Signal

Signals required to perform the test on the oscilloscope

- Clock Signal
- Chip Select Signal

Test Definition Notes from the Specification

Table 278 cs_n Setup and Hold Base Values

Unit	Data Rate				References
	1333	1600	1866	2133	
$t_{ISCS(base)}$	215	195	-	-	$V_{IH/L(AC)} = V_{REF(DC)}$ +/-150 mV
$t_{ISCS(base)}$	-	-	162.5	13.75	$V_{IH/L(AC)} = V_{REF(DC)}$ +/-135 mV

Table 279 Derating Values LPDDR3 tIS/tIH - AC/DC based AC 150

ΔtDS, ΔtDH derating in [ps] AC/DC based
AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV
DC 100 Threshold -> VIH(DC) = VREF(DC) + 100 mV, VIL(DC) = VREF(DC) - 100 mV

		DQS_t, DQS_c Differential Slew Rate											
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS-n Slew Rate V/ns	4.0	38	25	38	25	38	25	38	25	38	25	-	-
	3.0	25	17	25	17	25	17	25	17	25	17	38	29
	2.0	-	-	-	-	0	0	0	0	0	0	13	13
	1.5	-	-	-	-	-	-	-25	-17	-25	-17	-12	-4

NOTE 1. Empty cell contents are defined as not supported.

Table 280 Derating Values LPDDR3 tDS/DH - AC/DC based AC 135

ΔtDS, ΔtDH derating in [ps] AC/DC based
AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV
DC 100 Threshold -> VIH(DC) = VREF(DC) + 100 mV, VIL(DC) = VREF(DC) - 100 mV

		DQS_t, DQS_c Differential Slew Rate											
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS-n Slew Rate V/ns	4.0	34	25	34	25	34	25	34	25	34	25	-	-
	3.0	-	-	23	17	23	17	23	17	23	17	34	29
	2.0	-	-	-	-	0	0	0	0	0	0	11	13
	1.5	-	-	-	-	-	-	-25	-17	-25	-17	-12	-4

NOTE 1. Empty cell contents are defined as not supported.

Test References

- See *Figure 5, 77,78,79 & 80 and Table 66, 67 & 68 in Section 11 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3B, August 2013*.

Measurement Algorithm

1 Pre-condition the scope.
2 Triggered on either rising or falling edge of the Chip Select signal.
3 Find all the crossings on rising edge of the signal under test that cross VIH(AC).
4 Find all the crossings on falling edge of the signal under test that cross VIL(AC).
5 For all the crossings found, locate the nearest Clock crossings that cross 0 V.
6 Take the time difference of the signal under test's crossings to the corresponding clock crossing as tISCS.
7 Collect all the measured tISCS.
8 Report the worst tISCS measured as test result.
9 Measure the mean slew rate for all the Chip Select and CK edges.
10 Use the mean slew rate for Chip Select and CK to determine the ΔtIS derating value based on the derating tables.
11 The test limit for tISCS test = tISCS (base) + ΔtIS.

Expected/Observable Results

- The measured time interval between Chip Select setup time to respective clock crossing point must be within the specification limit.

tIHCS(derate)

Test Overview

The purpose of this test is to verify that the time interval from Chip Select (Chip Select rising/falling edge) hold time to the associated clock crossing edge must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Chip Select Signal
- Clock Signal

Signals required to perform the test on the oscilloscope

- Chip Select Signal
- Clock Signal

Test Definition Notes from the Specification

Table 281 cs_n Setup and Hold Base Values

Unit	Data Rate				References
	1333	1600	1866	2133	
$t_{IHCS(base)}$	240	220	180	155	$V_{IH/L(DC)} = V_{REF(DC)}$ +/-100 mV

Table 282 Derating Values LPDDR3 tIS/tIH - AC/DC based AC 150

ΔtDS, ΔtDH derating in [ps] AC/DC based
AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV
DC 100 Threshold -> VIH(DC) = VREF(DC) + 100 mV, VIL(DC) = VREF(DC) - 100 mV

		DQS_t, DQS_c Differential Slew Rate											
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS-n Slew Rate V/ns	4.0	38	25	38	25	38	25	38	25	38	25	-	-
	3.0	25	17	25	17	25	17	25	17	25	17	38	29
	2.0	-	-	-	-	0	0	0	0	0	0	13	13
	1.5	-	-	-	-	-	-	-25	-17	-25	-17	-12	-4

NOTE 1. Empty cell contents are defined as not supported.

Table 283 Derating Values LPDDR3 tDS/DH - AC/DC based AC 135

ΔtDS, ΔtDH derating in [ps] AC/DC based
AC 150 Threshold -> VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV
DC 100 Threshold -> VIH(DC) = VREF(DC) + 100 mV, VIL(DC) = VREF(DC) - 100 mV

		DQS_t, DQS_c Differential Slew Rate											
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS-n Slew Rate V/ns	4.0	34	25	34	25	34	25	34	25	34	25	-	-
	3.0	-	-	23	17	23	17	23	17	23	17	34	29
	2.0	-	-	-	-	0	0	0	0	0	0	11	13
	1.5	-	-	-	-	-	-	-25	-17	-25	-17	-12	-4

NOTE 1. Empty cell contents are defined as not supported.

Test References

- See *Figure 5, 77, 78, 79 & 80 and Table 66, 67 & 68 in Section 11of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3B, August 2013.*

Measurement Algorithm

1 Pre-condition the scope.
2 Triggered on either rising or falling edge of the Chip Select signal.
3 Find all the crossings on rising edge of the signal under test that cross VIL(DC).
4 Find all crossings on falling edge of the signal under test that cross VIH(DC).
5 For all the crossings found, locate the nearest Clock crossings that cross 0 V.
6 Take the time difference of the signal under test's crossings to the corresponding clock crossing as tIHCS.
7 Collect all the measured tIHCS.
8 Report the worst tIHCS measured as test result.
9 Measure the mean slew rate for all the Chip Select and CK edges.
10 Use the mean slew rate for Chip Select and CK to determine the ΔtIH derating value based on the derating tables.
11 The test limit for tIHCS test = tIHCS (base) + ΔtIH

Expected/Observable Results

- The measured time interval between Chip Select hold time to respective clock crossing point must be within the specification limit.

tIPWCS

Test Overview

The purpose of this test is to verify that the width of the high or low level of Chip Select signal must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Chip Select Signals

Signals required to perform the test on the oscilloscope

- Chip Select Signals

Test Definition Notes from the Specification

Table 284 cs_n Setup and Hold Base Values

Parameter	Symbol	MIN/MAX	Data Rate				Unit
			1333	1600	1866	2133	
Command Address Input Parameter							
CS_n input pulse width	t_{IPWCS}	MIN		0.7			$t_{CK(avg)}$

Test References

- See *Table 64 in Section 11 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3B, August 2013*.

Measurement Algorithm

1 Pre-condition the scope.
2 Triggered on either rising or falling edge of the Chip Select signal.
3 Find all crossings on rising/falling edge of the Chip Select signal that cross Vref.
4 tIPWCS is time started from a rising/falling edge of the Chip Select signal and ended at the following falling/rising (following edge should not same direction) edge.
5 Collect all tIPWCS.
6 Determine the worst result from the set of tIPWCS measured

Expected/Observable Results

- The worst measured tIPWCS must be within the specification limit.

15 Clock Enable Tests Group

This section provides the Methods of Implementation (MOIs) for Clock Enable tests for Clock Enable Signals using a Keysight Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

NOTE Both XYZ# and $\overline{XYZ}$ refer to complement. Thus, CK# is the same as $\overline{CK}$.

Probing for Clock Enable Tests

When performing the Clock Enable tests for Clock Enable Signals, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Clock Enable tests for clocks may look similar to the following diagram. Refer to the Connection tab in the DDR3 Electrical Performance Compliance application for the exact number of probe connections.

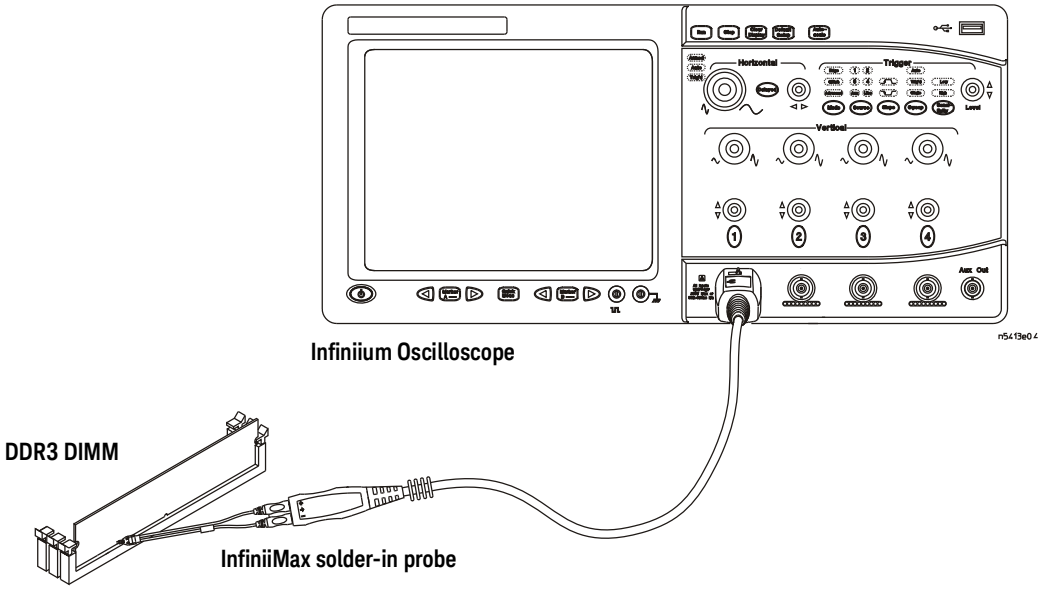

Figure 80 Probing for strobe plus tests

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 80 are just examples).

For more information on the probe amplifiers and differential probe heads, refer to the respective user guide for Probes.

Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the **Set Up** tab.

6 Select the **Test Mode**, **SDRAM Type, Speed Grade**, and **AC Levels** options.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

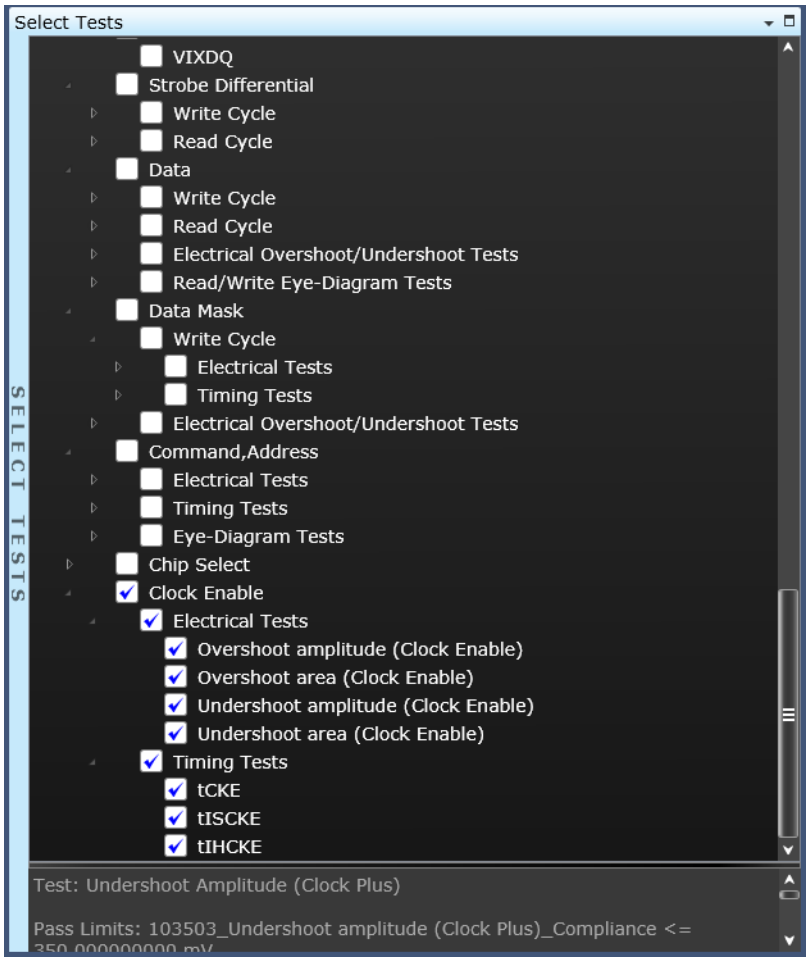

Figure 81 Selecting Clock Enable Select Tests

Electrical Test

Overshoot Amplitude / Area) (Clock Enable)

Test Overview

The Overshoot test can be divided into two sub-tests: Overshoot amplitude and Overshoot area.

The purpose of this test is to verify that the overshoot value of the test signal found from all regions of the acquired waveform is lower than or equal to the conformance limit of the maximum peak amplitude allowed for overshoot as specified in the JEDEC specification.

When there is an overshoot, the area is calculated based on the overshoot width and overshoot amplitude. The Overshoot area should be lower than or equal to the conformance limit of the maximum overshoot area allowed as specified in the JEDEC specification.

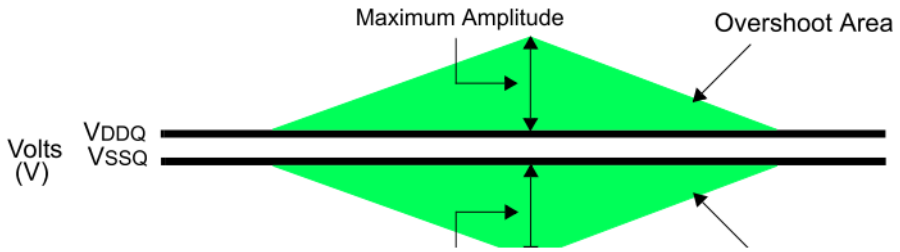

Figure 82 Clock Overshoot

Modes Supported

- LPDDR3

Signal cycle of Interest

- Read or Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Enable Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 285 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for overshoot area	Max	0.35		V
Maximum area above V_{DD}	Max	0.12	0.10	V-ns

Test References

- See *Figure 126 and Table 49 Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Set the number of sampling points to 2M samples.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Obtain the overshoot region. Overshoot region starts at the rising VDD (or VDDCA) crossing and ends at the falling VDD (or VDDCA) crossing.

4 Within Overshoot region #1, perform the following steps:

i Evaluate Overshoot Amplitude by performing the following steps:
a. Use TMAX and VMAX to get time stamp of maximum voltage on overshoot region of the acquired waveform.
b. Calculate: Overshoot Amplitude = VMAX – VDD (or VDDCA).

ii Evaluate Area below VDD (or VDDCA) = (Overshoot Region End – Overshoot Region Start) * VDD (or VDDCA).

iii Evaluate Total Area above 0 volt by using Trapezoidal Method Area Calculation as shown in following figure:

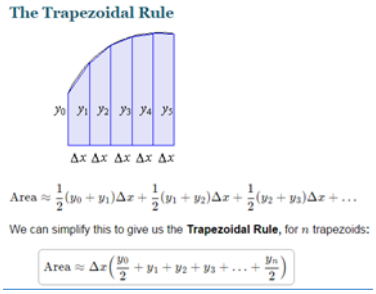

Figure 83 Trapezoidal Rule

iv Calculate area above VDD (or VDDCA) = Total area above 0 volt - area below VDD (or VDDCA).

v Store calculated result below for later worst case finding process;

- Overshoot Amplitude
- Area above VDD (or VDDCA)

5 Repeat the previous step for the rest Overshoot Region found in acquired waveform.

6 Find the worst result below from stored result. Compare test result to the compliance test limit.

- Overshoot Amplitude
- Area above VDD (or VDDCA)

Expected/Observable Results

- The measured maximum overshoot amplitude for the test signal must be less than or equal to the maximum overshoot value.
- The calculated overshoot area value must be less than or equal to the maximum overshoot area allowed.

Undershoot Amplitude / Area (Clock Enable)

Test Overview

The Undershoot Test can be divided into two sub-tests: Undershoot amplitude and Undershoot area.

The purpose of this test is to verify that the undershoot value of the test signal found from all regions of the acquired waveform is less than or equal to the conformance limit of the maximum peak amplitude allowed for undershoot as specified in the *JEDEC specification*.

When there is an undershoot, the area is calculated based on the undershoot width. The Undershoot area should be less than or equal to the conformance limit of the maximum undershoot area allowed as specified in the *JEDEC specification*.

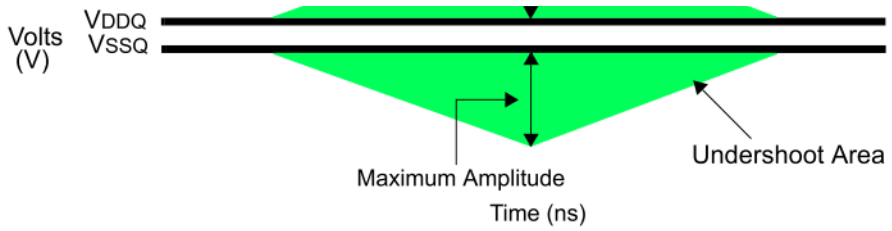

Figure 84 Clock Undershoot

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Read or Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Enable Signals

Signals required to perform the test on the oscilloscope

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 286 AC Overshoot/Undershoot Specification

Parameter	Min/Max	1333	1600	Units
Maximum peak amplitude allowed for undershoot area	Max	0.35		V
Maximum area below V_{SS}	Max	0.12	0.10	V-ns

Test References

- See *Figure 126 and Table 49 in Section 8 of the LPDDR3 SDRAM Specification in the JEDEC Standard JESD209-3E, December 2011.*

Measurement Algorithm

1 Set the number of sampling points to 2M samples.

2 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Obtain the undershoot region. Undershoot Region starts at falling 0 volt crossing and end at rising 0 volt crossing.

4 Within Undershoot region #1, perform the following steps:

   i Evaluate Undershoot Amplitude by performing the following steps:
   a. Use TMIN and VMIN to get time stamp of maximum voltage on undershoot region of the acquired waveform.
   b. Calculate: Undershoot Amplitude = 0- VMIN

   ii Evaluate total area below 0 volt by using Trapezoidal Method Area Calculation (refer to Figure 83)

   iii Store Calculated result below for later worst case finding process;

   - Undershoot Amplitude
   - Total area below 0 volt

5 Repeat the previous step for the rest Undershoot Region found in acquired waveform.

6 Find the worst result below from stored result. Compare test result to the compliance test limit.

   - Undershoot Amplitude
   - Total area below 0 volt

Expected/Observable Results

- The measured minimum voltage value for the test signal must be less than or equal to the maximum undershoot value.
- The calculated undershoot area value must be less than or equal to the maximum undershoot area allowed.

Timing Tests

tCKE

Test Overview

The purpose of this test is to verify that the pulse width of CKE signal must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Write

Require Read/Write Separation

- No

Signal(s) of Interest

- CKE Signal

Signals required to perform the test on the oscilloscope

- CKE Signal
- Clock Signal

Test Definition Notes from the Specification

Table 287 AC Timing

Parameter	Symbol	MIN/MAX	Data Rate		Unit
			1333	1600	
CKE minimum pulse width (HIGH and LOW pulse Width)	t_{CKE}	MIN	max (7.5 ns, 3nCK)		ns

Test References

- See *Figure 137 and Table 64 in Section 11 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3, December 2011*.

Measurement Algorithm

1 Pre-condition the scope.
2 Triggered on either rising or falling edge of the command/address/control signal under test.
3 Find all the crossings on rising/falling edge of the CKE signal that cross Vref.
4 Find all the crossings on rising edge of the Clock signal that cross Vref.
5 If CKE crossing count is more than one then perform this action
   i Find rising edge of Clock(ClkEdge1) which is nearest on the right side of first rising/falling edge of the CKE signal. Then, find rising edge of Clock (ClkEdge2) which is nearest on the right side of second rising/falling edge of the CKE signal. Calculate tCKE= ClkEdge2- ClkEdge1.
   ii Repeat previous step for all found CKE crossing.
6 If CKE crossing count is equal to one then perform this action
   i Find rising edge of Clock(ClkEdge1) which is nearest on the right side of first rising/falling edge of the CKE signal. Then, find rising edge of Clock (ClkEdge2) which is the last rising edge of clock signal. Calculate tCKE= ClkEdge2- ClkEdge1.
7 Determine the worst result from the set of tCKE measured.
8 Report the value of worst tCKE

Expected/Observable Results

- The worst measured tCKE must be within the specification limit.

tISCKE

Test Overview

The purpose of this test is to verify that the time interval from Clock Enable (Clock Enable rising/falling edge) setup time to the associated clock crossing edge must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Enable Signals
- Clock Signals

Signals required to perform the test on the oscilloscope

- Clock Enable Signals
- Clock Signals

Test Definition Notes from the Specification

Table 288 AC Timing (con'd)

Parameter	Symbol	MIN/MAX	Data Rate				Unit
			1333	1600	1866	2133	
CKE Input Parameter							
CKE input setup time	t_{ISCKE}	MIN		0.25			$t_{CK(avg)}$

Test References

- See *Figure 6 and Table 64 in Section 11 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3B, August 2013.*

Measurement Algorithm

1 Pre-condition the scope.
2 Triggered on either rising or falling edge of the Clock Enable signal.
3 Find all the crossings on rising edge of the signal under test that cross VIH(AC).
4 Find all crossings on falling edge of the signal under test that cross VIL(AC).
5 For all the crossings found, locate the nearest Clock crossings that cross 0 V.
6 Take the time difference of the signal under test's crossings to the corresponding clock crossing as tISCKE.
7 Collect all the measured tISCKE.
8 Report the worst tISCKE measured as test result.
9 Compare the test result to the compliance test limit.

Expected/Observable Results

- The measured time interval between Clock Enable setup time to respective clock crossing point must be within the specification limit.

tIHCKE

Test Overview

The purpose of this test is to verify that the time interval from Clock Enable (Clock Enable rising/falling edge) hold time to the associated clock crossing edge must be within the conformance limit as specified in the JEDEC specification.

Modes Supported

- LPDDR3 only

Signal cycle of Interest

- Write

Require Read/Write Separation

- No

Signal(s) of Interest

- Clock Enable Signals
- Clock Signals

Signals required to perform the test on the oscilloscope

- Clock Enable Signals
- Clock Signals

Test Definition Notes from the Specification

Table 289 cs_n Setup and Hold Base Values

Parameter	Symbol	MIN/MAX	Data Rate				Unit
			1333	1600	1866	2133	
CKE Input Parameter							
CKE input hold time	t_{ISCKE}	MIN		0.25			$t_{CK(avg)}$

Test References

- See *Figure 6 and Table 64 in Section 11 of the LPDDR3 SDRAM Specification, JEDEC Standard JESD209-3B, August 2013*.

Measurement Algorithm

1 Pre-condition the scope.
2 Triggered on either rising or falling edge of the Clock Enable signal.
3 Find all crossings on rising edge of the signal under test that cross VIL(DC).
4 Find all crossings on falling edge of the signal under test that cross VIH(DC).
5 For all the crossings found, locate the nearest Clock crossings that cross 0V.
6 Take the time different of the signal under test's crossings to the corresponding clock crossing as tIHCKE.
7 Collect all measured tIHCKE.
8 Report the worst tIHCKE measured as test result.
9 Compare the test result to the compliance test limit.

Expected/Observable Results

- The measured time interval between Clock Enable hold time to respective clock crossing point must be within the specification limit.