

Method of Implementation (MOI) for USB4 Transmitter & Receiver Return Loss

USB4 and USB4 Version 2.0 TX / RX Return Loss using
Keysight Vector Network Analyzer with Enhanced TDR app



Table of Contents

Table of Contents 2

Revision History 3

Configuration Requirements 4

Test Procedure..... 5

Measurement Setups 9

Measurement and Data Analysis 18

Manual Setup 23

Web Resources..... 29

Revision History

Revision	Comments	Date
1.0	First draft for E5080B series	30-July-2020
1.1	Updated USB4 ETT tool and test controller information	14-Mar-2022
1.2	Updated new USB4v1 test method using SigTest tool.	25-Aug-2022
1.3	- Added new USB4v2 test method using SigTest tool rev0.75 onwards. - Added new USB4v1 SMA and SMP test fixtures setup.	18-Feb-2023
1.4	Added new USB4v1 SMA test fixtures setup diagram.	30-Nov-2023
1.5	Added new procedure to enable SNP with gating in VNA.	07-Feb-2024

Reference documents

1. Universal Serial Bus 4 (USB4) USB4 Router Assembly Electrical Compliance Test Specification. Revision 1.04 – Sep 2023.
2. Universal Serial Bus 4 (USB4™) Specification; Version 1.0 (Oct 2022)
3. Universal Serial Bus 4 (USB4™) Specification; Version 2.0 (Aug 2023)
4. USB4 SIGTEST User Manual Revision 0.87 (Oct 2023).

Configuration Requirements

Description	Test equipment	Qty
Network analyzer	Keysight Vector Network Analyzer: (20 GHz is recommended for USB4/Type-C cable/connector; 26.5 GHz is recommended for USB4 Version 2.0.) 4-Ports (Min requirement to run SigTest tool): • E5080B: 4-port test set, 9 kHz to 20 GHz or higher, • E5081A: 4-port test set, 10 MHz to 20 GHz or higher, • P502xA/B-400 Streamline USB Series VNA or • M980xA-400 PXI Multiport VNA or • N522xB PNA Note 1: Ensure that VNA firmware revision is at least version A.17.25.05 or above (Windows 10) for SNP with gating. Note 2: Refer to the Appendix for manual setup if you are using a 2-Port VNA or the legacy E5071C for this testing.	1 ea.
Software (Recommended for gating setup when using legacy SMP test fixture)	S9x011A/B Enhanced time-domain analysis with TDR * Selection is based on the VNA platforms. x=6 for ENA, x=7 for Streamline USB, x=5 for PXI, x=3 for PNA family	1 ea.
USB-IF compliance tools	USB4 ETT tool (Rev 1.1.2 onwards) from USB-IF: https://www.usb.org/document-library/usb4ett	1 ea.
	USB4 SigTest tool (Rev 0.87 onwards) https://groups.usb.org/wg/usbecwg/document/folder/1139	1 ea.
Test controller	Test controller from Wilder Technologies • USB4-TPA-UC (USB4 microcontroller) • CG3-TPA-TR (Thunderbolt microcontroller) For more information about setting up the test controller and ETT tool, refer to USB4ETT tool PDF documentation or Keysight D9040USBC USB4 Compliance Test Application Online Help > Setting Up the Test Environment > SigTest Setup > USB4 ETT Tools Setup	1 ea.
Test fixture	Wilder Technologies Wilder USB4 Type-C fixture (SMA) • TF1 for Transmitter (TX); • TF2 + TF6 Low-Speed Unite for Receiver (RX). Note: The legacy 2.92mm SMP Wilder USB4/TBT3 fixture is non-compliant and only allowed for internal debug/testing. * Required for Legacy SMP fixture: Rosenberger 2.92mm pair cable and 2.92mm-SMP adapter x2	1 ea.
ECal module	Min. 2-Ports Electronic Calibration (ECal) Module EG: N7555A 2-Ports or N4433D-010/0DC 4-Ports	1 ea.
RF cable	3.5 mm or SMA cables of 4 GHz bandwidth or more * Y1740A-100 (3.5-mm m-m, 36 inch) cable is recommended for USB and PXI VNA	2 ea.
Adapter (For E5080B only)	Coaxial straight Female-SMA Female-SMA 50-Ohm adapters (Keysight 1250-1666).	4 ea.
Terminator	50-ohm terminations to terminate unused channels (EG: Keysight 909D-301)	2 ea.

Test Procedure

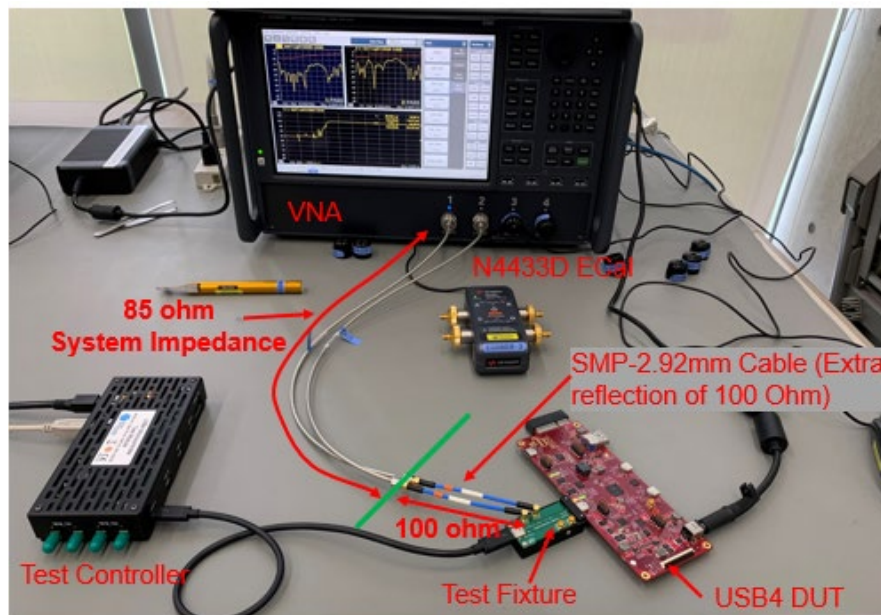
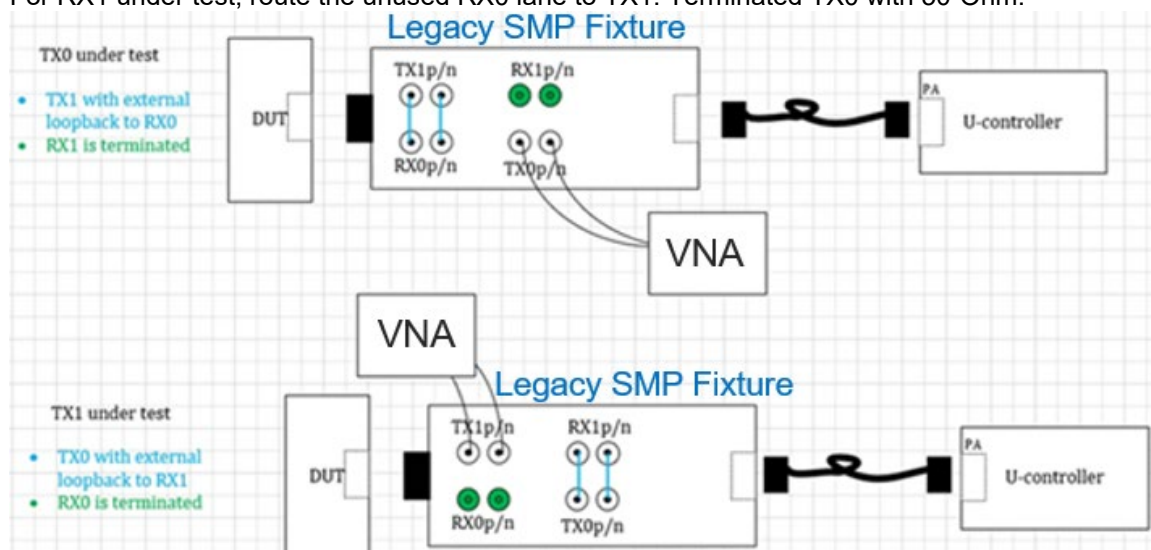
Test flow chart

Steps	Procedure
Step 1	The VNA should be powered on and allowed to warm up - the recommendation is for 24 hours prior to measurement.
Step 2	Set measurement conditions by recalling a state file or manual setup.
Step 3	Setup test equipment and test fixture connections based on test setup diagrams. • USB4 SigTest Tool • USB4 ETT tool • Wilder's microcontroller and its USB driver installation • Connect test fixture to test microcontroller, USB4 DUT and VNA port.
Step 4	Perform Electronic Calibration (ECal) for frequency-domain and time-domain For USB4v1 and USB4v2 SMA type test fixture - Perform ECal calibration for frequency-domain For legacy USB4v1 SMP type test fixture - Perform ECal calibration for both frequency-domain and time-domain. - Perform gating setup for both frequency-domain and time-domain. Note: The legacy 2.92mm SMP USB4/TBT3 fixture is non-compliant and only allowed for internal debug/testing.
Step 5	Run USB4ETT from the connected PC. • Connect the plug board to Port A of the test microcontroller for USB4 test. • In ETT GUI, select USB4 > Gen3 or Gen2 based on your cable DUT. - For USB4v2, select USB4 > Gen4 • Select and run test pattern: Transmitter Return Loss/Receiver Return Loss.
Step 6	Perform frequency-domain measurements to save the S-parameter touchstone file (S2P) for SigTest tool analysis. Please ensure that VNA firmware revision is at least version A.17.25.05 or above to enable SNP with gating function. For USB4v1 (gen2_rounded/gen2_legacy/gen3_rounded/gen3_legacy) • TX and RX differential return loss, Sdd22 (Normative) • TX and RX common-mode return loss, Scc22 (Normative) For USB4v2 (Gen4) • TX and RX differential return loss, Sdd22 (Informative) • TX Integrated return loss, IRL (Normative) • RX Integrated return loss, IRL (Informative)
Step 7	Run SigTest tool and check output result csv file for pass/fail results.

Test setup diagram

For USB4v1 RL testing using legacy 2.92mm SMP test fixture

- The legacy SMP fixture is for internal debug/testing only. For compliance certification, please use the new SMA fixtures testing a single lane at a time.
- A SMP to SMA cable/adaptor is required to connect the test fixture to VNA ports.
- Gating setup required to remove the 100-Ohm impedance from 2.92mm SMP.
- USB4 SigTest tool required topology setting to VNA Port 1-3 (BAL mode).
- For TX0 under test, route the unused TX1 lane to RX0. Terminated RX1 with 50-Ohm.
- For TX1 under test, route the unused TX0 lane to RX1. Terminated RX0 with 50-Ohm.
- For RX0 under test, route the unused RX1 lane to TX0. Terminated TX1 with 50-Ohm.
- For RX1 under test, route the unused RX0 lane to TX1. Terminated TX0 with 50-Ohm.

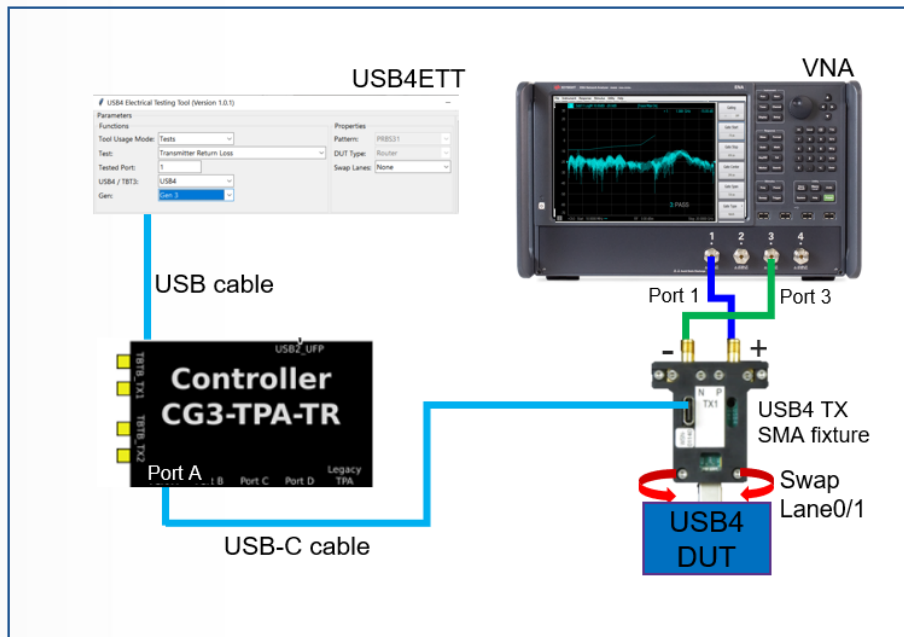


For USB4v1 RL testing using the SMA test fixture

- No gating setup or fixture de-embedding is needed. However, gating setup is allowed if required.
- USB4 SigTest tool required topology setting to VNA Port 1-3 (BAL mode).
- The RL test setup for TX and RX will be different as below.

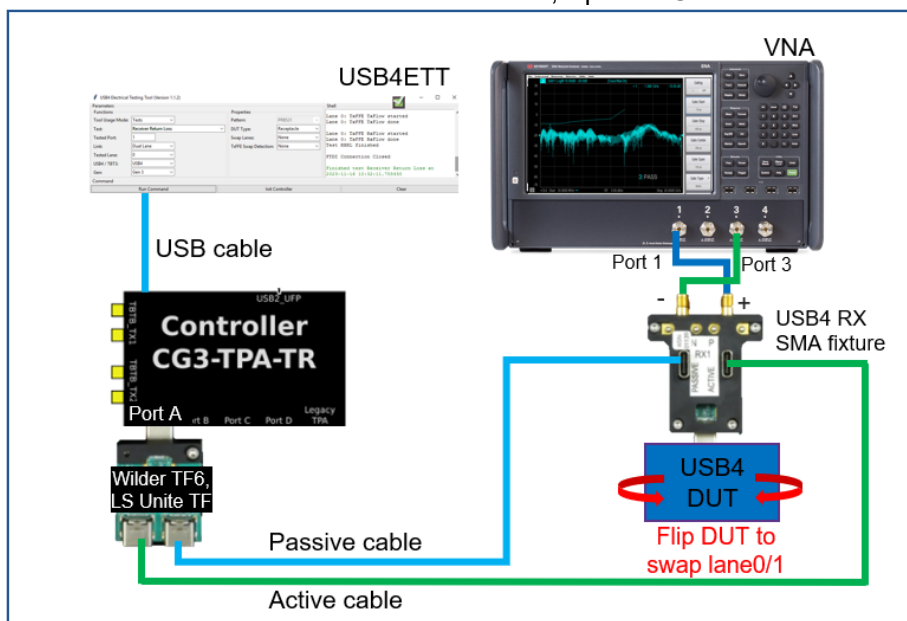
For Transmitter return loss setup using SMA test fixture

- Use Wilder USB4 Type-C TF1 for TX test fixture.
- The SMA fixture allows one lane at a time, flip the fixture's connector to test both TX0/TX1 lanes.



For Receiver return loss setup using SMA test fixture

- Use Wilder USB4 Type-C TF2 for RX TP3' + TF6 Low-speed unite test fixture.
- The SMA fixture allows one lane at a time, flip the DUT's connector to test both RX0/RX1 lanes.



- Flip the active and passive cable orientation connected to the Wilder TF6 low-speed unit fixture (to micro-controller) and verify the correct connection using the USB4ETT tool. A wrong connection will result in an error when executing the ETT tool.

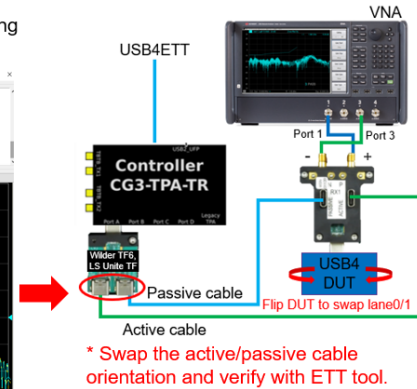
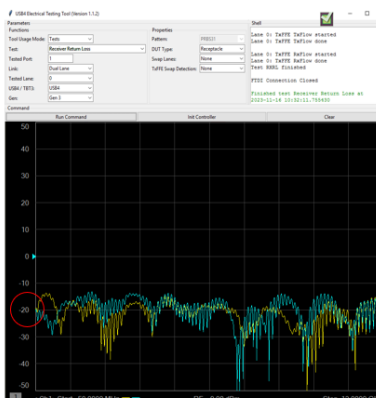
Wrong connection

- USB4ETT tool with error.
- VNA show Sdd11 return loss wave starting from 0 dB; indicating an open circuit.



Correct connection

- USB4ETT tool run without error and able to enter USB mode.
- VNA show Sdd11 return loss wave starting from 20 dB



For USB4v2 using the SMA test fixture

- No gating setup or fixture de-embedding is needed.
- USB4 SigTest tool required topology setting to VNA Port 1-3 (BAL mode).
- The actual setup diagram is still TBD.

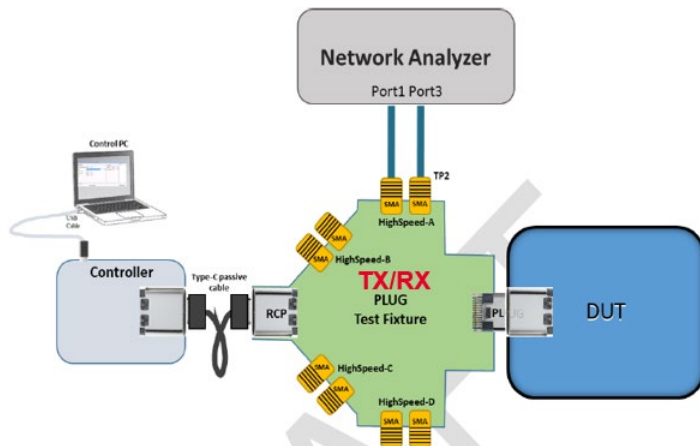
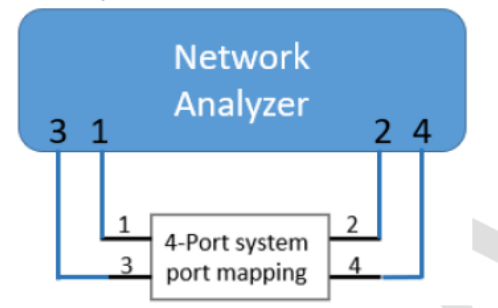


Figure 4. Transmitter Return Loss Test Setup

B.2 4-Port mapping convention

4-Port system shall be connected as shown in



Measurement Setups

Recalling a state file

This section describes how to recall a state file for Time Domain and Frequency Domain settings.

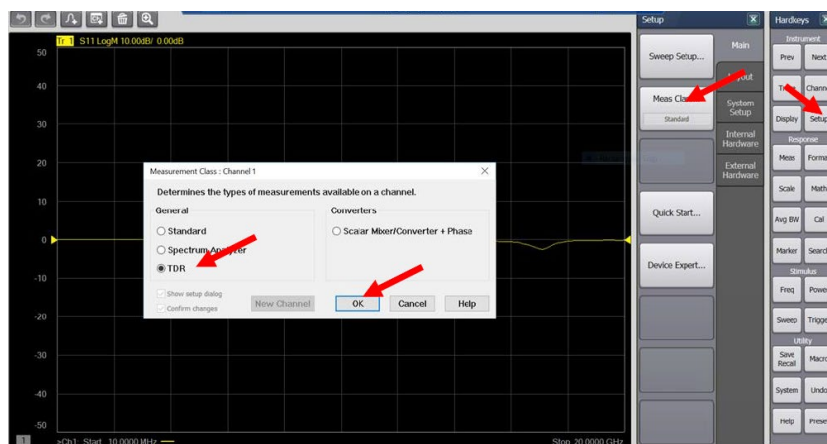
A state file can be downloaded from Keysight.com at the following URL.

www.keysight.com/find/ena-tdr_compliance

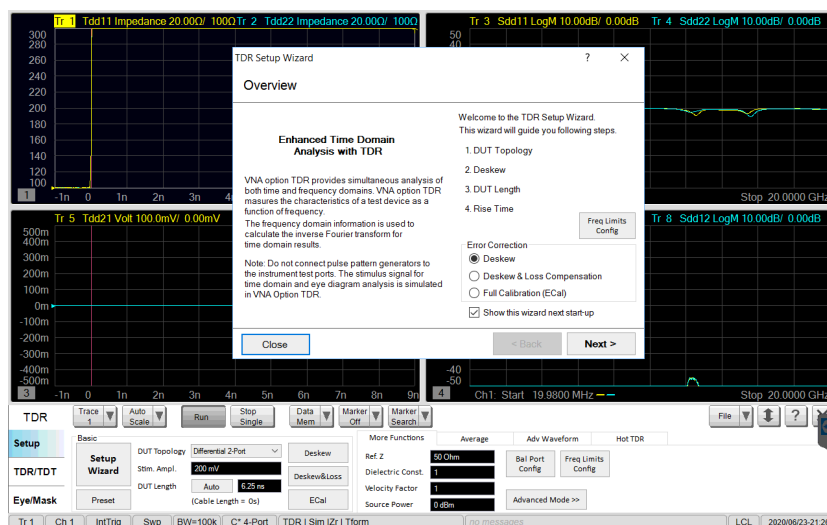
If you use your local PC to download, save the state file to a USB mass storage device in order to move it to the VNA unit. Connect the USB mass storage device to the front USB port of the VNA unit.

For manual measurement settings, refer to Appendix for manual setup procedure.

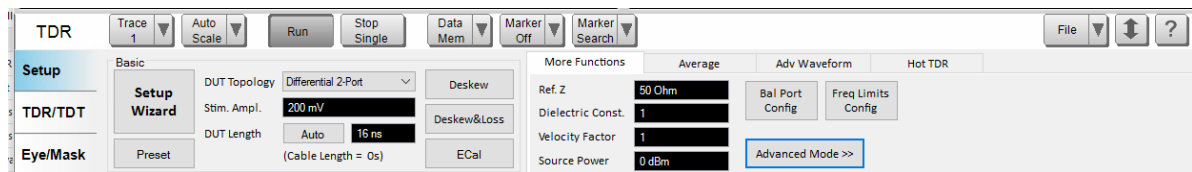
1. Click **Setup > Main > Meas Class...** to launch measurement class setup dialog box
2. Select **TDR** and click OK.



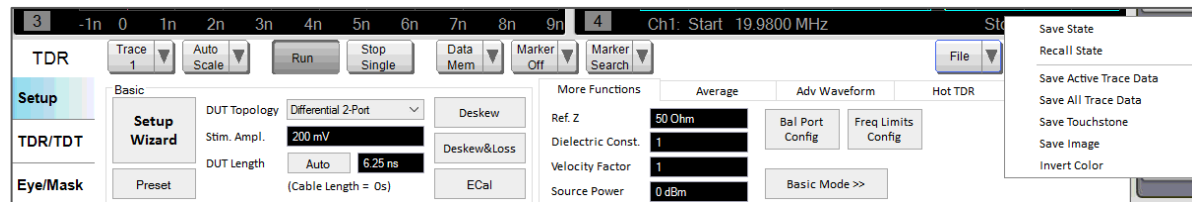
3. Select Close and confirm with Yes to close the setup wizard.



4. Select Click **Advanced Mode** of TDR software and Click Yes to enter the advanced mode.



- Click **File > Recall State**. Select the state file (*.tdr) and click Open to recall.



- The windows will launch pre-define state file configuration for Ethernet compliance testing.
- All the measurement settings including calibration information can be saved.
Select **File > Save State As... > State and Cal Set Date (*.csa)** to save the settings.

Common parameters setup for frequency domain measurements

- Press **Channel Next** to select Channel 2.
- Select **Sweep > Sweep Setup** and key-in sweep properties as below:

For USB4v1 sweep settings

- Set **Start** value to "10 MHz".
- Set **Stop** value to "12 GHz".
- Set **Power** value to "0 dBm".
- Set **Points** and set to "1600".
- Set **IF Bandwidth** to "1 kHz".

For USB4v2 sweep settings

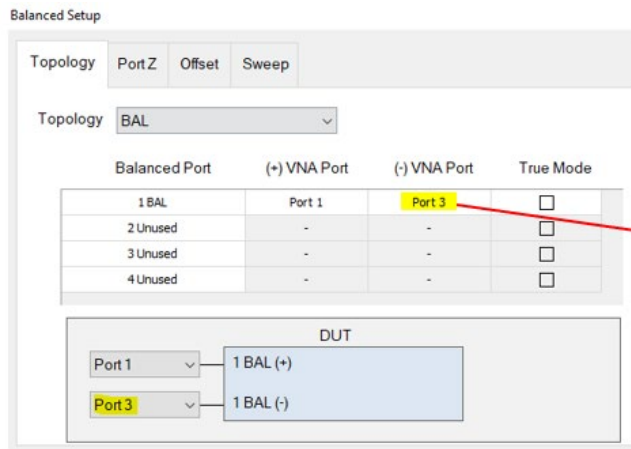
- Set **Start** value to "10 MHz".
- Set **Stop** value to "20 GHz".
- Set **Power** value to "0 dBm".
- Set **Points** and set to "1600".
- Set **IF Bandwidth** to "1 kHz".

- Select **Cal > Fixtures > Fixture Setup > Port Z...** Select and check "**Enable Port Z Conversion (all ports)**" to turn ON Port Z conversion at a converted value to 42.5 Ω .

4. Select **Meas > Balanced > Topology... > BAL**
5. Select **Balanced Port > 1 BAL > Port 1- Port 3**

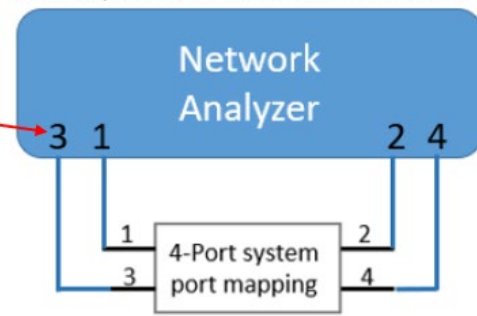
Note 1: SigTest tool only accept S2P input file from 2 Port measurement. You can set one **BAL** mode on Port 1-Port 3 for one measurement at a time. Optional to set **BAL-BAL** mode if you want to setup 2 pairs of lanes.

Note 2: If you are using a 2 Port VNA, setup the **Topology** using default **BAL** mode **Port 1-Port 2** and save the S2P S-parameter in default setting. SigTest tool v0.75 and above will be able to support S2P file with Port 1-Port 2 format as well.



B.2 4-Port mapping convention

4-Port system shall be connected as shown in



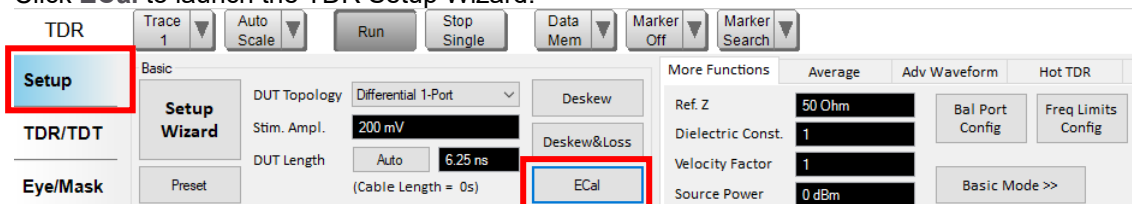
Calibration setup

The purpose of this step is to calibrate the RF effects such as delay, loss or mismatch of RF cables and test fixture traces before measurements.

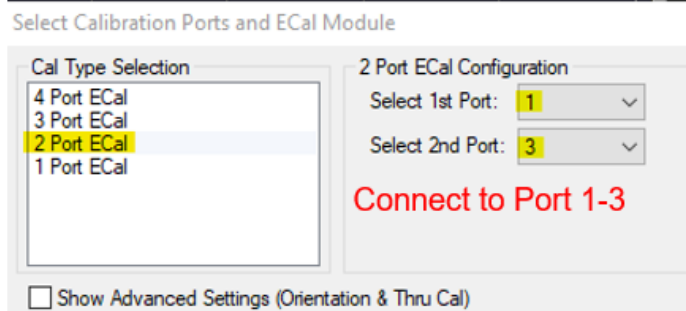
ECal calibration on time domain

ECal calibration for time-domain measurements is performed by the TDR software.

1. Press **Channel Next** to select Channel 1.
2. Click **Setup** tab.
3. Click **ECal** to launch the TDR Setup Wizard.



4. Connect the VNA ports (Port 1 and Port 3) to the ECal module with RF cables. Terminate unused ports with 50-Ohm terminators.
5. Click **Calibrate** button to perform ECal Calibration.

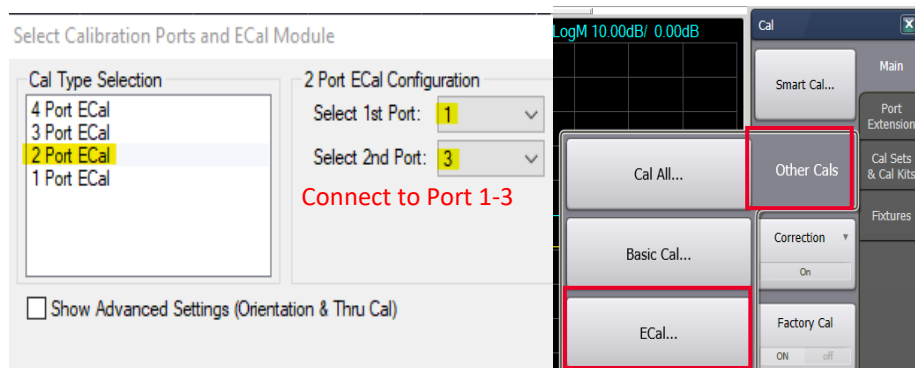


6. Click **Next** > to proceed. Completed calibration will show Green ✓ sign.
7. Click **Finish** to complete the ECal.

ECal calibration on frequency domain

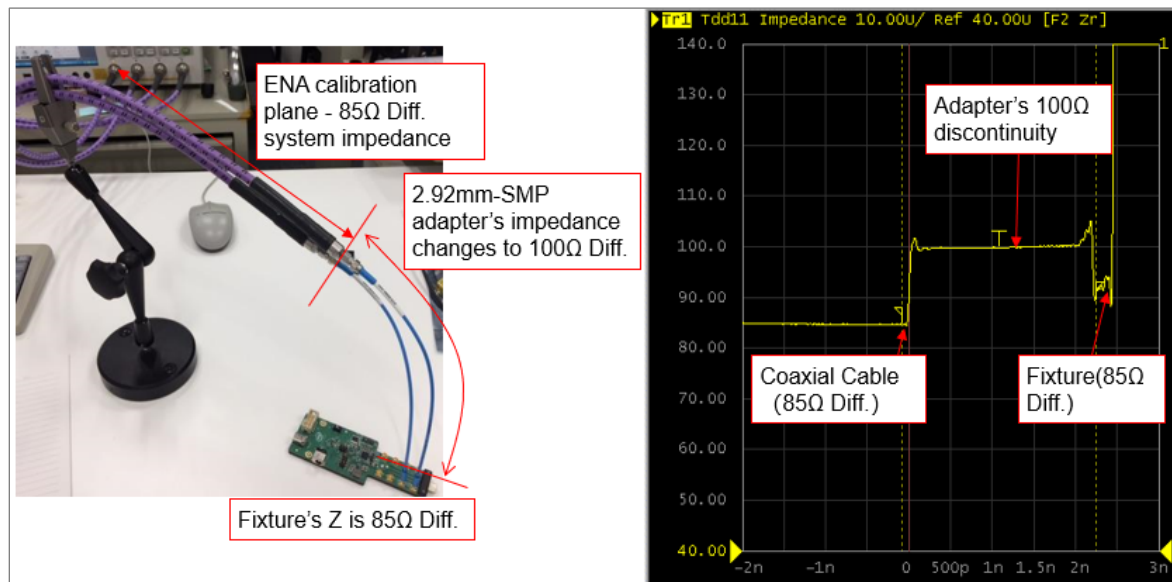
ECal calibration for frequency-domain measurements are performed by the VNA firmware.

1. Press **Channel Next** to select Channel 2.
2. Connect the VNA ports (Port 1 and Port 3) to the ECal module with RF cables.
3. Press **Cal** > **Main** > **Other ECal** > **Ecal...** > select **2-Port ECal** and click **Next** to proceed.
4. Click **Finish** when the ECal is completed.



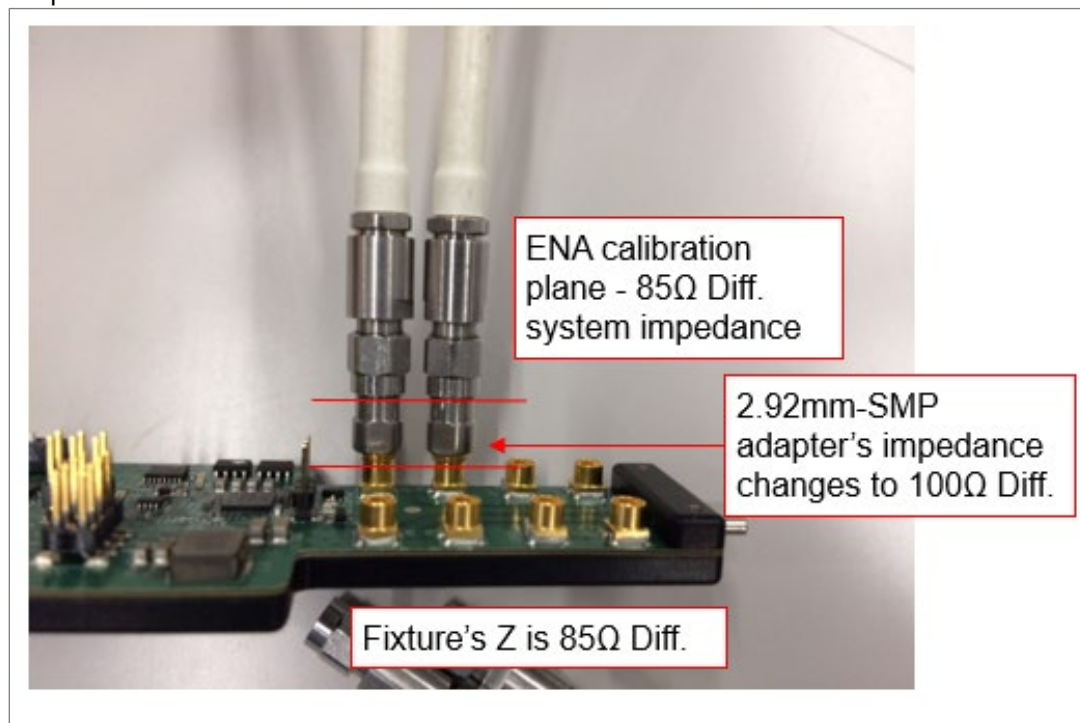
Gating setup – for legacy SMP type test fixture only

USB4 or Thunderbolt system impedance is set to 85Ω Differential. Both VNA and Wilder fixtures have 85Ω Differential system impedance. The 100Ω impedance discontinuity from 2.92mm-SMP needs to be canceled by applying the gating function.



Gating setup in time domain

1. Connect fixture to DUT as shown in reference setup above: Rosenberger 2.92mm-SMP adapter should be used.



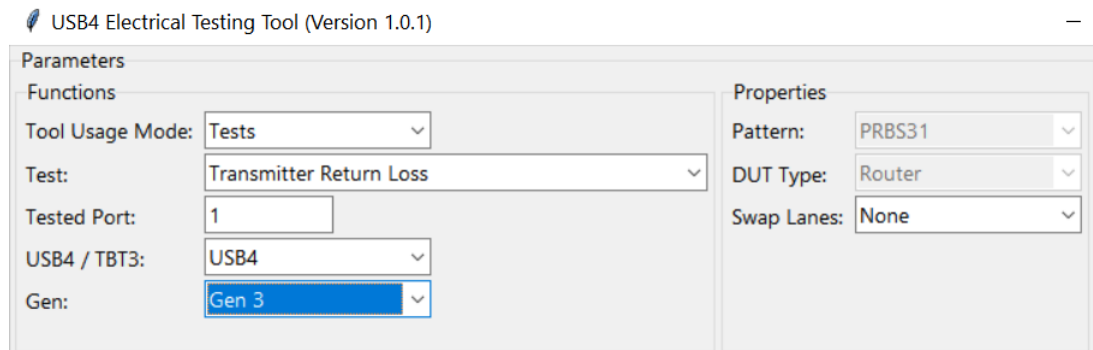
- Execute “**USB4 ETT**” tool. This script is used to control the DUT transmitter to output PRBS31 on all lanes with SSC turned on during the Return Loss measurement.

Test = Transmitter Return Loss/Receiver Return Loss

USB4/TBT3 = DUT type (USB4 or TBT3);

Gen = Gen 2 or Gen 3

Swap Lanes = None



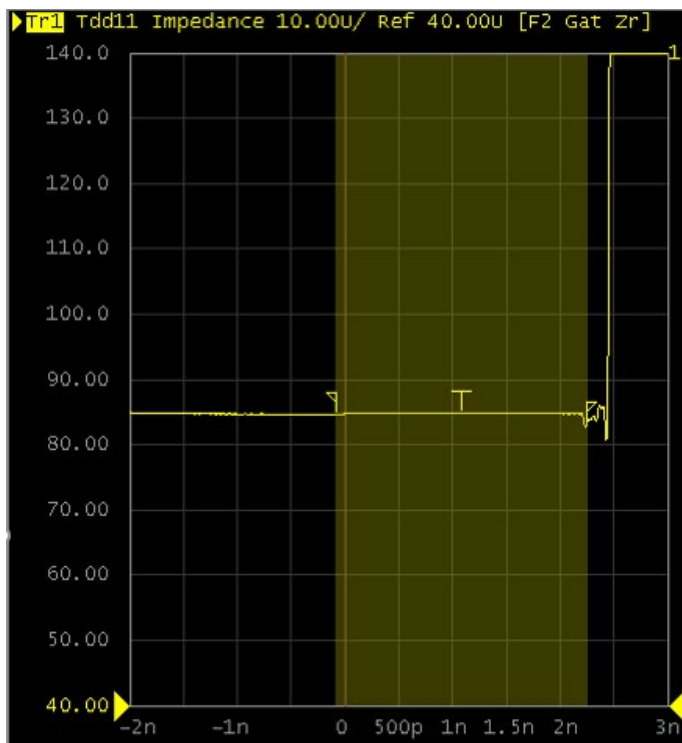
- Select **Trace 1** (Tdd11).
- Open **TDR/TDT** tab.
- Click **Gating** tab.
- Select Type “**Notch**” to remove the response inside the gate range.
- Place the markers and record the Start / Stop point of 100Ω discontinuity.



- Key-in Start / Stop timing value from Step 7 in Gating parameters.



9. Select and check “**Gating**” to enable the Gating feature. The impedance of Gating window (Yellow) is set to system impedance (85Ω Diff.)





10. After Enabling the Gating function, the DUT's impedance will change. Fine-tune Start / Stop value to maintain DUT's impedance value. DUT's impedance should not change after Gating.

Gating setup in frequency domain

Note: Please ensure that the VNA firmware revision is at least version **A.17.25.05** or above to enable SNP measurement with gating function.

1. Setup all the four traces (S11/ S13/S31/S33) on the VNA screen. The SNP with gating will only turn on the gating parameters on displayed traces.
2. Setup Macro to enable SNP with gating function. **Macro** > Key Setup > Macro Setup > Edit > load and saved the macro as snpgating.vbs file.

Text of macro:

```
dim vna: set vna = CreateObject("AgilentPNA835X.application")
dim scpi: set scpi = vna.ScpiStringParser

const DISABLED = 0
const ENABLED = 1
dim messages: messages = Array ("Is Disabled", "Is Enabled")

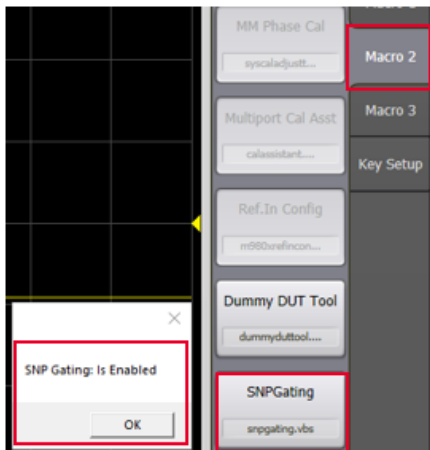
' Query the current state of SNP Gating
dim gating: gating = Scpi.Execute("DIAG:FEAT:ENAB? 'SNP_AllowGating'")

' Toggle the next state
dim nextState: nextState = ENABLED
if (CInt(gating)<> 0) then
    nextState = DISABLED
end if

' Send the next state
Scpi.Execute("DIAG:FEAT:ENAB 'SNP_AllowGating', "&nextState)

' Verify the state'
gating = Scpi.Execute("DIAG:FEAT:ENAB? 'SNP_AllowGating'")
'Annotate the state'
MsgBox("SNP Gating: "&messages(gating))
```

After saved, go to **Macro 2** > click on **SNPGating** and click **OK**. This will enable the “SNP Gating” on all the displayed traces on VNA.

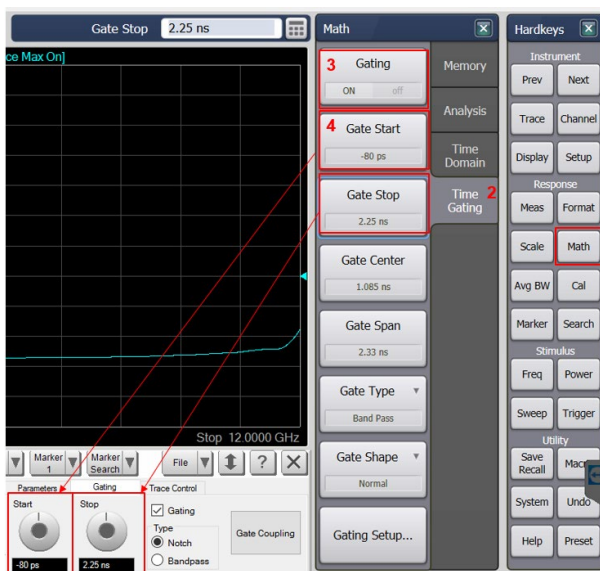


Note: VNA FW version A.17.25.05 & above enable SnP with gating on displayed traces only.

- Press **Math** > Time Gating > Turn Gating “ON”.



- Set the “Gate Start” and “Gate Stop” value as Time Domain channel. Select Gate type = “Notch”



Measurement and Data Analysis

Test parameters	USB4v1 – Legacy	USB4v1 – New	USB4v2
Test fixture	USB4 2.92mm SMP fixtures - Gating setup is required - Lane loopback routing for TX to RX	USB4v1 SMA fixtures - No gating setup or fixture de-embedding is needed.	USB4v1 SMA fixtures - No gating setup or fixture de-embedding is needed.
DUT topology	Default Port 1-2 SigTest accept S2P file at Port1-3 setting	Port 1-3 SigTest accept S2P file at Port1-3 setting	Port 1-3 SigTest accept S2P file at Port1-3 setting
Return loss	SigTest: Sdd22 and Scc22 (Normative)	SigTest: Sdd22 and Scc22 (Normative)	SigTest: Sdd22 only (Informative)
Integrated return loss	Not required	Not required	SigTest: IRL TX IRL – Normative RX IRL - Informative
TX's PAM3_PRTS7 waveform Bin file	Not required	Not required	Required for TX's IRL

USB4v1 return loss

USB4v1 return loss has changed to use SigTest tool compilation instead of VNA measurement. Only S2P file measurement is required. VNA traces with limit line can be used for debug purposes. **Note:** VNA firmware must be version **A.17.25.05** onwards to enable SNP with gating.

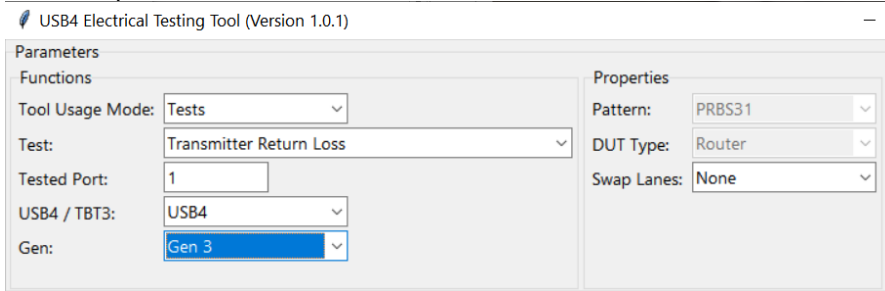
SigTest: Transmitter and receiver return loss (Sdd22/Scc22)

1. Connect the VNA ports (Port 1 to 3) to USB4 test fixture ports with RF cables according to the Table below. Follow Test Setup Diagram for cable and fixture connections.

VNA port#	Port 1	Port 3
TX test fixture	TX_P	TX_N
RX test fixture	RX_P	RX_N

2. Press Channel Next to select Channel 2 (Frequency Domain).
3. **[For Legacy 2.92 mm SMP test fixture]**, make sure you have setup the gating Start/Stop timing for frequency domain and turn on macro for SNPGating.
[For SMA test fixture] The transmitter and receiver return loss setup will be different using separate test fixtures. Refer to test setup diagram for details.
4. Select **Cal** > Fixtures > Fixture Setup > right click Port Z Conversion... uncheck "Enable Port Z Conversion (all ports)" to turn OFF Port Z Conversion. SigTest tool will normalize the S2P data to 85-Ohm during result compilation.
5. Execute **"USB4 ETT tool"** to control the DUT transmitter/receiver to output PRBS31 on all lanes with SSC turned on during the Return Loss measurement.
 - Test = Transmitter/Receiver Return Loss

- USB4/TBT3 = DUT type (USB4 or TBT3)
- Swap Lanes = None



6. Setup **Trace 1/2/3/4 (S11/S13/S31/S33)** for SNP measurement.



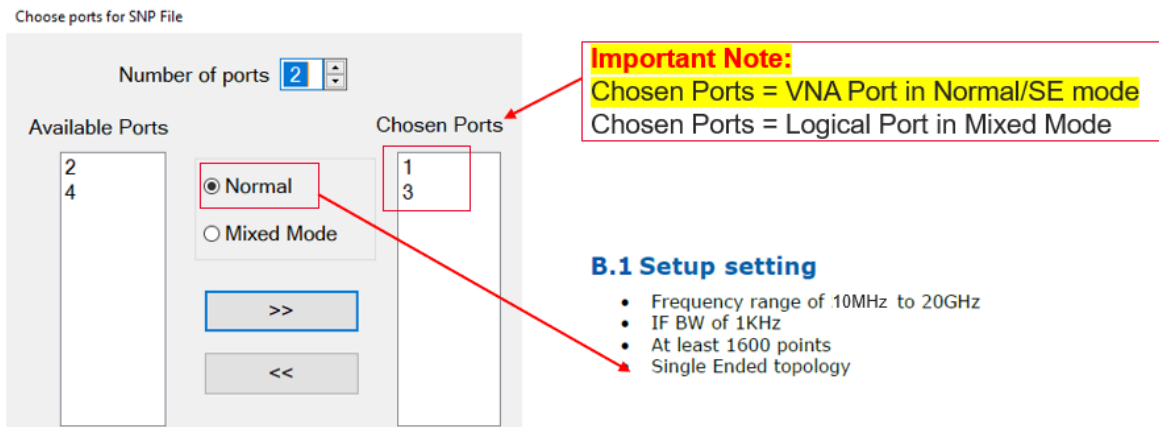
Note: VNA FW version A.17.25.05 & above enable SnP with gating on displayed traces only.

7. Press **Trigger** > Single.

Note: Before saving measurement data, always trigger a single measurement, and then allow the channel to go into Hold. This ensures that the entire measurement trace is saved.

8. Save S2P file: **Save Recall** > Save Other > Save Data.

9. Select "**Normal**" mode to save single-ended measurement. Select "**Chosen Ports**" to **Port 1 and 3** (VNA port). Note: BAL DUT topology allows users to select between Normal/Mixed Mode data.



10. Run SigTest tool to verify RL – Sdd22 and Scc22 pass/fail results. Press SHIFT + Right Click to call out Window PowerShell on your SigTest.exe folder.

TX lanes: Expected inputs are s2p file only

SigTest command: .\USB4_SigTest.exe *gen3_rounded tx tp2 rl .\Waveform\ none none rl_report none [RL_TXlane.s2p]*

RX lanes: Expected input is s2p file only

SigTest command: `.\USB4_SigTest.exe gen3_rounded rx tp2 rl .\Waveform\ none none rl_report none [RL_RXlane.s2p]`

SigTest supports all USB4 bitrates.

gen2_rounded = 10Gb/s

gen3_rounded = 20Gb/s

gen2_legacy = 10.3125Gb/s

gen3_legacy = 20.625Gb/s

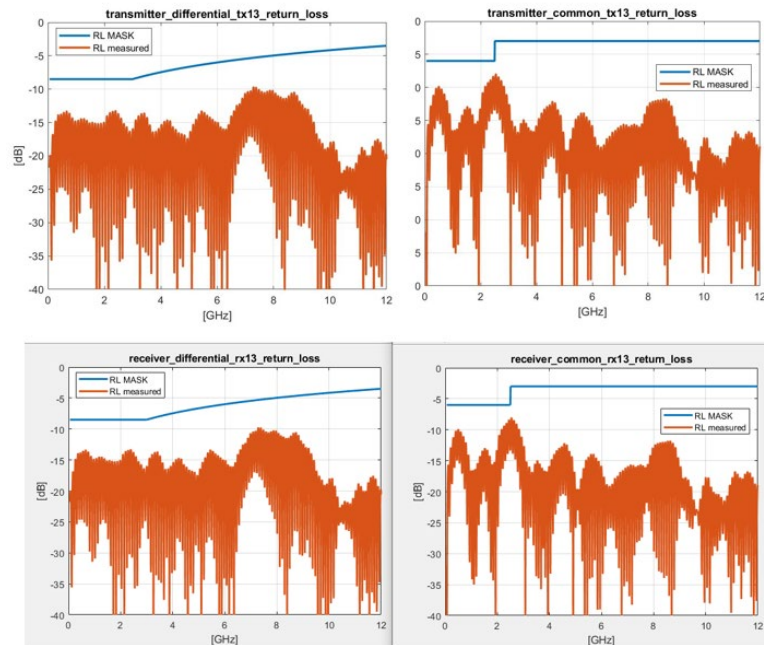
11. Verify pass/fail result from SigTest output csv file.
12. Repeat the test for all remaining USB4 lanes.
13. Repeat the test for all supported USB4 Gen2 and Gen3 speeds by changing USB4ETT tool parameter.

Windows PowerShell

SHIFT + Right Click to call out Window PowerShell on your folder

```
***** SIGTEST Version: 0.75 *****
Running SIGTEST : Technology : GEN3_ROUNDED, TestMode : TX, TestPoint : TP2
The following tests are in progress ...
Transmitter Return Loss
Reading S parameters File: .\Waveform\TX0_P13.s2p ..
The .\Waveform\TX0_P13.s2p Sparameters is normalized to 42.500000[ohm]
Writing rl_report
Writing rl_report
Writing result to
The tests are complete
```

Date:	25-Aug-22				
DIR:	.\Waveform\				
File:	none				
Transmitter Return Loss					
Normative:	Sdd22 MASK:	PASS			
Normative:	Sdd22 max[dB]	-9.7	Margin[dB]	4.4	Fmax[GHz] 7.287219
Normative:	Scc22 MASK:	PASS			
Normative:	Scc22 max[dB]	-8.4	Margin[dB]	2.4	Fmax[GHz] 2.447469



USB4v2 return loss and integrated return loss

USB4v2 return loss (Sdd22) and Integrated Return Loss (IRL) are measured by S-parameter touchstone file and SigTest tool compilation. VNA traces can be used for debug purposes.

Test parameters	Transmitter, TX	Receiver, RX
Differential return loss, Sdd22	Informative	Informative
Integrated return loss, IRL	Normative	Informative

1. Connect the VNA ports (Port 1 to 3) to USB4v2 test fixture ports with RF cables according to the Table below. Follow the Test Setup Diagram for cable and fixture connections.

VNA port#	Port 1	Port 3
TX test fixture	TX_P	TX_N
RX test fixture	RX_P	RX_N

2. Press Channel Next to select Channel 2 (Frequency Domain).
3. Select **Cal** > Fixtures > Fixture Setup > right click Port Z Conversion... uncheck "Enable Port Z Conversion (all ports)" to turn OFF Port Z Conversion. SigTest tool will normalize the S2P data to 85-Ohm during result compilation.
4. Execute the "**USB4ETT tool**" to control the DUT transmitter/receiver to output PRTS7 on the lane under test; the remaining lanes should be activated as aggressors transmitting PRTS19, with SSC turned on during the Return Loss measurement.
 - Test = Transmitter/Receiver Return Loss
 - USB4/TBT3 = DUT type (USB4 or TBT4)
 - Gen: Gen4
 - Swap Lanes = None
5. Setup **Trace 1 (S11)** for SNP measurement.

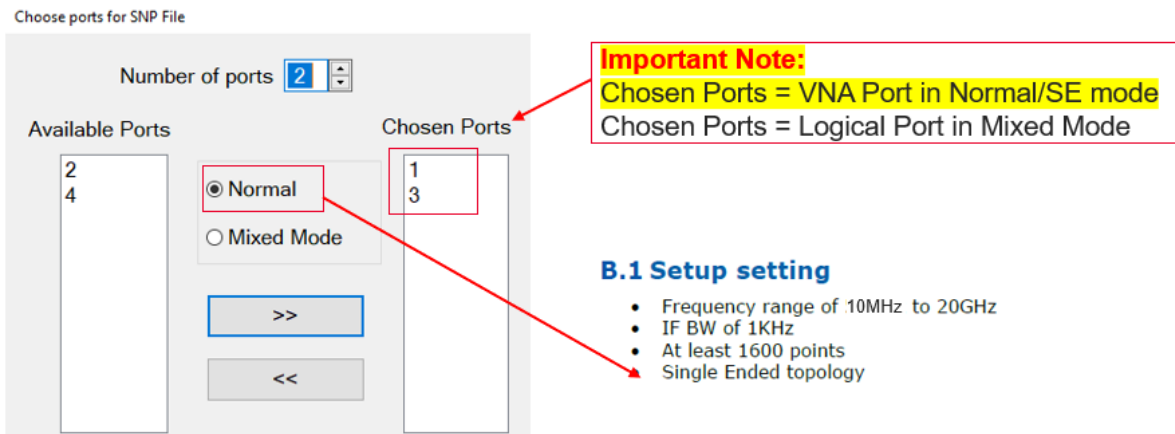
Note: VNA FW version A.17.25.05 & above enables SnP with gating on displayed traces only. If gating is needed (not mandatory for USB4v2), refer Gating setup to enable macro and display all 4 traces (SS11/S13/S31/S33) before measurement.



6. Press **Trigger** > Single.

Note: Before saving measurement data, always trigger a single measurement, and then allow the channel to go into Hold. This ensures that the entire measurement trace is saved.
7. Save S2P file: **Save Recall** > Save Other > Save Data

8. Select “Normal” mode to save single-ended measurement. Select “Chosen Ports” to **Port 1 and 3** (VNA port). Note: BAL DUT topology allows users to select between Normal/Mixed Mode data.



9. Run SigTest to verify RL (SDD22) and IRL pass/fail results. Press SHIFT + Right Click to call out Window PowerShell on your SigTest.exe folder.

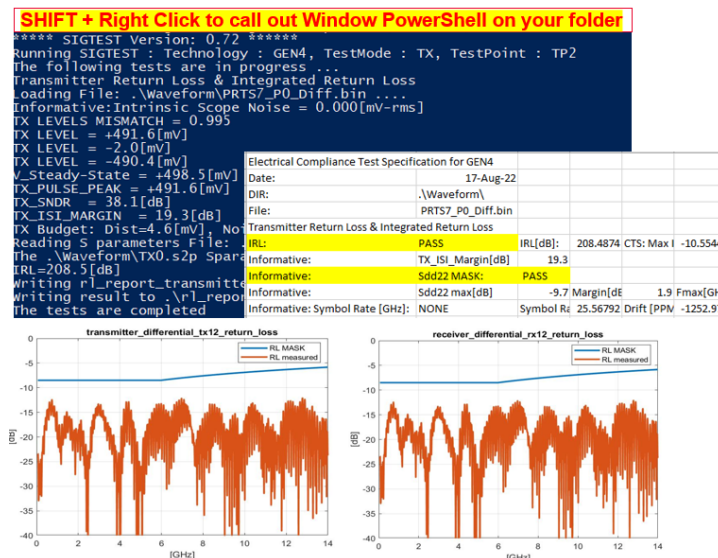
TX lanes: Expected inputs are s2p file and PAM3_prts7_waveform.bin of ui_jitter_vertical that used in Timing and Voltage measurement test.

SigTest command: `.\USB4_SigTest.exe gen4 tx tp2 rl .\Waveform\[TX_waveform.bin] none rl_report none [RL_TXlane.s2p]`

RX lanes: Expected input is s2p file only, no signal waveform is required.

SigTest command: `.\USB4_SigTest.exe gen4 rx tp2 rl .\Waveform\[none] none rl_report none [RL_RXlane.s2p]`

10. Verify pass/fail result from SigTest output csv file.
11. Repeat the test for all remaining USB4 lanes.
12. Repeat the test for all supported USB4 Gen2 and Gen3 speeds by changing USB4ETT tool parameter.



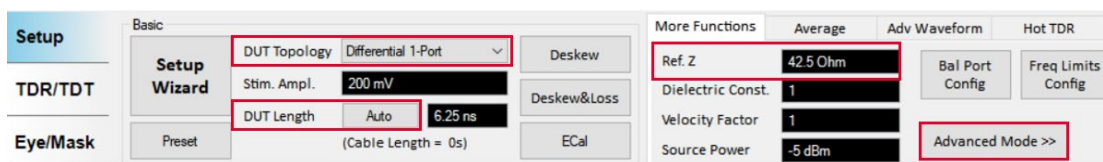
Manual Setup

The procedures of manual setup for time domain and frequency domain measurements are introduced in this section for reference. All the required testing parameters have been properly set and saved in the respective standards testing state file (*.tdr).

Channel & trace setup

If TDR setup wizard is shown when launching the TDR software, click **Close** button in the TDR setup wizard main window.

1. Open **Setup** tab in the TDR software
2. Click **Preset** to preset the instrument Click OK in a dialog box to continue.
3. Set **DUT Topology** to “**Differential 1 Port**” Click OK in a dialog box.
4. Click **Advanced Mode>>** and click Yes to enter to Advanced mode.
5. Set DUT Length to “Auto”.
6. Ref. Z = “42.5 Ohm”

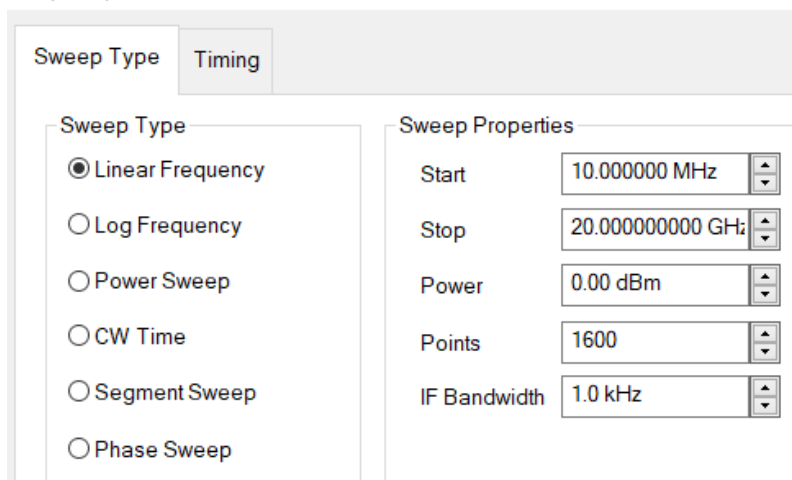


Frequency range setup

1. Based on USB4 CTS, setup the required testing requirements.
2. Select Sweep > Sweep Setup and key-in sweep properties as below:

Note: The latest USB4 CTS (Feb-2023) required the starting frequency at 10MHz.

Sweep Setup: Channel 2

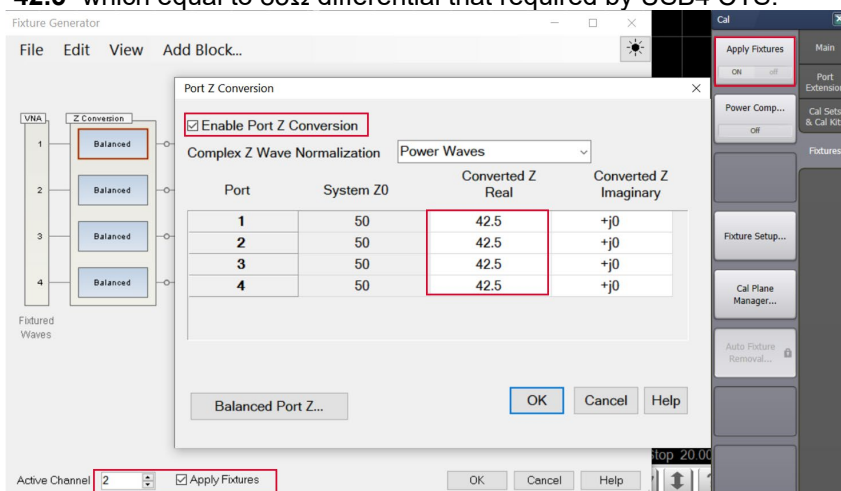


Run return loss from VNA trace (for USB4v1 only)

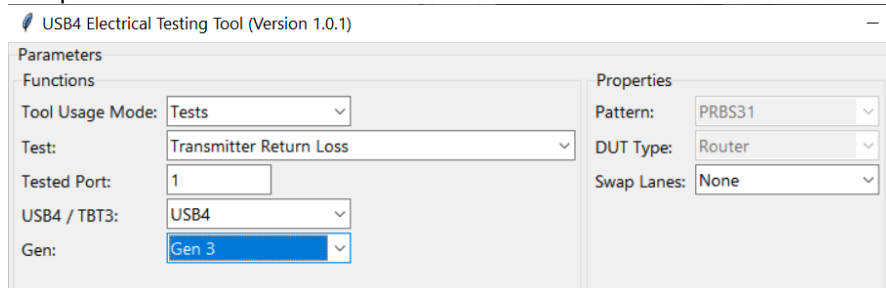
1. Connect the VNA ports (Port 1 to 3) to USB4 test fixture ports with RF cables according to the Table below. Unused TX/RX lanes that are not under test should be terminated with 50-ohm terminators.

VNA port#	Port 1	Port 3
TX test fixture	TX_P	TX_N
RX test fixture	RX_P	RX_N

2. Press Channel Next to select Channel 2 (Frequency Domain).
3. **[For Legacy 2.92 mm SMP test fixture]**, make sure you have setup the gating Start/Stop timing for this all the traces.
[For SMA test fixture] The transmitter and receiver return loss setup will be different using separate test fixtures. Refer to test setup diagram for details.
4. Select **Cal > Fixtures > Fixture Setup > right click Port Z Conversion...** check “**Enable Port Z Conversion (all ports)**” to turn ON Port Z Conversion. Make sure the **System Z0** is set to “**42.5**” which equal to 85Ω differential that required by USB4 CTS.



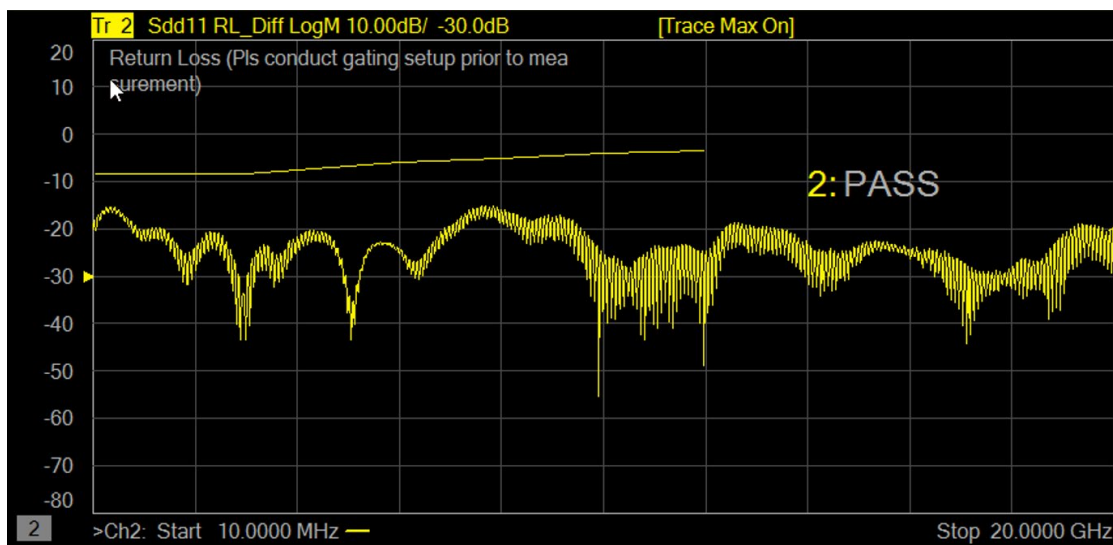
5. Execute “**USB4 ETT tool**” to control the DUT transmitter/receiver to output the required pattern with SSC turned on during the Return Loss measurement.
 - Test = Transmitter/Receiver Return Loss
 - USB4/TBT3 = DUT type (USB4 or TBT3)
 - Gen: Gen4/Gen3/Gen2
 - Swap Lanes = None



6. Select **Trace 2 (Sdd11) / Trace 2 (Scc11)** for differential return loss or common-mode return loss.
7. Press **Double-click** on the instrument front panel to enlarge the trace.
8. Press **Trigger** > Single.
9. Run and confirm the measured values are within the limit shown below. Otherwise, it will show Fail.

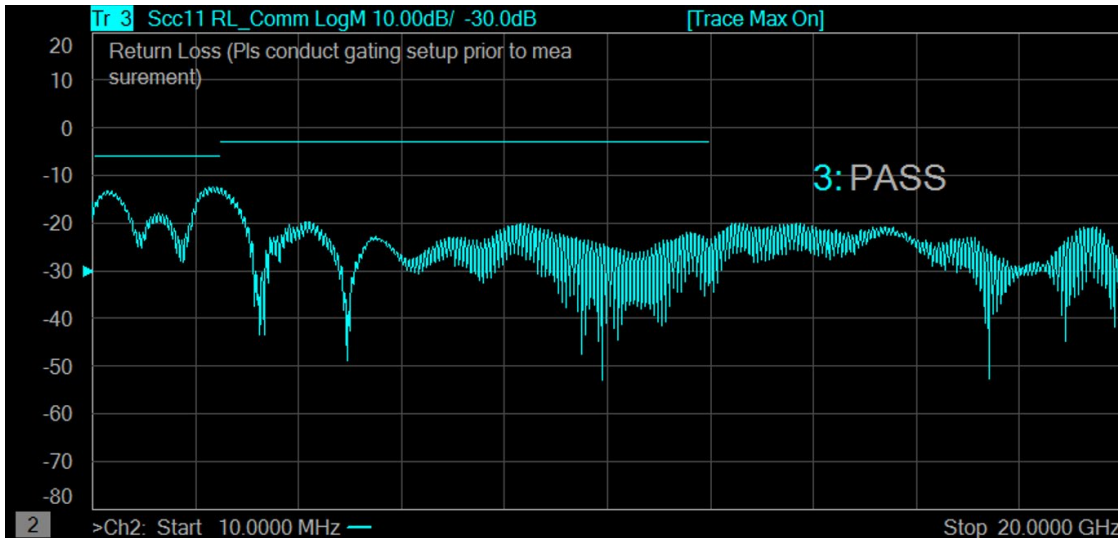
TX and RX differential return loss limit

Frequency	Stop frequency	Start limit	Stop limit
0.05 GHz	3.00 GHz	-8.50 dB	-8.50 dB
3.00 GHz	4.00 GHz	-8.50 dB	-7.50 dB
4.00 GHz	6.00 GHz	-7.50 dB	-6.00 dB
6.00 GHz	8.00 GHz	-6.00 dB	-5.00 dB
8.00 GHz	10.00 GHz	-5.00 dB	-4.15 dB
10.00 GHz	12.00 GHz	-4.15 dB	-3.50 dB



TX and RX common-mode return loss limit

Frequency	Stop frequency	Start limit	Stop limit
0.05 GHz	2.50 GHz	-6.0 dB	-6.0 dB
2.50 GHz	12 GHz	-3.0 dB	-3.0 dB



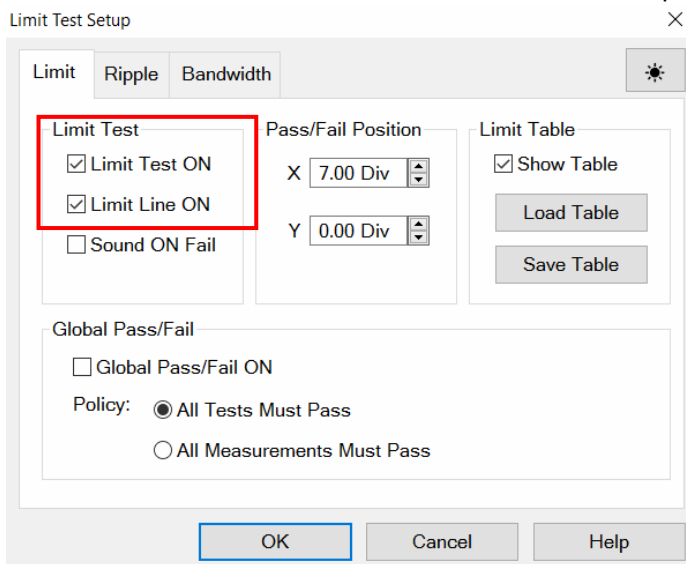
10. Repeat the test for all remaining USB4 lanes.
11. Repeat the test for all supported USB4 Gen2 and Gen3 speeds by changing USB4ETT tool parameter.

Defining limit line tables

1. Press **Trace Next** to select trace to set the limit line table.
2. Press **Math> Analysis > Limit Table >** to edit the limit table.

	Type	Begin Stimulus	End Stimulus	Begin Response	End Response
1	Max	0.000000 Hz	5.00000 GHz	-30.0000 dB	-30.0000 dB
2	Off	0.000000 Hz	0.000000 Hz	0.000000 dB	0.000000 dB

3. Press **Math> Analysis > Limit... >** to launch Limit Test Setup window.
4. Select to turn on “Limit Test ON” and “Limit Line ON”, optional to turn on “Sound ON Fail”.



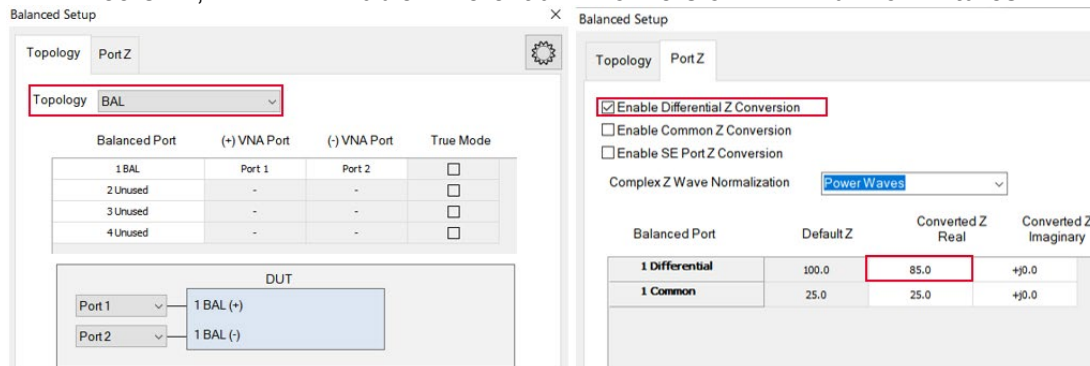
Setup impedance measurement using S9x010B time-domain option

Option 010 do not have a direct TDR trace and required manual setup to transform the frequency-domain trace to time-domain for impedance measurement.

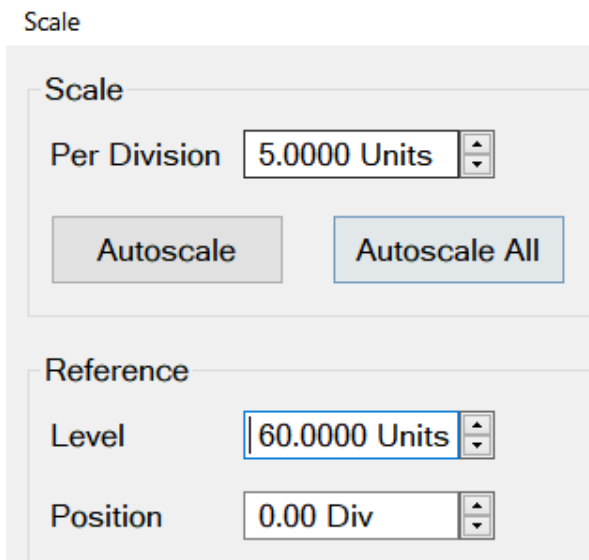
1. Add a new trace of Sdd1. Press **Meas** > Balanced >

Topology = **BAL**

PortZ = **85 Ohm**, check to “**Enable Differential Z Conversion**” and “**Turn on fixtures**”.



2. Select Trace Sdd11. Press **Math**> Time Domain > Transform “**ON**”. The trace will be transformed to time-domain.
3. Press **Math**> Analysis > Conversions > Z-Reflect
4. Select the Trace Sdd11, right click > Format > Linear Mag
5. Select the Trace Sdd11, right click > Scale >



6. Add Marker-1 and Marker-2 to measure Start/Stop timing of the 100 Ohm impedance.
7. Press **Math**> Time Gating > Gating “**ON**”. Gate Type = “**Notch**”
8. Insert **Gate Start/Gate Stop** timing acquired from impedance measurement previously.
9. Use the same **Gate Start/Gate Stop** value for **Sdd11 differential return loss** and **Scs11 Common mode return loss** measurements.
10. To search your Max/Min value of the trace, use the Search function.
 - Click Search> **Search...**

- Select “User 1” for Search Domain
- Enter the span range in time domain depending on DUT’s cable length (ex. Start = -1ns, Stop = 10 ns)
- Select “Maximum”
- Check “Tracking”
- Click “Execute” to search for the max impedance value in the range
- Click “OK”

Marker Search ×

Marker 1 ▾

☒ On

Search Type

Maximum ▾

Execute

☒ Tracking

Search Range

User 1 ▾

User Start -1.000000000 s ▴ ▾

User Stop 1.000000000 s ▴ ▾

Web Resources

[D9050USBC USB4 Version 2.0 Tx Test Software | Keysight](#)

[D9040USBC USB4 Tx Test Software | Keysight](#)

[USB4 Transmitter Compliance Test | Keysight](#)

[USB4 Receiver Compliance Test | Keysight](#)

[USB-C Testing For High Speed Interconnects | Keysight](#)

www.keysight.com/find/usb-c-testing

www.keysight.com/find/S94USBCB

www.keysight.com/find/ena-tdr_compliance

www.keysight.com/find/usb-vna

www.keysight.com/find/na

www.keysight.com/find/vnasoftware

www.keysight.com/find/ecal

For more information on Keysight Technologies' products, applications, or services,
please visit: www.keysight.com



This information is subject to change without notice. © Keysight Technologies, 2020 - 2024,
Published in USA, February 7, 2024, 3120-1446.EN