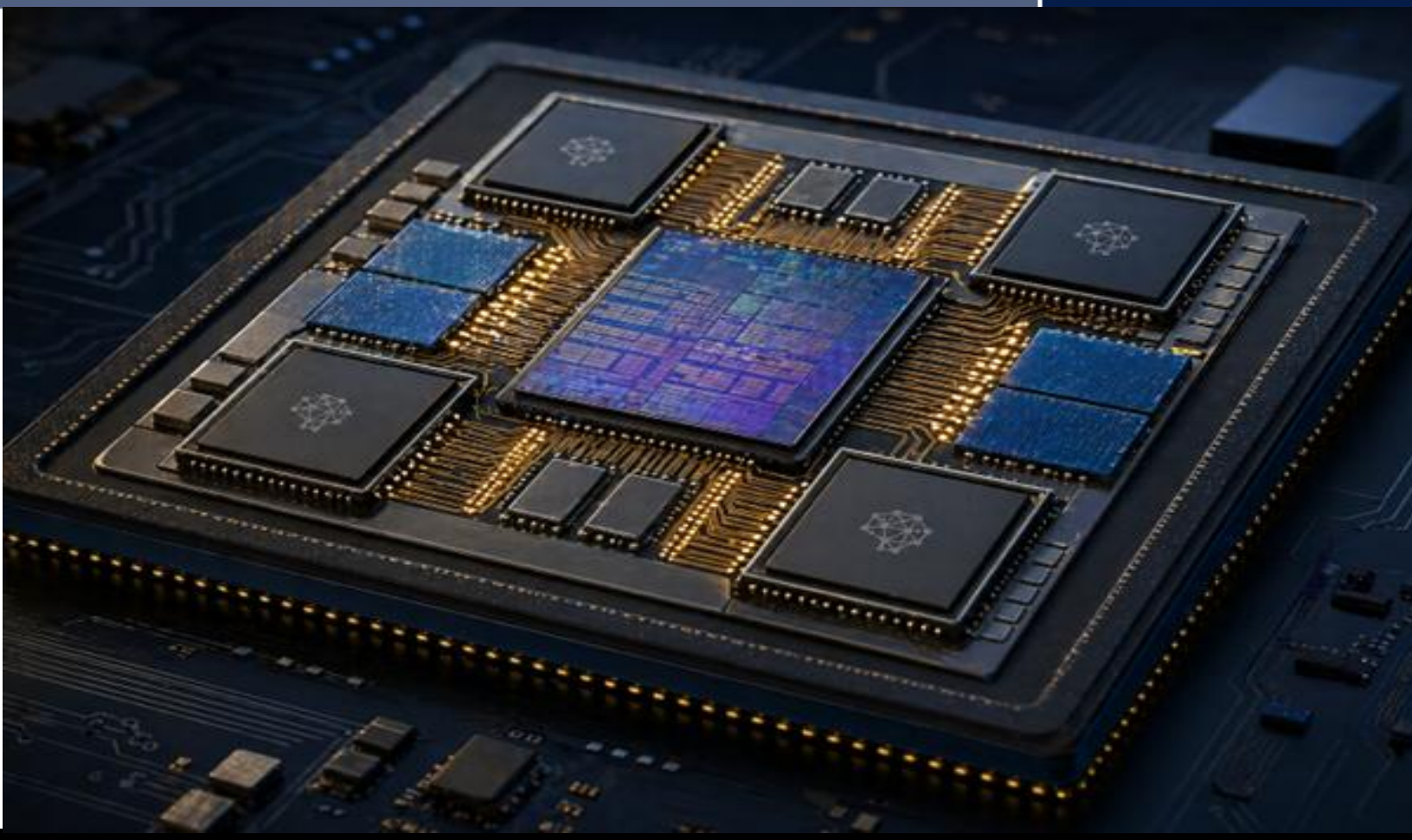
CASE STUDY



Intel Foundry Enables Pre-Silicon Validation for Next-Generation Chiplet Designs

Semiconductor and Advanced Packaging

Based on press release April 29, 2025

Keysight EDA and Intel Foundry Collaborate on EMIB-T Silicon Bridge Technology for Next-Generation AI and Data Center Solutions

KEYSIGHT

01 Company

Intel Foundry, provider of semiconductor process and advanced packaging technologies

02 Solutions

Keysight Chiplet PHY Designer with support for Intel Foundry EMIB-T, UCIe® 2.0, and Open Compute Project Bunch of Wires

03 Challenge

Improve chiplet interoperability, link margin validation, and system-level performance for AI and data center packaging

04 Results

Enabled an EMIB-T workflow for system-level link performance and compliance validation before manufacturing

AI and data center workloads are increasing demand for high-performance semiconductor packaging. These systems require reliable communication between chiplets and 3D integrated circuits, along with high-speed data transfer and efficient power delivery for next-generation semiconductor applications.

Keysight EDA and Intel Foundry collaborated to support Embedded Multi-die Interconnect Bridge-T (EMIB-T) technology using Keysight Chiplet PHY Designer. The workflow supports emerging interconnect standards, including Universal Chiplet Interconnect Express 2.0 and Open Compute Project Bunch of Wires, to improve chiplet design flexibility and enable pre-silicon validation.

> “By integrating standards like UCIe® 2.0, we enhance chiplet design flexibility for AI and data center applications, accelerating innovation and ensuring our customers meet next-generation demands with precision.”

Suk Lee

Vice President and General Manager, Ecosystem Technology Office, Intel Foundry

The Challenge

AI and data center systems are driving new requirements for semiconductor performance, bandwidth, and packaging density. To meet these demands, chiplet-based architectures and advanced packaging technologies are becoming more important across the semiconductor ecosystem.

Chiplet systems depend on reliable communication between multiple dies. Designers must account for signal integrity, power delivery, link performance, and standards compliance across complex interconnect structures. These challenges are especially important in 2.5D and 3D integrated circuit designs, where die-to-die connections must perform predictably within advanced packages.

Open standards such as Universal Chiplet Interconnect Express (UCIe) and Bunch of Wires (BoW) are helping the industry create more consistent approaches to chiplet interconnect. However, adopting standards is only part of the challenge. Designers also need validation workflows that can confirm compliance and evaluate link margin before silicon is manufactured.

For Intel Foundry's EMIB-T technology, the need is clear: advanced packaging must be supported by practical EDA workflows that help engineers evaluate performance earlier in the design process. Without pre-silicon validation, teams risk discovering issues too late, when changes can be costly and schedules are harder to protect.

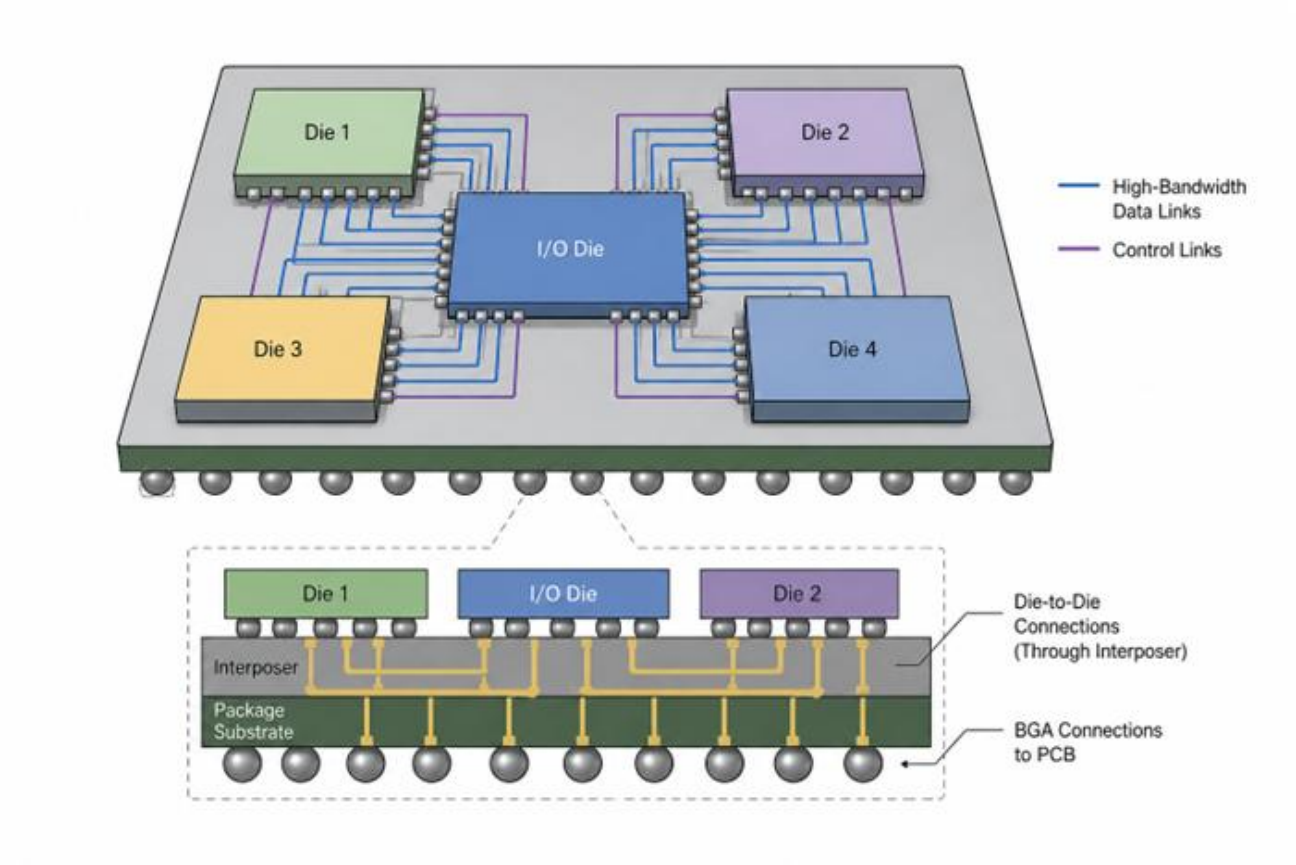


Figure 1. Multi-die package diagram shows die-to-die interconnect complexity

The Solution

Keysight EDA collaborated with Intel Foundry to support EMIB-T technology within Keysight Chiplet PHY Designer. EMIB-T is aimed at improving high-performance packaging solutions for AI and data center markets, including support for Intel 18A process node workflows.

Chiplet PHY Designer is a system-level chiplet and die-to-die design solution for high-speed digital applications. It enables pre-silicon validation and helps engineers evaluate system-level link performance and compliance before tapeout. In this collaboration, the solution added advanced simulation capabilities for the UCIe 2.0 standard and introduced support for the Open Compute Project BoW standard.

The workflow supports a standards-based approach to chiplet design. By enabling engineers to evaluate compliance and link margin earlier, the solution helps address a major risk area in advanced semiconductor development: the gap between package-level design intent and real-world link behavior.

For Intel Foundry, this collaboration supports EMIB-T adoption by giving customers a validation path aligned with emerging chiplet standards. For semiconductor design teams, it provides a more practical way to evaluate high-speed data transfer, interoperability, and system-level performance in advanced packages for AI and data center applications.

Keysight EDA 2025 for High-Speed Digital Design

Figure 2. Keysight EDA's Advanced Design System provides a powerful, integrated design and simulation environment to create digital twins and handle the complexities of SerDes designs, such as chiplets, memory, USB, and PCIe®

Results

The collaboration enabled an EMIB-T workflow for system-level link performance and compliance validation. Keysight planned to demonstrate the workflow at Intel Foundry Direct Connect, featuring Intel Foundry's EMIB-T technology and Keysight Chiplet PHY Designer capabilities.

The result gives chiplet designers a standards-based method to validate designs before manufacturing. That supports the broader goal of reducing development costs, mitigating risk, and accelerating semiconductor innovation. It also helps improve design flexibility by aligning EMIB-T workflows with UCIe 2.0 and BoW standards.

For AI and data center applications, this validation capability is especially important. These systems require high-speed data movement and efficient power delivery across advanced multi-die packages. Earlier validation helps engineering teams identify issues before they become manufacturing risks.

The work contributes to the growing chiplet interoperability ecosystem. By supporting compliance and link margin evaluation in a pre-silicon workflow, Keysight and Intel Foundry help make advanced packaging more accessible to design teams building next-generation AI and data center solutions.

Conclusion

Chiplet-based design is becoming essential for high-performance AI and data center systems. As packaging architectures become more complex, engineers need standards-based validation workflows that can help confirm performance before silicon is manufactured.

Keysight Chiplet PHY Designer supports Intel Foundry EMIB-T technology with pre-silicon validation for system-level link performance and compliance. The collaboration helps designers evaluate chiplet interconnect behavior earlier, reduce design risk, and support more flexible advanced packaging workflows.

Related Information

- Keysight Chiplet PHY Designer
- Intel Foundry EMIB technology
- Universal Chiplet Interconnect Express
- Keysight EDA and Intel Foundry Collaborate on EMIB-T Silicon Bridge Technology for Next-Generation AI and Data Center Solutions, April 29, 2025 press release