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ABCs of Writing a Custom Boundary Scan Test

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ABCs of Writing a Custom Boundary Scan Test

Sample vectors and code for expanding test coverage.

BOUNDARY SCAN OR JTAG (Joint Test Action Group) is an IEEE Standard 1149.1 that defines the test access port and boundary scan architecture of digital integrated circuits. Boundary scan is a test technique that involves devices designed with shift registers placed between each device pin and the internal logic (FIGURE 1). Each shift register is called a boundary scan cell. These boundary scan cells allow control and observation of what happens at each input and output pin. When these cells are connected together, they form a data register chain called the boundary register.

Boundary scan has become an important limited access solution for printed circuit board assemblies, and includes tests for digital integrated circuits interconnection, as well as testing and programming digital devices such as flash, EEPROM and serial peripheral interface (SPI) devices. Boundary scan also has the capability to execute other tests, as defined in the BSDL (Boundary Scan Description Language), including private instructions which support internal functions of a boundary scan device, such as built-in self-test (BIST).

The boundary scan operation is controlled by a test access port (TAP), the control system of a boundary scan device. The TAP controller of a boundary scan device consists of a 16-state machine (FIGURE 2). The flow of data to the instruction register (IR) and the data register (DR) is controlled by the test mode select (TMS) with a 0 or 1 bit to move from one state to another state, while the TCK synchronizes the 16-state machine operation. The TAP controller state diagram shows the sequence of any boundary scan test through the TAP controller, and applies to components that comply with IEEE 1149.1.

Each position in the DR and IR columns represents a state of the TAP controller of the 16-state machine that controls each boundary scan device. The DR column comprises data instructions that, when passed through, affect the operation and contents of the data register. The DRs include bypass register, a mandatory register that all boundary-scan-compliant devices must contain. Either that or it will need to have the optional IDCODE, USERCODE registers, or a designer-specified register that complies with the IEEE standard.

The IR column comprises data instructions that, when passed through, affect the operation and contents of the IR, a mandatory component of every boundary scan device.

The success of boundary scan in the manufacturing test environment depends largely on the availability of ATPG (Automatic Test Program Generation), which can help test engineers develop and generate the boundary scan tests (Figure 2).

The following are examples of automatically-generated boundary scan tests:

1. Infrastructure test – Verifies that the TAP of all boundary scan devices in the chain operate properly. If this test fails, testing stops and power is disabled from the board. This test is a preamble to all other boundary scan tests; it is an integral part of each test and is executed before each test runs.
2. Interconnect test – Verifies the boundary scan device pins 1149.1 and 1149.6 interconnection with other boundary scan device pins.
3. Buswire test – The bus wire test looks for opens on all the bussed boundary scan devices

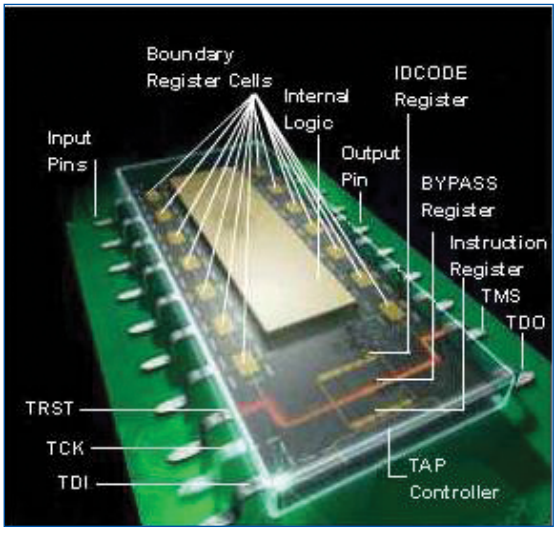

FIGURE 1. A boundary scan device.

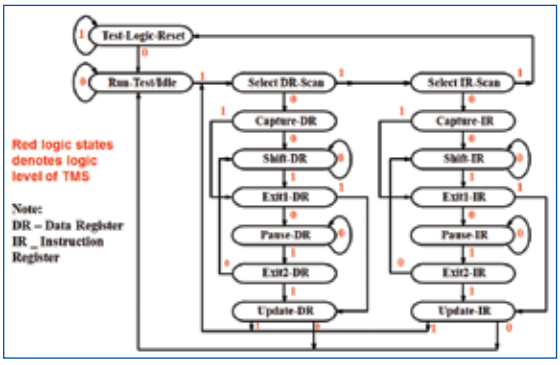

FIGURE 2. Test access port (TAP) state diagram.

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test developed on PC boundary scan tool can be executed at the ICT manufacturing test stage, if integrated into ICT.

- Integration of PC boundary scan tool in ICT during volume manufacturing will shorten development time, hence improving time-to-market.

FIGURE 1. M.2 SSD for tablet and laptop PC, the smallest commercial version.

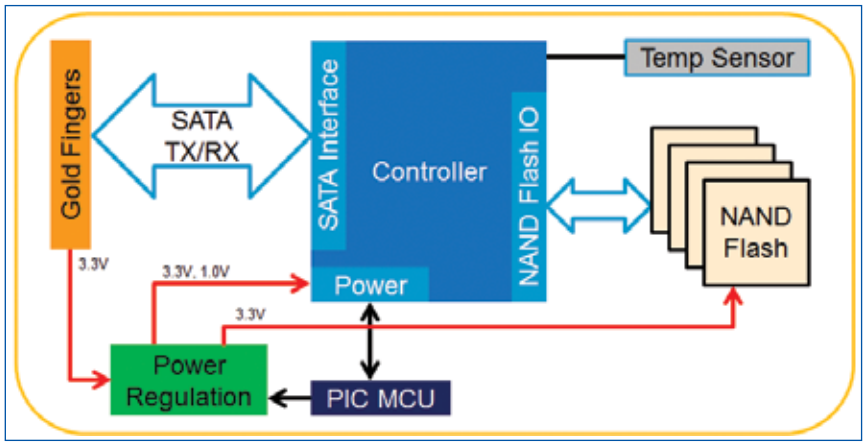

FIGURE 2. Typical tablet PC SSD block diagram.

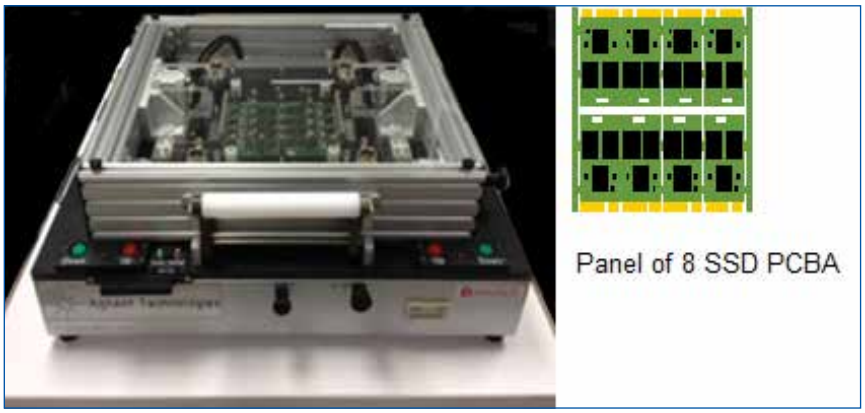

FIGURE 3. SSD fixture testing a panel of 8 SSD boards.

Not all SSDs are testable using ICT. Due to consumer demands for smaller, faster and longer battery life devices, the size of every component in electronics devices is also shrinking, including the printed circuit board.

Tablet/Notebook SSD. The smallest SSD form factor currently available in the market is the M.2 SSD (FIGURE 1), which supports the mSATA and PCIe interfaces normally used on tablet and notebook PCs due to their size and speed. FIGURE 2 shows the block diagram of an M.2 SSD, which consists of the NAND controller and NAND flash device.

The key manufacturing test challenges faced by tablet/notebook SSDs and smaller-sized HDD SSDs are that testpoints are limited, and very often these are available only for some critical nodes such as power and boundary scan pins. For this type of SSD, the boundary scan tool system is the only solution possible for manufacturing test.

Pc Boundary Scan Test

- PC boundary scan test can involve the following:
- Boundary scan interconnect and buswire test. Although there is only one boundary scan device, the interconnect and buswire will still be able to test a few pins that are interconnect or pins that have a self-monitoring boundary scan cell.
- Boundary scan pull-up/pull-down resistor.
- Boundary scan silicon nail: Tests interconnection between NAND controller and NAND flash devices.
- Loopback test between SATA/PCIe and NAND flash controller.
- Cover-Extend test for non-boundary scan devices and connectors.

In some cases programming is needed for SEEPROM, SPI flash and PIC devices.

There are limitations with using only the benchtop boundary scan tool, though. One is the issue of not being able to perform unpowered and powered tests, as an ICT system can. To resolve these limitations, a dedicated SSD manufacturing test solution has been developed to perform

both ICT and boundary scan test during volume manufacturing testing.

Setup of the manufacturing test system for SSD. The manufacturing test solution for SSDs comprises a benchtop boundary scan tool, measurement instrumentation and programmable power supply, with both hardware and software integrated. This solution is capable of performing unpowered short and open test using resistance measurement, as well as voltage measurement. This will ensure that important power nodes are tested the same way as they are in ICT. An advantage is that this is a lower-cost system compared with conventional ICT.

Advantages offered by the various instruments in this system include:

- Unpowered resistance measurement before powering up.
- During power up of the SSD PCBA, voltage and frequency measurements ensure that all the voltage rail and frequency on board are correct.
- Multiplex power supply, measurement and boundary scan test on a panel board.

The programmable power supply offers these benefits:

- Ability to control the supply voltage for the SSD board.
- Single universal power supply for different types of board and voltage requirements will enable testing of multiple SSD types.

The SSD manufacturing test solution will need a fixture (FIGURE 3) that will enable testing of a panel of SSD PCBAs for throughput enhancement and ease of handling by the production operator.

Such an SSD manufacturing test solution provides the following test coverage (FIGURE 4):

- NAND controller, including loopback to SATA/PCIe interface.
- NAND flash.
- DDR memory.
- PIC device.
- Resistance and voltage measurements on voltage rails.

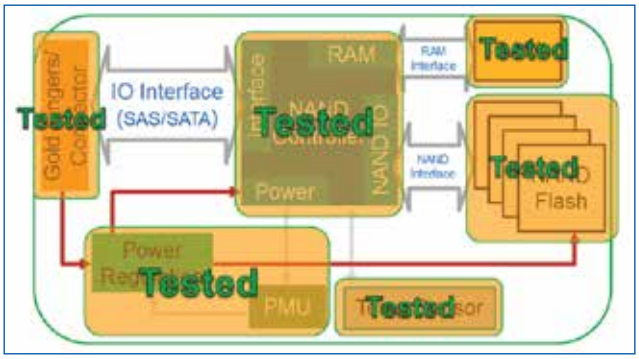

FIGURE 4. Test coverage offered by SSD manufacturing test solution.

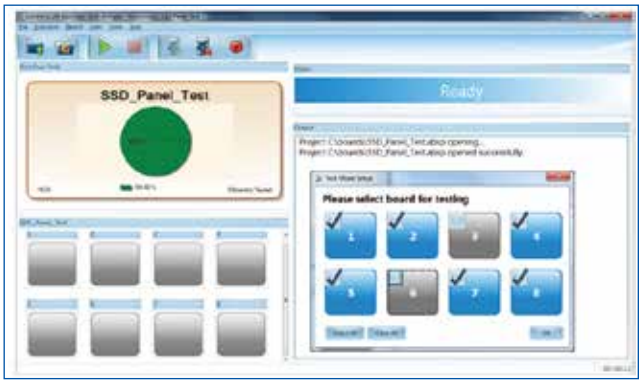

FIGURE 5. Production SSD test interface.

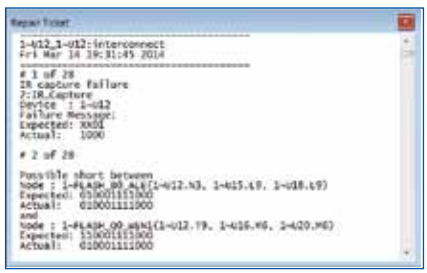

FIGURE 6. Failure ticket showing easy-to-read failure messages for operators.

SSD manufacturing test software. Software for test development in this test solution automatically integrates the following capabilities:

- Generation of the boundary scan test using board CAD data, BSDL and non-boundary scan test libraries.
- Setting the programmable power supply voltage and controlling the power on and off.
- Generation of measurement system commands to measure resistance, voltage and frequency on board.
- Generation of fixture wiring information for the fixture vendor.
- Generation of the manufacturing test sequence (FIGURE 5), which includes data logging of board serial number, pass/fail information and failure details (FIGURE 6).

This new solution permits testing of SSDs with smaller form factors during volume manufacturing. By integrating available measurement and testing tools supported with the development and production software interfaces, quality SSD boards can be ensured. CA

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```
"BYPASS  (11111111, 10000100, 00000101, 10001000,
  00000001), " &
"SAMPLE (00000010, 10000010), " &
"INTEST   (00000011, 10000011), " &
"HIGHZ    (00000110, 10000110), " &  -- Bypass with out-
  puts high-z
"CLAMP   (00000111, 10000111), " &  -- Bypass with bs value
"RUNT     (00001001, 10001001), " &  -- Boundary run test
"READBN (00001010, 10001010), " &  -- Boundary read
  normal mode
"READBT  (00001011, 10001011), " &  -- Boundary read test
  mode
"CELLTST  (00001100, 10001100), " &  -- Boundary selftest
  normal mode
"TOPHIP   (00001101, 10001101), " &  -- Boundary toggle
  out test mode
"SCANCN (00001110, 10001110), " &  -- BCR scan normal
  mode
"SCANCT  (00001111, 10001111)  " ;  -- BCR scan test mode
```

The manually-written custom test makes use of various test modes:

- CELLTST – boundary scan self-test normal mode.
- SCANCT – Boundary cell register (BCR) scant test mode.
- READBT – Boundary read test mode.
- TOPHIP – Boundary toggle out test mode, and
- RUNT – Boundary run test, which is not supported by the automatic test program generation.

FIGURE 6 shows the TDI signal waveform, expected TDO and actual waveform. The waveform graphics also show the device information, which includes either the hexadecimal or binary instruction. The user will also be able to navigate to the scan IR capture and DR capture executed during the test.

With the advancement of boundary scan software that supports simplified ISL, it is easier for test engineers to write custom tests to further expand test coverage. This is especially useful when implementing manufacturing tests on PCBAs with limited access, such as by using BIST, or when high-speed tests are required to test memory devices such as DDRs connected to a boundary scan device. **CA**

NPL National Physical Laboratory

Solder Joint Separation

When joints look perfect but nonetheless are failing, check the plating adhesion.

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SOLDER JOINT SEPARATION or failure can happen for a variety of reasons, even when every aspect of the assembly process is working correctly. In **FIGURE 1** the connector pin has separated from the surface of the printed board after reflow. The solder paste has reflowed correctly, and there is evidence on the pad of the joint and how the solder had successfully wetted up and around the contact to form a continuous fillet before the pin detached. There are some small voids in the joint, but these are very common between flush-mounted surfaces.

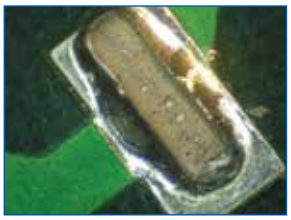

FIGURE 1. A separated connector pin post-reflow. The wetted solder suggests a plating adhesion issue.

If faced with this type of defect, take time to look at both surfaces – the PCB and connector pin – to understand and investigate the failure. In this case, there was plating separation from the connector pins. The solder paste reflow process was satisfactory, and solder wetted the plating and formed what looked like a perfect solder joint that would have passed any inspection or AOI. The plating adhesion to the base material was the problem, and just like pulling your foot out of a shoe, you are left with a perfect mold of the pin, but not a strong or reliable joint.

Conducting reflow simulations on the connector pins showed evidence of outgassing from the plating and complete dewetting on the surface of the pins. The point at which dewetting occurs may be time-dependent, and the time at reflow may not show the phenomenon. This should have been visible if solderability assessment had been conducted on the connectors. A wetting balance measurement can sometimes reveal dewetting not visible in practice.

These are typical defects shown in the National Physical Laboratory's interactive assembly and soldering defects database. The database (http://defectsdatabase.npl.co.uk), available to all this publication's readers, allows engineers to search and view countless defects and solutions, or to submit defects online. To complement the defect of the month, NPL features the "Defect Video of the Month," presented online by Bob Willis. This describes over 20 different failure modes, many with video examples of the defect occurring in real time. **CA**