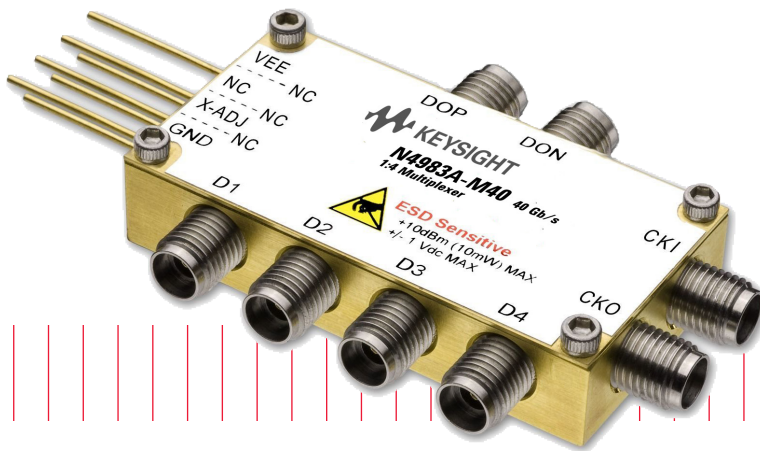


Keysight Technologies

N4983A Multiplexer and Demultiplexer

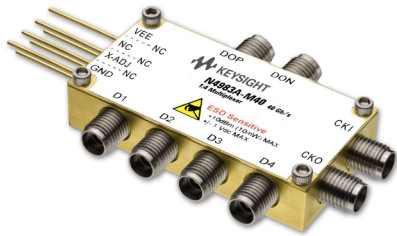
Data Sheet



N4983A-M40 44 Gb/s multiplexer

Features

- Wide operating range, 2 to 44 Gb/s
- Low output jitter
- Low power consumption
- Fast output rise/fall times
- High input sensitivity
- Half rate clock



Description

The N4983A-M40 is a broadband 4 to 1 multiplexer (MUX) with continuous coverage from 2 to 44 Gb/s. The four quarter-rate data inputs are single-ended and AC-coupled, while the full-rate data output is fully differential and DC-coupled. The MUX accepts a half-rate input clock and returns a quarter-rate output clock for driving other downstream circuits. A clock symmetry adjustment pin allows correction for data output duty cycle distortion. Power supply bias of negative 3.6 V is required.

Applications

The N4983A multiplexer 4:1, can be used with existing equipment to generate higher rate bit streams for use in telecom applications up to 44 Gb/s. Broadband test systems will benefit from the low power dissipation, precision connectors, and excellent output waveform characteristics. The compact size of the module allows the N4983A multiplexer 4:1, to be placed at the measurement plane, reducing or eliminating artifacts related to long cables.

Telecom and datacom applications

- 4:1 multiplexer and 1:4 demultiplexer
- Up to 44 Gb/s operation
- Broad bandwidth
- High input sensitivity
- Low power dissipation
- Precision connectors

Parameter	N4983A-M40	Units
Data input		
Bit Rate	0.5 to 11.0	Gb/s
Amplitude range	100 to 1000	mV p-p
Clock Input		
Type	Half-rate	
Frequency	1 to 22	GHz
Amplitude range	200 to 1400	mV p-p
Data Output¹		
Bit Rate	2 to 44	Gb/s
Amplitude (typical single-ended)	> 470	mV p-p
Jitter rms (typical)	< 0.9	ps
Rise/Fall time (typical 20-80%)	9	ps
Clock Output		
Type	Quarter-rate	
Frequency	0.5 to 11.0	GHz
Amplitude	> 400	mV p-p
DC Supply		
Voltage	-3.6	V
Current (nominal)	590	mA

1. Data output eye parameters (amplitude, jitter, rise/fall time) measured with Keysight 86100D Infiniium DCA-X Oscilloscope, with 86107A Precision Time Base and 86118A 70 GHz Remote Sampling Head modules.

Table 1

Absolute maximum rating

Parameter	Value
Supply voltage (VEE)	-4.0 V
Clock input power (CKI)	+10 dBm
Data input (D1, D2, D3, D4)	2 V p-p
DC input voltage to CKI, D1, D2, D3, D4	± 0.5 V
Operating temperature	0 to +70 deg C
Storage temperature	-50 to +125 dec C

Table 2

N4983A-M40 44 Gb/s multiplexer

Performance data

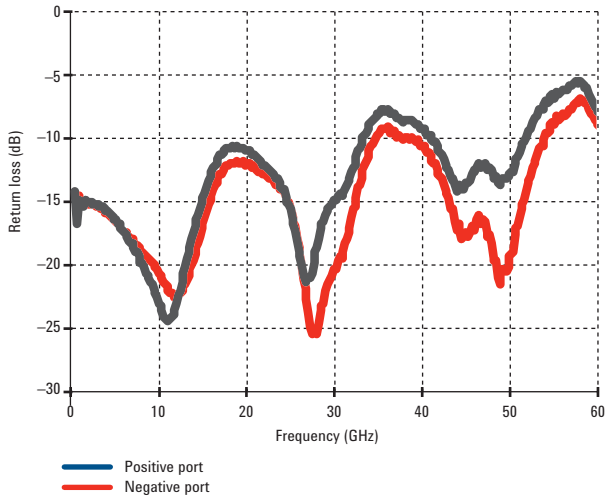


Figure 1. N4983A-M40 data output return loss

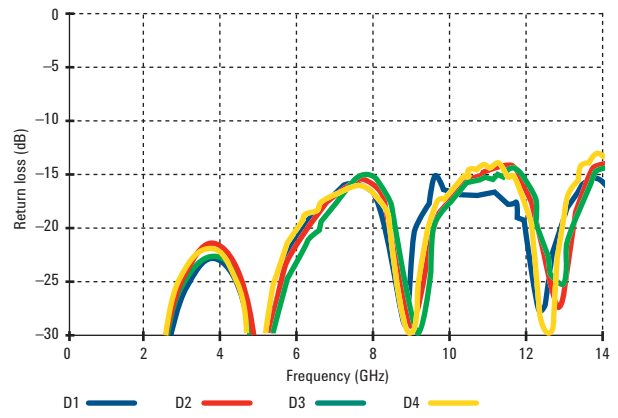


Figure 2. N4983A-M40 data input return loss

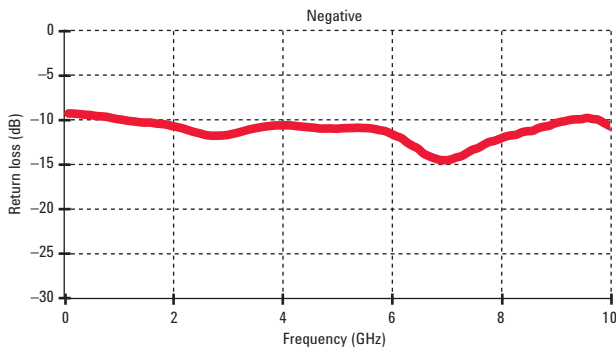


Figure 3. N4983A-M40 data input return loss

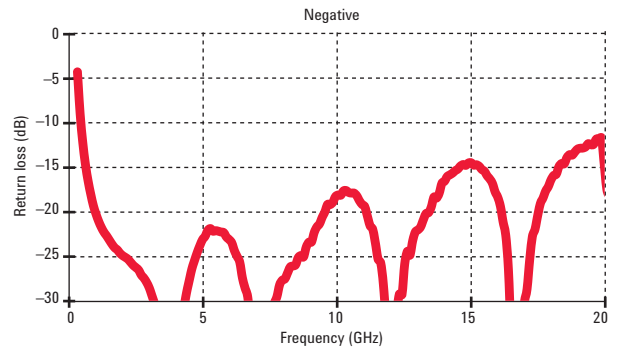


Figure 4. N4983A-M40 clock input return loss

N4983A-M40 44 Gb/s multiplexer

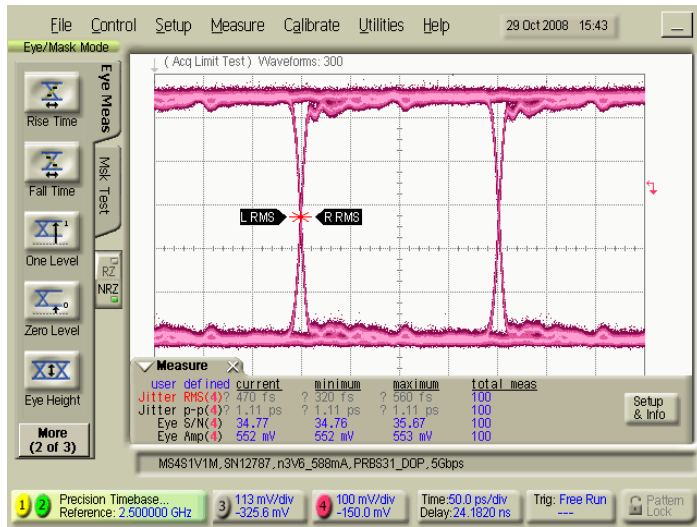


Figure 5. N4983A-M40 data output waveform @ 5 Gb/s. (4x 1.25 Gb/s, 2 e31-1 data inputs)

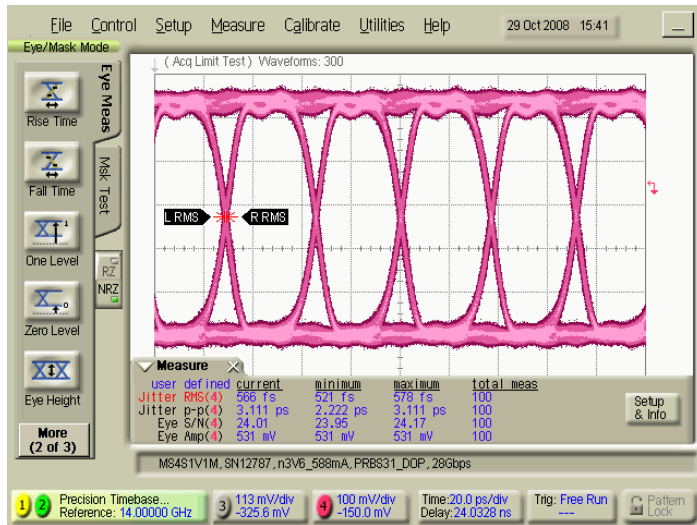


Figure 6. N4983A-M40 data output waveform @ 28 Gb/s. (4x 7 Gb/s, 2 e31-1 data inputs)

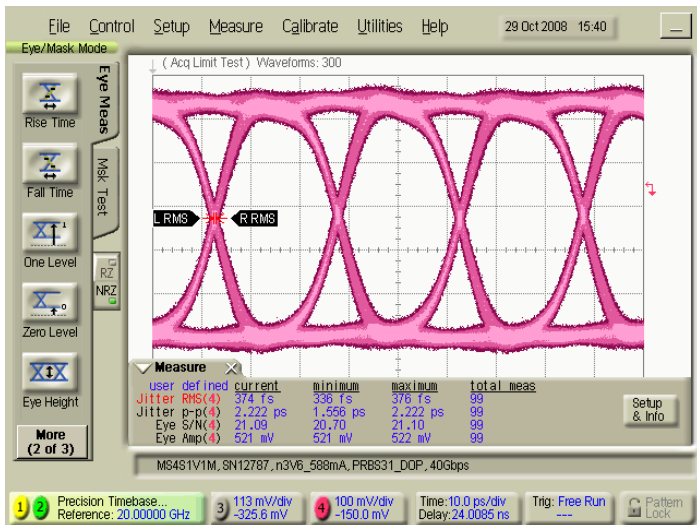


Figure 7. N4983A-M40 data output waveform @ 40 Gb/s. (4x 10 Gb/s, 2 e31-1 data inputs)

N4983A-M40 44 Gb/s multiplexer

Timing diagram

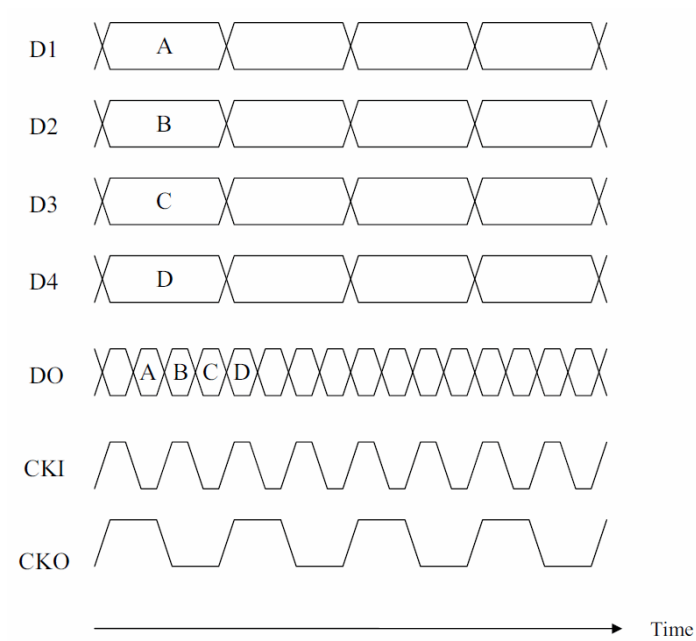


Figure 8. Timing diagram Note: Phase relationship between signals not implied.

Functional block diagram

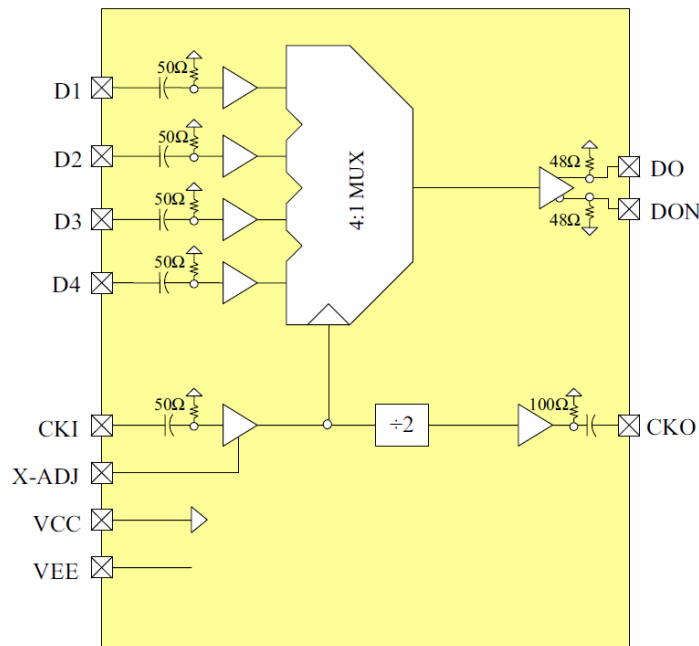


Figure 9. Functional block diagram

N4983A-M40 44 Gb/s multiplexer

Clock cross-over adjustment

The duty cycle of the input half-rate clock can have adverse effects on eye quality when deviating from 50%. Non-50% duty cycle is referred to as “duty cycle distortion” (DCD). DCD on the input clock will directly translate to double-tracking on the output eye, because adjacent bits would have unequal pulse-widths. DCD can happen by various means. For example, amplifiers operating in the non-linear regime when driven with large signals can often lead to un-evenly clipped waveforms and hence DCD. As another example, mismatches in differential circuits can cause voltage offsets between the differential signals thus leading to DCD. For these reasons, DCD can vary with frequency, temperature, and process variations.

The N4983A multiplexer 4:1 addresses the issue of clock DCD by providing an analog cross-over control for the input clock. This control pin allows the user to correct for a wide range of clock DCD. The cross over control is terminated internally with a 25 Ω load, and can accommodate a voltage range of ± 40 mV. An external attenuator or resistor in series is recommended to prevent from overdriving and damaging this sensitive input (see figure for example). Note that the cross-over range is limited to the rise/fall times of the input clock.

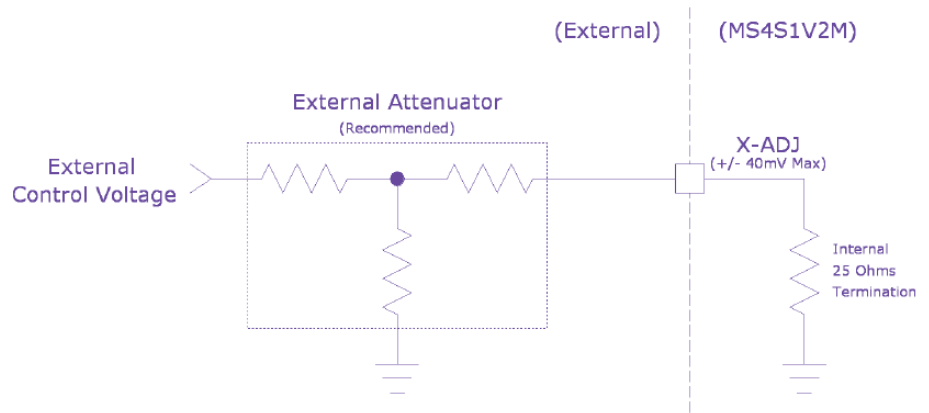


Figure 10. N4983A multiplexer clock cross-over adjust control

1) MUX clock
D.C. = 50%
X-ADJ = 0V

2) MUX clock
D.C. < 50%
X-ADJ < 0V

3) MUX clock
D.C. > 50%
X-ADJ > 0V

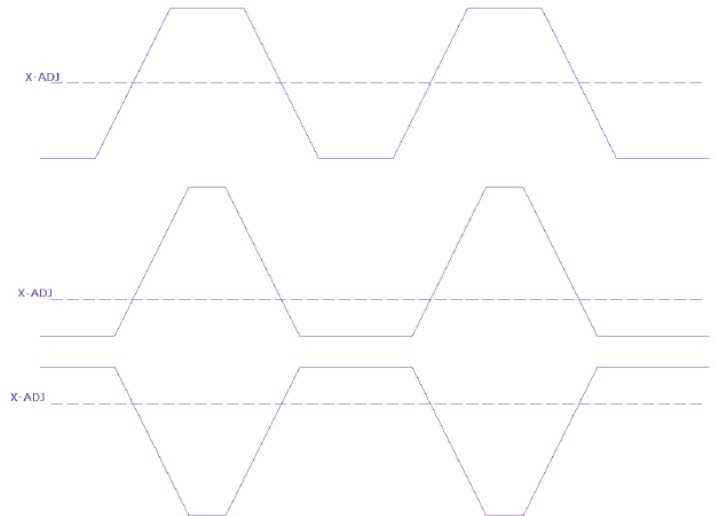


Figure 11. N4983A multiplexer clock duty cycle waveforms

Module outline

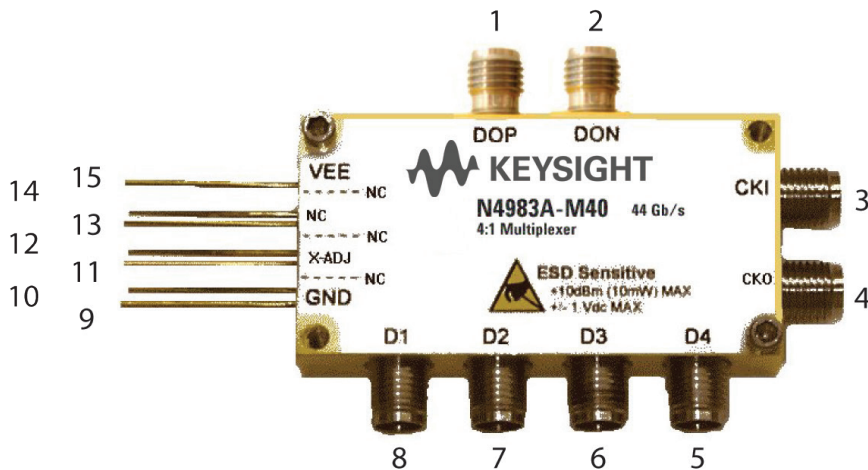


Figure 12. Outline

N4983A-M40 44 Gb/s multiplexer

Pin description (see Figure 11 below)

Name	Pin	Description	Note	Connector
DOP	1	Data channel output	Positive terminal of differential output	2.92 mm
DON	2	Data channel output	Negative terminal of differential output	2.92 mm
CKI	3	Clock input	1/2 of bit rate, e.g. 22 GHz for 44 Gb/s, Single-ended input	2.92 mm
CKO	4	Clock divided output	1/4 of bit rate, e.g. 11 GHz for 44 Gb/s, Single-ended output	2.92 mm
D4	5	Data channel input - bit position 4	Trailing/last serial data bit	2.92 mm
D3	6	Data channel input - bit position 3	-	2.92 mm
D2	7	Data channel input - bit position 2	-	2.92 mm
D1	8	Data channel input - bit position 1	Leading/first serial data bit	2.92 mm
VCC	9	RF & DC ground	Chassis/Module connection, 0 V	-
X-ADJ	11	Clock cross-over adjust	± 40 mV max, 25 Ω	-
VEE	15	Negative supply voltage	-3.6 V, DC	-
NC	10, 12 to 14	No connect	-	-

Table 3

Packaging information

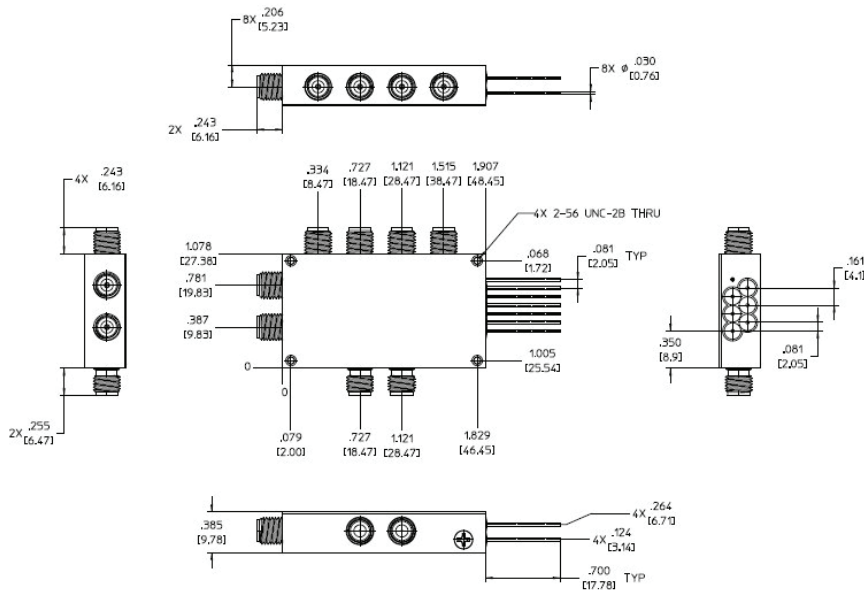


Figure 13. All measurements in inches [mm]

N4983A-D40 44 Gb/s demultiplexer

Features

- Wide operating range, 2 to 44 Gb/s
- Low output jitter
- Low power consumption
- Fast output rise/fall times
- High input sensitivity
- Half rate clock



Description

The N4983A-D40 is a broadband 1 to 4 demultiplexer (DEMUX) with continuous coverage from 2.6 to 44 Gb/s. Differential data inputs are DC coupled and terminated with 50 Ω resistors to minimize reflections. The DEMUX operates from a half rate single-ended, clock input. The module features single-ended AC coupled data outputs. Power supply of negative 3.6 V is required.

Applications

The N4983A demultiplexer 1:4, can be used in telecom applications operating at transmission speeds within the demultiplexer's 2.6 to 44 Gb/s input rate.

Broadband test systems will benefit from the low power dissipation, precision connectors, and excellent output waveform characteristics. The compact size of the module allows the N4983A demultiplexer to be placed at the measurement plane, reducing or eliminating artifacts related to long cables.

Parameter	N4983A-M40	Units
Data input		
Bit Rate	2.6 to 44.0	Gb/s
Amplitude range (single-ended)	150 to 1000	mV p-p
Clock Input		
Type	Half-rate	
Frequency	1.3 to 22	GHz
Amplitude range	200 to 1400	mV p-p
Data Output¹		
Bit Rate	0.65 to 11.0	Gb/s
Amplitude (typical single-ended)	> 230	mV p-p
Jitter rms (typical)	< 1	ps
Rise/Fall time (typical 20-80%)	12	ps
DC Supply		
Voltage	-3.6	V
Current (nominal)	300	mA

1. Data output eye parameters (amplitude, jitter, rise/fall time) measured with Keysight 86100D Infiniium DCA-X Oscilloscope, with 86107A Precision Time Base and 86118A 70 GHz Remote Sampling Head modules.

Table 4

Absolute maximum rating

Parameter	Value
Supply voltage (VEE)	-4.0 V
Data input (DI, DIN)	2.0 Vpp
Clock input power (CKI)	+10 dBm
DC input voltage to CKI, DI, DIN	± 0.5 V
Operating temperature	0 to +70 °C
Storage temperature	-50 to +125 °C

Table 5

N4983A-D40 44 Gb/s demultiplexer

Performance data

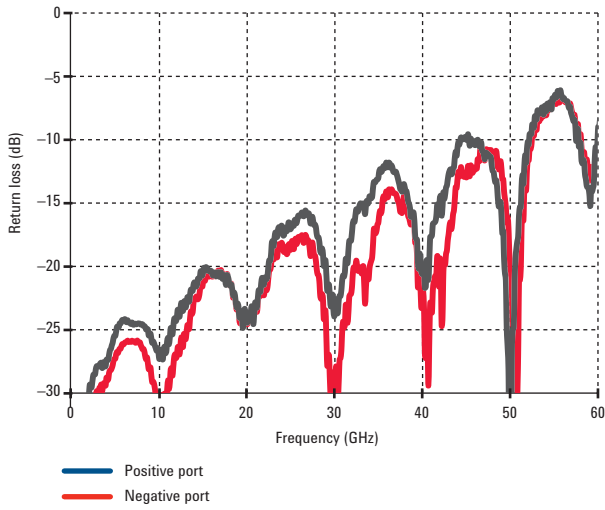


Figure 14. N4983A-D40 data input return loss

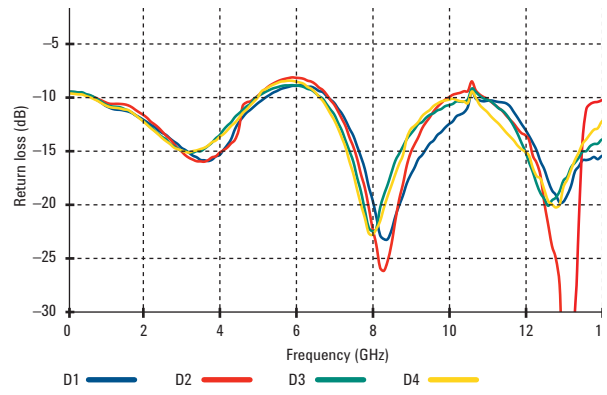


Figure 15. N4983A-D40 data output return loss

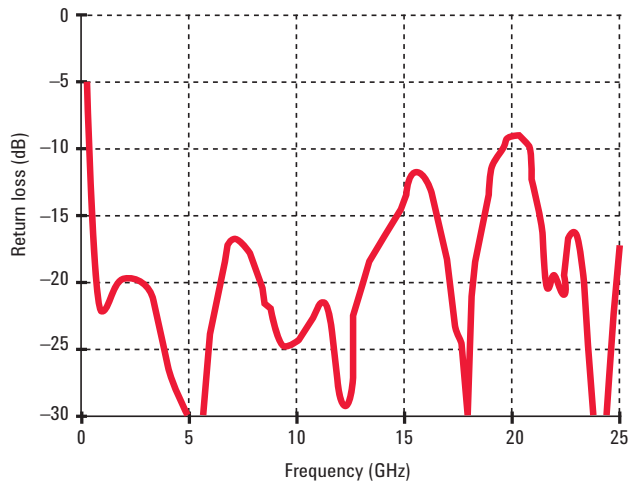
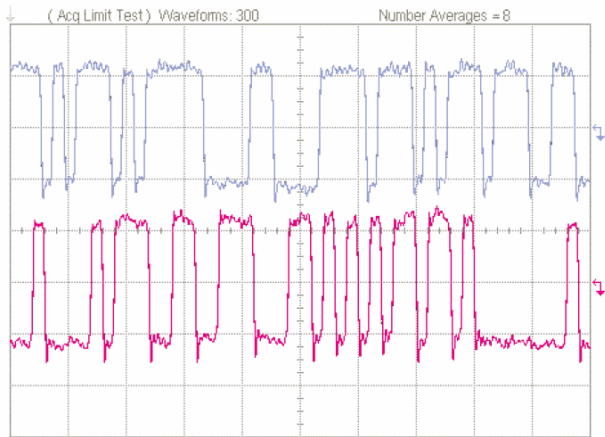


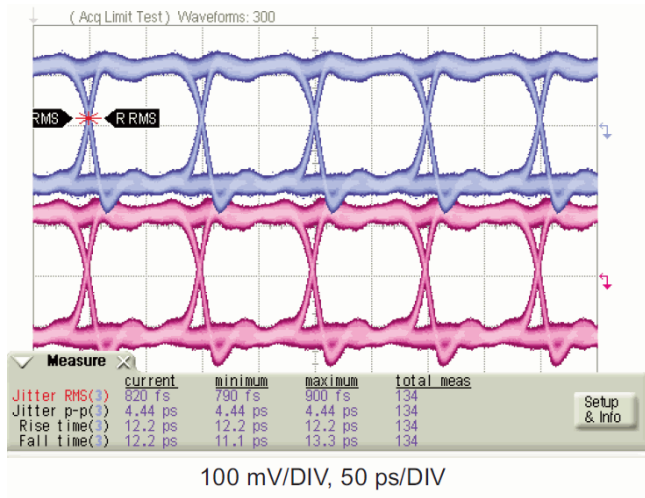
Figure 16. N4983A-D40 clock input return loss

N4983A-D40 44 Gb/s demultiplexer



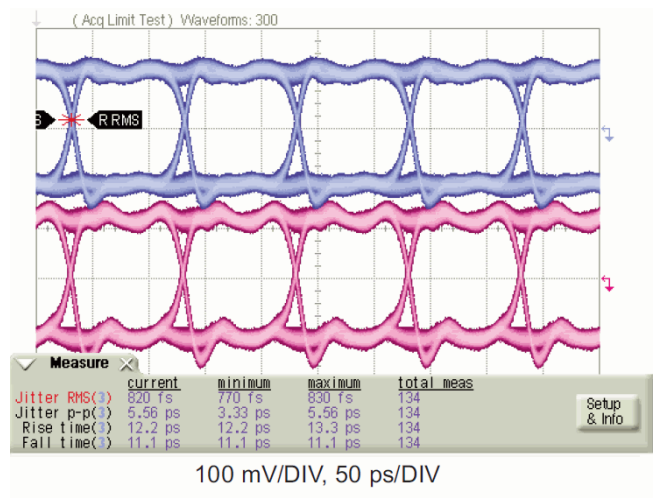
100 mV/DIV, 500 ps/DIV

Figure 17. N4983A-D40 data output waveforms @ 10 Gb/s (40 Gb/s data input)
Top: D3, Bottom: D4



100 mV/DIV, 50 ps/DIV

Figure 18. N4983A-D40 Data output eye diagrams @ 10 Gb/s (40 Gb/s data input).
Top: D1, Bottom: D2



100 mV/DIV, 50 ps/DIV

Figure 19. N4983A-D40 data output eye diagrams @ 10 Gb/s (40 Gb/s data input).
Top: D3, Bottom: D4

N4983A-D40 44 Gb/s demultiplexer

Timing diagram

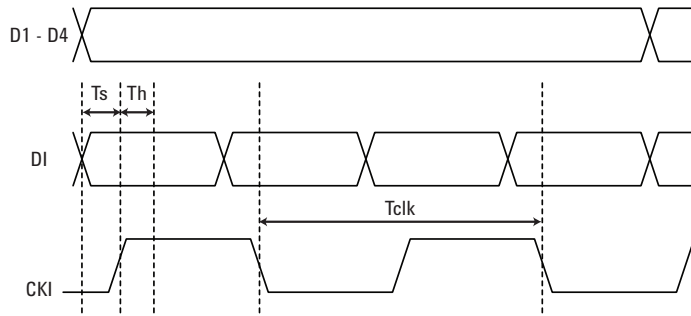


Figure 20. Timing diagram

Parameters	State	Min	Typ	Max
Ts (ps)	Setup time	4	-	-
Th (ps)	Hold time	4	-	-

Table 6

Functional block diagram

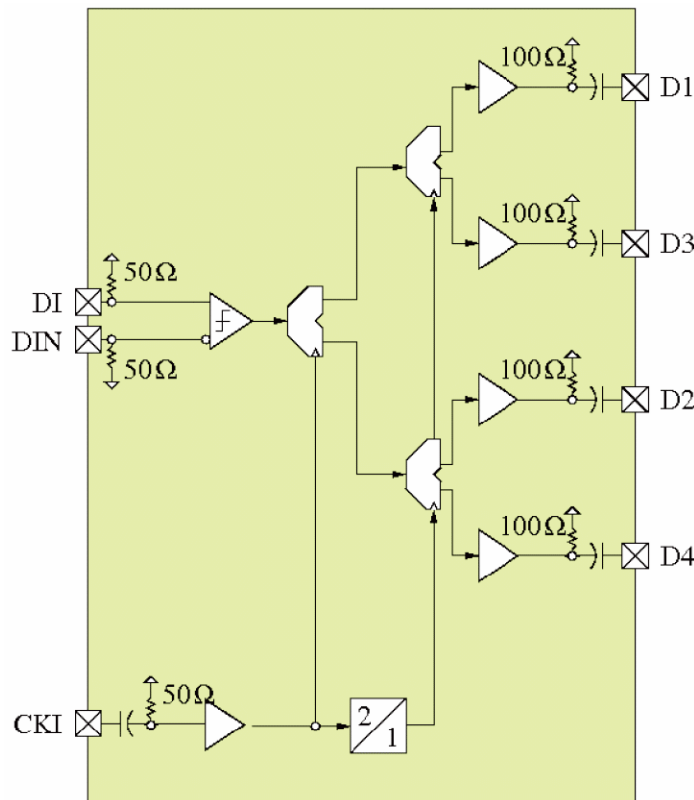


Figure 21. Block diagram

N4983A-D40 44 Gb/s demultiplexer

Module outline

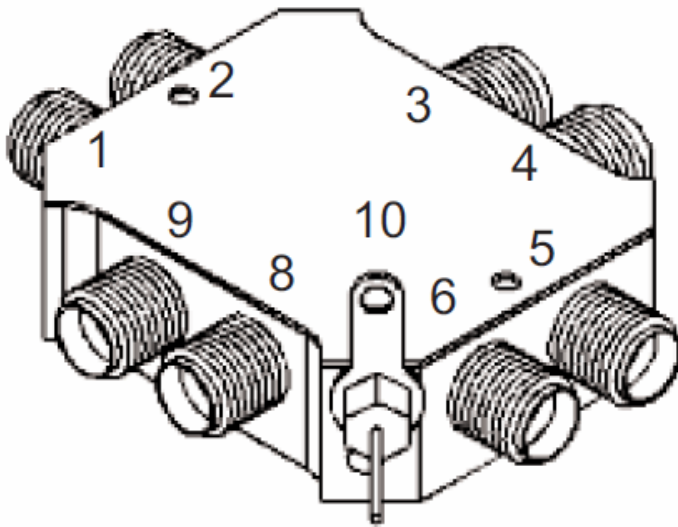


Figure 11. Module outline

Pin description

Name	Pin	Description	Note	Connector
D1	1	Data channel output - bit position 1	Leading/first serial data bit	2.92 mm
D3	2	Data channel output - bit position 3	Third bit	2.92 mm
DI	3	Data channel input	Positive terminal of differential input	2.92 mm
DIN	4	Data channel input	Negative terminal of differential input	2.92 mm
D4	5	Data channel output - bit position 4	Trailing/Last bit0	2.92 mm
D2	6	Data channel output - bit position 2	Second bit	2.92 mm
VEE	7	Negative supply voltage	DC pin, -3.6V	-
CKI	8	Clock input	1/2 of bit rate, e.g.: 20 GHz for 40 Gb/s full stop after 40 Gb/s. Single-ended input	2.92 mm
VCC	9	RF & DC ground	Chassis/Module connection, 0 V.	-
NC	11	No connect	-	-

Table 7

N4983A-D40 44 Gb/s demultiplexer

Packaging information

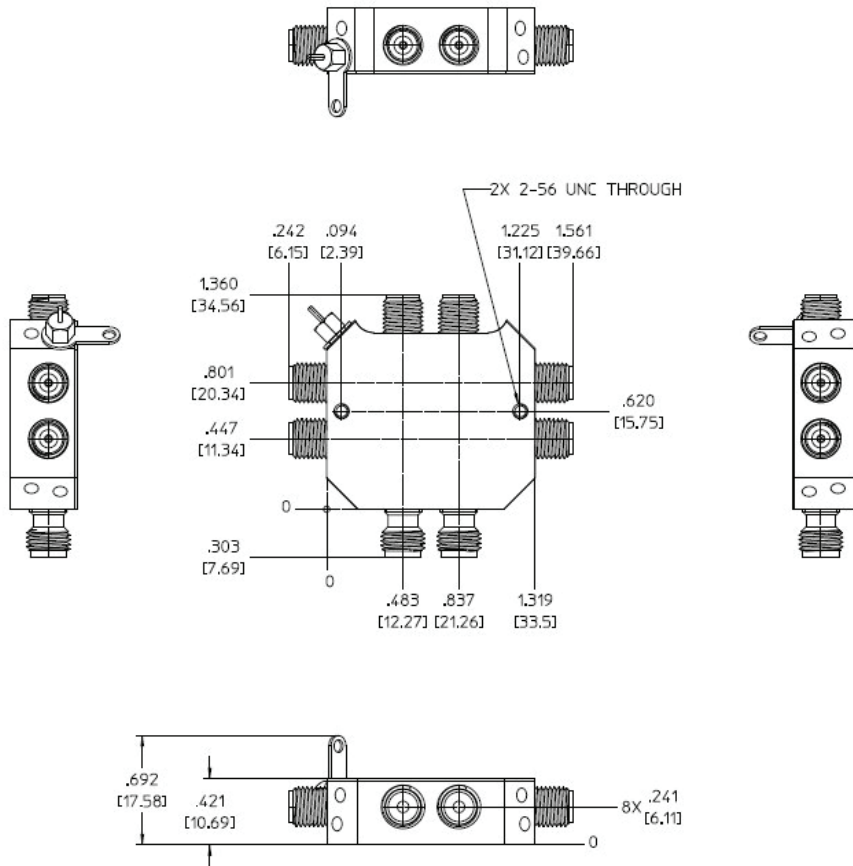


Figure 23. All measurements in inches [mm]

Ordering Information

- N4983A multiplexer and demultiplexer
- N4983A-M40 44 Gb/s 4:1 multiplexer
- N4983A-M56 56 Gb/s 4:1 multiplexer
- N4983A-D40 44 Gb/s 1:4 demultiplexer
- N4983A-D56 56 Gb/s 1:4 demultiplexer

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