M8085A MIPI® D-PHY Receiver Test Software

Calibration, Conformance, and Characterization Procedures

KEYSIGHT

USER GUIDE

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Keysight Technologies Deutschland GmbH
Herrenberger Strasse 130,
71034 Böblingen, Germany

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KEYSIGHT TECHNOLOGIES

MIPI D-PHY Receiver Tests with the M8070B Software supports the MIPI D-PHY signal generator configurations for single and multi-lane testing.

The following figure shows M8085A MIPI D-PHY Receiver Test setup with clock and data from a separate module:

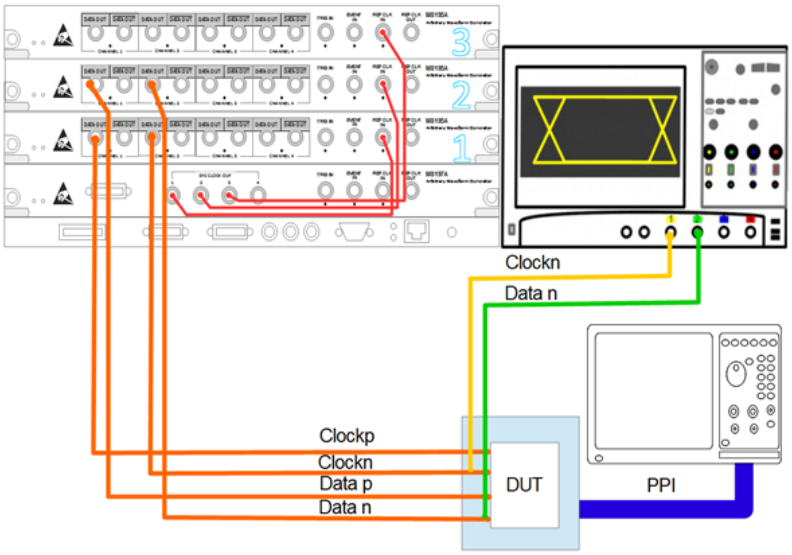


Figure 1 M8085A MIPI D-PHY Receiver Test Setup

The following figure shows M8085A MIPI D-PHY Receiver Test setup showing single lane with clock and data combined from one module:

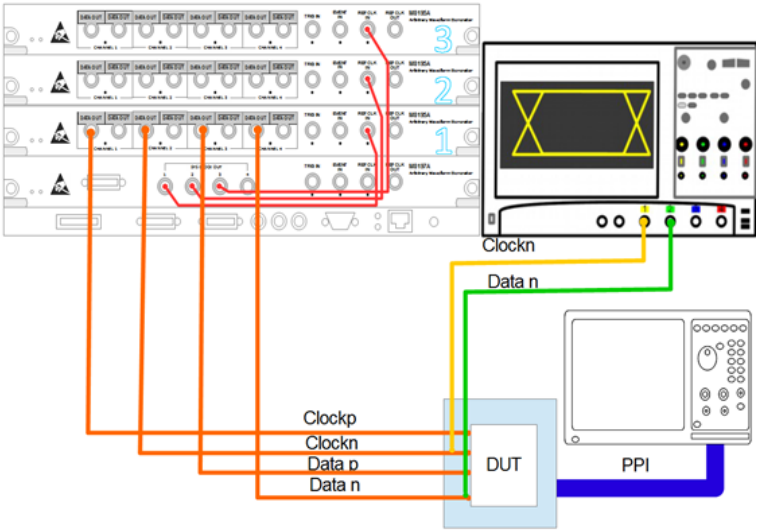


Figure 2 M8085A MIPI D-PHY Receiver Test Setup

Basic Requirements

Hardware Setup using M8195A AWG Module

Single-lane Setup

The required hardware setup for single-lane using M8195A module are following:

- One M8195A module
- An Embedded Controller (such as M9537A) or an external PC
- M9502A AXIe 2-Slot Chassis
- An Infiniium or SCPI compatible oscilloscope
- LAN or GPIB adapter

For hardware setup of a single lane (either Dual Channel or Four Channel mode):

1 Insert an M8195A and an Embedded Controller in the 2 slot frame AXIe chassis as shown in Figure 3.

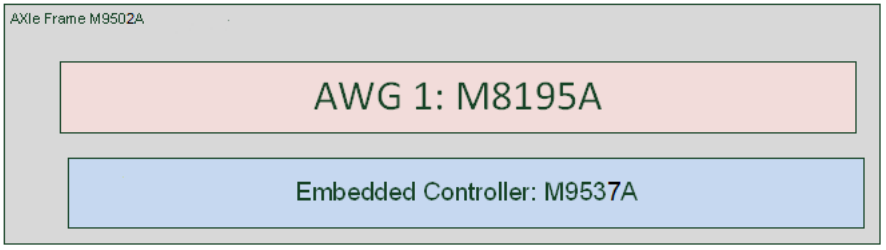


Figure 3 Hardware setup for Single-lane with module M8195A

2 M9502A contains only two slots. The Embedded Controller must be installed in the slot 1 of the AXIe chassis otherwise, it will not be able to connect to the internal PCIe interface of the frame.

3 The slot 2 contains the M8195A AWG module.

Multi-lane Setup

Following hardware setup is required for multi-lane:

- Two or three M8195A AWG modules to enable the multi-lane support (two data lanes in Dual Channel mode and up to four data lanes in Four Channel mode)
- One M8197A module to synchronize multi M8195A modules

- M9505A AXIe 5-Slot Chassis
  - for two lane structure - 2 slots for two M8195A modules, 1 slot for one M8197A module and 1 slot for embedded controller (optional)
  - for three lane structure - 3 slots for three M8195A modules, 1 slot for one M8197A module and 1 slot for embedded controller (optional)

NOTE **M8197A module is used to synchronize M8195A modules (Lane 1, Lane 2, Lane 3 and Lane 4). However, if you are using only single M8195A module (Lane 1), then M8197A is not required.**

Consider Figure 4 to achieve up to three lane hardware setup:

1 Put three M8195A and one M8197A in the 5 slot frame AXIe chassis.

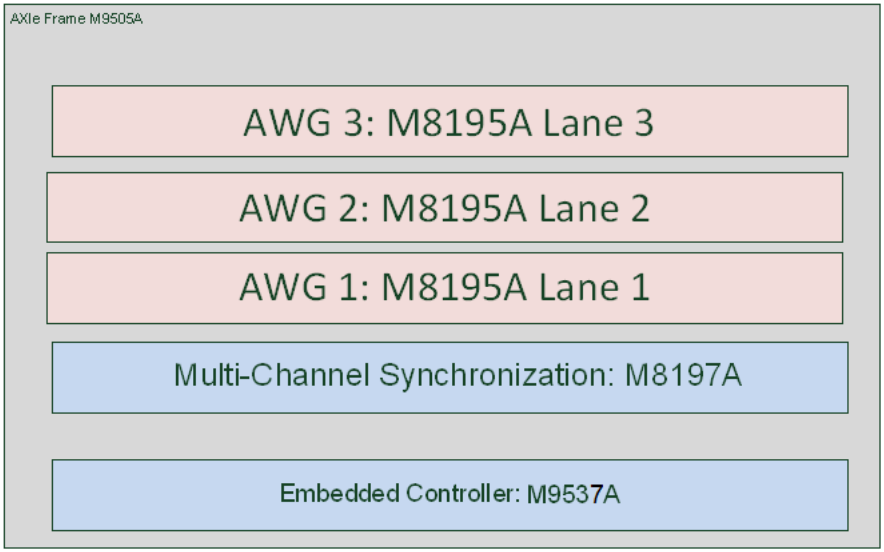


Figure 4 Hardware setup with two or three lane M8195A

2 The modules should be arranged inside a 5 slot chassis in the following order:
   - Slot 1: M8197A (Used for synchronization)
   - Slot 2: M8195A (Used for lane 1)
   - Slot 3: M8195A (Used for lane 2)

- Slot 4: M8195A (Used for lane 3)

NOTE You can also use an embedded controller for M8070B and/or the AWG SFPs or a remote PC as an external controller. The modules for multi-lane M8195A is also de-skewed itself.

Software Requirements

To install the MIPI D-PHY CTS plug-in, the M8070B software (version S6.0.100.2 or later) is required. You can download the software from the following link:

http://www.keysight.com/find/M8070B

License Requirements

The MIPI D-PHY CTS plug-in is a licensed feature. To enable it, Table 1 shows the required licenses:

Table 1 License required for MIPI D-PHY CTS plug-in

P/N	License	Description
M8085DE1A	-1TP	MIPI D-PHY 2.1 Editor for M819xA AWG, Transportable, Perpetual License
	-1NP	MIPI D-PHY 2.1 Editor for M819xA AWG, Network/Floating, Perpetual License
	-TRL	MIPI D-PHY 2.1 Editor for M819xA AWG, 30 Day Trial License
M8085DC1A	-1TP	MIPI D-PHY 2.1 Calibration, Conformance and Characterization Procedures for M819xA AWG, Transportable, Perpetual License
	-1NP	MIPI D-PHY 2.1 Calibration, Conformance and Characterization Procedures for M819xA AWG, Network/Floating, Perpetual License
	-TRL	MIPI D-PHY 2.1 Calibration, Conformance and Characterization Procedures for M819xA AWG, 30 Day Trial License

P/N	License	Description
M8085DUEA	-1TP	Upgrade MIPI D-PHY Editor from M8085A-DT1 to D-PHY 2.1, Transportable, Perpetual License
	-1NP	Upgrade MIPI D-PHY Editor from M8085A-DN1 to D-PHY 2.1, Network/Floating, Perpetual License
M8085DUCA	-1TP	Upgrade MIPI D-PHY Editor plus Calibration, Conformance and Characterization Procedures from M8085A-DT1 and M8085A-DTA to D-PHY 2.1, Transportable, Perpetual License
	-1NP	Upgrade MIPI D-PHY Editor plus Calibration, Conformance and Characterization Procedures from M8085A-DN1 and M8085A-DNA to D-PHY 2.1, Network/Floating, Perpetual License
N5990A	-010	Test Sequencer

Installing Plug-in

The MIPI D-PHY CTS plug-in must be installed separately other than the M8070B system software.

Please make sure that the system should already have M8070B (version 6.0.100.2 or later) software installed on it.

M8195A SFP should be installed from V3.6.0.0 and M8197A SFP should be installed from V3.6.0.0.

The installer for the MIPI D-PHY CTS plug-in is available either on CD or you may download it from the from the following Keysight web-page: www.keysight.com/find/m8085a.

For details on how to install the MIPI D-PHY CTS plug-in, refer to the *Keysight M8085A Plugins for MIPI Receiver Test Solutions Installation Guide*.

Currently, the shortcut for Keysight M8085A plug-ins is not auto-generated during installation.

To manually create a shortcut to the Keysight M8070B software on your desktop to access the M8085A plug-ins, perform the following steps:

1 Navigate to *C:\Program Files\Keysight\M8070B\bin* folder on your machine.

2 Right-click *Keysight.M8070B.exe* and click **Create Shortcut**.

3 Click Yes on the 'Shortcut' prompt to place the shortcut on the desktop.

4 On the desktop, right-click *Keysight.M8070B – Shortcut* icon and click **Properties**.

5 In the **Properties** window, modify the 'Target' location to *"C:\Program Files\Keysight\M8070B\bin\Keysight.M8070B.exe" /IgnoreAwg*.

6 Click **Apply** and exit the **Properties** window.

You may launch the *Keysight.M8070B – Shortcut* to access the M8085A plug-ins.

Related Documents

The plug-ins are installed separately from the plug-in manager.

For details on how to use the **Plug-in Manager** to install, uninstall and update the **M8085A** plug-in, refer to the *Installing M8085A Plugins for MIPI Receiver Test Solutions* section in *Keysight M8000 Series of BER Test Solutions Plugins for M8070B System Software Getting Started Guide*.

For M8070B plug-ins related documents, click **Start** > **Keysight M8070B** > **Keysight M8070B Documentation**.

Configuration Window

Once you start the software, the MIPI D-PHY Receiver Test Configuration window appears as shown in Figure 5:

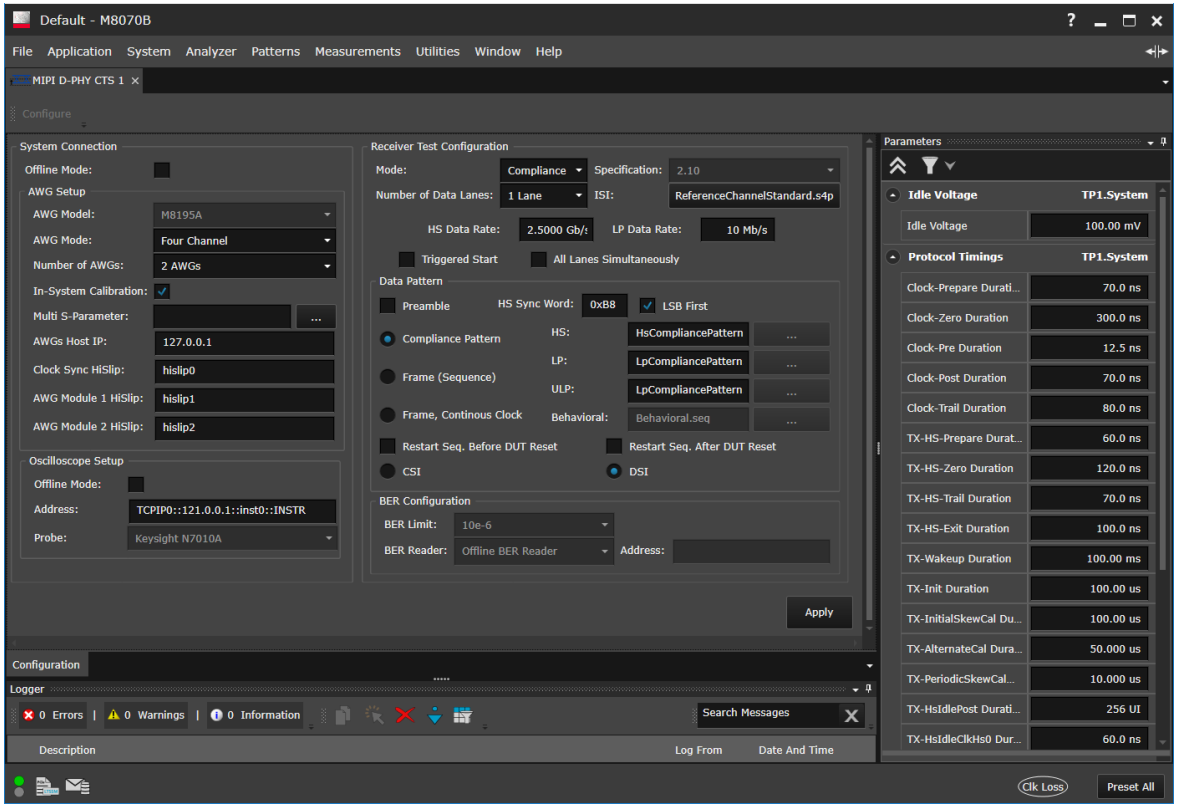


Figure 5 MIPI D-PHY CTS Configuration Window

The MIPI D-PHY Receiver Test user interface consists of the following GUI panels:

- Configuration
- Parameters
- Logger

Configuration

Configuration allows you to define the attributes for System Connection and for Receiver Test Configuration.

System Connection

This area includes the following attributes:

- Offline Mode: Select this check box to use the MIPI D-PHY Receiver Test software in an offline mode, i.e. without a proper physical connection to the DUT. In this mode, the application offers limited functionality and certain features are disabled.
- AWG Setup
  - AWG Model: The current version of M8085A software supports the M8195A AWG configuration only. The parameters for the connection setup of M8195A are described below:
    - M8195A Connection Setup: The M8195A AWG supports up to 4 Data lanes. The AWG Setup characteristics for M8195A are:
      - AWG Mode: It provides two options:
        - Four Channel - The four channel option uses all four channels of the AWG to generate data.
        - Dual Channel - The dual channel option uses two channels of the AWG to generate data.
      - Number of AWGs: Select the number of AWGs from the drop-down list. You can select up to three M8195A AWGs.
      - In-System Calibration: If set to 'On', this parameter enables the In-System AWG Calibration data for de-embedding. While the process of a normal de-embedding achieves de-embedding of the output amplifier only, using In-System Calibration achieves de-embedding of cables and probes as well (that is, the entire signal path), if applied. For more information regarding how to perform In-System AWG Calibration, see "Performing In-System AWG Calibration with Keysight IQ Tools" on page 35.
      - Multi S-Parameter: Define the s-parameter files to be de-embedded from the calculated waveform. To select one or more S-Parameter files, click this field and navigate to *C:\ProgramData\BitifEye\ValiFrame\SParameter\DPhy*. Select the required files and click Open. The selected file locations appear on the field and the de-embedding attributes are loaded.
      - AWGs Host IP: Provide the IP address of the AWG.

- Clock Sync HiSlip: Provide the HiSlip address of the Clock Sync module.
- AWG Module (1/2/3) HiSlip: Provide the HiSlip address of all the three connected AWGs in the respective fields.

- Oscilloscope Setup
  - Offline Mode: Select this check box to use the oscilloscope in offline mode, that is, without a live signal.
  - Address: Specify the VISA address of the connected oscilloscope.
  - Probe: The calibrations can be performed with the Keysight N7010A active termination adapter.

Receiver Test Configuration

It includes the following attributes:

- Mode: There are two modes:
  - Compliance Mode: The Compliance Mode strictly adheres to the tests and its parameter limits are defined in the MIPI D-PHY CTS. By default, the CTS limit values for the parameters used in the Calibration and Test procedures are defined within the application. The application does not allow you to modify values to the test parameters in Compliance Mode.

NOTE In the Compliance Mode, all tests are performed within the minimum and maximum values of the test parameters as defined in the MIPI D-PHY CTS specification.

  - Expert Mode: The Expert Mode allows you to customize the parameter limits, only if needed, to non-standard values, which can be helpful in debugging. By default, the CTS limit values for the parameters used in the Calibration and Test procedures are defined within the software. However, in Expert Mode, you may edit the parameter fields to indicate different values supported by your DUT.

NOTE In the Expert Mode, the plug-in allows you to change the parameter values within or beyond the maximum and minimum limits defined in the MIPI D-PHY CTS specification.

- Specification: This field displays version 2.10 only of the MIPI Alliance Specification for D-PHY, such that MIPI D-PHY Receiver Test software defines the corresponding values for parameters from this specification standard.
- Number of Data Lanes: The M8195A module has a multi-lane structure. The MIPI D-PHY Receiver Test software displays, by default, 1 Lane but gives you the option to select up to 4 Lanes from the drop-down options, depending on the Number of AWGs setting under System Connection.
- ISI: Specify the Inter Symbol Interference (ISI) S-Parameter file in the **.s4p* format.
- HS Data Rate: Specify a value for the high speed data rate for the signal. You can edit this field both in Compliance and Expert Modes.
- LP Data Rate: Specify a value for the low power data rate for the signal. You can edit this field both in Compliance and Expert Modes.

NOTE

Beginning with version 2.7 onwards, the M8085A MIPI D-PHY CTS plug-in supports a minimum **LP Data Rate** value of 1Mbps. However, using such lower data rate values can impact the pattern calculation time and memory usage. Therefore, the default **LP Data Rate** is set to 10 Mbps.

- Triggered Start: Select the check-box to trigger the LP-11 sequence in the signal. The MIPI D-PHY Receiver Test software performs this action for all tests except Test 2.2.2 where it triggers the LP-00 sequence.
- All Lanes Simultaneously: This check-box is applicable for multi-lanes. Select the check box to apply the test parameters on all data lanes simultaneously.

NOTE

By selecting the option All Lanes Simultaneously, you can save a lot of time if the test passes because all lanes are operating together simultaneously. However, if the test fails, you have to check each lane individually to find out the lane, where the error occurred.

Data Pattern

- Preamble: If HS Data Rate is set to 2.5 Gbps or higher, select this check box to insert a Preamble sequence in each burst of the generated HS data. The Preamble pattern consists of a 1010101010 pattern of $T_{PREAMBLE}$ duration (min. 32 UI to max. 512 UI) and is followed by an Extended Sync Pattern 11111111 (HS-1) in $T_{EXTSYNC}$ (of 8 UI).
- HS Sync Word: The value in this field indicates on the receiver side that the data transmission has started.
- LSB First: Select this check-box to transmit the LSB bit first in the Data Pattern.
- Compliance Pattern: Select this radio button to use the HS, LP and ULP compliance patterns defined in the CTS.
- Frame (Sequence): Select this radio button to define sequence files, in the **.seq* format, for HS, LP, ULP and Behavioral parameters. To select the sequence file for each parameter, click the corresponding ... button.
- Frame, Continuous Clock: Similar to “Frame (Sequence)”, but it enables continuous clock signal, even during the LP mode.
- Restart Seq. Before DUT: Select this check box to restart the sequences before the DUT transmission.
- Restart Seq. After DUT: Select this check box to restart the sequences after the DUT transmission.
- CSI: Select this option to verify conformance of the MIPI D-PHY sequences with the Camera Serial Interface (CSI) protocol. For more information on CSI Sequences, refer to “Sequence File Definition for CSI” on page 68.
- DSI: Select this option to verify conformance of the MIPI D-PHY sequences with the Display Serial Interface (DSI) protocol. For more information on DSI Sequences, refer to “Sequence File Definition for DSI” on page 77.

BER Configuration

For automated receiver testing, it is necessary to determine whether the DUT receives the data properly. This can be achieved by reading pass / fail information from the DUT. The Bit Error Ratio (BER) is measured and read. The MIPI D-PHY Receiver Tests Software supports two different BER Reader implementations.

- BER Limit: Select the BER limit for the tests.
- BER Reader: Following are the options available for the BER reader:

- Offline BER reader: This is the default option and does not require any address. Using the “Offline BER Reader” for each step of the test procedure, the MIPI D-PHY Receiver Tests Software shows pop-up dialogs requesting the user to reset and initialize the DUT and decides whether the DUT is working properly. This method is applicable to the DUT that allow a visual check, e.g. a Digital Serial Interface (DSI) device connected to a display. It is also possible to connect the DUT to the scope and verify if the output data is valid with help of the serial decoder. Using an offline BER reader will result in a semi-automated test as at each test point the user has to enter the pass / fail information.
- iBERreader: This option enables the custom BER reader. The usage of a “Custom BER Reader” enables fully automated testing for all transmission modes (HS and LP). This method requires the implementation of a class supporting the IBerReader interface by the user, providing access to the DUT’s pass/fail information. If required, refer to “IBerReader Interface Definition” on page 249 for details on integration method.
  - Address: Provide BER Reader address in this field, after selecting iBERreader.

Once the connections to the instrument are made successfully, click the **Apply** button.

Parameters Panel

The Parameters Panel allows you to change the Idle Voltage, Protocol timings supported by the DUT and the signal levels.

Figure 6 Parameters Panel

Idle Voltage

The parameter for Idle Voltage is shown in Figure 7 and described below.

Figure 7 Idle Voltage Parameter

Idle Voltage: The Idle voltage sets the offset on the AWG output amplifiers. This is the output offset voltage when the AWGs are in the Stop state.

Protocol Timings

The parameters provided by Protocol Timings are shown in the Figure 8 and described in Table 2 on page 28.

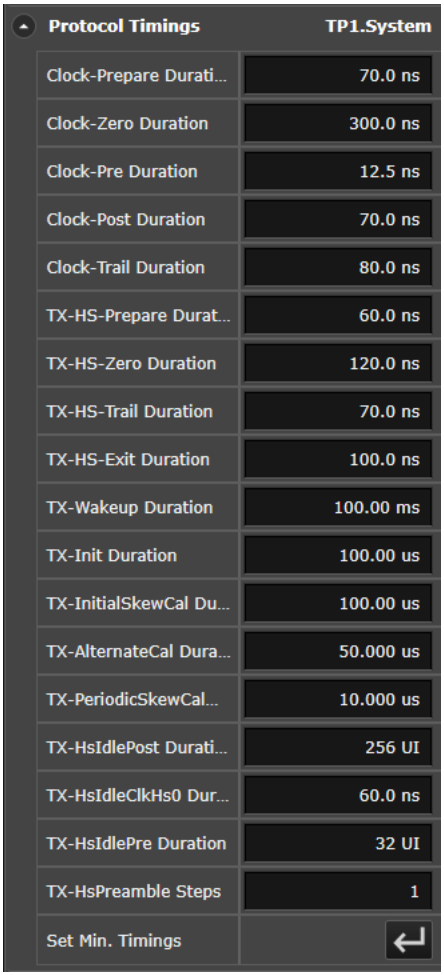


Figure 8 Parameters of Protocol Timings

Table 2 Parameters of Protocol Timings

Parameter	Description
Clock-Prepare Duration	Time taken by the high speed clock to drive bridge state (LP-00).
Clock-Zero Duration	Time taken in the HS-0 state while high speed driver is enabled and low power driver is disabled.
Clock-Pre Duration	Time (in UI) taken to drive the high speed clock in data rate before the startup of any data lane. UI are related to data channel's data rate (reciprocal relation) and has granularity of 2 as clock is of "two bits" granularity.
Clock-Post Duration	Time (in UI) taken to drive the high speed clock is driven in data rate after last data lane goes into low power mode. UI are related to data channel's data rate (reciprocal relation) and has granularity of 2 as clock is of "two bits" granularity.
Clock-Trail Duration	Time taken by the transmitter to drive HS-0 state after last payload clock bit of high speed transmission burst.
Clock-Miss Duration	Time taken by the receiver to detect the absence of clock transitions and disable the clock lane HS-RX..
TX-HS-Prepare Duration	Time taken by the transmitter to drive the data lane LP-00 state immediately before the HS-0-line state starting the HS transmission.
TX-HS-Zero Duration	Time taken by the transmitter to drive the HS-0 state until the TX-HS-Settle timer expires in order to neglect transition effects.
TX-HS-Trail Duration	Time taken by the transmitter to drive the Flipped Differential state after the burst of last payload data bit of high speed.
TX-HS-Exit Duration	Time taken by the transmitter to drive the LP-11 state following a HS burst.
TX-Wakeup Duration	Time taken by the transmitter to drive a Mark-1 state prior to a stop state in order to initiate an exit from ULPS.
TX-Init Duration	Time taken by the transmitter to drive a Stop state (LP_11).
TX-InitialSkewCal Duration	Time taken by the transmitter to drive the Skew Calibration pattern in the Initial Skew-Calibration mode.
TX-AlternateCal Duration	Set the duration when the transmitting signal drives the Alternate Calibration Pattern in the Alternate Calibration mode.
TX-PeriodicSkewCal Duration	Time taken by the transmitter to drive the Skew Calibration pattern in the Periodic Skew-Calibration mode.
TX-HsIdlePost Duration	Set the duration when the transmitting signal transitions from Data Burst to HS Idle state.
TX-HsIdleClkHs0 Duration	Set the duration when the transmitting signal drives in HS-Zero state on Clock lane.
TX-HsIdlePre Duration	Set the duration when the transmitting signal transitions from HS Idle state to next Data Burst state.
TX-HsPreamble Steps	Set the multiplier value for the required preamble steps to be inserted into the HS Burst. Each step is 32 UI in length. The parameter sets the multiplier value, which is multiplied by 32 UI, and the preamble sequence length is configured. The range for TPREAMBLE is from 32 UI (min.) to 512 UI (max.).
Set Min. Timings.	Set all the PHY timings to the minimum values based on the selected data rates.

Signal Levels

The parameters provided by Signal Levels are shown in the Figure 9 and described in Table 3 on page 29.

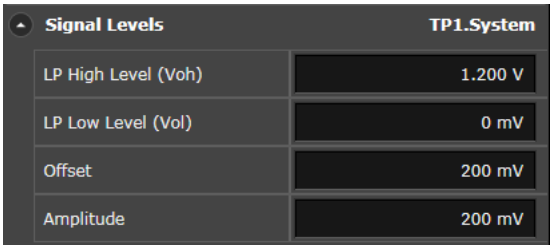


Figure 9 Parameters of Signal Levels

Table 3 Parameters of Signal Levels

Parameter	Description
LP High Level (Voh)	High Level voltage (Voh) at low power.
LP Low Level (Vol)	Low Level voltage (Vol) at low power.
Offset	▪ Sets Common High Speed Offset for both Dp and Dn, when Track Normal Line is “ON”. ▪ Sets Single Ended Offset for Dp and Dn, Track Normal Line is “OFF”.
Amplitude	▪ Sets Common High Speed Amplitude for both Dp and Dn, Track Normal Line is “ON”. ▪ Sets Single Ended Amplitude for Dp and Dn, Track Normal Line is “OFF”.

NOTE By default, the LP High Level Voltage parameter is set to 1.200 V, which corresponds to the Large Amplitude Mode. For Small Amplitude Mode, make sure that the LP High Level Voltage parameter is set to 750mV.

Logger Panel

The Logger Panel displays errors, warnings and information messages along with their respective descriptions, applications (from where they are generated) and their time stamps.

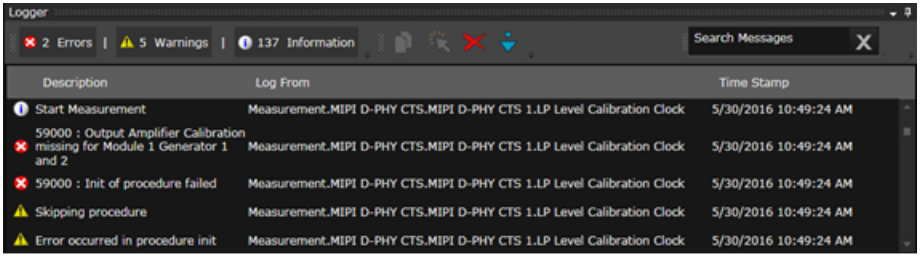


Figure 10 Logger Panel

Performing Procedures

After performing the configuration setup in the *Configuration Panel*; when you click **Apply**, the following test selection window is displayed.

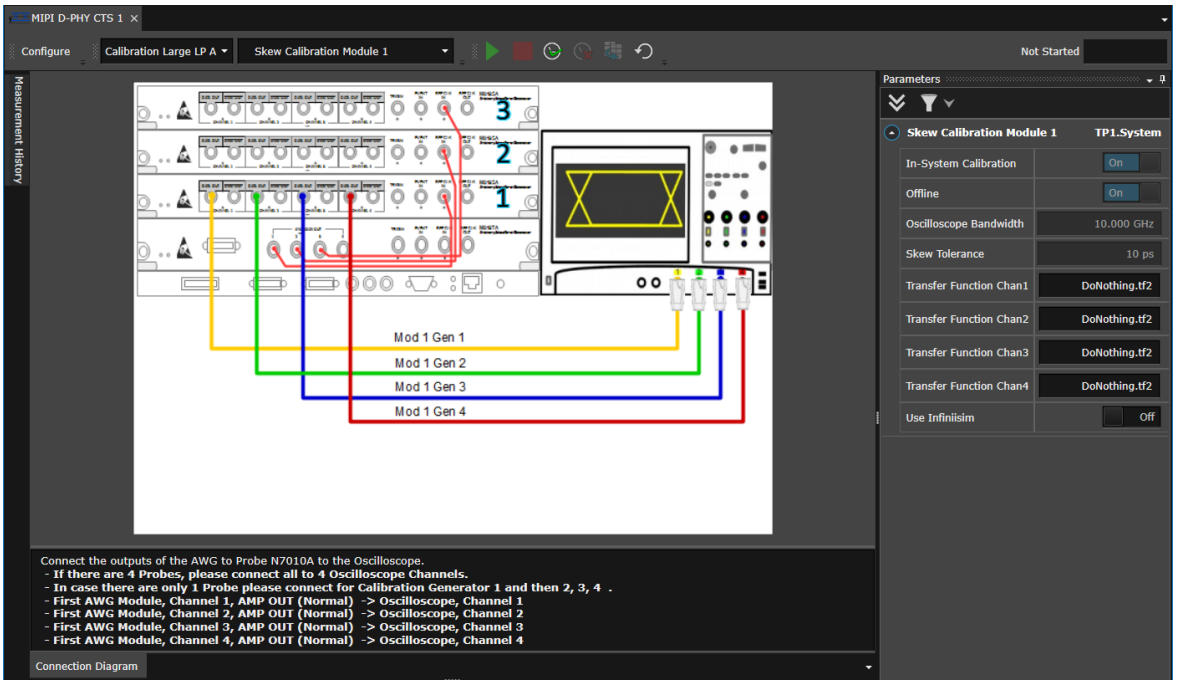


Figure 11 Performing the tests

This window allows you to select and perform the tests. For each selected procedure, it displays the connection diagram. It also provides you instructions to connect the output of the AWG to the Oscilloscope. Click the ▶ button to begin running tests. During the execution of all calibration and test procedures, the Status Indicator (Refer below for details on Status Indicator) displays the current state of a test. The results are displayed automatically in a data table and for some tests, graphical results are also available. Click the **Configure** button any time you wish to return to the Configuration Panel to re-configure the DUT and the test modes.

This window has the following options:

- Toolbar Buttons: The following table shows the available buttons on the toolbar:

Table 4 Toolbar Buttons

	Start /Continue Test	Starts a test.
	Stop Test	Stops the test.
	Step Into Test	Steps further into the test.
	Enable/Disable Test Run History	Enables or disables the test's run history.
	Clear Test History	Clears the test run history.
	Copy Test History Properties	Copies the test history properties to the currently running test.
	Reset	Resets the test to its default values.

- Measurement History: It maintains the history of executed tests along with their time stamp. It allows you to refer the previously run measurements and also compare their results.

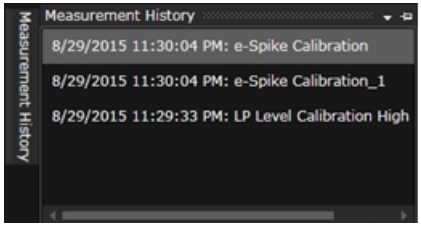


Figure 12 Measurement History

Click the  button present on the toolbar if you wish to toggle between the enable/disable measurement run history.

Click the button to copy the properties of run measurements on to the currently running measurement.

- Status Indicator: The status indicator shows the current state of a test. A test can have various states such as Not Started, Running, Stop, Error, Suspended and Finished.

  The following figure displays the status indicator while the test is running:

- Results (Tabular view): It shows results in tabular format for each procedure, i.e. measured values for calibrations and values for tests after they are complete.

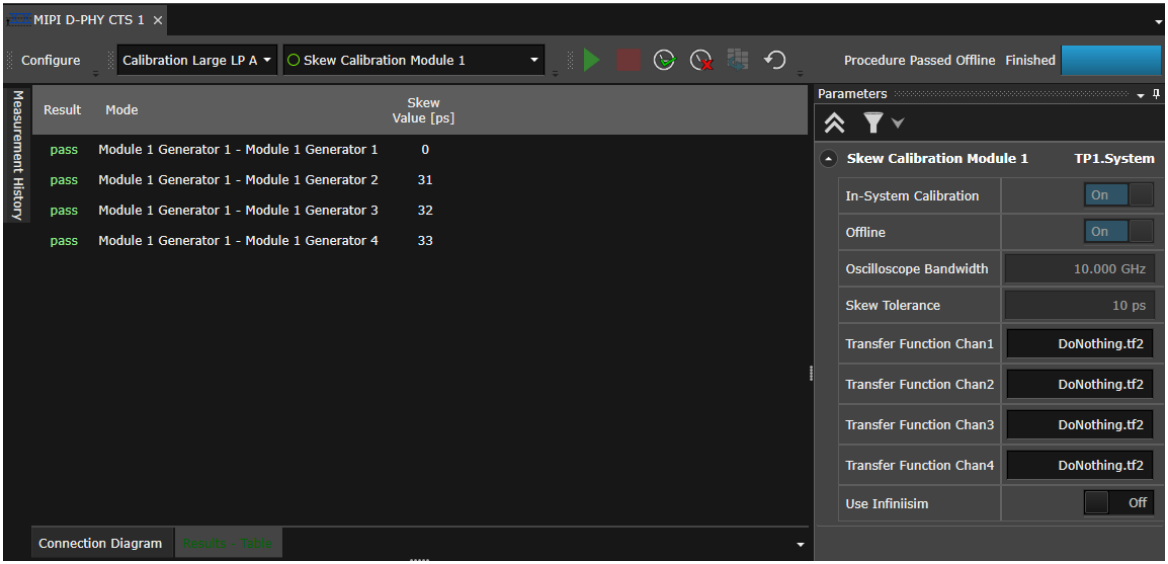


Figure 13 Tabular view for results

- Results (Graphical view): It shows the graphical results for some procedures, i.e. measured values for calibrations and tested values for the tests. For example, Figure 14 shows a sample graphical result for the respective Calibration performed.

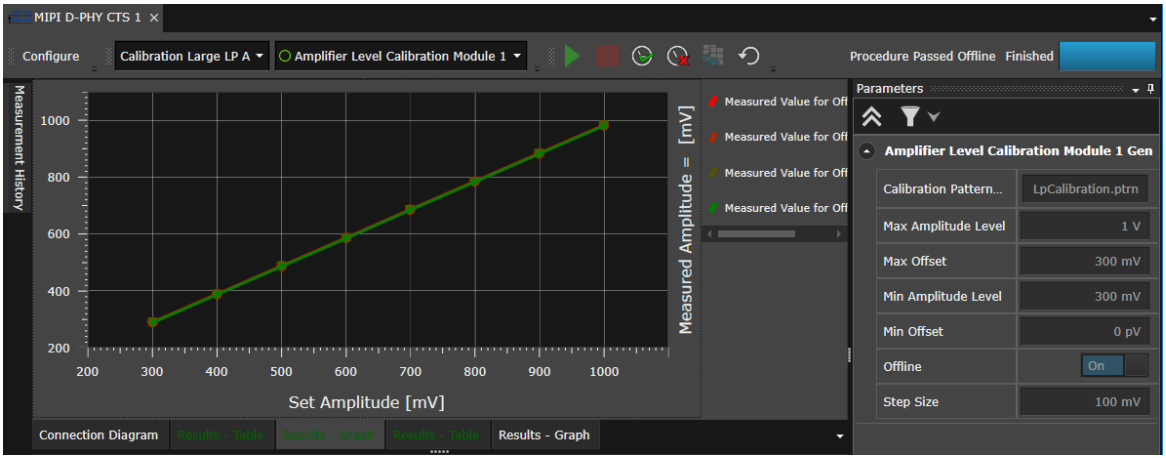


Figure 14 Graphical view for results

Performing In-System AWG Calibration with Keysight IQ Tools

To improve the quality of the MIPI D-PHY signal, you may enable the calibrated values obtained via the In-System Calibration of the connected AWGs. The In-System Calibration can be performed using the Keysight IQ Tools software, which you may download from www.keysight.com.

To perform In-System Calibration:

1 Launch the *Keysight IQ Tools* software.

2 In the **Configuration** area of the main window, click **Configure instrument connection**.

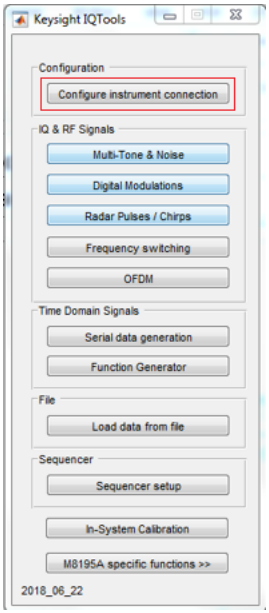


Figure 15 Main window of the IQ Tools software

3 In the **Arbitrary Waveform Generator Configuration** section of the **Instrument Configuration** window,

- For 4-Channel mode:
  - *a* Select **Instrument model** as *M8195A*
  - *b* Select **Mode** as *4 ch, deep mem, 16 GSa/s*
  - *c* Select **Connection** type as *visa*
  - *d* In the **VISA Address** field, type the address of the M8195A module

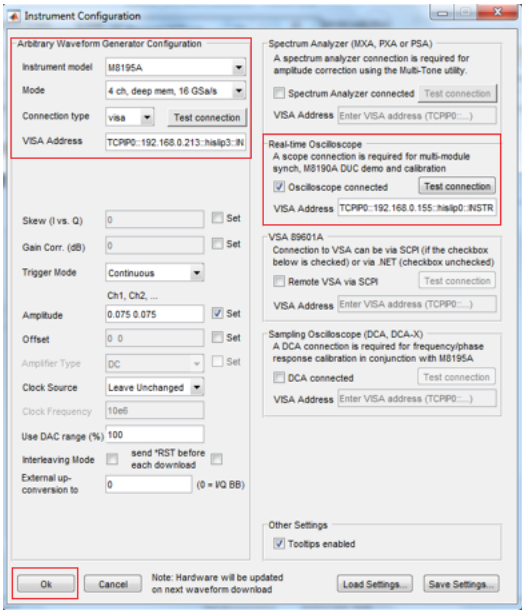


Figure 16 Settings on the Instrument Configuration window for 4-Channel

- For Dual Channel mode:
  - *a* Select **Instrument model** as *M8195A*
  - *b* Select **Mode** as *2 ch, deep mem, 32 GSa/s*
  - *c* Select **Connection** type as *visa*
  - *d* In the **VISA Address** field, type the address of the M8195A module

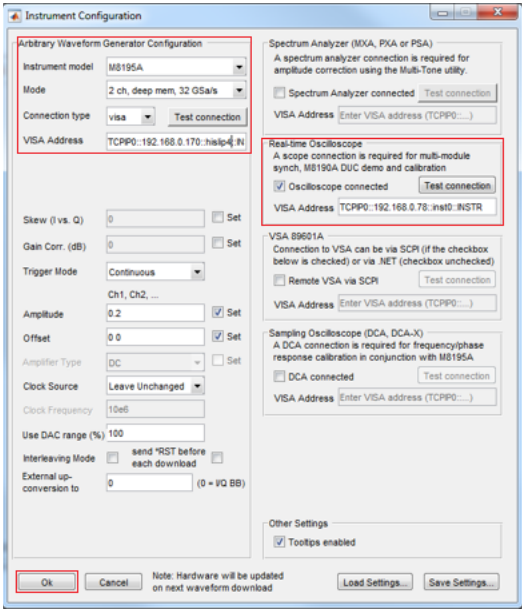


Figure 17 Settings on the Instrument Configuration window for Dual Channel

4 In the **Real-time Oscilloscope** section of the **Instrument Configuration** window,
   - *a* Select the **Oscilloscope connected** check box, if not checked already
   - *b* In the **VISA Address** field, type the address of the Oscilloscope.

5 Click **OK** on the Instrument Configuration window.

6 In the **Time Domain Signals** area of the main window, click **Serial data generation**.

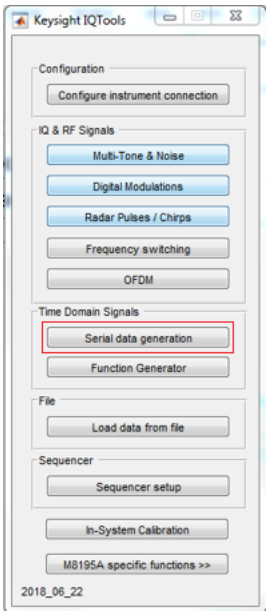


Figure 18 Accessing Serial data generation option

7 In the **Serial Data** window that appears, click **Show Correction**.

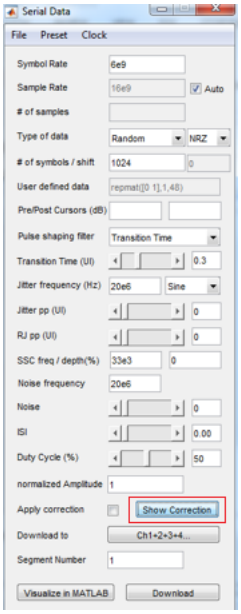


Figure 19 Accessing the Correction Management window

8 From the **Correction Management** window that appears, click **In-System Calibration**.

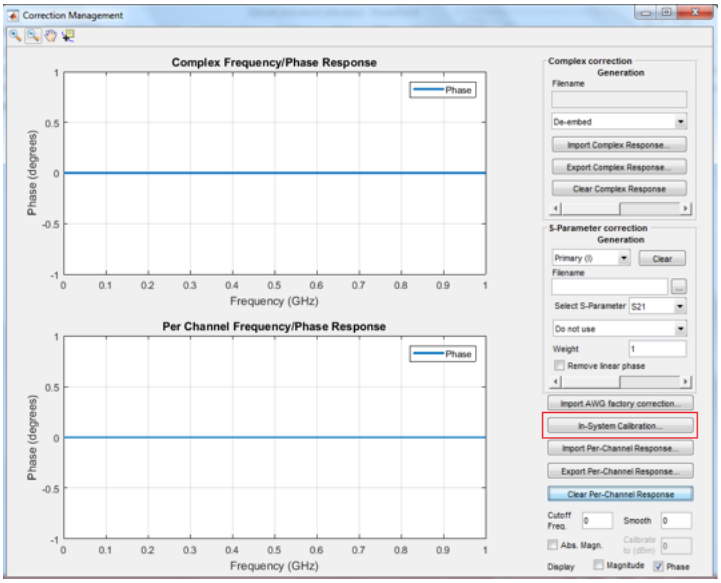


Figure 20 Selecting In-System Calibration option

9 On the **Frequency/Phase response calibration** window that appears,

- For 4-Channel mode

  a Ensure that the physical channels of the AWG and the Oscilloscope are connected as per the configuration shown in the **Channel Mapping** area (AWG Ch1 to Oscilloscope Ch1 and so on).

NOTE On the AWG complement outputs, ensure that terminations are connected.

b In the **Settings** area,

- **Sample Rate** value remains as-is
- If a Low-Pass Filter (LPF) is connected, the **Max. tone frequency** value should not exceed *8e9*

c Click **Run** to begin calibration measurements.

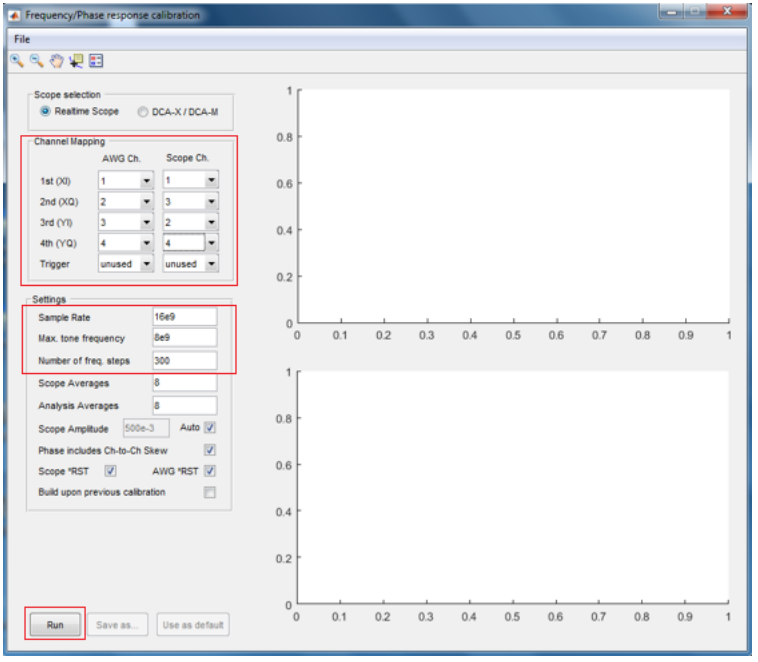


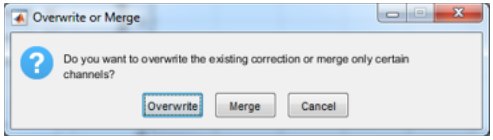
Figure 21 Validating settings to perform In-System Calibration

d If error messages are displayed,

- Validate the AWG-Oscilloscope Channel Mapping
- Reduce the Max. tone frequency value and try again

e If one or more outliers are found in the measurement, repeat the measurement a few more times.

f Once measurements are performed, overwrite the results.



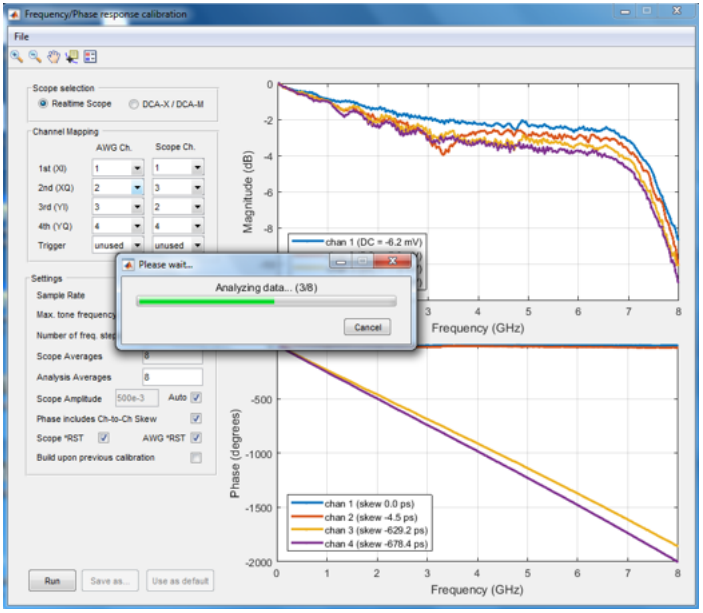


Figure 22 Viewing In-System Calibration results

- For Dual-Channel mode
  a Ensure that the physical channels of the AWG and the Oscilloscope are connected as per the configuration shown in the **Channel Mapping** area (AWG Ch1 to Oscilloscope Ch1 and so on).

NOTE On the AWG complement outputs, ensure that terminations are connected.

  b In the **Settings** area,
    - **Sample Rate** value remains as-is
    - No Low-Pass Filter (LPF) is connected, therefore, the **Max. tone frequency** value should be *16e9*
  c Click **Run** to begin calibration measurements.

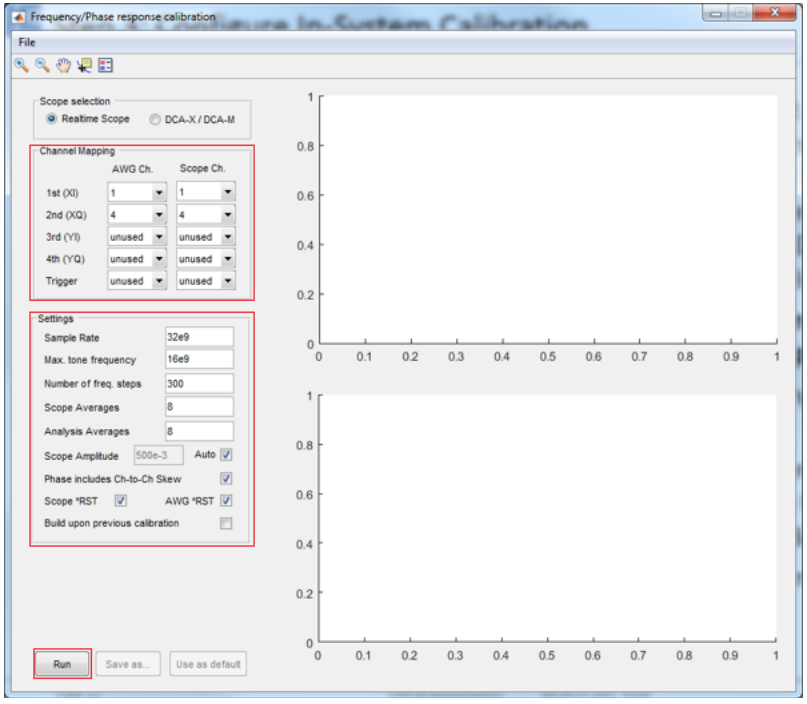


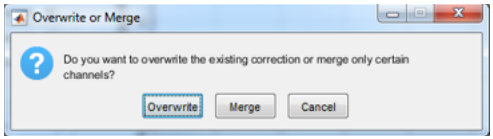
Figure 23 Validating settings to perform In-System Calibration

d If error messages are displayed,

- Validate the AWG-Oscilloscope Channel Mapping
- Reduce the Max. tone frequency value and try again

e If one or more outliers are found in the measurement, repeat the measurement a few more times.

f Once measurements are performed, overwrite the results.



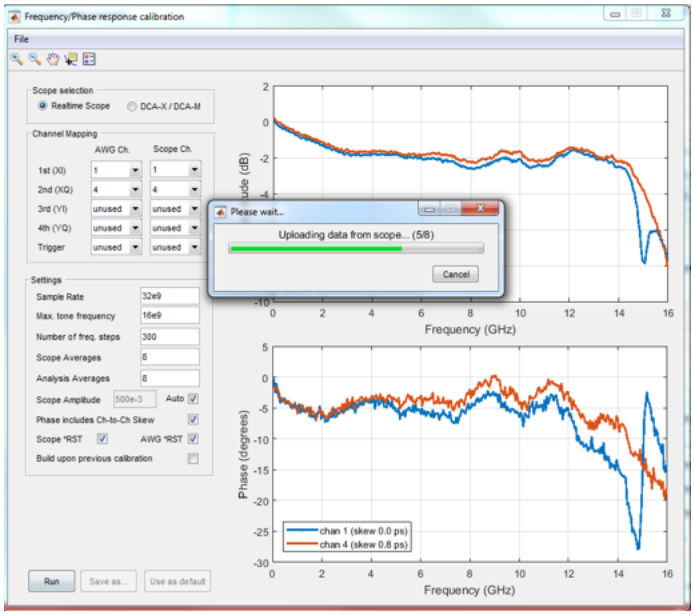


Figure 24 Viewing In-System Calibration results

10 To view the updated results, return to the **Correction Management** window.

- For 4-Channel mode

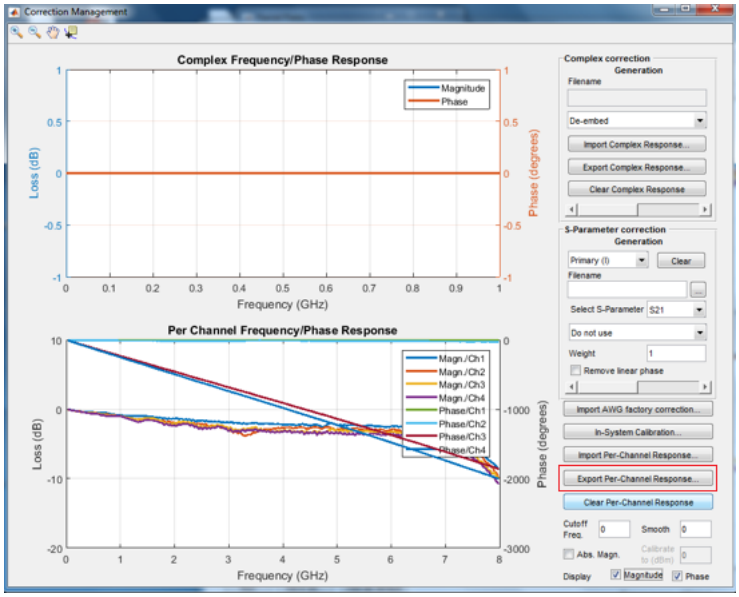


Figure 25 Exporting the Per-Channel Response

- For Dual-Channel mode

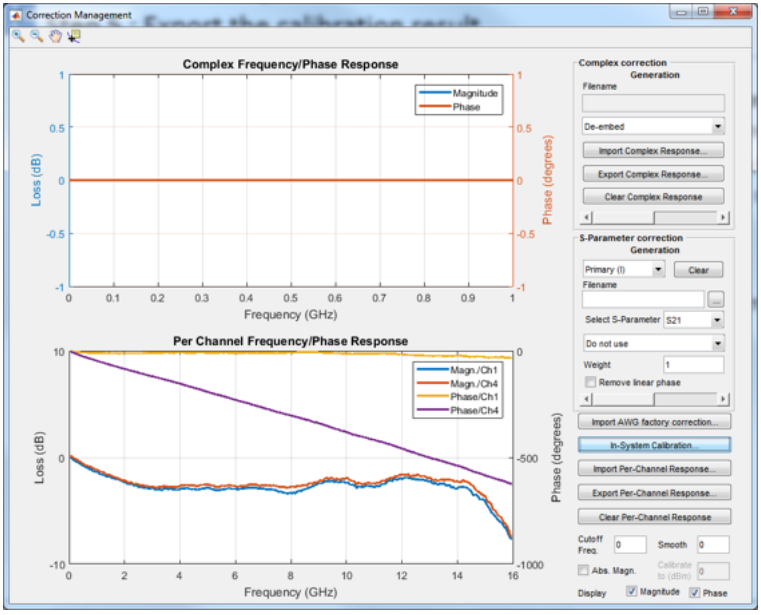


Figure 26 Exporting the Per-Channel Response

11 On the same window, click **Export Per-Channel Response...**.

12 On the **Save Frequency Response As...** window,

- For 4-Channel mode

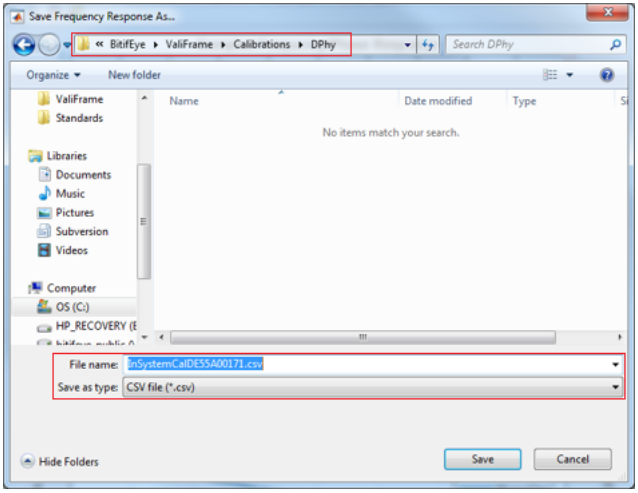


Figure 27 Saving the In-System Calibration values

a In the **Save as type:** drop-down field, select *CSV file (*.csv)*

b Navigate to the location *C:\ProgramData\BitifEye\ValiFrame\Calibrations\Dphy*

c Save the file with the following naming convention:

InSystemCal<*AWG-Serial-Number*>.csv

- For Dual-Channel mode

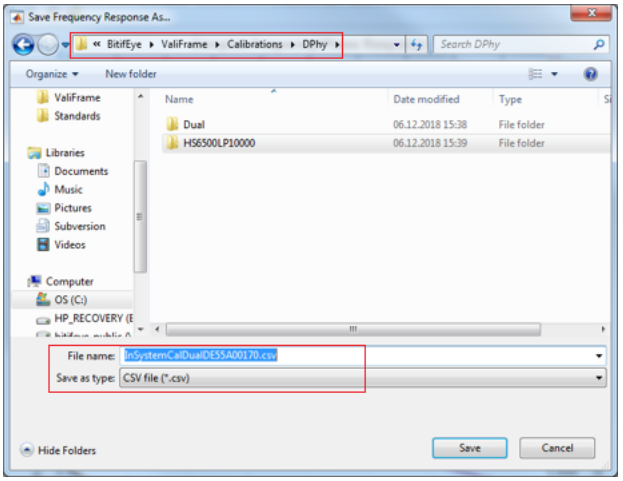


Figure 28 Saving the In-System Calibration values

a In the **Save as type:** drop-down field, select *CSV file (*.csv)*

b Navigate to the location *C:\ProgramData\BitifEye\ValiFrame\Calibrations\Dphy*

c Save the file with the following naming convention:

InSystemCalDual<*AWG-Serial-Number*>.csv

d To obtain the AWG Serial Number, go to **About Keysight M8195A**.

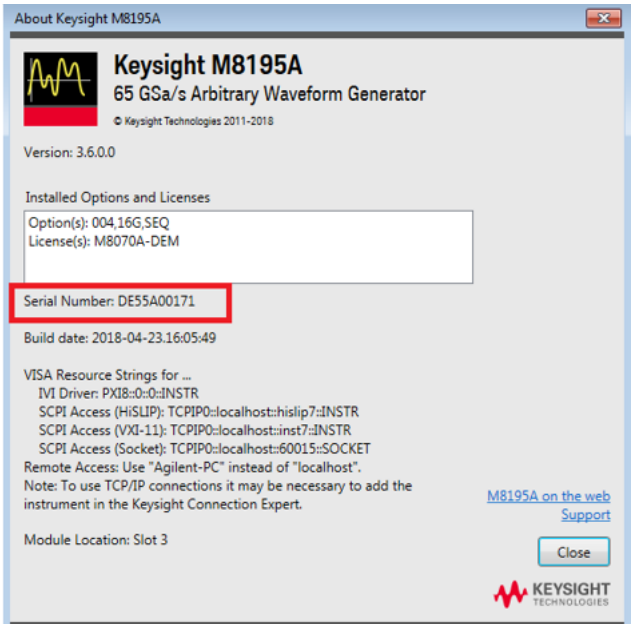


Figure 29 Identifying the AWG Serial Number

13 Repeat the entire process for each AWG that is physically connected.

14 Ensure to save the generated calibration output in the correct folder location with the CSV file format and the correct naming convention, as described earlier.

New Sequences in MIPI D-PHY 2.1

There are three sequences that are introduced in MIPI D-PHY specification 2.1 and the corresponding features in version 2.7 of the M8085A MIPI D-PHY CTS plug-in.

- Alternate Calibration Sequence
- Preamble Sequence
- HS-Idle Sequence

Understanding Alternate Calibration Sequence

When data rate of a transmitter signal is set to or modified to any value above 2.5 Gb/s, an alternate calibration sequence is applied. The purpose of this calibration is to achieve link power-up, link reinitialization, or both.

On signals operating at the aforementioned data rates, the Alternate Calibration Sequence follows an Initial Skew Calibration. The Alternate Calibration Sequence consists of a leading HS0 pattern, a Calibration Sync and a Calibration pattern (a PRBS9 sequence).

Figure 30 depicts the application of the Alternate Calibration Sequence after the Initial Skew Calibration Sequence in a signal with data rate above 2.5 Gb/s.

Figure 30 Signal with Alternate Calibration Sequence applied

To apply the Alternate Calibration Sequence in the signal generated using the MIPI D-PHY CTS, select **Frame (Sequence)** in the **Data Pattern** area followed by opening the *HsAlternateCal.seq* file from the location *C:\ProgramData\BitifEye\ValiFrame\Pattern\DPhy* in the **HS** field. Ensure that the **HS Data Rate** parameter is set to any value above 2.5 Gb/s. Then, click **Protocol Timings** in the **Signal Modifications & Impairments** area. Here, the **TX-InitialSkewCal Duration** parameter controls the timing for the Deskew Pattern in the Initial Skew Calibration Sequence applied on the signal, as shown in Figure 30.

To set the duration for the Calibration Pattern (PRBS9) in the Alternate Calibration Sequence, configure the value for **TX-AlternateCal Duration** parameter, which corresponds to the T_{ALTCAL} duration, as shown in Figure 31. As per *Table 19: Alternate Calibration Timing Parameters* of the *MIPI Alliance Specification for D-PHY*^{SM} *version 2.1*, the typical value of T_{ALTCAL_SYNC} is 8 UI whereas the maximum value that can be configured for T_{ALTCAL} duration, which corresponds to the **TX-AlternateCal Duration** parameter in the MIPI D-PHY plug-in, is 100 µs.

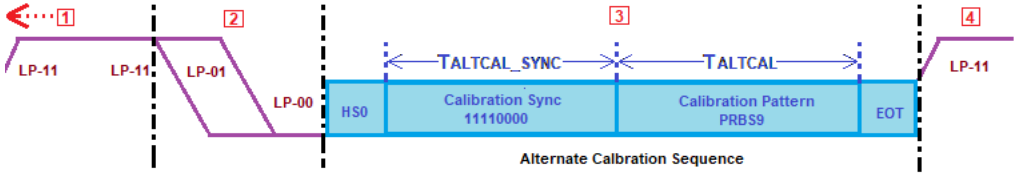


Figure 31 Understanding the Alternate Calibration Mode

Let's consider Figure 31 again to correlate the elements in the diagram with the Alternate Calibration Sequence file definition, which is applied in the MIPI D-PHY CTS plug-in during signal generation.

Following are the contents of the Alternate Calibration Sequence file *HsAlternateCal.seq*:

HSFreq: 1 GBit/s;

Blocks:

Init: LP11N128;

PreCal: LP11N16,LPHS;

AlternateCal: AlternateCal;

PostCal: LP11N128;

HS: LP11N1,B"HsCompliancePattern.dat",LP11N1;

LP: LP11N1,LPB"LpCompliancePattern.dat",LP11N1;

Sequence:

1. Init,1;

2. PreCal,1;

3. AlternateCal,1;

4. PostCal,1;

The *Init* block defines the LP-11 state along with the Initial Skew Calibration Sequence, which is depicted by the region marked as 1 in red text.

The next block *PreCal* defines the region marked as 2 in red text, where the signal transitions from LP-11 to LP-10 state.

The Alternate Calibration mode is defined by the *AlternateCal* block and is marked as 3 in red text. This block consists of a small HS-0 state followed by Calibration Sync pattern (11110000) of 8 UI duration. Then, a payload of PRBS9 sequence is sent in the Alternate Calibration Pattern, wherein a PRBS sequence generator is initialized prior to the Alternate Calibration to achieve the required payload, where the LSB is transmitted first. For more information regarding the PRBS sequence generated for the Alternate Calibration mode, refer to section *6.13 Alternate Calibration Sequence* of *MIPI Alliance Specification for D-PHY^{SM} version 2.1*.

The *PostCal* block, which defines the transition to LP-11 state is marked as 4 in red text.

The HS and LP blocks are not shown in the figure but they indicate that after the 128 iterations of LP-11 state, the next LP-11 state marks the beginning of the HS data payload (defined in the *HsCompliancePattern.dat* file) and another LP-11 state marks the end of the HS block. Similarly, the LP data payload (defined in the *LpCompliancePattern.dat* file) has one LP-11 state at the beginning and end of the LP block.

Therefore, for signals transmitted above 2.5 Gbps, the Alternate Calibration Sequence of **TX-AlternateCal Duration** is inserted; whereas for signals with data rate less than 2.5 Gbps, the Alternate Calibration Sequence is optional.

Understanding Preamble Sequence

On signals that are transmitted at data rates above 2.5 Gbps, the Preamble Sequence of short length can be optionally inserted at the start of every high speed (HS burst) payload to achieve a better clock-to-data skew, which occurs due to variations in temperature and voltage.

A normal High Speed Burst consists of an HS-0 state followed by a leader sequence with a pattern 00011101, which marks the beginning of the High-Speed Packet Data. The Preamble Sequence can be inserted just before the Leader Sequence.

The Preamble Sequence consists of a preamble pattern 101010 with a duration of $T_{PREAMBLE}$, which can be configured from a minimum of 32 UI to a maximum of 512 UI, as per *Table 20: Preamble Timing Parameters* of

the *MIPI Alliance Specification for D-PHY^{SM} version 2.1*. The Preamble Sequence also contains an Extended Sync pattern HS-1 of fixed length and with a duration of $T_{EXTSYNC}$, having a typical duration of 8 UI. The Extended Sync pattern is required to separate the Preamble Sequence from the Leader Sequence, to prevent the former from being detected by receivers as the Leader Sequence.

To enable Preamble Sequence on a High Speed Burst in the M8085A MIPI D-PHY CTS plug-in, the option **Preamble** in the **Data Pattern** area must be checked. Also, you can set the multiplier value for the required preamble steps to be inserted into the HS Burst by configuring the **TX-HsPreamble Steps** parameter under **Parameters**. By default, this value is set to 1, which corresponds to a typical $T_{PREAMBLE}$ duration of 32 UI. The plug-in multiplies the configured value of the Preamble Steps parameter with 32 UI, which in turn, sets the $T_{PREAMBLE}$ duration on the signal. Only prerequisite for the Preamble Sequence to be inserted by the MIPI D-PHY CTS is that the **HS Data Rate** must be configured to a value more than 2.5 Gb/s, otherwise the plug-in ignores the Preamble flag even if enabled.

Figure 32 shows the difference in the appearance of a normal High Speed Burst and a High Speed Burst that has Preamble Sequence enabled.

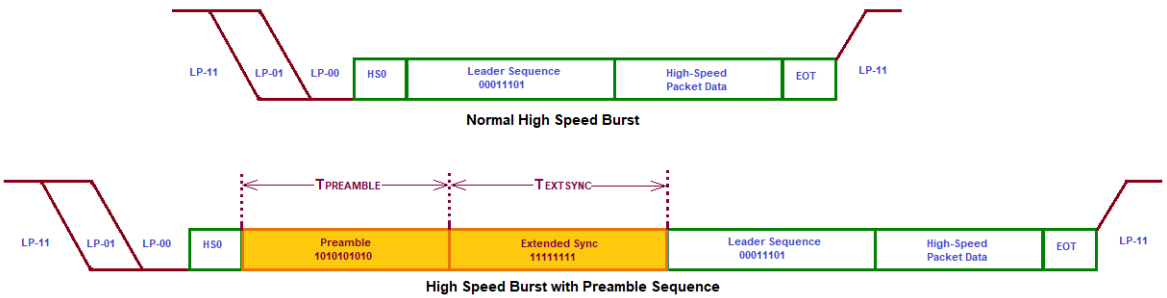


Figure 32 High Speed Burst - without and with Preamble sequence applied

Understanding HS-Idle Sequence

The HS-Idle Sequence is used to apply an HS-Idle state between two High-Speed Data Bursts during HS signaling, that is, without the need for transitioning to LP signaling. The purpose for using the HS-Idle state is to reduce the latency between the two HS Data Bursts, based on the data rate and HS-Idle timings.

As shown in Figure 33, the HS-Idle state comprises of HS-Idle-Post, HS-Idle-ClkHS0 and HS-Idle-Pre sub-states, with durations $T_{HS-IDLE-POST}$, $T_{HS-IDLE-CLKHS0}$ and $T_{HS-IDLE-PRE}$, respectively. After the last bit of the HS Data Bursts on all lanes, the Clock lane continues signaling for a duration of $T_{HS-IDLE-POST}$. Then, the Clock lane enters into HS-0 state for a duration of $T_{HS-IDLE-CLKHS0}$ and eventually, the Clock lane is active for a duration $T_{HS-IDLE-PRE}$ prior to exiting from HS-Idle state and entering into the first bit of the next HS Data Burst. For more information regarding the state transitions for the HS-Idle state, refer to section *6.15 HS-Idle State* of *MIPI Alliance Specification for D-PHY^{SM} version 2.1*.

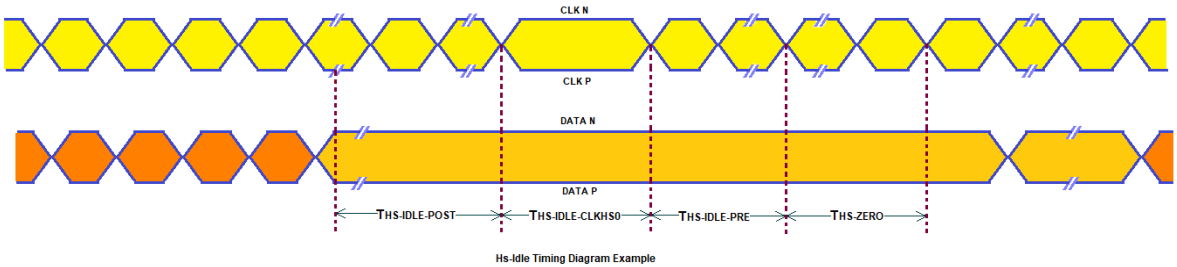


Figure 33 Signal with HS-Idle state applied

To apply the HS-Idle states in the signal generated using the MIPI D-PHY CTS, select **Frame (Sequence)** in the **Data Pattern** area followed by opening the *HsIdle.seq* file from the location *C:\ProgramData\BitifEye\ValiFrame\Pattern\DPhy* in the **HS** field. Then, in the list of **Parameters**, the **TX-HsIdlePost Duration** parameter controls the $T_{HS-IDLE-POST}$ duration, the **TX-HsIdleClkHs0 Duration** parameter controls the $T_{HS-IDLE-CLKHS0}$ duration and the **TX-HsIdlePre Duration** parameter controls the $T_{HS-IDLE-PRE}$ duration of the HS-Idle state. By default, the M8085A MIPI D-PHY CTS plug-in sets the “Default” values of these three timing parameters. The minimum, default and maximum values for each of these timing parameters are defined in *Table 21: HS-Idle State Timing Parameters* of *MIPI Alliance Specification for D-PHY^{SM} version 2.1*.

Let's correlate the elements in the diagram with the HS-Idle Sequence file definition, which is applied in the MIPI D-PHY CTS plug-in during signal generation.

Following are the contents of the HS-Idle Sequence file *HsIdle.seq*:

```
HSFreq: 1 GBit/s;

Blocks:
Init: LP11N128;
PreHs:LP11N1,B"HsCompliancePattern.dat";
Idle: HsIdleState;
PostHs:B"HsCompliancePattern.dat",LP11N1;

Sequence:
1. Init,1;
2. PreHs,1;
3. Idle,1;
4. PostHs,1;
LoopTo 1;
```

The *Init* block defines the LP-11 state.

The *PreHs* block defines the HS data payload (defined in the *HsCompliancePattern.dat* file) prior to entering Hs-Idle state.

Unlike other sequences, an LP-11 state does not mark the end of the HS data payload. Instead, the *Idle* block, which defines the HSIdleState, indicates the transition of the last bit of the HS data burst into the HS-Idle state.

Similarly, the next block *PostHs* defines the HS data payload (defined in the *HsCompliancePattern.dat* file) after exiting the Hs-Idle state.

2 Sequence and Data Files

Data File Format (*.dat or *.txt) / 59
Sequence File Format(*.seq) / 60
Sequence File Definition for CSI / 68
Sequence File Definition for DSI / 77

The test data are contained in sequence files, with the extension '.seq'. A sequence file consists of two parts: the Block definitions and the Sequence definition.

Modes supported by the MIPI D-PHY CTS

The MIPI D-PHY CTS plug-in supports two different mode groups:

- The Burst mode: In the Burst Modes (Burst, Burst Continuous Clock, Pure HS) a block of data is repeated infinitely. This block can contain LP Data and HS Data, pure LP data or pure HS data depending on the content of the data given for HS and LP. If either HS or LP data is empty (an empty text box for that particular data type), the software generates pure LP/HS data. If Pure HS is selected, no LP11 transitions are included and all LP data is neglected. The burst mode requires two sequences of data, one sequence for HS and other for LP. Each sequence can be set manually or be read by the software from a data file.A block consists of a name followed by one or more LP blocks:
  - LP Blocks: The format is LPxyNn. x and y can be 0 or 1, depending on the desired LP state. n represents the number of LP states.
- The Frame mode: In these modes (Frames and Frames, Continuous HS Clock), a sequence file allows running a sequence of blocks ending with an infinite loop over the complete number of blocks or an selection of the last blocks. Each individual block can be repeated (“looped”) N-times and the number of repetitions N can be selected for each block separately. In addition to the data files, the frame modes require a sequence file. It specifies the data rates and the sequence of blocks. The M8085A MIPI D-PHY CTS plug-in supports sequence files conforming to the CSI and DSI protocol standards. While the section below describes sequence file formats in general, refer to “Sequence File Definition for CSI” on page 68 and “Sequence File Definition for DSI” on page 77 to understand sequence file formats for CSI and DSI protocols respectively.

Data File Format (*.dat or *.txt)

For data definition in the MIPI D-PHY CTS plug-in, the hexadecimal (HEX) format is required. Bytes are represented in two digits, each ranging from 0 to 9 and A to F. The leading string "0x" is optional. Supported separators between data bytes are:

, (comma)

; (semicolon)

space (blank)

tab

line feed

nothing

Some examples:

- 0x01, 0xF3, 0x23
- 0134E734FF
- 32 FF E5 44

In addition to the pure HEX data, special commands are abbreviations of lists of hex bytes:

- 0x<HEX code>N<count>: repeat the byte <HEX code> <count> times.

For example: 0xABN5 is equal to AB AB AB AB AB.

- 0x<HEX code>S<count> repeat the byte <HexCode> N times for each data lane. In a one-data lane configuration the macro is similar to 0x<HEX code>N<count>, but in a multi-lane setup, it will repeat <HexCode> at each data lane <count> times.

For example, 0xABS4 is equal to AB AB AB AB in a 1-lane configuration, but will become AB AB AB AB at each data lane for a multi-lane setup.

An example for 2 data lanes:

0x02c05 is equal to D0: 02 03 04 05 and D1: 02 03 04 05.

For the counter with the "x" and two data lanes, 0x02x05 would lead to D0: 02 04 and D1: 03 05.

NOTE **The special commands require the leading "0x", otherwise they will not be recognized.**

Sequence File Format(*.seq)

For waveform generation in the MIPI D-PHY CTS plug-in, you may use sequence files. In the sequence file the data rate, data blocks and sequence are defined. Note that all parameters are even integers. The structure of a sequence file is shown in Figure 34.

HSFreq: <frequency in bits/s>

Blocks:

<BlockName 1>: <Block Definition 1>, ..., <Block Definition n1>;

...

<BlockName M>: <Block Definition 1>, ...,<Block Definition nM>;

Sequence:

1. <BlockName J>, <Loop Count R>; - First block

...

<N>. <BlockName K>, <Loop Count S>; - Nth block

...

<P>. <BlockName L>, <Loop Count T>; - Pth block

[LoopTo N]

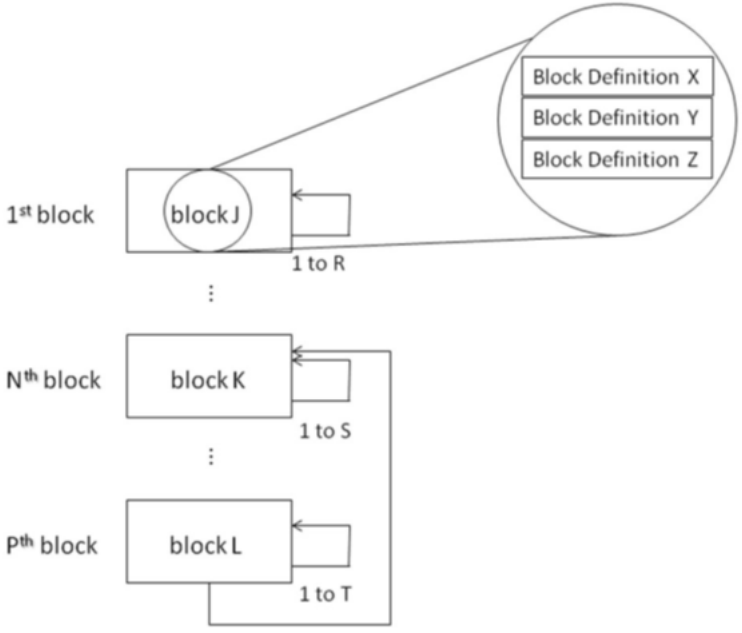


Figure 34 Block Diagram of a Sequence Example

Each block can comprise multiple sub-blocks (1 to n). Sub-blocks can be used in multiple blocks. In the sequence, blocks can be used as often as needed. Within the sequence, the LoopTo expression starts an infinite loop from block <N> to the last block <P>. If no LoopTo expression is specified, an infinite loop is created from block 1 to block P. Valid block definitions are:

- LP00, LP01, LP10, LP11: for a single LP state.
- LP<LP state 00,01,10, or 11>[<LP state 00,01,10, or 11>...] Only available in the Manual LP Framing mode and for LP pattern. It allows a sequence of LP states to be defined in one statement.

  For example: LP1101001011
- LPB"<filename>": for generating LP data specified in the file with the name <filename>. The file should be in the same folder as the sequence file. At the beginning of the data an escape trigger for LP or ULP data mode is sent before the data and a Mark-0/1 sequence is sent after the end of the data. For the data, the data file format given above must be used.

- LP<00, 01, 10, or 11>N<number of bits>: The LP state is sent <number of [HS] bits> times.
- LP<00, 01, 10, or 11>E<number of bits>: The LP state is sent until the block size reaches the number of HS bits given in <number of bits>.
- LPHSE<number of bits>: The block is filled with LP11 states and a LP–HS transition until the number of HS bits <number of bits> is reached.
- LPHS: The macro adds a LP–HS transition. It is mainly for influencing the block ending. If for example the following block starts with HS data, then the LP-HS transition will done at the end of the actual block. Without this macro the LP-HS transition would be added to the beginning of the following block. You do not need the macro for the following B macros, since they will trigger a LP-HS transition automatically if the previous block description contained LP states.
- B"<filename>": for generating HS data given in the file <filename>. The file should be in the same folder as the sequence file. If necessary, a LP-to-HS transition is generated before the data. A HS-to-LP transition is added if the following block contains LP states.
- BL<number of blanking bytes>: for generating HS blanking packets with a number of blanking bytes given in <number of blanking bytes>. The id (0x19), word counter, ECC (Error-Correcting Code) and CRC (Cyclic Redundancy Check) are calculated and added such that the number of bits is equal to (<number of blanking bytes>+6)*8;
- C<3 hex bytes>: For generating short packets like they are described in the CSI or DSI specifications. The resulting short packet will have the first byte as Data ID of this packet and the following two bytes as Packet DATA followed by the ECC for that packet. If necessary, a LP-to-HS transition is generated before the data. A HS-to-LP transition is added if the following block contains LP states.
- C<1 hex byte>"<filename>": for generating a long packet. The content in the filename will be taken as payload. The header will have the given hex byte as ID followed by a two byte word counter, followed by a ECC for that header data. At the end of the payload, a two byte CRC is added. If necessary, an LP-to-HS transition is generated before the data. An HS-to-LP transition is added if the following block contains LP states.

- PRBS<no.>(<seed1>|<seed2>| ... | <seedN>): for generating a PRBS of the polynomial <no.> with a seed of <seed1-N> for each lane. The <no.> is just a decimal number (only 9 is allowed), and the seeds are given in a hex number (example 0x789A). The number of input seeds should be the same as active lanes (example for 3 lanes <seed1> goes to D0, <seed2> goes to D1 and <seed3> goes to D2). If #seeds > #lanes the latest seeds will be ignored. If #seeds < #lanes an exception will be thrown. As a special case, if only one seed is provided but more than one lane is active, the pattern is distributed among all lanes.
- ULPEntry: Adds the ULP Entry escape sequence to the block. After the ULPEntry LP00 states plus finally an ULPExit should follow to create a specification conform ULP sequence.
- ULPExit<number of LP10 states>: Creates a ULP exit sequence. It is not allowed to combine this block definitions with other definitions, which means in this case the block must only contain this macro and no other.
- InitialSkewCal: adds an HS clock pattern to all data lanes to generate the skew calibration block at the beginning of the data transmission (see *MIPI Alliance Specification for D-PHY^{SM} Version 2.1*). It is not allowed to combine this block definition with other definitions, which means in this case the block must only contain this macro and no other. The block before needs to contain a LPHSE or LPHS block as last entry to force the frame generator to put the special LP-HS transition for the sync pattern at the end of the previous block. In this case, the sync word is replaced by 0xFF. In the sequence definition the loop counter value for the block will be replaced by a suitable value to generate the clock pattern for duration **TX-InitialSkewCal Duration** parameter given via the CTS user interface.
- PeriodicSkewCal: similar to InitialSkewCal, adds an HS clock pattern for line de-skew. This block is meant to be within the looped part of the pattern, and the same restriction as for InitialSkewCal apply. The duration of the line de-skew will be set by the **TX-PeriodicSkewCal Duration** parameter in the CTS user interface.

NOTE

- If blocks are looped, then the beginning of the block should have the same kind of data mode (LP or HS) as the block following it, otherwise the block loop will result in invalid LP to HS transitions.
- Video Frames which contain LP11 blanking periods should be rotated so that the block definition always ends with a LP11E command.
- If only the header contains LP11 states, then the header block should end with LPHSE to start the HS transmission at the end of the header block.
- In case of PureHS mode, an initial LP to HS transition is added in the form of a hidden intro block in the waveform generation, before an infinite loop of pure HS data stream is generated.

In any case to each sequence, an LP11 block is added to the beginning of the sequence. If required, an LP-HS transition is added if the first block starts with HS data. Also, a sync block is added for the synchronization of the LP and HS subsystems. These blocks need not to be added explicitly to the sequence. They are added automatically for all sequences, that is, even if a sequence with pure HS blocks is given.

Automatic Clock Generation

Depending on the data lane pattern, a clock lane signal is generated which adheres to the MIPI D-PHY standard. For every high speed burst on the data lane a transition from LP to HS will be done on the clock lane. The HS clock will be active as long as the HS burst on the data lane is active. After the HS data burst ended the clock lane will also transition back to its stop state in case the next HS burst on the clock is far enough away to fit in the transition segments. In case this LP mode is active for a shorter duration on the data lane the HS clock will stay active for both bursts and not transition back to clock LP mode.

The following sections describe the various elements of a sequence file for the CSI and DSI protocols, such that the sequence file definition generates a waveform that conforms to the MIPI Specification for Camera Serial Interface (CSI) and MIPI Alliance Specification for Display Serial Interface (DSI), respectively.

Generally, a sequence file consists of three elements that form together a sequence:

- HS Data Rate
- Blocks
- Sequence

Following is a real time example of a sequence file definition:

Example of a Sequence File Definition:

HSFreq: 200MBit/s;

Blocks:

LPInit1: LPB"Esc0ms.txt",LP11E13728;

LPPause: LP11N1024;

LPInit2: LPB"Esc100ms.txt",LP11E13728;

LPInit3: LPB"Esc200ms.txt",LP11E13728;

Header: B"FirstHsLine.txt",LP11E6016;

Video: B"VideoLine.txt",LP11E6016;

Sequence:

1 LPInit1,1;
2 LPPause,20000;
3 LPInit2,1;
4 LPPause,20000;
5 LPInit3,1;
6 LPPause,20000;
7 Header,1;
8 Video,319;

LoopTo 6;

Following are the real time examples of DSI and CSI sequence file definitions, respectively:

Example of a DSI Sequence File Definition:

```
HSFreq: 432.432MBit/s;

Blocks:

LPInit: LPB"HSyncEnd.txt",LP11E13728;

HSync: B"HSyncEnd.txt",LP11E12736,B"HSyncStart.txt",LP11E13728;

VSyncStart: B"HSyncEnd.txt",LP11E12736,B"VSyncStart.txt",LP11E13728;

VSyncEnd: B"HSyncEnd.txt",LP11E12736,B"VSyncEnd.txt",LP11E13728;

Video: B"HSyncEnd.txt",LP11E960,B"Video480pHSyncStart.txt",LP11E13728;


Sequence:
1   LPInit,1;
2   HSync,5;
3   VSyncEnd,1;
4   HSync,29;
5   Video,480;
6   HSync,9;
7   VSyncStart,1;
LoopTo 2;
```

Example of a CSI Sequence File Definition:

```
HSFreq: 158 MBit/s;


Blocks:

FrameStart: B"FrameStart.txt",LP11E10880;

Blanking: LP11E10880;

Video: C1E"compliance640_480.txt",LP11E10880;

FrameEnd: B"FrameEnd.txt",LP11E2048;
```

```
Sequence:
1   FrameStart,1;
2   Blanking,1;
3   Video,480;
4   Blanking,2;
5   FrameEnd,1;
```

Sequence File Definition for CSI

Overview

CSI is a MIPI Alliance standard for serial interface between a camera module and host processor. CSI adheres to the Low-Level Protocol (LLP), which is a byte orientated, packet based protocol that supports the transport of arbitrary data using Short and Long packet formats. Two packet structures are defined for low-level protocol communication: Long packets and Short packets. The format and length of Short and Long Packets depends on the choice of physical layer (MIPI C-PHY or MIPI D-PHY). For each packet structure, exit from the low power state followed by the Start of Transmission (SoT) sequence indicates the start of the packet. The End of Transmission (EoT) sequence followed by the low power state indicates the end of the packet. However, in CSI implementation, one burst consists of only one packet and LP11 state must be inserted before the start of a burst. Since it requires to go to LP state always, an explicit EoT packet is not required.

NOTE **A sequence file used for MIPI D-PHY or MIPI C-PHY conformance testing cannot be used for CSI/DSI conformance testing unless the header, payload and checksum data is included in the CSI/DSI block definitions in the sequences else the device rejects the packet.**

Long and Short Packet Formats

Long Packet

For MIPI D-PHY, a Long Packet shall be identified by Data Types 0x10 to 0x37. A Long Packet for the MIPI D-PHY physical layer option shall consist of three elements: a 32-bit Packet Header (PH), an application specific Data Payload with a variable number of 8-bit data words, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count field and an 8-bit ECC. The Packet footer has one element, a 16-bit checksum (CRC).

For C-PHY, the Long Packet structure for the C-PHY physical layer option shall consist of four elements: a Packet Header (PH), an application specific Data Payload with a variable number of 8-bit data words, a 16-bit Packet Footer (PF), and zero or more Filler bytes (FILLER). The Packet Header is 6N x 16-bits long, where N is the number of C-PHY physical layer Lanes. The Packet Header consists of two identical 6N-byte halves, where each half consists of N sequential copies of each of the following

fields: a 16-bit field containing eight Reserved bits plus the 8-bit Data Identifier (DI); the 16-bit Packet Data Word Count (WC); and a 16-bit Packet Header checksum (PH-CRC) which is computed over the previous four bytes. The value of each Reserved bit shall be zero. The Packet Footer consists of a 16-bit checksum (CRC) computed over the Packet Data using the same CRC polynomial as the Packet Header CRC and the Packet Footer used in the MIPI D-PHY physical layer option. Packet Filler bytes are inserted after the Packet Footer, if needed, to ensure that the Packet Footer ends on a 16-bit word boundary and that each C-PHY physical layer Lane transports the same number of 16-bit words (i.e. byte pairs).

For both physical layer options, the 8-bit Data Identifier field and the 16-bit Word Count (WC) field contain identical data. The CSI receiver reads the next WC 8-bit data words of the Data Payload following the Packet Header. The length of the Data Payload shall always be a multiple of 8-bit data words. For both physical layer options, once the CSI receiver has read the Data Payload, it then reads the 16-bit checksum (CRC) in the Packet Footer and compares it against its own calculated checksum to determine if any Data Payload errors have occurred.

In either case, Packet Data length = Word Count (WC) * Data Word Width (8-bits).

Short Packet

For each option (MIPI C-PHY and MIPI D-PHY), the Short Packet structure matches the Packet Header of the corresponding Low Level Protocol Long Packet structure with the exception that the Packet Header Word Count (WC) field shall be replaced by the Short Packet Data Field. A Short Packet shall be identified by Data Types 0x00 to 0x0F. A Short Packet shall contain only a Packet Header; neither Packet Footer nor Packet Filler bytes shall be present. For Frame Synchronization Data Types, the Short Packet Data Field shall be the frame number. For Line Synchronization Data Types, the Short Packet Data Field shall be the line number.

For the MIPI D-PHY physical layer option, the Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Short Packet.

For the C-PHY physical layer option, the 16-bit Checksum (CRC) allows one or more bit errors to be detected in the Short Packet but does not support error correction.

Short Packet Data Types shall be transmitted using only the Short Packet format. Refer to Table 6 Synchronization Short Packet Data Type Codes of the MIPI Alliance Specification for Camera Serial Interface (CSI), which indicates that Data Type for Frame Start Code is 0x00 and Data Type for Frame End Code is 0x01.

NOTE Between Low Level Protocol packets, there must always be an HS-LP or an LP-HS transition.

Frame and Line Synchronization Packets

Frame Synchronization Packets

Each image frame shall begin with a Frame Start (FS) Packet containing the Frame Start Code. The FS Packet shall be followed by one or more long packets containing image data and zero or more short packets containing synchronization codes. Each image frame shall end with a Frame End (FE) Packet containing the Frame End Code. For FS and FE synchronization packets, the Short Packet Data Field shall contain a 16-bit frame number. This frame number shall be the same for the FS and FE synchronization packets corresponding to a given frame.

Line Synchronization Packets

Line synchronization packets are optional. For Line Start (LS) and Line End (LE) synchronization packets, the Short Packet Data Field shall contain a 16-bit line number. This line number shall be the same for the LS and LE packets corresponding to a given line.

Frame Blanking and Line Blanking

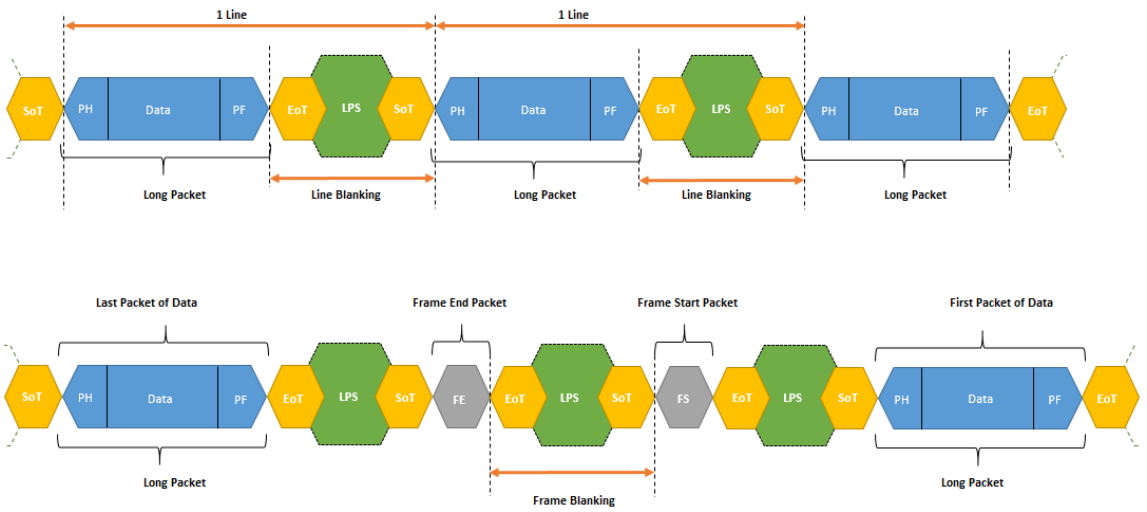


Figure 35 Block Diagram depicting packet structure for CSI sequence

Frame Blanking – The period between the Frame End packet in frame N and the Frame Start packet in frame N+1 is called the Frame Blanking Period.

Line Blanking – The period between the end of the Packet Footer (or the Packet Filler, if present) of one long packet and the Packet Header of the next long packet is called the Line Blanking Period.

Packet Data Payload Size Rules

For YUV, RGB or RAW data types, one long packet shall contain one line of image data. The total size of payload data within a long packet for all data types shall be a multiple of eight bits. The packet payload data format shall agree with the Data Type value in the Packet Header. Refer to *Section 11 Data Formats, Table 3 - Data Type Classes for eight different data type classes* and *Table 8 - Primary and Secondary Data Formats Definitions of the MIPI Alliance Specification for Camera Serial Interface (CSI)*.

To understand the concept of sequences in CSI implementation, consider the block diagram of a video packet shown below.

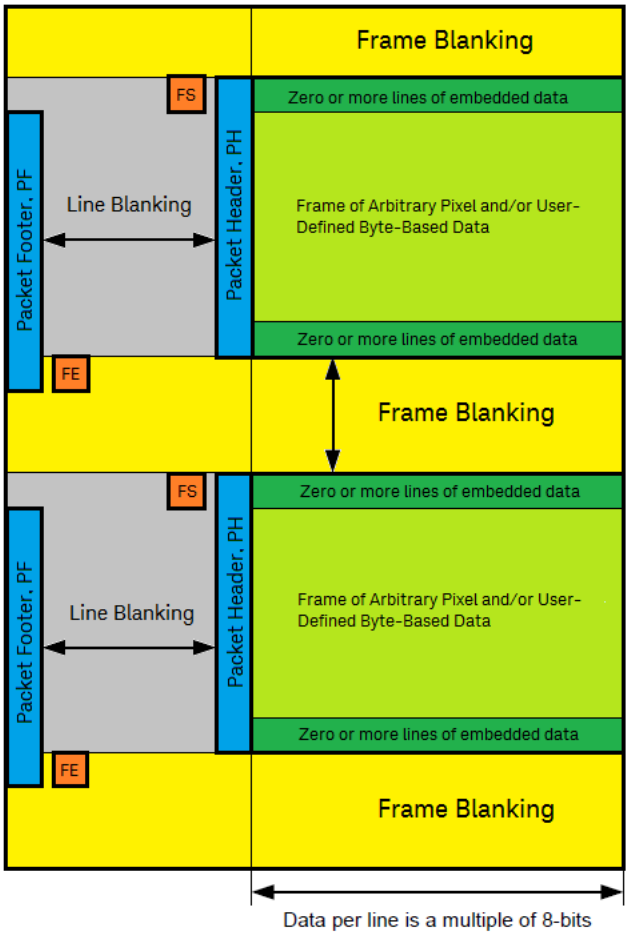


Figure 36 Block Diagram of a CSI Video Frame

For each video line transmission, the short packet or the FrameStart (FS) indicates start of transmission of the video packet. The payload data, which is contained in a long packet, consists of the Packet Header (PH),

followed by the actual arbitrary data and ending with the Packet Footer (PF). Another short packet or the FrameEnd (FE) indicates the end of transmission of the video packet. This data burst is in an HS state.

A Line Blanking (LP state) is transmitted between each video line, that is, after the end of a Packet Footer (PF) till the beginning of the next Packet Header (PH).

A Frame Blanking (LP state) is transmitted between each video frame, that is, after the end of a FrameEnd (FE) till the beginning of the next FrameStart (FS) short packet.

Understanding a CSI sequence file

The description of the block diagram corroborates the structure of the CSI sequence file shown below, for CSI implementation. Note that all the text files defined in the sequence must be placed in the same folder directory where the sequence file is located.

HSFreq: 158 MBit/s;

Blocks:

FrameStart: B"FrameStart.txt",LP11E10880;

Blanking: LP11E10880;

Video: C1E"compliance640_480.txt",LP11E10880;

FrameEnd: B"FrameEnd.txt",LP11E2048;

Sequence:

1. FrameStart,1;

2. Blanking,1;

3. Video,480;

4. Blanking,2;

5. FrameEnd,1;

The sequence definition in the given example contains an intrinsic looping. In the sequence, the blanking lines generate the frame blanking, and the video lines contain the line blanking, which is generated by the LP states. The number of lines for the video data and the associated blanking is defined by the device manufacturer. The sequence begins with the

FrameStart block running once, followed by a Blanking line. Then, the Video block runs for 480 lines ending with another Blanking line, followed by the FrameEnd block running once. This sequence loops over until manually aborted.

If considered closely, the FrameStart block generates the Frame Start (FS) short packet, with the Frame Start Code 0x00 as its header. This follows an HS-LP transition using LP11, where a line blanking is performed with an LPE marker, which fills the LP states until 10880 HS states are attained. The Blanking block generates a frame blanking packet of LP11, which fills the LP states until 10880 HS states are attained and is generated to provide for the LP-HS transition before the actual video payload begins transmitting. In the Video block, the C-Macro with a 1-byte data type of 0x1E generates the Packet Header of the long packet, followed by the actual payload video data (in Hex format) in the compliance640_480.txt file.

Since the video data is High-Speed, the end of the video packet follows an HS to LP transition with a line blanking packet of LP11, which fills the LP states until 10880 HS states are attained. Two blanking lines are sent to indicate the end of the video payload data and to save energy. The FrameEnd block generates the Frame End (FE) short packet, with the Frame End Code 0x01 as its header. This follows an HS-LP transition with a line blanking packet of LP11, which fills the LP states until 2046 HS states are attained.

Some other points to note are:

- Since you cannot send more than one packet per burst, Blanking (LP state) is inserted at the end of each burst to avoid HS data from concatenating.
- The length of the line and frame blanking is device dependent.
- The data type 0x1E corresponds to the pixel color code YUV422 8-bit used in the video. Refer to Section 11 Data Formats of the MIPI Alliance Specification for Camera Serial Interface (CSI) for more information about the other Data Types for various color codes.
- The line blanking length and bits per pixel of a specific color code helps you in determining the total line length in HS states. The E-marker is used for the LP states instead of N, such that it fills up the blocks until the total defined length of HS States is attained.

NOTE **To retain the same line rate for CSI implementation between MIPI D-PHY and MIPI C-PHY, it is recommended that you keep the number of HS states equal in the LP definition.**

If all lines in a sequence file definition have an LPE statement in the end, you may calculate the Frame Rate:

1 Multiply the number of lines with the number defined in the LPE statement of the sequence file definition.

2 Repeat step 1 for all lanes in the frame and add the resulting values for each lane.

3 Multiply the sum of all lanes with the HS period length, which derives the Frame Rate.

Calculating HS Data Rate for CSI sequence

To calculate the minimum HS data rate required to run the sequence, you must be aware of at least the frame rate and the device's display resolution, which is provided by the device manufacturer. The HS Frequency is the first line in the definition of a sequence file.

For example, let us consider that the device under test has a Frame Rate of 30 Hz and a display resolution of 640 x 480 pixels, where 640 is the horizontal resolution (or the length of each line) and 480 is the vertical resolution (or the number of video lines).

1 Calculate the line rate using the equation:

Line Rate = Frame Rate * Vertical Resolution

However, the number of video lines has certain number of blanking lines preceding and following the video data, which must be considered as well for data rate calculation. The equation for line rate is, therefore, modified to:

Line Rate = Frame Rate * (Vertical Resolution + no. of blanking lines)

Let us assume that there are 10 blanking lines in a frame.

In this case, Line Rate = 30 Hz * (480 + 10) = 14700 Hz

2 Determine the total length of lines in HS states.

i Determine the number of bits required for transmission of the video data. To do so, check the pixel color coding for the Data Type in the video. In this case, the pixel color code is YUV422, which uses 8-bit per pixel.

Total no. of bits per line = Bit-size per pixel * Horizontal resolution

In this case, Total no. of bits = 8 * 640 = 5120 bits per line.

ii The number of bits for video transmission is not sufficient for determining the total length of lines in HS states, since extra time is required for the LP states in the line blanking. Therefore,

you must consider the LP states and accordingly extend the bits per line. Considering these factors, a total length of 10880 lines in HS states can be safely used for calculation of the HS data rate.

3 Calculate the HS Data Rate using the equation:

Data Rate = Line Rate * Total length of lines in HS state

In this case, Data Rate = 14700 Hz x 10880 = 159.936 Mbps

Therefore, you can define the HS Data Rate (HSFreq) in the beginning of the sequence file, as shown in the example above.

For information on the CSI implementation in the MIPI D-PHY and MIPI C-PHY physical layer and detailed understanding of the protocol layer, refer to the *MIPI Alliance Specification for Camera Serial Interface (CSI)*.

Sequence File Definition for DSI

Overview

DSI specifies the interface between a host processor and a peripheral such as a display module. It builds on existing MIPI Alliance specifications by adopting pixel formats and command set specified in DPI-2, DBI-489 2 and DCS standards. Some significant differences between DSI and CSI are:

- CSI uses unidirectional high-speed Link, whereas DSI is half-duplex bidirectional Link
- CSI makes use of a secondary channel, based on I2C, for control and status functions
- CSI data direction is from peripheral (Camera Module) to host processor, while DSI's primary data direction is from host processor to peripheral (Display Module)
- CSI sequence file structure is different from that of the DSI sequence file structure. The former consists of only of the FrameStart and FrameEnd packet along with some blanking lines, whereas the latter consists of HSync, VSync and Blanking packages.

At the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets. The protocol defines required headers for each packet, and how header information is generated and interpreted.

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted in the Protocol layer to packets, following the packet organization. The Protocol layer appends packet-protocol information and headers, and then sends complete bytes through the Lane Management layer to the PHY. Packets are serialized by the PHY and sent across the serial Link. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands.

If there are multiple Lanes, the Lane Management layer distributes bytes to separate PHYs, one PHY per Lane, as described in Section 6 of the MIPI Alliance Specification for Display Serial Interface (DSI). Packet protocol and formats are independent of the number of Lanes used. The DSI protocol permits multiple packets to be concatenated, which substantially boosts effective bandwidth. This is useful for events such as peripheral initialization, where many registers may be loaded with separate write commands at system startup. There are two modes of data transmission, HS and LP transmission modes, at the PHY layer. Before an HS transmission can be started, the transmitter PHY issues a SoT sequence to

the receiver. After that, data or command packets can be transmitted in HS mode. Multiple packets may exist within a single HS transmission and the end of transmission is always signaled at the PHY layer using a dedicated EoT sequence. To enhance the overall robustness of the system, DSI defines a dedicated EoT packet (EoTp) at the protocol layer for signaling the end of HS transmission. In HS mode, time gaps between packets shall result in separate HS transmissions for each packet, with a SoT, LPS, and EoT issued by the PHY layer between packets. This constraint does not apply to LP transmissions.

Long and Short Packet Formats

Two packet structures are defined for low-level protocol communication: Long packets and Short packets. For both packet structures, the Data Identifier (DI) is always the first byte of the packet, which includes information specifying the type of the packet.

Long Packet

A Long packet shall consist of three elements: a 32-bit Packet Header (PH), an application-specific Data Payload with a variable number of bytes, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

After the end of the Packet Header, the receiver reads the next Word Count multiplied by the bytes of the Data Payload.

Once the receiver has read the Data Payload it reads the Checksum in the Packet Footer. The host processor shall always calculate and transmit a Checksum in the Packet Footer. Peripherals are not required to calculate a Checksum. Also, note the special case of zero-byte Data Payload: if the payload has length 0, the Checksum calculation results in (0xFFFF). If the Checksum is not calculated, the Packet Footer shall consist of two bytes of all zeros (0x0000). In the generic case, the length of the Data Payload shall be a multiple of bytes. In addition, each data format may impose additional restrictions on the length of the payload data, e.g. multiple of four bytes.

Short Packet

A Short packet shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length. The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet. Some short packets may also contain some data in the payload.

Long and Short packets have several common elements. The first byte of any packet is the DI (Data Identifier) byte. The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte. Peripherals shall support ECC in both forward- and reverse-direction communications.

DSI Sequence Format Description

Sync Event (H Start, H End, V Start, V End), Data Type = XX 0001 (0xX1)

Sync Events are Short packets and, therefore, can time-accurately represent events like the start and end of sync pulses. As “start” and “end” are separate and distinct events, the length of sync pulses, as well as position relative to active pixel data, e.g. front and back porch display timing, may be accurately conveyed to the peripheral. The Sync Events are defined as follows:

- Data Type = 00 0001 (0x01) V Sync Start
- Data Type = 01 0001 (0x11) V Sync End
- Data Type = 10 0001 (0x21) H Sync Start
- Data Type = 11 0001 (0x31) H Sync End

To represent timing information as accurately as possible a V Sync Start event represents the start of the VSA. It also implies an H Sync Start event for the first line of the VSA. Similarly, a V Sync End event implies an H Sync Start event for the last line of the VSA.

Sync events should occur in pairs, Sync Start and Sync End, if accurate pulse-length information must be conveyed. Alternatively, if only a single point (event) in time is required, a single sync event (normally, Sync Start) may be transmitted to the peripheral. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Display modules that do not need traditional sync/blanking/pixel timing should transmit pixel data in a high-speed burst then put the bus in Low Power Mode, for reduced power consumption.

EoTp, Data Type = 00 1000 (0x08)

This short packet is used for indicating the end of a HS transmission to the data link layer. Therefore, detection of the end of HS transmission may be decoupled from physical layer characteristics. The main objective of the EoTp is to enhance overall robustness of the system during HS transmission mode. Therefore, DSI transmitters should not generate an EoTp when transmitting in LP mode. The Data Link layer of DSI receivers

shall detect and interpret arriving EoTps regardless of transmission mode (HS or LP modes) to decouple itself from the physical layer. Unlike other DSI packets, an EoTp has a fixed format as follows:

- Data Type = DI [5:0] = 0b001000
- Virtual Channel = DI [7:6] = 0b00
- Payload Data [15:0] = 0x0F0F
- ECC [7:0] = 0x01

Blanking Packet (Long), Data Type = 01 1001 (0x19)

A Blanking packet is used to convey blanking timing information in a Long packet. Normally, the packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Like all packets, the Blanking packet contents shall be an integer number of bytes. Blanking packets may contain arbitrary data as payload.

The Blanking packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes, and a two-byte checksum.

Packed Pixel Stream, 16-bit Format, Long Packet, Data Type 00 1110 (0x0E)

This long packet (shown in the sequence example) is used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum.

Packet Header Error Detection/Correction

The host processor in a DSI-based system shall generate an error-correction code (ECC) and append it to the header of every packet sent to the peripheral. The ECC takes the form of a single byte following the header bytes. The ECC byte shall provide single-bit error correction and 2-bit error detection for the entire Packet Header.

Checksum Generation for Long Packet Payloads

Long packets are comprised of a Packet Header protected by an ECC byte and a payload of 0 to 216-1 bytes. To detect errors in transmission of Long packets, a checksum is calculated over the payload portion of the data packet. Note that, for the special case of a zero-length payload, the 2-byte checksum is set to 0xFFFF.

Checksum generation and transmission is mandatory for host processors sending Long packets to peripherals. It is optional for peripherals transmitting Long packets to the host processor. However, the format of Long packets is fixed; peripherals that do not support checksum generation shall transmit two bytes having value 0x0000 in place of the checksum bytes when sending Long packets to the host processor. The host processor shall disable checksum checking for received Long packets from peripherals that do not support checksum generation.

NOTE **An ECC byte can be applied to both Short and Long packets. Checksum bytes shall only be applied to Long packets.**

Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral timing requirements dictate which format is appropriate. In the following sections, Burst Mode refers to time-compression of the RGB pixel (active video) portion of the transmission.

Non-Burst Mode with Sync Pulses

This mode enables the peripheral to accurately reconstruct original video timing, including sync pulse widths. Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power. During HSA, HBP and HFP periods, the bus should stay in the LP-11 state.

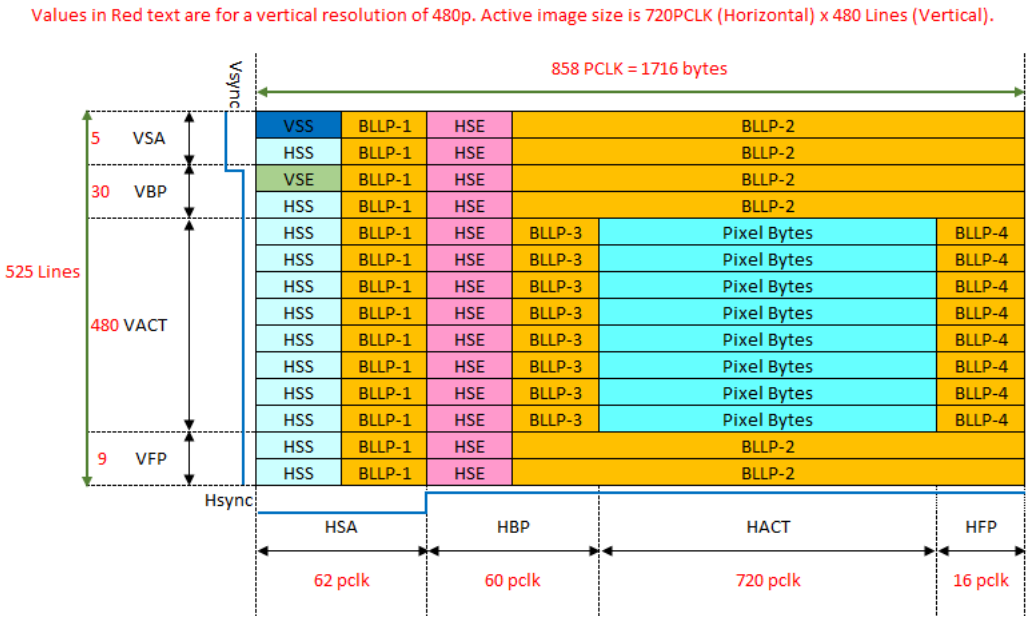


Figure 37 Block Diagram for Video transmission in Non-Burst mode with Sync Pulses

Non-Burst Mode with Sync Events

This mode functions in the same manner as the previous mechanism, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted. Here, only the start of each synchronization pulse (VSyncSHSyncStart and HSyncStart) is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

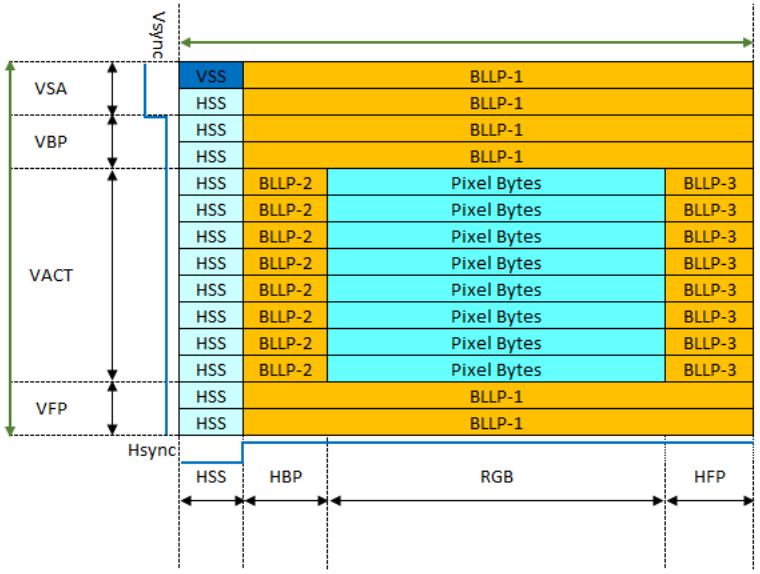


Figure 38 Block Diagram for Video transmission in Non-Burst mode with Sync Events

Burst Mode

RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link. In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. In the same manner as the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

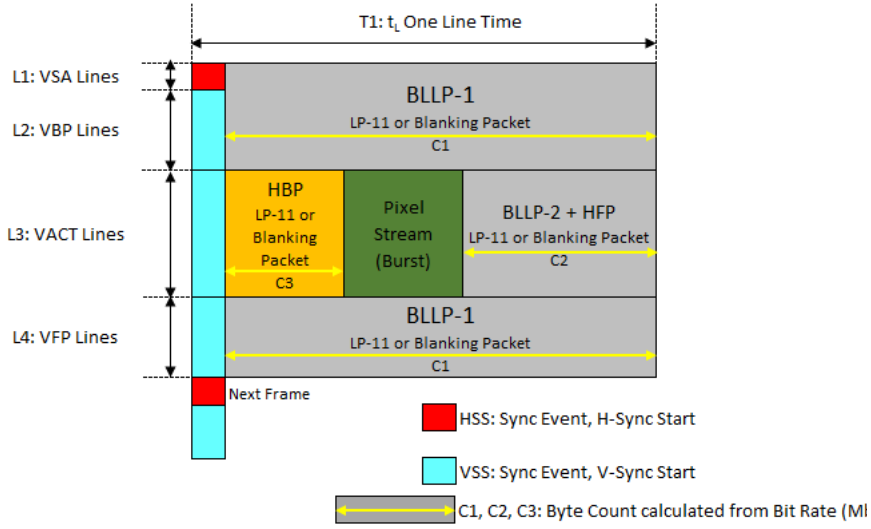


Figure 39 Block Diagram for Video transmission in Burst mode

Note that for accurate reconstruction of timing, packet overhead including Data ID, ECC, and Checksum bytes should be taken into consideration.

To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; The host processor should return to LP state once per scan-line during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero, and burst mode will be indistinguishable from non-burst mode.

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VSS; all other lines shall start with VSE or HSS. Note that the position of synchronization packets, such as VSS and HSS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Replacing B-Macros with C-Macros in a sequence file

Table 5 shows how a sequence file written originally using the B-Macros can be alternatively written using C-Macros.

Table 5 Sequence file definition using B-Macros and C-Macros

Sequence File Definition using B-Macro	Sequence File Definition using C-Macro
HSFreq: 432.432MBit/s; Blocks: LPInit: LPB"HSyncEnd.txt",LP11E13728; HSync: B"HSyncEnd.txt",LP11E12736,B"HSyncStart.txt",LP11E13728; VSyncStart: B"HSyncEnd.txt",LP11E12736,B"VSyncStart.txt",LP11E13728; VSyncEnd: B"HSyncEnd.txt",LP11E12736,B"VSyncEnd.txt",LP11E13728; Video: B"HSyncEnd.txt",LP11E960,B"Video480pHSyncStart.txt",LP11E13728; Sequence: 1. LPInit,1; 2. HSync,9; 3. VSyncStart,1; 4. HSync,5; 5. VSyncEnd,1; 6. HSync,29; 7. Video,480; LoopTo 2;	HSFreq: 432.432MBit/s; Blocks: LPInit: LPB"HSyncEnd.txt",LP11E13728; HSync: C310000,C080F0F,LP11E12736,C210000,C080F0F,LP11E13728; VSyncStart: C310000,C080F0F,LP11E12736,C010000,C080F0F,LP11E13728; VSyncEnd: C310000,C080F0F,LP11E12736,C110000,C080F0F,LP11E13728; Video: C310000,C080F0F,LP11E960,C0E"Video480p.txt",BL20,C210000,C080F0F ,LP11E13728; Sequence: 1. LPInit,1; 2. HSync,9; 3. VSyncStart,1; 4. HSync,5; 5. VSyncEnd,1; 6. HSync,29; 7. Video,480; LoopTo 2;

Upon considering each block closely, notice the following differences, otherwise the rest of the sequence definition remains the same.

- In the HSync block, the B“HSyncEnd.txt” is replaced by C310000,C080F0F and B“HSyncStart.txt” is replaced by C210000,C080F0F.
- In the VSyncStart block, the B“HSyncEnd.txt” is replaced by C310000,C080F0F and B“VSyncStart.txt” is replaced by C010000,C080F0F.
- In the VSyncEnd block, the B“HSyncEnd.txt” is replaced by C310000,C080F0F and B“VSyncEnd.txt” is replaced by C110000,C080F0F.
- In the Video block, the B“HSyncEnd.txt” is replaced by C310000,C080F0F and B“Video480pHSyncStart.txt” is replaced by C0E“Video480p.txt”,BL20,C210000,C080F0F.

To understand how the replacements were done, you must read the description given in the earlier sections about the B“<filename>” macro, C<3 hex bytes> and C<1 hex byte>” <filename>” macros.

Let us consider the contents of each text file closely.

Contents of HSyncEnd.txt

3100 0001

080F 0F01

As mentioned in the previous sections, the Data Type for the HSyncEnd signal is 0x31, which means this short packet has its Data ID as 31 and the following two bytes of Packet DATA as 00 00 followed by the ECC of 01.

Therefore, in a sequence, B“HSyncEnd.txt” can be written using the C<3 hex bytes> macro as C310000.

Contents of HSyncStart.txt

2100 0012

080F 0F01

As mentioned in the previous sections, the Data Type for the HSyncStart signal is 0x21, which means this short packet has its Data ID as 21 and the following two bytes of Packet DATA as 00 00 followed by the ECC of 12.

Therefore, in a sequence, B“HSyncStart.txt” can be written using the C<3 hex bytes> macro as C210000.

Contents of VSyncEnd.txt

1100 0014

080F 0F01

As mentioned in the previous sections, the Data Type for the VSyncEnd signal is 0x11, which means this short packet has its Data ID as 11 and the following two bytes of Packet DATA as 00 00 followed by the ECC of 14.

Therefore, in a sequence, B“VSyncEnd.txt” can be written using the C<3 hex bytes> macro as C110000.

Contents of VSyncStart.txt

0100 0007

080F 0F01

As mentioned in the previous sections, the Data Type for the VSyncStart signal is 0x01, which means this short packet has its Data ID as 01 and the following two bytes of Packet DATA as 00 00 followed by the ECC of 07.

Therefore, in a sequence, B“VSyncStart.txt” can be written using the C<3 hex bytes> macro as C010000.

Notice that within each text file considered so far, a hexadecimal value 080F 0F01 is mentioned. This is the EoT package, which is used at end of each HS transmission in a short packet. The EoT package has a fixed format with Data ID as 08, Payload Data as 0F0F and ECC of 01.

Therefore, at the end of each C<3 hex bytes> macro defined for the four files, you must add the C<3 hex bytes> macro for the EoT package as C080F0F, as shown in the sequence definition.

Contents of Video480pHSyncStart.txt

0EA0 0508

1084 1084

1084 1084

1084 1084

.

.

.

1084 1084

FA44 1914

001F 0000

0000 0000

0000 0000

0000 0000

0000 0000

0000 6F1D

2100 0012

080F 0F01

The elements of the actual video data in the file ‘Video480pHSyncStart.txt’ can be divided as follows:

- The header consists of Data ID: 0E followed by a two-byte word counter A005, followed by the ECC for that header data as 08.
- The actual video payload data starts from a hex value of 1084 and ends at a hex value of 1084. Note that the payload data is too long and has been truncated for documentation purpose.
- At the end of the payload, a two byte CRC is added, which is FA44.
- After the checksum, a Blanking packet is added to covey the blanking timing information in this video packet. This Blanking packet consists of the DI byte of 0x19, a two-byte Word Count of 1400, an ECC byte of 1F, a payload of 20 bytes, and a two-byte checksum of 6F1D. This blanking packet enables the HS-LP transition and corresponds to the HFP (Horizontal Front Porch) before the HSyncStart.
- In the end, a short packet in HS mode is generated, which has the HSyncStart data, which allows the HS-LP transition, before the device goes into a low power state.

Looking back at the Video block, the B“Video480pHSyncStart.txt” is replaced by C0E“Video480p.txt”,BL20,C210000,C080F0F, which indicates that only the actual payload data has been extracted into another text file named Video480p.txt and the rest of the data is appended using the C-Macro to the beginning and to the end of the payload data file. Notice that the Blanking packet with Data ID 0x19, which was part of the initial payload data, has been rewritten using the BL<number of blanking bytes> macros as BL20.

Irrespective of whether you use the B-Macros or the C-Macros, you must ensure that the data is defined in the correct order and you can use the sequence file in either format for waveform generation in the plug-in.

Notice that there has been no change made to the LPInit block of the sequence file, even though the HSyncEnd.txt file is used. This is because even though the HSyncEnd.txt contains hexadecimal data for HS mode, the LPB“filename” macro is used for generating Low Power data specified in the file HSyncEnd.txt, such that the display device is powered on.

To know more about the Data Types required to construct the short or long packets or to define C-Macros in a sequence file, refer to the *MIPI Alliance Specification for Display Serial Interface*.

Understanding a DSI sequence file

The DSI sequence file corresponds to the package structure shown in the image below, which is based on the Non-Burst mode with Sync Pulses:

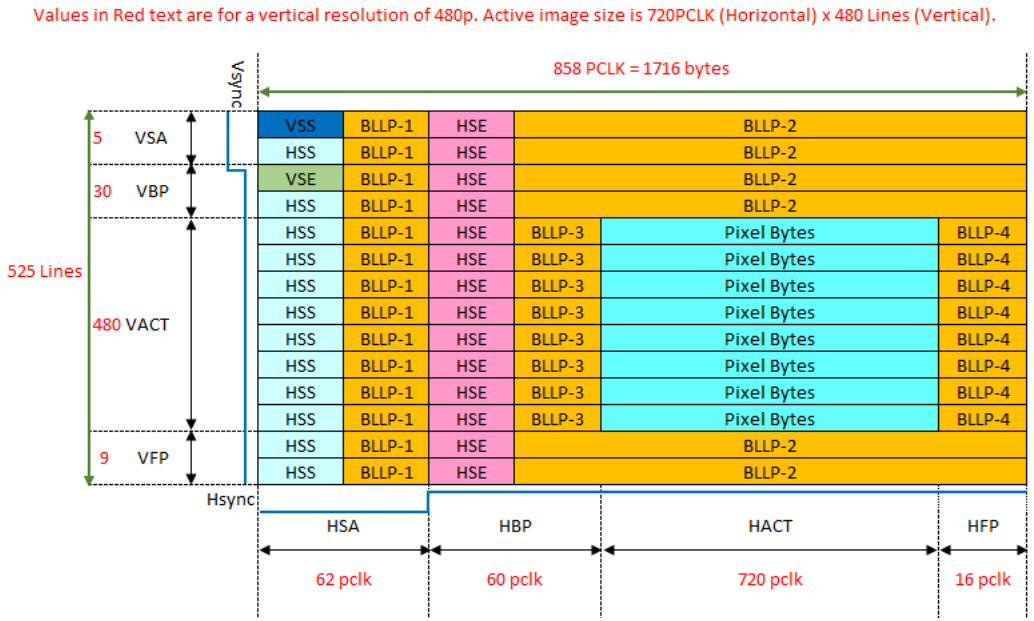


Figure 40 Block Diagram for Video transmission in Non-Burst mode with Sync Pulses

In general, the way the DVI functions is like the CRT mode. In a video frame of the CRT mode, an electron beam performed several horizontal traces and a vertical trace to begin the next frame. In the current technology, the HSS corresponds to the several horizontal traces whereas VSS corresponds to the vertical trace.

The VSyncStart (VSS) and HSyncStart (HSS) pulse are generated to mark the start of the video frame and define the timings of the device. For a video with resolution 720x480p, there are 720 horizontal active pixels, represented by HACT and 480 vertical active lines, represented by VACT. The device manufacturer provides the information about the horizontal blanking pixels and the vertical blanking lines that must be included to meet the timing and power saving requirements of the device, apart from the video transmission. In this case, a total of 138 horizontal blanking pixels are added to the 720 horizontal active pixels. Also, a total of 45

vertical blanking lines are added to the 480 vertical active lines. These HSync and VSync data is required for proper synchronization of the video data and to achieve proper timing in displaying the video data and is represented by HSyncActive (HSA) and VSyncActive (VSA), respectively. As described earlier, HSS, HSE, VSS and VSE are short packets containing High Speed data and blanking header information. They are part of the HSA and VSA.

Sync events are introduced such that only HSS have to be added. In this case, where Sync pulses are used, Blanking Lines can be added, which may be HS or LP, depending on the timing set between HSS and HSE.

The Horizontal Back Porch (HBP), Horizontal Front Porch (HFP), Vertical Back Porch (VBP), Vertical Front Porch (VFP) are indicated by BLLPs. The Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. The BLLP provides for the HS-LP and LP-HS transition when the device is powered on, during the switch to video mode and to save the device's power either in the idle state or just before the start of the video data. In this image, the HBP and HFP are indicated by BLLP-3 and BLLP-4, respectively whereas VBP and VFP are indicated by BLLP-1 and BLLP-2, respectively.

Now, let us consider the example given below of a sequence file for DSI implementation, derived from the video package displayed in the image above.

HSFreq: 432.432MBit/s;

Blocks:

LPInit: LPB"HSyncEnd.txt",LP11E13728;

HSync: C310000,C080F0F,LP11E12736,C210000,C080F0F,LP11E13728;

VSyncStart: C310000,C080F0F,LP11E12736,C010000,C080F0F,LP11E13728;

VSyncEnd: C310000,C080F0F,LP11E12736,C110000,C080F0F,LP11E13728;

Video:
C310000,C080F0F,LP11E960,C0E"Video480p.txt",BL20,C210000,C080F0F,LP11E13728;

Sequence:

1. LPInit,1;

2. HSync,9;

3. VSyncStart,1;

4. HSync,5;

5. VSyncEnd,1;

6. HSync,29;

7. Video,480;

LoopTo 2;

The LPInit block generates the HsyncEnd signal is a low power mode to power on the display device.

To achieve proper synchronization and timing for the video data, the HSync and VSync signals are used. The number of vertical blanking lines and horizontal blanking pixels are provided by the device manufacturer.

The HSync block, which loops over for 9 lines, generates the HSE signal, indicated by C310000,C080F0F before the device switches to low power mode until 12736 HS states are attained. The LP11E12736 corresponds to BLLP-2 on the image. Then, HSS signal is generated, indicated by C210000,C080F0F, after which the device enters into low power mode again until 13728 HS states are attained. The LP11E13728 corresponds to BLLP-1 on the image.

The VSyncStart block, which loops over once, generates the HSE signal followed by LP11E12736 state. Then, VSS signal is generated, indicated by C010000,C080F0F, after which the device enters into low power mode again until 13728 HS states are attained.

The HSync block loops over for 5 lines again before the VSyncEnd block loops over once. The VSyncEnd block generates the HSE signal followed by LP11E12736 state. Then, VSE signal is generated, indicated by C110000,C080F0F, after which the device enters into low power mode again until 13728 HS states are attained.

The HSync block loops over for 29 lines again before the Video block loops over for 480 lines. In the Video block, the HSE signal is generated followed by LP11E960 state. Here, in the duration between the Video line and HSyncEnd, there is a short LP state to allow the device to save power before the video starts. LP11E960, which forms the HBP, allows device to save power before switching to video mode. C0E“Video480p.txt” indicates the header information followed by the active payload data contained in the “Video480p.txt” file. The Video block displays BL20, which forms the HFP, before the HSS is generated again followed by switching into low power mode until 13728 HS states are attained.

Note that BLLP-1 and BLLP-2, that is, LP11E12736 and LP11E13728 are blanking lines. Instead of sending video data, long LP states are generated. The total number of HS states is driven by the E marker, which

means each line has a fixed duration, depending on the data rate. It includes the HS states before the LPE marker is defined and the time taken to switch to the HS mode.

You must always ensure that to define a proper sequence, each block must end with the same HS or LP state to avoid any unexpected loops.

Calculating HS Data Rate for the DSI sequence

To calculate the minimum HS data rate required to run the sequence, you must be aware of at least the frame rate, the Blanking Lines (HBlank and VBlank) and the device's display resolution, in other words, the pixels per line and lines per frame, which are provided by the device manufacturer. The HS Frequency is the first line in the definition of a sequence file.

For example, let us consider that the device under test has a Frame Rate of 60 Hz and a display resolution of 640 x 480 pixels, where 640 is the horizontal resolution (or the length of each line) and 480 is the vertical resolution (or the number of video lines). The number of header (blanking lines) is given as 45.

1 Calculate the total no. of lines using the equation:

   Total Lines = Video Lines + Header (Blanking) lines = 480 + 45 = 525 lines

2 Calculate the Line Rate using the equation:

   Line Rate = Frame Rate * Total Lines = 60 Hz x 525 lines = 31.5 kHz

3 Calculate the No. of pixels per line using the equation:

   No. of pixels per line = HBlanking + Horizontal Resolution

   where, the HBlanking data is given by the device manufacturer. Let us assume 160 HBlanking lines.

   Therefore, No. of pixels per line = 160 + 640 = 800 pixels per line.

4 Determine the number of bits required for transmission of the video data. To do so, check the pixel color coding for the Data Type in the video from the device's specification. In this case, the pixel color code is RGB, which uses 24-bits per pixel.

   Calculate the total no. of bits per line using the equation:

   Total no. of bits per line = Bit-size per pixel * No. of pixels per line

   In this case, Total no. of bits per line = 24 * 800 = 19.2 kbits per line

5 Calculate the HS Data Rate using the equation:

   Data Rate = Line Rate * Total no. of bits per line

   In this case, Data Rate = 31.5 kHz * 19.2 kbits per line = 604.8 Mbps

Therefore, for a VGA mode video with a frame rate of 60 Hz, you must set a data rate of 604.8 Mbps, which you can define as HSFreq in the beginning of the sequence file.

For information on the DSI implementation in the MIPI D-PHY and MIPI C-PHY physical layer and detailed understanding of the protocol layer, refer to the *MIPI Alliance Specification for Display Serial Interface*.

3 Results Description and Procedure Parameters

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MIPI D-PHY Receiver Test Software Procedure Parameters / 97

During the execution of all calibration and test procedures, the results are displayed automatically in a data table as well as graphically.

CAUTION

Before executing the calibration or test procedures, ensure that the System Connections are made properly with all necessary Setups. All calibrations and test procedures can be run in offline mode, that is, without any instrument connected. The offline mode is intended for product demonstrations with simulated data. CALIBRATIONS THAT ARE RUN IN OFFLINE MODE DO NOT GENERATE VALID CALIBRATED VALUES.

Result Description

Once the selected procedure is finished, an indicator shows the final status (such as, Pass / Fail / Incomplete) of a procedure. The meaning of the indicator is described in the Table 6.

Table 6 Indicator's result description table

Indicator	Description
	Procedure successfully passed the present run in online mode.
	Procedure successfully passed the present run in offline mode.
	Procedure could not proceed with the present run. Most likely the DUT failed during initialization or the test was stopped, so no test was conducted.
	Procedure failed the present run in online mode.
	Procedure failed the present run in offline mode.

MIPI D-PHY Receiver Test Software Procedure Parameters

The Procedure Parameters are available for each calibration and test procedure. You can see the selected Parameters at the right hand side of the user interface. The displayed parameters are only associated with the selected procedure. Procedures often have parameters with the same name, but the meaning may be slightly different and a change of a parameter value only affects the selected procedure.

4 Calibrations

Connections and Probing Methods / 100
Commonly used Procedure Parameters for Calibration Tests / 101
Calibration Large LP Amplitude / 104
Calibration Small LP Amplitude / 114

During the execution of all calibration and test procedures, the results are displayed automatically in a data table as well as graphically.

CAUTION

Before executing the calibration or test procedures, ensure that the System Connections are made properly with all necessary Setups. All calibrations and test procedures can be run in offline mode, that is, without any instrument connected. The offline mode is intended for product demonstrations with simulated data. CALIBRATIONS THAT ARE RUN IN OFFLINE MODE DO NOT GENERATE VALID CALIBRATED VALUES.

Connections and Probing Methods

Probing for LP Levels Calibration

For both Large and Small Amplitude LP Calibrations, the connection must be Single-Ended, Into Open. This can be achieved by connecting the outputs of the AWG to an N7010A active termination adapter.

Probing for HS Levels Calibration

For the HS Calibration, the connection must be Differential (one output of AWG is connected to the Normal and other is to the Complement for the calibrated channel), 100 Ohm Terminated. This can be achieved by connecting the outputs of the AWG to an N7010A active termination adapter.

Probing for Jitter Calibrations / Eye Opening Calibration

For the Jitter Calibrations, connect the outputs of the AWG lines (Clock N, Data P and Data N) with SMA direct connection to the oscilloscope (Channel 1, 2, 4).

Commonly used Procedure Parameters for Calibration Tests

Table 7 shows commonly used Procedure Parameters for Calibration Tests.

Table 7 MIPI D-PHY commonly used Procedure Parameters for Calibration Procedures

Common Parameter Name	Parameter Description
Acquisition Length	Minimum number of acquisition points (in UI) to be captured to perform calibration.
Calibration Channel Clock	Channel used to perform calibration on the Clock signal.
Calibration Channel Complement	Channel used to perform calibration on the inverted signal.
Calibration Channel Data	Channel used to perform calibration on the Data signal.
Calibration Channel Normal	Channel used to perform calibration on the non-inverted signal.
Calibration Pattern File	Pattern file that is used for calibration procedures, which is different from the pattern file used for configuring the DUT.
Calibration Sequence File	Sequence file that is used for calibration procedures, which is different from the sequence file used for configuring the DUT.
Differential Voltage Amplitude	Differential Voltage value applied during the ISI and Eye Height Calibrations.
DSO Number of Samples	Number of Sampling points set on the Oscilloscope to form the eye during calibration.
DSO Sampling Rate	Sampling rate of the Oscilloscope used during calibration. It calculates the averaging interval and must be set properly before the filtering is applied. If the oscilloscope is not capable to support 40GSa/s (default), this parameter can be modified in the Expert Mode, but generally, modification is not required.
Eye Height Target	Eye height value to be calibrated.
Eye Width Max. Variation	Maximum variation (in percentage) in Eye width value that is allowed during calibration.
Eye Width Target	Eye width value to be calibrated.
HS Sequence File	Sequence file that is used for the HS data instead of the sequence file specified while configuring the DUT.
In-System Calibration	Applies In-System AWG Calibration data to improve signal quality. Set to 'On' or 'Off' in the Configuration panel.
Initial Transition Time	Initial value of the transition time when calibration must be performed.
Jitter Frequency	Frequency of the induced Sinusoidal Jitter (that is, data rate divided by 10)
Logical 0 Threshold	Threshold voltage for the spike to meet logic 0.
Logical 1 Threshold	Threshold voltage for the spike to meet logic 1.

Max Amplitude Level	Maximum amplitude level set for calibration.
Max Energy Value	Maximum energy value calibrated for the e-Spike calibration.
Max Level	Maximum V_ILHS value that is calibrated.
Max LP High Level	Maximum V_OH value that is calibrated. For Small Amplitudes, the maximum threshold is 750mV whereas for Large Amplitudes, the maximum threshold is 1.3V.
Max LP Low Level	Maximum V_OL value that is calibrated.
Max Offset	Maximum AWG offset value to be set for the calibration.
Max Swing Value	Maximum value of the differential amplitude that is calibrated.
Max Threshold Difference	Maximum difference value of VIH-V_IL.
Maximum Transition Time	Maximum transition time taken to set the calibration.
Min Amplitude Level	Minimum amplitude level set for calibration.
Min Energy Value	Minimum energy value calibrated for the e-Spike calibration.
Min Level	Minimum V_ILHS value that is calibrated.
Min LP High Level	Minimum V_OH value that is calibrated.
Min LP Low Level	Maximum V_OL value that is calibrated.
Min Offset	Minimum AWG offset value to be set for the calibration.
Min Swing Value	Minimum value of the differential amplitude that is calibrated.
Min Threshold Difference	Minimum difference value of VIH-V_IL.
Minimum Transition Time	Minimum transition time taken to set the calibration.
Offline	Indicates whether the procedures are running offline or not.
Oscilloscope Bandwidth	Sets the Optimal Bandwidth of the Oscilloscope required to perform Calibrations. The bandwidth of 10GHz is applied when a Low Pass Filter is not applied on the AWG. If a Low Pass Filter is applied, the maximum bandwidth of the Oscilloscope can be used. Without a Low Pass Filter, there is noise in signal found with an Oscilloscope Bandwidth of 30GHz or higher.
Oscilloscope SSC Scale	Oscilloscope scale for the smoothing function
Reference Channel S-Parameter File	S-Parameter file selection for applying ISI. Default file is “ReferenceChannel_Standard.s4p” which contains the S-parameters of the MIPI standard channel. At data rates 4.5 Gbps and lower, the long channel is required to get enough ISI to close the eye with 0.2 UI.
Show Real Time Eye	Shows the Real Time on the oscilloscope during the measurements, if set to ‘On’; otherwise it suppresses the display of the Real Time Eye, this speeds up the measurement.
SJ Amplitude Range	Sets the start and stop values along with the steps size and stepper type of the Sinusoidal Jitter amplitude sweep.

SJ Frequency	Applied Sinusoidal Jitter frequency.
Skew Tolerance	Skew limit value. The calibration is finished if the skew between normal and complement channels is below this limit.
SSC Deviation	SSC minimum point or the maximum deviation of the nominal data rate (only 0 and negative values are allowed, because it is a down-spread SSC).
SSC Frequency	SSC frequency used to perform calibration.
Stepper Type	Stepping Mechanism applied to attain calibration. Select 'Linear' or 'BinarySearch' to apply transition time steps either at regular intervals (linear mode) or at an equivalent value of lower/higher limit of the transition time.
Step Size	Value used to decrement/increment at each step from minimum to maximum or vice-versa.
Target SSC Derivative	Value of SSC Derivative that must be achieved during Calibration.
Transfer Function Chan1	Sets the transfer function file for channel 1.
Transfer Function Chan2	Sets the transfer function file for channel 2.
Transfer Function Chan3	Sets the transfer function file for channel 3.
Transfer Function Chan4	Sets the transfer function file for channel 4.
Transition Time	Transition time required to perform ISI calibration. Ensure to set the same value for all dependent tests.
Transition Time Step	Step size on the transition time, which is required to attain calibration.
Use InfiniiSim	If set to 'On', the InfiniiSim transfer function of the Oscilloscope is applied instead of the replica trace.

Calibration Large LP Amplitude

Common Connection Diagram

The following diagrams illustrates the connection settings for all Calibration Large LP Amplitude procedures using the M8195A AWG configuration.

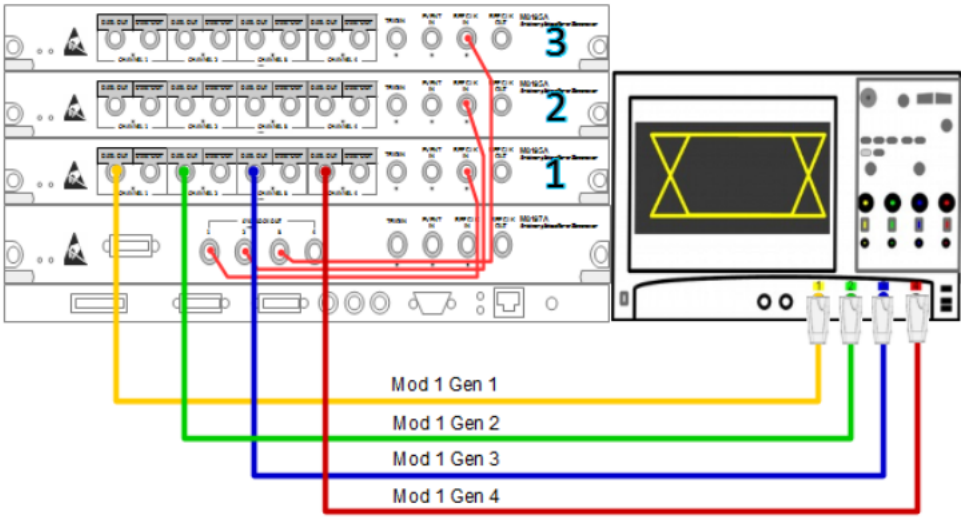


Figure 41 Connection Settings for Calibration Large LP Amplitude procedures

Skew Calibration Module 1

Connection

Refer to Common Connection Diagram on page 104.

Purpose

This procedure is used to calibrate the skew of all channels within a module by adjusting the skew of each channel so that the signals are aligned in the reference plane. This calibration should be run at each module.

Dependencies

No other calibration is required for this procedure.

Prior to conducting this calibration, the oscilloscope channels need to be de-skewed to avoid errors caused by the internal skew of the oscilloscope channels. This calibration is needed for all CTS tests.

Procedure

The normal data output signals of all channels within the module are connected to the DSO channels (1 to 4) respectively with SMA cables. For this procedure, the skew must be calibrated with the values lesser than the Skew Tolerance value. At first, a clock pattern is generated at the first channel and the skew is adjusted for all channels with respect to the first channel. The skew is measured and calibrated iteratively until its value is smaller than the given tolerance value.

Parameters

The parameters used for this calibration are listed alphabetically in Table 7.

Results

Table 8 Calibration data table "Skew Calibration"

Parameter name	Parameter description
Result	▪ Pass: the system skew was adjusted below the skew limit value. ▪ Fail: the adjustment failed.
Skew Value [ps]	It is the skew value of the channel with respect to the first channel of the module.

Amplifier Level Calibration Module 1 Gen 1 Clock Normal

Connection

Refer to Common Connection Diagram on page 104.

Purpose

It is used to calibrate the amplitude and offset values of all channels within a module. It also adjusts the amplitude and offset settings in order to make the measured values should be equal at all channels. It is run at each module of the AWG (separately for each channel).

Dependencies

No other procedure is required for this calibration.

Procedure

To start the calibration procedure, follow the steps given below:

- Connect the normal data output of all channels within the module to the DSO channels (1 to 4) respectively with SMA cables or use N7010A probes.
- It sets Target values for the Amplitude (difference between the LP high level and low level values) and Offset using the default values. Then, the AWG generates an LP signal with the default values of LP high level, LP low level and offset
- Once the LP signal is generated, the LP high level, LP low level, and offset are measured using an oscilloscope. Then, it checks whether the measured values are within the limits or not. If not, it continues to set the difference value (between measured and default) with-in the step till it finds the measured values within the limits.
- At each Generator, the above two steps are repeated and at the same time, both target and measured values are stored.

Parameters

The parameters used for this calibration are listed alphabetically in Table 7.

Results

Table 9 Calibration data table "Amplifier Level Calibration Module 1 Gen 1 Normal"

Parameter name	Parameter description
Result	▪ Pass: the adjustment passed. ▪ Fail: the adjustment failed.
Set Amplitude [mV]	Maximum Amplitude level set for the calibration. For proper calibration, the plug-in reduces the set amplitude level of the LP signal according to the defined Step Size.
Measured Value for Offset = 300 [mV]	Measured calibrated value when amplitude is offset by 300mV.
Measured Value for Offset = 200 [mV]	Measured calibrated value when amplitude is offset by 200mV.
Measured Value for Offset = 100 [mV]	Measured calibrated value when amplitude is offset by 100mV.
Measured Value for Offset = 0 [mV]	Measured calibrated value when amplitude is offset by 0mV.

Amplifier Level Calibration Module 1 Gen 2 Clock Complement

Connection, Purpose, Dependencies, Procedure, Parameters and Results

Same as Amplifier Level Calibration Module 1 Gen 1 Clock Normal on page 106.

Skew Calibration Module 2

Connection, Purpose, Dependencies, Procedure, Parameters and Results

Same as Skew Calibration Module 1 on page 104.

Amplifier Level Calibration Module 2 Gen 1 Data0 Normal

Connection, Purpose, Dependencies, Procedure, Parameters and Results

Same as Amplifier Level Calibration Module 1 Gen 1 Clock Normal on page 106.

Amplifier Level Calibration Module 2 Gen 2 Data0 Complement

Connection, Purpose, Dependencies, Procedure, Parameters and Results

Same as Amplifier Level Calibration Module 1 Gen 1 Clock Normal on page 106.

Inter module Skew Calibration

Connection

The following diagram illustrates the connection setting specifically for Inter Module Skew Calibration procedure using the M8195A AWG configuration, when two or more AWGs are connected.

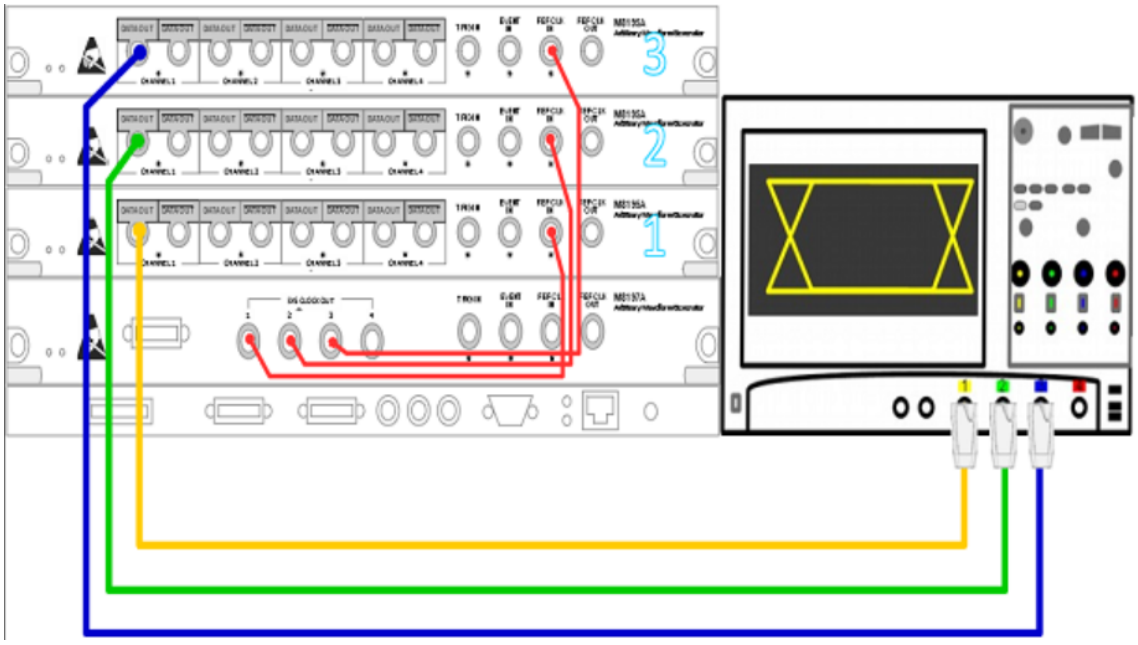


Figure 42 Connection Settings for Inter Module Skew Calibration

Purpose

It calibrates the skew among the modules of M8195A AWG. The modules of the M8195A AWG are aligned by the M8197A sync module and do not need an in-situ skew calibration. It requires only a static correction of the skew (that is, the cable skews need to be compensated).

Dependencies

This procedure does not depend on any other calibration. This calibration is required for all CTS tests. However, before conducting the test, the oscilloscope channels need to be de-skewed to avoid errors caused by the internal skew of the oscilloscope channels.

Procedure

At each module, the first channel normal data output signals are connected to the DSO channels (1 to 3) respectively with SMA cables. For this procedure, the skew must be calibrated with the values lesser than the Skew Tolerance value. At first, a clock (generally a step) pattern is generated at the first channel and the skew is adjusted for all other channels with respect to the first channel. The skew is measured and calibrated iteratively until its value is smaller than the given tolerance value.

Parameters

The parameters used for this calibration are listed alphabetically in Table 7.

Results

Table 10 Calibration data table "Inter module Skew"

Parameter name	Parameter description
Result	▪ Pass: it was possible to adjust the skew between lanes below the given tolerance. ▪ Fail: it was not possible to adjust the skew.
Skew Value [ps]	Skew value of the channel with respect to the first channel of the module.

LP Level Calibration Clock

Connection

Refer to Common Connection Diagram on page 104.

Purpose

This procedure calibrates the “LP-RX Logic 1 Input Voltage (V_OH)” and the “LP-RX Logic 0 Input Voltage, Non-ULP State (V_IL)” of the clock lane. This calibration should be run at all data lanes.

Dependencies

This calibration is required for the CTS test groups 2.1 and 2.2. It depends on the Amplifier Level calibration procedure.

Procedure

To start the calibration, follow the steps given below:

- Connect the normal and the complement data output signals of the lane that is being calibrated to the DSO channels 1 and channel 2 respectively, using N7010A probes.
- At first, the AWG generates an LP pattern and for this procedure, some LP high level values are set according to the specification range from the Max LP high level and decreased with a Step size value until the Min LP high value is reached.
- For each set LP high level value, a sweep performed at a range of the LP low level value starts from the Max LP low level and decreases with the Step Size value till the Min LP low level value is reached.
- Before doing the measurements, the signal is auto scaled so that a new trigger level is set based on the measured levels of the scaled signal. This is required in order to keep the signal stable during the measurement.
- At each step, the V_OH and V_OL values are measured at the normal and complement levels of the signal independently using an oscilloscope and at the same time, the set and measured values are stored.

Parameters

The parameters used for this calibration are listed alphabetically in Table 7.

Results

Table 11 Calibration data table "LP Low Level Calibration Clock"

Parameter name	Parameter description
Result	▪ Pass: the measured level is within the expected range of ±20% of the set level. ▪ Fail: the measured level deviates more than 20% from the set level.
Set High Level [mV]	Set amplitude value of the LP high level according to specification.
Measured Normal for LP Low Level [mV]	V_OH or V_OL amplitude value measured at the normal signal for the LP low level voltage.
Measured Complement for LP Low Level	V_OH or V_OL amplitude value measured at the complement signal for the Low LP low level voltage.

V_ILHS Calibration Clock

Connection

Refer to Common Connection Diagram on page 104.

Purpose

This procedure calibrates the "HS-RX Single-Ended Input Low Voltage (V_ILHS)" of the clock lane. This calibration procedure should be run at all data lanes.

Dependencies

This calibration is required for the CTS test groups 2.3 and 2.4, specially for Test 2.3.1 HS-RX Common Mode Voltage Tolerance (V_CMRX(DC)), Test 2.3.2 – HS-RX Differential Input High Threshold (V_IDTH), Test 2.3.3 – HS-RX Differential Input Low Threshold (V_IDTL), Test 2.3.4 – HS-RX Single-Ended Input High Voltage (V_IHHS) and Test 2.3.5 – HS-RX Single-Ended Input Low Voltage (V_ILHS).

It depends on the Amplifier Level Calibration procedure.

Procedure

Connect the normal and the complement data output signals of the lane that is being calibrated to the DSO channels 1 and 2 respectively, using N7010A probes. The procedure sets some V_ILHS values, starts with the "Max Level" and decreases it subsequently by the "Step Size" until the "Min Level" value is reached. At each set V_ILHS value, the actual V_ILHS value is measured independently at the normal and complement signals using a DSO and at the same time, all measured values are stored.

Parameters

The parameters used for this calibration are listed alphabetically in Table 7.

Results

Table 12 Calibration data table "V_ILHS Calibration Clock"

Parameter name	Parameter description
Result	▪ Pass: the measured level is within the expected range of ±20% of the set level. ▪ Fail: the measured level deviates more than ±20% from the set level.
Set Level [mV]	Set V_ILHS value
Measured Normal V_ILHS [mV]	Actual normal value as measured on channel 1 of the DSO using the most frequent value of a histogram measurement.
Measured Complement V_ILHS [mV]	Actual complement value as measured on channel 2 of the DSO using the most frequent value of a histogram measurement.

Differential Amplitude Cal Clock

Connection

Refer to Common Connection Diagram on page 104.

Purpose

This procedure calibrates the differential amplitude. This calibration procedure must be run for all data lanes.

Dependencies

This calibration is required for all CTS test groups.

It does not depend on other calibration procedures.

Procedure

Connect the normal and the complement data output signals of the lane being calibrated to the DSO channels 1 and 2 respectively, using N7010A probes. It sets some amplitude values with the Max Swing Value and decreases with the Step Size till the Min Swing Value is reached. At each Set Amplitude value, the normal and complement amplitude levels are measured and at the same time, the set and measured values are stored.

Parameters

The parameters used for this calibration are listed alphabetically in Table 7.

Results

Table 13 Calibration data table "Differential Amplitude Calibration"

Parameter name	Parameter description
Result	▪ Pass: the measured amplitude is within the expected range of ±20% of the set level. ▪ Fail: the measured amplitude deviates more than ±20% from the set level.
Set Amplitude [mV]	Set differential amplitude value.
Measured Normal Amplitude [mV]	Actual normal amplitude as measured on channel1 of the DSO using the most frequent value of a histogram measurement.
Measured Complement Amplitude [mV]	Actual complement amplitude as measured on channel 2 of the DSO using the most frequent value of a histogram measurement.
Measured Normal Low Level [mV]	Actual normal low level as measured on channel 1 of the DSO using the most frequent value of a histogram measurement.
Measured Complement Low Level [mV]	Actual complement low level as measured on channel 2 of the DSO using the most frequent value of a histogram measurement.

LP Level Calibration Data0

Connection, Purpose, Dependencies, Procedure, Parameters and Results

Same as LP Level Calibration Clock on page 110.

V_ILHS Calibration Data0

Connection, Purpose, Dependencies, Procedure, Parameters and Results

Same as V_ILHS Calibration Clock on page 111.

Differential Amplitude Cal Data0

Connection, Purpose, Dependencies, Procedure, Parameters and Results

Same as Differential Amplitude Cal Clock on page 112.

Calibration Small LP Amplitude

Connection Diagram for specific calibrations

The following diagram illustrates the connection settings for Jitter-based Calibration Small LP Amplitude procedures such as Intrinsic Jitter Calibration, Sinusoidal Jitter Calibration, Transition Time Cal, Rise Time - Eye Height Calibration, ISI Calibration, Eye Opening Calibration with Jitter and SSC Calibration, using the M8195A AWG configuration.

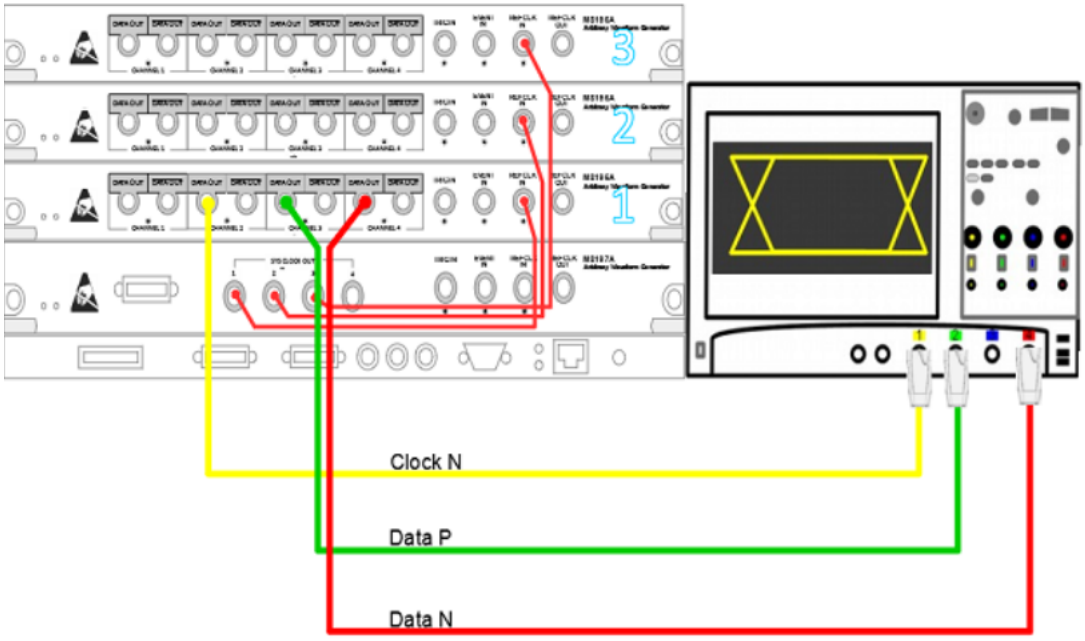


Figure 43 Connections for specific Calibration Small LP Amplitude procedures

Common Connection Diagram

The following diagrams illustrates the connection settings for certain Calibration Small LP Amplitude procedures using the M8195A AWG configuration.

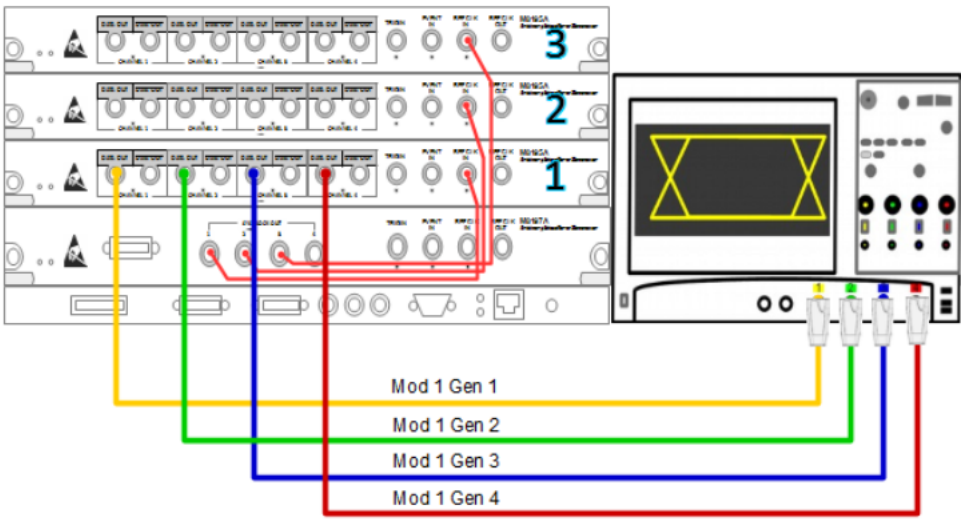


Figure 44 Connection Settings for most Calibration Small LP Amplitude procedures

LP Level Calibration Clock Small AWG Amplitude

Connection

Refer to the respective Common Connection Diagram on page 116.

Purpose

This procedure calibrates the “LP-RX Logic 1 Input Voltage (V_OH)” and the “LP-RX Logic 0 Input Voltage, Non-ULP State (V_IL)” of the clock lane. This calibration should be run at all data lanes.

Dependencies

This calibration is required for the CTS test groups 2.1 and 2.2.

Procedure

To start the calibration, follow the steps given below:

- Connect the normal and the complement data output signals of the lane that is being calibrated to the DSO channels 1 and channel 2 respectively, using N7010A probes.
- At first, the AWG generates an LP pattern and for this procedure, some LP high level values are set according to the specification range from the Max LP high level and decreased with a Step size value until the Min LP high value is reached.
- For each set LP high level value, a sweep performed at a range of the LP low level value starts from the Max LP low level and decreases with the Step Size value till the Min LP low level value is reached.
- Before doing the measurements, the signal is auto scaled so that a new trigger level is set based on the measured levels of the scaled signal. This is required in order to keep the signal stable during the measurement.
- At each step, the V_OH and V_OL values are measured at the normal and complement levels of the signal independently using an oscilloscope and at the same time, the set and measured values are stored.

Parameters

The parameters used for this calibration are listed alphabetically in Table 7.

Results

Table 14 Calibration data table "LP Level Calibration Clock Small AWG Amplitude"

Parameter name	Parameter description
Result	▪ Pass: the measured level is within the expected range of ±20% of the set level. ▪ Fail: the measured level deviates more than ±20% from the set level.
Set High Level [mV]	Set amplitude value of the LP high level according to specification.
Measured Normal for LP Low Level [mV]	V_OH or V_OL amplitude value measured at the normal signal for the LP low level voltage.
Measured Complement for LP Low Level	V_OH or V_OL amplitude value measured at the complement signal for the Low LP low level voltage.

V_ILHS Calibration Clock Small AWG Amplitude

Connection

Refer to the respective Common Connection Diagram on page 116.

Purpose

This procedure calibrates the “HS-RX Single-Ended Input Low Voltage (V_ILHS)” of the clock lane. This calibration procedure should be run at all data lanes.

Dependencies

This calibration is required for the CTS test groups 2.3 and 2.4, specially for Test 2.3.1 HS-RX Common Mode Voltage Tolerance (V_CMRX(DC)), Test 2.3.2 – HS-RX Differential Input High Threshold (V_IDTH), Test 2.3.3 – HS-RX Differential Input Low Threshold (V_IDTL), Test 2.3.4 – HS-RX Single-Ended Input High Voltage (V_IHHS) and Test 2.3.5 – HS-RX Single-Ended Input Low Voltage (V_ILHS).

Procedure

Connect the normal and the complement data output signals of the lane that is being calibrated to the DSO channels 1 and 2 respectively, using N7010A probes. The procedure sets some V_ILHS values, starts with the “Max Level” and decreases it subsequently by the “Step Size” until the “Min Level” value is reached. At each set V_ILHS value, the actual V_ILHS value is measured independently at the normal and complement signals using a DSO and at the same time, all measured values are stored.

Parameters

The parameters used for this calibration are listed alphabetically in Table 7.

Results

Table 15 Calibration data table "V_ILHS Calibration Clock Small AWG Amplitude"

Parameter name	Parameter description
Result	▪ Pass: the measured level is within the expected range of ±20% of the set level. ▪ Fail: the measured level deviates more than ±20% from the set level.
Set Level [mV]	Set V_ILHS value
Measured Normal V_ILHS [mV]	Actual normal value as measured on channel 1 of the DSO using the most frequent value of a histogram measurement.
Measured Complement V_ILHS [mV]	Actual complement value as measured on channel 2 of the DSO using the most frequent value of a histogram measurement.

Differential Amplitude Cal Clock Small AWG Amplitude

Connection

Refer to the respective Common Connection Diagram on page 116.

Purpose

This procedure calibrates the differential amplitude. This calibration procedure must be run for all data lanes.

Dependencies

This calibration is required for all CTS test groups.

It does not depend on other calibration procedures.

Procedure

Connect the normal and the complement data output signals of the lane being calibrated to the DSO channels 1 and 2 respectively, using N7010A probes. It sets some amplitude values with the Max Swing Value and decreases with the Step Size till the Min Swing Value is reached. At each Set Amplitude value, the normal and complement amplitude levels are measured and at the same time, the set and measured values are stored.

Parameters

The parameters used for this calibration are listed alphabetically in Table 7.

Results

Table 16 Calibration data table "Differential Amplitude Calibration"

Parameter name	Parameter description
Result	▪ Pass: the measured amplitude is within the expected range of ±20% of the set level. ▪ Fail: the measured amplitude deviates more than ±20% from the set level.
Set Amplitude [mV]	Set differential amplitude value.
Measured Normal Amplitude [mV]	Actual normal amplitude as measured on channel1 of the DSO using the most frequent value of a histogram measurement.
Measured Complement Amplitude [mV]	Actual complement amplitude as measured on channel 2 of the DSO using the most frequent value of a histogram measurement.
Measured Normal Low Level [mV]	Actual normal low level as measured on channel 1 of the DSO using the most frequent value of a histogram measurement.
Measured Complement Low Level [mV]	Actual complement low level as measured on channel 2 of the DSO using the most frequent value of a histogram measurement.

LP Level Calibration Data0 Small AWG Amplitude

Connection, Purpose, Dependencies, Procedure, Parameters and Results

Same as LP Level Calibration Clock Small AWG Amplitude on page 116.

V_ILHS Calibration Data0 Small AWG Amplitude

Connection, Purpose, Dependencies, Procedure, Parameters and Results

Same as V_ILHS Calibration Clock Small AWG Amplitude on page 118.

Differential Amplitude Cal Data0 Small AWG Amplitude

Connection, Purpose, Dependencies, Procedure, Parameters and Results

Same as Differential Amplitude Cal Clock Small AWG Amplitude on page 119.

Intrinsic Jitter Calibration

Connection

Refer to the respective Connection Diagram for specific calibrations on page 115.

Purpose

This procedure calibrates the intrinsic jitter amplitude.

Dependencies

This calibration is required for the CTS Test 2.3.8 – HS-RX Setup/Hold and Jitter Tolerance.

It does not depend on other calibration procedures.

Procedure

Connect the complement of the clock channel to the oscilloscope channel 1 and the normal and complement data outputs of the data lane to the 100 Ohm differential probe and probe to the oscilloscope channel 2. This procedure measures the intrinsic jitter.

Parameters

The parameters used for this calibration are listed alphabetically in Table 7.

Results

Table 17 Calibration data table "Intrinsic Jitter Calibration"

Parameter name	Parameter description
Result	▪ Pass: the measured jitter amplitude is within the expected range of ±20% of the set value. ▪ Fail: the measured jitter amplitude deviates more than ±20% from the set levels
Measured Jitter [mUI]	Measured value of the intrinsic jitter.

Transition Time Calibration

Connection

Refer to the respective Connection Diagram for specific calibrations on page 115.

Purpose

This procedure calibrates the transition time by measuring the effective rise time on the signal.

Dependencies

This calibration is required for the Eye Opening Calibration with Jitter. It does not depend on other calibration procedures.

Procedure

Sweep from the initial transition time to the maximum transition time. The step size is set uniformly. Measure effective rise time.

Parameters

The parameters used for this calibration are listed alphabetically in Table 7.

Results

Table 18 Calibration data table "Transition Time Calibration"

Parameter name	Parameter description
Result	▪ Pass: the measured rise time is within the expected range of ±20% of the set value of transition time. ▪ Fail: the measured rise time deviates more than ±20% from the set levels of transition time.
Set Transition Time [ps]	Set values of Transition Time uniformly divided between the Initial and Maximum transition times.
Measured Rise Time [ps]	Measured value of rise time.

Rise Time - Eye Height Calibration

Connection

Refer to the respective Connection Diagram for specific calibrations on page 115.

Purpose

This procedure calibrates the best HS transition time to get the maximum Eye Height. In faster transition times, there will be an implied amount of DCD which affects the related tests. The goal is to find a transition time which results in a bigger eye and lesser implied impairments.

Dependencies

This calibration is required for Test 2.3.2 and before this calibration Transition Time Calibration should be run. It depends on the HS data rate.

Procedure

This calibration runs in Small LP Amplitude group. The procedure searches the best HS transition time and can be performed in two different modes.

- **Linear**: In this mode, the calibration procedure starts from the minimum transition time and measures the eye height of the generated signal and also the amount of impairments. These results are stored in the report. Then, the transition time is increased by Transition Time Step. The eye height of generated signal is measured again. This process continues until either the maximum transition time is attained or the measured eye height is less than the 75% of the eye height target.
- **BinarySearch**: Initially, the Minimum Transition Time is applied and the eye height is measured. Then, the Maximum Transition Time is applied and eye height is measured again. After the second measurement, the middle value of transition time is applied. Using the BinarySearch approach, the procedure tries to find the best transition time that results in a bigger eye height. This approach is continued until the difference of higher limit and lower limit of the binary search approach is equal or less than the Transition Time step.

Only the best transition time values are written into the results table. The best transition time is the one which gives an eye height greater or equal to the eye height target with less impairment (implied DCD).

Parameters

The parameters used for this calibration are listed alphabetically in Table 7.

Results

Table 19 Calibration data table "Rise Time - Eye Height Calibration"

Parameter name	Parameter description
Result	▪ Pass: if the best rise time is found. ▪ Fail: if none of the measured eye height values are greater than 75% of the eye height target.
Set Transition Time [ps]	Set value of the transition time, which results in the best eye height.
Measured Eye height [mV]	Measured value of eye height for the corresponding transition time.
Measured Impairments [mUI]	Measured impairments, which are mostly the implied DCD when higher data rates are applied.

ISI Calibration

Connection

Refer to the respective Connection Diagram for specific calibrations on page 115.

Purpose

This procedure calibrates the Inter Symbol Interference on the signal.

Dependencies

This calibration is required for the "Eye Opening with Jitter Calibration" but it does not depend on other calibration procedures.

Procedure

Measure ISI for each TX equalization value defined in the Reference Channel S-Parameter (*s4p*) file.

Parameters

The parameters used for this calibration are listed alphabetically in Table 7.

Results

Table 20 Calibration data table "ISI Calibration"

Parameter name	Parameter description
Result	▪ Pass: the measured ISI values must be within ±20% from the values found in the S-Parameter file. ▪ Fail: the measured ISI values deviates more than ±20% from the values found in the S-Parameter file.
Set Tx EQ [dB]	Set values of Transmitter Equalization.
Measured ISI [mUI]	Measured value of ISI.

Eye Opening Calibration with Jitter (for HS Data Rate > 1500 MB/s and < 2500 MB/s)

This Eye Opening Calibration with Jitter is applicable only for data rates greater than 1500 MBits/s and less than 2500 MBits/s.

Connection

Refer to the respective Connection Diagram for specific calibrations on page 115.

Purpose

This procedure calibrates the eye height and eye-width.

Dependencies

This calibration is required for Test 2.3.8.2 Jitter and Eye Diagram Tolerance for Data Rates from 1.5Gbps to 2.5Gbps Data.

Ensure that the Sinusoidal Jitter Calibration, all Skew calibrations and all Level Calibrations have been performed before the actual test starts.

Set the transition time to 0.4 UI. This is calibrated in procedure, "Transition Time Calibration <data rate>". Then, apply an ISI of 0.2 UI. The ISI is calibrated by "ISI Calibration <data rate>", which calibrates the required TX-equalization.

This calibration is dependent on the HS data rate and you must repeat this calibration for all data rates.

Procedure

For the Eye-Width calibration, the amount of sinusoidal jitter that is required to close the eye to the specified eye width is obtained. At first, it measures the eye-width and checks whether it is in the specified variation limits. If not, the sinusoidal jitter is adjusted till the Eye Width Target is reached. For the Eye-Height calibration, the default differential voltage is applied and the eye-height is measured. Then, the differential voltage is reduced by 20% and applied and the eye-height is the measurement is done. This method is repeated till the Eye-Height Target is reached. At each measurement, all the values are stored. This procedure needs to be run again when a different HS data rate is selected.

Parameters

The parameters used for this calibration are listed alphabetically Table 7.

Results

Table 21 Calibration data table "Eye Opening Calibration with Jitter (>1500MB/s & <2500MB/s)"

Parameter name	Parameter description
Result	▪ Pass: it was possible to close the eye to the required specification. ▪ Fail: it was not possible to close the eye to the required specification.
SJ Frequency (MHz)	Applied value of the sinusoidal jitter.
SJ Amplitude (UI)	Applied SJ amplitude value to close the eye having eye-width between 500 mUI and 525 mUI.
Eye Width (mUI)	Measured eye-width value.

Eye Opening Calibration with Jitter (for HS Data Rate > 2500 MB/s and < 4500 MB/s)

This Eye Opening Calibration with Jitter is applicable for data rate ranges greater than 2500 MBits/s and less than 4500 MBits/s.

Connection

Refer to the respective Connection Diagram for specific calibrations on page 115.

Purpose

This procedure calibrates the eye height and eye-width.

Dependencies

Test 2.3.8.3 Jitter and Eye Diagram Tolerance for Data Rates from upper 2.5Gbps to 4.5Gbps Data.

You must run the Skew, LP Level Small AWG Amplitude calibrations, HS Level calibrations, Transition Time calibration and ISI calibration before running this calibration.

The transition time is set to 0.4 UI. This is calibrated in this procedure, “Transition Time Calibration <data rate>”. Then, an ISI of 0.2 UI is applied. The ISI is calibrated in the procedure “ISI Calibration <data rate>”, which also calibrates the required TX-equalization.

The amount of Sinusoidal Jitter that is required to close the eye to the specified eye width is obtained by performing the “Eye Width Calibration”. In the last step, the “Eye Height Calibration” is performed by changing V_OD of the HS signal to achieve the required eye height.

This calibration is dependent on the HS data rate and you must repeat this calibration for all data rates.

Procedure

Apply a transition time of 0.4 UI (80% -20%). Next, apply ISI via the selected reference channel model, and adapt the TX-Equalization to reach 0.8 UI of eye opening, measured by a horizontal histogram. If the channel, which was selected in the Configuration panel, is not applying enough ISI to reach 0.2 UI, a warning is prompted to inform the operator.

The Sinusoidal Jitter (SJ) is applied with a frequency, whose value is the data rate divided by ten so that an eye opening of 0.50 UI is attained. For characterization, a sweep of SJ amplitudes is performed and the eye opening is measured for each amplitude of SJ. At the end of this sweep,

the SJ is set so that an eye opening of 0.5 UI is achieved. Since the system has a very low Random Jitter, it is not required to target for the prorated eye of 0.53 UI.

Next, the calibration of the eye height is started. A Differential voltage of 200mV is applied and the eye height is measured by a vertical histogram. If the target eye height cannot be achieved with the nominal amplitude of 200mV, another trace is required in that case. Both top and bottom measurements of eye height are performed and the limits of the histograms are used for measurements at the center of the eye. This procedure is repeated by reducing the differential input voltage until an eye opening below the target value is attained.

Eye Opening calibration depends on the HS Frequency. It needs to be run for each HS Frequency selected.

Parameters

The parameters used for this calibration are listed alphabetically in Table 7.

Results

Table 22 Calibration data table "Eye Opening Calibration with Jitter (>2500MB/s & <4500MB/s)"

Parameter name	Parameter description
Result	▪ Pass: it was possible to close the eye to the required specification. ▪ Fail: it was not possible to close the eye to the required specification.
SJ Frequency (MHz)	Frequency of the applied sinusoidal jitter.
SJ Amplitude (UI)	Applied SJ required to close the eye with an eye width between 500 mUI and 525 mUI (assuming that the maximum deviation of the eye width is 5%).
Eye Width (mUI)	Measured eye width of the closed eye.

Calibration Data File

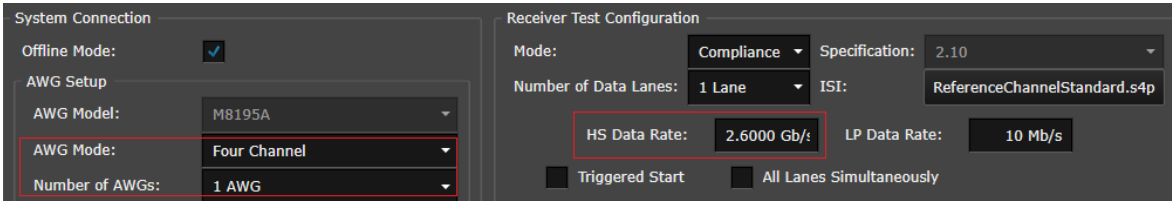
The calibration files generated during this calibration are:

- *EyeOpeningCalibrationJitterData0.txt* (Eye Width calibration)
- *EyeOpeningCalibrationVoltageData0.txt* (Eye Height calibration)

SSC Calibration

The SSC Calibration is available only when the following conditions are met in the Configuration panel of the M8085A MIPI D-PHY CTS plug-in:

- AWG Mode must be set to Four Channel
- Number of AWGs must be set to 1 AWG
- HS Data Rate must be set to a value greater than 2.5 GB/s



Connection

Refer to the respective Connection Diagram for specific calibrations on page 115.

Purpose

This procedure calibrates the SSC deviation and slope. The slope is calibrated by an SJ component at 1 MHz. By increasing the SJ amplitude, the SSC slope increases.

Dependencies

No other calibration is required.

Procedure

The MIPI D-PHY CTS plug-in creates a continuous clock pattern using the AWG.

The oscilloscope is configured to measure the measurement trend of the period including a low pass filter by averaging over a range of measurement points. The number of points depend on the SSC frequency and the sample rate of the oscilloscope. This process results in the SSC measurement. Then, an additional derivative is calculated to gain the SSC rate changes.

The SJ amplitude is modified and the resulting maximum and minimum slope values are measured.

Parameters

The parameters used for this calibration are listed alphabetically in Table 7.

Results

Table 23 Calibration data table "SSC Calibration (>2500 MBits/s)"

Parameter name	Parameter description
Result	▪ Pass: it was possible to close the eye to the required specification. ▪ Fail: it was not possible to close the eye to the required specification.
SSC Derivative (ppm/us)	Measured derivative of the SSC
SJ Amplitude (UI)	Applied SJ required to close the eye with an eye width between 500 mUI and 525 mUI (assuming that the maximum deviation of the eye width is 5%).

Calibration Data File

The calibration files generated during this calibration are:

- *SscCalibration.txt*
- *EyeOpeningCalibrationVoltageData0.txt* (Eye Height calibration)

5 Test Procedures

Connection Diagrams for the Test Procedures / 132
Clock Tests / 134
Data Tests / 160
Semi-Automated Tests / 191
LP Tests / 194
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The MIPI D-PHY receiver tests comprise of the following test groups:

- Clock
- Data
- Semi-Automated Tests
- LP Tests
- Behavioral Tests

This grouping streamlines the test process by minimizing the number of physical reconnection of cables and other test accessories.

Connection Diagrams for the Test Procedures

The following diagrams illustrate the connection settings, which is common for all Test Procedures:

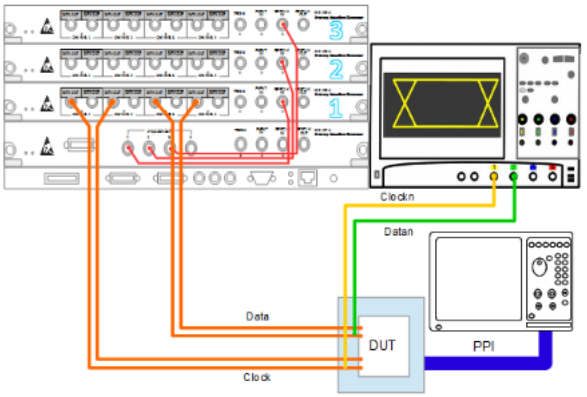

Figure 45 M8195A single module connection setup

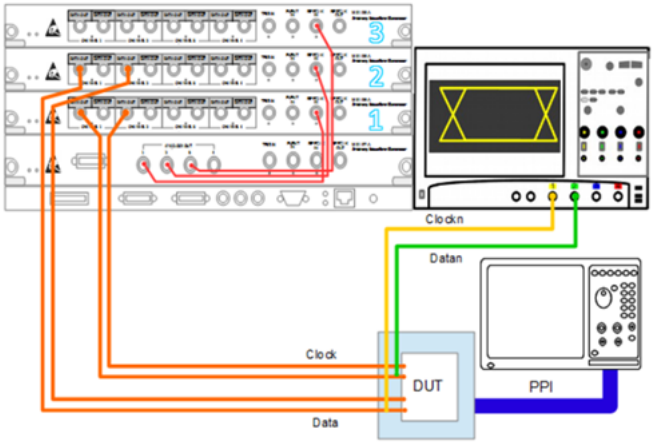

Figure 46 M8195A multi module connection setup

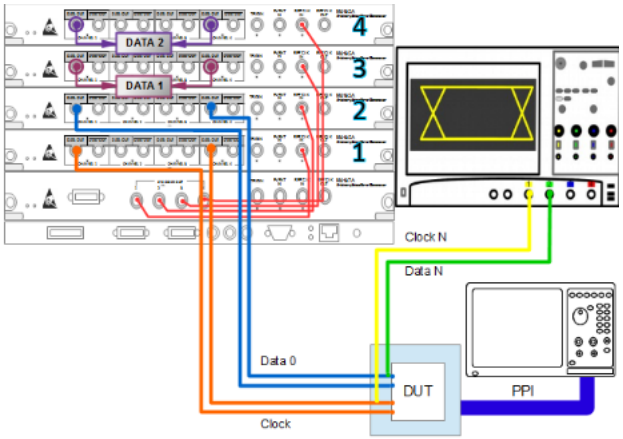

Figure 47 M8195A Dual-Channel mode connection setup

Each test can be performed in two modes: **Compliance** and **Expert Mode**. (Refer to Configuration Window on page 20). While the Compliance mode has pre-defined optimal values for the test parameters that cannot be modified; the Expert Mode allows you to customize values or limits for the parameters, only if required, so that you may analyze the behavior and limitations of a test. By default, the field for each parameter displays the values/limits from the CTS. If needed, edit the parameter values/limits to those supported by your DUT, which may be less than or beyond the CTS limits.

In Compliance and in the Expert Mode, follow the steps given below, which are common to all test procedures under the test groups—Clock, Data, Semi-Automated Tests and LP Tests:

- Make the connections for the selected test procedure as per the connection diagram shown in Figure 45, Figure 46 and Figure 47 for M8195A AWG.
- Click Run to transmit the test sequence to the DUT. Refer to Performing Procedures on page 31 to know how to run procedures.
- From the Results Table, verify that the DUT received the test sequence without errors.

For the remaining test groups, some of the tests additionally require some manual steps to be performed, which have been described in the respective sections.

Clock Tests

Test 2.3.1 Vcmrx Tolerance Clock

CTS Test Number and Name

Test 2.3.1 HS-RX Common Mode Voltage Tolerance (V_CMRX(DC))

Purpose

To verify that the DUT's HS receiver can successfully receive signals with common-mode voltage levels (V_CMRX (DC)) within the conformance limits.

Dependencies

For this test, run the following Calibration procedures as a prerequisite. (Refer to Performing Procedures on page 31 to know how to run procedures).

- High Speed Level (V_ILHS) Calibration
- Skew Calibration
- Skew Calibration Module 1
- Skew Calibration Module 2
- Amplifier Level Calibration
- Amplifier Level Calibration Module 1
- Amplifier Level Calibration Module 2
- Inter Module Skew Calibration
- V_ILHS Calibration Clock

Parameters

Table 24 Parameters used in Test 2.3.1 Vcmrx Tolerance Clock

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Maximum Tested value	Maximum common mode levels represented as V_CMRX.
Minimum Tested value	Minimum common mode levels V_CMRX.

Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
V_OD Array	HS transmission differential voltage array. The first value indicates the differential voltage amplitude and the second value (1 or -1) indicates the polarity 1.

Results

The DUT must receive all the test sequences for the maximum and the minimum common mode voltage without errors.

Table 25 Parameters in the result data table for "Test 2.3.1 Vcmrx Tolerance Clock"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence for all test cases. ▪ Fail: one or more test cases failed.
V_OD [mV]	Tested V_OD for this Step.
Min Passed V_CMRX [mV]	Minimum passed V_CMRX between all test cases.
Min Tested V_CMRX [mV]	Minimum V_CMRX tested so far.
Min Spec V_CMRX [mV]	Minimum V_CMRX according to specification.
Max Passed V_CMRX [mV]	Maximum passed V_CMRX between all test cases.
Max Tested V_CMRX [mV]	Maximum V_CMRX tested so far.
Max Spec V_CMRX [mV]	Maximum V_CMRX according to specification.

Test 2.3.2 V_IDTH and Test 2.3.3 V_IDTL Sensitivity Clock

CTS Test Number and Name

Test 2.3.2 – HS-RX Differential Input High Threshold (V_IDTH)

Test 2.3.3 – HS-RX Differential Input Low Threshold (V_IDTL)

Purpose

To verify that the DUT's HS receiver can properly detect HS-1 voltage levels that are at least as small as the minimum required value (V_IDTH) and HS-0 voltage levels that are at least as small as the minimum required value (V_IDTL).

Dependencies

Ensure that the Skew Calibration procedure, Inter Module Skew Calibration and V_ILHS Calibration Clock have been performed before the actual test starts. If these Calibration procedures have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

Parameters

Table 26 Parameters used in Test 2.3.2 V_IDTH and Test 2.3.3 V_IDTL Sensitivity Clock

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Maximum Tested value	Maximum common mode levels represented as V_CMRX.
Minimum Tested value	Minimum common mode levels.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Steps	Specifies the number of steps that are tested between the Start Value and the End Value for tests in which a range of values is tested.
V_CMTX	HS transmit static common-mode voltage. The common-mode voltage VCMTX is defined as the arithmetic mean value of the voltages at the Dp and Dn pins.

Results

- For DUTs supporting <= 1.5 Gbps, V_IDTH/V_IDTL must be less/greater than or equal to 70 mV/-70 mV.
- For DUTs supporting > 1.5 Gbps, V_IDTH/V_IDTL must be less/greater than or equal to 40 mV/-40 mV.

Table 27 Parameters in the result table for "Test 2.3.2 V_IDTH and Test 2.3.3 V_IDTL Sensitivity Clock"

Parameter name	Parameter description
Result	▪ Pass: the DUT's V_IDTH and V_IDTL minimum values conform to the specification. ▪ Fail: the DUT was not able to receive the test sequence with V_IDTH and V_IDTL values within the specification.
V_OD [mV]	Differential voltage used during the test.
V_CM [mV]	Common-mode level used during the test.
Min Passed V_IDTH/V_IDTL [mV]	Minimum value of V_IDTH and V_IDTL for which the DUT passed the test.
Min Tested V_IDTH/V_IDTL [mV]	Minimum value tested for V_IDTH and V_IDTL.
Min Spec V_IDTH/V_IDTL [mV]	Minimum value of V_IDTH and V_IDTL according to the specification.

Test 2.3.4 V_IHHS Sensitivity Clock

CTS Test Number and Name

Test 2.3.4 – HS-RX Single-Ended Input High Voltage (V_IHHS)

Purpose

To verify that the DUT's HS receiver is able to successfully receive HS signals with the maximum required single-ended voltage levels (V_IHHS). For details, see the CTS.

Dependencies

Ensure that the Skew Calibration procedure, Inter Module Skew Calibration and V_ILHS Calibration Clock have been performed before the actual test starts. If these Calibration procedures have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

Parameters

Table 28 Parameters used in Test 2.3.4 V_IHHS Sensitivity Clock

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Max Single Ended Voltage	For this test, a high-speed signal is sent to the DUT whose amplitudes are specifically chosen such that the TX V_OHHS single-ended levels are at the maximum RX V_IHHS limit of 460mV It can be calculated as (Common mode Voltage+(maximum allowed TX differential voltage/4)) i.e. 325+(540/4) = 460.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Steps	Specifies the number of steps that are tested between the Start Value and the End Value for tests in which a range of values is tested.

Results

The DUT must receive the test sequence without errors.

Table 29 Parameters in the result table for "Test 2.3.4 V_IHHS Sensitivity Clock"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors for V_IHHS values within the specification. ▪ Fail: the DUT failed to receive the test sequence.
V_OD [mV]	Differential voltage used during the test.
V_CM [mV]	The common-mode level used during the test.
Max Passed V_IHHS [mV]	Maximum value of V_IHHS for which the DUT passed the test.
Max Tested V_IHHS [mV]	Maximum value tested for V_IHHS.
Max Value V_IHHS	Maximum value of V_IHHS according to the specification.

Test 2.3.5 V_ILHS Sensitivity Clock

CTS Test Number and Name

Test 2.3.5 – HS-RX Single-Ended Input Low Voltage (V_ILHS).

Purpose

To verify that the DUT's HS receiver is able to successfully receive HS signals with the minimum required single-ended voltage levels (V_ILHS).

Dependencies

Ensure that the Skew Calibration procedure, Inter Module Skew Calibration and V_ILHS Calibration Clock have been performed before the actual test starts. If these Calibration procedures have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

Parameters

Table 30 Parameters used in Test 2.3.5 V_ILHS Sensitivity Clock

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Min Single Ended Voltage	For this test, a high-speed signal is sent to the DUT whose amplitudes are specifically chosen such that the TX V_OLHS single-ended levels are at the maximum RX V_ILHS limit of -40mV. It can be calculated as (Minimum Common Mode Voltage-(maximum allowed TX differential voltage/4)) i.e.95-(540/4) = -40.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Steps	Specifies the number of steps that are tested between the Start Value and the End Value for tests in which a range of values is tested.

Results

The DUT must receive the test sequence without errors.

Table 31 Parameters in the result table for "Test 2.3.5 V_ILHS Sensitivity Clock"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors for V_ILHS values within the specification. ▪ Fail: the DUT failed to receive the test sequence.
V_OD [mV]	Differential voltage used during the test.
V_CM [mV]	Common-mode level used during the test.
Min Passed V_ILHS [mV]	Maximum value of V_ILHS for which the DUT passed the test.
Min Spec V_ILHS[mV]	Maximum value tested for V_ILHS.

Test 2.3.6 HS RX CM Interference 50-450 MHz Clock

CTS Test Number and Name

Test 2.3.6 – HS-RX Common-Mode Interference 50 MHz – 450 MHz (ΔVCMRX(LF))

Purpose

To verify that the DUT's HS receiver is capable of tolerating worst-case common-mode interference for frequencies between 50 - 450 MHz, with amplitudes as high as the maximum required limit (ΔV_CMRX (LF)).

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

NOTE

For this test, the software automatically generates a peak voltage of 50 mVpk for DUTs supporting <= 1.5 Gbps. Similarly, it generates 25 mVpk for DUTs supporting > 1.5Gbps.

To change the value for HS data rate, refer to Configuration on page 21.

Parameters

Table 32 Parameters used in Test 2.3.6 HS RX CM Interference 50-450 MHz Clock

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
Frequency Range	Range of frequencies used in a calibration or test procedure.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Maximum Test Voltage	ΔV_CMRX (LF), Maximum Common-mode interference for 50 MHz – 450 MHz.
Minimum Test Voltage	ΔV_CMRX (LF), Minimum Common-mode interference for 50MHz – 450 MHz.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Steps	Specifies the number of steps that are tested between the Start Value and the End Value for tests in which a range of values is tested.
V_CMRX; V_OD	V_CMRX is the common-mode voltage HS receive mode; V_OD is defined as the difference of the voltages V_DP and V_DN at the Dp and Dn pins respectively.

Results

The DUT must receive the test sequence without errors.

Table 33 Parameters in the result table for "Test 2.3.6 HS RX CM Interference 50-450 MHz Clock"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors for V_ILHS values within the specification. ▪ Fail: the DUT failed to receive the test sequence.
V_CMRX [mV]	Common-mode voltage level used during this test step.
V_OD [mV]	Differential voltage level used during this test step.
Interference Frequency [MHz]	Interference frequency used during this test step.
Max Passed [mV]	Maximum interference amplitude for which the DUT was able to receive the test sequence without errors for the given common-mode and differential voltage levels.
Max Spec [mV]	Maximum interference amplitude for which the DUT must be able to receive the test sequence without errors for the given common-mode and differential voltage levels according to the specification.

Test 2.3.7 HS RX CM Interference beyond 450 MHz Clock

CTS Test Number and Name

Test 2.3.7 – HS-RX Common-Mode Interference Beyond 450 MHz (ΔVCMRX(HF))

Purpose

To verify that the DUT's HS receiver is capable of tolerating worst-case common-mode interference for frequencies greater than 450 MHz, with amplitudes as high as the maximum required limit (ΔV_CMRX (HF).

Dependencies

Ensure that Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

NOTE

For this test, the software automatically generates a peak voltage of 100 mVpk for DUTs supporting <= 1.5 Gbps. Similarly, it generates 50 mVpk for DUTs supporting > 1.5 Gbps.

To change the value for HS data rate, refer to Configuration on page 21.

Parameters

Table 34 Parameters used in Test 2.3.7 HS RX CM Interference beyond 450 MHz Clock

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
Frequency Range	Range of frequencies used in a calibration or test procedure.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Maximum Test Voltage	ΔV_CMRX (HF), Maximum Common-mode interference beyond 450MHz.
Minimum Test Voltage	ΔV_CMRX (HF), Maximum Common-mode interference beyond 450MHz.
Offline	Offline Mode.

Setup file name	The PPI BER Reader searches for a file name with the extension Setup.ala in the directory.
Steps	Specifies the number of steps that are tested between the Start Value and the End Value for tests in which a range of values is tested.
V_CMRX; V_OD	V_CMRX is the common-mode voltage HS receive mode; V_OD is defined as the difference of the voltages V_DP and V_DN at the Dp and Dn pins respectively.

Results

For all Lanes the DUT must receive the test sequence without errors.

Table 35 Parameters in the result table for "Test 2.3.7 HS RX CM Interference beyond 450 MHz Clock"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors for V_ILHS values within the specification. ▪ Fail: the DUT failed to receive the test sequence.
V_CMRX [mV]	Common-mode voltage level used during this test step.
V_OD [mV]	Differential voltage level used during this test step.
Interference Frequency [MHz]	Interference frequency used during this test step.
Max Passed [mV]	Maximum interference amplitude for which the DUT was able to receive the test sequence without errors for the given common-mode and differential voltage levels.
Max Spec [mV]	Maximum interference amplitude for which the DUT must be able to receive the test sequence without errors for the given common-mode and differential voltage levels according to the specification.

Test 2.3.8.1 HS-RX Skew-Amplitude Test for Data Rates 1.5Gbps and lower Clock

NOTE This test is available only for DUTs operating at HS rates < 1.5Gbps.

CTS Test Number and Name

Test 2.3.8 – HS-RX Setup/Hold and Jitter Tolerance

Purpose

To verify that the DUT can tolerate signals with worst-case timing error between the Clock and Data Skew signals.

Dependencies

Ensure that all the Calibration procedures have been performed before the actual test starts. For the value of the intrinsic jitter test parameter a particular result of the jitter calibration procedure is used. It is the jitter measured when no external jitter was injected, that is, the jitter inherent in the test setup.

Parameters

Table 36 Parameters used in Test 2.3.8.1 HS-RX Skew-Amplitude Test for Data Rates 1.5Gbps and lower Clock

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
BER Reader for Init String	Sets the Initialization string for the Clock in the bit-error-ratio reader.
Binary Search	If this parameter is set to false, then the skew will be swept first with the “Initial Step Size”. As soon as the first point is detected, at which the BER is above the given limit, the sweep ends. If this parameter is set to, true “Initial Step Size” is used until the fail point. The skew value is then reduced by half of the initial step size and, according to the binary search algorithm, increased or decreased depending on the BER result. For each step the step size is divided by 2 until “Min. Step Size” is reached.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Initial Skew Deviation	Allows to save time by starting the test with a Clock to Data Skew different to 0.5UI. The test range will be from 0.5 UI + Initial Skew Deviation to 1 UI and from -0.5 UI - Initial Skew Deviation to -1 UI.
Initial Step Size	This is the initial skew step size used in this test. If “Binary Search” is set to true, the skew will be increased for the T_HOLD verification and decreased for T-SETUP with this step size. After the first fail point, the initial step size is divided by a factor of two until the “Minimum Step Size” is reached. If “Binary Search” is set to false, the step size will be kept constant.
Intrinsic Jitter	This parameter allows the influence of the test setup on the pass/fail criteria to be removed. Since the specification limits are given at the pins of the RX and the eye may already be closed by ISI and other jitter components, half of the intrinsic jitter needs to be added to the setup and hold time. The default value is taken from the jitter calibration. If the jitter calibration was not conducted with the board used during the test, the intrinsic jitter value can be modified.
Maximum Tested Skew	Maximum tolerable skew between data and clock edges.
Min. Step Size	This is the minimum skew step size used with “Binary Search” set to true.
Offline	Offline Mode.
Transition Time	Transition time required to perform Rise Time calibration. Ensure to set the same value for all dependent tests.

V_CMTX max	Maximum HS transmit static common-mode voltage. The common-mode voltage VCMTX is defined as the value of the voltages at the Dp and Dn pins.
V_CMTX min	Minimum HS transmit static common-mode voltage. The common-mode voltage VCMTX is defined as the value of the voltages at the Dp and Dn pins.
V_OD	The value of differential output voltage V_OD which is defined as the difference of the voltages V_DP and V_DN at the Dp and Dn pins, respectively.

Results

The DUT must receive zero errors.

Table 37 Parameters in the result table for "Test 2.3.8.1 HS-RX Skew-Amplitude Test for Data Rates 1.5Gbps and lower Clock"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors. ▪ Fail: the DUT failed to receive the test sequence.
Skew Type	Type of skew used during the test are: Hold: Skew T_Hold Setup: Skew T_Setup Eye Opening: Skew T_Hold and T_Setup
VCMTX [mV]	HS transmit static common-mode voltage.
Max Passed [UI]	Maximum Skew value tested so far that did not prevent the DUT from receiving the test sequence.
Max Tested [UI]	Maximum tested Skew.
Max Spec [UI]	Maximum Skew that the DUT should be able to handle according to the specification.
Resulting minimum T_hold/T_setup [UI]	Minimum Skew that the DUT attained in its Hold or Setup states.
Comment	Displays information relevant to the tests.

Test 2.4.7 T_Clk-Prepare-Zero Compliance Procedure

CTS Test Number and Name

Test 2.4.7 – Clock Lane HS-RX T_CLK-PREPARE + T_CLK-ZERO Tolerance

Purpose

To verify that the DUT's Clock Lane HS receiver can tolerate receiving value for T_CLK-PREPARE+T_CLK-ZERO that conform to the specification.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

Parameters

Table 38 Parameters used in Test 2.4.7 T_Clk-Prepare-Zero Compliance Procedure

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
T-Clk-Post	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of T_HS-Trail to the beginning of T_Clk-Trail.
T-Clk-Pre	Time that the HS clock will be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.
T-Clk/HS Trail	This parameter has two meanings: ▪ During Clock Timing tests such as the "HS-RX Clock Tests", it is used for T_Clk-Trail, the time that the transmitter drives the HS-0 state after last payload data bit of a HS transmission burst. ▪ During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Trail, the corresponding time for the Data Lane(s).
T- Prepare; T- Prepare -Zero	▪ T- Prepare is the time that the HS clock will be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. ▪ T- Prepare –Zero is the time taken for the transmitter to drive HS -0 state prior to transmitting a sync sequence.

Results

The DUT must receive zero errors.

Table 39 Parameters in the result table for "Test 2.4.7 T_Clk-Prepare-Zero Compliance Procedure"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence for the given T_CLK-PREPARE + T_CLK-ZERO combination. ▪ Fail: the DUT failed to receive the test sequence.
T_Clk-Prepare [ns]	T_CLK-PREPARE used for this test step.
T_Clk-Zero [ns]	T_CLK-ZERO used for this test step.
T_Clk-Prepare+Zero [ns]	Total T_CLK-PREPARE + T_CLK-ZERO used for this test step.

Test 2.4.7a T_Clk-Prepare - Clock Procedure

CTS Test Number and Name

Test 2.4.7a T_Clk-Prepare - Clock Procedure

This test is provided additionally for product characterization. It is based on the CTS test 2.4.7.

Purpose

To characterize the DUT's Clock Lane HS receiver tolerance for T_CLK-PREPARE timing deviations.

Dependencies

This test is available in Expert Mode only.

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

Parameters

Table 40 Parameters used in Test 2.4.7a T_Clk-Prepare - Clock Procedure

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
End Value	For tests in which a range of values is tested; specifies the last value that is tested.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Start Value	Specifies the first value that is tested for tests in which a range of values is tested.
Steps	Specifies the number of steps that are tested between the Start Value and the End Value for tests in which a range of values is tested.
T-Clk-Post	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of T_HS-Trail to the beginning of T_Clk-Trail.

T-Clk-Pre	Time that the transmitter will drive the HS clock prior to any associated Data Lane beginning the transition from LP to HS mode.
T-Clk/HS Prepare	This parameter has two meanings: ▪ During Clock Timing tests such as the "HS-RX Clock Tests", it is used for T_Clk-Prepare, the time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. ▪ During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Prepare, the time specified for the Data Lane(s).
T-Clk/HS Prepare + Clk/HS-Zero	This parameter has two meanings: ▪ During Clock Timing tests such as the "HS-RX Clock Tests", it is used for T_Clk-Prepare + T_Clk_Zero (T_Clk-Prepare plus time that the transmitter drives the HS-0 state prior to starting the Clock). ▪ During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Prepare + T_Clk_Zero as specified for the Data Lane(s).
T-Clk/HS Trail	This parameter has two meanings: ▪ During Clock Timing tests such as the "HS-RX Clock Tests", it is used for T_Clk-Trail, the time that the transmitter drives the HS-0 state after last payload data bit of a HS transmission burst. ▪ During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Trail, the corresponding time for the Data Lane(s).

Results

The DUT must receive zero errors.

Table 41 Parameters in the result table for "Test 2.4.7a T_Clk-Prepare Clock Procedure"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence for the given T_CLK-PREPARE + T_CLK-ZERO combination. ▪ Fail: the DUT failed to receive the test sequence.
Parameter	Tested timing parameter.
Min Passed [ns]	Minimum T_CLK-PREPARE value for which the DUT passed the test.
Min Spec [ns]	Minimum T_CLK-PREPARE value according to the specification.
Max Passed [ns]	Maximum T_CLK-PREPARE value for which the DUT passed the test.
Max Spec [ns]	Maximum T_CLK-PREPARE value according to the specification.

Test 2.4.7b T_Clk-Prepare_Zero - Clock Procedure

CTS Test Number and Name

Test 2.4.7 T_Clk-Prepare_Zero - Clock Procedure

This test is provided additionally for product characterization. It is based on the CTS test 2.4.7.

Purpose

To characterize the DUT's Clock Lane HS receiver tolerance for T_CLK-PREPARE + T_CLK-ZERO timing deviations.

Dependencies

This test is available in Expert Mode only.

Ensure that Skew Calibration procedure and Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

Parameters

Same as Test 2.4.7a T_Clk-Prepare - Clock Procedure on page 148.

Results

The DUT must receive zero errors.

Table 42 Parameters in the result data table for "Test 2.4.7b T_Clk-Prepare_ Zero - Clock Procedure"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence for the given T_CLK-PREPARE + T_CLK-ZERO combination. ▪ Fail: the DUT failed to receive the test sequence.
T_Clk-Prepare [ns]	Tested T_CLK-PREPARE value.
T_Clk-Zero [ns]	Tested T_CLK -ZERO value.
Parameter	Tested timing parameters.
Min Passed [ns]	Minimum T_CLK-PREPARE + T_CLK -ZERO value for which the DUT passed the test.

Min Spec [ns]	Minimum T_CLK-PREPARE + T_CLK -ZERO value according to the specification.
Max Passed [ns]	Maximum T_CLK-PREPARE + T_CLK -ZERO value for which the DUT passed the test.
Max Spec [ns]	Maximum T_CLK-PREPARE + T_CLK -ZERO value according to the specification.

Test 2.4.8 T_Clock- Settle - Clock Procedure

CTS Test Number and Name

Test 2.4.8 – Clock Lane HS-RX TCLK-SETTLE Value

Purpose

To verify that the DUT's Clock Lane receiver incorporates a sufficient time out interval (T_CLK-SETTLE) to ignore transition effects that may occur during the HS Entry sequence.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

Parameters

Table 43 Parameters used in Test 2.4.8 T_Clock- Settle - Clock Procedure

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
Binary Search	If this parameter is set to false, then the skew will be swept first with the "Initial Step Size". As soon as the first point is detected, at which the BER is above the given limit, the sweep ends. If this parameter is set to, true "Initial Step Size" is used until the fail point. The skew value is then reduced by half of the initial step size and, according to the binary search algorithm, increased or decreased depending on the BER result. For each step the step size is divided by 2 until "Min. Step Size" is reached.

Disturbance Pattern	The methodology for this test involves sending HS burst sequences containing valid minimum-length T_CLK-PREPARE values (38 ns), followed by a valid minimum-length T_CLK-ZERO (262 ns), so that TCLK-PREPARE + TCLK-ZERO is at the minimum conformant value of 300ns. However, at the beginning of TCLK-ZERO, repeating 1010 HS clock data will be inserted in place of the first 95 - 38 = 57 ns of TCLK-ZERO. This 'false clock' sequence is used to create the appearance that the HS clock signal has started, when really there will be another period of HS-0 following this sequence, before the HS clock actually begins.
End Value	For tests in which a range of values is tested; specifies the last value that is tested
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Start Value	Specifies the first value that is tested for tests in which a range of values is tested.
Step Size in UI	Specifies the size of the steps in UI that is used between the Start Value and the End Value for tests in which a range of values is tested.
T-Clk-Post	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of T_HS-Trail to the beginning of T_Clk-Trail.
T-Clk-Pre	Time that the HS clock will be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.
T-Clk/HS Prepare	This parameter has two meanings: ▪ During Clock Timing tests such as the "HS-RX Clock Tests, it is used for T_Clk-Prepare, the time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. ▪ During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Prepare, the time specified for the Data Lane(s).
T-Clk/HS Prepare + Clk/HS-Zero	This parameter has two meanings: ▪ During Clock Timing tests such as the "HS-RX Clock Tests", it is used for T_Clk-Prepare + T_Clk_Zero (T_Clk-Prepare plus time that the transmitter drives the HS-0 state prior to starting the Clock). ▪ During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Prepare + T_Clk_Zero as specified for the Data Lane(s).
T-Clk/HS Trail	This parameter has two meanings: ▪ During Clock Timing tests such as the "HS-RX Clock Tests", it is used for T_Clk-Trail, the time that the transmitter drives the HS-0 state after last payload data bit of a HS transmission burst. ▪ During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Trail, the corresponding time for the Data Lane(s).

Results

The image data must be properly received by the DUT without error.

Table 44 Parameters in the result table for "Test 2.4.8 T_ Clock- Settle - Clock Procedure"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence for the given T_CLK-SETTLE value ▪ Fail: the DUT failed to receive the test sequence
max. passed T_Clk-Settle [ns]	Maximum T_CLK-SETTLE value for which the DUT passed the test
min. failed T_Clk-Settle [ns]	Minimum T_CLK-SETTLE value for which the DUT failed the test
min. Spec T_Clk-Settle [ns]	Minimum T_CLK-SETTLE value according to the specification
max. Spec T_Clk-Settle [ns]	Maximum T_CLK-SETTLE value according to the specification

Test 2.4.9 T_Clk-Trail - Clock Procedure

CTS Test Number and Name

Test 2.4.9 – Clock Lane HS-RX TCLK-TRAIL Tolerance

Purpose

To verify that the DUT's Clock Lane HS receiver can tolerate receiving values of T_CLK-TRAIL that conform to the specification.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

Parameters

Table 45 Parameters used in Test 2.4.9 T_Clk-Trail - Clock Procedure

Parameter	Description
BER Limit	Limit used for bit-error-ratio test
End Value	For tests in which a range of values is tested; specifies the last value that is tested.

HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Start Value	Specifies the first value that is tested for tests in which a range of values is tested.
Steps	Specifies the number of steps that are tested between the Start Value and the End Value for tests in which a range of values is tested.
T-Clk-Post	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of T_HS-Trail to the beginning of T_Clk-Trail.
T-Clk-Pre	Time that the HS clock will be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.
T-Clk/HS Prepare	This parameter has two meanings: ▪ During Clock Timing tests such as the “HS-RX Clock Tests, it is used for T_Clk-Prepare, the time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. ▪ During Data Timing tests such as the “HS-RX Data0 Tests”, it is used for T_HS-Prepare, the time specified for the Data Lane(s).
T-Clk/HS Prepare + Clk/HS-Zero	This parameter has two meanings: ▪ During Clock Timing tests such as the “HS-RX Clock Tests”, it is used for T_Clk-Prepare + T_Clk_Zero (T_Clk-Prepare plus time that the transmitter drives the HS-0 state prior to starting the Clock). ▪ During Data Timing tests such as the “HS-RX Data0 Tests”, it is used for T_HS-Prepare + T_Clk_Zero as specified for the Data Lane(s).
T-Clk/HS Trail	This parameter has two meanings: ▪ During Clock Timing tests such as the “HS-RX Clock Tests”, it is used for T_Clk-Trail, the time that the transmitter drives the HS-0 state after last payload data bit of a HS transmission burst. ▪ During Data Timing tests such as the “HS-RX Data0 Tests”, it is used for T_HS-Trail, the corresponding time for the Data Lane(s).

Results

For all test cases, the DUT must successfully receive the HS image data without error.

Table 46 Parameters in the result table for Test 2.4.9 T_Clk-Trail - Clock Procedure”

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence for the given T_CLK-TRAIL value. ▪ Fail: he DUT failed to receive the test sequence.
Parameter	Tested timing parameter.

Min Passed	Minimum T_CLK-TRAIL value for which the DUT passed the test.
Min Spec [ns]	Minimum T_CLK-TRAIL value according to the specification.
Max Passed [ns]	Maximum T_CLK-TRAIL value for which the DUT passed the test.
Max Spec [ns]	Maximum T_CLK-TRAIL value according to the specification.

Test 2.4.10 T_Clk-Miss Procedure

CTS Test Number and Name

Test 2.4.10 – Clock Lane HS-RX TCLK-MISS Value.

Purpose

To verify that the DUT's Clock Lane HS receiver correctly detects the cessation of clock activity and disconnects its line termination within the maximum allowed interval (T_CLK-MISS).

Dependencies

This test is available in Expert Mode only.

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

Parameters

Table 47 Parameters used in Test 2.4.10 T_Clk-Miss Procedure

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
End Value	For tests in which a range of values is tested; specifies the last value that is tested.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode.

Setup file name	The PPI BER Reader searches for a file name with the extension Setup.ala in the directory.
Start Value	Specifies the first value that is tested for tests in which a range of values is tested.
Steps	Specifies the number of steps that are tested between the Start Value and the End Value for tests in which a range of values is tested.

Results

The TCLK-MISS (Max Passed [ns]) must be less than 60 ns.

Table 48 Parameters in the results table for "Test 2.4.10 T_Clk-Miss Procedure"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence for the given T_CLK-MISS value. ▪ Fail: the DUT failed to receive the test sequence.
Parameter	Tested timing parameter.
Max Passed [ns]	Maximum T_CLK-MISS value for which the DUT passed the test.
Max Spec [ns]	Maximum T_CLK-MISS value according to the specification.

Test 2.4.11a T_Clk-Pre - Clock Procedure

CTS Test Number and Name

Test 2.4.11 – Clock Lane HS-RX TCLK-PRE and TCLK-POST Tolerance

Purpose

To verify that the DUT's Clock Lane HS receiver can tolerate the reception of bursts that has minimum-duration T_CLK-PRE values.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

Parameters

Table 49 Parameters used in Test 2.4.11a T_Clk-Pre - Clock Procedure

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
End Value	For tests in which a range of values is tested; specifies the last value that is tested.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Start Value	Specifies the first value that is tested for tests in which a range of values is tested.
Steps	Specifies the number of steps that are tested between the Start Value and the End Value for tests in which a range of values is tested.
T-Clk-Post	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of T_HS-Trail to the beginning of T_Clk-Trail.
T-Clk-Pre	Time that the HS clock will be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.
T-Clk/HS Prepare	This parameter has two meanings: ▪ During Clock Timing tests such as the “HS-RX Clock Tests,”, it is used for T_Clk-Prepare, the time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. ▪ During Data Timing tests such as the “HS-RX Data0 Tests”, it is used for T_HS-Prepare, the time specified for the Data Lane(s).
T-Clk/HS Prepare + Clk/HS-Zero	This parameter has two meanings: ▪ During Clock Timing tests such as the “HS-RX Clock Tests”, it is used for T_Clk-Prepare + T_Clk_Zero (T_Clk-Prepare plus time that the transmitter drives the HS-0 state prior to starting the Clock). ▪ During Data Timing tests such as the “HS-RX Data0 Tests”, it is used for T_HS-Prepare + T_Clk_Zero as specified for the Data Lane(s).
T-Clk/HS Trail	This parameter has two meanings: ▪ During Clock Timing tests such as the “HS-RX Clock Tests”, it is used for T_Clk-Trail, the time that the transmitter drives the HS-0 state after last payload data bit of a HS transmission burst. ▪ During Data Timing tests such as the “HS-RX Data0 Tests”, it is used for T_HS-Trail, the corresponding time for the Data Lane(s).

Results

The DUT must successfully receive the HS image data without error and the minimum TX conformant value for T_CLK-PRE must be 8*UI.

Table 50 Parameters in the result data table "Test 2.4.11a T_Clk-Pre - Clock Procedure"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence for the given T_CLK-MISS value. ▪ Fail: the DUT failed to receive the test sequence.
Parameter	Tested timing parameter.
Min Passed [ns]	Minimum T_CLK-PRE value for which the DUT passed the test.
Min Spec [ns]	Minimum T_CLK-PRE value according to the specification.
Max Passed [ns]	Maximum T_CLK-PRE value for which the DUT passed the test.
Max Spec [ns]	Maximum T_CLK-PRE value according to the specification.

Test 2.4.11b T_Clk-Post Clock Procedure

CTS Test Number and Name

Test 2.4.11 – Clock Lane HS-RX TCLK-PRE and TCLK-POST Tolerance.

Purpose

To verify that the DUT's Clock Lane HS receiver can tolerate the reception of bursts that has minimum duration T_CLK-POST values.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

Parameters

Same as Test 2.4.11a T_Clk-Pre - Clock Procedure on page 156.

Results

The DUT must successfully receive the HS image data without error and the minimum TX conformant value for T_CLK-POST must be 60 ns+52*UI.

Table 51 Parameters in the results data table "Test 2.4.11b T_Clk-Post Clock Procedure"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence for the given T_CLK-MISS value. ▪ Fail: the DUT failed to receive the test sequence.
Parameter	Tested timing parameter.
Min Passed [ns]	Minimum T_CLK-POST value for which the DUT passed the test.
Min Spec [ns]	Minimum T_CLK-POST value according to the specification.
Max Passed [ns]	Maximum T_CLK-POST value for which the DUT passed the test.
Max Spec [ns]	Maximum T_CLK-POST value according to the specification.

Data Tests

NOTE

For M8195A module, in Receiver Test Configuration, if you select “1 Lane” from “Number of Data Lanes:”, only Data0 tests are available. But if you select “2 Lanes”, then Data1 tests, corresponding to Lane 2, are also available along with Data0 tests.

Similarly, if you select “3 Lanes” or “4 Lanes”, Data2 tests or Data3 tests are available respectively, along with the preceding Data lane tests.

This section describes Data0 tests. Use the same description for Data1, Data2 and Data3 tests respectively.

Test 2.3.1 Vcmrx Tolerance Data

CTS Test Number and Name

Test 2.3.1 – HS-RX Common Mode Voltage Tolerance (V_CMRX(DC))

Purpose, Dependencies, Parameters, Results

Same as Test 2.3.1 Vcmrx Tolerance Clock on page 134.

Test 2.3.2 V_IDTH and Test 2.3.3 V_IDTL Sensitivity Data

CTS Test Number and Name

- Test 2.3.2 – HS-RX Differential Input High Threshold (V_IDTH)
- Test 2.3.3 – HS-RX Differential Input Low Threshold (V_IDTL)

Purpose, Dependencies, Parameters and Results

Same as Test 2.3.2 V_IDTH and Test 2.3.3 V_IDTL Sensitivity Clock on page 135.

Test 2.3.4 V_IHHS Sensitivity Data

CTS Test Number and Name

Test 2.3.4 – HS-RX Single-Ended Input High Voltage (V_IHHS)

Purpose, Dependencies, Parameters and Results

Same as Test 2.3.4 V_IHHS Sensitivity Clock on page 137.

Test 2.3.5 V_ILHS Sensitivity Data

CTS Test Number and Name

Test 2.3.5 – HS-RX Single-Ended Input Low Voltage (V_ILHS)

Purpose, Dependencies, Procedure, Parameters and Results

Same as Test 2.3.5 V_ILHS Sensitivity Clock on page 139.

Test 2.3.6 HS RX CM Interference 50-450 MHz Data

CTS Test Number and Name

Test 2.3.6 – HS-RX Common-Mode Interference 50MHz - 450MHz (ΔV_CMRX(LF))

Purpose, Dependencies, Parameters and Results

Same as Test 2.3.6 HS RX CM Interference 50-450 MHz Clock on page 140.

Test 2.3.7 HS RX CM Interference beyond 450 MHz Data

CTS Test Number and Name

Test 2.3.7 – HS-RX Common-Mode Interference Beyond 450MHz (ΔV_CMRX(HF))

Purpose, Dependencies, Parameters and Results

Same as Test 2.3.7 HS RX CM Interference beyond 450 MHz Clock on page 142.

Test 2.3.8.1 HS-RX Skew-Amplitude Test for Data Rates 1.5Gbps and lower Data0

NOTE This test is available only for DUTs operating at HS rates < 1.5Gbps.

CTS Test Number and Name

Test 2.3.8 – HS-RX Setup/Hold and Jitter Tolerance

Purpose

To verify that the DUT can tolerate signals with worst-case timing error between the Clock and Data Skew signals.

Dependencies

Ensure that all the Calibration procedures have been performed before the actual test starts. For the value of the intrinsic jitter test parameter a particular result of the jitter calibration procedure is used. It is the jitter measured when no external jitter was injected, that is, the jitter inherent in the test setup.

Parameters

Table 52 Parameters used in Test 2.3.8.1 HS-RX Skew-Amplitude Test for Data Rates 1.5Gbps and lower Clock

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
BER Reader for Init String	Sets the Initialization string for the Clock in the bit-error-ratio reader.
Binary Search	If this parameter is set to false, then the skew will be swept first with the “Initial Step Size”. As soon as the first point is detected, at which the BER is above the given limit, the sweep ends. If this parameter is set to, true “Initial Step Size” is used until the fail point. The skew value is then reduced by half of the initial step size and, according to the binary search algorithm, increased or decreased depending on the BER result. For each step the step size is divided by 2 until “Min. Step Size” is reached.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Initial Skew Deviation	Allows to save time by starting the test with a Clock to Data Skew different to 0.5UI. The test range will be from 0.5 UI + Initial Skew Deviation to 1 UI and from -0.5 UI - Initial Skew Deviation to -1 UI.

Initial Step Size	This is the initial skew step size used in this test. If “Binary Search” is set to true, the skew will be increased for the T_HOLD verification and decreased for T-SETUP with this step size. After the first fail point, the initial step size is divided by a factor of two until the “Minimum Step Size” is reached. If “Binary Search” is set to false, the step size will be kept constant.
Intrinsic Jitter	This parameter allows the influence of the test setup on the pass/fail criteria to be removed. Since the specification limits are given at the pins of the RX and the eye may already be closed by ISI and other jitter components, half of the intrinsic jitter needs to be added to the setup and hold time. The default value is taken from the jitter calibration. If the jitter calibration was not conducted with the board used during the test, the intrinsic jitter value can be modified.
Maximum Tested Skew	Maximum tolerable skew between data and clock edges.
Min. Step Size	This is the minimum skew step size used with “Binary Search” set to true.
Offline	Offline Mode.
Transition Time	Transition time required to perform Rise Time calibration. Ensure to set the same value for all dependent tests.
V_CMTX max	Maximum HS transmit static common-mode voltage. The common-mode voltage VCMTX is defined as the value of the voltages at the Dp and Dn pins.
V_CMTX min	Minimum HS transmit static common-mode voltage. The common-mode voltage VCMTX is defined as the value of the voltages at the Dp and Dn pins.
V_OD	The value of differential output voltage V_OD which is defined as the difference of the voltages V_DP and V_DN at the Dp and Dn pins, respectively.

Results

The DUT must receive zero errors.

Table 53 Parameters in the result table for “Test 2.3.8.1 HS-RX Skew-Amplitude Test for Data Rates 1.5Gbps and lower Clock”

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors. ▪ Fail: the DUT failed to receive the test sequence.
Skew Type	Type of skew used during the test are: Hold: Skew T_Hold Setup: Skew T_Setup Eye Opening: Skew T_Hold and T_Setup
VCMTX [mV]	HS transmit static common-mode voltage.
Max Passed [UI]	Maximum Skew value tested so far that did not prevent the DUT from receiving the test sequence.
Max Tested [UI]	Maximum tested Skew.

Max Spec [UI]	Maximum Skew that the DUT should be able to handle according to the specification.
Resulting minimum T_hold/T_setup [UI]	Minimum Skew that the DUT attained in its Hold or Setup states.
Comment	Displays information relevant to the tests.

Test 2.3.8.2 Jitter and Eye Diagram Tolerance for Data Rates from 1.5Gbps to 2.5Gbps Data0

NOTE This test is available only for DUTs operating at HS rates ≥ 1.5Gbps to < 2.5Gbps.

CTS Test Number and Name

Test 2.3.8 – HS-RX Clock-to-Data-Skew and Jitter Tolerance

Purpose

To measure the clock-to-data skew and jitter tolerance.

Dependencies

Ensure that all the Calibration procedure, including Transition time, ISI, Eye Opening, and HS levels calibration procedures are performed before the actual test starts. For the value of the intrinsic jitter test parameter, a particular result of the jitter calibration procedure is used. It is the jitter, which is measured when no external jitter was injected. In other words, the jitter is inherent in the test setup.

Procedure

The MIPI D-PHY CTS plug-in uses the *HSDeskew.seq* file, by default, which contains an initial skew block to allow the Receiver to align the data-to-clock-skew internally, followed by a test sequence that checks if the Receiver is receiving HS data properly.

The procedure applies the calibrated transition times, the selected reference channel and TX-Equalization to reach the ISI target value of 0.2 UI. Finally, the SJ is applied at a frequency of a tenth of the data rate value, and the swing (V_OD) is reduced to reach the target eye width of 0.5 UI and the eye opening of 40mV. Also, SSC is applied at a frequency of 33kHz and -5000 ppm to generate the maximum stress for the Receiver.

Then, the skew between clock and data is set to -0.3 UI, 0 UI and +0.3UI and the first common mode voltage offset of 0.2mV. The skew configuration is repeated for 0.15mV and 0.25mV offset values, so that there are 9 test points in total. For each point, the BER is measured. For the test to pass at all test points, a BER value, which is lower or equal to the target value, is required.

Parameters

The parameters in expert mode for this measurement are:

Table 54 Parameters used in "Test 2.3.8.2 Jitter and Eye Diagram Tolerance for Data Rates from 1.5Gbps to 2.5Gbps Data0"

Parameter (Global)	Description
Reference Channel S-Parameter File	The S-parameter file, which is used to emulate a channel during the test. For data rates below 4.5 Gbps, the long channel is recommended to reach the 0.2 UI ISI limit. For higher data rates, the standard channel is suitable.
Parameter (Test 2.3.8 HS RX Clock-to-Data Skew and Jitter Data0)	**Description**
BER Limit	Bit-Error Ratio limit value to determine the pass/fail status of the test
BER Reader for Init String	Sets the Initialization string for the Data in the bit-error-ratio reader
Common-Mode Voltage Levels	List of common mode voltage offset levels to be tested
Eye Height Target	Minimum Eye Height target set during calibration, which must be attained during the test
Eye Width Target	Minimum Eye Width target obtained during calibration, which must be attained during the test
HS Frequency	Frequency of the HS signal
Jitter Frequency	Frequency of the applied jitter
Offline	Offline Mode
SJ Amplitude	Amplitude of the Sinusoidal Jitter
Static Skew Values [UI]	List of skew values that will be applied for this test
Steps	Number of steps (read-only, depends on the skew and common mode voltage range)
Test Sequence File	The sequence file requires an initial skew pattern to allow the receiver to adapt to the static skew, and a test pattern that can be used for detecting bit errors

Results

The DUT must receive zero errors.

Table 55 Parameters in the result table for "Test 2.3.8.2 Jitter and Eye Diagram Tolerance for Data Rates from 1.5Gbps to 2.5Gbps Data0"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors. ▪ Fail: the DUT failed to receive the test sequence.
Target Eye Opening [mV]	Calibrated Vertical Eye Opening
Applied Amplitude (Vpp) [mV]	Amplitude applied to reach the calibrated eye opening
Applied SJ [mUI]	Amplitude of SJ that must be applied to reach the target eye width
Offset [mV]	Tested common mode Offset
Static Skew [mUI]	Skew applied for the actual test point

Test 2.3.8.3 Jitter and Eye Diagram Tolerance for Data Rates from upper 2.5Gbps to 4.5Gbps Data0

NOTE This test is available only for DUTs operating at HS rates ≥ 2.5Gbps and ≤ 4.5Gbps.

CTS Test Number and Name

Test 2.3.8 – HS-RX Clock-to-Data-Skew and Jitter Tolerance

Purpose

To measure the clock-to-data skew and jitter tolerance.

Dependencies

Ensure that all the Calibration procedure, including Transition time, ISI, Eye Opening, and HS levels calibration procedures are performed before the actual test starts. For the value of the intrinsic jitter test parameter, a particular result of the jitter calibration procedure is used. It is the jitter, which is measured when no external jitter was injected. In other words, the jitter is inherent in the test setup.

Procedure

The MIPI D-PHY CTS plug-in uses the *HSDeskew.seq* file, by default, which contains an initial skew block to allow the Receiver to align the data-to-clock-skew internally, followed by a test sequence that checks if the Receiver is receiving HS data properly.

The procedure applies the calibrated transition times, the selected reference channel and TX-Equalization to reach the ISI target value of 0.2 UI. Finally, the SJ is applied at a frequency of a tenth of the data rate value, and the swing (V_OD) is reduced to reach the target eye width of 0.5 UI and the eye opening of 40mV. Also, SSC is applied at a frequency of 33kHz and -5000 ppm to generate the maximum stress for the Receiver.

Then, the skew between clock and data is set to -0.3 UI, 0 UI and +0.3UI and the first common mode voltage offset of 0.2mV. The skew configuration is repeated for 0.15mV and 0.25mV offset values, so that there are 9 test points in total. For each point, the BER is measured. For the test to pass at all test points, a BER value, which is lower or equal to the target value, is required.

Parameters

The parameters in expert mode for this measurement are:

Table 56 Parameters used in "Test 2.3.8.3 Jitter and Eye Diagram Tolerance for Data Rates up per 2.5Gbps to 4.5Gbps Data0"

Parameter (Global)	Description
Reference Channel S-Parameter File	The S-parameter file, which is used to emulate a channel during the test. For data rates below 4.5 Gbps, the long channel is recommended to reach the 0.2 UI ISI limit. For higher data rates, the standard channel is suitable.
Parameter (Test 2.3.8 HS RX Clock-to-Data Skew and Jitter Data0)	**Description**
BER Limit	Bit-Error Ratio limit value to determine the pass/fail status of the test
BER Reader for Init String	Sets the Initialization string for the Data in the bit-error-ratio reader
Common-Mode Voltage Levels	List of common mode voltage offset levels to be tested
Eye Height Target	Minimum Eye Height target set during calibration, which must be attained during the test
Eye Width Target	Minimum Eye Width target obtained during calibration, which must be attained during the test
HS Frequency	Frequency of the HS signal
Jitter Frequency	Frequency of the applied jitter
Offline	Offline Mode
SJ Amplitude	Amplitude of the Sinusoidal Jitter
Static Skew Values [UI]	List of skew values that will be applied for this test
Steps	Number of steps (read-only, depends on the skew and common mode voltage range)
Test Sequence File	The sequence file requires an initial skew pattern to allow the receiver to adapt to the static skew, and a test pattern that can be used for detecting bit errors

Results

The DUT must receive zero errors.

Table 57 Parameters in the result table for "Test 2.3.8.3 Jitter and Eye Diagram Tolerance for Data Rates upper 2.5Gbps to 4.5Gbps Data0"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors. ▪ Fail: the DUT failed to receive the test sequence.
Target Eye Opening [mV]	Calibrated Vertical Eye Opening
Applied Amplitude (Vpp) [mV]	Amplitude applied to reach the calibrated eye opening
Applied SJ [mUI]	Amplitude of SJ that must be applied to reach the target eye width
Offset [mV]	Tested common mode Offset
Static Skew [mUI]	Skew applied for the actual test point

Test 2.3.9 HS RX SSC Tolerance Data

NOTE This test is available only for DUTs operating at HS rates >= 2.5Gbps on an M8195A module.

CTS Test Number and Name

Test 2.3.9–HS RX SSC Tolerance

Purpose

To measure the SSC tolerance of the receiver up to the limits defined in the MIPI D-PHY 2.1 specification for the SSC amplitude and its derivative.

Dependencies

Ensure that the SSC Calibration procedure has been performed before the actual test starts.

Procedure

The MIPI D-PHY CTS plug-in uses the default pattern and levels selected in the Configuration panel of the MIPI D-PHY CTS plug-in.

Then, the calibrated limits of SSC frequency and amplitude are applied on one side the SSC and on the other side, an SJ component is applied to reach the maximum/minimum derivative of the SSC.

Parameters

The parameters in expert mode for this measurement are:

Table 58 Parameters used in "Test 2.3.9 HS RX SSC Tolerance Data0"

Parameter	Description
SSC Frequency	SSC frequency used for this calibration (default is 33 kHz)
SSC Deviation	SSC minimum point or the maximum deviation of the nominal data rate (only 0 and negative values are allowed, because it is a down-spread SSC)
Test Range	Start and Stop value, and number of steps for the SSC derivative (done by SJ at 1 MHz)

Results

Table 59 Parameters in the result table for "Test 2.3.9 HS RX SSC Tolerance"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors. ▪ Fail: the DUT failed to receive the test sequence.
SSC Frequency [kHz]	Displays the SSC frequency in kHz
SSC Deviation [ppm]	Displays the SSC deviation in ppm
SJ Amplitude [mUI]	SJ amplitude that must be applied to reach the test point of the SSC derivative
SSC Derivative [ppm/µs]	Calibrated derivative of the SSC
Min Passed[UI]	Minimum Skew value tested so far that did not prevent the DUT from receiving the test sequence.
Min Tested [UI]	Minimum tested Skew.
Min Spec [UI]	Minimum Skew that the DUT should be able to handle according to the specification.

Test 2.4.2 T_HS-Prepare_Zero Compliance Procedure Data0

CTS Test Number and Name

Test 2.4.2 – Data Lane HS-RX THS-PREPARE + THS-ZERO Tolerance

Purpose

To verify that the DUT's Data Lane HS receiver can tolerate the reception of conformant values for THS-PREPARE + THS-ZERO.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

Parameters

Table 60 Parameters used in Test 2.4.2 T_HS-Prepare_Zero Compliance Procedure DataT0

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
T-Clk-Post	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of T_HS-Trail to the beginning of T_Clk-Trail.

T-Clk-Pre	Time that the HS clock will be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.
T-Clk/HS Trail	This parameter has two meanings: During Clock Timing tests such as the “HS-RX Clock Tests”, it is used for T_Clk-Trail, the time that the transmitter drives the HS-0 state after last payload data bit of a HS transmission burst. During Data Timing tests such as the “HS-RX Data0 Tests”, it is used for T_HS-Trail, the corresponding time for the Data Lane(s).
T- Prepare; T- Prepare -Zero	T- Prepare is the time that the HS clock will be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. T- Prepare –Zero is the time taken for the transmitter to drive HS -0 state prior to transmitting sync sequence.

Results

For all test cases, the DUT must successfully receive the HS burst data without error.

Table 61 Parameters in the result table for “Test 2.4.2 T_HS-Prepare_Zero Compliance Procedure Data0”

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors. ▪ Fail: the DUT failed to receive the test sequence.
T_HS-Prepare [ns]	T_HS-PREPARE used for this test step.
T_HS-Zero [ns]	T_HS-ZERO used for this test step.
T_HS-Prepare+Zero [ns]	Total T_HS-PREPARE + T_HS-ZERO used for this test step.

Test 2.4.2a T_HS-Prepare Data Procedure

CTS Test Number and Name

This test is provided additionally for product characterization. It is based on the CTS test 2.4.2.

Purpose

To characterize the DUT's Data Lane HS receiver tolerance for T_HS-PREPARE timing deviations.

Dependencies

This test is available in Expert Mode only.

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

Parameters

Table 62 Parameters used in Test 2.4.2a T_HS-Prepare Data Procedure

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
End Value	For tests in which a range of values is tested; specifies the last value that is tested.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Start Value	Specifies the first value that is tested for tests in which a range of values is tested.
Steps	Specifies the number of steps that are tested between the Start Value and the End Value for tests in which a range of values is tested.
T-Clk-Post	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of T_HS-Trail to the beginning of T_Clk-Trail.
T-Clk-Pre	Time that the HS clock will be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.

T-Clk/HS Prepare	This parameter has two meanings: ▪ During Clock Timing tests such as the “HS-RX Clock Tests, section 4.1”, it is used for T_Clk-Prepare, the time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission, ▪ During Data Timing tests such as the “HS-RX Data0 Tests”, it is used for T_HS-Prepare, the time specified for the Data Lane(s).
T-Clk/HS Prepare + Clk/HS-Zero	This parameter has two meanings: ▪ During Clock Timing tests such as the “HS-RX Clock Tests”, it is used for T_Clk-Prepare + T_Clk_Zero (T_Clk-Prepare plus time that the transmitter drives the HS-0 state prior to starting the Clock). ▪ During Data Timing tests such as the “HS-RX Data0 Tests”, it is used for T_HS-Prepare + T_Clk_Zero as specified for the Data Lane(s).
T-Clk/HS Trail	This parameter has two meanings: ▪ During Clock Timing tests such as the “HS-RX Clock Tests”, it is used for T_Clk-Trail, the time that the transmitter drives the HS-0 state after last payload data bit of a HS transmission burst. ▪ During Data Timing tests such as the “HS-RX Data0 Tests”, it is used for T_HS-Trail, the corresponding time for the Data Lane(s).

Results

For all test cases, the DUT must successfully receive the HS burst data without error.

Table 63 Parameters in the result table for “Test 2.4.2a T_HS-Prepare Data Procedure”

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors for T_HS-PREPARE values within the specification. ▪ Fail: the DUT failed to receive the test sequence.
Parameter	Timing parameter that is being tested.
Min Passed [ns]	Minimum T_HS-PREPARE for which the DUT passed the test.
Min Spec [ns]	Minimum T_HS-PREPARE according to the specification.
Max Passed [ns]	Maximum T_HS-PREPARE for which the DUT passed the test.
Max Spec [ns]	Maximum T_HS-PREPARE according to the specification.

Test 2.4.2b T_HS_Zero - Data Procedure

CTS Test Number and Name

This test is provided additionally for product characterization. It is based on the CTS test 2.4.2.

Purpose

To characterize the DUT's Data Lane HS receiver tolerance for T_HS-PREPARE + T_HS-ZERO timing deviations.

Dependencies

This test is available in Expert Mode only.

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

Parameters

Same as Test 2.4.2a T_HS-Prepare Data Procedure on page 174.

Results

For all test cases, the DUT must successfully receive the HS burst data without error.

Table 64 Parameters in the result table for "Test 2.4.2b T_HS_Zero - Data Procedure"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors for T_HS-PREPARE + T_HS-ZERO values within the specification. ▪ Fail: the DUT failed to receive the test sequence.
T_HS-Prepare [ns]	T_HS-PREPARE used for this step of the test.
T_HS-Zero [ns]	T_HS-ZERO used for this step of the test.
Parameter	Timing parameter that is being tested.
Min Passed [ns]	Minimum T_HS-PREPARE + T_HS-ZERO for which the DUT passed the test.

Min Spec [ns]	Minimum T_HS- PREPARE + T_HS-ZERO according to the specification.
Max Passed [ns]	Maximum T_HS- PREPARE + T_HS-ZERO for which the DUT passed the test.
Max Spec [ns]	Maximum T_HS- PREPARE + T_HS-ZERO according to the specification.

Test 2.4.3 T_HS Settle - Data Procedure

CTS Test Number and Name

Test 2.4.3 – Data Lane HS-RX THS-SETTLE Value

Purpose

To verify that the DUT's Data Lane receiver incorporates a sufficient time-out interval (T_HS-SETTLE) to ignore transition effects that may occur during the HS Entry sequence.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

Parameters

Table 65 Parameters used in Test 2.4.3 T_HS Settle - Data Procedure

Parameter	Description
BER Limit	The Limit used for bit-error-ratio test.
Binary Search	If this parameter is set to false, then the skew will be swept first with the "Initial Step Size". As soon as the first point is detected, at which the BER is above the given limit, the sweep ends. If this parameter is set to, true "Initial Step Size" is used until the fail point. The skew value is then reduced by half of the initial step size and, according to the binary search algorithm, increased or decreased depending on the BER result. For each step the step size is divided by 2 until "Min. Step Size" is reached.
Disturbance Pattern	Additional HS data byte appended after the valid HS burst.
End Value	For tests in which a range of values is tested; specifies the last value that is tested.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.

Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Start Value	Specifies the first value that is tested for tests in which a range of values is tested.
Step Size in UI	Specifies the size of the steps in UI that is used between the Start Value and the End Value for tests in which a range of values is tested; depending on the specific procedure.
T-Clk-Post	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of T_HS-Trail to the beginning of T_Clk-Trail.
T-Clk-Pre	Time that the HS clock will be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.
T-Clk/HS Prepare	This parameter has two meanings: ▪ During Clock Timing tests such as the "HS-RX Clock Tests, section 4.1", it is used for T_Clk-Prepare, the time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. ▪ During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Prepare, the time specified for the Data Lane(s).
T-Clk/HS Prepare + Clk/HS-Zero	This parameter has two meanings: ▪ During Clock Timing tests such as the "HS-RX Clock Tests", it is used for T_Clk-Prepare + T_Clk_Zero (T_Clk-Prepare plus time that the transmitter drives the HS-0 state prior to starting the Clock). ▪ During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Prepare + T_Clk_Zero as specified for the Data Lane(s).
T-Clk/HS Trail	This parameter has two meanings: ▪ During Clock Timing tests such as the "HS-RX Clock Tests", it is used for T_Clk-Trail, the time that the transmitter drives the HS-0 state after last payload data bit of a HS transmission burst. ▪ During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Trail, the corresponding time for the Data Lane(s).

Results

The T_HS-SETTLE must be greater than 85 ns + 6*UI.

Table 66 Parameters in the result table for "Test 2.4.3 T_HS Settle - Data Procedure"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors for T_HS-SETTLE values within the specification. ▪ Fail: the DUT failed to receive the test sequence.
max. passed T_HS-Settle [ns]	Maximum T_HS-SETTLE for which the DUT passed the test.

min. failed T_HS-Settle [ns]	Minimum T_HS-SETTLTE for which the DUT failed the test.
min. Spec. T_HS-Settle [ns]	Minimum T_HS-SETTLE according to the specification.
max. Spec T_HS-Settle [ns]	Maximum T_HS-SETTLE according to the specification.

Test 2.4.4 T_HS Trail - Data Procedure

CTS Test Number and Name

Test 2.4.4 – Data Lane HS-RX THS-TRAIL Tolerance

Purpose

To verify that the DUT's Data Lane HS receiver can tolerate receiving value for T_HS-TRAIL that conform to the specification.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remains the same.

Parameters

Table 67 Parameters used in Test 2.4.4 T_HS Trail - Data Procedure

Parameter	Description
BER Limit	The Limit used for bit-error-ratio test.
End Value	For tests in which a range of values is tested; specifies the last value that is tested.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Start Value	Specifies the first value that is tested for tests in which a range of values is tested.
Steps	Specifies the number of steps that are tested between the Start Value and the End Value for tests in which a range of values is tested.

T-Clk-Post	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of T_HS-Trail to the beginning of T_Clk-Trail.
T-Clk-Pre	Time that the HS clock will be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.
T-Clk/HS Prepare	This parameter has two meanings: ▪ During Clock Timing tests such as the "HS-RX Clock Tests", it is used for T_Clk-Prepare, the time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. ▪ During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Prepare, the time specified for the Data Lane(s).
T-Clk/HS Prepare + Clk/HS-Zero	This parameter has two meanings: ▪ During Clock Timing tests such as the "HS-RX Clock Tests", it is used for T_Clk-Prepare + T_Clk_Zero (T_Clk-Prepare plus time that the transmitter drives the HS-0 state prior to starting the Clock). ▪ During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Prepare + T_Clk_Zero as specified for the Data Lane(s).
T-Clk/HS Trail	This parameter has two meanings: ▪ During Clock Timing tests such as the "HS-RX Clock Tests", it is used for T_Clk-Trail, the time that the transmitter drives the HS-0 state after last payload data bit of a HS transmission burst. ▪ During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Trail, the corresponding time for the Data Lane(s).

Results

The DUT must successfully receive the HS image data without error.

Table 68 Parameters in the result table for"Test 2.4.4 T_HS Trail - Data Procedure"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors for T_HS-TRAIL values within the specification. ▪ Fail: the DUT failed to receive the test sequence.
Parameter	Timing parameter that is being tested.
Min Passed [ns]	Minimum T_HS-TRAIL for which the DUT passed the test.
Min Spec [ns]	Minimum T_HS-TRAIL according to the specification.
Max Passed [ns]	Maximum T_HS-TRAIL for which the DUT passed the test.
Max Spec [ns]	Maximum T_HS-TRAIL according to the specification.

Test 2.4.5 T_HS Skip - Data Procedure

CTS Test Number and Name

Test 2.4.5 – Data Lane HS-RX T_HS-SKIP Value

Purpose

To verify that the DUT's Data Lane receiver ignores any transition in the data lane following a validly formed HS burst for T_HS-SKIP periods within the specification.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remains the same.

Parameters

Table 69 Parameters used in Test 2.4.5 T_HS Skip - Data Procedure

Parameter	Description
BER Limit	The Limit used for bit-error-ratio test.
Default T_Reot	Time needed by the system to transition from HS to LP. If a DSO is available, its value will be calibrated at the beginning of the test. In other case, the provided value will be used.
Disturbance Pattern	Additional HS data byte appended after the valid HS burst.
End Value	For tests in which a range of values is tested; specifies the last value that is tested.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Start Value	Specifies the first value that is tested for tests in which a range of values is tested.
Step Size in UI	Specifies the size of the steps in UI that is used between the Start Value and the End Value for tests in which a range of values is tested; depending on the specific procedure.
T-Clk-Post	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of T_HS-Trail to the beginning of T_Clk-Trail.

T-Clk-Pre	Time that the HS clock will be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.
T-Clk/HS Prepare	This parameter has two meanings: ▪ During Clock Timing tests such as the "HS-RX Clock Tests,", it is used for T_Clk-Prepare, the time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. ▪ During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Prepare, the time specified for the Data Lane(s).
T-Clk/HS Prepare + Clk/HS-Zero	This parameter has two meanings: ▪ During Clock Timing tests such as the "HS-RX Clock Tests", it is used for T_Clk-Prepare + T_Clk_Zero (T_Clk-Prepare plus time that the transmitter drives the HS-0 state prior to starting the Clock). ▪ During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Prepare + T_Clk_Zero as specified for the Data Lane(s).
T-Clk/HS Trail	This parameter has two meanings: ▪ During Clock Timing tests such as the "HS-RX Clock Tests", it is used for T_Clk-Trail, the time that the transmitter drives the HS-0 state after last payload data bit of a HS transmission burst. ▪ During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Trail, the corresponding time for the Data Lane(s).

Results

- The presence of the extra data byte must not negatively affect proper reception of data for T_HS-SKIP values up to and including 40 ns.
- Optional, Informative: The presence of the extra data byte must affect proper reception of data (via the observation of errors) for T_HS-SKIP values greater than (55 ns + 4*UI).

Table 70 Parameters in the result table for "Test 2.4.5 T_HS Skip - Data Procedure"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors, therefore ignoring the extra data byte following the T_HS-TRAIL interval. ▪ Fail: the DUT failed to receive the test sequence.
max. passed T_HS-Skip [ns]	Maximum T_HS-SKIP for which the DUT passed the test.
min. failed T_HS-Skip [ns]	Minimum T_HS-SKIP for which the DUT failed the test.
min. Spec. T_HS-Skip [ns]	Minimum T_HS-SKIP according to the specification.
max. Spec. T_HS-Skip [ns]	Maximum T_HS-SKIP according to the specification.

Test 2.4.12a T_HsIdlePost - Data Procedure

CTS Test Number and Name

Test 2.4.12a – T_HsIdlePost - Data

Purpose

To verify that the DUT's Data Lane remains in the HS-0 state for a duration of $T_{HS-IDLE-POST}$ until the Clock Lane enters the HS-0 state.

Dependencies

Ensure that the Transition Time Calibration, ISI Calibration and Eye Opening Calibration with Jitter procedures have been performed before the actual test starts. If these calibration procedures have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remains the same.

Procedure

Load the *HsIdle.seq* file in the Configuration panel of the MIPI D-PHY CTS plug-in. The multiplier in the parameter **Steps** is multiplied with the value assigned to the parameter **Start Value** to obtain the minimum value for $T_{HS-IDLE-POST}$ on the data signal. This value should be less than or equal to the value defined in the parameter **End Value**, which defines the maximum value that must be attained by $T_{HS-IDLE-POST}$ on the data signal. The resulting minimum and maximum values are compared with the compliance values as per specification.

Parameters

Table 71 Parameters used in "Test 2.4.12a T_HsIdlePost - Data Procedure"

Parameter	Description
BER Limit	The Limit used for bit-error-ratio test.
BER Reader Init String	Sets the Initialization string for the Data in the bit-error-ratio reader
End Value	For tests in which a range of values is tested; specifies the last value that is tested.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode.
Start Value	Specifies the first value that is tested for tests in which a range of values is tested.

Steps	Specifies the multiplier value in UI that is used to obtain the actual value for the **Start Value** parameter.
T_HS-Prepare	During Data Timing tests such as the “HS-RX Data0 Tests”, it is used for T_HS-Prepare + T_Clk_Prepare as specified for the Data Lane(s).
T_HS-PrepareZero	During Data Timing tests such as the “HS-RX Data0 Tests”, it is used for T_HS-Prepare + T_Clk_Zero as specified for the Data Lane(s).
T_HsIdleClkHs0	Typical duration when Clock Lane attains and remains in HS-0 state.
T_HsIdlePost	Typical duration when Clock Lane continues signaling until the HS Data Bursts finish transmission on all Lanes.
T_HsIdlePre	Typical duration when Clock Lane exits the HS-0 state and is active before the next HS Data Burst.

Results

- The minimum and maximum values must not exceed 512 UI.

Table 72 Parameters in the result table for “Test 2.4.12a T_HSIdlePost - Data Procedure”

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors. ▪ Fail: the DUT failed to receive the test sequence.
Parameter	The parameter under test.
Min Passed [UI]	Minimum T_HsIdlePost on the Data Lane for which the DUT passed the test.
Min Spec [UI]	Minimum T_HsIdlePost as defined in the MIPI D-PHY specification.
Max Passed [UI]	Maximum T_HsIdlePost on the Data Lane for which the DUT passed the test.
Max Spec [UI]	Maximum T_HsIdlePost as defined in the MIPI D-PHY specification.

Test 2.4.12b T_HsIdleClkHs0 - Data Procedure

CTS Test Number and Name

Test 2.4.12b – T_HsIdleClkHs0 - Data

Purpose

To verify that the DUT's Data Lane continues the HS-0 state for a duration of $T_{HS-IDLE-CLKHS0}$ while the Clock Lane drives the HS-0 state.

Dependencies

Ensure that the Transition Time Calibration, ISI Calibration and Eye Opening Calibration with Jitter procedures have been performed before the actual test starts. If these calibration procedures have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remains the same.

Procedure

Load the *HsIdle.seq* file in the Configuration panel of the MIPI D-PHY CTS plug-in. The multiplier in the parameter **Steps** is multiplied with the value assigned to the parameter **Start Value** to obtain the minimum value for $T_{HS-IDLE-CLKHS0}$ on the data signal. This value should be less than or equal to the value defined in the parameter **End Value**, which defines the maximum value that must be attained by $T_{HS-IDLE-CLKHS0}$ on the data signal. The resulting minimum and maximum values are compared with the compliance values as per specification.

Parameters

Table 73 Parameters used in "Test 2.4.12b T_HsIdleClkHs0 - Data Procedure"

Parameter	Description
BER Limit	The Limit used for bit-error-ratio test.
BER Reader Init String	Sets the Initialization string for the Data in the bit-error-ratio reader
End Value	For tests in which a range of values is tested; specifies the last value that is tested.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode.
Start Value	Specifies the first value that is tested for tests in which a range of values is tested.

Steps	Specifies the multiplier value in UI that is used to obtain the actual value for the **Start Value** parameter.
T_HS-Prepare	During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Prepare + T_Clk_Prepare as specified for the Data Lane(s).
T_HS-PrepareZero	During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Prepare + T_Clk_Zero as specified for the Data Lane(s).
T_HsIdleClkHs0	Duration when Clock Lane attains and remains in HS-0 state.
T_HsIdlePost	Duration when Clock Lane continues signaling until the HS Data Bursts finish transmission on all Lanes.
T_HsIdlePre	Duration when Clock Lane exits the HS-0 state and is active before the next HS Data Burst.

Results

- The minimum and maximum values must not exceed 500 ns.

Table 74 Parameters in the result table for "Test 2.4.12b T_HsIdleClkHs0 - Data Procedure"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors. ▪ Fail: the DUT failed to receive the test sequence.
Parameter	The parameter under test.
Min Passed [UI]	Minimum T_HsIdleClkHs0 on the Data Lane for which the DUT passed the test.
Min Spec [UI]	Minimum T_HsIdleClkHs0 as defined in the MIPI D-PHY specification.
Max Passed [UI]	Maximum T_HsIdleClkHs0 on the Data Lane for which the DUT passed the test.
Max Spec [UI]	Maximum T_HsIdleClkHs0 as defined in the MIPI D-PHY specification.

Test 2.4.12c T_HsIdlePre - Data Procedure

CTS Test Number and Name

Test 2.4.12c – T_HsIdlePre - Data

Purpose

To verify that the DUT's Clock Lane remains active for a duration of $T_{HS-IDLE-PRE}$ until the Data Lane starts transmitting the next HS Data Burst.

Dependencies

Ensure that the Transition Time Calibration, ISI Calibration and Eye Opening Calibration with Jitter procedures have been performed before the actual test starts. If these calibration procedures have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remains the same.

Procedure

Load the *HsIdle.seq* file in the Configuration panel of the MIPI D-PHY CTS plug-in. The multiplier in the parameter **Steps** is multiplied with the value assigned to the parameter **Start Value** to obtain the minimum value for $T_{HS-IDLE-PRE}$ on the data signal. This value should be less than or equal to the value defined in the parameter **End Value**, which defines the maximum value that must be attained by $T_{HS-IDLE-PRE}$ on the data signal. The resulting minimum and maximum values are compared with the compliance values as per specification.

Parameters

Table 75 Parameters used in "Test 2.4.12c T_HsIdlePre - Data Procedure"

Parameter	Description
BER Limit	The Limit used for bit-error-ratio test.
BER Reader Init String	Sets the Initialization string for the Data in the bit-error-ratio reader
End Value	For tests in which a range of values is tested; specifies the last value that is tested.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode.

Start Value	Specifies the first value that is tested for tests in which a range of values is tested.
Steps	Specifies the multiplier value in UI that is used to obtain the actual value for the **Start Value** parameter.
T_HS-Prepare	During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Prepare + T_Clk_Prepare as specified for the Data Lane(s).
T_HS-PrepareZero	During Data Timing tests such as the "HS-RX Data0 Tests", it is used for T_HS-Prepare + T_Clk_Zero as specified for the Data Lane(s).
T_HsIdleClkHs0	Duration when Clock Lane attains and remains in HS-0 state.
T_HsIdlePost	Duration when Clock Lane continues signaling until the HS Data Bursts finish transmission on all Lanes.
T_HsIdlePre	Duration when Clock Lane exits the HS-0 state and is active before the next HS Data Burst.

Results

- The minimum and maximum values must not exceed 96 UI.

Table 76 Parameters in the result table for "Test 2.4.12c T_HsIdlePre - Data Procedure"

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors. ▪ Fail: the DUT failed to receive the test sequence.
Parameter	The parameter under test.
Min Passed [UI]	Minimum T_HsIdlePre on the Data Lane for which the DUT passed the test.
Min Spec [UI]	Minimum T_HsIdlePre as defined in the MIPI D-PHY specification.
Max Passed [UI]	Maximum T_HsIdlePre on the Data Lane for which the DUT passed the test.
Max Spec [UI]	Maximum T_HsIdlePre as defined in the MIPI D-PHY specification.

Test 2.4.12 T_HsIdlePost T_HsIdleClkHs0 T_HsIdlePre Data Compliance Procedure

CTS Test Number and Name

Test 2.4.12 – T_HsIdlePost T_HsIdleClkHs0 T_HsIdlePre - Data Compliance

Purpose

To verify that the DUT's Data Lane transmits the HS Idle state between two HS Data Bursts within a combined duration of $T_{HsIdleTiming}$ ($T_{HS-IDLE-POST}$ + $T_{HS-IDLE-CLKHS0}$ + $T_{HS-IDLE-PRE}$); such that each value meets compliance according to the specification.

Dependencies

Ensure that the Transition Time Calibration, ISI Calibration and Eye Opening Calibration with Jitter procedures have been performed before the actual test starts. If these calibration procedures have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remains the same.

Procedure

Load the *HsIdle.seq* file in the Configuration panel of the MIPI D-PHY CTS plug-in. The multiplier in the parameter **TX PPI Bus Width** is multiplied with the minimum values assigned to T_HsIdlePost and T_HsIdlePre in the parameter **T_HsIdlePost; T_HsIdleClkHs0; T_HsIdlePre** to obtain the minimum value for $T_{HS-IDLE-POST}$ and $T_{HS-IDLE-PRE}$ on the data signal. This value should be less than or equal to the maximum value defined in the same parameter. The resulting minimum, typical and maximum values are compared with the compliance values as per specification.

Parameters

Table 77 Parameters used in "Test 2.4.12 T_HsIdlePost T_HsIdleClkHs0 T_HsIdlePre - Data Compliance Procedure"

Parameter	Description
BER Limit	The Limit used for bit-error-ratio test.
BER Reader Init String	Sets the Initialization string for the Data in the bit-error-ratio reader
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.

Offline	Offline Mode.
TX PPI Bus Width	Specifies the multiplier value in UI that is used to obtain the minimum values for the T_HsIdlePost and T_HsIdlePre timings.
T_HS-Prepare	During Data Timing tests such as the “HS-RX Data0 Tests”, it is used for T_HS-Prepare + T_Clk_Prepare as specified for the Data Lane(s).
T_HS-PrepareZero	During Data Timing tests such as the “HS-RX Data0 Tests”, it is used for T_HS-Prepare + T_Clk_Zero as specified for the Data Lane(s).
T_HsIdlePost; T_HsIdleClkHs0; T_HsIdlePre	Matrix of Minimum, Typical and Maximum values for each sub state in the HS Idle state.

Results

- The minimum, typical and maximum values for each timing must not exceed the compliance values given in the specification.

Table 78 Parameters in the result table for ““Test 2.4.12 T_HsIdlePost T_HsIdleClkHs0 T_HsIdlePre - Data Compliance Procedure”

Parameter name	Parameter description
Result	▪ Pass: the DUT was able to receive the test sequence without errors. ▪ Fail: the DUT failed to receive the test sequence.
Parameter	The parameter under test.
T_HsIdlePost [UI]	Minimum, typical and maximum configured T_HsIdlePost values on the Data Lane for which the DUT passed the test.
T_HsIdleClkHs0 [ns]	Minimum, typical and maximum configured T_HsIdleClkHs0 values on the Data Lane for which the DUT passed the test.
T_HsIdlePre [UI]	Minimum, typical and maximum configured T_HsIdlePre values on the Data Lane for which the DUT passed the test.

Semi-Automated Tests

Test 2.4.6 Clock Lane T_CLK-TERM-EN

CTS Test Number and Name

Test 2.4.6 – Clock Lane HS-RX T_CLK-TERM-EN Value

Purpose

To verify that the time required the DUT's Clock Lane receiver to enable its HS line termination (T_CLK-TERM-EN) is within the conformance limits.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remains the same.

Parameters

Table 79 Parameters used in Test 2.4.6 Clock Lane T_CLK-TERM-EN

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Trigger Level	The voltage level at which the other test sequences are inserted into the main signal.

Results

The T_CLK-TERM-EN must be greater than (the time for Dn to reach V_TERM-EN), and less than 38 ns.

Table 80 Parameters in the result data table "Test 2.4.6 Clock Lane T_CLK-TERM-EN"

Parameter name	Parameter description
Result	▪ Pass: the termination is enabled within the specified time. ▪ Fail: the termination was not enabled on time.
Signal	Signal that is being tested.
Timing [ns]	Time that the DUT took to enable the termination.
Max Spec [ns]	Maximum T_CLK-TERM-EN according to the specification.

Test 2.4.1 Data Lane T_HS-TERM-EN

CTS Test Number and Name

Test 2.4.1 – Data Lane HS-RX TD-TERM-EN Value

Purpose

To verify that the time required the DUT's Data Lane receiver to enable its HS line termination (T_CLK-TERM-EN) is within the conformance limits.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remains the same.

Parameters

Same as Test 2.4.6 Clock Lane T_CLK-TERM-EN on page 191.

Results

For all Data Lanes, the T_D-TERM-EN must be greater than the time for Dn to reach 450 mV, and less than (35 ns + 4*UI) ns.

Table 81 Parameters in the result table for "Test 2.4.1 Data Lane T_HS-TERM-EN"

Parameter name	Parameter description
Result	▪ Pass the termination is enabled within the specified time. ▪ Fail: the termination was not enabled on time.
Signal	Signal that is being tested.
Timing [ns]	Time that the DUT took to enable the termination.
Max Spec [ns]	Maximum T_CLK-TERM-EN according to the specification.

LP Tests

Test 2.1.1 V_IH Sensitivity Clock

CTS Test Number and Name

Test 2.1.1 – LP-RX Logic 1 Input Voltage (V_IH)

Purpose

To verify that the DUT's LP receiver can properly detect Logic 1 voltage levels as low as the minimum required conformance limit (V_IH).

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remains the same.

NOTE

The DUT's LP-RX Logic-1 Detection Threshold must be less than or equal to 880 mV (for DUTs supporting a maximum HS rate <= 1.5Gbps) or 740 mV (for DUTs supporting a maximum HS rate > 1.5Gbps) in order to satisfy the conformance requirements for VIH. This demonstrates that the DUT can detect logic levels at least as low as 880 mV (or 740 mV), which is the minimum voltage level a receiver is required to detect as a Logic 1.

Parameters

Table 82 Parameters used in Test 2.1.1 V_IH Sensitivity Clock

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Max Tested Value	Maximum Input Voltage (V_IH).

Min Tested Value	Minimum Input Voltage (V_IH).
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Steps	Specifies the number of steps that are tested between the Start Value and the End Value for tests in which a range of values is tested.

Results

- For DUTs supporting a max HS rate <= 1.5Gbps the V_IH must be less than or equal to 880 mV.
- For DUTs supporting a max HS rate > 1.5Gbps) the V_IH must be less than or equal to 740 mV.

Table 83 Parameters in the result table for "Test 2.1.1 V_IH Sensitivity Clock"

Parameter name	Parameter description
Result	▪ Pass: the minimum V_IH that the DUT can handle without errors is smaller than or equal to the minimum value in the specification. ▪ Fail: the minimum V_IH that the DUT can handle without errors is larger than the minimum value in the specification.
Min Passed V_IH [mV]	Minimum input high-level voltage, VIH, is the voltage at which the receiver is required to detect a high state in the input signal.
Min Tested V_IH [mV]	Minimum tested V_IH.
Min Spec [mV]	Minimum V_IH for which the DUT must receive the data without errors according to the specification.

Test 2.1.2 V_IL Sensitivity Clock

CTS Test Number and Name

Test 2.1.2 – LP-RX Logic 0 Input Voltage, Non-ULP State (V_IL)

Purpose

To verify that the DUT's LP receiver can correctly detect Logic 0 voltage levels as high as the maximum required conformance limit (V_IL), when in the non-ULP state.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remains the same.

Parameters

Same as Test 2.1.1 V_IH Sensitivity Clock on page 194.

Results

The V_IL must be greater than or equal to 550 mV.

Table 84 Parameters in the result table for "Test 2.1.2 V_IL Sensitivity Clock"

Parameter name	Parameter description
Result	▪ Pass: the maximum V_IL that the DUT can handle without errors is larger than or equal to the maximum value in the specification. ▪ Fail: the minimum V_IL that the DUT can handle without errors is smaller than the maximum value in the specification.
Max Passed V_IL [mV]	Maximum V_IL for which the tests data was transmitted without errors.
Max Tested V_IL [mV]	Maximum tested V_IL.
Max Spec V_IL [mV]	Maximum V_IL for which the DUT must receive the data without errors according to the specification.

Test 2.1.4 V_HYST Sensitivity Clock

CTS Test Number and Name

Test 2.1.4 – LP-RX Input Hysteresis (V_HYST)

Purpose

To verify that the Input Hysteresis value (V_HYST) of the DUT's LP receiver is within the conformance limits.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remains the same.

Parameters

Table 85 Parameters used in Test 2.1.4 V_HYST Sensitivity Clock

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Initial Voltage Step Size	Initial voltage step size used at the beginning of the test, when the test value is close to the minimum value according to specification.
Maximum test Voltage	Maximum Input Hysteresis (V_HYST).
Minimum test Voltage	Minimum Input Hysteresis (V_HYST).
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Voltage Step Size	The step size by which the voltage is increased/decreased while running test.

Results

For all measured Lanes:

- The V_HYST-V_IH(Dp) must be greater than or equal to 25 mV.
- The V_HYST-V_IH(Dn) must be greater than or equal to 25 mV.
- The V_HYST-V_IL(Dp) must be greater than or equal to 25 mV.
- The V_HYST-V_IL(Dn) must be greater than or equal to 25 mV.

Table 86 Parameters in the result table for "Test 2.1.4 V_HYST Sensitivity Clock"

Parameter name	Parameter description
Result	▪ Pass: the Input Hysteresis value of the DUT's LP receiver is within the conformance limits. ▪ Fail: the Input Hysteresis value of the DUT's LP receiver is not within the conformance limits.
Min Passed V_IH [mV]	Minimum V_IH supported by the DUT.
Min Spec V_IH [mV]	Minimum V_IH that the DUT must support according to the specification.
V_IH Recover [mV]	V_IH value for which the DUT stops reporting errors after it failed.
V_HYST [mV]	Actual value of the DUT's V_HYST as measured during the test
Min Spec V_HYST [mV]	Minimum V_HYST of the DUT according to the specification.

Test 2.1.4 V_HYST Dynamic Clockp

CTS Test Number and Name

Test 2.1.4 – LP-RX Input Hysteresis (V_HYST)

Purpose

To verify that the Input Hysteresis value (V_HYST) of the DUT's LP receiver is within the conformance limits.

Dependencies

All calibrations are required.

In order to run this test, it is necessary to know the minimum V_IH and maximum V_IL values that the DUT supports. If Test 2.1.1 V_IH Sensitivity Clock (and Data0–Data3) and Test 2.1.2 V_IL Sensitivity Clock (and Data0–Data3) are run before this test procedure, the parameters "Tested V_IH" and "Tested V_IL" are filled automatically with the corresponding values. It is also possible to input these parameters manually before the test starts.

Parameters

Table 87 Parameters used in Test 2.1.4 V_HYST Dynamic Clockp

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Interference Frequency	Interference frequency used during this test step.
Interference Step Size	The step size by which the interference voltage is increased/decreased while running test.
Maximum Interference Amplitude (Vpk)	Maximum interference amplitude for which the DUT was able to receive the test sequence without errors for the given common-mode and differential voltage levels.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Tested VIH	Minimum V_IH supported by the DUT.
Tested VIL	Maximum V_IL supported by the DUT.
VIH during VIL Test	The Value obtained by V_IH while running V_IL test.
VIL during VIH Test	The Value obtained by V_IL while running V_IH test.

Results

Table 88 Parameters in the result table for "Test 2.1.4 V_HYST Dynamic Clockp"

Parameter name	Parameter description
Result	▪ Pass: the Input Hysteresis value of the DUT's LP receiver is within the conformance limits. ▪ Fail: the Input Hysteresis value of the DUT's LP receiver is not within the conformance limits.
Max Passed Interference V_IH [mV]	Maximum V_IH single ended interference supported by the DUT.
Min Failed Interference V_IH [mV]	Minimum V_IH single ended interference that caused the DUT to fail.
Max Passed Interference V_IL [mV]	Maximum V_IL single ended interference supported by the DUT.
Min Failed Interference V_IL [mV]	Minimum V_IL single ended interference that caused the DUT to fail.
Min Spec [mV]	Minimum single ended interference that the DUT must be able to handle according to the specification.

Test 2.1.4 V_HYST Dynamic Clockn

CTS Test Number and Name

Test 2.1.4 – LP-RX Input Hysteresis (V_HYST)

Purpose

To verify that the Input Hysteresis value (V_HYST) of the DUT's LP receiver is within the conformance limits.

Dependencies

All calibrations are required.

In order to run this test, it is necessary to know the minimum V_IH and maximum V_IL values that the DUT supports. If Test 2.1.1 V_IH Sensitivity Clock (and Data0–Data3) and Test 2.1.2 V_IL Sensitivity Clock (and Data0–Data3) are run before this test procedure, the parameters "Tested VIH" and "Tested VIL" are filled automatically with the corresponding values. It is also possible to input these parameters manually before the test starts.

Parameters

Same as Test 2.1.4 V_HYST Dynamic Clockp on page 198.

Results

Table 89 Parameters in the result table for "Test 2.1.4 V_HYST Dynamic Clockn"

Parameter name	Parameter description
Result	▪ Pass: the Input Hysteresis value of the DUT's LP receiver is within the conformance limits. ▪ Fail: the Input Hysteresis value of the DUT's LP receiver is not within the conformance limits.
Max Passed Interference V_IH [mV]	Maximum V_IH single ended interference supported by the DUT.
Min Failed Interference V_IH [mV]	Minimum V_IH single ended interference that caused the DUT to fail.
Max Passed Interference V_IL [mV]	Maximum V_IL single ended interference supported by the DUT.
Min Failed Interference V_IL [mV]	Minimum V_IL single ended interference that caused the DUT to fail.
Min Spec [mV]	Minimum single ended interference that the DUT must be able to handle according to the specification.

Test 2.1.5 LP-RX Minimum Pulse Width Response T_Min-RX Clock

CTS Test Number and Name

Test 2.1.5 – LP-RX Minimum Pulse Width Response (T_MIN-RX)

Purpose

To verify that the DUT's LP receiver can detect LP pulses with the minimum required duration.

Parameters

Table 90 Parameters used in Test 2.1.5 LP-RX Minimum Pulse Width Response T_Min-RX Clock

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Max Pulse Width	The maximum Pulse width for which the sequence can be received without error.
Min Pulse Width	The minimum Pulse width for which the sequence can be received without error.
Offline	Offline mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Steps	Specifies the number of steps that are tested between the Start Value and the End Value for tests in which a range of values is tested.
V_OH	Output high voltage.
V_OL	Output low voltage.

Results

The smallest T_LPX value for which the DUT can consistently receive the test sequence without errors must be less than or equal to 20 ns.

Table 91 Parameters in the result data table "Test 2.1.5 LP-RX Minimum Pulse Width Response T_Min-RX Clock"

Parameter name	Parameter description
Result	▪ Pass: the minimum pulse duration detected by the DUT is smaller than or equal to the specification value. ▪ Fail: the minimum pulse duration detected by the DUT is larger than the specification value.
Min Passed [ns]	Minimum pulse duration detected by the DUT
Min Spec [ns]	Minimum pulse duration according to the specification.

Test 2.1.7 LP-RX Interference Tolerance V_INT and f_INT Clock

CTS Test Number and Name

Test 2.1.7 LP-RX Interference Tolerance (V_INT and f_INT)

Purpose

To verify that the DUT Data Lane LP receiver can tolerate interference with voltage and frequency values within the conformance limits.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

Parameters

Table 92 Parameters used in Test 2.1.7 LP-RX Interference Tolerance V_INT and f_INT Clock

Parameter	Description
BER Limit	Limit used for bit-error-ratio test.
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Maximum Test Voltage	Maximum voltage of V_INT.

Minimum Test Voltage	Minimum voltage of V_INT.
Offline	Offline mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Steps	Specifies the number of steps that are tested between the Start Value and the End Value for tests in which a range of values is tested.
Test Frequencies	Defines the valid frequencies for the test.
V_OH	V_OH is the Thevenin output, high-level voltage in the high-level state, when the pad pin is not loaded
V_OL	V_OL is the Thevenin output, low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low-level state.

Results

In all test cases the DUT must be able to successfully receive the test sequence in the presence of the interfering signaling.

Table 93 Parameters in the result data table Test 2.1.7 LP-RX Interference Tolerance V_INT and f_INT Clock"

Parameter name	Parameter description
Result	▪ Pass: the DUT received the test sequence without errors. ▪ Fail: the DUT failed to receive the test sequence.
Interference Frequency [MHz]	Interference frequency used during this test step.
Max Passed [mV]	Maximum interference amplitude for which the DUT was able to receive the test sequence without errors for the given LP levels.
Max Spec [mV]	Maximum interference amplitude for which the DUT must be able to receive the test sequence without errors according to the specification.

Test 2.1.1 V_IH Sensitivity Data

CTS Test Number and Name

Test 2.1.1 – LP-RX Logic 1 Input Voltage (V_IH)

Purpose, Dependencies, Parameters and Result

Same as Test 2.1.1 V_IH Sensitivity Clock on page 194.

Test 2.1.2 V_IL Sensitivity Data

CTS Test Number and Name

Test 2.1.2 – LP-RX Logic 0 Input Voltage, Non-ULP State (V_IL)

Purpose, Dependencies, Parameters and Result

Same as Test 2.1.2 V_IL Sensitivity Clock on page 196.

Test 2.1.4 V_HYST Sensitivity Data

CTS Test Number and Name

Test 2.1.4 V_HYST Sensitivity Data0p

Purpose, Dependencies, Parameters and Result

Same as Test 2.1.4 V_HYST Sensitivity Clock on page 197.

Test 2.1.4 V_HYST Dynamic Datap

CTS Test Number and Name

Test 2.1.4 V_HYST Dynamic Data0p

Purpose Dependencies, Parameters and Result

Same as Test 2.1.4 V_HYST Dynamic Clockp on page 198.

Test 2.1.4 V_HYST Dynamic Datan

CTS Test Number and Name

Test 2.1.4 V_HYST Dynamic

Purpose Dependencies, Procedure, Parameters and Result

Same as Test 2.1.4 V_HYST Dynamic Clockn on page 199.

Test 2.1.5 LP-RX Minimum Pulse Width Response T_Min-RX Data

CTS Test Number and Name

Test 2.1.5 LP-RX Minimum Pulse Width Response (T_Min-RX)

Purpose, Dependencies, Procedure, Parameters and Result

Same as Test 2.1.5 LP-RX Minimum Pulse Width Response T_Min-RX Clock on page 201.

Test 2.1.7 LP-RX Interference Tolerance V_INT and f_INT Data0

CTS Test Number and Name

Test 2.1.7 LP-RX Interference Tolerance (V_INT and f_INT)

Purpose, Dependencies, Parameters and Result

Same as Test 2.1.7 LP-RX Interference Tolerance V_INT and f_INT Clock on page 202.

Behavioral Tests

Test 2.2.1 Init. Period T_INIT

CTS Test Number and Name

Test 2.2.1 – LP-RX Initialization period (T_INIT)

Purpose

To verify that the Slave meets the minimum T_INIT requirement. Each link has a master and a slave side. The master always generates the clock and is the main data source. The slave always receives the clock signal and is the main data receiver.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

For this test the LP calibrations are also required. If an IberReader interface is being used, please make sure that its ResetDut function performs a full restart of the DUT. As the DUT will enter ULPS during this test, a reset of the bit and error counters is not enough.

Procedure

NOTE This test is available only for the M8195A module.

It is required that the Master DUT initializes the Slave DUT by driving LP11 for a period longer than T_INIT (100 µs). If the initialization period is shorter or non-existent, all transitions on the line will be ignored by the Slave.

To implement the test:

- Click Run to send valid HS or LP data. Refer to Performing Procedures on page 31 to know how to run procedures.
- The software causes an observable result after T_INIT <100 µs. Observe whether the DUT has received the test data or not.
- Restart the DUT. The software slowly increases T_INIT (e.g. by steps of 10 µs) up to the point where the DUT receives the data properly.
- The DUT passes the test if minimum T_INIT ≥ 100 µs, otherwise it fails.

Parameters

Table 94 Parameters used in Test 2.2.1 Init. Period T_INIT

Parameter	Description
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Maximum Tested Value	Maximum Init. Period T_INIT.
Minimum Tested Value	Minimum Init. Period T_INIT.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Steps	Specifies the number of steps that are tested between the Start Value and the End Value for tests in which a range of values is tested.
Test Sequence	The name of the sequence file to be used for the test. It does not matter if it contains HS or LP data, as long as it produces an observable result.

Results

The value of T_INIT must be greater than the minimum protocol-specific conformance limit.

Table 95 Parameters in the result table for "Test 2.2.1 Init. Period T_INIT

Parameter name	Parameter description
Result	▪ Pass: the value of T_Init is greater than the minimum limit defined in the specification. ▪ Fail: one or more test cases failed.
TInit [ms]	TINIT is considered a protocol-dependent parameter and the minimum value of T_Init according to the specification is 100 ns.

Test 2.2.2 ULPS Exit TWakeup

CTS Test Number and Name

Test 2.2.2 – ULPS Exit: LP-RX T_WAKEUP Timer Value

Purpose

To verify that the Slave meets the minimum T_Wakeup requirement.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

For this test the LP calibrations are also required. If an IberReader interface is being used, please make sure that its ResetDut function performs a full restart of the DUT. As the DUT will enter ULPS during this test, a reset of the bit and error counters is not enough.

Procedure

When in ULPS mode, the Slave DUT should wait for an Exit Sequence formed by a Mark-1 State (LP-10) with a minimum duration of TWakeup = 1 ms, followed by a Stop State (LP-11). If the duration of TWakeup is shorter than 1 ms, the Slave should remain in ULPS mode.

To implement the test:

- Click Run. The DUT is set to ULPS. Refer to Section 1.2 Executing the Tests how to run procedures.
- The software sends an Exit Sequence with T_Wakeup = 0 ms and sends valid data.
- Observe that the DUT stays in ULPS state (valid data is ignored).
- The software gradually increases TWakeup (e.g. by 200 µs)
- The previous step is repeated until the DUT comes out of ULPS, where the valid data causes an observable result.
- If TWakeup ≥ 1 ms the DUT has passed the test, otherwise it has failed

Parameters

Table 96 Parameters used in Test 2.2.2 ULPS Exit TWakeup

Parameter	Description
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Maximum Tested Value	Maximum T_Wakeup.
Minimum Tested value	Minimum T_Wakeup.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.
Steps	Specifies the number of steps that are tested between the Start Value and the End Value for tests in which a range of values is tested.
ULPS Entry and exit Sequence	A ULPS entry sequence is sent to the DUT, followed by a Mark-1/Stop plus a valid HS burst on all lanes using nominal voltage levels. ULP Exit Sequence.is active high signal, asserted when ULP state is active and the protocol is ready to leave ULP state.
ULPS Entry Sequence	A ULPS entry sequence is sent to the DUT, followed by a Mark-1/Stop plus a valid HS burst on all lanes using nominal voltage levels.

Results

The DUT must exit the ULPS mode.

Table 97 Parameters in the result table for "Test 2.2.2 ULPS Exit TWakeup"

Parameter name	Parameter description
Result	▪ Pass: the value of T_Wakeup is greater than or equal to the minimum limit defined in the specification. ▪ Fail: the value of T_ Wakeup is smaller than the minimum limit defined in the specification.
TWakeUP [ms]	Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS. Its minimum value is 1 ms.

Test 2.2.3 Clock Invalid or Aborted Escape Entry

CTS Test Number and Name

Test 2.2.3 Clock Lane LP-RX Invalid/Aborted ULPS Entry

Purpose

To verify that the Slave ignores invalid/aborted ULPS Clock Lane Entry Sequences.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

For this test the LP calibrations are also required. If an IberReader interface is being used, please make sure that its ResetDut function performs a full restart of the DUT. As the DUT may enter ULPS during this test, a reset of the bit and error counters is not enough.

Procedure

Being in Stop State (LP-11), the Clock Lane ULPS is set via TX-ULPS-Rqst State (LP-10) and then TX-ULPS State (LP-00). Any sequence other than LP-11/10/00 should not bring the Clock Lane into ULPS, neither erroneous sequences such as LP11/10/01 and LP11/10/11 nor a valid Data Lane ULPS Entry Sequence (LP11/10/00/01/00).

To implement the test:

- Click Run to transmit a test sequence to the DUT. Refer to Performing Procedures on page 31 to know how to run procedures.
- For all three mentioned invalid ULPS Clock Lane Entry Sequences, verify that the Clock Lane does not enter ULPS. The software sends the invalid sequence and then valid HS data, which should be processed by the DUT.

Parameters

Table 98 Parameters used in Test 2.2.3 Clock Invalid or Aborted Escape Entry

Parameter	Description
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.

Results

In both cases, the integrity of the received data, as well as the overall operation of the DUT must not negatively affected by the presence of the invalid ULPS Entry sequences.

Table 99 Parameters in the result table for "Test 2.2.3 Clock Invalid or Aborted Escape Entry"

Parameter name	Parameter description
Result	▪ Pass: the test data was received by the DUT, which therefore did not enter ULPS. ▪ Fail: the test data was not received by the DUT.
Test Pattern	The final bit pattern received by the DUT.

Test 2.2.4 Data Invalid or Aborted Escape Entry

CTS Test Number and Name

Test 2.2.4 – Data Lane LP-RX Invalid/Aborted Escape Mode Entry.

Purpose

To verify that invalid Data Lane Escape Sequences are ignored by the Slave.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

For this test the LP calibrations are required. If an IberReader interface is being used, please make sure that its ResetDut function performs a full restart of the DUT. As the DUT may enter ULPS during this test, a reset of the bit and error counters is not enough.

Procedure

NOTE This test is considered as informative in CTS, the result graph cannot be drawn from the behavior of the DUT during the test run.

Any Escape-Entry sequence that has a Stop state (LP-11) other than the valid LP-11/10/00/01/00 sequence, e.g. LP-11/10/00/01/11 or LP-11/10/11/11/11 should be ignored by the Data Lane:

To implement the test:

- Click Run to transmit a test sequence to the DUT.Refer to Performing Procedures on page 31to know how to run procedures.
- For both mentioned invalid Data Lane Escape Entry Sequences, verify that the Data Lane ignores the invalid sequences. The software sends the invalid sequence between HS Bursts on the Data Lane, but the HS data should be received by the DUT.

Parameters

Same as Test 2.2.3 Clock Invalid or Aborted Escape Entry

Results

In both cases, the integrity of the received data, as well as the overall operation of the DUT does not negatively affected by the presence of the invalid/aborted Data Lane Escape Mode Entry sequences.

Table 100 Parameters in the result table for "Test 2.2.4 Data Invalid or Aborted Escape Entry"

Parameter name	Parameter description
Result	▪ Pass: the test data was received by the DUT, therefore did not enter ULPS. ▪ **Fail:** the test data was not received by the DUT.
Test Pattern	The final bit pattern received by the DUT.

Test 2.2.5 Data Invalid or Aborted Escape Command

CTS Test Number and Name

Test 2.2.5 – Data Lane LP-RX Invalid/Aborted Escape Mode Command

Purpose

To verify that the Slave ignores an invalid Entry Command in Escape Mode, which waits for the Transmitter to return to Stop State.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

For this test the LP calibrations are required. If an IberReader interface is being used, please make sure that its ResetDut function performs a full restart of the DUT. As the DUT may enter ULPS during this test, a reset of the bit and error counters is not enough.

Procedure

Using the ULPS Entry Command as a base for the corrupted command sequences, each valid Escape Entry sequence will have an LP-11 state aborting the Escape mode command. The invalid sequences should be ignored by the Data Lane.

To implement the test:

- Click Run to transmit a test sequence to the DUT. Refer to Performing Procedures on page 31 to know how to run procedures.
- For all the following invalid Escape-Entry command sequences, the software send each followed by valid HS data. The data lane must ignore the invalid sequences and the valid data is observable.

1 Valid Escape Mode Entry] + LP-01/00/01/00/01/00/10/00/10/00/10/00/10/00/01/11 + [Stop]

2 [Valid Escape Mode Entry] + LP-01/00/01/00/01/00/10/00/10/00/10/00/10/11/11/11 + [Stop]

3 [Valid Escape Mode Entry] + LP-01/00/01/00/01/00/10/00/10/00/10/11/11/11/11/11 + [Stop]

4 [Valid Escape Mode Entry] + LP-01/00/01/00/01/00/10/00/10/11/11/11/11/11/11/11 + [Stop]

5 [Valid Escape Mode Entry] + LP-01/00/01/00/01/00/10/11/11/11/11/11/11/11/11/11 + [Stop]

6 [Valid Escape Mode Entry] + LP-01/00/01/00/01/11/11/11/11/11/11/11/11/11/11/11 + [Stop]

7 [Valid Escape Mode Entry] + LP-01/00/01/11/11/11/11/11/11/11/11/11/11/11/11/11 + [Stop]

8 [Valid Escape Mode Entry] + LP-01/11/11/11/11/11/11/11/11/11/11/11/11/11/11/11 + [Stop]

Parameters

Table 101 Parameters used in Test 2.2.5 Data Invalid or Aborted Escape Command

Parameter	Description
Entry Command Pattern	Escape Entry Code used during the test (default is ULPS Escape Entry Code).
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.

Results

In all cases, the integrity of the received data, as well as the overall operation of the DUT must not negatively affected by the presence of the invalid/aborted ULPS command sequences.

Table 102 Parameters in the result data table "Test 2.2.5 Data Invalid/Aborted Escape Command"

Parameter name	Parameter description
Result	▪ Pass: the test data was received by the DUT, which therefore did not enter ULPS. ▪ Fail: the test data was not received by the DUT.
Test Pattern	The final bit pattern received by the DUT.

Test 2.2.7 Data Post-Trigger-Command

CTS Test Number and Name

Test 2.2.7 – Data Lane LP-RX Escape Mode, Ignoring of Post-Trigger-Command Extra Bits.

Purpose

To verify that the DUT LP-RX ignores any extra bits received following a Trigger Command.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

For this test. The LP calibrations are required. If an IberReader interface is being used, please make sure that its ResetDut function performs a full restart of the DUT. As the DUT may enter ULPS during this test, a reset of the bit and error counters is not enough.

Procedure

An Escape mode sequence containing a Trigger sequence followed by extra post-command bits, which is a combination of an extra byte of data after the Trigger command, and the ULPS Entry command as an extra byte is used. The invalid ULPS command byte should be ignored by the DUT.

To implement the test:

- Click Run to transmit a test sequence to the DUT. Refer to Performing Procedures on page 31 to know how to run procedures.
- For each of the available Trigger commands (Reset-Trigger, Unknown-3, Unknown-4, Unknown-5), the software sends the appropriate Escape Mode Entry sequence + Reset-Trigger command (01100010) + ULPS command (00011110) on all Data Lanes followed by the valid HS data.
- Verify that valid data is received at the DUT.

Parameters

Table 103 Parameters used in Test 2.2.7 Data Post-Trigger-Command

Parameter	Description
Extra bits	Bits added after the valid Trigger Command and before the Mark-1/Stop Exit sequence (default is ULPS Escape Entry Code).
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension *Setup.ala* in the directory.

Results

In all test cases the DUT must ignore all bits occurring after the last bit of the Trigger Command, by observing that the DUT properly received the image data stream without error.

Table 104 Parameters in the result table for "Test 2.2.7 Data Post-Trigger-Command"

Parameter name	Parameter description
Result	▪ Pass: the test data was received by the DUT, which therefore did not enter ULPS. ▪ Fail: the test data was not received by the DUT.
Test Pattern	The final bit pattern received by the DUT.

Test 2.2.8 Data LP-RX Escape Mode Unsupported or Unassigned Commands

CTS Test Number and Name

Test 2.2.8 Data LP-RX Escape Mode Unsupported/Unassigned Commands

Purpose

An Entry Command Pattern consists of 8 bits, therefore there are 256 possible combinations. Of these, one is assigned to the Low-Power Data Transmission Mode (11100001), one to the Ultra-Low-Power State Mode (00011110) and one to the Reset Trigger (01100010). The remaining 253 combinations are either Undefined modes (2), Unknown triggers (3), or Unassigned (248), and must be ignored by the DUT. This test verifies that all Unsupported and Unassigned commands are ignored by the DUT.

Dependencies

Ensure that the Skew Calibration procedure and the Inter Module Skew Calibration have been performed before the actual test starts. If the Skew Calibration procedure and Inter Module Skew Calibration have already been conducted in the course of running another HS test, the calibrations are still valid and do not need to be repeated as long as the settings under the Configuration Panel remain the same.

For this test the LP calibrations are also required. If an IberReader interface is being used, please make sure that its ResetDut function performs a full restart of the DUT. As the DUT may enter ULPS during this test, a reset of the bit and error counters is not enough.

Procedure

An Escape mode sequence containing an unassigned Escape Command, which is combination of 248 unassigned command codes, is used. The invalid undefined/unknown/unassigned command codes should be ignored by the DUT.

To implement the test:

- Click Run to transmit a test sequence to the DUT. Refer to Performing Procedures on page 31 to know how to run procedures.
- For each of the available 248 unassigned command codes, the software sends the appropriate Escape Mode Entry sequence + the Undefined 1 command code (10011111), on all Data Lanes followed by the valid HS data.
- The software repeats the previous step by replacing the Undefined 1 command code with Undefined 2 command code (11011110); Trigger commands (Reset Trigger, Unknown-3, Unknown-4, Unknown-5) and the 248 unassigned command codes followed by the valid HS data.
- Verify that valid data is received at the DUT

Parameters

Table 105 Parameters used in Test 2.2.8 Data LP-RX Escape Mode Unsupported or Unassigned Commands

Parameter	Description
HS Frequency	Frequency of the High-Speed operation mode during the execution of a procedure. To be chosen from the frequencies specified during the DUT configuration.
Offline	Offline Mode.
Setup file name	The PPI BER Reader searches for a file name with the extension Setup.ala in the directory.

Results

For all test cases, the DUT must ignore the unsupported/unassigned command, and successfully receives the image data stream.

Table 106 Parameters in the result table for "Test 2.2.8 Data LP-RX Escape Mode Unsupported/Unassigned Commands"

Parameter name	Parameter description
Result	▪ Pass: the test data was received by the DUT, which therefore did not enter ULPS. ▪ Fail: the test data was not received by the DUT.
Test Pattern	The final bit pattern received by the DUT.

6 SCPI Plug-in Interface

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SCPI Commands / 232

Description of already generated generic commands for plug-ins adapted to the new requirements based on the sub-model approach.

The structure of an identifier attached to a SCPI command contains now additional delimiter. A full qualified identifier has following structure:

'PluginName#SubModel:Location&FunctionalBlock.Parameter'

In many cases it is not necessary to add a full qualified identifier to every SCPI command. For example a plug-in is implemented a singleton or a location/parameter exists on once. Later on a detailed description will explain the usage and simplification of an identifier that comes along with a SCPI command for addressing plug-ins / sub-models / parameters and so on.

The identifier appended to every SCPI command should be optional to avoid SCPI commands like :PLUGin:rootnode:BREak ' ' // empty identifier

Architecture of a plug-in / sub-model concept

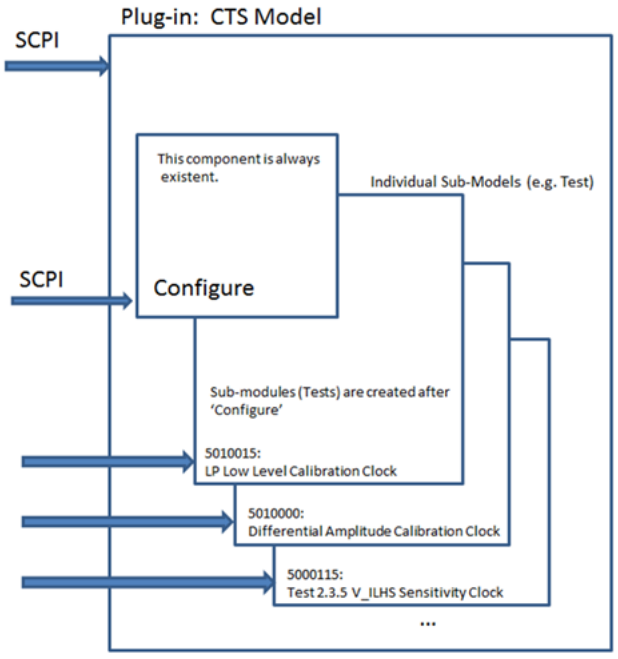

Figure 48 Plug-in / Sub-Model approach

Sorting and Using the SCPI Commands

This chapter describes the order in which the SCPI commands/queries must be sorted and run, which is in accordance with the work-flow on the MIPI D-PHY CTS plug-in user interface.

Following procedure describes how to start a new plug-in instance and how to run tests on the active instance.

1 On the SCPI Editor window, run the catalog query (**:PLUGin:CATalog?**) to check for the existing plug-ins in the M8070B software and to identify the correct plug-in string name.

-> :PLUGin:CATalog?

<- "Pattern Capture","Script Editor","DUT Control Interface","Error Ratio","Jitter Tolerance","Jitter Tolerance Template Editor","Output Level","Output Timing","Eye Diagram","MIPI C-PHY CTS","MIPI D-PHY CTS","MIPI C-PHY Editor","MIPI D-PHY Editor"

2 MIPI D-PHY CTS tests can be run only on the MIPI D-PHY CTS plug-in, so from the query result, use the plug-in string name "MIPI D-PHY CTS".

3 Create a new MIPI D-PHY CTS plug-in instance using the :PLUGin:DPHYTests:NEW command. For example, consider the name of the new MIPI D-PHY CTS plug-in instance to be 'MIPI D-PHY CTS 1'.

:PLUGin:DPHYTests:NEW 'MIPI D-PHY CTS 1'

4 Keysight recommends that prior to configuring the tests, you must manually set up the connection strings to the instrument, either in offline mode or online mode. The MIPI D-PHY CTS plug-in stores the last setting internally. If you have completed the connection setup, skip to step 6 else you must set the configuration parameters remotely. Run the :PLUGin:DPHYTests:PARameter:LIST? query to check for the list of parameters.

-> :PLUGin:DPHYTests:PARameter:LIST? 'MIPI D-PHY CTS 1'

<-
":TP1.Link&Connection.OfflineMode","1",":TP1.Link&Connection.AwgModel","M8190",":TP1.Link&Connection.AwgMode","FOUR",":TP1.Link&Connection.NumberOfAwgs","AWG2",":TP1.Link&AWG Setup.AwgHostIpAddress","127.0.0.1",":TP1.Link&AWG Setup.AwgClockSyncHiSlip","hislip0",":TP1.Link&AWG Setup.AwgOneHiSlip","hislip1",":TP1.Link&AWG Setup.AwgTwoHiSlip","hislip2",":TP1.Link&AWG Setup.AwgThreeHiSlip","hislip3",":TP1.Link&AWG Setup.AwgFourHiSlip","hislip3",":TP1.Link&Oscilloscope Setup.OscilloscopeOfflineMode","1",":TP1.Link&Oscilloscope

Setup.OscilloscopeAddress","TCPIP0::121.0.0.1::inst0::INSTR",":TP1.System&Global.TestMode","COMpliance",":TP1.System&Global.SpecVersion","v1_20",":TP1.System&Global.NumberOfDataLanes","LANE1",":TP1.System&Global.SyncWord","0xB8",":TP1.System&Global.LsbFirst","1",":TP1.System&Global.LpDataRate","10000000",":TP1.System&Global.HsDataRate","800000000",":TP1.System&Global.TriggeredStart","0",":TP1.System&Global.ManualDeskew","0",":TP1.System&Global.RestartSequenceAfterReset","0",":TP1.System&Global.RestartSequenceBeforeReset","0",":TP1.System&Global.PatternMode","COMpliance",":TP1.System&Global.AllDataLanesSimultaneously","0",":TP1.System&Global.HsModeDataFile","C:\ProgramData\BitifEye\Pattern\DPhy\HsCompliancePattern.dat",":TP1.System&Global.HsModeSequenceFile","C:\ProgramData\BitifEye\Pattern\DPhy\Hs.seq",":TP1.System&Global.HsModeFileName","HsCompliancePattern.dat",":TP1.System&Global.LpModeDataFile","C:\ProgramData\BitifEye\Pattern\DPhy\LpCompliancePattern.dat",":TP1.System&Global.LpModeSequenceFile","C:\ProgramData\BitifEye\Pattern\DPhy\Lp.seq",":TP1.System&Global.LpModeFileName","LpCompliancePattern.dat",":TP1.System&Global.UlpModeDataFile","C:\ProgramData\BitifEye\Pattern\DPhy\LpCompliancePattern.dat",":TP1.System&Global.UlpModeSequenceFile","C:\ProgramData\BitifEye\Pattern\DPhy\Ulp.seq",":TP1.System&Global.UlpModeFileName","LpCompliancePattern.dat",":TP1.System&Global.BehavioralSequenceFile","C:\ProgramData\BitifEye\Pattern\DPhy\Behavioral.seq",":TP1.System&Global.BehavioralSequenceFileName","Behavioral.seq",":TP1.System&Global.IsiFile","C:\ProgramData\BitifEye\SParameter\DPhy\IsiFile.s4p",":TP1.System&Global.IsiFileName","IsiFile.s4p",":TP1.System&Global.BerReader","OFFline",":TP1.System&Global.BerLimit","_1_06",":TP1.System&Global.BerReaderAddress","",":TP1.System&Global.Mipi Protocol","DSI",":TP1.System&Signal Levels.LowPowerHighLevel","1.2",":TP1.System&Signal Levels.LowPowerLowLevel","0",":TP1.System&Signal Levels.HighSpeedCommonLevel","0.20000000000000001",":TP1.System&Signal Levels.HighSpeedDifferentialSwing","0.20000000000000001",":TP1.System&Protocol Timings.ClockPrepareLength","7.0000000000000005E-08",":TP1.System&Protocol Timings.ClockZeroLength","2.9999999999999999E-07",":TP1.System&Protocol Timings.ClockPreLength","1.2499999999999999E-08",":TP1.System&Protocol

Timings.ClockPostLength","7.0000000000000005E-08",":TP1.System&Protocol
Timings.ClockTrailLength","8.0000000000000002E-08",":TP1.System&Protocol Timings.ClockMissLength","0",":TP1.System&Protocol
Timings.PrepareLength","6.3300000000000004E-08",":TP1.System&Protocol
Timings.ZeroLength","1.1230000000000001E-07",":TP1.System&Protocol
Timings.TrailLength","7.0000000000000005E-08",":TP1.System&Protocol
Timings.ExitLength","9.9999999999999995E-08",":TP1.System&Protocol
Timings.WakeupLength","0.10000000000000001",":TP1.System&Protocol Timings.InitLength","0.0001",":TP1.System&Protocol
Timings.InitialSkewCalLength","0.0001",":TP1.System&Protocol
Timings.PeriodicSkewCalLength","0.0001",":TP1.System&Protocol
Timings.SetTimingsToMin","",":TP1.System&Idle Voltage.Idle Voltage","0.29999999999999999"

If you wish to find the parameters associated with a calibration / test manually, run this command with the identifiers written in the following manner:

-> :PLUGin:DPHYTests:PARameter:LIST? 'MIPI D-PHY CTS 1#Skew Calibration Module 1'

<- ":TP1.System&Acquisition Parameters.PropertiesEditable","1",":TP1.System&Skew Calibration Module 1.Offline","1",":TP1.System&Skew Calibration Module 1.Use Infiniisim","0",":TP1.System&Skew Calibration Module 1.Transfer Function Chan1","DoNothing.tf2",":TP1.System&Skew Calibration Module 1.Transfer Function Chan2","DoNothing.tf2",":TP1.System&Skew Calibration Module 1.Skew Tolerance","1.1000000000000001E-11"

5 To set up / modify the value for one or more parameters, run the :PLUGin:DPHYTests:PARameter[:Value][?] command.

:PLUGin:DPHYTests:PARameter 'MIPI D-PHY CTS 1#:TP1.System&Global.HsDataRate', '2e9'

6 Once all required parameters are configured, run the :PLUGin:DPHYTests:CONFigure command. Based on your configuration, the list of calibrations and tests are created and the plug-in is ready to run the CTS tests.

7 To check the list of available calibrations and tests, run the :PLUGin:DPHYTests:LIST? query.

-> :PLUGin:DPHYTests:LIST?

<- "Skew Calibration Module 1","Amplifier Level Calibration Module 1 Gen 1 Clock Normal","Amplifier Level Calibration Module 1 Gen 2 Clock Complement","Skew Calibration Module 2","Amplifier Level Calibration Module 2 Gen 1 Data0 Normal","Amplifier Level Calibration Module 2 Gen 2 Data0 Complement","Inter Module Skew Calibration","LP Level Calibration Clock","V_ILHS Calibration Clock","Differential Amplitude Cal Clock","LP Level Calibration Data0","V_ILHS Calibration Data0","e-Spike Calibration","Differential Amplitude Cal Data0","Intrinsic Jitter Calibration 800 Mbps","Test 2.3.1 Vcmrx Tolerance Clock","Test 2.3.2 V_IDTH and Test 2.3.3 V_IDTL Sensitivity Clock","Test 2.3.4 V_IHHS Sensitivity Clock","Test 2.3.5 V_ILHS Sensitivity Clock","Test 2.3.6 HS RX CM Interference 50-450 MHz Clock","Test 2.3.7 HS RX CM Interference beyond 450 MHz Clock","Test 2.3.8 HS RX Clock-to-Data Skew","Test 2.4.7 T_Clk-Prepare_Zero Compliance Procedure","Test 2.4.8 T_Clock-Settle - Clock Procedure","Test 2.4.9 T_Clk-Trail - Clock Procedure","Test 2.4.11a T_Clk-Pre - Clock Procedure","Test 2.4.11b T_Clk-Post - Clock Procedure","Test 2.3.1 Vcmrx Tolerance Data0","Test 2.3.2 V_IDTH and Test 2.3.3 V_IDTL Sensitivity Data0","Test 2.3.4 V_IHHS Sensitivity Data0","Test 2.3.5 V_ILHS Sensitivity Data0","Test 2.3.6 HS RX CM Interference 50-450 MHz Data0","Test 2.3.7 HS RX CM Interference beyond 450 MHz Data0","Test 2.3.8 HS RX Data-to-Clock Skew Data0","Test 2.4.2 T_HS-Prepare_Zero Compliance Procedure-Data0","Test 2.4.3 T_HS-Settle - Data0 Procedure","Test 2.4.4 T_HS-Trail - Data0 Procedure","Test 2.4.5 T_HS-Skip - Data0 Procedure","Test 2.4.6 Clock Lane T_CLK-TERM-EN","Test 2.4.1 Data0 Lane T_HS-TERM-EN","Test 2.1.1 V_IH Sensitivity Clock","Test 2.1.2 V_IL Sensitivity Clock","Test 2.1.4 V_HYST Sensitivity Clock","Test 2.1.4 V_HYST Dynamic Clockp","Test 2.1.4 V_HYST Dynamic Clockn","Test 2.1.5 LP-RX Minimum Pulse Width Response T_Min-RX Clock","Test 2.1.6 LP-RX Input pos. Pulse Rejection e_spike Clock","Test 2.1.6 LP-RX Input neg. Pulse Rejection e_spike Clock","Test 2.1.7 LP-RX Interference Tolerance VINT and fINT Clock","Test 2.1.1 V_IH Sensitivity Data0","Test 2.1.2 V_IL Sensitivity Data0","Test 2.1.4 V_HYST Sensitivity Data0","Test 2.1.4 V_HYST Dynamic Data0p","Test 2.1.4 V_HYST Dynamic Data0n","Test 2.1.5 LP-RX Minimum Pulse Width Response T_Min-RX Data0","Test 2.1.6 LP-RX Input pos. Pulse Rejection e_spike Data0","Test 2.1.6 LP-RX Input neg. Pulse Rejection e_spike Data0","Test 2.1.7 LP-RX Interference Tolerance VINT and fINT Data0","Test 2.2.1 Init. Period TINIT","Test 2.2.2 ULPS Exit TWAKEUP","Test 2.2.3 Clock Invalid or Aborted Escape Entry","Test 2.2.4 Data Invalid or Aborted Escape Entry","Test 2.2.5 Data Invalid or

Aborted Escape Command","Test 2.2.7 Data Post-Trigger-Command","Test 2.2.8 Data LP-RX Escape Mode Unsupported or Unassigned Commands"

8 To select a specific calibration / test remotely, run the :PLUGin:DPHYTests:SELect command.

9 To find the list of parameters specific to the selected calibration / test, run the :PLUGin:DPHYTests:PARameter:LIST? query.

-> :PLUGin:DPHYTests:PARameter:LIST? 'MIPI D-PHY CTS 1#Test 2.3.1 Vcmrx Tolerance Data0'

<- ":TP1.System&Acquisition Parameters.PropertiesEditable","1",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.Offline","1",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.Setup Filename","Data0_HS",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.HS Frequency","800000000",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.BER Limit","9.9999999999999995E-07",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.Min Tested Value","0.070000000000000007",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.Max Tested Value","0.33000000000000002",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.V_OD Array","0.26;1|0.07;1|0.22;-1|0.07;-1"

10 To set up / modify the value for one or more parameters specific to the selected test, run the :PLUGin:DPHYTests:PARameter[:Value][?] command.

-> :PLUGin:DPHYTests:PARameter:VALue "MIPI D-PHY CTS 1#Test 2.3.1 Vcmrx Tolerance Data0:TP1.System&BER Limit","7.99E-09"

NOTE You can modify the values of parameters specific to calibration / test names only when the **Mode:** option under **Receiver Test Configuration** is set to **Expert Mode.**

11 To run the selected calibration / test on the MIPI D-PHY CTS plug-in instance, run the PLUGin:DPHYTests:STARt command. If you wish to abort the test while it is running, run the PLUGin:DPHYTests:STOP command.

Following procedure describes remote commands that may be run while the CTS tests are running.

1 Setup the connection according to the connection diagram and description displayed on the MIPI D-PHY CTS plug-in user interface. While you may run the :PLUGin:DPHYTests:CONNection:DIAGram?

and :PLUGin:DPHYTests:CONNection:CDEScription? queries to obtain the image details of the connection diagram and the connection description, respectively; the connection setup details can also be viewed on the MIPI D-PHY CTS plug-in user interface.

2 While calibration / test procedures start running, you may optionally run the following queries/commands:

- :PLUGin:DPHYTests:RUN:PROGress? to check the progress of the calibration / test procedure that is currently running.
- :PLUGin:DPHYTests:RUN[:STATus]? to indicate whether a calibration / test procedure is in the running state or not.
- :PLUGin:DPHYTests:RUN:LOG? to view the logs for the calibration / test procedure that has just been run.
- :PLUGin:DPHYTests:RUN:MESSage? to view the running state (NotStarted, Running, Error and Finished) of the calibration / test procedure.
- :PLUGin:DPHYTests:RUN:HISTory:CLEar to clear the history information for any calibration / test runs.
- :PLUGin:DPHYTests:RUN:HISTory[:STATe]? to indicate whether a test run history and result is available (indicated by 1) or no tests were run (indicated by 0).

3 During test runs, several dialogs appear as pop-ups, which describe setting up the device and also display the PASS/FAIL information of the DUT. However, if you require that the CTS test run be fully automated, you must implement an IBerReader. For more details, see IBerReader Interface on page 247.

4 To obtain a list of the calibration / test results that have already been run, use the :PLUGin:DPHYTests:HISTory:CATalog? query.

-> :PLUGin:DPHYTests:HISTory:CATalog?

<- "Test 2.1.1 V_IH Sensitivity Clock_1","Test 2.1.4 V_HYST Sensitivity Data0_1","Test 2.1.4 V_HYST Sensitivity Data0_1"

5 To view the results for a calibration / test from the historic results displayed in the previous step, run the :PLUGin:DPHYTests:FETCh:RESult[:VALue]? query.

-> :PLUGin:DPHYTests:FETCh:RESult:VALue? 'MIPI D-PHY CTS 1#Test 2.1.1 V_IH Sensitivity Clock_1'

<- #41343<?xml version="1.0" encoding="utf-16"?><TestResults version="2.0"><TestResult><Summary><ProcedureName>Test 2.1.1 V_IH Sensitivity Clock</ProcedureName><ProcedureID>5000540</ProcedureID><Result>Passed</Result><DateTime>04/28/2017 15:53:10</DateTime><Duration>00:00:32.6220000</Duration><Descr

iption>This procedure test the LP Input High Voltage Sensitivity.</Description></Summary><ResultTables><ResultTable><Title>V_IH Tolerance_Clock</Title><Subtitle>Verify the V_IH tolerance</Subtitle><Name>V_IH Tolerance_Clock</Name><Parameters><Parameter name="Offline" value="True" /></Parameters><Columns><Column name="Result" unit="" recommendedExponent="0" width="13"><Value>pass</Value></Column><Column name="Min Passed V_IH" unit="V" precision="0" recommendedExponent="-3" width="8"><Value>0.6</Value></Column><Column name="Min Tested V_IH" unit="V" precision="0" recommendedExponent="-3" width="8"><Value>0.6</Value></Column><Column name="Min Spec V_IH" unit="V" precision="0" recommendedExponent="-3" width="8"><Value>0.74</Value></Column></Columns><cellColours><cellColour Name="67928NoColor" Value="16777215" /><cellColour Name="67932NoColor" Value="16777215" /><cellColour Name="67936NoColor" Value="16777215" /><cellColour Name="67937NoColor" Value="16777215" /></cellColours><Images /></ResultTable></ResultTables></TestResult></TestResults>

6 To know if the test has passed or failed after running, run the :PLUGin:DPHYTests:FETCh:RESult:PFResult? query to identify its status. If the status for any test is returned as UNKNown, it is most likely that the test has not been run yet.

   -> :PLUGin:DPHYTests:FETCh:RESult:PFResult?

   <- "Skew Calibration Module 1",PASS

7 Repeat the previous steps, if you wish to obtain test results for other CTS tests that have already been run.

Following procedure describes remote reconfiguration of CTS Tests using the :PLUGin:DPHYTests:CONFigure command.

- **Method 1:**

1 Run one of the following commands:
   - Run the :PLUGin:DPHYTests:RESet command to reset the settings of the MIPI D-PHY CTS plug-in instance to the default values, OR,
   - Run the :PLUGin:DPHYTests:DELete command to remove the existing MIPI D-PHY CTS plug-in and its configuration. Then, run the :PLUGin:DPHYTests:NEW command to create a new MIPI D-PHY CTS plug-in instance, which contains the default settings.
2 Run the :PLUGin:DPHYTests:PARameter:LIST? query to check for the list of parameters and their default values.
3 To set up / modify the value for one or more parameters, run the :PLUGin:DPHYTests:PARameter[:Value][?] command.

4 Once all required parameters are configured, run the :PLUGin:DPHYTests:CONFigure command. Based on your configuration, the list of calibrations and tests are created and the plug-in is ready to run the CTS tests.

- **Method 2:**

1 In the existing instance of MIPI D-PHY CTS plug-in, run the :PLUGin:DPHYTests:PARameter:LIST? query to check for the list of parameters and their current values.

For example, if you run :PLUGin:DPHYTests:PARameter:LIST? "MIPI D-PHY CTS 1", a list of parameter name value pairs is returned, such as,

":TP1.Link&Connection.OfflineMode","0",

":TP1.Link&Connection.AwgModel","M8190",

":TP1.Link&Connection.AwgMode","FOUR",

":TP1.Link&Connection.NumberOfAwgs","AWG2",

":TP1.Link&AWG Setup.AwgHostIpAddress","127.0.0.1",

":TP1.Link&AWG Setup.AwgClockSyncHiSlip","hislip0",

":TP1.Link&AWG Setup.AwgOneHiSlip","hislip1", ":TP1.Link&AWG Setup.AwgTwoHiSlip","hislip2", ":TP1.Link&AWG Setup.AwgThreeHiSlip","hislip3", ":TP1.Link&AWG Setup.AwgFourHiSlip","hislip3", ":TP1.Link&Oscilloscope Setup.OscilloscopeOfflineMode","0",

":TP1.Link&OscilloscopeSetup.OscilloscopeAddress","TCPIP0::121.0.0.1::inst0::INSTR",

":TP1.System&Global.TestMode","COMpliance",

":TP1.System&Global.SpecVersion","v1_20",

":TP1.System&Global.NumberOfDataLanes",

"LANE1",":TP1.System&Global.SyncWord","0xB8",

":TP1.System&Global.LsbFirst","1",

":TP1.System&Global.LpDataRate","10000000",

":TP1.System&Global.HsDataRate","800000000",

":TP1.System&Global.TriggeredStart","0",

. . .

2 To set up / modify the value for one or more parameters (for example, the HS Data Rate), run the :PLUGin:DPHYTests:PARameter[:Value][?] command.

For example,

:PLUGin:DPHYTests:PARameter:VALue "MIPI D-PHY CTS 1#:TP1.System&Global.HsDataRate", "2e9"

3 Once all required parameters are configured, run the :PLUGin:DPHYTests:CONFigure command. Based on your configuration, the list of calibrations and tests are recreated and the plug-in is ready to run the CTS tests.

Remote Queries to find Parameter ranges (maximum and minimum limits)

The MIPI D-PHY CTS plug-in consists of several parameters, where you may define a value only within a permissible range. The MIPI D-PHY CTS plug-in automatically configures the ranges for such parameters based on certain options you may select on the user interface or remotely.

On the MIPI D-PHY CTS plug-in GUI, you may simply hover the mouse cursor over a specific parameter's value field to find its maximum and minimum permissible values. However, when working remotely, you may have to check the permissible ranges before configuring the value of a parameter.

While running a query for a parameter returns its current value, you can add the **MAX** and **MIN** identifiers in your query (separated by a comma after the plug-in identifier) to find the maximum and minimum value, respectively, for that parameter.

Consider the following examples to understand how to use these identifiers:

1 To check for the list of parameters and their default values, run the :PLUGin:DPHYTests:PARameter:LIST? query. Using this query, you may view the list of either global parameters or only such parameters that are specific to a test/calibration procedure.

2 To check the current value of a specific parameter, run the :PLUGin:DPHYTests:PARameter[:Value][?] query.

For example, consider the global parameter "Idle Voltage":

a Run the query to find its current value.

-> :PLUGin:DPHYTests:PARameter:VALue? 'MIPI D-PHY CTS 1#:TP1.System&Idle Voltage.Idle Voltage'

<- "0.29999999999999999"

The query returns the current value of Idle Voltage as 300mV.

b To be able to modify this parameter's value within the permissible limits, add the **MAX** and **MIN** identifiers in your query to find the maximum and minimum permissible values, respectively.

-> :PLUGin:DPHYTests:PARameter:VALue? 'MIPI D-PHY CTS 1#:TP1.System&Idle Voltage.Idle Voltage', MAX

<- "0.34999999999999998"

Using the **MAX** identifier, the query returns the maximum value of Idle Voltage as 350mV.

-> :PLUGin:DPHYTests:PARameter:VALue? 'MIPI D-PHY CTS 1#:TP1.System&Idle Voltage.Idle Voltage', MIN

<- "0.20000000000000001"

Using the **MIN** identifier, the query returns the minimum value of Idle Voltage as 200mV.

Similarly, you may find the permissible limits for any other global parameter on the Configuration window of the MIPI D-PHY CTS plug-in.

Now, consider another example of the test specific parameter “Max Tested Value” in **Test 2.3.1 Vcmrx Tolerance Data0** test under **Data0** test category:

a In the Connection Diagram window, run the :PLUGin:DPHYTests:SELect command to select the test whose parameters you wish to view and modify.

:PLUGin:DPHYTests:SELect 'MIPI D-PHY CTS 1#Test 2.3.1 Vcmrx Tolerance Data0'

b To check for the selected test parameters and their default values, run the :PLUGin:DPHYTests:PARameter:LIST? query.

-> :PLUGin:DPHYTests:PARameter:LIST? 'MIPI D-PHY CTS 1#Test 2.3.1 Vcmrx Tolerance Data0'

<- ":TP1.System&Acquisition Parameters.PropertiesEditable","1",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.Offline","1",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.Setup Filename","Data0_HS",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.HS Frequency","800000000",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.BER Limit","9.9999999999999995E-07",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.Min Tested Value","0.070000000000000007",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.Max Tested Value","0.33000000000000002",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.V_OD Array","0.26;1|0.07;1|0.22;-1|0.07;-1"

c While the current value of the parameter is displayed along with the name in the previous list, to check the value of the test-specific parameter separately, run the :PLUGin:DPHYTests:PARameter[:Value][?] query.

-> :PLUGin:DPHYTests:PARameter:VALue? 'MIPI D-PHY CTS 1#Test 2.3.1 Vcmrx Tolerance Data0:TP1.System&Max Tested Value'

<- "0.33000000000000002"

The query returns the current value of Max Tested Value as 0.33V.

d To be able to modify this parameter's value within the permissible limits, add the **MAX** and **MIN** identifiers in your query to find the maximum and minimum permissible values, respectively.

-> :PLUGin:DPHYTests:PARameter:VALue? 'MIPI D-PHY CTS 1#Test 2.3.1 Vcmrx Tolerance Data0::TP1.System&Max Tested Value', MAX

<- "2"

Using the **MAX** identifier, the query returns the maximum value of Max Tested Value as 2V.

-> :PLUGin:DPHYTests:PARameter:VALue? 'MIPI D-PHY CTS 1#Test 2.3.1 Vcmrx Tolerance Data0::TP1.System&Max Tested Value', MIN

<- "-2"

Using the **MIN** identifier, the query returns the minimum value of Max Tested Value as -2V.

Similarly, you may find the permissible limits for any other test-related parameters on the Connection Diagram window of the MIPI D-PHY CTS plug-in.

3 To set up / modify the value for one or more parameters, run the :PLUGin:DPHYTests:PARameter[:Value][?] command.

SCPI Commands

:PLUGin:DPHYTests:CATalog?

Query Syntax :PLUGin:DPHYTests:CATalog?

Identifier Not available.

Description This query returns the names of all active or closed MIPI D-PHY CTS plug-in instances in the current session of the M8070B software.

Query Example :PLUGin:DPHYTests:CATalog?

<- "MIPI D-PHY CTS 1","MIPI D-PHY CTS 2","MIPI D-PHY CTS test1"

:PLUGin:DPHYTests:CONFigure

Command Syntax :PLUGin:DPHYTests:CONFigure ['<Identifier>']

Identifier (Optional) MIPI D-PHY CTS plug-in identifier name.

Description This command is equivalent to pressing the Apply button on the MIPI D-PHY CTS plug-in user interface instance. Running this command applies the Configuration settings on the MIPI D-PHY CTS plug-in user interface and displays the Connection Diagram window. If working remotely, first run the :PLUGin:DPHYTests:PARameter:LIST? query to check for the list of available parameters for the configuration and also the :PLUGin:DPHYTests:PARameter[:Value][?] command to modify / change values of parameters individually, if needed.

Command Example :PLUGin:DPHYTests:CONFigure 'MIPI D-PHY CTS 1'

:PLUGin:DPHYTests:CONNection:CDEScription?

Query Syntax :PLUGin:DPHYTests:CONNection:CDEScription? '<Identifier>'

Identifier MIPI D-PHY CTS plug-in identifier name.

Description This command returns the description of the physical connection required for the MIPI D-PHY CTS test type selected under a category of tests in the Connection Diagram window of the MIPI D-PHY CTS plug-in user interface. If working remotely, first run the :PLUGin:DPHYTests:SELect command to select the test whose connection description you wish to know.

Query Example Following examples display the connection description from the MIPI D-PHY CTS plug-instance “MIPI D-PHY CTS 1” for “Skew Calibration Module 1” and “V_ILHS Calibration Clock” under the category “Calibration” and for the CTS test “Test 2.3.1 Vcmrx Tolerance Data0” under the category “Data0”, respectively.

-> :PLUGin:DPHYTests:CONNection:CDEScription? 'MIPI D-PHY CTS 1'

<- #3422Connect the outputs of the AWG to the Oscilloscope.\par - {\b AWG Module, Channel 1, AMP OUT (Normal) \b0} -> {\b Oscilloscope, Channel 1 \b0} \par - {\b AWG Module, Channel 2, AMP OUT (Normal) \ b0} -> {\b Oscilloscope, Channel 2 \b0} \par - {\b AWG Module, Channel 3, AMP OUT (Normal) \b0} -> {\b Oscilloscope, Channel 3 \b0} \par - {\b AWG Module, Channel 4, AMP OUT (Normal) \b0} -> {\b Oscilloscope, Channel 4 \b0}

-> :PLUGin:DPHYTests:CONNection:CDEScription? 'MIPI D-PHY CTS 1'

<- #3287- {\b First AWG Module, Channel 1, AMP OUT (Normal) \b0} -> {\b Oscilloscope, Channel 1 \b0} \par - {\b First AWG Module, Channel 2, AMP OUT (Normal) \b0} -> {\b Oscilloscope, Channel 2 \b0}

-> :PLUGin:DPHYTests:CONNection:CDEScription? 'MIPI D-PHY CTS 1'

<- #3655Connect the outputs of the AWG to the DUT and to the Oscilloscope.\par - {\b First AWG Module, Channel 1, AMP OUT (Normal) \b0} -> {\b DUT, Clock P. \b0} \par - {\b First AWG Module, Channel 2, AMP OUT (Normal) \b0} -> {\b DUT, Clock N. \b0} \par - {\b Second AWG Module, Channel 1, AMP OUT (Normal) \b0} -> {\b DUT, Data0 P. \b0} \ par - {\b Second AWG Module, Channel 2, AMP OUT (Normal) \b0} -> {\b DUT, Data0 N. \b0} \par - {\b Following generators must be connected to addiional DUT Lanes. \b0} \par - {\b Probe on DUT, Clock N \b0} -> {\b Oscilloscope, Channel 1 \b0}. \par - {\b Probe on DUT, Data0 N \b0} -> {\ b Oscilloscope, Channel 2 \b0}.

:PLUGin:DPHYTests:CONNection:DIAGram?

Query Syntax :PLUGin:DPHYTests:CONNection:DIAGram? '<Identifier>'

Identifier MIPI D-PHY CTS plug-in identifier name.

Description This command returns the description of the connection diagram image used for the MIPI D-PHY CTS test type selected under a category of tests in the Connection Diagram window of the MIPI D-PHY CTS plug-in user interface. If working remotely, first run the :PLUGin:DPHYTests:SELect command to select the test whose connection diagram description you wish to know. Since the SCPI Editor is not GUI-based, the resulting output is garbled text.

Query Example :PLUGin:DPHYTests:CONNection:DIAGram? 'MIPI D-PHY CTS 1'

:PLUGin:DPHYTests:CONNection[:WIRing]?

Query Syntax :PLUGin:DPHYTests:CONNection? '<Identifier>'

:PLUGin:DPHYTests:CONNection[:WIRing]? '<Identifier>'

Identifier MIPI D-PHY CTS plug-in identifier name.

Description This command returns the number of wiring connections required for the selected calibration / test in the MIPI D-PHY CTS plug-in user interface.

Query Example Following examples use both syntaxes shown for this command:

-> :PLUGin:DPHYTests:CONNection? 'MIPI D-PHY CTS 1'

<- 1

-> :PLUGin:DPHYTests:CONNection:WIRing? 'MIPI D-PHY CTS 1'

<- 1

:PLUGin:DPHYTests:DELete

Command Syntax :PLUGin:DPHYTests:DELete '<Identifier>'

Identifier MIPI D-PHY CTS plug-in identifier name.

Description This command deletes the MIPI D-PHY CTS plug-in instance.

Command Example :PLUGin:DPHYTests:DELete 'MIPI D-PHY CTS 1'

:PLUGin:DPHYTests:FETCh:RESult:PFResult?

Query Syntax :PLUGin:DPHYTests:FETCh:RESult:PFResult?

Identifier Not available.

Description This command returns the current Pass/Fail status of the test for the selected MIPI D-PHY CTS Calibration or Test name on the MIPI D-PHY CTS plug-in user interface. The status of the test could be either PASS, FAIL or UNKNOWN. The status Unknown appears if the selected calibration / test has not been run yet. If working remotely, first run the :PLUGin:DPHYTests:SELect command to select the test whose Pass/Fail status you wish to know.

Query Example Following examples display various Calibration / Test names along with their status:

-> :PLUGin:DPHYTests:FETCh:RESult:PFResult?

<- "Skew Calibration Module 1",PASS

-> :PLUGin:DPHYTests:FETCh:RESult:PFResult?

<- "Amplifier Level Calibration Module 1 Gen 1 Clock Normal",PASS

-> :PLUGin:DPHYTests:FETCh:RESult:PFResult?

<- "Intrinsic Jitter Calibration 800 Mbps",UNKNown

-> :PLUGin:DPHYTests:FETCh:RESult:PFResult?

<- "Test 2.3.6 HS RX CM Interference 50-450 MHz Data0",PASS

:PLUGin:DPHYTests:FETCh:RESult[:VALue]?

Query Syntax :PLUGin:DPHYTests:FETCh:RESult? '<Identifier>'

:PLUGin:DPHYTests:FETCh:RESult:VALue? '<Identifier>'

Identifier The calibration / test name in the MIPI D-PHY CTS plug-in instance. Note that the # symbol is part of the syntax and is inserted as a separator.

Description This query returns all test parameters, the formatting of the table and the results for the selected MIPI D-PHY CTS Calibration or Test name in an XML format.

Query Example Following example displays the data associated with the Test 2.1.1 V_IH Sensitivity Clock test.

-> :PLUGin:DPHYTests:FETCh:RESult:VALue? 'MIPI D-PHY CTS 1#Test 2.1.1 V_IH Sensitivity Clock_1'

<- #41343<?xml version="1.0" encoding="utf-16"?><TestResults version="2.0"><TestResult><Summary><ProcedureName>Test 2.1.1 V_IH Sensitivity Clock</ProcedureName><ProcedureID>5000540</ProcedureID><Result>Passed</Result><DateTime>04/28/2017 15:53:10</DateTime><Duration>00:00:32.6220000</Duration><Description>This procedure test the LP Input High Voltage Sensitivity.</Description></Summary><ResultTables><ResultTable><Title>V_IH Tolerance_Clock</Title><Subtitle>Verify the V_IH tolerance</Subtitle><Name>V_IH Tolerance_Clock</Name><Parameters><Parameter name="Offline" value="True" /></Parameters><Columns><Column name="Result" unit="" recommendedExponent="0" width="13"><Value>pass</Value></Column><Column name="Min Passed V_IH" unit="V" precision="0" recommendedExponent="-3" width="8"><Value>0.6</Value></Column><Column name="Min Tested V_IH" unit="V" precision="0" recommendedExponent="-3" width="8"><Value>0.6</Value></Column><Column name="Min Spec V_IH" unit="V" precision="0" recommendedExponent="-3" width="8"><Value>0.74</Value></Column></Columns><cellColours><cellColour Name="67928NoColor" Value="16777215" /><cellColour Name="67932NoColor" Value="16777215" /><cellColour

Name="67936NoColor" Value="16777215" /><cellColour Name="67937NoColor" Value="16777215" /></cellColours><Images /></ResultTable></ResultTables></TestResult></TestResults>

:PLUGin:DPHYTests:HISTory:CATalog?

Query Syntax :PLUGin:DPHYTests:HISTory:CATalog?

Identifier Not available.

Description This query returns the names of all calibration / test results that have already been run in the MIPI D-PHY CTS plug-in instance.

Query Example -> :PLUGin:DPHYTests:HISTory:CATalog?

<- "Test 2.1.1 V_IH Sensitivity Clock_1","Test 2.1.4 V_HYST Sensitivity Data0_1","Test 2.1.4 V_HYST Sensitivity Data0_1"

:PLUGin:DPHYTests:LIST?

Query Syntax :PLUGin:DPHYTests:LIST?

Identifier Not available.

Description This query returns the names of all calibration / test procedures that appear in the Connection Diagram window for a certain Configuration setting in the MIPI D-PHY CTS plug-in instance. Note that this query returns a value only while the Connection Diagram window of the MIPI D-PHY CTS plug-in instance is active. Use the :PLUGin:DPHYTests:CONFigure command to switch to the Connection Diagram window of the MIPI D-PHY CTS plug-in where the calibrations or tests are listed in their respective groups.

Query Example -> :PLUGin:DPHYTests:LIST?

<- "Skew Calibration Module 1","Amplifier Level Calibration Module 1 Gen 1 Clock Normal","Amplifier Level Calibration Module 1 Gen 2 Clock Complement","Skew Calibration Module 2","Amplifier Level Calibration Module 2 Gen 1 Data0 Normal","Amplifier Level Calibration Module 2 Gen 2 Data0 Complement","Inter Module Skew Calibration","LP Level Calibration Clock","V_ILHS Calibration Clock","Differential Amplitude Cal Clock","LP Level Calibration Data0","V_ILHS Calibration Data0","e-Spike Calibration","Differential Amplitude Cal Data0","LP Level Calibration Clock Small AWG Amplitude","V_ILHS Calibration Clock Small AWG Amplitude","Differential Amplitude Cal Clock Small AWG Amplitude","LP Level Calibration Data0 Small AWG Amplitude","V_ILHS Calibration Data0 Small AWG Amplitude","Differential Amplitude Cal Data0 Small AWG Amplitude","Intrinsic Jitter Calibration 800 Mbps","Transition Time Cal 800 Mbps","Rise Time - Eye Height Calibration 800 Mbps","Test 2.3.1 Vcmrx Tolerance Clock","Test 2.3.2 V_IDTH and Test 2.3.3 V_IDTL Sensitivity

Clock","Test 2.3.4 V_IHHS Sensitivity Clock","Test 2.3.5 V_ILHS Sensitivity Clock","Test 2.3.6 HS RX CM Interference 50-450 MHz Clock","Test 2.3.7 HS RX CM Interference beyond 450 MHz Clock","Test 2.3.8 HS RX Clock-to-Data Skew","Test 2.4.7 T_Clk-Prepare_Zero Compliance Procedure","Test 2.4.8 T_Clock-Settle - Clock Procedure","Test 2.4.9 T_Clk-Trail - Clock Procedure","Test 2.4.11a T_Clk-Pre - Clock Procedure","Test 2.4.11b T_Clk-Post - Clock Procedure","Test 2.3.1 Vcmrx Tolerance Data0","Test 2.3.2 V_IDTH and Test 2.3.3 V_IDTL Sensitivity Data0","Test 2.3.4 V_IHHS Sensitivity Data0","Test 2.3.5 V_ILHS Sensitivity Data0","Test 2.3.6 HS RX CM Interference 50-450 MHz Data0","Test 2.3.7 HS RX CM Interference beyond 450 MHz Data0","Test 2.3.8 HS RX Data-to-Clock Skew Data0","Test 2.4.2 T_HS-Prepare_Zero Compliance Procedure-Data0","Test 2.4.3 T_HS-Settle - Data0 Procedure","Test 2.4.4 T_HS-Trail - Data0 Procedure","Test 2.4.5 T_HS-Skip - Data0 Procedure","Test 2.4.6 Clock Lane T_CLK-TERM-EN","Test 2.4.1 Data0 Lane T_HS-TERM-EN","Test 2.1.1 V_IH Sensitivity Clock","Test 2.1.2 V_IL Sensitivity Clock","Test 2.1.4 V_HYST Sensitivity Clock","Test 2.1.4 V_HYST Dynamic Clock","Test 2.1.5 LP-RX Minimum Pulse Width Response T_Min-RX Clock","Test 2.1.6 LP-RX Input pos. Pulse Rejection e_spike Clock","Test 2.1.6 LP-RX Input neg. Pulse Rejection e_spike Clock","Test 2.1.7 LP-RX Interference Tolerance VINT and fINT Clock","Test 2.1.1 V_IH Sensitivity Data0","Test 2.1.2 V_IL Sensitivity Data0","Test 2.1.4 V_HYST Sensitivity Data0","Test 2.1.4 V_HYST Dynamic Data0","Test 2.1.5 LP-RX Minimum Pulse Width Response T_Min-RX Data0","Test 2.1.6 LP-RX Input pos. Pulse Rejection e_spike Data0","Test 2.1.6 LP-RX Input neg. Pulse Rejection e_spike Data0","Test 2.1.7 LP-RX Interference Tolerance VINT and fINT Data0","Test 2.2.1 Init. Period TINIT","Test 2.2.2 ULPS Exit TWAKEUP","Test 2.2.3 Clock Invalid or Aborted Escape Entry","Test 2.2.4 Data Invalid or Aborted Escape Entry","Test 2.2.5 Data Invalid or Aborted Escape Command","Test 2.2.7 Data Post-Trigger-Command","Test 2.2.8 Data LP-RX Escape Mode Unsupported or Unassigned Commands"

:PLUGin:DPHYTests:NEW

Command Syntax :PLUGin:DPHYTests:NEW '<Identifier>'

Identifier MIPI D-PHY CTS plug-in identifier name.

Description This command creates a new MIPI D-PHY CTS plug-in interface. Run this command only when no other MIPI D-PHY CTS instance is active.

Command Example :PLUGin:DPHYTests:NEW 'MIPI D-PHY CTS 1'

:PLUGin:DPHYTests:PARameter:LIST?

Query Syntax :PLUGin:DPHYTests:PARameter:LIST? ['<Identifier>']

Identifier (Optional) The calibration / test name in the MIPI D-PHY CTS plug-in instance or just the MIPI D-PHY CTS plug-in instance name. Note that the # symbol is part of the syntax and is inserted as a separator.

Description This query returns the names and the currently assigned values for each parameter, listed on the Configuration window or those associated with the selected calibration / test procedures in the currently active MIPI D-PHY CTS plug-in instance. If working remotely, you may run the :PLUGin:DPHYTests:NEW command to create a new instance of the MIPI D-PHY CTS plug-in and view the parameter names and their default values. If you have already run the :PLUGin:DPHYTests:CONFigure command to switch to the Connection Diagram window, you may run the :PLUGin:DPHYTests:SELect command to select a calibration / test whose parameters you wish to view.

Query Example Following examples display the parameters associated with the “Intrinsic Jitter Calibration 800 Mbps” (selected in the user interface only), “Test 2.3.1 Vcmrx Tolerance Data0” (specified in the query), and all parameters in the ‘MIPI D-PHY CTS 1’ plug-in instance, respectively, when they are selected.

- > :PLUGin:DPHYTests:PARameter:LIST?

<- ":TP1.System&Acquisition Parameters.PropertiesEditable","1",":TP1.System&Intrinsic Jitter Calibration 800 Mbps.Offline","1",":TP1.System&Intrinsic Jitter Calibration 800 Mbps.Use Deembedding","1",":TP1.System&Intrinsic Jitter Calibration 800 Mbps.In-System Calibration","1",":TP1.System&Intrinsic Jitter Calibration 800 Mbps.Transfer Function Chan1","DoNothing.tf2",":TP1.System&Intrinsic Jitter Calibration 800 Mbps.Transfer Function Chan2","DoNothing.tf2",":TP1.System&Intrinsic Jitter Calibration 800 Mbps.Transfer Function Chan4","DoNothing.tf2",":TP1.System&Intrinsic Jitter Calibration 800 Mbps.Calibration Channel Clock","Channel1",":TP1.System&Intrinsic Jitter Calibration 800 Mbps.Calibration Channel Data","Channel2",":TP1.System&Intrinsic Jitter Calibration 800 Mbps.Oscilloscope Bandwidth","10000000000",":TP1.System&Intrinsic Jitter Calibration 800 Mbps.HS Sequence File","MipiJitterCalibration.seq",":TP1.System&Intrinsic Jitter Calibration 800 Mbps.Show Real Time Eye","1"

Test 2.3.1 Vcmrx Tolerance Data0

-> :PLUGin:DPHYTests:PARameter:LIST? 'MIPI D-PHY CTS 1#Test 2.3.1 Vcmrx Tolerance Data0'

<- ":TP1.System&Acquisition Parameters.PropertiesEditable","1",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.Offline","1",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.Setup Filename","Data0_HS",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.HS Frequency","800000000",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.BER Limit","9.9999999999999995E-07",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.Min Tested Value","0.070000000000000007",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.Max Tested Value","0.33000000000000002",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.V_OD Array","0.26;1|0.07;1|0.22;-1|0.07;-1"

For 'MIPI D-PHY CTS 1' plug-in instance

-> :PLUGin:DPHYTests:PARameter:LIST? 'MIPI D-PHY CTS 1'

<- ":TP1.Link&Connection.OfflineMode","1",":TP1.Link&Connection.AwgModel","M8195",":TP1.Link&Connection.InSystemCalibrationCTS","1",":TP1.Link&Connection.AwgMode","FOUR",":TP1.Link&Connection.NumberOfAwgs","AWG2",":TP1.Link&AWG Setup.AwgHostIpAddress","127.0.0.1",":TP1.Link&AWG Setup.AwgClockSyncHiSlip","hislip0",":TP1.Link&AWG Setup.AwgOneHiSlip","hislip1",":TP1.Link&AWG Setup.AwgTwoHiSlip","hislip2",":TP1.Link&AWG Setup.AwgThreeHiSlip","hislip3",":TP1.Link&AWG Setup.AwgFourHiSlip","hislip3",":TP1.Link&Oscilloscope Setup.OscilloscopeOfflineMode","1",":TP1.Link&Oscilloscope Setup.OscilloscopeAddress","TCPIP0::121.0.0.1::inst0::INSTR",":TP1.System&Global.TestMode","COMpliance",":TP1.System&Global.SpecVersion","v1_20",":TP1.System&Global.NumberOfDataLanes","LANE1",":TP1.System&Global.SyncWord","0xB8",":TP1.System&Global.LsbFirst","1",":TP1.System&Global.LpDataRate","10000000",":TP1.System&Global.HsDataRate","800000000",":TP1.System&Global.TriggeredStart","0",":TP1.System&Global.ManualDeskew","0",":TP1.System&Global.RestartSequenceAfterReset","0",":TP1.System&Global.RestartSequenceBeforeReset","0",":TP1.System&Global.PatternMode","COMpliance",":TP1.System&Global.AllDataLanesSimultaneously","0",":TP1.System&Global.HsModeDataFile","C:\ProgramData\BitifEye\ValiFrame\Pattern\DPhy\HsCompliancePattern.dat",":TP1.System&Global.HsModeSequenceFile","C:\ProgramData\BitifEye\ValiFrame\Pattern\DPhy\Hs.seq",":TP1.System&Global.HsModeFileName","HsCompliancePattern.dat",":TP1.System&Global.LpModeDataFile","C:\ProgramData\BitifEye\ValiFrame\Pattern\DPhy\LpCompliancePattern.dat",":TP1.System&Global.LpModeSequenceFile","C

:\ProgramData\BitifEye\ValiFrame\Pattern\DPhy\
Lp.seq",":TP1.System&Global.LpModeFileName","LpCompliancePattern.d
at",":TP1.System&Global.UlpModeDataFile","C:\ProgramData\BitifEye\
ValiFrame\Pattern\DPhy\
LpCompliancePattern.dat",":TP1.System&Global.UlpModeSequenceFile","
C:\ProgramData\BitifEye\ValiFrame\Pattern\DPhy\
Ulp.seq",":TP1.System&Global.UlpModeFileName","LpCompliancePattern.
dat",":TP1.System&Global.BehavioralSequenceFile","C:\ProgramData\
BitifEye\ValiFrame\Pattern\DPhy\
Behavioral.seq",":TP1.System&Global.BehavioralSequenceFileName","Beh
avioral.seq",":TP1.System&Global.IsiFile","C:\ProgramData\BitifEye\
ValiFrame\SParameter\DPhy\
ReferenceChannel_Standard.s4p",":TP1.System&Global.IsiFileName","Ref
erenceChannel_Standard.s4p",":TP1.System&Global.BerReader","OFFline"
,":TP1.System&Global.BerLimit","_1_06",":TP1.System&Global.BerReaderA
ddress","",":TP1.System&Global.Mipi Protocol","DSI",":TP1.System&Signal
Levels.LowPowerHighLevel","1.2",":TP1.System&Signal
Levels.LowPowerLowLevel","0",":TP1.System&Signal
Levels.HighSpeedCommonLevel","0.20000000000000001",":TP1.System&
Signal
Levels.HighSpeedDifferentialSwing","0.20000000000000001",":TP1.Syste
m&Protocol
Timings.ClockPrepareLength","7.0000000000000005E-08",":TP1.System&
Protocol
Timings.ClockZeroLength","2.9999999999999999E-07",":TP1.System&Pro
tocol
Timings.ClockPreLength","1.2499999999999999E-08",":TP1.System&Prot
ocol
Timings.ClockPostLength","7.0000000000000005E-08",":TP1.System&Pro
tocol
Timings.ClockTrailLength","8.0000000000000002E-08",":TP1.System&Pro
tocol Timings.ClockMissLength","0",":TP1.System&Protocol
Timings.PrepareLength","6.3300000000000004E-08",":TP1.System&Proto
col
Timings.ZeroLength","1.1230000000000001E-07",":TP1.System&Protocol
Timings.TrailLength","7.0000000000000005E-08",":TP1.System&Protocol
Timings.ExitLength","9.9999999999999995E-08",":TP1.System&Protocol
Timings.WakeupLength","0.10000000000000001",":TP1.System&Protocol
Timings.InitLength","0.0001",":TP1.System&Protocol
Timings.InitialSkewCalLength","0.0001",":TP1.System&Protocol
Timings.PeriodicSkewCalLength","0.0001",":TP1.System&Protocol
Timings.SetTimingsToMin","",":TP1.System&Idle Voltage.Idle
Voltage","0.10000000000000001"

:PLUGin:DPHYTests:PARameter[:Value][?]

Command Syntax :PLUGin:DPHYTests:PARameter '<Identifier>','<new value for the parameter>'

:PLUGin:DPHYTests:PARameter:Value '<Identifier>','<new value for the parameter>'

Query Syntax :PLUGin:DPHYTests:PARameter? '<Identifier>'

:PLUGin:DPHYTests:PARameter:Value? '<Identifier>'

Identifier The parameter name, either from the Configuration window or specific to a calibration/test in the MIPI D-PHY CTS plug-in instance along with the new value for the parameter in scientific notation. Note that the # symbol is part of the syntax and is inserted as a separator.

Description This command modifies the value of either the configuration parameters or the specified parameter specific to the selected calibration / test procedures in the MIPI D-PHY CTS plug-in instance. Run the :PLUGin:DPHYTests:PARameter:LIST? query to check for the list of configuration parameters. You cannot modify the value of the configuration parameters after you run the :PLUGin:DPHYTests:CONFigure command, that is, switch to Connection Diagram window. Once you select a calibration / test procedure remotely using the :PLUGin:DPHYTests:SELect command in the MIPI D-PHY CTS plug-in instance. Run the :PLUGin:DPHYTests:PARameter:LIST? query to check for the list of parameters specific to calibration/test procedures.

Command Example :PLUGin:DPHYTests:PARameter 'MIPI D-PHY CTS 1#:TP1.System&Global.HsDataRate', '2e9'

:PLUGin:DPHYTests:PARameter "MIPI D-PHY CTS 1#Skew Calibration Module 1#:TP1.System&Skew Tolerance","11E-12"

NOTE You can modify the values of parameters specific to calibration / test names only when the **Mode:** option under **Receiver Test Configuration** is set to **Expert Mode**.

Notice that the way of denoting the identifier for parameters specific to calibrations / tests are slightly different from that for denoting the identifier for configuration parameters. When you run the :PLUGin:DPHYTests:PARameter:LIST? query for specific calibration / test, it returns a certain value to describe the parameter. For the **:PLUGin:DPHYTests:PARameter:Value '<Identifier>','<new value for the parameter>'** command to recognize the identifier correctly, you must modify the way the parameter is described.

Consider the following example:

-> :PLUGin:DPHYTests:PARameter:LIST? 'MIPI D-PHY CTS 1#Test 2.3.1 Vcmrx Tolerance Data0'

<- ":TP1.System&Acquisition Parameters.PropertiesEditable","1",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.Offline","1",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.Setup Filename","Data0_HS",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.HS Frequency","1600000000",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.BER Limit","7.9900000000000007E-09",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.Min Tested Value","0.070000000000000007",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.Max Tested Value","0.33000000000000002",":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.V_OD Array","0.26;1|0.07;1|0.22;-1|0.07;-1"

When you run the :PLUGin:DPHYTests:PARameter:LIST? query for Test 2.3.1 Vcmrx Tolerance Data0, it returns the parameters specific to that test along with their current values. If you wish to modify the value of the parameter 'BER Limit' (underlined above) remotely, you cannot simply use ":TP1.System&Test 2.3.1 Vcmrx Tolerance Data0.BER Limit" as the identifier for the **:PLUGin:DPHYTests:PARameter:Value** command. You must modify the text such that the identifier displays "current MIPI D-PHY plug-in instance name#Calibration/Test name:Functional Block&Parameter name". So, for this example, the identifier becomes "MIPI D-PHY CTS 1#Test 2.3.1 Vcmrx Tolerance Data0:TP1.System&BER Limit".

:PLUGin:DPHYTests:RESet

Command Syntax :PLUGin:DPHYTests:RESet '<Identifier>'

Identifier MIPI D-PHY CTS plug-in identifier name.

Description This command resets the settings of the MIPI D-PHY CTS plug-in instance to the default values.

Command Example :PLUGin:DPHYTests:RESet 'MIPI D-PHY CTS 1'

:PLUGin:DPHYTests:RUN:HISTory:CLEar

Command Syntax :PLUGin:DPHYTests:RUN:HISTory:CLEar

Identifier Not available.

Description This command clears the history information for any test runs from the "Measurement History" area in the MIPI D-PHY CTS plug-in instance.

Command Example :PLUGin:DPHYTests:RUN:HISTory:CLEar

:PLUGin:DPHYTests:RUN:HISTory[:STATe]?

Query Syntax :PLUGin:DPHYTests:RUN:HISTory?

:PLUGin:DPHYTests:RUN:HISTory:STATe?

Identifier Not available.

Description This query returns a 1 to indicate test run history and result is available or 0 indicates no tests were run.

Query Example -> :PLUGin:DPHYTests:RUN:HISTory:STATe?

<- 1

:PLUGin:DPHYTests:RUN:LOG?

Query Syntax :PLUGin:DPHYTests:RUN:LOG?

Identifier Not available.

Description This query returns the logs for the calibration / test procedure that has just been run in the MIPI D-PHY CTS plug-in instance.

Query Example Following examples display the query results when the “Skew Calibration Module 1” and “LP Level Calibration Clock” are run.

-> :PLUGin:DPHYTests:RUN:LOG?

<- #3118 04/28/2017 15:04:18,Measurement.MIPI D-PHY CTS.MIPI D-PHY CTS 1.Skew Calibration Module 1,Info,"Test Passed Offline"

-> :PLUGin:DPHYTests:RUN:LOG?

<- #3119 04/28/2017 15:04:58,Measurement.MIPI D-PHY CTS.MIPI D-PHY CTS 1.LP Level Calibration Clock,Info,"Test Passed Offline"

:PLUGin:DPHYTests:RUN:MESSage?

Query Syntax :PLUGin:DPHYTests:RUN:MESSage?

Identifier Not available.

Description This query returns the running state of the calibration / test procedure that you select remotely using the :PLUGin:DPHYTests:SELect command in the MIPI D-PHY CTS plug-in instance. The various running states, which the query returns, are NotStarted, Running, Error and Finished.

Query Example Following examples display the query results for certain tests, respectively, that has finished running and another that has not yet started.

-> :PLUGin:DPHYTests:RUN:MESSage?

<- "Finished"

-> :PLUGin:DPHYTests:RUN:MESSage?

<- "NotStarted"

:PLUGin:DPHYTests:RUN:PROGress?

Query Syntax :PLUGin:DPHYTests:RUN:PROGress?

Identifier Not available.

Description This query returns the progress of the calibration / test procedure that is currently running in the MIPI D-PHY CTS plug-in instance. The progress is indicated by a value between 0 and 1 based on the run progress and is represented in the scientific notation.

Query Example Following examples display the query results for certain tests, respectively, that have finished (1.0), not started (0.0), completed one-fourth (0.25) and half (0.5).

-> :PLUGin:DPHYTests:RUN:PROGress?

<- 1.000000000E+00

-> :PLUGin:DPHYTests:RUN:PROGress?

<- 0.000000000E+00

-> :PLUGin:DPHYTests:RUN:PROGress?

<- 2.500000000E-01

-> :PLUGin:DPHYTests:RUN:PROGress?

<- 5.000000000E-02

:PLUGin:DPHYTests:RUN[:STATus]?

Query Syntax :PLUGin:DPHYTests:RUN?

:PLUGin:DPHYTests:RUN:STATus?

Identifier Not available.

Description This query returns 1 or 0 to indicate whether a calibration / test you select remotely using the :PLUGin:DPHYTests:SELect command is in running state or not.

Query Example -> :PLUGin:DPHYTests:RUN:STATus?

<- 0

:PLUGin:DPHYTests:SELect

Command Syntax :PLUGin:DPHYTests:SELect '<Identifier>'

Identifier The calibration / test name in the MIPI D-PHY CTS plug-in instance. Note that the # symbol is part of the syntax and is inserted as a separator.

Description This command selects the specified Calibration / Test.

Command Example :PLUGin:DPHYTests:SELect 'MIPI D-PHY CTS 1#Test 2.1.4 V_HYST Sensitivity Data0'

PLUGin:DPHYTests:STARt

Command Syntax :PLUGin:DPHYTests:STARt

Identifier Not available.

Description This command starts running the calibration / test error ratio measurement that you select remotely using the :PLUGin:DPHYTests:SELect command in the D-PHY CTS plug-in instance.

Command Example :PLUGin:DPHYTests:STARt

PLUGin:DPHYTests:STOP

Command Syntax :PLUGin:DPHYTests:STOP

Identifier Not available.

Description This command is used to forcefully abort the calibration / test error ratio measurement while it is still running.

Command Example :PLUGin:DPHYTests:STOP

7 IBerReader Interface

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KEYSIGHT TECHNOLOGIES

The IBerReader interface is a .NET software interface, which allows communication with the proprietary external tools to perform automated tests. It is available for MIPI D-PHY, M-PHY, C-PHY and SATA Rx test plug-ins. It contains methods that are called during test runs to configure the device under test (DUT) and request the pass/fail information from the DUT. A DLL file is loaded at run time and a class is instantiated, which supports the IBerReader interface. The main function for getting the pass/fail information is the method *GetCounter(out double bitCounter, out double errorCounter)*. This method is defined in "IBerReader Interface Definition".

IBerReader Interface Definition

```
using System;

using System.Collections.Generic;

using System.Text;

namespace BerReader

{

public interface IBerReader

{

/// <summary>

/// This method is called to connect to your error
reader.

/// </summary>

/// <param name="address">The address string can be
used by your implementation to configure the
connection to the IBerReader interface</param> void
Connect(string address);

/// <summary>

/// This method is called to close the connection

/// </summary>

void Disconnect();

/// <summary>

/// This method is called prior to individual tests to
select the channels under test and the test mode. It
can be used to load pre-defined settings.

/// </summary>

/// <param name="mode"> Defines the test mode during
the test. The modes are Clock_HS, DataX_HS, DataX_LP,
DataX_ULP with X: 0-<number of data lines -1></param>
void Init(string mode);

/// <summary>
```

```
/// Is called at the beginning of the error
measurement and allows a reset for the DUT to be
implemented.

/// </summary>

void ResetDut();

/// <summary>

/// Starts the counters. This method MUST reset all
counters!

/// </summary>

void Start();

/// <summary>

/// Stop the DUT to read out the counters (see
GetReadCounterWithoutStopSupported()).

/// </summary>

void Stop();

/// <summary>

/// This method returns counters, the 1st counting the
bits/frames/lines or bursts and the 2nd one counting
the errors detected by the MipiBerReader. The
automation software will compute the BER using the
following equation BER=errorCounter/bitCounter. In
the case bitCounter = 0 even when the stimulus is
sending data, this is also interpreted as fail.

/// </summary>

/// <param name="bitCounter"> Contains the number of
bits which are received by the DUT. If it is not
possible to count bits the value can also contain
frames, or bursts. It is just a matter of the value
defined as target BER. If it is not possible to get
the number of bits/frames/bursts then the method can
return a value of -1 and the automation software can
compute the number of bits from the data rate and the
runtime.

</param>

/// <param name="errorCounter"> Total number of errors
since the last start.
```

```
/// </param>

void GetCounter(out double bitCounter, out double
errorCounter);

/// <summary>

/// This method returns a Boolean value indicating
whether the device supports reading the counters while
it is running. If this method returns false, the
device needs to be stopped to read the counters.

In this case the automation software will stop data
transmission before calling the GetCounter()
function, and re-start data transmission again after
reading the counter values.

/// </summary>

/// <returns> false if device needs to be stopped
before reading the counters, true if the counters can
be read on the fly.

</returns>

bool GetReadCounterWithoutStopSupported();

/// <summary>

/// This property returns a number to multiply the
value delivered by the bitCounter in the GetCounter()
function.

/// </summary>

Double NumberOfBitsPerFrame {set; get;};

/// This property returns the number of payload bits
in a frame used for the detection of the BER.

/// If i.e. the errorCounter in the GetCounter()
function is just the checksum error then this
parameter is the number of the payload.

/// </summary>

double NumberOfCountedBitsPerFrame {set; get;};

}

}
```

IBerReader Usage

Each of the methods and properties of this interface are used during test execution. To understand the meaning and duty of the functionality, you must know the point in a test where these functions will be called. A helpful source for understanding the meaning are the comments added for each method in the IBerReader Interface Definition on page 249.

Integration

Copy your compiled version, which is a dll, into the default folder, the path for which is *C:\Program Files\Keysight\M8070B\Plugins\Mipi\bin* folder. Each application (MIPI CPhy, MIPI DPhy, MIPI MPhy, SATA) has a separate program files folder which is named like the application name. The IBerReader Interface Defintion is identified and loaded according to the name of the dll (MIPI C-Phy: CPhyCustomBerReader.dll, MIPI D-Phy: DPhyCustomBerReader.dll, MIPI M-Phy: MPhyCustomBerReader.dll, SATA: SataCustomBerReader.dll) from the sub folder *Plugins\Mipi\bin* of the *C:\Program Files\Keysight\M8070B* folder. If the custom BER reader implementation needs support from other helper DLL files other then the existing PlugIn DLLs, you must place such DLL files also in the same folder location or they must be made available via the PATH variable Windows.

If loaded successfully, a new entry in the BerReader list of the Configure DUT dialog is visible. After selection of the “Custom BER Reader”, the address field becomes editable, and the text of the address field is used as the argument for the Init (string address) method.

Connect/Disconnect

If the operator presses the Start button in the user interface, which is the start of the execution of the test list, the Connect(string address) is called, before the execution of the first test. If this fails with an exception, the test automation aborts the execution. The Init string is needed to check why the connect function did not work. Check the functionality by using the Test GUI with the same text in the address field. At the end of each run, the Disconnect() method is called. A run is the time between the press on the start button and the final completed dialog, which is shown at the end. In case that the repetition parameter is greater than zero, the Disconnect() method is called after the last repetition.

Init

Init(string mode) is called once at the beginning of each test. The default parameters are set for the signaling and it is expected that the DUT can handle these default levels and timings at the RX side.

The content of the argument string “mode” is application dependent and needs to be requested from the application specific documentation. A more direct way to find out the exact string which is given as mode is to apply a break point in the Init method, and verify the setting for each test. In some applications like M-Phy, the argument of the mode string is available via the property grid and can even be modified for each test individually.

ResetDUT and GetCounter

ResetDut() is called just before each test point. It should be used to reset the bit and error counter and re-initialize the DUT to be ready for testing. A RX test procedure requires in the most cases several test points. For example, during a voltage sensitivity test several voltages are set and for each test point, a ResetDUT() is called. After the ResetDUT(), the test automation waits with the GetCounter(out double bitCounter, out double errorCounter) until the expected number of bits are transmitted. The number of bits depend on the target bit error rate and the confidence level that must be attained. As a simple calculation, the number of bits that must be compared is about three times of the target BER. Example target BER: 1e-10, Data Rate 1 GBit/s ? 3e10 bits are required ? 30 seconds test time is needed for each test point.

For a target BER below 1e-9, it may be suitable to request the bit and error counter before the theoretical integration time is reached to speed up the testing in case that errors are already visible. In this case, the test automation calls the GetCounter() method several times for each test point. It is expected that the bit and the error counters will not be reseted by these calls.

Configuration and Conditions

GetReadCounterWithoutStopSupported() is called before each test point. If the return value is true, then no Stop() or Start() methods are called. For some implementation, it is necessary to stop the execution of the bit comparison (see "LogicAnalyserBerReader"), before it is possible to read out the counter.

NumberOfBitsPerFrame and NumberOfCountedBitsPerFrame is used to compute the test time and BER. By these properties, it is possible to give a frame counter instead of a bit counter in the GetCounter() function. The

BER is calculated in this case by multiplying the bit counter with the NumberOfCountedBitsPerFrame. In applications where the data stream contains blanking periods, or bits which are not be taken into account for the bit comparison, the NumberOfBitsPerFrame and NumberOfCountedBitsPerFrame will be different, and the test time is extended. The values for these parameters depend on the pattern which is used for testing. For some applications the test pattern is well defined, but the test automation allows to use another one. In this case the IBerReader should provide suitable values for these parameters.

Example Code Description

The SDK for implementing the IBerReader interface comes with several example Visual Studio Projects and a project containing a test user interface, to test the implementation beforehand. The projects are:

- IBerReaderTestGui: project for building the IBerReader Test GUI. Via this GUI the functionality of the own implementation can be tested.
- LogicAnalyserBerReader: implementation using a logic analyzer as configuration tool and error detector.
- MipiCustomBerReader: example code with empty method implementations, which can be used as start for the own implementation.
- OfflineBerReader: example code for an offline BER reader. Instead of a direct access to a tool that configures the DUT, dialogs are shown to let the user do the configuration, and finally ask, if the DUT is working properly.

IBerReader Test GUI

The Test GUI allows to test the own implementation of a CustomBerReader. The GUI allows you to execute all methods of the IBerReader implementation. Since the source code is available, debugging can be done via this user interface.

MipiCustomBerReader

The MIPICustomBerReader project contains an empty CustomBerReader class. All necessary methods and properties are available but just contains a throw new Exception (“Not implemented.”) call. This project can be used as a template for implementation.

OfflineBerReader

The OfflineBerReader project contains the implementation of an “offline” version of a IBerReader supporting class. All methods show a dialog to the operator instead of calling the DUT or tools directly. It can be used to see when and how the IBerReader methods are used inside of the test automation.

LogicAnalyserBerReader

The LogicAnalyserBerReader IBerReader implementation enables controlling of the Logic Analyser (LA). In this application, the LA configures the device via the pattern generator modules, and the analyser modules are connected to the parallel interface of the DUT. Via this parallel interface, the same data which are received via the high speed MIPI D-PHY interface are sampled, and via a special trigger setup the pattern is compared. The counter of the trigger are used for gaining the number of received bursts, and the number of errors. The configuration of the DUT is done by loading and executing a LA pattern generator setup file, and the setup for the analyser contains the necessary port assignment for the PPI. To create a suitable setup for the actual DUT is under your control.

Debugging

Debugging using the Test GUI

The easiest way for debugging is using the Test GUI. The source code is available and therefore, it is possible to set break points in each method which is using the IBerReader functionality. If the developer puts the project of the IBerReader implementation in the same Visual Studio solution, it follows the source lines of the IBerReader class in case of stepwise running the debugger (Keys F10, step over, and F11, step into). To get a reasonable signal at the inputs of the DUT the test automation, a frame generator, or any other signal source, which can generate signals, conforming to the specification, can be used. If the test automation is used, either the offline BER reader can be used to stop the execution of the test at each IBerReader call, or the compiled DLL. If the compiled DLL is used, it makes more sense to use the test automation as startup application for debug than the Test GUI. Using the frame generator as controller for the signal sources is the most flexible way, because by the frame generator all parameters can be set in the optimum range to test the error free behavior of the DUT, and setting one parameter at the edge of the DUT capability, the error counter functionality can be tested.

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