Keysight D9040USBC USB4 Test Application

KEYSIGHT

PROGRAMMER'S REFERENCE

Notices

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CAUTION

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WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

In This Book

This book is your guide to programming the Keysight Technologies D9040USBC USB4 Test Application.

- Chapter 1, “Introduction to Programming,” starting on page 7, describes compliance application programming basics.
- Chapter 2, “Configuration Variables and Values,” starting on page 9, Chapter 3, “Test Names and IDs,” starting on page 37, and Chapter 4, “Instruments,” starting on page 105 provide information specific to programming the D9040USBC USB4 Test Application.

How to Use This Book

Programmers who are new to compliance application programming should read all of the chapters in order. Programmers who are already familiar with this may review chapters 2, 3, and 4 for changes.

Contents

1 Introduction to Programming

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This chapter introduces the basics for remote programming a compliance/test application. The programming commands provide the means of remote control. Basic operations that you can do remotely with a computer and a compliance/test app running on an oscilloscope include:

- Launching and closing the application.
- Configuring the options.
- Running tests.
- Getting results.
- Controlling when and were dialogs get displayed
- Saving and loading projects.

You can accomplish other tasks by combining these functions.

Remote Programming Toolkit

The majority of remote interface features are common across all the Keysight Technologies, Inc. family of compliance/test applications. Information on those features is provided in the N5452A Compliance Application Remote Programming Toolkit available for download from Keysight here: www.keysight.com/find/rpi. The D9040USBC USB4 Test Application uses Remote Interface Revision 7.2. The help files provided with the toolkit indicate which features are supported in this version.

In the toolkit, various documents refer to "application-specific configuration variables, test information, and instrument information". These are provided in Chapters 2, 3, and 4 of this document, and are also available directly from the application's user interface when the remote interface is enabled (View>Preferences::Remote tab::Show remote interface hints). See the toolkit for more information.

2 Configuration Variables and Values

The following table contains a description of each of the D9040USBC USB4 Test Application options that you may query or set remotely using the appropriate remote interface method. The columns contain this information:

- GUI Location – Describes which graphical user interface tab contains the control used to change the value.
- Label – Describes which graphical user interface control is used to change the value.
- Variable – The name to use with the SetConfig method.
- Values – The values to use with the SetConfig method.
- Description – The purpose or function of the variable.

For example, if the graphical user interface contains this control on the **Set Up** tab:

- Enable Advanced Features

then you would expect to see something like this in the table below:

Table 1 Example Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Set Up	Enable Advanced Features	EnableAdvanced	True, False	Enables a set of optional features.

and you would set the variable remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SetConfig 'EnableAdvanced' 'True'"

C# syntax
```

```
---------
remoteAte.SetConfig("EnableAdvanced", "True");
```

Here are the actual configuration variables and values used by this application:

NOTE Some of the values presented in the table below may not be available in certain configurations. Always perform a "test run" of your remote script using the application's graphical user interface to ensure the combinations of values in your program are valid.

NOTE The file, "ConfigInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 2 Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Configure	Acquisition number for TP3 Jitter Analysis	CTLECalibrationAcqNum	(Accepts user-defined text), 1, 5	Select the number of signal acquisition for TP3 jitter analysis.
Configure	Automation Auto Retry Count	AutomationAutoRetryCount	(Accepts user-defined text), 0, 1, 3, 5, 10	Select the number of auto retry for automation if the signal pattern check fail. Select [0] if user want the automation error shown without any auto retry.
Configure	Automation Timeout	AutomationTimeout	(Accepts user-defined text), 200	Select the controller automation timeout. Unit: Second.
Configure	Cable Model	EnableCableModel	true, false	Select whether to enable or disable the cable model used in the TP3 transmitter tests.
Configure	Cal Set Name	CALName	(Accepts user-defined text), None	Enter the Cal Set Name
Configure	Configure DUT respond time (ms)	ConfigureDUTRespond	(Accepts user-defined text), 1000, 2000, 3000, 4000, 5000	Configure the DUT respond time.
Configure	Configure Preset Number	ConfigurePresetNumber	1.0, 0.0	Select whether to enable or disable the configure preset number message prompt.
Configure	Connection prompt for MH2 Chipset	FVTPrompt	False, True	Select the option for message prompt

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Correction State	CalCorrectionState	OFF, ON	Select the Cal correction state (default is off)
Configure	Frequency Variation Acquisition Number	FreqVarAcqNum	(Accepts user-defined text), 1, 5, 10, 15, 20	Select the number of signal acquisition for live signal analysis (Signal Acquisition Method = [Live]) of Frequency Variation Training.
Configure	Gating Shape	RLGateShape	(Accepts user-defined text), NORMal, MAXimum, WIDE, MINimum	Configure the gate Shape.
Configure	Gating State	RLGateState	OFF, ON	Select the Gating state (default is off)
Configure	Gating Time Start	RLGateStart	(Accepts user-defined text), -69e-12	Configure the Start time.
Configure	Gating Time Stop	RLGateStop	(Accepts user-defined text), 1.095e-9	Configure the Stop time.
Configure	Gating Type	RLGateType	(Accepts user-defined text), NOTCh, BPASs	Configure the gate type.
Configure	Lane 0 Connection	L0Connection	5, 6, 7	Select the input channel for the Lane 0.
Configure	Lane 1 Connection	L1Connection	6, 5, 7	Select the input channel for the Lane 1.
Configure	Measurement Hysteresis	MeasurementHysteresis	(Accepts user-defined text), 0.008, 0.020	Set the measurement hysteresis for single-ended signal and differential signal in USB4 tests, except electrical idle. Unit: Volt.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Measurement Threshold Level	MeasurementThresholdLevel	(Accepts user-defined text), Auto, 0.00, 0.05	Set the measurement threshold level for single-ended signal and differential signal in USB4 tests, except Tx Electrical Idle Voltage tests. Unit: Volt. For [Auto], the USB 4 application will set the measurement threshold level to 0V if the middle voltage of the signal is within +/-100mV, else the measurement threshold level will set to middle voltage of the signal.
Configure	Pattern Check	EnableSignalCheck	1.0, 0.0	When pattern check is enabled, the input signal will be verified within reasonable range of timing and voltage limits. It will assist to detecting problems such as cabling errors before running a test.
Configure	Preset Calibration Acquisition Number	PresetCalibrationAcqNum	(Accepts user-defined text), 1, 5, 10, 15	Select the number of signal acquisition for live signal analysis (Signal Acquisition Method = [Live]) of Preset Calibration.
Configure	Preset Calibration DUT Type	PresetCalDUTType	Router, Receptacle	Select whether to setup DUT Type as Router or Receptacle while using USB4 controller
Configure	Replace TP3 PRBS31 waveform or recapture waveform	CTLECalibrationReplaceWav	true, false	Select true if want to replace the TP3 PRBS31 waveform in each run
Configure	Rx Cal Set Name	RxCALName	(Accepts user-defined text), None	Enter the Cal Set Name
Configure	Rx Correction State	RxCalCorrectionState	OFF, ON	Select the Cal correction state (default is off)
Configure	Rx Gating Shape	RxRLGateShape	(Accepts user-defined text), NORMal, MAXimum, WIDE, MINimum	Configure the gate Shape.
Configure	Rx Gating State	RxRLGateState	OFF, ON	Select the Rx Gating state (default is off)

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Rx Gating Time Start	RxRLGateStart	(Accepts user-defined text), -40e-12	Configure the Start time.
Configure	Rx Gating Time Stop	RxRLGateStop	(Accepts user-defined text), 4.33e-9	Configure the Stop time.
Configure	Rx Gating Type	RxRLGateType	(Accepts user-defined text), NOTCh, BPASs	Configure the gate type.
Configure	SBTX Test Pattern	SBTXPattern	SBTX	Select the test pattern used for SBTX measurement.
Configure	SBTX Trigger Level	SBTXTriggerThreshold	(Accepts user-defined text), 600.0E-03	Set the trigger level for SBTX test Unit: Volt.
Configure	SBU1 Connection	SBU1Connection	CHAN1, CHAN2, CHAN3, CHAN4	Select the input channel for the SBU1.
Configure	SBU2 Connection	SBU2Connection	CHAN1, CHAN2, CHAN3, CHAN4	Select the input channel for the SBU2.
Configure	Sample Size - AC Common Mode Voltage - PRBS31	SampSize_MemPts_ACCM_Live	(Accepts user-defined text), 337.5e-6, 500e-6	Select the time range used for acquiring signal for live signal analysis of AC Common Mode Voltage Measurement. Unit: seconds.
Configure	Sample Size - All Pattern (Live)	SampSize_MemPts_TBT3_Live	(Accepts user-defined text), 50e-6, 500e-6	Select the time range used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]), except Rise/Fall Time, Eye Diagram, Unit Interval, SSC, Equalization and Electrical Idle tests. Unit: seconds.
Configure	Sample Size - Electrical Idle	SampSize_MemPts_ElectricalIdle_Live	(Accepts user-defined text), 125e-6, 500e-6	Select the time range used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]) of Electrical Idle Voltage tests. Unit: seconds.
Configure	Sample Size - Equalization - SQ128	SampSize_MemPts_Equalization_Live	(Accepts user-defined text), 2.97e-6, 500e-6	Select the time range used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]) of Equalization tests. Unit: seconds.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Sample Size - Frequency Variation (Live)	SampSize_MemPts_FrequencyVariation_Live	(Accepts user-defined text), 337.5e-6, 500e-6	Select the time range used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]) of Frequency Variation tests. Unit: Mpts.
Configure	Sample Size - Jitter - TP2 - PRBS15	SampSize_MemPts_Jitter_Live	(Accepts user-defined text), 50e-6, 500e-6	Select the time range used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]), only for jitter tests. Unit: seconds.
Configure	Sample Size - Jitter - TP3 - PRBS31	SampSize_EyeDiagram_Live	(Accepts user-defined text), 50e-6, 125e-6, 500e-6	Select the time range used for acquiring signal for TP3-PRBS31 for TP3 jitter analysis and eye diagram measurement. Unit: seconds.
Configure	Sample Size - Preset Calibration - PRBS15	SampSize_PresetCal_Live	(Accepts user-defined text), 50e-6, 125e-6, 500e-6	Select the time range used for acquiring signal for Preset Calibration test. Unit: seconds.
Configure	Sample Size - Rise/Fall Time - SQ128	SampSize_MemPts_RiseFall_Live	(Accepts user-defined text), 50e-6, 500e-6	Select the time range used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]) of Rise/Fall Time tests. Unit: seconds.
Configure	Sample Size - SBRX (Live)	SampSize_MemPts_SBRX_Live	(Accepts user-defined text), 1.5e-3	Select the time range used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]) of SBTX tests. Unit: Mpts.
Configure	Sample Size - SBTX (Live)	SampSize_MemPts_SBTX_Live	(Accepts user-defined text), 200e-6	Select the time range used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]) of SBTX tests. Unit: Mpts.
Configure	Sample Size - Unit Interval, SSC and TP2 Eye Diagram measurement - PRBS31	SampSize_MemPts_UI_SSC_Live	(Accepts user-defined text), 337.5e-6, 500e-6	Select the time range used for acquiring signal for live signal analysis of Unit Interval, SSC Modulation and TP2 Eye Diagram tests. Unit: seconds.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Sampling Rate	SampRate	80.0E9, 40.0E9, 128.0E9, 64.0E9, 32.0E9	Select the sampling rate that must be used to acquire the waveform(s) for all USB4 tests. Unit: Sa/s.
Configure	Sampling Rate (Side Band Test)	SampRateSB	1.0E9, 20.0E9, 40.0E9, 1.0E9, 16.0E9, 32.0E9	Select the sampling rate that must be used to acquire the waveform(s) for all side band test. Unit: Sa/s.
Configure	Screenshot Image Size	ScreenShotImageSize	GRAT, SCR	Select the screenshot image size for the report items.
Configure	Side Band Acquisition Bandwidth	SideBandAcqBW	(Accepts user-defined text), 0, 1.0E9	Select the acquisition bandwidth for Side Band Test. (Default value is 0, which will set the bandwidth to "Auto")
Configure	Signal Trigger Level	TriggerThreshold	(Accepts user-defined text), 0.0, 50.0E-03, 100.0E-03, 150.0E-03, 200.0E-03, 250.0E-03, 300.0E-03, 350.0E-03, 400.0E-03, 450.0E-03, 500.0E-03, 550.0E-03, 600.0E-03	Set the trigger level for all the signal in USB4 tests. Unit: Volt.
Configure	Starting Test pattern in frequency variation training	FVTInitPattern	SQ2, SQ128	Select the starting Test Pattern
Configure	Tx Equalization Preset	TxEqualization_Preset	ALL, P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select ALL for all Preset numbers or select specific Preset number to test.
Configure	VNA BAL Port (Negative)	VNAPortNeg	2, 3	VNA Balance Port Negative
Configure	VNA BAL Port (Positive)	VNAPortPos	1	VNA Balance Port Positive

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	frequency variation training Trigger Level	FVTTriggerThreshold	(Accepts user-defined text), 0.0, 50.0E-03, 100.0E-03	Set the trigger level for frequency variation training Unit: Volt.
Run Tests	Event	RunEvent	(None), Fail, Margin < N, Pass	Names of events that can be used with the StoreMode=Event or RunUntil RunEventAction options
Run Tests	RunEvent=Margin < N: Minimum required margin %	RunEvent_Margin < N_MinPercent	Any integer in range: 0 <= value <= 99	Specify N using the 'Minimum required margin %' control.
Set Up	10 Gb/s	10 Gb/s	0.0, 1.0	Select whether the DUT support 10 Gb/s bit rate. Select whether the DUT support 10 Gb/s bit rate.
Set Up	10.3125 Gb/s	10.3125 Gb/s	0.0, 1.0	Select whether the DUT support 10.3125 Gb/s bit rate. Select whether the DUT support 10.3125 Gb/s bit rate.
Set Up	20 Gb/s	20 Gb/s	0.0, 1.0	Select whether the DUT support 20 Gb/s bit rate. Select whether the DUT support 20 Gb/s bit rate.
Set Up	20.625 Gb/s	20.625 Gb/s	0.0, 1.0	Select whether the DUT support 20.625 Gb/s bit rate. Select whether the DUT support 20.625 Gb/s bit rate.
Set Up	Automation Controller	AutomationController	TCPIP, USB4-TPA-UC	Select the type of Thunderbolt Automation Controller. Select the type of Thunderbolt Automation Controller.
Set Up	CTLE DC Gain 0dB	DC0dB	0.0, 1.0	Enable or disable 0dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 0dB CTLE DC Gain for the CTLE Calibration Run.
Set Up	CTLE DC Gain 1dB	DC1dB	0.0, 1.0	Enable or disable 1dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 1dB CTLE DC Gain for the CTLE Calibration Run.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	CTLE DC Gain 2dB	DC2dB	0.0, 1.0	Enable or disable 2dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 2dB CTLE DC Gain for the CTLE Calibration Run.
Set Up	CTLE DC Gain 3dB	DC3dB	0.0, 1.0	Enable or disable 3dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 3dB CTLE DC Gain for the CTLE Calibration Run.
Set Up	CTLE DC Gain 4dB	DC4dB	0.0, 1.0	Enable or disable 4dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 4dB CTLE DC Gain for the CTLE Calibration Run.
Set Up	CTLE DC Gain 5dB	DC5dB	0.0, 1.0	Enable or disable 5dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 5dB CTLE DC Gain for the CTLE Calibration Run.
Set Up	CTLE DC Gain 6dB	DC6dB	0.0, 1.0	Enable or disable 6dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 6dB CTLE DC Gain for the CTLE Calibration Run.
Set Up	CTLE DC Gain 7dB	DC7dB	0.0, 1.0	Enable or disable 7dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 7dB CTLE DC Gain for the CTLE Calibration Run.
Set Up	CTLE DC Gain 8dB	DC8dB	0.0, 1.0	Enable or disable 8dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 8dB CTLE DC Gain for the CTLE Calibration Run.
Set Up	CTLE DC Gain 9dB	DC9dB	0.0, 1.0	Enable or disable 9dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 9dB CTLE DC Gain for the CTLE Calibration Run.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Cable Type	CableType	1m Cable, Custom	Select the cable type used for testing. Select the cable type used for testing.
Set Up	Captive Device option	CaptiveDevice	0.0, 1.0	This is a Captive Device if checked the checkbox. This is a Captive Device
Set Up	Consumer Power Profile 1	ConsumerPowerProfile1	0.0, 1.0	Enable or disable Consumer Power Profile 1 support. Enable or disable Consumer Power Profile 1 support.
Set Up	Consumer Power Profile 2	ConsumerPowerProfile2	0.0, 1.0	Enable or disable Consumer Power Profile 2 support. Enable or disable Consumer Power Profile 2 support.
Set Up	Consumer Power Profile 3	ConsumerPowerProfile3	0.0, 1.0	Enable or disable Consumer Power Profile 3 support. Enable or disable Consumer Power Profile 3 support.
Set Up	Custom Cable De-Embed Mode	CustomCableMode	Same s-parameter file for Lane 0 and Lane 1, Different s-parameter file for Lane 0 and Lane 1	Select the custom cable de-embed mode. Select the custom cable de-embed mode.
Set Up	Custom Cable S-Parameter File	CustomCableSParameterFile	(Accepts user-defined text)	Select the custom cable s-parameter file used for testing. This s-parameter file only applicable if cable de-embed is enabled, Custom cable and same s-parameter file are selected. Select the custom cable s-parameter file used for testing. This s-parameter file only applicable if cable de-embed is enabled, Custom cable and same s-parameter file are selected.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Custom Cable S-Parameter File (Lane 0)	Lane0CustomCableSParameterFile	(Accepts user-defined text)	Select the custom cable s-parameter file used for lane 0 testing. This s-parameter file only applicable if cable de-embed is enabled, Custom cable and different s-parameter file are selected. Select the custom cable s-parameter file used for lane 0 testing. This s-parameter file only applicable if cable de-embed is enabled, Custom cable and different s-parameter file are selected.
Set Up	Custom Cable S-Parameter File (Lane 1)	Lane1CustomCableSParameterFile	(Accepts user-defined text)	Select the custom cable s-parameter file used for lane 1 testing. This s-parameter file only applicable if cable de-embed is enabled, Custom cable and different s-parameter file are selected. Select the custom cable s-parameter file used for lane 1 testing. This s-parameter file only applicable if cable de-embed is enabled, Custom cable and different s-parameter file are selected.
Set Up	Custom Fixture De-Embed Mode	CustomFixtureMode	Same s-parameter file for Lane 0 and Lane 1, Different s-parameter file for Lane 0 and Lane 1	Select the custom fixture de-embed mode. Select the custom fixture de-embed mode.
Set Up	Custom Fixture S-Parameter File	CustomFixtureSParameterFile	(Accepts user-defined text)	Select the custom fixture s-parameter file used for testing. This s-parameter file only applicable if fixture de-embed is enabled, Custom fixture and same s-parameter file are selected. Select the custom fixture s-parameter file used for testing. This s-parameter file only applicable if fixture de-embed is enabled, Custom fixture and same s-parameter file are selected.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Custom Fixture S-Parameter File (Lane 0)	Lane0CustomFixtureSParameterFile	(Accepts user-defined text)	Select the custom fixture s-parameter file used for lane 0 testing. This s-parameter file only applicable if fixture de-embed is enabled, Custom fixture and different s-parameter file are selected. Select the custom fixture s-parameter file used for lane 0 testing. This s-parameter file only applicable if fixture de-embed is enabled, Custom fixture and different s-parameter file are selected.
Set Up	Custom Fixture S-Parameter File (Lane 1)	Lane1CustomFixtureSParameterFile	(Accepts user-defined text)	Select the custom fixture s-parameter file used for lane 1 testing. This s-parameter file only applicable if fixture de-embed is enabled, Custom fixture and different s-parameter file are selected. Select the custom fixture s-parameter file used for lane 1 testing. This s-parameter file only applicable if fixture de-embed is enabled, Custom fixture and different s-parameter file are selected.
Set Up	DUT Orientation (USB Type-C)	DUTOrientation	Normal, Inverted	Select the orientation type, either 'Normal' or 'Inverted' for USB Type-C DUT. Select the orientation type, either 'Normal' or 'Inverted' for USB Type-C DUT.
Set Up	DUT Type	DUTType	Device, Host	Select the device type of the DUT, either 'Device' or 'Host'. Select the device type of the DUT, either 'Device' or 'Host'.
Set Up	Device Identifier	DeviceIdentifier	(Accepts user-defined text)	Identifier for the DUT in testing. Identifier for the DUT in testing.
Set Up	Enable Automation Controller	AutomationEnable	0.0, 1.0	Enable or disable the use of Thunderbolt Automation Controller. Enable or disable the use of Thunderbolt Automation Controller.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Enable CTLE Calibration	cfgCTLECal	0.0, 1.0	Enable or disable CTLE calibration to find the optimum CTLE DC Gain. Enable or disable CTLE calibration to find the optimum CTLE DC Gain.
Set Up	Enable Cable De-Embed	EnableCableDeEmbed	0.0, 1.0	Enable or disable cable de-embed to remove the losses. Enable or disable cable de-embed to remove the losses.
Set Up	Enable Fixture De-Embed	EnableFixtureDeEmbed	0.0, 1.0	Enable or disable fixture de-embed to remove the losses. Enable or disable fixture de-embed to remove the losses.
Set Up	Enable Predefined CTLE DC Gain	cfgPredefinedDCgain	0.0, 1.0	Enable or disable to predefined optimum CTLE DC Gain. Enable or disable to predefined optimum CTLE DC Gain.
Set Up	Enable Predefined Preset Number	cfgPredefinedPresetNum	0.0, 1.0	Enable or disable predefined optimum Preset Number. Enable or disable predefined optimum Preset Number.
Set Up	Enable Preset Calibration	cfgPresetCal	0.0, 1.0	Enable or disable preset calibration run to find the optimum Preset Number. Enable or disable preset calibration run to find the optimum Preset Number.
Set Up	Enable Saved Waveform	EnableSavedWaveform	0.0, 1.0	Enable or disable the use of saved waveform in the tests. Enable or disable the use of saved waveform in the tests.
Set Up	Enable Type-C Controller Automation	TCTCEnabled	0.0, 1.0	Enable or disable USB Type-C Test Controller automation. Enable or disable USB Type-C Test Controller automation.
Set Up	Fixture Type	FixtureType	N7015A (Including Plug), N7015A (Not Including Plug), Custom	Select the fixture type used for testing. Select the fixture type used for testing.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	PRBS11_NegSignal Directory	PRBS11_Neg_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS11 negative signal waveform. This variable use to store the directory of PRBS11 negative signal waveform.
Set Up	PRBS11_PosSignal Directory	PRBS11_Pos_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS11 positive signal waveform. This variable use to store the directory of PRBS11 positive signal waveform.
Set Up	PRBS31_NegSignal Directory	PRBS31_Neg_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS31 negative signal waveform. This variable use to store the directory of PRBS31 negative signal waveform.
Set Up	PRBS31_PosSignal Directory	PRBS31_Pos_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS31 positive signal waveform. This variable use to store the directory of PRBS31 positive signal waveform.
Set Up	PRBS9_NegSignalD irectory	PRBS9_Neg_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS9 negative signal waveform. This variable use to store the directory of PRBS9 negative signal waveform.
Set Up	PRBS9_PosSignalD irectory	PRBS9_Pos_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS9 positive signal waveform. This variable use to store the directory of PRBS9 positive signal waveform.
Set Up	Port Number	PortNumber	1 Port, 2 Ports	Select the number of ports supported by the DUT. Select the number of ports supported by the DUT.
Set Up	Port1 Name	Port1Name	(Accepts user-defined text), Port 1, (SELECT OR TYPE)	Set the port name for the first port. This field will be show in report. Set the port name for the first port. This field will be show in report.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Port2 Name	Port2Name	(Accepts user-defined text), Port 2, (SELECT OR TYPE)	Set the port name for the second port. This field will be show in report. Set the port name for the second port. This field will be show in report.
Set Up	Predefined CTLE DC Gain (10 Gb/s) (Port 1, Lane 0)	PredefinedCTLEDCGain10GbpsPort1Lane0	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 10 Gb/s tests of Port 1, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 10 Gb/s TP3 tests of Port 1, Lane 0. Select the predefined optimum CTLE DC Gain for bit rate 10 Gb/s tests of Port 1, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 10 Gb/s TP3 tests of Port 1, Lane 0.
Set Up	Predefined CTLE DC Gain (10 Gb/s) (Port 1, Lane 1)	PredefinedCTLEDCGain10GbpsPort1Lane1	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 10 Gb/s tests of Port 1, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 10 Gb/s TP3 tests of Port 1, Lane 1. Select the predefined optimum CTLE DC Gain for bit rate 10 Gb/s tests of Port 1, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 10 Gb/s TP3 tests of Port 1, Lane 1.
Set Up	Predefined CTLE DC Gain (10 Gb/s) (Port 2, Lane 0)	PredefinedCTLEDCGain10GbpsPort2Lane0	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 10 Gb/s tests of Port 2, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 10 Gb/s TP3 tests of Port 2, Lane 0. Select the predefined optimum CTLE DC Gain for bit rate 10 Gb/s tests of Port 2, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 10 Gb/s TP3 tests of Port 2, Lane 0.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined CTLE DC Gain (10 Gb/s) (Port 2, Lane 1)	PredefinedCTLEDCGain10GbpsPort2Lane1	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 10 Gb/s tests of Port 2, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 10 Gb/s TP3 tests of Port 2, Lane 1. Select the predefined optimum CTLE DC Gain for bit rate 10 Gb/s tests of Port 2, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 10 Gb/s TP3 tests of Port 2, Lane 1.
Set Up	Predefined CTLE DC Gain (10.3125 Gb/s) (Port 1, Lane 0)	PredefinedCTLEDCGain10_3125GbpsPort1Lane0	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 10.3125 Gb/s tests of Port 1, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 10.3125 Gb/s TP3 tests of Port 1, Lane 0. Select the predefined optimum CTLE DC Gain for bit rate 10.3125 Gb/s tests of Port 1, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 10.3125 Gb/s TP3 tests of Port 1, Lane 0.
Set Up	Predefined CTLE DC Gain (10.3125 Gb/s) (Port 1, Lane 1)	PredefinedCTLEDCGain10_3125GbpsPort1Lane1	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 10.3125 Gb/s tests of Port 1, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 10.3125 Gb/s TP3 tests of Port 1, Lane 1. Select the predefined optimum CTLE DC Gain for bit rate 10.3125 Gb/s tests of Port 1, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 10.3125 Gb/s TP3 tests of Port 1, Lane 1.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined CTLE DC Gain (10.3125 Gb/s) (Port 2, Lane 0)	PredefinedCTLEDCGain10_3125GbpsPort2Lane0	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 10.3125 Gb/s tests of Port 2, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 10.3125 Gb/s TP3 tests of Port 2, Lane 0. Select the predefined optimum CTLE DC Gain for bit rate 10.3125 Gb/s tests of Port 2, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 10.3125 Gb/s TP3 tests of Port 2, Lane 0.
Set Up	Predefined CTLE DC Gain (10.3125 Gb/s) (Port 2, Lane 1)	PredefinedCTLEDCGain10_3125GbpsPort2Lane1	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 10.3125 Gb/s tests of Port 2, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 10.3125 Gb/s TP3 tests of Port 2, Lane 1. Select the predefined optimum CTLE DC Gain for bit rate 10.3125 Gb/s tests of Port 2, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 10.3125 Gb/s TP3 tests of Port 2, Lane 1.
Set Up	Predefined CTLE DC Gain (20 Gb/s) (Port 1, Lane 0)	PredefinedCTLEDCGain20GbpsPort1Lane0	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 20 Gb/s tests of Port 1, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 20 Gb/s TP3 tests of Port 1, Lane 0. Select the predefined optimum CTLE DC Gain for bit rate 20 Gb/s tests of Port 1, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 20 Gb/s TP3 tests of Port 1, Lane 0.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined CTLE DC Gain (20 Gb/s) (Port 1, Lane 1)	PredefinedCTLEDCGain20GbpsPort1Lane1	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 20 Gb/s tests of Port 1, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 20 Gb/s TP3 tests of Port 1, Lane 1. Select the predefined optimum CTLE DC Gain for bit rate 20 Gb/s tests of Port 1, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 20 Gb/s TP3 tests of Port 1, Lane 1.
Set Up	Predefined CTLE DC Gain (20 Gb/s) (Port 2, Lane 0)	PredefinedCTLEDCGain20GbpsPort2Lane0	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 20 Gb/s tests of Port 2, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 20 Gb/s TP3 tests of Port 2, Lane 0. Select the predefined optimum CTLE DC Gain for bit rate 20 Gb/s tests of Port 2, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 20 Gb/s TP3 tests of Port 2, Lane 0.
Set Up	Predefined CTLE DC Gain (20 Gb/s) (Port 2, Lane 1)	PredefinedCTLEDCGain20GbpsPort2Lane1	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 20 Gb/s tests of Port 2, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 20 Gb/s TP3 tests of Port 2, Lane 1. Select the predefined optimum CTLE DC Gain for bit rate 20 Gb/s tests of Port 2, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 20 Gb/s TP3 tests of Port 2, Lane 1.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined CTLE DC Gain (20.625 Gb/s) (Port 1, Lane 0)	PredefinedCTLEDCGain20_625GbpsPort1Lane0	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 20.625 Gb/s tests of Port 1, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 20.625 Gb/s TP3 tests of Port 1, Lane 0. Select the predefined optimum CTLE DC Gain for bit rate 20.625 Gb/s tests of Port 1, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 20.625 Gb/s TP3 tests of Port 1, Lane 0.
Set Up	Predefined CTLE DC Gain (20.625 Gb/s) (Port 1, Lane 1)	PredefinedCTLEDCGain20_625GbpsPort1Lane1	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 20.625 Gb/s tests of Port 1, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 20.625 Gb/s TP3 tests of Port 1, Lane 1. Select the predefined optimum CTLE DC Gain for bit rate 20.625 Gb/s tests of Port 1, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 20.625 Gb/s TP3 tests of Port 1, Lane 1.
Set Up	Predefined CTLE DC Gain (20.625 Gb/s) (Port 2, Lane 0)	PredefinedCTLEDCGain20_625GbpsPort2Lane0	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 20.625 Gb/s tests of Port 2, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 20.625 Gb/s TP3 tests of Port 2, Lane 0. Select the predefined optimum CTLE DC Gain for bit rate 20.625 Gb/s tests of Port 2, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 20.625 Gb/s TP3 tests of Port 2, Lane 0.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined CTLE DC Gain (20.625 Gb/s) (Port 2, Lane 1)	PredefinedCTLEDCGain20_625GbpsPort2Lane1	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 20.625 Gb/s tests of Port 2, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 20.625 Gb/s TP3 tests of Port 2, Lane 1. Select the predefined optimum CTLE DC Gain for bit rate 20.625 Gb/s tests of Port 2, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 20.625 Gb/s TP3 tests of Port 2, Lane 1.
Set Up	Predefined Preset Number (10 Gb/s) (Port 1, Lane 0)	PredefinedPresetNumber10GbpsPort1Lane0	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 10 Gb/s tests of Port 1, Lane 0. The optimum Preset Number will be used to run the bit rate 10 Gb/s tests of Port 1, Lane 0. Select the predefined optimum Preset Number for bit rate 10 Gb/s tests of Port 1, Lane 0. The optimum Preset Number will be used to run the bit rate 10 Gb/s tests of Port 1, Lane 0.
Set Up	Predefined Preset Number (10 Gb/s) (Port 1, Lane 1)	PredefinedPresetNumber10GbpsPort1Lane1	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 10 Gb/s tests of Port 1, Lane 1. The optimum Preset Number will be used to run the bit rate 10 Gb/s tests of Port 1, Lane 1. Select the predefined optimum Preset Number for bit rate 10 Gb/s tests of Port 1, Lane 1. The optimum Preset Number will be used to run the bit rate 10 Gb/s tests of Port 1, Lane 1.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined Preset Number (10 Gb/s) (Port 2, Lane 0)	PredefinedPresetNumber10GbpsPort2Lane0	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 10 Gb/s tests of Port 2, Lane 0. The optimum Preset Number will be used to run the bit rate 10 Gb/s tests of Port 2, Lane 0. Select the predefined optimum Preset Number for bit rate 10 Gb/s tests of Port 2, Lane 0. The optimum Preset Number will be used to run the bit rate 10 Gb/s tests of Port 2, Lane 0.
Set Up	Predefined Preset Number (10 Gb/s) (Port 2, Lane 1)	PredefinedPresetNumber10GbpsPort2Lane1	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 10 Gb/s tests of Port 2, Lane 1. The optimum Preset Number will be used to run the bit rate 10 Gb/s tests of Port 2, Lane 1. Select the predefined optimum Preset Number for bit rate 10 Gb/s tests of Port 2, Lane 1. The optimum Preset Number will be used to run the bit rate 10 Gb/s tests of Port 2, Lane 1.
Set Up	Predefined Preset Number (10.3125 Gb/s) (Port 1, Lane 0)	PredefinedPresetNumber10_3125GbpsPort1Lane0	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 10.3125 Gb/s tests of Port 1, Lane 0. The optimum Preset Number will be used to run the bit rate 10.3125 Gb/s tests of Port 1, Lane 0. Select the predefined optimum Preset Number for bit rate 10.3125 Gb/s tests of Port 1, Lane 0. The optimum Preset Number will be used to run the bit rate 10.3125 Gb/s tests of Port 1, Lane 0.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined Preset Number (10.3125 Gb/s) (Port 1, Lane 1)	PredefinedPresetNumber10_3125GbpsPort1Lane1	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 10.3125 Gb/s tests of Port 1, Lane 1. The optimum Preset Number will be used to run the bit rate 10.3125 Gb/s tests of Port 1, Lane 1. Select the predefined optimum Preset Number for bit rate 10.3125 Gb/s tests of Port 1, Lane 1. The optimum Preset Number will be used to run the bit rate 10.3125 Gb/s tests of Port 1, Lane 1.
Set Up	Predefined Preset Number (10.3125 Gb/s) (Port 2, Lane 0)	PredefinedPresetNumber10_3125GbpsPort2Lane0	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 10.3125 Gb/s tests of Port 2, Lane 0. The optimum Preset Number will be used to run the bit rate 10.3125 Gb/s tests of Port 2, Lane 0. Select the predefined optimum Preset Number for bit rate 10.3125 Gb/s tests of Port 2, Lane 0. The optimum Preset Number will be used to run the bit rate 10.3125 Gb/s tests of Port 2, Lane 0.
Set Up	Predefined Preset Number (10.3125 Gb/s) (Port 2, Lane 1)	PredefinedPresetNumber10_3125GbpsPort2Lane1	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 10.3125 Gb/s tests of Port 2, Lane 1. The optimum Preset Number will be used to run the bit rate 10.3125 Gb/s tests of Port 2, Lane 1. Select the predefined optimum Preset Number for bit rate 10.3125 Gb/s tests of Port 2, Lane 1. The optimum Preset Number will be used to run the bit rate 10.3125 Gb/s tests of Port 2, Lane 1.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined Preset Number (20 Gb/s) (Port 1, Lane 0)	PredefinedPresetNumber20GbpsPort1Lane0	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 20 Gb/s tests of Port 1, Lane 0. The optimum Preset Number will be used to run the bit rate 20 Gb/s tests of Port 1, Lane 0. Select the predefined optimum Preset Number for bit rate 20 Gb/s tests of Port 1, Lane 0. The optimum Preset Number will be used to run the bit rate 20 Gb/s tests of Port 1, Lane 0.
Set Up	Predefined Preset Number (20 Gb/s) (Port 1, Lane 1)	PredefinedPresetNumber20GbpsPort1Lane1	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 20 Gb/s tests of Port 1, Lane 1. The optimum Preset Number will be used to run the bit rate 20 Gb/s tests of Port 1, Lane 1. Select the predefined optimum Preset Number for bit rate 20 Gb/s tests of Port 1, Lane 1. The optimum Preset Number will be used to run the bit rate 20 Gb/s tests of Port 1, Lane 1.
Set Up	Predefined Preset Number (20 Gb/s) (Port 2, Lane 0)	PredefinedPresetNumber20GbpsPort2Lane0	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 20 Gb/s tests of Port 2, Lane 0. The optimum Preset Number will be used to run the bit rate 20 Gb/s tests of Port 2, Lane 0. Select the predefined optimum Preset Number for bit rate 20 Gb/s tests of Port 2, Lane 0. The optimum Preset Number will be used to run the bit rate 20 Gb/s tests of Port 2, Lane 0.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined Preset Number (20 Gb/s) (Port 2, Lane 1)	PredefinedPresetNumber20GbpsPort2Lane1	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 20 Gb/s tests of Port 2, Lane 1. The optimum Preset Number will be used to run the bit rate 20 Gb/s tests of Port 2, Lane 1. Select the predefined optimum Preset Number for bit rate 20 Gb/s tests of Port 2, Lane 1. The optimum Preset Number will be used to run the bit rate 20 Gb/s tests of Port 2, Lane 1.
Set Up	Predefined Preset Number (20.625 Gb/s) (Port 1, Lane 0)	PredefinedPresetNumber20_625GbpsPort1Lane0	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 20.625 Gb/s tests of Port 1, Lane 0. The optimum Preset Number will be used to run the bit rate 20.625 Gb/s tests of Port 1, Lane 0. Select the predefined optimum Preset Number for bit rate 20.625 Gb/s tests of Port 1, Lane 0. The optimum Preset Number will be used to run the bit rate 20.625 Gb/s tests of Port 1, Lane 0.
Set Up	Predefined Preset Number (20.625 Gb/s) (Port 1, Lane 1)	PredefinedPresetNumber20_625GbpsPort1Lane1	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 20.625 Gb/s tests of Port 1, Lane 1. The optimum Preset Number will be used to run the bit rate 20.625 Gb/s tests of Port 1, Lane 1. Select the predefined optimum Preset Number for bit rate 20.625 Gb/s tests of Port 1, Lane 1. The optimum Preset Number will be used to run the bit rate 20.625 Gb/s tests of Port 1, Lane 1.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined Preset Number (20.625 Gb/s) (Port 2, Lane 0)	PredefinedPresetNumber20_625GbpsPort2Lane0	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 20.625 Gb/s tests of Port 2, Lane 0. The optimum Preset Number will be used to run the bit rate 20.625 Gb/s tests of Port 2, Lane 0. Select the predefined optimum Preset Number for bit rate 20.625 Gb/s tests of Port 2, Lane 0. The optimum Preset Number will be used to run the bit rate 20.625 Gb/s tests of Port 2, Lane 0.
Set Up	Predefined Preset Number (20.625 Gb/s) (Port 2, Lane 1)	PredefinedPresetNumber20_625GbpsPort2Lane1	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 20.625 Gb/s tests of Port 2, Lane 1. The optimum Preset Number will be used to run the bit rate 20.625 Gb/s tests of Port 2, Lane 1. Select the predefined optimum Preset Number for bit rate 20.625 Gb/s tests of Port 2, Lane 1. The optimum Preset Number will be used to run the bit rate 20.625 Gb/s tests of Port 2, Lane 1.
Set Up	Preset Number 0	P0	0.0, 1.0	Enable or disable Preset Number 0 for the Preset Calibration Run. Enable or disable Preset Number 0 for the Preset Calibration Run.
Set Up	Preset Number 1	P1	0.0, 1.0	Enable or disable Preset Number 1 for the Preset Calibration Run. Enable or disable Preset Number 1 for the Preset Calibration Run.
Set Up	Preset Number 10	P10	0.0, 1.0	Enable or disable Preset Number 10 for the Preset Calibration Run. Enable or disable Preset Number 10 for the Preset Calibration Run.
Set Up	Preset Number 11	P11	0.0, 1.0	Enable or disable Preset Number 11 for the Preset Calibration Run. Enable or disable Preset Number 11 for the Preset Calibration Run.
Set Up	Preset Number 12	P12	0.0, 1.0	Enable or disable Preset Number 12 for the Preset Calibration Run. Enable or disable Preset Number 12 for the Preset Calibration Run.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Preset Number 13	P13	0.0, 1.0	Enable or disable Preset Number 13 for the Preset Calibration Run. Enable or disable Preset Number 13 for the Preset Calibration Run.
Set Up	Preset Number 14	P14	0.0, 1.0	Enable or disable Preset Number 14 for the Preset Calibration Run. Enable or disable Preset Number 14 for the Preset Calibration Run.
Set Up	Preset Number 15	P15	0.0, 1.0	Enable or disable Preset Number 15 for the Preset Calibration Run. Enable or disable Preset Number 15 for the Preset Calibration Run.
Set Up	Preset Number 2	P2	0.0, 1.0	Enable or disable Preset Number 2 for the Preset Calibration Run. Enable or disable Preset Number 2 for the Preset Calibration Run.
Set Up	Preset Number 3	P3	0.0, 1.0	Enable or disable Preset Number 3 for the Preset Calibration Run. Enable or disable Preset Number 3 for the Preset Calibration Run.
Set Up	Preset Number 4	P4	0.0, 1.0	Enable or disable Preset Number 4 for the Preset Calibration Run. Enable or disable Preset Number 4 for the Preset Calibration Run.
Set Up	Preset Number 5	P5	0.0, 1.0	Enable or disable Preset Number 5 for the Preset Calibration Run. Enable or disable Preset Number 5 for the Preset Calibration Run.
Set Up	Preset Number 6	P6	0.0, 1.0	Enable or disable Preset Number 6 for the Preset Calibration Run. Enable or disable Preset Number 6 for the Preset Calibration Run.
Set Up	Preset Number 7	P7	0.0, 1.0	Enable or disable Preset Number 7 for the Preset Calibration Run. Enable or disable Preset Number 7 for the Preset Calibration Run.
Set Up	Preset Number 8	P8	0.0, 1.0	Enable or disable Preset Number 8 for the Preset Calibration Run. Enable or disable Preset Number 8 for the Preset Calibration Run.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Preset Number 9	P9	0.0, 1.0	Enable or disable Preset Number 9 for the Preset Calibration Run. Enable or disable Preset Number 9 for the Preset Calibration Run.
Set Up	Provider Power Profile 1	ProviderPowerProfile1	0.0, 1.0	Enable or disable Provider Power Profile 1 support. Enable or disable Provider Power Profile 1 support.
Set Up	Provider Power Profile 2	ProviderPowerProfile2	0.0, 1.0	Enable or disable Provider Power Profile 2 support. Enable or disable Provider Power Profile 2 support.
Set Up	Provider Power Profile 3	ProviderPowerProfile3	0.0, 1.0	Enable or disable Provider Power Profile 3 support. Enable or disable Provider Power Profile 3 support.
Set Up	Retimer	Retimer	0.0, 1.0	This is a retimer if set to true. This is a retimer if set to true
Set Up	SQ2_NegSignalDirectory	SQ2_Neg_wfm	(Accepts user-defined text)	This variable use to store the directory of SQ2 negative signal waveform. This variable use to store the directory of SQ2 negative signal waveform.
Set Up	SQ2_PosSignalDirectory	SQ2_Pos_wfm	(Accepts user-defined text)	This variable use to store the directory of SQ2 positive signal waveform. This variable use to store the directory of SQ2 positive signal waveform.
Set Up	SQ_NegSignalDirectory	SQ_Neg_wfm	(Accepts user-defined text)	This variable use to store the directory of SQ16/SQ32 negative signal waveform. This variable use to store the directory of SQ16/SQ32 negative signal waveform.
Set Up	SQ_PosSignalDirectory	SQ_Pos_wfm	(Accepts user-defined text)	This variable use to store the directory of SQ16/SQ32 positive signal waveform. This variable use to store the directory of SQ16/SQ32 positive signal waveform.
Set Up	SigTest Directory	SigTestDirectory	(Accepts user-defined text)	SigTest Directory SigTest Directory

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	SigTest Executable name	SigTestExeName	(Accepts user-defined text)	SigTest Executable name SigTest Executable name
Set Up	SigTest Timeout in ms	SigTestTimeout	(Accepts user-defined text)	SigTest Timeout in ms SigTest Timeout in ms
Set Up	SigTest Version	SigTestVersion	(Accepts user-defined text), 0.82	SigTest Version SigTest Version
Set Up	Specification Version	SpecVersion	USB4 Specification Ver 2.00	Select the test specification for testing. Select the test specification for testing.
Set Up	Test Lane Port 1	TestLanePort1	Both lanes, Lane 0 only, Lane 1 only	Select the test lane of Port 1 for testing. Select the test lane of Port 1 for testing.
Set Up	Test Lane Port 2	TestLanePort2	Both lanes, Lane 0 only, Lane 1 only	Select the test lane of Port 2 for testing. Select the test lane of Port 2 for testing.
Set Up	Test Setup Complete	TestSetupComplete	0.0, 1.0	Determine whether the test setup is completed. Determine whether the test setup is completed.
Set Up	User Comment	UserComments	(Accepts user-defined text)	Additional comments for the DUT in testing. Additional comments for the DUT in testing.
Set Up	User Description	UserDescription	(Accepts user-defined text)	Short description for the DUT in testing. Short description for the DUT in testing.

3 Test Names and IDs

The following table shows the mapping between each test's numeric ID and name. The numeric ID is required by various remote interface methods.

- Name – The name of the test as it appears on the user interface **Select Tests** tab.
- Test ID – The number to use with the RunTests method.
- Description – The description of the test as it appears on the user interface **Select Tests** tab.

For example, if the graphical user interface displays this tree in the **Select Tests** tab:

- All Tests
  - Rise Time
  - Fall Time

then you would expect to see something like this in the table below:

Table 3 Example Test Names and IDs

Name	Test ID	Description
Fall Time	110	Measures clock fall time.
Rise Time	100	Measures clock rise time.

and you would run these tests remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SelectedTests '100,110'"
arsl -a ipaddress -c "Run"

C# syntax
---------
remoteAte.SelectedTests = new int[]{100,110};
remoteAte.Run();
```

Here are the actual Test names and IDs used by this application. Listed at the end, you may also find:

- Deprecated IDs and their replacements.
- Macro IDs which may be used to select multiple related tests at the same time.

NOTE The file, "TestInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 4 Test IDs and Names

Name	TestID	Description
3.3.1 Tx Equalization Deemphasis (10 Gb/s) (Port 1, Lane 0)	21610	The equalization level at TP2 of a USB4 device must be within the specification.
3.3.1 Tx Equalization Deemphasis (10 Gb/s) (Port 1, Lane 0)	11610	The equalization level at TP2 of a USB4 host must be within the specification.
3.3.1 Tx Equalization Deemphasis (10 Gb/s) (Port 1, Lane 1)	21620	The equalization level at TP2 of a USB4 device must be within the specification.
3.3.1 Tx Equalization Deemphasis (10 Gb/s) (Port 1, Lane 1)	11620	The equalization level at TP2 of a USB4 host must be within the specification.
3.3.1 Tx Equalization Deemphasis (10 Gb/s) (Port 2, Lane 0)	21630	The equalization level at TP2 of a USB4 device must be within the specification.
3.3.1 Tx Equalization Deemphasis (10 Gb/s) (Port 2, Lane 0)	11630	The equalization level at TP2 of a USB4 host must be within the specification.
3.3.1 Tx Equalization Deemphasis (10 Gb/s) (Port 2, Lane 1)	21640	The equalization level at TP2 of a USB4 device must be within the specification.
3.3.1 Tx Equalization Deemphasis (10 Gb/s) (Port 2, Lane 1)	11640	The equalization level at TP2 of a USB4 host must be within the specification.
3.3.1 Tx Equalization Deemphasis (10.3125 Gb/s) (Port 1, Lane 0)	2610	The equalization level at TP2 of a USB4 device must be within the specification.
3.3.1 Tx Equalization Deemphasis (10.3125 Gb/s) (Port 1, Lane 0)	1610	The equalization level at TP2 of a USB4 host must be within the specification.
3.3.1 Tx Equalization Deemphasis (10.3125 Gb/s) (Port 1, Lane 1)	2620	The equalization level at TP2 of a USB4 device must be within the specification.
3.3.1 Tx Equalization Deemphasis (10.3125 Gb/s) (Port 1, Lane 1)	1620	The equalization level at TP2 of a USB4 host must be within the specification.
3.3.1 Tx Equalization Deemphasis (10.3125 Gb/s) (Port 2, Lane 0)	2630	The equalization level at TP2 of a USB4 device must be within the specification.
3.3.1 Tx Equalization Deemphasis (10.3125 Gb/s) (Port 2, Lane 0)	1630	The equalization level at TP2 of a USB4 host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.1 Tx Equalization Deemphasis (10.3125 Gb/s) (Port 2, Lane 1)	2640	The equalization level at TP2 of a USB4 device must be within the specification.
3.3.1 Tx Equalization Deemphasis (10.3125 Gb/s) (Port 2, Lane 1)	1640	The equalization level at TP2 of a USB4 host must be within the specification.
3.3.1 Tx Equalization Preshoot (10 Gb/s) (Port 1, Lane 0)	21510	The equalization level at TP2 of a USB4 device must be within the specification.
3.3.1 Tx Equalization Preshoot (10 Gb/s) (Port 1, Lane 0)	11510	The equalization level at TP2 of a USB4 host must be within the specification.
3.3.1 Tx Equalization Preshoot (10 Gb/s) (Port 1, Lane 1)	21520	The equalization level at TP2 of a USB4 device must be within the specification.
3.3.1 Tx Equalization Preshoot (10 Gb/s) (Port 1, Lane 1)	11520	The equalization level at TP2 of a USB4 host must be within the specification.
3.3.1 Tx Equalization Preshoot (10 Gb/s) (Port 2, Lane 0)	21530	The equalization level at TP2 of a USB4 device must be within the specification.
3.3.1 Tx Equalization Preshoot (10 Gb/s) (Port 2, Lane 0)	11530	The equalization level at TP2 of a USB4 host must be within the specification.
3.3.1 Tx Equalization Preshoot (10 Gb/s) (Port 2, Lane 1)	21540	The equalization level at TP2 of a USB4 device must be within the specification.
3.3.1 Tx Equalization Preshoot (10 Gb/s) (Port 2, Lane 1)	11540	The equalization level at TP2 of a USB4 host must be within the specification.
3.3.1 Tx Equalization Preshoot (10.3125 Gb/s) (Port 1, Lane 0)	2510	The equalization level at TP2 of a USB4 device must be within the specification.
3.3.1 Tx Equalization Preshoot (10.3125 Gb/s) (Port 1, Lane 0)	1510	The equalization level at TP2 of a USB4 host must be within the specification.
3.3.1 Tx Equalization Preshoot (10.3125 Gb/s) (Port 1, Lane 1)	2520	The equalization level at TP2 of a USB4 device must be within the specification.
3.3.1 Tx Equalization Preshoot (10.3125 Gb/s) (Port 1, Lane 1)	1520	The equalization level at TP2 of a USB4 host must be within the specification.
3.3.1 Tx Equalization Preshoot (10.3125 Gb/s) (Port 2, Lane 0)	2530	The equalization level at TP2 of a USB4 device must be within the specification.
3.3.1 Tx Equalization Preshoot (10.3125 Gb/s) (Port 2, Lane 0)	1530	The equalization level at TP2 of a USB4 host must be within the specification.
3.3.1 Tx Equalization Preshoot (10.3125 Gb/s) (Port 2, Lane 1)	2540	The equalization level at TP2 of a USB4 device must be within the specification.
3.3.1 Tx Equalization Preshoot (10.3125 Gb/s) (Port 2, Lane 1)	1540	The equalization level at TP2 of a USB4 host must be within the specification.
3.3.1 Tx Swing Preset 15 (10 Gb/s) (Port 1, Lane 0)	21710	The transmitter swing of Preset 15 of a USB4 Device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.1 Tx Swing Preset 15 (10 Gb/s) (Port 1, Lane 0)	11710	The transmitter swing of Preset 15 of a USB4 host must be within the specification.
3.3.1 Tx Swing Preset 15 (10 Gb/s) (Port 1, Lane 1)	21720	The transmitter swing of Preset 15 of a USB4 Device must be within the specification.
3.3.1 Tx Swing Preset 15 (10 Gb/s) (Port 1, Lane 1)	11720	The transmitter swing of Preset 15 of a USB4 host must be within the specification.
3.3.1 Tx Swing Preset 15 (10 Gb/s) (Port 2, Lane 0)	21730	The transmitter swing of Preset 15 of a USB4 Device must be within the specification.
3.3.1 Tx Swing Preset 15 (10 Gb/s) (Port 2, Lane 0)	11730	The transmitter swing of Preset 15 of a USB4 host must be within the specification.
3.3.1 Tx Swing Preset 15 (10 Gb/s) (Port 2, Lane 1)	21740	The transmitter swing of Preset 15 of a USB4 Device must be within the specification.
3.3.1 Tx Swing Preset 15 (10 Gb/s) (Port 2, Lane 1)	11740	The transmitter swing of Preset 15 of a USB4 host must be within the specification.
3.3.1 Tx Swing Preset 15 (10.3125 Gb/s) (Port 1, Lane 0)	2710	The transmitter swing of Preset 15 of a USB4 Device must be within the specification.
3.3.1 Tx Swing Preset 15 (10.3125 Gb/s) (Port 1, Lane 0)	1710	The transmitter swing of Preset 15 of a USB4 host must be within the specification.
3.3.1 Tx Swing Preset 15 (10.3125 Gb/s) (Port 1, Lane 1)	2720	The transmitter swing of Preset 15 of a USB4 Device must be within the specification.
3.3.1 Tx Swing Preset 15 (10.3125 Gb/s) (Port 1, Lane 1)	1720	The transmitter swing of Preset 15 of a USB4 host must be within the specification.
3.3.1 Tx Swing Preset 15 (10.3125 Gb/s) (Port 2, Lane 0)	2730	The transmitter swing of Preset 15 of a USB4 Device must be within the specification.
3.3.1 Tx Swing Preset 15 (10.3125 Gb/s) (Port 2, Lane 0)	1730	The transmitter swing of Preset 15 of a USB4 host must be within the specification.
3.3.1 Tx Swing Preset 15 (10.3125 Gb/s) (Port 2, Lane 1)	2740	The transmitter swing of Preset 15 of a USB4 Device must be within the specification.
3.3.1 Tx Swing Preset 15 (10.3125 Gb/s) (Port 2, Lane 1)	1740	The transmitter swing of Preset 15 of a USB4 host must be within the specification.
3.3.10 Tx Total Jitter (10 Gb/s) (Port 1, Lane 0)	21671	The total jitter (TJ) of a USB4 device must be less than maximum limit.
3.3.10 Tx Total Jitter (10 Gb/s) (Port 1, Lane 0)	11671	The total jitter (TJ) of a USB4 host must be less than maximum limit.
3.3.10 Tx Total Jitter (10 Gb/s) (Port 1, Lane 1)	21672	The total jitter (TJ) of a USB4 device must be less than maximum limit.
3.3.10 Tx Total Jitter (10 Gb/s) (Port 1, Lane 1)	11672	The total jitter (TJ) of a USB4 host must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.10 Tx Total Jitter (10 Gb/s) (Port 2, Lane 0)	21673	The total jitter (TJ) of a USB4 device must be less than maximum limit.
3.3.10 Tx Total Jitter (10 Gb/s) (Port 2, Lane 0)	11673	The total jitter (TJ) of a USB4 host must be less than maximum limit.
3.3.10 Tx Total Jitter (10 Gb/s) (Port 2, Lane 1)	21674	The total jitter (TJ) of a USB4 device must be less than maximum limit.
3.3.10 Tx Total Jitter (10 Gb/s) (Port 2, Lane 1)	11674	The total jitter (TJ) of a USB4 host must be less than maximum limit.
3.3.10 Tx Total Jitter (10.3125 Gb/s) (Port 1, Lane 0)	2671	The total jitter (TJ) of a USB4 device must be less than maximum limit.
3.3.10 Tx Total Jitter (10.3125 Gb/s) (Port 1, Lane 0)	1671	The total jitter (TJ) of a USB4 host must be less than maximum limit.
3.3.10 Tx Total Jitter (10.3125 Gb/s) (Port 1, Lane 1)	2672	The total jitter (TJ) of a USB4 device must be less than maximum limit.
3.3.10 Tx Total Jitter (10.3125 Gb/s) (Port 1, Lane 1)	1672	The total jitter (TJ) of a USB4 host must be less than maximum limit.
3.3.10 Tx Total Jitter (10.3125 Gb/s) (Port 2, Lane 0)	2673	The total jitter (TJ) of a USB4 device must be less than maximum limit.
3.3.10 Tx Total Jitter (10.3125 Gb/s) (Port 2, Lane 0)	1673	The total jitter (TJ) of a USB4 host must be less than maximum limit.
3.3.10 Tx Total Jitter (10.3125 Gb/s) (Port 2, Lane 1)	2674	The total jitter (TJ) of a USB4 device must be less than maximum limit.
3.3.10 Tx Total Jitter (10.3125 Gb/s) (Port 2, Lane 1)	1674	The total jitter (TJ) of a USB4 host must be less than maximum limit.
3.3.11 Tx Uncorrelated Jitter (10 Gb/s) (Port 1, Lane 0)	21871	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 device must be less than maximum limit.
3.3.11 Tx Uncorrelated Jitter (10 Gb/s) (Port 1, Lane 0)	11871	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 host must be less than maximum limit.
3.3.11 Tx Uncorrelated Jitter (10 Gb/s) (Port 1, Lane 1)	21872	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 device must be less than maximum limit.
3.3.11 Tx Uncorrelated Jitter (10 Gb/s) (Port 1, Lane 1)	11872	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 host must be less than maximum limit.
3.3.11 Tx Uncorrelated Jitter (10 Gb/s) (Port 2, Lane 0)	21873	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 device must be less than maximum limit.
3.3.11 Tx Uncorrelated Jitter (10 Gb/s) (Port 2, Lane 0)	11873	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 host must be less than maximum limit.
3.3.11 Tx Uncorrelated Jitter (10 Gb/s) (Port 2, Lane 1)	21874	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.11 Tx Uncorrelated Jitter (10 Gb/s) (Port 2, Lane 1)	11874	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 host must be less than maximum limit.
3.3.11 Tx Uncorrelated Jitter (10.3125 Gb/s) (Port 1, Lane 0)	2871	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 device must be less than maximum limit.
3.3.11 Tx Uncorrelated Jitter (10.3125 Gb/s) (Port 1, Lane 0)	1871	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 host must be less than maximum limit.
3.3.11 Tx Uncorrelated Jitter (10.3125 Gb/s) (Port 1, Lane 1)	2872	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 device must be less than maximum limit.
3.3.11 Tx Uncorrelated Jitter (10.3125 Gb/s) (Port 1, Lane 1)	1872	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 host must be less than maximum limit.
3.3.11 Tx Uncorrelated Jitter (10.3125 Gb/s) (Port 2, Lane 0)	2873	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 device must be less than maximum limit.
3.3.11 Tx Uncorrelated Jitter (10.3125 Gb/s) (Port 2, Lane 0)	1873	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 host must be less than maximum limit.
3.3.11 Tx Uncorrelated Jitter (10.3125 Gb/s) (Port 2, Lane 1)	2874	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 device must be less than maximum limit.
3.3.11 Tx Uncorrelated Jitter (10.3125 Gb/s) (Port 2, Lane 1)	1874	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 host must be less than maximum limit.
3.3.12 Tx Uncorrelated Deterministic Jitter (10 Gb/s) (Port 1, Lane 0)	21971	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 device must be less than the maximum limit.
3.3.12 Tx Uncorrelated Deterministic Jitter (10 Gb/s) (Port 1, Lane 0)	11971	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 host must be less than the maximum limit.
3.3.12 Tx Uncorrelated Deterministic Jitter (10 Gb/s) (Port 1, Lane 1)	21972	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 device must be less than the maximum limit.
3.3.12 Tx Uncorrelated Deterministic Jitter (10 Gb/s) (Port 1, Lane 1)	11972	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 host must be less than the maximum limit.
3.3.12 Tx Uncorrelated Deterministic Jitter (10 Gb/s) (Port 2, Lane 0)	21973	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 device must be less than the maximum limit.
3.3.12 Tx Uncorrelated Deterministic Jitter (10 Gb/s) (Port 2, Lane 0)	11973	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 host must be less than the maximum limit.
3.3.12 Tx Uncorrelated Deterministic Jitter (10 Gb/s) (Port 2, Lane 1)	21974	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 device must be less than the maximum limit.
3.3.12 Tx Uncorrelated Deterministic Jitter (10 Gb/s) (Port 2, Lane 1)	11974	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 host must be less than the maximum limit.
3.3.12 Tx Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 1, Lane 0)	2971	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 device must be less than the maximum limit.
3.3.12 Tx Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 1, Lane 0)	1971	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 host must be less than the maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.12 Tx Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 1, Lane 1)	2972	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 device must be less than the maximum limit.
3.3.12 Tx Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 1, Lane 1)	1972	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 host must be less than the maximum limit.
3.3.12 Tx Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 2, Lane 0)	2973	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 device must be less than the maximum limit.
3.3.12 Tx Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 2, Lane 0)	1973	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 host must be less than the maximum limit.
3.3.12 Tx Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 2, Lane 1)	2974	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 device must be less than the maximum limit.
3.3.12 Tx Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 2, Lane 1)	1974	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 host must be less than the maximum limit.
3.3.13 Tx Data Dependent Jitter (10 Gb/s) (Port 1, Lane 0)	41871	The sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit.
3.3.13 Tx Data Dependent Jitter (10 Gb/s) (Port 1, Lane 0)	31871	The sum of Data Dependent Jitter (DDJ) of a USB4 host must be less than the maximum limit.
3.3.13 Tx Data Dependent Jitter (10 Gb/s) (Port 1, Lane 1)	41872	The sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit.
3.3.13 Tx Data Dependent Jitter (10 Gb/s) (Port 1, Lane 1)	31872	The sum of Data Dependent Jitter (DDJ) of a USB4 host must be less than the maximum limit.
3.3.13 Tx Data Dependent Jitter (10 Gb/s) (Port 2, Lane 0)	41873	The sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit.
3.3.13 Tx Data Dependent Jitter (10 Gb/s) (Port 2, Lane 0)	31873	The sum of Data Dependent Jitter (DDJ) of a USB4 host must be less than the maximum limit.
3.3.13 Tx Data Dependent Jitter (10 Gb/s) (Port 2, Lane 1)	41874	The sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit.
3.3.13 Tx Data Dependent Jitter (10 Gb/s) (Port 2, Lane 1)	31874	The sum of Data Dependent Jitter (DDJ) of a USB4 host must be less than the maximum limit.
3.3.13 Tx Data Dependent Jitter (10.3125 Gb/s) (Port 1, Lane 0)	4871	The sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit.
3.3.13 Tx Data Dependent Jitter (10.3125 Gb/s) (Port 1, Lane 0)	3871	The sum of Data Dependent Jitter (DDJ) of a USB4 host must be less than the maximum limit.
3.3.13 Tx Data Dependent Jitter (10.3125 Gb/s) (Port 1, Lane 1)	4872	The sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit.
3.3.13 Tx Data Dependent Jitter (10.3125 Gb/s) (Port 1, Lane 1)	3872	The sum of Data Dependent Jitter (DDJ) of a USB4 host must be less than the maximum limit.
3.3.13 Tx Data Dependent Jitter (10.3125 Gb/s) (Port 2, Lane 0)	4873	The sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.13 Tx Data Dependent Jitter (10.3125 Gb/s) (Port 2, Lane 0)	3873	The sum of Data Dependent Jitter (DDJ) of a USB4 host must be less than the maximum limit.
3.3.13 Tx Data Dependent Jitter (10.3125 Gb/s) (Port 2, Lane 1)	4874	The sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit.
3.3.13 Tx Data Dependent Jitter (10.3125 Gb/s) (Port 2, Lane 1)	3874	The sum of Data Dependent Jitter (DDJ) of a USB4 host must be less than the maximum limit.
3.3.14 Tx Low Frequency Uncorrelated Deterministic Jitter (10 Gb/s) (Port 1, Lane 0)	21981	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 device must be less than the maximum limit.
3.3.14 Tx Low Frequency Uncorrelated Deterministic Jitter (10 Gb/s) (Port 1, Lane 0)	11981	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 host must be less than the maximum limit.
3.3.14 Tx Low Frequency Uncorrelated Deterministic Jitter (10 Gb/s) (Port 1, Lane 1)	21982	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 device must be less than the maximum limit.
3.3.14 Tx Low Frequency Uncorrelated Deterministic Jitter (10 Gb/s) (Port 1, Lane 1)	11982	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 host must be less than the maximum limit.
3.3.14 Tx Low Frequency Uncorrelated Deterministic Jitter (10 Gb/s) (Port 2, Lane 0)	21983	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 device must be less than the maximum limit.
3.3.14 Tx Low Frequency Uncorrelated Deterministic Jitter (10 Gb/s) (Port 2, Lane 0)	11983	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 host must be less than the maximum limit.
3.3.14 Tx Low Frequency Uncorrelated Deterministic Jitter (10 Gb/s) (Port 2, Lane 1)	21984	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 device must be less than the maximum limit.
3.3.14 Tx Low Frequency Uncorrelated Deterministic Jitter (10 Gb/s) (Port 2, Lane 1)	11984	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 host must be less than the maximum limit.
3.3.14 Tx Low Frequency Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 1, Lane 0)	2981	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 device must be less than the maximum limit.
3.3.14 Tx Low Frequency Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 1, Lane 0)	1981	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 host must be less than the maximum limit.
3.3.14 Tx Low Frequency Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 1, Lane 1)	2982	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 device must be less than the maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.14 Tx Low Frequency Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 1, Lane 1)	1982	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 host must be less than the maximum limit.
3.3.14 Tx Low Frequency Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 2, Lane 0)	2983	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 device must be less than the maximum limit.
3.3.14 Tx Low Frequency Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 2, Lane 0)	1983	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 host must be less than the maximum limit.
3.3.14 Tx Low Frequency Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 2, Lane 1)	2984	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 device must be less than the maximum limit.
3.3.14 Tx Low Frequency Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 2, Lane 1)	1984	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 host must be less than the maximum limit.
3.3.15 Tx Duty Cycle Distortion (10 Gb/s) (Port 1, Lane 0)	21961	The sum of Duty Cycle Distortion (DCD) of a USB4 device must be less than the maximum limit.
3.3.15 Tx Duty Cycle Distortion (10 Gb/s) (Port 1, Lane 0)	11961	The sum of Duty Cycle Distortion (DCD) of a USB4 host must be less than the maximum limit.
3.3.15 Tx Duty Cycle Distortion (10 Gb/s) (Port 1, Lane 1)	21962	The sum of Duty Cycle Distortion (DCD) of a USB4 device must be less than the maximum limit.
3.3.15 Tx Duty Cycle Distortion (10 Gb/s) (Port 1, Lane 1)	11962	The sum of Duty Cycle Distortion (DCD) of a USB4 host must be less than the maximum limit.
3.3.15 Tx Duty Cycle Distortion (10 Gb/s) (Port 2, Lane 0)	21963	The sum of Duty Cycle Distortion (DCD) of a USB4 device must be less than the maximum limit.
3.3.15 Tx Duty Cycle Distortion (10 Gb/s) (Port 2, Lane 0)	11963	The sum of Duty Cycle Distortion (DCD) of a USB4 host must be less than the maximum limit.
3.3.15 Tx Duty Cycle Distortion (10 Gb/s) (Port 2, Lane 1)	21964	The sum of Duty Cycle Distortion (DCD) of a USB4 device must be less than the maximum limit.
3.3.15 Tx Duty Cycle Distortion (10 Gb/s) (Port 2, Lane 1)	11964	The sum of Duty Cycle Distortion (DCD) of a USB4 host must be less than the maximum limit.
3.3.15 Tx Duty Cycle Distortion (10.3125 Gb/s) (Port 1, Lane 0)	2961	The sum of Duty Cycle Distortion (DCD) of a USB4 device must be less than the maximum limit.
3.3.15 Tx Duty Cycle Distortion (10.3125 Gb/s) (Port 1, Lane 0)	1961	The sum of Duty Cycle Distortion (DCD) of a USB4 host must be less than the maximum limit.
3.3.15 Tx Duty Cycle Distortion (10.3125 Gb/s) (Port 1, Lane 1)	2962	The sum of Duty Cycle Distortion (DCD) of a USB4 device must be less than the maximum limit.
3.3.15 Tx Duty Cycle Distortion (10.3125 Gb/s) (Port 1, Lane 1)	1962	The sum of Duty Cycle Distortion (DCD) of a USB4 host must be less than the maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.15 Tx Duty Cycle Distortion (10.3125 Gb/s) (Port 2, Lane 0)	2963	The sum of Duty Cycle Distortion (DCD) of a USB4 device must be less than the maximum limit.
3.3.15 Tx Duty Cycle Distortion (10.3125 Gb/s) (Port 2, Lane 0)	1963	The sum of Duty Cycle Distortion (DCD) of a USB4 host must be less than the maximum limit.
3.3.15 Tx Duty Cycle Distortion (10.3125 Gb/s) (Port 2, Lane 1)	2964	The sum of Duty Cycle Distortion (DCD) of a USB4 device must be less than the maximum limit.
3.3.15 Tx Duty Cycle Distortion (10.3125 Gb/s) (Port 2, Lane 1)	1964	The sum of Duty Cycle Distortion (DCD) of a USB4 host must be less than the maximum limit.
3.3.16 Tx AC Common Mode Voltage (10 Gb/s) (Port 1, Lane 0)	21121	The AC common mode peak-to-peak voltage at TP2 of a USB4 device must be less than maximum limit.
3.3.16 Tx AC Common Mode Voltage (10 Gb/s) (Port 1, Lane 0)	11121	The AC common mode peak-to-peak voltage at TP2 of a USB4 host must be less than maximum limit.
3.3.16 Tx AC Common Mode Voltage (10 Gb/s) (Port 1, Lane 1)	21221	The AC common mode peak-to-peak voltage at TP2 of a USB4 device must be less than maximum limit.
3.3.16 Tx AC Common Mode Voltage (10 Gb/s) (Port 1, Lane 1)	11221	The AC common mode peak-to-peak voltage at TP2 of a USB4 host must be less than maximum limit.
3.3.16 Tx AC Common Mode Voltage (10 Gb/s) (Port 2, Lane 0)	21321	The AC common mode peak-to-peak voltage at TP2 of a USB4 device must be less than maximum limit.
3.3.16 Tx AC Common Mode Voltage (10 Gb/s) (Port 2, Lane 0)	11321	The AC common mode peak-to-peak voltage at TP2 of a USB4 host must be less than maximum limit.
3.3.16 Tx AC Common Mode Voltage (10 Gb/s) (Port 2, Lane 1)	21421	The AC common mode peak-to-peak voltage at TP2 of a USB4 device must be less than maximum limit.
3.3.16 Tx AC Common Mode Voltage (10 Gb/s) (Port 2, Lane 1)	11421	The AC common mode peak-to-peak voltage at TP2 of a USB4 host must be less than maximum limit.
3.3.16 Tx AC Common Mode Voltage (10.3125 Gb/s) (Port 1, Lane 0)	2121	The AC common mode peak-to-peak voltage at TP2 of a USB4 device must be less than maximum limit.
3.3.16 Tx AC Common Mode Voltage (10.3125 Gb/s) (Port 1, Lane 0)	1121	The AC common mode peak-to-peak voltage at TP2 of a USB4 host must be less than maximum limit.
3.3.16 Tx AC Common Mode Voltage (10.3125 Gb/s) (Port 1, Lane 1)	2221	The AC common mode peak-to-peak voltage at TP2 of a USB4 device must be less than maximum limit.
3.3.16 Tx AC Common Mode Voltage (10.3125 Gb/s) (Port 1, Lane 1)	1221	The AC common mode peak-to-peak voltage at TP2 of a USB4 host must be less than maximum limit.
3.3.16 Tx AC Common Mode Voltage (10.3125 Gb/s) (Port 2, Lane 0)	2321	The AC common mode peak-to-peak voltage at TP2 of a USB4 device must be less than maximum limit.
3.3.16 Tx AC Common Mode Voltage (10.3125 Gb/s) (Port 2, Lane 0)	1321	The AC common mode peak-to-peak voltage at TP2 of a USB4 host must be less than maximum limit.
3.3.16 Tx AC Common Mode Voltage (10.3125 Gb/s) (Port 2, Lane 1)	2421	The AC common mode peak-to-peak voltage at TP2 of a USB4 device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.16 Tx AC Common Mode Voltage (10.3125 Gb/s) (Port 2, Lane 1)	1421	The AC common mode peak-to-peak voltage at TP2 of a USB4 host must be less than maximum limit.
3.3.17 Tx Eye Diagram (10 Gb/s) (Port 1, Lane 0)	21131	The eye diagram at TP2 of a USB4 device must be within the template as described in the specification.
3.3.17 Tx Eye Diagram (10 Gb/s) (Port 1, Lane 0)	11131	The eye diagram at TP2 of a USB4 host must be within the template as described in the specification.
3.3.17 Tx Eye Diagram (10 Gb/s) (Port 1, Lane 1)	21231	The eye diagram at TP2 of a USB4 device must be within the template as described in the specification.
3.3.17 Tx Eye Diagram (10 Gb/s) (Port 1, Lane 1)	11231	The eye diagram at TP2 of a USB4 host must be within the template as described in the specification.
3.3.17 Tx Eye Diagram (10 Gb/s) (Port 2, Lane 0)	21331	The eye diagram at TP2 of a USB4 device must be within the template as described in the specification.
3.3.17 Tx Eye Diagram (10 Gb/s) (Port 2, Lane 0)	11331	The eye diagram at TP2 of a USB4 host must be within the template as described in the specification.
3.3.17 Tx Eye Diagram (10 Gb/s) (Port 2, Lane 1)	21431	The eye diagram at TP2 of a USB4 device must be within the template as described in the specification.
3.3.17 Tx Eye Diagram (10 Gb/s) (Port 2, Lane 1)	11431	The eye diagram at TP2 of a USB4 host must be within the template as described in the specification.
3.3.17 Tx Eye Diagram (10.3125 Gb/s) (Port 1, Lane 0)	2131	The eye diagram at TP2 of a USB4 device must be within the template as described in the specification.
3.3.17 Tx Eye Diagram (10.3125 Gb/s) (Port 1, Lane 0)	1131	The eye diagram at TP2 of a USB4 host must be within the template as described in the specification.
3.3.17 Tx Eye Diagram (10.3125 Gb/s) (Port 1, Lane 1)	2231	The eye diagram at TP2 of a USB4 device must be within the template as described in the specification.
3.3.17 Tx Eye Diagram (10.3125 Gb/s) (Port 1, Lane 1)	1231	The eye diagram at TP2 of a USB4 host must be within the template as described in the specification.
3.3.17 Tx Eye Diagram (10.3125 Gb/s) (Port 2, Lane 0)	2331	The eye diagram at TP2 of a USB4 device must be within the template as described in the specification.
3.3.17 Tx Eye Diagram (10.3125 Gb/s) (Port 2, Lane 0)	1331	The eye diagram at TP2 of a USB4 host must be within the template as described in the specification.
3.3.17 Tx Eye Diagram (10.3125 Gb/s) (Port 2, Lane 1)	2431	The eye diagram at TP2 of a USB4 device must be within the template as described in the specification.
3.3.17 Tx Eye Diagram (10.3125 Gb/s) (Port 2, Lane 1)	1431	The eye diagram at TP2 of a USB4 host must be within the template as described in the specification.
3.3.18 Tx Total Jitter TP3 (10 Gb/s) (Port 1, Lane 0)	21661	The total jitter (TJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.18 Tx Total Jitter TP3 (10 Gb/s) (Port 1, Lane 0)	11661	The total jitter (TJ) at TP3 of a USB4 host must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.18 Tx Total Jitter TP3 (10 Gb/s) (Port 1, Lane 1)	21662	The total jitter (TJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.18 Tx Total Jitter TP3 (10 Gb/s) (Port 1, Lane 1)	11662	The total jitter (TJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.18 Tx Total Jitter TP3 (10 Gb/s) (Port 2, Lane 0)	21663	The total jitter (TJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.18 Tx Total Jitter TP3 (10 Gb/s) (Port 2, Lane 0)	11663	The total jitter (TJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.18 Tx Total Jitter TP3 (10 Gb/s) (Port 2, Lane 1)	21664	The total jitter (TJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.18 Tx Total Jitter TP3 (10 Gb/s) (Port 2, Lane 1)	11664	The total jitter (TJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.18 Tx Total Jitter TP3 (10.3125 Gb/s) (Port 1, Lane 0)	2661	The total jitter (TJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.18 Tx Total Jitter TP3 (10.3125 Gb/s) (Port 1, Lane 0)	1661	The total jitter (TJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.18 Tx Total Jitter TP3 (10.3125 Gb/s) (Port 1, Lane 1)	2662	The total jitter (TJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.18 Tx Total Jitter TP3 (10.3125 Gb/s) (Port 1, Lane 1)	1662	The total jitter (TJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.18 Tx Total Jitter TP3 (10.3125 Gb/s) (Port 2, Lane 0)	2663	The total jitter (TJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.18 Tx Total Jitter TP3 (10.3125 Gb/s) (Port 2, Lane 0)	1663	The total jitter (TJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.18 Tx Total Jitter TP3 (10.3125 Gb/s) (Port 2, Lane 1)	2664	The total jitter (TJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.18 Tx Total Jitter TP3 (10.3125 Gb/s) (Port 2, Lane 1)	1664	The total jitter (TJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.19 Tx Uncorrelated Jitter TP3 (10 Gb/s) (Port 1, Lane 0)	21771	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.19 Tx Uncorrelated Jitter TP3 (10 Gb/s) (Port 1, Lane 0)	11771	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.19 Tx Uncorrelated Jitter TP3 (10 Gb/s) (Port 1, Lane 1)	21772	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.19 Tx Uncorrelated Jitter TP3 (10 Gb/s) (Port 1, Lane 1)	11772	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.19 Tx Uncorrelated Jitter TP3 (10 Gb/s) (Port 2, Lane 0)	21773	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.19 Tx Uncorrelated Jitter TP3 (10 Gb/s) (Port 2, Lane 0)	11773	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.19 Tx Uncorrelated Jitter TP3 (10 Gb/s) (Port 2, Lane 1)	21774	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.19 Tx Uncorrelated Jitter TP3 (10 Gb/s) (Port 2, Lane 1)	11774	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.19 Tx Uncorrelated Jitter TP3 (10.3125 Gb/s) (Port 1, Lane 0)	2771	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.19 Tx Uncorrelated Jitter TP3 (10.3125 Gb/s) (Port 1, Lane 0)	1771	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.19 Tx Uncorrelated Jitter TP3 (10.3125 Gb/s) (Port 1, Lane 1)	2772	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.19 Tx Uncorrelated Jitter TP3 (10.3125 Gb/s) (Port 1, Lane 1)	1772	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.19 Tx Uncorrelated Jitter TP3 (10.3125 Gb/s) (Port 2, Lane 0)	2773	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.19 Tx Uncorrelated Jitter TP3 (10.3125 Gb/s) (Port 2, Lane 0)	1773	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.19 Tx Uncorrelated Jitter TP3 (10.3125 Gb/s) (Port 2, Lane 1)	2774	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.19 Tx Uncorrelated Jitter TP3 (10.3125 Gb/s) (Port 2, Lane 1)	1774	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.2 Tx Minimum Unit Interval, Max (10 Gb/s) (Port 1, Lane 0)	21152	The minimum unit interval at TP2 of a USB4 device must be within the specification.
3.3.2 Tx Minimum Unit Interval, Max (10 Gb/s) (Port 1, Lane 0)	11152	The minimum unit interval at TP2 of a USB4 host must be within the specification.
3.3.2 Tx Minimum Unit Interval, Max (10 Gb/s) (Port 1, Lane 1)	21252	The minimum unit interval at TP2 of a USB4 device must be within the specification.
3.3.2 Tx Minimum Unit Interval, Max (10 Gb/s) (Port 1, Lane 1)	11252	The minimum unit interval at TP2 of a USB4 host must be within the specification.
3.3.2 Tx Minimum Unit Interval, Max (10 Gb/s) (Port 2, Lane 0)	21352	The minimum unit interval at TP2 of a USB4 device must be within the specification.
3.3.2 Tx Minimum Unit Interval, Max (10 Gb/s) (Port 2, Lane 0)	11352	The minimum unit interval at TP2 of a USB4 host must be within the specification.
3.3.2 Tx Minimum Unit Interval, Max (10 Gb/s) (Port 2, Lane 1)	21452	The minimum unit interval at TP2 of a USB4 device must be within the specification.
3.3.2 Tx Minimum Unit Interval, Max (10 Gb/s) (Port 2, Lane 1)	11452	The minimum unit interval at TP2 of a USB4 host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.2 Tx Minimum Unit Interval, Min (10 Gb/s) (Port 1, Lane 0)	21151	The minimum unit interval at TP2 of a USB4 device must be within the specification.
3.3.2 Tx Minimum Unit Interval, Min (10 Gb/s) (Port 1, Lane 0)	11151	The minimum unit interval at TP2 of a USB4 host must be within the specification.
3.3.2 Tx Minimum Unit Interval, Min (10 Gb/s) (Port 1, Lane 1)	21251	The minimum unit interval at TP2 of a USB4 device must be within the specification.
3.3.2 Tx Minimum Unit Interval, Min (10 Gb/s) (Port 1, Lane 1)	11251	The minimum unit interval at TP2 of a USB4 host must be within the specification.
3.3.2 Tx Minimum Unit Interval, Min (10 Gb/s) (Port 2, Lane 0)	21351	The minimum unit interval at TP2 of a USB4 device must be within the specification.
3.3.2 Tx Minimum Unit Interval, Min (10 Gb/s) (Port 2, Lane 0)	11351	The minimum unit interval at TP2 of a USB4 host must be within the specification.
3.3.2 Tx Minimum Unit Interval, Min (10 Gb/s) (Port 2, Lane 1)	21451	The minimum unit interval at TP2 of a USB4 device must be within the specification.
3.3.2 Tx Minimum Unit Interval, Min (10 Gb/s) (Port 2, Lane 1)	11451	The minimum unit interval at TP2 of a USB4 host must be within the specification.
3.3.20 Tx Uncorrelated Deterministic Jitter TP3 (10 Gb/s) (Port 1, Lane 0)	21881	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.20 Tx Uncorrelated Deterministic Jitter TP3 (10 Gb/s) (Port 1, Lane 0)	11881	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.20 Tx Uncorrelated Deterministic Jitter TP3 (10 Gb/s) (Port 1, Lane 1)	21882	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.20 Tx Uncorrelated Deterministic Jitter TP3 (10 Gb/s) (Port 1, Lane 1)	11882	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.20 Tx Uncorrelated Deterministic Jitter TP3 (10 Gb/s) (Port 2, Lane 0)	21883	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.20 Tx Uncorrelated Deterministic Jitter TP3 (10 Gb/s) (Port 2, Lane 0)	11883	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.20 Tx Uncorrelated Deterministic Jitter TP3 (10 Gb/s) (Port 2, Lane 1)	21884	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.20 Tx Uncorrelated Deterministic Jitter TP3 (10 Gb/s) (Port 2, Lane 1)	11884	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.20 Tx Uncorrelated Deterministic Jitter TP3 (10.3125 Gb/s) (Port 1, Lane 0)	2881	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.20 Tx Uncorrelated Deterministic Jitter TP3 (10.3125 Gb/s) (Port 1, Lane 0)	1881	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 host must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.20 Tx Uncorrelated Deterministic Jitter TP3 (10.3125 Gb/s) (Port 1, Lane 1)	2882	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.20 Tx Uncorrelated Deterministic Jitter TP3 (10.3125 Gb/s) (Port 1, Lane 1)	1882	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.20 Tx Uncorrelated Deterministic Jitter TP3 (10.3125 Gb/s) (Port 2, Lane 0)	2883	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.20 Tx Uncorrelated Deterministic Jitter TP3 (10.3125 Gb/s) (Port 2, Lane 0)	1883	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.20 Tx Uncorrelated Deterministic Jitter TP3 (10.3125 Gb/s) (Port 2, Lane 1)	2884	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 device must be less than maximum limit.
3.3.20 Tx Uncorrelated Deterministic Jitter TP3 (10.3125 Gb/s) (Port 2, Lane 1)	1884	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 host must be less than maximum limit.
3.3.21 Tx Eye Diagram TP3 (10 Gb/s) (Port 1, Lane 0)	21991	The eye diagram at TP3 of a USB4 device must be within the template as described in the specification.
3.3.21 Tx Eye Diagram TP3 (10 Gb/s) (Port 1, Lane 0)	11991	The eye diagram at TP3 of a USB4 host must be within the template as described in the specification.
3.3.21 Tx Eye Diagram TP3 (10 Gb/s) (Port 1, Lane 1)	21992	The eye diagram at TP3 of a USB4 device must be within the template as described in the specification.
3.3.21 Tx Eye Diagram TP3 (10 Gb/s) (Port 1, Lane 1)	11992	The eye diagram at TP3 of a USB4 host must be within the template as described in the specification.
3.3.21 Tx Eye Diagram TP3 (10 Gb/s) (Port 2, Lane 0)	21993	The eye diagram at TP3 of a USB4 device must be within the template as described in the specification.
3.3.21 Tx Eye Diagram TP3 (10 Gb/s) (Port 2, Lane 0)	11993	The eye diagram at TP3 of a USB4 host must be within the template as described in the specification.
3.3.21 Tx Eye Diagram TP3 (10 Gb/s) (Port 2, Lane 1)	21994	The eye diagram at TP3 of a USB4 device must be within the template as described in the specification.
3.3.21 Tx Eye Diagram TP3 (10 Gb/s) (Port 2, Lane 1)	11994	The eye diagram at TP3 of a USB4 host must be within the template as described in the specification.
3.3.21 Tx Eye Diagram TP3 (10.3125 Gb/s) (Port 1, Lane 0)	2991	The eye diagram at TP3 of a USB4 device must be within the template as described in the specification.
3.3.21 Tx Eye Diagram TP3 (10.3125 Gb/s) (Port 1, Lane 0)	1991	The eye diagram at TP3 of a USB4 host must be within the template as described in the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.21 Tx Eye Diagram TP3 (10.3125 Gb/s) (Port 1, Lane 1)	2992	The eye diagram at TP3 of a USB4 device must be within the template as described in the specification.
3.3.21 Tx Eye Diagram TP3 (10.3125 Gb/s) (Port 1, Lane 1)	1992	The eye diagram at TP3 of a USB4 host must be within the template as described in the specification.
3.3.21 Tx Eye Diagram TP3 (10.3125 Gb/s) (Port 2, Lane 0)	2993	The eye diagram at TP3 of a USB4 device must be within the template as described in the specification.
3.3.21 Tx Eye Diagram TP3 (10.3125 Gb/s) (Port 2, Lane 0)	1993	The eye diagram at TP3 of a USB4 host must be within the template as described in the specification.
3.3.21 Tx Eye Diagram TP3 (10.3125 Gb/s) (Port 2, Lane 1)	2994	The eye diagram at TP3 of a USB4 device must be within the template as described in the specification.
3.3.21 Tx Eye Diagram TP3 (10.3125 Gb/s) (Port 2, Lane 1)	1994	The eye diagram at TP3 of a USB4 host must be within the template as described in the specification.
3.3.3 Tx SSC Down Spread Range, Max (10 Gb/s) (Port 1, Lane 0)	21168	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.3.3 Tx SSC Down Spread Range, Max (10 Gb/s) (Port 1, Lane 0)	11168	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.3.3 Tx SSC Down Spread Range, Max (10 Gb/s) (Port 1, Lane 1)	21268	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.3.3 Tx SSC Down Spread Range, Max (10 Gb/s) (Port 1, Lane 1)	11268	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.3.3 Tx SSC Down Spread Range, Max (10 Gb/s) (Port 2, Lane 0)	21368	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.3.3 Tx SSC Down Spread Range, Max (10 Gb/s) (Port 2, Lane 0)	11368	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.3.3 Tx SSC Down Spread Range, Max (10 Gb/s) (Port 2, Lane 1)	21468	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.3.3 Tx SSC Down Spread Range, Max (10 Gb/s) (Port 2, Lane 1)	11468	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.3.3 Tx SSC Down Spread Range, Max (10.3125 Gb/s) (Port 1, Lane 0)	2168	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.3.3 Tx SSC Down Spread Range, Max (10.3125 Gb/s) (Port 1, Lane 0)	1168	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.3.3 Tx SSC Down Spread Range, Max (10.3125 Gb/s) (Port 1, Lane 1)	2268	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.3.3 Tx SSC Down Spread Range, Max (10.3125 Gb/s) (Port 1, Lane 1)	1268	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.3.3 Tx SSC Down Spread Range, Max (10.3125 Gb/s) (Port 2, Lane 0)	2368	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.3 Tx SSC Down Spread Range, Max (10.3125 Gb/s) (Port 2, Lane 0)	1368	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.3.3 Tx SSC Down Spread Range, Max (10.3125 Gb/s) (Port 2, Lane 1)	2468	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.3.3 Tx SSC Down Spread Range, Max (10.3125 Gb/s) (Port 2, Lane 1)	1468	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.3.3 Tx SSC Down Spread Range, Min (10 Gb/s) (Port 1, Lane 0)	21165	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.3.3 Tx SSC Down Spread Range, Min (10 Gb/s) (Port 1, Lane 0)	11165	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.3.3 Tx SSC Down Spread Range, Min (10 Gb/s) (Port 1, Lane 1)	21265	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.3.3 Tx SSC Down Spread Range, Min (10 Gb/s) (Port 1, Lane 1)	11265	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.3.3 Tx SSC Down Spread Range, Min (10 Gb/s) (Port 2, Lane 0)	21365	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.3.3 Tx SSC Down Spread Range, Min (10 Gb/s) (Port 2, Lane 0)	11365	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.3.3 Tx SSC Down Spread Range, Min (10 Gb/s) (Port 2, Lane 1)	21465	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.3.3 Tx SSC Down Spread Range, Min (10 Gb/s) (Port 2, Lane 1)	11465	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.3.3 Tx SSC Down Spread Range, Min (10.3125 Gb/s) (Port 1, Lane 0)	2165	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.3.3 Tx SSC Down Spread Range, Min (10.3125 Gb/s) (Port 1, Lane 0)	1165	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.3.3 Tx SSC Down Spread Range, Min (10.3125 Gb/s) (Port 1, Lane 1)	2265	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.3.3 Tx SSC Down Spread Range, Min (10.3125 Gb/s) (Port 1, Lane 1)	1265	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.3.3 Tx SSC Down Spread Range, Min (10.3125 Gb/s) (Port 2, Lane 0)	2365	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.3.3 Tx SSC Down Spread Range, Min (10.3125 Gb/s) (Port 2, Lane 0)	1365	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.3.3 Tx SSC Down Spread Range, Min (10.3125 Gb/s) (Port 2, Lane 1)	2465	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.3.3 Tx SSC Down Spread Range, Min (10.3125 Gb/s) (Port 2, Lane 1)	1465	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.4 Tx SSC Down Spread Rate, Max (10 Gb/s) (Port 1, Lane 0)	21167	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
3.3.4 Tx SSC Down Spread Rate, Max (10 Gb/s) (Port 1, Lane 0)	11167	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
3.3.4 Tx SSC Down Spread Rate, Max (10 Gb/s) (Port 1, Lane 1)	21267	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
3.3.4 Tx SSC Down Spread Rate, Max (10 Gb/s) (Port 1, Lane 1)	11267	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
3.3.4 Tx SSC Down Spread Rate, Max (10 Gb/s) (Port 2, Lane 0)	21367	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
3.3.4 Tx SSC Down Spread Rate, Max (10 Gb/s) (Port 2, Lane 0)	11367	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
3.3.4 Tx SSC Down Spread Rate, Max (10 Gb/s) (Port 2, Lane 1)	21467	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
3.3.4 Tx SSC Down Spread Rate, Max (10 Gb/s) (Port 2, Lane 1)	11467	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
3.3.4 Tx SSC Down Spread Rate, Min (10 Gb/s) (Port 1, Lane 0)	21161	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
3.3.4 Tx SSC Down Spread Rate, Min (10 Gb/s) (Port 1, Lane 0)	11161	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
3.3.4 Tx SSC Down Spread Rate, Min (10 Gb/s) (Port 1, Lane 1)	21261	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
3.3.4 Tx SSC Down Spread Rate, Min (10 Gb/s) (Port 1, Lane 1)	11261	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
3.3.4 Tx SSC Down Spread Rate, Min (10 Gb/s) (Port 2, Lane 0)	21361	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
3.3.4 Tx SSC Down Spread Rate, Min (10 Gb/s) (Port 2, Lane 0)	11361	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
3.3.4 Tx SSC Down Spread Rate, Min (10 Gb/s) (Port 2, Lane 1)	21461	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
3.3.4 Tx SSC Down Spread Rate, Min (10 Gb/s) (Port 2, Lane 1)	11461	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
3.3.5 Tx SSC Phase Deviation (10 Gb/s) (Port 1, Lane 0)	21171	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 device must be within the specification.
3.3.5 Tx SSC Phase Deviation (10 Gb/s) (Port 1, Lane 0)	11171	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 host must be within the specification.
3.3.5 Tx SSC Phase Deviation (10 Gb/s) (Port 1, Lane 1)	21271	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.5 Tx SSC Phase Deviation (10 Gb/s) (Port 1, Lane 1)	11271	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 host must be within the specification.
3.3.5 Tx SSC Phase Deviation (10 Gb/s) (Port 2, Lane 0)	21371	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 device must be within the specification.
3.3.5 Tx SSC Phase Deviation (10 Gb/s) (Port 2, Lane 0)	11371	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 host must be within the specification.
3.3.5 Tx SSC Phase Deviation (10 Gb/s) (Port 2, Lane 1)	21471	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 device must be within the specification.
3.3.5 Tx SSC Phase Deviation (10 Gb/s) (Port 2, Lane 1)	11471	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 host must be within the specification.
3.3.6 Tx SSC Phase Slew Rate (10 Gb/s) (Port 1, Lane 0)	21172	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 device must be within the specification.
3.3.6 Tx SSC Phase Slew Rate (10 Gb/s) (Port 1, Lane 0)	11172	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 host must be within the specification.
3.3.6 Tx SSC Phase Slew Rate (10 Gb/s) (Port 1, Lane 1)	21272	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 device must be within the specification.
3.3.6 Tx SSC Phase Slew Rate (10 Gb/s) (Port 1, Lane 1)	11272	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 host must be within the specification.
3.3.6 Tx SSC Phase Slew Rate (10 Gb/s) (Port 2, Lane 0)	21372	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 device must be within the specification.
3.3.6 Tx SSC Phase Slew Rate (10 Gb/s) (Port 2, Lane 0)	11372	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 host must be within the specification.
3.3.6 Tx SSC Phase Slew Rate (10 Gb/s) (Port 2, Lane 1)	21472	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 device must be within the specification.
3.3.6 Tx SSC Phase Slew Rate (10 Gb/s) (Port 2, Lane 1)	11472	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 host must be within the specification.
3.3.6 Tx SSC Phase Slew Rate (10.3125 Gb/s) (Port 1, Lane 0)	2172	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 device must be within the specification.
3.3.6 Tx SSC Phase Slew Rate (10.3125 Gb/s) (Port 1, Lane 0)	1172	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 host must be within the specification.
3.3.6 Tx SSC Phase Slew Rate (10.3125 Gb/s) (Port 1, Lane 1)	2272	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 device must be within the specification.
3.3.6 Tx SSC Phase Slew Rate (10.3125 Gb/s) (Port 1, Lane 1)	1272	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 host must be within the specification.
3.3.6 Tx SSC Phase Slew Rate (10.3125 Gb/s) (Port 2, Lane 0)	2372	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 device must be within the specification.
3.3.6 Tx SSC Phase Slew Rate (10.3125 Gb/s) (Port 2, Lane 0)	1372	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.6 Tx SSC Phase Slew Rate (10.3125 Gb/s) (Port 2, Lane 1)	2472	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 device must be within the specification.
3.3.6 Tx SSC Phase Slew Rate (10.3125 Gb/s) (Port 2, Lane 1)	1472	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 host must be within the specification.
3.3.6 Tx SSC Slew Rate (10 Gb/s) (Port 1, Lane 0)	21164	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 device must be within the specification.
3.3.6 Tx SSC Slew Rate (10 Gb/s) (Port 1, Lane 0)	11164	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 host must be within the specification.
3.3.6 Tx SSC Slew Rate (10 Gb/s) (Port 1, Lane 1)	21264	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 device must be within the specification.
3.3.6 Tx SSC Slew Rate (10 Gb/s) (Port 1, Lane 1)	11264	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 host must be within the specification.
3.3.6 Tx SSC Slew Rate (10 Gb/s) (Port 2, Lane 0)	21364	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 device must be within the specification.
3.3.6 Tx SSC Slew Rate (10 Gb/s) (Port 2, Lane 0)	11364	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 host must be within the specification.
3.3.6 Tx SSC Slew Rate (10 Gb/s) (Port 2, Lane 1)	21464	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 device must be within the specification.
3.3.6 Tx SSC Slew Rate (10 Gb/s) (Port 2, Lane 1)	11464	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 host must be within the specification.
3.3.6 Tx SSC Slew Rate (10.3125 Gb/s) (Port 1, Lane 0)	2164	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 device must be within the specification.
3.3.6 Tx SSC Slew Rate (10.3125 Gb/s) (Port 1, Lane 0)	1164	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 host must be within the specification.
3.3.6 Tx SSC Slew Rate (10.3125 Gb/s) (Port 1, Lane 1)	2264	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 device must be within the specification.
3.3.6 Tx SSC Slew Rate (10.3125 Gb/s) (Port 1, Lane 1)	1264	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 host must be within the specification.
3.3.6 Tx SSC Slew Rate (10.3125 Gb/s) (Port 2, Lane 0)	2364	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 device must be within the specification.
3.3.6 Tx SSC Slew Rate (10.3125 Gb/s) (Port 2, Lane 0)	1364	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 host must be within the specification.
3.3.6 Tx SSC Slew Rate (10.3125 Gb/s) (Port 2, Lane 1)	2464	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 device must be within the specification.
3.3.6 Tx SSC Slew Rate (10.3125 Gb/s) (Port 2, Lane 1)	1464	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 host must be within the specification.
3.3.7 Tx Frequency Variation Training (10 Gb/s) (Port 1, Lane 0)	11166	The spread spectrum clocking (SSC) Frequency Variation at TP2 of a USB4 Host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.7 Tx Frequency Variation Training (10 Gb/s) (Port 1, Lane 0)	21166	The spread spectrum clocking (SSC) Frequency Variation at TP2 of a USB4 device must be within the specification.
3.3.7 Tx Frequency Variation Training (10 Gb/s) (Port 1, Lane 1)	11266	The spread spectrum clocking (SSC) Frequency Variation at TP2 of a USB4 Host must be within the specification.
3.3.7 Tx Frequency Variation Training (10 Gb/s) (Port 1, Lane 1)	21266	The spread spectrum clocking (SSC) Frequency Variation at TP2 of a USB4 device must be within the specification.
3.3.7 Tx Frequency Variation Training (10 Gb/s) (Port 2, Lane 0)	11366	The spread spectrum clocking (SSC) Frequency Variation at TP2 of a USB4 Host must be within the specification.
3.3.7 Tx Frequency Variation Training (10 Gb/s) (Port 2, Lane 0)	21366	The spread spectrum clocking (SSC) Frequency Variation at TP2 of a USB4 device must be within the specification.
3.3.7 Tx Frequency Variation Training (10 Gb/s) (Port 2, Lane 1)	11466	The spread spectrum clocking (SSC) Frequency Variation at TP2 of a USB4 Host must be within the specification.
3.3.7 Tx Frequency Variation Training (10 Gb/s) (Port 2, Lane 1)	21466	The spread spectrum clocking (SSC) Frequency Variation at TP2 of a USB4 device must be within the specification.
3.3.8 Tx Fall Time (10 Gb/s) (Port 1, Lane 0)	21112	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Fall Time (10 Gb/s) (Port 1, Lane 0)	11112	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Fall Time (10 Gb/s) (Port 1, Lane 1)	21212	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Fall Time (10 Gb/s) (Port 1, Lane 1)	11212	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Fall Time (10 Gb/s) (Port 2, Lane 0)	21312	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Fall Time (10 Gb/s) (Port 2, Lane 0)	11312	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Fall Time (10 Gb/s) (Port 2, Lane 1)	21412	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Fall Time (10 Gb/s) (Port 2, Lane 1)	11412	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.8 Tx Fall Time (10.3125 Gb/s) (Port 1, Lane 0)	2112	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Fall Time (10.3125 Gb/s) (Port 1, Lane 0)	1112	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Fall Time (10.3125 Gb/s) (Port 1, Lane 1)	2212	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Fall Time (10.3125 Gb/s) (Port 1, Lane 1)	1212	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Fall Time (10.3125 Gb/s) (Port 2, Lane 0)	2312	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Fall Time (10.3125 Gb/s) (Port 2, Lane 0)	1312	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Fall Time (10.3125 Gb/s) (Port 2, Lane 1)	2412	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Fall Time (10.3125 Gb/s) (Port 2, Lane 1)	1412	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Rise Time (10 Gb/s) (Port 1, Lane 0)	21111	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Rise Time (10 Gb/s) (Port 1, Lane 0)	11111	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Rise Time (10 Gb/s) (Port 1, Lane 1)	21211	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Rise Time (10 Gb/s) (Port 1, Lane 1)	11211	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Rise Time (10 Gb/s) (Port 2, Lane 0)	21311	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.8 Tx Rise Time (10 Gb/s) (Port 2, Lane 0)	11311	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Rise Time (10 Gb/s) (Port 2, Lane 1)	21411	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Rise Time (10 Gb/s) (Port 2, Lane 1)	11411	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Rise Time (10.3125 Gb/s) (Port 1, Lane 0)	2111	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Rise Time (10.3125 Gb/s) (Port 1, Lane 0)	1111	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Rise Time (10.3125 Gb/s) (Port 1, Lane 1)	2211	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Rise Time (10.3125 Gb/s) (Port 1, Lane 1)	1211	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Rise Time (10.3125 Gb/s) (Port 2, Lane 0)	2311	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Rise Time (10.3125 Gb/s) (Port 2, Lane 0)	1311	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Rise Time (10.3125 Gb/s) (Port 2, Lane 1)	2411	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.8 Tx Rise Time (10.3125 Gb/s) (Port 2, Lane 1)	1411	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.3.9 Tx Electrical Idle Voltage (10 Gb/s) (Port 1, Lane 0)	21141	The transmitter electrical idle output voltage at TP2 of a USB4 device must be less than maximum limit.
3.3.9 Tx Electrical Idle Voltage (10 Gb/s) (Port 1, Lane 0)	11141	The transmitter electrical idle output voltage at TP2 of a USB4 host must be less than maximum limit.
3.3.9 Tx Electrical Idle Voltage (10 Gb/s) (Port 1, Lane 1)	21241	The transmitter electrical idle output voltage at TP2 of a USB4 device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.9 Tx Electrical Idle Voltage (10 Gb/s) (Port 1, Lane 1)	11241	The transmitter electrical idle output voltage at TP2 of a USB4 host must be less than maximum limit.
3.3.9 Tx Electrical Idle Voltage (10 Gb/s) (Port 2, Lane 0)	21341	The transmitter electrical idle output voltage at TP2 of a USB4 device must be less than maximum limit.
3.3.9 Tx Electrical Idle Voltage (10 Gb/s) (Port 2, Lane 0)	11341	The transmitter electrical idle output voltage at TP2 of a USB4 host must be less than maximum limit.
3.3.9 Tx Electrical Idle Voltage (10 Gb/s) (Port 2, Lane 1)	21441	The transmitter electrical idle output voltage at TP2 of a USB4 device must be less than maximum limit.
3.3.9 Tx Electrical Idle Voltage (10 Gb/s) (Port 2, Lane 1)	11441	The transmitter electrical idle output voltage at TP2 of a USB4 host must be less than maximum limit.
3.3.9 Tx Electrical Idle Voltage (10.3125 Gb/s) (Port 1, Lane 0)	2141	The transmitter electrical idle output voltage at TP2 of a USB4 device must be less than maximum limit.
3.3.9 Tx Electrical Idle Voltage (10.3125 Gb/s) (Port 1, Lane 0)	1141	The transmitter electrical idle output voltage at TP2 of a USB4 host must be less than maximum limit.
3.3.9 Tx Electrical Idle Voltage (10.3125 Gb/s) (Port 1, Lane 1)	2241	The transmitter electrical idle output voltage at TP2 of a USB4 device must be less than maximum limit.
3.3.9 Tx Electrical Idle Voltage (10.3125 Gb/s) (Port 1, Lane 1)	1241	The transmitter electrical idle output voltage at TP2 of a USB4 host must be less than maximum limit.
3.3.9 Tx Electrical Idle Voltage (10.3125 Gb/s) (Port 2, Lane 0)	2341	The transmitter electrical idle output voltage at TP2 of a USB4 device must be less than maximum limit.
3.3.9 Tx Electrical Idle Voltage (10.3125 Gb/s) (Port 2, Lane 0)	1341	The transmitter electrical idle output voltage at TP2 of a USB4 host must be less than maximum limit.
3.3.9 Tx Electrical Idle Voltage (10.3125 Gb/s) (Port 2, Lane 1)	2441	The transmitter electrical idle output voltage at TP2 of a USB4 device must be less than maximum limit.
3.3.9 Tx Electrical Idle Voltage (10.3125 Gb/s) (Port 2, Lane 1)	1441	The transmitter electrical idle output voltage at TP2 of a USB4 host must be less than maximum limit.
3.4.1 Tx Equalization Deemphasis (20 Gb/s) (Port 1, Lane 0)	22610	The equalization level at TP2 of a USB4 device must be within the specification.
3.4.1 Tx Equalization Deemphasis (20 Gb/s) (Port 1, Lane 0)	12610	The equalization level at TP2 of a USB4 host must be within the specification.
3.4.1 Tx Equalization Deemphasis (20 Gb/s) (Port 1, Lane 1)	22620	The equalization level at TP2 of a USB4 device must be within the specification.
3.4.1 Tx Equalization Deemphasis (20 Gb/s) (Port 1, Lane 1)	12620	The equalization level at TP2 of a USB4 host must be within the specification.
3.4.1 Tx Equalization Deemphasis (20 Gb/s) (Port 2, Lane 0)	22630	The equalization level at TP2 of a USB4 device must be within the specification.
3.4.1 Tx Equalization Deemphasis (20 Gb/s) (Port 2, Lane 0)	12630	The equalization level at TP2 of a USB4 host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.1 Tx Equalization Deemphasis (20 Gb/s) (Port 2, Lane 1)	22640	The equalization level at TP2 of a USB4 device must be within the specification.
3.4.1 Tx Equalization Deemphasis (20 Gb/s) (Port 2, Lane 1)	12640	The equalization level at TP2 of a USB4 host must be within the specification.
3.4.1 Tx Equalization Deemphasis (20.625 Gb/s) (Port 1, Lane 0)	20610	The equalization level at TP2 of a USB4 device must be within the specification.
3.4.1 Tx Equalization Deemphasis (20.625 Gb/s) (Port 1, Lane 0)	10610	The equalization level at TP2 of a USB4 host must be within the specification.
3.4.1 Tx Equalization Deemphasis (20.625 Gb/s) (Port 1, Lane 1)	20620	The equalization level at TP2 of a USB4 device must be within the specification.
3.4.1 Tx Equalization Deemphasis (20.625 Gb/s) (Port 1, Lane 1)	10620	The equalization level at TP2 of a USB4 host must be within the specification.
3.4.1 Tx Equalization Deemphasis (20.625 Gb/s) (Port 2, Lane 0)	20630	The equalization level at TP2 of a USB4 device must be within the specification.
3.4.1 Tx Equalization Deemphasis (20.625 Gb/s) (Port 2, Lane 0)	10630	The equalization level at TP2 of a USB4 host must be within the specification.
3.4.1 Tx Equalization Deemphasis (20.625 Gb/s) (Port 2, Lane 1)	20640	The equalization level at TP2 of a USB4 device must be within the specification.
3.4.1 Tx Equalization Deemphasis (20.625 Gb/s) (Port 2, Lane 1)	10640	The equalization level at TP2 of a USB4 host must be within the specification.
3.4.1 Tx Equalization Preshoot (20 Gb/s) (Port 1, Lane 0)	22510	The equalization level at TP2 of a USB4 device must be within the specification.
3.4.1 Tx Equalization Preshoot (20 Gb/s) (Port 1, Lane 0)	12510	The equalization level at TP2 of a USB4 host must be within the specification.
3.4.1 Tx Equalization Preshoot (20 Gb/s) (Port 1, Lane 1)	22520	The equalization level at TP2 of a USB4 device must be within the specification.
3.4.1 Tx Equalization Preshoot (20 Gb/s) (Port 1, Lane 1)	12520	The equalization level at TP2 of a USB4 host must be within the specification.
3.4.1 Tx Equalization Preshoot (20 Gb/s) (Port 2, Lane 0)	22530	The equalization level at TP2 of a USB4 device must be within the specification.
3.4.1 Tx Equalization Preshoot (20 Gb/s) (Port 2, Lane 0)	12530	The equalization level at TP2 of a USB4 host must be within the specification.
3.4.1 Tx Equalization Preshoot (20 Gb/s) (Port 2, Lane 1)	22540	The equalization level at TP2 of a USB4 device must be within the specification.
3.4.1 Tx Equalization Preshoot (20 Gb/s) (Port 2, Lane 1)	12540	The equalization level at TP2 of a USB4 host must be within the specification.
3.4.1 Tx Equalization Preshoot (20.625 Gb/s) (Port 1, Lane 0)	20510	The equalization level at TP2 of a USB4 device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.1 Tx Equalization Preshoot (20.625 Gb/s) (Port 1, Lane 0)	10510	The equalization level at TP2 of a USB4 host must be within the specification.
3.4.1 Tx Equalization Preshoot (20.625 Gb/s) (Port 1, Lane 1)	20520	The equalization level at TP2 of a USB4 device must be within the specification.
3.4.1 Tx Equalization Preshoot (20.625 Gb/s) (Port 1, Lane 1)	10520	The equalization level at TP2 of a USB4 host must be within the specification.
3.4.1 Tx Equalization Preshoot (20.625 Gb/s) (Port 2, Lane 0)	20530	The equalization level at TP2 of a USB4 device must be within the specification.
3.4.1 Tx Equalization Preshoot (20.625 Gb/s) (Port 2, Lane 0)	10530	The equalization level at TP2 of a USB4 host must be within the specification.
3.4.1 Tx Equalization Preshoot (20.625 Gb/s) (Port 2, Lane 1)	20540	The equalization level at TP2 of a USB4 device must be within the specification.
3.4.1 Tx Equalization Preshoot (20.625 Gb/s) (Port 2, Lane 1)	10540	The equalization level at TP2 of a USB4 host must be within the specification.
3.4.1 Tx Swing Preset 15 (20 Gb/s) (Port 1, Lane 0)	22710	The transmitter swing of Preset 15 of a USB4 Device must be within the specification.
3.4.1 Tx Swing Preset 15 (20 Gb/s) (Port 1, Lane 0)	12710	The transmitter swing of Preset 15 of a USB4 host must be within the specification.
3.4.1 Tx Swing Preset 15 (20 Gb/s) (Port 1, Lane 1)	22720	The transmitter swing of Preset 15 of a USB4 Device must be within the specification.
3.4.1 Tx Swing Preset 15 (20 Gb/s) (Port 1, Lane 1)	12720	The transmitter swing of Preset 15 of a USB4 host must be within the specification.
3.4.1 Tx Swing Preset 15 (20 Gb/s) (Port 2, Lane 0)	22730	The transmitter swing of Preset 15 of a USB4 Device must be within the specification.
3.4.1 Tx Swing Preset 15 (20 Gb/s) (Port 2, Lane 0)	12730	The transmitter swing of Preset 15 of a USB4 host must be within the specification.
3.4.1 Tx Swing Preset 15 (20 Gb/s) (Port 2, Lane 1)	22740	The transmitter swing of Preset 15 of a USB4 Device must be within the specification.
3.4.1 Tx Swing Preset 15 (20 Gb/s) (Port 2, Lane 1)	12740	The transmitter swing of Preset 15 of a USB4 host must be within the specification.
3.4.1 Tx Swing Preset 15 (20.625 Gb/s) (Port 1, Lane 0)	20710	The transmitter swing of Preset 15 of a USB4 Device must be within the specification.
3.4.1 Tx Swing Preset 15 (20.625 Gb/s) (Port 1, Lane 0)	10710	The transmitter swing of Preset 15 of a USB4 host must be within the specification.
3.4.1 Tx Swing Preset 15 (20.625 Gb/s) (Port 1, Lane 1)	20720	The transmitter swing of Preset 15 of a USB4 Device must be within the specification.
3.4.1 Tx Swing Preset 15 (20.625 Gb/s) (Port 1, Lane 1)	10720	The transmitter swing of Preset 15 of a USB4 host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.1 Tx Swing Preset 15 (20.625 Gb/s) (Port 2, Lane 0)	20730	The transmitter swing of Preset 15 of a USB4 Device must be within the specification.
3.4.1 Tx Swing Preset 15 (20.625 Gb/s) (Port 2, Lane 0)	10730	The transmitter swing of Preset 15 of a USB4 host must be within the specification.
3.4.1 Tx Swing Preset 15 (20.625 Gb/s) (Port 2, Lane 1)	20740	The transmitter swing of Preset 15 of a USB4 Device must be within the specification.
3.4.1 Tx Swing Preset 15 (20.625 Gb/s) (Port 2, Lane 1)	10740	The transmitter swing of Preset 15 of a USB4 host must be within the specification.
3.4.10 Tx Total Jitter (20 Gb/s) (Port 1, Lane 0)	22671	The total jitter (TJ) of a USB4 device must be less than maximum limit.
3.4.10 Tx Total Jitter (20 Gb/s) (Port 1, Lane 0)	12671	The total jitter (TJ) of a USB4 host must be less than maximum limit.
3.4.10 Tx Total Jitter (20 Gb/s) (Port 1, Lane 1)	22672	The total jitter (TJ) of a USB4 device must be less than maximum limit.
3.4.10 Tx Total Jitter (20 Gb/s) (Port 1, Lane 1)	12672	The total jitter (TJ) of a USB4 host must be less than maximum limit.
3.4.10 Tx Total Jitter (20 Gb/s) (Port 2, Lane 0)	22673	The total jitter (TJ) of a USB4 device must be less than maximum limit.
3.4.10 Tx Total Jitter (20 Gb/s) (Port 2, Lane 0)	12673	The total jitter (TJ) of a USB4 host must be less than maximum limit.
3.4.10 Tx Total Jitter (20 Gb/s) (Port 2, Lane 1)	22674	The total jitter (TJ) of a USB4 device must be less than maximum limit.
3.4.10 Tx Total Jitter (20 Gb/s) (Port 2, Lane 1)	12674	The total jitter (TJ) of a USB4 host must be less than maximum limit.
3.4.10 Tx Total Jitter (20.625 Gb/s) (Port 1, Lane 0)	20671	The total jitter (TJ) of a USB4 device must be less than maximum limit.
3.4.10 Tx Total Jitter (20.625 Gb/s) (Port 1, Lane 0)	10671	The total jitter (TJ) of a USB4 host must be less than maximum limit.
3.4.10 Tx Total Jitter (20.625 Gb/s) (Port 1, Lane 1)	20672	The total jitter (TJ) of a USB4 device must be less than maximum limit.
3.4.10 Tx Total Jitter (20.625 Gb/s) (Port 1, Lane 1)	10672	The total jitter (TJ) of a USB4 host must be less than maximum limit.
3.4.10 Tx Total Jitter (20.625 Gb/s) (Port 2, Lane 0)	20673	The total jitter (TJ) of a USB4 device must be less than maximum limit.
3.4.10 Tx Total Jitter (20.625 Gb/s) (Port 2, Lane 0)	10673	The total jitter (TJ) of a USB4 host must be less than maximum limit.
3.4.10 Tx Total Jitter (20.625 Gb/s) (Port 2, Lane 1)	20674	The total jitter (TJ) of a USB4 device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.10 Tx Total Jitter (20.625 Gb/s) (Port 2, Lane 1)	10674	The total jitter (TJ) of a USB4 host must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (20 Gb/s) (Port 1, Lane 0)	22871	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 device must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (20 Gb/s) (Port 1, Lane 0)	12871	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 host must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (20 Gb/s) (Port 1, Lane 1)	22872	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 device must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (20 Gb/s) (Port 1, Lane 1)	12872	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 host must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (20 Gb/s) (Port 2, Lane 0)	22873	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 device must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (20 Gb/s) (Port 2, Lane 0)	12873	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 host must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (20 Gb/s) (Port 2, Lane 1)	22874	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 device must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (20 Gb/s) (Port 2, Lane 1)	12874	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 host must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (20.625 Gb/s) (Port 1, Lane 0)	20871	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 device must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (20.625 Gb/s) (Port 1, Lane 0)	10871	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 host must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (20.625 Gb/s) (Port 1, Lane 1)	20872	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 device must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (20.625 Gb/s) (Port 1, Lane 1)	10872	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 host must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (20.625 Gb/s) (Port 2, Lane 0)	20873	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 device must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (20.625 Gb/s) (Port 2, Lane 0)	10873	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 host must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (20.625 Gb/s) (Port 2, Lane 1)	20874	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 device must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (20.625 Gb/s) (Port 2, Lane 1)	10874	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a USB4 host must be less than maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (20 Gb/s) (Port 1, Lane 0)	22971	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 device must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (20 Gb/s) (Port 1, Lane 0)	12971	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 host must be less than the maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.12 Tx Uncorrelated Deterministic Jitter (20 Gb/s) (Port 1, Lane 1)	22972	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 device must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (20 Gb/s) (Port 1, Lane 1)	12972	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 host must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (20 Gb/s) (Port 2, Lane 0)	22973	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 device must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (20 Gb/s) (Port 2, Lane 0)	12973	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 host must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (20 Gb/s) (Port 2, Lane 1)	22974	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 device must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (20 Gb/s) (Port 2, Lane 1)	12974	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 host must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (20.625 Gb/s) (Port 1, Lane 0)	20971	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 device must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (20.625 Gb/s) (Port 1, Lane 0)	10971	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 host must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (20.625 Gb/s) (Port 1, Lane 1)	20972	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 device must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (20.625 Gb/s) (Port 1, Lane 1)	10972	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 host must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (20.625 Gb/s) (Port 2, Lane 0)	20973	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 device must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (20.625 Gb/s) (Port 2, Lane 0)	10973	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 host must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (20.625 Gb/s) (Port 2, Lane 1)	20974	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 device must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (20.625 Gb/s) (Port 2, Lane 1)	10974	The sum of uncorrelated deterministic jitter (UDJ) of a USB4 host must be less than the maximum limit.
3.4.13 Tx Data Dependent Jitter (20 Gb/s) (Port 1, Lane 0)	42871	The sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit.
3.4.13 Tx Data Dependent Jitter (20 Gb/s) (Port 1, Lane 0)	32871	The sum of Data Dependent Jitter (DDJ) of a USB4 host must be less than the maximum limit.
3.4.13 Tx Data Dependent Jitter (20 Gb/s) (Port 1, Lane 1)	42872	The sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit.
3.4.13 Tx Data Dependent Jitter (20 Gb/s) (Port 1, Lane 1)	32872	The sum of Data Dependent Jitter (DDJ) of a USB4 host must be less than the maximum limit.
3.4.13 Tx Data Dependent Jitter (20 Gb/s) (Port 2, Lane 0)	42873	The sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.13 Tx Data Dependent Jitter (20 Gb/s) (Port 2, Lane 0)	32873	The sum of Data Dependent Jitter (DDJ) of a USB4 host must be less than the maximum limit.
3.4.13 Tx Data Dependent Jitter (20 Gb/s) (Port 2, Lane 1)	42874	The sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit.
3.4.13 Tx Data Dependent Jitter (20 Gb/s) (Port 2, Lane 1)	32874	The sum of Data Dependent Jitter (DDJ) of a USB4 host must be less than the maximum limit.
3.4.13 Tx Data Dependent Jitter (20.625 Gb/s) (Port 1, Lane 0)	40871	The sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit.
3.4.13 Tx Data Dependent Jitter (20.625 Gb/s) (Port 1, Lane 0)	30871	The sum of Data Dependent Jitter (DDJ) of a USB4 host must be less than the maximum limit.
3.4.13 Tx Data Dependent Jitter (20.625 Gb/s) (Port 1, Lane 1)	40872	The sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit.
3.4.13 Tx Data Dependent Jitter (20.625 Gb/s) (Port 1, Lane 1)	30872	The sum of Data Dependent Jitter (DDJ) of a USB4 host must be less than the maximum limit.
3.4.13 Tx Data Dependent Jitter (20.625 Gb/s) (Port 2, Lane 0)	40873	The sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit.
3.4.13 Tx Data Dependent Jitter (20.625 Gb/s) (Port 2, Lane 0)	30873	The sum of Data Dependent Jitter (DDJ) of a USB4 host must be less than the maximum limit.
3.4.13 Tx Data Dependent Jitter (20.625 Gb/s) (Port 2, Lane 1)	40874	The sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit.
3.4.13 Tx Data Dependent Jitter (20.625 Gb/s) (Port 2, Lane 1)	30874	The sum of Data Dependent Jitter (DDJ) of a USB4 host must be less than the maximum limit.
3.4.14 Tx Low Frequency Uncorrelated Deterministic Jitter (20 Gb/s) (Port 1, Lane 0)	22981	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 device must be less than the maximum limit.
3.4.14 Tx Low Frequency Uncorrelated Deterministic Jitter (20 Gb/s) (Port 1, Lane 0)	12981	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 host must be less than the maximum limit.
3.4.14 Tx Low Frequency Uncorrelated Deterministic Jitter (20 Gb/s) (Port 1, Lane 1)	22982	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 device must be less than the maximum limit.
3.4.14 Tx Low Frequency Uncorrelated Deterministic Jitter (20 Gb/s) (Port 1, Lane 1)	12982	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 host must be less than the maximum limit.
3.4.14 Tx Low Frequency Uncorrelated Deterministic Jitter (20 Gb/s) (Port 2, Lane 0)	22983	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 device must be less than the maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.14 Tx Low Frequency Uncorrelated Deterministic Jitter (20 Gb/s) (Port 2, Lane 0)	12983	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 host must be less than the maximum limit.
3.4.14 Tx Low Frequency Uncorrelated Deterministic Jitter (20 Gb/s) (Port 2, Lane 1)	22984	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 device must be less than the maximum limit.
3.4.14 Tx Low Frequency Uncorrelated Deterministic Jitter (20 Gb/s) (Port 2, Lane 1)	12984	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 host must be less than the maximum limit.
3.4.14 Tx Low Frequency Uncorrelated Deterministic Jitter (20.625 Gb/s) (Port 1, Lane 0)	20981	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 device must be less than the maximum limit.
3.4.14 Tx Low Frequency Uncorrelated Deterministic Jitter (20.625 Gb/s) (Port 1, Lane 0)	10981	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 host must be less than the maximum limit.
3.4.14 Tx Low Frequency Uncorrelated Deterministic Jitter (20.625 Gb/s) (Port 1, Lane 1)	20982	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 device must be less than the maximum limit.
3.4.14 Tx Low Frequency Uncorrelated Deterministic Jitter (20.625 Gb/s) (Port 1, Lane 1)	10982	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 host must be less than the maximum limit.
3.4.14 Tx Low Frequency Uncorrelated Deterministic Jitter (20.625 Gb/s) (Port 2, Lane 0)	20983	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 device must be less than the maximum limit.
3.4.14 Tx Low Frequency Uncorrelated Deterministic Jitter (20.625 Gb/s) (Port 2, Lane 0)	10983	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 host must be less than the maximum limit.
3.4.14 Tx Low Frequency Uncorrelated Deterministic Jitter (20.625 Gb/s) (Port 2, Lane 1)	20984	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 device must be less than the maximum limit.
3.4.14 Tx Low Frequency Uncorrelated Deterministic Jitter (20.625 Gb/s) (Port 2, Lane 1)	10984	The sum of low frequency uncorrelated deterministic jitter (UDJ_LF) of a USB4 host must be less than the maximum limit.
3.4.15 Tx Duty Cycle Distortion (20 Gb/s) (Port 1, Lane 0)	22961	The sum of Duty Cycle Distortion (DCD) of a USB4 device must be less than the maximum limit.
3.4.15 Tx Duty Cycle Distortion (20 Gb/s) (Port 1, Lane 0)	12961	The sum of Duty Cycle Distortion (DCD) of a USB4 host must be less than the maximum limit.
3.4.15 Tx Duty Cycle Distortion (20 Gb/s) (Port 1, Lane 1)	22962	The sum of Duty Cycle Distortion (DCD) of a USB4 device must be less than the maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.15 Tx Duty Cycle Distortion (20 Gb/s) (Port 1, Lane 1)	12962	The sum of Duty Cycle Distortion (DCD) of a USB4 host must be less than the maximum limit.
3.4.15 Tx Duty Cycle Distortion (20 Gb/s) (Port 2, Lane 0)	22963	The sum of Duty Cycle Distortion (DCD) of a USB4 device must be less than the maximum limit.
3.4.15 Tx Duty Cycle Distortion (20 Gb/s) (Port 2, Lane 0)	12963	The sum of Duty Cycle Distortion (DCD) of a USB4 host must be less than the maximum limit.
3.4.15 Tx Duty Cycle Distortion (20 Gb/s) (Port 2, Lane 1)	22964	The sum of Duty Cycle Distortion (DCD) of a USB4 device must be less than the maximum limit.
3.4.15 Tx Duty Cycle Distortion (20 Gb/s) (Port 2, Lane 1)	12964	The sum of Duty Cycle Distortion (DCD) of a USB4 host must be less than the maximum limit.
3.4.15 Tx Duty Cycle Distortion (20.625 Gb/s) (Port 1, Lane 0)	20961	The sum of Duty Cycle Distortion (DCD) of a USB4 device must be less than the maximum limit.
3.4.15 Tx Duty Cycle Distortion (20.625 Gb/s) (Port 1, Lane 0)	10961	The sum of Duty Cycle Distortion (DCD) of a USB4 host must be less than the maximum limit.
3.4.15 Tx Duty Cycle Distortion (20.625 Gb/s) (Port 1, Lane 1)	20962	The sum of Duty Cycle Distortion (DCD) of a USB4 device must be less than the maximum limit.
3.4.15 Tx Duty Cycle Distortion (20.625 Gb/s) (Port 1, Lane 1)	10962	The sum of Duty Cycle Distortion (DCD) of a USB4 host must be less than the maximum limit.
3.4.15 Tx Duty Cycle Distortion (20.625 Gb/s) (Port 2, Lane 0)	20963	The sum of Duty Cycle Distortion (DCD) of a USB4 device must be less than the maximum limit.
3.4.15 Tx Duty Cycle Distortion (20.625 Gb/s) (Port 2, Lane 0)	10963	The sum of Duty Cycle Distortion (DCD) of a USB4 host must be less than the maximum limit.
3.4.15 Tx Duty Cycle Distortion (20.625 Gb/s) (Port 2, Lane 1)	20964	The sum of Duty Cycle Distortion (DCD) of a USB4 device must be less than the maximum limit.
3.4.15 Tx Duty Cycle Distortion (20.625 Gb/s) (Port 2, Lane 1)	10964	The sum of Duty Cycle Distortion (DCD) of a USB4 host must be less than the maximum limit.
3.4.16 Tx AC Common Mode Voltage (20 Gb/s) (Port 1, Lane 0)	22121	The AC common mode peak-to-peak voltage at TP2 of a USB4 device must be less than maximum limit.
3.4.16 Tx AC Common Mode Voltage (20 Gb/s) (Port 1, Lane 0)	12121	The AC common mode peak-to-peak voltage at TP2 of a USB4 host must be less than maximum limit.
3.4.16 Tx AC Common Mode Voltage (20 Gb/s) (Port 1, Lane 1)	22221	The AC common mode peak-to-peak voltage at TP2 of a USB4 device must be less than maximum limit.
3.4.16 Tx AC Common Mode Voltage (20 Gb/s) (Port 1, Lane 1)	12221	The AC common mode peak-to-peak voltage at TP2 of a USB4 host must be less than maximum limit.
3.4.16 Tx AC Common Mode Voltage (20 Gb/s) (Port 2, Lane 0)	22321	The AC common mode peak-to-peak voltage at TP2 of a USB4 device must be less than maximum limit.
3.4.16 Tx AC Common Mode Voltage (20 Gb/s) (Port 2, Lane 0)	12321	The AC common mode peak-to-peak voltage at TP2 of a USB4 host must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.16 Tx AC Common Mode Voltage (20 Gb/s) (Port 2, Lane 1)	22421	The AC common mode peak-to-peak voltage at TP2 of a USB4 device must be less than maximum limit.
3.4.16 Tx AC Common Mode Voltage (20 Gb/s) (Port 2, Lane 1)	12421	The AC common mode peak-to-peak voltage at TP2 of a USB4 host must be less than maximum limit.
3.4.16 Tx AC Common Mode Voltage (20.625 Gb/s) (Port 1, Lane 0)	20121	The AC common mode peak-to-peak voltage at TP2 of a USB4 device must be less than maximum limit.
3.4.16 Tx AC Common Mode Voltage (20.625 Gb/s) (Port 1, Lane 0)	10121	The AC common mode peak-to-peak voltage at TP2 of a USB4 host must be less than maximum limit.
3.4.16 Tx AC Common Mode Voltage (20.625 Gb/s) (Port 1, Lane 1)	20221	The AC common mode peak-to-peak voltage at TP2 of a USB4 device must be less than maximum limit.
3.4.16 Tx AC Common Mode Voltage (20.625 Gb/s) (Port 1, Lane 1)	10221	The AC common mode peak-to-peak voltage at TP2 of a USB4 host must be less than maximum limit.
3.4.16 Tx AC Common Mode Voltage (20.625 Gb/s) (Port 2, Lane 0)	20321	The AC common mode peak-to-peak voltage at TP2 of a USB4 device must be less than maximum limit.
3.4.16 Tx AC Common Mode Voltage (20.625 Gb/s) (Port 2, Lane 0)	10321	The AC common mode peak-to-peak voltage at TP2 of a USB4 host must be less than maximum limit.
3.4.16 Tx AC Common Mode Voltage (20.625 Gb/s) (Port 2, Lane 1)	20421	The AC common mode peak-to-peak voltage at TP2 of a USB4 device must be less than maximum limit.
3.4.16 Tx AC Common Mode Voltage (20.625 Gb/s) (Port 2, Lane 1)	10421	The AC common mode peak-to-peak voltage at TP2 of a USB4 host must be less than maximum limit.
3.4.17 Tx Eye Diagram (20 Gb/s) (Port 1, Lane 0)	22131	The eye diagram at TP2 of a USB4 device must be within the template as described in the specification.
3.4.17 Tx Eye Diagram (20 Gb/s) (Port 1, Lane 0)	12131	The eye diagram at TP2 of a USB4 host must be within the template as described in the specification.
3.4.17 Tx Eye Diagram (20 Gb/s) (Port 1, Lane 1)	22231	The eye diagram at TP2 of a USB4 device must be within the template as described in the specification.
3.4.17 Tx Eye Diagram (20 Gb/s) (Port 1, Lane 1)	12231	The eye diagram at TP2 of a USB4 host must be within the template as described in the specification.
3.4.17 Tx Eye Diagram (20 Gb/s) (Port 2, Lane 0)	22331	The eye diagram at TP2 of a USB4 device must be within the template as described in the specification.
3.4.17 Tx Eye Diagram (20 Gb/s) (Port 2, Lane 0)	12331	The eye diagram at TP2 of a USB4 host must be within the template as described in the specification.
3.4.17 Tx Eye Diagram (20 Gb/s) (Port 2, Lane 1)	22431	The eye diagram at TP2 of a USB4 device must be within the template as described in the specification.
3.4.17 Tx Eye Diagram (20 Gb/s) (Port 2, Lane 1)	12431	The eye diagram at TP2 of a USB4 host must be within the template as described in the specification.
3.4.17 Tx Eye Diagram (20.625 Gb/s) (Port 1, Lane 0)	20131	The eye diagram at TP2 of a USB4 device must be within the template as described in the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.17 Tx Eye Diagram (20.625 Gb/s) (Port 1, Lane 0)	10131	The eye diagram at TP2 of a USB4 host must be within the template as described in the specification.
3.4.17 Tx Eye Diagram (20.625 Gb/s) (Port 1, Lane 1)	20231	The eye diagram at TP2 of a USB4 device must be within the template as described in the specification.
3.4.17 Tx Eye Diagram (20.625 Gb/s) (Port 1, Lane 1)	10231	The eye diagram at TP2 of a USB4 host must be within the template as described in the specification.
3.4.17 Tx Eye Diagram (20.625 Gb/s) (Port 2, Lane 0)	20331	The eye diagram at TP2 of a USB4 device must be within the template as described in the specification.
3.4.17 Tx Eye Diagram (20.625 Gb/s) (Port 2, Lane 0)	10331	The eye diagram at TP2 of a USB4 host must be within the template as described in the specification.
3.4.17 Tx Eye Diagram (20.625 Gb/s) (Port 2, Lane 1)	20431	The eye diagram at TP2 of a USB4 device must be within the template as described in the specification.
3.4.17 Tx Eye Diagram (20.625 Gb/s) (Port 2, Lane 1)	10431	The eye diagram at TP2 of a USB4 host must be within the template as described in the specification.
3.4.18 Tx Total Jitter TP3 (20 Gb/s) (Port 1, Lane 0)	22661	The total jitter (TJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.18 Tx Total Jitter TP3 (20 Gb/s) (Port 1, Lane 0)	12661	The total jitter (TJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.18 Tx Total Jitter TP3 (20 Gb/s) (Port 1, Lane 1)	22662	The total jitter (TJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.18 Tx Total Jitter TP3 (20 Gb/s) (Port 1, Lane 1)	12662	The total jitter (TJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.18 Tx Total Jitter TP3 (20 Gb/s) (Port 2, Lane 0)	22663	The total jitter (TJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.18 Tx Total Jitter TP3 (20 Gb/s) (Port 2, Lane 0)	12663	The total jitter (TJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.18 Tx Total Jitter TP3 (20 Gb/s) (Port 2, Lane 1)	22664	The total jitter (TJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.18 Tx Total Jitter TP3 (20 Gb/s) (Port 2, Lane 1)	12664	The total jitter (TJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.18 Tx Total Jitter TP3 (20.625 Gb/s) (Port 1, Lane 0)	20661	The total jitter (TJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.18 Tx Total Jitter TP3 (20.625 Gb/s) (Port 1, Lane 0)	10661	The total jitter (TJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.18 Tx Total Jitter TP3 (20.625 Gb/s) (Port 1, Lane 1)	20662	The total jitter (TJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.18 Tx Total Jitter TP3 (20.625 Gb/s) (Port 1, Lane 1)	10662	The total jitter (TJ) at TP3 of a USB4 host must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.18 Tx Total Jitter TP3 (20.625 Gb/s) (Port 2, Lane 0)	20663	The total jitter (TJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.18 Tx Total Jitter TP3 (20.625 Gb/s) (Port 2, Lane 0)	10663	The total jitter (TJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.18 Tx Total Jitter TP3 (20.625 Gb/s) (Port 2, Lane 1)	20664	The total jitter (TJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.18 Tx Total Jitter TP3 (20.625 Gb/s) (Port 2, Lane 1)	10664	The total jitter (TJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.19 Tx Uncorrelated Jitter TP3 (20 Gb/s) (Port 1, Lane 0)	22771	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.19 Tx Uncorrelated Jitter TP3 (20 Gb/s) (Port 1, Lane 0)	12771	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.19 Tx Uncorrelated Jitter TP3 (20 Gb/s) (Port 1, Lane 1)	22772	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.19 Tx Uncorrelated Jitter TP3 (20 Gb/s) (Port 1, Lane 1)	12772	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.19 Tx Uncorrelated Jitter TP3 (20 Gb/s) (Port 2, Lane 0)	22773	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.19 Tx Uncorrelated Jitter TP3 (20 Gb/s) (Port 2, Lane 0)	12773	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.19 Tx Uncorrelated Jitter TP3 (20 Gb/s) (Port 2, Lane 1)	22774	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.19 Tx Uncorrelated Jitter TP3 (20 Gb/s) (Port 2, Lane 1)	12774	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.19 Tx Uncorrelated Jitter TP3 (20.625 Gb/s) (Port 1, Lane 0)	20771	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.19 Tx Uncorrelated Jitter TP3 (20.625 Gb/s) (Port 1, Lane 0)	10771	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.19 Tx Uncorrelated Jitter TP3 (20.625 Gb/s) (Port 1, Lane 1)	20772	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.19 Tx Uncorrelated Jitter TP3 (20.625 Gb/s) (Port 1, Lane 1)	10772	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.19 Tx Uncorrelated Jitter TP3 (20.625 Gb/s) (Port 2, Lane 0)	20773	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.19 Tx Uncorrelated Jitter TP3 (20.625 Gb/s) (Port 2, Lane 0)	10773	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.19 Tx Uncorrelated Jitter TP3 (20.625 Gb/s) (Port 2, Lane 1)	20774	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.19 Tx Uncorrelated Jitter TP3 (20.625 Gb/s) (Port 2, Lane 1)	10774	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.2 Tx Minimum Unit Interval, Max (20 Gb/s) (Port 1, Lane 0)	22152	The minimum unit interval at TP2 of a USB4 device must be within the specification.
3.4.2 Tx Minimum Unit Interval, Max (20 Gb/s) (Port 1, Lane 0)	12152	The minimum unit interval at TP2 of a USB4 host must be within the specification.
3.4.2 Tx Minimum Unit Interval, Max (20 Gb/s) (Port 1, Lane 1)	22252	The minimum unit interval at TP2 of a USB4 device must be within the specification.
3.4.2 Tx Minimum Unit Interval, Max (20 Gb/s) (Port 1, Lane 1)	12252	The minimum unit interval at TP2 of a USB4 host must be within the specification.
3.4.2 Tx Minimum Unit Interval, Max (20 Gb/s) (Port 2, Lane 0)	22352	The minimum unit interval at TP2 of a USB4 device must be within the specification.
3.4.2 Tx Minimum Unit Interval, Max (20 Gb/s) (Port 2, Lane 0)	12352	The minimum unit interval at TP2 of a USB4 host must be within the specification.
3.4.2 Tx Minimum Unit Interval, Max (20 Gb/s) (Port 2, Lane 1)	22452	The minimum unit interval at TP2 of a USB4 device must be within the specification.
3.4.2 Tx Minimum Unit Interval, Max (20 Gb/s) (Port 2, Lane 1)	12452	The minimum unit interval at TP2 of a USB4 host must be within the specification.
3.4.2 Tx Minimum Unit Interval, Min (20 Gb/s) (Port 1, Lane 0)	22151	The minimum unit interval at TP2 of a USB4 device must be within the specification.
3.4.2 Tx Minimum Unit Interval, Min (20 Gb/s) (Port 1, Lane 0)	12151	The minimum unit interval at TP2 of a USB4 host must be within the specification.
3.4.2 Tx Minimum Unit Interval, Min (20 Gb/s) (Port 1, Lane 1)	22251	The minimum unit interval at TP2 of a USB4 device must be within the specification.
3.4.2 Tx Minimum Unit Interval, Min (20 Gb/s) (Port 1, Lane 1)	12251	The minimum unit interval at TP2 of a USB4 host must be within the specification.
3.4.2 Tx Minimum Unit Interval, Min (20 Gb/s) (Port 2, Lane 0)	22351	The minimum unit interval at TP2 of a USB4 device must be within the specification.
3.4.2 Tx Minimum Unit Interval, Min (20 Gb/s) (Port 2, Lane 0)	12351	The minimum unit interval at TP2 of a USB4 host must be within the specification.
3.4.2 Tx Minimum Unit Interval, Min (20 Gb/s) (Port 2, Lane 1)	22451	The minimum unit interval at TP2 of a USB4 device must be within the specification.
3.4.2 Tx Minimum Unit Interval, Min (20 Gb/s) (Port 2, Lane 1)	12451	The minimum unit interval at TP2 of a USB4 host must be within the specification.
3.4.20 Tx Uncorrelated Deterministic Jitter TP3 (20 Gb/s) (Port 1, Lane 0)	22881	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.20 Tx Uncorrelated Deterministic Jitter TP3 (20 Gb/s) (Port 1, Lane 0)	12881	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 host must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.20 Tx Uncorrelated Deterministic Jitter TP3 (20 Gb/s) (Port 1, Lane 1)	22882	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.20 Tx Uncorrelated Deterministic Jitter TP3 (20 Gb/s) (Port 1, Lane 1)	12882	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.20 Tx Uncorrelated Deterministic Jitter TP3 (20 Gb/s) (Port 2, Lane 0)	22883	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.20 Tx Uncorrelated Deterministic Jitter TP3 (20 Gb/s) (Port 2, Lane 0)	12883	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.20 Tx Uncorrelated Deterministic Jitter TP3 (20 Gb/s) (Port 2, Lane 1)	22884	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.20 Tx Uncorrelated Deterministic Jitter TP3 (20 Gb/s) (Port 2, Lane 1)	12884	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.20 Tx Uncorrelated Deterministic Jitter TP3 (20.625 Gb/s) (Port 1, Lane 0)	20881	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.20 Tx Uncorrelated Deterministic Jitter TP3 (20.625 Gb/s) (Port 1, Lane 0)	10881	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.20 Tx Uncorrelated Deterministic Jitter TP3 (20.625 Gb/s) (Port 1, Lane 1)	20882	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.20 Tx Uncorrelated Deterministic Jitter TP3 (20.625 Gb/s) (Port 1, Lane 1)	10882	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.20 Tx Uncorrelated Deterministic Jitter TP3 (20.625 Gb/s) (Port 2, Lane 0)	20883	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.20 Tx Uncorrelated Deterministic Jitter TP3 (20.625 Gb/s) (Port 2, Lane 0)	10883	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.20 Tx Uncorrelated Deterministic Jitter TP3 (20.625 Gb/s) (Port 2, Lane 1)	20884	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 device must be less than maximum limit.
3.4.20 Tx Uncorrelated Deterministic Jitter TP3 (20.625 Gb/s) (Port 2, Lane 1)	10884	The sum of uncorrelated deterministic jitter (UDJ) at TP3 of a USB4 host must be less than maximum limit.
3.4.21 Tx Eye Diagram TP3 (20 Gb/s) (Port 1, Lane 0)	22991	The eye diagram at TP3 of a USB4 device must be within the template as described in the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.21 Tx Eye Diagram TP3 (20 Gb/s) (Port 1, Lane 0)	12991	The eye diagram at TP3 of a USB4 host must be within the template as described in the specification.
3.4.21 Tx Eye Diagram TP3 (20 Gb/s) (Port 1, Lane 1)	22992	The eye diagram at TP3 of a USB4 device must be within the template as described in the specification.
3.4.21 Tx Eye Diagram TP3 (20 Gb/s) (Port 1, Lane 1)	12992	The eye diagram at TP3 of a USB4 host must be within the template as described in the specification.
3.4.21 Tx Eye Diagram TP3 (20 Gb/s) (Port 2, Lane 0)	22993	The eye diagram at TP3 of a USB4 device must be within the template as described in the specification.
3.4.21 Tx Eye Diagram TP3 (20 Gb/s) (Port 2, Lane 0)	12993	The eye diagram at TP3 of a USB4 host must be within the template as described in the specification.
3.4.21 Tx Eye Diagram TP3 (20 Gb/s) (Port 2, Lane 1)	22994	The eye diagram at TP3 of a USB4 device must be within the template as described in the specification.
3.4.21 Tx Eye Diagram TP3 (20 Gb/s) (Port 2, Lane 1)	12994	The eye diagram at TP3 of a USB4 host must be within the template as described in the specification.
3.4.21 Tx Eye Diagram TP3 (20.625 Gb/s) (Port 1, Lane 0)	20991	The eye diagram at TP3 of a USB4 device must be within the template as described in the specification.
3.4.21 Tx Eye Diagram TP3 (20.625 Gb/s) (Port 1, Lane 0)	10991	The eye diagram at TP3 of a USB4 host must be within the template as described in the specification.
3.4.21 Tx Eye Diagram TP3 (20.625 Gb/s) (Port 1, Lane 1)	20992	The eye diagram at TP3 of a USB4 device must be within the template as described in the specification.
3.4.21 Tx Eye Diagram TP3 (20.625 Gb/s) (Port 1, Lane 1)	10992	The eye diagram at TP3 of a USB4 host must be within the template as described in the specification.
3.4.21 Tx Eye Diagram TP3 (20.625 Gb/s) (Port 2, Lane 0)	20993	The eye diagram at TP3 of a USB4 device must be within the template as described in the specification.
3.4.21 Tx Eye Diagram TP3 (20.625 Gb/s) (Port 2, Lane 0)	10993	The eye diagram at TP3 of a USB4 host must be within the template as described in the specification.
3.4.21 Tx Eye Diagram TP3 (20.625 Gb/s) (Port 2, Lane 1)	20994	The eye diagram at TP3 of a USB4 device must be within the template as described in the specification.
3.4.21 Tx Eye Diagram TP3 (20.625 Gb/s) (Port 2, Lane 1)	10994	The eye diagram at TP3 of a USB4 host must be within the template as described in the specification.
3.4.3 Tx SSC Down Spread Range, Max (20 Gb/s) (Port 1, Lane 0)	22168	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.4.3 Tx SSC Down Spread Range, Max (20 Gb/s) (Port 1, Lane 0)	12168	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.4.3 Tx SSC Down Spread Range, Max (20 Gb/s) (Port 1, Lane 1)	22268	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.4.3 Tx SSC Down Spread Range, Max (20 Gb/s) (Port 1, Lane 1)	12268	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.3 Tx SSC Down Spread Range, Max (20 Gb/s) (Port 2, Lane 0)	22368	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.4.3 Tx SSC Down Spread Range, Max (20 Gb/s) (Port 2, Lane 0)	12368	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.4.3 Tx SSC Down Spread Range, Max (20 Gb/s) (Port 2, Lane 1)	22468	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.4.3 Tx SSC Down Spread Range, Max (20 Gb/s) (Port 2, Lane 1)	12468	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.4.3 Tx SSC Down Spread Range, Max (20.625 Gb/s) (Port 1, Lane 0)	20168	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.4.3 Tx SSC Down Spread Range, Max (20.625 Gb/s) (Port 1, Lane 0)	10168	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.4.3 Tx SSC Down Spread Range, Max (20.625 Gb/s) (Port 1, Lane 1)	20268	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.4.3 Tx SSC Down Spread Range, Max (20.625 Gb/s) (Port 1, Lane 1)	10268	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.4.3 Tx SSC Down Spread Range, Max (20.625 Gb/s) (Port 2, Lane 0)	20368	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.4.3 Tx SSC Down Spread Range, Max (20.625 Gb/s) (Port 2, Lane 0)	10368	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.4.3 Tx SSC Down Spread Range, Max (20.625 Gb/s) (Port 2, Lane 1)	20468	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.4.3 Tx SSC Down Spread Range, Max (20.625 Gb/s) (Port 2, Lane 1)	10468	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.4.3 Tx SSC Down Spread Range, Min (20 Gb/s) (Port 1, Lane 0)	22165	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.4.3 Tx SSC Down Spread Range, Min (20 Gb/s) (Port 1, Lane 0)	12165	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.4.3 Tx SSC Down Spread Range, Min (20 Gb/s) (Port 1, Lane 1)	22265	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.4.3 Tx SSC Down Spread Range, Min (20 Gb/s) (Port 1, Lane 1)	12265	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.4.3 Tx SSC Down Spread Range, Min (20 Gb/s) (Port 2, Lane 0)	22365	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.4.3 Tx SSC Down Spread Range, Min (20 Gb/s) (Port 2, Lane 0)	12365	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.4.3 Tx SSC Down Spread Range, Min (20 Gb/s) (Port 2, Lane 1)	22465	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.3 Tx SSC Down Spread Range, Min (20 Gb/s) (Port 2, Lane 1)	12465	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.4.3 Tx SSC Down Spread Range, Min (20.625 Gb/s) (Port 1, Lane 0)	20165	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.4.3 Tx SSC Down Spread Range, Min (20.625 Gb/s) (Port 1, Lane 0)	10165	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.4.3 Tx SSC Down Spread Range, Min (20.625 Gb/s) (Port 1, Lane 1)	20265	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.4.3 Tx SSC Down Spread Range, Min (20.625 Gb/s) (Port 1, Lane 1)	10265	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.4.3 Tx SSC Down Spread Range, Min (20.625 Gb/s) (Port 2, Lane 0)	20365	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.4.3 Tx SSC Down Spread Range, Min (20.625 Gb/s) (Port 2, Lane 0)	10365	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.4.3 Tx SSC Down Spread Range, Min (20.625 Gb/s) (Port 2, Lane 1)	20465	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 device must be within the specification.
3.4.3 Tx SSC Down Spread Range, Min (20.625 Gb/s) (Port 2, Lane 1)	10465	The spread spectrum clocking (SSC) modulation dynamic range at TP2 of a USB4 host must be within the specification.
3.4.4 Tx SSC Down Spread Rate, Max (20 Gb/s) (Port 1, Lane 0)	22167	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
3.4.4 Tx SSC Down Spread Rate, Max (20 Gb/s) (Port 1, Lane 0)	12167	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
3.4.4 Tx SSC Down Spread Rate, Max (20 Gb/s) (Port 1, Lane 1)	22267	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
3.4.4 Tx SSC Down Spread Rate, Max (20 Gb/s) (Port 1, Lane 1)	12267	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
3.4.4 Tx SSC Down Spread Rate, Max (20 Gb/s) (Port 2, Lane 0)	22367	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
3.4.4 Tx SSC Down Spread Rate, Max (20 Gb/s) (Port 2, Lane 0)	12367	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
3.4.4 Tx SSC Down Spread Rate, Max (20 Gb/s) (Port 2, Lane 1)	22467	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
3.4.4 Tx SSC Down Spread Rate, Max (20 Gb/s) (Port 2, Lane 1)	12467	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
3.4.4 Tx SSC Down Spread Rate, Min (20 Gb/s) (Port 1, Lane 0)	22161	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
3.4.4 Tx SSC Down Spread Rate, Min (20 Gb/s) (Port 1, Lane 0)	12161	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.4 Tx SSC Down Spread Rate, Min (20 Gb/s) (Port 1, Lane 1)	22261	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
3.4.4 Tx SSC Down Spread Rate, Min (20 Gb/s) (Port 1, Lane 1)	12261	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
3.4.4 Tx SSC Down Spread Rate, Min (20 Gb/s) (Port 2, Lane 0)	22361	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
3.4.4 Tx SSC Down Spread Rate, Min (20 Gb/s) (Port 2, Lane 0)	12361	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
3.4.4 Tx SSC Down Spread Rate, Min (20 Gb/s) (Port 2, Lane 1)	22461	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
3.4.4 Tx SSC Down Spread Rate, Min (20 Gb/s) (Port 2, Lane 1)	12461	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
3.4.5 Tx SSC Phase Deviation (20 Gb/s) (Port 1, Lane 0)	22171	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 device must be within the specification.
3.4.5 Tx SSC Phase Deviation (20 Gb/s) (Port 1, Lane 0)	12171	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 host must be within the specification.
3.4.5 Tx SSC Phase Deviation (20 Gb/s) (Port 1, Lane 1)	22271	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 device must be within the specification.
3.4.5 Tx SSC Phase Deviation (20 Gb/s) (Port 1, Lane 1)	12271	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 host must be within the specification.
3.4.5 Tx SSC Phase Deviation (20 Gb/s) (Port 2, Lane 0)	22371	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 device must be within the specification.
3.4.5 Tx SSC Phase Deviation (20 Gb/s) (Port 2, Lane 0)	12371	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 host must be within the specification.
3.4.5 Tx SSC Phase Deviation (20 Gb/s) (Port 2, Lane 1)	22471	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 device must be within the specification.
3.4.5 Tx SSC Phase Deviation (20 Gb/s) (Port 2, Lane 1)	12471	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 host must be within the specification.
3.4.6 Tx SSC Phase Slew Rate (20 Gb/s) (Port 1, Lane 0)	22172	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 device must be within the specification.
3.4.6 Tx SSC Phase Slew Rate (20 Gb/s) (Port 1, Lane 0)	12172	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 host must be within the specification.
3.4.6 Tx SSC Phase Slew Rate (20 Gb/s) (Port 1, Lane 1)	22272	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 device must be within the specification.
3.4.6 Tx SSC Phase Slew Rate (20 Gb/s) (Port 1, Lane 1)	12272	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 host must be within the specification.
3.4.6 Tx SSC Phase Slew Rate (20 Gb/s) (Port 2, Lane 0)	22372	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.6 Tx SSC Phase Slew Rate (20 Gb/s) (Port 2, Lane 0)	12372	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 host must be within the specification.
3.4.6 Tx SSC Phase Slew Rate (20 Gb/s) (Port 2, Lane 1)	22472	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 device must be within the specification.
3.4.6 Tx SSC Phase Slew Rate (20 Gb/s) (Port 2, Lane 1)	12472	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 host must be within the specification.
3.4.6 Tx SSC Phase Slew Rate (20.625 Gb/s) (Port 1, Lane 0)	20172	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 device must be within the specification.
3.4.6 Tx SSC Phase Slew Rate (20.625 Gb/s) (Port 1, Lane 0)	10172	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 host must be within the specification.
3.4.6 Tx SSC Phase Slew Rate (20.625 Gb/s) (Port 1, Lane 1)	20272	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 device must be within the specification.
3.4.6 Tx SSC Phase Slew Rate (20.625 Gb/s) (Port 1, Lane 1)	10272	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 host must be within the specification.
3.4.6 Tx SSC Phase Slew Rate (20.625 Gb/s) (Port 2, Lane 0)	20372	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 device must be within the specification.
3.4.6 Tx SSC Phase Slew Rate (20.625 Gb/s) (Port 2, Lane 0)	10372	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 host must be within the specification.
3.4.6 Tx SSC Phase Slew Rate (20.625 Gb/s) (Port 2, Lane 1)	20472	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 device must be within the specification.
3.4.6 Tx SSC Phase Slew Rate (20.625 Gb/s) (Port 2, Lane 1)	10472	The spread spectrum clocking (SSC) phase slew rate at TP2 of a USB4 host must be within the specification.
3.4.6 Tx SSC Slew Rate (20 Gb/s) (Port 1, Lane 0)	22164	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 device must be within the specification.
3.4.6 Tx SSC Slew Rate (20 Gb/s) (Port 1, Lane 0)	12164	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 host must be within the specification.
3.4.6 Tx SSC Slew Rate (20 Gb/s) (Port 1, Lane 1)	22264	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 device must be within the specification.
3.4.6 Tx SSC Slew Rate (20 Gb/s) (Port 1, Lane 1)	12264	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 host must be within the specification.
3.4.6 Tx SSC Slew Rate (20 Gb/s) (Port 2, Lane 0)	22364	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 device must be within the specification.
3.4.6 Tx SSC Slew Rate (20 Gb/s) (Port 2, Lane 0)	12364	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 host must be within the specification.
3.4.6 Tx SSC Slew Rate (20 Gb/s) (Port 2, Lane 1)	22464	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 device must be within the specification.
3.4.6 Tx SSC Slew Rate (20 Gb/s) (Port 2, Lane 1)	12464	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.6 Tx SSC Slew Rate (20.625 Gb/s) (Port 1, Lane 0)	20164	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 device must be within the specification.
3.4.6 Tx SSC Slew Rate (20.625 Gb/s) (Port 1, Lane 0)	10164	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 host must be within the specification.
3.4.6 Tx SSC Slew Rate (20.625 Gb/s) (Port 1, Lane 1)	20264	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 device must be within the specification.
3.4.6 Tx SSC Slew Rate (20.625 Gb/s) (Port 1, Lane 1)	10264	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 host must be within the specification.
3.4.6 Tx SSC Slew Rate (20.625 Gb/s) (Port 2, Lane 0)	20364	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 device must be within the specification.
3.4.6 Tx SSC Slew Rate (20.625 Gb/s) (Port 2, Lane 0)	10364	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 host must be within the specification.
3.4.6 Tx SSC Slew Rate (20.625 Gb/s) (Port 2, Lane 1)	20464	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 device must be within the specification.
3.4.6 Tx SSC Slew Rate (20.625 Gb/s) (Port 2, Lane 1)	10464	The spread spectrum clocking (SSC) slew rate at TP2 of a USB4 host must be within the specification.
3.4.7 Tx Frequency Variation Training (20 Gb/s) (Port 1, Lane 0)	12166	The spread spectrum clocking (SSC) Frequency Variation at TP2 of a USB4 Host must be within the specification.
3.4.7 Tx Frequency Variation Training (20 Gb/s) (Port 1, Lane 0)	22166	The spread spectrum clocking (SSC) Frequency Variation at TP2 of a USB4 device must be within the specification.
3.4.7 Tx Frequency Variation Training (20 Gb/s) (Port 1, Lane 1)	12266	The spread spectrum clocking (SSC) Frequency Variation at TP2 of a USB4 Host must be within the specification.
3.4.7 Tx Frequency Variation Training (20 Gb/s) (Port 1, Lane 1)	22266	The spread spectrum clocking (SSC) Frequency Variation at TP2 of a USB4 device must be within the specification.
3.4.7 Tx Frequency Variation Training (20 Gb/s) (Port 2, Lane 0)	12366	The spread spectrum clocking (SSC) Frequency Variation at TP2 of a USB4 Host must be within the specification.
3.4.7 Tx Frequency Variation Training (20 Gb/s) (Port 2, Lane 0)	22366	The spread spectrum clocking (SSC) Frequency Variation at TP2 of a USB4 device must be within the specification.
3.4.7 Tx Frequency Variation Training (20 Gb/s) (Port 2, Lane 1)	12466	The spread spectrum clocking (SSC) Frequency Variation at TP2 of a USB4 Host must be within the specification.
3.4.7 Tx Frequency Variation Training (20 Gb/s) (Port 2, Lane 1)	22466	The spread spectrum clocking (SSC) Frequency Variation at TP2 of a USB4 device must be within the specification.
3.4.8 Tx Fall Time (20 Gb/s) (Port 1, Lane 0)	22112	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Fall Time (20 Gb/s) (Port 1, Lane 0)	12112	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.8 Tx Fall Time (20 Gb/s) (Port 1, Lane 1)	22212	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Fall Time (20 Gb/s) (Port 1, Lane 1)	12212	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Fall Time (20 Gb/s) (Port 2, Lane 0)	22312	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Fall Time (20 Gb/s) (Port 2, Lane 0)	12312	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Fall Time (20 Gb/s) (Port 2, Lane 1)	22412	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Fall Time (20 Gb/s) (Port 2, Lane 1)	12412	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Fall Time (20.625 Gb/s) (Port 1, Lane 0)	20112	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Fall Time (20.625 Gb/s) (Port 1, Lane 0)	10112	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Fall Time (20.625 Gb/s) (Port 1, Lane 1)	20212	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Fall Time (20.625 Gb/s) (Port 1, Lane 1)	10212	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Fall Time (20.625 Gb/s) (Port 2, Lane 0)	20312	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Fall Time (20.625 Gb/s) (Port 2, Lane 0)	10312	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Fall Time (20.625 Gb/s) (Port 2, Lane 1)	20412	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.8 Tx Fall Time (20.625 Gb/s) (Port 2, Lane 1)	10412	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Rise Time (20 Gb/s) (Port 1, Lane 0)	22111	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Rise Time (20 Gb/s) (Port 1, Lane 0)	12111	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Rise Time (20 Gb/s) (Port 1, Lane 1)	22211	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Rise Time (20 Gb/s) (Port 1, Lane 1)	12211	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Rise Time (20 Gb/s) (Port 2, Lane 0)	22311	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Rise Time (20 Gb/s) (Port 2, Lane 0)	12311	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Rise Time (20 Gb/s) (Port 2, Lane 1)	22411	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Rise Time (20 Gb/s) (Port 2, Lane 1)	12411	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Rise Time (20.625 Gb/s) (Port 1, Lane 0)	20111	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Rise Time (20.625 Gb/s) (Port 1, Lane 0)	10111	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Rise Time (20.625 Gb/s) (Port 1, Lane 1)	20211	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Rise Time (20.625 Gb/s) (Port 1, Lane 1)	10211	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.8 Tx Rise Time (20.625 Gb/s) (Port 2, Lane 0)	20311	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Rise Time (20.625 Gb/s) (Port 2, Lane 0)	10311	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Rise Time (20.625 Gb/s) (Port 2, Lane 1)	20411	The Tx output rise time and fall time at TP2 of a USB4 device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.8 Tx Rise Time (20.625 Gb/s) (Port 2, Lane 1)	10411	The Tx output rise time and fall time at TP2 of a USB4 host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9 Tx Electrical Idle Voltage (20 Gb/s) (Port 1, Lane 0)	22141	The transmitter electrical idle output voltage at TP2 of a USB4 device must be less than maximum limit.
3.4.9 Tx Electrical Idle Voltage (20 Gb/s) (Port 1, Lane 0)	12141	The transmitter electrical idle output voltage at TP2 of a USB4 host must be less than maximum limit.
3.4.9 Tx Electrical Idle Voltage (20 Gb/s) (Port 1, Lane 1)	22241	The transmitter electrical idle output voltage at TP2 of a USB4 device must be less than maximum limit.
3.4.9 Tx Electrical Idle Voltage (20 Gb/s) (Port 1, Lane 1)	12241	The transmitter electrical idle output voltage at TP2 of a USB4 host must be less than maximum limit.
3.4.9 Tx Electrical Idle Voltage (20 Gb/s) (Port 2, Lane 0)	22341	The transmitter electrical idle output voltage at TP2 of a USB4 device must be less than maximum limit.
3.4.9 Tx Electrical Idle Voltage (20 Gb/s) (Port 2, Lane 0)	12341	The transmitter electrical idle output voltage at TP2 of a USB4 host must be less than maximum limit.
3.4.9 Tx Electrical Idle Voltage (20 Gb/s) (Port 2, Lane 1)	22441	The transmitter electrical idle output voltage at TP2 of a USB4 device must be less than maximum limit.
3.4.9 Tx Electrical Idle Voltage (20 Gb/s) (Port 2, Lane 1)	12441	The transmitter electrical idle output voltage at TP2 of a USB4 host must be less than maximum limit.
3.4.9 Tx Electrical Idle Voltage (20.625 Gb/s) (Port 1, Lane 0)	20141	The transmitter electrical idle output voltage at TP2 of a USB4 device must be less than maximum limit.
3.4.9 Tx Electrical Idle Voltage (20.625 Gb/s) (Port 1, Lane 0)	10141	The transmitter electrical idle output voltage at TP2 of a USB4 host must be less than maximum limit.
3.4.9 Tx Electrical Idle Voltage (20.625 Gb/s) (Port 1, Lane 1)	20241	The transmitter electrical idle output voltage at TP2 of a USB4 device must be less than maximum limit.
3.4.9 Tx Electrical Idle Voltage (20.625 Gb/s) (Port 1, Lane 1)	10241	The transmitter electrical idle output voltage at TP2 of a USB4 host must be less than maximum limit.
3.4.9 Tx Electrical Idle Voltage (20.625 Gb/s) (Port 2, Lane 0)	20341	The transmitter electrical idle output voltage at TP2 of a USB4 device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.9 Tx Electrical Idle Voltage (20.625 Gb/s) (Port 2, Lane 0)	10341	The transmitter electrical idle output voltage at TP2 of a USB4 host must be less than maximum limit.
3.4.9 Tx Electrical Idle Voltage (20.625 Gb/s) (Port 2, Lane 1)	20441	The transmitter electrical idle output voltage at TP2 of a USB4 device must be less than maximum limit.
3.4.9 Tx Electrical Idle Voltage (20.625 Gb/s) (Port 2, Lane 1)	10441	The transmitter electrical idle output voltage at TP2 of a USB4 host must be less than maximum limit.
3.5.1 Tx Differential Return Loss (10 Gb/s) (Port 1, Lane 0)	21142	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.1 Tx Differential Return Loss (10 Gb/s) (Port 1, Lane 0)	11142	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.1 Tx Differential Return Loss (10 Gb/s) (Port 1, Lane 1)	21242	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.1 Tx Differential Return Loss (10 Gb/s) (Port 1, Lane 1)	11242	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.1 Tx Differential Return Loss (10 Gb/s) (Port 2, Lane 0)	21342	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.1 Tx Differential Return Loss (10 Gb/s) (Port 2, Lane 0)	11342	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.1 Tx Differential Return Loss (10 Gb/s) (Port 2, Lane 1)	21442	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.1 Tx Differential Return Loss (10 Gb/s) (Port 2, Lane 1)	11442	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.1 Tx Differential Return Loss (10.3125 Gb/s) (Port 1, Lane 0)	2142	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.1 Tx Differential Return Loss (10.3125 Gb/s) (Port 1, Lane 0)	1142	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.1 Tx Differential Return Loss (10.3125 Gb/s) (Port 1, Lane 1)	2242	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.1 Tx Differential Return Loss (10.3125 Gb/s) (Port 1, Lane 1)	1242	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.1 Tx Differential Return Loss (10.3125 Gb/s) (Port 2, Lane 0)	2342	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.1 Tx Differential Return Loss (10.3125 Gb/s) (Port 2, Lane 0)	1342	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.1 Tx Differential Return Loss (10.3125 Gb/s) (Port 2, Lane 1)	2442	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.1 Tx Differential Return Loss (10.3125 Gb/s) (Port 2, Lane 1)	1442	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.1 Tx Differential Return Loss (20 Gb/s) (Port 1, Lane 0)	22142	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.1 Tx Differential Return Loss (20 Gb/s) (Port 1, Lane 0)	12142	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.1 Tx Differential Return Loss (20 Gb/s) (Port 1, Lane 1)	22242	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.1 Tx Differential Return Loss (20 Gb/s) (Port 1, Lane 1)	12242	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.1 Tx Differential Return Loss (20 Gb/s) (Port 2, Lane 0)	22342	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.1 Tx Differential Return Loss (20 Gb/s) (Port 2, Lane 0)	12342	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.1 Tx Differential Return Loss (20 Gb/s) (Port 2, Lane 1)	22442	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.1 Tx Differential Return Loss (20 Gb/s) (Port 2, Lane 1)	12442	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.1 Tx Differential Return Loss (20.625 Gb/s) (Port 1, Lane 0)	20142	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.1 Tx Differential Return Loss (20.625 Gb/s) (Port 1, Lane 0)	10142	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.1 Tx Differential Return Loss (20.625 Gb/s) (Port 1, Lane 1)	20242	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.1 Tx Differential Return Loss (20.625 Gb/s) (Port 1, Lane 1)	10242	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.1 Tx Differential Return Loss (20.625 Gb/s) (Port 2, Lane 0)	20342	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.1 Tx Differential Return Loss (20.625 Gb/s) (Port 2, Lane 0)	10342	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.1 Tx Differential Return Loss (20.625 Gb/s) (Port 2, Lane 1)	20442	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.1 Tx Differential Return Loss (20.625 Gb/s) (Port 2, Lane 1)	10442	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (10 Gb/s) (Port 1, Lane 0)	21143	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (10 Gb/s) (Port 1, Lane 0)	11143	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (10 Gb/s) (Port 1, Lane 1)	21243	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.2 Tx Common Mode Return Loss (10 Gb/s) (Port 1, Lane 1)	11243	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (10 Gb/s) (Port 2, Lane 0)	21343	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (10 Gb/s) (Port 2, Lane 0)	11343	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (10 Gb/s) (Port 2, Lane 1)	21443	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (10 Gb/s) (Port 2, Lane 1)	11443	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (10.3125 Gb/s) (Port 1, Lane 0)	2143	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (10.3125 Gb/s) (Port 1, Lane 0)	1143	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (10.3125 Gb/s) (Port 1, Lane 1)	2243	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (10.3125 Gb/s) (Port 1, Lane 1)	1243	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (10.3125 Gb/s) (Port 2, Lane 0)	2343	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (10.3125 Gb/s) (Port 2, Lane 0)	1343	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (10.3125 Gb/s) (Port 2, Lane 1)	2443	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (10.3125 Gb/s) (Port 2, Lane 1)	1443	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (20 Gb/s) (Port 1, Lane 0)	22143	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (20 Gb/s) (Port 1, Lane 0)	12143	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (20 Gb/s) (Port 1, Lane 1)	22243	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (20 Gb/s) (Port 1, Lane 1)	12243	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (20 Gb/s) (Port 2, Lane 0)	22343	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (20 Gb/s) (Port 2, Lane 0)	12343	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.2 Tx Common Mode Return Loss (20 Gb/s) (Port 2, Lane 1)	22443	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (20 Gb/s) (Port 2, Lane 1)	12443	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (20.625 Gb/s) (Port 1, Lane 0)	20143	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (20.625 Gb/s) (Port 1, Lane 0)	10143	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (20.625 Gb/s) (Port 1, Lane 1)	20243	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (20.625 Gb/s) (Port 1, Lane 1)	10243	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (20.625 Gb/s) (Port 2, Lane 0)	20343	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (20.625 Gb/s) (Port 2, Lane 0)	10343	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (20.625 Gb/s) (Port 2, Lane 1)	20443	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
3.5.2 Tx Common Mode Return Loss (20.625 Gb/s) (Port 2, Lane 1)	10443	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.1 Rx Differential Return Loss (10 Gb/s) (Port 1, Lane 0)	21144	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.1 Rx Differential Return Loss (10 Gb/s) (Port 1, Lane 0)	11144	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.1 Rx Differential Return Loss (10 Gb/s) (Port 1, Lane 1)	21244	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.1 Rx Differential Return Loss (10 Gb/s) (Port 1, Lane 1)	11244	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.1 Rx Differential Return Loss (10 Gb/s) (Port 2, Lane 0)	21344	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.1 Rx Differential Return Loss (10 Gb/s) (Port 2, Lane 0)	11344	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.1 Rx Differential Return Loss (10 Gb/s) (Port 2, Lane 1)	21444	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.1 Rx Differential Return Loss (10 Gb/s) (Port 2, Lane 1)	11444	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.1 Rx Differential Return Loss (10.3125 Gb/s) (Port 1, Lane 0)	2144	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
4.6.1 Rx Differential Return Loss (10.3125 Gb/s) (Port 1, Lane 0)	1144	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.1 Rx Differential Return Loss (10.3125 Gb/s) (Port 1, Lane 1)	2244	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.1 Rx Differential Return Loss (10.3125 Gb/s) (Port 1, Lane 1)	1244	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.1 Rx Differential Return Loss (10.3125 Gb/s) (Port 2, Lane 0)	2344	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.1 Rx Differential Return Loss (10.3125 Gb/s) (Port 2, Lane 0)	1344	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.1 Rx Differential Return Loss (10.3125 Gb/s) (Port 2, Lane 1)	2444	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.1 Rx Differential Return Loss (10.3125 Gb/s) (Port 2, Lane 1)	1444	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.1 Rx Differential Return Loss (20 Gb/s) (Port 1, Lane 0)	22144	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.1 Rx Differential Return Loss (20 Gb/s) (Port 1, Lane 0)	12144	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.1 Rx Differential Return Loss (20 Gb/s) (Port 1, Lane 1)	22244	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.1 Rx Differential Return Loss (20 Gb/s) (Port 1, Lane 1)	12244	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.1 Rx Differential Return Loss (20 Gb/s) (Port 2, Lane 0)	22344	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.1 Rx Differential Return Loss (20 Gb/s) (Port 2, Lane 0)	12344	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.1 Rx Differential Return Loss (20 Gb/s) (Port 2, Lane 1)	22444	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.1 Rx Differential Return Loss (20 Gb/s) (Port 2, Lane 1)	12444	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.1 Rx Differential Return Loss (20.625 Gb/s) (Port 1, Lane 0)	20144	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.1 Rx Differential Return Loss (20.625 Gb/s) (Port 1, Lane 0)	10144	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.1 Rx Differential Return Loss (20.625 Gb/s) (Port 1, Lane 1)	20244	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.1 Rx Differential Return Loss (20.625 Gb/s) (Port 1, Lane 1)	10244	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
4.6.1 Rx Differential Return Loss (20.625 Gb/s) (Port 2, Lane 0)	20344	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.1 Rx Differential Return Loss (20.625 Gb/s) (Port 2, Lane 0)	10344	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.1 Rx Differential Return Loss (20.625 Gb/s) (Port 2, Lane 1)	20444	The Differential Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.1 Rx Differential Return Loss (20.625 Gb/s) (Port 2, Lane 1)	10444	The Differential Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (10 Gb/s) (Port 1, Lane 0)	21145	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (10 Gb/s) (Port 1, Lane 0)	11145	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (10 Gb/s) (Port 1, Lane 1)	21245	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (10 Gb/s) (Port 1, Lane 1)	11245	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (10 Gb/s) (Port 2, Lane 0)	21345	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (10 Gb/s) (Port 2, Lane 0)	11345	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (10 Gb/s) (Port 2, Lane 1)	21445	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (10 Gb/s) (Port 2, Lane 1)	11445	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (10.3125 Gb/s) (Port 1, Lane 0)	2145	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (10.3125 Gb/s) (Port 1, Lane 0)	1145	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (10.3125 Gb/s) (Port 1, Lane 1)	2245	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (10.3125 Gb/s) (Port 1, Lane 1)	1245	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (10.3125 Gb/s) (Port 2, Lane 0)	2345	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (10.3125 Gb/s) (Port 2, Lane 0)	1345	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (10.3125 Gb/s) (Port 2, Lane 1)	2445	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
4.6.2 Rx Common Mode Return Loss (10.3125 Gb/s) (Port 2, Lane 1)	1445	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (20 Gb/s) (Port 1, Lane 0)	22145	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (20 Gb/s) (Port 1, Lane 0)	12145	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (20 Gb/s) (Port 1, Lane 1)	22245	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (20 Gb/s) (Port 1, Lane 1)	12245	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (20 Gb/s) (Port 2, Lane 0)	22345	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (20 Gb/s) (Port 2, Lane 0)	12345	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (20 Gb/s) (Port 2, Lane 1)	22445	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (20 Gb/s) (Port 2, Lane 1)	12445	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (20.625 Gb/s) (Port 1, Lane 0)	20145	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (20.625 Gb/s) (Port 1, Lane 0)	10145	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (20.625 Gb/s) (Port 1, Lane 1)	20245	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (20.625 Gb/s) (Port 1, Lane 1)	10245	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (20.625 Gb/s) (Port 2, Lane 0)	20345	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (20.625 Gb/s) (Port 2, Lane 0)	10345	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (20.625 Gb/s) (Port 2, Lane 1)	20445	The Common Mode Return Loss at TP2 of a USB4 device must be less than maximum limit.
4.6.2 Rx Common Mode Return Loss (20.625 Gb/s) (Port 2, Lane 1)	10445	The Common Mode Return Loss at TP2 of a USB4 host must be less than maximum limit.
5.1.1 SBTX High Voltage Measurement (Port 1)	1101	The SBTX High Voltage Measurement of a USB4 device must be within specification limit.
5.1.2 SBTX Low Voltage Measurement (Port 1)	1102	The SBTX Low Voltage Measurement of a USB4 device must be within specification limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
5.1.3 SBTX Fall Time Measurement (Port 1)	1104	The SBTX Fall Time Measurement of a USB4 device must be within specification limit.
5.1.3 SBTX Rise Time Measurement (Port 1)	1103	The SBTX Rise Time Measurement of a USB4 device must be within specification limit.
5.1.4 SBTX UI Duration Measurement (Port 1)	1105	The SBTX UI Duration Measurement of a USB4 device must be within specification limit.
5.1.5 SBRX High Voltage Detection Measurement (Port 1)	1201	The SBRX High Voltage Detection Measurement of a USB4 device, it should establish link between 2.0V and 3.77V.
5.1.6 SBRX Low Voltage Detection Measurement (Port 1)	1202	The SBRX Low Voltage Detection Measurement of a USB4 device, it should not have link between -0.3V and 0.65V.
E.1.1 Tx SSC Down Spread Rate, Max (10.3125 Gb/s) (Port 1, Lane 0)	2167	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Max (10.3125 Gb/s) (Port 1, Lane 0)	1167	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Max (10.3125 Gb/s) (Port 1, Lane 1)	2267	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Max (10.3125 Gb/s) (Port 1, Lane 1)	1267	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Max (10.3125 Gb/s) (Port 2, Lane 0)	2367	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Max (10.3125 Gb/s) (Port 2, Lane 0)	1367	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Max (10.3125 Gb/s) (Port 2, Lane 1)	2467	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Max (10.3125 Gb/s) (Port 2, Lane 1)	1467	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Max (20.625 Gb/s) (Port 1, Lane 0)	20167	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Max (20.625 Gb/s) (Port 1, Lane 0)	10167	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Max (20.625 Gb/s) (Port 1, Lane 1)	20267	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Max (20.625 Gb/s) (Port 1, Lane 1)	10267	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Max (20.625 Gb/s) (Port 2, Lane 0)	20367	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Max (20.625 Gb/s) (Port 2, Lane 0)	10367	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
E.1.1 Tx SSC Down Spread Rate, Max (20.625 Gb/s) (Port 2, Lane 1)	20467	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Max (20.625 Gb/s) (Port 2, Lane 1)	10467	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Min (10.3125 Gb/s) (Port 1, Lane 0)	2161	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Min (10.3125 Gb/s) (Port 1, Lane 0)	1161	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Min (10.3125 Gb/s) (Port 1, Lane 1)	2261	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Min (10.3125 Gb/s) (Port 1, Lane 1)	1261	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Min (10.3125 Gb/s) (Port 2, Lane 0)	2361	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Min (10.3125 Gb/s) (Port 2, Lane 0)	1361	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Min (10.3125 Gb/s) (Port 2, Lane 1)	2461	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Min (10.3125 Gb/s) (Port 2, Lane 1)	1461	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Min (20.625 Gb/s) (Port 1, Lane 0)	20161	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Min (20.625 Gb/s) (Port 1, Lane 0)	10161	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Min (20.625 Gb/s) (Port 1, Lane 1)	20261	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Min (20.625 Gb/s) (Port 1, Lane 1)	10261	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Min (20.625 Gb/s) (Port 2, Lane 0)	20361	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Min (20.625 Gb/s) (Port 2, Lane 0)	10361	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Min (20.625 Gb/s) (Port 2, Lane 1)	20461	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 device must be within the specification.
E.1.1 Tx SSC Down Spread Rate, Min (20.625 Gb/s) (Port 2, Lane 1)	10461	The spread spectrum clocking (SSC) modulation frequency at TP2 of a USB4 host must be within the specification.
E.1.2 Tx SSC Phase Deviation (10.3125 Gb/s) (Port 1, Lane 0)	2171	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
E.1.2 Tx SSC Phase Deviation (10.3125 Gb/s) (Port 1, Lane 0)	1171	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 host must be within the specification.
E.1.2 Tx SSC Phase Deviation (10.3125 Gb/s) (Port 1, Lane 1)	2271	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 device must be within the specification.
E.1.2 Tx SSC Phase Deviation (10.3125 Gb/s) (Port 1, Lane 1)	1271	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 host must be within the specification.
E.1.2 Tx SSC Phase Deviation (10.3125 Gb/s) (Port 2, Lane 0)	2371	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 device must be within the specification.
E.1.2 Tx SSC Phase Deviation (10.3125 Gb/s) (Port 2, Lane 0)	1371	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 host must be within the specification.
E.1.2 Tx SSC Phase Deviation (10.3125 Gb/s) (Port 2, Lane 1)	2471	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 device must be within the specification.
E.1.2 Tx SSC Phase Deviation (10.3125 Gb/s) (Port 2, Lane 1)	1471	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 host must be within the specification.
E.1.2 Tx SSC Phase Deviation (20.625 Gb/s) (Port 1, Lane 0)	20171	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 device must be within the specification.
E.1.2 Tx SSC Phase Deviation (20.625 Gb/s) (Port 1, Lane 0)	10171	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 host must be within the specification.
E.1.2 Tx SSC Phase Deviation (20.625 Gb/s) (Port 1, Lane 1)	20271	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 device must be within the specification.
E.1.2 Tx SSC Phase Deviation (20.625 Gb/s) (Port 1, Lane 1)	10271	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 host must be within the specification.
E.1.2 Tx SSC Phase Deviation (20.625 Gb/s) (Port 2, Lane 0)	20371	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 device must be within the specification.
E.1.2 Tx SSC Phase Deviation (20.625 Gb/s) (Port 2, Lane 0)	10371	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 host must be within the specification.
E.1.2 Tx SSC Phase Deviation (20.625 Gb/s) (Port 2, Lane 1)	20471	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 device must be within the specification.
E.1.2 Tx SSC Phase Deviation (20.625 Gb/s) (Port 2, Lane 1)	10471	The spread spectrum clocking (SSC) phase jitter at TP2 of a USB4 host must be within the specification.
E.1.3 Tx Minimum Unit Interval, Max (10.3125 Gb/s) (Port 1, Lane 0)	2152	The minimum unit interval at TP2 of a USB4 device must be within the specification.
E.1.3 Tx Minimum Unit Interval, Max (10.3125 Gb/s) (Port 1, Lane 0)	1152	The minimum unit interval at TP2 of a USB4 host must be within the specification.
E.1.3 Tx Minimum Unit Interval, Max (10.3125 Gb/s) (Port 1, Lane 1)	2252	The minimum unit interval at TP2 of a USB4 device must be within the specification.
E.1.3 Tx Minimum Unit Interval, Max (10.3125 Gb/s) (Port 1, Lane 1)	1252	The minimum unit interval at TP2 of a USB4 host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
E.1.3 Tx Minimum Unit Interval, Max (10.3125 Gb/s) (Port 2, Lane 0)	2352	The minimum unit interval at TP2 of a USB4 device must be within the specification.
E.1.3 Tx Minimum Unit Interval, Max (10.3125 Gb/s) (Port 2, Lane 0)	1352	The minimum unit interval at TP2 of a USB4 host must be within the specification.
E.1.3 Tx Minimum Unit Interval, Max (10.3125 Gb/s) (Port 2, Lane 1)	2452	The minimum unit interval at TP2 of a USB4 device must be within the specification.
E.1.3 Tx Minimum Unit Interval, Max (10.3125 Gb/s) (Port 2, Lane 1)	1452	The minimum unit interval at TP2 of a USB4 host must be within the specification.
E.1.3 Tx Minimum Unit Interval, Min (10.3125 Gb/s) (Port 1, Lane 0)	2151	The minimum unit interval at TP2 of a USB4 device must be within the specification.
E.1.3 Tx Minimum Unit Interval, Min (10.3125 Gb/s) (Port 1, Lane 0)	1151	The minimum unit interval at TP2 of a USB4 host must be within the specification.
E.1.3 Tx Minimum Unit Interval, Min (10.3125 Gb/s) (Port 1, Lane 1)	2251	The minimum unit interval at TP2 of a USB4 device must be within the specification.
E.1.3 Tx Minimum Unit Interval, Min (10.3125 Gb/s) (Port 1, Lane 1)	1251	The minimum unit interval at TP2 of a USB4 host must be within the specification.
E.1.3 Tx Minimum Unit Interval, Min (10.3125 Gb/s) (Port 2, Lane 0)	2351	The minimum unit interval at TP2 of a USB4 device must be within the specification.
E.1.3 Tx Minimum Unit Interval, Min (10.3125 Gb/s) (Port 2, Lane 0)	1351	The minimum unit interval at TP2 of a USB4 host must be within the specification.
E.1.3 Tx Minimum Unit Interval, Min (10.3125 Gb/s) (Port 2, Lane 1)	2451	The minimum unit interval at TP2 of a USB4 device must be within the specification.
E.1.3 Tx Minimum Unit Interval, Min (10.3125 Gb/s) (Port 2, Lane 1)	1451	The minimum unit interval at TP2 of a USB4 host must be within the specification.
E.1.4 Tx Minimum Unit Interval, Max (20.625 Gb/s) (Port 1, Lane 0)	20152	The minimum unit interval at TP2 of a USB4 device must be within the specification.
E.1.4 Tx Minimum Unit Interval, Max (20.625 Gb/s) (Port 1, Lane 0)	10152	The minimum unit interval at TP2 of a USB4 host must be within the specification.
E.1.4 Tx Minimum Unit Interval, Max (20.625 Gb/s) (Port 1, Lane 1)	20252	The minimum unit interval at TP2 of a USB4 device must be within the specification.
E.1.4 Tx Minimum Unit Interval, Max (20.625 Gb/s) (Port 1, Lane 1)	10252	The minimum unit interval at TP2 of a USB4 host must be within the specification.
E.1.4 Tx Minimum Unit Interval, Max (20.625 Gb/s) (Port 2, Lane 0)	20352	The minimum unit interval at TP2 of a USB4 device must be within the specification.
E.1.4 Tx Minimum Unit Interval, Max (20.625 Gb/s) (Port 2, Lane 0)	10352	The minimum unit interval at TP2 of a USB4 host must be within the specification.
E.1.4 Tx Minimum Unit Interval, Max (20.625 Gb/s) (Port 2, Lane 1)	20452	The minimum unit interval at TP2 of a USB4 device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
E.1.4 Tx Minimum Unit Interval, Max (20.625 Gb/s) (Port 2, Lane 1)	10452	The minimum unit interval at TP2 of a USB4 host must be within the specification.
E.1.4 Tx Minimum Unit Interval, Min (20.625 Gb/s) (Port 1, Lane 0)	20151	The minimum unit interval at TP2 of a USB4 device must be within the specification.
E.1.4 Tx Minimum Unit Interval, Min (20.625 Gb/s) (Port 1, Lane 0)	10151	The minimum unit interval at TP2 of a USB4 host must be within the specification.
E.1.4 Tx Minimum Unit Interval, Min (20.625 Gb/s) (Port 1, Lane 1)	20251	The minimum unit interval at TP2 of a USB4 device must be within the specification.
E.1.4 Tx Minimum Unit Interval, Min (20.625 Gb/s) (Port 1, Lane 1)	10251	The minimum unit interval at TP2 of a USB4 host must be within the specification.
E.1.4 Tx Minimum Unit Interval, Min (20.625 Gb/s) (Port 2, Lane 0)	20351	The minimum unit interval at TP2 of a USB4 device must be within the specification.
E.1.4 Tx Minimum Unit Interval, Min (20.625 Gb/s) (Port 2, Lane 0)	10351	The minimum unit interval at TP2 of a USB4 host must be within the specification.
E.1.4 Tx Minimum Unit Interval, Min (20.625 Gb/s) (Port 2, Lane 1)	20451	The minimum unit interval at TP2 of a USB4 device must be within the specification.
E.1.4 Tx Minimum Unit Interval, Min (20.625 Gb/s) (Port 2, Lane 1)	10451	The minimum unit interval at TP2 of a USB4 host must be within the specification.
E.1.5 Tx Average Unit Interval, Max (10 Gb/s) (Port 1, Lane 0)	21154	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (10 Gb/s) (Port 1, Lane 0)	11154	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (10 Gb/s) (Port 1, Lane 1)	21254	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (10 Gb/s) (Port 1, Lane 1)	11254	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (10 Gb/s) (Port 2, Lane 0)	21354	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (10 Gb/s) (Port 2, Lane 0)	11354	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (10 Gb/s) (Port 2, Lane 1)	21454	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
E.1.5 Tx Average Unit Interval, Max (10 Gb/s) (Port 2, Lane 1)	11454	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (10.3125 Gb/s) (Port 1, Lane 0)	2154	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (10.3125 Gb/s) (Port 1, Lane 0)	1154	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (10.3125 Gb/s) (Port 1, Lane 1)	2254	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (10.3125 Gb/s) (Port 1, Lane 1)	1254	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (10.3125 Gb/s) (Port 2, Lane 0)	2354	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (10.3125 Gb/s) (Port 2, Lane 0)	1354	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (10.3125 Gb/s) (Port 2, Lane 1)	2454	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (10.3125 Gb/s) (Port 2, Lane 1)	1454	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (20 Gb/s) (Port 1, Lane 0)	22154	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (20 Gb/s) (Port 1, Lane 0)	12154	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (20 Gb/s) (Port 1, Lane 1)	22254	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (20 Gb/s) (Port 1, Lane 1)	12254	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
E.1.5 Tx Average Unit Interval, Max (20 Gb/s) (Port 2, Lane 0)	22354	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (20 Gb/s) (Port 2, Lane 0)	12354	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (20 Gb/s) (Port 2, Lane 1)	22454	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (20 Gb/s) (Port 2, Lane 1)	12454	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (20.625 Gb/s) (Port 1, Lane 0)	20154	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (20.625 Gb/s) (Port 1, Lane 0)	10154	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (20.625 Gb/s) (Port 1, Lane 1)	20254	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (20.625 Gb/s) (Port 1, Lane 1)	10254	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (20.625 Gb/s) (Port 2, Lane 0)	20354	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (20.625 Gb/s) (Port 2, Lane 0)	10354	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (20.625 Gb/s) (Port 2, Lane 1)	20454	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Max (20.625 Gb/s) (Port 2, Lane 1)	10454	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (10 Gb/s) (Port 1, Lane 0)	21153	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
E.1.5 Tx Average Unit Interval, Min (10 Gb/s) (Port 1, Lane 0)	11153	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (10 Gb/s) (Port 1, Lane 1)	21253	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (10 Gb/s) (Port 1, Lane 1)	11253	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (10 Gb/s) (Port 2, Lane 0)	21353	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (10 Gb/s) (Port 2, Lane 0)	11353	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (10 Gb/s) (Port 2, Lane 1)	21453	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (10 Gb/s) (Port 2, Lane 1)	11453	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (10.3125 Gb/s) (Port 1, Lane 0)	2153	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (10.3125 Gb/s) (Port 1, Lane 0)	1153	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (10.3125 Gb/s) (Port 1, Lane 1)	2253	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (10.3125 Gb/s) (Port 1, Lane 1)	1253	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (10.3125 Gb/s) (Port 2, Lane 0)	2353	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (10.3125 Gb/s) (Port 2, Lane 0)	1353	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
E.1.5 Tx Average Unit Interval, Min (10.3125 Gb/s) (Port 2, Lane 1)	2453	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (10.3125 Gb/s) (Port 2, Lane 1)	1453	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (20 Gb/s) (Port 1, Lane 0)	22153	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (20 Gb/s) (Port 1, Lane 0)	12153	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (20 Gb/s) (Port 1, Lane 1)	22253	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (20 Gb/s) (Port 1, Lane 1)	12253	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (20 Gb/s) (Port 2, Lane 0)	22353	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (20 Gb/s) (Port 2, Lane 0)	12353	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (20 Gb/s) (Port 2, Lane 1)	22453	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (20 Gb/s) (Port 2, Lane 1)	12453	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (20.625 Gb/s) (Port 1, Lane 0)	20153	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (20.625 Gb/s) (Port 1, Lane 0)	10153	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (20.625 Gb/s) (Port 1, Lane 1)	20253	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
E.1.5 Tx Average Unit Interval, Min (20.625 Gb/s) (Port 1, Lane 1)	10253	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (20.625 Gb/s) (Port 2, Lane 0)	20353	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (20.625 Gb/s) (Port 2, Lane 0)	10353	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (20.625 Gb/s) (Port 2, Lane 1)	20453	The mean unit interval at TP2 of a USB4 device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
E.1.5 Tx Average Unit Interval, Min (20.625 Gb/s) (Port 2, Lane 1)	10453	The mean unit interval at TP2 of a USB4 host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
G.1 Tx Preset Calibration (10 Gb/s) (Port 1, Lane 0)	11810	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (10 Gb/s) (Port 1, Lane 0)	21810	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (10 Gb/s) (Port 1, Lane 1)	11811	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (10 Gb/s) (Port 1, Lane 1)	21811	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (10 Gb/s) (Port 2, Lane 0)	11812	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (10 Gb/s) (Port 2, Lane 0)	21812	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (10 Gb/s) (Port 2, Lane 1)	11813	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (10 Gb/s) (Port 2, Lane 1)	21813	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (10.3125 Gb/s) (Port 1, Lane 0)	1810	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (10.3125 Gb/s) (Port 1, Lane 0)	2810	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (10.3125 Gb/s) (Port 1, Lane 1)	1811	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (10.3125 Gb/s) (Port 1, Lane 1)	2811	The Preset Calibration is used to find the optimized preset.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
G.1 Tx Preset Calibration (10.3125 Gb/s) (Port 2, Lane 0)	1812	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (10.3125 Gb/s) (Port 2, Lane 0)	2812	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (10.3125 Gb/s) (Port 2, Lane 1)	1813	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (10.3125 Gb/s) (Port 2, Lane 1)	2813	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (20 Gb/s) (Port 1, Lane 0)	12810	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (20 Gb/s) (Port 1, Lane 0)	22810	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (20 Gb/s) (Port 1, Lane 1)	12811	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (20 Gb/s) (Port 1, Lane 1)	22811	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (20 Gb/s) (Port 2, Lane 0)	12812	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (20 Gb/s) (Port 2, Lane 0)	22812	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (20 Gb/s) (Port 2, Lane 1)	12813	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (20 Gb/s) (Port 2, Lane 1)	22813	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (20.625 Gb/s) (Port 1, Lane 0)	10810	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (20.625 Gb/s) (Port 1, Lane 0)	20810	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (20.625 Gb/s) (Port 1, Lane 1)	10811	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (20.625 Gb/s) (Port 1, Lane 1)	20811	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (20.625 Gb/s) (Port 2, Lane 0)	10812	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (20.625 Gb/s) (Port 2, Lane 0)	20812	The Preset Calibration is used to find the optimized preset.
G.1 Tx Preset Calibration (20.625 Gb/s) (Port 2, Lane 1)	10813	The Preset Calibration is used to find the optimized preset.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
G.1 Tx Preset Calibration (20.625 Gb/s) (Port 2, Lane 1)	20813	The Preset Calibration is used to find the optimized preset.
Tx SSC Down Spread Deviation, Max (10 Gb/s) (Port 1, Lane 0)	21163	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Max (10 Gb/s) (Port 1, Lane 0)	11163	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Max (10 Gb/s) (Port 1, Lane 1)	21263	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Max (10 Gb/s) (Port 1, Lane 1)	11263	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Max (10 Gb/s) (Port 2, Lane 0)	21363	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Max (10 Gb/s) (Port 2, Lane 0)	11363	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Max (10 Gb/s) (Port 2, Lane 1)	21463	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Max (10 Gb/s) (Port 2, Lane 1)	11463	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Max (10.3125 Gb/s) (Port 1, Lane 0)	2163	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Max (10.3125 Gb/s) (Port 1, Lane 0)	1163	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Max (10.3125 Gb/s) (Port 1, Lane 1)	2263	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Max (10.3125 Gb/s) (Port 1, Lane 1)	1263	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Max (10.3125 Gb/s) (Port 2, Lane 0)	2363	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Max (10.3125 Gb/s) (Port 2, Lane 0)	1363	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Max (10.3125 Gb/s) (Port 2, Lane 1)	2463	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Max (10.3125 Gb/s) (Port 2, Lane 1)	1463	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Max (20 Gb/s) (Port 1, Lane 0)	22163	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Max (20 Gb/s) (Port 1, Lane 0)	12163	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx SSC Down Spread Deviation, Max (20 Gb/s) (Port 1, Lane 1)	22263	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Max (20 Gb/s) (Port 1, Lane 1)	12263	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Max (20 Gb/s) (Port 2, Lane 0)	22363	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Max (20 Gb/s) (Port 2, Lane 0)	12363	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Max (20 Gb/s) (Port 2, Lane 1)	22463	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Max (20 Gb/s) (Port 2, Lane 1)	12463	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Max (20.625 Gb/s) (Port 1, Lane 0)	20163	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Max (20.625 Gb/s) (Port 1, Lane 0)	10163	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Max (20.625 Gb/s) (Port 1, Lane 1)	20263	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Max (20.625 Gb/s) (Port 1, Lane 1)	10263	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Max (20.625 Gb/s) (Port 2, Lane 0)	20363	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Max (20.625 Gb/s) (Port 2, Lane 0)	10363	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Max (20.625 Gb/s) (Port 2, Lane 1)	20463	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Max (20.625 Gb/s) (Port 2, Lane 1)	10463	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Min (10 Gb/s) (Port 1, Lane 0)	21162	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Min (10 Gb/s) (Port 1, Lane 0)	11162	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Min (10 Gb/s) (Port 1, Lane 1)	21262	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Min (10 Gb/s) (Port 1, Lane 1)	11262	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Min (10 Gb/s) (Port 2, Lane 0)	21362	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx SSC Down Spread Deviation, Min (10 Gb/s) (Port 2, Lane 0)	11362	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Min (10 Gb/s) (Port 2, Lane 1)	21462	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Min (10 Gb/s) (Port 2, Lane 1)	11462	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Min (10.3125 Gb/s) (Port 1, Lane 0)	2162	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Min (10.3125 Gb/s) (Port 1, Lane 0)	1162	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Min (10.3125 Gb/s) (Port 1, Lane 1)	2262	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Min (10.3125 Gb/s) (Port 1, Lane 1)	1262	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Min (10.3125 Gb/s) (Port 2, Lane 0)	2362	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Min (10.3125 Gb/s) (Port 2, Lane 0)	1362	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Min (10.3125 Gb/s) (Port 2, Lane 1)	2462	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Min (10.3125 Gb/s) (Port 2, Lane 1)	1462	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Min (20 Gb/s) (Port 1, Lane 0)	22162	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Min (20 Gb/s) (Port 1, Lane 0)	12162	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Min (20 Gb/s) (Port 1, Lane 1)	22262	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Min (20 Gb/s) (Port 1, Lane 1)	12262	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Min (20 Gb/s) (Port 2, Lane 0)	22362	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Min (20 Gb/s) (Port 2, Lane 0)	12362	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Min (20 Gb/s) (Port 2, Lane 1)	22462	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Min (20 Gb/s) (Port 2, Lane 1)	12462	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx SSC Down Spread Deviation, Min (20.625 Gb/s) (Port 1, Lane 0)	20162	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Min (20.625 Gb/s) (Port 1, Lane 0)	10162	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Min (20.625 Gb/s) (Port 1, Lane 1)	20262	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Min (20.625 Gb/s) (Port 1, Lane 1)	10262	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Min (20.625 Gb/s) (Port 2, Lane 0)	20362	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Min (20.625 Gb/s) (Port 2, Lane 0)	10362	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.
Tx SSC Down Spread Deviation, Min (20.625 Gb/s) (Port 2, Lane 1)	20462	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 device must be within the specification.
Tx SSC Down Spread Deviation, Min (20.625 Gb/s) (Port 2, Lane 1)	10462	The spread spectrum clocking (SSC) modulation deviation at TP2 of a USB4 host must be within the specification.

4 Instruments

The following table shows the instruments used by this application. The name is required by various remote interface methods.

- Instrument Name — The name to use as a parameter in remote interface commands.
- Description — The description of the instrument.

For example, if an application uses an oscilloscope and a pulse generator, then you would expect to see something like this in the table below:

Table 5 Example Instrument Information

Name	Description
scope	The primary oscilloscope.
Pulse	The pulse generator used for Gen 2 tests.

and you would be able to remotely control an instrument using:

```
ARSL syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
arsl -a ipaddress -c "SendScpiCommandCustom 'Command=[scpi
command];Timeout=100;Instrument=pulsegen'"

arsl -a ipaddress -c "SendScpiQueryCustom 'Command=[scpi
query];Timeout=100;Instrument=pulsegen'"


C# syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
SendScpiCommandOptions commandOptions = new SendScpiCommandOptions();
commandOptions.Command = "[scpi command]";
commandOptions.Instrument = "[instrument name]";
commandOptions.Timeout = [timeout];
remoteAte.SendScpiCommand(commandOptions);

SendScpiQueryOptions queryOptions = new SendScpiQueryOptions();
queryOptions.Query = "[scpi query]";
queryOptions.Instrument = "[instrument name]";
```

```
queryOptions.Timeout = [timeout];
remoteAte.SendScpiQuery(queryOptions);
```

Here are the actual instrument names used by this application:

NOTE The file, "InstrumentInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 6 Instrument Names

Instrument Name	Description
Infiniium	the primary oscilloscope
Keysight VNA	The Vector Network Analyzer.
JBERTB	N4903B High Performance Serial BERT
JBERTA	N4903A High Performance Serial BERT

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