

Agilent N4220B Packet Analysis Probe for PCI Express

User's Guide



Agilent Technologies

Notices

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Manual Part Number

N4220-97001

Print History

N4220-97001, June 2004

N4220-97000, 2003

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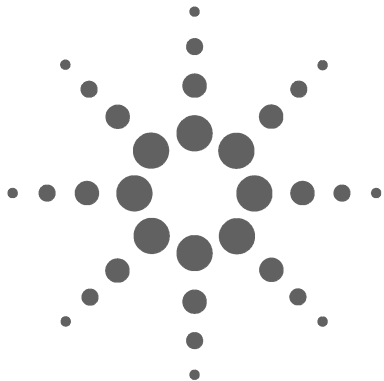
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1 Equipment and Requirements



Equipment Supplied

This section lists equipment supplied with the analysis probe and equipment requirements for using the analysis probe.

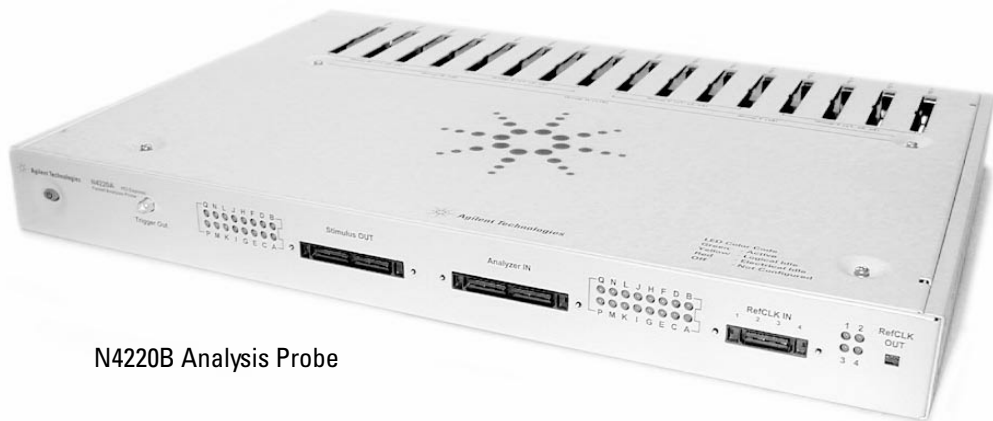
The equipment supplied with the analysis probe is shown in the illustration on the next page. It is listed below:

- Agilent N4220B analysis probe.
- Reference clock cable.
- Logic analyzer configuration files and tool software on CD-ROM.
- This *User's Guide*.
- Brackets and screws for stacking two Agilent N4220B analysis probes.
- Power supply.
- Power cord for the analysis probe.

If the power cord you received is not appropriate for your electrical power outlet type, contact your Agilent Technologies sales and service office. Use only the power cord supplied with the analysis probe.

The cable sets are sold separately. See "Bench Space for the Analysis Probe" on page 16 for a complete list.

See also "To get replacement parts" on page 124.



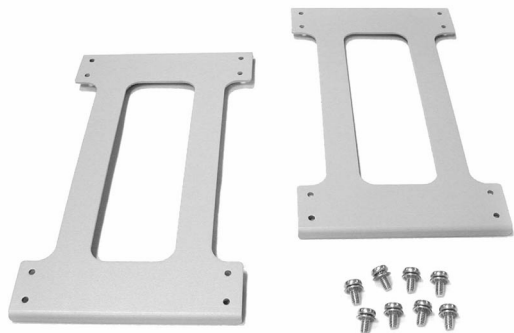
N4220B Analysis Probe



Reference Clock Cable



Power Cord



Brackets and screws



Power Supply

Additional Equipment Required

Logic analysis system

In addition to the items supplied with the analysis probe, you need all of the following items:

- An Agilent 16700- or 16900-series logic analysis system.
- One or more logic analyzer cards. The following Agilent Technologies logic analyzers may be used:
 - 16753A
 - 16754A
 - 16755A
 - 16756A
 - 16950A (in a 16900-series logic analysis system)
- (Optional) Torx T20 screwdriver for stacking two analysis probes.

Cable sets

In addition to the analysis probe, you must have one or more cable sets.

Table 1 Cable set product numbers (sold separately)




Product number	Description
N4221A	Midbus connector cable set using soft touch technology (comes with set of 5 retention modules and loopback board for probe self-test)
	
N4222A	x16 (split) midbus connector cable set using soft touch technology
	
N4223A	x16 slot connector cable set
	

Table 1 Cable set product numbers (sold separately)





Product number	Description
N4224A	x8 slot connector cable set
	
N4225A	x4 slot connector cable set
	
N4227A	x1 slot connector cable set
	

Table 1 Cable set product numbers (sold separately)

Product number	Description
N4228A	x8 (half) midbus connector cable set using soft touch technology (comes with set of 5 retention modules and loopback board for probe self-test)



Bench Space for the Analysis Probe

Take care to allow space for the analysis probe be placed near the target system and the logic analysis system.

Allow at least 12 cm (4.5 in) clearance above the analysis probe for connecting the logic analyzer cables.

Allow at least 5 cm (2 in) clearance on both sides of the analysis probe for proper cooling.

CAUTION

Do not block the airflow holes on the sides of the analysis probe box. Blocked airflow may cause overheating and equipment damage

If you stack two analysis probes, use the supplied brackets to maintain enough clearance for airflow and for the cables. See "Stacking the probes" on page 21.

Position the analysis probe and power supply so that it is not difficult to unplug the power cord.

See "Mechanical Characteristics" on page 129 for the dimensions of the analysis probe.

Device Under Test Electrical Requirements

See the Agilent *PCI Express Logic Analyzer Probing Design Guide* for detailed information on preparing your PCI Express system for measurements.

Reference clock

Each system must provide means of delivering a reference clock (for each PCI Express reference clock domain) for specific cases:

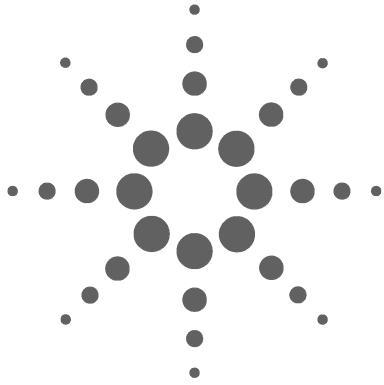
- When an LAI is used with a system that supports Spread Spectrum Clocking (SSC) on the reference clock to all the PCI Express agents and the SSC cannot be disabled
- When testing must be done with SSC enabled because a problem does not manifest with SSC disabled
- If the link frequency is intentionally margin tested outside the standard ± 300 ppm tolerance.
- If any clock domain reference clock operates outside a ± 150 ppm tolerance (note that this is more restrictive than the PCI Express standard of ± 300 ppm, but must be considered).

Note that this clock can be a dedicated clock, in which case appropriate terminators must be provided on the board. Alternately, the signals may be a tap off an existing clock, since the probes are designed to not significantly load the signals.

Midbus probes

To use a midbus probe, you must route signals to a set of pads on the circuit board. See the Agilent *PCI Express Logic Analyzer Probing Design Guide*.

1 Equipment and Requirements



2

Connecting the Analysis Probe



Installing Logic Analyzer Modules

You should install logic analyzer cards into your logic analysis system before you install software. You may need to physically connect the cards together to create multi-card *modules*.

NOTE

The analysis probe can only be used with the Agilent Technologies 16753/54/55/56A and 16950A logic analyzer cards. You may mix different models of logic analyzer cards in your setup.

Refer to the *Installation Guide* for your logic analysis system for instructions on installing the logic analyzer modules.

Deciding how many logic analyzer modules to use

Capturing traffic in one direction on a link requires one module. Capturing traffic in more directions or on more links requires more modules.

Table 2 Number of logic analyzer cards required

Lanes	Groups	Cards required
x1 or x4	1 (one lane, unidirectional)	1 individual card
x1 or x4	2 (one lane, bidirectional)	2 individual cards, or 2 cards connected as one module, or 4 cards connected as one module
x1 or x4	3	3 individual cards
x1 or x4	4	4 individual cards, or 4 cards conneced as two 2-card modules
x8	1 (unidirectional)	2 cards connected as one module
x8	2 (bidirectional)	4 cards connected as two 2-card modules, or 4 cards connected as one module
x16	1 (unidirectional)	4 cards connected as one module

Stacking Analysis Probes

For x16 bidirectional configurations, you need two analysis probes. The two analysis probes may be stacked using the following procedure.

CAUTION

To ensure adequate clearance for ventilation and cable egress, use only the supplied mounting brackets to stack the analysis probes.

Equipment required

- 2 brackets (supplied)
- 8 screws (supplied)
- Torx T20 screwdriver

Stacking the probes

- 1 It is easiest to begin with the top analysis probe. Set it on a small table or a substantial box so that the sides of the analysis probe overhang the edges of the support by 2-5 cm (1-2 inches).



2 Connecting the Analysis Probe

- 2 Install the first bracket using the top set of holes on the analysis probe. The lip of the bracket faces away from the analysis probe.



It is suggested that you install the screws in the following order. Install the 4 screws loosely at first, then tighten them once they are all in place.



- 3 Install the second bracket in the same way.
- 4 Slip the analysis probe with the brackets over the other probe, then secure it with the remaining screws.



Connecting the Analysis Probe to a PCI Express Link

This section describes:

- Connecting the analysis probe to a power source.
- Connecting the analysis probe to the device under test.
- Connecting the logic analyzer to the analysis probe.

To connect the analysis probe to a power source

The analysis probe is shipped from the factory with a power supply and cord appropriate for your country. If the cord you received is not appropriate for your electrical power outlet type, contact your Agilent Technologies sales and service office (see "Service and Repair Information" on page 124).

Position the analysis probe and power supply so that it is not difficult to unplug the power cord.

2 Connecting the Analysis Probe

WARNING

Maintain ground to avoid electrical shock. Use only the power supply and power cord supplied with the analysis probe. Connect the power cord only to a properly grounded electrical power outlet.

- 1 Connect the power cord to the power supply and to a socket outlet.



- 2 Connect the 12V power cord to the back of the analysis probe.



Ensure the power supply plug is completely seated in the power input receptacle.

To turn power ON

- Press the power button on the front of the analysis probe.



The power button is lighted when the switch is ON.

It is best to power on the analysis probe *before* loading a configuration file into the logic analysis system.

You may turn the analysis probe on before or after the logic analysis system is turned on. You may connect and disconnect the cable sets and the logic analyzer pods while the analysis probe and logic analyzer are powered on.

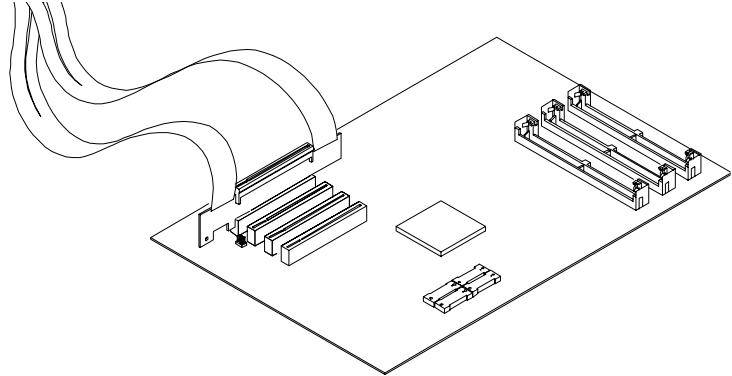
When you turn on the analysis probe, self-test and calibration will take about 45 seconds.

To turn power OFF

- Press the power button on the front of the analysis probe.

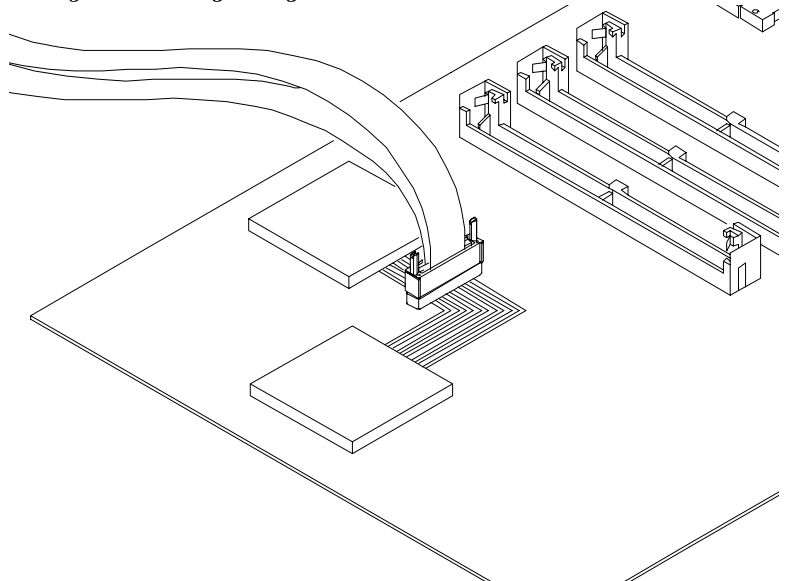
To connect a slot connector cable set to the device under test

- 1 Check that you have the right cable set for the width of the link you wish to probe.
- 2 Plug the cable into the slot.



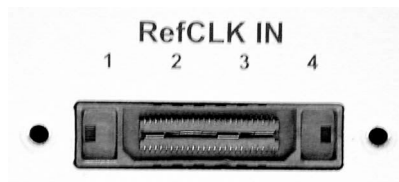
To connect a midbus cable set to the device under test

Information on designing hardware to be used with the midbus cable set may be found in the *Agilent PCI Express Logic Analyzer Probing Design Guide*.

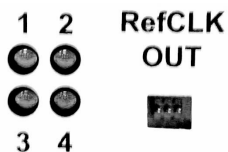


To connect the reference clock

If your measurement setup requires a reference clock signal (see “Reference clock” on page 17 or the Agilent *PCI Express Logic Analyzer Probing Design Guide*), connect the cable to the RefCLK IN connector on the front of the analysis probe.



If you are using several analysis probes, you can daisy-chain the reference clock to the next analysis probe by connecting to the RefCLK OUT connector.

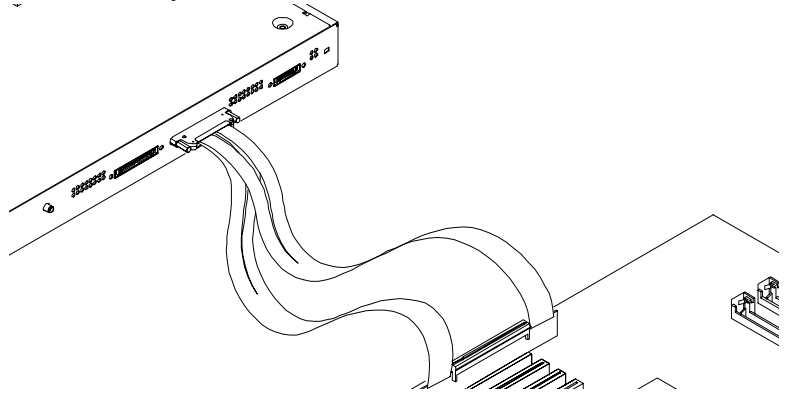


NOTE

Refclk 1 is used for margin testing and is linked to the probe's system clock. If the link under test goes into Squelch and the reference clock is turned off, then you should use RefClk 2, 3 or 4.

To connect the cable set to the analysis probe

Connect the cable to the connector on the analysis probe labeled “Analyzer IN”.

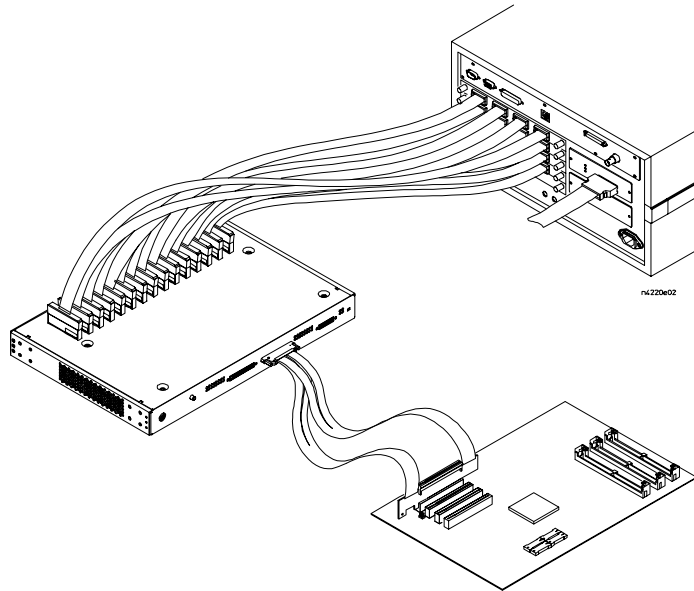


If you wish, you may secure the cable to the analysis probe using the provided screws.

To connect the logic analyzer to the analysis probe

Connectors on the analysis probe

The analysis probe has 16 slots along the top edge labeled "Pod 1" through "Pod 16". These slots are where the logic analyzer pods connect to the analysis probe.



"Groups"

The groups are arbitrarily named W, X, Y and Z. A "group" is all of the pods which are required to probe one direction of a link. In x1 and x4 modes there are 4 groups available, in x8 mode there are two groups available and in x16 mode there is one group.

Connect the pod cables from the logic analyzer cards to the analysis probe according to the following tables.

Table 3 Pod connections and configuration files

Group	Analyzer pod	Probe connector
x1 or x4, 1 group (1 individual card) 16700-series configuration file: N4220A_x1_1 16900-series configuration file: N4220B_x1_1.xml		
W	A1	Pod 1
W	A2	Pod 2
W	A3	Pod 3
W	A4	Pod 4
x1 or x4, 2 groups (2 individual cards) 16700-series configuration file: N4220A_x1_2 16900-series configuration file: N4220B_x1_2.xml		
W	A1	Pod 1
W	A2	Pod 2
W	A3	Pod 3
W	A4	Pod 4
Y	B1	Pod 9
Y	B2	Pod 10
Y	B3	Pod 11
Y	B4	Pod 12
x1 or x4, 3 groups (3 individual cards) 16700-series configuration file: N4220A_x1_3 16900-series configuration file: N4220B_x1_3.xml		
W	A1	Pod 1
W	A2	Pod 2
W	A3	Pod 3
W	A4	Pod 4
X	B1	Pod 5

Table 3 Pod connections and configuration files

Group	Analyzer pod	Probe connector
X	B2	Pod 6
X	B3	Pod 7
X	B4	Pod 8
Y	C1	Pod 9
Y	C2	Pod 10
Y	C3	Pod 11
Y	C4	Pod 12
x1 or x4, 4 groups (4 individual cards) 16700-series configuration file: N4220A_x1_4 16900-series configuration file: N4220B_x1_4.xml		
W	A1	Pod 1
W	A2	Pod 2
W	A3	Pod 3
W	A4	Pod 4
X	B1	Pod 5
X	B2	Pod 6
X	B3	Pod 7
X	B4	Pod 8
Y	C1	Pod 9
Y	C2	Pod 10
Y	C3	Pod 11
Y	C4	Pod 12
Z	D1	Pod 13
Z	D2	Pod 14
Z	D3	Pod 15

Table 3 Pod connections and configuration files

Group	Analyzer pod	Probe connector
Z	D4	Pod 16
x8, 1 group (2-card set, B is master) 16700-series configuration file: N4220A_x8_1 16900-series configuration file: N4220B_x8_1.xml		
W	B1	Pod 1
W	B2	Pod 2
W	B3	Pod 3
W	B4	Pod 4
W	A1	Pod 5
W	A2	Pod 6
W	A3	Pod 7
W	A4	Pod 8
x8, 2 groups (2, 2-card sets: A & B - B is master C & D - D is master) 16700-series configuration file: N4220A_x8_2 16900-series configuration file: N4220B_x8_2.xml		
W	B1	Pod 1
W	B2	Pod 2
W	B3	Pod 3
W	B4	Pod 4
W	A1	Pod 5
W	A2	Pod 6
W	A3	Pod 7
W	A4	Pod 8
Y	D1	Pod 9

Table 3 Pod connections and configuration files

Group	Analyzer pod	Probe connector
Y	D2	Pod 10
Y	D3	Pod 11
Y	D4	Pod 12
Y	C1	Pod 13
Y	C2	Pod 14
Y	C3	Pod 15
Y	C4	Pod 16
x16, 1 group (1, 4-card set: C is master) 16700-series configuration file: N4220A_x16 16900-series configuration file: N4220B_x16.xml		
W	C1	Pod 1
W	C2	Pod 2
W	C3	Pod 3
W	C4	Pod 4
W	D1	Pod 5
W	D2	Pod 6
W	D3	Pod 7
W	D4	Pod 8
W	B1	Pod 9
W	B2	Pod 10
W	B3	Pod 11
W	B4	Pod 12
W	A1	Pod 13
W	A2	Pod 14
W	A3	Pod 15

Table 3 Pod connections and configuration files

Group	Analyzer pod	Probe connector
W	A4	Pod 16

Table 4 Pod connections and configuration files for splitting multi-card logic analyzer modules across several groups

Group	Analyzer pod	Probe connector
x1, 2groups (1, 2-card set: B is master) 16700-series configuration file: N4220A_x1_2M2C 16900-series configuration file: N4220B_x1_2M2C.xml		
W	B1	Pod 1
W	B2	Pod 2
W	A1	Pod 3
W	A2	Pod 4
Y	B3	Pod 9
Y	B4	Pod 10
Y	A3	Pod 11
Y	A4	Pod 12
x1, 2groups (1, 4-card set: C is master) 16700-series configuration file: N4220A_x1_2M4C 16900-series configuration file: N4220B_x1_2M4C.xml		
W	C1	Pod 1
W	C2	Pod 2
W	B1	Pod 3
W	B2	Pod 4
Y	C3	Pod 9
Y	C4	Pod 10
Y	B3	Pod 11

Table 4 Pod connections and configuration files for splitting multi-card logic analyzer modules across several groups

Group	Analyzer pod	Probe connector
Y	B4	Pod 12
x1, 4 groups (2, 2-card sets: A & B - B is master C & D - D is master) 16700-series configuration file: N4220A_x1_4M2C 16900-series configuration file: N4220B_x1_4M2C.xml		
W	B1	Pod 1
W	B2	Pod 2
W	A1	Pod 3
W	A2	Pod 4
X	B3	Pod 5
X	B4	Pod 6
X	A3	Pod 7
X	A4	Pod 8
Y	D1	Pod 9
Y	D2	Pod 10
Y	C1	Pod 11
Y	C2	Pod 12
Z	D3	Pod 13
Z	D4	Pod 14
Z	C3	Pod 15
Z	C4	Pod 16
x8, 2 groups (1, 4-card set: C is master) 16700-series configuration file: N4220A_x8_2M4C 16900-series configuration file: N4220B_x8_2M4C.xml		

Table 4 Pod connections and configuration files for splitting multi-card logic analyzer modules across several groups

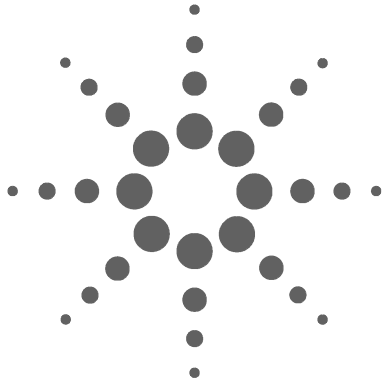
Group	Analyzer pod	Probe connector
W	C1	Pod 1
W	C2	Pod 2
W	B1	Pod 3
W	B2	Pod 4
W	D1	Pod 5
W	D2	Pod 6
W	D3	Pod 7
W	D4	Pod 8
Y	C3	Pod 9
Y	C4	Pod 10
Y	B3	Pod 11
Y	B4	Pod 12
Y	A1	Pod 13
Y	A2	Pod 14
Y	A3	Pod 15
Y	A4	Pod 16
x8, 2 groups (2, 2-card sets: A & B - B is master C & D - D is master) 16700-series configuration file: N4220A_x8_2 16900-series configuration file: N4220B_x8_2.xml		
W	B1	Pod 1
W	B2	Pod 2
W	B3	Pod 3
W	B4	Pod 4

Table 4 Pod connections and configuration files for splitting multi-card logic analyzer modules across several groups

Group	Analyzer pod	Probe connector
W	A1	Pod 5
W	A2	Pod 6
W	A3	Pod 7
W	A4	Pod 8
Y	D1	Pod 9
Y	D2	Pod 10
Y	D3	Pod 11
Y	D4	Pod 12
Y	C1	Pod 13
Y	C2	Pod 14

When you load a configuration file, it will ask which module to use for each group.

2 Connecting the Analysis Probe



3 Configuring a 16700-Series Logic Analysis System

CAUTION

Set up the workspace and the analyzer labels by loading a configuration file. Do not attempt to change the labels associated with the logic analyzer machines using the analyzer's Format tab. To control what data is displayed, use the configuration options in the Decode tool. Do not attempt to set up the workspace by dragging and dropping a Decode tool onto an analyzer; doing this will not set up the required labels.



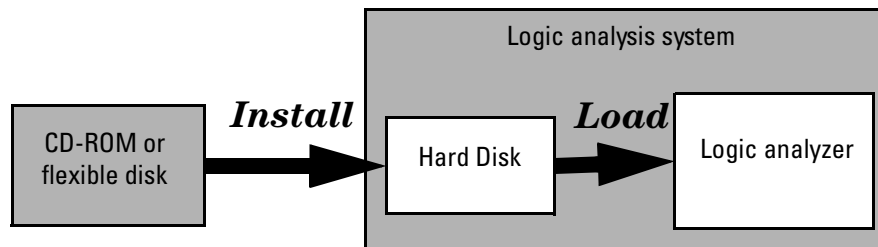
Installing Software

This chapter explains how to install the software you will need for your analysis probe.

Installing and loading

Installing the software will copy the files to the hard disk of your logic analysis system. After the software is installed, you can load configuration files into the logic analyzer modules.

Figure 1 Installing and loading configuration files



What needs to be installed

The following files are installed when you install the analysis software from the CD-ROM:

- Logic analysis system configuration files.
- N4220 PCI Express analysis toolset (automatically loaded with the configuration files; includes the Control tool and the Decode tool).

To install software from CD-ROM

Installing the PCI Express analysis software from the CD-ROM will take just a few minutes. If the software requires an update to the logic analysis system's operating system, installation may take approximately 15 minutes.

- 1 If the CD-ROM drive is external to the logic analysis system, turn on the CD-ROM drive first; then, turn on the logic analysis system.
- 2 Insert the CD-ROM in the drive.
- 3 In the logic analysis system's user interface, select the System Admin icon.
- 4 In the Software Install tab, select the **Install...** button.

Change the media type to **CD-ROM** if necessary.

- 5 Select the **Apply** button.
- 6 From the list of types of packages, double-click or double-select the **AUXILIARY-SW** package.

A list of the auxiliary software packages on the CD-ROM will be displayed.

- 7 Select the "**N4220A PCI Express Analysis Probe Support Package**" package. This package supports both N4220A and N4220B analysis probes.

If you are unsure if this is the correct package, click **Details** for information on what the package contains.

- 8 Select the **Install...** button.

The dialog box will display "Progress: completed successfully" when the installation is complete.

- 9 Select the **Close** button.

The configuration files are stored in
/logic/configs/hp/PCI_Express.

See the instructions printed on the CD-ROM package for a summary of the installation instructions.

See the online help for more information on installing, licensing, and removing software.

Loading Configuration Files

You configure the logic analyzer by loading a configuration file. The information in the configuration file includes:

- Label names and channel assignments for the logic analyzer.
- Workspace configuration including logic analyzer machines, PCI Express tools, and Listing tools.

This tool is not currently supported by the Setup Assistant.

The configuration files support both N4220A and N4220B analysis probes.

To choose a configuration file

Use the configuration file which matches the pod connections. Refer to Table 3 on page 30.

To load a configuration file

- 1 Click on the **File Manager** icon. Use File Manager to ensure that the subdirectory `/logic/configs/hp/PCI_Express` exists.

If the above directory does not exist, you need to install the software. See “To install software from CD-ROM” on page 41.
- 2 Using File Manager, select the configuration file from the `/logic/configs/hp/PCI_Express` directory, then click **Load**. If you have more than one set of logic analyzers installed in your logic analysis system, use the Target field to select the machine you want to load.
- 3 Close File Manager.

What loading a configuration file does

Loading one of these configuration files:

- Sets up the workspace.

There are two workspace tools associated with the PCI Express Packet Analysis Probe, "PCI Express Control" (the Control tool) and "PCI Express Decode" (the Decode tool).

3 Configuring a 16700-Series Logic Analysis System

The Control tool configures the probe by sending commands to the probe via the analyzer cables. The Decode tool decodes packets that are sent from the probe to the analyzer.

- Selects the state (synchronous) sampling mode for each logic analyzer machine and sets up the clock for Master J, both edges, and no qualifiers.

TimingZoom does not provide any useful data, so this feature is turned off.

- Sets each logic analyzer machine's pod threshold voltages for LVCMOS differential signals.
- Labels (maps) buses and signals coming from the analysis probe to the channels of the associated logic analyzer machines.

CAUTION

Set up the workspace and the analyzer labels by loading a configuration file. Do not attempt to change the labels associated with the logic analyzer machines using the analyzer's Format tab. To control what data is displayed, use the configuration options in the Decode tool. Do not attempt to set up the workspace by dragging and dropping a Decode tool onto an analyzer.

Configuring Signal Thresholds

CAUTION

Do not change the signal thresholds.

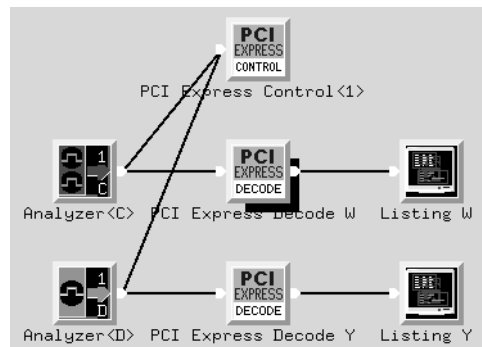
Remember that the logic analyzer is connected to the analysis probe. Changing these parameters will only disrupt the communication between the analysis probe and the logic analyzer—it will not affect how the analysis probe acquires signals from the PCI Express link.

Configuring the Workspace

Typical setup

This is a typical workspace setup. There is a single Control tool on the workspace (just one Control tool is needed for each Agilent N4220B analysis probe used). There are two analyzer machines, each probing one direction. There is a Decode tool and listing for each direction.

There is no display tool attached to the Control tool. The Control tool does not process any analyzer data and does not produce output. The sole reason for drawing lines from the analyzer(s) to the control tool is to inform the Control tool of which analyzer(s) it is using to control the probe.

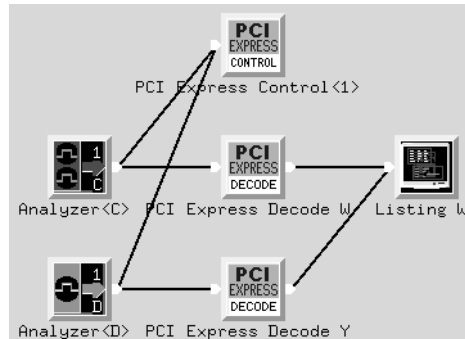


Looking at two directions in a single listing

If you want to view two directions in a single listing you can simply connect two Decode tools to a single listing window. Both Decode tools will produce labels with the same names. The listing window will disambiguate the label names by prefixing with the analyzer name, for example, "Analyzer<A>:Packet Decode". You can rename the analyzers on the workspace to something shorter or more meaningful. The directions in PCI

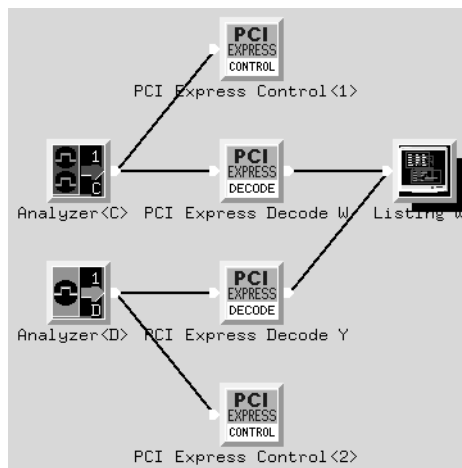
3 Configuring a 16700-Series Logic Analysis System

Express are called "Upstream" and "Downstream". If you rename the analyzers to "Up" and "Down", you will end up with label names such as "Up:Packet Decode" and "Down:Packet Decode".



Looking at two probes

If you are using two analysis probes with a single logic analysis system (this would be the normal use model for x16 bi-directional), you will have two Control tools on the workspace, one for each probe.



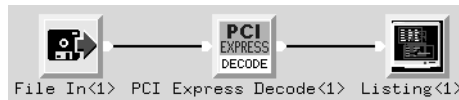
The output usually goes only to a Listing window. It could go to Chart, Distribution or SPA.

3 Configuring a 16700-Series Logic Analysis System

There is little point in sending output to a Waveform window. It's a state trace and the waveforms you see are what is generated by the probe, not what was presented to the probe on the link.

Looking at saved data

If you have saved data using the File Out tool connected to an analyzer machine, use the Decode tool to process the data before displaying it. Since there is no analysis probe in this setup, you do not need a Control tool.

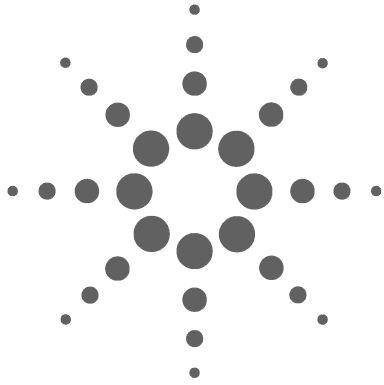


What Next?

Once you have configured the logic analysis system, you can:

- Configure the options for the Control tool.
- Set up a trigger.
- Capture data.
- Configure the options for the Decode tool.
- View the captured data.

These steps are briefly introduced in Chapter 6, “Capturing Data (16700-Series)” and documented in more depth in the online help for the Decode tool.



4 Configuring a 16900-Series Logic Analysis System

CAUTION

Initially set up the tools and the analyzer bus/signal definitions by loading a configuration file. Do not attempt to change the bus/signal names using the **Setup>Bus/Signal** dialog. To control what data is displayed, use the configuration options in the packet decoder tool.



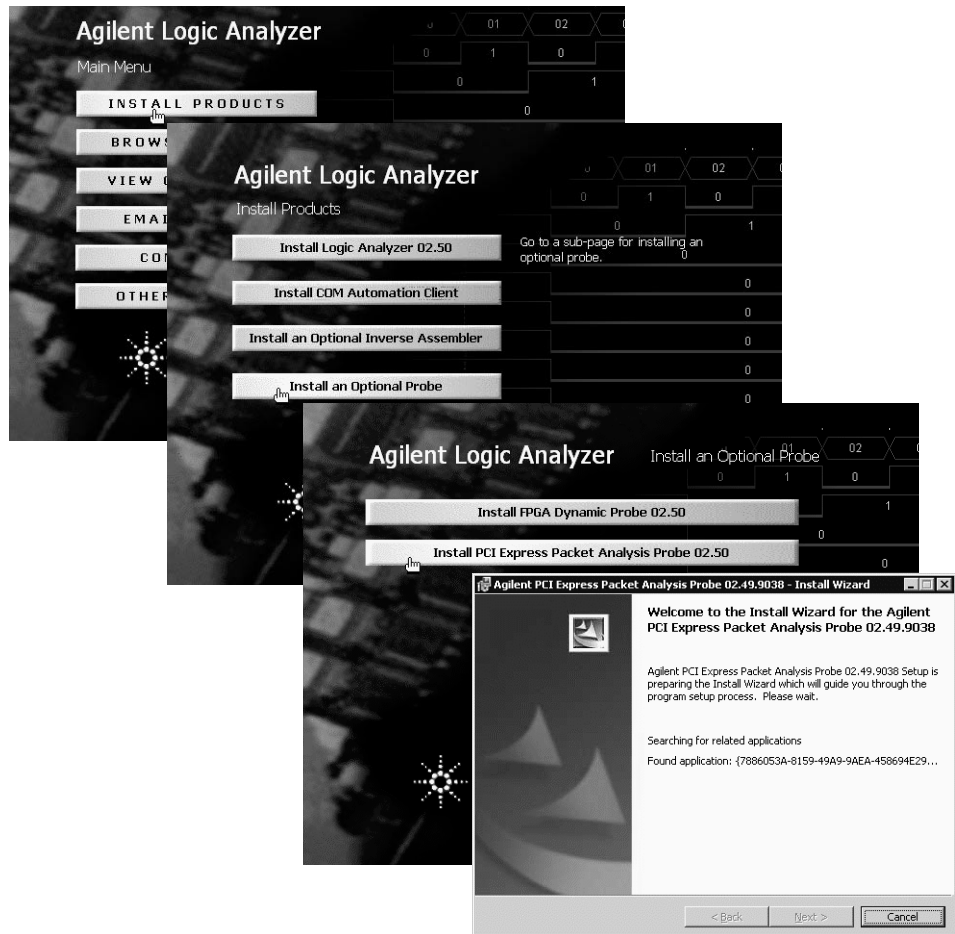
Installing Logic Analyzer Modules

You should install logic analyzer cards into your logic analysis system before you install software. Physically connect the cards together to create a multi-card *module*.

Refer to the Agilent Technologies *16900-Series Logic Analysis Systems Installation Guide* for instructions on installing the logic analyzer modules.

Installing the Software

- 1 Insert the product CD and select **Install Products>Install an Optional Probe>Install PCI Express Packet Analysis Probe**, then follow the instructions which are displayed.



- 2 Follow the instructions on the Entitlement certificate to install the license for the inverse assembler. For more information, go to the Index tab in the online help and click "license."

Loading Configuration Files

You configure the logic analyzer by loading a configuration file. The information in the configuration file includes:

- Signal/bus names and channel assignments for the logic analyzer.
- Tool configuration including logic analyzers, probes, packet decoders, and Listing displays.

To load a provided configuration file:

- 1 Close the logic analyzer window, if it is open.
- 2 Select **Start>Programs>Agilent Logic Analyzer>Agilent N4220B PCI Express Default Configs\N4220B**.
- 3 Click on the configuration you want.

When you click on a configuration file, the logic analyzer software will start and configure itself to use the PCI Express probe.

To load a provided configuration file without restarting the logic analyzer software:

- 1 Select **File>Open....**
- 2 Navigate to the configuration file.
- 3 The location may vary depending on your operating system. For Windows 2000 the default location is:

C:\Documents and Settings\All Users\Documents\Agilent Technologies\Logic Analyzer\Default Configs\Agilent\

4 Select the file and click Open.

To save a configuration file

The provided configuration file is read-only. If you modify the configuration and want to save your work, select **File>Save As...** and save the configuration with a new name.

Configuring Signal Thresholds

CAUTION

Do not change the signal thresholds.

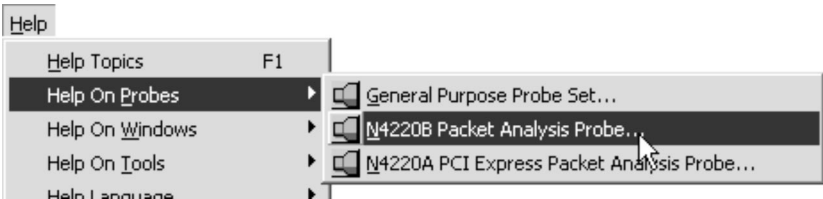
Remember that the logic analyzer is connected to the analysis probe. Changing these parameters will only disrupt the communication between the analysis probe and the logic analyzer—it will not affect how the analysis probe acquires signals from the PCI Express link.

Using the Logic Analyzer

See the online help for information on configuring and using the inverse assembler.

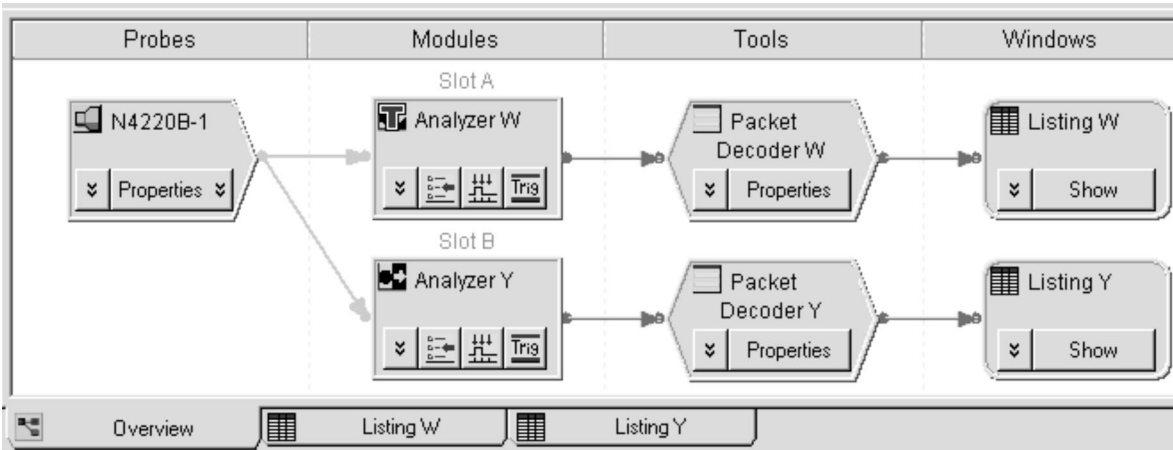
To view online help

When the probe software is installed and licensed, help is added to the Help menu at the top of the logic analyzer window and to the Contents section of the Help window.



To see an overview of how tools are set up

Select the Overview tab at the bottom of the logic analyzer window.

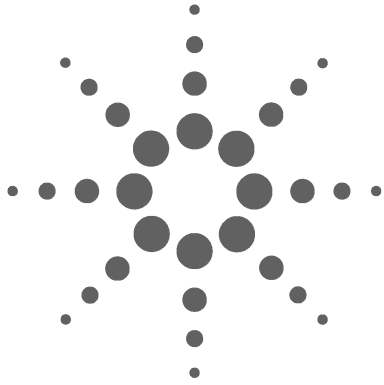


To make a measurement

Here is an overview of the steps to acquire and analyze PCI Express activity. See the online help for more information.

- 1** Configure the probe.
- 2** Set up a trigger.
- 3** Run the logic analyzer.
- 4** View the Listing display.
- 5** Use the Packet Decode tool or the Filter/Colorize tool to hide or highlight information in the Listing display.

4 Configuring a 16900-Series Logic Analysis System



5 Labels for Buses and Signals

CAUTION

Set up the workspace and the analyzer labels by loading a configuration file. Do not attempt to change the labels using the analyzer's Format tab. To control what data is displayed, use the configuration options in the Decode tool. Do not attempt to set up the workspace by dragging and dropping a Decode tool onto an analyzer; doing this will not set up the required labels.



Predefined Label Descriptions

The logic analyzer configuration file automatically sets up labels for most signals. Each label corresponds to a column in the listing display.

Some of the signals include:

8bbyte?	8B data on Lane ?
10bbyte?	10B data on Lane ?
squelch	Bit-per-lane. A value of 1 indicates the lane is squelched (electrical idle)
beacon	A value of 1 indicates that the beacon/dis label contains beacon information. A value of 0 indicates that the beacon/dis label contains disparity error information.
bonded	When 1, all lanes are bonded (de-skewed). Lanes <i>must</i> be bonded before the probe recognizer resources may be used or packets can be decoded.
linkidle	When 1, all lanes are transmitting idle data between packets. This can be used as a store qualification flag for conserving analyzer memory.
#orderedSet	Used to signal that a recognizer resource recognized an ordered set (set when a COMMA character is seen). This label is defined and used only on 16900-series logic analysis systems.
#packet	Used to signal that a recognizer resource recognized a packet.
#grp?	Used to signal that a recognizer resource recognized a packet beginning at a specific lane: <div style="margin-left: 40px;"> <p>#grp0 Packet begins on Lane 0</p> <p>#grp1 Packet begins on Lane 4</p> <p>#grp2 Packet begins on Lane 8</p> <p>#grp3 Packet begins on Lane 12</p> </div>
rd	Running disparity. Bit-per-lane. A value of 1 indicates positive, a value of 0 indicates negative running disparity.

kcode	When 1, an 8B character is a K character otherwise it's a D character. Bit-per-lane.
beacon/dis	When beacon has a value of 1, a 1 in beacon/dis indicates that a lane is beaconing. When beacon has a value of 0, a 1 in beacon/dis indicates a disparity error in the lane. This is a Bit-per-lane label.
8b/10b	When 1, the character has been translated to 8B and the 8bbyte? label contains the data. Otherwise it is a 10B character or invalid character and the 10bbyte? contains the data. Bit-per-lane.
valid	When 1, a character is present. Otherwise data is "blank". Bit-per-lane.

This is the definition of labels in the x1 configurations and is the pattern followed in other configs.

	Pod A4	Pod A3	Pod A2	Pod A1
8bbyte0*****
8bbyte1*****
8bbyte2*****
8bbyte3*****
10bbyte0*****
10bbyte1*****
10bbyte2*****
10bbyte3*****
sqelch	RRRR
beacon	.*.....
bonded	.*.....
linkidle	.*.....
#packet****
rdR.....R.....R.....R.....
kcodeR.....R.....R.....R.....
beacon/disR.....R.....R.....R.....
8b/10bR.....R.....R.....R.....
valid	RRRR

Notice that all the bit-per-lane labels have their bits (channels) indicated as "R" rather than "*". These labels are all reversed left-to-right. In all these labels the right-most bit applies to the right-most lane in the config, which is Lane 0. When presenting data in the Listing window, it is preferable to present Lane 0 as the left-most. This corresponds to the presentation in the PCI Express specifications. The bit-per-byte labels are reversed in

5 Labels for Buses and Signals

the configuration file so they correspond to lane order in the listing. For example, the MSB of the kcode label will correspond to Lane 0 as it is presented in the listing.

Also notice that each of the 10 least significant bits (channels) of each pod appear in two labels each. The probe generates either 8B or 10B data for each lane (independently). The "8b/10b" label indicates which a particular lane contains. If the "8b/10b" label indicates 8B then the labels "8bbyte?", "kcode", and "rd" are valid. Otherwise only the "10bbyte?" label is valid.

Required Labels

In order to decode packets, these labels must be supplied by the analyzer. These labels are all defined in the supplied configuration files.

It is recommended that you always start with one of these configuration files for configuring the analyzers you need for your particular setup.

The labels required for decoding the various lane widths are:

Required x1, x2, x4 Labels

8bbyte0	8 bits
8bbyte1	8 bits
8bbyte2	8 bits
8bbyte3	8 bits
10bbyte0	10 bits
10bbyte1	10 bits
10bbyte2	10 bits
10bbyte3	10 bits
kcode	4 bits
8b/10b	4 bits
squelch	4 bits
beacon/disp	4 bits
beacon	1 bits
bonded	1 bits
linkidle	1 bits
valid	4 bits

Required x8 Labels

8bbyte0	8 bits
8bbyte1	8 bits
8bbyte2	8 bits
8bbyte3	8 bits
8bbyte4	8 bits
8bbyte5	8 bits
8bbyte6	8 bits
8bbyte7	8 bits
10bbyte0	10 bits
10bbyte1	10 bits
10bbyte2	10 bits
10bbyte3	10 bits
10bbyte4	10 bits
10bbyte5	10 bits
10bbyte6	10 bits
10bbyte7	10 bits
kcode	8 bits

5 Labels for Buses and Signals

8b/10b	8 bits
squelch	8 bits
beacon/disp	8 bits
beacon	1 bits
bonded	1 bits
linkidle	1 bits
valid	8 bits

Required x16 Labels

8bbyte0	8 bits
8bbyte1	8 bits
8bbyte2	8 bits
8bbyte3	8 bits
8bbyte4	8 bits
8bbyte5	8 bits
8bbyte6	8 bits
8bbyte7	8 bits
8bbyte8	8 bits
8bbyte9	8 bits
8bbyte10	8 bits
8bbyte11	8 bits
8bbyte12	8 bits
8bbyte13	8 bits
8bbyte14	8 bits
8bbyte15	8 bits
10bbyte0	10 bits
10bbyte1	10 bits
10bbyte2	10 bits
10bbyte3	10 bits
10bbyte4	10 bits
10bbyte5	10 bits
10bbyte6	10 bits
10bbyte7	10 bits
10bbyte8	10 bits
10bbyte9	10 bits
10bbyte10	10 bits
10bbyte11	10 bits
10bbyte12	10 bits
10bbyte13	10 bits
10bbyte14	10 bits
10bbyte15	10 bits
kcode	16 bits
8b/10b	16 bits
squelch	16 bits
beacon/disp	16 bits
beacon	1 bits
bonded	1 bits
linkidle	1 bits
valid	16 bits

To define additional labels

CAUTION

Do not change or delete any of the predefined labels. They are required for packet decode.

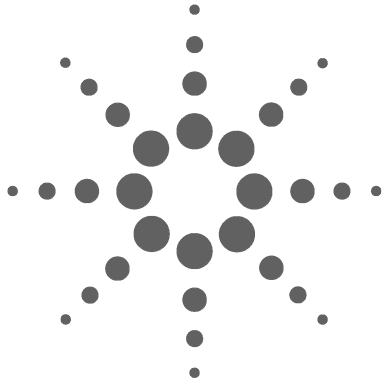
For 16700-series logic analysis systems

- 1 Open the Setup window.
- 2 Click the **Format** tab.
- 3 Click a label and select **Insert before...** or **Insert after...**
- 4 Click the signals under the appropriate pod, then select which bits to include in the label.

For 16900-series logic analysis systems

- 1 From the menu bar, select **Setup>Bus/Signal**.
- 2 Select **Add Bus/Signal** to add a new bus or signal.
- 3 The new bus/signal will appear with a system generated default name. Rename the new bus/signal if desired.

5 Labels for Buses and Signals



6 Capturing Data (16700-Series)

This chapter shows you how to set up logic analyzer triggers on an Agilent 16700-series logic analysis system to capture just the data you want.

The normal steps in using the logic analyzer are:

- 1 Configure the logic analyzer.
- 2 Configure the measurement using the Control tool.
- 3 Set up the trigger, and run the measurement.
- 4 Display the captured data.

The logic analyzer is configured, and labels are created (formatted) for the logic analysis channels when configuration files are loaded (see "Loading Configuration Files" on page 38).

NOTE

Note: The screens you see may be slightly different from what you see in this manual, depending on the version of your logic analyzer system software.

See Also

For instructions on capturing data using a 16900-series logic analysis system, see the online help.

This chapter describes setting up logic analyzer triggers. See "Displaying Captured Data (16700-Series)" on page 95 for information on displaying captured data.



Analysis Modes

This page discusses modes for the logic analyzer.

See page 68 for information on modes for the analysis probe.

State and Timing Modes

The Agilent N4220B Packet Analysis Probe for PCI Express is designed to be used only in state mode.

When to use the Sampling tab

You may safely use the Sampling tab of the logic analyzer's Setup and Trigger window to change:

- Trigger position (start/center/end)
- Sampling positions (after deskewing, to “fine-tune” the results if necessary)
- Acquisition speed/depth

Many of the settings are set by the configuration files and should not be modified. *Do not* use the Sampling tab to change:

- Analyzer mode (state/timing/eye scan)
- Clock setup

Control Tool Overview

The control tool is used for configuring the Agilent N4220B Packet Analysis Probe for PCI Express. It configures the probe by sending commands over the logic analyzer cables.

NOTE

The analyzer pods must be correctly connected to the probe and the probe must be powered on.

To start the Control tool

- 1 Display the Workspace window.
- 2 Loading one of the provided configuration files places a Control tool on the workspace.
- 3 Open the Control tool.

Buttons on the bottom of all tabs

Find Probe

Sends out commands through all analyzer modules connected to the control tool on the workspace to find analysis probe(s). This is required only when the probe was not powered on or analyzer pods were not connected when the configuration file was loaded.

Re-send Probe Setup

Send all configuration information from the control tool to the probe. This is required only when the probe was not powered on or analyzer pods were not connected when the configuration file was loaded. It could also be used if for any reason you suspect the probe may not be configured correctly.

Close

Close the control tool dialog. The same thing can be done with File->Close. This does not remove the tool from the workspace.

Setting the Analysis Probe Mode

Use the Acquisition area of Setup tab in the Control tool to set the operating mode of the analysis probe.

Analysis

In this mode you can acquire PCI Express activity from the link under test. Most of the graphical elements on the Setup tab which control the probe configuration are available only in Analysis mode. Also known as “normal mode.”

Pod ID

In Pod ID mode the probe places a pattern on each pod that identifies the location. After selecting Pod ID mode, open the Analyzer Format tab, then select "Pod Assignment...". For each pod in the analysis module there will be activity indicators. The "activity" on each pod will be a binary value that corresponds to the analysis probe pod number (1 .. 16).

De-Skew

In De-Skew mode, continuous activity is placed on all channels of all pods. The purpose of this activity is to provide a test basis for the analyzers Eye Finder feature. After selecting De-Skew mode, open the Analyzer Format tab, then select "Pod Assignment..." and verify that there is activity on each channel of each pod. Then open the Analyzer Sampling tab and select "Sampling Positions...", this will open the Eye Finder window, you can select "Run Eye Finder" to have the analyzer automatically measure and set the sampling position for each channel.

BIST

Built-In Self Test mode. Use this mode only if instructed to do so by Agilent Technologies.

Configuring the Analysis Probe for a Particular Link

Use the Setup tab in the Control tool to configure the analysis probe for the link you are probing.

Link Width

Select the number of lanes in the link you are probing. Of course, not all link widths are available for all probing accessories. For example, if you are using the N4227A x1 cable set, only the x1 width will be available.

The N4220B packet analysis probe was designed for manual setup of lane width. It was not designed to automatically sense the training sequence and program itself according to the sensed lane width. This was a conscious design decision to avoid locking into a potential broken training sequence that could jeopardize the entire debug effort.

To troubleshoot a target whose lane width is not clear:

- 1 Place the analysis probe in x16 mode.
- 2 Observe the end of the training sequence. Determine the lowest lane width that the target negotiated down to.
- 3 Based on what you see in the training sequence, load the configuration file appropriate for the lane width.

Query Probe Cable

The control tool determines which probe cable is connected to the probe by sending a query to the probe. The probe itself is able to detect if there is a probe cable attached and which probe cable it is. (There is no option for the user setting the probe cable type; the cable type must be detected by the probe and must be queried by the control tool.)

If you load a configuration that includes the Control tool, and the probe is powered on when the configuration is loaded, and the analyzer pods are correctly connected to the probe, and the probe cable also is correctly connected to the probe, the Control

tool will detect the cable type when it loads a configuration file, even if the cable type is different from the cable type that was connected when the configuration file was created.

You should only need to use the "Query Probe Cable" button if you change the cable after the configuration has been loaded, or if there was no probe cable attached when the configuration was loaded.

Physical Group

The icons in the Physical Group change depending on the type of cable that is connected. The default icons represent the outline of a mid-bus connector. If one of the slot connector cable sets is present, the icon changes to a representation of a slot connector.

The letters W, X, Y and Z in the Physical Group icons refer to the groups of pods identified by the same letters with a graphic on the top of the analysis probe, adjacent to the slots for the 16 pods.

With the mid-bus connector, up to four groups are available, depending on lane width. For example in x1, x2, and x4 link widths, there are four groups. The top group W is used when an x16 link is negotiated to x1, x2 or x4. Two groups are available for x8 links negotiated to x1, x2 or x4, one splits the mid-bus connector horizontally, the other vertically. Finally, the connector can be split into 4, allowing two complete x1, x2 or x4 links to be probed.

If you hover a mouse over one of these icons, a flyout (help bubble) will indicate its current usage, based on Link Width.

Select the Physical Group appropriate for your link and probing.

Data Mode

This option refers to how data is sent from the probe to the analyzer pods. Data on the physical PCI Express link is always 10B.

8B This is the "normal mode", the probe must be in 8B mode to use the triggering features in the Events Tab or to decode packets with the decode tool.

10B This mode is for low-level hardware debug. The 10B data is sent from the probe to the analyzer exactly as it is seen on the link. If characters on the link are scrambled, they will be scrambled in the trace listing.

Scramble

These options inform the probe if the 10B characters on the link are scrambled or not. Scrambling enabled is the default in PCI Express, but can be disabled on a link by negotiation.

Enable 1.0 Scrambling on the link is enabled, and is implemented according to rev. 1.0 of the PCI Express specification. If the probe is in 8B mode, it will de-scramble codes before sending them to the analyzer pods. (No effect in 10B mode.)

Enable 1.0a Scrambling on the link is enabled, and is implemented according to rev. 1.0a of the PCI Express specification. If the probe is in 8B mode it will de-scramble codes before sending them to the analyzer pods. (No effect in 10B mode.)

Disable Scrambling on the link is disabled, if the probe is in 8B mode it will NOT de-scramble codes before sending them to the analyzer pods. (No effect in 10B mode.)

Analyzer Boxes

There are up to four boxes below the "Query Probe Cable", the number is determined by the physical group selected. If you select a group that treats all the lanes probed with a cable as a single direction of a link, there will be one box. If select a group that can probe two directions, there will be two boxes. For four directions there will be four boxes.

Starting with one of the standard configuration files at
`/logic/configs/hp/PCI_Express`

is the recommended way for configuring all the analyzers you need for your particular setup.

No Analyzer The name of the analyzer associated with the Analyzer Box is in the upper left corner of the box. If you see the text "No Analyzer" rather than an actual analyzer name, it indicates that either the wrong configuration was loaded, the pods for that analyzer are not correctly connected, or the probe is not powered on.

Probe Pods Icon Below the analyzer name is an icon that indicates which of the 16 slots in the top of the analysis probe are assigned to this analyzer. Ensure that the analyzer pods are correctly connected.

Physical Group Icon Beside the Probe Pods Icon is a Physical Group Icon which has the same shape as the icon selected in the Physical Group box above. This version of the icon will color green the portion of the physical group that this analyzer is probing.

Set All Lanes Use this menu to set all of the lanes in the group to default locations on the mid-bus connector. The letters A..Q correspond to the letters on the front of the N4220B probe and the letters designating the probe points on the mid-bus connector. The LED corresponding to that position on the front of the N4220B probe should be green, indicating that the lane is active.

MUX Configuration If the choices available under "Set All Lanes" do not match the routing of lanes to the mid-bus connector on your link, set each lane individually.

Choosing a Ref Clock Source other than "Internal" will reduce the available choices of probe points.

Choosing a probe point which you had already selected for another lane will change that other lane to "n/c" (not connected).

Ref Clock Source By default the internal reference clock is used. If you want to use an external 100 MHz reference clock, connect one of the cables from the analysis probe's RefCLK IN connector to your reference clock and select the clock from this drop-down menu. You may use a different reference clock for each direction being probed.

Invert data on these lanes The PCI Express spec allows data on lanes to be inverted. Select the button under the lane number to instruct the probe to treat that lane as inverted.

Query Lane Inversion The probe can detect lane inversion if it sees training sequences. Selecting the "Query Lane Inversion" will cause the "Invert data" buttons to indicate the probes view of which lanes are inverted. You can override the probes view by selecting/de-selecting buttons manually. Your manual choices override what the probe may think it saw in training sequences.

Use this button if your decoded data does not look correct (such as bad CRCs reported even though the data should be correct). This will help ensure the probe sees the correct lane polarity.

Configuring Analysis Probe Outputs

Use the Setup tab in the Control tool to configure the analysis probe outputs.

Ref Clock Out

A buffered version of the clock received on the RefCLK IN cable. This can be used for "daisy-chaining" a single reference clock to multiple analysis probes. The buffered clock is available on the RefCLK OUT connector on the front of the analysis probe.

Stimulus Out

These options enable/disable activity on the Stimulus Out connector on the front of the analysis probe. This stimulus can be looped back to the Analyzer In connector with the N4221A midbus compression cable.

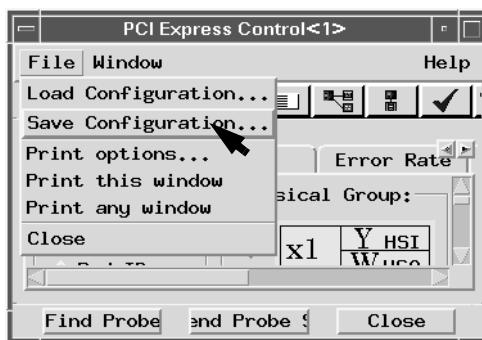
If the Acquisition mode is "Analysis", example PCI Express activity with Training Sequences, Skip Ordered-sets, Data Link Layer Packets and Transaction Layer Packets is output.

If the Acquisition mode is "SERT", the PCI Express Test Instrument Compliance Pattern is output.

To save settings and Eye Finder data

To save Control tool settings

Save a configuration using the File menu of any tool in the workspace.



The configuration file will include any changes you have made from the supplied configuration file, including:

- Changes to the workspace.
- Changes to labels in logic analyzer machine or in any of the display tools.
- Changes to settings in the Probe Control Tool.

Setting Up Logic Analyzer Triggers

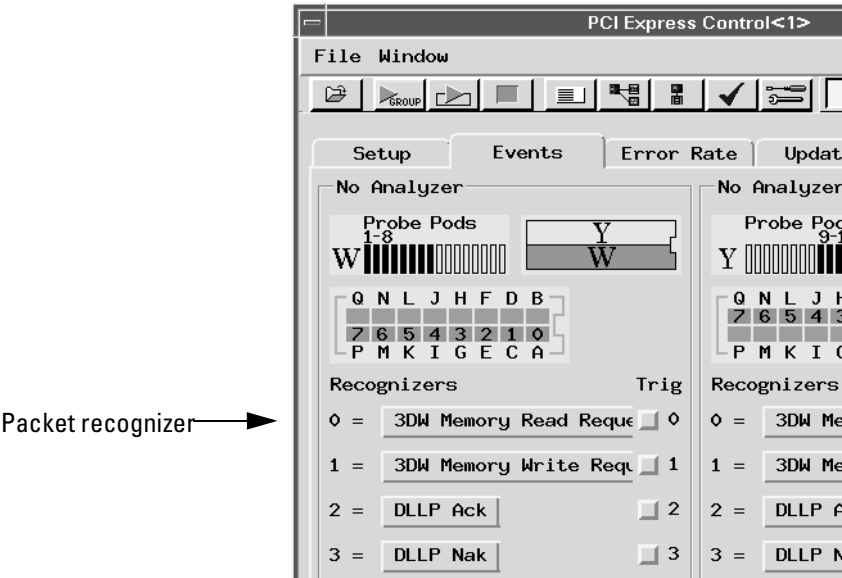
In most cases, you will want to trigger the logic analyzer on patterns on PCI Express packets, rather than on particular values of a label.

The analysis probe has dedicated, hardware-based packet triggering built in. The probe contains pattern recognizers that can be programmed to recognize PCI Express packets.

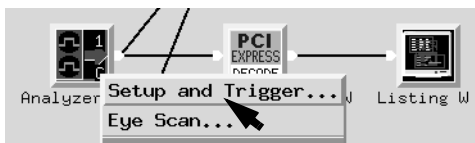
Depending on configuration, these sets of pattern recognizers will be assigned to separate analyzers or to the valid start positions for packets (Lanes 0, 4, 8 or 12).

To set up logic analyzer triggers (general procedure)

- 1 Use the Events tab of the Control tool to set up a packet recognizer.



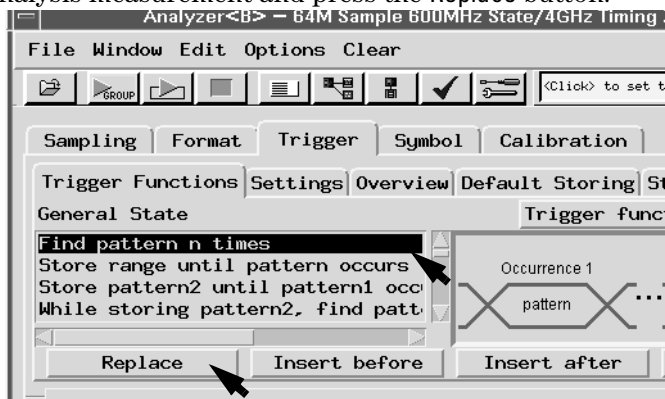
- 2 Open the logic analyzer's Setup window.



- 3 Select the Trigger tab.

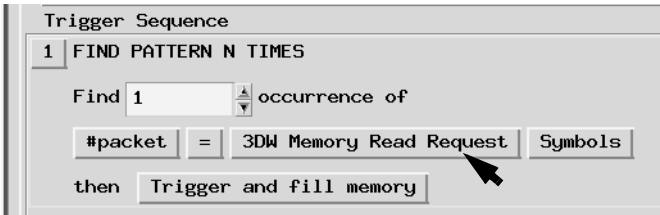


- 4 Select the trigger function that will be used in the logic analysis measurement and press the Replace button.

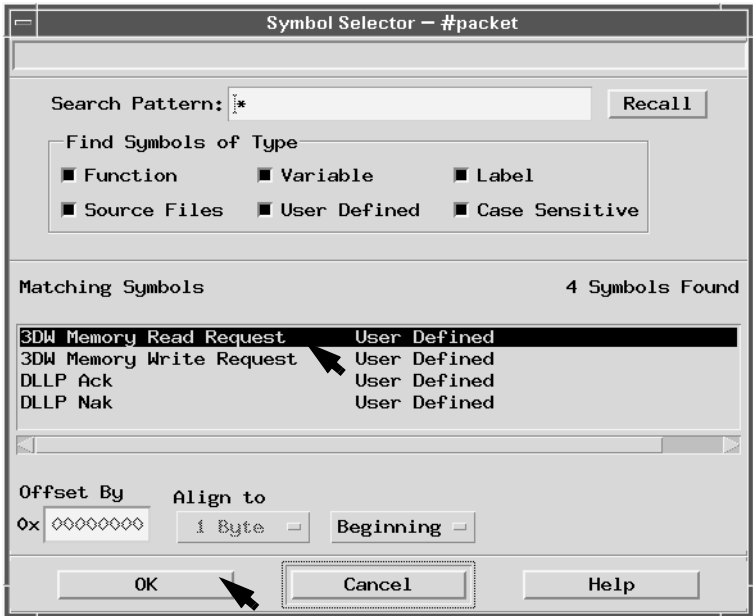


5 Select the packet recognizer which you defined in step 1.

Click to select the packet recognizer



The packet recognizers are listed in the Symbol Selector dialog



6 Define any other packets, patterns, ranges, and other resources that will be used in the logic analysis measurement.

7 Run the measurement.



Refer to the Agilent 16700-series logic analysis system's on-line help for general information on setting up triggers.

How packet triggering works

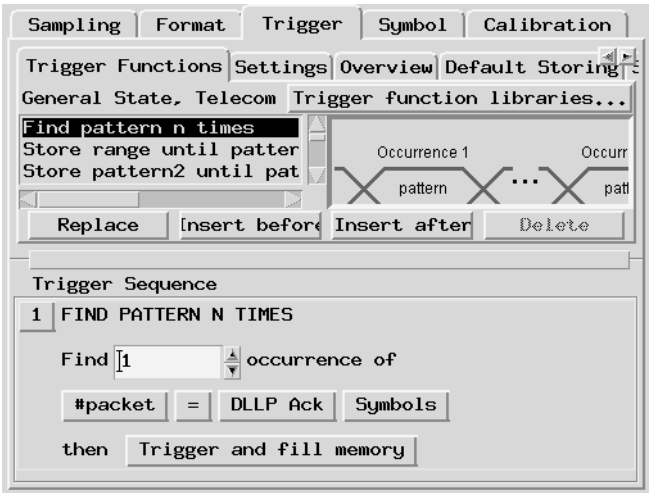
The analysis probe has dedicated packet triggering built in. The probe contains pattern recognizers (four for each direction of traffic) that can be programmed to recognize PCI Express packets. After resolving the “start of packet” (with PCI Express, this is not always lane 0) and deskewing, these recognizers look for matches to fields within the packet header and data payload of up to 24 bytes. The analysis probe will then send a signal back to the logic analyzer, which can use this signal in a trigger, using the full triggering resources of the analyzer (including counters, timers, sequences, and multi-way branching).

When a recognizer “fires,” it will set one of the following labels. The analyzer can trigger on a packet simply by setting up a pattern trigger using these labels:

- #packet** A packet occurred beginning on one of the legal lanes. This label is available in all configuration files.
- #orderedSet** An ordered set occurred. This label is available in all configuration files.
- #grp0** A packet occurred beginning on Lane 0. This label is available in x8 and x16 configurations.
- #grp1** A packet occurred beginning on Lane 4. This label is available in x8 and x16 configurations.
- #grp2** A packet occurred beginning on Lane 8. This label is available only in x16 configurations.
- #grp3** A packet occurred beginning on Lane 12. This label is available only in x16 configurations.

There are symbols defined for each of the above labels corresponding to the names of the events set up in the Events tab of the Control tool.

An example trigger:



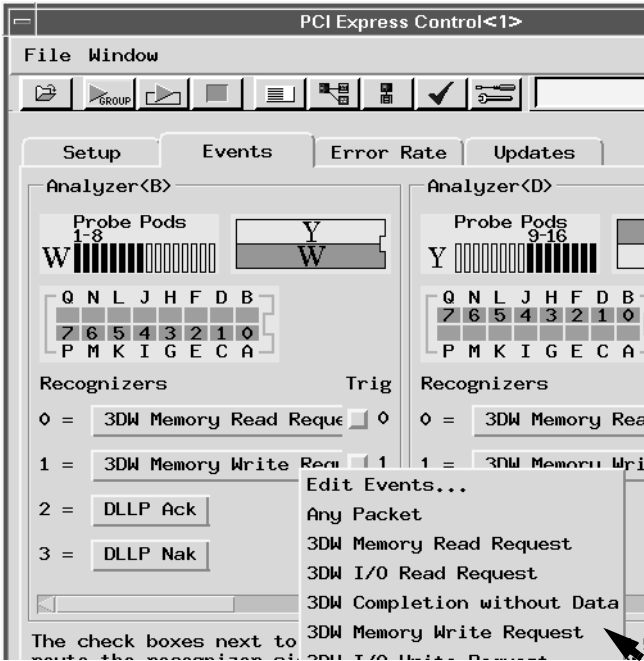
To set up a packet recognizer

Set up the recognizers using the Events tab of the Control tool.

NOTE

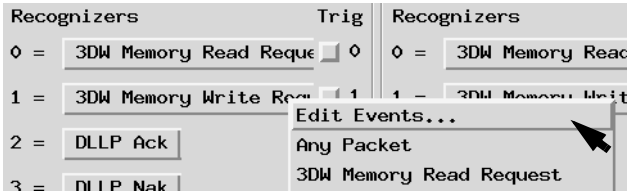
Packet recognizers can be used both for triggering and for searching.

- 1 Open the Control tool and select the Events tab.
- 2 Choose one of the pre-defined packets from the drop-down list of one of the recognizers.

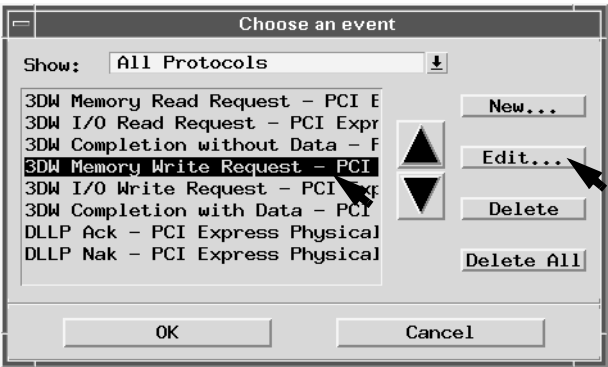


If you want the recognizer to fire on *any* packet of the selected type, you're done.

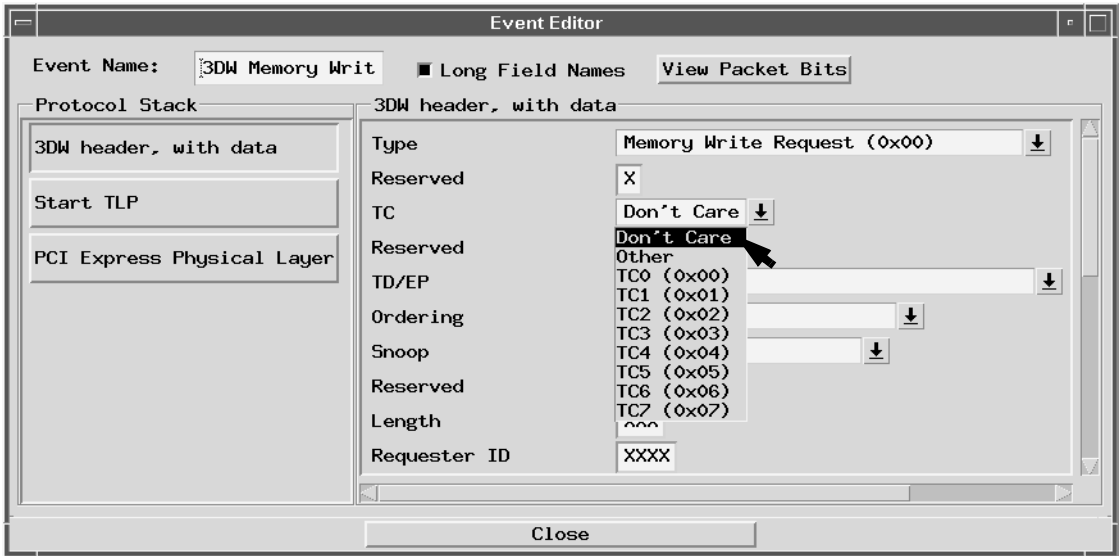
- 3 You can restrict the recognizer to fire only when certain fields of the packet have specific values, or define entirely new events, by selecting Edit Events....



4 Choose the event to edit, or create a new event.



5 Use the Event Editor to define the event.



6 (optional) Save the events in an events file. (See “Events files” on page 85.)

When you load a configuration file, all previously defined PCI Express events are deleted, and any events that are present in the configuration file are loaded. Saving the events in an events file allows you to use them in another configuration or share them with another user

Analyzers in the Events tab

There will be a recognizer box per analyzer as there was an analyzer box per analyzer in the setup tab. The name of the analyzer will appear in the upper left corner of the recognizer box. And, again, "No Analyzer" indicates an incorrect/incomplete setup for the usual reasons.

Recognizers

The four buttons under the "Recognizers" heading each behave the same. When you select a button you get a drop down menu with the entries

```
Edit Events...
Any Packet
(user defined events)
```

Edit Events...

This will pop up the Event Chooser, which is a list (initially empty) of all events that have been defined.

New... Define a new event.

Edit... Edit the selected event.

Delete Delete the selected event.

OK Assign the selected event to the current recognizer.

Cancel Exit the Event Chooser without assigning an event.

Event Editor

The "New..." and "Edit..." buttons will pop up the Event Editor.

The Event Name in the upper left corner defaults to "Event #1", "Event #2", etc. Edit that name to describe the event you are defining, that event name will show up in the drop down menu and as symbols for trigger labels in the analyzer.

Protocol Stack

Used for navigating through the event you are defining.

Edit Area

The edit area to the right of the Protocol Stack is used for selecting the values you are looking for in the various fields of the packet.

The top level always begins:

Special Character	Don't Care	Symbols
	Other	
	Start DLLP	
	Start TLP	

These recognizers work only with packets, so you should select either "Start DLLP" or "Start TLP". After you select the packet type, fields appropriate to that packet type will appear. You must define the packet from the beginning, appropriate fields continue to appear as you define the packet.

Values for specific fields are limited to 0, 1 or "don't care" (X). There is no way to specify a range of values for a field other than by the use of "don't care" bits.

View Packet Bits

At any point while you are defining a packet event, you can select the "View Packet Bits" to see a bit map of the pattern that will be programmed into the recognizer.

Close

Finish editing an event. This does not assign the event to a recognizer. That assignment is made by the "OK" button in the Event Chooser.

Trig

The buttons under the "Trig" heading indicate that when the given event occurs, a trigger signal should also occur on the "Trigger Out" connector on the front of the analysis probe.

Any Packet

The default, "don't care", packet. This will recognize any packet.

Events files

The events created in the Event Editor can be saved/restored in an ASCII (text) file.

NOTE

This events file can be loaded on another 16700-series logic analysis system configured with a PCI Express Control tool.

On the menu bar of the control tool under the File drop-down menu there are three entries related to events files:

- Import Events...
- Export Events...
- View Events in File...

Each menu item pops up a file browser that lets you select the file the action applies to. The actions:

Import Events

Read an events file and APPEND the events in the file to the events already defined in the Event Chooser.

Export Events

Writes ALL the events currently defined in the Event Chooser to the selected file.

View Events in File

Pops up a new window containing all the names of all the events in the selected events file. You can pop up multiple windows for viewing multiple files concurrently by selecting this option multiple times (each selection pops up one window).

Usage Hints

Format of events files. The events file is entirely ASCII (text). Since the 167XX is a Unix system, text lines are expected to end with just a newline ("\n") character. On Microsoft Windows systems, lines in text files end with carriage return ("\r") and linefeed ("\n"). Many utilities used for moving ASCII (text) files between Unix and Microsoft Windows systems take care of inserting/removing carriage return characters as appropriate. Be aware of this issue when moving files between systems—a file that contains carriage return characters will not be viewable or importable on 167XX logic analysis systems.

Importing and exporting event files. Events, as defined in the events file, are independent of analyzer configurations, label definitions, etc.

NOTE

You can create events with one system configuration, export an events file and then import that events file in another configuration.

Events are known within the logic analysis system by an internal ID. The name of the event as it appears in drop-down menus, etc. is essentially just a comment. You may give more than one event the same name—the "Import Events" feature and Event Editor don't check names for uniqueness. It is recommended that you give unique descriptive names to all events you create with the Event Editor.

Event files can be imported or exported quickly (as compared to system configuration files).

If you want to edit an imported event in the Event Editor, it may take several seconds for the Event Editor to pop up. You can use events immediately after import and without editing if you already know how the event is defined and don't need to look at it.

Deleting events. Likewise, deleting events in the Event Chooser is usually relatively quick, typically under a second, longer if you are deleting from a long list. However, if you are deleting an

event that has been edited since it was imported, or an event that was created in the Event Editor, then the event has a GUI which must be deconstructed. Deleting this type of event will take longer, perhaps several seconds.

System configuration files. When you save a 167XX system configuration file, it will include all the events currently defined in the Event Chooser. These events will be restored when the configuration file is loaded. The name(s) of any event file(s) you may have loaded during the session are *not* stored in the configuration file. When a configuration file is loaded it does *not* load any event files; it loads the events from the configuration file itself.

Pre-defined events files

A set of standard pre-defined Events files are available in the same directory as the standard pre-defined 167XX system configuration files:

`/logic/configs/hp/PCI_Express/`

These are the pre-defined event files in the directory:

N4220A_Events_3DW	TLP, 3DW header, no data, packet types
N4220A_Events_3DW_Data	TLP, 3DW header, with data, packet types
N4220A_Events_4DW	TLP, 4DW header, no data, packet types
N4220A_Events_4DW_Data	TLP, 4DW header, with data, packet types
N4220A_Events_DLLP	DLLP header types
N4220A_Events_Msg	TLP, 4DW header, no data, message types
N4220A_Events_MsgD	TLP, 4DW header, with data, message types
N4220A_Events_MsgVendor	TLP, 4DW header, no data, vendor defined messages
N4220A_Events_MsgVendorD	TLP, 4DW header, with data, vendor defined messages
N4220A_Events_common	Commonly used events

This is the list of all the events in each event file.

```
N4220A_Events_3DW:
    3DW Memory Read Request
    3DW Memory Read Request-Locked
    3DW I/O Read Request
    3DW Configuration Read Type 0
    3DW Configuration Read Type 1
    3DW Completion without Data
    3DW Completion, Lck Mem Read, no Data

N4220A_Events_3DW_Data:
    3DW Memory Write Request
    3DW I/O Write Request
    3DW Configuration Write Type 0
```

6 Capturing Data (16700-Series)

```
3DW Configuration Write Type 1
3DW Completion with Data
3DW Completion for Lck Mem Read

N4220A_Events_4DW:
4DW Memory Read Request
4DW Memory Read Request-Locked
4DW Routed to Root Complex
4DW Routed by Address
4DW Routed by ID
4DW Broadcast from Root Complex
4DW Local - Terminate at Receiver
4DW Gathered and routed to Root Complex

N4220A_Events_4DW_Data:
4DW Memory Write Request
4DWD Routed to Root Complex
4DWD Routed by Address
4DWD Routed by ID
4DWD Broadcast from Root Complex
4DWD Local - Terminate at Receiver
4DWD Gathered and Routed to Root Complex

N4220A_Events_DLLP:
DLLP Ack
DLLP Nak
DLLP PM
DLLP Vendor Specific
DLLP InitFC1-P
DLLP InitFC1-NP
DLLP InitFC1-Cpl
DLLP UpdateFC-P
DLLP UpdateFC-NP
DLLP UpdateFC-Cpl
DLLP InitFC2-P
DLLP InitFC2-NP
DLLP InitFC2-Cpl

N4220A_Events_Msg:
Msg Unlock
Msg PM_Active_State_Nak
Msg PM_PME
Msg PME_Turn_Off
Msg PME_TO_Ack
Msg Assert_INTA
Msg Assert_INTB
Msg Assert_INTC
Msg Assert_INTD
Msg Deassert_INTA
Msg Deassert_INTB
Msg Deassert_INTC
Msg Deassert_INTD
Msg ERR_COR
Msg ERR_NONFATAL
Msg ERR_FATAL
```

```
Msg Attention_Indicator_Off
Msg Attention_Indicator_On
Msg Attention_Indicator_Blink
Msg Power_Indicator_Off
Msg Power_Indicator_On
Msg Power_Indicator_Blink
Msg Attention_Button_Pressed
Msg Set_Slot_Power_Limit
```

N4220A_Events_MsgD:

```
MsgD Unlock
MsgD PM_Active_State_Nak
MsgD PM_PME
MsgD PME_Turn_Off
MsgD PME_TO_Ack
MsgD Assert_INTA
MsgD Assert_INTB
MsgD Assert_INTC
MsgD Assert_INTD
MsgD Deassert_INTA
MsgD Deassert_INTB
MsgD Deassert_INTC
MsgD Deassert_INTD
MsgD ERR_COR
MsgD ERR_NONFATAL
MsgD ERR_FATAL
MsgD Attention_Indicator_Off
MsgD Attention_Indicator_On
MsgD Attention_Indicator_Blink
MsgD Power_Indicator_Off
MsgD Power_Indicator_On
MsgD Power_Indicator_Blink
MsgD Attention_Button_Pressed
MsgD Set_Slot_Power_Limit
```

N4220A_Events_MsgVendor:

```
Msg Vendor_Defined Type 0 Routed to Root Complex
Msg Vendor_Defined Type 1 Routed to Root Complex
Msg Vendor_Defined Type 0 Routed by ID
Msg Vendor_Defined Type 1 Routed by ID
Msg Vendor_Defined Type 0 Broadcast from Root Complex
Msg Vendor_Defined Type 1 Broadcast from Root Complex
Msg Vendor_Defined Type 0 Local - Terminate at Receiver
Msg Vendor_Defined Type 1 Local - Terminate at Receiver
```

N4220A_Events_MsgVendorD:

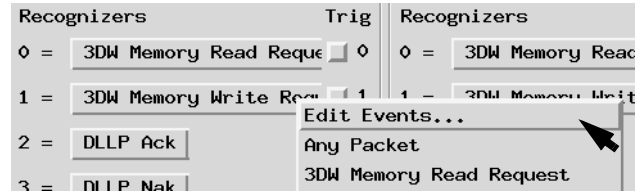
```
MsgD Vendor_Defined Type 0 Routed to Root Complex
MsgD Vendor_Defined Type 1 Routed to Root Complex
MsgD Vendor_Defined Type 0 Routed by ID
MsgD Vendor_Defined Type 1 Routed by ID
MsgD Vendor_Defined Type 0 Broadcast from Root Complex
MsgD Vendor_Defined Type 1 Broadcast from Root Complex
MsgD Vendor_Defined Type 0 Local - Terminate at Receiver
MsgD Vendor_Defined Type 1 Local - Terminate at Receiver
```

```
N4220A_Events_common:
  3DW Memory Read Request
  3DW I/O Read Request
  3DW Completion without Data
  3DW Memory Write Request
  3DW I/O Write Request
  3DW Completion with Data
  DLLP Ack
  DLLP Nak
```

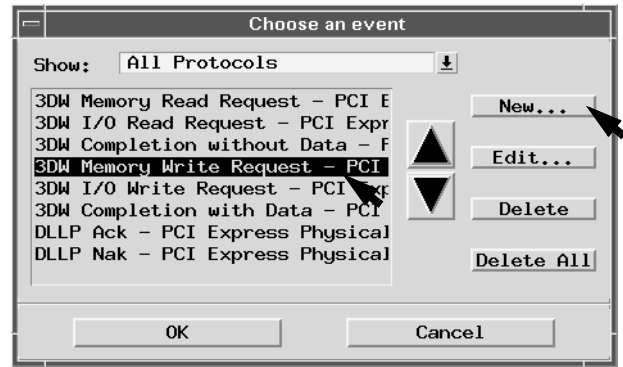
Examples of defining events

Example 1: Trigger on a Nak in the data link layer

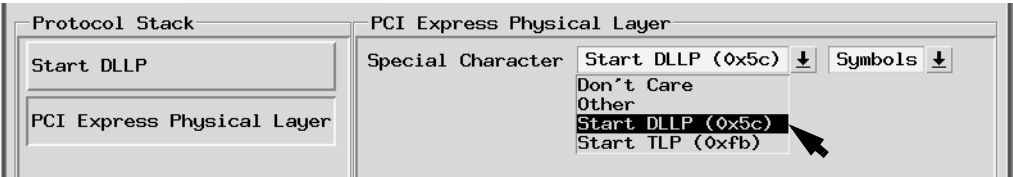
- 1 In the Events Tab, select "Edit Events..."



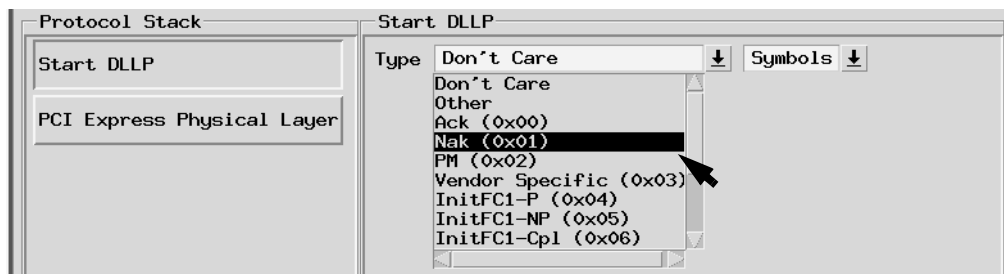
- 2 In the "Choose an event" dialog, select "New..." and make up a name for the event.



- 3 At "PCI Express Physical Layer" "Special Character" use the drop-down menu to select "Start DLLP".



4 Select the type of packet (Nak, in this case).



5 Refine the specification of the Nak packet, if necessary, then select Close.



Example 2: Trigger on a "PM_Active_State_Nak" message

- 1 In the Events Tab, select "Edit Events..."
- 2 In the "Choose an event" dialog, select "New..."
- 3 At "PCI Express Physical Layer" "Special Character" use the drop-down menu to select "Start TLP"
- 4 At "Start TLP" "Format of TLP" use the drop-down menu to select "4DW header, no data"
- 5 At "4DW header, no data" "Type" use the drop-down menu to select "Local - Terminate at Receiver (0x14)"
- 6 After this step, the "Local Message" drop-down menu appears with messages that are valid for "Local - Terminate at Receiver (0x14)".
- 7 At "4DW header, no data" "Local Message" use the drop-down menu to select "PM_Active_State_Nak (0x14)"

Creating custom triggers

There are symbols defined for all "8bbyte" and "10bbyte" labels that translate 8B/10B character names to their hexadecimal value. These labels can be used to create custom triggers using the logic analyzer's sequencer.

Examples:

```
Find 1 occurrence of
  8bbyte0 = D10.2 Symbols
then Trigger and fill memory

Find 1 occurrence of
  10bbyte0 = STP- Symbols Or
  10bbyte0 = STP+ Symbols
then Trigger and fill memory
```

Triggering between modules

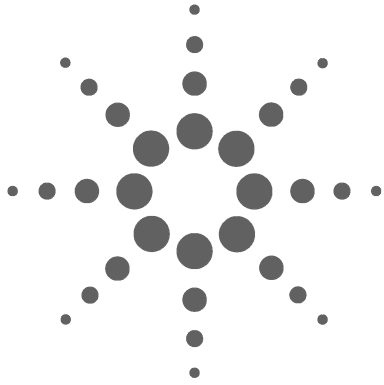
If you are using multiple analyzer modules, you will need to setup the intermodule bus (IMB). In the standard configurations that involve multiple modules, all modules are armed from group run. If you want one analyzer module to arm another analyzer module you will need to change the IMB setup.

Running a Measurement

- 1 Select the **Group Run** button in any window.



The Group Run button starts all of the logic analyzer machines together, so that you can collect data from both directions or from several links at the same time.



7 Displaying Captured Data (16700-Series)

This chapter provides an overview of the Decode tool and information on interpreting the Listing display on an Agilent 16700-series logic analysis system.

See Also

For instructions on displaying data using a 16900-series logic analysis system, see the online help.

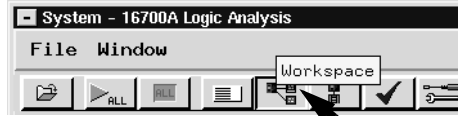
For 16700-series logic analysis systems, additional information about the Decode tool is in the online help.



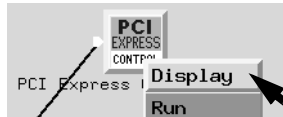
To view the online help

There is separate help for the Decode tool and for the Control tool.

- 1 Open the Workspace window.



- 2 If a Decode tool is not already in the workspace, load the appropriate configuration file.
- 3 Open the Decode tool or Control tool display.



- 4 Select **Help > On This Window....**



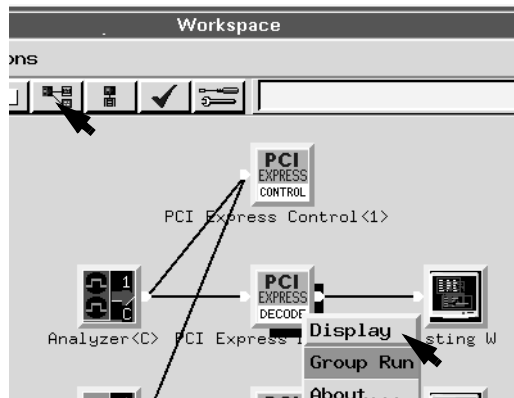
To display the captured data

To see the captured data, select the Listing tool from the workspace window.

Decode Tool

To start the Decode tool

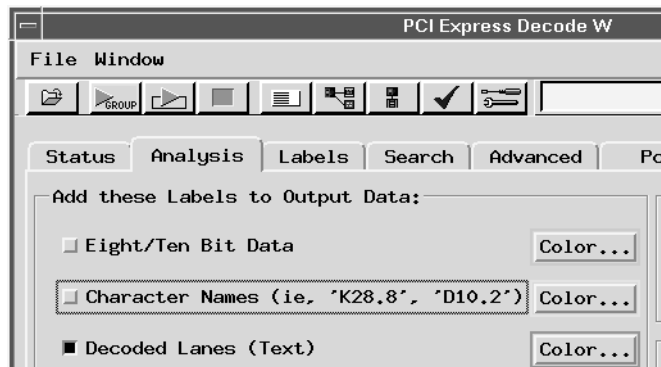
- 1 Display the Workspace window.
- 2 Loading one of the provided configuration files places a Decode tool on the workspace.
- 3 Open the Decode tool.



Status Tab

The status tab shows the status of the Agilent N4220B analysis probe as it relates to the analyzer that is supplying data to the decode tool. You cannot change any settings on this tab; use the Control tool to change the setup of the analysis probe. Changes made in the Control tool will be reflected in the Decode tool's Status tab, if they apply to the analyzer that is supplying data to the Decode tool.

Analysis Tab



Use the Analysis tab to select which columns (labels) and fields are displayed in the Listing window.

Add these Labels to Output Data:

This area allows you to add (or remove) certain labels from the listing. You can also change the color of each state based on the contents of these labels.

When you add a label, it will appear at the far right side of the listing (scroll over to see it). You can drag the headings in the Listing window to change the order of the columns.

Eight/Ten Bit Data button Select this button to include a single label which displays valid 8B and 10B data.

The Decode tool looks at both 8B and 10B labels. Because the 8B and 10B labels use mostly the same pod bits you have to look at the 8b/10b label to see whether the valid data is in the 8B label or the 10B label. When you select this button, the tool merges all this information into a single label. It is a single text label which displays the information for one state. The valid 8B or 10B data is presented in its original lane order. A single label is used to save a little display space and to slightly speed up display in the lister (only one label to iterate over), the name of this label varies by lane width:

Table 5 8B and 10B Labels

Width	Label
x1	L0 L0 L0 L0
x4	L0 L1 L2 L3
x8	L0 L1 L2 L3 L4 L5 L6 L7
x16	L0 L1 L2 L3 L4 L5 L6 L7 L8 L9 L10 L11 L12 L13 L14 L15

Character Names button Like many other protocol tools with Character Names, except the names for all lanes are placed in a single label and they are ordered like the original traffic much like the Eight/Ten Bit Data labels.

Decoded Lanes button This text label contains mnemonics for special characters and training sequences and hexadecimal values for data characters.

COM	Comma Character
SKP	Skip Character
FTS	Fast Training Sequence
PAD	Pad Character
IDL	Idle Character
SDP	Start Data Link Layer Packet
STP	Start Transaction Layer Packet
END	End Good Packet
EDB	End Bad Packet
TS1	Training Sequence 1
TS2	Training Sequence 2

Changing the color of packets Each packet type name has an associated color button. This button allows you to select a color for that type of packet.

The color associated with the "Decoded Packets" button itself is used only for packets not included in the list of packet types, which would be packets with undefined or reserved type fields.

The decode tool is limited to one color per analyzer state. This means that if any state contains the end of one packet and the beginning of the next, separate colors cannot be assigned to the two packets. Color-coding packet types will probably be most

useful when all packets begin on Lane 0. In cases where multiple packets can occur in a single state, color-coding may be confusing rather than helpful.

Eight colors are available for coloring label values in the Listing Window or waveforms in the Waveform Window. These colors are global to all Listing and Waveform windows. You can use the "Edit Colors..." button in the pop-up "Select Color" dialog to change one or more of the eight colors. Any change will be seen in all windows.

Of the eight default colors two are white: the first (left-most) and last (right-most). The first (left-most) is the default color for all label values and waveform drawings, changes in that color will be widely seen. The last (right-most) white color is a good choice for a user defined color in addition to the primary/secondary color theme of the six non-white default colors.

Bad CRC button Like many other protocol tools, a 1 in this label indicates that a CRC error was found in this state. This tool checks LCRC, ECRC and CRC.

NAK button A 1 in this label indicates that a DLLP Nak packet was found in this state.

Show fields for:

These buttons allow you to select either all fields or just a single line description in the decode text for DLLP and TLP packets.

Display field classes:

These buttons allow you to select which individual fields to display when the "Show fields for:" button is also selected.

The field classes contain these fields:

Other All fields that are not members of another class.

Reserved All fields identified as "Reserved" in the spec.

Packet Sequence Number The Packet Sequence Number in TLPs.

Format of TLP The "Fmt" field of TLP headers.

Type The "Type" field of TLP and DLLP headers.

Length The "Length" field of TLP headers.

Requester ID TLP Requester ID fields.

Tag TLP Tag fields.

Payload Decode of payloads in TLPs with data.

Address 64b, 32b and Register addresses in TLP headers.

Bus, Device, Function TLP Bus Number, Device Number and Function Number.

Completer ID TLP Completer ID fields.

Compl. Status TLP Completion Status fields.

Byte Count TLP Byte Count and Byte Count Modified fields.

AckNak_Seq_Num DLLP AckNak_Seq_Num field.

HdrFC DLLP HdrFC field.

DataFC DLLP DataFC field.

By default all classes are selected (button is black). When a button is de-selected (grey), fields of that class are not included in the decode. There can be a lot of fields in a PCI Express packet, by selecting only the fields you are currently interested in reading and de-selecting all others, you can create a decode display that is easier to read.

The options selected in these tabs will take effect after the next run of the analyzer or after the "Apply" button is selected. If you want to change several options it will be faster to change all the options in all the tabs that you want to change and then select "Apply" once, rather than selecting "Apply" after each individual option is changed.

Labels Tab

This tab allows you to select which labels to display in the Listing window. These are the choices:

8B Char Labels all labels that start with "8b"

10B Char Labels all labels that start with "10b"

Status Labels "kcode", "8b/10b", "valid", "squelch", "beacon", "bonded", "linkidle", "beacon/disp", "#packet", "#grp"

Other Labels trigger labels, user defined labels

Choosing just a few labels to display, rather than all of them, speeds up scrolling in the Listing window, and helps avoid placing important information way off screen to the right.

Search Tab

Features in this tab allow you to search for specific packets and display the result in a Listing window attached to the output of the Decode tool.

See "Searching from the Decode tool" on page 109.

Advanced Tab

Like the Analysis tab, the Advanced tab allows you change the way the decoded text appears in the Listing window. The Analysis tab lets you select whether to display whole classes of fields; use the Advanced tab to precisely control the display of individual fields.

The fields of the protocol are displayed on the left. You can scroll down to see the rest of the protocol. Double-click on a folder to see the fields in a protocol.

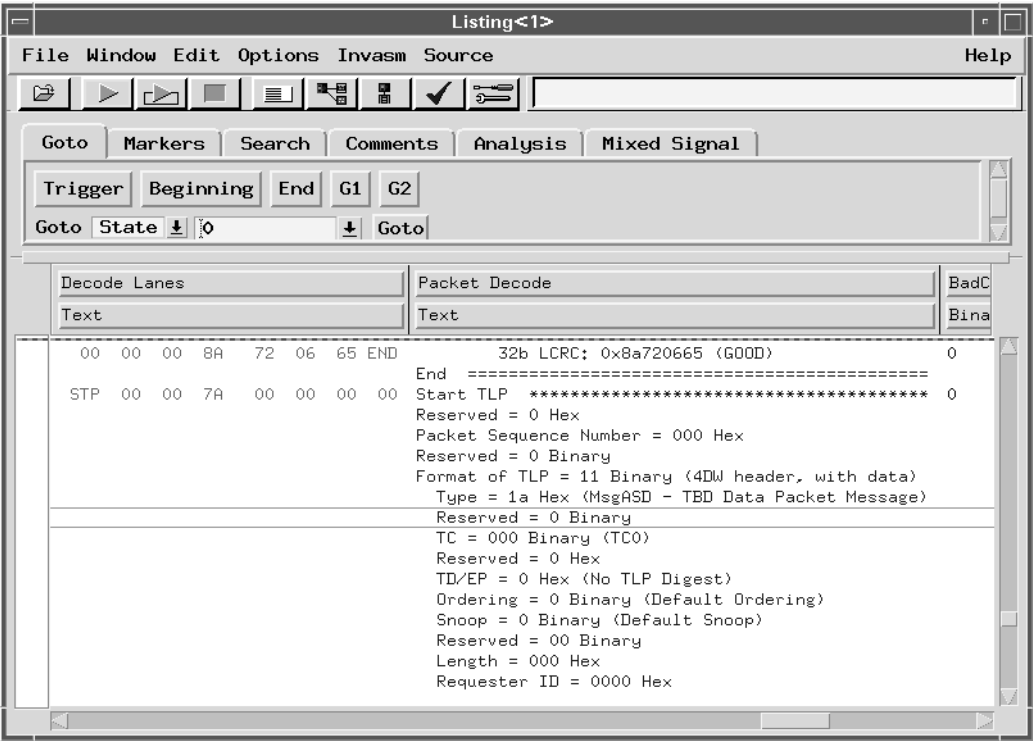
Select Yes to display a field, or No to suppress it.

The "Set all Display States to:" buttons at the bottom will set all fields to "Yes" or "No". For example, if you want to look at only a few fields you can set all display states to "No" and then set just the fields of interest to "Yes".

The options in the Analysis tab and Advanced tab work together. If the display of a protocol or field is turned off in either tab, it will not show up in the listing (No's are ORed). To see a protocol or a field in the listing, it must be enabled in both tabs (Yes's are ANDed).

See the online help for more information on the Advanced tab.

Understanding the Listing



Why are there several states on one line?

The the analysis probe can collect data from x1, x2, x4, x8 or x16 lanes. It can probe 1 direction in x16 or 1 or 2 directions in the other lane widths.

When the analysis probe is in x1 mode, data is decelerated by four, placing up to 4 symbols per state. When the analysis probe is in x2 mode, data is decelerated by two, again placing up to 4 symbols per state.

Why is some of the data “blank”?

When the probe is in x1 or x2 mode, it ensures that the deceleration results in SDP or STP symbols appearing in the Byte0 (Lane0) position so that the packet recognizers work correctly. It may need to leave some byte positions in the previous state "blank", indicating that by setting the appropriate bits in the "valid" label.

What do the column headings mean?

Each column in the listing corresponds to a logic analyzer label.

The Packet Decode label contains detailed information about each packet. All fields displayed under this label can be customized (color coded or omitted) using the Decode tool.

See also “Analysis Tab” on page 98 or “Predefined Label Descriptions” on page 58.

Choosing how to display data in each lane

The "Eight/Ten Bit Data", "Character Names" and "Decoded Lanes" analysis columns are three different ways of presenting the data as it occurs in the various lanes. You probably want to select just one of those three, using the Analysis tab in the Decode tool (see).

These three labels can present information in a more compact form than the analyzer labels. For the example, the analyzer has labels "8bbyte0" and "10bbyte0" which contain the data captured for Lane 0.

Only one of these two labels will have valid data at any one time, to determine which is valid you need to look at the MSB of "valid" to see if there is valid data in Lane 0 for that state, then you need to look at the MSB of "8b/10b" to see if it is 8B data (8bbyte0 is valid) or 10B data (10bbyte0 is valid). If it is 8B data, you also need to look at the MSB of "kcode" to see if it is a Special Character or Data Character. If it is 10B data, you need to look at the MSB of "beacon/disp" to see if it is a valid 10B code.

7 Displaying Captured Data (16700-Series)

The "Eight/Ten Bit Data" and "Decoded Lanes" analysis columns are created by looking at all these labels. If a lane contains a valid 8B code, the value is presented as two hex characters. If a lane contains a valid 10B code, the value is presented as three hex characters. If a lane contains an invalid 10B code, the text "inv" is shown rather than hex characters. If there is no valid data in that lane for that state the space is blank to indicate no data.

The "Character Names" label presents the same character name for 8B or 10B data (as defined). It also presents "inv" for invalid 10B codes and blank space for lanes with no valid data for the state.

When decoding x8, there is an extra space between lanes 3 and 4. When decoding x16 there are extra spaces between lanes 3 and 4, 7 and 8, 11 and 12. This is intended to improve readability by creating visual groups of 4 lanes.

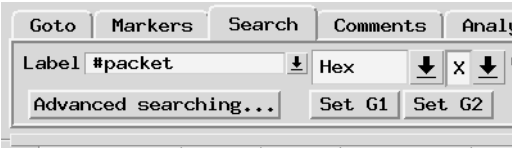
Searching

To search for text in the “Packet Decode” label

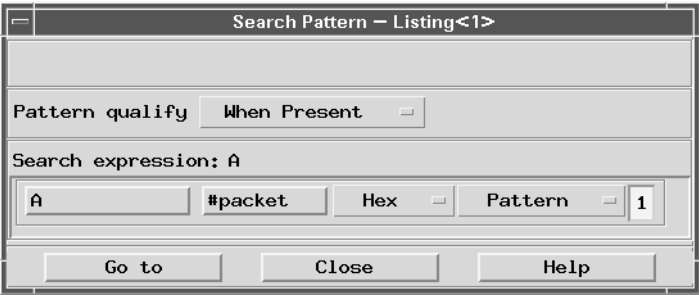
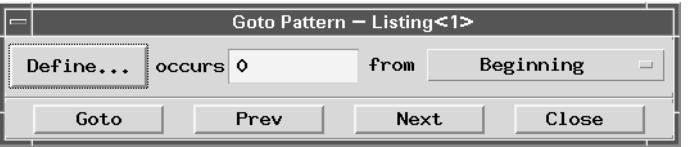
NOTE

In most cases, using packet recognizers for searching captured data is much faster than searching from the Listing window. See “Using Packet Recognizers for Search” on page 108.

- 1 In the Listing window, select the **Search** tab, then **Advanced Searching...**



- 2 Leave both the "Goto Pattern" dialog (pops up from the "Advanced searching..." button) and the "Search Pattern" dialog (pops up from the "Define..." button in "Goto Pattern") open and visible while you search.



NOTE

The search will take you to the state where the pattern was found, not to the decoded line within the state.

Search results are presented in the "Search Pattern" dialog. The text search is case insensitive.

If you want to search starting at the state you're looking at, select "Display Reference" in the Goto Pattern dialog. That may shorten the search time by avoiding searching states before the current Display Reference.

When you change options in the Decode tool, the search pattern is reset.

Choosing where to begin the search

Also, in the "Goto Pattern" dialog there is a drop down-menu, which looks something like this:

```
Define... occurs 1 from Beginning
```

The "Beginning" button is a drop-down menu that lets you select, "Beginning", "End", "Trigger", "Display Reference". "Beginning" is the default. If you want to search starting at the state you're looking at, select "Display Reference". That may shorten the search time by avoiding searching states before the current Display Reference.

Using Packet Recognizers for Search

Packet recognizers (the Events tab of the control tool) can be used to speed up searches, but you have to know in advance what you are going to be searching for.

Suppose you want to look at all the 3DW Memory Writes in the analysis buffer. Set up an event:

```
Special Character = Start TLP
Format of TLP    = 3DW header, with data
Type             = Memory Write Request
```

This recognizer will match all the packets of interest. You don't have to use this recognizer in the analyzer trigger, set up whatever trigger you want.

Suppose you named this event "3DW Mem Write", a symbol will be set up in the analyzer for the #packet label called "3DW_Mem_Write". Then in the listing window, in the Search

tab (#packet is an integer label, so you don't have to use "Advanced Search", you can if you want to, but this example doesn't) make these selections:

Label #packet Symbols value 3DW_Mem_Write when Present

NOTE

This search will use the hardware accelerated search in the logic analyzer card.

The hardware-assisted search is available only for data currently captured by the analyzer. If you save a configuration file with data and then later load that file, hardware-assisted search is not available for the saved data. That data is *not* all loaded into the card.

Other analyzer labels that may be useful in searches:

kcode To find special characters in Lane 0:

Label kcode Binary 1XXXXXXXXXXXXXXXXX when Entering

8b/10b When in 8b mode, a 10b character will be generated when there are character errors. This label can be used to search for 10b errors in 8b traces, for example:

Label 8b/10b Hex 0000 when Exiting

beacon Indicates that at least one lane is in the beacon state (signaling to indicate exit from L2 link power management)

Label beacon Binary 1 when Present

bonded All lanes are framed and valid skip ordered-sets have been seen.

Label bonded Binary 1 when Present

squelch Lane 4 is squelched (electrical idle)

Label squelch Binary XXXX1XXXXXXXXXXXXXXXXX when Present


Searching from the Decode tool

The Search tab in the Decode tool allows you to search for specific packets and display the result in a Listing window.

The search does not depend on any of the labels created by the Decode tool; it uses only the labels from the standard configurations of the analyzer.

StatusAnalysisLabelsSearchAdvanced

Listing Window:

Search from Display Reference in: Listing<1> 

Find Listing Windows

Hardware assisted search:

☐ Use hardware assisted search

Search beginning in these lanes:

0123

☒☐☐☐

Packet Search:

Find: 3DW Memory Read Request

PrevNext

Ordered-set Search:

Find: Any Ordered-set

PrevNext

Search from Display Reference in:

The "Display Reference" of the Listing window is indicated by a pair of light grey lines over and under the state that is the current display reference. By default, the display reference of a Listing window is the middle of the display area. You can change the display reference in a Listing window by selecting (from the Menu bar):

Listing<1>

OptionsInvasmSource

Options

Tabs

Popup on Run

Font

Display symbolic

Reference trigger...

Display reference

Top

• Middle

Bottom

The drop-down menu box lets you select which of the listing windows attached to the decode tool you want to perform the search in. If there is no listing window attached, you will see the text

No Listing Window(s)!

as the only entry in the drop-down menu box. You must have a listing window attached in order to use the search feature. If you attach a new listing window, or change the name of one already attached, you can select the "Find Listing Windows" button to update the drop-down menu box.

Hardware-Assisted Search:

The Use Hardware Assisted Search button enables use of the hardware assisted search function of the analysis card (1675[3,4,5,6]). The hardware search is used to find the start of a packet which is then compared with the full packet definition in software.

How Hardware-assisted search works. The hardware-assisted search can find a given pattern in a state. A pattern is set up based on the contents of the event, the hardware is programmed to search for that event, and then the search is started.

Since this hardware-assisted search can find a pattern only in one state and since PCI Express packets can span states, the hardware-assisted search is not always able to identify a complete packet, but rather a matching beginning of a packet. The rest of the packet is compared in software. If it doesn't make a complete match, the hardware-assisted search is started again on the state after the last potential match.

Effect of lane width. The hardware-assisted search is more effective in wider lane width configurations. This is because, for example, in a x16 configuration a pattern can be set up to match the first 16 bytes of a packet, whereas in a x4 configuration only the first 4 bytes of a packet can be used in the hardware-assisted search.

Search beginning in these lanes:

These buttons, one per lane for the current configuration, allow you to select the lanes in which to look for a start of packet. Packets may legally begin only in lanes that are a multiple of 4 (for example, lanes 0, 4, 8 and 12 in a x16 link). There are buttons for each lane to support searches for the exceptional condition of a packet beginning in an invalid lane.

When more than one lane is selected for the hardware-assisted search, it will first set up a pattern based on a packet beginning in the first lane that is selected. It will then set up a pattern for the next lane that is selected. So, for example, in x16 if all 16 lanes are selected for search, 16 different searches will be set up and executed.

With the software search, it makes little difference in execution time how many lanes are selected.

In some exceptional cases the software search may be faster than hardware assisted search. For example, if the trace buffer is filled with packets nearly identical to the event you are searching for and nearly every state contains the beginning of a packet, software search will probably be faster than hardware assisted search.

Packet Search:

The button beside "Find Event" contains the name of the currently defined event or "Any Packet" if an event has not been defined.

Selecting this button lets you pop-up the event editor to define a new event or you can select an event that is already defined from its drop-down menu.

Ordered-set Search:

Selecting this button allows you to choose which kind of ordered-set to find.

Prev / Next

The "Prev" and "Next" buttons are used to initiate a search.

The "Prev" button causes a search for the event defined by "Find Event" that begins at the state before the Display Reference and proceeds toward the beginning of the trace.

The "Next" button causes a search for the event defined by "Find Event" that begins at the state after the Display Reference and proceeds toward the end of the trace.

If the search succeeds, the state containing the beginning of the event being searched for will be moved to the Display Reference of the selected Listing Window.

If a search takes longer than about 1 second, a progress indicator will appear. The % complete indicator shows the percent of states from the Display Reference to the beginning/end of the trace that have been searched. The time indicator estimates the time remaining to search to the beginning/end of the trace. The "Cancel" button on the progress indicator allows you to stop the search. If you stop a search, the Display Reference of the Listing Window is not changed.

Note that neither "Prev" nor "Next" will find the current state, even if it contains the event defined in "Find Event".

Using an events file

As described in "Events files" on page 85, the events created in the Event Editor can be saved/restored in an ASCII (text) file. The same events are visible and usable in both the Search tab of the Decode tool and the Events Tab of the Control tool. An events file can also be loaded on another 16700-series logic analysis system configured with a PCI Express Control tool and Decode tool.

On the menu bar of the Decode tool under the File drop-down menu there are three entries related to events files:

- Import Events...
- Export Events...
- View Events in File...

Each menu item pops up a file browser that lets you select the file the action applies to.

Speeding up your searches

Search time depends on both the data in the trace and the data that is being searched for. Generally, the more similar the data in the trace is to the data being searched for (without being a match for the search), and the more data there is to search, the longer the search will take.

Using “advanced search”

Decode tools read data from an analysis card, find the beginnings of packets by looking at values in certain analyzer labels, create textual descriptions of the fields in the packet and attach those descriptions to specific states in the analyzer data.

So using advanced search to find text is a process of generating and searching strings. If you generate shorter strings it will take less time to generate/search. Some things you can do to shorten strings and thereby search times:

- In the Analysis tab of the Decode tool, turn off any labels you are not using for the search.
- In the Fields tab of the Decode tool, select only the fields you are using in the search. De-select all others.

Remember to select the Apply button at the bottom of the decode tool so your selections in the Analysis and Fields tab take effect.

Using the Decode tool

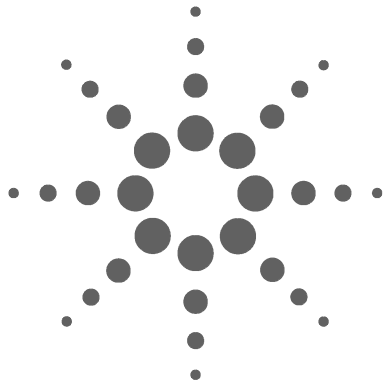
The Search tab in the Decode tool searches for events defined in the Event Editor (see “Event Editor” on page 83).

This is a more powerful search since you can specify values for multiple fields in the packet, which you can't with a text search.

This is a software search that reads data from analyzer labels and compares it to the selected event. Since it doesn't generate or use the decoded text labels it is quite a bit faster than the text search in the Listing window's Advanced Search.

The Search tab in the Decode tool also has a "Hardware-Assisted Search" option which only searches for packets that begin in Lane 0. The analyzer cards that are used with the analysis probe have a facility to search the trace buffer (RAM on the card itself) for a pattern (generally referred to as "hardware-assisted search"). The "Hardware-Assisted Search" sets up a pattern and instructs the card to search for it. This can be very fast since the card can search its own memory far faster than it can be transferred off the card and searched in software.

7 Displaying Captured Data (16700-Series)



8 Troubleshooting and Repair



Troubleshooting Problems with the Displayed Data

If no data is displayed after a run

- ✓ Check that the logic analyzer is correctly connected to the analysis probe.
- ✓ Check that all cables are correctly connected to the analysis probe.
- ✓ Load one of the supplied configuration files. If the format specification (the mapping of signals from the logic analyzer pods to labels) is changed, the Decode tool will work incorrectly or not at all.

If incorrect data is displayed

If the decoded data does not look correct (for example, bad CRCs are reported even though the data should be correct):

- ✓ Select the “Query Lane Inversion” button in the Control tool. This will ensure the probe sees the correct lane polarity.
- ✓ Deskew the logic analyzer. See “Deskewing the logic analyzer” on page 120

If a “BadCRC” is displayed

- ✓ If you see a bad CRC in a TLP and are tracing both directions of a link, search for the Ack/Nak to the TLP in the other direction.
- ✓ If the TLP is Acked, the bad CRC may be the result of a bit error in the analysis probe.

Problems with triggering and data

Any time data is suspect, look at the “bonded” label to ensure all of the lanes in a link are bonded. If you're in 8B mode, look at beacon/disp to verify no disparity errors.

Determine if a probe is bonded by running a measurement with a trigger on a value of 0 for the bonded label. For example:

```
Find 1 occurrence of  
bonded = 0 Hex  
then Trigger and fill memory
```

If this measurement triggers, the probe is not bonded. In tests at Agilent, when a probe bonds and stays bonded for a minute or more, it tends to stay bonded. The probe will lose bonding when there are too many character errors on a given lane. Then the bonding label goes to zero and the probe attempts to re-bond by watching for Skip Ordered-Sets.

If the probe will not bond continuously, you won't be able to make meaningful measurements.

Possible fixes to this problem include ensuring the target is being correctly probed and all connectors are correctly seated. You may also need to verify that the target is producing valid signals.

Deskewing the logic analyzer

If the data captured by the analyzer does not look like what you expect, you may need to deskew the analyzer before running any measurements. Deskewing trains the logic analyzer to sample each signal at the moment that it is most likely to be stable.

When to deskew the analyzer

Events which may require you to deskew the analyzer include:

- Any of the logic analyzer modules in the logic analysis system are replaced.
- The temperature is changed significantly.
- The frequency of the link being probed is changed to a frequency which is higher than what was used to deskew the analyzer.
- The analysis probe is connected to a new target PCI Express link.

To prepare to deskew

- 1 Make sure the analysis probe is connected to the cable set.
- 2 Make sure the analysis probe is connected to the logic analysis system.
- 3 Make sure the analysis probe is turned on.

Deskewing on a 16700-series logic analysis system

To begin the deskewing process

- 1 Open the Control tool.
- 2 Select the Setup tab.
- 3 Select the De-Skew mode.
- 4 From the logic analyzer machine, run Eye Finder. It takes about 15-20 minutes to deskew the analyzer. Progress is displayed in the Eye Finder results window.

- 5 Save the Eye Finder data (see "To save Eye Finder data" on page 121).

More information on deskewing can be found by selecting **Help>On this window** from the Control tool.

To save Eye Finder data

In the Eye Finder (that is, in the Sampling Positions dialog) use the File menu to save the results of the deskewing process.

Choose a file name which specifies the bus frequency and the analyzer setup.

It is a good idea to save Eye Finder data *immediately* after deskewing the analyzer and verifying the results.

To load Eye Finder data

Load Eye Finder data after you have loaded a new state configuration file.

NOTE

Each Eye Finder data file is specific to the logic analysis system setup which was used for the deskewing run. If the hardware setup has changed in any way (see "When to deskew the analyzer" on page 120) then you should deskew again.

- 1 Open the logic analyzer's Sampling tab.
- 2 Select Sampling Positions....
- 3 Select File then Load Eye Finder....
- 4 Select the file to load.

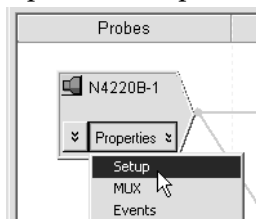
See "Deskewing the logic analyzer" on page 120 for more information on deskewing.

See the Help menu in the Sampling Positions dialog for more information about Eye Finder data files.

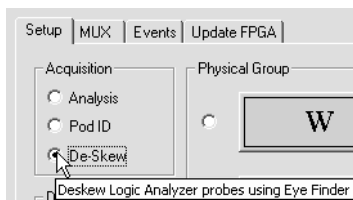
Deskewing on a 16900-series logic analysis system

To begin the deskewing process

- 1 Open the Setup tab of the probe tool.



- 2 Select the De-Skew mode.



- 3 Go to the Sampling tab of the logic analyzer module.



- 4 Select **Sample Positions...**



- 5 Select **Run**.



- 6 Save the logic analyzer configuration to a file.

Updating the FPGAs

You can update the FPGAs in the probe by sending new configurations over the analyzer cables. It takes 20 minutes or more (the FLASH memory erase time is variable) to update the FPGAs. This should only be done when requested by Agilent.

To update the FPGAs, use the Updates tab in the Control tool. At the top of the tab is text indicating the current FPGA version and Probe ID.

Update FPGA

This button will download the currently selected FPGA version.

Select FPGA Version

This box contains a list of available FPGA versions. The text area to the right of the list of available FPGA versions contains a description of the currently selected version.

Print update text

Send the contents of the text area to the currently configured printer.

Search for FPGA files

This will search the file system for FPGA files available for the analysis probe and update the "Select FPGA Version" box.

Service and Repair Information

To return a part to Agilent Technologies for service

- 1 Follow the procedures in the “Troubleshooting...” chapters to make sure that the problem is caused by a hardware failure, not by configuration or cabling problems.
- 2 In the U.S., call 1-877-4Agilent (1-877-424-4536). Outside the U.S., call your nearest Agilent sales office. Ask them for the address of the nearest Agilent service center.

To locate a sales or service office near you, go to the world-wide web site:

<http://www.tm.agilent.com>

and select Contact Us.

- 3 Package the part and send it to the Agilent service center.

Keep any parts which you know are working.

- 4 When the part has been replaced, it will be sent back to you.

The unit returned to you will have the same serial number as the unit you sent to Agilent.

The Agilent service center can also troubleshoot the hardware and replace the failed part. To do this, send your entire measurement system to the service center, including the logic analysis system and cables.

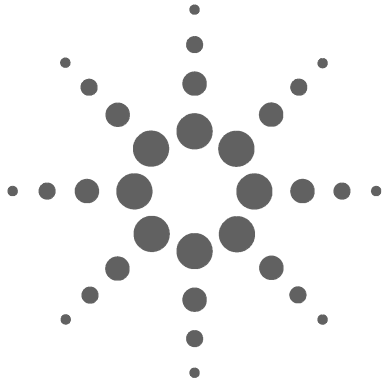
In some parts of the world, on-site repair service is available. Ask an Agilent sales or service representative for details.

To get replacement parts

The repair strategy for this product is board replacement. However, some mechanical parts may be replaced if they are damaged or lost. Contact your Agilent Technologies Sales Office for further information.

For some parts, exchange assemblies are available when a repairable assembly is returned to Agilent Technologies. These assemblies have been set up on the “Exchange Assembly”

program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.



9

Characteristics, Regulatory, and Safety Information



Analysis probe—operating characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the Agilent N4220B analysis probe.

Table 6 Connectors

Analyzer IN	Connectors for use only with an Agilent-supplied PCI Express slot cable set or midbus connector cable set.
Logic Analyzer Pod Outputs	Sixteen 100-pin Samtec connectors
Stimulus OUT	PCI Express Test Instrument Compliance Pattern is output if the Acquisition mode is "SERT" (enabled in software).
RefCLK IN	Min: 0.8V, Max: 5V, 90-110MHz. CAT I (Mains isolated)
RefCLK OUT	A buffered version of the clock received on the RefCLK IN connector (enabled in software).
Trigger OUT	BNC connector. Logic high level with 50-ohm load \geq 2.0 V. Logic low level with 50-ohm load \leq 0.4 V.

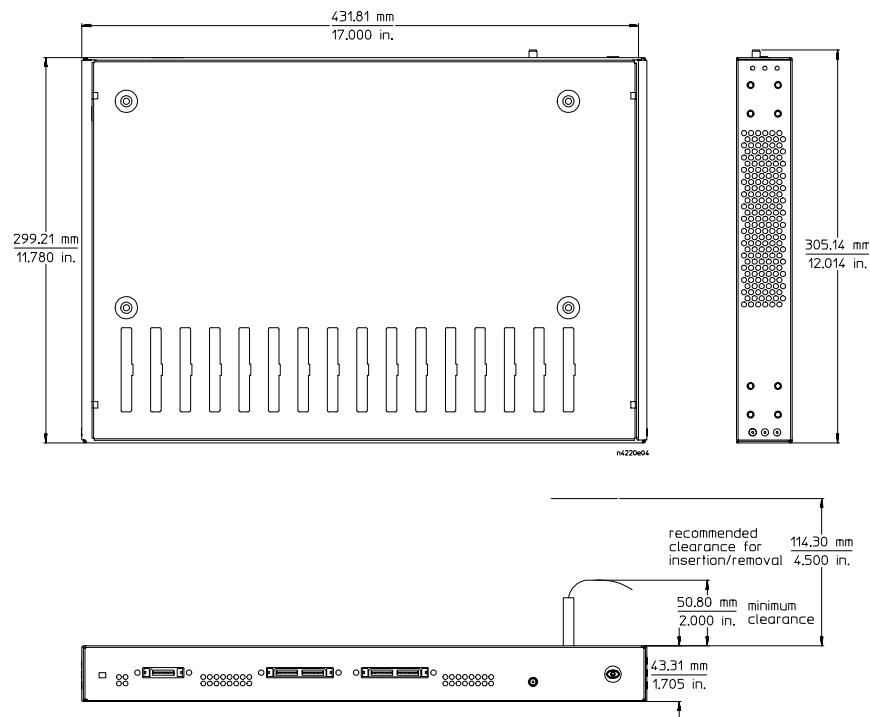
Table 7 Electrical Characteristics

Electrical Characteristics	
Power Requirements (Power Supply)	Input: 100-240 V, 1.5 A, 50/60 Hz, IEC 320 connector Output: 12 V, 5 A CAT II (Line voltage in appliance and to wall outlet)
Power Requirements (N4220B Analysis Probe)	Input: 12 V DC, 5 A. Use only with the provided power supply. CAT I (Mains isolated)
Power Requirements (Cable Sets)	Not applicable (passive device)
Load Modell	See Agilent Technologies document, <i>PCI Express Logic Analyzer Probing Design Guide</i> for information on how the probe may affect the link under test.

Table 8 Mechanical Characteristics

Mechanical Characteristics

Analysis Probe Dimensions See “Bench Space for the Analysis Probe” on page 16 for ventilation requirements.



Weight Probe: g (lb). Power supply: g (lb).

Table 9 Environmental Characteristics (Operating)

Environmental Characteristics (Operating)	
Temperature	Operating/non-operating: +20° to +30° C (+68° to +86° F)
Altitude	Operating/nonoperating 4,600 m (15,000 ft)
Humidity	Up to 50% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation on the circuit board. For indoor use only. Pollution degree 2: Normally only dry non-conductive pollution occurs. Occasionally a temporary conductivity caused by pollution may occur.

Safety Notices

This apparatus has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warnings

- Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.
- If you energize this instrument by an auto transformer (for voltage reduction or mains isolation), the common terminal must be connected to the earth terminal of the power source.
- Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.
- Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not use the instrument in a manner not specified by the manufacturer.

To clean the instrument

If the instrument requires cleaning: (1) Remove power from the instrument. (2) Clean the external surfaces of the instrument with a soft cloth dampened with a mixture of mild detergent and water. (3) Make sure that the instrument is completely dry before reconnecting it to a power source.

Safety Symbols



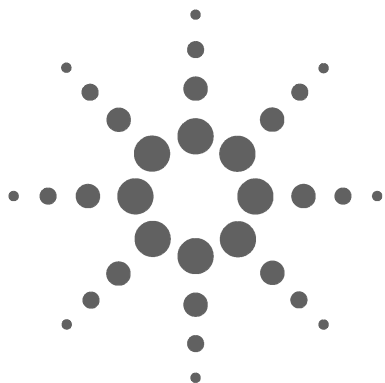
Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product..



Hazardous voltage symbol.



Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.



Glossary

Analysis Probe A probing solution connected to the target microprocessor. It provides an interface between the signals of the target microprocessor and the inputs of the logic analyzer. Also known as a “preprocessor” or an “LAI.”

Group All of the pods required to probe one direction of a lane.

Intermodule Bus The intermodule bus (IMB) is a bus in the frame that allows the measurement modules to communicate with each other. Using the IMB, you can set up one instrument to arm another. Data acquired by instruments using the IMB is time-correlated.

Label Labels are used to group and identify logic analyzer channels. A label consists of a name and an associated bit or group of bits. On 16900-series logic analyzers, labels are usually called “bus/signal names.”

LAI Logic Analyzer Interface, see *Analysis Probe*.

Machine (16700-series logic analysis systems only) Each measurement is handled by a different machine. Each machine is represented in the Workspace window by an icon. Typically, a machine corresponds to a single logic analyzer *module*. Logic analyzer resources such as pods and trigger terms cannot be shared by the machines. A module can be split into several machines.

Master Card In a module, the master card controls the data acquisition or output. The logic analysis system references the module by the slot in which the master card is plugged. For example, a 5-card Agilent Technologies 16755A would be referred to as *Slot C: machine* because the master card is in slot C of the mainframe. The other cards of the module are called expansion cards.



Module An instrument that uses a single timebase in its operation. Modules can have from one to five cards functioning as a single instrument. When a module has more than one card, system window will show the instrument icon in the slot of the *master card*.

Setup Assistant A software program on 16700-series logic analyzers that guides a user through the process of connecting and configuring a logic analyzer to make measurements on a specific microprocessor.

Symbol Symbols represent patterns and ranges of values found on labeled sets of bits. Two kinds of symbols are available:

- 1) Object file symbols – Symbols from your source code, and symbols generated by your compiler. Object file symbols may represent global variables, functions, labels, and source line numbers.
- 2) User-defined symbols – Symbols you create.

Target System The device under test.

Trigger Specification A set of conditions that must be true before the instrument triggers. See the printed or online documentation of your logic analyzer for details.

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