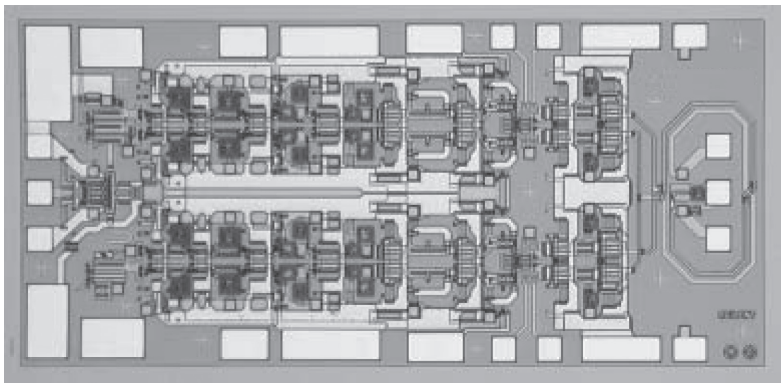
Keysight 1GG6-4059
3 to 20 GHz IQ Modulator

Data Sheet



Features

- 3.2 to 20 GHz operation
- > 2 GHz modulation bandwidth
- Good output power flatness with frequency and temperature
- Easy quadrature adjustment and impairment

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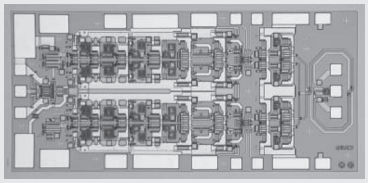
Description

The 1GG6-4059 is a broadband IQ modulator for microwave digital signal generation. The device is fabricated using the Keysight Technologies, Inc. GaAs/InGaAs/AlGaAs pHEMT process which combines outstanding performance with instrument grade reliability. The LO input is vector–modulated in response to differential signals into the I and Q ports.

The output signal is combined using an on–chip balun for single-ended operation with improved output power, carrier rejection, and dynamic range.



- Chip size: 2490 x 1200 µm (98.0 x 47.2 mils)
- Chip Size Tolerance: ±10 µm (±0.4 mils)
- Chip thickness: 62.5 ±15 µm (2.5 ±0.6 mils)

Absolute maximum ratings[1]

Symbol	Parameters/conditions	Min	Max	Units
V_{ss}	Negative supply voltage	–5.5	0	Volts
V_{blo}	Mixer bias voltage	–2	2	Volts
V_{ci}, V_{cq}	I and Q channel phase control voltage	–2	2	Volts
V_I, V_{Ibar} V_Q, V_{Qbar}	I and Q input voltages	–1.5	1.5	Volts
I_{di}, I_{dq}	Detector diode bias current		125	uA
V_{di}, V_{dq}	Detector diode bias voltage	–2	2	
VLO_{DC}	DC voltage on LO input	–2	2	Volts
PLO_{in}	Total LO input power		19.4	dBm
VDC_{RFout}	DC voltage at RF output	–9	9	Volts
T_{bs}	Backside temperature[2]	–55	75	°C
T_{max}	Maximum assembly temperature (for 60 seconds maximum)		300	°C
T_{stg}	Storage temperature	–65	165	°C

1. Operation in excess of any one of these ratings may result in permanent damage to this device. T_A = 25 °C except for T_{bs}, T_{stg}, and T_{max}.
2. For MTTF > 5 x 10^5 hours. Operation in excess of T_{bs} will degrade MTTF.

DC specifications/physical properties[1]

Symbol	Parameters/conditions	Min	Typ	Max	Units
V_{ss}	Supply voltage	–5.2	–5.0	–4.8	Volts
I_{ss}	Supply current	0.92	1.1	1.33	Amps
$V_{(I-Ibar)}$,$V_{(Q-Qbar)}$	Differential modulation voltage drive		150		mV rms
V_c	Quadrature coarse adjust control voltage (automatically set by DC feedback loop to equalize V_{di} and V_{dq} to within five millivolts)	–1.3		+1.0	Volts
V_{ci} –V_{cq}	Quadrature fine adjust – to achieve quadrature		±0.05		Volts
	Quadrature fine adjust – full–scale		±0.5		Volts
IV_{di}, IV_{dq}	Detector diode bias current	25	50	100	uA
V_{di}, V_{dq}	Detector voltage (RF off)	0.5	0.75	1.1	Volts
dV_{di}, dV_{dq}	Detected voltage ($Vd_{rf\,on}$ – $Vd_{rf\,off}$) (LO = 10 dBm @ 20 GHz)[2]			–0.1	Volts
V_{blo}	Mixer bias voltage (Set for highest P_{out} at highest use frequency)	–1.2	–0.6	0	Volts
RL_{di}, RL_{dq}	Resistive load on di and dq	75 k	100 k	125 k	Ohms

1. Measured on wafer with T_{chuck} = 25 °C unless otherwise noted.
2. Detector deflection is negative.

RF specifications

Symbol	Parameters/conditions	Min	Typ	Max	Units
f	Frequency range	3.2		20	GHz
P_{LO}	LO input power	6	7	10	dBm
Gain ratio	Ratio of I to Q gain	0.8	1.0	1.2	V/V
RL_{LO}	LO input return loss		–12	–8	dB

1. Measured on wafer with T_{chuck} = 25 °C unless otherwise noted. Conditions: V_{blo} = –0.8V, V_{ss} = –5.0 V

Applications

The 1GG6-4059 adds accurate direct vector modulation to RF and Microwave signals.

Biasing

The 1GG6-4059 operation requires a single –5 V power supply (V_{SS}) and other biases and adjustments as shown in the chip schematic in Figure 1. Two 50 µA current sources bias internal detector diodes. The DC negative feedback loop automatically sets coarse quadrature and stabilizes device performance against time and temperature effects. V_{blo} optimizes mixer conversion loss and linearity. There are also four external adjustments which are frequency–dependent:

1. V_{ci}–V_{cq}: Fine adjustment of quadrature (note that coarse quadrature is automatically adjusted by the negative feedback loop).

2. I (or Q) channel gain: To compensate for slight channel gain differences.

3. I channel offset: A small DC offset to cancel in–phase carrier leakage paths to the output.

4. Q channel offset: A small DC offset to cancel quadrature carrier leakage paths to the output.

Values for the above four should be determined during factory calibration.

Operation

The 1GG6-4059 includes a balun to reduce carrier leakage and maximize output power. This works because the balun responds only to differential-mode signals, while carrier leakage is common-mode.

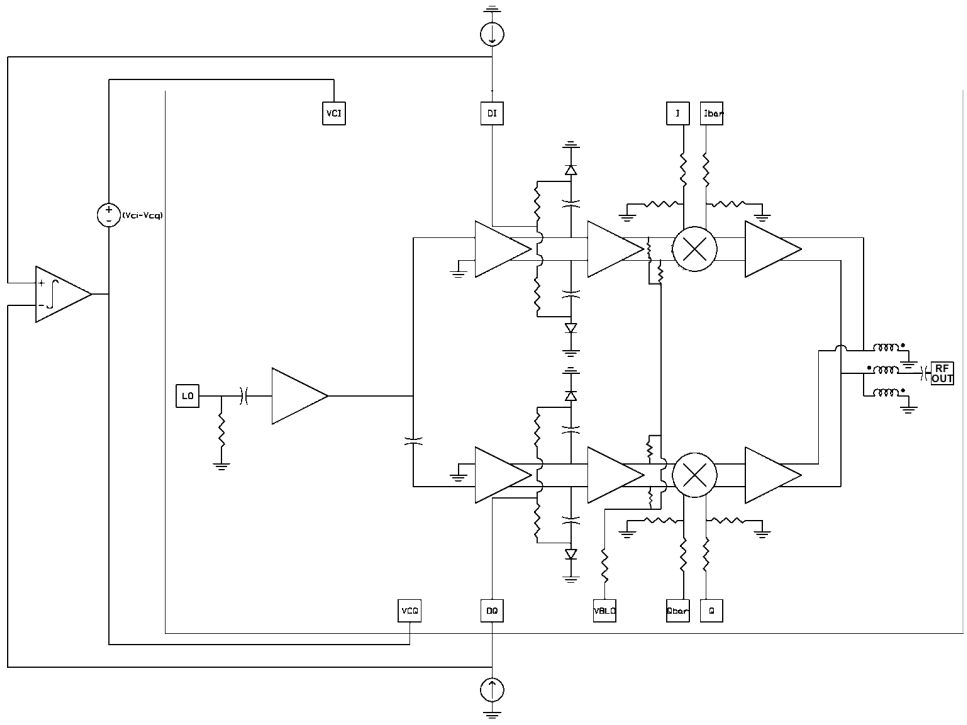


Figure 1. 1GG6-4059 electrical control diagram

The five separate V_{ss} pads should be bypassed with 47 pF capacitors placed very close to the chip. A 0.1 uF cap should be used to bypass V_{ss}, and can be located on the bias board.

Note that the 1GG6-4059 output is close to a square wave, containing strong harmonic content at odd multiples of the carrier frequency. External filtration is required if these harmonics are unacceptable.

V(I–I_{bar}) and V(Q–Q_{bar})

I and Q port input impedances change as a function of V_{blo} and frequency. Input impedances drop as V_{blo} is adjusted more positive as the mixer FETs are spending a greater proportion of the time turned on. Input impedances also drop as RF frequency increases because the post amplifier's capacitive loading effects increase at higher frequencies.

The specifications in this data sheet refer to voltages directly at the I and Q pads of the chip. For finite I and Q signal source impedances, the user may choose to increase the source voltage as frequency increases to maintain constant voltage drive at the chip I and Q ports.

Imperfect mixer port–to–port isolation produces some RF energy at the I and Q ports. Care should be used to prevent standing waves from creating ripples in the device performance. It is recommended that a closely spaced, LC low pass filter is used with a corner frequency of 1 - 2 GHz to prevent LO leakage through the baseband paths, and to maintain a controlled termination impedance at the LO rates.

Diode Biasing

The detector bias current supplies must be able to source into +1 V.

V_{blo}

Conversion gain and IM3 performance are weak functions of V_{blo}. Settings from –1.2 to 0 V will usually show little sensitivity. A recommended setting of –0.7 to –0.5 will come close to optimum performance for most devices. Optimum V_{blo} is a function of FET pinchoff voltage, which varies from chip to chip and wafer to wafer.

LO Harmonic Content

Due to the high–pass / low–pass nature of the lead/lag phase shifters, changing harmonic energy on the LO input could invalidate the calibration. Harmonic content less than –45 dBc will generally obviate this concern. Unless otherwise indicated in the figures below, P_{in} = 7 dBm. V_{blo} is not readjusted between different measurements.

Input LO Power

The FET–based phase shifters produce their own distortion. Higher drive levels exacerbate this problem and adversely affect quadrature drift performance over temperature. The highest sensitivity occurs at lower frequencies. Improved quadrature drift can be obtained by sloping the LO power down at low frequencies. A 2 - 4 dBm LO drive at 3.2 GHz results in no appreciable degradation in IM3 products, or LO feedthrough drift while gaining several dB in reduced image drift. An LO drive as high as 10 dBm at 20 GHz will cause minimal degradation to quadrature drift, and may fractionally improve IM3 products.

Assembly Techniques

See Figure 2 for bond pad dimensions and locations.

Epoxy die–attach using a conductive epoxy, and solder die– attach using a fluxless gold–tin solder preform are both suitable assembly methods. The IC must be attached to an electrically conductive surface that forms DC and RF ground for the circuit. Wire mesh bonds (500– line/inch or equivalent) should be used at the RF input and output ports. These bonds must be kept as short as possible to minimize parasitic inductance. DC bias may be supplied through conventional 0.7–mil gold wire bonds. Using 1.0 mil wire is not recommended.

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling and assembly. PCB Contract Manufacturers and sub-contractors should note that the 1GG6-4059 has a human body model ESD sensitivity as low as 75 volts. MMIC ESD precautions, handling considerations, and die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Keysight Technologies GaAs MMIC ESD, Die Attach and Bonding Guidelines - Application Note, literature number 5991-3484EN provides basic information on these subjects.

RoHS Compliance

This device is RoHS Compliant. This means the component meets the requirements of the European Parliament and the Council of the European Union Restriction of Hazardous Substances Directive 2011/65/EU, commonly known as RoHS. The six regulated substances are lead, mercury, cadmium, chromium VI (hexavalent), polybrominated biphenyls (PBB) and polybrominated biphenyl ethers (PBDE). RoHS compliance implies that any residual concentration of these substances is below the RoHS Directive's maximum concentration values (MVC); being less than 1000 ppm by weight for all substances except for cadmium which is less than 100 ppm by weight.

Bonding Pad Location and Dimensions

	Xlower	Ylower	Xupper	Yupper		Volts DC		
Name	(um)	(um)	(um)	(um)	Description	Min	Typ	Max
LO_{in}	17	520	97	600	Local oscillator input pad	–2	0	2
VSS_B	17	25	147	265	–5 V input buffer amplifier supply	–5.5	–5	0
VCQ	187	25	387	155	Lead phase shifter bias voltage	–2		1.5
DQ	630	20	785	120	Q path detector bias	–1	0.8	1.5
VSS_{LOQ}	827	20	1150	120	–5V Q path lo amplifier supply	–5.5	–5	0
V_{BLO1}	1240	15	1425	110	Mixer bias voltage	–1.5	–0.6	0.5
Q	1517	15	1597	95	Q path non–inverted baseband input	–1.5		1.5
Q_{BAR}	1667	15	1747	95	Q path inverted baseband input	–1.5		1.5
VSS_{P1}	1813	15	2073	95	–5 V postamp supply voltage	–5.5	–5	0
RF_{OUT}	2222	520	2302	600	RF output signal	–9	0	9
VSS_{P2}	1813	1025	2073	1105	–5 V postamp supply voltage (duplicate)	–5.5	–5	0
I	1667	1025	1747	1105	I path non–inverted baseband input	–1.5		1.5
I_{BAR}	1517	1025	1597	1105	I path inverted baseband input	–1.5		1.5
V_{BLO2}	1240	1010	1425	1105	Mixer bias voltage (duplicate)	–1.5	–0.6	0.5
VSS_{LOI}	827	1000	1150	1100	–5V I path LO amplifier supply	–5.5	–5	0
DI	630	1000	785	1100	I path detector bias	–1	0.8	1.5
VCI	187	965	387	1095	Lag phase shifter bias voltage	–2		1.5

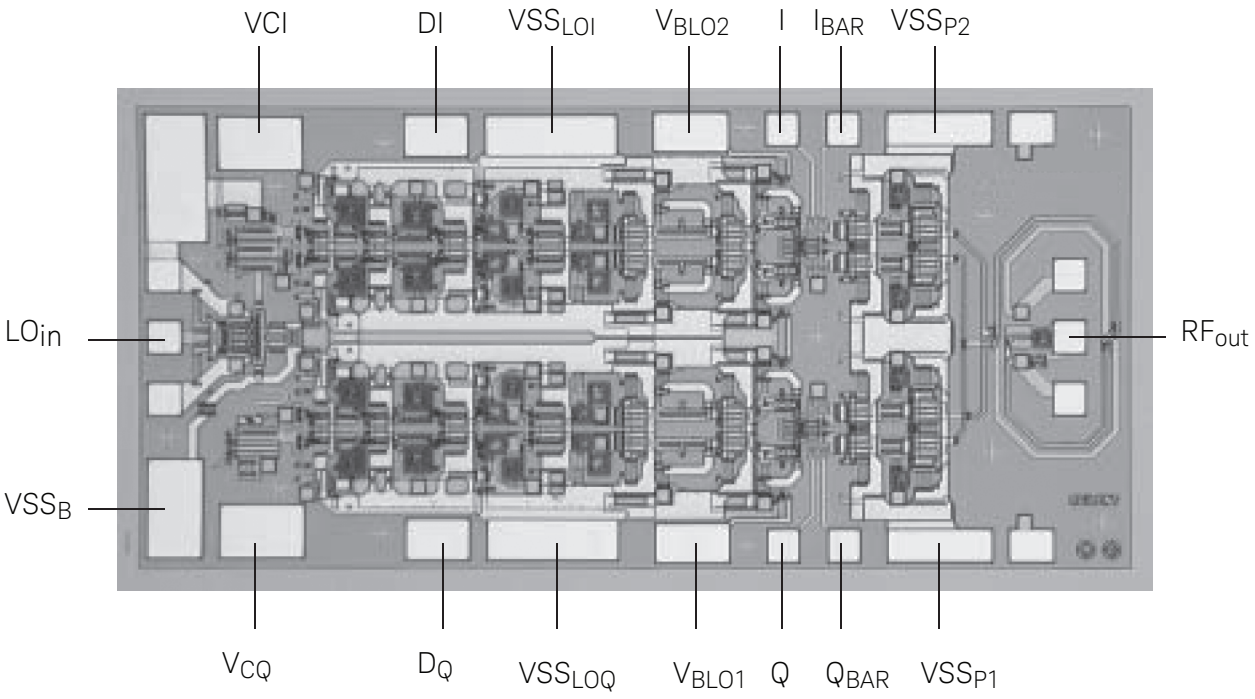


Figure 2. Bond pad identification

Supplemental Data

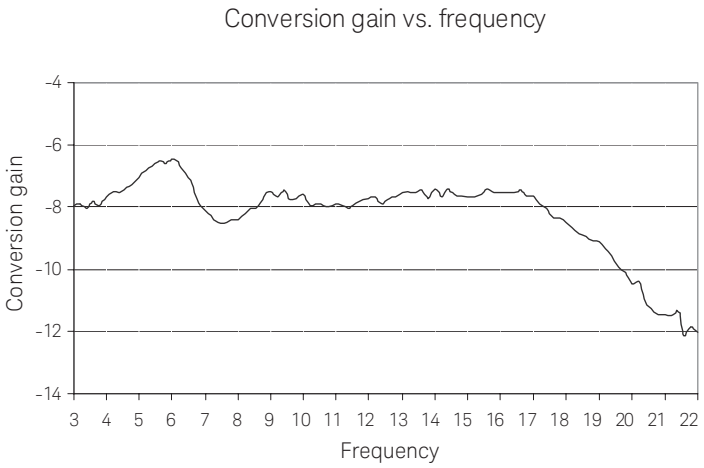


Figure 3. Conversion efficiency

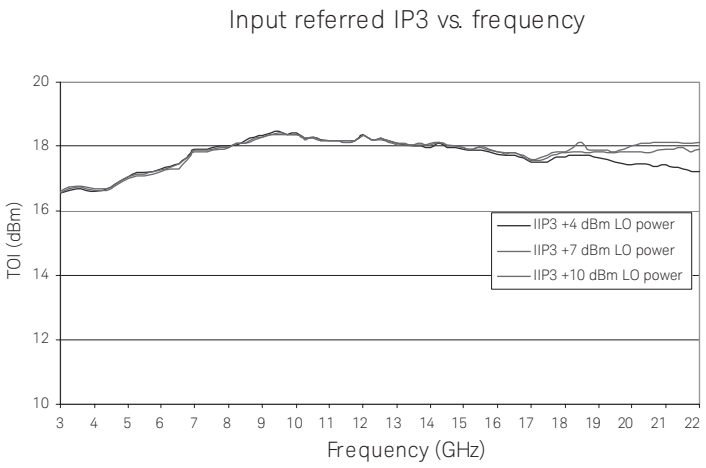


Figure 4. Input–referred IP3 vs. frequency

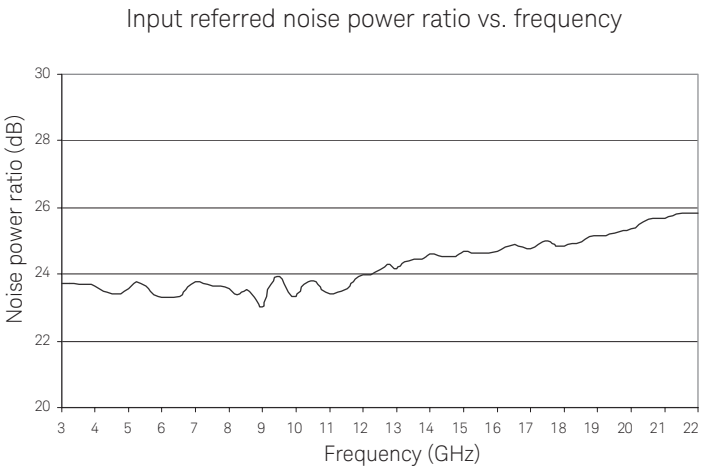


Figure 5. Input–referred noise power ratio

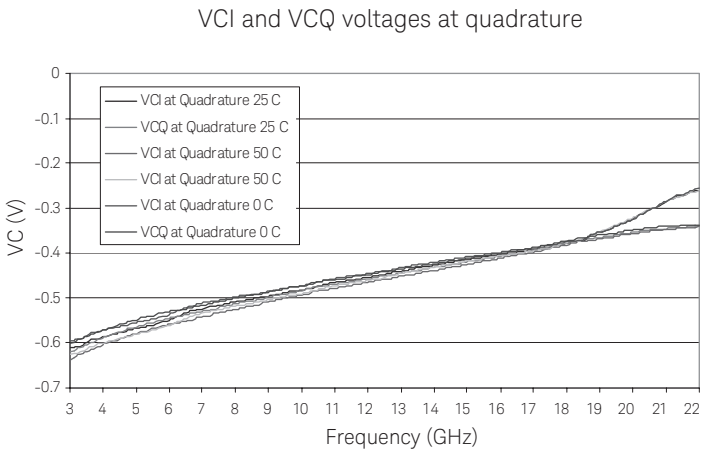


Figure 6. VCI and VCQ at quadrature

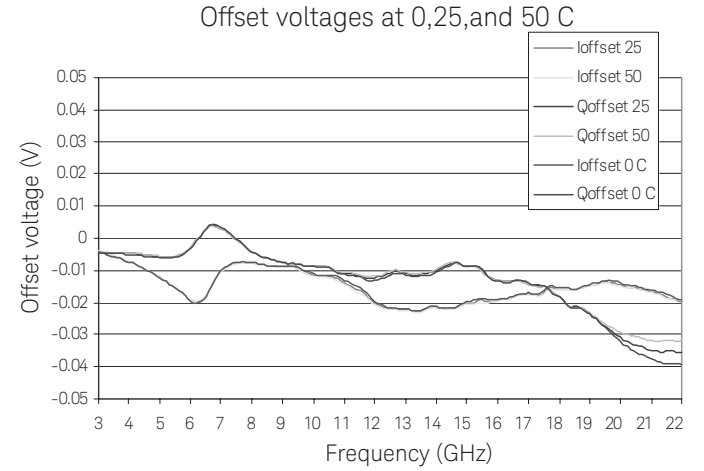


Figure 7. Offset voltages

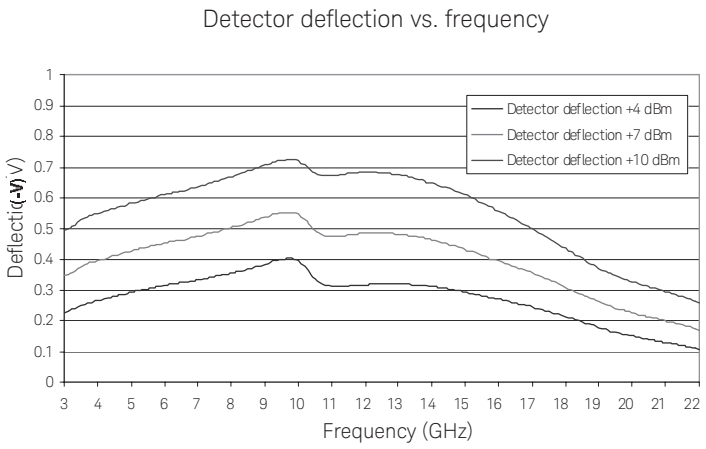


Figure 8. Detector deflection

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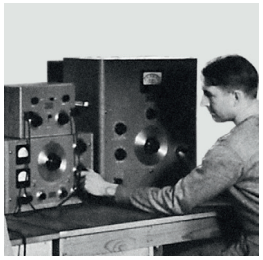

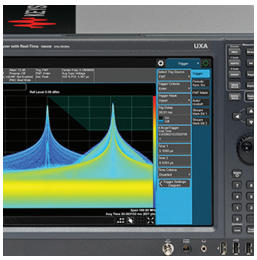

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The product described in this data sheet is RoHS Compliant. See *RoHS Compliance* section for more details.

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