Software
Release Note

Keysight i1000D Series In-Circuit Test Systems

Software Release Note v3.51p

KEYSIGHT TECHNOLOGIES

This document is Release Notes for Software v3.51p.

Supported Products

U9401B – i1000D Press Down ICT System

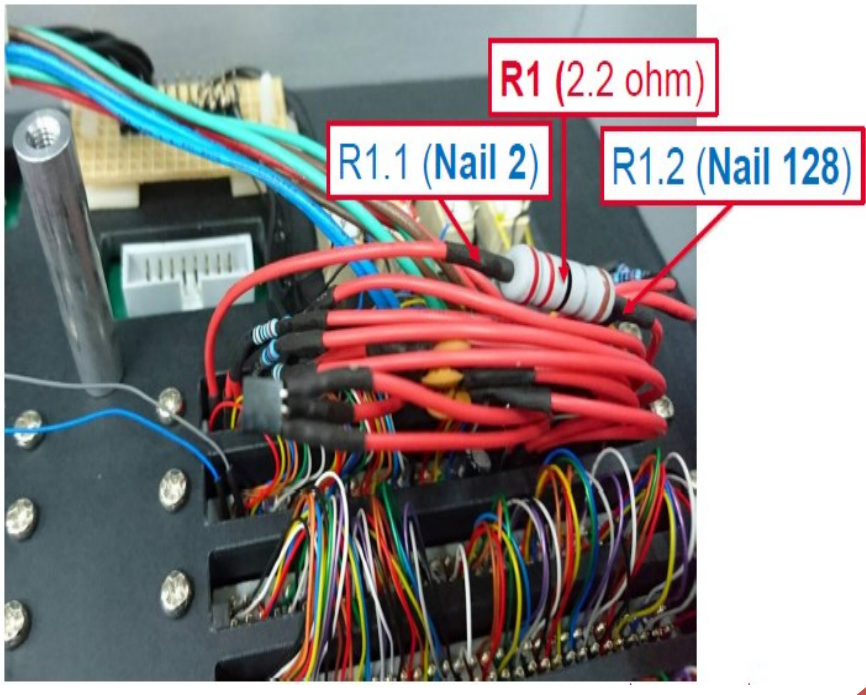
U9403A – Keysight Mini ICT System

U9405A – i1000D Small Foot Print ICT System (Inline/Offline)

What Is New?

PVF Enhancement:

We found current PVF doesn't support 4 wire test diagnostics. Including standard PVF and SFP PVF. In order to add 4 wire test diagnostics PVF must be modified and implement v3.51p new software. I also need CE who own PVF. Please help to do PVF modification. Later, TME will send out PVF modification document to you. Please note, after modifying PVF, old software and v3.51p will not compatible. Only v3.51p support 4 wire test function.



New “Abort” Function:

The “Abort” function can be interrupt the test when it test is failed.

At version 3.5.0pa, the “Abort” function is only abort test in the current group. In **Figure 1** sample, user can add an “A” in the Style column. When the 1%FS101 test is failed, the “Abort” function is activated. And the following resistor test will be cancelled.

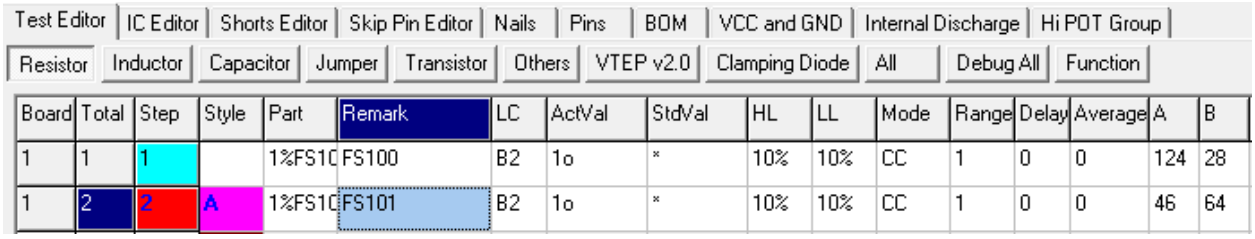


Figure 1 The “Abort” in editor interface at V3.5.0a

The program will run test start from next group. The next test group as defined in the test sequence till whole test sequence finish.

For example, in **Figure 2** sample, the R23 is added “Abort” in the style column. When the R23 test is failed, all of the resistor test will be escaped. The test will start from next test group, like as capacitor group.

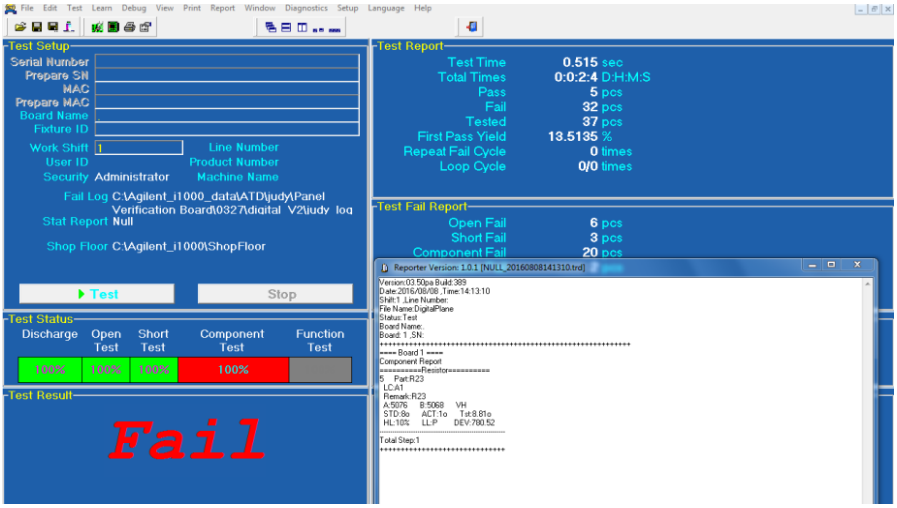


Figure 2 The "Abort" at operator interface at V3.5.0pa

The new "Abort" function is different from version 3.5.1p.

Compare with last "Abort" function. The new "Abort" will cancel all of test tab, not only one group.

As **Figure 3** sample, if any of component test is activated, whatever is resistor, capacitor or others, whole component test will be end.

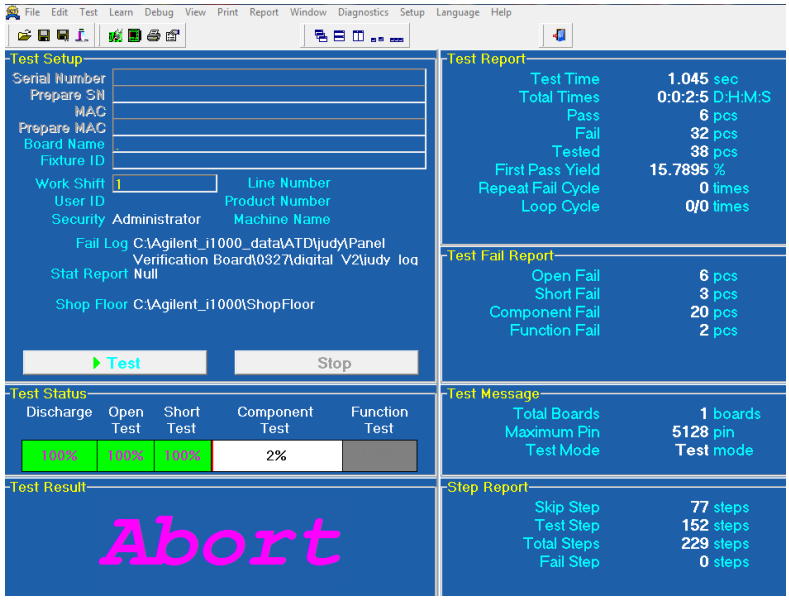


Figure 3 The "Abort" at operator interface at V3.5.1p

KEYSIGHT TECHNOLOGIES

Enhanced I2C Feature:

Before V3.5.1p, The i1000 provides the I²C programming GUI to test standard I²C EEPROM, like as 24Cxx serials. All of these EEPROMs have the fixed device select code (device type identifier and chip enable address).

Table 1 I²C EEPROM Device Select Code

	Device Type Identifier				*Chip Enable Address*			*R/W*
	b7	***b6***	***b5***	***b4***	***b3***	***b2***	***b1***	***b0***
Device Select Code	***1***	***0***	***1***	***0***	***E2***	***E1***	***E0***	***R/W***

For these EEPROM device's device type identifier is fixed to 1010. The chip enable address is according board's designer has different value.

The i1000 user can set the chip enable address in the I²C programming GUI for different chipset. And R/W is used operation list to select.

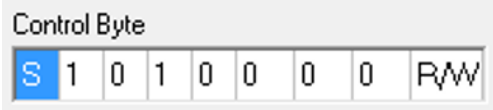


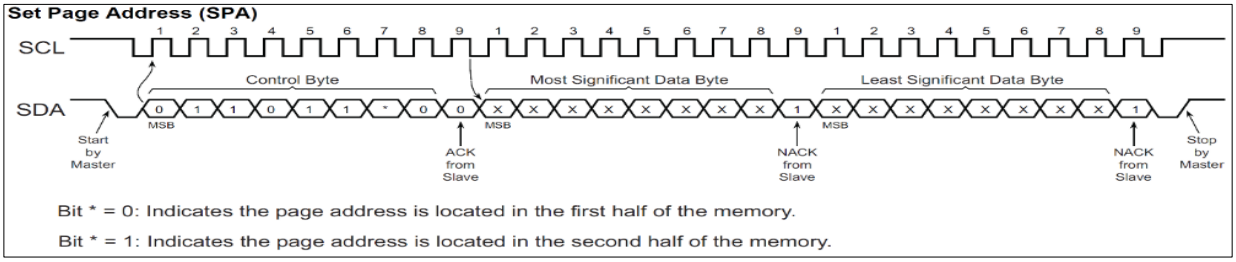
Figure 4 Control Byte Setting

User can view the device select code at I²C GUI. The upper control byte is fixed. User cannot modify it.

Hereto, all of contents are before V3.5.1p. The V3.5.1p has a new feature for I²C. After V3.5.1p, the I²C supports JEDEC JC42.4 (EE1004-v) Serial Presence Detect (SPD) Compliant.

The SPA has different control byte, after V3.5.1p, the i1000 provides the variable control byte, let user can define different control byte.

Example: AT34C04 programming



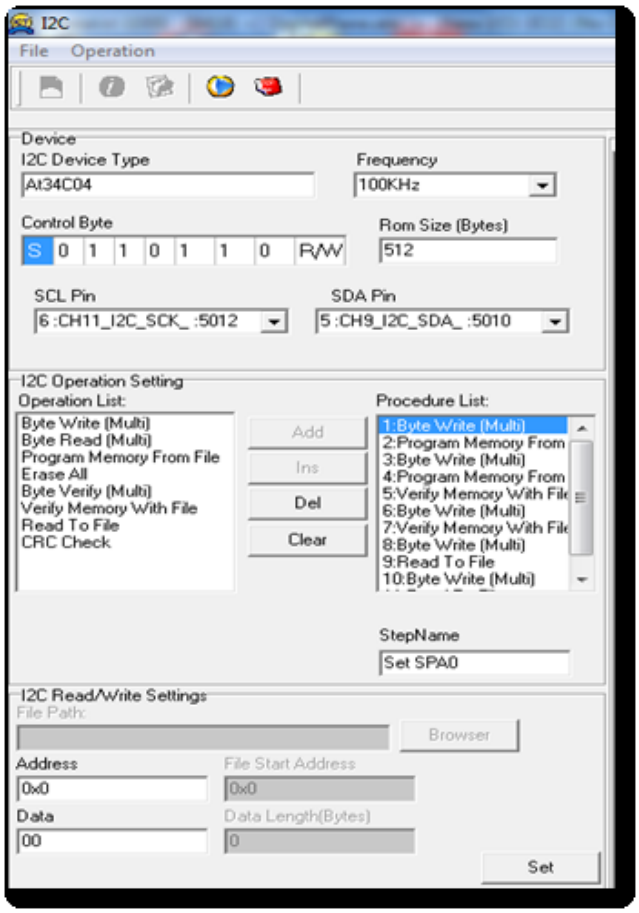


Figure 5 Set Page Address

Table 2 AT34C04 SPA

Set Page Address (SPA)	*Memory Address Location*
0 (6C)	***00h to 7Fh***
	80h to FFh
1 (6E)	***00h to 7Fh***
	80h to FFh

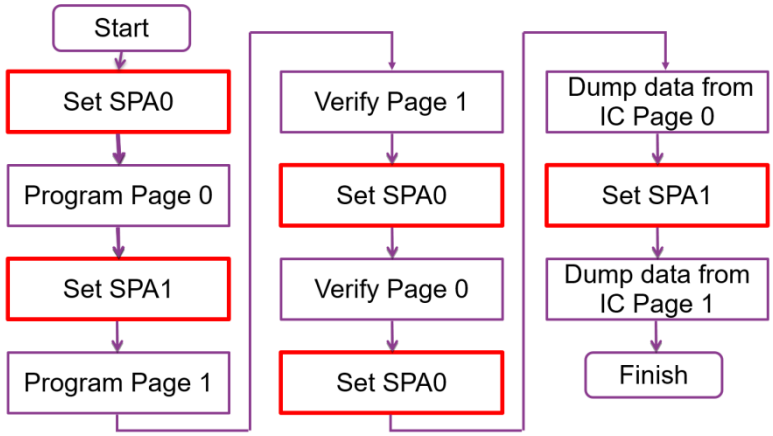


Figure 6 AT34C04 Programming Flow Chart

Support 10KHz For Testjet:

The original Keysight TestJet use 8KHz for learning and testing.

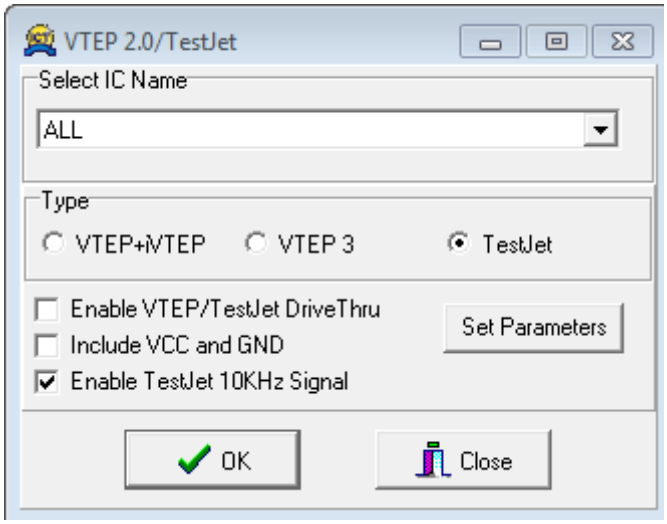


Figure 7 VTEP 2.0 with TestJet 10KHz Signal setting

After version 3.5.1p, provides a new 10KHz signal for TestJet. User can check/uncheck “Enable TestJet 10KHz Signal” option according upper picture.

Important: The new 10KHz signal is just use for the TestJet ONLY! The VTEP is also used 8KHz signal.

The original 8KHz signal’s EB option is 0. Please refer to

Capacitor | Jumper | Transistor | Others | VTEP v2.0 | Clamping Diode | All | Debug All | Function

Style	Part	Remark	LC	ActVal	StdVal	HL	LL	Mode	Range	Delay	Average	A	B	EA	EB	TestVal	DEV(%)
EP	U2	U2(1_1)	A1	*	159.9812m	479.94	79.990	TJ	1	0	0	5108	0	2	0	159.9812mV	161.8438
EP	U2	U2(2_2)	A1	*	95.375mV	286.12	47.687	TJ	1	0	0	5042	0	2	0	95.375mV	93.7813
EP	U2	U2(3_3)	A1	*	75.0781mV	225.23	37.539	TJ	1	0	0	5040	0	2	0	75.0781mV	78.6875
EP	U2	U2(4_4)	A1	*	59.3656mV	178.09	29.682	TJ	1	0	0	5038	0	2	0	59.3656mV	59
EP	U2	U2(5_5)	A1	*	47.7719mV	143.31	23.885	TJ	1	0	0	5036	0	2	0	47.7719mV	45.4688
EP	U2	U2(7_7)	A1	*	38.95mV	116.85	20mV	TJ	1	0	0	5034	0	2	0	38.95mV	40.4688
EP	U2	U2(8_8)	A1	*	50.5812mV	151.74	25.290	TJ	1	0	0	5032	0	2	0	50.5812mV	48.7813
EP	U2	U2(9_9)	A1	*	65.7031mV	197.10	32.851	TJ	1	0	0	5030	0	2	0	65.7031mV	64.3125

Figure 8 TestJet with 8KHz at EB Cell

If user used the 10KHz signal for TestJet test, the EB option will be change to 1. Please refer to **Figure 9**

Capacitor | Jumper | Transistor | Others | VTEP v2.0 | Clamping Diode | All | Debug All | Function

Style	Part	Remark	LC	ActVal	StdVal	HL	LL	Mode	Range	Delay	Average	A	B	EA	EB	TestVal	DEV(%)
EP	U2	U2(1_1)	A1	*	67.2312mV	201.69	33.615	TJ	1	0	0	5108	0	2	1	67.2312mV	68.6875
EP	U2	U2(2_2)	A1	*	40.4906mV	121.47	20.245	TJ	1	0	0	5042	0	2	1	40.4906mV	40.2813
EP	U2	U2(3_3)	A1	*	30.4156mV	91.246	20mV	TJ	1	0	0	5040	0	2	1	30.4156mV	31.25
EP	U2	U2(4_4)	A1	*	24.7687mV	74.306	20mV	TJ	1	0	0	5038	0	2	1	24.7687mV	26.3438
KEP	U2	U2(5_5)	A1	*	19.1687mV	57.506	20mV	TJ	1	0	0	5036	0	2	1		
KEP	U2	U2(7_7)	A1	*	16.6969mV	50.090	20mV	TJ	1	0	0	5034	0	2	1		
EP	U2	U2(8_8)	A1	*	20.8469mV	62.540	20mV	TJ	1	0	0	5032	0	2	1	20.8469mV	20.5313
EP	U2	U2(9_9)	A1	*	26.675mV	80.025	20mV	TJ	1	0	0	5030	0	2	1	26.675mV	27.5625

Figure 9 TestJet with 10KHz at EB Cell

Pins Test:

The pins test identifies fixture contact problems.

For the i1000D, similar to the Shorts test, Pins test is generated using a known good production board during the debug stage.

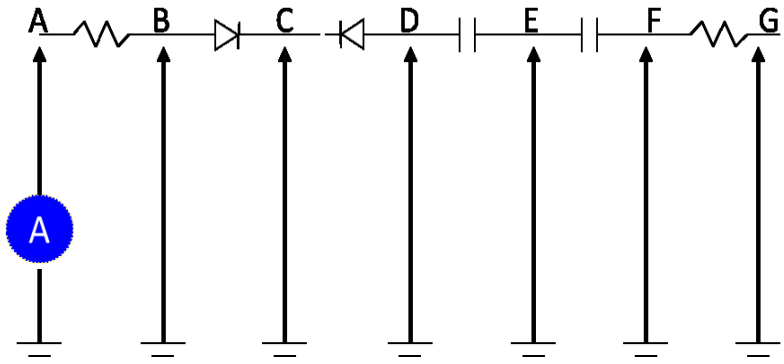


Figure 10 Simple Circuit for Pins Test

Given a simple circuit shown in **Figure 10,** there is a circuit board with Nodes “A” through “G” with different components in between the nodes.

The Pins test generation starts from the 1st nail

(normally ground) and 50uA current source is connected to it, while all the other nodes are connected to ground.

If there is current flow and the measured impendence is below 40k Ohm, then the probe is considered making good contact to the printed circuit board and this nail/node will be included in the Pins test group.

If there is no current flow and the measured impendence is at or above 40k Ohm, then the probe is not making contact and this nail/node will be excluded from the Pins test group.

Some nodes, like node “E” in this example, is isolated by 2 capacitors to other nodes. Therefore, there will not be any current flow even though the probe contact is good. Thus, it is excluded from Pins test group and won’t be covered by Pins test.

Once this node/nailed is done, it will be reconnected to ground and the next node/nail is moved from the ground connection to the source and testing continues until the last node/nail.

There are some special nodes like node “C”, where the node is on the cathode of the two diodes in the above example. As the two diodes are back-biased, the current source signal will not be propagated. When the software detects such a situation, the polarity of the source is reversed and there will ample current flow and the node is no longer isolated and can be tested. The node will be included in the Pins test group, yet in a special group called “Group Two”.

After being learned and saved to “ATD” file, the PCB can be tested following the same process. However, only the nodes in “Pins test group” will be executed and the “pass/fail” result will show up indicating whether the impendence is below or above 40K Ohm.

How to Learn and Debug Pins Test

Figure 11 shows the Pins test editor interface, where Pins test can be learned and debugged.

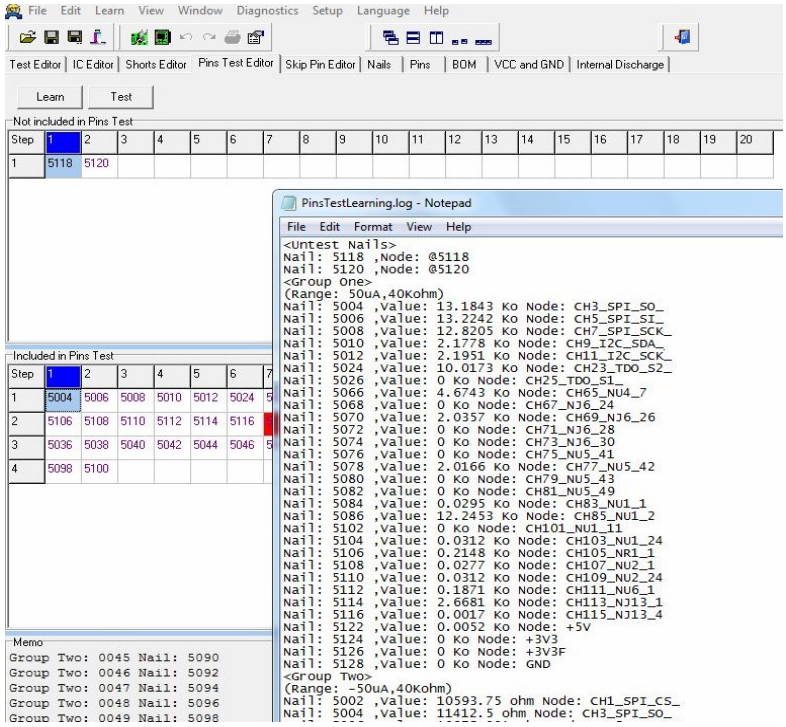


Figure 11 Pins Test Editor Interface (Learn)

For Pin tests, the current source value and measurement threshold are predefined and cannot be modified by the user, and the whole process is very simple and straight forward.

Once the Known good PCBA is pressed down to the fixture, the user can click the “Learn” button, and 3 areas in the interface will be updated. They are:

“Not included in the Pins Test” shows all the “isolated” nails which cannot be covered by pins tests.

“Included in the Pins Test” shows all the eligible nails which can be tested by pins tests.

“Memo” shows a sub group of nails which can be tested using revered current in Pins test.

Following every learning operation, a log file called “Pinstestlearning.log” will be created and placed at “/log” folder under the current board directory.

On top of the information available in the GUI, the file contains the measurement result for all the nails in the Pins test group.

This log file will be overwritten by subsequent new learning.

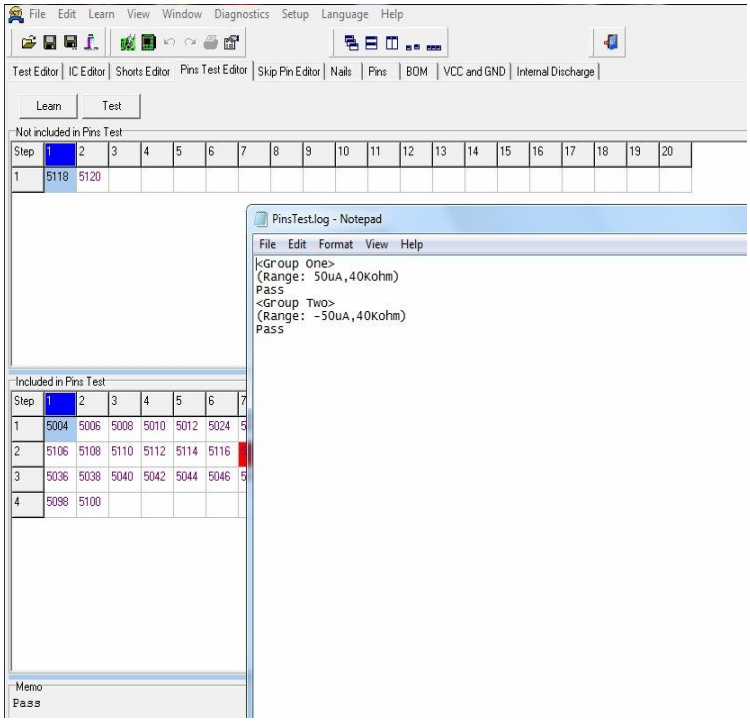


Figure 12 Pins Test Editor Interface (“test”)

To verify the Pins test, just clicking the “Test” button as shown in **Figure 12**. The “Memo” section will show the test result and a new log file called “Pinstest.log” will be created at the “/log” of the current board directory.

Enable Pins Test in Production

To do this, Pins test needs to be enabled in the system setting by following the path in the GUI (As shown in): “Setup→Parameters→Test→Enable Pins Test”

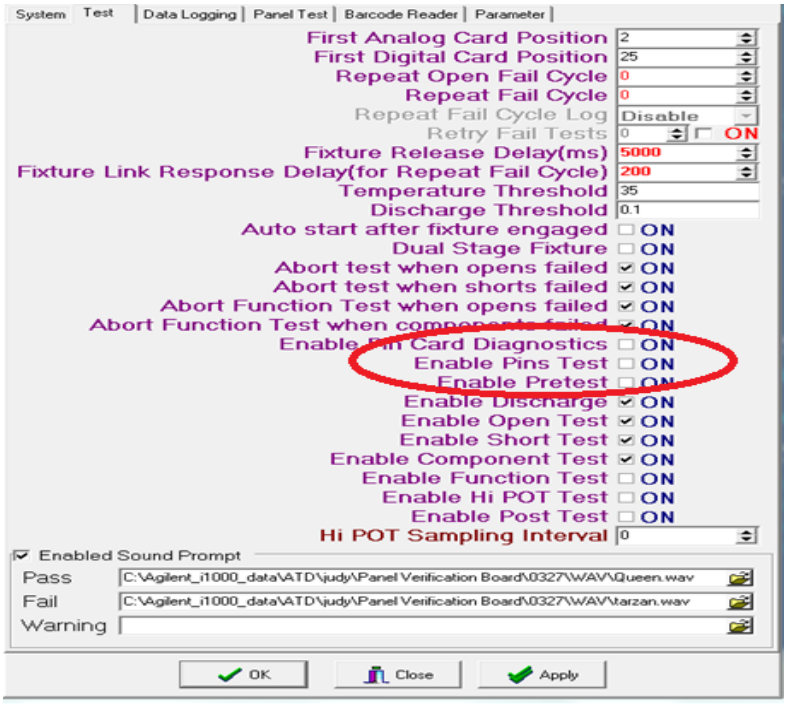


Figure 13 Enable Pins Test

Shorts Learning Log File:

During shorts learning and testing, if there is big capacitor between 2 nodes in the circuitry, and the settling delay is set too low, the system may measure a low impendence between these 2 nodes.

As a result of this, after learning, these two nodes will be included in a shorts group. If there is a real shorts between them, the system will not be able to detect it.

To help the user, i1000 software will create a log file called “shorts_verify.log” after shorts learning is done.

This file is located at the “log” folder under the board directory, and will be overwritten each time shorts are learned.

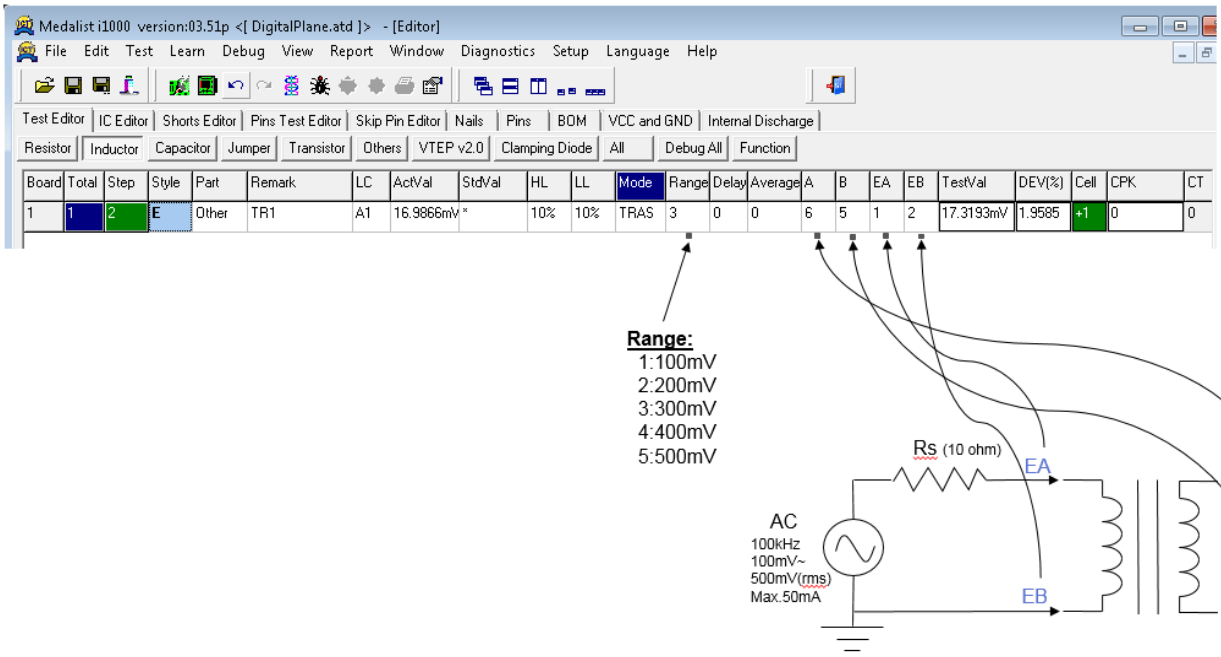
```
==========================================================

Capacitors in Short Pin Group:

==========================================================

CP7        470uF      A:51 (SPG:4)
                      B:71 (SPG:4)

==========================================================

Resistors in Short Pin Group:

==========================================================

R10        10o        A:22 (SPG:5)
                      B:28 (SPG:5)
```

Figure 14 Example of “shorts_learning.log” file

In the example file shown in **Figure 14**, there is big capacitor “CP7” between nails “51” and “71”. After learning, these nodes are assigned as SPG 4.

After checking this file, the user can modify the “settling delay” parameter, and re-run learning. Eventually, these 2 nodes can be removed from the shorts group.

Transformer Mode:



An AC constant voltage source is used to test transformer. The measurement circuit and test setup are arranged as follows:

The AC signal source is 100 kHz fixed frequency. Five of voltage (Vrms) levels 100 mV, 200 mV, 300 mV, 400 mV and 500 mV are used in this measurement that correspond with range settings 1, 2, 3, 4, and 5 respectively.

NOTE:

The test resources for DUT inputs EA, EB and outputs A,B MUST from the different sense group!! Please refer:

C:\Agilent_i1000\INI\Sense_ProvideMapping.ini

to select the proper resources.

For Example,

The Analog board No.1, from

"***Sense_ProvideMapping.ini***":

Group 1 = 1,2,3,4, 9,10,11,12, ...

Group 2 = 5,6,7,8, 13,14,15,16, ...

Correct resources assignment:

A, B : Pins 1,2

EA, EB : Pins 5,6

(Pins 1,2 and Pins 5,6 are NOT the same group)

Wrong resource assignment:

A, B : Pins 1,2

EA, EB : Pins 3,4

(Pins 1,2,3 and 4 are in the same group)

Program Support Script:

Introduction

Program Control Language is created by Keysight Technologies as an enhancement to the i1000 Test Program capability. The i1000 software is a simple test sequencer which does not have much capability to allow programmers to perform logic operations in between test steps. Though features such as EXT mode is included to allow external script executions, there is still a lack of flexibility as the external scripts does not have access to the test step parameters of the test program. Therefore external scripts can only perform operations that are independent of the test program, for example reformatting test data log files at the end of the test cycles or communication with external servers to upload test results and logs.

Taking the i1000 software forward to the next level, a mode called Program Control Script (PCS) is introduced. Programmer can create scripts in PCL and execute them in the PCS mode within the test program. PCS mode is available in all test groups of the i1000 software, and it interacts and transfer values between the script and the test program directly. This allows programmers to make logical operations based on the inputs from the test programs. One good example is that programmer can now check the version of the DUT in the fixture by

executing certain test steps using the PCS script and then selectively enable the appropriate groups of tests to run. This is commonly known as automatic board versions control.

PCL is developed with high similarity to C Programming, one of the commonly used programming language in the world. This allows an easier learning path for programmers whom are already familiar with C Programming. Programmers will find themselves very comfortable with the structure and the commands and syntaxes while using PCL. Inputs and Outputs linkage to the i1000 test program is added to PCL to allow programmers to easily access the values of fields in any test steps within the test program (ATD).

While PCL contains similarity to C Programming, it does not have the same level of functions and commands like C Programming. PCL is aimed to provide the programmers with the ability to work with the test parameters and values of the test program. Therefore, it contains a subset of commands that is sufficient to create a small non-GUI based script.

PCL is Program Control Language. This is the name of the language which the programmer will use to create the script for the PCS step.

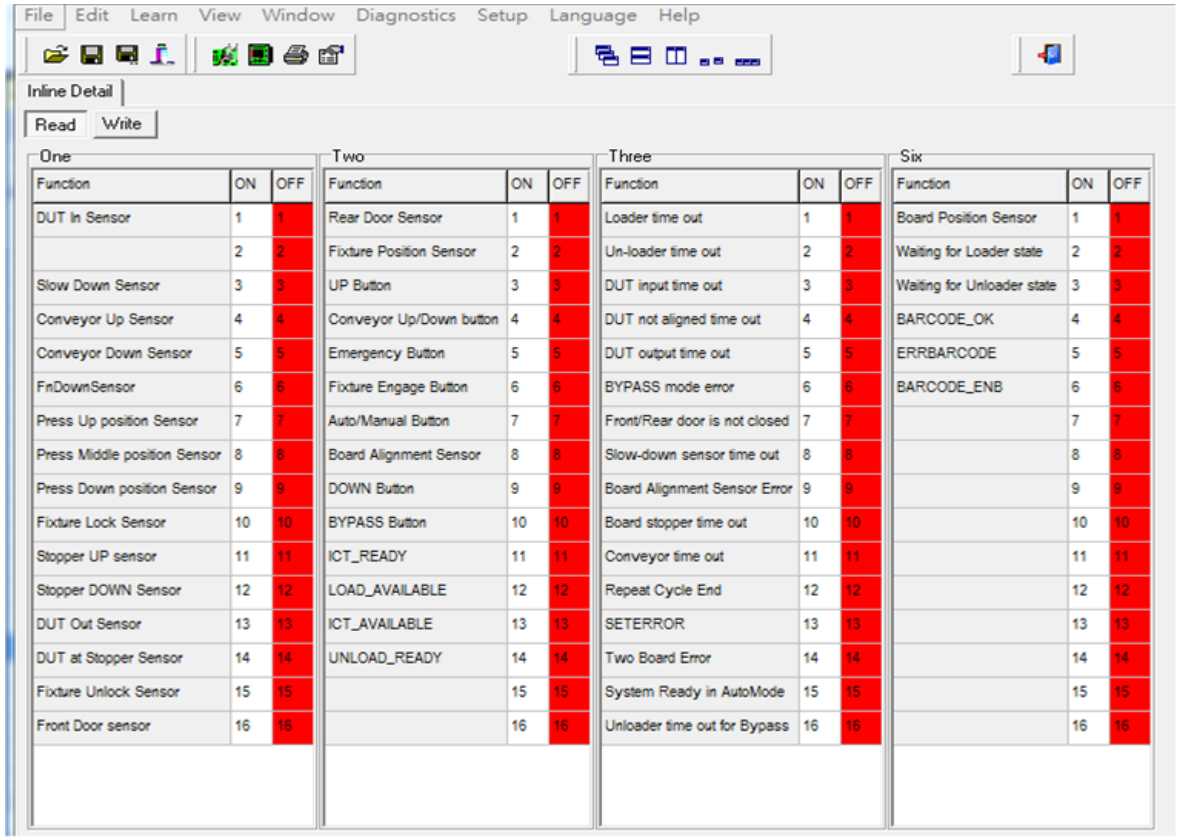
PCS is Program Control Script. This is the test mode that will execute the script in the test program.

ATD is the test program file of the i1000 that contains all the test steps

EXT is External Script mode. This is a test mode offered by the i1000 software which will allow user to assign and execute an EXE or BAT files.

Diagnostics GUI Enhancement:

Enhanced Diagnostics GUI show whole signal name for each signal of SFP system



One

Function	ON	OFF
DUT In Sensor	1	1
	2	2
Slow Down Sensor	3	3
Conveyor Up Sensor	4	4
Conveyor Down Sensor	5	5
FnDownSensor	6	6
Press Up position Sensor	7	7
Press Middle position Sensor	8	8
Press Down position Sensor	9	9
Fixture Lock Sensor	10	10
Stopper UP sensor	11	11
Stopper DOWN Sensor	12	12
DUT Out Sensor	13	13
DUT at Stopper Sensor	14	14
Fixture Unlock Sensor	15	15
Front Door sensor	16	16

Two

Function	ON	OFF
Rear Door Sensor	1	1
Fixture Position Sensor	2	2
UP Button	3	3
Conveyor Up/Down button	4	4
Emergency Button	5	5
Fixture Engage Button	6	6
Auto/Manual Button	7	7
Board Alignment Sensor	8	8
DOWN Button	9	9
BYPASS Button	10	10
ICT_READY	11	11
LOAD_AVAILABLE	12	12
ICT_AVAILABLE	13	13
UNLOAD_READY	14	14
	15	15
	16	16

Three

Function	ON	OFF
Loader time out	1	1
Un-loader time out	2	2
DUT input time out	3	3
DUT not aligned time out	4	4
DUT output time out	5	5
BYPASS mode error	6	6
Front/Rear door is not closed	7	7
Slow-down sensor time out	8	8
Board Alignment Sensor Error	9	9
Board stopper time out	10	10
Conveyor time out	11	11
Repeat Cycle End	12	12
SETERROR	13	13
Two Board Error	14	14
System Ready in AutoMode	15	15
Unloader time out for Bypass	16	16

Six

Function	ON	OFF
Board Position Sensor	1	1
Waiting for Loader state	2	2
Waiting for Unloader state	3	3
BARCODE_OK	4	4
ERRBARCODE	5	5
BARCODE_ENB	6	6
	7	7
	8	8
	9	9
	10	10
	11	11
	12	12
	13	13
	14	14
	15	15
	16	16

Bug Fixed List

ID	*Description*
491648	Add memo for columns [Range]/[EA]/[DAV]/[EDAV] of [SPOT] mode ◦
491580	Fix SPI mode report "Data address is bigger than file!" issue when loading test hex file.
491576	Fix [SPI]/[I2C] [Read to file] issue when using nail 5062/5004(Reverse Plane).
491574	[Overall Result Log] untested item should show “Skip”.
491558	Fix [SPS] report wrong [OV]/[OC] message.
491557	Fix [SPS] report [OV]/[OC] at wrong column in Operator Mode.
491554	Fix right-click on Function step cannot display the “sort status”.
491460	PCS only works in Function group. All other groups does not work even when the mode is present.
490822	Add memo for "OUTP" mode.
490471	change the memo: “STP Delay Time” to “ICT Ready Delay Time”
490357	Add "PCS" description to Memo.
489002	Fix Board view pops up error message very often when nail locater is on the wrong side
488033	Fix i1000 Calibration - Frequency measurement issue
488008	Fix I2C debug GUI cannot keep “hex format”.
487873	SDA use nail 5004, SCL use nail 5002, Read to file data are always “00”.
485577	Fix 6700 "CT" does NOT work correctly
485195	Panel Level Style M must be deleted automatically when user select a part name with a board number
482642	Shopfloor Datalog missing Failure information
482641	Shopfloor data log incorrectly generated due to wrong settings in INI file
482045	Pins test Table changed to Editable.
481208	V350pa will still display error message when we insert a new step into the panel program.
480516	Mini ICT: The first 6 component always test failed when digital card installed.

480303	style "Abort" function need to abort whole test sequence in software
472478	software always report open fail in Overall data log file when short test fail
471750	Digital debug GUI always show "supplemental library error" when modify any vector.
463765	When device number in spi/i2c/bscan test files are not matched in ATD, Software will crash during load ATD program
462503	TPG need to analyze 4 wire sensing on duplicate nails
460163	Fix TPG Net name too long cause display issue.
451828	When receive delay set to 400ns in library, software will not set to 1000ns.
419649	i1000_Abort didn't work. I1000_start command with PDU status UP also didn't raise the PDU
461006	TPG does not process 4wire measurements for part library.
471064	TPG Remote sense resource waste resources
480524	The new "Mini ICT" system type will cause shorts test fail when the new version ATD tests by old version sw.
477273	fail log file should support single file when user test panel board
470732	Add "N"(no reset) style to CET
485923	Add memo for "TRAS" mode
484673	BSDL 內無"BYPASS" command 時，TPG & library assignment need to pop-up "Missing [BYPASS] command" Error message, generate .err (error log file).
483430	Software should use page write time only when user setup byte and page write time
491638	[Overall Result Log] should add (Skip) mark for untested items.
491646	I1000 software auto-detect N67xx (USB port), and auto fill-in "1st SPS Serial Number".
491659	Remove i1000 SFP [I/O Cards] redundant data.
486029	Add PCS mode missing information in Memo.
356621	Change inline SFP signal names in GUI for better understanding

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