XE7-class M8040A 64 Gbaud High-Performance Bit Error Ratio Tester (BERT)

Master your next design

Data Sheet and Technical Overview – Version 12.5

At a Glance

Keysight Technologies M8040A is a highly integrated BERT for physical layer characterization and compliance testing. It supports pulse amplitude modulation 4-level, 3-level (PAM4, PAM3) and non-return-to-zero (NRZ) signals, and symbol rates up to 64 Gbaud (corresponding to 128 Gbit/s). It can be used for testing devices designed for 400/200 GbE, 800G, OIF CEI-56G and CEI-112G, PCIe 64/32/16/8/5 GT/s, USB4 Version 2.0, USB 3.2, USB4, Thunderbolt 3 and Thunderbolt 4.

The M8040A BERT's true error analysis provides repeatable and accurate results, optimizing the performance margins of your devices.



KEYSIGHT

Table of Contents

List of Acronyms 3

Introduction 6

Specifications for M8045A and M8046A Modules and M8057A/B Remote Head 15

Specifications for Pattern Generator Module M8045A and Remote Head M8057A/B 16

Jitter Specifications 27

External Interference (RI/SI) Sources 31

Adjustable Intersymbol Interference (ISI) 33

External ISI Channel Boards 35

Pattern Sequencer, Filler Symbol Filtering, and Interactive Link Training 37

Specifications for M8046A Analyzer Module 46

User Interface and Remote Control 59

General Characteristics and Physical Dimensions 66

Remote Head M8057A/B 67

Specification Assumptions 68

Ordering M8040A High-Performance BERT 69

Related Keysight Literature 72

Confidently Covered by Keysight Services 74

List of Acronyms

Acronym	Full Name / Description
AC	Alternating Current
AWG	Arbitrary Waveform Generator
AXIe	AdvancedTCA Extensions for Instrumentation (modular instrumentation platform)
BER	Bit Error Ratio
BERT	Bit Error Ratio Tester
BUJ	Bounded Uncorrelated Jitter
CCIX	Cache Coherent Interconnect for Accelerators
CDR	Clock Data Recovery
CEI	Common Electrical I/O (OIF)
CTLE	Continuous-Time Linear Equalizer
CTS	Compliance Test Specification
DC	Direct Current
DCA	Digital Communications Analyzer (Keysight product name for sampling oscilloscopes)
DCI	DUT Control Interface
DDR	Double Data Rate (memory interface)
DFE	Decision Feedback Equalizer
DJ	Deterministic Jitter
DUT	Device Under Test
ESD	Electrostatic Discharge
FBE	First Bit Error
FBER	First Bit Error Ratio (PCIe 6.x/7.x metric defined by the PCI-SIG)
FEC	Forward Error Correction
FFE	Feed-Forward Equalizer
FIR	Finite Impulse Response
FLR	Frame Loss Ratio
GAUI	Gigabit Attachment Unit Interface
GBd / Gbaud	Gigabaud (10^9 symbols per second)
GbE	Gigabit Ethernet
GDDR	Graphics Double Data Rate (memory interface)
GND	Ground
GT/s	Gigatransfers per Second
GUI	Graphical User Interface
HDR	High Data Rate (InfiniBand)
HF	High Frequency
IEEE	Institute of Electrical and Electronics Engineers
IQ	In-Phase and Quadrature (modulation)
ISI	Intersymbol Interference
JTF	Jitter Transfer Function
KR4	Reed-Solomon FEC RS(528,514) used for 100G NRZ Ethernet interfaces

Acronym	Full Name / Description
LF	Low Frequency
LFPS	Low-Frequency Periodic Signaling
LPDDR	Low-Power Double Data Rate (memory interface)
LPO	Linear Pluggable Optics
LTSSM	Link Training and Status State Machine
MIPI	Mobile Industry Processor Interface
mUI	milli-Unit Interval
NDR	Next Data Rate (InfiniBand)
NRZ	Non-Return-to-Zero
OIF	Optical Internetworking Forum
OJTF	Observed Jitter Transfer Function
OS	Ordered Set
PAM3/4/6/8	Pulse Amplitude Modulation (3/4/6/8 levels)
PCIe	Peripheral Component Interconnect Express
PCS	Physical Coding Sublayer
PG	Pattern Generator
PHY	Physical Layer
PJ	Periodic Jitter
PLL	Phase-Locked Loop
PON	Passive Optical Network
ppm	parts per million
PRBS	Pseudo-Random Bit Sequence
PRTS	Pseudo-Random Ternary Sequence
QPRBS	Quaternary Pseudo-Random Bit Sequence
RI	Random Interference
RJ	Random Jitter
RMS	Root Mean Square
rSSC	Residual Spread Spectrum Clocking
Rx	Receiver
S/N	Serial Number
SAS	Serial Attached SCSI
SATA	Serial ATA (Serial Advanced Technology Attachment)
SCPI	Standard Commands for Programmable Instruments
SER	Symbol Error Ratio
SI	Sinusoidal Interference
SJ	Sinusoidal Jitter
SKP	Skip (ordered set used in PCIe and USB for clock compensation)
SMA	SubMiniature Version A (connector)
sRJ	Spectrally Distributed Random Jitter
SSC	Spread Spectrum Clocking
SSPRQ	Short Stress Pattern Random Quaternary
TBT	Thunderbolt

Acronym	Full Name / Description
Tx	Transmitter
TxEQ	Transmitter Equalization
UI	Unit Interval
USB	Universal Serial Bus
UXR	Ultra-High-Bandwidth Real-Time Oscilloscopes (Keysight product name)
Vpp	Peak-to-Peak Voltage
VSR	Very Short Reach
XML	eXtensible Markup Language

Introduction

M8000 Series of BER Test Solutions

Simplified time-efficient testing is essential when you are developing next-generation computer, consumer, or communication devices.

The Keysight M8000 Series is a highly integrated BER test solution for physical layer characterization, validation, and compliance testing.

With support for a wide range of data rates and standards, the M8000 Series provides accurate, reliable results that accelerate your insight into the performance margins of high-speed digital devices.

Shift into high gear with the M8000 Series and take the design verification express lane.



M8020A J-BERT Platform	M8040A BERT Platform	M8050A BERT Platform
M8041A, M8051A, M8062A	*M8045A, M8046A, M8054A*	*M8009A, M8042A. M8043A, M8053A*
Up to 16 Gb/s (32 Gb/s with MUX) NRZ	**Up to 64 GBd NRZ and PAM3/4**	**Up to 120 GBd NRZ and PAM3/4/6/8**

Figure 1. The M8000 Series BER Test Solution is highly integrated and scalable to address the test challenges of the next generation of high-speed digital receiver test.



Figure 2. The M8000 Series BER test solution is highly integrated and scalable to address the test challenges of the next generation of high-speed digital receiver test.

M8040A High-Performance BERT 64 Gbaud – Simplifies accurate receiver characterization of devices operating up to 32 and 64 Gbaud with NRZ, PAM3 and PAM4 signals

The M8040A high-performance BERT 64 Gbaud extends the M8000 Series for 400G data center interconnect testing and PCIe 4/5, CCIX, SAS, USB 3.2, USB4, TBT3/4 and MIPI M-PHY receiver characterization.

M8040A BERT Platform Key Features

- Data rates from 2 to 32 and 64 Gbaud
- PAM4, PAM3 and NRZ selectable from the user interface
- Built-in 5-tap transmitter FFE with multiple presets to compensate for loss
- Integrated and calibrated jitter injection: RJ, LF and HF PJ (multi-tone, sinusoidal), BUJ, clk/2 jitter, sRJ, rSSC, and SSC (spread spectrum clocking)
- Forward Error Correction (FEC) encoding and error insertion for testing DUTs with FEC decoder
- Two pattern generator channels per module to emulate an aggressor lane
- Linearity tests with adjustable PAM4 and PAM3 levels
- Interactive link training for PCI Express 2.5/5/8/16/32/64 GT/s
- Interactive link training for USB 3.2, 5 Gb/s and 10 Gb/s, x1 and x2
- New SSC clock switch profile supported according to CTS V1.02
- SKP OS filtering for PCI Express 2.5/5/8/16/32/64 GT/s and SKP OS filtering for USB 3.2
- PCIe pre-coder support
- USB4 Version 2.0 pre-coder and scrambler support
- USB4 Version 2.0 inverse pre-coder support
- USB4 LFPS support
- ALIGN filtering for SATA 3G/6G and SAS 3G/6G/12G
- Short connections to the DUT with remote heads for the pattern generator
- True PAM4 error detection in real time for low BER levels
- Built-in and adjustable equalization to re-open closed eyes
- Integrated clock recovery and control of external clock recovery units N1076A/B, N1077A, N1078A
- RI and SI level interference injection via M8054A interference source and M8194A/95A/96A AWGs
- Graphical user interface and remote control via M8000 system software
- Real-time error distribution analysis to debug burst error conditions
- Reference clock multiplier support with SSC extended to 64 Gbaud

Applications

The M8040A can be used for receiver (input) testing for many emerging interconnect standards, such as:

- IEEE 802.3bs 400 and 200 Gigabit Ethernet (200GAUI, 200GBASE, 400GAUI, 400GBASE)
- IEEE 802.3bj 100 Gigabit Ethernet
- IEEE 802.3cd 50, 100 and 200 Gigabit Ethernet
- IEEE 802.3ck 400 Gigabit Ethernet
- OIF CEI-56G and CEI-112G (NRZ and PAM4 versions)
- 25G and 50G PON

- PCI Express 64/32/16/8/5/2.5 GT/s
- DDR, LPDDR and GDDR7 memory interfaces
- SAS
- USB 3.2, USB4 and USB4 Version 2.0 and Thunderbolt 3/4
- DisplayPort 2.1
- MIPI M-PHY interface
- 64G/112G Fibre Channel
- InfiniBand HDR and NDR
- Proprietary interfaces for chip-to-chip, chip-to-module, backplanes, repeaters, and active optical cables, operating up to 64 Gbaud.

Highest level of integration streamlines receiver test setups

With the M8040A, all critical test capabilities for input/receiver (RX) characterization are built in. The pattern generator module provides calibrated and integrated jitter sources and de-emphasis to emulate the transmitter (TX) and to compensate for channel loss in the test setup. In addition, the M8040A provides an internal clock synthesizer and a second pattern generator output channel to emulate an aggressor lane.

The analyzer provides true PAM4 and NRZ error analysis in real time and full sampling to measure down to very low BER and SER.

This high level of integration with the M8040A makes the receiver test setup connections easier and more robust. Set up and debug time are shortened, calibration is simpler, and the frequency of re-adjustments is reduced, resulting in a more efficient use of overall test time.

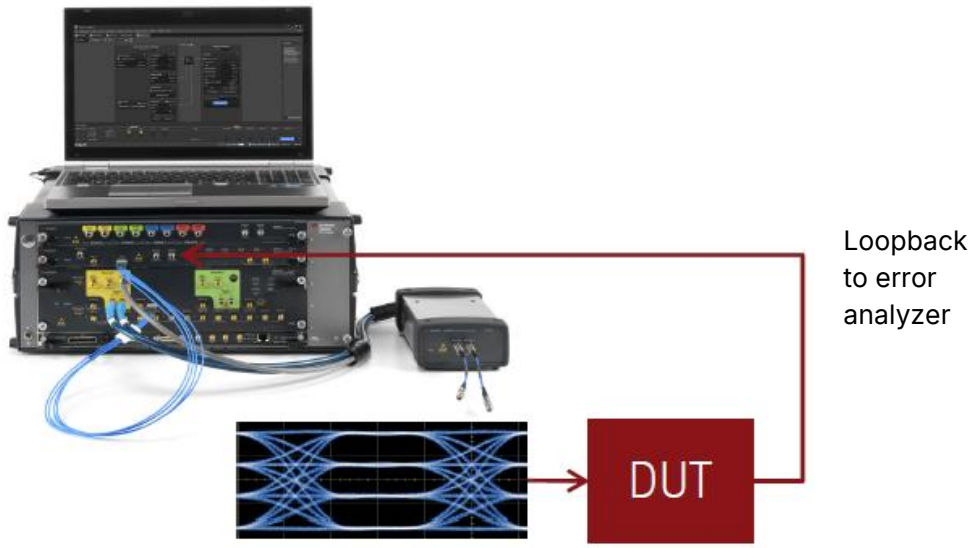


Figure 3. The M8040A streamlines complex receiver test setups. Each of the 1 or 2 pattern generator channels provides built-in de-emphasis, jitter sources, and a remote head to reduce the distance between the generator output and the DUT test board. The full sampling error analyzer can detect errors in real time for NRZ, PAM3 and PAM4 signals without the need to split up the PAM4 signal for multiple error detector channels.

Repeatable and Accurate Results with M8040A

The M8040A high-performance BERT provides clean NRZ, PAM3 and PAM4 signals up to 64 Gbaud with fast transitions and low intrinsic jitter. The remote head concept of M8040A with the short 1.85 mm cables brings the performance close to the device under test, minimizing signal degradations caused by lossy channels.



Figure 4. The remote head M8057A/B is required for each channel and is required for NRZ, PAM3 and PAM4 signals. It contains an adjustable gain amplifier without re-timer. Users can select NRZ, PAM3 or PAM4 coding and de-emphasis tap settings from the user interface with no need to reconnect cables. The cable between the remote head and the module is 0.85 m long. This allows positioning the remote head closely to the test board for the device under test.

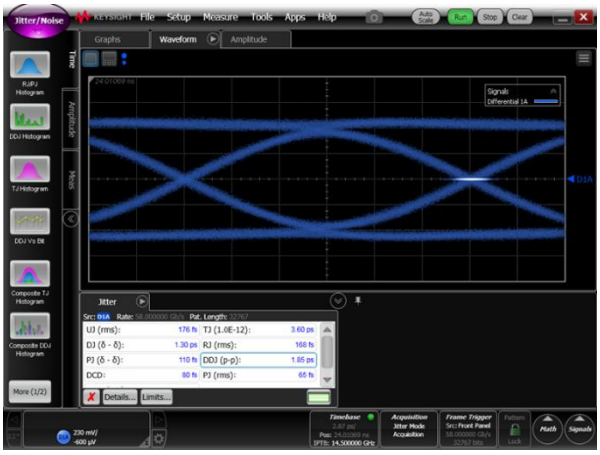


Figure 5. Clean 58 Gbaud NRZ output signal of pattern generator module M8045A with remote head M8057B using the internal clock source with 600 mV output amplitude and PRBS 2^{15}-1. Measured with Infiniium DCA-X 86100D with N1045A and manual de-emphasis adjustment.

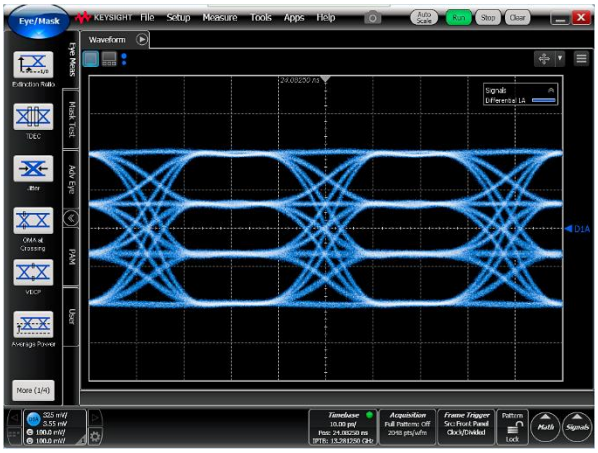


Figure 6. Clean 26.5625 Gbaud PAM4 output signal of pattern generator module M8045A with remote head M8057B using the internal clock source with 600 mV output amplitude and PRBS 2^{15}-1. Measured with Infiniium DCA-X 86100D and N1045A and manual de-emphasis adjustment.

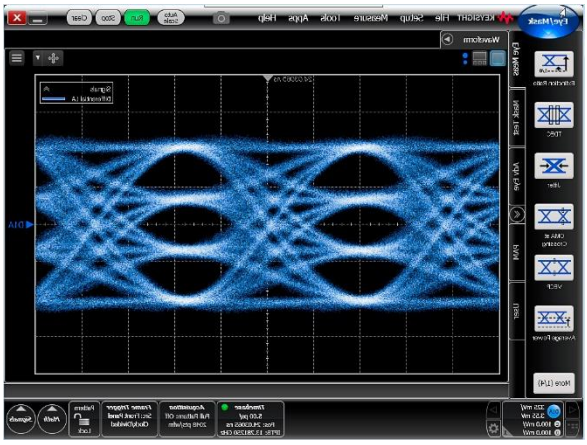
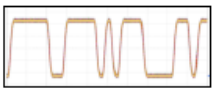
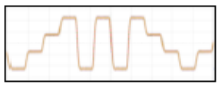


Figure 7. Clean 53.125 Gbaud PAM4 output signal of pattern generator module M8045A with remote head M8057B using the internal clock source with 600 mV output amplitude and PRBS 2^{15}-1. Measured with Infiniium DCA-X 86100D and N1045A and manual de-emphasis adjustment.

Emulate Stress Conditions for NRZ, PAM3 and PAM4 Input Tolerance Testing with M8040A

M8040A provides all capabilities required for input tolerance testing:

- 1 or 2 channels. The second channel can be used as an aggressor lane to emulate crosstalk effects
- Data rates are adjustable from 2 Gb/s NRZ up to 64 Gbaud PAM3 or PAM4, selectable as NRZ, PAM4, or PAM3
- Algorithmic PRBS, QPRBS, PRTS and memory-based patterns, pattern sequencer with loops, error injection at the bit level (NRZ patterns) and at the symbol level (PAM3 and PAM4 patterns)
- Generates FEC-encoded patterns with pre-coder on 1 lane to test DUTs with FEC decoder
- Built-in and calibrated jitter sources that can be used simultaneously: Random Jitter (RJ), multi-UI low-frequency jitter, multi-tone high-frequency jitter, BUJ, clk/2 jitter, Spread-Spectrum Clocking (SSC), Residual SSC (rSSC), Spectrally Distributed RJ (sRJ)
- Lock system clock to an external reference clock with a multiplying PLL
- De-emphasis for pre- and post-cursor to emulate transmitter de-emphasis and compensate for loss in the test setup
- Inject Random Interference (RI) and Sinusoidal Interference (SI) via couplers. The M8000 software controls M8054A, AWG M8195A and M8196A as RI/SI source or as aggressor lanes
- Automated jitter tolerance testing

	NRZ 	PAM4 
Effective data rate	**Bit rate**	**Symbol rate**
32 Gbit/s	32 Gbit/s	16 Gbaud
64 Gbit/s	64 Gbit/s	32 Gbaud
128 Gbit/s	128 Gbit/s	64 Gbaud

Covered by M8040A

Related IEEE802.3cd 50/100/200GBASE/GAUI proposed symbol rate * # of lanes	**Related IEEE802.3bs 200GBASE/200GAUI symbol rate # of lanes**	**Related IEEE802.3bs 400GBASE/400GAUI symbol rate # of lanes**	**Related OIF CEI-56G symbol rates**	
25.78125 Gb/s NRZ * 1 lane	26.5625 Gbit/s NRZ * 8 lanes	26.5625 Gbit/s NRZ * 16 lanes		
26.5625 Gbaud PAM4 *1/2/4 lanes 53.125 Gbaud PAM4 *1/2 lanes	26.5625 Gbaud PAM4 * 4 lanes	26.5625 Gbaud PAM4 * 8 lanes 53.125 Gbit/s NRZ * 8 lanes	LR-PAM4: MR-PAM4: MR-NRZ: VSR-PAM4: VSR-NRZ:	19.6 to 30 Gbaud 18 to 29 Gbaud 39 to 56.2 Gbit/s 18 to 29 Gbaud

			XSR-PAM4: XSR-NRZ: USR-NRZ:	39 to 56.2 Gbit/s 18 to 29 Gbaud 39.8 to 58 Gbit/s 19.6 to 58.0 Gbit/s

Master PAM4 Receiver Test Challenges with M8040A BERT Platform

Design and test engineers who need to characterize devices that support PAM4 data formats are facing new test challenges in addition to the signal integrity issues known from 25 Gb/s NRZ device testing.

For PAM4 input receiver tolerance test, this means impairments that may occur in the real world should be tolerated by the receiver under test without exceeding the desired BER level. Typical receiver tests include jitter tolerance, interference tolerance test and level sensitivity margins that are applicable for NRZ and PAM4 devices. In addition, PAM4 receivers require additional margin testing for level non-linearity, crosstalk effects from adjacent lanes and vertical eye closure.

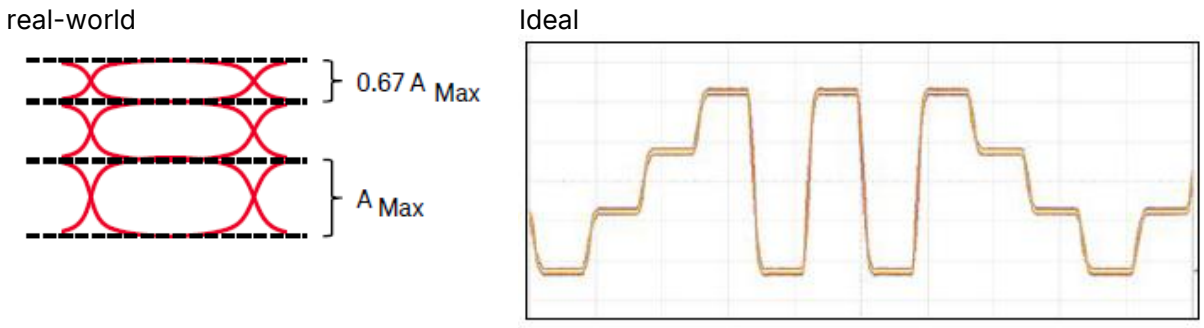


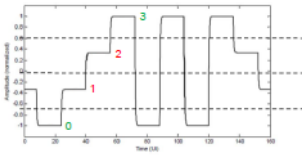
Figure 8. PAM4 eyes can show a level separation mismatch. Receivers must be able to detect the digital signal content properly within the given mismatch ratio.

Real-time Error Analysis for PAM4, PAM3 and NRZ Signals

Receiver verification checks if the receiver under test operates below the specified BER while emulating the worst-case transmitter and channel conditions. BER measurements are well established for NRZ signals by using a traditional BERT, but what does this mean for PAM4 signals?

For proper error detection of PAM4 signals, all thresholds (V_{low}, V_{mid}, and V_{upper}) must be analyzed simultaneously to ensure a correct symbol error measurement (see Figure 9). If a “1” is detected at the V_{mid} threshold, the received pattern can have level 2 or 3. Only if the level detected at Vupp is checked simultaneously with Vmid can it be determined whether the received inputs have the

correct level for a 2 or a 3. If two thresholds are errored within one UI, this case translates just into one symbol error.



Detecting	1	0
Threshold Vupp	= 3	= 0 or 1 or 2??
Threshold V mid	= 2 or 3?	= 0 or 1?
Threshold V low	= 1 or 2 or 3?	= 0

PAM-4	Vupp	Vmid	Vlow	Gray	
3	1	1	1	1	0
2	0	1	1	1	1
1	0	0	1	0	1
0	0	0	0	0	0

Figure 9. Only a true PAM4 error analyzer like M8040A can provide a PAM4 symbol error ratio in real time without post-processing. Error ratios down to 10^{-15} or error-free can be measured even for long PRBS 2^{31}–1, SSPRQ, QPRBS13-CEI or QPRBS31-CEI patterns. Errored 0,1,2,3 and symbol errors can be counted separately for further debugging.

The M8040A provides real-time error analysis of PAM4, PAM3 and NRZ signals.

Key capabilities of the error analyzer module M8046A include:

- One differential channel per analyzer module
- Symbol rates from 5 to 58 Gbaud for PAM4 and PAM3 and from 5 to 64 Gb/s for NRZ
- Native PAM4 decoding
- Built-in equalization to re-open closed eyes at the analyzer input
- Selectable expected patterns like QPRBS31, SSPRQ, pattern memory, pattern sequencing, masking, gray coding and custom PAM4 symbol mapping
- Integrated clock recovery option and control via M8070ADVB of external clock recovery units N1076A/B, N1077A, N1078A
- DUT control interface allows access to built-in error counters from the M8070ADVB advanced measurement software package
- Can be used in combination with M8045A pattern generator or M8194A/95A/96A AWGs

Automated Receiver Calibration and Characterization for IEEE 802.3bs/cd, IEEE 802.3ck, OIF-CEI-56G-VSR/-MR/-LR-PAM4, PCI Express 4.0, 5.0 and 6.0, USB 3.2, USB4 Version 2.0, TBT3 and TBT4 Interfaces

To simplify compliance testing and characterization of receivers, Keysight provides receiver test automation software for various electrical and optical interface standards. The following table gives an overview of the test automation software solutions available for the M8040A high-performance BERT.

Standard	Interface	Variants	BERT	Test automation software
IEEE 802.3bs/ cd	Electrical, Chip-to-module, Chip-to-chip, Backplane	400GAUI-8 200GAUI-4	M8040A	M8091BSCA Electrical Receiver Conformance Test Application for IEEE 802.3bs/ cd
IEEE 802.3bs/cd/db	Optical	400GBASE-LR8/-FR8 and 200GBASE-LR4/-FR4/-DR4 400G-DR4/-FR4/-SR4 and MSAs	M8040A	N4917BSCB Optical Receiver Stress Test Solution
IEEE 802.3ba	Optical	100GBASE-SR4/LR4/ER4 and MSAs	M8040A	N4917BACA Optical Receiver Stress Test Solution
IEEE 802.3ck	Electrical, Chip-to-module, Chip-to-chip,	100GAUI-1 400GAUI-4	M8040A	M8091CKCA Pre-compliance Receiver Test Automation for IEEE 802.3ck, draft 3.3
OIF CEI 4.0	Electrical, host and module	56G-VSR, -MR, -LR PAM4	M8040A	M809256CA Electrical Receiver Conformance Test Application for OIF-CEI-56G
PCI Express 5.0	Electrical	PCIe 2.5/58/16/32 GT/s	M8040A	N5991PB5A Receiver Test Automation for PCIe 5.0 base specification N5991PC5A Receiver Test Automation for PCIe 5.0 PHY Test Specification for CEM N5991PA3A-ADD Automated LinkEQ RX and TX testing
PCI Express 6.0	Electrical	PCIe 64 GT/s	M8040A	N5991PB6A Receiver Test Automation for PCIe 6.0 base specification – 64 GT/s only
SAS	Electrical	SAS 12 and 24 Gb/s	M8040A	N5991SA4A Receiver Test Automation for SAS
SATA	Electrical	SATA 3	M8040A	N5991ST3A Receiver Test Automation for SATA
DDR5	Electrical	DDR5	M8040A	M80885RCA Receiver Test Automation for DDR5
USB 3.2	Electrical	USB 3.2	M8040A	N5991U32A Receiver Test Automation for USB 3.2
USB4 Version 2.0	Electrical	USB4 Gen2 (10G NRZ) USB4 Gen3 (20G NRZ) USB4 Gen4 (25.6G PAM3)	M8040A	N5991U42A Receiver Test Automation for USB4 Version 2.0

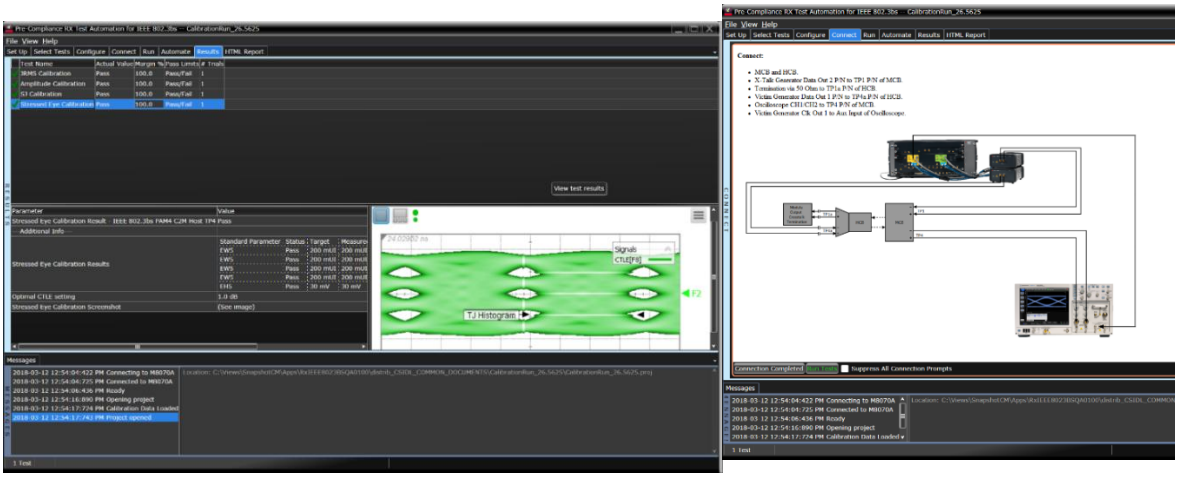


Figure 10. Automate the complicated stress signal calibration procedure with guided steps on how to connect the test setup and pre-compliance measurements by using the M8091CKCA receiver test automation software for IEEE 802.3bs for chip-to-module interfaces 400GAUI-8 and 200GAUI-4. The figure shows screenshots of the automation software with the results of a successful stress calibration (left side) and guided test setup (right side).

Specifications for M8045A and M8046A Modules and M8057A/B Remote Head

M8045A pattern generator module for two data channels, 3-slot AXIe



M8045A pattern generator module for one data channel, 3-slot AXIe



M8057A/B remote head with cable connections (0.85 m) front and rear view



M8046A analyzer module, 1-slot AXIe



Figure 11. Front panel views of pattern generator module M8045A (top) as 2 and 1 channel (center) versions, remote head M8057A/B, and error analyzer module M8046A (bottom). To allow a very short connection to the device under test, the remote head is used. One remote head is needed for each of the pattern generator data outputs of M8045A.

Specifications for Pattern Generator Module M8045A and Remote Head M8057A/B

The pattern generator supports symbol rates up to 32 Gbaud or 64 Gbaud, default is one channel and NRZ format. The remote head M8057A/B is needed once per channel. Using the P and N outputs of the M8045A without a remote head is prohibited.

For the following generator functions a separate module option is required:

- PAM4 coding up to 32 Gbaud (M8045A Option 0P3)
- PAM4 extension to 64 Gbaud (M8045A Option 0P6)
- Second data channel (M8045A Option 0G2)
- Advanced jitter sources (M8045A Option 0G3)
- De-emphasis (M8045A Option 0G4)
- Reference clock multiplier with bandwidth 2/5 MHz (M8045A Option 0G6)
- Extended calibration for 50G PON (M8045A Option 0G8)
- Forward Error Correction (FEC) encoding (M8045A Option 0G9)

Data Output (DATA OUT 1, DATA OUT 2)

All timing parameters are measured @ 0.5 V into ground at data outputs of remote head M8057A/B.

Table 1. Data output characteristics for M8045A with remote head M8057A/B.

Parameter	Value
Symbol rate	2.025 to 32.4 Gbaud for M8045A Option -G32 2.025 to 58.0 Gbaud (all specifications are valid up to 58 Gbaud with over-programming up to 64.8 Gbaud) for M8045A Option -G64
Data format	NRZ (default) PAM4 (requires M8045A Option -0P3 and for symbol rates above 32 Gbaud -0P6 in addition) PAM3 (requires M8045A Option -0P3)
Channels per module	1 or 2 (requires M8045A Option -0G2 and second remote head)
Amplitude with M8057B for symbol rates < 58 Gbaud	80 mV to 0.9 Vpp single ended 160 mV to 1.8 Vpp differential
Amplitude with M8057A For symbol rates < 32.4 Gbaud For symbol rates < 58 Gbaud	50 mV to 0.9 Vpp single ended 100 mV to 1.8 Vpp differential 50 mV to 0.6 Vpp single ended 100 mV to 1.2 Vpp differential
Amplitude accuracy	±10% ±10 mV typical (AC)[1]
Output voltage window	–1 to +3.0 V depends on external termination voltage[5]
External termination voltage	–1 to +3.0 V
Offset accuracy	25 mV +10% of offset +1% of amplitude. The offset is defined as 0.5 * (HIL+LOL). See [5]

Transition time [2]	9 ps typical (20 to 80%) for symbol rates > 32.4 Gbaud 11 ps typical (20% to 80%) for symbol rates ≤ 32.4 Gbaud
Intrinsic total jitter	8 ps typical @ 32.0 Gb/s NRZ, PRBS 15, BER 10^{-12}
Intrinsic random jitter (NRZ)	5 mUI rms typical @ symbol rates between 2.025 Gbaud and < 22 Gbaud 7 mUI rms typical @ symbol rates between 22 Gbaud and < 32.4 Gbaud 10 mUI rms typical @ symbol rates between 32.4 Gbaud and < 40 Gbaud 13 mUI [8] rms typical @ symbol rates between 40 Gbaud and < 52 Gbaud 10 mUI rms typical @ symbol rates between 52 Gbaud and < 58 Gbaud For M8045A with option -0G8 only: 10 mUI rms typical @ symbol rates between 49.5 Gbaud and < 58 Gbaud
Data delay range	0 to 10 ns, resolution 100 fs
Data delay accuracy	± (max. (1.5 ps or 10 mUI whichever is higher) + 1% of entered value) typical[3]
Electrical idle	The output transitions from full swing to 0 V amplitude and vice versa at constant offset within 1 UI.
Skew between normal and complement output	3 ps maximum at the end of the recommended cable pair. Fixed.
Skew between data output ch 1 and data output ch 2	370 ps maximum[4] Repeatability after manual de-skew ± 300 ps typical
Termination impedance range	To protect the output stage, the output is disabled when an unexpected voltage or termination impedance is detected. DC output coupling mode: Termination range for devices connected to data out: • Unbalanced 50 Ω +15 Ω / –10 Ω • Balanced 100 Ω ±30 Ω typical Operation into open[7] is possible for the following ranges when DC coupled and balanced termination modes are selected: • Output amplitude max. 450 mV • Offset 0 to 370 mV
Termination modes	Balanced/ unbalanced
Coupling	DC/ AC selectable coupling of device under test
Connectors	1.85 mm, female

1. At 5 Gbaud measured with DCA-X N1045A and clock pattern and in the middle of the eye
2. Measured with DCA-X N1045A
3. At constant temperature
4. Requires M8070A software revision 4.5 or M8070B SW 6.0 or later and a module serial number above DE56C00400
5. High level voltage range = 2/3 * Vterm - 0.95 V < HIL < V_{term} + 2 V
6. Low level voltage range = 2/3 * V_{term} - 1 V < LOL < V_{term} + 1.95 V
7. Available with M8070B SW 7.5 and higher
8. For M8045A with a module serial number below MYxxx02000 the intrinsic random jitter between 40 and <52 Gbaud is 12 mUI rms typical

De-emphasis (DATA OUT)

The M8045A provides built-in de-emphasis with positive and negative cursors based on a Finite Impulse Response (FIR) filter; see Figure 12. Users can enter the de-emphasis in coefficient

values. The M8045A supports five de-emphasis cursors with an adjustable main-cursor position between cursor 1 and cursor 3. A prerequisite for using the adjustable main cursor is M8070B software revision 7.1 or later.

This allows selecting the following configurations:

Main cursor position	Number of pre-cursors	Number of post-cursors
1	1	3
2	2	2
3	3	1

Table 2. Specifications for multi-tap de-emphasis (requires Option 0G4).

Parameter	Value NRZ	Value PAM4
De-emphasis taps	5, can be adjusted for each channel independently	
Coefficient c0	0.0 to ± 0.45 [1]	0.0 to ± 0.45 [1]
Coefficient c1	0.0 to ± 0.45 [1]	0.0 to ± 0.45 [1]
Coefficient c2	0.0 to ± 1.0 [1]	0.0 to ± 1.0 [1]
Coefficient c3	0.0 to ± 0.45 [1]	0.0 to ± 0.45 [1]
Coefficient c4 [2]	0.0 to ± 0.45 [1]	0.0 to ± 0.45 [1]
Cursor coefficient resolution	0.001 is supported in user interface with SW 9.0 or later, hardware resolution is coarser.	0.001 is supported in user interface with SW 9.0 or later, hardware resolution is coarser.
Tap optimization	Auto-optimization of DE taps is possible when using DCA and M8070ADVB	

1. The sum of the absolute values of all cursors may not exceed 1.0: $|c0|+|c1|+|c2|+|c3|+|c4| \leq 1$. Also, $|c0|$, $|c1|$, $|c3|$, $|c4| < |c2|$.
2. Requires M8070A software 5.0 or M8070B SW 6.0 or later.

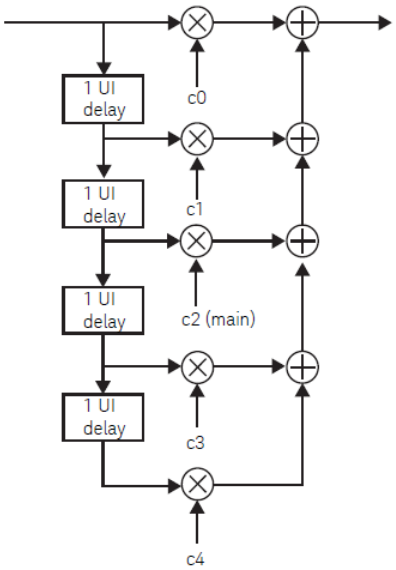


Figure 12. The pattern generator of M8045A provides integrated de-emphasis to emulate TX equalization. The example shows a configuration with two post-cursors c3 and c4, the main cursor c2 and two pre-cursors c0 and c1.

De-emphasis Presets for PCIe Testing

If PHY protocol mode PCIe3, PCIe4, PCIe5 or PCIe6 is selected for the pattern generator sequence, the multi-tap FIR is replaced by a PCI Express type of FIR editor. Coefficients are then entered as integers dependent on the selected full swing. A full swing from 24 to 63 coefficient resolution steps can be selected.

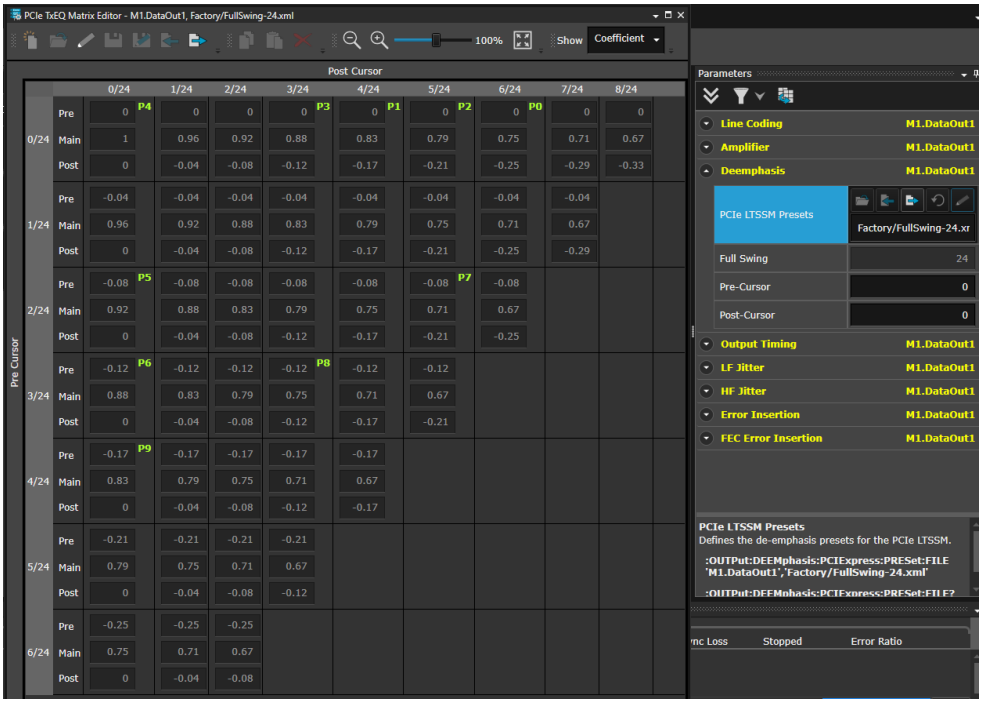


Figure 13. The TxEQ matrix editor can be accessed if the PHY protocol mode PCIe 3, PCIe 4 or PCIe 5 is selected for the pattern generator sequence.

Forward Error Correction (FEC) Encoding (DATA OUT)

The M8045A pattern generator module supports Forward Error Correction (FEC) and precoding according to IEEE 802.3cd.

Users can inject pre- and post-FEC errors to test the DUT's FEC decoder function.

Table 3. Specifications for FEC (Forward Error Correction) encoding (requires Option 0G9).

Parameter	Value
FEC encoding	50GBASE-R, 100GBASE-R, 200GBASE-R, 400GBASE-R
Reed-Solomon Code	RS (544,514)
Scrambler	PRBS 2^{58}-1
Pattern sequence	These patterns from the pattern library can be FEC encoded: Remote faults, Scrambled idle
Line coding	PAM4

Symbol rate	26.5625 Gbaud PAM4: 50GBASE (all PCS lanes), 100GBASE (PCS 0-9 on Channel 1 and 10-19 on Channel 2), 200GBASE (PCS 0,1) 400GBASE (PCS 0,1) 53.125 Gbaud PAM4: 100GBASE (all PCS lanes), 400GBASE (PCS 0,1, 2,3 on Channel 1 and PCS 4,5,6,7 on Channel 2)
FEC symbol error injection	For 50GBASE-R: Pre-FEC: insertion of a single BIP Post-FEC: FEC symbol errors, randomly distributed, selectable amount of symbol errors per FEC frame
Pre-coder	PAM4: 1/ (1+D) mod4, can be switched on/off. Follows IEEE802.3 Clause 135.5.7.2. for PAM4 encoded lanes.
Synchronization to A400GE-DD and G800GE	Yes, requires trigger and reference clock connection. Requires M8045A-0G9 and M8070B 7.0 or later.
Prerequisites	M8045A with option 0P3 and 0G9, M8070A SW 5.1/ M8070B 6.7 or later.

USB4 LFPS Generator (DATA OUT)

The USB4 LFPS Generator utility generates LFPS patterns with the M8070B software, allowing configuration of cycles, period, duty cycle, pre-data, and idle duration. Supported by M8042A and M8045A modules, it handles USB4 Gen 2 (10 Gbps), Gen 3 (20 Gbps), and Gen 4 (25.6 Gbaud) data rates. The LFPS Generator offers Calibration and Rx testing modes, controllable with Start and Stop buttons.

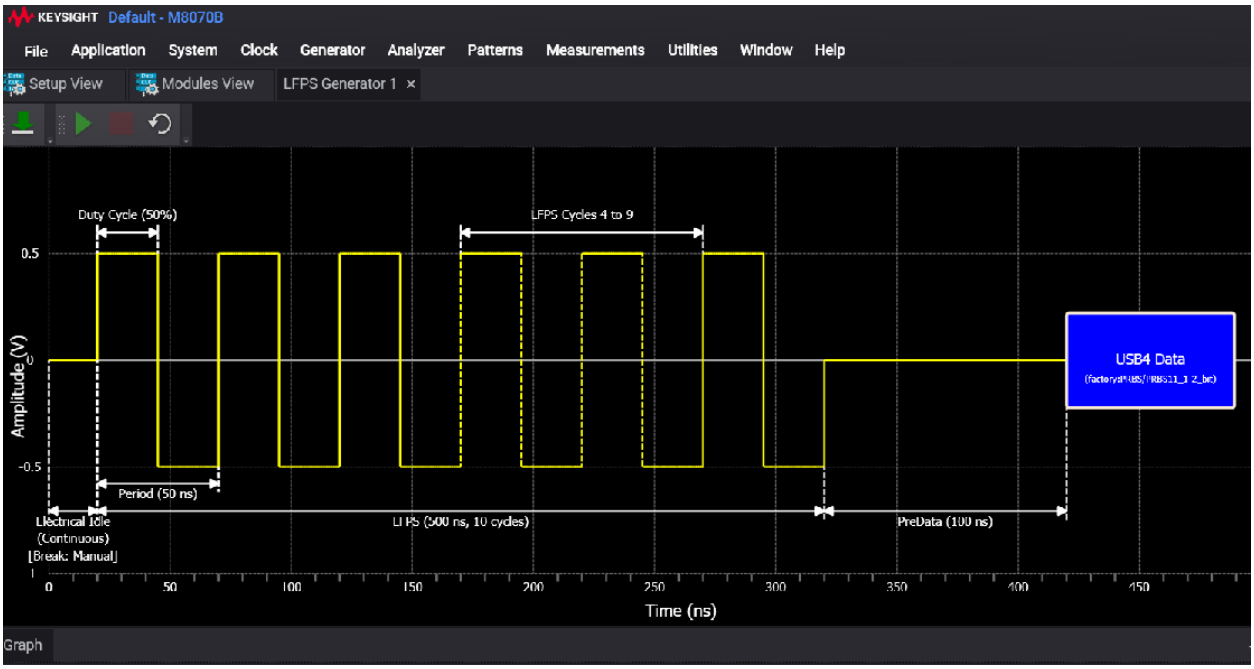


Figure 14. The USB4 LFPS generator utility.

Clock Output 1 and 2 (Channel 1 CLK OUT, Channel 2 CLK OUT)

These clock outputs provide two modes. They can operate with the same jitter as the corresponding data output or operate in a clean mode.

Table 4. Specifications for channel 1 clock output and channel 2 clock output.

Parameter		Value
Frequency range		1.0125 to 16.2 GHz with M8045A-G32 1.0125 to 32.4 GHz with M8045A-G64
Frequency divider factors		Symbol rate / clock divider: 2, 4, 8, 16. Divided output frequency must fit into frequency range
Clean clock mode	On Off	No jitter injection, no SSC Same jitter and SSC as data output of same channel
Amplitude		1 V typical nominal single ended
Duty cycle		50%, accuracy ± 15% typical
Intrinsic random jitter		6 mUI rms typical for symbol rates between 2.025 Gbaud and ≤ 27 Gbaud 10 mUI rms typical for symbol rates > 27 Gbaud. Refers to mUI of symbol rate.
Termination		50 Ω into GND or external termination voltage. Do not operate into open.
Coupling		AC coupled. Single ended.
Connectors		3.5 mm, female

Clock Output (CLK OUT)

This is a differential clock output with many sub-rate clock dividers. LF SJ and HF jitter can be turned off and on individually. HF jitter has the same setting as HF jitter of data output of channel 1. Delay on the trigger output also impacts clock output.

Table 5. Clock output specifications.

Parameter		Value
CLK frequency range		2.025 to 16.20 GHz
Clock divider in relation to clock frequency range		n * (1, 2, 4, 8, 10, 16, 20, 24, 30, 32, 40, 50, 64, 66, 80) with n= 1 < 16.2 GHz n= 2 for 16.2 GHz to 32.4 GHz n= 4 > 32.4 GHz For other dividers use TRIG OUT
Frequency resolution		1 Hz
Frequency accuracy		± 15 ppm
Amplitude	Differential Single ended	0.2 to 2.0 V, 10 mV steps 0.1 to 1 V, 5 mV steps
Output voltage window		–1 to +3 V [1]
External termination voltage		–1 to +3 V
Transition times		20 ps typical (20 to 80%)

Duty cycle	50%, accuracy ± 15%
Clock modes	See Table 6
Intrinsic random jitter	300 fs rms typical at 16.2 GHz and clock divider = 1
Jitter injection	LF Jitter: • Can be set independently from Data Out • Has the same LF jitter parameters and ranges as Data Out HF Jitter: • On -> the jitter values from Data Out1 HF Jitter are applied to Clock Out • Off -> no HF Jitter SSC: • SSC is a system-wide parameter and therefore applies to CLK OUT too Jitter delay: from + 40 ns to -40 ns
SSB phase noise[2]	–85 dBc/Hz typical at 10 kHz offset and internal clock and 10/100 MHz as external reference clock –80 dBc/Hz typical with 10 kHz offset for reference clock multiplier bandwidth 0.1 MHz
Termination	50 Ω into GND or external termination voltage. Do not operate into open. Unused outputs must be terminated into termination voltage
Coupling	DC coupled, differential
Connectors	3.5 mm, female

1. If Vterm is other than 0 V the following applies:
High level voltage range = 2/3 * Vterm – 0.95 V < HIL < Vterm + 2 V
Low level voltage range = 2/3 * Vterm – 1 V < LOL < Vterm + 1.95 V
2. For reference clock multipliers < 400.

Table 6. Clock modes.

Parameter	Value	
	Clock generation	**Input frequency range**
Internal	PLL with internal reference	N/A
Reference	PLL with bandwidth below 1 kHz	10/100 MHz
Direct	No PLL. Maximum symbol rate is 16.2 Gbaud	8.1 to 16.2 GHz
Reference clock multiplier bandwidth 100 kHz	m/n PLL with loop bandwidth 100 kHz m, n = 1 to 1620	10 MHz to 16.2 GHz

Reference Clock Input (REF CLK IN)

This input allows locking the system clock to an external reference clock of 10 or 100 MHz instead of the internal oscillator. It also allows the use of an external clock; see the clock modes in Table 6.

An SSC-tolerant PLL is used to multiply the external reference clock to the system clock.

Table 7. Reference clock input specifications (M8045A only).

Parameter	Value
Input amplitude	0.2 to 1.4 Vpp
Input frequency	10 MHz to 16.2 GHz, depends on clock mode and max. data rate option [1]
Interface	Single ended. 50 Ω nominal
Connector	SMA, female

1. A minimal slew rate of 0.3 V/ns at the REF CLK IN signal is required to ensure a proper frequency measurement. If this requirement cannot be met, the input frequency should be set manually.

Table 8. Predefined settings for reference clock multiplier (M8045A with Option 0G6 only).

Ref clock input	Standard	Target data rate	Multiplier	PLL loop BW
100 MHz	PCIe [1]	32 Gbaud (NRZ or PAM4)	320	2 MHz
100 MHz	PCIe	16 Gb/s	160	2 MHz
100 MHz	PCIe	8 Gb/s	80	5 MHz
100 MHz	PCIe	5 Gb/s	50	5 MHz
100 MHz	PCIe	2.5 Gb/s	25	5 MHz
100 MHz	USB4 Gen2	10 Gb/s	100	5 MHz
100 MHz	USB4 Gen3	20 Gb/s	200	5 MHz
103.125 MHz	TBT3 Gen2	10.3125 Gb/s	100	5 MHz
103.125 MHz	TBT3 Gen3	20.625 Gb/s	200	5 MHz
19.2 MHz	MIPI M-PHY	2.496/2.9184/4.992/5.8368/ 9.984/11.6736 / 19.968 / 23.3472 Gb/s / 23.3472 Gbaud PAM-4	130/152/260/304/520/608/1216	2 MHz
26 MHz	MIPI M-PHY	2.496/2.912/4.992/5.824/ 9.984/11.648 / 19.968 / 23.296 Gb/s / 23.296 Gbaud PAM-4	96/112/192/224/384/448/896	2 MHz
38.4 MHz	MIPI M-PHY	2.496/ 2.9184/ 4.992/ 5.8368/ 9.984/ 11.6736 / 19.968 / 23.3472 Gb/s / 23.3472 Gbaud PAM-4	65/76/130/152/260/304/608	2 MHz
52 MHz	MIPI M-PHY	2.496/2.912/4.992/5.824 9.984/11.648 / 19.968 / 23.296 Gb/s / 23.296 Gbaud PAM-4	48/56/96/112/192/224/448	2 MHz
Prerequisites	Requires M8045A with a serial number above MYxxx1000 and M8070B software revision 6.5 or later. Older serial numbers can be upgraded (M8045A-UR4, Return-to-Keysight).			

1. Requires M8070B SW 8.0 or later.

Trigger Output (TRG OUT)

This output is used to send a trigger signal to another connected device, such as an oscilloscope. Also, it can be used to generate a sub-rate clock. The trigger output can be used in different modes:

- Divided clock, dividers:
  - For <16.2 Gbaud trigger data rate range 2 to 65532
  - For 16.2 to 32.4 Gbaud trigger data rate range 4 to 65532 with step resolution of 2
  - For > 32.4 Gbaud trigger output data range 8 to 65532 with step resolution of 4
- Sequence block trigger with adjustable pulse width and offset
- PRBS sequence trigger with adjustable pulse width

Table 9. Trigger output specifications.

Parameter	Condition	Value
Amplitude	Single-ended Differential	0.1 to 1.0 Vpp 0.2 to 2.0 Vpp
Jitter injection		The injected jitter is identical to the jitter at the CLOCK OUT
Delay range		0 to 100 ns, resolution 100 fs
Delay accuracy		± (max. (1.5 ps or 10 mUI whichever is higher) + 1 % of entered value) typical [3]
Skew between trigger output and data output ch 1 or ch 2, [2 3 4]		370 ps maximum Repeatability after manual deskew ± 250 ps typical
Duty Cycle Distortion (DCD)		In divided clock mode: ± 20 ps
Output voltage window		-1 to 3 V [1]
External termination voltage		-1 to 3 V
Interface		Differential, 50 Ω
Connector		3.5 mm, female

1. If Vterm is other than 0 V the following applies:
   - High level voltage range = 2/3 * Vterm – 0.95 V < HIL < V_{term} + 2 V
   - Low level voltage range = 2/3 * Vterm – 1 V < LOL < V_{term} + 1.95 V
2. Requires M8070A software 4.5 or M8070B SW 6.0 or later and a module serial number above DE56C00400
3. At constant temperature
4. Sequencer controlled trigger (use a cable with 3.75 ns delay (~ 865 mm) connected to trigger output)

Reference Clock Output (REF CLK OUT)

Outputs a 10 and 100 MHz clock, 1 Vpp single ended into 50 Ω.

Connector: SMA, female.

Control Input A and B (CTRL IN A, CTRL IN B)

Functionality of each input can be configured as sequence trigger or error addition.

Table 10. Control input specifications.

Parameter	Value
Input voltage	-1 V to +3 V
Termination voltage	-1 V to +3 V
Termination voltage accuracy	± (25 mV+1%)
Threshold voltage	-1 V to +3 V
Delay to data output	< 1 ms, repeatability ±512 UI (requires M8070A software 4.5/ M8070B SW 6.0 or later and a module serial number above DE56C00400)
Connector	3.5 mm, female

Control Output A and B (CTRL OUT A, CTRL OUT B)

Generates a pulse or static high/low when controlled by the sequencer.

Table 11. Control output specifications.

Parameter	Value
Amplitude [1]	0.1 V to +2 V
Output voltage [1]	-0.5 to 1.75 V
Delay to data output	±512 UI ± jitter amplitude/2 (requires M8070A software 4.5/ M8070B SW 6.0 or later and a module serial number above DE56C00400)
Connector	3.5 mm, female

1. When terminated with 50 Ω into GND. Doubles into open.

Connection Link A and B (LINK 1234)

This communication link enables interactive link training with low latency between an M8045A pattern generator channel and an M8046A analyzer module. Performing the link training using the **M8046A error analyzer** requires a 4-wire mini coax cable **M8051A-801** (also orderable as M8041-61601) and M8045A with a serial number of MY/DExxx1000 or higher. Older serial numbers can be upgraded (M8045A-UR4, Return-to-Keysight).

The link interface enables interactive, low-latency link training (as required by PCIe or USB) between a pattern generator channel and one of the error analyzer modules.

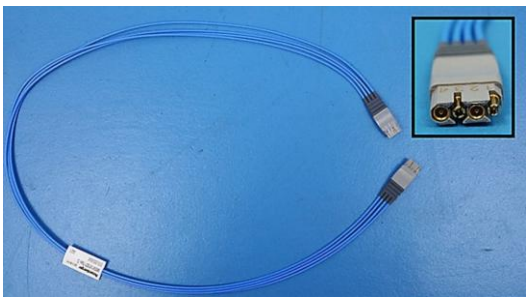


Figure 15. Link interface 4-wire mini coax M8051A-801.

IMPORTANT Ensure that you use the correct cable to perform link training. Using an incorrect cable will cause the link training to fail or damage the hardware.

Synchronization Out (SYNC OUT)

The sync output is a clock output to synchronize additional modules to a common clock. It can be used to synchronize the M8046A with the system internal clock.

System Input A/B (SYS IN A/B)

These are control inputs to synchronize events for the pattern sequencer.

Table 12. System input specifications.

Parameter	Value
Input voltage	-1 V to +3 V
Termination voltage	-1 V to +3 V
Threshold voltage	-1 V to +3 V
Delay to data output	< 1 ms, Repeatability ±512 UI. (requires M8070A software 4.5 or M8070B SW 6.0 or later and a module serial number above MY/ DE56C00400)
Connector	SMA, female

System Output A/B (SYS OUT A/B)

Generates a pulse or static high/low controlled by the pattern sequencer. A and B outputs are independently controllable.

Table 13. System output specifications.

Parameter	Value
Amplitude [1]	0.1 V to 2 V
Output voltage [1]	-0.5 to 1.75 V
Delay to data output	±512 UI ± jitter amplitude/2 (requires M8070A software 4.5/M8070B SW 6.0 or later and a module serial number above DE56C00400)
Connector	SMA, female

1. When terminated with 50 Ω into GND. Doubles into open.

Auxiliary Input (AUX IN)

Not used.

Clock Input (CLK IN)

For future use. See reference clock input for direct clock mode.

Jitter Specifications

The M8045A has integrated and calibrated jitter sources. To use jitter injection, M8045A Option -0G3 is required.

Table 14. Specifications for low frequency periodic jitter (requires Option -0G3 advanced jitter sources).

Parameter		Value
Low frequency periodic Jitter (LF PJ) (generated by IQ modulator)	Amplitude range	0 to 123.5 UI * symbol rate (in Gbaud) for modulation frequencies of 100 Hz to 10 kHz, see table below. For modulation frequencies between 10 kHz and 40 MHz the maximum LF PJ = $\frac{7.792\ \text{UI} * 10^{-3} * \text{symbol rate (baud)}}{\text{modulation frequency (Hz)}^{1.2}}$
	Frequency	100 Hz to 40 MHz, sinusoidal modulation
	Jitter amplitude accuracy	± 2% ± 1 ps typical
	Two-tone	yes
	Adjustable	For each data channel independently, same LFPJ for clock and trigger

Low frequency periodic jitter

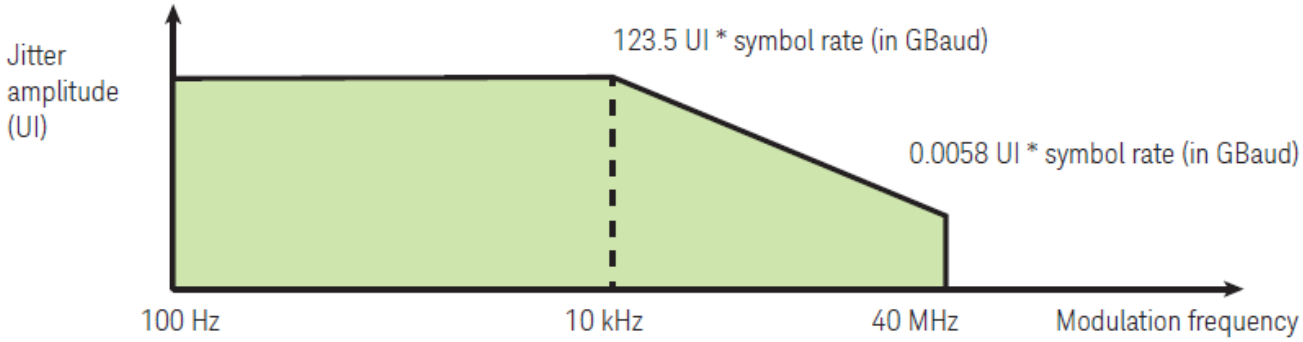


Figure 16. Low frequency periodic jitter maximum depends on data rate and modulation frequency.

Table 15. Low frequency periodic jitter ranges.

Symbol rate	Max UI at modulation frequency 100 Hz to 10 kHz	Max UI at modulation frequency 10 MHz	Max UI at modulation frequency 40 MHz
2.025 to 4.05 Gbaud	250 to 500 UI	0.0625 to 0.125 UI	0.012 to 0.025 UI
4.05 to 8.1 Gbaud	500 to 1000 UI	0.125 to 0.25 UI	0.024 to 0.048 UI
8.1 to 16.2 Gbaud	1000 to 2000 UI	0.25 to 0.5 UI	0.048 to 0.095 UI
16.2 to 32.4 Gbaud	2000 to 4000 UI	0.5 to 1 UI	0.095 to 0.19 UI
32.4 to 64.8 Gbaud	4000 to 8000 UI	1 to 2 UI	0.19 to 0.38 UI

Table 16. Specifications for high frequency periodic jitter, random jitter, bounded uncorrelated jitter, clock / 2 jitter (all require M8045A Option -0G3 advanced jitter sources).

Parameter	Value	
High frequency jitter (generated by delay line)	Range	1 UI for > 32.4 Gbaud, for ≤ 32.4 Gbaud minimum of: - 1 UI - 1 UI - (PJ frequency - 250 MHz) / 100 MHz * 0.2 UI - 0.5 UI if RJ low pass filter is 1000 MHz - 0.5 UI if external delay modulation is on Note: This is max sum of RJ, HF-PJ1 and HF-PJ2, external delay modulation and BUJ.
High frequency periodic jitter (HF PJ1 and HF PJ2)	Range	See HF jitter above [1]
	Frequency	1 kHz to 500 MHz. For symbol rates < 4 Gbaud the max modulation frequency is symbol rate / 8. Two tone possible. Sweep. Sinusoidal
	Jitter amplitude accuracy	±3 ps ± 10% typical [2]
	Adjustable	For each channel independently
Random jitter (RJ)	Range	0 to 72 mUI rms (1 UI p-p max.) [1]
	Jitter amplitude accuracy	±300 fs ± 10% typical
	Filters	High pass: 10 MHz and "off", Low pass: 100 MHz, Low pass: 500 MHz, Low pass: 1 GHz (for symbol rates ≥ 7.5 Gbaud)
	Adjustable	For each channel independently
	Crest factor	14 (peak-peak to rms ratio)
Spectrally distributed RJ	Range	0 to 72 mUI (1 UI p-p) [1]
According to PCIe 2 (sRJ) [3]	Frequency	LF: 0.01 to 1.5 MHz, HF: 1.5 to 100 MHz
	Jitter amplitude accuracy	± 300 fs ± 10% typical
	Adjustable	For each channel independently
Bounded uncorrelated jitter (BUJ)	Range	See HF jitter above [1]
	PRBS polynomials	2^n–1, n = 7, 8, 9, 10, 11, 15, 23, 31
	Filters	50/100/200 MHz low pass 3rd order
	Jitter amplitude accuracy	± 5 ps ± 10% typical for settings shown in table below
	Adjustable	For each channel independently
	Rate for PRBS generator	625 Mb/s, 1.25 Gb/s, and 2.5 Gb/s
Clock/2 jitter	Range	± 50 mUI or ±5 ps typical (whichever is less). Note: this means that first eye can be up to 50 mUI or 5 ps longer or shorter than subsequent eye
	Adjustable	For each channel independently

1. Range of HF jitter applies to sum of RJ, HF-PJ1 and HF-PJ2, external delay modulation and BUJ. See further limitations under high frequency jitter specifications.
2. For symbol rates above 32.4 Gbaud at an ambient temperature of 25 ± 6 °C
3. Requires M8070B software rev 6.0 or later. sRJ is mutually exclusive with RJ and BUJ. Valid if sRJ low pass filter is "on".

Table 17. BUJ accuracy applies for these BUJ settings.

BUJ calibration settings[1]	Rate for PRBS generator	PRBS polynomial	Low pass filter
CEI 6G	1.25 Gb/s	PRBS 2^9-1	100 MHz
CEI 11G	2.5 Gb/s	PRBS 2^{11}-1	200 MHz
Gaussian	2.5 Gb/s	PRBS 2^{31}-1	100 MHz
CEI 25G	2.5 Gb/s	PRBS 2^{11}-1	200 MHz
CEI 56G	2.5 Gb/s	PRBS 2^{11}-1	200 MHz

1. Other settings are not calibrated and do not necessarily generate the desired jitter histograms for all data rates of the PRBS generator

Table 18. Specifications for Spread Spectrum Clocking (SSC). Requires M8045A Option -0G3 advanced jitter sources.

Parameter	Value	
SSC (Spread Spectrum Clock)	Symbol rate range for SSC	2.025 to 32.4 Gbaud
	Range	See HF jitter above [1]
	Asymmetric SSC [1]: Upper deviation range Lower deviation range	0 to 1% -1% to 0
	Frequency	100 Hz to 200 kHz
	SSC amplitude accuracy	± 0.025% typical
	Outputs	Can be turned on/ off together for CLK OUT, DATA OUT 1, DATA OUT 2, TRG OUT, Channel 1 and 2 CLK OUT
Residuals SSC [1]	Range	0 to 600 ps
	Frequency	10 to 100 kHz
	Outputs	Can be turned on/ off together for CLK OUT, DATA OUT 1, DATA OUT 2, TRG OUT, Channel 1 and 2 CLK OUT

1. Requires M8070B SW 6.0 or later.

External Jitter Modulation

An external modulation source can be used to modulate the delay of the M8045A data outputs, clock output and trigger output.

Data Modulation Inputs (DATA MOD IN 1, 2)

This input can be used for delay modulation by an external source for each data output channel individually.

Table 19. Specifications for external jitter modulation on data outputs.

Parameter	Value	
External jitter – data modulation input 1 and 2	Range	Up to 1 UI for symbol rates > 32.4 Gbaud
		Up to 0.5 UI for symbol rates ≤ 32.4 Gbaud [1]
	Maximum	0.8 Vpp max
	Frequency	Up to 500 MHz
Gain [2]		For symbol rates up to 16.2 Gbaud: 1 UI/ 0.725 V ± 5% typical For symbol rates > 16.2 Gbaud: 1 UI/ 0.725 V ± 12% typical
Linearity		50 mUI
Connectors		3.5 mm, female

1. See HF jitter specifications for the maximum sum of RJ, HF-PJ1 and HF-PJ2, external delay modulation and BUJ
2. For symbol rates above 32.4 Gbaud at an ambient temperature of 25 ± 6 °C

Clock Modulation Input (CLK MOD IN)

This input can be used for delay modulation of TRIG OUT and CLK OUT; the modulation affects both outputs simultaneously.

Table 20. Specifications for external jitter modulation for clock and trigger.

Parameter	Value	
External jitter – clock modulation input	Description	Input for the delay modulation for the TRG OUT and CLK OUT. Affects both data outputs
	Range	Up to 1 UI for symbol rates > 32.4 Gbaud Up to 0.5 UI for symbol rates ≤ 32.4 Gbaud [1] 0.8 Vpp max
	Frequency	Up to 500 MHz
Gain [2]		For symbol rates up to 16.2 Gbaud: 1 UI/ 0.725 V ± 5% typical For symbol rates > 16.2 Gbaud: 1 UI/ 0.725 V ± 12% typical
Linearity		50 mUI
Connectors		SMA, female

1. See HF jitter specifications for the maximum sum of RJ, HF-PJ1 and HF-PJ2, external delay modulation and BUJ
2. For symbol rates above 32.4 Gbaud at an ambient temperature of 25 ± 6 °C

External Interference (RI/SI) Sources

The Keysight M8054A interference source and M8194A, M8195A and M8196A AWGs can be used as level interference sources with sinusoidal and random modulation. The M8000 system software controls the interference parameters such as amplitude, bandwidth and crest factor. Keysight provides matched coupler pairs for injecting the RI or SI signal before or after the channel. See the table below.

Table 21. Specifications for external level interference sources RI/SI with M8194A, M8195A, M8196A and M8054A.

Parameter	M8070A/B	M8194A	M8195A	M8196A/ M8054A
Random Interference (RI)		Yes	Yes	Yes
	Amplitude range (single ended, at DAC output of AWG)	0 mV to 800 mV, 1 mV resolution	0 mV to 1 V, 1 mV resolution	0 mV to 1 V, 1 mV resolution
	Lowest frequency range	230 kHz to 45 GHz	320 kHz to 20 GHz (ch1 with deep memory: 100 Hz to 25 GHz)	160 kHz to 32 GHz
	Highest frequency range	230 kHz to 45 GHz	320 kHz to 25 GHz	160 kHz to 32 GHz
	Crest factor (peak ratio)	> 5 [2]	> 5 [,2]	> 5 [,2]
Sinusoidal Interference (SI)		Yes	Yes	Yes
	Amplitude range (single ended, at DAC output of AWG)	0 mV to 800 mV, 1 mV resolution	0 mV to 1 V, 1 mV resolution	0 mV to 1 V, 1 mV resolution
	Frequency range	230 kHz to 45 GHz	320 kHz to 25 GHz (channel 1 with deep memory: 100 Hz to 25 GHz)	160 kHz to 32 GHz
Common Mode Sinusoidal Interference (CMSI)		Yes	Yes	Yes
	Amplitude	0 mV to 800 mV, 1 mV resolution	0 to 995 mV, 1 mV resolution	0 to 995 mV, 1 mV resolution
	Modulation frequency range	1 MHz to 12 GHz, one and two tone [1]	1 MHz to 12 GHz, one and two tone [1]	1 MHz to 12 GHz, one and two tone [1]
	Phase range	-360 to 360 deg	-360 to 360 deg	-360 to 360 deg
Differential Mode Sinusoidal Interference (DMSI)		yes	Yes	Yes
	Amplitude	0 mV to 800 mV, 1 mV resolution	0 to 995 mV	0 to 995 mV

Parameter	M8070A/B	M8194A	M8195A	M8196A/ M8054A
	Modulation frequency range	1 MHz to 12 GHz, one- and two-tone [1]	1 MHz to 12 GHz, one- and two-tone [1]	1 MHz to 12 GHz, one- and two-tone [1]
	Channel coupling	Yes, for channel 1 & 2, channel 3 & 4		
	Amplitude correction factor [3]	0 to 8.	0 to 10.	
	Phase range	-360 to 360 deg	-360 to 360 deg	-360 to 360 deg
Simultaneous injection of CMSI and DMSI	Simultaneous injection of CMSI and DMSI [1]	0 mV to 800 mV, 1 mV resolution	0 to 995 mV	0 to 995 mV
Recommended accessories	M8045A-802 Matched directional coupler pair, 1 to 50 GHz, 13 dB, 2.4 mm (recommended for RI and highest BW), M8045A-803 Matched coupler pair, DC to 50 GHz, 12 dB, 2.4 mm (recommended for PCIe5, CMSI, DMSI)			
Software pre-requisites	M8070B SW 7.0 or higher	M8194A FW 2.0.31.0 or later and M8070B SW 7.0 or later	M8195A firmware V3.2.0 or higher	M8196A firmware V2.1.0.0 or higher. For M8054A: M8070B 6.5 or higher

1. Sum of amplitude in case of two-tone modulation must be within amplitude range
2. Requires M8070B software revision 7.2 or higher
3. Can be used to compensate for differences in channel losses in channel coupling mode

Adjustable Intersymbol Interference (ISI)

The M8070ISIB - Adjustable ISI Package simplifies receiver testing by offering flexible handling of test channels. A channel response can be emulated at the transmitter side by specifying its insertion loss at specific frequency points. Channel emulation can be combined with actual physical ISI trace boards to result in a new test channel.

- Cable embedding and de-embedding
- Adjustable insertion loss [-3,+2 dB] with 0.5 dB accuracy (typical) around the reference channel

The M8070ISIB is a licensed software package that requires M8070B version 9.5 or higher.

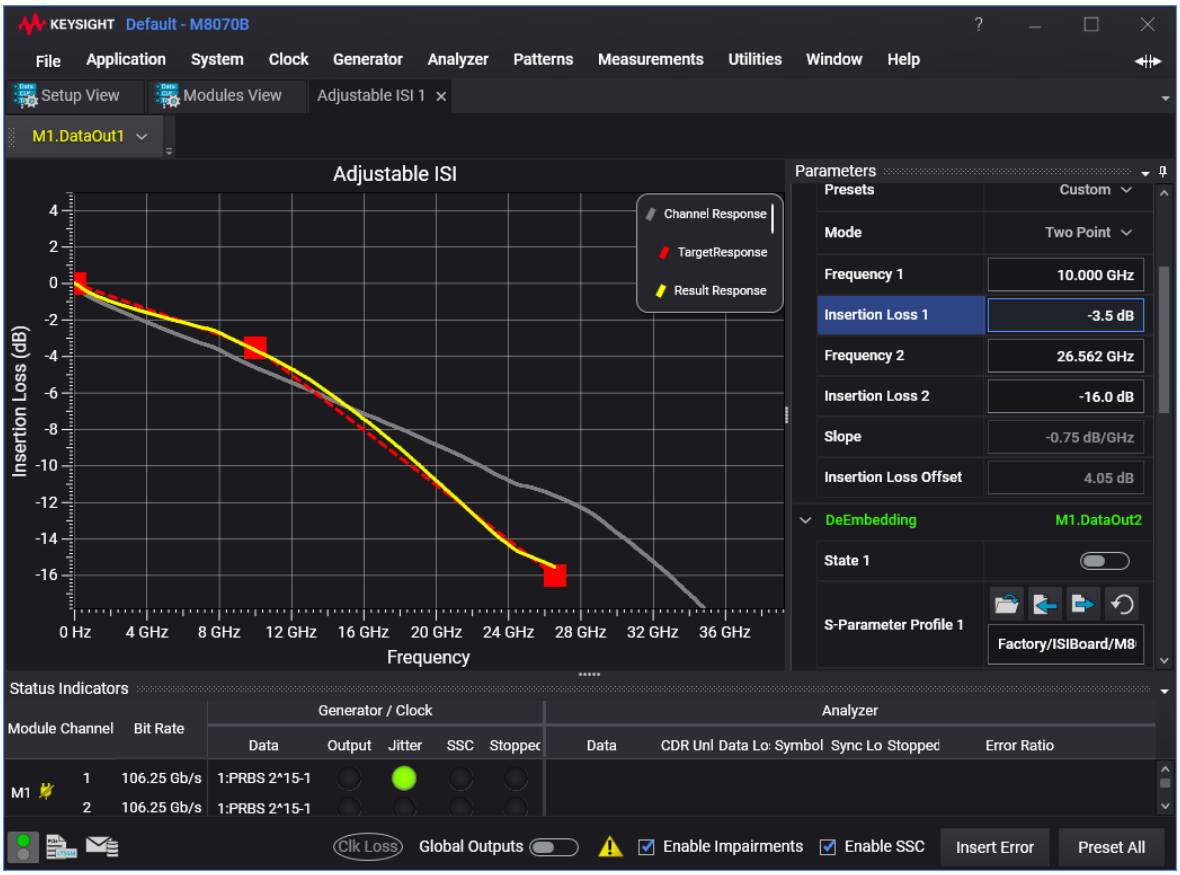


Figure 17. The Adjustable Intersymbol Interference M8070ISIB enables fast tuning of the insertion loss of an existing test channel to accelerate the testing of a digital receiver.

Table 22. Specifications for adjustable ISI with M8070ISIB Adjustable ISI software package when used with M8045A pattern generator module.

Parameter	Value
Cable de-embedding	• Choose from a list of M8000 standard accessories or use S-parameter files to combine up to two cables

Adjustable insertion loss	• Adjust the insertion loss of an external trace board at one or two frequencies up to the signal Nyquist frequency (baud rate / 2) • Can be used stand-alone (without trace board) • [-3 dB, +2 dB] adjustable loss range with 0.5 dB accuracy
Software pre-requisites	M8070B version 9.5 or later
Hardware pre-requisites	M8045A with de-emphasis option -0G4
License types	Choose between node-locked, transportable, network, USB-dongle license types either perpetual or with limited duration The network license is only recommended when using multiple M8040A setups within one company

External ISI Channel Boards

Keysight offers external ISI channel boards to emulate realistic channel loss conditions for high-speed receiver testing.

M8049A ISI Channel Boards

For symbol rates below 32 GBd, the M8049A ISI channel boards are recommended. For detailed specifications and available channel profiles (S-parameters) for the M8049A, refer to the M8049A ISI Channel Boards data sheet.



Figure 18. M8049A ISI channel boards.

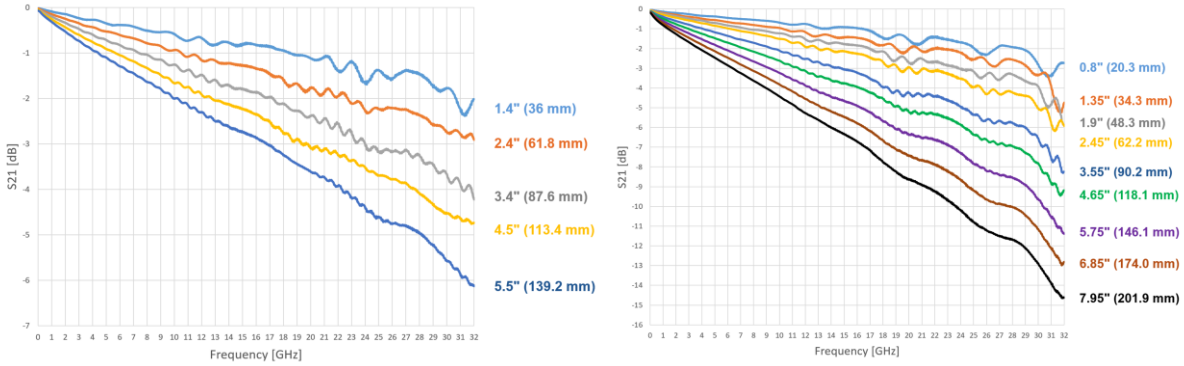


Figure 19. Typical insertion loss (S21) of the M8049A-001 and -002 ISI channel boards.

M8067A ISI Channel Boards

The M8067A ISI channel boards support a wide range of channel loss profiles for symbol rates above 32 GBd, enabling accurate emulation of high-frequency interconnect impairments. The M8067A ISI channel boards provide well-characterized physical channels for emulating realistic intersymbol interference and channel loss in high-speed receiver testing at symbol rates up to 64 GBd and 120 GBd.

They offer multiple trace lengths and connector variants, enabling controlled insertion loss of approximately 5 dB to 30 dB across the relevant frequency range, with individual S-parameter models for accurate embedding.

The compact boards can be placed close to the DUT and are designed for repeatable, standard-oriented receiver stress and tolerance testing. For detailed specifications and available channel profiles for the M8067A, refer to the M8067A ISI Channel Boards data sheet.



Figure 20. Keysight offers ISI channel boards M8067A-001, -002, -003, -004, and -005. The boards -001 and -002 offer 1.85 mm connectors and are suitable for emulating channel losses to characterize receivers that operate up to 64 GBd. For characterizing receivers that operate at symbol rates above 64 GBd and up to 120 GBd, we recommend using the ISI channel boards M8067A-003, -004, or -005 with 1.00 mm connectors.

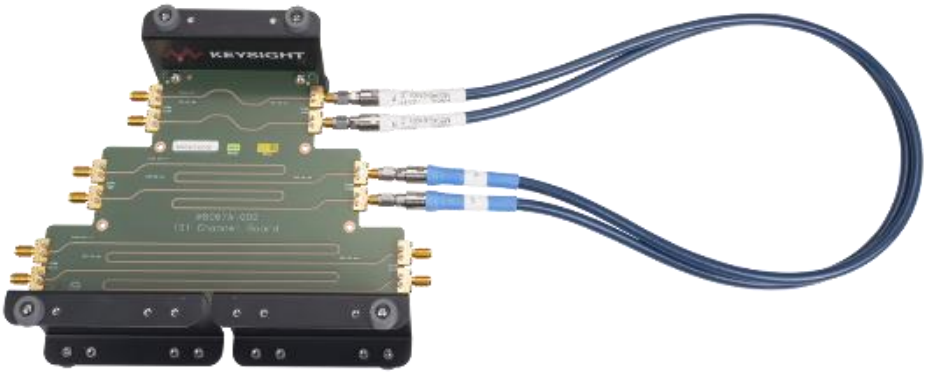


Figure 21. To achieve higher loss, you can cascade two ISI channels by connecting them with a cable.

Pattern Sequencer, Filler Symbol Filtering, and Interactive Link Training

Table 23. Specifications for pattern and sequencer.

Parameter	Value
Odd PRBS [1]	2^n–1, n= 7 [2], 9, 10, 11, 13, 15, 23, 23p, 31, 33, 35, 39, 45, 49, 51
Even PRBS	2^n, n = 7, 10, 11, 13, 15, 23
QPRBS	OIF-CEI: QPRBS13-CEI, QPRBS31-CEI IEEE 802.3: QPRBS13, PRBS13Q, PRBS31Q, SSPRQ MIPI M-PHY 6: PRBS9Q, PRBS13Q, PRBS15Q
PRTS [2]	3^n-1, n = 7, 17, 19, 23
New patterns in library	PAM4-linearity, JP03A, JP03B, PAM3-STAIRS64
PAM3 coding	requires M8045A-0P3 / M8046A-0P3. Custom symbol mapping
PAM4 coding	Gray coding, custom mapping of 00, 01,10,11 to symbols 0,1,2,3. Requires option -0P3 /-0P6.
Mark density	PRBS 1/8 to 7/8
Zero substitution	Yes
Export/Import	Patterns from M8000 and N4900 series can be imported
Pattern library	Yes
User definable memory	NRZ: 2 Gbit/channel, PAM4: 1 G Symbol / channel
Vector/sequence granularity	512 bit
Pattern capture	Yes, raw data for PAM4 • Capture data starts on event • User defined (minimum) amount of pre-event bits/ symbols and minimum capture bit/symbols • Events: single error, user-defined error bursts, CTRL In A/B, immediate • Max 2 Gbit/ch capture data for NRZ, 1 G Symbol / ch for PAM4 Save captured data: • With errors • As expected data (ignores error content) • As PG data (ignores error content) • Export via pattern editor windows • Convert bits into all other codings and vice versa • Ability to mask error bits automatically Display of captured data: • Display errors with color coding Navigate through error bits/symbols (find next/previous)
Pattern sequencer	3 counted loop levels, 1 infinite loop, # of blocks: 500
Masking	Expected bits can be masked (ignored) during error counting. Bitwise and block-wise masking is possible.

1. Polarity is inverted compared to ParBERT and J-BERT N4903A/B and N49xx series.
2. M8046A requires M8070B SW 10.5 or later.

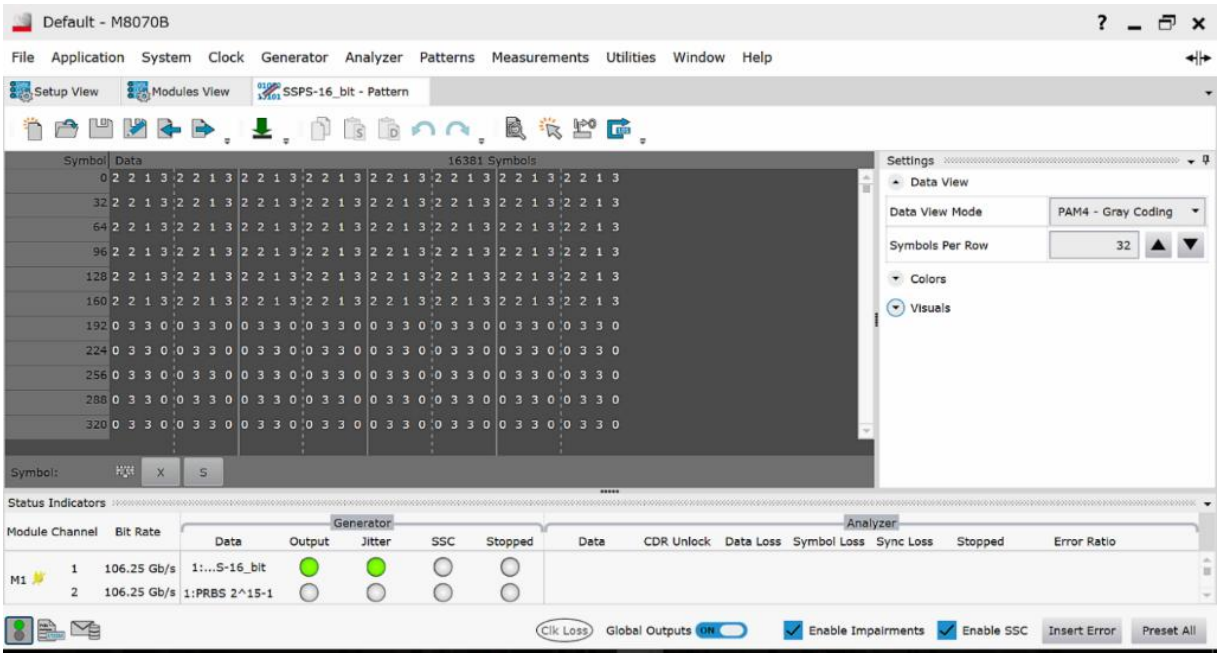


Figure 22. The pattern editor in the M8070B software allows editing NRZ bits and PAM4 symbols. The PAM4 symbol to bit mapping can be selected as Gray coded or custom with adjustable PAM4 levels. Quaternary PRBS, like QPRBS13-CEI or QPRBS31, according to CEI and IEEE standards can be selected as well as SSPRQ and PAM4 linearity test patterns.

Pattern and Sequence Editors

The M8070B system software provides a Sequence Editor and a Pattern Editor to create the stimulus for characterization and standards-based receiver tests of NRZ, PAM3, and PAM4 devices:

- Sequence Editor: sequences of up to 500 blocks with three counted loop levels and one infinite loop. Start and break conditions, block triggers on the trigger and system outputs, and an XML view for direct editing are available.
- Predefined sequences for PCI Express, USB, and SATA, as well as PHY protocol modes for link training and SKP OS/ALIGN filtering
- Pattern Editor: creation, import, and export of user patterns up to 2 Gbit per channel for NRZ and 1 Gsymbol per channel for PAM4, with binary, symbol, and coded views
- Factory pattern library with algorithmic and standard patterns such as PRBS, QPRBS13-CEI, PRBS13Q, PRBS31Q, SSPRQ, PRTS, PAM4 linearity, JP03A/B, and FEC-encoded patterns
- Separate sequences for pattern generator and analyzer channels, including bitwise and block-wise masking of expected bits

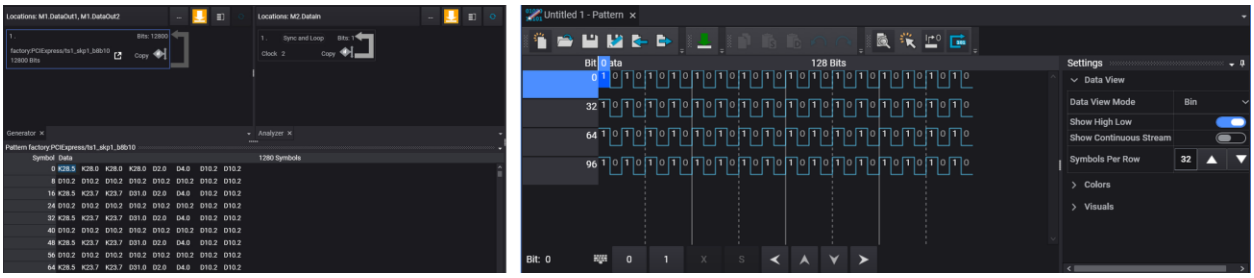


Figure 23. Sequence Editor with a PCI Express training pattern in 8B/10B symbol view (left) and Pattern Editor with bit-level waveform view (right).

Filtering of SKPs, SKP OS and ALIGNs (M8046A Option -0S2, Option -0S4, -0S6, -0N2)

SKPs, SKP OS and ALIGN are filler symbols used for clock compensation. Filtering of such symbols is required whenever a Device Under Test (DUT) modifies respective filler symbols embedded in the test pattern. This occurs whenever the DUT and BERT are operated with independent clocks. Depending on the loopback implementation in the DUT, it can happen with synchronized clocks as well. When SKP OS or ALIGN filtering is enabled, the pattern generator sequence must use a test pattern version that includes SKP OS or ALIGNs. The error detector sequence must use an expected test pattern version without them. Respective patterns are part of the factory pattern library. This functionality requires M8046A-0S2 for PCIe, M8046A-0N2 for PCIe at 64 GT/s, M8046A-0S4 for USB 3.2, or M8046A-0S6 for SATA/SAS and an M8070B software revision 6.0 or later. M8046A-0N2 requires M8046A-0S2.

Table 24. Specifications for SKP OS and ALIGN filtering (M8046A Option -0S2, -0S4, -0S6).

Standard		Software revision and license needed
PCIe	64 GT/s with 1b/1b coding 8/ 16/ 32 GT/s with 128b/ 130b coding 5 GT/s with 8b/ 10b coding 2.5 GT/s with 8b/ 10b coding	Requires M8046A-0N2, -0S2 and M8070B SW rev 8.0 or later Requires M8046A-0S2 and M8070B SW rev 6.5 or later Requires M8046A-0S2 and M8070B SW rev 6.7 or later Requires M8046A-0S2 and M8070B SW rev 7.0 or later
CCIX	20 / 25 GT/s	Requires M8046A-0S2 and M8070B SW rev 6.5 or later
USB	5 Gb/s with 8b/ 10b coding 10 Gb/s with 128b/ 132b coding	Requires M8046A-0S4 and M8070B SW rev 6.7 or later
SATA/SAS	3 / 6 Gb/s with 8b/ 10b coding 12 Gb/s with 8b/ 10b coding	Requires M8046A-0S6 and M8070B SW rev 6.7 or later

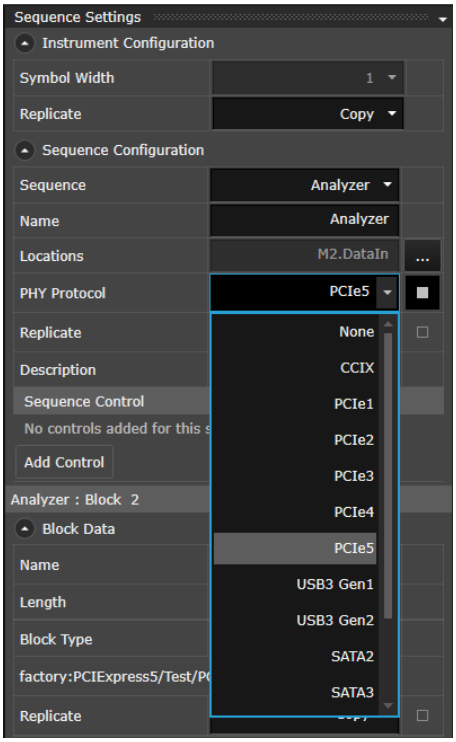


Figure 24. Users can select in the pattern sequencer menu between PCIe6, PCIe5, PCIe4, PCIe3, PCIe2, PCIe1, SAS 3, SAS 2, SAS 1, SATA 3, SATA 2, CCIX, USB 3.0 (5 Gb/s) or USB 3.1 (10 Gb/s) as PHY protocol to enable the SKP OS and ALIGN filtering feature with M8046A-0S2/-0N2 (PCIe), -0S4 (USB), or -0S6 (SATA/SAS).

Interactive Link Training for PCIe

In some industry standards, such as PCIe, the transmitter de-emphasis and receiver equalization must be optimized during a training sequence to compensate for the actual channel loss caused by PC board materials.

For testing receivers of such interfaces, you need an error analyzer that understands the low-level protocol of the bring-up sequence including speed changes and triggering changes of the pattern generator's de-emphasis setting.

M8046A provides a link training status state machine that supports PCIe 8, 16, 32 GT/s and 64 GT/s. It is suitable for testing the root complex and endpoint. It supports 2 channels; each M8046A requires a respective license set.

Prerequisites for this functionality:

- Module hardware: M8046A Option -0S1 (8 GT/s, 16 GT/s and 32 GT/s). Requires M8045A or M8042A and M8046A modules with a high-speed communication link (LINK 1234), which are available for all M8045A/M8046A serial numbers of MY/DExxx01000 or later. The M8046A-0A4 integrated clock recovery and a pattern generator with M8045A-0G4 de-emphasis or M8042A-0G4 de-emphasis are also required. M8046A-0S2 is recommended.
- Module hardware: M8046A Option -0N1 (64 GT/s). Requires M8045A and M8046A modules with a high-speed communication link (LINK 1234), which are available for all serial numbers of MY/DExxx01000 or later. The M8046A-0A4 integrated clock recovery and a pattern

generator with M8045A-0G4 de-emphasis or M8042A-0G4 de-emphasis are also required. M8046A-0S1, M8046A-0S2 and M8046A-0N2 are required.

- Software: M8070B rev 6.7 or later for M8046A-0S1, and M8070B rev 9.0 or later for M8046A-0N1. For interactive link training with M8046A and M8042A, M8070B rev 10.5 and M8045A module driver 3.5 or later are required.

Dynamic RX EQ for PCIe Link Training

M8046A now allows using the custom values of threshold and FFE coefficients for all PCIe data generations (Gen1-Gen6) during the Link Training process. This applies the back-channel settings that minimize the BER. Values must be specified in the RX EQ Matrix Editor.

The RX EQ Matrix Editor is available under the Analyzer menu.

This feature is applicable if PHY protocol mode is selected as PCIe3, PCIe4, PCIe5, or PCIe6 for the Error Detector. The option to enable and select saved settings is available under the “LTSSM” section of Data In.

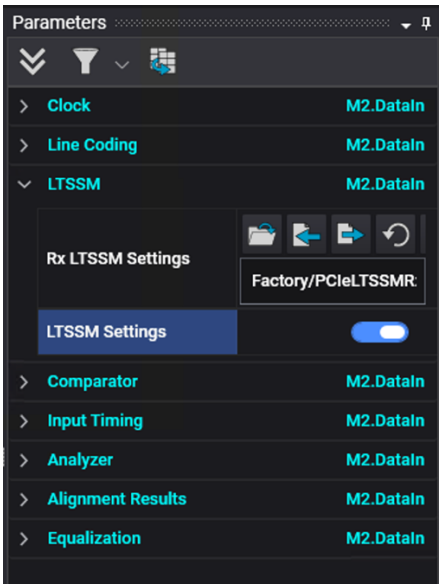


Figure 25. Rx LTSSM settings in the M8070B.

Interactive Link Training for USB 3.2

USB 3.2 compliance testing requires the product under test to enter loopback, a state at which the product under test sends the incoming bitstream at its receiver back from its transmitter without applying error correction. To enter loopback, the product under test must go through several LTSSM (Link Training and Status State Machine) handshakes during which the link speed and bandwidth are negotiated, as well as the receiver equalization fine-tuned.

M8046A provides a USB 3.2 interactive LTSSM that adapts to the timing requirements of the product under test, making the link training step trivial, helping you focus on the actual receiver test.

Furthermore, the USB 3.2 specification defines dual-lane (x2) mode for the USB Type-C connector. In this mode, both transmitters and receivers operate simultaneously, producing aggregate bit rates of 10 Gb/s (5 Gb/s x2) and 20 Gb/s (10 Gb/s x2). A product that can operate in x2 mode must be tested accordingly, as close as possible to operating conditions. To do so, the M8040A High-Performance BERT allows the usage of a second M8046A module to enable interactive link training functionality for both lanes concurrently.

Prerequisites for this functionality:

- Module hardware: M8046A Option -0S3. Requires M8045A and M8046A modules with a high-speed communication link (LINK 1234), which are available for all serial numbers of MY/DExxx01000 or later. The M8046A-0A4 integrated clock recovery is also required. M8046A-0S4 is recommended.
- If testing dual lane mode: a second M8046A module with the same configuration and an M8045A module with two licensed channels.
- Software: M8070B rev 7.5 or later.

Interactive Link Training Applications (Plugins)

Link training with the M8070B previously required multiple manual steps and detailed editing of sequence blocks. The Interactive Link Training application consolidates all necessary parameters in a single, easy-to-use interface. It is started from Application > Interactive Link Training in the M8070B by selecting either PCIe LTSSM or USB 3.2 LTSSM. Both plugins share the same user interface; only the tabs of the configuration panel differ.

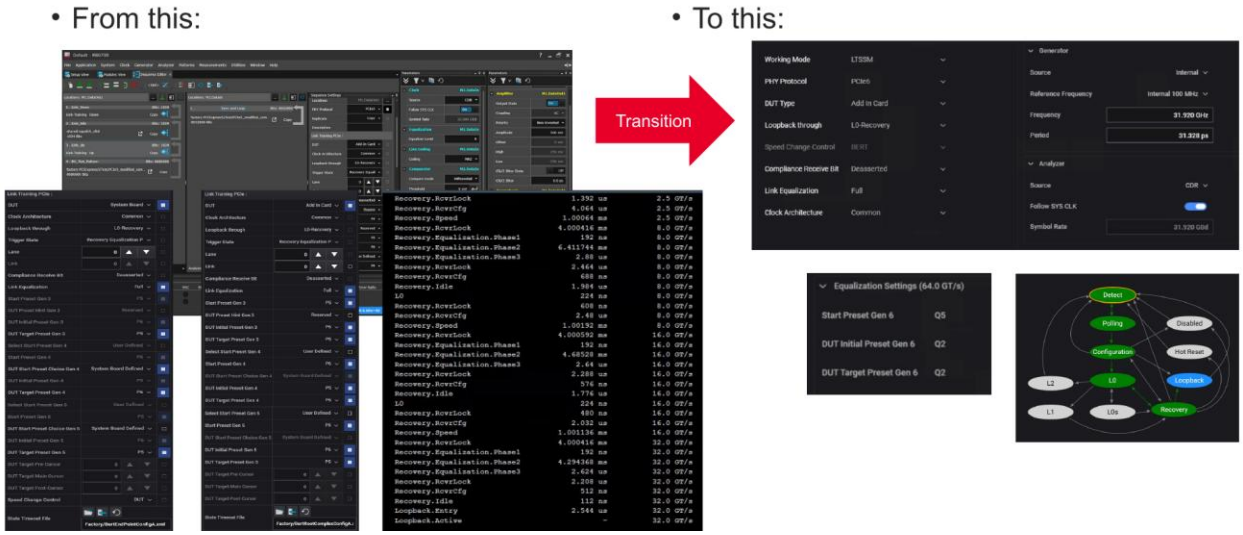


Figure 26. From sequence-based link training setup (left) to the Interactive Link Training application (right): only the mandatory LTSSM parameters, the equalization settings, and the bubble diagram are needed.

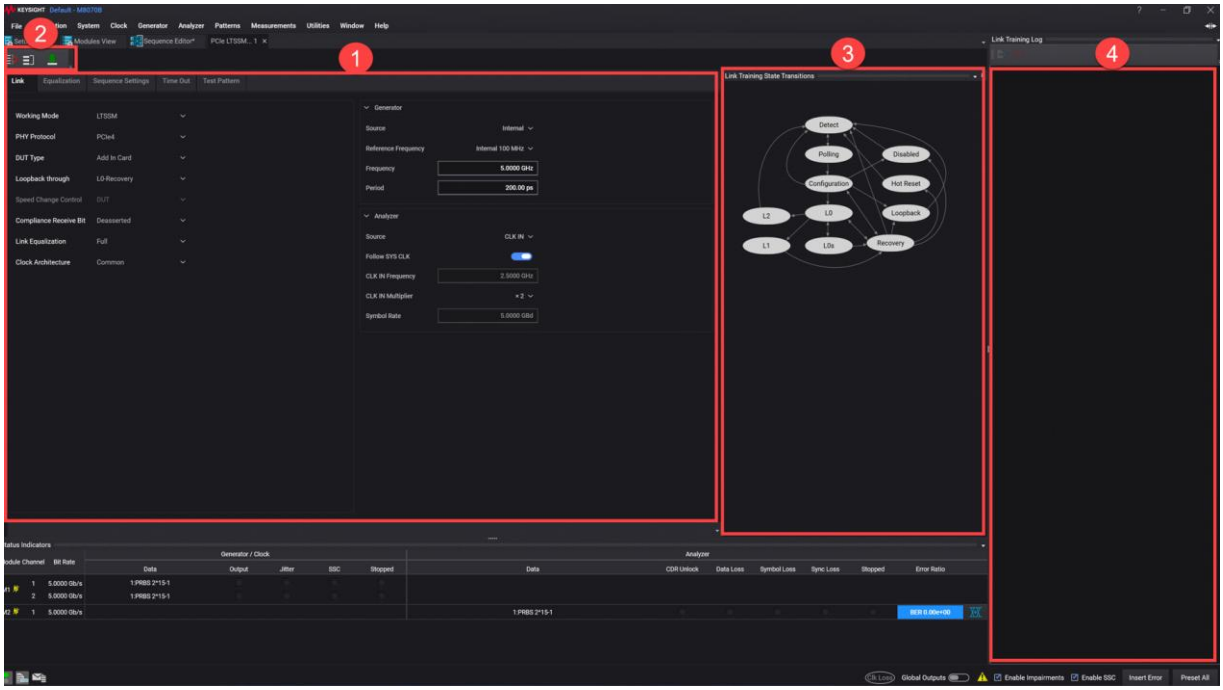


Figure 27. Interactive Link Training application for the PCIe LTSSM: (1) configuration panel, (2) toolbar with Break, Restart, and Download, (3) link training state transitions (bubble diagram), and (4) link training log.

The configuration panel provides only the essential parameters, so that no sequence blocks need to be managed in the Sequence Editor:

- PCIe LTSSM: Link tab (PHY protocol, DUT type, Loopback Through, Compliance Receive Bit, and clock settings) and Equalization tab (presets per PCIe generation and RX EQ matrix editor). Sequence Settings tab (trigger state, lane, link, and state timeout file) and Time Out tab (dedicated editor for all LTSSM state timeouts). Test Pattern tab (including inverse precoding and FEC decoding options for PCIe 6.0).
- USB 3.2 LTSSM: Link tab (PHY capability, target state, trigger state, LFPS period, duty cycle, Warm Reset LFPS cycle, generator SSC and analyzer settings). Signaling and Timing tab (tBurst, tRepeat-0/1, tPWM, and tLFPS-0/1). Loopback Pattern tab and Connection Diagram tab with the recommended x1 and x2 hardware setups.

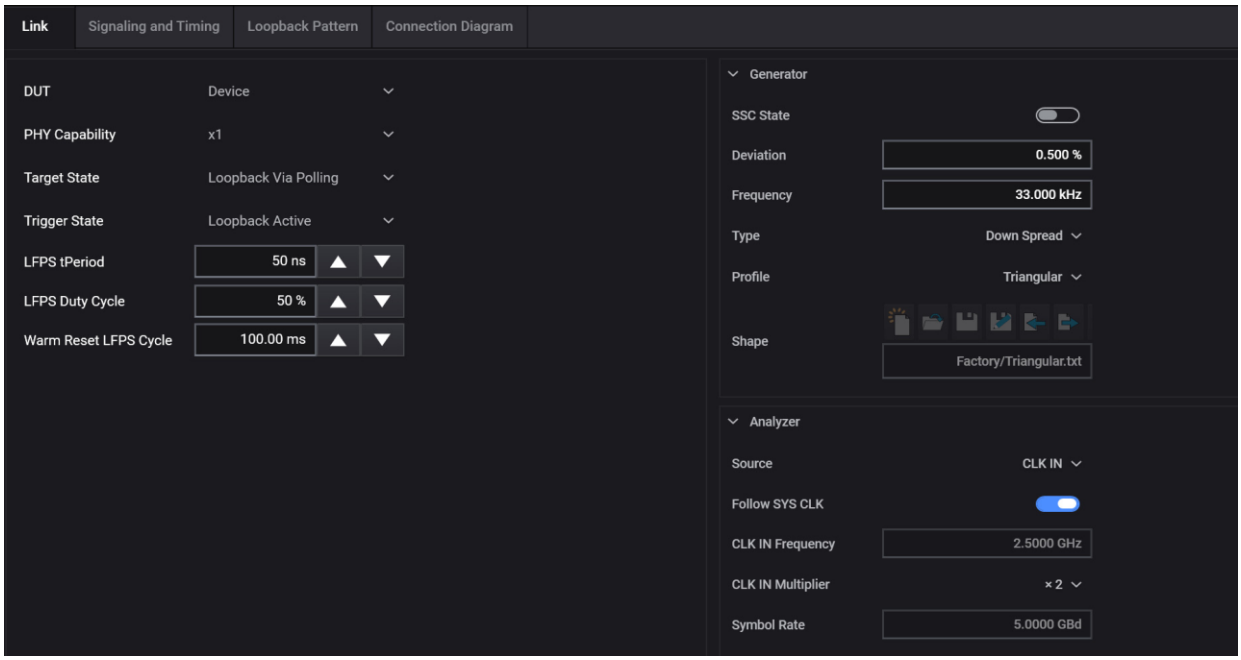


Figure 28. Link tab of the USB 3.2 LTSSM configuration panel with the target state Loopback Via Polling, LFPS settings, and generator SSC settings.

Bubble Diagrams and Link Training Log

The Link Training State Transitions window visualizes the LTSSM flow as a bubble diagram, so that a successful or failed link training can be verified at a glance without analyzing lengthy log files. Passed states are shown in green, failed states in red, and the last active state in blue. States that are not supported by the BERT, such as L0s, L1, L2, Hot Reset, and Disabled, are shown in gray. Clicking a state shows its sub-states, timeout values, execution times, and transfer rates. Since LTSSM transitions typically take only milliseconds, the Replay button replays the complete link training step by step.

The Link Training Log lists all executed steps with time stamps, including the exchanged transmitter equalization presets, and identifies the root cause of a failure, for example an unexpected LTSSM state change. The log can be exported for documentation.

Benefits at a glance

- Fewer configuration steps: one panel with the mandatory parameters instead of multiple sequence blocks
- Easier debugging: timeouts can be edited directly, and the selected bubble highlights the corresponding state in the Time Out tab
- Immediate pass/fail visibility of every LTSSM state and transparent sub-state timing
- One application for two protocols, remote-controllable via SCPI (:PLUGin:LTSSMTest subsystem)

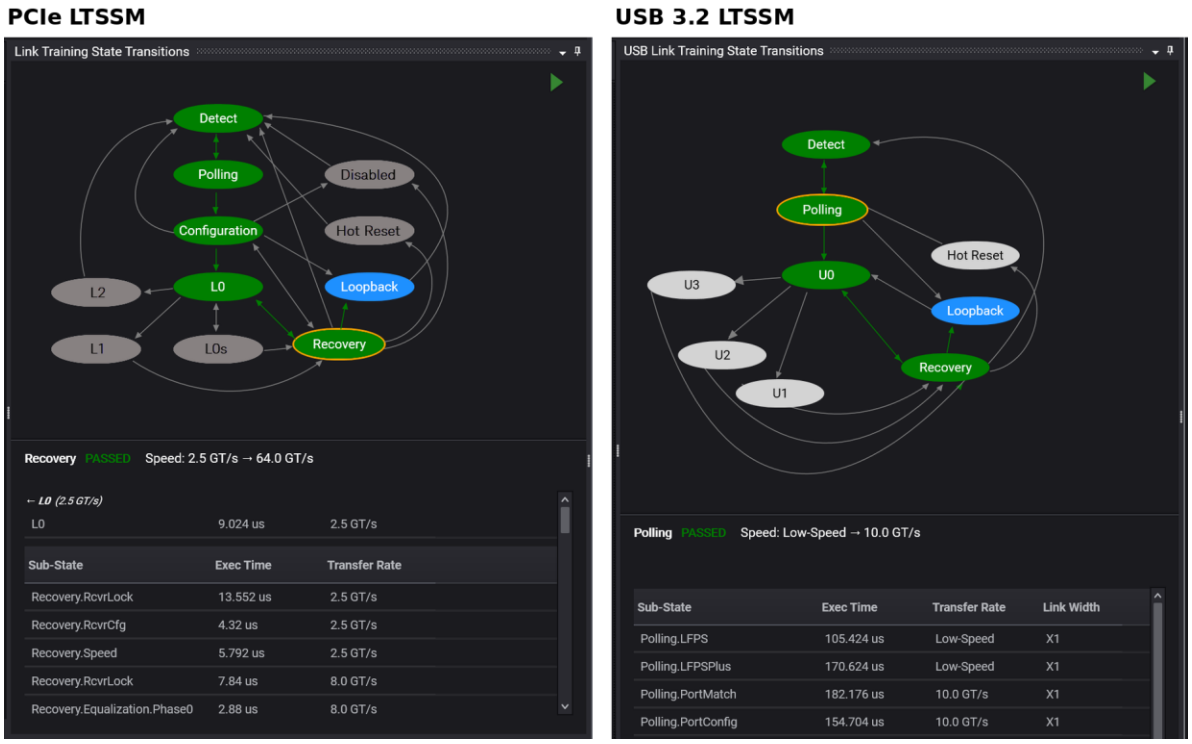


Figure 29. LTSSM bubble diagrams of the PCIe LTSSM (left) and USB 3.2 LTSSM (right) plugins. The tables below the diagrams list the sub-states of the selected state with execution time, transfer rate, and link width.

Specifications for M8046A Analyzer Module

Overview

The Keysight M8043A and M8046A error analyzer modules support flexible receiver test configurations and can be used either standalone or in combination with the M8045A pattern generator. For symbol rates above 64 GBd, a real-time oscilloscope-based error analysis approach (using the Infiniium UXR-Series) is supported and fully automated through the M8070B system software. In addition, a DUT's internal error counter can be accessed via the DUT Control Interface (DCI), enabling automated receiver measurements such as jitter tolerance testing.

The following table provides an overview of available error analysis choices for the M8040A BERT platform:

Parameter	M8043A Error Analyzer	M8046A Error Analyzer	Infiniium UXR Real-time Oscilloscope
Supported symbol rates @ PAM4	2.4 to 64 GBd	2.4 to 58 GBd	14 to 224 GBd
Applications	400/800G Ethernet, 112G LPO (Linear interfaces as per LPO-MSA and OIF-CEI PAM4-LINEAR), PCIe 7.0 128 GT/s [1]	PCIe up to 6.x 64 GT/s and lower, USB 3.2, USB4, MIPI M-PHY	1.6/3.2T Ethernet, PCIe 7.0 / 8.0 pathfinding, custom SerDes
Line coding	NRZ, PAM4	NRZ, PAM3, PAM4	NRZ, PAM3, PAM4, PAM6, PAM8
Filtering of filler symbols	SKP OS Filtering for PCIe 128 GT/s (option -0S2)	SKP OS Filtering for PCIe 2.5, 5, 8, 16, 32, and 64 GT/s (options -0S2, 0N2) and CCIX 20/25 Gb/s (option -0S2) SKP OS Filtering for USB 3.2, dual lane (option –0S4) ALIGN Filtering for SATA 3G/6G and SAS 3G/6G/12G (option -0S6)	No
Interactive link training	PCIe LTSSM for 128 GT/s (option -0S1)	PCIe LTSSM for 8, 16, 32, and 64 GT/s (options -0S1, -0N1) USB 3.2 LTSSM, dual lane (option -0S3)	No

1. The support is limited to the base specification only (no SSC).



Figure 30. Front panel of M8046A.

The M8046A supports symbol rates up to 32 Gbaud (both NRZ and PAM4) and 58 Gbaud (PAM4) or 64 Gb/s (NRZ), the default is 32 Gbaud and NRZ format. The analyzer module can be used for error analysis in conjunction with the M8045A pattern generator and the M8195A/M8196A arbitrary waveform generator. For the following functions a separate module option is required:

- PAM3/4 decoding up to 32 Gbaud (M8046A Option -0P3), extension to 58 Gbaud (M8046A Option -0P6)
- Equalization for symbol rates above 32.4 Gbaud (M8046A Option -0A3)
- Analyzer, 1 channel, data rate up to 64 Gbaud, NRZ (M8046A Option -A64)
- Clock recovery up to 32 Gbaud (M8046A Option -0A4), extension to 64 Gbaud (M8046A Option -0A5)
- Interactive link training for PCIe 8/ 16/ 32 GT/s (M8046A Option -0S1)
- Interactive link training for USB 3.2, 5/ 10 Gb/s, x1/ x2 (M8046A Option -0S3)
- Interactive link training extension for PCIe 64 GT/s, requires M8046A-0S1/US1 (M8046A Option -0N1)
- SKP OS filtering for PCIe 2.5[1)]/ 5/ 8/ 16/ 32/ 64 GT/s and CCIX 20/25 Gb/s (M8046A Option -0S2)
- Filtering of SKP OS extension for PCIe 64 GT/s, requires M8046A-0S1/-US1 (M8046A Option -0N2)
- SKP OS filtering for USB 3.0, 3.1, 3.2 (M8046A Option -0S4)
- ALIGN filtering for SATA 3[1]/6 Gb/s and SAS 3[1]/6/12 Gb/s (M8046A Option -0S6)
- PAM3 inverse pre-coding for USB4v2 (M8046A Option -0P3)

[1] Requires integrated clock recovery M8046A Option -0A4/-0A5

Data Input (DATA IN)

Table 25. Data input characteristics for M8046A.

Parameter	Value
Symbol rate [7]	2.45 to 32.4 Gbaud NRZ for M8046A-A32, 2.45 to 32.4 Gbaud PAM3/4 for M8046A-A32 with -0P3 For modules with a serial number below MYxxx02000 the range is 5.0 to 30.0 Gbaud 2.45 to 64.8 Gbaud NRZ for M8046A-A64 2.45 to 58 Gbaud PAM3/4 for M8046A-A64 with -0P3, -0P6 and -0A3 (all specifications are valid up to 53.2 Gbaud with over-programming). Requires serial number above MYxxx02000.
Channels per module	1
Data format	NRZ (default) PAM3 (requires M8046A Option -0P3 and for symbol rates above 32.4 Gbaud M8046A Option -A64, -0P3, -0P6, -0A3) PAM4 (requires M8046A Option -0P3 and for symbol rates above 32.4 Gbaud M8046A Option -A64, -0P3, -0P6, -0A3)
Max # of M8046A per M9505A chassis	up to 4

Input sensitivity [1, 3, 7]	For symbol rates from 2.45 to 32.4 Gbaud for NRZ and PAM4: 12% of input range setting + 30 mV eye height per eye, single ended and differential. For BER of 10^{-12}. **NRZ:** 32.5 to 64.2 Gb/s: 16% of input range setting + 35 mV eye height single ended and differential. For BER of 10^{-12} **PAM3/4:** 32.5 to 53.2 Gbaud [2]: 12% of input range setting + 15 mV eye height per eye, single ended and differential. For BER of 10^{-6} For modules with a serial number below DExxx00515 these specifications apply: NRZ: 70 mV single ended and differential PAM4: 70 mV per eye single ended and differential
Max input voltage amplitude	1600 mVpp differential for balanced patterns. 1000 mVpp differential for non-balanced patterns. For modules with serial number below DExxx00515: 1000 mVpp differential for balanced and non-balanced patterns
Input voltage window	-1 V to +3 V
Termination voltage [5]	-1 V to +3 V for modules with serial number above DExxx00515
Timing resolution	0.1 ps
Input bandwidth (3 dB)	16 GHz with smooth roll-off
Sampling point	Manual[6] and automatic. Finds optimum voltage range, threshold and delay of the sampling point. Delay accuracy is 20 mUI or 1.5 ps whichever is higher. [4] One sampling edge per UI.
Decision threshold range	Full input voltage range with 1 mV resolution
Equalizer modes	• Automatic equalizer coefficient optimization • Equalizer presets with standard analyzer data input cable compensation. The equalizer gain is controlled as equalizer level, and the losses of the standard cabling are automatically included in the equalizer setting • Manual coefficient entry with cable compensation. The coefficients of the FFE (Feed Forward Equalizer) can be entered manually. Additionally, the losses of the standard cabling are automatically included in the equalizer setting • Manual coefficient entry. The coefficients of the FFE can be entered manually. No cable losses are automatically compensated. Use this mode when using non-standard cabling.
Automatic equalizer coefficient optimization	Requires an input signal with random-like pattern. It is an iterative procedure to minimize BER. This function requires M8070B software rev 6.0.210 or later. This table shows the maximum loss [8] that can be compensated for symbol rates above 32 Gbaud:

Symbol rate	NRZ With external clock [9]	NRZ With CR	PAM3/4 With external clock [9]	PAM3/4 With CR
32 Gbaud	18.5 dB	16.5 dB	11.0 dB	9.0 dB
35 Gbaud	18.0 dB	16.0 dB	10.0 dB	8.5 dB
40 Gbaud	16.0 dB	16.0 dB	9.5 dB	8.5 dB
45 Gbaud	15.0 dB	13.0 dB	8.5 dB	8.5 dB
50 Gbaud	14.5 dB	12.5 dB	7.5 dB	5.0 dB
53.125 Gbaud	14.0 dB	12.0 dB	5.0 dB	1.5 dB
56 Gbaud	13.5 dB	12.0 dB	1.5 dB	0 dB
58 Gbaud	13.0 dB	12.0 dB	0 dB	0 dB

External redriver	For higher channel loss compensation, e.g. for testing PCIe server boards, the M8047A/B/C can be used together with M8046A. M8047A/B/C can be controlled from M8070B. See M8047A/B/C data sheet for more details.
Equalizer presets with cable compensation	For symbol rates up to 32 Gbaud: Up to 13 dB at 32.4 Gbaud NRZ. Up to 5.5 dB at 29 Gbaud PAM4. Up to 5.1 dB at 26.5625 Gbaud PAM4 FFE with 55 presets for PAM4 and 120 presets for NRZ. See figure below. No Equalizer license is needed below 32 Gbaud. For symbol rates above 32 Gbaud: the use of presets is not recommended. Please use automatic equalizer tap optimization instead: Up to 3 dB at 58 Gb/s for NRZ signals. (requires M8046A-0A3 and -A64): 120 presets for NRZ, FFE.
Manual equalizer coefficients	16 (FIR) filter coefficients, numbered from 0 to 15. Coefficient 2 is the main-cursor and cannot be changed. The available value range is: • Coefficient 0: -0.25 to + 0.25 • Coefficient 1: -0.5 to + 0.5 • Coefficient 2: 1.0 • Coefficient 3: -0.5 to +0.5 • Coefficient 4: -0.25 to + 0.25 • Coefficient 5: -0.125 to +0.125 • Coefficient 6 to 15: -0.0625 to +0.0625 The sum of all 16 coefficients may not be 0
Phase margin NRZ Phase margin PAM4	1 UI – 12 ps typical for PRBS 2^{15}– 1 @ BER of 10^{-12} 1 UI – 8 ps typical for clock pattern @ BER of 10^{-12} 280 mUI typical, measured at 26.5625 Gbaud with PRBS 2^{15}-1 @ BER of 10^{-12} 200 mUI typical, measured at 32.4 Gbaud with PRBS 2^{15}-1 @ BER of 10^{-12} 100 mUI typical, measured at 53.2 Gbaud with PRBS 2^{15}-1 @ BER of 10^{-6}
Interface	Differential: 100 Ω nomina Single ended: 50 Ω nominal DC coupled, terminate unused input with 50 Ω For modules with a serial number below DExxx00515: AC coupled, terminate unused input with 50 Ω
Connectors	2.4 mm, female

1. Measured with PRBS 2^{15} – 1
2. Measured between 100 and 400 mV input range and with a module serial number MYxxx02000 and higher
3. Valid at room temperature.
4. With 48 to 52% duty cycle at CLK IN signal.
5. Termination voltage must be within a window of DC common mode voltage ± 1.5 V.
6. For symbol rates < 4.9 Gbaud the automatic alignment is recommended after recovery from clock loss
7. For serial numbers below MYxxxx2100 the minimum symbol rate is 5 Gbaud, CDR mode only.
8. Measured with M8049A-002 and M8049A-003 and automatic equalization optimization
9. Measured with a clean clock from M8045A channel clock output

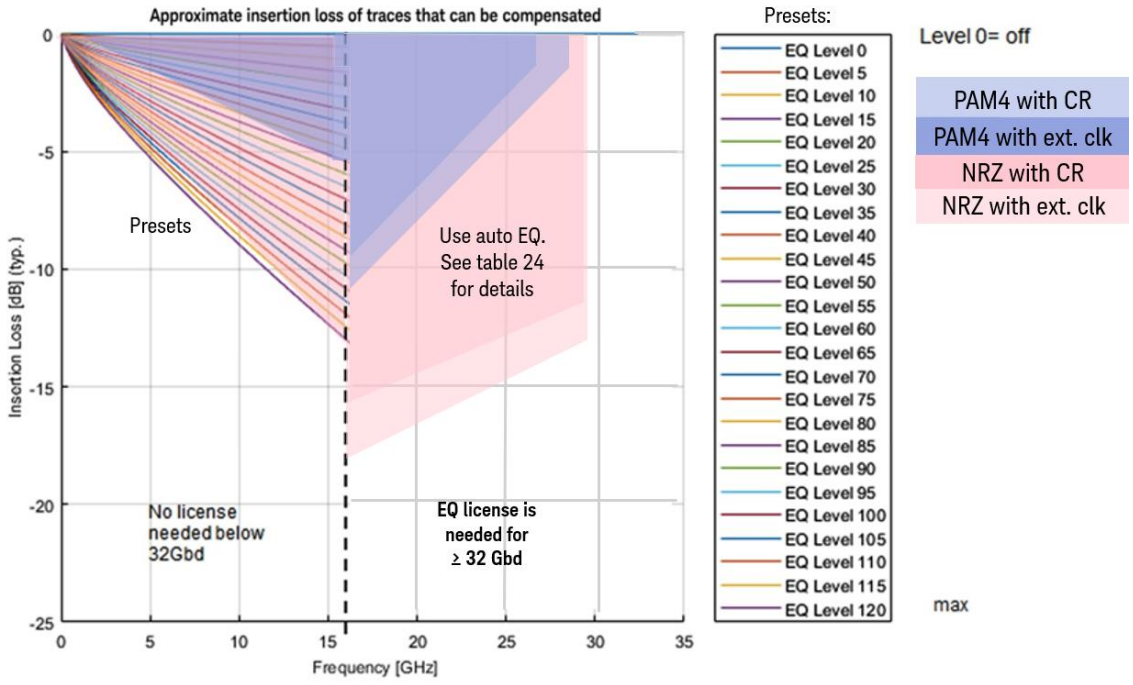


Figure 31. The M8046A provides built-in equalization to reduce channel loss in the loopback channel. The available ranges for PAM4 and NRZ signals up to 64 Gbaud are shown here. For symbol rates above 32 Gbaud the M8046A-0A3 equalizer option is required.

Table 26. Specifications for integrated clock recovery (requires M8046A option 0A4, 0A5).

Parameter	Comment	Value for M8046A Option 0A4/UA4 and 0A5/UA5
Clock recovery symbol rate range [2]		NRZ: 2.45 to 32.4 Gb/s (requires M8046A option -0A4) NRZ: 2.45 to 64.8 Gb/s (requires M8046A options -A64, -0A4 and -0A5) PAM3/4: 2.45 to 32.4 Gbaud (requires M8046A with options -0A4 and -0P3) PAM3/4: 2.45 to 58 Gbaud (all specifications are valid up to 53.2 Gbaud with over-programming), (requires M8046A options -A64, -0A4, -0A5, -0P3, -0P6, and -0A3)
Selectable loop type	First and second order PLL - see figure below for description	Yes
Tunable loop bandwidth [3]		2 to 20 MHz. For second order PLL the range depends on selected peaking. 4 to 16 MHz with PAM4 and symbol rate > 32.4 Gbaud [1]
Loop bandwidth accuracy		± 30% typical for symbol rates ≥ 4.9 Gbaud and loop bandwidth < 16 MHz
Transition density		25-100%
Clock recovery peaking range		Up to 4 selectable settings (dependent on loop bandwidth and baud rate)

Acquisition	Input symbol rate must be within the range of ± 500 ppm of the set symbol rate	± 500 ppm typical
Tracking range	SSC can be tracked when symbol rate is set to center frequency. SSC frequency ≥ 30 kHz	± 3000 ppm typical (for symbol rate up to 32.4 Gbaud)
CDR freeze		Not provided

1. There is no limitation to set the loop bandwidth in the range of 2 to 20 MHz, but it may not lock.
2. For SN below 2100 minimum symbol rate is 5 Gbaud, below SN 2100 min symbol rate is 5 Gbaud.
3. Below 4.05 Gbaud maximum loop bandwidth is 10 MHz

First order PLL (type 1)

- A type 1 is defined by bandwidth. No peaking.
- JTF bandwidth = OJTF bandwidth.
- Used by some communication standards

Second order PLL (type 2)

- A type 2 is defined by JTF loop bandwidth. No peaking.
- JTF bandwidth > OJTF bandwidth.
- Used by some computing standards

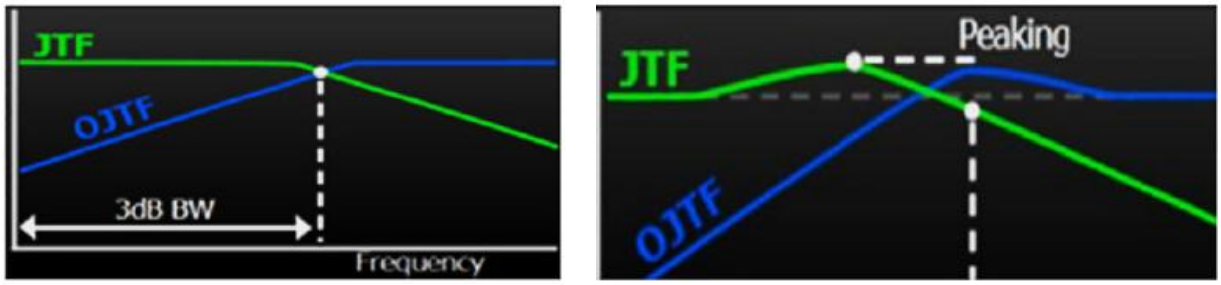


Figure 32. The M8040A provides a built-in clock recovery option. You can choose between a first and second order PLL characteristic.

External Clock Input (CLK IN)

Table 27. Specifications for clock input of analyzer.

Parameter	Value
Amplitude	Minimum 200 mVpp, maximum 1 Vpp
Frequency range [1]	2.5 to 32.4 GHz Note: In clk “x 2” mode for symbol rates above 25 Gbaud an external bandpass filter (M8061A-803) has to be used on the clock input. The filter has to be removed for symbol rates below 25 Gbaud. In clk “x 1” mode no filter is needed.
Multiplier internal	1.2
Connector	3.5 mm, female

1. Below 5 GHz transition time of clock signal should be < 25 ps

Recovered Clock Output (REC CLK OUT)

This output provides a recovered clock when using the integrated clock recovery function of M8046A. It can be used to trigger a DCA sampling oscilloscope. It is only provided for M8046A modules with S/N above DExxx1000.

Table 28. Specifications for recovered clock output of analyzer.

Parameter	Value
Amplitude	Fixed 600 mVpp typical
Symbol rate 4.9 to 32.4 Gbaud	Symbol rate at data inputs/2 (maximum of 16.2 GHz)
Symbol rate ≥ 32.4 Gbaud	Symbol rate at data inputs/4 (maximum of 16.2 GHz)
Connector	3.5 mm, female

SYNC Input (SYNC IN)

Can be used to clock the analyzer from the pattern generator's M8045A system clock via the sync output A/B (requires cable M8051A-801). Not needed if external clock is used. This input is only available for M8046A modules with a serial number below DExxxx01000.

Control Input A (CTRL IN A)

Functionality can be configured as sequence trigger or pattern capture event.

Table 29. Specifications for control inputs of analyzer.

Parameter	Value
Input voltage	-1 to -3 V
Termination voltage	-1 to -3 V
Termination voltage accuracy	± (25 mV +1%)
Threshold voltage	-1 to -3 V
Response time	± 512 UI repeatability
Connector	3.5 mm, female

Control Output (CTRL OUT A)

Outputs a pulse in case of an error. Generates a pulse or static high/low when controlled by the sequencer.

Table 30. Control output specifications for M8046A.

Parameter	Value
Amplitude	0.1 to 2 V
Output voltage	- 0.5 to 1.75 V

Delay from data input	< 1 ms, repeatability ±512 UI (requires M8070A software 4.5/ M8070B 6.0 or later)
Connector	3.5 mm, female

Communication Link (LINK 1234)

This communication link provides a low-latency communication path between M8045A and M8046A modules for enabling interactive link training, e.g., for 5/8/16/32 GT/s PCIe. It requires the cable M8051A-801. This interface is available for M8046A modules with a serial number above DExxx01000. Upgrades are available for older serial numbers (M8046A-US1, requires return-to-Keysight).

M8046A Error Detector Measurement Capabilities

Table 31. Measurement capabilities.

Parameter	Comments	M8070A	M8070B	M8070ADVB	M8070EDAB
BER, SER	Accumulation and instantaneous	Yes	Yes		
Jitter tolerance		Yes	No	Yes	
BER Scan with RJ, DJ separation		No [2]	No	No [2]	
Output level and Q-factor		No	No	No	
Sampling point view		Yes[1]	Yes		
Automated de-emphasis optimization	• Scope-based: Optimize TDECQ or Eye Opening (See table below for supported DCA) • BER-based: Minimize BER (via error analyzer or DCI)	No	No	Yes	
		No	No	Yes	
Real-time oscilloscope-based error analysis	See table below for details	No	No	Yes	
Counters	Compared bits, errored bits Compared 0 bits, errored 0 bits Compared 1 bits, errored 1 bits Compared symbols, errored symbols	Yes	Yes		

	Compared symbols 0, 1, 2, 3 Errored symbols 0, 1, 2, 3				
BER versus parameter automated sweep		Yes	No	Yes	
Error distribution analysis		No	No	No	Yes

1. Requires M8070A SW 4.0/M8070B SW 6.0 or later.
2. The measurement is available in the user interface, but just for debugging/troubleshooting purposes. The accuracy of jitter separation results is unspecified in case of NRZ and invalid in case of PAM4 signals.

External Clock Recovery

The Keysight N1076A/B, N1077A, N1078A electrical and optical clock recovery units can be used to recover a clock from NRZ and PAM4 patterns to clock the M8046A error analyzer. The clock recovery units can be controlled from the M8000 system software for BER and jitter tolerance testing.

Table 32. Conditions for use of external clock recovery.

Parameter	N1076A/77A	N1076B/78A	
Symbol rate	PAM4: 0.05 to 32.8 Gbaud (characteristic) [1]	PAM4: 0.125 to 65.6 Gbaud (characteristic) [1]	
Sensitivity with recommended accessories	30% of input range + 45 mV for M8046A with serial number above DExxx00515 (single ended and differential). For M8046A modules with a serial number below DExxx00515 these specifications apply: NRZ: 200 mV PAM4: 120 mV per eye		
Number of consecutive symbols without transition	NRZ: 144 PAM4: 72 (144 bit)		
Measurements	Jitter tolerance, BER		
Software pre-requisites	M8070A 3.6 or higher N1010A Flex DCA A.05.61 or higher, no extra licenses needed	M8070B 6.0 or later and M8070ADVB N1010A Flex DCA A.05.80 or higher, no extra licenses needed	
	Note: The M8070A/B and the N1010A controlling the external clock recovery units should run on the same controller. The N1010A Flex DCA software cannot be operated interactively while being controlled by M8070A/B. If a DCA-M is used in the same test setup, we recommend controlling it from a second PC/ controller.		
Hardware pre-requisites	N1076A-232 or N1077A-232 for symbol rates above 16 Gbaud M8046A-A32 with serial number above DExxx00200.	For symbol rates above 32 Gbaud: N1076B-264/N1078A-264 and M8046A-A64	
Recommended accessories (for differential signals)	• Qty 1 of Keysight N1027A-2P2 microwave pick-off tee, 2.4 mm connectors, matched pair	For rates above 32 Gbaud: • Qty 1 of Keysight N1027A-2P1	For rates below 30 Gbaud: • Qty 1 of Keysight N1027A-2P8

	• Qty 2 of Keysight 11900B adapter 2.4 mm (f) to 2.4 mm (f)	microwave pick-off tee, 1.0 mm connectors, matched pair • Qty 2 of Keysight 11921B adapter 1 mm (m) to 1.85 mm (f) • Qty 2 of Keysight 11921F Adapter 1.85 mm (f) to 1.0 mm (f)	microwave pick-off tee, 1.85 mm connectors, matched pair • Qty 2 of Keysight 11900B adapter 2.4 mm (f) to 2.4 mm (f)
	• Qty 2 of Keysight 83059A adapter 3.5 mm (m) to 3.5 mm (m) for mounting the pick-off tee directly to inputs of N107xA/B • Qty 1 of Keysight M8046A-802 matched cable pair 2.4 mm, 2 ps		

1. Range depends on selected option.

Error Analysis Using Infiniium UXR-Series Oscilloscopes

For symbol rates up to 58 GBd with support for PCIe and USB 3.2 interactive link training, the M8046A error analyzer module is available. For symbol-pattern error analysis up to 64 GBd, the M8043A error analyzer module can be used.

For symbol rates above 64 GBd, the M8000 system software (M8070B) supports the use of Keysight Infiniium UXR-Series real-time oscilloscopes as a BERT error detector.

The **M8070ADVB** Advanced Measurement Package is required and allows the UXR-Series real-time oscilloscope to be controlled from the M8070B system software.

In this configuration, the oscilloscope captures the high-speed waveform, which is then decoded into a pattern stream. The M8000 system software uploads the acquired data, performs pattern synchronization, and compares the received data against the expected pattern, including long PRBS polynomials such as PRBS31Q.



Figure 33. UXR-Series oscilloscope used as an error detector alongside the BERT pattern generator.

This approach enables measurement of target BERs down to approximately 10^{-6} to 10^{-7} at symbol rates up to 224 GBd within typical measurement times of around one minute. The Infiniium UXR-Series oscilloscope provides highly configurable equalization and integrated clock recovery supporting symbol rates up to 224 GBd. Pattern-based equalization is also supported, allowing users to define a known pattern and optimize equalization parameters for accurate high-baud-rate error analysis.

Typical key capabilities of the Infiniium UXR-Series real-time oscilloscopes include:

- **Analog bandwidth:** Up to **110 GHz**, enabling direct capture of ultra-high-speed serial signals.
- **Real-time sampling rate:** Up to **256 GSa/s**, providing high time resolution for accurate waveform reconstruction and jitter analysis.
- **ADC resolution:** High-resolution **10-bit** ADC architecture, supporting improved vertical resolution and better noise performance.
- **Integrated clock recovery:** Built-in clock recovery supporting symbol rates up to **224 GBd**, suitable for NRZ and PAM4 signaling.
- **Advanced equalization:** Configurable CTLE, FFE, and decision-feedback equalization (DFE), including pattern-based equalization, optimized for very high baud rates.
- **Deep acquisition memory:** Supports long record lengths (up to **2 Gsamples**) to enable sustained BER measurements, rare-event analysis, and decoding of long PRBS sequences.

For example, in addition to the FFE and CTLE parameters typically available in BERT error detectors, the DFE of the oscilloscope can be used, and the DFE parameters are fully accessible within the M8070B. The oscilloscope does not provide an automatic setting for the CTLE but provides automatic optimization for the DFE and FFE. The following equalization combinations can be used: CTLE, FFE, DFE, CTLE + FFE, CTLE + DFE, and FFE + DFE.

For more details, please refer to the M8070ADVB Advanced Measurement Package User Guide and the related application note "BER Measurement with Real-Time Oscilloscope Integrated in M8070B Software".

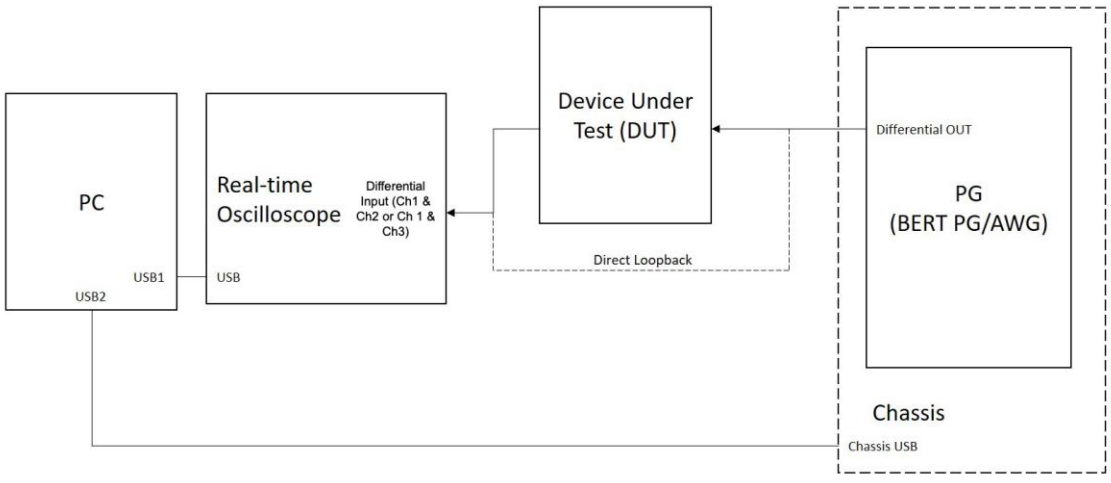


Figure 34. Block diagram of the setup where a real-time oscilloscope is used as an error detector.

Table 33. Specifications for error analysis with M8070ADVB using a real-time oscilloscope.

Parameter	Value
Symbol rates and Supported real-time oscilloscope models	Maximum symbol rate is limited by the UXR model: 14 GBd to 60 GBd for UXR0334A or B 14 GBd to 60 GBd for UXR0402/4A, AP, B, or BP 14 GBd to 75 GBd for UXR0502/4A or B 14 GBd to 96 GBd for UXR0592/4A, AP, B, or BP 14 GBd to 105 GBd for UXR0702/4 A, AP, B, or BP 14 GBd to 160 GBd for UXR0802/4A or B 14 GBd to 180 GBd for UXR0802/4A or B with the 90 GHz upgrade 14 GBd to 200 GBd for UXR1002/4A or B 14 GBd to 224 GBd for UXR1102/4A or B
Hardware acceleration	Hardware acceleration is active for 256 GSa/s UXR models when parameters are set in the M8070B with M8070ADVB to meet all of the following conditions: Symbol rate: 51.2 GBd to 224 GBd CDR type: 2nd order PLL CDR loop bandwidth: Symbol rate / 2655 to Symbol rate / 500 Measurement time compared with hardware acceleration inactive: JTOL measurements: reduced by a factor of 1.8 (meas.) BER measurements: reduced by a factor of 2.5 to 3.5 (meas.) When hardware acceleration is active. Display shall be turned OFF to achieve fastest measurement times. Factor of acceleration depends on parameter settings of the UXR such as e.g., line coding, baud rate, bits per acquisition and is provided as an estimation.
Target BER	Hardware acceleration active: ~10^{-7} Hardware acceleration inactive: ~10^{-6}
Coding	NRZ, PAM4, PAM6, and PAM8
Pattern capture	Yes
Masking	Expected bits can be masked (ignored) during error counting. Bitwise and block-wise masking is possible.
Expected patterns	User definable: PRBS 2^n-1 with n = 7, 9, 10, 11, 13, 15, 23, 31, 33, 35, 39, 41, 45, 47, 49, 51 Memory patterns with max. pattern length of 256 kbit
Measurements	Jitter tolerance, BER and SER Error distribution analysis (restrictions with respect to memory depth of UXR to be able to capture maximum frame length may apply) Automated parameter sweep versus BER
Measurement time	Depends on: Expected pattern type Expected pattern length (in case of memory patterns) Symbol rate Equalizer usage and parameters Acquisition depth in UI Target BER and confidence level
BER and symbol counters	BER counters: Compared bits Errored bits Compared 0 bits, compared 1 bit

	Errored 0 bits, errored 1 bit Symbol counters: Compared symbols Errored symbols For each symbol level: Compared symbols Errored symbols
Error distribution statistics	Yes, for details see Table 42. Requires M8070EDAB license.
Parameters	Acquisition Number of bits per acquisition. (Note: The maximum number of bits per acquisition is limited by the oscilloscope's acquisition memory depth, symbol rate and clock recovery setting.) Global acquisition bandwidth limit Channel bandwidth limit and filter type Pattern capture up to 100 Mbit Horizontal reference clock: internal, external 10 MHz and 100 MHz Clock: Follow Sys Clock, symbol rate Line Coding: Coding (NRZ, PAM4, PAM6, PAM8) Symbol mapping (uncoded, Gray, custom) Custom symbol mapping Comparator: Compare mode (single-ended / differential) Polarity (non-inverted / inverted) Auto-set thresholds User-defined thresholds Equalizer FFE - Number of taps and pre-taps FFE - Auto-set coefficients CTLE - DC gain CTLE - Frequency pole #1, Frequency pole #2, CTLE - Frequency zero #1 DFE- Taps DFE - Auto-set coefficients Clock Recovery (2nd Order CR) Loop bandwidth Symbol rate divider Damping factor Sample delay (PAM4 only) Auto alignment Covers thresholds, sample delay and equalizer coefficients Automatically set scope parameters: Thresholds FFE coefficients (cannot be changed by user) Sample delay position (in case of NRZ)
Software pre-requisites	UXR: Infiniium version 11.40.00202 or higher M8070B: M8000 system software. See Table 44 for minimum required software revision M8070ADVB advanced measurement package software. See Table 44 for minimum required software revision.
Measurement packages	Following licenses are required on the oscilloscope in addition: D9020PAMA or D9320PAMA Pulse Amplitude Modulation PAM-N analysis software D9020ASIA or D9320ASIA Advanced signal integrity software (Equalization, InfiniiSim, Crosstalk Analysis)
Controlling connection to UXR	LAN recommended

User Interface and Remote Control

M8070B System Software Overview

The M8070B system software for the M8000 Series of BER test solutions is required to control the M8040A BERT.

The Keysight **M8070B system software** is the central control, configuration, and analysis platform for the M8000 Series bit error ratio tester (BERT) systems including the M8050A BERT platform. It provides a unified user interface and software framework for controlling pattern generators, error analyzers, clock modules, interference sources, and associated instruments within the M8000 ecosystem.

Designed for high-speed digital and optical interconnect validation, the M8070B supports symbol rates from low-speed applications up to 224 GBd, covering NRZ and PAM4 signaling, and enabling comprehensive physical-layer and link-layer test workflows.

For the remote-control interface, feature tables of the software packages, and system requirements, see the Data Sheet.

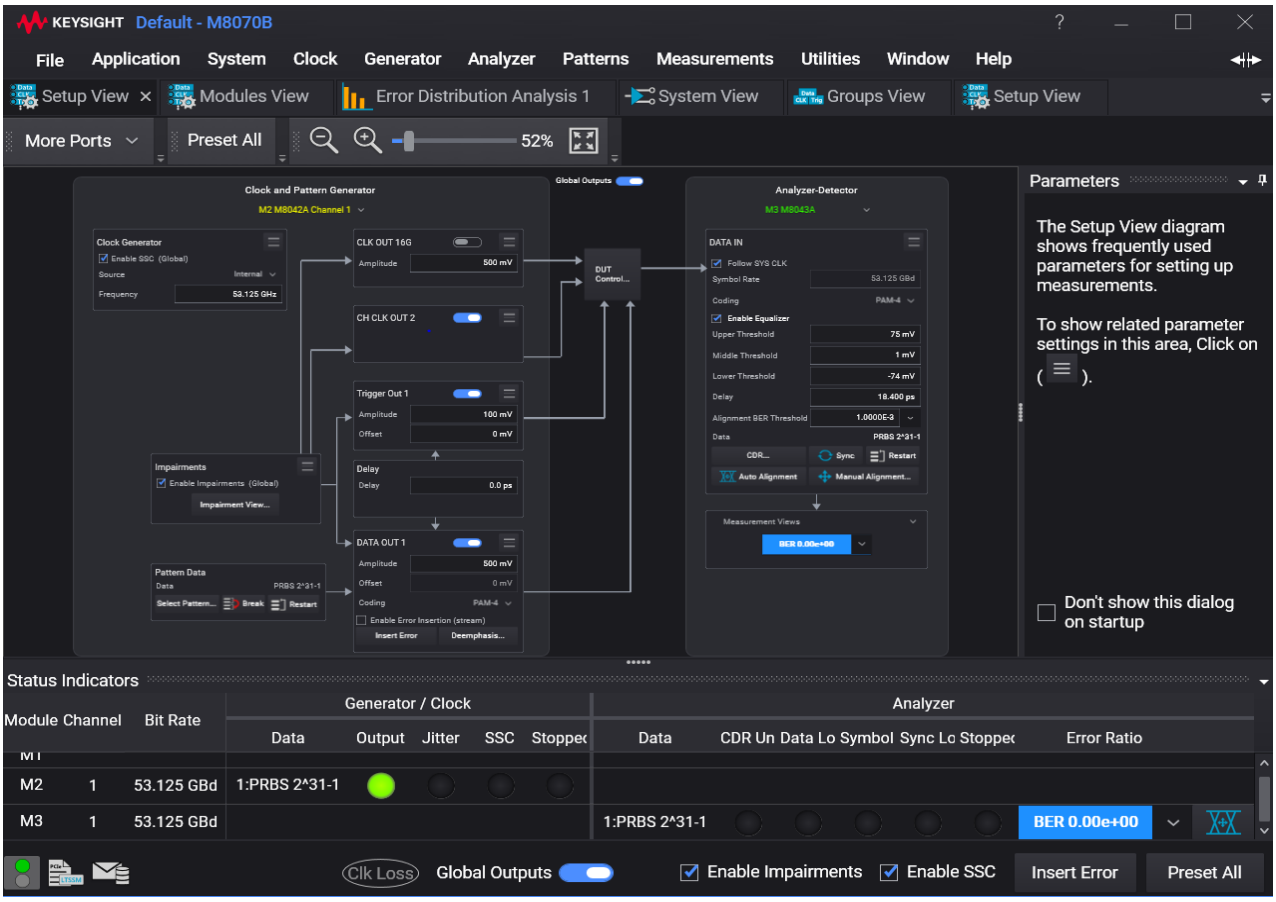


Figure 35. The M8070B system software is required to control the M8050A BERT. The user interface provides control of all parameters. It provides a graphical user interface and remote control via SCPI. Shown is the setup view with the M8040A BERT modules.

Unified Instrument Control and Test Configuration

The M8070B software offers a single, coherent environment for configuring complex BERT test setups. It manages instrument discovery, parameter configuration, synchronization, and timing alignment across all connected M8000 modules and supported external instruments.

Key configuration capabilities include:

- Pattern selection and sequence control
- Error detector configuration and BER measurement setup
- Clocking, triggering, and synchronization control
- Interference and noise source coordination
- Equalization and de-embedding configuration

Pattern-Based BER Analysis and Measurement Automation

The M8070B supports advanced pattern-based BER measurements using hardware error analyzers as well as real-time oscilloscopes for very high symbol rates. The software handles pattern alignment, synchronization, and comparison against the expected data stream, including long PRBS sequences such as PRBS31Q.

Integrated automation features include:

- Sequencer-based test execution
- Measurement state control and conditional branching
- Automated sweeps and stress conditions
- Deterministic triggering and event handling

High-Speed Equalization and Channel Compensation

To support reliable error analysis across lossy and impaired channels, the M8070B provides software control of advanced equalization and compensation functions. This includes configuration of transmitter and receiver equalization, backchannel de-embedding, and pattern-aware optimization.

The software supports:

- Control of FIR, FFE, and CTLE-based equalization
- Channel response measurement and coefficient calculation
- Compensation of channel loss, skew, and dispersion
- Pattern-based equalization optimization at very high symbol rates

Support for External Instruments and Extended Baud Rates

For symbol rates beyond the capability of hardware error analyzers, the M8070B seamlessly integrates with Keysight Infiniium real-time oscilloscopes, including the UXR-Series. In this configuration, captured waveforms are decoded into pattern streams and analyzed by the M8070B using the same pattern-based BER framework.

Scalable Architecture and Future-Ready Design

The M8070B system software is designed as a scalable and modular platform, supporting current and future M8000 hardware modules and applications. Software options enable expansion from basic BER testing to advanced jitter tolerance, link training, and stress testing scenarios.

Its architecture supports:

- Multi-module and multi-channel test configurations
- Future feature and standard support via software updates
- Integration into automated test systems and lab environments

Table 34. User interface and remote-control interface.

Parameter	Value
Controller requirements	Embedded PC: Choose M8040A-BU1 or -BU3 for a pre-installed embedded controller M9537A including pre-installation of M8070B software and module licenses. M8040A-BU3 is pre-configured with Windows 10 IoT Enterprise. Otherwise: M9537A 1-slot AXIe embedded controller, choose options for Windows 10 or 16 GB RAM, SSD. External PC: USB connection recommended between external PC and AXIe chassis. Minimum of 8 GB RAM recommended For PCIe connectivity please refer to list of supported PCs for AXIe Technical Note, pub no. 5990-7632EN
Operating system	Windows 10 IoT Enterprise Windows 11
Controller connectivity with AXIe chassis	USB 2.0 (Mini-B) recommended, PCIe 2.0/8x (for highest data throughput and desktop PC)
Programming language	SCPI. Not compatible with N4900 Series and ParBERT 81250A
Remote control interface	Desktop or Laptop PC: LAN M9537A: LAN
Save/Recall	Yes
Software update	Under the help menu the M8070B can show if there are newer SW revisions of M8070B, M8070ADVB, M8070ISIB, M8070EDAB, and module driver packages available for download from keysight.com.
SCPI recorder [1]	Allows recording of the SCPI commands that correspond to the interactive control in the GUI. This includes: • Parameter changes • Sequence and pattern configuration • Measurement creation, configuration and execution • Group configuration • Save and recall of settings The recorded SCPI commands can be copied to the clipboard or saved to a file for later playback.
Display resolution	Minimum requirement 1024 x 768

Software pre-requisites	Keysight IO Libraries Suite 2024 Update 2 Build 21.1.17 or newer M9505A AXIe 5-slot chassis firmware: Version 2.1.6 or newer M9502A AXIe 2-slot chassis firmware: Version 2.1.6 or newer .
Software download	See www.keysight.com/find/m8070b for the latest version

1. M8070B V7.2 or higher, older versions included in M8070ADVB

M8070ADVB Advanced Measurement Software Package

Table 35. Functions provided by the M8070ADVB Advanced Measurement Software Package.

Parameter	Value
Measurements	See table measurements
Export of measurement results	Jitter tolerance results as *.csv file
Controlling other instruments via M8070B	External clock recovery units, e.g. N1076A, N1076B, N1077A, N1078A Real-time oscilloscopes, e.g. DSAZ634A, UXR0334A
Scripting interface	The built-in scripting engine is based on IronPython. It enables the control of the device under test as well as other test equipment. Function hooks are available to tailor your measurements, such as read-out of built-in error counters or initializing the device
DUT control interface	Enables access to built-in error counters and status registers of a device under test (BIST) for use with automated measurements like accumulated BER and jitter tolerance. Can also be used to customize the measurements to DUT specific needs. IronPython scripting and .NET libraries are supported to interface with the DUT. Example scripts to read the BER from N4891A or G800GE module tester or to manually enter the BER are available.
Auto-optimizing de-emphasis taps	De-emphasis taps are calculated to maximize eye height or optimize the TDECQ value. Can be combined with embedding/de-embedding of S-parameter files. The following oscilloscope models are supported: Infiniium UXR series real-time oscilloscope and N1060A, N1094A/B, N1092C/E, 86108B DCA sampling oscilloscopes. Requires M8070B rev 6.7 or later. Additionally, de-emphasis taps can be optimized to minimize the BER read from an error analyzer or from the DUT Control Interface.
Software pre-requisites	M8070B version 6.0 or later
License types	Choose between node-locked, transportable, network, USB-dongle license types either perpetual or time-based with 6/12/24 month duration. The network license is only recommended when using multiple M8040A setups within one company.

The M8070ADVB Advanced Measurement Package supports the following measurements with the M8040A modules (M8045A and M8046A):

Table 36. Measurements of the M8070ADVB Advanced Measurement Package w.

Measurement	What it shows	Value for the user
Output Timing	BER versus sampling delay (bathtub curve)	Fast view of the horizontal eye margin; for PAM4, available for debugging only

Jitter Tolerance	Maximum tolerated jitter amplitude versus jitter frequency, compared to editable templates	Automated, standards-oriented jitter tolerance characterization with pass/fail results
Parameter Sweep	BER versus any swept generator or analyzer parameter	Automated sensitivity and margin sweeps without scripting
BER-Based De-emphasis	BER for each de-emphasis preset or setting over time	Fast identification of the optimal transmitter equalization for the DUT

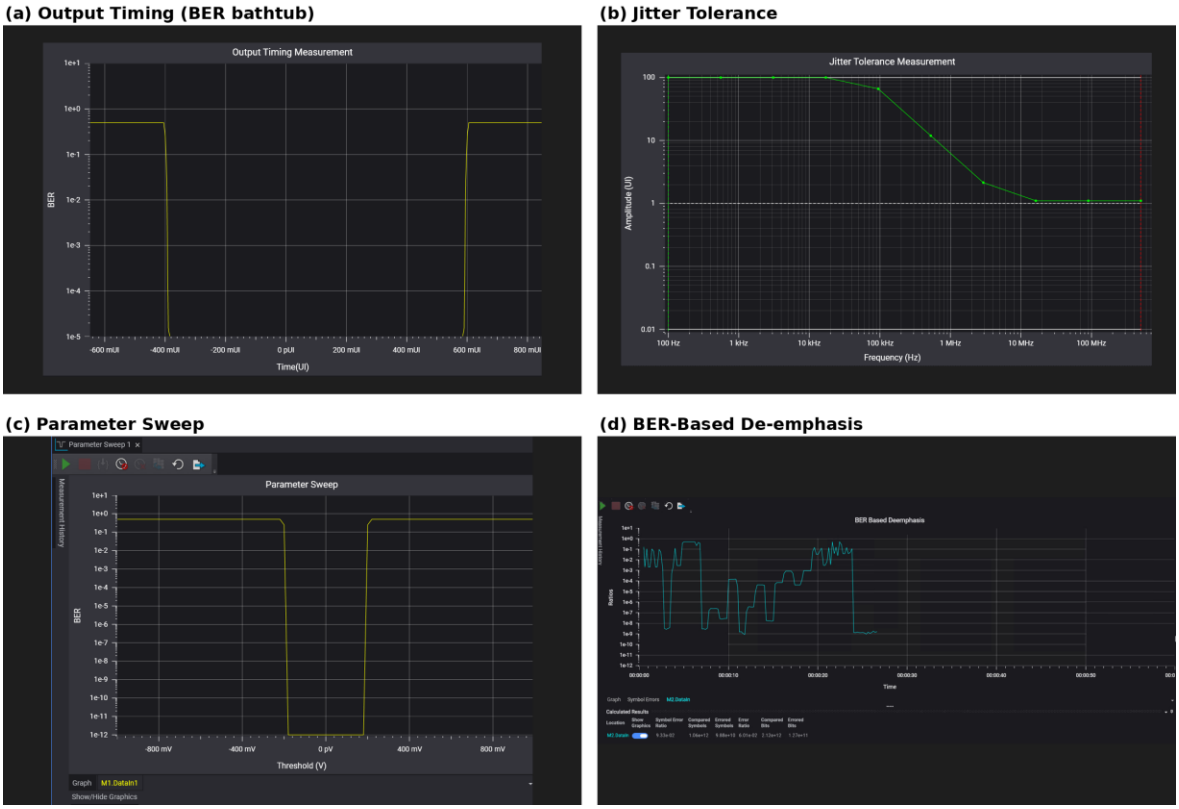


Figure 36. Examples of M8070ADVB measurement results in the M8070B: (a) output timing (BER bathtub), (b) jitter tolerance, (c) parameter sweep, and (d) BER-based de-emphasis.

In addition, the package provides utilities that extend the M8000 workflow:

- Script Editor for automating measurement sequences directly in the M8070B
- DUT Control Interface (DCI) for accessing the internal error counters of a DUT
- SCPI Editor for interactive remote-control development
- Control of external instruments: DCA sampling oscilloscopes for automatic de-emphasis optimization, N1076A/B, N1077A, and N1078A clock recovery units, and real-time oscilloscopes as error detectors

M8070EDAB Error Distribution Analysis Package

The M8070EDAB Error Distribution Analysis Package enables detailed analysis of where and how errors occur within a received data stream. It provides statistical evaluation of error distributions in

time, phase, and symbol position, allowing correlation of error events with jitter, noise, and signal impairments. This package is used for root-cause analysis of BER degradation and for identifying systematic error mechanisms in high-speed links.

Two links with the same pre-FEC BER can have a very different FEC margin. Random, isolated errors are easily corrected, whereas bursts of errors that concentrate many errored symbols in one codeword lead to uncorrectable frames. M8070EDAB shows not only how many errors occur, but also how they are distributed. This lets you measure or estimate the frame loss ratio (FLR) after FEC decoding and identify the root cause of burst errors.

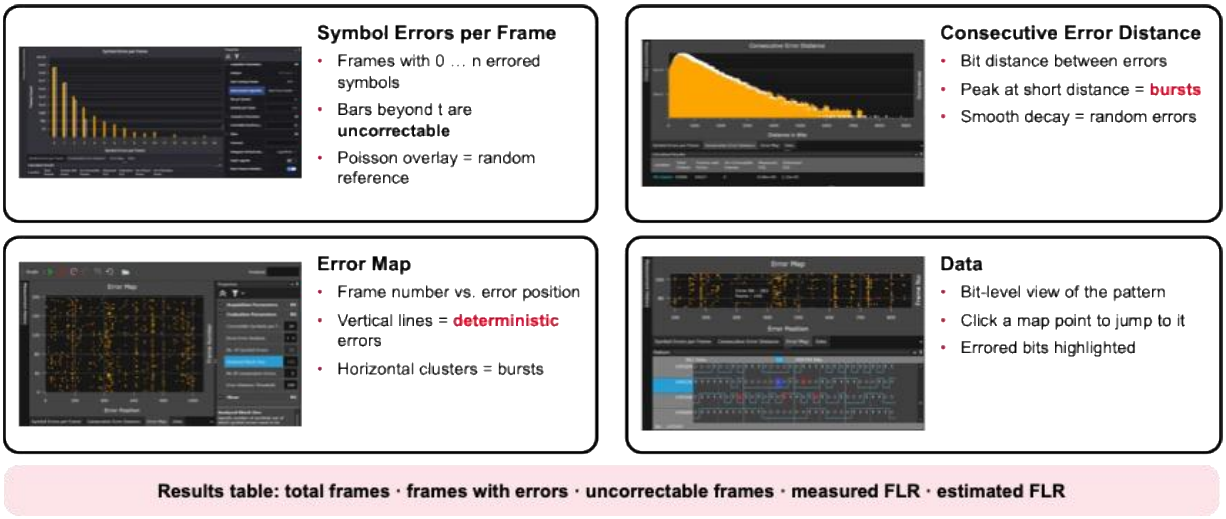


Figure 37. Four views of the M8070EDAB: symbol errors per frame with uncorrectable threshold and Poisson reference, consecutive error distance, error map, and bit-level data view.

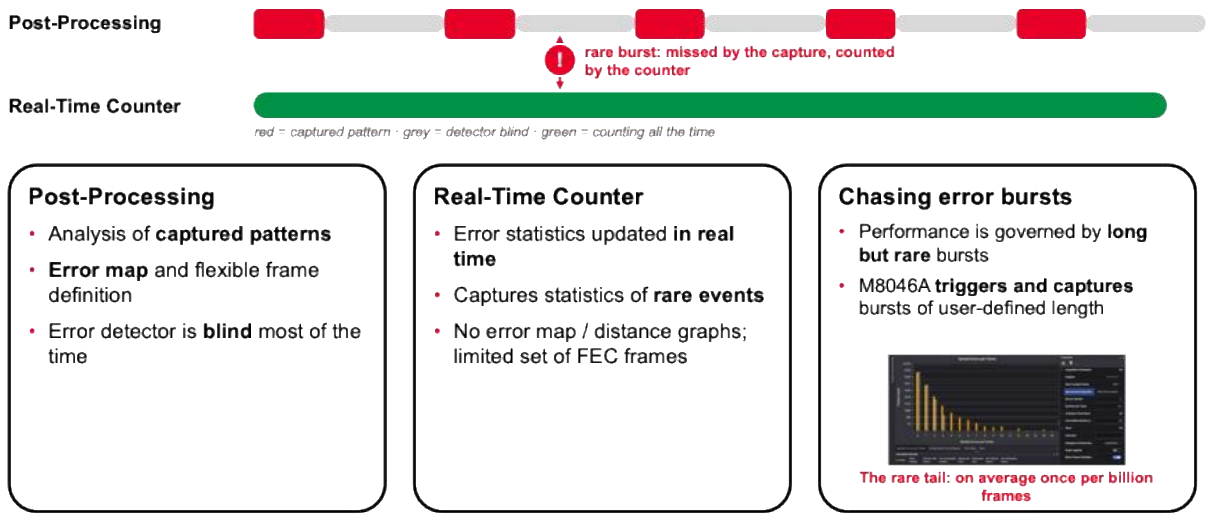


Figure 38. Two algorithms: Post Processing of captured patterns (error map and flexible frame definition) and Real Time Counter for statistics of rare events over long measurement times.

Key capabilities

- Error statistics: errored symbols per frame, consecutive error distance, error map, and a results table with total frames, frames with errors, uncorrectable frames, and measured and estimated FLR
- User-defined framing for any coding scheme: 1 to 10,000 bits per symbol, 1 to 10,000 symbols per frame, and an adjustable number of correctable symbols per frame; presets for KP4, KR4, and PRBS framing
- Two algorithms: Post Processing of captured patterns (error map and flexible frame definition) and Real Time Counter for statistics of rare events over long measurement times
- FBER for PCIe 6.0 and 7.0 in Real Time Counter mode, for example with 2 bits per symbol and 1024 symbols per frame (one flit)
- Burst error capture with the M8046A error analyzer: trigger on a user-defined burst and capture up to 2 Gbit around the event
- Offline analysis of pattern files, measurement history, and SCPI remote control

Table 37. What M8070EDAB adds beyond pre-FEC BER and host FEC counters.

Capability	Pre-FEC BER only	Host FEC counters	M8070EDAB with M8000 BERT
Random vs. bursty vs. deterministic errors	No	Partial: counts only	Yes: errors per frame, error distance, error map
Inspection of errored patterns	No	No	Yes: from error map to bit view
Any coding and framing	Not applicable	Fixed to host PCS/PMA	Yes: user-defined symbols and frames
Rare burst capture	No	Limited	Yes: trigger and capture of up to 2 Gbit
Offline analysis of files	No	No	Yes: pattern files
Standards in one tool	Not applicable	One per device	KP4, KR4, PRBS, and PCIe flit FBER

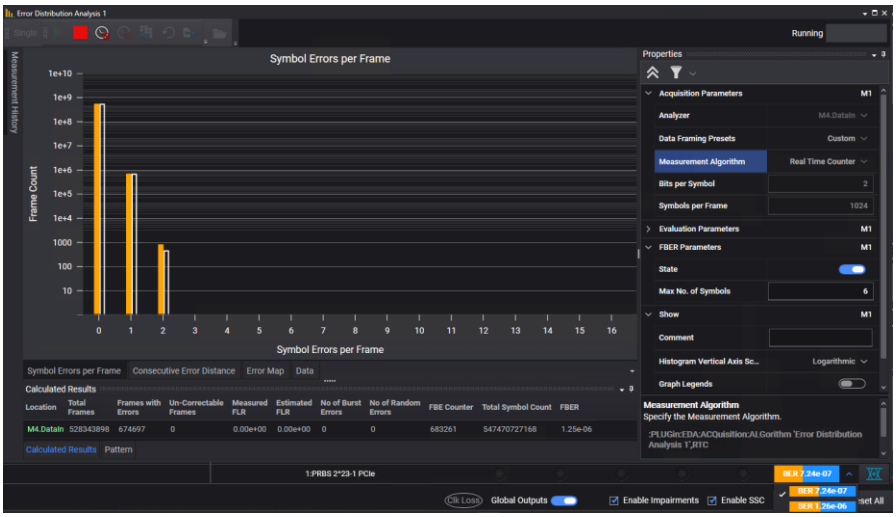


Figure 39. Error distribution analysis: PCIe 6.0 64 GT/s BER & FBER measurements before FEC decoding.

General Characteristics and Physical Dimensions

Modules M8045A and M8046A

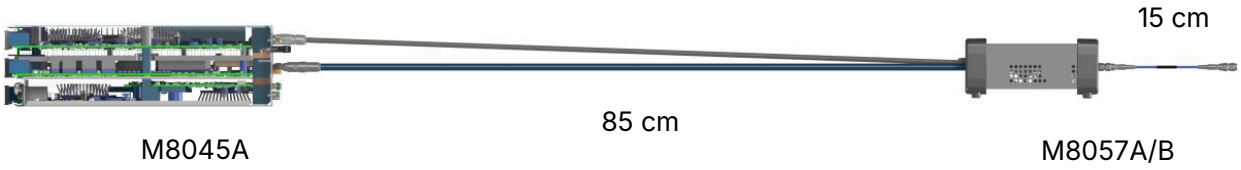
Table 38. General characteristics for M8045A and M8046A modules.

Parameter	Value M8045A	Value M8046A
Operating temperature	5 to 40 °C (41 to + 104 °F)	
Storage temperature	–40 to +70 °C (modules) (–40 to + 158 °F)	
Operating humidity	15 to 95% relative humidity at 40 °C (non-condensing)	
Storage humidity	24 to 90% relative humidity at 65 °C (non-condensing)	
Power requirements (module only) (W x H x D)	Single channel: 515 W Dual channel: 605 W	238 W
Physical dimensions for modules (W x H x D)	3-slot AXIe module: 351 x 92 x 315 mm (13.8 x 3.6 x 12.4 inch)	1-slot AXIe module: 351 x 30 x 309 mm (13.8 x 1.2 x 12.2 inch)
Physical dimensions for M8040A-BU1/-BU2 (W x H x D)	Installed in 5-slot AXIe chassis: 462 x 193 x 446 mm (18.2 x 7.6 x 17.6 inch)	
Weight net	M8045A module: single channel 6.9 kg (15.2 lb) M8045A dual channel: 7.5 kg (16.5 lb) With M8040A-BU1: 25 kg (55 lb) With M8040A-BU2: 21 kg (46.3 lb)	M8046A module: 3.6 kg (8.0 lb) In bundle with M8045A and in a 5-slot chassis: 24.6 kg (54.3 lb)
Weight shipping	M8045A module: 11 kg (24 lb) With M8040A-BU1/-BU3: 37 kg (82 lb) With M8040A-BU2: 33 kg (73 lb)	M8046A module: 7.5 kg (16 lb) In bundle with M8045A and in a 5-slot chassis M9505A: 37.6 kg (83 lb)
Recommend recalibration period	1 year	
Warm-up time	30 minutes	
Cooling requirements	Slot airflow direction is from right to left. When operating the M8045A/46A, choose a location that provides at least 50 mm of clearance at each side. See also the start-up guide for M9505/6A chassis.	
EMC	IEC 61326-1	
Safety	IEC 61010-1	
Quality	ISO 9001, 14001	

Remote Head M8057A/B

Table 39. General characteristics for M8057A/B remote head.

Parameter	Value
Operating temperature	5 to 40 °C (41 to + 104 °F)
Storage temperature	–40 to +70 °C (modules) (–40 to + 158 °F)
Operating humidity	15 to 95% relative humidity at 40 °C (non-condensing)
Storage humidity	24 to 90% relative humidity at 65 °C (non-condensing)
Physical dimensions (W x H x D)	Remote head 117 mm x 68 mm x 185 mm, (4.6″ x 2.7″ x 7.3″)
Physical dimensions for remote head with cable	Length of cable connection between M8057A/B and M8045A module: 85 cm



Weight net	1.7 kg (3.75 lb)
Weight shipping	6.5 kg (14.4 lb)
Recommended recalibration period	1 year
Warm-up time	30 minutes
EMC	IEC 61326-1
Quality management	ISO 9001, 14001

Specification Assumptions

The specifications in this document describe the instruments' warranted performance. Non-warranted values are described as typical. All specifications are valid in the specified operating temperature range after the warm-up time and after auto-adjustment. If not otherwise stated, all outputs need to be terminated with 50 Ω to GND.

All M8045A specifications, if not otherwise stated, are valid at the end of the cable **M8045A-801** (included with M8045A shipments).

All M8046A specifications, if not otherwise stated, are valid using the **M8046A-802** (2.4 mm matched cable pair). The M8046A-802 is included with M8046A shipments.

Specification (spec.)

Warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of **0 °C to 40 °C** and after a **15-minute warm-up period**. Specifications are valid within **±10 °C** following auto-calibration. All specifications include measurement uncertainty and are established in compliance with **ISO 17025** methods. Performance values in this document are specifications only where explicitly identified as such.

Typical (typ.)

Characteristic performance that **80 % or more** of manufactured instruments are expected to meet. Typical values are **not warranted**, do not include measurement uncertainty, and are valid only at **room temperature (approximately 23 °C)**.

Nominal (nom.)

The mean or average characteristic performance, or a value defined by design, such as connector type, physical dimension, or operating speed. Nominal values are **not warranted** and are measured at **room temperature (approximately 23 °C)**.

Measured (meas.)

A parameter measured during development to indicate expected performance. Measured values are **not warranted** and are valid only at **room temperature (approximately 23 °C)**.

Accuracy

Represents the traceable accuracy of a specified parameter. Accuracy includes measurement error, time-base error, and calibration source uncertainty.

Ordering M8040A High-Performance BERT

The M8040A is scalable and upgradeable. The following table shows all available options. Upgrade options are shown below.

Description	Product #	Option	Comment
High-Performance BERT 64 Gbaud (systemizing number for factory pre-installation)	M8040A		
Pattern generator and clock module, 32/64 Gbaud, 3-slot AXIe	**M8045A**		
Pattern generator one channel NRZ, data rate up to 32 Gbaud	M8045A	G32	One of these is required (requires remote head, M8057A/B)
Pattern generator one channel NRZ, data rate up to 64 Gbaud	M8045A	G64	
Second channel, hardware and license (requires remote head, M8057A/B)	M8045A	0G2	
Advanced jitter sources for receiver characterization, module-wide license	M8045A	0G3	
De-emphasis, module-wide license	M8045A	0G4	
Reference clock multiplier, module-wide license	M8045A	0G6	
Forward Error Correction (FEC) encoding, module-wide license	M8045A	0G9	
Extended calibration for 50G PON, module-wide license	M8045A	0G8	No upgrade possible
PAM4 encoding up to 32 Gbaud, module-wide license	M8045A	0P3	
Extension to PAM4 encoding up to 64 Gbaud, module-wide license	M8045A	0P6	Only with G64, 0P3/UP3
Short cable 1.85 mm (m) to 1.85 mm (m), 0.15 m, absolute matching 699 ps ± 1 ps	M8045A	801	Included in M8057B-KIT and M8040A-KIT-003
Remote head for M8045A pattern generator, 1 channel	M8057A		
Analyzer module, 32/64 Gbaud, 1-slot AXIe	**M8046A**		
Analyzer, one channel, data rate up to 32 Gbaud, NRZ	M8046A	A32	
Analyzer, one channel, data rate up to 64 Gbaud, NRZ	M8046A	A64	
Equalization, license (only needed for > 32 Gbaud)	M8046A	0A3	Only with A64
PAM4 decoding up to 32 Gbaud, license	M8046A	0P3	
PAM4 decoding extension to 58 Gbaud, license	M8046A	0P6	Only with A64, 0P3, 0A3
Clock recovery for 32 Gbaud, license	M8046A	0A4	
Clock recovery extension to 64 Gbaud, license	M8046A	0A5	Only with A64 and 0A4
Interactive link training for PCIe, license	M8046A	0S1	Requires 0A4, 0G4
SKP OS filtering for PCIe and CCIX, license	M8046A	0S2	
Interactive link training for USB 3.2, license	M8046A	0S3	Requires 0A4
SKP OS filtering for USB 3.x, license	M8046A	0S4	Opt. 0A4 recommended
ALIGN filtering for SATA 3/6G, SAS 3/6/12G, license	M8046A	0S6	Opt. 0A4 recommended
Interactive link training extension for PCIe 64 GT/s, license	M8046A	0N1	Opt, 0S1/US1 required
PCIe Filtering of SKP OS Extension for 64 GT/s	M8046A	0N2	Opt. 0S2, Opt. 0S1, Opt. 0N1 are required
Cable 2.92 mm (m) to 2.92 mm (m), 0.5 m for clock input	M8046A	801	Qty 1 recommended
Matched cable pair 2.4 mm (m) to 2.4 mm (m), length 0.85 m	M8046A	802	Included in M8046A-KIT and M8040A-KIT-002.
Software and chassis			
System software for M8000 Series	M8070B	unlicensed	
Advanced measurement package	M8070ADVB	1FP/1TP/ 1NP/1UP [1]	
Error distribution analysis package	M8070EDAB	1FP/1TP/ 1NP/1UP [1]	
Adjustable ISI package	M8070ISIB	1FP/1TP/ 1NP/1UP[1]	
5-slot AXIe chassis with USB option	M8040A	BU2	
5-slot AXIe chassis with USB option and embedded controller M9537A	M8040A	BU3	Not recommended due to Windows 10 OS
5-slot AXIe chassis with USB option and embedded controller M9538A	M8040A	BU7	

1. Multiple types of licenses are available. Choose between 6/12/24 month support subscriptions.

Default Accessories Included with Shipments

Item	Shipping Kit Contents
M8045A module	Four 50 Ω terminations, two M8045A-801 short cables for remote head (reference cables), ESD protection kit, certificate of calibration, license entitlement certificate.
M8046A module	One bandpass filter for clock input, M8046A-802 matched cable pair, ESD protection kit, certificate of calibration, license entitlement certificate, one M8051A-801 cable for LINK 1234 connection.
M8057A/B remote head	Includes cable connection to M8045A pattern generator module, one 50 Ω termination (2.4 mm).
M8040A-BU2	Bundle M9505A AXIe chassis, USB cable, getting started guide, AXIe filler panel(s), power cord.
M8040A-BU3	Bundle M9505A AXIe chassis with embedded controller, Windows 10 installed, USB cable, getting started guide, AXIe filler panel(s), power cord.
M8040A-BU7	Bundle M9505A AXIe chassis, M9538A embedded controller module, Windows 11 installed, USB cable, getting started guide, AXIe filler panel(s), power cord.
M8070B	CD-ROM with M8070B system software

Recommended Accessories

Part Number	Description
M8045A-801 [1]	Short cable, 1.85 mm (m) to 1.85 mm (m), 0.15 m, 699 ps delay ± 1 ps (two are recommended for each differential data output of M8057A/B)
M8046A-802 [2]	Matched cable pair 2.4 mm (m) to 2.4 mm (m), 2 ps, length 0.85 m (recommended for data input of M8046A analyzer)
M8046A-801	Cable 2.92 mm (m) to 2.92 mm (m), 0.5 m (recommended for clock input of M8046A analyzer)
M8051A-801	M8000 sync cable (when using the system clock of M8045A for M8046A) and LINK 1234 connection
8490G-006	Attenuator, 6 dB, 1.85 mm
N9398F	DC block 2.4 mm
M8045A-802	Matched directional coupler pair, 1 to 50 GHz, 13 dB, 2.4 mm (recommended for external interference source RI/SI)
M8045A-803	Matched coupler pair, DC to 50 GHz, 12 dB, 2.4 mm (recommended for PCIe)
M8061A-803	Bandpass filter 11.1 to 17.5 GHz, SMA (for M8046A clock input)
N1027A-2P2	Microwave pick-off tees, 2.4 mm, matched pair (Qty 1 is recommended for use with N1076A/77A)
N1027A-2P8	Microwave pick-off tees, 1.85 mm, matched pair (Qty 1 is recommended for use with N1076B/N1078A up to 32 Gbaud)
N1027A-2P1	Microwave pick-off tees, 1.0 mm, matched pair (Qty 1 is recommended for use with N1076B/N1078A above 32 Gbaud)
11921G	Adapter 1.0 mm (m) to 1.85 mm (m) (Qty 2 is recommended for use with pick-off tees N1027A-2P1)
11921F	Adapter 1.0 mm (f) to 1.85 mm (f) (Qty 2 is recommended for connecting data cables to pick-off tee N1027A-2P1)
11900B	Adapter 2.4 mm (f) to 2.4 mm (f) (Qty 2 is recommended for connecting cables to pick-off tees)
83059A	Adapter 3.5 mm (m) to 3.5 mm (m) (Qty 2 is recommended for connecting pick-off tees directly to N1076A/77A inputs)
11904C	Adapter 2.92 mm(f) to 2.4 mm (m)
11904D	Adapter 2.92 mm (m) to 2.4 mm (f)
Y1226A	Rack-mount kit for AXIe 5-slot chassis M9505A
M8047C	PCI Express Re-driver recommended for PCI Express testing up to 64 GT/s

[1] Two Included in standalone M8057B-KIT & system shipment M8040A-KIT-003
[2] Included in standalone M8046A-KIT and system shipment M8040A-KIT-002

M8040AU Upgrades

All upgrades for M8040A High-Performance BERT 64 Gbaud are available through the special part number M8040AU.

Description	Product #	Option	Comment
Upgrades for M8040A High-Performance BERT 64 Gbaud	M8040AU		
M8045A Pattern generator and clock module, 32/64 Gbaud, 3-slot AXIe			
Upgrade to 64 Gbaud	M8045A	U64	License
Upgrade to second channel, hardware and license (requires remote head, M8057A/B)	M8045A	UG2	Requires return-to-factory
Upgrade to advanced jitter sources for receiver characterization, module-wide license	M8045A	UG3	License
Upgrade to de-emphasis, module-wide license	M8045A	UG4	License
Upgrade to reference clock multiplier, module-wide license	M8045A	UG6	Requires return-to-factory for S/N <MYxxx01000
Upgrade to Forward Error Correction (FEC) encoding, module-wide license	M8045A	UG9	License
Upgrade to PAM4 encoding up to 32 Gbaud, module-wide license	M8045A	UP3	License
Upgrade to extension to PAM4 encoding up to 64 Gbaud, module-wide license	M8045A	UP6	Only with G64/U64/UP3
Remote head for M8045A pattern generator, 1 channel	M8057B		
M8046A Analyzer module, 32/64 Gbaud, 1-slot AXIe			
Upgrade M8046A for data rates up to 64 Gbaud, NRZ	M8046A	U64	Requires return-to-factory
Upgrade to equalization, license	M8046A	UA3	Only with A64/U64
Upgrade to PAM4 decoding up to 32 Gbaud, license	M8046A	UP3	License
Upgrade to PAM4 decoding extension to 58 Gbaud, license	M8046A	UP6	Requires return to factory for S/N < MYxxx02000. Requires A64/U64, 0A3/UA3 and 0P3/UP3
Upgrade to clock recovery 32 Gbaud, license	M8046A	UA4	Requires return to factory for S/N<DExxx01000.
Upgrade to clock recovery extension to 64 Gbaud, license	M8046A	UA5	Only with A64/U64
Upgrade to interactive link training for PCIe, license	M8046A	US1	Requires -0A4/-UA4. Requires return to factory for S/N<MYxxx01000
Upgrade to SKP OS filtering for PCIe and CCIX, license	M8046A	US2	License
Upgrade to interactive link training for USB 3.2	M8046A	US3	License
Upgrade to SKP OS filtering for USB 3.x, license	M8046A	US4	License
Upgrade to ALIGN filtering for SATA/SAS and CCIX, license	M8046A	US6	License
Upgrade to interactive link training for PCIe 64 GT/s, license	M8046A	UN1	Opt 0S1/US1 required
Upgrade to PCIe Filtering of SKP OS Extension for 64 GT/s, license	M8046A	UN2	S/N > MYxxxx1000, -0S2/US2 required

Related Keysight Literature

Product Data Sheets, Technical Overviews, and Configuration Guides

Description	Publication Number
XE8-class M8050A High-Performance BERT 120 GBd – Data Sheet	3122-1338.EN
XE8-class M8050A High-Performance BERT 120 GBd – Configuration Guide	3122-1285.EN
XE8-class M8050A High-Performance BERT 120 GBd – Technical Overview	Coming Soon
XE7-class M8040A High-Performance BERT 64 GBd – Data Sheet	5992-1525EN
XE7-class M8040A High-Performance BERT 64 GBd – Configuration Guide	Coming Soon
XE5-class J-BERT M8020A High-Performance BERT – Data Sheet	5991-3647EN
M8053A Interference Source 64 GHz – Data Sheet	3124-1184.EN
M8054A Interference Source 32 GHz – Data Sheet	5992-3917EN
M8049A ISI Channel Boards – Data Sheet	5992-3617EN
M8067A ISI Channel Boards – Data Sheet	3122-2261.EN
M9502A and M9505A 2- and 5-slot AXIe Chassis – Data Sheet	5990-6584EN
M9506A High-Performance 5-slot AXIe Chassis – Data Sheet	5992-3786EN
M9538A AXIe Embedded Controller – Data Sheet	3125-1003.EN
M8047C PCIe Redriver for 32 GBd – Data Sheet	3124-1732.EN
N7718C Optical Reference Transmitter – Data Sheet	3124-1652EN
Infiniium UXR-Series Oscilloscopes – Data Sheet	5992-3132EN
N1000A DCA-X Sampling Oscilloscope Platform – Data Sheet	5992-3271EN

Test Automation Software Data Sheets

Description	Publication Number
N5992DP2A DisplayPort 2.1 Receiver Test Automation Software – Data Sheet	3124-1689.EN
N5992U42A USB4 Version 2.0 Receiver Test Automation Software – Data Sheet	3125-1034.EN
N5992U32A USB 3.2 Receiver Test Automation Software – Data Sheet	3125-1425.EN
N5991P PCI Express Receiver Test Automation Platform – Data Sheet	5992-4365EN
M8091BSCB Receiver Test Automation Software for IEEE 802.3bs/cd – Data Sheet	3124-1256.EN
M809256CB Receiver Test Automation Software for OIF-CEI 4.0 (56G) – Data Sheet	3124-1257.EN
M809212CA Receiver Test Automation Software for OIF-CEI 5.0, CEI-LINEAR, LPO-MSA	3123-1849.EN
M8091CKCA Receiver Test Automation Software for IEEE 802.3ck – Data Sheet	3122-2122.EN
M8091DJCA Receiver Test Automation Software for IEEE 802.3dj – Data Sheet	3125-1419.EN
N4917BSCB 400/800G Optical Receiver Stress Test Automation Software – Data Sheet	5992-4040EN
N4917DJCA 1.6T Optical Receiver Test Automation Software – Data Sheet	3124-1643.EN

Application Notes, White Papers, and Posters

Description	Publication Number
BERT Applications – White Paper	5992-3479EN
BER Measurement with Real-Time Oscilloscope in M8070B Software – Application Note	5992-2676EN
Advanced Modulation and Coding Challenges – White Paper	5992-3021EN
Total Jitter Measurement at Low Probability Levels – Application Note	5989-2933EN
How Signal Equalization Works for Different Systems – White Paper	5989-3777EN
Error Analysis of PAM4 Signals – Application Note	5992-3268EN
Your Path to 1.6T – Poster	3123-1060EN
Conformance Testing of 800G Ethernet Links for the Data Center – Application Note	3121-1220.EN
Equalizer (Tx/Rx) Optimization at 112 Gbps – Application Note	3124-1727.EN
Race to 448 Gbps – White Paper	7125-1060.EN

Confidently Covered by Keysight Services

Prevent delays caused by technical questions or unplanned system downtime with Keysight Services. Keysight Services support your test operations with expert technical assistance, instrument repair and calibration, software support, training, flexible acquisition program options, and more.

KeysightCare agreements provide dedicated, proactive support through a single point of contact for your instruments, software, and solutions. Covering a broad portfolio of Keysight hardware and application software, KeysightCare helps maximize uptime with committed response times, direct access to experts, and efficient issue resolution.

Keysight Services Offering

Offering	Benefits
KeysightCare 	KeysightCare provides elevated support for Keysight instruments and software, with access to technical support experts that respond within a specified time and ensure committed repair and calibration turnaround times (TAT). KeysightCare offers multiple service agreement tiers, including KeysightCare Assured, Enhanced, and Application Software Support. See the KeysightCare data sheet for details.
KeysightCare Assured	KeysightCare Assured goes beyond basic warranty with repair services that include committed TAT and unlimited access to technical experts.
KeysightCare Enhanced	KeysightCare Enhanced includes all the benefits of KeysightCare Assured plus Keysight's accurate and reliable calibration services, accelerated and committed TAT, and technical response.
Keysight Support Portal & Knowledge Center	All KeysightCare tiers include access to the Keysight Support Portal where you can manage support and service resources related to your assets such as service requests and status or browse the Knowledge Center.
Education Services	Build confidence and gain new skills to make accurate measurements, with flexible Education Services developed by Keysight experts, including Start-up Assistance.
Alternative acquisition options	
KeysightAccess	Reduce budget challenges with a subscription service enabling you to get the instruments, software, and technical support you want for your test needs.

Recommended Services

Maximize your test system uptime by securing technical support, repair, and calibration services with committed response and turnaround times. **One-year KeysightCare Assured** is included with every new instrument purchase. Extend coverage by purchasing **multi-year KeysightCare upfront** to eliminate annual maintenance purchase cycles and administrative overhead, while ensuring secured service coverage for **2, 3, or 5 years**.

Service	Description
KeysightCare Enhanced *	**Includes technical and application support, warranty and calibration**
R-55B-001-1	KeysightCare Enhanced – Upgrade 1 year
R-55B-001-2	KeysightCare Enhanced – Extend to 2 years
R-55B-001-3	KeysightCare Enhanced – Extend to 3 years (Recommended)
R-55B-001-5	KeysightCare Enhanced – Extend to 5 years (Recommended)
KeysightCare Assured	**Includes technical and application support and warranty**
R-55A-001-2	KeysightCare Assured – Extend to 2 years
R-55A-001-3	KeysightCare Assured – Extend to 3 years
R-55A-001-5	KeysightCare Assured – Extend to 5 years
Start-Up Assistance	
PS-S10	Instrument fundamentals and operations starter
PS-S20	Optional, technology & measurement science standard learning

* Available in select countries. For details, please view the data sheet: KeysightCare Uptime, Precision, Expertise. At Your Service. R-55B-001-2/3/5 must be ordered with R-55B-001-1.



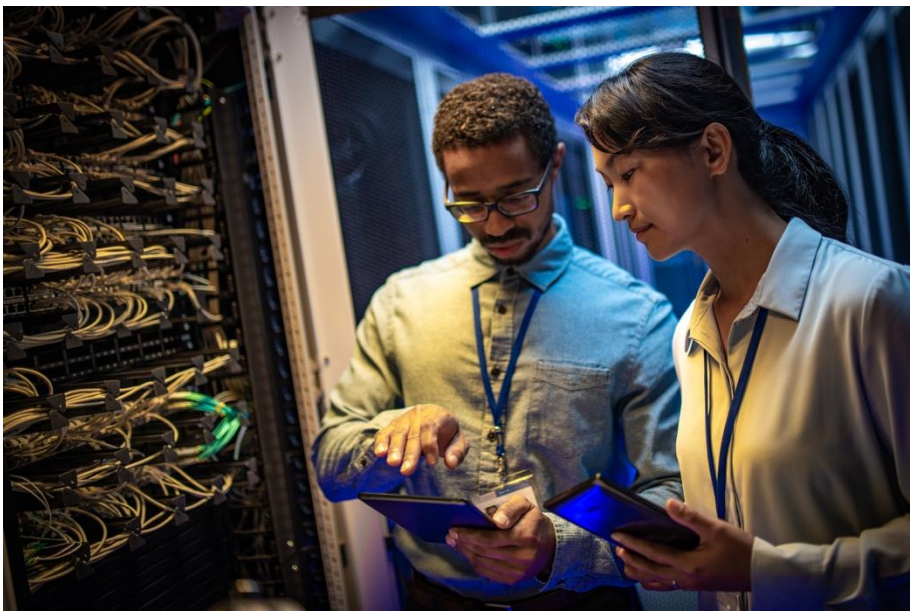
Solution Engineer Professional Services

Keysight Solution Engineer (SE) Professional Services provide expert, hands-on support to help you design, configure, and optimize complex test solutions with confidence. SE Professional Services can include system architecture consulting, application-specific test setup and validation, measurement methodology review, automation and software integration support, test optimization, on-site or remote troubleshooting, and tailored training for engineering teams.

By using deep domain expertise across high-speed digital, SerDes, optical, and protocol-specific applications, Keysight SE Professional Services help shorten time-to-results, improve measurement accuracy, and maximize return on your test investment.

Service	Description
PS-XPS-100/200/300	Solution Engineer Professional Services (Familiarization, Consulting)
PS-XSUP-006/012/018/024/036	Professional Services for Solution Support (6/12/18/24/36 months)
PS-XINS-100/200/300	Solution Engineer Installation Services
PS-XSUP-AESN1	Solution Engineer Productivity Services and Support Days Delivered Over 12 Months (from order or if attached to a solution, with solution delivery)

Ask your local Keysight representative to include any of these or other available services as part of your next M8040A BERT system order to maximize performance, uptime, and long-term value.





Keysight enables innovators to push the boundaries of engineering by quickly solving design, emulation, and test challenges to create the best product experiences. Start your innovation journey at www.keysight.com.

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